SUPPLEMENT TO

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OCTOBER 23, 1997

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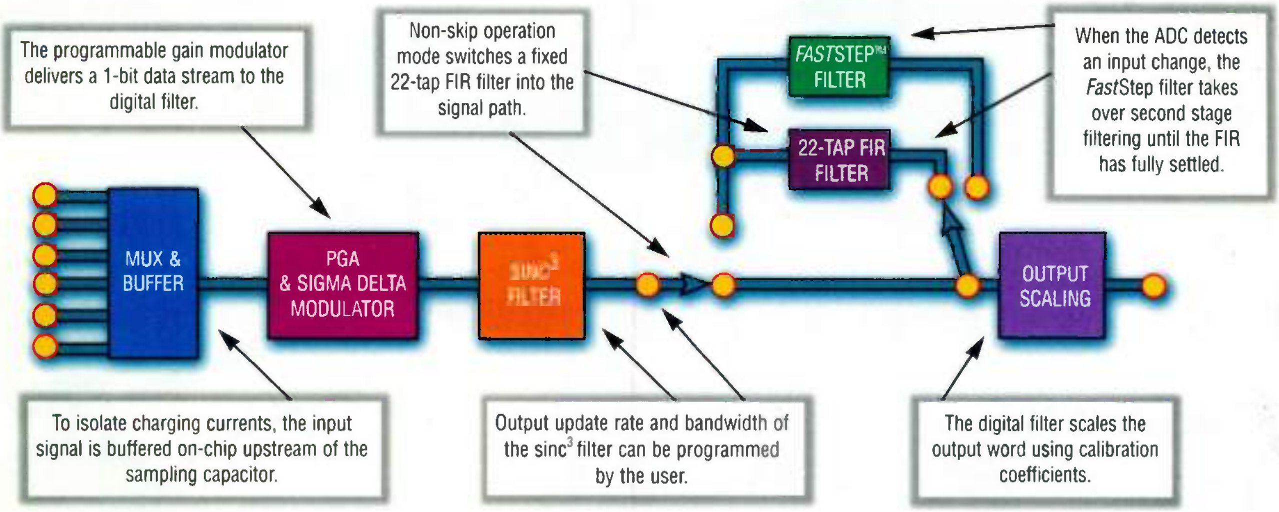
Optimize This 24-Bit ΣΔ ADC To Meet All Your Industrial Needs.



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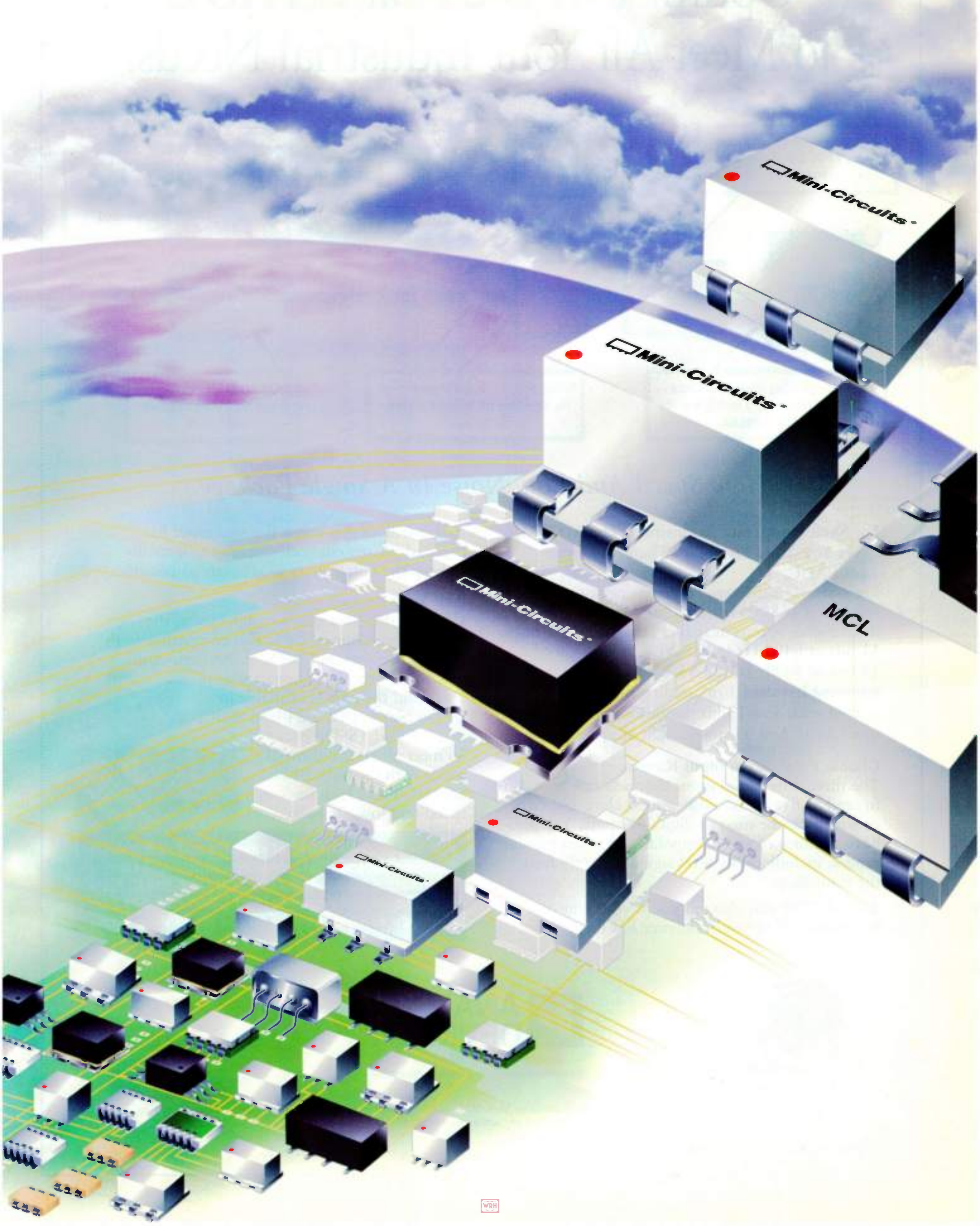
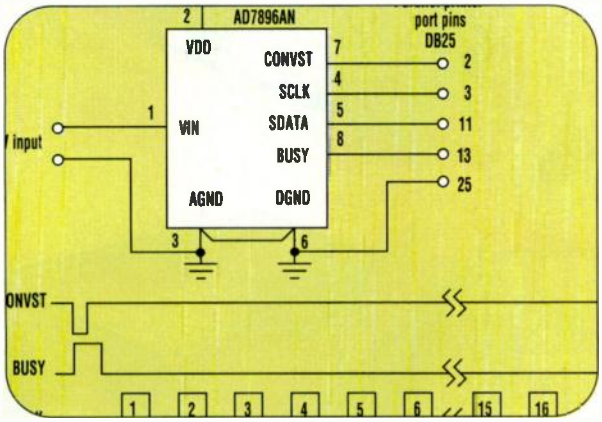


BEST IDEAS FOR DESIGN

IDEAS VOTED 'BEST OF ISSUE' BY THE READERS OF ELECTRONIC DESIGN

EDITORIAL DIRECTORY

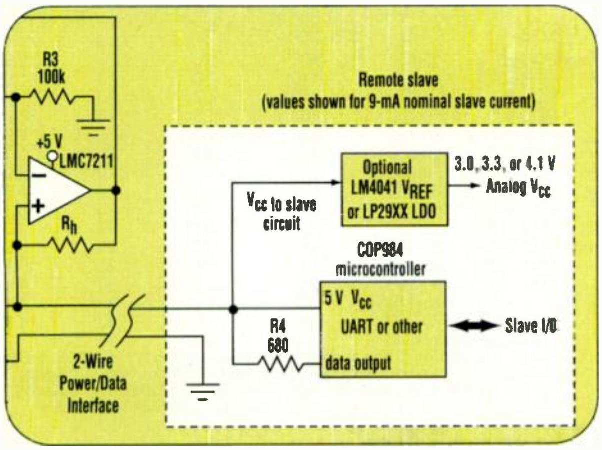


p. 12

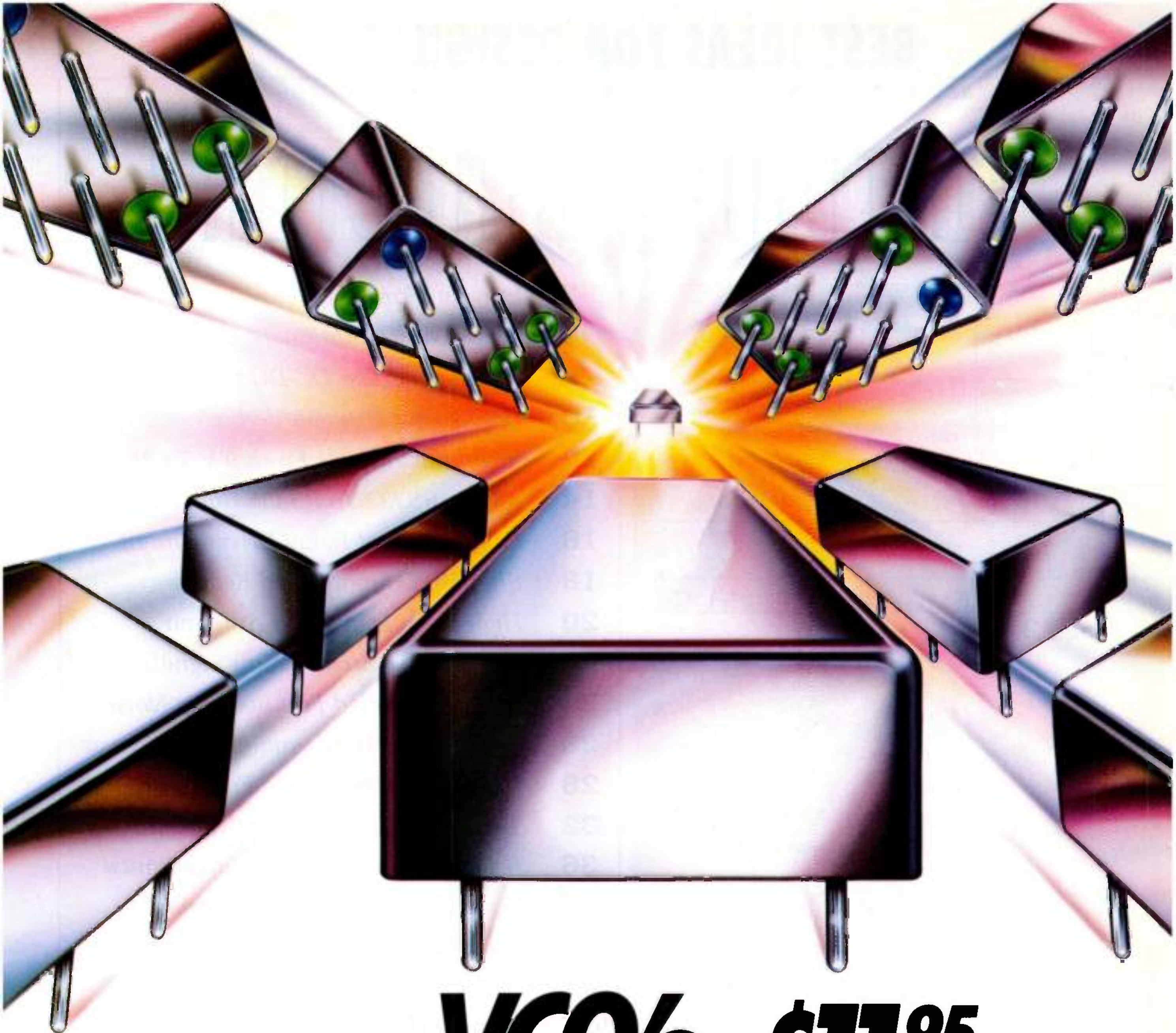
```
(a)

uses crt;
var a,e,f,g:integer
  begin
  clrscr;
  port[888]:=0;
  port[888]:=250;
  port[888]:=248;
  clrscr;
  for f:=1 to 8 do
   begin
   for g:=1 to 32 do
     begin
     port [888]: =249;
     delay(1);
     e:=port[889];
     a:=e and 128;
     if (a=128) then write ('0 ')
else write ('1 ');
     port[888]:=251;
     end;
   writeln;
    end;
```

p. 18



p. 32



INTRODUCTION

Welcome to the second annual collection of the best of Ideas For Design. The ideas contained in this supplement to Electronic Design pick up where last year's supplement (published with the October 24, 1996 issue) left off. In this issue, we begin with the Idea voted "Best of Issue" in the April 1, 1996 issue and move forward from there, including as many ideas as space allows.

The Ideas for Design section is truly the readers' section. Based on our many readership studies, we know that Ideas for Design is the best-read section in the magazine, along with the inimitable Bob Pease's Pease Porridge. However, the IFD section also is a place where every reader has a good chance of seeing his or her name in print, bylining an idea submitted for consideration in the section.

Publishing the section in each issue requires a steady supply of ideas coming in from readers. We do not solicit particular ideas for this section—it's whatever the mail, express services, e-mail, fax, or whatever, brings us each day.

We're not looking for literary masterpieces here—simply good design ideas logically described in a reasonable length and with reasonably sized illustrations. Our editors will take care of the writing style. As always, brevity is a virtue, and in fact, many ideas are returned to engineers because they simply are too long and would take up all the allowable space in the section. We re-draw all circuits to conform to our style, and our policy is to send all authors a copy of our redrawn circuits and graphs for the author to check them for accuracy. We also send authors a pre-publication edited copy of their text for review. Although our $100 honorarium for publication of an idea hardly compensates any engineer for the time and knowledge invested in developing the idea, it certainly doesn't make the process less attractive. Furthermore, earlier this year, we raised the additional amount we award to the winners of "Best of Issue" from $150 to $300.

Throughout this issue, you'll note that we have used small (otherwise blank) spaces to include a message encouraging readers to submit their ideas for possible publication in the Ideas for Design section. It's your section, and we're waiting to hear from you.

STEPHEN E. SCRUPSKI
Editorial Director

READER SERVICE 97

True RMS Operation Test

HERMAN P. RAAB, Engineering Services, 9140 Sherwood Ln., Indianapolis, IN 46240-1252; (317) 848-4950.

The following is a simple test to determine whether your voltmeter or DVM produces true RMS voltmeter readings—and it doesn't require using a second meter:

Connect a diode, such as a 1N4004, in series with the voltmeter and provide a switch to bypass the diode. If the meter's input impedance is greater than 100 kΩ, provide a bypass resistor of 33 k 1/2 W across the meter.

Then, using this circuit with the switch closed, measure the ac power-line voltage. Open the switch and take a second reading of the half wave rectified voltage on the ac power line. If the meter is a true RMS meter, the second reading will be 70.7% of the first reading. On the other hand, if the second reading is only 50%, this indicates that the meter is responding to the average instantaneous voltage and has been calibrated by the manufacturer to output a value equal to the RMS equivalent for a sine wave input and will produce erroneous RMS readings for nonsinusoidal inputs.

The mathematics of this test method is straightforward. First, for line voltages of greater than 100 V, the forward drop in the diode produces only a negligible error (less than 1%). The swamping resistor, if necessary, negates any small reverse leakage introduced by the diode. Discarding every other half cycle cuts the average of the instantaneous voltage of the ac power line in half, and also cuts in half the average of the square of the instantaneous voltage. The root of this mean square is the square root of 0.5 or 0.707.

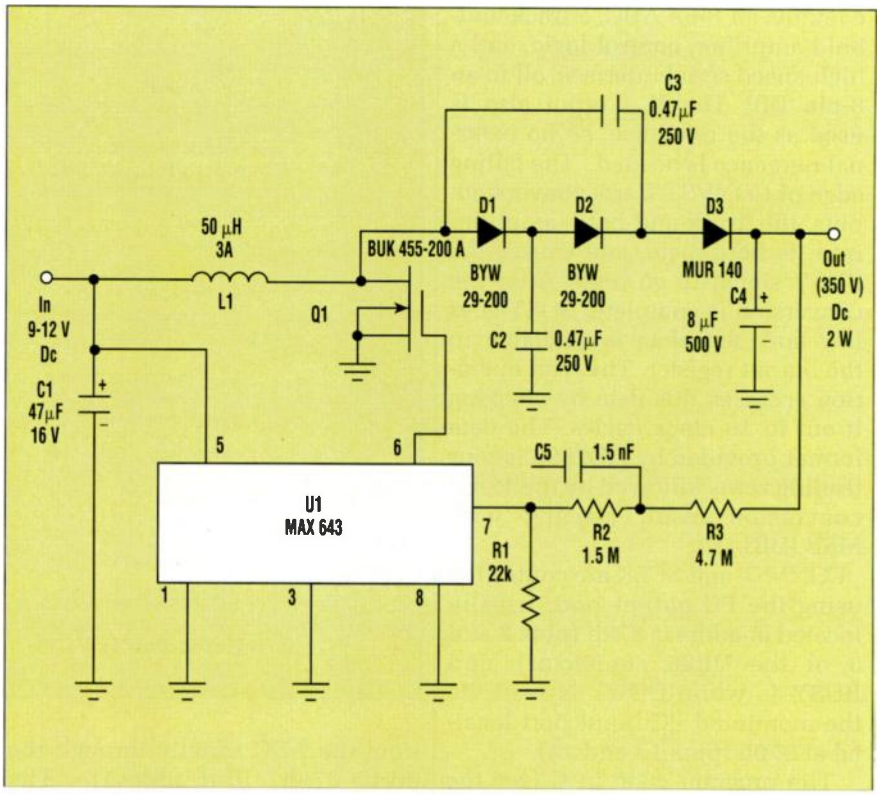
Voted "Best of Issue" Electronic Design, April 1, 1996

Transformerless DC-DC Converter

PATRICK GUEULLE, 55, Rue de Richelieu, B.P. 279, 76055 Le Havre, Cedex, France.

When used with an external MOSFET and diode, the Maxim MAX 643 step-up regulator can generate output voltages significantly higher than its input—typically 15 V from a 5-V power supply, and possibly much more with the addition of an external feedback voltage divider (see the figure).

A maximum output of 50 V is suggested, but voltages as high as 150 to 200 V can be achieved with an acceptable efficiency (greater than 50% with a careful design). An additional voltage-multiplying stage can easily be added in order to double (or more) the output voltage to 300, 350, or even 400 V. At the switching frequency of 45 kHz, the capacitors in the doubler stage need not be large. A 0.47-μF capacitor is sufficient for an output power of 2 W. All diodes should exhibit fast recovery times, and for D1 and D2, a high peak current rating. Since the inductor must withstand current peaks in excess of 3 A, a high saturation current is mandatory. Iron powder toroidal



THE MAX 643 STEP-UP REGULATOR can generate output voltages significantly higher than its input: usually about 15 V from a 5-V power supply.

chokes used for interference suppression in 60-Hz light dimmers have been found adequate, if somewhat bulky. A 3 to 5 A ac rating is a suitable and low cost device.

The output of the converter is semi-regulated to 350 V, the output voltage being determined by the value of R3. The converter operates as long as the output voltage is lower than required, and then stops. The standby input current is as low as 2 mA when stopped. As soon as the voltage across the output capacitor falls under a slightly lower threshold, the converter starts again, drawing approximately 400 to 500 mA from its 9 to 12 V supply.

The on/off duty cycle depends only on the load characteristics. The converter may well operate all the time at the full 2 W load, but also just starts from time to time if no load is connected across the output capacitor.

Voted "Best of Issue"
Electronic Design,
April 15, 1996

Data Acquisition Made Easy

ALEXANDER EISEN, State University of New York, Physics Dept., 239 Fronczak Hall, Buffalo, NY 14260; (716) 645-2590;

In cases where only one analog input needs to be measured, expensive data-acquisition plug-ins can be avoided. The design presented here uses a fast, 12-bit, sampling ADC with a 100-kHz throughput rate and a parallel printer port to link to a PC—a straightforward interface that doesn't even require opening the computer case (*see the figure*).

The AD7896AN developed by Analog Devices, Norwood, Mass., contains an 8-µs ADC, a track-and-hold amplifier, control logic, and a high-speed serial interface, all in an 8-pin DIP. The V_{DD} input also is used as the reference, so no external reference is needed. The falling edge of CONVST starts conversion, puts the track-and-hold amplifier into its hold state, and causes the BUSY signal to go high. After the conversion is complete, BUSY goes low and new data is available in the output register. The read operation accesses this data by clocking it out in 16 clock cycles. The data format provided by AD7896 is four leading zeros followed by the 12-bit conversion result starting with MSB (DB11).

CONVST and SCLK are controlled using the PC output port, usually located at address 378h (pins 2 and 3 of the DB25 connector), and BUSY is while DOUT is read via the monitored PC input port located at 379h (pins 13 and 11).

The program code in C (*see the listing*) initiates ADC conversion, waits until it's done (the BUSY line goes low), and then clocks data out from the ADC serially through the port 379h (brd_addr+1). The acquired data is stored into an array, and after N conversions are completed, gets stored into a data.dat file on floppy disk. Now the data can be analyzed and processed as needed. To fully utilize the speed of an ADC, the communication portion of the program

```
#include   <dos.h>
#include   <stdio.h>
#define    brd_addr 0x378
#define N 1024
take_data();
main()
{
            int i;
            FILE*fd;
            double data[N];
            for(i=0;i<N;i++){
                        data[i]=take_data();
            }
            fd=fopen("b:\\data.dat","wb");    /*write data to file*/
            fwrite(data,sizeof(data),1,fd);   /*b:\data.dat*/
            fclose(fd);
            return 0;
}
take_data()
{
            int i;
            double result;
            unsigned int data,temp;
            data=0;
            outportb(brd_addr,0xfd);      /*SCLK-low, CONVST-high*/
            outportb(brd_addr,0xfc);      /*start conversion*/
            outportb(brd_addr,0xfd);
            do{
                          temp=0x0010&inportb(brd_addr+1); /*poll BUSY
till low*/
                  }while(temp!=0);
            for(i=0;i<16;i++)[             /*output 16 clock cycles*/
                  outportb(brd_addr,0xff);        /*SCLK-high*/
                  temp=-inportb(brd_addr+1); /*MSB in port 379h
is inverted*/
                  outportb(brd_addr,0xfd);        /*SCLK-low*/
                  temp>>=7;              /*move bit to LSB position*/
                  temp&=0x0001;           /*extract next bit*/
                  data|=temp;             /*OR-ed with data*/
                  data<<=1;               /*prepare for next bit*/
            }
            data>>=1;
            result=data;                       /*changes data format to
"double"*/
            result/=800;                       /*scales down data to a
real value*/
            printf("%5.4f\n",result);    /*if 5V power supply is
used*/
             return(result);
 }
```

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W31	Thermal	1	0.5 - 50A	Toggle Actuator	9230
W33	Thermal	1 or 2	2 - 20A	Snap-in, Rocker Actuator	9330
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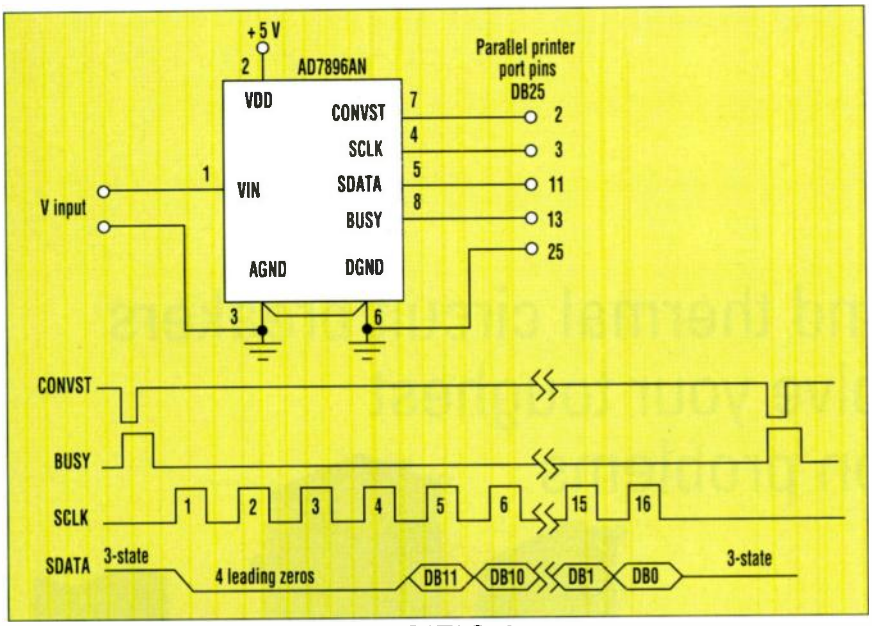


EXPENSIVE DATA-ACQUISITION plug-ins can be avoided using this circuit. In fact, the simple setup uses just a 12-bit sampling ADC with a 100-kHz throughput rate and a parallel printer port as the PC interface.

code could be rewritten in an assembler and called from main().

This design isn't limited to this application. The same technique could be used with other more sophisticated ADCs with serial communication capabilities, such as the 24-bit AD7714 from Analog Devices or the 18-bit MAX132 from Maxim Integrated Products, among many others. Some of these have additional features such as multi-channel multiplexed inputs, built-in digital filters with adjustable cutoff frequency, programmable gain input buffers, built-in references, autozeroing, and calibration. All of these features can be configured and programmed in a way similar to the one presented here.

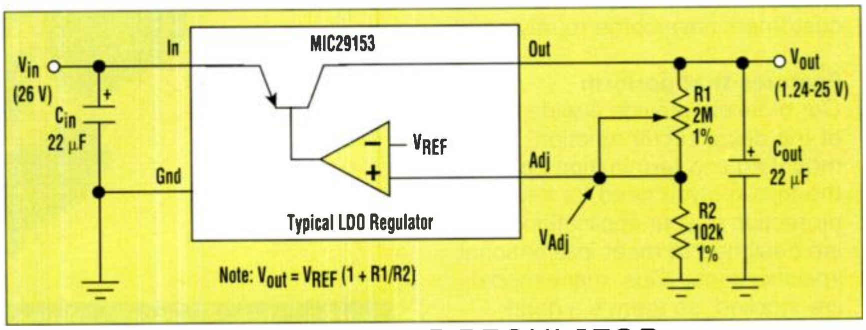
Voted "Best of Issue" Electronic Design, May 1, 1996

Regulator Adjusts From 0 V To 25 V

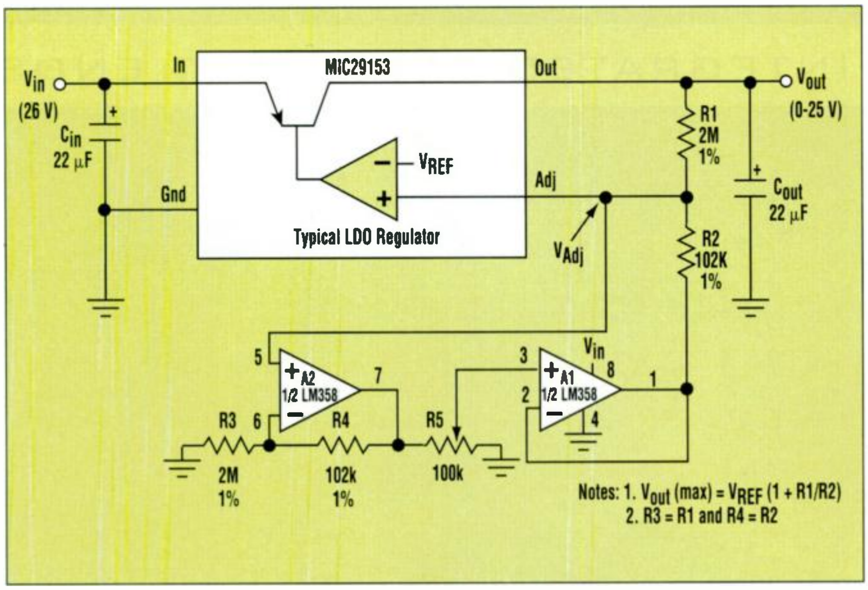
GERALD L. KMETZ . Micrel Semiconductor Inc., 1849 Fortune Dr., San Jose, CA 95131; (408) 435-3448; fax (408) 944-0510.

An adjustable power supply should provide a range that includes 0 V. But a typical adjustable regulator does not facilitate adjustment to voltages lower than V_{REF} (the internal bandgap voltage) (*Fig. 1*). Feedback-loop summing junction V_{Adj} must be biased at V_{REF} to provide linear operation. The lowest output voltage available from this circuit is provided when R1 = 0 Ω. For the MIC29153 LDO Regulator, V_{REF} = 1.24 V. $V_{out}(min) = V_{REF}(1 + R1/R2)$.

The next circuit shown provides an adjustment down to 0 V by controlling the ground reference of the feedback divider (*Fig. 2*). Moreover, it makes use of the internal bandgap reference to provide both accuracy and economy. Noninverting amplifier A2 senses V_{REF} (via V_{RAdj}) and provides a gain of just slightly more than unity. When R5 is adjusted to supply ground to voltage follower A1, then ground is also applied to the bottom of feedback voltage divider R1 and R2, and operation is identical to the circuit previously shown (adjusted to provide maximum output voltage) (*Fig. 1, again*). Conversely, when R5 is adjusted so the input to voltage follower A1 is taken directly from the output of amplifier A2, the bottom of voltage divider R1 and R2 is biased such that V_{Adj} will equal V_{REF} when



1. A TYPICAL ADJUSTABLE REGULATOR does not permit adjustment to the internal bandgap voltages lower than VREF.



2. THIS CIRCUIT PROVIDES ADJUSTABILITY down to 0 V by controlling the ground reference of the feedback divider.

V_{out} is 0 V. Rotation of R5 results in a smooth variation of output voltage from 0 V to the upper design value, determined by R1 and R2. Once again, $V_{out}(max) = V_{REF}$ (1 + R1/R2).

The gain of amplifier A2 is 1 + R4/R3 = 1.05, in this example. It is interesting to note that the portion of gain above unity is the reciprocal of the attenuation ratio afforded by feedback divider R1 and R2; i.e., R4/R3 = 1/(R1/R2).

To provide optimal ratio matching, resistors R3 and R4 have been chosen to be the same values and types as their respective counterparts, R1 and R2.

Voted "Best of Issue" Electronic Design, May 13, 1996

3-Wire RS232 To RS485 Converter

W. STEPHEN WOODWARD, University of North Carolina, Venable Hall, CB3290, Chapel Hill, NC 27599-3290.

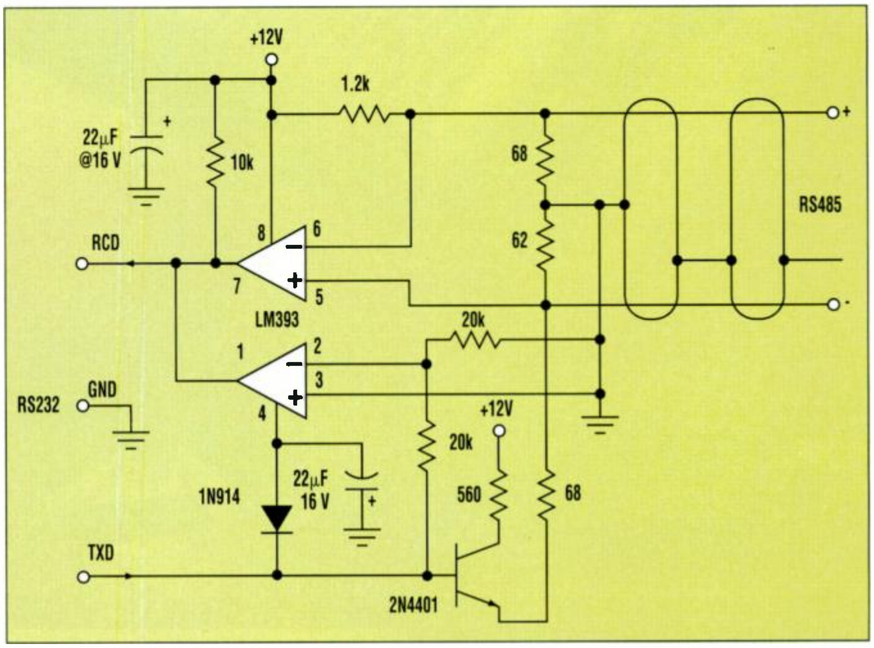
The RS485 signaling standard, with its high speed, noise-resistant differential communication, has gained a lot of popularity in industrial applications.

On the other hand, single-ended asynchronous RS232 lives on and occasionally the need arises for I/O interface between devices using these incompatible standards. Commercial devices exist, of course, but many are somewhat pricey and most work only with fully implemented RS232 ports that support "modem handshaking" signals the converter uses to control the direction of information flow over the inherently half-duplex RS485 cable.

This little circuit needs only a minimal "3-wire" RS232 implementation plus one +10-V to +15-V supply voltage to provide a transparent link capable of sending data at transmission rates up to tens of kbaud (*see the figure*).

Circuit operation is as follows: When both 232 and 485 are idle (232 port in MARK state and no 485 device active), the 485 link is held in the "1" state by the 1200-Ω pullup. This causes the top comparator to hold the 232 RCD line negative and therefore in "MARK" state.

When a character is transmitted by the 232 port, it begins with a positive-going (SPACE state) "START" bit on the TXD line. In response the 2N4401 pulls the "–"



ONLY A "3-WIRE" RS232 IMPLEMENTATION along with a +10 to +15-V supply voltage) is needed to provide a transparent link good for data rates up to tens of kbaud.

485 conductor more positive than the "+" wire, thus transmitting the "START" down the 485 cable. Meanwhile, the bottom comparator holds the "wire-or" (LM393s have open collector outputs) 232 RCD low, blocking the 232 port from "hearing" its own transmission. So the receive side of the 232 port remains idle, just like a well-behaved half-duplex should. The rest of the bits of the character follow along in the same fashion.

When a character originates somewhere along the 485 bus, it begins with a 485 transceiver going active and driving the "–" line above "+". This causes the upper half of the LM393 comparator to release RCD and this time the bottom comparator doesn't prevent it from being pulled high. The data bits are thus allowed to arrive at the RS232 port where they appear at standard RS232 bipolar voltage levels.

The common-mode voltage range and noise-rejection capabilities of this circuit are compatible with standard 485 specifications. The converter's speed is mainly limited by loading of the comparator outputs due to cable capacitance. So it's a good idea to limit the length of the RS232 cable to a couple of feet.

Doing so makes data rates as high as 100 kbaud feasible.

Voted "Best of Issue"
Electronic Design,
June 10, 1996

Fault-Tolerant Relay Driver Circuit

SCOTT C. WILLIS and MARK J. JONES, Loral Federal Systems, 9500 Goodwin Dr., MS 120/025, Manassas, VA 22110;

Mechanical relays are useful in remote switching applications that require electrical isolation between control and switched circuits. The traditional approach for driving the relay coils uses a single-transistor common-emitter switch, along with a suppression diode. This basic circuit is often extended in redundant systems by paralleling two transistor switches driven by separate controllers. However, these devices are a potential single point of failure in a high availability system.

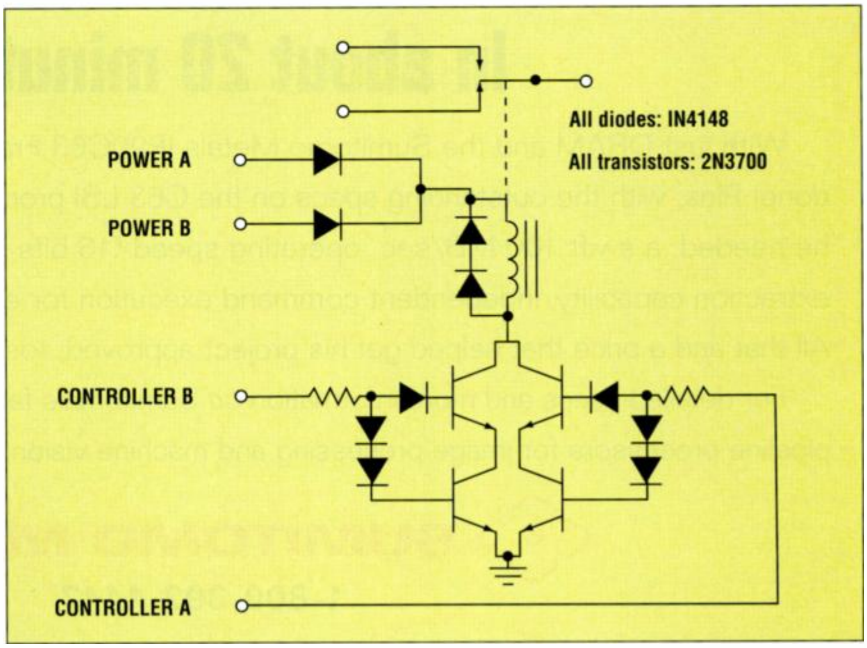
Shown is a circuit that can reduce the likelihood of having an unrecoverable failure in the relay driver circuit (*see the figure*). Additional transistor switches, inserted in series with the original controlling transistors, maintain proper operation if a single transistor fails. The diodes connected to the upper transistors prevent reverse base current flow if the collector-base junctions break down.

The diodes connected to the lower transistor provide proper biasing for the circuit. The upper and lower transistors will have a similar V_{be} since they are the same type and have nearly identical currents. Therefore, the V_{ce} of the lower transistor will be about the same as one diode voltage drop, and the device will be operating in the active region.

Power to the relays can be provided by one of two voltage sources connected together through diodes in a wired-OR configuration. The additional diode clamps the coil inductance voltage spike in the event one of the suppression diodes fail shorted.

Note that this circuit is applicable to both conventional and latching relays. Also, an additional relay is required for full redundancy, but is not an option in many weight-sensitive aerospace applications.

Voted "Best of Issue"
Electronic Design,
June 24, 1996



MANY POTENTIAL SINGLE POINTS OF FAILURE are eliminated by this relay driver with added transistors and diodes.

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	+/-18mA @ 2.3V VCC
	+/-6mA @ 1.8V VCC
Supply Current (I_{CC})	0.25µA
Speed* (t_{PD})	1.8ns @ 3.3V
	2.0ns @ 2.5V
	3.0ns @ 1.8V
Noise V_{OLP}/V_{OLV}	0.8/-0.8V @ 3.3V
	0.6/-0.6V @ 2.5V
	0.25/-0.25V @ 1.8V

Over-voltage Tolerance Specifications*

Input Leakage Current (I_I)	($0 \leq V_I \leq 3.6V$)	0.04µA
3-STATE Output Leakage (I_{OZ})	($0 \leq V_O \leq 3.6V$)	0.04µA
Power-Off Leakage Current (I_{OFF})	(V_I or V_O=3.6V)	0.25µA

* typical values represented

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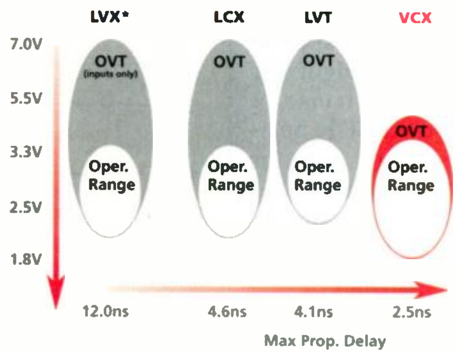

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READER SERVICE 96

Simple PC Smart Card Reader

PATRICK GUEULLE, B.P. 279, 76055 Le Havre Cedex, France.

ISO 7816-compliant "synchronous" smart cards (such as those used for prepaid telephone cards) are simply secure serial EPROMs or EEPROMs and can be read without the need of intricate hardware or software.

Shown is the simplest possible arrangement, based upon a direct connection of the smart card socket to the parallel printer port of any PC (*Fig. 1*).

Only a spare 5-V power supply is needed, possibly borrowed from an unused "joystick" port. The 15-ohm resistor is needed to avoid any short-circuits when anything but a true smart card is inserted into the connector.

Two layouts can be found for the flat contacts on the card itself. Figure 2a shows the oldest one (AFNOR), mainly used in France, and Figure 2b, the internationally approved one (ISO).

It should be stressed that on most modern cards with their contacts in the ISO position, contacts #4 and #5 are not used, and are often omitted.

Smart card connectors are usually fitted with a full set of sixteen wipers; eight for the contacts in the AFNOR position, and eight for the contacts in the ISO position. It is a good practice to parallel the wipers with the same number in both sets.

Read operations can be performed by means of very simple software. For example, the short Turbo-Pascal program shown in Figure

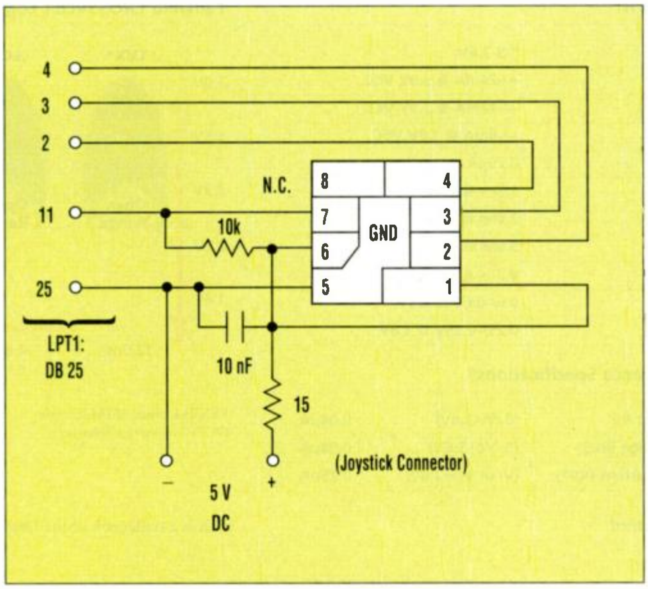
(a)

```
uses crt;
var a,e,f,g:integer
  begin
  clrscr;
  port[888]:=0;
  port[888]:=250;
  port[888]:=248;
  clrscr;
  for f:=1 to 8 do
   begin
   for g:=1 to 32 do
     begin
     port [888]: =249;
     delay(1);
     e:=port[889];
     a:=e and 128;
     if (a=128) then write ('0 ') else write ('1 ');
     port[888]:=251;
     end;
   writeln;
   end;
end.
```

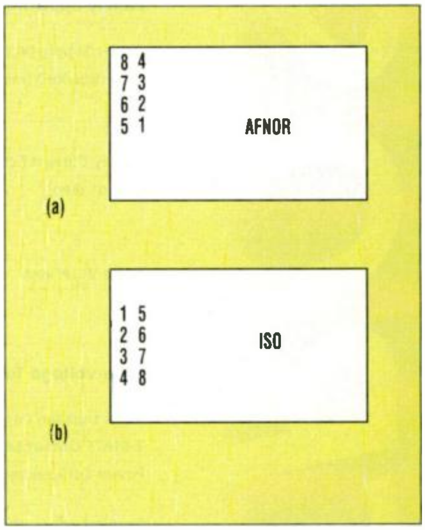
(b)

```
1 0 1 1 1 0 1 1 0 0 0 0 0 0 1 1 0 1 1 1 0 0 0 1 0 1 0 1 0 0 1 1
1 1 0 0 0 0 1 1 0 1 0 1 0 1 1 1 0 0 0 0 0 1 0 0 0 0 0 0 0 1 1 0
1 1 0 0 0 0 1 1 0 1 0 1 1 1 1 0 0 0 0 1 0 0 0 0 0 0 0 0 0 1 1 0
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1
```

3. A SHORT TURBO-PASCAL PROGRAM can perform read operations. Fig. 3b's program lists all 256 bits of memory.



1. THE SIMPLEST APPROACH for synchronous cards uses a direct connection socket to the PC parallel port.



2. TWO LAYOUTS are attributed for the flat contacts on smart cards. Fig. 2a shows AFNOR (the oldest one), and Fig. 2b shows the internationally-approved ISO layout.

```
(a)

uses crt;
var a,e,f,g:integer;
  begin
  clrscr;
  port[888]:=0;
  port[888]:=252;
  port[888]:=254;
  port[888]:=252;
  port[888]:=248;
  clrscr;
  for f:=1 to 16 do
   begin
   for g:=1 to 32 do
     begin
     port[888]:=248;
     delay(1);
     e:=port[889];
     a:=e and 128;
     if (a=128) then write('0 ') else write ('1 ');
     port[888]:=250;
     end;
   writeln;
   end
end.

(b)

1 0 0 0 0 0 0 0 0 1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 1 0 1 0
1 1 1 0 1 0 1 0 0 1 0 0 1 0 0 1 0 1 0 0 0 1 1 0 1 1 0 0 0 1 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
0 0 0 0 1 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 0 0 0 0 0 0 0 0 0
0 0 0 0 1 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
```

4. FIG. 4a IMPLEMENTS THE INSTRUCTION SET of most smart cards used in Europe. Fig. 4b shows the results obtained with a recent German phonecard.

3a. It uses the LPT1 port to send "micro-instructions" to the smart card, and to sense the bits that the card outputs on its data line (contact #7).

The instruction set used here is the one for Gemplus GPM256-type cards, 256-bit OTP EPROMs used as token holders in many applications (for example, prepaid telephone cards in France and in most countries of the world). The program lists all 256 bits of the memory (*Fig. 3b*).

The second program listing implements the instruction set of "Eurochip" cards, secure EEPROMs that are widely used for third-generation prepaid telephone cards in some European countries using the German system (*Fig. 4a*). Figure 4b shows the results obtained with a recent German phone card, the extra bits of which are used to implement some type of cryptographic protection.

It is worth noting that even such a simple reader could well be used to grant access to a PC or software or data files, only to the bearer of a suitable smart card (used prepaid telephone smart cards usually still contain a unique serial number that cannot be forged easily).

Voted "Best of Issue" Electronic Design, July 8, 1996

High-Frequency Loop Antenna

M.J. SALVATI, Flushing Communications, 150-46 35th Ave., Flushing, NY 11354; (718) 358-0932.

Tuned-loop active antennas have been confined to low and medium frequencies for several reasons, primarily due to the difficult requirements for the active circuitry. Good performance in the 5-to-30-MHz range requires an amplifier with extremely high input impedance and low noise that can drive 75-Ω loads at high signal levels at frequencies over 30 MHz. Combining dual FET source followers and the Maxim 436 wideband transconductance amplifier can produce such an amplifier (*see the figure*).

A balanced configuration is used for the tuned loop to preserve the symmetry of the figure-eight polar antenna pattern. With FET source followers on the amplifier's front end, only the 1-MΩ gate resistors load the tuned circuit, so tuning is very sharp and resistance to off-frequency interference is very high. The FETs drive the MAX436's differential inputs, which amplifies the balanced signal and converts it to a single-ended output.

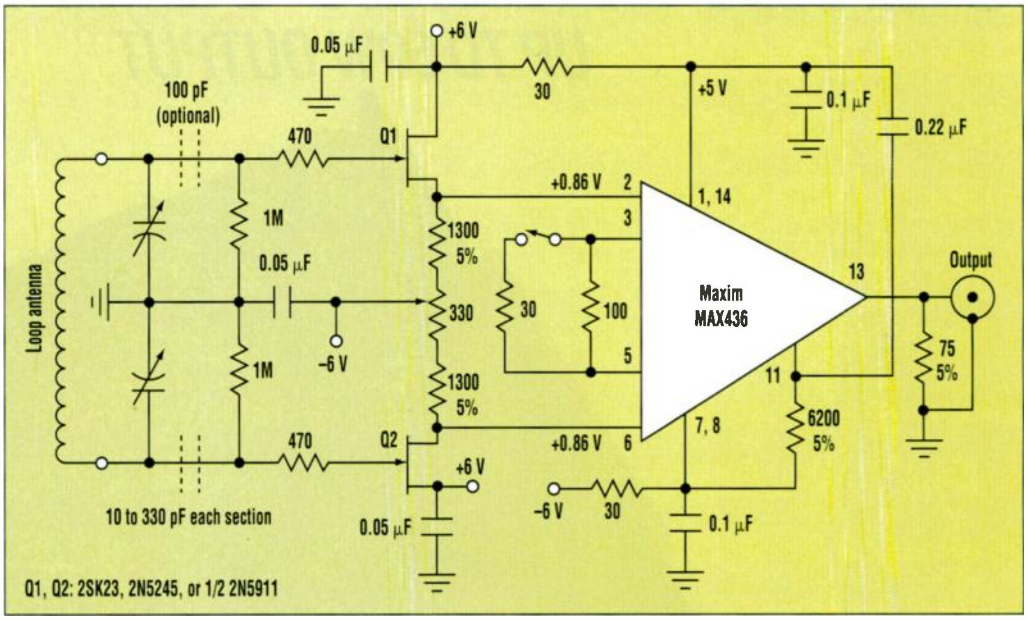
Voltage gain for this amplifier is switch selectable at either 8 dB or 20 dB into a 75-Ω load. Since the amplifier is designed to work into a 75-Ω load, the device can be connected to the receiver with a length of RG59U cable. Maximum undistorted output is 1500 mV into 75 Ω, so overloading is unlikely even at the high-gain setting.

A three-turn, 15-in. diameter coil (made from No. 8 aluminum ground wire with 1/2-in. between turns) will cover from 4.4 to 16 MHz with a dual 10-to-330-pF variable capacitor. A single-turn

coil (built with a 48-in. long strip of 1-1/4-in. wide sheet aluminum) will cover from 13 to 55 MHz (although performance falls off past 40 MHz). This unusually wide frequency range coverage is due in part to the FET source follower's extremely low input capacitance.

The 470-Ω resistors prevent gate damage from accumulated static charge when handling the loops to change the frequency range. These resistors' Johnson-noise contribution is negligible due to the high-noise environment typical of an indoor site. If the reception site has unusually strong ac fields, adding 100-pF input capacitors can reduce the levels of 60-to-180-Hz pickup, otherwise they're unnecessary. The only adjustment required is to zero the output via the 330-Ω trimmer.

This type of loop typically has very high output even at the low gain setting (the output of the prototype unit required that a 15-dB attenuation be added to the output for A-B comparisons with a fan of 1/4-wavelength antennas located outdoors at the same height as the loop). Whether the loop can outperform an outdoor wire antenna depends primarily on the noise environment in the loop's vicinity, and the signal attenuation by the building's walls. In any case, this loop should outperform any other type of indoor antenna.



COMBINING DUAL FET SOURCE FOLLOWER and Maxim's 436 transconductance amplifier creates a high-impedance, low-noise amplifier that makes possible a high-frequency loop antenna.

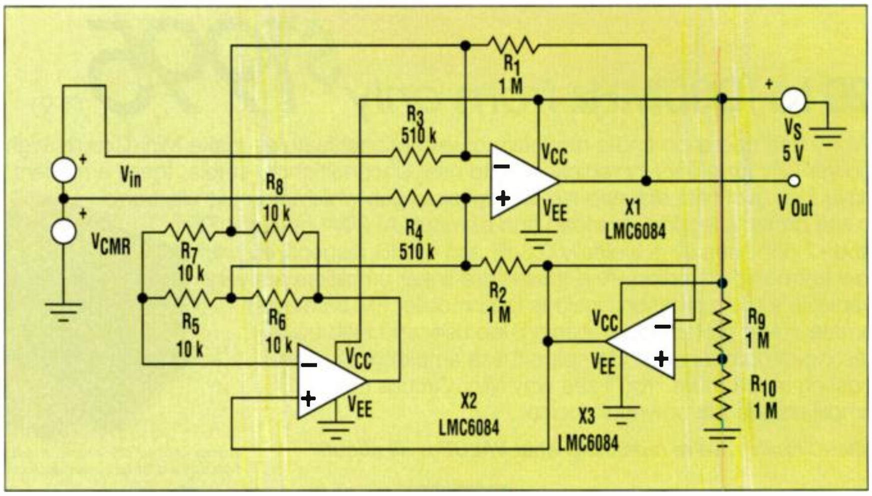
Voted "Best of Issue" Electronic Design, July 22, 1996

Diff Amp Digitizes Small Signals

JERRY STEELE, National Semiconductor Corp., Tucson Design Center, 940 Finance Center Dr., Suite 120, Tucson, AZ

This differential amplifier handles common-mode voltages up to ±24 V on a 3.3-V supply, or up to ±40 V on a 5-V supply (*Fig. 1*). It comes in handy when interfacing analog-to-digital converters (ADCs) or data-acquisition systems (DASs) in 3.3-V or 5-V single-supply systems to inputs with a wide common-mode range.

Differential amplifier X1 is the actual diff amp, and R1, R2, R3, and R4 are the gain-setting resistors. X2 forces the common-mode voltage at X1's inputs to zero with respect to a quiescent biasing point provided by X3. The wide availability of dual and quad low-voltage op amps permits implementa-



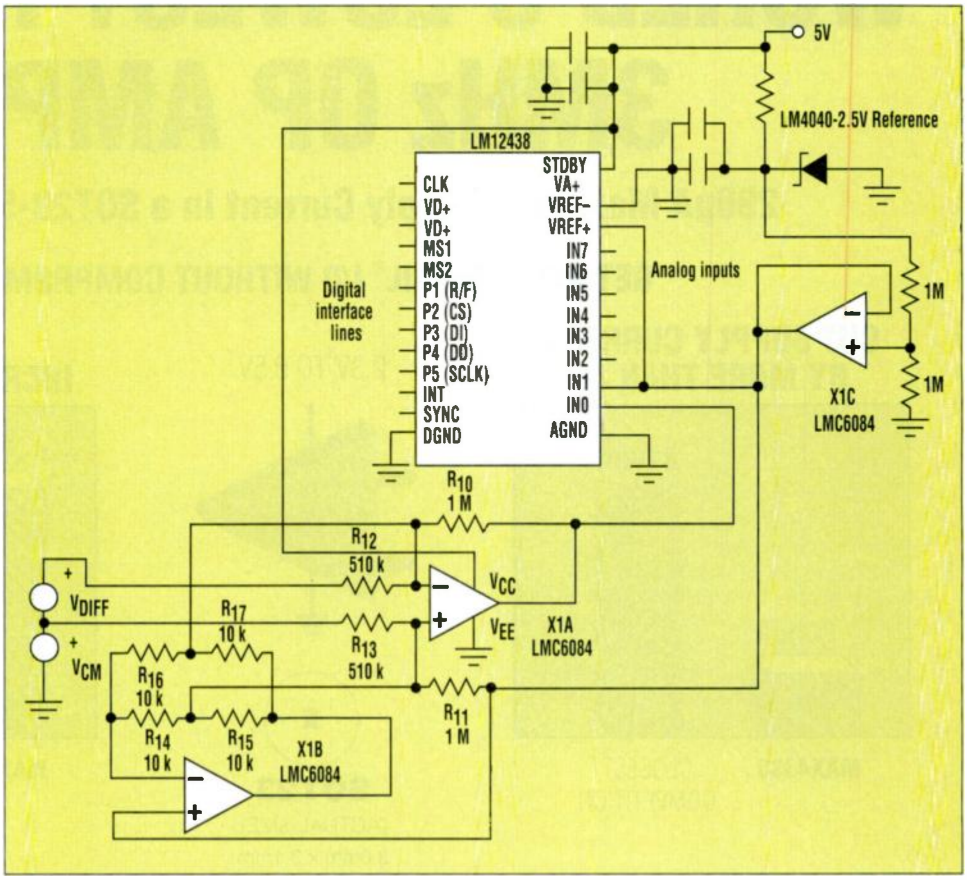
1. THIS DIFFERENTIAL AMPLIFIER handles comm on-mode voltage of up to ±24 V on a 3.3-V supply, or ±40 V on a 5-V supply.

Circle No. 100 - For U.S. Response
Circle No. 101 - For International

tion with one IC package.

Biasing at one-half supply, or at some reference well within the supply rails, is necessary because positive-going common-mode inputs require X2's output to swing negative. R5, R6, R7, and R8 should be at least an order of magnitude impedance less than the gain-setting resistors of X1. Common-mode signals induce currents into R3 and R4 that would otherwise induce voltage at X1's inputs were it not for the compensating current flow through R6 and R8. The available current in R6 and R8 is a function of available output swing from X2 and the values of R6 and R8 (assuming that these currents are well within X2's current capability and current limit).

The impedance relationship of R6 and R8 to gain-setting resistors limits the use of this circuit to high-impedance differential-amplifier circuits, and it's not well suited for wide-bandwidth circuits. The high impedances also favor the use of JFET or CMOS input op amps.



2. COMMON-MODE INPUTS of up to ± 40 V, while operating on a 5-V supply, can be handled by this data-acquisition-system input configuration.

As with any differential amplifier, the gain-setting resistors should be matched as close as possible (use a prepackaged resistor network if feasible). The effects of R5, R6, R7, and R8 on X2 isn't that critical. However, because they form impedances off of the input nodes of the differential amplifier, they also should be closely matched.

When incorporating the differential amplifier with a low-voltage DAS, the amplifier's bias point is at the DAS's reference voltage, at approximately half supply (2.5 V on a 5-V system) (*Fig. 2*). The amplifier output will swing in both the positive and negative directions from this center value. By configuring the DAS high-side input to the sense-amplifier output, and the low side to the sense reference, gives the DAS a bipolar dynamic range. Using a bipolar dynamic range takes advantage of the sign bit available in many DASs and ADCs, and provides an extra bit of resolution. This amplifier must always precede the multiplexer inputs of a DAS or multichannel ADC because the multiplexer can't handle the high common-mode voltage.

Reference:

Orense, Lester R., "Measure Power Without Iso Amps," Electronic Design, Sept. 17, 1992, p. 90.

Voted "Best of Issue" Electronic Design, August 5, 1996

Temp-Controlled Fan Reduces Noise

KERRY LACANETTE . National Semiconductor Corp., 6377 E. Tanque Verde Rd., Suite 101, Tucson, AZ 85175; (520) 751-3769; fax (520) 751-2379.

Cooling fans help prevent computers, instruments, and other equipment from overheating, but they also produce noise that can contribute to user fatigue. One way to combat heat and noise simultaneously is to operate the fan at a low speed when system temperature is low, and

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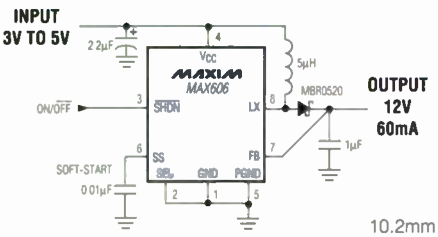

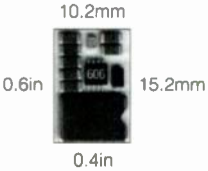

Area = 0.24in²
= 63mm²
Max. Height = 1.35mm

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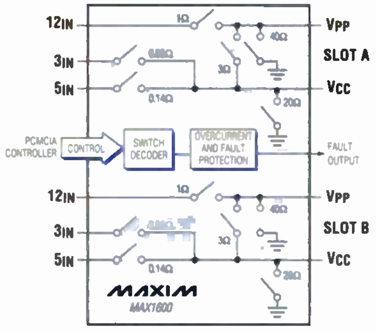
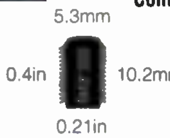
- Thin, 1.35mm High External Components
- 1.11mm High µMAX Package
- 1µA (max) Shutdown
- 5V, 12V, or Adjustable Output
- MAX606EVKIT-MM

PCMCIA/CardBus Power Network Switches 1A for 2 Slots in Host Machines

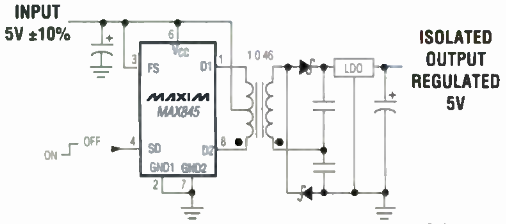


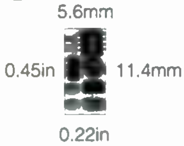
MAX1600 (Available 6/96)
- No External Components
- Narrow 5mm SSOP
- Dual Switches:
  - 3.3V (1A, 0.08Ω)
  - 5V (1A, 0.14Ω)
  - V_{PP} (12V, 120mA)
- Overcurrent & Thermal Protection
- Allows Hot Insertion
- Code-Compatible with Industry-Standard Controllers



Area = 0.08in²
= 54mm²
Max. Height = 1.85mm

Isolated Power Supply Fits PCMCIA LAN Cards





Area = 0.1in²
= 63mm²
Max. Height = 1.5mm

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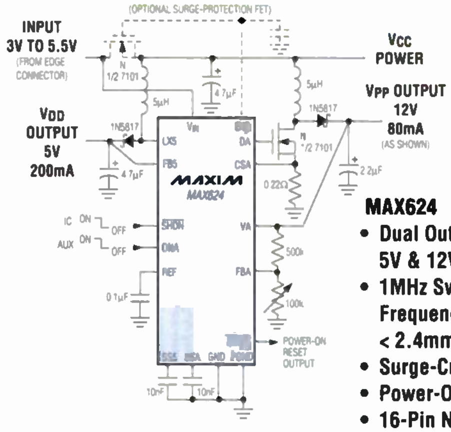

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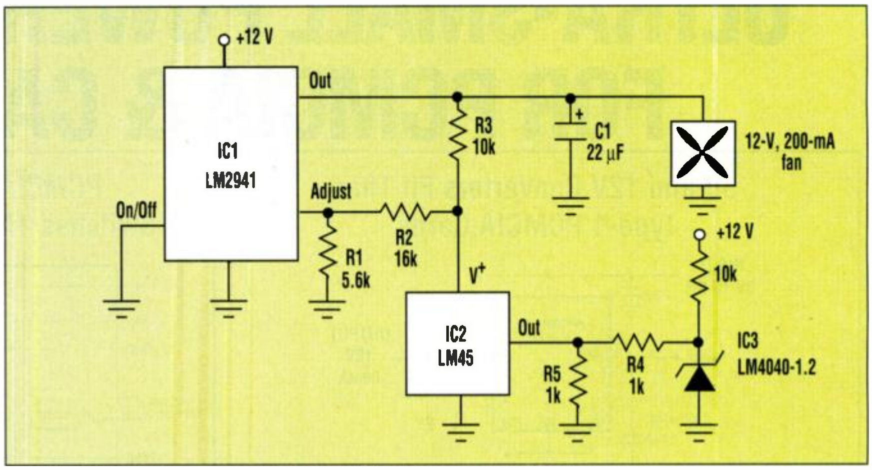
increase fan speed only when temperature exceeds a predetermined threshold. This limits the fan's speed and noise to the minimum necessary for adequate cooling.

The circuit described here needs only three ICs to smoothly increase fan speed as temperature rises above an easily set trip point. Furthermore, the circuit can be extremely compact because two of the ICs are available in tiny SOT-23 packages. Low-dropout voltage regulator IC1 provides power to the fan and to temperature sensor IC2 (*see the figure*). The voltage on IC2's supply pin is equal to:

$$V^+ = 1.275[1 + (R2/R1)] = 1.275[1 + (16k/5.6k)] = 4.9 \text{ V}$$

which is an excellent nominal supply voltage for the LM45 temperature sensor. IC2 drives the middle of the resistor divider across voltage reference IC3. Because the LM45's output stage can only source current, its output voltage will remain at about 610 mV until IC2's temperature rises above 61°C (IC2 has a nominal output voltage equal to 10 mV/ °C). Above 61°C, IC2 will drive the 500-Ω Thevenin resistance of the divider, which will cause IC2's supply current to increase rapidly with rising temperature.



THIS SYSTEM'S COOLING FAN runs at a relatively low rate when temperature sensor IC2 is at a low temperature, thus reducing noise. However, as temperature rises above 61 °C, the fan's speed increases smoothly.

At low temperatures, IC1 supplies the fan with:

$$V_{fan} = 1.275(1 + (R2 + R3)/R1) + R1 \times IQ2 = 1.275(1 + (26k/5.6k)) + 10k \times 80 \ \mu A = 8 \text{ V}$$

where IQ2 is the quiescent supply current of IC2.

As temperature rises above the point where IC2's output voltage exceeds the Thevenin voltage set by R4 and R5, IC2's supply current increases by about 20 µA/ °C above the threshold. IC2's supply current flows through R1 and directly affects the regulator's output voltage. Therefore, if temperature rises 20 °C above the nominal 61 °C threshold, the regulator's output voltage will rise to 12 V and the fan will operate at full speed.

During operation, the fan quickly and smoothly accelerates to a speed that's sufficient to keep the system temperature in the acceptable range without any sudden changes in fan speed.

Voted "Best of Issue"
Electronic Design,
August 19, 1996

Optically Isolated Analog Multiplexer

W. STEPHEN WOODWARD, Venable Hall, CB3290, University of North Carolina, Chapel Hill, NC 27599-3290; Internet: woodward@net.chem.unc.edu.

Accurate analog data acquisition in noisy (e.g., industrial) environments often requires galvanic isolation of signal sources from each other and from data system ground. Commercial devices such as isolation amplifiers can solve the problem, but it becomes messy because isolated power sources are usually required for each input channel.

The circuit described here provides three channels of optically-isolated input that will work for many precision signal-acquisition applications, and needs no expensive hybrid isolation amplifiers or floating power supplies (*see the figure*). In fact, the only power required is a single +5-V rail with ground common to the ADC.

Multiplexer operation is based on an ordinary quad-channel optoisolator (PS2501-4). Each LED (such as E1) in combination with input-scaling resistor R1 will, in response to V_{in}, pass a current $I1 = (V_{in} - V_{led})/(R1 + R_s)$, where V_{led} = the LRD's forward voltage drop and R_s = the signal source's internal resistance.

R1 is chosen to establish a full-scale LED current near 500 µA. Assuming (for example) that channel 1 is selected, the resulting photocurrent in P1 will tend to pull A1's summing point. In response, A1 will forward-bias E2 to generate a balancing photocurrent in P2.

Multi-channel optoisolators exhibit excellent tracking of coupled gains and other parameters. Consequently, the E2 current required to maintain this balance will closely track I1 as will the Vled of E2 closely equal the Vled of

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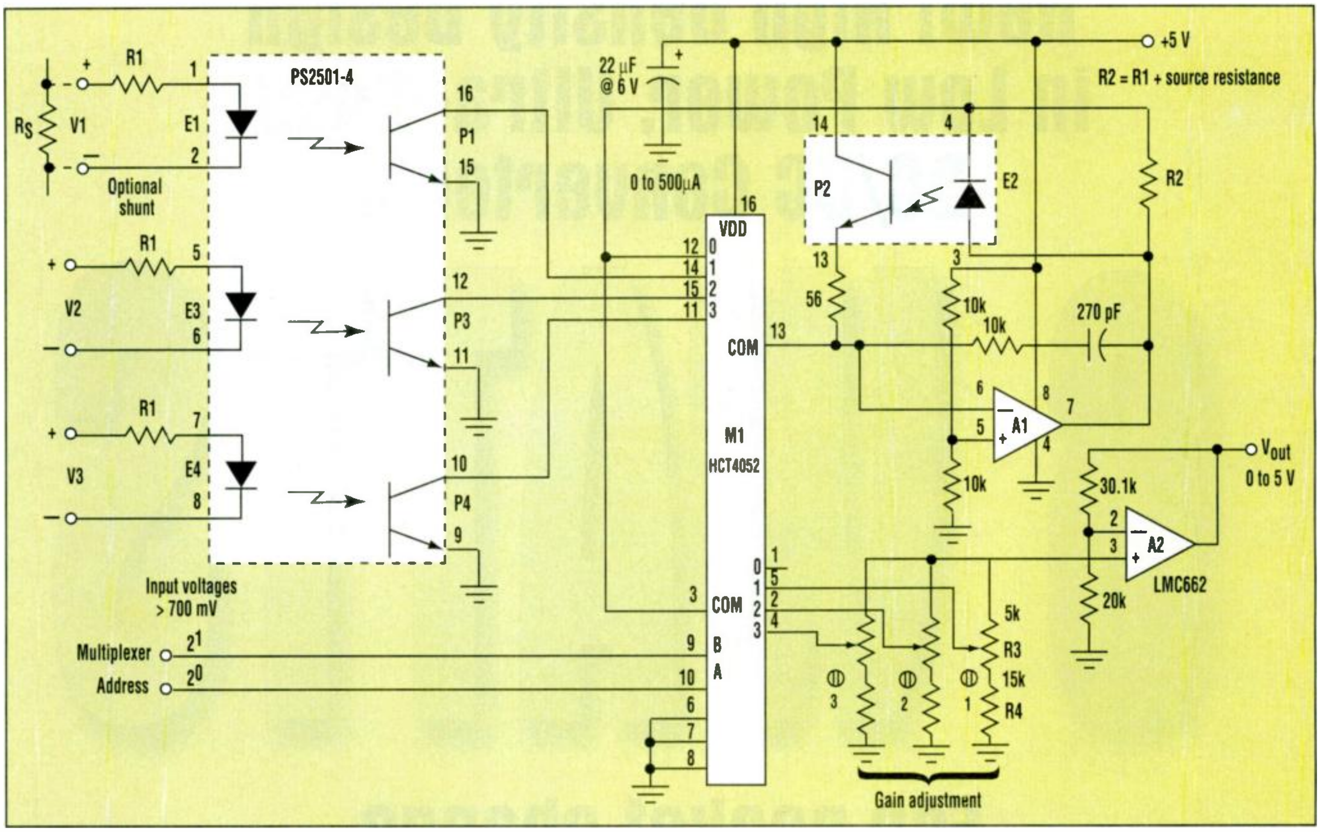


THIS ANALOG MULTIPLEXER provides three channels of optically isolated input that works in many precision signal-acquisition applications. The only power needed is a single +5-V rail with ground common to the analog-to-digital converter.

E1. This leads to an interesting and useful relationship. Assume R2 is chosen so that R2 = R1 + Rs. Then I2, the total current sourced by A1 to the parallel combination of E2 and R2, will be: $I2 = I1 + V_{led}/(R1 + Rs)$. But from above, we know $I1 = V_{in}/(R1 + Rs) - V_{led}/(R1 + Rs)$. Thus, $I2 = V_{in}/(R1 + Rs)$ and the current sourced through M1 to the gain-adjustment network is directly proportional to the floating input voltages. Therefore, it's independent of the LED voltage drops.

Of course, there's no such thing as a free lunch, and this compensation trick only works for $V_{in} > V_{led}$. That means input voltages below the threshold required for at least some conduction in the LEDs (about 700 mV) can't be sensed at all. But many applications don't involve input voltages that go to zero and are not troubled by this limitation. For example, if a shunt resistor of 511 Ω is used at the multiplexer input in combination with R1 = 20k and R2 = 20.5k, standard industrial 4-to-20-mA current loop signals can be accurately (within 0.1%) sensed because minimum V_{in} = 500 Ω x 4 mA = 2 V.

Minor mismatches between the input channels are accommodated with the gain-adjustment trimmer provided for each channel. Using trimmer wipers as input terminals may look peculiar, but it results in convenient, non-interacting gain adjustments for each channel. In addition, because the setting is insensitive to variations in wiper contact resistance, it's time- and temperature-stable. Interchannel settling to 0.1% is a respectable 20 ms. Useful frequency response of the multiplexer extends to 50 kHz.

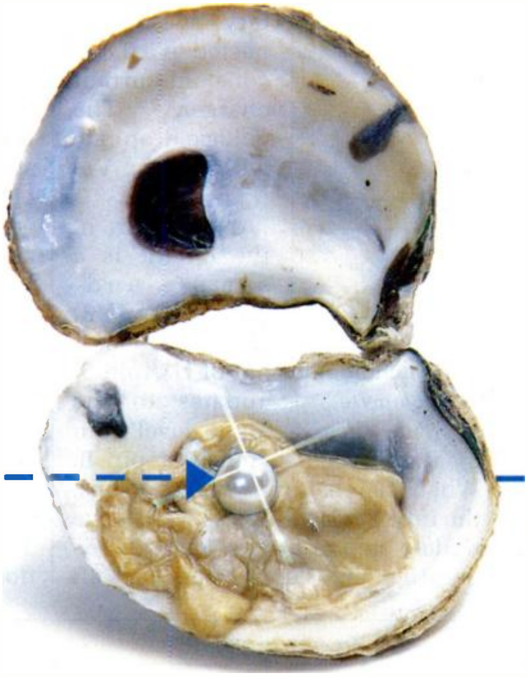
Voted "Best of Issue"
Electronic Design,
September 3, 1996

Use –ΔV To Terminate Fast Charging

ARIE RAVID, Linear Technology Corp., 1630 McCarthy Blvd., Milpitas, CA 95035-7487; (408) 432-1900
woodward@net.chem.unc.edu.

During charging of NiCd and NiMH batteries, their temperature will rise. This characteristic can be used to control termination of the charge process, but a temperature sensor must be bonded to the battery. Such a configuration is costly and at times awkward. However, the inter-

Remember, it's what's in the package that counts.



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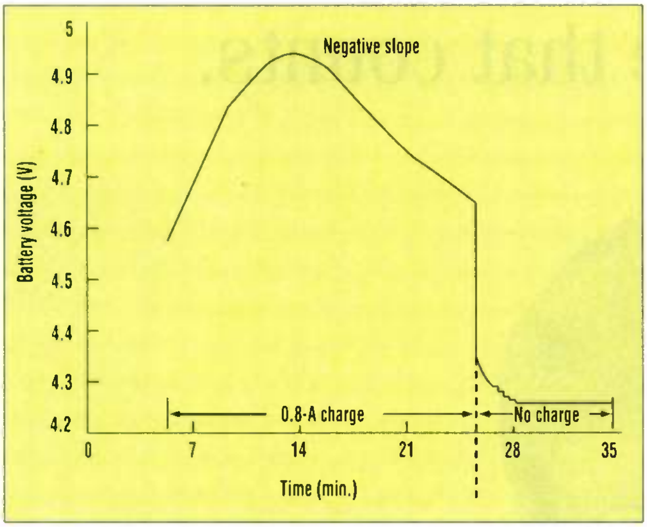


1. A THREE-CELL BATTERY (Panasonic P130-SCR) was connected to a 0.8-A constant-current charger to determine the voltage drop rate, which was −0.54 mV/s.

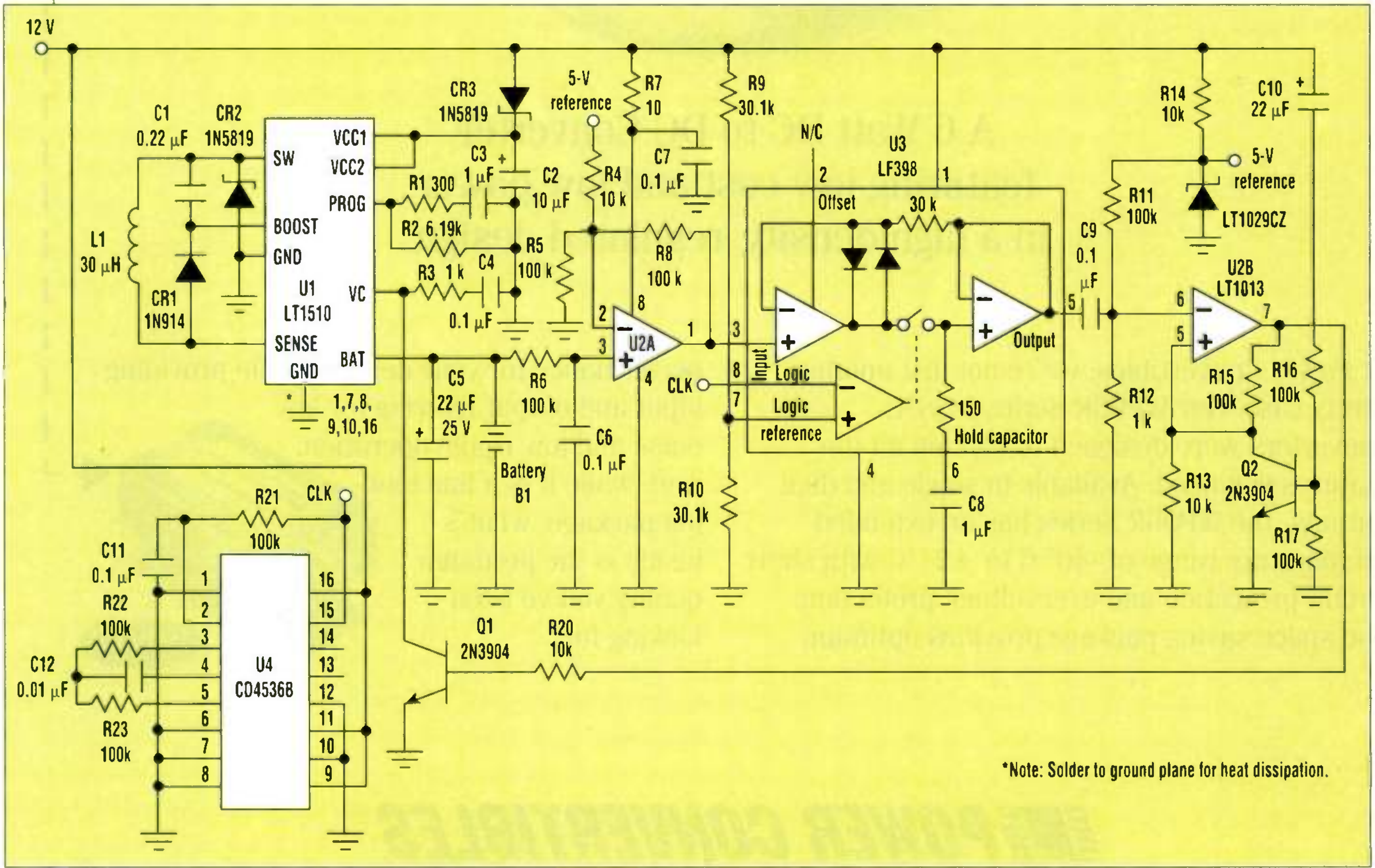
nal battery-temperature rise toward the end of charge causes the battery voltage to drop. The drop can be detected and used to terminate a fast charge.

To determine the voltage drop rate in the case presented here, a three-cell (Panasonic P130-SCR) battery was connected to a 0.8-A constant-current charger. The voltage drop rate was −0.6 mV/s (*Fig. 1*).

At the heart of the circuit is a sample-and-hold IC (U3) (*Fig. 2*). The output of U3 (pin 5) updates to the input level (pin 3) at every clock pulse at pin 8. When the battery voltage drops, the input to U2 drops as well. If the update step at the output of U3 is negative and large enough, U2B latches in high state. Q1 turns on and terminates the charge by pulling the V C pin of U1 down, thus disabling it. U1 is a switch-mode constant-current-type battery charger; however, any controllable current source will do.

U2A and the associated passive components smooth, amplify, and level-shift the battery voltage. The timer (U4) updates the hold capacitor C8 every 15 seconds. The timer signal stays high for 7 ms, a sufficient time for the hold capacitor to get charged to the input level. U2B and the associated parts form a latch that requires a momentary negative voltage at pin 6 to change state. R15 supplies the negative feedback and Q2. R16, R17, and C10 reset the latch on turn-on.

U3's output voltage droops at a rate proportional to the hold-capacitor internal leakage and the leakage current at pin 6 (typically 10 pA). This droop is very low and doesn't affect the circuit's opera-



2. THE CHARGE-TERMINATION method employed with this three-cell NiCd battery charger, which has ΔV termination, was able to provide a consistent charge.

tion. The minimum battery negative voltage slope required for termination can be calculated from:

$$-dV/dt = V_{trig} /(T_{clk} G_{U2A})$$

where V_{trig} is the trigger voltage of U2B ($V_{trig} = V_{ref} \times R12/(R11 + R12) = 5 \times 1/101 = 49.5E - 3$ V; T_{clk} is the clock period (15 seconds); and G_{U2A} is the gain of the first stage (R8/(R4 || R5) = 11.

Hence,

$$-dV/dT = 49.5E - 3 \text{ V}/(15 \text{ seconds} \times 11) = 0.3 \text{ mV/s}$$

The circuit in Figure 2 was tested with a three-cell NiCd battery (Panasonic 1.4 Ah P140-SCR). A total of 68 charge/discharge cycles were performed—the average charge was 1.59 Ah and the standard deviation was 0.0106 Ah. The consistent charge (standard deviation is 0.67% of average) verifies that the charge-termination method described is reliable.

Voted "Best of Issue"
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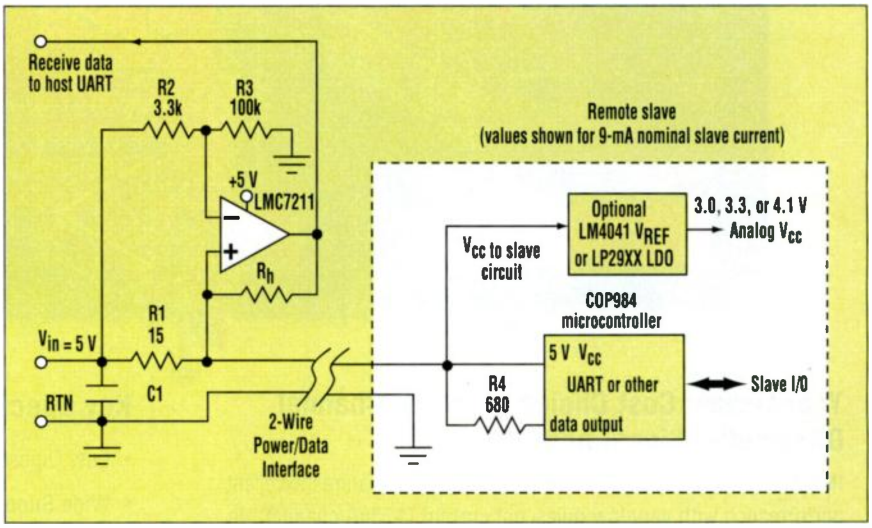
Two Wires Carry Power And Data

BOB HANRAHAN, National Semiconductor Corp., 50 Tice Blvd., Woodcliff Lake, NJ 07675; tel. (201) 782-9002; fax (201) 476-9200.

At times designers are faced with a limited amount of wire and/or a limited cost to communicate with a remote device such as a sensor. Many devices, such as the LM2893 and other carrier-based technologies, exist that allow communication over an ac or dc power line employing an AM or FM modulation scheme. However, they tend to be costly. The design presented here is a simple, low-cost method for sending data across the same wire as is being used to supply power. The scheme is based on modulating current from a remote device back to a host. A later example shows how the host also can modulate voltage to the slave. The host decodes the data by sensing current changes to the slave and recovering the data with an analog comparator. The scheme will cause a small drop in the supply voltage to the remote device that is insignificant in most applications.

The remote microcontroller sends data by sinking current through an output port and series resistor to ground. The resistor value is chosen by calculating the maximum current required by the remote circuit and choosing a resistor that will increase the current required by an amount that can be easily measured with the shunt circuit shown (*Fig. 1*). Designers must ensure that normal operation of the slave doesn't cause current excursions that get interpreted as data, otherwise they must filter these conditions (explained later). In some cases, hysteresis may be necessary and can be added with a bit of positive feedback.



1. THIS RECOVERY CIRCUIT operates by modulating current from a remote device back to a host. Here, a single comparator senses the amount of current passing through the shunt resistor.

The recovery circuit in Figure 1 utilizes a single comparator that senses the amount of current passing through the shunt resistor. If a UART is being used, such as provided in the COP984 8-bit microcontroller, the comparator is configured to provide a logic low when a data bit is on (mark). The comparator is biased with the divider R2/R3 so that the data output from the comparator is stable logic high during normal no-data-flow operation. When a start bit is sent from the remote, the increase in current is sensed by the host and the comparator drives a logic low into the host UART or other recovery device. When the output data is off, the output from the remote device is off and thus not sinking current.

The Figure 1 circuit employs a National Semiconductor LMC7211 comparator. The part was chosen because, unlike traditional comparators, the common-mode input range extends to the positive rail.

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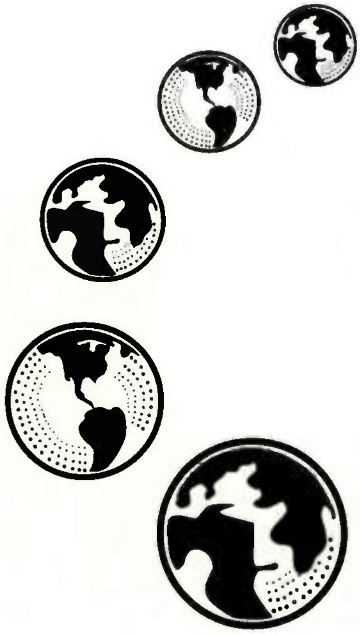

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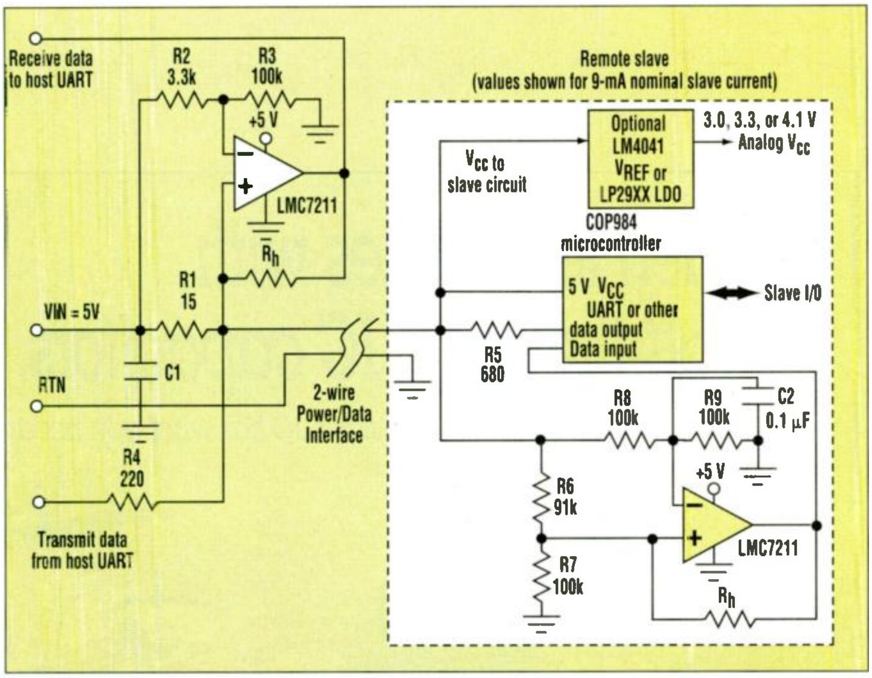

2. A SIMPLE VOLTAGE DIVIDER (R1/R4) modulates the voltage from the host to the slave. The slave circuit compares the voltage being provided to the voltage stored in C2.

This is required when sensing a voltage with a potential at or near the positive rail. Other reasons for using this part include its low operating voltage (down to 2.7 V), its push-pull output (saves a pull-up), and an extremely small SOT23-5 package. This implementation has been optimized for a total slave current load of 9 mA. The comparator reference voltage is set a 4.84 V with R2 and R3. With Vin set at 5.0 V, the drop across shunt R1 will result in the voltage at the noninverting input being either 4.87 V when the signal from the microcontroller is off (high) or 4.77 V when it is on.

Many microcontrollers, such as the NSC COP8 shown, will operate properly with voltages as low as 2.5 V. In this example, the slave voltage will stay within 5% of the 5-V VCC if the slave doesn't generate significant load change. Designers must consider the minimum and maximum slave current when choosing the bias resistor values, as well as the current variation generated by the internal operation of the microcontroller.

With this circuit, the slave current can vary between 6 mA and 10 mA without significantly affecting operation. Larger variations may require a larger shunt R1 (and thus a larger VCC drop), and an appropriate change in reference resistor R2. Fast transient current changes also may be filtered by adding hysteresis with a positive feedback resistor (Rh347k), and/or by adding a filter capacitor (C1) from the noninverting input to ground (0.1 µF). Slave VCC decoupling capacitors must be carefully selected to ensure that the total capacitance doesn't distort the relatively slow current modulation. A value of 1 µF will limit the data frequency to about 10 kbits/s.

In some applications, slave circuits may not tolerate the VCC noise generated by the modulator. This may be seen in situations where a large variation occurs at the slave and an analog block is being employed. In these situations, either a voltage reference (such as an LM4040/4041) if the current required is limited, or an LP2951 low-dropout regulator can be used if the current requirement is up to 100 mA (LP2952 or LP2960 for current up to 0.5 A). This regulator circuit is able to generate a stable voltage a few hundred millivolts below the lowest slave voltage, or set at a standard fixed voltage of 3.0, 3.3, 4.1 V, etc.

Both the LMC7211 and LMC6772 feature delay times that enable them to be used for frequencies up to about 128 kbits/s, depending on the value of the capacitor required at the slave. For higher-frequency applications, a faster device can be used. In addition, the Figure 1 circuit may be used when operating with a 3-V power source.

A bidirectional circuit also can be implemented by modulating the voltage from the host to the slave and modulating current from the slave back to the host. This design may require a greater variation in voltage to the slave to ensure adequate margins. The recovery circuit for the slave can employ the same single comparator. In this case, however, the comparator is looking at the absolute voltage change from the host.

In another configuration, a simple voltage divider (R1/R4) can modulate the voltage from the host to the slave (*Fig. 2*). The slave circuit simply compares the voltage being provided to the voltage stored in C2. The C2/R8/R9 time constant is set much longer than 8 bit times so that the reference level will be stable for this worst-case situation. When the host sends a bit, R4 will pull the slave voltage down and the slave comparator will pass a logic low back to its UART or other receiving device. The host will see its own transmitted data looped back into its recovery circuit. This is typically ignored or can be used for error checking (compare transmitted to received data). The circuits shown are meant to be foundations for a circuit that will work in a particular system. They may not be optimum for a particular design, but using these concepts, designers may implement this extremely small and low-cost communications scheme with great results.

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Bridge Measures Small Capacitance

JEFF WITT, Linear Technology Corp., 1630 McCarthy Blvd., Milpitas, CA 95035-7487; (408) 432-1900, ext. 3710.

Capacitance sensors measure a wide variety of physical quantities, such as position, acceleration, pressure, and fluid level. The capacitance changes involved often are much smaller than the stray capacitances, particularly if the sensor is remotely placed.

The circuit described was developed to measure a 50-pF cryogenic fluid-level detector, with only 2-pF full-scale change, hooked to several hundred picofarads of varying cable capacitance. This requires a circuit with high stability, sensitivity, and noise rejection, but insensitivity to strays caused by cables and shielding. Battery operation and analog output also were desired for easy interfacing to other instruments.

Two traditional circuit types have drawbacks: Integrators are sensitive to noise at the comparator, and voltage-to-frequency converters typically measure stray as well as sensor capacitance. The capacitance bridge presented here measures small transducer capacitance changes yet rejects noise and cable capacitance.

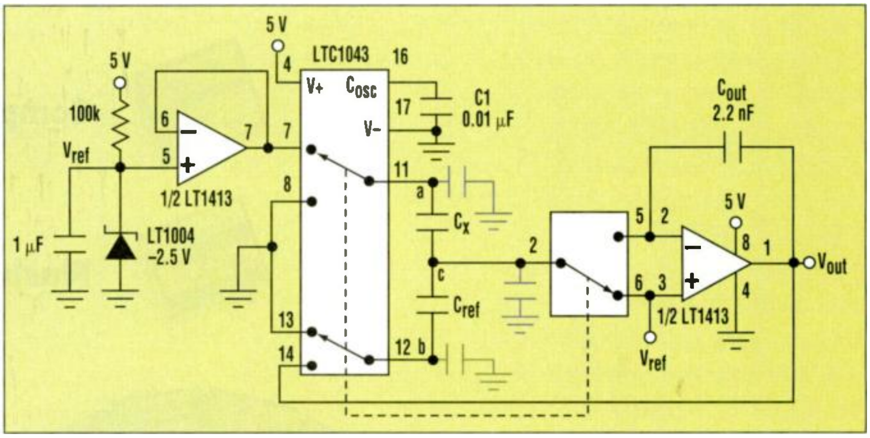
The bridge shown is designed around the LTC1043 switched-capacitor building block (*Fig. 1*). The circuit compares a capacitor (C_x) of unknown value with a reference capacitor (C_{ref}). The LTC1043, programmed with C1 to switch at 500 Hz, applies a square wave of amplitude V_{ref} to node a, and a square wave of amplitude V_{out} and opposite phase to node b. When the bridge is balanced, the ac voltage at node c is zero, and:

$$V_{out} = V_{ref}\,(C_x / C_{ref})$$

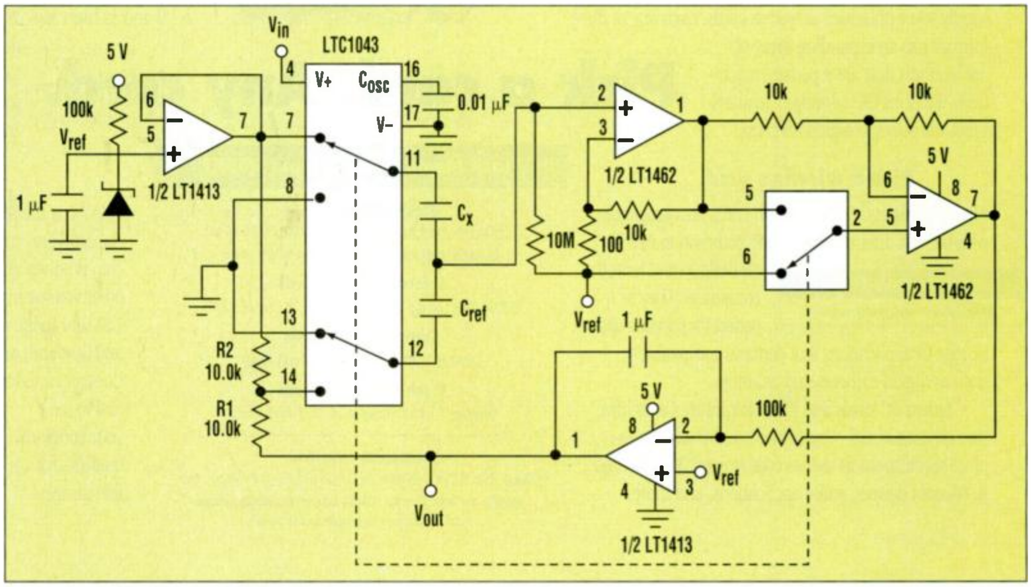
Balance is achieved by integrating the current from node c using an op amp (LT1413) and a third switch on the LTC1043 for synchronous detection. With C_{ref} = 500 pF and V_{ref} = 2.5 V, this circuit has a gain of 5 mV/pF. When measured with a DMM, it achieves a resolution of 10 fF for a dynamic range of 100 dB. It also rejects stray capacitance (shown as ghosts in Figure 1) by 100 dB. If this rejection isn't important, the switching frequency f can be increased to extend the circuit's bandwidth, which is given by:

$$BW = f(C_{ref} / C_{out})$$

C_{out} should be larger than C_{ref}. The circuit operates from a single 5-V supply and consumes 800 μA. If the capacitances at nodes a and c are kept below 500 pF, the LT1078



1. THIS CAPACITOR BRIDGE measures small transducer capacitance changes even in the presence of large strays, and it rejects noise and cable capacitance.



2. HIGHER RESOLUTION was obtained by modifying the circuit in Figure 1, for cases when capacitance change is small.

micropower dual op amp may be used in place of the LT1413, reducing supply current to a mere 160 μA.

If the capacitance change is small, the circuit can be modified for higher resolution (*Fig. 2*). A JFET-input op amp (LT1462) amplifies the signal before demodulation for good noise performance, and the integrator's output is attenuated by R1 and R2 to increase the sensitivity of the circuit.

If $\Delta Cx << Cx$, and $C_{ref} \approx Cx$, then:

$$V_{out} - V_{ref} \approx V_{ref} (\Delta Cx / C_{ref})[(R1 + R2)/R2]$$

With $C_{ref} = 50$ pF, the circuit has a gain of 5 V/pF and can resolve 2 fF. Supply current is 1 mA. The synchronous detection makes this circuit insensitive to external noise sources and, in this respect, shielding isn't terribly important. However, to achieve high resolution and stability, care should be taken to shield the capacitors being measured. This circuit was used for the fluid-level detector mentioned previously by putting a small trim capacitor in parallel with C_{ref} to adjust offset and by trimming R2 for proper gain.

Bridge circuits are particularly suited for differential measurements. When Cx and C_{ref} are replaced with two sensing capacitors, these circuits measure differential capacitance changes, but reject common-mode changes. CMRR for the circuit in Figure 2 exceeds 70 dB. In this case, however, the output is linear only for small relative capacitance changes.

Voted "Best of Issue"
Electronic Design,
November 4, 1996

Composite Video Sync Stripper

MARK AMARANDOS and JEFF LIES, Harris Corp., Semiconductor Sector, 1503 South Coast Dr., Suite 320, Costa Mesa, CA 92626; (714) 433-0600; fax (714) 433-0682.

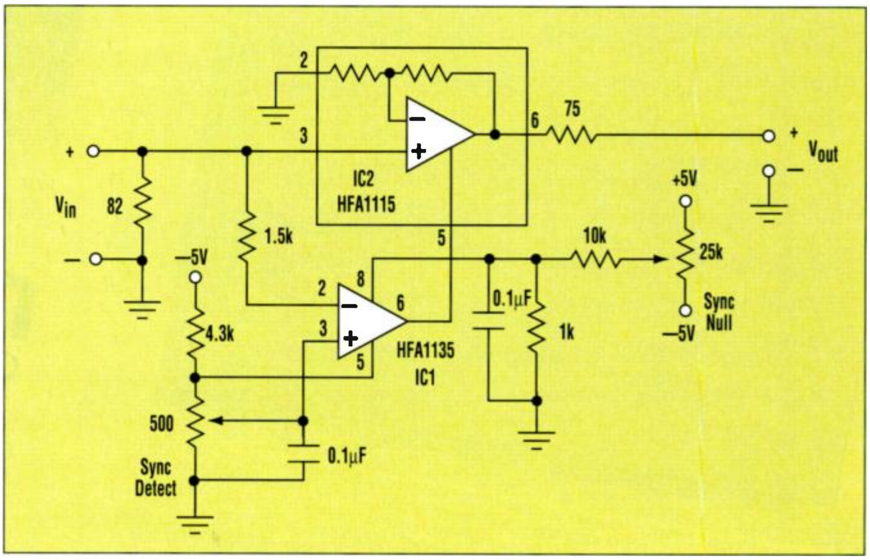
The sync stripper, a common video circuit, often is found in applications where premium channels are scrambled by cable operators so that they can be viewed only by authorized subscribers. Removing the sync pulse makes it impossible for the television receiver to lock onto the video signal, thus producing a highly distorted picture.

In addition, sync strippers are used to remove the sync pulse from video signals preceding analog-to-digital conversion. After removing the sync pulse, the active video portion of the signal may be gained up to the full-scale input range of the converter for better resolution.

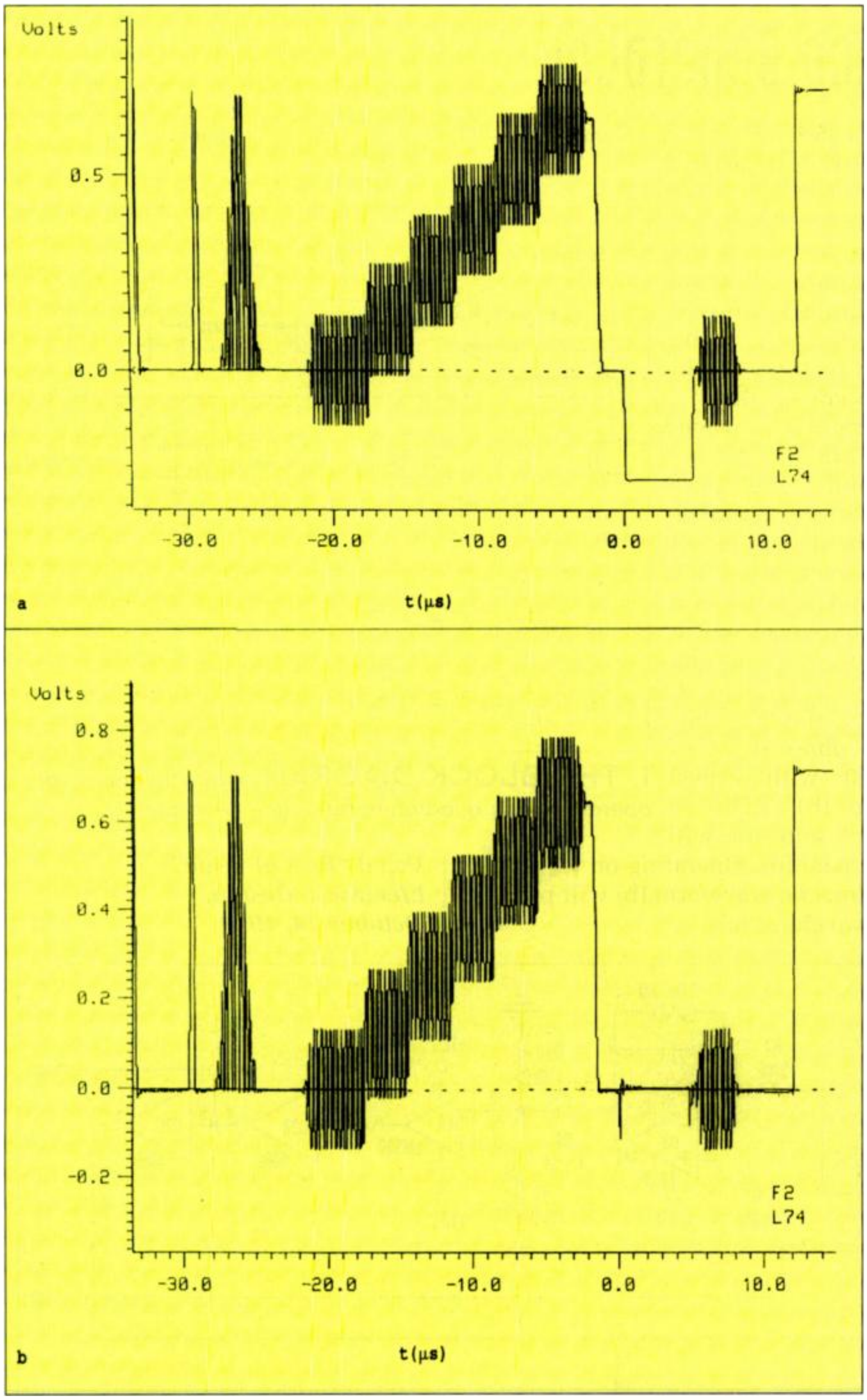
The composite video sync stripper shown consists of an HFA1135 limiting amplifier (IC1) and an HFA1115 limiting buffer (IC2) (*Fig. 1*). IC2 is configured for a gain of 2 in order to provide unity gain while driving a double-terminated 75-Ω line. IC1 is configured as a comparator and performs the sync detect function. The sync detect adjustment is nominally set for a comparator threshold of –0.2 V.

During a sync pulse, the output of IC1 is set by the voltage on its V_H pin. The output of IC1 drives the V_L input of IC2. The sync null potentiometer sets the V_H level for the comparator. It's adjusted for a 0-V output from IC2 during the sync interval. This adjustment eliminates offset errors in the clamp circuit and in IC1. During the sync period, the output of IC2 isn't allowed to go below 0 V, thereby removing the sync pulse.

In a comparison of the sync stripper's input and output waveforms



1. IN THIS VIDEO SYNC STRIPPER, IC1 is configured as a sync detector. Its output drives the VL input of IC2 to 0 V during the sync pulse and thus removes it from the video signal.



2. THE SYNC STRIPPER'S composite video waveform is shown at the input (a) and the output with the sync pulse removed (b).

(*Figs. 2a and 2b*), it can be seen that the active portion of the video signal crosses below 0 V. This is the reason why a simple half-wave rectifier can't be used as a composite video sync stripper.

While this circuit removes the sync pulse, it preserves the full range of the active video portion of the signal. The circuit does produce a glitch that's a few nanoseconds wide, but most receivers won't recognize this glitch as a sync pulse. In sensitive applications, this glitch can be reduced by a low-pass filter.

A simple variation of the circuit may be used to insert sync pulses. This is achieved by setting the comparator stage V_H level to 1 V and the V_L level to –0.3 V. The comparator's input polarity is selected to give a negative-going pulse during the sync interval. That pulse drives the V_H pin of the HFA1115, thereby inserting a –0.3-V sync pulse into the video data stream.

Voted "Best of Issue" Electronic Design, October 14, 1996

ADVERTISERS INDEX

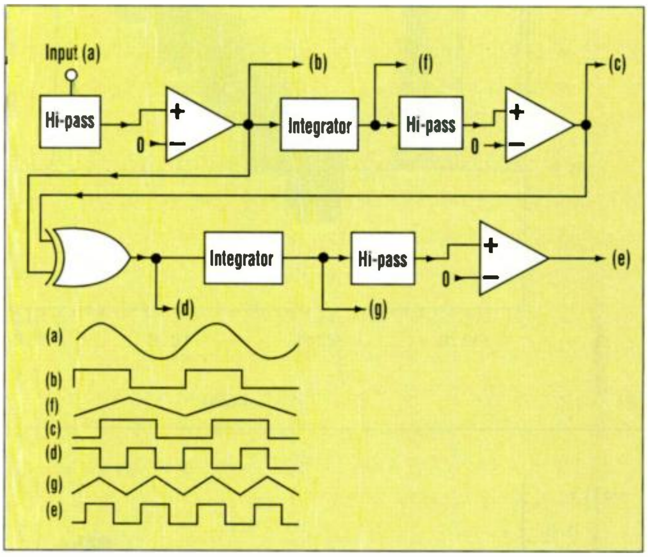
Quadrature Reference Generator

GIOVANNI ROMEO, Istituto Nazionale di Geofisica, Vi di Vigna Murato 605, I-00143 Roma, Italy; telephone: +39-6-51850305; fax: +39-6-5041181; Internet: romeo@marte.ingrm.it.

The circuit described here produces phase-related signals from an input sinewave of slightly variable frequency. The same result may be obtained using a PLL (excluding the use of more sophisticated digital methods), but the PLL approach proves to be less stable and slower to lock than the design shown.

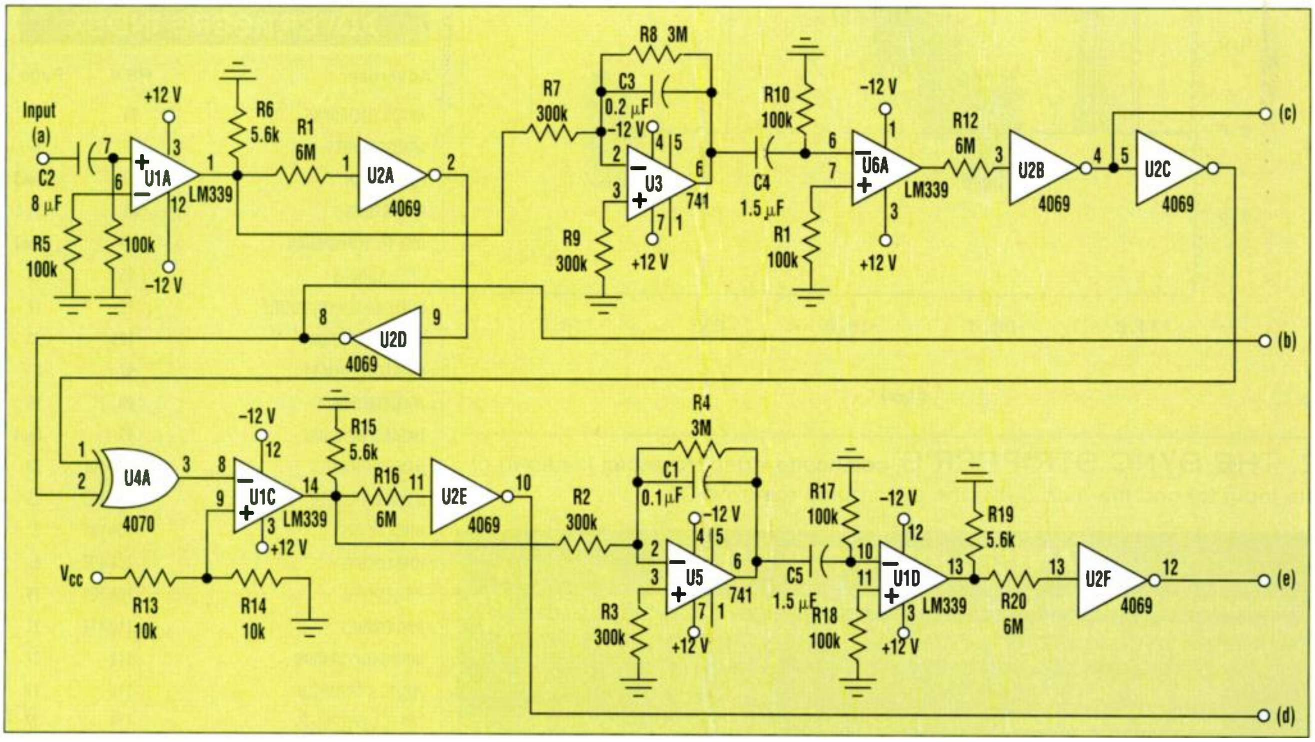
The original purpose of the design was to derive a signal to control lock-in of the mechanical position of an infrared telescope's oscillating mirror (the prototype operation frequency was between 10 and 30 Hz). The oscillation waveform was a sinusoid detected by an LVDT.

Figure 1 shows the theory of operation. The sinusoidal input waveform passes through a high-pass filter, which removes the dc contents of the signal. A zero-cross detector produces a square wave (b) with the same frequency of the input. Passing through a quasi-integrator, the waveform (b) becomes the triangular waveform (f). A second high-pass filter removes the dc content of waveform (f), and a second zero-cross detector produces the waveform (c). Waveform (c) has a phase delay of 90° with respect to (b). XOR-ing (b) and (c) will create (d). Operating on (d) as was done on waveform (b) will produce waveform (e).



1. THE BLOCK DIAGRAM shows the theory of operation for a quadrature reference generator.

Voted "Best of Issue" Electronic Design, October 24, 1996



2. DESIGNED TO WORK with a 17-Hz input, this quadrature reference generator was used to control the mechanical position of an infrared telescope's oscillating mirror.

PM DC Motor Speed Control

KLAUS ACHLEITNER, University of Cape Town, Dept. of Chemistry, Rondebosch 7700, Cape Town, South Africa, tele phone: +27-21-650-2525; fax: +27-21-689-7499; e-mail: Klaus@psipsy.uct.ac.za.

Speed control of permanent-magnet (PM) dc motors with the aid of optical or dc tachometers is generally inconvenient and difficult, particularly on motors with integral gearboxes. The high-speed shaft of the motor that drives the gearbox isn't always accessible and the speed of the geared-down shaft often is too low for tachometers.

Described here is a single-supply regulating speed-control circuit that doesn't require a tachometer. It keeps the motor torque high under load by using positive feedback to compensate for the drop due to armature resistance. In unregulated variable-speed PM dc motor systems, the drop in speed under load is particularly pronounced at low motor supply voltages.

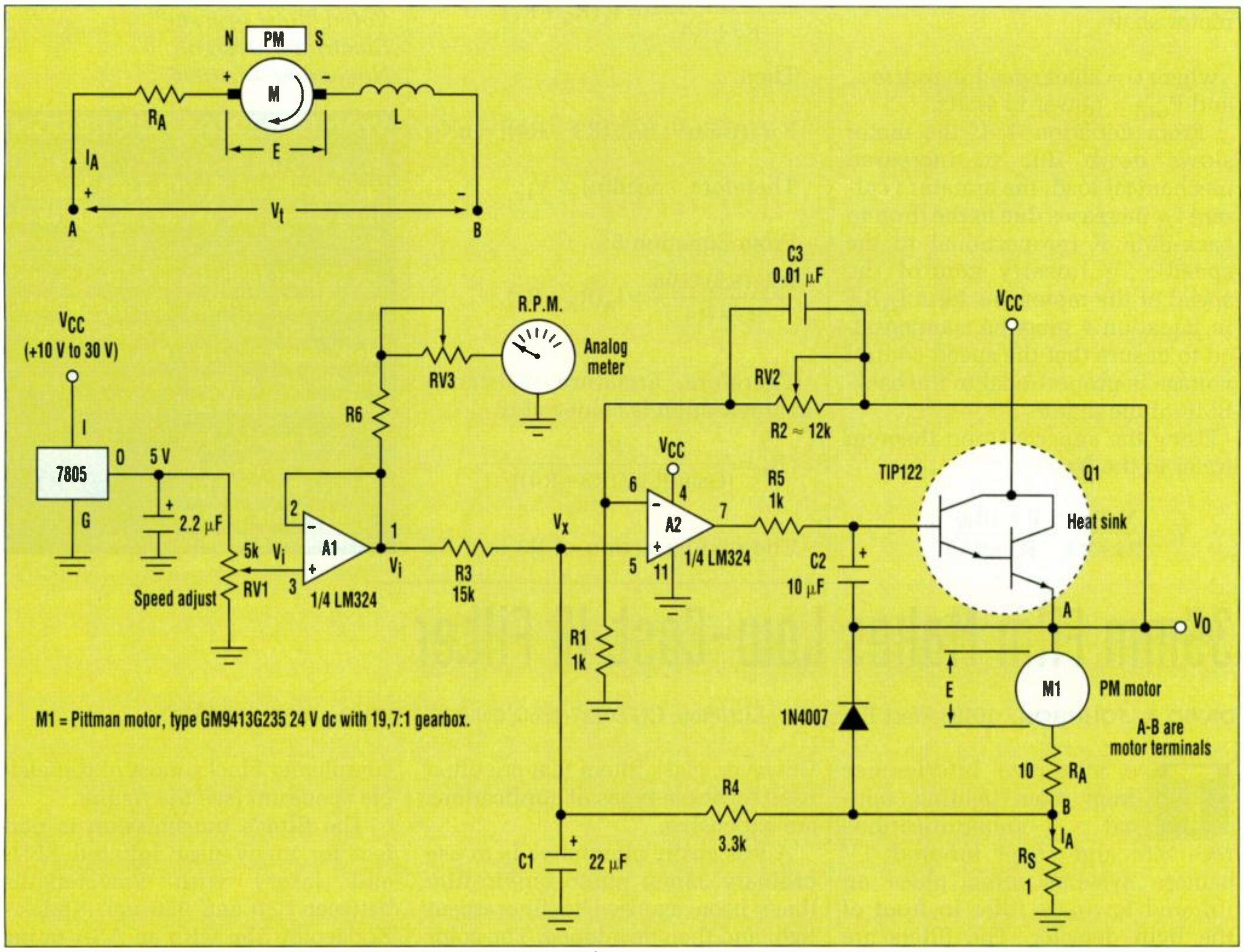
The positive-feedback generates a negative resistance that compensates for the nonlinear effects caused by armature resistance and thereby ensures that the speed-control input voltage (V_i) linearly controls the speed of the motor.

A PM dc motor can be modeled by the equivalent circuit shown in the figure. The steady-state equation for this motor is equal to:

$$V_t = E + I_A R_A \quad (1)$$

where E = back-EMF (V); R_A = armature resistance (Ω); V_t = applied voltage (V); I_A = armature current (A); and L = winding inductance (H), and:

$$E = nK_E \quad (2)$$



THIS SINGLE-SUPPLY SPEED-CONTROL circuit for permanent-magnet dc motors doesn't require a tachometer and keeps the motor torque high under load by using positive feedback. The positive feedback compensates for the drop due to armature resistance.

where speed = n (rpm); K_E = constant (volts/rpm); and K_T = torque constant (N-m/A).

Therefore, from equation 1:

$$V_t = nK E + I_A R_A \quad (3)$$

Consequently,

$$n = \frac{V_t - I_A R_A}{K_E} \quad (4)$$

The torque is proportional to the armature current:

Torque $T = K_T I_A$

where T = damping torque + friction torque + load torque (N-m)

The power output from the motor shaft is:

P_{out} = T ω (watts), i.e., at the motor shaft

where ω = shaft speed in rad/sec., and P_{out} = power in watts.

From Equation 4, if the motor slows down due to increased mechanical load, the armature current I_A increases due to the drop in back-EMF E (proportional to the speed). To linearly control the speed of the motor, the term $I_A R_A$ in Equation 4 must be compensated to ensure that the speed-control voltage is proportional to the back-EMF of the motor.

Using the superposition theorem (refer to the figure):

$$V_x = \frac{V_i(R4)}{R3+R4} + \frac{R_s I_A(R3)}{R3+R4}$$

where R_S I_A= voltage proportional to armature current IA.

Voltage gain for the input noninverting signal = [(R2/R1) + 1] = Gain

Vo = Vx [(R2/R1) + 1]

$V_o = E + I_A R_A + I_A R_S = V_x[(R2/R1) + 1]$

where:

$$E + I_A(R_A + R_S) = \frac{V_i(R4)\ \text{Gain}}{R3+R4} + \frac{R_s I_A(R3)\ \text{Gain}}{R3+R4}$$

Rearranging:

$$E = \frac{V_i(R4)\ \text{Gain}}{R3+R4} + \frac{R_s I_A(R3)\ \text{Gain}}{R3+R4} - I_A(R_A + R_S)$$

However, in the above equation, if:

$$\frac{R_s I_A(R3)\ \text{Gain}}{R3+R4} = I_A(R_A + R_S) \quad (5)$$

Then:

$E = [(\text{Gain}V_i\ R4)/(R3 + R4)] = nK_E$

Therefore, speed(n) ∝ V_i .

From Equation 5:

$$\frac{R_s I_A(R3)\ \text{Gain}}{R3+R4} = I_A(R_A + R_S)$$

Therefore, armature resistance compensation is achieved if:

$$R_S = \frac{R_A}{[\text{Gain}(R3)/(R3+R4)] - 1}$$

The divider action of R3 and R4 together with the Gain reduce the value required for RS to minimize the power dissipation.

C1 and R4 damp the positive-feedback signal's response time, but they also form a low-pass filter and attenuate the motor current noise fed to the A2 input. The maximum output voltage swing from A2 is approximately VCC - 2 V, and there is a 1.2-V Vbe loss by T1. This implies that the supply voltage VCC should be about 5 V above the maximum desired motor voltage in order to allow for extra output drive to the motor under heavy load conditions. A reasonable choice for Rs is approximately RA/10 and the gain of A2 should be trimmed with RV2 to ensure the motor's speed does not drop when loaded.

Voted "Best of Issue"
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November 18, 1996

35mm Film Makes Low-Cost IR Filter

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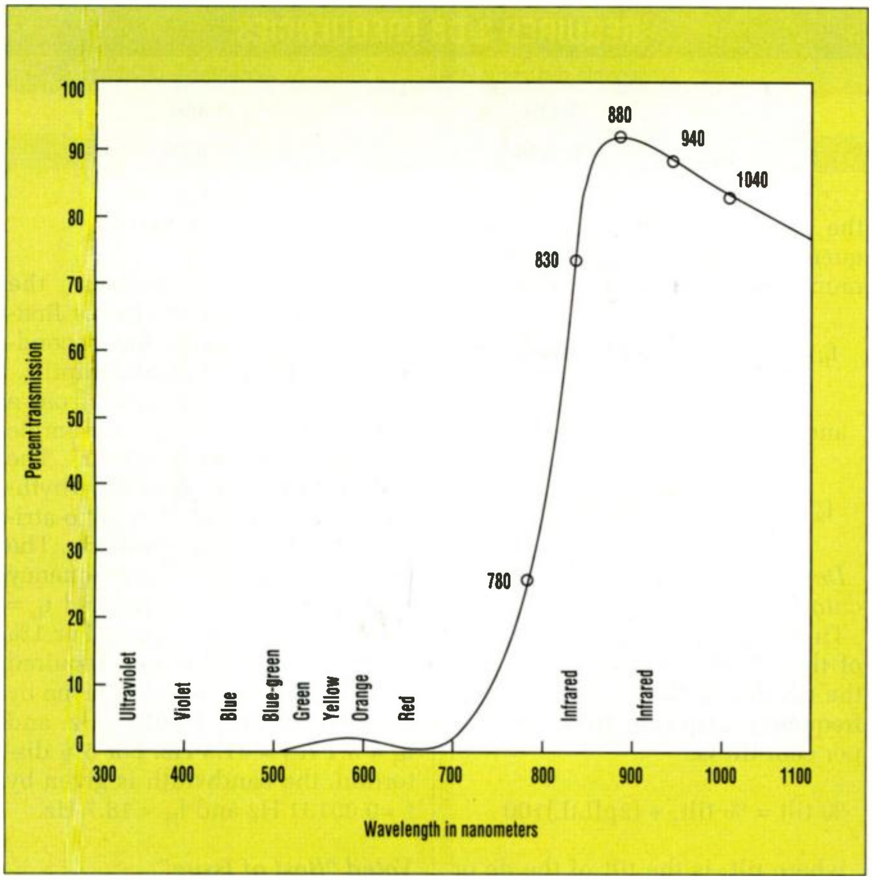
To minimize interference from room lighting, optical communications receivers and some infrared TV camera systems often place an infrared low-pass filter in front of the light detector. The filters are designed to block most of the visible light, allowing the near infrared light to pass and reach the detector. However, glass filters that are often used for these types of applications are expensive.

A less costly alternative is to use ordinary 35mm photographic film that's been exposed to fluorescent light and then developed. The color negative produced after the photographic developing process has a sharp cutoff at about 830 nm and completely blocks most of the visible spectrum (*see the figure*).

The filter's transmission is perfect for many near infrared LEDs and lasers with wavelengths between 830 and 950 nm. Kodak's Kodacolor film with an ASA rating of 100 that's exposed to a "cool white" fluorescent light for five seconds works the best. The film



WHEN EXPOSED TO "COOL WHITE" fluorescent light for five seconds, the color negative (using Kodacolor 100 ASA film) produced after the developing process exhibits a sharp cutoff at about 830 nm.

processor should be told to develop the film in the usual manner but not make any prints. The color negatives become the filter material. A typical 36-exposure roll will cost only about $5.00. The film can be easily cut into any required size or shape. However, the film is not recommended for applications where it can become scratched or exposed to moisture.

Voted "Best of Issue"
Electronic Design,
December 2, 1996

Quick Estimate Of Signal Bandwidth

FRANK T. KOIDE, University of Hawaii, Dept. of Electrical Engineering, 2540 Dole St., Honolulu, HI 96822; (808) 956-7406; fax (808) 956-3427.

Spectral analysis is the typical way to determine the bandwidth required to process a complex signal. But does a simpler and more rapid method exist? Avoiding the rigor of spectral analysis by simply estimating the durations of the high- and low-frequency components of the signal, a quick first-cut approximation of the required high and low 3-dB frequencies is possible.

Determining the high-frequency cutoff:

The effect of high-frequency limiting is obvious as bandwidth decreases (*Fig. 1*). At a bandwidth of 6.2 kHz, which corresponds to an increase of 1% in rise time of the signal, slight rounding of the leading edge is barely noticeable. No change occurs at the trailing edge because fall time exceeds rise time. At 2.8 kHz, or a 5% increase in rise time, rounding of the leading edge is more noticeable. At a bandwidth of 1 kHz , the distortion is obvious.

For a signal with a minimum rise or fall time of t_r and an amplifier bandwidth f_H, the output rise or fall time is degraded to:

$$t_o = \sqrt{t_r^2 + \left(\frac{0.350}{f_H}\right)^2}$$

assuming a high-frequency roll-off of -20 db/decade or a second-order system at critical damping. for an increase in rise or fall time of 1 percent:

$$t_o = 1.01\ t_r = \sqrt{t_r^2 + \left(\frac{0.350}{f_H}\right)^2}$$

and the minimum required bandwidth is:

$$f_H = \frac{0.350}{\sqrt{0.0201}\ t_r} = \frac{2.46}{t_r}$$

or

$$f_H \geq \frac{2.5}{t_r}$$

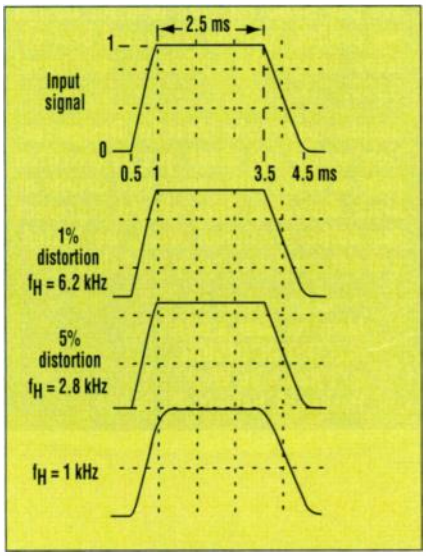
for an allowable increase of 5 percent in rise or fall time, the minimum required bandwidth is given by;

$$f_H = \frac{0.350}{\sqrt{0.1025}\ t_r} = \frac{1.093}{t_r}$$

or

$$f_H \geq \frac{1.1}{t_r}$$

Because data is extracted manually from the waveform, it's quicker to use the duration of the high-frequency component instead of the rise or fall time. Thus, in terms of



1. HIGH-FREQUENCY distortion increases as bandwidth decreases. The test signal is a 1-V, 200-Hz trapezoid with tr = 0.4 ms and tf = 0.8 ms.

REQUIRED 3-DB FREQUENCIES

	Negligable distortion (1%)	Acceptable distortion (5%)
fH	3.1/tH	1.4/tH
fL	0.0016/tL	0.008/tL

the duration of the highest frequency competent t_H, the minimum high-frequency cutoff is:

$$f_H \geq \frac{2.46}{0.8\ t_H} = \frac{3.1}{t_H} \text{ for 1\% distortion}$$

and

$$f_H \geq \frac{1.093}{0.8\ t_H} = \frac{1.4}{t_H} \text{ for 5\% distortion}$$

Determining the low-frequency cutoff:

The output tilt or sag is the sum of the tilt of the input signal and the tilt due to the amplifier's low-frequency response limiting. The per cent tilt is:

$$\%\ \text{tilt} = \%\ \text{tilt}_s + (2pfLtL)100$$

where tilt_s is the tilt of the dc or lowest frequency component of the signal, t_L is the duration and f_L is the amplifier's low-frequency cutoff.

For a 1 percent tilt attributable to the amplifier, the maximum allowable low-frequency cutoff is given by

$$f_L = 1/628t_L = 0.00159/t_L$$

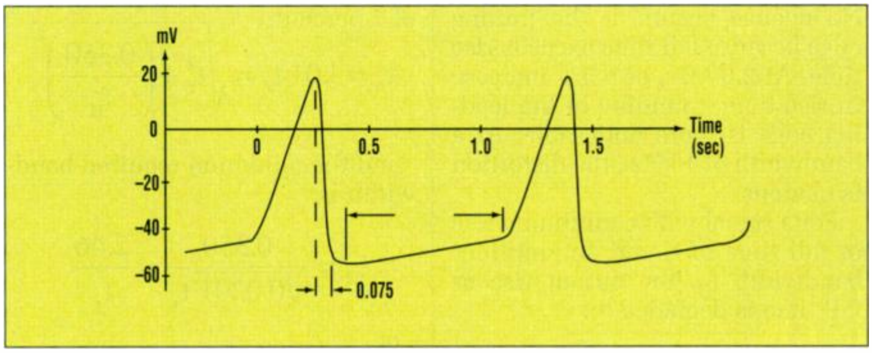
or

$$fL = 0.0016/t_L \cong 0.00016/t_L$$

The table summarizes the required 3-dB frequencies for first-order transfer gains and second-order systems at critical damping.

The waveform generated from a heart pacemaker is a good example for this design idea (Fig. 2). The waveform is typical of the rhythmic discharge of an S-A (sino-atrial) node fiber in heart muscle. The high-frequency and low-frequency durations are t_H = 75 ms and t_L = 0.61 seconds, respectively. For 1% distortion, the minimum required small-signal bandwidth is given by f_L=0.0016/0.61 = 0.00262 Hz, and f_H = 3.1 /t_H = 41.3 Hz. For 5% distortion, the bandwidth is given by f_L=0.00131 Hz and f_H = 18.7 Hz.

Voted "Best of Issue"
Electronic Design
December 16, 1996



2. THIS HEART-MUSCLE WAVEFORM generated from a pacemaker helps to illustrate how the circuit functions. The minimum small-signal bandwidth for negligible distortion is fL = 0.0016/0.61 = 0.00262 Hz and fH = 3.1/tH = 41.3 Hz. Acceptable distortion requires that fL = 0.0131 Hz and fH = 18.7 Hz.

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RTD To RS232 Interface

W. STEPHEN WOODWARD, Venable Hall, CB3290, University of North Carolina, Chapel Hill, NC 27599-3290; Internet: woodward@net.chem.unc.edu.

A popular type of precision temperature sensor is the "100-W" platinum resistance thermometer (PRT) or resistance temperature device (RTD). The well-characterized, highly-stable and nearly-linear temperature response (usually 0.385% per °C) of these sensors, combined with their ability to work over a -200 °C to +200 °C range (much higher in some packages), makes them versatile and robust.

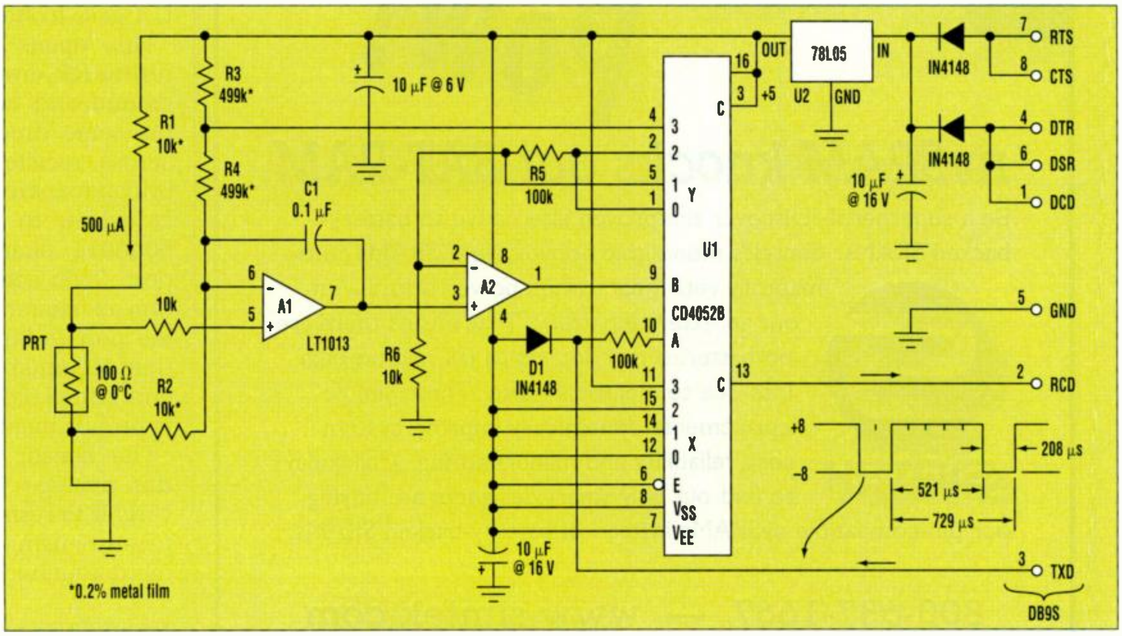
The circuit shown (*see the figure*), combined with simple software (*see the listing*), represents an accurate, simple, and inexpensive interface that works with any MS-DOS-compatible PC with an RS-232 port.

The transducer obtains operating power from the port, so no additional power supply is needed here. It achieves accuracy to better than ±1 °C with no internal precision components, except for four resistors

The values given cover the 0 to 180 °C temperature range and achieve nearly 0.1 °C resolution at a 1-Hz conversion rate. "Four-wire" excitation and sensing of the PRT reduces errors from sensor lead resistance by a factor of 100. Sensor excitation current is a low 500 µA, limiting sensor power dissipation to 25 µW, thus holding self-heating error to << 0.1 °C.

The PRT is connected in a bridge consisting of R1, R2, and the series combination of R3 and R4. LT1013 integrator A1 accumulates any imbalance signal from the bridge, which nulls when Rprt/R1 = R2/(R3 + R4). This occurs near Rprt = 100 Ω for the values shown: 100/10 k = 10 k/l Ω. For higher temperatures, Rprt > 100 Ω and A1's output ramps up.

```
SCREEN 1:
CLS:PRINT " ********************************
   PRINT " ****** PRT"; CHR$(196); CHR$(16);" RS232 demo *********
   PRINT "***********************************
   LOCATE 6, 1:PRINT"RTD Temp, Ohms=";

' 18.2065...# of MSDOS-compatible Time-of-Day "ticks"/second
DEF SEG=0:'T.O.D. clock lives at memory addresses (&H46C,D)

'Generate PRT readout string
prt$ ="": FOR i%=1 TO 1342: prt$=prt$ + CHR$(&H1 0):NEXT

DIM t%(1342), r%(1342):'Generate temperature and resistance lookup tables
FOR i%=0 TO 1342
  rtd =.0522 * (1900 + i%): 'convert index to resistance
  r%(i%) = 100 * rtd
t%(i%) = ((((((2.24696.E-06*rtd) - 1.06721E-03)*rtd)+.287283)*rtd) + 221.574)*rtd -
24189.1
 NEXT

' Setup COMport to accept PRT character stream
    OPEN "COM1:9600,N,5,1,BIN,RB2000,TB2000" FOR RANDOM AS #3

Thermometer
 PRINT #3, prt$;: ' Drive PRT resistance -> digital conversion
 sum%=0: ' Reset PRT character tally
 FOR tclk% = 1 TO 18: 'Sum PRT pulses for 18/18.2065Hz=0.9887 second
   y%=PEEK(&H46C): WHILE PEEK(&H46C)=y%; WEND: ' Await a T.O.D. tick
   x%=LOC(3): sum%=sum% + x%: a$=INPUT$(x%,3):
   NEXT
 LOCATE 6, 17
 temp = t%(sum%)/100: PRINT USING "###.#": temp;: PRINT CHR$(248);"C";
 PRINT USING"###.#"; temp * 1.8 + 32;: PRINT CHR$(248);"F";
 PRINT USING"###.##"; r%(sum%)/100;: PRINT CHR$(234);
 GOTO Thermometer
```



COMBINED WITH SIMPLE SOFTWARE, this circuit becomes an accurate, inexpensive RTD interface that works with any MS-DOS compatible PC with an RS232 port.

Comparator A2 combines with the dual CD4052B multiplexer U1 to close the feedback loop around A1 by periodically shorting across R2, thus increasing the average value of the denominator in the right side of the bridge equation.

This restores bridge balance for temperatures as high as 180 °C. Note that the ratiometric nature of the bridge topology makes conversion accuracy insensitive to power-supply drift, so no precision voltage reference is needed.

Digitization of sensor resistance is driven by RS232 characters of the binary pattern (including start/stop bits) of 0000011, transmitted by the PC COM port on "TXD."

As usual, "0"s are represented by positive voltage on the RS-232, and "1"s by negative voltage. With the arrival of each character, U1 samples the state of A2's output. If low, indicating bridge balance, U1 goes into state 1 of its four possible states.

This shorts across resistor R5, driving pin 2 of A2 to 5 V and latching A2 low for the remainder of the character time. Meanwhile, state 1 holds the "RCD" line negative, so the COM port receives no character. If, however, A2's output is high, indicating bridge imbalance, U 1 goes to state "3".

This opens the connections to resitor R5, dropping pin 2 of A2 to ground and latching A2 high. At the same time, a short is placed across resistor R3, nudging the bridge toward balance, and "RCD" is driven to +5 V, echoing the 0000011 character to the COM port. This action causes the fraction of characters echoed back to the port to be proportional to the time R3 must be shorted to maintain bridge balance, and, therefore, is proportional to Rprt.

The sensor program computes this average frequency and converts it to resistance and then temperature using a 4th-order linearizing polynomial.

Voted "Best of Issue" Electronic Design, January 6, 1997

SCA Receiver Demodulates Additional Subcarriers

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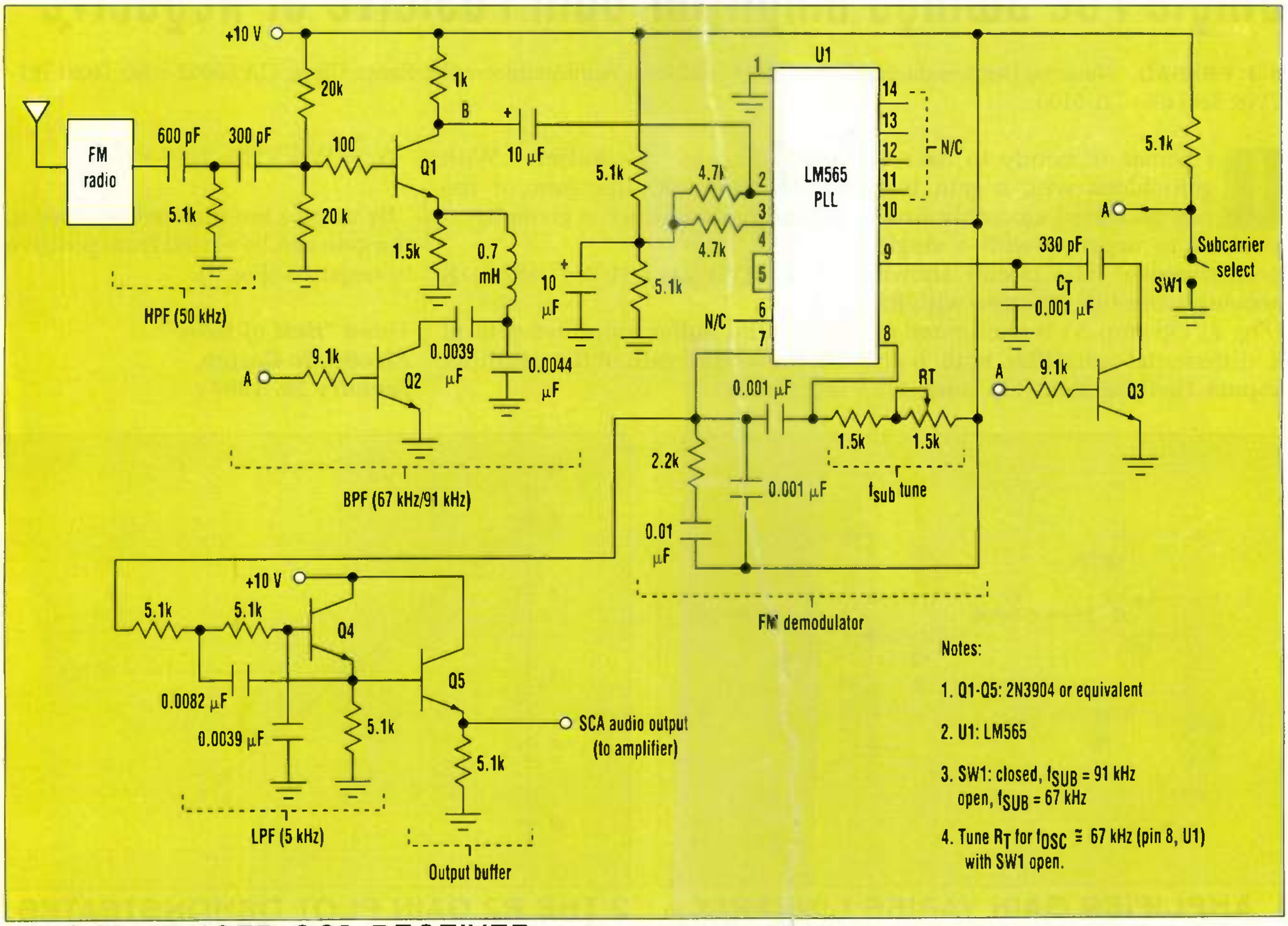
The FCC has authorized some FM radio stations to broadcast uninterrupted background music for commercial use on one or more FM subcarriers. This service is known as subsidiary carrier authorization (SCA). It is done via a frequency-modulated subcarrier, typically at 67 kHz.

However, in some cases, additional subcarrier(s) are present. Each of these subcarriers is FM-modulated with different program material. A common second subcarrier frequency is 91 kHz. These frequencies were chosen so as to minimize interference with the normal stereo programming. They're also present at a much lower level than the main channel information, usually at only about 5 to 10% FM deviation of the main carrier frequency. This SCA receiver can provide commercial-free music from one of two possible carriers. The SCA signal is monaural, and is relatively wideband (7 kHz). This bandwidth is adequate for reasonable quality music transmission.

A simple PLL-based FM demodulator can be made to demodulate these two subcarriers and provide a source of background music. A couple of references help to illustrate a simple SCA receiver design[1], and the basics of the PLL FM detector[2]. The receiver described here provides some enhancements to that basic design, such as better selectivity, the choice of two possible subcarriers, and an optional squelch circuit (*see the figure*).

The input to this receiver is fed from the wideband audio output from an FM radio's first FM detector. This is the point that feeds the FM stereo demodulator in an FM receiver. Care should be taken so that the signal is tapped off at a point that hasn't yet been filtered (subcarrier(s) are still present).

This FM input signal is then



THIS ENHANCED SCA RECEIVER provides improved selectivity over a typical SCA receiver. It also offers the listener a choice of two possible subcarriers to make use of all subcarriers currently in popular use.

passed through a second-order high-pass filter and peaker stage (Ql), which serves to bandpass and provide additional gain within the input spectrum prior to the FM demodulator input. The FM detection is accomplished by a simple LM565 PLL IC (U1) operating as an FM demodulator.

The PLL's VCO is tuned to 91 kHz via RT/CT. The demodulated output signal is available at pin 7, which is followed by a second-order LPF/buffer combination (Q4). The characteristics of this filter can be modified to suit the user.

The design shown has an audio corner frequency of about 5 kHz. The filtered output is the recovered audio output and is the input to an audio amplifier. To choose the second subcarrier (67 kHz), the peaker and VCO are gang-tuned by the Q2 and Q3 saturating switch transistors. These devices switch in appropriate valued parallel capacitors to retune the peaker and VCO to the proper frequency for reception of the second subcarrier signal.

Circuit values shown are for an FM level of about 50 to 300 mV rms at the input to the peaker stage. In addition, the PLL dynamic characteristics can be altered as desired by modifying the loop filter2. The typical recovered audio level at pin 7 of U1 is 200 mV rms. Other enhancements could include a "squelch" circuit, which mutes the demodulator's output if the input carrier frequency is lost.

To receive SCA signals, the FM receiver can simply be tuned to normal FM stations and then the presence of either or both subcarliers can be checked. Checking c. be done with a spectrum analyz or by simply listening to the SC receiver output on each of the tw subcarriers. A list of FM radio st tions in a particular region th carry SCA (and at what subcarri frequencies) may be available.

One caveat: The SCA service typically a pay-for-use servic thus the receiver should not b used for commercial applications.

References:
1.V. Lakshminarayanan, Electronic Circuit Design Ideas
2.National Semiconductor Linear Applications Databook, 1986 edition (AN46 and AN146).

Voted "Best of Issue"
Electronic Design,
February 3, 1997

Single Pot Swings Amplifier Gain Positive Or Negative

S.J. PRASAD, National Semiconductor Corp., MS Al-555,2900 Semiconductor Dr., Santa Clara, CA 95052-8090; (408) 721-7178: fax (408) 721-5100

It comes in handy to have a gain block with a gain that can be varied smoothly from positive to negative with a single potentiometer. The circuit shown accomplishes this function with R2 (*Fig. 1*). Op amp A1 is configured as a differential amplifier with both inputs tied together. Op amp A2 functions as a buffer. With Rl=R3=R4=R=5k, the gain of the differential amplifier is given by:

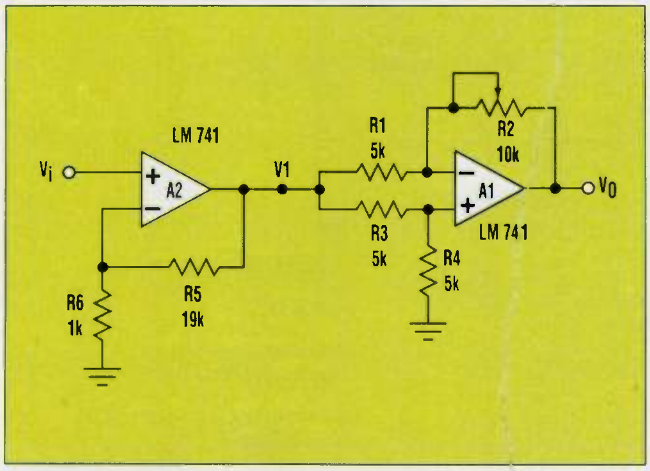
$$A_{V1} = (V0/V1) = (1/2)(1-(R2/R1))$$

With the buffer amplifier gain of 20, the overall gain of the amplifier is given by:

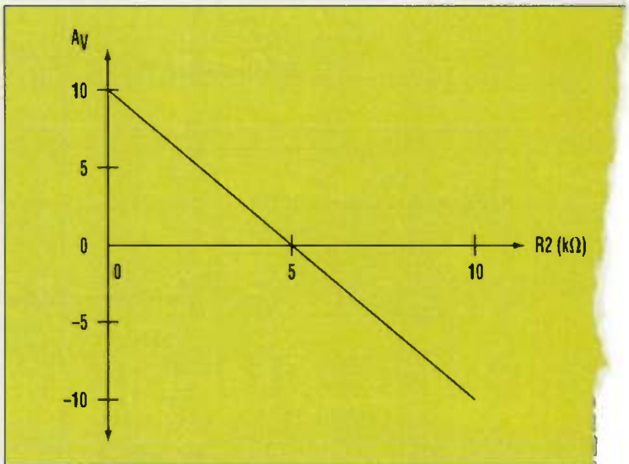
$$A_V = (V0/V1) = 10(1-R2/R1)$$

By using a ten-turn potentiometer the gain can be varied from positive to negative (*Fig. 2*).

Voted "Best of Issue"
Electronic Design,
January 20, 1997



1. AMPLIFIER GAIN VARIES LINEARLY in this circuit with adjustment of potentiometer R2, providing positive and negative gains.



2 THE R2 GAIN PLOT DEMONSTRAT the smooth variation from positive to negative gain in gain block circuit.

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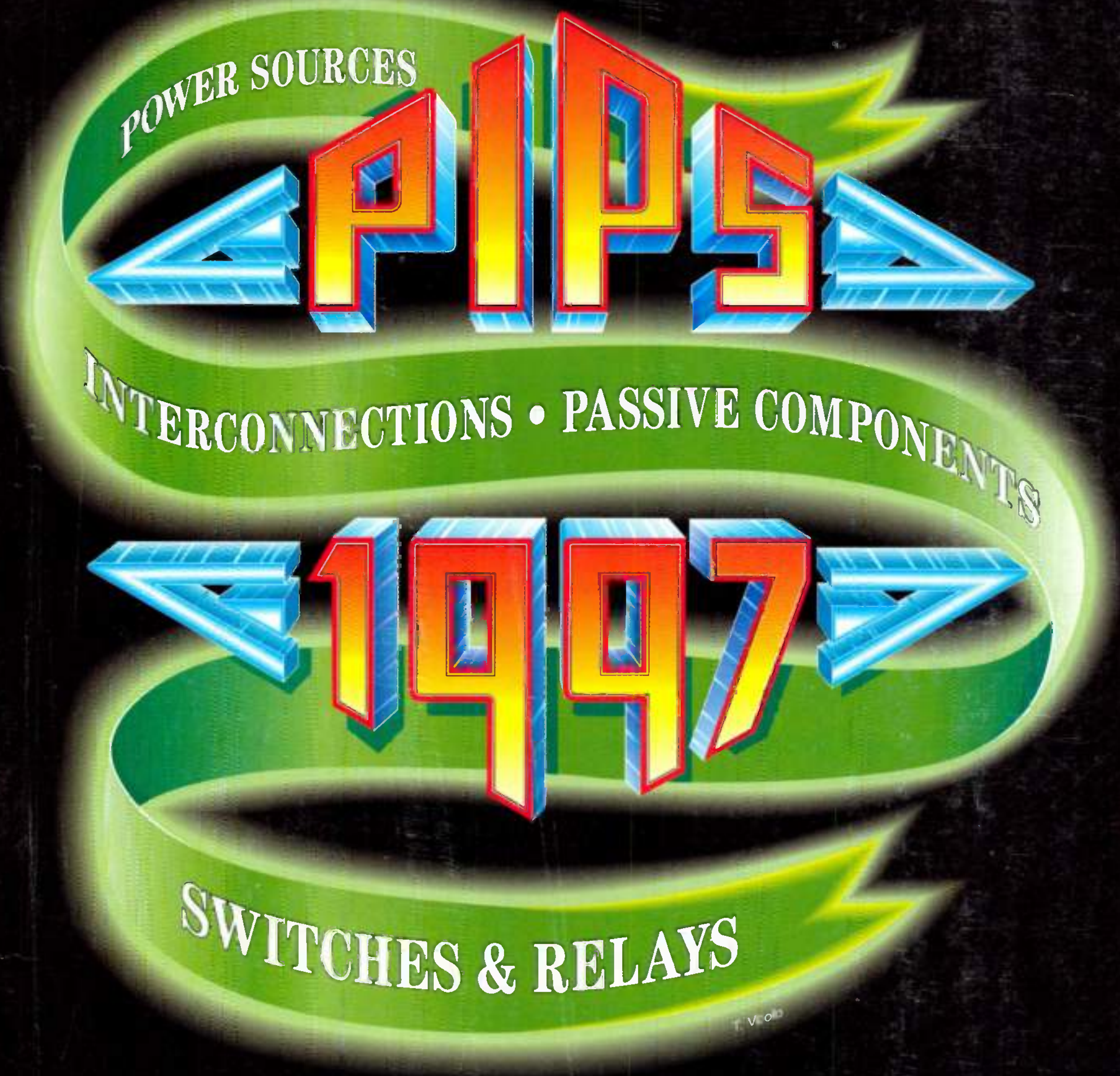
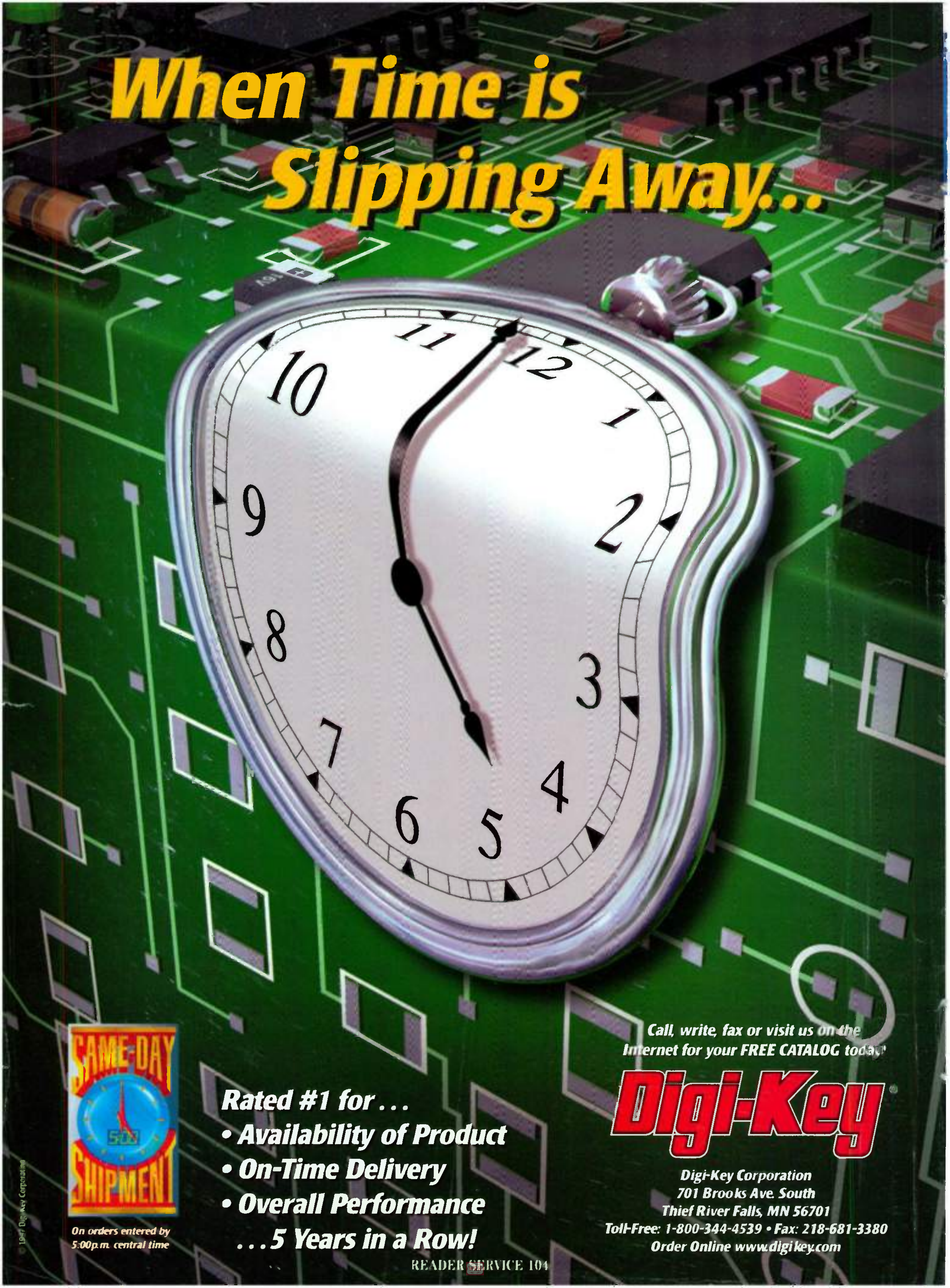


"PIPS" HIGHLIGHTS FROM 1997



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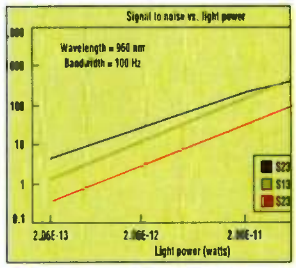
PIPS FEATURES


21



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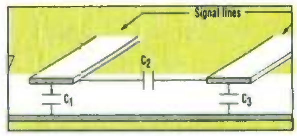

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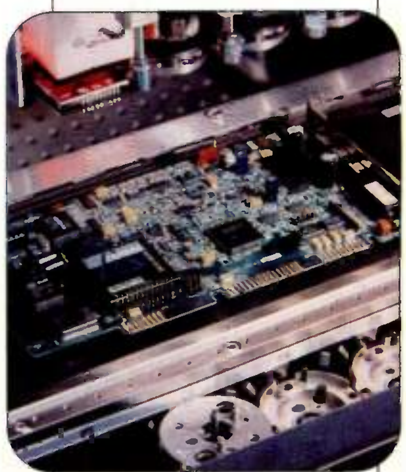

37

Welcome to Electronic Design's second annual PIPS Supplement, a compendium of feature articles and manufacturers listings of a broad range of products that comprise the backbone of electronics technology: power supplies, interconnections, passive components, and switches and relays. The PIPS section appears monthly in Electronic Design, usually in the first issue of each month, with each installment giving special focus to a particular product area, while also covering new products in all four of the basic areas.

The PIPS sections are designed to cover topics that are vital to total system design, but can be overlooked in reporting the rapid-fire developments--the latest whiz-bangs--in today's fast-moving electronics industry. Nevertheless, these more mature product areas are filled with innovation, albeit usually quiet ones, as the latest microprocessors and signal-processing chips. The need to cover such developments led the editors of Electronic Design to establish the PIPS sections in 1990 as a way of carrying out our commitment to deliver all the information important to today's designers.

In this edition, we have collected many of the feature articles that have appeared in the PIPS sections during the past year. The articles cover a wide range of technologies, from power converters to optical detectors to connectors and cooling technologies. Each article is authored by a specialist in the field. Taken together, they represent a strong statement of the vigorous quest for innovation by designers engaged in these technologies, which matches the efforts of those working in the top semiconductor laboratories. In many ways, the design and application of some of these "mature" technologies is where the real engineering comes in when designing today's systems. These technologies often bear the brunt of the unpleasant ancillary effects created by the more glamorous developments in high-profile technologies. The challenges involving thermal design, EMI suppression, and power control call for a breadth of engineering knowledge that is unmatched in most other fields.

Looking ahead to next year, here's the lineup of topics we have planned as special features in the PIPS sections in Electronic Design for 1998:

January: Power Converters
February: Interconnects
March: Passive Components
April: Optoelectronics
May: Motor Controls
June: Packaging
July: Power Management
August: Board-Level Interconnects
September: Passive Components
October: Fiber Optics
November: Power Supplies
December: Packaging

As we pointed out in last year's PIPS Supplement, it takes a strong commitment to our readers' total information needs, and a recognition of the importance of these technologies, to consistently publish new and useful information on them.

STEPHEN E. SCRUPSKI
Editorial Director

Optical Detector Selection: A Delicate Balancing Act!

EARL HERGERT
Hamamatsu Corp., 360 Foothill Rd., PO Box 6910, Bridgewater, NJ 08807; (800) 524-0504; fax (908) 231-1218.

For Optimum System Performance, The Optical Detector Must Be Matched Carefully To Its Amplifier.

Selecting the correct optical detector can be one of the most critical aspects of designing a viable instrument. While manufacturers' catalogs can give much useful data about the detectors themselves, they don't paint a complete picture. Designers must combine a knowledge of the performance features of the various solid-state detector devices available with an awareness of how amplifiers can affect those features. An incorrect match can seriously compromise overall system performance.

When considering a detector-amplifier combination, it is critical to define the application. Factors such as light power, bandwidth, wavelength, power consumption, and cost will often dictate the detector technology to be used. The most popular options are a photodiode, a p-i-n photodiode, or an avalanche photodiode (APD).

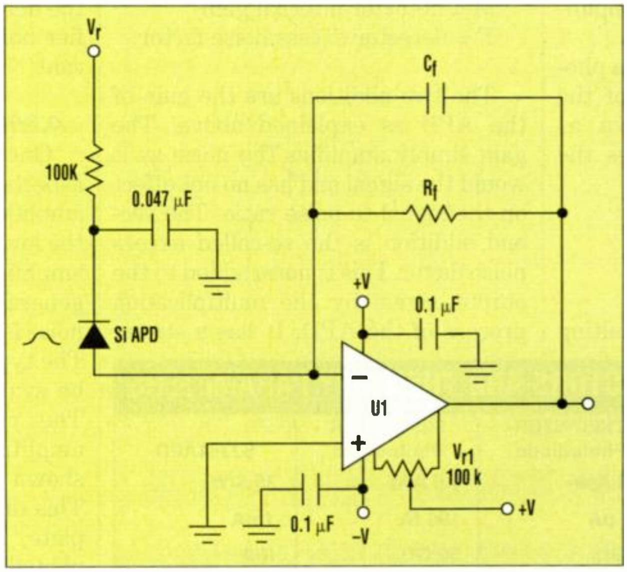
A silicon photodiode is essentially a pn junction consisting of a positively-doped p region and a negatively-doped n region. Between these two regions lies a neutral region known as the depletion region. When light enters the device, electrons in the crystalline structure become excited. If the light energy is greater than the band gap energy (Eg) of the material, electrons will move into the conduction band. This creates holes in the valence band where the electrons were originally located.

These electron hole pairs are created throughout the device. Electron hole pairs generated in the depletion region drift to their respective electrodes—n for electrons and p for holes. This results in a positive charge build up in the p layer and a negative charge build up in the n layer.

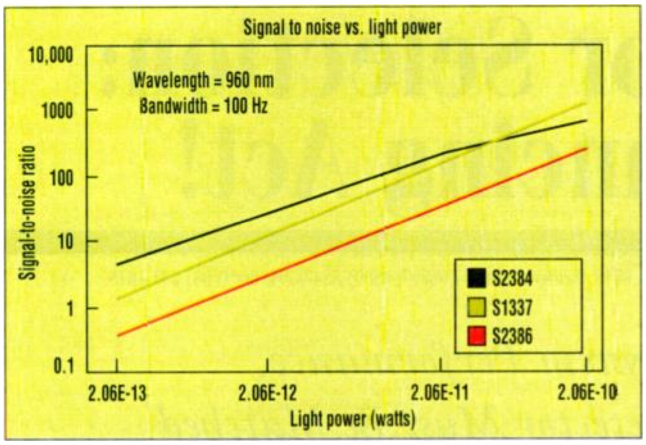
The amount of charge is directly proportional to the amount of light falling on the detector. If an external circuit is connected to the p and n electrodes, current will flow in the circuit.

The above describes the photovoltaic mode of operation. It also is possible to apply a reverse bias to the photo detector. Known as the photoconductive mode, this method is generally used for p-i-n photodiodes and APDs , and has the effect of increasing the electrical field strength between the electrodes as well as the depth of the depletion region. The advantages of photoconductive operation are higher speed, lower capacitance, and better linearity. But since the dark current depends on the reverse bias voltage, the dark current becomes larger with increasing bias voltage.

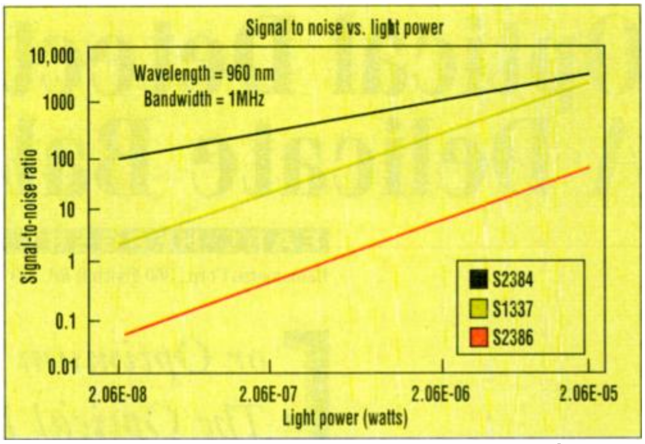
The APD is a specialized silicon p-i-n photodiode designed to operate with high reverse-bias voltages. Large reverse voltages generate high electric fields at the pn junction. Some of the electron hole pairs passing through or generated in this field gain sufficient energy (greater than the bandgap energy) to create additional electron hole pairs in a process known as impact ionization. If the newly-created electron hole pairs acquire enough energy, they also create electron hole pairs. This process is known as avalanche multiplication and is the mechanism by which APDs produce internal gain. Internal gain is an



1. Knowledge of amplifier noise generation is essential if a proper match is to be made between the detector and the amplifier—a necessary feature of any viable system. The transimpedance amplifier shown is one of many possible amplifier configurations.



2. In narrow-bandwidth applications, the photodiode yields better performance than the APD when the amplifier's noise is no longer a factor.



3. Because the APD's gain boosts the signal above the amplifier's noise, it's a good choice for wide-bandwidth applications.

important attribute when the detector is combined with an amplifier, as we shall see later.

The noise in a photodiode can take one of two forms.

The first is the shot noise of the dark current, which results from the statistical uncertainty in the arrival rate of photons. Shot noise is present in all signals, and can be described with the following equation:

$$I_{dark} = \sqrt{2qi_{dark}B}$$

where

i_{dark} = rms noise current

q = electron charge

I_{dark} =photogenerated signal current

B = bandwidth of detector-amplifier combination

The second noise source for a photodiode is the thermal noise of the shunt resistance. Also known as Johnson noise, this noise takes the form of:

$$I_{jRsh} = \sqrt{\frac{4kTB}{R_{sh}}}$$

where

I_{jRsh} = rms noise current resulting from Johnson noise

k = Boltzmann's constant

T = absolute temperature of the photodiode

R_{sh} = shunt resistance of the photodiode

The shot noise will dominate in photoconductive operation, while the Johnson noise will dominate in photovoltaic mode.

Since an APD is always operated in the photoconductive mode, its noise takes the same form as the photodiode dark current shot noise, with the addition of a few terms:

$$I_{APDdark} = \sqrt{2qi_{dark}M^2FB}$$

where

M = detector internal gain

F = detector excess noise factor

The two additions are the gain of the APD as explained above. The gain simply amplifies the noise as it would the signal and has no net effect on the signal-to-noise ratio. The second addition is the so-called excess noise factor. This is noise added to the output signal by the multiplication process of the APD. It has a strong dependence on wavelength as well as gain.

So far, only the noise equivalent power (NEP) has been a factor in detector selection. As the light level increases, however, the NEP no longer plays a role in the signal-to-noise ratio. The shot noise of the signal itself tends to dominate the signal-to-noise ratio, as shown by:

$$I_{signal} = \sqrt{2q(i_{signal}+i_{dark})M^2FB}$$

where

i_{signal} = photogenerated signal before gain

If the application has strong light signals, one would only need to consider the shot-noise performance of the detector, as dark noise and amplifier noise will be relatively insignificant.

AMPLIFIER SELECTION

One of the most overlooked aspects of detector selection is the amplifier. The amplifier usually sets the lower noise floor for the detector-amplifier combination. Therefore, a general understanding of amplifier noise is helpful in choosing a detector. The type of amplifier circuit that will be evaluated here is shown (*Fig. 1*). The circuit is a transimpedance amplifier and the noise equations shown apply to that configuration. This discussion is by no means complete, however. The design of the photodiode amplifier is very complex and volumes have been written on the subject (*see References at end of article*).

Amplifier noise can be broken

TABLE 1: SELECTED DETECTORS AND THEIR KEY PARAMETERS

Parameters	S1337-33BR Photodiode	S2386-33BR Photodiode	S2384APD
Sensitivity (S)	0.6 A/W	0.6 A/W	30 A/W
Dark Current (i_{dark})	10 pA	100 fA	1 nA
Shunt resistance (Rsh)	1 GΩ	50 GΩ	N/A
Terminal Capacitance (Ct)	65pF	4300 pF	40 pF
Excess Noise Factor (F)	1	1	3.7
Gain (M)	1	1	60

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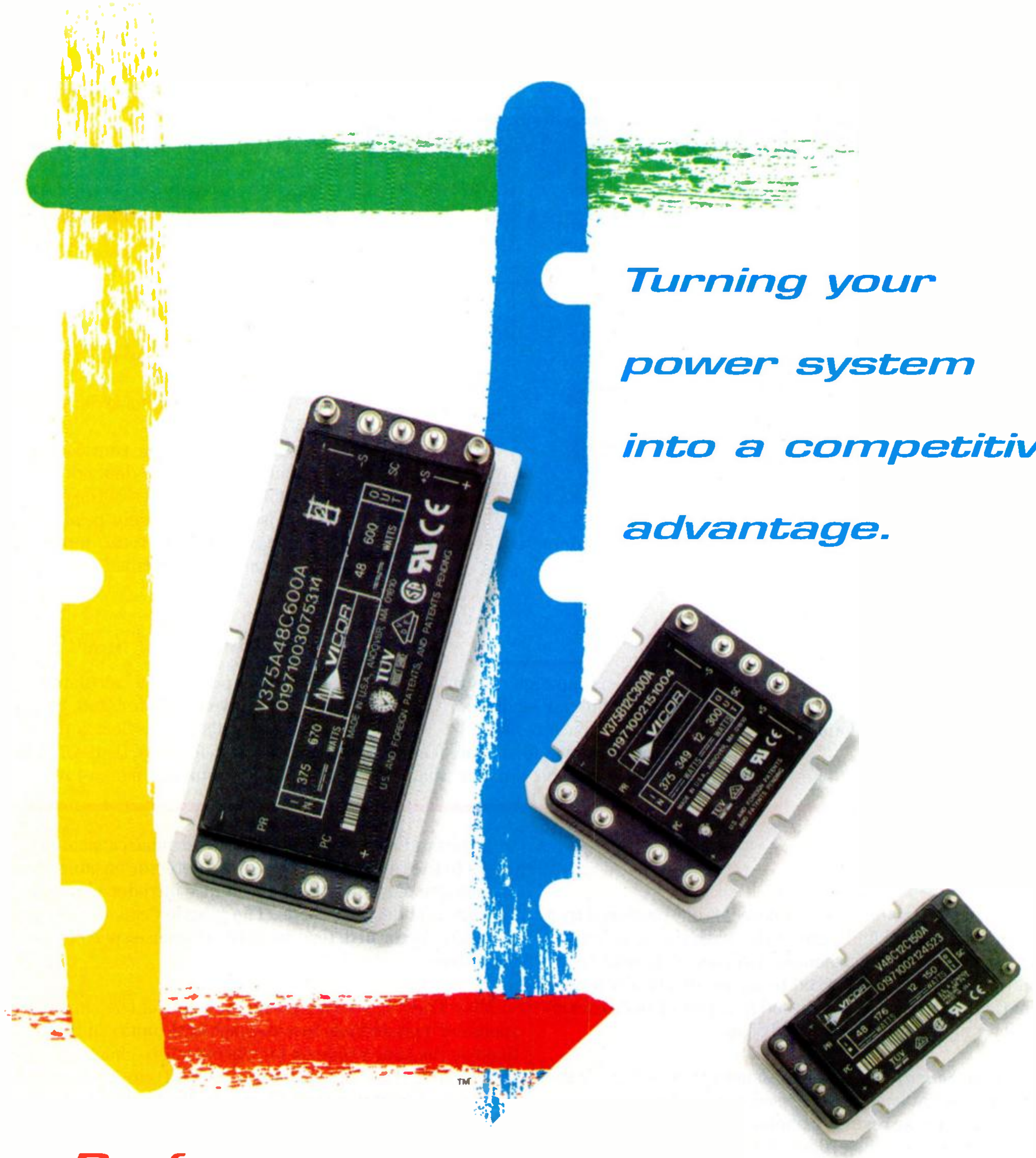

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TABLE 2: SELECTED DETECTORS AND THEIR KEY PARAMETERS

Parameters	S1337-33BR Photodiode	S2386-33BR Photodiode	S2384APD
I_{dark}	1.8e-14	1.7e-15	—
I_{apdark}	—	—	2.6e-12
I_{Rsh}	4e-14	5.7e-15	—
I_B	5.6e-15	5.6e-15	5.6e-15
I_f	4e-14	4e-14	4e-14
I_v	3.5e-15	2.3e-13	3.6e-17
I_{tot}	6e-14	2.3e-13	2.6e-12
NEP Detector + Amp	1e-13Wrms	3.8e-13Wrms	8.6e-14Wrms
NEP Detector	7e-14	9.9e-15	8.6e-14

Bandwidth = 100Hz, feedback resistor = 1GΩ, amplifier bias current = 1 pA, input noise voltage = 15 nV/Hz $^{1/2}$

down into three major components. The first two should seem familiar as they take the same form as the photodiode shot noise and Johnson noise. The first term is the shot noise of the amplifier input bias current (I_b). As a general rule, this current is much lower than the photodiode dark current, therefore it seldom presents a problem.

The second term is the Johnson noise of the amplifier feedback resistor, I_f, given by:

$$I_f = \sqrt{\frac{4kTB}{R_f}}$$

where

I_f = rms current due to Johnson noise of amplifier feedback resistance

R_f = feedback resistor

Since the value of the feedback resistor must be smaller than the shunt resistance of the photodiode, this term often dominates the amplifier noise.

The third term arises from the input voltage noise of the amplifier, and it takes the form:

$$I_v = \sqrt{V_a^2 \frac{4\pi^2}{3} c_t^2 B^3}$$

where

I_v = rms current noise due to voltage noise of amplifier

V_a = input voltage noise density ($nV/(Hz)^{1/2}$)

The voltage noise current is interesting in that it is very dependent on the terminal capacitance of the detector. It also is very closely related to the bandwidth. The total detector-amplifier noise is described by:

$$I_{tot} = \sqrt{(I_{dark})^2+(I_{Rsh})^2+(I_b)^2+(I_f)^2+(I_v)^2}$$

It is now possible to calculate the NEP for a given detector, and, based on these calculations, select a detector that is best for a particular application. It is useful to make a table of

Glossary

Spectral Response—The photocurrent produced by a given level of incident light varies with the wavelength. This relationship between the photoelectric sensitivity and wavelength is referred to as the spectral response characteristic and is expressed in terms of photo sensitivity, quantum efficiency, and so on.

Photo Sensitivity—This measure of sensitivity is the ratio of radiant energy expressed in watts (W) incident on the device, to the resulting photocurrent expressed in amperes (A). For example, 0.5 A/W

Quantum Efficiency (QE)—The quantum efficiency is the number of electrons or holes that can be detected as a photocurrent divided by the number of incident photons. This is commonly expressed in percent (%).

Dark Current (I_{dark})/*Shunt Resistance* (R_{sh})—The dark current is a small current that flows when a reverse voltage is applied to a photodiode, even in a dark state. This is a source of noise for applications in which a reverse voltage is applied to photodiodes (for example, as with p-i-n photodiodes). In contrast, for applications where no reverse voltage is applied, noise characteristics are figured out from the shunt resistance. This shunt resistance is the voltage to current ratio in the vicinity of 0 V.

Terminal Capacitance (Ct)—The terminal capacitance refers to the total capacitance of the detector pn-junction capacitance plus any stray capacitance introduced by the package and detector leads. The junction capacitance is the major factor in determining the response speed of the photodiode.

Rise Time (t_r)—This is the measure of the time response of a photodiode to a stepped light input, and is defined as the time required for the output to change from 10% to 90% of the steady output level. It depends upon the incident light wavelength and the load resistance.

Cut-Off Frequency (f_c)—This refers to the response of high speed avalanche and p-i-n photodiodes to a sinewave-modulated light input. It is defined as the frequency at which the photodiode output decreases by 3 dB.

Frequency Bandwidth(B)—Defined as the frequency range of the detector system, it is generally limited by the response speed of the detector amplifier. If the detector is limiting the response speed, the Frequency Bandwidth will equal the cut-off frequency.

Noise Equivalent Power (NEP)—The NEP is the amount of light equivalent to the noise level of a device. Stated differently, it is the light level required to obtain a signal to noise ratio of unity. NEP is measured at a bandwidth of 1 Hz and thus expressed in units of $W/\sqrt{Hz}$.

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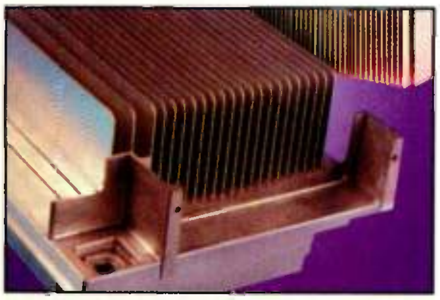

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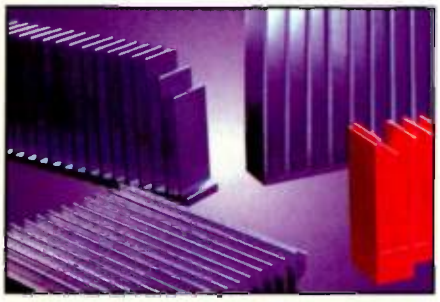

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the various devices under consideration and see what parameters affect performance the most (*Table 1*). As can be seen from the table, the S1337 photodiode is designed for low capacitance, the S2387 for low dark current, and the APD to produce gain. The devices were selected with approximately the same active area size.

The same amplifier will be used in the calculation of noise to get a feel for how the detector affects the total noise performance.

Some light is shed on detector selection, in the context of noise, in (*Table 2*). From the above, it would seem to make the most sense to select the APD, but the APD requires a high-voltage power supply to bias it, is very temperature sensitive, and generally costs more than a photodiode.

Therefore, in the example shown, the S1337 would seem to be the best choice. Furthermore, when considering the detector's signal-to-noise performance at various light levels, it can be seen that the photodiode's performance will be better than the APD's when the amplifier noise is no longer a factor (*Fig. 2*). This is because of the excess noise factor of the APD.

Unless the application demands the lowest NEP possible, the photodiode would be the best choice under these conditions.

Based on the equations given, it is evident that amplifier noise is strongly dependent on the bandwidth. Note that the results shown in Figure 2 were calculated at a bandwidth of 100 Hz. If the calculation was instead done at a 1-MHz bandwidth, the result would turn out to be much different (*Fig. 3*).

Because of the higher noise in wide-bandwidth applications, the APD is a good choice as it boosts the signal above the noise of the amplifier. Overall, choosing the correct detector is very application-specific. Here are some guidelines that should prove helpful:

Try to use the smallest active area possible. If the light source for the application is diffuse, this might not be practical but from the standpoint of noise, small diodes have lower capacitance and dark current. They also are less expensive.

In most applications, small capacitance will be more important than small dark current. Furthermore, the NEP in the catalogs does not take capacitance into account, therefore care should be exercised when comparing detectors using NEP.

In low-bandwidth applications, photodiodes operating in a photovoltaic mode will generally outperform device-operated photoconductivity. To reduce noise, the detector shunt resistance should be much greater than the feedback resistance.

To reduce the Johnson noise, use as large a feedback resistor as possible in the first amplifier stage.

In wide-frequency-bandwidth applications, PIN photodiodes operating in the photoconductive mode are preferred because of lower terminal capacitance. APDs, with their internal gain, also perform well in wide-band applications. They should be considered when the light source is weak and the amplifier noise is large.

EARL HERGERT earned a BA in Physics from Rutgers University and has been an Applications Engineer with Hamamatsu since 1989.

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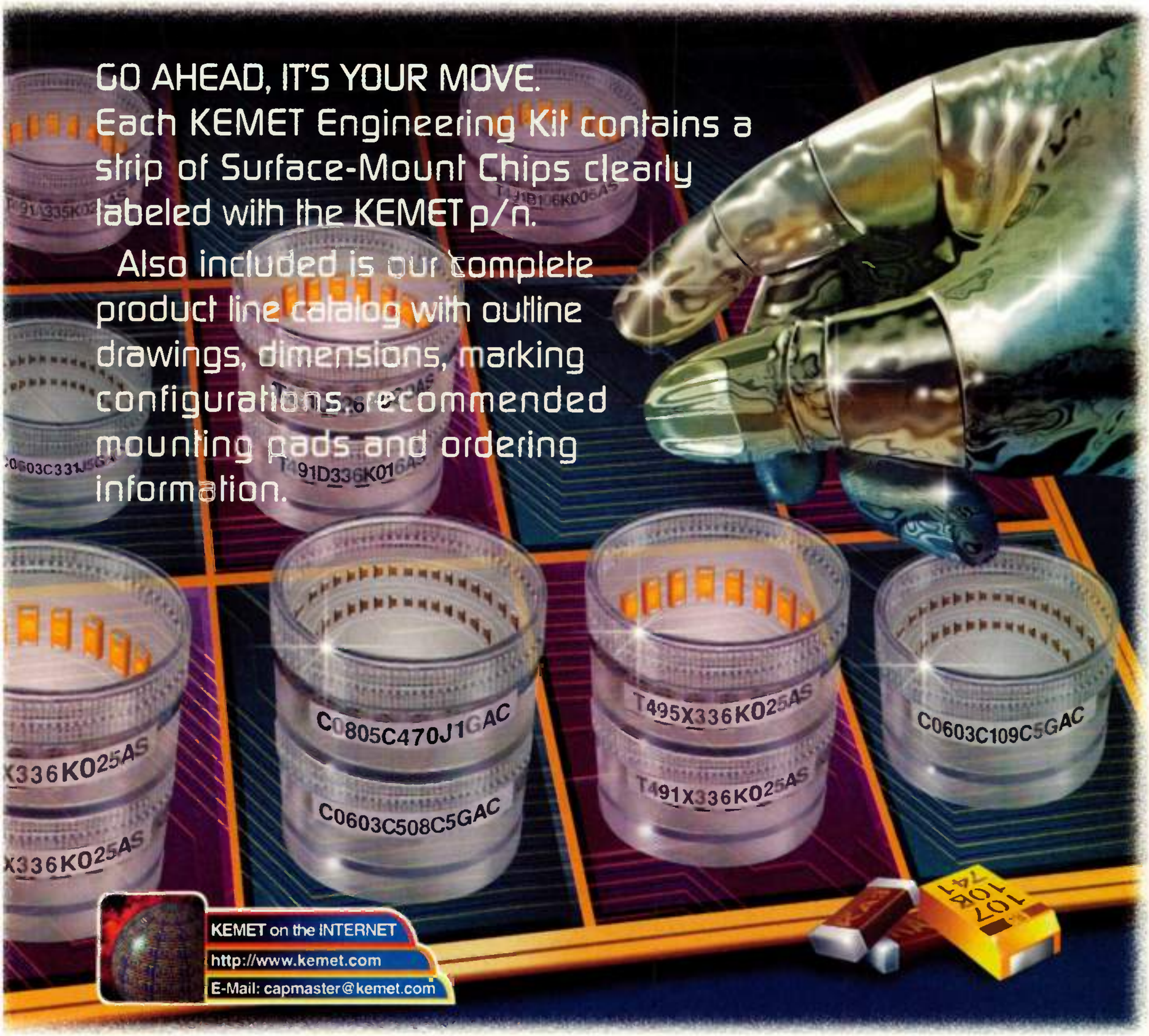

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Design Considerations For High-Performance Backplanes

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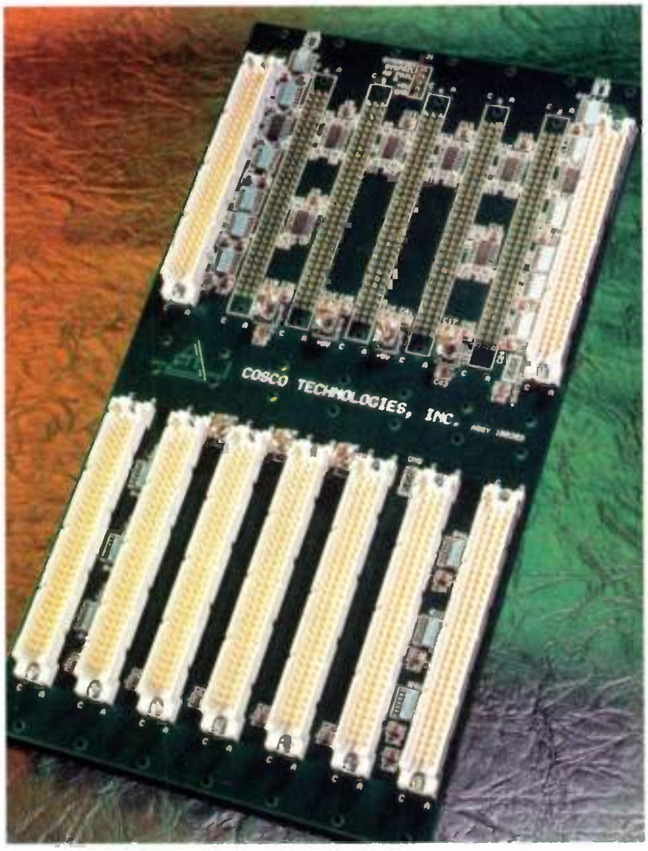
Although I/O Rates Keep Pushing The Envelope, Backplane Technology Is Staying Ahead Of The Game.

No matter how advanced the computer system, optimum performance still depends heavily on the ability of the backplane to accurately and reliably move large amounts of data from one system board to another as quickly as possible. Specifically, the backplane is a critical component in the performance equation since advances in active silicon devices are not directly transferable to the backplane. Fortunately, advances in pc-board fabrication such as fine-line traces and multilayer construction, combined with the advent of inexpensive surface-mount devices, have vastly improved backplane performance and reliability, while keeping costs down.

Despite the technological improvements, backplanes remain as somewhat of a bottleneck in high-end applications as I/O rates spiral upward. For example, typical Category 5 twisted-pair runs at 100 Mbits/s; wide and fast SCSI maintains 40 Mbits/s data streams; and home PCs costing less than $2000 are running at 166 MHz and using PCI interfaces capable of 256 Mbits/s data transfers. This kind of performance is driven by the market place. The entertainment market needs high-resolution, full-motion video. The information systems market for large enterprises demands reliable high-speed information retrieval and storage, while the communications market requires high-bandwidth switches and routers. When choosing a backplane to meet the requirements of these applications, three primary factors must be considered—signal integrity, power distribution, and reliability.

The backplane is responsible for maintaining signal integrity while accurately and quickly moving information, both digital and analog, from one system board to another (*Fig 1*). It also is responsible for maintaining accurate timing relationships between clock and data information as the signals propagate. Loss of signal integrity comes from three main sources—reflections, crosstalk, and propagation delays.

Reflections occur in backplanes when there is a change of impedance anywhere along the conductive path of the signal (*Fig. 2*). These changes in impedance can be caused by something as simple as a change in the thickness of a trace. The resulting reflections can either cause spurious negative effects such as false "1s" or "0s," or aid in the turn-on of drivers, as in the case of reflective-wave switching used in VMEbus or PCI systems. In any case, strict adherence to the specification attached to the architecture in question is essential if unwanted reflections

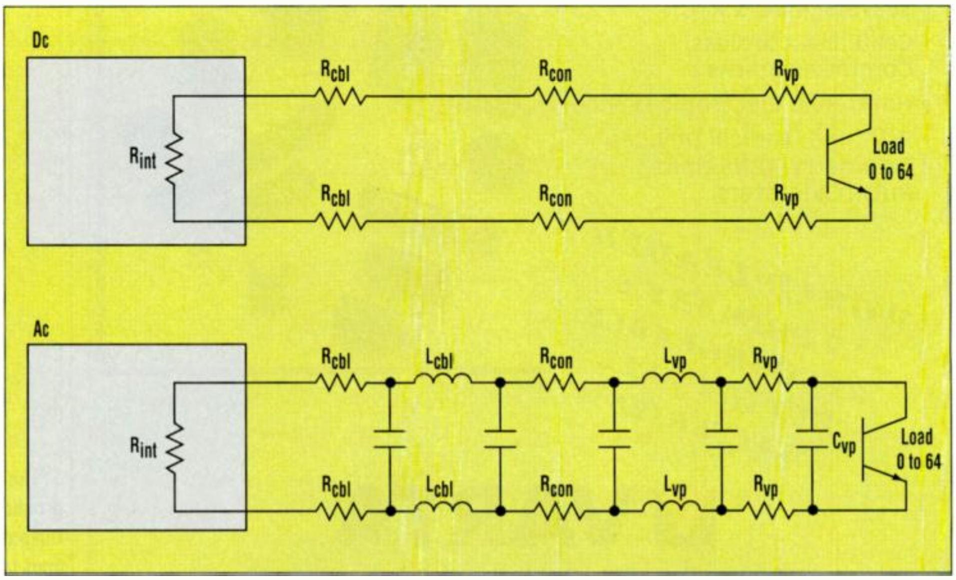


1. Responsible for maintaining signal integrity as information is passed from board to board, the backplane is facing increasing performance pressures as data rates target 80 Mbytes/s and beyond.

are to be avoided.

Crosstalk in backplanes can lead to false switching and intermittent operation and is mostly a capacitance coupling phenomenon (*Fig. 3*). As such, the crosstalk between signal lines can be approximated as being inversely proportional to the distance between the signal lines, and directly proportional to the distance between the signal lines and the ground plane.

One technique for reducing crosstalk is to use fine-line technology that increases the distance between signal lines while decreasing the distance between the signal line and reference plane. It has been shown that going from 12-mil lines to 5-mil lines can reduce crosstalk by up to 25%. Though once prohibitive, the cost of fine-line technology has decreased steadily over the last five years due to advances in etching technology combined with improved standards of cleanliness in the photo-etching and pc-board manufacturing process.



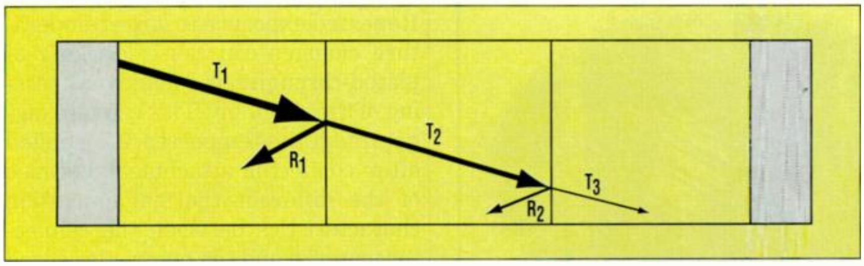
4. The equivalent circuit for the dc and ac modes of power distribution introduces the equivalent capacitance C_{VP} that is created by using plane pairs in the pc-board layout.

Propagation delays are not a problem if the timing relationships between clocks and signals are maintained. To maintain timing, special attention must be paid to trace lengths and the difference in propagation due to signal lines running on the surface and those surrounded by epoxy glass. Uncertainty in the propagation time of data with respect to the clock could cause a "1" to be interpreted as a "0" or vice versa.

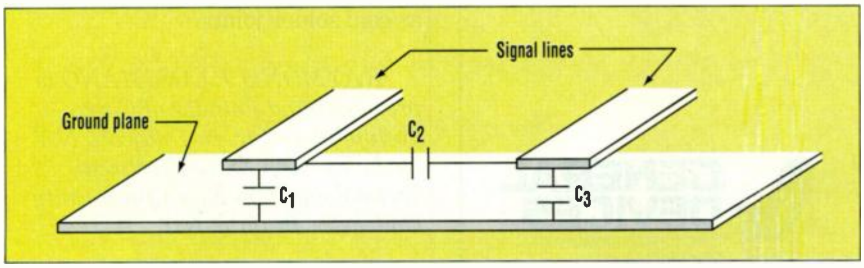
In most backplane systems, the power is supplied to the boards via the backplane. It is important that a low-resistance path is provided by the backplane to ensure that all boards in the system share the same reference with respect to the supply and ground. This reference also must be maintained under dynamic conditions. The equivalent circuits for the dc and ac modes of power distribution; depicted is a model of distributed capacitance (C_{vp}) that is created by using plane pairs in the pc-board lay-up (*Fig. 4*). This is an effective stabilizing capacitance because of the low-inductance path to the load. The ground and power pairs are used to create a distributed capacitance to control the change in current created by simultaneous switching of lines on a 64- and 128-bit buses (*Fig. 5*). Surface-mount decoupling capacitors and terminators should be used because of their low-inductance leads.

High reliability with respect to the backplane is critical as any failure that requires the backplane to be replaced normally means the whole system must be dismantled. The probability of a backplane failure could be viewed as the sum of the probability of the pc-board failure, plus the probability of connector-system failure, and the probability of process-induced failures.

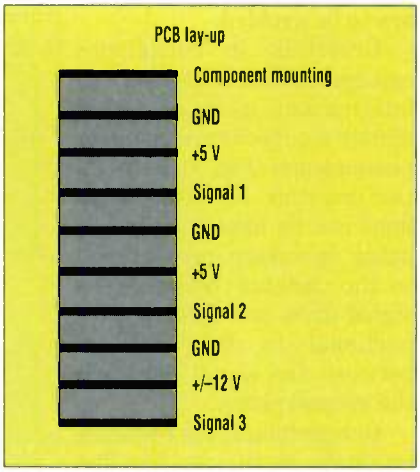
Pc-board failures can be minimized by maximizing the distance between conductors, minimizing the number of plated-through holes, minimizing the length of lines, avoiding sharp turns and square corners, and making sure that the line width spec-



2. Caused by changes in impedance anywhere along a signal's path, reflections can either cause negative spurious effects such as false highs and lows, or aid in the turn-on of drivers.



3. Crosstalk between signal lines is mostly a capacitance coupling problem and can be approximated as being inversely proportional to the distance between the signal lines, and directly proportional to the distance between the signal lines and ground.



5. The distributed capacitance created by using ground and power pairs controls the change in current caused by simultaneous switching of of lines on 64- or 128-bit buses.

ified in the design is matched with the process capability of the pc-board fabricator.

Connector reliability is a function of lubrication, wipe, normal force, plating integrity, and the number of contacts. Choosing a backplane system based on a two-piece connector system like VME or CompactPCI will go a long way toward optimizing wipe, normal force, and plating, because the epoxy glass is eliminated as a substrate for carrying one of the mating surfaces.

Processes used to assemble the backplane affect system reliability. Repeated exposure to large temperature changes can cause cracking of plated-through holes and overstressing of the assembly. This can be exaggerated if the temperature is applied after connector attachment because of the different thermal expansion characteristics between the connector material and the epoxy glass used in pc boards. Other common process-induced failures include contamination from fluxes and solders, as well as cold solder joints.

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Switches: The Linchpins Of A Good Design

PETER BROUILLETTE

C&K Components Inc., 57 Stanley Ave., Watertown, MA 02172-4802; (617) 926-6400; fax (617) 926-6846.

Given Proper Foresight, The Lowly Switch Can Connect Actual With Perceived Quality—A Key Factor For Design Success.

As design cycles shrink, many engineers are waiting until the last minute to select a switch suitable for their application. While this approach may work in some cases, it often leads to delays, cost overruns, and even design modifications. In addition, giving such short shrift to what is often the key interface between the user and the piece of equipment can not only compromise the actual quality of the item, but the perceived quality as well.

Seven key points to keep in mind to avoid program delays, and to improve customer satisfaction are:

Ergonomics should not be taken for granted. The look and feel of the switch reflects on the product in which it is used. Actuation force, travel, and switch tactility are all factors that affect this. Visual feedback is also important. Toggle and rocker switches display actuator status well, while rotary and push-button switches require marking or illumination.

Environmental compatibility is essential. All too often, unsealed switches are specified for applications that require a sealed solution. One of the most common sources of failure in switch products is foreign substances in the contact area.

In addition, the designer should ensure that the manufacturer has tested the switch under environmental conditions similar to those found in the end application. The best-in-class switch manufacturers will test their switches extensively to simulate real-world, long-term usage.

All pc-board-mounted switches are not equal. By acknowledging this, designers can avoid critical damage during soldering. Surface-mount switches must be manufactured from materials that can withstand temperatures as high as 260°C (high-temperature nylons and liquid-crystal polymers are recommended). Through-hole switches on a hybrid board also must be capable of withstanding the high temperatures. Testing for this tolerance is essential.

Electrical loads are critical considerations, if a switch is to perform to specification. Too often, in-rush currents are ignored with switches used to activate power supplies. Likewise, switches used for power applications are frequently misused in dry-circuit applications.

Factoring in the switch interface

The wide range of products most good manufacturers offer helps to avoid the lengthy lead times required for semi- to full-custom product runs.

up front helps ensure effective operation. Addressing this problem when the design is complete leads to switch actuation difficulties. The alignment of the switch in relation to the product's actuator must be studied. The actuator style must be compatible with the type of switch being used. Elastomer actuators on electrical equipment are growing in popularity due to their low cost and sealing performance, yet they may dampen the critical feel of the switch.

Modifications to standard products can extend lead times. Most switch manufacturers offer a catalog illustrating a wide range of standard products. The variety helps the designer avoid time-consuming custom modifications.

All switch suppliers are not equal. When the switch decision is delayed until the end of a product's development cycle, the switch supplier is often selected in haste. This quick decision can be as detrimental to a design project as selecting the wrong switch for the application.

Designers should know exactly who is manufacturing the switch, and where it is produced. Does the company build its own product or second-source it? If an off-shore switch manufacturer has been chosen, the designer must factor in the extended lead times that could be involved, as well as the difficulties that may be encountered when requesting application information and resolving technical issues. When selecting a manufacturer, a frame of reference for quality must be established. An ISO9001 registration is essential, while a Total Quality Management (TQM) operating philosophy should be a strong consideration.

While much of the talk in the industry dwells on the pressure designers are under to keep costs down, don't forget that switch suppliers are under the same pressures. Even the most reputable suppliers cannot waste valuable resources ensuring that each product they sell meets all application requirements. It is up to the designer to see what compromises were made, and which ones, if any can be tolerated. A key question the designer engineer should ask is, "Am I absolutely certain that there is a standard switch available from a reliable supplier, in the volumes I require, at the price I need, and that meets all of my requirements?" If not, then the switch application must be addressed at the start of the product design.

PETER BROUILLETTE graduated from The University of Lowell, Mass., in 1983. He joined Augat, Inc.-Alcoswitch in 1987 as a Senior Design Engineer. He joined C&K Components, Inc. in 1994, and is currently Director of Engineering.

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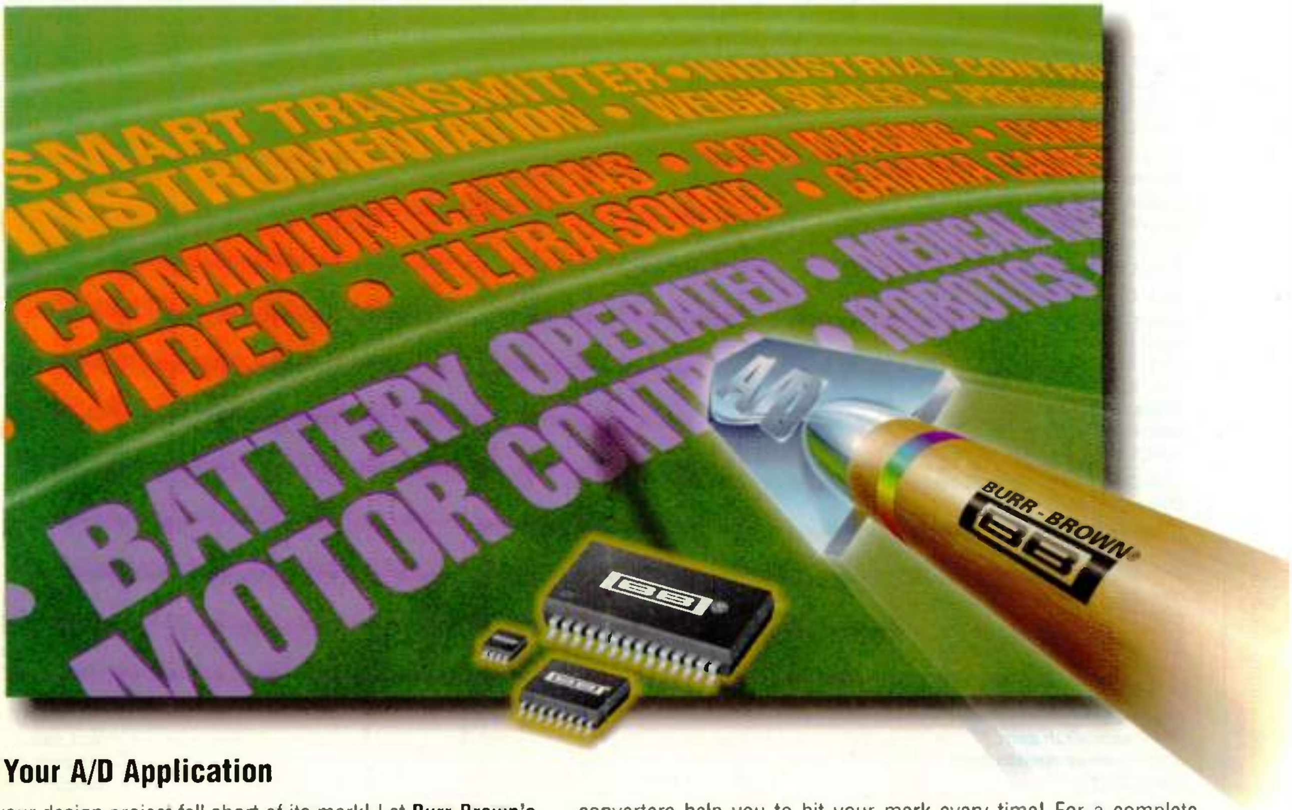

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ADS1210	±0.0015	±312mV to ±5V	24	20	26	$9.60	11284	80
ADS1212	±0.0015	±312mV to ±5V	22	16	1.4	$7.25	11360	81
ADS1214	±0.0015	±20mV to ±320mV	22	16	1.4	$7.25	11368	82

HIGH-SPEED A/D CONVERTERS *preliminary information

Product	Resolution (Bits)	Speed (MHz)	Power (mW)	SNR (dB)	DNL (LSB)	SFDR (dBFS)	Supply (V)	Price (1kpcs)	FAX*LINE* # 1-800-548-6133	Reader Service #
ADS800	12	40	390	64	±0.6	61	+5	$29.00	11286	83
ADS803	12	5	116	69	±0.3	82	+5	$9.55	11398	84
ADS824*	10	75	315	59	±0.5	70	+5	$8.50	11403	85
ADS930/931	8	30	66/63	46/48	±0.4	51/49	+3/+5	$3.37/$3.27	11349	86

GENERAL PURPOSE A/D CONVERTERS *no missing code

Product	Resolution (Bits)	INL (LSB)	DNL* (Bit)	Sample Rate (kHz)	Power (mW)	SINAD (dB)	THD (dB)	Price (1kpcs)	FAX*LINE* # 1-800-548-6133	Reader Service #
ADS7813	16	±2.0	16	40	35	87	-90	$20.00	11302	87
ADS7817	12	±1	12	200	2.3	71	-83	$5.18	11369	88
ADS7822	12	±0.75	12	75	0.54	71	-82	$4.64	11358	89
ADS7825	16	±2.0	16	40	50	86	-90	$28.46	11304	90

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Manufacturer	Power range	Lifespan	Positions available	Actuator styles	Ganging option	Mounting configurations	Packaging options	High-temp. plastics	Full -seal and/or gas-tight options
APEM Components, Inc. Wakefield, MA 01880-4444 Barry Mitchell (617) 246-1007 Fax (617) 245-4531 bmitchel@apem.com http://www.apem.com CIRCLE 169	Dry circuit to 100 mA @50 V dc	2000 cycles (min)@ full rated electrical load	One to 12	Piano, flush, extended, slide	Yes	Through-hole, SMD, vertical, right angle, piano, half pitch, tri state	Tape & reel, anti static, tubes, bulk, trays	Yes — reflow compatible, UL94V-O rated	Yes
Bourns, Inc. Riverside, CA 92507 Customer Service (909) 781-5079 Fax (909) 781-5378 http://www.bourns.com CIRCLE 170	100 mA, 50 V dc	2000 cycles	One to 12	Piano, raised, recessed	No	SMD, through hole, insertable	Tubes, tape & reel	Yes	No
C&K Components, Inc. Watertown, MA 02172-4802 Joan Donahue-Servey (617) 926-6400 Fax (617) 926-6846 jdonahue@ckcorp http://www.ckcorp.com CIRCLE 171	0.1 mA @ 5 V dc to 25 mA @25 V dc	2000 to 20,000 actuations	Two to 12 on DIPs, eight, 10, and 16 on DIP coded rotary	Flush, extended, piano	No	SMD with 1/2-pitch spacing; SMD with 0.1 spacing; through hole, right angle	Tube, tape & reel	Yes	Yes
CTS Corp., Electrocomponents Elkhart, IN 46514 Ron Sumrak (219) 296-0415 Fax (219) 293-1240 ctselect@mail.michiana.net http://www.ctscorp.com CIRCLE 172	100 mA or 50 V dc, non switching	1000 to 10,000 actuations	One to 12	Low profile, extended	No	SMD and through hole	Tube for all, tape & reel for SMD	Yes, for SMDs	Full seal with bottom epoxy and removable tape
EAO Switch Corp., Secme Div. Milford, CT 06460 G. Bracci (203) 877-4577 Fax (203) 877-3694 info@eaoswitch.com http://www.eaoswitch.com CIRCLE 173	50 mA @ 24 V dc	1000 to 2000 actuations	Two to 12	Standard, low profile, piano	No	Through hole and SMD	Tube, tape & reel	Yes, to 85°C operating, to 260°C for 1 min. infrared soldering	Sealed for soldering
EECO Switch Santa Ana, CA 92705 Sales Dept. (714) 835-6000 Fax (714) 953-3747 sales@eecoswitch.com http://www.eecoswitch.com CIRCLE 174	100 mA @ 5 V dc	20,000 actuations	Eight, 10, 16	Flush, extended	Yes	SMD and through hole	Tape & reel, tubes	Yes	Yes
E-Switch Brooklyn, MN 55428 Kris Akse (612) 504-3525 Fax (612) 531-8235 info@e-switch.com http://www.e-switch.com CIRCLE 175	Switching, 25 mA @ 24 V dc; carrying, 100 mA @ 50 V dc	2000 cycles	One to 12	Recessed, extended	No	SMD, through hole, IC machine insertable	ICtubes, tape & reel	Yes, UL94V-O high-temp plastic	Process-sealed and tape-sealed versions
Globtek Inc. Northvale, NJ 07647 Sales Dept. (201) 784-1000 Fax (201) 784-0111 globtekl@chelsea.ios.com http://gramercy.ios.com/~globtek CIRCLE 176	100 mA @5 V dc, 25 mA @25 V dc	2000 cycles	Two to 12	Top, side, right angle, J-lead, rotary	No	SMD, through hole	Tape & reel, bulk	No	Yes
Grayhill, Inc. LaGrange, IL 60525 Dan Neumann (708) 354-1040 Fax (708) 354-2820 dan_neumann@grayhill.com http://www.grayhill.com CIRCLE 177	1 mA @ 5 V dc up to 150 mA @ 30 V dc	5000 to 20,000	Two to 12	Slide, rocker (raised and recessed both), toggle	Yes	SMD, through hole, right angle, piano DIP	Tube, tape & reel	Yes	Yes
NKK Switches Scottsdale, AZ 85260 Bob Wanless (602) 991-0942 Fax (602) 998-1435 CIRCLE 178	100 mA @ 5 V dc	20,000 (min)	10 and 16	Screw-driver, shaft, dial, knob	Yes	SMD, through hole	Tape &reel	Yes	No
Shogyo International Corp. Plainview, NY 11803 Mark Rubin (516) 349-5200 Fax (516) 349-7744 CIRCLE 179	25 mA @24 V dc	2000 cycles	Up to 12	Normally recessed	No	Through hole	Tubed or tape & reel	PPS	No

Air-Cooling Electronic Systems: An Introduction

AL EISAIAN
NMB Technologies Inc., 9730 Independence Ave., Chatsworth, CA 91311; (818) 341-3355; fax (818) 341-8207.

As Component Density Spirals Upward, Careful Enclosure Design And Fan Placement Is Essential To Avoid System Failure.

With higher-performance systems coming in increasingly smaller boxes, the task of providing adequate cooling for critical components is more challenging than ever. Because of the increasing power densities, thermal-management issues must now be considered up front in the product development cycle to prevent complete system failure. Along with early planning, good thermal design within an enclosure requires the proper application of two simple concepts. First, the system must provide for adequate airflow around heat-generating components and heat-dissipating elements (such as heat sinks). Second, the system must allow for adequate space and power for the incorporation of the required cooling fans. The remaining design issues, from a thermal management standpoint, consist primarily of determining fan positioning and ducting, and selecting the proper number and type of fans.

Until recently, natural air convection provided adequate cooling for virtually all pc-board-based electronic systems. However, the upward spiral in generated heat is making the use of forced-air convection using fans and blowers a necessity (*Fig. 1*). In combination with heat sinks, they have proven to be highly effective for low- to mid-range systems. These fan-cooled electronic systems include everything from notebook PCs to set-top boxes aimed at home Internet access. Their presence in such high-volume, highly competitive markets forces designers to perform a delicate balancing act between cost and performance, placing greater burdens on the design of an active cooling system.

Other factors also must be taken into account. Since Jan. 1, 1996, the European Union has imposed a strict EMC (electromagnetic compatibility) directive on equipment makers selling their wares in Europe. The relatively airtight package required to shield from electromagnetic and radio frequencies makes it even tougher to cool the system. In addition, many markets are experiencing a lower tolerance for overall system noise, providing an even greater design task for small systems that require high-speed fans for adequate airflow.

1. As more components are packed into a single enclosure, the design engineer must factor in cooling earlier in the design cycle than ever before. Issues such as space, location, enclosure ducting, type, size, number of fans, and enclosure resistance must all be considered if overheating followed by system failure is to be avoided.

With an eye toward the mobile computers implementing fans this year, one thing is clear—the trend toward hotter systems is not going away. Designers must incorporate active thermal management elements, such as fans, into small enclosures, or at least be ready to do so very soon. But small portable computers represent just one of many different electronic systems that use fans. Single-fan systems still represent the most common implementation. However, some of the more mature products that employ forced-air cooling technology, like high-speed test equipment and desktop PCs or larger computers, use multiple fans. In fact, many fan-cooled systems incorporate subsystems, such as power supplies, that are actually cooled by fans.

There has been a recent resurgence in the use of variable-speed fans in mobile systems to maximize battery life. At idle, when the processor is not active, the fan slows down to its minimum RPM. At peak load, when cooling is needed, the fan speeds up.

Another important trend includes the use of airflow or temperature monitors to increase overall system reliability. Since the entire system

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depends on the ability of the cooling fan to deliver the required amount of air, if it fails, damage to the system could be considerable. Even if the fan never fails, blockage of the air-intake vents can significantly reduce airflow.

The first step in designing a forced-air cooling system requires an estimation of the necessary airflow. This calculation depends on two things: The heat generated within the enclosure, and the maximum temperature rise permitted inside. A very good estimate of power dissipation in a system is ac input power. Most battery powered systems typically include an ac input for a power source, so this estimate is simple to obtain.

It is essential, when calculating total power, that a designer allow for possible future changes or the addition of heat-generating subsystems. The power dissipation estimate also should be based on a worst-case power appraisal of a fully loaded system. In fact, when a compact product is not a priority, it is considered a very good practice to design the enclosure so that an additional fan can be added in series or parallel—just in case mistakes are made and additional cooling is required later on.

An estimate of required airflow required in a hypothetical enclosure can be obtained from:

$$Q = \frac{3.16W}{T_F}$$

or

$$Q = \frac{1.76W}{T_C}$$

where:

Q = Airflow required in cfm (ft^3/min.)

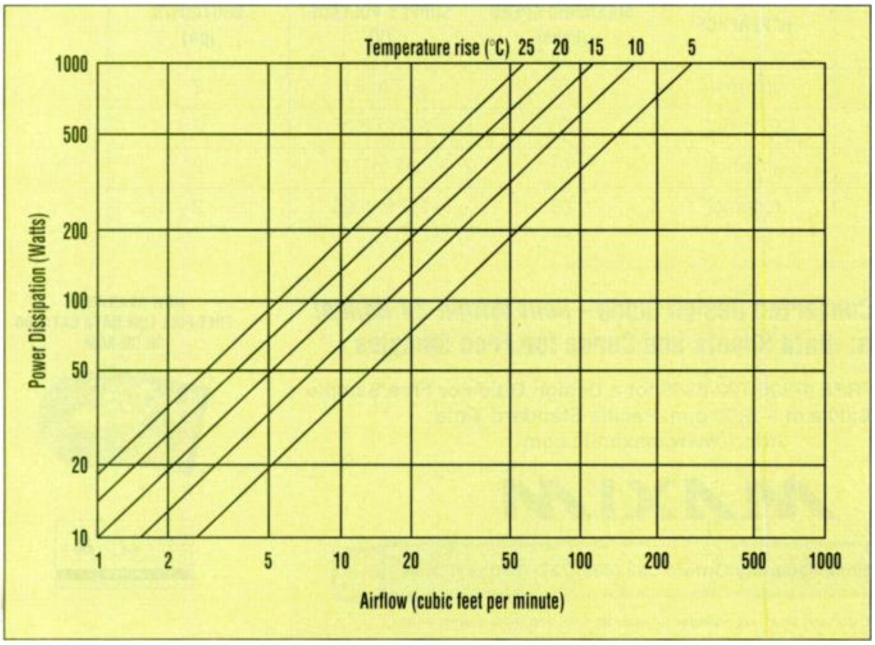
W = Heat dissipated in Watts

T_C = Temperature rise above inlet temp in °C

T_F=Temperature rise above inlet temp in °F

For example, 32 cfm (cubic feet per minute) of airflow is required for a system that dissipates 200W and allows a 20°F temperature rise. By keeping maximum temperature rise as a constant, and plotting the power dissipation and required airflow on the x and y axes, we can create a simple lookup table (*Fig. 2*).

In this graph, the vertical axis represents the heat to be removed in Watts, while the horizontal axis represents airflow in cfm. Both axes are logarithmic. The sloping lines define the temperature rise in degrees centigrade. To use the graph, find the sloping line that represents the permitted temperature rise, then find the point on the line that corresponds to the heat to be removed. The horizontal position of this point shows the airflow required to cool the enclosure.



2. By keeping maximum temperature rise as a constant, and plotting the power dissipation and required airflow on the x and y axes, we can create a simple lookup table to estimate the required airflow in a hypothetical enclosure. To use the graph, find the sloping line that represents the permitted temperature rise, then find the point on the line that corresponds to the heat to be removed. The horizontal position of this point shows the airflow required.

Measuring the actual airflow produced by a fan mounted in an enclosure is much more difficult and costly than simply estimating the airflow required. Obstructions in the airflow path cause static pressure within the enclosure, reducing the efficiency of the fan. The nonlinear relationship between airflow and static pressure is plotted for a typical axial cooling fan (*Fig. 3*).

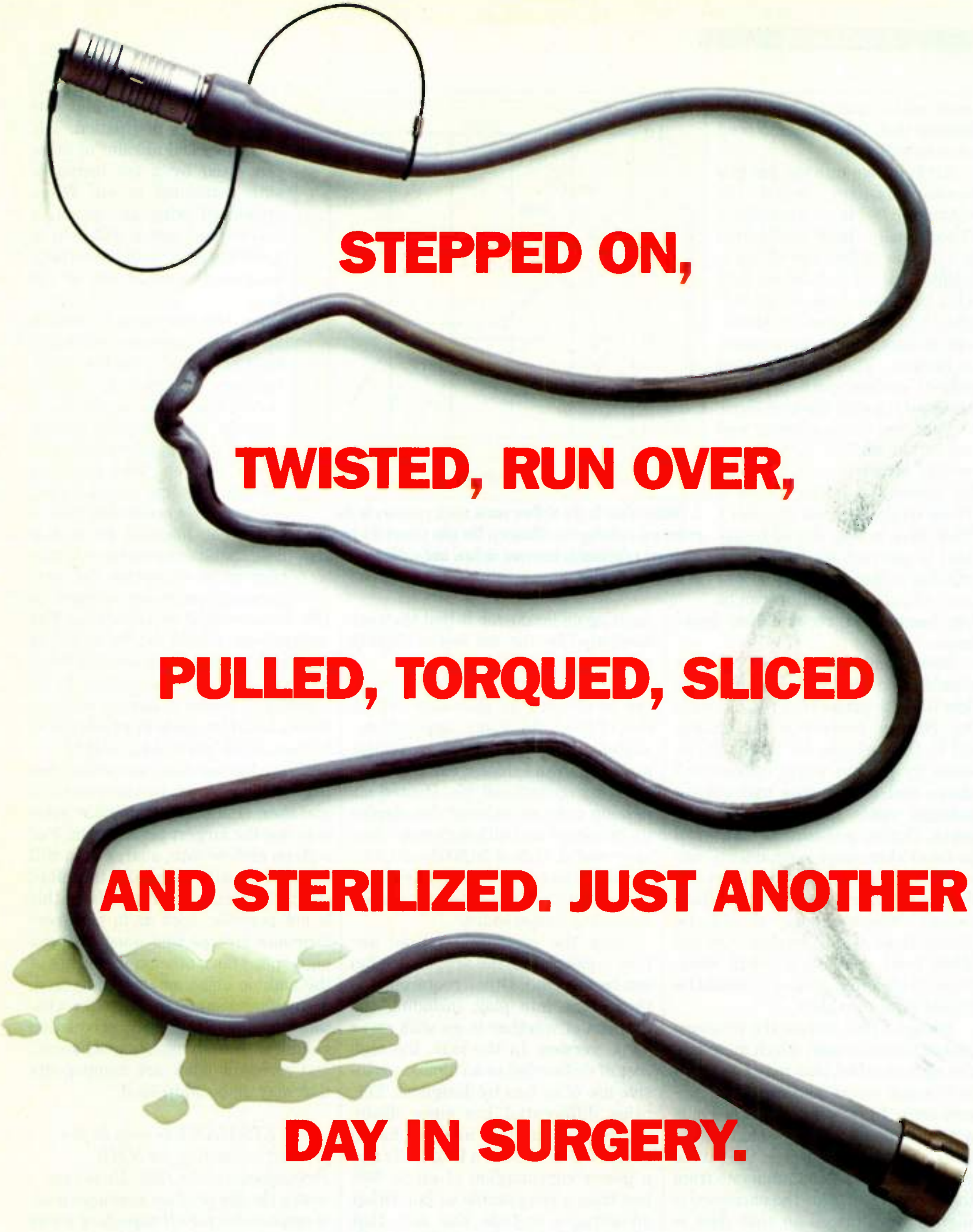
Obviously, to achieve maximum airflow, obstructions should be minimized. But in many cases, it may be necessary to include obstructions in the form of baffles so that the airflow can be directed through hot subassemblies or specific components that need cooling. In fact, in small systems, it may even be necessary to use the components themselves as baffles to direct airflow.

Determining actual airflow through a sample of the finished system is very accurate, yet extremely costly, time-consuming, and cumbersome. In practice, empirical methods are typically used to estimate airflow resistance. In fact, based on experience, the following guidelines may prove helpful in estimating system impedance.

- An empty enclosure usually reduces airflow by 5 to 20%.
- A densely packaged enclosure reduces airflow by 60% or more.
- Most electronic enclosures have a static pressure of between 0.05 and 0.15 inches of H_2O.

Assuming a dense package, the airflow requirement we calculated to be 32 cfm previously should, in fact, be capable of delivering at least 80 cfm in free air.

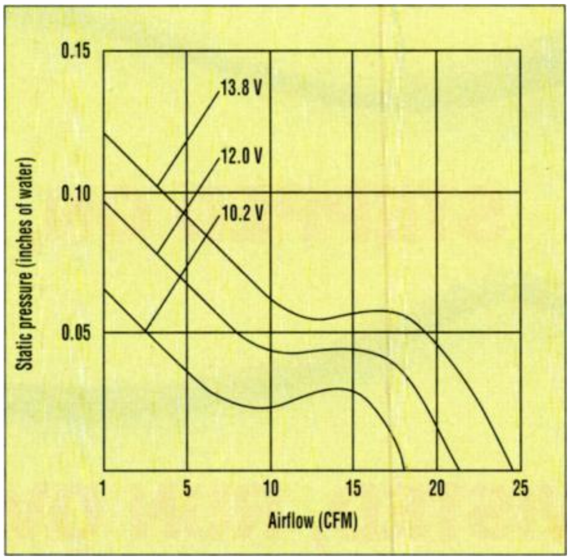
Designers have a choice of using a fan to exhaust air from, or blow air into, an enclosure. Given no other variables, the same volume of air should be required for exhaust or intake. But in real-world applica-


STEPPED ON,
TWISTED, RUN OVER,
PULLED, TORQUED, SLICED
AND STERILIZED. JUST ANOTHER
DAY IN SURGERY.

tions, each situation has other factors that must be factored into the equation.

Air is drawn into the fan in a laminar fashion, while air exhausted is turbulent. Theoretically, heat dissipation in a turbulent flow can be up to double that of a laminar flow with the same rate of air volume. But the region of turbulent airflow near a fan exhaust is limited. Therefore, a well defined airflow path must be designed through the enclosure.

Vents at the beginning and end of the airflow path should be 50% larger in area than the fan opening—possibly larger if it's an intake fan and includes a filter. Also, baffles should be utilized to prevent air from recirculating in the fan. Up to 90% or more of potential airflow can be lost because of recirculation problems.



3. Obstructions in the airflow cause static pressure in the enclosure, reducing fan efficiency. The plot shows the typical nonlinear relationship between airflow and static pressure for an axial cooling fan.

Subassemblies and components should be located so as to direct the flow of air to places that require cooling. Natural convection can greatly aid in this process for larger enclosures by placing warm components above cool components and placing exhaust vents higher than intake ports. During pc-board layout, keep in mind that large components can shield smaller components from the flow of air. Components with critical cooling requirements should be placed close to air intakes. On the other hand, components with resistance to high temperatures should be placed close to outlets.

Exhaust fans reduce the pressure within the enclosure, which increases the airborne dust that may be drawn in through vents and cracks in the enclosure. In fact, if dust exclusion is a requirement, fan placement at the intake is better. A filter at the intake removes airborne contaminants from the incoming air, plus the enclosure is slightly pressurized so that dust is not drawn into the enclosure.

The downside is that filters must be changed regularly to eliminate dust buildup. Accumulated dust can severely restrict airflow, causing elevated temperatures, and potential failure for the system. Another factor to take into account when implementing an intake fan is that the heat dissipated by the fan motor slightly warms the incoming air.

Fan reliability and longevity also can be affected by placement within the system. In many applications, implementing the fan as an intake, rather than an exhaust, can double or triple its operational life. Heated air passing over an exhaust fan strains its bearings, and although most fans are rated at a life of 50,000 hours, this can be reduced by as much as 20,000 hours for each 10°C increase in fan operating temperature.

Once the system's required airflow is calculated, the proper-size fan can be selected. Other requirements then come into play, including the decision of whether to go with an ac or dc version. In the past, the high cost of dc fans led to an almost exclusive use of ac fans by designers. This price differential has since disappeared. Factors that make dc fans a better choice include a longer life and a power consumption of up to 60% less than a comparable ac fan. Other advantages include the fact that speed is directly proportional to voltage, EMI/RFI levels are lower, and that they make it simpler to implement an airflow alarm system.

The widest selection of dc fans are available in 12- and 24-V versions. With fans, a higher voltage is generally preferred since higher current means lower current and less overall power dissipation. The frequency and amount of noise generated by a fan increases with rotational speed. When presented with an option, a lower-speed motor will help to minimize noise and, potentially, increase the useful life of the fan.

Once the enclosure's airflow and static pressure estimates have been made, the fan manufacturer can provide airflow curves that allow a fan to be selected with adequate cooling potential. Designers should use these curves with caution though. In some cases, it may not be clear whether the curves represent nominal or worst-case fan performance. A further word of caution, fan performance may vary as much as 10% from nominal specifications. Fan comparisons should not be based on performance in free air—which doesn't exist in a real enclosure. To be considered accurate, airflow comparisons should be made at pressures of between 0.05 and 0.15 in. of H_2O.

Noise has no effect on cooling, but may be important to the product's end user. One way to minimize noise is to use the largest possible fan. For a given airflow rate, a larger fan will run at a slower speed and therefore create less noise.In areas where this is not possible, such as in high-performance laptops that must use tiny high-speed fans, other components of the audible noise may be addressed. Many fan manufacturers offer custom fans given sufficient production volumes. Aerodynamic, mechanical, and resonant noise are components that may all be addressed.

AL EISAIAN has been in fan product marketing for NMB Technologies since 1989. He is currently the fan product manager and is responsible for all aspects of axial cooling fan sales. He holds a BS degree in electrical engineering from Oklahoma State University and an MBA from Pepperdine University.

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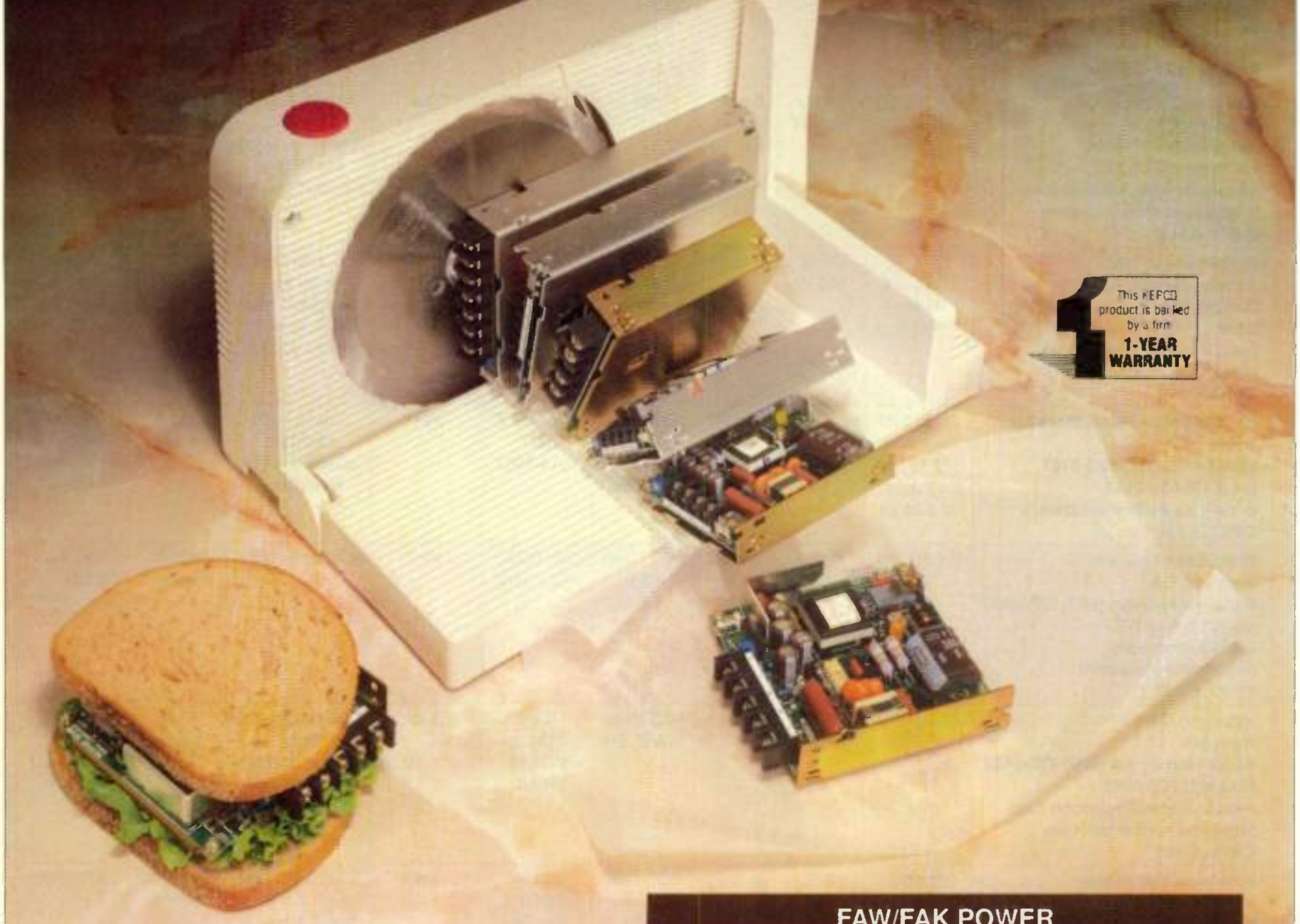

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15V	FAW, FAK	FAW, FAK	FAW, FAK	FAW	FAW
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Manufacturer	Available sizes	Power supplies	Number of slots	EMI/RFI protection	Standards compliance	Optional backplanes	Other main features	Delivery time	Other bus-based enclosures
AP Labs **San Diego, CA** **Steve Gills (619) 546-8626** **fax (619) 546-6278** **e-mail: steve@sd.aplabs.com** **http://www.sd.aplabs.com** **CIRCLE 191**	6U, 9U, 3U, rackmount, ATR	100 to 1200 W	3 to 42	MIL-STD-461C	EIA rack, ATR, MIL-STD-810E	Yes	Shock/vibration isolation, split backplanes, dual redundant power, thermal monitoring	2 to 10 weeks	PC/AT, Multibus, CompactPCI
Calmark Corp. **San Gabriel, CA** **R.L. Rosenthal (818) 287-0451** **fax (818) 287-7350** **CIRCLE 192**	3U up sub-racks	None	Unlimited	Whatever required	DIN 41494, IEC 297	No	Cooling fans, custom features	8 to 10 weeks ARO	None
Carlo Gavazzi Inc. **Brockton, MA** **Steve Curbesero (508) 588-6110** **fax (508) 588-0498** **e-mail: stevec@mupac.com** **CIRCLE 193**	2U to 15U	100 to 2000 W	1 to 21	FCC Class A with conductive metal-to-metal interfaces	UL 1950, CSA, EN 60950, VDE Class A	Yes	Redundant power supplies, hot-swap backplanes, system monitoring	6 to 8 weeks	VXI, Futurebus, CompactPCI, Sun, PC/AT, Multibus I and II
Dawn VME Products **Fremont, CA** **Sales (510) 657-4444** **fax (510) 657-3274** **e-mail: dawnsales@aol.com** **http://www.dawnvme.com** **CIRCLE 194**	3U, 6U, 9U	150 to 1000 W	3 to 21	N/A		Yes	Voltage, fan-fail, and over-temperature monitoring; attitude/tilt switch	3 days to 6 weeks	CompactPCI
DY4 Systems Inc. **Kanata, Ontario, Canada** **Duncan Young (613) 599-9199** **fax (613) 599-7777** **e-mail: dyoung@dy4.com** **http://www.dy4.com** **CIRCLE 195**	1/2 ATR short, 3/4 ATR short, 1 ATR long	78 to 250 W	5 to 15	MIL-STD-461C	ARINC 404A, IEEE 1101.2, ANSI/VITA 1994	No	Conductive cooling, configured front panel, fans, dc or ac supplies	6 to 26 weeks	None
Electro Space Fabricators Inc. **Topton, PA** **Lisa Keller (610) 682-7181** **fax (610) 682-2133** **e-mail: sales@esfinc.com** **CIRCLE 196**	3U to 12U high and 160 to 140 mm deep, or custom	N/A	1 to 27	Shielding per custom requests	ANSI IEEE STD. 1014-1987	Yes	Custom and standard enclosures and front panels	4 to 6 weeks	VXI, Multibus II
Elma Electronic Inc. **Fremont, CA** **Sandhya Kedlaya (510) 656-3400** **fax (510) 656-3783** **sales@elma.com** **http://www.elma.com** **CIRCLE 197**	3U, 6U, 9U, 12U	100 W	3 to 21	FCC Class A & B, VDE-B, CE, MIL-STD-461C	UL, CSA, FCC, TUV	Yes	Auto daisy chain	2 to 4 weeks	VXI, PC, Multibus II, CompactPCI
Hybricon Corp. **Ayer, MA** **Karen Harrington (508) 772-5422** **fax (508) 772-2963** **e-mail: Karen@hybricon.com** **http://www.hybricon.com** **CIRCLE 198**	3U to 13U	80 to 1350 W	2 to 21	FCC Class A & B, EN	IEEE 1101.1, 1101.10, 1101.11	No	Optimized air flow, accommodations for peripheral devices, easy access	6 to 8 weeks ARO	VME64x, CompactPCI, Futurebus, custom
Interlogic Industries **Melville, NY** **Bert Freifeld (516) 420-8111** **fax (516) 420-8007** **e-mail: infoview@ix.netcom.com** **http://www.infoview.com** **CIRCLE 199**	3U, 6U	120, 200, 400, 600, 800 W	4 to 21	FCC 2780 and VDE 0871	Within ISO9002 and DIN 41494 framework	Yes	VSB, VMX bus, extender and transition cards	Stock to 2 weeks	AT, ATX
Knurr USA Inc. **Simi Valley, CA** **Curtis Schatz (805) 526-7733** **fax (805) 584-8376** **CIRCLE 200**	3U, 5U, 6U, 8U	400, 600 W	12 to 20	Full	EMC MIL-810E, VG, DIN	No	EMC, full grounding, injector/ejector, board locating pins	2 to 6 weeks	Table top
Powerbox USA **Broomfield, CO** **Peter Wagner (303) 439-7220** **fax (303) 439-7211** **peter.wagner@powerbox.sc** **CIRCLE 201**	3U, 6U	30 to 600 W	1 to full rack	FCC/VDE Class A or B	Various safety, EMI/RFI, packaging	Yes	Dc inputs, hot swap, redundant	1 to 12	CompactPCI

MANUFACTURERS OF VMEbus ENCLOSURES

Manufacturer	Available sizes	Power supplies	Number of slots	EMI/RFI protection	Standards compliance	Optional backplanes	Other main features	Delivery time	Other bus-based enclosures
Rose and Bopla Enclosures **Frederick, MD** **George Miller (301) 696-9800** **fax (301) 696-9494** **CIRCLE 202**	100 by 160 to 200 by 220 mm; 9 to 84 TE	N/A	1 to 28	EMI/RFI spray and gaskets	IP, NEMA, DIN, UL	Yes	Portable and rackmount, cassettes, flexible sizing	Stock or 6 to 8 weeks	Eurocard
Schroff Inc. **Warwick, RI** **Jennifer D'Amico (800) 451-8755** **fax (401) 738-7988** **CIRCLE 203**	2U to 12U	160 to 750 W	1 to 21	CE compliance	DIN, IEEE 1101.10, VITA	Yes	Full range of accessories, cases for aesthetics	6 to 8 weeks	CompactPCI, VME64x, VXI, custom
Tracewell Systems Inc. **Westerville, OH** **Fred Meyer (614) 846-6175** **fax (614) 848-4525** **CIRCLE 204**	3U, 6U, 9U; 160 to 400 mm; or custom	65 to 1200 W or custom	1 to 21	Any requirement including tempest	DIN, EIA, VME Rev. C.1, VXI 1.4	Standard or sold separately	Automatic BG/IACK SMT backplane, power plane, power/air monitoring	4 to 6 weeks	VME64x, VXI, CompactPCI, PC/AT
VERO Electronics Inc. **Wallingford, CT** **John Bratton (800) 642-VERO** **fax (203) 949-1101** **e-mail: vero@vero-usa.com** **http://www.vero-usa.com** **CIRCLE 205**	1U, 17 in., 12 in., and up	50 to 1500 W	2 to 21	FCC Class B	UL, FCC, DIN/IEEE, MIL	Yes	Cooling, strengthening, custom	1 to 8 weeks	CompactPCI, VXI, VME64, VME64x

SIEMENS

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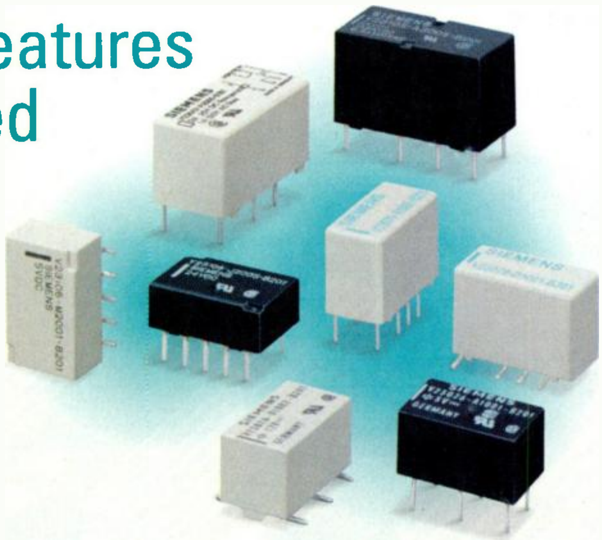

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Contact Rating	30W 60VA	30W 62.5VA	60W 62.5VA	60W 125VA	50-150W 250VA
Nominal Coil Power	30-150mW	100-200mW	70-140mW	150-300mW	75-360mW
Terminals	Pin or SMD	Pin or SMD	Pin or SMD	Pin	Pin
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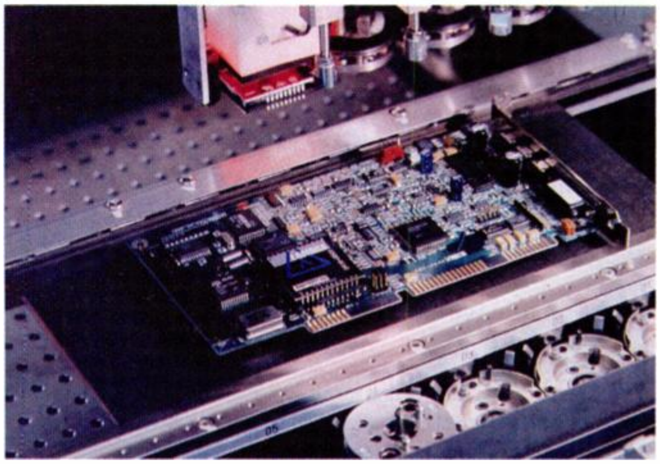
Surface-Mount DC-DC Converters Come Of Age

MICHAEL WAGNER

Lambda Electronics Inc., 515 Broad Hollow Rd., Melville, NY 11747; (516) 694-4200; fax: (516) 293-0519.

Improved Thermal Management Has Produced Lightweight Power Converters In A Wide Range Of Power Ratings.

By eliminating manual assembly steps, automated surface-mount assembly of pc boards has proved its value in reducing manufacturing costs and improving reliability. But manufacturers' aspirations for total surface-mount assembly have been frustrated by limited access to dc-dc converters that are small and lightweight enough for the typical pick-and-place machine. As a result, converters must be added manually.



1. Using a special pc-board material, surface-mount dc-dc converters can now be manufactured in a range of power ratings well above the 10-W limit that excessive weight and bulk previously imposed on such devices. As a result, manufacturers that have invested heavily in SMT can prepare to reap maximum benefit from their investment.

This problem is of particular concern to high-volume telecom and computer manufacturers who are not seeing optimal return on their investment in surface-mount technology (SMT). Help is at hand, however, thanks to recent developments in thermal management technology that allow for a smaller, lighter, power package in a wider range of power outputs.

To date, the chief obstacle to surface-mounting converters has been excessive weight. Thermal encapsulation and other established techniques for dissipating heat from power converters have not allowed these components to be made light enough to be handled by SMT pick-and-place equipment, especially at power ratings of 10 W or higher. The end effector of the typical pick-and-place machine has a maximum capacity of between 50 g and 70 g. This capacity has caused a situation to develop whereby manufacturers that have invested significant sums in SMT automation equipment are still taking the extra steps needed to manually mount and solder through-hole power converters on the card.

These manual steps typically take place after solder masking, auto placement of SMT components, wave soldering, and inspection. The through-hole converter is placed on the board, followed by another automated or manual solder operation and another inspection. The next step involves a manual lead clip process to ensure proper height of the protruding through-hole pin, so that the back side of the pc board has no icicles. If the lead is cut improperly, damage to the solder joint may occur, adversely affecting reliability. Manufacturer frustration is further fueled by thermal issues stemming from the general trend toward higher operating currents at lower voltages. Heat dissipation from the converter must continue to be managed so that other on-board components are unaffected.

Even at power ratings below 10 W, the lack of a fundamental technological solution for designing surface-mountable converters has proven problematic. In a typical scenario, a manufacturer of LAN equipment might create a tiered product line with similar functionality, but different power requirements. The low-end model for a small office will share many design features with the unit intended for a major company, but the high-capacity model requires on-board dc-dc converters with a higher power rating or more cards to support a larger system. If surface-mountable converters are available only for the low-end power requirements, it becomes impractical to scale up the same distributed-power design and manufacturing process—unless through-hole units continue to be relied upon for the entire product line.

In the absence of a standard surface-mountable dc-dc solution, the extra design time and expense needed to create fully customized surface-mountable converters for specific applications also has discouraged manufacturers interested in total SMT assembly. Full-custom converters can take three to six months to develop, and require a sizable investment. As a result, despite their disadvantages, through-hole converters have remained the default choice of electronics designers.

Spurring the need to develop surface-mount solutions is the fact that voltage requirements in microelectronics devices are expected to become more diverse and complex. While the most popular output for on-board power is 5 V, 3.3 V is often needed for microprocessor chips and CMOS circuits. The industry trend is moving toward a voltage range of 1.2 V to 3.9 V. Outputs of 12 V are used for analog circuitry such as gate arrays and operational amplifiers and comparators, while many designs call for 15-V outputs to be post-regulated to 12 V for noise reduction.

In addition, certain applications, such as RS-232 communication and dual-rail operational amplifiers, call for 3- or 5-V outputs to be combined on the same card with ±12- or 15-V outputs for analog applications. The existence of an overall solution for creating standard surface-mountable power converters will greatly facilitate the rapid development of SMT converters to meet these evolving requirements.

The excessive weight and bulk inherent to the typical dc-dc converter is a direct result of thermal management efforts. The thermal design of any power converter must effectively and reliably convect heat away from both the converter and the pc board on which it is mounted. The heat may be internally generated during operation, or may come from wave soldering of the converter to the card. The high heat generated during the soldering process must be dissipated rapidly to prevent melting of the solder bonds inside the converter.

Means used to dissipate this heat include the use of a two-step potting process to apply a silicon-based, thermally conductive potting material. A vacuum step is employed to eliminate any air bubbles from the encapsulation. While the extra weight of the potting material can be handled in a manual-assembly process, it is impractical for components intended for automated surface-mounting.

Another strategy that designers rely upon to reduce heat is increasing the surface area of the power module. Making converters larger, however, tends to make them significantly heavier as well as bulkier, so that it becomes even more difficult for automated pick-and-place equipment to handle them. Also, the extra volume of the component means that it occupies extra board space, which is a critical concern for end users who are constantly trying to minimize card size in space-constrained applications.

Recent advances in thermal management for on-board power converters, however, have provided a feasible method of achieving the reductions in component weight needed for pick-and-place operations at power ratings of 10 W and above. As a result, standard surface-mountable converters can now be created to meet the needs of a much wider range of end-use equipment and applications (*see Fig. 1*).

This technique involves the use of a special pc-board material with 10 times the thermal transfer capability of FR-4. The converter is inverted and mounted to the card using a lead-frame attach, so that its heat spreader substrate faces upward, dissipating thermal energy away from the converter and the card. The lead-frame attach incorporates 64 or 88 pins (depending on the power rating of the converter), which further conduct heat off to the sides of the converter or through traces on the card.

2. The result of this new design for surface-mount dc-dc converters is highly effective thermal dissipation, allowing only a minimal temperature increase between the converter and the card. Furthermore, this rise is consistent, as there are no significant hot spots caused by the convection scheme.

The result of this new design, which has been developed in consultation with leading OEMs in the telecommunications and computer fields, is highly effective thermal dissipation, allowing only minimal temperature rise between the converter and the card. Furthermore, this temperature increase is consistent, as there are no significant hot spots caused by the convection scheme (*see Fig. 2*). Package density is significantly increased, and thermal potting is eliminated. The savings in weight and size achieved by the new design allow on-board converters of 10 W or higher to be lightweight and small enough for existing SMT vacuum-end affectors to pick up.

By permutating this design into a variety of standard input and output voltages, with single, dual, and triple output options, the advantages of surface-mountable power converters can be made readily available for virtually any on-board dc-dc scenario.

DESIGN BENEFITS

By eliminating the need for encapsulation, and making possible a higher packaging density and thus, smaller component size, the new design allows converters with power ratings of 10 W and above to meet the weight threshold for SMT. The new surface-mount converter design allows footprints as small as 1.96 $in.^2$ for 5- and 10-W converters, 3.24 $in.^2$ for 20-W converters, and 6.25 $in.^2$ for 30-W

models. As with all on-board components, a low vertical profile is essential for dc-dc converters to allow the maximum number of cards on a rack. The high packaging density of the new converter design translates into very low profiles of between 0.35 in. and 0.4 in.

None of the design changes aimed at improving thermal characteristics to surface mount the dc-dc converters accomplish this goal at the expense of electrical performance. Electrical parameters for the new design are either comparable or superior to previous-generation through-hole devices. All applicable Belcore and ETSI specifications are met, including input transients, input-to-output isolation, and radiated and conducted EMI.

Fast start-up time is a key performance characteristic of on-board power converters, ensuring on-board circuitry is intelligent during hot-plug applications, which are common in telephone switching equipment. With a 10-ms start-up capability, the new surface-mountable converters establish a new performance benchmark for standard products.

After power is applied to the card, the converter establishes its output voltage within a maximum of 10 ms, so that the card becomes intelligent extremely quickly after being plugged into a live voltage source.

Manufacturers of product lines containing several models of equipment with tiered power ratings can now consider surface-mount converters for more than just the low-power models.

With heat dissipation reduced as a design obstacle, it is possible to engineer surface-mountable converters at dozens of standard input and output voltages. By selecting from a wide range of standard converters that match typical ranges of specification requirements, OEM designers can minimize customizing and, where practical, rely on relatively little modification of these designs. Furthermore, surface-mountable dc-dc converters can be made available with little lead time, so that manufacturers can derive the benefits of total SMT assembly without risking delays in product development or increasing time-to-market. The increased applicability, scalability, and availability of surface-mountable dc-dc converters will, for the first time, make total SMT assembly in distributed-power architectures a compelling option for many designers.

MICHAEL WAGNER has a BSEE from Polytechnic University. He is market segment manager (telecommunications) for Lambda Electronics Inc. in Melville, New York.

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Board-Level Connectors For High-Speed Systems

SCOTT MICKIEVICZ
AMP Inc., MS 39-01, P.O. Box 3608, Harrisburg, PA 17105-3608; (717) 592-6439.

Long Considered A Mechanical Problem, These Connectors Are Now At The Forefront Of Design.

With new generations of logic devices offering twice the speed of the generation before it, designers are being forced to carefully evaluate the entire signal path of these high-speed systems to avoid problems. An often-underestimated weak link is the connector, which frequently has to deal with hundreds of tightly packed signal lines that can be switching in the gigahertz range. As a result, the electrical characteristics of the connector, and its effect on signal integrity, have come under close scrutiny.

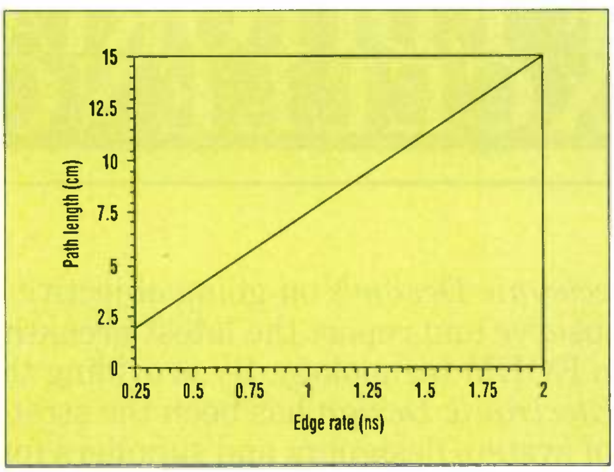
Factors to be considered include impedance mismatches, trace routing, skew, and parasitics due to the affects of inductance and capacitance, and the pc-board material itself. Their effects have led to the emergence of two popular connector topologies—open-pin field and controlled impedance—with their respective advantages of high density and high performance. Depending on the particular application, a combination of the two or a single connector, appropriately partitioned, may be the optimum solution.

The first priority is to determine whether the system falls under the rather broad umbrella of high speed. The term high speed itself can be an ambiguous term, used by different people to mean different things. From our perspective, when discussing high speed we are referring to a system in which transmission-line effects must be accounted for. Edge rate is the key here. When the round trip of the signal is longer than the edge rate, the line must be analyzed as a transmission line. In practical terms, the maximum permissible signal path is a generous 15 cm at a 2-ns edge rate, but only 2 cm when edge rates decrease to 250 ps (*Fig. 1*). The point at which this critical length is exceeded is the point at which transmission-line rules start to apply.

TYPICAL TWO-PIECE BACKPLANE CONNECTOR OPTIONS

Type	Connector	Spacing (row by column)	Number of rows	Number of pins
Controlled impedance	SL 100	0.100 by 0.100 in.	4	40 signal pins/in.
	HS3	2 by 2.5 mm	0	100 signal pins/in.
Open-pin field	2-mm HM	2 by 2 mm	5,5 + 2* 8,8 + 2*	62 pins/in. 100 pins/in.
	2-mm HM	1.5 by 2mm	12	150 pins/in.

The "+2" configuration includes a shield as the outer rows.



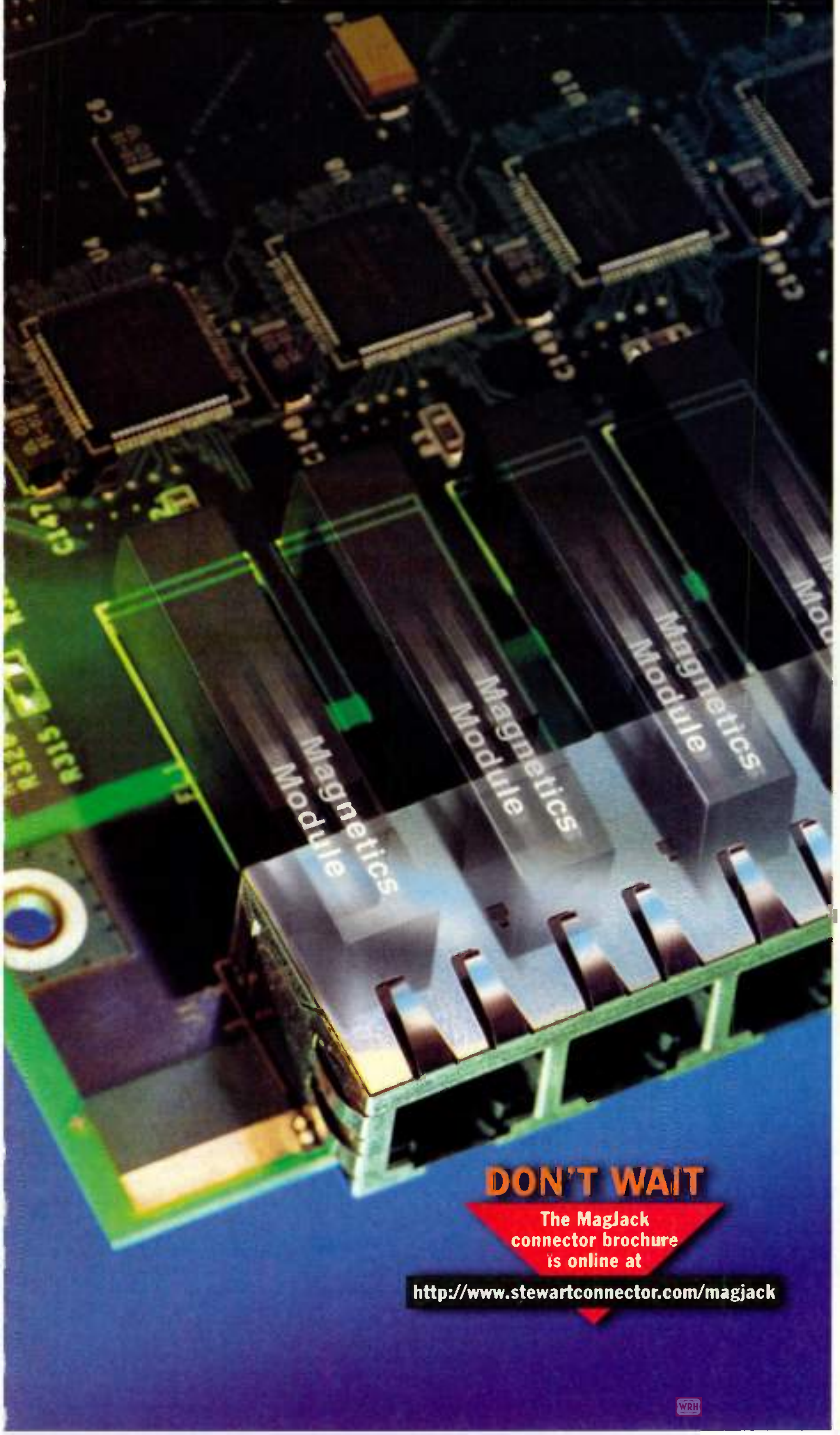
1. With data rates running into the hundreds of megabytes/s, high-speed signal pathways are behaving increasingly like transmission lines, and must be analyzed accordingly. When the combination of edge rate and path length falls into the area above the diagonal line, transmission-line design rules apply.

Once the expected data rate has been defined, the variety of available two-piece backplane connectors gives designers an array of options. Two popular choices are open-pin-field connectors and controlled-impedance connectors. The latter use ground planes between columns or rows of pins to achieve stripline or microstrip configurations, similar to those used in pc boards. Just like a pc-board design, a key system design technique is controlling the impedance to reduce reflections, ringing, and other unwanted effects of impedance mismatches.

Each connector type has cer-

Clean up your signal. Free up your board.

Introducing the Stewart MagJack™: the network magnetics you can plug into.



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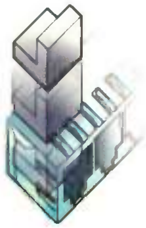
When it comes to signal integrity, it's what's inside that counts. That's why we took the magnetics off the board and integrated them directly into the MagJack body, to provide better EMC. Our integrated design offers enhanced common-mode performance over discrete magnetic components at frequencies up to 200 MHz and reduces near-field noise coupling. Less common-mode current improves signal integrity for clearer, more reliable transmissions and enhanced network performance. And because MagJack minimizes exposed PC board traces, it reduces the possibility of performance-robbing EMI.



MagJack integrates the isolation transformer and common mode filter into the shielded housing, minimizing signal degradation and conserving valuable board space.

Save Your Space.

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We challenged our people to make the best connectors in the world. They did. To find out more about Stewart's MagJack, call 717-235-7512.

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Insilco Technologies Group

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Phone: 717-235-7512 • Fax: 717-235-7954

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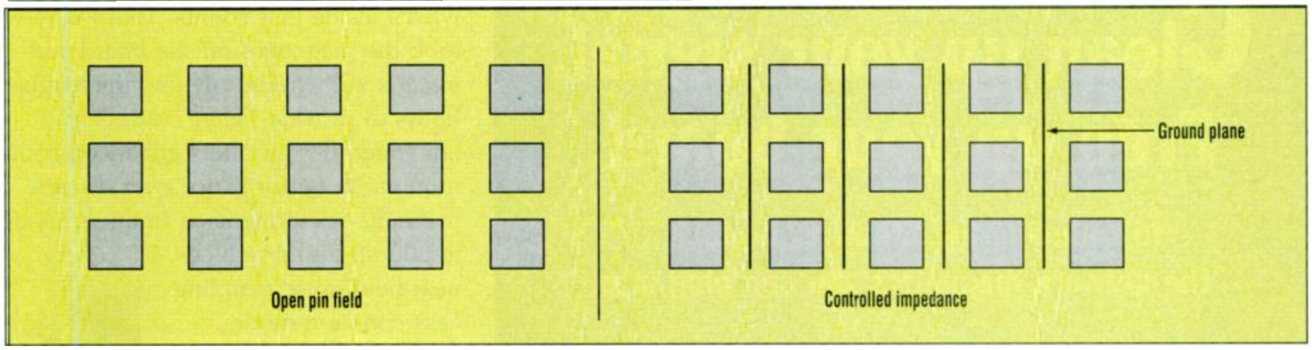
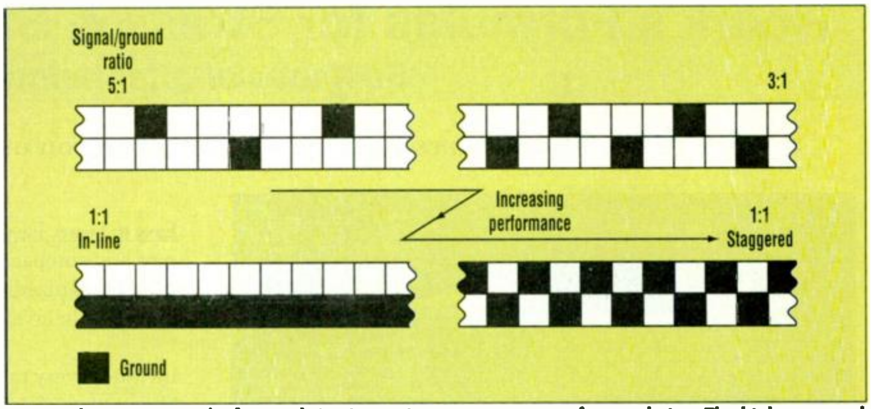


2. Controlled-impedance connectors use ground planes between each row of signal pins to provide a consistent impedance and a constant number of signal pins per inch. This design gives such connectors the edge in overall performance.

tain advantages in terms of speed, signal density, signal integrity, and cost. A brief comparison of some common AMP two-piece connectors used in high-speed backplane applications is given (*see the Table*). The basic difference in configurations between open-pin-field and controlled-impedanceconnectors is depicted (*Fig. 2*).

Connectors using open-pin fields have long been the choice for board-to-board applications. As both the signal-to-ground ratio and the arrangement of signal and ground pins affect pulse fidelity, high-speed pulse propagation in these connectors can be improved by assigning more pins to ground to reduce the circuit impedance. The best arrangement is a staggered signal-ground-signal-ground arrangement to prevent crosstalk between lines (*Fig. 3*). However, as signal rise times become faster, more pins must be allocated to ground. At rise times over 10 ns, a 5:1 ratio usually provides adequate performance. At 3 to 10 ns, the recommended ratio becomes 3:1. At even higher speeds, a 1:1 ratio is advisable.

The obvious disadvantage is that up to half the connector resources are dedicated to ground. This is contrary to the desire for high-packaging densities since half the pins are "wasted" to achieve signal-transmission quality. The solution is to offer a built-in



3. Signal integrity in a high-speed circuit requires generous use of ground pins. The highest-speed circuits require a 1:1 staggered relationship of signal to ground pins.

ground plane to control impedance and reduce crosstalk. This is the key design advantage of controlled-impedance connectors and it provides greater efficiency in terms of signal pin use as all signal pins are available for signal-carrying purposes.

As with any component, connector selection must be weighed against application requirements. Open-pin-field connectors offer the highest pin density, but the density of usable signal pins will vary with the signal-to-ground ratio. But by carefully selecting the connector, partitioning signals, and assigning grounds prudently, these connectors will meet a wide range of needs well into the picosecond range. Controlled-impedance connectors extend performance even further, making them the choice for high-end applications pushing the envelope of performance and density. Plus, they have a constant signal-pin density since pins don't have to be assigned to ground.

PACKAGING & DENSITY

The drive toward higher densities in packaging includes connectors, of course. But because a connector also is a mechanical device, there are some practical limits on size. Backplane connectors typically have centerline spacings of 2.0 mm or 2.5 mm between pins. A common measure of a connector's capability is the number of pins it provides per linear inch, and more importantly, the number of signal pins. The number of signals per linear inch directly affects the practical size of boards requiring a large number of I/Os. While traditional connectors offer four rows of pins, newer designs are now offering eight or ten to provide a greater signal density per linear inch.

While conventional wisdom may say that a 2.0-mm connector is better than a 2.5-mm connector when it comes to packaging density, conventional wisdom isn't always right. The prudent designer must consider a number of factors before making a connector decision. Since conventional wisdom would favor the 2-mm connectors, let's look at the case for the 2.5-mm connectors.

Trace routing—A 2.5-mm pin spacing makes it easier to route traces between the pins. Easier trace routing can result in fewer board layers, fewer problems in resolving problems with skew from uneven path lengths. It also allows multiple traces to run between pins.

Skin effect—Another consideration affecting trace routing at high speeds is skin effect. At the very high frequencies of emerging communication systems like Sonet and Fibre Channel, the small cross-sectional area of traces can produce significant skin-effect losses as the energy propagates only on the outside of the conductor. Skin effects can be reduced by using larger traces. A 2.5-mm spacing will allow larger traces with more convenience. Here again, new dielectric materials allow greater design flexibility in trace widths and the thickness of board layers since the height and width of the trace is a factor in determining characteristic impedance.

Skew—An important effect that must be considered in designing a connector into the system. Since each

row of a connector typically has a different length, due to the right-angle daughtercard connector, the connector introduces skew if multiple rows are used for parallel data. Skew can be easily corrected by introducing different compensating path lengths in theboard traces.

Capacitance—Large backplane connectors are through-hole devices using plated-through holes (PTH). The capacitance of the PTH is a function of the surface area of the hole and the dielectric constant of the board material. Since thick boards have deep PTHs, the increase in surface area increases the capacitance. Higher capacitance is of concern for two reasons: It can slow the rise time of a signal, and it can increase crosstalk from capacitive coupling between lines. A larger separation between pins decreases the coupling and lowers crosstalk.

Alternative board materials can be used to lower capacitance (and to provide faster propagation speeds). The choice of board material directly affects board stackups allowed to maintain the required impedances. Traditional FR-4 fiberglass epoxy boards have a relatively high dielectric constant of 4.5, which directly limits how thin board layers—and by extension PTHs—can be. Characteristic impedance for microstrip and stripline circuits, after all, is determined solely by the geometrical relationship between the signal line and ground plane and by the dielectric constant of the material separating them. Other materials, such as Teflon, GETEK, and Rogers 3000 PTFE, have lower dielectric constants—about 3 or less—that allow thinner multilayer boards to be fabricated.

Since the signal-to-ground ratio in a connector depends on the edge rate of the signals, the designer should carefully evaluate the needs of various signals. High-speed signals with picosecond edge rates require a 1:1 ratio. Lower-speed signals, including control signals, can get by with fewer ground pins. The same signal-to-ground ratio does not have to be consistent throughout the connec[illegible] Slow-speed signals can be allocate[illegible] one end of the connector at a 5:1 or signal-to-ground ratio. High-sp[illegible] signals at a 1:1 ratio also can[illegible] grouped together.

Depending on the system, sev[illegible] levels of partitioning can be u[illegible] Such partitioning makes more ef[illegible]tive use of connector resources reducing the number of pins dedi[illegible]ed to ground. An alternative is to u[illegible] more than one connector. For exa[illegible]ple, use a controlled-impedance connector for high-speed signals and an open-pin-field connector for medium- and low-speed signals.

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ADVERTISERS INDEX

ANALOG DESIGN SOLUTIONS 1

Ultralow-Noise LDO Voltage Regulators

Communication and VCO circuits require well regulated, low noise supply lines that can switch on and off quickly. They also need small size, high precision, and low power ICs.

MIC5205/06 low-dropout linear regulators can improve noise performance by 20dB over other regulators, making them ideal for voltage-controlled oscillator (VCO) and RF circuits.

Both are low-dropout PNP regulators that include a reference bypass pin for additional noise reduction. A single 470pF capacitor, connected from the bypass pin to ground, reduces output noise by V_{OUT}/1.24V (12dB for the 5V part) and creates a noise pole below 100Hz.

With better than 1% output accuracy and ground current of less than 0.6mA at a 100mA load, the MIC5205/06 are ideal for hand-held battery-powered applications.

The MIC5205/06 are efficient, accurate, ultralow-noise regulators with typical output noise of 260nV/$\sqrt{Hz}$. To maximize battery life, the dropout voltage is typically 10mV at light loads. At the rated 150mA output, dropout voltage is only 165mV.

Key Features

- Ultralow noise
- 150mA output current
- 1% output accuracy
- Wide choice of output voltages
- "Zero" off-mode current
- Current, thermal and reverse battery protection
- Fast transient response
- Ultra-tiny SOT-23-5 and MSOP-8 packages

Prolongs Battery Life

The MIC5205/06 extend operating life by prolonging battery charge. It maintains regulation with as little as a 50mV differential between input and output and offers an on-chip on/off control that reduces power drain to less than 1µA. In sleep mode, quiescent current drops to nearly zero, further extending battery life.

Protection

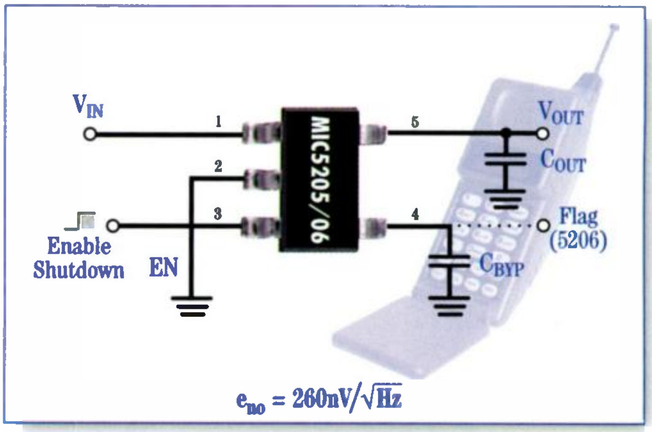
Additional safety features include reversed battery protection, current limiting and overtemperature shutdown. The MIC5206 also provides an Error Flag to indicate output voltage faults such as low battery, overcurrent, or overtemperature conditions.

Fixed or Adjustable Voltages

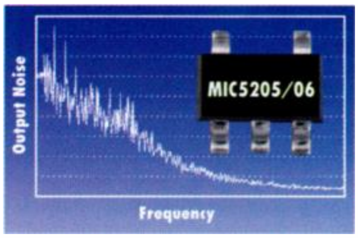
The MIC5205/06 are available with fixed or adjustable output voltages. Standard fixed voltages are 3.0V, 3.3V, 3.6V, 3.8V, 4.0V and 5.0V. All parts have 1% initial accuracy and operate over a junction temperature range of -40°C to +125°C.

Designed for Ultralow-Noise

The MIC5205/06 were designed for excellent low-noise performance but have even better performance with an optional external capacitor. This capacitor

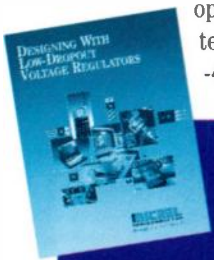


(C_{BYP}) is inserted into the voltage divider that sets the loop gain necessary to achieve a specific output voltage. Although gain is a necessary part of the feedback that makes a regulator work, it also "amplifies" noise. The capacitor reduces the loop gain at high frequencies to reduce high-frequency noise.



Fits Anywhere

Both of these new regulators are available in Micrel's IttyBitty™ SOT-23-5 five-lead packages and include a logic compatible Enable pin. The MIC5206 is also available in the new Micrel Mini8™ 8-lead MSOP package.



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