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ELECTRONIC DESIGN

TECHNOLOGY · APPLICATIONS · PRODUCTS · SOLUTIONS

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OCTOBER 23, 1997

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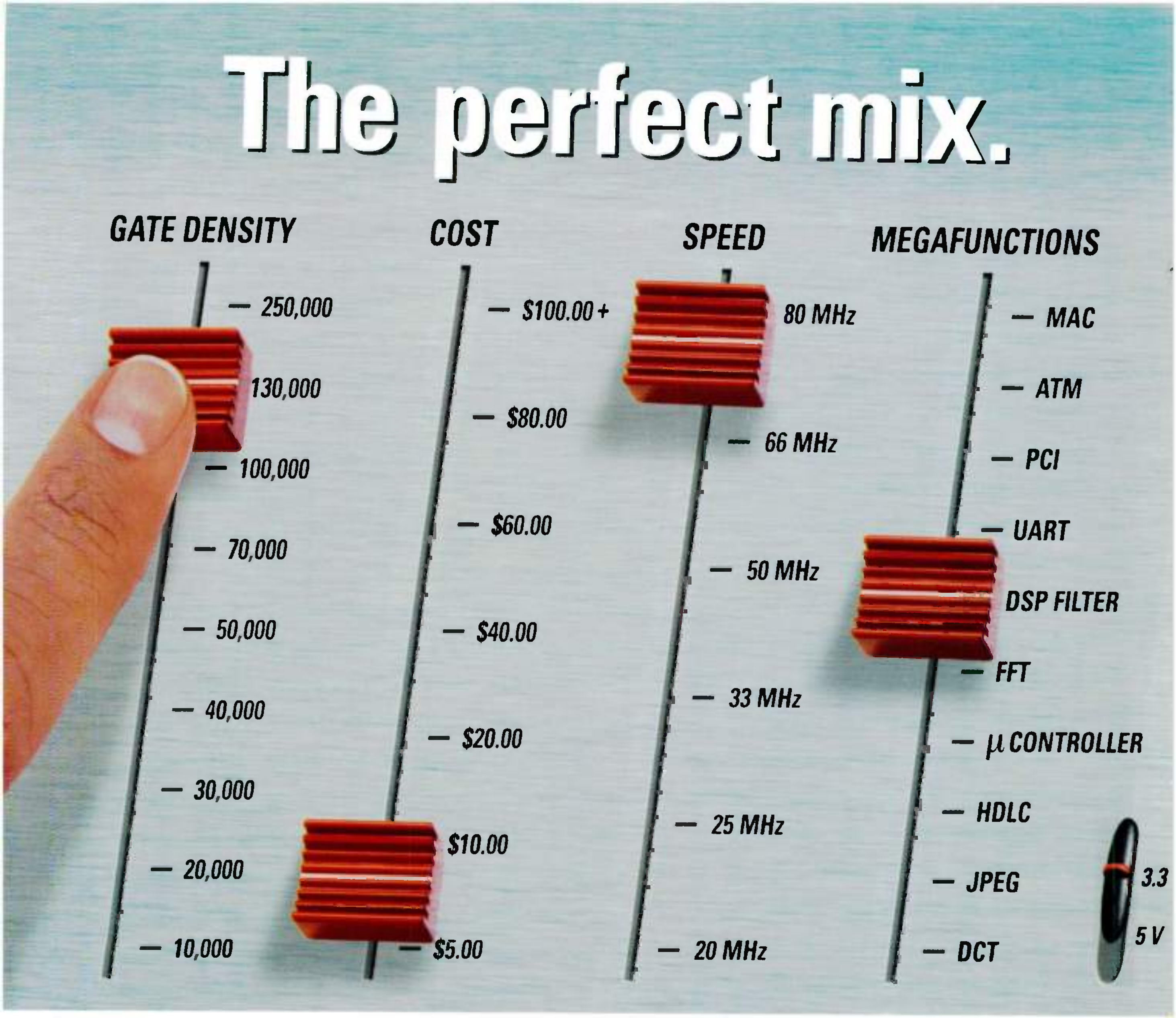

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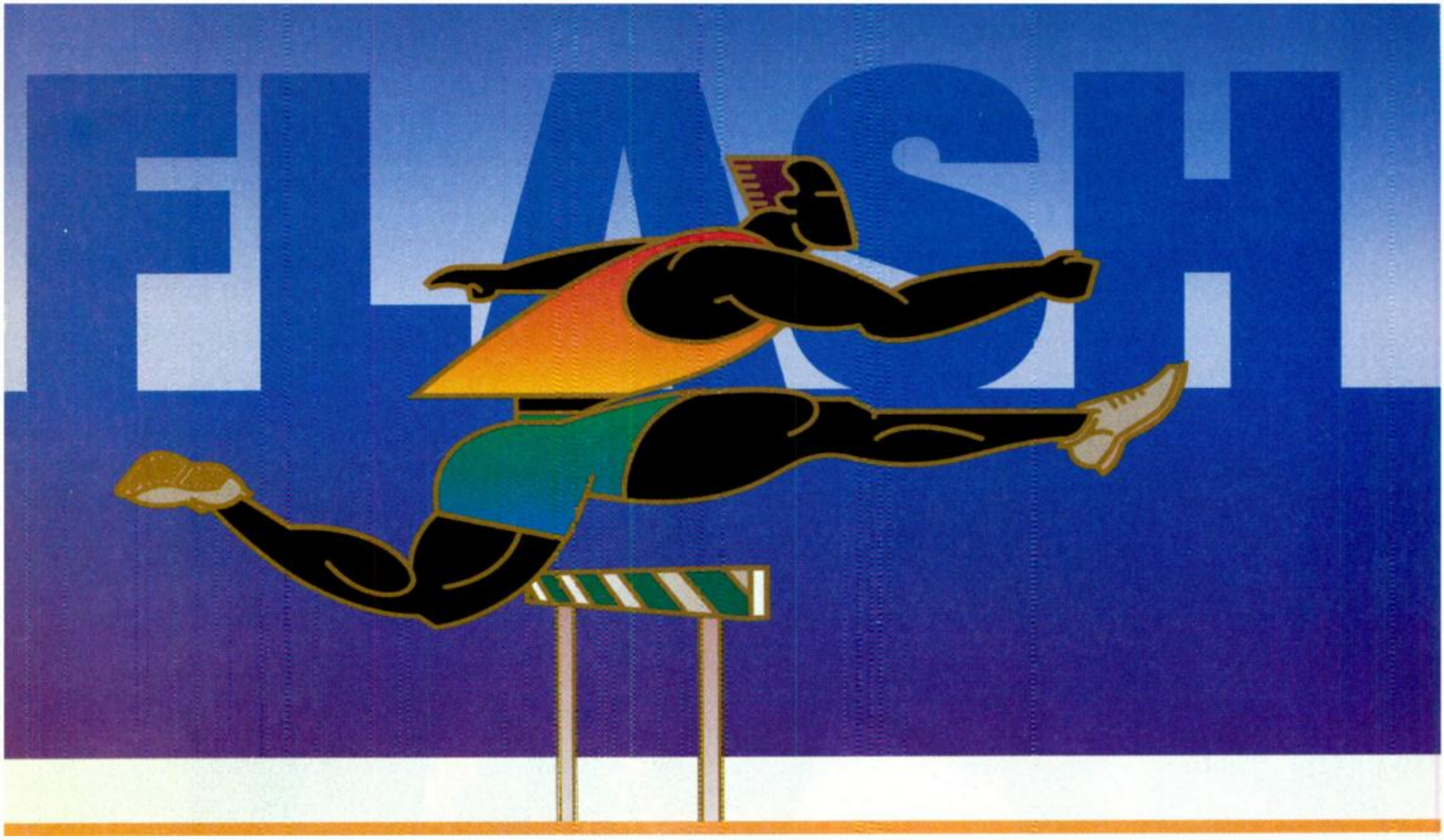

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68HC916X1	16-bit	50K	2K SRAM	GPT	A/D, PWM, 2 SCI, SPI	120 QFP
68HC916Y1	16-bit	48K	4K SRAM	TPU, GPT	A/D, SCI, SPI	160 QFP
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October 23, 1997 Volume 45, Number 23

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TECH INSIGHTS

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DEPARTMENTS

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ELECTRONIC DESIGN

TECHNOLOGY • APPLICATIONS • PRODUCTS • SOLUTIONS

October 23, 1997 Volume 45 Number 23

EDITORIAL OVERVIEW

COVER ILLUSTRATION BY: BRUCE JABLONSKI

Jesse H. Neal Editorial Achievement

1967 First Place Award	1978 Certificate of Merit
1968 First Place Award	1980 Certificate of Merit
1972 Certificate of Merit	1986 First Place Award
1975 Two Certificates of Merit	1989 Certificate of Merit
1976 Certificate of Merit	1992 Certificate of Merit

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Efficiency @ Full Load	90%	88%	91%
Osc. Frequency	10kHz or 80kHz, 80kHz*	20kHz or 150kHz, 150kHz**	800kHz
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Function	Double/Invert	Double/Invert	3/2, 2/3 Fractional Converter

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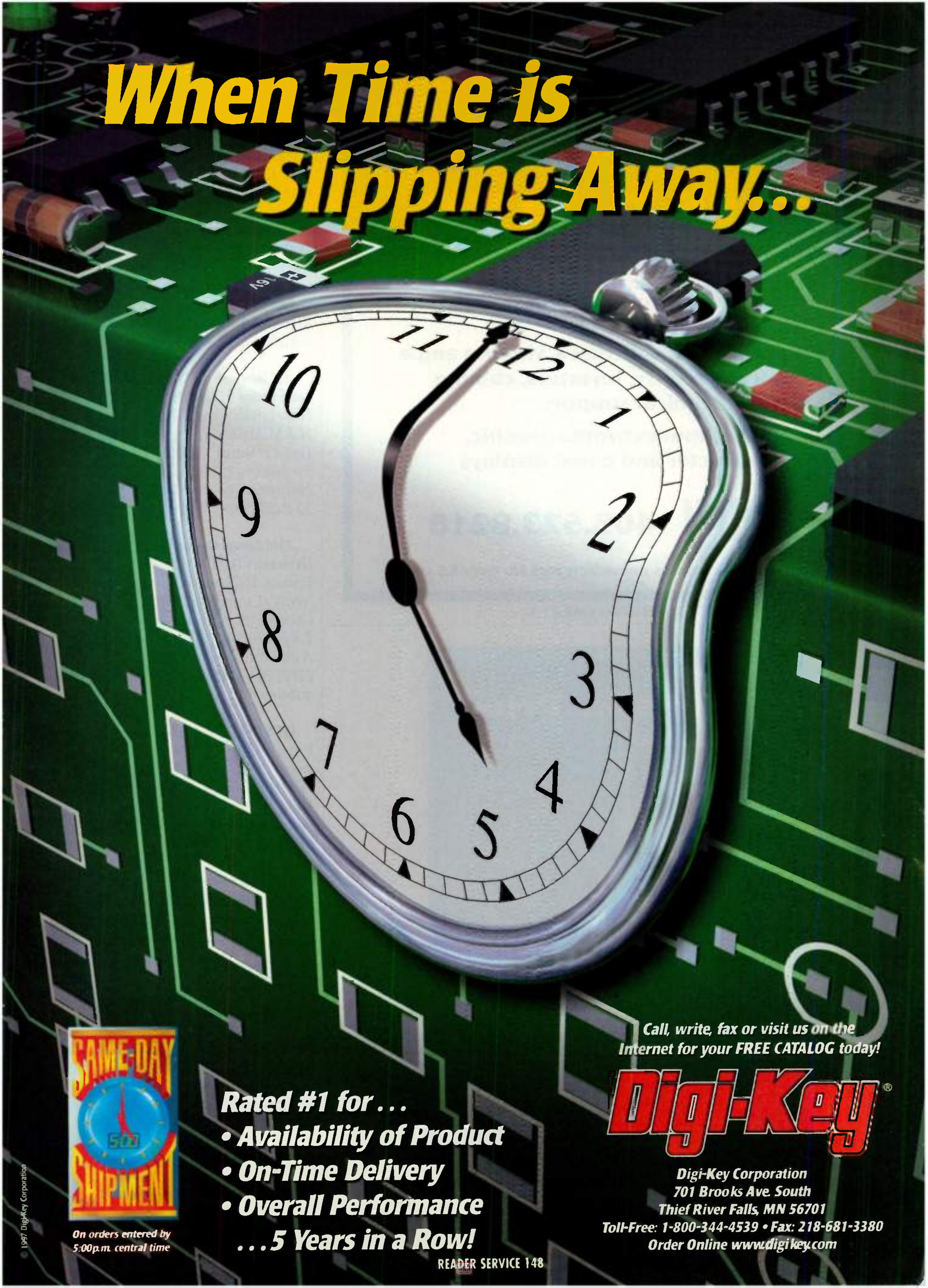
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NOVEMBER 1997

IEEE Nuclear Science Symposium (NSS '97), November 8-15. Albuquerque, NM. Contact Roger Gearhart, SLAC, P.O. Box 4349, Stanford, California 94309; (415) 926-2709; fax (415) 926-4999.

IEEE Intelligent Transportation Systems Conference (ITS '97), Nov. 9-12. Boston Park Plaza Hotel, Boston, MA. Contact Richard Sparks, 8 Richard Rd., Bedford, Massachusetts 01730; (617) 862-3000; fax (617) 863-0586; e-mail: r.sparks@ieee.org.

IEEE International Conference on Computed Aided Design (ICCAD), Nov. 9-13. Red Lion Hotel, San Jose, CA. Contact Ralph H.J.M. Otten, Electrical Engineering Department, Delft University of Technology, Mekelweg 4, 2628 CD, Netherlands, +31 15-2781600; fax +31 15-2786190; otten@et.tudelft.nl.

23rd Annual Conference of IEEE Industrial Electronics (IECON '97), November 9-14. Hyatt Regency Hotel, New Orleans, Louisiana. Contact Michael Greene, 200 Broun Hall, Electrical Engineering, Auburn University, Auburn, Alabama 36849-5201; (334) 844-1828; e-mail: greene@eng.auburn.edu.

LEOS '97, Nov. 10-13. Crowne Plaza Parc Fifty Five Hotel, San Francisco, CA. Contact Melissa K. Estrin, IEEE/LEOS, 445 Hoes Ln., P.O. Box 1331, Piscataway, NJ 08855-1331, (908) 562-3896; fax (908) 562-8434; e-mail: mestrin@ieee.org.

Productronica '97, Nov. 11-14. Messegelande, Munich, Germany. Contact Messe Munchen GmbH, Messegelande, D-80325 Munchen, Germany; +49 (89) 51 07-0; fax +49 (89) 51 07-506; e-mail: info@messe-munchen.de; Internet: http://www.Productronica.de.

Supercomputing '97, Nov. 15-21. San Jose Convention Center, San Jose, CA. Contact IEEE Computer Society, 1730 Massachusetts Ave., N.W., Washington, DC 20036-1992; (202) 371-1013; fax (202) 728-0884; http://www.computer.org.

Asian Test Symposium, Nov. 17-19. Akita, Japan. Contact Y. Takamatsu, +81 89 927-9955; e-mail: takamatsu@cs.ehime-u.ac.jp.

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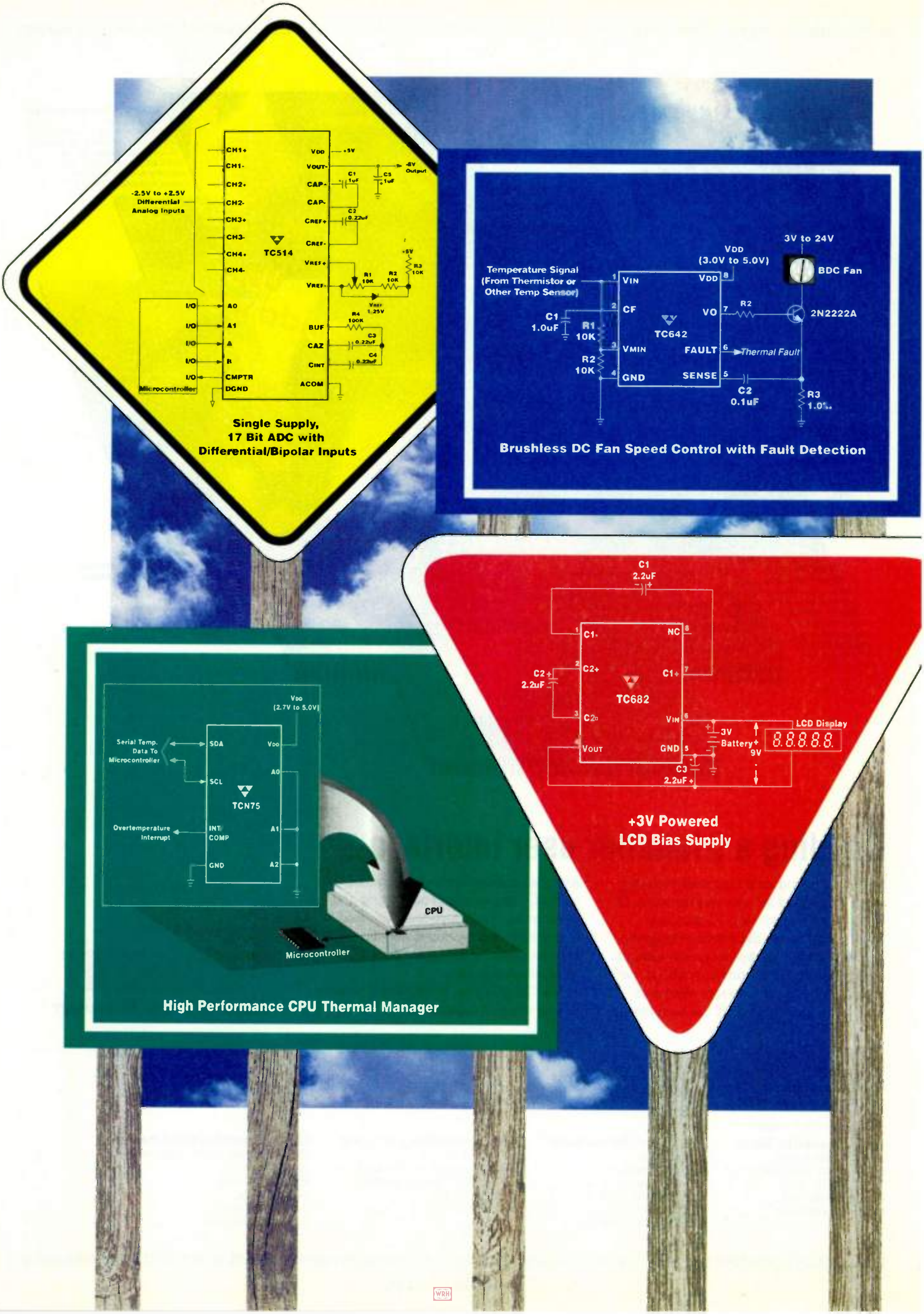

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NOVEMBER

COMDEX/Fall '97, November 17-21. Las Vegas Convention Center, Las Vegas, Nevada. Contact Softbank Comdex Inc., 300 First Ave., Needham, Massachusetts 02194-2722; (617) 433-1500; Internet: http://www.comdex.dom.

IPC National Conference: Solutions for Ultra-High-Density PWBs, Nov. 20-21. Biltmore Hotel, Santa Clara, CA. Contact John Riley, IPC director of education, (847) 509-9700, ext. 308.

DECEMBER

Winter Simulation Conference (WSC '97), December 7-10. Renaissance Waverly Hotel, Atlanta, Georgia. Contact David Withers, LEXIS-NEXIS, P.O. Box 933, Dayton, Ohio 45401; e-mail: David.Withers@lexis-nexis.com.

IEEE International Electron Devices Meeting (IEDM), Dec. 7-11. Washington Hilton & Towers, Washington, DC. Contact Phyllis Mahoney, Widerkehr & Assoc., 101 Lakefrorest Blvd., Suite 270, Gaithersburg, MD 20877; (301) 527-0900; fax (301) 527-0994; e-mail: pwmahoney@aol.com.

36th IEEE Conference on Decision & Control, December 8-12. Hyatt Regency, San Diego, California. Contact Ted E. Djaferis, Department of Electrical & Computer Engineering, University of Massachusetts, Amherst, Massachusetts 01003; (413) 545-3561; fax (413) 545-1993; e-mail: djaferis@ecs.umass.edu.

Workshop on Internet Technology & Systems (WITS), December 9-12. Marriott Hotel, Monterey, California. Contact USENIX Conference Office, 22672 Lambert Street, Suite 613, Lake Forest, California 92630; (714) 588-8649; fax (714) 588-9706; e-mail: conference@usenix.org; Internet: http://www.usenix.org.

JANUARY 1998

Seventh Joint Magnetism & Magnetic Materials Conference (INTEMAG), January 6-9. Hyatt Regency Embarcadero Hotel, San Francisco, California. Contact John Nyenhuis, School of ECE, Purdue University West Lafayette, Indiana 47907-1285; (317) 494-3524; fax (317) 494-2706; e-mail: smag@ecn.purdue.edu.

Annual Reliability & Maintainability Symposium/Product Quality & Integrity (RAMS), Jan. 20-22. Anaheim Marriott, Anaheim, CA. Contact V.R. Monshaw, Consulting Services, 1768 Lark Lane, Cherry Hill, New Jersey 08003; (609) 428-2342.

Photonics West, Jan. 24-30. San Jose, California. Contact the SPIE Exhibits Dept., P.O.Box 10, Bellingham, Washington 98227-0010; (360) 676-3290; fax (360) 647-1445; e-mail: exhibits@spie.org.

Seventh Security Symposium, January 26-29. Marriott Hotel, San Antonio, Texas. Contact USENIX Conference Office, 22672 Lambert Street, Suite 613, Lake Forest, California 92630; (714) 588-8649; fax (714) 588-9706; e-mail: conference@usenix.org; Internet: http://www.usenix.org.

IEEE Power Engineering Society Winter Meeting, January 31-February 5. Tampa, Florida. Contact Jim Howard, Tampa Electric Co., Post Office Box 111, Tampa, Florida 33601; (813) 228-4653; fax (813) 228-1333; e-mail: j.howard@ieee.org.

FEBRUARY 1998

IEEE International Solid-State Circuits Conference (ISSCC '98), Feb. 5-7. San Francisco Marriott, San Francisco, California. Contact Diane Suiters, Courtesy Associates, 655 15th St. N.W., Washington, DC 20005; (202) 639-4255; fax (202) 347-6109; e-mail: isscc@courtesyassoc.com.

Portable by Design, February 9-13. Santa Clara Convention Center, Santa Clara, California. Contact Rich Nass, Electronic Design, 611 Route 46 West, Hasbrouck Heights, New Jersey 07604; (201) 393-6090; fax (201) 393-0204; e-mail: portable@class.org.

The Wireless Symposium and Exhibition, February 9-13. Santa Clara Convention Center, Santa Clara, California. Contact Bill Rutledge, Penton Publishing, 611 Route 46 West, Hasbrouck Heights, New Jersey 07604; (201) 393-6259; fax (201) 393-6297; instant faxback (800) 561-7469; Internet: www.penton.com/wireless.

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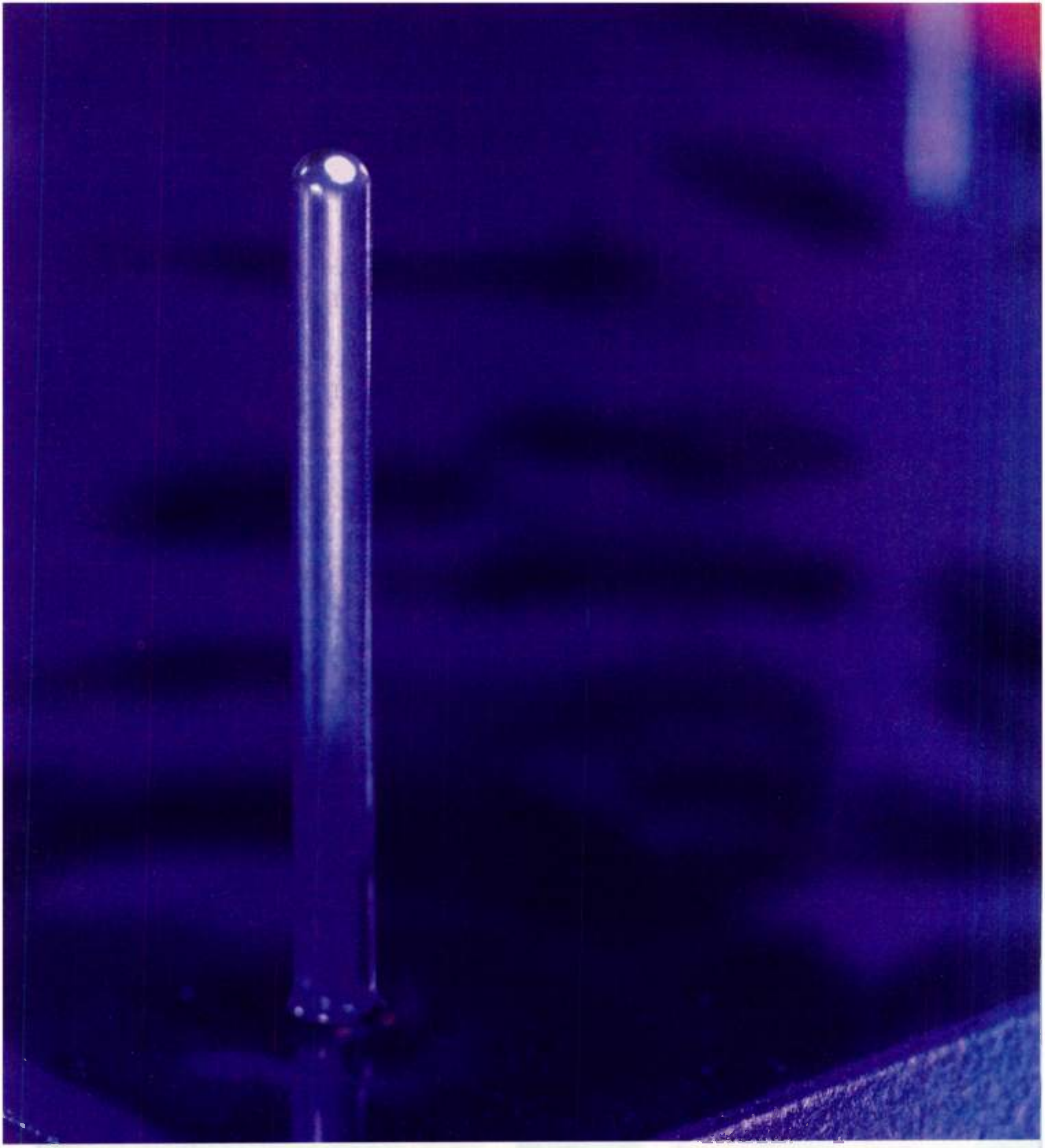

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READER SERVICE 177

EDITORIAL

What's In A Name?

If you've taken a good, close look at the cover of this issue, you'll notice that there are four new words that appear under the *Electronic Design* banner. They are:

TECHNOLOGY ▪ APPLICATIONS ▪ PRODUCTS ▪ SOLUTIONS

In the magazine business, these words are what's known as a "tag line." Basically, it's a catchy term or phrase that helps further define a magazine's position in the marketplace. Many publications use them to reinforce or hype their circulation ("The Most Widely Distributed Magazine..."); status ("The No. 1 Newspaper Covering..."); frequency ("The Only Bi-Weekly Magazine..."); or readership ("The Top Journal For CEOs").

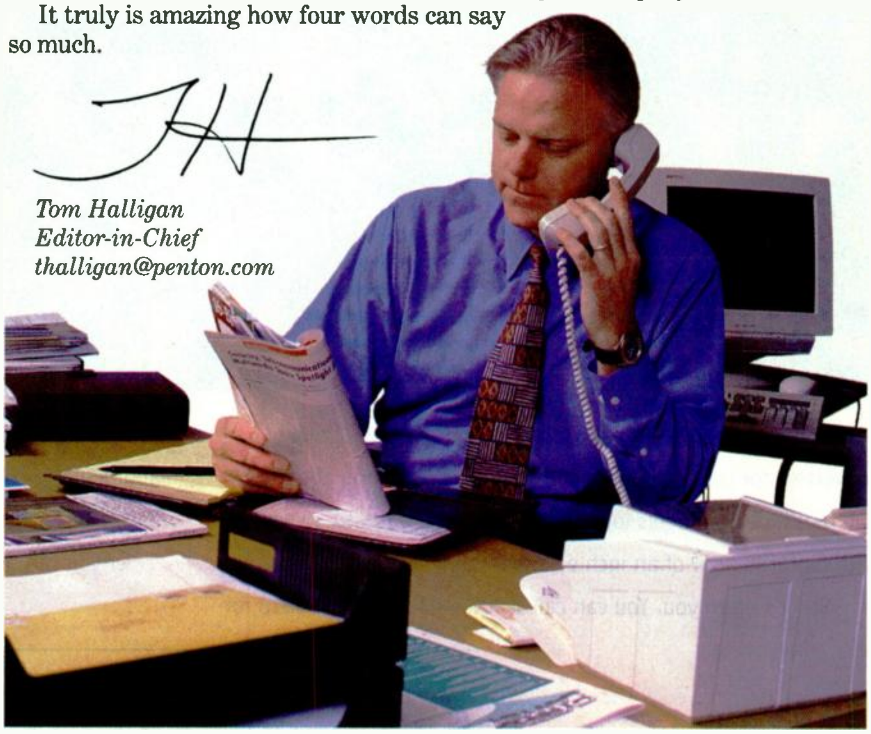
ELECTRONIC DESIGN
TECHNOLOGY·APPLICATIONS·PRODUCTS·SOLUTIONS

All of these tag lines are fine. However, *Electronic Design* has adopted a new tag line that succinctly and directly defines our editorial mission. What now appears under the banner are words that our editorial team focuses on every time they sit down to write or edit an article. They inform both our readers and advertisers exactly what our mission is—today and tomorrow.

We selected the tag line for two specific reasons. First, these four words represent the core components of our editorial mission. Technology—providing in-depth coverage and analysis on emerging and new technologies emanating from the electronic industry's top labs, R&D facilities, universities, and cutting-edge companies from around the world. Applications—analyzing how new technology is targeted to specific applications, such as telecommunications, medical, consumer, or computing. Products—presenting the latest products we feel will help our readers, design engineers and engineering managers, compete in the high-tech design world. Solutions—offering you contributed articles, columns, and design tips that help you build better products faster and more efficiently.

Second, the tag line represents the environment in which today's design engineer works. New technology emerges and is embraced by design engineers to build or improve a product for a specific application, which leads to a new product introduction that will become a better solution for your company's customers.

It truly is amazing how four words can say so much.



Tom Halligan
Editor-in-Chief
thalligan@penton.com

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(Cycle time/ns: -8 = 125 MHz, -10 = 100 MHz, -12 = 83 MHz

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READER SERVICE 171

If Batteries Only Had A Brain...

With all the technology at our disposal, why can't we develop a battery subsystem that can accurately gauge the remaining time in a laptop, handheld computer, or cellular phone? It turns out that the technology is available, but no one is willing to absorb the cost. The system makers want the technology, but they don't want to pay for it. The battery makers have the technology, but they want the system manufacturers to pay for it.

The answer is in the Smart Battery System specification, which was developed by a group of battery and IC vendors. A smart battery is defined as a battery equipped with specialized hardware to provide the battery's present state, as well as calculated and predicted information, to the host. The smart battery is accompanied by a smart charger, which alters its charging characteristics in response to information provided by the smart battery.

Key to the SBS spec is the System Management Bus (SMBus). The SMBus is a two-wire interface through which simple power-related chips can communicate with the rest of the system. It uses the I≈C bus as its backbone. However, some fundamental differences exist between the SMBus and the I≈C bus. For example, the SMBus is based on fixed voltage levels, whereas the I≈C levels are scalable. And the SMBus specifies a minimum operational clock speed and device time-outs.


RICHARD NASS
COMPUTER SYSTEMS

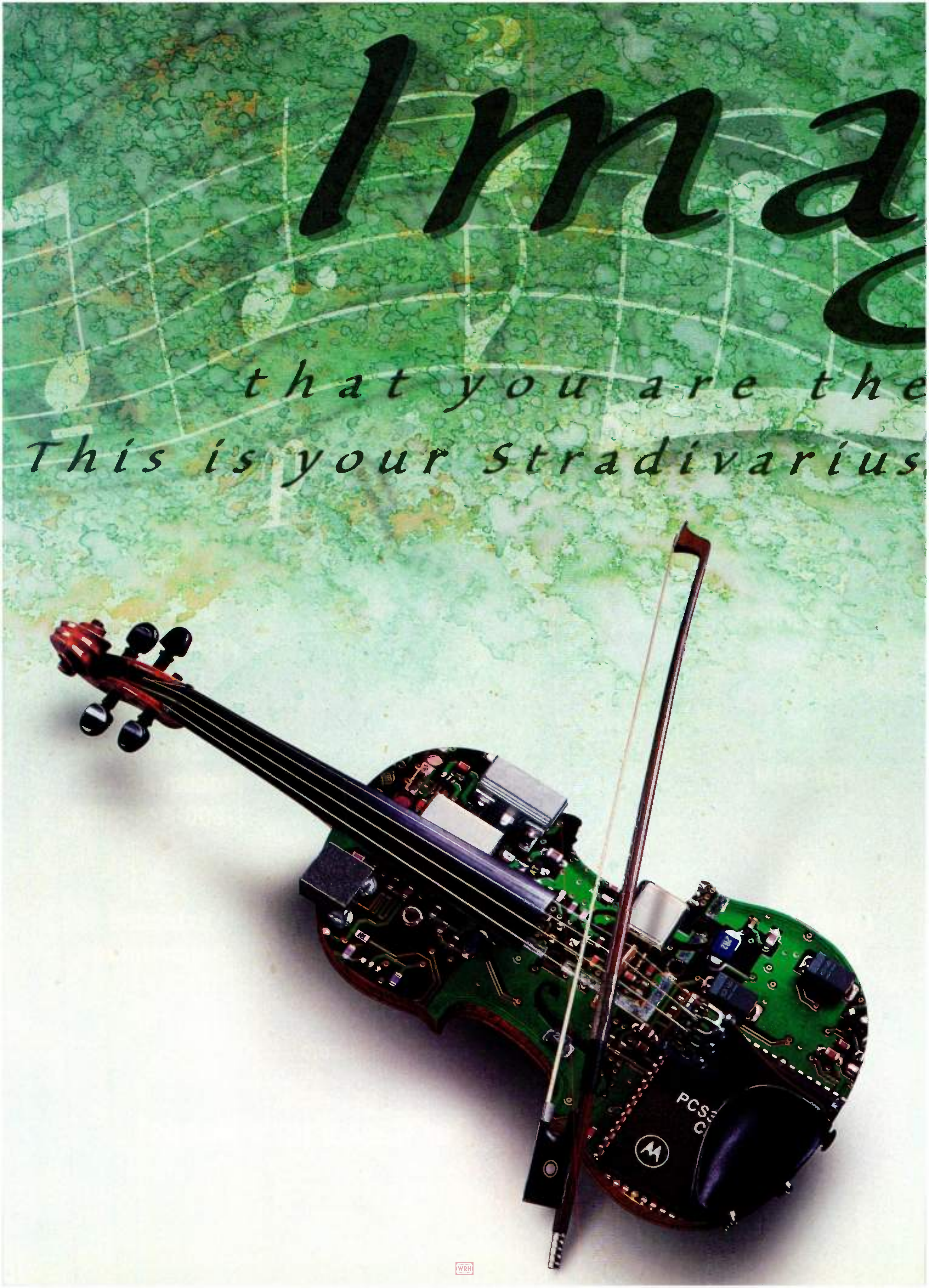
The power-management circuitry can query a device driver to determine if an action will cause harm to the system's integrity. For example, spinning up a disk drive when the battery is nearly discharged may cause its output voltage to drop below acceptable limits, causing a system failure. To prevent this, the device driver needs the correct information from the battery. If the driver queries the battery and discovers that there's not enough power, it can request that the power-management system turn off a noncritical subsystem, such as the LCD backlight, and then try again.

The interface to the SMBus can be found in many places, but is most commonly put into the chip set or the keyboard controller. Intel's latest mobile chip set, the 430TX, contains the SMBus interface. In a microcontroller, such as the keyboard controller, the system would write to the proper register addresses and the microcontroller would translate those commands to SMBus commands. In the chip set, that process is handled in hardware.

The smart battery and charger combination provide two distinct advantages in system performance and cost. First, charging characteristics are integral to the battery itself, allowing for chemistry independence and ideal charging algorithms that match the specific cell types. Each smart battery defines the charging scheme that's best suited to its chemistry and capacity. This makes the most of the usable energy at each charge, cuts the charge time, and maximizes the number of charge cycles (the number of times a battery can be charged). Second, the cost and complexity of the system is reduced as the charger need only provide the charging voltage and current specified by the battery, without duplicating the measurement and control electronics already in the battery.

When it comes to the battery subsystem, there's been some controversy as to where the charging commands originate. The charger should get its commands from the battery, as defined by the specification. But it's important to prevent an application from sending commands to the charger. If that did happen, it's possible a piece of code (i.e., a virus) could come in and tell the charger to overcharge the battery, causing it to explode.

There needs to be an interface for the operating system to get information from the battery, the charger, the battery subsystem, and any other SMBus device. That interface allows the operating system to receive information. But it's important that the OS not be able to send commands to the charger. A virus wouldn't come from the OS itself, but rather from a utility. *rnass@penton.com*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Computer Program Monitors Microchip Etch Process

A system that monitors the etching process during microchip manufacture is expected to dramatically reduce the cost and effort of recognizing, locating, and correcting malfunctions as they occur in production. Such malfunctions can, on average, cost manufacturers millions of dollars. The relatively low-cost technology also rectifies fabrication errors in the last stages of manufacture of printed-circuit boards. The seeds of the program came from a Sematech project that began back in September 1995, combining the resources of Advanced Micro Devices, San Jose, Calif., and Sandia National Labs, Albuquerque, N.M. The technique, invented by Sandia scientists Pam Ward, Joel Stevenson, and Michael Smith, officially began development in December of 1996.

The technique is based on work done jointly by Sandia and the National Center for Manufacturing Sciences, Ann Arbor, Mich., which improved the manufacture of pc-boards. The initial problem researchers tried to overcome was how to deal with the often temperamental behavior of the two or three gases involved in the etching process. In some instances, for example, a leak may be present that allows air to enter and form its own plasma. Or a flow controller may stick producing the wrong mix. In other cases, the pumping speed may be off, or a residue of moisture may be in the system. All of these factors can adversely affect the way the plasma will perform.

Although the technique of monitoring plasmas to etch circuits during pc-board manufacture is well known, Sandia developed a computer program that makes it possible to analyze the process as it occurs and correct a variety of malfunctions before a batch is spoiled. Although the technique can't detect the moment of complete removal of the epoxy smears that develop near the end of the fabrication process, it can help approximate the moment of removal by assuring that the plasma is healthy and working accurately.

Because both printed-circuit boards and microchip devices are etched by plasmas, the natural progression was to translate the technology for use with microchips. The recently developed microchip technique combines a new version of Sandia's sophisticated computer program with a camera and peripheral equipment such as a laptop computer.

The program works by controlling up to 64 pieces of equipment, and once the monitor detects a failure, can work to rectify it by paging for help, sounding an alarm, running diagnostics, adjusting plasma parameters, and replacing any needed parts. The camera is utilized to spectroscopically analyze optical emissions from the plasmas as they etch the silicon wafers. Though the technique isn't new, the software program allows near-instant analyses of emitted wavelengths to detect if the plasma is behaving incorrectly. It does this by pattern recognition, which examines the plasmas fingerprint and compares it to the fingerprint of a known failure.

Further details can be obtained by contacting the Media Relations department of Sandia National Labs at (505) 844-8066 or by checking out either of the Lab's web pages at *http://www.sandia.gov/media/whatnew.html* or *http://www.sandia.gov/LabNews/LabNews.html*. CA

Flat Plastic Displays Should Be Ready By The End Of The Year

Commercial products using light-emitting polymer (LEP) technology, developed by Cambridge Display Technology Ltd (CDT), Cambridge, England, are expected to enter volume production before the end of the year, according to Mark Gostick, the company's marketing director. The first appearance is expected to be in the form of backlights for displays and keyboards in mobile telephones made by Philips Electronics BV of the Netherlands.

Gostick explains that CDT holds 11 basic patents covering light-emitting plastic materials, one involving light emission from conjugated polymers. He claims the patents are now "uncontested" following the withdrawal of opposition and the signing of licenses by Philips Components B.V. and UNIAX Corp., Santa Barbara, Calif. German chemical firm Hoechst AG of Frankfurt has been licensed to manufacture the polymer materials.

To date, licenses have covered only what Gostick designates "low information content" display devices with fewer than 100,000 pixels. Applications include backlights and monochrome digit displays for digital instruments, clocks, calculators, telephones, and the like. Now Gostick is busy signing up licensees for high-information-content licenses.

Already one such license has been granted for the development of a 2.5-in. diagonal high-resolution display for use in "virtual reality" head sets. Gostick will not name his most recent partner, but it has been identified as Integrated Device Technology Inc. of Santa Clara, Calif. Additional partnerships will be consummated by the beginning of 1998, Gostick promises, including a deal with "a very large Japanese company" that will develop high-definition full-color panels of at least 12 in. diagonal for use in various computer displays.

So far, light-emitting polymer displays have been limited to the emission of green light. But now Cambridge Display is concentrating efforts on blue and red displays, increasing efficiency and lifetime. Gostick claims that lifetime has been extended now to around 15,000 hours continuous operation. Other areas for development include the use of flexible substrates and the use of materials other than glass. For more information, visit Cambridge Display Technology Ltd.'s web site at *http://www.cdtld.co.uk*. PF

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New Characterization Technology Targeted At Intellectual Property

A technology agreement between Synopsys, Mountain View, Calif., and Advanced RISC Machines, Los Gatos, Calif., will aim to develop a new technology for complex intellectual-property (IP) core characterization used in systems-on-a-chip (SoC) designs. This partnership is expected to provide designers with a reliable methodology for exchanging timing information, reduce the risk of misinterpreting delay numbers without sacrificing performance, and cut the turnaround time from a week down to one day. Consequently, designers are able to save literally months of expert resources.

This characterization technology for complex cores will be based on a combination of the EPIC-based Analog Circuit Engine (ACE) technology and a newly developed hybrid static/dynamic analysis. In effect, it will provide design knowledge encapsulation to adequately measure complex timing and behavior (state-dependent delays), and provide Spice-level accuracy on designs with millions of transistors. It takes a designer's knowledge of critical parameters and encapsulates them within a control file. As a result, designers who don't have in-depth knowledge about the core, but wish to use it, can still characterize to a new process without help from the original designer. The control file is created as a by-product of the design process and thus requires minimal design overhead. The characterization technology solution will include a complete set of API functions that let users control output format, including SDF and STAMP.

This solution is meant to replace existing gate characterization systems that have proven inadequate for advanced devices containing soft/firm/hard cores of IP. Synopsys plans to release a product with this technology in the last quarter of this year. For further details on the technology, contact the company at (415) 962-5000, or visit its web site at *http://www.synopsys.com.* CA

Behavioral Language Eyed As Driver Of Mixed-Signal Apps

To help spur the growth of multi-domain designs for mixed-signal IC and pc-board markets, Mentor Graphics Corp., Wilsonville, Ore., and European-based LEDA S.A., are jointly developing an implementation of a VHDL-AMS analog behavioral language. The implementation will support the IEEE VHDL-AMS 1076.1 standard, and rely on the use of the Eldo analog simulation kernal.

Once completed, the implementation will allow mixed-signal engineers to simulate both analog and digital parts of a system simultaneously, as well as develop a comprehensive system verification strategy. In addition, it will provide a migration path for designers to move from a traditional analog design methodology, based on Spice or its derivatives, to a faster system-style top-down approach that's unrestricted by language limitations. As a result, engineering teams will have the flexibility to choose the analog behavioral language, whether Verilog-A/MS or VHDL-AMS, that best fits the needs for a particular design block, without the worry of how to simulate the design. As an added benefit, the planned implementation will allow mixing and matching of VHDL-AMS and structural device-level descriptions.

As part of the agreement, Mentor Graphics will offer a VHDL-AMS simulator that will include LEDA's VHDL-AMS Analyzer. The product, which will be part of Mentor's family of advanced system-verification solutions, will be available shortly after the standard is finalized. In the meantime, the two companies will continue their work within the IEEE committees on VHDL-AMS 1076.1 standards enhancements. For further details, contact *http://www.mentorg.com.* CA

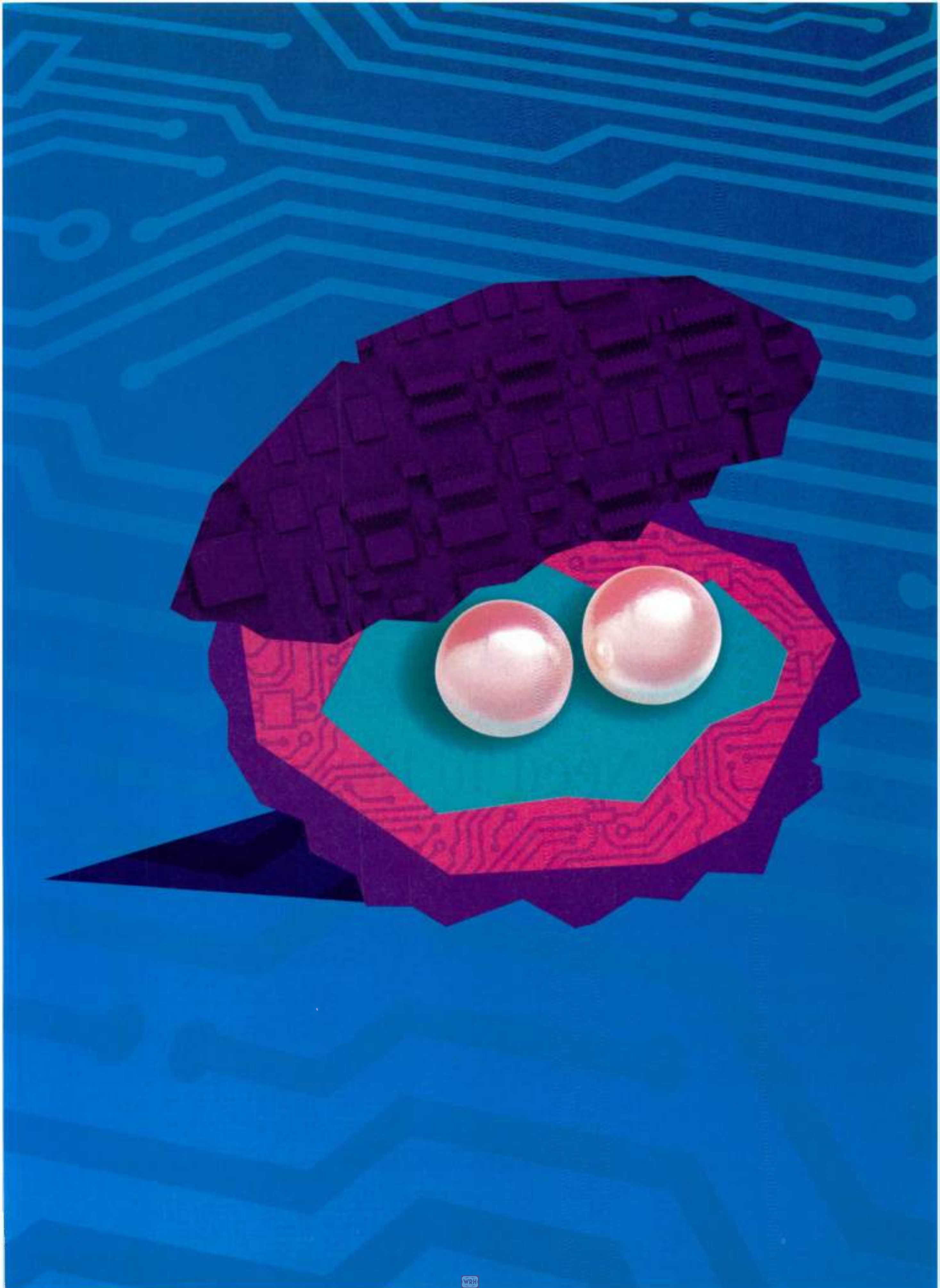
Specialized Flat-Panel Displays Meet Stringent Standards

A number of display-based applications, such as instrumentation, industrial control, factory automation, and entertainment, are known for their stringent design requirements. Two of the most important requirements include the ability to offer wide viewing angles and to function under extreme environmental conditions. Until now, the CRT has been the technology of choice for these applications. But many have sought, with limited success, to use liquid-crystal-display (LCD) technology as a replacement to the more traditional CRT.

A year-long alliance between Honeywell Business and Commuter Aviation Systems, Phoenix Ariz., and Mitsubishi Electronics America Inc., Sunnyvale, Calif., now hopes to overcome the limitations of the LCD technology through the development of a flat panel display referred to as DU-1080. This color, thin-film transistor (TFT) LCD will be specifically targeted for application in business aircraft and regional airlines.

At the heart of the device will be an LCD based on Mitsubishi's ANGLEVIEW flat-panel-display technology. It will incorporate Mitsubishi's panel and panel electronics combined with Honeywell's system-level technology to meet the stringent front-of-screen performance requirements of avionics displays. The panel and panel electronics technology will enable the richly saturated color and wide viewing angle capabilities. For additional details concerning this ongoing alliance, contact either Steve Henden of Honeywell at (602) 436-5312, or John Garner of Mitsubishi Electronics America at (408) 730-5900. CA

Edited by Roger Engelke



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Throw Away Those Silly Little 3D Glasses! New Interactive Display Frees Users From Wearing Them

Mention 3D displays—such as those for movies and video games—and the need to wear special polarizing glasses immediately comes to mind. To that end, the first professional 3D-viewing systems based on polarized glasses are currently available commercially. But the Heinrich-Hertz Institute, Berlin, Germany, has gone one step further: scientists there have developed a system that allows the display of 3D graphics from a PC monitor's screen without the need to wear special glasses. The implementation is a first step toward 3D displays for PCs or other desktops that are not yet close to market availability. They've further demonstrated an interactive 3D display that interprets the viewer's interest by reacting to eye movements.

The institute's scientists placed a "lenticular screen" made by Carl Zeiss AG, Oberkochen, Germany, in front of an LCD screen. This allows the LCD screen to display the image contents of the left and right data sources simultaneously in columns one beneath the other *(Fig. 1)*. As a result, columns 1, 3, 5, 7, etc., display the information for the left eye, while columns 2, 4, 6, 8, etc., show the information for the right eye.

The lenticular screen separates the two stereo pictures for the viewer's eyes. A head-tracking mechanism automatically tracks the movements of the viewer's head. Depending on these movements, the screen is mechanically adjusted to the left or to the right.

In a demonstration, the scientists used a flat thin-film-transistor (TFT) LCD color screen with a diameter of 14 in. and a resolution of 1024 by 768 pixels, resulting in stereo resolution of 1024 by 384 pixels. The lenticular screen adjustment had a mechanical positioning precision of 1 µm. Two IR sensors were employed to track the head's movements.

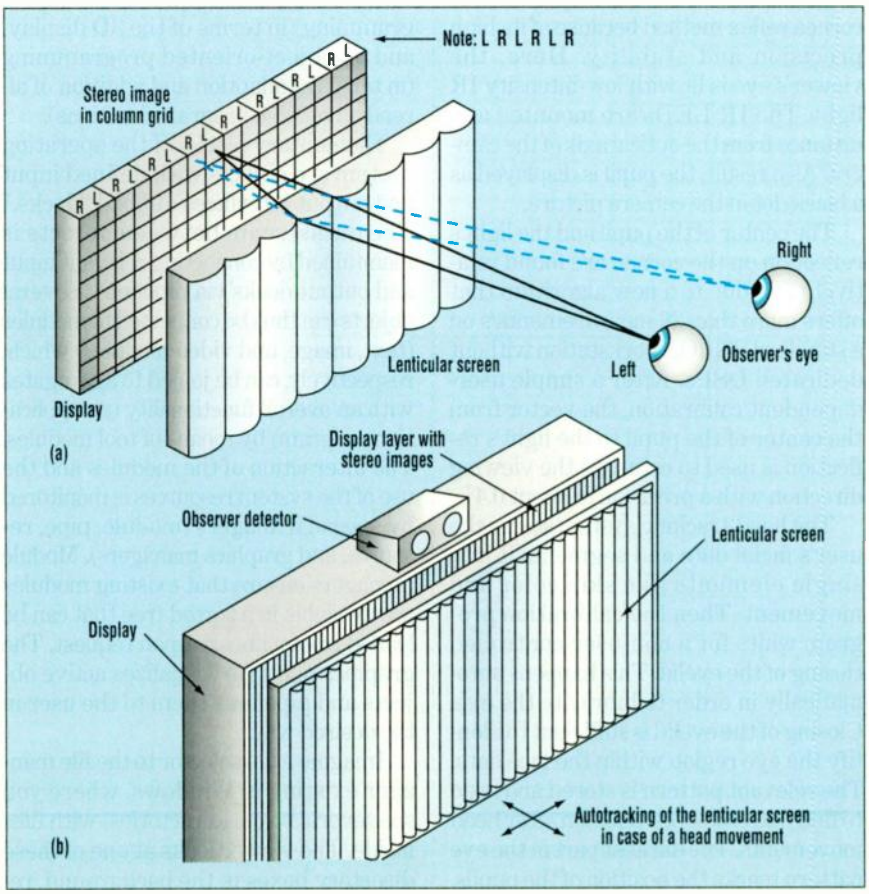
Input signals were either two analog CVBS camera signals (one for the left and one for the right eye) or a digital PC SVGA signal. The display unit's overall dimensions are 394 by 384 by 144 mm.

Other scientists at the institute considered practical implementations of 3D displays for PCs. They reason that 3D viewing on a PC can mean a lot more than just the display of 3D images, such as images in CAD programs.

The advent of graphical-user interfaces like windows, icons, and mouse pointers have considerably simplified the use of computer programs and files, compared with purely text-oriented input and output techniques. However, strictly 2D surfaces present obvious restrictions: when several applications run simultaneously, overlapping windows make it more difficult to watch the screen and to follow its contents.

A demonstration system dubbed BLICK (the German word that means "view") which was developed at the Heinrich Hertz Institute promises to clean up the virtual desktop *(Fig. 2)*. Stepping into the third dimension, it has opened up the possibility of providing documents, video images, application programs, databases, and networked computers with a clearer and more readable viewing structure.

The system's key elements are the aforementioned 3D display, a graphical 3D-user interface, a camera to measure the head's motion (a head-tracker or observer detector), and a system to gauge the direction of the user's gaze (eye-tracker). The display eliminates the need for 3D-viewing glasses and gives the user a genuine 3D representation of images produced either directly by the 3D visual operating system, or for video conferences by a stereo camera. With the head-tracker, a simple movement of the user's head can pull formerly hidden objects to the screen. Simultaneously, the eye-tracker determines the movements of the user's eyes and adjusts the screen so that only the object being looked at appears in full focus. Objects out of the user's gaze are temporarily considered unimportant and therefore shown out of focus to ensure that they



1. A lenticular screen allows the separation of viewed images created in a raster-scan mode (a). When placed in front of a flat LCD screen, the screen allows automatic tracking of a 3D image (b).

fade out of the viewer's perception.

Another important feature of BLICK is eye control. By interpreting the user's eye motions in the context of an application or by reacting to the user looking at an icon or a "hot" word, the system starts applications, shows connections between data objects, and downloads a hyperlinked document from the Internet. "If the system answers quickly and precisely, the user will forget that the computer is watching him," claims Dr. Siegmund Pastoor, BLICK project manager at the institute. "The viewer gets the feeling of communicating with an intelligent system that reacts to his intentions even before he has expressed them."

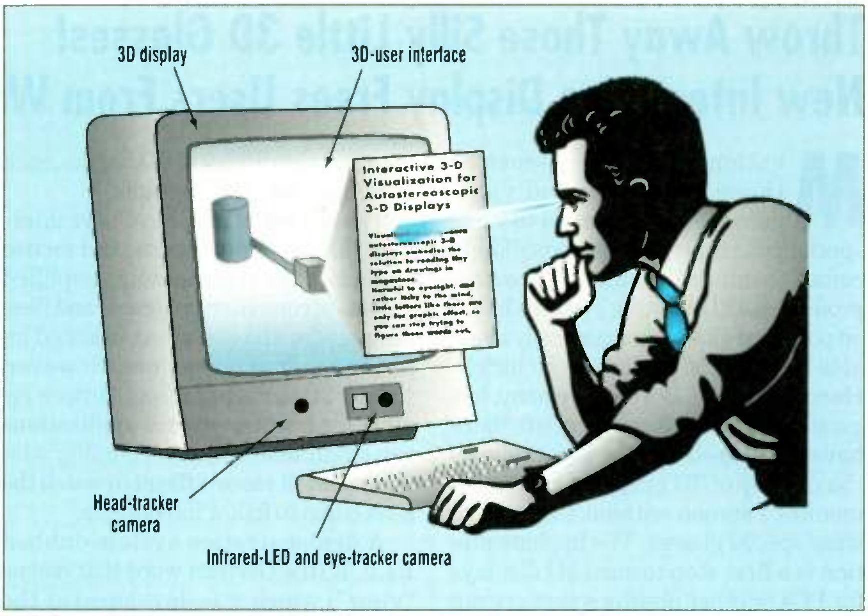
Because the eyes' movements are measured as well, it would not be possible to use any kind of polarizing glasses. The eye tracking is used to estimate the currently fixed viewing point within the 3D display's viewing room. This information is required to realize the non-command-based interactions as well as to implement the change of the image definition (focusing intensity).

The institute's scientists opted for the cornea reflex method because of its high precision and stability. Here, the viewer's eye is lit with low-intensity IR light. The IR LEDs are mounted at a distance from the optical axis of the camera. As a result, the pupil is displayed as a black dot in the camera picture.

The center of the pupil and the light's reflection on the cornea are found relatively fast due to a new algorithm that offers more than 20 measurements/s on a standard SGI/O2 workstation without dedicated DSPs. After a simple user-dependent calibration, the vector from the center of the pupil to the light's reflection is used to estimate the viewing direction with a precision of about 0.4°.

The head-tracking system stores the user's facial data and segments it into single elements like skin color and movement. Then the calibration program waits for a non-user-controlled closing of the eyelid. This happens automatically in order to lubricate the eye. Closing of the eyelid is sufficient to identify the eye region within the face data. The relevant pattern is stored and used to find back the eyes' position after head movements. The darkest part in the eye pattern marks the position of the pupils.

A core element of the interface is a new operating system that supports



2. A demonstration system developed by scientists at the Heinrich Hertz Institute allows instantaneous interactive viewing of 3D images on a desktop computer. The system uses the lenticular screen described in figure 1.

the 3D display, the act of "active seeing" and does not require instruction-based interactions. The operating system is based on the technique of visual programming (in terms of the 3D display) and on object-oriented programming (in terms of adaption and addition of already available program functions).

Elementary blocks of the operating system are objects with defined input and output interfaces dubbed "docks." The datastream between objects is maintained by connecting relevant input and output docks via pipelines. Several objects can thus be connected to modules (text, image, and video modules) which, respectively, can be joined to aggregates with an overall functionality (an application program) by means of tool modules. The interaction of the modules and the use of the system resources is monitored by special managers (module, pipe, resource, and graphics managers). Module managers ensure that existing modules are available in a sorted tree that can be loaded from a library upon request. The graphics manager visualizes active objects and pipelines them to the user in the desired way.

Imagine a file selector to the file manager existing in Windows, where you see several boxes (directories) with files inside. The viewer looks at one of these directory boxes in the background, resulting in the creation of a pipeline connecting a "selector" with the relevant directory box. A long arm reaches out of the selector and at the end of this arm, there's a tray where the viewer is able to view the table of contents of the selector (equivalent to the selected directory boxes table of contents).

Having read the file names, the viewer turns his view to one of the text viewers at the right part of the screen. Immediately, a text page with the contents of the file where the user had the last view appears. Everything happens interactively without entering any short keys and without clicking the mouse in a non-order-based manner.

In a similar manner, hyperlink connections can be established with a web browser by remaining at the relevant URL link keyword for a short period of time (e.g., 150 ms). The fitting document then appears in the foreground while the other documents are made smaller and shifted to the background. Looking at one of the background documents is enough to fetch it back to the foreground. By changing his viewing angle (which means by moving his head), the viewer is able to look at documents that were previously not visible.

For more information, contact Dr. Siegmund Pastoor at the Heinrich-Hertz Institute, Nachrichtentechnik, Einsteinufer 37, 10587 Berlin, Germany; +49 30/31 00 24 35.; fax +49 30/31 00 22 13.

Alfred Vollmer

Liquid Crystal Displays Expand Their Empire

Recent Technological Developments Broaden The Playing Field As Flat-Panel Displays Look To Replace CRTs.

CHRIS CHINNOCK, Technical Marketing Service, 47 East Rocks Rd., Norfolk, CT 06851; (203) 849-8059; fax (203) 849-8069; e-mail: 76061.3671@compuserve.com.

Liquid crystal displays (LCDs) are the most dominant flat-panel display (FPD) technology available today—and for the foreseeable future. Driven by the demand of the notebook computer market, both thin-film transistor (TFT) and supertwisted nematic (STN) LCDs are showing steady improvement, and manufacturing capacity continues to increase. But LCDs are now moving beyond their traditional notebook base into new applications. Perhaps the biggest "killer app" that LCD manufacturers are eying is replacing the CRT in a wide variety of applications. Eventually, they hope to replace the monitor at your desktop computer.

While LCDs continue to show astonishing growth, it is not without risk. The most fundamental concern is with supply and demand, since this will drive manufacturing investment and profitability for years to come.

One major issue facing FPDs is whether consumers will soon move beyond the 12.1-in. standard notebook size to 13.3-in. displays. If there is rapid movement to this bigger size, it could set off a new spiral of plant investment with a potential price plunge for 12.1-in. displays. This situation is exactly what happened two years ago when consumers moved from 10.4 in. to 12.1 in..

According to Joel Pollack, display marketing manager, Sharp Electronics, Camas, Wash., the debate may already be over. "Initially, I didn't think consumers would want a 13.3-in. display in a notebook because it was becoming too big and heavy, and pricey. But now I think there will be substantial demand for this size," he says. What he sees emerging is perhaps a new class of computer: a hybrid between a desktop and a notebook. Such a computer would be used as a desktop machine, but also would be semiportable for occasional use in another office and at home. Almost all computer makers offer, or are planning, computers for this purpose.

Desktop Monitors

Until recently, LCDs have mostly created new products and product categories such as laptops or palmtops. But they're now beginning to replace CRTs in established product areas. The biggest application is replacement of desktop computer monitors, but it'll be a few years before these flat-panel monitors have much of a volume impact. Before such a monitor reaches the average consumer's desk, it will appear in higher-end applications that can support its initial higher cost—financial trading, medical imaging, transportation, information kiosks, CAD/CAM, and graphic design.

Flat-panel monitors are smaller and less bulky than CRTs *(Table 1)*. But these advantages come with a hefty price tag—they cost two to five times as much as an equivalent CRT. How fast they take off will be driven by pricing and capacity. Pam Himmel, monitor marketing manger, NEC Technologies, Kanagawa, Japan, thinks that "market penetration seems to take off at two times CRT pricing." Others think 1.5 times is the magic number. But no one knows for sure. Compounding the problem is capacity. Most TFT-LCD factories are running full-tilt to meet 12.1-in. demand, and can devote only a small portion of production to larger-sized displays for desktop monitors. Even if huge demand developed overnight, the factories could not supply it. Moreover, next-generation facilities are needed to support even larger substrate sizes for economical production of bigger displays.

TABLE 1: COMPARING FLAT-PANEL DISPLAYS AND CRT MONITORS

Parameter	Typical 15-in. flat-panel monitor	Equivalent 17-in. CRT monitor
Depth	5 in. or 7 in., including base	18 in.
Weight	15 lbs	40 lbs
Power consumption	40 W	125 W
Emissions	Extremely low	EMI inherent with high-voltage electron beams
Cost	STN: \$1500-\$3000 TFT: \$2700-\$5000	\$600-\$900

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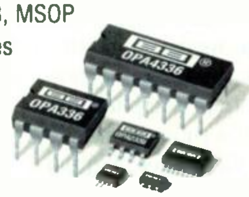

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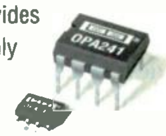

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envelope. For example, the demands of notebooks are producing TFT displays with more pixels. They're thinner, lighter, and less power hungry than their predecessors. For CRT replacement, the push is to much larger and brighter displays with wider viewing angles.

It is perhaps in these non-laptops that show the most interesting advances. Many industry observers now say that some of these displays actually have better performance than CRTs. With contrast ratios exceeding 300:1, brightness of 250 Cd/m^2, and full gamut of colors, they do indeed provide a compelling visual display. Most of these improvements are the result of shrinking transistor and bus geometries (higher aperture ratios); bigger and more efficient backlights; plus advances in display drivers, polarizes, films, and color filters.

The one area where most experts maintain that LCDs are inferior to CRTs is in viewing angles. But that disparity no longer applies. A host of new methods are now available to boost viewing cones to 140°, which is very close to the CRTs' range.

For the laptop, having an active matrix display with a nonsymmetric viewing angle of ±45° left/right, +10° up, and -30° down, is actually sufficient. Such restricted viewing cones are good for privacy, but are generally unacceptable for most CRT replacement applications. In addition, all LCDs suffer image reversals and reductions in contrast, color purity, and brightness as the viewing angle increases. This phenomena is caused primarily by differences in the optical path length as light moves through the LCD structure.

A variety of techniques have been developed to offset this effect. Dual or multidomain techniques, which widen viewing cones to 80° up/down and right/left, are being phased out due to the higher cost and optical artifacts they produce. Optical compensation films are easily bonded to the polarizers, and widen the up/down viewing angle to 90° and right/left viewing angle to 120°. While this solution is effective in expanding viewing in one direction, it's far tougher to use in expanding viewing in all directions

Reducing the thickness of liquid-crystal layer (cell gap) from 4.5 to 5.0 µm to about 4.3 µm helps reduce optical path length differences, improving off-axis contrast ratios with little image reversal. Combining optical compensation with cell-thickness reduction is a popular technique that Dale Maunu, product marketing manger at Mitsubishi, Kanagawa, Japan, says, "will become widespread this year." Up/down viewing improves to about 110°, while left/right viewing can reach 140°.

In addition, two new LCD architectures have been developed that provide outstanding viewing cones. In-plane switching, developed by Hitachi, Ibaraki, Japan, modifies the internal LCD structure to obtain up/down and left/right viewing of 140°. With traditional LCDs, the electrodes that control the orientation of the liquid crystal molecules are fabricated on separate glass substrates and placed on either side of the liquid crystal material. But with in-plane switching, the control electrodes are fabricated on a single glass substrate. While excellent viewing angles are possible, the new electrode structure reduces light throughput, and the liquid crystal switch method slows the speed of response.

Fujitsu, Miyazaki, Japan, has developed a technology called vertically aligned LCD that also can produce up/down and left/right viewing of 140°. To do this, they chose a new liquid crystal material that aligns its molecules vertically and perpendicular to the glass substrates. When voltage is applied, the liquid crystal molecules rotate to nearly parallel to the glass substrates. Fujitsu has combined the technique with a multidomain technology to obtain wide viewing angles, fast response times, and high contrast ratios.

STN Still Has Legs

STN (passive-matrix) LCDs are popular for many applications because they're half the cost of comparable TFT displays. Historically, however, their performance has always needed improvement. But that has changed. Both Sharp and Hitachi are shipping displays that dramatically improve shadowing, contrast, and response speed *(Table 2)*.

TABLE 2: COMPARING BASIC PARAMETERS FOR A 12.1-IN. SVGA COLOR STN DISPLAY

Parameter	Conventional color STN display	SuperClear display (Hitachi)	HC addressing (Sharp)
Contrast ratio	25:1 (60 Hz frame rate)	50:1 (150-Hz frame rate)	40:1 (60-Hz frame rate)
Response speed	300-350 ms	150 ms (90 ms by the fourth quarter 1997)	150 ms (100 ms by the fourth quarter 1997)
Number of colors	16 M*	16 M*	256 k**
Shadowing	6% to 24%	Little to none	<5%
Price	X	1.15X	1.3X

** = Obtained with external graphics controller cards; ** = color-palette capability is built into module.*

Both companies use a technique called multiline addressing. While other companies, such as Motif, Wilsonville, Ore., and Optrex, Tokyo, Japan, have developed multiline addressing techniques, Sharp and Hitachi demonstrated 12.1-in. SVGA displays at SID '97 that were impressive. The picture is crisp, bright, and able to show windowed videos with little image blurring. While not at the level of current TFT performance, it may be equivalent to where performance was two years ago.

Multiline addressing discards today's way of sequentially addressing rows in the display. Instead, using algorithms and memory, incoming images are analyzed to determine which rows should be updated most frequently. In this way, areas of fast motion are updated more often then areas of little or no motion. This driving-scheme optimization produces a faster speed of response. How these algorithms accomplish this feat is what distinguishes the various multiline addressing approaches from each other.

In addition, improved processing parameters have helped to eliminate shadowing, or crosstalk between adjacent rows. Contrast has been improved through thinner cell gaps, compensation films, and better drive techniques.

These achievement milestones are significant because it breaks through a performance wall which has held STNs at about 10 to 11 in. and VGA resolution. Now, 17-in. XGA STN displays are available, but multiline addressing techniques only have been used on 12.1-in. displays so far. Expect to see them extended to larger displays very soon, however. These improvements will extend the life of STN for quite some time.

Even more important perhaps, now

STNs can be incorporated into desktop monitors at much lower price points with acceptable performance. STN factories don't face the same demands as TFT factories, thus they can better respond to increased demand.

Low-Temp. Polysilicon Ready

While CRTs are still used in some projection products, they're rapidly being displaced by products that use FPDs. Today, three technologies are in use for flat-panel-projection products: amorphous silicon, high-temperature polysilicon, and digital micromirrors. But an emerging technology, low-temperature polysilicon, soon may change the dynamics of this market

Overhead panel products are paper-sized (8.5 in. by 11 in.) projection devices meant to be used with a conventional overhead projector. While such products were early flat-panel leaders, their popularity is now fading in favor of more integrated systems. Integrated projectors include their own light source and optics, and produce a much better image.

For integrated projectors, both amorphous silicon and polysilicon-active-matrix LCDs are commonly used. Sharp, for example, is a supplier of amorphous silicon 6.4-in.-diagonal projection displays with VGA and SVGA resolution. Amorphous silicon panels are made with the same process used to make laptop displays. They're bigger than polysilicon panels, and require interconnection of the off-screen driving electronics.

Polysilicon has higher electrical characteristics than amorphous silicon. These traits allow fabrication of smaller on-screen transistors and driver electronics all on the same substrate. The benefit is a more integrated display that also can enable smaller, brighter, and lighter projectors. The trade-off is that expensive and small-diameter quartz substrates must be used, limiting economies of scale and keeping prices high. Primary suppliers such as Sony, Kanagwa, Japan; Seiko-Epson, Nagano, Japan; and Sarif, Vancouver, Wash., offer VGA and SVGA products in the 2-in to 5-in size range. Polysilicon products also are used in camcorder viewfinders and in head-mounted displays, such as virtual-reality gaming.

High-temperature polysilicon processing actually converts amorphous silicon to polysilicon in an oven. But new laser-conversion techniques allow lower processing temperatures and thus, the use of traditional glass substrates. This trend will help lower costs by 35% to 40%, and allow much larger polysilicon displays to be produced.

Most vendors seem to be sticking with smaller-sized, low-temperature poly displays to start. Sharp and Seiko-Epson are sticking with projection products, Sanyo, Gifu, Japan, is eying the camcorder market, and Sony is planning a joint-manufacturing venture that would target the automotive industry, But Toshiba, Yokohama, Japan, has announced it will develop large diagonal displays using the technology. According to Sharp's Pollack, "We are probably now on the verge of finally seeing volume production of low-temperature polysilicon products." Look for the company to begin sampling displays before the end of the year.

Virtual Displays

Significant, and perhaps, revolutionary progress also is being made on new technologies that will produce virtual displays *(Table 3)*. The idea is to use optical magnification to produce an image that appears bigger and farther away than it actually is. Head-mounted devices (HMDs) for gaming and monitors for wearing computers (used in maintenance and inspection applications) are typical virtual displays. A head-mounted monitor, for example, may use a tiny 1-in. display that's within an inch or two of the eye, but the image could look like a desktop monitor at arm's length.

But these devices have not fared well in the market. HMD manufacturers Virtual Vision, Redmond, Wash., Virtual I/O, Seattle, Wash., and Forte, Rochester, N.Y., have all fallen by the wayside. The problem, according to Glen Kepthart, vice president of marketing for display products at Kopin, Taunton, Mass., is that "development of content has been slow, resolutions have been poor, and price points too high."

Nevertheless, big things are happening in virtual displays. For example, new technologies are emerging that address performance and, hopefully, price issues. This new crop of displays boost pixel densities up to a whopping 2500 lines/in. In addition, new market opportunities are being explored-mail/fax viewers, web phones, digital cameras, smart-card readers, and DVD viewers.

Kopin, DisplayTech, Longmont, Colo., and Siliscape, Palo Alto, Calif., are all introducing new LCD technologies that have impressive pixel density in very small packages. For example, DisplayTech's device features 640 by 480 pixels at about 2000 lines/in., while Kopin's CyberDisplay features 320 by 240 pixels at 1700 lines/in., with 2500 lines/in. planned by the end of the year.

Siliscape, a Silicon Valley start-up, plans to sample their new miniature display soon. The SVGA device features a 2500 dot/in. resolution, and is packaged with a compound optical system that's only 0.81 in. by 1.19 in. by 0.44 in. "We have no problem showing 10-point text on our displays," says Alfred Hildebrand, Siliscape's president and CEO.

Kopin's LCD technology fabricates the electronics in silicon at a traditional

TABLE 3: TECHNOLOGIES VYING FOR USE IN PRODUCTS WITH VIRTUAL DISPLAYS

Company	Technology	Resolution and color	Diagonal size	Deliver time frame
Siliscape	LCD on silicon	800 by 800 pixels Color	0.36 in.	Sampling mid '97
Kopin	LCD on glass with lift-off silicon electronics	320 by 240 pixles Amber	0.24 in.	Sampling now
Displaytech	Ferro-electric LCD on silicon	640 by 480 pixels Color	0.4 in.	Sampling now
Motorola	GaAs LED array	240 by 144 pixels Amber	Not available	Sampling now
Planar	Active-matrix electroluminescent display on silicon	640 by 480 pixels Yellow	0.76 in.	Sampling now
Reflection Technology	Scanned linear array of LEDs	864 by 256 pixels Red	Not applicable	In production

foundry then transfers them to glass. Traditional TN liquid crystal is then used to produce a transmissive LCD assembly. Color devices are obtained by using red, green, and blue color filters, which reduce the pixel count by 33%.

Both Siliscape and DisplayTech produce color images using field sequential techniques, whereby red, green, and blue LEDs are used to sequentially illuminate the display at about 180 frames/s. Both also feature a silicon electronics substrate upon which a reflective layer and liquid-crystal material are added, so the display operates in the reflective mode. DisplayTech uses a ferro-electric liquid crystal, whereas Siliscape uses a polymer-dispersed liquid crystal.

Planar America, Beaverton, Ore., also is sampling a miniature display based on electroluminescent technology. Here, yellow-green phosphors are deposited on top of an active matrix fabricated in silicon. Applying voltage causes the phosphors to emit their own light. Densities up to 1000 lines/in. are possible today, with 2000 lines/in. expected by end of the year.

An alternative approach to virtual displays is being pursued by both Motorola, Tempe, Ariz., and Reflection Technologies, Waltham, Mass. Both use arrays of LEDs to produce the image. Reflection Technologies scans a linear array of LEDs to produce an image suitable for displaying faxes, but at much lower resolution than alternative technologies They soon hope to be able to scan red, green, and blue LEDs to produce a full-color image.

Motorola is now qualifying a manufacturing line that will produce their Virtuo Vue display. This display consists of a 2D array of LEDs, and optics, producing a virtual image that's equivalent of a 17-in. monitor. The GaAs LEDs are arranged in a 240-by-144 pixel matrix that produces an amber image.

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HOW VALUABLE	CIRCLE
HIGHLY	525
MODERATELY	526
SLIGHTLY	527

Which Technology Will Make Digital TV A Household Name?

CRT, Plasma, And Liquid-Crystal Display Technologies All Are In The Running For Use In HDTV-Based Applications.

W. K. BOHANNON, Manx Research, 2060 Ridgecrest Pl., Escondido, CA 92025; (619) 735-9678.

What will digital television (DTV) look like? The PC powerhouses would like DTV to have a PC monitor with a 4:3 aspect ratio and square pixels, while Hollywood wants DTV to display 1920-by-1080-resolution images in a 16-by-9 letterbox, progressive or interlaced SMPTE 274M high-definition production standard format.

For now, the next big revolution in home-TV technology is coming to you digitally, by way of recent negotiations between the broadcast industry and the FCC. Exactly what digital TV will look like when it arrives is still open to discussion. Many expect DTV to look more like a bright, high-resolution computer display than today's murky, low-resolution TV sets. The big question is: What kind of technology will be used?

At the last Comdex show in Las Vegas, Nev., the first set-top Internet boxes were displayed. These set-top boxes and wide-screen TVs are not DTV-compatible, but they are indicative of one direction that DTV might be headed toward—couch potato net-surfing. The set-top boxes allow the user to connect via modem to the Internet, and display the information on a standard or wide-aspect-ratio TV set.

In another direction, the convergence of computers and TV, and the passage of new DTV standards this past December has brought DTV one step closer. At the most recent National Association of Broadcasters (NAB) show, for example, the first major exhibition of a local DTV broadcast with programming via satellite relay from WHD-TV, the model HDTV station in Washington DC, was demonstrated. While the DTV images looked nice, exactly how DTV will be implemented for U.S. homes has yet to be decided—despite the fact that full-scale DTV broadcasts are supposed to happen within the next 18 months in the largest American cities.

Compaq Computer, Microsoft, and Intel recently announced an agreement to work together as the "DTV team." This team will help set the kind of standards needed to implement DTV on PCs, as well as create a much closer convergence between TVs and PCs. The PC-DTV team hopes to quickly get a wide range of hybrid PC/TVs and digital-TV appliances running with 4:3 aspect ratio SDTV-like signals.

Several video resolutions reside within the multimode plan the PC-DTV team wants to implement. In a dual-mode base layer denoted HD0, video-camera-originated material would be shown at 704-by-480 pixels, with film-originated material shown at the SMPTE 1280-by-720 resolution (16:9 aspect ratio). After a few years and t[illegible] evitable advances in technology, th[illegible] DTV team would allow the base lay[illegible] move up to the full 1920-by[illegible] SMPTE progressive resolution [illegible] 16:9 aspect ratio. The television indu[illegible] is not very receptive to the PC-DT[illegible] group since PC people seem to be sticking close to a 4:3 aspect ratio. The PC industry wants square pixels while the TV industry wants odd-shaped pixels in a 16:9 aspect ratio or whatever aspect and resolution they decide to broadcast.

At any rate, DTV will require a lot of high-speed hardware just to decode and prepare for a display device. And whether or not HD0 is 4 by 3 or 16 by 9, it is not a slow standard, since a full-capability decoder would need a 22-Mpixel/s data rate. The full version of true high-definition TV, the HD2 mode, wou[illegible] quire a 124-Mpixel/s decoder. B[illegible]

1. Sharp's low-cost LCD monitor with STN LCD improvements is expected to capture a large share of the emerging flat-panel desktop market. It's being considered for PC-TV applications.

cording to Bob Sterns, senior vice president of technology and corporate development at Compaq, by using the PC-TV team's base-layer HD0 approach and the current generation of video-decompression and display (4 by 3) hardware, the initial digital TV sets can be offered at a price point close to today's analog sets. Sterns says that "the incremental cost of adding DTV reception to a PC will likely be as little as $100."

A study entitled "Consumer DTV Screening Survey," done by Systems Research Corp., Rochelle Park, N.J., for Harris Corp., Melbourne, Fla., indicates that many people would not pay more than a $1000 differential for HDTV over conventional sets, and a large percentage (23%) don't want to pay anything more than the cost of a standard TV set. Clearly this kind of low price point for a higher-resolution display can only be reached by CRT-based TV sets and PC monitors in the near term. Within a few years though, perhaps another technology could provide a reasonable alternative. Regardless of the lack of signal format consensus, the PC-DTV crowd is not going to wait.

Intel and Music Television (MTV) are creating TVs out of PCs with today's technology by launching a new programming system called "Intercast". This creation, which brings TV programming and web content together, allows "intercast-enhanced" Pentium PC users to interact with the broadcast. According to Ron Whittier, senior vice president and general manager of Intel's Content Group, "Intercast Jam on MTV" is music video for the PC generation. It shows that "the PC is the receiver of digital broadcasting in the future," says Whittier.

On the other side of the picture, the cable-TV industry is moving quickly to bring high-speed Internet access through local cable providers, in effect trying to turn a TV set into a PC monitor or vice versa. In selected areas, a 27-Mbit digital channel can be tuned in, allowing channel surfers to drop out of TV-land and connect to the Internet digitally.

Currently, the 27-Mbit/s signal is limited by a single 10-Mbaud Ethernet connection to the PC in the cable "SurfBoard" manufactured by the San Diego, Calif.-based company Next Level Systems. However, when the complete system is up to speed and PCI cards (or set-top boxes) with dual-tuners capable of tuning to both MTV and the 27-Mbaud Internet channel are available, users should be able to fully interact, at high speed, with anything they see on MTV.

2. Genesis Microchip's HDTV plasma chip set utilizes a Fire Wire interface and offers a potential solution to the problem of digitally interfacing to a TV for digital TV (DTV) applications.

According to Robert Rast, GI's HDTV spokesman, the existing GI cable-TV set-top boxes also can be used to bring a full-resolution DTV signal into the home since the compressed DTV signals only need about 18 Mbits/s. However, there is no agreed-upon digital interface to the TV. Some consumer-electronics manufacturers would like to see a Fire Wire interface between the set-top box and the DTV. But, according to Genesis Microchip's Jordon Duval, who recently demonstrated a wide, HDTV-like image with Genesis's scan conversion chips on a Fujitsu plasma panel, the Fire Wire interface chips are too expensive for consumer TV. Duval expects that the lower-cost, low-voltage differential signal (LVDS) interface standard that Genesis uses will be adopted for home DTVs.

Display Technology Options

Given the unpredictable future of digital television and personal computers, what kind of displays will be available to fully utilize DTV or PCTV technology? Even if the battle between Silicon Valley and Hollywood forces the consumer to choose between a digital TV set in 16-by-9 or a PCTV set with a 4:3 aspect ratio, it is clear that higher resolutions are necessary. And, regardless of the type of display device, certain interface issues will have to be addressed. Very few of the existing display devices can sync up to a full-resolution or even half-resolution, interlaced DTV signal. Only some of the very expensive, high-end CRT projectors from Sony, NEC, and others can operate at the required SMPTE signal resolutions. But if a general-purpose interface is developed, there are many display devices that will have enough resolution.

Matsushita Electronics recently spotlighted a 17-in. SXGA, 1280-by-1024 CRT monitor with a shortened tube length capable of providing crisp, clear images at higher resolutions. Utilizing a 100° deflection angle, the CRT has approximately the same depth as a 14-in. 90° CRT. Once on the market, it will enable 4:3-aspect PCTV displays to be offered at low cost with a smaller footprint.

Addressing an even closer convergence of PC and TV, Sony has developed a 24-in. Trinitron CRT with a 16:10 aspect ratio and a 1920-by-1200-pixel line resolution targeted at the computer market. Even though the computer industry seems to like 4: 3 aspect ratios, Sony thinks that a double-page, 0.26-to-0.29-mm-dot-pitch display with good brightness (95 Cd/mm^2) and contrast will be popular. In addition, the high-resolution display will do a great job of showing letterbox movies and Internet graphics in the spare pixels along the top and bottom of the screen.

By comparison, Hitachi has developed a 19-in. monitor for computer applications. The monitor, capable of up to 1600-by-1200-pixel resolution, provides the large screen size necessary for high resolution, yet avoids the large size and high cost associated with 21-in. computer monitors. Hitachi's monitor, while not quite fitting full SMPTE 274M signals at 1920 by 1080 pixels, will certainly do a good job with the 1280-by-720-pixel SMPTE standard at a 16:9 aspect ratio. The company also has developed a 27-in. SVGA 800-by-600-pixel-resolution CRT for DTV or PCTV users. This 4:3-aspect-ratio unit, due to be announced during the fall Comdex, will be "competitively priced." Hitachi supposedly has a 30-in. version under development, also with a 4:3 aspect ratio.

LCD technology, in the direct-view TFT category, is still not cheap. Nor is it seamlessly multisync like a CRT. Although the leading manufacturers are gearing up to make millions of 13- to 15-in. full-color TFTs at 1024-by-768- or 1280-by-1024-pixel resolution, don't expect to see any large-size LCDs inexpensive enough for home use within the 18-month time the broadcast industry promised to begin DTV. But if they're a little expensive, the best LCD monitors, such as NEC's 20-in. 1600-by-1200-pixel UXGA TFT, are looking better than CRTs. One of the benefits of NEC's LCD is that because it has a digital matrix of pixels, it doesn't have to face modulation transfer function (MTF) issues that usually limit a CRT to lower contrast and brightness at higher resolutions.

Sharp, has recently announced a newer, low-cost version of its very-high-performance, passive-matrix STN LCD *(Fig.1)*. These products called High Contrast Addressing (HCA) use a special multiplexed addressing scheme to achieve a high contrast ratio. According to Sharp, their approach is not the usual static active addressing scheme proposed by others to achieve better images on STN LCDs. Sharp supposedly still uses ortho-normal functions for the rows and columns, but also "looks ahead"—examines the image to be displayed and then generates the optimal row vectors in its multiline drive scheme depending upon the image content. Because they are not limited to a fixed-number-of-rows-at-a-time generator, Sharp is able to compute the optimal row functions for any image.

Sharp has a number of other display products on the market, including a 12.1-in SVGA STN that promises to cost half the price of a TFT, as well as 13.8-, 15-, and 17-in. XGA resolution, high-performance STN LCDs. There certainly is the potential for Sharp to be selling a 15-in. STN monitor for about $1500 in the near term. This price is about twice the cost of a comparative 17-in. CRT monitor, but if the application requires a much smaller footprint, reduced emissions and lower power consumption, then an LCD monitor is probably a good deal. Even though Sharp's HCA technology has considerable promise, the STN LCD's response time is too slow in some designs. On the bigger panels, Sharp quotes a 300-ms response time, twice that of the 12.1-in.'s 150-ms response.

Sharp also has 20- and 40-in. TFT LCDs. The 20-in. TFT has a resolution of 1280 by 1024 pixels with a 0.31-mm dot pitch, which is fine for the lower-resolution SMPTE standard. The TFT LCD's display looks great given Sharp's super-high aperture ratio and wide viewing angle. The 40-in. TFT only has SVGA and 800-by-600-pixel resolution. It also has a huge 1-mm dot pitch, and would be able to show the lowest resolution ITU-format DTV standard, but it doesn't look very competitive.

If the 20-in and bigger direct-view LCDs would drive the cost of a DTV set way over $10,000, what about rear-screen-projection-LCD technology? A lot of the bigger TV sets today are rear-screen CRT units. Sony, for example, showed two models of LCD rear-projection sets at the Japan Electronics show late last year. One was a 37-in., 30-kg model with or without a multiple-subnyquist-encoding (MUSE) HDTV decoder, and the other was a 50-in., 43-kg model with a MUSE decoder. Both of the two 16:9-aspect-ratio TV sets can be powered by just one of Sony's 1.43-in. 1600-by 480-pixel-resolution LCDs, or by a three-panel engine based on 1.35-in. 1068 by 480 LCDs.

The one-panel rear-screen projector does not use color filters, relying instead on a three-panel staggered-dichotic mirror arrangement with a micro lens on the LCD panel. The design results in bright saturated colors and low cost—about one-half the cost of the three-panel set. Both the three-panel and the one-panel sets exhibit the same brightness and use the same 100-W Philips lamp. The one-panel system has slightly better blues than the three-panel system, however the three-panel system gives better skin tones. Production of the one-panel 50-in. version will start in the summer. Expect to see a 50-in. (one panel) set selling for less than $2000, after discounting.

Toshiba leapt into the LCD projection-TV market with a 40-in. rear screen. The unit, which is 100-cm wide by 121.5-cm high and 38-cm deep, weighs only 35 kg. The set fits into corners where a 29-in. CRT TV can't. Like the Sony rear-screen TVs, Toshiba's set is a one-panel LCD unit, but it's powered by a 250-W metal-halide lamp instead of Sony's 100-W lamp. It is composed of a custom 5-in. LCD panel with 1,230,000 pixels (approximately 854 by 480 by RGB) in a 16:9 aspect ratio. The resolution of the LCD allows Toshiba to display VGA, 640-by-480-pixel images at a 4:3 aspect ratio, without losing any information.

Other Promising Options

Japan's HDTV signals are vastly different from the U.S.'s because the MUSE standard needs an 8.1-MHz analog baseband signal whereas the U.S.'s DTV signal scheme is all digital trellis-coded signal within a 6-MHz bandwidth. Japanese HDTV signals have 1035 active lines with a 2:1 interlace that can be easily converted by 7/15-line sampling to 483 lines. A 480-line LCD easily accommodates the 483-line HDTV decoded signal as well as 4:3-aspect-ratio computer signals. In the Japanese LCD rear projectors currently exhibited, the analog video containing the horizontal line data is re-sampled at a clock rate equivalent to the LCD's pixels-per-line count.

The U.S. DTV 1920-by-1080-pixel resolution picture signal can be either interlaced or progressively scanned. Therefore, the 2:1 interlaced DTV signal can be reduced to two 540-line images, assuming that one keeps to the proposed 1080 active-lines per frame scheme. If an LCD rear-screen projector manufacturer wanted to quickly convert the U.S. DTV signals to run on the current crop of Japanese 16:9-aspect-ratio LCDs, then each interlaced DTV field would have to be further decimated to fit onto 480 lines. The required amount of resizing to reduce a 540-line field to a 480-line field is relatively minimal. The existing Genesis Microchip low-cost image-scaling chips have demonstrated they are quite capable of providing the resizing *(Fig. 2)*.

If a 40- to 50-in. 16:9-aspect-ratio TV set that directly interfaces with your favorite game or PC is too large for your living room, then how about a plasma display? It offers the same screen size in an even thinner, up-against-the-wall

3. Encapsulated color gives NEC's 42-in. 853-by-480-pixel plasma-panel display a brightness of 200 Cd/m^2. To produce colors, each pixel has a tiny color filter, much like an LCD.

package. The downside is that plasma displays are just beginning to ship, and are not cheap enough for general home use. Among the current, newly announced plasma-display products in Japan are Fujitsu's 16:9, 42-in. Home Theater set and Mitsubishi's 40-in. set.

NEC recently showed a 42-in. 853-by-480-pixel plasma-display unit *(Fig. 3)*. The set boasts high brightness (200 Cd/m^2) as well as good colors, due to NEC's encapsulated-color-filter technology. Instead of relying exclusively on red, green, and blue light-emitting phosphors to produce colors, each pixel has a tiny color filter, much like an LCD.

NEC's next step is to make a 51- or 52-in. plasma display device, in 16 by 9 format. They are concentrating on the HDTV arena for now, but may make a 4:3-aspect-ratio high-resolution version. Clearly, the same kind of resizing necessary for the LCD devices could be done for 480-line plasma displays—something that an NEC spokesperson said was on their DTV road map. Plasma technology would certainly be a good choice for wide-format DTV images, but at 480 lines the resolution is a little low. Moving to a design with more lines would make a better image, but that would require higher horizontal resolution, something that today's plasma technology has a hard time achieving.

At any resolution, the price of plasma displays is way above the mythical $100 per diagonal inch that plasma proponents like to use as a target. Even that price is much higher than the $40 per inch price typical of CRT rear-projection displays. Plasma-display technology cost may be high today, but one industry leader says that within five to six years they expect to see plasma panels offered in the $60 to $70 per diagonal inch range. That price point may place a 40-in. plasma set within the reach of some DTV consumers; about $2500 after 2003. The $40/in. price is one that Sony can probably hit with an LCD rear-projection set, however that price is based on 480-line, high-temperature polysilicon TFTs.

Fortunately for LCD manufacturers, making low-cost 1024-by-768-pixel or even higher-resolution 1.3- to 1.8-in. TFT LCDs in a variety of formats is not an issue. It is fully expected that consumers will be able to choose between low-cost, direct-view CRTs, rear-projection CRTs and rear-projection LCD TV sets in wide formats before Hollywood and Silicon Valley ever resolve their differences.

William Bohannon is chief scientist at Manx Research. He has more than 25 years of experience in the computer and projector industry. As chief scientist for Display Products at Proxima Corp. from 1989-1994, he developed important business relationships with several Japanese laboratories and companies. His career also includes positions at TRW, Hughes Aircraft, and Kappa Systems.

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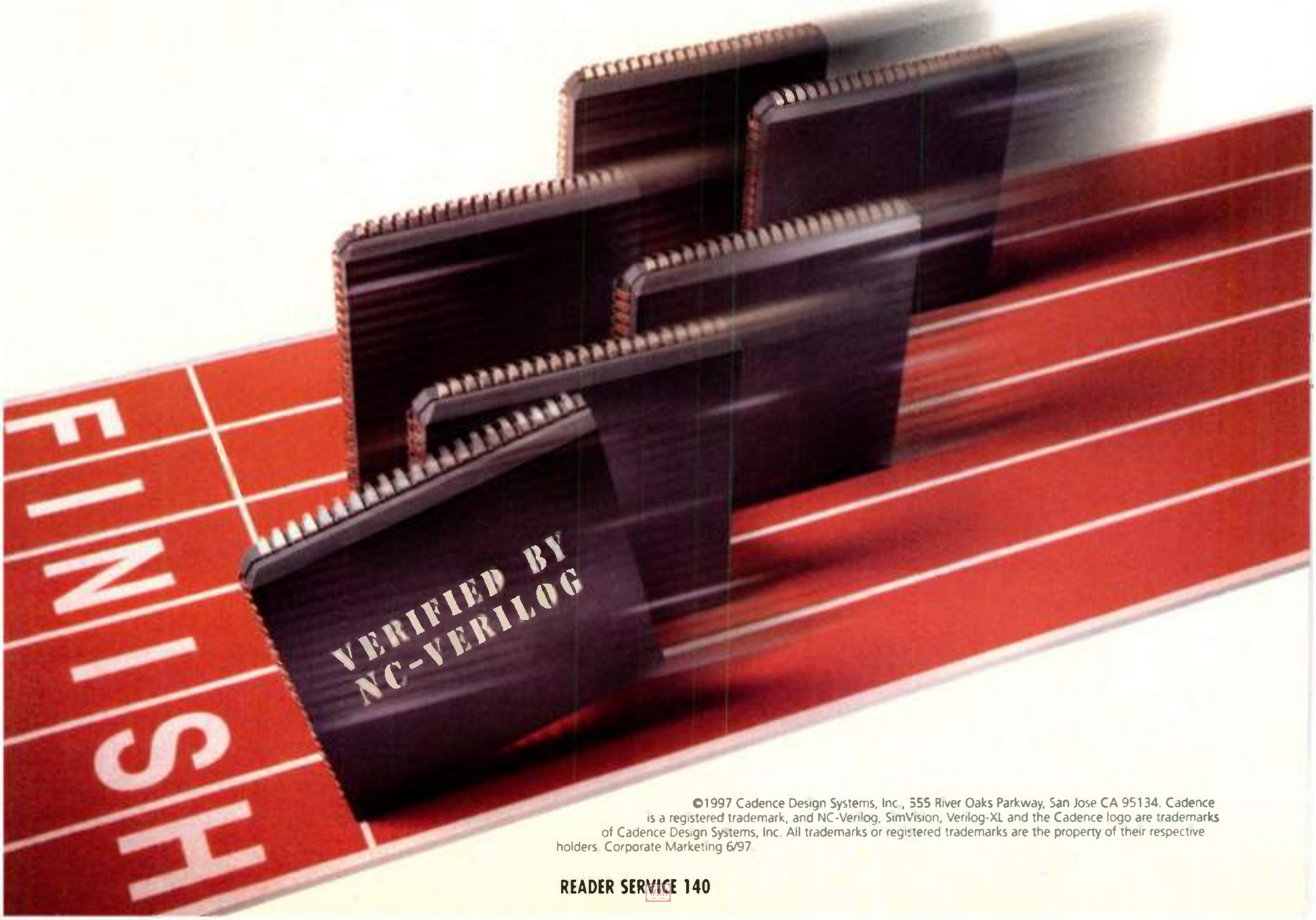

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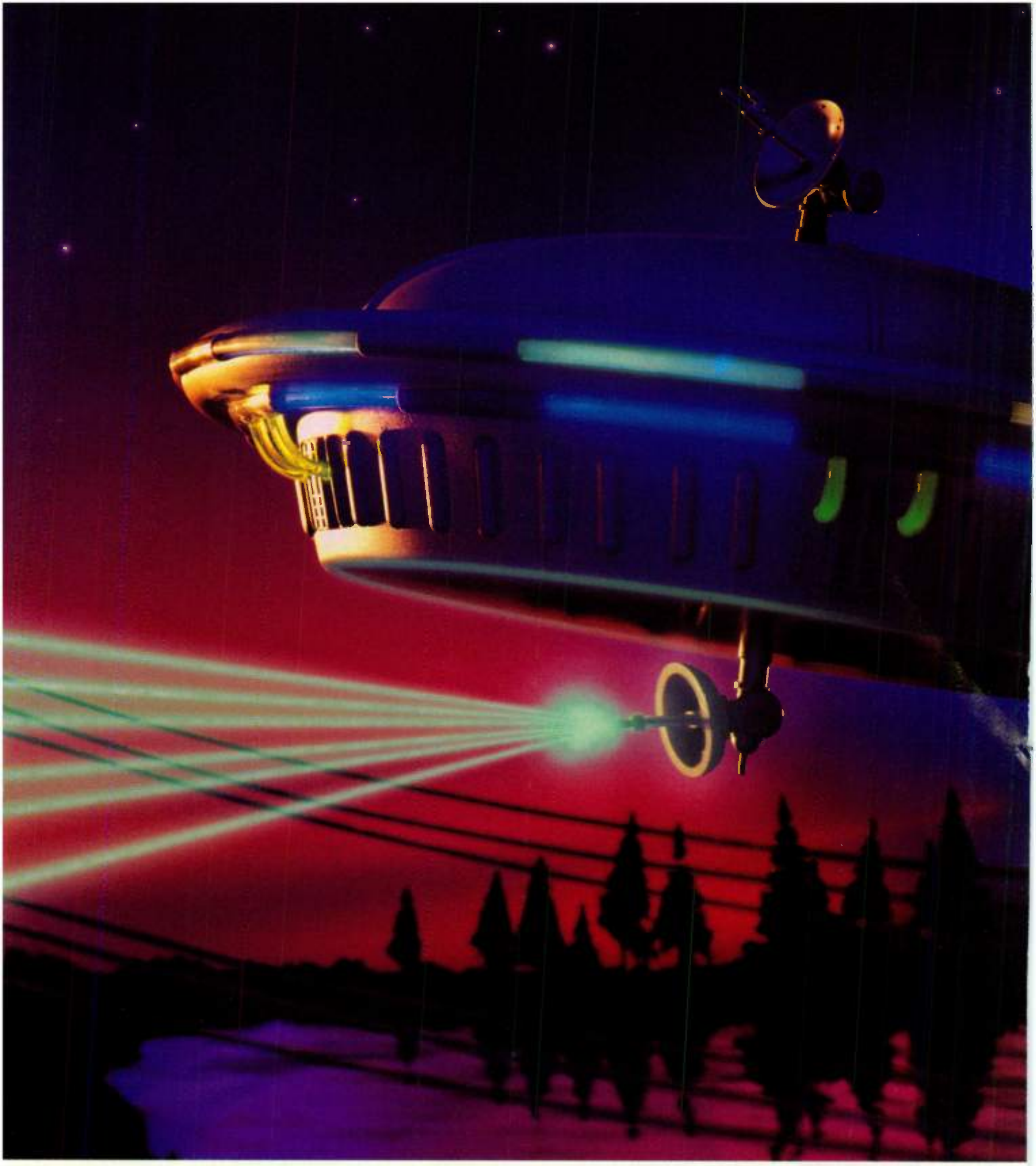

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In many PC system design camps, engineers are under a false assumption that full-motion 30 frames/s provides the acceptable video quality for the next generations of consumer electronics systems and entertainment PCs. However, there's considerably more than meets the eye in this particular case since there are several key parameters constituting consumer-quality video. Foremost, it demands delivery of sustained and uniform 30-frames/s video. In addition, it requires tear-free delivery, the elimination of so-called interlaced video artifacts, and spatial sampling to maintain the correct aspect ratio for display.

Consumer-Grade Video

MPEG-2 video has four times the resolution of MPEG-1, but it falls short of consumer-quality video when implemented in software-only solutions. Even with multimedia extension (MMX) instruction sets, MPEG-2 software decoders fail to provide the proper levels of video performance. As systems designers move from today's MPEG-2 technology to advanced television or High Definition TV (HDTV), video resolution requirements will be six times that of MPEG-2. As a result, cost-effective, software-only implementations of HDTV will be virtually impossible. Therefore, the astute systems engineer involved with next generations of video design should have a sound understanding of the factors contributing to consumer-quality video.

Under normal circumstances, video frames are delivered at a regular interval. But if there is varying latency between the delivery of frames from the decoding process, the 30 frames/s are delivered at irregular intervals, creating nonuniform delivery which manifests itself in jerky motions. Obviously, this is unacceptable for consumer-quality video.

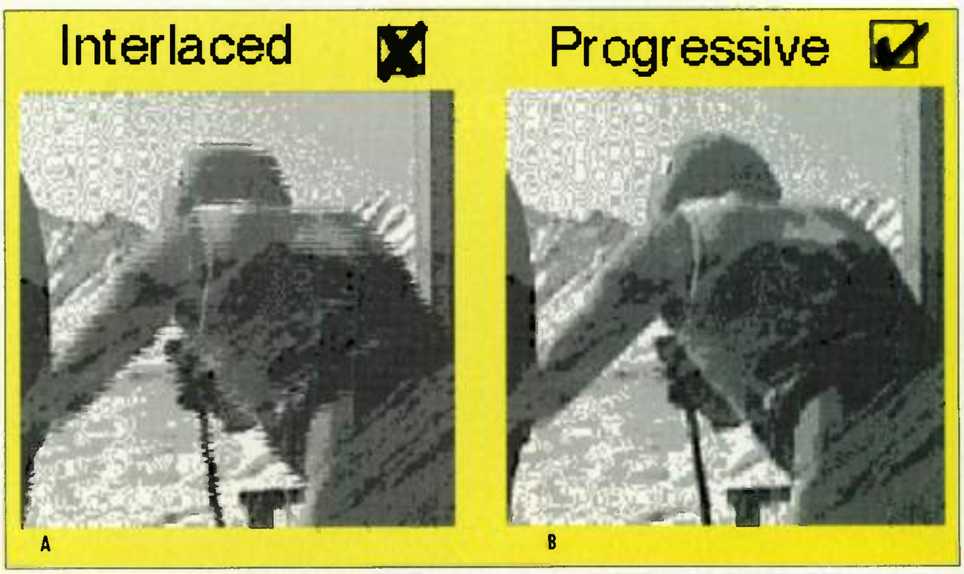
Next in the definition of consumer-quality video, tear-free delivery is required. The term "tear" refers to a displayed video frame that is partially updated, which frequently occurs when decoding is solely performed via software. This artifact results when the display process and the frame update are not synchronized.

Consumer-quality video eliminates these so-called interlaced video artifacts. Most MPEG-2 content generated for TV displays is referred to as interlaced. This means each of the 30 video frames consists of two fields, 16 ms apart. When these two fields are displayed together as a single frame on a PC that utilizes a progressive display, an annoying combing effect or serrated motion created during that 16-ms interval is observed (*Fig. 1*). As a result, TV-interlaced video content must be converted to progressive format to eliminate video artifacts.

Consumer-quality video also requires spatial scaling to maintain the correct aspect ratio for display purposes. For example, decoded resolution of 720-by-480 rectangular pixels need to be spatially scaled to fill up the entire screen of 1024 by 768, 800 by 600, or 640 by 480 square VGA pixels, while maintaining the correct aspect ratio of 4:3. TV video pixels are rectangular while PC VGA pixels are square. Hence, the correct aspect ratio must be factored in to display the decoded video on a PC.

Approaches And Trade-offs

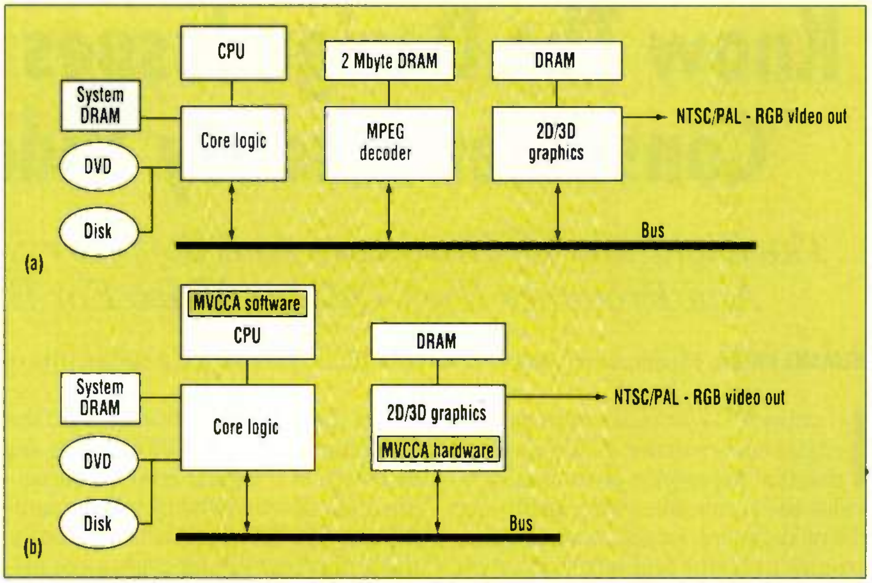
At the outset, there are two design approaches systems engineers must consider for implementing MPEG-2 DVD video decoding in a PC application. One option is to use a complete



1. These two screen shots illustrate the difference between interlaced (a) and noninterlaced (b) video.

hardware-based design. The other is to exploit the present batch of powerful CPUs with MMX and implement both audio and video decoding in software. Given the cost-sensitivity of today's PC consumers, their perception of acceptable price points and, most importantly, consumer demand for high-quality video, both approaches pose unacceptable trade-offs to the systems designer.

The hardware implementation hands the systems engineer a relatively expensive design *(Fig. 2a)*. Presently, the cost of an MPEG-2 audio/video hardware decoder subsystem is in the $150 range. It requires an additional bus slot and involves a cumbersome installation process of connecting additional cables from the hardware video decoder to the graphics controller. In this case, video tearing, poor scaling, and interlaced artifacts limit video quality. Therefore, this option results in an expensive solution that falls short of expected customer-quality video.

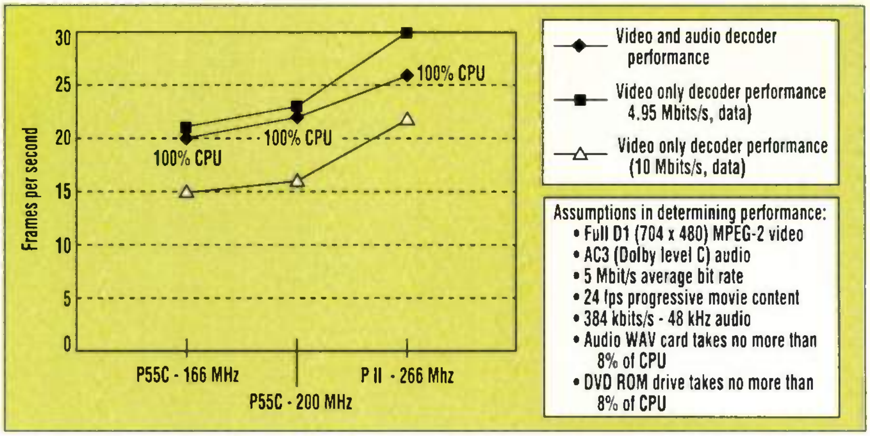


2. MPEG-2 decoding can be accomplished by an all-hardware system (a) or a hybrid architecture where specialized hardware is used only for the most memory-intensive portions of the algorithm (b). In the hybrid approach, other decoding tasks are handled in software by the host CPU.

The software CPU-driven approach, on the other hand, is relatively inexpensive, and no additional bus slots or cables are required. However, it does not produce the level of consumer-quality video for PCs as described earlier. Currently, software-only MPEG-2 designs, even those using a powerful 200-MHz MMX CPU, can only produce 20 to 22 frames/s. In addition, the present crop of graphics controllers are not designed to handle TV interlaced video. As a result, interlaced video artifacts, nonuniform video delivery, video tearing, and poor-quality scaling occur.

Another approach, which is a hybrid of the two discussed above, is to have audio decoding implemented in hardware and video in software. Implementing audio decoding in hardware costs from $10 to $15 and presents several problems that prevent it from being a viable design option. First, hardware audio requires an additional PCI bus slot. Second, audio represents only a small portion of the entire problem of achieving consumer-quality video.

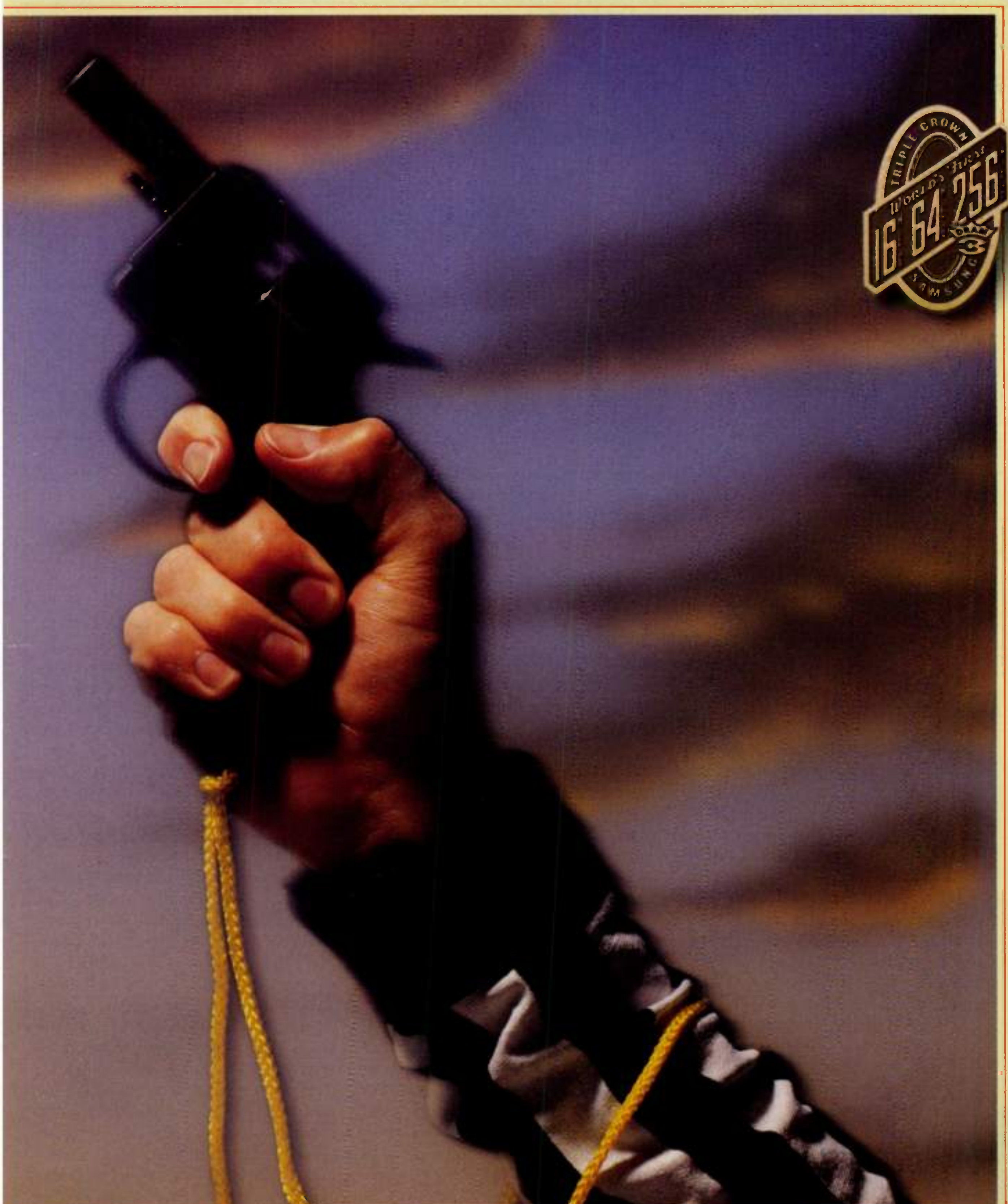
Audio decoding is strictly a compute-bound problem. So, as CPU speed increases, the amount of time required for the audio decoding process goes down linearly. In this case, segmenting audio decoding into hardware and video into software still does not achieve consumer-quality video. It leaves the bulk of the problem of video decoding unresolved.



3. A comparison of video frame-rate performance achieved using variable CPU speeds.

Performance rankings for software-based video/audio decoding, and video-only decoding delivered at variable bit rates, are shown *(Fig. 3)*. Each analysis is based on a 166- and 200-MHz Pentium MMX CPU, and a 266-MHz Pentium II CPU. Utilizing 100% of the CPU power, this software-based video/audio decoder achieves only 20-frames/s video at 166 MHz; 22 frames/s at 200 MHz; and at best, 26 frames/s at 266 MHz.

At 4.85-Mbit/s rates, video-only decode performance is 21 frames/s at 166 MHz, 23 frames/s at 200 MHz, and 30 frames/s at 266 MHz. At 10 Mbits/s, video-only decode performance is 15 frames/s at 166 MHz, 16 frames/s at 200 MHz, and 22 frames/s at 266 MHz.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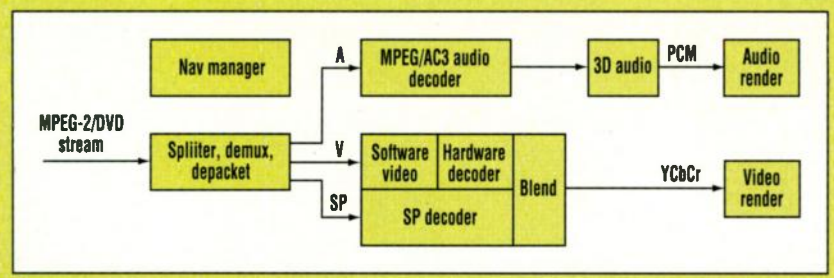


(a)

MVCCA Performance

MPEG-2 video +AC3 audio	MMX-200	MMX-266
Non-MPEG-2 accellerated graphics controller	22 fps (0% CPU spare)	25 fps (0% CPU spare)
With MPEG-2 accellerated graphics controller	30 fps (5% CPU spare)	30 fps (25% CPU spare)

(b)

4. The MVCCA architecture balances multimedia functions between hardware acceleration and software, achieving optimal CPU usage (a). A comparison is shown between video decoding performed with a non-MPEG-2 accelerated graphics controller and decoding with an MPEG-2 (MVCCA) AGC (b).

For 48-kHz, 384-kbit encoded AC-3 audio, decoding performance can be measured as a percentage of CPU utilization involving both floating-point implementation and the MMX instruction set. At 166 MHz, 19% for floating point and 14% for MMX are used; at 200 MHz, 15% and 10% are used, respectively; and with a 266-MHz Pentium II processor, 8% and 9% are used, respectively.

Balanced Partitioning

The system engineer also should take into consideration bottlenecks that involve both compute bandwidth and memory bandwidth limitation. To resolve these issues, a carefully balanced partitioning of processing functions between hardware and software should be utilized. In doing so, the memory bandwidth bottleneck is eliminated when memory-intensive portions of the decoding functions are placed in hardware. This opens up the necessary headroom for processing a sustained 30-frames/s rate. To open up the CPU-to-systems memory bandwidth,the motion compensation part of the MPEG decoding algorithm should be placed in the graphics controller.

High-quality de-interlacing, scaling, and subpicture alpha blending also are implemented in the graphics controllers as part of this balanced hardware/software partitioning. MPEG-2 accelerated graphics controllers are thus created by implementing these functions in silicon *(Fig. 2b)*.

No additional chip or bus slot is required, since motion-compensation logic is embedded in the graphics controller. An additional 2 Mbytes of DRAM required for motion compensation is shared with the graphics-controller frame buffer. Since displayed video is available in the local frame buffer, no additional PCI/AGP (advanced graphics port) bandwidth is required and the tearing artifact is eliminated since both decode and display functions are synchronized.

Several major considerations are involved in moving software functions into hardware. The most important one is that this partitioning be regarded as a system-level architecture, rather than an array of changes. There are such considerations as the optimal transfer of data over the PCI bus or the AGP; minimizing the amount of data copied and reducing the total amount of memory required; ensuring full concurrency between hardware and software; delivering hardware-quality tear-free video; and ensuring that hardware/software partitioning works seamlessly with such Microsoft-defined applications programming interfaces (APIs) as DirectDraw and DirectShow.

A system level architecture that has considerable promise is the Motion Video Collaborative Compression Architecture (MVCCA) developed by Mediamatics *(Fig. 4a)*. Incoming MPEG-2/DVD packetized data consists of audio, video, subpicture graphics and control information. It first goes through the splitter, demultiplexer, and de-packetization. Control data goes to the navigation manager for user-interface purposes.

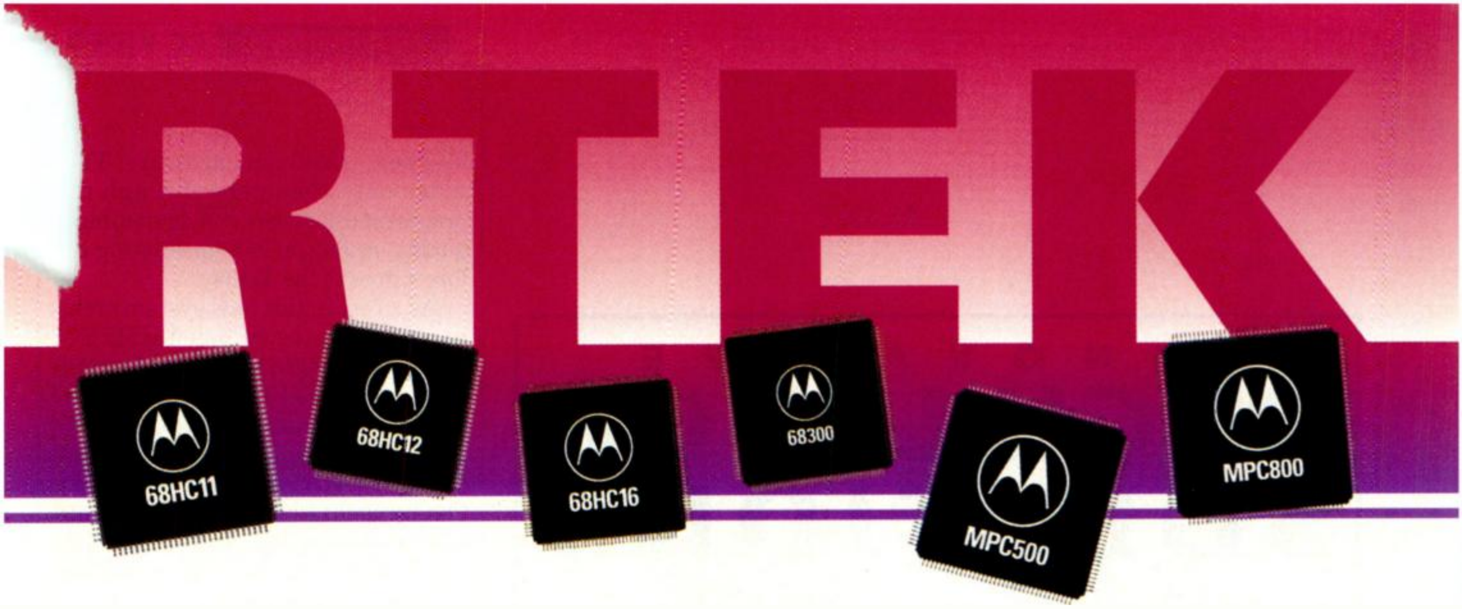
Audio data goes through a software-based audio decoder. In some cases, if a six-channel source is involved and the PC has only two speakers, then the software converts the data from six channels to two by utilizing the 3D audio algorithm. As shown, the video decoder is divided into hardware and software with motion compensation being performed in software. However, blending of subpicture graphics with video is performed in hardware by the graphics controller. The output is then sent to the video-rendering process.

In the video subsection of this architecture, there are different elements associated with decoding the compressed video into a video frame. Here, variable-length decoding (VLD), inverse quantization (IQ), and inverse discrete cosine transform (IDCT) are all performed in software. These functions are compute-bound, rather than memory-bound. As a result, the amount of time required to perform these processes scales linearly with the CPU's processing speed.

Take for example a comparison between a 133-MHz and a 266-MHz MMX CPU. The amount of time required to perform compute-intensive processes such as VLD, IQ, and IDCT on the 266-MHz CPU would be about half that required on 133-MHz CPU. As a result, performance benefits for these types of functions are directly influenced by increased CPU speeds.

However, video decoding functions such as motion compensation and block reconstruction are memory-bound. Due to existing cache subsystem design, these functions inefficiently use available system memory bandwidth. This problem is further aggravated by the inability of memory bandwidth to scale linearly with CPU speeds.

While subpicture decoding is best performed in software, blending of the decoded video frames with the subpicture data, using the subpicture



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blender, is done in hardware. Th video data then goes through t process of color space conversion, hig quality scaling, and de-interlacing b fore it goes to the display.

As a result, this new system architecture defines a new breed of MPEG-2 hardware-based accelerated graphics controllers that include MPEG motion compensation, VGA/2D/3D graphics functions, color space conversion, and subpicture blending. The motion-compensation function interfaces to a PCI bus or AGP and to a memory management unit block, which is part of the graphics controller.

Also, MVCCA utilizes less bandwidth than completely software-based video decoding solutions. Maximum PCI bandwidth is 16.5 Mbytes/s; av age PCI bandwidth is less than Mbytes/s; and system memory us is 1.5 Mbytes. The comparison her between video decoding perforn solely in software and decoding p formed using the MVCCA balanc architecture.

Without an MPEG-2 accelerated graphics controller and a 200-MHz MMX CPU, a PC can only produce 22 frames/s and leaves no CPU power in reserve *(Fig. 4b)*. But with an MPEG-2 accelerated graphics controller, video decoding is at a full 30 frames/s with 5% CPU power left over. With a 266-MHz MMX CPU, the nonaccelerated graphics controller approach yields 25 frames/s and, once again, leaves no spare CPU power. However, MVCC used in a similar set up takes video coding to full 30 frames/s, this ti leaving 25% of the CPU power spare. Utilizing a balanced system chitecture not only delivers consum quality video, but also frees up syste resources so a variety of other applications can run concurrently.

Hemant Bheda is co-founder and vice president of engineering at Mediamatics. He has over ten years experience working in video compression and VLSI architectures. He holds a Master's Degree in electrical engineering from San Diego State University.

HOW VALUABLE	CIRCL
HIGHLY	57
MODERATELY	57
SLIGHTLY	57

Wescon/IC Expo '97 Moves To The Center Of The Action

In Its First Year In Silicon Valley, Wescon/IC Expo Looks At Advances In ICs, Networking, And Communications.

John Novellino

For the first time in Silicon Valley, Wescon/IC Expo 97 will celebrate "Technology on the Move" with a conference schedule emphasizing IC technologies, networking, and wireless communications. Other conference tracks will focus on power management, multimedia, software, and design, test, and manufacturing issues.

The applications conference portion of the show begins on Monday, Nov. 3 with workshops and short courses at the Santa Clara Convention Center. The technical sessions and industry exhibition run Nov. 4-6, with the sessions at Santa Clara and an expected 1400 exhibits at both Santa Clara and the San Jose Convention Center. The second annual IC Expo will consist of a dedicated exhibit area on the Santa Clara show floor where semiconductor manufacturers will display their latest products. Booths numbered 200 to 3000 are at the San Jose site, and booths 5000 to 6000 are at Santa Clara.

Show officials note that more than 80% of attendees commuted to Wescon's former northern California venue at the Mosconi Center in San Francisco from Silicon Valley. As a result, they say, the new dual locations for the 46th Wescon should be more convenient for both attendees and exhibitors. Free shuttle buses will run continuously between the two venues from 8:00 a.m. to 6:00 p.m. Nov. 4-6. Also, attendees will be given free tokens (a different one for each day) that will allow unlimited rides between convention centers on the Silicon Valley light rail system's Guadalupe line.

New at this year's application conference are engineering workshops, half-day events that offer application-specific training from engineers at software, tool, and device technology developers and manufacturers. Additionally, a series of half and full-day short courses provide in-depth information on communications, computer, and microelectronics design applications and solutions. The workshops, short courses, and keynote addresses require additional fees. The technical and plenary sessions and roundtables are free to all attendees.

IC workshops, sessions, and short courses will cover design of regular and digital signal processors, ASICs, and programmable chips; system-on-a-chip integration; and embedded applications. Specific topics include hardware-description languages, high-performance packaging, rapid prototyping, and quality and reliability issues. The communications track is further divided into two areas: networking and wireless. Hot topics in networking include Internet connectivity, CE platforms, MPEG video, and TCP/IP. Wireless is covered in sessions on cellular networks, broadband connectivity, and wireless design tools. MPEG-1 and MPEG-2 standards, image processing, and 3D audio are handled in the multimedia track.

Power topics, which come under the IC technologies track, include regulation and management of battery power. Two sessions in the software track specifically tackle embedded applications. One takes on Java, and the other looks at benchmarking and integration of real-time operating systems. An applications track encompassing design, test, and manufacturing examines is-

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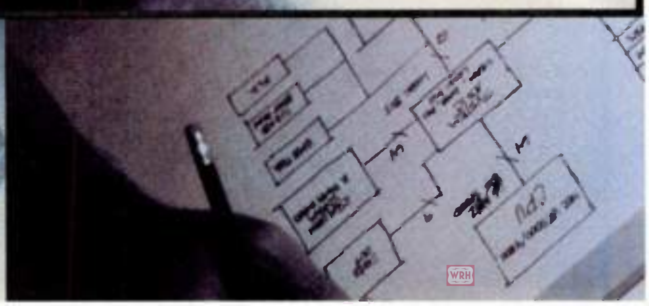

NEC

READER SERVICE 198

sues such as sensing and power control, storage and high-performance I/O devices, and using the world-wide web to cut concept-to-delivery time.

The time and length of the technology sessions vary, so attendees should keep a schedule handy *(see the table)*.

Session S4, "System-on-a-Chip Integration," includes a paper entitled "Core + ASIC Methodology—the Pursuit of System-on-a-Chip," by Ann Marie Rincon, a senior engineer at IBM's Microelectronics Division. Rincon notes that the ability to integrate complete system functionality on one chip is driving a new paradigm in which the focus shifts from gate-level optimization to maximizing functionality and minimizing time-to-market. Critical to getting the most out of such designs is the ability to take full advantage of predesigned cores, but the complexity of these cores can tax the capability of traditional design methods. Challenges include varying interface needs, inconsistent test requirements, limited core porosity, multiple types of cores. Rincon proposes solutions and presents examples of working system-on-a-chip hardware.

A paper entitled "An Intelligent Power-Supply Conditioning System Using an Embedded Microcontroller" looks at how to reproduce the main power source accurately and quickly to ensure uninterruptible power in the event of an outage on the main power supply (Session S17). Charles Melear, manager of advanced microcontroller applications engineering at Motorola Inc., writes that even a few minutes worth of power will allow a computer

WESCON/IC EXPO '97 TECHNICAL SESSIONS

Tuesday, November 4				
Morning	**S1** GPS (Communications) 9:30-11:00	**S3** Multimillion-gate design (IC Technologies/Power Mgmt.) 9:30-10:30	**S4** System-on-a-chip integration (IC Technologies/Power Mgmt.) 10:30-Noon	**S5** Multimedia–Part I (Multimedia) 9:30-11:00
	S7 Debugging tools and techniques (Software) 9:30-11:30	**S8** Software engineering for the computer programmer (Software) 9:30-11:30	**S9** Design/Test/Manufacturing (Design/Test/Manufacturing) 9:30-Noon	
Noon-2:00 p.m.	Keynote 1: Digital Culture–Reinventing business in the networked age			
Afternoon	**S2** Internet appliances/CE platforms (Communications) 1:00-3:00	**S6** Multimedia–Part II (Multimedia) 1:00-2:30		
Wednesday, November 5				
7:15-9:00	Keynote 2: The networked age by design			
Morning	**S11** Wireless general session–Part I (Communications) 9:30-Noon	**S13** New silicon architectures The next wave (IC Technologies/Power Mgmt.) 9:30-11:30	**S14** Microcontrollers (IC Technologies/Power Mgmt.) 9:30-11:30	**S15** Interface solutions for low-voltage applications in desktop and portable systems (IC Technologies/Power Mgmt.) 9:30-11:30
	S19 Java in embedded systems (Software) 9:30-11:30	**S21** Sensing and power control (Design/Test/Manufacturing) 9:30-11:30		
Noon-2:00 p.m.	Keynote 3: The transistor's impact on the electronics industry			
Afternoon	**S12** Wireless general session-Part II (Communications) 1:00-3:30	**S16** Battery power management (IC Technologies/Power Mgmt.) 1:00-2:30	**S17** Power regulation (IC Technologies/Power Mgmt.) 3:00-5:00	**S18** Graphics for multimedia (Multimedia) 2:00-4:30
	S20 Software development General session (Software) 3:00-4:00			
Thursday, November 6				
Morning	**S24** Internet connectivity (Communications) 9:30-11:30	**S25** IC technologies New design processes (IC Technologies/Power Mgmt.) 9:30-10:30	**S26** Embedded applications (IC Technologies/Power Mgmt.) 10:30-11:30	**S27** Benchmarking and integration of embedded real-time operating systems (Software) 9:30-10:30
	S28 Bus implementation issues (Design/Test/Manufacturing) 9:30-11:00	**S29** Storage and high-performance I/O (Design/Test/Manufacturing) 9:30-11:00	**S30** Using electronic engineering databases and the WWW to dramatically reduce the concept-to-delivery cycle (Design/Test/Manufacturing) 9:30-11:30	**S31** IEEE Region 6 student paper contest (Design/Test/Manufacturing) 9:30-Noon

System Automates Testing Of Displacement Force

The Model 921A displacement-force test station can test virtually any component that requires accurate displacement-force measurements such as membrane switches, including polydomes, metal domes, elastomer, and conventional keypads. The system continuously measures contact resistance during testing, and meets ASTM standards.Three operational modes—local, PC, and engineering—are available. In engineering mode, up to 5000 data points are acquired and stored in one test. Users can get test data with a displacement resolution of 0.00254 mm (0.0001 in.). The 921A is useful for first-article product tests, audit testing, engineering investigation, inspection, and life-study testing. When integrated with an automatic feed or x-y positioner, the system can serve as an automated test station for a variety of production applications. The Model 921A's base price is $9500. Delivery is within 30 days of ordering.

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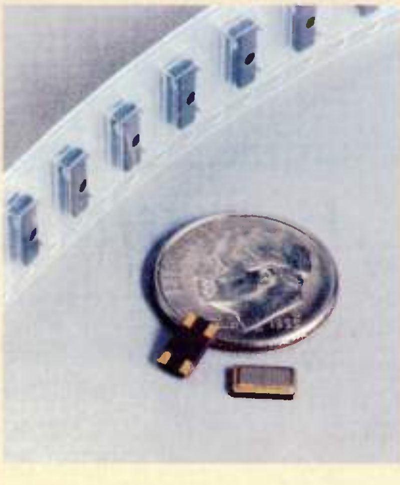
A pair of miniature crystals are aimed at surface-mount applications with limited board space. The ECX-64, a quartz crystal for wireless telecommunication applications, offers low power consumption, tight frequency stability, and high-frequency fundamental capability up to 40.000000 MHz. Overall frequency range is 12.000000 to 100.000000 MHz, with stability of ±4 ppm from –10 to +60°C. The crystal measures 6.0 mm by 3.5 mm by 1.1 mm. The ECX-64 costs $2.00 each in quantities of 1000, $1.50 each for 10,000, and $1.20 each for 100,000. The ECX-3TA tuning fork crystal, which measures 7.3 mm by 4.3 mm by 2.0 mm, is ideal for low-profile applications such as data modems, host adapter cards for PCI, and SCSI interfaces. The device supplies the popular, real-time 32.768000-kHz frequency with extended operating range capabilities of –40° to +80°C. The ECX-3TA costs $0.80 each in quantities of 3000, $0.65 each for 12,000 pieces, and $0.55 each for 102,000.



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Booth 2647

system to save any work in progress and perform an orderly shutdown. The backup supply should allow transactions with serial ports, disk drives, etc. to continue without glitches. Also, undervoltage and overvoltage conditions, which can be disruptive, must be avoided.

Benchmarking is important in any new system, but can be critical for real-time operating systems. In "A Real-World Approach to Benchmarking DSP Real-Time Operating Systems," Elizabeth Keate, a senior application engineer at Spectron Microsystems, discusses key metrics typically used to evaluate RTOS performance (Session S27). According to Keate, many RTOS vendors offer timing information that is intended to provide a first-order indication of overall performance. But, most of this information is based on home-grown benchmarks that portray their products in the best light, and fail to consider the needs of real-world applications. The paper examines some of the shortcomings of traditional benchmarking techniques and proposes an alternative approach.

It seems that the faster memory capabilities grow, the faster the need for bigger and quicker memories grows. The next leap may come from work being done on a content-addressable read-only memory (Carom) being developed under a grant from the U.S. Army. "Carom: A Solid-State Replacement for the CD-ROM," by Klaus Holtz, president of Omni Dimensional Networks, describes a credit-card-size plastic module that may be able to store entire digital movies while wearing a smaller price tag and sporting a smaller footprint than a CD-ROM (Session S29). Holtz says other advantages include all solid-state reading without turntables or lasers, very low power consumption, very fast random access, and no vibration or dirt contamination. The goal is to match the price and data density of a CD-ROM.

The IC technologies track also contains a roundtable discussion on "New Silicon Architectures—The Next Wave" (Session S13). According to the session's description, PC growth has stalled, with the double-digit increases of the early '90s fueled by new users, being replaced by more moderate growth rates driven by upgrades and obsolescence. Roundtable moderator Stephen A. Drukker, president of OPTi Inc., says emerging products like entertainment

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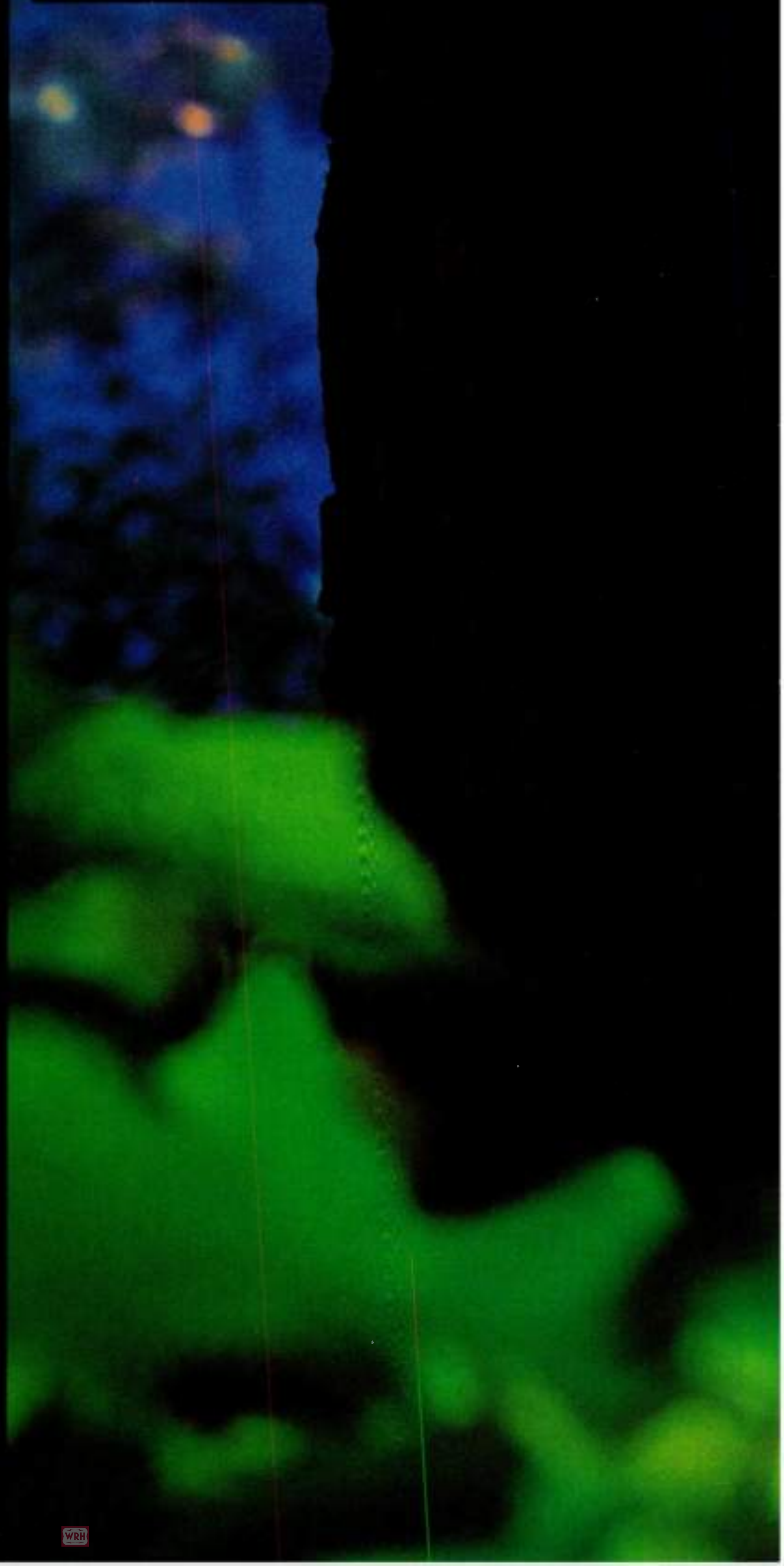

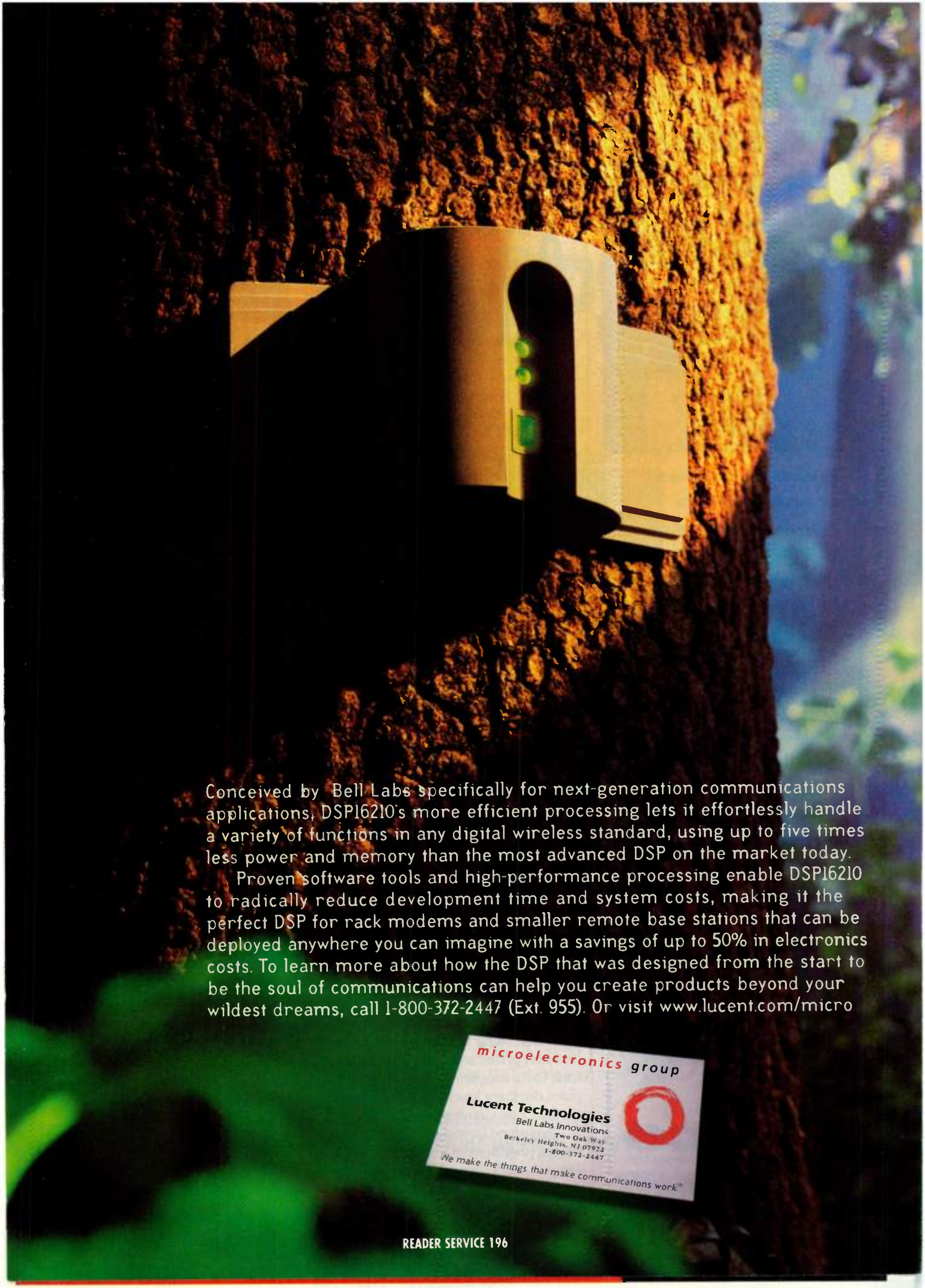
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FEBRUARY 1998

IEEE Applied Power Electronics Conference and Exposition (APEC '98), February 15-19. The Disneyland Hotel, Anaheim, California. Contact Pamela Wagner, Courtesy Associates, 655 15th St., N.W., Suite 300, Washington, DC 20005; (202) 639-4990; fax (202) 347-6109; e-mail: pwagner@courtesyassoc.com.

Conference on Optical Fiber Communication (OFC '98), February 22-27. San Jose Convention Center, San Jose, California. Contact Lisa Myers, OSA Conference Services, 2010 Massachusetts Ave., N.W., Washington, D.C. 20036-1023; (202) 416-1980; fax (202) 416-6100; e-mail: ofc.info@osa.org.

38th Israel Conference on Aerospace Sciences, February 25-26. Tel-Aviv and Haifa. Contact Technion-Israel Institute of Technology, Haifa 32000, Israel; 972-4-8292713; fax, 972-4-8231848; e-mail: alice@aerodyne.technion.ac.il.

MARCH 1998

Sixth Annual Embebbed Systems Conference East, Mar. 31-Apr. 2. Chicago's Navy Pier Festival Hall, Chicago, IL. Contact Miller Freeman Inc., 600 Harrison St., San Francisco, CA 94107; (415) 905-2354; fax (415) 905-2220; Internet: http://www.embedsyscon.com/.

APRIL 1998

Southeastcon '98, Apr. 10-15. Hyatt Regency, Orlando International Airport, Orlando, FL. Contact Parveen Ward, ECE Dept., University of Central Florida, Orlando, FL 32816; (407) 823-2610; fax (407) 823-5835; e-mail: pfw@ece.engr.ucf.edu.

MAY 1998

IEEE International Conference on Evolutionary Computation, May 3-9. Ankorage, Alaska. Contact Patrick K. Simpson, Scientific Fishery Systems Inc., Post Office Box 242065, Anchorage, Alaska 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@akaska.net.

IEEE International Conference on Neural Networks (ICNN '98), May 3-9. Anchorage, Alaska. Contact Patrick K. Simpson, Scientific Fishery Systems Inc., Post Office Box 242065, Anchorage, Alaska 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@akaska.net.

IEEE World Congress on Computational Intelligence, May 3-9. William A. Egan Civic and Convention Center, Anchorage, Alaska. Contact Patrick K. Simpson, Scientific Fishery Systems Inc. Post Office Box 242064, Anchorage, Alaska 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@alaska.net.

Seventh IEEE International Fuzzy Systems Conference, May 3-9. Anchorage, Alaska. Contact Patrick K. Simpson, Scientific Fishery Systems Inc., Post Office Box 242065, Anchorage, Alaska 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@alaska.net.


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IEEE/IAS Industrial & Commercial Power Systems Technical Conference (I&CPS), May 4-7. Edmonton, Alberta, Canada. Contact Marty Bince, Modicon Canada Ltd., 5803 86th St., Edmonton, Alberta T6E 2X4, Canada; (403) 468-6673; fax (403) 468-2925.

IEEE International Conference on Acoustics, Speech & Signal Processing (ICASSP '98), May 12-15. Seattle Convention Center, Seattle, WA. Contact Les E. Atlas, Dept. EE(FT 10), University of Washington, Seattle, WA 98195; (206) 685-1315; fax (206) 543-3842; e-mail: atlas@ee.washington.edu.

JUNE 1998

IEEE/MTT-S International Microwave Symposium (MTT 98), June 7-12. Baltimore Convention Center, Baltimore, MD. Contact Steven Stitzer, Westinghouse Electric Corp., P.O. Box 1521, MS 3T15, Baltimore, MD 21203; (410) 765-7348; fax (410) 993-7747.

USENIX 1998 Technical Conference, June 13-17. Marriott Hotel, New Orleans, LA. Contact USENIX Conference Office, 22672 Lambert Street, Suite 613, Lake Forest, CA 92630; (714) 588-8649; (714) 588-9706; e-mail: conference@usenix.org; Internet: http://www.usenix.org.

JULY 1998

IEEE International Geoscience & Remote Sensing Symposium (IGARSS '98), July 6-10. Sheraton Seattle, WA. Contact Tammy I. Stein, IGARSS Business Office, 2610 Lakeway Dr., Seabrook, TX 77586-1587, (281) 291-9222; fax (281) 291-9224; e-mail: tstein@phoenix.net.

IEEE Power Engineering Society Summer Meeting, July 11-17. Sheraton Hotel, San Diego, California. Contact Terry Snow, San Diego Gas & Electric, P.O. Box 1831, San Diego, California 92112; (619) 696-2780; fax (619) 699-5096.

IEEE Power Engineering Society Summer Meeting, July 12-16. Sheraton San Diego Hotel & Marina, San Diego, California. Contact Terry Snow, San Diego Gas & Electric, Post Office Box 1831, San Diego, California 92112; (619) 696-2780; fax (619) 699-5096; e-mail: t.snow@ieee.org.

SPIE's Annual Meeting & Optical Instrumentation Show, July 19-24. San Diego, CA. Contact SPIE Exhibits Dept., P.O. Box 10, Bellingham, WA 98227-0010; (360) 676-3290; fax (360) 647-1445; e-mail: exhibits@spie.org.

IEEE Nuclear & Space Radiation Effects Conference (NSREC '98), July 20-24. Newport Beach, California. Contact Jim Schwank, Sandia National Laboratories, Post Office Box 5800, MS-1083, Albuquerque, New Mexico 87185-1083; (505) 844-8376; fax (505) 844-2991; e-mail: schwanjr@sandia.gov.

AUGUST 1998

AUTOTESTCON '98, Aug. 24-27. Salt Palace Convention Center, Salt Lake City, UT. Contact Robert Myers, Myers/Smith Inc., 3685 Motor Ave., Suite 240, Los Angeles, CA 90034; (310) 287-1463; fax (310) 287-1851; e-mail: bob.myers@ieee.org.

OCTOBER 1998

IEEE International Conference on Systems, Man, & Cybernetics, Oct. 12-14. Hyatt Regency La Jolla, La Jolla, CA. Contact M.A. Jafari, Dept. of Industrial Engineering, Rutgers University, P.O. Box 909, Piscataway, NJ 08855; (908) 445-3627; (908) 445-5467; e-mail: jafari@gandalf.rutgers.edu.

NOVEMBER 1998

Photonics East & Electronic Imaging International Exhibition, November 1-6. Boston, Massachusetts. Contact SPIE Exhibits Dept., Post Office Box 10, Bellingham, Washington 98227-0010; (360) 676-3290; fax (360) 647-1445; e-mail: exhibits@spie.org.

Voice, Video & Data Communications Conference & Exhibition, November 1-6. Boston, Massachusetts. Contact SPIE Exhibits Dept., Post Office Box 10, Bellingham, Washington 98227-0010; (360) 676-3290; fax (360) 647-1445; e-mail: exhbits@spie.org.

NOVEMBER 1998

IEEE Global Telecommunications Conference (Globecom '98), Nov. 9-13. Sydney, Australia. Contact Sam Reisenfeld, School of Electrical Engineering, University of Technology, Sydney, P.O. Box 123; Broadway, NSW 2007, Australia; +61 2-330-2435; e-mail: samr@trnasmit.ee.uts.edu.au.

LINEAR TECHNOLOGY

DESIGN NOTES

"LCD Bias" and "Backup Supply" Applications for the LT1316 Micropower DC/DC Converter – Design Note 166

Gary Shockey and Jeff Witt

Some step-up DC/DC converter functions require input current limiting because of high source impedance or limited capability of power components. The LT®1316, a micropower step-up DC/DC converter with peak switch current control, meets these needs. The device draws 33μA quiescent current and contains a 0.6Ω, 30V switch that can be programmed for a maximum peak current between 30mA and 600mA with an external resistor. It also has a low-battery detector that remains active in shutdown, where quiescent current drops to 3μA. The two circuit examples below illustrate how the LT1316's current limit function allows realization of difficult converter circuits.

2-Cell, Low Profile LCD Bias Generator Fits in Small Places

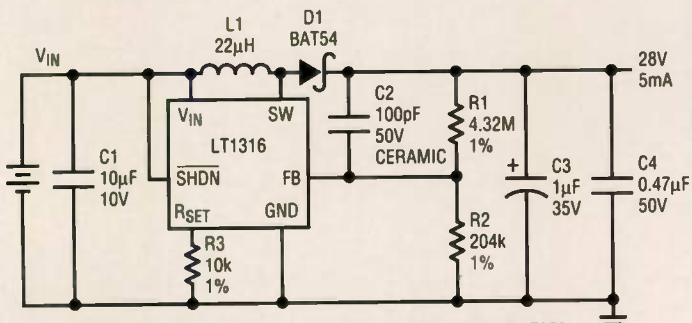
Portable electronic products with LCDs are getting thinner, resulting in severe restrictions on component height. LCD bias generators placed in or near the display housing need to use low profile (under 2mm) components to meet height restrictions. These low profile inductors and capacitors have somewhat higher parasitic resistance than their higher profile equivalents; hence, switching regulator peak current must be controlled to keep the inductor from saturating and to keep output voltage ripple under control. The LT1316, with its programmable current limit function, is ideal for use as an LCD bias generator.

Figure 1's circuit delivers 5mA at up to 28V from a 2-cell battery, using components that are under 2mm high. Peak current is limited to 350mA by 10k resistor R3 at the R_{SET} pin. The parallel combination of a 1μF, 35V tantalum and a 0.47μF, 50V ceramic keep output ripple voltage to 180mV, less than 1% of the output voltage. Output voltage and inductor current waveforms at an input voltage of 2V and load current of 4mA are detailed in Figure 2. The 28V output can be varied by changing the value of R2 or by summing a current into the LT1316 FB pin.

Higher output current can be generated if a higher input supply voltage is available. Table 1 shows output current for supply voltages of 2V, 3.3V and 5V. Up to 20mA at 28V can be generated from a 5V supply. Efficiency using these low profile components is a few points lower than it would be with larger components, but it is still above 74%.

Table 1. Output Current for Input Voltages of 2V, 3.3V and 5V

V_{IN}	L	PEAK CURRENT	R_{SET}	OUTPUT CURRENT
2V	22μH	350mA	10k	5mA
3.3V	22μH	550mA	7.5k	15mA
5V	47μH	350mA	10k	20mA



C1: MURATA GRM235Y5V106Z010
C3: SPRAGUE 592D105X9035B2
C4: MURATA GRM426Y5V474Z050
L1: MURATA LQH3C220K04 0.71Ω DCR

DN166 F01

Figure 1. 2-Cell to 28V Converter for LCD Bias Generators Uses Components Under 2mm Tall

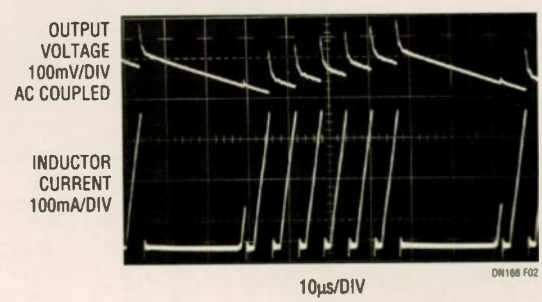


Figure 2. Controlled, Low Peak Current Keeps Output Voltage Ripple Under 180mV$_{P-P}$

Super Capacitor-Powered Backup Supply

Typical backup supplies for low power (several µW) logic systems operate from a lithium battery or a high energy density capacitor (a "super cap"). Some systems may require a higher power backup: for example, a "last gasp" write to flash memory might require several mW for several seconds. There are obstacles to efficient operation at higher loads from these power sources. Both the long-life lithium batteries and super caps have large series resistances that result in reduced efficiency at high RMS currents and poor regulation due to IR drop. In addition, the super cap output voltage, in contrast to a battery's, decreases continuously as power is drawn and the capacitor must be substantially discharged to obtain its stored energy. A micropower switching regulator is required, and the LT1316, with its ability to precisely control peak switch current, is ideally suited to such high impedance energy sources.

Figure 3 shows a 5V, 6mA backup supply operating from a 0.1F, 5.5V, 75Ω super cap. The super cap, C_{SUP}, is charged through R1 from a normally present 5V. The charge state is monitored with the LT1316's low-battery detector; the READY line is high when C_{SUP} is near full charge. When a power loss is detected, the system can pull the RUN line high to turn on the backup supply. The LT1316 operates as a simple boost regulator, generating 5V power until C_{SUP} has discharged to 1.5V. R_{SET} programs the peak switch current of the LT1316. Figure 4 shows the input and output voltage as the circuit supplies a fixed 6mA load. The output remains regulated at 5V as the input voltage drops. With peak switch current programmed to ~500mA (R_{SET} = 5.1k), output regulation is maintained for 9.6 seconds. Also plotted are the results with a peak current of 100mA (R_{SET} = 33k), enough switch current to satisfy the 6mA load current at the lowest input voltage. The benefit is obvious; the lower peak current results in lower RMS current from the super cap, reducing losses and extending backup time by 22% to 11.7 seconds.

The accurate control of peak switch current also allows the designer to better match the inductor to the power demands of the application, reducing system size and cost. Figure 5 shows the circuit operation under identical operating conditions, with a smaller CD43 series inductor substituted for the larger CD54. At higher peak currents, the additional inductor loss lowers operating time by 5%. With a low peak switch current, there is essentially no penalty for using the small inductor.

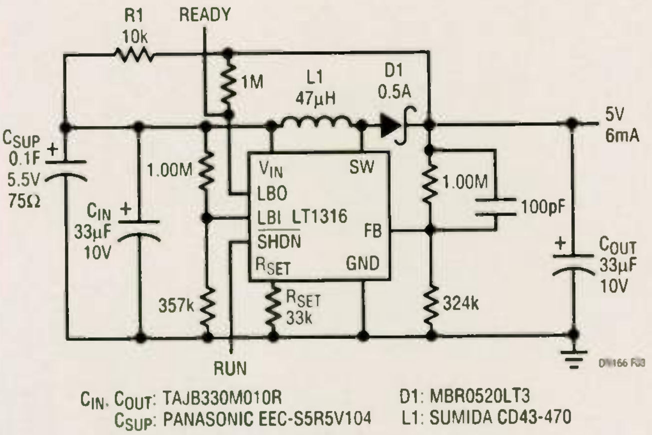


Figure 3. Super Cap Backup Supply

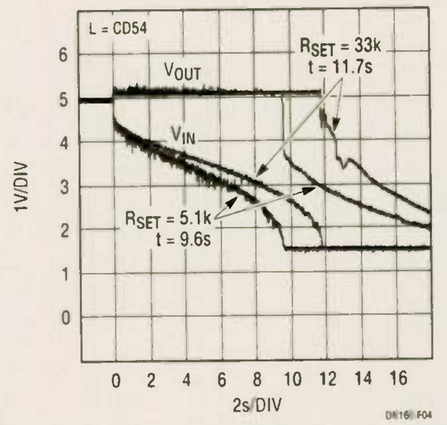


Figure 4. Lower Peak Current Results in Longer Operating Time

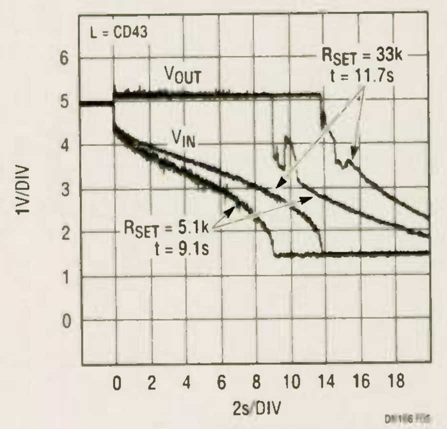


Figure 5. Lower Peak Current Allows the Use of Smaller Inductors

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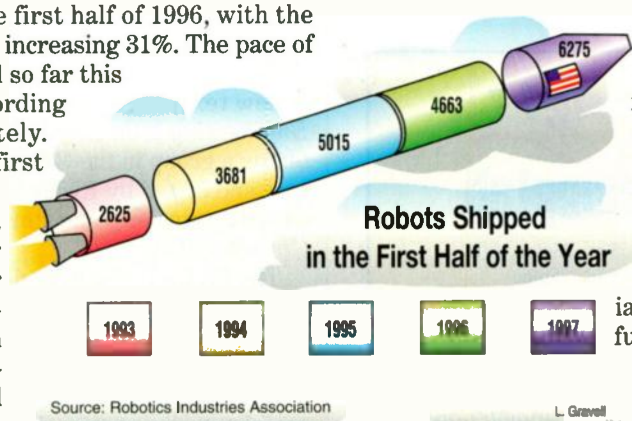
ELECTRONIC DESIGN QUICK LOOK

■ Edited by Mike Sciannamea and Debra Schiff

MARKET FACTS

Not Just Lost In Space

Formerly a niche market that has now grown into an industry, robotics are seen in the aerospace, automotive, consumer goods, electronics, food and beverage, and pharmaceutical markets. According to the Robotic Industries Association, the current U.S. robot population numbers approximately 78,000. In the second quarter of this year, U.S.-based robotics companies shipped 3142 units, which translates into $279.3 million. In the first half of the year, these same companies shipped 6275 robots (valued at $547.7 million). The executive vice president of the association, Donald Vincent, says that these numbers represent a 35% increase over the first half of 1996, with the dollar value of the shipments increasing 31%. The pace of orders that have been placed so far this year has been puzzling, according to Vincent, but not completely. Orders were up 43% in the first quarter, but down 32% in the second. Vincent points to a slowing in the orders for spot-welding robots. So far this year, he says, spot-welding is the largest application for robots, but more spot-welding robots were ordered in the second quarter of last year than in the first half of this year combined. Other applications, such as material assembly, handling, and removal have picked up the slack, making up for the drop in spot-welding-robot orders. Arc welding, coating/dispensing, and painting are a few of the other leading applications in the robotics market. Robots are perfectly suited to tedious, hazardous, or extremely precise jobs that are more cost-effectively handled by machines than humans. Based on revenue received on shipments, spot-welding applications held the robot market by 30%. The second largest sector, material handling, grabbed 27% of the market. With 18%, coating applications ate the third largest piece of the pie. Further breaking down the robot market, arc welding (13%), material removal (4%), dispensing (3%), assembly (3%), and inspection (1%) applications were the shapers of the rest of the nearly $1 billion North American robotics market. Of the market, auto manufacturers and their suppliers have the lion's share at 50% to 60%. According to the Robotics Industry Association's spin-off group, Automated Imaging Association, the auto industry also is seeing a rise in the number of machine-vision products, particularly 3D vision. Industry leaders in the automotive robotics market include ABB Flexible Automation, Acuity Imaging, Adept Technology, Cognex, Deneb Robotics, FANUC Robotics North America, Kawasaki Robotics, Motoman, Nachi Robotics, Omron, PTT Vision, and Panasonic Factory Automation. Some of the top distributors include Antenen Research, Automated Concepts, The Robot Company, and The Robot Shop. It's easy to see why robotics, as an industry, is doing so well. To begin with, robots are reliable. They're easily justified, and come in all kinds of sizes that are just perfect for all kinds of applications. One of the primary reasons why robots have gained so much ground in the consumer electronic market, as well as the business electronic market, is the trend toward miniaturization. Many of the manufacturing tasks involved in miniaturization can only be successfully and reliably performed by robots. Motorola, for example, uses robots in the miniaturization of its pagers, cellular phones, and two-way radios. One of the examples that the association gives of success stories in robotics is Honeywell Home and Building Control. Through robotics and related automation technologies, the company was able to reduce the cost of its bimetal and clip thermostat subassembly operation by $500,000 in the first year. Honeywell had attended the association's Agile Automation Workshop on Flexible Parts Feeding, and picked up the techniques to improve their process.

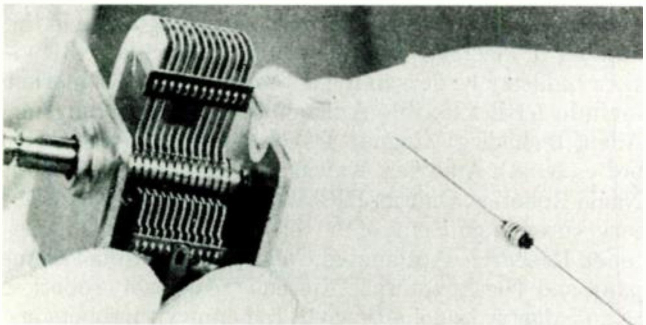


For all kinds of valuable information about robotics, how the Robotics Industries Association works, and who the suppliers and manufacturers are in the market, try accessing their World Wide Web site: *http://www.robotics.org*. Otherwise, those readers who are interested may write to the Robotics Industries Association, 900 Victors Way, P. O. Box 3724; Ann Arbor, MI 48106; (313) 994-6088; fax (313) 994-3338.—**DS**

40 YEARS AGO IN ELECTRONIC DESIGN

Varicap: Variable Capacitor

This tiny electronic component, the size of a teardrop, has special characteristics necessary for effective operation as a voltage variable capacitor. Varicap, produced by Pacific Semiconductors Inc., Culver City, California, has no filament to heat, and has no moving parts as does the reactance tube and the variable capacitor which this device is capable of replacing. The unit weighs less than a gram, is a highly rugged device, and operates reliably from -65 to +150 C. For FM transmission and reception, the miniaturization factor is extremely important, as it allows the production of



lightweight devices of greater adaptability and reliability. In television manufacture, it is possible through the use of this capacitor, to eliminate the fine tuning control. In color television, the incorporation of this device into the circuitry, will permit automatic observation and maintenance of color fidelity. *(Electronic Design, Oct. 15, 1957, p. 5)*

This might have been the first commercially available varactor diode, but certainly engineers of the time were aware of the voltage-variable capacitance properties of semiconductor diodes.—SS

New Books: Transistor Circuit Engineering, Richard F. Shea, Editor; John Wiley and Sons, New York; 468 pages, $12.00.

In the few years since transistors came into being there has been a steady evolution in the manner of their treatment and in the development of circuits particularly suited to their inherent characteristics. It was soon evident that with the proper types of transistors and associated circuit all of the operations heretofore performed by vacuum tubes could be accomplished equally well with transistors.. With the mounting drive for miniaturization of complex electronic systems, for which transistors have an obvious appeal, there has been increasing activity in the development of special purpose transistors and more suitable circuits by which to utilize their characteristics most effectively. Such advancement has encouraged the publication of new texts on the subject, of which *Transistor Circuit Engineering* is an excellent example. This book was written by a group in the GE Electronics Laboratory in Syracuse and edited by Richard F. Shea of the GE KAPL, who edited an earlier transistor text, *Principles of Transistor Circuits* (1953).

The first few chapters deal with transistor parameters and equivalent circuits, and with the applications of transistors in radio and TV. Many forms of audio, power, intermediate and rf amplifiers as well as oscillators, modulator and detector circuits, are illustrated and analyzed. Additional useful notes on matrix algebra are included in the Appendix. One chapter is allotted to the troublesome problems of bias stabilization and temperature equalization.

Perhaps the most significant part of the book to those already modestly familiar with transistors and their circuits will be the last three chapters which deal with pulse circuits, systems and special circuits. Another notable feature is the consideration given to active filters, dc converters, inverters and voltage regulator circuits under the chapter heading of Special Circuits.

A set of problems and pertinent bibliographic material is included at the end of each chapter. The book might well serve as an advanced undergraduate text for an engineering course in transistor circuit or as a reference book for the engineer already active in the transistor field. (Review written by Joseph P. Harper, Head of the Dept. of Physics, Univ. of Scranton.) *(Electronic Design, Oct. 15, 1957, p. 160)*

This was one of the classic early books on transistor circuit design.—SS

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Roederstein's MKP 1840 capacitors are also self-healing and do not exhibit a piezio-electric effect. The new 5mm lead-space capacitors are available in C-values up to .10µF and in a 100-volt rating. Larger sized capacitors are available in higher voltages and capacitance values up to 10µF. All are encapsulated in flame-retardant cases.

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OFF THE SHELF

Developing USB PC Peripherals is a guide to the evolving universal serial bus (USB) specification version 1.0. It provides a step-by-step methodology while following through design practices. The book includes illustrations, graphics, firmware, software code examples, and key industry contact numbers to give beginners and experienced engineers all they need to know to develop their own USB peripherals. The 176-page book is priced at $29.95. Contact Annabooks, 11838 Bernardo Plaza Court, San Diego, CA 92128; (619) 673-0870; fax (619) 673-1432; Internet: http://www.annabooks.com.

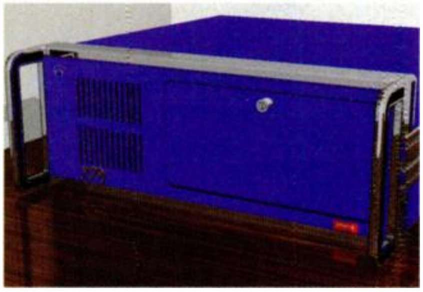
The CRC Handbook of Electrical Filters provides information for the nonspecialist about the various types of filters, their design, and applications. The book covers approximation theory and methods and introduces CAD packages that perform approximation and synthesis for both analog and digital filters. Also included are design methods for LCR, active-RC, digital, mechanical, and switched-capacitor (SC) filters. The 448-page book is priced at $79.95. Contact CRC Press, 2000 Corporate Blvd., N.W., Boca Raton, FL 33431-9868; (800) 272-7737; fax (800) 374-3401; Internet: http://www.crcpress.com.

Broadband Networking: ATM, SDH, and SONET is a comprehensive survey of the state-of-the-art in the design, planning, and management of digital transport networks. Topics that are discussed in the book include new regulatory developments; asynchronous transfer mode (ATM) principles and information formats; broadband signaling, connection control, and network-level management; traffic performance and management; resilience in a multilayer transport network; practical information on design and implementation; network planning and tools; and a look at network performance and synchronization. The 600-page book is priced at $85. Contact Artech House Publishers, 685 Canton Street, Norwood, MA 02062; (781) 769-9750; fax (781) 769-6334; Internet: http://www.artech-house.com.

Coffee, Tea, Or Sound?

It's not bad enough that unless you're in First Class, you have to pay for a headset to listen to the "radio" or the cut-to-fit movie. The sound stinks. The earphones are uncomfortable, and the audio has the unmistakable glass-against-the-wall feeling to it. Sure, some of us travel with personal portable stereos with built-in earphones, and that's all well and good unless you actually want to watch the film the airline plays on longer trips. But, the sound is so tinny and unrealistic that it's distracting to anyone with any sense of space and time. I haven't even begun to hit on competing with the continuous roar of the engines and the sound of the air hitting the wings and the cabin wall.

To combat these travelers' dilemmas, a Sydney, Australia-based company, Lake DSP Pty, Ltd. (Lake), has designed the TP1 TheatrePhones Mastering System. TP1 brings high-quality, three-dimensional surround



sound to airline passengers through the airline's existing stereo audio system. The six-year-old company supplies architectural acoustic simulation hardware and software to automotive, professional audio, research, simulation, and telecom- munications concerns.

TheatrePhones Mastering System works by playing multichannel surround sound into a computer simulation of a theater system with five or more speakers. Out of that simulation, TP1 yields a standard stereo soundtrack that mimics how the speakers would sound if the listener was actually in the theater. The key is presenting the illusion of the existence of virtual sound sources located around the passenger. The soundtrack can then be transferred in the typical manner to video tape for distribution.

Capturing the acoustical path from the loudspeaker to the reflective surfaces in a room to the listener's eardrum, the Lake TP1 TheatrePhones Mastering System is completely digital. The patented acoustic simulation technology offers the user a truly detailed "look" at the sound associated with fine theater sound systems and home-theater digital equipment. Lake Convolution, the digital signal processing system, is the source for the realistic externalization and localization described by test listeners of TP1.

As opposed to current systems (where you can see the actors' lips moving, but they're not mouthing the words you're hearing), TP1 uses real-time technology. The picture and sound are synchronized. Another feature of the system that other audio systems cannot imitate is that TheatrePhones don't require listener-specific headsets.

The appeal of the system is that airlines won't need to sacrifice funding on new audio or video playback equipment to support TP1 TheatrePhones. According to Lake, airlines can even upgrade their entire fleet's audio setup from a central location without investing a dime on the plane itself. Another important feature is the quality-control certification program. With TP1's quality control program, the airline is assured that their audio is consistently of high quality.

The system fits all popular surround-sound formats in its inputs. It also comes packaged with a number of high-quality listening environments. These environments are easily selected at the time of mastering, depending on the material chosen for production.

For more information, contact Lake DSP Pty, Ltd., Suite 1501, Level 15, 33 Bligh St., Sidney, NSW, 2000, Australia; 61 2 9233 8655; fax 61 2 9233 8656; Internet: http://www.lake.com.—**DS**

FLIPPING THROUGH THE INTERNET ROLODEX

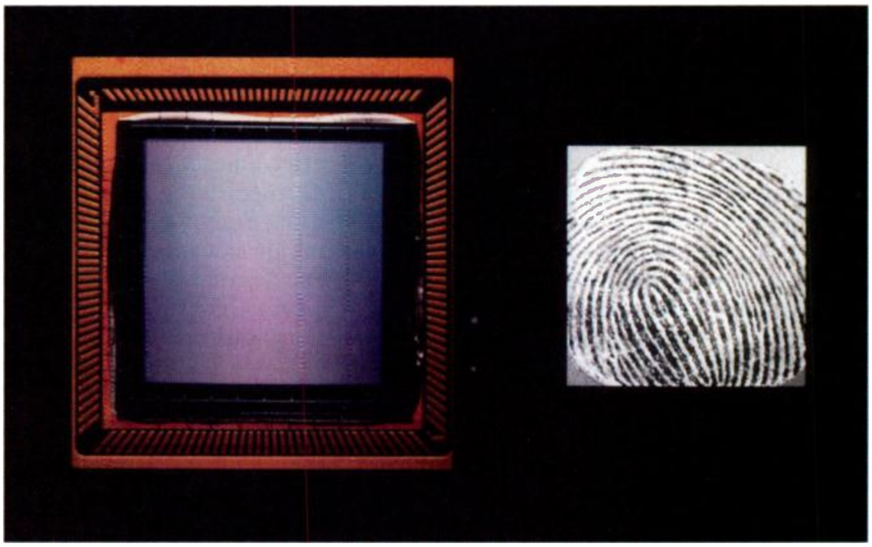
http://www.berkeleynucleonics.com: Check out Berkeley Nucleonics Corporation's newest version of it's web site. The homepage features links to digital delay generators, light pulse generators, nuclear pulse generators, general purpose pulse generators, NIM power supplies, on-line resources, accessories, trade show calendars, and an extensive price list.

Application notes on VXI/VME, optoelectronics, specifications on picosecond timing electronics, and a resume submission form also are found here. The site also features extensive information on the company's lines of peak digitizers, time-to-signal converters, and custom temperature sensing and control systems.

http://www.sony.com/professional: Sony Electronic's latest site is specifically designed to suit the professional electronics user. All of the company's product information is organized into a tree structure for quick and easy searches. Speaking of searching, the first thing visitors see when they point their browsers to this site is a search utility. Surfers looking for video and multimedia production equipment, videoconferencing systems, digital electronic cinematography products, high-definition digital production products, automation and transmission products for television newsroom applications, digital cameras, and display products, among others, can find details on them here. The site is divided into six sections: Product Applications, Product Categories, New and Notable, Software Downloads, Info and Support, and Search. Product Applications covers everything from Amusement/Novelty to Studio Production. Product Categories lists Sony's entire lines of products in alphabetical order. In the New and Notable section, Sony focuses on news stories, major sales, product introductions, partnerships, and press releases. Drivers, configuration software, and utilities may be had in the Software Downloads section. The ever-important Information and Support includes the Sony Help Desk, Sony SupportNET, and Sony Virtual Reception Desk. Finally, clicking on the Search option brings the user back to the search engines that are posted on each page.

http://www.safetylink.com: In the "Bookmark This One" category, the Safety Link site is the most helpful site of its kind yet. Indeed, this is the most extensive collection of electrical product safety links available on the web. At the time this was written, there were over 400 links that were featured here at the site. Basically, any visitor whose products have to wear the UL, CSA, TUV, or VDE tattoo of safety will find what they are looking for at Safety Link. In addition, visitors can win a free one-year subscription to International Product Safety News. The Table of Contents of last year's issue can be found at the site if you're so interested. "The New Approach—Legislation, and Standards on the Free Movement of Goods in Europe, 2nd edition" can be ordered here as well. Also featured are links to corporate supporters, safety resources, EMC resources, safety articles, FAQs, MRAs, telecom resources, the Product Safety Society, ergonomics, quality and environment resources, and many other links are available at this site.

Putting The Finger On Security



In these times, security goes way beyond just storing your most valuable documents and information under lock and key. Even items such as photo-ID cards and electronic passkeys can be easily duplicated and/or altered by anyone who wishes to gain access to sensitive files. But there is one new and nearly surefire method of security and identification. And it's right at the tip of your finger.

SGS-Thomson Microelectronics (STM) has announced the release of the first working prototype of a microchip that registers the pattern of a human fingertip, detecting variations in electrical currents running along the ridges and valleys of the skin. The working prototype was recently demonstrated at the CardTech/SecurTech Conference held in Orlando, Fla.

The company's patented electronic fingerprinting imaging sensor, the subject of a technical paper presented earlier this year at the International Solid State Circuits Conference (ISSCC), differs from existing technologies. Through direct physical contact, the sensor array "grabs" a fingerprint pattern without using an optical or mechanical adapter such as a scanner or camera. When the individual wishing a security clearance places his or her finger onto the chip's silicon surface, the capacitive sensors register the fingerprint pattern by interacting with electric field variations on that person's skin. Consequently, the chip then creates an electrical representation of a fingerprint which can be checked against files of registered fingerprints.

Designers at SGS-Thomson say that this technology offers superior gray-scale image quality and a direct route to the digital information normally used in the personal identification process.

Compared to other personal identification methods such as infrared and retinal scans, the electronic fingerprint technology is said to provide heightened security, ease-of-use, and cost benefits. The one-chip solution is smaller in size, and ultra-low power when compared to optical methods, consuming less than 1 mW at 5 V. It also generates higher image quality than most other identification methods, including technologies that are based on heat. Since the chip's pixels are on a pitch of more than 25 µm, it can easily be integrated into standard CMOS technology, the digital microprocessing common to desktop computers, in order to keep costs low.

For more information on this development, contact SGS-Thomson Microelectronics, 55 Old Bedford Rd., Lincoln, MA 01773; (617) 259-0300; fax (617) 259-9423; Internet: http://www.st.com.—MS

INTERNET NEWS

Aside from speedy delivery of information, the other primary request of Internet users is security. A new offering from Querisoft, SecureFile 1.0, uses Microsoft's CryptoAPI technology to promote an environment of privacy for users. The unique aspect of this software is that it doesn't just protect Internet usage—it totally protects the desktop.

Once users load SecureFile into the system, a SecureFolder icon is created on the desktop. Personal documents can be protected simply by dragging and dropping the files onto the icon. Documents with multiple users can be brought into a secure environment for exchange over the Internet with an e-mail client.

Because the software is fully integrated with Microsoft Office 97, all security operations can be performed from within Excel or Word. And for those who enjoy having their hands held during the process, Wizards are built into the system. There also is a built-in Certificate Manager to provide the export or import of X.509 version 3.0 certificates, including VeriSign Digital IDsSM.

Querisoft linked with VeriSign to provide users with the means to exchange their digital IDs with each other in a secure environment. Also supported in the software is RecoverKey CSP from Trusted Information Systems. RecoverKey allows users to recover files that were secured with keys that were damaged, lost, or stolen.

Cryptographic tokens such as Spyrus Lynks Privacy Card and Fortezza Cards also are integrated with the system, which is priced at $39.95.

For more information, contact Querisoft Inc., 3390 Peach Tree Rd., Suite 1700; Atlanta, GA 30326; (404) 812-6264; fax (404) 812-6267; Internet: http://www.querisoft.com.

Virus protection is another form of security that people tend to forget about until their system fails. One way to handle this problem is to prescan information that comes into the working environment. Recently, Trend Micro granted a patent license to The Electric Mail Company to protect its clients' e-mail, a major source of virus infection via file attachments.

The InterScan VirusWall technology automatically scans Internet e-mail attachments for viruses before sending them into the corporation. According to the National Software Testing Laboratory, InterScan VirusWall processes e-mail three times faster than McAfee's WebShield. It beats Norton AntiVirus by a factor of 1.5.

The VirusWall can block Java applets, Active X controls, and other software applications not recognized by the Authenticode protocol. This protocol's source is the commercial software supplier. The virus scanner also examines SMTP e-mail attachments, HTTP downloads, and FTP files.

Electric Mail is an Internet e-mail company based in Vancouver, B.C., with many U.S. customers. Recently, Electric Mail added E-mmunity virus protection to its cadre of offerings. E-mmunity automatically scans all Internet e-mail attachments for viruses before delivering them to the service's subscribers. No hardware, software, or maintenance is required. The monthly fee is $35 for 30 subscribers.

For more information, contact Trend Micro Inc., 10101 N. De Anza Blvd., 4th Flr., Cupertino, CA 95014-9985; (408) 257-1500; fax (408) 257-2003; Internet: http://www.antivirus.com.

Brooktrout Technology has partnered with Centigram Communications to pair OneView Web Internet faxing capability with Brooktrout's TR114 Series Universal Port fax boards. The boards offer full fax processing on a single multichannel board. It allows users to view their voice, fax, and compound messages, and allows for creation, answering, or forwarding of messages via the Internet, circumventing the cost of a local call.

Contact Centigram Communications, 91 E. Tasman Dr., San Jose, CA 95134; (408) 944-0250; fax (408) 428-3732; Internet: http://www.centigram.com.

Y2K UPDATE

There comes a time when anyone with half a grip on the Year 2000 Date Change issue decides to surf the Internet in search of things he or she hasn't already seen or heard of concerning the problem. I have an excuse: it's my job. But for those of you who don't have the time (the plaintive cry of most engineers), here's a very helpful site to check out: *http://www.solace.co.uk*.

SEEKING SOLACE

Solace Consulting Services has provided some interesting data on its site that may change some minds about products out there that call themselves "solutions." Their research shows that 30% of the packages available to address the Y2K issue give false or misleading results. In the testing phase, 40% of those packages failed to perform comprehensive tests. Another 40% failed to give clear and concise warnings. A whopping 80% didn't even address the software issue. Sadly, 80% don't offer localized support. And, finally, 81.25% performed tests that weren't even germane to compliance. The take-home message here, as asserted by Solace, is that you get what you pay for—stay away from freeware and shop around.

Also at the site is an Abridged Matrix, which spells out the test results of 14 different software products. Solace looks at 25 different aspects of software reactions to Y2K, but they're just described at the site. The matrix only shows the points that the various software scored.

The following list is the testing ground for all the software that Solace encounters:

- reliability
- guarantees
- installation support
- power on real-time clock rollover
- real-time clock century byte test
- a BIOS compliance test
- ability to retest
- 2000 leap year real-time clock
- free demo or evaluation copy
- availability
- site license version
- ease of use
- foreign language versions
- 2000 leap year system clock
- 2001 leap year system clock
- system clock rollover
- software listing
- software analysis
- software helpline/assistance
- price
- software protection
- fix
- additional tests
- comments

WHAT DO THESE TESTS MEAN?

Starting with the "power on real-time clock rollover," because most real-time clocks rollover from 1999 to 1900 (as opposed to the system clock which tends to rollover to 2000 just fine), it's the most commonly tested element of the Y2K problem. It's also the test most likely to fail on most PCs, according to Solace.

The real-time clock century byte test looks at whether the byte that carries the 19xx or 20xx information refuses to retain the century because of an exhausted CMOS real-time clock back-up battery or an interfering BIOS. If software fails this test, then the programmer must make the change a permanent one.

If compliance software does not test BIOS compliance, then the real-time clock testing is not fully complete. Basically, the BIOS doesn't "talk" to the real-time clock unless a date instruction is requested by either software or DOS commands.

Through all the clock testing mentioned above, plus a system-clock rollover test, only three software programs came near the maximum score of 55. Two products were from Greenwich Mean Time Inc., the Check 2000 PC and Client Server products, scoring 50 points each. Computer Experts' offering scored 53 points in the clock tests.

The software tests (with a maximum score of 15) are based on whether or not the software on the computers' hard disks would be audited to the extent of producing a list of all executable programs, whether or not the software will analyze the software list produced and tell where the problems lie, and if the software package provides live web site support or a support telephone number in the local region (or a toll-free number). Again, the two winners in this category turned out to be Check 2000 PC and Check 2000 Client/Server.

Solace does separate Availability and Support into an entirely different category, judging on four sectors: availability, localized telephone support, local contact points, and foreign language support. The total number of points that can be awarded in this category is 20. The Greenwich Mean Time products, as well as Deeside Technology's freeware, each were awarded 20 points. Two close runners up were Prove It 2000 (18 points) and Eye-t Technology's (17 points) software.

WARNING! WARNING!

Warning systems are essential for the end user's working environment, as well as peace of mind. Solace bases its warning point system on whether the software is unable to run other software concurrently, clear on-screen warnings, halt procedures while closing software, and if warnings are clear in the literature. Software examined by Solace has the opportunity of gaining a total of 10 points in this category.

Three software packages from Computer Experts, Eye-t Technology, and The RighTime Company were awarded 10 points for their warning systems. Greenwich Mean Time's programs each hit the eight point mark. Several companies, same as in the Software Testing category, rated zero in this category. These companies were NSTL, JDM-Bug, Doschk, and American Megatrends. All of those companies offerings are freeware.

So, if you're the decision-maker, or you know the person who is, it might be a good idea to check out Solace's services. Good market research often prevents costly mistakes.

For more information on these developments, contact Solace Consultancy Services Ltd., 9 Crowmere Avenue, Bexhill on Sea, East Sussex, England TN40 2BA; fax: 44 1424 217791; e-mail: info@solace.co.uk.—**DS**

QUICKNEWS

I've Got The Power—Altec Lansing Technologies, long recognized as one of the leaders in consumer audio technology, has added to its family of PowerCube computer audio speakers. The company's line of speakers is completely digital and fully integrates with any computer. Users set the speakers' levels via a graphical-user interface.

These speakers, the ACS43 system, communicate with the CPU via the USB. Within the speakers, Altec Lansing has included a USB microcontroller circuit which decodes the digital signals sent from the CPU to the speakers. Then, the chip algorithmically processes the data into multichannel audio signals. It also sends the signals to the correct drivers so that they can interpret the sound for the user.

Speaking of drivers, the ACS43 set of speakers has two 3-in. full-range drivers. In addition, the system features 10 W rms of audio power output. The system uses Altec Lansing's patented side-firing driver technology and Dolby Pro-Logic circuitry to create True Digital Audio.

Each individual speaker measures 13 in. by 9 in. by 7 in. and weighs 4.5 lb. The speakers are formed from light gray, textured ABS, and are UL/CUL/CE approved. The sensitivity is 300 mV input for full output and the input impedance is >10 kΩ.

The ACS43 speaker system retails for $49.95.

For more information on the OwerCube ACS43 speakers, contact Altec Lansing Technologies, Milford, PA 18337-0277; (717) 296-4434; fax (717) 296-6887; Internet: http://www.altecmm.com.

Showing Their Tru Colors—TruVoice text-to-speech (TTS) software, available in English, Spanish, French, German, and Italian, is used in commercial computer telephony, handheld translation dictionaries, and a number of other applications. The software, from Centigram Communications Corporation, has now been licensed to Parlance Corporation. Parlance plans to use TruVoice in its NameConnector service.

NameConnector marries speech recognition software with computer and telephony technology to produce a different kind of corporate telephone system. Using the NameConnector service, users dial one access number and say one name to reach that person. The system houses up to 4500 names.

OK, we've all encountered this technology before, but NameConnector repeats back the selected name in a natural sounding "voice" (via TruVoice) to confirm that the name you said was actually the person that you're seeking. One advantage that Centigram is touting is the fact that mobile communication users, such as those individuals in sales or other high-travel positions, don't have to look up an extension or input it while driving.

TruVoice uses a patented voice synthesizer and linguistic rules to analyze vocally volunteered data and spew out natural-sounding speech. The entire NameConnector service is a combination of hardware and software that works directly with an enterprise's existing telephone system.

For more information, contact Parlance Corporation at (888) 289-4458, or Centigram Communication Corporation 91 E. Tasman Dr., San Jose, CA 95134; (408) 944-0250; fax (408) 428-3732; Internet: http://www.centigram.com.

HOT PC PRODUCTS

The VisionBook Plus, Pro, and Elite notebooks from Hitachi are Pentium-based computers packed with communications features. The Plus model is targeted toward small-office/home-office managers, retail consumers, and tight-budgeted corporate buyers. The Pro and Elite notebooks are ideal for the communications-conscious consumer or telecommuter.

The VisionBook Plus weighs 6.5 lb. with the battery, and measures 1.7 in. by 11.7 in. by 9.3 in. It comes with

a full-size Windows 95 keyboard, a Synaptics touchpad, a Lithium Ion or Nickel Metal Hydride "smart battery," and a wireless infrared port. The laundry list of features is pretty healthy: choice of Pentium 133 or 166 MHz processor with MMX technology, 256 k L2 cache, U.S. Robotics 33.6-kbit/s fax/data modem, 16 Mbytes EDO DRAM (upgradeable to 128 Mbytes), removable 1.44 or 2.1 Gbyte hard drive, 10X CD-ROM drive (interchangeable with 1.44 Mbyte floppy disk drive), slots for two Type II or one Type III PCMCIA cards, support for Zoom Video, SoundBlaster Pro 3.01, 64-bit graphics acceleration, internal microphone, and two speakers.

The list of pre-installed software includes: Windows 95, Hitachi ConfigSafe 95 diagnostics, Microsoft Works, and Microsoft Money. The back side of the VisionBook Plus features a parallel port, an ac adapter port, a security lock, a ps/2 mouse and keyboard port, an external monitor port, a serial interface port, and an expansion slot. Pricing for the 133 MHz Pentium system with a 1.4-Gbyte hard disk drive and a 12.1-in. high-addressing dual-scan display begins at $1799. For a 166 MHz Pentium with MMX technology with a 2.1-Gbyte hard disk drive and a 12.1-in. TFT display starts at $3499.

Moving on to the VisionBook Pro, Hitachi raises the stakes with this

one. It's the first notebook with a cellular-ready U.S. Robotics 56-kbit/s modem with X2 technology and a 10Base-T Ethernet LAN port. In addition to the features mentioned above for the Plus model, the Pro has a 13.3-in. full-color XGA display, a modular CPU design, a removable 2.1- or 3.2-Gbyte hard-disk drive, and the Hitachi Processor Module.

The Hitachi Processor Module is a CPU daughter-board with a standard surface-mount PCI connector.

It has several key chip sets. The module allows upgradability and thermal cooling. It integrates the Pentium processor, a PCI set systems logic controller, a thermistor, and Level 2 cache in either 256- or 512-kbyte configurations. A copper shield on top of the board keeps the processor module cool.

The only differences between the Elite and the Pro are that the Elite is very thin, weighs in at 5.15 lb., has 2 Mbytes of video RAM, and has two touchpad buttons.

The Pro is priced between $3199 and $5299, and the Elite carries a $4999 price tag.

For more information, contact Hitachi PC Corporation, 2520 Junction Ave., San Jose, CA 95134; (408) 321-5000; fax (408) 321-5100; Internet: http://www.HitachiPC.com.

The new ViRGE family of software drivers from S3 are designed to increase the rendering capabilities of the ViRGE 3D accelerators. According to Jon Peddie Associates, Tiburon, Calif, who tested the drivers with the Ziff-Davis 3D WinBench 97, these new high-performance software drivers raised performance over 50%. S3 supplies companies with multimedia acceleration hardware and its associated software.

The testing system comprised a Dell Dimension XPS M200s, Intel 200 MHz Pentium processor with MMX technology, an S3 ViRGE/GX graphics accelerator with 4 Mbytes EDO DRAM, 32 Mbytes SDRAM DIMM, a 512-kbyte pipelined burst SRAM cache, a 2.1-Gbyte EIDE drive, a 3.5-in. 1.44-Mbyte disk drive, an Iomega Zip EIDE drive, a 12X min/16X max CD-ROM drive, and Windows 95. When S3 combined their latest 3D accelerator, the ViRGE/GX2 with the Pentium II, a Dell Dimension XPS H266, the performance yielded a 3D Winmark 97 score of 81.2. This score is in comparison with the 61.6 mark of the ViRGE/DX and the GX 3D.

Against ATI Rage2 and Matrox Mystique, S3's drivers had more hardware support in the following fields: fog vertex, specular highlights, color-key transparencies, alpha transparencies, linear, mip-map linear, dithering, perspective correction, fog vertex/color key, and fog vertex/alpha. Designers tend to look for speedy 3D rendering engines, but since speed is becoming less of an issue, 3D performance has risen to the forefront. The ViRGE accelerator showed that it provides very high-quality images without a drain on performance.

Contact S3 Inc., 2801 Mission College Blvd., P. O. Box 58058; Santa Clara, CA 95052-8058; (408) 588-8000; fax (408) 980-5444; Internet: http://www.s3.com.

KMET'S KORNER

...Perspective on Time-to-Market

BY RON KMETOVICZ
President, Time to Market Associates Inc.
P. O. Box 1070, 100 Prickly Pear Rd., Verdi, NV 89439; (702) 345-1455; fax (702) 345-0804


RON KMETOVICZ
CONTRIBUTING EDITOR

In searching for improved time-to-market, consider spending less on tools and more on the people who use them. To explain, I'll digress a bit to describe an automotive situation I recently encountered.

I own a 1984 Ford Bronco II 4 by 4, whose odometer reads over 110,000 miles. My wife bought the car used in 1986 for $8000 and drove it until 1994. She then moved on to a new machine and passed the B2 (as we call it) on to me. It takes me deep into the Tahoe National Forest reliably. The body dents and dirt provide ample evidence of where the B2 travels. It's a great tool for the application and it's cheap (about $3000, in good condition).

In contrast, my friend Doug stopped by with his new top-of-the-line Jeep Grand Cherokee. On the specification sheet, his machine makes my Bronco II look like dead, decaying meat. Come to think of it, just looking at the two side-by-side produces the same effect. His V8 produces more horsepower than the V6, and his computer system controls the power distribution to all four wheels. Add climate control, styled wheels, leather interior, a fancy paint job, and power everything to produce the ultimate feature set. I could not contain my enthusiasm to see it do its magic in the dirt. But, it never happened!

First, to get the gas mileage up, Jeep installs street radial tires. Driving them over a rock bed shreds them to pieces, so sharp rocks must be avoided. Doug also wants to keep it looking nice inside and out, so the machine must stay on pavement, preferably in an urban or interstate environment. Getting it dirty, scratched, or dented was out of the question. A mountain frame and wheel alignment was completely out of consideration. This vehicle typically costs about $30,000.

My Bronco II gets the off-road job done for $27,000 less, and I don't have to worry about breaking it. In getting from point A to point B in rugged country it works better than the new pampered fancy machines. Now take this point into the product-development environment.

Design tools, computers, and software decline in value up to 50% per year. Working just a year or two behind the bleeding edge saves a lot of money. If you can use older systems effectively and remain competitive, they offer great value. But a trade-off occurs. Those using the time-tested tools must be as productive as those using the new ones to maintain parity in getting new product to market. The specifications and features of the new tools don't always translate into improved design productivity.

As with the Grand Cherokee, the extra burden of excess performance and unnecessary complexity may actually reduce the productivity of those electing to use the new material.

My request of engineering managers and their teams is to carefully review how you spend money on tools. If you can't identify and measure productivity gains, stay with the old systems and spend the savings on adding more smart people to your staff.

To obtain an e-mail copy of "The Complete List for Late Product Information," readers may contact Mr. Kmetovicz at kmetovicz@aol.com.

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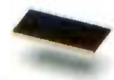

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We've taken the industry's first T1 Single-Chip Transceiver, the DS2151, and added more features without adding cost. The DS2152 Enhanced T1 Single-Chip Transceiver starts with all the great features of the original:

- Incorporates line interfacing, framing, elastic stores, and line monitors in a small, 100-pin LQFP package, saving board space, component count, and cost
- Handles both long and short haul lines so it can be deployed anywhere within the network
- Provides same footprint for T1 (DS2152) and E1 (DS2154) devices, allowing you to move from the North American to the European/Asian market with a simple chip change

Less Firmware; One Processor for Multiple Channels

But the DS2152 then goes on to add features to increase flexibility with two goals in mind. First, it incorporates more functions in the hardware, eliminating the expense and time required for firmware or external hardware development. Second, the new chip reduces processor real-time servicing. One processor can now service multiple channels, reducing board space consumed and costs for additional chips.

The New Features Menu

- **Crystalless Jitter Attenuation:** A single T1 clock source can now serve up to 28 channels, greatly reducing the board space required and the cost of multiple crystals. This feature is especially advantageous in multi-port designs.
- **Hardware Voice Signaling Support:** The DS2152 can move signaling across the user's backplane without firmware intervention, which unburdens the host from handling the real-time voice signaling and leaves it free to perform other functions.
- **Non-Multiplexed and Multiplexed Bus Option:** Your equipment can directly connect to an inexpensive 8-bit controller or a complex 16- or 32-bit host.
- **Per-Channel Conditioning:** The user can "groom" each DS0 channel independently as required, especially useful in Fractional T1 applications and for testing and provisioning DS0 channels.
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READER SERVICE 147

IC Controllers Provide Notebooks With 20 W Of Stereo Power

With The Use Of Increased Input Voltage And Higher Power FETs, New Controller-On-A-Chip Can Supply More Power.

Frank Goodenough

COVER FEATURE

You have been assigned the challenging task of designing a new notebook computer packed with "multimedia bells and whistles." Because these machines demand enough power to handle high-end graphics and other multimedia functions, marketing-oriented people keep pushing for even more power out of laptops and notebook computers, with some wanting as much as 20 W of rms audio output power. Their attitude can be described as "so what if the case melts down after just a couple of hours of driving a pair of large 4-Ω speakers and long before the battery runs dry." Never mind that this computer also requires lots of battery power.

But designers shouldn't begin pulling their hair out yet. To help them cope, a new IC from Linfinity Microelectronics is now available to answer the call. It sports a pair of pulse-width-modulated (PWM) class-D controllers designed to drive four low on-resistance power-FET bridges *(Fig. 1)*. This dual-controller chip, dubbed the LX1720, creates so-called class-D audio from the two linear stereo audio signals using PWM techniques similar to those used in switching-regulator controllers and in ac motor-speed control.

Class-D switching audio amplifiers have been around for a long time and the technique has been tried, albeit unsuccessfully, for high-volume consumer audio applications. The PWM switching rate for the audio must be higher than that for control of 50- to 60-Hz motors and, in most cases, higher than that for dc-dc converters. The LX1720 operates at a frequency of about 350 kHz

Bigger FETs = More Power

The LX1720 can create significantly more power if increased input voltage and higher power FETs are used. Efficiency typically runs better than 90%. As is the case with switching power supplies based on IC controllers and off-chip FETs, efficiency cannot be guaranteed since the lowest-cost FETs may not have low enough on-resistance to provide the efficiency. Linfinity's 20-W (10 W rms per stereo channel) reference design takes up little space on a printed-circuit board (pc board) of only about 1.5 by 1.2 in. *(Fig. 2)*.

As FETs get smaller, so will the amplifier. The amplifier now uses FETs with an on-resistance specified at 0.1 Ω. Under these conditions, including the 0.1-Ω FET switches, the amplifier's audio bandwidth spans a frequency range of 18 Hz to 20 kHz, while the output signal distortion is less than 0.5% while running off a 7- to 25-V power-supply rail. For most applications, the FETs do not need to be heat-sinked because of their very low on-resistance.

Other Applications

There are other applications for the LX1720 besides notebooks. These include virtually any battery-powered consumer products, including portables. The LX1720 should extend battery life for all of these applications. When not driving FETs, the LX1720's power drain operating from a 7- to 25-V power-supply rail is just 7 mA in the normal mode, and less than 1 µA in the sleep mode.

As noted earlier, by changing the power FETs and/or their power-supply voltage, higher power amplifiers are possible, which opens up some other applications. For example, it makes possible kilowatt audio amplifiers that could be located inside a loudspeaker and powered by batteries (lead acid) placed inside the speaker.

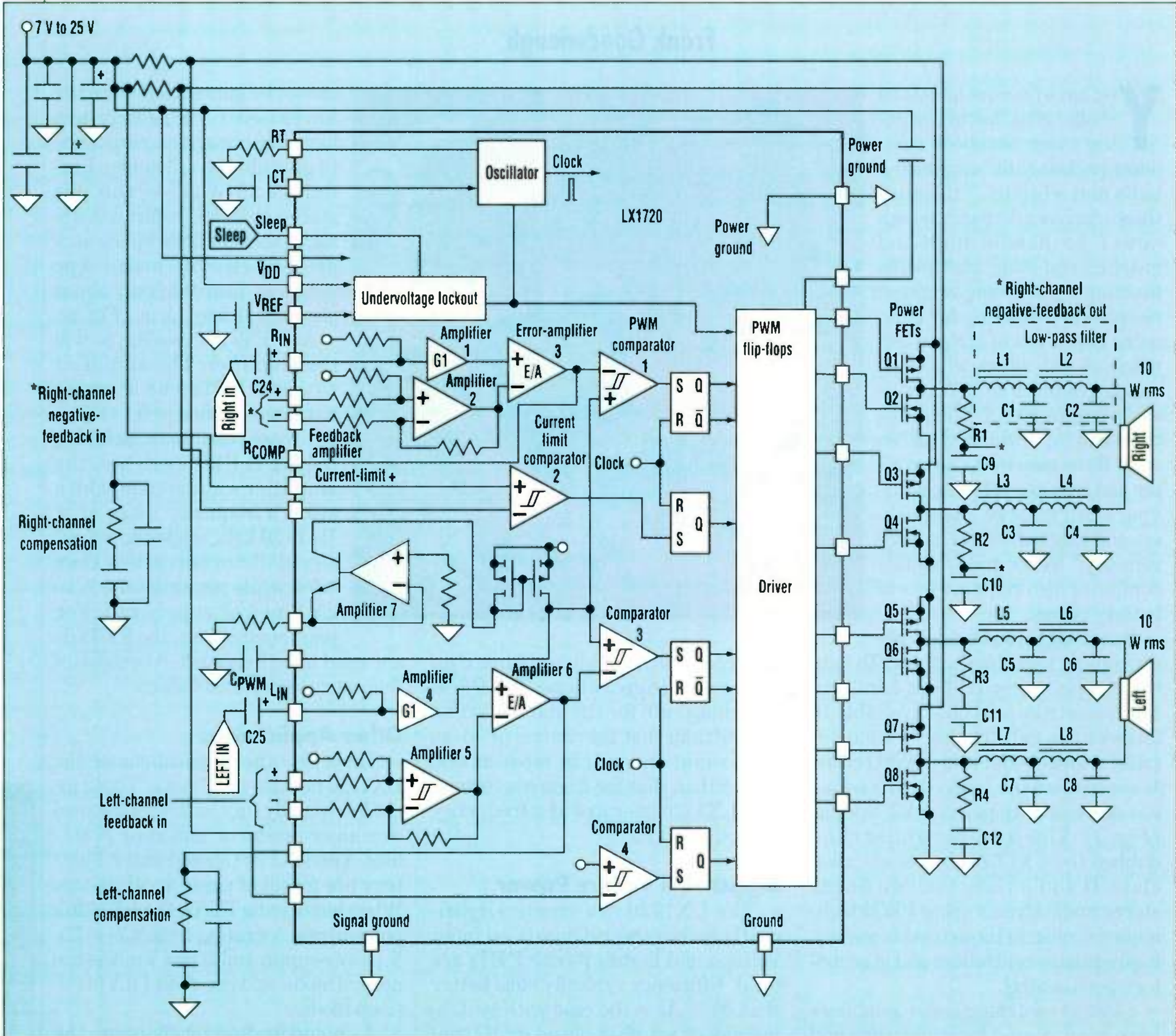
Here's How It Works

The LX1720 is a stereo controller with two identical PWM switch-mode modulation channels that share some of the resources required for optimum low-power and low-noise operation *(Fig. 1, again)*. The oscillator, which operates at a frequency up to 500 kHz, is among the shared resources, as is the undervoltage-lockout circuitry, which enables the safe operation of the controller by monitoring the supply voltage and turning off the oscillator's power when the supply voltage dips below a certain level.

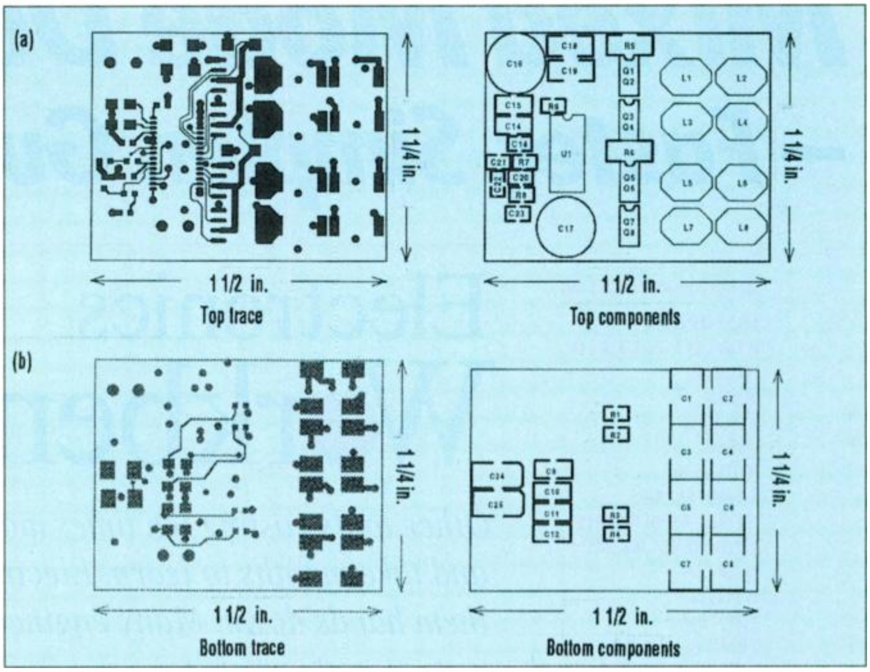
The two channels also share the ultra-linear PWM ramp that's independently generated from the oscillator. This ramp is made a function of the supply voltage through the use of AMP7 and its associated circuitry that generates a current proportional to the supply voltage. This current produces the ramp across off-chip capacitor CPWM (C15) whose voltage is then fed to PWM comparators 1 and 3. Since both the right and left channels are identical, only the right channel is described. In a typical implementation, the oscillator frequency is set to 330 kHz with off-chip resistor RT and capacitor CT. The clock output from the oscillator enables the resetting of the PWM flip-flops and several additional functions.

As noted earlier, a full-bridge output power-circuit configuration is used to enable single supply operation and for providing the maximum amount of output power to the speakers. Either 4-Ω or 8-Ω speakers can be used.

Because of the full-bridge configura-



1. Negative feedback around both baseband audio loops minimizes distortion in amplifiers built with the Linfinity LX1720.



2. The LX1720 lets a designer put a dual 10-W rms stereo amplifier on less than 1.5 by 1.25 in. of pc board as shown here with actual-size top-side (a) and bottom-side components (b).

tion and single-supply operation, the input signal and feedback stages must use level shifting for proper operation. The signal "Right in" from the right input audio source on the left of figure 1 goes through capacitor C24 to remove any dc components at the input of amplifier 1. A dc level is added to the signal at this point to enable processing inside the LX1720. This compound signal is amplified to the proper level with amplifier 1 and is applied to the high-bandwidth transconductance amplifier, amplifier 3, which features the stable gain characteristics essential for this application.

The inverting input of amplifier 3 gets its signal from the output of feedback amplifier 2. The high-frequency ground-to-supply voltage pulses present at the junctions of FETs Q1-Q2 and Q3-Q4 are removed by filtering with the use of resistor-capacitor combinations R1-C9 and R2-C10. The output of these low-pass RC filters and the signal is sensed with differential amplifier 2. The error signal between the incoming audio signal at the output of amplifier 1 and the output signal at the output of amplifier 2 is amplified through amplifier 3 and is applied to PWM comparator 1 where it is compared to the PWM regulating ramp discussed earlier. The PWM pulse at the output of comparator 1 is then latched at the output of the R-S flip-flop which turns the output power MOSFETs on and off.

For low-voltage applications such as those found in desktop and notebook computers, these MOSFETs are surface-mount devices with approximately 100 mΩ of on-resistance. At the output of these FETs, two four-pole LC filters connected to each leg of the power bridge filter out the high-frequency switching waveform. The filter element values are chosen to give the best rejection at 330 kHz while providing the best audio signal from the speakers. With a 15-V supply, the circuit is capable of providing more than 10 W of continuous rms power per channel with better than 90% efficiency.

Price And Availability

The LX1220 operates over the commercial-perating temperature range. It comes in a 36-pin SSOP package. In 1000-unit quantities, it is priced at $11.75 each.

Linfinity Microelectronics Inc., 11861 Western Ave. Garden Grove, CA 92641; (714) 898-8121; Internet: http:// www.linfinity.com.

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READER SERVICE 181

New Cycle Proportionality Factor Eases PFM Converter Design

Use Of A New Parameter ξ (Xi) Offers The Basis For A Universal Design Method Applicable To Any One-Shot Sequenced PFM Flyback Or Autotransformer Boost Converter.

DARRYL PHILLIPS, Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086; (408) 737-7600.

Over the last three years, second-generation PFM (Pulse Frequency Modulation) controller ICs have emerged, offering both extremely low quiescent current and high efficiency. Designed to maximize battery life in portable products, they minimize switching losses by only switching as needed service the load. The resulting quiescent current is on the order of 100 µA, even in circuits designed for over 10 W. This makes them well adapted for use in cellular telephones, personal digital assistants (PDAs), and other instrumentations that demand considerable power for short periods of activity but spend the majority of their operating time in a low-power standby mode. They are available for buck, boost, and inverting topologies.

Some of the new PFM controllers are suitable for flyback and autotransformer-boost applications *(Fig. 1)*. Use of a current-limited one-shot sequenced control scheme allows them to adapt to a wide range of input voltages and duty cycles. They offer stable operation with high duty cycles without additional slope compensation circuitry—even in continuous conduction mode. These attributes raise the prospects of using low-cost, off-the-shelf transformers such as the Versa-Pac series from Coiltronics.

One-Shot Sequenced Converters

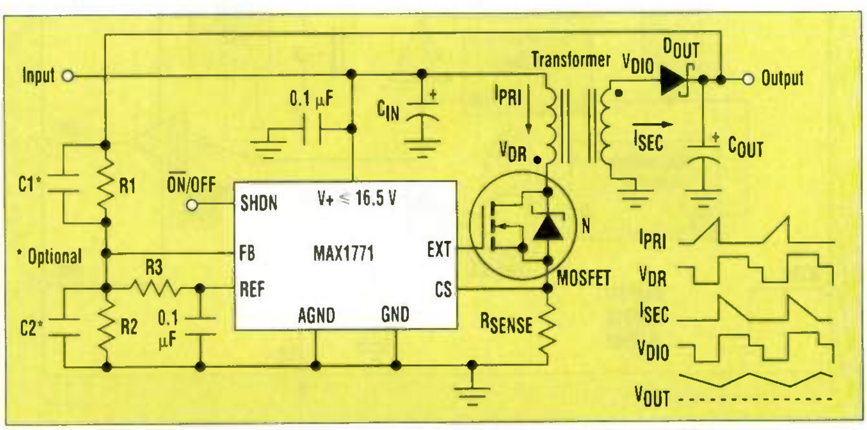
PFM controllers transfer a discrete amount of energy per cycle and regulate the output voltage by modulating switching frequency. Current-limited one-shot sequenced PFM controllers utilize an error comparator, current sense comparator, minimum-off-time one-shot, and maximum time one-shot for feedback and control *(Fig. 2)*. This frees them from the timing constraints associated with a traditional gated-oscillator core.

When the output voltage drops too low, the error comparator sets a flip-flop that turns on the external MOSFET. Turning on the MOSFET allows current to ramp up in the transformer primary winding, storing energy in a magnetic field. The MOSFET turns off when either the current sense comparator or maximum-on-time one-shot is tripped. Interrupting the input current causes the transformer to generate a voltage surge that forces current from the secondary winding through the output diode to the output filter capacitor and load. As the stored energy is depleted, the current ramps down until the diode turns off. At this point, the transformer may ring a little due to residual energy and stray capacitance. The output filter capacitor stores charge when current flowing through the diode is high and releases it when the current is low, thereby maintaining a steady voltage across the load.

As the load increases, the output filter capacitor discharges faster and the error comparator initiates cycles sooner, increasing the switching frequency. Maximum output current and maximum switching frequency are limited by the minimum off-time, around 2 µs for the MAX1771. The minimum-off-time one-shot enforces a lower limit to how soon the error comparator can initiate a cycle to ensure adequate time for energy transfer to the output during the second half each cycle. Depending on the controller and circuit, a PFM converter can reach full load in either discontinuous or continuous conduction modes. *Continuous conduction mode* is just jargon implying that the transformer current does not ramp to zero during each cycle.

Comprehensive Design Equations

Unfortunately, the lack of comprehensive equations for PFM flyback and autotransformer boost circuits leaves designers groping in the dark, struggling with the derivation of key



1. Some of the new PFM controllers are suitable for flyback applications. Stable operation over a wide range of duty cycles permits using low-cost, off-the-shelf transformers in a wide range of applications.

circuit parameters and selection of external components. Few tools are available for evaluating the feasibility of the circuit and key trade-offs before fabrication and purchasing components. Experimentation in the lab is needed, even during early stages of design. However, this can lead to considerable expense and wasted time.

The impediment to obtaining comprehensive design equations is the interdependency between the peak switching current and transformer primary inductance. The peak switching current (set by the current sense comparator) is a key parameter that affects the specifications of all the power components is the circuit. Flyback and boost converter circuits should be designed to output the maximum load current from the minimum input voltage. Under these conditions, the average input current and peak switching current for a flyback circuit are related by:

$$I_{IN,AVG} = \frac{V_{OUT} I_{OUT(MAX)}}{\eta V_{IN(MIN)}} = \frac{t_{ON}\left(I_{IN,PEAK} - \frac{1}{2}\Delta I_{IN}\right) + t_{OFF}(0)}{t_{ON} + t_{OFF}}$$

where the nominal efficiency is typically around 75% to 85%. The problem is encountered when one tries to substitute for the on-time ripple current:

$$\Delta I_{IN} = \frac{t_{ON} V_{IN}}{L_{PRI}}, \text{ but}$$

$$t_{ON} = \frac{\left(I_{IN,PEAK} - I_{IN,VALLEY}\right) L_{PRI}}{V_{IN}} = \frac{\Delta I_{IN} L_{PRI}}{V_{IN}}$$

Around and around we go. One could try assuming a MOSFET on-time. However, for anything but a narrow range of applications and operating conditions, assuming a single value results in erroneous or unoptimal answers.

Introducing ξ (Xi)

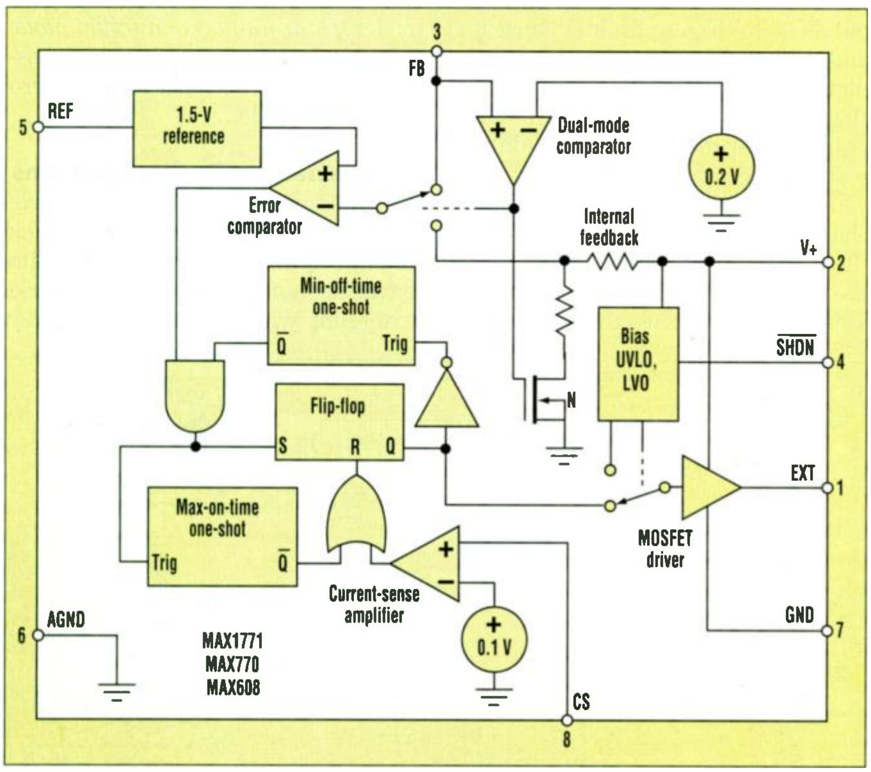
The foundation for comprehensive PFM flyback and autotransformer-boost design equations lies in the Cycle Proportionality Factor ξ (Xi). This new parameter overcomes the interdependency between the peak switching current and transformer primary inductance. It achieves this by normalizing them with respect to the timing characteristics of the PFM controller and the circuit *(see "What is ξ (Xi)?" p. 92)*.

A Simple Definition

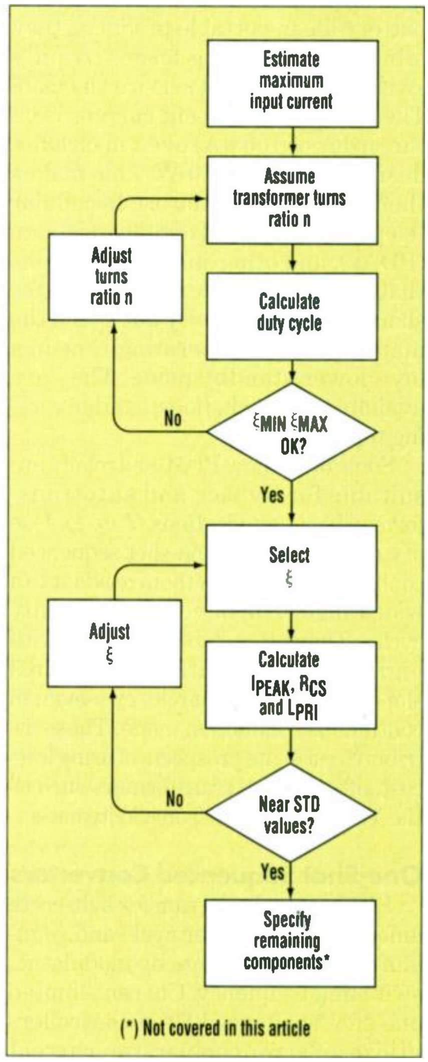
For practical purposes, the following definition puts things into perspective. The Cycle Proportionality Factor is merely a parameter that ensures that the peak switching current and inductor values are consistent with each other for achieving the desired output power. ξ (Xi) is based on the controller and circuit timing characteristics:

$$\xi = \frac{t_{OFF(MIN,IC)}}{t_{ON(CIRCUIT)}} \frac{\delta_{NAT}}{\left(1 - \delta_{NAT}\right)}$$

where δ_{NAT} is the natural duty-cycle or transformer current ramp-up and ramp-down-time duty-cycle based on the circuit voltage specifications and



2. Current-limited one-shot sequenced PFM controllers utilize an error comparator, current-sense comparator, and minimum off-time one-shot and maximum on-time one-shot for feedback and control. This frees them from the timing constraints associated with a traditional gated-oscillator core.



3. A PFM based flyback or autotransformer boost circuit can be designed using ξ in a few easy well-defined steps.

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the transformer turns ratio n:

$$\delta_{NAT(FLYBACK)} = \frac{V_{OUT}}{V_{OUT} + nV_{IN}}$$

and $\delta_{NAT(AUTO\text{-}BOOST)}$

$$= \frac{(V_{OUT} - V_{IN})}{(V_{OUT} - V_{IN}) + (n+1)V_{IN}}$$

ξ is a superset of the ripple current ratio. Values less than 1 represent a circuit with full-load operation in continuous conduction mode. Here, ξ is the transformer primary ripple current ratio $\Delta I/I_{PEAK}$. For values greater than 1, ξ quantifies the dead time in a circuit with full-load operation in discontinuous conduction mode. As a result, ξ offers a basis for determining whether a design is in continuous or discontinuous conduction mode at full load, deriving the relevant design equations and choosing between them.

Introducing Limits ξ_{MIN} And ξ_{MAX}

During design, one simply selects a value for ξ between ξ_{MIN} and ξ_{MAX}. These limits are delineated by the maximum and minimum on-time specifications of the controller IC at the minimum and maximum input voltages, respectively:

$$\xi_{MIN} = \frac{t_{OFF(MIN)}}{t_{ON(MAX)}} \frac{\delta_{NAT(MAX)}}{(1 - \delta_{NAT(MAX)})}$$

and

$$\xi_{MAX} = \frac{t_{OFF(MIN)}}{t_{ON(MIN)}} \frac{\delta_{NAT(MIN)}}{(1 - \delta_{NAT(MIN)})}$$

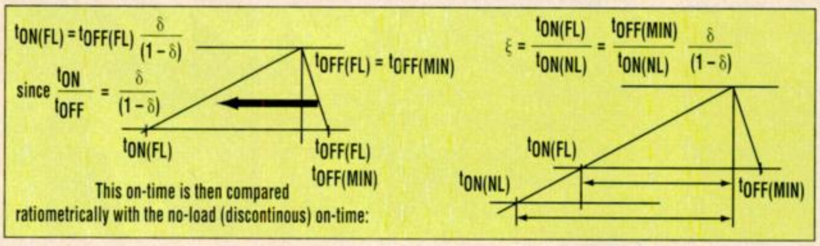
where δ_{MAX} is the natural duty cycle at the minimum input voltage, and δ_{MIN} is the duty cycle at the maximum input voltage.

ξ_{MIN} describes how deep into continuous conduction mode the circuit can operate at the minimum input voltage without bumping into the maximum on-time of the controller IC. The maximum-on-time one-shot forces the MOSFET to switch off and not remain on excessively when the input voltage is abnormally low.

The second limit ξ_{MAX} is a flag indicating when a potential for violating the minimum on-time of the controller IC exists. It is a warning to check that the transformer primary winding inductance not too low. The minimum on-time is a soft limit that describes when operation infringes on the propagation delays of the controller IC. Operating the device with on-times shorter than this can cause

What is ξ?

The Cycle Portionality Factor ξ (Xi) is a ratiometric timing parameter that compares the no-load (discontinuous)* current ramp-up and ramp-down times of the circuit with the full-load timing limits of the PFM controller IC. With one-shot sequenced PFM controller ICs, maximum load occurs at maximum frequency and is limited by the minimum off-time. Therefore, ξ is calculated by first referring the minimum off-time to a corresponding on-time using the circuit duty cycle.



Thus, selecting ξ is equivalent to choosing a no-load on-time normalized to the minimum off-time. The comparative case is discontinuous conduction mode. No-load is just a well-defined occurrence.

**The comparative case is discontinuous conduction mode. No-load is just a well-defined occurence.*

$\xi_{(MIN)}$ AND $\xi_{(MAX)}$ WITH THEIR INTERPRETATIONS, AND SUGGESTED VALUES FOR ξ*

$\xi_{(MIN)}$	$\xi_{(MAX)}$	Meaning	Full-load conduction mode	Response	Suggested ξ
<0.3	>1	OK	Deep in continuous	Maybe reduce n	0.4
$0.3 < \xi_{(MIN)} < 0.6$	>1	Good	Continuous	None	0.7
$0.6 < \xi_{(MIN)} < 1$	>1	OK	Shallow in continuous	Maybe increase n	1
>1	$>\xi_{(MIN)}$	High duty cycle operation**	Discontinuous	Increase n or the minimum input voltage, if practical	$1.2\ \xi_{(MIN)}$ and $<\xi_{(MAX)}$
$<\xi_{(MAX)}$	<1	Low duty cycle operation**	Continuous	Decrease n or the maximum input voltage if possible. Ensure minimum inductance is not violated	$(\xi_{(MIN)} + X_{(MAX)}/2$
$>\xi_{(MAX)}$	$>\xi_{(MIN)}$	Input voltage range is too wide		Narrow the input range	

*ξ is assumed to be $\xi_{(MIN)} \le \xi \le \xi_{(MAX)}$

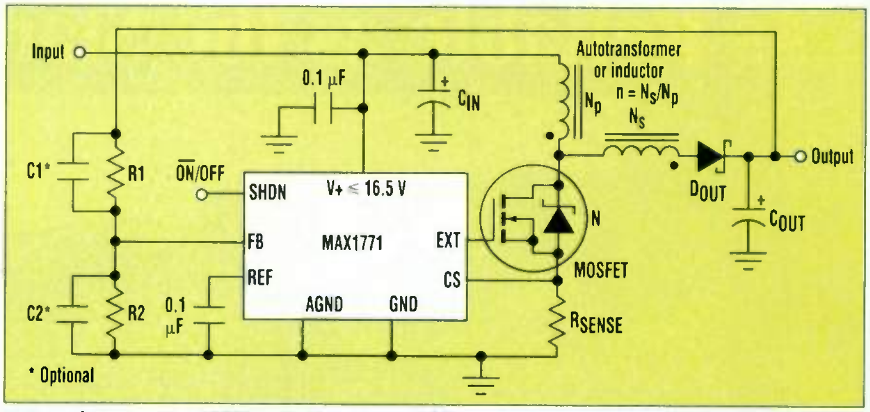
** Operation with high or low duty cycles can require an increased I_{PEAK}.

jitter or difficulty enforcing the peak current limit, especially during overload conditions.

There are no wrong values for ξ assuming the limits ξ_{MIN} and ξ_{MAX} are not violated: there are only trade-offs. High values for ξ shift the design to a lower inductor value and higher peak-switching current. Low values for ξ allow higher output current for a given peak switching current.

This may be an important consideration for designers of high-power circuits. That's because in those design situations, reducing peak switching current improves efficiency and makes thermal design a more-manageable task.

The values ξ_{MIN} and ξ_{MAX} can be used to determine the feasibility of circuit requirements during the initial stages of design and to aid in selection of the transformer (or autotransformer) turns ratio. For example, $\xi_{MIN} > \xi_{MAX}$ implies that the input voltage range is too wide and needs to be narrowed. The table interprets various combinations of ξ_{MIN} and ξ_{MAX} and suggests values for ξ *(see the table)*. Note that where possible, n should less than 5 or greater than 0.2, allowing for use of off-the-shelf transformers.



4. One-shot sequenced PFM controllers are suitable for use in autotransformer boost circuits, such as this one for a 60-V photodiode bias. They can operate over a wide range of duty cycles, allowing implementation for an extreme range of output voltages using low-cost, off-the-shelf commercial transformers.

Easy Design Steps Using ξ (Xi)

It is unnecessary to understand ξ to use it. The following design procedure details how to find the peak switching current and corresponding inductance value for any PFM flyback or autotransformer-boost application using ξ *(Fig. 3)*. Included is an example for a simple battery-powered 60-V 10-mA autotransformer-boost converter for avalanche photodiode bias operating from two NiCd cells *(Fig. 4)*. This example assumes a PFM controller IC with a 2 µs minimum off-time, 1.3-µs minimum on-time and 16-µs maximum on-time. Equations for this and other circuits are listed *(see "Critical Design Equations," p. XXX)*.

1. Estimate Maximum Input Current: Calculate the maximum input current based on the minimum input voltage and desired output power. For a 2-V minimum battery voltage

$$I_{IN,DC(MAX)} = \frac{V_{OUT} I_{OUT(MAX)}}{\eta_{NOM} V_{IN(MIN)}} = \frac{60\ V \times 10\ mA}{0.75 \times 2\ V} = 400\ mA$$

where η_{NOM} is the nominal efficiency. Initially assume 80%, or 75% for low-voltage applications (V_{IN} or $V_{OUT} < 5$ V).

2. Assume an Initial Secondary/Primary Transformer Turns Ratio "n": The precise secondary/primary turns ratio is not important in flyback and boost converters. Integer-based turns ratios within the 5/1 to 1/5 range, such as 1/5, 2/4, and 3/3, are preferred since they allow the use of off-the-shelf transformers. With boost converters n = 0 represents use of an ordinary inductor, n = 1 represents use of a 1:1 autotransformer, etc. A suggested range of values for the autotransformer boost converter example is:

$$n \approx \sigma\left(\frac{V_{OUT} - V_{IN}}{V_{IN}}\right) - 1$$

$$= (0.13 \text{ to } 0.15)\left(\frac{60\ V - 2.4\ V}{2.4\ V}\right) - 1$$

$$= 2.1 \text{ to } 35$$

Critical Design Equations

Here's a pallet of PFM flyback and autotransformer-boost design equations not listed in the main article text. However, refer to the article for variable and constant definitions.

Suggested transformer turns ratio for flyback converters:

$$n = \sigma \frac{V_{OUT}}{V_{IN}}$$

Flyback peak switching current for continuous and discontinuous conduction modes respectively:

$$I_{IN,PEAK} = I_{IN,DC(MAX)} \frac{2}{\delta_{NAT(MAX)}(2-\xi)}$$

$$I_{IN,PEAK} = 2I_{IN,DC(MAX)}\left(1 + \xi\frac{(1-\delta_{NAT(MAX)})}{\delta_{NAT(MAX)}}\right)$$

Autotransformer boost peak switching current in continuous conduction mode:

$$I_{IN,PEAK} = I_{IN,DC(MAX)} \frac{2}{(2-\xi)} \frac{1}{\delta_{NAT(MAX)} + (1-\delta_{NAT(MAX)})/(n+1)}$$

where σ is a rough-range parameter based on the timing specifications of the controller IC.

$$\frac{t_{OFF(MIN)}}{t_{ON(MAX)}} = \frac{2\ \mu s}{16\ \mu s} = 0.13 \le \sigma \le 1.5$$

$$= \frac{2\ \mu s}{1.3\ \mu s} = \frac{t_{OFF(MIN)}}{t_{ON(MIN)}}$$

In this case, we are ignoring the suggestion to try a solution using n = 1 to take advantage of an off-the-shelf 1:1 transformer, such as the Coiltronics Octa-Pac series. Using ξ will let us get away with this.

3. *Calculate the Resulting Natural Duty Cycles:* Compute the maximum, typical and minimum duty cycles for operation at the minimum, typical and maximum input voltages respectively. For the n = 1 autotransformer circuit example, they are:

$$\delta_{NAT(MAX)} = \frac{(V_{OUT} - V_{IN(MIN)})}{(V_{OUT} - V_{IN(MIN)}) + (n+1)V_{IN(MIN)}}$$

$$= \frac{(60\ V - 2.0\ V)}{(60\ V - 2.0\ V) + (1+1)2.0\ V} = 93.5\%$$

$$\delta_{NAT(MAX)} = 93.5\%,\ \delta_{NAT(TYP)} = 92.3\%$$

$$\delta_{NAT(MIN)} = 87.5\%$$

where the minimum, typical and maximum input voltages are 2 V, 2.4 V, and 4 V, respectively.

4. *Interpret ξ_{MIN} and ξ_{MAX}:* Calculate ξ_{MIN} and ξ_{MAX} and then interpret the results using the table as a guide. If the turns ratio is adjusted as recommended in the table, recalculate using the new duty cycles.

$$\xi_{MIN} = \frac{t_{OFF(MIN)}}{t_{ON(MAX)}} \frac{\delta_{NAT(MAX)}}{1-\delta_{NAT(MAX)}}$$

$$= \frac{2\ \mu s}{16\ \mu s} \frac{0.935}{1-0.935} = 1.80$$

$$\xi_{MAX} = \frac{t_{OFF(MIN)}}{t_{ON(MIN)}} \frac{\delta_{NAT(MIN)}}{1-\delta_{NAT(MIN)}}$$

$$= \frac{2\ \mu s}{1.3\ \mu s} \frac{0.875}{1-0.875} = 10.8$$

By interpreting the results using the table as a guide, we see that the circuit operates in discontinuous conduction mode at full-load near the minimum input voltage. A higher peak switching current will be needed to compensate. This is the consequence of the trade-off made in Step 2.

5. *Choose ξ:* Simply select a value for ξ between ξ_{MIN} and ξ_{MAX}. Following the suggestions in the table yields a value of 2.16 for the autotransformer boost example.

6. *Determine the Peak Switching Current:* Choose the correct equation for the peak switching current using the selected value for ξ as a guide. Since ξ ≥ 1, use the autotransformer-boost equation for operation in discontinuous conduction mode:

$$I_{IN,PEAK} = 2I_{IN,DC(MAX)} \frac{\delta_{NAT(MAX)} + \xi(1-\delta_{NAT(MAX)})}{\delta_{NAT(MAX)} + (1-\delta_{NAT(MAX)})/(n+1)}$$

$$= 2 \times 0.400\ A \frac{0.935 + 2.16(1 - 0.935)}{0.935 + (1 - 0.935)/(1+1)}$$

$$= 889\ mA$$

Note that use of ξ in the discontinuous conduction mode equation has automatically compensated for the trade-off in Step 2 by increasing the peak switching current to allow use of an off-the-shelf n = 1 transformer. When selecting a current sense resistor based on this peak current, select a standard value less than calculated for a higher peak current.

$$R_{CS} = \frac{V_{CS(MIN)}}{I_{IN,PEAK}} = \frac{0.085\ V}{0.889\ A} = 0.096\ \Omega$$

where $V_{CS(MIN)}$ is the minimum current sense threshold for the controller IC selected.

7. *Specify the Primary Inductance:* Select a primary inductance such that $L_{PRI(MIN)} \le L_{PRI} \le L_{PRI(MAX)}$, where:

$$L_{PRI(MIN)} = \frac{V_{IN(MAX)} t_{ON(MIN)}}{I_{IN,PEAK}}$$

$$= \frac{4\ V \times 1.3\ \mu s}{0.889\ A} = 5.85\ \mu H$$

$$L_{PRI(MAX)} = \frac{V_{IN(MIN)} t_{ON(MAX)}}{I_{IN,PEAK}}$$

$$= \frac{2\ V \times 16\ \mu s}{0.889\ A} = 36.0\ \mu H$$

Select a standard value greater than or equal to:

$$L_{PRI} = \frac{V_{IN(MIN)} t_{OFF(MIN)}}{I_{IN,PEAK}\xi} \frac{\delta_{NAT(MAX)}}{(1-\delta_{NAT(MAX)})}$$

$$= \frac{2\ V \times 2\ \mu s}{0.889\ A \times 2.16} \frac{0.935}{(1-0.935)} = 30.0\ \mu H$$

The closest standard value, 33 µH, should work fine.

When connecting N_{PRI} windings of a pin-configurable transformer in series, note that the inductance increases as N_{PRI}^2 and the saturation current rating decreases as $1/N_{PRI}$. Connecting windings in parallel results in no change from the single winding inductance or single-winding saturation current rating, although the rms current rating increases due to reduced resistance. The saturation current rating must exceed the worst-case peak switching current:

$$I_{SAT} > I_{IN,PEAK(MAX)} = \frac{V_{CS(MAX)}}{R_{CS}}$$

$$= \frac{0.120\ V}{0.096\ \Omega} = 1.25\ A$$

There are no wrong values for ξ assuming the limits ξ_{MIN} and ξ_{MAX} are not violated. If the resulting current-sense resistor and inductance values are impractical, then nudge ξ as needed to bring the circuit in sync with available values. Now that the peak switching current and transformer turns ratios are known, the rest of the components can be selected. Since this is beyond the scope of this article, we will end here. For a full set of design procedures and examples showing how to calculate specifications for all of the components, contact the Applications Engineering Department at Maxim Integrated Products.

Advantages Of Using ξ (Xi)

Use of the new Cycle Proportionality Factor ξ (Xi) eases the process of PFM controlled flyback and autotransformer boost design by offering a well-defined design procedure and answers to seven key design questions:

1. Is the input voltage range excessive? *Answer:* Whenever $\xi_{MIN} > \xi_{MAX}$.
2. What transformer turns ratios can be used and what values are optimal? *Answer:* Interpret ξ_{MIN} and ξ_{MAX} using the table.
3. Does the design operate in continuous or discontinuous conduction mode at full load? *Answer:* Is ξ less or greater than 1?
4. In a discontinuous conduction mode design, how much must the peak switching current be increased to

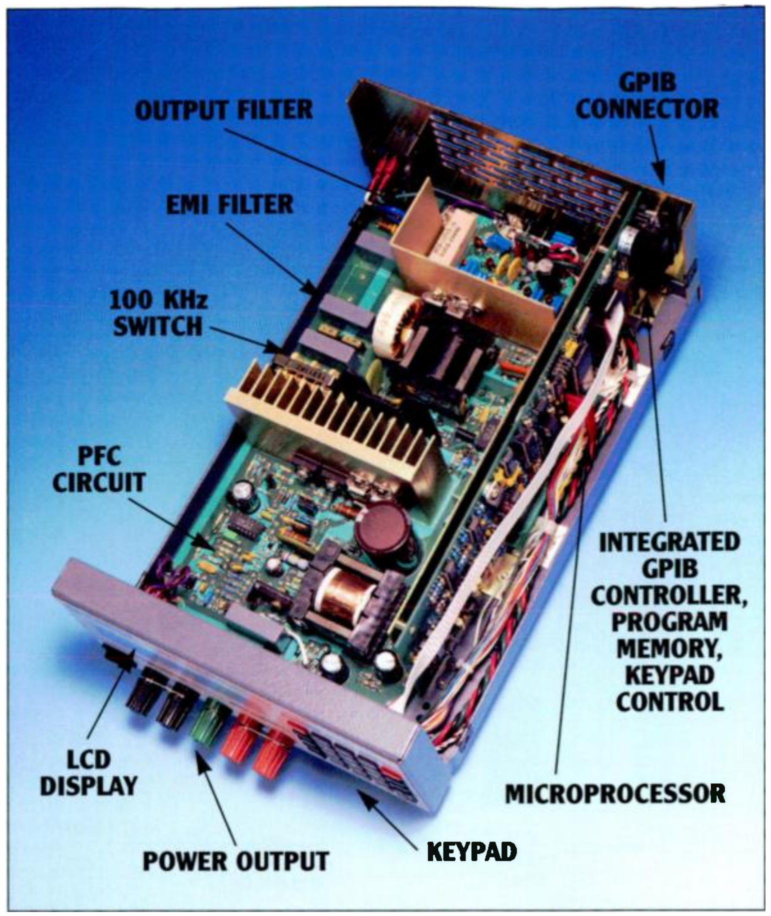
TEAR ON DOTTED LINE TO REMOVE AND SAVE

SERIES ABC

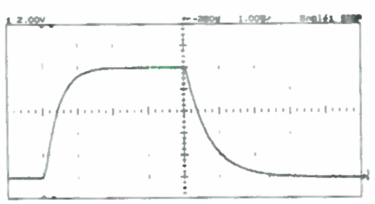
Kepco's ABC bench power supply embodies features like high frequency switch-mode conversion, wide range input (85-264V a-c) and power factor correction. It meets the EN 61000-3-2 harmonic limits and does not disturb the other instruments on your bench. A built-in EN 55022 class B input EMI filter means it is at home in your home or lab. It sits silently on your work bench and produces clean d-c.

Six different models are available from 0-10V at 10A to 0-125V at 1A. Hook it up to a GPIB controller and your ABC power supply integrates into a test system. The ABC is shipped with an instrumentation software driver using VISA* I/O to facilitate integration.

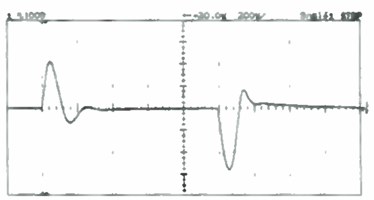
* Virtual Instrumentation Software Architecture (requires the installation of the 16-bit VISA driver from the GPIB card supplier.)



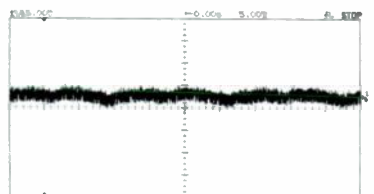
Inside View of Model ABC 10-10DM



Trace showing typical programming speed for 0-100% voltage,full load
Vertical 2.00V/division
Horizontal 1 ms/division



Trace showing typical recovery of output voltage when load is step-changed 50-100%
Vertical 100 mV/division
Horizontal 200 µs/division



Trace showing typical output ripple at full load
Vertical 5 mV/division
Horizontal 5 ms/division

ABC MODEL TABLE

MODEL	d-c OUTPUT			RIPPLE AND NOISE (mV) p-p						EFFICIENCY
	RANGE		POWER	2x SOURCE FREQUENCY		SW FREQUENCY		SPIKE (50 MHz)		100% LOAD 85-264V a-c
	VOLTS	AMPS	WATTS	TYP	MAX	TYP	MAX	TYP	MAX	% MIN
ABC 10-10DM	0-10	0-10	100	2	4	2	4	3	6	65%
ABC 15-7DM	0-15	0-7	105	3	6	3	6	4	8	66%
ABC 25-4DM	0-25	0-4	100	5	10	5	10	5	10	66%
ABC 36-3DM	0-36	0-3	108	7	15	7	15	7	15	67%
ABC 60-2DM	0-60	0-2	120	12	24	12	24	12	24	68%
ABC 125-1DM	0-125	0-1	125	25	50	25	50	25	50	70%

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ABC INPUT CHARACTERISTICS

SPECIFICATIONS		RATING/DESCRIPTION	CONDITION
a-c Voltage	nominal	100/120/220/240V a-c	Single phase
	range	85-264V a-c	Wide range
Frequency	nominal	50-60Hz	>63Hz Input leakage current exceeds spec
	range	47-63Hz (400Hz)	
Current	85V a-c	1.8A(1)	Maximum at 100W output
	120V a-c	1.3A(1)	
	240V a-c	0.65A(1)	
	264V a-c	0.60A(1)	
Initial turn-on surge		5A peak for less than 150 usec	85-264V a-c 0-100% load
Power factor	min	120V 0.97 240V 0.93	100% load
EMC immunity to:			
	Radiated RF	EN 61000-4-3	level 3
	Magnetic field	EN 61000-4-8	level 4
	Electrostatic discharge	EN 61000-4-2	level 2 4KV contact level 3 8KV air discharge
	Conducted RF	EN 61000-4-6	level 3
	Electrical fast transient	EN 61000-4-4	level 3
	Surges	EN 61000-4-5	level 4
EMC emissions:	Conducted	EN 61000-3-2	Harmonics (0-2 KHz)
		EN 6100-3-3	Fluctuation & Flicker
		EN 55022 Class B	0.15~30 MHz
	Radiated	EN 55022 Class B	30~1000 MHz
Leakage current	120V a-c	<0.25mA	Source frequency in 47-63Hz range
	240V a-c	<0.5mA	

(1) Input current for 100W output. For the 120W ABC 60-2M and 125W ABC 125-1M the output current is proportionally higher.

ABC OUTPUT CHARACTERISTICS

SPECIFICATIONS		RATING/DESCRIPTION	CONDITION
Type of stabilizer		Automatic crossover	Voltage/Current
Adjustment range		0 to 100%of rating	Voltage/Current
Source effect	Voltage	<0.01% E_O max	Nominal ± 15% of input voltage
	Current	<0.01%I_O max	
Load effect	Voltage	<0.01% E_O max	0 to 100% load change
	Current	<0.02%I_O max	
Temperature effect	Voltage	<0.01% E_O max	Per degree C (0 to 50°C)
	Current	<0.01%I_O max	
Time effect	Voltage	<0.01% E_O max	0.5-8.5 hours
	Current	<0.01%I_O max	
Error sense		0.5V per wire	Voltage allowance
Isolation voltage		500V d-c or peak	Output to ground
Programming time		2ms max	0-100%
Programming accuracy	Voltage	0.025% E_O max	
	Current	0.1%I_O max(1)	
Readback/Display accuracy	Voltage	0.05% E_O max	
	Current	0.1%I_O max	
Transient recovery to load change	Excursion	<5% E_O max	50%-100% load change return to 1% E_O max
	Recovery	<200 usec	
Overshoot		None	Turn ON/OFF
Data entry	Local	24 key keypad	Front panel
	Remote	GPIB (IEEE 488.2)	SCPI commands

(1) ABC 25-4DM: 0.05%; ABC 36-3DM, ABC 60-2DM and ABC 125-1DM: 0.025%

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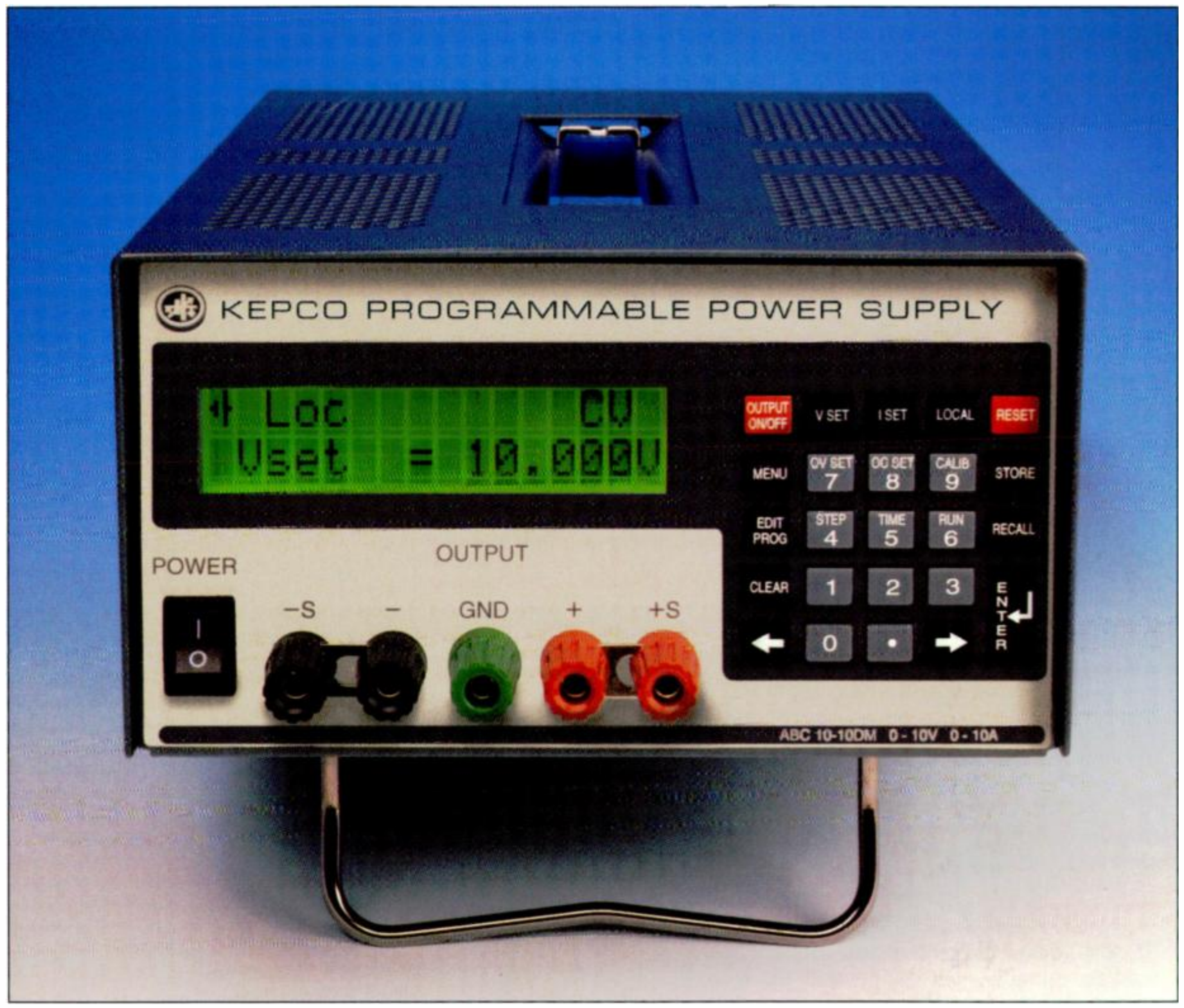
Kepco's new GPIB Keypad-controlled 100W Power Supply



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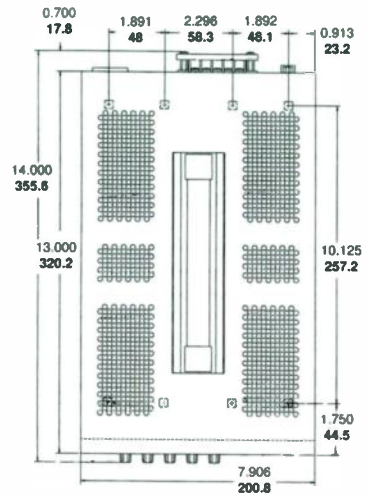
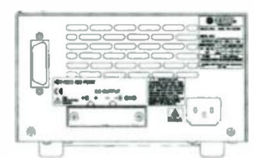


TOP VIEW



REAR VIEW

Rack Adapters: 5 1/4" x 19"
RA 71 1 unit ABC
RA 72 2 units ABC

ABC GENERAL (ENVIRONMENTAL) SPECIFICATIONS

SPECIFICATIONS		RATING/DESCRIPTION	CONDITION
Temperature	Operating	0° to +50°C	No derating 100%P_O max
	Operating	+50°C to +70°C	Linear derating to 40%P_O max
	Storage	-40° to +85°C	
Humidity		0 to 95% RH	Non condensing operating & storage
Shock		20g, 11msec ±50% half sine	3-axes 3 shocks each axis
Vibration		5-10Hz 10mm double amplitude	Non operating, 1 hour each axis
		10-55Hz 2g	
Altitude		Sea level to 10,000 ft	
Cooling		Natural convection	

ABC PHYSICAL CHARACTERISTICS

SPECIFICATIONS		RATING/DESCRIPTION	CONDITION
Dimensions	English	7.9" x 4.9" x 14"	±1/32"
	Metric	200.8 x 124.6 x 355.6 mm	±0.8 mm
Weight	English	11 lbs.	Unpacked
	Metric	5 Kg	
a-c input connections	Front	Panel ON/OFF switch	
	Rear	Detachable IEC 320 type connector	3 wire fused
Output local connections	Front	5 binding posts	±Output; ±Sense; Ground
	Rear	5 terminal barrier strip	
Remote control programming		One standard GPIB connector	Rear SCPI & IEEE 488-2 commands
Digital display front panel		Voltage, current, mode, status, menu, program,	2 x 16 character alphanumeric LCD with LED backlight
Rack adapters		5 1/4" x 19"	RA 71 1 unit ABC RA 72 2 units ABC

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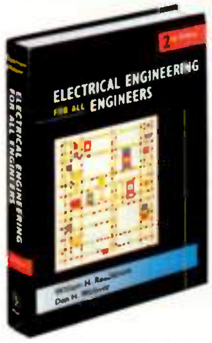

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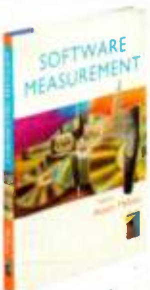

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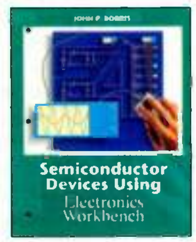
Semiconductor Devices Using Electronics Workbench

John P. Borris



This simulation manual is ideal for use with an introductory electronics text. Easy-to-use exercises instruct the first-time user of Electronics Workbench on the use of this software and review Resistor-Capacitor-Inductor (RCL) circuit applications. Topics include rectifier and zener diodes, various biasing techniques used in transistor amplifier circuits, Junction Field Effect amplifiers, troubleshooting exercises and more. Appendix contains equivalent circuits to supplement the chapters on amplifiers.

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compensate for the dead time? *Answer:* Calculate $I_{IN,PEAK}$ using ξ.

5. How deep into continuous conduction mode can the design be pushed without violating the maximum on-time of the controller IC? *Answer:* The limit is defined by ξ_{MIN}.

6. When must one pay attention to ensure the minimum on-time is not violated? *Answer:* When $\xi_{MAX} < 1$, or ξ approaches ξ_{MAX}.

7. What trade-offs can be made when designing for standard component values; or when trading off component size, cost and availability? *Answer:* Adjust n and ξ and then examine the corresponding changes in component specifications.

Application of the Cycle Proportionality Factor ξ (Xi) can reduce design time and development costs by reducing experimentation required in the lab and money expended purchasing components for the initial prototype. It does this by offering a well-defined procedure suitable for design of an initial prototype, as well as a basis for computer-aided design. Potential problems with the input voltage range and transformer secondary/primary turns ratio can be evaluated before time and money are expended ordering and trying custom or off-the shelf transformers.

For brevity, this article focused specifically on using ξ with PFM controllers in flyback and autotransformer boost circuits. This same analytical approach has been applied to PWM controllers and all basic switching-power-supply technologies. Adapting the approach required deriving the corresponding PWM definition of ξ and peak-switching-current equations.

Darryl Phillips is a member of the technical staff at Maxim Integrated Products. He holds a BSEL from California Polytechnic State University, San Luis Obispo.

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CONFERENCE PREVIEW

Technical Sessions At ITC '97 Look To Tackle Mixed-Signal Test

Testing Of Mixed Analog And Digital Circuits Takes Center Stage, But Design-For-Test. Built-In Self-Test, And Multichip Modules Also Share The Spotlight.

John Novellino

Microcontrollers are finding their way into more systems these days. Once inside, they usually encounter the analog signals that represent real-world movements and environmental changes. Increasingly, this mixture of digital and analog signals is taking place on one IC. Recognizing this strong growth in mixed-signal circuitry, the 1997 International Test Conference (ITC '97) has adopted mixed-signal test as its theme. Four technical sessions grouped together as a one-day track, a panel session, and a tutorial session support the conference's emphasis on mixed-signal test.

With 40 technical sessions and 10 panel sessions, as well as 16 tutorials and three workshops outside the normal conference schedule, ITC '97 and the larger event known as "Test Week" have something for almost every engineer involved in test issues *(see the program grid)*. Among the prominent issues to be covered are design-for-test (DFT), built-in self-test (BIST), multichip modules (MCMs), and quiescent current testing (I_{DDQ}). All have been hot topics for some time and will continue to be for the foreseeable future. In addition, a pair of lecture series each feature two back-to-back lecture sessions. One series covers unpowered opens testing; the second looks at diagnosis and failure analysis.

The conference and its associated exhibition will be held at the Sheraton Washington Hotel, Washington, D.C., Nov. 3-5. Tutorials are scheduled for Nov. 1 and 2, while the three workshops run concurrently on Nov. 5 after the conference sessions have been completed and all day on Nov. 6.

The conference's coverage of mixed-signal testing begins Monday night with Panel Session 1, "The top 10 mixed-signal test issues." Five panel members will each present their three biggest mixed-signal test problems and solicit other concerns from the audience. At the end of the discussion, an audience vote will determine the top 10. Organizers hope to identify new areas for research, market opportunities, and possibly ITC '98 papers.

Tuesday's sessions feature a full day of mixed-signal issues, starting with Session 16, "Mixed-signal measure-

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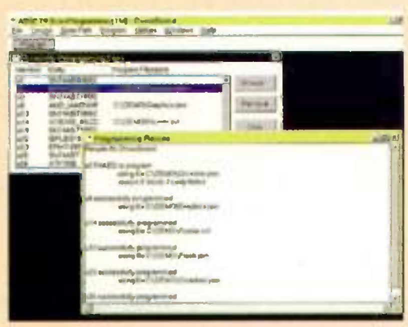
MemoryConnect is a product that automates the interconnect testing of memory arrays that do not include a boundary-scan interface. Increasing interconnect test coverage on a pc-board is one way to decrease overall manufacturing costs. But test coverage is often limited because most DRAMs and SRAMs are not boundary-scan compatible. MemoryConnect uses a board's boundary-scan test channel to verify the integrity of address, data, and control lines between memories and other boundary-scan devices. It thus eliminates the need to generate many test vectors. The product also automatically provides net-level diagnostics for any memory interconnect faults found. A future product, MemoryDirect, will supply pin-level diagnostics. MemoryConnect is the first



product to result from a joint development program between Asset InterTech and LogicVision Inc. It is available now for $14,995.

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ment techniques." Scheduled papers include "Dynamic testing of ADCs using wavelet transforms," "A simplified polynomial-fitting algorithm for DAC and ADC BIST," and "Signal generation using periodic single- and multi-bit sigma-delta modulated streams."

Mixed-Signal Bus Examined

The following two sessions in the track take on the emerging IEEE-P1149.4 Mixed-Signal Test Bus Standard. Session 21, "Measurements using P1149.1," includes papers on "Design, fabrication, and use of mixed-signal testability structures," "Parasitic effect removal for analog measurement in P1149.4 environment," and "Implementation of mixed-signal current and voltage testing using the IEEE-P1149.4 infrastructure." This is followed by another panel discussion, Session 26, "On-chip 1149.4, what for?" Organizers note that IEEE-P1149.4 is an attempt to bring structure to mixed-signal test strategies that some designers see as the only way to manage the increasing demands of ever more complex mixed-signal circuitry. Others, however, say the proposed standard doesn't address developers' problems. Panel members will discuss the status of on-chip P1149.4 and debate its merits.

Wrapping up the track is Session 31, "Mixed-signal BIST/DFT." Papers will discuss histogram-based analog BIST, current-based analog scan, BIST for functional and structural testing of analog and mixed-signal ICs, and on-chip measurement of the jitter-transfer function of charge-pump PLLs.

For those willing to arrive two days before the conference (and pay an additional registration fee), a Saturday tutorial will cover "Metrics, techniques, and new developments in mixed-signal testing." The session runs from 8:30 a.m. to 4:30 p.m., as do the other tutorials. The tutorial will review the basics of analog and digital circuits and how manufacturing defects influence their behavior. Standard test techniques for sinusoidal-based and time-domain testing will be discussed, including how digital sampling techniques can be used to perform sinusoidal-based tests on continuous-time signals. Other issues to be addressed are noncoherent and coherent sampling, multitone testing, noise testing, and DFT methods currently under development.

The lecture series on diagnosis and failure analysis includes a panel discus-

1997 INTERNATIONAL TEST CONFERENCE

			Monday November 3		
8:30-10:30 a.m.	Plenary Session Keynote address: James T. Healy, president and CEO, Genus Corp.; Invited address: Colin Maunder, BT Laboratories				
1:30-3:00 p.m.	Session 2 Dynamic current testing	Session 3 Embedded core testing	Session 4 ATE hardware improvements for high-speed test	Session 5 MCM systems test	Session 6 Lecture series: Unpowered opens testing
3:30-5:30 p.m.	Session 7 I_{DDQ} testing	Session 8 Progress on standards and benchmarks	Session 9 Memory test	Session 10 Test synthesis	Session 11 Lecture series: Unpowered opens testing
8:00-9:30 p.m.	Panel 1 The top 10 mixed-signal test issues	Panel 2 Partial scan is dead, long live almost-full scan	Panel 3 Ethics, professionalism, and accountability—Does it exist in test?	Panel 4 Vision systems for board test: Meeting their promise?	Panel 5 How can we test chips that mix logic and DRAM?
			Tuesday, November 4		
8:30-10:00 a.m.	Session 12 Microprocessor test I	Session 13 Lecture series: Diagnosis and failure analysis	Session 14 Deterministic BIST	Session 15 Components for MCMs: Known-good die and substrates	Session 16 Mixed-signal measurement techniques
10:30 a.m.-Noon	Session 17 Microprocessor test II	Session 18 Lecture series: Diagnosis & failure analysis panel	Session 19 Design for delay test	Session 20 Concurrent checking	Session 21 Measurements using P1149.4
1:30-3:00 p.m.	Session 22 High-performance probes and sockets	Session 23 BIST and DFT economics	Session 24 On-line testing techniques for VLSI	Session 25 Defect behavior, test efficiency, and fault-model extension	Session 26 Mixed-signal panel
3:30-5:30 p.m.	Session 27 Board-level test methods	Session 28 Software for new test strategies	Session 29 Design-for-test topics	Session 30 Putting the squeeze on test sequences	Session 31 Mixed-signal BIST/DFT
			Wednesday, November 5		
8:30-10:00 a.m.	Session 32 Test engineering topics	Session 33 Tools and techniques for defect	Session 34 Specialized BIST generators	Session 35 Advances in digital logic diagnosis	Session 36 Fault modeling
10:30 a.m.-Noon	Session 37 New frontiers in test	Session 38 Design verification and diagnosis	Session 39 Delay fault testing	Session 40 Test language standards	Session 41 Advances in probe technology from the '97 Southwest Test Workshop
1:30-3:00 p.m.	Panel 6 So what is an optimal test mix? A discussion of the Sematech methods experiment	Panel 7 Embedded core test plug-and-play: Is it achievable?	Panel 8 On-line testing: Industrial practice and perspectives	Panel 9 Contract manufacturers' role in board test evolution	Panel 10 Subcontract test—New frontiers or new problems for the IC industry?
	Workshops begin: Fifth International Workshop On The Economics Of Design, Test, And Manufacturing IEEE International Workshop On I_{DDQ} Testing First IEEE International Workshop On Testing Embedded Core-Based Systems				
			Thursday, November 6		
	Workshops continue				

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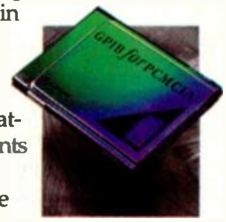

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sion (Session 18) with the provocative title, "Logic diagnosis: Potential yield-improvement driver of occasional entertaining diversion?" According to the panel, memory array diagnosis can be highly automated because cell failures often suggest exact failure coordinates. But logic diagnosis requires time-consuming failure data logging and off-line processing to localize the failure. As the session description puts it, "Will logic diagnosis ever be automatable to the point that it can be included in manufacturing testing, or is that a hopeless cause?"

Pointed Panels

The ITC panel discussions are always interesting, and this year's group should be no exception. Panel 2's title states, "Partial scan is dead. Long live almost-full scan." In the early 1990s, advances in sequential test generation and numerous ideas on how best to select scan flip-flops seemed to make partial scan feasible for very large designs, according to the session's description. And the promise of lower area and performance penalties lured many traditionally non-scan designer groups to adopt partial (less than 50%) scan. But the unpredictability of sequential test-pattern generation seems to have moved designers to near-full scan. The panel intends to examine the issues involved and pass a verdict.

And speaking of provocative, how's this: "Ethics, professionalism, and accountability—Does it exist in test?" The description of the session (Panel 3) puts it very simply. "If we are not testing 100% and we know it and we know of techniques to improve test quality which we don't apply, is this ethical, let alone sue-able? Who is ultimately accountable?"

The integration of DRAMs into logic chips has created new test challenges

50-MHz Tester-Per-Card System For Flash Memories

The KALOS test system is the first flash memory tester to employ a "tester-per-card" architecture. Designed specifically to address the most rapidly growing segment of the IC memory industry, the KALOS system provides an independent 50-MHz tester behind each device under test. Because of its high level of integration and parallel test capability, the tester requires only 1 m^2 of floorspace. Up to 16 flash memory devices can be tested in parallel in wafer-sort or final-test applications. Each of the 16 test cards has 48 I/O pins. Production shipments of the KALOS system are scheduled for March 1998. Call the company for price information.

***Credence Systems Corp.**, 215 Fourier Ave., Fremont, CA 94539; (510) 657-7400; fax (510) 623-2560.*
CIRCLE 548
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Memory BIST Tool Handles Many Types And Configurations

Sunrise MemBIST is a design tool for adding built-in self-test (BIST) to various embedded memories, including SRAM, DRAM, and ROM. It is based on patented, next-generation technology that provides fault diagnosis, built-in self-repair, and algorithm programmability needed to test memories in complex ICs.

Using Sunrise MemBIST, design engineers select the characteristics of their embedded memory through a graphical-user interface. The tool then automatically generates register transfer level (RTL) code for the logic blocks in the memory BIST framework structure. The RTL code is automatically verified with an included test bench, then synthesized using a commercial design synthesis tool. Direct links verify the logic function and timing using the company's Chronologic VCS and Motive tools, respectively.

Different memory test algorithms are needed to ensure complete defect coverage, depending on memory type and circuit implementation of the cells. To accommodate these differences, the tool offers 12 built-in algorithms and an option for defining proprietary custom test algorithms. Users can specify any configuration—single-port, dual-port, multiport, synchronous, or asynchronous—and can specify all controls and read/write timing memories. Also available are test features in the BIST logic for ATPG testing of the embedded memory's shadow logic.

The ability to deliver full diagnostic information permits users to determine all failing data bits and addresses. This fault-isolation information is also important for memory repair, which is desirable in large embedded DRAMs.

Sunrise MemBIST was developed in partnership with Heuristic Physics Laboratories, Milpitas, Calif. It is fully integrated with into the TestGen suite of tools. Prices for a single floating license with unlimited usage start at $40,000.

***Viewlogic Systems Inc.**, 293 Boston Post Rd. West, Marlboro, MA 01752-4615; (508) 480-0881; fax (508) 480-0882; http://www.viewlogic.com.*
CIRCLE 549
Booth 201

because DRAM and logic semiconductor processes, test methods, and test equipment have traditionally been distinct. Panel 5 addresses the question, "How can we test chips that mix logic and DRAM?" Members will look for solutions currently available.

So Much To Choose From

With the proliferation of test techniques now available, designers are often left wondering which method, or combination of methods, is right for their next project. Panel 6 should offer some help. Sematech sponsored a multi-year test-methods study that collected detailed test data on a large number of sample parts from one of the consortium's member companies. The methods compared were scan-based stuck-at, scan-based transition delay, full-pin functional, and I_{DDQ}. Panel members will present the results of this study and recommend an optimum test mix.

The strong growth in embedded core-based systems has prompted the addition of a third workshop to Test Week. The First IEEE Workshop on Testing Embedded Core-Based Systems aims to solve the increasing problems of effectively testing the individual core or system-on-a-chip. The session will bring together core creators, integrators, and manufacturers in an informal forum for presenting and discussing the latest developments in test. (Workshops require an additional registration fee.)

In addition to the workshop, Panel 7 also looks at testing of embedded cores. The panel notes that combining the distinct tests of different cores into a single chip-level test is becoming a major challenge and examines whether and how cores can be made with plug-n-play tests.

The longest running of the three is the Fifth International Workshop on the Economics of Design, Test, and Manufacturing, which will explore current and future trends and how they are driven by the economics of delivering increasingly complex electronic systems. The workshop will focus on the economic impact of decisions directly associated with the design, manufacturing, test, and field maintenance of electronic devices, multichip modules, boards, and systems.

Back for its third year is the IEEE International Workshop on I_{DDQ} Testing. Organizers note that I_{DDQ} testing is used to screen many ICs and has made significant inroads in analog and mixed-signal testing. The theme of this year's event is "Testing for reliability faults of submicron ICs." Topics will include all aspects of current testing, defect coverage, test vector selection, built-in current sensing, and current sensors.

I_{DDQ} also is the focus of Session 7, which will include papers on using the technique on submicron and deep submicron, low-power CMOS ICs. Other papers discuss I_{DDQ} test for automotive products and an application involving current signatures.

Dual Keynotes

ITC '97 features two keynote addresses to be delivered by James T. Healy, president and CEO of Genus Corp., and Colin Maunder of BT Laboratories. Healy's address will look at how commonality in terms of design rules, architecture, and fabrication processes will become easier as CMOS devices take over from bipolar. The result will be a favorable environment for the development of a single design, monitor, and test network. Healy predicts that cooperation between manufacturers of design tools, process diagnostic equipment, and automated test equipment will create a path to the "known-perfect device."

Maunder's talk will examine humankind's increasing dependence on electronic machines. He notes that in many cases computers, fax machines, mobile phones, and other devices no longer enhance our working lives but instead form the basis of our jobs. That is, if they don't work, neither do we. And this dependence will continue to grow, not only in the workplace but also at home. "So how will increasing dependence impact the design and test of electronic products?" asks Maunder. His keynote will discuss how society's relationship with, and expectations of, electronics might change and pose some challenges for the test engineering community.

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If you're designing wireless communications devices, we're the antenna and battery pack specialist you need.

LAN/WAN Interfaces: Plugging Into The Cloud

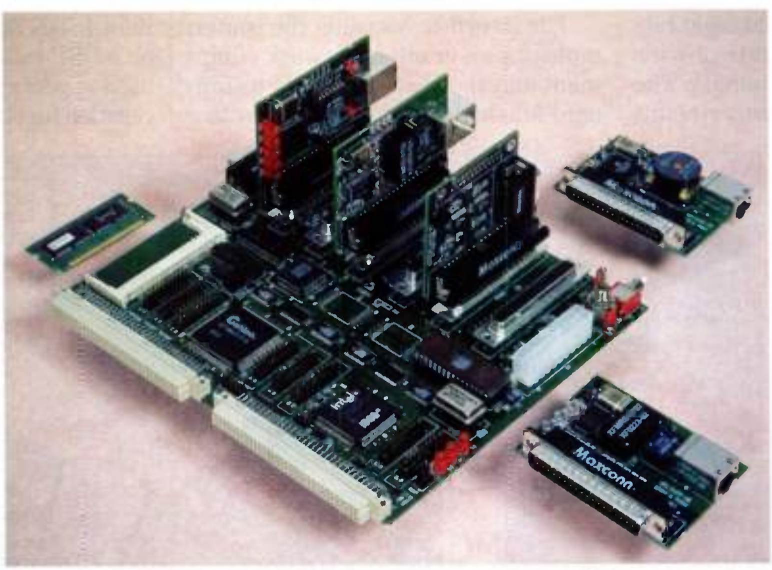
Today's Distributed Organizations Rely On Webs of T1, ISDN, And ATM To Tie Their Branch And Home Offices Together. This Has Created A Huge Market For Chips, Boards, And Boxes That Bridge The LAN/WAN Gap.

Lee Goldberg

SPECIAL REPORT

The LAN/WAN (local-area network/wide-area network) interface has emerged as one of the most lively frontiers in the communication universe. Within the past five years, high-speed data connections have become as indispensable to the modern methods of work and commerce as telephones were earlier this century.

While the personal computer and LAN technology has changed how *people* work, its recent fusion with WAN technology is revolutionizing how *organizations* work. Just as LANs have increased individual productivity by linking computers, servers, and other resources together within an office, the humble router has given WANs the power to tie organizations together, across states, continents, and even UPS delivery zones.



Art Courtesy: Galileo Technologies

WANs Go Public

This trend began during the late eighties, when LANs were in their infancy and high-speed data connections were almost solely used by large corporations to tie their mainframe computers together. Typically, these were costly, dedicated leased analog or digital lines, connected at each end by cabinets full of multiplexers, modems, and customer premises equipment (CPE) to handle the network interface.

During this time, the proliferation of servers, Ethernet, and token-ring networking products has made it possible for even the smallest office to enjoy many of the services (high-speed printers, centralized databases, e-mail, etc.) previously available only in large corporate offices.

PCs and the early LANs made it feasible for companies to spin-off small, efficient branch offices that could be located closer to their clients. Of course, information-intensive enterprises, like insurance, banking, car rental, and most sales functions required close connection with the parent company's computing resources.

As a result of this demand (as well as big changes in telecommunication tariff regulations), many less expensive options for inter- and intra-city data connections became available. Large closets full of equipment began to be replaced by routers that could divert portions of LAN traffic across the public network to other LANs or to the Internet.

During the past five years, the wider selection of reasonably priced public data services allowed smaller businesses to venture on to the WAN (*Fig. 1*). This in turn opened up the market for entirely new classes of relatively inexpensive WAN interface equipment for smaller offices and home-based businesses.

In response to the increasing demand for equipment, IC manufacturers began to introduce a wide variety of integrated services digital network (ISDN) adapters, T-1 line interfaces, and highly integrated communication controllers. These devices have greatly simplified the complex task of translating the frame and packet-based LAN traffic into the formats used by wide-area networks *(see "A sampling of LAN/WAN interface components," p. 112)*.

In the remainder of this article, we'll take a quick survey of some of the more prevalent WAN technologies and the devices used to tie them to LANs.

WAN's Roots In Telco Tech

It's important to remember that most of the underlying technologies used today for making point-to-point connections across WANs trace their origins back to the telephone system. While the services offered remained pretty much the same, the Bell System continually upgraded its transport and switching systems. As early as the sixties, the telcos were using digital trunking to bundle and transport hundreds (or thousands) of digitized voice channels across their long-distance lines before being converted back to analog at their destination.

Back in those early days, a sampling rate of 4 kHz was chosen to reproduce the roughly 3.5 kHz bandwidth thta had been allocated to an analog voice channel. It was decided that eight bits of resolution was sufficient to provide analog-equivalent sound quality. The resulting full-duplex, 64-kbit/s streams are referred to as DS0's (digital signal level zero). These DS0s are the basic element that were used to build the early Dataphone Digital Data Services (DDS) which provided point-to-point digital connection and evolved into switched-56 services. ISDN, T1, and T3 connections are also composed of bundles of these DS0 channels.

Phy Layer Options

You can look at these WAN technologies from three perspectives—the physical-layer, the services run on the connections, and the devices used to connect to them. We'll start with a look at some of the most commonly used physical layers, perhaps the most relevant topic to EEs.

Although WAN backbones are built with fiber optics and microwave links, twisted-pair wiring is still usually employed to make the last-mile connection. The most basic copper-based datacom technology is the DDS. It provides users with a single channel that can be configured as either a dedicated tie line between facilities or as a switched service to other DDS subscribers. It provides an inexpensive way to bridge Ethernet, SNA, and other networks, implement frame relay service, or deliver basic videoconferencing.

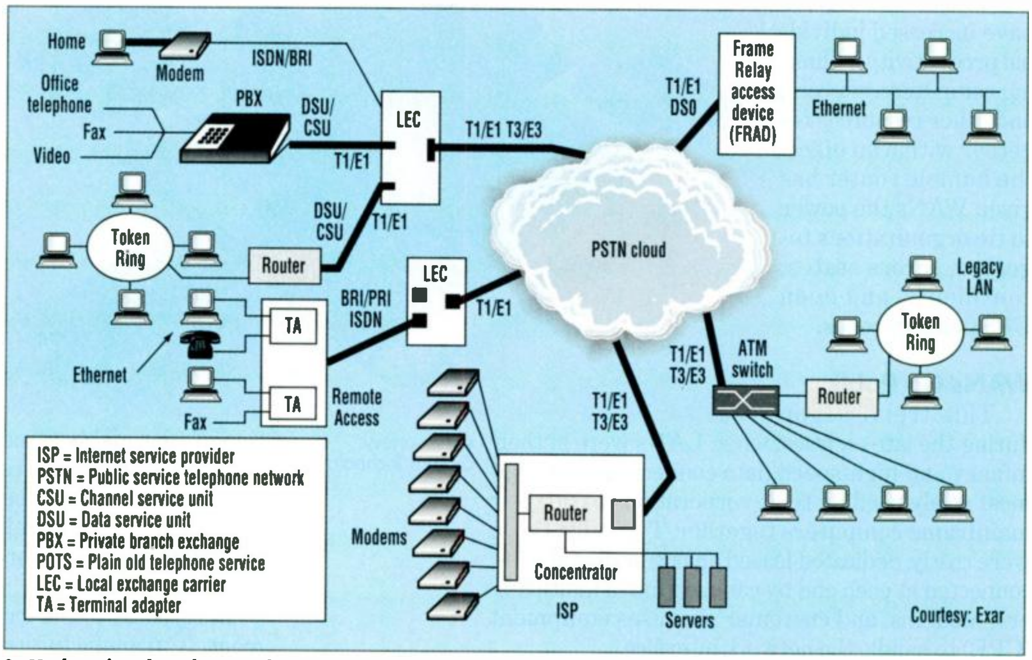
Most DDS connections only give subscribers access to 56 kbits/s of the 64 kbits/s available in its DS0 channel. This is because DDS "borrows" one bit from each 8-bit word it transmits to perform in-band signaling and control tasks. To connect to this and other digital services, we must employ a digital modem, otherwise known as a Data Service Unit (DSU). In addition to buffering and converting the data stream to a bipolar pulse format, the DSU is responsible for maintaining the stringent timing and interface requirements of the phone network.

The interface between the router, multiplexer, or other network equipment and the DSU is usually a standard full-duplex serial interface with a full compliment of handshake and control lines *(Fig. 2)*. The V.35 standard appears to be the most popular standard for DSU interfaces in North America, but there are several other commonly used ones, including V.36, RS232, RS449, X.21, and EIA-530.

The ISDN Connection

The next step up on the digital food chain is the basic rate interface, or ISDN line. In this arrangement, your friendly local carrier supplies you with a specially groomed wire pair connection. 2B1Q encoding is used to transmit a full-duplex 144 kbit/s datastream up to 18,000 feet. Time-division multiplexing (TDM) divides the flow into two 64 kbit/s DS0, or "B" channels, plus a 16 kbit/s "D" or control channel. Depending on the application, the B-channels can be independently configured for either voice or data, or even bonded to form a single 128-kbit data connection.

One of the best aspects of ISDN is that it is a mature, stable technology with clearly defined interoperability standards. While they are relatively commonplace now, there is a surprising amount of technology packed into an ISDN line interface. For example, most ISDN network terminations rely on a DSP-based adaptive filter that is used to perform the complex echo cancellation function to rid the line of near-



1. Modern distributed networks may take advantage of multiple WAN technologies to tie their far-flung nodes together. This example illustrates most of the commonly used methods of employing public networks to extend a LAN's reach.

end reflections and far-end echoes.

The recent flurry of integrated ISDN terminator and transceiver chips has made it much easier and less costly to incorporatedigital line terminations into a router or other network device *(Fig. 3)*.

While ISDN has had an underwhelming reception in the U.S. consumer market, it is enjoys much more popularity in Europe and Japan. Smaller American businesses are showing a renewed interest in ISDN as they are discover how incredibly useful a switched 64/128 kbit/s connection can

A Sampling Of LAN/WAN Interface Components

Audio Codes Ltd.

Audio Codes has recently developed the AC4804A-C, a Quad Voice-Over-Frame Relay processor. It can process four voice/fax channels simultaneously, performing any one of five global standard codec algorithms and inserts the resulting stream into a frame relay line.

3A Yoni Netenyahu St., Or-Yehuda, 60256, Israel; +972-3-533-3107; fax 972-3-533-3108; e-mail: marketing @audiocodes.com **Circle 577**

Cirrus Logic Inc.

Manufacturing ICs for both LAN and telecom applications, the company's product portfolio includes Ethernet, Fast Ethernet, T1/E1, and xDSL products, as well as high-speed multifunction modems. A recent introduction is the CL-CD4400, a four-channel communications controller with an on-chip PCI interface. Each channel can sustain transfer rates up to 8 Mbits/s, with a single channel operating up to 52 Mbits/s. Its software-driven architecture allows it to support most LAN and WAN protocols, including HDLC, Async-HDLC/PPP and programmable Sync.

3100 West Warren Ave., Fremont, CA 94538-6423; (510) 623-8300 **Circle 578**

Exar Corp.

Exar's communications products use mixed-signal technologies to produce innovative, highly integrated solutions for conventional telecom and ATM applications. Among its newest releases is the XR-T4000, a programmable universal serial interface for connecting network equipment to DSUs. It supports most global standards, including V.35, V.36, RS232, RS449, X.21, and EIA-530. Also hot from Exar's ovens is the XR-T72XX family of ATM UNI chips, designed specifically to provide a direct interface between a local ATM network and T3/E3 lines.

48720 Kato Road, Fremont, CA 94538; (510) 688-7000; fax (510) 688-7010; Internet: http://www.exar.com **Circle 579**

Galileo Technologies Inc.

Although its main focus is on low-cost, high-performance 10/100 Ethernet switching, Galileo uses its expertise in PCI bus-based systems to make inroads into the WAN access market. Its innovative GT-96010 is a coprocessor that works in conjunction with its switching components to provide a seamless path between Ethernet and ISDN/Frame Relay networks, as well as support HDSL/ADSL connections. The chip has six high-speed multi-protocol controllers, a full-duplex 10Base-T Ethernet interface, a pair of DMA controllers for each channel, and two flexible TDM channels for direct WAN interfacing.

142 Charcot Ave. San Jose, CA 95131-1101; (408) 367-1400; fax (408) 367-1401; Internet: http://www.galileot.co **Circle 580**

Level One Communications

Level One specializes in providing mixed-signal solutions for high-speed transmission and networking applications. They have been a pioneer in the development of HDSL, MDSL, and other "pair gain" transmission technologies. Their components are used in both telephone and data communications (LAN/WAN) networks. Their product line includes long- and short-haul T1/E1/J1 transceivers, switched 56/DDS transceivers and CSU/DSUs, ISDN interface circuitry, and digital subscriber loop (DSL) transceivers for HDSL and multirate DSL service.

9750 Goethe Road, Sacramento, CA 95827; (916) 855-5000; fax: (916) 854-1102; Internet: http://www.level1.com **Circle 581**

Lucent Technologies

Obviously the big kid on the block, Lucent's Microelectronics Group has been making telecom semiconductors longer than anybody. Their vast product line also includes ATM and LAN components. One of their latest developments is the Silicon Suite, an IC design process that allows customers to create their own semi-custom products at a much lower cost than previous methodologies. Designers can rough out a design using a large library of line interfaces, standard processor cores, DSPs, and other building blocks, and then fine-tune it with custom digital and mixed-signal circuits. Another interesting new product is the T7901, a single wide-area connection (SWAC) transceiver. This complete ISDN interface includes three HDLC channels, a four-wire S/T interface, and a plug-and-play function.

555 Union Blvd., Allentown, PA 18103; (610) 712-6011 **Circle 582**

Maker Communications Inc.

Maker's strength is in developing high-performance programmable communications processors, firmware, and development tools. They currently make chips and software to handle SAR, switching, and custom cell processing functions for 155 and 622 Mbit/s ATM applications. Maker's most recent development, the MXT3020, is a unique single-chip coprocessor that provides a seamless bridge between ATM and TDM circuits. It is capable of interfacing with T1, E1, and JT2 framers, as well as telephony busses such as MVIP and SCSA. Capable of terminating up to 2048 DS0's, the processor supports circuit emulation services over ATM,

(continued on page 114)

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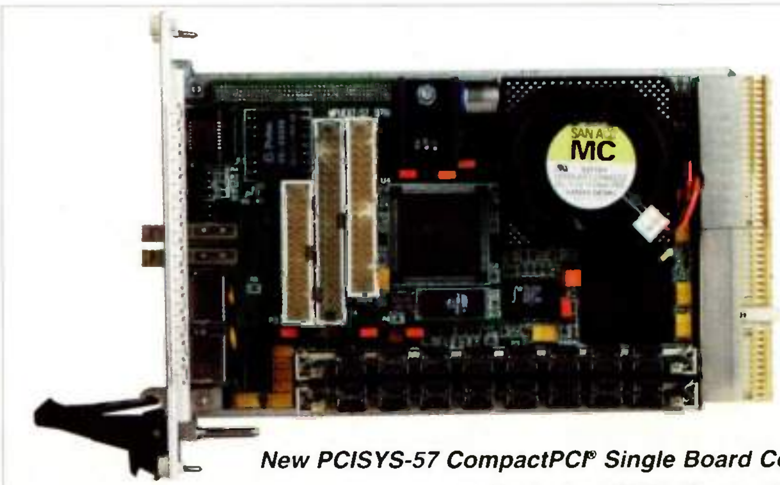

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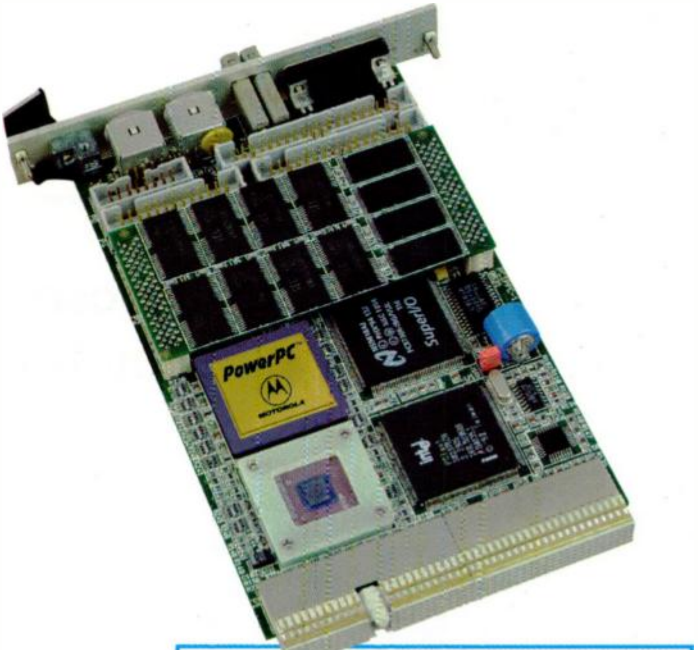


PCIPPC-1 microcomputer

PowerPC™ 603e running from 100 to 133 MHz, MPC 106 chipset, VGA, 32MB DRAM, 4 MB Flash EPROM, COM1-2, LPT1, Keyboard, PS/2 mouse

The high performance, low power consumption and small die size of Motorola's PowerPC™ 603e microprocessors make it ideally suited for a number of demanding applications found in the embedded systems market such as military equipment, avionics or aerospace applications, high speed data communication or real-time data processing.

GESPAC has introduced the first complete PowerPC™ computer compatible with the 3U CompactPCI® specification. Low power consumption, high integration, small form factor and rugged environmental specification makes this board unique in the market. Major OEM accounts have adopted our PowerPC™ board.

Avionics and aerospace equipment manufacturers are using our PCIPPC-1 because it offers a complete PowerPC™ embedded controller that measures just 100 x 160 mm using a 10 layer PCB, and Ball Grid Array (BGA) devices. Intensive tests are near completion for space qualified applications using this board.

Military embedded controllers require low power and small form factor CPUs for mobile and rugged applications. GESPAC's PowerPC™ offers excellent MTBF, shock and vibration specifications for these applications.

Telecom equipment is widely based on the CompactPCI technology. The PCIPPC-1 offers high performance, large software support and serviceability using an 8-slot passive PCI backplane implementation for advanced data communication systems.

All-in-one, Low power, Compact and Rugged forma makes GESPAC's PowerPC unique to the market

Our partnership with customers allows us to provide flexible and customized products, and to deliver a turnkey solution including complete software support.

The latest announcement by Motorola®, offering its PowerPC™ 603e microprocessors and MPC106 PCI Bridge/Memory Controller chips at extended temperatures, will allow us to address critical applications running in severe industrial environments.

Choosing the right real-time OS for your embedded PowerPC™ application

GESPAC's PowerPC™ is based on the PREP platform. This hardware reference platform allows hosting of various real-time operating systems. GESPAC currently supports VxWorks® and pSOS™ and offers a complete Board Support Package with source code and documentation.

GESPAC believes that time to market is critical for OEM products therefore, we develop partnerships with our customers offering a complete solution including hardware boards and software tools. Launching competitive embedded products to the market faster depends on the selection of appropriate software tools.

VxWorks® on GESPAC's PowerPC™

Tornado™ and VxWorks® are used as the development and execution environment for industrial, real-time applications. VxWorks® is a powerful, scalable, real-time operating system based on Tornado™, a graphically oriented cross-development environment. The user writes their program and compiles it on a UNIX or a Windows® workstation. The object code is then downloaded into the target system using a serial port or an Ethernet link.

GESPAC's Board Support Package enables developers to use VxWorks® easily with the PCIPPC-1 target board. The BSP includes PowerPC™ boot procedure, timer, serial and Ethernet drivers, FLASH EPROM and memory controllers, keyboard and PS/2 mouse support, IDE, Floppy and VGA drivers.

pSOS™ Real-Time OS

pSOSystem™ / PowerPC™ is a complete real-time operating system package supporting the ANSI and POSIX standard used in embedded military, avionics, consumer electronic, and aerospace equipment.

pSOS™ scaleable RTOS comes with a complete suite of development tools and networking services. pSOS is the industry leader with the largest installed base of applications worldwide.

GESPAC offers a complete BSP for the PowerPC™ target. It includes the source code for the boot procedure, timers, serial and Ethernet drivers, FLASH EPROM and memory controllers, keyboard and PS/2 mouse support, IDE, Floppy and VGA drivers.

New Pentium® MMX™ with Ethernet targets Embedded applications

PCISYS-57 Pentium® Single Board Computer

Pentium® MMX™, Ethernet, 82430HX chipset, 64MB DRAM, 256 kB L2 cache, USB, EIDE, Floppy, COM1-2, LPT1, Keyboard, PS/2™ mouse. 2 MB Flash EPROM

The PC is everywhere. Originally intended for office desktops, the PC architecture has attracted many embedded system designers. Due to the wide availability of low cost and high performance hardware and software tools, this standard architecture is also becoming the defacto architecture of embedded applications.

Embedded computers are a special class of computers. Reliability, ruggedness, small form factor, long term availability, quality and quick time-to-market are key issues.

GESPAC offers a new high performance, highly integrated Pentium® MMX™ and Ethernet controller computer. Additionally, the PCISYS-57 includes COM1-2, LPT1 and USB peripheral ports. This powerful implementation in a single Eurocard format makes the PCISYS-57 ideally suited for industrial automation, process control, telecom units, mass storage or medical systems.

This Single Board Computer sets new levels of performance. The 233+ MHz MMX™ technology and the "TRITON II" 430HX PCI bus interface are dramatically enhancing the capabilities of embedded systems. The powerful Pentium 64-bit engine with 256 Kb of Level2 cache, makes Windows NT™ or any large scale application soar. Low power dissipation is achieved by reducing the CPU clock frequency while still achieving a bandwidth of 100 MB/s on the backplane.

Embedded controllers are more connected. They must provide or retrieve data from remote equipment. The on-board 10 Mbits/s Ethernet controller provides distributed processing capability. For example, the operating system and the application can be downloaded from the network for diskless configuration.

This board is more rugged than any other PC/AT form factor. On-board Flash EPROM with a capacity of 2 MB is available for embedding in solid-state memory DOS™ or real-time operating systems such as VxWorks® and pSOS™.

The PCISYS-57 offers a flexible solution. It can be stripped down to a blind node configuration, removing EIDE, Floppy and LPT1 interface on the low profile mezzanine. The Ethernet controller can also be removed, turning this board to the most compact Pentium® MMX™ implementation.

Low power consumption is achieved by under-clocking the CPU and fine tuning the Plug & Play BIOS. The board can be powered up through the CompactPCI® backplane or using the on-board power supply connector available for stand alone configuration.

- ***Higher performance***
- ***Greater Connectivity***
- ***Ruggedized***

This board is fully compatible with standard PC/AT operating systems such as DOS™ or Windows NT™, or any real-time kernel.

Embedding Windows NT™

Windows NT™ is a robust, mature, widely accepted and supported operating system in the desktop industry. It offers an advanced graphical user interface and large networking capabilities including TCP/IP and remote access. Unlimited choices of third party development tools and ready to use device drivers shrink the development time of the most complex applications.

Embedded applications need more than that! Windows NT™ is a multi-tasking operating system, but it is not a deterministic real-time kernel. Furthermore, a ROMable feature and small footprint are necessary for diskless configurations.

A partner with VenturCom®, GESPAC offers an easy to use development tool for integrating, configuring, and building dedicated Windows NT™ target systems. This package consists of a suite of driver and component support such as Null-Display and Null-Input, FLASH Boot Support, and various configuration tools for shrinking standard Windows NT™ down to 8 MB of RAM and 10 MB of disk space.

Real-time extensions including high speed clocks and timers, memory allocation control, I/O and interrupt direct access turn Windows NT™ into a true, hard real-time operating system.

GESPAC's fault tolerant system aims at mission critical applications

Fault tolerant and redundant systems are widely used for critical applications in military, telecom, or avionics embedded controllers. These systems must remain fully operational under any circumstances. No downtime is required for an airplane anti-collision system or for large-scale call centers and Telecom central offices.

Dual client CompactPCI® System

2 units with Pentium and Ethernet, redundant power supplies, 2 GB HDD, RAID support, EMC compatible

The passive backplane approach of CompactPCI® allows a board swap or the expansion of the system configuration in a few minutes, but the system must be turned off. Replacement of a failed or suspect adapter while the system continues to run, providing uninterrupted service, is achieved using a full redundant architecture based on a client / server model.

GESPAC has implemented a fault tolerant system using a client / server architecture. Two fully redundant units are installed in a CompactPCI® chassis and are interconnected using an Ethernet link. While one unit is processing all the critical data, the other unit monitors the functioning of the complete system.

If an incorrect mode is detected on the main processing unit, the second CompactPCI® unit takes over the control for critical data processing. The failed unit can be powered down and replaced while the system continues to process all the critical data. After this maintenance procedure, the system resumes the client / server operation.

GESPAC introduces this dual client CompactPCI® system based on two fully redundant Pentium® boards. The two CPUs are plugged into two separate CompactPCI backplanes and are processing the mission critical data using the client / server operation mode. This true redundant 3U system provides uninterrupted service. It also features dual redundant hot-swap load sharing power supplies, RAID support, and two 2GB EIDE hard disks. This system is fully compatible with EMC legislation. Optionally, this system can be expanded to a 6U enclosure with a large number of slots available for user I/O functions and a choice of front panel or rear I/O panel access.

Mission critical systems requires no downtime

Please contact GESPAC for more information on fault tolerant system solutions.

Hot-Swapping available with CompactPCI

The CompactPCI® connector accommodates the mechanical prerequisites for "Hot-Swapping" by staging the pin sequence within the backplane male connector.

A fully capable hot-swap system must include the hardware platform but also the software services and device drivers. Currently, the PCI Hot Plug Workgroup has approved a draft for the Hot Plug 1.0 specification following the major contribution of Compaq®.

Hot-swapping is likely to be adopted by the CompactPCI® technical committee in the near future because it has major advantages. Not only is it supported by major hardware and software manufacturers, but it also provides an easy migration path allowing one to use existing PCI adapters and to turn them into hot plug devices using hot plug drivers.

The hardware platform is based on a slot-specific power control allowing a single slot to be powered down without stopping the entire system operations.

The software implementation is OS specific but it should include the device driver of the adapter and hot plug services and primitives. Hot plug operations are controlled through a user interface where requests are issued to quiet an adapter, and to turn slots on and off.

A typical hot swap operation includes the following operation: notification of the intention to remove an adapter. All activities are stopped on the adapter and the specific slot is powered down. The user can safely remove the standard PCI adapter and replace it. The new board can then be powered up again and the software resumes activities.

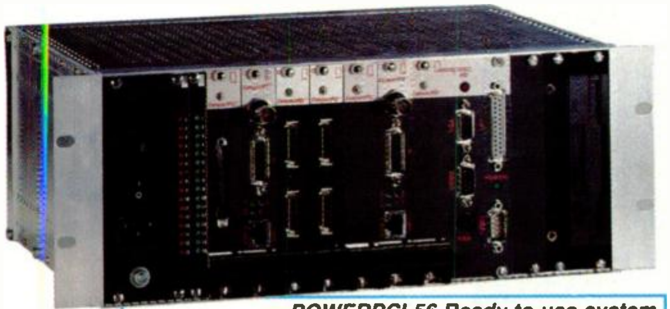
The "Hot-Swap" PICMG technical committee must still define the actual implementation of the hardware platform on the CompactPCI backplane.

GESPAC shrinks design time offering customized and ready to use industrial systems

In recent months, there has been a great deal of talks about PLCs having had their days. The PLC is not dead, but its architecture is tied too closely to a unique vendor-controlled technology. Proprietary architecture means that the end-user cannot benefit from the full support for alternative vendors and I/O interfaces.

Open control architecture using the PC technology provides greater flexibility with a large choice of I/Os, high performance CPUs, and a large support of IEC-1131 or SCADA software packages.

GESPAC offers a complete CompactPCI® ruggedized system for this new generation of industrial computers allowing higher performance and greater flexibility to the system engineer. For example, the ready to use POWERPCI-56 system includes a Pentium® CPU and VGA, COM1-2, LPT1, IDE and Floppy using only one slot. This 60 TE chassis comes equipped with an 8-slot backplane and a 150 Watt power supply. A 4-slot backplane and plug-in power supply are also available.



POWERPCI-56 Ready to use system

Pentium® CPU, 64 MB of DRAM, VGA,COM1-2, LPT1, Kbd
7-slots available for plug-in Industrial I/O CompactPCI® board
PC/104 interface for distributed I/Os

Additional functions such as Ethernet, high speed VGA, and a PCMCIA controller can also be installed in the chassis to extend the MMI and networking capabilities of the system. Any type of CompactPCI® adapter can be mounted to complete the features of this industrial controller.

In the same chassis, GESPAC offers a large choice of industrial plug-in I/O boards (digital, analog, and thermocouple) and an Industry Pack™ carrier for hundreds of different mezzanines including RS-232 / RS-485 serial lines and signal conditioners.

Various fieldbus controllers (FIP, CAN, or any PC-104 board) can also be mounted in the system for low cost distributed I/O solutions. This architecture is widely used in PLC open controllers.

GESPAC provides ready to use and pre-configured systems according to customer requirements: size of the enclosure (60 or 84 TE, 3U or 6U), with fan tray, etc. Various power supply units ranging from 28 VDC to 110 / 220 VAC are also available on request. The customer may order the system with a standard operating system pre-installed such as Windows NT™ or VxWorks®. This system is fully compatible with EMC legislation and other industrial certifications can be completed on specific requests.

GESPAC offers Ready to use and Pre-configured CompactPCI® industrial computers

Please contact GESPAC for a complete list of industrial I/Os and system devices available on CompactPCI® or pre-configured and ready to use complete systems.

Combining 3U and 6U CompactPCI maximizes performance and flexibility

High performance and flexibility using an open architecture are the most often requested capabilities of 6U systems. GESPAC offers a 6U CompactPCI® enclosure where a standard 3U CPU can be mounted.

3U CompactPCI® CPU boards deliver more bandwidth on the backplane because they provide a direct PCI interface to the backplane (100 MB/s transfer are typically achieved with the 82430HX chipset).

Typically, 6U CPU boards use the level 1 PCI bus for local functions such as on board VGA, SCSI, and Ethernet. Thus, a PCI to PCI bridge is required to access the backplane. In this case, only 70 MB/s of bandwidth is available

100 MB/s bandwidth available
Specific bus installation

for additional high speed communication functions.

Telecom and industrial systems are using a high speed PCI backplane for system functions and also a dedicated bus interface for specific data processing such as voice packets. This additional backplane sits on top of the enclosure. GESPAC's system offers the possibility to plug any type of 6U peripheral board with the CompactPCI interface at the bottom of the PCB and the dedicated bus interface on top.

Compared to the traditional 6U CPU model with a fixed, defined bus interface, this solution offers more flexibility.

This complete enclosure comes with an 8-slot backplane, a 250 Watt power supply, 1.2 GB EIDE hard disk and a 3.5" Floppy. A fan tray can be mounted at the bottom of the chassis for severe environments.

For more information on the different CompactPCI® ready-to-use 6U systems, please contact GESPAC.

GESPAC's Panel PC withstands the most severe environment extended temperature, shock and vibration

Unique Panel PC
Extended temperature from -25 to 70° Celsius 486 DX4, 16 MB of DRAM & Flash EPROM 10.4" TFT display, COM1-2, EN 50155 Railway specifications

Some industrial applications are really severe. Embedded controllers get bumped and dropped. They have to work when temperatures are really high or really low. They are exposed to humidity, salt air or dust storms. Train equipment, military systems and outdoor controllers are typical applications where system designers should seriously consider true extended temperature products.

GESPAC introduces a unique, ready-to-use Panel PC for the most severe industrial environment and fully operational from -25° to +70° Celsius. Furthermore, this system has also been fully certified according to the EN 50155 railways specification including shock and vibration, and EMC compatibility.

Based on our new 486DX4 extended temperature CPU, this system offers a high performance core CPU with 16 MB of Flash EPROM Solid State Disk, COM1-2, and a PC/104 port for an additional plug-in mezzanine. The user interface is based on a 10.4-inch TFT display with 200 cd/m2 luminance, display resolution of 640x480 and automatic day/night switch. An optional touchscreen and a fully sealed keyboard can be mounted in the enclosure. This system uses a compact and rugged enclosure (300x280mm and 70mm of width). Various power supply units can be installed (DC/DC or AC/DC ranging from 24 VDC to 220 VAC).

This system can be adapted to customer specific requirements. Private label, user defined enclosures, and specific front panel layout can be completed by the GESPAC engineering team. Additional plug-in functions such as fieldbus network and digital or analog I/Os can also be mounted in the system using the PC/104 extension port.

Unique Panel PC Fully certified for -25° to +70° C. operations EN-50155 railway specification

GESPAC offers a very flexible system for extended temperature applications. Please contact GESPAC for more information on this unique product or for specific requirements.

All you need is a 486 DX4 board operating from -25° to + 70° Celsius

For years, the lack of extended temperature components on the PC/AT platform was a serious limitation for the use of x86 embedded controllers. System designers had to sample boards and components from production batches designed for commercial use (0 to +50 degree Celsius). This process compromises MTBF, reliability and quality issues.

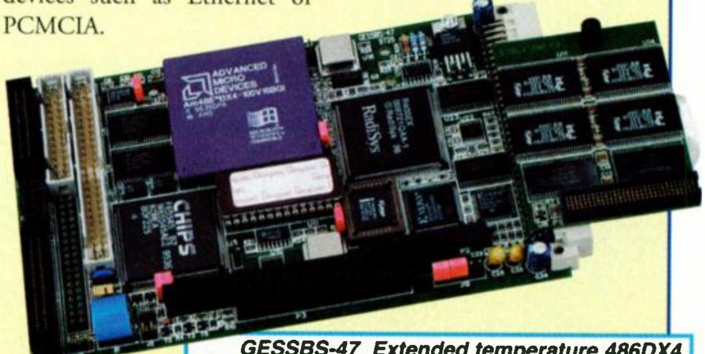
The time has come for a new generation of fully qualified industrial PC/AT components. 486 CPUs and Chipset controllers are now available for extended temperature operations (-25 to +70 degree Celsius) with a long term availability guarantee. Fully certified high performance PC/AT embedded controllers can be designed using this new generation of components.

The new 486 DX4 compact and rugged CPU allows system designers to develop a wide variety of OEM equipment fully certified for extreme operating temperatures. The ready to use GESSBS-47 board is a complete PC using only 160x100mm of PCB and it can be used in a stand alone configuration for embedded controllers.

This board features 16 MB of DRAM and 16 MB of Flash EPROM for embedding PC/AT compatible operating systems and applications. Additionally, it comes with a 65545 VGA controller from Chips & Technology® and all the PC/AT peripheral ports including COM1/2, LPT1, Floppy and IDE hard disk interface. A PC/104 port is used to stack inexpensive devices such as Ethernet or PCMCIA.

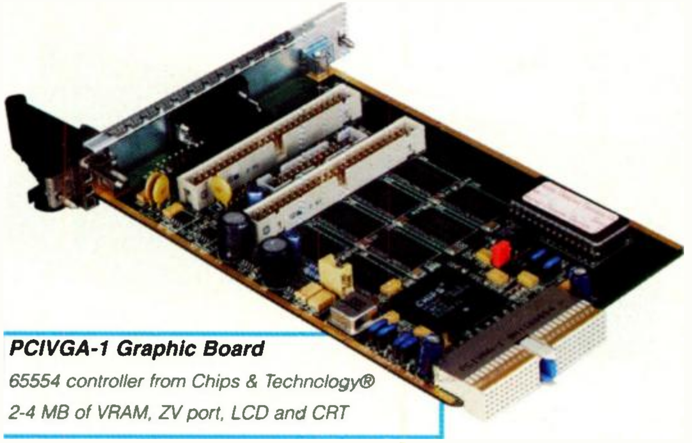
The GESSBS-47 is fully compatible with the G-96 bus specification and it can be expanded using a large range of industrial I/O boards such as digital and analog functions available from the GESPAC catalog.

Additionally, this board can be customized according to customer requirements.



GESSBS-47 Extended temperature 486DX4
Single Board Computer, VGA, COM1-2, LPT1 16 MB of DRAM & Flash EPROM, PC/104, Floppy & IDE

Graphic & live video boards gunning for compact and rugged mobile multimedia equipment



PCIVGA-1 Graphic Board

65554 controller from Chips & Technology®

2-4 MB of VRAM, ZV port, LCD and CRT

Today, embedded controllers must deliver graphic information; 3-D GUI, frame grabber and multimedia functions are now widely used in OEM equipment. Man-machine interface in the production line, remote display for unmanned vehicles, rugged professional cameras, mobile live video systems, and video conferencing are typical applications for low power and high performance graphic and frame grabber adapters.

The CompactPCI® bus provides high performance and full electrical compatibility with the standard PCI desktop components, along with a very large software support for advanced graphical user interface. In addition, CompactPCI® offers a more rugged and compact form factor ideal for harsh environments and ease of maintenance using a passive backplane, and 8 slots without a PCI to PCI bridge for large topology.

The PCIVGA-1 is a high performance VGA controller offering a 64-bit accelerated engine for both CRT and LCD displays. This board is based on the 65554 controller from Chips & Technology and it supports 2 to 4 MB of VRAM for large display resolutions. A Zoom Video port for multimedia capture is also implemented. The Panel link interface allows interface to a remote LCD display. To summarize, the PCIVGA-1 is an industry leader for graphic solutions. It offers exceptional performance and superb video quality allowing flexible implementation in a large variety of industrial applications such as avionics, military and multimedia systems.

GESPAC offers Low-Power, High-Performance, 64-Bit Video Accelerated LCD/CRT CompactPCI® boards

MotionVideo™, using our new PCIMVA-1 adapter allows playback of live video images for guidance systems and rugged multimedia equipment. Full motion images are captured, using a NTSC / PAL decoder, then transferred to the CL-GD7556 graphic controller for interactive visual computing. This board drives CRT and LCD displays and also supports the ZV-Port for MPEG video playback and teleconferencing. The PCIMVA-1 comes equipped with 2 or 4 MB of VRAM, allowing large display resolutions. Low power management is achieved using the VESA® Display Power Management Signaling technology. This board is an extremely flexible and cost-effective multimedia solution for a large range of applications.

For more information on these graphic functions, please contact GESPAC.

FireWire™ unleashes the power of industrial digital video

IEEE-1394, commonly named FireWire™, is a high speed serial bus. It provides new ways to capture and to transmit color images using distributed and Hot-Plug device functions connected though an inexpensive twisted pair serial bus.

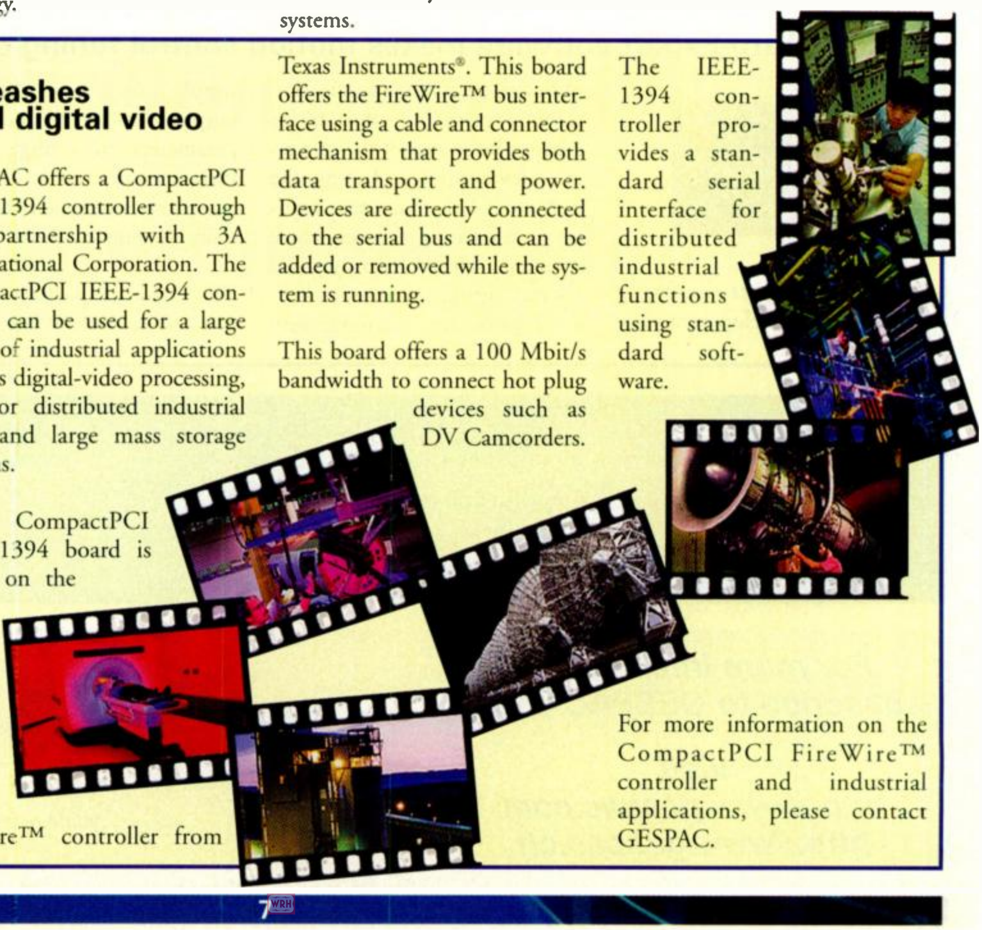
Supported by industry leaders such as Apple, Sony, Texas Instruments and Microsoft, the IEEE-1394 serial bus is the cornerstone of future PCs systems acting as a high speed multimedia expansion bus. The IEEE-1394 offers complete software support including device drivers for the major operating systems. The IEEE-1394 offers unique opportunities for digital image processing, factory automation, telephony applications and data storage applications.

GESPAC offers a CompactPCI IEEE-1394 controller through its partnership with 3A International Corporation. The CompactPCI IEEE-1394 controller can be used for a large range of industrial applications such as digital-video processing, local or distributed industrial I/Os and large mass storage systems.

The CompactPCI IEEE-1394 board is based on the Firewire™ controller from Texas Instruments®. This board offers the FireWire™ bus interface using a cable and connector mechanism that provides both data transport and power. Devices are directly connected to the serial bus and can be added or removed while the system is running.

This board offers a 100 Mbit/s bandwidth to connect hot plug devices such as DV Camcorders.

The IEEE-1394 controller provides a standard serial interface for distributed industrial functions using standard software.



For more information on the CompactPCI FireWire™ controller and industrial applications, please contact GESPAC.

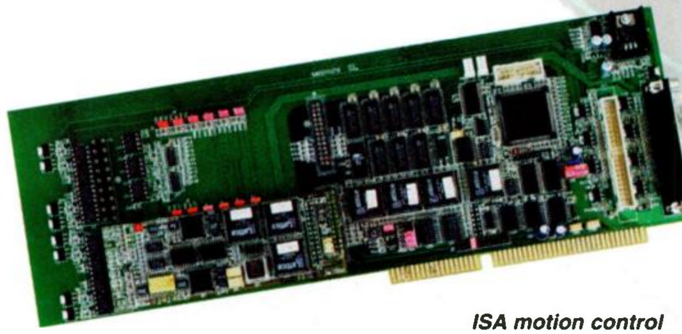
GESPAC's leading motion control board now available on ISA bus

GESPAC offers a new ISA motion control board for high performance machine tool, multi-axis robotics and tracking systems. GESPAC provides a complete solution based on a dedicated DSP processor and a complete software environment to shorter the development time of the most complex applications.

When timing is everything, GESPAC's motion control is the best solution

GESPAC's motion control hardware drives four DC or brushless axes or more using additional plug-in boards. The motion control package includes high performance hardware and the Auto-Expert software for easy axis tuning. This solution is ideally suited for motion control applications where time to market is critical.

The ISADMC-4P board is based on the powerful DSP56002 @ 40MHz and includes four 16-bit DAC outputs, four incremental encoder inputs and sixteen 12-48VDC opto-isolated digital I/O ports. The ±10V analog output drives any servo-amplifier in torque mode or in current mode.



ISA motion control

4 DC or brushless axes, Auto-Expert software

The regulation firmware is embedded inside the Flash EPROM on the board and performs the regulation loop for each axis. It also includes the trajectory generator that will calculate axis acceleration and deceleration. Safety features to prevent damage in case of malfunction or even user programming are also in the firmware. Commands sent by the host CPU are processed by this low level software. Additionally, this firmware implements a data recorder function for debugging purposes.

This complete hardware solution is also available on different industrial form factors: VME bus for high-speed CNC systems and G-96 industrial bus for compact and rugged applications.

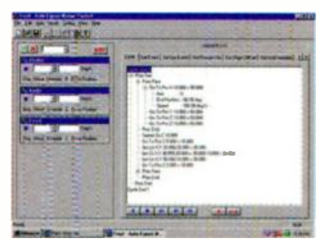
Our motion control package will soon be available on the CompactPCI® architecture and it will be released with a new Windows NT™ version of the Auto-expert software.

Please contact the GESPAC sales force to receive our complete motion control brochure and a working demonstration of the Auto-Expert software.

The Auto-Expert software makes motion control tuning easy

The Auto-Expert software decreases the development time of the most complex application using a powerful solution for tuning all the axes of the process in a few minutes. Tuning the 2nd order Pole Placement regulator, calculating the resonance frequency, closed loop dynamic control, introduction of feedforward loops are becoming very simple tasks. A digital scope output displays all the tuning parameters on a single screen. Programming of a single or multi-axis sequence is based on a simple motion editor.

This software package is fully compatible with Windows® 95 and Windows NT™ operating systems.



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STRATEGIC PARTNERS WORKING TOGETHER

Information has always been a part of the developmental strategy needed for success in the OEM market. In today's fast-paced, competitive global market environment, technology information has become a priority. Systems designers not only want to know what their strategic supply partners are doing today, but where they're going. Designers and suppliers must now work in tandem to align enabling technology with the customer's system requirements. These strategies demand strong partnerships in the development of competitive products.

A third strategic partner completes this alliance. This partner's mission is to observe and report today's product availability by its editorial staff of respected experts, while constantly probing for the next generation of enabling technology. The constant flow of exclusive and vital information helps to bring systems designers and suppliers together as strategic partners. It also provides engineers and engineering managers with an enhanced ability to bring more competitive products to market, faster.

Electronic Design is that strategic information partner — a partner who provides the information that helps the systems designer make those critical decisions that stay the course of the technology road map.

Your Strategic Information Partner.

ELECTRONIC DESIGN

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be for everything from videoconferencing to Internet access.

Thanks to the declining cost of both interface hardware and the services themselves, the majority of smaller routers for small-office/home office (SOHO) applications are built around ISDN connections. Also, many ISDN lines are finding a home emulating DDS connections that were originally used in most older systems.

T1 And Beyond

Moving past ISDN, we now enter the realm of trunk lines. These larger

(continued from page 112)
such as PBX trunking, computer telephony, and performs frame relay and inverse multiplexing functions.

73 Mount Wayte Avenue., Framingham, MA, 01702; (508) 628-0622; fax (508) 628-0256;e-mail: info@maker.com.
Circle 583

Mitel Semiconductor

Mitel's strengths include many years of experience in nearly every aspect of telephony and data communications imaginable, plus, video, and optoelectronics. Specialties include all levels of ISDN, T1/E1, and T3/E3 components, and switching elements, and interfaces for high and low-speed lines. They also have a full line of TDM bus-based computer telephony ICs and software. Information-hungry designers should be aware that Mitel's data book and application notes make excellent reference materials concerning the vagaries of nearly any aspect of TDM networks.

350 Legget Drive, Kanata, Ontario, Canada K2K 1X3; (613) 592-2122; fax (613) 592-6909; Internet: http://ww.semicon.mitel.com **Circle 584**

MMC Networks

Much like Galileo, MMC has concentrated on providing low-cost, high-performance 10/100 Ethernet and ATM switch components. Its proprietary shared-memory VIX architecture enables it to perform per-flow queuing for both packet and cell-based traffic. The addition of their Anyflow 5500 network processing engine can be added to their switch to provide layer-3 routing and protocol translation between virtually any LAN or WAN connection. With a bandwidth of up to 40 Gbits/s, its flexible I/O structure can interface to multiple Ethernet, ATM, and T1/E1 or T3/E3 transceivers. The chip set's software-driven network processor can be programmed to handle advanced functions such as IP multicast, virtual SAR, layer-3 address translation, and per-flow QoS control.

1143 Arques Ave., Sunnyvale, CA 94086-4602; (408) 731-1600; fax (408) 731-1660; Internet: http://www.mmcnet.co
Circle 585

Motorola

Motorola's Networking And Computing Systems Group has leveraged its microprocessor technologies and high-density processes to create a vast family of communication controllers. At the low end, its SC series integrates 68000 processor cores and specialized firmware with serial and parallel interfaces for items such as ISDN adapters. At the high end of its product line, the 860T Power QUICC controllers incorporate Power PC cores, 32-bit RISC controllers, multiple parallel and serial HDLC channels, plus specialized I/O and memory cores. Variants of the Power QUICC family can be used to interface 10 and 100 Mbit Ethernet networks to WAN services, including multiple T1/E1 lines and TDM busses used for computer telephony.

6501 William Cannon Dr. West, Austin, TX 78735-8598; attn: Fenerec Koplyay (512) 891-7228; e-mail: fenerec_koplayay@risc.sps.mot.com; Internet: http://ww.mot.com
Circle 586

PMC-Sierra, Inc.

PMC has been making high-performance networking components, with a focus on ATM, SONET/SDH, and T1/E1, for a long time. In addition to manufacturing the usual framers and multiplexers, the wizards in Burnaby have distinguished themselves by providing some of the first fully functional 622-Mbit/s ATM physical layer devices. Another recent breakthrough is their PM736x FREEDM series of HDLC controllers. Using a PCI Bus as a backplane, these 100+ Mbit/s packet processors can terminate up to 32 T1/E1, SDL, or DS3 lines and support up to 128 simultaneous HDLC channels.

105-8555 Baxter Place, Burnaby, BC, Canada V5A4V7; (604) 415-6000; fax (604) 415-6200 **Circle 587**

Pulse Components Division

Pulse makes a variety of magnetics and other line interface components for high-speed telephony and LAN applications. The newest addition to its product line is the TM311 family of coded mark inversion (CMI) line transceivers. Intended for SONET/SDH telecom applications, the transceivers are available in E4/STM-1 (278.528 Mbit/s) and STM-1 (311.04 Mbit/s) speeds.

Two Pearl Buck Court, Bristol, PA 19007-6812; (215) 781-6400; fax (215) 781-6403 **Circle 588**

Telogy Networks

Noted for its software-centric communications products and systems, Telogy concentrates on LAN/WAN bridging technologies. These include a complete microprocessor/DSP software solution for transmission of voice, fax, and data over packet-based networks. One of its latest products is its FPGA-based Golden Gateway ATM inverse multiplexer chip set, which allows designers to easily add this capability to existing equipment.

20250 Century Blvd., Germantown, MD 20874; (301) 948-5204; fax (301) 417-0324; e-mail: TN@telogy.com; Internet: http://www.telogy.com **Circle 589**

TranSwitch Corp.

Pioneers in ATM LSI chips, TranSwitch also offers a full line of T1/E1, T3/E3, line interfaces and other components for inverse multiplexing, framing, and switching. One of its latest releases is the E123 MUX, a single-chip device that multiplexes 16 E1 (2.048 Mbit/s) signals onto a single E3 (34.368 Mbit/s) line.

8 Progress Drive., Shelton, CT, 06484; (203) 929-8810; fax (203) 929-9453; Internet: http://www.transwitch.com **Circle 590**

bundles of TDM-aggregated DS0 channels were originally used to transport traffic between central offices, but are now commonly found serving as fat pipelines in larger offices, computer centers, and Internet service providers.

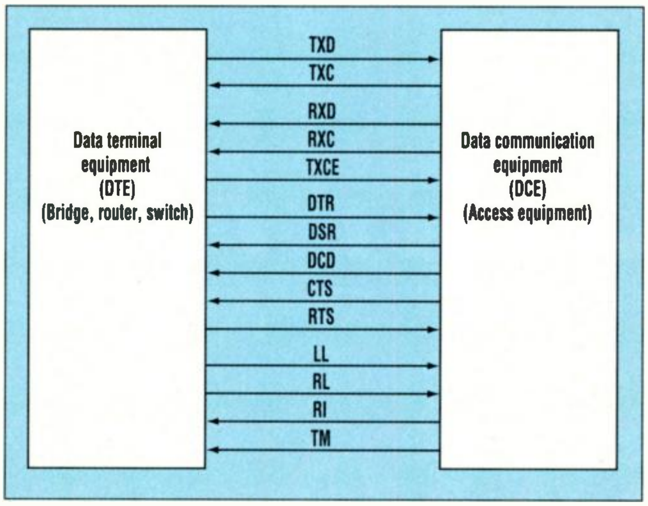
Within the telecomunications industry, there is a standard multiplexing hierarchy that bundles groups of DS0 channels into larger groups. The fundamental unit is the T1 line, which carries 24 64 kbit/s DS0 channels for a total of 1.536 Mbits/s capacity. Overhead framing bits add another 8 kbits/s to the channel, bringing it up to 1.544 Mbits/s. Its European counterpart, the E1 line, carries 30 DS0 channels.

At the physical layer, a T-1 line still uses a four-wire connection. The original dc-balanced modulation scheme employs bipolar alternate mark inversion (AMI). A binary eight/zero suppression (B8ZS) code substitution scheme is used to help the line's repeaters maintain synchronization by substituting a special code any time it senses a block of eight consecutive zeroes in the data stream. This was developed nearly 30 years ago to provide the T-1 line repeaters' primitive clock recovery circuits with a steady source of signal transitions. In those early days of T-1, these repeaters had to be placed every few thousand feet or so in order to regenerate the signal. Typical distances between repeaters today have increased to about a mile.

T-1 comes in a wide variety of flavors, depending on the application you have in mind. The original "straight" T-1 is used primarily for point-to-point transport of all 24 channels and can be used for fixed applications such as Internet traffic concentration.

In some cases, a straight T1 line can terminate at a telco's central office, and obtains switching for its channels using robbed-bit signaling or dual tone multi-frequency (or DTMF, better known as touch tone) dialing. Signaling also can be used to bond two or more DS0s together into a larger data channel for applications with greater speed requirements. Most carriers also will provide "fractional T-1" service, where the same four-wire interface delivers smaller numbers of DS0 channels for a reduced price.

In addition, switched T-1 services can be provided using something called a primary-rate interface (PRI). In this arrangement, 23 of the line's TDM channels are allocated to voice or data traffic. One DS0 time slice is reserved for use as a single 64 kbit/s control channel which handles call requests and maintenance functions for the other channels. PRIs can interface directly to ISDN networks as well as individual ISDN lines.



2. The DSU provides a standardized electrical interface between WAN access equipment and LAN elements. The high-speed full-duplex serial interface allows routers, bridges, and switches to communicate easily with whatever line interface they happen to be using. The DSU's universal pinout can support several international electrical interfaces, such as RS-232, V.35, V.36, and X.21.

Groups of T-1 lines can be multiplexed together onto higher capacity lines. The T-3 line is a veritable monster, bundling 28 T-1 lines for a total of 672-DS0s, or 44.736 Mbits/s worth of capacity. At T-3 speeds, the traditional four-wire interface can no longer cut the mustard, and either coaxial or fiber-optic cable must be used to run out to the customer's site.

Beyond traditional TDM services, the most promising technology appears to be the digital subscriber loop (DSL). This relative newcomer to the telephony scene comes in several different flavors, including the high-rate subscriber loop (HDSL), rate-adaptive DSL (RADSL), and asymmetric DSL (ADSL).

ADSL has attracted a lot of attention over the past couple of years because it promises to deliver T1+ speeds (up to 8 Mbits/s in the downstream direction) over a conventional copper pair without special line conditioning. As the name implies, ADSL does not have equal bandwidth in both directions, but even its lowest upstream rate of 384 kbits/s should be more than adequate for many applications.

Since ADSL is only a last-mile (actually 12,000+ feet) technology, its data streams must be collected and funneled onto a PSTN trunk line, or routed into the Internet. This ability to bypass the public switched telephone network's (PSTN's) switching infrastructure may be one of ADSL's greatest advantages, since the carriers are already complaining that their switches are reaching saturation in areas with high Internet subscribership.

The ADSL Forum, an industry consortium, and working committees within T1/E1 and ETSI are working to produce working standards that will get interoperable equipment onto the street as quickly as possible. *(For further details on ADSL, see "Broadband Communications To The Home: Challenges On The Last Mile,"* ELECTRONIC DESIGN, *Oct. 2, 1995, P. 67, and watch for an in-depth update on broadband tech in the upcoming Dec. 1, 1997 issue.)*

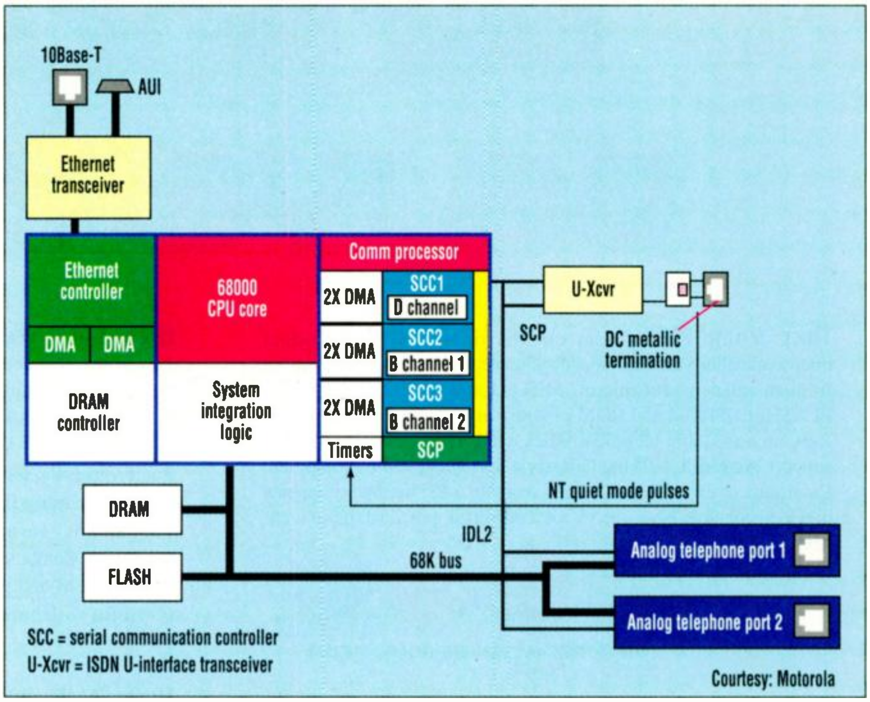
WAN Protocols And Services

Once we have a raw digital connection, it must somehow be structured so that the networks on either side can talk to each other in their native language. The problem is that LANs are either packet- or cell-based, with framing and control protocols that are completely different from those used for WAN transport. In most applications, high level data link control (HDLC) or some other variant of the X.25 protocol is used to harmonize the two networks. Its job is to insert flags that identify the beginning and end of a data packet and send messages that perform flow control at the LAN interfaces.

While HDLC is good for point-to-point connections, frame relay is a popular extension of HDLC which encapsulates packets for transport within a

switched WAN environment. Because frame relay enables "dial-up" LAN-LAN connections and is nearly transparent to most LAN protocols, it has found wide acceptance within the datacom community.

People are playing other interesting tricks with WANs these days, including shipping ATM cells over it. Known as cell relay, T-1 has been used to extend high-speed ATM networks to areas where deploying a dedicated network wouldn't be practical. Because a T-1 line is much slower than a standard OC-3 (155 Mbit/s) ATM connection, a technique known as inverse multiplexing is often used to split a data stream and carry it across multiple T-1 channels. At the other end, the streams are multiplexed back together into a single flow.



3. ISDN routers have become inexpensive and simple to implement, thanks to large-scale integration. Consisting of four or five ICs (including memory and Ethernet interface), this "personal router" employs a single-chip communications controller to handle both the ISDN protocol conversion and act as an Ethernet media access controller.

The WAN Access Market

The increasing use of remote access and distributed workplaces has created an enormous market for an expanding array of LAN/WAN interface equipment. Following are some of the types of products you can expect to be designing or using in the near future:

• *SOHO routers* are intended for offices with two to six computers, and usually have an ISDN or low-rate frame relay connection to the WAN for remote access to corporate LANs or the Internet. A single 10Base-T Ethernet interface allows it to sit on the local network and serve all the platforms connected to it.

• *Frame relay access devices (FRADs)* encapsulate LAN traffic inside a frame structure for transport across a switched packet service network. They can be either standalone boxes like ISDN adapters, or they can be embedded as line cards within a larger router.

• *Branch offices* which need constant contact with a central facility will probably require a larger router connected to a FRAD or fractional T-1 line. Besides remote access, tasks for this equipment might include a direct tie line to a corporate mainframe or server. LAN interfaces can include 10/100Base Ethernet or token-ring.

• *Regional offices* that serve multiple remote sites could require a serious router, possibly with multiple protocol capabilities. One could expect to terminate multiple T-1 lines and act as a gateway for traffic to central computing facilities over T-3 lines.

• *Enterprise routers* are the flagships of the line, intended to handle traffic from central headquarters and large data processing facilities. In these applications, multiple protocols are the order of the day as they handle Ethernet, token-ring, and local ATM traffic from multiple servers, backbones, and modem banks. Moving data between T-1/3 lines, high-rate frame relay services, and even traffic from metropolitan SONET rings may all be in a day's work for these behemoths. Think gigabits.

• *Internet Service Provider (ISP) Servers* are a relatively new application for routers that is rapidly becoming a significant part of the market. These boxes are used to concentrate traffic from dozens or even hundreds of modems onto high-speed T-class lines for transport into the Internet.

• *Set-top boxes* might strike you as an unlikely place to stick a router, but in fact they will probably serve as a WAN interface for many homes using cable modems or ADSL to receive entertainment and information. Equipped with a video output and a 10Base-T Ethernet connection, these units will probably employ a single-chip communication processor to sort out the traffic between the box's MPEG decoder and its home-area network interface.

References

A T-1/E-1 Primer and *The Digital Networking Handbook* are available from Racal Datacom, 1601 N. Harrison Parkway, P.O. Box 40744, Fort Lauderdale, FL 33340-7044; (800) RACAL-55; fax (305) 846-4942.

The Mitel Telecommunications Circuit Data Book is available from Mitel Semiconductor, 350 Legget Drive, Kanata, Ontario, Canada K2K 1X3; (613) 592-2122; fax (613) 592-6909; Internet: http://www.semicon.mitel.com.

Special thanks to Dave Chase and Al Miller at Level One Communications, Daljeet Mundae at Mitel Semiconductor, and Al Ghasakanuan at Exar for their time, patience, and invaluable assistance in the preparation of this article.

HOW VALUABLE	CIRCLE
HIGHLY	574
MODERATELY	575
SLIGHTLY	576

UPDATE ON CELLULAR COMMUNICATIONS

European Mobile Multimedia Wagons Start to Roll

The European Telecommunications Standards Institute (ETSI) will choose its radio-access technology for third-generation digital cellular mobile-communications systems December 19. ETSI has assigned five concept groups to evaluate 13 candidate air interface technologies volunteered by 10 international consortia *(Table 1)*. At the same time, at least two proposals are on the table for a fixed network architecture for what ETSI refers to as its Universal Mobile Telecommunications System (UMTS).

The idea behind UMTS is that it will provide broadband access at rates up to at least 2 Mbits/s for mobile multimedia terminals. ETSI set a tight schedule for the new services such a system will provide. The current plan is for the first UMTS network to start commercial operation on a limited basis on January 1, 2002. This trial service will begin service with a limited amount of RF spectrum in the range set aside for UMTS (between 1900 and 2170 MHz). During the following three years more spectrum will be made available to give a grand total of 215 MHz—155 MHz for terrestrial use and 60 MHz for satellite use. This will enable commercial services to be in full operation across Europe by January 2005.

While UMTS is a European concept, ETSI officials stress that the choice of the technology standard will ensure that, so far as is practical, it will allow compatibility and interworking with similar third-generation mobile communications systems in other parts of the world. These systems will be built in Japan and North America as part of a family of advanced mobile communications systems designated IMT-2000 by the International Telecommunications Union.

IMT-2000, ETSI says, will allow UMTS terminal users to roam from network to network worldwide.They also are quick to point out that although UMTS is regarded as a "third-generation" system, there's no intention that it should be seen as displacing existing "second-generation" digital cellular networks that are based on the current GSM standard.

The new system is expected to enhance, extend, and complement the facilities currently provided by such systems. ETSI, working with the American National Standards Institute (ANSI) T1P1 Standardization Committee, has developed technical standards that will allow existing GSM networks to be enhanced to incorporate new hardware and software features dubbed GSM Phase 2+.

These features will provide data communications of up to 64-kbit/s and higher. The integration of other previously independent wireless-data projects also is under consideration for even higher data rates for small, wideband hot-spots.

Two such projects underway at ETSI that could provide complementary services to UMTS are the Mobile Broadband Systems and the Broadband Radio Access Network project, BRAN. The Mobile Broadband Systems will operate at around 42.5 to 43.5 GHz and 65 to 66 GHz and provide up to 155-Mbit/s applications. The BRAN project includes radio services such as Hiperlan, a high-speed LAN intended for up to 25-Mbit/s data rates in indoor, localized environments. ETSI says that it also plans to explore the relationship between UMTS and wireless local-loop applications.

All this planned connectivity has implications for the design of user terminals. In particular, ETSI has come up with the notion of what it calls "soft" multistandard terminals. In theory, such a device could be reprogrammed, while in use, enabling it to comply with whatever network is most convenient to use at the time.

Software to reconfigure the mobile unit will be downloaded over the radio link, and could be determined by what type of connection a user needs. For example, it can be an asymmetrical connection for Internet access where the downlink needs to provide the highest possible data rate while the uplink from mobile to network can tolerate relatively low speeds. Or, it can be a video

TABLE 1. CANDIDATE TECHNOLOGIES FOR UMTS TERRESTRIAL RADIO ACCESS (UTRA)

Candidate Technology	Proposing Consortium
Wideband Direct Sequence Code Division Multiple Access (CDMA)	CSEM/Pro Telecom of Switzerland, Ericsson from Sweden, France Telecom/CNET, Nokia, Siemens
	Fujitsu Europe Telecom R&D Centre
	NEC Technologies (UK) Ltd.
	Panasonic-Matsushita Europe, Matsushita Communications Ind. Ltd.
Orthogonal Frequency Division Multiplex (OFDM)	Sony International (Europe) GmbH
	Telia Research
	Lucent Technologies
Wideband Time Division Multiple Access (TDMA)	CSEM/Pro Telecom, Ericsson, France Telecom/CNET, Nokia, Siemens
Wideband TDMA/CDMA	Swill Telecom PTT
	CSEM/Pro Telecom, Ericsson, France Telecom/CNET, Nokia, Siemens
Opportunity Driven Multiple Access	Vodafone Ltd., Salbu R&D (Pty) Ltd. of South Africa
Flexible Frames Structure	Philips Consumer Communications, Philips Research
Multi-Dimensional Packet Reservation Multiple Access (MD PRMA)	NEC Technologies (UK) Ltd., Kings College, London

Source: ETSI, June 1997

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Cable assemblies are available through the following:

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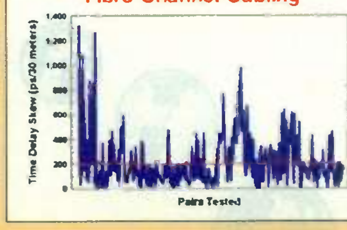

Other fibre channel cable designs create unacceptably high skew — the entire length must be inspected to find skew <200ps/30m.

TurboQuad™ cabling is designed to provide consistently low skew — increasing reliability and reducing cost.

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TABLE 2. EUROPEAN MOBILE MARKET

Market in 2005	Total Mobile Market	Mobile Multimedia Segment[1]	Mobile Multimedia (as % of total)
Users (millions)	200	32	16
Service revenues (billions $)	104	24[2]	23
Traffic (million Mbytes/month)	6320	3800	60
Traffic (million Mbytes/user/month)	32	119	

Notes:
1. In this study, data services such as DECT and ISDN services, and future data services delivered via GSM (General Packet Radio Service or High-Speed Circuit Switched Data) are counted as multimedia services. Present circuit-switched data services in GSM (<10 kb/s) or short message services are not part of multimedia services.
2. Plus a further $10 billion from terminal revenues.

Source: UMTS Forum, June 1997

telephone call (where symmetrical high speed is required), narrowband voice, and so on.

One concept that will be introduced when GSM network operators open Phase 2+ features is the Virtual Home Environment. This concept means that any terminal can present subscribers with a familiar set of service options and a human interface, irrespective of network or location.

One perceived advantage of the soft terminal approach is that rigid technical standards for terminals can be kept to a minimum, side-stepping tedious approvals and harmonization testing procedures that have traditionally been mandatory for any telecommunications equipment in Europe.

Apart from RF hygiene, the mandatory standards are likely to be limited to an insistence on software compatibility. While no firm decisions have been announced, the industry is saying that ETSI will insist on the use of a language such as Java.

A decision to go soft for terminal technology also means that market analysts conclude there will be opportunities for a wide variety of terminals tailored for specific applications. For example, Clare McCarthy, a senior consultant with London-based Ovum Ltd., has identified 24 potential applications ranging from simple text, voice, and video-based electronic mail to full video conferencing and live video relays from sporting events. She says that each is likely to require one of three possible approaches to mobile multimedia terminal design: one based on portable computers, one derived from electronic organizers or pocket computers, and one which is, effectively, an enhanced traditional mobile telephone.

One factor that may have a significant effect on terminal design is, that where UMTS is concerned, European regulators may no longer want to make a distinction between telecommunications services and entertainment broadcasting. Indeed, the British government has stated that it will raise no objections to the idea of UMTS subscribers using their mobile telephones to watch TV.

Estimates of market size vary depending on why the forecast is being made. McCarthy is very careful not to overestimate and mislead potential equipment manufacturers. As a result, she predicts that by 2005, there will be around 16 million mobile multimedia terminals in use in Europe. On the other hand, the UMTS Forum—an organization with 80 members including network operators, service providers, and equipment makers—is more concerned that sufficient RF spectrum is opened up for UMTS applications over the next 20 years, and thus, is more inclined to over estimate.

Dr Monika Bezler, chairperson of the UMTS Forum's market aspects group, predicts that there will be 32 million such terminals in use in 2005, although she points out that she has counted users of GSM Phase 2+ services as well as UMTS terminals *(Table 2)*. Both Bezler and McCarthy agree that by 2005 there will be 200 million digital mobile telephones and terminals of all kinds in use throughout Europe.

Peter Fletcher

READER SERVICE 130

Objects Push A Paradigm Shift In Distributed Computing

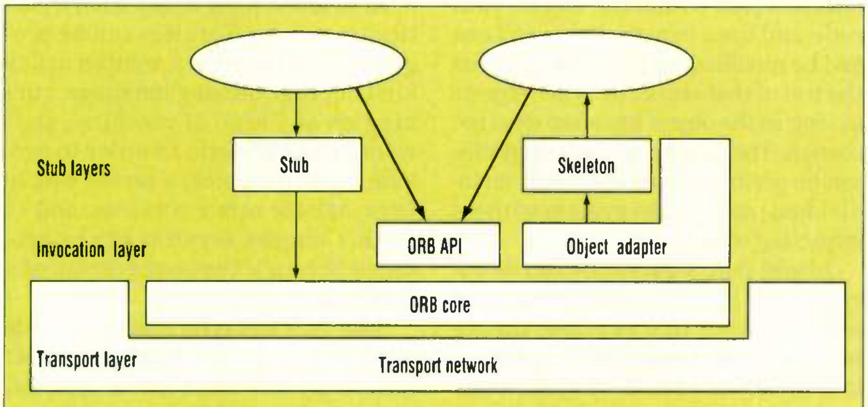
The Common Object Request Broker Architecture Facilitates Work On Applications Without The Worry Of Communication Issues.

MICHEL GIEN, Chorus Systems, 1999 S. Bascom Ave., Suite 400, Campbell, CA 95008; (408) 879-4116.

The Internet has changed the way the world does business. It also has given new life to a 20-year old programming methodology—object-oriented programming. The Internet ushered in a world of standardized transport mechanisms, browsers, and distributed applications, then fired our imaginations to figure out how objects could be applied to this global network. Distributed objects became the hottest technology of the year due to three distinct product trends:

- The remarkably rapid acceptance of light objects such as those produced by Sun Microsystems' Java. The objects are simpler to produce than ever, and offer cross-platform capabilities, as well.
- The rise of component-style, object-based architecture in enterprise applications. The basic concept of plugging in additional functionality is being applied to applications ranging from Netscape's Navigator to Oracle's WebServer cartridges to SAP AG's R/3. IT shops are starting to think in similar ways about building functional components for in-house applications.
- The Common Object Request Broker Architecture (CORBA), which is the glue that holds all of these systems together. CORBA allows objects to locate each other and interact on any network, without having to know their implementation. Thus, the vision of truly worldwide interoperable distributed computing can become a reality with objects and CORBA.

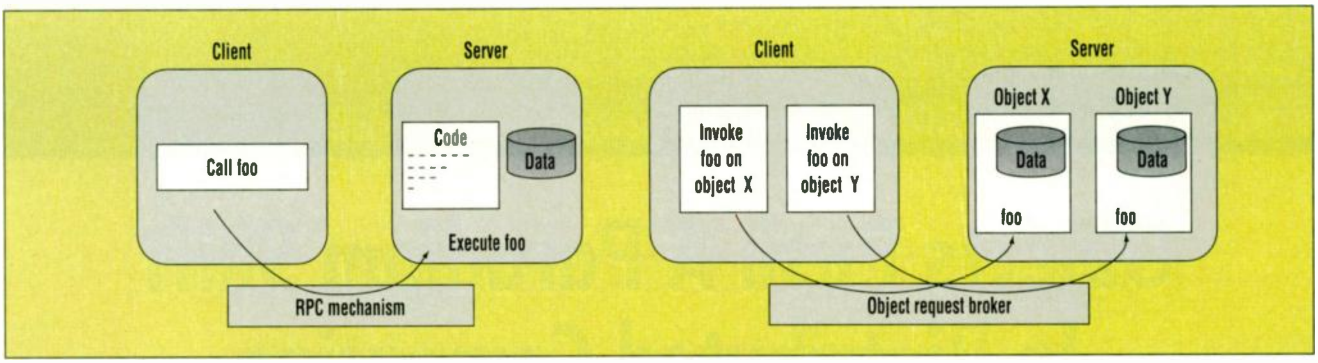
The allure of objects is compelling. Distributed objects can unify application architectures in a way that has never been attempted before, providing leaps in improved productivity, as well as cross-platform compatibility. Developers can easily develop, use, or re-use distributed software components that interoperate independently of hardware, network, or software platforms. This feature is particularly important in the embedded systems field where devices may operate without a GUI front end. Objects allow the designer to add incredible functionally such as interactive remote access from a JAVA-based terminal to real-time objects. Objects are also key to the software architecture of today's Internet appliances such as set-top boxes and web phones. However, the challenge of incorporating objects, and more importantly, CORBA is a daunting one.



1. In the CORBA model, objects communicate over a software bus by references. Any object requesting service is a client, and the object supplying the service is the server. Objects communicating on the same machine would not use the transport network. The network is transparent to objects that use it to communicate between separate computers.

RPC To Distributed Objects

During the mid-1980s, distributed system architectures were defined by two key software trends: client/server computing based on the concept of Remote Procedure Call (RPC), and object-oriented programming supported by such programming languages as C++. The software became more of a determining factor of the overall system capability than either the hardware or networks. The limitations of the software-constrained architectures often were defined by the implementations of the RPC-based client/server and object-oriented software.



2. The remote procedure call (RPC) differs from the ORB model in that the calling process assumes that the server is identical, in terms of protocols, programming language, and operating system environment. RPCs communicate in terms of network addresses, while ORBs communicate by object reference.

Today, a major architectural shift in the computing industry is taking place again. The distributed characteristics of the client/server computing model are being combined with a system-wide object software perspective, referred to as "distributed-object computing." It is being widely adopted within the embedded systems marketplace for the scalability and functionality offered by distributed objects.

Object-Oriented Programming

Object-oriented programming is a design and program structuring concept. An object is a software component or building block providing some services. The designer only needs to know the interface to the object to access its services. The actual code and data that implement the services within an object are invisible outside of that object. They are encapsulated within the object.

Encapsulating software functions within objects provides a straightforward way of decomposing complex applications and software systems into a set of simpler components implemented as objects, and interacting through their object interfaces. Interface and implementation need not be specified and written at the same time. Different embedded system design and programming teams can separately implement the functions (also called methods) of a set of objects without the need to interact with other teams implementing other objects. A controls expert, for example, can build the control objects, and a less-experienced application engineer can then apply them quickly and correctly. Such an approach is recursive, and objects can be made of other objects of finer grain and so forth.

An important benefit of object-oriented programming is the ability to reuse objects in different contexts. Object software is organized into hierarchical classes and subclasses. Starting from libraries of object classes, engineers can create new classes or extend existing ones by inheriting properties of previously defined classes when new services are needed. Those new classes will then be available for future uses, possibly in different contexts, saving programming, reducing testing, and ensuring consistent operation

Polymorphism is a characteristic that allows object methods to react differently, depending on specific class or subclass membership. For example, this characteristic would allow a pump object to respond differently if it were part of a reactor unit than if it were part of a mixer.

Because the code and data that implement the services of an object are encapsulated within the object, such code and data can evolve over time and be modified without any effect on the use of that object by other objects as long as the object interface does not change. Therefore, software upgrades can be performed transparently on individual parts of the system without impacting others.

In addition, legacy code can be encapsulated into objects by wrapping a software layer that provides the object interface around the old code, allowing current embedded system software to be used as a foundation layer.

Reusability of legacy code, as well as commercial off-the-shelf (COTS) software components enabled by object-oriented programming, allows developers to focus their energy on application-specific objects that implement their own core added-value. This feature makes their products more competitive, and faster to market.

Object-oriented languages have been designed to support that model. Smalltalk was the precursor; C++ was designed as an object-oriented extension of the C language; and Java is the latest born. Eiffel, Ada, and Objective-C are other examples of object-oriented programming languages.

Distributed Objects

The client/server model of today's enterprise computing is undergoing a fundamental paradigm shift. The model is moving from the concept of a two-way interaction, supported by the remote procedure call (RPC) paradigm, to the concept of distributed services. In a distributed system, clients request services, and not applications. Clients do not know how and where services are implemented. They only need to know what to ask from a particular service. Services can be programs or data servers, written in any kind of programming language, running on any kind of machine, anywhere on a network. In order to provide a given service, a server can, in turn, ask for other services, and so forth. Complex services can be provided through the cooperation of a multitude of servers.

This very powerful concept is made possible by the introduction of object technology into client/server systems. As seen above, objects provide services through well-defined interfaces. Distributed objects extend access to their services to other objects running on other computers in a network.

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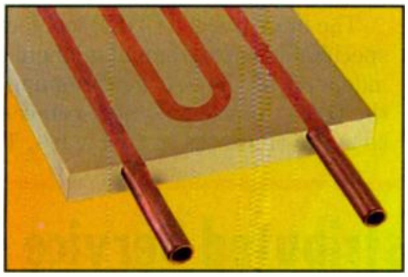

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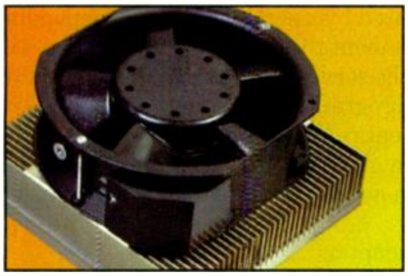

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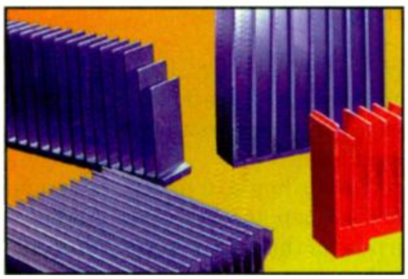

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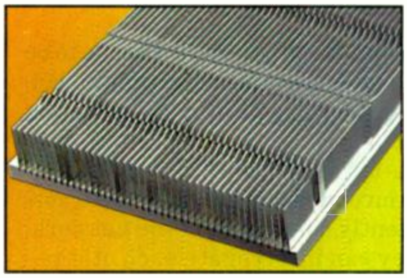

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Distributed objects don't have to be written in the same programming language or run on the same operating system and computer. Distributed objects are smart pieces of software that can invoke each other's services transparently, anywhere in the network. They can interrogate each other—"tell me what you do." Distributed objects are very dynamic; they come and go, and move around.

Today, the IT industry is building distributed-object applications that span networked desktops and services taking advantage of the increased network bandwidth. Those applications allow geographically separated hardware components to participate in a single computer system, like the Internet does.

The environment that lets objects talk to each other so that developers can share them among different applications, operating systems, and hardware platforms is the Common Architecture Request Broker (CORBA). CORBA is a set of standards developed by the Object Management Group (OMG), which comprises over 700 member companies developing or using distributed-object systems and applications.

CORBA defines a standard language, the interface definition language (IDL), used to express the interfaces to access the services provided by an object. IDL is independent of the programming language used to write the code of client and server objects. Standards for mapping the IDL to common programming languages such as C, C++, or Java have been defined by the OMG.

At runtime, invocation of object services is supported by an object request broker (ORB). The ORB allows objects to interact with each other even when they don't know about each other. It translates service invocation requests and their associated parameters from a client object into the format understandable by the server object. The ORB then transports requests and replies by underlying operating systems and networks *(Fig. 1)*. It acts like a standard software bus that also can interact with proprietary object protocols such as Microsoft's ActiveX (OLE/COM).

A client, in CORBA terminology, is a computational context that makes requests on a CORBA object through one of its references. A CORBA object is an abstract programming entity with an identity, an interface, and an implementation. From a client's perspective, the object's identity is encapsulated within the object's reference.

The interface of a CORBA object is specified in a programming-language-independent IDL. A client running on the ORB can use an object reference to make requests in two ways. The

Implementing A Distributed Service With CORBA

The following example shows how to implement a simple distributed service using CORBA. The purpose of the service is to allow clients to print messages on a remote console. This service is provided by a single CORBA object representing the console. The interface for this CORBA object is defined in the OMG IDL, as follows:

```
interface Console {
    void print(in string message);
};
```

The console object will be implemented by a server program. Depending on the ORB, it may be possible to implement the service in a way where the ORB plays an active role in launching the server program. However, for simplicity, we will assume that the server program is started by a means outside of the ORB, and that it will run for the entire lifetime of the service.

While the details may differ, depending on the ORB and the object adapter being used, the server program must generally perform the following tasks:

- Initialize the ORB and the object adapter.
- Create a programming language entity (code and data) incarnating the CORBA object. This entity is called the servant. In this example, the servant will be a C++ object.
- Bind an object reference representing the CORBA object with the servant and the skeleton, which the ORB will use to call the servant.
- Make the object reference available to clients.
- Wait for invocations.

A client of the console service must generally do the following:

- Initialize the ORB.
- Obtain an object reference for the CORBA object providing the service.
- Use this object reference to make requests.

The most common, and simplest, way of implementing CORBA programs uses compiler-generated stubs (client) and skeletons. The dynamic invocation interface and the dynamic skeleton interface provide increased flexibility, but are more difficult to use, and usually less efficient.

Stub and skeleton code are generated according to a programming language mapping for IDL, in our case the C++ mapping. How this is done depends on the IDL compiler. For the purpose of this example we will assume that the following four files are generated:

console.H - header file for the stub for the Console interface
console.C - implementation of the stub, compiled and linked with both client and server programs
sk_console.H - header file for the skeleton
sk_console.C - implementation of the skeleton, compiled and linked with the server program only.

(continued on page 130)

most common way is through a compiler-generated stub. Using the stub, a request takes the syntactic form of a native programming-language-object invocation, or function invocation. The advantage of using a stub is that invocations are type checked (dynamic or static check, depending on the programming language used). Moreover, the implementation of stub-based invocation can be highly optimized.

Alternatively, the client can use an object reference together with the dynamic invocation interface (DII). The DII allows a client to make invocations without compile-time knowledge of the object type. Independently of the way the invocation is performed, the ORB directs the request to the server identified by the object reference. A server is a computational context in which the implementation of an object resides. Generally, a server corresponds to a process or task. When a request is received in a server, the server identifies the Object Adapter used by the object implementation. An object adapter is an identifiable entity within the context of a server. A server may support multiple object adapters.

The object adapter is responsible for locating, and possibly creating, a servant incarnating the invoked CORBA object. A servant can be anything executable, for instance a script, but typically it takes the form of a programming language object, such as a C++ object. The object adapter also must locate the skeleton through which the servant can be invoked. Generally, the skeleton can take two forms: static and dynamic. A static, compiler-generated skeleton transforms a request into an appropriate invocation of the servant. A dynamic skeleton uses the dynamic skeleton interface (DSI). When using a dynamic skeleton, the application must provide a generic implementation for all operations of the CORBA object interface. Finally, the server invokes the servant through the skeleton.

The application code executing in the server must register CORBA objects in an object adapter. This operation is called binding. Also, a binding is an object-adapter-maintained relationship between a CORBA object, and the different elements making up its implementation. Bindings also may include skeleton code which allows the object adapter to access the CORBA object incarnated as a programming-language-servant object, and code or information which allows the object adapter to locate, and possibly create, a servant object incarnating the invoked CORBA object.

Servants are instances of application code while the skeleton is typically provided by the IDL compiler. In general, a servant is only associated

(continued from page 128)

The servant used in the server to incarnate the console object must be an instance of a C++ class, which implements the console interface. Different styles of implementation classes have been specified by the OMG. Here we show one of the styles supported by the CHORUS/COOL ORB.

```
#include "sk_console.H"

//
// Implementation class for Console, skeleton inheritance style
//
class ConsoleImpl : public _sk_Console {
public:
        void
    print(const char* message, CORBA_Environment&);
};
```

Using the CHORUS/COOL ORB, the server program's main function could look like this:

```
#include <api/api.h>
#include <stdio.h>
#include "consoleImpl.H"

    int
main(int argc, char* argv[])
{
        // Initialize the ORB and the Object Adapter.
    CORBA_ORB_ptr orb = CORBA_ORB_init(argc, argv, 0);
    CORBA_BOA_ptr boa = orb->OA_init(argc, argv, 0);

        // Instantiate the servant incarnating the CORBA object.
    ConsoleImpl consoleImpl;

        // Bind the servant to a new object reference.
    Console_ptr console = consoleImpl._this();

        // Export the object reference to the simple COOL naming service.
        // The CORBA naming service could be used for added portability,
        // but the example would grow.
    COOL_NamingService_var naming = thisCapsule->naming_service();
    naming->export("consoleService", console);

        // Wait for invocations.
    boa->run();
    return 0;
}
```

A simple client for writing "Hello World" on the console would look like this:

```
#include "console.H"

    int
main(int argc, char* argv[])
{
        // Initialize the ORB.
    CORBA_ORB_ptr orb = CORBA_ORB_init(argc, argv, 0);

        // Obtain the object reference from the COOL naming service.
    COOL_NamingService_var naming = thisCapsule->naming_service();
    CORBA_Object_ptr obj;
    naming->import("consoleService", obj);
    Console_ptr console = Console::_narrow(obj);
    CORBA_release(obj);

        // Call the Console service.
    console->print("Hello World!\n");
    return 0;
}
```

PETER JENSEN, Chorus Systems

with the CORBA object during an invocation. A CORBA object need not be incarnated by the same servant each time it is invoked. The mapping of CORBA objects to servants is the sole responsibility of the object adapter (*see "Implementing A Distributed Service With CORBA," p. 128*).

The ORB

The role of the ORB is to send requests and receive replies, using the services of an underlying transport network (e.g., TCP/IP). However, many embedded-system applications need some control over the execution resources, not only for the application's own use of these resources, but also for the ORB's. Platform-independent abstractions of such resources are provided by a new generation of ORBs targeting real-time embedded systems.

For example, the CORBA ORB standard implemented by Chorus Systems' CHORUS/COOL provides flexible bindings to optimize object invocations depending on an object's location, operating system capabilities, and network protocols. In addition, it's componentized structure allows the optimization of the memory footprint and run-time performance by installing only those ORB services required by the application and the supporting configuration. This design allows minimal ORB profiles well adapted to various embedded system constraints.

Real-Time Is On The Mark

Many of today's embedded systems interact with a physical environment requiring real-time systems in which timing constraints must be met for the application to be correct. The environment produces stimuli, which must be accepted by the system within time constraints. Time-constrained behavior can obviously be critical to not just mission success, but to the safety of property and human life in the case of transportation systems or air-traffic-control software.

In addition, most embedded systems need to operate continuously, 24 hours a day, seven days a week, with a behavior that remains acceptable, even in the case of faults. Moreover, distributed embedded systems also need to be integrated with other distributed embedded systems as well as distributed enterprise systems, in multitier architectures. Such multitier architecture includes the control or operational layer, consisting of a network of control computers, connected on an industrial bus in process control systems, or on a signaling network in telecommunications systems.

Many companies building these types of critical systems are looking for the combination of a real-time embedded ORB with a real-time operating system platform that is fully configurable and componentized. For example, the CHORUS/ClassiX communication-oriented RTOS platform

A given ORB implementation can take advantage of an underlying RPC mechanisim (e.g. DCE).

can accommodate application-defined policies, taking into account various real-time constraints as well as other embedded systems requirements such as memory footprint. Additionally, there's fine grain management of resources such as thread scheduling, memory management, synchronization, interrupt management, timers, and interprocess communication. It can support simultaneously different system and Application Programming Interfaces (APIs), in particular, for the migration of legacy applications, and conformance with recognized API standards such as RT-POSIX. Finally, it provides non-stop operation features, such as fault confinement, on-the-fly dynamic software reconfiguration, and hot-restart of system and applications.

Before There Were ORBs

Before ORBs came into fashion, the main support for message passing within a system was the RPC. However, RPCs do not offer the simple elegance offered by today's ORBs. RPCs allow communication between network addresses, while ORBs establish communications between objects (*Fig. 2*).

An RPC is a simple extension of the traditional procedure call programming facility, which refers to a procedure of a program running on a remote computer. This concept was introduced in the mid-70's in a famous research paper by Greg Nelson from DEC Research Center, Palo Alto, Calif. A client thread calls (with some parameters) a remote server procedure which processes the call and provides a reply to the client thread. The client thread remains blocked until the reply comes back from the server. A RPC facility assumes a homogeneous environment between client/server programming languages and execution environments. However, it can be complemented by standard data representation protocol. For example, the External Data Representation (XDR) standard, in order to accommodate different data representations between clients and servers. RPC is a low-level communication mechanism between procedures, within the context of a given programming language, or a given operating system environment. An example is DCE's RPC.

An ORB is a high-level communication mechanism allowing objects to invoke each others services. The main function of an ORB is to accommodate the differences between the client and server object programming language and execution environments, therefore making heterogeneity transparent. In that respect, ORBs encapsulate the RPC mechanism. A given ORB implementation can take advantage of an underlying RPC mechanism (e.g. DCE). If the communication transport layer used by the ORB does not provide an RPC facility, the ORB will need to implement it by itself, as part of its functions.

For a programmer, an ORB is much simpler to use because the ORB will automatically take care of the adjustment of the client's request to the server execution environment. The only thing that the client needs to know is the high-level definition of the server's interface described in IDL. With RPCs only the communication environment is made transparent.

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Bottom line, the ORB communication model is much richer, offering naming (instead of network addresses), security, dynamic adaptation, and other powerful features, while providing a very clear and strict framework.

From Islands To Unification

The move toward a distributed object architecture benefits engineers and companies. By removing concerns about architectural constraints, management can focus on process improvements. Future advanced system software architectures for embedded systems will behave like unified automation architectures rather than isolated islands that need to be integrated together.

The technology can be extended out onto the World Wide Web to allow access to complex software applications via browsers, to assist with such critical business operations as inventory, customer orders, and shipping and delivery.

Distributed objects offer an infrastructure that makes it easy to provide a functional analysis of an embedded system without having to worry about the physical construction of the system. This advantage will reduce configuration costs, enable faster startups, and increase the capacity to have more secure and reusable code. Object-oriented embedded systems can extend object technology right down to the instrument level. As suppliers shift their focus from dealing with architecture issues to developing distributed-object application components, they can improve the performance of their customer's installations.

Michel Gien is co-founder and chief technology officer at Chorus Systems. He joined the Cyclades computer network research team at INRIA (French National Institute for Research in Information Sciences) in 1971. In 1979, still at INRIA, he led a project that introduced Unix in France.

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WRH

UPDATE ON EMBEDDED FUZZY LOGIC TOOLS

Fuzzy Logic Tool Teams With Silicon For Compact Embedded Designs

The combination of a rich graphical development tool, along with specialized instructions added to a 16-bit microcontroller, may make it practical to use fuzzy logic in embedded applications previously not possible. Motorola's 68HC12 includes instructions for fuzzy logic. The fuzzyTECH development tool from Inform, Aachen, Germany, generates 68HC12 assembly code. The combination of the two allows designers to attack fairly complex and nonlinear applications with a well-integrated, low-cost microcontroller.

The 68HC12 is a superset of Motorola's 68HC11. Binary 68HC11 code will run on the HC12, and HC11 source code will be accepted by the HC12 assembler with no changes. Four instructions were added to the HC11 instruction set: MEM for fuzzification, REV and REVW for non-weighted and weighted rule evaluation, and WAV for weighted defuzzification. These four instructions enable a large amount of compact fuzzy processing. A trapezoidal membership function can be defined by four 2-byte values. The first two values represent the beginning point and the slope of the leading edge of the trapezoid, each to 16-bit resolution. The second two values represent the slope and end point of the trailing edge. The MEM function keeps track of the number of membership functions associated with each variable in the fuzzy rule set. It compares the variable's value to each assigned membership function, calculates its degree of membership, and stores the results.

Rule evaluation on the HC12 uses a fuzzy logic approach called the MIN-MAX method which takes the minimum antecedent in any individual rule as the overall truth of that rule. In cases where rules are assigned weights, i.e., where one rule has more influence on the outcome than others, the REVW instruction multiplies the result of each rule evaluation by a fraction representing its relative importance before sending it to the fuzzy outputs.

Once the outputs of the rule evaluation are combined into a composite output, the WAV instruction computes a single, "crisp" output value. While there are a number of different "defuzzification" methods, the HC12 uses the singleton method. For each membership function in the output, it takes the "singleton" or height of that trapezoid at its center. The crisp output is calculated by averaging the output values of the singletons weighted by their heights.

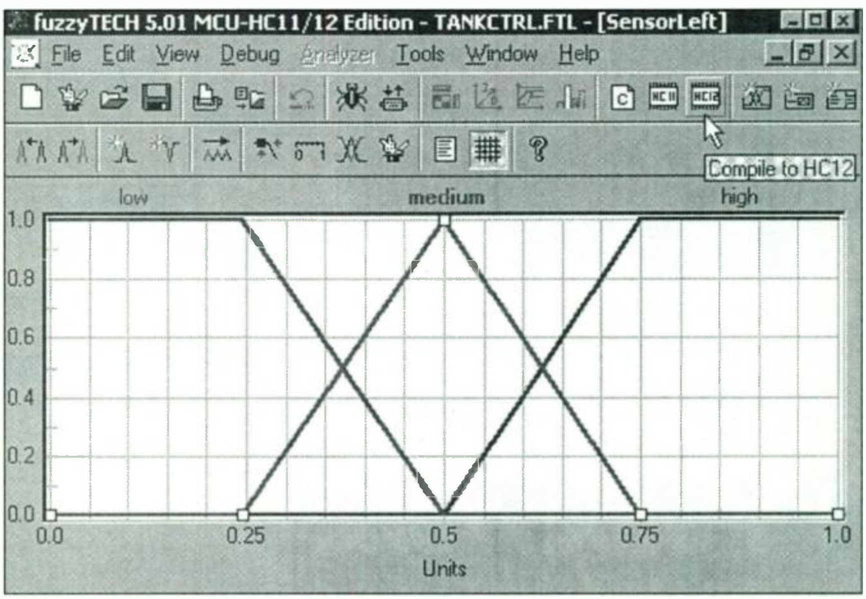
The software that performs fuzzification is the fuzzy inference kernel. The kernel's size depends on the number of rules, the number of antecedents (IF, AND, OR), the number of consequences (THEN) per rule, and the number of input and output variables and membership functions assigned. Using the fuzzy instructions on the 68HC12, a fuzzy control example employing two input variables and one output variable with seven membership functions each, and 17 rules, each with two antecedents and one consequence, is compiled to 54 bytes. It ran an evaluation in about 66 µs at 8 MHz. The same control example on the 8-bit 68HC11 compiled to 262 bytes and ran in about 750 µs at 4 MHz. Part of the difference is in the code.

Embedded fuzzy logic has been implemented using a fuzzy coprocessor and a standard microprocessor, but inter-chip communication overhead and costs have been high. Other approaches involve high-speed 32-bit processors, appropriate for some cases but not for small, cost-sensitive applications.

The Motorola/Inform combo is aiming at low-cost, high-speed applications such as anti-lock braking, disk-drive head-positioning control, and auto ignition control. These applications have complex, often nonlinear, problems along with very short control-loop requirements, where a traditional mathematical model would be too slow. Fuzzy logic on a fast, 16-bit microcontroller can often do the job at a speed and cost point that is practical for the application.

The fuzzyTECH development tool provides a completely graphical environment for creating and editing rules, setting up membership functions, implementing inference methods, and selecting defuzzification techniques. Some of these steps are enhanced by design wizards. For example, the Fuzzy Design Wizard prompts the user with a series of dialog boxes to generate a fuzzy system prototype. Another wizard, the Fuzzy Variables Wizard, assists in creating complete variable definitions.

The linguistic variable editor lets you assign a name to an input variable and define its membership functions *(see the figure)*. Both the variable and the membership functions have linguistic names. For example, the variable "tempera-



fuzzyTECH's membership function editor lets you assign membership functions to linguistic variables. Here, the variable SensorLeft has three membership functions. An input value of 30 would have a degree of membership of 0.8 in the function "Low," and a degree of membership of 0.2 in "High."

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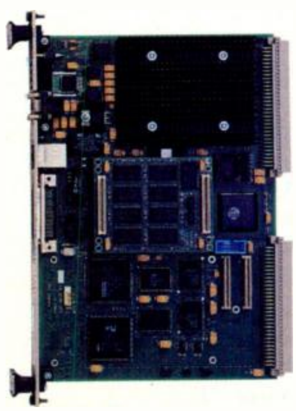

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ture" might have membership functions called "cold," "cool," "comfortable," "warm," and "hot." Each membership's function is drawn as a graph representing the degree to which any given temperature value satisfies the concept of "cool," "warm," and so on *(see "Fuzzy logic makes a decision," p. xxx)*. These are the degrees of membership, or degrees of "truth," used in fuzzy inference. Fuzzy logic performs logical operations using degrees of truth rather than absolute ones and zeroes.

Once variables are defined, they need to be combined in logical rules of a form like: "IF Speed is High AND Tree is Near THEN Brake is Hard." The actual values associated with high speed and the nearness of the tree will determine the actual hardness to be applied to the brake. The output of this one rule will then be combined with the outputs of other rules to determine the final, crisp, result. The fuzzyTECH tool provides three different editors for creating and modifying the rule base. One editor uses a spreadsheet format that can provide a good overview of small rule bases. For more complicated applications, there is a matrix rule editor that lets you work with entire slices of the rule base at once. Rules also can be edited in a text format using Inform's hardware-independent Fuzzy Technology Language.

There also is a choice of inference methods, including MIN-MAX described above and MAX-PROD. There also is a set of operators for rule aggregation, including compensatory operators which more closely represent human decision making. Defuzzification techniques include the singleton method described, plus others like the center of gravity and the mean of maximum method used in pattern recognition.

Also included in fuzzyTECH are interactive optimization tools for system tuning. A 3D plot lets you see the behavior of system outputs relative to inputs, and a statistical analyzer shows how frequently individual rules are firing and helps identify redundant or unneeded rules. The debug mode gives access to all the rule editors, membership function editors, and other editors to let you dynamically see the status of any given element while the system is running. You also can modify a rule or membership function on-the-fly and observe resulting behavior. The fuzzyTECH version for the HC12 has a cross-link debugging mode that uses the chip's background debug mode (BDM) port for accessing memory to fine-tune a running system. This avoids interference with system operation that would occur if you used a serial port. For instance, you can change the shape of a membership function associated with a variable and observe the change in the system's behavior. At the same time, you can see the results in a trace window inside fuzzyTECH.

Motorola supplies a $99 evaluation board (68HC912B32), bundled with a copy of the limited-function Explorer version of fuzzyTECH HC11/12. The full version of plus add-on modules for neuro-fuzzy systems, real-time optimization, and data analysis starts at $2290.

Contact Motorola MCU Information, P.O. Box 13026, Austin, TX 78711; (800) 765-7795, X985; *http://www.mcu.mot-sps.com*. Inform Software (U.S.), 2001 Midwest Rd., Oak Brook, IL 60521; *http://www.fuzzytech.com*.

TOM WILLIAMS

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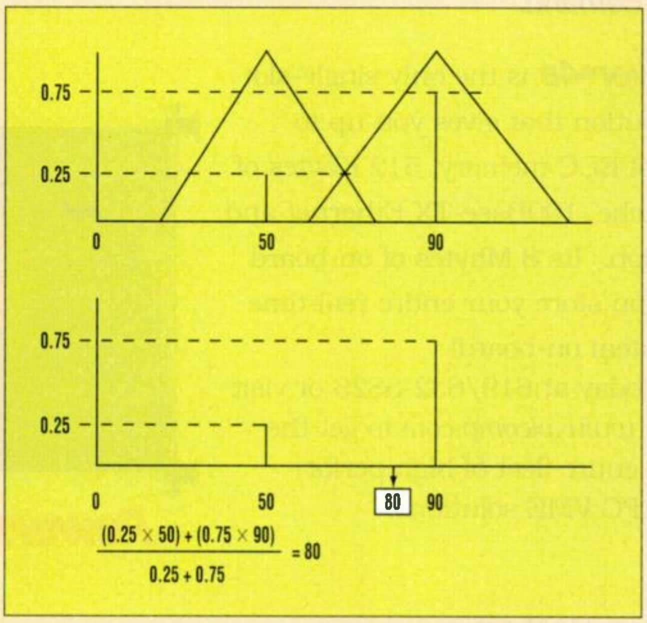
Fuzzy Logic Makes A Decision

Many factors can go into deciding how to cool a room. Among them are temperature, humidity, light intensity, and the number of people in the room. Then there are options for accomplishing the goal: how much to run the compressor, fan speed, if and how far to open vents, and so on. In this simple example, two rules in a fuzzy application have determined, on the basis of their input values, two different fan speeds—50 rpm falls in the "medium" membership functions, while 90 rpm falls into "fast." There could possibly be another category "real fast," if desired.

Note, however that the degree of truth (the vertical axis) output by each rule is less than 100%. One rule determines a speed of 50 rpm to only 25% while the other recommends 90 rpm to 75%. The latter rule will thus have more influence on the final outcome, but the first rule will also contribute. The singleton method averages the two output values weighted by their heights. In this case, the final fan speed would be 80 rpm, and the two rules in question might have been something like:



IF Temp is High AND Humidity is Medium THEN Fan is High

and

IF Temp is High AND People is Low THEN Fan is Medium

The corresponding outputs for fan speed are resolved as shown *(see the figure)*.

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ERA-2SM	DC-6000	15.2	12.4	4.6	26.0	40	2.00
ERA-3	DC-3000	20.8	12.1	3.8	23.0	35	2.10
ERA-3SM	DC-3000	20.2	11.5	3.8	23.0	35	2.15
ERA-4	DC-4000	13.5	▲17.0	5.5	▲32.5	65	4.15
ERA-4SM	DC-4000	13.5	▲16.8	5.2	▲33.0	65	4.20
ERA-5	DC-4000	18.8	▲18.4	4.5	▲33.0	65	4.15
ERA-5SM	DC-4000	18.5	▲18.4	4.3	▲32.5	65	4.20
ERA-6	DC-4000	11.3	▲18.5	8.4	▲36.5	70	4.15
ERA-6SM	DC-4000	11.3	▲17.9	8.4	▲36.0	70	4.20

Note: Specs typical at 2GHz, 25°C. Exception: ▲ indicates typ. numbers tested at 1GHz.
* Low frequency cutoff determined by external coupling capacitors.
① Price (ea.) Qty 1000: ERA-1 $1.19, -2 $1.33, -3 $1.48, -4, -5 or -6 $2.95. SM option same price.

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K3-ERASM: 10 each ERA-4SM,-5SM,-6SM (30 pieces) only $99.95

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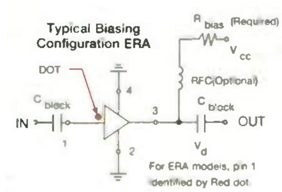
Size (mils)	Value
80x50	10, 22, 47, 68, 100, 220, 470, 680, 1000, 2200, 4700, 6800, 10,000 pf
120x60	.002, .047, .068, .1 µf

ERA-1 ERA-1SM
ACTUAL SIZE



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Circle 520

Create A Quiet –5 V Supply For 14-Bit ADCs

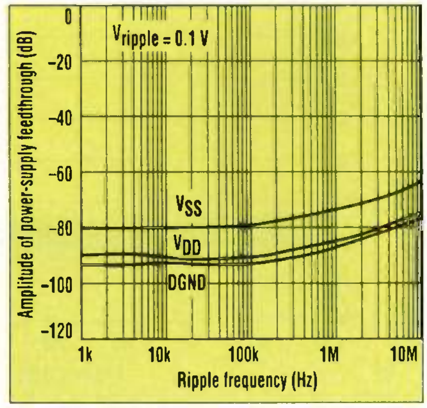
KEVIN R. HOSKINS
Linear Technology Corp., 1630 McCarthy Blvd., Milpitas, CA 95035-7417; (408) 432-1900; fax (408) 434-0507.

Many high-performance data-acquisition systems reap multiple benefits when using ±5-V supplies rather than a single 5-V supply. These benefits include the ability to handle larger signal magnitudes than is possible with a single 5-V supply. This increases a system's dynamic range and helps improve the signal-to-noise ratio. Operating on ±5 V also increases headroom, which is important for signal conditioning.

Compared to operating on 5 V, conditioning circuitry operating on ±5 V has twice the headroom, allowing it to easily handle ±2.5-V signals without clipping. In addition, the greater headroom avoids the limitations of rail-to-rail operation and widens the selection of high-performance op amps and analog-to-digital converters (ADCs).

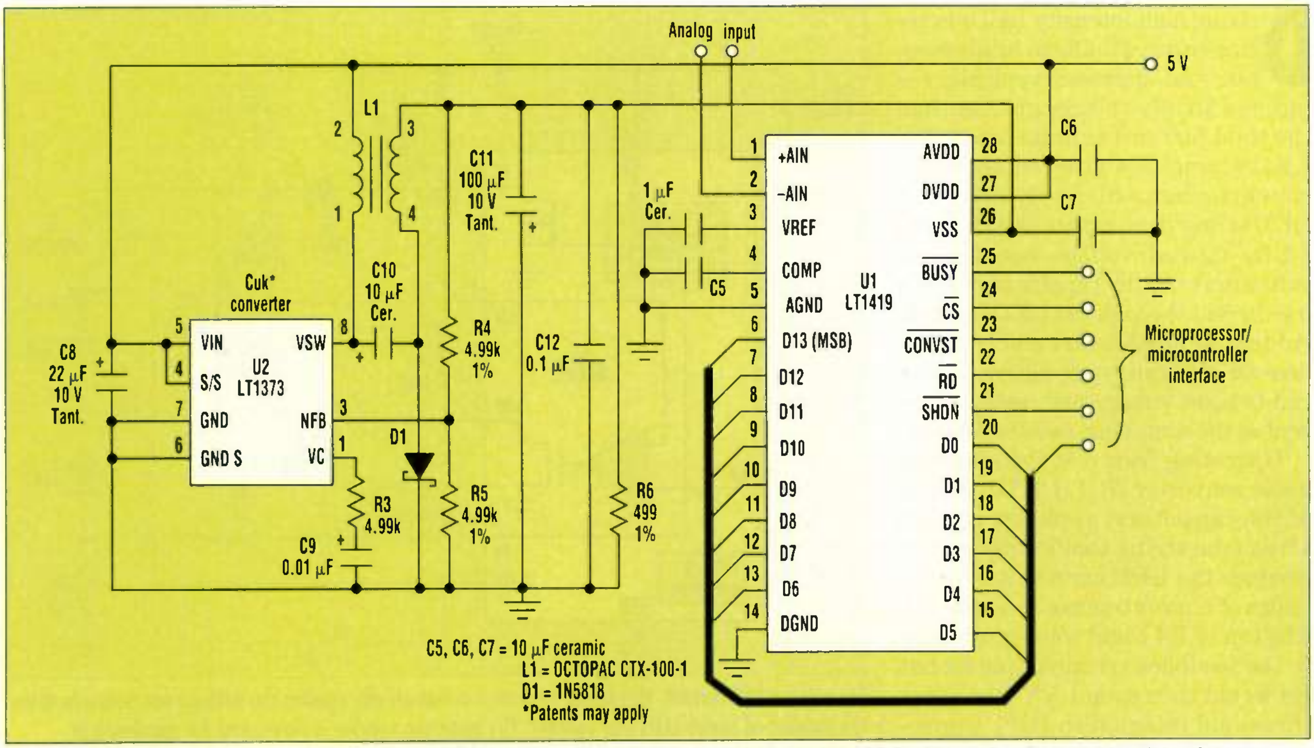
A switching or charge-pump power supply is an efficient way to create a –5-V supply from a single 5-V supply. However, these circuits aren't generally recommended for use with ADCs, which typically have inadequate power-supply rejection ratio (PSRR) that decreases with increasing frequency.

The circuit described here combines two features to enable the ADC to achieve 14-bit performance *(Fig. 1)*. The first feature is the low-noise Cuk-configured switching regulator (U2). This configuration has the advantage of a small triangular switching-current waveform through the secondary inductor. This current waveform is continuous, producing much less harmonic content than is created by a typical positive-to-negative voltage converter with its rectangular switching current waveform. The second feature is U1's very high PSRR *(Fig. 2)*. Figure 2 shows that when operating on ±5 V, the negative and positive PSRR are typically 80 dB and 90 dB, respectively, up to 200 kHz for a 100-mV ripple voltage. Combined with the proper layout, the U1's high PSRR allows it to convert signals without signal degradation while using Figure 1's Cuk switching regulator.

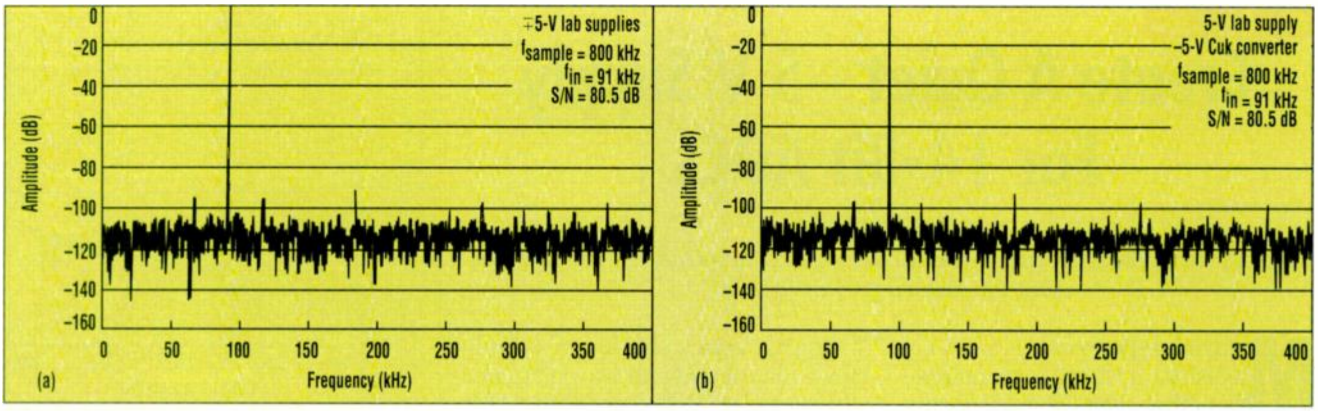


2. U1's positive-supply PSRR of 80 dB and its negative-supply PSRR of 90 dB up to 200 kHz provide a significant contribution to this ADC's wideband conversion performance and its 80-dB SINAD.

Excellent results were derived with the fast Fourier transforms *(Figs. 3a and 3b)*. Figure 3a is an FFT of U1 operating on ±5 V from a lab supply and converting a full-scale 91-kHz sinewave at 800 ksamples/s. The noise floor is approximately 114 dB below full scale; the second harmonic's



1. U1's 80-dB PSRR allows switching regulator U2 to generate the –5 V supply that powers the ADC without signal-conversion degradation.



3. This FFT of U1, powered by a ±5-V lab supply, shows a SINAD of 80.5 dB for a 91-kHz input sampled at 800 ksamples/s (a). When U1's –5-V supply is generated by a Cuk switching regulator based on U2 (b), the SINAD (80.5 dB), the noise floor, and the 91-kHz fundamental's harmonic components remain essentially the same as those shown in (a).

amplitude is approximately 90 dB below full scale; and the SINAD is 80.5 dB. Figure 3b shows the FFT of U1 operating on a 5-V lab supply and –5 V from the U2-based Cuk circuit. The noise floor and the second harmonic's amplitude remain the same relative to full scale, and the SINAD remains the same at 80.5 dB.

Circle 521

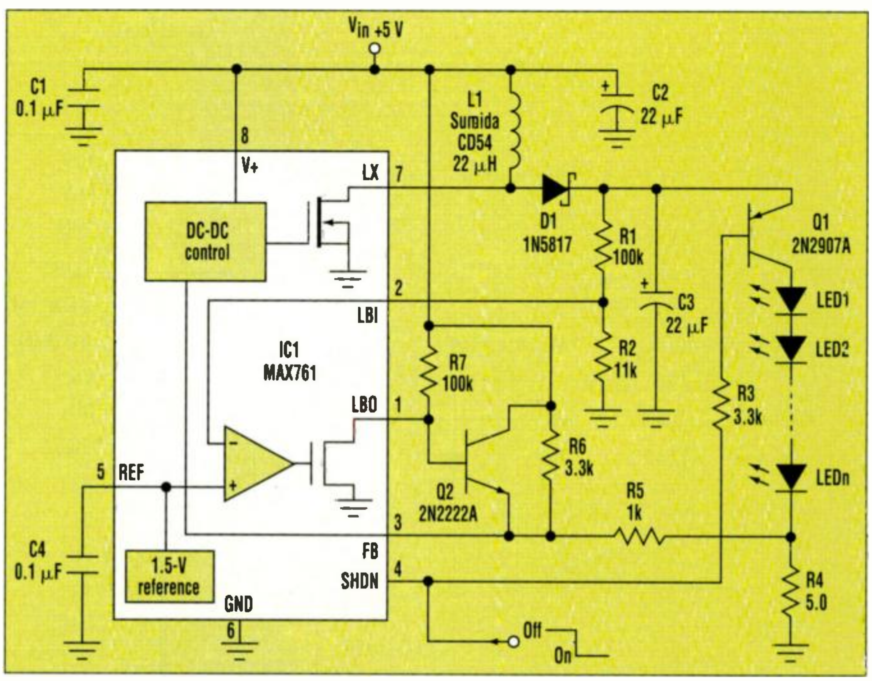
Logic Power Drives High-Intensity LEDs

LEN SHERMAN
Maxim Integrated Products, 120 San Gabriel Dr., Sunnyvale, CA 94086; (408) 737-7600.

Driving high-intensity LEDs in series ensures uniform brightness, but that approach typically requires a supply voltage greater than the total forward voltage across the LED string. A switch-mode boost converter can efficiently drive the LED string from inputs less than the LEDs' forward voltage, but such circuits aren't usually capable of regulating current through the LEDs as well. Adding some resistors and two garden-variety transistors allows the circuit to boost voltage and regulate current at the same time *(see the figure)*.

Operating from 5 V, the standard boost converter (IC1, L1, D1, and all of the capacitors) applies a voltage across the string that's sufficient to produce the LED current set by the value of current-sense resistor R4. The top of R4 could connect directly to the feedback terminal (pin 3), but R4 would then drop 1.5 V (the sense threshold internal to IC1). Consequently, it would dissipate excessive power equal to 1.5 V × I_{LED}. R5 and R6 form a divider with V_{in} that introduces an offset, shifting the low-level feedback from R4 to a level usable at the FB terminal. Together, the R4-R6 values shown set the LED current at 88 mA.

When the SHDN terminal is pulled high, the switching regulator turns off. To ensure that the LEDs turn off completely during shutdown,



For a given LED current, this boost converter automatically applies the voltage necessary to drive the number of series LEDs you connect. The minimum number is three, and the maximum is determined by the maximum drive voltage (15 V).

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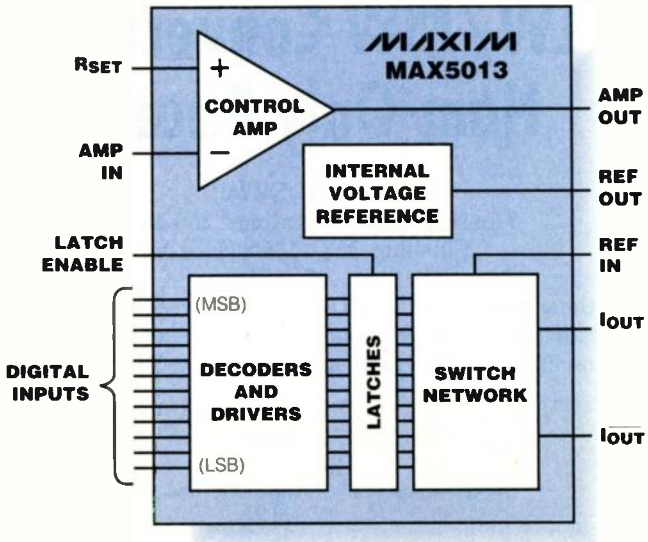

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the on/off signal also turns off a pnp transistor in series with the LEDs (Q1). Q2 and the low-battery comparator in IC1 form a protection circuit. Without it, the loss of feedback attending an open circuit in the LED string would allow excessive voltage to build on C3. If this voltage reaches the 15-V limit determined by R1 and R2, the open-drain switch at LBO turns off, allowing Q2 to turn the circuit off by pulling FB high.

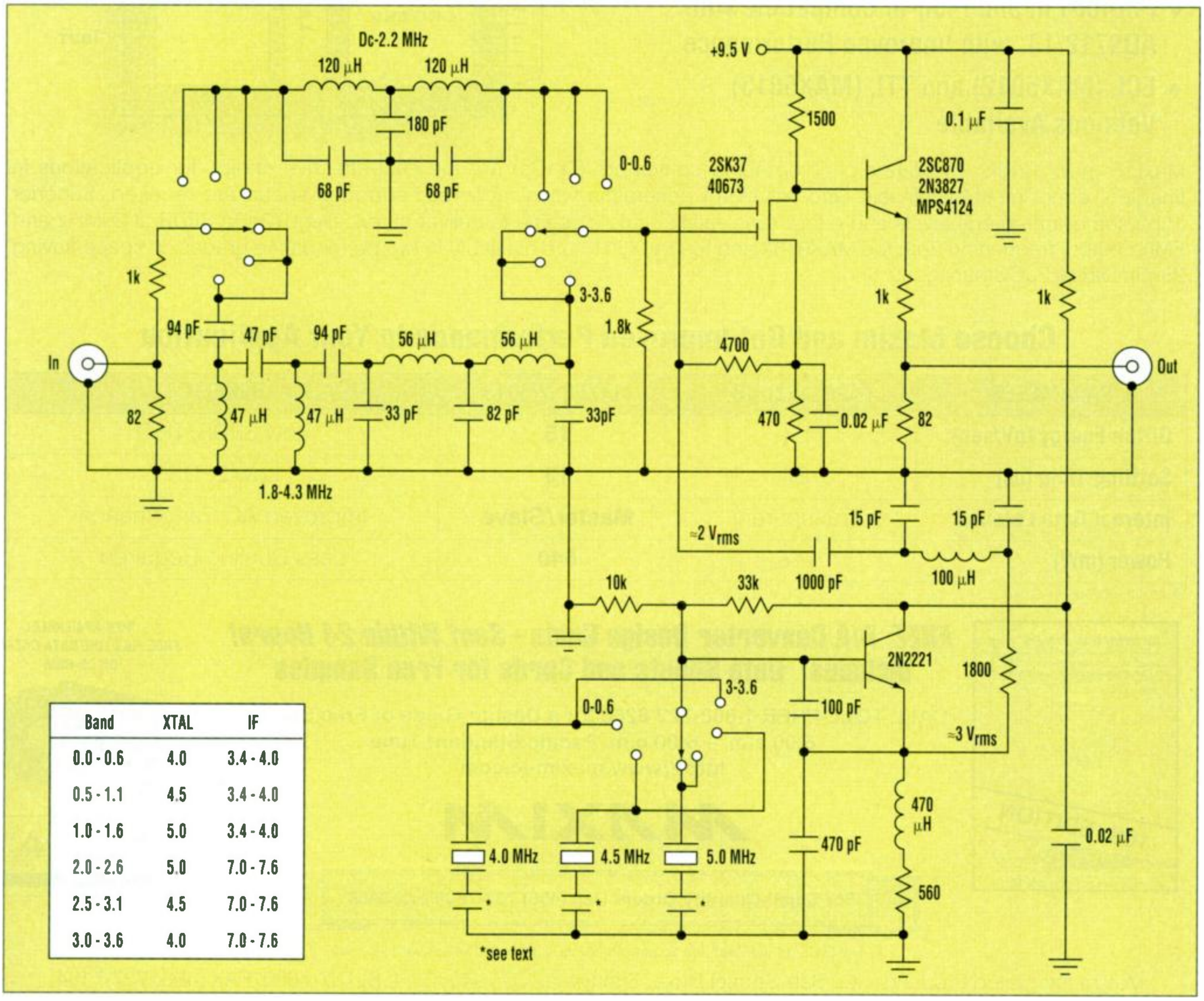
Circle 522

LW/MW Converter For Ham-Only Receivers

M.J. SALVATI
Flushing Communications, 150-46 35th Ave.,
Flushing, NY 11354; (718) 358-0932.

Before the advent of broadband communications receivers with synthesized oscillators, high-grade, ham-band receivers used crystal oscillators and a variable IF to cover relatively narrow (500-600 kHz) frequency segments. The schematic shows a circuit that will adapt most of these receivers to cover the long-wave (150-400 kHz), standard (520-1600 kHz), and tropical (2.2-2.4 and 3.2-3.4 MHz) broadcast bands, plus all of the other interesting stations in the 0.1-1.6 and 2.0-3.6 MHz frequency ranges *(Fig. 1)*.

The circuit consists of untuned bandpass filters, a MOSFET mixer, and a crystal oscillator. The only control is the band-selector switch. The actual tuning is done with the receiver itself (acting as a variable-frequency IF amplifier). Only three crystals are



Band	XTAL	IF
0.0 - 0.6	4.0	3.4 - 4.0
0.5 - 1.1	4.5	3.4 - 4.0
1.0 - 1.6	5.0	3.4 - 4.0
2.0 - 2.6	5.0	7.0 - 7.6
2.5 - 3.1	4.5	7.0 - 7.6
3.0 - 3.6	4.0	7.0 - 7.6

1. This circuit will adapt most ham-only receivers to cover long-wave (150-400kHz), standard (520-1600kHz), and tropical (2.2-2.4 MHz and 3.2-3.4 MHz) broadcast bands, as well as other stations in the 0.1-1.6 and 2.0-3.6 MHz frequency ranges.

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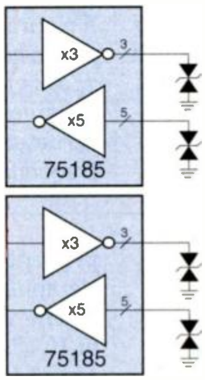

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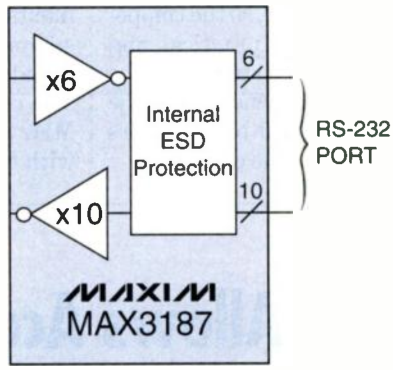

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	MAX1489E	0/4	±15	±8	±15	230	±12	1489
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	MAX1406	3/3	±15	±8	±15	230	±12	145406

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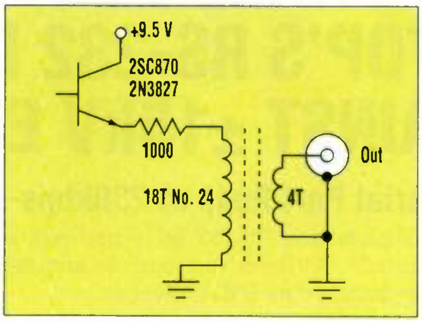
needed for six bands because the 80-meter ham band is used as a *difference* IF for the LW and MW bands, and the 40-meter ham band is used as a *sum* IF for the short-wave bands.

When one of the LW/MW bands is selected, a two-section low-pass filter with a 2.2-MHz corner is inserted to eliminate IF pickup, image frequencies, and to prevent overload by nearby shortwave transmitters. When one of the short-wave bands is selected, a two-section high-pass filter with a 1.8-MHz corner and a two-section low-pass filter with a 4.3-MHz corner are inserted for similar reasons. The design impedance for these filters is approximately 1200 Ω, so the component values are highly practical, and any mismatch in the driving source will not affect the passband shape. The mismatch at the output of the filters was found to improve the corners.



2. In this high-gain output circuit, a resistive divider was replaced with a transformer output.

The frequency ranges mentioned above and in the chart *(Fig. 1, again)* are for a receiver with 600-kHz segments. If your receiver uses 500-kHz segments, coverage of the standard broadcast band is limited to 1500 kHz. The obvious remedy is to add a 5.5-MHz crystal. The capacitors in series with the crystals are a means of excitation control. In the unit shown, they ranged from 20 to 62 pF; the values used should produce approximately 3-V_{rms} oscillator output voltage. This voltage is applied to the mixer's injection gate through a low-pass filter to eliminate oscillator harmonics. An emitter-follower with a voltage divider reduces both the mixer output level and its impedance to values suitable for a hot receiver. If higher output is needed, replace the resistive divider with a transformer output *(Fig. 2)*.

The input impedance of the circuit is 75 Ω, so it must be driven by a low-impedance signal source. A loop antenna with a 75-Ω output *(see "High-Frequency Loop Antenna,"* ELECTRONIC DESIGN, *July 22, 1996, p. 112)* is the ideal signal source, since ferrite-rod "loops" can easily be constructed to provide coverage at the frequencies involved.

Circle 523

Circuit Allows Accurate Sync Of Multiple CCTV Signals

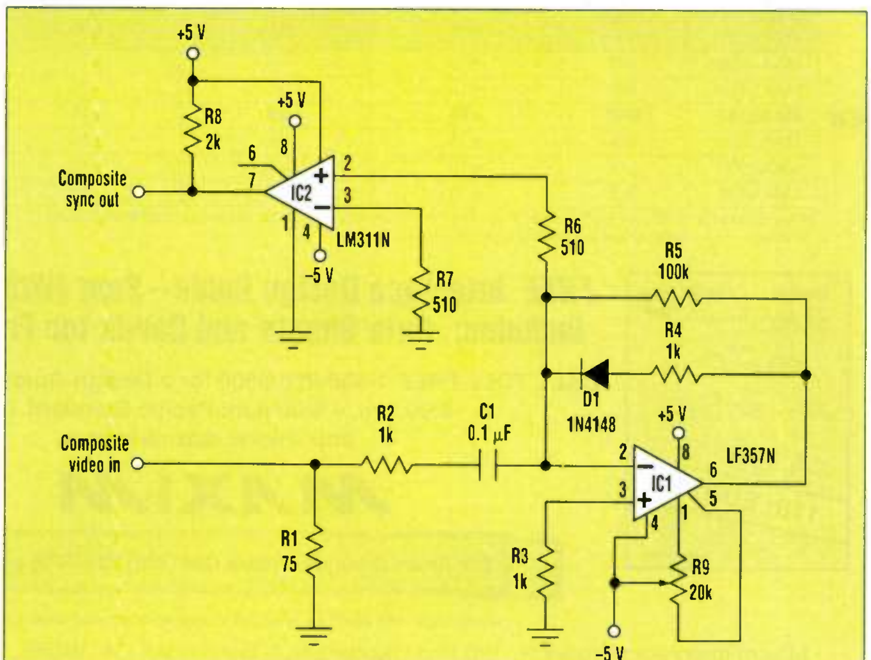
R.J. NACHAZEL
Vista Electronics, 23461 Vista Vicente Way, Ramona, CA 92065; (760) 789-2189.

There are times when CCTV sync signals must maintain temporal fidelity when derived from composite video. One such case involves applications in which several video sources are polled by an instrument which then extracts photometric data from video scenes.

The circuit described here replicates the incoming sync pulse width exactly. This allows accurate clamping at dark level, which succeeds the horizontal sync level.

The composite video input is terminated at resistor R1 and ac-coupled by capacitor C1 to the inverting input of op amp IC1 *(see the figure)*. A negative voltage is inverted by IC1 with a gain of approximately –1 because of the conduction of diode D1. This clamps the negative sync tip at the amplifier reference which, in this case, is the circuit ground. When D1 isn't conducting (the video input is positive), the amplifier input pin presents a high impedance and the clamping action ceases.

The voltage at the negative input of IC1 is shared at IC2 (positive input in this circuit, but an inverted output may be obtained by using the negative input) to create the Composite Sync Out signal. Potentiometer R8 is used to adjust the output for best symmetry.



Accurate clamping of CCTV signals at dark level is achieved by this circuit, which is able to replicate an incoming sync pulse width exactly.

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JANUARY 1999

Annual Reliability & Maintainability Symposium (RAMS), Jan. 19-21. Washington Hilton, Washington, DC. Contact V.R. Monshaw, Consulting Services, 1768 Lark Lane, Cherry Hill, NJ 08003; (609) 428-2342.

IEEE Power Engineering Society Winter Meeting, Jan. 31-Feb. 4. New York, NY. Contact Frank Schink, 14 Middlebury Lane, Cranford, NJ 07016; (908) 276-8847; fax (908) 276-8847.

FEBRUARY 1999

Photonics West, Feb. 6-12. San Jose, CA. Contact SPIE Exhibits Dept., P.O. Box 10, Bellingham, WA 98227-0010; (360) 676-3290; fax (360) 647-1445; e-mail: exhibits@spie.org.

IEEE International Solid-State Circuits Conference (ISSCC '99), February 15-17. San Francisco Marriott, San Francisco, CA. Contact Diane Suiters, Courtesy Associates, 655 15th St., N.W., Washington, DC 20005; (202) 639-4522; fax (202) 347-6109; e-mail: isscc@coutesyassoc.com.

Portable by Design, Feb. 21-25. Santa Clara Convention Center, Santa Clara, CA. Contact Rich Nass, Electronic Design, 611 Route 46 West, Hasbrouck Heights, NJ 07604; (201) 393-6090; fax (201) 393-0204; e-mail: portable@class.org.

The Wireless Symposium and Exhibition, February 21-25. San Jose Convention Center, Santa Jose, California. Contact Bill Rutledge, Penton Publishing, 611 Route 46 West, Hasbrouck Heights, New Jersey 07604; (201) 393-6259; fax (201) 393-6297; instant faxback (800) 561-7469; Internet: www.penton.com/wireless.

MARCH 1999

Southeastcon '99, March 25-29. Marriott Resort Hotel, Lexington, Kentucky. Contact Don Hill, 1676 Donelwal Drive, Lexington, Kentucky 40511-9021; (606) 257-8487; fax (606) 323-1034; e-mail: d.w.hill@ieee.org.

MAY 1999

IEEE/IAS Industrial & Commercial Power Systems Technical Conference (I&CPS), May 3-6. Nuggett Hotel, Sparks, Nevada. Contact Kerry Flannigan, Sierra-Nevada Power Co., Post Office. Box 10100, Reno, Nevada 89520; (702) 689-4848; fax (702) 689-4139.

JUNE 1999

IEEE/MTT-S International Microwave Symposium (MTT '99), June 13-18. Anaheim, California. Contact Robert Eisenhart, 5982 Ellenview Avenue, Woodland Hills, California 91367; (818) 716-1995; fax (818) 713-1161.

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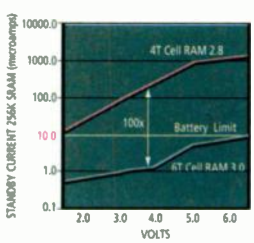

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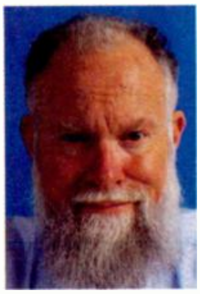
Once upon a time there was a little boy named Epaminandas. *(This is an old esaeP's Fable.)* His mother told him to go out and play. So he went out and played around his neighborhood, and after a while, his neighbor Miss Suzie called to him, "Epaminandas, let me give you a nice piece of cake to take home to your mother." Epaminandas soon started home with a piece of cake in his hand.

But by the time he got home, the cake was in terrible condition, as the little boy had clenched it tightly in his fist. When he got home, his mother asked, "Epaminandas, what do you have there?" And the boy explained about the piece of cake. His mother said, "If anybody ever gives you a present like that, bring it home on top of your head."



BOB PEASE OBTAINED A BSEE FROM MIT IN 1961 AND IS STAFF SCIENTIST AT NATIONAL SEMICONDUCTOR CORP., SANTA CLARA, CALIF.

The next day, Epaminandas went out to play. After he wandered around the neighborhood for a while, his Aunt Ann called out, "Epaminandas, come over here and I will give you something to take home to your mother." She gave Epaminandas a pound of freshly-churned butter. As soon as he got out of Aunt Ann's house, he put the butter on top of his head and put on his hat, and went directly home.

It was a hot day. When he got home, the last of the butter was just dribbling down his face, his back, and his ears... and his mother asked him, "Epaminandas, what do you have there?" Epaminandas explained how his Aunt Ann had given him a gift, and he brought it home just like he had been told.

Epaminandas' mother was somewhat exasperated. She told him, "Epaminandas, you foolish boy, the next time somebody gives you a gift like that, you should take it down to the spring, and hold it under the water until it is cool, and then put it on some green leaves, and carry it home."

The next day, Epaminandas went out to play. He walked up by his Grandmother's house. She called out to him. "Epaminandas, I want to give you a kitten to take home." The little boy very faithfully took the kitten down to the spring, and held it under the water until it was cool. And like he was told, he then put it on some green leaves and brought it home.

When he got home, his mother soon figured out what had happened. She said, "Epaminandas, you foolish boy, if anybody ever gives you a gift like that again, put a string around its neck, and lead it home behind you."

The next day, Epaminandas went out to play. It was nearly noon when he went by his Aunt Dorothy's house, and she called out to Epaminandas to bring a gift home to his mother. She gave him a loaf of freshly-baked bread. He put a string around its neck, and led it all the way home. By the time he got home, there wasn't much left of it.

His mother said, "Epaminandas, you foolish boy, you surely do everything just wrong. Now, I am going out to do some shopping. You stay home. I just baked six pies. You mind how you step in the middle of those pies." So Epaminandas waited until his mother had left, and then he stepped *very carefully* right in the middle of each pie. *(End of Fable)*

This was a fable that my mother Beulah Pease used to tell me when I was small. Surely an esaeP's Fable. I think I caught onto the message: that there were times when following explicit instructions could be wrong. Sometimes common sense is required. Even if the coach did tell you to run 3 plays and then punt, if you have been able to get down to the 5-yard line, first-and-goal, it might be reasonable to call a time-out and get permission to go in for the touchdown.

Now I just borrowed a copy of this old FABLE from a library. This story was published about 1912, and the only substantive difference between that story and what my mother told me was having a puppy instead of a kitten. And all the characters in that published story were African-American. I guess those days were closer to the days of slavery than 1997. I'll let you do the subtraction, and the politically-correct debates.... Having the characters in a story speak in Ebonics was "politically correct" or acceptable then. But my mother didn't tell it with Ebonics. Epaminandas was just another little boy. She sure did know a lot about little boys.

In fact, she used to tell me at times when I had gotten her really *provoked*, "When you grow up, I hope you have a little boy just like you." Such a terrible curse!!

My mother told me about the time when I was small and she was pouring me some milk. I said, "Enough." But she kept on pouring. So I took the glass away, and the milk spilled on the table. And she *whacked* me...and I don't doubt that I deserved it.

A number of years later, I was pouring some milk—out of a *glass* milk-bottle—for my 4-year-old son Benjamin. He said "Enough." He tried to pull his glass away. BUT I held the lip of the bottle on his glass, and I would not let him pull it away until I was ready to stop pouring. We never spilled a *drop*.

I sometimes see ads about the electronic circuits that can make a dog obey by giving them a shock when they get too close to a fence-line, or when they bark too much. My comment is, "Will it work on Product Engineers?" Because sometimes, product engineers are told exactly what to do —and then they go and do something else. Sometimes it is *exactly* wrong.... I know of some specific examples, but I *refuse* to recite them here.

PEASE PORRIDGE

BOB PEASE

Now, someone will surely say, "Bob, *you* wouldn't put an electronic shocker on a Product Engineer just because he made some mistakes, would you?" And he surely wouldn't like my answer—because I surely would. At least on a few of them that I have done business with. A couple that didn't have any better judgement than Epaminandas did....

One reader told me about the time he took his car in to get "smogged," recently. He *instructed* the technician that he should do the testing without linking the computer to the official computers in Sacramento, because it was not likely to pass—he suspected a leaky hose.

When he came back, he found that the technician had decided it probably would pass, so in order to save time, he left the computer linked up. Unfortunately, the car failed. The car was then listed PERMANENTLY as a "gross polluter." When the car's owner contacted the DMV in Sacramento, Calif., he was told that it was *impossible* to have the "gross polluter" designation removed. My advice to the owner was to have the technician figure out how to get it removed, because it was *his* mistake. If he couldn't undo his error, the owner should take the technician to small claims court. Sue him for several thousand dollars, which represented the decrease in value of the car from what it used to be worth. Or maybe he could get one of those dog-collars, and turn up the voltage, and take it out of his hide....

There are many times when a person has to break rules. He just has to be aware of the problems—or consequences—in case he has made an error when breaking the rule.

All for now. / Comments invited!
RAP / Robert A. Pease / Engineer
rap@webteam.nsc.com—or:

Mail Stop D2597A
National Semiconductor
P.O. Box 58090
Santa Clara, CA 95052-8090

P.S. Note, there once was a man named Epaminondas who was a politician and general for Thebes in Ancient Greece about 405 to 362 BC. None of the stories I read about him indicated any problems with his failure to follow instructions.... / rap

Logic-Synthesis Tool Aimed At High End

BuildGates, a logic-synthesis tool that addresses the issues of productivity bottlenecks in high-performance complex IC design, offers improved timing results, on average 10%. Also, capacity is 5 to 7 times greater that current synthesis methods.

BuildGates can offer these benefits thanks to a number of unique features incorporated into its modular architecture. The first, an algorithm-based technology mapping feature, eliminates cumbersome rule sets and speeds runtimes. In fact, the tool can work with million gate designs and supports multiple, simultaneous delay calculators, including linear, nonlinear and user-defined.

Another unique feature is its static timing-analysis engine based on a pin-based timing algorithm. With this algorithm, information is stored at each pin in the net list, thereby enabling incremental updates and automatic time budgeting across blocks. This feature allows fast analysis of large designs and accurate exception characterization of false and multicycle paths.

As an added feature, the tools modular architecture can support hierarchical synthesis with automatic constraint management. BuildGates is available now and is compatible with current design flows. It supports both Verilog and VHDL and can run on both SunOS and Solaris platforms. Pricing starts at $85,000. CA

***Ambit Design Systems**, 2933 Bunker Hill Rd., Suite 215, Santa Clara, CA, 95054; (408) 566-8000.* **CIRCLE 490**

In-Circuit Emulator Targets HW/SW Co-Verification

The Avatar product, a clone of the VirtuaLogic emulation system but without the debugging features, aids with hardware/software co-verification issues. Very simply, a verified design implementation on the VirtuaLogic emulation system is downloaded to Avatar from the compiler database using a simple one-step process. This "replica" of the design in the Avatar system can then be used by the software designers and system integrators for their testing and integration purposes.

Using replicates of emulated designs (multiple copies of early prototypes) within the design flow allows companies to perform system-integration testing prior to committing to fabrication. And, by parallelizing hardware regression, and software and system debug, the design teams project schedule can be shortened significantly. The tool is transparent to the user, other than the fact that it operates in much the same way as the silicon would.

The Avatar is available now, with cost depending on capacity size. The base tool, with a capacity of up to 200,000 gates, sells for $100,000. Additional capacity starting prices are 400,000 gates for $175,000; 600,000 gates for $250,000; 800,000 gates for $325,000; 1,000,000 gates for $400,000; and 1,200,000 gates for $475,000. CA

***IKOS Systems Inc.**, 19050 Pruneridge Ave., Cupertino, CA 95014; (408) 255-4567.* **CIRCLE 491**

READER SERVICE 127

Source Code Tool Guides Users Through Large Projects

A multiplatform graphical browsing and editing tool lets programmers visualize the structure and scope of large-scale software projects. Called Source-Navigator, the tool lets teams of developers navigate C, C++, Java, Tcl, and Fortran code bases. In large projects, there's a need to understand existing legacy code that may have been poorly documented and written by people who are no longer with the organization. Source-Navigator can help developers identify which components in a project will be affected by code changes.

Built on browser and database technology, Source-Navigator parses and builds a database of the project and provides real-time querying of code relationships. This includes relationships such as cross-references and hierarchy. The database is interfaced to a graphical display so that users get a visual feel for the architecture of the software. The symbol browser contains information about classes, member functions, and the files where they are located.

Source-Navigator is available now for WindowsNT and a variety of Unix platforms. Pricing starts at $3000. There's also a free single-user version called Source-Navigator Lite. TW

Cygnus Solutions, 1235 Chesapeake Terrace, Sunnyvale, CA 94089 (408) 542-9600. **CIRCLE 492**

Tools Support Embedded Development for PowerPC

CodeWarrior for PowerPC Embedded Systems supports Motorola's MPC821 and MPC860 PowerPC embedded processors. CodeWarrior for PowerPC Embedded Systems has all of the tools, libraries, documentation, and examples needed to develop—on a Windows 95/NT platform—software for the MPC821 and MPC860 embedded processors.

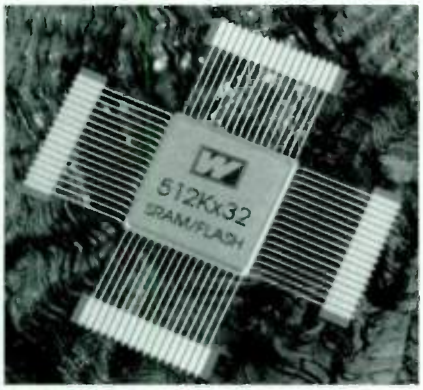
Features include: Metrowerks' Integrated Development Environment (IDE); optimizing C/C++ compiler; support for PowerPC EABI (Embedded Applications Binary Interface), ELF (Executable and Linkable Format) / DWARF (Debug With Arbitrary Record Format) object files; support for Motorola's S-Records; and source- or assembly-level debugging.

Using the CodeWarrior Debugger for PowerPC Embedded Systems from a desktop computer, a programmer can debug software running on Motorola's MPC821/860ADS bare board, any MPC8xx board that supports BDM (Background Debug Mode), or even a PowerPC system that has an RS-232 serial port. For debugging software running on a PowerPC-based RTOS (Real Time Operating System), CodeWarrior for PowerPC Embedded Systems includes MetroTRK (Target Resident Kernel), a software debug monitor. CodeWarrior for PowerPC Embedded Systems is priced at $899. Purchasers also receive a BDM cable with power cable and a serial cable for source-level debugging. TW

Metrowerks, 2201 Donley Dr., Suite 310, Austin, TX 78758 (512) 873-4700. **CIRCLE 493**

Module Mixes SRAM And Flash Memory Types

Combining the two most commonly used memory types in embedded systems, the WSF512K32-29XX module packs up to 16 Mbits of SRAM and 16 Mbits of flash nonvolatile memory. The



SRAM block has an access time of 25 ns, while the 5-V flash memory can perform reads at 90 ns and has 10,000-cycle write endurance. Both memory blocks are organized as 512 kwords by 32 bits, and the flash memory uses a sectored architecture consisting of eight 64 kbyte sectors, any combination of which can be concurrently erased.

The dual memory combo comes in either a 66-pin hermetic ceramic package that's 1.385 in. on a side, or a 68-lead CQFP, which is just 0.18 in. thick and fits the JEDEC standard 0.990-in. CQFJ footprint. Available in commercial, industrial, and military temperature ranges, the modules are available from stock to eight weeks. Prices for the high-reliability hermetic modules in lots of 100 start at less than $1000 per unit. DB

White Microelectronics, *4246 E. Wood St., Phoenix, AZ 85040; Philip Farahmand, (602) 437-1520; or on the web at http://www.whitemicro.com.* CIRCLE 494

Dual-Port SRAMs Allow Internal Bank Switching

The bank-switchable dual-port SRAMs in the 7072xx and 70V72xx series offer double the bandwidth over conventional multiplexed SRAM-based system designs. They occupy less board area while delivering comparable cost-per-bit value in high-performance applications. Address-to-data-access times are as short as 15 ns for either port, while power consumption of the SRAMs at maximum speed is typically just 900 mW.

Based on a proprietary architecture, the dual-port devices provide up to 1 Mbit of storage, and are internally organized into banks within a common memory array. The chips each have two independent ports, with separate control, address, and I/O pins. This enables each port to provide asynchronous access to any free memory block. Accesses to specific banks are controlled by external bank select input pins (via user direct control), or via software control (with semaphore signals. Mailboxes and interrupts are provided to allow interprocessor communications.

The bank-switchable SRAMs are housed in 100-lead TQFPs (14 mm on a side), and are available in sample or production quantities. Prices for the devices range from $19.95 apiece in production quantities for the 707278 (a 32-kword-by-16-bit, 25-ns memory) up to $32.95 each for the 70V72288, a 64-kword by 16-bit, 20-ns device. DB

Integrated Device Technology Inc., *2975 Stender Way, Santa Clara, CA 95054; Bill Beane, (408) 754-4685; or on the web at http://www.idt.com.* CIRCLE 495

Serial EEPROM Packs Secure Storage For DIMMs

The 34WC02, a serial-presence-detect (SPD) memory for DIMM memory modules, provides 256 bytes of serially accessible EEPROM storage (via an IIC interface) and meets the JEDEC requirements for the SPD device for DIMMs. The first 128 bytes (addresses 0 to 7FH) store the presence detect and the DIMM manufacturer's information. The remaining 128 bytes are available for the PC manufacturer to store additional manufacturing or system information.

A 16-byte on-chip page register helps reduce the time required for write operations. Protecting the first 128 bytes from corruption is critical, because those bytes contain the identifying information needed for system initialization. They could even affect module functionality or cause a voiding of the product's warranty if changed.

The 34WC02 includes both hardware and software protection schemes to ensure data integrity. Software protection prevents inadvertent writes by locking out write pulses to the first 128 bytes of the memory array (the remaining 128 bytes can be written to or read from). To activate this mode, users must send a write command to the memory's One-Time-Programmable write-protect register. Hardware protection is accomplished via a signal pin that's tied to the supply voltage—when the supply is present the entire chip is write-protected. This hardware mode also overrides the software mode and write-protects the second 128-byte block.

The memory operates from a 1.8 to 6-V power supply and consumes less than 1 mA when active and near zero current when on standby. Package options for the memory include plastic miniDIPs, SOICs, and TSSOPs. In lots of 10,000 units the 34WC02 sells for $0.90 each. DB

Catalyst Semiconductor Inc., *1250 Borregas Ave., Sunnyvale, CA 94080; (408) 542-1112; or on the web at http://www.catsemi.com.* CIRCLE 496

Real-Time Clock Chips Support ACPI Standard

Able to comply with the advanced configuration and power interface (ACPI) standard, the bq3285LD (for 3-V systems) and bq3285ED (5 V) real-time clock circuits now include a day-of-the-month alarm, as well as all of the features included in the previous-generation bq3285 clock circuit. The day-of-the-month alarm will be used as part of the overall "wake up" scheduling built into all new computers and is a requirement for all computers that have the Microsoft Windows logo in 1998.

In addition to all of the alarm settings, the clock chips include 242 bytes of nonvolatile data storage and a 32-kHz output that can be used for memory refresh and processor communication timing. The clock can operate from the backup and provide a 10-year data retention time as well as clock operation in the absence of power. Price for either the LD or ED version is $3.63 each in lots of 5000 units. The clocks come in 24-lead SSOPs. DB

Benchmarq Microelectronics Inc., *17919 Waterview Pkwy., Dallas, TX 75252; Paul Nossaman, (972) 437-9195; http://www.benchmarq.com.* CIRCLE 497

Conditioning Card Carries Filters, Sample-And-Hold

The DBK45 signal-conditioning card combines filtering and sample-and-hold functions on one four-channel PC-plug-in card for applications that must have minimized skew and high-frequency aliases. The four differential or single-ended inputs each has a low-pass filter, simultaneous sample-and-hold, and BNC connector. A set of supplied plug-in headers allows users to configure each filter individually for cut-off frequencies from dc to 50 kHz, with Butterworth, Chebyshev, or Bessel characteristics. The card captures signals from the multiple inputs concurrently within 50 ns of each other. Up to 64 cards can be attached to one DaqBook, DaqBoard, or Daq PC-Card data acquisition system for a total of 256 differential inputs. The DBK45 costs $695. JN

IOtech Inc., 25791 Cannon Rd., Cleveland, OH 44146; (216) 439-4091; fax (216) 439-4093; e-mail: sales@iotech.com; http://www.iotech.com. **CIRCLE 498**

VXI Controllers, Embedded Computers Run The Gamut

A full line of slot 0 controllers, interfaces, and embedded computers for the VXIbus covers a wide range of applications and price points. For low-cost applications, GPIB- and RS-232-to-VXIbus slot 0 interfaces are available starting at $1600. For applications requiring the communications speeds of the VXIbus backplane and the use of external host computers, MXIbus-to-VXIbus slot 0 interfaces are available. Prices for the interfaces start at $4335.

Low-cost embedded modular computers and high-performance embedded Pentium-based computers are offered for portable standalone applications. In addition, they can be employed in applications that require embedded processing. Pricing for the embedded modular computer starts at $4995. JN

VXI Technology Inc., 17912 Mitchell, Irvine, CA 92614; (714) 955-1894; fax (714) 955-3041. **CIRCLE 499**

PowerPC Emulator Includes Trace, Software Breakpoints

The SPS-1000 is a mid-range PowerPC emulation tool for users who need capabilities that aren't supplied by standard background tools. A very flexible, high-speed coax connects the SPS-1000 main unit to a processor-specific pod that attaches to the target system. Features include 128 software breakpoints that can be set in ROM or RAM, an address trigger point with delay for capturing trace data around a specific address of interest, and a 128K (512K optional) trace buffer. Also included is SourceGate II, the company's source-level debugger software, which accepts output file formats from all major compilers. The SPS-1000, with 128K of trace memory and a choice of MPC505, MPC8xx, or PPC40x pod, and SourceGate II costs $6995. Additional pods cost $3000. JN

Huntsville Microsystems Inc., P.O. Box 12415, Huntsville, AL 35815; (205) 881-6005; fax (205) 822-6701. **CIRCLE 500**

Automated System Checks CMDA, PCS Telephones

The CDMA Automatic Test System (CDMA-ATS) y tests cellular and PCS phones for adherence to CDMA performance standards. The system comes with predefined test suites for TIA IS-98A, ANSI J-STD-018, and CDG test standards. Users also can define and execute custom test procedures. On the hardware side, the system uses the TAS 4500 FLEX RF channel emulator, which simulates RF propagation conditions (multipath fading, log-normal fading, etc.).

Also part of the system is the TAS 4600 noise and interference emulator, which mimics carrier-to-noise and carrier-to-interference conditions. Control functions are performed by the TASKIT/CDMA software. CDMA-ATS prices start at $144,000. JN

Telecom Analysis Systems Inc., *34 Industrial Way East, Eatontown, NJ 07724; (908) 544-8700; fax (908) 544-8347; e-mail: 76546.2353@compuserve.com.* **CIRCLE 501**

Software Writes Vectors For Non-Boundary-Scan ICs

A cluster testing tool, the Acutap AACDB software, automatically creates vectors for non-boundary-scan devices so that designers can use whole-chain boundary-scan testing on boards that have non-scan devices. When used with the ATGEN test-generator software, the new tool generates board-level cluster tests for any system that uses the Teradyne Victory boundary-scan software. The tool includes a library of popular SSI and MSI device models and supports fault-dictionary-based fault diagnosis. The product requires the ATGEN base software, device model support, and the JED2Z18 tester translator. It runs on Intel-architecture PCs, Sun Sparc systems (Solaris I and II), HP 9000/700 (HP-UX), et al.. Prices for the Acutap AACDB tool start at $6000. JN

Acugen Software Inc., *427-3 Amherst St., Suite 391, Nashua, NH 03063; (603) 881-8821; fax (603) 881-8906; e-mail: acugen@acugen.com.* **CIRCLE 502**

Palm-Size Emulator Handles Intel 80486, AMD Am486

The SuperTAP emulator line has been expanded to cover the Intel 80486 and AMD Am486 families of microprocessors. The SuperTAP 486 supports real-time emulation for SX and DX processors up to 66 MHz. Zero-wait-state overlay memory is available to 33-MHz bus speeds. Versatile communications options for the palm-size unit include serial and Ethernet for Windows 3.11, 95, and NT, as well as Unix platforms.

The CAD UL XDB debugger and linker/locator (Link386 linker/locator for the Am486), and SuperTAP 486 make up an integrated tool chain with full support for 16- and 32-bit architectures on PC and Sun hosts . Pricing for 66-MHz support, 64K trace, 1 Mbyte of overlay memory, 32-bit time stamp, Ethernet and RS-232, debugger, linker, and locator is $16,995. JN

Applied Microsystems Corp., *P.O. Box 97002, Redmond, WA 98073-9702; (206) 882-2000; Internet: http://www.amc.com.* **CIRCLE 503**

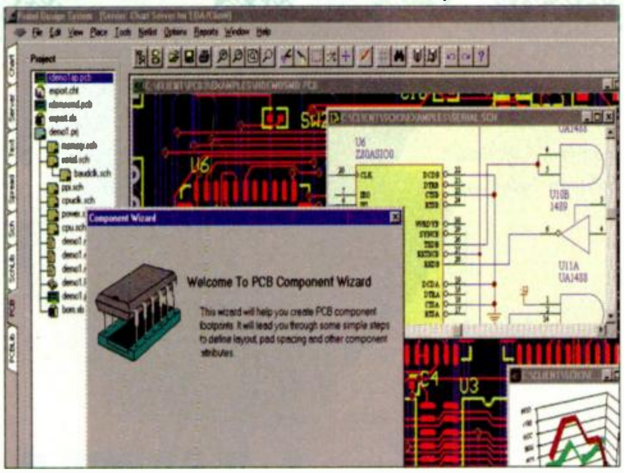
Advanced PCB^3

Printed Circuit Board Design Server for EDA/Client

Constraints and Rule Scripts bring rules-driven PCB layout to the desktop. Features real-time design rule checking, high-speed design capability, 16 Signal layers, 4 power planes and intelligent split planes. Component Wizard automates footprint creation. This top-to-bottom re-engineered PCB design tool is seamlessly integrated with other EDA/Client plug-ins.

EDA/Client PLUG-IN SERVER

$2995



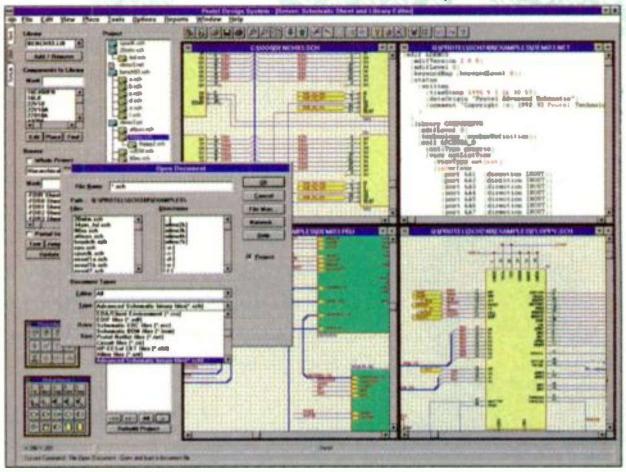
Advanced Schematic^3

Schematic Capture Server for EDA/Client

Advanced Schematic was the first Windows-based schematic capture system to provide engineers with a design tool that supported industry standard OrCAD® design files and libraries. Advanced Schematic 3 carries the designer beyond the boundary of today's EDA desktop. Engineered to "plug-in" to tomorrow's multi-user/multi-tool environment.

EDA/Client PLUG-IN SERVER

$595*



Advanced PLD^3

Programmable Logic Design Server for EDA/Client

Integrated, versatile and powerful development environment for Programmable Logic. Advanced PLD brings a new degree of integration to PLD design. Based on the industry-standard CUPL Hardware Description Language, Advanced PLD includes editing, compiling and simulation tools supported by a comprehensive and expandable collection of device libraries.

EDA/Client PLUG-IN SERVER

$995*

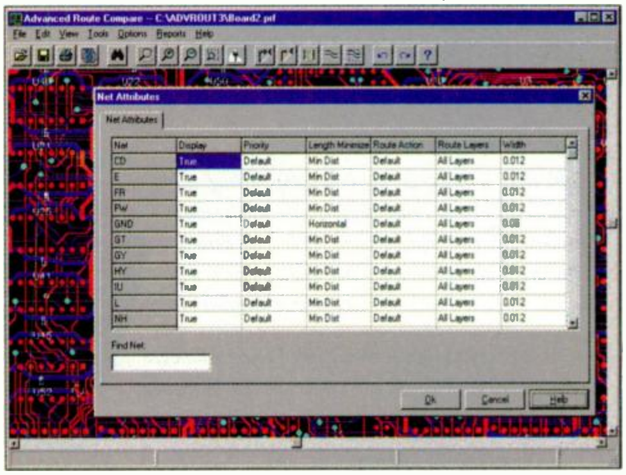
Advanced Route^3

Shape-Based Autorouter Server for EDA/Client

Combines the power of shape-based routing with artificial intelligence to provide the most direct route to board completion. An easy-to-use powerhouse that routes more like an experienced designer than any other current technology. Finally, a shape-based router that any designer can use, at a price that every designer can afford.

EDA/Client PLUG-IN SERVER

$995*



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READER SERVICE 183

JOHN NOVELLINO
TEST & MEASUREMENT

"A thumbnail look at what is happening in the world of distribution."

Changes Are Coming And NEDA Conference Will Discuss Them

"Reinventing distribution: where do we go from here?" is the theme of this year's Executive Conference of the National Electronic Distributors Association. The event, scheduled for Oct. 26-28 at the Renaissance Chicago Hotel, Chicago, Ill., will examine the changes currently facing the distribution industry and what distributors can expect as they approach the next century.

The NEDA Executive Conference is a good way to keep up with the new and different opportunities that present themselves to the industry, according to Skip Streber of Arrow/Schweber Electronics, the conference's planning committee chairman. "Distributors need to understand changes in the current environment and the the changes we anticipate we'll have in the next three to five years, in order to reinvent their companies," said Streber. "Each speaker will talk about one of the critical pieces of the new environment for distributors to contemplate."

Among the speakers is Joseph Pyne, senior vice president of marketing at United Parcel Service (UPS). He will look at the issues that are shaping and redefining distribution channels, with special emphasis on the implications for electronic distributors. The association also expects that Pyne will talk about the repercussions of the recent UPS strike, which cost NEDA members an average weekly loss of almost $125,000, according to a survey the association conducted during the strike.

Other speakers include Tom Fallon, vice president of supply operations at Cisco Systems Inc., and Don Hnatsyshin, corporate vice president of worldwide procurement at Newbridge Networks Corp. They will explore the expanding business opportunities provided to distributors in both the vertical and virtual enterprises.

Web Site Lets Users "Build" A Custom Computer System

Avnet's Computer Marketing Group (CMG) has established a new business unit, Avnet Direct, which will sell business customers name-brand computer products and services over the Internet. Using the group's web site, http://www.avnetdirect.com, customers can specify a computer system based on their unique needs. Once the customized system has been "virtually" built on the site, an order is automatically sent to Avnet CMG's Production Integration Center for physical assembly. More than 20 preconfigured systems also are available for entry-level, mid-range, and high-performance applications.

The site, which operates 24 hours a day, seven days a week, offers users inventory availability, pricing, specifications, features, and benefits for over 40,000 computer products from 130 manufacturers. A product search and specification engine helps customers specify their system. Users can enter processor type and speed, amount of RAM, disk drive size, and other details. The engine then searches for systems that meet the specifications and lists them side-by-side for a price and feature comparison. Custom systems are shipped within 48 hours of order receipt.

"More and more companies will standardize on web commerce in the future," said Richard Lawson, Avnet Direct's general manager. "We intend to be well-placed to not only meet our customers' need for efficiency, but to help make them more educated buyers." The company plans to open additional sites that are customized to specific environments.

Tool Helps Buyers Find ICs Quickly On The Open Market

OEMs looking to buy ICs on the open market can use a new tool that creates customized product information lists from Cafe Silica, a web site that acts as an electronic trading center. The tool, Quick Start, also allows customers to select the delivery method and frequency of the requested product information. Using Cafe Silica, operated by American IC Exchange, Aliso Viejo, Calif., OEMs also can sell their excess supply of ICs.

To create a product information list, OEMs submit their part-number cross-reference lists. On a regular basis, Cafe Silica scans the inventory and generates a "match list." Alternatively, buyers can generate a customized product list themselves by clicking on the Quick Start "setup" icon and selecting the product types, part numbers, or manufacturers that they regularly use. Users can choose Internet, fax, or e-mail notification every day if desired. Cafe Silica will create a list every time the customer accesses the web site at http://www.cafesilica.com.

Buyers can request a quote and place an order on-line or by fax, phone, or e-mail. All products listed on Cafe Silica are in the company's inventory and can ship the same day. If the customer prefers, American IC Exchange will bond inventory according to their schedule.

Time Gets Wakefield's Heatsink Products

Time Electronics is now a primary distributor of Wakefield Engineering Inc.'s line of heatsinks and other thermal management products. Wakefield Engineering, Wakefield, Mass., had previously scaled back its number of distributors by 35% to provide more focus and support to its distribution channel, according to company officials. Carl Swanson, Wakefield's distribution sales manager, said, "Time Electronics' design assistance, value-added services, and excellent product mix will enable customers to easily procure cost-effective thermal management solutions required by the latest generation of electronic products." Time Electronics is a member of Avnet's OEM Marketing Group., Tempe, Ariz. It handles connectors, passive and electromechanical components, and semiconductors and performs value-added services.

Richardson Picks Up MOSFETs For RF Communications Use

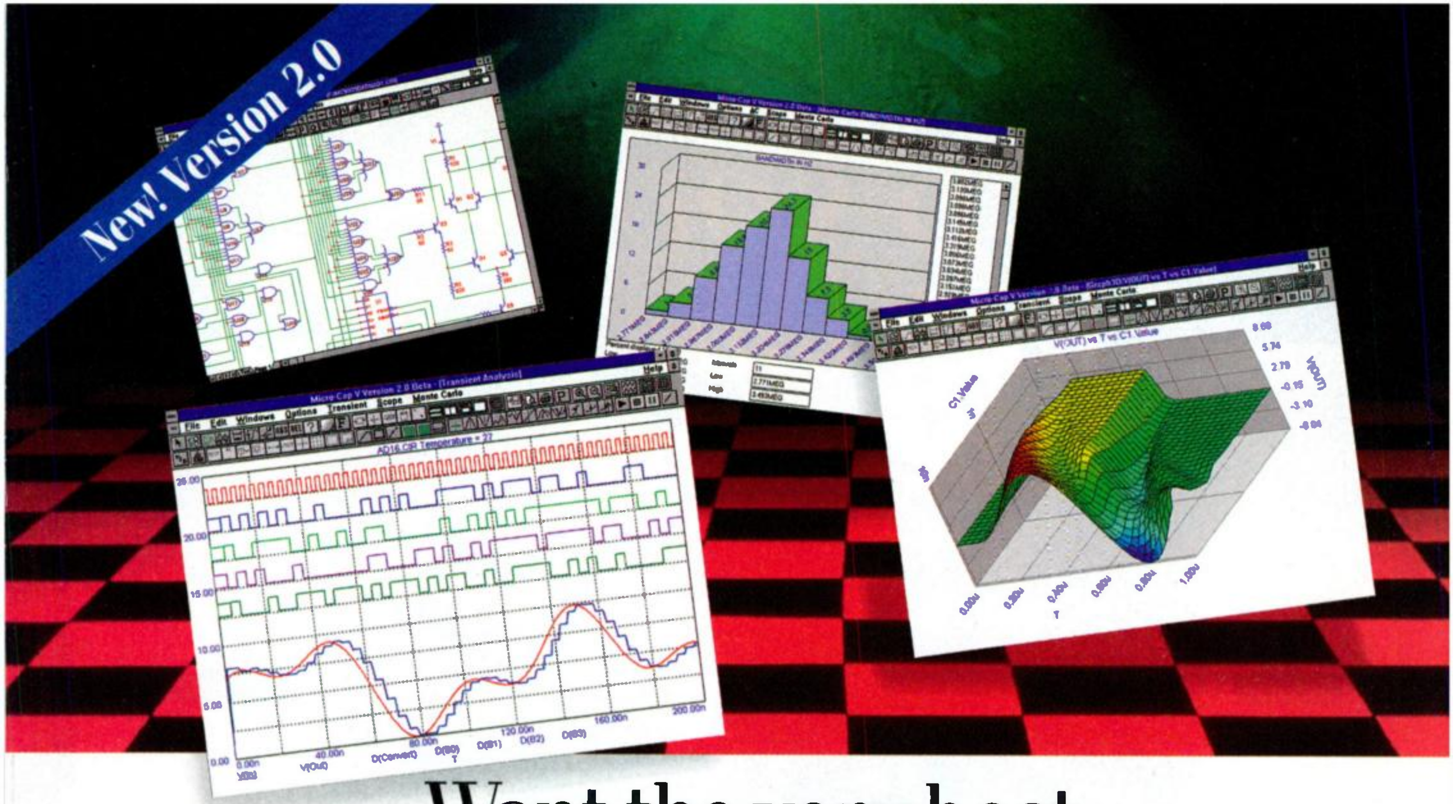
Two new families of transistors designed for surface-mount communication applications in the 100-to-500-MHz range are being distributed by Richardson Electronics Ltd., LaFox, Ill. The WRLS-01xx series includes three class A MOSFETs with 1-dB compression points of 30, 33, and 36 dBm from a 7.5- to 10-V supply. They provide over 12.0 dB of gain from 100 to 200 MHz. The WRLS-04xx series of three class A MOSFETs have 1-dB compression points of 30, 33, and 35.4 dBm from a 7.5- to 10-V supply and deliver more than 10 dB of gain from 400 to 500 MHz. Both series—from RF Products Inc., Sacramento, Calif.—come in high-dissipation, low-inductance ceramic SO-8 surface-mount packages.

Talon's VXI Test Lines Now Handled By Ward Davis

Talon Instruments, a manufacturer of digital test and measurement equipment employing the VXIbus, has signed up Ward Davis Associates as its new California representative. Ward Davis, which has offices in Southern and Northern California, specializes in VXI-based products and offers customers integrated solutions. Talon commented that the distributor's sales team "offers technical knowledge and experience with a young and aggressive outlook."

NEDA Says Top Distributors' Sales Grew 12% In 1996

Annual shipments for distributors jumped 12% in 1996 compared with 1995, to an estimated $24.5 billion, according to data just released by the National Electronic Distributors Association (NEDA). The total is based on actual sales by companies that report information for the NEDA's Distribution Business Index and accounts for sales of the top 200 North American and Canadian electronic distributors. It does not include independent or international distributors and accounts primarily for OEMs. For more details, contact Marilyn Thomas Wieland, NEDA's vice president of industry practices, at (312) 558-9114.



Want the very best in Analog/Digital simulation? Introducing Micro-Cap V Version 2.0

Micro-Cap V is a fast, precision, 32-bit analog/digital simulator with an intuitive fifth generation user interface, and a library of more than 10,000 pre-modeled parts. Based on Spice3 and PSpice™, it offers the best features and capability of both.

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Download the free working demo at www.spectrum-soft.com.

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• Parameter Stepping	Multidimensional
• Optimizing Parts Modeler	Yes
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READER SERVICE 189

Creating Ads To Meet Recruitment Challenges Means Merging The Knowledge Of Engineering And Personnel Heads

Michael Bruce

According to the U.S. Department of Labor, there's good news and bad news for the electronic industries. The good news is that significant, sustained industrial growth will double the number of jobs available up to the year 2005 and beyond. The bad news, however, is that companies will be challenged to find efficient and economical ways to recruit qualified engineering employees to meet that growth. It may be even more difficult in some quarters, as consolidation and trade, patent, regulatory, and market/profit margin issues result in negative images for specific industry segments and major companies.

These challenges may be met by merging the knowledge and talents of engineering managers with department heads who know what skills and traits will be needed. Mix those attributes with the more general knowledge and techniques used by executives in personnel departments and the result is key. The marriage of engineering knowhow and human resources capabilities is vital to successful recruitment.

Fortunately, there are techniques and strategies that can be used to recruit both outstanding and acceptable personnel, even during adverse times characterized by negative publicity. Though validated, these methodologies and their implementations are not well-known. But before examining the techniques, let's contrast recruiters, agencies, and advertising specialists.

Most executive recruitment firms and traditional employment agencies have short-term "make the placement and get the fee" priorities, instead of long term employee adaptability, productivity, and career orientation. The majority of recruitment advertising agencies only give lip service to these matters. They produce unimaginative ads aimed at generating responses from all types of applicants—most of them from unsuitable candidates—instead of replies from a handful of the best candidates.

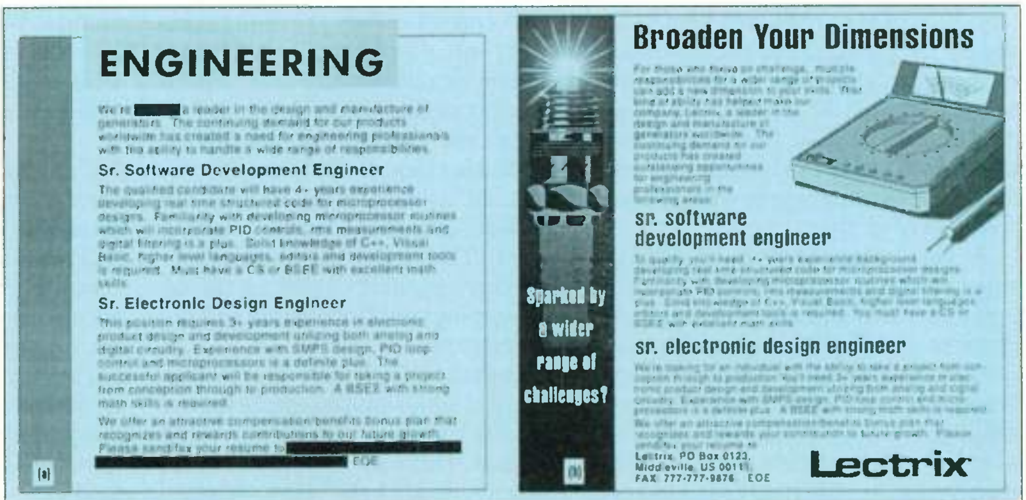
Better Ads = Better Employees

While it's true that classified recruitment ads are generally intended to attract the most responses, they also attract people looking for any kind of job *(Fig. 1a)*. Some of these people stretch their abilities and experience too far and may be unsuited to the actual job and departmental environment. Advertising is the broadest way to reach out to potential applicants, but it can be sharpened to weed out the unqualified, and narrowed to exclude unqualified individuals. And it is far less expensive, since it costs a fraction of executive recruiter and employment agency fees.

Good recruitment advertising makes use of marketing techniques that have been validated in business-to-business and product marketing, as well as corporate-image and financial advertising efforts. The objective is to persuade the right engineering applicant to further his or her career at company X, and to give that candidate an idea of the company's culture, needs, and opportunities *(Fig. 1b)*.

An effective recruitment ad is analogous to a movie preview, both focus on the most exciting and appealing elements of the job or film. Those appeal factors should be inserted into the ad to make the job compelling to the candidate. If research is a key part of the job, make sure to emphasize it in the ad.

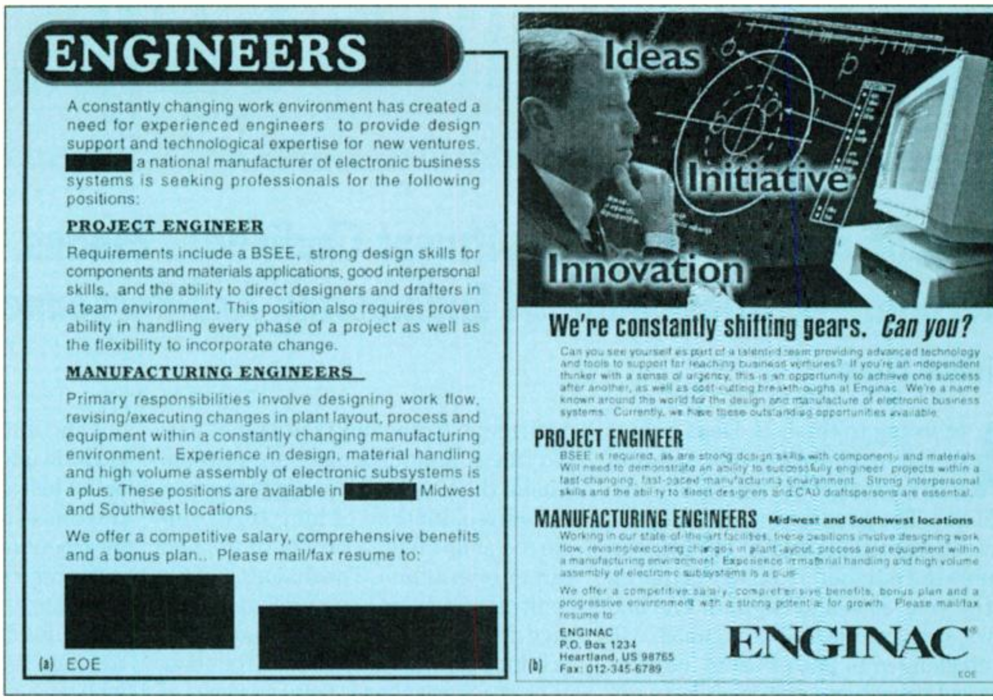
All good recruitment ads contain in-



1. Engineering recruitment ads can be both deadly, as can be seen by the ad on the left, and dynamic, as can be seen by the ad on the right. By talking up the company instead of talking to the candidate, the ad on the left is essentially talking to itself (a). Job candidates first want to know if they fit in, as the phrase in the ad on the right shows (b).

centives to attract the right candidates and disincentives to discourage the wrong candidates. They also have active headlines and integrated artwork so as to be noticed by the qualified potential employee, even if the potential employee is simply browsing through classifieds.

The key is to turn a passive reader into an active applicant. An engineering manager who supervises the context, design, and placement of a recruitment ad through the company's personnel department should be more concerned with overcoming a potential (good) applicant's inertia, rather than merely competing with all the other ads in a newspaper or trade magazine.



2. Instead of having a technically correct recruitment ad as shown in the one on the left (a), the ad should appeal to the candidate's interest, as shown in the one on the right (b). Without a headline to grab the reader's attention, an ad can miss a key opportunity to generate a quality response.

The incentive may be thought of as hot buttons that the ad should press to excite the reader and motivate him or her to respond. What line managers and personnel professionals sometimes lose sight of is that good recruitment advertising is about more than jobs—it's about targeting and appreciating individual talents. Ads should be fine-tuned to give an even better hook that is both noticed and accepted (generated responses). For example, such qualities as "systems expertise" or "applications experience," and the ability to "persuade/influence others on a project team" may be the hot buttons of a "Type A" personality *(Fig. 2a)*. In another case, the comfort factors may lie with production routines and being in a unit where change is infrequent *(Fig. 2b)*.

Studies over a 10-year period indicate that the hire attracted by a highly creative, motivational recruitment ad remains on the job, on average, two-to-three times longer than the hire attracted by executive recruiters and employment agencies. That kind of staying power yields lower costs, higher morale, and greater productivity. These benefits are particularly important to electronic design firms, where the dynamics may be the most challenging, and where the impact of roller-coaster changes in defense spending, for example, threaten the basic job stability of a company, industry subgroup, or particular region.

Here are three ideas that may help ensure that your company's recruitment ads are doing the right job:

Persuade and screen. Effective recruitment ads don't just deliver vast numbers of applicants in response to a job opening. In fact, they're geared to do the opposite. They are designed to attract only a select number of highly qualified candidates. But selecting out means attracting beyond basic skill requirements, not just eliminating unqualified persons. Look upon a recruitment ad as a selling device (to persuade) as well as a hiring device (to screen). The ad also can act as a preview and screening device for the actual employment interview to take place later on.

Find mutual interests. The best recruitment ads should integrate the department's priorities with those of the applicant. This task requires more ingredients than a brief job description and a sketch of the company. Using input from department heads, the ad should explain what makes the position different, or even unique, within the industry, and why only engineers with these specific qualities in their backgrounds would excel at and be interested in this job.

Use hidden motivators. The best candidates are generally considered those who already have jobs. These people need special incentives to give up the known for the unknown. Such incentives strike the right chord with their hot buttons and motivate the candidates to actively seek new opportunities. While positive incentives are obvious, an adverse development or other negative situation also can provide such a stimulus.

For example, a company that has been downsizing will attract candidates who want to do more with less. A demanding department head might very well be welcomed by high achievers and those who prefer high-stress environments. The ad copy places the adversity in a context where it is viewed as a challenge. And there are many candidates who prefer such environments and appreciate the ad's candor.

The whole point of effective recruitment advertising is to get better talent at lower cost. Engineering managers

should borrow a page from their own professional abilities and standards, and help guide and design ads that succeed on both the cost and performance levels. The rewards in attracting the right job candidate are substantial: the new engineer is more productive, generally performs more enthusiastically, and remains and grows with the company or division longer.

Power Of Negative Thinking

Negatives in ads also can be powerful recruitment tools. Many managers mistakenly view negatives (such as spending cutbacks, program cancellations, downsizing, a poor safety or performance record on a high-profile program or product, or merger-mania) as harmful or limiting to the recruitment process. Among electronic firms and high-tech companies in general, there also may be incidents such as allegations of employee discrimination, the aftermath of a hostile takeover, corporate relocation, strict environmental considerations, or some other issue given broad negative play in the media.

Surprisingly, negatives can be utilized in a constructive manner, and if used skillfully, can increase the chances of attracting the best-suited candidates that will become loyal, productive engineers. The exploitation of this contrarian doctrine rests on identifying, articulating, and utilizing the distinctive qualities of a job opportunity and those in the setting where it resides. In turn, these attributes become the inducements and disincentives that respectively attract the right candidates and discourage those that really would not make a successful transition to the new job, or stay the course.

The key is a kind of feedback mechanism, whereby the experienced engineering manager articulates the essentials and priorities to the human resources department. The department head should get involved in the recruitment process, even to the point of reviewing and redesigning ad copy. This individual must make sure that the appeal is in the engineering context, and is specific to the requirements and environment of the position that's available. Here are some examples:

- An authoritative manager or supervisor will be disliked by most applicants, but some candidates actually prefer structure, clear direction, and authority.
- A very demanding department head may be too much for many candidates, but would be welcomed by applicants that are high achievers and/or those that prefer high-pressure environments.
- Conversely, an easy-going executive appeals to those prospective employees that desire elbow room and the chance to display initiative.
- A company facing a downsizing mandate will attract candidates that roll-up their sleeves and who want to do more with less. That vista also lures turn-around specialists.
- A corporation with a diversity challenge will beckon to applicants that seek to reform or correct the problem from within, by persuasion instead of confrontation.
- A business that has suffered a financial reversal can recruit the more innovative "lean and mean" operatives that can cut costs, redesign, or reengineer the project or department infrastructure. An enterprise that has experienced embarrassing product failures is honey to engineering bees and technical specialists determined to fix what is broken.
- Not everyone is happy in a state-of-the-art firm, working independently, or in a highly competitive environment; some people still prefer long-established companies, working under experienced mentors, in firms that emphasize teamwork.

The remark that "for every pot there is a cover" applies to the recruitment context, too. One applicant's negative is another's major attraction; one company's woes are ambrosia to the right job-seeker. A corporation coping with negative conditions can work smartly to attract solid candidates if it uses approaches and techniques that are tailored to such situations. The accompanying figure exhibits successful ads that make use of negatives, and also contain some contrasts to show how an ordinary ad can be reworked.

Guidelines

Here are some guidelines for turning negatives into positives when it comes to recruitment ads:

- Line managers should acknowledge the actual department environment or culture. Prioritize the most attractive or powerful inducements and the least attractive or negative aspects. All of the traits should come from the operational context, not the perceptions of staff people too remote from the situation.
- Don't be apologetic, defensive, or evasive of the negatives. Turn them to your advantage using proven industrial psychology techniques coupled with recruitment strategies.
- Don't rely on customary or "me too" ads. Make them distinctive so they stand out among all the other recruitment ads, and their content and arrangement work in combination to overcome the inertia of potential candidates that are only browsing. Develop the thinking that the ad serves as a form of first interview, and that you are free to state whatever you wish.
- Ads and other messages about the company's products, services, and image get top priority and meticulous attention. Recruitment ads should enjoy similar status to win the competition for qualified or superior candidates. Recruitment ads should blend selling devices with hiring devices.
- Recognize that it is not easier to attract prospective employees during economic downturns or uncertain times, just because the labor pool is larger due to layoffs. The best candidates are those with jobs, not those without work, and the former are generally reluctant to give up the known for the unknown. They need special incentives that strike the right chord with their hot buttons, and motivate them to actively seek new opportunities. Similarly, the incorporation of disincentives will eliminate those would-be candidates looking for any kind of job or who may be stretching their capabilities too far.

Michael Bruce, founder and president of McFrank & Williams Advertising Agency, New York, N.Y., has been creating motivational ads since 1968. He also heads The Center for Staffing Research, a recruitment think tank. He may be contacted at (800) 599-1919.

New FLUIDTOOLS with elbows and valves solves pipe and tube flow problems on your PC

Wouldn't it be nice if you could solve flow problems without having to look up all of your data? With FLUIDTOOLS, you can do just that? It's easy as A-B-C.

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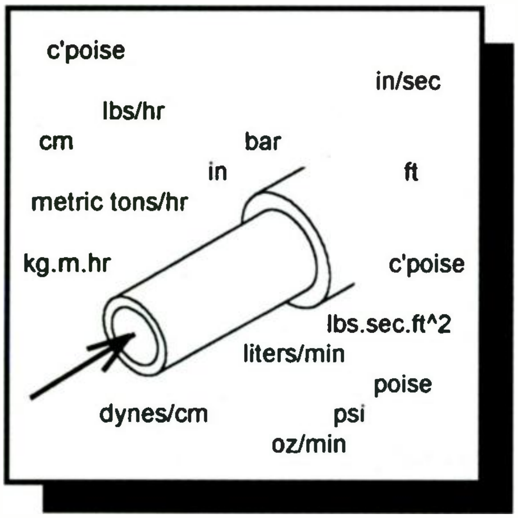
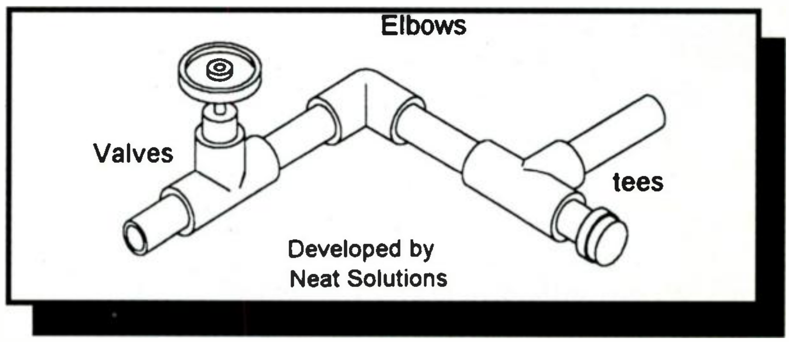
- **Press "calculate" . . .**

It's that simple!

Program accepts mixed units



FLUIDTOOLS solves liquid and gas flow problems including escaping gas problems. It can solve for diameter, length, flow rate, pressure, or viscosity when doing liquids. Gas problems solve for quantity and DPSI.



Some of the important Features of FLUIDTOOLS . . .

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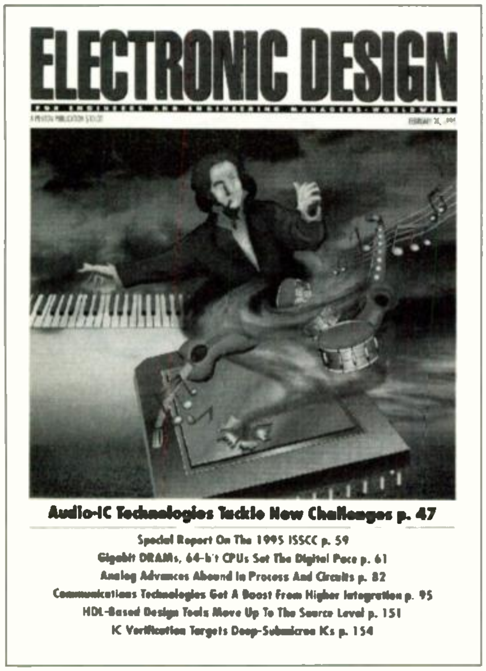

A third strategic partner completes this alliance. This partner's mission is to observe and report today's product availability by its editorial staff of respected experts, while constantly probing for the next generation of enabling technology. The constant flow of exclusive and vital information helps to bring systems designers and suppliers together as strategic partners. It also provides engineers and engineering managers with an enhanced ability to bring more competitive products to market, faster.

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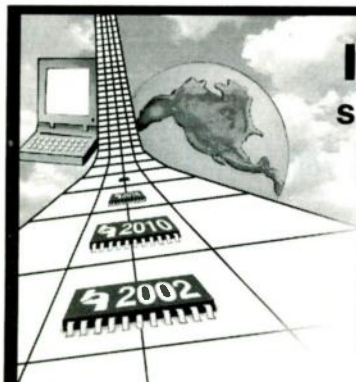

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Qualified candidate will be responsible for 50% design (full custom CMOS logic and circuit) and 50% verification (generating and maintaining test suite in Assembly language). Must have a minimum of a MSEE with 2+ years experience or a BSEE with 4+ years of experience. Background in computer architecture and CMOS circuit design using SPICE is required. Must also have working experience with VERILOG (preferred) or VHDL. **Job Code: BLED-971**

Product Engineer

Qualified candidate must have 5+ years experience and familiarity with CMOS processing techniques and testing methodology. Must also have hands-on experience in silicon debug to include micro-probing, wafer deprocessing, understanding of schematics and datasheet parameters and characterization of devices across all datasheet parameters and end-use systems. Experience with design of hardware and software of small microcontroller-based systems is required. CMOS mixed signal or digital experience preferred. Background working on microcontroller-based devices with analog I/O a plus. **Job Code: ESED-972**

Applications Engineer

Selected candidate will be responsible for providing technical marketing support for the development and implementation of customer applications dealing with complex operating systems. Will assist sales staff in assessing potential application of company products to meet customer needs and prepare detailed product specifications. A BSEE, minimum of 7 years experience and background with power conversion and low-power analog circuits required. **Job Code: DFED-10972**

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Successful candidate will be responsible for the analysis, design, programming, debugging and modification of software and will troubleshoot code for firmware (IC embedded code) applications. Work often involves analog and digital hardware and software operating systems. Must have a minimum of 5 years experience, knowledge of hardware design, as well as the ability to program in machine, assembly and high-level languages, such as C and C++. Experience programming portable electronic applications and battery-powered microcontrollers is preferred. **Job Code: DFED-10971**

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INDEX OF ADVERTISERS

Domestic*
International **

ANALOG DEVICES

Industrial Control ICs

Affordable Signal Processing Solutions for Measurement and Control Applications

CONTENTS

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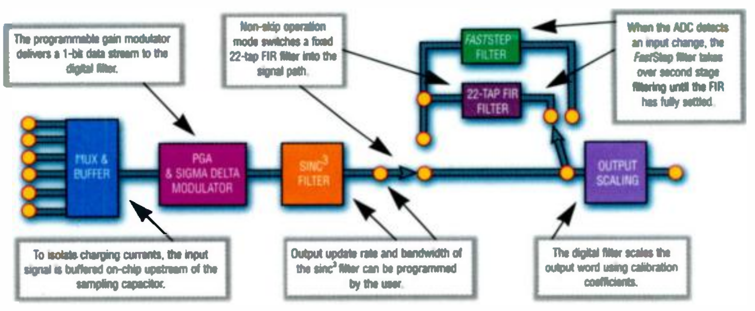
http://www.analog.com

AD7731



New High Speed and Low Noise in a 24-Bit, No-Missing-Codes ΣΔ ADC

The AD7731 is a complete analog front-end for process control operations. This ADC's sigma-delta architecture consists of an analog modulator and a low-pass programmable digital filter, allowing adjustment of filter cutoff, output rate and settling time. Featuring a proprietary programmable front end (allowing for a range of seven unipolar and bipolar input signals from ±20 mV to ±1.28 V), the AD7731 can deliver noise-free, 16 bits of peak resolution at 800 Hz. It can also be tailored for even higher speeds and resolutions – anywhere from 11 bits at 6400 Hz (±20 mV) to 19 bits (guaranteed) at 50 Hz (±1.28 V).

The AD7731 can switch between channels with a 1 ms settling time and still maintain noise-free 13-bit performance with input signals from ±40 mV up to ±1.28 V. This extremely flexible part also contains self-calibration and system-calibration options, and features an offset drift of less than 5 ppm/°C and a gain drift of less than 2 ppm/°C. And does it all from a single +5 V supply.

All functions on the AD7731 can be accessed via the 3-wire serial interface, making the part compatible with microcontrollers and digital signal processors. Two of the six analog input pins can be software configured as digital outputs. It comes in 24-lead DIP, and 24-lead SOIC and TSSOP packages.

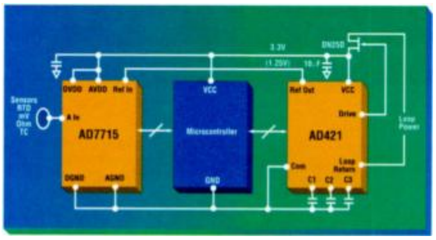
KEY FEATURES
- Noise-free, 16-bit words at 800 Hz
- PGA with seven unipolar or bipolar input signals
- 1 ms settling time between switched channels

AD7731 **Price $9.86** **Faxcode 2131** **Circle 01**

All prices shown in USD, 1,000s, recommended resale, FOB U.S.A.

Complete Smart Transmitter Solutions Available with Intelligent Converters

The AD421 is a HART®-compatible, high-precision DAC that converts digital data to current (4 mA to 20 mA) with 16-bit resolution and monotonicity. It provides either +5 V, +3.3 V or +3 V regulated output that can power all other devices in your transmitter. The AD421 is available in a 16-lead, 0.3" wide plastic DIP and SOIC package.



The AD7714 and AD7715 are charge balancing ADCs with programmable gain front ends, 0.0015% nonlinearity, and low-pass filters with programmable filter cutoffs. Both devices operate from a single +3 V or +5 V supply. The AD7714 (24 bits, no missing codes) consumes less than 3 mW typically at +3 V and 5 mW at +5 V, and comes in 24-lead DIP and SOIC packages, and 28-lead SSOP. The AD7715 (16 bits, no missing codes) has similar power consumption and is available in a 16-lead DIP or 16-lead SOIC.

KEY FEATURES
- 3-wire serial interface
- Fast, accurate 24- or 16-bit resolution
- Low power consumption

AD421	Price $6.75	Faxcode 1892	Circle 02
AD7714	Price $9.89	Faxcode 1812	Circle 03
AD7715	Price $5.99	Faxcode 1813	Circle 04

8-Bit and 10-Bit ADCs: Micro Packages at Micro Prices

This family of two 8-bit and four 10-bit ADCs will operate from +2.7 V to +5.5 V and consume only 1.5 mW @ 100 kSPS (typical). The ability to automatically power-down after conversions makes these devices the ADC of choice in applications where power consumption is critical. They also come in a variety of packages, including the space-saving 8-lead microSOIC package, which saves board space by over 50%.

The 8-bit, single channel models (AD7819/23) are specified with a 4.5 ms conversion time, and the 10-bit ADCs carry a maximum 400 kSPS throughput rating, with the AD7810/3 designated as single channel, the AD7811 as a 4-channel, and the AD7812 as an 8-channel.

KEY FEATURES
- Very low power consumption
- Small 8-lead microSOIC package
- Operates -40°C up to +125°C

AD7810	Price $2.45	Faxcode 2061	Circle 05
AD7811	Price $2.90	Faxcode 2062	Circle 06
AD7812	Price $3.30	Faxcode 2062	Circle 07
AD7813	Price $2.55	Faxcode 2063	Circle 08
AD7819	Price $1.95	Faxcode 2064	Circle 09
AD7823	Price $1.95	Faxcode 2065	Circle 10

KEY PARAMETERS

	Units	AD7819	AD7823	AD7810	AD7811	AD7812	AD7813
Resolution	bits	8	8	10	10	10	10
Number of Input Channels		1	1	1	4	8	1
Interface		Parallel	Serial	Serial	Serial	Serial	Parallel
Power Supply	V	+2.7 to +5.5	+2.7 to +5.5	+2.7 to +5.5	+2.7 to +5.5	+2.7 to +5.5	+2.7 to +5.5
Throughput	kSPS	200	135	350	350	350	400
Accuracy	LSB	±0.5	±0.5	±1.0	±1.0	±1.0	±1.0
Can Use V_{DD} As Reference		Yes	Yes	Yes	Yes	Yes	Yes
Power-Down		Yes	Yes	Yes	Yes	Yes	Yes
Power (max throughput)	mW	10.5	10.5	10.5	10.5	10.5	10.5
Power @ 100 kSPS	mW			2.7	2.7	2.7	3.46
Power @ 50 kSPS	mW	2.89	2.7				
Power @ 10 kSPS	µW	577	540	270	270	270	346
Power @ 1 kSPS	µW	57.75	54	27	27	27	34.6
Analog Input Range		0V to V_{DD}	0V to V_{DD}	0V to V_{DD}	0V to V_{DD}	0V to V_{DD}	0V to V_{DD}
Pin Count		16	8	8	16	20	16
Package		DIP, SOIC, TSSOP	DIP, SOIC, µSOIC	DIP, SOIC, µSOIC	DIP, SOIC, TSSOP	DIP, SOIC, TSSOP	DIP, SOIC, TSSOP
Temperature Range	°C	-40 to +125	-40 to +125	-40 to +105	-40 to +105	-40 to +105	-40 to +105

ANALOG DEVICES FOR DATA SHEET FAXBACK 1-800-446-6212

New High Speed, Low Power ADCs for General-Purpose Applications

The AD976A and AD977A are 16-bit, 200 kSPS, low-power ADCs that operate from a single +5 V supply. Each converter contains a successive approximation, switched capacitor ADC, internal +2.5 V reference and a high speed interface. The ADCs are factory-calibrated to minimize all linearity errors, and power dissipation is just 100 mW for this 200 kSPS sampling rate.

	AD976A	AD977A
Interface	Parallel	Serial
A_{IN} Ranges (V)	±10	±10, ±5, ±3.3, 0-10, 0-5, 0-4
Packages	28-lead DIP, SOIC, SSOP	20-lead DIP, SOIC, 28-lead

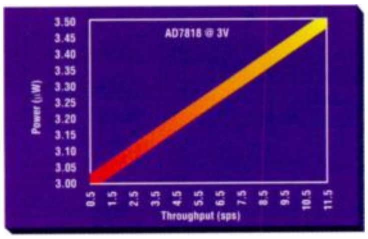
Both components are fabricated on Analog Devices' BiCMOS process and include high-performance bipolar devices in addition to CMOS transistors. Designed for use in general-purpose applications such as gas analyzers, scanners, memory testers, communications and biomedical instrumentation, the AD976A and AD977A offer complete, single-chip, highly integrated A/D solutions.

KEY FEATURES
- 16-bit BiCMOS ADC with 200 kSPS throughput rate
- Low 100 mW power dissipation
- Power-down mode with AD977A

AD976A	Price $26.00	Faxcode 1953	Circle 11
AD977A	Price $20.00	Faxcode 1958	Circle 12

New ADC with On-Chip Temperature Sensor Consumes Less Than 3.5 µW

The AD7817, a 4-channel 10-bit A/D converter and the AD7818, a single-channel 10-bit A/D converter, have on-chip temperature sensors with a temperature accuracy of 1°C (max) at 25°C and 2°C (max) between -40°C to +85°C. Both devices contain a 10 µs successive-approximation converter, an on-chip clock oscillator, inherent track-and-hold functionality, and an on-chip reference (+2.5 V ±1%). Taking 10 temperature readings every second, the part consumes less than 3.5 µW. The on-chip sensors of the AD7817 and AD7818 can be accessed via channel 0. The AD7816 is a temperature-monitoring-only device.



The AD7816 and AD7818 are available in an 8-lead SOIC and microSOIC, and the AD7817 is available in a 16-lead SOIC and TSSOP. Operating in a wide supply range (+2.7 V to +5.5 V), and the ability to power-down between conversions, mean power consumption is reduced to a minimum.

KEY FEATURES
- Automatic power-down
- 10-bit ADC with 10 µs conversion time
- AD7816 & AD7818 available in 8-lead microSOIC

AD7816	Price $1.30	Faxcode 2091	Circle 13
AD7817	Price $3.50	Faxcode 2091	Circle 14
AD7818	Price $2.80	Faxcode 2091	Circle 15

New World's First 14-Bit ADC in an 8-Lead SOIC

The AD7894 (14-bit) and AD7895 (12-bit) are pin-compatible, 2-wire serial interface ADCs that can handle serial input ranges up to ±10 V, and will operate from single +5 V supply in the tiny 8-lead SOIC. Both feature low power consumption (20 mW at full speed) and an automatic power-down mode whereby power consumption can be dramatically reduced at lower speeds. The AD7895 features a fast 3.8 µs 12-bit ADC with a 500 ns track/hold amplifier, while the 14-bit AD7894 has a throughput rate of 165 kSPS.

The AD7894 and AD7895 need only reference inputs and decoupling capacitors for complete data acquisition systems. With their combination of low power consumption, fast conversion rates and tiny 8-lead SOIC packages, the AD7894/5 line is perfect for a wide range of industrial and instrumentation applications, as well as battery powered or portable applications.

KEY FEATURES
- 14-bit ADC handles ±10 V input
- Single +5 V supply
- World's first 14-bit ADC in 8-lead SOIC

AD7894	Price $8.90	Faxcode 2157	Circle 16
AD7895	Price $4.95	Faxcode 1985	Circle 17

New Family of 12- and 14-Bit ADCs Features Simultaneous Sampling & Conversion

Analog Devices' AD7862/3/4 family of ADCs offers high speeds (throughput rates up to 250 kSPS), high resolution (12 and 14 bits), multiple channels (two and four), a wide input range (±10 V), and single +5 V supply. The AD7863 is the 14-lead upgrade to the popular 12-bit AD7862 (making it pin-compatible in its space-saving 28-lead SSOP).

The dual (AD7862/3) and quad (AD7864) channels make this family an excellent choice for the demanding world of motor control applications, which require the simultaneous capture of currents from at least two phases of three-phase motors in order to minimize phase shifts during measurement and control of the channels. The 14-bit dual channels of the AD7863 also make it ideal for I/O processing of QPSK and QAM as well as composite digitizing for multiple video sources.

KEY FEATURES
- Throughput rates up to 250 kSPS
- Simultaneous conversion of two or four channels
- Accept bipolar signals up to ±10 V

AD7862	Price $11.00	Faxcode 2081	Circle 18
AD7863	Price $16.85	Faxcode 2086	Circle 19
AD7864	Price $14.75	Faxcode 2087	Circle 20

Digital-to-Analog Converters

New Industry's First High-Voltage, Single and Dual Supply 128-Position Digital Potentiometers

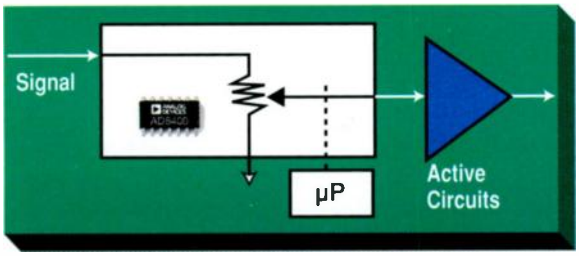
The AD7376 is a potentiometer replacement that provides a single channel, 128-position digitally-controlled variable resistor device with available terminal resistances of 10 kΩ, 50 kΩ, 100 kΩ and 1 MΩ. It will operate from a wide range of single (+5 V to +30 V) and dual (±5 V to ±15 V) supplies. The AD7376 has been optimized for instrument and test equipment applications, providing high voltage with resistance-value choices between bandwidth or power dissipation.

KEY FEATURES
- 128-position potentiometer replacement
- Power shut-down less than 1 µA
- 3-wire SPI compatible serial data input

AD7376	Price $2.57	Faxcode 2111	Circle 21

Single Channel RDAC Provides Solid-State Control

Complementing our dual- (AD8402) and quad- (AD8403) channel 8-bit RDACs (Resistor Digital-to-Analog Converters) is the AD8400 single channel converter available in 1 kΩ, 10 kΩ, 50 kΩ and 100 kΩ values.



This "digitally controlled resistor" comes in an 8-lead PDIP or SO package and can be used as a replacement for mechanical potentiometers and variable resistors, or as an adjustment in new designs for programmable filters, delays, volume controls, DC gain/offsets and line impedance matching. The AD8400 contains a 256-position, digitally-controlled variable resistor that operates from +2.7 V to +5.5 V in single-supply systems with rail-to-rail signal range.

KEY FEATURES
- Single-channel, 8-bit RDAC
- Available in 1 kΩ, 10 kΩ, 50 kΩ and 100 kΩ
- Small PDIP-8 and SO-8 packages

AD8400	Price $1.12	Faxcode 1867	Circle 22

Quad 14-Bit DAC Family Expands with Added Features

The AD7836 is the third in the growing family of quad 14-bit DACs from ADI, all of which offer double buffered inputs, power-on reset and the ability to clear all DACs to a user-defined voltage. In addition to providing ±10 V outputs from reference voltages of ±5 V, the AD7836 accommodates separate buffered reference inputs for each DAC and has the ability to insert an offset voltage on each DAC output. This DAC also has a fifth DAC register to allow loading of a user-defined code to all four DACs without affecting the contents of the other DAC registers.

Part	Interface	No. of Ref. Inputs	Output Voltage Range	Package
AD7834	Serial	1 x V_{REF} ± input	±8.192	28-lead SOIC
AD7835	Par./byte	2 x V_{REF} ± inputs	±8.192	44-lead PQFP
AD7836	Parallel	4 x V_{REF} ± inputs	±10	44-lead PQFP

KEY FEATURES

- Quad DAC with separate buffered reference inputs
- Serial or parallel interface
- New ±10 V output voltage range

AD7834	Price $21.25	Faxcode 1859	Circle 23
AD7835	Price $22.35	Faxcode 1859	Circle 24
AD7836	Price $22.35	Faxcode 2030	Circle 25

Op Amps

SINGLE-SUPPLY AMPLIFIER SELECTION GUIDE

Part Number				Temp Range	Supply Voltage			Rail-to-Rail		Vos (µV)	e noise (nV/√Hz)	I_{SY} (mA)	I_{BIAS} (nA)	GBP (MHz)	Key Features
	1X	2X	4X		3 V	5 V	±15 V	In	Out						
OP	113	213	413	I		●	●			125	4.7	1.75	650	3.5	Low noise, low drift
OP		279*		I		●		●	●	4000	22	3.5	300	5	80 mA output current
OP	181	281	481	I	●	●			●	1.5	70	0.004	10	0.1	4 µA Rail-to-Rail
OP	183	283		I	●	●	●			100	10	1.5	600	5	5 MHz from +3 V to +36 V
OP	184	284	484†	H	●	●	●	●	●	65	3.9	1.25	300	3.25	Like OP27, single supply
OP	162	262	462	H	●	●	●	●	●	325	9.5	0.65	600	15	15 MHz Rail-to-Rail
OP	191	291	491*†	H	●	●		●	●	300	35	0.4	50	3	Low power R-R in/out
OP	193	293	493	H	2 V	●	●			75	65	0.015	15	0.035	Precision, long battery life
OP	196	296*	496†	H	●	●		●	●	300	26	0.05	10	0.35	Micropower R-R in/out
OP		295	495	H	●	●	●		●	300	51	0.15	20	0.075	Accuracy and output drive
AD	820	822	824†	I	●	●	●		●	400	16	0.8	0.012	1.8	JFET input, low power
AD	823			I	●	●	●		●						JFET input, 16 MHz
AD	8531	8532	8534	H	●	●		●	●	25 mV	45	0.7	<10 pA	3	250 mA R-R in/out
SSM		2135		I		●	●			2000	5.2	3.5	750	3.5	Excellent for audio
											tp (ns)	I total (mA)			
CMP			401*†	H	●	●			●	3000	17	7.7			Highest speed 3 V comparator
CMP			402†	H	●	●			●	3000	54	2.4			Lower power CMP401
AD	8041	8042		I	●	●	●		●	7000	15	5.5	3200	160	High speed video
AD			8044†	I	●	●	●		●	6000	16	3.25	4500	150	High speed, low power
AD	8031	8032		I	2.7 V	●		●	●	1500	15	0.8	1000	80	High speed, low power

Temperature Ranges I: -40°C to +85°C, H: -40°C to +125°C

Packages † Available in narrow SO packages; *TSSOP will be available

Specifications given at V_S = +5 V

In Amps

Low-Cost Instrumentation Amplifier Breaks "Make vs. Buy" Decision

The AD623 is a unity-gain stable instrumentation amplifier with an output stage that can swing rail-to-rail, and an input stage that can swing 150 mV below ground. No gain setting resistor is needed for unity gain and only 1 gain setting resistor is required for gains from 2 to 1000. The AD623 is ideal for low-power battery operated systems operating on a wide range of power supply voltages from +3 V to ±5 V at less than 0.5 mA quiescent current. The performance of the AD623 is superior to discrete op amp designs, improving on CMRR (93 dB @ gain = 10), linearity (10 ppm) and offset temperature stability (1 µV/°C), while reducing board space and component costs.

The AD623 is available in both DIP and surface mount packages and is specified for operation from -40°C to +125°C.

KEY FEATURES
- Rail-to-rail output
- Low-power wide-supply range
- Replaces discrete solutions, improved performance

AD623	Price $1.60	Faxcode 2138	Circle 26

Temperature Sensors

New Accurate Temperature Measurement (± 0.1°C) and Low Power Consumption

The ADT70 and ADT71 provide excitation and signal conditioning for resistance-temperature device and will, with high performance platinum elements, measure a 1000°C range (range or gain can be set using only one external resistor). This is an extremely accurate part that will, as part of a PRTD system, introduce an error of only ±0.1°C, which can be reduced to zero at a single calibration point.

Both products operate from either +5 V or ±5 V supplies, and contain a shutdown function for battery powered equipment that reduces the quiescent current from 3 mA to less than 10 µA. Each also features a precision rail-to-rail output instrumentation amplifier. Both ADT70 and ADT71 are available in 20-lead DIP and SO packages.

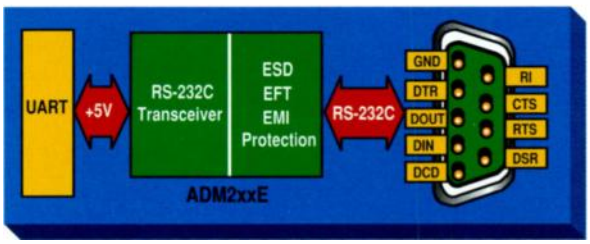
KEY FEATURES
- PRTD temperature measurement range
- Includes two matched current sources
- Rail-to-rail output instrumentation amplifier

ADT70	Price $4.24	Faxcode 2123	Circle 27
ADT71	Price $4.00	Faxcode 2123	Circle 28

Interfaces

RS-232C/V.28, RS-422 and RS-485 Line Drivers and Transceivers

Designers who need to meet demanding EMI/EMC and EIA standards in applications as diverse as PDAs, laptop computers, modems, packet switching, LANs, and EMI-sensitive applications will find their parts solution among these lines of robust line drivers, receivers and transceivers. ESD immunity for the ADM2xxE series (supporting up to 460 kbits/s data rate) and ADM483E/5E (250 kbits/s) is ±15 kV. All operate from a single +5 V supply.



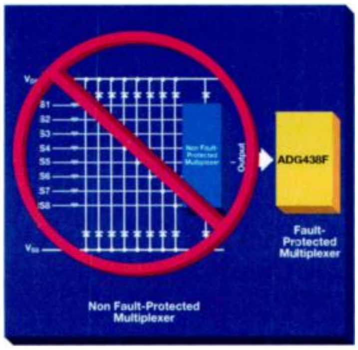
KEY FEATURES
- EMI/EMC compliant
- Single +5V supply
- ±15kV ESD protected

ADM202E	Price $1.40	Faxcode 1992	Circle 29
ADM207E	Price $2.20	Faxcode 1991	Circle 30
ADM208E	Price $2.20	Faxcode 1991	Circle 31
ADM211E	Price $2.20	Faxcode 1991	Circle 32
ADM213E	Price $2.20	Faxcode 1991	Circle 33
ADM483E	Price $1.20	Faxcode 2094	Circle 34
ADM485E	Price $1.65	Faxcode 2254	Circle 35

ANALOG DEVICES FOR DATA SHEET FAXBACK 1-800-446-6212

High Performance Fault Protected Multiplexers

The ADG438F and ADG439F are high performance multiplexers protected against overvoltages of -40 V to +50 V. They also protect in downstream devices because the output is clamped below the power rail. If the power rail is cut due to momentary power loss, the output will be clamped at zero. Only the channel on which the overvoltage occurs is clamped, all other channels remain unaffected. With an ON resistance of 400 Ω, ON resistance match of 3 Ω max, and Δ ON resistance of 5 Ω max over the extended industrial temperature range of -40°C to +105°C, the performance of the ADG438F and ADG439F outperforms other multiplexers currently on the market.



These multiplexers are available in 16-lead DIP and both wide- and narrow-body SOIC packages.

Parameter	ADG438F	ADG439F
Delta R_{on}	3 Ω max	3 Ω max
ON Leakage	±30 nA max	±15 nA max
t_{on}	300 ns max	300 ns max
I_{dd}	0.25 mA max	0.25 mA max

KEY FEATURES
- Overvoltage and fault protection (-40 V to +50 V)
- Extended industrial temperature range (-40°C to +105°C)
- Narrow-body SOIC package available

ADG438F Price $3.64 Faxcode 1855 Circle 36
ADG439F Price $3.64 Faxcode 1855 Circle 37

References

Model	Reference Type	Output Voltage	Maximum Error †	Maximum Tempco ppm/°C †	Quiescent Current (μA)	Max Output Current (mA)	Noise Voltage 0.1 – 10 Hz (μV p-p)	Packages Available	Price ($)	Faxcode
NEW										
ADR290	Series	2.048	±2 mV	8	12	5	6	SO, TSSOP, TO-92	1.95	2110
* ADR291	Series	2.500	±2 mV	8	12	5	8	SO, TSSOP, TO-92	1.95	2110
ADR292	Series	4.096	±3 mV	8	15	5	12	SO, TSSOP, TO-92	1.95	2110
ADR293	Series	5.000	±3 mV	8	15	5	15	SO, TSSOP, TO-92	1.95	2255
AD1580	Shunt	1.225	±1 mV	50	50	10	50	SOT-23	0.75	1963
AD1581	Series	1.225	±0.1 %	50	65	5	50	SOT-23	0.75	2124
* AD1582	Series	2.500	±0.1 %	50	65	5	70	SOT-23	0.75	2125
AD1583	Series	3.000	±0.1 %	50	65	5	85	SOT-23	0.75	2125
AD1584	Series	4.096	±0.1 %	50	65	5	110	SOT-23	0.75	2125
AD1585	Series	5.000	±0.1 %	50	65	5	140	SOT-23	0.75	2125

† Best electrical grade

* Sample kit will include only these parts

Circle 38

Motor Controls

New

Entire Motor Control Signal Chain on a Chip

The ADMC300 provides an entire motor control signal chain on a chip. Based on our 33 MHz ADSP-2171 digital signal processor, this chip has been optimized for servo motor control and features a complete suite of peripherals including a 12-bit PWM generator, an encoder interface unit and an event timer. It includes two extra 8-bit PWM timers, and can be expanded through two serial ports and a 12-bit digital I/O port. The only components required for operation are a microprocessor crystal, an 8-pin serial ROM and six capacitors.

KEY FEATURES
- 25 MHz fixed-point DSP
- Three-phase 12-bit PWM generator
- Two 8-bit PWM auxiliary timers

ADMC300 Price $9.50* Faxcode 2253 Circle 39

Quantities of 100,000

New

World's First Dual-Axis Monolithic Accelerometer

The ADXL250 is the first fully integrated dual-axis ±50 g accelerometer available commercially with signal conditioning on a single monolithic IC. The ADXL150, a single-axis version, also includes on-board signal conditioning. Compared to existing solutions, both devices provide greater sensitivity, reduced drift, lower noise and smaller packaging. The ADXL150/250 are available in hermetic, 14-lead, surface-mount CERPAK packages.

The ADXL150/250 are ideally suited for vibration monitoring required to spot mechanical problems, trigger preventive maintenance and diagnose the health of rotating and oscillatory machinery.

KEY FEATURES
- Fully integrated dual-axis ±50 g accelerometer w/signal conditioning
- -40°C to +85°C industrial operating range
- Power consumption 1.8 mA per axis

ADXL150	Price $12.45*	Faxcode 2060	Circle 40
ADXL250	Price $19.95*	Faxcode 2060	Circle 41

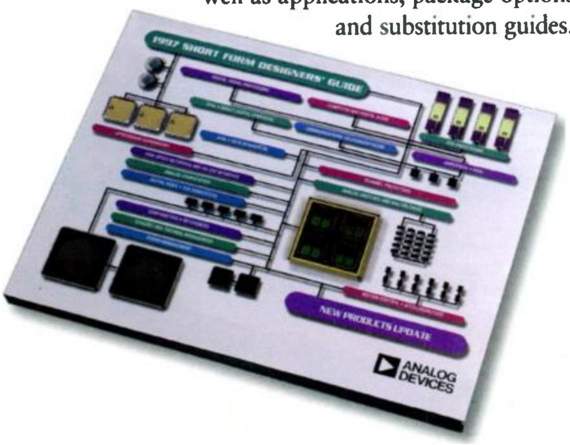
**Quantities of 100*

New

Short Form Catalog and CD-ROM

If you can't get to the Web or a fax machine, you can still get information on our other products.

Our 1997 Short Form Designer's Guide is organized to allow easy reference to hundreds of A/D and D/A converters, amplifiers, comparators, converters, DSPs, switches, multiplexers, voltage references, motion controllers and other components. This publication features selection trees, part specs, pin and block diagrams, as well as applications, package options and substitution guides.



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