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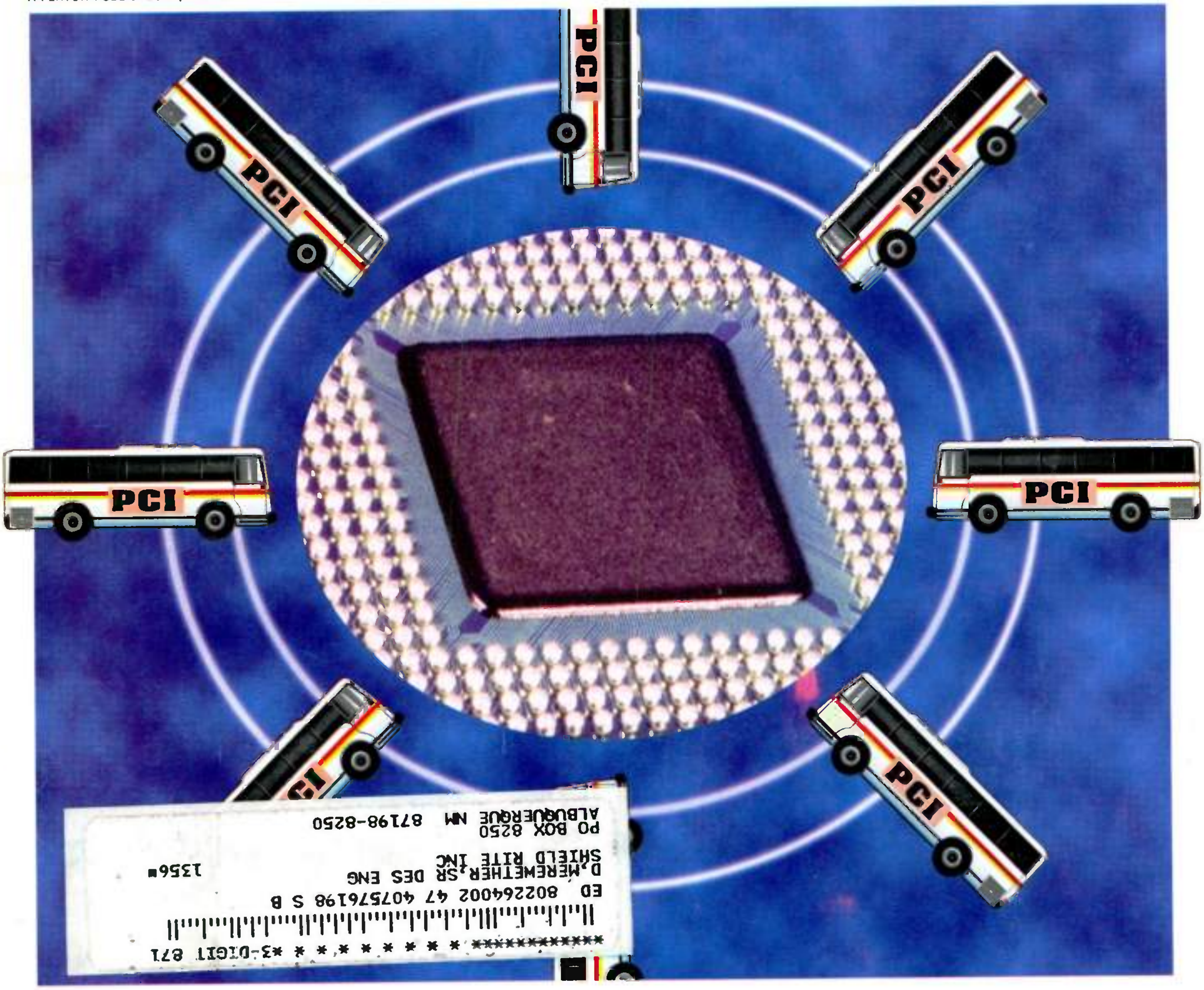

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November 3, 1997 Volume 45, Number 24

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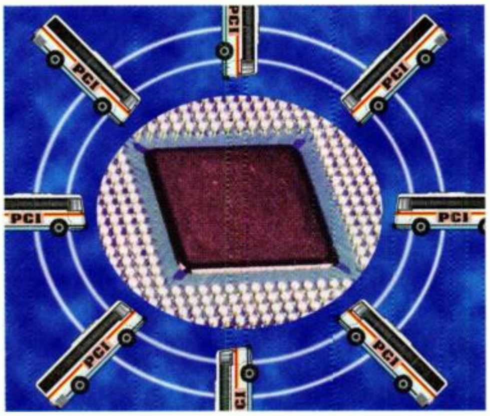

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November 3, 1997 Volume 45, Number 24

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Editor-in-Chief: **TOM HALLIGAN** (201) 393-6228 thalligan@penton.com
Executive Editor: **ROGER ALLAN** (201) 393-6057 rallan@class.org
Managing Editor: **BOB MILNE** (201) 393-6058 bmilne@class.org

Technology Editors:

Analog & Power: **FRANK GOODENOUGH** (617) 227-4388 75410.2361@compuserve.com
Communications: **LEE GOLDBERG** (201) 393-6232 leeg@class.org
Power, Packaging, Components & Optoelectronics: **PATRICK MANNION** (201) 393-6097 pcmann@ibm.net
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Digital ICs: **DAVE BURSKY** (San Jose) (408) 441-0550, ext. 105; dbursky@class.org
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New Products: **ROGER ENGELKE JR.** (201) 393-6276 rogere@csnet.net
Contributing Products Editor: **MILT LEONARD**

Editorial Headquarters:

(201) 393-6060 Fax: (201) 393-0204 E-mail: edesign@class.org
P.O. Box 821, Hasbrouck Heights, N.J. 07604

Field Correspondents:

West Coast Executive Editor:
DAVE BURSKY (San Jose) (408) 441-0550, ext. 105; dbursky@class.org
Western Regional Editors:
CHERYL J. AJLUNI (San Jose) (408) 441-0550, ext. 102; cjajluni@class.org
TOM WILLIAMS (Scotts Valley) (408) 335-1509 tomwillm@ix.netcom.com
2025 Gateway Place, Suite 354, San Jose, CA 95110
(408) 441-0550 Fax: (408) 441-6052

London: **PETER FLETCHER**
16 Malyons Road, Hextable, Kent, BR8 7RE UK
44 1 322 664 355 Fax: 44 1 322 669 829 E-mail: panflet@cix.compulink.co.uk

Munich: **ALFRED B. VOLLMER**
Eichenstr. 6, 82024 Taufkirchen (near Munich) Germany
49 89 614-8377 Fax: 49 89 614-8278 E-mail: Alfred_Vollmer@compuserve.com

Chief Copy Editor: **MICHAEL SCIANNAMEA** (201) 393-6024 mikemea@class.org
Copy Editor: **DEBRA SCHIFF** (201) 393-6221 debras@csnet.net
Ideas For Design Consulting Editor: **JIM BOYD** xl_research@compuserve.com
Contributing Editors: **RON KMETOVICZ, ROBERT A. PEASE, WALT JUNG**
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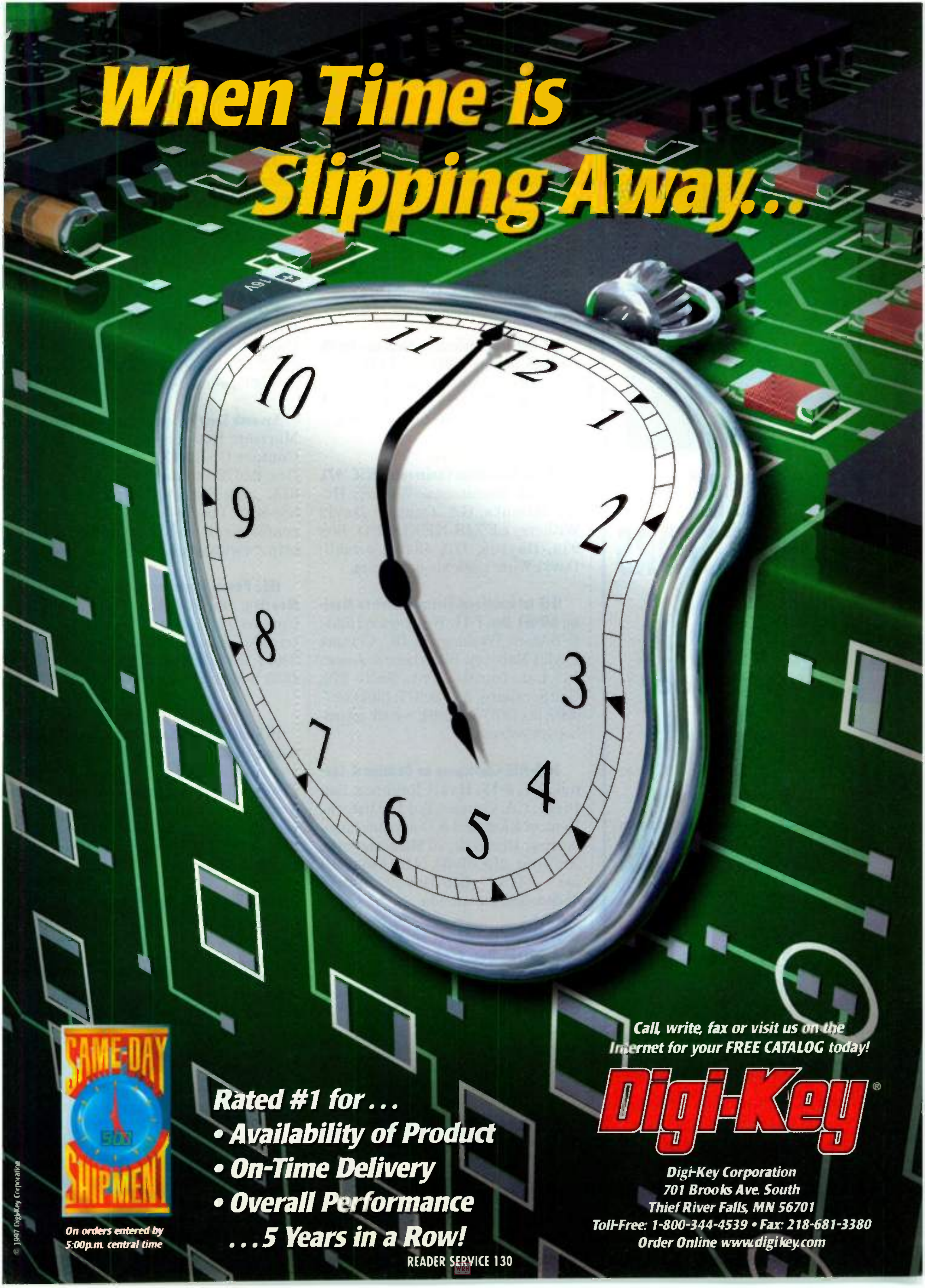
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Asian Test Symposium, Nov. 17-19. Akita, Japan. Contact Y. Takamatsu, +81 89 927-9955; e-mail: takamatsu@cs.ehime-u.ac.jp.

COMDEX/Fall '97, Nov. 17-21. Las Vegas Convention Center, Las Vegas, NV. Contact Softbank Comdex Inc., 300 First Ave., Needham, MA 02194-2722; (617) 433-1500; Internet: http://www.comdex.dom.

IPC National Conference: Solutions for Ultra-High-Density PWBs, Nov. 20-21. Biltmore Hotel, Santa Clara, CA. Contact John Riley, IPC director of education, (847) 509-9700, ext. 308.

DECEMBER 1997

Winter Simulation Conference (WSC '97), Dec. 7-10. Renaissance Waverly Hotel, Atlanta, GA. Contact David Withers, LEXIS-NEXIS, P.O. Box 933, Dayton, OH 45401; e-mail: David.Withers@lexis-nexis.com.

IEEE International Electron Devices Meeting (IEDM), Dec. 7-11. Washington Hilton & Towers, Washington, DC. Contact Phyllis Mahoney, Widerkehr & Assoc., 101 Lakefrorest Blvd., Suite 270, Gaithersburg, MD 20877; (301) 527-0900; fax (301) 527-0994; e-mail: pwmahoney@aol.com.

36th IEEE Conference on Decision & Control, Dec. 8-12. Hyatt Regency, San Diego, CA. Contact Ted E. Djaferis, Dept. of Electrical & Computer Engineering, University of Massachusetts, Amherst, MA 01003; (413) 545-3561; fax (413) 545-1993; e-mail: djaferis@ecs.umass.edu.

Workshop on Internet Technology & Systems (WITS), Dec. 9-12. Marriott Hotel, Monterey, CA. Contact USENIX Conference Office, 22672 Lambert Street, Suite 613, Lake Forest, CA 92630; (714) 588-8649; fax (714) 588-9706; e-mail: conference@usenix.org; Internet: http://www.usenix.org.

JANUARY 1998

Seventh Joint Magnetism & Magnetic Materials Conference (INTEMAG), Jan. 6-9. Hyatt Regency Embarcadero Hotel, San Francisco, CA. Contact John Nyenhuis, School of ECE, Purdue Univ., West Lafayette, IN 47907-1285; (317) 494-3524; fax (317) 494-2706; e-mail: smag@ecn.purdue.edu.

Annual Reliability & Maintainability Symposium/Product Quality & Integrity (RAMS), Jan. 20-22. Anaheim Marriott, Anaheim, CA. Contact V.R. Monshaw, Consulting Services, 1768 Lark Lane, Cherry Hill, NJ 08003; (609) 428-2342.

Photonics West, Jan. 24-30. San Jose, CA. Contact the SPIE Exhibits Dept., P.O.Box 10, Bellingham, WA 98227-0010; (360) 676-3290; fax (360) 647-1445; e-mail: exhibits@spie.org.

Seventh Security Symposium, Jan. 26-29. Marriott Hotel, San Antonio, TX. Contact USENIX Conference Office, 22672 Lambert Street, Suite 613, Lake Forest, CA 92630; (714) 588-8649; fax (714) 588-9706; e-mail: conference@usenix.org; Internet: http://www.usenix.org.

IEEE Power Engineering Society Winter Meeting, Jan. 31-Feb. 5. Tampa, FL. Contact Jim Howard, Tampa Electric Co., P.O. Box 111, Tampa, FL 33601; (813) 228-4653; fax (813) 228-1333; e-mail: j.howard@ieee.org.

FEBRUARY 1998

IEEE International Solid-State Circuits Conference (ISSCC '98), Feb. 5-7. San Francisco Marriott, San Francisco, CA. Contact Diane Suiters, Courtesy Associates, 655 15th St. N.W., Washington, DC 20005; (202) 639-4255; fax (202) 347-6109; e-mail: isscc@courtesyassoc.com.

Portable by Design, February 9-13. Santa Clara Convention Center, Santa Clara, California. Contact Rich Nass, Electronic Design, 611 Route 46 West, Hasbrouck Heights, New Jersey 07604; (201) 393-6090; fax (201) 393-0204; e-mail: portable@class.org.

The Wireless Symposium and Exhibition, Feb. 9-13. Santa Clara Convention Center, Santa Clara, California. Contact Bill Rutledge, Penton Publishing, 611 Route 46 West, Hasbrouck Heights, NJ 07604; (201) 393-6259; fax (201) 393-6297; instant faxback (800) 561-7469; Internet: http://www.penton.com/wireless.

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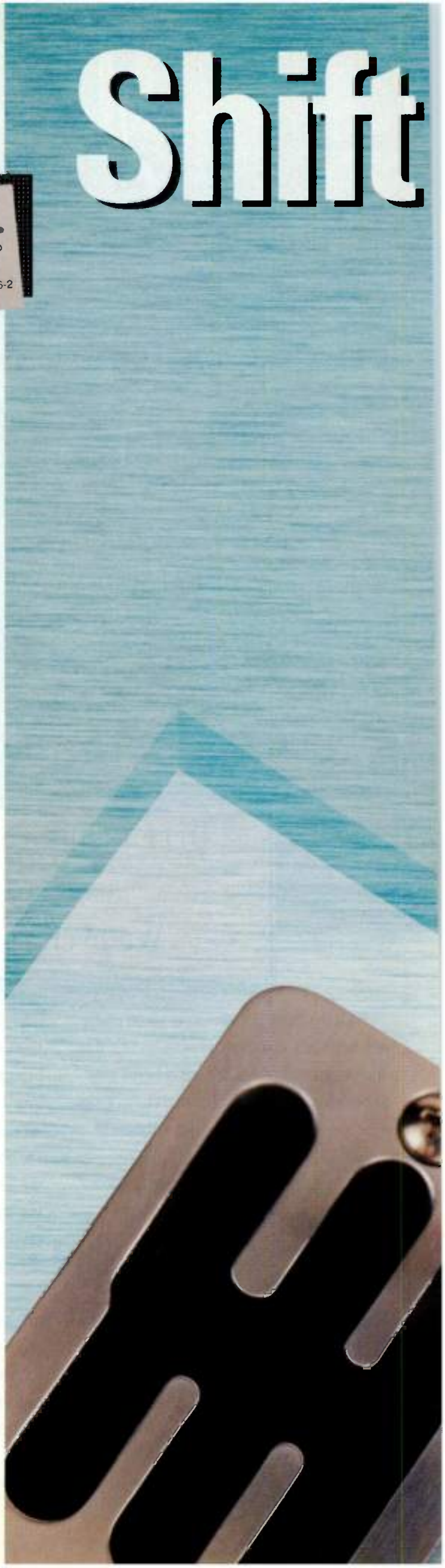

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EPF10K100A	100,000	4,992	24 Kbits	35%	3.3 V
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FEBRUARY 1998

IEEE Applied Power Electronics Conference and Exposition (APEC '98), Feb. 15-19. The Disneyland Hotel, Anaheim, CA. Contact Pamela Wagner, Courtesy Associates, 655 15th St., N.W., Suite 300, Washington, DC 20005; (202) 639-4990; fax (202) 347-6109; e-mail: pwagner@courtesyassoc.com.

Conference on Optical Fiber Communication (OFC '98), Feb. 22-27. San Jose Convention Center, San Jose, CA. Contact Lisa Myers, OSA Conference Services, 2010 Massachusetts Ave., N.W., Washington, D.C. 20036-1023; (202) 416-1980; fax (202) 416-6100; e-mail: ofc.info@osa.org.

Design, Automation, and Test in Europe Conference and Exhibition (DATE '98), Feb 23-26. Le Palais des Congres de Paris, Porte Maillot. Contact European Conferences, 11C Wemyss Pl., Edinburgh EH3 6DH, UK; +44 131-225-2892; fax +44 131-225-2925.

38th Israel Conference on Aerospace Sciences, Feb. 25-26. Tel-Aviv & Haifa. Contact Technion-Israel Institute of Technology, Haifa 32000, Israel; 972-4-8292713; fax, 972-4-8231848; e-mail: alice@aerodyne.technion.ac.il.

MARCH 1998

International Verilog Converfence and VHDL International User Forum (IVC/VIUF), Mar. 16-19. Santa Clara Convention Center, Santa Clara, CA. Contact MP Associates, 5305 Spine Rd., Suite A, Boulder, CO 80301; (303) 530-4562; fax (303) 530-4334; e-mail: lee@mpa-net.com; Internet: http://www.hdl-con.org.

Second Intellectual Property in Electronics Seminar (IP '98), Mar. 23-24. Westin Hotel, Santa Clara, CA. Contact John Whitaker, Miller Freeman Technical Ltd., +44 181-316-3297; e-mail: ed98@cityscape.co.uk.

Sixth Annual Embebbed Systems Conference East, March 31-April 2. Chicago's Navy Pier Festival Hall, Chicago, IL. Contact Miller Freeman Inc., 600 Harrison St., San Francisco, California 94107; (415) 905-2354; fax (415) 905-2220; Internet: http://www.embedsyscon.com/.

APRIL 1998

Southeastcon '98, Apr. 10-15. Hyatt Regency, Orlando International Airport, Orlando, FL. Contact Parveen Ward, ECE Dept., University of Central Florida, Orlando, FL 32816; (407) 823-2610; fax (407) 823-5835; e-mail: pfw@ece.engr.ucf.edu.

MAY 1998

IEEE International Conference on Evolutionary Computation, May 3-9. Ankorage, AK. Contact Patrick K. Simpson, Scientific Fishery Systems Inc., P.O. Box 242065, Anchorage, AK 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@akaska.net.

IEEE International Conference on Neural Networks (ICNN '98), May 3-9. Anchorage, Alaska. Contact Patrick K. Simpson, Scientific Fishery Systems Inc., Post Office Box 242065, Anchorage, Alaska 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@akaska.net.

IEEE World Congress on Computational Intelligence, May 3-9. William A. Egan Civic and Convention Center, Anchorage, AK. Contact Patrick K. Simpson, Scientific Fishery Systems Inc. P.O. Box 242064, Anchorage, AK 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@alaska.net.

Seventh IEEE International Fuzzy Systems Conference, May 3-9. Anchorage, Alaska. Contact Patrick K. Simpson, Scientific Fishery Systems Inc., Post Office Box 242065, Anchorage, Alaska 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@alaska.net.

IEEE/IAS Industrial & Commercial Power Systems Technical Conference (I&CPS), May 4-7. Edmonton, Alberta, Canada. Contact Marty Bince, Modicon Canada Ltd., 5803 86th St., Edmonton, Alberta T6E 2X4, Canada; (403) 468-6673; fax (403) 468-2925.

IEEE International Conference on Acoustics, Speech & Signal Processing (ICASSP '98), May 12-15. Seattle Convention Center, Seattle, Washington. Contact Les E. Atlas, Dept. EE(FT 10), University of Washington, Seattle, Washington 98195; (206) 685-1315; fax (206) 543-3842; e-mail: atlas@ee.washington.edu.

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CONFERENCE PREVIEW

Sights And Sounds Are Abounding At The Fall Comdex Conference

Highlights Of The Annual Trade Show Include A PCI Audio System, DVD Products, And Other Audio/Video Devices.

Richard Nass

Once again, the Comdex Fall '97 trade show promises to be a blitz of sight and sound, as each of the multimedia-product vendors tries to outdo one another. This year's show takes place on Nov. 17-21 in Las Vegas, Nev. Each year, the noise level rises slightly, and a preview of the products to be announced ensures that this trend will continue.

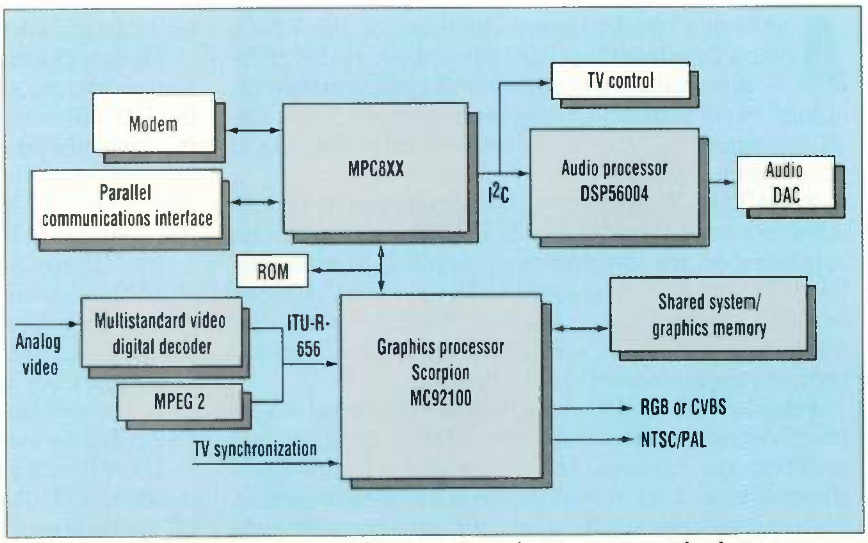
One product sure to garner attention is the EMU8010 PCI audio system, developed by the E-Mu Systems Div. of Creative Labs Inc., Scotts Valley, Calif. The chip's features include a bus-mastering PCI interface, up to 32 Mbytes of RAM mapped to host memory, on-chip page-mapped memory-management support for 4-kbyte pages of sound RAM, an on-chip MPU-401-compatible MIDI UART, and interfaces for Zoom Video (ZV) audio and a host modem.

The chip contains an effects engine that executes 512 instructions in each sample period. The engine receives 31 input audio streams; sixteen come from the wavetable-synthesizer channels, and six of the remaining streams come from three asynchronous sources (two each from the CD-ROM digital-audio receiver, the ZV interface, and the general-purpose SPDIF receiver). The engine outputs 32 streams: two to both the AC97 stereo digital-to-audio converter (DAC) and the main SPDIF output; six to the other SPDIF outputs; and one to a sample-rate converter for a bus-mastering transfer to host memory.

An on-chip cache is available for each audio channel. The caches are filled with data from the host memory. The data is sent to the interpolator, and is then prefetched in the caches based on the memory addresses programmed into the channel. The 4-kbyte pages allow contiguous logical audio memory to be relocated into noncontiguous 4-kbyte blocks of host memory. A 24-bit sound-memory address can be generated, using up to 16 Msamples. An 8-bit sample size is supported in host memory on a channel-by-channel basis. The chip also can playback interleaved 8- and 16-bit samples by pairs of adjacent tracks.

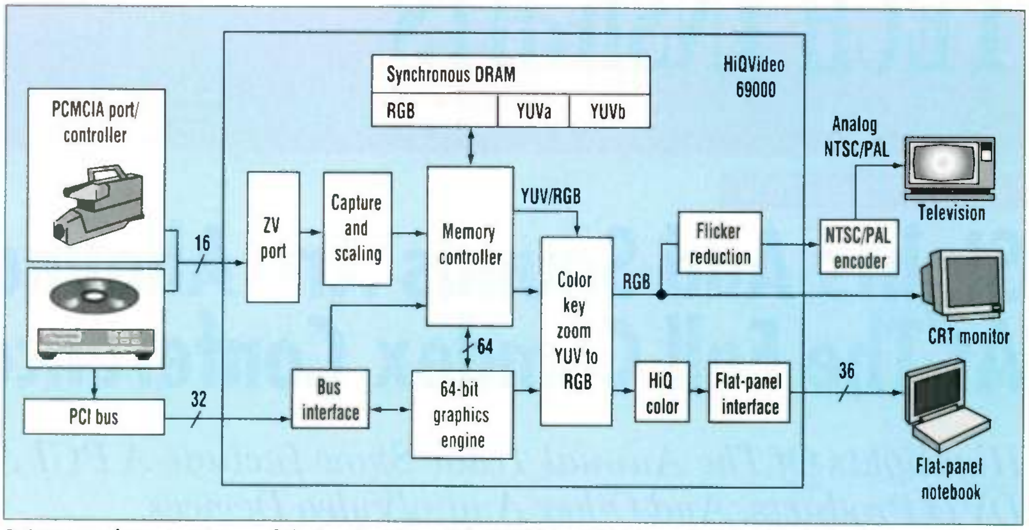
The PCI audio chip contains a programmable codec and mixer interface, whose characteristics are determined at reset and initialization by the EEPROM and the hardware-control register. The interface defaults to the AC97 codec, but also supports generic I2S to both analog-to-digital converters (ADCs) and DACs, the Creative V32A codec-mixer, or a 16-, 18-, or 20-bit latch-enabled DAC. In all cases, the codec audio streams are logically connected to the effects engine.

The EMU8010's multifunction PCI interface is compatible with Revision 2.1 of the PCI specification. Its PCI core buffers write commands to the internal registers. These commands are then normally completed with minimal wait states. PCI reads to internal registers



1. The Scorpion chip lets designers assemble interactive television systems. The chip accepts a standard ITU-R-656 video stream with embedded synchronization codes as well as an input from MPEG-2, DVD, and other digital-video sources. A glueless interface to an external processor, such as a PowerPC or ColdFire, is included.

are typically completed in one bus operation with some number of wait states for reading RAM-based registers. If a PCI read is decoded while any previous PCI write is pending, a retry termination will occur for the read.



2. Integrated memory is one of the key features of the HiQVideo 69000 graphics IC. The single-chip controller connects directly to a PCI bus or a ZV. Aimed at mainstream notebooks, it consumes just 350 to 650 mW.

DVD Comes Of Age

Last year's show proved to be the starting point for the digital video disk (DVD) industry. There were many demonstrations of players both in the computer and consumer space. This year's show will offer much of the same, with enhancement to both audio and video. The latest generation of Pentium-class microprocessors, specifically the Pentium II, gives system designers the flexibility to handle audio and video in either hardware or software. Each of the combinations has its trade-offs, and also is dictated by performance and cost issues.

DVD technologies offer much promise to application and game developers, as well as movie-title producers. Current storage capacities are 4.7 Gbytes for a single data layer, single-sided disk; 8.5 Gbytes for a dual data layer, single-sided disk; 9.4 Gbytes for a single data layer, dual-sided disk; and 17 Gbytes for a dual data layer, dual-sided disk. The initial releases are of the first variety, which is still over six times the capacity of a traditional CD-ROM. DVD also adds MPEG-2 video and Dolby Digital Surround Sound AC-3 audio, a realistic multimedia and computing environment.

One vendor that's remained at the leading edge of the DVD spectrum is the Disk Products Div. of Toshiba America Information Systems Inc., Irvine, Calif. The company will showcase its slimline DVD-ROM Drive aimed at notebook manufacturers. The SD-C2002, which measures 17-mm high and weighs 380 g, brings a new class of applications to mobile users, including digital video and audio playback; fast data transfer for interactive applications; on-line storage; data retrieval; and movie viewing. The low height results from the use of a low-

VIP Ushers In New Era Of PC Video

As the need for PC-based video grows, the VESA Video Interface Port (VIP) offers an open video architecture standard that meets the performance requirements of current and next-generation platforms. The VIP standardizes the interface between video devices and the graphics controller.

The VESA VPort Committee, consisting of over 15 member companies involved in PC video and graphics, hammered out the specification which should be ratified by the end of this year. The recently released PC98 Guidelines from Microsoft acknowledges the committee's work—the VESA VIP standard is "strongly recommended," and will become a requirement in the near future.

Prior to VIP, the PC video market was forced to embrace a number of incompatible proprietary standards and architectures. Some of the architectures relied on asynchronous buses that weren't designed for video streaming. Such architectures are ill-suited for isochronous video data types, and are already showing limitations with no future enhancement possibility. Clearly, the incompatibility, unpredictability of performance, and overall confusion inhibits the growth of the PC video market.

These problems formed the impetus for the VIP. With a nonproprietary standard specifically designed for video, the VIP offers mix-and-match flexibility and encourages the development of a wide range of low-cost PC-oriented video devices. Numerous leading companies are currently developing VIP-based products, with the hope of demonstrating them at Fall Comdex '97.

The VIP consists of two ports: a 9-pin video port, and a 4-pin bidirectional host port for control and data transfer. The VIP only requires 13 pins for a graphics chip implementation. This is an important advantage as graphics chip designers typically suffer severe pin limitations. The low pin-count has another benefit. It fits into the existing 26-pin VESA feature connector.

The VIP offers the advantage of a de facto industry standard, ITU-R-656, with extensions that are useful for PC applications. For example, the support of dummy data during active video is an extension that is particularly useful for video scaling.

(continued on page 42)

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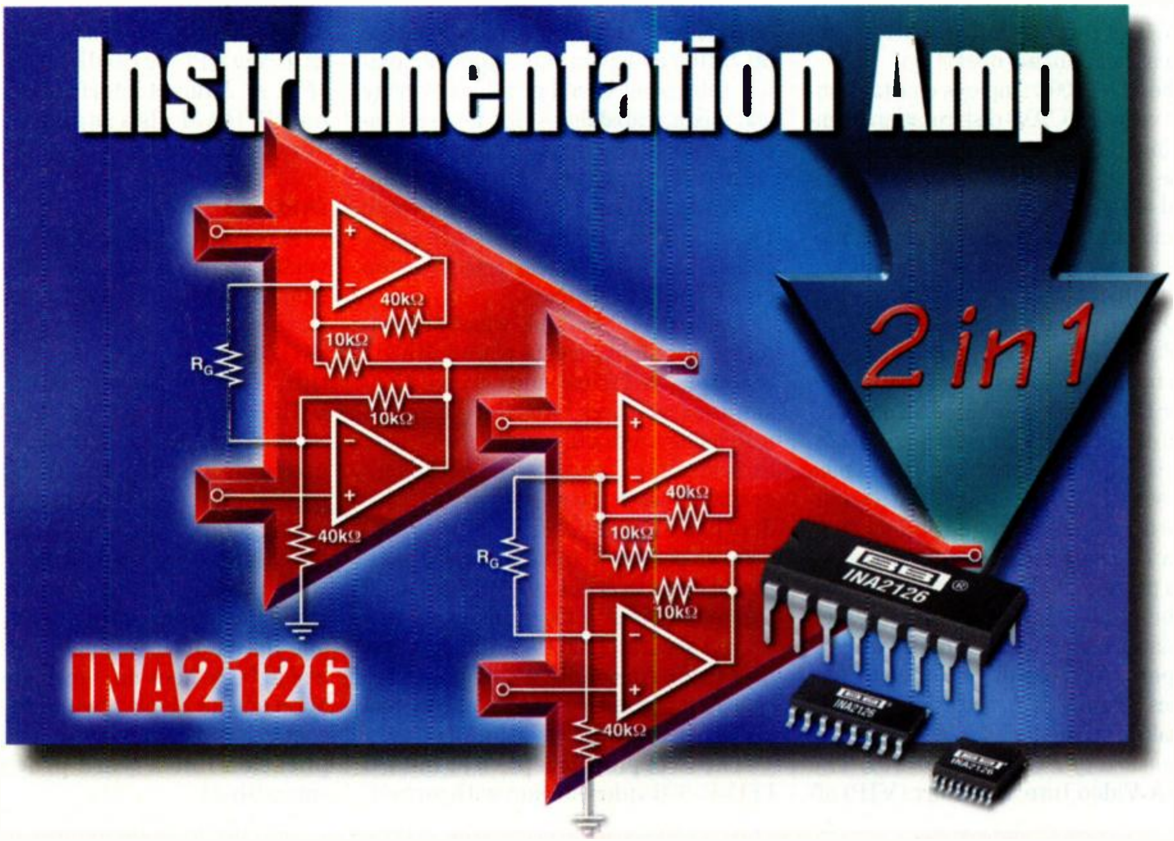

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INA2126 dual precision instrumentation amplifier features excellent performance with very low quiescent current (175µA/channel). In addition, a wide operating voltage range of ±1.35 to ±18V makes INA2126 ideal for low cost portable instrumentation and data acquisition systems.

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Key Specifications

- Low Quiescent Current.............................175µA/channel
- Wide Supply Range..............................±1.35 to ±18V
- Low Offset Voltage..250µV max
- Low Offset Drift..3µV/°C max
- Low Noise...35nV/√Hz
- Gain Equation...5 + 80kΩ/R_G

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Distributors: Anthem: (800) 826-8436 • **Digi-Key Corp:** (800) 338-4105 • **Insight Electronics:** (888) 488-4133 • **J.I.T. Supply:** (800) 246-9000 • **Sager Electronics:** (800) 724-3780 • **SEMAD (Canada):** (800) 567-3623 profile optical pick-up head and a thin disk motor. The drive can read all types of DVD data, as well as CD-ROMs and CD-R media. What further suits it for portable applications is its low power draw, with an average consumption of 3.0 W. The result is longer battery life and less heat during operation.

The SD-C2002 employs constant angular velocity (CAV) disk rotation to enable fast data transfers from any place on the disk. With the constant rotational speed of CAV, the drive can read the inner and outer tracks of data on the media at different speeds. The result is a data transfer rate of 2.7 Mbytes/s for DVD media, and 2.4 Mbytes/s for CD-ROM media. It also supports synchronous burst transfers of 16.7 Mbytes/s under DMA multiword Mode-2 and PIO Mode 4. An ATAPI interface and a 128-kbyte cache buffer to further enhance performance. Other specifications include a 110-ms average random seek and a 180-ms average random access when playing DVD media.

The popularity of PC-based video mandates a standard for hardware developers. As a result, the Video Electronics Standards Association (VESA) has taken on the task *(see "VIP ushers in new era of PC video," p. 40)*. The VESA Video Interface Port (VIP) offers an open video architecture standard that meets the performance requirements of both current and next-generation platforms.

Interactive Television

Dealing with similar applications, the MC92100 Scorpion chip supplies flexible, television-based graphics overlay and mixing capabilities that let users incorporate interactive features into new and existing products. Designed by Motorola's Semiconductor Products Sector, Phoenix, Ariz., the chip suits such applications as intelligent televisions, set-top boxes, and DVD players.

Using the IC, multiple windows of interactive graphics can be placed directly on top of a traditional video stream. Consequently, users can, for example, watch television while, at the same time, browsing the Internet. The Scorpion's graphics match the resolution and color depth of standard NTSC/PAL baseband video. A selectable square pixel filter ensures that both computer-based and television-specific graphics are displayed accurately in their intended aspect ratio. An adaptive deflicker filter checks the graphics on a pixel-by-pixel basis to maintain a flicker-free display.

The Scorpion accepts a standard ITU-R-656 video stream with embedded synchronization codes. Or, the video can be genlocked with a television horizontal flyback and vertical synchronization signal. The input also can come from MPEG-2, DVD, and other digital-video sources. A glueless interface to an external processor, such as a PowerPC or ColdFire, is included *(Fig. 1)*. A direct interface to an external SDRAM also supports up to 4 Mbytes of memory.

Dual Displays

A few years ago, graphics-controller vendors gave laptop users the ability to simultaneously display the same image on the laptop's liquid crystal display (LCD) and an external cathode-ray tube (CRT). Now, thanks to the ViRGE/MXi developed by S3 Inc., Santa Clara, Calif., users can simultaneously display two different and independent images. For example, while giving a presentation, the user could have the presentation mode of the software running on the external display, while the laptop's display contains the speaker notes. A second example would be to keep an e-mail application open on one display, while the second contains some type of productivity application like a word processor or spreadsheet.

(continued from page 40)

The VIP's Host Port, though consisting of only four signals, supports many different transfer types. A transfer can be terminated by either the master or the slave at any byte boundary. Other features of the VIP's Host Port include hardware polling, time-out, and retry. These features offer a great deal of flexibility and efficiency for a wide range of applications.

While the video port is owned by one device at any given time, the host bus is a shared resource. This offers tremendous flexibility in many current and future applications. For example, it is possible to play a DVD movie while the video decoder captures Intercast or VBI data from a TV channel and transfers them to the graphics chip through the host bus.

In addition, the VIP supports the Plug-and-Play and Power-Down Mode features. Upon power-up, the graphics controller polls the locations of the VIP address space, then reports the ensuing result to the Plug-and-Play configuration manager. The Power-Down Mode allows the graphics chip to put the VIP slave devices to sleep, then stops the clock and the control signals.

Consider a design example where two VIP modules are attached to the graphics chip. One board can act as a DVD module that plugs directly into the graphics board. The other can act as a TV tuner-video-capture board connected to the graphics board through a low-cost VESA Feature Connector ribbon cable.

In this example, compressed DVD data is transferred to the DVD module through the VIP host port. The decompressed data is then transferred through the VIP video port to the graphics frame buffer, and is subsequently displayed on the monitor.

Note: The VIP is a device-level standard, not a system-level standard. In other words, it's an OEM standard, not a retail standard. Though mechanical examples are given in the specification, manufacturers are free to develop custom solutions to address specific needs. For example, it's possible to implement the entire VIP system on the same graphics adapter or even the motherboard without using modules. This also lets OEMs to differentiate their products.

The VIP is being developed as an upgradable standard. Future generations will feature extensions to both the video and host buses to support significantly more demanding applications such as HDTV.

The VESA VIP also works with IEEE 1394, an external isochronous bus (the VIP is an internal isochronous bus). An interface linking the two buses offers a compelling solution for demanding PC video applications.

Contributed by Chris Lam, SGS-THOMSON Microelectronics Inc.

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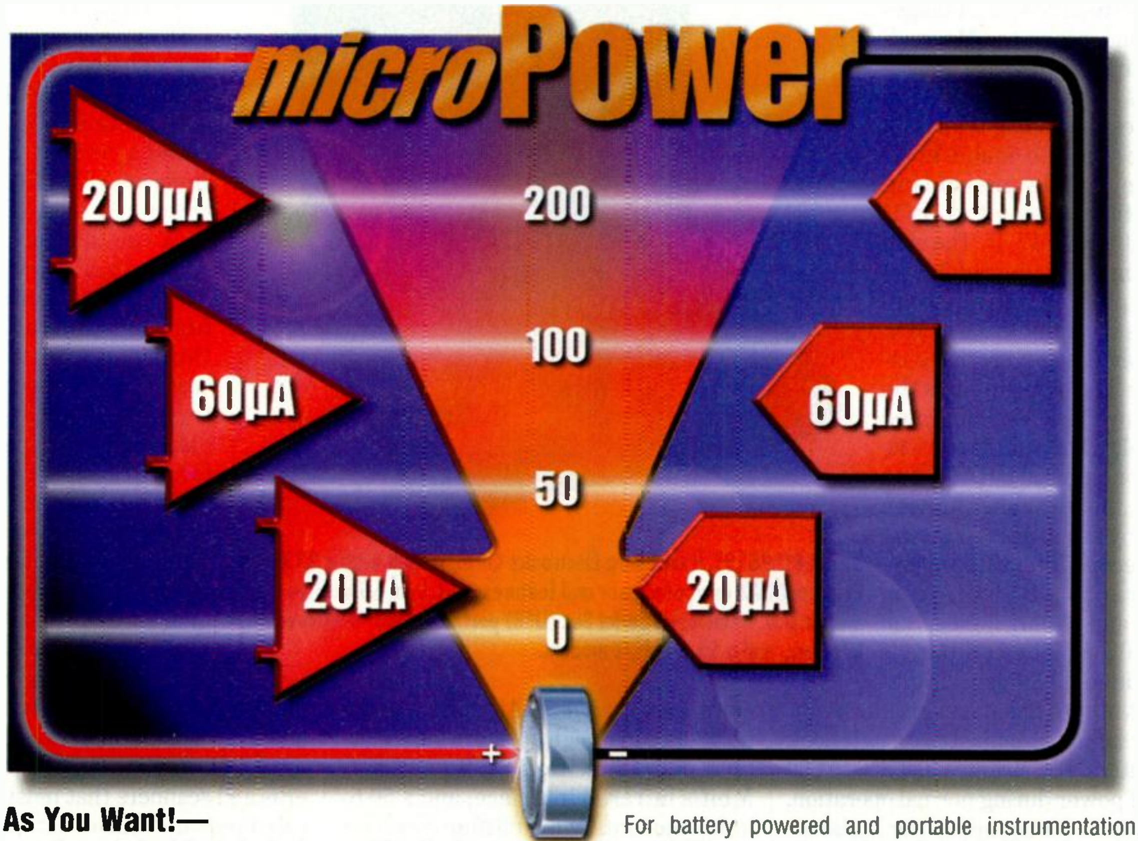

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ADS7816	12	+5	1.9	Yes	8-DIP, SO-8, MSOP-8	11355	80
ADS7817	12	±2.5	2.3	Yes	8-DIP, SO-8, MSOP-8	11369	81
ADS7822	12	+5	0.54	Yes	8-DIP, SO-8, MSOP-8	11358	82
ADS1212	22 at 10Hz, 16 at 1kHz	+5	1.4	Yes	18-DIP, SO-18	11360	83
ADS1213	22 at 10Hz, 16 at 1kHz	+5	1.4	Yes	24-DIP, SO-24	11360	84
ADS1214	22 at 10Hz, 16 at 1kHz	+320mV	1.4	Yes	18-DIP, SO-18	11368	86
ADS1215	22 at 10Hz, 16 at 1kHz	+320mV	1.4	Yes	24-DIP, SO-24	11368	87

IAs

Product	I_Q (µA)	Description	Channels	Packages	FAXLINE#	Reader#
INA122	60	Single Supply Instrument Amp	1	SO, DIP	11388	88
INA126	175	Precision Instrument Amp	1, 2	MSOP, SO, DIP	11365	89
INA132	160	Difference Amp	1	SO, DIP	11353	90

Op Amps

Product	I_Q (µA)	Description	SR (V/µs)	Channels	Packages	FAXLINE#	Reader#
OPA336	20	CMOS	0.03	1, 2, 4	SOT-23, MSOP, SO, DIP	11380	91
OPA241	25	Precision	0.01	1	SO, DIP	11406	92
OPA237	170	Gen. Purpose	0.5	1, 2, 4	SOT-23, MSOP, SSOP, SO	11327	142

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The ViRGE/MXi works with 2 Mbytes of integrated DRAM to offer high-end 2D and 3D performance, as well as improved power management and integrated Macrovision for DVD devices. Macrovision copy protection modifies the analog television output signal to enable DVD viewing while preventing users from taping the DVD content with a VCR. The chip offers an easy upgrade path, as it is pin- and software-compatible with the ViRGE/MX, the previous-generation controller. The chip employs the company's S3RAM integrated DRAM, which eliminates the need for external DRAM. As a result, power consumption drops by as much as 50%.

A second integrated-memory graphics IC hails from Chips and Technologies, San Jose, Calif. The company's HiQVideo 69000 is a single-chip, 2-Mbyte flat-panel graphics controller aimed at mainstream notebook computers. It consumes just 350 to 650 mW of power during normal operation. The chip features support for high-resolution modes, real-time video acceleration, 16:9 aspect-ratio support, vertical and horizontal bilinear video interpolation, and a flicker-free reduction process for television displays. It connects to a PCI bus or a ZV Port for 30-frame/s video capture *(Fig. 2)*.

Portable-system designers can get full support for the Mobile Pentium MMX processors by employing the MobilePRO BIOS, developed by SystemSoft Corp., Natick, Mass. The software saves power by using a stop-grant/auto-halt power-down mode. Because the software is compatible with the Pentium II line of microprocessors, designers can easily upgrade from a standard Pentium processor. A bundled suite includes the BIOS, firmware layers to support PCI, Plug-and-Play, power management, Universal Serial Bus (USB), and the Advanced Configuration and Power Interface (ACPI).

A portable PC that takes advantage of the latest technology is the PC-9820T, designed by Sharp Electronics Corp., Mahwah, N.J. The laptop computer is built with a 233-MHz Pentium MMX microprocessor *(Fig. 3)*. Also included are a 13.3-in. super high aperture (SHA) active-matrix LCD, a USB port, a 4-Mbit/s infrared interface, and a 56.6-kbit/s modem. Two multifunction bays let users swap in a floppy-disk drive, a CD-ROM drive, an extra battery, or an ac adapter, depending on their needs. The company claims that the SHA display gives an XGA resolution about 60% brighter and draws 33% less power than conventional active-matrix displays.

3. The PC-9820T, from Sharp Electronics Corp., is built with a 233-MHz Pentium MMX microprocessor and features a 13.3-in. SHA active matrix LCD, a Universal Serial Bus (USB) port, a 4-Mbit/s infrared interface, and a 56.6-kbit/s modem.

USB Support

The USB continues to increase in popularity from many different aspects—from system designers to application and firmware developers to end users. Peripheral developers can reduce their products' time-to-market using the Human Input Device (HID) Simulator from LCS/Telegraphics Inc., Cambridge, Mass. The HID Simulator permits firmware and driver development to occur concurrently. It emulates the device being developed and demonstrates correct device behavior, creating a log of successful USB communications. It also allows for the emulation of most HIDs for testing and development purposes by modifying the descriptor fields in the accompanying software. Target products include joysticks, keyboards, and mice.

A pair of 8-bit microcontrollers from Mitsubishi Electronics America Inc., Sunnyvale, Calif., are designed for USB applications. The M37640 is a high-end device tuned for 12-Mbit applications (the maximum rate for USB) such as audio, printing, and digital cameras. The M37532 is for lower-speed cost-sensitive applications like mice, joysticks, gamepads, and keyboards.

The M37640 contains a USB function-control unit that third-party developers can customize for specific applications. It supports the four data-transfers types specified for USB—control, isochronous, interrupt, and bulk. Each transfer type is employed for a different class of peripheral. Isochronous transfers provide guaranteed bus access and a constant data rate. Interrupt transfers are for HIDs that must infrequently communicate small amounts of data. Bulk transfers are necessary for devices such as digital cameras and scanners that must communicate large amounts of data, but only as bus bandwidth becomes available. Control transfers also are useful for burst data and host-initiated communications, where bus management is a concern.

The analog transceiver in the M37640 is integrated into the chip, eliminating the need for an external device. The chip generates the 48-MHz clock using a frequency synthesizer. To optimize a design for maximum EMI reduction, the synthesizer will run on an oscillator that generates an operating frequency as low as 6 MHz. To reduce power consumption, the chip features wait and stop modes.

The M37532 offers a typical operating current of 8 mA, which equates to 40 mW at 5 V. The part can operate from a supply voltage as low as 4.1 V. It features an 8-channel, 10-bit ADC, 16 kbytes of ROM, 29 programmable I/O ports, and three 8-bit timers.

How Valuable	Circle
Highly	554
Moderately	555
Slightly	556

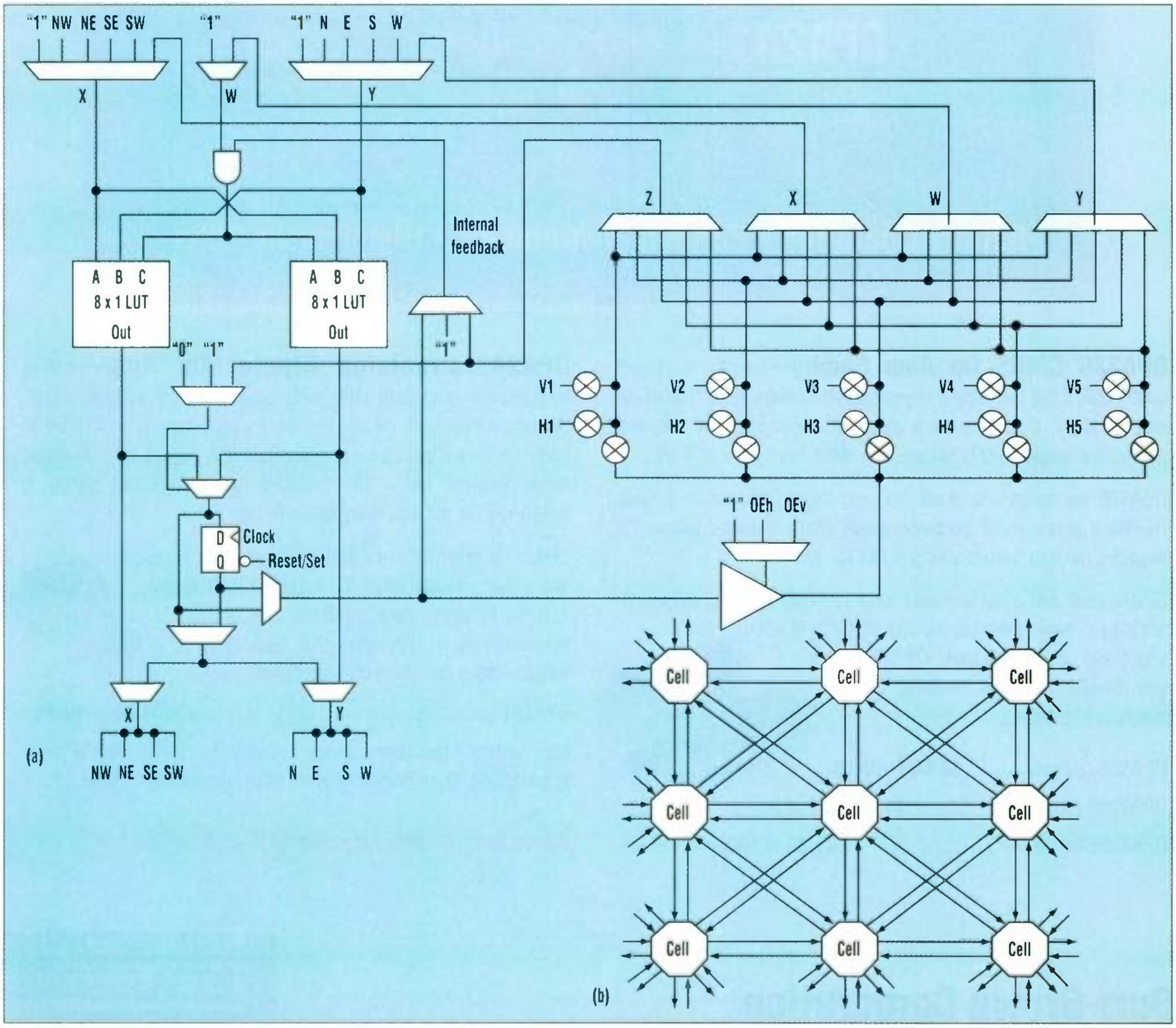
FPGAs Pack Distributed SRAM And Flexible Logic

Small Blocks Of SRAM And Eight-Way Logic Cell Connectivity Combine To Give FPGAs High Flexibility.

Dave Bursky

When implementing systems with field-programmable gate arrays (FPGAs), designers are constantly asking for improved on-chip connectivity to make better use of the on-chip resources and obtain faster logic structures. And for many of the larger designs—circuits with 10,000 gates or more—on-chip memory is a key factor to efficiently implement register files, I/O buffers, and other storage-intensive functions.

Addressing all of these issues and more, the AT40K series of dynamically reconfigurable field-programmable gate arrays from Atmel provides a logic-efficient, SRAM-based solution that allows the efficient synthesis of high-density behavioral designs with



1. Atmel's AT40K "medium-grain" core logic cells include dual 3-input LUTs, an upstream AND gate, a register, clock and preset inputs, and registered or non-registered internal feedback (a). Instead of just the common North, East, South, and West inputs, the cells allow diagonal connections (b).

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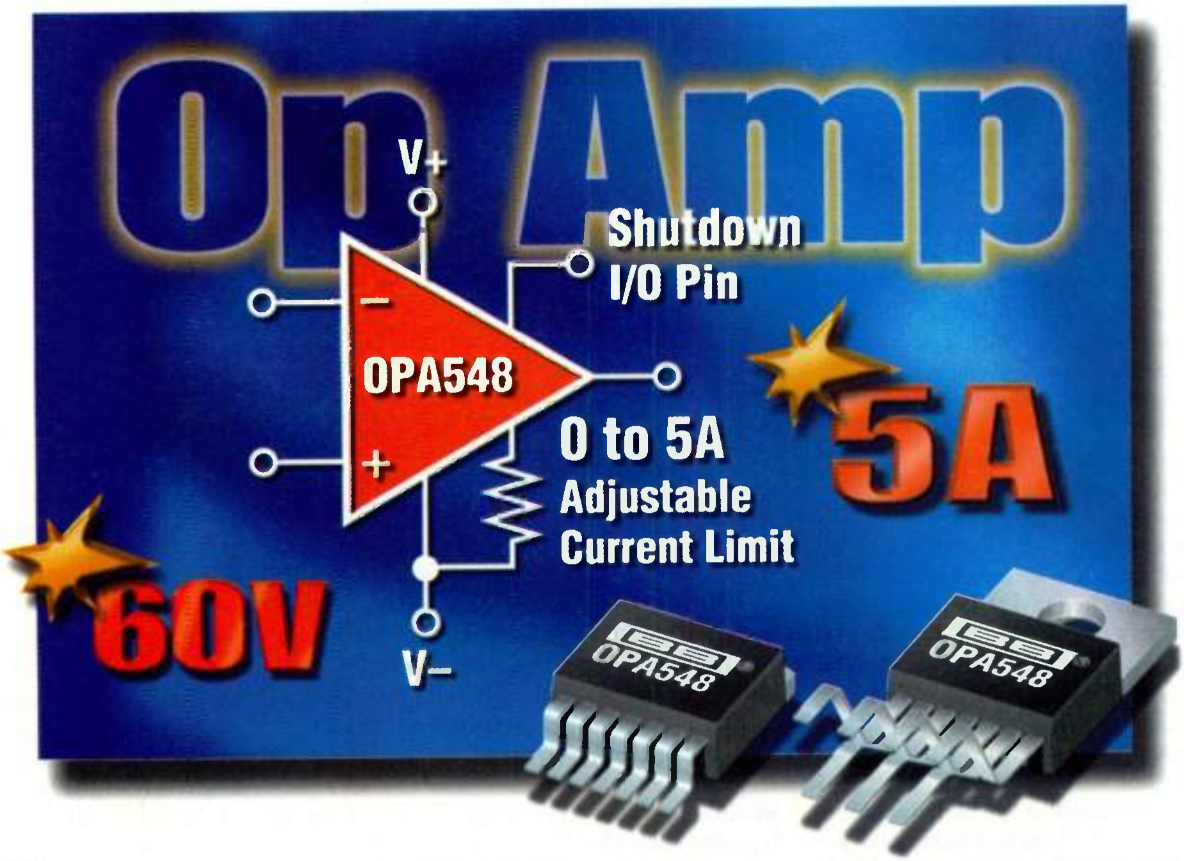

OPA548—easy to use and it packs a peak output of 5A (3A continuous). It operates on up to ±30V dual supplies or a +60V single supply. Input common-mode range extends below V– to simplify single supply circuits. It's ready made for driving heavy loads such as motors, valves, speakers, or as a programmable V/I source.

More Control—OPA548 gives you more control over your high output current circuitry. Internal current limit and thermal shutdown protect it from overload. A low power resistor, potentiometer, or a programming voltage (D/A converter) sets the current limit. A logic output signal on the shutdown I/O pin tells you if thermal shutdown has occurred. You can even apply a logic signal to this same pin to shut down the amplifier, reducing the quiescent current.

OPA548 is available in two power packages: 7-lead DDPAK and 7-lead TO-220. It is priced from **$5.45** in 1000s.

Products	Description	Max V_S (V)	Peak I_{OUT} (A)	Slew Rate (V/µs)	Packages	Dual Available	FAX*LINE#* (800) 548-6133	Reader Service #
OPA548	Single Supply, Shutdown	60	5	10	TO-220, DDPAK		11389	220
OPA547	Single Supply, Shutdown	60	0.75	6	TO-220, DDPAK		11326	221
OPA544	FET-Input	70	2	8	TO-220, DDPAK	X	11250	222
OPA541	High Current, FET-Input	80	9	10	Power Plastic, TO-3	X	10737	223
OPA512	Very High Current	100	15	4	TO-3		10600	224

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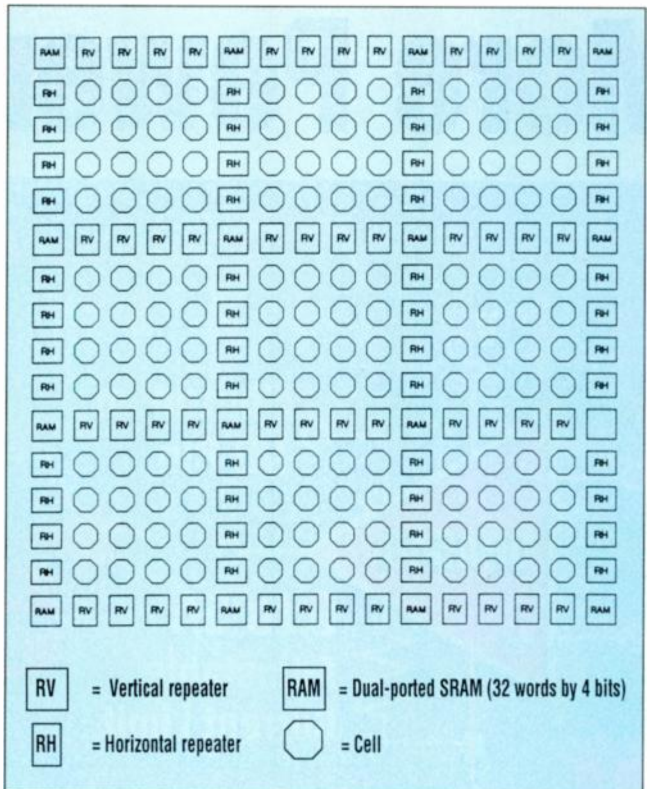
Available in complexities from 8000 to 50,000 gates, AT40K series member are considered to use medium-grained logic cells. Each look-up table (LUT)-based cell has a four-input logic block that consists of two 3-input LUts, an upstream AND gate, a register with selectable registered or nonregistered internal feedback, and inputs for Clock and Preset signals *(Fig. 1a)*. A single cell can be used to implement any two 3-input functions (adders, counters, decoders, etc.), or any single 4-input function (multiplexers, 4-bit parity generators, flip-flops, etc.).



2. To reduce bus loading and provide local, minimal delay memory, the AT40K FPGAs surround each sector (a group of 16 logic cells) with a hierarchy of bus wires as well as bus repeaters. In the corner of each sector, a 32-word by 4-bit block of dual-port/single-port SRAM provides a configurable local block of memory.

By configuring the cell, designers can use the logic in four basic modes—arithmetic, DSP, networking, and logic synthesis. In the arithmetic mode, the two 3-input LUTs with two outputs serve as a full adder or simple counter stage. In the DSP mode, the full adder can be combined with the cell's upstream AND gate to form a multiplier cell. In the networking mode, the two LUTs can be combined to form a 2-to-1 multiplexer with three-stated output—ideal for complex switches and large multiplexing tree structures. The logic synthesis mode allows the 3-input LUTs to be combined to create a 4-input LUT with or without a registered output—a structure that supports the synthesis of random logic functions.

Unlike LUT cells in other FPGAs that only allow horizontal or vertical connections to nearby cells, the AT40K LUTs also allow connections to diagonal neighbors, thus providing eight-way connectivity *(Fig. 1b)*. Furthermore, on-chip distributed SRAM cells that offer single- or dual-port capabilities allow designers to efficiently locate blocks of SRAM anywhere on the chip. The FPGAs also have a fully PCI-compliant I/O capability, thus permitting the chips to serve in many of the PCI-based embedded systems as well as in specialty personal computer systems (industrial PCs and support boards, for example).

Atmel plans to offer five family members, the AT40K05, K10, K20, K30 and K40, that will offer a range of usable logic gates from 3000 to 10,000 for the K05 to 30,000 to 50,000 for the K40. SRAM bits included on the chips will start at 2048 on the K05 and increase to 4608, 8192, 12,800, and 18,432 bits on the K10, K20, K30, and K40, respectively. Maximum I/O pin counts range start at 128 and increase to 192, 256, 320 and 384, respectively. However, depending on the package selected for the chip, not all the I/O pads may be used.

Designed to operate from 5 V, the arrays have typical operating currents ranging from 15 to 170 mA; standby currents are well below 500 µA. A 3.3-V version with 5-V tolerant I/O lines and lower current consumption will be available the first quarter of 1998.

By taking advantage of the more efficient interconnects possible with the eight-sided LUT blocks, functions such as unpipelined multipliers can operate at speeds of up to 40 MHz, or two-dimensional 3-by-3 convolvers with FIFO buffers can be implemented with almost no routing, consuming just 700 cells of a 20-kgate AT40K20, and can operate at 40 MHz. The abundant cell-to-cell connections allow the logic cells to be connected orthogonally or diagonally to each other, making possible large multiplier arrays with little or no routing resource consumption, thus improving performance.

Groups of 16 logic cells, organized as a 4-by-4 cell mini-array, are called sectors, and each sector has 10 local and five express buses (in five planes), running horizontally and vertically. Express buses are staggered every two sectors so a cell has access to a total of 40 express buses and 20 local buses. Special circuits called repeaters are used to transfer signals between buses, and they are located at the bottom and side of each column or row of cells in each sector. Blocks of RAM are located at each corner of the sectors (one for every 4-by-4 block of logic cells), thus giving designers flexibility in localizing the memory near the logic *(Fig. 2)*. Direct cell-to-cell connections require no routing and incur no delay.

Each block of SRAM can be configured as single- or dual-ported (32 words by 4 bits) and provide designers with the resources to assemble SRAM blocks of any size or architecture. Furthermore, since the blocks are distributed across the chip, delays are minimal, enabling the implementation of high-speed LIFOs, FIFOs, and other memory blocks that are needed in real-time video and networking applications. Each bit in the dual-port memory array is formed with transparent latches, which simplifies the logic structure of the cell.

The flexible I/O cells on the chip provide designers with 28 different paths into the logic array. Each I/O pin can be directly connected to any one of three

DESIGN NOTES

The LTC1590: Applications Versatility of Dual 12-Bit DAC

Design Note 167

Kevin R. Hoskins

INTRODUCTION

CMOS multiplying digital-to-analog converters (MDACs) make versatile building blocks that go beyond their basic function of converting digital data into analog signals. This Design Note details some of the other circuits that are possible when using the LTC®1590 dual, serial 12-bit current output DAC. This DAC, shown in Figure 1, features:

- 2- and 4-Quadrant Multiplying Capability
- Outstanding INL and DNL: 0.1LSB Typ, 0.5LSB Max Over Temperature
- Low Supply Current: 10µA
- 3-Wire, Daisy-Chainable SPI Serial I/O
- Clear Input Resets DACs to Zero Scale
- Small Footprint: Narrow 16-Lead SO Package

The LTC1590 is designed for a wide range of applications, including process control and industrial automation, automatic test equipment, software controlled gain adjustment, digitally controlled filters and power supplies. This DAC is available in 16-lead narrow SO and PDIP packages.

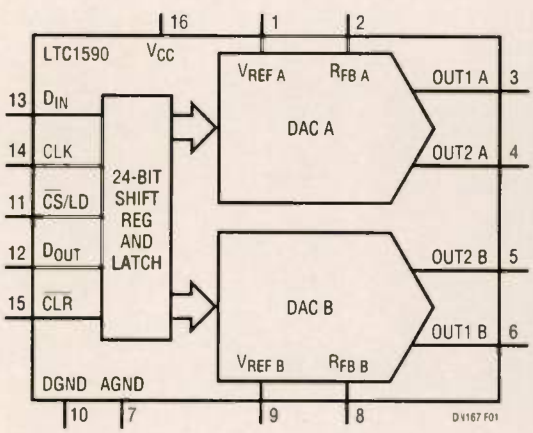


Figure 1. This Single-Supply, Dual 12-Bit DAC Features Serial Interface, ±10V Reference Input Range and a CLR Pin That Resets the Output to Zero

APPLICATIONS

Digitally Controlled Attenuator and PGA

The circuit shown in Figure 2 uses the LTC1590 to create a digitally controlled attenuator using DAC A, and a programmable gain amplifier (PGA) using DAC B. The attenuator's gain is set using the following equation:

$$V_{OUT} = -V_{IN}\frac{D}{2^n} = -V_{IN}\frac{D}{4096}$$

where:

V_{OUT} = output voltage
V_{IN} = input voltage
n = DAC resolution in bits
D = value of code applied to DAC

The attenuator's gain varies from 0 to –4095/4096 in 4096 steps. A code of 0 completely attenuates the input signal.

The PGA's gain is set using the following equation:

$$V_{OUT} = -V_{IN}\frac{2^n}{D} = -V_{IN}\frac{4096}{D}$$

where:

V_{OUT} = output voltage
V_{IN} = input voltage
n = DAC resolution in bits
D = value of code applied to DAC

The gain is adjustable from –4096/4095 to 4096 in 4095 steps. A code of 0 is meaningless, since this results in infinite gain and the amplifier operates open-loop. With either configuration, the attenuator's and PGA's gains are set with 12-bit accuracy.

Amplified Attenuator and Attenuated PGA

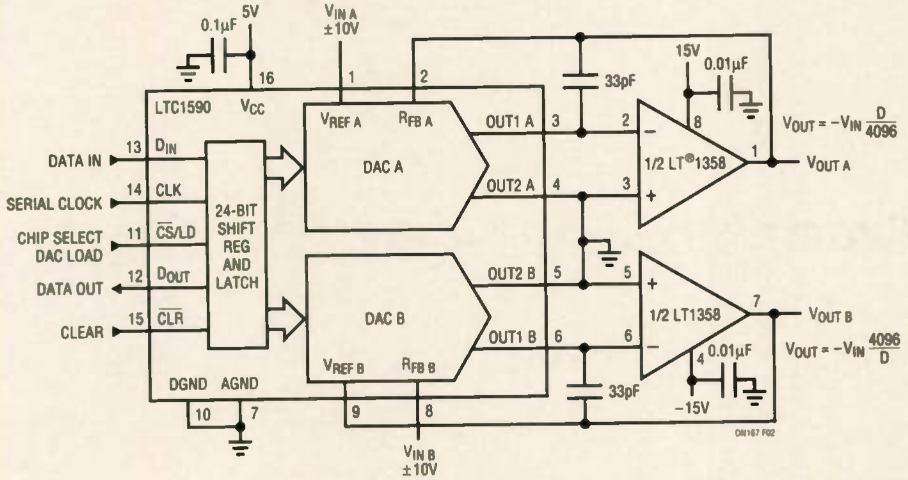
Further modification to the basic attenuator and PGA is shown in Figure 3. In this circuit, DAC A's attenuator circuit is modified to give the output amplifier a gain set by the tio of resistors R3 and R4. The equation for this attenu- or with output gain is:

$$V_{OUT} = -V_{IN}\frac{D}{2^n}\,\frac{R3 + R4}{R3} = -V_{IN}\frac{D}{256}$$

ith the values shown, the attenuator's gain has a range of to approximately −16. This range is easily modified by ıanging the ratio of R3 and R4. In the other half of the rcuit, an attenuator has been added to the input of DAC B, configured as a PGA. The equation for this PGA with input attenuation is:

$$V_{OUT} = -V_{IN}\frac{2^n}{D}\,\frac{R1}{R1 + R2} = -V_{IN}\frac{256}{D}$$

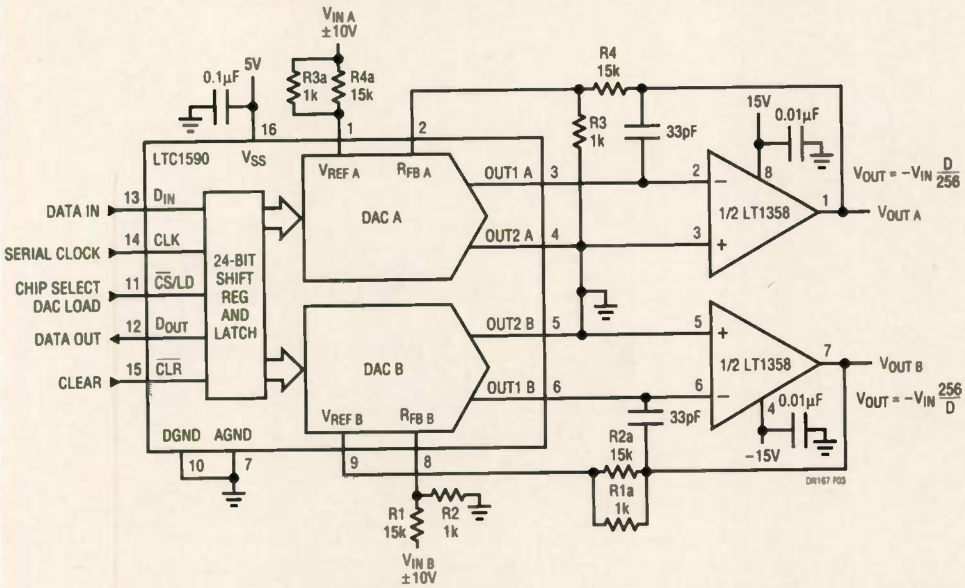
This sets the gain range from approximately −1/16 to −256. Again, a code of 0 is meaningless. This range can be modified by changing the ratio of R1 and R2.



DIN A	VOUT A/VIN A
0	0
1	−1/4096
4095	−4095/4096 ≈ −1

DIN B	VOUT B/VIN B
0	ILLEGAL: OP AMP IS OPEN LOOP
1	−4096
4095	−4096/4095 ≈ −1

Figure 2. The LTC1590's DACs are Configured as an Attenuator (DAC A) and a Programmable Gain Amplifier (DAC B), Each with a Range of 72dB



DIN A	VOUT A/VIN A
0	0
1	−1/256
256	−1
4095	−16(4095/4096) ≈ −16

DIN B	VOUT B/VIN B
0	ILLEGAL: OP AMP IS OPEN LOOP
1	−256
256	−1
4095	−(1/16)(4096/4095) ≈ −(1/16)

Figure 3. Minor Additions to Figure 1's Circuit Increase Its Flexibility by Adding Gain to the Attenuator (DAC A) and Attenuation to the PGA (DAC B)

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adjacent logic cells on the array edge, or signals can be routed directly to an express bus via any one of four signal repeaters. There are actually two types of I/O cells, primary and secondary.

Primary cells provide connections to the core cells and into repeaters on the row above and below the core cell. They have a programmable input delay, CMOS or TTL I/O levels, a pull-up or pull-down resistor, or can be configured with an open source/drain output. Secondary I/O cells connect on diagonals to the cell above and below the core cell accessed by the primary I/O cell. The secondary cell also connects to the repeater of the cell above and the cell below. Additional I/O cells in the corner of sectors increase access to usually underutilized corner core cells and are handy for very fast address decoding.

To support the AT40K family, Atmel has crafted a suite of electronic design automation tools in its FPGA Designer 5.0 tool set. The suite comes with over 20 fully characterized complex logic functions (blocks of intellectual property (IP)) that can be used as is or modified, as well as more than 50 automatic component generators (compilers) that can be used to create fully specified, reusable soft cores of many commonly needed functions. These soft cores can be "instantiated" by either VHDL or Verilog descriptions generated by behavioral design. Circuit designs synthesized by tools from Cadence, Mentor, Everest, Exemplar, ViewLogic, and Synopsys can be employed. Furthermore, the Designer 5.0 tool suite seamlessly ties into EDA tools from OrCAD, Data I/O, ViewLogic, Veribest, Cadence, Mentor, and Synopsys.

Price And Availability

The FPGA Designer 5.0 tool suite is now available and sells for $995. Samples of the AT40K20, a 20-kgate/8-kbit member of the family, are immediately available in 84-lead PLCC packages and sell for $58 each in lots of 1000 units. Package options for the family range from the 84-lead PLCC to BGA packages with over 400 contacts for the largest family members.

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TEXAS INSTRUMENTS

Automated BIST Solutions Arrive For Mixed-Signal ICs

Designers Can Add Built-In Self-Test For The Mixed-Signal Portions Of Their ICs. The First Circuits Covered Are ADCs and PLLs.

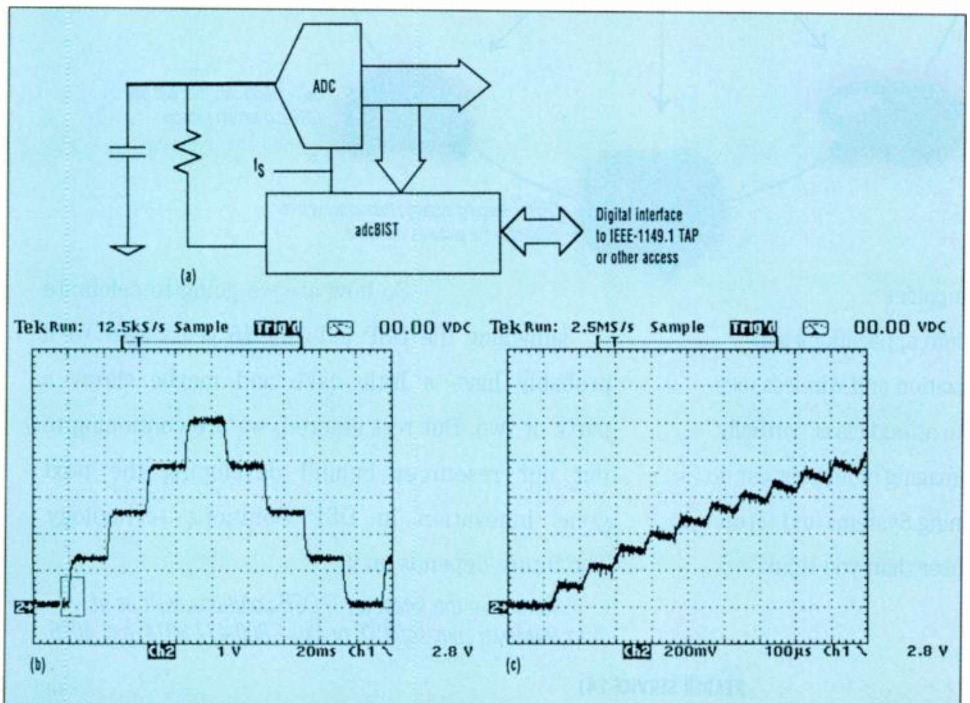
John Novellino

Automating the testing of analog circuits has, like its design counterpart, lagged behind automating digital testing. As more analog circuity ias added to digital ICs, this lack of automated analog test capability becomes a potentially serious problem. So the introduction of a solution for adding built-in self-test (BIST) to complex mixed-signal ASICs during the front end of the design process is a welcome addition to the designer's tool box.

The new tools, adcBIST and pllBIST from LogicVision Inc., target the most frequently used mixed-signal macros, ADCs and PLLs. The products consist of a combination of intellectual property (IP) and design services. The IP portions are delivered as synthesizable Verilog or VHDL RTL code suitable for automated layout. Implemented during the front end of IC design, adcBIST and pllBIST make the addition of BIST almost transparent to the designer, according to the company. The IP is backed up by design services that include application notes and consultation for customizing the BIST implementation. Customization may range from a single BIST implementation with various options and optimizations to a full-chip design-for-test methodology for both digital and mixed-signal circuitry.

The tools are aimed specifically at what's come to be known as "big D, little a" chips—complex ICs that are mostly digital with some analog thrown in. Test challenges these chips present include complexity that hinders access to the mixed-signal sections, problems caused by on-chip noise, and the lack of digital amenities like standard fault models, automated tools, and standard DFT methods. Also, digital testing is independent of the automated test equipment used while mixed-signal testing has been highly ATE-dependent.

Other techniques either in use or proposed for testing of mixed-signal ICs suffer from a number of problems, according to LogicVision. Disadvantages include too much overhead, either in gates or analog circuitry; no correlation to a functional specification; an affect on the chip's performance; and insufficient tolerance to process variations and noise. Also, they cannot be customized and may require changes to the analog design and resimulation. As a result, many companies say that 80% of the test effort is directed at the 20% of the chip that is analog.



1. The adcBIST circuitry connects to the ADC's input and output with no internal modifications needed (a). Together with the off-chip RC filter, the BIST circuit uses a digital algorithm to generate a full-swing analog stimulus (b). The 15-mV RMS noise on the stimulus appears as approximately 50 LSB peak-to-peak to a 12-bit ADC, but the BIST technique tolerates this level (c).

The adcBIST and pllBIST solutions use patented all-digital methods that fully test ADCs and PLLs at-speed. They're nonintrusive and avoid access problems by providing interfaces to an IEEE-1149.1 test access port (TAP). "Our mixed-signal BIST solution will revolutionize the test of mixed-signal circuits by overcoming the hurdles preventing high-quality testing today," says Robert Smith, Logic Vision's marketing and business development vice president. "We consider our all-digital approach to be industrial strength. By this I mean that we're offering an approach that is robust, tolerates noise, and is independent of process variations. It also delivers detailed in-

dependent diagnostics, and because it's digital, it's technology independent."

With adcBIST, designers can measure offset, gain, second- and third-order harmonic distortion, and idle-channel noise for comparison to test limits elsewhere, either on the chip, off the chip, or in ATE. This capability allows at-speed testing of fast ADCs on low-speed testers, and makes it easier to debug design and yield problems. The adcBIST circuitry is connected only to the input and output of the ADC under test. No changes or connections to the converter's internal nodes are needed.

Three levels of analysis capability are available to suit individual needs. The adcBIST-MN version supplies minimal on-chip circuitry for testing at high speed with intermediate results for simple off-chip calculations. This minimal version generates an analog stimulus for connection to the ADC through an on-chip multiplexer, but it may require an off-chip RC circuit for smoothing, depending on the clock rate, sample rate, and linearity *(Fig. 1)*. As it samples the stimulus, the ADC outputs the results to the adcBIST circuit, which processes it and sends six intermediate results to the TAP or other test-access circuit. Off-chip circuitry or ATE then calculates offset, gain, second- and third-order distortion, and idle-channel noise.

The next level, adcBIST-ST, includes all the MN circuitry. It also generates individual values for the same five measurements for comparison to test limits elsewhere on chip, off-chip, or in ATE. The highest analysis level, adcBIST-MX, adds the ability to compare the values to limits—which can be hard-coded on-chip or loaded in through the TAP controller—to determine a pass or fail.

The pllBIST product is a universal solution for analog and digital PLLs. It works with ATE that supplies a constant-frequency reference clock and low-speed control. Again, connection is only through the input and output of the PLL under test; no changes or connections to the internal nodes of the PLL are needed. A multiplexer is inserted in the reference-clock input path. The tool can test PLLs containing two-state phase comparators (for example, Exclusive-OR gates) or three-state comparators (for example, charge-pumps).

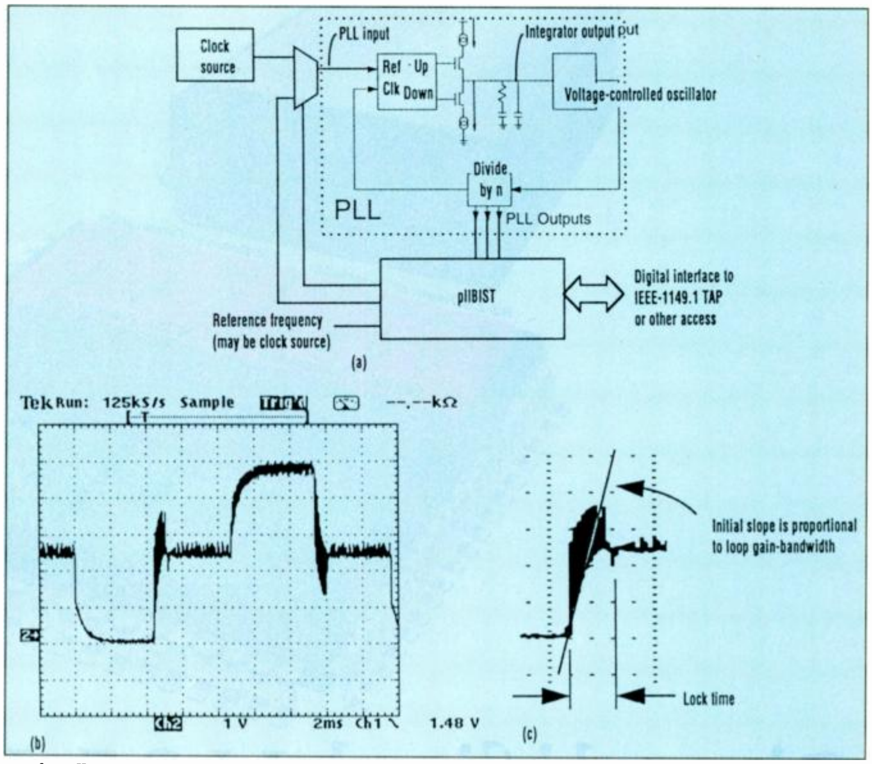
Users, again, have three levels of capability available. The pllBIST-MN version checks loop gain-bandwidth and frequency lock range. It multiplexes the external reference clock and a stimulus generated on-chip *(Fig. 2)*. If the PLL is data-driven, the data must be alternating ones and zeros. The loop's output, which consists of the voltage-controlled oscillator (VCO) frequency divided by two and other integer values if they exist, plus the lock indicator, are processed by pllBIST. Digital results for the loop gain-bandwidth and the upper and lower limits of the frequency lock range are output to an IEEE-1149.1 TAP or other access circuit.

To those capabilities, the next step up, pllBIST-ST, adds peak-to-peak and/or RMS jitter measurements. Users can load in the cumulative distribution function (CDF) limits for the jitter (0-100% for peak-to-peak, 16-84% for RMS) from off-chip or have them hard-wired on-chip. This feature allows the entire CDF to be measured. Capture and lock times also are measured.

At the top end, pllBIST-MX, like its ADC companion, compares the output values to limits to yield pass/fail results. Limits are loaded in at test time from off-chip or hard-wired on-chip.

LogicVision is developing a number of other mixed-signal BIST products. The company says the priorities and schedules for these products will be driven by market and customer needs.

Smith says the digital approach taken by LogicVision overcomes limitations of current mixed-signal test methods. The digital technique works with existing design tools, which are virtually all digital. Also, digital test patterns are easily portable across different testers, which saves time, and engineers can use their existing digital ATE rather than having to buy separate mixed-signal testers.



2. The pllBIST circuitry requires a multiplxer inserted in the reference clock's input path (a). An example measurement uses the analog waveform at the integrator's output (b). The lock-time and loop gain-bandwidth measurements are easily seen in the waveform's expanded view (c).

PRICE AND AVAILABILITY

The adcBIST and pllBIST products will be available in the first quarter of 1998. Prices for the IP and design services that make up the products are quoted based on the customer's specific test and design requirements and schedule.

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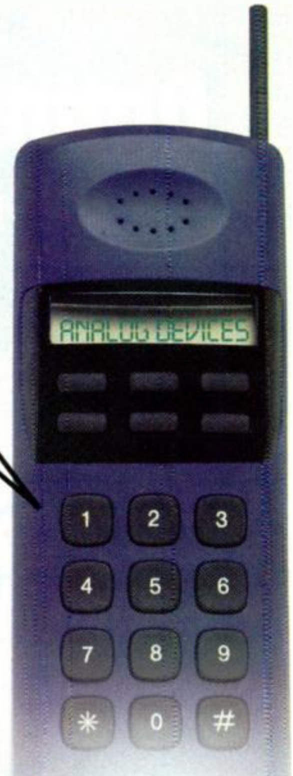

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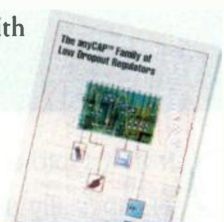

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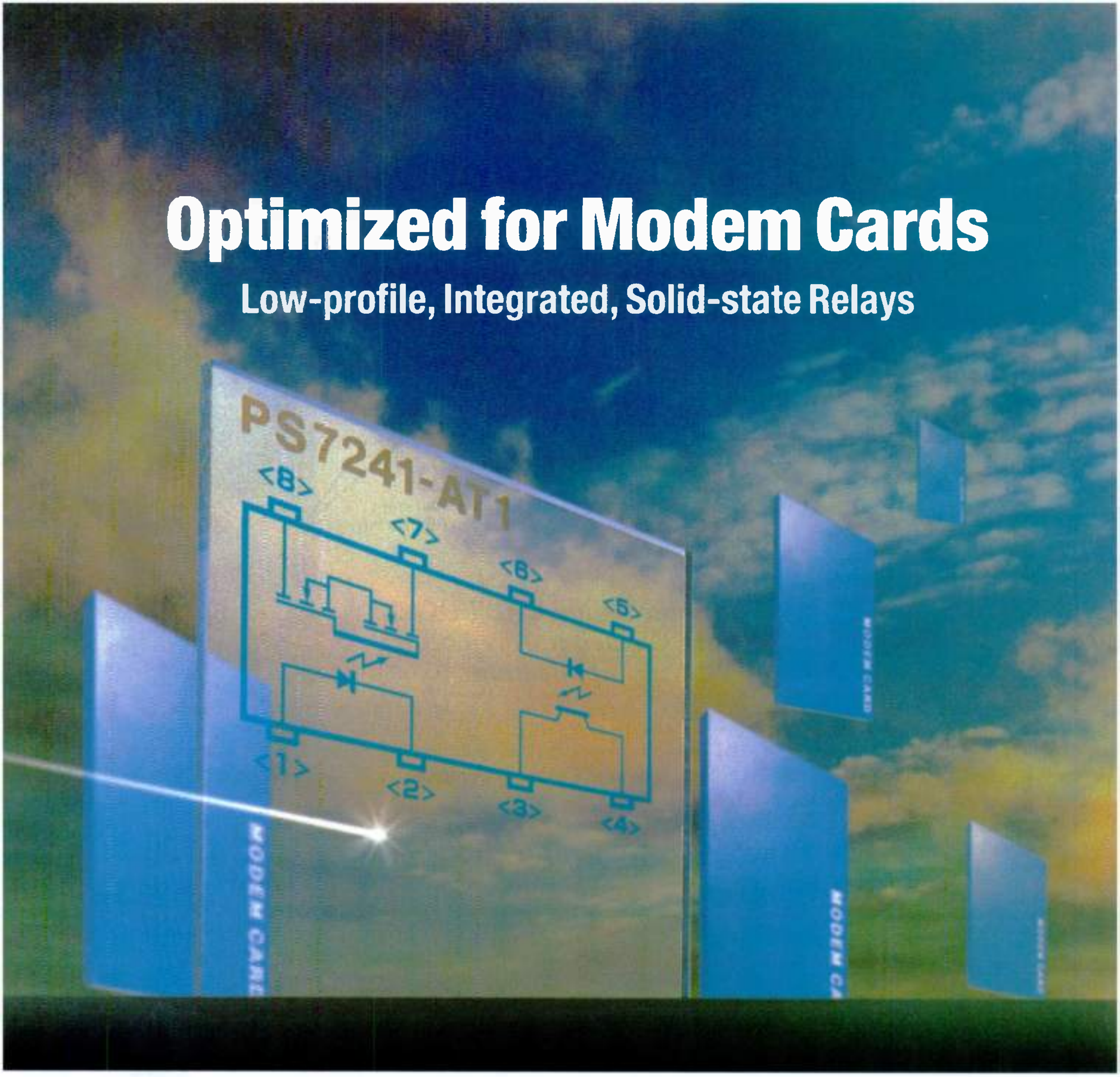

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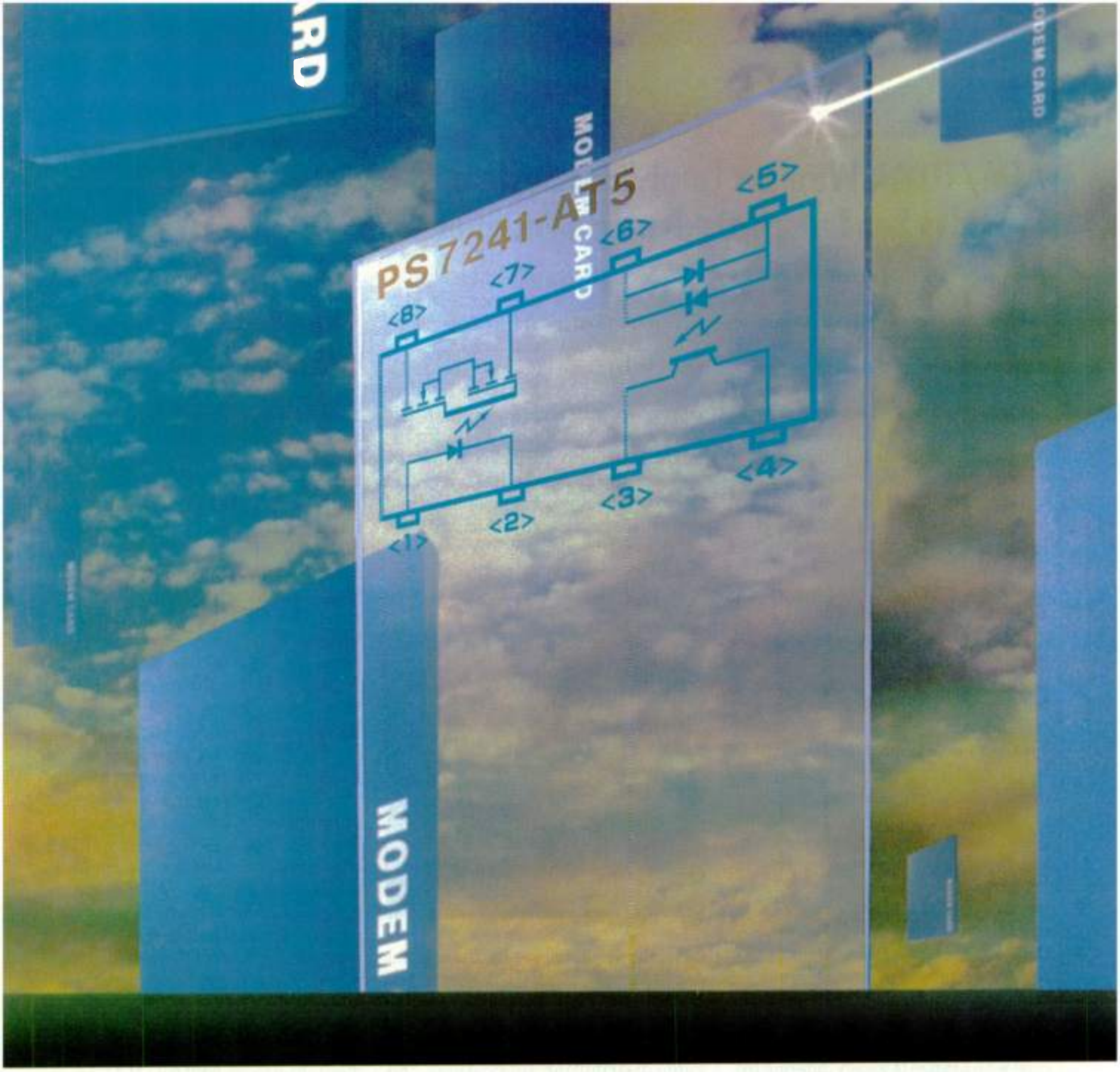

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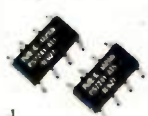

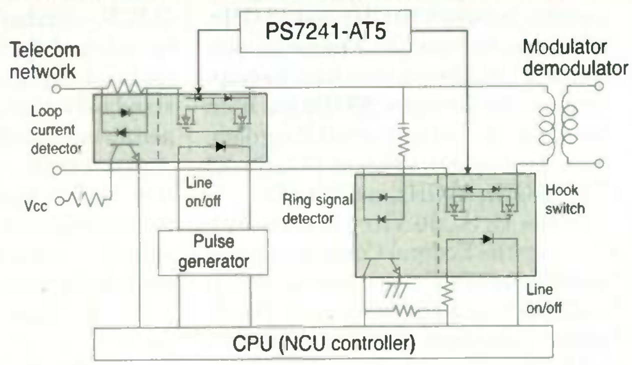

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UPDATE ON WIRELESS LOCAL LOOPS

ATM/TDMA Wireless Local-Loop System Provides Bandwidth-On-Demand Facilities

By combining asynchronous transfer mode (ATM) and time-division multiple-access (TDMA) technologies, Alcatel Telecom, Nanterre, France, and Stanford Telecom, Sunnyvale, Calif., have developed a point-to-multipoint, microwave wireless local-loop access system that provides true bandwidth-on-demand facilities. "It can provide telephone company customers with virtual dedicated data circuits equivalent to leased lines, at rates ranging from 64 kbits/s to 2 Mbits/s or more," according to Jérôme de Vitry, vice president for radio communications at Alcatel Telecom's Radio, Space and Defense Division. He claims the system—designated 9900 WW—will cost five times less than competing systems. It is tailored specifically for fixed-telecommunications network operators who need rapid deployment of broadband services to "high-end residential and small- and medium-enterprise" customers. It also is targeted toward PCS network operators who want to build high-capacity micro-cellular networks. Stanford is responsible for the ATM-TDMA signal-processing architecture while Alcatel developed the RF technology, and will handle systems integration and marketing.

The geographical diversity of potential buyers across North America and Europe means that the system must cope with a range of widely differing frequencies between 10 GHz and 42 GHz. In Europe, for example, France has settled on 28 GHz for wireless local-loop applications; in Germany, 26GHz has been chosen; while in the United Kingdom, there are opportunities at 17 GHz, 22 GHz, 26 GHz, 35 GHz, and 42 GHz.

In the U. S., de Vitry is watching closely as the Federal Communications Commission (FCC) prepares to auction frequencies for Local Microwave Distribution Systems (LMDS) applications, and for a new breed of telephone company known as Competitive Local Inter-exchange operators (CLIX). De-Vitry expects the LMDS auctions to start in December, and believes that LMDS operators will be bidding for frequencies at 31 GHz, while there is "some indication" that the spectrum around 28 GHz will be sold to the CLIX operators.

He claims that the new Alcatel system can be almost instantly reconfigured to cope with all of those frequencies and more, if necessary. Such a high degree of flexibility derives from the modular architecture chosen for the system, separating the RF subsystem from the signal-processing or baseband section. George Hendry, Stanford Telecom's vice president, Wireless Broadband Products, explains that the signal-processing system is designed to meet the standard set by the Digital Audio-Visual Council (DAVIC) and the European Telecommunications Standards Institute (ETSI).

> ...bandwidth allocation is managed by a MAC software package, which only provides service when a customer demands it...

"Although designed originally for video distribution applications, the DAVIC standard is ideal for almost any broadband application," he says. The main advantage of using the DAVIC standard is that it presents a fixed-rate and format interface to the radio section. As a result, the operating RF of the system can be changed without affecting the core signal-processing section. "It's simply a matter of changing the RF cards in the rack," de Vitry adds.

Yet another advantage of DAVIC ensures that customer terminal equipment—the "roof-top box" as de Vitry calls it—can be relatively inexpensive. He describes the roof-top terminal as "a box about the size of a pocket calculator with a 20-cm diameter antenna attached." The antenna is connected by cable to an internal modem unit that delivers services to the end user. The indoor unit effectively operates as a network bridge, providing an Ethernet or T1/E1 interface for data and/or voice. The unit can bridge up to 256 Ethernet addresses, "more than adequate for the average small business, teleworker, or technologically advanced family," claims Hendry.

The technology that Stanford Telecom has developed to allow variable and fixed bit-rate ATM traffic to be carried on a TDMA radio interface has taken three years of intense effort and the filing of 16 basic patents to bring to fruition. The system is designed so that one ATM cell is allocated to each TDMA time slot. Each cell comprises 53 bytes—47 bytes of information payload, a single byte sub-header and five bytes of header, to comply with the latest ATM Forum specification for access layer 5 (AL5). The design adds a few more bytes for additional header and framing data, to bring the total per time slot to 67 bytes. "That represents 35 µs per slot," Hendry says.

"The thing we are proud of is how we achieve ATM rates over the air," Hendry says. "We use several layers of encoding—convolution encoding and Reed-Solomon encoding followed by error correction and an inversion to achieve a bit-error rate of 10^{-10}—equivalent to that achieved in fixed networks," he adds. The real secret, though, is how the system can supply bandwidth on demand. That nugget is subject to 16 patents, and is highly proprietary.

What he did reveal is that bandwidth allocation is managed by a medium-access control (MAC) software package, which only provides service when a customer demands it on a transaction-by-transaction basis. When a service demand is made, a service request signal defining the nature of the subsequent transmission is sent to the hub station. The hub then allocates the customer's terminal just enough time slots to accomplish the task, and tells it which time slots it can use and when. The exception to this technique is voice telephony traffic. In this case, a virtual duplex channel will be allocated for the duration of the call.

Asymmetrical operation is achieved by treating the two parts of a conversation independently for time-slot allocation. This means that the circuit is only

occupied by a particular user for the minimum number of time slots required at any given instant. The extreme case for asymmetrical operation occurs when a user is browsing the Internet. That application generally means relatively large downloads that need to be received as fast as possible, with relatively long periods of inactivity. At the same time, traffic on the uplink is mostly limited to an occasional single mouse-click command. "Since a mouse click requires only two bits of data, the command will be sent along with the service request, effectively using no bandwidth at all," says Hendry.

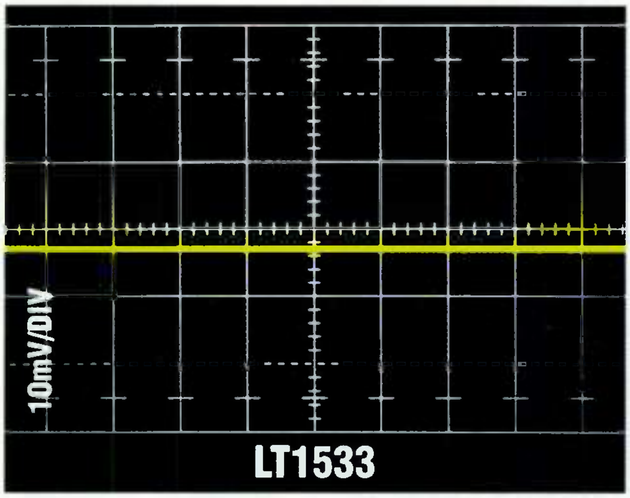
By contrast, with the high data rates and flexibility of the 9900 WW, competitive systems based on code-division multiple-access (CDMA) technology are able only to offer "plain ordinary telephone services plus ISDN basic rate," deVitry claims. "That is simply not sufficient for new operators who need to serve the most lucrative markets first and quickly," he asserts, pointing out that they must be able to provide broadband T1/E1 facilities or, at the very least, primary-rate ISDN connections to small businesses, and to what he defines as "TAFs"—technologically advanced families. To achieve fast and economic building of their new networks, these operators will need to use wireless local-loop (WLL) technology since they have neither the time nor the money to install fiber cables.

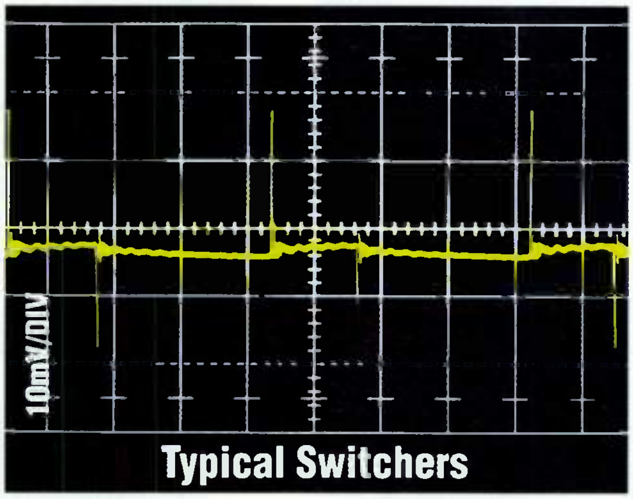
Both the new round of FCC auctions and the liberalization of Europe in January 1998 fit nicely with time scales for the new system. Presently, the new technology is just emerging from the laboratory and is in pilot trial phases of its development. Extensive field testing is expected to start with potential customers early in 1998, and volume production set to begin in late 1998 or early 1999. "This is new technology," de Vitry admits " and will require extensive trials to gain the confidence of purchasers and regulators alike."

For more information, contact Alcatel Telecom; Radio, Space, and Defense Division; 5, rue Noel-Pons; 92734 Nantere Cedex, France; +33 1 46 52 33 92; Internet: http://www.alcatel.com/radio, or Stanford Telecom, 1221 Crossman Ave., Sunnyvale, Calif., 94089-1117; Telephone (408) 745-2673; Internet: http://www.stelhq.com.

Peter Fletcher

100µV Output Noise Switching Regulator





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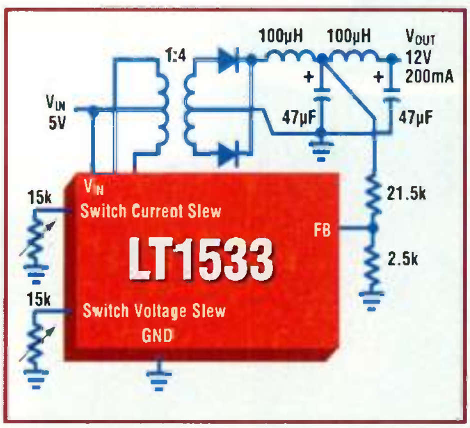

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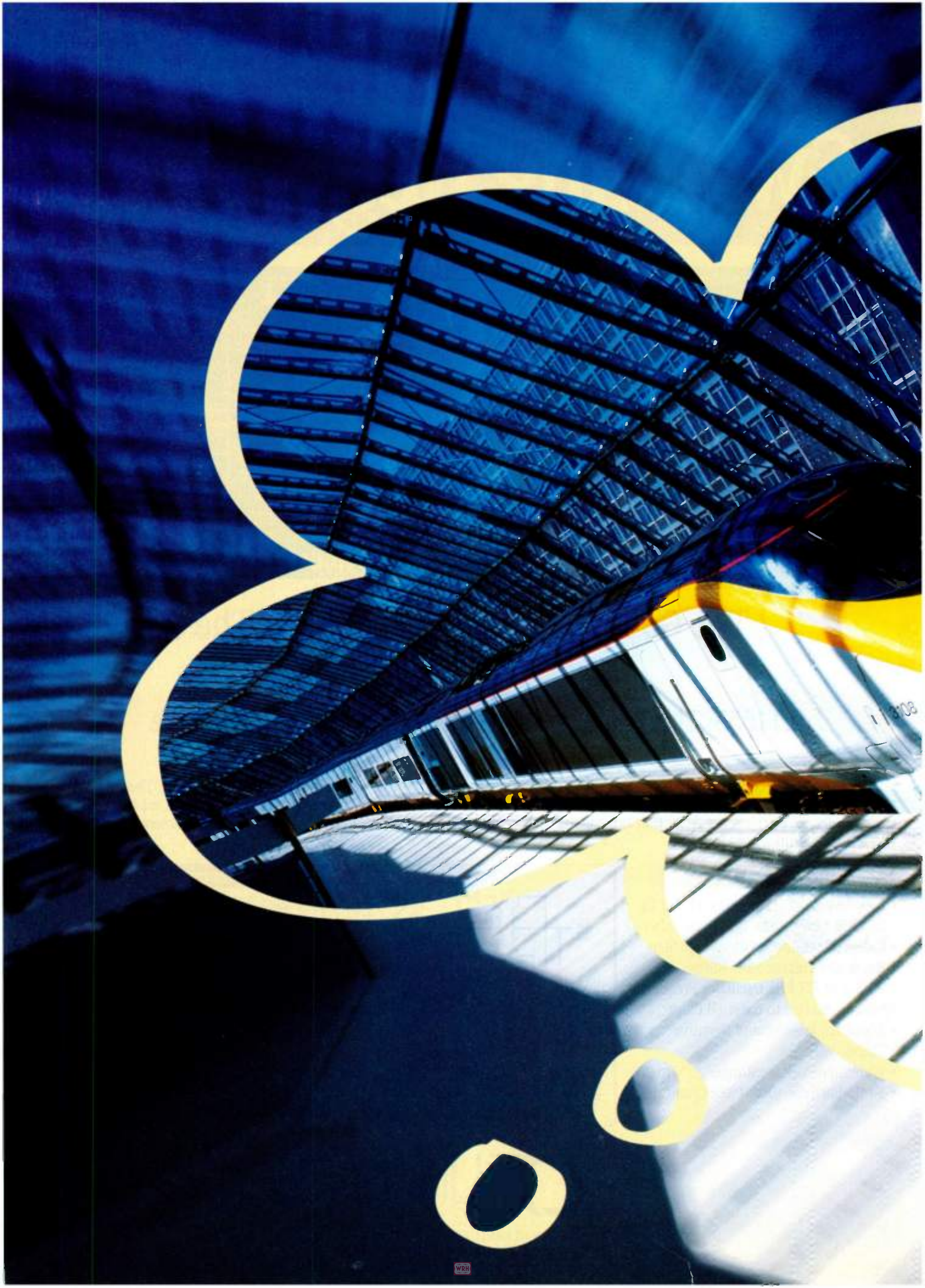
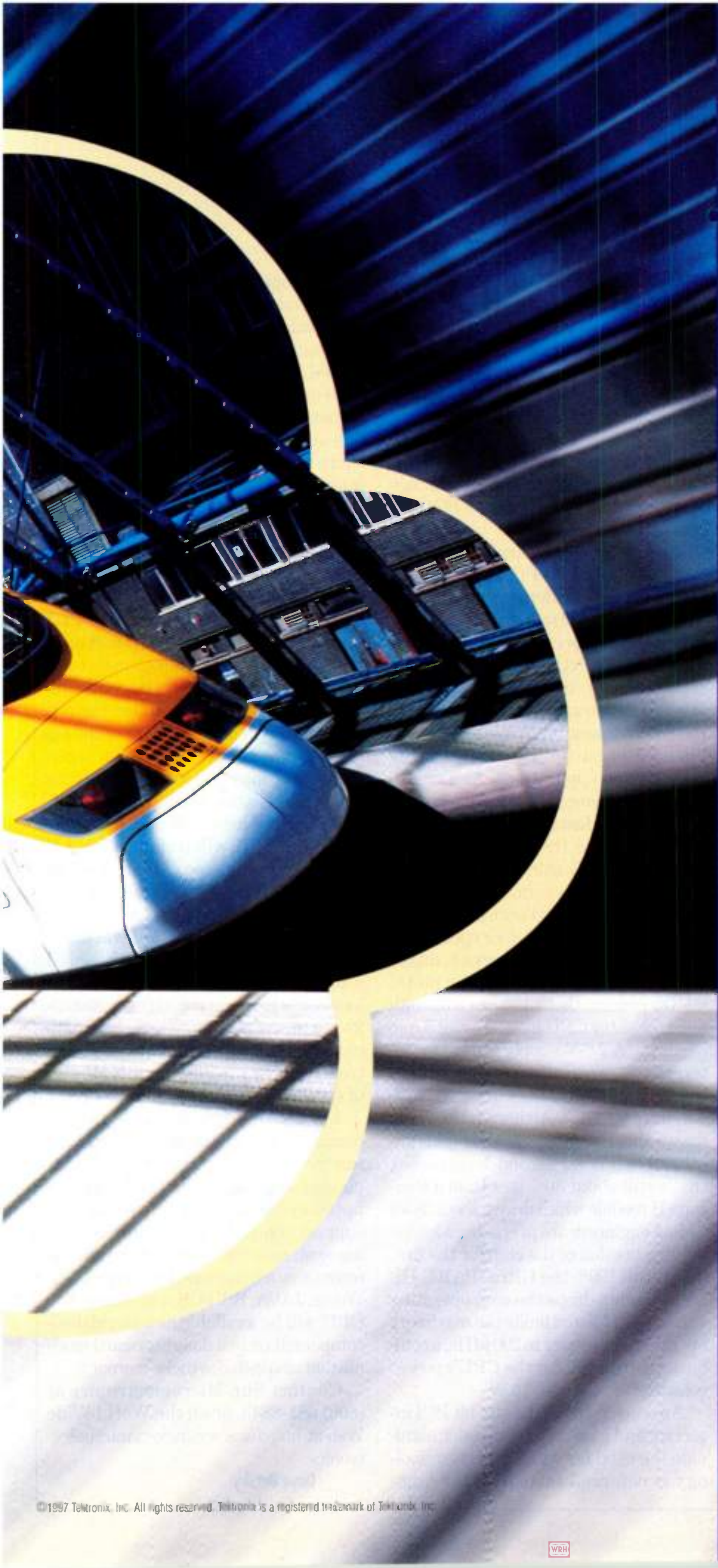




UPDATE ON UltraSPARC CPUs

PCI-Based UltraSPARC CPU Brings Down System Costs

The 64-bit RISC architecture of the UltraSPARC processor, already established as a high-performance engine for high-end Unix workstations and servers, will soon be recast to form the heart of PC-like Unix workstations and many other PCI-based systems. Designers at Sun Microelectronics are striving to reduce the cost of the processor, lower its power, and allow it to take advantage of the multitude of inexpensive PCI support chips and boards.

The forthcoming UltraSparc IIi will leverage standard PCI/PC building blocks while also offering the advanced features of the UltraSparc—a four-way superscalar processor core, 16-kbyte data and instruction caches, visual instruction set enhancements, 800-Mbyte/s data transfers, and support for the Solaris operating system, as well as binary compatibility with existing Sparc-based applications. As a result, CPU performance has been left uncompromised. Clocked at 300 MHz and using a 2-Mbyte cache, the UltraSparc IIi delivers a SPECint95 of 11.6 and a SPECfp95 of 15—significantly better than a Pentium II or Pentium Pro module running at a similar clock speed.

Lower chip cost and power is due to the use of a 0.25-µm, 5-layer metal CMOS process that squeezes a 5.5-million-transistor CPU into 12 by 12.5 mm of silicon. A 2.6-V supply is used for internal logic, while a 3.3-V supply powers the I/O buffers (I/O lines interface with 3.3- or 5-V logic). Although the CPU draws about 24 W at 300 MHz (plus another 4 to 5 W for second-level cache), that's still about 30% less than a Pentium II module which draws about 38 W.

Sun engineers are preparing a lower-voltage version of the chip for the first quarter of 1998, the UltraSPARC IIi-LV. This chip drops the core operating voltage by 10% and limits the maximum operating frequency to 200 MHz, a combination that will cut the CPU's power consumption to about 10 W.

An on-chip 33/66-MHz 32-bit PCI interface and a memory controller eliminate the need for what in PC terminology is referred to as North-bridge support logic. Supplementing the CPU is a second chip that provides advanced PCI bridge (APB) support and bus expansion if more PCI bus slots are required. The 33/66-MHz interface gives system designers a choice of various architectures by combining the CPU and one or more APBs. And, to improve Store operation performance, the PCI interface provides store compression, which gathers multiple stores into a single PCI write transaction.

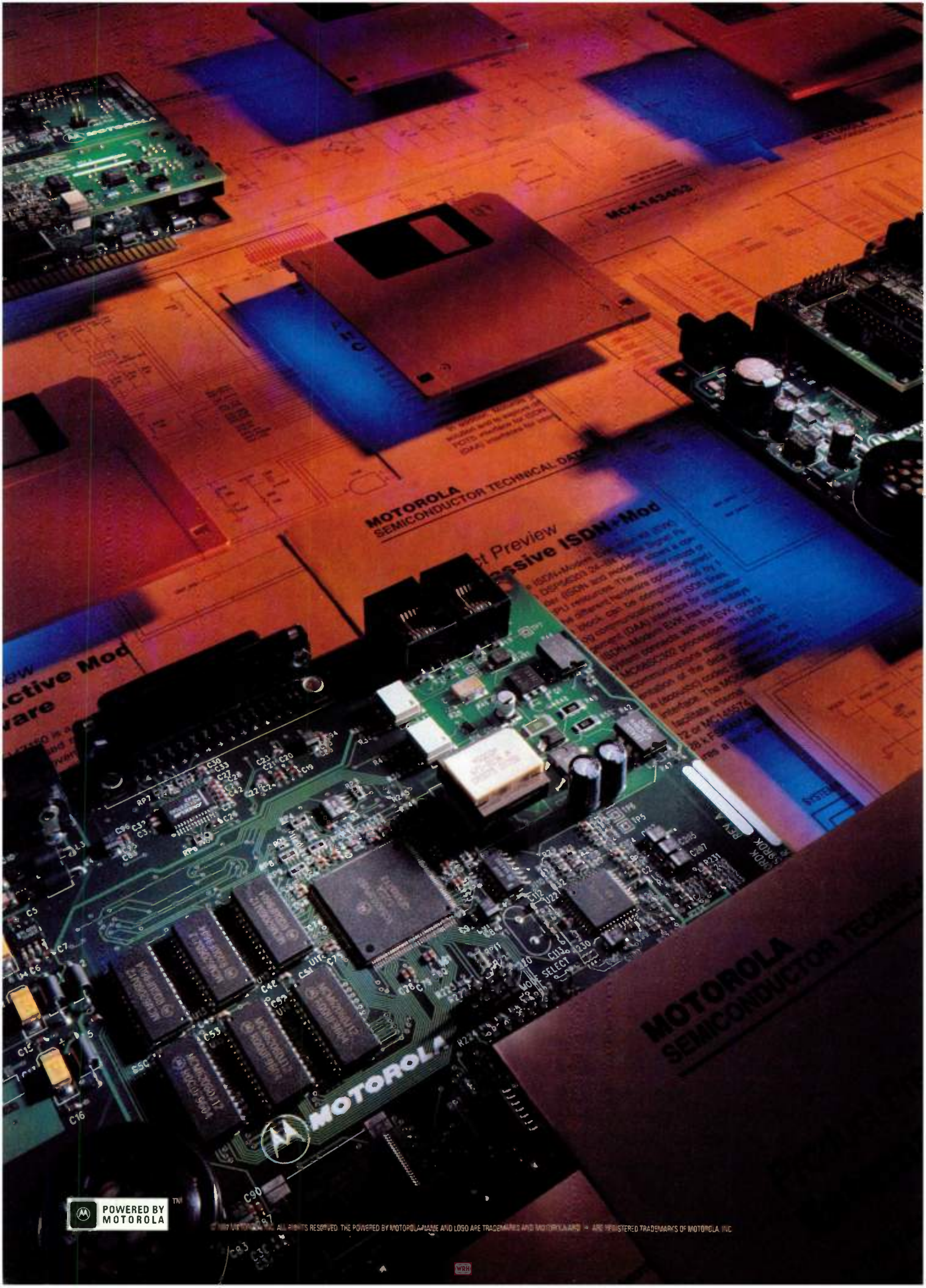
The APB chip converts the 33/66-MHz PCI bus into two independent 32-bit/33-MHz PCI buses, providing up to eight PCI slots. Each of those PCI buses, in turn, can be expanded once more with the APB chips, for up to 32 PCI slots—ideal for servers, communication control systems, and industrial applications. The ultra-port architecture I/O port also provides a high-speed 64-bit slave interface, transferring data at up to 6.4 Gbits/s (800 Mbytes/s).

For additional PC-like system operation, the CPU will include a DRAM controller and memory-management unit that performs 32-bit virtual address to 32-bit physical address translation and supports single-level hardware tablewalks. The MMU is based on a 16-entry fully-associative translation look-aside buffer and handles 8- and 64-kbyte (or mixed) page sizes. Also included is the second-level cache controller, which supports up to 2 Mbytes of synchronous SRAM.

For desktop applications (low-cost workstations/netstations), systems can run the Solaris operating system for application compatibility with other Sparc-based systems. Additional software support comes from real-time operating-system software from Chorus Systems (now a Sun-owned company), VxWorks, JAVA, BSD/OS, and others. The CPU will be available as a standalone component or in a daughter-card module that also includes cache memory.

Contact Sun Microelectronics at (800) 681-8845, or on the World Wide Web at http://www.sun.com/microelectronics.

Dave Bursky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PRODUCT FEATURE

Flash-Based Field-Programmable Gate-Array Family Adds 46 Kbits Of SRAM

For applications that require large amounts of on-chip static RAM for various system functions, there's a new family of FPGAs—the GFD260F series—that adds up to 46 kbits of static RAM storage onto logic arrays. The basic logic-array structure and configuration approach is the same as that in the company's previously released GF250F series—nonvolatile but reprogrammable flash/EPROM configuration elements controlling the connectivity of up to 310,000 equivalent gates of logic. However, the older family contains no SRAM, therefore it must use its logic cells to form blocks of RAM—a very inefficient approach for memory blocks of several hundred bits and larger.

Based on a 0.6-µm CMOS technology like the GF250F series, the GF260F family will initially contain up to 123 kgates (57 kgates usable, estimated), and up to 46 kbits of SRAM (organized in blocks of 256 words by 9 bits). The memory cells can be configured as synchronous or asynchronous SRAM blocks of almost any width or depth (including x9 for parity support), or as a FIFO or other memory function. The memory blocks in the GF260F series, though, are the only blocks among all of the FPGA suppliers that have integrated FIFO support as well as parity generation and checking logic.

Multiport memories with independent, simultaneous read and write operations also can be configured—from one read and write port up to 10 read and one write port (multiple writes aren't supported). Access and cycle times for the memory are less than 15 ns, which allows the memories to deliver synchronous or asynchronous operation at speeds of up to 67 MHz, while consuming about 8 µW/gate/MHz.

There will initially be three members in the GF260F family, the GF260F100, F180 and F310, which pack raw logic gate counts and SRAM capacities of 43 kgates/14 kbits, 92 kgates/23 kbits, and 123 kgates/46 kbits, respectively, and have typical logic-gate usage levels of just over 46%. The FPGAs also will offer maximum I/O pad counts of 248, 360, and 424 contacts, respectively, although lower-pin-count packages can be used to reduce cost. Current package options include a 391-lead ceramic pin grid array, metal quad flat packs with 208 or 304 leads, or the new shrink ball grid arrays packages with 352 and 560 contacts.

The design flow for the FPGAs is the same as designers would use with other gate-array design systems, allowing circuit entry with either HDL or schematic tools. The company also has its ProASIC library of preconfig-

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(continued from page 68)
ured logic functions from which designers can extract blocks to use in their designs. In addition to generic design partitioning, synthesis and optimization, and simulation and timing analysis tools, the tool suite includes a memory compiler for the SRAM, and FPGA-specific place and route software, and device programming software.

Samples of the GF260F180 are available now, with the GF260F100 and F310 expected out in the first and second quarters of 1998, respectively. When housed in a 560-contact eSBGA package, the GF260F180 sells for $599 apiece in quantities of 100 units. By the end of 1998, the company expects the chip price to drop to just $241 each in lots of 5000 units.

GateField Corp.
47100 Bayside Pkwy.
Fremont, CA 94538-9942
Peter Feist, (510) 623-4400
http://www.gatefield.com
CIRCLE 485
DAVE BURSKY

Speedy Field-Programmable Gate Arrays Feature Both Logic And Memory

Jumping into the high-density/high-speed corner of the FPGA market, QuickLogic took the wraps off its pASIC 3 family of high-speed FPGAs. These arrays offer the equivalent of up to 100,000 gates and 15 kbits of embedded SRAM. The QL3000 family members can operate at speeds of up to 275 MHz thanks to the use of 0.35-µm design rules and a four-level metal CMOS process that gives the FPGAs maximum performance and the smallest chip area for a CMOS implementation.

A second version of the family, the QL3000R series, includes all the features of the QL3000 chips, but also contains blocks of SRAM on-chip. The smallest array, the QL3012R, packs 12,000 gates and 10 blocks that contain a total of 5760 bits of storage, while the largest family member, the QL3100R packs 100,000 gates and 26 blocks totaling 14,976 bits. The RAM is divided into 576-bit, dual-port RAM modules that are individually configurable and easily cascadable. The blocks can be configured as synchronous or asynchronous, and single- or dual-ported.

The first chip to be sampled is the QL3025, a 25-kgate device with 1212 dedicated flip-flops, 204 I/O pads (maximum), and 8064 bits of RAM in the R version. Of the 204 I/O pads, 196 are bidirectional and PCI-compliant, four are high-drive input-only, and four are high-drive input/distributed network pins.

The distributed network pins have low skew—less than 0.5 ns—and are used to distribute clocks inside the array. Two of the inputs are array clock/control networks that feed signals to the logic-cell flip-flop clock, set, and reset inputs. The other two signal inputs are global clock/control net-
(continued on page 70)

(continued from page 69)

works available to the logic cell, clock, set, and reset inputs; the input and I/O register clock, reset, and enable inputs; and the output-enable control.

The chip area required by the logic is so small, thanks to the ViaLink antifuse technology and the four levels of metal interconnections, that the I/O pad ring had to be reduced to match the area of the logic. The resulting chips are 1/3 to 1/2 the area of SRAM-based devices, and thus will sell for considerably less.

To achieve the smaller area, designers at QuickLogic moved to a staggered pad ring approach that allows the same number of I/Os as a straight pad ring, but requires much less area. Thus, the QL3000 family can offer densities of 12,000 to 100,000 gates with I/O pin counts of 140 to 363 without the high silicon cost that in-line pad rings would result in. In addition, every member of the QL3000 and 3000R family includes full IEEE 1149.1 JTAG support to provide full scan- and boundary scan-path testability.

The logic and I/O cells in the pASIC 3 family are logically identical to the cells in the pASIC 2 family. They can implement a wide range of functions that operate at high speeds—typically at least 20% faster than the pASIC 2 series. Logic cells contain the equivalent of about 24 gates and can be configured with up to 16 inputs to deliver high-performance for wide combinatorial functions. Moreover, the cell can be configured to provide up to five independent logic elements, offering high device utilization when implementing multiple small logic structures.

Functions such as a 16-bit counter can operate at over 225 MHz, while datapaths can function at speeds of over 275 MHz. In addition, the pASIC 3 chips can implement a 33-MHz master or slave PCI bus that complies with the 2.1 version of the spec. The FPGAs operate from a 3.3-V supply but have I/O buffers that can operate in mixed 3.3/5-V systems as well as in 3.3-V-only systems.

Software support for the pASIC 3 family is available in three forms—the turnkey QuickWorks package provides a complete software solution from design entry to logic synthesis, to place-and-route, and to simulation. The QuickChip and QuickTools packages provide a solution for designers who use Cadence, Exemplar, Mentor, Synopsys, Synplicity, Viewlogic, Veribest, or other third-party tools for design entry, synthesis, or simulation. Tool enhancements provide higher-quality Verilog and VHDL synthesis, a drag-and-drop pin editor, and timing-driven place-and-route.

Samples of the QL3025 are immediately available, and the next member to be sampled will be the QL3060. Versions with embedded SRAM will be ready in mid-1998. In high volume, prices for the pASIC 3 family devices start at $8.90 for the QL3012. In 100-unit quantities, the QL3060 will sell for $84. The QuickChip tools are available free and can be downloaded from the

(continued on page 71)

(continued from page 70)

company's website. Also available on the web site is an On-Line Evaluator that allows designers to securely upload their Verilog and VHDL synthesis, perform the placement and routing, and view the results.

QuickLogic Corp.
1277 Orleans Dr.
Sunnyvale, CA 94089-1138
Don Faria, (408) 990-4000
http://www.quicklogic.com
CIRCLE 486
DAVE BURSKY

Skinnied-Down PowerPC Processor Favors Embedded Applications

By delivering a throughput of about 1.4 MIPS/MHz, the MPE603E offers designers of embedded systems four speed grades that provide speed/power/cost trade-offs to meet multiple system performance and price points. To retarget the 603 processor for embedded applications, designers at Motorola removed the floating-point unit to shrink the chip area and power consumption to that the chip can compete in the cost-sensitive embedded arena. However, the chip still packs dual 16-kbyte caches and dual MMUs that support 4 petabytes (252) of virtual memory and 4 Gbytes of physical memory.

With no other hardware changes, the MPE603E can run all software written for the PowerPC CPUs, except for the floating-point commands. If not executed directly, these commands will cause the CPU to trap and execute a subroutine to emulate the floating-point instructions. But, most embedded applications don't require floating-point computations, which falls in line with the applications the company has in mind—controlling network bridges and routers, network printers, RAID storage systems, etc.

Due to its reduced area, the 100-MHz CPU sells for just $20.69 each in lots of 10,000 units; the 133-MHz unit goes for $28.10, the 166-MHz version for $35.91, and the 200-MHz version for $44.50, all in similar quantities. At those clock speeds, the CPU delivers a throughput of 141, 188, 235, and 282 MIPS, respectively, but at significantly lower power consumption levels than the 603e.

The MPE603e can operate from a 2.5- or 3.3-V power supply and offers three power-savings modes: doze, nap, and sleep. All development tools for the previous 600-series processors can be used with MPE603e. Package options for the chip include a 240-lead ceramic QFP, and a 255-contact ceramic BGA. Samples are available immediately.

Motorola Inc.
6501 William Cannon Dr. West
Austin, TX 78735-8598
(800) 521-6274
http://www.mot.com/sps/powerpc
CIRCLE 487
DAVE BURSKY

High-Speed BiCMOS Field-Programmable Gate Arrays Handle 270-MHz Data Rates

An active repeater to speed signal movement coupled with a biCMOS process technology give the DL5000 family of field-programmable gate arrays the highest-performance to date for SRAM-based FPGAs. Developed by DynaChip, the DL5000 series supports clock and data rates of up to 270 MHz, and performs complex operations at clock rates of up to 200 MHz. The first devices in the family will be offered in complexities of 1250, 5000, and 10,000 gates, with the 5-kgate device the first to be sampled. Also in development is a CMOS family of FPGAs that the company expects to sample in early 1998.

The DL5000 FPGAs deliver the high speeds that advanced system logic demands for applications such as test systems, communications systems, graphics subsystems, and many others. To achieve the high speed, designers combined a fast 0.8-µm biCMOS process with a proprietary active repeater architecture that places active devices to rejuvenate signals at every connection. The horizontal wire lines contain two types of active elements—unidirectional repeaters called connection amplifiers, and the bidirectional Active Repeaters.. Most designs implemented in the DL5000 arrays will have no more than three Active Repeaters in the critical path, which translates to a worst-case net delay of just 3.3 ns or less.

The active repeaters thus eliminate many of the delays associated with pass-gate-based interconnects used in conventional FPGAs. While delays for wire nets with multiple pass gates in conventional FPGAs increase exponentially as additional connections are made, Active Repeater delays are purely linear. As a result, as fanout and net length increases, devices employing the Active Repeaters maintain their speed. For example, a 32-bit fully synchronous loadable counter can run at 140 MHz, a 4-by-4-bit multiplier runs at 170 MHz, an 8-bit fully synchronous loadable counter runs at 200 MHz, and a 24-bit adder/accumulator runs at 200 MHz.

The architecture of the DL5000 series FPGAs consists of logic blocks arranged in large, 5-by-7 block routing regions; each logic block contains the equivalent of about 20 gates. Connection buffers drive signals onto vertical and horizontal buses that connect every block in the routing region. Active Repeaters, distributed throughout the routing channels, connect different regions with worst-case delays as short as 1 ns, independent of fanout.

Input and output blocks provide ECL, PECL, and GTL interface levels at speeds of up to 300 MHz. A companion chip, the DT1000, allows the DL500 devices to communicate with slower system components at TTL levels. On the chip are six low-skew clock lines that keep skew to less than 250 ps. To ease testing, the chips include JTAG boundary-scan circuitry.

The 5000-gate DL5256 array is the first to be sampled. In 100-unit quantities , it sells for $281 apiece. The 1250-gate device will be sampled later this quarter, and the 10-kgate chip will be sampled in early 1998. Super-ball-grid-array packages with 204 contacts, or 208-pin ceramic PGAs will be used to house all three FPGAs in the DL5000 family. Power consumption depends on circuit configuration, but will typically be in the 4-to-6-W range when powered by a 5-V supply. To develop circuit configurations with the arrays, the company also created the DynaTool software, which supports Verilog and VHDL synthesis flows using the Synopsys and Exemplar design tools.

DynaChip Corp.
1255 Oakmead Pkwy.
Sunnyvale, CA 94086
Mike Ingster, (408) 481-3100
http://www.dynachip.com
CIRCLE 488
DAVE BURSKY

Low-Voltage 8-Bit Microcontroller Family Keeps Cycle Times Short

With operating voltages as low as 2 V, the KS88xx family of 8-bit microcontrollers offers designers up to 16 kbytes of one-time-programmable (OTP) EPROM or mask-programmed ROM. At the heart of the controller is an optimized SAM87 CPU core that employs a register-to-register architecture. There are 78 commands in the instruction set. The core includes both Idle and Stop modes, which can be used to reduce power drain. Instructions execute in just 750 ns when the CPU is clocked at 8 MHz.

The core was designed with modularity in mind and will be used as the basis for an "arrangeable" microcontroller family. The controllers in the KS88Cxxxx family provide designers with fast-turnaround, low-power devices that minimize the cost penalty versus ROM-based counterparts, as well as offer 100% electrical compatibility.

The first member of the family, the KS88P0916, packs 16 kbits of EPROM, 317 bytes of static RAM, multiple timer-counter functions (two 8-bit timers, a 16-bit counter-timer, and an 8-bit auto-reloading counter), three 8-bit I/O ports, and one 2-bit port. Also included on the controller are a watchdog timer and power-on-reset circuitry. Because the chip is the same size as its ROM counterpart, it will be available at a slight (10 to 20%) premium over the ROM part, rather than the typical 2X or 3X premium of many previous OTP controllers.

The controllers are specified for operation over a –20 to +85°C range and can be powered by 2-to-5.5-V supply for operation at a maximum clock speed of 4 MHz, and from 2.2 to 5.5 V for 6-MHz operation, and from 2.4 to 5.5-V for 8-MHz operation. In the stop mode, the chip draws just 1 mA.

Samples of the KS88P0916, available now, come in 32-lead SO plastic packages. In lots of 100,000 units, the OTP version sells for $1.64 each, while the mask-ROM version sells for $1.49 apiece in similar quantities. Bare chips also are available, as are versions with half the OTP EPROM or ROM. A *(continued on page 74)*

(continued from page 72)
suite of development tools, the SMDS II+ development system, provides support for all of the company's 4- and 8-bit MCUs.

Samsung Semiconductor Corp.
3655 N. First St.
San Jose, CA 95134-1713
Mike Erwin, (408) 954-7000
http://www.sec.samsung.com
CIRCLE 489
DAVE BURSKY

Tool Suite Makes It Possible To Develop PC-Based VME Control Software

The ability to upgrade and reconfigure VME-based control systems hardware without making fundamental changes to application software is made easier with a novel component suite. Users are able to create and maintain industrial control applications in either the ladder logic format familiar to PLC programmers, or by writing in C++. IOWorks lets PC-based control algorithms communicate with the underlying hardware via a software component that can access the VME bus and through board-specific drivers.

Control programs created with IOWorks can be linked to graphical user interfaces ,such as InTouch from Wonderware, Irvine, Calif., or to instrumentation programs, such as those from National Instruments, Austin, Texas. The latter include LabVIEW, ComponentWorks, and BridgeView. In fact, it can work with any product that can access a dynamic link library (DLL). Thus, most Intel architecture/VME-based embedded applications can be given a user interface or user monitoring and data collection capability that runs under WindowsNT. In addition, you can opt to run the control program on the host PC or download it to a single-board computer (just keep the user interface on the PC).

While IOWorks isn't limited to VMIC's own hardware, a basic set of components lets you access VMIC's products; a hardware toolkit is available for accessing third-party boards. The three base components are Visual IOWorks, IOWorks Manager, and Softlogic Link. The visual tool lets you create control programs using IEC-1131-3-compliant languages such as ladder logic diagrams, instruction lists, structured text, function blocks, and sequence charts. The visual tool can generate over 100 control algorithms such as lead/lag, PID, alarms, cutoff, math functions, coils, and contacts. It also supports user-defined libraries and functions.

An optional component, the C++ package, can translate the programs created with the visual tool into C++ source code. The Soft Logic Link component is a WindowsNT package that launches the appropriate compiler, builds the application, and downloads it to the target. The target system can be another Intel-based board running WindowsNT, or the real-time extensions to WindowsNT supplied by VenturComm, Cambridge, Mass. In that case, the same application compiled and run on the host PC, or parts of it, can be moved to a target board without modification.

Users always have the option of developing their programs completely or partially in C++. If the program is to run under WindowsNT, the Visual C++ may be used.If the targets is running one of the supported real-time operating systems—QNX or VxWorks—it needs to be recompiled with the appropriate compiler and reconfigured for the given board, but otherwise left unmodified. For QNX, the compiler would be Watcom and for VxWorks, it would be either the GNU compiler supplied by Wind River Systems, Alameda, Calif., or from Green Hills Software, Santa Barbara, Calif.

The Manager component of the basic component set manages the IOWorks environment. With Manager, you connect to specific targets, monitor the activity on those targets, and selectively download control program modules to various targets. From within the Manager, the event manager performs actions based on the occurrence of specified events. A number of events can trigger actions, such as data received, data changing, periodically occurring events, and error conditions.

When used with a graphical user interface package such as Wonderware's InTouch, or a virtual instrumentation system like National Instruments' LabVIEW, IOWorks adds a rich set of control loop capabilities. For example, a virtual instrument acquiring data from a system can be set up via dynamic data exchange (DDE) for use as inputs to the control program on the host PC. Using these additional products makes it possible to link the control logic, programmed as ladder logic or C++, to real-world-oriented control displays that contain representations of pumps, valves, tanks, motors, and the like.

Alternatively, that data can be sent from the host-based program to be used as input to the control loop running on another single-board computer. Additional graphical knobs, slider controls, and the like can be added to the instrumentation interface; these allow for user intervention in the control program. The transfer of data between programs is aided by the universal I/O controller (UIOC) component. In conjunction with the Manager, you set up dynamic data links with drag-and-drop. This means data can not only be shared with the embedded control program, but practically with any Windows application, such as Microsoft Excel.

VME Microsystems International
12090 South Memorial Parkway
Huntsville, AL 35803
(205) 880-0444
http://www.vmic.com
CIRCLE 490
TOM WILLIAMS

Low-Power Digital-Signal-Processor Engine Takes On Wireless Needs

Targeted at cost-sensitive applications ,the DSP16000 core and first product offshoot, the DSP16210, tackle issues of cost, performance, power consumption, and time-to- market to help simplify the design of wireless systems. The digital-signal-processor core includes a mixed 16- and 32-bit instruction set for high code density and can perform dual 32-bit accesses and two multiply-accumulates *(continued on page 76)*


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Clock Speed
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(continued from page 74)

in a single cycle. The 16-bit instructions are used to encode control operations and simple data moves, while the 32-bit commands encode complex instructions that exploit the features included in the core's architecture.

When clocked at 100 MHz, the chip can deliver a throughput of 100 MIPS or 200 million MAC operations per second (since one instruction contains two operations). An on-chip cache that holds up to 31 dual-MAC instructions helps reduce system power by minimizing accesses to the external memory, and a well-balanced register set offers good internal support for high-level-language code compilation. A 20-bit unified linear address space provides a comfortable code and data-storage space external to the chip. However, because the processor was designed with portable applications in mind, it can operate from power supplies as low as 2.7 V, and at that supply level draws 0.94 mA/MHz.

Specialized hardware to support communications-oriented applications make the processor core much more efficient at such applications—special Viterbi acceleration includes add-compare-select, and trace-back encoding, while on-the-fly saturation and rounding are controllable for bit-exact standards. In addition, a bank of eight accumulators help reduce memory accesses, thus lowering system power. Also, a more efficient multiplier design allowed engineers to embed two 16-by-16-bit multipliers and yet not consume more power than one of the previous 16-bit multipliers.

The first commercial chip based on the core is the DSP16210 and is targeted at multichannel speed coders and multichannel modems for wireless and wire-line systems. Included on the chip along with the core is a 60-kword by 16-bit dual-ported RAM, two-kbyte I/O RAMs to support fast DMA channels, a 4-kword boot ROM, and support logic for TDMA and timing. When clocked at 100 MHz, the chip packs enough performance to implement at least four complex speech coders (GSM, HR, or EFR) and many channels of error correction and equalization, or multiple V.34 modems.

Beyond the core and the first standalone offering, Lucent has developed a suite of development tools that include integrated C-language and DSP code source debugging software. Hardware breakpoints are available, and they can be extended to program and data memory access based on location or data value. In addition to source-code debugging, the company provides a patented system for architectural debug, which gives designers a schematic picture of the architecture. Consequently, programmers can see data move through the architecture as the DSP code is stepped, enabling them to observe saturation and rounding as it occurs. This scheme also lets programmers see parts of the architecture that aren't being used, and thus where optimizations might be possible. Communication to the chip is done over a 20-Mbit/s JTAG interface.

The DSP16210 will be sampled

(continued on page 78)

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Family Specifications*

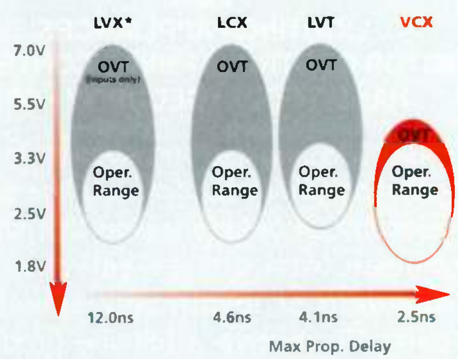
Power Supply (VCC)	1.8-3.6V
Drive (IOL/IOH) (min)	+/-24mA @ 3.0V VCC
	+/-18mA @ 2.3V VCC
	+/-6mA @ 1.8V VCC
Supply Current (ICC)	0.25μA
Speed* (TPD)	1.8ns @ 3.3V
	2.0ns @ 2.5V
	3.0ns @ 1.8V
Noise VOLP/VOLV	0.8/-0.8V @ 3.3V
	0.6/-0.6V @ 2.5V
	0.25/-0.25V @ 1.8V

Over-voltage Tolerance Specifications*

Input Leakage Current (II)	(0≤VI≤3.6V)	0.04μA
3-STATE Output Leakage (IOZ)	(0≤VO≤3.6V)	0.04μA
Power-Off Leakage Current (IOFF)	(VI or VO=3.6V)	0.25μA

* typical values represented

Fairchild *CROSSVOLT* Logic Families



* LVX 244, others 16244 function
OVT=Over-voltage Tolerance

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READER SERVICE 136

(continued from page 76)
later this year; in lots of 100,000 units, the chip will sell for about $50 apiece. ASIC designs using the DSP16000 core can be started immediately for production in 1998.

Lucent Technologies
Microelectronics Group
1247 Cedar Crest Blvd.
Allentown, PA 18103-6265
Robert Franzo, (610) 712-3521
http://www.lucent.com
CIRCLE 491
DAVE BURSKY

Cross-Development Tools Harness Commercial IDE For Embedded Arena

Many embedded-systems developers have longed for a visually integrated development environment (IDE) as rich and versatile as those used by their desktop and MIS colleagues. A number of embedded tool vendors have endeavored to meet these demands with products that could integrate tools and support cross development and debugging. Accelerated Technology has taken the approach of saying, "Why not take an existing IDE and soup it up to support embedded development?" The result is the POWERplant embedded development environment (EDE), which is based on the Microsoft Developer Studio.

Developer Studio is the IDE for all of Microsoft's development tools and resources, including Visual C++, J++, Visual BASIC, and other tools like CodeSafe. In addition to code-development tools, Developer Studio provides a project manager and editor. POWERplant EDE integrates those facilities with various cross compilers, debuggers, and other tools specific to the needs of embedded development. In addition, Developer Studio's browse and class manager also can be used for embedded projects.

To use the cross-development tools, first you create a make file. The output of the build process then is filtered and presented in Development Studio's build window. If errors occur during build, you click on the error and the source file associated with that error appears in the edit window with the cursor located at the line containing the error.

After completing the build process, you can invoke the debugger by clicking on a menu item that's been placed into Microsoft Developer Studio. Accelerated provides a registry configuration file that inserts the POWERplant toolbar into Microsoft Developer Studio and integrates with the tools menu. A copy of Developer Studio is included with the purchase of POWERplant EDE and the install wizard accomplishes the integration.

Accelerated Technology has designed its Nucleus plus real-time operating system to span a wide range of RISC, CISC, and DSP microprocessors. For quicker development of Nu-
(continued on page 80)

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READER SERVICE 242

(continued on page 78)
cleus plus-based applications on a WindowsNT platform, Accelerated provides an NT version of Nucleus plus called MNT. MNT runs as a WindowsNT process. All Nucleus tasks are created as WindowsNT threads and have equal NT priorities. MNT is responsible for priority and time-based scheduling of the tasks

You can compile, run, and debug a large portion of your embedded application in the workstation environment before cross-compiling it and getting down to the issues specific to the target environment. Using VNET—a networking prototype that also runs native on the PC—you can run several instances of MNT and have them communicate via shared memory or over a TCP/IP network. Versions of POWERplant EDE are available—along with appropriate compilers and debuggers—for the x86 real and protected mode, the 68xxx, PowerPC, i960, MIPS, SH, 29K, ARM, and Coldfire processors. Licenses are $1500 per seat.

Accelerated Technology
720 Circle Drive East
Mobile, AL 36609
(334) 661-5770
http://www.atinucleus.com
CIRCLE 492
TOM WILLIAMS

PC-Based Tool Environment Supports Distributed Development

A PC-based integrated development environment for embedded systems lets users manage projects and integrate third-party tools while working in small teams or on large, geographically dispersed projects. A copy of pRISM+ from Integrated Systems offers users a basic set of integrated tools for one of five different processor families, with support for additional families planned for the future. In addition to the basic tools, there are optional tools available from ISI as well as other tools provided by third-party partners.

Tools such as compilers, debuggers, code browsers, CASE tools, performance-analysis tools, etc., can be integrated into pRISM+ by being made compliant with the common object request broker architecture (CORBA) specification defined by the Object Management Group, Framingham, Mass. ISI has published the API to the pRISM+ communication server, which runs on the CORBA backplane, so that third-party tools can hook in to the same level as those supplied by ISI.

In addition, the environment maintains a symbol server attached to the object request broker (ORB) supplied by Iona Technologies, Dublin, Ireland. The symbol server maintains a repository of information that's available for all tools that require it. The ORB lets tools on the same machine communicate in the same way as tools on separate machines connected over a network. Access to target systems also takes place via the communication server.

The pRISM+ software is oriented toward ISI's pSOSystem scalable real-time operating system, whose kernel is called pSOS+, so projects using pRISM+ will most likely be using pSOS+ as their underlying RTOS. Because pSOS+ has many possible modules and setup options, there's a point-and-click Wizard that first offers several default pSOS+ configurations and lets you select operating system components for your application. It then checks for consistency and for any conflicts in the setup.

Once the underlying operating-system configuration has been completed, the main point of interaction with the environment is the pRISM+ Manager, a floating toolbar with icons for the various integrated tools. It's from this point where you launch tools. The tool manager also is the manager of the information repository. From the toolbar, you go to the project editor, which provides an overview of all project files and allows quick access.

The basic capabilities of the project manager can be extended with the optional Sniff+ tool. Sniff+ offers a more comprehensive programming environment that includes source browsing and graphical display of calling trees and code comprehension for reverse engineering and reuse. Any module in the tree display can be brought up into the editor by clicking on it. Sniff+ also offers document building, and automatic make/build facility, as well as a configuration-management and version-control capability. The version-control and configuration-management tools provided with Sniff+ can be replaced with other commercially available tools, such as ClearCase from Pure Atria, or PVCS from Intersolv.

The basic package of pRISM+ is delivered with the Wizard, pRISM+ Manager/toolbar, and a compiler and a debugger for the target processor. The debuggers are kernel-aware, and ISI is attempting to supply its own products for the basic package wherever possible. For example, ISI's Searchlight debugger is supplied for the MIPS platform package, while the SingleStep debugger from Software Development Systems, Oak Brook, Ill. is supplied for the 68000 platform. This doesn't preclude the use of third-party debuggers that are pRISM+ compliant if the user so desires. An ARM compiler and debugger are supplied for the ARM package.

Optional tools that can be ordered with the pRISM+ package direct from ISI include the Sniff+ tool, and the ESp and Object Browser analysis tools. ESp can be compared to a software logic analyzer. It presents an event-based sequence of action for analysis plotted along a time line. You can view which tasks are pending, blocked, running, waiting for data, and interrupts are active. Then you can view the timing relationship between them.

The Object Browser lets you monitor system behavior at specific time. It can take either manual or automat snapshots of any pSOSystem objec such as queues, memory regions, tasks, and capture their states. The data then can be used to graph object usage and behavior over time. For example, you could graphically monitor stack usage over time.

The initial releases of pRISM+ will support the PowerPC, MIPS, 68000, x86, and ARM processors with a complete suite of either ISI's own tools or third-party tools available from the company.

Integrated Systems Inc.
201 Moffett Park Dr.
Sunnyvale, CA 94089
(408) 542-1500
http://www.isi.com
CIRCLE 493
TOM WILLIAMS

Advertisement

LinearSolutions

Rail-to-Rail Op Amps

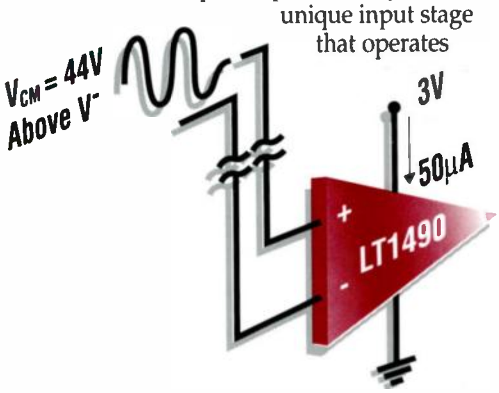
LINEAR TECHNOLOGY

August 1997

First Universal Micropower Rail-to-Rail Op Amp

The LT1490's 8-lead MSOP requires 50% less board space than an SO-8

The dual LT1490 and quad LT1491 op amps operate on all single and split supplies with a total voltage of 2V to 44V while drawing only 50µA of quiescent current per amplifier. They have a unique input stage that operates and remains high impedance when taken above the positive supply. The inputs take 44V both differential and common mode even when operating on a 3V supply. Unlike most micropower op amps, the LT1490/LT1491 can drive heavy loads; their rail-to-rail outputs drive 20mA.



Features:

- "Over the Top Input": Input Common Mode 44V Above V^-
- Single Supply Input Range: -0.4V to 44V
- Micropower: 50µA/Amplifier Max
- Reverse Battery Protection to 18V
- High CMRR: 84dB Min
- No Phase Reversal
- 8-Lead MSOP

Price: $1.95 ea/1K pcs
Packages:
Dual 8-Lead MSOP, SO, DIP
Quad 14-Lead SO, DIP

Suggested Further Reading on the Web:
DN134: Telephone Ring-Tone Generation
LT MAGAZINE: The LT1490/LT1491 Over-the-Top Dual and Quad Micropower Rail-to-Rail Amplifier, Feb '96 p.18

Circle No. 210

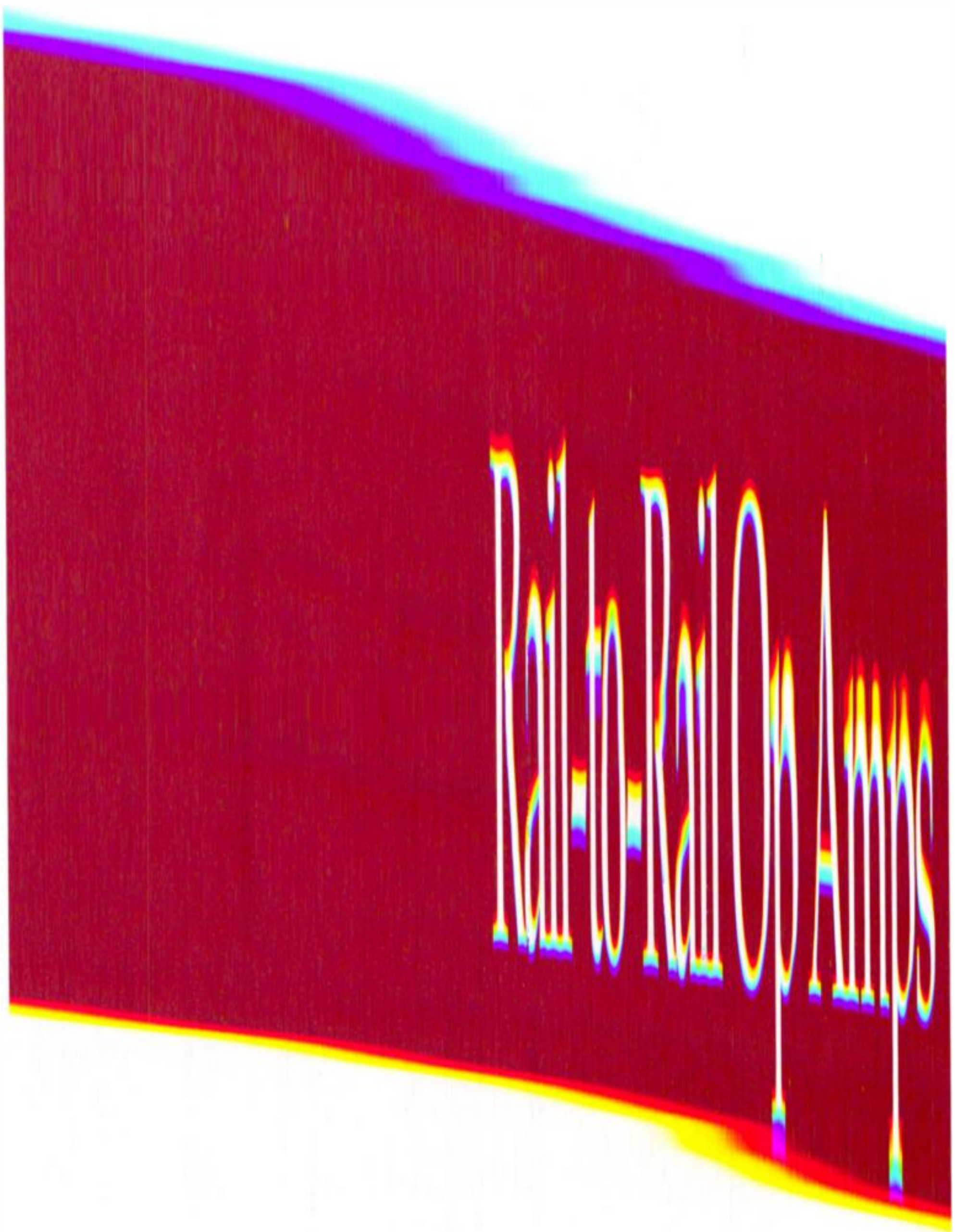
Rail-to-Rail Input & Output Amplifiers

			DC SPECS		AC SPECS			POWER SUPPLY SPECS		
SINGLE	DUAL	QUAD	V_{OS} Max µV	Drift Max µV/°C	CMRR Min Min dB	GBW kHz	SR V/µs	Is Max per Amplifier, µA	Supply Voltage (V) Min	Max
LTC1152			**10**	**0.01**	**115**	700	0.5	2.5mA/5µA*	2.7	14
LT1218L			**90**	3	**97**	300	0.1	420/30*	2.0	16
LT1219L			**90**	3	97	150	0.05	420/30*	2.0	16
	LT1495	LT1496	375	**2**	90	3	1 V/ms	**1.5**	2.2	36
	LT1490	LT1491	800	6	84	180	0.06	50	**2**	**44**
	LT1466L	LT1467L	390	7	83	120	0.04	**75**	2.3	16
	LT1366	LT1367	475	6	81	400	0.13	520	**1.8**	36
	LT1368	LT1369	475	6	81	160	0.065	520	**1.8**	36
	LT1498	LT1499	475	2.5	81	**10 MHz**	**6**	2.2 mA	2.2	36

* In Shutdown

In This Issue...

www.linear-tech.com



56-Year Operation on Two AA Batteries!

Drawing only 1.5µA of supply current, these 12-bit accurate op amps are ideal for battery powered instrumentation

For battery and sensor applications where supply current is paramount, the LT1495 dual and LT1496 quad rail-to-rail op amps furnish precision performance with minuscule power drain, 1.5µA max. Accuracy of the amplifier is not compromised by the current level: input offset voltage is 375µV maximum with maximum drift of 2µV/°C, input offset current is 100pA maximum. The devices also feature a unique input stage which allows operation with common mode voltages above the positive supply.

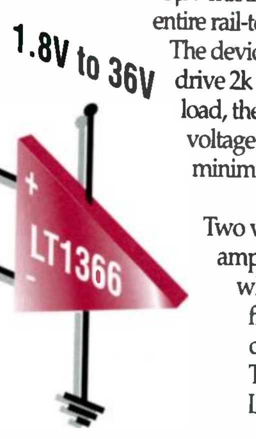
Features:
- Low Supply Current: 1.5µA Max
- Low Offset Voltage: 375µV Max
- Very Low V_{OS} Drift: 2µV/°C Max
- "Over The Top Input" Common Mode =10V at $V_S = 3V$
- Output Sources and Sinks 500µA Load Current
- Wide Supply Range: 2.2V to 36V

Price: $3.35 ea/1K pcs
Packages:
Dual 8-Lead SO, DIP
Quad 14-Lead SO, DIP

Circle No. 212

Precision Performance from 1.8V to 36V

Sense current with battery voltages as low as 1.8V



Operating over a wide 1.8V to 36V supply range, the LT1366 dual and LT1367 quad combine low offset voltage and high gain with rail-to-rail operation. Offset voltage is 475µV maximum across the entire rail-to-rail input range. The devices can easily drive 2k loads: with a 2k load, the open-loop voltage gain is 500V/mV minimum.

Two versions of the amplifier are offered which differ in frequency compensation. The LT1366 and LT1367 have conventional compensation, and are stable with load capacitances of 100pF or less. The LT1368 dual and LT1369 quad are compensated for use with a 0.1µF output capacitor which improves supply rejection and lowers output impedance at high frequencies.

Features:
- Wide Supply Range: 1.8V to 36V
- High A_{VOL}: 500V/mV Minimum Driving 2k Load
- Low Offset Voltage: 475µV Max
- High Common Mode Rejection Ratio: 81dB
- High Output Drive: 30mA

Price: $3.50 ea/1K pcs
Packages:
Dual 8-Lead SO, DIP
Quad 14-Lead SO

Suggested Further Reading:
DN89: Applications of the LT1366: Rail-to-Rail Amplifier
LT MAGAZINE: The LT1366 Family: Precision, Rail-to-Rail Bipolar Amplifier, Oct '94 p.13

Circle No. 214

LINEAR TECHNOLOGY

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Micropower, Guaranteed Low V_{OS} from Rail-to-Rail

Requiring only 75µA maximum per amplifier, the LT1466L dual and LT1467L quad deliver 12-bit accuracy from a 3V supply. Input offset voltage is only 390µV maximum across the entire rail-to-rail range and the minimum open-loop gain of 400V/mV into a 10k load virtually eliminates all gain error. Operating from supplies as low as 2.3V, the LT1466L/LT1467L are ideal for battery applications.

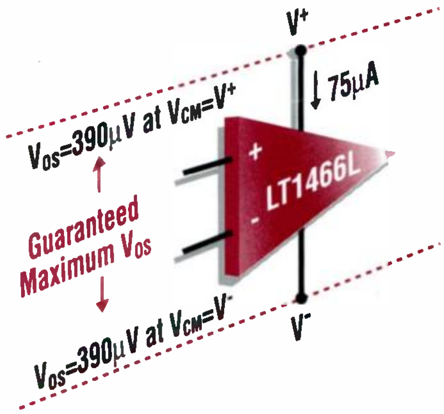
Features:
- Low Supply Current: 75µA Max
- 390µV V_{OS} Max for $V_{CM} = V^- \text{ to } V^+$
- High Common Mode Rejection Ratio: 83dB Min
- Low Input Offset Current: 3.6nA Max
- Wide Supply Range: 2.3V to 16V

Price: $4.15 ea/1K pcs
Packages:
Dual 8-Lead SO, DIP
Quad 16-Lead SO

Circle No. 216

Suggested Further Reading:
LT MAGAZINE: New Rail-to-Rail Amplifiers: Precision Performance from Micropower to High Speed, Dec. '96 P. 18.

The LT1466L/LT1467L ease design by guaranteeing a maximum V_{OS} value at both supply rails



The Highest Precision Op Amp. Period.

The LTC1152 has the best DC specs of any op amp with maximum 10µV offset voltage, 100nV/°C input offset voltage drift, 100pA input bias current and 115dB min CMRR. A high frequency onboard charge pump eliminates the crossover distortion and limited CMRR imposed by competing technologies. The LTC1152 also includes a shutdown feature which drops supply current to 5µA and puts the output stage in a high impedance state.

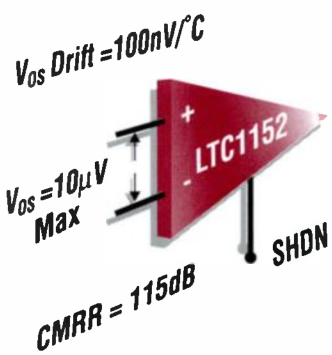
Features:
- Ultralow Input Offset Voltage: 10µV Max
- Ultralow Input Offset Drift: 100nV/°C Max
- Output Drives 1k Load
- Operates from 2.7V to 14V Total Supply Voltage

Price: $3.15 ea/1K pcs
Packages:
Single 8-Lead SO, DIP

Circle No. 218

Suggested Further Reading:
LT MAGAZINE: The LTC1152 Rail-to-Rail Operational Amplifier, June '94 p.3

Virtually error-free DC performance, very little drift over time and temp, and very low noise at low frequencies

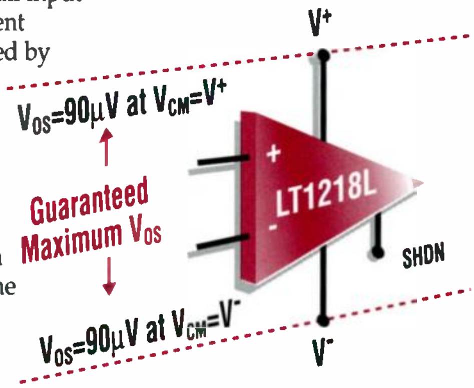


16-Bit Accuracy from Rail-to-Rail

90μV maximum offset voltage is guaranteed across *entire* input range

The LT1218L/LT1219L single op amps feature a low input offset voltage of 90μV maximum and 16-bit linearity (5V supply) over the entire rail-to-rail input range. The excellent linearity is obtained by using a patented technique, which trims the offset voltage twice, once for inputs at the positive supply, then again for the inputs at the negative supply.

The resulting common rejection of 97dB min is much better than competitive amplifiers.



Circle No. 220

Features:
- 90μV Max V_{OS} for $V_{CM}=V^-$ to V^+
- High Common Mode Rejection Ratio: 97dB Min
- Wide Supply Range: 2V to 16V
- Shutdown Mode: I_S<30μA

Price: $2.90 ea/1K pcs
Packages:
Single 8-Lead SO, DIP

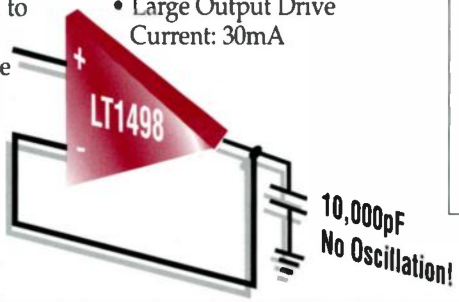
Suggested Further Reading:
LT MAGAZINE: New Rail-to-Rail Amplifiers: Precision Performance from Micropower to High Speed, Dec. '96 P. 18.

6V/μs, 10MHz Op Amp is Stable with10,000pF

With 110dB PSRR, the LT1498/LT1499 maintain performance over a supply range of 2.2V to 36V

Combining speed with DC precision, the LT1498 dual and LT1499 quad rail-to-rail amplifiers are ideal for low voltage signal conditioning. Used as a unity-gain buffer in a 3V 12-bit system, the LT1498/LT1499 are guaranteed to add less than 1LSB error. The devices have the ability to drive capacitive loads up to 10,000pF without oscillating, easing design requirements.

Features:
- 475μV Max V_{OS} for $V_{CM}=V^-$ to V^+
- Wide Gain-Bandwidth Product: 10MHz
- High Slew Rate: 6V/μs
- Low Supply Current per Amplifier: 2.2mA
- Large Output Drive Current: 30mA



Price: $3.80 ea/1K pcs
Package:
Dual 8-Lead SO, DIP
Quad 14-Lead SO

Suggested Further Reading:
DN50: High Frequency Amplifier Evaluation Board
LT MAGAZINE: New Rail-to-Rail Amplifiers: Precision Performance from Micropower to High Speed, Dec. '96 P. 18.

Circle No. 222

For more details, contact Linear Technology Corporation,
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LINEAR TECHNOLOGY
FROM YOUR MIND TO YOUR MARKET AND EVERYTHING IN BETWEEN

ELECTRONIC DESIGN QUICK LOOK

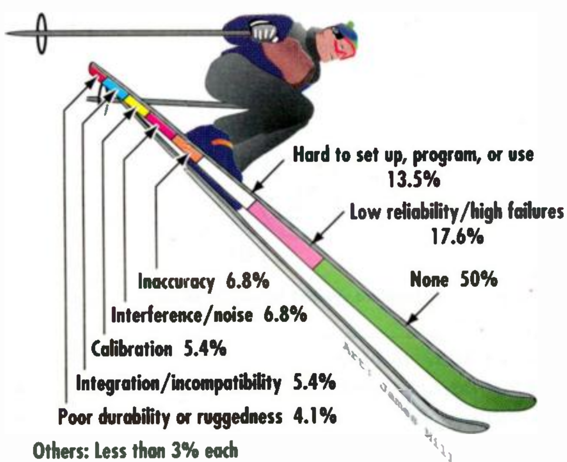
■ Edited by Mike Sciannamea and Debra Schiff

MARKET FACTS

Problems On The Slopes

Although one of the most popular tools in market analysis is the end-user poll, sometimes the results yield numbers that don't tell the story that the high-level executives like to hear. On the other hand, critical data that points to flaws in design or manufacturing can lead a company to retool and produce a different product that will be much more successful than originally intended. In the case of temperature controllers, companies in the field might want to talk to the professionals at Venture Development Corp. who've just released their "Worldwide Market For Industrial Electronic Temperature Controllers" study (2nd edition). The report is the result of a series of interviews done with OEMs and end users. The participants were asked about problems they had encountered with their industrial electronic temperature controller products and with the suppliers of those products. Other participants filled out a mail survey that asked the same questions. As seen in the figure, half of the end users and OEMs said that they weren't having any problems with the products they were currently using. The participants who did find problems with the electronic temperature controllers said that low reliability with high failure rates were the biggest problems. The second largest area of contention was in set up. Users complained that the products were too hard to set up, program, and use. According to Venture Development, that figure (13.5%) corresponds to another question in the survey that asked what the most important selection criterion was for the products. The answer was quality and reliability. What the study is telling vendors is that in order to compete in today's cutthroat market, they must invest more heavily in their quality, reliability, and ease-of-use features and manufacturing processes. Many participants also expressed a need for menu-driven displays and displays with prompt messages. Other problems (depicted in the figure) with these controllers were: inaccuracy, interference and noise, calibration, integration and incompatibility, and poor durability and ruggedness. Other issues that accounted for less than 3% were: inadequate autotuning, inadequate safety, poor serviceability, and slow response time. As far as vendor issues were concerned, the biggest problems were in delivery and availability (56.3%). Another strong message for vendors was the respondents' cry for better service and support (46.9%). It should be common sense by now for vendors of industrial electronic temperature controllers—better service and support equals more repeat customers. Other complaints include: poor product documentation (15.6%), lack of product knowledge by sales people (12.5%), and infrequent visits by sales people (9.4%). Issues that represented less than 6% each were: slow delivery of spare parts, poor application support, poor service support on obsolete models, and poor training for customers. In the study, however, the most identified "nonproduct" criterion for the selection of a particular vendor was price. But, according to Venture Development, high price was not identified as a problem by either the OEMs or the end users. The study provides in-depth analysis of market sizes, segmentations, and forecasts; users' needs; competitors; and strategies and recommendations. Regional and country market trends are related, also by industries and applications. Features such as packaging styles, autotuning, control modes, input and output capabilities, displays, accuracy, programming and adjustment methods, communication interfaces and networks, and temperature control ranges are studied in the report. Recommendations include: types and features, industries, geographical regions, and applications to target, and effective channels of distribution.

End User's Complaints With Industrial Electronic Temperature Controllers



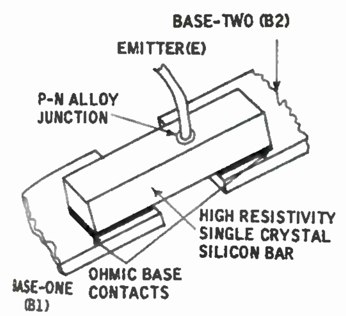
Source: Venture Development Corporation

For more information, contact Venture Development Corp., One Apple Hill, Natick, MA 01760-9904; (508) 653-9000; fax (508) 653-9836; e-mail: info@vdc-corp.com.—**DS**

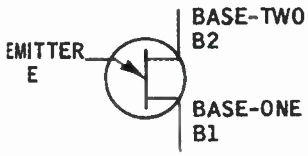
40 YEARS AGO IN ELECTRONIC DESIGN

Gas Thyratron Equivalent: Silicon Unijunction Transistor

Circuit simplification and stable negative resistance characteristics are outstanding features of new series of silicon unijunction transistors. Circuitry is such that any of the three terminals can be used as signal input or load output. The silicon unijunction transistor is a three-terminal semiconductor device which consists of an N-type silicon bar mounted between two ohmic base contacts, with a P-type emitter near base two. It has stable N-type negative resistance characteristics over a wide temperature range. Six standard types are available from the General Electric Co., Syracuse, N.Y., 2N489-2N494. In contrast to the conventional junction transistor, the unijunction transistor exhibits open circuit stable negative resistance characteristics. It is primarily useful in switching and oscillator applications. The unijunction transistor can be operated in a variety of circuit configurations such that any of the three terminals can serve as a signal input or a load output.



Construction of silicon unijunction transistor. The Silicon bar is a high resistivity, doped N-type single crystal.



Standard symbol for unijunction transistor.

The device operates by conductivity modulation of the silicon between the emitter and base one when the emitter is forward biased. In the cutoff or standby condition, the emitter and interbase power supplies establish potentials between the base contacts, and at the emitter, such that the emitter is back biased. If the emitter potential is increased sufficiently to overcome this bias, holes (minority carriers) are injected into the silicon bar. These holes are swept toward base one by the internal field. The increased charge concentration, due to these holes, decreases the resistance and hence decreases the internal voltage drop from the emitter to base one. The emitter current then increases regeneratively until it is limited by the emitter power supply. *(Electronic Design, Nov. 15, 1957, p. 113)*

The UJT was a versatile device, and for many years was a favorite of circuit designers in the "Ideas For Design" section.—**SS**

Ready for Sputnik

When Sputnik first crashed into world headlines, very few laboratories in the U.S. were prepared to receive the radio broadcasts from the Russian "moon." The Boulder Laboratories of the National Bureau of Standards was one of the first to set up a crash program to obtain information from Sputnik. According to Ralph J. Slutz, Chief of the Radio Propagation Physics Division, "The Russians have presented us with an unexpected gift in that their satellite is broadcasting on 20 and 40 mc." Boulder Labs was one of the few laboratories in the U.S. properly instrumented to study radio waves coming from the outer atmosphere at these frequencies. By studying the signals from the satellite, they expect to gain much knowledge about the amount of ionization the satellite is passing through and other characteristics of this ion media which are all important in radio transmission. *(Electronic Design, Nov. 15, 1957, p. 8)*

This was Electronic Design's first mention of Sputnik, launched the previous month. As noted before in this column, Sputnik had a profound effect in spurring renewed efforts in American technology and science education.—**SS**

JUST A REMINDER

It's now been over 30 days since we first introduced the First Annual QuickLook Paper Airplane Contest. So, are you working out your bugs, yet? You should be, because we're expecting to make our judgements just after January 1, 1998.

In case you forgot, or missed the last few issues of *Electronic Design*, we're interested in seeing how creative you can be with a paper airplane. And, of course, electronics. The basic premise is, "How many electronics can you fit onto a paper airplane and still have it fly?" That doesn't mean loading the thing up with useless electronics. The electronics have to DO something. Hopefully, something interesting.

1-800-Batteries

For the most creative paper airplane, we, in conjunction with 1-800-BATTERIES are giving a $150 gift certificate to be used with their catalog of batteries. Second prize is a $50 gift certificate, also to be used with the battery catalog. 1-800-BATTERIES also has donated 100 3-V lithium batteries to be given to the first 100 people who send in a self-addressed, stamped envelope (SASE) to our offices (listed below).

The rules are:

- All planes must be made of paper;
- Glue and paperclips are accepted;
- The plane must be fully assembled when we receive it;
- The wingspan can be no larger than 3 ft.;
- No smart-aleck "paper airplanes" that are really pieces of paper wrapped around consumer (or otherwise) electronics.

Entrants may send their SASEs to QuickLook Editors, *Electronic Design*, 611 Route 46 West, Hasbrouck Heights, NJ 07604. None of the airplanes will be returned, so take pictures before sending them off! Good Luck!—**DS**

New From Allegro

At 11, Elizabeth had already begun her mastery of motion control applications

Allegro Takes Command of Your Digital Microstepping Motor Control Applications

For over thirty years, Allegro has delivered the products that control the full range of motion better, more reliably, and more accurately than anyone else in the industry. Ranging from PWM closed loop current control to back-EMF sensing and 3 V operation, we put you in command of your motion control applications.

The New A3955 provides bi-directional pulse-width modulated (PWM) control

Our new A3955 motor driver IC continues our tradition of top performance and innovation. It is a full-bridge device which incorporates an on-chip 3-bit/8-level non-linear D/A converter and is optimized for the digital microstepping (eight-step) control of 2-phase bipolar stepper-motors.

The A3955 is capable of continuous output currents of up to +/-1.5 A, and operating voltages to 50 V. The internal D/A converter allows the current to be controlled in Full, Half, Quarter, and 8-microstep per step modes. The non-linear DAC minimizes the number of required digital control lines necessary for microstepping. Microstepping increases motor step resolution, reduces torque variations, and resonance problems at low speed.

Key features of the A3955 include:

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- Rated at up to 1.5 A and up to 50 V
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If there's a better way of dealing with tough motion control applications, Allegro will find it... and make it available to you. That's why you should call Allegro first because we're into motion control.

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READER SERVICE 118

TRUDEL TO FORM

JOHN D. TRUDEL
CONTRIBUTING EDITOR

How do we know if we're doing well in business? Most people would probably say if there is no problem, we don't need to do anything.

Many think business is just fine. Profits are good, the stock market is setting records, and, despite layoffs everywhere, the jobless rate is low. Part of this is how we count the numbers, but no matter.

Still, I think there is a consensus that most of the things we buy are built elsewhere. Because most products are built elsewhere, many U.S. firms, profitable or not, are losing their ability to innovate.

Increasingly, U.S. plants assemble products to which the value is added elsewhere. An amazing statistic is that as Oregon crossed over from timber to high-tech employment, the state's average wage actually dropped. Presumably, that is because so much of what we call "high tech" is foreign assembly plants. The result is, in essence and with some exceptions, a third-world economy: tourism, natural resources, and assembly plants.

These plants have mostly low-wage jobs and pay few taxes. They are used to modulating our trade numbers. The assemblies are imported, but the products shipped are counted as domestic, and perhaps even as exports, depending on where they go.

High-wage Japan calls such industrial hollowing *kudoka*. They see top management's job and the purpose of national economic policy is to resist it. They want to keep the value-added and high-wage jobs for themselves. Their business strategies are wrapped around a national policy of prosperity through exports. The Pacific Rim nations doing well at trade all use customized variations of the Japanese model, not ours.

Conversely, in the West, the CEO's job is seen as simple profit delivery. If he must, slash and burn the firm to produce profits; if people object, then that's just tough cookies. On top of this, our government takes an adversarial role with business, and it cares most about protecting low-wage jobs.

Our smartest trading partners are simply delighted to let us have what we want if we let them have the high ground. That is classic Sun Tzu strategy: "Always leave your enemy a path of retreat." If we resist, they can easily cause pain by removing what we want—low-wage jobs and short-term profits. They can dump products below cost or withhold key components. Just a few words can drop the stock market drastically, or even close a plant. If I were the CEO of a large firm, I might not dare oppose the patent sell-out in public, for fear of reprisals.

Think of global market flow as a river. If you go with the flow, you manage for "cheaper, faster," and cut R&D. Many will help you drift and wave as you pass, but the end of the ride is a low-profit wasteland.

Conversely, if you opt for innovation, you will be swimming upstream toward prosperity. The stakes are more than just corporate profits; they are societal affluence and world power. The cold war is over. What now matters is economic power, and its basis is found in technology. Nations once fought over trade routes and raw materials, but the battleground of the future is in intellectual property.

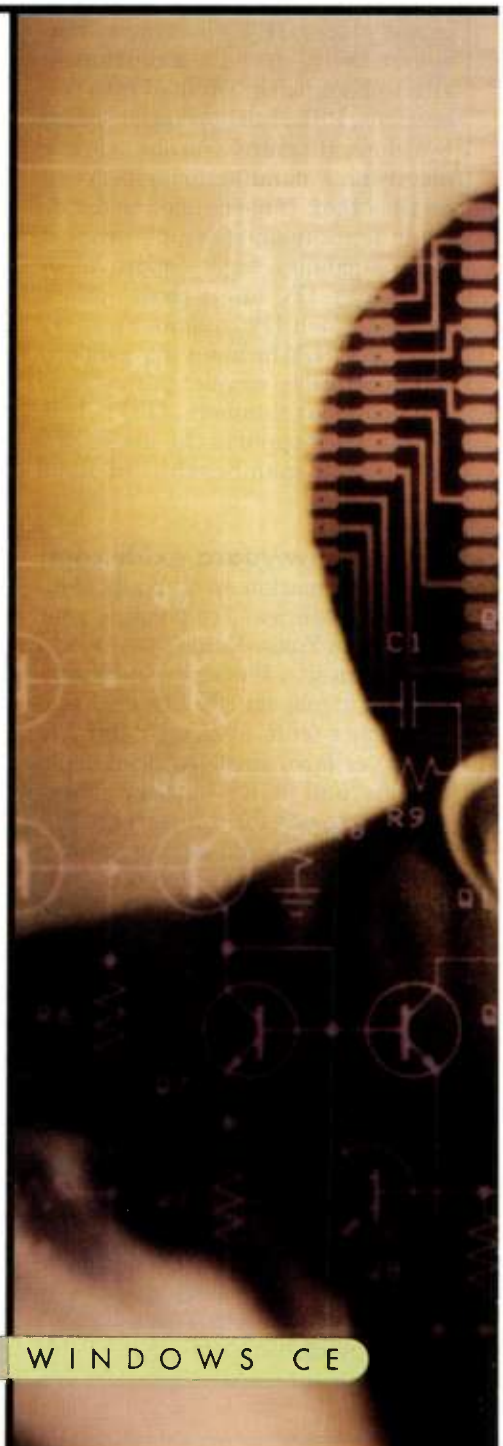
In the Information Age, both the river (market) and the boats (products) are mental constructs. That allows for limitless abundance. Successful innovators can not only invent unique jet boats to blow past competition; with luck, they can create their own rivers. Beating competitors is good, but making them irrelevant is much more profitable.

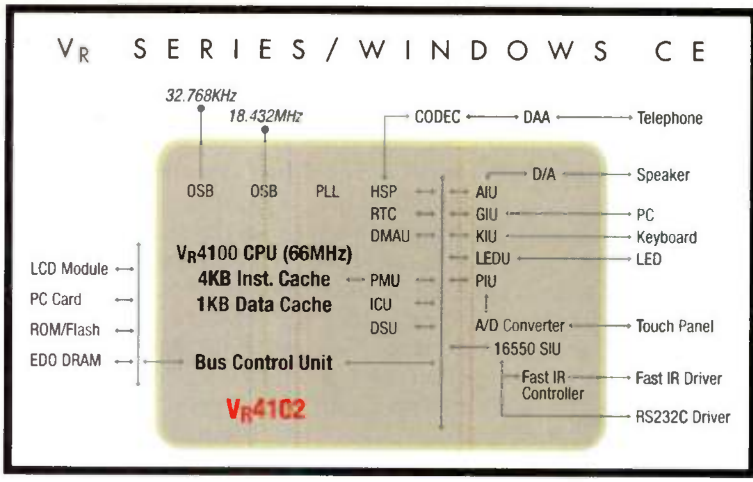
John D. Trudel, CMC, provides business innovation consulting to selected clients. Lectures, keynotes, and workshops also are available. He is the author of "High Tech with Low Risk." The Trudel Group, 33470 Chinook Pl., Scappoose, OR 97056; (503) 638-8644; fax (503) 543-6361; e-mail: jtrudel@gstis.net; Internet: http://www.trudelgroup.com.

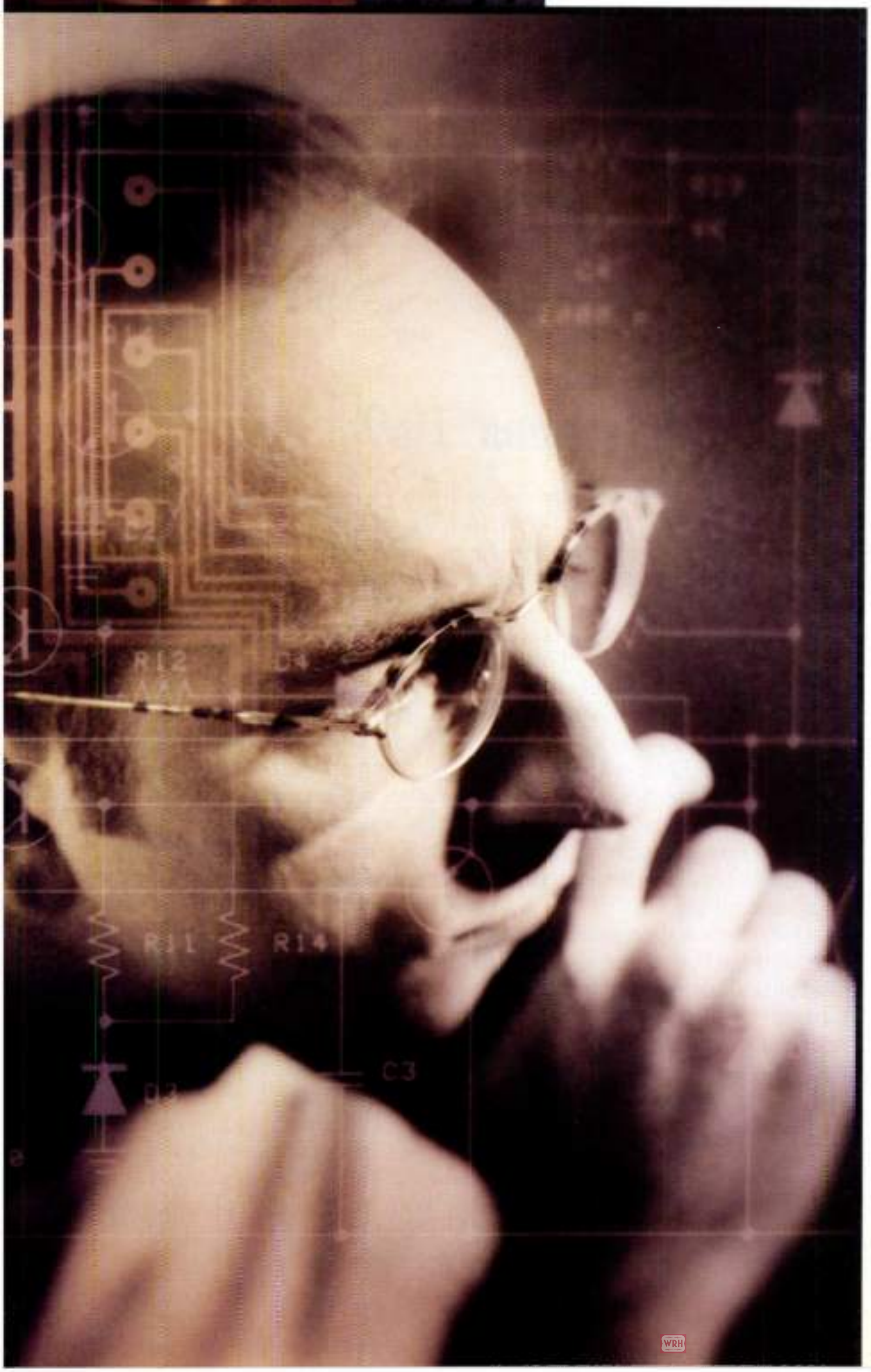
INTERNET ROLODEX

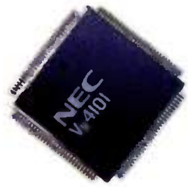
http://www.ipc.org: Stopping off at this URL will allow engineers and designers to use the Institute for Interconnecting and Packaging Electronic Circuits' (IPC's) brand new search tool, the Product and Service Locator Matrix (PSLM). IPC members who manufacture and assemble printed-circuit boards—electronics manufacturing services and/or printed wiring board providers and manufacturers—are all listed in one place. By gathering these sources all in one place, OEMs looking to outsource their jobs have a convenient site to bookmark. Divided into two sections, PSLM lists printed wiring board manufacturers on one side and electronics manufacturing services on the other. If users need to divide their searches further, by product type, capability, facility approval, or geography, IPC offers those options as well. Each IPC member's entry listed in PSLM includes the company name, address, contact person, and telephone/fax numbers. IPC is U.S. based, but supports the needs of a worldwide membership of 2300 companies.

http://www.yuasa-exide.com: Need information on all kinds of industrial batteries? Try pointing your browser to Yuasa-Exide's new World Wide Web site. Batteries and chargers for switchgear (flooded lead-acid batteries from 50 Ah to 400 Ah, VRLA cells for small footprint applications, and SCRF battery chargers); batteries for uninterruptible power supplies and back-up power for all applications (sealed rechargeables and valve regulated lead-acid batteries); batteries for security (NP line of sealed rechargeables); and power, batteries, and service for communications (all of the above plus EPIC and turnkey programs, and single-source units for dc power systems) are all featured at Yuasa-Exide's site. Surfers also can find batteries for small enginel. Some of these even include motorcycle and motor scooter batteries. Also, visitors to the site can find a comprehensive list of service locations, and direct e-mail access to Yuasa-Exide's support staff.



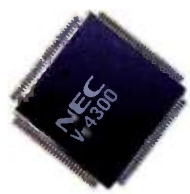






VR4101. Created for Windows CE products, it offers ultra low-power and incredible MIPS per Watt.

VR4102. Delivers Windows CE hand-held computer applications tremendous power and performance in a high-integration system on a chip.



VR4300. Ideal where high-performance and low-cost drive your design. Offers outstanding MIPS per dollar.

NEC

READER SERVICE 189

QUICKNEWS

A Congenial Network?—The FriendlyNet family of end-to-end intranetworking solutions from Asanté has now been expanded to include three Fast Ethernet hubs. These Fast Ethernet hubs are available in either five-, eight-, or 16-port versions. The FriendlyNet line is targeted toward small/home offices and businesses, and corporate workgroups.

Specific applications that could benefit from the speed of these new networking hubs include CAD/CAM, publishing, and medical imaging. All of Asanté's FriendlyNet Fast Ethernet hubs are compliant with the IEEE 802.3u standard. They feature uplink ports to simplify cascading multiple hubs or connection to an existing 100-Mbit/s segment with the use of a bridge or switch.

Responding to the need for space-saving devices, the three new Fast Ethernet hubs all feature small form factors. Wall-mountable, the five-port hub measures 8.8 in. by 4.4 in. by 1 in. The eight- and 16-port hubs are both 13 in. by 9 in. by 1.8 in. In addition, both the eight- and 16-port hubs can be rack-mounted.

The five-port Fast Ethernet hub is priced at $295; the eight-port hub goes for $579; and the 16-port hub carries a $1159 price tag.

For more information, contact Asanté, 821 Fox Lane, San Jose, CA 95131; (408) 435-8388; fax (408) 432-1117; Internet: http://www.asante.com.

Hi Ya!—The Samurai chip set from Micron Electronics brings the engineer 64-bit PCI on the Intel architecture, and supports 64-bit/66-MHz PCI. The new chip set is located within Micron's Powerdigm XSU, the high-power graphics workstation. The Powerdigm XSU is optimized for Windows NT Workstation 4.0. Currently, the Powerdigm system has been reduced $600.

The new chip set is able to sustain a data rate of 400 Mbytes/s. Samurai increases PCI bus master throughput by supporting lower latencies. Providing separate cache-line read and write buffers, Micron's chip set boasts memory subsystem support of up to 1 Gbyte of Sync-Dram and up to four Pentium II processors.

The demand for bandwidth is no problem with Micron's new chip set and workstation. The Powerdigm XSU, priced starting at $6199, is loaded to the hilt with all kinds of useful features from a 4 Gbyte Ultra-Wide SCSI-3 drive to the 3Com 3C905 PCI 10/100 Ethernet NIC. Also included are dual 200 MHz Pentium Pro processors.

For more information on the Samurai chip set, contact Micron Electronics, 900 E. Karcher Rd., Nampa, ID 83687; (208) 893-3434; fax (208) 893-3424; Internet: http://www.micronpc.com.

Bad Boys, Bad Boys, Whatcha Gonna' Do?

It may not be as exciting as watching criminals get arrested on "Cops," but there's a new application for wireless technology that may help to keep the bad guys off the streets.

Bell Atlantic NYNEX Mobile and the Charlotte-Mecklenburg, N.C., Police Department have recently announced plans to equip the local police fleet with the wireless data technology known as Cellular Digital Packet Data (CDPD).

Laptop computers using Bell Atlantic NYNEX Mobile AirBridge CDPD service will be installed in over 460 Charlotte-Mecklenburg police vehicles, including patrol cars, the mobile command post, SWAT vans, crime-scene vans, patrol boats, and canine-unit vehicles. The service will provide those officers in the field with nearly instantaneous wireless access to information before they approach a vehicle, house, or suspect. This will allow them to make the decision to deal with the situation either by themselves or to radio for assistance.

The AirBridge CDPD system gives field officers access to local, state, and national law enforcement databases to retrieve complete motor vehicle records, criminal warrants, police reports, and other information in just a few seconds.

"We believe in the value of technology in police work. When officers graduate from the police academy, they should be given a badge, a gun, a radio, and a laptop," says Charlotte-Mecklenburg Police Chief Dennis Nowicki. "This new technology will directly benefit local residents as well by enabling our officers to spend less time doing paperwork and more time in the community."

"Our wireless data service, known as AirBridge Packet Service, uses our existing cellular network. This capability provides police departments with a much more reliable, affordable, and versatile alternative to traditional two-way radios," says Jim Akerhielm, Bell Atlantic NYNEX Mobile's vice president for the Southeast Region. "There's no need to build more radio towers or be concerned with network maintenance or upgrades. Bell Atlantic NYNEX Mobile takes full responsibility for maintaining and upgrading the system."

The software that allows officers to connect to national, state, and federal databases, police information systems, the National Crime Information Computer, and the N.C. Division of Motor Vehicles is being provided by Cerulean Technology Inc. of Marlborough, Mass. Akerhielm adds that his company is interested in working with other police departments throughout the country that may be interested in using wireless data technology.

In addition to saving time, the mobile computer systems were designed to help increase the security of police department communications. Sensitive messages are encrypted or scrambled by both the software and the CDPD network to prevent unauthorized reception.

For additional information on the CDPD technology and its potential uses, readers may contact Bell Atlantic NYNEX Mobile on the World Wide Web at http://www.banm.com, or Cerulean Technology at http://www.cerulean.com.—MS

"Stop Noise Two Ways"

Most people know that a pacifier will stop noise, sometimes very quickly, other times it takes a little longer. The method, however, works. Add a little sweetness and it works even faster. And for certain applications the pacifiers come in different shapes and sizes.

Conec Filter Connectors stop noise as well. Noise created by EMI/RFI in today's high speed digital systems. And just like pacifiers, Conec Filter Connectors come in different configurations - industry standard d-sub, high density d-sub, filltered adapters, modular jacks and combo d-sub, with power filtering and signal filtering. We don't add any sweeteners. What we do add is our patented planar filters. The technology with a proven track record, combined with the industry's best connectors—ours. Both technologies fully integrated, for best results in filtering.

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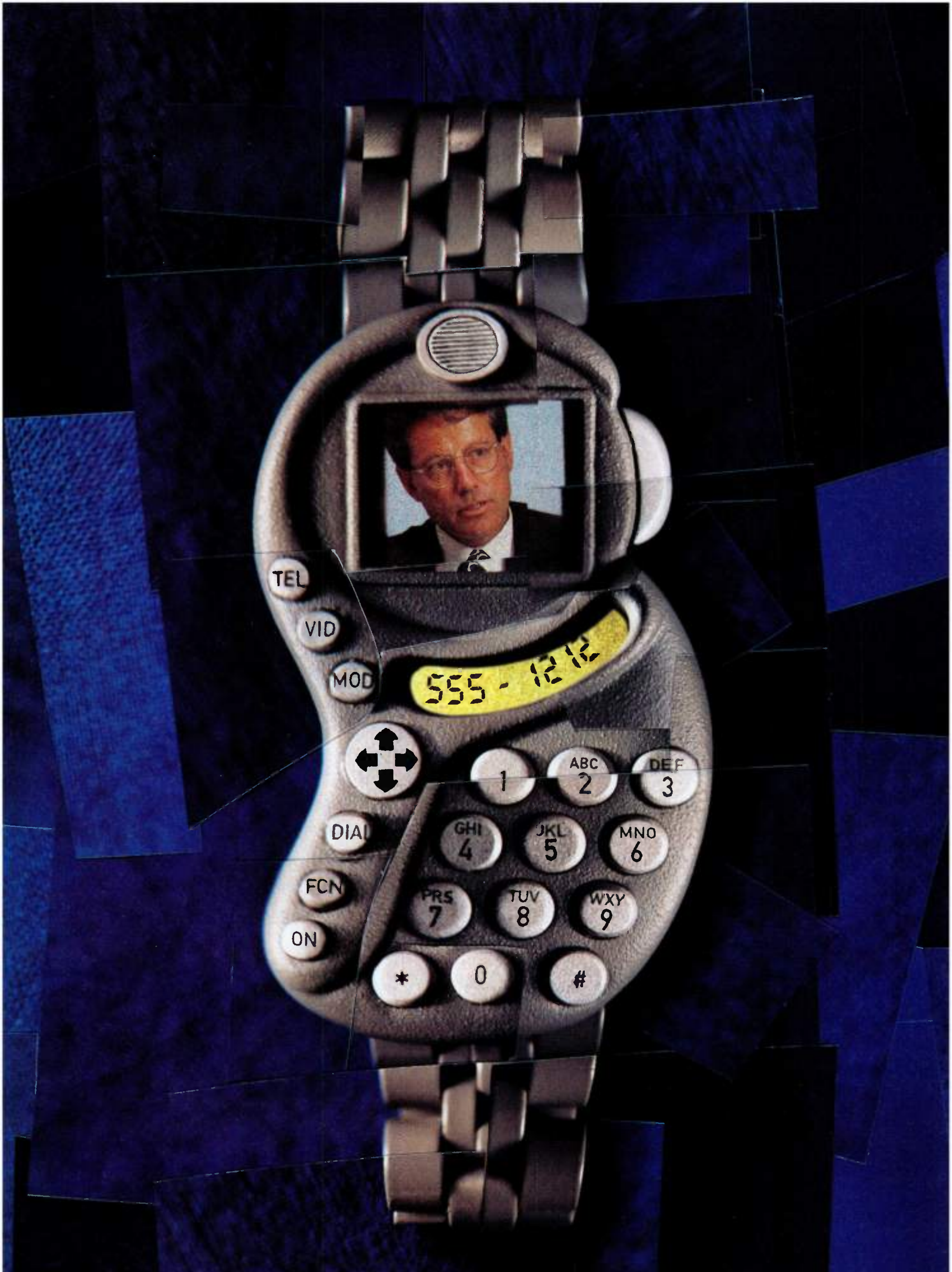
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This remarkable digital cell phone wristwatch isn't yet available, but the flash technology that's making it possible is. Today. From AMD.

AMD

HOT PC PRODUCTS

Viper V330 from Diamond Multimedia is a 2D and 3D graphics board that delivers 128-bit processing. It may look primarily like a gaming board (because it is), but Viper whips out Windows-based business graphics faster than you can say "Visual Aids." Full-screen video also is an option since Viper uses TV output that's upgradeable to include DVD, TV tuners, and video-capture applications.

The card is based on the Riva 128 graphics accelerator, developed by NVIDIA Corp. and SGS-Thompson Microelectronics. Viper uses 128-bit buses to speed data through the internal processing blocks. Speaking of speed, the card delivers accelerated full-screen, MPEG-1 video playback at up to 30 frames/s.

As far as ratings go, Viper wears a 3D Winbench rating of over 225 million WinMarks (640 by 480 pixels, 16 bits/pixel). The card's 2D rating is 140 million WinMarks for Windows 95 and 130 million WinMarks for Windows NT (1024 by 768 pixels, 16 bits/pixel). All of the benchmarks were performed on a Pentium II 266-MHz MMX CPU.

Viper works the graphics computations by using 50 separate 32-bit floating-point math engines. These engines each run at 100 MHz, yielding a compute throughput of 5 GFLOPS. The on-chip RAMDAC runs at 230 MHz, yielding true-color (24-bit) support at 1152 by 864 pixels. It also handles high-color (16-bit) support at up to 600 by 1200 pixels. Refresh rates are up to 200 Hz.

Because the card features an NTSC/PAL output port, Viper's output can be directly fed into NTSC/PAL, S-VHS, composite-video monitors, or VCRs.

Two versions of the Viper card are currently available: a retail version with a PCI interface bundled with drivers and application software, and an OEM version with either an AGP or PCI interface.

For more information, contact Diamond Multimedia Systems Inc., 2880 Junction Ave., San Jose, CA 95134-1822; (408) 325-7000; Internet: http://www.diamondmm.com.

ClusterPRO, from Realtime Performance, is an open architecture application that uses the company's ControlPRO 97 foundation. Also recently released MonitorPRO 97 works with ControlPRO to give users analysis and data acquisition capabilities. Realtime Performance's control software controls over 10,000 pieces of semiconductor manufacturing equipment worldwide.

ControlPRO uses a Windows NT type of interface in intranet-based distributed data and analysis situations. With the addition of ClusterPRO, the tools can provide users with scheduling and control algorithms in support of multichambered cluster software.

ClusterPRO runs as a server with remote procedure call interfaces. This feature allows manufacturers of cluster controllers to build applications or enhance previously existing ones by integrating software modules, third-party applications, and other tools.

Those manufacturers in search of standard architectures need not fear, ClusterPRO uses Cluster Tool Module Communications. The tool tightens up communication links to work with the Remote Procedure Call interface in beefing up SECS communications. As a result, users will see a faster response time and a more robust system.

MonitorPRO 97 pumps up semiconductor processing tools by delivering real-time data acquisition, data plotting, data reporting, and production monitoring. With all this data, the tool allows users full control of equipment, based on their parameters. When users establish set points for system variables, equipment events, or sensor data, the values can be used in the maintenance of equipment and in meeting performance standards.

For more information, contact Realtime Performance Inc., 158 Commercial St., Sunnyvale, CA 94086; (408) 245-6537; fax (408) 245-6547; e-mail: marketing@rp.com.

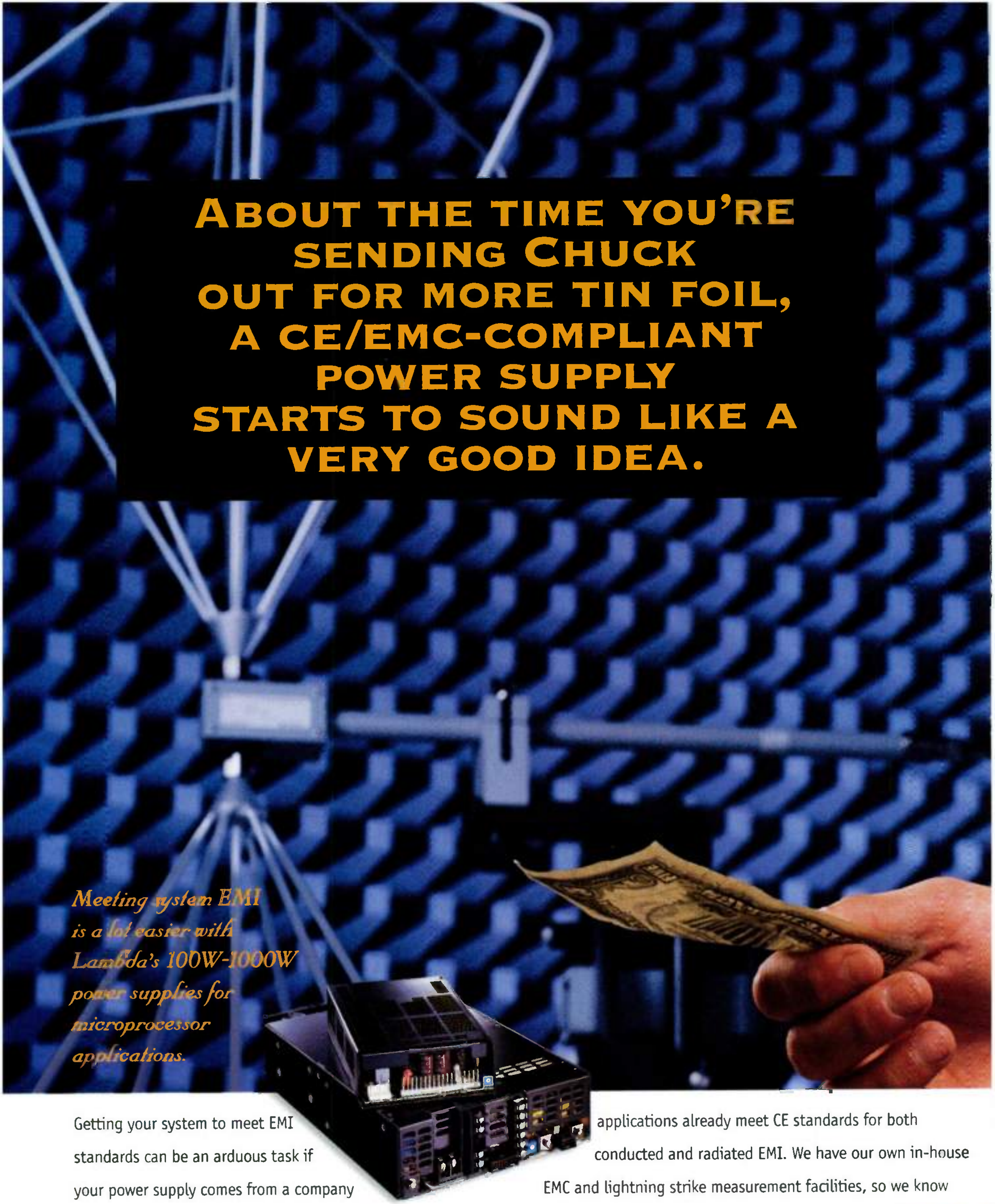
The D/240PCI-T1 and the D/300PCI-E1 are high-density, PCI processor-independent computer telephony products. Dialogic Corporation's newest offerings feature up to 30 ports of DSP-based voice processing. The company manufactures computer telephony components for the call-center management, data, fax, speech synthesis, voice, and voice-recognition markets.

Computer telephony PCI products like the D/240PCI-T1 and D/300PCI-E1 help developers and OEMs to build Internet Protocol telephony gateways, call-center solutions, unified messaging systems, and media servers. These products supply the network protocol support, switching fabric, and voice-processing tools to bring technologies used in teleconferencing, faxing, and Internet applications to users with high performance and reliability.

In order to bring standard PCI technology to its users, Dialogic spent some time with the PCI Special Interest Group (SIG). PCI SIG is a group comprising members of the microcomputer industry who perform independent tests on new technology. The group found that Dialogic's new products met their 2.1 specification in interoperability.

Designers working on ISA platforms do not have to change their existing applications, since these PCI products are designed to SCSA standards, allowing for easy migration to PCI platforms. They also have been approved for up to 20 channels of DSP-based voice applications.

Contact Dialogic Corp., 1515 Rt. 10, Parsippany, NJ 07054; (973) 993-3000; fax (973) 993-3093; Internet: http://www.dialogic.com.



Getting your system to meet EMI standards can be an arduous task if your power supply comes from a company that considers it to be your problem, not theirs.

But at Lambda we supply solutions, not just power. Our 100W-1000W PFC power supplies for microprocessor-based applications already meet CE standards for both conducted and radiated EMI. We have our own in-house EMC and lightning strike measurement facilities, so we know these supplies can stand the test of worldwide regulations, as well as the test of nature.

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GREENLOOK

While attending a party recently, a friend asked me about which electronic technology would see the most exciting developments over the next decade. I paused, thinking about the myriad of advances in submicron structures, gigabit networks, optical computers, and smart sensors. After a while, I finally answered with the two-word phrase made famous by a certain Scottish starship engineer in a well-loved TV series: "It's Green!"

It is with these words that we welcome you to *Electronic Design's* new section, "GreenLook." Our goal is to provide you news and technical insights from the emerging field of environmentally and socially responsible engineering practices, better known as "green engineering."

First, what do you think of when you hear the term "green engineering?" Do images of granola-munching, tie-dyed, counterculture types spring to mind? Do you imagine them issuing tedious diatribes about the evils of technology and capitalism from the comfort of their solar-powered tepees? Think again.

Rather than being a fringe movement, environmentally responsible practices are being increasingly adopted by big and small companies across the globe. It usually doesn't involve costly or exotic technology. It just means taking some responsibility for the stuff we design and produce.

Green engineering simply involves looking carefully at the materials consumed when making a product, as well as the waste generated during its manufacture. It also means that we must consider the full life-cycle of the widgets we unleash upon the world. This includes how much energy and other resources they will consume during their lifetime, as well as what happens when we're done with them.

There are many reasons to be concerned with the environmental impact of the stuff we make, but the one we can all agree upon is the bottom line: profits. Many companies, including those in the electronics industry, are discovering that green in the environment means green in the wallet. Often, it's because the less they put up their smokestacks, out their waste pipes, and into their dumpsters, the more they are shipping.

Also, companies like SGS Thompson, Compaq, and Legacy Systems are finding that, in the long run, it's much less costly to prevent pollution than to clean it up! Finally, if our industry gets its act together voluntarily, we can reduce or avoid any further government regulations or sanctions.

But green engineering isn't just about business. I'm sure that all of us would like to provide our children a more cleaner and more hopeful world than the one we inherited.

In some ways, developing clean technology is like the space race of the sixties. It presents a new set of technical challenges that may change the way we look at the world forever. Some might say that these are impossible goals, but that's dangerous to say to an engineer! We are problem-solvers at heart, and will find opportunity in creating the technologies that will lead us to a sustainable economy.

We also should realize that we don't have to wait for upper-level management to make environmental concerns a priority. As engineers, we wield great power in the choices we make. When you consider that our design decisions are multiplied by the number of products produced, you can see that any effort to reduce waste or pollution can yield big results. No single person should bear the entire burden, but the results will be better if we all do our part.

This column will strive to keep you informed of products, practices, tools, and technologies that you can use on the job that have positive environmental effects. We'll also update you on what individuals and companies are doing to incorporate green technology into their products.

You're invited to send in any tidbits you've discovered, or to request coverage on any topics that you feel deserve coverage. Mike Sciannamea will gladly accept submissions at **mikemea@class.org.** You also can contact me at **leeg@class.org.**

Lee Goldberg

OFF THE SHELF

Introduction to Optical Engineering provides a basic primer to modern optical engineering, covering the fundamental concepts as well as practical techniques and applications, including the latest technology in fiber sensors and optical communications. Basic optical principles are presented, including reflection, refraction, aberrations, diffraction, and interference. Optical devices and processes also are discussed, along with simple optical instruments, photodetectors, spatial light modulators, holography, and lasers. Two chapters are devoted to linear system transforms and signal processing, with another chapter featuring a discussion on fiber optics. The 409-page book is priced at $44.95. Contact Cambridge University Press, 40 W. 20th St., New York, NY 10011-4211.

The TAB Electronics Yellow Pages aims to help readers find the best deal on electronics and computer equipment or components without spending much time searching through catalogs. Companies are listed alphabetically according to equipment type. Entries include addresses, telephone numbers, fax numbers, e-mail addresses, and technical-support numbers. Also included is information on warranties, payment options, and refund policies. Cross-referencing will help readers find suppliers for equipment such as audio equipment, CPUs, robotics, and short-wave radio equipment. The 390-page book is priced at $29.95. Contact McGraw-Hill, 11 W. 19th St., New York, NY 10011.

Land-Mobile Radio Systems Engineering presents the science and the art of system design procedures in land-mobile radio system engineering. Chapter-end problems and solutions provide insight into how the theory and various analytical procedures are used in practice. Featured are numerous figures, tables, and equations. The 495-page book is priced at $79. Contact Artech House Publishers, 685 Canton St., Norwood, MA 02062; (800) 225-9977, ext. 4030; fax (781) 769-6334; Internet: http://www.artech-house.com.

Don't Tell Racer X About MATRIX$_X$

Many times we here at QuickLook will let our readers in on information having to do with automotive applications. From batteries to global positioning systems, we're right on top of the latest developments. Within the automotive industry, the benchmarks for performance are set at the racetrack.

But combining advances in embedded software and high-performance automobile engineering at the same time is new. One company, Integrated Systems, typically recommends its MATRIX$_X$ family of design tools for military applications such as gun turrets, missile guidance systems, flight controllers, and battlefield simulations. In addition, their design tools can be found in semiconductor manufacturing and gold-mine processing facilities. Today, the Newman/Haas Racing Team is using MATRIX$_X$ to develop their vehicle systems.

Newman/Haas is owned by actor Paul Newman and auto racing legend Carl Haas. The team belongs to an Indy car racing series called Championship Auto Racing Teams (CART). CART comprises weekend racers of highly technical vehicles that travel 230 mph or more on specially treated surfaces. Two of the team's drivers this year are Michael Andretti and Christian Fittipaldi.

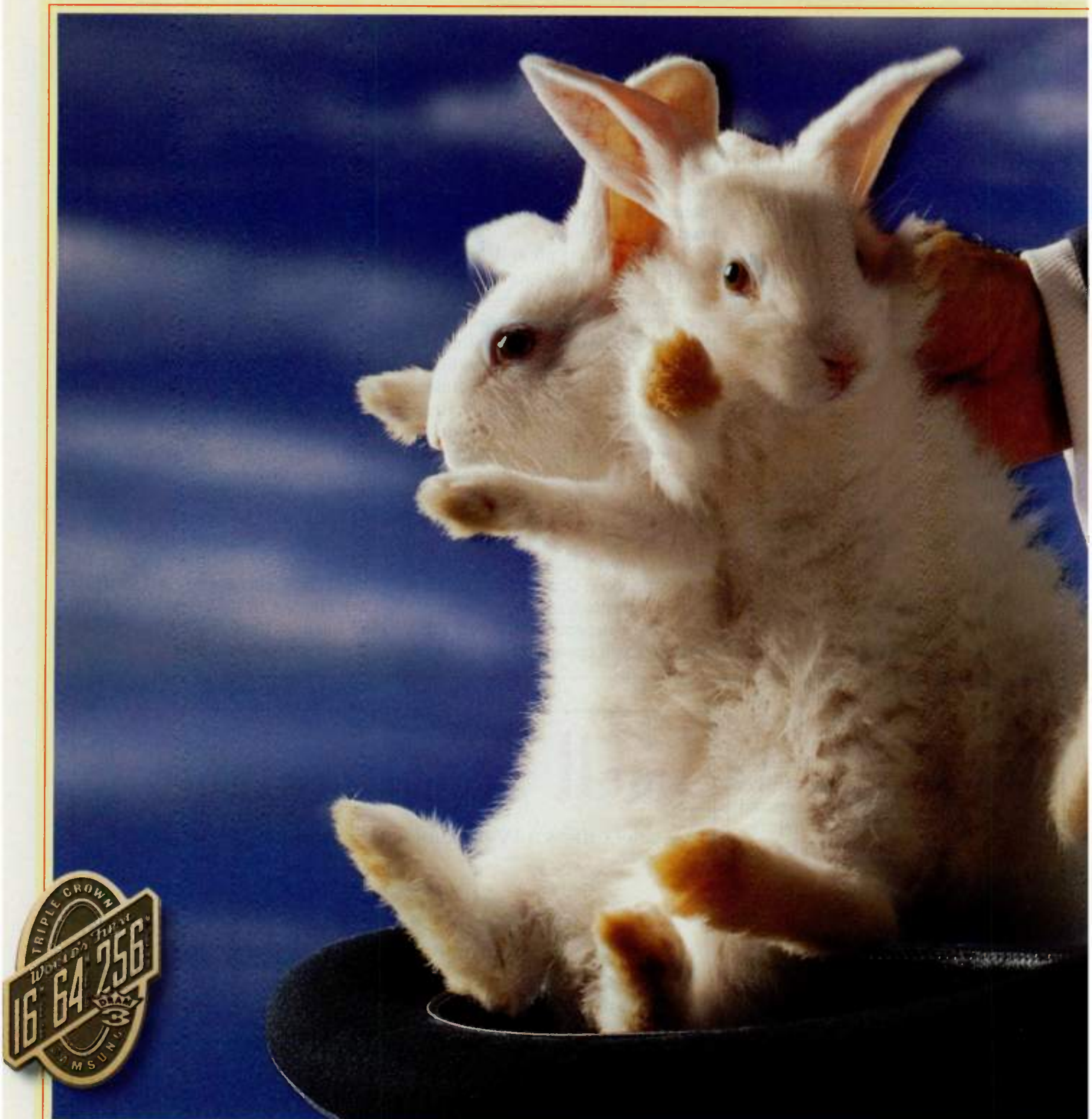
The drivers are beholden to a highly experienced team of engineers and mechanics. Specifically, the engineers are responsible for supplying the optimum settings for the car's suspension, shocks, powertrain, and aerodynamic surfaces. The engineers use advanced analysis tools such as MATRIX$_X$ to model the different track and weather conditions, as well as other changing variables in the race. The drivers' practice laps provide data for the engineers, which is used to drive the MATRIX$_X$ simulations. The simulations validate the new designs before the team modifies the car. Bottom line: more simulation equals fewer practice laps and tweakings before race time.

In CART racing, teams are severely limited as far as practice times are concerned. The teams may only practice and prepare for the race in the space of about two hours per weekend. This is are when the team must set the aerodynamics, tires, engine, gearbox, and suspension. For every minute spent in the pit, a minute of practice time is gone.

Newman/Haas picked MATRIX$_X$ for their engineering analysis tools because they found that the tools allowed them to find the best set-up in the least amount of time. The engineers examined many of the tools available, taking into account that the racing environment is so challenging. Newman/Haas specifically looked for tools that wouldn't limit their processes, which are constantly improving. Integrated Systems' tools gave them the flexibility they need. The models that are used are so complex that the team uses a powerful Silicon Graphics workstation to handle graphics and computations.

A unique aspect of CART racing is that the track conditions may change drastically from one race to the next. Tracks can vary from super-speedways to tight road courses. That means that the team must configure the car specifically to the track for each race. Integrated Systems' tools allow racers to predict the best set-up possible, depending on road conditions, leaving the team more time to devote to the mechanics of the car.

For more information, contact Integrated Systems Inc., 201 Moffett Park Dr., Sunnyvale, CA 94089; (408) 542-1500; fax (408) 542-1950; Internet: http://www.isi.com.—**DS**



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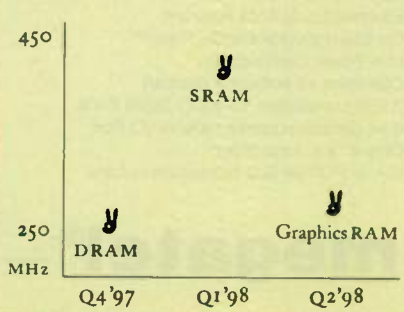

Which means it isn't a radical change in technology. But an incremental step.

It's not revolutionary. It's *evolutionary*.

And since that means only minimal system redesign is required to use the DDR part, it may be the best news of all.

THE ENVELOPE, PLEASE

This column was established to tell engineers how their peers (and sometimes their families) are doing in comparison to the rest of the industry. We choose to spotlight individuals or companies that stand out in interesting and innovative ways. If you know of an individual or a company that's recently won an award, let either Mike Sciannamea at *mikemea@class.org*, or Deb Schiff at *debras@csnet.net* know so we can let everyone else know. We believe that honor is an important characteristic, and we'd like to pass that on.

In the heat of the just-completed summer, the American Electronics Association (AEA) honored MicroSim Corp. for its DesignLab electronic design automation (EDA) software. The Innovation Award for technology recognized DesignLab specifically for its integrated, start-to-finish EDA system for mixed analog and digital circuits. The 13-year-old company specializes in circuit simulation products that support Microsoft Windows 95, NT, and Sun Microsystems.

The American Electronics Association boasts 3000 member companies, with the Orange County (Calif.) Council holding a roster of 170 electronics, software, and information technology (IT) companies.

For more information, contact MicroSim Corporation, 20 Fairbanks, Irvine, CA 92717; (714) 770-3022; fax (714) 445-0554; BBS (714) 830-1550; e-mail: nmchugh@microsim.com.

Communications & Power Industries (CPI) has chosen Brush Wellman as its Strategic Supplier of the year for 1997. Of the 85 suppliers that CPI uses, 35 of are Key Suppliers. Of that group, six are in the upper echelon of the Strategic Supplier level.

CPI provides an enormous variety of solutions in the broadcast/communications, electronic countermeasures, industrial, medical, radar, and scientific markets. Interested readers may contact CPI on the World Wide Web at *http://www.cipp.com* for more details on its Beverly Microwave Division, Communications and Medical Products Division, Eimac Division, Microwave Power Tube Products Division, Satcom Division, and Traveling Wave tube Products Division.

Brush Wellman's record of eight consecutive months of 100% on-time delivery and 100% quality with CPI won it the Dock-to-Stock characterization. Basically, that means there is no incoming inspection for Brush Wellman materials. The company are suppliers of beryllium, alloy, ceramic, precious metal, circuit metallization, and other products.

For more information on their product offerings, readers may contact Brush Wellman, 22 Graf Rd., Newburyport, MA 01950; (508) 463-6543.—**DS**

INTERNET NEWS

Making e-commerce an even safer choice for intelligent Internet surfers, IBM has released its 4758 PCI cryptographic coprocessor/adapter. The new card is designed to work in such applications as Internet transactions, in-flight entertainment, and other privacy-oriented areas. The encryption implementation used on the 4758 is certified by the National Institute of Standards and Technology (NIST).

The not-immediately apparent use of the PCI cryptographic coprocessing/adapting technology in the personal, video-on-demand airline capacity has been approved by industry professionals. Why would the airline industry need such encryption protection? Well, the movies provided on airplanes are often pre-video release, and therefore, open to potential piracy. IBM's new card allows movie supply companies to meet the motion picture industry's encryption requirements for this purpose.

Users can program the 4758, which is SET-enabled. It uses Data Encryption Standard keys, RSA private keys, meets the Federal Information Processing Standard 140-1 for tamper resistance. The 4758 is a one-slot, Type-3 add-in attachment for PCI bus 2.1 supporting computers.

The new cryptographic coprocessor/adapter includes a time-of-day clock, hardware-based random number, and RS-232 serial port. Within the card is a subsystem that's outfitted with an Intel-compatible 80486 processor with 4 Mbytes of RAM and 2 Mbytes of flash memory.

For more information, contact IBM North America, 1133 Westchester Ave., White Plains, NY 10604; (520) 574-4600; Internet: http://www.ibm.com/security.

OK, I just bought a new car, and I'd like to show off my hot new wheels to my cousins in Arizona. Fortunately for the both of us, we each have a good Internet provider, because by using Boca Research's Video Phone Kit, Video Phone Classic, or Video Phone Elite, we can use Galacticomm's Cast-a-Vision to link up "in person." Now, my young cousin can see a video of my car's new interior, ask me about the features, and I can answer him live, free-of-charge.

Mind you, HE doesn't need the software or videoconferencing software, unless he wants to show me his new truck. All he has to do is hook up to Boca's host site, *http://www.bocaplace.com*, with either Netscape Navigator or Microsoft's Internet Explorer v 4. The Internet broadcasting software is licensed to Boca from Galacticomm for broadcasting live video, audio, or anything that can be displayed on a PC over the Internet.

Boca gives many examples, some like the one above, of ways to use the software, such as monitoring childcare, buying animals over long distances, etc. In the office, managers can check in on spreadsheets as they're being made, or documents as they're being written. Boca will bundle scaled-down versions of the software with its 33.6- and 56-kbit/s modems.

For more information, contact Boca Research, 1377 Clint Moore Rd., Boca Raton, FL 33487-2722; (561) 997-6227; fax (561) 997-7189.—**DS**

"CHOOSING NEC FOR OUR EMBEDDED PROCESSOR HAD A LOT TO DO WITH TIME. *THE LACK OF IT, THAT IS."*

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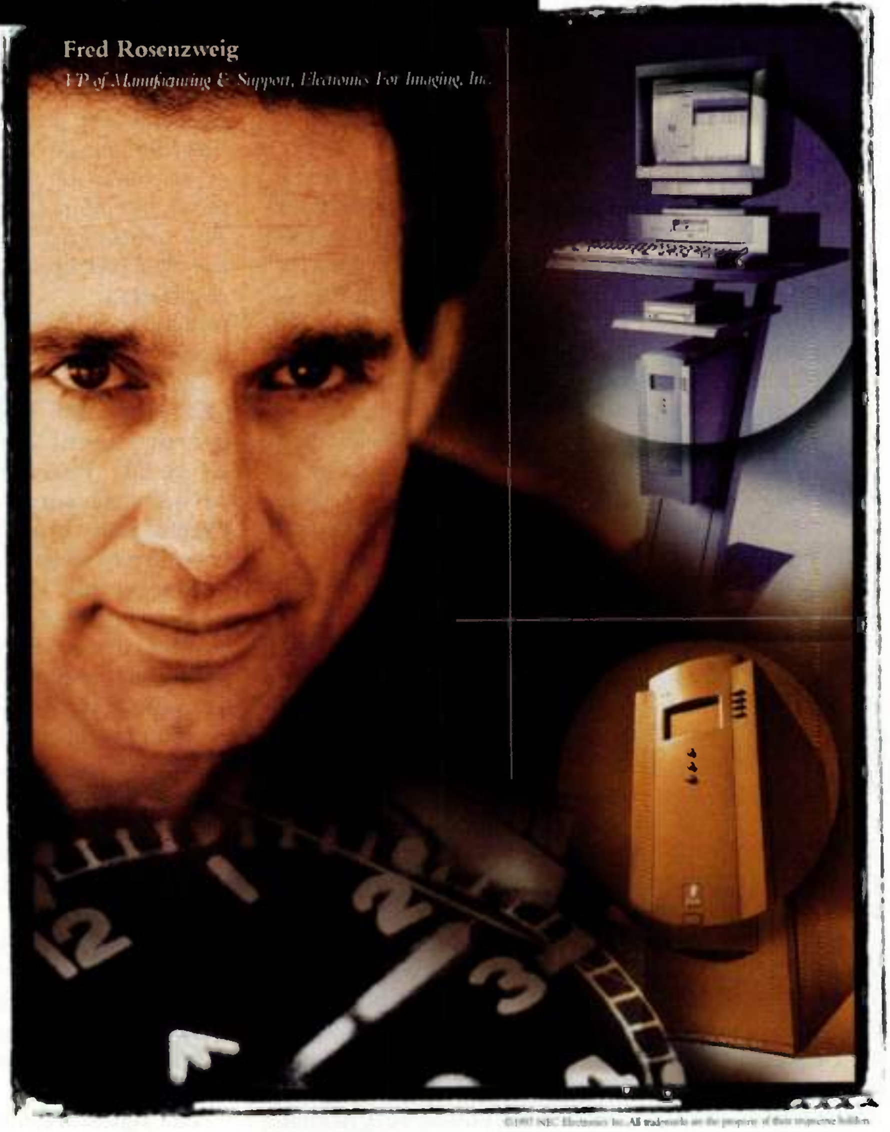

"EFI is constantly developing the next level in leading-edge color printing with the Fiery® Color Server.™ Our history is to be first to market and we have always been responsive to the needs of our customers.

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"Scalability is another reason we selected NEC to play a major part in the future of our product line. The top-to-bottom scalability of NEC's MIPS® RISC architecture will be instrumental to the range of devices EFI is introducing over the next year—from black and white low-end printers, to very high-end production machines.

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Y2K UPDATE

As the drop dead deadline grows nearer to the Year 2000 Date Change (Y2K), it has become evident that many of the companies who've offered solutions have concentrated solely on the COBOL compliance problem. Tailoring millions of lines of code to fit into the four-digit date field needed to support Y2K application data has grown into a software issue, instead of an individual programmer issue. Initially, all of the dollar predictions for the cost of the mammoth project were based on what independent programmers would charge per line of code. Now, with software designers working insane hours, the Y2K market is flooded with solutions in the form of software that will not only find the offending code, data, or operations, but will fix it as well.

But what about all of the other applications and codes? Struck with the imbalance in solutions for other languages, companies beset with these other languages and applications are finding that they have to spend outrageous amounts of money on consultants to fix their precompliant applications. However, like needles in haystacks, there are a few companies out there who are tackling challenges other than COBOL, such as PL/I. Data Integrity, for one, recently introduced its Millennium Solution for PL/I. Millennium Solution for PL/I features a mathematical approach called Dynamic Centuries to address the Y2K issues. Data Integrity's first product that deals with Y2K, Millennium Solution for COBOL, has been available since 1996, and is the inspiration for the company's foray into the PL/I arena.

Why would an enterprise choose Data Integrity's solution? Typical approaches use field expansion and windowing, while the Millennium Solution repairs the code without changing existing databases or archived data. The solution focuses in more closely on the offending dates, trims down the number of lines of code requiring compliance changes by over 90%, and reduces testing requirements by 90%. All of these advantages add up to big savings in time and money, especially at this late stage in the game.

According to the company, when managers have used Millennium Solution, they've found less than 1% of code needed to be changed. This figure is in opposition to the 6% to 12% lines of code quoted in industry averages of projected system failures. The result is a large drop in the compliance program's bottom line. Calculations have yielded a high end of 45% in cost savings (total cost). The basis of that cost lies in the time it takes staff members to find, fix, and test date-sensitive programs.

For more information on the Dynamic Centuries automated Y2K compliance process or Data Integrity's Millennium Solution, contact Data Integrity Inc., 228 Highland Ave., West Newton, MA 02165; (617) 964-1977; (617) 244-2324; Internet: http://www.dii2000.com.—**DS**

Forget X-Ray Vision Specs, Try RADAR Flashlights

Imagine that you're a police officer. It's your first day on the beat and you've just chased a suspect around a corner, only to lose him. You can't see a thing so you whip out your trusty flashlight. It may look like a regular flashlight, but it's not. It's a RADAR flashlight. You push the button, aim the beam on the wall and instantly, you see your suspect behind the wall.

It may seem a bit futuristic, but researchers at the Georgia Institute of Technology have already developed a prototype RADAR flashlight that can detect "a stationary individual behind a solid wooden door, or standing four feet behind an eight-inch block wall," says Gene Greneker, the principal research scientist on the project. Basically, the device works by using RADAR and a signal processor to detect movement. The prototype can even pick up respiration from up to three meters away.

The beam itself is pretty narrow, about 15° to 20°. The device's main purpose is to detect body movement that is generated by breathing. If criminals are worried about exposure to radiation, they wouldn't have a leg to stand on in a lawsuit. The flashlight emits 10 times less radiation than the exposure leakage level allowed for microwave ovens in the U. S. Essentially, that level translates into the same amount of radiation exposure derived from automatic doors that open on sensor commands.

In its prototype stage, the signal processor is located on the outside of the casing. Respiration signals can be viewed on a computer-based signal process monitor. Eventually, the researchers plan to shrink the processor, through the use of high-speed signal-processing technology, so that it fits within the flashlight casing.

Key applications for the RADAR flashlight include finding hostages within a room, based on their movements or RADAR respiration signatures; and finding survivors who've been buried beneath piles of rubble from earthquakes, accidents, or bombings. Correction officers performing bed checks during lockdown also will find the tool useful.

The signal from the RADAR flashlight is different from other kinds of technologies that are meant to function in the same manner in that it can penetrate clothing. It also can even detect breathing through a heavy coat. The human body only needs to move a few millimeters in either direction for the RADAR flashlight to pick up that person's movement.

For more information on the prototype RADAR flashlight, contact Georgia Institute of Technology, Atlanta, GA 30332-0828; (404) 894-3444; fax (404) 894-6983; Internet: http://www.gtri.gatech.edu.—**DS**

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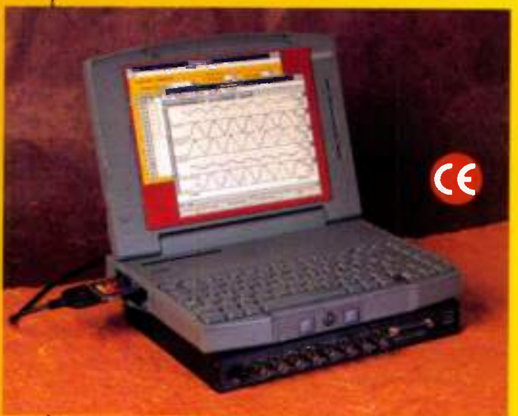

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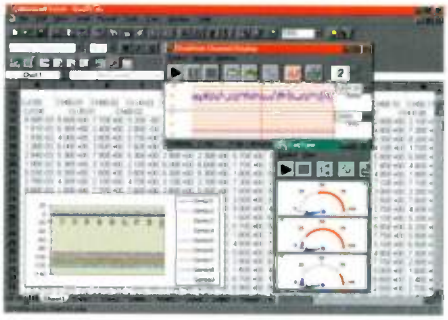

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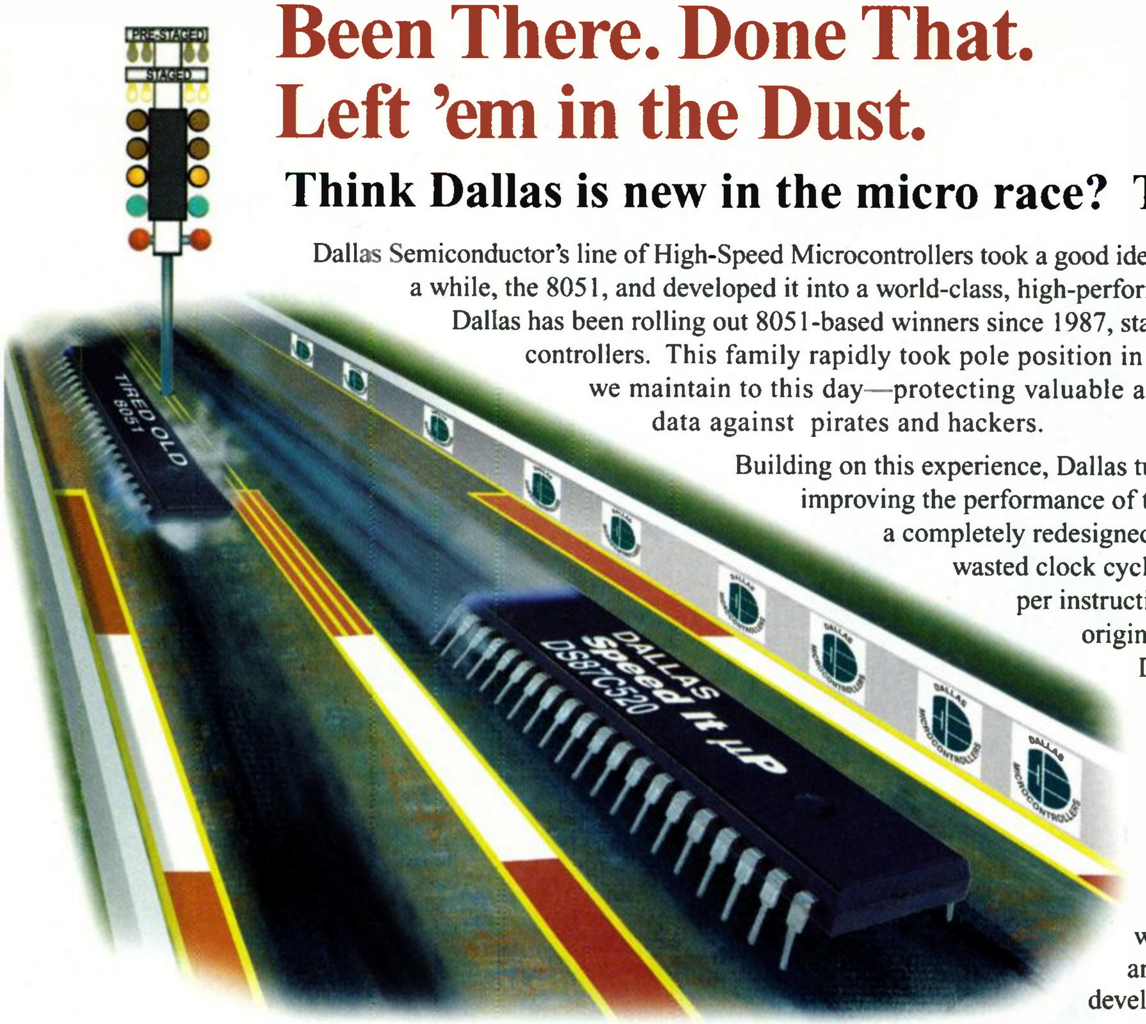
CIRCLE 325

Been There. Done That. Left 'em in the Dust.

Think Dallas is new in the micro race? Think again.



Dallas Semiconductor's line of High-Speed Microcontrollers took a good idea that's been around for a while, the 8051, and developed it into a world-class, high-performance machine. In fact, Dallas has been rolling out 8051-based winners since 1987, starting with Secure Microcontrollers. This family rapidly took pole position in the field—a position we maintain to this day—protecting valuable application software and data against pirates and hackers.

Building on this experience, Dallas turned its attention toward improving the performance of the 8051. The result was a completely redesigned core that eliminates wasted clock cycles. Using only 4 clocks per instruction (compared with the original 8051's 12 clocks), the DS87C520 runs up to a maximum clock speed of 33MHz, providing a performance level equivalent to a 99 MHz 8051. This allows you to turbo-charge your system without costly changes in architecture, software, or development tools.

Look under the hood and check out the added features:

- **On-Chip Memory Removes Performance Bottlenecks:** The DS87C520 offers 16K bytes of EPROM and 1.2K bytes of SRAM. With the additional SRAM onboard, part count can be reduced and performance levels can be further increased.
- **Power Management Mode for Portable Systems:** In this mode, you can reduce operating power requirements by 80%, while normal processor operations continue at a slower internal clock speed. Special circuitry allows the processor to automatically shift gears back to high speed when needed.
- **Extra Equipment:** In addition to the standard peripherals, the DS87C520 adds features that have traditionally been provided by external components. These include a second serial port, power-on reset, brownout detector, and watchdog timer.

Take a victory lap around the rest of our High-Speed Micro product family.

DS80C310	High-performance, low-cost 8051 replacement
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For more information, contact our pit crew.

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READER SERVICE 128

Ring Architecture Connects Up To 128 PCI Buses

Single-Chip Interface Allows Dual Rings To Add Fault Tolerance Without Dropping PCI Compatibility.

Richard Nass

COVER FEATURE

Don't worry. PCI has lots of bandwidth left, at least that's what we've been told. But lo and behold, that's not really the case when you open up the hood. When you get into higher end and server applications, 132 Mbytes/s just don't cut it. Even at 64 bits, 264 Mbytes/s can produce a bottleneck.

So what's the alternative? We could go to a proprietary scheme, but that would mean throwing away all the users' investments in PCI-based hardware, as well as the manufacturers' investments in research and development time. A better alternative is a configuration that would allow us to tie together a bunch of PCI buses, each running at 132 Mbytes/s. Such a scheme has been developed by Sebring Systems, Los Gatos, Calif. It's dubbed the Sebring Ring. While adding a layer of fault tolerance, the ring also removes PCI's slot limitation. With up to 128 PCI buses available to a system, the theoretical number of slots jumps to 512.

PCI 2.1 Compliant

The Sebring Ring can be used as an I/O backplane and cluster interconnect mechanism in servers and embedded computers, and as a switch fabric in switches, routers, and hubs. The beauty of the ring is that it is hardware and software compatible with today's PCI infrastructure. It maintains full compliance with the PCI 2.1 specification. It also operates in accordance with the I^2O specification. In addition to accelerating and expanding the PCI functionality, the ring adds packet- and cell-switching capabilities.

The ring is actually a dual, counter-rotating ring network which is formed by interconnecting four unidirectional, point-to-point links, each 16 bits wide and operating at 266 MHz *(Fig. 1)*. The peak transfer rate is set at 532 Mbytes/s. However, as the process matures, higher bandwidths will evolve. The links come from the Sebring SRC3266 chips, which provide a PCI expansion and acceleration mechanism. The chips form a network of PCI buses with an aggregate bandwidth sufficient for all pairs of networked PCI buses to communicate concurrently at the full PCI speed *(Fig. 2)*.

The SRC3266s form virtual bus-bus bridges and, as bridges, are software-transparent when operating. The ICs adhere to the PCI-PCI Bridge Standard and emulate a bus hierarchy during the configuration process. As a result, the Sebring Ring is BIOS autoconfigurable, and modules plugged into it retain their Plug-and-Play compatibility. Hence, no driver changes are required.

In operation, the SRC3266s act as interchanges. The Sebring Ring protocol is modeled after ATM, except that it employs variable-size cells as the mechanism to carry data (ATM uses cells fixed at 53 bytes). The cells could contain PCI commands, addresses, data, and response codes. Sebring Ring cells containing a bus transaction are limited to 52 bytes, making it easy to pad the cell to 53 bytes for an extended transmission over a standard ATM link. Cells containing 56 bytes (with encapsulated 53-byte ATM cells) also are supported, allowing the Sebring Ring to serve as an ATM switch fabric.

Network address generation without the use of real-time software interaction is achieved using Addressing Mapping Content Addressable Memory (AMCAM). The AMCAM generates the routing tag as a function of the transaction address. The AMCAM is loaded automatically and transparently as a byproduct of the system's autoconfiguration process.

Delays Around The Ring

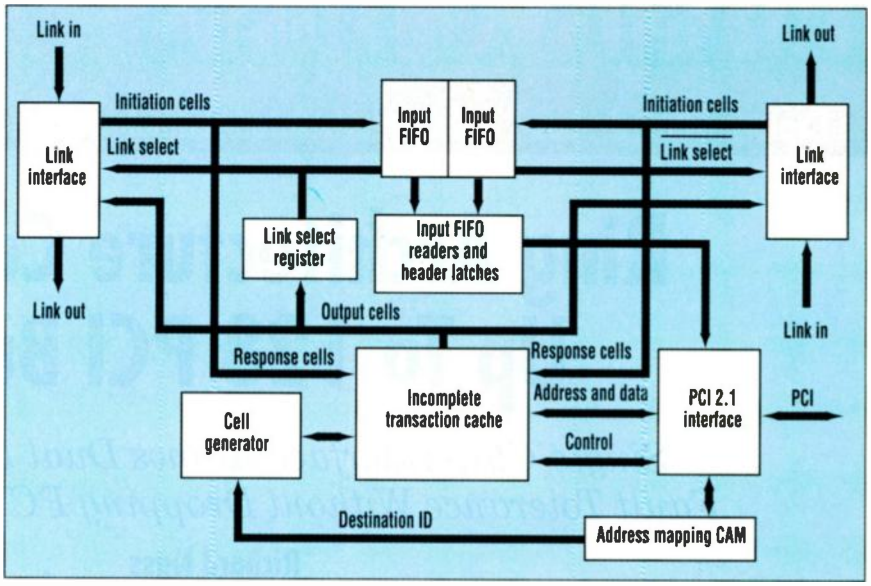
Round-trip delay is a concern on the Sebring Ring because all transactions include both an initiation and a response cell, and because latency is at least as important as throughput in determining overall system performance. When a local PCI transaction addresses a location mapped at another Sebring Ring node, the address phase on the local PCI bus is translated into an initiation cell and routed the short way around the ring to its destination, where the original PCI transaction is recreated. When this transaction completes on the target PCI bus, a response cell is returned in the reverse direction to the originating node to either retire information saved about a posted transaction or to complete a delayed transaction. All information that's required to retry a transaction is retained until a positive acknowledgment is received. The information is retained through the use of a response cell to maintain fault tolerance, as well as data and transaction integrity. Posting and read prefetching are used whenever permissible to allow the initiating PCI bus to proceed with a minimum number of wait states, regardless of the response delay.

While the reverse ring is optional in fiber-distributed data interface (FDDI) (and unavailable in Token Ring), it's required in the Sebring Ring. The SRC3266 interface contains the circuitry to drive both rings, which results in fault tolerance, four times the data throughput, and a reduced round-trip latency.

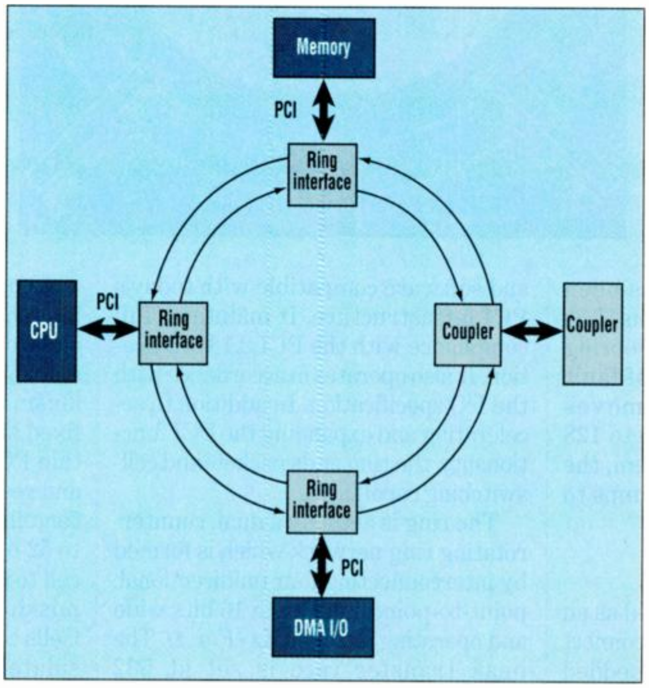
Because the Sebring Ring is circular, and paths are available in both directions, the maximum travel distance is halfway around the ring. With a uniform distribution of source-destination pairs, the average distance traveled is one-quarter of the ring's circumference. The worst case for data concurrency occurs when all trips are exactly halfway around, resulting in a concurrency of four times. To optimize performance, data "producers" should be placed next to data "consumers." Even with the producer-consumer pairs at the worst-case distance, the aggregate throughput is only four times the link rate. However, this scenario can be transformed into the best case by reassigning the modules to backplane slots.

The ring is specified to operate at an aggregate throughput of 4.25 Gbytes/s under ideal conditions. Such conditions occur when the traffic distribution is uniform throughout the ring. Adding in the typical overhead, such as a header, response cells, addresses, cyclic redundancy check, and an equal mix of reads and writes at the maximum cell size, the data throughput is 2.4 Gbytes/s. But it's possible to achieve an even higher throughput by taking advantage of nonuniform traffic distributions.

Cells are transmitted by waiting for a cell boundary or idle slot to appear in the through-traffic at a ring interface. If a through-cell enters during the emission of a locally generated cell, it is temporarily stored in a one-cell bypass FIFO to prevent a collision. The ring interface can emit one cell at a time, and only if its bypass FIFO is empty. Such a rule spreads the traffic out in time so that traffic entering the network is absorbed with a minimum disruption to traffic

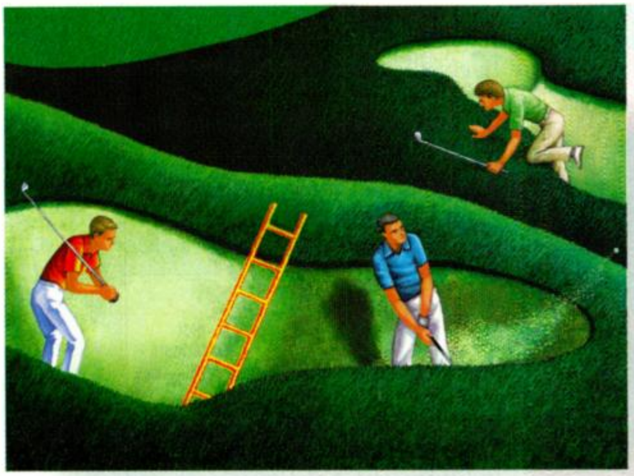


2. The SRC3266 ring interface chips form a network of PCI buses with an aggregate bandwidth sufficient for all pairs of networked PCI buses to communicate concurrently at the full PCI speed. The combined peak transfer rate is 532 Mbytes/s.

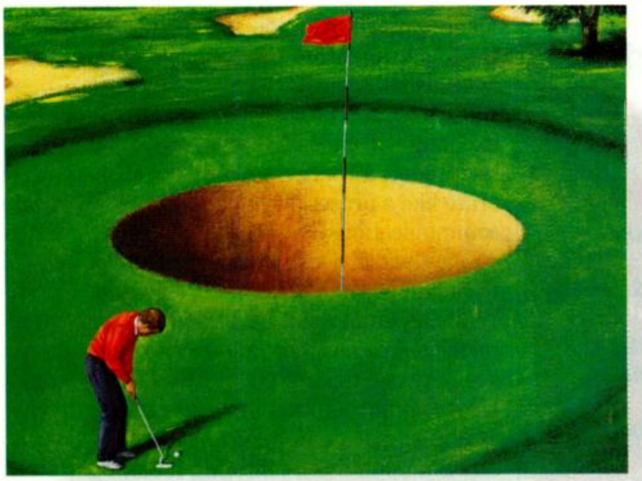


1. The Sebring Ring consists of a dual, counter-rotating ring network, which is formed by connecting four unidirectional, point-to-point links. Each link is 16 bits wide and operates at 266 MHz.

Designing With Ordinary PCI Interface Chips.



Designing With The New S5920 PCI Interface Chip.



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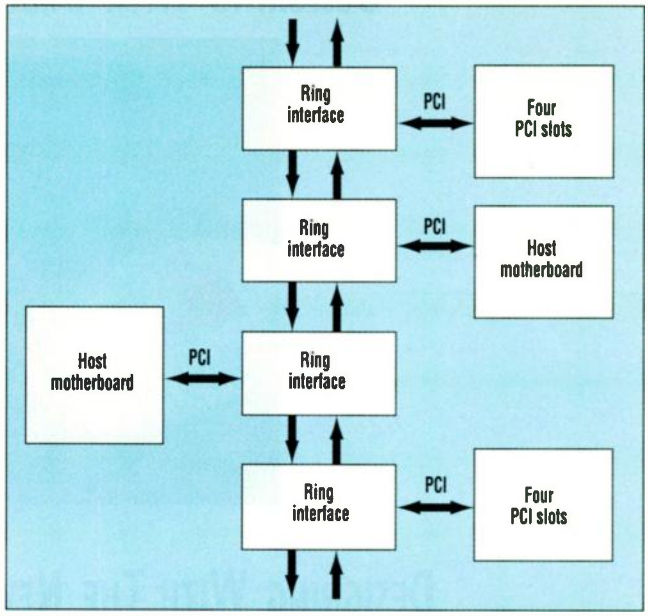
that's already on the network. When the network is relatively idle, this rule has almost no effect on operation. The bypass FIFO either doesn't fill or empties before the next transaction initiation completes on the local PCI bus.

The Sebring ring can operate as an interprocessor communications medium. In this fashion, the SRC3266s form a cluster-interconnection mechanism for servers *(Fig. 3)*. Because the interfaces transparently translate the bus transactions into an exchange of ATM-like cells, the architecture lets an entire LAN or WAN operate like a processing cluster with low communications overhead.



3. The Sebring Ring can perform communications between processors. In this configuration, the ring chips form a cluster-interconnection mechanism for servers.

Bandwidth doesn't necessarily have to be allocated evenly over the ring. While an empty slot isn't required for collision-free merging, idle-empty slots are required to empty a bypass FIFO. Upstream nodes that generate traffic at a high rate can prevent a downstream node from emitting a cell by preventing it from emptying its bypass FIFO. To handle this procedure, a "fairness counter" is implemented at each link interface. The device counts down at one rate when emitting a cell and at a potentially different rate when it observes an idle at the link output.

The relative counting rates determine the fraction of the link bandwidth that the node can utilize. When the two rates are equal, the node can use up to 50% of the link bandwidth. A predetermined threshold sets the point at which a node may emit a cell.

A cell's travel time depends on the amount of competing traffic and the distance traveled. Also, at each node, there's a pipeline delay as well as a possible delay in the bypass FIFO. This delay depends on the probability of the through-bound cell entering the interchange (the SRC3266 chip) while a locally generated cell is being emitted. In the SRC3266, the minimum pipeline delay per node is two clocks at 266 MHz. The maximum delay is 15 clocks, and occurs when the cell is diverted into the bypass FIFO.

The SRC3266 includes two 512-byte input FIFOs, enough to hold 20 of the largest cells. Traffic addressed to a node with a full input FIFO can't exit there and instead travels all the way around the ring and is removed by its source node. The only disruption this causes is the minor performance loss due to the additional traffic. The source notes the retry and makes another attempt unless the retry limit has been reached. In this case, software is invoked using an interrupt. Retries are possible, but infrequent due to the relative buffer sizes and traffic characteristics.

Price And Availability

The SRC3266 is fabricated in a 0.35-mm CMOS process. It's housed in a 266-pin BGA surface-mount package. Available in sample quantities by year's end, it sells for $59 each in lots of 10,000 units. Production will commence in the first quarter of 1998.

Sebring Systems Inc., 16400 Lark Ave., Los Gatos, CA 95032; (408) 358-7827; http://www.sebring.com. CIRCLE 525

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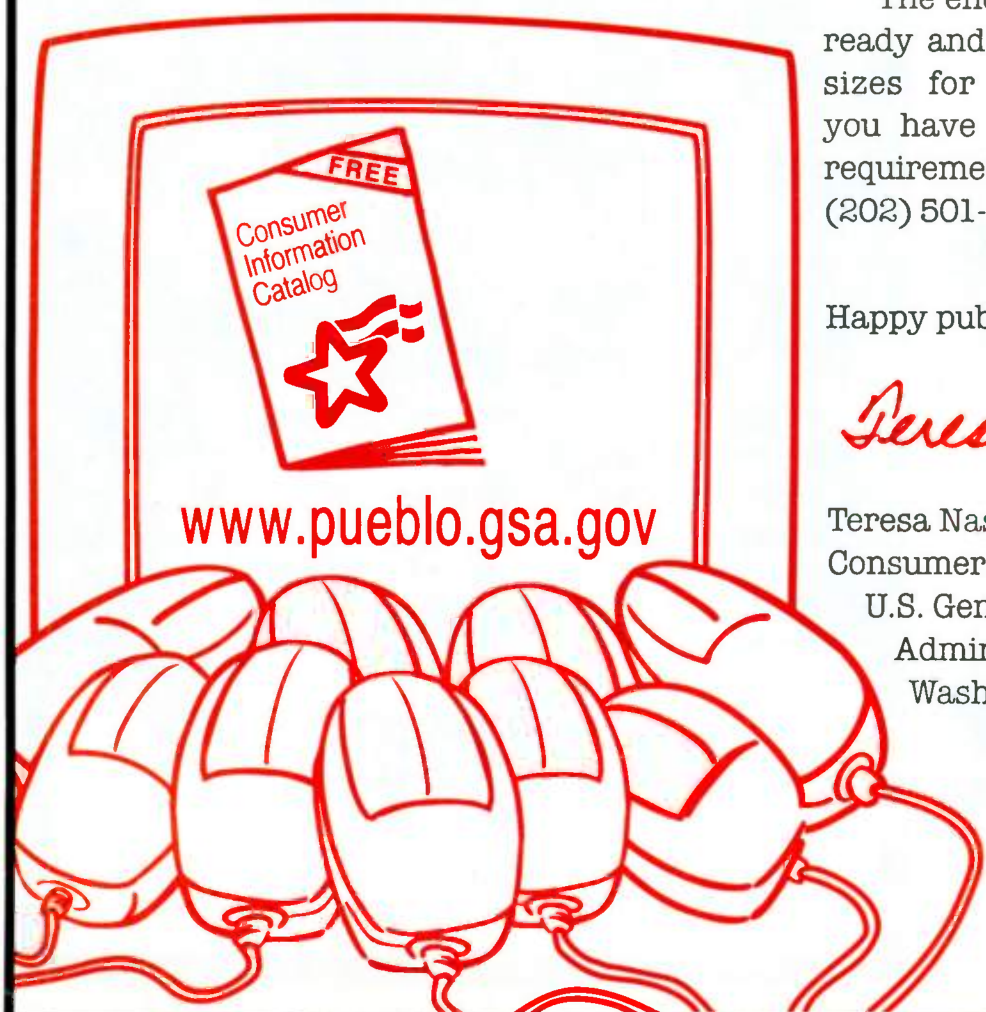

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Teresa Nasif, Director
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From Buses To Rings

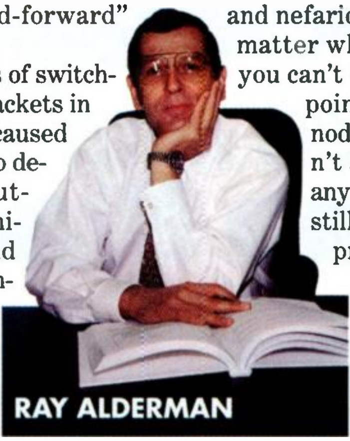
Rings are the second topography in the architectural food chain of computers. While buses are two-dimensional (they have length and width, but no depth), rings are the first tool for building three-dimensional architectures.

As mentioned in last column, we know that the primary aberrant behavior of a bus is blocking latency, and the secondary performance-robbing characteristics are connection and disconnection latency. Rings eliminate all three of these nefarious behaviors, but they substitute three new ones: switching latency, routing latency, and reverse-scalability.

A ring is simply a bus with its ends tied together. Instead of the bidirectional interface used on buses, each node on a ring has two separate interfaces; one for input and one for output. Each node can receive and transmit data to and from the ring simultaneously because the connections are point-to-point. This is where all of the problems begin.

When a node on the ring sends data to another node, that packet must go through each node in the ring until it arrives at the intended recipient. The more nodes in the ring, the longer it takes. This is reverse-scalability, the opposite of what we want in an architecture. The nice thing about a ring, however, is that a potential user can never be blocked. Every node is free to transmit data on the point-to-point connection to the next node in the ring at any time.

Once the data is put out on the ring, each node between the sender and receiver must handle the packet. Typically, the data comes into a node through a FIFO. The address of the packet is compared to the receiving-node's address and if there's a match, the data is moved into local memory. If there's no match, the data must be sent to the out-going interface and then on to the ring's next node. This involves switching latency (from the incoming FIFO to the comparator) and routing latency (moving the data to internal memory or to the outgoing FIFO). These primitive rings that work in this manner are commonly referred to as "store-and-forward" architectures.


RAY ALDERMAN

The laborious delays of switching and routing data packets in each node on the ring caused some bright engineer to develop "worm-hole routing" techniques to minimize the switching and routing latencies. Worm-hole routing is to the ring what cache-coherency is to the bus: a latency-management technique. If you constructed a worm farm with two sheets of glass with soil between them, you will observe that, as the worm burrows past a fixed point, the dirt will fall back into the hole as he passes by, and there's no physical evidence that he was ever there. Data packets can do the same thing in a ring.

The technique works by overlapping the address-comparison phase of packet routing with the switching latency of the incoming data. The destination address comes into the receiving interface and is immediately routed to the comparator while the FIFO is still filling up. If there's no address match, the output of the incoming FIFO is automatically routed to the output interface, even before the packet is completely received. The packet then simply goes through the incoming and outgoing connections leaving no trace that it was ever there, just like the worm burrowing through the soil. By overlapping the routing phase with the data phase, it gives the illusion that there's no routing latency, and only the switching latency remains.

However, the ring has other problems; most notably, its ability to survive. If the ring is cut at any point, or if any node interface on the ring locks up, the entire architecture will collapse. Every node in the ring is a single point of failure.

Cox Communications solved this problem with their Ring-in-Ring architecture. This architecture consists of a stack of rings connected at four points on each individual ring. Each ring maintains all the typical latencies and nefarious behaviors. But, no matter where you cut the ring, you can't kill it. The only single point of failure is a single node itself, and that doesn't affect other nodes on any of the rings. While you still have some scalability problems, survivability goes up dramatically. Some nodes in the system must now route data packets to two possible outputs (either to their own local ring or the connection to the next ring). Using worm-hole routing techniques, the routing latency is still zero, and you're left with only the switching latency. Because there's only one input channel and two possible output channels, you can't be blocked.

The only remaining problem is the scalability. The maximum number of nodes a packet must traverse on the Ring-in-Ring architecture is Ns+2+Nr, where Ns is the number of nodes between the sender and the inter-ring connection, and Nr is the number of nodes between the recipient and the inter-ring connection, unless the sender or receiver is the inter-ring node. If any of these connections are cut, or if any of the nodes between the sender and recipient fail, the formula could change significantly, or it could stay the same, depending on your position in the structure. So, any failures in the architecture make the packet latency a dynamic function dependent on your position, and which node died.

Consequently, rings aren't deterministic and they don't perform well in real-time applications. Apple and National Semiconductor developed silicon for an architecture called Quick-ring a few years ago. It had some interesting characteristics and held some promise as a low-end peripheral interface for desktop (non-deterministic) machines. Consequently, it was overcome by IEEE 1394 and USB as the peripheral interconect methodology for the desktop.

Ray Alderman is the Executive Director of VITA. He can be reached at exec@vita.com.

Embedded Designs Stack Up In Your Favor

Layering Commodity Components Helps Maximize Available Space In Compact, High-Performance Systems.

MATT ST. PETER, RadiSys Corp., 5445 NE Dawson Creek Dr., Hillsboro, OR 97124; (503) 615-1100.

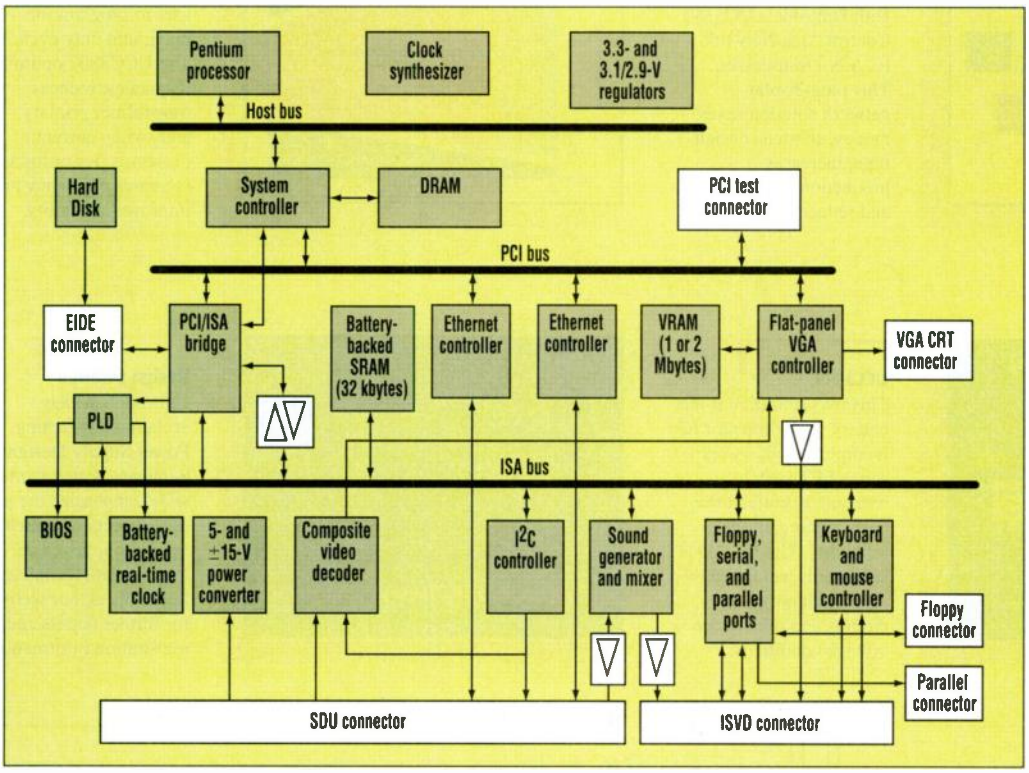
The complexity of embedded pc boards—and their often demanding size requirements—force designers to work increasingly in three dimensions. Tight enclosures often contain the same essential components as laptop computers, from power supplies and batteries to hard-disk drives and on-board memory. To accommodate the major components that comprise these systems, designers should consider thinking in three dimensions, using a layering approach, which could cut pc-board real estate in half.

A stacked-component strategy using off-the shelf PC components is possible only by overcoming three thorny issues—limited space, high heat, and interfering emissions. A host of issues must be considered in the space planning, including customer limitations, heat problems associated with smaller space, zero waste, ease of access and repair, and component selection. As far as customer limitations go, customers continually present embedded-system designers with firm size constraints. These limitations may be due to a wide variety of factors. The project may replace and upgrade an existing module, the size has already been specified by another component, a larger size can lead to high cost, and/or the enclosure resembles a battery case or glove compartment.

Regardless of the reason for the space restriction, the designer must fill all available spaces as efficiently as possible. The layout process itself is iterative and intricate—for every component, designers must map out a proposed location, consider all the mitigating factors involved in choosing that location, and rearrange any other components as necessary. They should consider every design requirement with each placement, asking these questions:

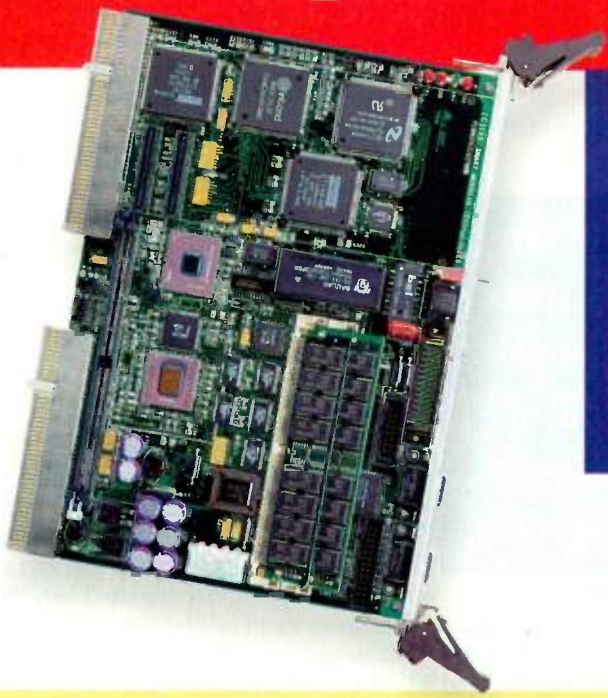
- Does the component fill the available space efficiently?
- What is its impact upon adjacent parts?
- Will any testing be required?
- If so, can the component be tested, removed, repaired, or upgraded easily?
- Does the design's assembly sequence adversely affect its placement?
- Does the design affect the production process?

Engineers creating a stacked design should start with the largest components—those that are likely to reside on the system's upper level—and work their way down to the smallest. Placing larger com-



A stackable embedded system doesn't necessarily have to be limited in its functionality. The example design, shown here, is built with a 340-Mbyte hard drive, a Pentium processor (with a heat sink), 32 Mbytes of RAM, a dc-dc converter, SoundBlaster compatibility, dual Ethernet ports, a video controller with 2 Mbytes of VRAM, a PCI bus, 26- and 44-pin connectors, a battery, and more.

PowerPC 603e CompactPCI



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ponents first quickly defines a pc's size. While that size may exceed original specifications, identifying the issue early lets engineers re-write a system's parameters or develop creative strategies for staying within them. There's no way to predict all the conflicts that will arise in a layered system, especially when size plays a significant role. Using commodity components should give designers the necessary time to consider the implications of their placement.

Smaller Equals Hotter

The general trend in this industry is to pay more for better technology. Designers must make trade-offs between cost and efficiency, or in this instance, cost and heat. Compact, embedded designs usually generate more concentrated heat.

Multimedia systems are among the most challenging, with their Pentium processors running RAM-hungry operating systems; supporting sound and video, I/O, and large disk drives. While all systems need carefully crafted cooling strategies, multimedia system designers need to account for the cumulative effects that several high-temperature components have on the rest of a system. With clever designs that work in three dimensions rather than two, more options are available.

Having identified a system's chief dimensional constraint, a preliminary design size target should be set. The final dimensions of the embedded system may change, but setting a preliminary parameter will quickly narrow the field of components considered.

Zero Wasted Space

Using a three-dimensional approach to board layout rather than the traditional 2D model forces designers to think outside of the box. Consider the following characteristics of this example: the design had no room for even a two-pin header, it employed many small outline (SO) parts on the back of the board, and full functionality had to be within a 5.2 in. by 8.3 in. by 1.0-in. enclosure.

The system comprised a 340-Mbyte hard drive, a Pentium processor (with a heat sink), 32 Mbytes of RAM, a dc-dc converter, SoundBlaster compatibility, dual Ethernet ports, a video controller with 2 Mbytes of VRAM, a PCI bus, 26- and 44-pin connectors, a battery, and more *(see the figure)*.

Here are some of the shortcuts used:

- The hard drive floats over several low-emission chips;
- The dc-dc converter floats over several less-sensitive chips;
- The SO-DIMMs float over several chips;
- The Pentium's heat sink curls over other components;
- The BGA chips are in the middle by themselves.

Regardless of the reason for the space restriction, the designer must fill all available spaces as efficiently as possible.

One key to efficient 3D layout is taking into consideration the four phases of a project: prototyping and testing, troubleshooting and debugging, replacement and repair, and standard operation. By taking advantage of removable components, such as the disk drive, RAM, and CPU-heat sink, technicians can access all areas necessary.

At some point, the designer will need to attach an in-circuit emulator or analysis module to the processor (there must be enough room for the instrument and its cabling). Without good planning, attaching a probe to the processor without running into the power supply may be impossible. That could require changing the location of other parts just to finish testing.

Fine-pitch components also can pose access problems. These parts include SQFPs, TSOPs, and high pin-count PQFPs. Before placement, it's important to consider their reliability, the likelihood of their future replacement, and any harsh conditions under which they must operate.

As embedded designs shrink in size, it is reasonable to expect a greater use of ball-grid arrays (BGAs), for a number of reasons. The solder-ball matrices have larger features than larger fine-pitch components. Because they're built on a small pc board, their thermal expansion can match that of the main circuit board. Also, BGAs are only 0.1-in. high, leaving plenty of room in a system with tight dimensions. However, BGAs have a potential downside—removing them requires a concentrated blast of hot air to melt their solder.

Some components in a stacked design are so large that they mask others. Power supplies fit into this category, as do batteries. In such cases, engineers can wire these components off the board during debugging. They also may consider bolt-on versions of these large components.

Component Selection

It's impossible to overstate the value of gauging component reliability before selection. Designers should consider all the stresses that will befall a system on the production line and in its operating environment. Then the designer must adjust the placement strategies accordingly.

For instance, the example multimedia player's DRAM modules are available in only a few sizes. Vertical-module sockets were quickly dismissed. At more than 1-in. high, they were above the 0.5-in. limit. To maximize the board's real estate, the memory modules would mount at right angles. That approach reduced the possibilities to a dual 72-pin socket and a single 144-pin socket.

As the component-selection process moves forward in this fashion, other considerations can arise and trade-offs will undoubtedly occur. A smaller hard drive could be used, but its price may drive the system's total cost beyond acceptable limits.

High Heat

The issues that affect heat planning include placement of the hard drive and microprocessor, fans vs. heat sinks, side effects, and power-management software. Heat is the single most important factor in decreasing the reliability of most pc-compatible compo-

nents. Controlling heat will be an even greater challenge when the product is shrunk to half its usual size.

One of the most critical placement considerations involves the relationship between the disk drive and the CPU. In addition to a sensitivity to strong EMI fields, the drive has restrictive heat specifications. Placing it above, or even near, a Pentium-class processor in a tight space, especially one with little or no ventilation, could reduce the drive's reliability.

These two large components greatly influence the layout and layering of a stacked design. A system's 2.5- or 1.8-in. hard drive can become an issue almost immediately, especially when accompanied by a 2.2-in. by 2.2-in. dc-to-dc converter. But because these parts are shorter than 0.5 in., they can float above shorter board components.

To place the components properly, first sort them by size, then by the likelihood of their layering. Processors and DRAM, for example, are larger parts, but they must be anchored to a board. But disk drives, batteries, and power supplies don't generally suffer such limitations.

Components with a high likelihood of layering generally fall into two categories—those that can be stacked without regard to the circuitry underneath and those that consume most or all of the available vertical space, thereby limiting or eliminating the possibility of placing any other parts beneath them.

Fans Vs. Heat Sinks

Forced air cooling is not a consideration for many embedded systems. Noise, unreliability, power drain, and inefficiency are some of the main problems. Designers have various heat-sink choices to investigate, such as different metals and fans, or bolting the sink to the enclosure.

The design's size also may negate the use of a fan. The enclosure may be too small to accommodate one. Or the enclosure must remain sealed to function properly. And, even if using a fan is an option, a system's operational environment might not make it advisable. For example, a fan could pull excess dust into an enclosure.

Convection is another strategy for cooling an embedded design, though this approach still assumes some airflow. Even if caused only by heat cycles, the design will still depend on some internal air movement to carry the heat away from the components to the enclosure. While this approach is feasible in some environments, such as those with low power and room for air to circulate, it might not be appropriate for others.

Another heat-reduction strategy is conduction. A designer can bolt components to casings, use certain metals to accelerate heat transfer, or vary the thickness of an enclosure to conduct heat away from a design. Some smaller components could dissipate their heat directly into the printed circuit board.

Side Effects

Stacking components in a small enclosure might satisfy the size and operational criteria, however, it also can introduce or exaggerate some behaviors. These side-effects include excess heat, vibration, pressure, and electrical interference.

Compact embedded systems generate heat. Even low-voltage Pentium-class chips produce a significant amount of heat, given a small enough space, a high enough clock speed, and minimal ventilation. While judicious component placement may help mitigate these effects, other heat-reduction strategies may be necessary.

For example, assume the dc-dc power supply module with an efficiency of 75%, and its buck regulators at 92% produce about 5 W. Because the power supply generates most of that heat, designers could consider bolting it to the enclosure's lid. Another strategy might be to place a piece of aluminum above the converter to conduct its heat directly to the lid and accelerate heat dissipation.

Power-Management Software

Whenever possible, designers should always integrate software-based power management into heat-reduction strategies. For example, there's no reason for a multimedia player's processor to operate during a movie. The VGA controller handles playback on-the-fly. So, an efficient design could reduce heat by ensuring that the processor is powered up only when necessary.

BIOS-level power management is generally not as efficient as application-specific power management. The software engineer designing the application knows better than the BIOS which sections are required to complete a task, and can therefore, better predict when the hardware can safely power down.

Interfering Emissions

Emissions planning is most directly affected by noisy ICs, vibration, and electrical interference. In an embedded system, there are generally plenty of fields to go around. Despite an operating efficiency of 80%, even a decent power supply produces considerable radiation. Nearby buck regulators also produce their own magnetic fields.

Sometimes a different component—one that still meets a design's size targets—can lessen EMI effects. Using buck regulators with toroidal- instead of bobbin-style coils, for instance, produces less radiation.

There will be times when components are simply too sensitive to place near a magnetic field of any significance. Hard drives fall into this category, as do video decoders and some audio circuitry. In this case, designers should consider floating a field-producing component such as a power supply above one that is insensitive to its effects, such as VRAM.

Small, stacked designs can exaggerate the effects of low-frequency vibration. Designers should add up the tolerances of their vertical components to check a system's susceptibility to vibration. If it's particularly sensitive, turn to brackets, bolts, or shock absorbers to hold components in place.

Rigid mounting is often found to be more reliable than padding, which can cause secondary vibration problems. When a bolt-in version of the drive is not available, try a press-fit bracket to attach the drive to the enclosure. As noted earlier, brackets offer the additional benefit of conducting heat to the system's enclosure.

Finally, as the distance between the enclosure and its components shrinks, designers should consider the potential for electrical shorting. While SOICs have plastic to protect them, the metal contacts on some resistors, capacitors, and through-hole components do not. To alleviate the possibility of dangerous shorts, choose strategic locations for plastic inductors around the pc board. In the event of any incidental pressure, they would

serve as braces against the case lid. This protection from shorts to the case could reduce the distance between the pc and case lid by another 0.1 in.

Electrical Interference

With mouse, network, and other communications lines, some embedded systems can be a cabling nightmare. A multimedia player could require 24 separate wires just for the video. Many embedded systems must meet strict standards for electrical interference, making connecting components that much more challenging.

One way of untangling the cabling problem elegantly, while reducing the chances of electrical interference, is to use low-voltage differential signaling (LVDS). For example, LVDS will convert the 24 video wires into four twisted pairs multiplexed at 180 MHz. This approach cuts interference with sensitive electrical instruments because the sum of the signals running up and down the twisted pair is zero. LVDS also eliminates the loop currents associated with creating a common ground for 24 wires.

Designers also might consider electronically sealing the seams of their embedded-system enclosures to reduce electrical interference. This sealing, as opposed to simple overlapping, can reduce the chances of stray electrical noise from escaping.

Consider that layered, three-dimensional designs require teamwork between engineering and manufacturing. After examining size, dependencies, relationships to circuitry, and access issues, manufacturing engineers must review a design's assembly sequence. It may preclude a particular component arrangement. Production engineers who will construct the embedded system also should offer their perspective, one that could streamline or reduce the cost of manufacturing a design.

Matt St. Peter is a hardware manager with RadiSys Corp. He holds a Master's in Computer and Information Sciences and a BSEE from the University of Delaware.

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WHAT'S ON BOARD

Serving notice to the PC industry, PCtel Inc., Milpitas, Calif., has announced approval on the first of a dozen patents applied for that relate to its host-based signal-processing modem technology. Already used in over two million PCs, the HSP-based modem allows users to upgrade the modem by just installing new software. This allows PC manufacturers to embed the low-cost modem front end circuitry right onto the motherboard. The patent covers the execution of the soft-modem function in a multitasking environment. The HSP modem takes advantage of today's advanced CPUs, such as the Intel Pentium II with MMX technology, to provide a software-based solution with more flexibility than a general-purpose DSP or a dedicated modem chip. The software supports data rates up to 33.6 kbits/s. A future upgrade will permit 56 kbit/s data rates. Drivers are available for Windows 3.11, Windows 95, and Windows NT 4.0. Contact Shawn Owens, (408) 383-0452, or on the World Wide Web at *http://www.pctel.com.*

In another soft-modem development, Smart Link Technologies Inc., Milpitas, Calif., has designed modem-control software that works in conjunction with the CrystalClear audio chip from Cirrus Logic to provide a low-cost single-chip modem solution. When used with the sound chip, the Modio software allows users to add modem, fax, and telephony features to a system for just $15. The software taps the unused processing power of the host CPU for modem signal processing. Data can be transferred four times faster than a hardware modem since the software modem is not constrained by the UART typically embedded in hardware modems. In addition, Modio takes advantage of Cirrus Logic audio components to provide an integrated audio solution with SoundBlaster Pro and AdLib/OPL3, Windows Sound System, and DirectSound compatibility. Contact Peter Tsepeleff, (408) 941-7900, or on the World Wide Web at *http://www.smlink.com.*

With a peak data-transfer rate up to 1.56 Gbits/s, a transmitter and receiver chip set from Sony Semiconductor Company of America, San Jose, Calif., allows designers to locate high-resolution displays up to 10 m from a host system with just a single twisted-wire pair. The CSB1451Q and CXB1452Q provide a long-distance cable alternative for VGA, SVGA, XGA, and SXGA data bandwidths versus competitive products that support cable lengths of 3 m or less, and require at least four cables. The chip set uses an ultra-high-speed 1-bit differential serial data port to transmit 18-bit color VGA/SVGA/XGA images or 9-bit color SXGA image data without compression or encoding. The chips support 1 pixel/shiftclock or 2 pixels/shiftclock and have all the functions required for operation: serializer, deserializer, cable driver, and cable equalizer. The equalizer adjusts the receiver gain automatically to accommodate cables of different impedances and lengths. The CXB1451Q consumes 0.8 W, while the receiver chip consumes about 1 W, both when powered by 3.3 V. The chips are housed in 180-lead PQFPs and sell for $9.90 apiece in 1000-unit lots. Contact Jean-Pierre Laussade, (408) 955-6572, or on the World Wide Web at *http://www.sony.com/semi.*

Dropping the operating read voltage to the lowest level yet for a high-density flash memory, SGS-Thomson Microelectronics, Lincoln, Mass., has released a 1.8-V, 8-Mbit memory. Hardware- and software-compatible with AMD flash memory chips and hardware-compatible with Intel flash products—the M29R800 (by-8 or by-16 pin-switchable) or M29R008 (by-8 only)—the memory reduces power drain in portable embedded systems such as cell-phones, pagers, and modems. For program and erase functions, the memory requires 2.7 to 3.6 V, but data can be read from the memory with supplies from 1.8 to 3.6 V, versus the 2.2 V or higher required by other memories. The flash memory includes an automatic standby mode that waits for an inactive bus period of 150 ns and then switches to a standby mode that drops the current to 1 µA. The chips feature optional dual boot blocks and standard sector protect and temporary unprotect functions, plus a customizable one-time programmable ROM array for storing security information. Samples are immediately available and sell for $12 apiece in 10,000-unit lots; the M29R008, whose price has not been set, will be available early next year. Contact Philippe Berge, (617) 259-0300, or on the World Wide Web at *http://www.st.com.*

VME64 Board Is Powered By A 200-MHz TurboSparc CPU

The Sparc 8/64 is an I/O-extended version of Sun's SparcStation 5, Model 170 workstation. The computer board combines a 170- or 200-MHz TurboSparc processor with a VME64 interface, dual Ethernet ports, and dual fast SCSI 2 interfaces. Mixing this level of performance with the the redundant I/O results in a platform suited for telecommunications and ruggedized COTS applications. Up to 256 Mbytes of DRAM can be employed using stackable, screw-down modules.

Other features include two SBus expansion slots, a parallel and two serial ports, and keyboard and mouse connections. By maintaining the Sparc compatibility, the board can run any of the thousands of Solaris 1.x and 2.x off-the-shelf software solutions. The Sparc 8/64 also runs the VxWorks 5.3 and Tornado real-time operating systems. The board also is available with a 110-MHz microSparc II processor.

Themis Computer, *3185 Larelview Ct., Fremont, CA 94538; (510) 252-0870; http://www.themis.com.*

CIRCLE 548

Digital-Audio Board Encodes In Real Time

The Falcon-563 is a digital-audio board that fits the half-size PCI bus form factor. Based on a Motorola DSP56301 chip, the board performs two-channel Dolby AC-3 encoding in real-time on a standard PC. On-board receivers and transmitters support AES/EBU and S/PDIF formats, making it suitable for professional and consumer digital-audio applications. The board accepts a SMPTE time-code input signal, allowing accurate encoding start and stop times, while also supplying time-code reference stamps within the recorded disk file. Bundled software allows for development under the Windows 95 or Windows NT operating system.

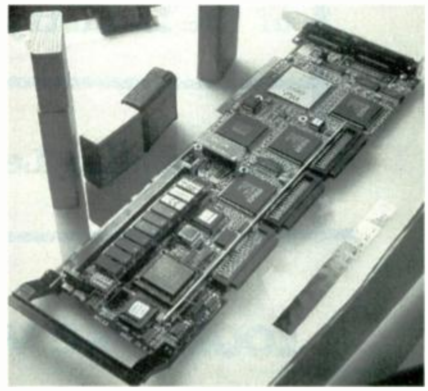
Momentum Data Systems, *17330 Brookhurst St., Suite 140, Fountain Valley, CA 92708; (714) 378-5805; http://www.mds.com.* **CIRCLE 549**

RAID Level 5 Controller Handles 2400 I/O Transactions Per Second

OEMs can develop high-end enterprise-level servers and storage subsystems using the DAC960PJ RAID level 5 controller, developed by Mylex Corp. The board boasts a throughput of 2400 I/O transactions/s. The high level of performance is attained by combining a 66-MHz i960RD processor with the company's 86238 RAID controller chip. In addition, a monolithic Windows NT driver helps increase overall system throughput.

A background initialization feature enable setup tasks to be performed while the rest of the system is being configured. This can be a major time saver if multi-gigabyte hard-disk drives are employed. A BIOS configuration utility enables automatic system setup, independent of the operating system and without the need for any external software utilities.

A RAID expansion feature lets users add drives to existing arrays



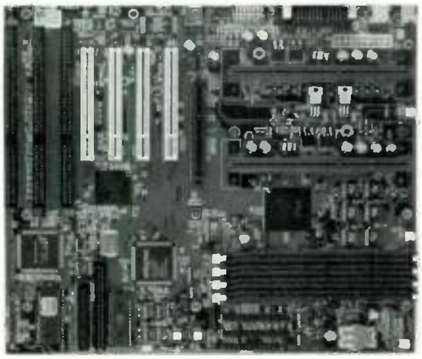
and re-stripe the data across all drives. Users than can opt to use the additional storage space to expand the capacity of the existing logical drive or to create a new logical drive. The RAID migration allows easy reconstruction of data from one RAID configuration to another. A RAID 0 configuration can be migrated to a RAID 5 while the server stays online. Lastly, the built-in copy-drive-group feature allows users to transfer the contents of one logical drive to another in one step.

The DAC960PJ RAID level 5 controller supports PCI hot plug, which lets the user manage or replace a controller without taking down the server. Evaluation units are available now. Volume shipments are planned for the first quarter of next year. One-, two-, and three-channel configurations are available. Prices range from $1050 to $1350 each in large quantities.

Mylex Corp.
34551 Ardenwood Blvd.
Fremont, CA 94555
(510) 796-6100
http://www.mylex.com
CIRCLE 494
RICHARD NASS

Motherboards Support Pentium II and AGP

A family of six motherboards offers two key features—they're built with Pentium II microprocessors and they support the Advanced Graphics Port (AGP). Based on Intel's 440LX chip



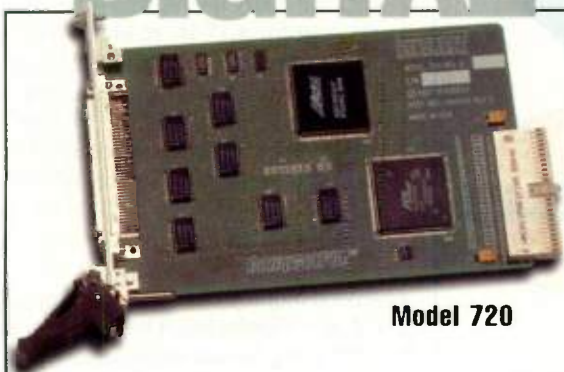
set, the motherboards' processor can run from 233 to 300 MHz. Other features include EDO and SDRAM support, 33-MHz Ultra DMA, and Wake-on-LAN capability. The boards are built with the Leadtek Research Win-Fast 3D L2300 AGP accelerator. The AGP bus provides a direct interface to main memory without burdening the CPU bus. The motherboards support the 2X specification for transfers up to 532 Mbytes/s. They run Windows 95 or Windows NT. The models P6SLE, P6SLA, and P6SLS are single-CPU boards, while the P6DLF, P6DLS, and P6DLH are dual-CPU boards. The P6DLH is I_2O-ready with a built-in I960 processor. The other differences are in the boards' form factors and the amount of memory they can support. In 1000-unit lots, prices run from $300 to $800. All are available immediately.

***Supermicro Computers Inc.**, 2051 Junction Ave., San Jose, CA 95131; (408) 895-2000; http://www.supermicro.com.* **CIRCLE 495**

3.5-In. Hard Disk Drive Raises Bar To 20 Gbytes

The push toward higher disk-drive capacities seems endless. The latest example is the Tomahawk AV Gold 20, which stores 20 Gbytes in a 3.5-in. form factor. Aimed at high-end audio and video applications, the drive is available with an Ultra SCSI or Ultra2 LVD SCSI interface, resulting in a transfer rate up to 80 Mbytes/s and a cable length up to 12 m. The Tomahawk AV Gold 20 offers a spindle speed of 7200 rpm, a 7.9-ms average seek time, and an internal data rate of 180 Mbits/s. In addition to the magneto-resistive (MR) heads and digital PRML data channel, the drive features a proprietary hybrid servo technology, which increases the accuracy of the track following as well as the drive's durability. A 2-Mbyte cache buffer increases the error-recovery margin while increasing performance. Evaluation units of the Tomahawk AV Gold 20 20-Gbyte disk drive are available now for $2245. Large volumes will be available in the first quarter of next year.

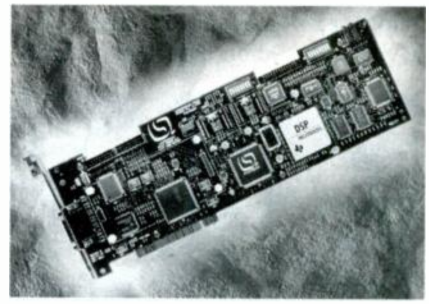
***Micropolis Inc.**, 21211 Nordhoff St., Chatsworth, CA 91311; (818) 709-3300; http://www.micropolis.com.* **CIRCLE 496**



DSP Board Saddles Latest TI Processor

The latest in DSP chips, the TI TMS320C6201, forms the basis of the PCI/C6200 board suited for high-end embedded environments, such as voice processing and speech recognition. The board, built with a PCI interface, supplies 1600 MIPS of processor power using the 200-MHz DSP chip.

The PCI/C6200 is available with a host of development and debugging software, which lets designers rapidly build complete DSP-based systems. Bundled host-communication software provides control, download and data transfer, host-based DMA, signals, and mailboxes. Other available software includes host and C6200 interface libraries, a core I/O library that supports the configuration of the MVIP and SCbus interfaces, and a boot loader. The board's compiler makes maximum use of the C6x chip's parallel execution capabilities, allowing up to eight instructions to be per-



formed simultaneously. Supported operating systems include Windows 95 and Windows NT.

The DSP board contains a site for an analog I/O module for user customization. It's also built with a 132-Mbyte/s PCI host interface and can handle up to 8 Mbytes of SDRAM. Available immediately, prices for the PCI/C6200 start at $3000.

Loughborough Sound Images Inc., *70 Westview St., Lexington, MA 02173; (617) 860-9020; http://www.lsi-dsp.com.*
CIRCLE 497

Can't Afford A 21? Try A 19 On For Size

The cost of a 21-in. display is often too high for many users, who often end up settling for a 17-in. model. To fill the gap between the 17's and 21's is the VS-19, a 19-in. display that boasts a viewable area of 18.8 in. The key feature of the VS-19 is its horizontal scanning frequency—95 kHz, which results in a resolution of 1600 by 1200 pixels at a 75-Hz refresh rate. The monitor offers a 0.28-mm dot pitch, on-screen display controls, and universal voltage regulation. The high-contrast CRT includes an invar shadow mask and nonglare, anti-static treated glass. It meets the Swedish MPR-II standard for low radiation emissions, and its energy efficiency rating is in compliance with the Energy Star and VESA DPMS standards. Available now for both PCs and Macs, the VS-19 display retails for $999.

KDS USA, *12300 Edison Way, Garden Grove, CA 92841; (714) 379-5599; http://www.kdsusa.com.*
CIRCLE 498


New!
Embedded Target System
with on board Ethernet.
intel

Carrier Boards Employ Latest DSP CPUs

A pair of carrier boards, the Monaco and the Daytona, are built with the latest DSP chips from TI, the TMS320C6x. The Monaco is a quad-VME board, while the Daytona is a dual-PCI board. The Monaco board can hold four 200-MHz processors, each with its own bank of 800-Mbyte/s synchronous burst SRAM and another bank of 400-Mbyte/s synchronous DRAM. There's also a bank of SRAM that's shared globally. With its VME64 architecture, the board is suited for communications applications. The architecture allows for four independent, high-speed, bidirectional data-flow channels between standard mezzanine boards and each of the four DSPs. The Daytona board has room for two DSP chips, which are arranged in a shared-memory architecture. The on-board PCI interface can sustain 130-Mbyte/s block transfers. The Monaco board will be available in the first quarter of 1998, while the Daytona will follow that by one quarter.

***Spectrum Signal Processing**, 8525 Baxter Pl., 100 Production Ct., Burnaby, BC, Canada V5A 4V7; (604) 421-5422; http://www.spectrumsignal.com.*
CIRCLE 499

Accelerator Speeds Graphics, Gaming, Digital Video

The Viper V330, a 128-bit media accelerator, is intended for both business users and gamers. Featuring NVIDIA's RIVA 128 media controller, the Viper offers excellent 2D, 3D, and digital video playback performance. Populated with 4MB of 100-MHz SGRAM, the Viper couples the 128-bit graphics engine with a 128-bit data path to memory. Other features include a TV-output capability, full-screen MPEG-1 video playback, and multimonitor support. The board also can be upgraded to support DVD, and allows television viewing and video capturing using an optional Diamond TV-tuner capture card. In 2D testing, the accelerator earned scores of 140 million WinMarks for Windows 95 and 130 million WinMarks for Windows NT. In 3D testing, it yielded a score of over 225 3D WinMarks. By off-loading intensive processing from the host CPU, the Viper lets the PC perform 2D and 3D multi-

(continued on page 110)

(continued from page 108)
media functions in tandem without hindering overall system performance. The board can display resolutions up to 1600 by 1200 pixels, with color depths up to 32-bit true color. A 230-MHz RAMDAC enables flicker-free refresh rates.

The Viper enables full-motion digital-video playback, with frame rates as high as 30 frames/s. The accelerator combines key hardware-based video functions, including support for DirectDraw and DirectVideo in Windows 95, image scaling, color-space conversion, and filtering. The board comes bundled with a host of games and business productivity software, as well as the InControl Tools 95 desktop utility software, which lets users make on-the-fly adjustments for display resolution and color depth. Available now, the Viper sells for under $200.

***Diamond Multimedia Systems Inc.**, 2880 Junction Ave., San Jose, CA 95134; (408) 325-7000; http://www.diamondmm.com.* **CIRCLE 500**

Software Hastens PowerPC Product Development

To ensure prompt, efficient software development for next-generation PowerPC processors, developers can take advantage of SingleStep Solutions, an integrated software development environment for the PowerPC 750 and 740 microprocessors. Running on Unix and Windows host platforms, the software incorporates advanced instruction-set simulation and distributed emulation capabilities, as well as a comprehensive suite of debugging tools. Embedded developers can get an early start on their designs, then verify hardware prototypes using the SingleStep Distributed Emulation Solution for Hewlett-Packard's Processor Probe.

"Point and click" kernel awareness is included for over a dozen commercial real-time operating-system kernels, including Nucleus, OSE, pSOSystem, RTEK, RTXC, and VxWorks. The tools offer the native look-and-feel under both Windows (3.1, 95, and NT) and UNIX (HP-UX, Solaris, and SunOS) and include on-line help. The SingleStep start at $2000 for Sun, Solaris and HP-UX workstations and $1500 for Microsoft Windows NT and Windows 95 workstations. C and C++ compilers integrated with SingleStep for the PowerPC 700 are available for Sun, Solaris and HP-UX based workstations starting at $4400 and for Windows NT and Windows 95 platforms starting at $2200.

***Software Development Systems**, 815 Commerce Drive, Oak Brook, IL 60521; (708) 368-0400.* **CIRCLE 501**

Multi-Sharc Board Bridges Up To C40 Peripherals

VME system designers using Sharc-based DSP boards now can choose from a host of high-performance I/O peripherals, thanks to the 4288 I/O intensive SHARC-based VMEbus processor board. The board offers expansive data throughput and interface options, compatibility with multivendor heterogeneous DSP systems, and on-board scalable processing power. The 4288 is built with a main Sharc processor, a SharcPac mezzanine site, the MIX mezzanine bus (up to three stacking modules), Sharc link ports, TMS320C40 communication ports, an on-board PowerQUICC controller, a VME64 master-slave interface, and an Ethernet interface.

The heart of the 4288 is its 40-MHz AD21062 processor, which delivers up to 120 MFLOPS and has connectivity to all of the major I/O paths and memory resources including a 2-Mbyte VMEbus spooler SRAM. The SharcPac mezzanine module holds up to six processors. For high-end DSP applications, the 4288 can be employed as an I/O subsystem to support other Sharc processor boards. Ten 40-Mbyte/s Sharc link ports are brought out to the front panel, providing high-speed data paths to other Sharc boards in the system. Additional link ports are routed internally between the main Sharc, the SharcPac site, and the PowerQUICC. Optionally, three link ports from the SharcPac site may be brought to P2 connector.

Suitable applications for the 4288 include radar, sonar, echo cancellation, telecom and multimedia systems, as well as general-purpose signal-processing applications such as FFTs, sonar and radar processing, medical imaging, demodulation, and digital filtering. The 4288 Multi-Sharc I/O processor starts at $6495, with production slated for the first quarter of 1998.

***Pentek Inc.**, One Park Way, Upper Saddle River, NJ 07458; (201) 818-5900; http://www.pentek.com.* **CIRCLE 502**

New Challenges Place Power Squarely In The Spotlight

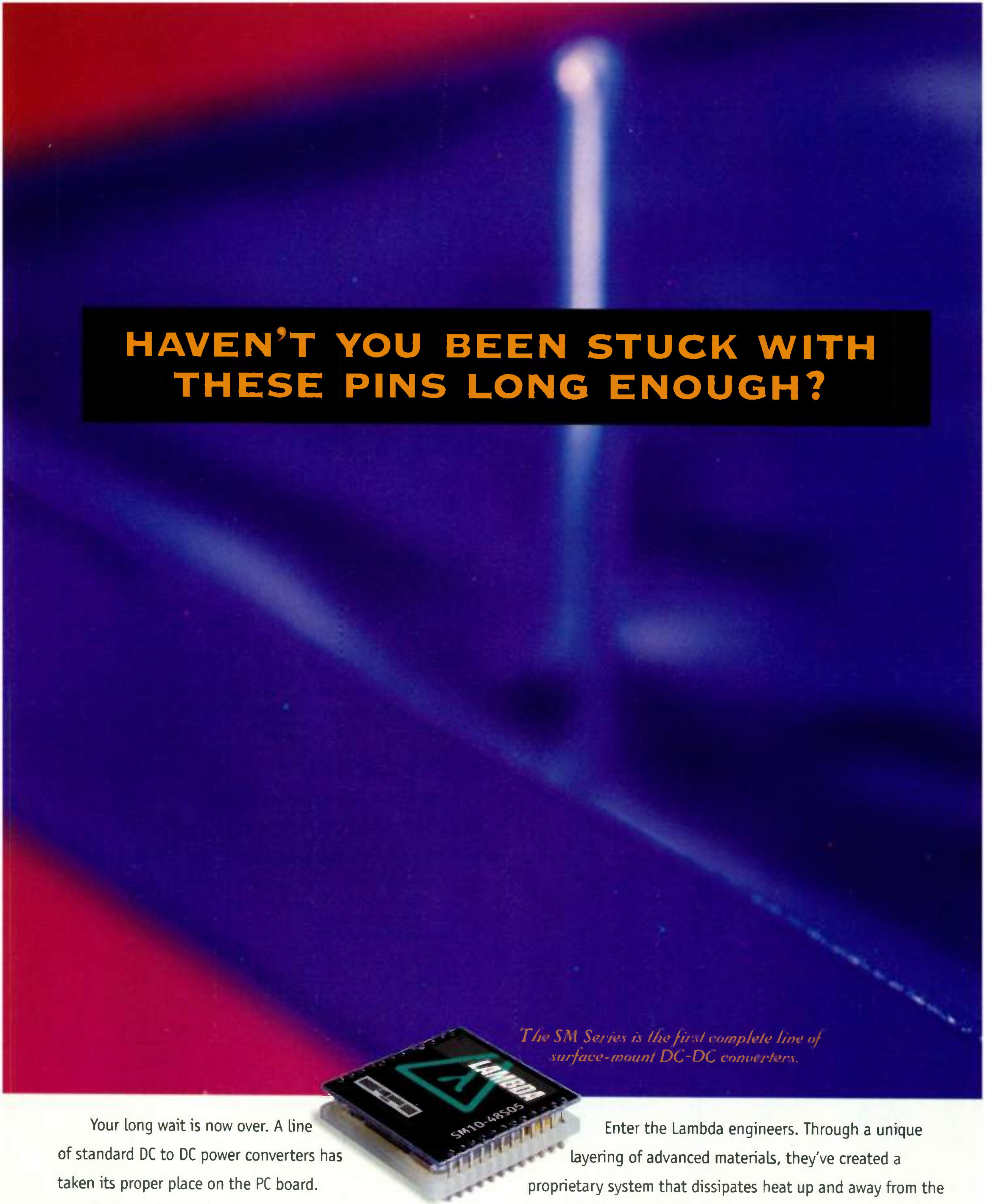
A Number Of Recent Advances, Both Technical And Political, Have Shoved Power To The Forefront Of Electronic Systems Design.

BY PATRICK MANNION
Power, Packaging, Components and Optoelectronics Editor

Welcome to *Electronic Design's* first Power Technology Focus. Borne of a need to bring power-supply manufacturers, designers, and users together on a common platform, the Power Technology Focus presents a wide-angle view of the issues and problems facing power designers, now and in the near future. Ranging from the concrete (designing a distributed power system) to the abstract (European Directives), the articles all have one thing in common—they are designed to leave the reader with a clearer understanding of what it will take to design, or design in, a power supply that will carry a system well into the next millennium. Additionally, the focus here is on the manner in which peripheral developments, both technological and political, have conspired to shove power design closer to the forefront of the design process.

For many years, core technologies such as power have covered the back end of the design process, which was fine as long as power just meant having 5 V where you needed it. Now, the power supply faces the challenge of out-

TRENDS AND SOLUTIONS



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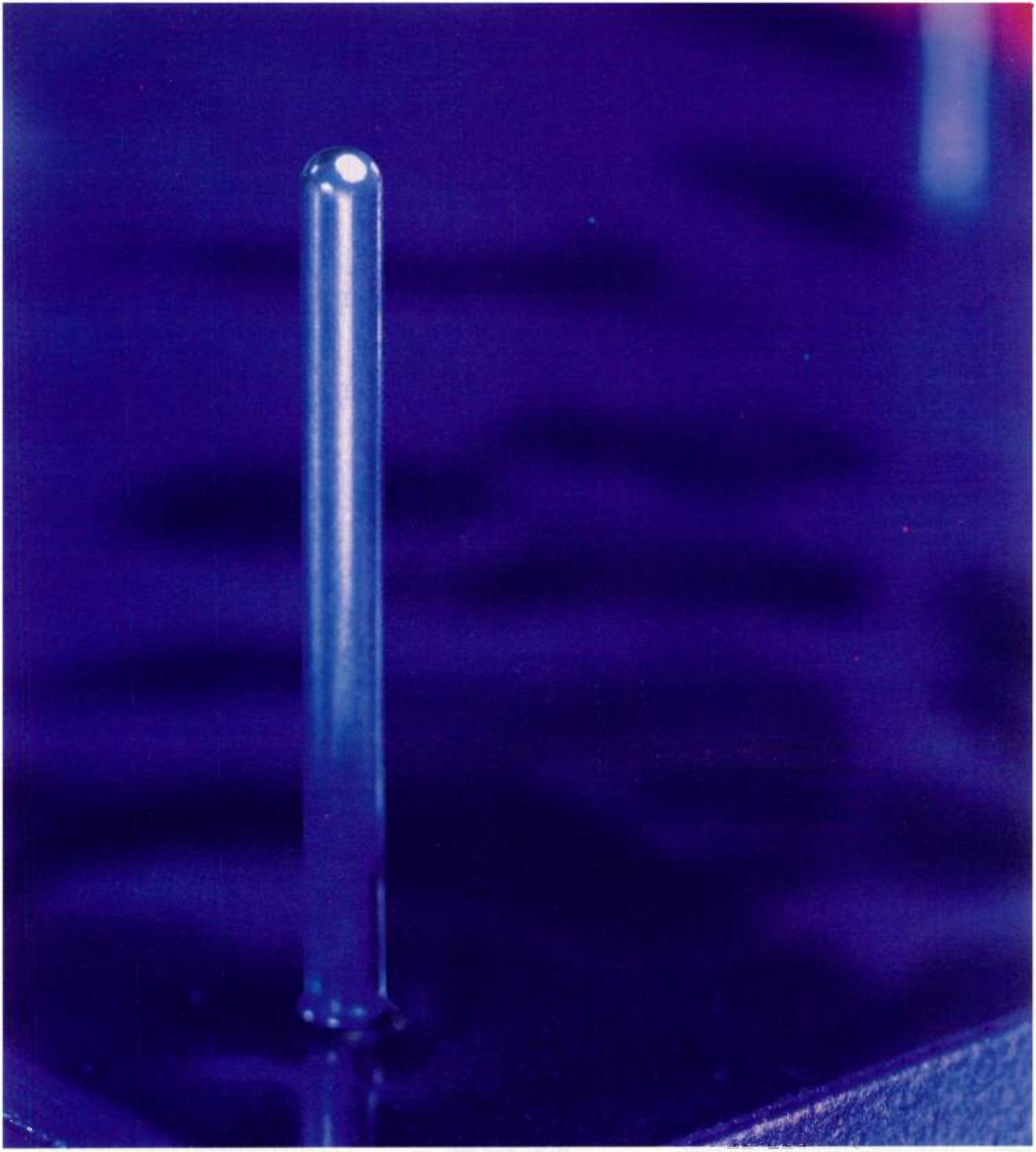
(We'd be happy to go into more detail, but then it wouldn't be proprietary anymore.)

So we've eliminated the need to manually place and solder through-hole converters.



putting higher power, at lower voltages, from a smaller footprint, and with massive current transients. And they must do this while becoming safer, more reliable, cheaper, and more accurate.

Along with these technical challenges, power-supply manufacturers are now having to deal with less-concrete factors as they target the European market. Here, a push for a common standard has resulted a new set of standards called the European Directives. While these requirements can be met technically, at issue are the cost of compliance and CENELEC's (European Committee for Electrotechnical Standardization) inability to outline a final standard and define a set date for compliance.

The Directives have evolved into such a Gordion Knot that many believe they do more harm than good. To comply, designers must first decide into which category their product falls—industrial, residential, commercial etc. Thanks to many subtle differentiators and gradations, categorization is not so easy. Designers must then search for an up-to-date version of the standard and hope that standard still applies, in its original form, when the final product is shipped.

If you're looking to initiate compliance right away, but don't know where to start, Intertek Testing Services, Cortland, N.Y., can assess your situation. Reach them at (800)-WorldLab. If you already know the standard you need to conform to, but don't have an up-to-date version of the specification, call Compliance Engineering of Andover, Mass., at (508) 681-6673 and ask for Patricia LeBlanc.

With compliance-enforcement dates slipping beyond the year 2000, many power-supply and system designers are in somewhat of a quandry when it comes to justifying the expense of Euro compliance today. For many, it may be beneficial to wait for high volumes to push the cost of compliance down. According to Laurence Bloom of Venture Development Corp. (VDC), a technology research firm out of Natick, Mass., the number of OEMs that required PFC supplies in 1996 was 56.3%. VDC expects this percentage to rise to 75.7% by 2001. As PFC is one of the most expensive hurdles to Euro compliance, the higher volumes should go a long way toward bringing the cost of Euro compliance down. For more information on the European Directives and how to comply, see the article from Don Mulvey of dpa Solutions, Ronkonkoma, N.Y., entitled *"Modular Front Ends Tackle Harmonization Issues,"* on page 155.

Technical Challenges

After tracking down and finalizing your design parameters and specifications, you must now get a handle on power-supply trends and requirements. Take a look at *"Flexible Supplies Build Fast Track To Optimum Power,"* on page 118, from John Carroll of Lambda Electronics Inc., Melville, N.Y. Among other topics, this article will compare a centralized architecture with a distributed one.

Should you decide to opt for the latter, Lars Thorsell of Ericsson Components, Stockholm, Sweden, will remind you why you did so, applaude your wisdom, and guide you through the design process in his article *"Distributed Power Architectures Enter The Mainstream,"* on page 127. If redundancy and hot swapping are in your future, Paul O'Boyle and Steve Kugler of Kepco Inc., Flushing, N.Y., would like you to benefit from their experience through their article *"Redundancy And Hot Swapping Keep Systems Running,"* on page 134.

Noise And EMI

Noise and EMI are in everyone's future, unfortunately. However, in *"Reducing Noise And EMI In Distributed Power Systems,"* on page 166, Gabriel Suranyi of Lucent Technologies, Microelectronics Group, Mesquite, Texas, provides some practical, back-to-basics advice for reducing them to a manageable level.

Closely linked to noise and EMI is the issue of transient response with high-end processors. Lazar Rozenblat of Todd Products Corp., Brentwood, N.Y., meets the challenge head on in *"Understanding The Transient Response Of A Switch-Mode Supply,"* on page 161.

Power Backup

The familiar external UPS is having to justify its market-leading position lately, as it squares up against a number of new internal designs from the likes of Amsdell, Richmond Hill, Ontario, Canada (see the Product Feature *"Inverter Forms Core Of Miniature UPS/SMPS Combo,"* on page 183), and Technology Dynamics, Bergenfield, N.J.

According to Mishaal Naik, senior strategic officer at Amsdell, the day of the internal UPS has arrived, thanks to very high levels of integration and falling component costs. Of course, Chris Tecca, representing American Power Conversion, West Kingston, R.I., a leading manufacturer of external UPSs, takes exception to this. He argues that embedding a UPS handicaps the user when it comes time to upgrade a system. He also questions the feasability of having a battery, which is guaranteed to fail at some stage, embedded within a system. Aron Levy, president of Technology Dynamics, makes some very good points in his take on the situation in *"DC UPS Provides Alternate Backup Solution,"* on page 142.

External UPSs are having to justify their market-leading position as they square up against a number of new internal design options.

Down And Dirty

If some solid electronic design sounds like a refreshing change, turn to page 173 where Don Comiskey of Power Trends, Warrenville, Ill., will regale you with ideas for the lowly integrated switching regulator in his article *"ISR Transforms Into A Versatile Power Source."* In addition, *"Linear Power-Supply Module Comes Complete,"* on page 182, announces the linear supply's answer to the dc-dc converter. The miniature module contains everything needed to roll-your-own linear supply.

We hope that this insight into the world of power makes your upcoming design flow a little easier. If there are any topics you would like to see highlighted in the next Power Technology Focus, please don't hesitate to contact me at (201) 393-6097, or e-mail me at pmannion@penton.com.

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READER SERVICE 165

Flexible Supplies Build Fast Track To Optimum Power

Despite Increasing Cost Pressures, Power Supplies Must Deliver Higher Power, At Lower Voltages, In Feature-Rich, Flexible Configurations.

BY JOHN CARROLL

Lambda Electronics Inc., 515 Broad Hollow Rd., Melville, NY; (516) 694-4200; fax: (516) 752-2627.

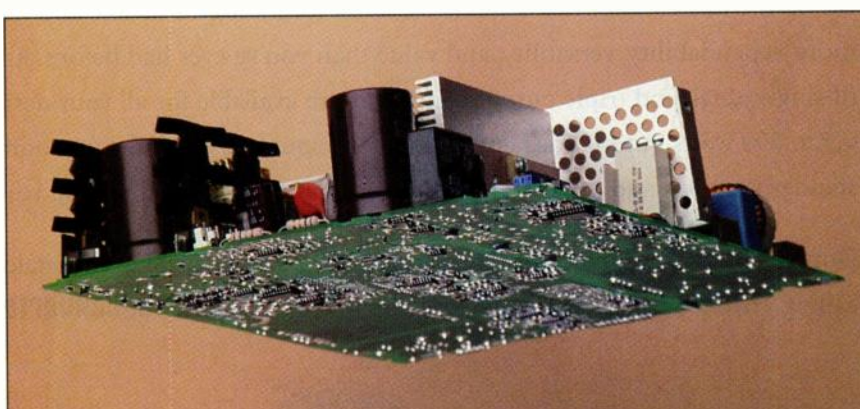
Along with the rapid development of power solutions for high-end processors, there also have been significant developments in system-level power architectures for applications such as embedded-processor equipment, workstations, card cages, enclosures, racks, and backplane equipment. As in the chip-level arena, these developments have been driven, in part, by requirements for lower output voltages at increased power levels for system logic and memory.

The changes also are being driven by requests for auxiliary outputs to handle greater system demands, and to reduce the use of multiple power supplies. In addition, as computer technology permeates the critical financial, communication, industrial, and data-processing arenas, more signaling and safety features are being added to enhance system reliability.

While these additions work well for the power-supply end user, power-supply manufacturers are facing a catch 22 situation in that this increased functionality, flexibility, and power must be provided within a footprint that continues to shrink. Combined with ever-present cost and time-to-market pressures passed on by OEMs, these additions have forced power-supply manufacturers to push their design and manufacturing capabilities to the limit *(Fig. 1)*.

Power Requirements

The total power requirements for industrial systems and microprocessor-based equipment have escalated in recent years, with many systems calling for 500 to 1000 W of power to satisfy today's requirements, while leaving a certain amount of headroom power for future growth. Recent estimates of market distribution by power level are shown in Figure 2. Prior to 1995, roughly 16% of the market was addressed by a 300-W supply, while 49% was at 500 W, 17% at 750 W, and



1. Using enhanced design and manufacturing techniques, such as reduced component counts and surface-mount technology, power-supply manufacturers are responding to customer demands for enhanced functionality, higher power, and greater reliability—all within a smaller footprint. In a typical scenario, the bottom side of the power supply's pc board uses all surface-mount construction, while through-hole modules are stacked on the top side.

18% at 1000 W. Recent changes in system architecture, and an overall increase in power required, has shifted the distribution so that 55% of the market is now handled by a 750-1000-W power supply.

Some principal reasons for this increase include faster system logic and the popular use of multiple CPUs within a single system for parallel processing. Usually, memory requirements are increased for these functions. While chip designs featuring greater density and narrower linewidths call for lower voltages, higher currents are needed to drive the increased amounts of logic and memory. Currents as high as 150 A on the main output are now required to adequately power some systems.

Most systems now use either 5 or 3.3 V to power logic and memory, with some systems going to atypical voltages. These voltage can range fromfrom 1.8 to 5.7 V. In response to widely varying output-voltage needs, some power supplies now offer a high-power, adjustable main output which allows system voltage to be set by adjusting a potentiometer. This feature guarantees that OEMs can realize a power supply with the precise main output voltage required by the system. In addition, if the power supply is used at a given voltage in a current system, it does not have to be requalified at the new voltage for a next-generation system with a reduced main output voltage.

Tighter regulation of system power continues to be a necessity. Most power supplies now provide a main output regulated to within 0.5% to 1% of the specified voltage, with some providing regulation as tight as 0.1%.

Auxiliary Power

Power requirements for auxiliary outputs also are increasing to allow disk drives and communication hardware to keep up with the new generation of Pentium, Pentium Pro, and Klamath processors. Peripheral activity and access speeds have seen a dramatic increase, to the extent that this accessory hardware has become an integral part of every microprocessor-based system. To conserve space and save costs, system power supplies also are now being called upon to power fans and other components that were previously powered by separate power supplies.

As many as six outputs are called for in some applications, including:

± 12 V—The –12-V auxiliary is typically used to power system communications via serial and/or parallel ports, while the 12-V auxiliary output can drive various peripheral or host data storage functions. Typically, the dependence upon these two auxiliary outputs to power an increased number of serial/parallel ports, system fan requirements, and storage device requirements has resulted in bulkier auxiliary outputs and more thermally efficient power supplies to provide more power in a smaller envelope.

Auxiliary 3.3- and 5-V outputs—These outputs work in tandem with the main output to meet the power requirements of logic and memory of mixed technologies. The demand for additional host activities such as system-level interface-monitoring signals, and additional logic and memory requirements for peripheral activities have driven the output power typically required from these outputs to approximately 200 W.

24-V auxiliary output—This output powers additional peripherals such as fans, monitors, and associated bus activities.

48-V auxiliary output—This output addresses bus requirements usually found inside a control panel or in most racks and enclosures.

While power levels and capabilities continue to increase, the cost of power continues to head in a downward direction. Typical costs for high-quality standard power supplies for OEM equipment are now approaching \$0.45/W to \$0.50/W, versus approximately \$1/W in the early 1990s. These cost reductions are being driven by competitive pressures on OEMs, which translate into demands for cost savings from power-supply vendors and, in turn, from component suppliers. Improved automation, designing for manufacturability, reduced compo-

TRENDS IN SUPPLIES FOR EMBEDDED-PROCESSOR SYSTEMS

Parameter	Five years ago	Two years ago	Today	Future
Size	Adequate	Downward trend	Maximize minimum allotment	DPA/rackmount
V_{out} offering	5, ±12, 24 V	3.3, 5, æ12, 24 V	Same V_{out} with 3.3-5-V aux adjust; higher-powered 5- and 12-V auxs	More outputs in one box; increased power, lower voltages
P_{out} main	Adequate for system needs	More power and adjustable outputs	Wide-range adjust, highest-power outputs	Wide range adjust, tighter regulation
P_{out} aux	Used for system-level monitoring functions only	Power increasing and more flexibility	More power in one-box solution	High-power adjust main, flexible aux with more power
Current share	Sometimes	Necessity	Necessity	Necessity
Overtemperature (OT)	Sometimes	Always OT or fan fail	Always OT or fan fail	Look for consolidated OT and fan-fail signals
Fan fail	Not popular	Always OT or fan fail	Always OT or fan fail	Look for consolidated OT and fan-fail signals
Remote sense	Sometimes	Available as an option	Necessity	Necessity
Remote on/off	Sometimes	Necessity	Necessity	Necessity
VME signals	Not popular	Optional	Optional	Necessity, with added signals
Sequencing	Not popular	Optional	Optional	Necessity
AC-DC good	Sometimes	Necessity	Necessity	Necessity
Hot swap	Not popular	Interesting	Optional for rack power	Available with rack power
Dynamic response	Response times are slow; systems not demanding	Trend toward decreasing response times	Minimum response time meets processor demand	Almost instantaneous (logic/technology restricted)

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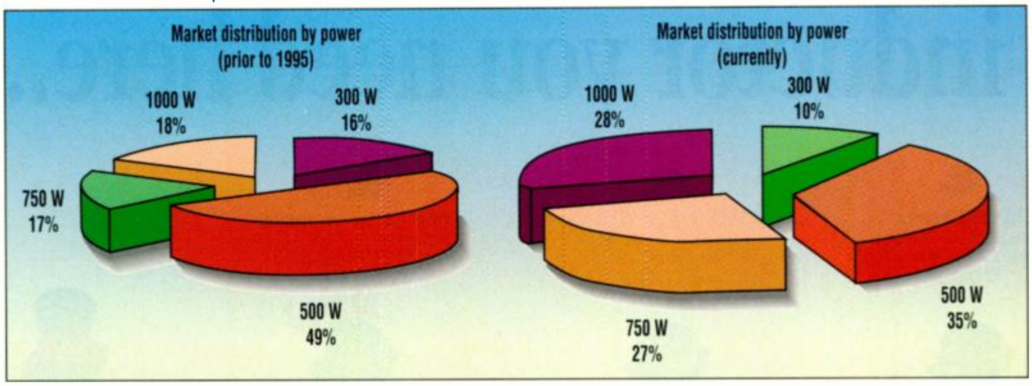

2. The total power requirements for industrial and microprocessor-based power supplies have escalated in recent years with many systems calling for 500 to 1000 W of power to satisfy today's requirements while leaving a certain amount of headroom power for future growth. Reasons for this increase include faster system logic and the popular use of multiple CPUs within a single system for parallel processing. The CPUs are usually coupled with more memoryto handle the increasing functionality of these systems.

nent counts, and more efficient use of personnel also are enabling cost reductions in the power-supply arena.

Reliability, Signaling, And Safety

With downtime no longer an option in a myriad of highly sensitive applications, reliability standards for power supplies continue to increase. MTBFs of up to 150,000 hours are now in demand. As a result of this need for reliability, the calculation of MTBF is moving toward stricter methods, such as Bellcore TR-TSY-000332, which weighs the tolerances of each component instead of allowing averaging of similar components.

Despite stricter monitoring and improved reliability, failures can still occur. The key is to prevent power failure from causing catastrophic system failure. This task calls for more signaling and safety features in system-level power supplies. The more popular features being included are:

Power redundancy—In recent years, N+1 or N+2 redundancy (key to fault-tolerant operation) has become a fixture on power specifications.

Current sharing—By allowing multiple power supplies to share the full load, disruptions are avoided should one unit fail, and the service life of individual units is extended. Active current-sharing, supported by a control circuit, is becoming more prevalent, supplanting brute force current-share solutions.

Hot swapping—If one power supply fails, it can be removed from the system and replaced by a new unit without turning the ac power off, so the system maintains all of its memory and no downtime results.

Interface signals—System designers are no longer willing to place a power supply in a system and let it operate independently. For example, if a fan fails or the temperature in the power supply rises, they want that information to be provided before the power supply fails. Signals such as fan fail, overtemperature, ac good, dc good, remote on/off, and overcurrent have become extremely popular in recent years. Other features include:

- Remote-sense on all outputs to allow the power supply to compensate for load fluctuations.
- Output sequencing to define the order in which the outputs turn on. For example, in a machine tool system, while the system is initializing itself to zero on all three axes, the user can keep power from being supplied to the keyboard and mouse to prevent any accidental keystroke or other input that might cause an error.
- Power factor correction to address European EMC issues, and to reduce the input line current to a level that can be powered from a regular wall outlet instead of a dedicated fixed-line power source. Power factors of 0.99 or higher are becoming standard.
- Overvoltage protection to automatically shutdown all outputs in the event of an overvoltage condition is required.
- VME signals to work with VMEbus technology to supply the capability for a system reset, power-supply reset, or ac power-fail signal. When included in the power supply, it eliminates the need for additional circuitry in the system design to meet these needs.
- Overcurrent shutdown and auto-reset to prevent damage to the power supply and possibly the system.
- Faster dynamic response to handle fluctuations in load. While this feature is more critical in chip-level power, even system-level power solutions are starting to demand its inclusion.

With respect to power backup, progress is being made in achieving more-simplified handling of backup power in PC applications in the case of power disruptions. Similar changes for systems with higher power requirements are more elusive. Technologies are now emerging that show great promise for the incorporation of the uninterruptible power-supply (UPS) function into the PC itself, inexpensively and relatively smoothly. No integrated solutions are available yet, but technologies are being evaluated for PC power supplies up to 200 W.

For the larger, more sophisticated systems, such as embedded computers and minicomputers with power requirements of 500 W and up, the limitations of existing battery technologies preclude the incorporation of the UPS function within the same enclosure as the processor. The physical size of the batteries required for sufficient storage capacity demands the use of a separate, external UPS system. Alternatively, backup can be achieved using flywheels or redundant input feeds, such as an ac line plus a generator feed, with redundant power capability.

Another important reliability concern is electromagnetic interference (EMI). Switching-transistor power supplies are typically the biggest source of EMI in the system. Reducing EMI is essential to avoid interfer-

ence with disk drives and other components. Emphasis on meeting EMI standards is growing, causing a trend toward precertification for compliance to conducted and radiated EMI standards, such as the strict CE EMC system-level directive. Power supplies that meet the stringent CE EMC directive and other EMI standards eliminate the need for engineers to add special shielding or filtering to the system to compensate for power-supply-related interference. This capability can significantly reduce costs and development time, as well as enhance system reliability.

The Incredible Shrinking Box

The conservation of space is a constant concern for power supply designers. No longer is there leeway to accommodate any footprint the power supply requires. In fact, most system designers normally consider the power supply the last item on a long list of more critical systems. As a result of this attitute, the trend in recent years has been to minimize the space allocated to power, especially because the system designer considers this dead space which cannot be used by the host system. Although smaller footprints are achievable, this task is complicated by the need to supply more power from the smaller box.

This need is putting pressure on designers to improve operating efficiency to help deal with heat dissipation. The space constraints also are leading to some innovative power-supply design solutions. For example, reduced component counts and the popular use of surface-mount assembly have led to smaller power-supply designs with enhanced reliability (through improved thermal dissipation and more automated assembly). In a typical scenario, the bottom side of the power supply's PC board uses all surface-mount construction, while through-hole modules are stacked on the top side *(Fig. 1, again)*.

In the future, even higher-power applications will likely shift from box enclosures to card-level power architectures, where the power supply is provided via card-mounted, highly scalable, and flexible power modules that can be hot swapped and modified with ease. Power is distributed from the bus to specific locations, and more cards can be plugged in to handle more features, peripherals, and other requirements as systems grow in size and complexity. Because more custom or value-added engineering is required, card-level solutions are more expensive than enclosed power supplies. However, as hot-swap capability, redundancy, and flexibility become more important, the relative cost of these solutions will likely decrease as standard solutions become more widely available. Alternatives to card-mounted power solutions that achieve similar results (while consuming more space) are rack-mounted arrangements where enclosed power supplies are redundantly mounted in racks designed either by the power supply vendor or the OEM.

> **"These flexible, standard supplies are also allowing faster creation of new, user-specific combinations of standard features..."**

Insisting On Flexibility

A greater percentage of power supplies are now being provided to OEMs by outside vendors, and this trend is expected to continue. In 1995, market analysis indicated a nearly even split between merchant and captive supply of switching power supplies. This represented a decided shift from prior years, when typically, nearly 66% of power supplies were created by in-house design. The potential benefits of outsourcing—assuming that a workable power solution can be found on the market as a standard or modified-standard component—include reduced costs and shortened development time for an increased number and type of power supplies. In other words, the power-supply market is becoming niche-oriented to address multiple tasks and applications.

To meet the growing demand for system-level power supplies that meet a wide range of specifications for system and auxiliary power, as well as signaling and safety features, standard solutions in more flexible configurations are needed. Unfortunately, in many instances OEMs are still unable to find the combinations of outputs and features they need on the market. This situation forces them to pick one of three options: redesign their systems to accommodate an existing power solution, use cumbersome combinations of multiple power supplies, or opt for a costly and time-consuming custom solution.

Designers' calls for lower cost and improved flexibility are not going unheard, however, and there is a distinct trend toward greater flexibility in recent and upcoming standard power-supply designs. These flexibility enhancements include:

- More output configurations at more power levels, including 500, 750, and 1000 W.
- Voltage adjustability in the 3- to 6-V range for the main output.
- An increased number of higher-power auxiliary outputs. Instead of three or four total outputs, some manufacturers now offer the main output plus four auxiliaries.
- An increased number of optional output configurations to meet a wide range of system needs. By allowing users to mix and match possibilities, including multiple 12- and –12-V outputs, 3.3- and 5.2-V auxiliaries at higher power levels, and 24- and 48-V outputs, more power requirements can be met with off-the-shelf solutions to speed the design process.

A full palette of signaling and safety features and options, are also being included. Such options provide for fault-tolerant, redundant operation with hot-swap capabilities.

These flexible, standard power supplies are also allowing faster creation of new, user-specific combinations of standard features, and have set the stage for the expanded use of modified standard, value-added power supplies. Modified standard power supplies can satisfy a greatly expanded range of application needs, while eliminating the design risk and reducing nonrecurring engineering costs and development time compared to start-from-scratch custom components.

Into the Future

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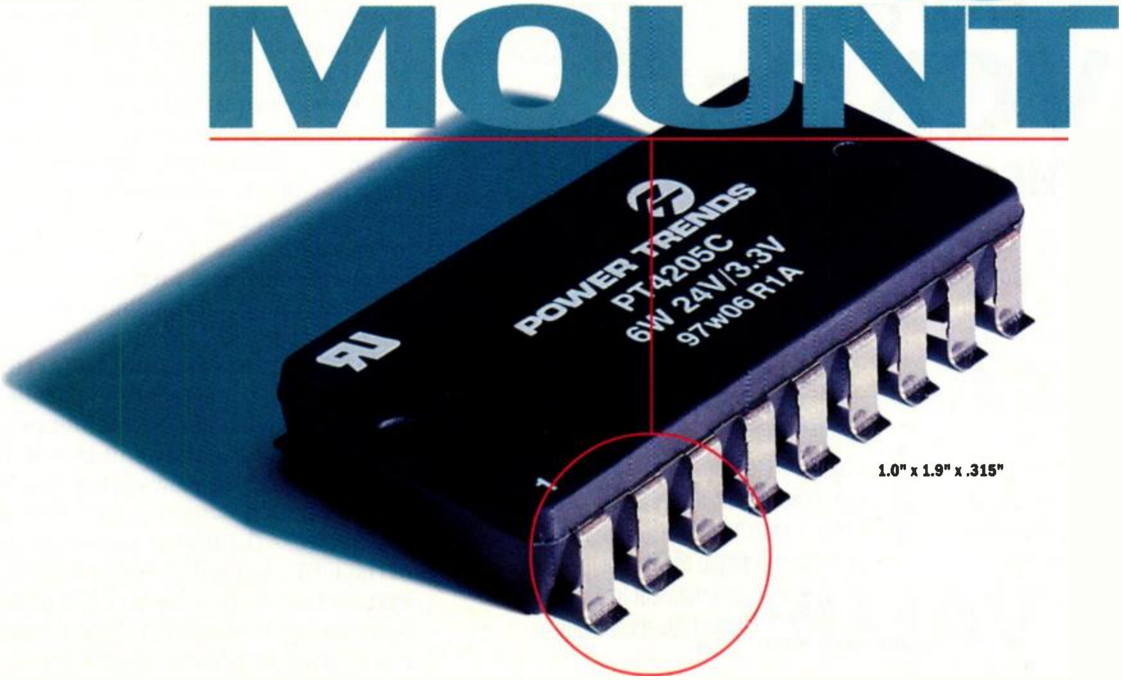

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Product Selector Guide

	Outputs		Input Voltage Range	
Power	Vo	Io	18 - 40V	36 - 75V
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5W	3.3V	1.5A	PT4205	PT4202
6W	5V	1.2A	PT4206	PT4203
6W	12V	0.6A	—	PT4204
7W	+5V / -5V	1A ea	—	PT4301
7W	+5V / +3.3V	1A ea	—	PT4302
15W	3.3V	4.5A	—	PT4110
15W	5V	3A	PT4104	PT4101
15W	12V	1.2A	PT4105	PT4102
15W	15V	1A	PT4106	PT4103

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creasing sophistication of power needs, make it likely that the trend toward increased use of standard power supplies with a greatly expanded range of capabilities will continue. Also, system-level power solutions will continue to shrink in size from enclosed black boxes to distributed power architectures. In addtion, future power requirements for microprocessor-based electronic equipment will likely involve continued reductions in voltage, increases in current levels, tighter voltage regulation, more auxiliary outputs, faster dynamic response, and further enhancements in safety and signaling capabilities *(see the table)*.

In the near term, due to faster CPUs and the emergence of parallel processing with increased memory use, the most popular solution will likely be a quad- or pent-output power supply. This power supply will not only address the higher power needs of the CPU, but will handle auxiliary system functions as well. Adjustable main-output voltage and flexibility in configuring auxiliary outputs are essential to allow wide applicability and elude the added expense and time-to-market penalties of multiple or custom power supplies or system redesigns. Black-box power solutions should not only handle a wide range of system power needs, they should be rack-mountable and offer hot-swap capability along with the signaling and safety features that have come to be regarded as basic requirements in recent years.

John Carroll is market segment manager (computer equipment) for Lambda Electronics Inc., Melville, NY. Carroll is a member of the IEEE and holds MBA and BSEE degrees from Adelphi University, Garden City, NY, and New York Maritime College, Fort Schuyler, Bronx, NY, respectively. Carroll is the commanding officer of a U. S. Naval Reserve unit supporting an amphibious squadron in the event of the deployment of U. S. Marine Corps.

How Valuable	Circle
Highly	535
Moderately	536
Slightly	537

Distributed Power Architectures Enter The Mainstream

Falling Component Costs And Increasing Customer Performance Demands Make Distributed Power The Architecture Of Choice.

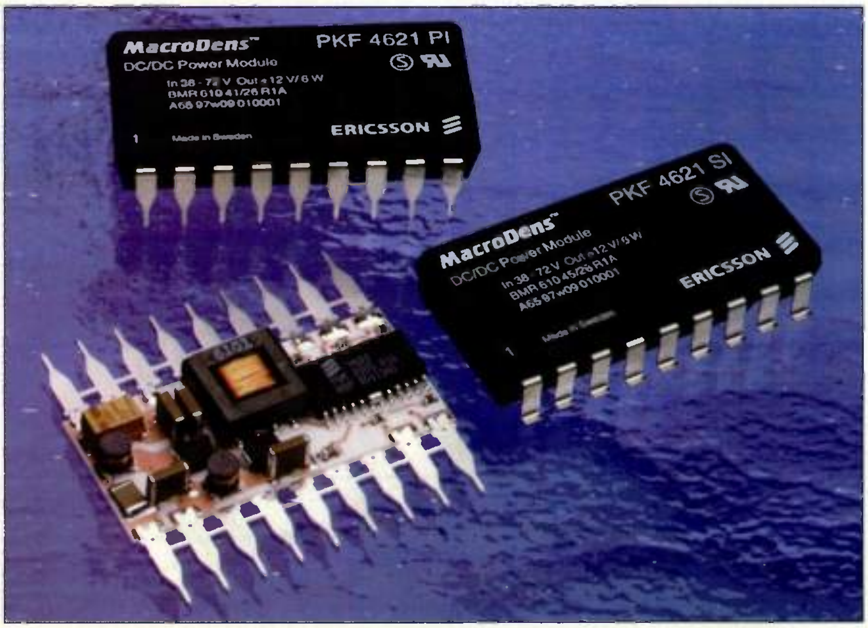
BY LARS THORSELL

Ericsson Components AB, Energy Systems Division, Power Modules, S-164 81, Kista-Stockholm, Sweden; (46) 8 721 6000; fax (46) 8 721 7001.

In complex systems, the power architecture chosen can have significant implications for the overall design. One of the key decisions that must be made early on is whether to go with a central or distributed architecture. Until recently, all but the most crucial systems settled for the relatively low-cost, centralized solution, while the expensive, distributed-power architecture (DPA), was relegated to high-reliability applications.

Now, however, the falling cost of implementing a DPA has made it a much more attractive alternative. Low-cost, standard power modules have been a key facilitator in the architecture's proliferation *(Fig. 1)*. Although still commanding a premium, the advantages of a DPA in terms of reliability, safety, fault isolation/tolerance, upgradability, and hot-swap capability, make it the architecture of choice for today's high-reliability systems. Having decided to opt for a DPA, there are a number of issues that must be addressed for optimum performance. These include, partitioning/distribution, electrical and thermal performance, cost, and power-module selection.

The default approach to getting power to where it is needed, at the right voltage and current, is the centralized power architecture. Here, a large power supply creates all the required voltages, which are then distributed at full current around the sys-



1. The availability of low-cost, standard surface-mount power modules has been a key factor in the acceptance of distributed power as a viable, affordable solution over a more centralized architecture. The advantages of the distributed architecture, in terms of reliability, fault tolerance, lower noise, and flexibility, make it a necessary design strategy for a high-performance, high-availability system.

tem *(Fig. 2)*. With voltages of 3.3 V and below becoming more common, the extended wiring and trace lengths associated with a central power architecture create their own problems. Remote sensing can address some of these issues, but as the systems get bigger, remote sensing introduces its own significant complexities.

The next step up from this approach is to separate the rectification from the regulation, and move the critical control closer to the load. However, distributing rectified line voltages is a major safety issue due to the high voltage level, as well as the lack of isolation. It does have benefits over the centralized architecture in that current levels, at a given power, are lower.

As a result of these voltage and isolation safety issues, the system may use an ac-dc power supply to provide an isolated, lower-level voltage, typically either 24 V or 48 V. Keeping to these standard voltages ensures the maximum choice of standard converter modules, and also ensures that the system voltage is considered safe from a regulatory point of view. Another major benefit from using this lower dc voltage is that it becomes much simpler to install battery backup. This distributed-voltage design has allowed for the development of three distinct levels of DPA implementation: power per shelf, power per function, and power per board *(Fig. 2, again)*. Availability and flexibility are major differentiators between the various core approaches.

Closest to the centralized power approach is the power-per-shelf architecture, where a complete rack of electronics is powered from a local dc-dc converter. This design gives many of the benefits of distribution, but means using larger converters. Since larger power converters first achieved price competitiveness for these devices, this was the early approach, but any problem on a given power rail, such as failure on a single board, can affect all cards in that rack.

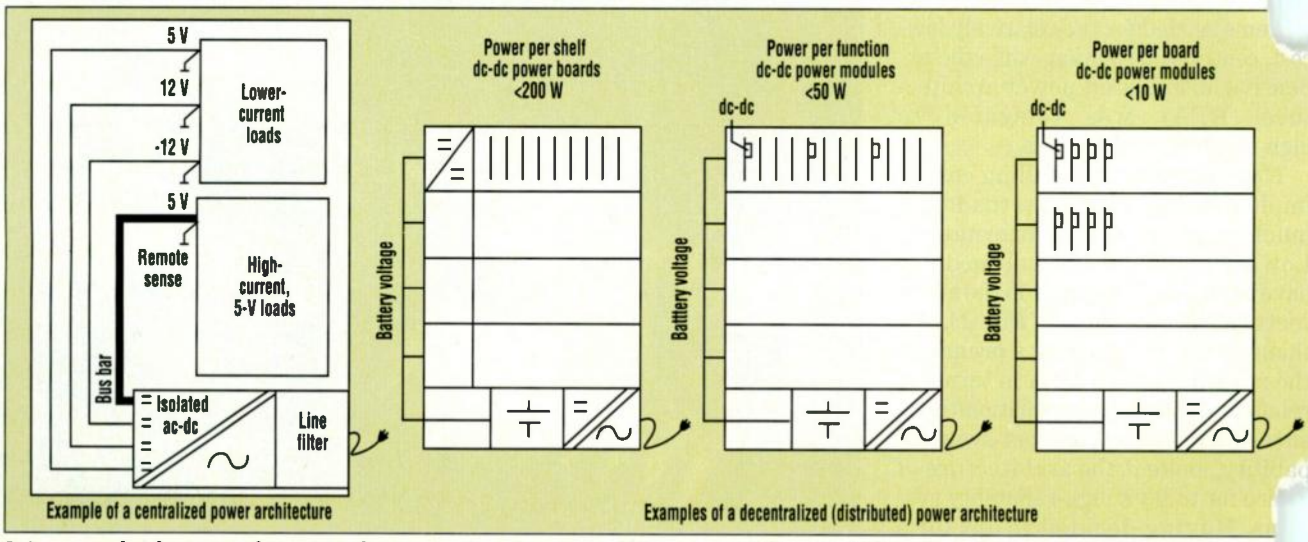
To reduce system interdependence further, it is possible to use power per function, where each discrete function, spread across several boards, will have its own power conversion. This design localizes any board failure and aids debugging and repair while improving availability. However, it probably means that field repairs will require complete sets of boards, rather than individual cards.

Power per board, where each board is self-contained for accurately controlled power, is the natural extension of this approach, and provides the ultimate in DPA. With this structure there is no impact on other parts of the system should one board fail. If a specific board needs an unusual or unexpected voltage, it is only an issue for t[he] board and easily fixed, rather tha[n af]fecting the main power supply an[d] the system wiring. This feature is useful at the original system design stage, but becomes a major benefit when considering the ongoing life costs of upgrades or improvements in the field.

Having decided upon a DPA, with its various architectural advantages, there are still a number of issues that must be addressed for optimum performance. These include partitioning/distribution, electrical and thermal performance, cost, and power-module selection. Because designers are now able to use standa[rd] modules, rather than being forced [into] the custom designs typical for a [cen]tralized design, they need not con[cern] themselves with topologies, circui[t de]sign, and magnetics.

Distribution Voltage

DPA assumes that the mains is contained, and both insulated and isolated from the system, which immediately simplifies the electrical safety issues within the system. Distributing only voltages categorized as SELV (<60V dc) removes many regulatory requirements and specifications. The key design parameters for the line power supply are now the distribution vol[t]age and the overall system power[, to]gether with any requirements r[elat]ing to the various line voltage le[vels]



2. In a centralized power architecture, a large power supply creates all the required voltages, which are then distributed, at full current, around [the] system. With the popularity of voltages of 3.3 V and below, extended wiring and trace lengths become a problem. Distributed power, in its th[ree] main forms, eliminates these problems. The power-per-shelf architecture gives many of the benefits of distribution, but uses larger converters. Power per function localizes faults and aids debugging and repair while improving availability. However, it may mean that field repairs will require complete sets of boards, rather than individual cards. Power per board is the ultimate in a DPA.

No-Penalty PROM Cell Allows Customization Of Logic Circuits

A programmable logic element that adds no additional process cost promises to give designers of microprocessors and other logic circuits the ability to perform a number of functions such as customization, identification, serialization, redundancy, and code patching. Developed by researchers at Intel Corp., Hillsboro, Ore., and slated for presentation at next month's International Electron Devices Meeting (IEDM), Washington, D.C. (paper 34.3), the experimental one-time programmable cell is based on salicide agglomeration of polysilicon fuses. Experimental versions of the fuse have been implemented in a 0.25-µm CMOS process that employs a polysilicon thickness of about 0.2 µm and titanium-silicide (TiS_2) films with a sheet resistance value of 3 to 4 Ω/square.

The polyagglomeration fuse (PAF) is programmed by bias stress that results in temperatures high enough to cause agglomeration of the titanium-silicide. Prior to programming, the fuses have a resistance value of 50 to 100 Ω, depending on the dimensions, the silicide thickness, and the silicide's quality. Silicide quality, in turn, depends on polysilicon line width and doping control.

When a current beyond a certain level is injected, the fuse resistance value increases, indicating the formation of discontinuities in the silicide layer *(see the figure, left)*. This increased resistance value varies greatly from device to device, and can range from several hundred to several hundred-thousand ohms.

As the voltage level is increased, current increases in a nonlinear mode due to self-heating. When the dissipated power reaches a critical level, fusing occurs and the element goes to a much higher resistance value. The fusing event is one with negative feedback, thus a given fuse may be stressed only once.

Subtle Changes

Damage caused by programming has been examined by Intel's researchers, and was found to be very subtle. The damage was confined to the silicide layer and its interfaces with the polysilicon layer and the overlying dielectric material, reducing fears of lower circuit reliability or impaired operation due to the fuses. In contrast, traditional fuses made of polysilicon or metal require the implementation of openings in the overlying layers to facilitate the process of material removal.

The fusing operation can occur at relatively low current and voltage levels (a current of just 8 mA, for example), and can take place rather swiftly in just 1 ms. However, post-programming resistance is significantly enhanced if more energy is dumped into the element.

A Special Circuit

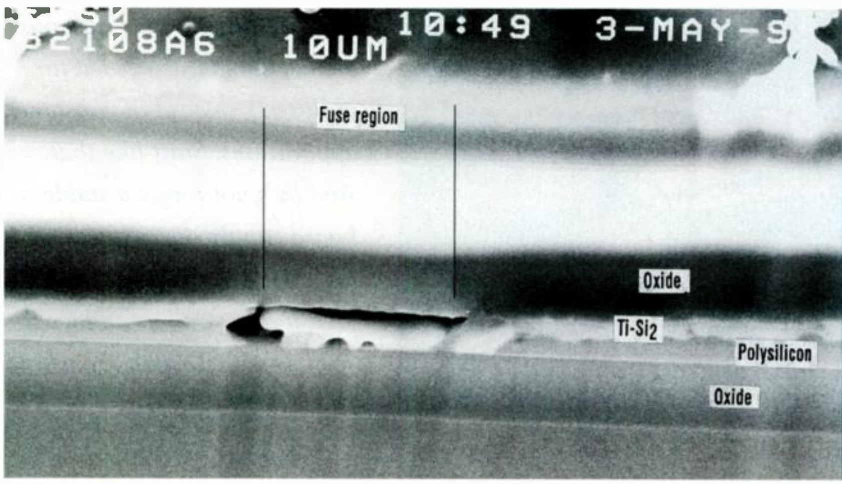
Intel's researchers developed a special programming circuit so that the circuit can be included, along with the logic, on the chip. In a simplified version of the circuit, programming occurs when a logic low is asserted on the gate of a large p-channel MOS transistor *(see the figure)*. The sensing circuit is a balanced solution to a stringent set of requirements, the foremost of them being that the sensing currents be kept low.

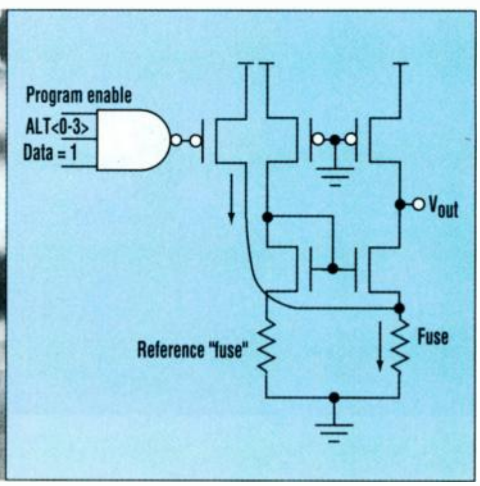
Sensing occurs by comparing the fuse resistance value with a reference resistance value that's set to eight times the value of the unburned fuse. This ratio of reference to fuse resistance values creates a default (unburned) output voltage that is low enough to be interpreted as a logic low state.

For a programmed fuse, the resulting output voltage is high enough to be interpreted as a logic high state. Thus, the gain of the circuit is sufficient for single-ended voltage outputs.

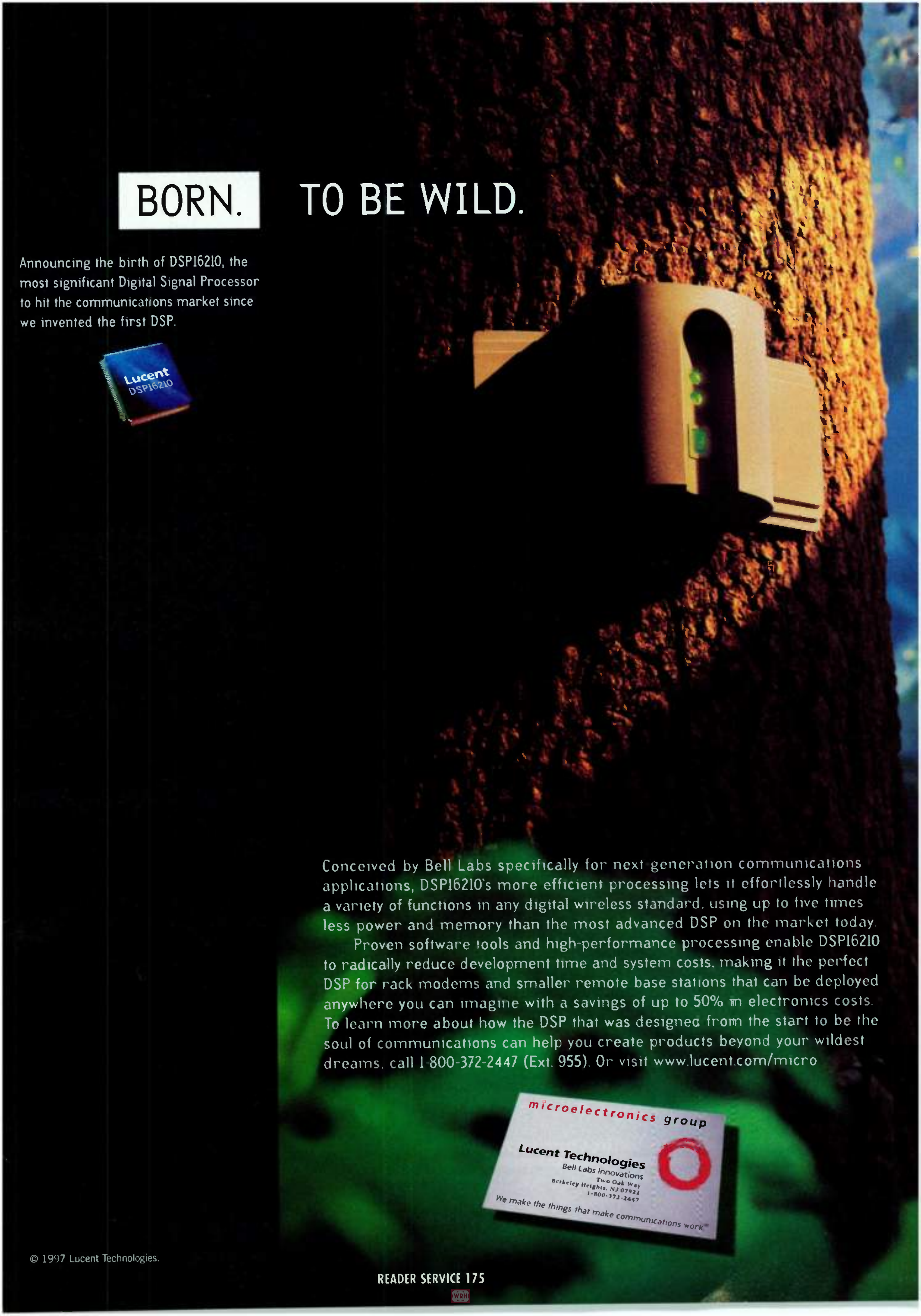
In the case of the circuit shown in the figure, the ratio of reference to unburned fuse resistance represents a balanced trade-off between output high voltage (VOH), and output low voltage (VOL) levels.

Dave Bursky





By agglomerating the silicide layer through voltage and current biasing, a fuse region in this PROM cell developed by Intel can be programmed with little or no damage to the overlying dielectric and underlying polysilicon layers (left). The simplified programming and sense circuitry uses the resistance of a reference fuse to compare it with that of a fuse to be programmed. This method allows it to determine if the fuse can be programmed, and then to enable the circuit to program the fuse (right).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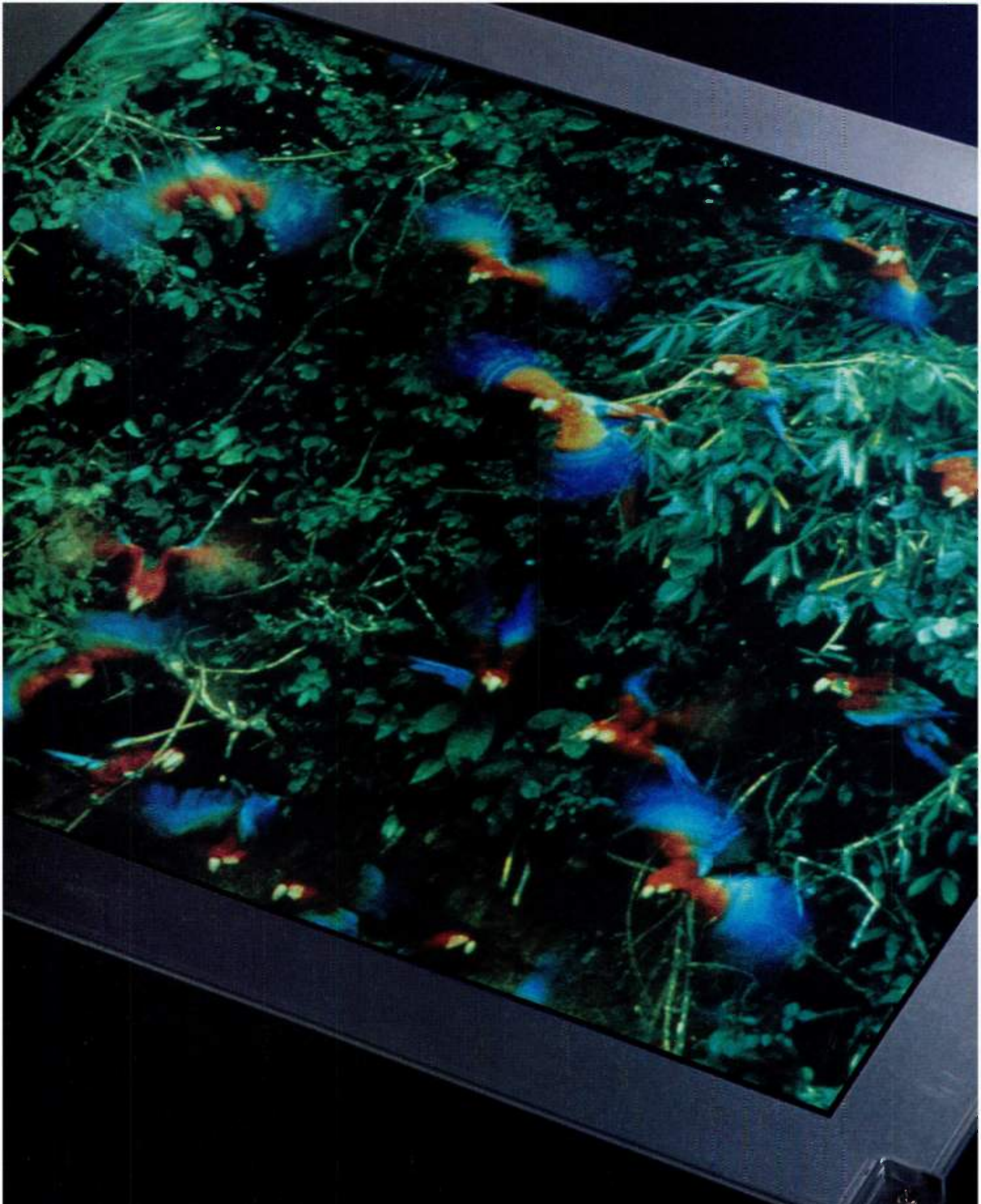


HARRIS SEMICONDUCTOR

POWER SOLUTIONS

SEPTEMBER, 1997

AUTOMOTIVE

COMPUTER POWER

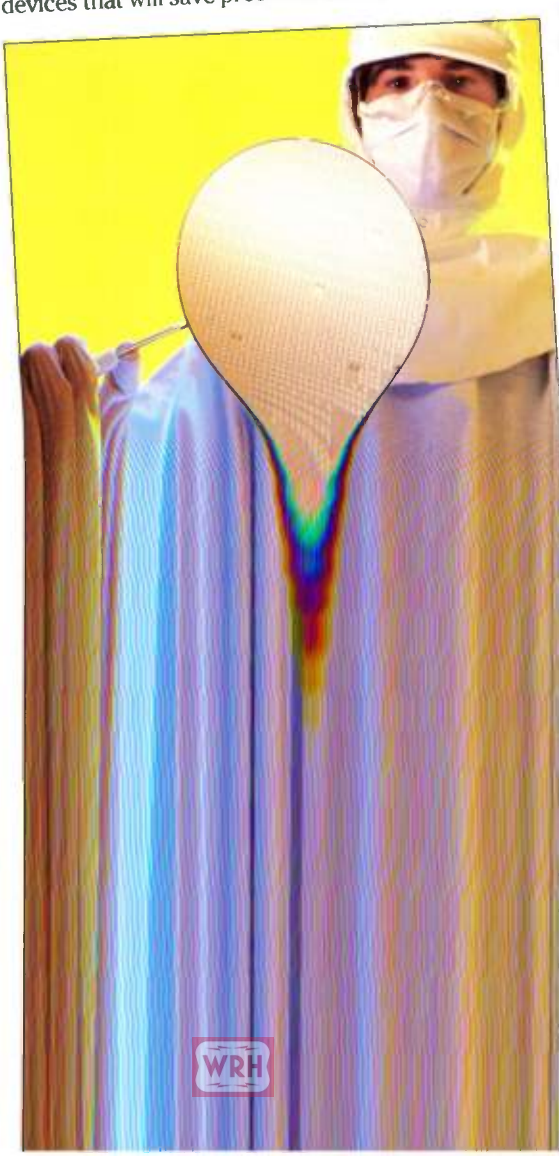
INDUSTRIAL

NEW EVALUATION BOARDS AVAILABLE

NEW DESIGN RESOURCE CD AVAILABLE

Harris Leads with *UltraFET*™ MOSFETs

"On resistance 10% lower than the nearest competition" is the compelling feature marking the launch of Harris' *UltraFET* MOSFET series. While ramping up to meet demands for devices that will save precious battery



the front lines of MOSFET technology," says Tom Daly, Director of Discrete Power Marketing. "It was the reason for building the world's first 8-inch wafer fab, Fab 8, at our Mountaintop, Pennsylvania facility. The manufacturing technology at that facility, joined with the *UltraFET* MOSFET breakthroughs, will make the latest MOSFET technology available to designers in very high volumes."

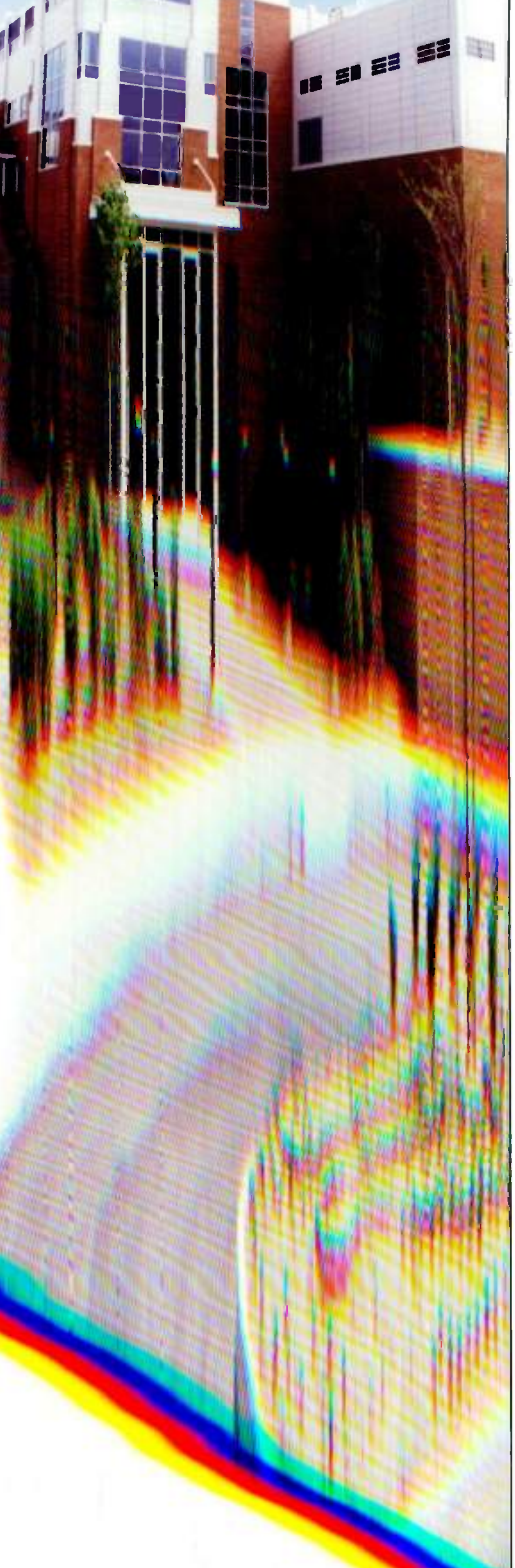
Cost Saving Benefits

The *UltraFET* MOSFET series consists of N- and P-channel MOSFETs with the lowest on resistance in the industry

Harris Opens World's First 8" Power Pipeline™

products, a 55-volt device, for automotive and industrial applications. Harris will continue to roll out *UltraFET* MOSFETs for the fast growing communications, computer, EDP, higher-voltage markets, and industrial motor drives. These devices will be particularly popular for cellular phones, laptop and desktop PCs, as well as portable and handheld equipment in

The new Power MOS fabrication facility at Mountaintop, Pennsylvania is the first 8" fab dedicated to power devices. With this state-of-the-art expansion, Harris Semiconductor becomes the only company offering an 8" discrete power pipeline with onsite capabilities



Production at the Fab 8 facility includes metal-oxide semiconductor field-effect transitors (MOSFETs) and insulated gate bipolar transitors (IGBTs).

Lowest Cycle Time

Designed to meet manufacturing technology requirements for 10 years, the fab is able to change and set up tools without interrupting production. Revolutionary changes have been made in manufacturing processes, which have resulted in the lowest cycle time in the power semiconductor industry. This has been done through constraint management from raw wafer through test, brand and ship.

IMPReSS Scheduling

Fab 8 operates under IMPReSS (Integrated Manufacturing Production Requirements Scheduling System), Harris' world-wide system. Using linear programming, IMPReSS generates plans that are capacity, WIP and materials efficient on the first run.

Through Standard Mechanical Interface (SMIF), Fab 8 maintains a Class 1 wafer environment during manufacturing, tool installations and service. Combining this with robust robotic processing has achieved an unprecedented low number of defects. Harris' award-winning Maverick lot program has been applied to all products at probe and final test, testing parametric distribution and comparing the specification. As a result, customer risk to product not within normal distribution is minimized. Special tests beyond customer specification may be applied to guard against circuit interaction. On most products, Harris also uses a 100% redundant quality test at branding to further assure the lowest PPM levels. Finished products are also tested in Real Time Indicator, which was pioneered by Harris. This assures reliability in the field with short-term testing each week.

"The most important aspect of *UltraFET* MOSFET success is close alignment with our customers," says Joe Manganello, MOSFET Marketing Manager. "We've sent over 2,000 *UltraFET* MOSFET devices to a very large customer base and early feedback indicates that we have something very special here. We're monitoring these customers very closely to help understand their applications and testing requirements, thereby reducing design-in time."

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AND ASK FOR
EXTENSION #7745

- Internet *http://www.semi.harris.com*
- Technical Assistance E-mail: *centapp@harris.com*

few months.

Fab 8 Key Factor

"*UltraFET* MOSFET indicates that Harris is digging in very aggressively on

UltraFET™ is a trademark of Harris Corporation.

More to Come

In July '97, Harris introduced the first in a series of *UltraFET* MOSFET

Continued on page 2

HIP6000 – PWM Controllers Enable Wide Range of DC-DC Applications

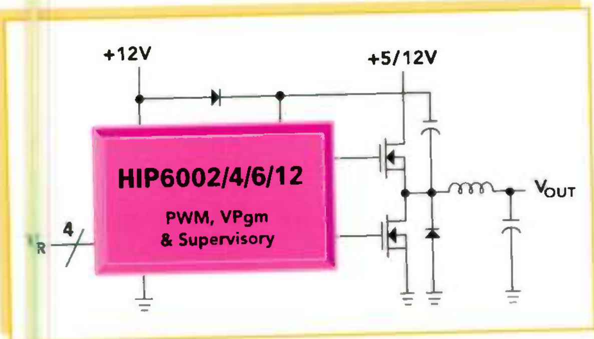
HIP6000, a family of easy-to-use, yet high-performance, PWM controllers, steps down input voltages from up to 15V down to 1.26V. Using voltage-control mode and lossless overcurrent protection, stable DC-DC converters can be constructed with first-pass design success. While easy to use, these devices provide outstanding parameters, such as 1% voltage referenced over full operating conditions, and a 15 MHz-gain bandwidth product error amplifier, making for well-regulated outputs.

Synchronous buck devices provide adaptive dead time which takes the guesswork out of shoot-through protection. All parts drive cost effective N-channel MOSFETs.

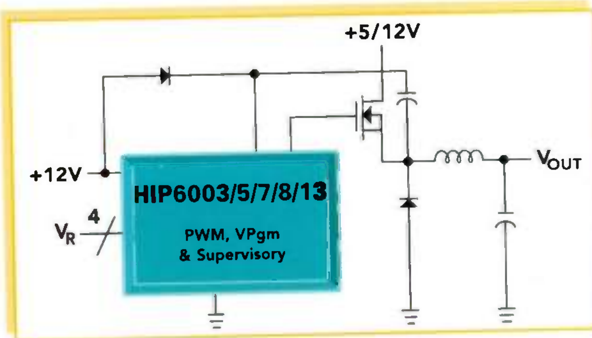
With or without built-in DACs for output voltage programmability, these provide system solutions ranging from general-purpose embedded applications to point of use DC-DCs for leading-edge processors including Pentium II™ , K6™, PowerPC™ and 6x86™.

Application Services

To make it easier to evaluate our products, we've developed several reference designs and additional application aides. For example, our HIP6006EVAL1 and HIP6007EVAL1 are general purpose evaluation boards, backed by application notes which suggest circuit values for 3, 6, 9, 12 and 15 amp applications. Additionally, we can provide the service of feedback network analysis.



Synchronous Rectified Buck Driving External Harris MOSFETs



Standard Buck Driving External Harris MOSFETs

Evaluation Boards for HIP6000 Family

HIP6002EVAL1	Embedded Style for Pentium Pro
HIP6003EVAL1	VRM Design for Pentium Pro
HIP6004EVAL1	VRM Design for Pentium II
HIP6004EVAL3	Embedded Style for Pentium II
HIP6005EVAL3	Embedded Style for Pentium II
HIP6006EVAL1	General Purpose 9A Design
HIP6007EVAL1	General Purpose 9A Design

In today's accelerated marketplace, a designer's time is extremely limited. To provide a quick and easy way to assess our products, Harris Semiconductor offers three types of reference designs. Designers can evaluate the performance of the Harris DC-DC converters in an embedded motherboard application, VRM design or in general purpose applications. Our reference designs are fully compliant to Intel specifications for Pentium Pro and Pentium II class microprocessors.

Pentium is a trademark of Intel Corporation. Power PC is a trademark of IBM. K6 is a trademark of AMD Corporation. 6X86 is a trademark of Cyrix Corporation.

COMPUTER POWER

High Efficiency Surface Mountable MOSFET for DC-to-DC Converters

The RFD16N02L/SM is intended for use in high frequency DC-to-DC power converters, and has very low gate charge per unit $r_{DS(ON)}$ in order to minimize switching losses. Packaged in TO-251AA and TO-252AA surface-mount packages, they are ideal where space and efficiency are necessary.

At 16 Amps and 20 Volts (avalanche rated), these N-channel devices are ideally suited for conversion applications up to 300 watts. In low voltage DC power supplies, they may also be used as a pass transistor. PSPICE™ models are available to reduce design cycle time. Logic level gates enable these devices to be used for general purpose load control.

Part No.	Package	Evaluation Board
RFD16N02L	TO-251AA	N/A
RFD16N02LSM	TO-252AA	N/A
RFD16N02LSM9A	TO-252AA	N/A

Features

- 15A/20V/0.022 Ohm N-channel
- Low $r_{DS(ON)}$ provides cost-effective general purpose low side load control
- Logic level gate input
- Can be operated directly from 5V logic circuits
- Avalanche energy rated
- Designed for switching inductive loads such as inductors, coils, and transformers

Benefits

- Low gate charge per unit $r_{DS(ON)}$
- Low gate charge provides superior efficiency in low voltage, high frequency DC-to-DC converter applications
- Temperature compensating PSPICE electrical model
- PSPICE model aids in circuit simulation and reduces design cycle time
- Available in the TO-251AA and TO-252AA packages
- TO-252AA surface mount package for high volume automated assembly

COMPUTER POWER

RF1K49223 - Dual P-Channel Saves Board Space

The RF1K49223 is a dual, 2.5A, 30V, 0.150 Ohm, avalanche rated, P-channel enhancement mode MOSFET, packaged in an SO-8 (surface mount SOIC) package. It features a 30V breakdown voltage, which provides extra operating guard band over competitive 20V products. It can replace two RFD15P05SM devices or two 30V to 60V P-channel devices in low-current applications in less than half of the footprint of the TO-252AA packaged RFD15P05SM. The RF1K49223 is used in products which have power-saving features to extend battery life.

Features

- 2.5A/30V/0.150 Ohm dual P-channel MOSFET
- Replaces two RFD15P05SM devices
- PSPICE™ thermal model
- Temperature compensating PSPICE model

Benefits

- Dual functions per package reduces parts count
- Consumes less than half the board space
- PSPICE thermal model provides steady state and dynamic temperature modeling capability
- PSPICE model aids in circuit simulation and reduces design cycle time

COMPUTER POWER

RF1K49224 - Complementary Pair Saves Space, Reduces Circuitry

The RF1K49224 is a complementary, 3.5A, 30V, 0.060 Ohm, avalanche rated, N-channel, enhancement mode MOSFET and a 2.5A, 30V, 0.150 Ohm, avalanche rated, P-channel enhancement mode MOSFET, packaged in an SO-8 (surface mount SOIC) package. It features a 30V breakdown voltage which provides extra operating guard band over competitive 20V products.

Replacing a N-channel MOSFET and a P-channel MOSFET in low-current applications in less than half of the footprint of the TO-252AA package, the RF1K49224 can be used in a half H-bridge configuration as a gate driver for capacitive loads such as multiple paralleled MOSFETs.

Features

- 3.5A/30V/0.060 Ohm N-channel and 2.5A/30V/0.150 Ohm P-channel complementary MOSFET
- Replaces two TO-252AA (D-Pak) packaged devices
- PSPICE thermal model
- Temperature compensating PSPICE model

Benefits

- N-channel and P-channel configurations in one package reduces part count
- Consumes less than half the footprint of a TO-252AA (D-Pak) package
- PSPICE thermal model provides steady state and dynamic temperature modeling capability
- PSPICE model aids in circuit simulation and reduces design cycle time

COMPUTER POWER

RF1K49221 - Dual Functions Reduce Parts Count

The RF1K49221 is a dual, 2.5A, 60V, 0.130 Ohm, avalanche rated, 2KV ESD protected, N-channel enhancement mode MOSFET packaged in an SO-8 (surface mount SOIC) package. It features a 60V breakdown voltage, which provides extra operating guard band over competitive 50V products. Replacing two RFD3055SM devices in low-current applications with less than half the footprint of the TO-252AA packaged RFD3055SM, it can be used in a half H-bridge configuration for power-supply applications and as a dual low side switch for general-purpose load control applications. It includes a 2KV ESD protection network for enhanced field reliability.

Features

- 2.5A/60V/0.130 Ohm dual N-channel MOSFET
- Replaces two RFD3055 devices
- 2KV ESD gate-source ESD protection
- PSPICE thermal model
- Temperature compensating PSPICE model

Benefits

- Dual functions per package reduces parts count
- Consumes less than half the board space
- ESD protection provides improved immunity to ESD failures
- PSPICE thermal model provides steady state and dynamic temperature modeling capability
- PSPICE model aids in circuit simulation and reduces design cycle time

COMPUTER POWER

Industry's First Full 4-Channel PCI Hot Plug Solution Reduces File Server Downtime

Until recently, the only way for a user to perform maintenance or expand the Peripheral Component Interface load/adapter cards in a file server was to take the system off line. Since these cards typically are high-capacitance loads, they can draw huge levels of in-rush current when inserted, dragging down the input power rail. This can be fatal to the host, often causing it to crash the system. For mission-critical file servers, this can represent several thousands of dollars per down event. Likewise, if an adapter (i.e., ethernet, 100 base T, mass storage card, etc.) was to fail or short, it typically causes the file server's motherboard power to collapse or sag, causing the system to go down. While fusing each slot helps to electrically isolate load cards from the motherboard, their response time is too slow and too crude to provide adequate protection. To avoid these downtime situations, PCI Hot Plug standards have been developed.

Harris Hot Plug Solution

Designed to meet these new standards, the HIP1011 Hot Plug Controller and RF1K49211 MOSFET eliminate costly server down time. This simple solution provides protection for all 4 voltages used by PCI adapter cards, +5, +3.3 and +/-12V. Each slot needs its own Hot Plug Controller, which is individually protected as opposed to the adapter card. This places the burden of Hot Plug compatibility with the file server manufacturer rather than the adapter card, avoiding problems with backward compatibility. Harris Semiconductor continues to develop innovative solutions in the area of hot swapping. The HIP1012, a device optimized for high-end disk drive systems (DASD) is in development.

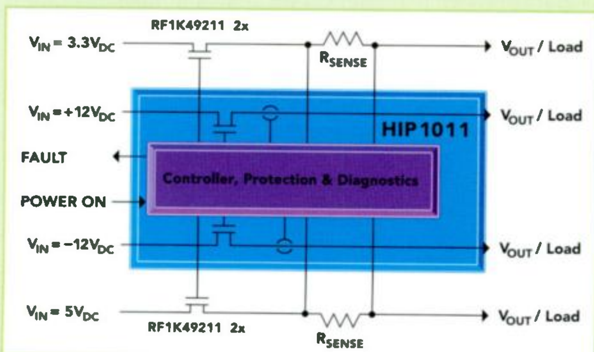
COMPUTER POWER

RF1K49211 Supporting Cost-Effective PCI Hot Plug Solution

Designed to work with the HIP1010 Hot Plug Controllers, the RF1K49211 power MOSFET, in combination with this IC, presents the designer with a solution that not only optimizes function, but also reduces cost. These large-area power devices are produced on a less complex (and less expensive) process than is necessary for the IC. This allows Harris to shrink the IC, improving the circuit solution cost once more.

Packaged in a surface-mount SO-8 package, this 12-Volt, 7-Amp device has only 0.020 Ohm on resistance, and has a logic level gate control. Because the RF1K49211 is avalanche rated, it is impervious to most transients encountered in hot-swap situations. In addition to

Functional Diagram



HIP1011 Key Features

- Load control for 3.3, 5, +/-12V
- Integrated MOSFETs and RSENSE for +/-12V
- Adjustable over-current protection for each output (electronic circuit breaker)
- Adjustable turn-on ramp rate
- Under voltage protection for 3.3, 5 and +12V outputs
- No charge pump needed
- Fault diagnostic
- 16-pin SOIC

Key Features

- 12V, 20 Ohm, N-channel MOSFET
- S08 package

the primary hot plug application, this device is ideal for 5 Volt to 3.3 Volt DC-to-DC converters, as well as general-purpose load control directly from logic ICs or microcontrollers.

Features

- 7A/12V/0.020 Ohm N-channel MOSFET
- Logic level gate input
- Lower $r_{DS(ON)}$ than a TO-252AA (D-Pak) package
- PSPICE thermal model
- Temperature compensating PSPICE model

Benefits

- Extremely low $r_{DS(ON)}$ reduces power dissipation and improves system efficiency
- Can interface directly with logic and microcontrollers or microprocessors
- Consumes less than half the footprint of a TO-252AA (D-Pak) package
- PSPICE thermal model provides steady state and dynamic temperature modeling capability
- PSPICE model aids in circuit simulation and reduces design cycle time

PCI Slot Power Specifications

Voltages	Max Load Current
5V +/- 5%	5A
3.3V +/- .3V	7.6A
+12V +/- 5%	500mA
-12V +/- 10%	100mA

Maximum of 25W per board

COMPUTER POWER

Easier Logic Level Load Control for the Low Side

Translating the logic level (5 Volt) commands of microcontrollers and microprocessors just got easier with the devices listed below. With current ratings of 45 Amps, these devices translate logic level commands into action as they control loads such as motors, inductors and transformers. "Because they were specifically designed for the 20-Volt environment, they are more cost effective than higher voltage alternatives," says Milton Peters, Product Marketing Engineer for commercial MOSFETs. These parts are avalanche rated, an added feature which helps protect them from over-voltage transients on the rail supply. Their very low gate charge per unit on resistance makes them easy to drive, an important factor when used in high-frequency applications such as DC-to-DC converters.

Engineers will have an easier time designing with the parts because their temperature compensating PSPICE electrical models aid in circuit simulation, thereby reducing design cycle time. They are available in several packages: TO-220AB, TO-262AA (through hole), and TO-263AB (surface mount).

Features

- 15A/20V/0.022 Ohm N-channel
- Low $r_{DS(ON)}$ provides cost effective, general purpose low side load control
- Logic level gate input
- Can be operated directly from 5V logic circuits
- Avalanche energy rated
- Designed for switching inductive loads such as inductors, coils, and transformers

Benefits

- Low gate charge per unit $r_{DS(ON)}$
- Low gate charge provides superior efficiency in low voltage, high frequency DC-to-DC converter applications
- Temperature compensating PSPICE electrical model
- PSPICE model aids In circuit simulation and reduces design cycle time
- Available in the TO-220AB, TO-262AA, and TO-263AB packages
- TO-263AB surface mount package for high-volume automated assembly. The TO-262AA is available for height-restricted, through hole applications

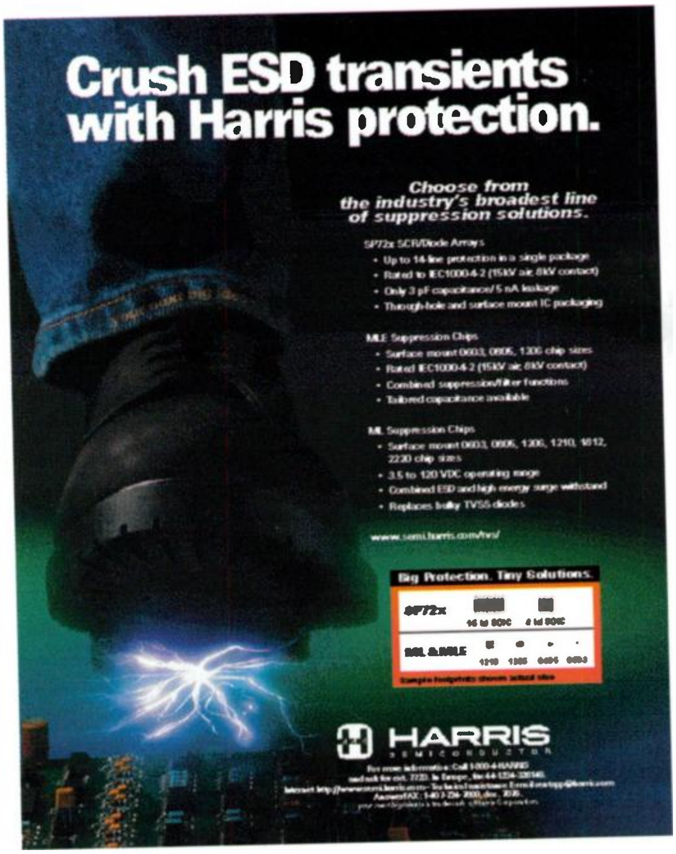
Part No.	B_{VDSS}	Polarity	$r_{DS(ON)}$ @5V	$r_{DS(ON)}$ @10V	Package
RFP/1S60P03	30V	P	–	0.026Ω	TO-220/262/263
RFP/1S70N03	30V	P	–	0.010Ω	TO-220/262/263
RFP/1S42N03L/SM	30V	P	0.025Ω	–	TO-220/262/263
RFP/1S42N03	30V	P	–	0.025Ω	TO-220/262/263
RFP/1S45N02L/SM	20V	P	0.022Ω	–	TO-220/262/263

What's New in Suppression

UltraMOV™

Harris has just introduced the highest surge current rated series of radial MOV (UltraMOV), complementing its LA and C-III series of radial varistors. These devices, intended for AC line applications, are high current and energy MOVs covering 130V to 625Vrms applications. This new series is offered in radial lead disc sizes of 7, 10, 14, and 20mm, with peak surge current ratings of up to 10kA (8x20uS).

These devices provide new options for TVSS OEMs in meeting new surge requirements, as specified in the new UL1449, rev. 2, as well as the space constraint concerns of many designs. In addition to this portfolio, Harris is also offering a super high current 20mm radial MOV series, rated for 12kA. These parts are designed for operation in TVSS/UL1449 applications.



ML Nickel Barrier End Terminations

Although they say it can't be done, Harris has proudly introduced the world's first nickel barrier end termination option for its multilayer series of leadless surface-mount suppressors. This option offers an alternative to two standard silver end termination finishes. The new nickel-tin material is suited for either reflow or wave solder operations. It is intended to address those applications that do not permit silver end terminations or otherwise prefer this finish. This option is available for the ML and MLE series suppressors; the new data sheets describe how to specify it when ordering.

Gas Discharge Tubes

Your one stop for suppression devices is further extending its offerings with the introduction of the Harris Gas Discharge Tube Series. Harris has now added this important technology to the MOV, Multilayer, Silicon Arrays, and Surgector™ devices to provide the most comprehensive portfolio from any single source! GDTs have long been the transient voltage product solution for telecom applications, suited for AC line operation as well. In fact, MOV/GDT combinations are often used to address high surge energy needs and demanding clamp performance requirements. Devices will be available along with the new "GDT" brochure in November.

SP72X IC Arrays

This series of SCR-diode arrays, with its very low capacitance and leakage, has become a hero in protecting data/signal line circuits from ESD and other transients. In fact, the new SP723 is rated to the highest level (level 4, 8kV contact) of the IEC 1000-4-2 ESD standard. The SP720, 721, and 723, offer the designer flexibility in terms of the number of lines protected and package styles for through hole or surface mount, and we're not stopping there. Right now we are developing new SP devices that will further extend protection performance and offer new package options.

Ultrafast IGBT Challenges MOS

In designing power converters today, one of the most difficult decisions facing designers is which device to use for the power switch.

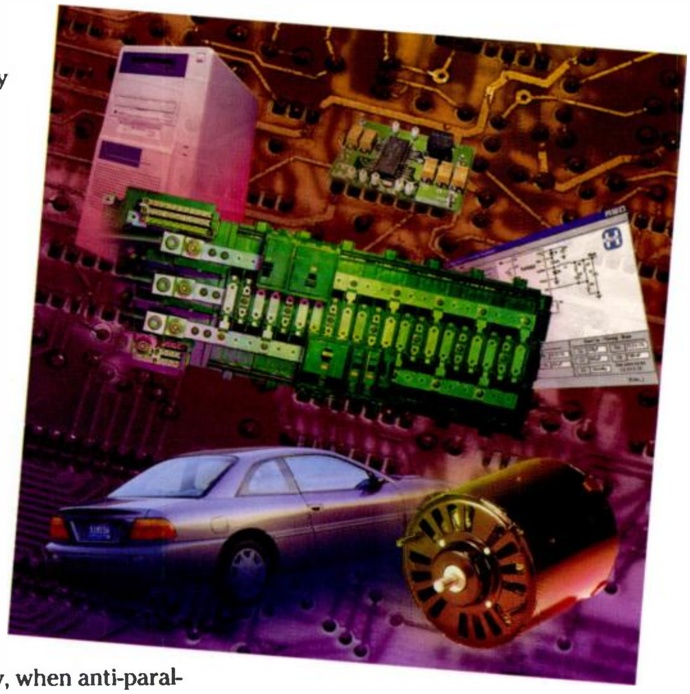
IGBT Competes with MOS Switches

The invention of the IGBT, with substantially higher current densities and lower $r_{DS(ON)}$ across the operating temperature range, provided a powerful competitor for the PowerMOS transistor, particularly at lower frequencies. The IGBT slowly evolved into new-generation offerings, improving operating frequency and saturation voltage. Suddenly designers were able to control the bipolar fall time tail, and standard operating frequencies of 50kHz at rated current became available. As quickly as these products were put on the market, designers began to displace MOS switches with the higher performance IGBT.

Now the operating frequency boundary can be extended to 60kHz or higher.

Circuit Configuration Determines Selection

Whether to select an IGBT or PowerMOS transistor is determined by circuit configuration, but it's clear that at 100kHz and lower, the IGBT usually represents the best choice. Usually, when anti-parallel diodes are needed, IGBTs in combination with optimized discrete diodes can handle more current than any PowerMOS transistor. In applications where no anti-parallel diodes are needed, the IGBT offers the chance to save silicon die area, and therefore costs, up to switching frequencies of about 60kHz.



Harris Semiconductor World Wide Web Site Now on CD-ROM

The Harris Semiconductor Design Resource CD includes all of the most recent information included on our web site, including product specification data sheets, applications data, and more.

The CD was developed to provide more direct and, in most uses, faster access to data than is typically achieved when the web is accessed via modem. It is also, of course, valuable to many customers who do not have access to the Internet.

The Design Resource CD has many helpful features built in. It uses its own browser and search engine for immediate random access to any desired information. It also contains Harris Hot Links, which allow users with a web connection direct access to the most up-to-date specifications and information. Further, all data sheets are in industry-standard Adobe Acrobat™ .pdf format and can be printed on local printers.

To order your copy of the Design Resource CD-001, please call 1-800-4HARRIS, ext. 7745.

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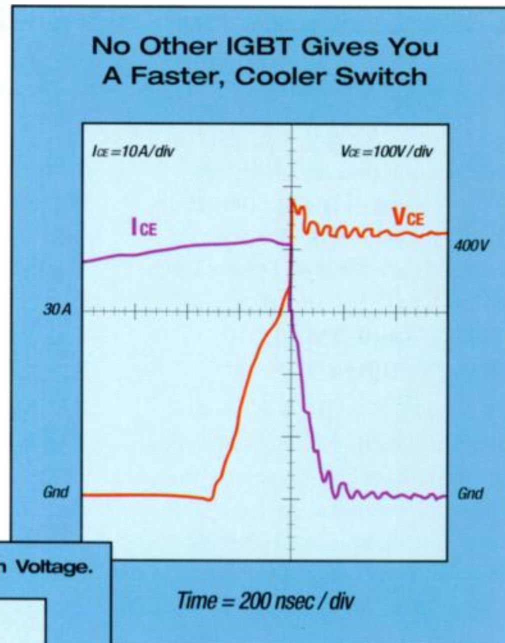
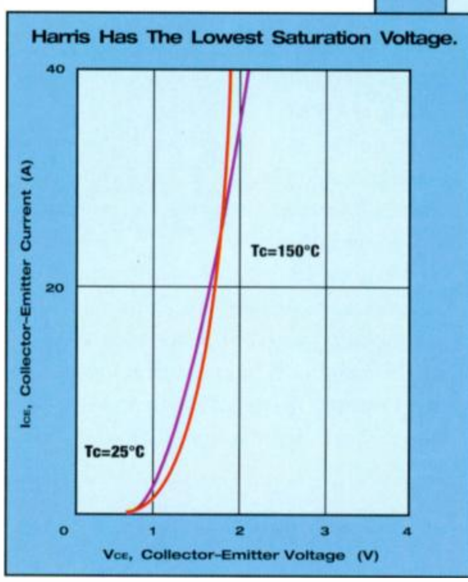
Ultrafast IGBT Solutions Cut System Costs

Harris B-Speed IGBT's
- Fast 140ns fall time
- Low on state voltage drop
- Square switching SOA
- Lower cost



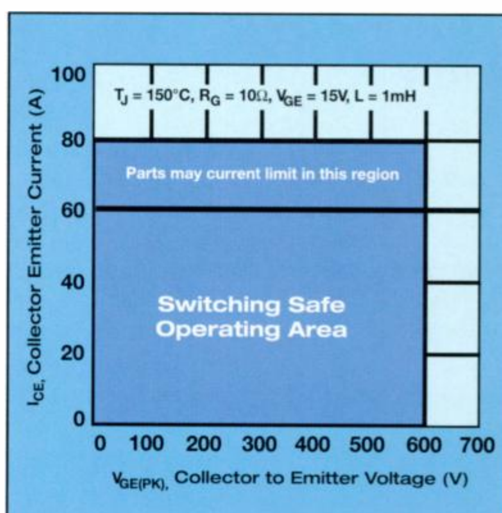
Third-generation Ultrafast IGBTs developed by Harris Semiconductor offer the lowest saturation voltages and turn-off energy, combined with the highest current densities, in the IGBT market. These UFS IGBTs can reduce part counts and lower system costs.



Features include high operating frequency, reduced conduction loss, more rugged circuit capability, improved hard-switching capability and improved circuit fault tolerance.

Harris was first in the industry with a 600V IGBT assembled with a size 1 die. This IGBT outperforms MOSFETS at 50 kHz and lower switching frequencies in a *non-derated part*. Harris was also first with a 600V IGBT, which challenges size 3 MOSFETs in the application of fractional horsepower motor control and line voltage switching power supplies.

The UFS series offers a full selection of B-Speed, C-Speed and Rugged IGBTs. Applications include switched and resonant mode power supplies, AC motor control, DC servo and robotics drives, uninterruptible power supplies, battery chargers and DC choppers and welders.



INDUSTRIAL

Rugged IGBTs Reduce Circuit Failure

More efficient AC motor controls, DC servo and robotic drives, DC choppers and anything requiring short circuit withstand capability can be built with Harris Rugged Ultrafast IGBTs. Rugged switches, such as the HGTP20N60C3R, meet the most demanding requirements of the motor drive industry by delivering 600V/40A muscle at 25 DEG, 20A @ 110° C.

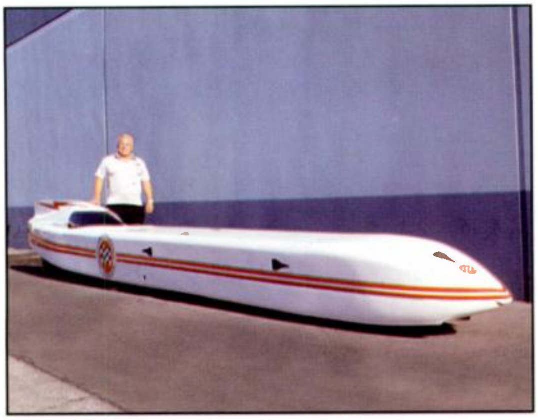
With an industry-first rating at 480 volts and 150 DEG C, Harris Rugged IGBTs withstand 10µsec of Short Circuit Withstand Time (SCWT). The tailored dV/dt improves motor reliability and reduces RFI and EMI. Switching speed meets industry standards and, coupled with low VCE(on), reduces energy losses. Fall times are tailored for motor control with 330ns typical hot inductive. Switching speeds are also tailored to industry requirements with square switching SOA of 80 Amps.

Features:
- Guaranteed 10µsec SCWT @ max junction temp
- Soft dV/dt reduces RFI & EMI in circuit
- Reduced conduction loss
- Improved hard switching
- Low on-state voltage drop of 1.8 typical at 25C

Benefits:
- Smaller heat sink requirement
- Simplified circuit design
- Reduced circuit failure
- Lower system costs
- Lower assembly costs

AUTOMOTIVE

Advanced Electric-Powered Streamliner to Reach 300 mph



World Record Performance Associates of Santa Ana, California is recognized worldwide for the design, construction and racing of some of the world's fastest vehicles. In August and October 1997, a new, totally electric streamliner land speed vehicle will be tested and run at the Bonneville Salt Flats. Harris IGBTs will play an important role in helping this advanced racing machine approach or exceed 300 mph - powered only by an advanced design battery pack. Harris devices were selected because they offer the most efficient power switching available. The IGBTs help the driver precisely control power, with minimum losses, to a pair of 200hp motors. Follow this exciting performance breakthrough at our web site:

www.semi.harris.com/saltflat/

NORTH AMERICA

Sales Office Headquarters

Harris Semiconductor
2401 Palm Bay Road, N.E.
Palm Bay, Florida USA 32905
TEL: 1-800-442-7747
(407) 727-9207
Extension 7745

Authorized Distributors

ALLIANCE ELECTRONICS
1-800-608-9494
ALLIED ELECTRONICS
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ZEUS ELECTRONICS
1-800-524-4735*

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EUROPE

Sales Office Headquarters

Harris Semiconductor
Mercure Centre
Rue de la Fusée 100
1130 Brussels, Belgium

Harris Semiconductor Information Centre
Osprey House
Berkeley Business Park
Finchampstead,
Berkshire RG40 4YJ, England
Fax : 44 -1189 328148

Sales Offices

FRANCE
Harris Semiconducteurs SARL
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Harris Semiconductor GmbH
Kieler Strasse, 55 - 59
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UNITED KINGDOM
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and fluctuations in the target markets.

Right away, cable sizes can be reduced when using the higher distribution voltage of a DPA, compared to a centralized approach. At 48 V, only 10% of the conductor cross section is needed, compared to distributing 5 V centrally. Also, the effect of any voltage drops is significantly reduced. The same current benefit means that 48-V power can be brought onto a board without needing multiple connector pins or special connector types to achieve the current loading.

In addition, by bringing the regulation closer to the load, elements of the system are effectively decoupled from each other. This technique greatly simplifies the design, especially for advanced, high-speed circuits, since each board can be considered a self-contained entity. This is increasingly important as power-supply requirements go from just providing X volts at Y amps, to providing tight dc-voltage regulation while handling dynamic current requirements and managing high-frequency noise. A DPA, with dc-dc converters on each board, inherently provides a level of isolation from both low-frequency and high-frequency effects elsewhere in the power system. With these effects out of the way, designers can focus on handling the local dc-voltage, dynamic-current, and local high-/low-frequency problems.

On-Board, DC Voltages

With increasing power density, on-board power distribution, even with DPA, needs careful consideration. The use of multilayer boards with a dedicated earth plane is well known, and a valuable first step, but sizing the power traces is still important. A useful aid is the normalized graph *(Fig. 3)*. This plots trace width against maximum bus length for a range of voltages, assuming 35-µm copper (1oz /ft^2), 1-A current, and a maximum permitted volage drop of 1%.

For a given voltage, the chart allows the minimum trace width for the estimated, or actual, trace length to be found. It also can indicate the limitation to be placed on trace length for a given trace width. The chart can be used for other voltage-drop limits, currents, or for thicker copper, simply by applying a suitable multiplier. For example, for a 2.5% maximum voltage drop, multiply the maximum length by 2.5 or reduce the trace width by a factor of 2.5.

Dynamic Voltage

For dynamic voltages, consider a simple example where a 5-V, 1-A supply needs to provide an additional 100 mA, with a 5-ns response, with less than 4% voltage change. An initial analysis of a 12-cm long, 1.5-mm wide, 35-µm trace with earth plane return shows a 42-Ω resistance, which gives a steady voltage drop of 42-mV, and a change of only 4.2 mV, well within the 200-mV requirement.

The problem, however, is that 5 ns is not dc. Considering the converter, for the moment, to be an ideal component, the inductance inherent in the power trace will limit performance, as predicted by the equation for lumped inductance:

$$\Delta V = -L\left(\frac{dI}{dt}\right)$$

A more accurate model is to consider the trace as a distributed inductance, combined with the beneficial effects the capacitance of the trace has on the earth plane. The dynamic impedance of several typical configurations is shown in the table. If our example is a two-layer board with an earth plane, 50 Ω would be a typical value, very different from the dc resistance. In addition, dc-dc converters are real, not ideal, components, and they have a finite ability to supply transient currents.

One reason why that is the case is the frequency of operation, since even a 500-kHz converter will require 2 µs to deliver extra power. The total energy-transfer capability will be determined by the specific converter topology and implementation. Several cycles may be needed to deliver increased power. Check the data sheet of the converters you are considering to ensure that they have a suitable dynamic response. Vendors' application teams should be both able and willing to help determine dynamic response for specific applications.

One method to improve transient response is to provide local distributed capacitance within the on-board power distribution. The values will depend on the transient capability of the converter, and the overall distribution network. Returning to our simple example, typically the converter/distribution response will enable the dynamic power to be controlled within 40 µs, and after perhaps 200 µs, the current can be treated as dc. To calculate the capacitor needed, use the formula C = I(dt/dV). Using our values of 100 mA, 40 µs and 200 mV gives:

$$C = (0.1)(40\times10^{-6})/(0.2) = 20\ \mu F$$

It should be noted that some dc-dc converters do not limit the rate of rise of voltage at turn on, and exhibit an overcurrent condition if large values of capacitor are fitted. However, if the total capacitive load is less than 100 µF/A, it should not be a problem.

Additionally, it is important to apply the usual good practice of distributing a network of low-ESR, low-ESL, high-frequency capacitors around the circuit to supply the very fast, 10-ns-order, switching transients needed by digital circuits. Since capacitors in parallel add, while the effective inductance and resistance drop, the effect of multiple high-frequency capacitors on C/R and C/L ratios is magnified. Therefore we have three levels of decoupling: bulk electrolytic for low frequencies, distributed ceramic for mid-range frequencies, and the pc-board dielectric for very high frequencies.

Designers should not be tempted, however, to simply add a bit more for luck, because large capacitor values, (i.e. over 100 µF/A), can have negative effects, including longer settling times, lower converter bandwidth, reduced phase margin, and possible instability. Check the data sheet and application notes from the prospective vendor and, if in doubt, talk to the support engineers about the application.

While considering decoupling, it is worth emphasizing that although the noise generated by dc-dc converters is usually within the ripple requirements, in extreme cases, some additional filtering may help. However, with the high frequencies of 500 kHz and above, the size of components needed for either RC or LC low-pass filters makes them an easy addition.

With this level of challenge likely to be dwarfed by future technologies that are heading down toward 1.3 V, with powers up to 70 W, and dynamic requirements an order of magnitude tougher, taking distributed power right up to the processor for maximum control may well provide the only practical solution.

Fault Tolerance And Upgrading

Although a DPA inherently provides significant fault tolerance when applied as power per board, let us not lose sight of the fact that instead of one large supply, we now have 10, 50, or even hundreds in a large system. The goal is not just to behave well when there is a failure, but to get closer to no failures. For a system with 100 individual converters to average only one failure every five years requires a mean time between failures of at least 500 years.

The extremely high demand for standard converters has gone a long way toward helping achieve this goal by providing ideal opportunities for successful investment in production processes and automation to raise reliability to new levels. Designers should check the cumulative effect of module life expectancy on the overall system.

Despite these high levels of reliability, failures can still occur. By breaking down the power supply into a distributed solution, however, a DPA immediately limits the impact of a power fault. This advantage not only makes the fault easier to isolate, it also allows for hot swapping. In addition, with the fast response of high-frequency converters, a DPA offers quick and controlled start up of inserted cards.

The four basic failure modes that are possible for the converter range from degraded performance, to stoppage, to loss of regulation, to input short circuit. The first two should be included in the diagnostic scheme for the system as a whole.

Overvoltage occurrences with centralized systems can cause damage throughout the system, so many complex schemes have been devised to protect against it. The problem is only exacerbated by excess voltage capability to compensate for busbar voltage drops. Power-per-board converters in a DPA not only limit the scope for damage and have much-less-vulnerable, fully integrated feedback loops, but in many cases include limited overvoltage capability, such as 7 V for a 5-V supply. Compared to the integrated feedback loop of the converter, external feedback is usually introducing an extra failure mechanism. But linking a module's remote-control pin to a voltage-detection system to shut down under overvoltage conditions can be a straightforward protection scheme.

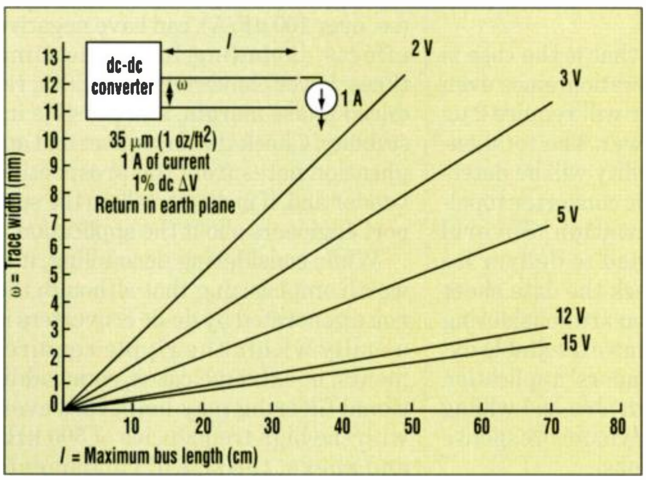
To handle excessive input current, it is important that the distribution system is correctly fused and sized, remembering to take into consideration not only the normal load, but the rated full-power capability of the module. Most converters will include an overcurrent protection mechanism, and it is important to take this into account when considering the local fault effects.

Whether the circuit shuts down completely, automatically tries to reset, or operates in current limited mode has impact on distribution design and sizing of local tracks. Converters which shut down may require external cycling circuitry to bring them back up after a fault.

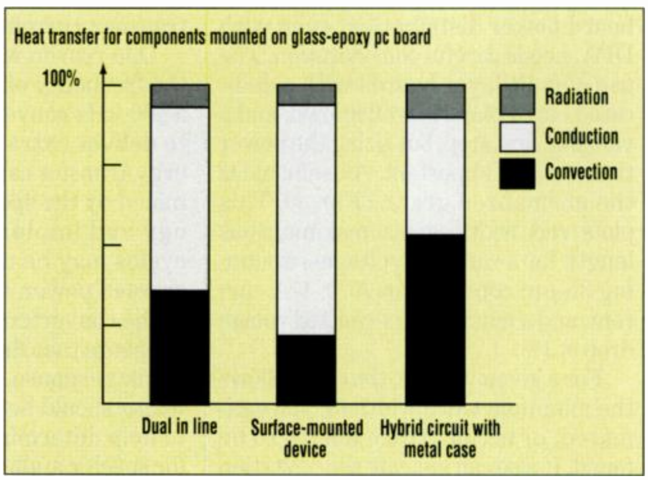
Thermal Issues

The dispersed nature of a DPA provides the major benefit of spreading the heat around the system—reducing the problem of local hotspots. But there are still many aspects of thermal design to consider for an effective system. Since power consumption is fixed by the system load, converter efficiency has a major impact on heat generated, though skillful internal design can result in apparently similar converters having very different thermal limits. When comparing efficiencies, don't forget to check that the figures are linked to the power level, particularly when, for the purposes of standardization or availability, a module is used below its rated power. Certain topologies lose efficiency at low loads, which can compromise an overall thermal budget.

At the basic level, a decision has to be made on whether the system will require forced cooling or rely on convection, trading a higher power density for the additional design requirement for sufficient cool airflow. It is



3. This normalized graph helps to size the required power traces. This graph plots trace width against maximum bus length for a range of voltages, assuming 35-mm copper (1oz /ft2), 1-A current, and a maximum voltage drop of 1%. For a given voltage, the chart allows the minimum trace width for the estimated, or actual, trace length to be found. It also can indicate trace-length limits.



4. The dispersed nature of a DPA provides the major benefit of spreading the heat around the system, reducing the problems of local hotspots, but there are still many aspects of thermal design to consider for an effective system. Bear in mind the differences between the heat transfer modes for different package styles, and to appreciate whether the converter requires additional heatsinking for rated performance.

TYPICAL IMPEDANCE FIGURES FOR VARIOUS BOARDS

Circuit-Board Configuration	Dynamic Impedance (Ω)
Multilayer board with a dedicated plane for each voltage plus earth plane that assumes 0.8-mm glass-epoxy dielectric.	1 to 5
Two-layer board with a complete earth plane that assumes 1.6-mm glass-epoxy dielectric.	20 to 60
Two-layer board with an incomplete earth plane that assumes 1.6-mm glass-epoxy dielectric.	50 to 100
Single-layer board that assumes 2.5-mm typical voltage-bus width.	>100

useful to bear in mind the differences between the heat transfer modes for different package styles, and to appreciate whether the converter requires additional heatsinking for rated performance *(Fig. 4)*. Careful planning when mounting the converter can pay dividends, especially for the increasing range of surface-mount components for which conduction through the leads is an essential cooling mechanism. The mechanical and space implications of this design can be critical.

The thermal resistance between the internal semiconductors and the outside world is a major factor for converter manufacturers in determining the maximum temperature of operation. Avoiding hotspots is particularly critical. Ensuring that maximum ratings are not exceeded, remember the rule of thumb is that the MTBF drops by a factor of two for every 10°C temperature rise. As a result, operating temperature, energy density, and reliability are considered together.

Once the total heat dissipation is calculated, and estimates have been made of the resulting ambient temperature, review the effect on case temperatures, and the resulting impact on converter power rating. Often, it isn't possible to achieve all the component ratings at the same time, so check whether the power must be derated at the anticipated operating temperature. Some power modules can achieve less than one-third of their 20°C rating at an 85°C case temperature.

Selection Criteria

Three important parameters on the data sheet, efficiency, operating temperature, and reliability are interrelated, and, unusually, do not require a trade-off. They actually reinforce each other. Efficiency is key to determining the thermal conditions, but ensure that the efficiency figures relate to the actual operating power level planned. Look for power/efficiency curves for maximum confidence.

Operating temperature is usually specified depending on the predominant cooling mechanism. For example, pin or case temperatures limit the power achievable from a given design. The higher the rated temperature, the more power you're likely to be able to use in practice.

Reliability is unusual in that it is not directly measurable. It is, therefore, important to question the estimation method, and particularly the temperature assumed. Check for the supplier's failure-rate database and field history to understand the confidence level behind the specification. A module manufacturer's 100% burn-in before shipment can have a significant impact on in-system yield.

For power-per-board applications, excessive weight can require extra strengthening of the board, yielding cost and space penalties. While the internal topology and operating frequency are big issues for converter designers, they have less impact on users. Most modern products will offer levels of regulation and voltage accuracy which will comfortably meet requirements. Of more importance is the practical power density achieved in each specific application, so don't just look at the headline power rating, check it out in your system, with your cooling, at your ambient temperature and with your required reliability.

Cost

The pace of progress and competition means that midlife upgrades and flexible system configuration are necessary engineering responses to marketing pressure. With a DPA there are no constraints on the use of new or different technologies, since each board contains all the power conditioning necessary for its own operation. It also is much more cost effective to use a common system cabinet, and then add the individual converters as each new function is plugged in. Users of simpler systems are not paying for capacity they don't need, but when their needs grow, the option is there to expand at a relatively low cost.

The biggest impact on cost, however, has been the widespread use of distributed modules in telecommunication systems. The quantities required have not only offered suitable payback to justify very advanced manufacturing investment, they also have taken some manufacturers up the yield learning curve very quickly. Integration and automation hold the key. For example, using an in-house, high-voltage, power-semiconductor IC fabrication facility, Ericsson Components has reduced its advanced ceramic thick-film hybrid-technology power-module component count down to around 20, with only two semiconductors *(Fig. 1, again)*.

Nonetheless, cost is a bigger issue than just the purchase price of the converter. Assembling that converter onto the application board also is important. The latest generation of surface-mount modules suit the weight limit of vacuum actuators on standard pick-and-place machines. The modules can be assembled onto boards in an automatic in-line process, on the same equipment, and at the same time as the other components. No expensive additional handling or processing is required. With MTBF figures now proven in excess of 560 years, spares holding and field maintenance costs also are reduced.

Lars Thorsell is the strategic marketing and deputy general manager at the Power Modules Department of Ericsson Components AB, Energy Systems Division, Sweden. A committee member of the European Power Supply Manufacturer's Association, Thorsell received his BSEE from Stockholm's Technical Institute in 1969.

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Redundancy And Hot Swapping Keep Systems Running

In Markets Where Downtime Is Unacceptable, High-Availability Systems Are A Prerequisite.

BY PAUL O'BOYLE AND STEVE KUGLER

Kepco Inc.,131-38 Sanford Ave., Flushing, NY 11352; (718) 461-7000; fax (718) 767-1102; http://www.kepcopower.com

The need for systems to tolerate failures without interrupting service has grown in step with the rapid deployment of electronic systems in applications such as data processing, financial and equities services, telecommunications, and transportation. Many of these systems have on-line; real-time; and, in some cases, safety-related, requirements. Along with our dependency on these systems comes a rising intolerance for downtime that would impact customer service, sales, and, ultimately, corporate profits.

Regardless of the reliability and backup contingencies built into the system, if power is not available, the system won't operate. N+1 redundancy and hot swapping offer a means of ensuring uninterrupted operation if a power fault occurs. Implementation of fault tolerant power systems is now becoming standard for many systems and networks where even short periods of downtime can significantly affect processes or services *(Fig. 1)*.

Before a reliable N+1 scheme can be implemented, a number of critical questions must be answered:

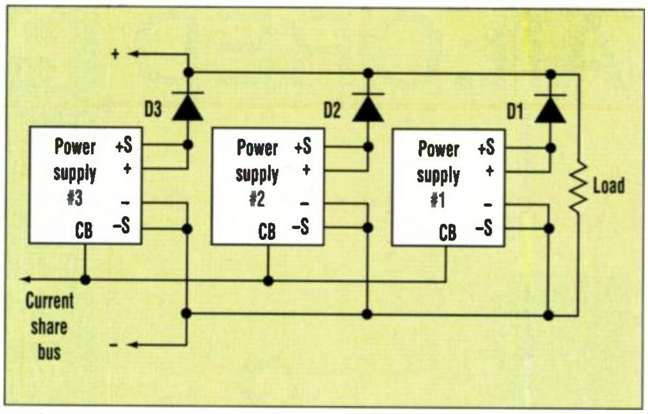
- How much power do I need?
- Do I need current sharing?
- How does current sharing work?
- How do I detect failures?

In addition, basic terminology, such as the difference between OR-ing, blocking, isolation, and steering diodes, can often lead to confusion.

A critical link in all electrical/electronic industrial systems is the need to convert source power, typically from the ac mains, to isolated, regulated, and conditioned low-voltage dc power. N+1 redundancy ensures continuity of this power through the use of a power conversion system that can tolerate a fault to one component without losing

1. The HSP series of 1000-W power supplies comply with many requirements of the fault-tolerant systems now becoming pervasive in data-processing, telecom, financial, and transportation systems. These requirements include N+1 redundancy with current sharing, hot-swappability, and universal input-voltage ranges.

system functionality. An extension of this, an N+2 system, can tolerate a fault to two components. Closely linked to redundancy is the concept of hot swapping, the ability to remove and replace a failed unit without removing power to the system or compromising system functionality. This feature becomes important once a failure occurs in the N+1 system. The benefits of N+1 redundancy are greatly reduced if the system must be powered down in order to locate and replace the failed unit.



2. Three power supplies paralleled with forced sharing. Blocking diodes D1, D2, and D3 keep each supply isolated from each other, allowing the system to continue operating if one power supply fails.

How Much Power?

To evaluate how much power is needed for an N+1 redundancy system, first establish the power required for the load. Then, determine the minimum number of units that can supply that power. Add one for an N+1 system, add two for an N+2 system, and so on. For example, if you're operating a 48-V rail that must maintain a minimum of 2 A to its load, you might use two 2-A units in parallel. This technique is N+1 redundancy, since the system could still supply 2 A to the load if one unit failed. If you use three 1-A units in parallel, you would still have N+1 redundancy, since the system could still supply 2 A to the load if one unit failed. If you used three 2-A units, you would now have N+2 redundancy, where the system will tolerate the failure of two units simultaneously without affecting system operation.

Do I Need Current Sharing?

An example of a simple N+1 redundant system might be three 1-A power supplies connected in parallel to supply a load with 2-A. If current sharing is not implemented, the nature of voltage sources dictates that the power supply with the highest voltage (one will always be slightly higher than the others) will supply all the current to the load until it reaches its current limit. It then becomes a current stabilizer, and its voltage drops to the level of the next-highest supply which assumes the role of voltage stabilizer. Only after it goes into current mode will the next unit assume part of the load, and so on. The last unit, the one with the smallest voltage setting, ends up controlling the voltage and provides the least current.

The principal disadvantage of this method is that the power supplies will be loaded unequally, leading to increased power-supply failure rates. A further disadvantage is that the voltage seen by the load will change slightly as each unit goes into its current limit and passes voltage control to the next lowest unit, leading to degraded transient recovery in the event of a power module failure. To improve reliability and transient recovery, modern power supplies designed for N+1 redundancy must have either a passive or active means of forced current sharing so that all units share the current load equally *(Fig. 2)*. Current sharing results in lower operating temperatures and reduced failure rates, as well as improved response time, while the cost and complexity of the actual circuitry is low.

How Does Current Sharing Work?

Passive current sharing can be implemented in applications where poor load regulation can be tolerated. If two poorly regulated supplies are connected in parallel, the output voltage decreases as the output current through the power supply set at the higher voltage increases. At some point, the second power supply will begin to supply more of the current, resulting in automatic load sharing. This design requires no additional circuitry and is fail-safe, but depends on poor regulation to operate properly.

Active or forced current sharing is a form of master-slave operation in which the current supplied by the master is measured and the other units are controlled to match the current, ensuring that they are all equally loaded *(Fig. 3)*. The load-share or current-share bus signal line represents the highest current output of any one supply. This line is fed back to each power supply in the system and compared to the actual current being supplied by that unit. If the current-share-bus (CSB) voltage represents an unequal load share, the CSB voltage will be higher than the current-share line for that unit, requiring that unit to supply more current. The nature of the circuit dictates that it will stabilize when all units are supplying an equal share of the current. A requirement of N+1 redundant systems employing load sharing is that all modules in the system must be able to be preset to the voltage being supplied by the system.

Detecting Failure

N+1 redundancy offers an enormous increase in system reliability since two units would have to fail simultaneously for the power system to fail. If, for example, the failure rate of one unit is 10 x 10^5 (equivalent to a MTBF (mean-time between failures) of 100,000 hours), the failure rate of the N+1 system is approximately (1 x 10^5) x (1 x 10^5) or 1 x 10^{10}, equivalent to a MTBF of 10 billion hours. This amounts to an enormous increase in reliability. Obviously, for the N+1 redundant system to work, it must recognize that a failure has occurred and be capable of indicating which component or unit failed without shutting down the system. The detection scheme should accurately and consistently identify and localize a failure to a specific replaceable module. Without built-in circuits to identify and localize the fault, it is impossible to determine which unit needs servicing while maintaining system power. The same circuits that monitor power-supply outputs in order to detect fault conditions can also be used to provide indications that a fault in a particular module exists. Relay contacts can be a convenient way of providing electrically isolated fault indications.

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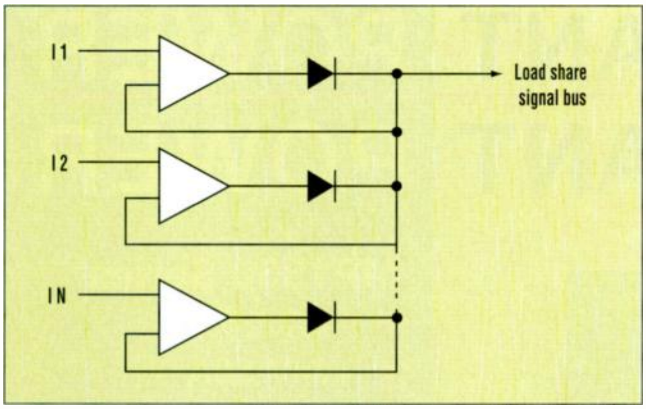
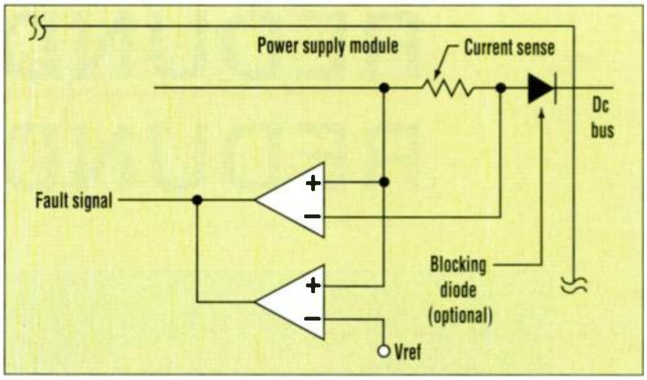


3. This simplified schematic diagram of a current sharing circuit shows blocking diodes. The load-share or signal line represents the highest current output of any one supply. This is fed back to each power supply in the system and compared to the actual current being supplied by that unit.



4. Simplified fault detection circuit that monitors output voltage and current. The circuit detects faults even if the blocking diode shorts out. The load-sharing signal, which essentially determines which power supplies are providing current to the load, and how much, would be used for current monitoring in real-life N+1 systems.

Fault detection goes hand in hand with fault isolation, which isolates the power system from any adverse effects of a failure. These functions are the basic elements of any fault-tolerant power system. The following examples are offered to illustrate the difficulties involved.

Output Low Faults—Consider the method for detecting an output low (undervoltage) failure. For a single power supply, the fault detector need only monitor output voltage (or current, in current-stabilized applications) to determine if the output is operating within specification. Any power-bus fault must be caused by the failure of the one and only power supply. In the case of the simplest N+1 system, that of two output-paralleled power supplies, the task becomes much more complex. If the output of one of the power supplies fails low, the other power supply will continue to support the load. The fault detector must be capable of determining that a fault has occurred, and which of the two power converters is defective so that the power system can be serviced. The problem intensifies when three or more power converters comprise the power system.

Several schemes can be implemented to address this problem. The most direct method is to insert a diode in series with each output between the power converter output and the power bus, and to monitor the output of the power converter itself. Called OR-ing, blocking, isolation, or steering diodes, these diodes all perform similarly in different circuits, while performing all four functions. The diodes isolate (block) the output of each unit from the power bus, allowing the fault detector to report a failure, while OR-ing (or steering) the current output of each unit to be applied to the load. The diodes isolate the current share bus of each unit so that a failure of any unit doesn't affect overall functioning of the N+1 system, while at the same time performing an OR function to allow the voltage representing the power supply providing maximum current to control the current-share bus *(Fig. 3, again)*.

In the event of an output low fault, in this example, the diode blocks the power-bus voltage from forcing the power converter output high, and the fault detector of the defective converter can now measure and report the output failure.

There are problems with this approach, however. Since all of the load current drawn by the power bus flows through these diodes, they are normally quite large and expensive, and in most applications require some amount of heatsinking. These diodes are essential only for hot-swapping applications. If redundancy and fault indication are needed, but not on-line replacement (hot swapping), efficiency can be greatly improved by eliminating the blocking diodes. Furthermore, if the blocking diode fails shorted, as is most common in these applications, the fault detector cannot detect low-output failures unless additional circuitry is employed to monitor the voltage drop across the diode. This circuitry must be capable of distinguishing voltage drops of the same order of magnitude as the output ripple voltage, and in applications where power bus load current varies significantly, this technique can be very inconsistent.

A solution that avoids most of the above problems is to use blocking diodes and monitor both output voltage and current of each module *(Fig. 4)*. In the event of a power module failure in which the output fails low, the fault detector will sense that no current is supplied to the load and indicate a fault, even while the bus voltage remains high. This form of fault detection also works with a shorted blocking diode, since module current, not voltage, is the key parameter being monitored. The only requirement is that forced load sharing be used, since the load-share signal forms the basis for the operation of the module current detector.

Output High Faults—Similar problems exist for output-high (overvoltage) failures. Consider the same two power converters operating in N+1 redundancy, now with output-blocking diodes installed. If one converter fails output high, the second converter senses an overvoltage condition and stops delivering output power. This feature avoids the pitfall of having all of the output-paralleled power converters follow the defective module into overvoltage (often called "selective overvoltage"), but now both

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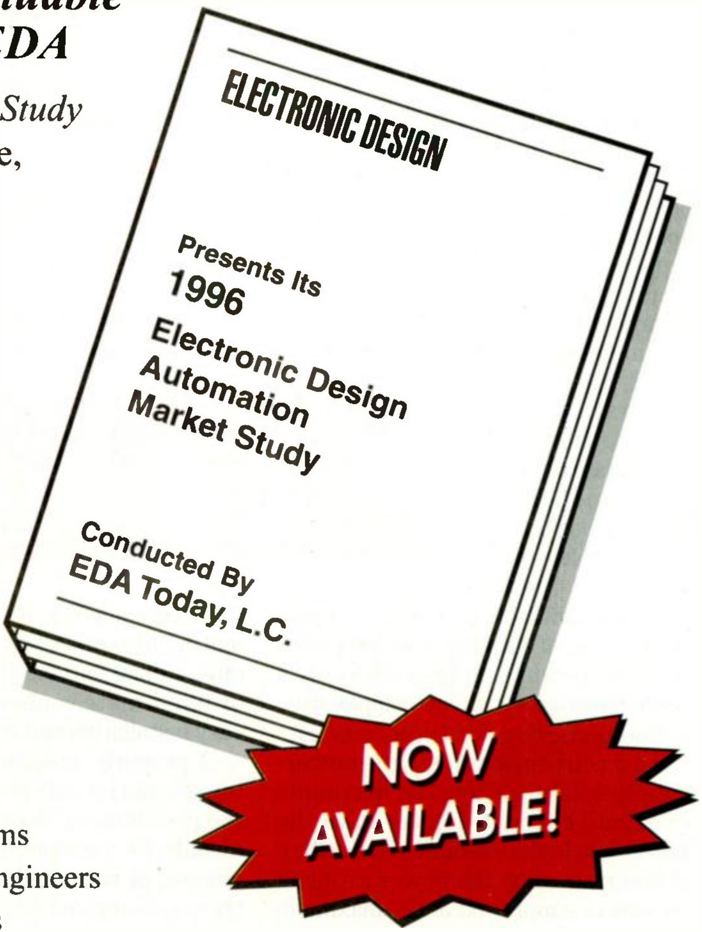

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power supplies will show an output fault. If the power supply with the output-high fault shuts down. the second converter will recover and the fault signal will be valid. However, if overvoltage shutdown does not occur, it is impossible to determine which power converter failed.

A better way is for the fault detector to monitor both the power bus voltage and the current delivered by each power supply to determine whether or not each power converter is operating properly. This technique improves the accuracy of the detector circuit while negating the need for blocking diodes.

This method is not entirely foolproof, however, since it cannot detect shorted blocking diodes, nor does it eliminate their need in hot-swap applications. Nevertheless, it is the most complete and accurate method presently available to determine operating status of output-paralleled power converters while on-line, with only a modest increase in circuit complexity.

Compensating For Load Failures

In a conventional, single-power-supply configuration, the maximum overload current delivered to the power bus in the event of a load failure is determined by the power rating of the power supply and/or the maximum current limit setting. The use of high-redundancy power systems (N+2, N+3, etc.) creates special problems, especially in telecommunications applications where the power supply must operate in both voltage- and current-stabilized output regulation modes. Excess capacity can be dangerous if the power bus is shorted, and all of the power supplies deliver their maximum output current through the system's load wiring. Thermal damage and even insulation fires are possible.

Solutions include distributed-load-protection devices (fuses, circuit breakers, thermistors, etc.), and sizing of load wiring based on maximum possible current delivery of the power system. Many power supply designs include either fixed or optional time-out circuits as part of the overcurrent-protection circuitry. These circuits shut down the power supply after 10 to 30 seconds on the assumption that long-term overloads represent major load problems that have already compromised the system. Be aware that this is not a viable option for power supplies supporting battery-based power buses, such as in many telecommunication applications, where long-term current-stabilized operation is a normal operating condition.

Other Considerations

Connector design must be carefully considered to permit removal and insertion of power modules with power applied. The connectors used for hot-swapping must incorporate protection against arcing, since nonenergized contacts will come into contact with energized components. Reliable connector mating also must be a consideration, often calling for guide bars, guide pins, or blind-mate connectors to ensure easy installation and removal.

> "...fault-tolerant power systems require separately generated and protected power sources for each of the power converters..."

A properly designed hot-swap system should include protection against the possibility of installing the wrong module, for example, one with a different output voltage. Most importantly, the power bus must be protected from excessive transients due to the charging of the output power capacitor which can occur during insertion or extraction of the power supply module.

True fault-tolerant power systems should address loss of source power as well as loss of power conversion. Indeed, many fault-tolerant power systems require separately generated and protected power sources for each of the multiple power converters used to supply the dc power bus. Others use either on-line or off-line uninterruptible power sources (UPSs) with battery or generator backup in the event of primary power loss. Still others, most notably telecommunication systems, use a distributed power architecture consisting of a combination of all of the above applied to both source and load circuits

The burden of these additional protective functions adds significant life-cycle costs which must be considered against performance requirements. For instance, using on-line UPSs for source-power redundancy involves in-rush start-up current of the power converters, while specification of off-line UPS requires knowledge of the correct relationship between output ride-through time and UPS transfer time to preserve power-bus integrity. Batteries create their own overhead burdens in the form of maintenance, charging requirements, and environmental considerations.

Available Options

Power supplies incorporating many of the features discussed above are available from several manufacturers, among them HC Power (HC1010 Series), Lambda/Qualidyne (MPS Series), Antec, Switching Power Inc., International Power Source, and Kepco Inc. (HSP and HSF Series). All represent products specifically designed for fault-tolerant power systems used in the international marketplace. They include such features as wide-range (universal) input with power factor correction, internally-mounted output isolation diodes, forced load-sharing circuitry, blind-mate connectors and fault detector circuitry with both visual and electrical indicators. The Kepco HSP Series logical fault detector with selective overvoltage shutdown provides accurate fault detection and fault isolation both with and without the optional isolation diode.

Paul O'Boyle is a senior design engineer at Kepco and specializes in new product development. He holds a BSEE from the Polytechnic Institute of Brooklyn, N.Y. His previous design experience includes military and industrial power converters. He is currently engineering group leader for switch-mode power-supply development.

Steve Kugler is supervisor of technical writing/webmaster at Kepco and has a BA in English from Lehman College. He spent 25+ years working in military, commercial, and marketing technical documentation.

HOW VALUABLE	CIRCLE
HIGHLY	541
MODERATELY	542
SLIGHTLY	543

DC UPS Provides Alternate Backup Solution

While The DC UPS' Embedded Approach Has Many Advantages, A Successful Implementation Takes Careful Planning Early In The Design Process.

BY ARON LEVY

Technology Dynamics Inc., 100 School St., Bergenfield, NJ 07621, (201) 385-0500; fax (201) 385-0702.

Utility blackouts and brownouts are facts of life, with industry pundits citing an average of 100 anomalies in utility power per month. With the amount of electronic systems going on line, utility power is only likely to get worse before it gets any better. Although the protection of sensitive equipment through the use of an ac stand-alone UPS may provide a quick-and-easy solution at first glance, these devices are plagued with cost, reliability, and efficiency issues. To add to the problem, many switch-mode power supplies (SMPSs) may be incompatible with an ac UPS unless the UPS' output is rated much higher than the load requirements, with the added cost that may entail. While power-factor correction could solve the problem, this feature is not standard in many SMPSs.

A substantially cheaper, more reliable and more efficient alternative to the ac UPS is the integrated dc UPS (DUPS) *(Fig. 1)*. Basically an SMPS with battery-backup features, a DUPS achieves the same goals as an ac UPS, but with a 15% to 20% increase in efficiency, at a cost of no more than 10% to 20% of a regular SMPS. To incorporate this solution however, requires preplanning and serious consideration at the system-design phase, while its power needs and sensitivity to power interruption must be clearly defined.

1. Basically a switch-mode power supply with battery-backup features, a DUPS achieves the same goals as an ac UPS, but with a 15% to 20% increase in efficiency, at a cost of no more than 10% to 20% that of a regular switch-mode power supply. To incorporate this solution however, requires preplanning and serious consideration at the system-design phase, while its power needs and sensitivity to power interruption must be clearly defined.

Backup Options

Despite the importance of power backup, especially in medical, telecommunications, process control, or financial institutions, in the vast majority of cases, the design and cost of employing a UPS is often left up to the end user. This situation deprives that end user of a choice, with the possibility that they may default to a standalone ac UPS, placed between the utility input and the system. Redesigning the system for an alternative backup solution is likely not an option.

At face value, this seems to be an easy and straightforward solution, and one which will result in the satisfaction of both the user and (undoubtedly) the maker of the UPS. On closer examination, though, the use of a standalone ac UPS can be an expensive, unreliable, and highly inefficient solution to the backup problem. The maintenance of this inefficient system is ongoing, and for the duration of the system's life cycle, may add up to a sizable amount. Aside from cost and effi-

ADAPTABLE

ciency, what is rarely highlighted is the fact that there is a severe incompatibility problem (not known to most users) between ac UPSs and switch-mode power supplies (SMPSs).

The Compatibility Problem

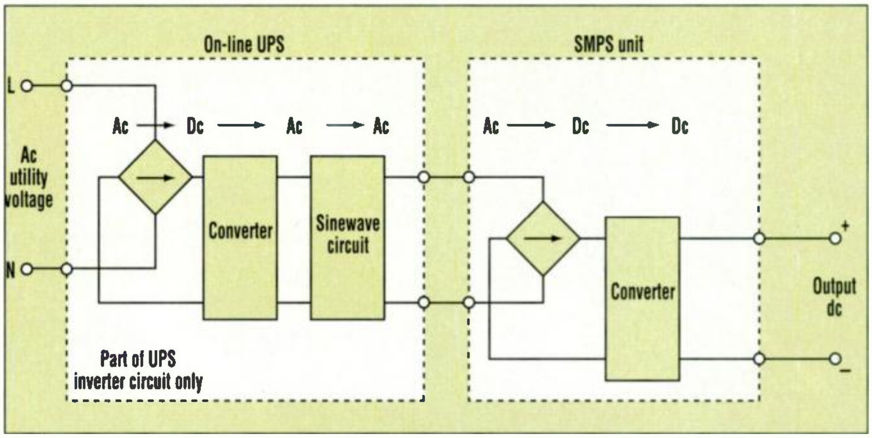
Most end users are oblivious to the severe problems encountered when an on-line UPS works with a non-linear load, such as an SMPS. The topology of an SMPS (also known as an off-line power supply) requires that the input ac voltage be rectified and then filtered by relatively large capacitors—approximately 1000 µF per 1000 W of output. This rectifier-filter creates a poor power factor of 0.6 to 0.65 and very high peak currents for the charging of this capacitor.

Repeated measurements under practical conditions show that in an SMPS the current peak-to-RMS ratio reaches a crest factor in the range of 2.5 to 3.5. These current peaks occur at approximately the peak of the voltage sinewave *(Fig. 2)*. Problems arise from these high-magnitude current pulses which can overload the UPS and distort its output, leading to inefficient UPS operation and severe degradation of its performance. As a result, many UPS manufacturers suggest that the user purchase an ac UPS rated at up to three times the expected load rating. This fix can be very expensive. While incorporating power-factor correction into the SMPS can alleviate the problem, many supplies available today, especially in the US, don't incorporate this feature, yet.

The Final Twist

The final twist to the ac standalone UPS strategy comes when the sequence of events, from the ac mains through the UPS to the output of the SMPS, is examined. Within the UPS, the utility voltage is rectified and filtered to produce a dc rail. This dc rail is chopped to high-frequency PWM pulses (class D configuration), and then integrated and filtered to produce a highly regulated, clean sinewave with a total harmonic distortion of less than 5%. Much effort and expense goes into producing this sinewave with such low distortion.

This voltage is then delivered to the SMPS (in the host system) as input. There it is rectified again and filtered to produce a dc rail just like the one in the UPS *(Fig. 3)*. Right away this process is seen to be wasteful, if not ridiculous. The irony of it, which seems to escape most people, is that the majority of users insist on, and pay extra money for, a pure sinewave voltage from the UPS—only to use it for an apparatus that rectifies it. This apparatus (the SMPS) in the host system would have been better off if the input voltage was dc rather than ac. Hence, the DUPS is called into action.



3. The irony of the wasteful, repetitious conversion typical of an ac standalone UPS, is that the majority of users insist on, and pay extra money for, a pure sinewave voltage from the UPS—only to use it for an apparatus that rectifies it. The host system would have been better off if the input voltage was dc rather than ac, bringing the DUPS into play.

DUPS Design Methods

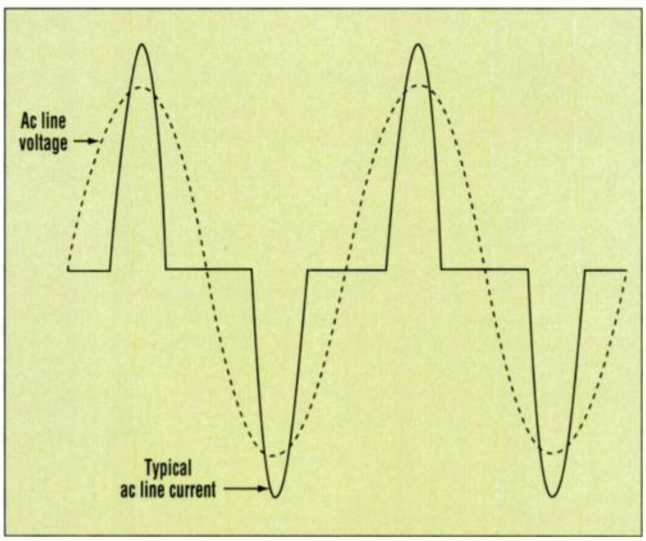
A DUPS is actually an SMPS with battery backup features. The backup is done either directly by a battery placed across the output of this SMPS, or by a high-frequency dc-dc converter embedded within the SMPS. In any case, this system avoids double conversion *(see "A UPS Primer," p. 146)* when on utility, and no sinewave needs to be generated. The overall efficiency continuously (while on utility) is 75% to 80%, as opposed to 56% to 60%, for a UPS/SMPS combination.

More importantly, overall price is 10% to 20% more than the price of a standard SMPS. As that is the case, backup can frequently be obtained at a fraction of the cost of an ac UPS.

DUPS battery backup may be accomplished in a variety of ways, some very direct and easy, and some more complex. Let's take a look at the easy ones first.

DUPS With LVBD

Often, an SMPS with a single output of 24 V (military or communications) or 48 V (telecommunications) needs to be backed up by a battery for a few minutes to a few hours. The output of the SMPS within this system is either 24 V or 48 V; this is the voltage which needs to be



2. In an SMPS, the current peak-to-RMS ratio reaches a crest factor in the range of 2.5 to 3.5. These current peaks occur at approximately the peak of the voltage sinewave. These high-magnitude current pulses can overload the standalone ac UPS and distort its output, leading to inefficient UPS operation and severe degradation of its performance.

supplied by the backup battery if the utility fails.

It makes sense in such a case to connect the battery to the output of the SMPS, so if the utility (or the SMPS) fails, the battery can take over *(Fig. 4)*. The problem however, is that in this arrangement, the battery may, in the case of a lengthy blackout, be totally drained unless something stops this from happening. This issue can be answered with the low-voltage battery disconnect (LVBD).

It makes sense to connect the battery to the output of the SMPS, so if the utility (or SMPS) fails, the battery can take over.

In this scheme, the LVBD circuit uses a FET transistor as a switch to permit discharge of the battery current into the load until the battery reaches a low threshold. The disconnect level is arbitrary, but in the range of 21 to 22 V for a 24-V battery, or 42 to 43 V for a 48-V battery. At this point, the logic cuts off the gate drive to the FET, and no further discharge is possible. Upon return of the utility voltage, the circuit is reset immediately and the output of the SMPS is restored from the utility.

The battery is now charging from the SMPS output directly, via the body diode of the FET. An "ac fail" signal, a rather standard feature in most SMPSs, is sent by the SMPS to the host system to notify it that the output is now derived from the battery. Knowing the discharge time, the host system is programmed to shut down when the proper time arrives—and do it without any crashes. This method is the simplest and least costly. It also is the most reliable and efficient. No battery energy is wasted for conversion, and charging is done simply from the SMPS output. These are the main advantages of the low-voltage, battery disconnect backup method. The main disadvantage is that this method is suitable only to

An Uninterruptible Power-Supply (UPS) Primer

On a daily basis, and in thousands of places around the world, personal computers and workstations crash due to utility failures, or merely a dip in their voltages. The crashes cause loss of data and system malfunctions, leading to a significant loss of time while trying to restore the lost information and reset the system. In developing countries the problem is greatly magnified due to poorly regulated and very unpredictable utility power. With the increasing use of these electronic systems predicted to cause even further problems for the utility services, power backup has risen to the forefront of electronic system design.

The most common backup system is widely known as the uninterruptible power supply (UPS). This standalone unit contains a battery, power inverter and control, and alarm circuitry. A traditional UPS takes in utility (or generator) power and provides an ac output voltage, similar to the utility in terms of voltage and frequency. The size of the internal battery, along with the UPS rating, the conversion efficiency, and the magnitude of the load, determine the backup time after the utility fails. Common backup times range between five to 15 minutes.

Generally, UPS equipment is rated in volt-amperes (VA), not watts, because the load may contain a reactive component. The bigger the battery (in terms of ampere-hour capacity), and the smaller the load, the longer the resultant backup time will be. Often, manufacturers specify backup time at both half and full load.

UPS Options

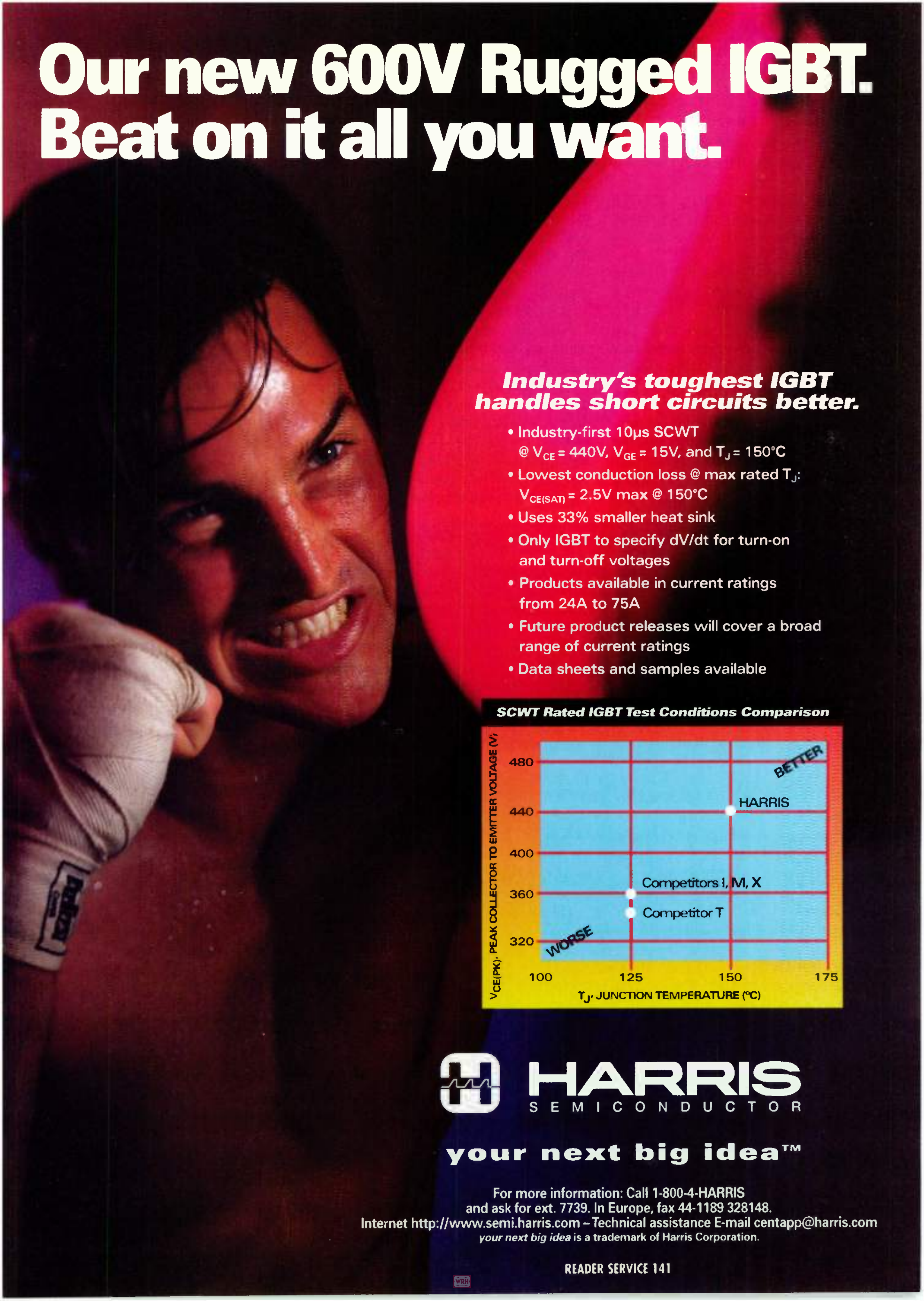
There are two major types of UPSs widely available in the consumer and industrial electronics markets. The first is called standby or line interactive, and the second is commonly called on line or double conversion.

The standby UPS delivers the utility voltage as is, or after some conditioning, to the output terminal, and from there to the load via relay contacts or a solid-state switch. Once it is sensed that the utility voltage has failed or dropped below some threshold, the relay transfers the load to an internal inverter. The inverter converts the voltage of the internal battery to an ac voltage of a similar magnitude and frequency to the utility supply.

The battery now starts a slow discharge and its voltage gradually drops. If the utility voltage reappears quickly, the load is transferred back to it by the relay. However, if the utility blackout lingers, the battery discharges continuously until a certain predetermined threshold is reached, at which time the control circuitry cuts off the UPS in order to avoid deep discharge of the battery. When this occurs, the load loses input power.

Prior to this occurrence however, the alarm circuitry within the UPS alerts the user using a visual alarm, usually a red, or blinking-red LED, and audio alarms. The audio beeps typically start at one every few seconds, and progress to rapid beeps as the UPS reaches cut off. Also, relay contacts deliver electric alarm signals to the user to enable the initiation of an orderly shutdown procedure. These alarm signals may be communicated to the host system via an RS-232 or RS-485 communication protocol, thus enabling automatic control over the host system's operation. Sophisticated UPSs provide a screen display, in an MS Windows environment, which appears on the host-system's monitor, that advises the user how much time re-

(continued on page 148)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host systems that are characterized by the following type of SMPS unit:

• The host system employs a single-output SMPS of 12, 24, or 48 V, or some other standard battery voltage (in multiples of 12 V).

• The host system must be able to work well in the low- to high-battery range, which is ±10% of nominal. Whatever the battery type used, this must hold. If the active circuitry in the host system needs tight regulation, this method is not a suitable option.

The battery itself should be relatively insensitive to the charging method, and be tolerant of a high charge after a discharge. For this reason, the use of maintenance-free, sealed, lead-acid batteries is recommended. These batteries are rugged, tolerant, and insensitive to charge. They also are cheap compared to all others. The battery is normally not contained in the SMPS, but within the host system. If very-long backup time is required, it can be packaged in a separate external cabinet.

A DUPS With Multioutput SMPS

A more complex situation arises when the SMPS provides several outputs *(Fig. 5)*. In this case, it is not possible to place a battery (with LVBD) across the output, because only one output will be backed up and the rest will not. Instead, the DUPS accepts ac input from the utility as well as dc input from the battery. When the ac power fails, a signal is delivered to activate a dc-dc converter embedded within the SMPS. This converter produces a voltage of 350-V dc to replenish the dc rail, thus keeping the SMPS, and all of its outputs, alive. The activation of the dc-dc converter is quick (1 to 3 ms), and it is well within the holdup time of the SMPS. The large capacitors on the dc rail store a significant amount of energy, with a high energy-to-volume ratio, due to the high voltage. Hence, no extra storage is needed to facilitate a seamless, transition between the utility and the battery. The outputs are never interrupted, and the dc rail never falls off.

A dc-dc converter rated at 1.5 kW back-up power, when designed to switch at high frequencies of 60 kHz to 100 kHz, measures only 5 in. by 5.25 in.

(continued from page 146)

mains on the battery. Some "smart software" is also available to program the orderly shutdown of the host system without human intervention – a useful feature if the system is unattended when power failure occurs.

The majority of standby UPSs in the market provide a quasi-square-wave ac voltage to the load. This allows a substantial cost reduction, since it is much easier to convert battery voltages (12, 24, or 48 V) to quazi-square-wave than to pure sinewave. This also contributes to making the unit smaller, lighter, and more efficient, and does not seem to bother most computers.

Despite these advantages, however, the standby UPS suffers from a major disadvantage: the transfer of the load from the utility to the internal inverter is made by relay, causing a disruption of 5 to 10 ms in current flow to the load. Fortunately, most personal computers (and some electronic systems) can tolerate such a disruption without a detrimental effect on performance. Therefore, inexpensive standby UPSs are used by millions by owners and users of PCs all over the world.

On-Line UPS

In this type of UPS, the internal inverter is actively working at all times, and its output feeds the host system. As a result, the inverter must work continuously (even when utility voltage exists.) In addition, on-line UPSs usually provide pure sinewave voltage on their output terminals, and that complicates its circuitry, adding to its volume and cost. Therefore, the price of an on-line UPS is three-to-five times that of a standby UPS with the same power rating. The internal inverter runs on the battery continuously, and the battery is charged from a high-power converter (charger) within the unit while running on utility voltage. Hence the frequently used name "double-conversion UPS."

A simpler method is to run the inverter on the rectified voltage of the utility. This technique makes the charger much smaller, since it only charges the battery (it does so slowly over 10-12 hours). When the utility drops, the battery takes over the dc rail, causing the operation of the inverter to continue without interruption. The two main features of the on-line UPS are its sine-wave output and its true uninterruptible operation. Almost all of the on-line UPSs in the market contain an output transformer, and provide galvanic isolation from the utility—a highly desirable feature for safety and noise reduction.

On-line UPSs range from 500 VA to several hundred kVA. Most with internal batteries are adequate for five to 15 minutes of backup time during power interruptions. Some high-power units are equipped with a separate cabinet for the battery, and provide hours of backup time. If very long backup is required (12 to 48 hours), to avoid a huge battery bank, a generator UPS may be a better choice.

Many on-line UPSs are equipped with a solid-state transfer switch (SSTS) which enables the transfer of the load to the utility if the UPS fails. This transfer also permits maintenance work on the UPS while the load is temporarily fed from the utility. A phase-locked-loop (PLL) circuit within the UPS ensures seamless transfer of the UPS by the SSTS, as it switches between the utility and inverter and vice versa. In terms of frequency and phase, the PLL circuit locks the UPS to the utility at all times.

The main advantage of the UPS is that it is a stand-alone unit. As such, it may be added arbitrarily only to systems or loads that cannot tolerate utility interruptions. Therefore, the decision to use it is left to the end user and then it becomes an optional add on.

The main disadvantage is that UPSs are relatively expensive (especially on-line machines), and their size, weight, and power consumption are significant. Even though these costs and physical impacts are passed along to the host system (i.e. the end user), this overall outlay, and the continuous maintenance thereafter, are to be considered as well.

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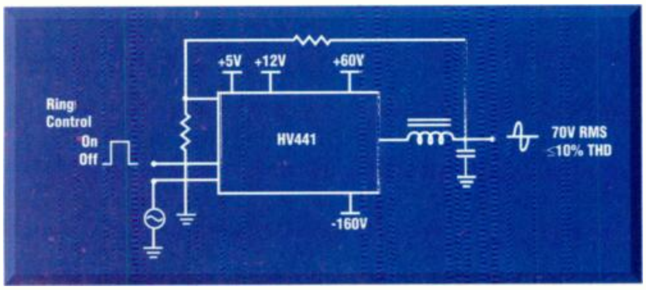

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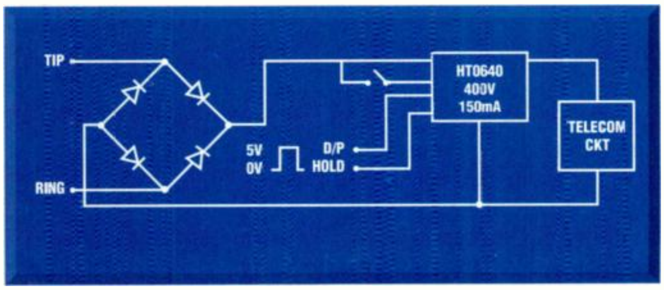

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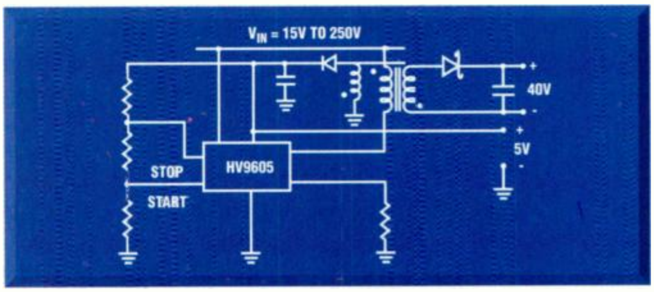

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HV441	Ring Generator IC	70V RMS self regulated, < 10% THD, 5 REN	Now
HV421	Ring Generator IC	120V P-P Output, 1 REN	Now
TN2524	N-Channel MOSFET	240V, for HV441 enhancement to 20 REN	Now
TP2522	P-Channel MOSFET	220V, for HV441 enhancement to 20 REN	Now
HV9110	SMPS PWM IC	10 to 120V input, 1MHz oscillator	Now
HV9605	SMPS PWM IC	15 to 250V input, optimized 1.4W output	Q1 '98
HV9221	Dual SMPS PWM IC	15 to 450V input, 1MHz oscillator	Q1 '98
HT0640	Line Switch IC	400V, 150mA, 15Ω, clamped output	Now
TP2640	P-Channel MOSFET	400V, 150mA, 15Ω	Now
HT0440	Isolated MOSFET Driver IC	400V Isolation, Dual Channel	Now

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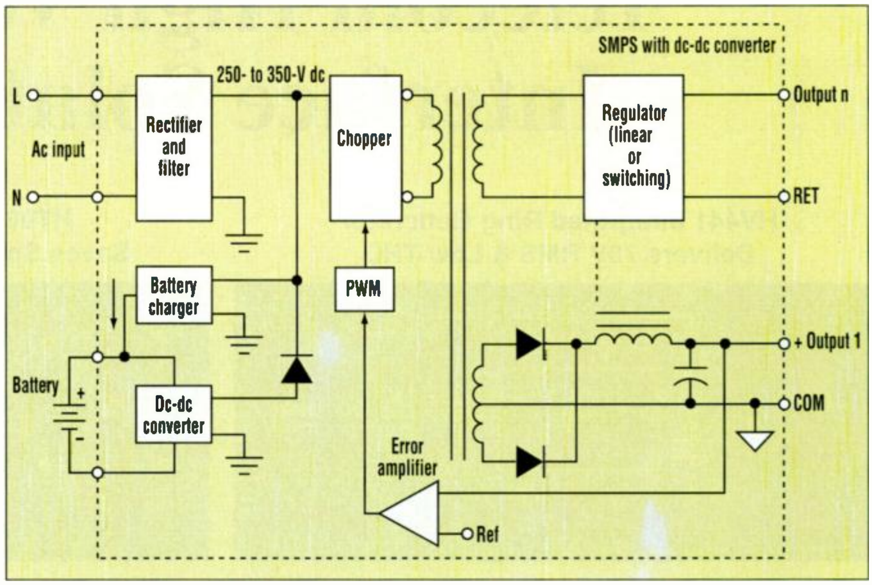


5. When the SMPS provides several outputs, the DUPS accepts ac input from the utility as well as dc input from the battery. When the ac power fails, a signal is delivered to activate a dc-dc converter embedded within the SMPS. This converter produces a voltage of 350-V dc to replenish the dc rail, thus keeping the SMPS, and all of its outputs, alive.

by 2 in. and weighs less than 2 lb. As mentioned previously, the converter remains inhibited while the utility voltage exists, but it is fired up when the utility fails. Therefore, under normal conditions, it does not dissipate any energy and the SMPS works strictly as a power supply. When the dc-dc converter operates, the unit as a whole works at 60% to 65% efficiency, as opposed to 50% to 55% typical of an ac-UPS combination.

While an ac UPS dissipates power all of the time, and is, therefore, costly to maintain over years of operation, the dc-dc converter or LVBD circuits don't dissipate any power in the standby mode. With a 1-kW load, this results in a saving of approximately $1000 in energy costs over a period of five years of continuous operation.

At this point, a comparison can be drawn between the DUPS and the ac standby UPS *(see "A UPS Primer," again)*, which also does not dissipate power in the standby mode. However, there are profound differences which exist between the two which give the DUPS two enormous advantages. First, the DUPS uses the energy stored in the dc rail. This feature allows it time to transfer without interruption. Second, the DUPS' high-frequency operation allows it to incorporate smaller and lighter components, while at the same time giving it quick-start capabilities.

As for the DUPS, regardless of whether an LVBD or a dc-dc converter is used, the battery must be charged from the SMPS. A simple battery-charging circuit can be designed for this function, either as an added output or as a small, high-frequency switching regulator. A rectified secondary voltage from the power transformer within the SMPS can produce a good charging voltage, if regulated by an inexpensive, three-terminal linear regulator. The cost of components is barely $1.50 for a 1-A charger working into a 24-V battery.

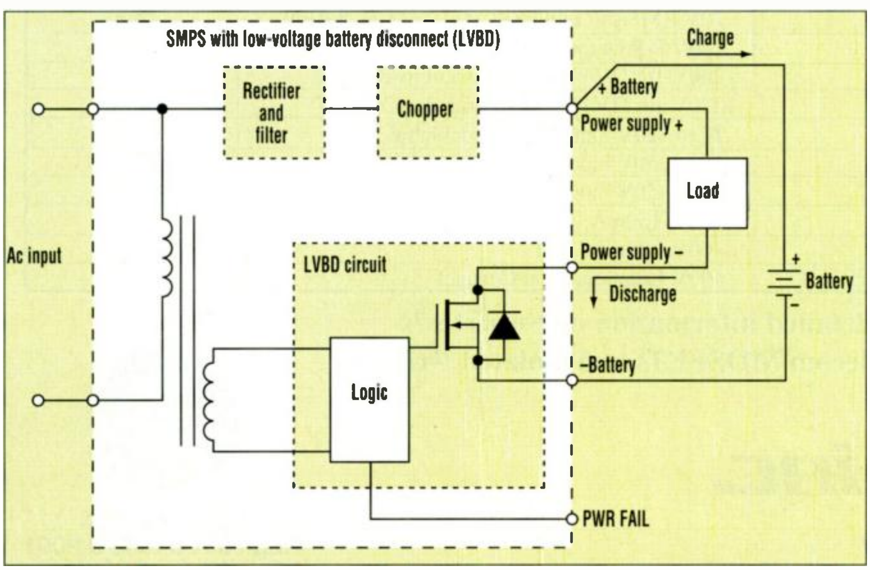
DUPS With An Integrated Topology

The DUPS design can be further simplified if the dc-dc-converter module is eliminated, and an integrated design topology used instead. While efficiency will not be improved in this approach, cost and volume will. Consider that the dc-dc converter circuit can share the same power transformer as the SMPS. Also consider a simple microprocessor circuit which controls all the functions of the SMPS. This controller senses the utility voltage and activates the power transistors of the converter stage. In this scheme there is only one power transformer, resulting in lighter weight, lower volume, and lower cost.

Design-Implementation Checklist

For a successful, problem-free implementation of a DUPS, with or without an embedded dc-dc converter, the following considerations must receive priority early in the design stage.

- If only one output is needed, it should be as close as possible to the nominal voltage of a standard battery (12, 24, or 48 V, etc.). This voltage will make it possible to connect a back-up



4. It makes sense to connect the battery to the output of the SMPS, so that if the utility (or the SMPS) fails, the battery can take over. The problem with this arrangement is that the battery may, in the case of a lengthy blackout, be drained. The low-voltage battery disconnect (LVBD) prevents the battery drain.

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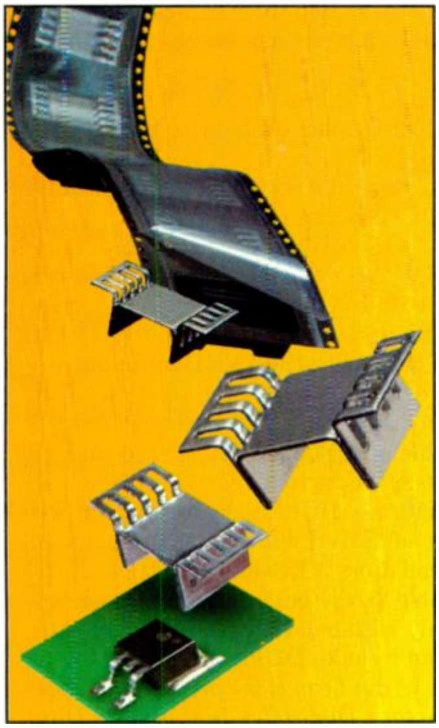

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battery at the output as long as LVBD is included in the SMPS.

• If the major output is suitable for DUPS with LBVD, but one more small output is needed, it is cheaper and easier to produce the second output using a small, encapsulated dc-dc converter driven from the main output of the DUPS.

• If multiple outputs are needed, consider the cost comparison between a number of dc-dc converters driven from a main output (as in distributed-power style), along with a central dc-dc converter embedded module to facilitate DUPS configuration.

• When designing an SMPS for a system, make it so that it can work directly from 115-/230-V ac or 350-V dc. Most SMPSs on the market will accept 350-V dc into their ac input terminals and will work just fine, because the ac is being rectified anyhow. Do not include in the design an ac fan or an auxiliary power supply (for housekeeping) which requires an ac input. Then, all that will be needed to implement a DUPS is a 250- to 350-V dc.

• If possible, leave room inside the SMPS for the possible inclusion of a dc-dc-converter module. Also, offer the end user the option to buy the SMPS with the LVBD or dc-dc-converter option from the very start, just in case he or she will need uninterruptible operation later. In case the end user elects to forego the option and later need it, be ready to sell a replacement SMPS with these options. Most end users will (with very little help) be able to replace the existing power supply with one that is identical in size, but includes DUPS options.

Aron Levy is the president of Technology Dynamics Inc., and its Divisions Nova Electric and Mid Eastern Industries. He holds a B.S. in Electrical Engineering from L.I. University and a master's degree in Business from Columbia University. He has published over 25 articles on power-conversion subjects in technical magazines and conferences the U.S. and abroad.

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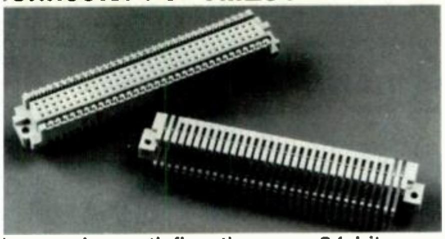

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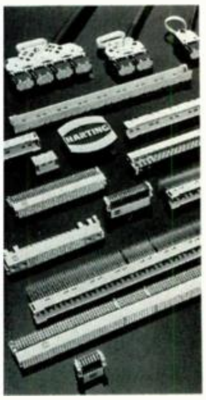

har-pak® 2.5MM High Density Connector System

Developed for backplane and daughter board applications in modern rack systems. The 5 row 2.5 mm connector design offers solderless PCB terminations, optimum utilization, of space three dimensional modularity, high contact density, EMI protection, and the ability to double-side surface mount components on daughter cards without loss of a 15mm card pitch. The *har-pak* connector system permits using a three dimensional 2.5mm grid. Only one connector style is required to solve your power, signal, ground, and high data rates, simplifying the design and manufacturing of future systems. The compliant pin technology utilizes the same 1mm plated through hole standard for many DIN 41612 compliant pin technologies. Consistency in design uses the many years of manufacturing and design experience already available. These attributes combined can lead to new advancements in board-level designs: 15mm card pitch with double-sided surface mounted daughter cards, butterfly or mid-plane techniques, modular design both horizontally and vertically, low number of system components combination with other standardized packaging systems, and lower applied costs.

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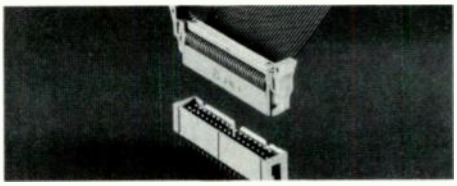
New SEK "Press'n Snap" Press in Header

Low profile press-in headers can be added to single or double-sided surface mount printed circuit boards any time after reflow. Press-in terminations of the two row .100" pitch headers permit easy installation into plated through holes without soldering. Removable temporary inserts allow any flat die to press the connectors. The straight header is shrouded by four plastic walls and available in versions from 6 to 64 contacts. The mating connectors are flat ribbon terminated socket connectors from HARTING's SEK range. These can be latched to the headers by using the locking levers installed onto the strain relief. The levers secure the socket connector to the end walls of the



header. Placing the locking levers on the socket instead of the PCB header saves valuable board real estate.

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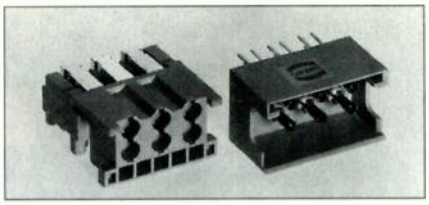

Designed for high speed data transfer rates. Can be used in the iec 1076-4-2 2.5mm High Density connector system, *har-pak®* Provides more space efficiency, high frequency capability, easy handling, low applied cost and application with current equipment and emerging metric equipment practices. Designed for PCB termination on both daughter card to backplane connection; allowing users to bring signal directly into the backplane without a cable transition.

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Modular Front Ends Tackle Harmonization Issues

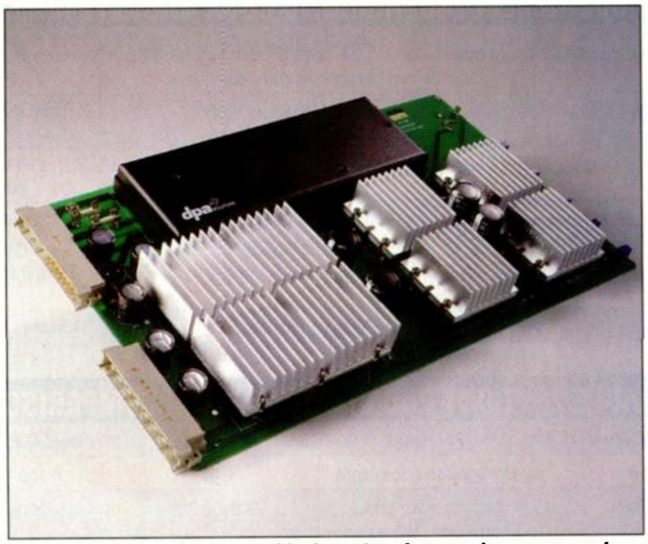
Thanks To A Tightly Regulated European Market, These Quality Front Ends Must Take Center Stage In Any Successful Modular Power-Supply Design.

BY DON MULVEY

dpa Solutions, Division of Custom Power Systems Inc., 33 Comac Loop, Ronkonkoma, NY 11779; (516) 4716300; fax (516) 471-0101.

With the global market's emphasis on the European Union (EU) and its electromagnetic compatibility (EMC) and safety directives, issues such as standardization, harmonization, surge suppression, and power-factor correction have come to the forefront of the design process. The emphasis on these features, combined with ever-increasing time-to-market pressure, has resulted in a spin-off component from power-supply manufacturers called the front-end module.

While front ends are not new, the emergence of front-end modules, with varying levels of isolation, EU compliance, voltage regulation, and ease of use has meant that conforming to EU regulations is not as difficult or as expensive as it might once have been. However, the wide array of modules to chose from means system design issues, such as safety, cooling, interfacing, maintenance, redundancy, and cost must be carefully examined before a final choice is made *(Fig. 1)*.



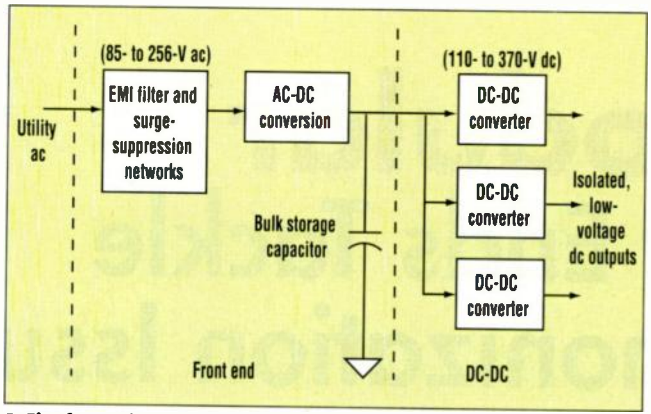
1. The emergence of a range of high-quality, front-end, power-supply modules means that conforming to European Union regulations for noise and safety might not be as difficult or as expensive as it might once have been. However, a number of system design issues, such as cooling, interfacing, maintenance, redundancy, and cost must be carefully examined before a final product is chosen.

Over the last several years there has been much fanfare regarding modular, high-density dc-dc converters (MHDCs). Several power-supply manufacturers have invested millions of dollars in developing new versions of modular dc-dc converters and marketed them as "component solutions" for power-system design. They claim that the system designer can employ these devices as routinely as they would design in a crystal oscillator or an IC. This notion is not too far from the truth, but only in strictly dc-dc applications where systems run off a regulated, low-voltage dc battery system. One example is a central-office environment where a -48-V dc battery system is used. However, when off-line conversion (ac input) is required for the application, the need to convert the "dirty" utility ac power into a clean, usable dc energy source for dc-dc converters arises.

Until recently, designing an ac-dc converter for powering dc-dc converters was fairly elementary. Simple rectification techniques and canned EMI filters satisfied most requirements. Now, with the EU and its EMC and safety directives, the situation has become more complicated. The nations of the EU have combined their individual requirements into a series of CENELEC specifications (*Table 1*). Each of these specifications are called European Norms (ENs) or Harmonizing Documents (HDs). Of these, the specification which has forced the greatest change in how power systems are designed is EN61000, which is driven by the EMC directive. Although this specification continues to evolve, and enforcement dates drift, system designers are adhering to it to ensure product acceptance in Europe.

Many of the standards under EN61000 mirror domestic standards, such as ANSI/IEEC62.41 for surge. However, there is no domestic version of EN61000-3-2 for harmonic emissions. This single specification has caused the most dramatic change in switching power-supply design since the introduction of the power MOSFET. The consolidation of all these EMC specifications has had the overall effect of helping move the power-supply market toward standardization. Today, the vast majority of off-line applications above 100 W require power-factor correction, EMI filtering to EN55022 Level B, and surge suppression to comply with the CENELEC requirements. These requirements make the goal of designing in modular dc-dc converters much more complicated for the system engineer.

Due to these complications, the use of MHDCs in off-line applications requires extensive design work unless a standard power converter, which possesses all of the necessary features, could be employed between the ac line and the dc-dc converters. Without a standard solution, the greatest benefits of modular dc-dc converters—low design-in cost and fast time to market—are undermined. This need for a standard solution has been answered with the emergence of a new power converter module called the front-end module.



2. This figure shows the major building blocks of an off-line switching power supply. The term "front end" fits well because it makes up the front part of the power supply, with respect to the direction of energy flow.

The Front End

Recent iterations have evolved from, and complement, the component power-supply market, particularly dc-dc converters. The term "front end" fits well since it makes up the front part of an off-line power supply, with respect to the direction of energy flow (*Fig. 2*). When powering dc-dc converters in off-line applications, the ac input voltage must be filtered and converted into a dc voltage first, before being isolated and converted into a low-voltage dc output by the dc-dc converters.

This first conversion stage (front end) can be implemented in one of three ways. The first, and simplest, technique is rectification and bulk

TABLE 1: EUROPEAN ELECTROMAGNETIC COMPATIBILITY (EMC) STANDARDS

Governing Standard	Description	Impact On Power-Supply Design
EN61000-3-2	Limits on harmonic current emissions	Requires power-factor correction
EN61000-4-2	Electrostatic discharge (ESD)	Requires additional suppression networks (RCs) on all control I/O
EN61000-4-4	Electrical fast-transient immunity	Requires very good insulation and surge-suppression devices (MOVs)
EN61000-4-5	Surge immunity	Requires very good insulation and surge-suppression devices (MOVs)
EN55022-1 (conducted)	Conducted emissions	Requires extensive input filtering, especially for class B
EN55022-1 (radiated)	Radiated emissions	Requires good mechanical layout and/or shielding

TABLE 2: FRONT-END CIRCUIT-DESIGN COMPARISON

Circuit Approach	Parts Count	Features	Efficiency	Best-Fit Applications	Approximate Cost
Rectification	Low	Unregulated dc output	> 97%	< 100-W systems	< $0.1/W
Nonisolated boost	Medium	Active power-factor correction, regulated output	90% to 96%	> 100-W systems	Approximately $0.25/W
Isolated boost	High	Active power-factor correction, isolated and regulated output, full overload protection, easy to parallel	75% to 85%	Battery-backed, non-isolated (buck) dc-dc converters	Approximately $0.50/W

Design Engineering Bulletin

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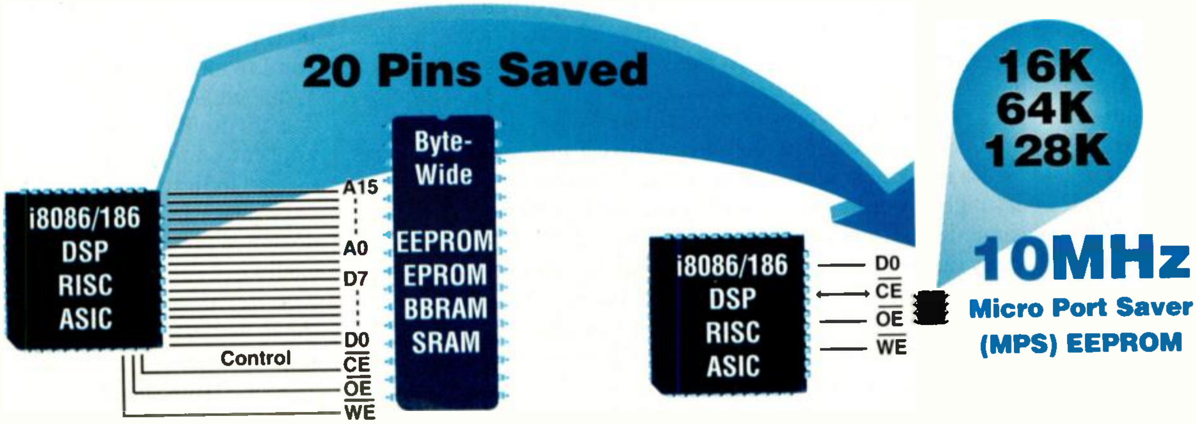
New Product and Applications Information for Design Engineers

10MHz MPS™ EEPROMs

Replace Parallel Memories



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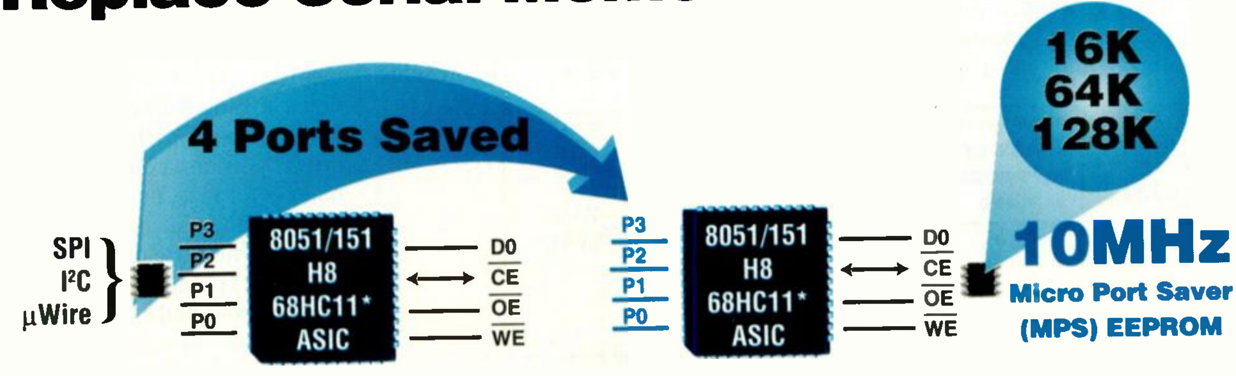


World's Fastest Serial Interface
50% Power Savings

* See AN103

storage of the energy in large electrolytic capacitors *(Fig. 3a)*. Unfortunately, the resulting ac-line current waveform is nonsinusoidal. Very narrow pulses, with very high peak currents and high harmonic content, are created, causing line noise. This implementation is clearly the simplest and most cost effective, but it does not meet the requirements of EN61000-3-2 for harmonic emissions.

The second approach to the ac-dc front end is a nonisolated, power-factor-corrected (PFC), boost converter *(Fig. 3b)*. This converter boosts the ac waveform to a voltage greater than the peak of the ac sine wave (usually 380 V dc) by integrating the peak currents of the boost over the entire sine wave. This technique results in a sinusoidal input current, a very high power factor, and low harmonic emissions. However, EMI filtering is tricky due to the very low input capacitance before the boost converter. The peak currents through the boost can easily conduct onto the line, thereby raising conducted emissions significantly. Care must be taken with this method when designing to meet the limits of EN55022 class B for conducted emissions.

The most recent, and most complex, approach for the front end is the isolated ac-dc front end—sometimes referred to as a switch-mode rectifier *(Fig. 3c)*. This implementation provides an isolated, and well-regulated low-voltage output of either 24- or 48-V dc. This output is accomplished by adding a dc-dc-converter stage to the output of the PFC boost. The approach uses both a rectification stage and an active boost stage, along with the dc-dc converter, in what turns out to be a high-performance, high-parts-count, and relatively high-cost front-end solution.

Trade-Offs

Each circuit approach has distinct advantages, trade-offs, and implementation costs *(Table 2)*. Ideally, the system designer would carefully consider which approach best suits the application early on in the design process. Additional considerations when employing modular high density dc-dc converters in off-line applications revolve around the architecture and the mechanical configuration of the system. Because MHDCs are board-mountable devices, they fit well in just about any electronic equipment. However, supplying power from the front end to the individual dc-dc converters may not be so easy. Many factors need to be considered, not the least of which include: the power-system architecture, safety, cooling, mechanical interfaces, maintenance issues, redundancy, design-in costs, and material costs.

Available Options

After analyzing a given application for all of the above parameters, the system engineer needs to know what products are available to suit the application. Standard solutions offered today essentially fall into two classes: board-mountable devices or modular, plug-in, rack-mount assemblies.

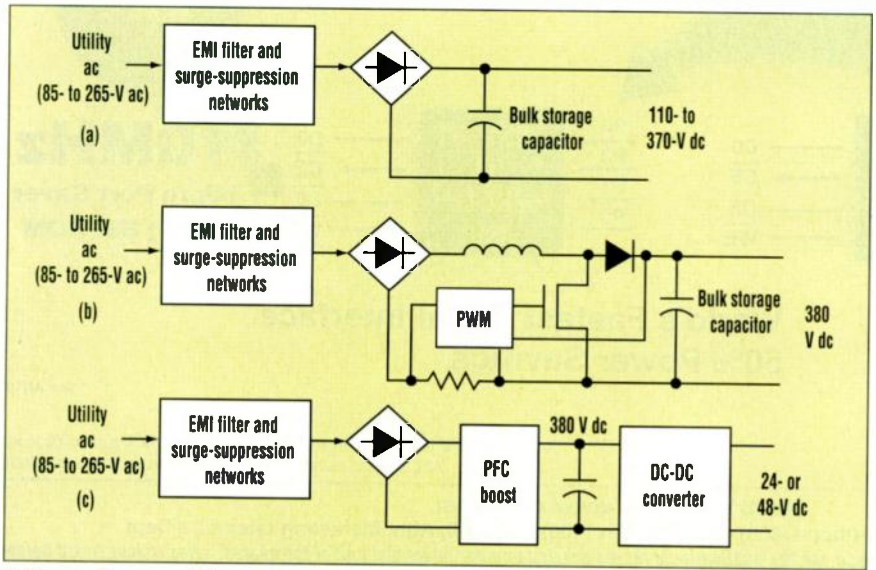
Board-mount devices—With standardization of the front end has come a broad range of board-mountable modules. Many MHDC manufacturers offer a module, physically similar to their dc-dc modules, which handles the PFC-boost function of the front end. However, the system designer is still required to choose an EMI filter, hold-up capacitor, and other peripheral circuits to employ the devices properly. When choosing a particular manufacturer's device, be careful to read the application notes that accompany the device in detail. Without the proper experience in filter and power layout design, a power-system engineer can easily get caught up in months of design iterations trying to get some of these devices to meet all of the EMC requirements.

Aside from the power-handling capability of the device, key parameters and options to examine include: whether or not power derating is required, the maximum operating baseplate temperature, available protection, control I/O, what levels of EMC compliance are included, and what peripheral components are required. A handy list to use when evaluating modules from various manufacturers is provided in Table 3. Don't be fooled by misleading specifications such as power density. When comparing different models for size, be sure to include all peripheral circuitry and heatsinks required. Unlike dc-dc converters, PFC modules typically occupy less than one half of a front-end's volume.

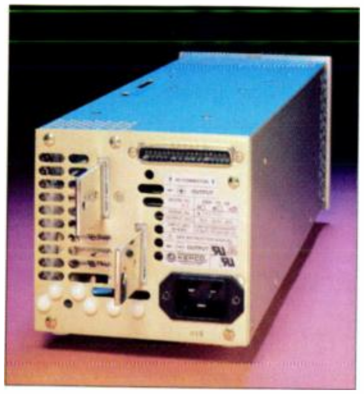
Some modular solutions are offered which satisfy the entire PFC front end, complete with EMI filtering and output hold-up capacitors. For example, the MFE series from dpa Solutions will power dc-dc converters and satisfy the EMC directive without any additional circuitr or heatsinks, other than a fuse *(Fig. 1, again)*.

Caution

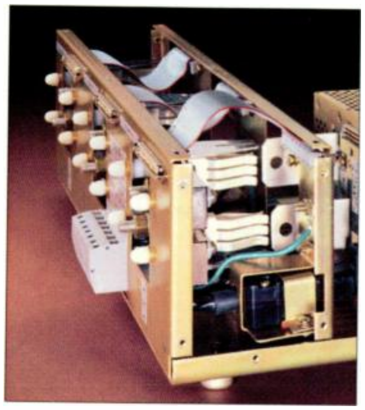
One word of caution in reference to the cooling requirements for these modular products. While power-supply manufacturers have done a fantastic packaging job, increasing power densi-



3. The simplest type of front end uses only rectification and filtering *(a)*. The second approach employs an active power-factor-corrected boost between the rectifiers and the storage capacitor *(b)*. The third type of front end implements a dc-dc switching regulator after the storage capacitor *(c)*.



Rear View of the HSP plug-in module



Rear view, cover removed, of the rack housing showing the heavy-duty bus-bar connections that make HSP's "Hot Swap" practical. Note: The a-c input connector is supplied with a mating connector, too.

Series HSM
Modular version for
hard wired applications

For applications that do not require hot-swap plug-in capabilities, see Kepco Series HSM power modules. They bolt to your chassis and provide a stable 1000W output.

HSP SIGNALS AND FLAGS

SPECIFICATIONS		RATING/DESCRIPTION	CONDITION
Status Flags (Form C dry relay contacts)	POWER	Indicates low source voltage signal asserted 5 msec prior to loss of output voltage	Both NO and NC available
	OUTPUT	Indicates normal operation	
	OVER TEMP	Over temperature shutdown	
	FAN FAIL	Failure of internal fan	
Status Indicators front panel LEDs Status indicators and status flags are isolated and operate independently although driven by the same detector circuit	POWER	Green	Lit when a-c is sufficient
	DC FAIL	Red	Lit when output failure is detected
	OVER TEMP	Yellow	Lit when thermostat activates
	FAN FAIL	Red	Lit when fan failure is detected

HSP CURRENT HARMONICS, SOURCE TRANSIENTS AND EMI SPECIFICATIONS

PARAMETER	DOCUMENT	SPECIFICATION
IMMUNITY(1)		
Radiated RF (Ampl. mod.)	EN 61000-4-3	10V/m, 80-1000MHz
Radiated RF (Pulse mod.)	EN 61000-4-3	10V/m, 900MHz
Magnetic Field	EN 61000-4-8	30A/M, 50Hz
Electrostatic Discharge	EN 61000-4-2	4KV (contact) 8KV (air)
Conducted RFI	EN 61000-4-6	10Vrms, 0.15-80MHz
Electrical Fast Transient	EN 61000-4-4	2KV, Tr/Th = 5/50ns
Surge (CM, DM)	EN 61000-4-5	4KV (CM) Tr/Th = 8/20μs 2KV (DM) Tr/Th = 8/20μs
EMISSIONS		
Conducted RF	FCC Class A CISPR 22, Class A	0.45-30MHz 0.15-30MHz
Current Harmonics	EN 60555-2 and EN 61000-3-2	0-2KHz

(1) All immunity levels meet the requirements for heavy industrial applications per EN 50082-2 using Criteria A (no operational effect).

HSP PHYSICAL CHARACTERISTICS

SPECIFICATIONS		RATING/DESCRIPTION	CONDITION
Dimensions	English	5.38" x 5.22" x 16"	Excluding front latch, circuit breaker, handle and rear connections
	Metric	137 x 133 x 406 mm	
Weight	English	19lbs	
	Metric	8.6Kg	
Source connection		3 pin IEC connector	Compatible with molded line cord
Load connection		Two bus bars 1.25" x 0.125" x 2.5"	Keyed for plug-in housing
Signal connection		37 Pin D-subminiature connector	

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❑ **I WANT** a free demo.

❑ **SEND ME** Kepco's Full Line Catalog on Instrumentation and Modular Power Supplies for System, Bench and the OEM, #146-1862

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Name ______________________ M/S ________ Title ________
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Phone ( ) ______________ Fax No. ( ) ______________

ACCESSORY HOUSINGS FOR HSP MODELS

RA 60

Tool-activated locking devices mount HSP modules

RA 60
19˝ Rack (3) HSP Modules
3 slots wired in parallel for redundancy
hot swap connectors

RA 62
19˝ Rack (3) HSP Modules
2 slots wired in parallel,
1 independent
hot swap connectors

RA 63
19˝ Rack (3) HSP Modules
independent slots
hot swap connectors

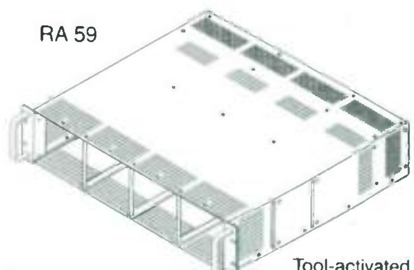
RA 58
19˝ Rack (3) HSP Modules
independent slots, hardwire

To configure the above rack housings for 23˝ or 24˝ wide rack cabinets, add suffix -23E or -24E respectively

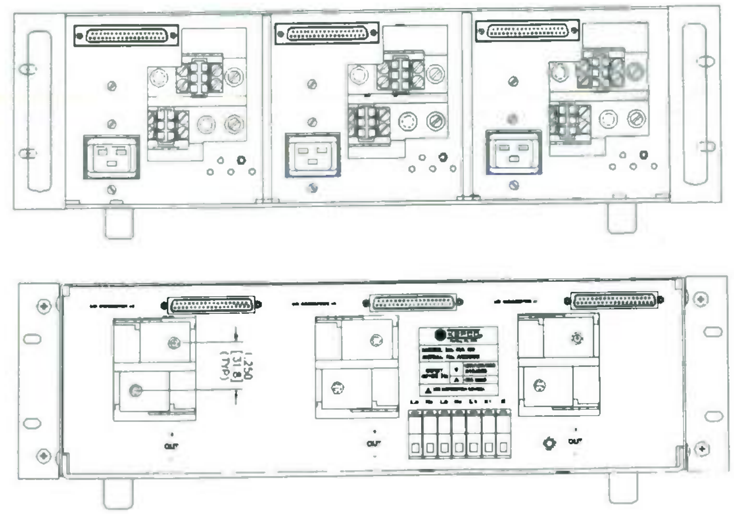
RA 59
24˝ Rack (4) HSP Modules
4 slots wired in parallel
hot swap connectors

RA 61
24˝ Rack (4) HSP Modules
independent slots, hardwire

RA 59



Tool-activated locking devices mount HSP modules

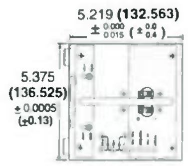


RA 60 front view (top), RA 60 rear view (bottom)

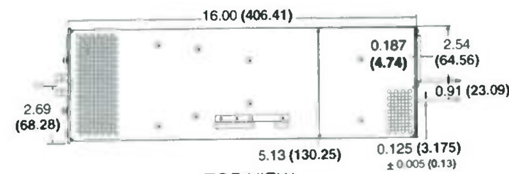
OUTLINE DIMENSIONAL DRAWINGS FOR HSP PLUG-IN MODULES

Fractional dimensions in light face type are in inches. **dimensions in bold face type are in millimeters.**

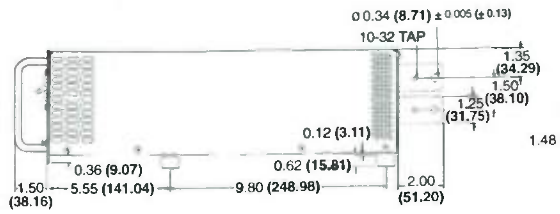
Tolerance: ± 1/64" **(0.4)** between mounting holes
± 1/32" **(0.8)** other dimensions



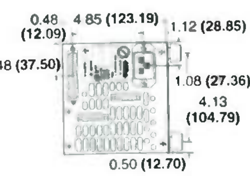
FRONT VIEW



TOP VIEW



SIDE VIEW



REAR VIEW

HSP ACCESSORIES

118-0776	line cord set with NEMA 5-20P termination (125V/20A)
142-0381	source power entry mating connector
142-0422	I/O mating connector
108-0203	I/O connector jackposts (set of two)
108-0296	I/O connector shell
101-0159	screw for mounting plastic feet

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FEATURES

- Remote sensing.
- Control/programming of voltage, current, current limit and OVP.
- Current walk in control.
- Safety agency approvals: UL 1950, CSA 22.2 no. 234, TÜV EN 60950.
- HSP meet ANSI C62.41/EN 61000-4-5 guidelines for withstanding surges on the mains.
- HSP are ~ 5" x 5" crossection plug-ins that mount three abreast in a standard 5.25" x 19" rack adapter. Output voltage settings and current limit can be pre-set so an HSP can be plugged in without powering down the system.
- HSP are fully protected for any overload including a short circuit. Normal overload protection is continuous current limiting. A switch selectable option will latch the power off after 20 seconds to avoid damage to load wires. An overvoltage protector latches the power off whenever the output exceeds a user-set limit.
- Remote control of HSP is provided via one of two isolated TTL-level signals, one normally high and the other normally low. An internal 5V supply powers this circuit and provides the auxilliary 5V, 100mA output. This voltage is available whenever source power is applied whether or not the main output is inhibited. The main output is normally ON if no remote logic is applied. The main output voltage is remotely trimmable by resistance. Both the output voltage and current limit are adjustable over the range 20%-100% by a 0-10V analog voltage.

HSP OUTPUT CHARACTERISTICS

SPECIFICATIONS		RATING/DESCRIPTION	CONDITION
Output setting range		-30% to +10%	Of nominal output
		-30% to +25%	48V Models only
Source effect	typ	0.05%	Nominal ± 15%
	max	0.1%	
Load effect	typ	0.05%	5%-100% load operation between 0-5% load results in increased ripple and degraded transient response
	max	0.1%	
Temperature effect	typ	0.01%	Per degree C (0 to 50°C)
	max	0.02%	
Combined effect (source, load temperature & time)	typ	0.15%	
	max	0.3%	
Time effect (drift)	typ	0.05%	0.5-8.5 hours
	max	0.1%	
Start up time	max	1 second	Any source/load
Recovery characteristics	Excursion	<3% of Nominal Output	50-100% load
	Recovery	1000W: 100 µsec 1500W: 300 µsec	Return to 1% of setting
Ride through	min	21.5 Milliseconds	From loss of source to flag signal
Hold-up time	min	5 Milliseconds	After signal flag
Overshoot	turn on	+3% max	Any source 5%-100% load
	turn off	none	
Error sense	3.3 & 5V	0.25V	Voltage allowance per wire
	All others	0.4V	
Series connection (output floats)		500V	Maximum voltage off ground
Parallel connection (for redundancy)		Current shares within 5% of rated load	5-100% load, hot-swappable
Selective overvoltage shutdown		Adjustable 100-140% of nominal; factory set to 130%	Latched, reset by cycling source power off
Current limiting		Constant current mode Factory set 110% of I_O max	Optional shutdown mode with 20 second delay
Remote on/off	RC-1	Normally high	Isolated form C or TTL
Remote on/off	RC-2	Normally low	Isolated form C or TTL
Over temperature		Thermostat, auto re-start	With hysteresis

HSP GENERAL SPECIFICATIONS

SPECIFICATIONS		RATING/DESCRIPTION	CONDITION
Temperature		-20° to +71°C (see model table)	Operating
		-40° to +85°C	Storage
Humidity		0 to 95% RH	Non condensing operating & storage
Shock		20g 11msec ±50% half sine	Non-operating 3-axes 3 shocks each axis
Vibration		5-10Hz 10 mm double amplitude	Non operating 1 hour each axis
		10-55Hz 2g	
Altitude	operating	Sea level to 10,000 ft	
	storage	Sea level to 160,000 ft	
Isolation	Output-case	500V d-c	25°C, 65%RH
Withstand voltage	Input-output	3000V a-c rms	25°C, 65%RH
	Input-case	1500V a-c rms	
Safety		UL 1950; VDE EN 60950; CSA 122.2 No. 234-M90 level 5	Information Technology Equipment
Type of construction		Enclosed, plug-in style includes status LEDs, circuit breaker, handle,voltage/current trimmers, monitor test points	Stand alone or rack mountable into RA 60 Accommodates up to 3 units
Cooling		Internal d-c fan	Exhaust to rear

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SERIES HSP

The Kepco HSP series comprises a group of ten models, seven 1000 watt power supplies with outputs from 3.3 volts to 48 volts and three 1500 watt power supplies with outputs from 24 volts to 48 volts. All models feature current-sharing for parallel redundant N+1 operation. Models with the or-ing diode, option R, are capable of hot swapping when plugged into Kepco's RA 60 series rack adapters. A mechanical keying scheme allows the user to define which power supply will plug into a specified slot in the housing. Output voltage and current limit settings are adjustable from the panel and may also be remotely adjusted.

The 1000 watt HSP have a wide range a-c input (90-277V a-c). The 1500 watt models operate from 180-277V a-c mains. Both feature an active power factor correction (PFC) front end to suppress harmonic generation per EN 60555-2 and EN 61000-3-2.

HSP have optional built-in "or-ing" diodes for redundancy paralleling and a "hot-swap" capability. These are specified by appending the suffix "R" to the model number.

Three HSP models shown in RA 60 Housing

HSP INPUT CHARACTERISTICS

SPECIFICATIONS		RATING/DESCRIPTION	CONDITION
a-c Voltage 1000W models	nominal	100-250V a-c	Single phase
	range	90-277V a-c	Wide range
a-c Voltage 1500W models	nominal	200-250V a-c	Single phase
	range	180-277V a-c	Wide range
d-c Voltage(1)	1000W	125-420V d-c(1)	Polarity insensitive
	1500W	250-420V d-c(1)	Polarity insensitive
Brownout Voltage	1000W	75V a-c	
	1500W	150V a-c	
Source Frequency		47-440Hz	>63Hz, input leakage current exceeds tabulated value
Source Current	120V a-c	1000W: 11.0A rms	Typical
	240V a-c	1000W: 5.5A rms 1500W: 8.0A rms	
Power Factor	Typical	0.99	Any source, 25% to 100% load
	Minimum	0.96	

(1) Safety approval is for a-c operation only.

CE HSP are CE marked per the Low Voltage Directive (LVD), EN60950

This KEPCO product is backed by a 5-YEAR WARRANTY firm

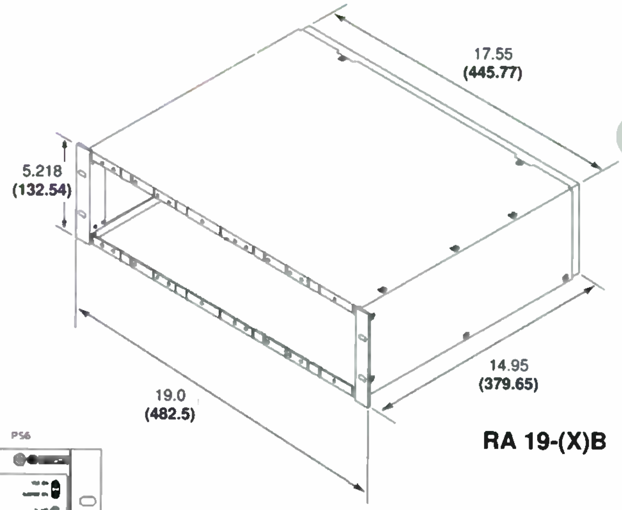
HSP MODEL TABLE

SPECIFICATION	OUTPUT VOLTAGE		OVP SETTING	RATED OUTPUT CURRENT			RIPPLE		NOISE	EFFICIENCY
Unit	Volts		Volts	Amps			mV p-p		mV p-p	Percent
Condition	Factory Set	Adjustment Range	Factory Setpoint	50°C	60°C	71°C	Source max	Switching max	(Spike) 20MHz	100% Load Nominal input
1000 WATT MODELS										
HSP 3.3-230	3.3	2.3-3.6	4.29	230	173	105	20	30	100	71
HSP 5-200	5	3.5-5.5	6.5	200	150	95	20	30	100	72
HSP 12-84	12	8.4-13.2	15.6	84	63	40	20	40	120	73
HSP 15-66	15	10.5-16.5	19.5	66	49.5	31.4	20	40	150	76
HSP 24-42	24	16.8-26.4	31.2	42	31.5	20	20	60	240	77
HSP 28-36	28	19.6-30.8	36.4	36	27	17	20	60	280	78
HSP 48-21	48	33.3-59.2	62.4	21	16	10	20	60	480	80
1500 WATT MODELS										
HSP 24-60	24	16.8-26.4	31.2	60	45	28.6	20	60	120	77
HSP 28-53	28	19.6-30.8	36.4	53	39.8	25.2	20	60	140	78
HSP 48-30	48	33.3-59.2	62.4	30	22.5	14.3	20	60	240	80

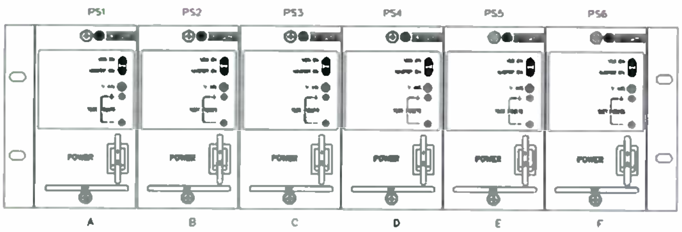
ACCESSORIES FOR HSF MODELS

OUTLINE DIMENSIONAL DRAWINGS

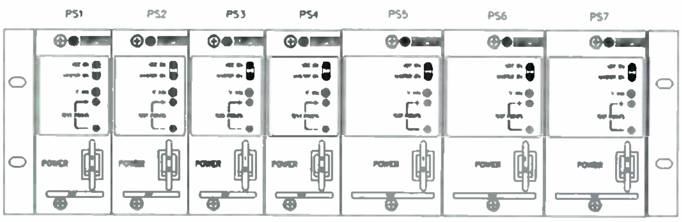
Fractional dimensions in light face type are in inches.
Dimensions in bold face type are in millimeters.



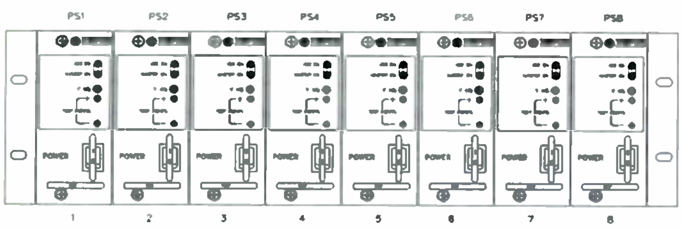
RA 19-(X)B



RA 19-6B Rack Adapter with (6) 150W HSF Installed



RA 19-7B Rack Adapter with (4) 100W and (3) 150W HSF Installed



RA 19-8B Rack Adapter with (8) 100W HSF Installed

RA 19-(X)B ACCESSORIES

Accessory	Part Number	Use
Filler Panel 1/24 Rack	RFP 19-24	Cover unused 1/24 rack slots
Filler Panel 1/12 Rack	RFP 19-12	Cover unused 1/12 rack slots
Filler Panel 1/8 Rack	RFP 19-18	Cover unused 1/8 rack slots
Filler Panel 1/6 Rack	RFP 19-16	Cover unused 1/6 rack slots
Filler Panel 2/8 Rack	RFP 19-28	Cover unused 2/8 rack slots
Filler Panel 2/6 Rack	RFP 19-26	Cover unused 2/6 rack slots
Filler Panel 3/8 Rack	RFP 19-38	Cover unused 3/8 rack slots
Filler Panel 1/2 Rack	RFP 19-48	Cover unused 1/2 rack slots

Weights	English	Metric
RA 19-(X)B	22 lbs	10Kg
50W	4 lbs	1.8Kg
100W	5 lbs	2.3Kg
150W	5.5 lbs	2.5Kg

RA 19-8B Rack Adapter Rear Panel

This is the standard rear panel configuration. Other connector options are available. Please consult the factory.

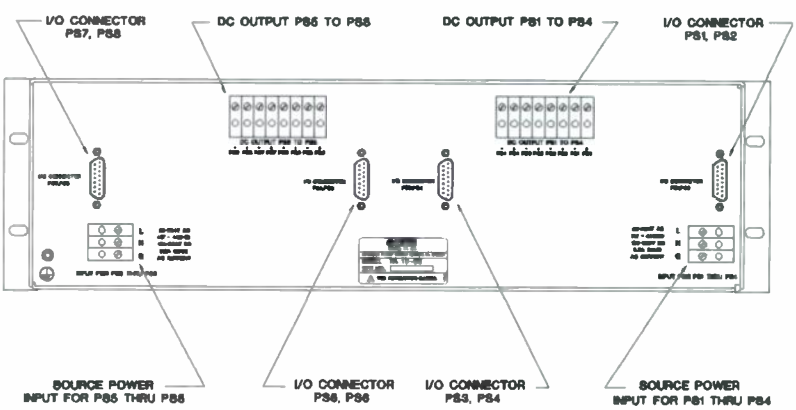
The I/O Connector functions are brought out as follows:

1- Error sense (+S, -S) for each position.

2- Output voltage (+V, -V) for each position to permit wiring for local sense.

3- Current share bus (one) connection brought out for each pair of modules. (Each pair internally connected using DIP switches on the backplane).

4- Output status alarm contacts (Form C) for each position.



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FEATURES

- **Built-in EMI filter:** Attenuates the conducted noise below the requirements of both FCC and VDE 0871 for Class B computing devices.
- **Remote error sensing:** All HSF provide separate remote error sense terminals: 0.25V drop/wire.
- **Forced current share:** Used to configure an N+1 system. When the current share bus of paralleled HSF are connected together, the load current divides equally. If one unit fails, the remaining units will divide the load equally among themselves and continue to supply uninterrupted current to a critical load. The failed unit is isolated by built-in or-ing diodes.
- **Alarm:** A built-in relay provides either normally open (close on failure) or normally closed (open on failure) contacts that may be used to provide an external failure indication.
- **Plug-in connector:** The HSF obtain mains power and provide output via a 24 pin connector that mates with a corresponding connector in the rack adapter.
- **Keying:** The HSF are keyed according to their voltage rating. When the corresponding rack adapter key (pin) is installed by a user, only an HSF of the correct voltage can be inserted into the keyed slot.
- **Safety:** Designed to meet UL 1950, CSA C22.2 No. 234 (M90) level 3 and EN 60950 (a-c input

FAW 100W Model

For applications that do not require hot-swap plug-in capabilities, see Kepco FAW-series power modules. They bolt to your chassis and provide a stable 15, 25, 50, 100 or 150W output.

HSF INPUT CHARACTERISTICS

SPECIFICATION		RATING	CONDITION
a-c Voltage	nom	120-240V a-c	Single phase
	range	95-264V a-c	
d-c Voltage	range	125-370V d-c(1)	Polarity insensitive
Brown-out voltage	min	85V a-c/110V d-c	Ripple, source and load effect increase
Frequency	nom	50-60Hz	Single phase
	range	47-440Hz(2)	
EMI		FCC and VDE 0871	Conducted Class B
Soft-start circuit		Thermistor or thyristor limiter	
Leakage current	max	0.5mA UL method	120V a-c 50-60Hz
	max	0.75mA VDE method	240V a-c 50-60Hz
Startup time	max	50W<500ms 100 &150W<200ms	From turn on until d-c output reaches nominal
Holdup time	typ	20msec	120V a-c
	min	15msec	100V a-c

INPUT CURRENT (Amperes)		50W	100W	150W	
a-c Current	typ	1.0	2.0	3.0	120V a-crms
	max	1.2	2.4	3.5	
	typ	0.5	1.0	1.5	240V a-c rms
	max	0.7	1.6	2.0	
Fuse value		3.0	5.0	6.3	250V type 5x20mm
Initial turn-on surge, first half cycle		45	45	45	120V a-c rms
		90	90	90	240V a-c rms
Efficiency	typ %	76	76	76	Max load, nominal output
Circuit type		Forward Converter			
Switching frequency	typ	120KHz			Nominal load

(1) Note: Safety agency approvals are valid only for a-c input because of the fuse rating
(2) At 440Hz the leakage current exceeds the UL safety specification

HSF OUTPUT CHARACTERISTICS

SPECIFICATION		RATING	CONDITION
Source Effect	typ	1.0%	95-132 or 190-264V a-c
	max	2.0%	
Load Effect	typ	1.0%	10% to 100% load
	max	2.0%	
Temperature Effect	typ	1.0%	Nominal input, rated load 0-40°C
	max	2.0%	
Combined Effect	typ	2.0%	Includes source, load and temperature
	max	4.0%	
Time Effect (drift)	typ	0.1%	0.5-8.5 hr, max load, 25°C
	max	0.5%	
Recovery Characteristic	excursion	<±4%	Step load 50-100%, rise time >50μs
	recovery	2ms	To within 1%

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146-1869

YOU NEED KEPCO'S PLUG-IN HOT SWAPS WHEN...

...YOUR EQUIPMENT BAY IS SHORT ON SPACE.

Give us 3U x 19″ and get:
(3) 1000W plug-in power supplies or (6) 150W plug-ins or (8) 100W plug-ins or (8) 50W plug-ins or mix the 50, 100 and 150W modules in the rack.

...YOU HAVE TO STAY ON-LINE, NO MATTER WHAT.

Kepco's plug-in, fault tolerant, hot swap power supplies current share and have built-in or-ing diodes for real N+1 redundancy.

...YOU NEED TO MIX 'N MATCH.

Kepco's hot swap power supplies range from 3.3~48V;
50, 100, 150 and 1000 watts per module; up to 3000W per 3U rack.

Series HSF 50-150W plug-in modules for multi output or N+1 redundancy

Series HSP 1000W plug-in modules for multi output or N+1 redundancy

LOOK INSIDE FOR PROBLEM SOLVING DETAILS

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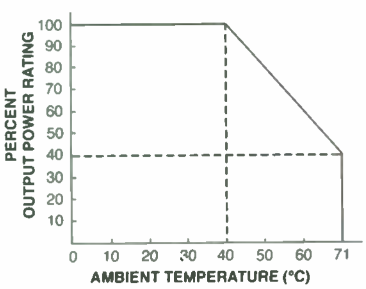
SERIES HSF

The Kepco HSF series of hot-swappable plug-in power supplies are designed to be combined in an N+1 fault-tolerant power system. Built-in forced current sharing and or-ing diodes are provided for this purpose. HSF may also be used independently as a multi-output power supply.

HSF are designed as plug-ins to a Kepco series RA 19-(X)B rack. The RA 19-6B will accommodate six 150W plug-in modules. The RA 19-8B will accommodate eight 50W or 100W plug-in modules. The RA 19-7B will accommodate three 150W and four 50W or 100W plug-in modules. It will also accommodate four 150W and three 50W or 100W plug-in modules.

The front panel of each plug-in HSF module contains an on-off switch and a "V d-c on" light. When HSF modules are paralleled, the module with the highest voltage setting automatically becomes the "master" (indicated by the front panel "master on" light). The other units are slaves, track the voltage setting of the master and equally share the load current. The front panel voltage adjustment trimmer provides adjustment of the output voltage. A pair of test points provide access at the front panel to measure the voltage.

FIGURE 1: OUTPUT POWER RATING VS. AMBIENT TEMPERATURE



HSF MODEL TABLE

MODEL	OUTPUT VOLTS	ADJUSTMENT RANGE	OVP SETTING (VOLTS)	OUTPUT CURRENT AMPS 0-50°C	CURRENT LIMIT (AMPS)	SW RIPPLE mV typ	SW RIPPLE mV max	NOISE (spike) mV max
50 WATT MODELS								
HSF 5-10	5	4.5-5.5	7.0~8.0	0-10.0	10.5~12.0	30	60	<120
HSF 12-4.2	12	11.4-12.6	13.7~15.7	0-4.2	4.4~5.1	35	70	<190
HSF 15-3.4	15	13.5-16.5	17.0~19.0	0-3.4	3.6~4.1	45	90	<220
HSF 24-2.1	24	22.5-25.5	27.0~30.5	0-2.1	2.2~2.6	50	100	<310
HSF 48-1	48	45.0-51.0	53.5~60.0	0-1	1.1~1.3	60	150	<350
100 WATT MODELS								
HSF 5-20	5	4.5-5.5	7.0~8.0	0-20	21.0~24.0	30	65	<120
HSF 12-8.3	12	11.4-12.6	13.7~15.7	0-8.3	8.7~10.0	35	70	<190
HSF 15-6.6	15	13.5-16.5	17.0~19.0	0-6.6	7.0~8.0	40	80	<220
HSF 24-4.2	24	22.5-25.5	27.0~30.5	0-4.2	4.4~5.2	50	110	<310
HSF 28-3.5	28	26.5-29.5	32.0~35.0	0-3.5	3.7~4.2	60	140	<330
HSF 48-2	48	45.0-51.0	53.5~60.0	0-2	2.1~2.4	80	220	<530
150 WATT MODELS								
HSF 5-30	5	4.5-5.5	7.0~8.0	0-30	32.0~36.0	30	60	<120
HSF 12-12	12	11.4-12.6	13.7~15.7	0-12	13.0~15.0	35	70	<190
HSF 15-10	15	13.5-16.5	17.0~19.0	0-10	11.0~13.0	40	80	<220
HSF 24-6	24	22.5-25.5	27.0~30.5	0-6	6.3~7.5	50	110	<310
HSF 28-5	28	26.5-29.5	32.0~35.0	0-5	5.3~6.1	60	140	<330
HSF 48-2.8	48	45.0-51.0	53.5~60.0	0-2.8	3.0~3.5	80	220	<530

(1) Current limit is a rectangular type, not foldback.

HSF GENERAL SPECIFICATIONS

SPECIFICATION		RATING/DESCRIPTION	CONDITION
Temperature		0° to 71°C (see figure 1)	Operating
		-40°C to +85°C	Storage
Humidity		Up to 95% RH	Non-condensing Operating & storage
Shock		20g, 3 axes (11msec ±5msec pulse duration)	Non-operating 3 shocks each axis
Vibration		5-10Hz: 10mm amplitude 3 axes	Non-operating 1 hour each axis
		10-55Hz: 2g, 3 axes	
Isolation	Output-Case	500V d-c, 100M Ohm	25°C, 65% RH
Type of construction		Plug-in	
Cooling		Convection	
Withstand voltage 50W	Input-Output	3.75KV a-c for 1 minute	25°C, 65% RH Y caps removed
	Input-Case	2KV a-c for 1 minute	
Withstand voltage 100W,150W	Input-Output	3KV a-c for 1 minute	25°C, 65% RH Y caps removed
	Input-Case	2KV a-c for 1 minute	
Safety		UL 1950; EN 60950; CSA 22.2 No. 950-95	

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ties as high as 100 W/in.[3], conversion efficiencies have not risen sufficiently to compensate for the decrease in available surface area. The result is a very small module, with a very small surface area, and very high heat dissipation. For 0.5-in.-high modules operating at 90% efficiency, 100 W/in.^{3} means 5 W/in.^{2} of power dissipation. For air-cooled applications, this becomes a genuine exercise in thermodynamics. Since most of the board space gets occupied by bulky EMI components and storage capacitors, the smallest module may not be the best solution.

Rack-mount assemblies—Several manufacturers also have responded to the front-end need with isolated 24- and 48-V hot-pluggable products. These are often referred to as distributed front ends. Although they serve well as bulk power supplies in systems employing distributed dc-dc converters, they are not distributed front ends themselves. Instead, they supply power to a dc distribution bus. In order for a power converter to be a distributed component, it must have the ability to be placed in the system at the point of load. The so-called distributed front ends are typically large in size and power-handling capability (500 to 1000 W), and are rack mountable, making it impossible to situate them in a distributed fashion.

The greatest benefit these types of converters offer is their isolated outputs. The low-voltage outputs offer a lot of freedom to the system designer when bussing power to the dc-dc converters. Instead of having to deal with dangerous ac voltages, a low-voltage dc is distributed to the dc-dc converters. The only negative trade-off in bussing the dc is that the conductors must carry currents two to six times greater than when ac is distributed. When battery back-up is required, these type of converters are ideal. Again, a handy list for product evaluation purposes is provided *(Table 4)*.

The MHDC's greatest attribute is its modularity. Now complemented by standard front-end converters, MHDCs can be employed much more efficiently, with minimal design-in time and cost. There is no single best approach or product for every system and in every instance there are numerous considerations that must be made. The front-end module is a relatively new breed of power converter just starting to evolve, and as such, will take on many forms to successfully satisfy the power needs of MHDC-based power systems. It will very likely be the catalyst for wide spread implementation of MHDC's in the future.

Donald Mulvey is the vice president of sales and marketing at dpa Solutions. He holds a BSEE from the State University of New York, Stony Brook, and has been in the power supply industry for 10 years.

TABLE 4: CHECKLIST OF KEY PARAMETERS FOR EVALUATING RACK-MOUNTED FRONT-ENDS

Parameter	Value or Yes/No
Power range (W)	
Maximum 19-in. rack configuration	
Current sharing	
Built-in fan	
Short-circuit and overload protection	
Control I/O	
Electromagnetic Compliance	
Harmonics emissions	
Electrostatic discharge	
Surge	
Conducted emissions	
Radiated emissions	
Mechanical	
Module size (L by W by H)	
Weight (per module)	
Is standard rack available?	
Maximum height of rack	
Maximum depth of rack with cabinet	

TABLE 3: CHECKLIST OF KEY PARAMETERS FOR EVALUATING BOARD-LEVEL FRONT-END MODULES

Parameter	Value or Yes/No
Power range (W)	
Power derating at 85-V ac	
Maximum operating baseplate temperature (°C)	
Short-circuit protection	
Control I/O	
Electromagnetic Compliance	
Harmonics emissions	
Electrostatic discharge	
Electrical fast transient	
Surge	
Conducted emissions	
Radiated emissions	
Peripheral Components Required (In Addition To Power Module)	
Electromagnetic-interference filtering	
Fusing	
Heatsinks	
Hold-up capacitors	
In-rush-limiting device	
Rectifiers	

HOW VALUABLE	CIRCLE
HIGHLY	570
MODERATELY	571
SLIGHTLY	572

READER SERVICE 108

Understanding The Transient Response Of A Switch-Mode Supply

Fast-Changing Load Currents And Extended Cabling Can Conspire To Jeopardize An Otherwise Sound Design.

BY LAZAR ROZENBLAT

Todd Products Corp., 50 Enjay Blvd., Brentwood, NY 11717; (516) 231-3366; fax (516) 952-3048; e-mail: lrozenblat@toddpower.com

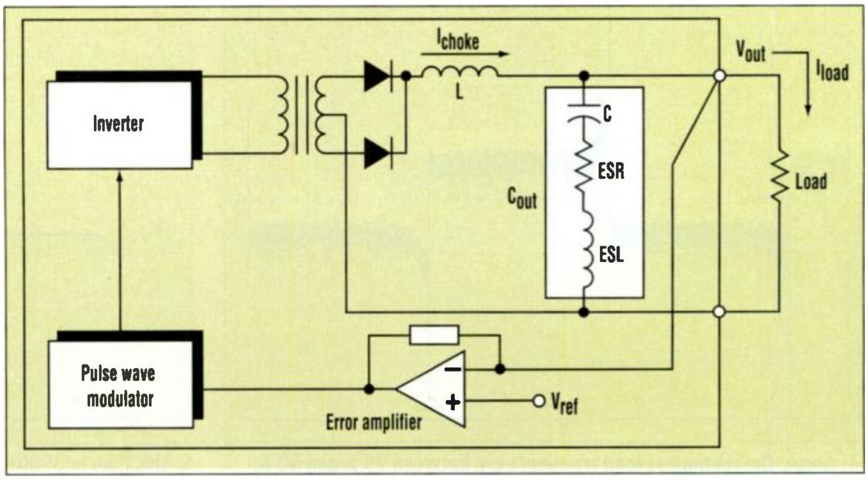
Understanding the mechanism of response to transients of switch-mode power supplies is essential for the proper selection and use of these supplies. Transient analysis is often based on the so-called "small-signal model" that assumes transient deviations in the closed feedback loop are so small that all loop components remain within their linear region. Unfortunately, in many applications, a load change may be large and rapid enough to drive the error amplifier into saturation such that small-signal analysis becomes invalid.

Further complicating the issue is the fact that the error amplifier often takes its input from the terminals of the supply. As a result, voltage drops along the load cables due to large, fast-changing load currents may not be accurately compensated for. While computer simulation or differential equations may be used here to predict circuit behavior, large-signal models are rarely available for the power-supply user. However, some rough estimates of voltage deviations can help users in this situation find a suitable compensating capacitor.

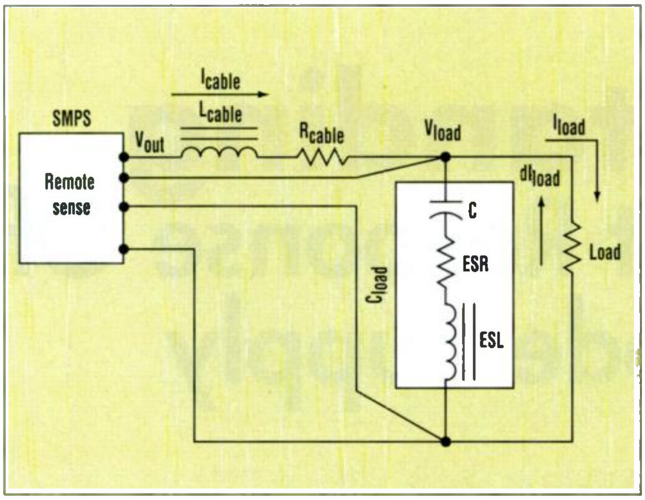
In a simplified circuit of a switch-mode power supply (SMPS), an error amplifier (EA) compares output voltage V_{out} with a reference V_{ref} and controls the duty cycle, D, via a pulse-width modulator (PWM) *(Fig. 1)*. The output capacitor C_{out} is represented by its equivalent circuit that includes the equivalent series resistance (ESR) and the equivalent series inductance (ESL). When we have a load step ΔI (we will assume ΔI is positive, that is the load increases), current through choke L cannot be instantly changed. No matter how quick the control circuit is, there is a finite time t needed for L to accommodate ΔI:

$$t > \frac{L\Delta I}{(V_{in}D_{max}) - V_{out} - V_{diode}}$$

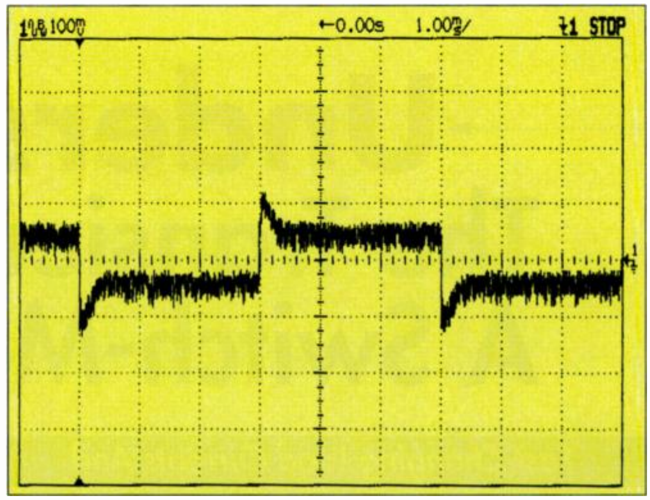
where D_{max} = the maximum duty cycle



1. This simplified diagram of an SMPS shows that the switching load current in the first moment flows through the output capacitor, represented by an equivalent series resistance (ESR) and an equivalent series inductance (ESL). The ESR and ESL cause the output-voltage deviation.



2. Load cables introduce their own inductance and resistance. Therefore the peak transient deviation and response times specified in the product data books are normally only valid when measured right at the power-supply's terminals, unless otherwise specified.



3. Output-voltage deviation with continuous load transients between 25 A and 50 A (50-µs transition time) measured at the output connector. Slightly different levels of steady-state voltage at different I_{load} allow current sharing and redundant operation.

and V_{diode} = the diode's voltage drop.

Until I_{choke} slews to the new load current, the switching component of I_{load} flows through C_{out}. This results in an output-voltage deviation ΔV_{out} that may be as much as:

$$\Delta V_{out(max)} \leq \frac{ESL(dI_{load})}{dt} + ESR(\Delta I)$$

where dI_{load}/dt is the load-current's slew rate (amps per second). While the SMPS's output capacitors act as a reservoir for these transient currents, the number of capacitors used is normally a trade-off for the manufacturer between cost, size, and transient response.

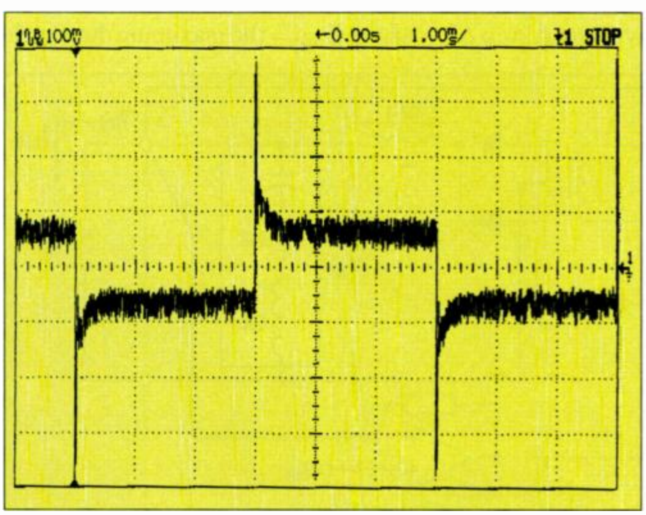
Cable Effects

The delay in the supply's inductor is only half the problem. When load cables are introduced, all the ground rules change. An SMPS product catalogs often specify two values: peak transient deviation and response time. But because load cables always have a certain self-inductance, L_{cable}, and a resistance, R_{cable}, these data are normally valid only when measured right at the power-supply terminals, unless otherwise noted *(Fig. 2)*. When I_{load} changes, Faraday's law tells us L_{cable} will cause an initial voltage deviation ΔV of:

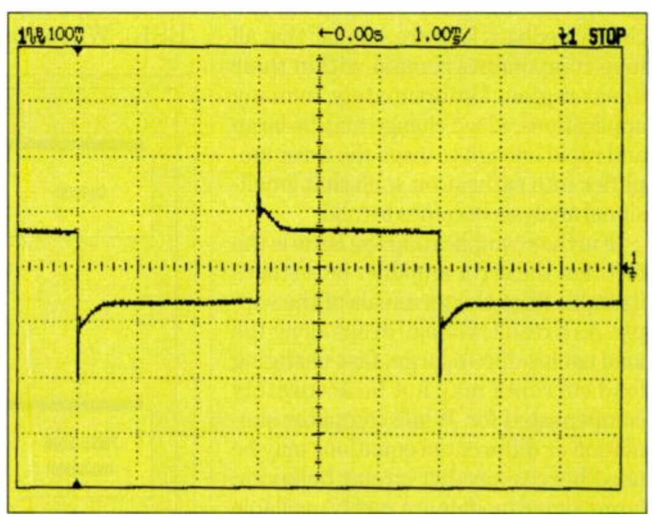
$$\Delta V = \frac{-L_{cable}(dI_{load})}{dt}$$

In addition, R_{cable} will cause an output voltage drop as I_{load} slews.

As an example, the typical inductance of AWG#10 stranded hook-up wire is 0.15 µH/foot. For a 1-ft. pair, we will have an inductive glitch of 150 mV for the load step of 0.5 A/µs, a glitch of 300 mV for 1 A/µs, and a whopping inductive glitch of 3 V for 10 A/µs. This initial deviation does not depend on the power supply, as it is purely a function



4. Again, the continuous load transients are between 25 A and 50 A, but the load is connected via a pair of 1-ft. cables (AWG#10) with a 0.1-µF terminating capacitor. The larger peak transient deviation is due to the inductance of the load cables.



5. This time, a 3900-µF terminating load capacitor serves as a reservoir for the 25- to 50-A transient current. The capacitor's low ESL and high capacitance reduce peak transient deviation as well as ripple to give a smoother ouput waveform.

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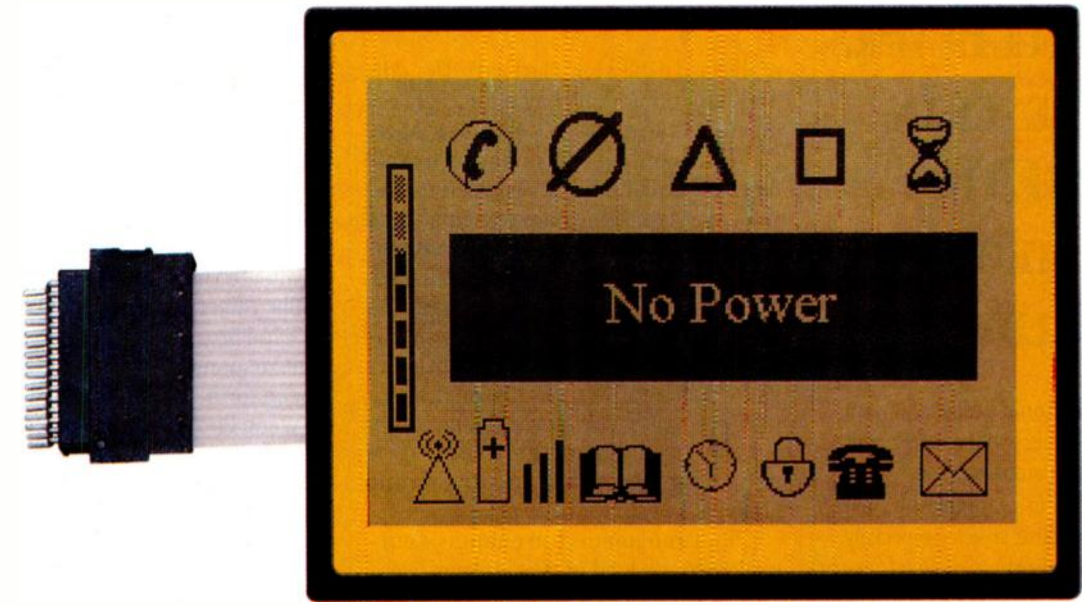

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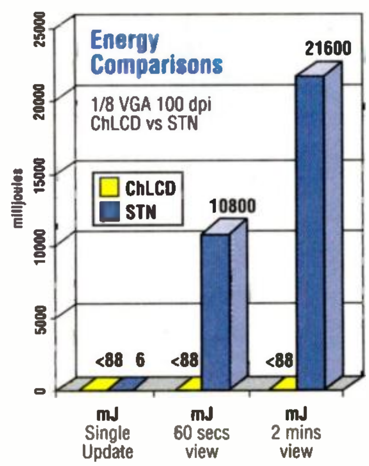

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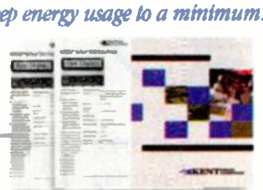

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READER SERVICE 169

of the load cables and the load's dI_{load}/dt. The only thing that may effectively reduce ΔV is an external load capacitance.

While computer simulation or differential equations may be used to find the exact transient response (and thus find a suitable compensating capacitor), the problem is that we need accurate large-signal models of an SMPS power stage, PWM, and error amplifier. Since this "inside" information is rarely available to a power-supply user, we will try to provide some rough estimates that could help the SMPS user that is attempting transient analysis.

The time needed to change a current through load cables is given as:

$$t_1 \cong t_{delay} + t_{rise} \qquad \text{eq.1}$$

where t_{delay} = the SMPS delay time and t_{Rise} = the time needed for I_{cable} to catch up to the load current. This rise time is given as:

$$t_{rise} = t_{delay}\left(\frac{\dfrac{dI_{load}}{dt}}{\left(\dfrac{V_{max} - V_{load}}{L_{cable}}\right) - \dfrac{dI_{load}}{dt}}\right)$$

where V_{max} is the maximum output voltage during the transient recovery of the supply.

During this time, the load current will slew up to $t_1 dI_{load}/dt$, and it can be shown that this may cause the output voltage to dip by as much as:

$$\Delta V_{out(max)} < ESR\left(\frac{t_1 dI_{load}}{dt}\right) \qquad \text{eq.2}$$
$$+ t_1^{\,2}\left(\frac{dI_{load}/dt}{C_{load}}\right)$$

A Typical Scenario

For example, an SMPS has a nominal V_{out} of 5 V and V_{max} = 5.5 V. The load changes from 25 A to 50 A (ΔI =25 A) over a 50-µs time span (dI_{load}/dt=0.5 A/µs); t_{delay} is 20 µs and the inductance of the load cable is 0.3 µH (which is the inductance of a pair of stranded wires AWG#10 measuring 1 ft. each). Suppose the load cables are terminated with a capacitor rated at 3900 µF, 10 V (LXF series, United Chemi-Con), and with an ESR of less than 24 mΩ.

As shown in equation 3, the time needed for I_{cable} to catch up with I_{load} would be t_1 = 29 µs. Judging from equation 4, $\Delta V_{out(max)}$ is less than 0.45 V. If this deviation is not acceptable, another capacitor has to be connected parallel to the load.

The effects of load cables and external capacitors on the example of transient response of a Todd TMX-350 prototype for a continuous load transient between 25 A and 50 A, with a transition time of 50 µs (0.5 A/µs), are shown *(Figs. 3, 4, and 5)*. The output-voltage deviation when the load is connected directly to the output connector is shown *(Fig. 3, again)*. The slightly different levels of steady-state voltages at different load currents (droop) allow automatic current sharing of two or more power supplies and provide glitch free "hot swaps." These output-level changes are typically around 2%.

The response (with remote sense) when the same load connected via a pair of AWG #10-size stranded wires measuring 1 ft. each, with a 0.1-µF ceramic capacitor and no external electrolytic capacitors, also is shown *(Fig. 4, again)*. The response of the same circuit, with a 3900-µF, 10-V United Chemi-Con, LXF series terminating load capacitor is much improved *(Fig. 5, again)*.

Lazar Rozenblat is a senior engineer (Design Group) at Todd Products. He received his Engineer Degree from the Leningrad Institute for Electronic Communication before becoming a member of the research staff at the Institute for Electronic Instrumentation in Kishenev, Russia.

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HOW VALUABLE	CIRCLE
HIGHLY	532
MODERATELY	533
SLIGHTLY	534

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READER SERVICE 247

Reducing Noise And EMI In Distributed Power Systems

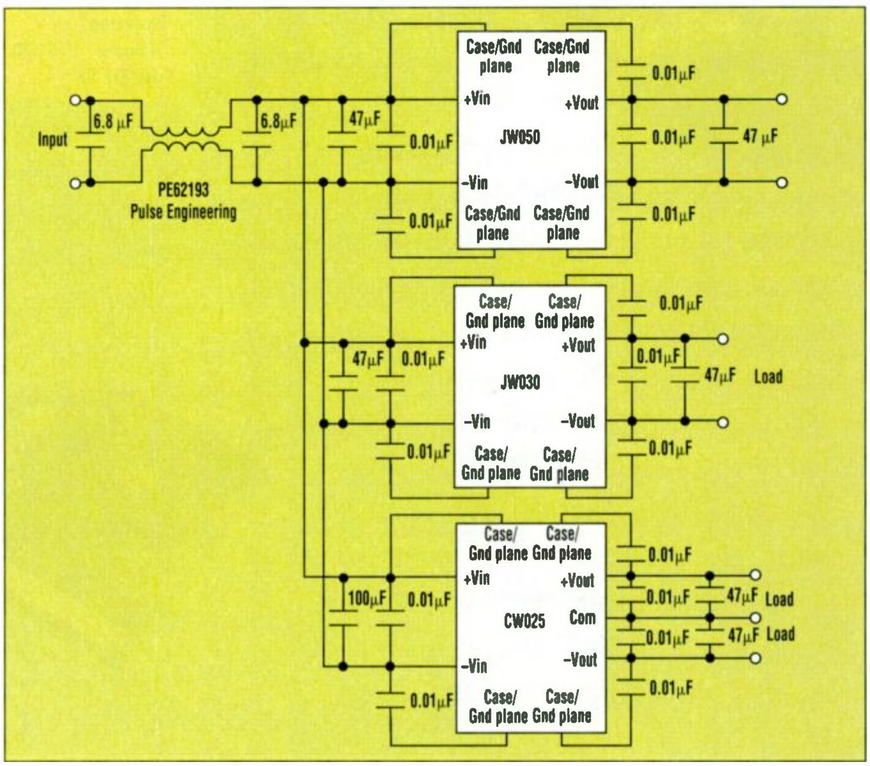
The Fast-Switching Currents And Voltages Demand The Use Of External Filtering And Careful Layout Techniques To Achieve Class B Compliance.

BY GABRIEL G. SURANYI

Lucent Technologies, Microelectronics Group, 3000 Skyline Dr., Mesquite, TX 75149; (972) 284-2000; fax (972) 284-2900.

The close proximity of the converters and loads in a distributed power system elevates the importance of noise and electromagnetic interference (EMI) containment in this environment. In a typical distributed power system, a front-end supply produces an intermediate dc voltage (i.e., 48 V) that is bussed to one or more dc-dc converters located close to their respective loads (typically one per circuit board). These converters, in turn, convert the intermediate bus voltage to a reduced, highly regulated level (i.e, 5 V) that is supplied directly to the load.

By their nature, on-board switching converters exhibit fast voltage- and current-switching transients that generate both conducted and radiated emissions. Fast switching on logic loads, such as CPUs, also produces conducted noise that reflects back to the input of the on-board converter. This conducted noise, in turn, generates electric and magnetic fields that radiate noise into other circuitry. Systems designers must control the noise emanating from the on-board converter so that it does not interfere



1. One of the advantages of using a distributed power architecture is that it increases flexibility by enabling designers to address noise and EMI concerns locally at each converter. The three basic rules for containing the noise generated by the power module are: return the noise currents to the source using as short a route (loop) as possible; reduce the impedance of these loops by reducing inductance and increasing capacitance; and identify alternate routes and suppress them by adding impedance.

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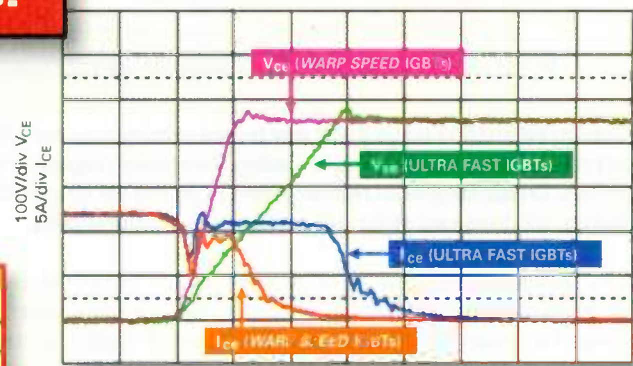

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18-26 A	IRG4BC40W	600	TO-220	91654
18-26 A	IRG4PC40W	600	TO-247	91656
26-36 A	IRG4PC50W	600	TO-247	91657

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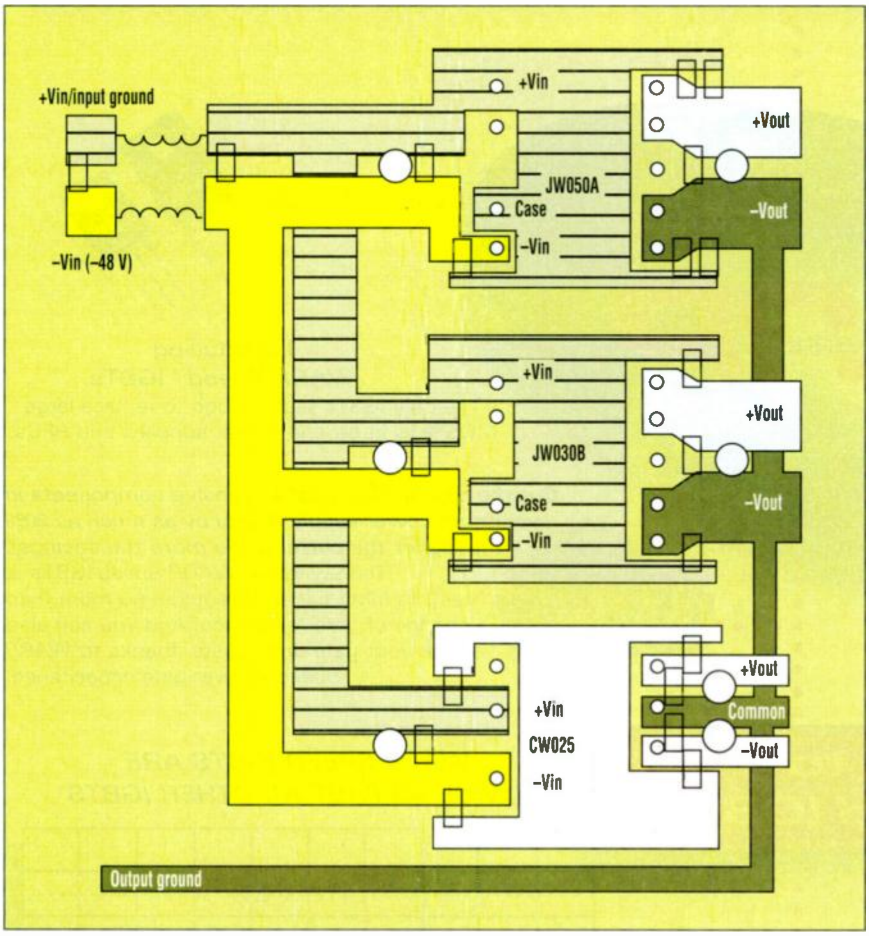

2. Good layout practices can go a long way toward reducing noise and EMI. Traces from different layers are annotated by a difference in shading. Rectangular components indicate ceramic capacitors. Circular components represent low-ESR (equivalent series resistance) electrolytic capacitors, which are used on the converter inputs to improve stability.

with other system circuitry, or propagate into the ac main supply.

Board-mounted dc-dc converters are typically designed to pass both the CISPR and FCC Class A radiated emissions requirements for industrial, commercial, and business environments. These requirements are sufficient to ensure that noise and EMI from the converter doesn't affect other components. However, to meet the more stringent Class B requirements for residential and general public use, containment external to the converter may be needed.

Conducted emissions containment is seldom provided within the latest high-power modules. One reason is that it gives the designer greater flexibility in meeting the emissions requirements of various applications. Second, it reduces costs and reduces real estate requirements by enabling designers to provide a single filter network for multiple converters located on the same board. Most manufacturers are fully aware of their module's external filtering needs, and are quite willing to assist users in meeting noise-containment requirements. Many also offer packaged filter modules optimized for their converters.

Layout Considerations

Good board layout is essential for minimizing the amount of noise an on-board converter conducts or radiates. Ideally, the board should provide wide power paths routed closely together in parallel. In addition, all copper loop areas on the board, which can act as antennas, should be kept to a minimum. For example, remote sense leads are generally connected from the converter output to a local regulation point some distance from the converter. At the same time, output leads typically take a parallel path to the same remote point, creating a loop. To minimize this loop, the remote sense leads should be routed very close to the power paths.

To help shield other circuitry from noise radiating from the fast switching power train, board designers should avoid running signal lines under the converter. Ideally, ground planes would be placed under the converter to isolate the converter from the signal lines. Generally, all signal paths should be separated from power paths.

External Filters

There are two types of conducted noise–common mode and differential mode. Common-mode noise, which is coupled through the capacitance between components such as heat sinks and transformer isolation windings, appears between frame ground and the converter's input conductors. Differential noise appears across the input conductors.

The three basic rules for containing the noise generated by the power module are: return the noise currents to the source using as short a route (loop) as possible; reduce the impedance of these loops by reducing inductance and increasing capacitance; and identify alternate routes and suppress them by adding impedance.

Common-mode noise exhibiting high-frequency content can be steered back to the on-board converter by ceramic capacitors (typically 0.01 to 0.1 µF) placed between input and output conductors and the case ground. Lower-frequency differential-mode noise can be mitigated using ceramic capacitors (usually 0.1 to 1.0 µF) placed close to the converter between the input leads. A similar capacitor should be placed between the output leads. All of these bypass capacitors should be placed as close to the converter as possible to minimize loop area.

If the design still doesn't meet conducted noise requirements, designers may need to add an EMI input filter. Many converter vendors offer such filters, which are optimized for their converters. However, if you have to design it yourself, a good rule of thumb is to provide 24 dB of filtering at the converter's switching frequency with a damping factor of 0.707. Typically, a common-mode inductor of less than 1 mH is sufficient to meet class B limits.

POWER TECHNOLOGY FOCUS:

A bulk capacitor at the input can be used to maintain converter stability.

One of the advantages of using a distributed power architecture is that it increases flexibility by enabling designers to address noise and EMI concerns locally at each converter. The high intermediate voltages bused to each local converter also help with noise and EMI containment. For example, these high voltages increase the options for using series inductors to implement the converter's EMI input filter. The higher the input voltage, the less likelihood there is of voltage drops across the inductor pulling the converter out of regulation.

Sample EMI/Noise Solution

A sample circuit contains three dc-dc converters: a 50-W module with a single 5-V output; a 30-W module with a single 12-V output; and a 25-W module with dual ±15-V outputs *(Fig. 1)*. The board layout for that circuit demonstrates how good layout practices and a single discrete filter circuit can be used to meet the stringent CISPR Class B requirements as mentioned earlier *(Fig. 2)*.

Traces from different layers are annotated by a difference in shading. Rectangular components indicate ceramic capacitors. Circular components represent low-ESR (equivalent series resistance) electrolytic capacitors, which are used on the converter inputs to improve stability. The input EMI inductor is a common-mode inductor.

Typically, radiated noise can be contained by following good layout practices. However, in some cases, designers also may need to add filtering. The general procedure to follow is to first bring conducted emissions down to acceptable levels, and then tackle radiated emissions.

Gabriel Suranyi is a power systems engineer and a member of the technical staff at Lucent Technologies. He is responsible for power architecture development and customer support. He holds a BSEE from New York University and an MBA from Stevens Institute, Hoboken, N.J.

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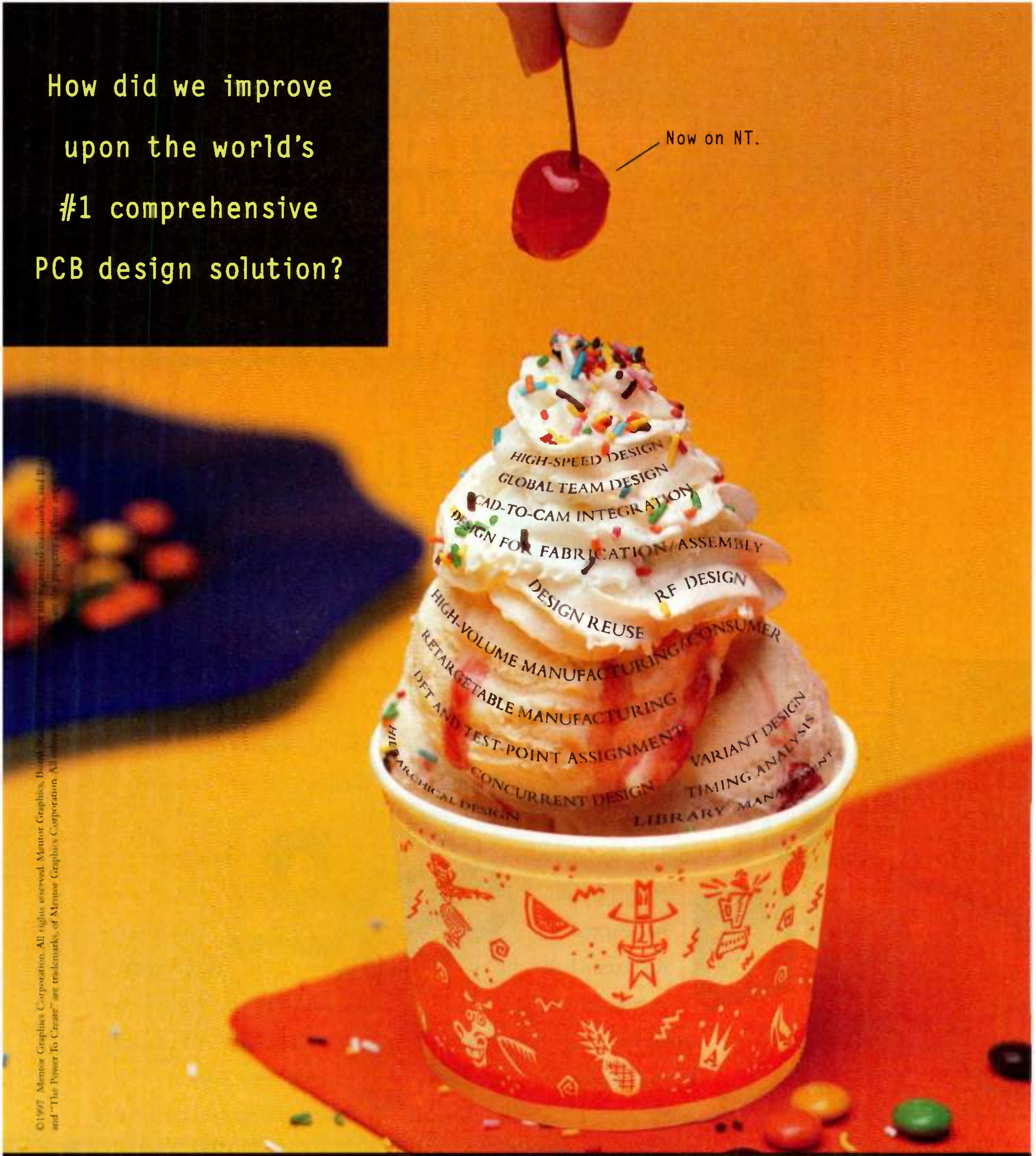

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READER SERVICE 202

ISR Transforms Into A Versatile Power Source

By Taking Advantage Of Its Adjust Feature, An ISR Can Regulate Several Different Types Of Output Parameters.

BY DONALD V. COMISKEY

Power Trends Inc., 27715 Diehl Rd., Warrenville, IL 60555; (630) 393-6901; fax (630) 393-6902.

Integrated switching regulators (ISRs) are self-contained devices that are designed and optimized to function primarily as voltage regulators to provide a constant output voltage to a variable load. With the addition of a minimal amount of external circuitry, however, the ISR can be transformed into a constant current source, providing a variable output voltage across a variable load in order to maintain a constant current. This allows the designer to use the outstanding characteristics of a switching regulator in an application that would normally employ a linear device.

The advantages to using the ISR over linear device are a dramatic improvement in efficiency and a reduction in required board space. A series-pass transistor operated in its linear region can mean substantial power dissipation and the need for a large heatsink. In contrast, the ISR comprises a high-frequency PWN buck regulator with typical efficiencies of 85 to 95%. The ISR is housed in a small, SIP and with its minimal heat dissipation and high efficiency, no heatsinking is required.

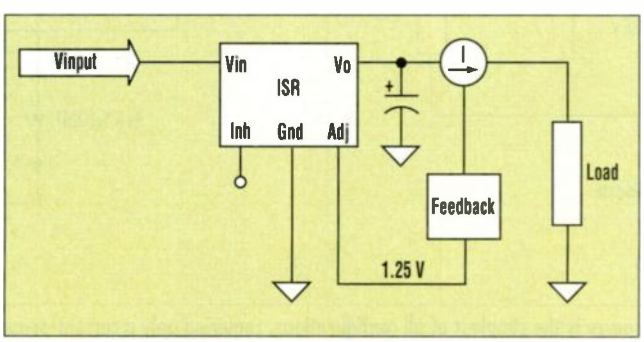
Among the number of applications that can take advantage of this constant-current source include those required to drive light sources, motors, focus coils, and various types of sensors. Battery-charging applications requiring high-current, bulk-charge states also can use this highly efficient constant-current source. Constant currents ranging from 100 mA to 3 A can be obtained.

The constant current application uses the adjust pin of the ISR in conjunction with an external feedback mechanism *(Fig. 1)*. Depending on the particular application, the feedback mechanism could be as simple as a single current-sense resistor. For other applications, the current-sense resistor could be used along with a simple op-amp stage.

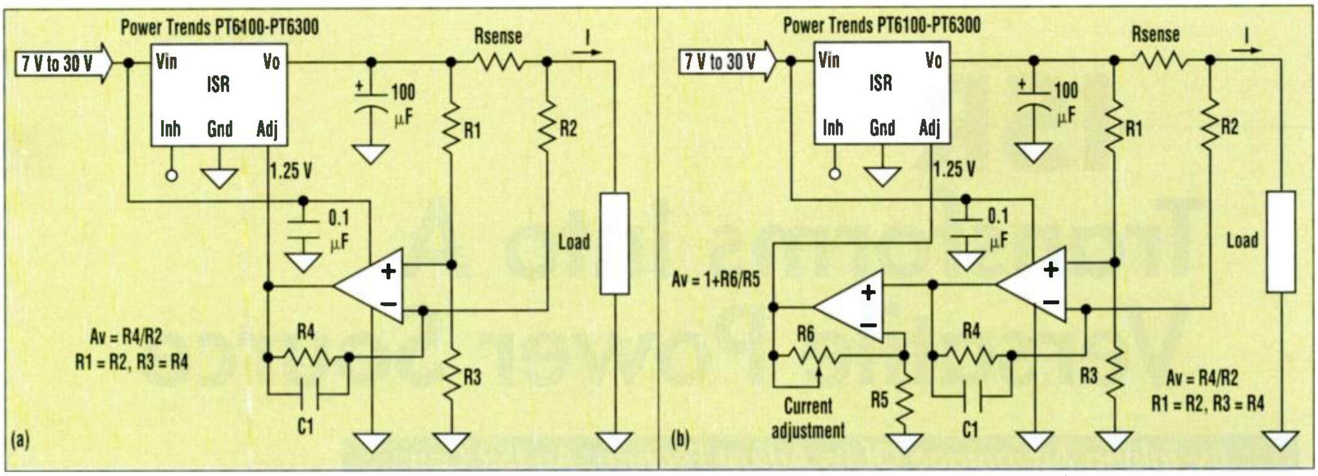
Theory Of Operation

Internally, the ISR's adjust pin is connected to the center-point of a high-impedance resistor-divider network used to sample the output voltage of the ISR. For proper operation, the external feedback circuit used for the constant-current source must appear as a low-impedance voltage source capable of dominant control of the adjust pin. For greatest accuracy, the characteristic impedance of this voltage source should be less than 1 kΩ. The use of a typical op-amp stage or a current-driven, low-impedance sense resistor are two methods of establishing this dominant voltage source *(Fig. 2a and b and Fig. 3a and b)*.

Normally, the ISR's internal circuitry would monitor and regulate its output voltage so



1. The ISR is transformed into a constant-current source using the ISR's adjust pin in conjunction with an external feedback mechanism.



2. The ground-referenced-load constant-current source uses an op amp as a difference amplifier to monitor the voltage drop across a sense resistor (Rsense) (a). Any necessary gain is built into the diff-amp stage. The ground-referenced-load constant-current source can be made adjustable by following the difference-amp stage with a variable-gain, noninverting, op-amp stage (b).

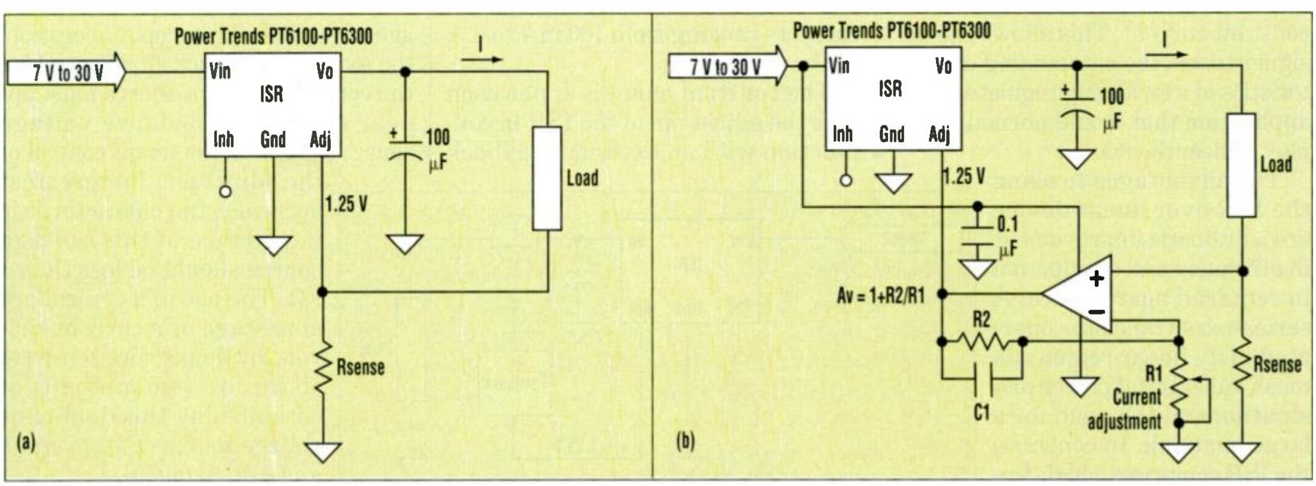
as to maintain a voltage of 1.25 V at its adjust pin. The addition of the external feedback circuit will, instead, force the ISR to monitor and regulate its output current in order to maintain the same 1.25 V at the adjust pin. The external circuit makes use of a current-sense resistor which provides a voltage translation of the delivered load current. This current-to-voltage translation is scaled so that the desired output current equates to a voltage of 1.25 V.

The scaling is accomplished by selecting the value of the current sense resistor and the gain of any associated op-amp stage. Efficiency and noise immunity are two things to consider when choosing the value of the current-sense resistor and any associated gain. A compromise needs to be made between the voltage drop across the resistor and the power dissipated by the resistor. Where possible, a rule of thumb is to select a resistor value that will develop a voltage drop of 100 mV at the desired output current.

Application

The constant-current source can be designed to accommodate either ground-referenced or floating load configurations. For a ground-referenced load, the current-sense resistor is placed directly in series with the output of the ISR and the load. The voltage drop across the resistor, hence the current, is measured differentially using an op-amp employed as a difference amplifier. Any necessary gain is built into the diff-amp stage *(Fig. 2a, again)*. Adjustment of the output current can be accomplished through an additional op-amp stage configured as a variable-gain, non-inverting amplifier *(Fig. 2b, again)*.

For a floating load configuration, the current-sense resistor is placed in series with the return end of the load and ground *(Fig. 3a)*. In its simplest form, the voltage drop across the resistor, hence the current, is monitored via a direct connection to the ISR's adjust pin. Since the adjust pin looks like a relatively high impedance, it can be assumed that the entire load current flows through the low-impedance current-sense resistor. In cases where efficiency outweighs simplicity, a noninverting op-amp stage, with gain, can be used along with a much smaller-



3. The floating-load constant-current source is the simplest of all configurations, requiring only a current-sense resistor (Rsense) that connects directly to the ISR's adjust pin (a). A more efficient version of the floating-load constant-current source employs a lower-value current-sense resistor and an op-amp stage with gain. The current can be adjusted using variable gain (b).

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Designing a front end for powering DC/DC Converter modules doesn't have to be a time consuming task. Our Modular Front End (MFE) series enables you to drop a fully integrated front end into your power supply to get you up and running immediately.
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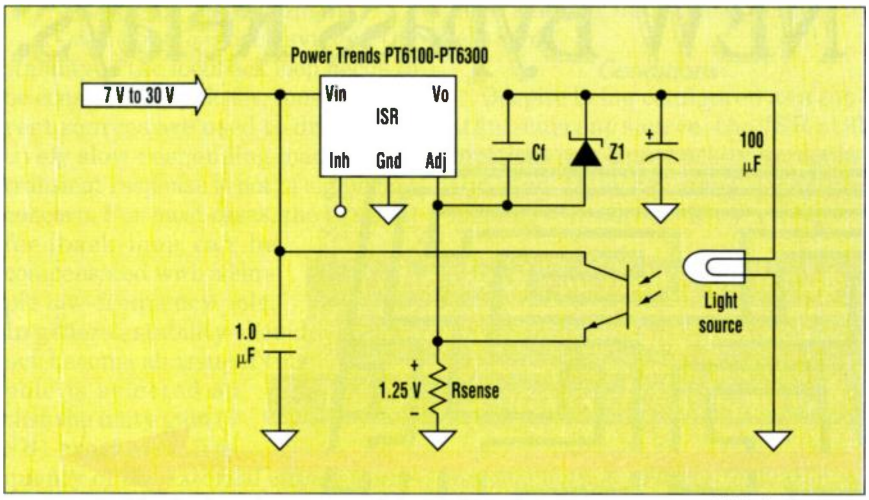
POWER TECHNOLOGY FOCUS: VERSATILE ISRs



6. An external feedback mechanism is used to transform the ISR into a constant-light-intensity source. The feedback mechanism comprises the light source, a photo detector, and a current-sense resistor. In effect, the ISR regulates the photo-transistor's output current.

stant-current source provides an ideal solution for this application. For both instances, the Power Trends PT6204 (2 A) ISR can be used to provide the 1.2 A. With an input voltage of 24 V and a nominal lamp voltage of 12 V, there is plenty of headroom to guarantee regulation.

For the ground-referenced lamp, a modified version of Figure 2a can be used *(Fig. 4)*. For the desired output current of 1.2 A, a 100-mΩ current-sense resistor will yield a voltage drop of 120 mV. In order to equate this 120-mV drop to 1.25 V at the adjust pin, the gain of the op-amp stage needs to be 10.4. Therefore, if R1 and R2 are selected as 1 kΩ, R3 and R4 will need to be 10.4 kΩ.

For the floating lamp, a modified version of Figure 3a can be used *(Fig. 5)*. For the desired output current of 1.2 A, a current-sense resistor of 1.04 Ω will need to be used to develop the 1.25 V at the adjust pin. It should be noted that even though this solution is very simple, the fact that the current-sense resistor will dissipate 1.5 W doesn't make it the most efficient approach. A more efficient solution would be to use the circuit of Figure 3b with a current-sense resistor of 100 mΩ and an op-amp gain of 10.4.

Constant Intensity Source

The versatility of the ISR becomes further evident with its use as a constant light-intensity source *(Fig. 6)*. The external feedback mechanism comprises a light source, a photo detector, and a current-sense resistor. This external feedback circuit forces the ISR to regulate the output intensity of the light source in order to maintain a voltage of 1.25 V at the ISR's adjust pin. A phototransistor is employed as an emitter follower and produces a predetermined photo-detection current at the desired light intensity. The detection current flows through the low-impedance current-sense resistor which is sized to develop a voltage drop of 1.25 V. In effect, the ISR regulates the photo-detection current from the phototransistor, which should correspond to the desired light intensity.

For greatest accuracy, the value of the current-sense resistor should be less than 1 kΩ. Depending on the response characteristics of the load and the detector used, external compensation (such as Cf) may need to be incorporated to ensure stable operation of the feedback loop.

As in the constant-current source, the right ISR needs to be selected to suit the current demand of the light source. Also, to meet the required headroom between the input and output voltages of the ISR, the voltage developed across the light source should not exceed Vin minus 2.5 V.

Optional Zener diode Z1 may be used to limit the maximum output voltage of the ISR or the intensity of the light source. This may become necessary in cases where the desired light intensity cannot be obtained due to degradation of the light source or an obstructed light path. The value of Z1 is chosen in order to clamp the output voltage to VZ1 + 1.25 V. Without Z1, the output voltage of the ISR could approach the input voltage in an effort to obtain the desired light intensity. As in the case of the constant-current source, the constant-intensity source should be designed so that the output voltage of the ISR cannot exceed 25 V.

Another Example

Assume that at the desired light intensity, the photo detection current is 5 mA. Then, Rsense = 1.25 V/5 mA = 250 Ω. The closed loop will regulate the 1.25 V across the 250-Ω resistor, maintaining a constant phototransistor current of 5 mA. The maintained 5-mA current corresponds to a regulated intensity from the light source.

The constant-current source and constant-intensity-source circuits described are just some of the alternative uses of the ISR. Conceivably, use of the ISR's adjust pin and an external feedback mechanism can transform the ISR into a generic power source, able to efficiently regulate of several different output parameters. The type of parameter being regulated would appear to be only limited by the availability of the appropriate sensor or transducer used in the feedback loop.

For example, the ISR could be used along with: a thermocouple to regulate the temperature oproduced by a heating element or thermoelectric device; an air-flow sensor to regulate the air velocity produced by a fan; a pressure transducer to regulate the output of a liquid pump, and so on. Who said switching regulators had to be boring? Here's your chance to be creative!

Don Comiskey is an applications engineer at Power Trends. He has worked with both the Power Systems Group at Northrop Grumman Corporation, and the Wireless Data and Automotive Products Groups at Motorola. He holds an ASEET from DeVry Institute of Technology, Chicago, Ill.

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500-W Switchers Feature Up To Seven Outputs

The MXXB Series of switching power supplies output 500 W and can have from one to seven outputs. Single-output models have ratings from 5 V at 100 A to 48 V at 10 A. All outputs are floating and individually regulated to ±0.2%. Other features include an efficiency of 85%, Class A compliance for conducted emissions, and an operating temperature range of 0° to 70°C. The supplies measure 2.5 by 5.05 by 9.0 in. and come with overload, thermal, reverse-voltage, and input undervoltage protection. Pricing ranges from $279 to $420, and delivery is from four to six weeks.

Deltron Inc., 290 Wissahickon Ave., P.O. Box 1369; North Wales, PA 19454; Jack Phillips, (215) 699-9261; fax (215) 699-2310. **CIRCLE 593**

Proportional DC-DC Converter Outputs Up To 10 W

Outputting up to 10 W, the P10 proportional dc-dc converter has an output voltage range of 100 to 8 kV, an efficiency of up to 80%, a load regulation of less than 10%, and an operating temperature range of –20° to 85°C. Continuous short-circuit protection and a pi-network input filter are provided. Measuring 2.5 by 3

by 0.88 in., the converter comes in a six-sided copper case with a nonconductive base. Pricing is $81 each per 100; delivery is from stock to two weeks.

Orion Industries Inc., 3 Industrial Dr., Unit 6, P.O. Box 206, Windham, NH 03087; Sales Dept., (603) 894-4242; fax (603) 894-4291. **CIRCLE 594**

MANUFACTURERS OF AC-DC POWER SUPPLIES OVER 500 W

Manufacturer	Output power (W)	Switching or linear	Output voltages (V dc)	Output	Input range (V ac)	EMI shielding options	Power-factor correction	Cooling options
ABP Rockville, MD Eyal Halevy (301) 424-1760 Fax (301) 424-5222 E-mail: abpco@erols.com	1200 to 1600	Switching	2 to 48	Eight	85 to 264; universal	Yes	Yes (0.98 to 0.99)	Fan included
Absopulse Electronics Ltd. Carp, Ontario John Gowanlock (613) 836-3511 Fax (613) 836-7488 E-mail: absopulse@abopulse.com	50 to 10 k	Switching	5 to 250	One to five	90 to 240, universal	Yes	Yes	Fan or convection
Astec Carlsbad, CA Chris Jones (760) 930-4780 Fax (760) 930-4700 E-mail: chrisjones@astec.com http://www.astec.com	500 to 6000	Switching (linears available for 15 to 115 W)	2 to 60	One to 12	85 to 264	Standard; EMI filter meets Level B conducted/ radiated	Yes, standard	Integral fan
Brandt Electronics Inc. Mountain View, CA Joe Churchill (415) 967-4944 Fax (415) 967-9105	50 to 5000	Both	2 to 12 k	Single and multi	Universal, autoselecting	Yes	Yes	Convection, conduction, fan cooled
Computer Products Inc. South Boston, MA Cheryl Peckham (800) 733-9288 Fax (617) 464-6612 http://www.computerproducts.com	3 to 3000	Switching	1.5 to 48	One to five	Both	Yes	Yes	Heatsinks, fans
Conversion Equipment Corp. Orange, CA Roy Allman (714) 637-2970 Fax (714) 637-8654 E-mail: rallman@cecpower.com	100 to 5000	Switch-mode only	1 to 100	Up to nine	90 to 264, autorange or universal	Yes	Yes	Convection, forced air, conduction, radiation
Custom Power Systems Inc. Ronkonkoma, NY Don Mulvey (516) 467-5328 Fax (516) 467-5066 E-mail: sales@custompower.com http://www.custompower.com	500 to 2000	Both	2.2 to 400	One to 10	85 to 265	Sealed or vented enclosures	Yes	Fan, convection, conduction
EG&G Optoelectronics Covina, CA Customer Service (818) 967-9521 Fax (818) 967-3151 E-mail: eod@egginc.com	Up to 4 k for modules; up to 300 k for systems	Both	3.3 to 300	One to 10	115 to 440	Yes	Yes	Air, baseplate, liquid
Electronic Measurements Inc. Neptune, NJ John Breickner (732) 922-9300 Fax (732) 922-9334	500 to 90 k	Switching and SCR	5 to 1000	Mostly single	110, 208, 230, 400, 480; user switchable	N/A	Yes	All air cooled
Engineered Magnetics Inc. Rancho Dominguez, CA Harry Ross (310) 635-9555 Fax (310) 898-3422	Up to 8 M	Both	Up to 15 k	Up to four	Up to 34 k	Special enclosure and magnetic shielding	Yes	Convection, forced air, or water cooled

High-Power UPS Saves On Rack Space

The model PUPS-1500R is a 1500-VA rack-mount UPS that requires only 5.25 in. of vertical rack space. The device comes with microprocessor technology in the form of an IGBT inverter. Protection features include brownout and surge protection, automatic battery test, internal diagnostics, overload protection, and automatic bypass for fail-safe operation. An RS-232 interface allows automatic shutdown of all popular networks, while user programmability allows customization to the specific application. Pricing is from $1899 and delivery is from stock.

***Behlman**, 80 Cabot Court, Hauppauge, NY 11788; Ron Storm, (516) 435-0410; fax (516) 951-4341.*

CIRCLE 595

Miniature DC-DC Converters Facilitate Power Distribution

Measuring 1.25 by 0.8 by 0.4 in., the 300WFR series of dc-dc converters has been augmented by seven new devices that take an input of 4.5 to 9 V and output from 3.3 to 15 V, or ±12 or ±15 V dc. The devices's standard features include 1500 V dc input-to-output isolation, continuous short-circuit protection, and low-output ripple and noise. Ouput voltage accuracy is ±1% and the line/load regulation is ±5%. The operating temperature range is -25° to 71°C and cooling is by free air. Pricing is from $25.60 to $27.60, depending on model; delivery is from stock to six weeks.

***Conversion Devices Inc.**, 15 Jonathan Dr., Brockton, MA 02401; Dave DeLuca, (508) 559-0880; fax (508) 559-9288.* **CIRCLE 596**

MANUFACTURERS OF AC-DC POWER SUPPLIES OVER 500 W

Manufacturer	Output power (W)	Switching or linear	Output voltages (V dc)	Outputs	Input range (V ac)	EMI shielding options	Power-factor correction	Cooling options
Gamma High Voltage Research Inc. Ormond, FL V. Demeo (904) 677-7070 Fax (904) 677-3039 E-mail: gammaHV@aol.com	5 to 1 k	Both	100 to 100 k	Four (max)	100, 200, 220, 240	Yes	Yes	None
International Power Sources Inc. Ashland, MA Susan Cervenak (508) 881-7434 Fax (508) 879-8669 E-mail: ips-sales@intlpower.com http://www.intlpower.com	15 to 1000	Switching	3.3 to 48	One to five	Universal and autoranging	Encaged box	Yes	Convection and internal fan
Kepco Inc. Flushing, NY Frank Toich (718) 461-7000 Fax (718) 767-1102 ftoich@kepcopower.com http://www.kepcopower.com	0 to 1500	Switching	3.3 to 48	One to three	Universal	Optional enclosure	Yes	Built-in fans in models over 200 W
Lucent Technologies Berkeley Heights, NJ Charlie Hartley (908) 508-8226 Fax (908) 508-8192 E-mail: cjhartley@lucent.com	10 to 5 k	Switching	1.5 to 170	Between one and eight	Universal and autoselecting	Either Class A or Class B	Yes	Forced air or convection
Melcher Inc. Chelmsford, MA Rob Sinclair (978) 256-1812 Fax (978) 256-4642 E-mail: rsinclair@melcher-power.com http://www.melcher-power.com	500 to 3 k	Switching	5, 12, 15, 24, 48	One to three	Universal	Fully shielded (all products)	Yes	Fan, heatsink/ convection
Mid-Eastern Industries Inc. Bergenfield, NJ Harold Lerner (201) 385-0500 Fax (201) 385-0702 http://www.techexpo.com/www/mideast	Up to 12 k	Linear	0 to 5, 0 to 30, 0 to 100, 0 to 400, 0 to 1000, 0 to 1500	One to three	57 to 440	Yes	No	Air, water, immersion in oil
Power Conversion Products Inc. Crystal Lake, IL Cathy Shelley (815) 459-9100 Fax (815) 459-9118 E-mail: cathys@pcpinc.com http://www.pcpinc.com	Up to 3 k per rectifier, up to four rectifiers per shelf	Switching	12, 24, 48	One per mounting shelf	85 to 264	N/A	Yes	Convection, and fan
RO Associates Sunnyvale, CA Wayne Niederjohn (408) 744-1450 Fax (408) 744-1521 E-mail: wniederjohn@roassoc.com http://www.roassoc.com	300 and 600 to 1 k	Switching	300 and 380	One	85 to 265	Yes	Yes	Yes
Sierra West Power Systems Las Cruces, NM John Camilliere (505) 522-8828 Fax (505) 522-8766	500 to 10 k	Both	0 to 500	One to 10	90 to 300; universal, autoselecting	Yes	Yes	Fan or conduction

Power-Factor-Corrected Front Ends Save Design Time

The MFE Series are fully integrated, board- and chassis-mountable, power-factor-corrected (PFC) front ends. The devices save time by allowing the designer to efficiently design in PFC front ends into telecom, file-server, and industrial applications. No external components are required to power dc-dc converters.

The series is available in 250-, 500-, 750-, and 1400-W versions, all of which include integral EMI filtering, hold-up capacitors, integral phase control, input overvoltage protection, and short-circuit protection. The devices have a profile of 1.1 to 1.5 in., and operate in temperatures up to 70°C. Regulatory approvals include Class B EMI, as well as UL and CE safety requirements. Complete monitoring signals, including overtemperature and shutdown, are included. Pricing is from $0.25/W.

***DPA Solutions**, 33 Comac Loop, Ronkonkoma, NY 11779; Don Mulvey, (516) 471-6300; fax (516) 471-0101; e-mail: sales@dpasolutions.com; Internet: http://www.dpasolutions.com.*

CIRCLE 597

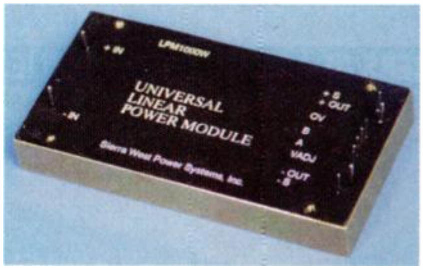
MANUFACTURERS OF AC-DC POWER SUPPLIES OVER 500 W

Manufacturer	Output power (W)	Switching or linear	Output voltages (V dc)	Outputs	Input range (V ac)	EMI shielding options	Power-factor correction	Cooling options
Signal Technology Corp. Keltec Operation Fort Walton Beach, FL Lynn Weese (850) 244-0043 Fax (850) 664-0546 E-mail: lweese@keltec.sigtech.com http://www.sigtech.com	200 to 10 k	Both	2 to 35 k	From one up	Universal	MIL-STD-461	Yes	Air, liquid, conduction
Spellman High Voltage Electronics Corp. Hauppauge, NY Eric Marko (516) 435-1600 Fax (516) 435-1620 E-mail: sales@spellmanhv.com	Up to 120 k	Switching	300 to 400 k	One to three	100 to 400	Yes	Yes	Fan, convection
Switching Power Inc. Ronkonkoma, NY John Bellone (800) 456-8118 Fax (516) 981-7266 E-mail: sales@switchpwr.com http://www.switchpwr.com	100 to 4 k	Switching	2 to 48	One to five	Universal, autoselecting (115/240)	Yes	Yes	Fan or custom options
Switching Systems International Anaheim, CA Jim McCarty (714) 712-4500 Fax (714) 712-4520 http://www.ssi4power.com	150 to 1 k	Switching, low-power linear auxiliaries available	2 to 85	One to nine	85 to 264, autoselecting	Class A and B, conducted and radiated	Yes	Convection, fan
Technology Dynamics Inc. Bergenfield, NJ Mark Jacobs (201) 385-0500 Fax (201) 385-0702 http://www.technology-dynamicsinc.com	15 to 3 k	Switching	3.6 to 500	Up to six	90 to 264	Yes	Yes	Convection, conduction, liquid
Tectrol Inc. Downsview, Ontario Paul Carroll (416) 630-8108 Fax (416) 638-0553 E-mail: sales@tectrol.com	10 to 4 k	Both	2 to 300	One to 12	85 to 264, universal and autoselecting	As required, to CISPR B	Yes	Fan or natural convection
Todd Products Corp. Brentwood, NY Ray DeGennaro (516) 231-3366 Fax (516) 231-3473 http://www.toddpower.com	150 to 1500	Switching	3.3 to 60	Single or multiple	90 to 264	Included	Yes	Convection, forced air
Unipower Corp. Coral Springs, FL John Jimenez (954) 346-2442 Fax (954) 340-7901 E-mail: sales@unipower-corp.com	250 to 3 k	Switching	2 to 48	Up to 10	85 to 264 universal, 85 to 132 or 180 to 264 autorange	Four- to six-sided case shielding	Yes	Open frame with external cooling, or cased with fan
Xentek Power Systems San Marcos, CA Stan Miner (760) 471-4001 Fax (760) 471-4021 E-mail: info@xentek.com http://www.xentek.com	150 to 1 k	Both	2 to 48	One to seven	85 to 264 universal, 85 to 145 and 185 to 260 autoselect	CISPR-11 and 22 for EMI	Yes	Convection and integral forced air

Linear Power-Supply Module Comes Complete

With much of the research and innovation in the field of power now focusing on switching power supplies, the designer is left with few choices when it comes to procuring a linear power supply. They can either purchase a complete power supply from a few companies that still manufacture linears, design their own, or use three-terminal regulators for low-current applications. So far, in-between modules haven't been an available option.

Recognizing this, Sierra West Power Systems has just announced a new line of patented linear power modules that contain the pass transistors, error amplifier, reference, current limiter, control circuitry, overvoltage crowbar, and input and output capacitors all in one package. Called the Universal Linear Power Module (ULPM), the highly flexible device can drive any kind of load and allows designers to quickly ,and relatively inexpensively, put together a custom power solution.



The fully encapsulated component is packaged in a standard 2.4-by-4.6-by-0.6-in. aluminum case and features a dropout voltage of just 300 mV with a 34-A output current. Rated at 1000 W at 34 A and 30-V output, the module's output voltage is externally programmable at 500 Ω/V from an output of 0 to 30 V dc. The input voltage range is 4.5 to 35 V dc. The module can be paralleled, has remote-sensing capability, and needs no external bias supply. The overvoltage and overcurrent trip points are externally adjustable. Not load sensitive, the modules will drive capacitive, inductive, motor, dynamic, and semiconductor loads.

The modules are priced at $150.00 each in sample quantities and delivery is from stock to four weeks. Other output voltages and power levels are available.

Sierra West Power Systems Inc., 300 N. Telshor Blvd., Suite 500, Las Cruces, NM 88011; John Camilliere (505) 522-8828; fax (505) 522-8766

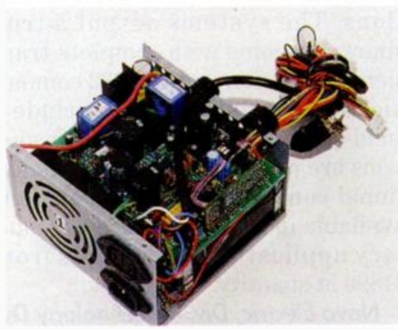
Patrick Mannion

Inverter Forms Core Of Miniature UPS/SMPS Combo

Although uninterruptible power supplies (UPSs) are not new, the consumer end of the computer-system market has been too cost-sensitive for what has traditionally been an expensive and bulky add-on. Resistance to the UPS's general acceptance also comes from the lack of awareness of the many benefits of a UPS.

In a breakthrough design that should push power protection into the mainstream, Amsdell Inc. has introduced a low-cost UPS/switch-mode power-supply combination that can fit in the palm of your hand. Called the Integrated Power Protection System (IPPS), the device weighs in at 3 kg (with battery) and uses the company's SCR-based miniature inverter.

The IPPS operates off 110/220 V ac, has a built-in microprocessor, and a capacity of 200 VA for up to 15 minutes



run time with a Pentium CPU and a 14-in. monitor. The ac transfer time is 4 ms. The device measures 150 by 150 by 85 mm, has a power factor of 0.7, an ac output current of 1 A (for the monitor), and an efficiency of over 85%. A maintenance-free, lead-acid battery is used (12 V, 4 Ah).

The cornerstone of the IPPS's design, and the reason it can reach the company's predicted $100 price range, is Amsdell's own inverter. Half the size of a credit card, the inverter uses SCRs instead of MOSFETs for the full-bridge switches. SCRs are smaller, less expensive, and easier to switch than MOSFETs. A high-frequency power MOSFET is used to turn the bridge on and off. The inverter's efficiency is rated at up to 96%, and it can be scaled in accordance with any conventional power supply.

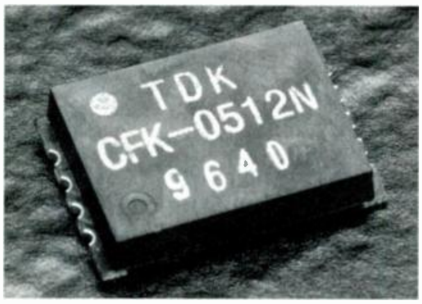
The internal IPPS will be available in production quantities by early 1998. Pricing is under $100.

Amsdell Inc., 45 Mural St., Unit 5, Richmond Hill, Ontario, Canada L4B 1J4; Mishaal Naik, (905) 881-3020; fax (905) 881-3023; Internet: http://www.amsdell.com.

Patrick Mannion

Low-Profile DC-DC Converters Output Up To 1.2 W

The CFK series of surface-mount dc-dc converters have a profile of 3.5 mm and output up to 1.2 W with an efficiency of 85% in load ranges of 20% to 100%. To reduce radiated EMI and



magnetic leakage, the package material consists of the company's composite ferrite material. The converters take an input of 5 V and output voltages of -5, ±12, –12, and –24 V. Full-rated output power is available at temperatures up to 50°C, with derating to 70°C. Pricing is under $15 each per 1000, and available now.

TDK Corp. of America, 1600 Feehanville Dr., Mt. Prospect, IL 60056; Pat Carson, (847) 390-4478; Internet: http://www.tdk.com. **CIRCLE 598**

On-Line UPS Handles From 3 kVA To 10 kVA

The True On-Line series of 3-kVA to 10-kVA UPS systems target both personal and commercial applications. The systems output a true sinewave, come with complete transient protection and RS-232 communication capabilities, and include a solid-state transfer switch. The systems are rack-mountable, have additional run-time capability, and are available in rugged designs for military applications. Pricing is from $1890 in quantity.

Nova Electric, Div. of Technology Dynamics Inc., 100 School St., Bergenfield, NJ 07621; Howard Schrier, (201) 385-0500; fax (201) 385-0702; e-mail: novaelc@mail.idt.net.
CIRCLE 599

10-W, Single-Output DC-DC Converter Outputs 3.3 V

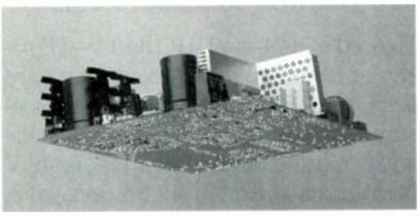
The DFC10 Series dc-dc converter handles up to 10 W while delivering 3.3 V to its single output with an efficiency of 83%. Measuring 1 by 2 in., the

converter has an operating temperature range of -40° to 85°C and takes inputs of 12, 24, or 48 V. Other features include continuous overcurrent protection and a five-side-shielded case. UL, CSA, and CE approvals have been acquired. Pricing is $51 each for 250; production quantities are available from stock in six to eight weeks.

Power-One, 740 Calle Plano, Camarillo, CA 93012; Sales Dept., (800) 678-9445; fax (805) 388-0476.
CIRCLE 600

Medium- To High-Power Supplies Are CE-Compliant

The RP Series of 500-, 750-, and 1000-W ac-dc supplies are CE-compliant and come with an adjustable main output (3.0 to 5.75 V) and 64 standard combinations of up to five total outputs.



The series provides up to 150 A and comes with auxiliary outputs delivering voltages of –12, 12, 3.3, 5.0, 24, or 48 V. Standard features include power-factor correction and signals such as fan fail, ac fail, and dc good. Options include current sharing, overcurrent protection with 10-second auto restart, VME signals, and output sequencing. The reliability is rated at 150,000 hours MTBF. Pricing is less than $0.50/W in quantity.

Lambda Electronics Inc., 515 Broadhollow Rd., Melville, NY 11747; John Carroll, (516) 694-4200; fax (516) 752-2627; e-mail: lambda@ix.netcom.com. CIRCLE 601

60-W DC-DC Converter Comes With A Low Profile

An addition to the company's EriPower PKG range, the PKG 2623 12-V, 60-W dc-dc converters have a profile of 11.0 mm and feature a ceramic substrate with copper plating for improved reliability and efficiency. The devices have an efficiency rating of 88% and an input voltage range of 18 to 36 V. Other features include an input-to-output isolation of 1000 V dc, ambient temperature operation up to 60°C, and a load regulation of 10 mV. Protection includes output power limiting, overvoltage, and thermal shutdown. Pricing is $63 each in 500-unit quantities.

Ericsson Components AB, Energy Systems Div., S-164 81 Kista, Sweden; Lars Thorsell, (46) 8 721 7045; fax (46) 8 721 7001; e-mail: eka.ekaltl@mesmtpse.ericsson.se. CIRCLE 602

350-W, DC-Input Supplies Also Are Hot-Swappable

The TMX-350 series dc-input power supply matches the size and performance of its RMX-350 ac-input counterpart. This allows OEMs to swap these 350-W, multiple-output supplies within a single mounting, cooling, and connection design. The TMX Series can be mounted in a redundant configuration with the RMX Series to provide a true fault-tolerant power system with battery back-up capability. The dc-input supplies feature current sharing, a dual-converter design, and compliance with both Bellcore and NEBS standards. Pricing is $455 each in quantity; delivery is six weeks.

Todd Products Corp., 50 Emjay Blvd., Brentwood, NY 11717; Sales Dept., (516) 231-3366; fax (516) 231-3473. CIRCLE 603

READER SERVICE 217

Low-Voltage DC-DC Converters Are High Density

The AK60 and AK80 are 500-kHz, fixed-frequency, dc-dc converter modules that output up to 100 and 192 W, respectively, with an efficiency of 86%. The AK60 has output voltages of 5, 12, 15, and 24 V and measures 2.3 by 2.4 in., while the AK80 outputs 3.3, 5, 12, 15, or 24 V and measures 2.4 by 4.6 in. Both feature undervoltage lockout and overtemperature shutdown to meet ETSI and NEBS standards. An isolation voltage of 1500 V allows them to meet EN41003 requirements. Other features include an operating temperature range of –20° to 85°C and an MTBF of over one million hours. Pricing for the 100-W AK60 is $89 each per 500, while the AK80 is $110 each per 500.

Astec America Inc., 6339 Paseo del Lago, Carlsbad, CA 92009; Phil Toplanksy, (760) 930-4713. **CIRCLE 604**

Hot-Swappable, Load-Sharing Switchers Output Up To 250 W

The CPA2-250 are 250-W switching power supplies that come with load-sharing and hot-swap capability, as well as built-in power-factor correction (0.99), all in a 1U-high rack-mount package. The two independently regulated outputs are individually configurable from 3.3 to 24 V. Features include EMI suppression exceeding Class B requirements, a universal input, and CE mark and UL/CUL/EN safety compliance. Protection includes overvoltage, short circuit, IEC68 shock and vibration immunity, and power-fault indication. Pricing is $250 each per 100 and delivery is from stock to eight weeks.

Power General, Div. of Nidec America Corp., 152 Will Dr., Canton, MA 02021; Charlie Welsch, (781) 830-1104; fax (781) 830-1155; e-mail: cwelsch@nidecpg.com; Internet: http://www.nidec.com. **CIRCLE 605**

24-Pin DIP DC-DC Converters Are Isolated To 1500 V rms

Housed in a 24-pin DIP, the TW-CB series of 1.5- to 3-W dc-dc converters are isolated to 1500 V rms. The devices measure 1.25 by 0.80 by 0.40 in., are available with input voltages of 5, 12, 24, or 48 V (±10%), and with output voltages of 5, 12, or 15 V. The line and load regulations are both ±1%. Other features include an internal pi filter, short-circuit protection, an operating temperature range of –25° to 71°C, and a ripple and noise figure of 1% peak-to-peak maximum. Pricing is $9 each in quantity. Delivery is from stock to eight weeks.

Polytron Devices Inc., P.O. Box 398, Paterson, NJ 07544; Sheri Lynn, (973) 345-5885; fax (973) 345-1264. **CIRCLE 606**

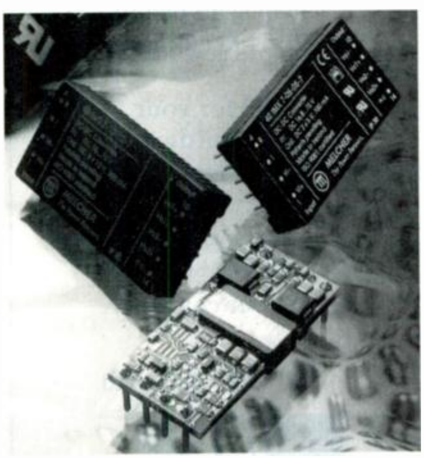
High-Voltage Supplies Come In Low-Profile Format

Measuring 19 by 19 in. with a height of 1.75 in. (10 and 300 W) or 3.5 in. (600 and 1200 W), the SL Series of 1- to 130-kV supplies have an efficiency of 85%. All models feature a resonant high-frequency inverter with proprietary control for high reliability in harsh environments. Other features include four input-voltage options of 100, 115, 200, and 220 V ac, and protection that includes overvoltage, arc, and short circuit. All bear the CE mark and are UL, CSA, and IEC950 approved. Pricing is from $1615.

***Spellman High Voltage Electronics Corp.**, 475 Wireless Blvd., Hauppauge, NY 11788; Sales Dept., (516) 435-1600.* **CIRCLE 607**

Low-Cost DC-DC Converters Use Planar Transformers

The IMX7 family of 7-W dc-dc converters uses planar magnetics and synchronous rectifiers to improve efficiency and facilitate surface-mount manufacturing. The devices come with four input-voltage options of 8.4 to 36 V, 16.8 to 75 V, 40 to 121 V, and 66 to 150 V, in a package measuring 1 by 2 by 0.4 in. A single output of 3.3 or 5.1 V, or dual, isolated outputs of 5/5, 12/12, 15/15, or 24/24 allow the configuration of 3.3- to 48-V outputs. The converter can be operated in parallel, with no derating from –40° to 71°C, or with an extended range of up to 85°C. Additional features include transient voltage protection per IEC 801, EMI levels below EN55022 level B requirements, and 1500-V-dc isolation. Pricing starts at $35 each per 2500.



***Melcher**, 187 Billerica Rd., Chelmsford, MA 01824; Rob Sinclair, (888) MELCHER; Internet: http://www.melcher-power.com.* **CIRCLE 608**

48-V Switchmode Power System Targets Communication

The Galaxy Power System 4848 is a 48-V, 4800-A power system for communications providers that features a 200-A switchmode rectifier design and a modular architecture with hot-swappable components. The system operates off a wide range of input voltages, including 208, 220, 240, 380, 400, and 480 V ac at either 50 or 60 Hz. Features include displays for load current and plant voltage, alarm monitoring for rectifiers and plant components, float/boost mode control, and low-voltage battery and load disconnects. Optional features include remote access, peripheral monitoring, and battery reserve-time protection. Both centralized and distributed configurations are available. Pricing for an 800-A version ranges from $33,700 to $35,000.

***Lucent Technologies**, Room 30L-15P-BA, 555 Union Blvd., Allentown, PA 18103; Response Center, (800) 372-2447, Dept. R45; fax (610) 712-4106.* **CIRCLE 609**

75-W DC-DC Converters Save On Cost And Board Space

The triple-output MP75 Series of 75-W dc-dc converters come in a half-size footprint of 2.4 by 2.5 in. Available in over 30 models, the devices have input voltages of 9 to 18, 18 to 36, 36 to 72, or 225 to 380 V, and triple-output-voltage options of 5, 12, and 12 V, 5, 15, and 15 V, or 5, 12, and 5 V. Single-output models are also available. All outputs are independent, short-circuit protected, and load regulated to *(continued on page 188)*

(continued from page 187)
±1% on the main output, and ±2% on the auxiliaries. The main output is adjustable and comes with remote sense. Other features include a transient response of 500 µs, isolation up to 4300 V dc, and an efficiency figure of up to 85%. Pricing is under $100 in quantity.

International Power Sources Inc., 200 Butterfield Drive, Ashland, MA 01721; Richard Sakakeeny, (508) 881-7434; fax (800) 226-2100; Internet: http://www.intlpower.com. **CIRCLE 610**

Current-Sharing AC-DC Supply Meets EN61000 Limits

Meeting EN61000 harmonic limits and FCC/VDE/CISPR class B standards, the CMP350 350-W ac-dc supply offers current-sharing and remote-sense capability. The supply also complies with UL1950, EN60950, and CSA 22.2-234/950 safety standards. Measuring 10 by 5 by 1.75 in. (open frame) or 10.5 by 5 by 1.75 (enclosed), the supply has a universal 90- to 264-V-ac input, one to four regulated outputs, and includes overcurrent, overvoltage, and overtemperature protection. Pricing is $378 each per 250.

Computer Products, 7 Elkins St., South Boston, MA 02127; Phil Brucato, (800) 733-9288; fax (617) 464-6679. **CIRCLE 611**

Miniature DC-DC Converter Has High Power Density

The EM Series of dc-dc converters measure 2.0 by 2.0 by 0.45 in. and handle up to 25 W. The converters take inputs of 9 to 18, 18 to 36, or 36 to 72 V and provide single or dual (balanced) outputs of 5, 12, or 15 V, and triple outputs of 5/±12, 5/±15 V, and 5/12/-15 V. Standard features include 500-V-dc input-to-output isolation, an efficiency of 88%, a load regulation (dual output) of ±1%, and a ripple/noise figure of 1% peak to peak. Other features include power foldback short-circuit protection and a shielded case. Pricing is from $69.70 to $75 each per 100.

Wall Industries Inc., 5 Watson Brook Rd., Exeter, NH 03833; Russ Berube, (603) 778-2300; fax (603) 778-9797; e-mail: wallind@nh.ultranet.com; Internet: http://www.conres.com/wtop.htm. **CIRCLE 612**

Charge Pumps Convert Power Efficiently Without Inductors

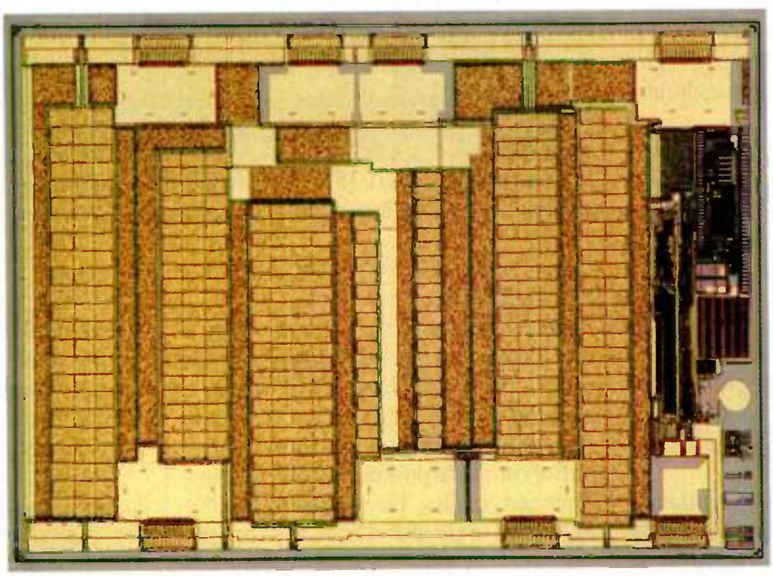
Charge Pumps, Invented Over Twenty Years Ago, Are Witnessing A Resurgence Of Interest In The Design Community.

Frank Goodenough

SPECIAL REPORT

After two decades of "kicking around," charge pumps are beginning to come into their own. In fact, any designer considering a dc-dc converter for a portable application such as a cellular telephone or a PDA might think about using a charge pump instead of an inductor-based device.

The term "charge pump" refers to a type of dc-dc converter that uses capacitors rather than inductors or transformers to store and transfer energy *(Fig. 1)*. Charge pumps are often referred to as switched-capacitor converters. They include one or more switches or diodes that charge and discharge one or more of the circuit's capacitors.



Art Courtesy: National Semiconductor Corp.

Only four companies offer charge-pump product lines —Maxim Integrated Products Inc., Sunnyvale, Calif.; Linear Technology Corp (LTC), Milpitas, Calif.; National Semiconductor Corp., Sunnvale, Calif.; and Analog Devices Inc., Norwood, Mass.

Like Maxim with its RS-232 family of ICs, many companies use them internal to other ICs. For example, both Maxim and LTC use charge pumps in rail-to-rail I/O op amps, while SGS-Thomson uses them as a bootstrap supply in a 600-V half-bridge driver (the L6569) where they aid in driving n-channel power FETs and IGBTs. They also use them in a low-dropout (LDO) controller (LPR30) designed to drive an external n-channel MOSFET pass device.

To understand how a charge pump works, we must first look at its predecessor, the classic 7660 *(see "The colorful history of the 7660 charge pump IC," p. 192)*. That particular device operates as either a voltage doubler or as an inverter *(Fig. 1, again)*. That is,

$$V_{OUT} = 2 \times V_{IN}$$

As a voltage doubler, during phase 1 when switches S1 and S2 are closed and S3 and S4 are open, capacitor C1 charges to:

$$q1 = C1 \times V_{IN}$$

During phase 2, when switches S1 and S3 are open and S3 and S4 are closed, the charge from capacitor C1 (q1) plus an equal charge (q2) consisting of $C2 \times V_{IN}$ is transferred to capacitor C2. Since q1 = q2,

$$V_{OUT} = 2 \times V_{IN}$$

As an inverter, during phase 1 when switches S1 and S2 are closed, pump capacitor C1 is charged to:

$$q1 = C1 \times V_{IN}$$

During phase 2, switches S1 and S2 are open, S3 and S4 are closed, and the charge on capacitor C1 is transferred to C2 and inverted. That is, the positive terminal of C1 is connected to ground and the negative terminal is connected to the output.

The most compelling reason to use charge pumps is to avoid inductors. Why? Compared with capacitors, inductors are offered by fewer suppliers; have fewer standard specifications or dimensions; have greater sensitivity to layout; feature greater height; produce more electromagnetic interference (EMI); and are higher in cost.

On the other hand, until about five years ago, charge pumps have held themselves back. The only available device was the original 7660. It was a simple voltage doubler/inverter rated at about 20 mA of output current. It typically converted a 5-V rail to 10 V or to -5 V. It came in an 8-pin DIP with an unregulated output.

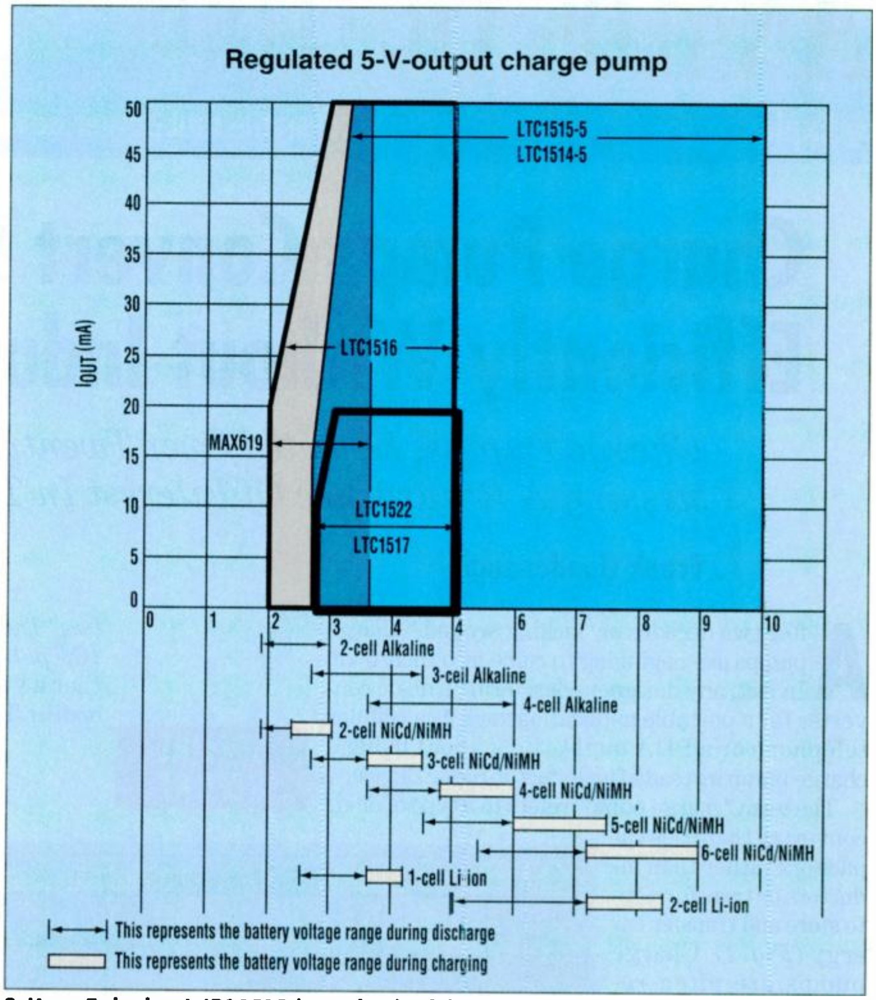
When Maxim introduced their RS-232 chip sporting the dual positive and negative outputs a few years ago, they discovered that many of their customers were only using it for its charge pump, not for its transceivers. Soon after, both LTC and Maxim came out with standalone devices to do the job.

The last few years has seen a flurry of developments in charge pumps, and as noted earlier, Analog Devices is jumping into the arena. These companies have essentially come up with a broad choice of charge pumps that are much more versatile and easier to use. Most new charge-pump applications are found in battery-powered applications. Examples of charge-pump advances include:

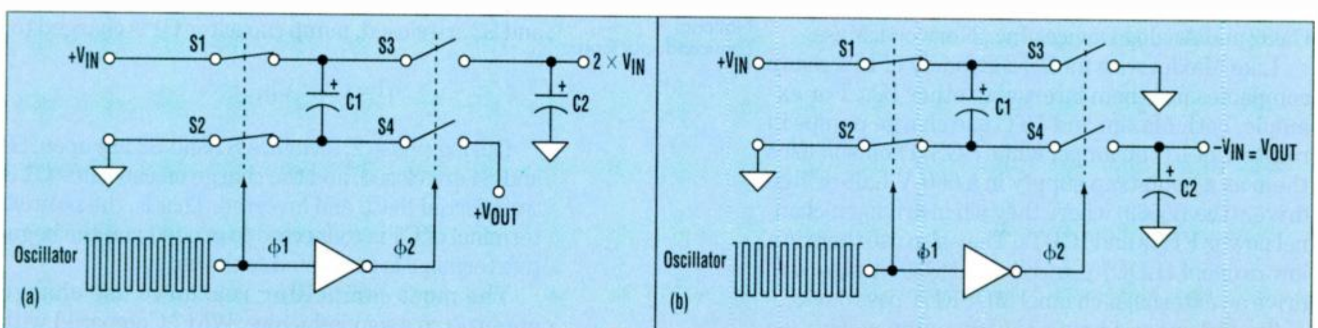
- Multiple output devices
- Regulated output devices
- Unregulated, high-current-output devices
- Higher and user-selectable switching frequencies
- Greater accuracy
- Lower ripple
- Lower output impedance
- Fractional-ratio converters that convert 5 V to 3.3 V, and vice versa
- Shut-down capability
- Smaller size
- Charge pumps that are being developed for special tasks such as providing the negative bias voltage required by the GaAs amplifiers in portable wireless equipment.

Many of the advances in current-generation charge pumps are very dependent upon other advances. For example, a higher operating frequency is responsible for lower ripple, and for smaller size of complete pumps as off-chip capacitors are smaller. The size decrease lies at the top of the list of charge-pump advances. It signifies that charge pumps have joined the forces of "deintegration." They can be sprinkled anywhere in a system, even if it's already been designed on a single chip. Single-output devices appear in SOT-23 packages, multiple-output devices in slightly larger SOTs, and in tiny 8-pin packages.

One way to examine the advances in charge pumps is to compare them with the original 7660, which Maxim has done for a handful of their recent SOT-23-



2. Linear Technology's LTC 1515/1514 family of charge pumps handles a wide range of input voltages. They satisfy battery charging requirements during charging and discharging modes.



1. Charge pumps can operate in either one of two modes: as voltage multipliers (a), or as voltage inverters (b).

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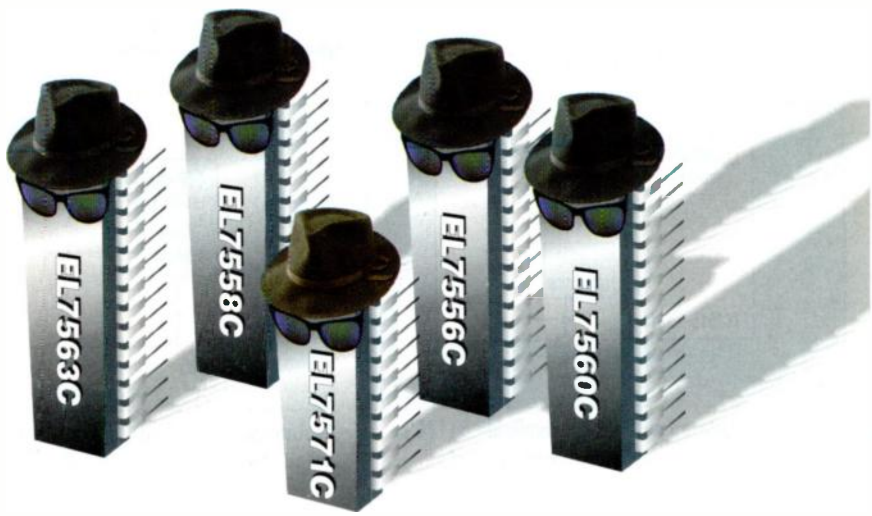
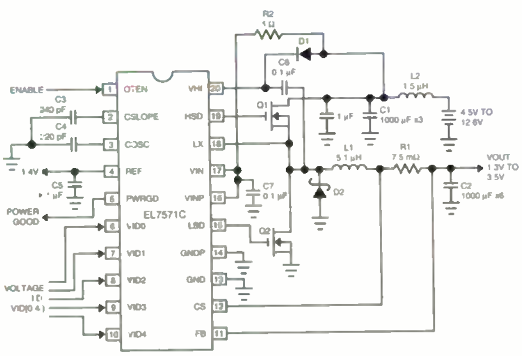


EL7571C
PWM Step Down Controller



- V_{IN} = 4.5V to 12.6V, V_O = 1.3V to 3.5V
- External FETs, I_O = >20 Amps
- >90% Efficiency
- 1% Output Accuracy
- Synchronous Switching
- Current Mode Control
- 5-bit DAC Controlled Output Voltage
- Operates Up to 1 MHz

EL7556C Adjustable CPU Power Supply Unit

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- Simple to Use
- Integrated FETs on Chip
- High Efficiency >90%
- Compact Design
- Operates Up to 1 MHz
- Low Cost

EL7558C
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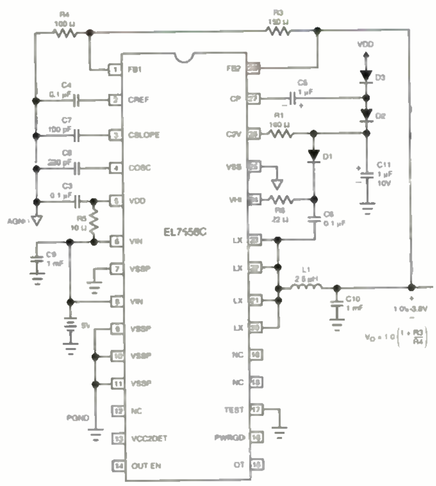

- V_{IN} = 4.5V to 5.5V, V_O = 1.0V to 3.8V
- Internal FETs, I_O = 8 Amps
- >90% Efficiency
- 1% Internal Reference
- Synchronous Switching
- Current Mode Control
- No Heat Sink Required
- Operates Up to 1 MHz

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- 1% Output Accuracy
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- Current Mode Control
- 4-bit DAC Controlled Output Voltage
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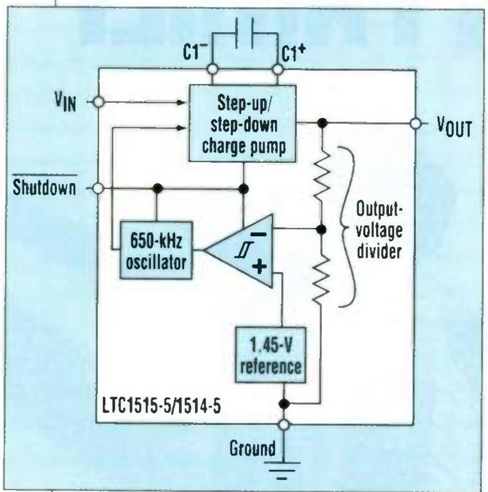
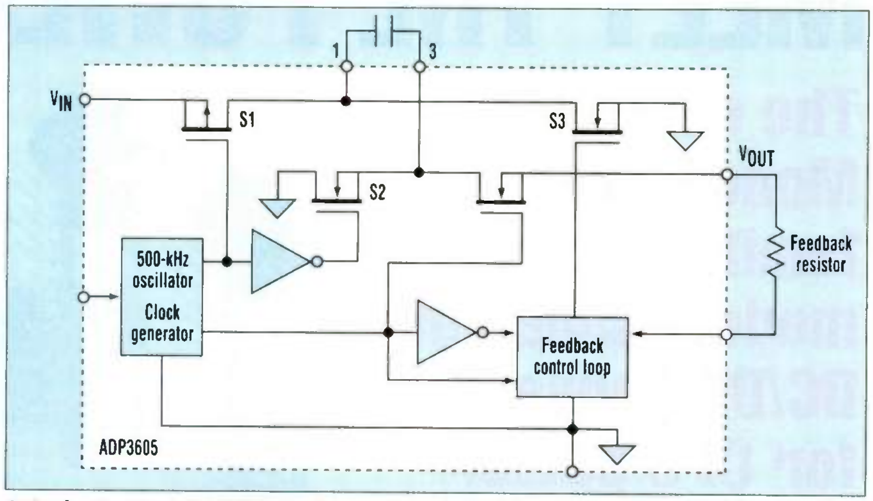
READER SERVICE 140



3. Regulated outputs are available on LTC's 1515/1514 family of charge pump ICs.



4. Analog Devices' ADP3605 regulated-output charge pump IC provides a -3-V inverted output at a current of 120 mA.

packaged charge pumps *(Table 1)*. Note that the MAX871 uses capacitors as small as 0.1 µF, yet maintains an output impedance below 35 Ω. The 7660 needs 10 µF to achieve an output impedance of 55 Ω. The impedance of both the switches and the capacitors contribute to the total output impedance. In addition, Maxim has doublers (not inverters) in SOT-23 packages (the MAX1682/1683) that are otherwise identical to the MAX828/829.

LTC, long an IC charge-pump supplier, has just introduced a new family of charge pumps aimed at battery charging and other tasks in portable equipment and systems *(Table 2)*. Sporting most of the bells and whistles of what might be called "third-generation charge-pumps," they're particularly aimed at dealing with a declining battery voltage. This is a common situation where it is necessary to provide a regulated output voltage with a battery voltage that starts out above the supply's output voltage when fresh, and declines to below the output voltage after

The Colorful History Of The 7660 Charge Pump IC

Charge pumps made up of discrete semiconductors or vacuum tubes have been around considerably longer than their IC versions. Called "flying capacitor" circuits, they were preceded by electromechanical charge pumps that used relays. Prior to that time—during the early 1930s—there were purely mechanical charge pumps (such as the ones that generated "man-made" lighting without inductors or transformers at the GE exhibit at the 1939 New York World's Fair). Those early charge pumps were used to test high-voltage power systems and components. They charged high-voltage capacitors in parallel and discharged them in series.

It took an engineer by the name of Dave Bingham, then of Intersil, to figure out how to build an IC charge pump. However, several enormous challenges stood in the way. Bipolar technology was great, but it lacked a good switch. CMOS provided a good switch, but potentially latched-up. For CMOS to work, the wells (or tubs) containing the n-channel FETs (in a p-well process) should be tied to the most positive supply. Otherwise, the wells forward-bias and latch-up occurs.

In a typical charge pump, the most positive supply at turn on is the input voltage, say 5 V. However, once operational, the most positive supply becomes the internally generated voltage, which in Bingham's 7660, runs twice the input supply or +10 V. Some of the top analog IC designers of the time (the late 1970s) said that it couldn't be done, and that latch-up was inevitable.

In response to that challenge, Bingham developed a topology that avoided forward-biasing the well by the use of "well snatchers." The well snatcher sensed the output voltage and handed over the well biases to ensure that they would always be attached to the most positive potential in the die. Special layout tricks ensured that any renegade minority carriers would be sucked up long before they could form silicon control rectifiers (SCRs), further cutting the chance of latch-up. To everyone's amazement, the circuit worked.

Since no customer had ever before asked for a monolithic charge pump (no one ever asked Intel for a microprocessor), the part was launched in the late 1970s with some trepidation by Intersil. But it became an instant success. Some 20 years later, millions of units a month of the 7660 are being produced from many suppliers (for some suppliers, the 7660 is their only charge pump). Is there a 20-year-old digital IC that can claim it is still going into new designs? Bingham continued to refine and improve on the original 7660. Early on, at Maxim Integrated Products (which he founded), Bingham developed a charge pump that generated both plus and minus voltages (+2 V and −2 V from the input voltage). He then combined it with RS-232 drivers and receivers to form the very first 5-V powered RS-232 transceivers.

use. For example, alkaline batteries start at 1.5 V and decline to 0.9 V at end of life. This situation demands a buck-boost topology. The LTC1514-5 and LTC1515-5 charge pumps do just that kind of job. They and several others are displayed on a chart showing the range of battery voltages they serve *(Fig. 2)*.

The proprietary regulator section of these charge pumps with their wide input voltage range (horizontal axis) consists of a charge pump, a reference, a comparator, and some logic *(Fig. 3)*. When the divided-down output voltage drops below the reference voltage, the charge pump is enabled, boosting the output back into regulation. A unique architecture allows the input voltage to be either stepped-up or stepped-down to produce a regulated output. Internal circuits sense the voltage between the input and output and control the charge pump's operating mode (step up or down). In addition, the output impedance of the charge pump is adjusted to halt large inrush currents and to allow for a wide input range. When the input voltage is lower than the output, the charge pump operates as a doubler. When the input is greater than the output, the charge pump operates as a step-down gated switch.

Analog Devices' new family of charge pumps contains a regulated inverter—the ADP3605. It puts out 3 V at 120 mA *(Fig. 4)*. The charge pump runs off a single positive rail as low as 3 V and provides an output voltage range from –1.2 to –4 V. In addition, a single external feedback resistor sets the output voltage.

National Semiconductor has realized what should be a rapidly growing niche market; in order to fill it, they recently developed a proprietary circuit based on an array of CMOS switches. When operated in a preprogrammed sequence, they provide their charge pumps—such as their model LM3350—with the ability to step-up or step down their input voltage in a 3:2 or 2:3 ratio. The charge pump's internal clock runs at 900 kHz, permitting the use of tiny, low-cost chip capacitors. It sports a shutdown mode and comes in an MSOP-8 package.

As CPU voltages continue to drop, it will be interesting to see if other fractional charge pumps appear. As of this writing, many companies are falling over each other to get into the race to fill market needs. The current trend is 5 V to 3.3 V to 1.8 V, but even lower voltages are on the horizon. Stay tuned for further developments.

Companies mentioned in this article

Analog Devices Inc.
3 Technology Way
Norwood, MA 02062
(800)262-5643
http://www.analog.com
CIRCLE 588

Linear Technology Corp.
1630 McCarthy Blvd.
Milpitas, CA 95035
(408) 432-1900
http://www.linear-tech.com
CIRCLE 589

Maxim Integrated Products Inc.
120 San Gabriel Dr.
Sunnyvale, CA 94086
(408) 737-7600
http://www.maxim-ic.com
CIRCLE 590

National Semiconductor Corp.
2900 Semiconductor Dr.
Sunnvale, CA 95052
(408) 721-5000
http://www.nsc.com
CIRCLE 591

SGS-Thomson Microelectronics Inc.
55 Old Bedford Rd., Lincoln North Bldg.
Lincoln, MA 01773
(617) 259-0300
http://www.st.com
CIRCLE 592

TABLE 1. COMPARING MAXIM'S CHARGE-PUMP ICs WITH THE 7660

Parameter	7660	MAX828	MAX829	MAX870	MAX871
Board area* (in.^{2}/mm^2)	0.048/31.0	0.013/8.3	0.013/8.3	0.013/8.3	0.013/8.3
Height (mm)	1.75	1.45	1.45	1.45	1.45
Output resistance (ohms)	55	20	20	20	20
Oscillator frequency (kHz)	10	12	35	125	500
I_Q (µA)	110	60	150	700	2600
Price (10k-unit lots)	$1.05	$0.80	$0.80	$0.80	$0.80

*Including capacitors

TABLE 2. COMPARING LINEAR TECHNOLOGY'S REGULATED DC-DC SWITCHED-CAPACITOR IC CONVERTERS

Device	Current	Input voltage range	Significant features
LTC1517ST-5	Up to 20 mA	2.7 to 5 V	Available in 5-lead SOT-23
LTC1522CS8	Up to 20 mA	2.7 to 5 V	Available in SO-8 Has shutdown capability
LTC1522CMS8	Up to 20 mA	2.7 to 5 V	Available in MSOP Has shutdown capability
LTC1515-3/5, -3.3/5	Up to 50 mA	2.7 to 10 V	Has step-up/step-down capability with power-on reset
LTC1514-3.3, -5	Up to 50 mA	2.7 to 10 V	Has step-up/step-down capability with low-battery indication

How Valuable	Circle
Highly	585
Moderately	586
Slightly	587

Verification Is Revolutionizing The IC Design Process

Shrinking Process Geometries, Increased Capacity, And Complexity Of DSM Design Set The Stage For A New Verification Methodology.

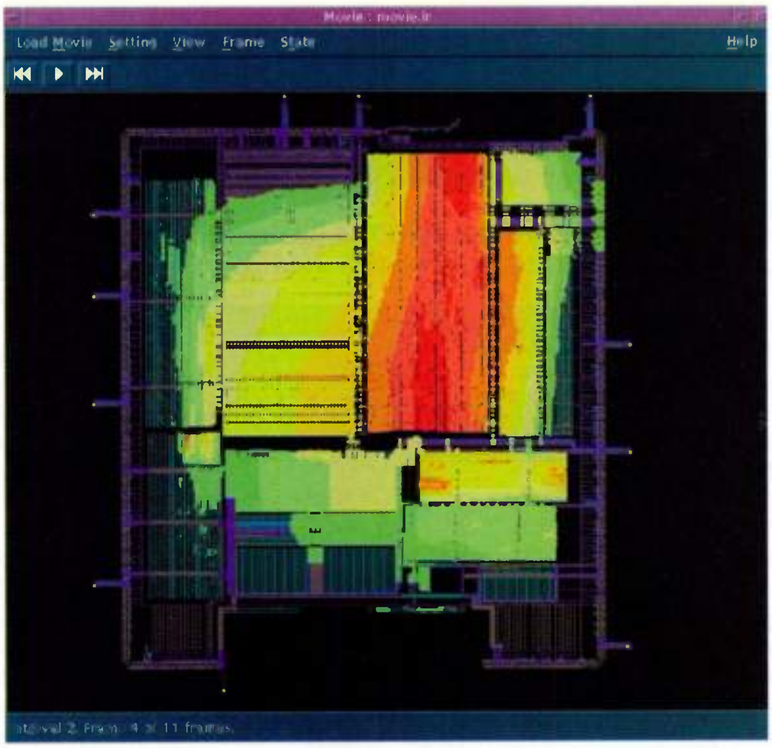
Cheryl Ajluni

The electronic design automation (EDA) industry is facing a verification challenge that has the potential to dramatically change the face of IC design. Analysts at Dataquest, San Jose, Calif., concur, having recently identified verification as being at the heart of two of the major shifts taking place in IC design. As stated in the company's EDA Landscape report: "The first and most obvious shift is the adoption of the resistor-transistor logic (RTL) netlist, if it can be called a netlist, as the golden netlist. Gate-level design no longer has a place in today's design methodology.

The second shift is the movement of analysis tools into both RTL and physical verification realms. The third shift is the abandonment of separate verification teams as a viable concept. Verification teams will retreat into the background and once again the design team will bear total responsibility for the design."

Anticipating this challenge, just about every EDA-related company is trying to re-identify itself as a "verification" company. As a result, confusion on both the part of the designer and the vendor has surfaced on everything from how to define it, and how it will impact today's design methodologies, to how to develop appropriate solutions.

SPECIAL REPORT



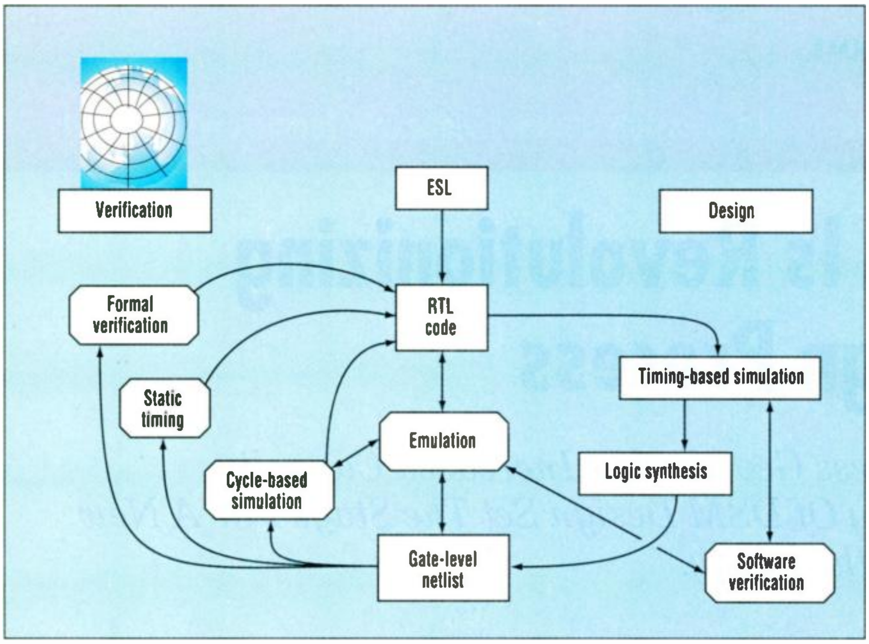
Art Courtesy: Simplex

What's considered to be traditional verification, such as simulation and prototyping, typically works well for modern IC designs made on processes with line widths of 0.5-µm or smaller. Although it is characterized by a division between functional or front-end verification strategies, and the back-end or physical verification strategies, traditional verification is generally considered to be a front-end issue.

But as IC designs migrate to features below 0.5 µm to true deep-submicron (DSM—0.35 µm and below) environments, the verification picture changes dramatically. The new verification methodology, in whatever final form it may be, will be comprised of any number of component pieces, ranging from code-coverage, RTL verification and extraction, to hardware/software co-verification and verification of IP (intellectual property) *(Fig. 1)*.

Identifying The Problem

The answer to how verification has evolved may be gleaned by looking at the history of EDA *(see "A*



1. This graphic offers a look at the new IC design verification tool suite as determined by Gary Smith, EDA Analyst at Dataquest, San Jose, Calif.

look back at EDA's history," p. 198). Design capacities and performance would not be able to grow without smaller design geometries that have caused the breakdown of traditional verification. An additional factor is the "consumerization" of electronics, a trend that has shortened design cycles and increased time-to-market pressures. Speeding up the design cycle typically means trying to speed up simulation and eliminating design iterations. These occur at the front end of the design cycle and have led to such advances as formal verification, faster simulators, accelerators, and virtual prototyping.

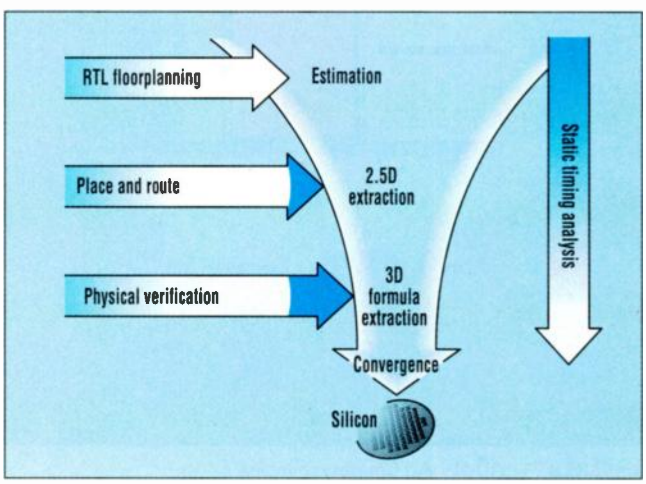
The solution to the verification challenge lies in understanding how these process changes will change how design and verification methodologies must work together. Shashank Goel of Simplex Design Systems explains, "IC design is now an issue of yield; the ability to supply parts in a short amount of time, not just time-to-market. Yield used to be a functional issue, but now this isn't enough. Now the designs need to be reliable enough to run at certain speeds; this means better verification. But, at 0.25 µm, designers are forced to build systems and finding that their old verification techniques no longer work. Many designers are trying to re-engineer old tools and are finding this approach still doesn't work. The problem is that older non-submicron verification technologies could only tell you a design would work at certain criteria. Now density, complexity, and logistics also are important for verification. So, the emphasis has moved from making the logic work to how the logic works. IC design is now verification of infrastructures."

Verification And The Designer

IC designers working with 0.35-µm geometries are hitting a verification wall because traditional verification techniques no longer provide them with the information they need to ensure a design will work properly. This is the view held by Rod Favaron of Mentor Graphics, Wilsonville, Ore. He explains, "You need to be able to answer three questions. Does your design function correctly? Does it meet performance? And, after it's built, does it still work? So, verification for today's IC designer falls into three categories: function, performance, and producibility."

Favaron adds, "When addressing the issue of chip verification, there are five problem areas or verification bottlenecks that the designer should be aware of: RTL verification and analysis such as RTL floorplanning, hardware-dependent software which applies to the marrying of the hardware and the software together, logic verification and analysis (for example, how much faster can we do our job), testability, and DSM verification and analysis which includes such things as physical verification and extraction, and DSM interconnect."

Because the verification problem stems from DSM issues at the back end of the design cycle, it's logical to assume that this is where the most dramatic changes in verification will take place. As Goel explains, "Deep-submicron (nanometer) verification is essentially very different from its previous incarnation. Digital design in micrometer technologies (25 to 0.5 µm) required physical verification for two purposes, process design rule adherence and netlist comparison, to catch errors in 'circuit to layout' translation. If designers were right on both counts, the chips were fabricated with high fidelity. Today's finer-process technologies and SoC design methods exacerbate these issues—although, you may find that both design-rule checking (DRC) and layout versus schemactic (LVS) are well addressed even in the DSM world—and introduce a high probability of 'soft errors' such as coupling-related logic distortion and delays, and IR-drop-related gate-strength reduction. These effects show up during regular full-speed



2. This performance-verification methodology from Cadence offers one way for the IC designer to overcome the failings of traditional IC design verification techniques.

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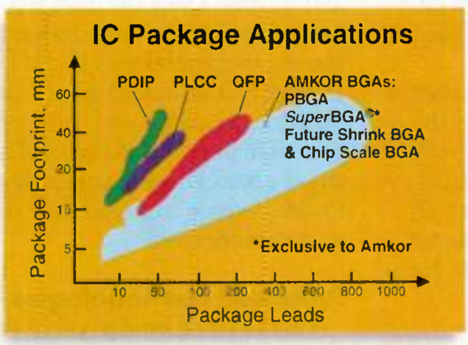

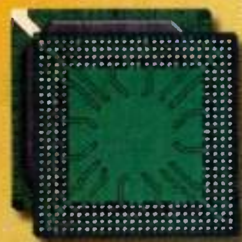

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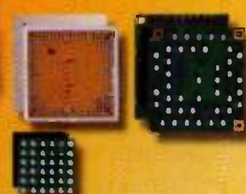

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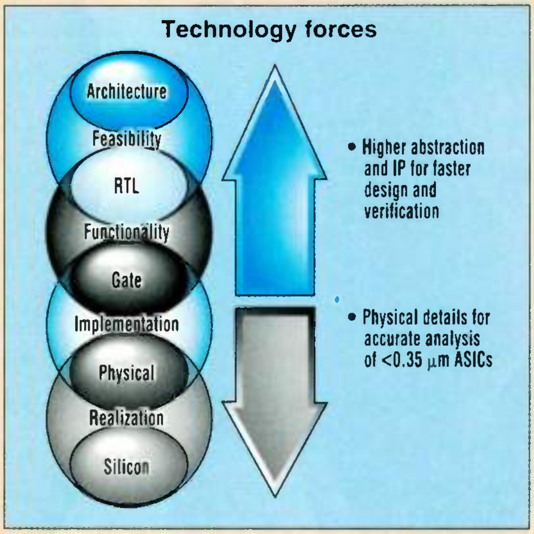
READER SERVICE 109

A Look Back At EDA's History

To understand how verification has become such a crucial issue, it might be wise to first take a step back and understand how EDA has evolved. During the heydays of CAD, designs had capacities of no more than 1000 gates. All placement and layout was done by hand. Then, along came the birth of EDA in 1981. It developed out of the challenge of automated design creation. The innovations that made this possible were schematic capture and simulation. This first generation of EDA witnessed designs with capacities as high as 5000 gates on 2-µm processes. Those of us who were around in those days will remember the emergence of companies such as Daisy, Mentor, Valid, and Zycad.



In the late 1980s, change was again in the air thanks to a new challenge of high-level design. Verilog and VHDL high-level design languages (HDLs) were innovations that addressed this challenge. This second generation spanned from 1988 to 1994, during which time the 1-µm barrier was broken and design capacities as high as 100 Kgates were achieved. Many factors played a role in the shaping of this era. The demand to bring prices down gave way to lots of electronics being placed on a single chip. And, the development of Verilog and VHDL to describe design and synthesis meant that sophisticated tools were needed for placement and routing. A great deal of attention was focused on IC layout and design implementation. Companies like Cadence that focused on the layout problem and Synopsis with its synthesis solution came to the forefront of the design community.

Now in 1997, a new challenge of design verification is facing the EDA community as it enters its third generation, prompted by a migration to deep-submicron designs. The problem is compounded by the fact that design capacities have grown astronomically large—upwards of 1 million gates *(see the figure)*. The ability to leverage such high capacities with continually decreasing design geometries opens the door to tremendous performance increases. Unfortunately, today's design tools are unable to leverage these performance gains to the fullest because they lack appropriate verification means, especially at the physical end of the design cycle. Designers are forced to ponder not whether they can build something so huge, but will it work if they do?

Many designers thus end up overdesigning or guardbanding. In other words, the designer doesn't get his or her bang for the buck. This is the first piece in a ripple that propagates throughout the entire design cycle. It starts at the back end of the design cycle and works its way forward. Design creation is forced to travel farther downstream as design verification travels upstream. And, it will continue to be driven upstream as systems on a chip (SoC) become more complex. The final implementation of the design must now be verified against the original design conception.

operation and not during the first vector stress on a tester."

Goel further says that "as the majority of design starts move to .25 µm, these effects will become more pronounced, causing either much larger overdesigns or a failure of the design to converge swiftly to the specification. Informal handling of these effects tends to spread in performance across the lots of parts being designed. To avoid large variance in the performance of fabricated chips, designers will need tools to verify each of these physical effects, so as to tighten the distribution of part speed and quality around the designed specification."

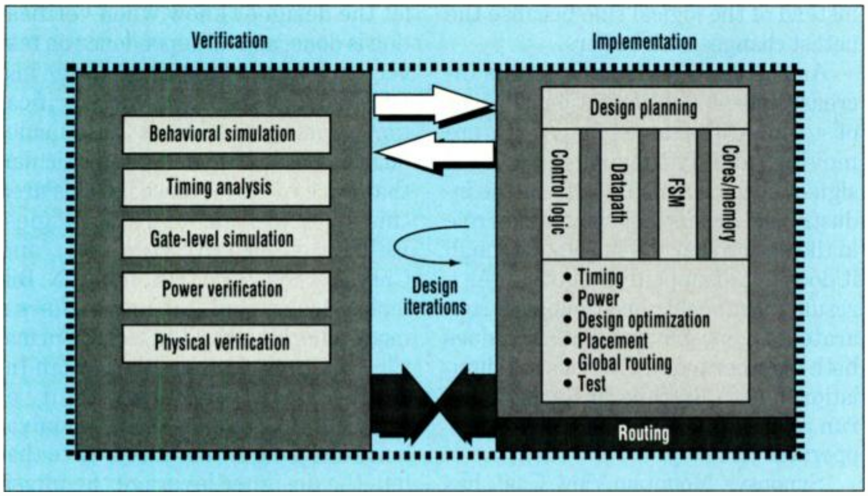
What's Needed

Identifying the verification problem is the easy part; solving it is another story altogether. What most people agree on is that the new face of verification centers on two things: complexity and performance. The Semiconductor Industry Association roadmap suggests that the way to attack the first part of the problem is by abstraction hierarchy. In the area of performance, what's needed is a way to connect the high and low levels of abstraction when trying to deal with DSM interconnect and timing issues.

It is generally accepted that the solution to the verification problem will be as complex and multifaceted as the problem itself. According to Victor Berman, vice president of strategic marketing at Denali, Palo Alto, Calif., "It will be heavily dependent on a number of factors that will define both the technical and business issues embodied in the design. These include the use of custom versus off-the-shelf components, price elasticity of targeted markets, time-to-market pressures, the importance of 'bleeding edge' performance, and features versus price and volume. Once the design parameters of the product are understood, a plan for verification may be put in place. In most real life situations, this plan will build incrementally on the experiences gained in previous designs, attacking those areas where large holes were found or where large gains can be made at reasonable cost."

Proposed Methodologies

On the traditional physical verification front, Dracula from Cadence, San



3. Viewlogic's vision of what the new verification methodology should be focuses on the combination of two key areas: verification and implementation.

Jose, Calif., has long dominated the playing field. This is changing now since the migration to a DSM design environment has brought up many issues designers did not have to deal with before. In fact, one industry observer says that this change forces us to get closer to the physics of the design, not just the physical aspects. The effect of this change is that the DSM physical verification playing field has been virtually wiped clean, leaving an opening for many EDA tool vendors to try to stake a claim.

One of the companies hoping to lay down firm roots in DSM physical verification is Mentor Graphics. Its approach is an open strategy based on a framework of databases—the FDB (filtered database) and the PDB (parasitics database)—they hope that some day will become de facto standards. With its open strategy, Mentor would then be forced to compete with other companies' tools to be plugged into this framework. An example of this would be Mentor's xCalibre parasitic extraction tool.

Mentor adopted this database approach because of its strong belief that the most important thing is not just the data, but what you do with it. Ultimately, different types of analyses, such as power grid and noise solver, are needed. But different analyses algorithms require different information from the design. With the database approach, all of the information can be collected up front. Then as the user plugs in analysis tools, the information needed for that tool is simply pulled from the database. The database ensures that the information obtained from different models of the same thing is consistent. In effect, the FDB physical database is created as if the entire circuit is going to be modeled. This is possible because of its hierarchical nature.

It's actually quite simple to understand how it works when you consider that an interconnect connects electrically within a design, but the parts reside in different pieces. FDB basically goes in and searches each net's hierarchy for the particular pieces of information it wants. It has the ability to handle large capacities since it can break up an entire design and work on, for example, a single 50-kgate piece, at a time. It then extracts the information on the 50-kgate piece. Because FDB is just looking at the electrical circuits, there is no interaction between the 50-k pieces that need to be taken into consideration. Other tools do a similar partitioning, but FDB is able to minimize the disturbance and maintain the integrity of the nets throughout the process.

Rounding out its back-end verification strategy, the company plans to introduce a static timing analysis (STA) tool that promises to eliminate many of the traditional problems often associated with STAs. These include the inability to handle high capacities, difficulty of tool use, and slow operation.

Simplex focuses its DSM verification solutions on two specific area: extraction and analysis. The reason is that in a DSM design environment, interconnect delays drive gate delays. So for electrical verification, what's needed is an interconnect-centric method as opposed to a gate/transistor-centric method. The problem is that trying to gauge C is a difficult undertaking, but you need to accurately find the coupling capacitances during the parasitic extraction process for design iterations to converge at the back end. Simplex tools are able to do this by offering multidisciplinary verification on the full chip that addresses five key areas: power, electromigration, coupling, signal integrity, and timing.

According to Shashank Goel, "The next area of verification is electrical verification matching logical behavior with mask definitions. To do this you need three different abstraction levels. But electrical verification is the key and we are only just beginning to understand it. Whoever gets the solution to electrical verification will provide the key to the puzzle."

Goel feels that it will take a number of years for layout/electrical verification to get to where DRC is today. The technology is getting there, but the issue remains getting enough inertia built up and standards developed to get the ball rolling. It also will require an understanding of how the economic model changes as you begin to use IP and verification together.

The approach to DSM physical verification by Cadence Design Systems, San Jose, Calif., is referred to as performance verification—flow-based parasitic extraction, reduction, and analysis *(Fig. 2)*. Centered around Dracula (a flat, 2-level hierarchical tool for medium and large designs), Vampire (a full hierarchical, repetitive-based tool for large designs), and Diva (an interactive, mixed-signal tool for cells, blocks, and small chips), this approach supports the company's position that accuracy is not the holy grail of DSM design. Without the context, accuracy doesn't mean very much.

The company's intent is to bridge the gap of information between process and ECAD people by pushing process information further up in the design cycle and using it to drive the design process. According to the company, end designers need a solution that will address both ends of the design process. This is required by SoC. In fact, designers will need an entire tool set to handle the overall SoC problem, which Cadence intends to offer.

The approach by Viewlogic, Fremont, Calif., is to solve the verification problem by what it calls ASIC 2000. It revolves around the idea that verification and implementation are now becoming interdependent *(Fig. 3)*. In effect, ASIC 2000 takes leading point and other tools and builds interfaces to them to give the user a push-button flow. What the company can then do is provide models using verification tools that can be used for parasitic extraction to get the accuracy it needs to drive the design flow. Then, it can take these tools and ties them back into the design process. This provides a much faster turnaround time because the accuracy is much easier to obtain. Consequently, system DSM solutions will be driven by verification-analysis tools.

Avant! Corp., Fremont, Calif., has another take on the verification problem. The way they see it, the laws of physics are the same, but the way we deal with them now have changed, because DSM design rules are changing the needs of verification. Designers depend on verification because it's the last step to get to zero defects, and if they fail, the cost associated with that failure can be devastating. With people putting their careers on the line for these verification tools, they will need to make sure the verification tools they use will work properly.

Avant! is confident that their solution will give designers this guarantee. One of its newer tools, Hercules, deals with changes in design rules and features an interface to a debug environment to make the process of debugging a chip easier. The tool uses the physical hierarchy of design for verification. As a consequence, it can eliminate the need to debug large parts of the design at once, which was the old way of debugging. Instead, the designer can debug small portions of the design at any time.

The company recognizes the need for a common database, especially at very deep submicron levels of 0.18 µm and less. As such, they're planning a common database product to be released sometime this year. Avant! also believes that the world will revolve around the physical and not the logical side of design. As such, the golden netlist now belongs to the physical side instead of the logical side because the netlist changes with buffers.

As the complexity of designs increase, gate-level simulation runs out of steam. At the same time, ASICs are moving quickly toward static level sign-off. This is a major shift for the industry and means that simulation's role in the design flow diminishes, although it does not disappear altogether. As a result, functionality and timing get separated. Event-driven simulation does both together today. Cycle-based simulation is 10 to 100 times faster, so it can run regression tests to see if the RTL operates correctly.

Synopsys, Mountain View, Calif., has traditionally focused on the event-driven simulation verification technique. Recently though, to help address timing issues, the company purchased EPIC, San Jose, Calif., which offers transistor-level tools Time Mill and Path Mill Verification. In addition, its latest tool releases, Primetime and Synopsys 97, are targeted at attacking some of the problems arising from migration to a DSM environment.

From the company's perspective, the future of simulation is functionality; hence there is a need for formal verification. The challenge is: how much verification is enough? And, now as chips are getting larger and more complex, how can you be sure that you have found every bug? The problem never goes away. Formal verification can help address this problem by telling the designer when enough is really enough. Property verification, the next generation of formal verification, is now an area of active research. It asks questions like "does my design do what I want it to do?" Synopsis interests in formal verification lie in this area.

More To The Story

While the verification problem stems from the physical design side, solutions to the problem are not limited to this design space. Future articles will seek to address such areas as hardware/software co-verification, IP, models, and code coverage in more detail.

Formal verification is one of the most talked about areas of functional verification. The main reason why is because of the limitations often associated with traditional simulation. These limitations include its inability to exhaustively verify designs, its failure to let the designer know when verification is done, and its dependence on test vectors which get extremely large in a DSM environment. Formal verification promises to address these inadequacies. Two companies, in particular, that have made advances in this area this year, are Lucent Technologies' Bell Labs, Murray Hill, N.J., and Chrysalis Symbolic Design Inc., N. Billerica, Mass. Bell Labs now offers a model checking tool known as Formal Check. Chrysalis offers the Design Insight formal verification family of tools. As the company sees it equivalence checking is the safety valve that lets the designer leverage the physical-problem change.

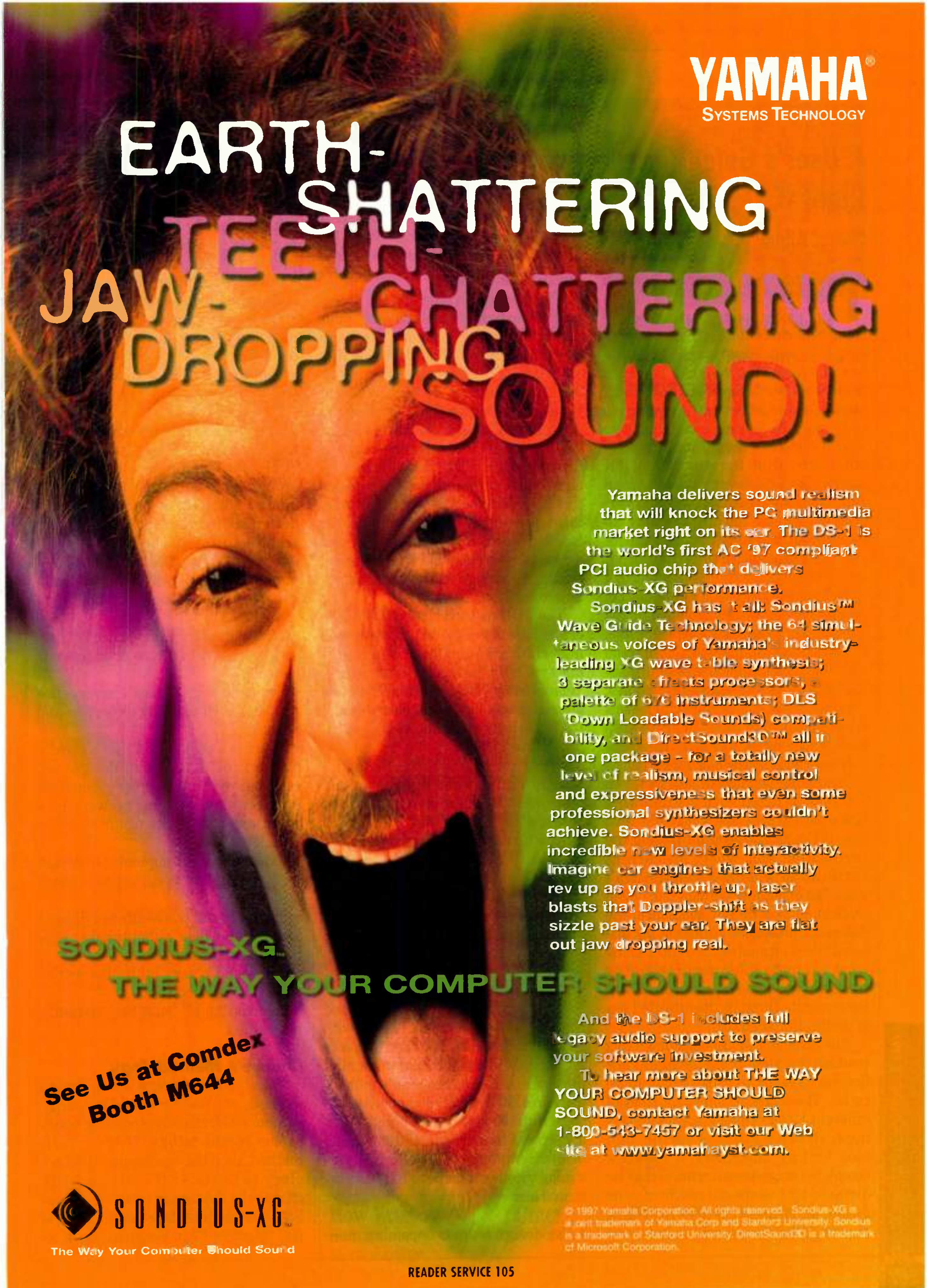
From the perspective of SoC technology, formal verification is considered to be in its infancy. For SoC technology, the amount of work such verification requires goes up exponentially with chip complexity.

Bell Labs is investigating the use of its technology in hardware/software co-verification. While its Formal Check tool can perform software verification, the company feels the next step is in learning how it may be integrated in such a way as to make it useful to potential hardware/software co-verification customers. The company also suggests that the future of the tool may involve going in the direction of behavioral-level verification and looking at how the tool targets RTL.

Chrysalis also agrees that RTL verification is a big territory, with the bulk of experimental energy being devoted here. In fact, RTL verification is seen as the wall for functional verification. It expects that solutions in this area will be available in the next few years. The company is now working on learning how to make formal functional techniques practical across a wide range of areas.

Beyond this, some industry observers suggest that further change will take place out of a need to bolt the physical and logical pieces of the design together. In any event, we must first understand the physical world to be able to drive the analyses that in turn drive the implementations.

How Valuable	Circle
Highly	576
Moderately	577
Slightly	578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READER SERVICE 105

EDA

EDA WATCH

Formal Verification Of IC Designs Is Growing Sharply As Applications Expand

Interest in formal verification has increased sharply, as a result of the challenges associated with verifying today's complex designs. Simulation is occupying an ever-increasing portion of the design cycle—anywhere from 50 to 80%. Some companies have chosen to spend large amounts of money on hardware accelerators and faster cycle-based functional simulators. This step might satisfy this year's deadlines, but it is an incomplete solution to a more fundamental, longer-term problem.

To illustrate, suppose we were trying to verify a small microcontroller, such as the Z80, by using cycle-based simulation or hardware acceleration. The Z80, by today's standards, is an ancient piece of hardware containing only 208 state bits, 13 inputs, and approximately 5000 equivalent gates. Thus, the Z80 can undergo two (208 + 13) unique possible state transitions. Even a simulator that runs at a rate of 1 trillion vectors/s would take 250 years to completely verify it, and this doesn't even include the much-greater time needed to create and check the vectors. Extrapolated relativity theory shows that the creation of the universe took a good deal less time. The fact is that it is impossible for simulation-based verification, no matter how fast, to ever catch up with the growth rate of modern microelectronics.

But, designs today are almost always verified using an inherently incomplete set of test vectors. Bugs which are missed by these vectors cause costly design iterations. Bugs often slip into the final product, which can lead to costly recall and refabrication, an embarrassing public relations problem, potentially causing stock prices to plummet.

The collective goal of formal verification is to drastically reduce design iterations, especially those that come late in the design cycle. Traditional debugging is performed in equal portions throughout the design cycle. In general, the later bugs are identified, the longer it takes, and the more costly they are to fix.

The main benefit of formal verification is to catch the bugs at the earlier RTL stages. By doing so, costly late iterations are minimized.

Today's formal verification tools do this by using several techniques: RTL design rule checking (RTL-DRC), specification (or property) checking, and equivalence checking. Each of these has its own unique set of uses and advantages.

Design Rule Checking

RTL-DRC is the method of checking RTL code for coherence against generally accepted-as-correct digital-design practices. The benefits of RTL-DRC are to quickly fix a maximum number of bugs early in the design cycle and to reduce the number of synthesis iterations. It is used prior to the first synthesis or simulation run. One of its primary advantages is that the checks it performs don't require extra work on the part of the engineer. Many companies prefer this technique because it does not force a radical design methodology shift. A few examples of bugs caught by RTL-DRC are bus contention, dead-end states (states which cannot be exited or reentered), nontoggling or single-toggling bits, infinite loops, redundant state bits or memory elements, unnecessary I/O, and variable range violations.

Specification Checking

Specification checking requires the engineer to do some extra work and also to adopt a new methodology. Its payoff is in the ability to debug RTL designs in much greater detail than possible with simulation. For instance, an engineer can write a specification which checks a bus for a potential protocol error, and the tool will report all the conditions under which it could happen. Unlike simulation, which requires the engineer to create test vectors to find the error, specification checking technologies also enable reachability analysis (is one state reachable from another), dead-code detection (finding RTL code that can never be executed), and retiming verification (relocating logic across memory elements).

A few obstacles, however, still stand in the way of widespread acceptance. Although static specifications are often reliable, sequential specifications can often be difficult or impossible to check exhaustively and they frequently have unpredictable run times. Another drawback is that engineers must fundamentally alter their thinking patterns in terms of failure conditions instead of test vectors. Finally, the user interfaces of such tools are still in their infancy.

Equivalence Checking

Equivalence checking is a technique that allows engineers to compare two designs on a functional basis. The goal of equivalence checking is to maintain functional consistency from RTL to gates, or even to full custom layout. The main advantage is that it reduces the number of late design iterations by identifying the functional inconsistencies early on.

A design undergoes many transformations before it is finally implemented. The steps may include schematic capture and/or RTL design, refinement, synthesis, tweaking, test and clock-tree insertion, place and route, or full custom layout. There is always a strong chance of introducing functional errors during each of these steps. With equivalence checking, the low-level implementation can always be compared to the original RTL model to ensure those errors don't happen. Equivalence checking has many other alternative uses such as migrating FPGA designs to ASICs, migrating designs from one ASIC library to another, and design reuse checking of gates against their RTL models.

There is now a new, strong emergence of formal verification technology, which due, in part, to customers who are discovering the inherent limits of simulation and are trying alternative methods. Product managers are improving their skills of communicating the benefits and eliminating the fear factor associated with new tools and methodologies. Most importantly, customers are becoming aware of the successful companies which already employing formal verification, such as Intel, IBM, Motorola, Texas Instruments, National Semiconductor, SGS-Thomson Microelectronics, Lucent Technologies, AMD, Sun Microsystems, Hewlett-Packard, Siemens, Toshiba, Fujitsu, NEC, and many others. But, perhaps the biggest reason for this trend is continued tool improvements and expanded applications.

The future of formal verification technology holds great promise, especially as more of the new tools are adopted into design flows. Of course, the user interfaces will continue to be simplified, an especially crucial feature for specification checkers. In general, tools will need to handle higher levels of abstraction, particularly as behavioral synthesis becomes more widespread. Equivalence checker speed and capacity improvements can be expected. Finally, algorithms that handle more complex arithmetic structures will be employed.

Perhaps one of the most exciting advances will be in integration with other tools. For instance, integration of RTL floorplanning with formal verification will yield a versatile and solid verification platform for synthesis, repartitioning, design reuse, core integration, and static-timing analysis.

Widespread acceptance of the technology is beginning to take off as the potential applications grow and begin to cross industry boundaries. Semiconductor manufactures, ASIC vendors, end users, and even systems houses are already beginning to use and see the benefits of formal verification. With simulation-based verification quickly losing its battle with design complexity, companies will be forced to embrace formal verification. Those who begin using and implementing simulation-based veritication now will be the technology leaders of the next generation.

Contributed by Pierre Bricaud, director, EP Division, Avant! Corporation, Fremont, CA. For further information, check out the company's web site at http://www.avanticorp.com.

HOW VALUABLE	CIRCLE
HIGHLY	560
MODERATELY	561
SLIGHTLY	562

EDA WATCH

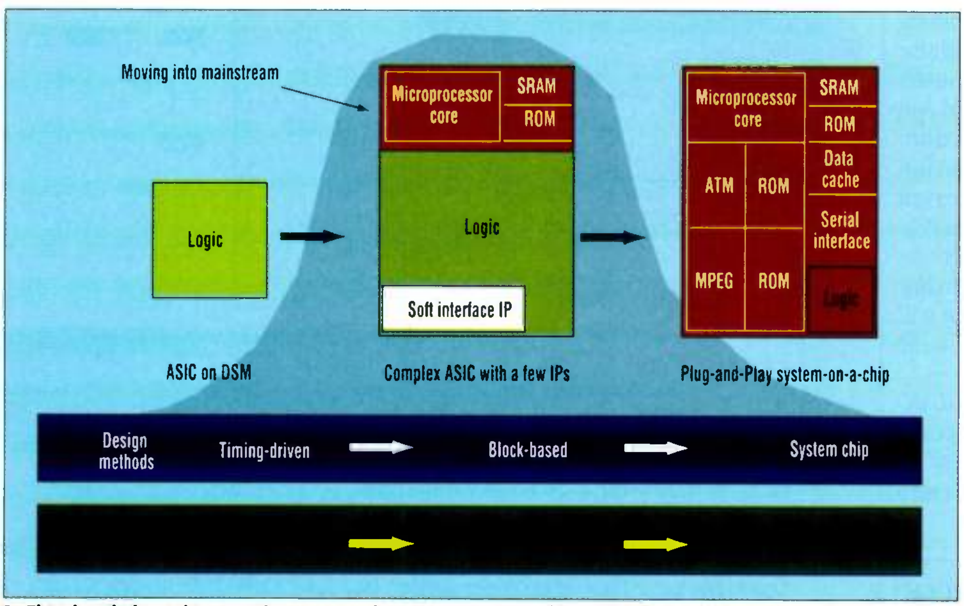
System Chip Verification: Moving From "ASIC-Out" To "System-In" Methodologies

Electronic content in consumer products is growing at an accelerated pace. These products are characterized by shorter development cycles, reduced costs, and increased product differentiation. Furthermore, silicon manufacturing capabilities are far exceeding industry expectations. For example, volume production of 0.18-µm processes are expected by the year 2000. As a result, electronic systems currently occupying multiple printed-circuit boards (pc boards) with up to 10 Mgates can be integrated into a single chip.

The processes of consumerization and siliconization are driving the requirements for "system chips" that integrate many system functions and include both hardware and software components. These system chips will be quickly realized through the integration of system-level macros or intellectual-property (IP) blocks that have been pre-designed and pre-verified in a standalone environment. The challenge that designers will face is the verification of the entire system chip along with its embedded software. To further complicate matters, many of these system chips will contain analog as well as digital blocks that must be verified together.

Design methodologies are moving from today's timing-driven flow to a "block-based" flow with macro system functions from previous designs or other sources used as building blocks *(Fig. 1)*. With the increased adoption of standards like VSI and the proliferation of "block" providers who build macro and system functions based on these standards, we should expect to see complete "plug-and-play" system chips by the turn of the century.

To meet the system-chip verification challenge, the methodology must make the transition from today's "ASIC-out" flow, where system specifications and chip implementations are defined and verified in primarily discrete, uncoupled, or loosely coupled steps, to a "system-in" flow where chips are verified within a system context. To meet the plug-and-play system-chip verification requirements, the methodology must migrate to an "interface-based" flow where the primary task is verification of the interfaces between pre-verified blocks that are being integrated for full system-chip realization.



1. This detailed graphic provides a comprehensive overview of how the design industry is broken down in terms of design methods and verification methods that are currently being used.

System-In Verification

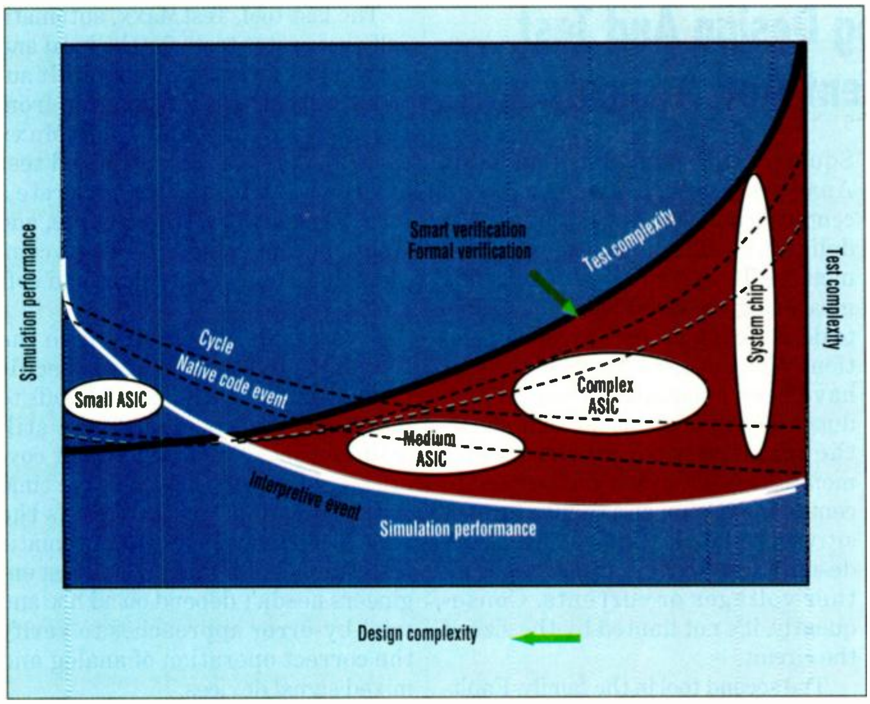
There are four major issues that must be considered when building a methodology to support a system-in verification flow process:

1. Functional and architectural level modeling should be used extensively for system function definition, verification, and architectural tradeoffs during logic block selection. Traditional ASIC design flows start directly with RTL design entry, and there is very little time spent at the functional and architectural level. The "system-in" approach involves the complete modeling of systems and their operating environment, as well as the extraction of a realistic chip test bench from the system model. To take full advantage of the work done at the functional and architectural levels, there must be a smooth flow from system-level design and verification tools to RTL and gate-level tools.

2. Simulation speed alone will not close the "verification gap." There are three variables that govern verification throughput: the complexity of the design, the size of the test bench, and the speed of the simulator. Conventional focus has been on increasing verification throughput by adding simulation speed by using native-compiled event-driven code simulators or by trading design visibility to move to a cycle-based simulator.

Even the fastest simulator that is currently available will not enable complete system-chip verification of a 10-Mgate design. Instead, we must combine the fastest simulation tools with the management of design complexity through the use of functional and architectural modeling, and the management of test-bench complexity by employing "smart verification" techniques.

3. Cycle-based simulation by itself will not be applicable to many design styles. Cycle-based simulators rely on synchronous design models and test benches in order to gain performance by only looking at data on clocked boundaries. Many logic blocks provided by third parties or through design reuse will not be fully synchro-



2. This chart specifically depicts the applicability of various system-in verification techniques that can be used in order to close the system-chip verification gap.

nous. To convert designs or test benches to run on a cycle-based simulator may require much more time than the simulation speed-up gained over event-based simulation.

The ideal solution is a flexible approach that maximizes simulation throughput using cycle simulation where possible, while enabling blocks of the design to remain in their event-based environment. In addition, many system chips will have a significant number of analog blocks integrated with digital blocks. To completely verify system-level functionality, it will be necessary to perform co-simulation between the analog and digital blocks. Again, this requires much flexibility in the simulator. This complete flexibility can be accomplished only through the use of a single-threaded simulator that integrates a cycle-based engine with an event-based engine and co-simulation with an analog simulator.

4. Smart verification is required to tame test bench growth. As system-chip designs get larger, the natural tendency of designers is to use more functional tests to verify correct operation. A larger test bench simply exacerbates the verification throughput problem. Instead, emerging techniques that either focus tests more efficiently or even remove them completely will be necessary. Code-coverage analysis is just one example of a smart verification technique. These tools will help users decide to what degree a particular function is covered (or not) and help to minimize the number of tests needed to reach desired functionality.

Taking smart verification even further are emerging formal verification tools that may eliminate certain classes of simulation completely. For example, the use of RTL to gate equivalence checks can minimize the amount of post-synthesis gate-level simulation that needs to be performed before ASIC sign-off. Designers of system chips will require a suite of these smart verification tools to minimize the number of test benches that need to be run *(Fig. 2)*.

Interface-Based Verification

The next methodology shift will occur as system chips evolve to "plug and play" systems consisting of well-defined and pre-verified hardware and software "virtual components" that communicate with each other via standardized on-chip buses. These system chips will present a host of new verification challenges that will include:

1. A greater requirement for software and hardware partitioning analysis. Similar to trade-offs made today in pc-board design, plug-and-play system-chip designers will have to decide what type of functionality to provide via hardware and what functionality can be programmed through embedded software. This will require a partitioning analysis at the architectural level with tools that are currently being researched.

2. Hardware and software co-verification. After a partitioning decision is made, verification of the system should begin, which includes the verification of embedded system software. This process carries forward from the most abstract ISS models to RTL models and perhaps even to a hardware model represented through emulation. Tools to support hardware/software co-verification from the system-level through gates will become available for widespread use over the next year.

3. More smart verification through a combination of techniques. Since the verification gap will still be significant with plug-and-play system chips, additional tools need to be provided to facilitate optimized test-bench development at the system design level as well as the carry-forward of those test benches to the RTL level.

4. The development of a user "cockpit" which will facilitate working with multiple models at different levels of abstraction. As system chips get more complex, so does the verification environment. We envision a future "cockpit" that will enable a suite of tools to be applied to models that exist in various levels of abstraction to make it easier for a user to develop and target tests, evaluate functionality, and facilitate the debugging of complex system chips.

Contributed by Glenn Abood, vice president and general manager of Logic Design and Verification Products. He is responsible for all aspects of Cadence's logic verification and synthesis products. For further details on Cadence's "System-In" and "Interface-Based" verification methodologies see the company's web site at: http://www.cadence.com.

HOW VALUABLE	CIRCLE
HIGHLY	557
MODERATELY	558
SLIGHTLY	559

PRODUCT FEATURE

Tool Suite Makes Analog Design And Test Automation More Efficient And Accurate

As design complexity intensifies, the trend toward analog/mixed signal becomes more evident. That's because certain functions just can't be described with digital design techniques. The only problem is that while a whole slew of digital design and test automation tools are available, the same can't be said for analog and mixed-signal designs. In fact, analog design has traditionally been done by a select few experts. And even then, they were forced to rely on make-shift design methodologies and test techniques they threw together themselves. But as analog design begins to make its way to the ASIC mainstream, this scenario must change.

Now Opmaxx has developed a family of tools that speaks directly to the problem of what the company refers to as analog design and test automation (ADTA). The tools—FaultMaxx, DesignMaxx, and TestMaxx—work by generating useful test and design results, making it possible for designers to accurately and efficiently analyze and test analog circuitry.

The family of tools don't function as a circuit simulator. Rather, they fit into traditional analog design and test environments, making use of existing simulators and manipulating the associated input/output files. More specifically, the tools allow for dc, ac, and transient sensitivity computation, generation of fault test vectors for soft and hard faults, fault computation, and design evaluation.

The first tool, DesignMaxx, based on the use of proprietary algorithms that perform Monte Carlo, Root Sum Square (RSS), and Extreme Value Analysis (EVA), provides a design centering and analysis capability that delivers results in as little as a few minutes. It accomplishes this task by measuring the sensitivity of a design to dc, ac, and transient circuit simulation. When at least two simulations have been completed, the tool produces a graphical output that shows the sensitivity for all circuit elements. This data then can be used to center the design and reduce its sensitivity to fabrication variations. A design's sensitivity is measured as either voltages or currents. Consequently, it's not limited by the size of the circuit.

The second tool in the family, FaultMaxx, enables fault modeling and computation of analog circuits. It combines the results of the DesignMaxx sensitivity analysis with design layout data and schematic connectivity. Utilizing a systematic partition approach, it automatically partitions faults into two categories—hard or soft. To calculate the hard faults, such as an open or a short, the tool employs a gradient technique to measure the effect as a voltage or current.

For the soft faults, each element in the analog circuit is compared to different scenarios that measure the element's relative fault-free deviation in relationship to its relative faulty deviation. Once the process of fault identification is completed through, the results are brought together into a single fault dictionary that can be employed by the designer to build a test strategy.

The last tool, TestMaxx, automatically generates tests for the hard and soft faults of the analog circuit. It automatically takes information from the DesignMaxx and FaultMaxx tools and creates an optimized test environment. It's able to generate a structured set of tests for ac, dc, and transient conditions, including a complete detection of both hard and soft faults.

As a result, designers have the flexibility to create design specific test strategies and make trade-offs to meet cost requirements, yet still maintain specifications for fault coverage. Moreover, they can save time in test development as well as the length of time it takes for automatic test equipment testing. Thus, test engineers needn't depend on ad hoc and trial-by-error approaches to verify the correct operation of analog and mixed signal devices.

The Opmaxx family of tools are ideal for product development of analog electronic devices used in various applications ranging from automotive, consumer electronics, and computer, to wireless products. All three tools, available now, run on Sun, HP, or NT workstations. They currently provide support for the HSPICE simulator, with planned support for SPICE3, Spectre, and Saber.

The DesignMaxx, FaultMaxx, and TestMaxx tools may be purchased individually for $70,000, $25,000, and $60,000, respectively, or as a package for $135,000.

Opmaxx Inc.
8209 S.W. Cirrus Dr.
Beaverton, OR 97008
(503) 520-9200
http://www.opmaxx.com
CIRCLE 503
CHERYL AJLUNI

Board- And System-Level Design Environment Enables Modeling, Reuse

Higher-speed, higher-complexity designs are challenging current design methodologies. Today it's no longer sufficient to simply analyze designs on an individual component basis; there are just too many. The interaction between components plays a much more significant role than in the past, especially if the components are different architectural blocks of IP (intellectual property).

To help meet the needs of board- and system-level designers in this complex design space, Omniview has developed a design modeling and synthesis tool, Galaxy, that can model system-level designs at the architectural level using standard component models. The first in a series of future system-level design reuse and synthesis tools, Galaxy offers designers a complete design environment for full-board and -system synthesis, and is an enabler or virtual prototyping. The tool consists of the company's Fidelity synthesis engine, a robust suite of component design libraries, development tools for user-defined cus-

(continued on page 209)

(continued from page 208)
tomized libraries, and an interface to leading EDA design environments.

Galaxy, which allows designers access to a variety of functions (static timing verification, multiple processor and bus structure impact performance analysis, memory sizing, and co-simulation with behavioral VHDL models to validate detailed designs), also offers a number of significant benefits.

For example, the tool lets designers capture and save, either in part or in whole, designs for later use. And, with the Fidelity synthesis engine, hardware engineers and system architects can use the traditional ASIC synthesis methodology for board- and system- design—a function that previously wasn't automated with electronic-design-automation (EDA) tools.

Galaxy also boasts the ability to run multiple hardware design options against a single software option and vice versa. In addition, with its intuitive, easy-to-use GUI (graphical user interface), designers can actually learn and begin to use the tool in a matter of hours.

At the core of the Galaxy tool lies a configuration system and a series of constraint-based reasoning algorithms. These permit the synthesis of highly complex designs using a library of components organized as a functional hierarchy. The tool starts from a high-level description of the board or system design, such as a block diagram. Then after refinement of the abstract block diagram, it automates component selection, timing analysis, and schematic generation.

At this stage, the designer can input various design parameters, such as cost, size, weight, and process technology. Galaxy uses this information to select components and run a static timing analysis. Because the Galaxy tool links to other design environments, such as Mentor Graphics Design Architect and Design Viewpoint Editor, compatible schematics and design viewpoints can be generated by Galaxy that interface with simulation, layout, and a number of other downstream tools.

During operation, Galaxy functions in either a what-if or optimization mode. In the what-if mode, the tool stops when it finds a design that meets the designer's specifications or suggests changes that need to be made in order for the design to meet the specifications. When in the optimization mode, the tool builds all of the designs that are possible and ranks them based on the designer's preferences. The designer then simply selects the most optimal design for implementation.

For designers interested in hardware/software partitioning, Galaxy interfaces to the company's Cosmos tool. With this link, designers can use Cosmos to create high-level block diagrams at the architectural level and evaluate performance; effectively conducting hardware/software tradeoffs at the architectural level. The block diagrams then can be input into the Galaxy tool to allow for a top-down design flow at the board and system level.

The Galaxy tool comes equipped with a standard design library that features hundreds of component families and models. A library-management tool and a synthesis debugger round out the product offering. For designers who wish to create their own models for custom components or components not in the standard library, a library builder tool also is provided. As a result, designers can import data from existing materials-resource-planning (MRP) databases to keep their libraries current.

The Galaxy tool currently accepts VHDL, with Verilog support planned for a future release. Now available, it runs on Sun SPARC and HP 9000 Workstations. Galaxy sells for $60,000 per license and includes the Fidelity engine, the library, and the debugger. Update service to the tool is available via the web.

Omniview
901 Mariner's Island Blvd.
Suite 575
San Mateo, CA 94404
(415) 286-9458
http://www.omnivw.com
CIRCLE 504

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Circle 520

Quick And Practical Design Of A High-Pass Third-Order Bessel Filter

THEODORE KARATZAS
Honeywell-Kostas Karayannis S.A., 58, Kapodistriou Str., GR142 35 Nea Ionia, Athens, Greece; phone: 68 00 460 - 4; fax: 68 53 522.

In the design of a proximity switch using PIN diodes as the receiving element, the signal is first amplified and then must be filtered from any noise before proceeding to the several signal-conditioning stages of the proximity switch. Typically, to reject any noise resulting from 50-Hz supplies, neon lamp frequencies, 100 Hz harmonics, and any other anticipated sources of noise, a unity-gain third-order Bessel filter is a good choice for giving a flat response without damping at the corner frequency (this doesn't happen with Butterworth or Chebyshev filters).

The filter shown provides a zero response at dc and a flat response from corner frequency f_{cp}, up to f_u *(Fig. 1)*. The f_u frequency is where A_{vc} gain crosses unity *(Fig. 2)*.

The filter is a high-pass type only for the region between f_{cp} and f_u. In practice, f_u varies with temperature and the filter will be subjected to more error drift near f_u.

The following procedure, which uses equally sized capacitors, enables the selection and calculation of the wider range of resistors that are available as opposed to capacitors:

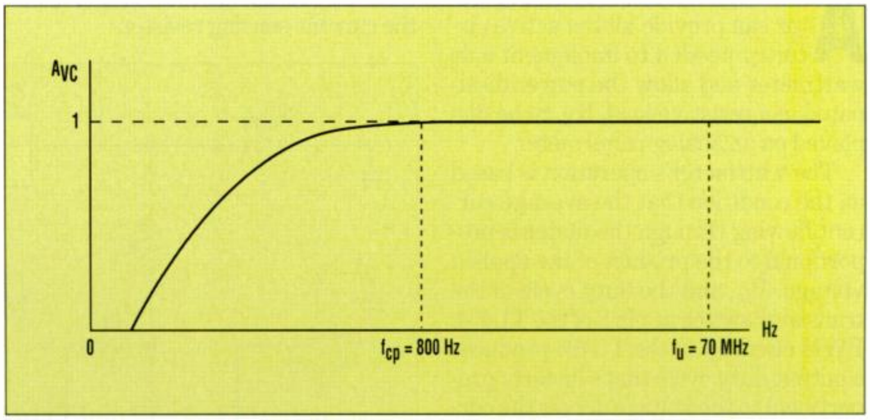
1. Estimate which frequencies are to be rejected and determine the corner frequency f_{cp}.
2. Select an op amp with a range of frequencies in which the open-loop gain $A_{vlo} \geq 100$. This value must be maintained from dc up to the unity-gain frequency f_u, in order to keep the actual frequency response with 0.1 dB of the theoretical response.
3. Select a value for the three equally sized capacitors C1 = C2 = C3.
4. From the chosen corner frequency, calculate the capacitors initial value C'.

$$C' = \frac{1}{2\pi f_{cp}} \qquad \text{Eq. 1}$$

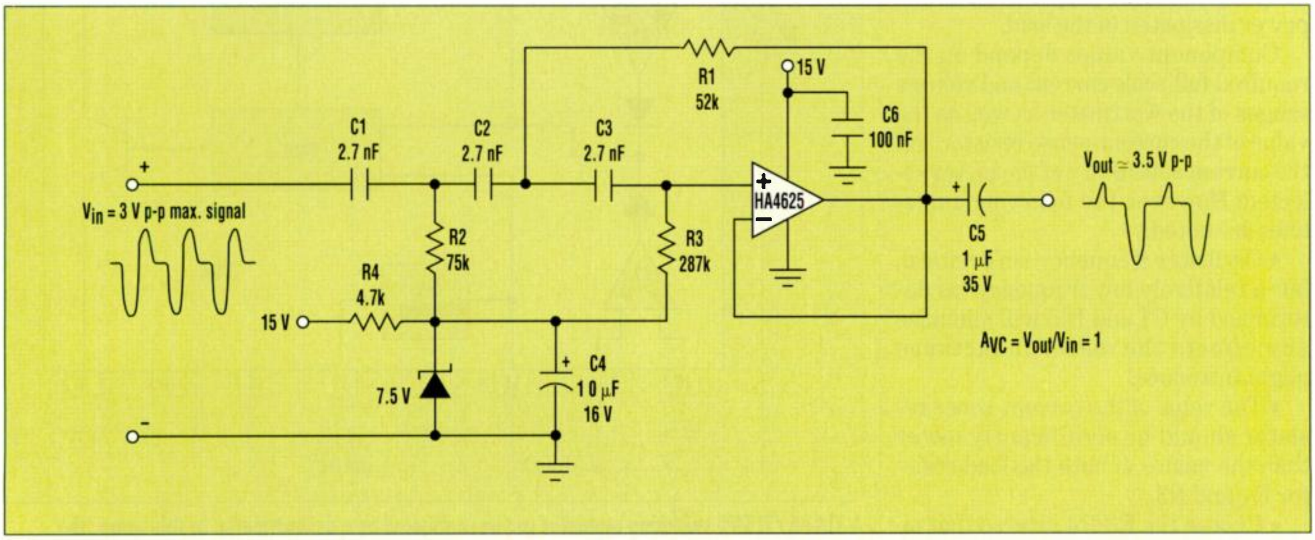
5. For equally sized capacitors, calculate the scaling factor K.

$$K = \frac{C'}{C1} = \frac{C'}{C2} = \frac{C'}{C3} \qquad \text{Eq. 2}$$

6. Calculate the three final resistor values according to: R1 = KR1'; R2 = KR2'; R3 = KR3', where R1' = 0.7027;



2. Given is the high-pass Bessel filter frequency response from DC to 70 MHz, using a corner frequency f_{cp} = 800 Hz and incorporating the HA-4625 high-speed op amp.



1. Unlike Butterworth or Chebyshev filters, this third-order Bessel filter exhibits no overshoot or overdamping at the corner frequency, f_{cp}.

R2' = 1.012; and R3' = 3.940 are the initial resistor values for a high-pass Bessel filter.

The following is an example set up for a PIN diode signal as the input to the filter:

1. The value of the required corner frequency is: f_{cp} = 800 Hz.

2. An HA-4625 op amp, with A_{vlo} = 200, from dc up to 70 MHz is selected.

3. For the three equally sized capacitors, 2.7-nF, 1% film is selected.

4. From the above f_{cp}, the initial value of capacitors, C' is calculated:

$$C' = \frac{1}{2\pi f_{cp}} =$$

$$\frac{1}{6.28 \times 800} = 200 \ \mu F \qquad \text{Eq. 3}$$

5. The scaling factor K is then calculated:

$$K = \frac{C'}{C1} = \frac{C'}{C2} = \frac{C'}{C3},$$

$$K = \frac{200 \times 10^{-6}}{2.7 \times 10^{-9}} = 74 \times 10^{3} \qquad \text{Eq. 4}$$

6. The final resistor values are calculated, according to the high-pass Bessel filter initial values: R1', R2', R3:

R1 = KR1' = 52k
R2 = KR2' = 75k
R3 = KR3' = 287k

Circle 521

Wattmeter Employs Switching-Regulator IC

FRED FRANKE
Cursor Control Corp., P.O. Box 808, Kings Park, NY 11754; (516) 265-4971.

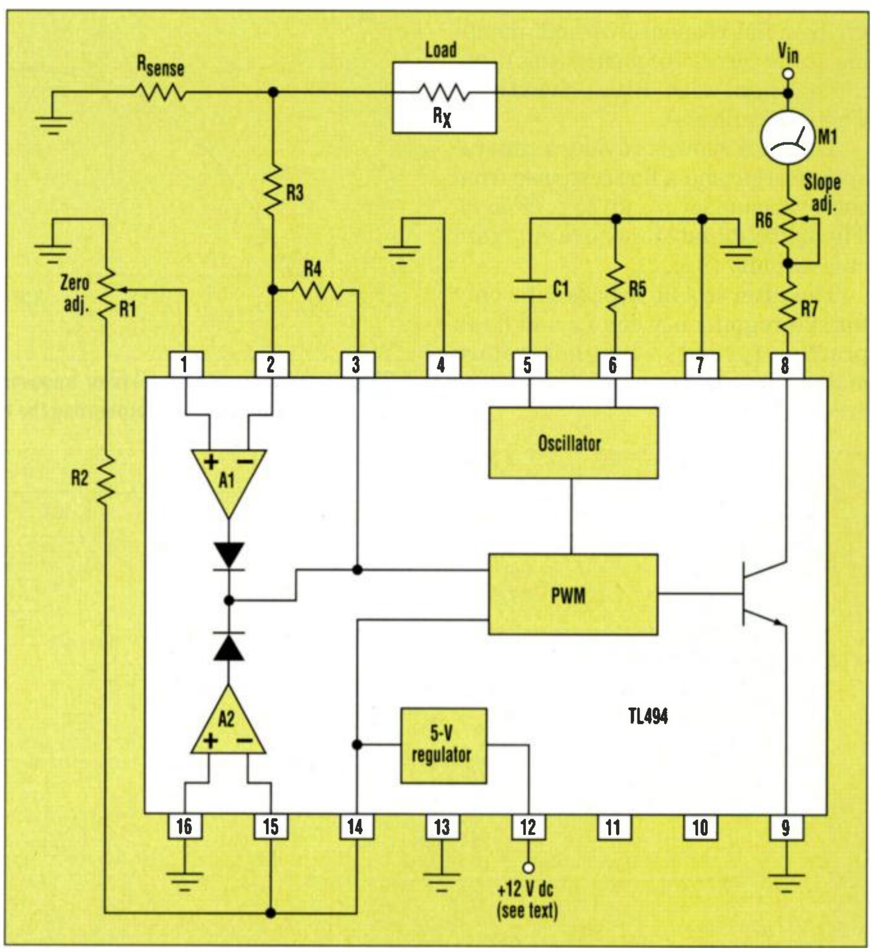
An inexpensive switching regulator can provide all the active circuitry needed to implement a dc wattmeter and allow the power dissipated in a resistive load, R_X, to be displayed on an analog panel meter.

The wattmeter's operation is based on the condition that the average current flowing through the meter is proportional to the product of the applied voltage, V_{in}, and the duty cycle of the transistor switch at pin 8 of the TL494. PWM circuitry in the TL494 produces a output duty cycle that's linearly proportional to the voltage across the current-sensing resistor R_{sense}. The average current passing through the meter is therefore proportional to the power dissipated in the load.

Component values depend on the required full-scale current and voltage ranges of the wattmeter as well as the value of the current-sense resistor and the current sensitivity of the meter selected. However, the following guidelines are noted:

- Oscillator frequency isn't critical, but a relatively low frequency (as determined by C1 and R5) will minimize any effects the meter inductance might introduce.
- The value of the current-sense resistor should be significantly lower than the values of both the load resistor R_X and R3.
- Choose the R3/R4 ratio so that op amp A1 produces a swing of just less than 3 V for the full-scale swing across the current-sensing resistor.
- Adjust R1 for 0% duty cycle with zero current flowing through R_{sense}.
- Select R6 and R7 to produce rated full-scale meter current based on an 85% duty cycle at maximum applied voltage V_{in}.

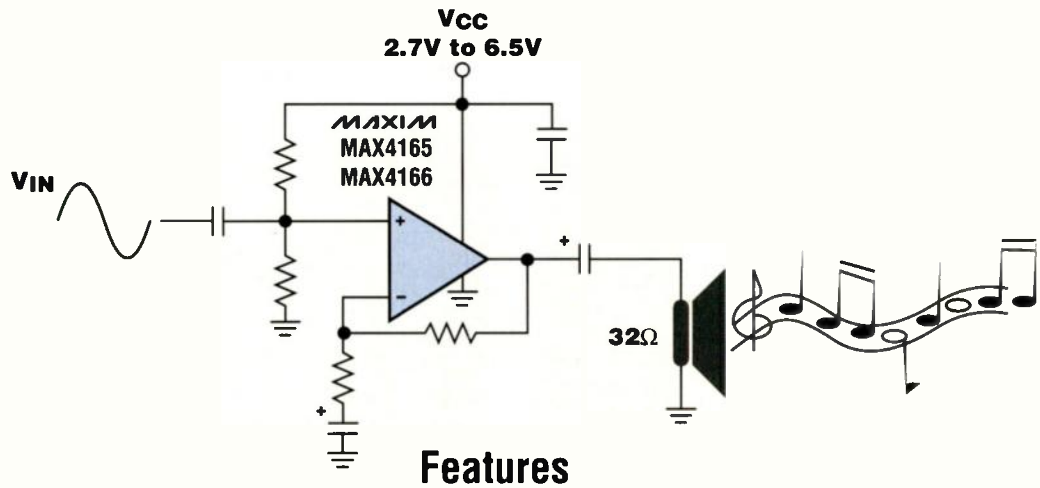
Applied voltage (V_{in}) should be limited to 40 V due to the voltage rating of the TL494. If the range of interest of V_{in} is never less than 10 V or so, pin 12 of the TL494 may be directly connected to V_{in}, resulting in a self-powered wattmeter.



A TL494/TL594 switching regulator can be configured as a dc wattmeter. In this setup, the power dissipated in a resistive load is displayed on an analog panel meter.

SOT23 OP AMPS GUARANTEE 80mA OUTPUT DRIVE

5MHz Gain Bandwidth with Operation Down to 2.7V



Features

- High, 80mA Output Drive
- 5MHz Gain Bandwidth
- 38μA Low-Power Shutdown
- Operates Down to 2.7V
- Available in SOT23 Package
- Rail-to-Rail® I/O

Maxim's new family of low-power, precision rail-to-rail I/O op amps is ideal for any portable, high-drive system. Applications include hands-free car-phone kits, cell phones, portable headphone/speaker drivers, and audio amplification for computers, sound ports, and set-top boxes.

Choose Maxim for the Best Low-Power, Single-Supply Rail-to-Rail I/O Amplifiers

PART	NO. OF AMPS	GBW (MHz)	OUTPUT DRIVE CAPABILITY (mA, min)	SUPPLY CURRENT PER AMPLIFIER (mA, max)	SUPPLY VOLTAGE RANGE (V)	INPUT OFFSET VOLTAGE (mV, max)	SHUTDOWN	PACKAGES
MAX4165	1	5	±80	1.4	+2.7 to +6.5	±1.5	No	5-pin SOT23
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MAX4167	2	5	±80	1.4	+2.7 to +6.5	±0.85	No	8-pin SO/DIP
MAX4168	2	5	±80	1.4	+2.7 to +6.5	±0.85	Yes	10-pin μMAX, 14-pin SO/DIP
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Circle 522

Wide-Band Analog White-Noise Generator

ALFREDO GALLERANI
Istituto di Radioastronomia del C.N.R., Via P. Gobetti 101, 40129 Bologna, Italy.

Commercially available white-noise generators are rather expensive. The circuit presented here, however, is an inexpensive version that produces frequencies up to about 300 MHz. Its operation is based on the noise generated by the Zener breakdown phenomenon in the BJT inversely polarized base-collector junction. In other words, such shot noise involves the statistical fluctuations of the current flow present in the bipolar transistor.

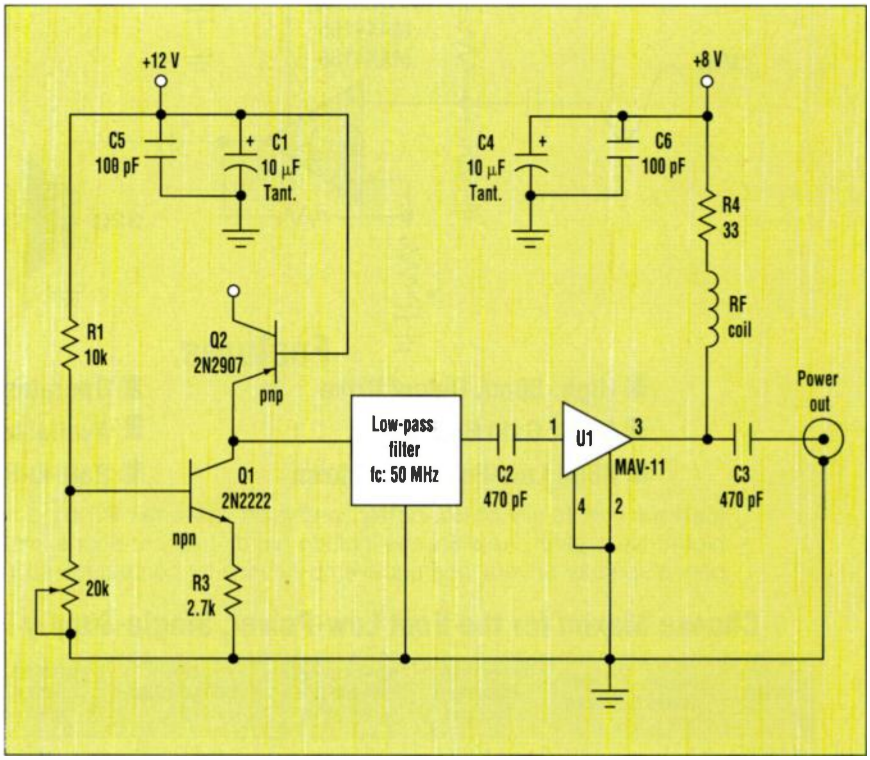
The generator shown makes use of a common 2N2907 biased by the constant current source supplied by a 2N2222 *(Fig. 1)*. To increase the amount of shot noise attainable, the collector of the 2N2907 is left open and the base-emitter is reverse-biased. That is, the BJT is connected as a Zener diode to exploit the reverse breakdown phenomenon.

With this configuration, the reverse breakdown voltage exhibited by the emitter-base junction can be easily observed using an ordinary spectrum analyzer. The attainable bandwidth is about 300 MHz, and the power output is about –70 dBm.

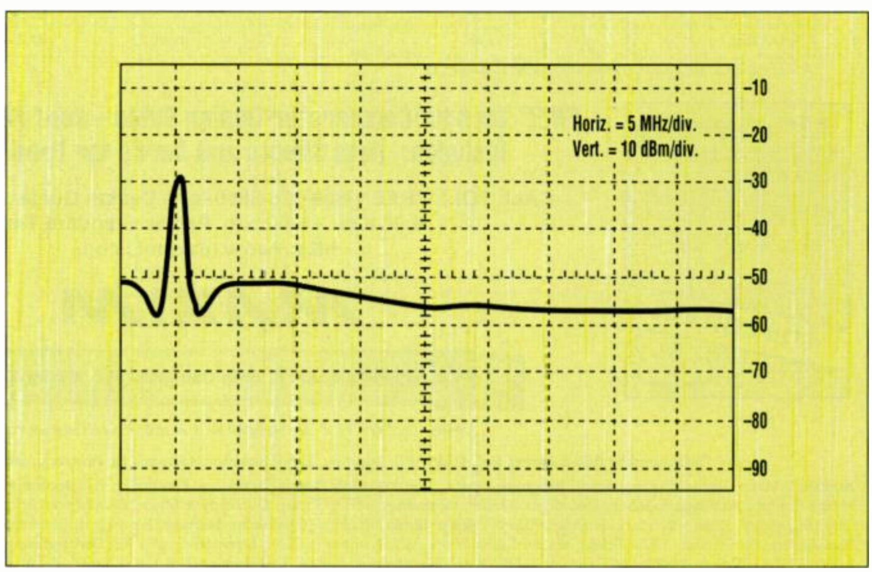
To increase the noise power, one or more amplifiers, such as the monolithic MAV-11 from Mini-Circuits, can be added. The 50-MHz low-pass filter (the PLP-50 from Mini-Circuits) inserted between the generator and the first MAV-11 is necessary to maintain the amplifier output power compression at an acceptable value. But, of course, with this configuration, the bandwidth is restricted to the 0-50 MHz range, i.e., the power spectrum vanishes outside the cutoff frequency of the filter.

In Figure 1, R4 is needed to limit the current delivered to the amplifier. L1 provides high impedance to isolate the dc source from the RF signal. C3 removes any dc content from the output of the generator. The 20k trimmer connected between the base and ground in Figure 1 permits a wide range of the attainable output noise up to –60 dBm *(Fig. 2)*.

At the Istituto di Radioastronomia del C.N.R., this circuit is currently being used to simulate cosmic white noise, in which the radioastronomical signal (a coherent white noise) to be extracted is buried.



1. This white-noise generator bases its operation on the noise generated by the Zener breakdown of Q2 and is a capable of delivering a constant -60 dBm in a 0-50 MHz bandwidth.



2. Shown is the response measurement obtained using an AIL/TECH spectrum analyzer.

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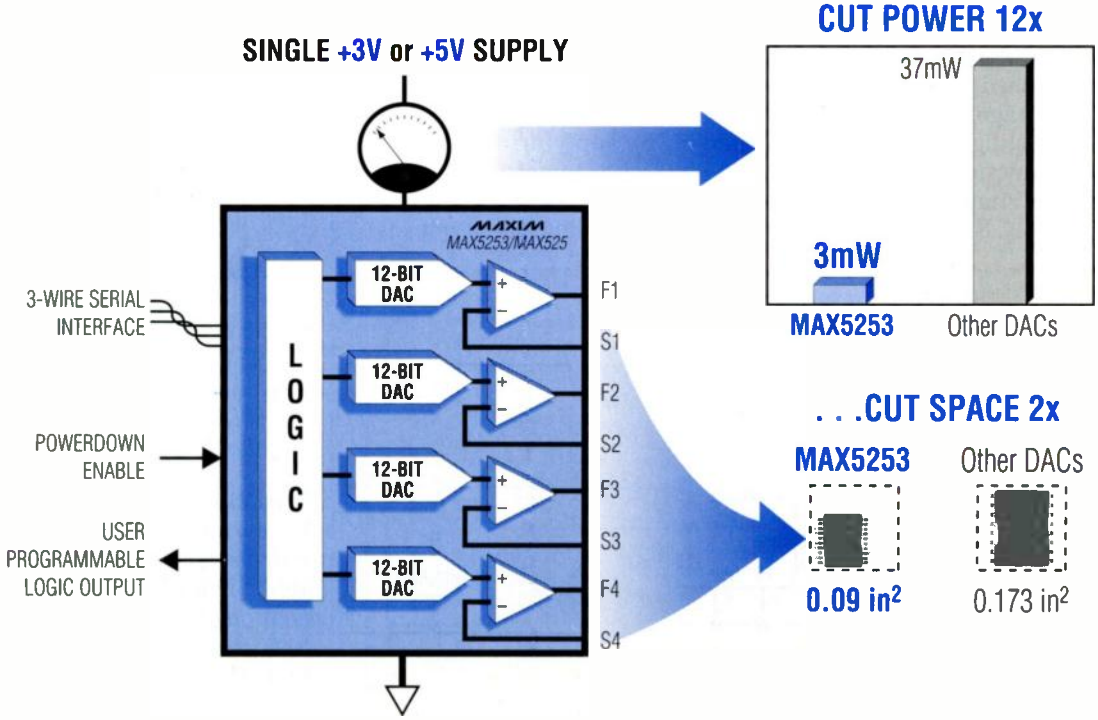

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Circle 523

Power Supply Write-Protects SmartVoltage Memories

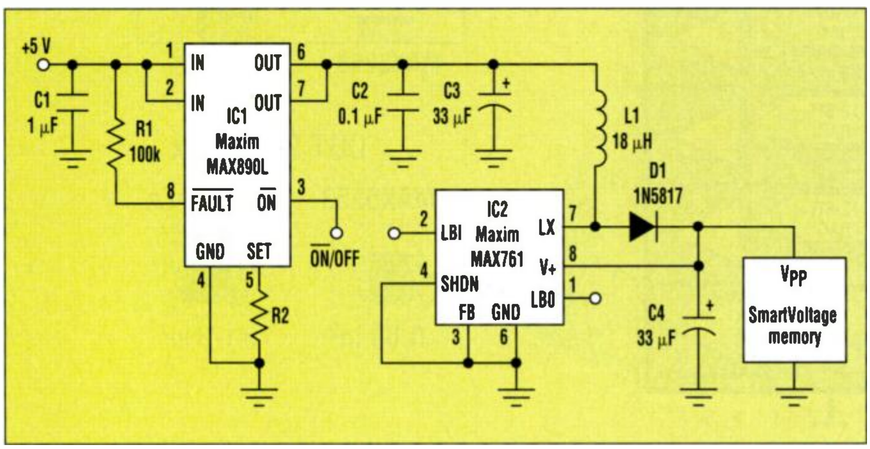
ROGER KENYON

Maxim Integrated Products, 120 San Gabriel Dr., Sunnyvale, CA 94086; (408) 737-7600.

Second-generation FlashFile memory devices developed by Intel, which employ the company's SmartVoltage technology, can operate with a 5-V V_{pp} supply in addition to the established 12 V V_{pp}. This dual-operating voltage causes a problem in write-protecting the memory.

One write-protection method for flash memories is simply to turn off the 12-V V_{pp} supply. Since most systems derive this supply from 5 V using a boost converter, turning off the converter only lowers the supply to 5 V minus a diode drop—not 0 V. Such protection was effective for the earlier 12-V-only flash memories, but not for the SmartVoltage memory with its 5-V operating capability.

The circuit shown solves this problem. IC2 is a step-up dc-dc converter that boosts 5 V to 12 V, and IC1 is a high-side switch that serves as a power switch and current limiter *(see the figure)*. Therfore, when IC1 is turned off by applying a TTL-logic "1" to pin 3, the memory supply V_{pp} goes to 0 V. IC1 limits the current (between its IN and OUT terminals) according to the value $R2 = 1240/I_{limit}$, where R2 is in ohms and I_{limit} is in amperes (with a maximum of 1 A). A value of 1.5 kΩ, for example, will set the limit near 1 A. If lower peak-load currents are needed, the R2 value should be higher.



This circuit properly write-protects the Intel SmartVoltage flash memory by ensuring that its V_{pp} will be lowered to 0 V. First generation protection circuits typically drop only to 5V.

VOTE!

Read through the Ideas for Design in this issue. Then select your favorite, and circle the appropriate number on the Reader Service Card. The winner will receive a $300 Best-of-Issue award.

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IFD WINNERS

David A. Johnson, 10198 West Berry Dr., Litleton, CO 80127-1856; (303) 973-8408. The idea: *"35mm Film Makes Low-Cost IR Filter"*, December 2,1996 Issue.

Frank T. Koide, University of Hawaii, Dept. of Electrical Engineering, 2540 Dole St., Honolulu, HI 96822. The idea: *"Quick Estimate of Signal Bandwidth"*, December 16, 1996 Issue.

W. Stephen Woodward, CB3290, University of North Carolina, Chapel Hill, NC 27599-3290; email: woodward@net.chem.unc.edu. The idea: *"RTD To RS-232 Interface"*, January 6, 1997 Issue.

S. J. Prasad, National Semiconductor Corp., MS A1-555, 2900 Semiconductor Dr., Santa Clara, CA 95052-8090; (408) 721-7178. The idea: *"Single Pot Swings Amplifier Gain Positive Or Negative"*, January 20, 1997 Issue.

David Albean, Thomson Consumer Electronics, P.O. Box 6139, Indianapolis, IN 46206; (317) 587-4950. The idea: *"SCA Receiver Demodulates Addi-tional Subcarriers"*, February 3, 1997 Issue.

W. Stephen Woodward, CB3290, University of North Carolina, Chapel Hill, North Carolina 27599-3290; email: woodward @net.chem.unc.edu. The idea: *"Optically-Isolated Amplifier Has Super-Stable Zero"*, February 17, 1997 Issue.

W. Stephen Woodward, CB3290, University of North Carolina, Chapel Hill, North Carolina 27599-3290; email: woodward @net.chem.unc.edu. The idea: *"RS-232 Stepper Control Exhibits Versatility"*, March 3, 1997 Issue.

Tim R. Bengston, Rose Electronics, 1991 Concourse Dr., San Jose, CA 95131; (408) 943-0200. The idea: *"Constant Power Load Needs Only a Few Parts"*, March 17, 1997 Issue.

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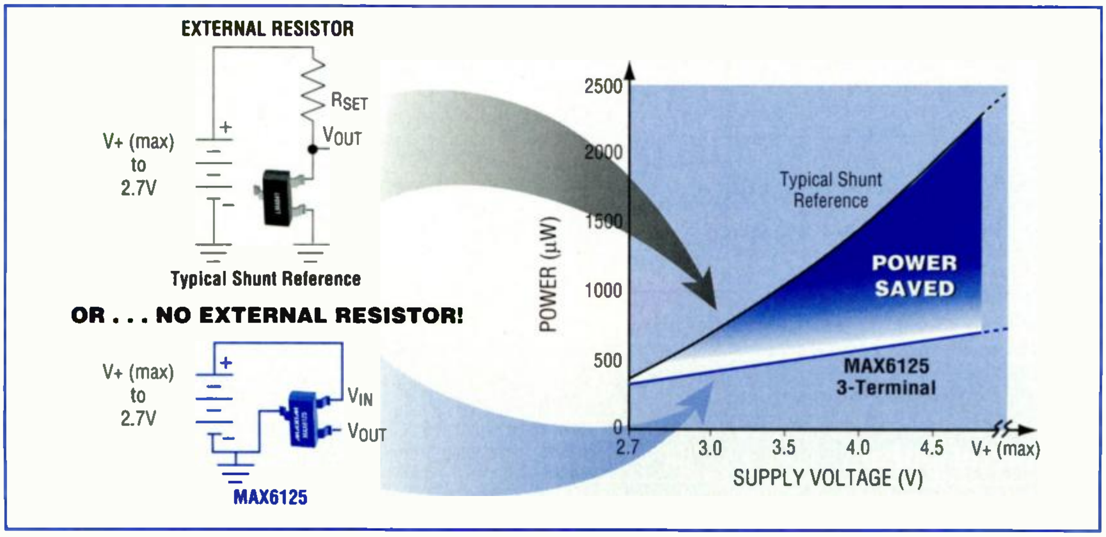

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MAX6145	4.5	79	50	4.7	3-pin SOT23
MAX6150	5.0	80	50	5.2	3-pin SOT23
MAX6160	Adj. (1.23 to 12.4)	75	50	2.7	4-pin SOT143
MAX6520	1.2	50	50	2.4	3-pin SOT23

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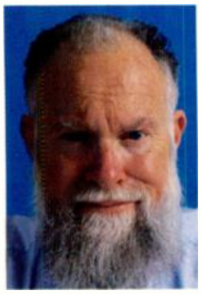
BOB PEASE

What's All This Aptitude Stuff, Anyhow?

Once upon a time there was a very smart guy—let's call him Bob—who was getting lousy grades. *(This is another esaeP's Fable.)* He was in danger of flunking out of MIT, even though he had a very high IQ. His father sent him to the Human Engineering Lab (which I'll abbreviate as HEL) in Boston, to take a set of Aptitude Tests. When all the results were known, Bob took the report and went in to see the Dean of Students (who had been wanting to have a talk with him). Bob showed him the results—high scores in many aptitudes. The Dean went over to a file cabinet, unlocked it, and solemnly brought out—a goldfish bowl. It was stuffed full of dollar bills. He told the young man, "Bob, put your dollar in, too. Each of the dollars in here was put in by a person with 'too many aptitudes.' If and when you graduate, you win all the money in the bowl. But I must caution you that the reason the bowl is so full is because 'too-many-aptitude persons' do not find it easy to graduate. They get distracted too easily on too many subjects." *(End of Fable.)*



BOB PEASE OBTAINED A BSEE FROM MIT IN 1961 AND IS STAFF SCIENTIST AT NATIONAL SEMICONDUCTOR CORP., SANTA CLARA, CALIF.

Did the goldfish bowl of money ever get claimed by a graduate? Did the Dean of Students at MIT ever actually do that? Did the Dean of Students ANYWHERE actually set up such a challenge? Maybe—maybe not.

Maybe the whole story is apocryphal. But there is an element of truth about this. The first thing I must explain is that the young student "Bob" was not RAP. I never went to see the Dean of Students at MIT. I never took the HEL tests nor got my test results until 5 months after I graduated. I have never *seen* a goldfish bowl full of dollar bills. But I certainly can imagine one.

When I went to MIT, I was good at taking tests. Of all the guys I knew in my high school, I was about the best at taking tests. We had a math teacher, Pappy Mirtz, who explained at the beginning of the term, "This term we are not having any un-announced tests." Most of the class cheered. He grinned, wryly, "I am announcing them all, *now*." The class groaned. But the teachers who gave a little test every day did get a lot of respect, and they were generally very good teachers.

When I started taking tests at MIT, I figured out that the *cream* of 500 other schools—most of whom were the best test-takers in *their* schools—were all taking tests, and they were having problems. The first test I took in Physics 8.01 was very simple. I remember it perfectly: A small mass (m) comes along at velocity (v) and smacks into a larger mass (2m) at rest, and bounces back. Allowing for the conservation of momentum and of energy, what are the resulting speeds? I started out to do the test. I struggled, and realized I could not get the equations to work right. I figured out what the answer was, and crunched the equations together backwards until they gave the right answers—just in time to hand in the paper. (The answer is that the small mass bounces back with velocity = −1/3 v and the larger mass moves forward at 2/3 v. No momentum or energy is lost.)

When we sat around before the next class, some guys were discussing what they thought the class average would be. Some guys guessed 70 or 80 or 85. When the papers were returned, the class average was announced—50. Obviously, a lot of other kids had some troubles, too. More than I did.

Like I said before, I was always pretty good at taking tests. I figured out the right way to take them. We had 3-hour finals in our courses. For example, I went in well-prepared for the 5.02 final in the spring of 1958—General Chemistry. In the first hour, I did all the problems the best I could. I recognized that the test-makers were (as usual) putting in a lot of extraneous information and useless, distracting facts. In the second hour, I brought out a glass and a quart of Hampden Ale, and drank it. Meanwhile, I checked all my answers for dumb errors, as well as I could. At the end of the second hour, I packed up my stuff and handed in my exam and walked out. I figured I certainly couldn't improve my test results in the third hour by hanging around, but I might panic a poor few souls and improve my score compared to the class average. I did pass that exam. Not sure what I got; probably a B− or a C+, which was FAR above average on those tough chemistry exams. Hey, I knew how to drive a slide rule. Still do.

In the fall of my senior year, I was taking a course (8.721) in Advanced Physics. I won't say much about the poorly taught course (which was, many of us believed, designed to flunk out 1/2 of the senior class). But they gave us some homework problems. I didn't do them. I thought I knew how to do them. Then they showed us last year's final exam. It had the same problems. I didn't do the "practice exam." Then they showed us the *previous* year's exam. It had the same problems. I didn't do them. Previous year's homework, likewise.

When I went into the final—guess what problems were there. The same darned problems. I had to do them, so I did them. I passed the course. But they did manage to flunk half of the senior class. Meanwhile, I had decided that all this quantum-mechanical stuff was not very *physical*, so I bailed out and got into Electrical Engineering. Even as I was planning to survive that 8.721 class and its final, I was taking a couple of labs in Course VI (Electrical

BOB PEASE

Engineering) plus a couple of theoretical courses—and having FUN! So that is why I got my B.S. in EE, not in Physics. And I graduated in September of 1961, not in June, because I was taking so many courses in EE, that I couldn't start my thesis until June.

After I graduated, I went to work for Philbrick Researches. I was doing technical writing, and studying the design of op amps (with vacuum tubes, and germaniums, and silicon transistors, too). I learned from some pretty good engineers, too; Bob Malter, Tim Noble, George Philbrick, Bruce Seddon, and Al Pearlman. I learned some marketing angles from George and from Dan Sheingold. I saw some true MASTERS at work. I was having a LOT of fun!

Now, it is a fact that 5 months after I graduated, I went in to the Human Engineering Lab for some testing, because I was having so much fun. Why did I go in? Not sure. I guess a friend recommended it.

What did I learn? That I had good aptitudes at a LOT of things. Let me explain the Wiggly Block test: if you take a big block of wood, and use a jigsaw to cut it into several curvy pieces in the X dimension, and then *again* in the Y dimension, you get a group of blocks that are curvy, and they all fit together if you fit them wisely. A 4-by-5 matrix of 20 blocks. Assembling this puzzle from randomly turned and jumbled pieces is one of the standard old tests for engineering aptitudes at the HEL. They call this "Structural Visualization." Most engineers are very good at this test. Surgeons are. English majors ain't. The *absence* of Structural Visualization is called Abstract Visualization, and English majors usually have *this*. I did very well at assembling this Wiggly Block quickly. Heck, I could even do it with my eyes closed, with a blindfold.

What other tests did I do well at?

- Silograms, which is a name for a silly test that correlates well with learning languages.
- English language vocabulary. (Did then, still do, even though I still like a lot of short words.)
- Ideaphoria—ability to be innovative, creative, have lots of ideas.
- Accounting aptitude—the ability to check errors in numbers.
- All other Structural Visualization tests that correlate with the wiggly block and other engineering work.
- Objective personality.
- Analytical reasoning.
- Inductive reasoning.
- Number memory.
- Memory for Design.
- Tonal memory.
- Foresight.
- Counting backwards.
- Number reasoning.
- Spelling.
- Finger dexterity (right hand).

What tests did I score low on?

- Pitch discrimination.
- Timbre discrimination.
- Color-blindness. (I am slightly colorblind.)
- Finger and tweezer dexterity (left hand).
- Abstract visualization.

What does it mean if you have an aptitude and you aren't using it? You may, without noticing why, get frustrated. Let's say you have good musical aptitudes. If you have to drop out of a choir to work on "work," you may get frustrated, and yet not be able to put your finger on why. I had to drop out of a chorus, but I keep my licks by singing along with the radio. There are ways to exercise such aptitudes if you are aware that you have them.

What does it mean if you are doing OK in a job where your aptitudes are needed, but *your* aptitudes are low? You may be doing OK by working *hard* as a salesman, or a manager—but you may be getting frustrated. Maybe you should plan to shift your career into an area that's a better fit with your aptitudes.

What does it mean if you have too many aptitudes? It indicates that you are likely to be easily distracted, with too many irons in the fire. It makes it easy to be a jack-of-all-trades—and master of none. If you are aware of this, you can concentrate on the necessary tasks when it's really important, and get that task done. Like graduating from school. (Or completing a column before deadline.)

I have recommended to several engineers, and technicians, and friends, to take the HEL tests. Often, they learn about some aptitude, missing or *extra*, that explains why they were not happy in their career.

So if you are curious why you are having fun at some job, or curious why you are doing OK even though you are *not* having fun, you might think about taking these tests.

The tests are of all sorts; in general, they are fun. They take three 3-1/2 hour sessions, typically (but not necessarily) on consecutive days. The fee in 1997 is $480. Not cheap, but if it changes your life, it's a bargain.

Now, here's a curve: FORGET the name Human Engineering Laboratory. Call up the Johnson O'Connor Research Foundation, in any city listed below. THAT is the new name for the HEL. Ask for more information.

My wife has been tested. My kids have been tested. For example, we had Benjamin tested when he did so well at geometry that they put him into the advanced algebra section, where he struggled miserably. Benjamin's Strùctural Visualization is quite high, so he did well at geometry. (Probably he inherited it from his mother.) But his accounting aptitude is low, which means he makes lots of mistakes on numbers and codes, and he can't spot the mistakes. NOW it all makes sense!!

I almost forgot about the subject of aptitudes, because I gave a lecture on this at a local amateur science group several years ago, and then set it aside. Finally, I realized I had not written it up as a column. Here you are. Enjoy!

All for now. / Comments invited!
RAP / Robert A. Pease / Engineer
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Computer Tech Support

Let's Take Another Look.

The August 4 column on computer tech support drew a surprising amount of mail; indeed, more than was ever anticipated. While the volume is encouraging, quite a few readers raised points that were never addressed in the original piece (some quite vocally). Before much time passes, I'd like to answer these important issues directly.

The first business is to correct some readers' mistaken impressions vis-à-vis that column. The reference "calendar months of debugging" was not related to overall functionality of the computer, but to final video system refinement (as careful reading reveals). Now, on to the mail.

RF Consultant Judd Sheets of Odin Engineering wrote two long and pointed letters on the support topic, which are distilled into one below.

I read your column about Tech Support and wanted to relate my opinions on the subject. Like most of us, I use a computer extensively. But, time spent maintaining them is, frankly, money taken from my pocket.

To me, it's unbelievable that anyone would have to follow such a circuitous path of solution. Yet, this seems to be accepted by many computer users. Every time new hardware or software is installed, they then spend many hours tweaking to make things work as they were supposed to out of the box. I, for one, find this situation intolerable. If you want to do real work with the PC and make money, it had better work the first time, every time.

I have, for several years, used a Macintosh (Mac) for most of my work, reserving a PC for those few applications where I couldn't find a Mac equivalent. I spend almost no time maintaining the Mac, even though it is a much more complex setup than the PC. The PC is a minimal system with only a few applications installed, yet it crashes occasionally for no apparent reason. I use a schematic-based microwave simulation package on the Mac that most RF engineers would die for, DragonWave by Gigasim Inc. (http://www.gigasim.com)

I'm not here to say that the Mac is the ultimate computer. But, for this engineer, it works better, saves me money, and is just a better tool than any other platform I've seen to date. Even though the Mac cost me more, it has provided far greater return on my investment than the PC, solely because of lower maintenance costs.

I certainly am not trying to point the finger of guilt at anyone in particular, only at our collective complicity in accepting marginal computer products and manufacturer's tendency to ship incomplete, under engineered products. Is it reasonable to expect a typical nonengineer user to go through what you did to get their computer working?

Shouldn't we be able to merely plug in a new card, turn it on and, in some large percentage of cases, have it function flawlessly? I expect (and get) such performance from your company's products, so why not those of the PC vendors?

WALT JUNG

The main premise of your article seemed to be that vendor support is often incompetent and insufficient, and can be supplanted by combing the Internet. While I absolutely agree with you, it is the basic necessity of this effort that I find offensive.

Am I an idealist?—sure I am. But I fail to see why we should continually forgive the PC industry for the status quo in personal computing reliability. If the computer breaks, get it fixed. But simple upgrades and installs should almost never trigger a protracted troubleshooting session.

Certainly, a lot of these problems stem from PC motherboard diversity, software versions, etc. Windows 95 is amazing in it's ability to install itself on the majority of machines. However, I have seen little from the PC industry in improving the situation other than the largely forgotten 'plug and play' hype. Features and speed alone seem to drive the market. Users must demand better quality, as well as speed goals.

I've found at least a partial solution in the Mac. Mine has been very reliable. When I added a video card, I plugged it in, loaded the drivers, and that was it. I don't think much about the machine; it just does what I ask.

Again, I am not suggesting that the Mac is the ultimate computer. But users should expect more from their computers than 166 MHz, 32-Mbytes of RAM, 2-Gbyte hard drive, and a low price. That expectation includes trouble-free operation for the life of the product, not an expectation of quirky behavior and intractable problems.

I find that Judd Sheet's points fall into several categories, such as: time is money; Macs perform better and need less support; and his main point that both PC performance and support could be (a lot) better.

On the first point, certainly no one can disagree that lost computer maintenance time is lost money, or that more reliable and versatile computers save costs in the long run. But looking at it from the bigger picture, there is simply a lot more to it than just those issues.

A hardware platform choice is best made from multiple viewpoints, including the initial cost, software availability, vendor reliability, support requirements, network capabilities, just to name a few. Regardless of one's personal desires, a corporate standard can dictate the platform for you. Also, you always need to look out in time to project software/hardware support. For example, I often use PSpice for simulation, so I wouldn't pick a Mac for a new engineering machine (Mac PSpice support has been dropped).

Mac users are vocal with their opinions on the machine's advantages in ease-of-use and low support requirements—I got several messages to this effect. I can't argue, in fact I hope Mac users continue to get good service.

But even if the superiority issue were totally true, there is today about a 10:1 ratio of installed PCs vs. Macs. Whatever the cause, such a disparity drives software vendors to the predominant platform. And, without continually evolving and supported software, what good is any machine, however superior?

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To me, hardware choice at this level is a nonissue, as I have learned from some past experience. When you choose a technically superior platform and knowingly bypass the mainstream, you can run a risk (as I once did with a Zenith Z-100 vs. a PC). The risk is being caught out on the limb of a machine with dwindling and expensive support. On the other hand, in spite of some technical shortcomings, lowest common denominator hardware may be a better choice for software and information availability, and it is usually a no-brainer issue on initial costs. For example, if you are willing to tackle support issues yourself, you can build a truly powerhouse PC-clone today for about $1500, which also can be a real learning experience.

For better or worse, the PC does seem to be established as a corporate hardware standard. Given all of these factors, the stickiest part comes with managing the bottom line cost of PC support.

This leaves us with the thornier aspect of how PC support can be better. On this point, I do heartily agree that improvements are needed. Support shouldn't be such an agony! We, as consumers of PC systems, undoubtedly deserve better service and support for our dollars.

This latter issue is rather well addressed in a letter from Bill Lenihan of Hughes Aircraft Co.:

I commend you for finding a way to solve your problems despite all the barriers. I have also gone through similar torture tests and emerged (usually) victorious. But, there is a problem buried where you say "In spite of the ...consumed calendar months ...I still find the entire experience a positive one." You are speaking here as a proud engineer having conquered another challenge.

There is nothing wrong with that, except that it perpetuates the mind-set (among those who design products!) that it is OK for products to foul up, and to be poorly documented and supported. When confronted with cases as yours, we engineers need to think and act more like dissatisfied consumers. Yes, I've solved similar computer problems, but I don't want to. I want to get my work done. I expect all software to have good documentation, and any package over $100 to have good documentation and a human being at the company who will answer questions and help me solve my problems (I don't expect to pay extra fees for this support—are you listening, Bill Gates?).

A lot has been written about how the ideal engineer should be able to wear many hats: design, manufacturing, marketing, etc. Let's not forget the most important one: customer!

P.S. The alternative tech support via the Internet is only useful if your computer basically works, including the mouse, modem, and communication software. What are the alternatives if that isn't the case?

P.P.S Would you tolerate a similar tech support scenario with your car?

Well, Bill Lenihan makes some good points, and (perhaps rightly so) takes me to task for not calling the PC industry support structure more of a spade. I'll address his addendums prior to his main point.

If your computer is down and can't track down 'Net info, borrow your friend's computer. Inconvenient, but not impossible.

No, I wouldn't tolerate a similar support scenario from a car dealer. In fact, I had a nightmare of support frustration several years ago, when my wife's car developed a case of stalling in traffic. After repeated visits without a fix plus loss of a year, the dealership bought the car back. Of course, you do need to be doggedly persistent in such cases (and your state needs to have a "lemon law"). But going to the top of the management chain (the dealership president) may be your only solution. They may not always be willing to listen, so be prepared.

TIP: In terms of PC tech support, following a logical checklist can be of some help in problem resolution (see "Help Yourself"[1]). In this article, which features a survey of user opinions on tech support, several companies had superior support ratings. Of course, if you've personally had an unresolved problem with tech support, it doesn't matter how many others say that company is just fine—to you, it's still an unresolved issue.

I recently had a support problem with the machine that fostered the video problem of the August column. In the Windows 95 upgrade of this two-year-old machine, the motherboard-based hard disk controller simply refused to load in anything but "compatibility mode," meaning that the Windows 95 system suffered serious slowdowns. Support-line calls and messages to the PC's vendor drew recommendations of "Contact Microsoft, this is a Windows 95 problem." To make a long story short, a Microsoft Knowledgebase article (#Q151911) on this topic eventually led me to the controller chip manufacturer's website (*http://www.cmd.com/graphical/teq/ide/win95.htm*) where I downloaded a FAQ plus a driver set which ultimately fixed the problem.

But this fix arrived after the PC's vendor had steadfastly ignored several e-mails specifically asking if disk controller drivers could impact this area. Ironically, the fix came from the controller chip manufacturer, not the PC vendor who had used their chip on a motherboard. It's easy for me to conclude that this particular company simply isn't interested in supporting old PCs.

To return to the main thrust of Bill's letter, he's right; after the fix is in, then it is time to address the source of the original problem. But, this is the truly hard part, where we hardly know where to turn and have little leverage.

TIP: As noted, do document your problems, and present them to the vendor in as clear and concise a way as possible. If and when you should end up finding the fix somewhere else, perhaps a summary letter to the support supervisor, or better yet, the company president, may be in order.

I'll admit I don't know how to best impact the overall support situation, beyond spreading helpful words here. The PC support problem is very real, and isn't likely to go away. When companies like Microsoft get away with releasing a major operating system like Windows 95 without any printed documentation, then you know who's in the driver's seat (it ain't us users). Vendors are aware that their customers know their support can be iffy. A recent study showed that in a significant number (25%) of test calls to support lines, the support personnel couldn't reliably answer questions taken directly from the company's own on-line FAQs![2]

To finish on an up-note, the original column made the point that when

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things do go right, the Web can be a valuable information source. Nothing makes this point like the story below, from David Starr of Analog Devices.

I read your "Computer Tech Support" article and enjoyed it a lot. I also find Usenet gives good tech support, and read it frequently.

Here's my best Internet story. My computer fairy dropped a middle-aged Pentium 90 clone on me. It was "sorta" running, but so slowly that the ADSP2181 ICE was dying on me.

I figured it might be a motherboard jumper setting problem. Of course, the documentation was long gone, with no maker's name on the casework or motherboard (shrewd marketing tactic that). No little sheet of paper with jumper settings, nothing inside the case.

Finally, I took the only number on the whole silly machine and dropped it into the AltaVista search engine. Lo and behold, I got the maker's web site, the motherboard's instruction sheet, and a FAQ page. The FAQ had all the jumper settings; the works!

David, I'm glad that you gave us an example of how things can sometimes work positively!

Obviously, the tough issues of computer tech support won't find a final end in this column, nor likely a future one.

TIP: In the meantime, it serves us to reflect carefully on that fancy new machine and what goes along with it in terms of support. We can be more discerning in terms of support for whatever we do select.

Thanks to all those readers who wrote in on this topic, plus a special thanks to Windows 95 guru Hampton Childress who tipped me off on the Q151911 document.

Walt Jung is a corporate staff applications engineer for Analog Devices, Norwood, Mass. A longtime contributor to Electronic Design, he can be reached via e-mail at Walter.Jung@Analog.com.

References:

1. David Gabel, Eileen McCooey, "Tech Support Survey," *Windows Magazine*, August, 1997.
2. Jim Carlton, "Computer Help Lines Fail to Click OK in Survey That Finds Array of Glitches," *Wall Street Journal*, August 25, 1997.

PC-Card Reader/Writer Intended For SCSI Systems

Equipped with a built-in universal power supply for voltages between 90 and 260 V ac, and 50/60 Hz in the desktop versions, the PC-Card Readers/Writers of the MCDISK-G and MCDISK-E series also offer a SCSI interface. MCDISK accepts PC-Card (formerly known as PCMCIA cards) types I to III and offers support for SRAM, EPROM, Flash , and OTP cards of up to 64 Mbytes. However, it supports PC-ATA (miniature disk drives) as well, with a storage capacity of up to 4 Gbytes. Target applications of the portable device are industrial PCs, access control, data loggers, NC machine control, and storage for machine parameters. The desktop MCDISKs are CE marked, UL listed, FCC class B compliant, and they meet the relevant EMC requirements. AV

***MPL AG**, Taefernstr. 20, 5405 Baden-Daettwil, Switzerland, phone +41 56 493 30 80; fax +41 56 493 30 20.*
CIRCLE 512

Vector Signal Generator Targets Digital Signals Of Up To 3.3 GHz

The SMIQ family of vector signal generators represents a new generation of signal generators capable of digital modulation up to 3.3 GHz. It features a fading simulator option for the generation of fading signals. Consequently, it's possible to attain 6 and 12 path fading in full compliance with the test specifications of the mobile radio standards.

The SMIQ signal generators are capable of digital as well as analog modulation. They're intended for use in the development and production of receivers and components for digital mobile radio and other communications systems. With a baseband bandwidth of 30 MHz, vector modulation enables the generation of complex modulation signals for the RF carrier at bandwidths up to 60 MHz. This makes the SMIQ family capable for DAB (Digital Audio Broadcasting), DVB (Digital Video Broadcasting), and CDMA (Code Division Multiple Access) applications.

In addition to vector modulation, SMIQ can convert internally generated or externally fed data signals into the common digital modulation formats. The modulation formats 4FSK, GFSK, GMSK, BPSK, 8PSK, D8PSK, QPSK, OQPSK, Pi/4-DQPSK, and 16QAM to 256QAM can be generated with clock rates up to 7.5 Msymbols per second. The SMIQ signal generators feature tailored menus for the most important mobile radio standards. These menus offer a choice of preprogrammed network-conforming standard signals. Burst and frame structures are displayed graphically to help the user understand various complex signals. AV

***Rohde&Schwarz**, Muehldorfstr. 15, 81671 Munich, Germany; phone: +49 89 41 29 22 32; fax +49 89 41 29 32 08.* **CIRCLE 511**

Smart-Power Chip Contains CAN Controller

Manufactured in a third generation bipolar-CMOS-DMOS technology (BCD-3) the IC L9942 contains all of the control and driver functions needed to operate a door lock. The device, which is connected directly to a single-wire CAN bus, includes an ST6-type 8-bit microcontroller core, EPROM program memory, CAN protocol handler, line interface, voltage regulator, contact monitoring circuit, and H-bridge power amplifier that's able to drive up to 4 A. Thanks to its Power SO-36 package, the entire circuit can be integrated within a door lock module. This package requires the same area as a standard SO-20 package. That means it can be handled during board manufacturing with already existing tools, even though the new package offers better heat conductivity. The chip can be programmed, tested, and emulated with all of the existing hardware and software tools for the ST-6 family. AV

***SGS-Thomson Microelectronics**, 55 Old Bedford Rd., Lincoln North Bldg., Lincoln, MA 01773; (617) 259-0300.*
CIRCLE 510

High-Voltage 0.8-µm CMOS Processes Suit ASIC Solutions

Austria Mikro Systeme and Thesys, Erfurt, Germany, are introducing a new family of mixed-signal CMOS processes, designated as CXT, CXY, and CYZ, which are targeted for high-voltage ASIC solutions up to 50 V. The 0.8-µm double-metal, single-poly, basic process "CXT (C08HA)" was developed mainly for ASICs that incorporate complex digital parts with high-speed and high-density elements operating in a high-voltage environment. The "CXY (CX0HD)" process is a double-metal, double-poly version for integrating linear capacitances. The "CXZ (CX08HI)" is a double-metal, double-poly, high-resistive poly process for linear resistance applications requiring a minimum area.

Various high-voltage devices are available in addition to the standard low-voltage MOS transistors, such as HV-NMOS, -PMOS, -DMOS transistors; n-junction FETs, and so on. High-voltage and standard devices can be easily combined on the same ASIC through the new technology. Low power consumption, fast switching capabilities, and applicability to a wide range of automotive and industrial performance requirements are other key benefits of this new family. That's because they can withstand high-voltage spikes which typically occur in such environments. RE

***Austria Mikro Systeme**, Schloß Premstätten, A-8141 Unterpremstätten, Austria; phone: +43 (03136) 52 500; fax: +43 (03136) 52 501, 53 560; e-mail: info@ams.co.at; Internet: http://www.ams.co.at.* **CIRCLE 513**

Edited by Roger Engelke

Pc-Board Tools Complete Product Family

Two new members have been added to the Integra Station product family for the design of printed-circuit boards. The tools—Integra Station Basic and Classic—are targeted at electrically ensuring consistent schematic and pc-board layout through real-time integration in a single database. This means that all data, whether physical or logical, is automatically updated to keep the project data consistent. And, as a result, all changes such as the addition or deletion of a component or symbol, are immediately implemented in all areas of the project.

The Integra Station Basic tool is specifically intended for use by designers with limited budgets and moderate technology requirements. It features 4 signal layers, 32 power layers, and 2000 component pins. Two add-on packages, Advanced Technologies and Programmable Post Processor, are available for use with the tool. The first package includes split power planes, class-to-class design rules, variant design, pad shaving, module reuse and testpoint management. The Programmable Post Processor (PPP) compiler and parser run-time version comes with PPP macro manager, PPP output, TXFOUT, Gerber and penplot panelization, and collimation test in NC drill.

The Integra Station Classic tool offers a full-featured pc-board layout variant targeted at designers who require a highly-integrated system with additional functionality via add-on packages for specialized applications. The tool features 32 signal layers and 32 power layers and offers three optional technology packages An Advanced Rule package provides class-to-class rules with on-line DRC, paired blind and buried vias, functionality, and a compiled PPP macro for extracting high speed rules to CCT SPECCTRA.

Both tools are now available on the PC. Integra Station Classic sells for $14,000, while its add-on packages, Advanced Rule, Industrial and Consumer, and Programmable Post Processor, cost $7000, $5000, and $3500, respectively. The Integra Station Basic goes for $3500, while its add-on packages, Advanced Technologies, and Programmable Post Processor, both sell for $3500 apiece. CA

Mentor Graphics Corp., 8005 S.W. Boeckman Rd., Wilsonville, OR 97070; (503) 685-7000 or (800) 547-3000; http://www.mentorg.com.
CIRCLE 460

Bus Simulation Model Supports 1394-1995 Standard

A third-party 1394 Bus Simulation Model is now available that supports the functional verification of components and systems based on the IEEE 1394 high-performance serial bus standard. The model, which enables designers to set up 1394 test environments and develop test benches in a relatively short period of time, promises to help reduce functional and timing errors prior to silicon or board fabrication.

The model works by checking for the protocol of any 1394 transactions. All possible errors then are flagged and logged to better facilitate the debug process. In this manner, designers can cut down on design iterations by detecting and correcting any functional errors early in the design cycle. Test benches can be created using the high-level design command interface present in the model.

The 1394 Bus Simulation Model supports all transactions and transfers in the IEEE 1394-1995 standard specification. It consists of three independently controllable sub-models that include PHY, LINK, and LINK-PHY Monitor. Each of the sub-models can support 100-, 200-, and 400-Mbit/s speeds. The PHY and LINK sub-models are targeted for use in multi-node test environments. They allow designers to mix and match test scenarios to verify designs l.

The 1394 Bus Simulation Model, which is available now, can support all Verilog and VHDL simulation environments. It may be purchased as part of the 1394 SANDesigner ADVantage Toolkit, and is priced at $30,000 per site license. CA

Sand Microelectronics Inc., 3350 Scott Blvd., #24, Santa Clara, CA 95054; (408) 235-8600; e-mail: info@sandmicro.com; Internet: http://www.sandmicro.com.
CIRCLE 462

CSM Tool Offers Increased Automation And Flexibility

Specifically targeted at Component and Supplier Management (CSM), Explore version 3.5 offers a number of advanced features not present in previous tool versions. Such features include a rules-based search capability that lets users quickly find functionally equivalent parts known as the Aspect Component Expert upgrades and downgrades; and an optional tool known as Dashboard that allows users to perform sophisticated search, analysis, and reporting routines with the push of a button.

Aspect Component Expert includes the underlying rules for equivalents, as well as upgrades and downgrades. It works by quickly searching both legacy databases and Aspect's VIP Reference Databases to weed out redundant part numbers. The rules are included in the VIP reference Database and can be modified by the designer from within the Explore 3.5 tool.

When unable to locate an exactly equivalent component to replace one that's becoming obsolete, the designer can turn to upgrades or downgrades. These options enable the designer to locate components that are either an upgraded or downgraded version of the obsolete component. In this case, the Explore 3.5 tool would return a list of appropriate alternative components, given particular technical and business criteria.

The optional Dashboard tool comes with a pre-configured set of best practice operations. The designer can launch a sequence of multiple Component and Supplier Management operations simply by pushing a button. Traditionally, launching a Component and Supplier Management operation could take as many as 10 or 20 steps.

Explore 3.5 is available now, with price depending on the configuration purchased as well as the number of users. Dashboard also is available as an option for users that have Explore 3.5. CA

Aspect Development Inc., 1300 Charleston Rd., Mountain View, CA 94043; (415) 428-2700; (800)-941-1046; e-mail: sales@aspectdv.com; Internet: http://www.aspectdv.com.
CIRCLE 461

Simulator Targets A/MS Design Environment

Traditionally, there haven't been many tools aimed specifically at the analog or mixed-signal (A/MS) design environment. With the introduction of ViewAnalog, an analog and mixed-signal simulator, designers should have an easier time designing and developing analog and mixed-signal circuits.

The tool, based on UC Berkeley's SPICE3 and the Georgia Institute of Technology's XSPICE, offers native analog and gate-level digital simulation capabilities, and can analyze switch-mode power supplies, mixed-signal ASICs, RF communication systems, interconnects, connect systems, and mixed electrical/mechanical systems.

As an interactive tool, it enables users to break free from the more traditional batch-style Spice analysis. Its Spice browsing and modeling-editing capabilities simplify design entry and allow for interactive cross-probing of the schematic. At the core of the tool are a series of high performance algorithms that provide very fast simulation and improved convergence for difficult circuits.

More specifically, the ViewAnalog tool features a host of capabilities, including behavioral modeling, sweeping of any circuit variable, 12-state timing simulation, interactive waveform cross-probing, automatic curve-family generation, and real-time display of voltages, currents, and power dissipation. It offers support for BSIM3 version 3 and SOI MOSFET models.

The ViewAnalog simulator is available now as part of Viewlogic's, Marlboro, Mass., Workview Office Version 7.4 suite of Windows-based EDA tools. It's tightly integrated with the company's ViewDraw schematic capture tool. The Windows version sells for $5500 for a node-locked version. A floating license sells for $7500. CA

Intusoft, *P.O. Box 710, San Pedro, CA 90733; (310) 833-0710; Internet: http://www.intusoft.com.* **CIRCLE 463**

Analog/Mixed-Signal Tool Focuses On Test Automation

Test Designer is a simulation-based test synthesis product that automates analog and mixed signal (A/MS) fault simulation, fault diagnostics, test software development, and acceptance test generation. It allows users to pair different circuit configurations with various analyses to create tests to detect one or more component failure modes or out-of-tolerance conditions. Test Designer then runs the entire suite of tests automatically.

When completed, a test strategy report is generated that summarizes the test results. The results then can be output to a file in several formats suitable for reports and user documentation. Finally, the tests can be imported to the designer's test programming language. These files contain the logical structure of the tests so that the designer only needs to add the test-equipment-specific coding.

The Test Designer tool offers a number of features beneficial to the analog/mixed signal designer. An automated failure analysis capability, for example, allows the designer to easily define and select a series of component faults or other out-of tolerance conditions. The simulator then automatically inserts each failure mode without altering the appearance of the schematic, performs the analysis, and removes the fault. This process requires no user intervention and is repeated until all faults have been inserted and simulated.

Detailed test reports and a fault tree are generated, allowing the designer to develop a test strategy for automation testing. In addition, a Quick Edit mode permits users to make a change to a circuit and instantly resimulate. As a result, the designer can see a comparison of current and previous measurement results.

Test Designer also offers a schematic entry capability that can integrate all of the relevant design and test information, fault analysis results, and test sequence data. The designer can define all part faults graphically using simple dialog entries. As an added benefit, the proper net list for each failed part scenario is generated automatically.

Test Designer, available now, is compatible with x86 PC with 32-Mbyte RAM, and Windows 95 or NT. It sells for $12,000 with a maintenance fee equivalent to 15% of the original purchase price. CA

Intusoft, *P.O. Box 710, San Pedro, CA 90733; (310) 833-0710, Internet: http://www.intusoft.com.*
CIRCLE 464

Virtual Prototyping Tool Targets IP-Based Designs

By using a novel virtual prototyping tool specifically targeted at intellectual property-based ASIC and IC designs, designers can see how a design will perform in the real world before committing to a particular physical library or foundry. The tool offers estimation, RTL Floorplanning, and time-budgeting capabilities. These features become particularly critical as IC design projects migrate to 0.35-µm geometries. Early in the design cycle at such levels, designers are forced to analyze technology and architecture trade-offs to accurately predict area, speed, and power across DSM (deep submicron) technologies. A virtual prototyping tool such as Design VP makes this possible, and saves design time and money in the process.

The Design VP tool is process-independent, supports both VHDL and Verilog descriptions, and allows users to understand the delays up front to accurately predict the performance of an RTL design before deciding on a specific technology. In this manner, designers can exchange architectural blocks and scale across technologies to understand the impact each element has on the entire design. It also has a floorplanning feature, as well as being able to perform full-chip estimation and drive logic synthesis and static timing analyses.

TimeSlice, a time-budgeting and partitioning tool, comes as an option to the Design VP tool. It works by eliminating the need for numerous logic synthesis iterations and automatically performs time budgeting and partitioning for every single block on the entire design.

The Design VP and TimeSlice tools are available now, and through December of 1997 will sell for $25,000 and $15,000, respectively. CA

Compass Design Automation, *1865 Lundy Ave., San Jose, CA 95131; (408) 434-7820; or on the Internet: http://www.compass-da.com.*
CIRCLE 465

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Now the easiest and most cost-effective way to read, program and verify 2716 – 8 megabit EPROMS. Support for Micros, Flash, EPROM, 16-bit, PLDs, and Mach (call for support list for specific models, or download demos from our BBS or web site).

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Souped Up SH-3 32-Bit CPU Runs At 100 MHz

The latest upgrade to the SH-3 family of 32-bit RISC CPUs is a version that runs at a 100-MHz clock rate—67% faster than the previously available versions. The higher speed provides greater throughput, which enables OEMs to create new systems or enhance existing designs while maintaining their software enhancements.

The power-efficient SH7708R and 7718R chips deliver a throughput of 100 MIPS when running at 3.3 V and 100 MHz. At that speed the chips dissipate just 400 mW, typical, and include versatile power-management capabilities. The enhanced CPU includes a5-stage pipeline, a linear address space of 4 Gbytes, and a 16-bit fixed instruction length for improved code density.

The SH7708R and 7718R contain similar features, except that the 7718R also packs a 200 MFLOPS floating-point unit to support graphics applications. Common resources on the CPUs include a memory-management unit, an 8-kbyte cache (also configurable as a 4-kbyte cache and 4 kbytes of SRAM), a 32-bit multiplier-accumulator, a three-channel 32-bit timer, a serial communications interface, a real-time clock, watchdog timer, a glueless interface to most memory types (SDRAM, fast-page DRAM, SRAM, and burst ROM), and still other functions. In 10,000 unit quantities, the SH7708R sells for $21 apiece, while in similar quantities the 7718R sells for $25 each. Samples are immediately available, with production scheduled for the first quarter of 1998. DB

Hitachi Semiconductor (America) Inc., *2000 Sierra Point Pkwy., MS-080, Brisbane, CA 94005-1897; (800) 285-1601; http://www.hitachi.com.*
CIRCLE 466

Large SDRAM DIMMs Target Big Memory Subsystems

Targeted for large computer systems, servers, and workstations, 200-pin dual in-line memory modules (DIMMs) provide memory densities ranging from 16 to 256 Mbytes per module. The JEDEC-compatible 200-pin modules are fully registered or buffered. Either approach allows the module to appear as a single load to the system, rather then having each SDRAM chip appear as a load (as is typical in all the unbuffered modules). This single-load-per-module is critical if the system has to support four such modules and achieve gigabyte/s bandwidth over the memory bus.

Modules are available in 2-Mword by 72-bit up through 32-Mword by 72-bit versions with ECC, or in by-64 versions without ECC. Cycle times are 10, 12, or 15 ns, and linear or interleave burst lengths are 1, 2, 4, 8, or page. The buffered or registered modules also include PLL-controlled timing to ensure optimum performance in the system. The PLL clock circuit synchronizes the clock signal on the module, thus ensuring timing accuracy. In combination with the buffered design, the circuit makes it feasible to use multiple DIMMs on the same motherboard. The modules measure 6.051 inches long by 1.25 in. high, with prices starting at about $6.5/megabyte. DB

Smart Modular Technologies Inc., *4305 Cushing Pkwy., Fremont, CA 94538; Bill Johnston, (510) 623-1231; http://www.smartm.com.* **CIRCLE 467**

Embedded PCI Interface Eases MPC860 Designs

Tying the MPC860 PowerQUICC processor to the PCI bus, the PCI9080 and the 9080RDK-860 reference design kit offers a simple solution for streamlining MPC860 system designs. The PCI9080 provides a PCI 2.1-compliant bus master interface that can operate at 3.3 or 5-V and includes an I^2O compatible messaging unit along with eight 32-bit mailbox and two 32-bit doorbell registers. Two on-chip independent DMA channels handle data transfers between the local bus memory to and from the PCI host bus.

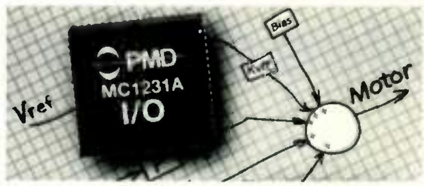
The chip packs eight programmable FIFO buffers to allow zero-wait-state burst operation. There's also programmable local bus support for non-multiplexed 32-bit address/data or multiplexed 32- or 16-bit buses, as well as slave accesses of 32-, 16-, or 8-bit local bus devices. The development kit supporting the 9080 includes the chip residing on a PCI v2.1-compliant bus-master board, which can be configured as a PCI adapter or embedded system.

A full software development kit is included—the kit contains advanced programming libraries and source code, Windows 95 and NT device drivers, and source code, as well as monitoring and debug software. The development kit sells for $2495. DB

PLX Technology Inc., *390 Potrero Ave., Sunnyvale, CA 94086; Mark Easley, (408) 774-9060, or on the web at: http://www.plxtech.com.*
CIRCLE 468

Brushless Motor Control Chip Set Adds Flexibility

Based on DSP technology, the MC1231A brushless motor control chip set employs an advanced servo filtering scheme that allows optimization of the motor settling time. In addition to the servo control, the chip set is thought to be the first that directly performs sinusoidal commutation of brushless motors using the motor's encoder signal to determine phase angle. Up to two independent motor axis can be controlled by the MC1231A.



The DSP engine allows the servo algorithm to be executed completely in software, thus improving the flexibility of the chip set to handle new motor requirements. The servo filter provides full proportional, integral, derivative (PID) control as well as velocity feedforward. All gain parameters are alterable on-the-fly. The chip set also supports a dc bias register, torque limiting, and a programmable servo error limit, which allows the chip set to automatically detect problems in the system mechanics.

Additional features include four user-selectable profiling modes—S-curve, trapezoidal, velocity contouring, and electronic gearing—as well as two directional limit switch inputs per axis.The chip set is available in a one- or two-axis configuration and consists of two chips, each housed in a 68-lead PLCC. The two-axis version sells for $85.00 per set in lots of 1000 units. DB

Performance Motion Devices Inc., *97 Lowell Rd., Concord, MA 01742; Chuck Lewin, (508) 369-3302, or on the Web at http://www.pmdcorp.com.*
CIRCLE 469

Catalog Sways Toward Motion-Control Products

The *1998 Motion Control Product Catalog* from Galil Motion Control Inc., Mountain View, Calif., covers the company's complete line of motion controllers, software tools, amplifiers, and motors. Detailed product specs, selection guidelines, technical references, pricing and ordering information, dominate the book. Also included are educational segments that discuss a step-by-step process for specifying motion control, a 23-page tutorial on the basics of motion-control systems and programming, and various application stories. For a free copy of the catalog, contact Galil at (800) 377-6329; fax (650) 967-1751; or e-mail at: *galil@galilmc.com.* RE
CIRCLE 470

Plug Into Brochure On High-Density Connectors

Stacking connectors and other products specially designed for high-density devices, such as laptops and cellular phones, are the focus of "Perfect for High Density," AMP's (Harrisburg, Pa.) new brochure. Brief descriptions of 20 connectors are accompanied by photos and illustrations. Also detailed are 0.6-mm and 0.8-mm free height connectors, a 0.8-mm high-density interconnection system, and a 0.015-in. to 0.100-in. centerline surface-mount connectors. More detailed info can be obtained using toll-free numbers given in the catalog. For more general information or to get the brochure, call (800) 522-6752; Internet: *http://www.amp.com.* RE CIRCLE 471

Wireless Communications Get The Call In This Catalog

A 240-page catalog from TriQuint Semiconductor Inc., Hillsboro, Ore., dials up the complete run of products offered by the company's Wireless Communications Division (WCD). Included are data sheets for WCD standard IC products, as well as application notes and evaluation board productivity kits to assist RF system designers in choosing integrated devices that best meet their design requirements. Summary information is provided on three of the company's advanced GaAs processes available to those who wish to design their own ICs. To order a free copy, call (503) 615-9000; fax (503) 615-8901; e-mail: *sales@tqs.com.* RE CIRCLE 472

Connector Selecting Guide Ensures No "Diss"-connection

The new quick reference guide, *The LEMO Connector Selector*, breaks down LEMO USA's (Santa Rosa, Calif.) product line into an easy-to-read product selection tool for engineer's needing to locate the right connector solution. Each connector is featured with a photo followed by technical information that includes contact configurations and types, shell styles, materials, options, ratings, and cable specifications. LEMO's connectors are available in single, multi, or mixed contact insert configurations, including coaxial, triaxial, high voltage, fiber optic, fluidic/pneumatic, and thermocouple. Call LEMO USA at (800) 444-5366; fax (707) 578-0869; e-mail: *lemous@lemo.ch*; Internet: *http://www.lemo.ch.* RE CIRCLE 473

Government/Space Products Guide Is Out Of This World

Available free of charge to qualified engineers is the completely new 1400-page desk reference, *Government and Space Products*. The databook, offered by International Rectifier, El Segundo, Calif., contains detailed technical specifications and application information for a range of products required in high-reliability power-conversion systems such as power supplies. Among the examples detailed are control ICs, HEXFET power MOSFETs, IGBTs, and Schottky and fast-recovery diodes, several of which are radiation-hardened versions in special hermetically sealed packages. To get the guide, fax IR's literature department at (909) 975-5699. RE CIRCLE 474

Short-Form Catalog Gives Thanks For The Memories

Enhanced Memory Systems Inc., Colorado Springs, Colo., recently announced a short-form catalog and new application notes for its high-performance specialty memories, the enhanced DRAM (EDRAM) and enhanced synchronous DRAM (ESDRAM) products. Featured is an overview of the company's 4-Mbit EDRAM and 16-Mbit ESDRAM products. The 20-page catalog compares these products against other specialty memories in random access time and sustained bandwidth. Application notes help designers match EDRAM and ESDRAM products with popular, high performance processors from Analog Devices, Motorola, and others. Call (719) 481-7002; fax (719) 488-9095. RE CIRCLE 475

Technological Advances Have Family Ties

SEC Family News, from Samsung Electronics, combines the company's most recent technological advances with information about people, places, and ideas around the world. In its September 1997 edition, features included Samsung's sports philosophy and support, including TOP (The Olympic Partner) IV for wireless communications of the 1998 Winter and 2000 Summer Games. Also profiled was Korea's TFT-LCD business and Samsung's partnership with Vietnam. To find out more, call Russell Dubner at (212) 704-8222, or Amy Lu at (212) 704-4453. Or access the web page at : *http://www.sec.samsung.co.kr.* RE
CIRCLE 476

Waves Of Measurement Products Get The Spotlight

A comprehensive Measurement Products Catalog for 1997/1998 has been issued by Tektronix Inc., Beaverton, Ore. Instrumentation solutions covered range from low-cost instrumentation and handheld products to conventional measurement products and advanced mixed-signal test solutions. Featured within the 630-page catalog are 80 new products and measurement solutions, as well as tutorials and application and technical notes. Extensive indices list products by name and function, as well as category. For further information on the catalog, call (800) 426-2200 (press 3, code 1040), or visit the company's web site at: *http://www.tek.com/Measurement.* RE
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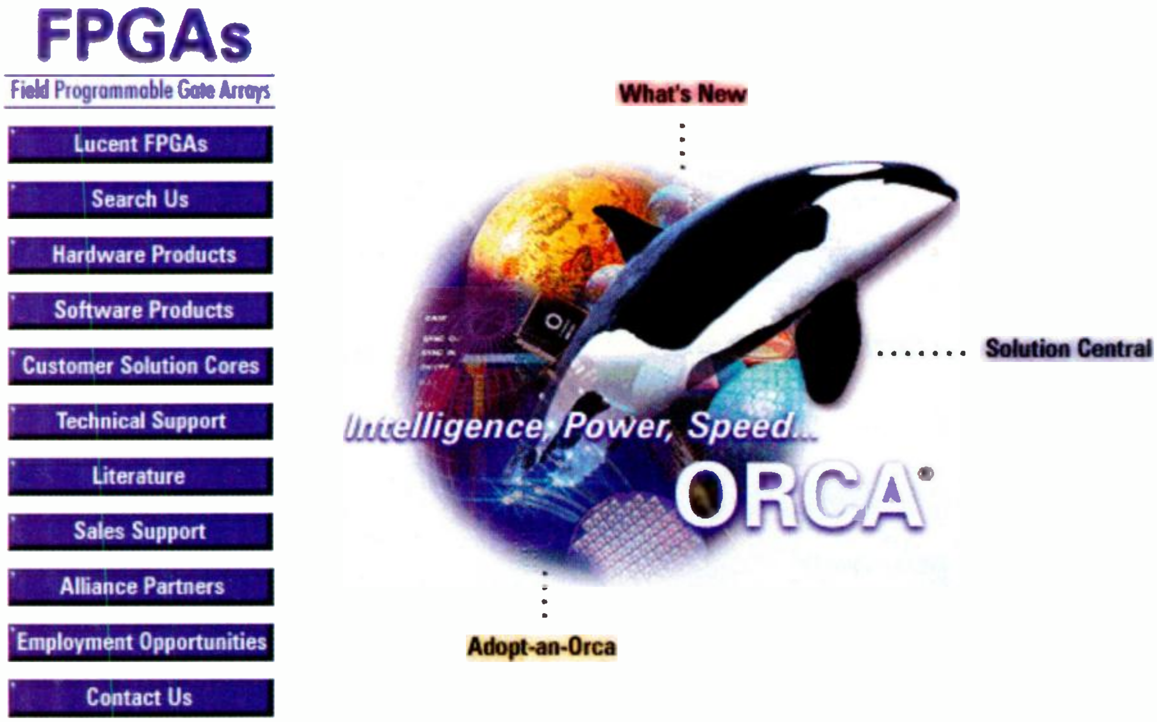

Our New Web Site is Making Waves!

Our redesigned site gives you access to all the latest information about our *ORCA*® series field-programmable gate arrays (FPGAs). Included in this on-line product guide are data sheets, product briefs, ordering information, product availability, application notes, article reprints, and much more. We also provide extensive technical support options including e-mail directly to our customer support engineers. It's the perfect information source for component and design engineers.

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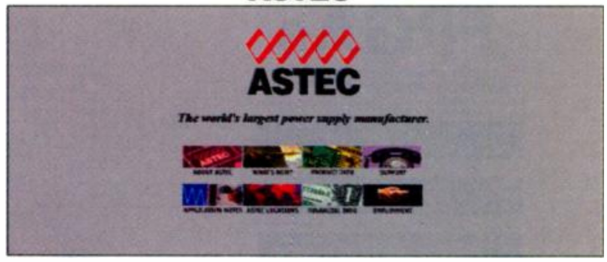

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http://www.mill-max.com

ELECTRONIC DESIGN CATALOG/LITERATURE REVIEW

THERMAL CLAD DESIGN GUIDE

New for 1997, Bergquist Thermal Clad Design Guide features the New Band Ply Family of material as well as updated technical information on Thermal Clad, Insulated Metal Substrate. THERMAL CLAD materials allow designers to reduce the number of thermal interfaces in the assembly and take advantage of the high thermal conductivity of the metallic layers of THERMAL CLAD.

CIRCLE 250

BERGQUIST COMPANY

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B+K Precision has introduced four device programmers that offer comprehensive device libraries, excellent performance, and high flexibility, at extremely competitive prices. Model 840 is $199, and Model 841 is $249. Model 842 is $695 and Model 843 is $795. Specifications are included in the New B+K Precision Catalog. Tel: 773-889-1448. Fax: 773-794-9740. Visit us at www.bk-precision.com

CIRCLE 251

B&K PRECISION

FREE T & M PRODUCTS CATALOG

The 1997 catalog from Lecroy offers complete technical information and pricing on our complete line of digital oscilloscopes. Also included are technical application notes covering many topics.

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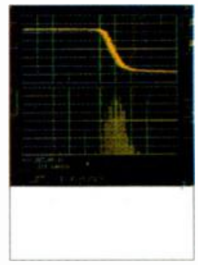

CIRCLE 252

LECROY

Digital Modulation

A new application in Communication note introduces the concepts of digital modulation, Topics include how information is modulated onto I and Q signals, different types of digital modulation, filtering and multiplexing techniques,how digital transmitters and receivers work, and much more. Emphasis is placed on understanding the critical tradeoffs that designers make in order to optimize systems for efficiencies of bandwidth, power , and cost.

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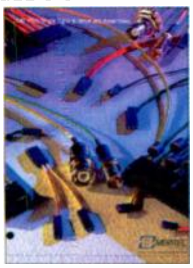

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Catalog describes the RelCalc2 software package, which automates Mil-HDBK-217 or Bellcore on your PC, and allows quick and easy reliability analysis of your electronic products. Phone: (818) 991-0057, Fax: (818) 991-1281

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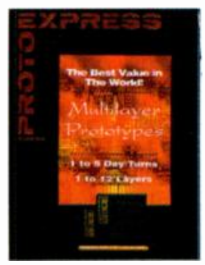

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TERN, INC.

Kepco's New Power Supply Catalog

Kepco's new power supply catalog and handbook integrates in one volume digital and analog power supplies that allow for a high degree of control flexibility including VXI. Recently Kepco has introduced many new digital models; they are cataloged here with full specifications. Modular units include p-c card multi-output models, high-density dc-dc converters, and high power plug-in models for N+1 redundancy applications..

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ELECTRONIC DESIGN CATALOG/LITERATURE REVIEW

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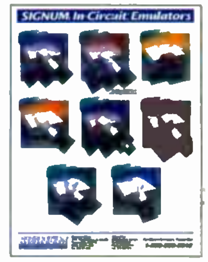

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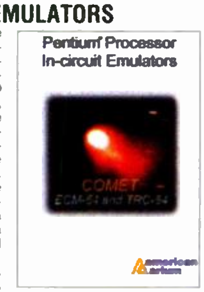
American Arium has been the primary market supplier of Pentium® processor In-circuit Emulators since 1991. In 1995, the company introduced their Pentium® Pro In-circuit Emulator. Recently, American Arium announced the release of Comet In-Circuit Emulators. These were specifically designed for the embedded software developer, with special attention paid to the 66Mz real-time trace engine and ultra-accurate breakpoints. The Comet ECM-54 is a portable low cost solution which provides processor control through the Intel defined, JTAG debug port. Comet TRC-54 is a full featured In-Circuit Emulator with American Arium Data Capture Technology.



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AMERICAN ARIUM

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Western Design Center's product selection and developer guide describes our 65C02-BASED CMOS low power IC microprocessors. Included is information about our chips, boards and licensable cores.

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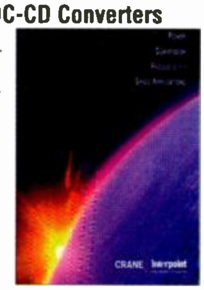

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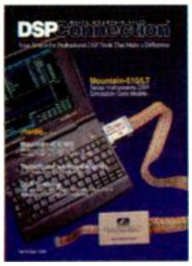
E-SWITCH

ELECTRONIC DESIGN CATALOG/LITERATURE REVIEW

THE DSP CONNECTION™



Featuring the complete line of DSP development tools from White Mountain DSP, the DSP Connection is your source for the latest information on DSP development. Application articles, features and views from industry leaders in DSP make this publication a must for developers in DSP as well as those new to DSP. Make the DSP Connection. phone: (603) 883-2430, Fax: (603) 882-2655.
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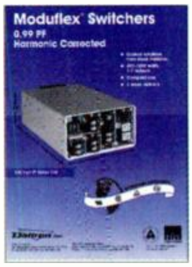

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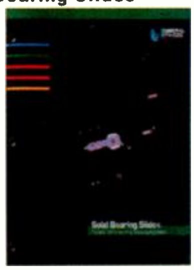

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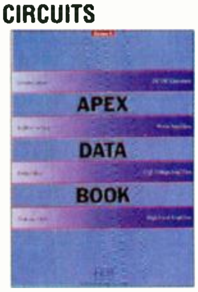

The 7th edition Apex Power Integrated Circuits data book contains complete product data sheets and applications notes for Apex Microtechnology's power Amplifier PWM Amplifier and DC/DC Converter product lines.
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APEX

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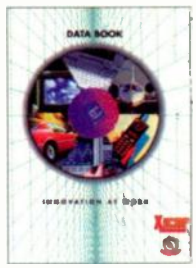

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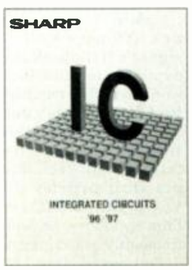
CIRCLE 287

MICROTEC

SHARP FIFOs



First-in, First-out memories are just the stuff the no-nonsense design environment of the '90s is meant to build on. Used as data buffers between systems operating at different speeds, FIFOs conserve valuable board space, streamline design tasks and reduce system cost. Sharp's new 1997 IC Short Form Catalog is packed with information about Sharp FIFOs.

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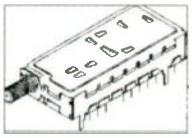

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A/D Electronics' free BNC Connector catalog features a variety of BNC's in different configurations. This 10 page catalog offers both 50 and 75 ohm styles. The design engineer can obtain complete specs, dimensional drawings and evaluation samples upon request. A/D Electronics also supplies a variety of interconnects for the OEM. Technical Support is available by contacting: 253-851-8005 or Fax: 253-851-8090. Website: www.adelectronics.com

CIRCLE 292

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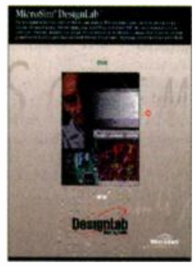
Interface Technologies distributes Version 7.1 of MicroSim DesignLab and MicroSim Pspice A/D with Schematics. Version 7.1 supports long file names in Windows 95 and Windows NT, includes DXF export, enhanced simulation libraries, library browser and search engine, and automated move, select and edit in MicroSim PCBoards. Call 1-800-357-1636 or browse http://www.i-t.com for more information.



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CIRCLE 297

C&K COMPONENTS INC.

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Our 28 page four color catalog is an excellent buyers guide for design and production engineers shopping for EPROM /FLASH/PLD/FPGA design, programming, erasing and test tools. The catalog offers products for every budget and level and also includes a host of Socket converters and adapters for DIP, PLCC, TSOP, QFP technologies. For more information call Logical Devices at 800-331-7766. web: http://www.logicaldevices.com

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"X86 and 683xx/HC16 Design Tips"

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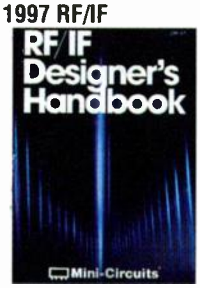
MICROTEK INTERNATIONAL

MINI-CIRCUITS FREE 1997 RF/IF

Mini-Circuits brand new 760 page RF/IF Designer's Handbook is now available for distribution worldwide. The handbook is loaded with fresh design and applications information, such as modern surface mount techniques, practical articles about VCO's, ERA MMIC amplifiers and more, answers to frequently asked questions, definitions of terms, convenient selection guides and handy conversion charts.



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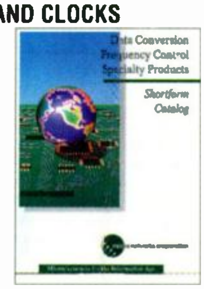
MINI-CIRCUITS

DATA CONVERSION AND CLOCKS

Micro Networks Corp. short form catalog covering standard data converters and frequency control products. Products are designed for commercial, industrial, and military applications in computers, communications and control circuits. Phone: (508) 852-5400



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ELECTRONIC DESIGN CATALOG/LITERATURE REVIEW

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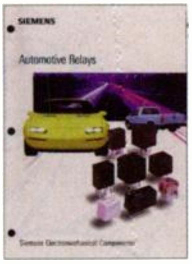

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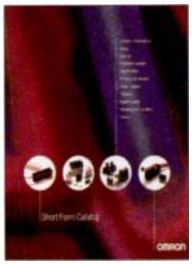

CIRCLE 305

OMRON ELECTRONICS, INC.

NEW SWITCHING REGULATORS

Power Trends, Inc. has released a new 80 page full-line catalog for its complete line of Integrated Switching Regulators and DC to DC converters. the catalog introduces significant new products along with extensions to existing product lines. Complete specifications, photos and standard applications are provided for each product along with mechanical configuration options and ordering information.

CIRCLE 306

POWER TRENDS, INC.

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CIRCLE 307

OTTO Control

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Techron's medical products brochure provides information about the companies capabilities as a supplier of gradient amplifier systems. Two new companion data sheets list specifications for the TEC7782 gradient amplifier and 8700 gradient amplifier systems. For more information visit our web site at www.techron-amps.com, call us at 219-294-8300 or send e-mail to techron@crownintl.com.

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TECHRON

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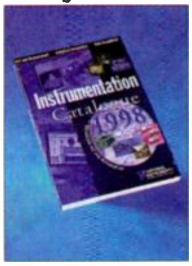

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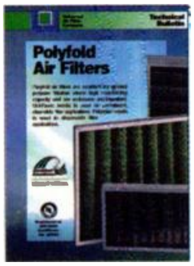

CIRCLE 312

UNIVERSAL AIR FILTER

Application Specific Interconnect Guide

Samtec's application Specific Product Group can quickly design modified and custom interconnects. This guide provides an overview of the capabilities, including contact and pin modifications, modified and custom insulator bodies and special services such as custom plating and packaging, and shows an extensive array of example interconnects. For information call 1-800-SAMTEC9. Fax: (812) 948-5047

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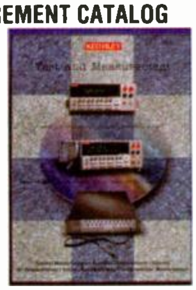
NEW TEST & MEASUREMENT CATALOG

Keithley offers its new 1997 catalog of test and measurement instruments including DMMs, electrometers, precision sources, voltmeters, source-measure units, power supplies, switch systems and more. Phone: 500/552-1115. FAX: 216/248-6168 http:// www. keithley.com



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Hasbrouck Heights, NJ; (201) 393-6060
National Sales Manager: Russ Gerches
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Director Of Marketing: Walker Johnson
San Jose, CA (408) 441-0550, FAX: (408) 441-6052
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MODEL TECHNOLOGY INC.	290,254	238,235
MOTOROLA MICROCOMPUTER	-	33
MOTOROLA SEMICONDUCTOR	-	2-3
MOTOROLA SEMICONDUCTOR	-	66-67
MPL ELEKTRONIK	337	60
MURATA ELECTRONICS	-	17**
NATIONAL INSTRUMENTS	187	25
NATIONAL SEMICONDUCTOR	-	8
NEC ELECTRONICS	190	80AA*
NEC ELECTRONICS	189	80LM*
NEC ELECTRONICS	188	149*
NEEDHAMS ELECTRONICS	191	229
NEXLOGIC TECHNOLOGY	406	241
NIPPON ELECTRIC	345	36-37
NIPPON ELECTRIC	206	56-57
NJR CORPORATION	341	6
NOHAU CORPORATION	407	243
OCTAGON SYSTEMS	408,273	242,236
OKI SEMICONDUCTOR	209	18-19*
OMRON ELECTRONICS INC	227,305	23*,239
ONTIME ELECTRONICS	281	237
ORCAD SYSTEMS	228	Cov2
ORCAD SYSTEMS	310	239
OTTO CONTROLS	307	239
OVERNITE PROTOS	409	241
PACIFIC SOFTWORKS	410	243
PENTEK INC.	229	76
PENTON INSTITUTE	-	81
PEP MODULAR COMPUTERS, INC.	230	21
PHILIPS SEMICONDUCTORS	231	18-19**
PICO ELECTRONICS	99	64,88
POTTER & BRUMFIELD	304	239
POWER DSINE INC.	102,258	24,235
POWER ONE INC	234	141
POWER TRENDS	233,306	125,239
PRECISION INTERCONNECT	235,285	65,237
PROTO EXPRESS	257,418	235,241
RLC ENTERPRISES	294,411	238,241
ROLYN OPTICS	266	236
SAMSUNG SEMICONDUCTOR	236	80XY*
SAMSUNG SEMICONDUCTOR	237	63**
SAMTEC INC.	238,279	145,237
SANYO DENKI	239	172
SENSORAY	-	105
SHARP MICROELECTRONICS	288,289	237,238
SIGNATEC	415	242
SIGNUM SYSTEMS	412 ,265	244,236
SIPEX	243	53
SMART MODULAR	244	94
STANFORD RESEARCH SYSTEMS	245,315	104,239
STEWART CONNECTOR	301	239
SUPERTEK INC	246	149*
SYNERGY SEMICONDUCTOR	144	68-69
SYNERGY SEMICONDUCTOR	145	70-71
T-CUBED SYSTEMS	256	235
TANNER RESEARCH	270	236
TEAM MIPS	185	28-29
TECCOR ELECTRONICS INC	146	78
TECHRON INDUSTRIAL	217,308	185,239
TEKNOR MICROSYSTEMS	100	100
TELEDYNE RELAYS	242	79
TELEDYNE RELAYS	340	177
TELTONE	269	236
TEMIC	-	13
TERN INC.	413,262	244,235
TEKTRONIX	-	62-63*
TEKTRONIX	-	82-83*
TEXAS INSTRUMENTS	241	50-51
TEXAS INSTRUMENTS	-	80HI*
TRANSISTOR DEVICES INC	114	135
TRANSISTOR DEVICES INC	226	177
UNITRODE INTEGRATED	267	236
UNIVERSAL AIR FILTER	312	239
VICOR	116	97
VISHAY INTERTECKNOLOGY INC	117	80S*
VISICOM LABORATORIES INC	339	99
VISTA CONTROL	291	239
VMETRO, INC.	343	111
VMIC	278	237
WESTERN DESIGN CENTER	272	236
WHITE MOUNTAIN DSP INC.	276	237
XENTEK POWER SYSTEMS	98,303	187,239
XICOR	219,286	157,237
XILINX	247	165
YAMAHA SYSTEMS TECHNOLOGY INC	105	201*
Z-WORLD ENGINEERING	414	241
Z-WORLD ENGINEERING	151	105
Z-WORLD ENGINEERING	274	236

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International **

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WOW! DC to 8GHz (up to +18.5dBm output)

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Model	*Freq. (MHz)	Gain (dB)	Max. Power Out (dBm, @ 1dB Comp)	Dynamic Range NF(dB)	Dynamic Range IP3(dBm)	@Device Current(mA)	①Price $ ea. (10 Qty.)
ERA-1	DC-8000	11.8	11.7	5.3	26.0	40	1.80
ERA-1SM	DC-8000	11.8	11.3	5.5	26.0	40	1.85
ERA-2	DC-6000	15.6	12.8	4.7	26.0	40	1.95
ERA-2SM	DC-6000	15.2	12.4	4.6	26.0	40	2.00
ERA-3	DC-3000	20.8	12.1	3.8	23.0	35	2.10
ERA-3SM	DC-3000	20.2	11.5	3.8	23.0	35	2.15
ERA-4	DC-4000	13.5	▲17.0	5.5	▲32.5	65	4.15
ERA-4SM	DC-4000	13.5	▲16.8	5.2	▲33.0	65	4.20
ERA-5	DC-4000	18.8	▲18.4	4.5	▲33.0	65	4.15
ERA-5SM	DC-4000	18.5	▲18.4	4.3	▲32.5	65	4.20
ERA-6	DC-4000	11.3	▲18.5	8.4	▲36.5	70	4.15
ERA-6SM	DC-4000	11.3	▲17.9	8.4	▲36.0	70	4.20

Note: Specs typical at 2GHz, 25°C. Exception: ▲ indicates typ. numbers tested at 1GHz.
* Low frequency cutoff determined by external coupling capacitors.
① Price (ea.) Qty.1000: ERA-1 $1.19, -2 $1.33, -3 $1.48, -4, -5 or -6 $2.95. SM option same price.

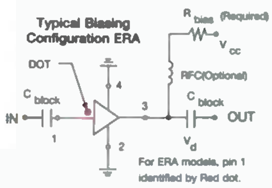
DESIGNER'S AMPLIFIER KITS:

K1-ERA: 10 of each ERA-1,-2,-3 (30 pieces) only $49.95
K1-ERASM: 10 of each ERA-1SM,-2SM,-3SM (30 pieces) only $49.95
K2-ERA: 10 of each ERA-4,-5 (20 pieces) only $69.95
K2-ERASM: 10 each ERA-4SM,-5SM (20 pieces) only $69.95
K3-ERASM: 10 each ERA-4SM,-5SM,-6SM (30 pieces) only $99.95

Chip Coupling Capacitors at 12¢ each (50 min.)

Size (mils)	Value
80x50	10, 22, 47, 68, 100, 220, 470, 680, 1000, 2200, 4700, 6800, 10,000 pf
120x60	.002, .047, .068, .1 µf

ACTUAL SIZE



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Cypress has expanded its family of industry-leading SRAMs to provide solutions for wireless applications. Our new low-speed, low-voltage, low-power 256K SRAMs provide a wide V_{CC} range (1.65 V to 5 V) and low I_{SB2} (100 nA, typ.; 5 µA, max.) to significantly extend battery life in portable products.

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These 256K SRAMs are offered in RTSOP (Reverse TSOP) and in standard TSOP, SOIC, and PDIP packaging, making them ideal for a variety of small-form-factor applications, such as pagers, cellular phones, and handheld games.

Cypress's new SRAMs use an innovative 6T-cell, 0.5-micron process technology to enable very small die size and lower price.

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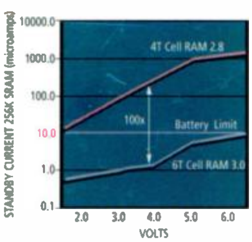
The new 256K SRAMs broaden Cypress's portfolio to provide customers a solid migration path, as well as "one-stop shopping." Now, from a single source, you can choose the SRAM that best meets your design challenge.

Low-Power SRAM Selector Guide

PART #	t_{AA}	V_{CC}	I_{SB2} (Max.)	I_{SB2} (Typ.)
CY62256	70 ns	4.5–5.5 V	5 µA	100 nA
CY62256V	70 ns	2.7–3.6 V	5 µA	100 nA
CY62256V25	125 ns	1.8–2.7 V	3 µA	100 nA
CY62256V18	150 ns	1.65–1.95 V	2 µA	100 nA



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