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TECHNOLOGY · APPLICATIONS · PRODUCTS · SOLUTIONS

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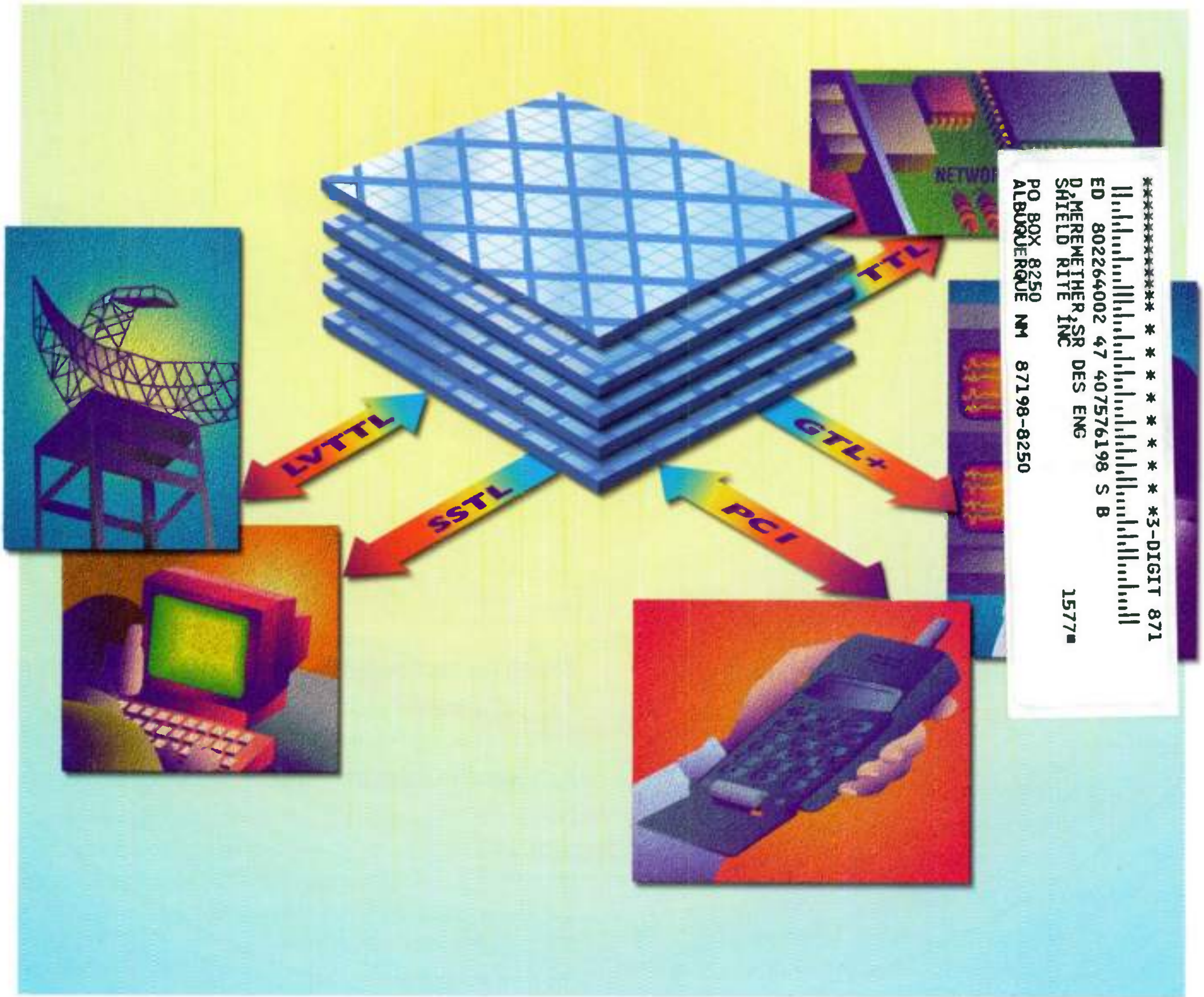
NOVEMBER 17, 1997



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November 17, 1997 Volume 45, Number 25

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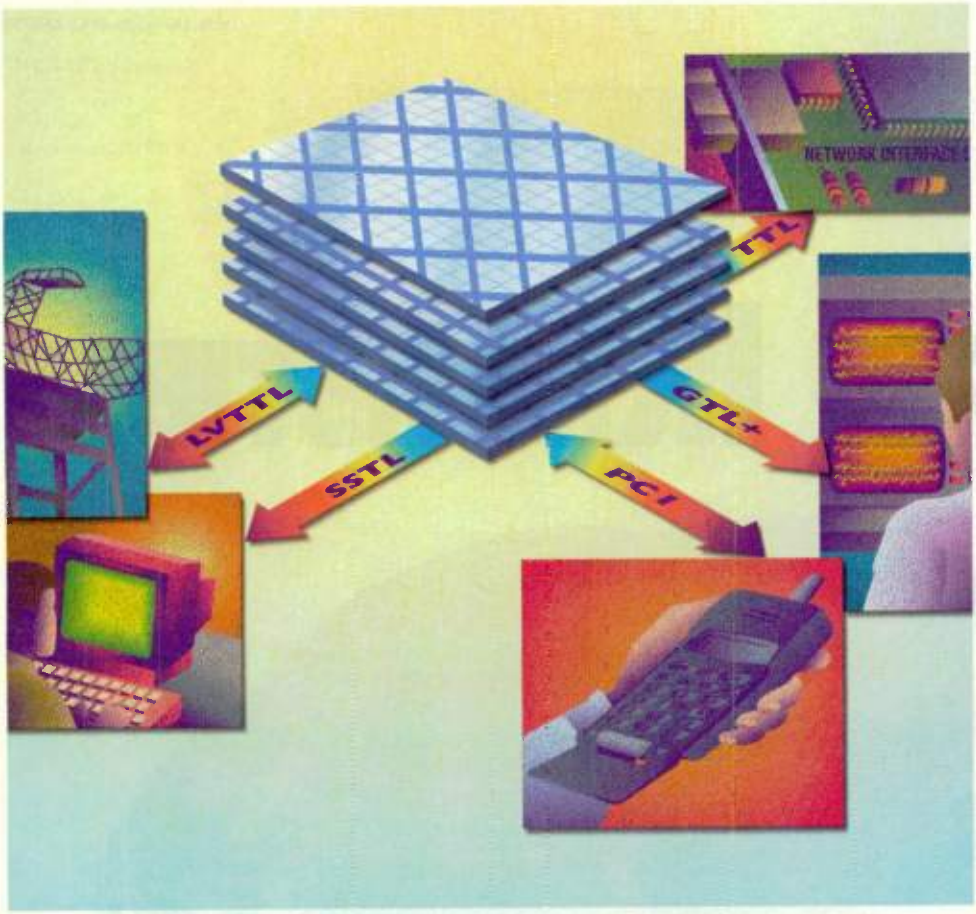

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ELECTRONIC DESIGN

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November 17, 1997 Volume 45, Number 25

EDITORIAL OVERVIEW

COVER ILLUSTRATION BY:
MARGARET ENDRES-BANGS

Jesse H. Neal Editorial Achievement

1967 First Place Award	1978 Certificate of Merit
1968 First Place Award	1980 Certificate of Merit
1972 Certificate of Merit	1986 First Place Award
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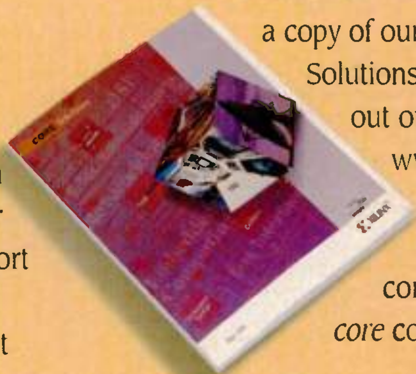

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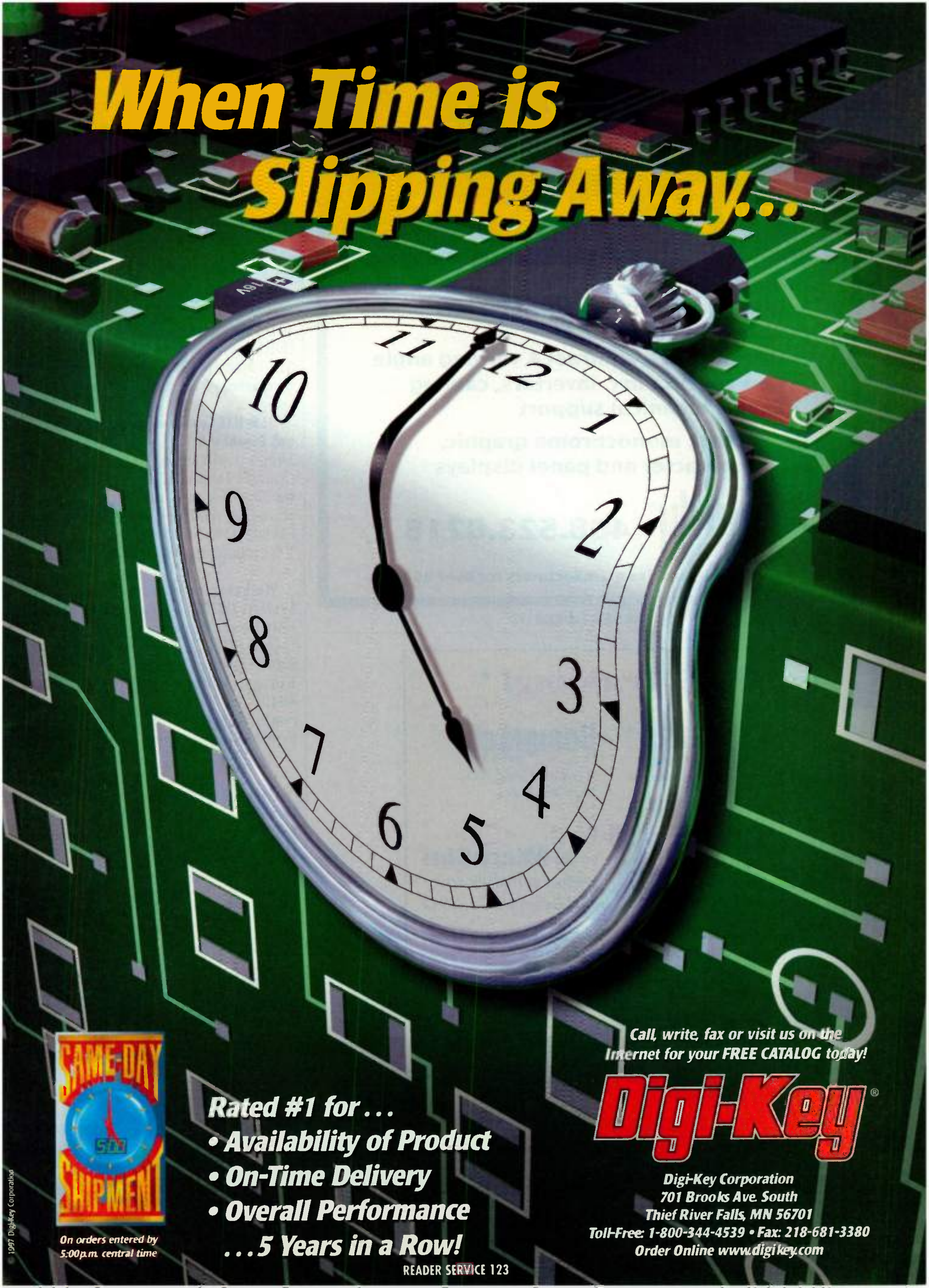
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DECEMBER 1997

Winter Simulation Conference (WSC '97), December 7-10. Renaissance Waverly Hotel, Atlanta, Georgia. Contact David Withers, LEXIS-NEXIS, P.O. Box 933, Dayton, Ohio 45401; e-mail: David.Withers@lexis-nexis.com.

IEEE International Electron Devices Meeting (IEDM), Dec. 7-11. Washington Hilton & Towers, Washington, DC. Contact Phyllis Mahoney, Widerkehr & Assoc., 101 Lakeforest Boulevard, Suite 270, Gaithersburg, Maryland 20877; (301) 527-0900; fax (301) 527-0994; e-mail: pwmahoney@aol.com.

36th IEEE Conference on Decision & Control, December 8-12. Hyatt Regency, San Diego, California. Contact Ted E. Djaferis, Dept. of Electrical & Computer Engineering, University of Massachusetts, Amherst, Massachusetts 01003; (413) 545-3561; fax (413) 545-1993; e-mail: djaferis@ecs.umass.edu.

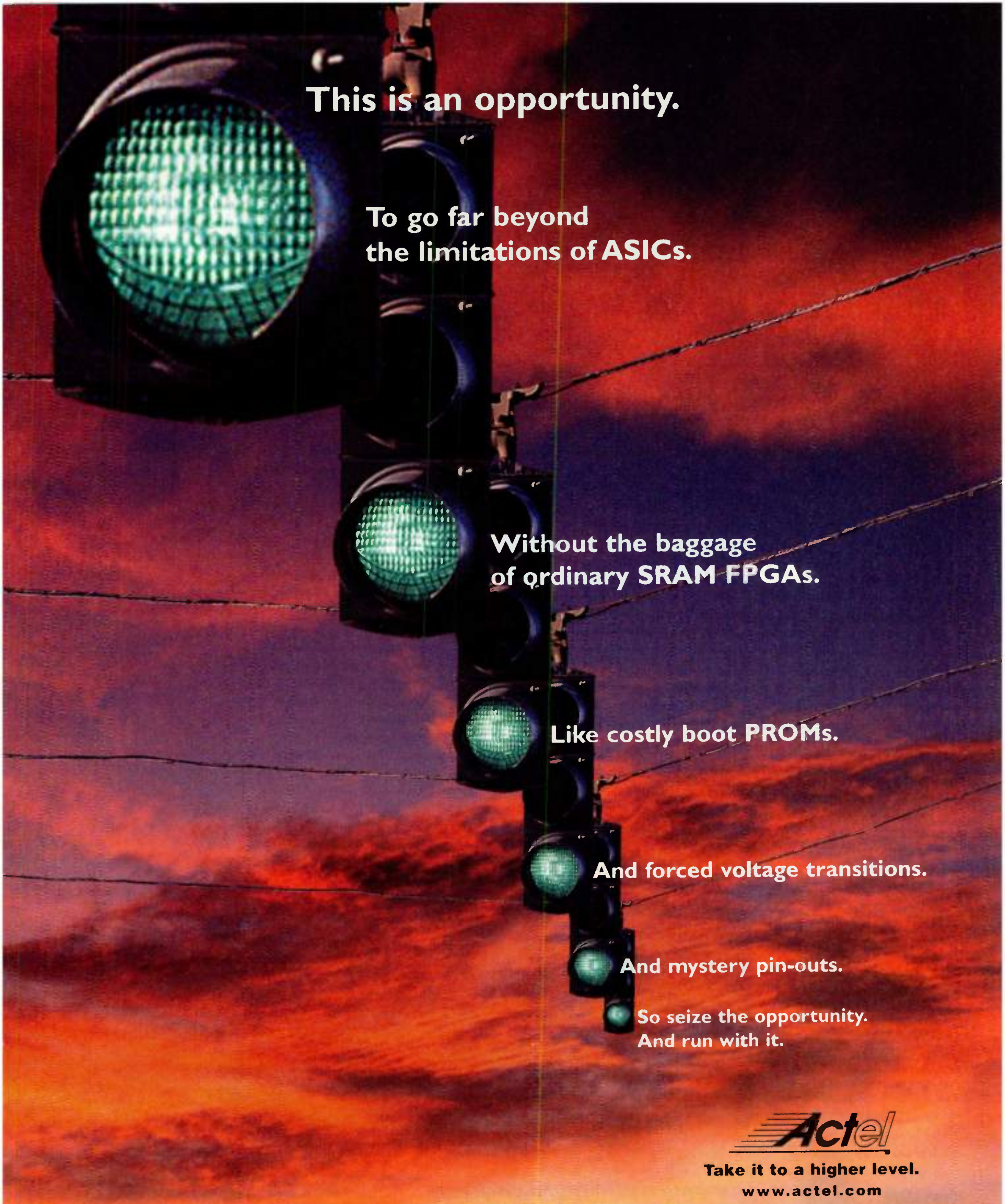
Workshop on Internet Technology & Systems (WITS), December 9-12. Marriott Hotel, Monterey, California. Contact USENIX Conference Office, 22672 Lambert Street, Suite 613, Lake Forest, California 92630; (714) 588-8649; fax (714) 588-9706; e-mail: conference@usenix.org; Internet: http://www.usenix.org.

JANUARY 1998

Seventh Joint Magnetism & Magnetic Materials Conference (INTEMAG), January 6-9. Hyatt Regency Embarcadero Hotel, San Francisco, California. Contact John Nyenhuis, School of ECE, Purdue Univ., West Lafayette, Indiana 47907-1285; (317) 494-3524; fax (317) 494-2706; e-mail: smag@ecn.purdue.edu.

Annual Reliability & Maintainability Symposium/Product Quality & Integrity (RAMS), January 20-22. Anaheim Marriott, Anaheim, California. Contact V.R. Monshaw, Consulting Services, 1768 Lark Lane, Cherry Hill, New Jersey 08003; (609) 428-2342.

Photonics West, January 24-30. San Jose, California Contact The SPIE Exhibits Department, Post Office Box 10, Bellingham, Washington 98227-0010; (360) 676-3290; fax (360) 647-1445; e-mail: exhibits@spie.org.



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JANUARY 1998

Seventh Security Symposium, Jan. 26-29. Marriott Hotel, San Antonio, TX. Contact USENIX Conference Office, 22672 Lambert St., Suite 613, Lake Forest, CA 92630; (714) 588-8649; fax (714) 588-9706; e-mail: conference@usenix.org; Internet: http://www.usenix.org.

IEEE Power Engineering Society Winter Meeting, Jan. 31-Feb. 5. Tampa, FL. Contact Jim Howard, Tampa Electric Co., P.O. Box 111, Tampa, FL 33601; (813) 228-4653; fax (813) 228-1333; e-mail: j.howard@ieee.org.

FEBRUARY 1998

IEEE International Solid-State Circuits Conference (ISSCC '98), Feb. 5-7. San Francisco Marriott, San Francisco, CA. Contact Diane Suiters, Courtesy Associates, 655 15th St. N.W., Washington, DC 20005; (202) 639-4255; fax (202) 347-6109; e-mail: isscc@courtesyassoc.com.

Portable by Design, Feb. 9-13. Santa Clara Convention Center, Santa Clara, CA. Contact Rich Nass, Electronic Design, 611 Route 46 West, Hasbrouck Heights, NJ 07604; (201) 393-6090; fax (201) 393-0204; e-mail: portable@class.org.

The Wireless Symposium and Exhibition, Feb. 9-13. Santa Clara Convention Center, Santa Clara, CA. Contact Bill Rutledge, Penton Publishing, 611 Rte. 46 West, Hasbrouck Heights, NJ 07604; (201) 393-6259; fax (201) 393-6297; instant faxback (800) 561-7469; Internet: http://www.penton.com/wireless.

IEEE Applied Power Electronics Conference and Exposition (APEC '98), Feb. 15-19. The Disneyland Hotel, Anaheim, CA. Contact Pamela Wagner, Courtesy Associates, 655 15th St., N.W., #300, Washington, DC 20005; (202) 639-4990; fax (202) 347-6109; e-mail: pwagner@courtesyassoc.com.

Conference on Optical Fiber Communication (OFC '98), Feb. 22-27. San Jose Convention Center, San Jose, CA. Contact Lisa Myers, OSA Conference Services, 2010 Massachusetts Ave., N.W., Washington, D.C. 20036-1023; (202) 416-1980; fax (202) 416-6100; e-mail: ofc.info@osa.org.

Design, Automation, and Test in Europe Conference and Exhibition (DATE '98), Feb 23-26. Le Palais des Congres de Paris, Porte Maillot. Contact European Conferences, 11C Wemyss Pl., Edinburgh EH3 6DH, UK; +44 131-225-2892; fax +44 131-225-2925.

38th Israel Conference on Aerospace Sciences, Feb. 25-26. Tel-Aviv & Haifa. Contact Technion-Israel Institute of Technology, Haifa 32000, Israel; 972-4-8292713; fax, 972-4-8231848; e-mail: alice@aerodyne.technion.ac.il.

MARCH 1998

International Verilog Converfence and VHDL International User Forum (IVC/VIUF), March 16-19. Santa Clara Convention Center, Santa Clara, California. Contact MP Associates, 5305 Spine Rd., Suite A, Boulder, Colorado 80301; (303) 530-4562; fax (303) 530-4334; e-mail: lee@mpa-net.com; Internet: http://www.hdlcon.org.

Second Intellectual Property in Electronics Seminar (IP '98), March 23-24. Westin Hotel, Santa Clara, California. Contact John Whitaker, Miller Freeman Technical Ltd., +44 181-316-3297; e-mail: ed98@cityscape.co.uk.

Sixth Annual Embebbed Systems Conference East, March 31-April 2. Chicago's Navy Pier Festival Hall, Chicago, Illinois. Contact Miller Freeman Inc., 600 Harrison St., San Francisco, California 94107; (415) 905-2354; fax (415) 905-2220; Internet: http://www.embedsyscon.com/.

APRIL 1998

Southeastcon '98, April 10-15. Hyatt Regency, Orlando International Airport, Orlando, Florida. Contact Parveen Ward, ECE Dept., University of Central Florida, Orlando, Florida 32816; (407) 823-2610; fax (407) 823-5835; e-mail: pfw@ece.engr.ucf.edu.

16th IEEE VLSI Test Symposium, April 26-30. Hyatt Regency Monterey, Monterey, California. Contact Rob Roy, Intel Corp., MS:JFT-102, 5300 Elam Young Pkwy., Hillsboro, Oregon 97124-6497; (503) 264-3738; fax (503) 264-9359; e-mail: robroy@ichips.intel.com.

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EDITORIAL

Just Have To Have Convergence

At least once a month, I go to my local electronics megastore to buy a few music CDs and just poke around for a while. The place has everything an audio/videophile, technophile, and gadget lover would want. Plus, there are action movies playing on big screens with surroundsound; music thumping from the audio department; and assorted sounds emanating from the computer department. Of course, there's always something new to check out and demo models to play with, while a salesperson insists that I *need* to take that product home today.

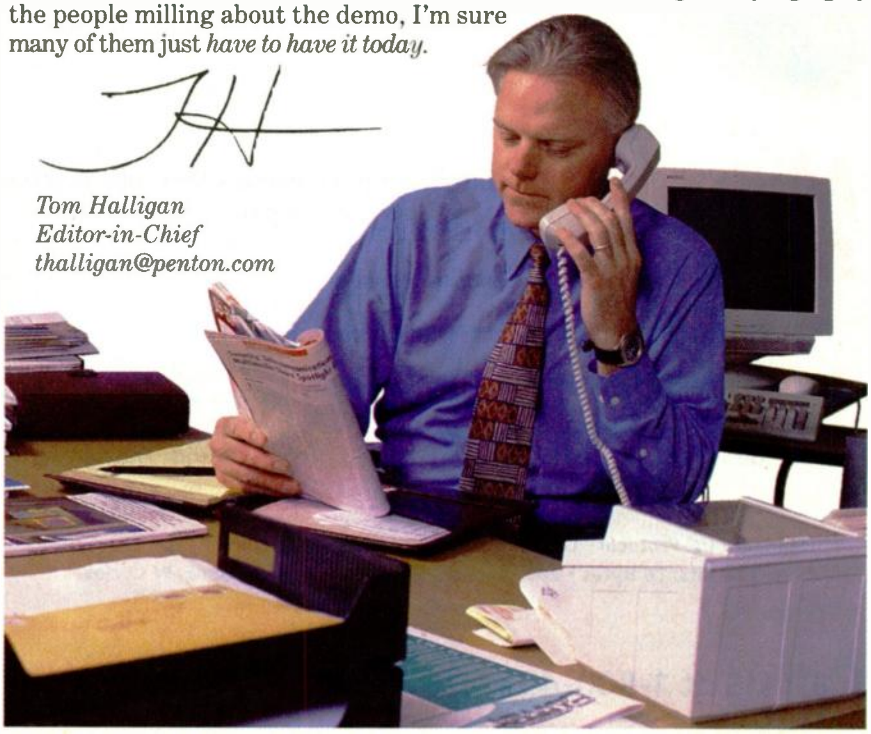
It's almost impossible to go away empty-handed because the store is a multimedia funhouse, and you feel as if you just *have* to have the latest product. And apparently, a lot of consumers agree, because 1997 marks the sixth consecutive record-setting year for the consumer electronics industry.

What's hot? A variety of new digital products and home "information appliances." In the digital arena, the new Digital Versatile Disk (DVD) players, digital cameras, and digital cellular phones are taking off. Information appliances—cordless phones, computers, modems, monitors, and software—are seeing consistent growth. Home-entertainment products also are doing well. Sales of home-theater systems, VCRs, direct-to-home (DTH) satellite systems, electronic games, and compact audio systems will increase over last year's figures. Another growth area is mobile electronics, including wireless telephones, aftermarket vehicle security, radar detectors, and factory-installed autosound.

These are examples of a "mega-trend" that the Consumer Electronics Manufacturers Association (CEMA) calls "convergence," which they define as the merging of traditional consumer electronics, such as audio, video, and personal communications products, with the digital world of PCs. Examples include TVs that feature built-in software to browse the Internet, and PCs with elaborate internal audio systems and TV tuner modules. It all comes down to the convergence of products that once were designated to either the home-entertainment market (family room) or the home-information market (home office).

What's not so hot? CEMA says that aftermarket autosound and pagers will lag behind last year's sales, as well as direct-view color TVs, rack audio systems, and separate audio components.

My favorite new product is the DVD player. It's expensive, but the quality of the audio and video on a wide-screen monitor was outstanding. And judging by the people milling about the demo, I'm sure many of them just *have to have it today*.



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Truth In Advertising?

My husband came home from work not too long ago with a story that a friend had e-mailed him. Maybe you've heard this story before. It's a dialogue between a customer support employee (E) and a software tool user (U).

E—*Computer assistance; may I help you?*

U—Yes, I was just typing along, and all of a sudden the words disappeared.

E—*Hmmm. What does your screen look like now?*

U—It's blank; it won't accept anything when I type.

E—*Is the power cord plugged in?*

U—Yes, it is.

E—*Good. Can you see another cord back there?*

U—No. It's dark. The only light I have is coming from the window.

E—*Turn on the lights.*

U—I can't; there's a power outage.

E—*A power outage? OK, we've got it licked now. Do you still have the packing stuff your computer came in?*

U—Yes.

E—*Good! Pack up your system and take it back to the store where you bought it.*

U—Really? Is it that bad?

E—*Yes. I'm afraid it is.*

U—All right, I suppose. What do I tell them?

E—*Tell them you're too dumb to own a computer.*

CHERYL AJLUNI
DESIGN AUTOMATION

Once you stop laughing, you may realize that this joke represents a bigger problem indicative of many segments in industry; not the least of which is the EDA industry. It's what many refer to as "truth in advertising." This means that when you buy something, you know exactly what it is and what it will do. However, there are times when this is not the case. Most designers today don't have enough time to evaluate new tools and verify every product feature claim. As a result, they often end up buying a tool and realizing after it's too late that it doesn't work as promised. And this will eat away at their already shortened product development cycles.

I know this to be true because I've talked to designers who have been in this position. They often find themselves sitting in the dark wondering why their computer doesn't work, despite the fact that the obvious culprit is a power outage. They're too involved in the project and too trusting of vendors' claims to see the nose on their face.

And as the industry migrates to smaller geometries, the problem is compounded. In a deep submicron (DSM) environment, the physics of the devices begin to break apart. The result is an emergence of tools designed to deal with these parasitic effects in a "behind the scenes" manner. This is ideal since most designers don't want to know what's going on behind the scenes anyway—they just want answers. Subsequently, the tools begin to play the role of the expert. But, if you don't understand what the tool does and why, then how can you evaluate its performance in the first place? You can't. You have to trust that your vendor has been honest with you. This is a heavy burden for any company, whose bottom line is money, to live up to. Some obviously do it better than others.

And there are those companies who would rather focus on knocking their competition instead of touting the benefits of their own tools. It's almost as if there is some sort of underground community of people lurking around the EDA trenches, looking for any information that can be twisted into an attack on the competition. But, I like to think that dignity and common courtesy still exist today, even in the face of the bottom line. Don't get me wrong, a good portion of the responsibility for truth in advertising lies in the hands of the EDA tool vendors. However, designers also must bear responsibility for their own actions. *cjajluni@class.org.*

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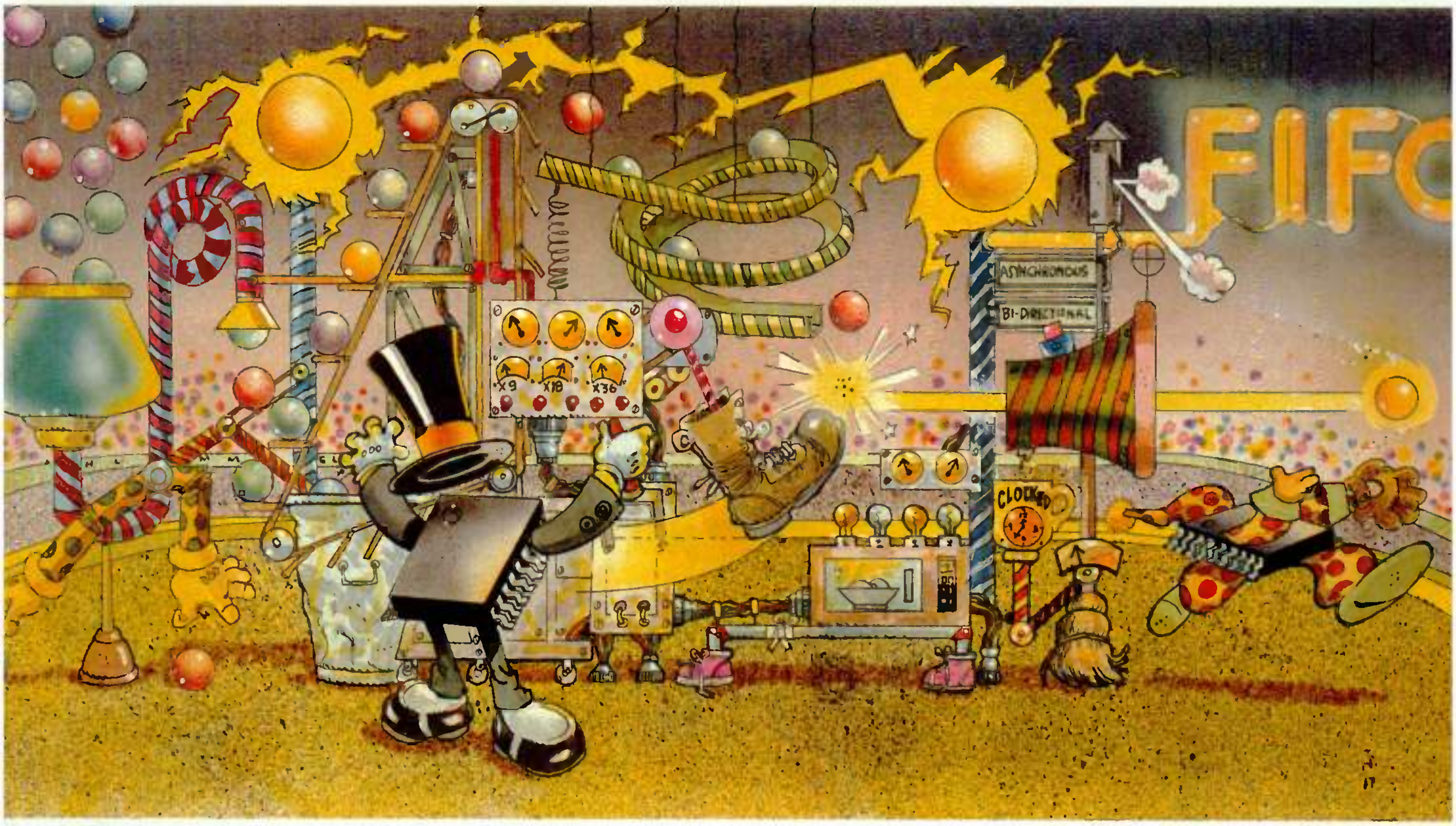

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Device	Description	Pins
Asynchronous FIFOs		
QS7201	512 x 9 with Buffer Memory	32, 28
QS7202	1K x 9 with Buffer Memory	32, 28
QS7203	2K x 9 with Buffer Memory	32, 28
QS7204	4K x 9 with Buffer Memory	32, 28
Clocked x9 FIFOs		
QS72211	512 x 9 Parallel Synchronous	32
QS72221	1K x 9 Parallel Synchronous	32
QS72231	2K x 9 Parallel Synchronous	32
QS72241	4K x 9 Parallel Synchronous	32
Clocked x18 FIFOs		
QS72215	512 x 18 Parallel Synchronous	68
QS72225	1K x 18 Parallel Synchronous	64
Clocked x36 FIFOs		
QS723611	512 x 36 x 2 Bidirectional Clocked FIFO with Dynamic Bus Sizing	144
QS723620	1K x 36 Clocked FIFO with Dynamic Bus Sizing	132
QS723621	1K x 36 x 2 Bidirectional Clocked FIFO with Dynamic Bus Sizing	144
QS725420A	256 x 36 x 2 Bidirectional Clocked FIFO	132, 144

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READER SERVICE 171

MAUS Detects An Aircraft's Hidden Damage Beneath Metal

The portable MAUS (Mobile Automated Scanning) system uses ultrasound or electromagnetic fields to peer beneath composite or metal surfaces to detect hidden damage. Developed for the Air Force's Wright Laboratory by Boeing Company (formerly McDonnell Douglas) Phantom Works, St. Louis, Mo., MAUS is much faster and significantly more accurate than previous methods that required tedious, labor-intensive inspections and perhaps disassembly of the complete system or components to be inspected. Ultrasound sensors are used for composite surfaces and electromagnetic sensors for metal surfaces.

MAUS consists of a handheld unit about twice the size of a computer mouse connected to its electronics box, and a laptop computer. Interchangeable sensors attached to the unit are guided over the area to be inspected, dramatically improving the quality of information to assist engineers in making component integrity decisions. The gathered data is portrayed on the computer screen in color or shades of gray, and can be saved for later analysis. The images allow for quick interpretation and analysis in three dimensions. Approximately 200 square feet an hour can be scanned on average.

Though still considered in the prototype stage, MAUS is working its way into Air Force operational use at Air Force Material Command Air Logistics Centers. Directorate engineers have made MAUS available to the Navy, race-car teams, and racing-boat teams to demonstrate the system's commercial potential. Several airlines have used MAUS sensors , cutting the time needed to inspect seams along the top of an aircraft from 100 hours to 4 hours, without removing interior components. Charles Buynak, senior materials research engineer with the directorate, is working with the U.S. Auto Club (USAC) to use MAUS on Indy-style race cars. He and colleagues traveled to the Indianapolis Motor Speedway to test the concept. Using ultrasound, MAUS found disponds and other anomalies that a surface inspection might portray as minor, or might miss altogether. Call their Public Affairs Office at (937) 255-2725; Internet: *http://www.wpafb.af.mil/ascpa/index.html*. RE

TV/Multimedia Production All Wrapped Into One Device

To stay competitive in the consumer-electronic-based applications age, manufacturers can no longer afford to start from scratch every time they develop a new product. Instead, they're being forced to leverage intellectual property, whether in the form of software, hardware, or support services, offered by other vendors. This frees them up to focus on what they do best, as opposed to every detail of a new product's implementation.

Such is the case in a joint effort between Applied Magic Inc., San Diego, Calif., and Cadence Design Systems, San Jose, Calif.: They're developing a home entertainment device that can deliver professional-quality multimedia production features at an affordable price. The device, which will attach to a television, is similar in appearance to a cable set-top box. Once in place, it will give the most novice consumers the ability to create multimedia productions from a variety of sources, including videos, CDs, and the Internet on a home digital video recorder.

Under the terms of the agreement, Applied Magic will develop the device, including its hardware and software. Cadence's professional services organization will come up with the infrastructure to implement the device concept by creating the required ICs. By utilizing an outside resource to develop the needed custom ICs, Applied Magic hopes to successfully price their home multimedia system below the critical $1000 consumer-electronics barrier. Actual products are expected to be ready sometime in early 1998. For more information, contact Kevin Mosher, VP of operations, at (760)-931-6417; *klm@applied-magic.com;* Internet: *http://www.applied-magic.com*. CA

Hardware/Software Co-Design Model Under Development

Shrinking time-to-market cycles and more-complex designs harkens the call for creating software (SW) and hardware (HW) components in unison. The alternative, of course, entails designing each separately and then integrating them at the back end of the design cycle—an option that's no longer viable because the potential for back-end integration problems is too risky.

Fujitsu Microelectronics, San Jose, Calif., and Viewlogic Systems, Marlboro, Mass., have teamed up to create a SPARClite Instruction Set Simulator (ISS) model for HW/SW co-design and co-verification. The model will support all macro functional capabilities of Fujitsu's SPARClite processor, including cache hits/misses for instruction and data cache, cycle counts, burst mode, wire buffer, pre-fetch, and cycle-stealing. The model also will be cycle accurate for performance estimation and analysis. Special features included in the model will enable systems designers to control the simulation performance of the model versus timing accuracy.

Because the SPARClite ISS model is being designed with HW/SW co-development in mind, it will be delivered using Viewlogic's Eagle technology. It will work with the company's Eagle I tool for linking the software development environment with hardware simulation. As a result, customers can immediately begin using HW/SW co-development methods and tools in their design systems.Contact Viewlogic at *http://www.viewlogic.com* or Fujitsu at (800) 866-8608. CA

Edited by Roger Engelke

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MAY 1998

IEEE International Conference on Evolutionary Computation, May 3-9. Ankorage, Alaska. Contact Patrick K. Simpson, Scientific Fishery Systems Inc., P.O. Box 242065, Anchorage, AK 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@akaska.net.

IEEE International Conference on Neural Networks (ICNN '98), May 3-9. Anchorage, AK. Contact Patrick K. Simpson, Scientific Fishery Systems Inc., P.O. Box 242065, Anchorage, AK 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@akaska.net.

IEEE World Congress on Computational Intelligence, May 3-9. William A. Egan Civic and Convention Center, Anchorage, AK. Contact Patrick K. Simpson, Scientific Fishery Systems Inc. P.O. Box 242064, Anchorage, AK 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@alaska.net.

Seventh IEEE International Fuzzy Systems Conference, May 3-9. Anchorage, AK. Contact Patrick K. Simpson, Scientific Fishery Systems Inc., P.O. Box 242065, Anchorage, AK 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@alaska.net.

IEEE/IAS Industrial & Commercial Power Systems Technical Conference (I&CPS), May 4-7. Edmonton, Alberta, Canada. Contact Marty Bince, Modicon Canada Ltd., 5803 86th St., Edmonton, Alberta T6E 2X4, Canada; (403) 468-6673; fax (403) 468-2925.

IEEE International Conference on Acoustics, Speech & Signal Processing (ICASSP '98), May 12-15. Seattle Convention Center, Seattle, WA. Contact Les E. Atlas, Dept. EE (FT 10), University of Washington, Seattle, WA 98195; (206) 685-1315; fax (206) 543-3842; e-mail: atlas@ee.washington.edu.

JUNE 1998

IEEE/MTT-S International Microwave Symposium (MTT 98), June 7-12. Baltimore Convention Center, Baltimore, MD. Contact Steven Stitzer, Westinghouse Electric Corp., P.O. Box 1521, MS 3T15, Baltimore, MD 21203; (410) 765-7348; fax (410) 993-7747.

USENIX 1998 Technical Conference, June 13-17. Marriott Hotel, New Orleans, LA. Contact USENIX Conference Office, 22672 Lambert St., Suite 613, Lake Forest, CA 92630; (714) 588-8649; (714) 588-9706; e-mail: conference@usenix.org; Internet: http://www.usenix.org.

JULY 1998

IEEE International Geoscience & Remote Sensing Symposium (IGARSS '98), July 6-10. Sheraton Seattle, WA. Contact Tammy I. Stein, IGARSS Business Office, 2610 Lakeway Dr., Seabrook, TX 77586-1587, (281) 291-9222; fax (281) 291-9224; e-mail: tstein@phoenix.net.

IEEE Power Engineering Society Summer Meeting, July 11-17. Sheraton Hotel, San Diego, CA. Contact Terry Snow, San Diego Gas & Electric, P.O. Box 1831, San Diego, CA 92112; (619) 696-2780; fax (619) 699-5096.

LINEAR TECHNOLOGY
DESIGN NOTES

RS485 Transceivers Operate at 52Mbps Over 100 Feet of Unshielded Twisted Pair – Design Note 168

Victor Fleury

The propagation delay of typical RS485 transceivers can vary by as much as 500% over process and temperature. In applications where high speed clock and data waveforms are sent over long distances, propagation delay and skew uncertainties can pose system design constraints and limit the maximum data rate. The LTC®1685 high speed RS485 transceiver family addresses this problem by guaranteeing over temperature a precision propagation delay of 18.5ns ±3.5ns, a better than ten times improvement over other CMOS transceivers.

The LTC1685 is geared for half-duplex operation, whereas the LTC1686/LTC1687 can operate in full-duplex mode. All include a receiver fail-safe feature, whereby the receiver output remains in a high state over the entire 12V to –7V common mode range when the inputs are left open or shorted together. A novel protection technique permits indefinite short circuiting of the driver and receiver outputs to supply or ground, while limiting the current to 20mA.

HIGH SPEED DIFFERENTIAL SCSI (FAST-20/FAST-40 HVD)

The LTC1685's high speed and tight driver/receiver propagation-delay window make the LTC1685 a natural choice as the external transceiver in high speed (40Mbps) differential SCSI applications. Figure 1 shows a 100-foot passively terminated category 5 unshielded twisted pair (UTP) connection as used in high speed differential SCSI applications. Figure 2 shows a 20ns (50Mbps) pulse propagating down the circuit of Figure 1. Note that in order to achieve these speeds at these distances, it is important to use high quality cable, such as category 5 UTP.

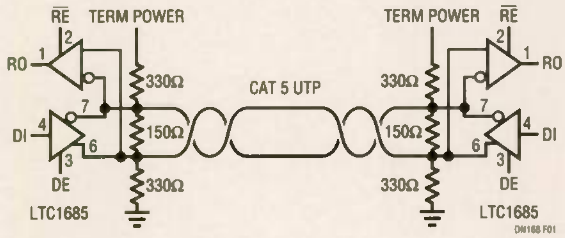

Figure 1. Fast-20/Fast-40 Differential SCSI Application

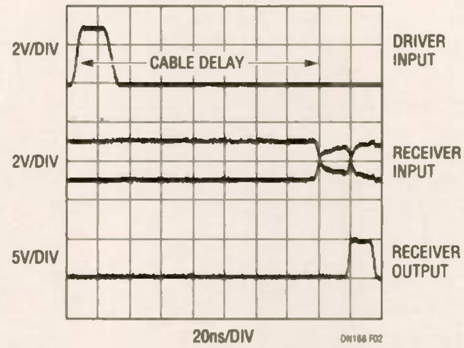

Figure 2. 100 Feet of Category 5 UTP: 20ns Pulse

SCSI applications place strict requirements on the propagation delay variation of its transceivers. For a group of LTC1685 transceivers on the same board, the propagation delay variation will be smaller than the ±3.5ns guaranteed specification. This is because the ±3.5ns propagation delay window covers the entire commercial temperature range, whereas transceivers placed on the same board will have very similar ambient temperatures. Hence, the difference in their propagation delays should be better than the ±3.5ns specification (typically better than ±2ns). This makes the LTC1685 the best choice for high speed SCSI applications.

TRANSMISSION OVER LONG DISTANCES

The LTC1686/LTC1687 can be used as repeaters to extend the effective length of a high speed twisted-pair line. Figure 3 shows a 3-repeater configuration using 2000-foot segments of category 5 UTP.

1Mbps Over 12,000 Feet Using Repeaters

By adding two repeaters to the configuration of Figure 3, we are able to propagate a single 1µs pulse (1Mbps) over 12,000 feet of category 5 UTP. At this data rate and cable lengths, one can obtain minimal pulse width degradation

Note: HVD = High Voltage Differential

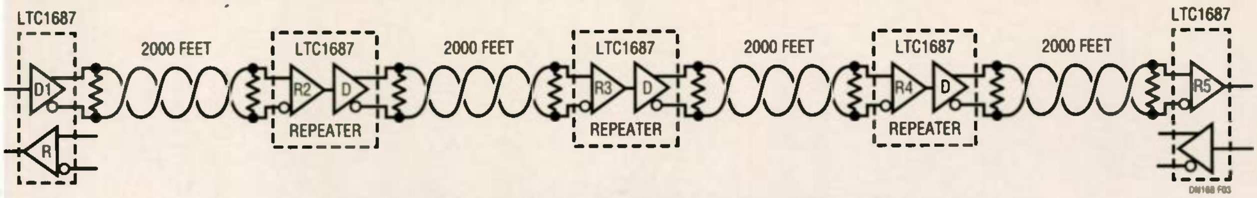

Figure 3. 1.6Mbps, 8000 Feet (1.5 Miles) Using Three Repeaters

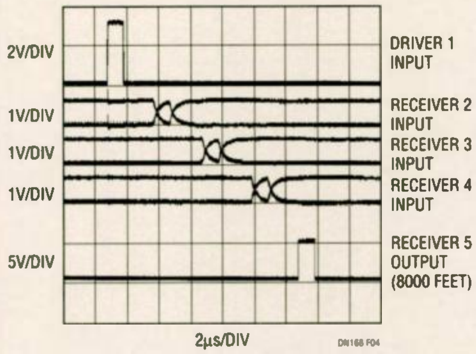

Figure 4. Differential Signals at the Far End of the First Three 2000-Foot Cable Segments

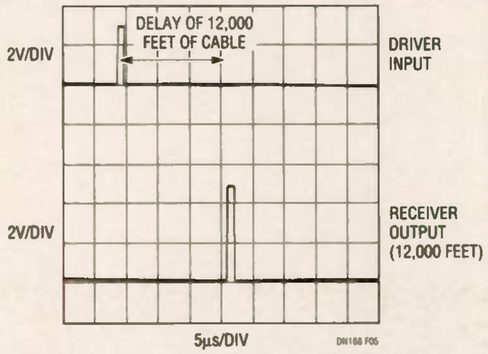

Figure 5. 1µs Pulse Over 12,000 Feet Category 5 UTP

s the signal traverses through the repeater network. igure 4 shows some receiver input and output signals at he far end of the first three 2000-foot cable segments of he network. The DC resistance of 2000 feet of category 5 JTP divides the signal nearly in half. AC losses tend to filter he 1µs pulse. The total attenuation is shown by the middle hree traces of Figure 4. Note, however, that the output ulse (bottom trace) is nearly the same width as the input ulse (top trace), meaning that the LTC1687 repeaters are ble to regenerate the signal with little loss in pulse width. igure 5 shows the waveforms at the near and far end of the ntire 12,000-foot network. The imperceptible loss in pulse vidth implies that we can cascade even more repeater networks and potentially achieve **1Mbps operation at total listances of well over 12,000 feet!**

.6Mbps Over 8000 Feet Using Repeaters

or the same cable distance, high data rates will limit the naximum number of repeaters. Figure 6 shows the propa- jation of a single 600ns pulse through the 3-repeater ietwork of Figure 3. The bottom two traces show a 1.6Mbps quare wave at the input and output of the network, espectively. Notice that the duty cycle does not noticeably legrade, however, there is a degradation of the pulse width is shown in the second trace. Thus, in order to achieve eliable performance at long distances, a compromise nust be reached between cable distance and quality, data ate and number of repeaters.

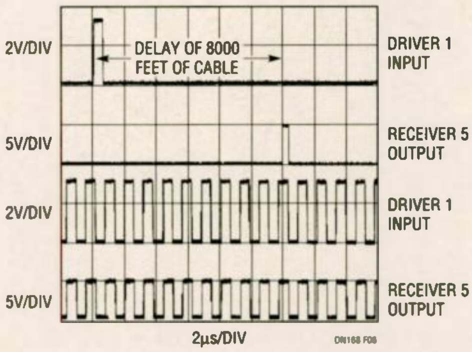

Figure 6. 1.6Mbps Pulse and Square Wave Signals Over 8000 Feet Category 5 UTP Using Three Repeaters

CONCLUSION

The LTC1685 family of high speed RS485 transceivers allows for up to 52Mbps transmission over reasonable distances (100 feet), as well as moderate speed over long distances (1.6Mbps, 2000 feet). Using repeaters can substantially increase the effective length. At 1.6Mbps, three repeaters can carry data a total of 8000 feet and five repeaters can carry 1Mbps data over 12,000 feet of category 5 UTP.

For literature on our RS485 Transceivers, call **1-800-4-LINEAR**. For applications help, call (408) 432-1900, Ext. 2453

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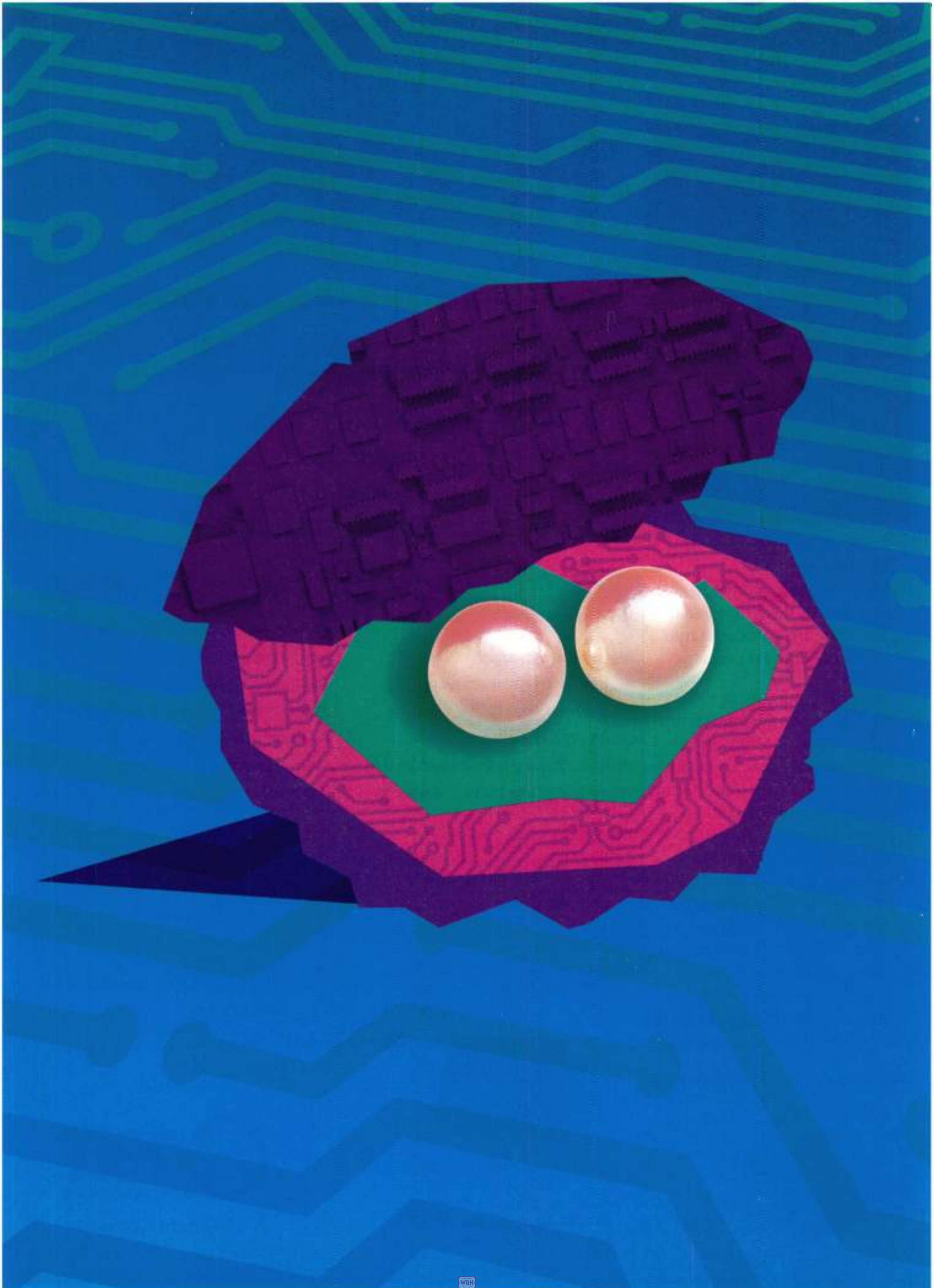

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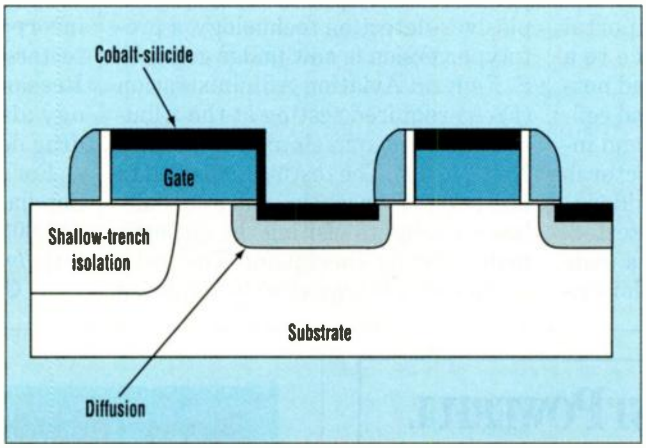
Shrinking Six-Transistor SRAM Cell Size Leads To Larger Embedded Memory

The smallest six-transistor memory cell to date, occupying an area of just 2.912 μm^2, employs a combination of a silicon-nitride visor on a shallow, trench-isolated structure, and a cobalt-salicide direct-strap interconnect. Developed by researchers at the ULSI Device Development Laboratories of NEC Corp., Kanagawa, Japan, the device is made on a 0.18-µm process that reduces the number of manufacturing steps to just one additional mask and one extra etching step. This development, detailed in paper 34.1, is just one of many that will be detailed at next month's IEEE International Electron Devices Meeting, Washington, D.C., December 8-10.

In contrast to the NEC device, other embedded SRAM processes use local interconnections that require one additional metallization and two additional lithography steps, or an implant step and one or or two mask steps. NEC's improved structure promises to simplify the manufacturing process by reducing the number of additional steps needed and reducing the area required by the memory cells. Therefore, more memory can be packed into the same area, and the area of already designed memory arrays can be reduced, allowing designers to shrink the size of their chip.

Such small SRAM cells bode well for advanced microprocessors and system logic functions, graphics processors, and communications subsystem controllers that contain large on-chip caches or interface buffers (FIFOs or LIFOs). Today's 64-bit microprocessors for example, pack 32 to 64 kbytes of on-chip cache, a function that occupies about 40% of the chip area. The trend is to progress to even larger on-chip caches. By reducing by 20% to 40% the area occupied by the memory, either more memory will fit on the same size chip or more logic functions can be added to make a more advanced CPU.



The cobalt-silicide layer on an SRAM cell developed by NEC provides a direct connection between the gate and the diffusion region. This direct link eliminates at least one process step and eases the misalignment tolerances required.

To fabricate the new structure, NEC's researchers use a krypton-fluoride (KrF) excimer laser to define all levels from isolation to second-level metal. After the basic diffusions and the lightly doped drain (LDD) implants are completed, a silicon-nitride sidewall spacer is selectively etched at the desired location for the direct-strap formation. When the cobalt silicidation is performed, the gate and source/drain regions are connected only where the spacer is removed, coupling the gates to the diffusion regions *(see the figure)*. Additionally, the resistance of the contact is low enough that even with misalignments of less than 0.1 µm between the contact and gate, circuits would still function. In contrast, a shared contact that has a diameter of 0.24 µm allows only a 0.04-µm misalignment to maintain a resistance value of less than 100 Ω. That limitation is due to insufficient step-coverage of the sputtered titanium in the contact hole.

The junction leakage to the substrate is lower with the new direct-strap process than with the shared-contact approach by more than an order of magnitude. The shared contact is opened on the LDD region through the sidewall spacer. With the direct-strapping technology, a highly-doped diffusion extends completely under the silicide region.

Another key aspect of the new fabrication process is the use of the silicon-nitride visor on the shallow trench isolation to achieve borderless contacts to the diffusions. The visor prevents the side of the silicon substrate in the trench isolation region from short-circuiting to the diffusion. Only with over-etching the shallow-trench isolation region dielectric for approximately 40 nm, the silicon-nitride visor remains at the edge of the trench after a silicon-nitride LDD spacer is formed. This processing does not interfere with either the CMOS process or the direct-strapping process and promises to reduce leakage currents to the substrate by two orders of magnitude, from 2×10^{-12} to 2×10^{-14}, reducing standby currents and eliminating the need for a contact implant.

Dave Bursky

Sensor-Based Technology To Enable More Exact Explosives-Detection Systems

Identifying individuals who have recently been in contact with a wide variety of explosive chemicals is one of the best defenses against acts of terrorism. This identification is especially crucial in areas such as airports, where hijackings and bombings happen all too often. Thanks to a three-year development effort at Sandia National Laboratory, Albuquerque, N.M., that capability may soon be available. Sandia has been working on an explosives-detection technology for the U.S. Federal Aviation Administration, and is now ready to unveil the results.

Sandia's project is based on a chemical sensor and a unique chemical preconcentrator technology. The latter was originally developed at Sandia as part of its Department of Energy mission to protect critical nuclear weapons facilities. A person standing under a specialized device using the technology will be exposed to a small sample of air. This air is then collected and passed through the chemical sensor (also known as an ion-mobility spectrometer).

The sensor, is fully equipped to recognize the distinct chemical footprints of a variety of explosives. As a result, if the person tested has even the slightest concentration of explosive residue on his or her skin or clothing, the quantity and type of chemical is displayed on an adjacent computer screen.

The explosives-detection portal bares a striking resemblance to a metal detector. It has vents and nozzles located inside the walls and ceiling that facilitate the output and intake of air samples. The detector is fully automated, and can provide instructions to the person being tested. The instructions are given in a male voice and include such directions as "Enter the portal," "Turn left," and "Exit the portal." The entire detection process can be performed quickly, requiring the person being tested to stand inside the detector portal for no more than just a few seconds.

Although specific information about the portal's capabilities—such as the types and quantities of explosives it can detect—are not being disclosed for security reasons. The head researcher on the project, Kevin Linker, says simply that "it is capable of detecting very small concentrations of all explosives of interest."

While, a commercial product has yet to be developed utilizing the explosives-detection technology, a prototype version is now under going U. S. Federal Aviation Administration (FAA)-required testing at the Albuquerque International Airport in New Mexico. The testing, expected to last two to four weeks, will affect airline passengers visiting the airport's main security checkpoint. The test's sample size is expected to comprise over 2000 passengers. The testing is completely voluntary.

When the testing is completed, researchers hope to use the results to gauge passenger acceptance of the technology and to identify any reliability issues that need to be addressed. Additionally, researchers will utilize the information to optimize the detector's performance.

All findings also will be submitted to the FAA, who will use the information to determine the feasibility of licensing and manufacturing the explosives-detection portal technology for use at airports across the country. It is expected that the final commercial version of the technology will be incorporated into current metal detectors as single walk-through units. Researchers claim that the technology also can be adapted for use in drug detection.

For additional information, contact Sandia National Laboratory at (505) 845-0011, or check out its web site at http://www.sandia.gov/News.html.

Cheryl Ajluni

Scientists In Europe Debate The Future Of 0.1-µm And Lower Fine-Line IC Lithographic Processes And Advanced SiGe Devices

A clearer picture of future fine-line IC lithography processes and what kind of silicon-germanium (SiGe) devices lie ahead has emerged from panel discussions and presentations at this year's European Solid-State Device Research Conference (ESSDERC '97), which recently took place near Stuttgart, Germany. Lithography processes with feature sizes of 0.1-µm (100-nm) and less, as well as advanced SiGe devices, were among the hottest topics at the conference. Fifteen out of the conference's 160 technical papers and a one-day workshop dealt with structures made on processes with feature sizes below 0.1 µm, underlying the importance of this subject.

For example, researchers at the University of Liverpool, England, discussed how they built a vertically integrated MOSFET with minimum features of 0.1 µm. The 50-nm-thick gate oxides used were grown by plasma oxidation at temperatures below 150°C. Gate electrode and source materials were made by using a two-stage amorphous silicon deposition process at a temperature of 560°C, followed by a rapid thermal annealing step at 700°C for 30 seconds. The source electrode was realized in a SiGe low-temperature (490°C) process.

To more efficiently handle the short-channel effects that plague MOSFETs made on processes in the 0.1-µm range, scientists at the university of Tohoku in Japan decided not to employ widely used ion implantations. Instead, they opted for a selective epitaxial process with low-pressure chemical-vapor deposition (LPCVD).

The smaller the structure, the more difficult the doping process. In a paper presented by researchers at the University of Dortmund, Germany, the main focus was on doping semiconductors with minimum feature sizes of 50 nm (0.05 µm). The researchers pointed out the problems such fine dimensions bring with them and that static fluctuations of the dopant have a major impact on the entire process. With channel lengths below 0.1 µm, electrical transistor parameters like threshold voltage or maximum transconductance can become worse with the result that even digital circuits can show malfunctions.

The French research institutes LETI and CEA, both of Grenoble, France, compared three 0.75-nm n-channel MOSFETs. In addition to being made by conventional methods, they also used indium and gallium for doping by means of ion implantation, with a constant gate-oxide thickness of 3.5 nm.

TSMC, Hsin-Chu City, Taiwan, and Philips, Eindhoven, The Netherlands talked about 0.5-µm processes they de-

veloped (which may go to 0.1 µm) for flash memories. In the read mode, the memories only require a single voltage supply of 1.8 V. They use bidirectional Fowler Nordheim tunneling for erasing as well as for programming. Erasing and programming of single cells require 10 and 5 ms, respectively. When programming the memories in the page mode, the scientists achieved programming times of 5 µs per bit, and every single cell was able to survive for more than 100,000 write/erase cycles.

Scientists at ESSDERC '97 also discussed what types of directions lithography processes will take: Will they be optical? Ion-beam? Or a projection electron approach such as SCALPEL? Or combinations of all three? "The battle for 100-nm lithography is not decided yet," says Professor Dr. Bernd Hoeflinger, the Institut fuer Mikroelektronik (IMS), Stuttgart, Germany, which organized the conference with the University of Stuttgart.

The topic was well represented at the conference with 10 papers devoted to it. By using SiGe compounds, it is possible to realize concepts in silicon that were only possible with III/V semiconductors until now. According to studies performed at the Universities of Southampton and Liverpool, England, and the University of Bilbao, Spain, SiGe is well-suited for realizing I^2L logic in high-performance applications requiring low-power consumption needed for mobile applications.

In a joint paper, the universities' representatives presented their first results of integrated SiGe injection logic circuits. Actual gate-delay measurements achieved were very close to the results of the simulations performed, while all the devices were made were made with a switching time per gate in the 100-ns range. According to the simulations, a 1.2-µm process allows for the realization of SiGe I^2L circuits with a minimum gate delay time of 20 ps.

Representatives of the University of Ulm, Germany, and of Temic, Heilbronn, Germany, used a SiGe heterojunction bipolar transistor (HBT) production process to make a 1.8-GHz amplifier requiring 4.6 mA at 3.6 V. Its minimum noise is 1.9 dB with 20dB gain.

Growing SiGe on silicon wafers allows devices to handle even higher frequencies. For example, the Semiconductor Technology Division of the Electronics and Telecommunications Research Institute (ETRI), Taejon, Korea, reported on a SiGe preamplifier with a bandwidth of 9 GHz. National Semiconductor, Sunnyvale, Calif., investigated the effects of processing temperatures on device design rules for SiGe HBTs. As professor Dr. Hoefflinger of the IMS points out, SiGe will be of high interest for future thin-film-transistor (TFT) displays as well. However, this will not be because of its ability to handle high speeds, but rather due to its ability to work at low temperatures.

For further information about the conference and upcoming events, or to order the conference proceedings, contact Andrea Zinsinger at the IMS, Allmandring 30a 70569 Stuttgart, Germany; telephone +49 (711) 685-5860; fax +49 (711) 685-5930; e-mail: zinsinger@mikro.uni-stuttgart.de.

Alfred Vollmer

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Device	CPU	Flash	Memory	Timer	Peripherals	Package
68HC912B32	16-bit	32K	1K SRAM, 768 EEPROM	16-bit	A/D, PWM, SCI, SPI	80 QFP
68HC916R1	16-bit	50K	2K SRAM	CTM	2 SCI, SPI	132 PQFP
68HC916X1	16-bit	50K	2K SRAM	GPT	A/D, PWM, 2 SCI, SPI	120 QFP
68HC916Y1	16-bit	48K	4K SRAM	TPU, GPT	A/D, SCI, SPI	160 QFP
68F333	32-bit	64K	4K SRAM	TPU	A/D, SCI, QSPI	160 QFP

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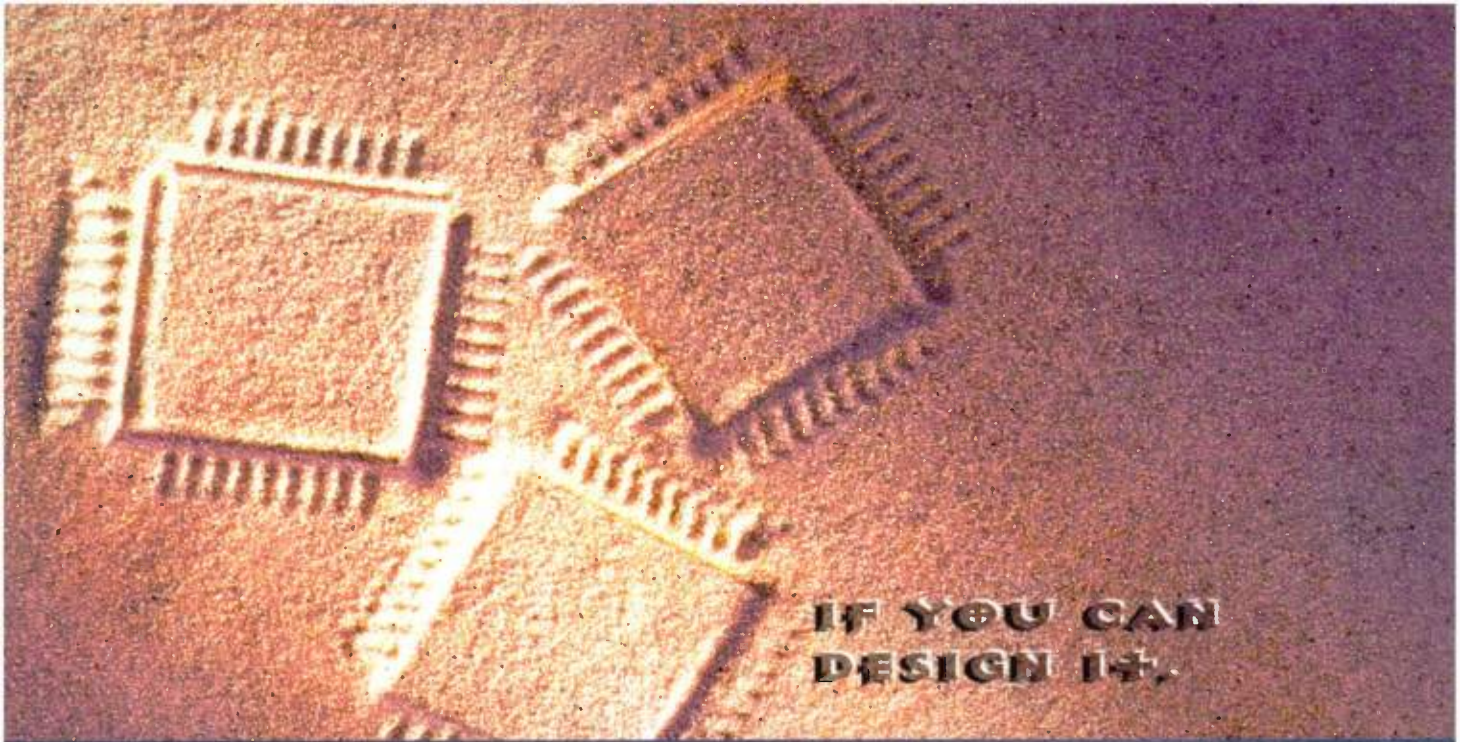
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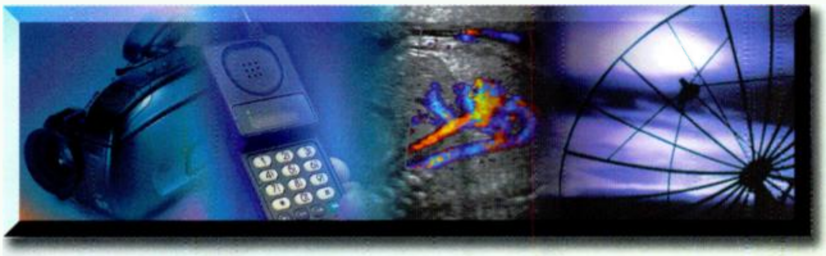
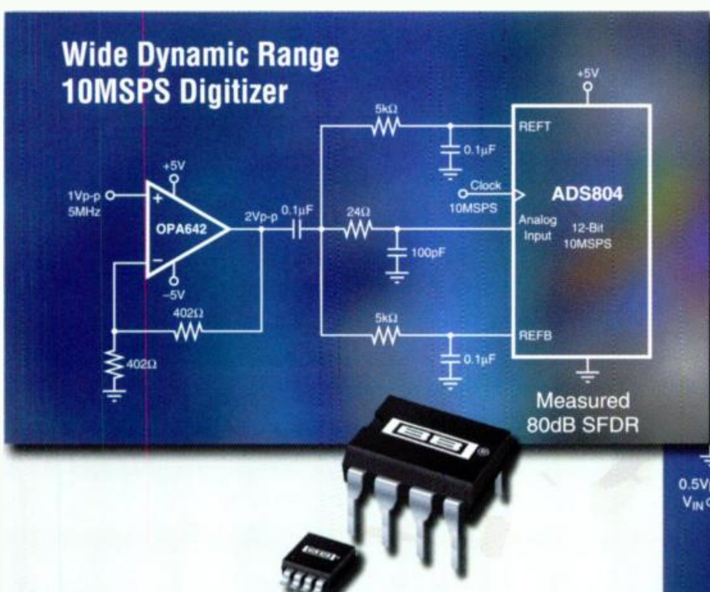
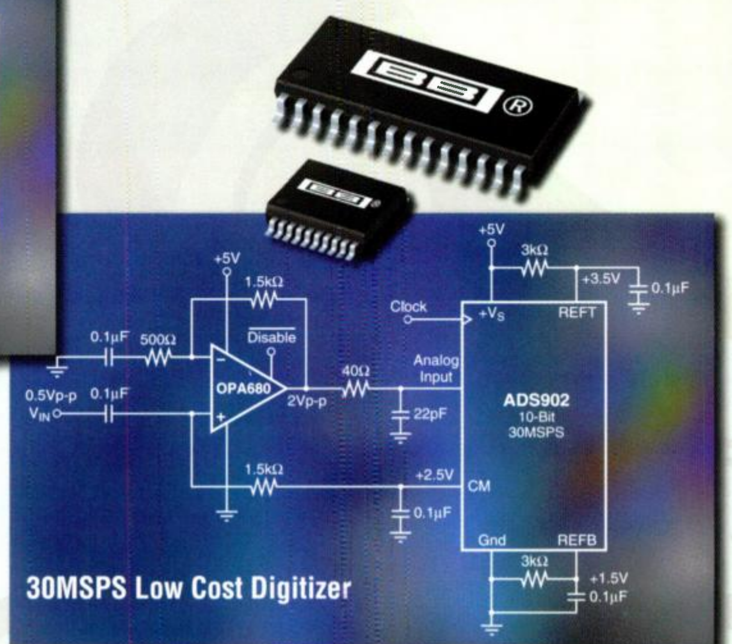


Burr-Brown *SpeedPLUS* A/D Converter Products

Product	Resolution (Bits)	Sample Rate (MHz)	f_{IN} (MHz)	SNR (dB)	SFDR (dB)	DLE (LSB)	Power (mW)	Supply (V)	Ref	Packages[(1)]	Price (1Kpcs)
f_S>5MHz											
ADS800	12	40	12.5	62	61	±0.4	390	+5	Int	E,U	$29.00
ADS801	12	25	5	65	61	±0.3	270	+5	Int	E,U	$20.55
ADS803	12	5	2	69	82	±0.25	114	+5	Int	E,U	$9.55
ADS804	12	10	4.8	69	80	±0.3	180	+5	Int	E,U	$10.95
ADS805	12	20	8	67	77	±0.25	285	+5	Int	E,U	$16.95
ADS820	10	20	10	60	63	±0.2	195	+5	Int	E,U	$6.36
ADS822	10	40	10	60	70	±0.5	161	+5	Int/Ext	E	$6.80
ADS823	10	60	10	60	75	±0.5	265	+5	Int/Ext	E	$8.50
ADS824	10	75	10	59	70	±0.5	315	+5	Int/Ext	E	$9.95
ADS830	8	60	10	50	68	±0.5	180	+5	Int/Ext	E*	$4.95
ADS831	8	80	10	49	67	±0.5	265	+5	Int/Ext	E*	$7.95
ADS900	10	20	10	50	53	±0.7	52	+3	Int	E	$5.70
ADS901	10	20	9	54	51	±0.9	48	+3	Ext	E	$5.65
ADS902	10	30	12.5	57	58	±0.3	140	+5	Ext	E	$6.65
ADS930	8	30	12.5	46	51	±0.4	66 at 3V	+3/+5	Int	E	$3.37
ADS931	8	30	12.5	48	49	±0.5	63 at 3V	+3/+5	Ext	E	$3.27

NOTE: (1) *E=28-pin SSOP   E*=20 Lead QSOP   U=28-pin SOIC • Bold face = New Products*





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Precision A/D Converters

Burr-Brown A/D Converter Products

Product	Res. (Bits)	Sampling Rate (kHz)	# Chan.	Interface	Type	Linearity (%)	NMC[1] (Bits)	SINAD (dB)	Power (mW)	Packages[2]	Price (1Kpcs)
f_s<5kHz											
ADS1201	24	0.01	1 Diff	Modulator	DeltaSig	±0.0015	24	–	10	E,P,U	$5.76
ADS1210	24	0.01	1 Diff	Serial	DeltaSig	±0.0015	24	–	60	P,U	$9.60
ADS1211	24	0.01	4 Diff	Serial	DeltaSig	±0.0015	24	–	60	E,P,U	$10.52
ADS1212	22	0.01	1 Diff	Serial	DeltaSig	±0.0015	22	–	1.4	P,U	$7.25
ADS1213	22	0.01	4 Diff	Serial	DeltaSig	±0.0015	22	–	1.4	E,P,U	$8.50
ADS1214	22	0.01	1 Diff	Serial	DeltaSig	±0.0015	22	–	1.4	P,U	$7.25
ADS1215	22	0.01	4 Diff	Serial	DeltaSig	±0.0015	22	–	1.4	E,P,U	$8.50
5kHz<f_s<50kHz											
ADS574	12	40	1 SE	Parallel	SAR	±0.012	12	70	100	P,U	$12.45
ADS7806	12	40	1 SE	Parallel/Serial	SAR	±0.012	12	72	35	P,U	$9.47
ADS7807	16	40	1 SE	Parallel/Serial	SAR	±0.0022	16	86	35	P,U	$25.75
ADS7812	12	40	1 SE	Serial	SAR	±0.012	12	72	35	P,U	$9.25
ADS7813	16	40	1 SE	Serial	SAR	±0.003	16	87	35	P,U	$20.00
ADS7824	12	40	4 SE	Parallel/Serial	SAR	±0.012	12	72	50	P,U	$12.30
ADS7825	16	40	4 SE	Parallel/Serial	SAR	±0.003	16	86	50	P,U	$28.46
50kHz<f_s<200kHz											
ADC700	16	59	1 SE	Parallel/Serial	SAR	±0.006	13	–	765	H	$69.60
ADS774	12	117	1 SE	Parallel	SAR	±0.012	12	68	120	P,U	$16.95
ADS7804	12	100	1 SE	Parallel	SAR	±0.012	12	72	100	P,U	$11.00
ADS7805	16	100	1 SE	Parallel	SAR	±0.0045	16	86	100	P,U	$20.50
ADS7808	12	100	1 SE	Serial	SAR	±0.012	12	72	100	P,U	$9.95
ADS7809	16	100	1 SE	Serial	SAR	±0.003	16	86	100	P,U	$20.50
ADS7816	12	200	1 Diff	Serial	SAR	±0.024	12	72	3.5	E,P,U	$5.33
ADS7817	12	200	1 Diff	Serial	SAR	±0.024	12	71	4	E,P,U	$5.18
ADS7820	12	100	1 SE	Serial	SAR	±0.012	12	72	100	P,U	$10.25
ADS7821	16	100	1 SE	Parallel	SAR	±0.0045	16	86	100	P,U	$27.47
ADS7822	12	75	1 Diff	Serial	SAR	±0.018	12	71	0.54	E,P,U	$4.64
ADS7832	12	117	4 SE	Parallel	SAR	±0.024	12	69	3.5	P,N	$16.00
ADS7833	12X3	150	10 Diff	Serial	SAR	±0.018	12	–	125	N	$23.75
ADS7841	12	200	4 SE	Serial	SAR	±0.024	12	72	3.5	E	$5.59
ADS7842	12	200	4 SE	Parallel	SAR	±0.024	11	70	3.5	E	$6.21
ADS7843	12/8	200	4 SE	Serial	SAR	±0.048	11	–	3.5	U	$4.95
200kHz<f_s<500kHz											
ADS7800	12	333	1 SE	Parallel	SAR	±0.012	12	69	215	H	$23.95
ADS7811	16	250	1 SE	Parallel	SAR	±0.006	15	86	250	P,U	$24.75
ADS7815	16	250	1 SE	Parallel	SAR	±0.006	15	84	250	U	$20.00
ADS7818	12	500	1 Diff	Serial	SAR	±0.024	12	70	10	E,P,U	$6.25
ADS7852	12	500	8 SE	Parallel	SAR	±0.024	12	72	3.5	P,U	$7.50
500kHz<f_s<5MHz											
ADS7810	12	800	1 SE	Parallel	SAR	±0.018	12	69	250	P,U	$23.75
ADS7819	12	800	1 SE	Parallel	SAR	±0.018	12	70	275	P,U	$12.20
ADS7831	12	600	1 SE	Parallel	SAR	±0.024	12	69	275	P,U	$11.42

NOTES: (1) No Missing Codes (2) *U=SOIC E=SSOP N=PLCC P=PDIP H=Ceramic • Bold face = New Products*

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The Rise Of Multimedia PCs Taxes The Graphics Subsystem

Today's Graphics Processor Must Handle 2D and 3D Acceleration As Well As Video.

RON DRAFZ, JOHN REDER, AND STEVE ROGERS, Texas Instruments Inc., P.O. Box 660199, MS 8711, Dallas, TX 75266; (972) 480-3462.

The term "multimedia" has been bandied about the electronics industry for nearly a decade. During that time, the concept of multimedia has evolved to include a wider range of base-level technologies that make the PC a viable platform for a wider range of experiences. This, in turn, attracts a wider range of users.

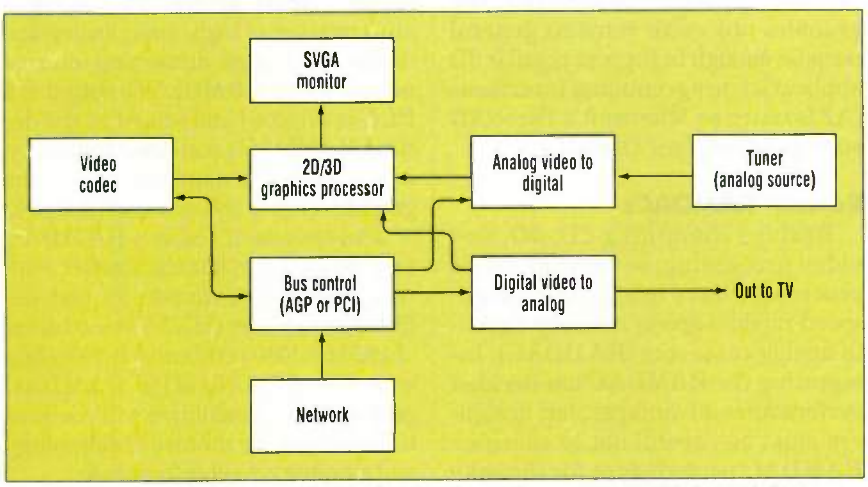
Today, a great deal of effort is being exerted to improve the visual content of the PC. Capabilities such as three-dimensional (3D) graphics engines, two-dimensional (2D) accelerators, and enhanced video processing are challenging PC system designers with functionality previously unattainable in business and consumer PCs. On the other hand, change in one place in an architecture may have adverse effects in other parts of the system.

Today, the traditional multimedia PC is being enriched with what are considered as "entertainment capabilities." Flat, unresponsive graphics; fuzzy, out-of-synch video; and hollow-sounding audio will soon be unacceptable. Users will increasingly be bringing real-time video images and other resource-demanding data streams into PCs. And new business applications, such as videoconferencing, personnel training using virtual-reality simulation, and video image editing will further spur the spread of entertainment-oriented multimedia PC capabilities.

"The PC98 Hardware Design Guide," co-authored by Intel and Microsoft, defines a robust set of multimedia requirements and recommendations for PCs in the near future. For example, all systems are required to support 3D graphics acceleration, and many also are expected to include video features such as tuners, analog video capture, television outputs, and digital video disk (DVD) playback.

Looking at the generic building blocks needed to handle the enhanced visual content multimedia PCs will be asked to process, the graphics processor becomes a central focus point *(Fig. 1)*. A robust, fully featured graphics processor is critical to successfully enabling next-generation multimedia PCs.

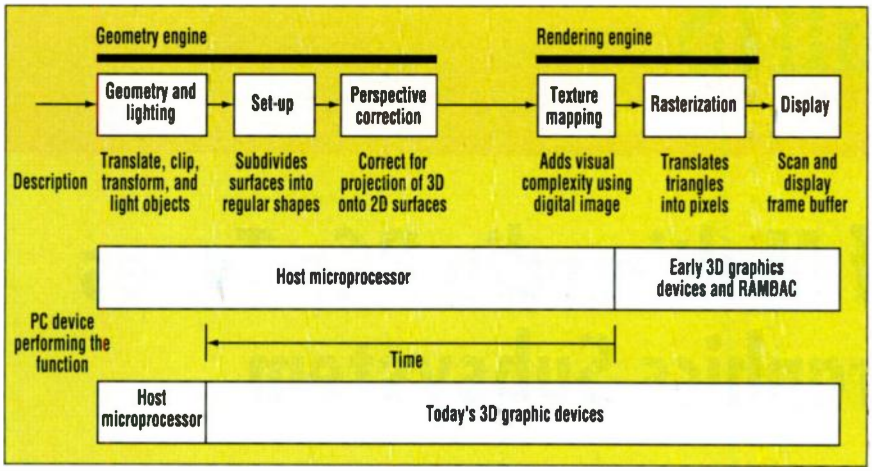
Today's crop of graphics engines bring the visual realism previously found only in high-end workstations to business and consumer PCs. This class of graphics processor combines three distinct functions: high-performance 3D, 2D acceleration, and advanced video processing. These new integrated graphic processors balance high-quality, 3D polygon and textured graphics acceleration, Windows acceleration, and MPEG-1/MPEG-2 video playback with an integrated Super VGA core. They also add an integrated RAMDAC and video ports.



1. Today's graphics board looks different than one from a few years ago. This is partly because it's now asked to handle 3D graphics and video. The data bus is either PCI or AGP.

Multidimensional To The Core

By combining 3D, 2D, and video operations in the same graphics core, these processors provide additional flexibility in data handling and assure



2. Graphics devices have continued to absorb more of the 3D pipeline over time. The 3D graphics pipeline takes a 3D model of the desired scene and transforms it into individual pixels for display on a 2D monitor.

no duplication of functionality.

The 3D graphics pipeline takes a 3D model of the desired scene and transforms it into individual pixels for display on a 2D monitor *(Fig. 2)*. Some of the earliest 3D graphics processors only performed the rasterization step, while a separate RAMDAC performed the display function. This left the remaining computational-intense steps to the PC's host CPU, which significantly limited overall 3D performance. Over time, graphics processors have continued to absorb more of the 3D pipeline, providing true hardware acceleration.

Today, the best mainstream graphics processors even include the set-up function, leaving only the geometry and lighting functions to the host. This evolution has significantly improved 3D performance, providing better image detail with higher frame rates. Having this sort of set-up engine on-chip significantly reduces the processing load on the host CPU and system bus, typically a PCI bus or accelerated graphics port (AGP).

New graphic-processor cores are capable of a high degree of parallelism which allows several pixels to be processed concurrently. This type of design ensures a high throughput while maintaining low latency between primitives. An advanced graphics engine normally won't require that one primitive be processed completely before the next can begin processing.

Some graphics processors can further reduce their processing load by not wasting time processing pixels that won't be written to memory. The processor accomplishes this by first rasterizing each primitive to determine the pixels that it covers on the screen, and then putting each pixel through a sequence of operations. As the pixel is put through this sequence, if it fails any of the tests along the way, it will not take part in any further processing. For example, if a pixel fails the depth test, it won't have a texture address calculated for it, nor will it have texture data read from memory and applied.

In addition to accelerating 3D, today's advanced graphics accelerators must be highly optimized for legacy graphics operations such as block transfers, raster operations, DOS graphics modes, and linear and planar memory addressing. Even today's most advanced Windows-based computers boot up in VGA mode, requiring that a VGA core be included in every graphics chip. It's also important to note that the graphics processor remains general purpose enough to support popular 3D application programming interfaces (APIs) such as Microsoft's Direct3D and Silicon Graphics' OpenGL.

Rockin' RAMDACs

Besides combining 2D, 3D, and video processing, several graphics processors have integrated a high-speed random-access memory digital-to-analog converter (RAMDAC). Integrating the RAMDAC has decided performance advantages, but designers must be careful not to sacrifice RAMDAC performance for the sake of an integrated graphics processor. The RAMDAC's speed has a critical effect on the display's refresh rate. If the speed is inadequate, the monitor won't be able to quickly shift images or display fast-moving images. In addition, the RAMDAC should support a wide range of screen resolutions from 320 by 200 to 1600 by 1200 pixels, and refresh rates from 60 to 100 Hz. The RAMDAC also dictates whether the color depth will be 8, 16, 24, or 32 bits.

The graphical nature of multimedia PCs increases the demands placed on the RAMDAC. For example, today's typical 17-in. monitor supports 1280 by 1024 pixels with 16 bits/pixel of color resolution at a 75-Hz refresh rate. This requires a 135-MHz RAMDAC with a 64-bit wide-pixel data bus feeding data at a rate of 197 Mbytes/s to the RAMDAC. However, 21-in. monitors support 1600 by 1200 pixels with 24 bits/pixel of color resolution at an 85-Hz refresh rate. This requires a 250-MHz RAMDAC with a 128-bit-wide pixel data bus feeding data at a rate of 653 Mbytes/s to the RAMDAC.

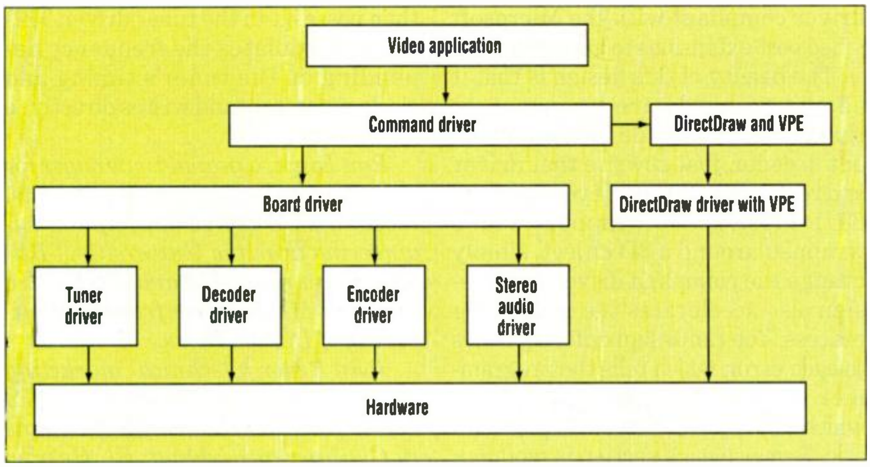
RAMDACs actually output more data than can be seen on a display. About 40% of the bandwidth is thrown away. These high data rates have forced the integration of RAMDACs with the 2D/3D graphics engine. The data bus widths and speeds demand integration; otherwise, pin counts would make device packaging prohibitively expensive.

PLLs To The Rescue

Speeds of this sort require phase-locked loops (PLLs) to generate stable clocks for the integrated RAMDAC, internal graphics-processor logic, and external memory devices. PLL designs are a mixture of high-speed analog and digital technology supporting internal rates of 100 to 450 MHz. The output of a PLL is selected and scaled to the desired RAMDAC pixel-clock frequency, as well as to the required rates of the graphics engine and external memory.

The speeds of today's RAMDAC may be dizzying, but the market is already demanding support for high-definition television (HDTV) resolutions of 1920 by 1080 pixels and RAMDACs with speeds of 270 MHz. RAMDAC performance capabilities will continue to be driven by monitor technology and monitor price/performance.

Until now, a PC's graphic-processing capabilities have taken precedence



3. The software element of the graphics subsystem can help or hinder performance. Tasks can be sectionalized to specific code segments using object-oriented programming.

over its video handling facilities. This is about to change. How PCs import and manipulate both live and stored video signals will become increasingly important for users as new peripherals such as DVDs, digital cameras, and digital satellite broadcasting services gain in popularity.

Video decoders and encoders play the role of video signal gatekeepers for the PC by converting analog video signals into digital signals for processing by the PC's graphics processor *(Fig. 1, again)*. The digital signals are then reconverted into analog signals that can be displayed on analog video equipment like a TV or stored on a VCR.

But, a new breed of video decoders is emerging. Essential to these decoders is the high-quality video imaging that they allow on a PC display. Some decoders have a number of features that assure high-quality analog-to-digital video conversions. For example, performing comb filtering on both the luminance (brightness) and chrominance (color) paths that traverse a decoder dramatically improves the preservation of detail in the image.

Previous-generation decoders have only done comb filtering on the chrominance path, or on neither path. Some older decoders without comb filtering eliminated large amounts of picture detail while simultaneously introducing distortions into the image. Another advanced feature that must be supported by both the video decoder and video encoder is genlock, which produces accurate and high-quality colors in images even when the video input comes from a source with unstable clock timings.

On the output side, a video encoder converts the digital graphic information from the graphics processor into analog signals for outputting to a television. Here, a host of new capabilities bring the quality of PC video on a par with consumer-electronics systems. For example, a flicker filter is an important part of the encoder if the flicker often experienced on interlaced TV screens is to be eliminated. Computer imagery designed for display on a progressive-scan monitor often contains fine lines, which flicker when displayed on an interlaced TV. A flicker filter smoothes these lines while maintaining adequate detail.

Televisions truncate about 5% of the incoming video signal, commonly referred to as overscanning. Conversely, computer monitors display the entire image, so the graphics device must fill the entire monitor with information. Therefore, if a computer image is displayed on a TV, critical information may be lost. Today's more advanced encoders include an overscan compensation filter to scale computer imagery for display on a TV.

If the digital-to-analog converter (DAC) in a video encoder doesn't have adequate precision, another distortion (contouring) can occur. Contouring, which marks the transitional areas from one color to another with visible lines resembling the lines of a contour map, can be eliminated when the encoder has a DAC that's capable of at least 10 bits of precision.

With the advent of DVD, which supplies video source material to users in a digital form, excellent reproductions could be copied by recording the output of the video encoder onto a VCR tape. Macrovision was developed to prevent these attempts at piracy. It adjusts the video synchronization signals so that the VCR can't lock onto and record the signal while simultaneously allowing the user to view the video content on a normal TV. This technology is becoming a required feature of all video encoders used to view digital content.

Glueless, Not Clueless

In many designs, glue logic is used to convert, modify, amplify, or buffer signals as they are passed from one functional hardware block to another. Each glue logic device adds cost to a cost-sensitive end product. In addition, each piece of glue logic adds time to the design of a product that competes in the PC whirlwind market.

Fortunately, digital-video and graphics-device manufacturers have begun to adopt standards that provide seamless interfaces. Many of these devices currently utilize either a VMI or ITU-656 digital interface, which reduces many compatibility issues. The VESA Video Port committee is expected to soon adopt a common digital video interface standard, probably based on the Video Interface Port (VIP) proposal. The VIP combines features of both the VMI and the ITU-656. Once this standard is adopted and implemented, digital-video and graphics devices should all be compatible with one another.

The Soft Underbelly

Underlying all of these hardware challenges and concerns is the software—perhaps the ultimate "Gotcha!" In the ever-changing world of software device drivers, the one in use today will always be superseded by another faster driver. The question becomes: How easily and effectively can the system cope with new software as it becomes available? A modular, object-oriented driver structure will help alleviate some of this problem by allowing drivers to be slotted into or removed from the overall software architecture.

Another software concern is how efficiently will device drivers interact with the system's operating environment. A slight hiccup between the driver and the operating system can become a major bottleneck to data throughput. Only a seamless data flow will optimize the potential of the underlying hardware. To some extent, data-flow problems can be avoided by conforming to the requirements of the operating system and the APIs. However, even standards compliance is no substitute for sound software design.

Good object-oriented programming will sectionalize tasks to specific code segments. When the video application becomes the end-user interface, the programmer can choose different styles for the graphical-user interface (GUI) *(Fig. 3)*. The command driver issues commands to the board driver and uses video-port extensions to display the streaming video. The individual chips are all handled by the board driver. Each chip, tuner, decoder, encoder, and audio has its own driver to map certain characteristics like brightness, contrast, NTSC format, and change frequency. In addition to these drivers, the graphics-card maker must write a driver compliant with the Microsoft video port extensions to DirectDraw.

The beauty of this design is that it adapts to hardware upgrades or changes. If you decide to use a different decoder, just rewrite that driver and replace the old one. If you want the GUI interface to support video wrapped around a 3D object, simply change the command driver. This design also accelerates the debugging process. You can assign different codes to each error, which tells the programmer writing the video application which of the lower drivers is problematic. Because each section is modular, driver updates also can be modular.

To examine how these drivers interact, follow how the user may change TV channels. The user will select a channel from 1 to 125 depending on what channels are enabled. Then, in the command driver, the selected channel is converted to a channel frequency, depending on the format (NTSC, PAL, or SECAM) and band (standard or cable). It then passes this information to the board driver, who then passes it to the tuner driver. This driver modulates the frequency depending on the tuner's timing and clock generators and writes directly to the device.

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Optimizing DSP-Based System Design For Real-Time Applications

Dual DSP's, novel debugging techniques, and a structured hardware-software integration method help speed the design process.

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Real-time signal-processing systems are a significant challenge to designers. Common issues include the memory size to DSP MIPS trade-off, I/O strategy, debugging capability, and hardware/software integration. As we shall see, there are new techniques which together allow a smoother, more predictable path to a successfully working system. Throughout this article, the implementation of a Dolby Digital audio decoder[1] is used to illustrate the techniques (see "Dolby Digital—An Overview," p. 54).

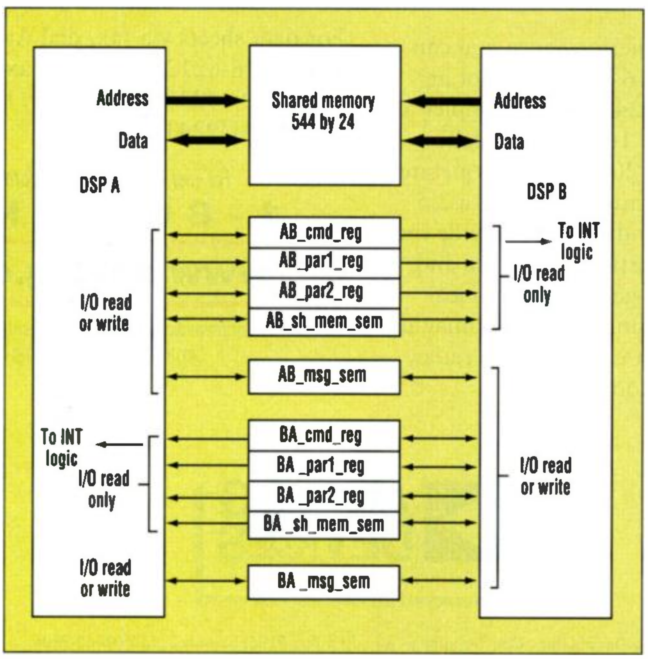
Design Requirements

Analysis of the system requirements is crucial to beginning the design process. A top-down design approach is recommended, specifying the hardware requirements based on a good understanding of the application, particularly the software implementation. Typical audio algorithm-dependent requirements are processor speed, memory, precision (resolution), dynamic range, and distortion. Apart from overdesigning the system, the only way to get a confident design architecture is to begin with a tentative hardware platform, and actually develop first-generation DSP code. The first-pass design is then improved by iteratively refining the hardware and software specifications until the design trade-offs are satisfactory. Examples of such iterations include choosing special hardware for cyclic redundancy check (CRC) calculation or using optimized DSP instructions.

In most audio decompression tasks, including Dolby Digital, the algorithm consists of two major stages:

1. Parsing the input bit stream with specified/computed bit allocation, and generating frequency-domain transform coefficients for each channel
2. Performing the inverse transform to generate time-domain pulse-code modulation (PCM) samples for each channel

After generating initial DSP code for each major module, the MIPS (processor usage) and memory requirements can be estimated. In addition, the bandwidth, scheduling, and type of data flowing from one module to the next also is known. The first-generation DSP code also reveals the dynamics of the overall decode process, which are very important in determining the scheduling of tasks, and thereby the intertask communication requirements.

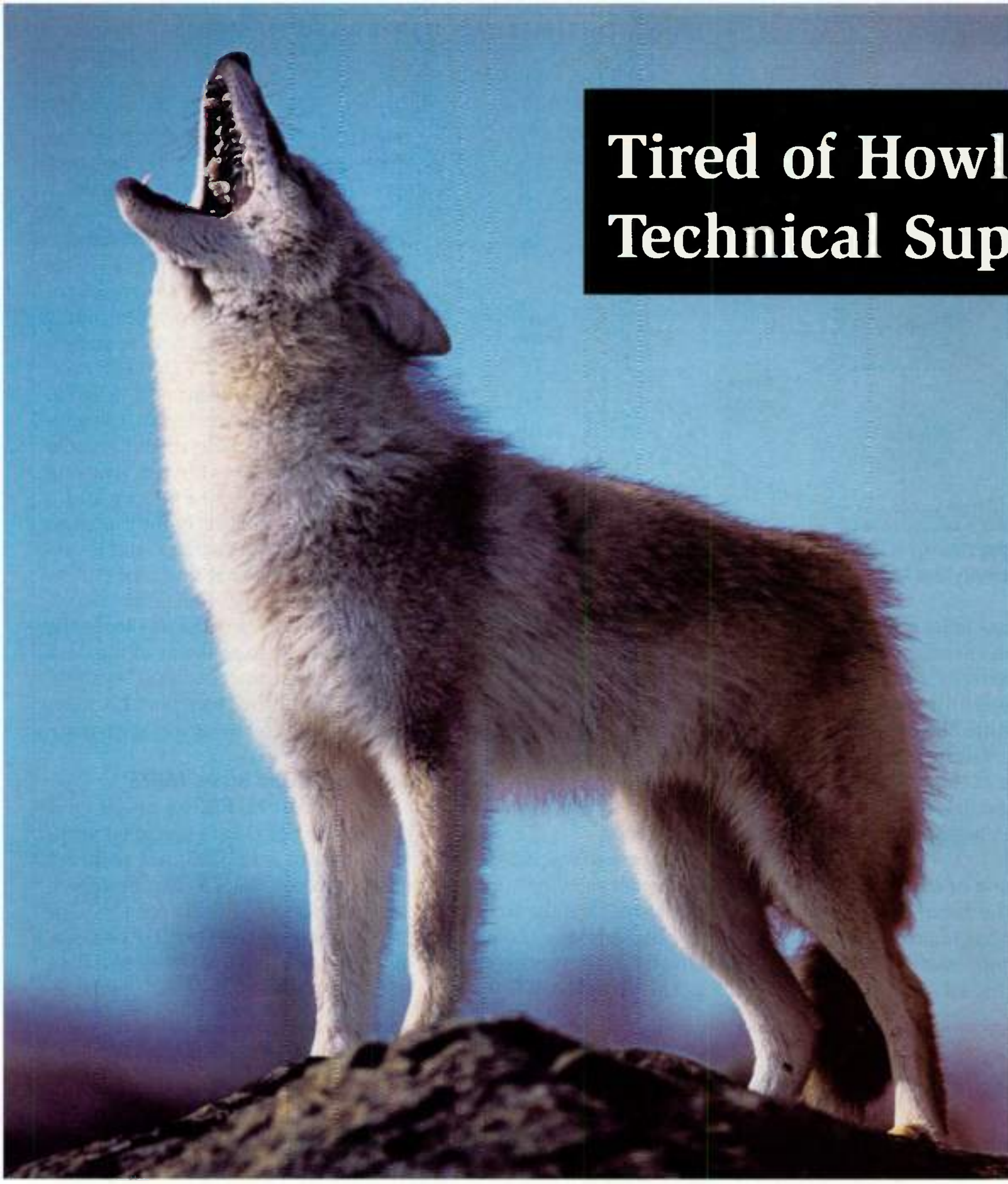


1. The figure shows how shared memory and message semaphore registers control the communication channels between the two DSPs.

MIPS Vs. Memory

A careful balance must be obtained between memory and available processing bandwidth utilization. Typically, memory can be saved by using more MIPS or MIPS could be saved by using more memory.

An example of such a trade-off in the Dolby Digital decompression process is in the decoding of the exponents for the sub-band transform coef-



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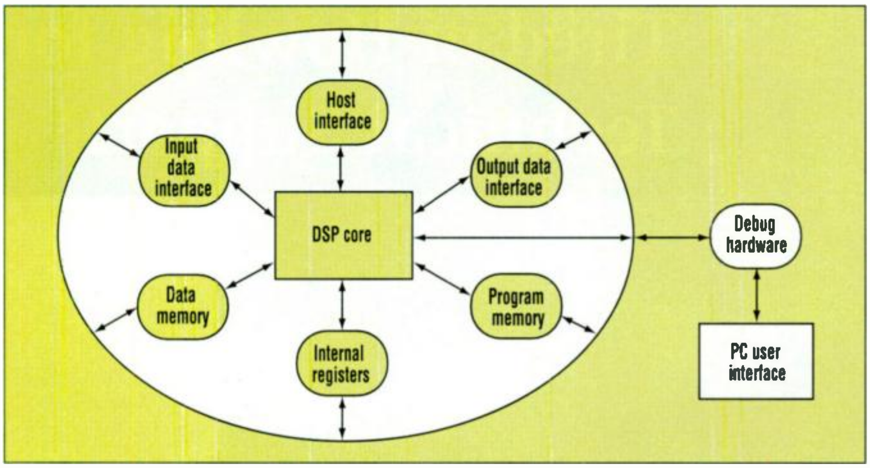


2. A conventional debugging strategy is illustrated here. While cumbersome, it does provide access to the DSP core, memory, and I/O.

ficients. The exponents must arrive in the first block of the encoded frame and may or may not arrive for the subsequent blocks, depending on the reuse flags. But, within the block itself, six channels are multiplexed, and the exponents arrive in the bitstream compressed (block coded) for all six channels, before the mantissas of any channel are received.

The decompression of exponents has to happen for the bit allocation process as well as scaling of mantissas. However, once decompressed, the exponents might be reused for subsequent blocks. In this case, they would be stored in a separate array (256-by-24-bit elements for six channels equals 1536 memory locations). On the other hand, if exponents are stored in compressed form (only 512 memory locations), decompression would be required for the subsequent block, even if the reuse flag is set.

The second approach was chosen for two reasons: memory savings (in this case, 1 kwords saved) and the fact that in the worst-case scenario, the exponents have to be decompressed for every block. Therefore the MIPS allocated must be large enough to meet the worst-case scenario, allowing the use of spare MIPS under better conditions.

Input FIFOs Save System Cost

Designing the proper input FIFO is important not only for the correct operation of the core DSP system, but it can simplify the overall system design. For example, in a TV set-top box, where encoded audio is multiplexed in an MPEG2 transport stream, the minimum buffering requirement for audio (per MPEG spec) is 4 kbytes. By using an 8-kbyte input FIFO, any audio bursts from a correctly multiplexed MPEG2 transport stream can be accepted, meaning that no extra buffering is required upstream in the demultiplexer chip. This design allows the demultiplexer to pass any audio data directly to the decoder DSP system, regardless of the transport bit rate, thereby reducing overall system cost.

Output FIFOs Save MIPS

Significant MIPS can be saved if the output FIFOs are designed properly. The output FIFOs act as direct memory access (DMA) engines, feeding decompressed audio data to digital-to-analog converters (DACs). Audio converters require their input data to be at a fixed sample rate, with no

Dolby Digital—An Overview

Originally developed for broadcast television audio, Dolby Digital (formerly AC3) is an audio coding technique that allows multi-channel, high-fidelity audio information to be transmitted over a low-bandwidth channel, or stored on a medium where audio data space is at a premium. The coding technique converts the sound into frequency bands.

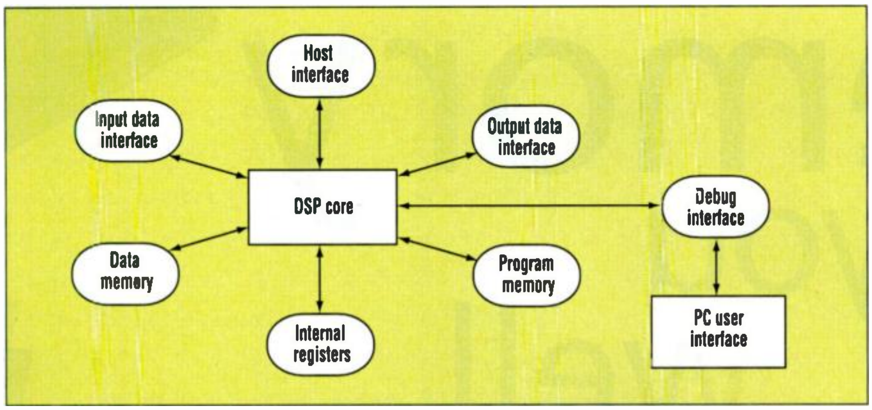
The human ear cannot perceive sounds which are close in frequency to a loud sound. The coding algorithm takes advantage of this by removing the masked sounds, according to a set of threshold curves which model the masking behavior of the ear. For each frequency band, because the inaudible information has been removed, fewer bits are now required to represent the sound.

For a given block of sound, the available bits for transmission are allocated amongst the frequency bands depending on the particular characteristics of the spectrum. This process is continuously changing, varying as the program material varies.

The normal output of a Dolby Digital decoder is six channels of audio: front right, front left, front center, rear right, rear left, and a nondirectional bass subwoofer channel (known as 5.1 channels). In some playback scenarios, traditional two-channel stereo or mono, playback may be required. The decoder has to be able to create a correctly balanced stereo or mono output, from the original 5.1 channels.

Dolby Digital includes a method of setting the dialog level to a consistent level for different program sources. The decoder also has to handle the control of dynamic range, using a compression technique. This technique allows both the loud and the quiet sections of a program to be heard when the overall volume level is set low.

The processes required by a Dolby Digital decoder include parsing the incoming bitstream to detect the synchronizing information and other additional information about the audio data, error checking using CRC, dequantizing using the bit-allocation information, and a frequency to time domain transform algorithm. Because the audio data is usually streamed in real time, the decoding processes have to occur within a strict time budget.



3. This simplified debugging strategy employs a two-wire port and a debug interface to gain access to the DSP and other necessary points. By using this method, the designer gains real-time capability.

missed samples allowed. Without output FIFOs, the DSP has to be interrupted at the sampling frequency (Fs) rate. Every interrupt has some amount of overhead associated with switching the context, setting up the pointers, etc. Using a 32-sample output FIFO, with a half-empty interrupt signal to the DSP, the DSP is now interrupted at a rate of $F_S/16$. The interrupt overhead is reduced by a factor of 16, which can result in two-to-three MIPS of savings. In addition, the need to synchronize the DSP core operation to every clock of the output DACs is reduced.

Dual DSPs Simplify Partitioning

Two DSPs can work in parallel, executing different portions of the algorithm and potentially increasing the available processing bandwidth by nearly 100%. The actual gains realized will depend on the nature of the processes involved. Correct software scheduling, to insure that the DSP engines are not waiting for each other, is mandatory.

Fortunately, most audio decompression algorithms are suitable for multiprocessor implementations. The tasks of bit allocation and processing the inverse transform are obvious candidates for the use of two DSPs. The first DSP (DSP A) works on parsing the input bitstream, recovering all data fields, computing the bit allocation, and passing the frequency-domain transform coefficients to the second DSP (DSP B). DSP B completes the task by performing the inverse transform (inverse fast-Fourier transform or inverse discrete-cosine transform depending on the algorithm). While DSP B is finishing the transform for a channel, DSP A is working on the next channel, making the processing parallel and pipelined. The tasks are nicely overlapping in time and, as long as tasks are of the same complexity, there will be no waiting for either DSP.

Software design is a big challenge in such a system, since an interprocessor communication protocol has to be derived. Synchronizing the two cores and making sure that there are no shared-resource access violations is a formidable task. Also, any additional code used for communication protocol is consuming both program memory space as well as valuable processing bandwidth. So, a trade-off has to be made to make the communication protocol very simple, yet very robust, and sufficient to perform all necessary tasks. In our example system, there is a shared memory of 544 words as well as a communication mailbox consisting of 10 I/O registers (five for each direction of communication (*Fig. 1*). Shared memory is used as a high- throughput channel, while communication registers serve as a low-bandwidth channel, as well as semaphore variables for protecting the shared resources.

Both DSPs can write to or read from shared memory. However, software management provides that the two DSPs never write to or read from shared memory in the same clock cycle. This technique avoids the use of expensive dual-port RAM. It is possible, however, that one DSP writes and the other reads from shared memory at the same time, given a two-phase clock in the DSP core. This way, several virtual channels of communications could be created through shared memory. For example, one virtual channel is the transfer of frequency- domain coefficients and another virtual channel is the transfer of PCM data.

While the first DSP is putting the PCM data into shared memory, the second DSP might be reading the encoded data at the same time. In this case, both virtual channels have to have their own semaphore variables for traffic control residing in the AB_shared_memory_semaphore register. Different physical portions of shared memory are dedicated to the two data channels. The AB_command_register is connected to the interrupt logic so that any write access to that register by DSP A results in an interrupt being generated to DSP B, if enabled. In general, I/O registers are designed to be written by one DSP and read by another. The only exception is the AB_message_sempahore register which can be written by both DSPs. Full symmetry in communication is provided even though, for most applications, the data flow is from DSP A to DSP B. However, messages usually flow in either direction. Hence another set of five registers with BA prefixes allow for communication from DSP B to DSP A.

Inter-DSP Messages

The AB_message_sempahore register is very important because it synchronizes the message communication. For example, if the DSP A wants to send the message to DSP B, it must first check that the mailbox is empty (the previous message has been taken) by reading a bit from the AB_message_semaphore register.

If the bit is cleared, DSP A can proceed with writing the message and setting this bit to one, indicating a new state: transmit mailbox full. DSP B may either poll this bit or receive an interrupt (if enabled on the DSP B side), to find that a new message has arrived. Once DSP B processes the new message, it clears the flag in the semaphore register, indicating to DSP A that the transmit mailbox has been emptied.

If DSP A had another message to send before the mailbox was cleared, it would have put the message in a transmit queue, whose depth depends on how much message traffic exists in the system. During this time, DSP A

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would be reading the mailbox-full flag. After DSP B has cleared the flag, DSP A can proceed to send the next message. In this case, both DSPs write and read access to the same physical register. However, they will never write at the same time, since DSP A is reading the flag until it is zero and setting it to one, while DSP B is reading the flag (if in polling mode) until it is one and writing a zero. Thus, these two processes will be staggered in time by the handshake protocol.

Shared-Memory Control

Shared memory is handled similarly. The AB_shared_memory_semaphore register is used. Once DSP A has computed the transform coefficients, but before they can be placed into shared memory, it must check that the previous set of coefficients for the previous channel has been taken by DSP B. While DSP A is polling the semaphore bit which is in the AB_shared_memory_semaphore register, it may receive a message from DSP B, via interrupt, that the coefficients are taken. In this case, DSP A resets the semaphore bit in the register in its interrupt handler. In this manner, DSP A has exclusive write access to the AB_shared_memory_semaphore register, while DSP B can only read from it.

For Dolby Digital decoding, DSP B is polling for the availability of data in shared memory in its main loop, because the dynamics of the decoding process are data driven. There is no need to interrupt DSP B with the message that the data is ready, because at that point DSP B may be busy finishing the previous channel. Once DSP B gets to the correct point in the program loop, then the data will be extracted.

The exclusive write access to the AB_shared_memory_semaphore register by DSP A is particularly important if there is another virtual channel (e.g. PCM data) implemented. In this case, DSP A might be writing the PCM data into shared memory while DSP B is taking out Dolby Digital data. If DSP B sets the Dolby Digital channel flag to zero, and DSP A sets the PCM flag to one, there will be an access collision in the semaphore register and system failure will result. To avoid this problem, DSP B sends a message that it took the data from shared memory and DSP A sets shared memory flags to zero in its interrupt handler. In this technique full synchronization is achieved and no access violations occur.

Debug Strategy

In a complex real-time system, each subsystem has to perform its task correctly, on time, and cohesively with all other subsystems. While each individual subsystem can be tested and made to work correctly, first attempts at integration often result in system failure. To prevent this failure, a good debugging strategy must be incorporated at the design phase.

Conventional Strategies

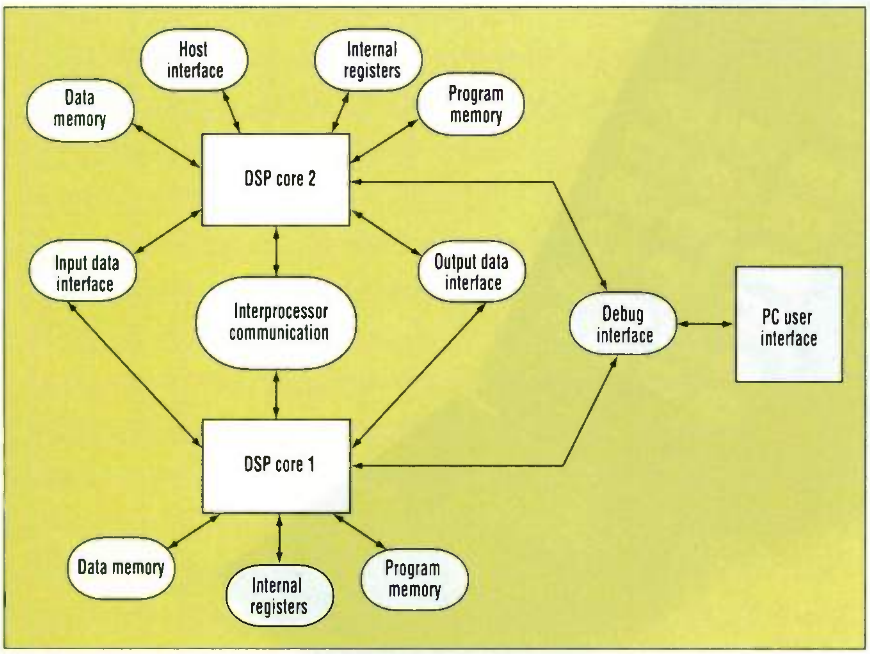
Debuggers can be static or dynamic. Static debugging involves halting the system and altering and/or viewing the states of the various subsystems via their control/status registers. This examination offers a lot of valuable information, especially if the system can automatically freeze on a break-point or other trapped event that the user can prespecify. It should be noted however, that because the system has been altered from its runtime state, some of the debug actions and measurements could be irrelevant, e.g. timer or counter values.

Dynamic debugging occurs while the system is actually running the application. For example, state variables can be traced over time just like a signal on an oscilloscope. Both types of debugging require special hardware with visibility to all the subsystems of interest. For example, in a DSP-based system, the debug hardware would need access to the DSP core and associated subsystems *(Fig. 2)*. Furthermore, dynamic debugging is more complex than static debugging because the debug hardware can upset the running subsystems. Unlike a static debugging session, one cannot hold off all the system hardware during a debugging session because the system is active. Typically, this requires dual-port access to all the targeted subsystems.

A Simplified Solution

Assuming that there is a DSP in the system with access to all the control and state variables of interest, a simple interrupt-based debug communication interface can be built. The solution is an additional communication interface to the DSP core *(Fig. 3)*. A simple two-wire clock plus data interface is used, where the PC can signal read or write requests with transitions on the data line while holding clock high. Meanwhile, the debug port can send back an active low acknowledge on the same data line after the subsequent falling edge of the clock.

A debugging session involves read and write messages sent from an external PC to the DSP via the debug inter-



4. Debugging a multi-DSP system requires a more complex strategy which enables access to both processors and their shared resources.

face. Assuming multiple-word messages in each debugging session, the DSP accumulates each word of the message by taking short interrupts from the main task and reading from the debug interface. Appropriate backup and restore of main task context should be implemented to maintain transparency of the debug interrupt. Only when the processor accumulates the entire message (the end of the message is determined by a suitable protocol), is it serviced. In the case of a write message from the PC, the DSP writes the specified control variable(s) with specified data.

In the case of a read request from the PC, the DSP compiles the requested information into a response message, writes the first of these words into the debug interface, and simply returns to its main task. The PC then pulls out the response message words via the same mechanism. Each read by the PC causes an interrupt to the processor which reloads the debug interface with the next response word until the whole response message is received by the PC. Such a dynamic debugger can easily operate in static mode by implementing a special control message from the PC to the processor to slave itself to the debug task until instructed to resume the application. This scheme requires some intelligence at the PC end. Some additional programming also is required to setup the debugging interrupt handler within the DSP. However, since the debug communication involves short interrupts there is very little waste of processor bandwidth.

Multiprocessor Environments

Each processor in a multiprocessor system will usually have dedicated resources (memory, internal registers, etc.) and some shared resources (data input/output, interprocessor communication, etc.) *(Fig. 4)*. The debug interface can be viewed as a shared resource because it communicates with both processors. The PC user can explicitly specify which processor is being targeted in the current debugging session with appropriate syntax in the first word of the messaging protocol.

On receiving this first word from the PC, the debug interface initiates communication only with the specified processor by sending it an initial interrupt. Once the targeted processor receives this interrupt it reads out the first word, assumes control of the debug interface (by setting a control bit), and directs all subsequent interrupts to itself. This technology effectively holds off the other processor(s) for the duration of the current debugging session.

Once the targeted processor has received all the words in the debug message, it services the message. In the case of a write message, it writes the specified control variable(s) with the specified data and then relinquishes control of the debug interface so that the PC can target any desired processor for the next debugging session.

In the case of a read request, the corresponding read response has to make its way back from the processor to the PC before the next debugging session can be initiated. The targeted processor prepares the requested response message, places the first word in the debug interface, and returns to its main task. Once the PC pulls this word out, the processor receives an interrupt to place the next word. Only after the complete response message has been pulled out does the processor relinquish the debug interface so the PC can start the next debugging session with any desired processor.

Low-Level Simulation Helps

After the initial specification phase, hardware and software designs are usually undertaken as parallel efforts. After design in a Hardware Description Language (HDL) like Verilog, individual testing of hardware blocks is performed using test vectors with HDL simulations including Register-Transfer Level (RTL) and gate-level models. For I/O interfaces, this also will involve developing HDL models of external blocks to test out the interface as though it were in a complete system.

On the software side, the algorithm is initially implemented using C or some other high-level language. This implementation can only roughly model the hardware (fixed-point precision etc.), and mainly serves as a reference decoder for subsequent steps. It also allows the designer to fully understand the details of the application.

The second stage involves using a bit-precise, functionally-accurate software simulator for the DSP. This design allows the engineer to develop actual machine code for the application, and eventually match the reference decoder output using input test vectors.

However, the independent hardware/software efforts will most likely miss many integration and system issues, which if left unverified could lead to a serious misfit during the integration phase. These kinds of problems this late in the process could cost significant amounts of time and money.

Hardware emulation techniques, such as Quickturn, can be used to verify the design at very high speeds—only 10-to-100 times slower than real-time. However, much time and effort is required to fit the hardware design into the emulator. Even then, the engineer has to compromise with some shortcuts—like faking external memory or I/O—which affect the validity of the tests and reduce confidence in the results. In spite of all this, and the cost of the emulator itself, this strategy is still viable because it could save a revision of silicon or system design.

Full-System Simulation

An alternative approach is to run the application on the full system using RTL simulation. Many designers do not even consider this as an option because the simulation is very slow. Typically, RTL runs a million times slower than real time. One second of real-time could take up to a few hundred hours to simulate! However, in some cases this approach is acceptable and even preferable to hardware emulation. The main advantage is that RTL simulation of the application is as close as you can get to the real hardware, and it yields very-high confidence. External blocks also can be modeled in RTL and interfaced to the system under design to setup an accurate system environment.

In our example of Dolby Digital decompression, an audio frame (the smallest independently decodable unit) is typically 32 ms long (a few hours of simulation time). Successful decoding of a small set of compliance test frames will exercise all the I/O and DSP states required for the application. This is sufficient to eliminate all major system problems and gain very-high confidence for first system trials.

Furthermore, RTL simulation offers easy and extended visibility into the hardware, which is very useful in quick debugging. Troubleshooting a problem on actual hardware or even

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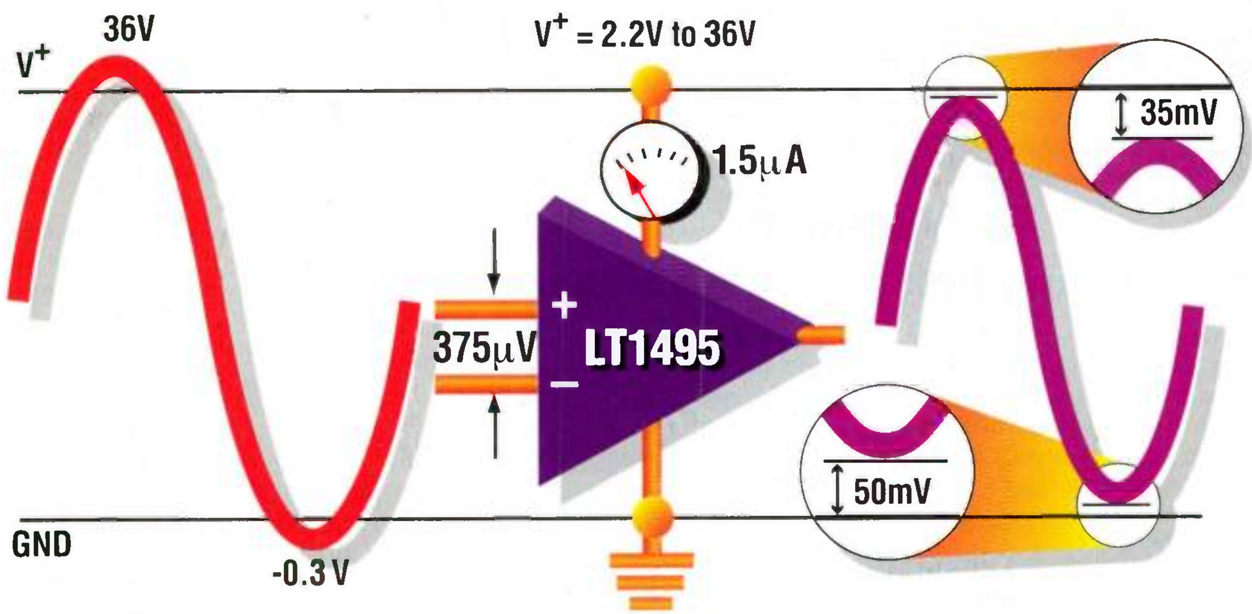

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emulators can easily take many days, whereas an RTL simulation can point to the problem very quickly.

The dynamics of the real-time environment also can be easily verified, especially critical in a multiprocessor design. Computer time is no longer an issue with faster and more easily available machines. Once the application is verified via RTL simulation there is very-high confidence in the system design as a whole. With the Dolby Digital decoder example, every application developed using the above strategy has worked immediately with the very first download of software.

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Terry Ritchie holds a BSET from Illinois State University, and is the director of marketing for DSP audio at Cirrus Logic.

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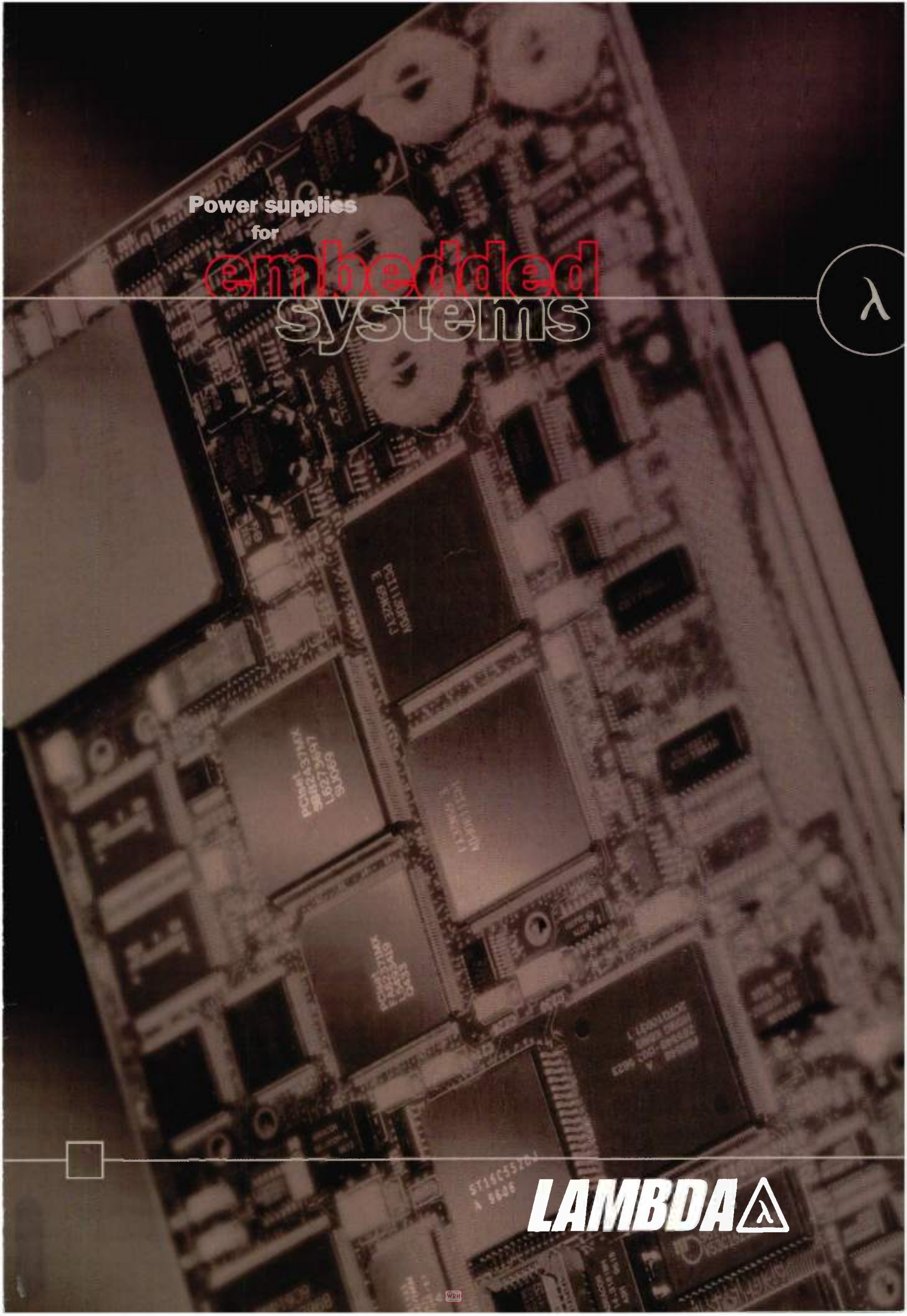
3. "AC-3: Flexible Perceptual Coding for Audio Transmission and Storage," Todd, Craig C., Davidson, Grant A., Davis, Mark F., Fielder, Louis D., Link, Brian D., Vernon, Steve, Audio Engineering Society 96th Convention, Feb. 1994, preprint 3796.
4. "AC-3: Operation, Bitstream Syntax and Features," Davis, Mark F. and Todd, Craig C., Audio Engineering Society 97th Convention, Nov. 1994, preprint 3910.
5. "Digital Audio Compression Standard (AC-3)," Advanced Television Systems Committee, Dec. 20, 1995.

How Valuable	Circle
Highly	538
Moderately	539
Slightly	540

Power supplies for embedded systems



LAMBDA

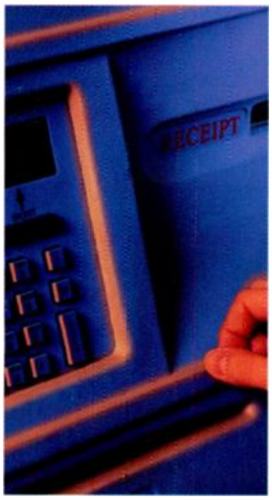
Lambda has power solutions for all high-power, high-reliability embedded processor applications.

Racks/Enclosures Include power supply support of approximately 500-1000W for all logic, memory, card power, computer architecture support and peripheral requirements. Typical systems demand the power supply provide multiple outputs including 3.3v and 5v, VME signals, output sequencing, current share, system level interface signals (such as AC good, DC good, remote sense, remote on/off and fan fail).

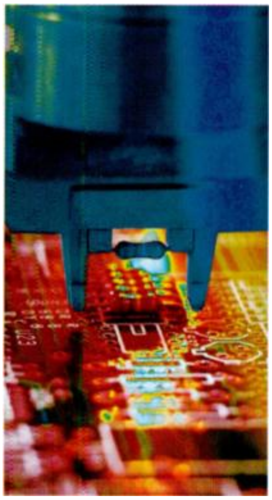
Workstations Typical requirements include up to 1000W in a multi output configuration. Sensitive workstations require constant monitoring functions via AC and DC good signals, remote on/off, tight regulation low ripple/noise, low levels of conducted and radiated EMI. Output voltages usually combine to include a high power 5v/3.3v main, +/-12v and 24v auxiliaries as well as an additional 3.3v high powered aux putput.

Mass Storage RAID Systems Power requirements are redundant in set-up and rely upon low ripple/ noise, low radiated and conducted EMI, current sharing capabilities from the power supplies and output sequencing. In addition, typical power ranges from 300W to 1000W in triple, quad and pent outputs relying heavily upon a high power 3.3v and 5v combination.

	Racks/Enclosures	Workstations	Mass Storage RAID Systems
UltraFlex Series	■	■	■
PFD Series	■	■	■
SM Series		■	■
RP Series	■	■	■
SV Series		■	■
SWT, ZWS, VSB Series			



Automated Services
Typical power required by these systems has increased to approx 600 to 1200W with an increased number of system signals being supplied by the power supply. In remote areas of operation, this equipment requires redundant, fault tolerant performance including current sharing power supplies which offer VME signals, AC and DC good, remote sense, remote on/off and overtemperature signals.



Factory Automation
Medium to high power (500-1000W), multiple output: incorporating 3.3v, 5v high powered outputs as well as system interface signals to monitor multiple operations at one time including AC and DC good, sequencing, current share, remote on/off, extended overcurrent protection with auto-restart and remote sense. The nature of this machinery requires a highly reliable, fault tolerant, redundant power supply.

Peripherals Multi-output products, medium to high power, including high power outputs for the demanding surge loads and power requirements. Normally require over-temperature and fan fail signals to support the system, as well as remote sense, AC and DC good signals.

Embedded Processor Instrumentation
Power ranges from 100-1000W requiring single and multiple outputs of a high reliability nature. Quality products that support system level functions are required to have AC and DC good, remote on/off, remote sense, some current sharing possibilities, VME signals, sequencing and extended overcurrent protection with auto-restart.

UltraFlex Series

The UltraFlex® Series provides high performance and high power density, with either a power factor corrected AC input or a 48 VDC input. Available with up to 10 outputs, the UltraFlex Series offers a customized power supply at standard product lead times.

These modular power supplies offer state-of-the-art power densities, exceptional flexibility, reliability, and outstanding performance.

Fully customized and available in two weeks.

Universal AC input or 48 VDC input.

Meets worldwide EMI requirements and full international safety agency approvals, (UL, CSA, VDE, CE mark).

Available with PFC and system interface and monitoring signals.

PFD Series

The PFD Series is designed to provide 750 or 1000W of power in a multiple output configuration with the industry's widest operating input range (36-75 VDC) ensuring worldwide operation through worst case input power sags and surges.

The PFD Series is designed with standard features such as current sharing, fan fail detection and input/output signals.

Wide range DC input: 36 - 75 VDC

Complete ETSI and Bellcore compliance.

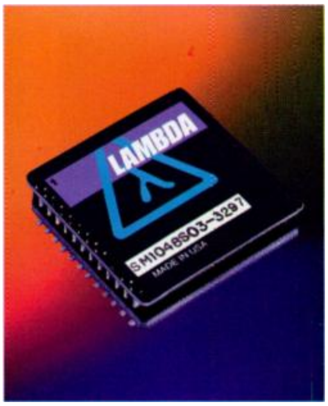
Meets worldwide telecom EMI requirements.

High powered 3.3V and 5V outputs in 750 or 1000W packages.

Available with system interface signals and current sharing.

Worldwide safety agency approvals, (UL, CSA, VDE, CE mark).

SM Series



This new line of surface mountable power supplies includes 56 DC-DC converter models with an extensive selection of standard voltages and currents so that OEM designers will easily be able to have accessibility to a range of converters for onboard power applications.

First complete line of surface mountable DC-DC converters in a low profile (0.4").

Hot pluggable with a 10m sec hold-up time.

Broad product offering from .30W in 56 different models.

Short lead time (< 4 weeks).

Worldwide safety agency approvals, (UL, CSA, CE mark).

RP Series

The RP series represents the first line of standard 500, 750 and 1000W supplies which complies with the EMC directive for CE marking and offers a high power, adjustable (3.0 to 5.75V) main output combined with higher powered 3.3V and 5.0V auxiliary outputs. A feature rich product, the RP Series is ideally suited for all embedded microprocessor applications.

CE-EMC compliance.

High powered adjustable 3.3V and 5V outputs in same package.

Worldwide safety agency approvals. (UL, CSA, TUV, CE mark)

Ideal for embedded micro-processor applications (microprocessor specific output voltages offered with VME signals).

Ideal for fault tolerant, redundant operation.

SV Series

The SV Series is available in 100W, 150W and 250W single output models, and 130W, 200W and 300W multiple output models, with or without power factor correction in the same footprint. For applications such as computer peripherals, point of sale equipment and communication equipment, the SV Series provides unequaled cost, flexibility and performance.

Universal AC input in a low profile (1.77") package.

Broad offering with over 62 models in single and multiple outputs.

Worldwide safety agency approvals. (UL, CSA, VDE, CE mark)

Available with or without power factor correction in the same footprint.

SWT, ZWS, VSB Series

Lambda's new SWT, ZWS and VSB Series are ideally suited for use in computers, peripherals, factory, office automation and other high volume applications offering low cost single and multiple output power supplies.

All models meet radiated and conducted EMI to Curve B for unparalleled global performance in a cost effective package with OEM-type input and output connectors.

Universal AC input (85 - 265 VAC)

Broadest product line with over 100 models in single and multiple outputs.

Designed for low cost, high volume production needs.

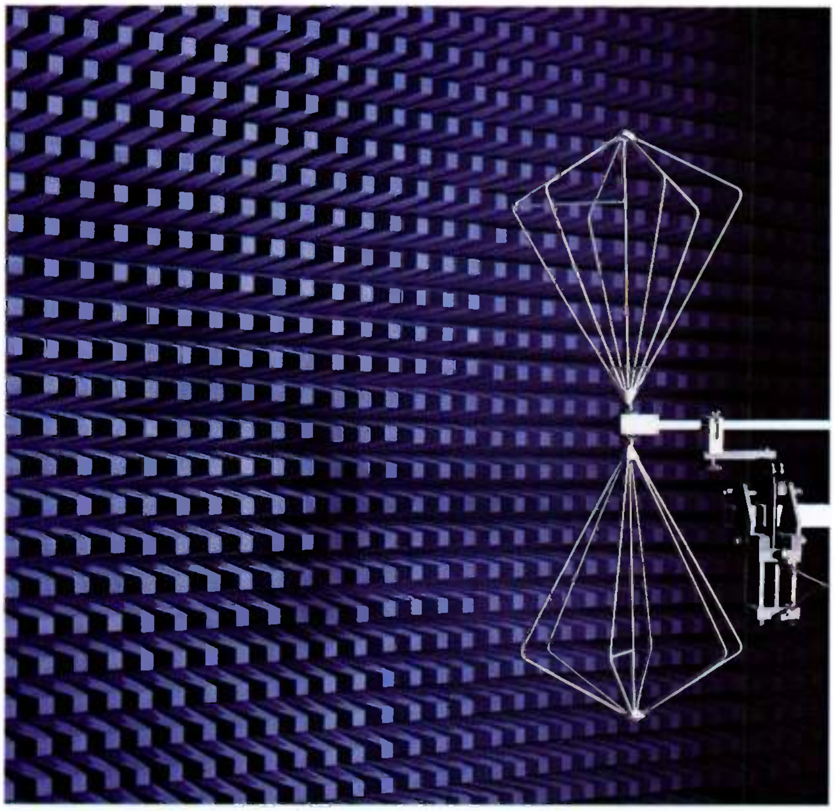
Worldwide safety agency approvals, (UL, CSA, VDE, CE mark), power factor correction and global EMI compliance.

Embedded system power supplies selector guide

Power (W)	# of Outputs	Input	Output, VDC	Dimensions	Remote On/Off	Remote Sense	AC/DC Good	Current Share	VME Signal	OT	Fan Fail
RP Series											
500	T, Q, P	85-265 VAC	3.3, 5, ±12, 24, 48	2.5 x 5 x 12	•	•	•	•	•	•	•
750	T, Q, P	85-265 VAC	3.3, 5, ±12, 24, 48	2.5 x 8 x 12	•	•	•	•	•	•	•
1000	T, Q, P	85-265 VAC	3.3, 5, ±12, 24, 48	2.5 x 8 x 12	•	•	•	•	•	•	•
PFD Series											
750	Q, P	36-75 VDC	3.3, 5, 12, 24, 48	2.65 x 8 x 12	•	•	*	•	•		•
1000	Q, P	36-75 VDC	3.3, 5, 12, 24, 48	2.65 x 8 x 12	•	•	*	•	•		•
SV Series											
100	S	85-265 Auto or Universal	5, 12, 24	1.77 x 4.75 x 7.5	•	•	•				
150	S	85-265 Auto or Universal	5, 12, 24	1.77 x 4.75 x 8.5	•	•	•				
250	S	85-265 Auto or Universal	5, 12, 15, 24, 28, 48	1.77 x 4.75 x 9.5	•	•	•				
115	T	85-265 Auto or Universal	5, ±12	1.77 x 4.75 x 8.5	•	•	•				
170	T	85-265 Auto or Universal	5, ±12	1.77 x 4.75 x 9.5	•	•	•				
300	T	85-265 Auto or Universal	5, ±12	1.77 x 4.75 x 11	•	•	•				
130	Q	85-265 Auto or Universal	5, ±12, 24	1.77 x 4.75 x 8.5	•	•	•				
200	Q	85-265 Auto or Universal	5, ±12, 24	1.77 x 4.75 x 9.5	•	•	•				
300	Q	85-265 Auto	5, ±12, 24	1.77 x 4.75 x 11	•	•	•				
Ultraflex Series											
400	S, M	85-265 VAC	2, 3.3, 5, 12, 15, 24, 28, 36, 48	2.5 x 5 x 10	•	•	•	•		•	•
600	S, M	85-265 VAC	2, 3.3, 5, 12, 15, 24, 28, 36, 48	2.5 x 5 x 12	•	•	•	•		•	•
SM Series											
5	S, D	24 or 48 VDC	5, ±12, ±15	.395 x 1.4 x 1.43	•			•			
10	S, D	24 or 48 VDC	3.3, 5, ±12, ±15	.395 x 1.4 x 1.43	•			•			
20	S, D	24 or 48 VDC	3.3, 5, ±12, ±15	.395 x 1.4 x 1.83	•			•			
30	S, D, T	24 or 48 VDC	3.3, 5, 8, ±12, ±15	.395 x 2.4 x 2.54	•			•			
SWT Series											
30	T	86-265 VAC	+/-5, ±12	1.2 x 5 x 3							
40	T	86-265 VAC	+/-5, ±12	1.4 x 5 x 3							
65	T	85-265 VAC, auto	+/-5, ±12	1.77 x 6 x 3.5							
100	T	86-265 VAC	+/-5, ±12	1.77 x 7.75 x 4.25							
VS Series											
10	S	85-132 VAC	3.3, 5, 2, 15, 24, 36, 48	.67 x 3.86 x 1.77							
15	S	85-132 VAC	3.3, 5, 2, 15, 24, 36, 48	.67 x 4.53 x 1.97							
30	S	85-132 VAC	3.3, 5, 2, 15, 24, 36, 48	.98 x 5.22 x 1.97							
50	S	85-132 VAC	3.3, 5, 2, 15, 24, 36, 48	.98 x 7.68 x 1.97							
75	S	85-132 VAC	3.3, 5, 2, 15, 24, 36, 48	1.26 x 8.76 x 1.97							
100	S	85-132 VAC	3.3, 5, 2, 15, 24, 36, 48	1.26 x 8.76 x 2.44							
150	S	85-132 VAC	3.3, 5, 2, 15, 24, 36, 48	1.42 x 8.76 x 2.95							
ZWS Series											
5	S	86-265 VAC	3.3, 5, 2, 15, 24, 36, 48	.83 x 3.86 x 1.77							
10	S	86-265 VAC	3.3, 5, 2, 15, 24, 36, 48	.83 x 4.13 x 1.97							
15	S	86-265 VAC	3.3, 5, 2, 15, 24, 36, 48	.83 x 4.92 x 1.97							
30	S	86-265 VAC	3.3, 5, 2, 15, 24, 36, 48	1.02 x 5.24 x 2.17							
50	S	86-265 VAC	3.3, 5, 2, 15, 24, 36, 48	1.02 x 7.68 x 2.17							
75	S	85-265 VAC, auto	3.3, 5, 2, 15, 24, 36, 48	1.38 x 8.74 x 2.17							
100	S	85-265 VAC, auto	3.3, 5, 2, 15, 24, 36, 48	1.38 x 8.74 x 2.44							
150	S	85-265 VAC,	3.3, 5, 2, 15,	1.58 x 8.74 x 2.95							

*DC Good

How Lambda serves the embedded systems OEM

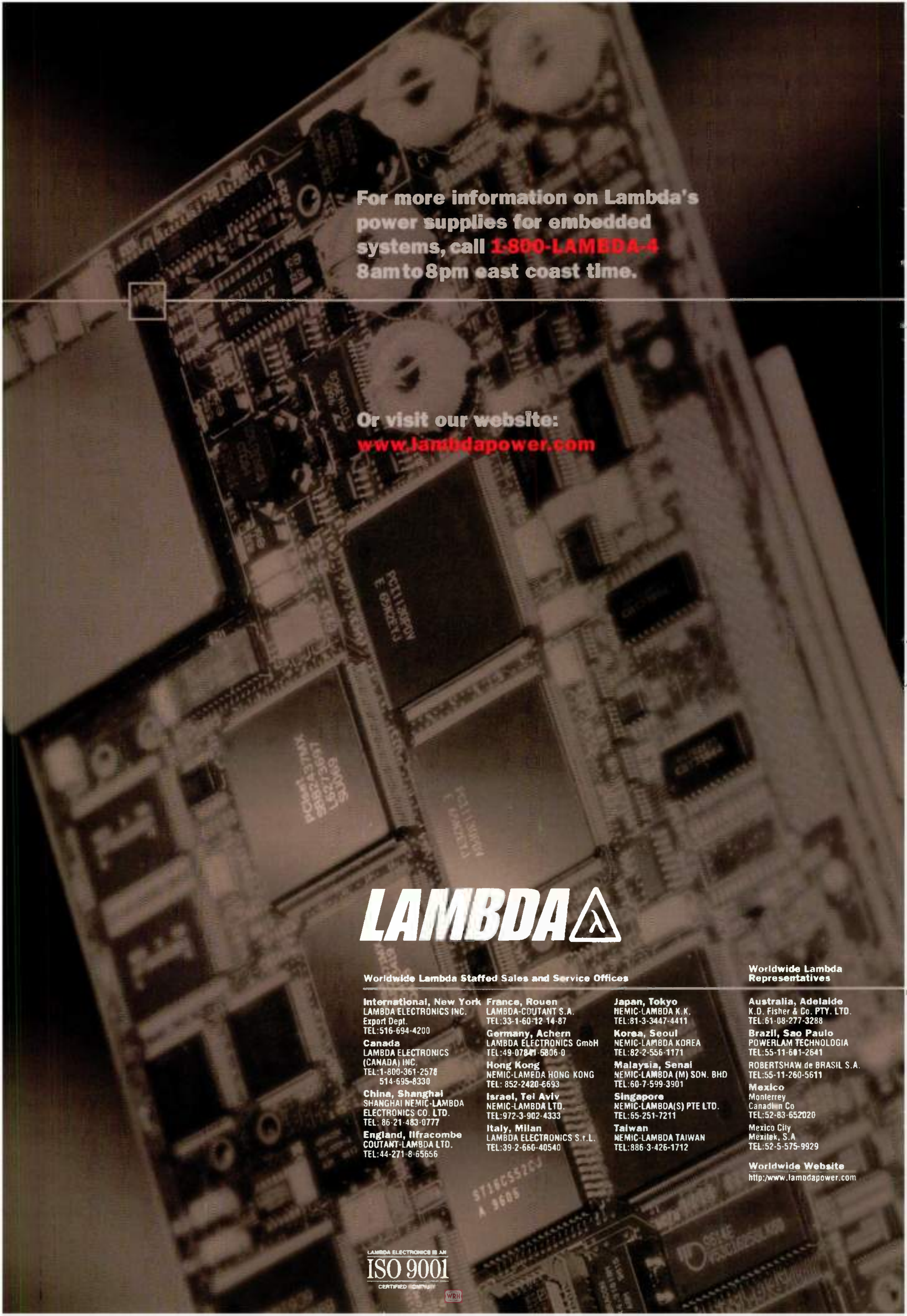


Design cycle time. We can shorten your time to market in several ways. First of all, we have more than 1000 standard models available from stock. Next, many of our solutions are modular and scalable. With our UltraFlex line, for example, we use off-the-shelf modules to instantly create a power supply tailored to your exact needs. For most full-featured configurations, we now *guarantee* delivery within 72 hours of accepting an order.

Flexibility. For OEMs whose needs aren't met by a standard product, Lambda offers the ultimate in design flexibility—our Value-Added Solutions. Instead of waiting a year or more for a custom power supply to be developed for your new product, you can get a Value-Added Solution from Lambda in just 3 to 12 weeks.

Lambda is uniquely positioned to supply these modified-standard solutions because we start with the industry's broadest line of off-the-shelf building blocks.

CE/EMC-compliance. Embedded systems engineers and integrators face a constant struggle to lower EMI to meet worldwide standards, and power supplies are a significant source of EMI in their systems. Rather than leave it our customers to deal with the problem, we've invested in our own in-house EMI and lightning strike measurement facilities. The result is the new RP Series, the first CE/EMC-compliant power supplies.


For more information on Lambda's power supplies for embedded systems, call 1-800-LAMBDA-4 8am to 8pm east coast time.
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UPDATE ON DIGITAL CELLULAR TELEPHONES

Digital Mobile Telephones Will Face The Challenge Of Integrating Passive Components As They Permeate The Consumer Sector

By the end of this century, there will be more cellular telephones than wired ones in several countries around the world. That's the opinion of Dr. Yrjoe Neuvo, senior vice president of product creation at Nokia Mobile Phones, Espoo, Finland. "Cellular telephones will become a consumer product subject to the cost pressures of a consumer market," he says. This means that design concepts must be carefully thought out to meet the time-to-market demands of the consumer market.

"Today, discrete passive components account for 95% of a mobile telephone's components, and are responsible for 80% of the volume as well as for 70% of the cost," claims Neuvo. He points out that a typical mobile telephone currently consists of five ICs and 60 passive components. However, by the year 2000, it will be required to have just two ICs and 10 passive components. At an annual price decrease of 25%, and a form factor and weight reduction of about the same, reducing the number of components is a must.

Neuvo thinks that there is still a huge potential for reducing power consumption in a mobile telephone. "If a mobile telephone from 1986 had a relative power consumption of 10, this value would be just three for a 1998 model. For a year 2000 model this would even decrease to a power consumption factor of one," he elaborates.

He feels that simultaneously, the performance of a cellular telephone needs to increase from about 80 MIPS in 1996 to 120 MIPS in 1998 to 200 MIPS in the year 2000. This increase can be achieved by increasing IC gate density per square millimeter from 15,000 in 1996 to 30,000 in 1998, and to 50,000 by the year 2000. He envisions CMOS as becoming a viable technology for the frequency range of 0.8 to 2.0 GHz.

He sees passive components as the biggest problem for future integration. Resonators, adaptive networks, filters, oscillators, and the like can only be integrated under very difficult circumstances. Furthermore, currently used capacitors, resistors, and inductors are still needed for tasks such as bias preadjustment, bypasses, and interference filters.

The trend in Europe is toward multimode cellular telephones. As a result, all the RF filters for every single frequency band need to be available within the telephone, and each filter must have a dynamic range of more than 100 dB. "Imagine the RF-filter efforts that must be made in order to design a multimode telephone capable of handling GSM-900, GS-1800, and GSM-1900 systems," says Neuvo. GSM-900 is the "classic" 900-MHz original GSM system which can now be found in about 40 to 50 countries worldwide. GSM-1800, also known as PCS-1800, is an 1800-MHz system. And, GSM-1900 is a 1900-MHz system currently being built in several United States cities.

The advantage of such a multimode telephone is obvious: If mobile telephone operators sign roaming contracts, it would be possible to use a U.S. GSM-1900 mobile telephone all over Europe, Hong Kong, or Australia. According to Neuvo, multimode mobile telephones will have the biggest market share with new sales. Therefore, one of the most important areas of work is miniaturizing the passive filters. Ceramic, dielectric, and surface acoustic wave (SAW) filters have significantly decreased a mobile telephone's size within the last year, "but a real breakthrough in filter technology has not occurred,"adds Neuvo.

As a first step, IF filters must be optimized for the channel bandwidth. If several access techniques and modulation methods are used in a multimode terminal, several parallel filters are needed. Adaptive filters can be implemented using DSP, however the in-band dynamic range on the order of 100 dB sets tough requirements for today's analog-to-digital converters (ADCs). "Evolution in CMOS technology will take care of this problem," Neuvo says. "Subharmonic IF-sampling architectures utilizing sigma-delta type ADCs will offer one solution," he adds.

The solution for these problems might be direct sampling where the RF is converted directly into the baseband without the detour via the IF. Therefore, extremely sharp filters are needed, however, the need for significantly less-passive components will be the result. While in today's digital mobile telephones about 70% of the functionality is handled by hardware and 30% by software, this will totally change, according to Neuvo. "By the year 2002, hardware will only count for 30%, 70 % of a digital mobile telephone's functionality will then be realized by software," he says. Neuvo believes that there will only be one universal hardware architecture with a standardized DSP and microprocessor platform for digital mobile telephones. RF channel handling as well as product differentiation will then be implemented by software. Depending on the distribution channels, this software can already be implemented during manufacturing or at the point of sales. The customer only pays for the functionality he or she gets. The next step will be reloading the software via the mobile telephone software, which might be interesting for updates or functional extensions.

Nokia, for example, has already gained some experience with software updates over the air. The company has designed and is delivering a so-called "D-Box," a set-top box for German digital TVs where the software update feature is already implemented.

However, one point is still the most critical for Nokia. It's that new innovations are required for the integration and packaging of filters, oscillators, and discrete components as well as antennas.

For more information, contact Dr. Yrjoe Neuvo, Nokia Mobile Phones, P. O. Box 100, FIN-00045, Nokia Group, Finland. Telephone 358-10-5051. Fax 358-10-505-5742.

Alfred Vollmer

ELECTRONIC DESIGN QUICK LOOK

Edited by Mike Sciannamea and Debra Schiff

MARKET FACTS

Jump Starting The Market

When people generally think of batteries, they usually think of their watches, portable stereos, or even their cars. But, what they don't know is that the U. S. battery industry alone carries a $6.1 billion price tag. You'd be hard pressed to find a home in the United States that doesn't have a flashlight, smoke detector, watch, battery-operated toy, notebook computer, or personal digital assistant. According to a new report from Business Trend Analysts and the Leading Edge Group, "The U. S. Battery Market, 1997 Edition," this country's battery market has matured. It's grown at an average pace of 2.9% each year for the first half of the 1990s. Sales are expected to keep the growth up at an average annual rate of 2.7% over the next decade. This moderate pace will yield sales of nearly $8 billion by midway through the next decade. The report says that the battery market has experienced a slowing trend over the last twenty years, with peaks in the mid- and late-1980s. But, overall, the largest end-use products, including consumer electronics, games, and toys, not to mention automobiles, have matured, thus bringing on the slow growth in the market. In the battery market, there are two main categories: storage and primary. Storage batteries, including the automotive battery group, account for about two-thirds of the market. Last year, the automotive sector of the battery market saw 94.3 million units sold. The storage batteries also include the growing rechargeable battery segment. One interesting element that affects replacement battery demand, especially in the automotive sector, is weather. Unpredictably harsh winters or summers significantly raise demand due to higher failure rates. Last year's replacement market saw only a 1.5%

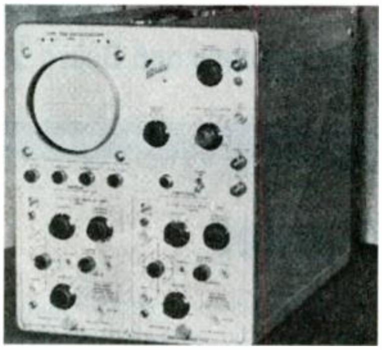
Art: Tony Vitolo

growth in sales, while in 1995, the replacement market sank 5.6%. Another aspect of growth in the automotive end is the evolution of electrical vehicles. General Motors, Honda, and several other automakers are finally bringing their electrical offerings to a mass audience. Although these vehicles are only offered commercially on a limited basis, the companies are working on future generations of fuel cell- and battery-operated electrical vehicles. Despite the fact that California's Air Resource Board mandate of zero-emission cars accounting for 2% of all of a manufacturer's sales in 1998 was killed, the outstanding mandate requiring that 10% of new cars sold must be zero-emissions by 2003 is still in effect. Rechargeable batteries such as nickel metal-hydride and lithium are increasingly used in applications such as cellular and other wireless telecommunications, portable computers, and cordless power tools. These types of rechargeables also may be seen as viable options in the electrical vehicle sector. Primary batteries, made up $2 billion of the U. S. battery market in 1996. According to the report, these types of batteries are in 90% of U. S. households at least once a year. Around 40% of sales of primary batteries occur during the fourth-quarter holiday shopping season. As may be obvious already, the two heavy hitters in the battery industry's advertising race are Duracell and Eveready. The two largest consumer battery manufacturers each set aside approximately $66 million for advertising last year. In addition to the two biggies, Panasonic and Sony also launched major promotional campaigns in 1996. Typically, the battery campaigns included mail-in rebates and cross-promotional items from other products or movies. As far as the global reach of batteries from the U. S. is concerned, in 1996, battery imports added up to $1.7 billion and exports totaled $1.4 billion. Many of the battery manufacturers have focused on expanding their manufacturing and distribution operations into China, Taiwan, and Thailand. Exports rose 40% in the first five years of the 1990s.

For more information, contact Business Trend Analysts, 2171 Jericho Turnpike, Commack, NY 11725-2900; (516) 462-5454; fax (516) 462-1842.—**DS**

40 YEARS AGO IN ELECTRONIC DESIGN

Type 536 High-Frequency Scope: Identical X-Y Deflection



Type 536 oscilloscope has identical horizontal and vertical deflection characteristics with the same type of preamplifier plugged into both channels. It converts to a general-purpose instrument when the Type 53/54T time-base generator is plugged into the horizontal amplifier. Horizontal and vertical characteristics include: differential inputs, dc-to-10-mc pass bands, 0.035 μsec risetime, nine calibrated deflection factors from 0.05 V per div to 20 V per div with vernier controls for adjusting sensitivity between steps, less than one degree relative phase shift to well beyond 10 mc, adjustable phase balance up to 20 mc, five division of deflection at 20 mc without overdriving input amplifiers. Tektronix Inc., Dept. ED, P. O. Box 831, Portland 7, Ore. *(Electronic Design, Nov. 15, 1957, p. 121)*

Tektronix continued to upgrade oscilloscopes from simple waveform displays to true measurement instruments.—SS

"Ten Electro-Commandments"

For the benefit of those who engage in electronics design, development, and just plain tinkering, take heed.

1. Beware the lightning that lurketh in an undischarged condenser lest it cause these to bounce upon thy head in a most ungentlemanly manner.
2. Cause thou the switch that supplieth large quantities of juice to be opened and thusly tagged that thy days may be long in this earthly vale of tears.
3. Prove to thyself that all circuits that radiateth and upon which thou worketh are grounded and thusly tagged lest they lift thee to radio frequency potential and causeth thee to make like a radiator, also.
4. Tarry thou not amongst those fools who engage in intentional shocks for they are not long for this world.
5. Take care thou useth the proper method when thou taketh the measure of a high voltage circuit so that thou dost not incinerate both thee and thy test meter; for verily, though thou hast no plant account number and can be easily surveyed, the test meter doth have one and as a consequence bringeth much woe unto the supply officer.
6. Take care thou tampereth not with interlocks and safety devices for this insureth the wrath of the supervisor and bringeth the fury of the department head upon they shoulders.
7. Work thee not on energized equipment for if thou dost so thy shopmates will surely be buying beers for the widow and consoling her.
8. Verily, verily I say unto thee never service equipment alone for electrical cooking is sometimes a slothful process and thou might sizzle in thine own fat upon a hot circuit for hours on end before thy Maker sees fit to end thy misery and drag thee into His fold.
9. Trifle thee not with radioactive tubes and substances lest thou commence to glow in the dark like a lightning bug.
10 Commit thou to memory all the works of the prophets which are written down in the chapters of thy bible which is the Safety Manual, and which giveth out with the straight dope and consoleth thee when thou has suffered from thy superior.—Reprinted from a report from the U. S. Naval Ordinance Laboratory, Silver Spring, Md. *(Electronic Design, Nov. 15, 1957, p. 18)*

No comment—if you can't top it, let it be.—SS

OFF THE SHELF

Object-Oriented Modeling and Design creates a language-independent graphical notation for analyzing problem requirements, design solutions, and implementing those solutions in a specific program or language base. The book focuses on high-level, front-end conceptual process of analysis and design, presents a practical orientation, and includes extensive examples, learning-centered exercises, and industrial object-oriented application case studies. The 528-page book is priced at $65. Contact The Penton Institute, 1100 Superior Ave., Cleveland, OH 44114; (800) 223-9150; fax (216) 696-6023; Internet: http://www.penton.com.

ISO/QS 9000 Yearbook: 1998 explores a range of issues concerning the worldwide set of quality standards known as ISO 9000, as well as the specialized standards known as QS 9000. Included are case studies from companies on how they received ISO/QS 9000 certification and how they are implementing ISO procedures. The book contains predictions of upcoming changes that may impact a company's maintenance of standards—plus training- and industry-specific topics. The 448-page book is priced at $60. Contact McGraw-Hill Inc., Customer Services, P. O. Box 545, Blacklick, OH 43004-0545; (800) 722-4726; fax (614) 755-5645; Internet: http://www.mcgraw-hill.com.

ATM Switches offers an in-depth evaluation of what the new generation of high-speed switches can and cannot deliver. The book discusses the Asynchronous Transfer Mode (ATM) standard, including user requirements, technical challenges, current equipment limitations, and necessary ancillary components to telecommunicate. The book examines high-speed network challenges, and presents the first generation of switching systems currently available as commercial products. The 336-page book is priced at $75. Contact Artech House Publishers, 685 Canton St., Norwood, MA 02062-2610; (800) 225-9977, ext. 4030; fax (781) 769-6334; Internet: http://www.artech-house.com.

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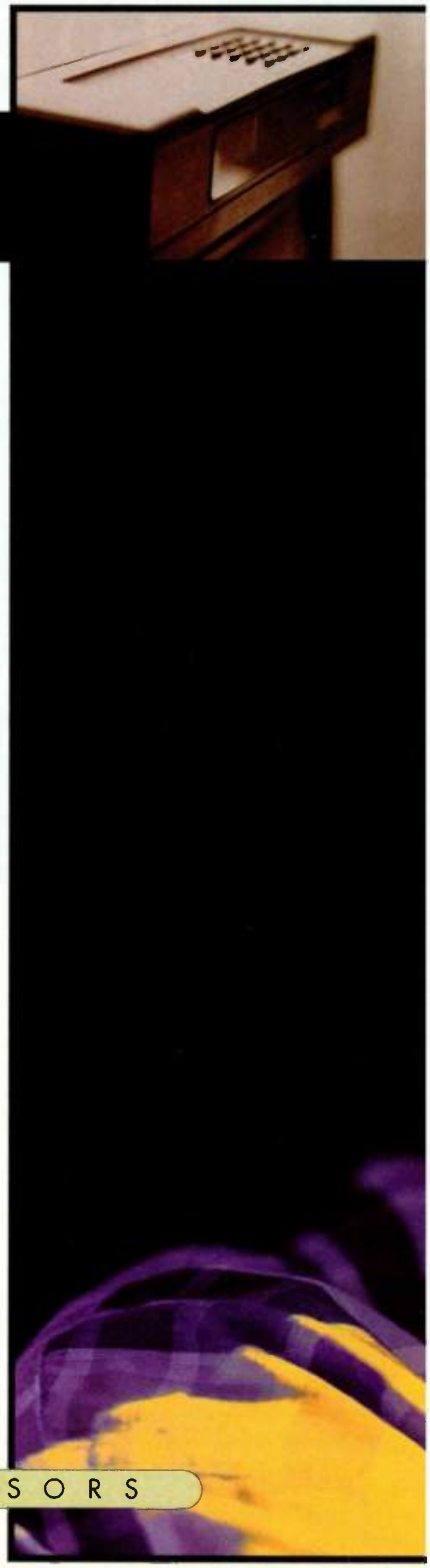

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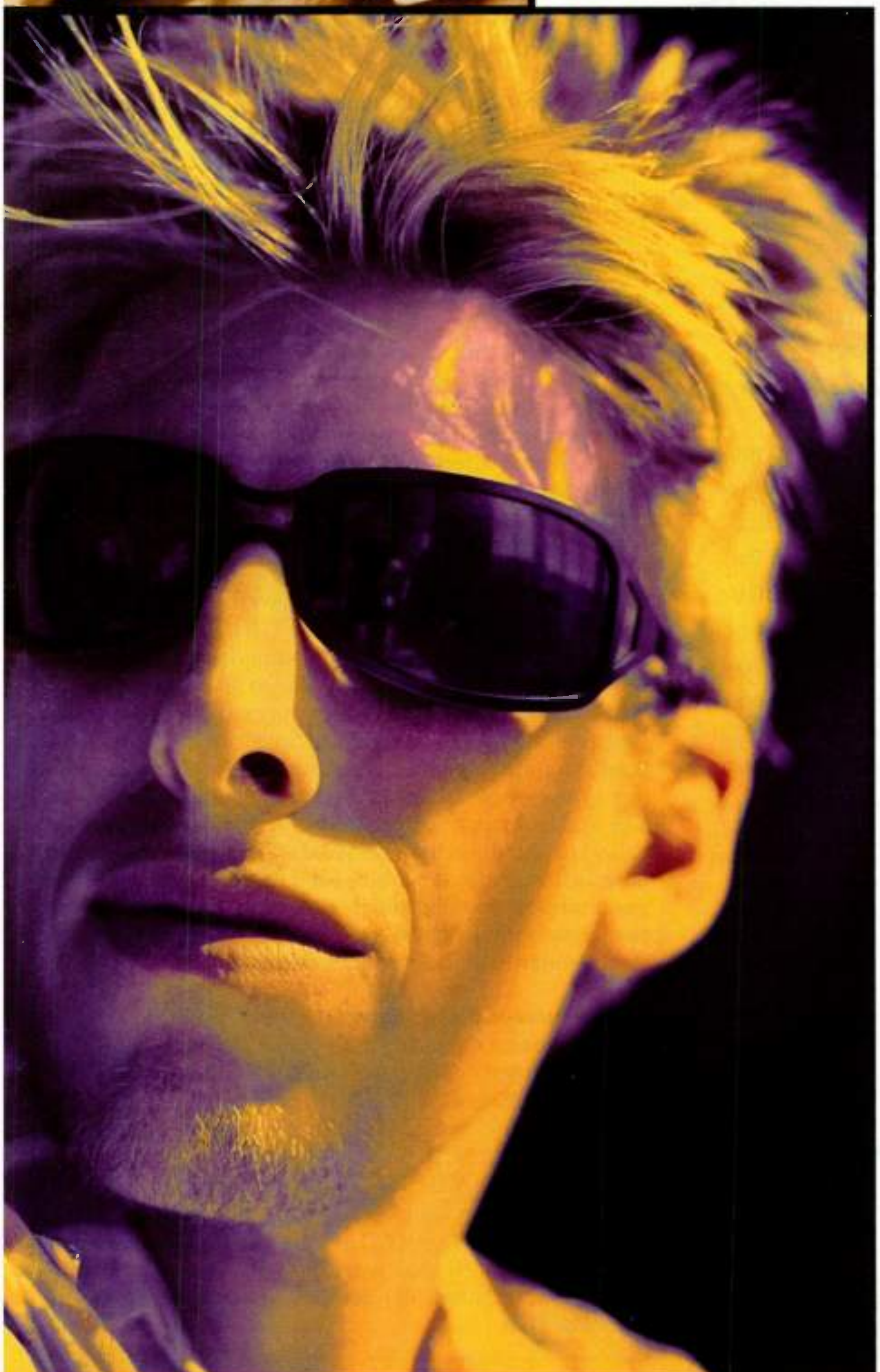
Power Consumption	200mW	250mW	1.8W/2.2W	<6W
Supply Voltage	3.3V	3.3V	3.3V	3.3V
MIPS/W	185	320	---	---
Windows CE Support	V1	V2	V2	---
Chipset Support	Yes	Yes	Yes	Yes
Feature Highlights	5 Ch. DMA Controller RAM/ROM Controller Serial Interface IrDA™	Soft Modem 4-mode PMU 10-bit DAC/ADC Single-cycle MAC	High-perf. MMU, Single/Double Precision FP *Ideal for high-performance embedded applications*	400 MFLOP FPU L2 Cache controller Two-way superscaler pipeline



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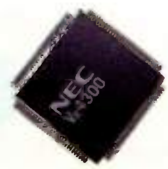

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INTERNET ROLODEX

http://www.semisearch.com: FabLink Corporation's new site features a powerful new Internet search engine that's specifically tailored for the semiconductor industry. Because most web surfers perform searches at least once during their time on line, FabLink recognized the need for a search engine that yields more useful results than the big, general engines. Valuable information such as contacts, links, and on-line catalogs can be found at the site. Plans for expansion include the addition of conference and training information, current technical publications, and industry association information. The company offers services such as electronic catalogs, automated procurement, and web-page design.

http://www.natinst.com: Check out National Instruments' new site for the latest evaluation copies of LabVIEW, LabWindows/CVI, BridgeVIEW, Lookout, and other virtual instrumentation software. The site also features extensive pages of the latest industry news. Visitors to the site will find on-line support, new product and technology developments, product data sheets, alliance information, and the Instrumentation Web. The Instrumentation Web feature is a huge database of User Solutions articles that show visitors National Instruments software and hardware in action. The newest additions to the site include: a glossary of industrial and instrumentation terms, extranet capabilities for Alliance Program members and international branch offices, and optional registration for users who wish to receive updates directly through their e-mail.

http://www.irf.com: International Rectifier has revamped their entire web site to answer the specific needs of the engineers who click on their URL. Visitors looking for solutions for their power-conversion process can go to product specific topical sites. These sites feature data sheets, application notes, white papers, design tips, selection guides, short-form catalogs, Spice and Saber models, product-status updates, images of case styles and package types, parametric values, and pricing information. The short-form catalog for 1997 is in .PDF format that includes part-number hyperlinks that bring the engineer to datasheets. Links at the site send engineers to sales representatives, distributors, technical support, and literature. Engineers with an eye for trade shows can click on the calendar listings for more information.

http://www.aldec.com: Try Aldec's site for the latest information on design entry, logic synthesis, and verification software for programmable logic designs. Their newest tool, Enhanced VHDL Tutorial with Applications (EVITA) is now available at the site. EVITA allows visitors to interact with on-screen hardware designs and learn how to use VHDL in their designs. The shareware version of EVITA contains chapters on architecture and signals, as well as entity. The software explains VHDL concepts through real-world objects, schematic diagrams, and pictures. The complete version of EVITA is priced at $795.

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AK7712A Technical Overview
Digital Audio Features
• 20-bit Stereo A/D with 97dB SNR
• Two 20-bit Stereo D/As with 97dB SNR
• Flexible I/O Structure Supports Additional D/A Outputs, A/D Inputs
DSP Features
• 24-bit Fixed-Point Processor
• 54ns Instruction Cycles with up to Six Operations per Cycle
• 384 X 32-bit Program RAM
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* Check with your local AKM sales office for a list of supported algorithms

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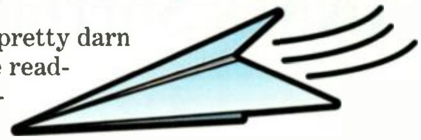
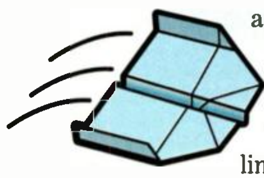
READER SERVICE 192

JUST A REMINDER



I must say that it's pretty darn rewarding to have readers who are so involved in this First Annual QuickLook Paper Airplane Contest. To answer one question, "paper" can be any size under one-eighth of an inch thick. Basically, at that point you're playing in cardboard or really heavy oaktag territory.

If you have no idea what I'm referring to, we're running a contest. A paper airplane contest.We here at *QuickLook* want to see what kind of innovative work you can do on a paper airplane. Be as creative as you like, but what we're looking for is the most creative use of working electronics on a paper airplane.



We do have a few simple guidelines here:

- Get your paper airplanes to us by January 1, 1998.
- As I said before, paper airplanes must be made of paper. No balsa wood, thin plastics, or metal sheeting. No need to cheat—be creative.
- Paperclips and/or glue are accepted, but be sensible about it—the thing's still got to fly at least 12 ft.
- Planes must be preassembled before we receive them. We simply don't have time to put them together.
- No wingspans larger than 3 ft (that's a big plane, by the way). If I can't carry it, then it's not going to be in the competition.

1-800-Batteries

If you have any questions regarding airplane designs or contest rules, e-mail me at: *debras@csnet.net.*

The core of the contest is how you can creatively use electronics in the design of a paper airplane. If you can wow the editors of *Electronic Design* with your innovative bit of flying fancy, you'll be sure to win. Speaking of winning, the prizes are: one $150 gift certificate for first prize, and one $50 gift certificate for second prize, both to be used with our sponsor's (1-800-BATTERIES) catalog.

And conveniently for you, 1-800-BATTERIES also is offering, free of charge, 3-V lithium batteries for the first 100 engineers who send us self-addressed, stamped envelopes (SASE) requesting one. You don't necessarily need to use the battery to power your design on your paper airplane, but we'd be interested in seeing what you can do with it anyway.

Just a few other notes. We're not going to return any of your planes, so take pictures before you send them to us. And, of course, send your battery requests, SASEs, and airplanes to QuickLook Editors, *Electronic Design*, 611 Route 46 West, Hasbrouck Heights, NJ 07604. Good luck!—**DS**

Adventures In Communication Design™
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8-Port MAC
10/100 Ethernet controller with PCI interface; full and half duplex flow control.
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OFF THE SHELF

ISO 9000: An Implementation Guide for Small to Mid-Sized Businesses is a step-by-step guide to ISO 9000 certification specifically written for small to mid-sized businesses. The book shows sample procedures that can easily be adapted for in-house use and presents a cost-effective blueprint for doing the necessary work, including a detailed roll-out plan for implementation. The book includes many real-life examples, and contains case studies and illustrations. The 272-page book is priced at $47.95. Contact St. Lucie Press, 2000 Corporate Boulevard, N.W., Boca Raton, FL 33431; (800) 272-7737; fax (800) 374-3401; Internet: http://www.slpress.com.

Electronic Connector Handbook covers the basic functions of connectors and details the full range of electronic connectors that are currently available. Connector parameters are discussed in an application context to expedite implementation, and extensive design and materials selection criteria are provided for the full range of connectors. Readers will be shown techniques for determining a connector's potential degradation mechanisms, the degradation mechanisms that will be active in the application, and the criteria for failure in a connector. The 600-page book is priced at $89.50. Contact McGraw-Hill Inc., Customer Services, P.O. Box 545, Blacklick, OH 43004-0545; (800) 722-4726; fax (614) 755-5645; Internet: http://www.mcgraw-hill.com.

C++: How To Program teaches C++ programming by emphasizing program clarity through structured and object-oriented programming methods. The book addresses concepts such as control structures, functions, arrays, pointers, strings, and references, with "Thinking in Objects" chapter sections. The book also covers data abstraction, inheritance, polymorphism, templates, and structured exception handling. The 950-page book is priced at $51. Contact The Penton Institute, 1100 Superior Ave., Cleveland, OH 44114; (800) 223-9150; fax (216) 696-6023; Internet: http://www.penton.com.

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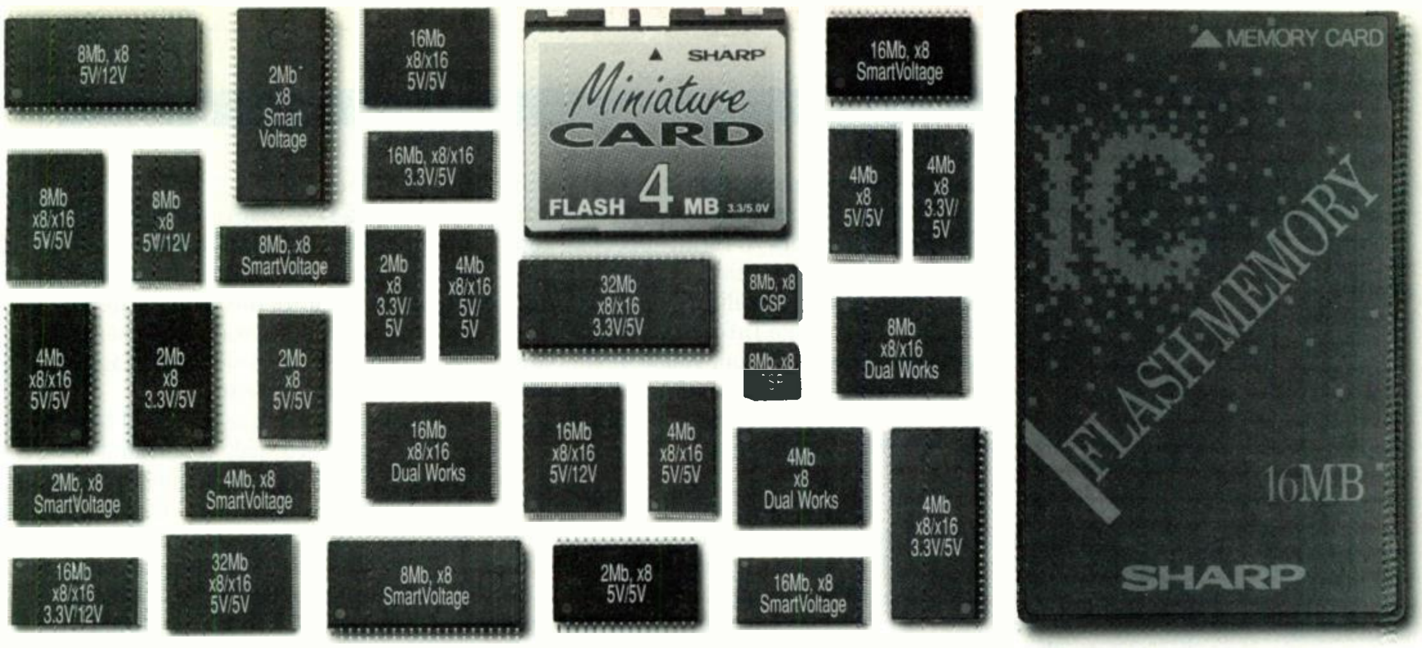

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READER SERVICE 206

THIS JUST IN...

Sainsbury's Supermarkets Ltd., London, England, one Europe's largest grocery chains, will be testing SCS Corp.'s passive radio frequency identification (RF/ID) system, the I² System, to automate grocery tracking and distribution processes.The I² technology is an intelligent system that can accurately scan multiple items at once without sorting, straightening, or unpacking them (ELECTRONIC DESIGN, *July 7, p. 48E*).

The pilot program will first utilize the I2 technology within Sainsbury's chilled foods supply chain, which handles approximately 225,000 crates of prepared meals each week for the company's supermarkets. Merchandise, down to the carton level, will be labeled with SCS's patented Dura-labels at vendors' locations and will be tracked through Sainsbury's distribution centers to retail supermarkets, and also into each supermarkets' cold-storage facilities.

For more information, contact SCS Corporation, 10905 Technology Place, San Diego, CA 92127; (619) 485-9196; fax (619) 485-0561; e-mail: info@scs-corp.com.

In an acquisition that puts them in the thick of the embedded systems industry, Sun Microsystems, Mountain View, Calif., has purchased French software vendor Chorus Systems for an undisclosed amount.

According to Tom Williams, *Electronic Design's* Embedded Systems/Software editor, Sun plans to adapt Chorus' real-time multithreaded kernel to its own JavaOS to support the Java language for embedded network systems. In addition, Sun is staking its position in the enterprise with networking and server technology in terms of its existing Solaris operating system.

The combination is intended to offer the ability to scale from the very large down to very small networked devices with a memory footprint of less than 10 kbytes. However, Sun still must fit Java's inherent limitations in terms of real-time deterministic behavior (e.g., automatic garbage collection) with the real-time characteristics of the Chorus OS. For more information, see Sun's website: http://www.sun.com.—**MS**

TIPS ON INVESTING

Investors are faced with so many options that only individuals with the time and incentive to devote enormous amounts of research can hope to make consistently good decisions about their investments.

Investors also are aware of the rising costs of funding basic financial goals that most of us share—educations for our children and grandchildren; a comfortable retirement; or care for an elderly relative. These goals should be approached from a long-term perspective, and many individual investors are uncertain as to how to develop a long-term investing strategy to meet them.

HENRY WIESEL
CONTRIBUTING EDITOR

Under these circumstances, many investors are best served by working with financial consultants to retain one or more of the many investment management firms that construct individual portfolios designed to help meet the needs of each client. Professional investment management was once available only to large institutions and wealthy individuals who could afford to commit millions of dollars to long-term investments. However, many prestigious firms now accept accounts at minimums as low as $25,000.

Professional investment managers offer an array of management styles, investment strategies, and portfolio options. These experienced professionals have access to the research capabilities that enable them to sift through all the information that must constantly be analyzed to develop and implement a coherent investment strategy.

Professional managers are conversant with the historical behaviors of the financial markets, and they spend most of their work time following stock and bond activity. They also monitor economic and political developments, which must be factored into a long-term plan to keep it flexible enough to be responsive to short-term challenges and potential opportunities in the investing environment. Such managers work under a clearly defined investment discipline, which removes the emotion that often skews the individual investor's decisions. Finally, these managers have access to institutional-level trading capabilities that produce significant economies of scale.

A financial consultant can be your resource and guide you through the basic steps of selecting a professional investment manager, during which you:

Define your investment goals. To what end are you investing these funds? How long are you able to commit the money? How much risk are you willing to assume?

Identify the professional investment manager(s) whose investment styles, risk/return profiles, and performance histories are compatible with your needs.

Monitor the activity of the managers you choose. Make sure you understand clearly how the manager calculates performance data, as there is no industry standard for reporting results.

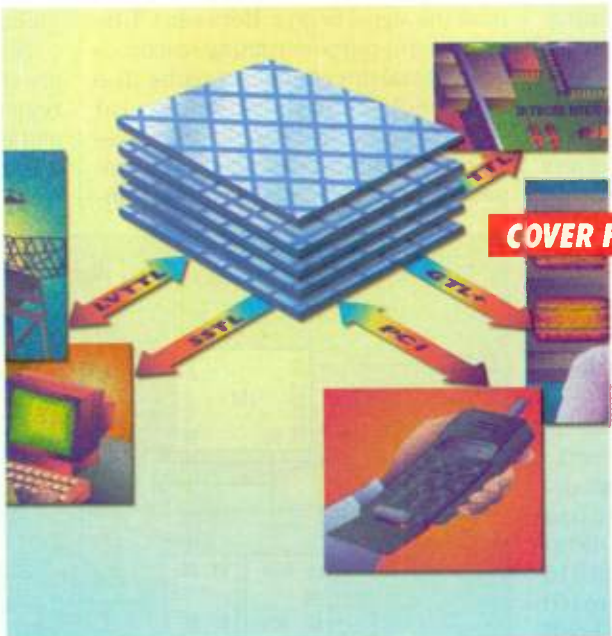
Professional portfolio management is one method of making intelligent investment decisions. For many investors, the results can be highly satisfactory.

Henry Wiesel is a Vice President, Financial Consultant, and Qualified Pension Coordinator at Smith Barney. He may be contacted at 1040 Broad St., 2nd Floor, Shrewsbury, NJ 07702; (800) 631-3331, ext. 8563.

High-Density FPGA Family Delivers Megagate Capacity

Combining Blocks Of Embedded SRAM With Up To One Million Gates, The Virtex Family Will Operate In 150-MHz-Clock Systems.

Dave Bursky



COVER FEATURE

Higher density and greater performance are the two mantras that every supplier of field-programmable gate arrays (FPGAs) has been reciting over the last few years. Coincidental with their efforts to craft denser and faster circuits, process technologies have advanced such that 0.25-µm design rules and five levels of metal interconnects can now be used to implement advanced FPGA architectures.

Taking advantage of those process advances are designers at Xilinx, San Jose, Calif. They've crafted their next generation family of SRAM-based FPGAs to offer from less than 20 kgates to over 500 kgates in the initial release, with utilization percentages of more than 90%. And, by late 1998 the family will offer up to one million gates, and the ability to operate at system clock rates of over 150 MHz.

Initial family members will include devices with from 2000 to over 20,000 logic cells [each cell contains the equivalent of one four-input look-up-table (LUT) building block and one register], and from 120 to over 600 user I/O pads. The first family member to be sampled will pack 6000 logic cells and 260 I/O pads. The I/O lines will offer plenty of system flexibility, providing configurable levels such as GTL+, LV TTL, SSTL3-I, and SSTL3-II.

Furthermore, the SRAM-based parts will allow fast system configuration. A 2-Mbit configuration file (for a 100-kgate chip) requires less than 3 ms to upload over an 8-bit interface using the byte-wide express mode. The short upload time allows the system to reconfigure the logic with minimal delay in its operations, permitting designers to reuse the logic in a system to reduce hardware cost.

In addition to abundant routing resources, designers at Xilinx crafted a novel virtual diagonal interconnect (VDI) scheme (sometimes called vector-based interconnect) that allows accurate prediction of delays in a net. The prediction is based solely on the straight-line distance between the source and load, without needing the number of vertical and horizontal tracks used. The VDI scheme will allow designers to work with very accurate interconnect delay models, making macroblock placement very flexible.

Core logic in the Virtex family of FPGAs is designed for operation from 2.5 V. The I/O buffers are designed for 3.3-V operation and are 5-V tolerant, allowing the circuits to tie into 5-V systems. Improved logic cells contain a four-input LUT and a D-type flip-flop or latch with common Clock, Clock-Enable, and Set/Reset signals, but have individually selectable polarity for each control signal *(Fig. 1)*. Logic cells are paired together to form a slice. Two slices are grouped together to form a configurable logic block (CLB). Supporting the high-speed clocking are on-chip PLLs that help minimize signal skews, perform clock multiplication, and allow the chips to handle the stringent timing requirements of buses such as the 66-MHz version of PCI.

Built For Speed

The cells within a CLB also have high-speed carry-propagation logic to minimize delays when multiple blocks are cascaded. Therefore, large, high-speed functions such as 100-MHz 32-bit counters or ALUs can be implemented. Dedicated carry logic also is included to ease the implementation of multipliers, allowing very efficient implementation of shift-and-add operations. The more-efficient implementation saves one logic level of delay and reduces the area by about 30% over the area typically required for a 16-by-16-bit binary-tree style multiplier. A 16-by-16-bit binary-tree multiplier with no pipelining runs at 50 MHz (20 ns), while a four-state fully-pipelined version runs at 83 MHz.

Additionally, the logic functions can readily handle high-speed pattern decoding operations. Dual three-state buffers provide designers with independent output-enable signals. Each of the flip-flops can be programmed individually to serve as either a transparent or level-sensitive latch, or as a D flip-flop.

At the heart of each LUT is a 16-bit static RAM that can either be used for logic-function lookup, or can serve as a 16-word-by-1-bit static memory that can be combined with other LUT RAMs to form registers, buffers, etc. Additionally, two four-input LUTs can be combined to form an independent five-input LUT or a 4:1 multiplexer. The four-input LUT has a basic delay of just 1.2 ns.

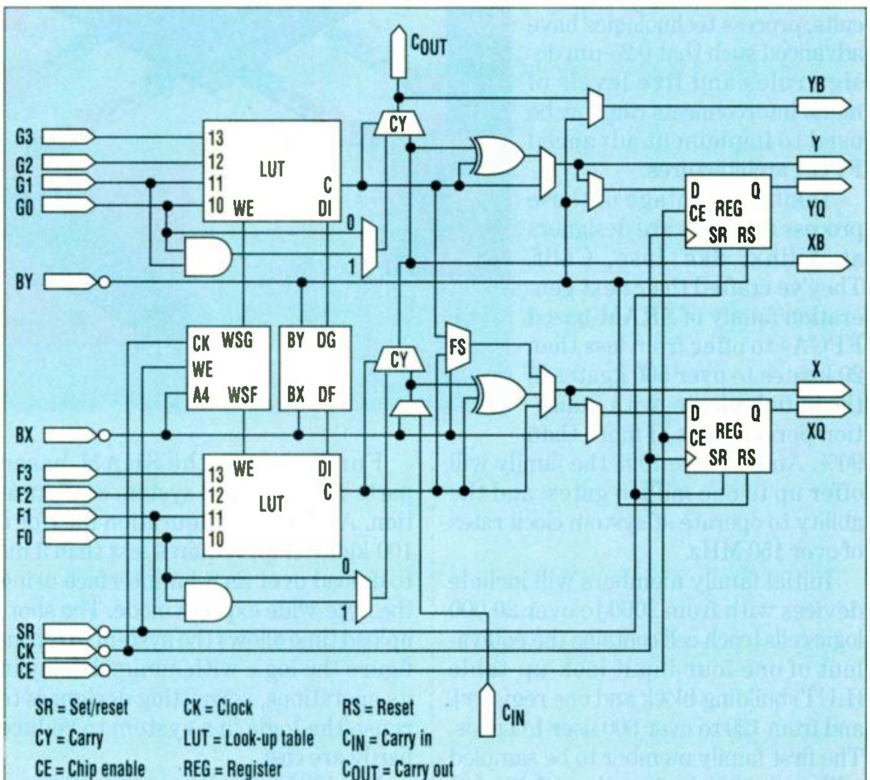
When used in a registered system, the I/O blocks allow a logic function to offer a registered clock-to-output delay of 6 ns without the PLL, and 3.5 ns with the PLL. Maximum I/O data-transfer speeds can take place at 110 MHz without the PLL, and at up to 160 MHz with the PLL. Such I/O cell speeds will allow the implementation of circuit functions such as 155-MHz SONET data-stream processors or 66-MHz PCI-bus interfaces (at 3.3 V). Additionally, the availability of on-chip RAM and a synthesis-friendly logic-cell structure will allow many new complex system functions to be implemented on the FPGAs.

The arrays also contain dedicated blocks of true dual-port static RAM, from eight to 30 blocks of 4 kbits each. Each block can be configured into several aspect ratios (word depth by word width) of 4 k by 1, 2 k by 2, 1 k by 4, 512 by 8, or 256 by 16. The blocks are integrated onto chips with from 20 to 200 kgates. The SRAM blocks are fully-synchronous and have cycle times of less than 10 ns. The five-level metal process used to fabricate the chips gives designers plenty of routing resources. That allows the SRAM blocks to be configured in any desired width. Five blocks can be combined to form a 2-kword-by-10-bit video line buffer, nine blocks can be combined to form a 4-kword-by-9-bit FIFO buffer with parity, or four blocks to form a 2-kword-by-8-bit FIFO.

The internal structure of the FPGA consists of an array of VersaBlocks, each of which contains a general routing matrix and a configurable logic block *(Fig. 2)*. There are four logic cells per CLB, and each logic cell, as mentioned earlier, consists of a four-input LUT. Inside the CLBs are fast routing paths (called fast feedbacks) to minimize the signal delays. Between CLBs are general-purpose routing resources and several direct-connect paths. The fast-feedback paths allow several LUTs to be chained together to implement wider functions with minimal impact on performance. The direct-connect paths provide high-speed interconnections directly between two adjacent CLBs in the horizontal direction, bypassing the extra loading of the general routing matrix.

Associated with each VersaBlock is a general routing matrix (GRM) that includes the switch matrix through which horizontal and vertical routing resources connect. This matrix also is the means by which the general-purpose routing lines gain access to the VersaBlock. Single-length lines connect signals from one GRM to the next adjacent GRM, while buffered Hex lines connect signals from one GRM to another, a distance of six blocks away. Long lines span the length of the chip (vertical long lines), or the width of the chip (horizontal long lines). These lines are buffered wires capable of distributing the signals across the circuit quickly and efficiently.

Surrounding the core of the FPGA are the I/O buffer cells, which contain registered inputs, registered outputs, and three-state enable control *(Fig. 2, again)*. Through the configuration software, some basic characteristics of the



1. Two logic cells and their associated logic form a slice in the Virtex FPGAs from Xilinx. Two such slices form one configurable logic block. Each logic cell has four inputs and contains a 16-bit SRAM look-up table and a configurable D-type flip-flop. The two logic cells in the slice share a common carry logic chain and the flip-flop control signals.

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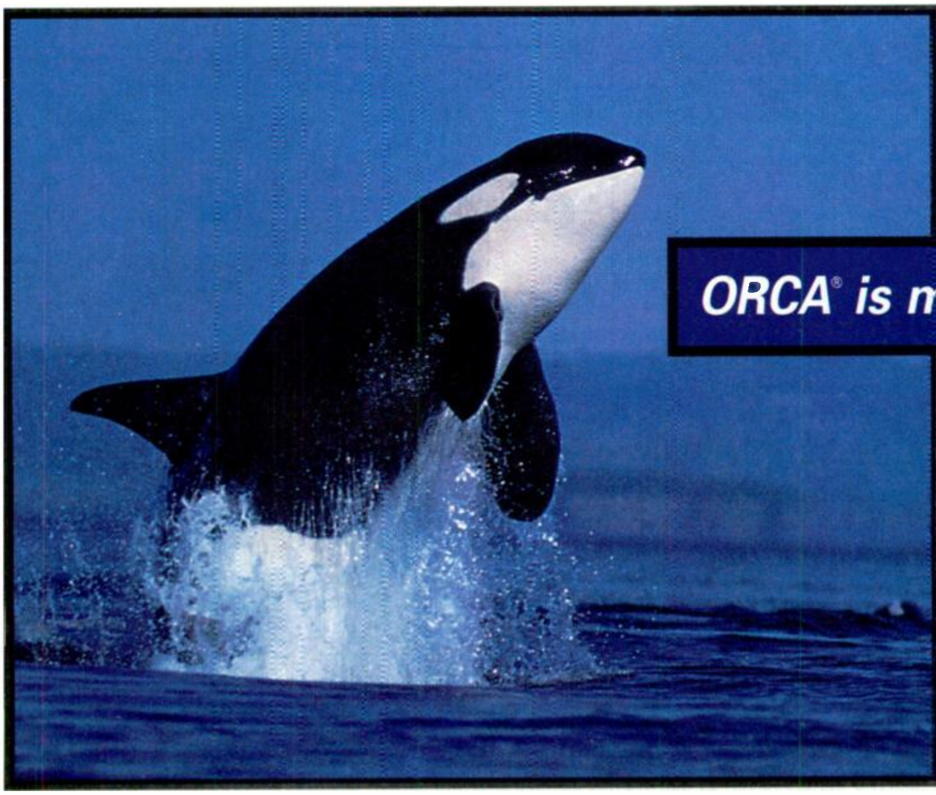

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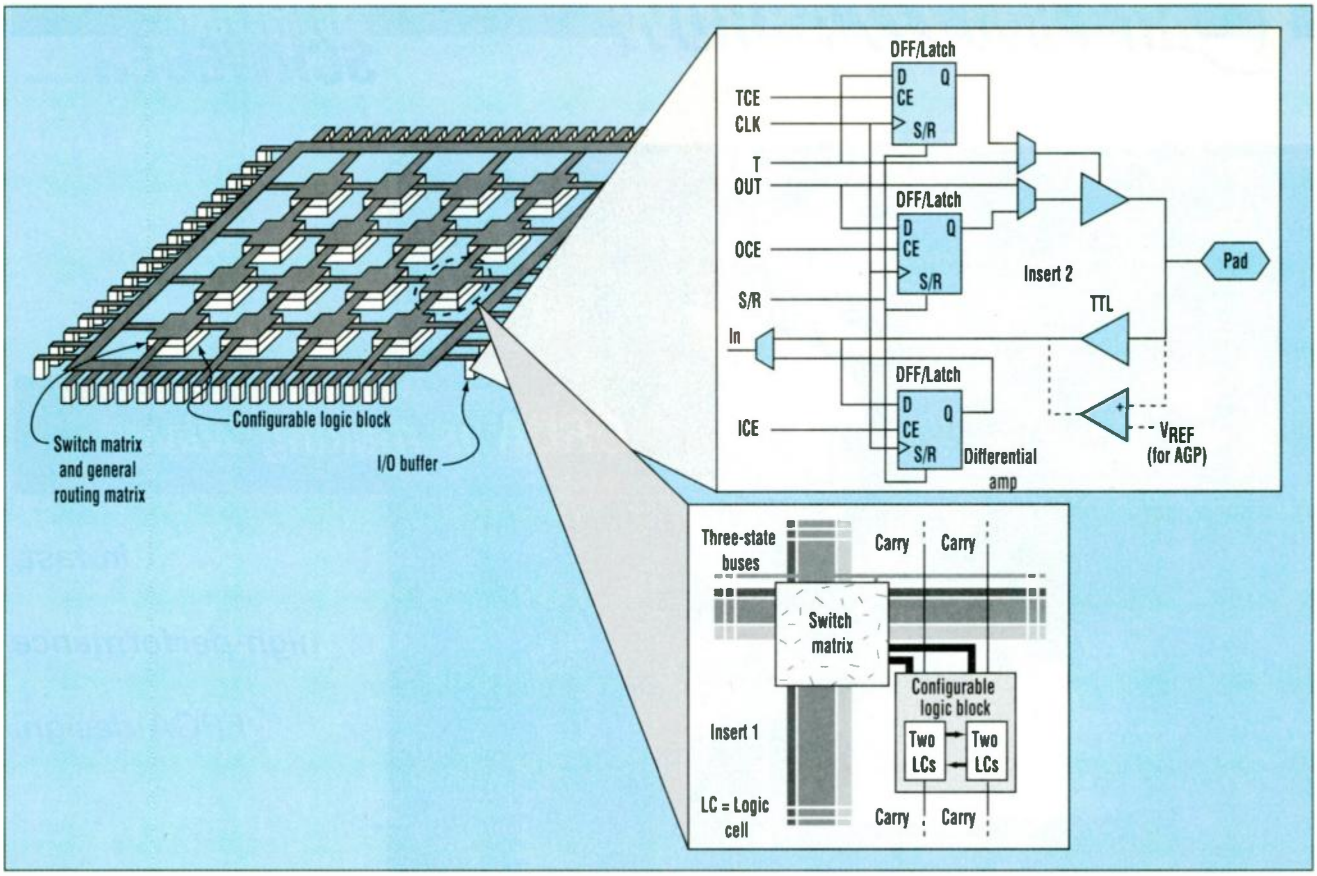

2. The core of the Virtex FPGAs consists of an array of configurable logic blocks (insert 1), each associated with an overlying switch and general routing matrix. Surrounding the logic array are the flexible I/O buffers (insert 2) that provide multiple interface options and offer programmable slew rates.

cell can be set, like slew rate, pull-up, input delay, and other aspects of buffer operation. Bus interface options, selectable at configuration time, include GTL+, SSTL, or LVTTL.

Abundant Routing

Routing resources are loosely divided into three categories: global routing, I/O routing, and dedicated routing. Global routing resources are used to distribute signals with very high fanout throughout the entire device (8 ns to cross a 100-kgate device). There are two tiers of global routing resources—primary and secondary. Primary resources are dedicated global nets that are intended to distribute high-fanout clock signals with minimum skew. All CLB and I/O buffer clock pins can be driven by a global buffer. Secondary routing resources consist of global routing backbones per CLB column. These backbones can distribute any high-fanout signal via the long lines in the column; the resources also are more flexible than the primary resources because the secondary resources are not restricted to which CLB pins may be accessed.

Additional routing resources around the periphery of the chip support the I/O buffers and form the interface between the core logic and the I/O buffers. This routing is referred to as the VersaRing, and is used to facilitate pin-swapping and redesign so that board layouts won't have to be modified if internal logic and I/O buffer connections are updated. Finally, dedicated routing resources are provided to ensure some signals are always available for use to create buses with three-state buffers and carry signals for the dedicated carry logic.

Logic designs on the Virtex family are supported by the company's Alliance Series software, which includes complete support for the unified libraries, relationally-placed macros, and trace capability. The tool suite is based on the next-generation tools for the XC4000X family. It employs a strong constraint-driven design philosophy that works in conjunction with the high-performance predictable interconnect to allow accurate design analysis early in the design flow. The Alliance Series tool suite also has links to most popular EDA tool sets, allowing high-level design and synthesis tools to capture and implement the design. Dedicated IEEE 1149.1 JTAG support with boundary-scan logic allows for both pattern updates and in-system testing to be performed.

Price And Availability

The first Virtex device to be sampled contains 6000 logic cells and 260 user I/O lines. It will sell for between $200 to $400 each in sample quantities, and for less then $90 a piece in large quantities when the chip hits volume production in late 1998.

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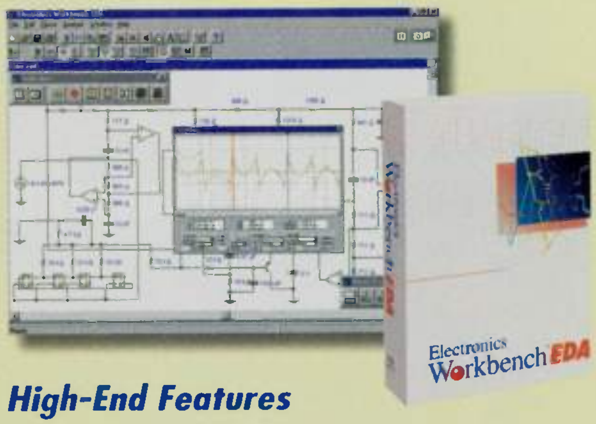

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Advanced DRAM Architectures Overcome Data Bandwidth Limits

Novel Architectures For Next-Generation DRAMs Are Pushing Data-Transfer Rates Beyond 500 MHz While Offering New Features And Control Options.

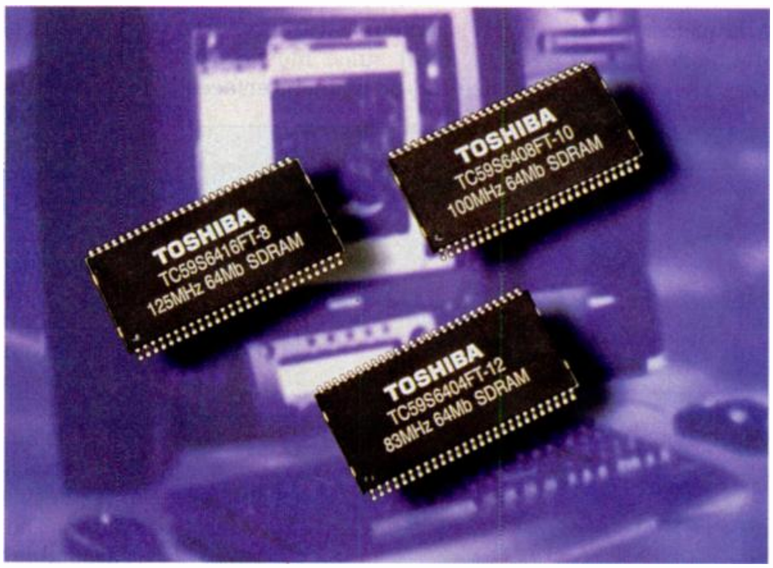
Dave Bursky

SPECIAL REPORT

Today's computer systems and graphics subsystems are pushing standard DRAM architectures to their limits. They also are looking for higher-performance devices that will enable memory subsystem performance levels two to four times faster than fast-page mode or extended-data-out DRAMs. Memory designers are crafting new generations of dynamic memories using synchronous data-transfer schemes, byte-serial transfers with dual-edge clocking, and multibank architectures. These new memory types will allow designers to build memory subsystems that can transfer data at rates up to 1.6 Gbytes/s, allowing the subsystems to keep pace with the fastest CPUs and graphics engines.

As data rates go up, so must memory capacity—at the high data rates projected for new memory chips, current 16- and 64-Mbit devices would be emptied in the blink of an eye. Limited production quantities of 256-Mbit chips are available from several vendors and following the standard 4X progression, prototypes of 1-Gbit and even 4-Gbit DRAMs, have been demonstrated at various research conferences. But as manufacturers try to move from engineering prototypes to production at the 256-Mbit level, they're finding interest in an intermediate 128-Mbit density device that would allow vendors to offer a 4-Mword by 32-bit chip. Two such chips could provide a 32-Mbyte base memory for desktop or portable computers.

There are five architectures competing for the high-speed sockets used in main memory subsystems: the synchronous DRAM (SDRAM), which includes its second-generation brother the SDRAM II, and its soon-to-be-sampled faster cousin, the double-data-rate (DDR) SDRAM; the Rambus DRAM (RDRAM), and its new cousin, the direct RDRAM; the forthcoming SyncLink DRAM (SLDRAM); the Multibank DRAM (MDRAM); and the cache-enhanced synchronous DRAM (ESDRAM), a synchronous version of the original EDRAM. Comparing the key features of the SDRAM, DDR SDRAM, Direct RDRAM, and SLDRAM at the 64-Mbit level provides an interesting blend of similar features and significant differences that designers must deal with *(see the table)*.



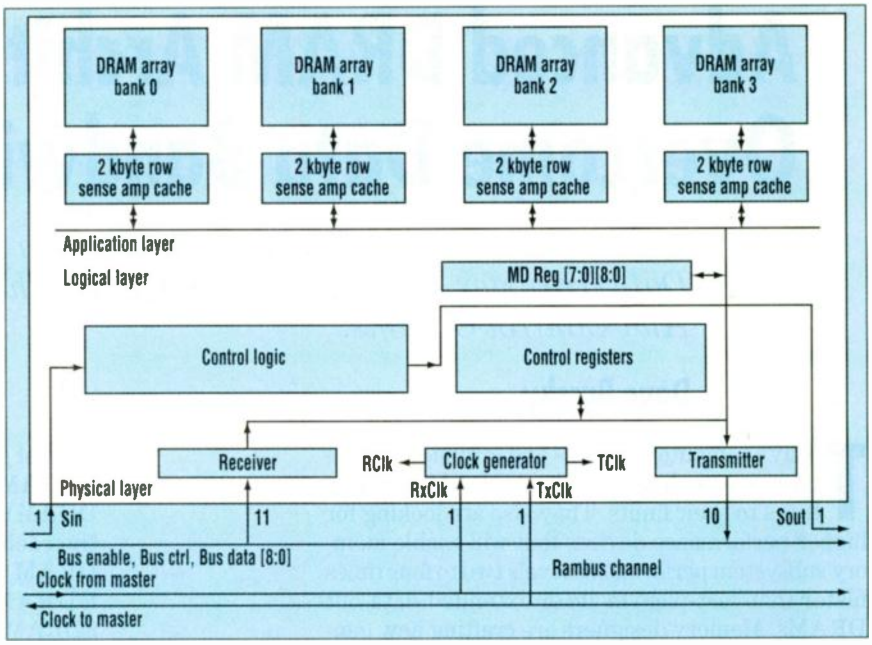
Art Courtesy: Toshiba

Graphics subsystems can take advantage of these memory types to replace the dual-ported video RAMs that are now used only in legacy graphics subsystems. In addition to the previously mentioned memory types, there are some graphics-specific DRAMs that also have been developed—the synchronous graphics RAM (SGRAM), as well as specialty memories such as the Window DRAM. However, they will not be covered in this report.

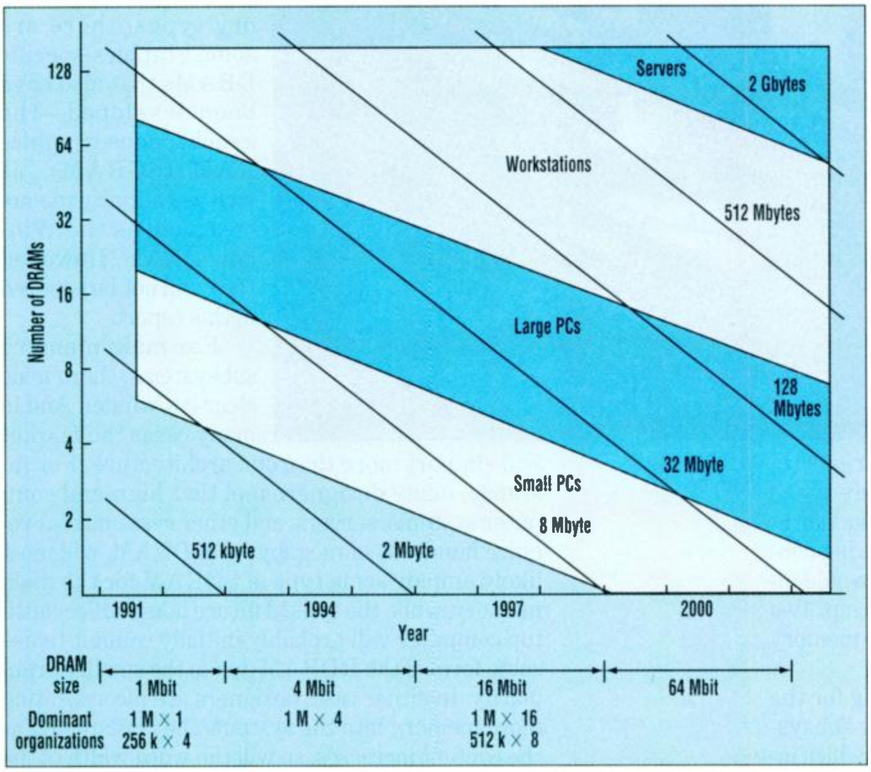
For main memory subsystems, there is no clear-cut winner. And in many cases the market will support more than one architecture. For instance, many designers feel that high-end computer systems, servers, and other systems that require hundreds of megabytes of DRAM, will most likely employ some type of SDRAM for the main memory, while the typical future home-office desktop computer will probably initially commit to use some form of the RDRAM due to the smaller granularity. In either case, designers are incorporating more memory into the systems they create and as the content increases, so will the word width of the memory chips to better deal with memory system granularity *(Fig. 1)*.

The issue of granularity is one that continually raises its head, especially as memory capacity per chip increases. The first sign of the granularity issue emerged years ago, and as a result, DRAMs started to come in word widths of four bits. Reduced ground-bounce and better noise-immune I/O line designs along with higher densities then made practical 8-, 16- and even 32-bit-wide memory chip organizations, and with that the ability to set the desired system granularity. Large memory systems would most often employ narrower word widths since such systems often require a lot of depth, while smaller systems often desire wider word chips since the memory depth is smaller and wide memories could greatly reduce chip count.

For instance, current 64-Mbit SDRAMs are available with word widths of 4, 8, or 16 bits. Assuming a 64-bit-wide memory module, if the unit is assembled with 4-bit-wide SDRAMs, it would have a depth of 16 Mwords, and a total storage of 128 Mbytes; if built with 8-bit-wide SDRAMs, the module would pack 64 Mbytes and have a depth of 8 Mwords. DIMM versions could double that storage by doubling up the memory. And the even larger DIMM modules, such as those used in workstations or servers, could pack even double the 64-bit DIMM amount (up to 512 Mbytes/module) since most large DIMMs use 128-bit-wide interfaces.



2. Multiple DRAM banks in the concurrent RDRAM developed by Rambus are each associated with a 2-kbyte sense-amplifier cache. On-chip control logic handles read and write operations performed in cooperation with a synchronous, concurrent protocol that handles the block-oriented, interleaved (overlapped) data transfers.

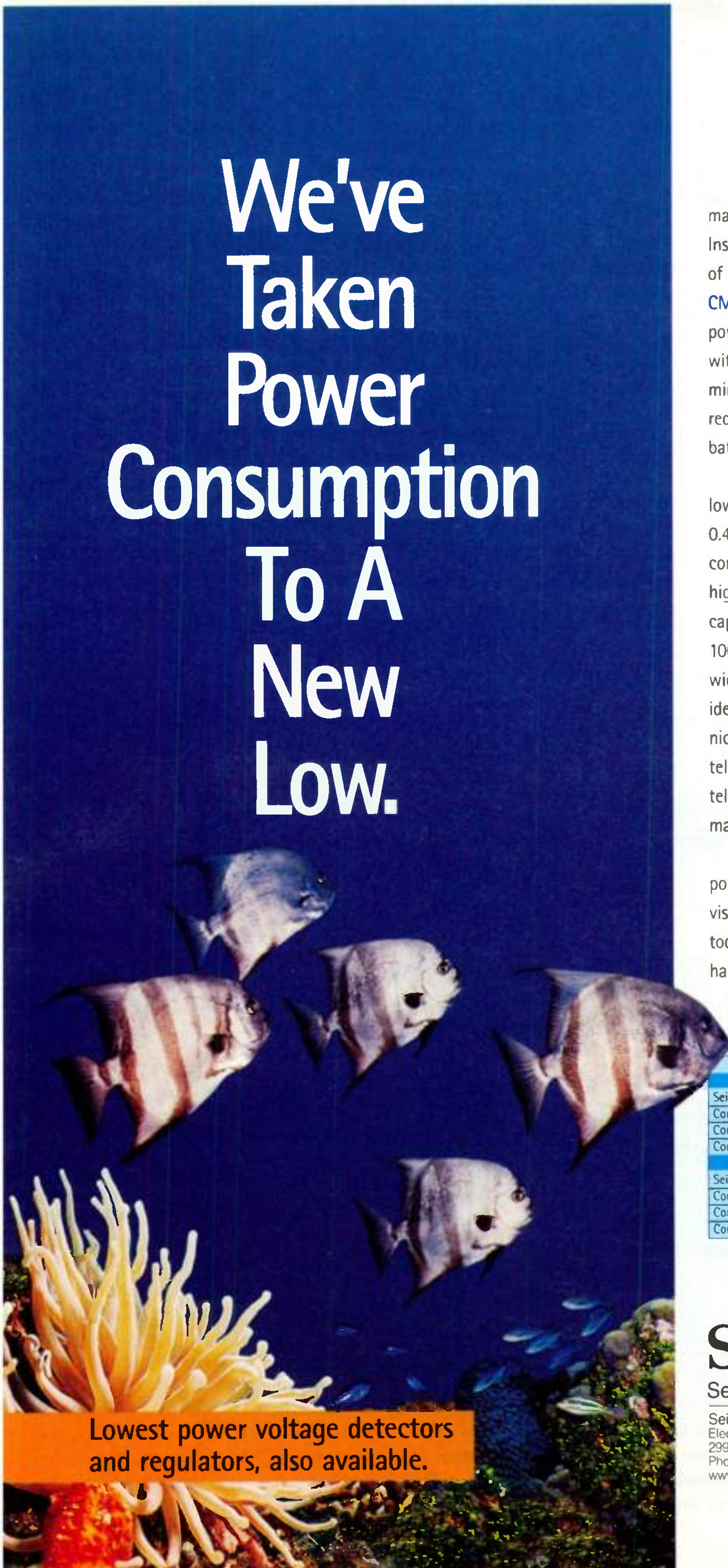


1. The size of a memory subsystem and the choice of available memory organizations at a particular storage density level often determines the granularity of the memory upgrade as this graph from Hitachi depicts.

Such storage capacities are so large that small-system users would be hard-pressed to afford memory upgrades. Graphics subsystems are looking at even wider DRAMs—chips with 32-bit data ports are a better fit since most graphics systems require 8 Mbytes or less of memory, and just two to four chips would supply the entire memory space.

Wider organizations such as a 4-Mword by 16-bit device would reduce the SIMM granularity to 32 Mbytes using just four SDRAMs. That would permit manufacturers to offer affordable modules. Alternatively, memories such as the 16-Mbit RDRAM use a byte-serial approach to transfer data bytes between the memory and the system. The host system would then reassemble the wide data words for storage in the cache. Thus, a small memory upgrade module that contains as little as 2 Mbytes (one chip) can provide the desired upgrade options. For instance, in the case of the Nintendo 64 video game, which uses a single 16-Mbit RDRAM for the internal memory, a plug-in memory expansion module contains just a single 16-Mbit RDRAM, thus doubling the system's memory *(see "The impact of advanced DRAM technologies," p. 80)*.

Of all the interfaces discussed and proposed, only the EDRAM, SDRAM



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EEPROM Power Consumption Comparison Chart

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Competitor 1	1.0 mA	1.0 µA
Competitor 2	2.0 mA	50.0 µA
Competitor 3	0.5 mA	30.0 µA
[illegible] WIRE (24C)		
Seiko Instruments	0.3 mA	1.0 µA
Competitor 1	3.0 mA	100.0 µA
Competitor 2	2.0 mA	100.0 µA
Competitor 3	1.0 mA	30.0 µA

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and RDRAM are currently in production. Engineering samples of the cache-enhanced synchronous DRAM are expected shortly from Enhanced Memory Systems, and the first prototype of the SLDRAM is currently in design by Toshiba, Siemens, and Mosaid Technologies, and is targeted for sampling in late 1998. The second-generation SDRAM and the DDR SDRAM are slated for sampling late this year and in early 1998, respectively, while Direct RDRAM chips also are in design but targeted for sampling in mid-to-late 1998.

Each of these memory interfaces has its pros and cons that technically fall into several categories—latency, bandwidth (peak versus sustained), and scalability. Latency is the time required from an initial request to obtain the first data. In older DRAMs this is the equivalent of access time, but since the advent of static-column and fast-page mode, DRAMs have a burst transfer mode that lets them transfer as little as a page or up to the entire contents of the memory chip. The memory latency—the time to the first access—is as important as the time for each subsequent data word in the transfer sequence (the burst length).

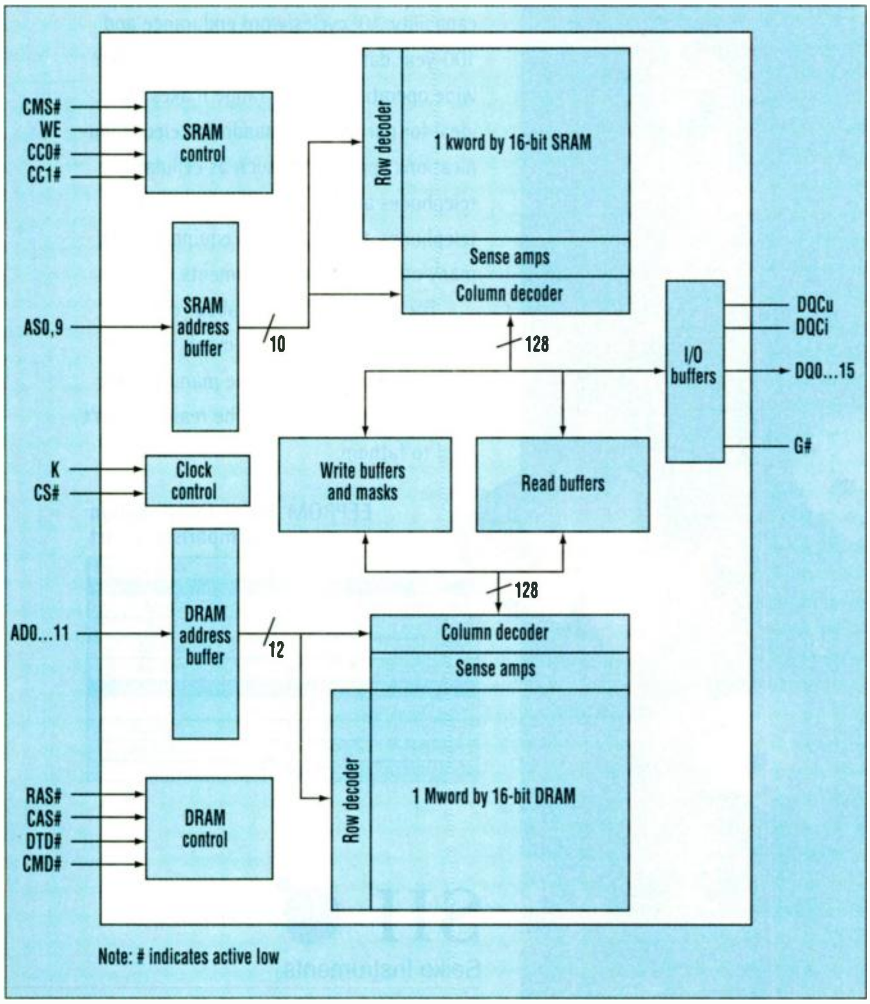
The sustained bandwidth that the memory can achieve is then the burst size (the number of sequential accesses) divided by the total access time, which can result in a sustained bandwidth value that can be less then half the peak bandwidth. Although 16/18-bit (parity) versions of the RDRAM are not yet available, projected peak bandwidth for the SDRAM, RDRAM and SLDRAM are roughly 400 Mbytes/s for the 100-MHz SDRAM, over 1.5 Gbytes/s for a projected 16/18-bit RDRAM, and about 800 Mbytes/s for an SLDRAM.

In terms of scalability, the SDRAM, DDR SDRAM, and SLDRAM can be used in typical 2D memory arrays that can expand the word depth or word width and provide simple memory subsystem extensions. The RDRAM and its forthcoming Direct RDRAM cousin require a different approach since they use byte- and word-serial system interfaces, respectively, and employ a host-system interface controller that receives the byte/word serial data from the memory chips and reassembles the 32- or 64-bit wide-word data or instructions, or breaks wide word information into the byte/word-serial stream for transfer to the memory subsystem.

In many systems, a single RDRAM interface controller will typically be used to access a linear array of RDRAM chips over an 8/9-bit data bus. That interface is more pin-efficient than the SDRAM since data and addresses are sent over the common RDRAM bus. Although the bus is narrower than the wide-word memory bus formed by an array of SDRAMs, the higher clocking rate (over 600 MHz) gives the bus its high performance. However, one interface controller is pretty much assigned for one bank of RDRAMs. If a second bank were needed to increase bandwidth, a second controller would have to be added along with the memories, rather than just adding another row of memory chips.

In main memory systems, latency was very important when cache sizes were small. However with substantial on-chip caches and external level-2 caches, most of the memory latency for cache fills is hidden. But on cache misses, the time to reach the first data word is critical since without data, the CPU could stall, slowing the entire system. Most of the clocked memories do have a two- or three-cycle penalty to reach the first data word, but then make up for the latency by transferring the remaining words very rapidly.

The original RDRAM had a large latency (several hundred nanoseconds) that basically detracted from the device performance when the chips were evaluated for use in main memory systems. However, for graphics applications that



3. One of the first attempts to speed up DRAM access time was the cache DRAM that is now available from Enhanced Memory Systems. The memory's internal architecture consists of a standard DRAM storage array and a cache that's formed from the sense-amplifier array. The cache and the memory array are linked by a wide on-chip bus so that the entire cache can be loaded in just a single cycle.

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used long strings of data transfers, the RDRAM delivered top-notch performance and has now found a home on several graphics and multimedia cards.

Souped-Up Memory

Many timing and feature improvements have been made to the RDRAM in its second-generation implementation, the Concurrent RDRAM, to optimize it for use in main memory subsystems. The Concurrent RDRAM will be available in 8-bit- or 9-bit-wide versions in either 16/18- or 64/72-Mbit capacities and can burst unlimited-length strings of data at 1.67 ns/byte (600 MHz). The sustained bandwidth for 32-byte transfers (a cache line fill, for example) is 426 Mbytes/s—a speed faster than any other DRAM approach. Although Rambus has architected the memories in conjunction with various partners, it does not manufacture or market the chips. Rather, Rambus licenses the controller interface cell and the memory design to its silicon partners. Those licensees include Hitachi, LG Semicon, NEC, Oki, Samsung, and Toshiba. Other suppliers also have signed on to produce the forthcoming Direct RDRAM—Fujitsu, Hyundai, IBM, Siemens, Texas Instruments, Micron, and Mitsubishi.

Internally, the 64/72-Mbit Concurrent RDRAM is divided into four banks (two banks in the 16/18-Mbit version), with each bank assigned 2-kbyte (1 kbyte in the 16/18-Mbit chip) row sense amplifier cache, much like the cache DRAM from Enhanced Memory Systems. The multiple banks are tied into on-chip control logic that handles the read and write operations *(Fig. 2)*. The chips employ a synchronous, concurrent protocol to handle the block-oriented, interleaved (overlapped) transfers and like the original RDRAMs, have only 16 active signals and require a total of just 32-pins on the controller interface.

A low effective latency, competitive with SDRAMs, is possible by operating the two or four 1- or 2-kbyte sense-amplifier banks as high-speed caches and using a page-type random-access mode to deal with large block transfers. Concurrent (simultaneous) bank opera-

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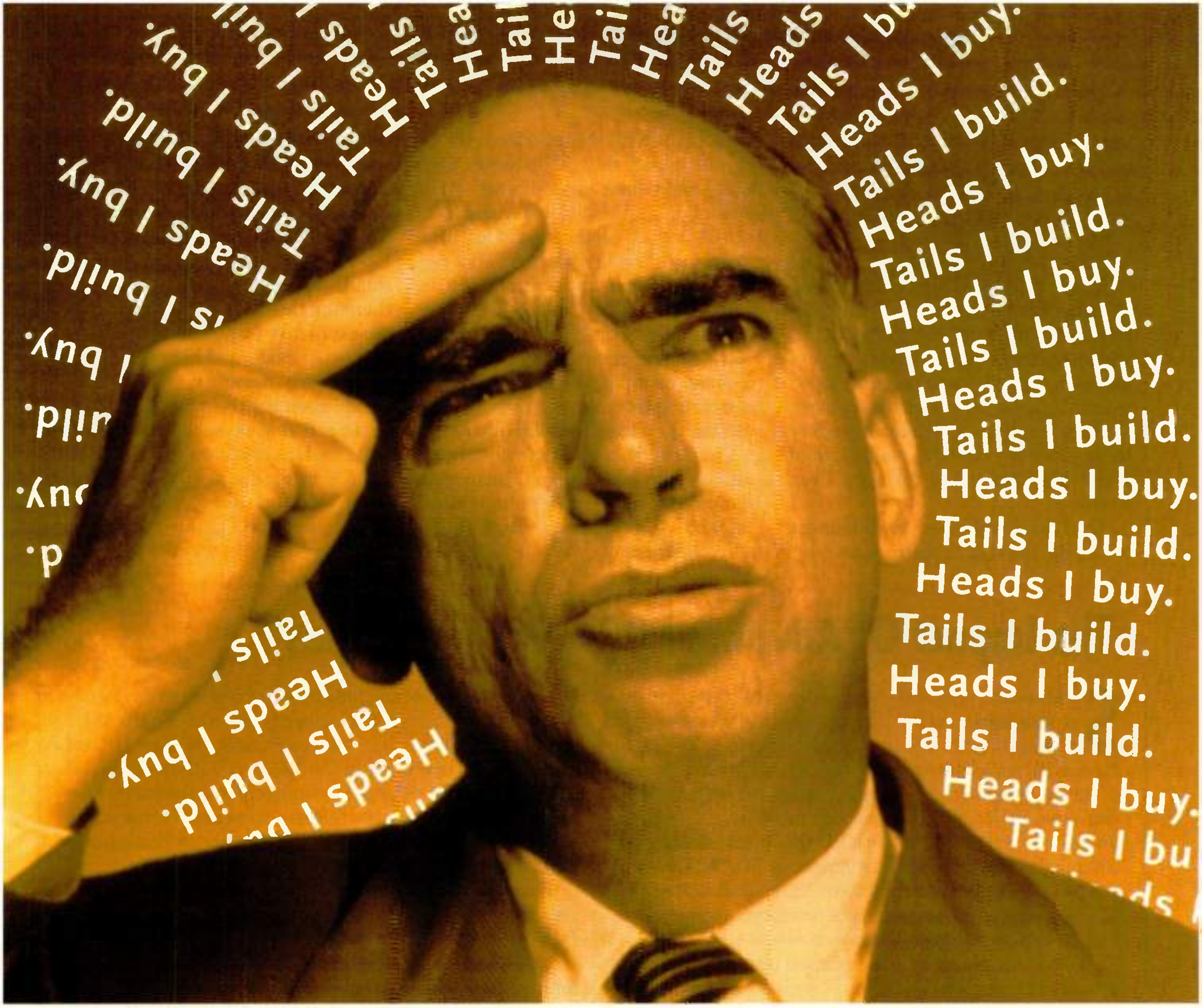
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tions yield a high effective bandwidth by using interleaved transactions. For graphics applications the memories also include write-per-bit and mask-per-bit capabilities.

Further enhancements to the RDRAM will arrive by mid-1998 when Rambus and its partners release samples of the Direct RDRAM, a 16/18-bit-wide version of the RDRAM. The enhanced interface was jointly developed with Intel to better match the memory to Pentium CPUs and deliver roughly three times the effective bandwidth of a 100-MHz SDRAM for a random workload.

The DRDRAM interface will consist of a 16- or 18-bit data path and an 8-bit control bus, with the interface able to operate at clock rates of up to 800 MHz (rising and falling edges of a 400-MHz clock). DRDRAMs will be available in both 64- and 128-Mbit densities for main memory applications, and a 32-Mbit device for graphics applications also is planned for release in late 1998. The chips are essentially the first super-pipelined memories that offer a multiple-transaction pipeline and conflict-free transaction interleaving to achieve a sustained performance of 1.5 Gbytes/s.

The electrical interface will be the same as that used in the Concurrent Rambus interface—differential clocks and a 1.8-V termination voltage. Internally, the memory will use a 128-bit-wide core so that a quad-word (16-byte) transfer can be done internally on every cycle. In addition, the DRDRAM chips will operate from a 2.5-V supply, employ a 0.8-V signal swing around a 1.4-V reference level, and incorporate some low-power modes to better suit them for the mobile systems market (just 0.75 mW on power-down, 10 mW in the nap mode, and between 500 and 600 mW when doing reads or writes). Complementing the memory chips will be the Rambus access controller (RAC) which can support a single DRDRAM interface or two Concurrent RDRAM interfaces.

Another aspect defined by Rambus for all its memories was the packaging,

The Impact Of Advanced DRAM Technologies

Synchronous DRAMs, originally expected to make a strong impact on PC performance in 1997, have yet to do so primarily due to technical obstacles. The fix for those SDRAM challenges is hopefully now in place in terms of new chip sets, tighter timing specs for both SDRAM chips and SDRAM-based memory modules, plus a higher awareness on the part of both PC OEMs and the supplier community. But if the implementation of SDRAM architecture seems to have been problematic, the technical difficulties of transitioning to even more advanced memory architectures are incrementally more severe.

Workstations and PCs are pointed toward an abruptly upscaled performance plateau. These powerful new systems will require synchronization and tight coupling between the CPU, the chip set, the memory modules, I/O ports, motherboard, and peripherals far beyond anything that's been achieved so far.

Even in the most advanced systems available, with the SDRAM memory bus operating at 100 MHz, there is only 10 ns available for a clock cycle. The SDRAM itself requires up 6 ns, leaving about 4 ns for all other timing aspects combined. As evidenced this past year, that limited time has proven to be an enormous challenge explains Bill Johnston, V.P. of Product Marketing for Smart Modular Technologies Inc., Fremont, Calif. Now new DRAM architectures, with Rambus currently the front runner, are promising operating frequencies of 400 to 600 MHz, which will drive clock cycles down to 2.5 and 1.6 ns, respectively.

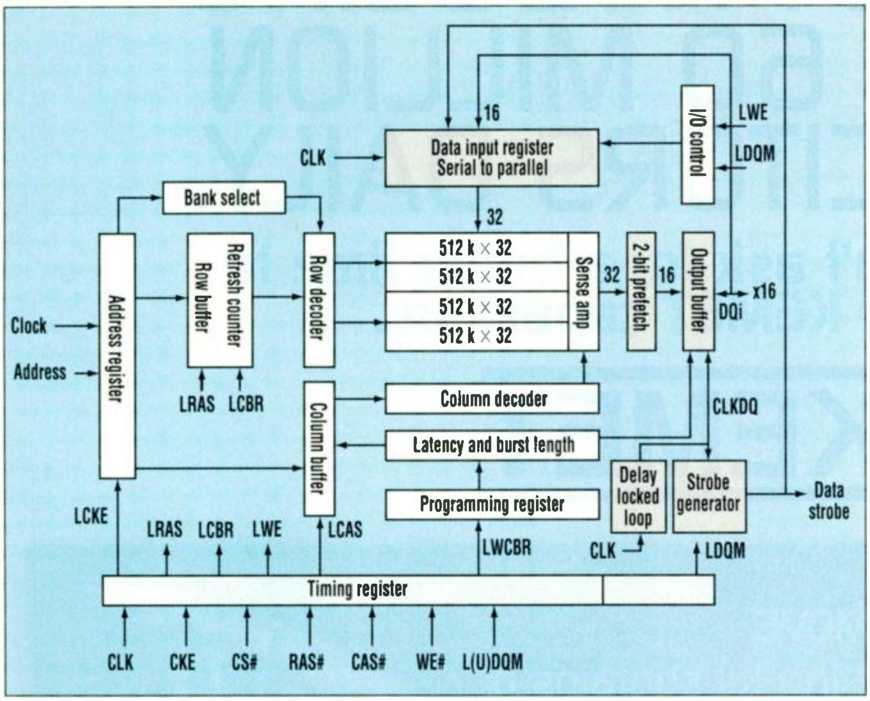
For independent memory-module manufacturers, continues Johnston, the design constraints for these advanced modules will contribute to a supplier fallout already triggered by escalating manufacturing and test requirements. Module manufacturers already are faltering if they are not equipped and experienced with cutting-edge surface-mount technology and advanced test equipment that can run at 300 MHz and beyond. To ship parts at a quality level that OEMs expect, module manufacturers must perform both full parametric and full functional testing at frequency with various patterns, testing every bit on every DRAM.

It is likely that in less than two years, the new DRAM architectures operating in the 400-to-600-MHz range will require 660-MHz testing to adequately test the parts. Few independent memory-module suppliers are positioned today to provide even the 330-MHz capability and have the financial resources to maintain that leading edge.

Furthermore, explains Johnston, the additional design engineering expertise required for Rambus-based DIMMS, or the equivalent with competing DRAM architectures such as SLDRAM or DDR DRAM, raises the ante for memory module design competence. There are new design challenges as systems transition from simple connection of DRAMs on a pc board to microstrip-line and transmission-line design.

To simulate signal-integrity of the module design, the memory controller model, the connector model, and of course the detailed modeling of the traces and components on the module must be considered. Major OEMs have begun requiring simulation data from module makers so that data can be included in their system simulations. In addition to these design constraints, if any memory-module maker is not, for example, already implementing micro-ball-grid-array (MBGA) packaging competence, it has little chance of surviving this next transition phase.

The implications also are severe for buyers of memory modules, whether they are PC OEMs or individuals in the aftermarket. It is likely that for advanced-DRAM-based modules, only module designs that have been simulated, tested, and finally verified by actual operation in a specific system will meet performance requirements. PC OEMs will partner much more tightly with carefully selected memory module suppliers, and the memory aftermarket may be controlled exclusively by the OEMs who manufacture the systems, with consumers buying only modules specified for a particular system.



4. Employing four 32-bit-wide memory banks, the bidirectional double-data-rate SDRAM developed by Samsung includes some additional circuits such as a strobe generator and a delay-locked loop. These circuits provide all the timing signals needed to minimize timing margins and provide the chip-to-host signaling.

but not just at the chip level. Board layouts and proprietary module layouts also were defined to ensure the memories would deliver their best performance. With the DRDRAM, Rambus and Intel have opted to use the micro ball-grid array, a chip-scale package that reduces lead inductances and board area. And at the module level, they have moved to standard form factors such as DIMMs, which will allow 1, 2, or 3 modules per channel and support serial presence-detect signals for module identification.

Reducing The Latency

One of the first memories to tackle the latency issue—the cache DRAM developed by Enhanced Memory Systems—combined a DRAM and a 4-kbit cache on the same chip. The cache is actually formed by the sense-amplifier array and some additional logic and allows the memory chip to provide standard access times for a random read (with no matching information held in the on-board cache). However, after the standard row access time for the first piece of data (25 ns), subsequent data transfers can take place in just 10 ns per transfer if the desired data is now in the cache. (The random read causes the contents of the page in which the data resides to be transferred into the 4-kbit cache; subsequent read accesses to the same page are read from the cache.)

Although the initial memory was only a 4-Mbit device, the company is now sampling a 16-Mbit version based on synchronous DRAM technology that includes a four-bank organization to achieve the high transfer rate—27-ns row accesses and 12-ns column accesses *(Fig. 3)*. When fitted with LV TTL I/O buffers, the memory will be able to operate at 133 MHz and perform 1-1-1-1 transfers at 66 MHz, 2-1-1-1 transfers at 133 MHz, and 3-1-1-1 transfers at 200 MHz. That speed is about double that of standard DRAMs. IBM is now the only alternate source for the EDRAMs.

The 16-Mbit synchronous DRAMs, with their dual-bank architecture were the first mainstream (multiple-sourced) new architecture memories to offer performance levels well above that achievable with extended-data-out DRAMs. However, first-generation 16-Mbit SDRAMs, although specified as 100-MHz devices, actually delivered performance levels well below the claimed 100-MHz clock speeds.

Although the SDRAMs are designed to a JEDEC standard, slight differences in the interpretation of the specification and the test methodologies have made interchangeability a concern. Though the chips were capable of 100-MHz system operation under ideal conditions, due to timing differences in most PCs they have limited operation to 66 MHz. Subtle spec differences often prevent "blind" interchangeability between different company's ostensibly identical memories.

In fact, according to Art Kilmer, manager of memory applications at IBM, the latest x86 motherboard chip sets that support SDRAMs have brought out the differences in SDRAMs that are available from various manufacturers, and it will take a while to figure out which tests are best to assure interchangeability. One issue with the memories is the number of banks that can stay open when the host

A COMPARISON OF NEXT-GENERATION 64-MBIT DRAMs

Parameter	DDR SDRAM	Direct RDRAM	SLDRAM	Today's SDRAM
Bandwidth	1.6 Gbytes/s	1.6 Gbytes/s	1.6 Gbytes/s	0.8 Gbytes/s
Clock frequency	100 MHz	400 MHz	200 MHz	100 MHz
Data-transfer frequency	200 MHz	800 MHz	400 MHz	100 MHz
Bus width	16 bits x 4	16 bits	16 bits x 2	16 bits x 4
Granularity	32 Mbytes	8 Mbytes	16 Mbytes	16 Mbytes
Package/module	TSOP/DIMM	To be determined	VSMP/DIMM	TSOP/DIMM
System power (4 devices/system)	1500 mA	1200-1500 mA	1000 mA	500 mA
Active power (1 device)	375 mA	1000-1300 mA	440 mA	125 mA
Hard-error recovery capability	Excellent	Limited	Excellent	Excellent
Application	Midrange-high end	Low end-midrange	Midrange-high end	Low end-high end

Source: Hitachi

system performs bank-to-bank interleaving. The latest "BX" chip set from Intel allows up to 32 banks to stay open, but the timing and loading issues have yet to be fully analyzed.

To boost SDRAM performance, memory designers have tightened some of the ac timing margins, dc parameters, driver characteristics, and layout rules on first-generation 16-Mbit parts to achieve "true" 100-MHz operation to meet the so called PC-100 100-MHz SDRAM specification requirements for 100-MHz system operation. *(Details are available on the Intel web site: http://www.intel.com/developer.)* Memory designers also are pushing process technology to achieve even higher speeds—clock rates of up to 143 MHz will be sampled in early 1998. Specifications for DIMMs, both unbuffered and buffered and registered DIMMs, with capacities up to 256 Mbytes, also are defined on the Intel web site.

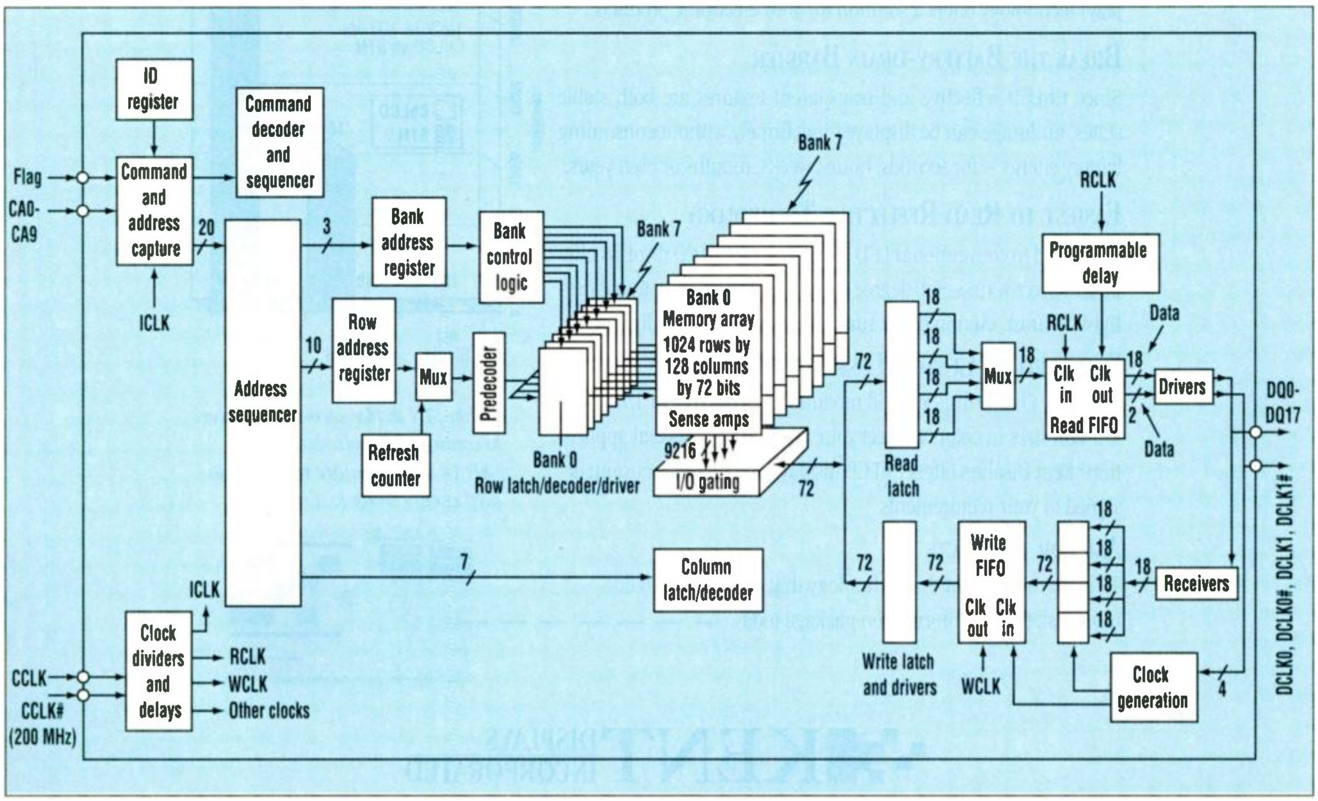
The 16-Mbit generation, though, is giving way to higher-performance 64-Mbit devices that employ four banks per chip. SDRAMs in the 16- and 64-Mbit generations are available with word widths of 4, 8, or 16 bits, and a few companies are considering a 32-bit-wide SDRAM at the 64-Mbit and 256-Mbit levels. When fabricated with 0.25-µm features, the chips will be able to operate with 3-1-1-1 burst timing. To achieve the faster 2-1-1-1 timing, a shrink to 0.22-µm features will have to be done, probably in late 1998.

One potential problem with SDRAMs when it comes to portable systems is that their power consumption is higher than the previous-generation memories that used the extended-data-out timing. To overcome that problem, designers at IBM are working on a low-power SDRAM that uses the clock enable line to help reduce standby and self-refresh currents by 50 to 75%, while not increasing active currents. The low-power 64-Mbit SDRAM thus achieves a standby or self-refresh current of just 0.5 mA (versus 2 mA for the standard SDRAM), while maintaining a page-miss or page-hit active current of 130 and 125 mA, respectively. However, the higher bus speeds of the PC-100 and still faster parts will increase the active currents. As a result, more attention must be paid in portable system design to minimizing bus activity in order to reduce the active power levels of the SDRAMs.

The Evolving SDRAMs

The biggest change coming to SDRAMs in the next 6 to 12 months, however, is the double-data-rate upgrade that allows the chips to deliver data twice as fast by using both rising and falling clock edges, much like the Rambus memories use both clock edges. The DDR technology is a capability that can be added to any device, thus there could be a family of DDR devices to meet different market needs. The higher data-transfer rates possible with DDR allow such memories to satisfy bandwidth requirements for high-end desktop PCs, high-performance graphics adapters, and workstation servers.

Internally, DDR memories are similar to standard SDRAMs, but employ, in the case of the Samsung bidirectional DDR SDRAM, four 512-kword by 32-bit internal memory banks, which feed into an output data buffer *(Fig. 4)*. Additional circuitry to handle strobe generation and timing synchronization (a strobe generator and a delay-locked



5. The SyncLink DRAM developed by the SyncLink Consortium employs a pipelined architecture with eight internal memory banks that can be concurrently accessed. A 72-bit word from the memory array is sent to the read latch and then serialized into four 18-bit subwords. The subwords are sequentially delivered to the host system over the 18-bit data bus.

loop) end up increasing the chip's area by about 4% over that of the standard-data-rate SDRAM.

Some key differences between single- and dual-data-rate devices include a reduced column-address-strobe latency, a reduced number of burst length choices, and the addition of a one-cycle write latency for the DDR chips. The DDR chips also will use differential rather than single-ended clocking; however, the DDR parts will give up the clock suspend and burst-read/single-bit write capabilities of single-data-rate devices. In terms of ac timing requirements to achieve a 200 Mbit/s data rate from the memory pins, that requires a clock cycle of 10 ns, an input setup time of 2 ns, an input hold time of 1 ns, a DQS to clock time of 1 ns, a data output to clock time of 1 ns, and a DQS to data output time of just 0.75 ns.

DDR memories actually will come in two variants—one that employs a unidirectional strobe, in which the Read Strobe signal is synchronous with the clock signal; and the other version employs a bidirectional strobe that does not have to be synchronous with the clock, but rather the data strobe signal is generated by the memory controller. The typical read and write timing for a unidirectional DDR memory uses the clock to latch control and address into the memory and a data strobe to latch data into the memory controller during the read cycle. During a write cycle, there is no data strobe and all signals and data are referenced to the clock.

Unidirectional parts, according to Bob Eminian, manager of DRAM marketing for Samsung, will require a few more pins since the chips will include the clock drivers. Clock and data lines on all DDR variants, though, will employ series-stub-terminated logic (SSTL) interfaces to handle the fast signal edge rates, while all other pins will have LV TTL interfaces.

In the bidirectional part, the DQS signal is generated by the memory controller and is not necessarily synchronous with the clock. That provides a larger valid-data window and will permit expandability on unbuffered DIMMs of up to 512 Mbytes for 64-bit-wide modules. On the negative side, the bidirectional DDR parts have a back-to-back read-write gap and are not well suited for implementation in a 4-bit-wide organization for deep memories. Use of external clocks also limits command-bus bandwidth.

Both implementations will deliver similar system performance, but some systems might gain a slight performance advantage with one versus the other, depending on the system architecture. Actually, explains Eminian, the market application may be the determining factor. In some application research Samsung did, they found that the PC market would probably favor the versions with the bidirectional DQS at the 64-Mbit level with either an 8- or 16-bit data width. Engineering-level samples of the 64-Mbit BDDR chips are now available from the company, with full production versions targeted for availability in mid-1998. Such parts would provide the simplest upgrade for existing SDRAMs and be ideal for the Socket 7 PC systems with the advanced graphics port. Such DDR chips would come in a 66-lead thin, small-outline package and be used on 168-contact DIMMs.

For graphics applications starting in about mid-1998, continues Eminian, a 32-bit 16-Mbit unidirectional part would provide the simplest upgrade from synchronous graphics DRAMs and would most likely be housed in 100-lead quad-sided flat packages. Such parts would operate at clock rates from 125 to 143 MHz. Finally, for the workstation/server type markets expected in 1999, designers are considering a bidirectional DQS version with no strobe that will come in capacities of 256 Mbits with either a 4- or 8-bit-wide data word and clock at 125 to 143 MHz. Such devices would carry no legacy-compatibility requirements and come in a new package to deal with the more stringent timing requirements.

One key issue as memory chips hit capacities of 64 Mbits and higher, is packaging. Designers at Rambus were the first to acknowledge the need for special packages to deal with high-speed memories and crafted unique vertical in-line packages that reduced lead lengths to a bare minimum. Today, chip-scale packaging and ball-grid array technology are being deployed, but the bulk of memory chips are still targeted to go into SO or QFP style packages.

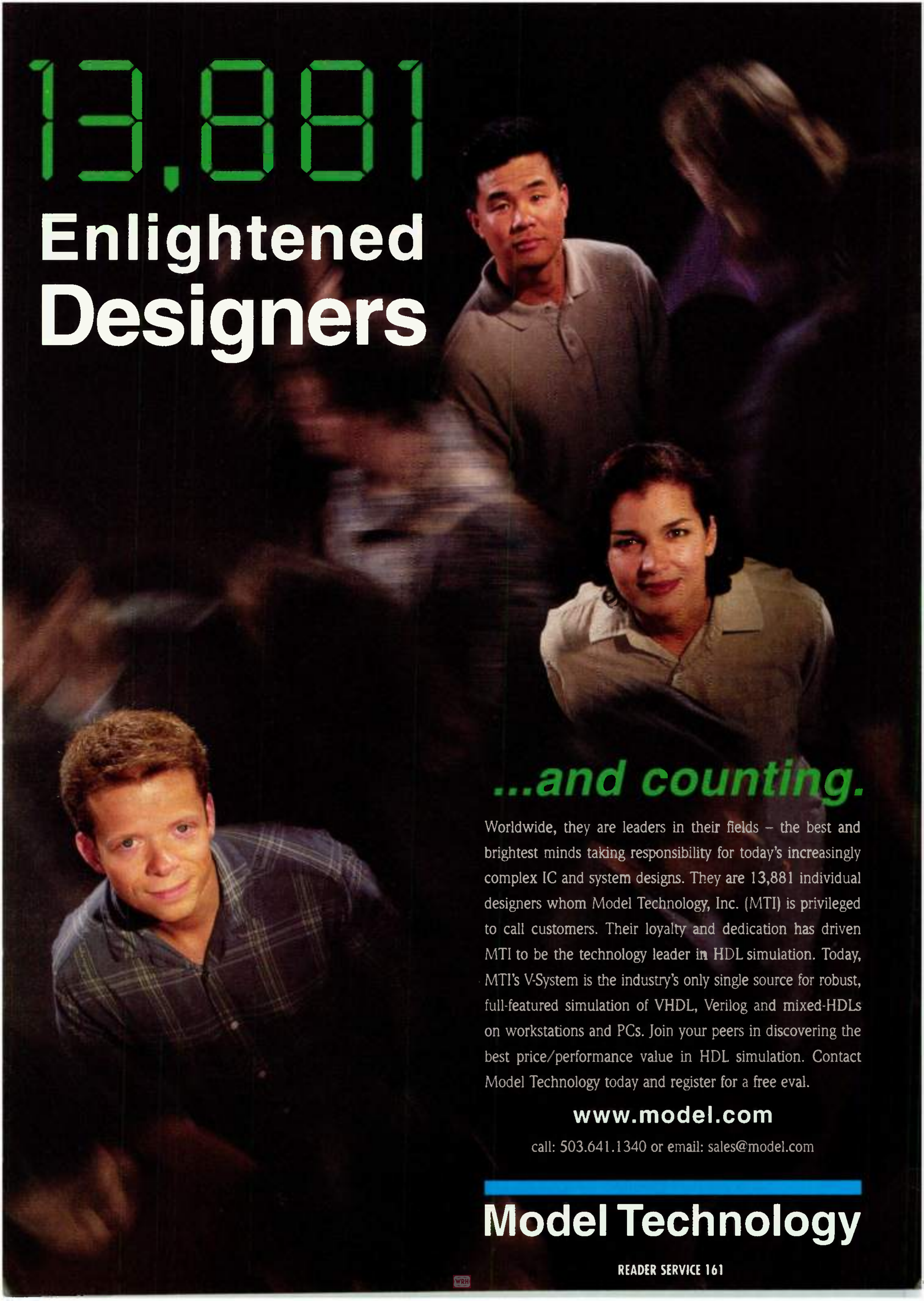
In the SO world, 500-mil-wide packages are most common, but in an uncommon move, Hitachi has made a commitment to offer all its forthcoming 256-Mbit devices in a 400-mil-wide package, saving about 47% of the memory board space as would have been required with traditional first-generation 500-mil packaged memories. That also should eliminate the need for a major module redesign when moving from the 500-mil 64-Mbit devices.

An alternative to that is a stacked memory approach that IBM and other companies are pursuing. Reminiscent of the early attempts in the 16-kbit DRAM era to solder two DIPs on top of each other to double the density, IBM is taking 16- and 64-Mbit EDO or SDRAMs housed in thin SO packages and stacking two or four of them on top of each other to form tiny memory modules that can be mounted on DIMM PC boards. This approach can produce modules four times denser than possible with single-layer devices, with little or no change in physical system layout. The stacked packages employ a pinout that is a superset of the JEDEC pinout, but the card pad connections remain the same. Separate row-address-strobe signals or a chip-select per deck are needed for independent deck operation. There's also a slight increase in power over a single-device stack because when one chip is active, the other devices are in standby and still drawing a small amount of current.

The SyncLink Approach

The SLDRAM has been gaining a lot of momentum in the last 12 months and the rejuvenated SDRAM Consortium has not only finished the definition for what the first chip will be, but also has funded the creation of the first 64-Mbit implementation. The consortium's chair, Farhad Tabrizi of Hyundai, describes the chip specification as an open standard that will allow multiple companies to implement devices to achieve an 800-Mbyte/s bandwidth (400 Mtransfers/s) thanks to an 18-bit I/O port (16 bits of data and two bits for ECC). Intended for use in systems with 64-bit data words, the extra bits provide an 8-bit ECC check word when four chips are used in parallel.

The high-speed operation of the chip requires much attention to be paid to packaging. To that end, the chip will be offered in both a 64-lead vertical surface-mount package that allows high-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density memory arrays to be constructed, and in an 80-lead TSOP. Initially expected to be implemented with a 0.25-µm process at Siemens, the chip will operate at 2.5 V. Full details of the SLDRAM target specification are available on the Consortium's web site: *http://www.sldram.com.*

So, what exactly is an SLDRAM? Well, for starters, it looks very similar to an SDRAM, but packs eight internal memory banks, a clocked synchronous interface that is terminated with small-swing signaling, and employs a programmable data burst transfer protocol *(Fig. 5)*. These changes from the SDRAM approach decouple the internal DRAM address and control paths from the data interface, allowing the memory to achieve higher bandwidth data transfers. Like DDR SDRAMs, SLDRAMs will use both rising and falling clock edges to transfer data, and a return clock signal to help improve timing margins.

Internally, an SLDRAM consists of a memory array organized as eight banks, each structured as 128 kwords by 72 bits, and each 72-bit word is transferred over the 18-bit I/O interface in a burst of four 18-bit words. All transactions begin with a request packet, with read and write request packets containing the specific command and address information required. Read and write data are transferred in packets, with a single-column access involving the transfer of a single data packet (a burst of four 18-bit words). Data from either one or two columns in a page may be accessed with a single request packet, with a two-column request resulting in a continuous burst of eight 18-bit data words.

Prior to normal operation the SLDRAM must be initialized, with various internal registers and timing delays set up for proper system operation. Functions such as power-up/hardware reset, exit shutdown, controller driver adjust, command and write-timing synchronization, and ID assignment are just some of the setups that must be done. A SyncLink memory chip may have multiple subRAMs or blocks, and except for initialization, which is at least partly a node (device) function, the blocks act essentially like independent RAMs and each handles one request at a time.

The memory chips are connected by commands and data links—the controller drives the command link to send Read, Write, Load, Store and Event commands to the memories. The datalink is driven by an SLDRAM and received by the controller in the case of Read and Load transactions, or driven by the controller and received by an SLDRAM in the case of Write transactions. In a typical SLDRAM system topology, the host controller provides a 10-bit command link bus, a two-byte datalink bus, and Select, LinkOn, and other control/clock signals, which connect to an array of SLDRAM that shares common command and data buses. A daisy-chained serial bus (serial in and serial out on each chip) is used during power-up to synchronize the SLDRAMs and assign unique IDs to each.

One other novel memory type is available to provide higher memory system bandwidth—the multibank MoSys DRAM, which provides a high-bandwidth 16-bit interface that can transfer data at up to 666 Mbytes/s when clocked at 166 MHz. Internally, MDRAMs use 32 banks per megabyte. That will permit the chips to handle many overlapping transactions, thus maximizing the data bandwidth, and that results in a data bandwidth very close to the peak bandwidth. The bank switching approach also keeps the data latency very low.

The one main limitation of MDRAMs is that they require short buses and that, in turn, limits the number of memory chips to just four. Current density levels of the parts range from 0.5 to 2 Mbytes per chip, and even higher densities are on the drawing boards. Thus, although for limited memory applications the MDRAMs can serve as main memory, they would appear to be better suited for high-speed buffers and graphics applications.

References:

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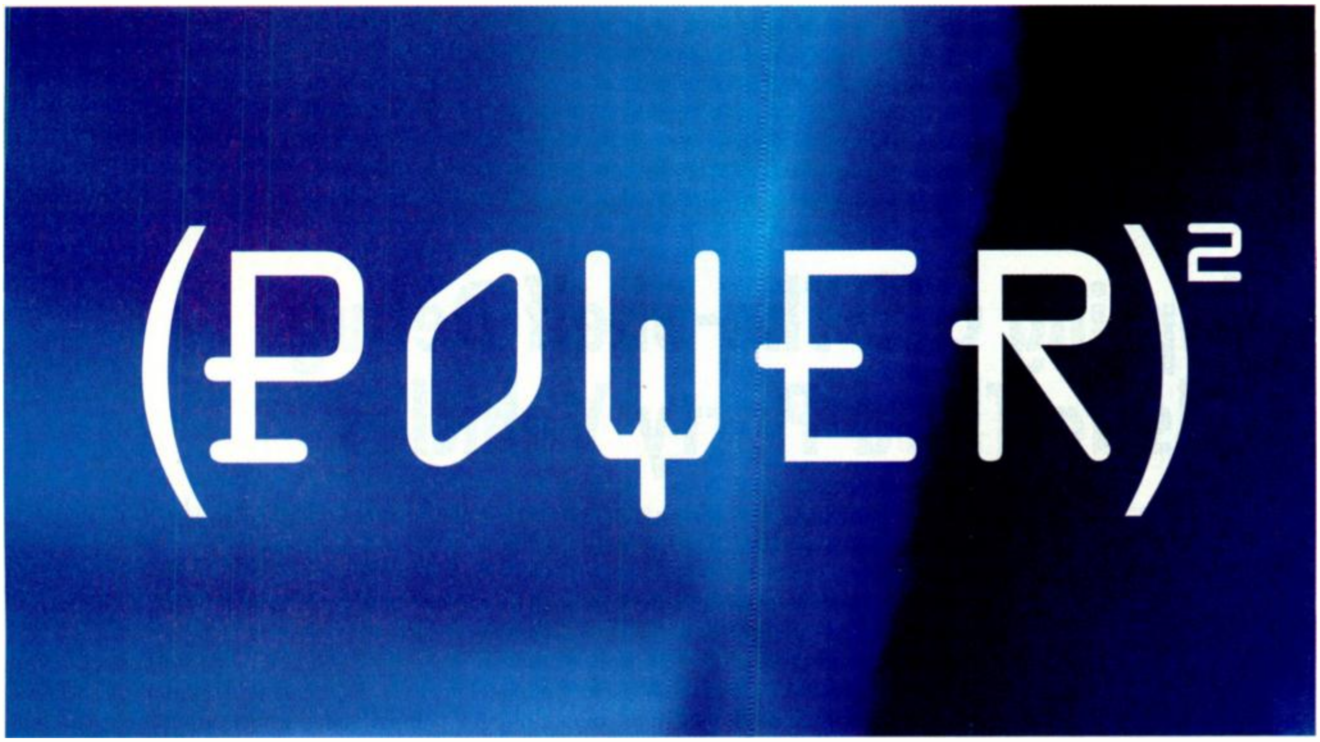
S. Przybylski, *New DRAM Technologies: A Comprehensive Analysis Of The New Architectures*, MicroDesign Resources, 1996

How Valuable	Circle
Highly	544
Moderately	545
Slightly	546



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Adapting Off-The-Shelf Debug Tools To Third-Party Vehicles

A Modular Approach Can Help Developers Adapt Their Favorite Tools To New Combinations Of Processors, OS Environments, And Target Interfaces.

DOUG SALOT, Microtec Corp., 880 Ridder Park Drive, San Jose, CA 95131 (408) 487-7000; e-mail: salot@microtec.com.

Embedded software development tool vendors increasingly need to support a variety of host platforms, development languages, target platforms, and hardware and software systems that sit between the host and the target. These include simulators, in-circuit emulators, real-time kernels, ROM monitors, ROM emulators, and BDM connections. However, it is virtually impossible for one tool vendor to cover all of the possible combinations the market demands. As a result, tool vendors have begun developing tools that can be extended by third parties through published interfaces.

In fact, some software development tool vendors have attempted to simplify tool adaptation efforts to the cookbook level. This has reduced the cost of tool adaptation and enabled third parties to modify off-the-shelf tools in ways that wouldn't otherwise be possible. This article will explore one dimension of customization for one class of tool: the debugger. There are similar adaptation strategies to re-target debuggers to new target processors, new development languages, and new executable and debug file formats, and for other classes of tools such as compilers and profilers.

Debugger Adaptation

One of the most common tool adaptation efforts today involves porting a debugger for an existing processor to a new debug *vehicle*. A vehicle can be loosely defined as the mechanism a debugger uses to control target execution and to access state information on the target. It might be composed of several component layers *(Fig. 1)*. Examples of debug vehicles include:

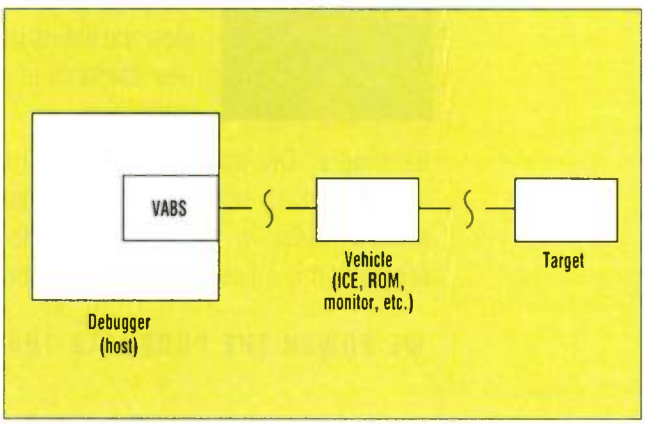
- An in-circuit emulator (ICE) connected to a target board;
- An instruction-level simulator;
- A real-time kernel with some sort of debug service running on the target;
- A native UNIX operating system (OS) with a ptrace interface; and
- A ROM monitor on a target board with no OS.

A debugger designed to work with only one type of vehicle, such as an ICE from a single vendor, might have hard-coded knowledge about the feature set of that vehicle and the communication protocol used to send commands and get results. If the developer asks such a debugger to read a target memory location when the target is controlled by an ICE, the request might take the following path.

The developer first asks for memory using the debugger graphical-user interface (GUI) or command-level interface. The debugger then translates the request into a command packet that the ICE will understand. The packet is next sent to the ICE via some specific communication protocol, such as TCP/IP, over a specific communication channel, such as Ethernet. Firmware on the ICE decodes the packet, interprets the request, and translates the request into the bus signals needed to read the memory location.

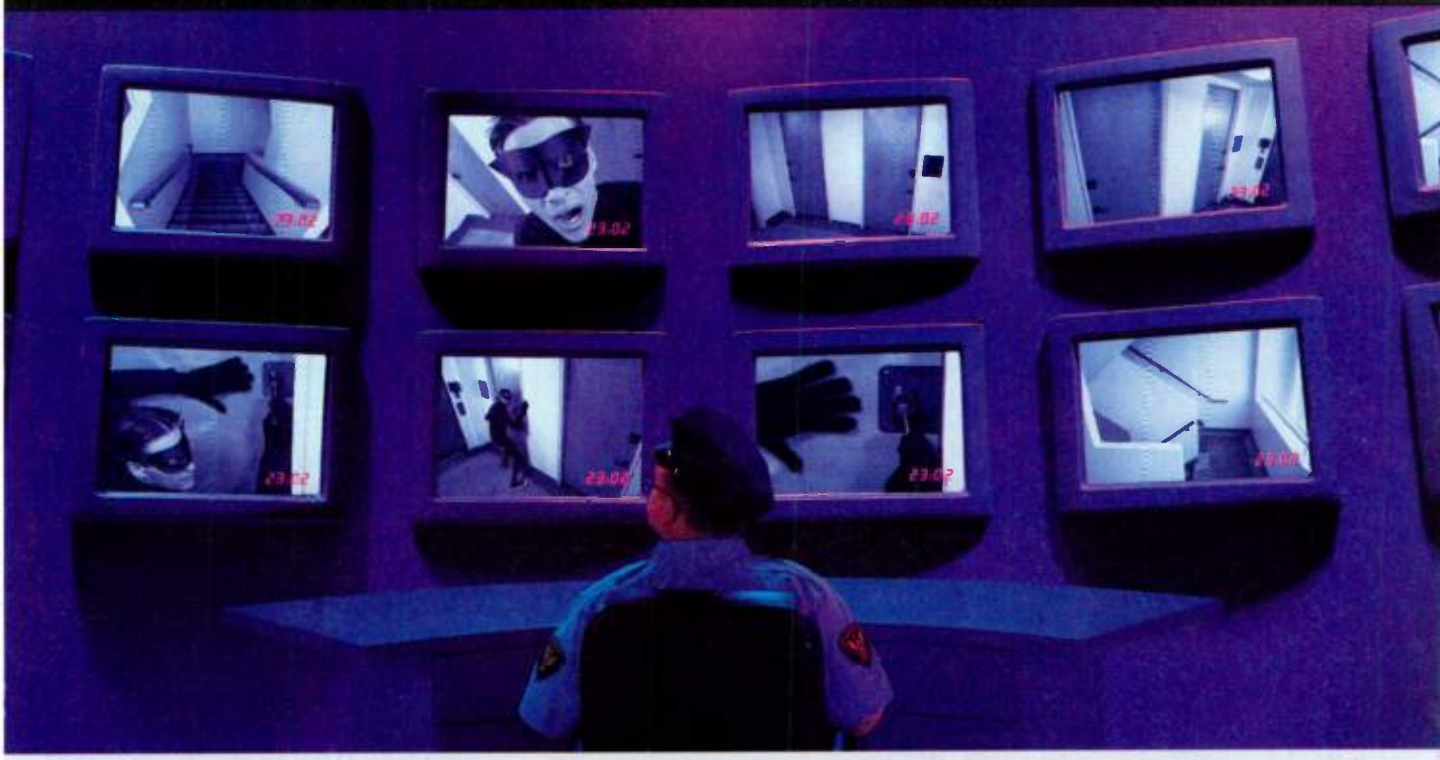
Adapting this type of debugger to a new vehicle, such as a real-time kernel debug server, would require major surgery. Among the needed changes would be:

- Dropping support for features no longer supported, such as hardware-assisted breakpoints and trace collection;
- Adding support for new features such as task-qualified breakpoints and kernel re-



1. A vehicle abstraction (VABS) is a software module that plugs into a host-based debugger to adapt the functionality of the debugger to the specifics of a given "vehicle" that interacts with the target system. Vehicles can include in-circuit emulators, ROM monitors, instruction set simulators, and so on. The VABS communicates with the debugger via a published application programming interface.

Imagine Being Able To Look At A Digital Design Problem This Way.



This view of system behavior was provided by the HP 16500C logic analysis system and the HP 16505A prototype analyzer.

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Sample VABS Data Structure

The example below is an actual VABS data structure that was taken from Microtec's XRAY debugger.

```
VABS vabs_def =
{                                  /* VABS definition structure */
 1, 1,                             /* VABS version 1.1 */
 VABSTYP_MON,                      /* this is a monitor type */
 False,                   /* ow one-time init */
 "1.0",                   /* our driver version 1.0 */
 "VABS version 1.1",
 "SPA",                   /* license name */
 NULL,
 "EXAMPLE",                        /* product name */
 "Example VABS",                   /* init message */
 VCONF_FLUSHREGS                   /* flush registers */
 | VCONF_ATTACH_THREAD,            /* attach threads */
 0,                                /* no memop config flags */
 0,                                /* no execution config flags */
 VCONFB_THRD_SPECIFIC,             /* one break entry per thread breakpoint */
 VCONFL_UNLOAD,                    /* unload done in the VABS */
 1024,                    /* size of optimal read/write */
 1024,                    /* max size of read/writes */
 0, 0,                             /* fill and search not built-in */
 0,                                /* no run_until supported yet */
 3,
 (void *)spa_bi_cmds,              /* built-in commands */
 "EXAMPLE RTOS",                   /* system name */
 MODEL_TASK,              /* we support pure thread model */
 0,                                /* pad */
 CMDDIS_RESTART,                   /* disabled commands */
 CMDDIS_MT1(MTCMD_ARGS),
 CMDDIS_NONE,
 spa_mtcmds,              /* GUI commands we replace */
 &spa_brkexts,            /* breakpoint support customizations */
 NULL,                    /* TABS filled in dynamically */
 0,                                /* size of private data per board */
 0,                                /* size of private data per process */
 sizeof(SPA_THREAD_PRIV),          /* size of private data per thread */
 0,                                /* error table size */
 NULL,                    /* error table */
 &spa_settings,           /* replacement strings, etc */
 0, 0, 0, 0, 0, 0, 0, 0,  /* byte padding */
 0, 0, 0, 0,              /* word padding */
 0, 0, 0, 0,                       /* long padding */
 VabsInit,                         /* our init routine */
 VabsConnect,             /* our connection function */
 VabsDisConnect,          /* our disconnect function */
 VabsConnectProc,                  /* callback from a connection */

 NULL,                    /* we don't handle the msg loop */
 NULL,                    /* we don't handle the msg loop */
 VabsSocketHandle,                 /* callback when message received on
                                      our port */
 VabsSpawn,                        /* download object to target */
 VabsMem,                          /* our routine to read/write memory */
```

(continued on page 94)

source browsing;
- Changing the way debugger commands are converted into packets;
- Changing the communication protocol; and
- Changing the communication device driver.

After doing things the hard way for many years, debugger vendors discovered they could write the basic core of the debugger once and adapt the personality of the debugger to various vehicles through plug-in modules that conformed to well-defined interfaces. As these interfaces matured, they were published and made available to third parties. It is now possible for third parties—such as a kernel vendor, ICE manufacturer, or even an end-user—to adapt sophisticated debugging tools to their specific vehicles or run-time environments.

In this article, a plug-in debugger personality module for vehicle adaptation is called a "vehicle abstraction" or VABS.

The salient features of a VABS are:

- The module is packaged a certain way and conforms either to a well-defined binary interface (sometimes called an ABI) or to some sort of loosely coupled interface protocol such as RPC, CORBA or DCOM.
- The module uses mechanisms provided by the debugger to enable, disable, extend, replace, and modify debugger features as appropriate.
- The module translates debugger requests into vehicle-specific requests.
- The module translates vehicle events into debugger events.
- The module needs a mechanism to request debugger services.

A tool vendor might recognize that there are layers with finer granularity than the vehicle itself that can be reused among different vehicles, such as a communication protocol layer and a communication device layer. This article ignores these lower layers and assumes that the entire VABS is monolithic. Most of the concepts in this article will apply to any reconfigurable debugger from any tool vendor.

Packaging—There are three basic considerations that determine how a VABS should be packaged:

1) the speed across the interface;

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Sample VABS Data Structure

(continued from page 92)

```
NULL,               /* no memory access functions */
NULL,               /* no memory config functions */
NULL,               /* no memory mapping functions */
VabsRegs,                  /* register access */
NULL,               /* no thread state information provided */
VabsExec,                  /* Execution control */
NULL,               /* no restart capability */
VabsStop,                  /* halt execution of tasks */
VabsControl,               /* task control */
NULL,               /* no reset functionality yet */
NULL,               /* no shared library handling */
VabsBreakPoint,     /* breakpoint control */
NULL,               /* no commands uploaded from target */
NULL,               /* no remote instances */
NULL,               /* no remote commands */
VabsRemoteList,     /* access remote lists */
NULL,               /* no private data routine */
VabsErrorString,           /* error messages */
};                         /* end of VABS def */
```

The vabs_def symbol is exported by the DLL, and this symbol is looked up when the debugger loads the DLL. All communication with the VABS goes through this data structure.

2) the implementation language and run-time issues; and

3) host OS support for the package architecture.

Interface speed—Interface speed will directly influence the debugger's performance. That speed is a function of the type of parameter packing and unpacking required and the communication channel used between the debugger and the VABS module. In general, modules that can be mapped to the same process space as the debugger will always have better interface performance than those that live in a separate process or on a separate machine.

There are advantages to isolating a module in its own process space and using interprocess communication between the debugger and the VABS module, but we'll choose the intraprocess model for speed. Since the module will be running in the same process on the same machine as the debugger, we can ignore parameter marshaling issues such as endianity and alignment. We also can safely assume that the connection between debugger and module is a reliable one, so no error-checking protocol is required.

Language and run time—The ideal interface is language-independent, but languages such as C++ have very specific calling conventions and name-binding rules that make it difficult to map to other languages. However, C++ has several desirable properties as an interface language. Using the "this" pointer to act as an instance handler lets you create multiple instances of an interface. An interface can be purely *abstract* or it can include default implementations, and default implementations can be overridden

You can preserve these desirable properties without being bound to the naming and calling conventions of C++ by designing a C-level interface using an instance handle that points to a data structure containing function vectors *(Fig. 2)*.

Another run-time issue that can affect the design of our system is the threading model. Multithreading has certain advantages, such as the ability to support multiple vehicles simultaneously without worrying that any single vehicle might seriously degrade the performance of the system as a whole. To simplify things, however, assume a single-threaded model for this article.

Host support—Since we've chosen an in-process communication model, we can ignore all of the inter-process communication models offered by various operating systems. We simply need a way to find and load the third-party module.

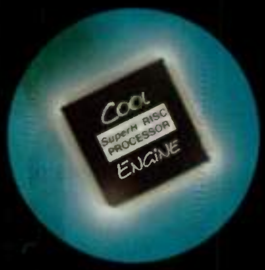
Virtually all host operating systems support dynamically loadable libraries (DLLs), so we'll choose the DLL as our module package. Different hosts have different approaches to binding a DLL to an executable at run time, but we can safely ignore most of these differences by making some simplifying assumptions. First, assume that the debugger will only refer to a single name within the DLL: the name of the data structure that contains the VABS instance data and method vectors. Second, the VABS DLL must not directly call any functions in the debugger executable. As part of the module initialization sequence, we'll pass in a handle to a vector table of debugger functions we wish to export to the module.

These assumptions mean that we will directly load the VABS DLL from the debugger rather than have the OS load it based on some late name-binding scheme. Once loaded, we only need the address of a single data structure that contains everything else we need to know about the vehicle.

Configuration—In addition to a functional interface, the VABS data structure must also tell us how to tailor debugger functionality to match the functionality of the vehicle. One thing the debugger must know is the process model supported by the vehicle and the target run-time environment. This tells the debugger how to present snapshots of the run-time environment to the user, and how execution control and state access need to be qualified.

Process models include:

- A single-process model, for run-time environments in which single application owns all target resources;
- A single-process model with multiple tasks, in which a one application can spawn multiple tasks, each with its own register contexts;
- A multiple-process model, such as a traditional Unix OS;
- A multiple-thread model, for run-time environments that can be viewed as a



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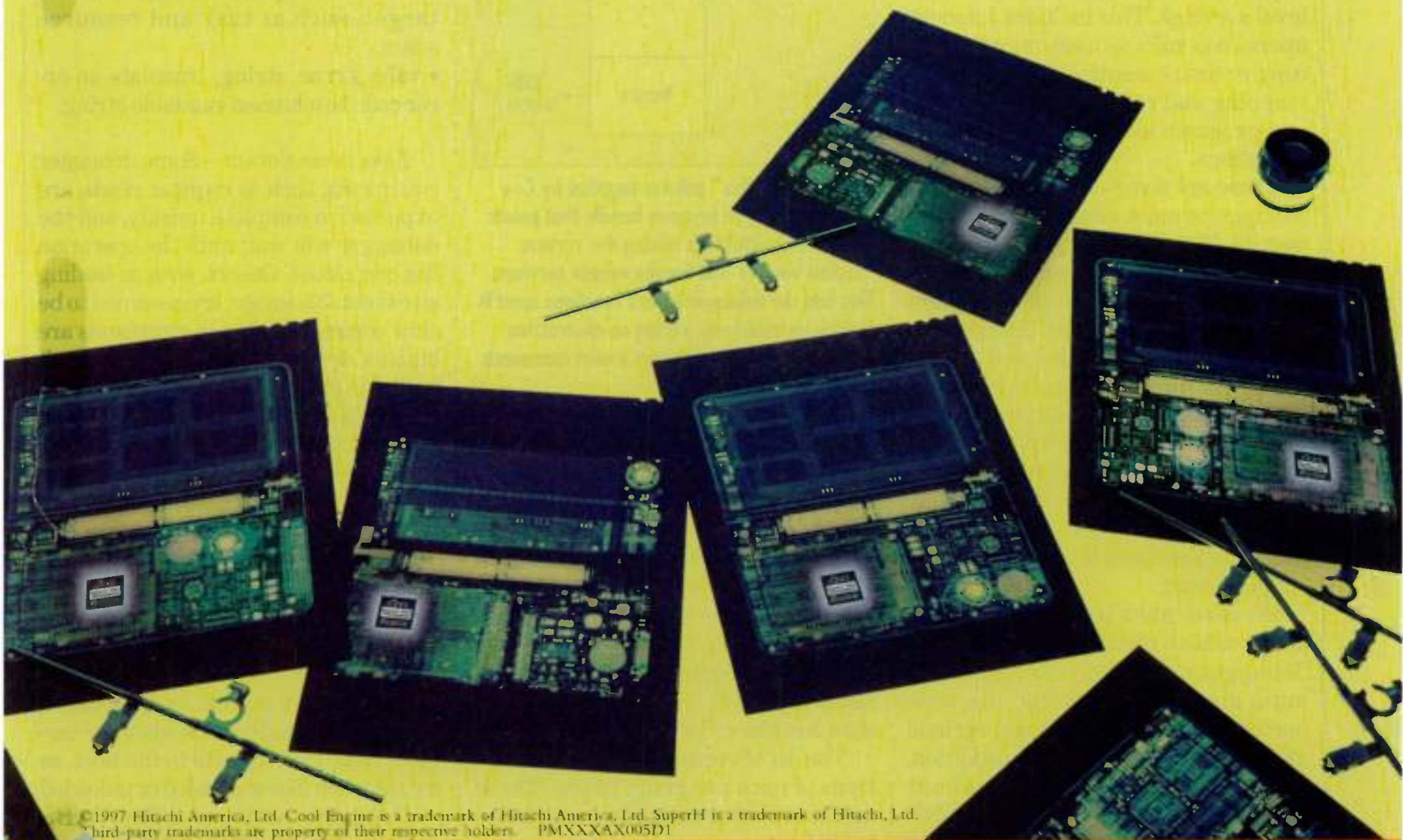

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collection of independent threads; and
• A multiple-process model with multiple threads, in which there is a parent/child relationship between processes and threads.

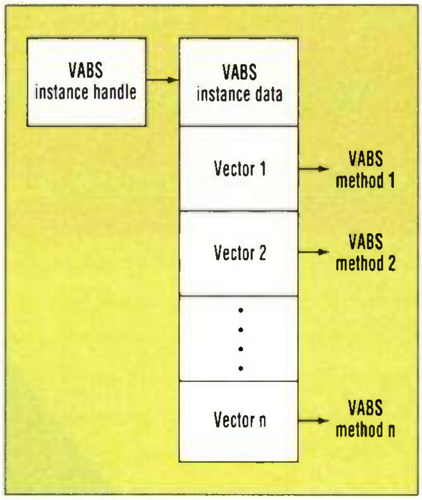
The debugger also must know which operations the vehicle directly supports. Those that aren't supported will be subsumed by built-in debugger implementations that rely on lower-level services. This includes memory operations such as memory compare, copy, or test; execution operations like stepping and running to an address; and program loading and unloading operations.

There are some commands that the debugger cannot subsume if not supported. Target-oriented commands connecting and disconnecting a selected board from a list of boards are sometimes unsupported. Setting current threads or processes and attaching/detaching to/from threads or processes may not be within the capabilities of vehicles like ROM monitors, as may be resetting a board or restarting a process. These commands simply need to be disabled at the debugger user-interface level if the vehicle can't support them.

We also must tell the debugger about vehicle metrics that may affect debugger operation, like the maximum number of breakpoints supported and the maximum and optimal memory access block size. In addition, the debugger needs to know about memory access alignment or word-size limitations and the relative cost of various operations.

As the final step in vehicle configuration, we must tell the debugger about new commands specific to our vehicle. The debugger needs enough information to parse these commands, dispatch them, display on-line help, and perhaps bring up GUI elements for the new commands.

Command translation—Once the VABS module has been loaded and initialized and the VABS configuration data has been read, the VABS will begin receiving requests from the debugger. The VABS is solely responsible for translating these requests into messages that the underlying vehicle can understand and passing the results of those requests back to the debugger.



2. Using the "this" pointer supplied by C++ lets you create an instance handle that points to a data structure containing the various function vectors that invoke vehicle services. This lets the debugger access functions specific to a given vehicle by placing an abstraction layer between the debugger's own commands and those of the vehicle.

In some cases, the VABS will handle the request locally without communicating to the vehicle. VABS requests are made through the VABS method vectors in the VABS data structure. Each vector needs to be filled in with the address of a function that will handle the request, or with NULL to indicate that the request is not supported *(see "Sample VABS data structure," p. XX)*.

The list of vectors and brief descriptions of each are given below. Those methods that are required are shown in bold.

• **vabs_init**, initialize the VABS;
• vabs_connect, connect to a board;
• vabs_connect_proc, connect to a process;
• vabs_disconnect, disconnect from a board;
• vabs_object_load, download an executable image to the target;
• **vabs_mem_access**, read and write target memory;
• vabs_mem_ops, fill, search, test, copy and compare memory;
• vabs_mem_config, set memory map configuration;
• vabs_mem_map, get memory map configuration;
• **vabs_register**, read and write target registers;
• **vabs_thread_state**, get the current execution state;
• **vabs_execute**, control execution;
• vabs_restart, restart a process or thread;
• vabs_stop, halt execution;
• vabs_process_control, attach, detach, suspend, resume, stop, and kill threads and processes;
• vabs_reset, reset a board;
• **vabs_breakpoint**, control breakpoints;
• vabs_remote_list, access lists on the target, such as task and resource state;
• vabs_error_string, translate an error code to a human-readable string.

Event translation—Some debugger commands, such as register reads, are expected to complete quickly, and the debugger will wait until the operation has completed. Others, such as loading an executable image, are assumed to be slow commands. These commands are initiated by the debugger, but it doesn't wait for the command to complete. Command completion is signaled by an asynchronous event.

It is the VABS' responsibility to detect when the vehicle has completed a request and to generate a debugger event in response to that completion. Examples of such supported events might include the creation or termination of a process, or the starting or stopping of a process or thread. The debugger also must be informed when a breakpoint is modified, or when the target makes I/O requests to the host, as well as when files are loaded or unloaded

Debugger services—The VABS sometimes needs help from the debugger to complete commands. A [illegible] of debugger services must be exp[illegible] the VABS and, for reasons des[illegible] earlier, we'll use a data structure [illegible] contains function vectors for each [illegible]vice, similar to the VABS data structure. A pointer to this structure is passed to the VABS at initialization time. Services similar to the following might be exposed:

• HostProcessExpression (evaluate an expression and return the res[illegible]
• HostSendError (send an er[illegible] warning message to the user);
• HostStatusLine (update sta[illegible]formation);
• HostReceiveEvent (notify [illegible] debugger of an event);
• HostLoadFile (ask the debu[illegible]

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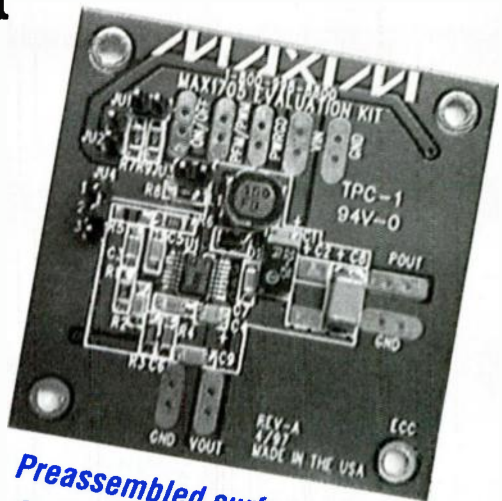
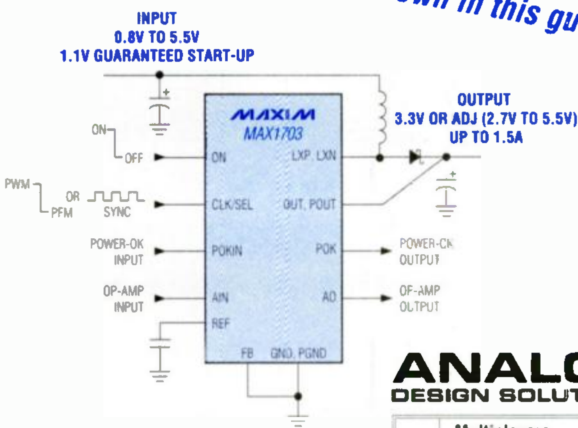


Preassembled surface-mount evaluation kits are available for most circuits shown in this guide.



PART NUMBER	SWITCH SIZE (A)	CURRENT OUTPUT (mA)		PACKAGE	ADDITIONAL FEATURES
		3.6VIN, 5VOUT	1.2VIN, 3.3VOUT		
MAX1703*	2	1500	500	16-pin narrow SO	Highest current
MAX1700*	1	1000	300	16-pin QSOP	Simplest device
MAX1701*	1	1000	300	16-pin QSOP	Includes battery monitor and linear-regulator controller
MAX1705	1	1000	300	16-pin QSOP	Includes 200mA linear regulator
MAX849	1	1000	300	16-pin narrow SO	Includes A/D converter
MAX1706	0.5	300	110	16-pin QSOP	Includes 200mA linear regulator
MAX848	0.5	300	110	16-pin narrow SO	Includes A/D converter

*Future product—contact factory for availability

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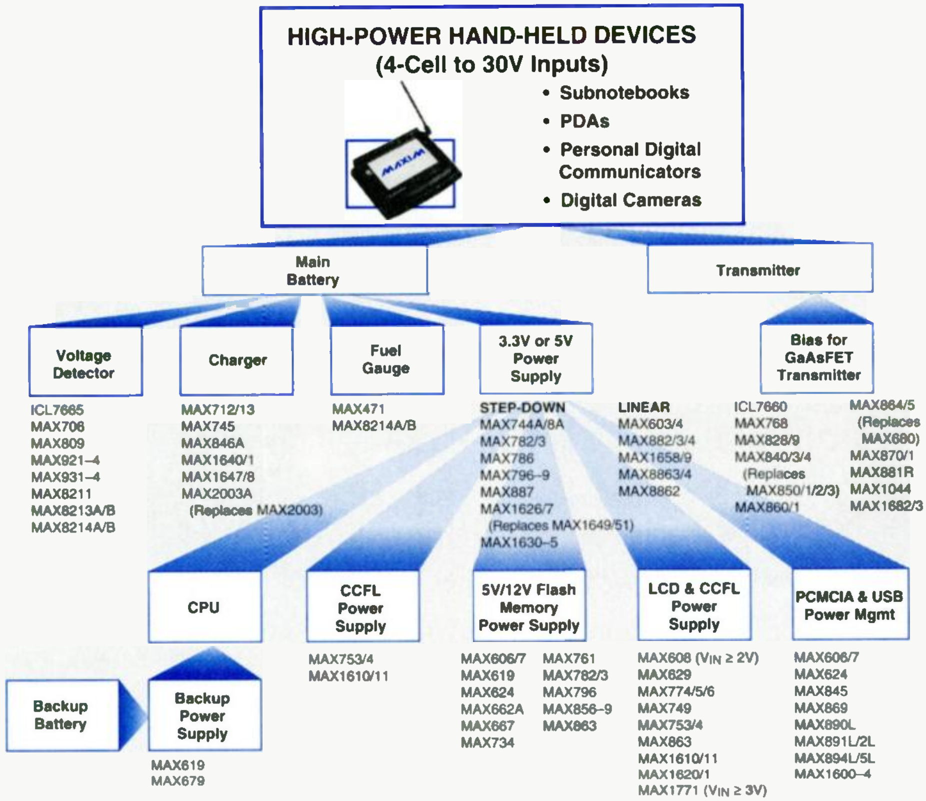
MAXIM



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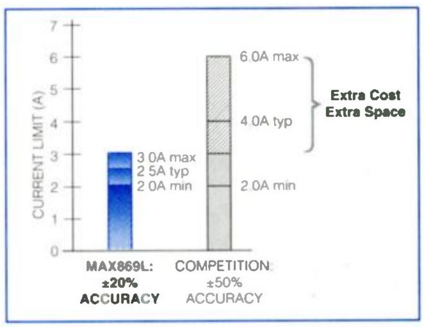
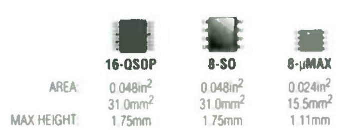
MAX890L Family:

- Protects System Supply Against Glitches from Shorts and Surges
- Universal Serial Bus (USB) Compatible
- FAULT Output Signal
- 20%-Accurate, User-Set Current Limit
- Up to 2.5A Current Limits (MAX869L)
- 2.7V to 5.5V Input Range
- Small μMAX Packages (MAX891L/MAX892L)
- 13μA Supply Current
- 0.1μA Shutdown
- Thermal-Overload and Short-Circuit Protection





PART NUMBER	RON @ 4.5V (mΩ)	RON @ 3V (mΩ)	MAXIMUM CURRENT (A)	COUNT	PACKAGE
MAX869L	38	45	2.50	Single	16-QSOP
MAX890L	75	90	1.25	Single	8-SO
MAX891L	120	150	0.63	Single	8-μMAX
MAX892L	250	300	0.31	Single	8-μMAX
MAX894L	120	150	0.63	Dual	8-SO
MAX895L	250	300	0.31	Dual	8-SO

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- Palmtops
- Medical Meters
- Remote Controls
- Pagers

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MAX606/7
MAX662A
MAX761

12V, 60mA–120mA
MAX606/7
MAX717–721
MAX734
MAX761

5V
MAX606/7
MAX619
MAX756/7
MAX856–9

DUAL 5V & 12V
MAX624
MAX863

LCD Power Supply

POSITIVE
MAX608 ($V_{IN} \geq 2V$)
MAX863 (dual output)
MAX1771 ($V_{IN} \geq 3V$)

NEGATIVE
MAX722/3
MAX735
MAX749
MAX774/5/6

DOUBLING OR INVERTING CHARGE PUMPS
ICL7660
MAX828/9
MAX860/1
MAX864/5
MAX868
MAX870/1
MAX1044
MAX1680/1
MAX1682/3

Voltage Detector

ICL7665
MAX706
MAX809
MAX921–4
MAX931–4
MAX8211/12
MAX8213A/B
MAX8214A/B

3.3V or 5V Power Supply (for CPU)

STEP-UP
MAX606/7
MAX619
MAX679
MAX722/3
MAX731
MAX751
MAX756/7
MAX797/8
MAX848/9
MAX856–9
MAX863
MAX1642/3
(Replaces MAX866/7)
MAX1700/1
MAX1703
MAX1705/6
MAX1771

DUAL 5V & 12V
MAX863

STEP-UP/DOWN
MAX710/11
MAX761/2
MAX1672
MAX1771

STEP-DOWN
MAX639/40/53
MAX797/8
MAX887
MAX1626/7
(Replaces MAX1649/51)

LINEAR REGULATORS
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MAX667
MAX882/3/4
MAX1658/9
MAX8862
MAX8863/4
MAX8865/6

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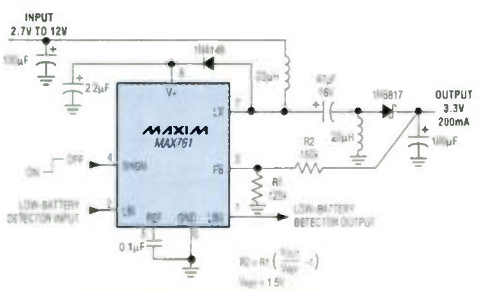
Compact Step-Up/Down DC-DC Converters for Li-Ion and 4-Cell Battery Stacks

Step Up/Down 4 Cells to 5V with 85% Efficiency

Input: 2.7V to 12V
Output: Adj. (1.5V to 6V)
Up to 200mA

MAX761

- Step-Up/Down Without Transformer
- 85% Typical Efficiency
- 100µA (max) Quiescent Supply Current
- 5µA (max) Shutdown
- No Leakage Through Diode in Shutdown
- For 500mA Applications, Refer to the MAX1771 Controller

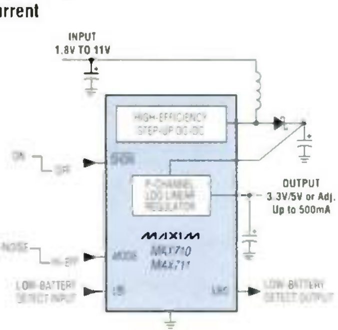


NEW Step-Up/Down Converter Makes $5V_{OUT}$ from 1.8V to 11V Input

Input: 1.8V to 11V
Output: 3.3V or 5V at up to 500mA
Adj. (2.7V to 5V)

MAX710/MAX711

- Step Up/Down Without Transformer, Single Inductor
- Boost DC-DC Followed by Linear Regulator
- Very Small Inductor
- Output Fully Off in 0.2µA Shutdown
- Low-Noise or High-Efficiency Setting
- 100µA Quiescent Supply Current
- Linear Regulator Filters Output Ripple
- MAX710EVKIT
- For a 250mA part in a smaller package, refer to the MAX1672 (available 10/97)



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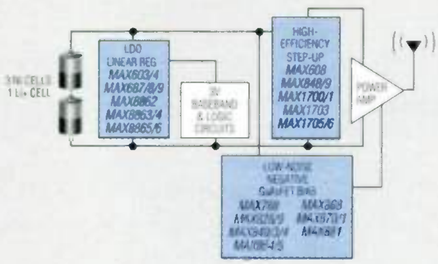

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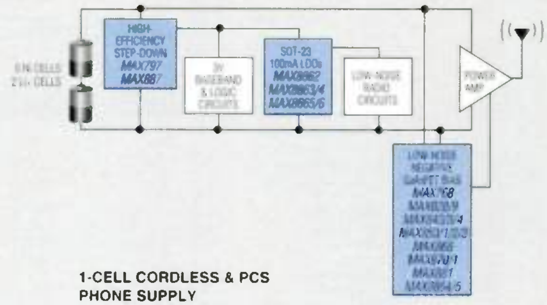

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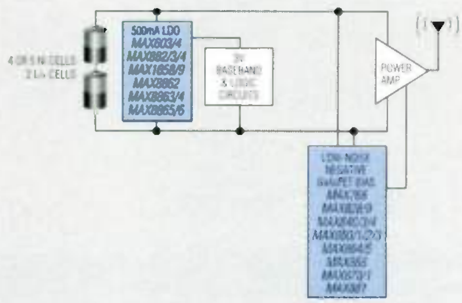
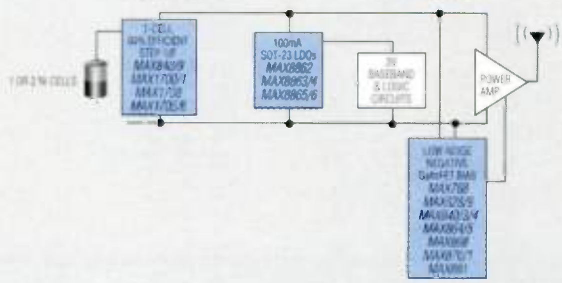


1-CELL CORDLESS & PCS PHONE SUPPLY



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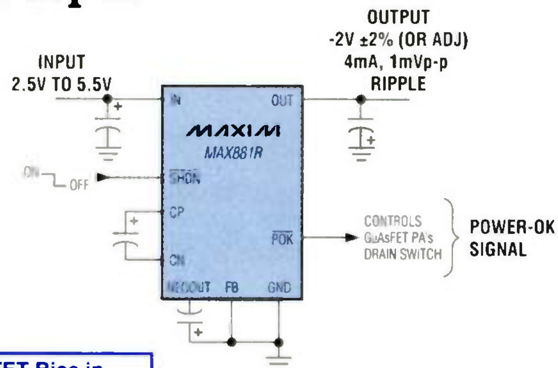
NEW Smallest Complete Bias Supply for GaAsFET Power Amps Now Fits in Small µMAX Package and Includes Power-OK Output

MAX881R (Available 12/97)

- Small, Thin µMAX Package:
  - 1/2 Size of 8-Pin SO
  - 1.11mm Max Height
- Uses Only 0.22µF Capacitors
- Power-OK Signal Controls Drain Switch to GaAsFET Power Amplifier
- 1mVp-p Low-Noise Output Ripple
- 1µA Logic-Controlled Shutdown
- 1ms Guaranteed Start-Up
- 2.5V to 5.5V Input
- -0.5V to $-V_{IN}$ Output
- MAX881EVKIT Available
- See also: MAX840–MAX844 (available now)



Complete GaAsFET Bias in 1/2 the Size

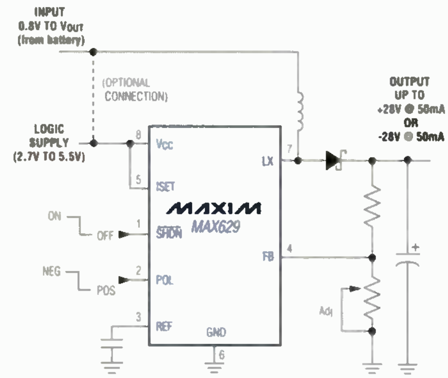
	MAX843	MAX881R
	8-SO	10-µMAX
AREA	0.048in² 31.0mm²	0.024in² 15.5mm²
MAX HEIGHT	1.75mm	1.11mm

High-Efficiency Positive and Negative Supplies for LCDs and Biases

NEW 8-Pin Device Has Built-In 28V Switch for Positive or Negative LCD Supplies

Input: 0.8V to 28V
Output: Up to +28V (or -28V)
Up to 150mA

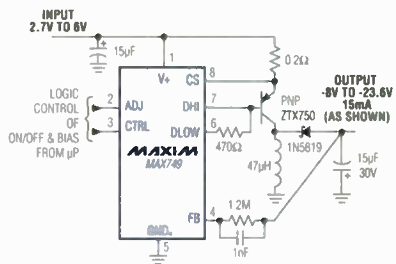
MAX629
- 8-Pin SO Package
- Internal 28V, 500mA N-Channel Switch
- Up to +28V or -28V Output
- 80µA Quiescent Supply Current
- 1µA (max) Shutdown Current
- Up to 300kHz Switching for Small Components
- Adjustable Current Limit for Small Inductors
- MAX629EVKIT



-24V Negative LCD Bias Has Digital Voltage Control

Input: 2.7V to 6V
Output: Unlimited Negative Voltage
Up to 2.5W

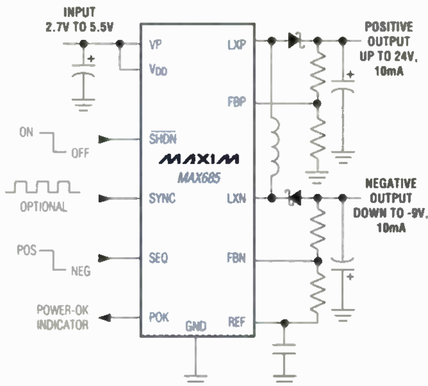
MAX749
- 8-Pin SO Package
- Digital Adjust Range: 1/3 to Full-Scale in 64 Steps
- Single Resistor Sets Full-Scale VOUT
- 60µA (max) Quiescent Supply Current
- 15µA (max) Shutdown
- MAX749EVKIT-SO
- See also: MAX1620/MAX1621 (positive outputs)



Low-Noise Dual-Output (Pos & Neg) Supply for CCDs and LCDs Uses Only One Inductor

Input: 2.7V to 5.5V
Output: Up to +45V and -16V
10mA Each Output

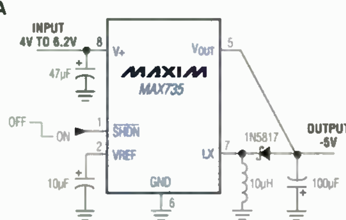
MAX685 (Available 12/97)
- Dual Output Using Single Inductor
- Low-Noise, 40mVp-p Output Ripple
- 220kHz/400kHz Fixed-Frequency PWM Operation
- Internal Switches
- Small 16-Pin QSOP Package (same size as 8-pin SO)
- Power-OK Indicator
- Power-On Sequencing Select
- 0.1µA Logic-Controlled Shutdown
- MAX685EVKIT



Compact, Low-Noise Negative Supply Delivers 250mA with 77% Efficiency

Input: 4V to 6.2V
Output: -5V
Up to 250mA

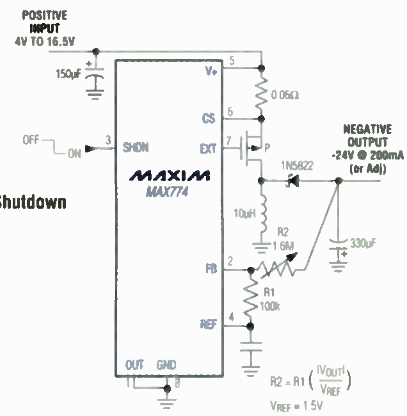
MAX735
- Small Size
- High Efficiency
- 160kHz Low-Noise PWM Control
- 10µA Logic-Controlled Shutdown
- Small Components
- MAX735EVKIT
- See also: MAX755 (adj. output)
MAX764/5/6 (low supply current)



Negative LCD Bias Supply is 83% Efficient

Input: 4V to 16.5V
Output: Unlimited Negative Voltage
Up to 4.8W

MAX774/MAX775/MAX776
- 83% Efficient from 10mA to 200mA (at -24V)
- 100µA (max) Supply Current
- 5µA (max) Logic-Controlled Shutdown
- 8-Pin SO Package
- 300kHz Current-Limited PFM Control Scheme
- MAX774EVKIT-SO

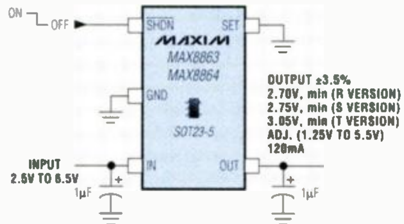


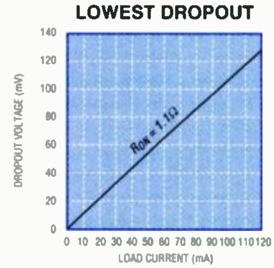
Small, Low-Noise Linear Regulators Have Lowest Dropout Voltages

Low-Noise, Miniature 120mA Linear Regulators Have Lowest Dropout

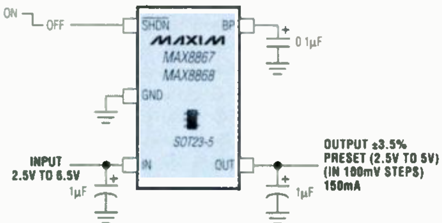
MAX8863/MAX8864

- 110mV Dropout at 100mA
- P-Channel MOSFET Pass Switches
- 80µA Supply Current at All Loads & in Dropout
- Smallest Output Capacitor: 1µF
- Active C_{OUT} Discharge in Shutdown (MAX8864 only)
- 1µA Shutdown Current
- Reverse Battery and Thermal Protection
- Output Current Limit
- For Same Pinout as '2980/'2981 see MAX8873/MAX8874





Best Combination of Low Dropout and Low Noise for 150mA SOT23 Linear Regulators



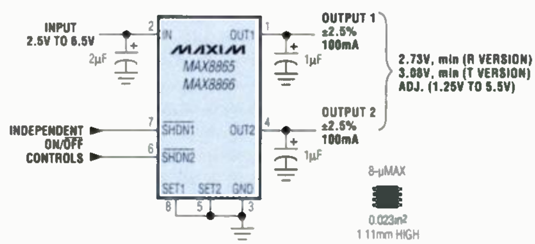
MAX8867/MAX8868 (Available 10/97)

- Low Output Noise, $30\mu V_{RMS}$
- Lowest Dropout:
  - 120mV at 100mA
  - 190mV at 150mA
- Low, 90µA Supply Current
- P-Channel MOSFET Pass Switch
- Preset Outputs in 100mV Steps (±3.5% accuracy)
- Reverse Battery Protection
- Output Current Limit
- 1µA Logic-Controlled Shutdown
- Short-Circuit and Thermal-Overload Protection
- Pin-Compatible with MAX8863/MAX8864
- For Same Pinout as '2982 see MAX8877/MAX8878

Dual, 100mA LDOs Fit in Only 0.024in^2 and 1.11mm Height

MAX8865/MAX8866

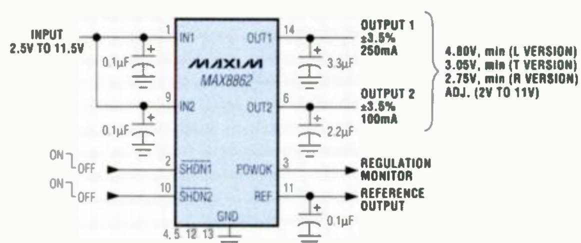
- 110mV Dropout at 100mA
- Fits in Small µMAX Package
- 145µA Supply Current at All Loads & in Dropout
- P-Channel MOSFET Pass Switches
- Smallest Output Capacitor: 1µF
- Active C_{OUT} Discharge in Shutdown (MAX8866 only)
- 1µA Shutdown Current
- Reverse Battery and Thermal Protection



Dual High- and Low-Power Linear Regulators Fit in Single Package to Save Space

MAX8862

- Dual 250mA and 100mA Outputs
- 1.8W High-Power SO Package (same size as standard 14-pin narrow SO)
- Low Dropout (200mV at 250mA)
- 1µA (max) Shutdown Current



MAXIM SECOND SOURCE	SAME SPECS AS:	COMPETITOR'S EQUIVALENT
MAX8873/MAX8874	MAX8863/MAX8864	'2980
		'2981
MAX8877*/MAX8878*	MAX8867/MAX8868	'2982

*Future product—available after November 1997

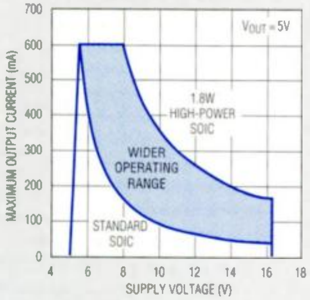
Now Available in Second-Source† Pinouts!

Maxim's SOT23 linear regulators are available with the same pinouts as the '2980/'2981 and '2982, so you can replace your SOT23 linears with lower dropout equivalents and get longer battery life.

† Maxim's maximum input voltage range is 6V operating, 6.5V absolute max

Low-Dropout, 500mA Linear Regulators Fit Small, High-Power Packages

WIDER OPERATING RANGE EASES DESIGN



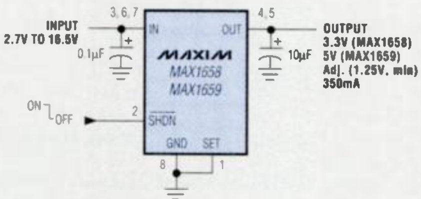
Maxim's high-power linear regulators use two unique technologies (P-channel MOSFET pass transistors and high-power packaging) to produce devices with low dropout voltages, very low supply currents (independent of output current), and wider operating ranges than those of typical bipolar regulators. This combination of features is ideal for small, low-cost battery-powered systems with widely varying operating conditions. These regulators have battery-saving features at light loads and still deliver low dropout at heavy loads, making them very versatile.

HIGH POWER, SMALL FOOTPRINT

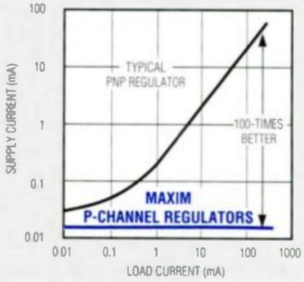
NEW Battery-Saving Linear Regulators Consume Only 30µA and Deliver 350mA

MAX1658/MAX1659

- Special High-Power 8-Pin SO Package Dissipates 1.2W
- Wide Input Range (2.7V to 16.5V)
- Low Dropout Voltage (490mV at 350mA)
- 30µA Supply Current
- ±3% Output Accuracy
- 1µA (max) Shutdown Current
- Thermal-Overload and Current-Limiting Protection



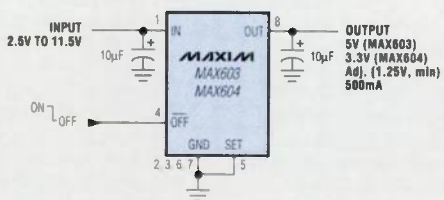
LOWEST SUPPLY CURRENTS = LONGEST BATTERY LIFE



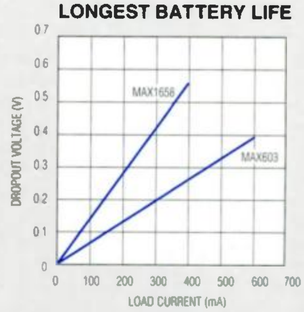
World's Smallest 500mA LDO Linear Regulator Fits in SO-8

MAX603/MAX604

- Special High-Power 8-Pin SO Package Dissipates 1.8W
- Wide Operating Range Eases Designs
- Low Dropout Voltage (320mV at 500mA)
- P-Channel Design Uses Only 15µA Supply Current at I_{OUT} = 500mA
- 2µA (max) Shutdown Current
- See Also: MAX882/3/4 (200mA I_{OUT} and LBI/LBO Low-Battery Detector)



LOWEST DROPOUT = LONGEST BATTERY LIFE



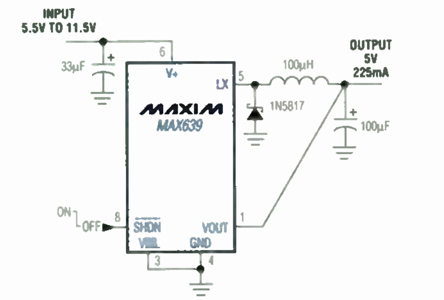
PART NUMBER	INPUT VOLTAGE (V, max)	OUTPUT CURRENT (mA)	$R_{DS(ON)}$ (5V OUT) (Ω)	SUPPLY CURRENT (µA)	POWER DISSIPATION (W)	PINS-PACKAGE	POWER SWITCH
MAX8863/4	6.5	120	1.1	80	0.57	5-SOT23	P-Channel
MAX8865/6	6.5	2 x 100	1.1	145	0.33	8-µMAX	Dual P-Channel
MAX8867*/8*	6.5	150	1.2	90	0.57	5-SOT23	P-Channel
MAX882/3/4	11.5	200	1.1	11	1.5	8-SO	P-Channel
MAX8862	11.0	250 & 100	0.8	250	1.5	14-SO	Dual P-Channel
MAX667	16.5	250	0.9	20	0.47	8-SO	PNP
MAX1658/9	16.5	350	1.4	30	1.2	8-SO	P-Channel
MAX603/4	11.5	500	0.65	15	1.8	8-SO	P-Channel
MAX687/8/9	11.0	>1A	External	150	N/A	8-µMAX	Ext. PNP

* Future product—available after October 1997

High-Efficiency 3.3V & 5V Step-

Maxim's step-down converters feature greater than 90% efficiency over wide load-current ranges, prolonging battery life at both light loads (10mA) and heavy loads (up to 10A). Many of these employ Maxim's proprietary Idle Mode™ control scheme, which saves battery life by automatically changing operating modes depending on the load current. At heavy and moderate loads, they pulse-width modulate (PWM) to diminish resistive losses due to high peak currents. At light loads, they pulse-frequency modulate (PFM) to minimize gate-charging losses and thus reduce quiescent supply current.

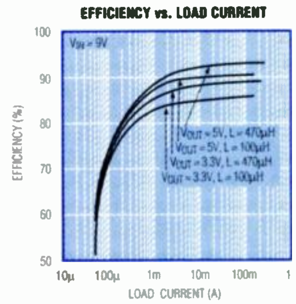
Idle Mode optimizes the converters' performance by responding to changing load demands without software intervention, simplifying system software design. However, you can also override automatic switchover and remain in PWM mode if the application requires low-noise, fixed-frequency output ripple even at light loads.

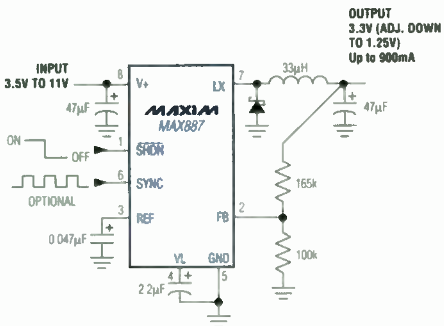


225mA Step-Down Uses Only 10µA Supply Current

MAX639 (5V)
- Lowest Quiescent Supply Current (10µA)
- High Efficiency Over Wide Load Range
- 4% Output Tolerance
- Few External Components
- 0.5V Dropout at 100mA
- LBI/LBO Low-Battery Detector
- MAX639EVKIT-SO
- See also: MAX640 (3.3V)
  MAX653 (3V)

Circuit A

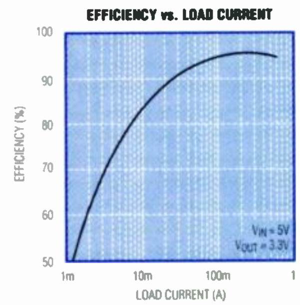


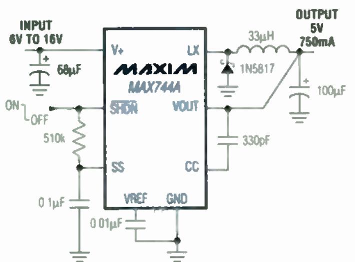


500mA, 94%-Efficient PWM Fits Synchronous Rectifier and Main Switch in 8-Pin SO

MAX887 (3.3V or adj.)
- Compact 8-Pin SO Package
- Internal Synchronous Rectifier
- 94% Efficient
- 300kHz Idle Mode™ PWM Operation
- Allows External Synchronization (10kHz to 400kHz)
- 2µA Logic-Controlled Shutdown
- Small External Components
- Minimum Dropout Voltage
- MAX887EVKIT-SO

Circuit B

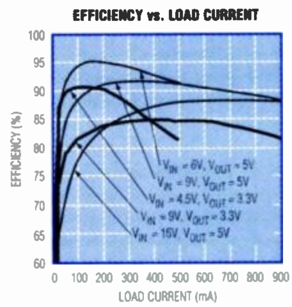




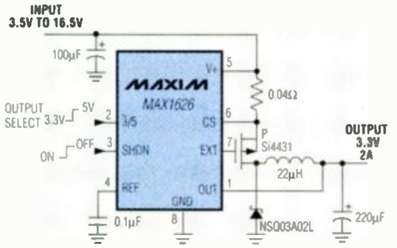
750mA PWM Step-Down Exhibits No Subharmonic Switching Noise

MAX744A (5V)
- 159kHz to 212.5kHz Oscillator Avoids 455kHz IF Band
- Low 1.7mA Quiescent Supply Current
- Low 6µA Shutdown
- MAX744AEVKIT-SO
- See also: MAX730A, MAX738A (5V)
  MAX763A, MAX748A (3.3V)
  MAX750A, MAX758A (adj.)

Circuit C



Down Converters Deliver Up to 10A

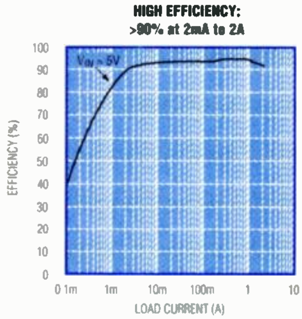


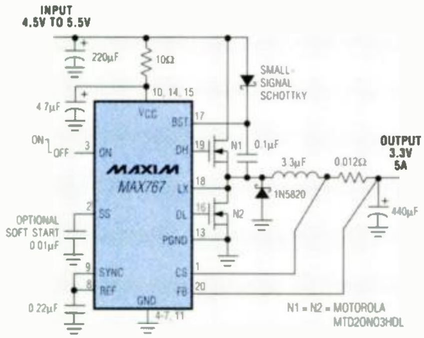
2A Step-Down Gives Longest Battery Life

MAX1626 (3.3V or 5V)

- Lowest Dropout: 100% Duty Cycle (350mV at 2A)
- >90% Efficiency from 10mA to 2A
- 70µA Supply Current
- 1µA (max) Logic-Controlled Shutdown
- 8-Pin SO Package
- 300kHz Current-Limited PFM Control
- MAX1626EVKIT-SO
- See also:
  MAX1627 (adj. output)
  MAX1649/MAX1651

Circuit D



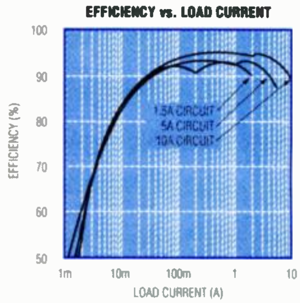


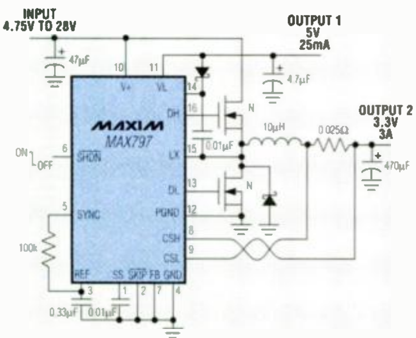
5A Pentium™ & PowerPC™ Supply Fits in 1.4in^2, No Heatsink Needed

MAX767 (3.45V or 3.6V)

- Dedicated 5V to 3.3V Solution
- Up to 10A Output, All N-Channel Design
- Component Selection & Suppliers Listed for 1.5A, 3A, 5A, 7A, & 10A Applications
- Low 700µA Quiescent Supply Current
- Low 120µA Standby Supply Current
- MAX767EVKIT-SO
- See also: MAX767R (3.45V), MAX767S (3.6V)

Circuit E



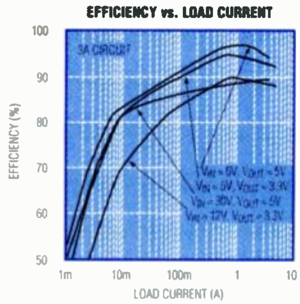


High-Current, High-Efficiency Step-Down Takes 28V Inputs

MAX797 (3.3V or adj.)

- Up to 10A Output
- Adjustable Output
- 5V Linear Regulator Output
- 150kHz/300kHz Fixed-Frequency PWM Operation
- Low-Cost All N-Channel Design
- 375µA Quiescent Supply Current (5V out)
- 1µA Shutdown
- MAX797EVKIT-SO

Circuit F



High-Efficiency 3.3V & 5V Step-Down DC-DC Converters

IOUT	VIN (V, max)	PART NUMBER	CIRCUIT	TYPE	NOTES
75mA	16.5	MAX638	–	PFM	16.5V input range
200mA	16.5	MAX667	–	Low-Dropout Linear Regulator	16.5V input range
225mA	11.5	MAX639/40/53	Circuit A	PFM	Lowest quiescent supply current (10µA)
250mA	11.5	MAX882/3/4	–	Low-Dropout Linear Regulator	Package power dissipation = 1.5W
500mA	11.5	MAX603/4	–	Low-Dropout Linear Regulator	Package power dissipation = 1.8W
750mA	16	MAX744A/48A	Circuit C	PWM	Internal P-channel MOSFET, no subharmonic noise
900mA	11	MAX887	Circuit B	Idle Mode™ PWM with Sync. Rect.	Compact, internal switches, synchronizable
2A	16.5	MAX1649/51	–	PFM Controller	Low quiescent supply current (110µA)
2A	16.5	MAX1626/27	Circuit D	PFM Controller with 100% Duty Cycle	Lowest quiescent supply current (70µA), low dropout, high efficiency
10A	5.5	MAX767	Circuit E	Idle Mode™ PWM Controller with Sync. Rect.	Dedicated 5V to 3.3V converter
10A	30	MAX796/7/9	Circuit F	Idle Mode™ PWM Controller with Sync. Rect.	30V input range, adjustable output
10A	30	MAX782/3/6	–	Idle Mode™ PWM Controller with Sync. Rect.	Dual-output system-integrated supplies

Pentium is a trademark of Intel Corp. PowerPC is a trademark of IBM Corp. Idle Mode is a trademark of Maxim Integrated Products

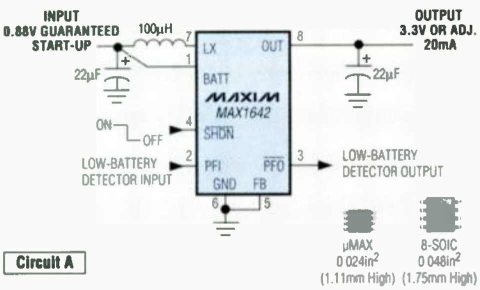
Step-Up from 1 to 3 Battery Ce
High Efficiency, Low Quie

Maxim's step-up DC-DC converters provide the best combination of low quiescent current, high efficiency, and small size. They are the perfect choice for battery-powered portable applications.

Maxim offers a broad range of low-voltage step-up DC-DC converters that operate from single-battery-cell inputs (down to 0.9V) up to regulated 3.3V system supply inputs. The following circuits are primarily intended to generate main-system supply voltages (usually 3.3V or 5V) or 5V flash memory supplies in battery-powered hand-held systems. However, these circuits (like the MAX619 and MAX608) can also be used as local 5V supplies in otherwise 3V-only systems. We assume that a battery "cell" has a 0.9V minimum voltage and is nominally 1.2V.

NEW 0.88V Start-Up Pager Supply Fits Synchronous Rectifier in Ultra-Small Package

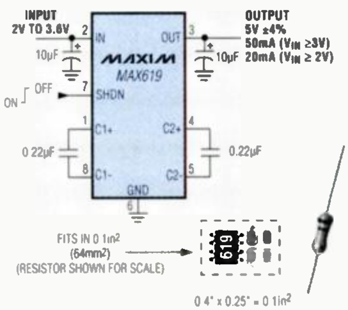
MAX1642/MAX1643
- 83% Efficiency
- Ultra-Small µMAX Package:
  - 1/2 Area of 8-Pin SO
  - 1.11mm High
- 0.88V Guaranteed Start-Up
- Internal Synchronous Rectifier
- 11µA Quiescent Supply Current
- 2µA Logic-Controlled Shutdown (MAX1642)
- Two Low-Battery Detectors (MAX1643)
- 2V to 5.2V Output Range
- MAX1642EVKIT



Circuit A

5V Backup Supply Fits in 0.1in²

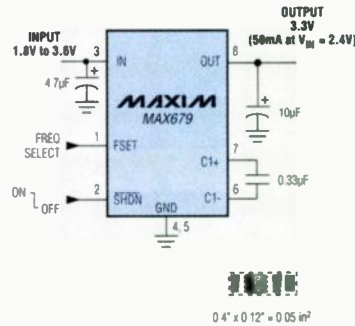
MAX619
- No Inductor—Low-Profile
- 1µA Logic-Controlled Shutdown
- 75µA Supply Current
- Low-Cost Components
- MAX619EVKIT-SO



Circuit B

NEW 3.3V Backup Supply Fits in 0.05in²

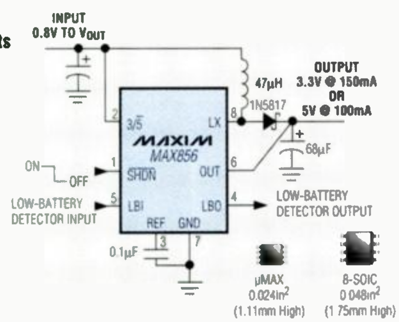
MAX679
- No Inductors
- 1.11mm-High µMAX Package
- 50µA Supply Current
- 1µA Shutdown
- Up to 1MHz Operation



Circuit C

Small 2-Cell Step-Ups: 85% Efficiency, 25µA Quiescent Current

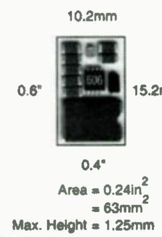
MAX856
- 85% Efficiency
- µMAX Package (1.11mm High)
- 25µA Supply Current
- 1µA Shutdown
- Current Limiting Permits Ultra-Small Inductor
- MAX856EVKIT-MM
- See also:
  - MAX857 (Adj, 125mA)
  - MAX858 (3.3V/5V, 35mA)
  - MAX859 (Adj, 35mA)
  - MAX756 (3.3V/5V, 300mA)
  - MAX757 (Adj, 300mA)

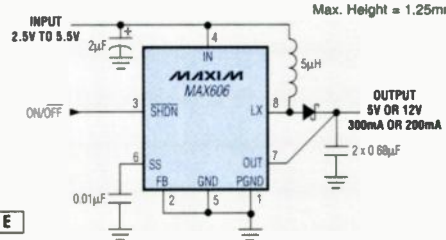


Circuit D

Entire 5V Step-Up Fits Thin Type-1 PCMCIA Cards

MAX606/MAX607
- 1MHz Switching Frequency (MAX606)
- 1.25mm-High External Components
- 1.11mm-High µMAX Package
- Low 200µA Quiescent Supply Current
- 1µA (max) Shutdown
- Soft-Start Prevents Surge Currents
- 5V, 12V, or Adjustable Output
- MAX606EVKIT-MM



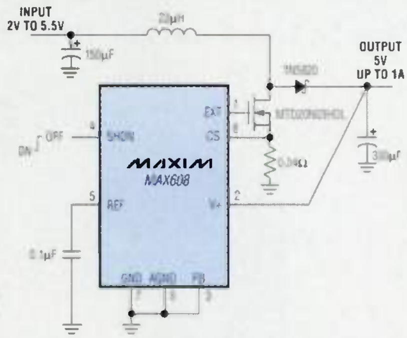


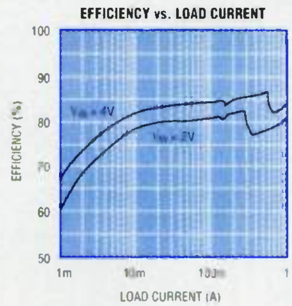
Circuit E

Idle Mode is a trademark of Maxim Integrated Products

lls with the Best Combination of scent Current, and Small Size

1A Step-Up Converter Boosts 2V Inputs with High Efficiency

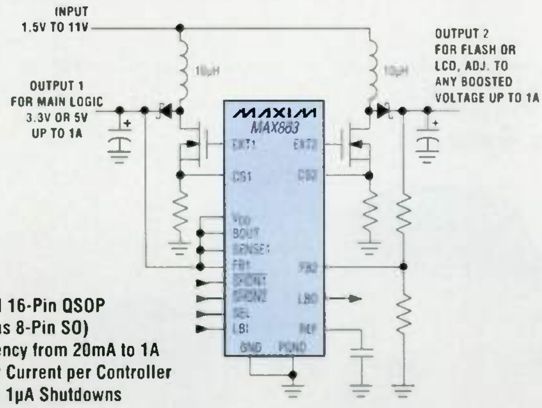




MAX608
- Down to 2V Inputs
- Adj. Output: V_{IN} to 16.5V
- >80% Efficiency from 20mA to 1A
- Small External Components
- 1µA Shutdown Current
- Current-Limited PFM
- MAX608EVKIT-SO
- See also: MAX1771 (unlimited V_{OUT})
  MAX770–MAX773

Circuit F

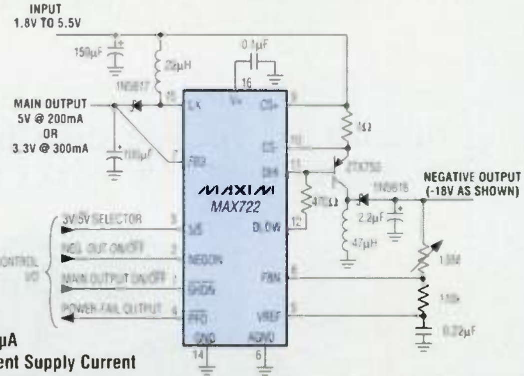
NEW Smallest Dual-Output Boost DC-DC Converter Powers Logic & LCD or Flash from 1.5V Input



MAX863
- Fits in Small 16-Pin QSOP (same size as 8-Pin SO)
- >90% Efficiency from 20mA to 1A
- 45µA Supply Current per Controller
- Independent 1µA Shutdowns
- Current Limiting
- Step-Up/Down Configurable
- MAX863EVKIT-SO

Circuit G

Dual-Output Step-Up: 5V or 3.3V Plus Negative LCD Bias from 2 Cells



MAX722
- Low 60µA Quiescent Supply Current
- Low 20µA Shutdown
- 87% Efficiency at 200mA
- Small External Components
- Detects Output Power Failure
- MAX722EVKIT-SO
- See also: MAX723 (3V)
  MAX717–MAX721 (3.3V/5V plus 12V Flash)

Circuit H

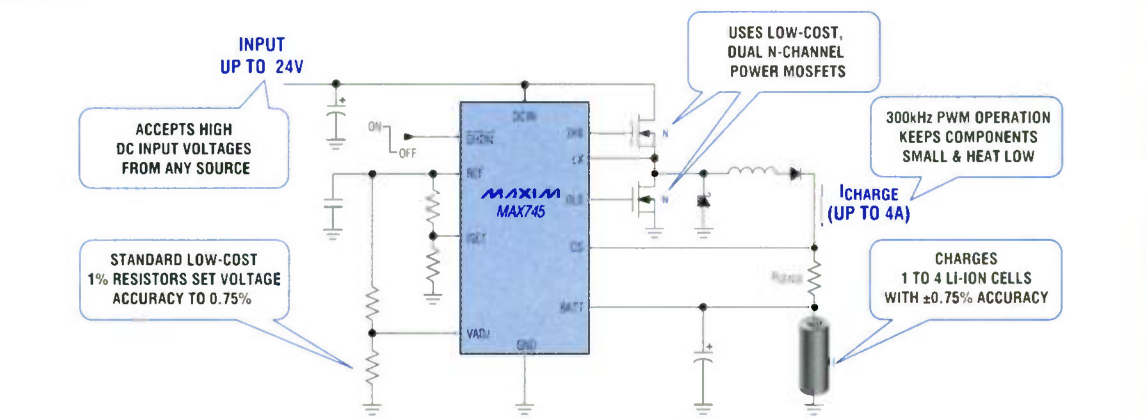
Low-Voltage Step-Up Converters

INPUT (NO. OF BATTERY CELLS*)	5V OUTPUT CURRENT	3.3V OUTPUT CURRENT	PART NUMBER	CIRCUIT	NOTES
1	15mA	20mA	MAX866/7	–	Guaranteed to 0.9V start-up
			MAX1642/3	Circuit A	Guaranteed to 0.88V start-up, internal synchronous rectifier = high efficiency
	Up to 300mA	Up to 500mA	MAX1700 Family	Front page	See MAX1700/1, MAX1703, MAX1705/6, MAX848/9 on front page
2 or 3	–	60mA	MAX679	Circuit C	No inductors, smallest size
	50mA	–	MAX619	Circuit B	No inductors, smallest size
	100mA	125mA	MAX856–859	Circuit D	µMAX package, 85% efficiency, 25µA I_Q
	200mA	300mA	MAX756/7		Best combination of high efficiency & low I_Q
			MAX717–721	Circuit H	Dual output: OUT1 = 3.3V/5V, OUT2 = 5V/12V
			MAX722/3		Dual output: OUT1 = 3.3V/5V, OUT2 = negative
		–	MAX606/7	Circuit E	1MHz switching, 1.25mm max circuit height
	Up to 1.1A	Up to 1.5A	MAX1700 Family	Front page	See MAX1700/1, MAX1703, MAX1705/6, MAX848/9 on front page
	1A	1A	MAX608	Circuit F	0.65mA supply current, 2V input, adj. V_{OUT}
		1A	MAX1771	–	0.65mA supply current
	2 x 1A	2 x 1A	MAX863	Circuit G	Dual-output boost in small package

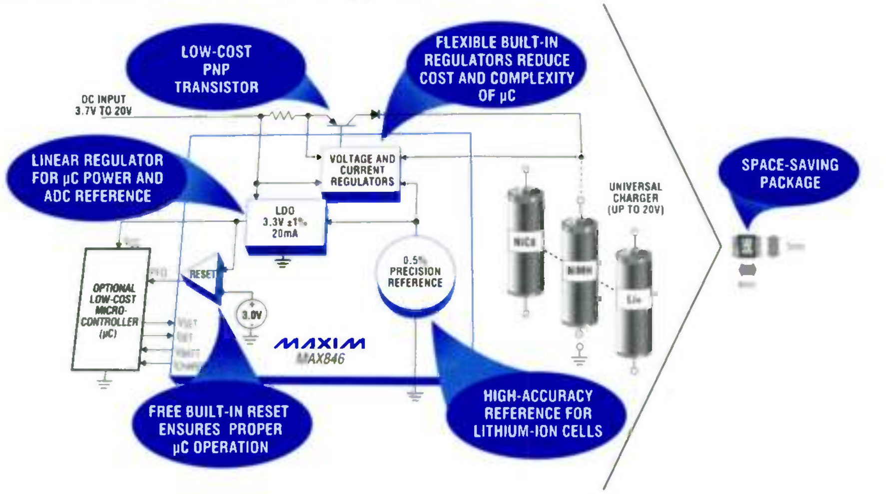
* EACH CELL = 0.9V TO 1.6V

High-Accuracy Battery Ch
Give Faster Charges

±0.75% Precision Li-Ion Charger Delivers 4A Without Heating



Precise 1% Voltage and Current Regulator Forms Core of Low-Cost Charger System



PART	CHEMISTRY				DESCRIPTION
	Li+	NiCd	NiMH	Multi	
MAX745	✔				Switch-Mode, Stand-Alone
MAX846A	✔	✔	✔	✔	Linear-Mode, Stand-Alone System or Microcontroller Adjustable
MAX1647/1648	✔	✔	✔	✔	Switch-Mode w/SMBus™ Interface
MAX2003A		✔	✔		Switch-Mode, Stand-Alone
MAX712/713		✔	✔		Linear-Mode, Stand-Alone
MAX1640/1641		✔	✔	✔	Switch-Mode, Current-Source

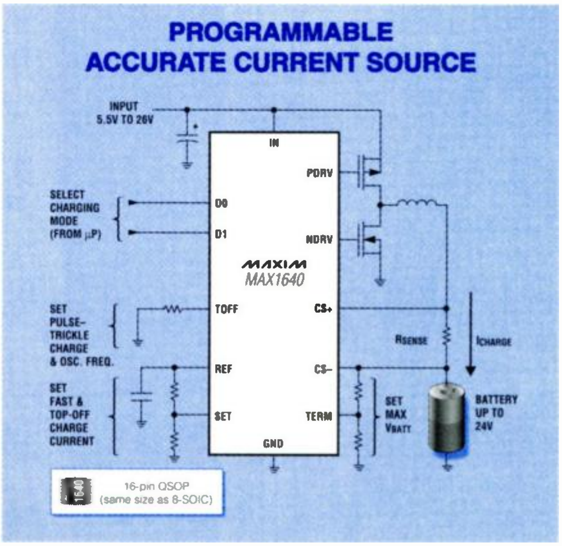
SMBus is a registered trademark of Intel Corp.

argers and Current Sources and Longer Run-Time

NEW Programmable Current Source Reduces Heat with 95%-Efficient DC-DC Conversion

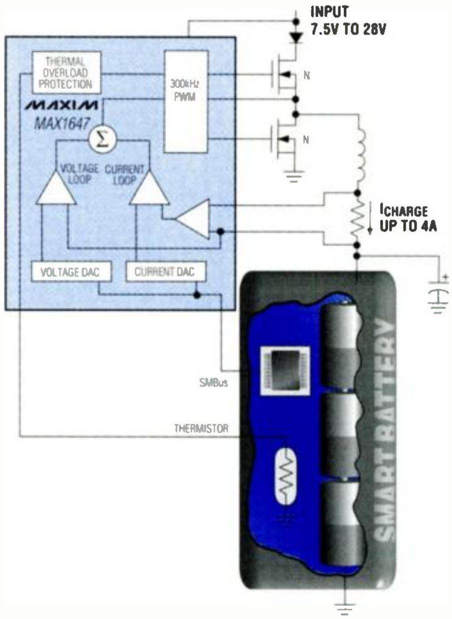
MAX1640/MAX1641

- 2%-Accurate Current Regulation (MAX1641) (5% for MAX1640)
- 16-Pin QSOP Package (same size as SO-8)
- 5.5V to 26V Input Range
- Optional Synchronous Rectifier for Higher Efficiency
- High-Side (MAX1640) or Low-Side (MAX1641) Current Sensing
- Adjustable Voltage Limit (2V to 24V)
- Up to 500kHz PWM Operation
- MAX1640EVKIT



World's First SMBus™ Smart Battery Charger: Highly Integrated, High-Efficiency Chemistry-Independent Charger

- SMBus:
  - Fastest Charge Times
  - Longest Battery Life
  - Chemistry Independent
- High Efficiency:
  - Low Temperature Rise— Very Important in Today's Notebook Computers
  - Smallest Size: No Heatsink
  - Low Cost: No Heatsink
- High Performance and Integration:
  - 0.2% Voltage Accuracy
  - Digitally Programmable Voltage and Current
  - Charges Any Chemistry, to 4A
  - Internal Battery Thermal Protection



Regulated Charge Pumps Provide Compact, Low-Cost Power without Inductors, for Portable Equipment

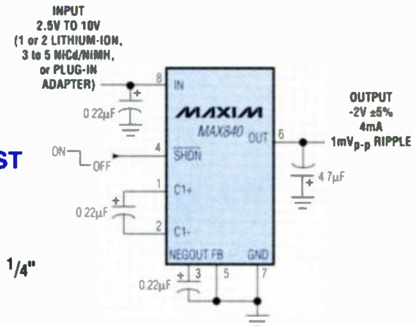
Complete Bias Generator for GaAsFET Power Amps—Lowest Noise and Smallest

MAX840

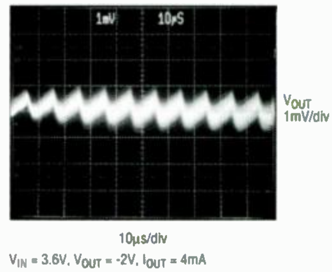
- Lowest Noise: 1mVp-p Output Ripple
- Fits in 0.1in²
- Power Directly from Lithium Battery
- Replaces 8 Components & 2 ICs
- 1µA (max) Shutdown
- MAX840EVKIT-SO
- See also:
  MAX843/MAX844
  (Adj. Output & LCD Features)
  MAX850–MAX853

SMALLEST SIZE

LOWEST INPUT VOLTAGE



LOWEST NOISE: 1mVp-p OUTPUT NOISE AND RIPPLE

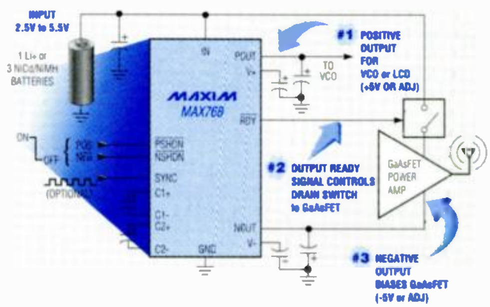


Low-Noise Dual Supply for GaAsFET Power-Amp Bias and VCO

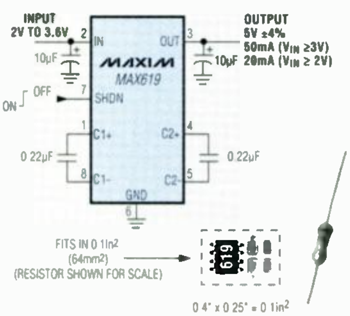
Compact IC Performs 3 Power-Supply Jobs for Wireless Handsets

MAX768

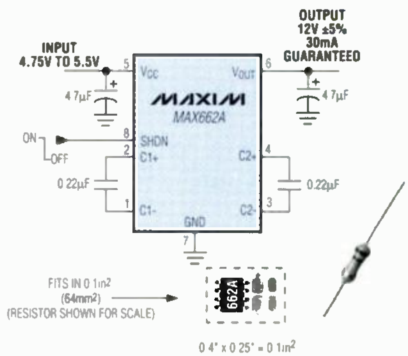
- Dual Positive/Negative Regulated Outputs: ±5VOUT from 3VIN
- Output-Ready Indicator Controls GaAsFET Drain Switch
- 2mVp-p Output Ripple
- Synchronizable Switching Frequency
- 0.1µA Independent Shutdown Controls
- Adjustable Output Voltages



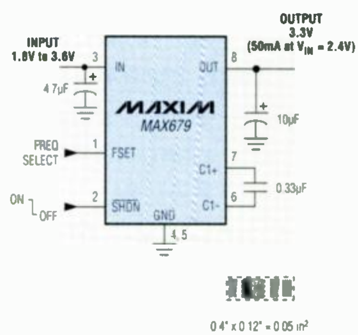
Compact 5V Backup Supply Fits in 0.1in²



12V Output Without Inductors: Fits in 0.1in²



NEW 3.3V Supply Boosts from 1.8V Input, Fits in 0.05in²



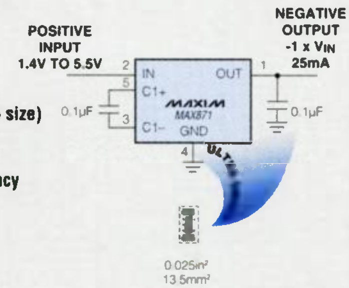
MAXIM

DC-DC Conversion Without Inductors: Charge Pumps Save Space and Cost

NEW Smallest Charge-Pump Inverters Use 0.1µF Capacitors to Bias GaAsFET Power Amps

MAX870/MAX871

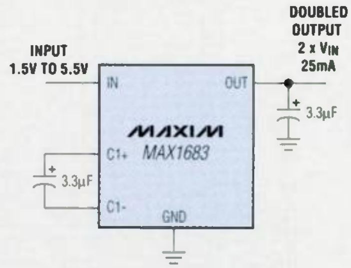
- Smallest Circuit:
  - 0.025in² (16mm²)
  - SOT23-5 Package
  - 0.1µF Capacitors (0805 size)
- 25mA Output Current
- 20Ω Output Impedance
- 0.5MHz Switching Frequency
- Shutdown Mode



NEW Smallest Charge-Pump Doubler is 1/4 Size of '7660: Fits in SOT23-5

MAX1682/MAX1683 (Available 11/97)

- Smallest Circuit:
  - SOT23-5 Package
  - 3.3µF Capacitors
- 90µA Quiescent Supply Current (MAX1682)
- Switching Frequency Above Audio Range (MAX1683, 35kHz)
- 20Ω Output Impedance
- 1.5V to 5.5V Input Range



Save Space and Power Over the '7660—Choose the Best Features for Your Application

PARAMETER	'7660	MAX828	MAX829	MAX870	MAX871	MAX1682*	MAX1683*
Package	SO-8	SOT23-5	SOT23-5	SOT23-5	SOT23-5	SOT23-5	SOT23-5
Output Impedance (Ω)	55	20	20	20	20	20	20
Oscillator Frequency (kHz)	10	12	35	125	500	12	35
Capacitors (µF)	10 (for 55Ω)	10 (for 20Ω)	3.3 (for 20Ω)	1 (for 20Ω)	0.1 (for 35Ω), 0.33 (for 20Ω)	10 (for 20Ω)	3.3 (for 20Ω)
Configuration	Both	Inverter	Inverter	Inverter	Inverter	Doubler	Doubler

*Future product—available after November 1997

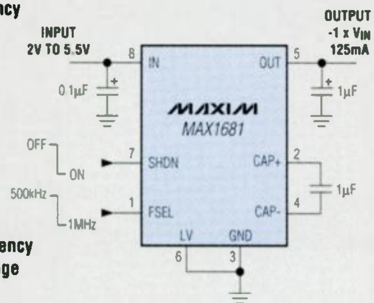
Smallest 50mA/125mA Charge Pumps Operate Up to 1MHz, Produce Positive or Negative Outputs Using 1µF Caps

NEW MAX1680/MAX1681

- 125mA Output
- Up to 1MHz Switching Frequency
- Fit in 8-Pin SO Package
- Use 1µF Capacitors for 3.5Ω Output Impedance
- Invert or Double the Input
- 1µA Shutdown
- Pin Compatible with MAX660

MAX860/MAX861

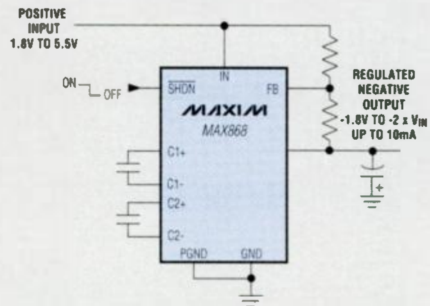
- 50mA Output
- Up to 250kHz Switching Frequency
- Fit in 8-Pin SO or µMAX Package (1/2 size of 8-pin SO)
- Use 2.2µF Caps for 12Ω Output
- Invert or Double the Input
- 1µA Shutdown
- Pin Compatible with MAX660



NEW Smallest Regulated Inverting Charge Pump Optimizes Capacitor Size, ROUT, and Supply Current

MAX868 (Available 10/97)

- Set Output from -1.8V to -2 x V_{IN} using Two Resistors
- Switching Frequency Varies with Load Demand:
  - Small Capacitors (0.22µF for 10mA load)
  - Low Supply Current (35µA at no load)
- Low 70Ω Output Resistance (with 0.22µF caps)
- 0.1µA Logic-Controlled Shutdown
- 10-Pin µMAX Package (1/2 size of 8-pin SO, 1.11mm high)



Part Number	Input Voltage Range (V)	Output Voltage (V)	Quiescent Supply Current (mA), max(typ)	Output (mA)	Control Scheme	Pins-Package Options*	Temp. Ranges**	EV Kit	Features	Price† 1000-up ($)
STEP-UP SWITCHING REGULATORS										
MAX606/607	3 to 5.5	5 or 12 or adj.	0.5(0.25)/0.3(0.15)	200	PFM	8-μMAX	E	Yes	1MHz switching frequency fits Type 1 PCMCIA cards	3.25
MAX608	1.8 to 16.5	5 or adj.	0.11(0.085)	1A	PFM	8-DIP, 8-SO	E	Yes	Same as MAX1771, but accepts low input voltages	1.89
MAX629	2.7 to 28	V_{IN} to 28 or 0 to -28	0.100(0.080)	10 at 28V	PFM	8-SO	E	Yes	30V/0.5A internal switch, configure as +28V or -28V	2.85
MAX630	2 to 16.5	Adj.	0.125(0.070)	30mW	PFM	8-DIP, 8-SO	C,E,M		Improved RC4123 second source	2.88
MAX631/632/633	1.5 to 5.6/ 12.6/15.6	5/12/15 or adj.	0.4(0.135)/ 2(0.5)/2.5(0.75)	40/25/20	PFM	8-DIP, 8-SO	C,E,M		Only two external components	2.56
MAX641/642/643	1.5 to 5.6/ 12.6/15.6	5/12/15 or adj.	0.4(0.135)/ 2(0.5)/2.5(0.75)	300/550/ 325	PFM	8-DIP, 8-SO	C,E,M		PFM controller	2.87
MAX731	1.8 to 5.25	5	4(2)	200	PWM	8-DIP, 16-WSO	C,E,M	Yes		2.60
MAX732	4 to 9.3	12	3(1.7)	200	PWM	8-DIP, 16-WSO	C,E,M	Yes		2.76
MAX733	4 to 11	15	3(1.7)	125	PWM	8-DIP, 16-WSO	C,E,M	Yes		2.60
MAX734	1.9 to 12	12	2.5(1.2)	120	PWM	8-DIP, 8-SO	C,E,M	Yes	12V flash memory, hot insert	2.23
MAX752	1.8 to 16	Adj.	3(1.7)	2.4W	PWM	8-DIP, 8-SO	C,E,M	Yes		2.94
MAX756/757	1.1 to 5.5	(3.3 or 5)/adj.	0.060(0.045)	250	PFM	8-DIP, 8-SO	C,E	Yes	Best combination of low I_Q & high 86% efficiency	1.95
MAX761/762	2 to 16.5	12/15 or adj. to 16.5	0.1(0.080)	120	PFM	8-DIP, 8-SO	C,E,M	Yes	12V flash memory, lowest I_Q, 1.8V/3V/5V inputs	2.23
MAX770/771/772	2 to 16.5	5/12/15 or adj.	0.1(0.085)	1A	PFM	8-DIP, 8-SO	C,E,M	Yes	Controllers, high efficiency over wide I_{OUT} range	1.80
MAX1771	2 to 16.5	12 or adj.	0.1(0.085)	1A	PFM	8-DIP, 8-SO	C,E,M	Yes	Same as MAX771, but with single 100mV current-sense limit	1.80
MAX773	3 to 16.5	Adj.	0.1(0.085)	1A	PFM	14-DIP, 14-NSO	C,E,M		Controller, high-voltage applications	1.80
MAX848/849	0.7 to 5.5	3.3 or 2.7 to 5	0.06	100 to 600	PWM	16-NSO	E	Yes	1-3 cell step-up, low-noise, fixed-frequency PWM	2.38/2.50
MAX856/857	0.5 to 6	(3.3 or 5)/adj.	0.060(0.025)	100	PFM	8-SO, 8-μMAX	C,E	Yes	Smallest, best combination of low I_Q & high 85% efficiency	1.72
MAX858/859	0.5 to 6	(3.3 or 5)/adj	0.060(0.025)	25	PFM	8-SO, 8-μMAX	C,E	Yes	Smallest, best combination of low I_Q & high efficiency	1.72
MAX863	1.5 to 11	2 pos. adj.	65(40)	1A	PFM	16-QSOP	E	Yes	Dual output, lowest I_Q, high efficiency	2.80
MAX866/867	0.5 to 6	(3.3 or 5)/adj.	0.06(0.027)	90	PFM	8-SO	E	Yes	Guaranteed 0.9V start-up, low I_Q	1.76
MAX1642/1643	0.7 to 5.5	3.3 or adj.	16(10)	90	PFM	8-μMAX	E	Yes	High efficiency, synchronous rectifier, dual LBI/LBO	1.76
MAX1700/1701	0.7 to 5.5	2.5 to 5.5	0.100(0.060)	800	PWM/ PFM	8-SO/16-QSOP	E	Yes (1700)	1V guaranteed start-up, MAX1701 includes 2 battery monitors and op-amp block	††
MAX1703	0.8 to 5.5	3.3 or adj. (2.7 to 5.5)	0.140(0.100)	1.5A	PWM/ PFM	16-NSO	E	Yes	1.1V guaranteed start-up, 92% efficiency	††
MAX1705/1706	0.7 to 5.5	2.5 to 5.5 (dual)	0.190(0.100)	800/500	PWM/ PFM	16-QSOP	E	Yes	Dual output: step-up and 200mA linear regulator, 1V guaranteed start-up	3.15/2.96
STEP-UP/DOWN SWITCHING REGULATORS										
MAX710/711	1.8 to 11	3.3 or 5/adj.(2.7 to 5)	0.1(0.08)	250	PFM	16-NSO	E	Yes	No transformer, step-up and linear	2.95
MAX761	2.7 to 12	Adj. (1.5 to 6)	0.1(0.08)	200	PFM	8-DIP, 8-SO	C,E,M		No transformer, SEPIC	2.23
MAX1672	1.8 to 11	5 or 3.3 or adj. (2.7 to 5.0)	0.125(0.100)	150	PFM	16-QSOP	E	Yes	Step-up followed by linear regulator, in/out disconnect in shutdown	††

* Package Options: DIP = Dual-In-Line Package, SO = Small Outline (N = Narrow, W = Wide), SSOP = Shrink Small-Outline Package, μMAX = Micro Max, TO-__ = Can
** Temperature Ranges: C = 0°C to +70°C, E = -40°C to +85°C, I = -25°C to +85°C, M = -55°C to +125°C
† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchanges.
†† Future product—contact factory for pricing and availability. Specifications are preliminary.

DC-DC Switching Converters (continued)

Part Number	Input Voltage Range (V)	Output Voltage (V)	Quiescent Supply Current (mA), max(typ)	Output (mA)	Control Scheme	Pins-Package Options*	Temp. Ranges**	EV Kit	Features	Price† 1000-up ($)
STEP-DOWN SWITCHING REGULATORS										
MAX638	2.6 to 16.5	5, adj.	0.6(0.135)	75	PFM	8-DIP, 8-SO	C,E,M			2.56
MAX639/640/653	4 to 11.5	5/3.3/3 or adj.	0.02(0.01)	225	PFM	8-DIP, 8-SO	C,E,M	Yes	Ultra-low I_Q	2.96
MAX1649/1651	3 to 16	5/3.3 or adj.	0.1(0.080)	2A	PFM	8-DIP, 8-SO	C,E	Yes	Drives external P-channel FET, low I_Q, but with 96.5% duty cycle and single 100mV current-sense limit	1.60
MAX1626/1627	3 to 16.5	3.3 or 5/adj.	0.080(0.060)	2A	PFM	8-SO	E	Yes	Same as MAX1651, but with 100% duty cycle, high efficiency, and controller	1.88
MAX730A/50A/63A	Up to 11	5/adj./3.3	3(1.7)	500	PWM	8-DIP, 8-SO	C,E,M	Yes	No subharmonic switching noise	2.15
MAX738A/48A/58A	Up to 16	5/3.3/adj.	3(1.7)	750	PWM	8-DIP, 16-WSO	C,E,M	Yes	No subharmonic switching noise	2.60
MAX744A	4.75 to 16	5	2.5(1.2)	750	PWM	8-DIP, 16-WSO	C,E,M	Yes	Optimized for cellular communications, no subharmonic switching noise	2.90
MAX1640/1641	5.5 to 30	6 to 30	4(2)	50W	PWM	16-QSOP	E	Yes	High-efficiency current-source, synchronous rectifier	2.75
MAX767	4.5 to 5.5	3.3, 3.45 (R), or 3.6 (S)	0.75	1.5A to 10A	PWM	20-SSOP	C,E	Yes	Dedicated 5V-to-3.3V, high efficiency, small size	3.40
MAX796/797/799	4.5 to 30	5.05/3.3/2.9/adj.	1(0.7)	50W	PWM	16-DIP, 16-NSO	C,E,M	Yes	Synchronous rectifier, secondary output regulation, high efficiency over full I_{OUT} range	3.65
MAX887	4 to 11	Adj.(1.27 to 9)	0.5(0.2)	500mA	PFM/ PWM	8-SO	E	Yes	Internal synchronous rectifier, high efficiency, synchronizable	2.44
INVERTING SWITCHING REGULATORS										
MAX735/755	4 to 6.2	-5/adj.	3(1.6)	275	PWM	8-DIP, 8-SO	C,E,M		>80% efficiencies	2.15
MAX736/37/39/59	4 to 8.6	-12/-15/-5/adj.	3(1.6)	500	PWM	14-DIP, 16-WSO	C,E,M	Yes	>80% efficiencies	2.75
MAX749	2 to 6	Digital adj.	0.06	5W	PFM	8-DIP, 8-SO	C,E,M	Yes	Digital adjust for negative LCD	2.49
MAX764/765/766	3 to 16.5	-5/-12/-15 or adj. to 21ΔV	0.1	200	PFM	8-DIP, 8-SO	C,E,M	Yes	Lowest I_Q	2.38
MAX774/775/776	3 to 16.5	-5/-12/-15 or adj.	0.1	1A	PFM	8-DIP, 8-SO	C,E,M	Yes	Controllers, high efficiency over wide I_{OUT} range	2.20
DUAL-OUTPUT SWITCHING REGULATORS										
MAX624	3 to 5.5	5 & 12 or adj.	0.6(0.3)	200 at 5V 80 at 12V	PFM	16-NSO	I		1.2MHz switching frequency fits Type 1 PCMCIA cards	5.25
MAX685	2.7 to 5.5	Pos: 2.7 to 24 Neg: -1.3 to -9	2(1)	10/output	PWM	16-QSOP	E	Yes	CCD power supply, single inductor, internal switches	††
MAX742	4.2 to 10	±12, ±15	15(8)	±15W	PWM	20-DIP, 20-WSO	C,E,M	Yes	Drives external MOSFETs	3.91
MAX743	4.2 to 6	±12, ±15	30(20)	±1.5W	PWM	16-DIP, 16-WSO	C,E,M	Yes	Internal power MOSFETs	4.49
MAX863	1.5 to 11	2 pos. adj.	65(40)	1A each	PFM	16-QSOP	E	Yes	Lowest I_Q, high efficiency	2.80
MAX1705/1706	0.7 to 5.5	Switcher: 2.5 to 5.5 LDO: down to 2.5	0.190(0.100)	800/500	PWM/ PFM	16-QSOP	E	Yes	Step-up, LDO, 1V guaranteed start-up	3.15/2.96
MAX717–721	0.9 to 5.5 (battery), 7 to 18 (plug-in adapter)	3.3 (MAX717), 3.3 or 5 (MAX718/720), 3 or 5 (MAX719/721) plus 5 or 12	60, 40 in shutdown	300 @ 3.3V, up to 2.5W on 12V	PFM	16-NSO	C, E	Yes	Dual output for 3.3V and 5V logic or 12V PCMCIA/LCD	4.95
MAX722/723	0.85 to 5.5 (battery), 7 to 18 (plug-in adapter)	3.3 or 5 (MAX722), 3 or 5 (MAX723)	60, 40 in shutdown	300 @ 3.3V, up to 2.5W on neg output	PFM	16-NSO	C, E	Yes	Dual output for 3.3V or 5V logic and negative LCD to -40V	4.63

* Package Options: DIP = Dual-In-Line Package, SO = Small Outline (N = Narrow, W = Wide), SSOP = Shrink Small-Outline Package, µMAX = Micro Max, TO-__ = Can

** Temperature Ranges: C = 0°C to +70°C, E = -40°C to +85°C, I = -25°C to +85°C, M = -55°C to +125°C

† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchanges rates.

†† Future product—contact factory for pricing and availability. Specifications are preliminary.

Part Number	Input Voltage Range (V)	Output Voltage (V)	Quiescent Supply Current (mA), max(typ)	Output (mA)	Pins-Package Options*	Temp. Ranges**	EV Kit	Features	Price† 1000-up ($)
CHARGE-PUMP CONVERTERS—UNREGULATED									
MAX660	1.5 to 5.5	$-V_{IN}$, $+2 \times V_{IN}$	0.5(0.12)	100	8-DIP, 8-SO	C,E,M		8-pin SO	2.95
MAX680	2 to 6	$\pm 2 \times V_{IN}$	2(1)	±10	8-DIP, 8-SO	C,E,M		Dual output	1.62
MAX828/829	1.25 to 5.5	$-V_{IN}$	0.09(0.06)	25	5-SOT23	E		Better than ICL7660, smaller capacitors, ultra-small, lower R_{OUT}	1.30
MAX860/861	1.5 to 5.5	$-V_{IN}$, $+2 \times V_{IN}$	0.33(0.18)	50	8-SO, 8-μMAX	C,E,M		Up to 250kHz oscillation frequency	1.45
MAX864	1.5 to 6.2	$\pm 2 \times V_{IN}$	0.3(0.2)	±10	16-QSOP	E		5kHz to 200kHz frequency select, 1μA shutdown	1.50
MAX865	1.5 to 6.2	$\pm 2 \times V_{IN}$	1.0(0.6)	±10	8-μMAX	E		Ultra-small μMAX package	1.30
MAX870/871	1.25 to 5.5	$-V_{IN}$	1(0.7)	25	5-SOT23	E		Smallest inverter, 0.1μF capacitors, 500kHz switching	1.30
MAX1044	1.5 to 10	$-V_{IN}$, $+2 \times V_{IN}$	0.2(0.03)	20	8-DIP, 8-SO	C,E,M		60kHz oscillator boost mode	1.19
MAX1680/1681	2 to 5.5	$-V_{IN}$, $+2 \times V_{IN}$	2(1.2)	125	8-SO	E		125kHz to 1MHz operation, small capacitors, same pinout as MAX660	2.05
MAX1682/1683	1.5 to 5.5	$+2 \times V_{IN}$	0.09 (0.06)	25	5-SOT23	E		Improved ICL7660, small caps, ultra-small SOT23, lower R_{OUT}	††
ICL7660	1.5 to 10	$-V_{IN}$, $+2 \times V_{IN}$	0.175(0.110)	20	8-DIP, 8-SO, 8-TO99, 8-μMAX	C,E,M		μMAX package	1.09
ICL7662	4.5 to 20	$-V_{IN}$, $+2 \times V_{IN}$	0.6(0.25)	10	8-DIP, 8-SO, 8-TO99	C,I			1.86
Si7661	4.5 to 20	$-V_{IN}$, $+2 \times V_{IN}$	2(0.3)	10	8-DIP, 8-SO, 8-TO99	C,I			1.86
CHARGE-PUMP CONVERTERS—REGULATED									
MAX619	2 to 3.6	5	0.15	60	8-DIP, 8-SO	C,E,M	Yes	No inductors, battery backup	1.60
MAX622	3.5 to 16.5	$V_{IN} + 11$	0.5(0.07)	500μA	8-DIP, 8-SO	C,E		High-side switching	1.86
MAX662A	4.5 to 5.5	12	0.5(0.19)	30mA, guaranteed over temp.	8-DIP, 8-SO	C,E,M	Yes	World's smallest 12V flash memory programmer	2.09
MAX679	1.8 to 4	3.3	0.050(0.035)	20	8-μMAX	E	Yes	Up to 1MHz f_{OSC}, small caps	1.55
MAX768	2.5 to 5.5	Dual ±5 or adj.	0.8(0.45)	2 x 10mA	16-QSOP	E		Performs 3 power functions for handsets: $-2 \times V_{IN}$ for GaAsFET bias, $+2 \times V_{IN}$ for VCO, negative power-ready signal	2.40
MAX840/843/844	2.5 to 10	-2 or adj.	1.1(0.75)	10	8-SO	I,E	Yes	Low-voltage negative GaAsFET bias, low noise, 1μA shutdown	1.75
MAX850–853	4.5 to 10	-4.1 or adj.	3(2)	5	8-SO	I,E	Yes	Negative GaAsFET bias, low noise, 1μA shutdown	1.65
MAX868	1.8 to 5.5	Adj., (-1.8 to $-2 \times V_{IN}$)	0.050(0.035)	10	10-μMAX	E		Supply current varies with load, uses 0.22μF caps	††
MAX881R	2.5 to 5.5	-2 or adj.	0.9(0.5)	5	10-μMAX	E	Yes	GaAsFET PA bias in 1.11mm-high package, includes power-OK output signal	††

* Package Options: DIP = Dual-In-Line Package, SO = Small Outline (N = Narrow, W = Wide), SSOP = Shrink Small-Outline Package, μMAX = Micro Max, TO-__ = Can

** Temperature Ranges: C = 0°C to +70°C, E = -40°C to +85°C, I = -25°C to +85°C, M = -55°C to +125°C

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Battery Chargers

Part Number	No. of Cells Charged	Cell Chemistry	Charge Rate	Charge Termination Method	Pins-Package Options*	Temp. Ranges**	EV Kit	Features	Price† 1000-up ($)
MAX712/713	1 to 16	NiMH/NiCd	Fast, trickle	0ΔV, max V, max temp, max time (neg ΔV, MAX713)	16-DIP, 16-NSO	C,E,M	Yes	Linear or switcher, supplies load while charging, built-in termination algorithms	3.09
MAX745	1 to 4	Li+	Digital prog.	Voltage and current limit	20-SSOP	E	Yes	High-efficiency switch mode, 0.75% precision	4.50
MAX846A	1 to 10	Li+/NiCd/NiMH	Fast, trickle, top-off	Universal charger, user set	16-QSOP	E	Yes	Complete system, 1%-accurate V_{OUT} for Li+, built-in 1% LDO, drives PNP, cost-saving, independent V & I reg loops	3.25
MAX1640/1641	1 to 16	Universal	Fast, trickle, top-off	Voltage and current limit	16-QSOP	E	Yes	High-efficiency PWM current-source, synchronous rectifier	2.75
MAX1647/1648	1 to 8	Universal	Digitally programmed	Voltage and current limit, thermistor	20-SSOP/16-NSO	E	Yes	SBS level 2 smart-battery charger with SMBus interface (MAX1647)	4.79/4.25
MAX2003/A	1 to 16	NiCd and/ or NiMH	Fast, trickle, top-off	Temp slope, neg. ΔV, max temp, max time	16-DIP, 16-WSO 16-NSO	C	Yes	Linear, built-in termination algorithms, discharge-before-charge, pulse trickle (A)	3.25/3.80

LCD & CCFL Display Power Supplies

Part Number	Input Voltage Range (V)	DC-DC Output Voltages (V)	Quiescent Supply Current (µA)	Pins-Package Options*	EV Kit	Features	Price† 1000-up ($)
MAX629	2.7 to 28	V_{IN} to 28 or 0 to -28	80	8-SO	Yes	Internal 30V/0.5A switch	2.85
MAX749	2 to 6	Negative LCD	60	8-DIP, 8-SO	Yes	Digital LCD adjustment	2.49
MAX753	6 to 24	CCFL drive, configurable; negative LCD, configurable	100	16-DIP, 16-NSO		Digital CCFT and LCD adjustment	4.45
MAX754	6 to 24	CCFL drive, configurable; positive LCD, configurable	100	16-DIP, 16-NSO		Digital CCFT and LCD adjustment	4.45
MAX759	4 to 15	Negative LCD, adjustable	1.2mA	14-DIP, 16-WSO	Yes	Internal MOSFET	2.75
MAX774/775/776	3 to 16.5	Negative LCD, adjustable	85	8-DIP, 8-SO	Yes	PFM controller, high efficiency, 5µA shutdown	2.20
MAX828/829	1.25 to 5.5	$-V_{IN}$	60	5-SOT23		No inductors, low-cost compact pager supply, better than '7660	1.30
MAX860/861	1.5 to 5.5	$-V_{IN}$ or 2 x V_{IN}	180	8-SO, 8-µMAX		No inductors, up to 250kHz oscillator, 2.2µF caps, smallest pager LCD supply	1.45
MAX868	1.8 to 5.5	Adj.($-V_{IN}$ to -2 x V_{IN})	35	10-µMAX	Yes	Supply current varies with load, compact, low I_Q for pagers	††
MAX870/871	1.25 to 5.5	$-V_{IN}$	700	5-SOT23		Smallest inverter, uses 0.1µF capacitors, 500kHz switching	1.30
MAX1044	1.5 to 10	$-V_{IN}$ or 2 x V_{IN}	30	8-DIP, 8-SO		No inductors, 60kHz boost pin, pager LCD supply	1.19
MAX1610	4.5 to 28	CCFL drive, configurable	2mA	16-SO	Yes	Internal MOSFET, digital adjust, open and shorted lamp protection	3.85
MAX1611	4.5 to 28	CCFL drive, configurable	2mA	16-SO	Yes	Internal MOSFET, digital SMBus adjust, open and shorted lamp protection	3.85
MAX1620	4.5 to 24	Positive or negative LCD, configurable	500	16-QSOP		Digital adjust, 32 levels	1.99
MAX1621	4.5 to 24	Positive or negative LCD, configurable	500	16-QSOP		SMBus adjust, 32 levels	1.99
MAX1771	2 to 16.5	Positive LCD, adjustable	85	8-DIP, 8-SO	Yes	PFM controller, high efficiency, 5µA shutdown	1.80

* Package Options: DIP = Dual-In-Line Package, SO = Small Outline (N = Narrow, W = Wide), SSOP = Shrink Small-Outline Package, µMAX = Micro Max, TO-__ = Can

** Temperature Ranges: C = 0°C to +70°C, E = -40°C to +85°C, I = -25°C to +85°C, M = -55°C to +125°C

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load a symbol table);
- HostAccessSymbols (access the symbol table); and
- HostPromptUser (ask the user for additional information).

Build and implementation issues—The debugger must be able to find the VABS DLL and to verify that it is compatible with the version of the VABS interface supported. There are several valid approaches to this problem, but for simplicity we can encode all of the information needed into the DLL filename.

For some environments, such as Windows NT, the DLL must use the same run-time model as the debugger. If the debugger is multithreaded, then the DLL also must be built for multithreading. To ensure compatibility and to simplify debugging, the DLL also should use the same run-time version and linking model as the debugger.

A subtle disadvantage of the DLL model in a single-threaded environment, as opposed to a separate process model, involves receiving asynchronous events from the vehicle. In a single-threaded system, only one part of the system has control of the processor at any given time. If the VABS needs to poll the vehicle for events, it may miss events if it doesn't have control of the processor when an event comes in.

The best way to handle this condition is with multiple threads. However, the DLL model can still be salvaged in environments that don't support multiple threads by registering the communication channel with the debugger. The debugger can then check the channel for activity during its normal processing loop and pass control to the VABS as needed to handle in-coming events.

Future Directions

The future may see tool customization extended to the application domain. Tool vendors are coming to realize that developing and debugging applications in the telecommunications industry, for example, share certain characteristics within that industry, but they may not be the same as those shared within the automotive industry.

In general, there is a trend in the software industry toward viewing products as servers and exposing interfaces that allow new clients to be developed and individual server components to be replaced by third-party components. The long-term results should enable sharply focused domain-specific solutions that leverage the efforts of tool vendors who are free to focus on their core markets.

Doug Salot is the run-time integration lead for the XRAY Pro debugger product group at Microtec Corp. He holds a BA in biochemistry and computer science from the University of California, San Diego, and was previously vice president of engineering at Systems & Software Inc.

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Circle 520

Circuit-Break Locator For The Holidays

W. STEPHEN WOODWARD
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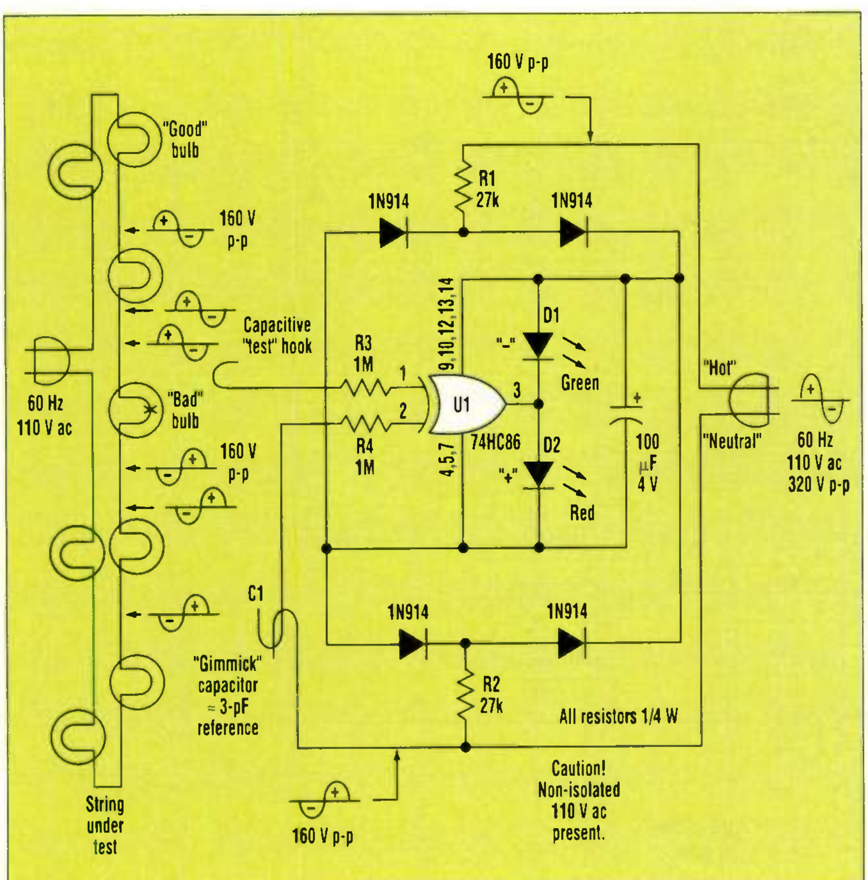
Early every January, my household, like many, undertakes the "Ordeal of Post-Christmas Undecoration." One of the chores associated with dismantling and packing away Christmas ornaments is fixing those strings of series-connected miniature incandescent lamps in which a filament has opened up, the internal filament-bypass device has failed to work, and a whole array of 50 or 100 lights has consequently gone dark. I've discovered there aren't many activities as well-calculated to dampen any lingering holiday cheer as having to do several of these haystack/needle searches. The circuited illustrated here comes to the rescue by sniffing out defective bulbs by capacitively sensing the electric fields they produce *(see the figure)*.

To understand how it works, consider a string of bulbs with an open-circuited filament, labeled in the schematic as "String Under Test." The intact filaments on either side of the burned-out bulb complete continuous circuits from the ac supply all the way around to the opposite ends of the broken filament. The ac voltage differential between wires leading to any intact bulb is zero, but the differential between the connections to the defective bulb will be the full 110 V. The presence of 110 V ac on a wire produces large electrostatic fields that are easily detected through plastic insulation. The high-impedance CMOS inputs of "XOR" U1 can do just that.

Resistors R1 and R2, in addition to delivering operating power to the circuit, effectively suspend U1 midway between the ac supply rails. Thus, equal-amplitude (160 V p-p) but opposite-phase voltage differentials will exist between U1 and both ac rails. R4 and C1 reference U1 pin 2 to ac "neutral," while R2 and the "Test" electrode are used to capacitively probe the voltages present in the wires of the String Under Test. U1 then performs as a phase-sensitive detector of those ac voltages.

Suppose the Test electrode is held close to point A. Because A is continuous with the "hot" rail, the signals at U1's inputs will have opposing phases. One input will be high (logic one) whenever the other is low (logic zero). This causes XOR U1 to hold pin 3 high, so D2 glows. If the probe is moved to points B or C, the same phase relationship will persist and D2 will still glow. But if the probe is brought near D, the sensed phase will reverse because the circuit break lies between D and the hot rail. Consequently, neutral phase voltage is induced in the probe. Pin 3 will therefore go low, extinguishing D2, lighting D1, and thus designating the offending filament. The defective lamp then is replaced.

In actual use, when the bad-bulb search is commenced near the power-plug end of the String Under Test,the initial phase relationship will be arbitrary, so either D1 or D2 may glow. In either case, it's the sudden change in which a LED is lit as the probe is moved along the String Under Test that indicates when the broken filament has been found.



This frustration-reducing circuit-break locator quickly locates bulbs with failed internal filament-bypass devices among strings of series-connected miniature incandescent lamps.

VOTE!

Read the Ideas for Design in this issue, select your favorite, and circle the appropriate number on the Reader Service Card. The winner receives a $300 Best-of-Issue award.

Circle 521

A PC Printer-Port-Based 12-Bit AC Power Controller

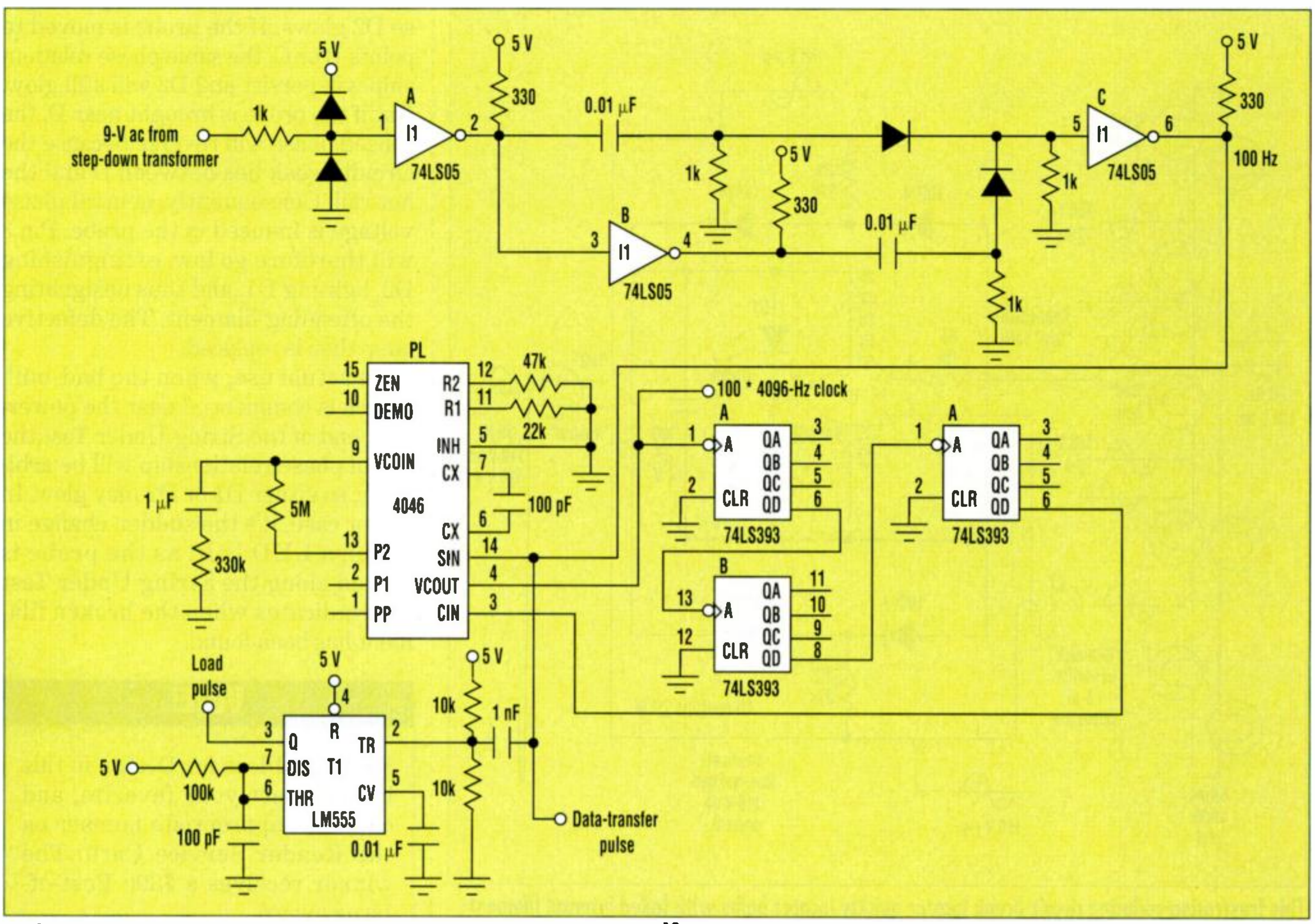
PRAMOD UPADHYAY
National Institute of Immunology, Aruna Asaf Ali Marg, New Delhi 110067, India; fax: 91-11-6162125; e-mail: pkumar@nii.ernet.in.

A thyristor switch typically is used when controlling power in the kilowatt range. In a thyristor, the output power is controlled by controlling the time (or phase angle) during which the thyristor remains "closed" in a conduction cycle. To control phase-angle firing, the circuit must be able to detect when the line voltage crosses zero, and then determine how long to wait before firing a control element in each half cycle.

The digitally controlled phase-angle firing circuit described here generates an ac mains synchronous clock of 4096*2*ac main frequency. At the start of every half cycle of ac power, a set of counters running at 4096*2*ac power frequency counts a 12-bit number. At the end of the count, a triac is fired. The 12-bit number is output through the data port of the parallel printer adapter. Because the data port is only 8 bits wide, data is written in two steps and a "buffer" data layer is introduced to transfer the entire 12 bits in one step to the counters.

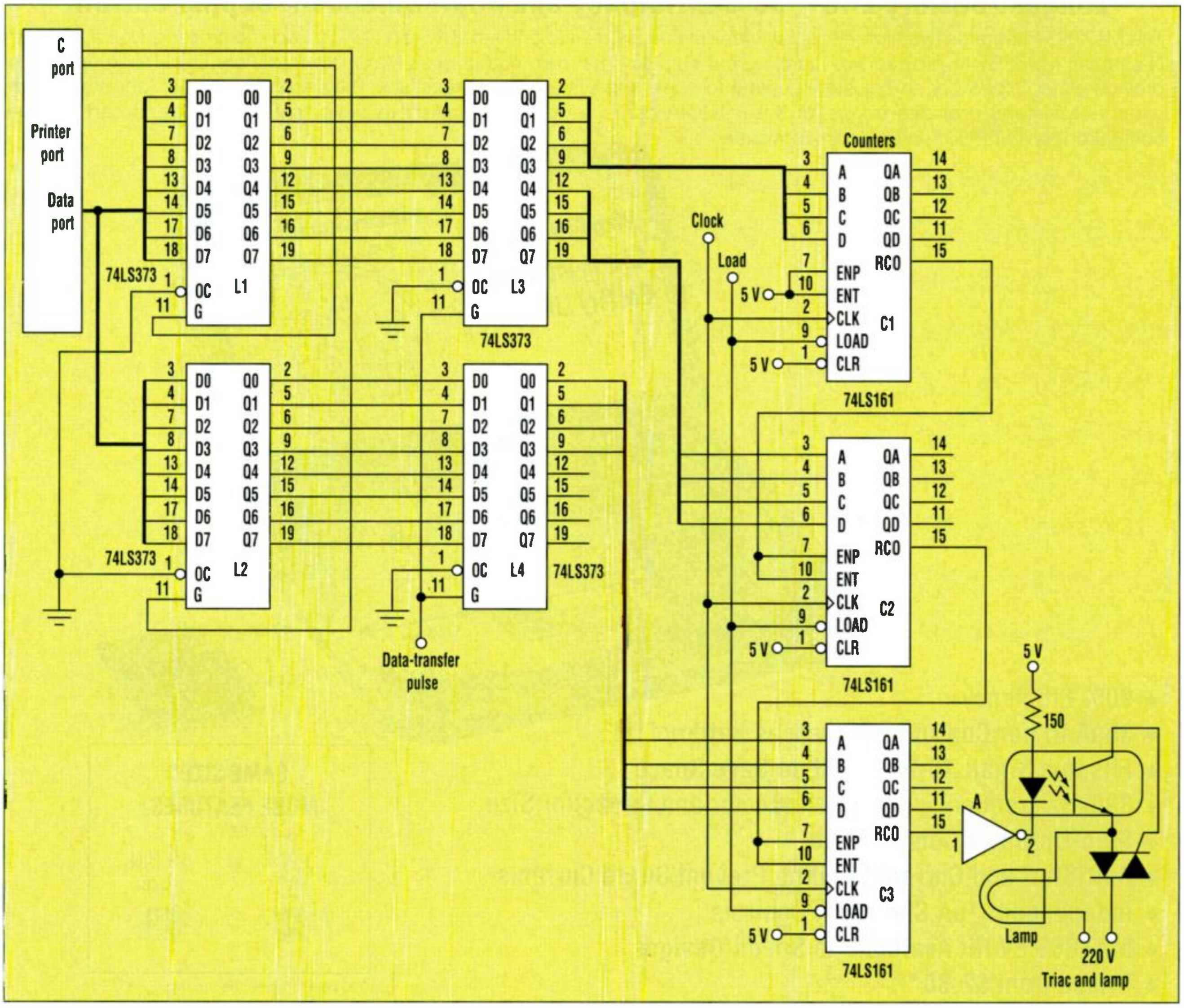
Looking at the circuit diagram of the timer, a 1-kΩ resistor and two diodes produce an ac mains synchronous square wave clipped to 0-5 V *(Fig. 1)*. A positive differentiator is created by an RC network around inverters I1(A) and I1(B). These inverters produce a spike at every zero crossing of ac mains. Inverter I1(C) sums these two spikes to create a pulse at every zero crossing of the ac line voltage. The clock frequency appearing at the output of I1(C) is 2*ac line frequency. In our case, this frequency is 100 Hz, with the ac mains frequency being 50 Hz. Since a 12-bit controller is desired, every half cycle of ac mains should be marked with 4096 points. This is accomplished by multiplying 4096 with an ac mains synchronous 100-Hz signal using the phase-locked loop PL. The 100*4096-Hz clock is fed to counter C1, C2, and C3.

The diagram of the data multiplexer shows that the PC printer port is connected to two octal transparent latches (LS373), and the respective latch is selected by two bits of the control port *(Fig. 2)*. The circuit works as follows: A 12-bit signal is divided into two parts, one 8-bit-wide LSB and the other 4-bit MSBs. The eight LSB bits are written to latch L1, and four MSBs



1. The timer circuitry generates an ac mains synchronous clock running at 2^{12}*2*ac-line frequency to run the trigger delay counter in Figure 2.

to L2. To transfer the complete 12-bit word to the counter in one pass, two layers of latches—one layer comprised of latches L1 and L2 and the other L3 and L4—are introduced. The ac-line synchronous 100-Hz signal is used to transfer data from latch L1/L2 to latch L3/L4. After some delay, introduced by timer T1, this signal also is used to load counters C1, C2, and C3. At the end of the countdown, the carry output "fires" the triac.



2. The thyristor firing angle is controlled with 12-bit accuracy by latching 2 bytes of data output from the PC's parallel printer port.

Circle 522

Get An 8-Bit Parallel Port From A PC's Serial Port

YONGPING XIA
Teldata Inc., 8723A Bellanca Ave., Los Angeles, CA 90045.

The interface circuit described here provides a bidirectional 8-bit parallel port operated through a PC's serial port. The serial port also powers the circuit so that no additional power supply is required.

An 8-bit universal shift/storage register (74HC299) is used to buffer the input/output data *(see the figure)*. The 74HC299 needs four control signals to perform the shift, load, and output enable functions. These signals

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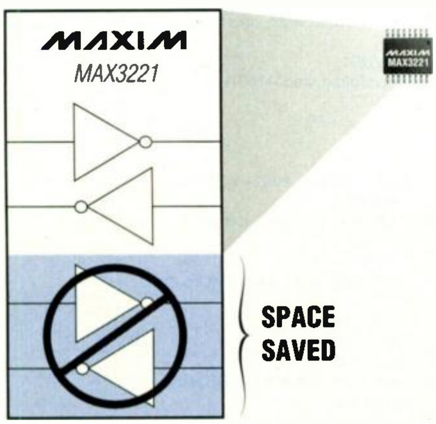
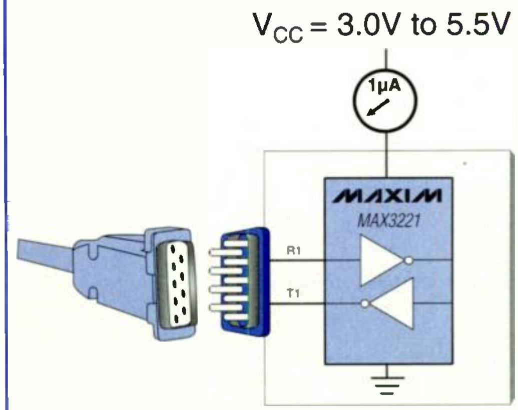
Maxim's new MAX3221 is the first single-supply, 1-transmitter/1-receiver RS-232 IC. It is available in a 16-pin SSOP package that reduces board space 50% over previous RS-232 transceivers. And, the MAX3221 guarantees data rates up to 120kbps.

Eliminate a Transceiver and Cut Board Space



AutoShutdown™ Reduces Supply Current to 1µA



Select the Space-Saving RS-232 Transceiver for Your Design

PART	No. of Tx/Rx	SUPPLY VOLTAGE (V)	SUPPLY CURRENT (µA)	PIN-PACKAGE	DATA RATE (kbps)
MAX3221	1/1	3.0 to 5.5	1	16 SSOP	230
MAX3223	2/2	3.0 to 5.5	1	20 SSOP	230
MAX3243	3/5	3.0 to 5.5	1	28 SSOP	230

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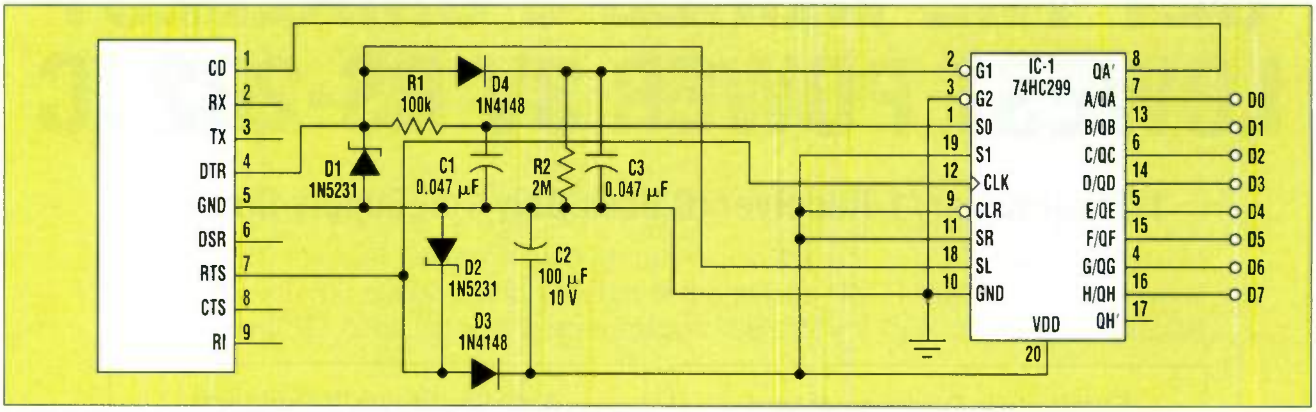
Circle No. 146 - For U.S. Response
Circle No. 147 - For International



This simple circuit converts a PC's serial port to a self-powered, 8-bit bidirectional parallel I/O port.

```
#include <stdio.h>
#include <dos.h>
#include <conio.h>
#include <math.h>

#define MCR        4        /* control register     */
#define MSR        6        /* status register      */

int i, out=0, base_add1=0x3f8, base_add2=0x2f8, read_data=0;

void set_port(void)
{
   out⇒=0x03;
   outportb(base_add1+MCR, out); /* power on      */
   delay(1000);
}

void send_clock(void)
{
   out&=0xfd;
   outportb(base_add1+MCR, out);
   delay(1);
   out⇒=0x02;
   outportb(base_add1+MCR, out);
   delay(1);
}
void read_port(void)
{
   out⇒=0x01;
   outportb(base_add1+MCR, out);
   delay(100);
   send_clock();
   read_data=0;
   for  (i=0; i<8; i++)
   {
      read_data+=(inportb(base_add1+MSR)&0x80)/128*pow(2,i);
      out&=0xfe;
      outportb(base_add1+MCR, out);
      delay(8);
      send_clock();
      out⇒=0x01;
      outportb(base_add1+MCR, out);
      delay(20);
   }
}

void write_port(int write_data)
{
   out⇒=0x01;
   outportb(base_add1+MCR, out);
   delay(100);
   for (i=0; i<8; i++)
   {
      out&=0xfe;
      outportb(base_add1+MCR, out);
      delay(8)
      if (write_data!=write_data/2*2)
      {
         outi=0x01;
         outportb(base_add1+MCR, out);
      }
      send_clock();
      write_data/=2;
      out⇒=0x01;
      outportb(base_add1+MCR, out);
      delay(10);
   }
   out&=0xfe;
   outportb(base_add1+MCR, out);
}

void dis_data(void)
{
   gotoxy(2, 1);
   printf("data = %d      ", read_data      );
}

void main(void)
{
   clrscr();
   set_port();
   /* read port         */
   read_port();
   dis_data();
   /* write 0x55 to port  */
   write_port (0x55);
}
```

are: CLK (clock), S0 (shift/load control), SL (serial input), and G1 (output enable). In addition, the serial port also should provide a stable power supply to the IC.

Because the serial port has only two directly controllable lines (pin 4 and 7), a few signals have to share one output line. The power supply (V_{dd}) and CLK share pin 7, which normally is high. The clock signal is generated by a C program with high duty cycle *(see the listing)*. Note that both pin 4 and pin 7 are clamped to 5.1 V by D1 and D2.

The IC will be powered by C2 when pin 7 is low. C2 will be recharged when pin 7 returns high. The S0, SL, and G1 signals are formed on pin 4. In Load mode, pin 4 is high such that one clock signal will load input D0-D7 into the IC. In Shift mode, the duty cycle of the pin 4 signal is selected to keep S0 low and G1 high. In Output mode, pin 4 remains low so that the data in the IC will appear on D0-D7.

IFD WINNER

Patrick Guelle, 55, Rue de Richelieu,B.P. 279, 76055 Le Havre Cedex (France); tel/fax: +33 02 35 43 53 53. The idea: *"Tiny Smart Card OS for PIC16C84"* April 1,1997 Issue.

JULY 1998

IEEE Power Engineering Society Summer Meeting, July 12-16. Sheraton San Diego Hotel & Marina, San Diego, CA. Contact Terry Snow, San Diego Gas & Electric, P.O. Box 1831, San Diego, CA 92112; (619) 696-2780; fax (619) 699-5096; e-mail: t.snow@ieee.org.

SPIE's Annual Meeting & Optical Instrumentation Show, July 19-24. San Diego, California. Contact SPIE Exhibits Dept., P.O. Box 10, Bellingham, Washington 98227-0010; (360) 676-3290; fax (360) 647-1445; e-mail: exhibits@spie.org.

IEEE Nuclear & Space Radiation Effects Conference (NSREC '98), July 20-24. Newport Beach, California. Contact Jim Schwank, Sandia National Laboratories, Post Office Box 5800, MS-1083, Albuquerque, New Mexico 87185-1083; (505) 844-8376; fax (505) 844-2991; e-mail: schwanjr@sandia.gov.

AUGUST 1998

AUTOTESTCON '98, August 24-27. Salt Palace Convention Center, Salt Lake City, Utah. Contact Robert Myers, Myers/Smith Inc., 3685 Motor Avenue, Suite 240, Los Angeles, California 90034; (310) 287-1463; fax (310) 287-1851; e-mail: bob.myers@ieee.org.

OCTOBER 1998

IEEE International Conference on Systems, Man, & Cybernetics, October 12-14. Hyatt Regency La Jolla, La Jolla, California. Contact M.A. Jafari, Dept. of Industrial Engineering, Rutgers University, P.O. Box 909, Piscataway, New Jersey 08855; (908) 445-3627; (908) 445-5467; e-mail: jafari@gandalf.rutgers.edu.

NOVEMBER 1998

Photonics East & Electronic Imaging International Exhibition, November 1-6. Boston, Massachusetts. Contact SPIE Exhibits Department, Post Office Box 10, Bellingham, Washington 98227-0010; (360) 676-3290; fax (360) 647-1445; e-mail: exhibits@spie.org.

Voice, Video & Data Communications Conference & Exhibition, November 1-6. Boston, Massachusetts. Contact SPIE Exhibits Dept., Post Office Box 10, Bellingham, Washington 98227-0010; (360) 676-3290; fax (360) 647-1445; e-mail: exhbits@spie.org.

IEEE Global Telecommunications Conference (Globecom '98), Nov. 9-13. Sydney, Australia. Contact Sam Reisenfeld, School of Electrical Engineering, University of Technology, Sydney, P.O. Box 123; Broadway, NSW 2007, Australia; +61 2-330-2435; e-mail: samr@trnasmit.ee.uts.edu.au.

DECEMBER 1998

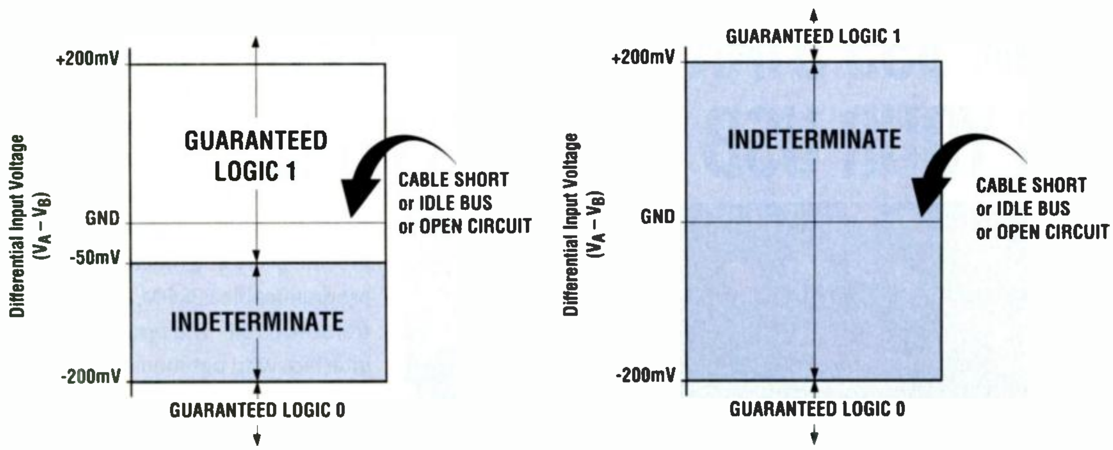
12th Systems Administration Conference (LISA '98), December 6-11. Marriott Hotel, Boston, Massachusetts. Contact USENIX Conference Office, 22672 Lambert Street, Suite 613, Lake Forest, California 92630; (714) 588-8649; (714) 588-9706; e-mail: conference@usenix.org; Internet: http://www.usenix.org.

GET GUARANTEED RS-485 LOGIC 1 OUTPUT DURING OPEN CIRCUIT: CUT 10Mbps POWER 3 TIMES!

New MAX3089 Allows Selectable Full/Half-Duplex Operation!

Maxim's new MAX3080–MAX3089 family are the first ICs that meet both RS-485 receiver specifications and provide a fail-safe output, guaranteeing a logic 1 during a short circuit or open circuit. The MAX3086's supply current is 600μA maximum—3 times lower than the closest competing 10Mbps device.

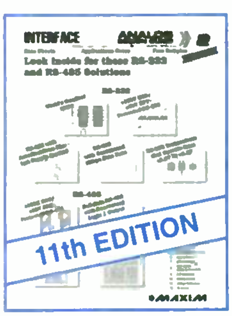
FAIL-SAFE OUTPUT GUARANTEES LOGIC 1 DURING SHORT OR OPEN CIRCUIT



Select the Ideal Fail-Safe RS-485 IC for Your Design

PART	HALF/FULL DUPLEX	DATA RATE (Mbps)	SLEW-RATE LIMITED	LOW-POWER SHUTDOWN	RECEIVER/ DRIVER ENABLE	QUIESCENT CURRENT (μA)	TRANSCEIVERS ON BUS	PIN COUNT	INDUSTRY-STANDARD PINOUT
MAX3080	Full	0.115	Yes	Yes	Yes	375	256	14	75180
MAX3081	Full	0.115	Yes	No	No	375	256	8	75179
MAX3082	Half	0.115	Yes	Yes	Yes	375	256	8	75176
MAX3083	Full	0.5	Yes	Yes	Yes	375	256	14	75180
MAX3084	Full	0.5	Yes	No	No	375	256	8	75179
MAX3085	Half	0.5	Yes	Yes	Yes	375	256	8	75176
MAX3086	Full	10	No	Yes	Yes	375	256	14	75180
MAX3087	Full	10	No	No	No	375	256	8	75179
MAX3088	Half	10	No	Yes	Yes	375	256	8	75176
MAX3089	Selectable	Selectable	Selectable	Yes	Yes	375	256	14	75180*

* Pin compatible with 75180, with additional features implemented using pins 1, 6, 8, and 13.



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Circle No. 150 - For U.S. Response
Circle No. 151 - For International

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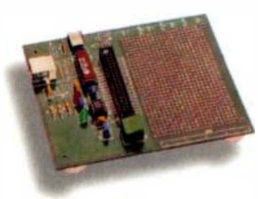
CY3650	Low-Speed USB Development System	CY7C630XX CY7C631XX CY7C632XX	$495
CY3640	USB Starter Kit	CY7C630XX CY7C631XX CY7C632XX	$99



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BOB PEASE

Bob's Mailbox

Hi, Bob:

A couple of things I have learned that make working with copper-clad boards much easier are the use of a hot-air soldering tool, and a good pair (sharp point) of tweezers for stripping the foil from the fiberglass substrate. Also, the pc-board prototype routing machines you see in a number of electronic publications are an excellent tool for doing almost any kind of work with copper-clad board—from cutting shaped pc-board pieces, to elaborate double-sided prototypes made for TSOP and SSOP devices.

The routing machine that I use (LPKF) will allow you to use a pointed-tip milling tool to quickly cut very-fine lines through the copper foil. It's much neater and faster than the X-acto knife I have used in the past. The hot-air soldering tool can be used to remove unwanted foil after all the routing and drilling is complete. A drill tool will drill holes, and a second milling tool will cut through the pc board.

Since the routing machine is basically a specialized plotter, controlling it is fairly simple. It came with fairly good software, but I find it easier to export files from the CAD tool I am familiar with in HPGL format. Making multiples of a board is a simple cut-and-paste operation, and making a duplicate board at a later date only requires loading a file. The L-shaped box you mentioned in your article would take about 15 minutes to layout, export, and rout. Two L-shaped boxes would take 16 minutes.

BOB LUTES
Design Engineer
M-tron Industries
Yankton, S.D.

Maybe 15 minutes for <u>you</u>. But 15 weeks for me to learn to drive that computer without crashing. Fortunately big SHEARS, tin-snips, and metal-nibblers still work well—RAP

Dear Bob:

New EE grads are a source of both enthusiasm and comic relief (providing there's not a schedule to meet). Most are of the opinion that "there are 'digital' electronics and 'analog' electronics." Their various instructors never take time to warn them that "there's no such thing as 'digital'—just funny-looking analog with more or less two common states."

Two things have become more common over the years. First, EE students are actually encouraged to treat digital circuits as ideal circuits, ignoring the analog component. Especially at the frequencies we're using today for these components, more circuits do not work as expected. Ah! too bad the world wasn't really a pile of capacitive and inductive elements.

The second problem seems to be in the selection of passive components. Is it my imagination, or are nearly all EE students leaving school with naiveté that nominal value plus tolerance is all that matters? Why has it never dawned on them to ask why there are different materials available for resistors and capacitors? Using other than a ceramic capacitor seems to be thought of not as a possible design need, but a fashion statement <sigh>.

I recently ran across the *Passive Electronic Component Handbook* by Charles Harper, $89.50, available from: *http://www.books.mcgraw-hill.com* Where are texts like this being used in EE courses?

CHRIS ANDERSON
via e-mail

There's also a book by Ian Sinclair on Passive Components, about $30, ISBN 07506 02295, with good insights. But no school is going to use anything practical like THAT in any course. Are they?—RAP

All for now. / Comments invited!
RAP / Robert A. Pease / Engineer
rap@webteam.nsc.com—or:

Mail Stop D2597A
National Semiconductor
P.O. Box 58090
Santa Clara, CA 95052-8090

Hardwired FPGA Lowers System Manufacturing Cost

The XH3 series of hardwired FPGA replacements allows designers of FPGA-based systems to lower manufacturing costs once the configuration pattern is solidified. They consist of area-efficient replacements that contain a sea-of-gates core and the Xilinx-specific I/O ring, JTAG support, and logic to emulate the FPGA configuration modes built into the base silicon. The hardwired chips also support the unique features of the popular XC4000 and XC5000 FPGAs. Based on 0.5-µm, 5-V CMOS technology, the XH3 devices are fully PCI-compatible. Six devices, with capacities ranging from 15,000 to 225,000 gates and 112 to 352 I/O pads, will initially be included in the XH3 family. This will enable designers to convert even the highest-density XC4000EX designs into lower-cost hardwired alternatives.

Designers at the company feel they have solved the incompatibility problems typically associated with conventional ASIC replacement of FPGAs. This was done by providing a seamless path in which logic redesign, re-verification, and regeneration of test vectors are eliminated. All logic blocks and signal nets are maintained, as are their relative position on the chip versus the SRAM-based FGPAs

A 50-kgate equivalent to the Xilinx XC4036EX FPGA, the XH304, sells for just $6.50 apiece in lots of 250,000 units. Nonrecurring engineering charges start at $19,000, and lead times for conversion and prototype build are five to six weeks for typical designs. DB

Xilinx Inc., 2100 Logic Dr., San Jose, CA 95124-3400; Chuck Fox, (408) 559-7778; http://www.xilinx.com.
CIRCLE 460

Programmable System Chip Trims Active Power By 89%

Targeted at low-power system designs, the ZPSD211R⇓a 5-V programmable MCU support chip⇓ trims the operating power by 80% versus a standalone 5-V EPROM while integrating additional functions on the chip. Therefore, the ZPSD211R offers on-chip resources that include 32 kbytes of EPROM, a programmable address decoder, a simple PLD, extra I/O ports, and several security features. It also contains a programmable interface that can tie the chip to any 8-bit microcontroller, such as that offered by Intel, Motorola, Philips, and others.

As a result, in an 80C31-based system with an MCU clock of 6 MHz, the ZPSD211R consumes just 1.32 mA. In contrast, a 5-V solution that consists of just an EPROM draws more than four times the operating current, while a fully-fleshed out EPROM solution would draw about 12 mA—almost an order of magnitude higher.

On standby, the chip requires only 20 µA, which is about a tenth the amount required by a multicomponent approach. The chips can be configured with the company's low-cost development tools ($99) or with the regular more-advanced tool set. The ZPSD211R comes in either commercial or industrial temperature-grade versions. The 70-ns, 8-bit 5-V ZPSD211R comes in 44-lead PLCCs and TQFP plastic packages and sells for $2.19 apiece in lots of 100,000 units. DB

WSI Inc., 47280 Kato Rd., Fremont, CA 94538; David Raun, (510) 656-5400; web: http://www.wsitd.com.
CIRCLE 461

Free HDL Software Eases Programmable Logic Design

Available at no extra charge, hardware description language (HDL) synthesis will be included in the next release of the MAX+PLUS II development software (Version 8.1). The "HDL for free" strategy will enable designers to take advantage of the increasing densities of PLDs by adding powerful synthesis tools to every desktop. Users can choose to specify either VHDL or Verilog as their HDL language, and can easily obtain the necessary authorization code through the World Wide Web.

The software is available to the over 10,000 existing tool users under maintenance contract, and will be included for all future purchasers of the MAX+PLUS II software. Altera links its web site to an internal database so that customers with valid maintenance contracts can quickly access new features.

As part of the MAX+PLUS II release (version 8.1), the company also has introduced a mid-range tool configuration called the Based Development System, which includes design entry through HDL or schematic entry. The tool suite, which sells for $995, also includes timing analysis, functional simulation, floorplan editing, LPM support, on-line help, and compilation support for Altera devices of less than 10,000 gates. DB

Altera Corp., 101 Innovation Dr., San Jose, CA 95134; Bob Beachler, (408) 544-7000; http://www.altera.com.
CIRCLE 462

Price Parity Lets Designers Use Either GALs Or ispGALs

Readjusted prices have created price parity between the previously more expensive ispGAL22V10 in-system programmable GAL and the standard GAL22V10. As a result, the 1000-piece price of the isp version now matches the GAL22V10 prices for the 7.5-, 10-, and 15-ns speed grades. The ispGAL22V10 is the only low-density PLD to support the in-system programmability, and with the pricing parity, it promises to open up many applications to ispGALs.

The ispGALs come in the same 28-lead PLCC package option that houses the standard GAL22V10s, and with the same data-sheet specifications as the standard device. The four no-connect pins on the GAL22V10's PLCC package are used for the four ISP interface signals. The isp devices can be in-system programmed using a PC or a workstation during development, or through a configuration connector or embedded controller on the target system. Programmer support is available from many programmer manufacturers; design software is available from the company in the form of the ISP Synario System and ISP Synario Starter Software. More advanced packages from Lattice, Data I/O, Logical Devices, Minc, Orcad, ISDATA Omation, and others provide designers with most, if not all, of what they need to complete a design. Respective prices for the 7.5-, 10-, and 15-ns ispGAL and GAL devices are $5.90, $3.20, and $2.70 each in 1000-unit quantities. Delivery is from stock. DB

Lattice Semiconductor Corp., 5555 Northeast Moore Court, Hillsboro, OR 97124-6421; Steve Stark, (503) 681-0118; http://www.latticesemi.com.
CIRCLE 463

Mil-Grade SRAM Packs 1 Mbit, Accesses In 15 ns

Estimated to be the fastest military-grade 1-Mbit SRAM available, a monolithic 1-Mbit memory fabricated by Cypress Semiconductor on its

RAM3 process, can provide access times of as little as 15 ns. The device conforms to the standard microcircuit drawing (SMD) specification 5962-89598, and is immune to alpha particles thanks to its six-transistor memory cell structure. The low-power chip consumes only 10 mA during standby and just 1 mA at 2 V when in its lowest-power data-retention mode. In addition, the memory is radiation-tolerant and can withstand up to 20,000 rad (Si), thus making the chip well suited for applications in avionics, radar, sonar, and communications systems. The 1-Mbit SRAM is in volume production and comes in 32-contact LCCs or 32-pin DIPs, with speed grades ranging from 15 to 120 ns. Prices start at $49.50 each in lots of 100. DB

Cypress Semiconductor Corp., 3901 N. First Street, San Jose, CA 95134-1599; Jim Townsend, (408) 943-2600; http://www.cypress.com. **CIRCLE 464**

PCI Target Chip Meets Proposed PCI 2.2 Spec

A target-only single-chip PCI interface, the S5920, is designed to comply with both the current PCI 2.1 specification and the proposed PCI 2.2 standard. The chip also is software-compatible with the company's previous S5933 interface circuit. This allows customers to replace the chip with a lower-cost target-only solution for applications that don't require the bus-mastering features.

The S5920 controller provides the interface between the PCI bus and various synchronous and asynchronous systems that have 8-, 16-, or 32-bit local-bus connections of up to 40 MHz. PCI bus operation at speeds of up to 33 MHz are supported and the chip can transfer data at the full bus bandwidth of 132 Mbytes/s. An integrated 32-byte bidirectional FIFO buffer memory allows the chip to support zero-wait-state burst operation or offer programmable wait states (0 to 7 states).

For mailbox support, a direct Add-On mailbox data strobe pin was included, along with 8-, 16-, and 32-bit PCI Add-On mailbox registers with byte-level status registers and mailbox read/write interrupts. Four definable memory block pass-through regions support one to four local-bus address range decodes.

Complementing the S5920 is the company's Matchmaker controller development kit, which provides a proven reference platform for prototyping. In OEM quantities, the 160-lead PQFP-housed S5920 sells for $15. DB

Applied Micro Circuits Corp., 6195 Lusk Blvd., San Diego, CA 92121; Anil Bedi, (619) 450-9333; or on the web at http://www.amcc.com. **CIRCLE 465**

512k-by-16 EDO DRAM Transfers Data At 83 MHz

Organized as 512 kwords by 16 bits, the V53C818H high-speed DRAM with extended-data-out capability can sustain a data-transfer rate of 83 MHz. The 12-ns EDO cycle time and 30-ns row-address-

strobe (RAS) access time allow the DRAM to serve in digital-video-disk subsystems, graphics frame buffers, and peripherals such as laser printers, etc. A pair of V53C818H's can replace four 256k-by-16 DRAMs and trim system cost by about 15% while reducing component count. The short access times of the EDO memories can significantly reduce host-processor data manipulation overhead. That's because the processor may not need as many wait states as were needed with slower (60 ns) 512k-by-32 DRAMs. The V53C818H comes housed in either 40-lead, 400-mil SOJ packages, or 40-/44- lead, 400-mil TSOP II-style packages. It's available in RAS-access speed grades starting at 30 ns and increasing in 5-ns steps to 50 ns—that corresponds to EDO cycle times of 12, 14, 15, 17, and 19 ns, respectively. The 30-ns RAS speed grade draws 230 mA from a 5-V supply during EDO page-mode operation; on CMOS standby it draws just 2 mA. Both fast-page-mode and 3.3-V versions also are available. In lots of 1000 units, the EDO V53C818H prices start at $6.25 apiece. Delivery is from stock. DB

Mosel Vitelic, 3910 North First St., San Jose, CA 95134-1501; Rajit Shah, (408) 433-6000, or on the web at http://www.moselvitelic.com. **CIRCLE 466**

FPGA Library Adds Reed-Solomon, FFT/DFT Cores

Both encode and decode cores for Reed-Solomon error handling are now available for use on the Xilinx XC4000-series of field-programmable gate arrays. The cores provide the full functionality of a general Reed-Solomon decoder or encoder and all of the necessary interface circuitry. The cores are part of the company's AllianceCore program and are sold and directly supported by Integrated Silicon Systems Ltd., Belfast, Northern Ireland. The parametrized design of the cores allows designers to rapidly configure them for a wide variety of applications—digital video, satellite broadcast, and data storage, for example.

Additional cores that perform fast Fourier and discrete Fourier transforms, developed with Rice Electronics, Florissant, Mo., perform FFT and DFT transforms twice as fast as any processor-based design currently available—as little as 30 µs for a 1024-point FFT. Multiple channels can be instantiated in a single FPGA, allowing designers to create filter banks with minimal logic. The FFT and DFT cores are available as part of the Xilinx design library, but the Reed-Solomon cores must be licensed from ISS. They can be contacted at (44) 1-232-664-664, or via e-mail at *info@iss-dsp.com*. DB

Xilinx Inc., 2100 Logic Dr., San Jose, CA 95124-3400; Rich Sevcik, (408) 559-7778; or on the Internet at: http://www.xilinx.com./products/logicore/tblcores/htm. **CIRCLE 467**

Video Line Drivers Offer Performance Plus

A family of dual and triple op amps and programmable buffers developed by National Semiconductor combines high speed, high output current, and low power consumption for video and high-speed data-transmission applications. The devices have buffer-driven, common-emitter outputs that source or sink up to 130 mA and drive a low-impedance load to within 1.0 V of either supply rail. Supply current is as low as 1.6 mA/channel.

The dual drivers are for applications that involve driving video signals through twisted-pair cabling and for signal-boosting tasks such as driving transformers. The triples are suitable for driving RGB video through coaxial cable. The family of duals includes two dual op amps (CLC5602 and CLC5622) and two programmable buffers (CLC5612 and CLC5632). The family of triples includes one triple op amp (CLC5623) and a triple programmable buffer (CLC5633). All devices operate from either a single +5-V or dual 5-V supply. The line drivers also qualify for use in communications systems, residential broadband systems, digital video and instrumentation.

Packaging options for the industrial temperature range are plastic DIP, MSOP, and SOIC. Unit prices in quantities of 1000 range from $1.79 for the CLC5602 and CLC5612 to $2.23 for the CLC5623 and CLC565633. ML

National Semiconductor Corp., *4899 Wheaton Dr., Fort Collins, CO 80525-9483; http://www.national.com.*

CIRCLE 468

Current-Mode Amplifiers Use Little Power

A family of wideband, current-mode amplifiers designed by Maxim Integrated Products offer the right mix of performance parameters for high-speed video applications. Differential gain and phase errors are 0.08%/0.03°, 0.1% settling time is 20 ns, and slew rate is 400 V/µs. Available in single, dual, and quad versions, the amplifiers operate on a single 5-V supply or dual supplies in the range of ±2.25 V to ±5.5 V. They draw 1 mA per amplifier and deliver output currents up to ±60 mA.

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WINNING COMBINATION

An Unbeatable Team for Your Real-Time Embedded Design.

It's an unsurpassed combination: Motorola's broad line of microcontrollers. Plus Motorola's real-time operating system—developed specifically for the 68HC12, 68HC16, 68300, MPC500, and MPC800 Families.

And now for the 68HC11, too! Big news. Motorola's real-time operating system can now be used for embedded design on one of the most widely used microcontrollers out there.

The RTEK™ kernel. Our optimized kernel can help you use Motorola microcontrollers in winning ways. The RTEK kernel delivers maximum performance with minimum size. It's a field-proven operating system with an easy-to-use C language interface, plus it supports both static and dynamic kernel objects.

With a new feature: scalability. The RTEK kernel is fully scalable for most Motorola microcontrollers, such as the 68HC11, 68HC12, 68HC16, and 68300 Families. That can greatly reduce program memory requirements, and decrease your system and component costs.

Faster time-to-market. The RTEK kernel is designed to help reduce code development and test time. It features more than 190 kernel services that provide task, memory and interrupt management, event synchronization, data movement, and exclusive accesses. Three separate scheduling methods are supported—pre-emptive, time-sliced, and round robin. The RTEK kernel can be used with confidence because it reflects the same commitment to quality found in Motorola's microcontrollers.

Call today for a free demo kit. And find out all that the RTEK kernel can do for you. Just dial (800) 262-5486 ext. 963 today for more information and to order the free demo copy of the RTEK kernel. Or, visit our web site at http://www.mcu.motsps.com to see our full product portfolio.

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WRH

(continued from page 114)

Compensated for applications with closed-loop gains of +2 (6 dB) or greater, the MAX4180, MAX4182, MAX4183, and MAX4186 provide a –3-dB bandwidth of 245 MHz (1-kΩ load resistance) and a 0.1-dB bandwidth of 90 MHz. The MAX4181, MAX4184, MAX4185, and MAX4187 are compensated for gains of +1 (0 dB) or greater and provide a –3-dB bandwidth of 270 MHz (1-kΩ load resistance) and a 0.1-dB bandwidth of 60 MHz. For multiplexing applications, the MAX4180, MAX4181, MAX4183, and MAX4185 have a low-power shutdown mode that lowers power-supply current to 120 µA maximum and places the outputs in a high-impedance state. Unit pricing starts at $1.80 for quantities of 1000. Packing options are SO, SO-23, and QSOP. ML

Maxim Integrated Products, 120 San Gabriel Dr., Sunnyvale, CA 94086; (408) 737-7600. **CIRCLE 469**

Hot-Swap Controller Manages Comm Ports

Operating at from –3 V to –15 V, the UCC3920 is a programmable hot-swap power manager intended for –12-V hot-plugging applications (such as Ethernet and AUI ports), as well as backplane modules. The device has a programmable active-current limit of 0 to 3 A and includes a power FET. For power-management and circuit-breaker functions, the only external components needed are a fault capacitor and a power-supply bypass capacitor. Other features include unidirectional current flow, low-power sleep mode, programmable start delay, fault-current level, maximum output sourcing (up to 4 A), and maximum fault time. In the event of a constant fault, the internal fixed 2% duty-cycle ratio limits average output power. Package options are 16-pin DIL and SOIC. Unit pricing in quantities of 1000 is $2.95. ML

Unitrode Corp., 7 Continental Blvd., Merrimack, NH 03054-0399; (603) 424-2410. **CIRCLE 470**

Adjustable-Output Linear Regulators Boast Speed

Three novel adjustable-output linear regulators exhibit typical transient-response times of 1 ns or less for powering low-voltage processors and I/O cores, actively terminating GTL buses, and post-regulating switching power-supply outputs. The CS-5207A, CS-5208, and CS-5210 provide 7 A, 8 A, and 10 A, respectively. Minimum dropout voltage is 1.0 V (1.25 V maximum) at 7 A for the CS-5207A, 1.1 V (1.30 V maximum) at 8 A for the CS-5208, and 1.20 V (1.40 V maximum) at 10 A for the CS-5210.

The CS-5207A is pin-compatible with the LT1584 family of linear regulators. Each regulator has an adjustable output that's set by an external resistive divider. The voltage of the CS-5208 and CS-5210 can be set between 1.25 and 4.5 V, and the output range for the CS-5207A is from 1.25 and 5.0 V. Output voltage is regulated to 1% accuracy. All devices contain short-circuit protection, current limiting, and thermal-shutdown features. Packaged in a 3-lead plastic TO-220 with a heat-sink mounting tab, the regulators are priced at $2.53 each in quantities of 10,000. ML

Cherry Semiconductor Corp., 2000 South County Trail, East Greenwich, RI 02818; 800-272-3601. **CIRCLE 471**

Dual Op Amp Comes Housed In An SOT-23

A dual op amp designed by Burr-Brown, housed in a package one-quarter the size of the conventional SO-8, targets low-cost miniature applications. The OPA2337 in an SOT-23 package combines low bias current, high speed, and a rail-to-rail output swing with a quiescent supply current of only 450 µA per channel. The input common-mode range includes ground, qualifying the device for many single-supply circuit configurations. Supplies in the range of 2.5 to 5.5 V can be used. Each channel operates at speeds up to 1.5 MHz with a slew rate of 1 V/µs. Typical applications include battery-powered instruments, photodiode preamplifiers, medical instruments, test equipment, audio systems, ADC drivers, and consumer products. Operating temperature range is –40 to +85°C. Pricing per channel is $0.19 in production quantities. ML

Burr-Brown Corp., 6730 S. Tucson Blvd., Tucson, AZ 85706; (520) 746-1111. **CIRCLE 472**

EDA

Front-End HDL Tools Target Ease Of Use

Two recently released tools, the EALE/HDL and EASE/HDL, are intended to provide easy-to-use affordable HDL front-end solutions. The EALE/HDL textual tool is a syntax sensitive editor for VHDL, Verilog, and C. It incorporates a number of features that make it easier and quicker for the user to write in HDL code. These features include color-coding, keyword templates, and a rich set of synthesis templates. EALE/HDL is a configurable tool with a customized user interface. As such, support for other languages may be added; the user also can create personal templates. The tool contains a Multiple Document Interface on PC and UNIX environments.

The graphical front-end EASE/VHDL tool allows for design entry using bubble diagrams for familiar state machines. Based on VHDL, the tool features constructs like generics and multiple architectures, and offers type checking and reserved word-checking capabilities.

At the heart of the tool lies a design navigator that visualizes design hierarchy and alternatives with the help of multiple architectures and multiple used component instantiations. It accepts VHDL component instantiations that are defined graphically using block diagrams, and VHDL processes entered using process symbols. Handwritten VHDL can be merged with the graphical descriptions to combine graphical control and readability with the textual power of VHDL. In addition, existing designs may be reused by merely importing the VHDL files.

Component instantiations are automatically created. During the tool's operation, users simply enter a database. The tool then generates optimized, readable VHDL code tuned for a variety of synthesis products.

Both the EASE/VHDL and the EALE/HDL tools are available now on PCs running Windows 95 or Windows NT and UNIX platforms. The tools may be purchased as either a node-locked or floating license. Prices start at $595. Complete functional versions can be downloaded from *http://www.translogiccorp.com.* CA

Translogic BV, Galvanistraat 14-1, P.O. Box 620, 6710 BP Ede, The Netherlands; +31 (0)318 64 20 76; e-mail: info@translogic.nl. **CIRCLE 475**

Debug Capability Eases Use Of Verification Tool

The most recent release of the VERA verification system, VERA 3.0, incorporates a source-level debugger and a link to the System Realizer and CoBALT emulators from Quickturn. These features have been added to make the tool easier to use and more effectively able to verify the correct operation of blocks, ASICs, and complete systems faster than previously possible.

The source-level debugger is targeted specifically for VERA-HVL (Hardware Verification Language), a language used for functional validation. VERA-HVL can be employed to create test conditions much more exhaustive and stressful, with less engineering effort, than can be created in a Verilog environment. With the source-level debugger in place, the engineer now can observe and control the various concurrent operations that may be occurring in these testbenches.

With the tight link to Quickturn's emulators, both design and verification engineers can use the exact same VERA testbenches with an emulator, which they previously used for verification with Verilog. As a result, users can easily retarget their testbenches from driving Verilog simulations to driving the same circuit running in an emulator.

VERA 3.0 also offers a host of other new features, including a flexible graphical interface based on the Tcl/Tk script, and the ability to set up breakpoints, see the different parallel contexts, and find out about the status of different threads of execution as a design is being validated. VERA 3.0 supports the Verilog-XL, NC-Verilog, VCS, Frontline, and Speedsim simulators. It's now available on Sun and HP platforms. Floating licenses range in price from $7500 to $27,500, depending on the option purchased. CA

Systems Science, 1860 Embarcadero Rd., Suite 260, Palo Alto, CA 94303; (415) 812 1800; info@systems.com. **CIRCLE 476**

Multiple Pc-Board Solutions Offer Flexibility

Today's pc-board designer requires more flexibility in configuring tool solutions to specifically meet their needs. To create this flexibility, Cadence Design has devised a three-tier pc-board design packaging and pricing solution. The first tier solution is comprised of Allegro PCB—an entry-level solution that allows users designing boards with lower pin and layer counts access to high performance capabilities at a low cost.

The second tier features Allegro Designer, which is targeted at users designing complex and dense pc boards with high layer and pin counts. This particular tool comes bundled with the EditPlace and AutoPlace modules for automatic and auto-interactive placement. The last tier offers the Allegro Expert tool, designed for users designing high-speed pc boards. A special feature of this tool is that designers are able to handle the latest packaging technologies, such as multichip modules, in a technology-independent physical design environment. The Allegro Expert tool comes bundled with the EditRoute and FastCircuit auto-interactive solutions for routing high-speed designs. The three pc-board tier solutions are all based on the same underlying database and user interface.

All of the solutions are available now on either a Windows NT or UNIX platform. The cost is the same regardless of the platform. Allegro PCB, Allegro Designer, and Allegro Expert, respectively, sell for $10,000, $25,000, and $45,000. Each tier configuration may be purchased with optional versions of the AutoRouter, which starts at $3000, or the Concept HDL design capture solution, which starts at $6000. Users can purchase a single license to float between Windows NT and UNIX environments. CA

Cadence Design Systems Inc., 555 River Oaks Parkway, San Jose, CA 95134; (408)-943-1234; Internet: http:// www.cadence.com.
CIRCLE 477

Module Adds To Functionality Of Formal RTL Product Family

The latest addition to the Design Insight formal RTL design tool product family, Multi-Cycle Analyzer (MCA), focuses on formal RTL design for datapath logic. The module, which combines simulation with formal verification, is targeted for use by ASIC and IC engineers needing to validate the functionality of RTL design specifications. The module can be used to validate complex sequential datapaths, such as pipelined arithmetic logic units (ALUs). And, as a symbolic simulator, it allows designers to analyze and prove the correct operation of complex protocol details over many clock cycles.

The MCA module enhances the control logic validation by processing complex initialization sequences. Both values and symbolic equations are propagated through the logic of a design. If logic values are propagated, then the MCA acts basically as a cycle-based simulator by simulating any number of standard vectors to initialize a circuit for analysis. From this starting point, the user then can utilize the logic exploration and model checking features of Design Insight and its state-machine analyzer module.

Symbolic simulation, on the other hand, propagates the entire equation that determines the value of the bit for all input values, and not just a single logic value for each bit. The MCA then can prove that the datapath operates correctly under all conditions by analyzing these equations across a set of registers between a user-selected set of input and output signals.

The MCA module supports both standard VCD and binary textual vector formats for input and output. It's available now as an add-on option for Design Insight and sells for $25,000. CA

Chrysalis Symbolic Design Inc., 101 Billerica Ave., 5 Billerica Park, North Billerica, MA 01862; (508) 436-9909, e-mail: info@chrysalis.com. **CIRCLE 478**

Mechanical/Electrical Pc-Board Link Established

The PowerPCB Pro/ENGINEER Link provides a link between electrical and mechanical computer-aided design (CAD). Developed through a Cooperative Software Partners program (CSP) with Parametric Technology Corporation (PTC), the tool links the Pad's PowerPCB printed-circuit board design tool with PTC's Pro/ENGINEER environment.

The link allows design engineers to model the effects of pc-board component placement decisions against mechanical enclosures and other constraints. Then, placement improvements or changes to the design can be annotated back to PowerPCB from within Pro/ENGINEER. With this ability to backward-design changes, designers can accomplish such tasks as annotating modifications made to the board outline, placement keep outs, and component placements. Subsequently, component placement cycles are shortened dramatically.

The link also provides a package mapping capability that allows users to use a map file to replace pc-board decals with existing, complex-shaped Pro/ENGINEER 3D part library objects for true 3D representation. Other significant features of the link include 3D data passing so designers can automatically pass component height values from PowerPCB to Pro/ENGINEER. As a result, users will be able to initiate modeling without having to develop 3D libraries in the Pro/ENGINEER environment.

Because the link also allows the placing of parts in 3D, design engineers can use Pro/ENGINEER to place components in 3D, thereby minimizing placement iterations on PowerPCB. The PowerPCB-Pro/ENGINEER link is available now, with the caveat that users also have the Pro/ENGINEER Pro/ECAD option. The link is selling for $1995. CA

Pads Software Inc., 165 Forest St., Marlboro, MA 01752; (508) 485-4300.
CIRCLE 479

Latest Version Of Tool Makes HDL Debugging Easier

Early this year, Debussey 3.0, a tool for orchestrating the complete HDL debugging environment, was introduced. Its latest version, Debussey 3.1, takes this base and adds advanced functionality to aid the engineer through the design process. More specifically, Debussey 3.1 is an integrated environment that includes a waveform viewer known as turboWave, a back-annotated RTL source code tracer known as turboTracer, and a hierarchical schematics generator known as turboSchema.
(continued on page 124)

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This latter feature allows for automatic generation of schematics with true hardware meaning.

The tool also enables simultaneous viewing and debugging of source code, schematics, and simulation results. Other major features include the ability to perform post processing of interactive simulation with various simulators; and a synchronized-window environment that links source code, waveform, and schematics display together through drag and drop.

A hierarchical browser/editor provides the design engineer with an intuitive display by spanning the entire source hierarchy, instantly performing traces to any part of the design. And, sync waveform windows allow design engineers to compare different simulation results. Debussey 3.1 includes VHDL and NT capabilities as well as an editing capability in the schematic generator module. A power analysis tool also is included in the package. The tool is compatible with most Verilog simulators and is available now. Contact the company directly for pricing information, ca

Novas Software Inc., *2105 S. Bascom Ave., Suite 140, Campbell, CA 95006; (408) 377-8611; Internet: http://www.novassoft.com.* **CIRCLE 480**

Tool Enables Hardware And Software Co-Verification

Increased complexity of embedded systems and the trend toward shorter product development cycles has pushed the need for hardware/software co-verification design tools. Virtual-CPU (V-CPU) allows designers of embedded systems to analyze and validate the interaction between hardware and software early in the development process, when design options are still available. It provides a virtual CPU as a replacement for the target processor. The tool comes with a software execution environment that is integrated with a logic simulator.

A bus-functional model (BFM) runs in either host-code execution mode in a workstation process or in target-code execution mode within an instruction set simulator (ISS). This improves performance significantly and provides greater ability to observe and control the executing software. The embedded-system software executes as though it were running on the target CPU.

The representation of the embedded-system hardware running in the logic simulator responds to bus cycles as if they were initiated by the target CPU. Once there's an executable description of the software and hardware available, co-verification of the embedded system in question can begin. As the development proceeds, the user can choose to either leave the hardware/software descriptions abstract or make them more detailed. Because the tool will fit into existing development processes, both the hardware and software engineers can continue to design using familiar tools.

The V-CPU co-verification tool is now available for use with embedded systems that use MIPS, PowerPC, Motorola 68K, X86, ARM, and I960 CPUs, as well as the PCI bus. V-CPU also supports co-verification of embedded systems built around other CPUs and buses. The tool sells for $40,000. CA

Simulation Technologies, *2299 Palmer Dr. #202, St. Paul, MN 55112; (612) 631-1858.* **CIRCLE 481**

Tool Boosts Performance And Design Density

The latest release of the XACTstep tool, XACTstep M1, offers digital designers increased design performance and device densities. A host of new features include advanced device-modeling capabilities and place-and-route algorithms, auto-interactive tools that enable a choice between push-button or manually directed design methodologies, and support for standards-based design flows.

With the algorithmic enhancements in place, users can, for example, obtain 25% better performance on the Xilinx XC4000E devices. The optional auto-interactive tools result in shorter compile times. Also, because the tool delivers programmable logic specific high-level flows, users can choose the best methodology for their environment or design.

The XACTstep M1 features a new modular architecture for the rapid delivery of incremental technologies, new features, additional device support for Xilinx FPGA and CPLD solutions, and new software versions. Consequently, releases can be made independently of the tool, making it possible for users to leverage the new release features without having to relearn a new tool.

The XACTstep M1 software tool is now available for PCs running Windows 95 or Windows NT 4.0, and UNIX workstations including Sparc compatible, SunOS 4.1.3 and Solaris 2.3, HP-UX and IBM RS6000. Its selling price ranges from $495 to $5995, depending on device support, computing platform, and software configuration purchased. Current XACTstep 5.2/6.0 users under a support or maintenance plan will receive the upgrade free of charge. CA

Xilinx Inc., *2100 Logic Dr., San Jose, CA 95124; (408) 559-7778; http://www.xilinx.com.* **CIRCLE 482**

Synthesis Tool Automates Library Development

An automatic cell library synthesizer, dubbed SYNSPEC, allows ASIC and semiconductor vendors to provide libraries in a timely fashion, while user can customize their own libraries on the fly to meet specific LSI design requirements. It accomplishes this by automatically generating logic and timing models. Incorporated in the tool is a highly accurate modeling capability. It's based on the use of PWL and table lookup models that take into account input waveform dulling as well as specially developed modeling techniques.

The tool features a reverse logic synthesis capability that can generate gate models from the Spice transistor connection information input. Consequently, logic models can be provided featuring full compatibility with physical elements. Also included are Spice waveform generators, cell logic tests, transparent generation of EDA library/documentations, cell characterization, and a strong graphical user interface (GUI). The models generated by the tool can interface with most EDA vendors tools and library formats. SYNSPEC has a starting price of $150,000. CA

EXD Technologies Inc., *4633 Old Ironsides Rd., Suite 318, Santa Clara, CA 95054; (408) 970 1480.* **CIRCLE 483**

One-Chip Ethernet Hub Has Reference Hardware, Software

The NWK954 is a single-chip, four-port, 10/100Base-TX repeater that's been designed for the extremely price-sensitive SOHO hub market. Its mixed-signal technology allows it to incorporate a complete MAC controller and four PHY-layer interfaces on one chip to reduce component cost and board space. Thanks to this high level of integration, it requires only a single 25-MHz reference clock and a set of standard 1:1 magnetics to form a complete four-port repeater. The device local and backplane extension ports cascades up to six chips and stacks up to 10 groups, for a total of 240 connections. A set of status LED drivers also are incorporated into the chip, allowing it to display port activity, collisions, and hub status.

To expedite the design process, a complete reference design is available. Along with the necessary schematics, pc-board layouts, and component list, the NWK954 reference design includes a full set of Microsoft and Novell-certified software drivers. Compatible with most major platforms, the drivers support interfaces to Windows 95 and NT, as well as several flavors of Novell Netware, including ODI, ODIOS/2, and NDIS 2.01.

Available during the fourth quarter of this year, the NWK954 is packaged in a 128-pin PQFP and costs $29.50, in 1000-piece quantities. LG

GEC Plessey Semiconductors, 1500 Green Hills Rd., Scotts Valley, CA 95067; attn: Tim Mahon, (408) 438-2900; http://www.gpsemi.com.
CIRCLE 484

Gig Ethernet Transceiver Supports Multiple PHYs

Capable of supporting fiber and twinax interfaces, the Am79761 GigaPHY-SD is a physical layer 10-bit transceiver that complies with the latest 802.3z draft standard for Gigabit Ethernet. The device can be deployed in backbone interconnects for Ethernet switches, in switch or repeater uplinks, and in connections between high-performance servers. It performs serializing and deserializing of the 8B/10B 10-bit data between its 10-bit parallel interface and its PHY-layer serial channel. The GigaPHY-SD performs all clock recovery and word synchronization, and uses an internal 125-MHz oscillator to generate a 1.25-GHz clock.

The transceiver can directly drive copper twin-axial cables for short-haul connections of 25 to 35 meters, and can

directly interface to a standard PECL-level optical transceiver to drive 2 to 500 meters of multimode fiber or up to 3 km of single-mode fiber. A reference design for the Am79761 is available now. It includes board layouts, Gerber plots, component lists, and all other information required for the successful first-pass design of a fiber or copper-based Gigabit PHY.

Sampling now, with production volumes later this year, the Am79761 GigaPHY-SD costs $23.50 each in 1000-piece orders. LG

Advanced Micro Devices Inc., One AMD Place, P.O. Box 3453, Sunnyvale, CA 94088-3453; (800) 222-9323, (408) 749-5703, www.amd.com.
CIRCLE 457

CMOS Gigabit Ethernet MAC Available As Chip Or Core

Incorporating both the media-access-control (MAC) and 8B/10B encode/decode functions for Gigabit Ethernet, the VNS67501 V/eNet GEM is available as a standalone product or as an embeddable core for semi-custom applications. The MAC/ENDEC core has a standard 10-bit parallel interface to the PHY layer, and a high-speed 32-bit full-duplex parallel interface for passing data to a host system or switch fabric.

In addition to its basic functions, the core has built-in statistics capture and error processing logic, plus an 8-kbyte FIFO. This provides head-of-line buffering to help moderate traffic flows within large switch fabrics. Further congestion control is provided with embedded logic that can automatically prevent buffer overflow without burdening an external controller. If the buffer exceeds a user-selected threshold, it can cause the MAC to signal the transmitting end to "throttle back" by sending pause frames to the reverse channel, per the IEEE approved protocol.

With a core size of less than 250 µm on a side, the V/eNet GEM can be incorporated into a standard CMOS ASIC, with lots of space available for switch logic, controllers, and custom logic. The next version of the chip and core, anticipated for early next year, will incorporate the full IEEE 802.3z standard feature set, including auto negotiation and CSMA/CD capability. Also available in the first quarter of 1998 will be the VNS67600 V/2PHY, a CMOS Gigabit PHY-layer interface that incorporates serializer/deserializer and clock recovery functions.

Sampling in the fourth quarter of this year, the VNS67501 MAC costs $45 each in quantities of 10,000 pieces. When released next year, the anticipated price for the VNS67600 PHY is $18 each. LG

VLSI Technology Inc., 1109 McKay Dr., San Jose, CA 95131: (408) 434-300; fax (408) 922-5252; http://www.vlsi.com.
CIRCLE 458

Quad Magnetics Modules For 10/100-TX, ATM, FDDI

The PE-69037 and H1001 are fully integrated, four-port, magnetics modules that provide a complete line interface for Ethernet, ATM, and FDDI applications. Intended for use in concentrators, multiport adapters, hubs, and routers, these compact devices have a 1-in. by 1.15-in. footprint and can save board space, design time, and assembly costs. They exceed 802.3u and ANSI X3.236-1995 specifications for 100-Mbit/s Ethernet and 155 Mbit/s ATM transmission. The PE-69037 has common-mode chokes on all transmit channels for increased noise suppression, while the H1001 does not. Available now, the PE-69037 costs $6.60, and the H1001 costs $6 each, when ordered in 10,000-piece lots. LG

Pulse Engineering, 1220 World Trade Center Dr., San Diego, CA 92126; Dave Richkas, (619) 674-8100; fax (619) 674-8202; http://www.pulseeeng.com.
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CONVENTIONAL
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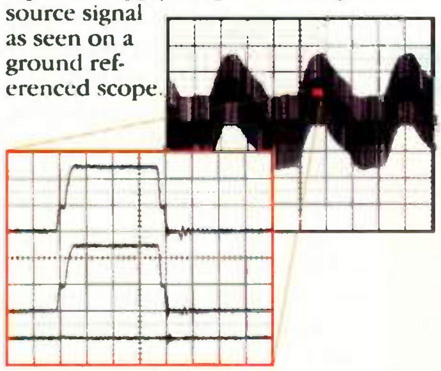

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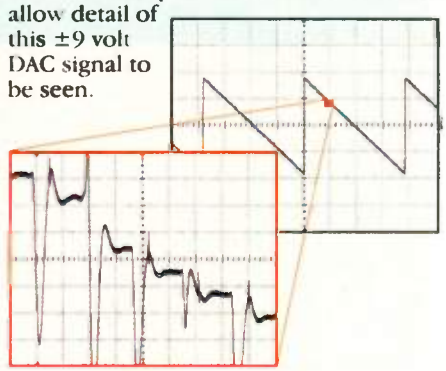
CONVENTIONAL
A scope lacks sufficient position range and lacks the ability to recover from overdrive to allow detail of this ±9 volt DAC signal to be seen.



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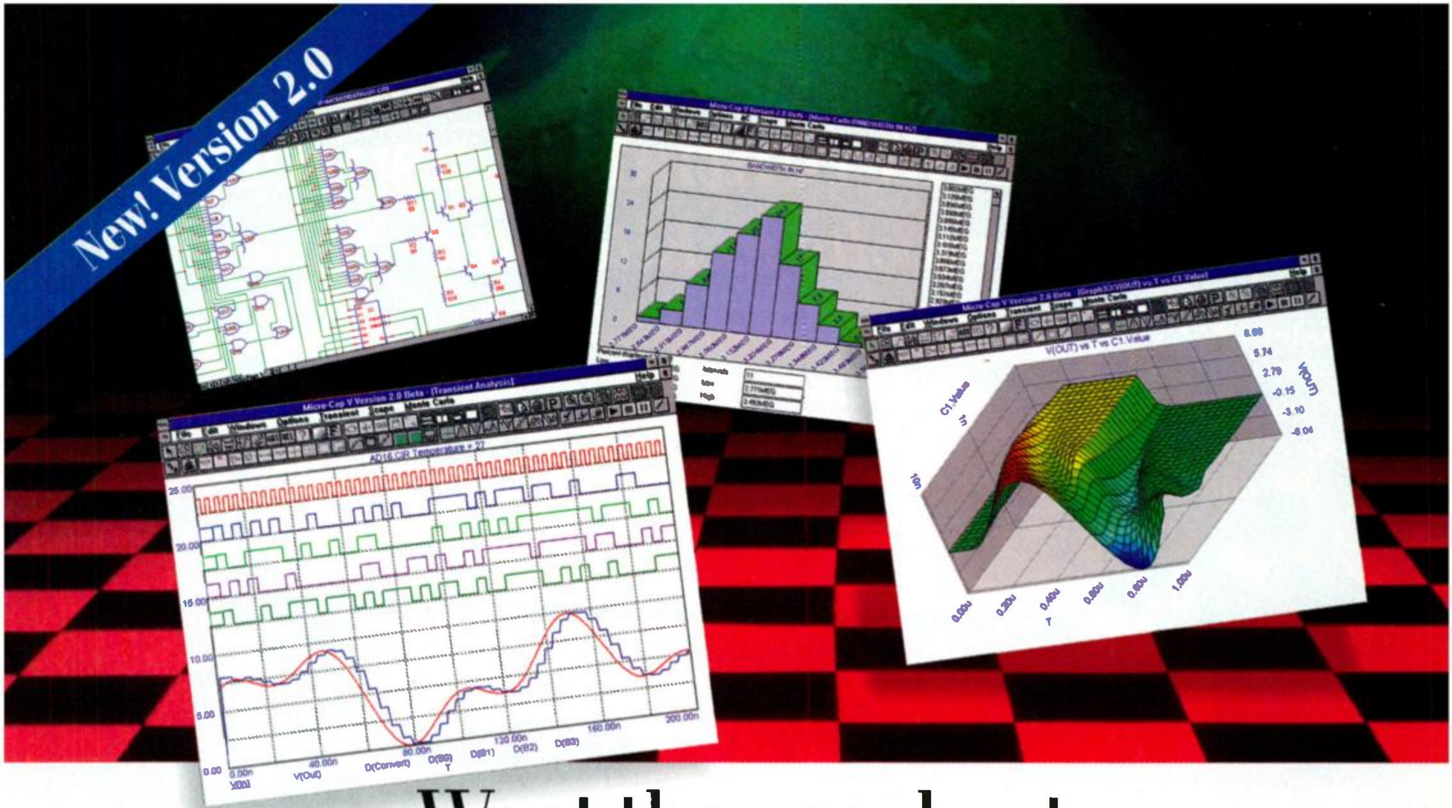

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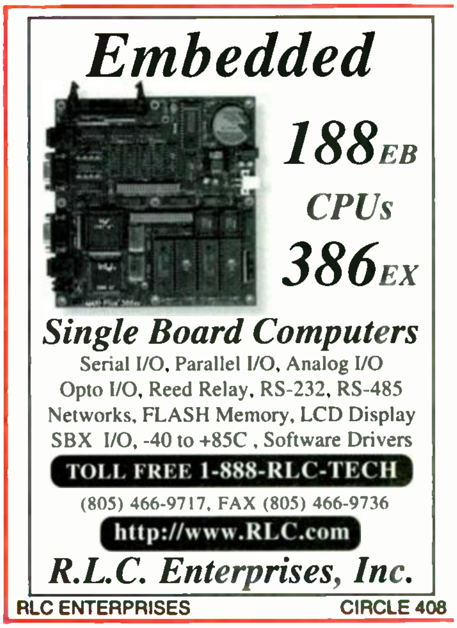
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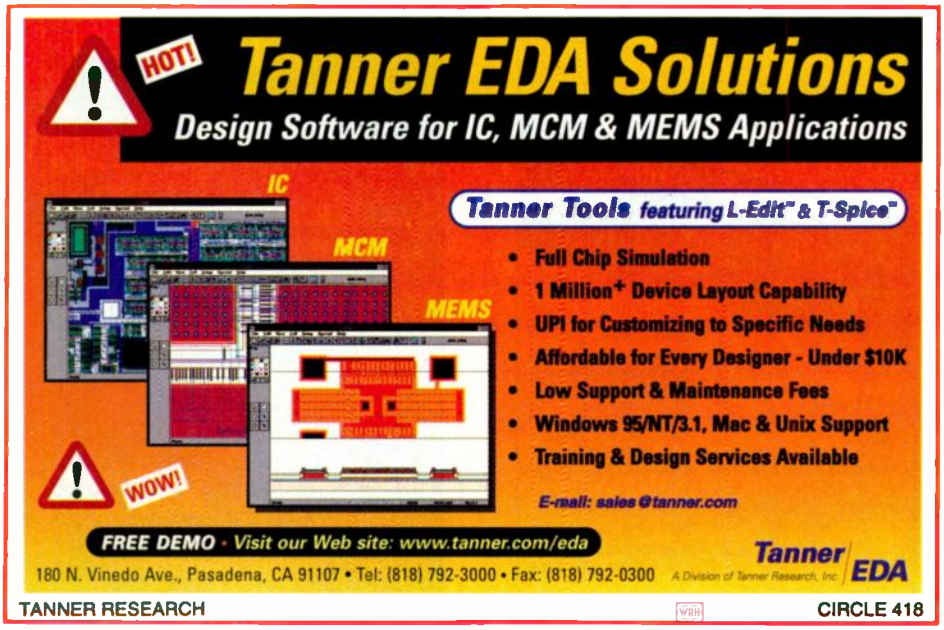
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Febuary 23	1/3/98
March 9	1/27/98
March 23	2/10/98
April 6	2/24/98
April 20	3/10/98
May 1	3/21/98
May 13	4/2/98
May 25	4/14/98
June 8	4/28/98
June 22	5/12/98
July 6	5/26/98
July 20	6/9/98
August 3	6/23/98
August 17	7/7/98
September 1	7/22/98
September 14	8/4/98
October 1	8/21/98
October 12	9/1/98
October 22	9/11/98
November 2	9/22/98
November 16	10/6/98
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December 14	11/3/98

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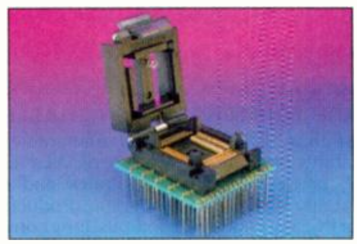

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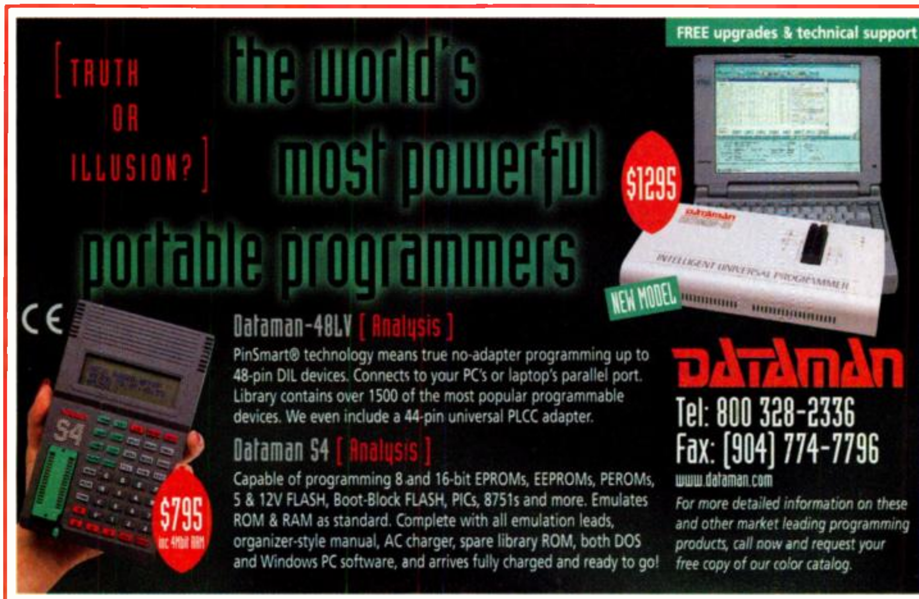

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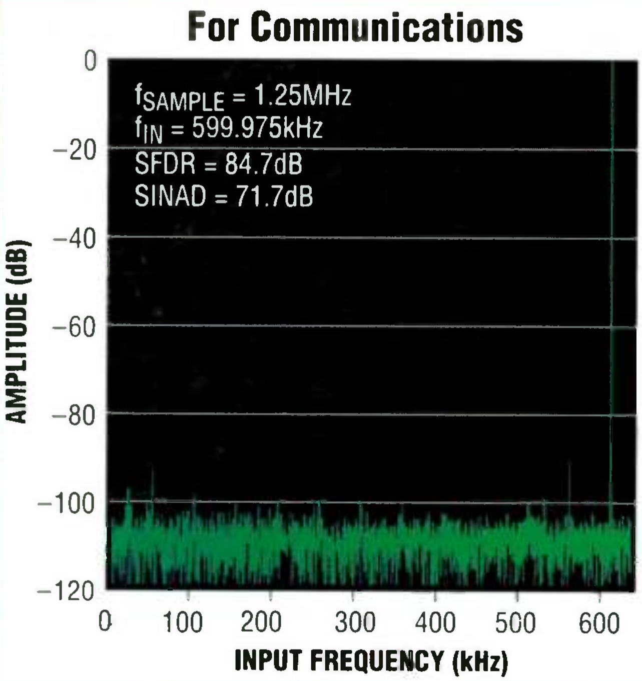

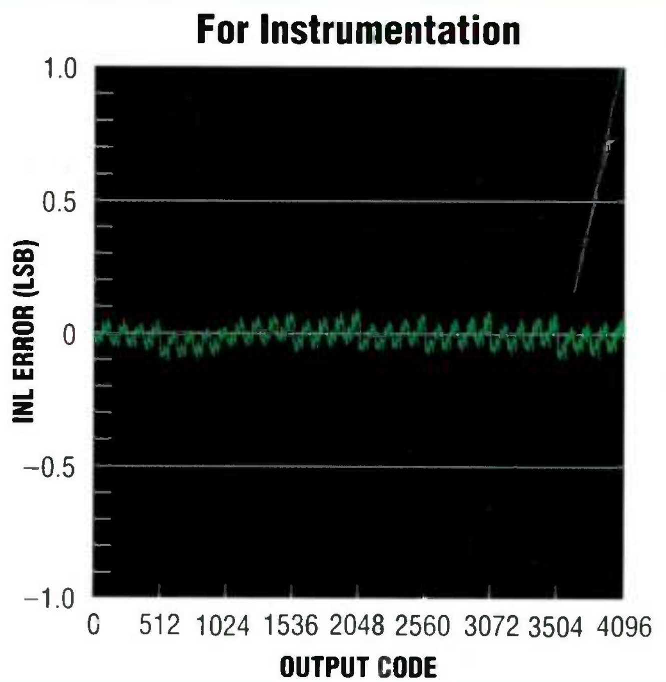

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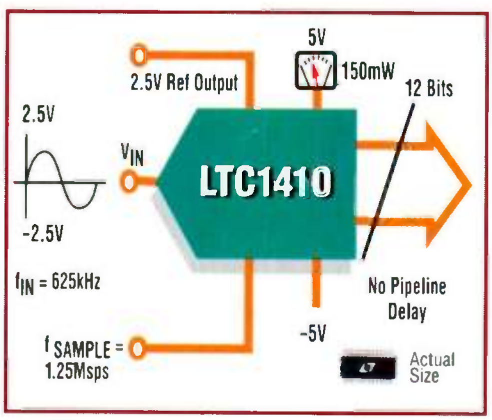

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