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ELECTRONIC DESIGN

TECHNOLOGY · APPLICATIONS · PRODUCTS · SOLUTIONS

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DECEMBER 15, 1997

Double-Poly Process Enables Low-Cost Microwave ICs p. 37

Shift into high gear.

Shift to a new level of performance with Altera's high-speed FLEX 10K-2 devices.

Altera has taken the highest density programmable logic family to the next level of performance. Now you can shift even more of your gate array designs to FLEX® 10K programmable logic.

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Device	Gates	Logic Elements	Embedded RAM	Performance Improvement*	Supply Voltage
EPF10K30A	30,000	1,728	12 Kbits	40%	3.3 V
EPF10K50V	50,000	2,880	20 Kbits	40%	3.3 V
EPF10K70	70,000	3,744	18 Kbits	22%	5.0 V
EPF10K100A	100,000	4,992	24 Kbits	35%	3.3 V
EPF10K130V	130,000	6,656	32 Kbits	38%	3.3 V

*Estimated performance with -2 speed grade using MAX+PLUS II v. 8.1 compared to -3 speed grade using MAX+PLUS II v. 8.0

Setting the pace with low power and packaging options.

FLEX 10K-2 lets you choose 5.0 V or 3.3 V supply voltage and numerous package options to fit your design needs.

Accelerate your design process with MAX+PLUS II.

Our easy-to-use MAX+PLUS II development tools have been optimized for greater design flexibility and seamless compatibility with leading EDA design systems. And, MAX+PLUS II offers compilation times of under 30 minutes for most designs, further speeding the design process.

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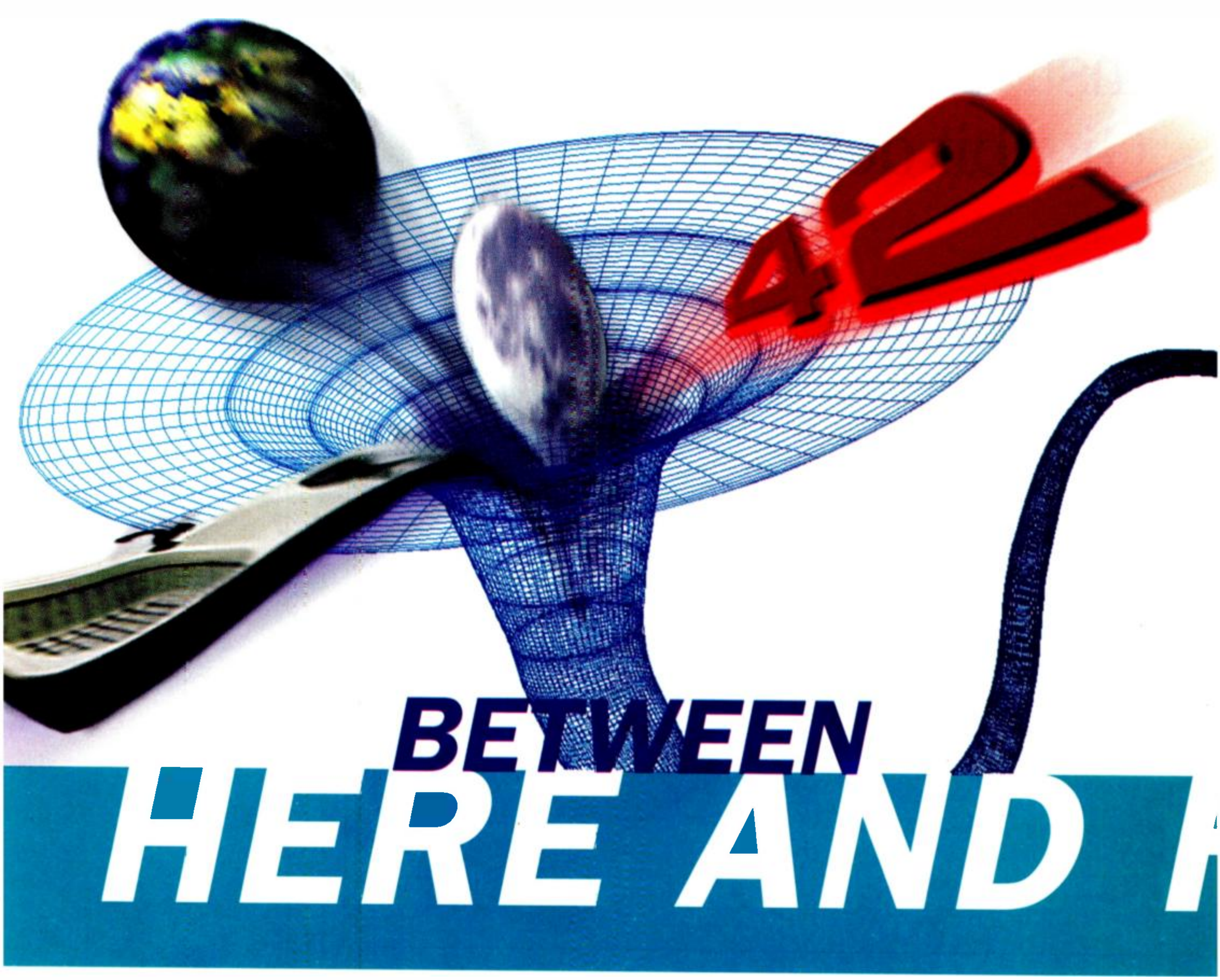

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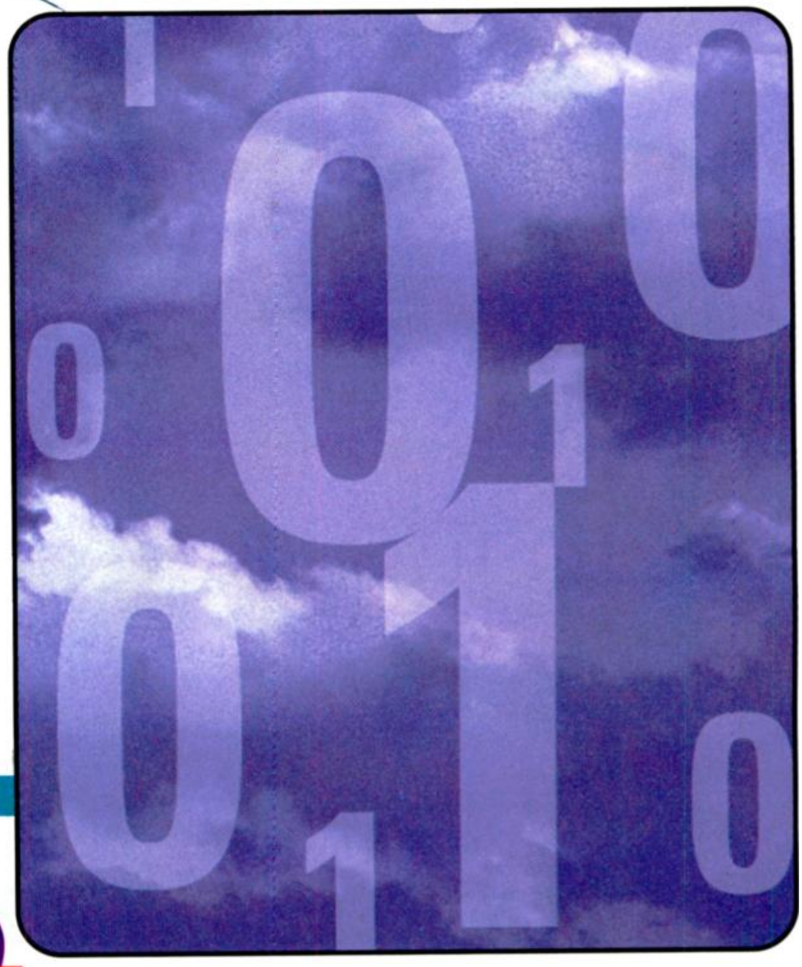

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ELECTRONIC DESIGN

TECHNOLOGY•APPLICATIONS•PRODUCTS•SOLUTIONS

December 15, 1997 Volume 45, Number 28

EDITORIAL OVERVIEW

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ELECTRONIC DESIGN
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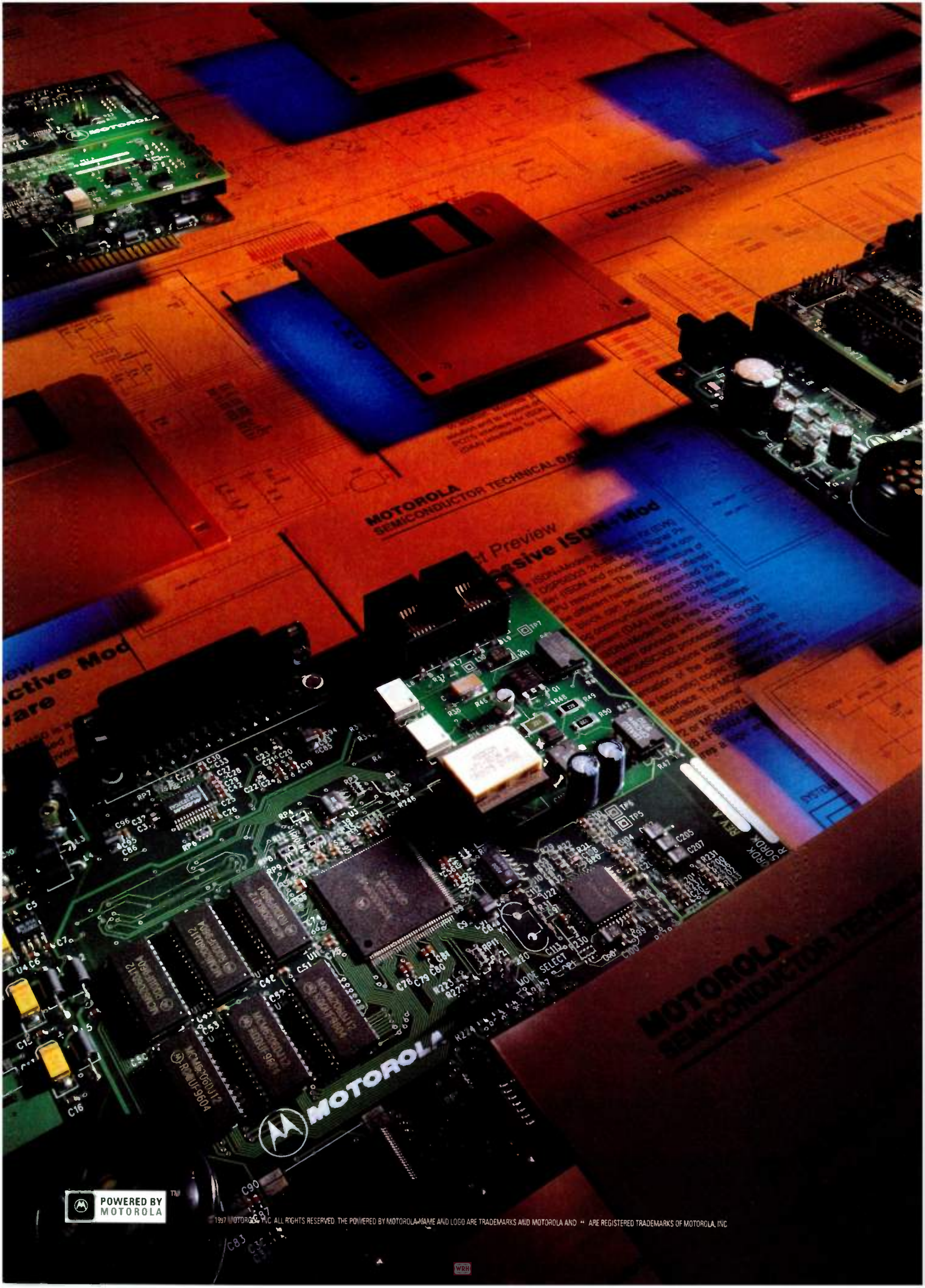
December 15, 1997 Volume 45, Number 28

EDITORIAL OVERVIEW

COVER ILLUSTRATION BY:
MARGARET ENDRES-BANGS

Jesse H. Neal Editorial Achievement

1967 First Place Award	1978 Certificate of Merit
1968 First Place Award	1980 Certificate of Merit
1972 Certificate of Merit	1986 First Place Award
1975 Two Certificates of Merit	1989 Certificate of Merit
1976 Certificate of Merit	1992 Certificate of Merit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MOTOROLA SEMICONDUCTOR TECHNICAL DATA
POWERED BY MOTOROLA

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TECHNOLOGY•APPLICATIONS•PRODUCTS•SOLUTIONS

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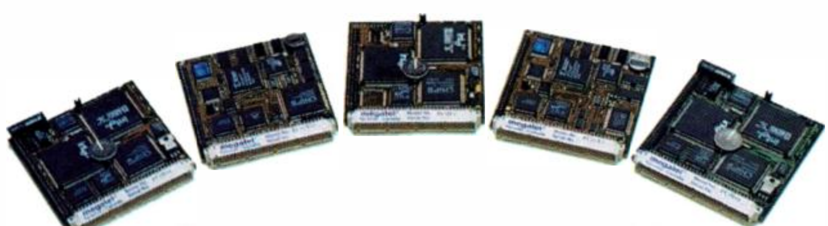

MEETINGS

JANUARY 1998

Seventh Joint Magnetism & Magnetic Materials Conference (INTEMAG), Jan. 6-9. Hyatt Regency Embarcadero Hotel, San Francisco, CA. Contact John Nyenhuis, School of ECE, Purdue Univ., West Lafayette, IN 47907-1285; (317) 494-3524; fax (317) 494-2706; e-mail: smag@ecn.purdue.edu.

Annual Reliability & Maintainability Symposium/Product Quality & Integrity (RAMS), Jan. 20-22. Anaheim Marriott, Anaheim, CA. Contact V.R. Monshaw, Consulting Services, 1768 Lark Lane, Cherry Hill, NJ 08003; (609) 428-2342.

Photonics West, Jan. 24-30. San Jose, CA. Contact The SPIE Exhibits Dept., P.O.Box 10, Bellingham, WA 98227-0010; (360) 676-3290; fax (360) 647-1445; e-mail: exhibits@spie.org.

Seventh Security Symposium, Jan. 26-29. Marriott Hotel, San Antonio, TX. Contact USENIX Conference Office, 22672 Lambert St., Suite 613, Lake Forest, CA 92630; (714) 588-8649; fax (714) 588-9706; e-mail: conference@usenix.org; Internet: http://www.usenix.org.

IEEE Power Engineering Society Winter Meeting, Jan. 31-Feb. 5. Tampa, FL. Contact Jim Howard, Tampa Electric Co., P.O. Box 111, Tampa, FL 33601; (813) 228-4653; fax (813) 228-1333; e-mail: j.howard@ieee.org.

FEBRUARY 1998

Developer's Conference & Interoperability Workshop, Feb. 2-4. Hyatt Regency Hotel & Conference Center, Kauai, Hawaii. Contact Ellen Gooch (212) 226-2042, ext. 228; e-mail: egooch@usar.com.

IEEE International Solid-State Circuits Conference (ISSCC '98), Feb. 5-7. San Francisco Marriott, San Francisco, CA. Contact Diane Suiters, Courtesy Associates, 655 15th St. N.W., Washington, DC 20005; (202) 639-4255; fax (202) 347-6109; e-mail: isscc@courtesyassoc.com.

Portable by Design, Feb. 9-13. Santa Clara Convention Center, Santa Clara, CA. Contact Rich Nass, Electronic Design, 611 Route 46 West, Hasbrouck Heights, NJ 07604; (201) 393-6090; fax (201) 393-0204; e-mail: portable@class.org.

If you use these tools....

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- **102.4 kHz real-time bandwidth**
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My how things have changed. In the 22 years since we first introduced the Power MOSFET family, the concept of sophisticated, portable, electronic devices has evolved from a futuristic vision to a commonplace reality. Through our technological commitment to both silicon and packaging, TEMIC has made the Power MOSFET over 1000 times smaller while dramatically reducing on-resistance. From the first Power MOSFET to the new 32M-cell TrenchFET,

3000mΩ/in²–29W/in²

1975

Siliconix introduced first Power MOSFET

Computers now fit on top of a desk.

70mΩ/in² – 34.5W/in²

1982

Siliconix introduced higher power, more thermal efficient DMOS technology

Portable phones now fit into a suitcase

2mΩ/in² – 57W/in²

1990

Siliconix introduced first LITTLE FOOT® SO-8

Disk drives now fit in portable computers.

1.3mΩ/in²

1994

Siliconix introduced TrenchFET® and LITTLE FOOT TSSOP-8

EDITORIAL

The "M" Word And Other Thoughts

As we close out 1997 and inch ever-closer to the year 2000, you better get accustomed for the forthcoming two-year bombardment of the "M" word from every possible media, marketing, and advertising venue on the planet. No, we're not talking more *M*ichael (Jordan) hype, as he closes out his spectacular career. This is even bigger.

This is about the *Millennium*, a once-every-thousand-year event that has the world abuzz. And there is no doubt that future pop historians will look back at this time span and pay homage to the word millennium as the most infamous and overused buzzword of the 20th Century.

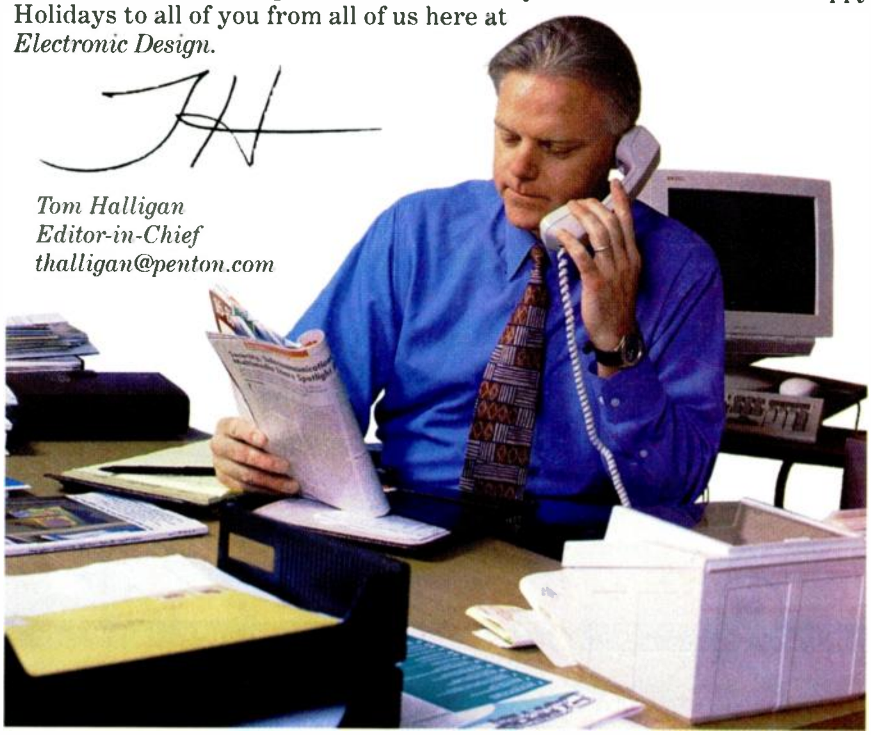
Adding even more hype to the *M word* are the dire warnings concerning the "Year 2000 (Y2K) Problem" or the "Millennium Time Bomb" as it is often called by the general news media. As all of you certainly know, there will be a great deal of angst at 12:01 a.m. on January 1, 2000 for those CEOs and MIS directors who didn't fix or patch their computers' clocks.

The next two years should be quite interesting and (hopefully) a lot of fun as we enter a new era. And if you're a Futurist by trade, you should do well on the talk-show circuit. But, even though our collective attention will be pointed ahead, we should not forget about many of the significant events that have helped us not only to survive on this planet, but to prosper as well.

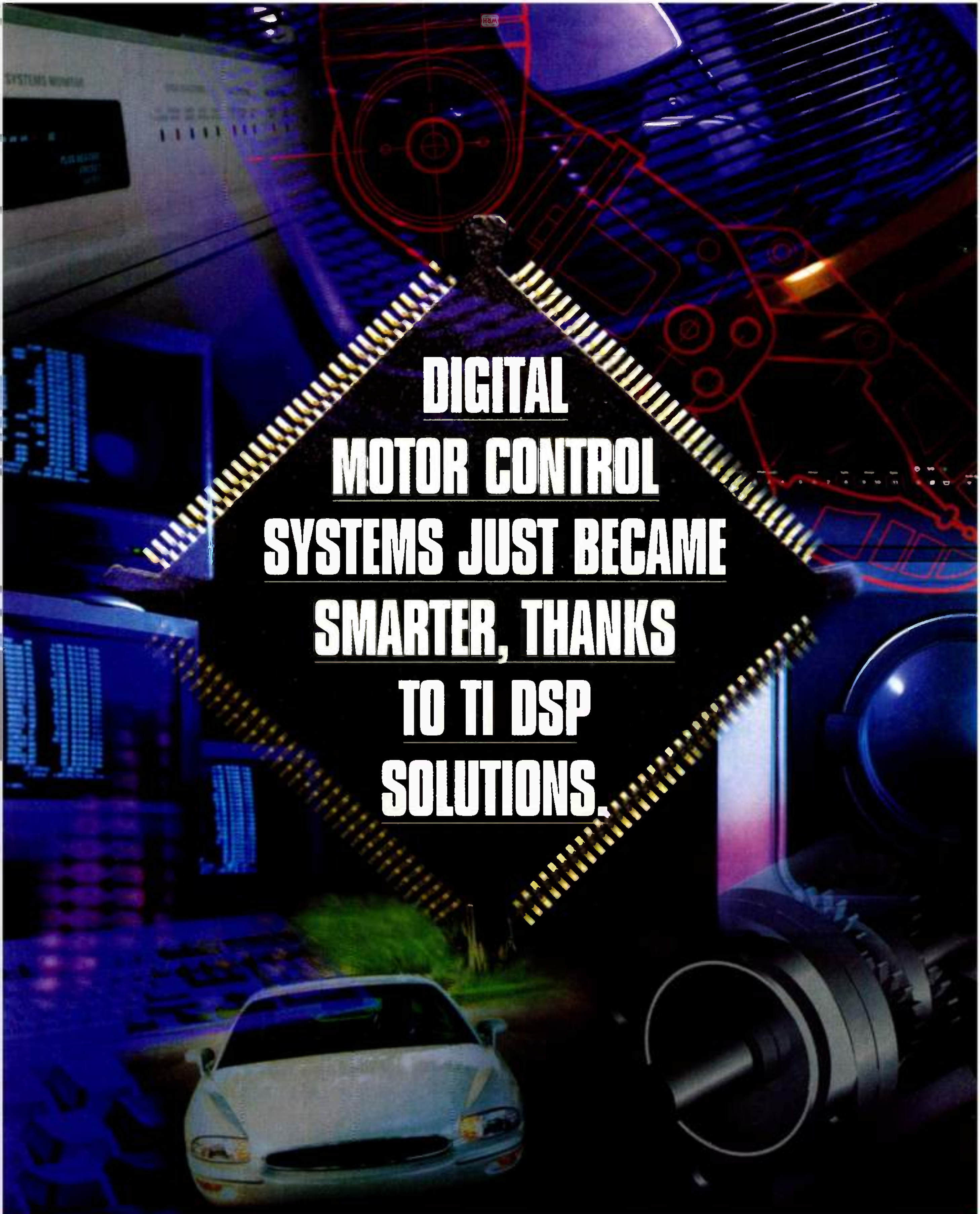
Exactly 50 years ago this month, the transistor was born. And many will argue that no other invention in the history of mankind has impacted or had a direct influence on the majority of people on the planet as this one has.

Our hats are off to Bell Laboratories, Walter Brattain, John Bardeen, William Shockley, and all of the other key Bell scientists who played such a critical role in developing the transistor. The world owes you many thanks.

And stay tuned for *Electronic Design's* annual Technology Forecast Issue scheduled for January 12. We will be focusing on Intellectual Property (IP) issues, featuring several Special Reports and Contributed Articles. We'll be talking about the effects of IP on the design of IC cores, megacells, and ASICs; its role in electronic design automation (EDA) and software tools; and its relationship to test and measurement. Rounding out the issue will be a number of opinions from some of the leading experts in the design community on what IP will mean to the future designer. It's an issue that you can't afford to miss! Happy Holidays to all of you from all of us here at *Electronic Design*.



Tom Halligan
Editor-in-Chief
thalligan@penton.com


DIGITAL
MOTOR CONTROL
SYSTEMS JUST BECAME
SMARTER, THANKS
TO TI DSP
SOLUTIONS.

THE FIRST SINGLE-CHIP DSP CONTROLLER REDUCES OVERALL SYSTEM COST WHILE INCREASING PERFORMANCE.

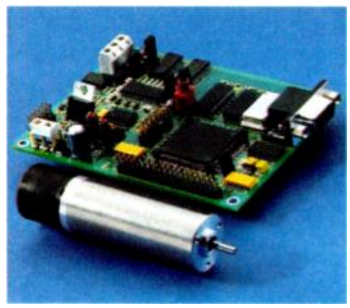
The first DSP controller specially optimized for digital motor control systems, the TMS320C24x, is now available from Texas Instruments. In fact, designing with TI DSP Solutions will give you far greater accuracy, reduced electrical consumption, quieter operation and greater reliability. And allow you to use inexpensive brushless motors in a majority of control applications. In short, you'll be able to increase performance while reducing the total system cost over current 16/32-bit microcontroller-based designs.

The 'C24x DSPs from TI feature a 20-MIPS 16-bit, fixed-point core and integrate a unique event manager supporting up to 12 pulse-width-modulation (PWM) outputs, with PWM and I/O features that include three timers, nine comparators, dead-band generation logic and a state-space vector PWM generator. Also in the event manager are four capture inputs (two of which can serve as direct inputs for optical-encoder quadrature pulses), bringing you all the advantages of DSP with all the needed peripherals.

And now is the perfect time to start designing with DSPs. Texas Instruments, the world leader in DSP Solutions, offers dedicated application notes, a motion control kit (MCK) and world-class development tools including a high-level C compiler. Also available is a 'C24x EVM (Evaluation Module) packaged along with a suite of emulation debugging tools, assembler and linker. In fact, it's the best way to make your digital motor control systems smarter.

TMS320C240 ('F240)

- *20-MIPS core*
- *544 words RAM*
- *16K words flash ('F240)*
- *16K words ROM ('C240)*
- *Dual 10-bit A/D converters*
- *Event manager (for PWM control)*
- *Peripherals (SCI, SPI, 28 I/O pins)*
- *Watchdog timer*



$995 Motion Control Kit

The kit comes with 'F240 board (flash version of 'C240), power inverter, debugger, peripheral program generator, DC brushless motor and operational software for both trapezoidal and sinusoidal modes.

For more information on TI DSP Solutions for digital motor control, call 1-800-477-8924, ext. 4082, or visit us at www.ti.com/sc/4082 on the Internet.

READER SERVICE 161

D S P S O L U T I O N S

TEXAS INSTRUMENTS

It Was A Very Good Year

In anyone's book, 1997 was a banner year for the electronics industry, and the communications sector in particular. This past year has screamed by like a Gigabit Ethernet packet, leaving in its wake a formidable trail of quantum leaps in performance, technical breakthroughs, and paradigm shifts.

This frenzied activity is in part due to an enlightened, business-minded United States Congress that has finally gotten government out of the social engineering business and has allowed market forces to assume a dynamic role in charting the course of our technology. Thanks to a number of forward-thinking legislators like Newt Gingrich, the communication industry is now free of excessive regulation, and is experiencing unparalleled growth. As a result, these efforts have fueled the demand for faster, better, cheaper communication technologies of all sorts.

For example, 56-K modem technologies will soon make high-speed Internet access over plain old telephone service (POTS) lines a reality for most of North America, and soon, much of Europe. Thanks to close cooperation between Lucent, Rockwell, Texas Instruments, and U.S. Robotics, this emerging standard is delivering seamless service and near-ISDN rates for a fraction of the cost of a true digital line. Pretty darn good for a technology that was virtually unheard of until late last year!

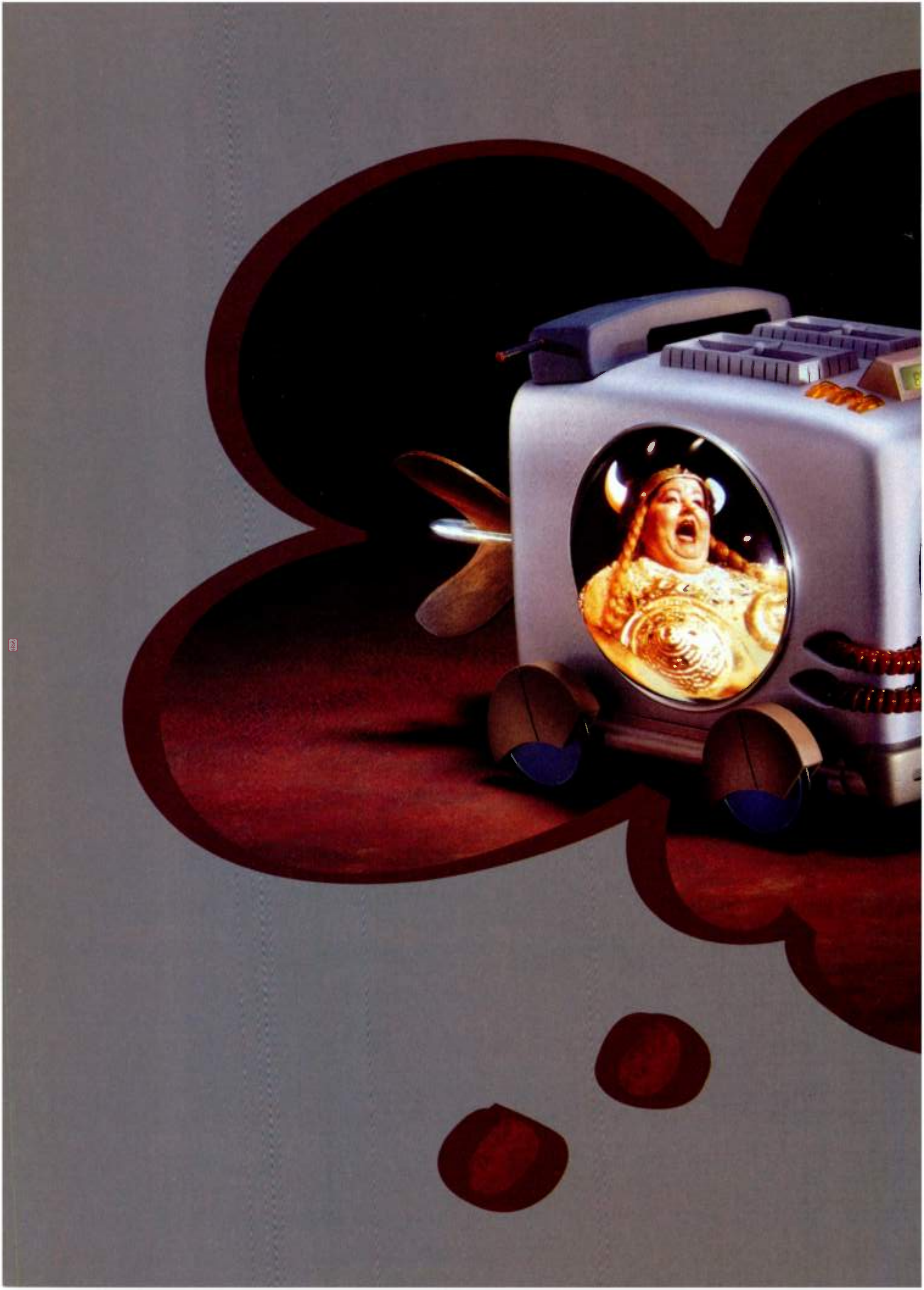

LEE GOLDBERG
COMMUNICATIONS

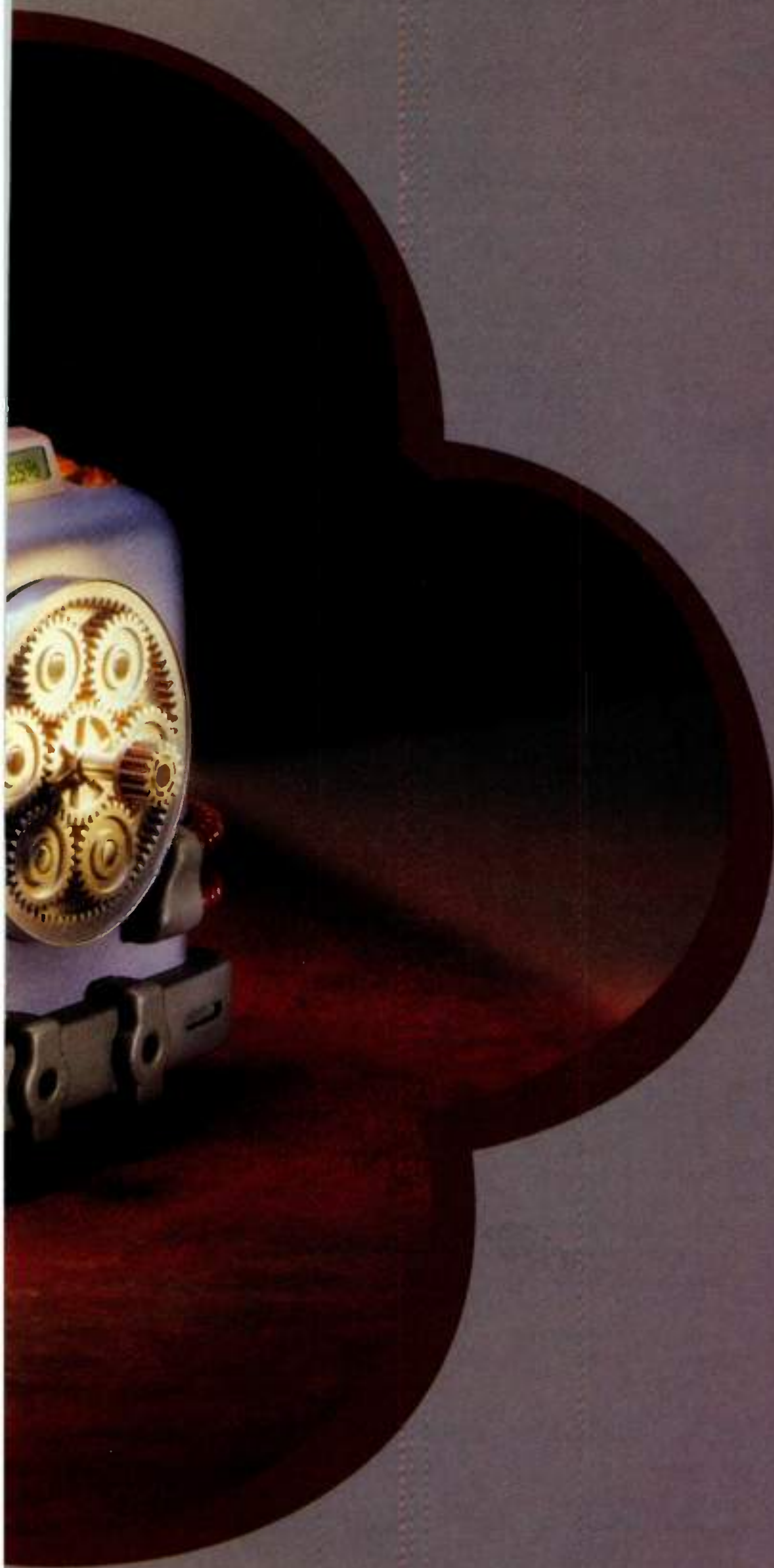
At this time last year, Gigabit Ethernet was merely an exotic concept. Now, it has become a reality, with the IEEE 802.3z committee delivering workable interim specifications quickly enough to see working hardware this year. Now that asynchronous transfer mode (ATM) has lost sole proprietorship of the Gigabit franchise, it will have to compete on a level playing field with the rest of the technologies for a share of the market. This competition should spur manufacturers to drive down the price of chips and, consequently, deliver new and higher levels of performance.

Competitive forces also are producing best-of-breed technologies in the residential broadband arena. Thanks to products that are based on the MCNS/DOCSIS standard, cable modems have taken the early lead in the race to wire America's homes with megabit-class Internet access. Not wanting to be left standing behind in the dust, asymmetric digital subscriber line (ADSL) technology is undergoing a rapid evolution as well. Vendors are now working together to synthesize the right combination of encoding, modulation, and transmission schemes in order to deliver megabit service over ordinary telephone lines. The Baby Bells and local exchange carriers (LECs) also are contributing heavily to a quick roll-out of ADSL by helping competitive LECs deploy the new technology in their particular service areas. The level of cooperation is almost amazing to see.

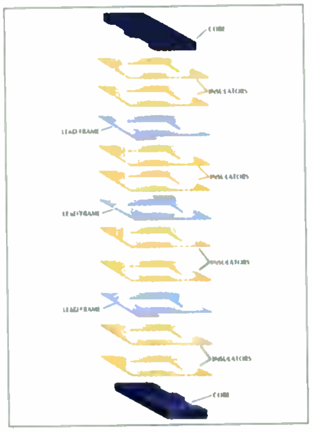
Since communication is so heavily driven by standards activity, it's nice to see Microsoft so heavily involved in paving the way for progress. True Darwinian competition has proven its infallibility as the superior Windows operating system has finally emerged victorious against its competition. The secret to their success? Open systems. By supporting so many communications standards, the Windows-based PC has become a communication platform that is second to none. Everything ranging from videoconferencing and computer telephony integration to megabit-speed Web browsing is supported by the Windows 95 operating system. This ubiquitous platform will increasingly dominate the communications scene, and we will all benefit greatly from it.

With the advent of Microsoft's new and improved version of the Java language, and the imminent release of Windows 98, we can probably expect the same kind of amazing progress in the year to come. It will be interesting to see what will happen in the next 12 months. I can hardly wait. *leeg@class.org*





Planar Transformers Make Smaller Power Supplies A Reality



As the size of electronic products continues to shrink, it's no wonder that more and more designers are choosing planar transformers for switch-mode power supplies in their space-critical applications. Planar transformers don't use big ferrite cores and magnet wire. They're made instead from copper leadframes and flat copper spirals that are etched on thin sheets of dielectric material. The spirals are stacked in flat, high-frequency ferrite cores to form the transformer's magnetic circuit. The result is a transformer with the current densities you like and in a 40 percent smaller space. Efficiency i [illegible] percent at switching frequencies through 500 kHz.

What' more, [illegible] printed circuit board construction allows them to be manufactured with automated assembly equipment, which yields excellent unit-to-unit repeatability. The performance of all transformers within a production run, and from one run to another, is highly uniform, which translates into higher production yield. Planar assembly also minimizes parasitic reactances, so high-frequency ringing in the transformer's output voltage is greatly reduced. Planar transformers achieve excellent primary-to-secondary and secondary-to-secondary dielectric isolation as well.

Planar transformers from Signal Transformer are available in configurations with one, two, or three outputs, four isolated six-turn windings, and four isolated eight-turn windings. The windings can be connected as needed to accommodate a wide range of input voltages. They can be used in power supplies that deliver up to 200 W of DC power at switching frequencies to 1 MHz, and they work with input voltages from 120 VDC to 375 VDC.

For more information about Signal's unique planar transformers, contact Signal Transformer Co., Insilco Technologies Group, 500 Bayview Ave., Inwood, NY 11096-1792, call (516) 239-5777, fax us (516) 239-7208, or send us an e-mail at www.signaltransformer.com **READER SERVICE 185**

Low Profile International Transformers

Feature Industry Standard Pin-to-Pin Compatibility

Signal Transformer Co., Inc. offers a Low Profile International Series that features pin-to-pin compatibility with the existing industry standard for low profile transformers. Designed to meet VDE 0805, the new series offers improved electrical performance, resulting in better regulation efficiency and lower temperature rise; rigid pin construction for easier board insertion and higher reliability; full encapsulation for all wave soldering processes; and mounting holes for greater resistance to shock and vibration.

In addition to VDE standards, the Low Profile International Series transformers comply with UL and CSA standards. They are available in 2VA, 6VA, and 9VA, with output voltages ranging from 50V through 230V.

All stock transformers are available through Signal's PRONTO℠ 24-Hour Shipment Program.

Contact Signal Transformer Co., Insilco Technologies Group, 500 Bayview Ave., Inwood, NY 11096-1792.
Phone: (516) 239-5777; Fax: (516) 239-7208;
http://www.signaltransformer.com

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Multi-Purpose International High-Power Transformers

High Performance with Greater Volumetric Efficiency TUV Certified.

Signal Transformer's Multi-Purpose International Series (MPI) high-power transformers operate from 200 VA to 900 VA and feature higher volumetric efficiency than conventional 50/60 Hz transformers.

Featuring unique coil construction and winding methods, the MPI transformers have exceptionally good isolation of 4000 VRMS Hipot and low leakage current. They also have a 5-mil-thick copper Faraday shield to reduce common mode noise. Fasten/screw-type shock-proof terminals are used on the series.

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READER SERVICE 187

Photonic-Electronic Microchip Takes First Step Toward Reality

Scientists at Columbia University, New York, N.Y., have bonded an ultra-thin sheet of magnetic garnet, a photonic material that transmits light in only one direction, to a semiconductor, a component of microelectric circuitry. This advance could eventually help to create a microchip that combines electronics and its optical equivalent, photonics. Such technology could have a dramatic effect on fiber-optic communications, leading to the development of such miniaturized optical devices a tiny lasers and implantable medical sensors.

A key step in this breakthrough was the ability to slice an ultra-thin sheet—9 µm thick—from the magnetic garnet crystal. Previously, integration between photonic and electronics had not been possible because garnet and other magnetic crystals can't be grown on a semiconductor substrate. Magnetic isolators can't be made efficiently no any material other than magnetic garnets. Consequently, the need arose to place garnet crystals on semiconductors.

The Columbia research team fired high-energy beams of helium ions at a planar region that's just below the surface of the crystalline material—yttrium iron garnet (YIG)—to loosen it from its substrate, gadolinium gallium garnet. Then they applied chemicals to the region to cut the bonds entirely, slicing off an ultra-thin sheet of magnetic material from a single crystal. The sample then was lifted off and bonded to a high-quality semiconductor.

According to Prof. Richard M. Osgood, co-author of the research, the goal of this effort is to make devices that allow light to go in only one direction on a fiber-optic microchip. Light guides etched into the magnetic crystal, when exposed to a magnetic field, allow the light to travel in one direction only, making the light guide an effective routing device in an optic-fiber network. For more information, call (212) 854-5573; fax (212) 678-4817. RE

High-Performance EDA Solutions Sought In Two-Company Project

The gap between the performance capabilities of silicon and the tools that leverage this capability continues to spread further apart. The reason for this chasm is that these tools simply haven't kept pace. Intel Corp., Santa Clara, Calif., and Cadence Design Systems, San Jose, Calif., are now going through with a rather simple plan to close this gap—the two companies will work together on optimizing EDA tools for the Intel architecture workstation platforms.

The first step in this plan will have both companies focus on IA-32-based applications. The next goal will be to understand and respond to user requirements for advanced EDA solutions targeting Intel's future Merced (IA-64) processor. Intel's 64-bit architecture platform is expected to offer greater advantages for performance-critical EDA applications than is currently possible. As a result, the Cadence/Intel relationship will serve to drive development of best-in-class solutions that deliver the optimum power, price/performance, and salability customers will need for next-generation product development.

The two companies will initially focus on optimizing the performance of Cadence's Verilog-XL simulator. To accomplish this, Cadence engineers will work with Intel in a software lab environment to examine, develop, and implement programming code optimizations. Technology from Intel's Application Solution Center will be used to improve operation of the Verilog-XL simulator on Intel architectures. In addition, code implementations will be identified that can take advantage of the multiple pipelines available in the Intel architecture while maintaining a single code stream for both UNIX and Windows NT operating systems. These and other performance-related optimizations are expected to result in as much as a 50% savings in simulation execution time. The two companies also will attempt to develop a product strategy that will allow Cadence's tools to take maximum advantage of the IA-64 processor family. For additional information, go to Cadence's web site at *http://www.cadence.com*. CA

SKYchannel Gains Certification As ANSI Standard

The SKYchannel 320-Mbyte/s 64-bit Packet Bus, developed by SKY Computers Inc., Chelmsford, Mass., has been approved as an ANSI standard (ANSI/VITA 10-1995) for high-performance communication over the VMEbus' P2 connector. Typical SKYchannel applications include image and signal processing for military and medical equipment. The architecture supplies the communications between daughtercards and motherboards, between boards, and between chassis for scalable multiprocessing. Up to 4096 PowerPC, SHARC, or Intel i860 microprocessors can operate together in a Distributed Shared Memory Architecture. And up to 256 VMEbus boards can be connected in one SKYchannel system.

The SKYchannel architecture reduces data-transfer latencies and blocking using deep high-speed FIFO buffers combined with local-node DMA engines and Packet Controllers at every SKYchannel interface. All SKYchannel transfers to the FIFOs are pipelined writes from source to destination, providing a constant and sustained 320-Mbyte/s data-transfer rate. The data rate is sufficient for multiple operations without overloading the communication path. Several transactions can be interleaved without slowing any transfer, allowing full utilization of the bus. Copies of the standard can be found at *http://www.vita.com*. Contact SKY Computers at (508) 250-1920; at *http://www.sky.com*. RN

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Fast Charge IC Selection Guide

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bq2003	NiCd, NiMH, Lead Acid	-ΔV, ΔT/Δt, max. temp., voltage, and time	16/0.300" DIP, 0.300" SOIC
bq2004/E	NiCd, NiMH Lithium-Ion	-ΔV, PVD, ΔT/Δt, max. temp., voltage and time	16/0.300" DIP, 0.150" SOIC
bq2005	NiCd, NiMH	-ΔV, ΔT/Δt, max. temp., voltage, and time	20/0.300" DIP, 0.300" SOIC
bq2007	NiCd, NiMH	-ΔV, PVD, max. temp., voltage, and time	24/0.300" DIP, 0.300" SOIC
bq2031	Lead Acid, Lithium-Ion	Dual-step max. voltage, min. current	16/0.300" DIP, 0.150" SOIC
bq2054	Lithium-Ion	Constant voltage/ minimum current	16/0.300" DIP, 0.150" SOIC
bq2902/3	Rechargeable Alkaline	Maximum voltage	8/14/0.300" DIP, 0.150" SOIC

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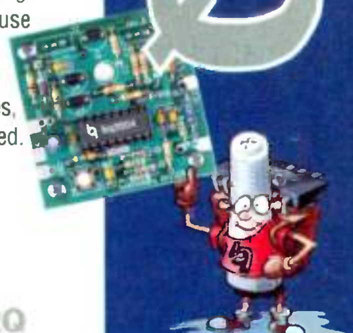

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Centralized Standards Funding Comes To EDA

In a move to create a unified voice for driving EDA standards, the EDA Consortium (EDAC), San Jose, Calif., announced that it will begin directing all standard funds through its organization. This represents a major shift from the way funds are typically dispersed. Currently, a number of different standards bodies exist and they receive funds from a variety of sources. Often times there exists conflicting standards and efforts despite attempts to collaborate. A unified fund dispersal is seen as one way to help bring together today's disparate and incongruous standards. This move also is expected to help eliminate duplicate and overlapping efforts in standards creation and help existing standards bodies focus on solving customer issues.

Under the new business model, the EDA consortium will be responsible for collecting funds for standards from its member companies and distributing them to the various standards organizations. A reporting structure will be established to keep member EDA companies informed as to how their money is being spent and to set metrics for tracking successful completion of goals.

This plan will encompass all major standards bodies, including CFI, ECSI, EDIF, OVI, VI, and VSIA. These standards bodies will benefit from having a single source of EDA funding by gaining more visibility within the EDA Consortium. In exchange, the EDA industry and end users can expect a better return on standards investment, fewer duplicated efforts, and more productivity from engineering resources. For further information on this EDAC effort, contact (408) 287-3322, or check out its web site at *http://www.edac.org*. CA

Allocation Standard To Smooth Operation Between TV And Cable

EIA-745, a recently formulated automatic channel installation standard, defines how television receivers and set-top boxes can be given needed information in the event that a cable operator modifies the allocation established in EIA-542. EIA-542 defines channel allocations for cable-ready TV services. The new standard was created by the Consumer Electronics Manufacturers Association (CEMA), which also issued a Recommended Practice that provides guidance on how the receiver should respond when new channel-allocation information is transmitted.

Using the standard and Recommended Practice, cable operators and TV manufacturers will enhance compatibility between their cable systems and TV receivers by providing a standardized way of numbering modified channel allocations. Cable operators may reassign broadcast channels to different frequencies than were originally broadcast over th air to limit interference and for other operation purposes. With these two documents, cable-ready receivers can "map" or correct their channel read-outs to compensate for these moves. Using the same channel allocations will ultimately enhance cable TV viewing.

For example, EIA-542 assigns channel number 7 to the 175.2625 MHz channel. A cable operator may move programming on channel 7 to channel 27 at 301.2625 MHz. The consumer must know that the "Channel 7 News" is now actually on channel 37 and enter 37 into the remote control. By using formats defined in EIA-745, a cable operator may sound this changed channel allocation via the vertical blinking interval (VBI) line 21, which can then be stored in the receiver's memory. Receivers so equipped may then map the changed allocation so that when channel 7 is entered by the viewer, the receiver will tune to the frequency for channel 37 and the "Channel 7 News" will appear.

EIA-745 and the Recommended Practice can be ordered by calling (800) 854-7179, or by surfing into Global Engineering Documents' web site at *http://www.global.ihs.com*. RE

Projection Display Working Group Is Established

Addressing the rapid growth of the projection display market, the U.S. Display Consortium (USDC), San Jose, Calif., has launched a Projection Display Working Group (PDWG). The group consists of representatives from dpiX (a Xerox company), Electrohome, IBM, InFocus, Proxima, Sarnoff, and Texas Instruments.

The first activity of the PDWG is to issue a request for proposal (RFP) for illumination technologies. Light modulation technologies have been a catalyst in the projection-display boom over the past several years, and there's been quite a bit of activity surrounding the design and manufacture of light modulators for projection applications. Although the light modulators that are currently used vary in size, the trend is toward smaller light valves around one inch in diagonal size. The main purpose of USDC RFP is to stimulate the production of illumination technologies that are well matched to the new light modulators.

Compact lamps, using metal-halide or xenon-arc discharges, provide the light for most of today's projection-display systems. However, such lamps are limited in both light output and lifetime. Further development of these technologies is encouraged by PDWG, but solid-state proposals for application of innovative approaches (e.g., lasers) also are welcomed, provided that a viable commercial product results in three to five years. To obtain a copy or respond to the RFP, or for additional information, contact the USDC at (408) 277-2400, fax: (408) 277-2490. RE

Edited by Roger Engelke

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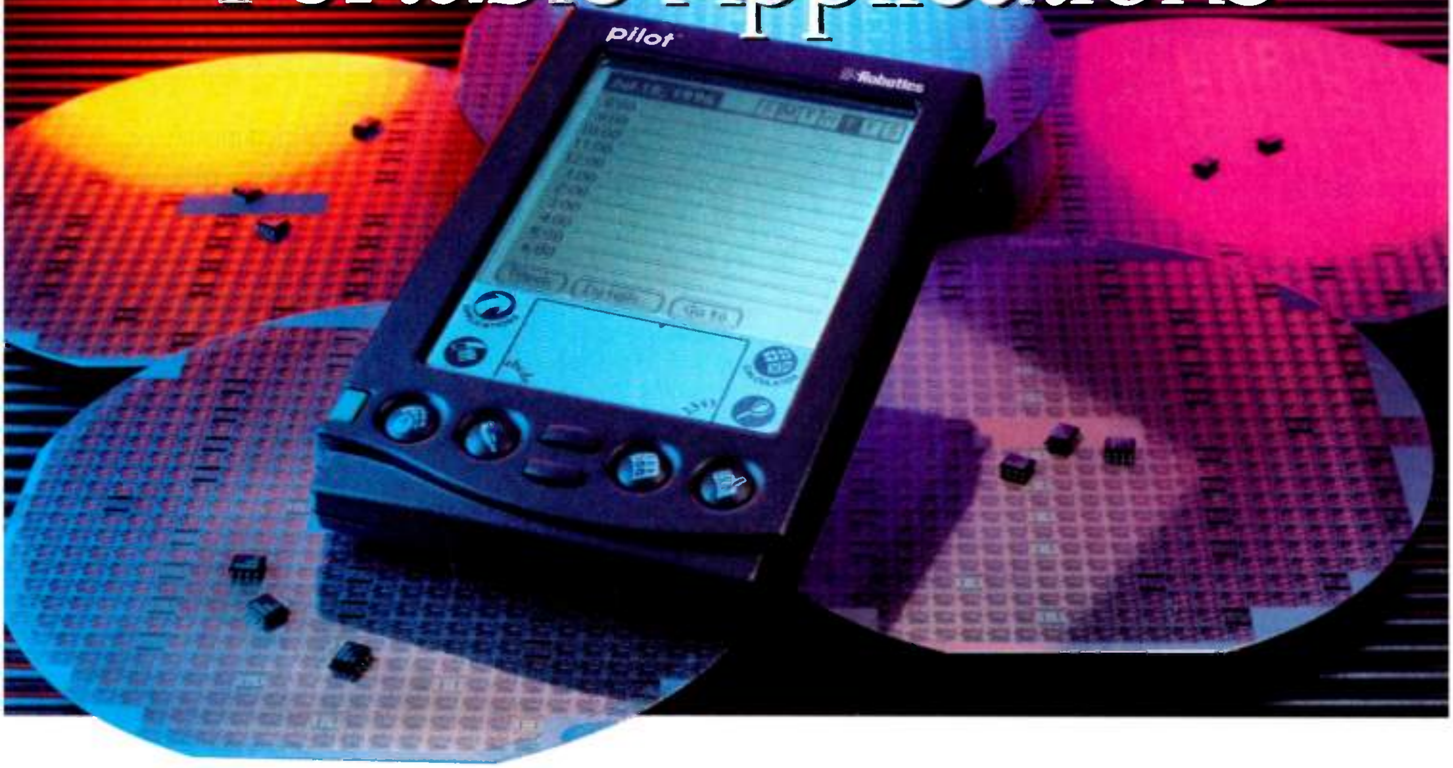

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SP4422A	2.2V to 6V	8mA[1]	•	Requires minimal board space	Remote Control Units, Portable Instruments, POS Terminals, LCD Displays
SP4423	2.2V to 6V	5mA[1]	•	Low Power	PDA's, Calculators, LCD Displays
SP4424	1V to 6V	6mA[2]	•	Dual oscillator for coil and lamp control	Pagers, Digital Watches, LCD Displays
SP4425	1V to 6V	37mA[2]	•	Max light output @ low voltages	Pagers, Cell Phones, LCD Displays
SP4430	1V to 3V	75mA[3]	•	DC/DC converter	Cell Phones, PDA's, Pagers

1. Vdd = 3.0V 2. Vdd = 1.5V 3. Vdd = 1.0V

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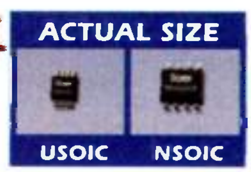

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READER SERVICE 164

Molecular Filter Coating For Sensors Increases Sensitivity Up To 500 Times

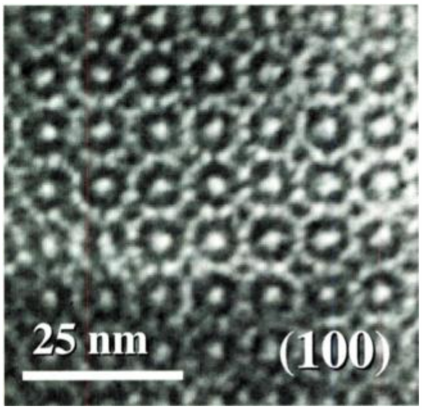
When the condition known as "Gulf War Syndrome" first entered our consciousness after the Persian Gulf War, there was much debate on whether the returning soldiers actually suffered from an illness, or from the effects of participating in conflict. Today, the focus has shifted course, and rests firmly on finding out if the soldiers were exposed to chemical weapons. Had the technology been available at the time, the issue may have been resolved.

Now, a joint effort by researchers at Sandia National Laboratory, Albuquerque, N.M., and the University of New Mexico's National Science Foundation Center for Microengineered Materials, has resulted in a super-sensitive coating, or molecular filter, that can increase a sensor's sensitivity by as much as 500 times. With a thickness of only 1 µm, it causes a negligible increase in the sensor's size.

This ongoing effort, funded by the Department of Energy's (DOE's) Basic Energy Sciences program, also has the potential for use in other applications. Environmental monitoring, for example, is one area where a smaller, more accurate sensor, could definitely come in handy. Oil and pharmaceutical companies, which rely on the use of a molecular separation process to produce grades of gasoline and a variety of drugs, also could benefit from this development.

The concept of using an artificial coating as a molecular filter is not new. In fact, thin films of surfactant (surface-acting molecular) templated mesoporous materials have long been considered for application in membrane-based separations, selective catalysis, and sensors. Most thin films available today, however, are fabricated using a very time-consuming process. These films are granular in nature and have pore channels oriented in a parallel fashion to the substrate surface. As a result, transport across the films is not facilitated by the pores. In effect, molecules entering through the surface are halted at dead ends.

Another difficulty associated with these artificial coatings is that they are not seamless. These coatings are fabricated by allowing gel to dry on sections of substrates. This process results in the formation of fractured borders in the coating that act as a sieve. Consequently, molecules intended for inspection can easily flow through its cracks. Other methods for making the transparent mesoporous films have been proposed but, as of yet, their viability has not been confirmed.



In contrast, what Sandia's researchers sought to produce was a coating with an interior network of tiny tunnels that would allow large numbers of molecules to enter through the surface and exit the base of the film. To accomplish this goal, they developed a new method for creating a virtually seamless artificial coating. This is accomplished by continually removing a substrate from a liquid bath. The artificial coating, in reality a lightweight gel known as a nanocomposite, is formed as water and alcohol evaporate from the substrate's surface. Because the molecules in the gel basically "self-arrange" themselves into what researchers refer to as a "molecular rug," no assembly of gel pieces is required *(see the figure)*.

The unique "self-assemble" characteristic of the gel is due to the two-sided nature of the organic surfactant molecules. The hydrophoic side of the molecule hates water, while the hydrophilic side loves it. When placed in a solution of silica and water, small groups of the organic molecules arrange themselves such that the hydrophilic sides of the molecules face outward in wheel-like shapes forming an ordered array. The hydrophobic sides remain within the circles. The silica in the solution surrounds the hydrophilic sides, attracted by the circular rims of the arrays. The organics of the material can then be removed by a heating process, also known as pyrolysis. The net effect is an inorganic silica fossil with a periodic arrangement of pores where the organics used to be.

Using this method for the rapid synthesis of continuous mesoporous thin films on a solid substrate, the resulting mesoporous films are in a cubic phase. This means that the film's pores are connected in a three-dimensional network that guarantees their accessibility from the film surface. What you end up with is a material filled with tunnels of a particular size capable of separating molecules of differing dimensions; in effect a molecular filter.

This coating is unique in that the size of its pores can be controlled. In fact, researchers can make the pores as large as 100 Å to accommodate a variety of molecules and depending on the molecular makeup of the chemical compound being inspected. By comparison, other types of molecular filters such as zeolites have pores which can never exceed a dimension of 13 Å.

As the principal investigator at Sandia, Jeff Brinker, explains, "The material's extreme porosity increases the sensor's surface area, and therefore sensitivity, by a factor of about 500." As a result, the film-like coating, when used in conjunction with a sensor, can significantly improve the detection of dangerous or potentially lethal air- and water-borne molecules much more quickly then previously possible.

According to the researchers, the extremely high surface area of the film also can be modified to detect chemical weapons. This was demonstrated recently when researchers modified the film and applied it to a sensor. Under laboratory conditions, they successfully detected 200 parts per billion of a Sarin simulant; the same chemical agent used in a terrorist attack in the Tokyo subway. According to Brinker, "At these concentrations, a human being can survive for approximately 50 minutes."

For further information on this development contact Sandia at (505) 844-8066, or see their web site at http:/www.sandia.gov.

Cheryl Ajluni

Hybrid Digital Image Sensor Technology Based On CCD And CMOS Technologies Boasts Low Cost And High Performance

Researchers from the Digital Image Sensor Product Group, Texas Instruments (TI), Dallas, are hoping to help open the door for new PC-imaging applications by providing an alternative to cameras based on CCD and CMOS image sensors. They developed a new digital imaging sensor technology, known as BCMD (Bulk Charge Modulated Device), that combines the best of both CCD and CMOS technologies.

Modern CCD sensors offer a number of benefits, not the least of which is the capability for large production volume and design simplicity. And, since the technology is mature, it's been fully optimized to provide a high level of performance that includes high sensitivity, low dark current, and low noise. However, it does have its disadvantages. CCD sensors often exhibit higher system power and therefore require many power supplies. And, a CCD sensor's architecture makes on-chip system integration difficult at best. Coupled with the technology's inability to output anything besides analog and what you're left with is a technology that has its limitations in the area of emerging PC-imaging applications.

Similarly, CMOS-based image sensors offer a number of benefits including the ability to provide a digital input and output, as well as an on-chip system integration capability. These devices exhibit a lower system power and can operate off either 5- or 3.3-V power supplies. As opposed to the CCD sensor, CMOS sensors are marked by a lower total system cost. But, just like CCD sensors, CMOS image sensors have a number of disadvantages that limit their effectiveness for some PC-imaging applications. For example, the technology has not reached what many would consider to be a level of maturity. As such, it is plagued by some architectural problems and can make design and process optimization difficult. In addition, CMOS-image sensors are known for having a high dark current, low sensitivity, and a high noise level.

TI's BCMD sensor technology eliminates many of these obstacles by leveraging only the best features of each sensor. It is, in fact, a hybrid of the CMOS processes and CCD sensor technology.

One problem BCMD technology addresses is a CMOS image sensor's lack of a well to accumulate charge, which causes low sensitivity. Borrowing from the charge-well design of the CCD image sensor, the BCMD sensor has a buried well on the gate of the device's transistor *(see the figure)*. This significantly improves sensitivity. For example, a BCMD sensor configured into a 1/3-in. VGA device with a 640↔480 resolution and a 7.4↔7.4-µm pixel size features a sensitivity of 78 mV/lux. By comparison, the same device based on a CCD image sensor exhibits 41-mV/lux sensitivity.

This hybrid sensor design also eliminates driving requirements of CCD image sensors, while simultaneously leveraging a CCD's line-addressable nature. Since a BCMD sensor can be fabricated using high-volume CMOS processes, it will offer improved price/performance over existing CCD sensors which are currently made using costly nonstandard fabrication processes.

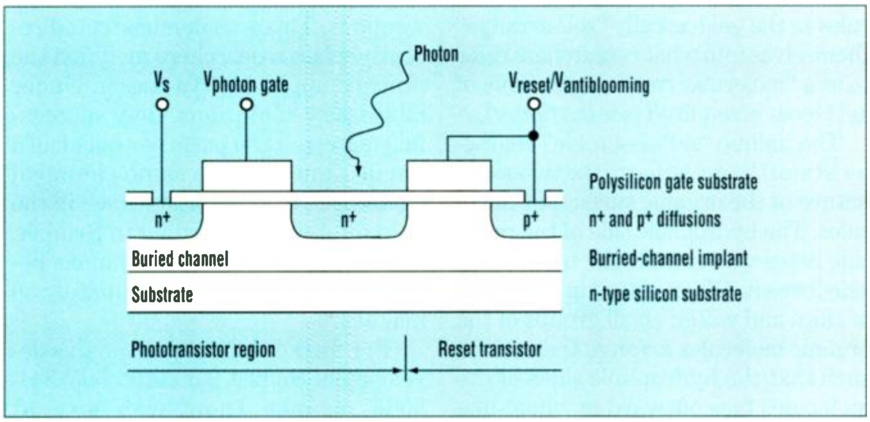
The low cost of the BCMD technology also can be attributed to its ability to enable on-chip systems integration and a simplified power-supply design. TI's researchers do not anticipate any difference in testing and optical quality packaging requirements for the BCMD technology.

Other high-performance capabilities offered by the BCMD sensor include low dark current of less than 5 nA at 50°C and low electrical noise of less than 0.5 mV. The reduction in dark current is attributed to a technique known as surface state pinning. The low-noise capability stems from the use of a correlated-double sampling circuit. This circuit effectively works to suppress pixel fixed pattern noise due to device mismatch and eliminates reset noise. And, sensors based on BCMD technology will provide support for industry-standard 5-V and 3.3-V power sources. This replaces the complicated and expensive range of nonstandard power voltages required by CCDs. TI believes that in using the BCMD sensor, designers of digital and analog cameras can achieve better price/performance ratios, and the cost of digital cameras should become more economical. It is expected that this alone will encourage additional imaging applications for PC users.

Future work on this technology will focus on the development of BCMD sensors that are complementary to digital signal processors (DSPs), mixed-signal products, and ASICs. Other work will center on the integration of all drivers and the analog-to-digital converter on-chip using a single 3.3-V supply. The researchers will also try to integrate digital defect and dark-current nonuniformity corrections circuits on-chip, as well as on-chip integration of image-compression circuits with various processing algorithms. Samples of the BCMD sensor are expected the first quarter of 1998.

More information is available at www.ti.com/sc/docs/msp/disp.htm or call TI's Literature Response Center at (800) 477-8924, ext 4500.

Cheryl Ajluni



Basic structure of a bulk charge modulated device (BCMD) sensor developed by Texas Instruments. The CMOS sensor marries the best of both worlds of CCD sensors and CMOS processing.

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Parallel Processing Approach Using Unique Algorithms Boosts Placement And Routing

Designing ICs today often stretches the performance limits of available EDA tools. As designers begin utilizing deep submicron technologies, defined as 0.35 µm and below, the problem only gets worse. This is because of the difficulties that have arisen from the gap that exists between the performance capabilities with such small silicon-design-rule geometries, and the inability of current EDA tools to take advantage of this situation. Of particular concern is the impact this migration has on the time it takes to place and route (P&R) large designs.

The P&R process is heavily dependent on the number of blocks that need to be placed, the distances between the blocks, and the number and length of the routing paths. These factors all increase as IC feature size shrinks. As a result, the time it takes to place and route a design significantly increases. To combat this growing problem, Gambit Automated Design, San Jose, Calif., developed an approach that combines a series of unique algorithms with the traditional techniques of parallel processing.

The first algorithm, a placement algorithm, is better characterized as a partitioning algorithm because it works by initially breaking a design's logic into pieces hierarchically *(see the figure)*. Subsequently, the pieces are further subdivided. Remaining partitions requiring further partitioning are then handed off to be processed by a number of different processors.

The algorithm structure is based on a common root with a mesh underneath that is able to provide multiple combinations leading to the same solution. During placement, the algorithm searches through a tree, or network of solutions, and if it finds a bad solution, it notifies the other processors not to search in that direction. This approach reduces the area to be searched by more than half, thus shortening the total time required for the placement of large designs.

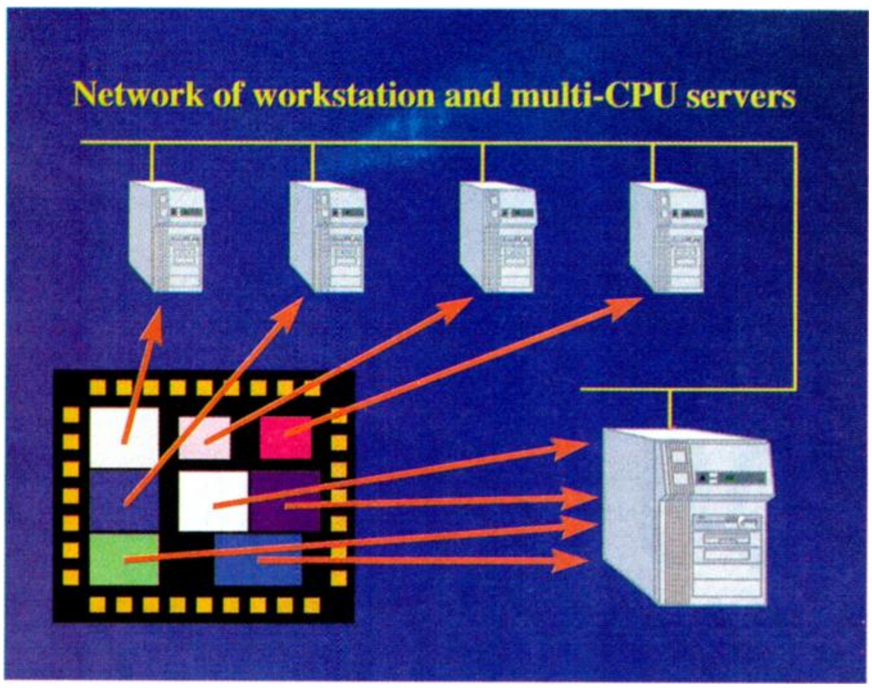
Gambit's routing algorithm is based on a proprietary hybrid process and combines the features offered by channel and line-search routers. During place and route, the algorithm initially routes some of the long runs.

This process can be run concurrently on different machines with each machine routing a different portion of the chip using global routing information. Once this is completed, the routing algorithm takes a second pass, this time incorporating a more standard maze-based solution. Unrouted paths and shorts are identified, then windows are drawn around the areas requiring a fix. The windows serve to isolate the region during routing and contain enough information to complete the route successfully. Each window can accommodate up to a few dozen paths that need fixing. These windows are then handed off to a processor to be completed; each requiring no more than a few minutes to complete. Since the processes are executed in parallel, each process can be relatively small. As a result, feedback from the processes can be provided quickly.

While the key to utilizing Gambit's technology is made possible through the use of Gambit's internally developed algorithms for placement and routing, the success of this approach rests on the use of coarse-grained multiprocessing techniques. Coarse-grained multiprocessing operates over an Ethernet network and does not use a shared-memory model.

The process works by dividing applications into relatively large, independent tasks that can be distributed over a network to a group of workstations. It allows the application itself to implement parallel processing through system calls and the applications programmer to allocate the resources. The speed increase with this process comes from allocating relatively independent parts among several workstations that can be processed simultaneously. The result is a significant increase in throughput. Using four to eight CPUs, for example, yields 2 to 4↔ typical improvement in overall performance. Resulting designs suffer no penalty in die size and timing. Besides the throughput increase, Gambit's technology overcomes one of the largest drawbacks to current P&R solutions: the fact that they operate as a single large process requiring a great deal of memory. Gambit's core P&R algorithms can run across multiple processors and consume less memory per process. In fact, each of the processors requires no more than 128 Mbytes of physical memory. By comparison, routing a large design using a serial routing algorithm may require as much as a gigabyte of memory.

Cheryl Ajluni



Gambit's placement algorithm partitions the logic hierarchically. It then divides the partitioned pieces a second time and hands the pieces off to different processors to work on.

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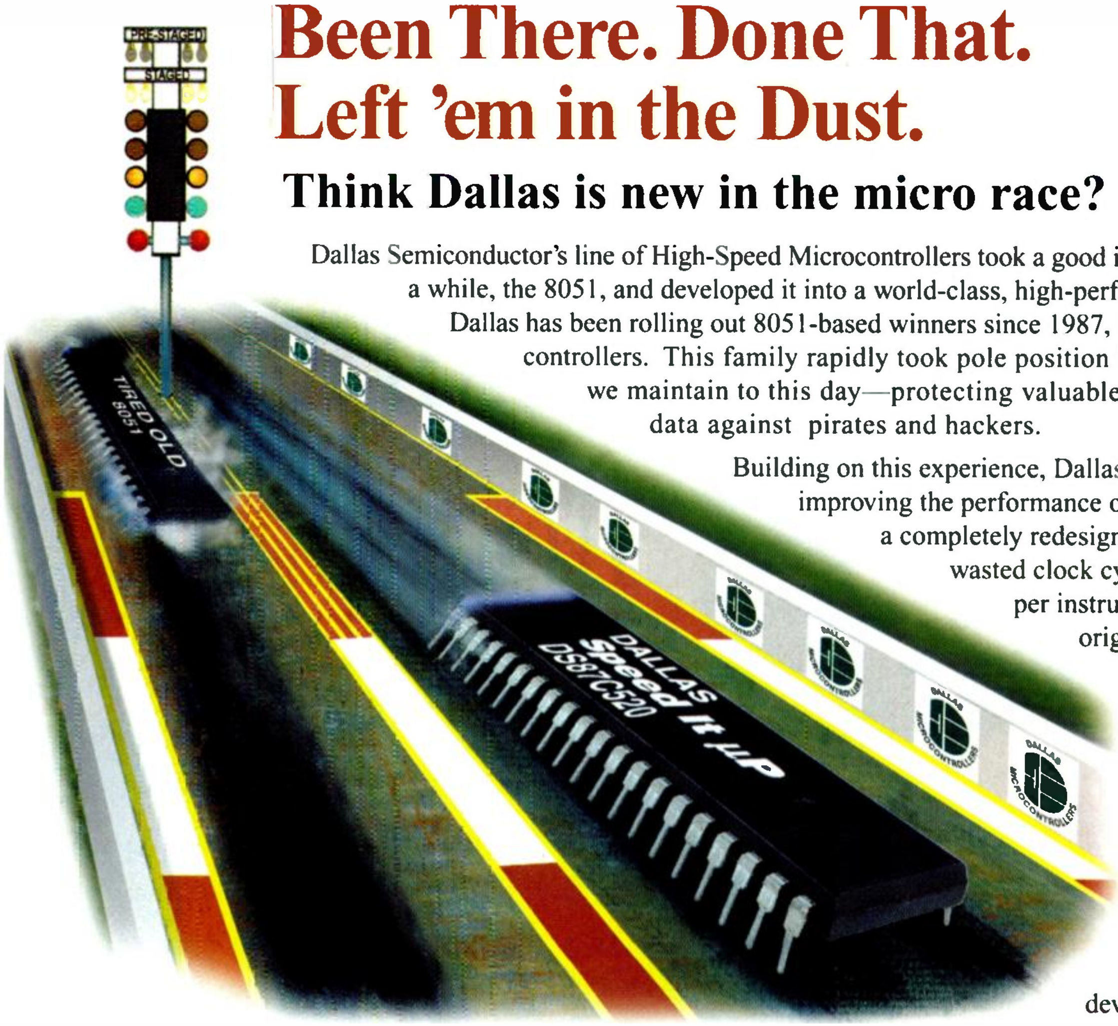

Dallas Semiconductor's line of High-Speed Microcontrollers took a good idea that's been around for a while, the 8051, and developed it into a world-class, high-performance machine. In fact, Dallas has been rolling out 8051-based winners since 1987, starting with Secure Microcontrollers. This family rapidly took pole position in the field—a position we maintain to this day—protecting valuable application software and data against pirates and hackers.

Building on this experience, Dallas turned its attention toward improving the performance of the 8051. The result was a completely redesigned core that eliminates wasted clock cycles. Using only 4 clocks per instruction (compared with the original 8051's 12 clocks), the DS87C520 runs up to a maximum clock speed of 33MHz, providing a performance level equivalent to a 99 MHz 8051. This allows you to turbo-charge your system without costly changes in architecture, software, or development tools.

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READER SERVICE 111

Double-Poly Process Enables Low-Cost Microwave ICs

Bipolar Process Delivers Medium-Power And Small-Signal Transistors With A Cutoff Frequency Of More Than 23 GHz.

Peter Fletcher

COVER FEATURE

Mobile and cordless telephones are the first targeted applications for a range of silicon microwave ICs that Philips Semiconductors, Nijmegen, The Netherlands, will make available early in 1998. The circuits are fabricated on a bipolar process that uses two layers of polysilicon and was adapted from standard IC techniques.

Using the "Double Polysilicon" process, Philips' engineers developed medium-power and small-signal bipolar silicon transistors with a cutoff frequency (f_t) over 23 GHz, the ability to operate at 3 V or less, relatively low noise, and high efficiency at power gains of 20 dB at 2 GHz.

Moreover, since the process results in RF transistors whose collector contact is routed to the surface of the chip rather than through the substrate, transistors can be isolated from each other. This allows them to be used for IC functions that require several transistors and passive components like capacitors, resistors, and inductors to form silicon microwave ICs. At the same time, since all electrical contacts are brought to the die's top surface, the substrate is effectively isolated, allowing direct contact to the ground plane.

Pieter Lok, RF innovation manager for Philips' Discrete Semiconductors Business Group, says the idea is to satisfy mobile-telephone makers in their continuing quest for smaller size, lighter weight, longer talk, and standby times, and good performance in terms of range and drop outs, and, above all, lower cost.

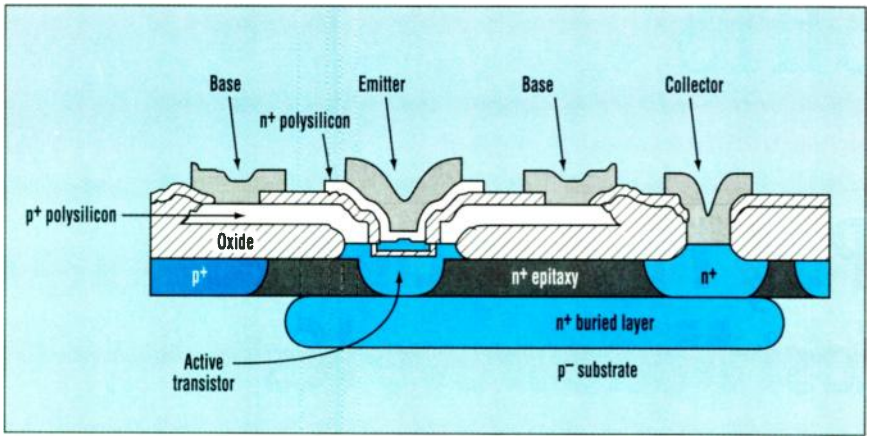
He explains, "We translated those requirements into technology drivers. First, we had to reduce component costs and component count. Then we had to look at efficiency, especially for transmitter power amplifiers, because that's the main contributor to talk time and the telephone makers want to be able to use smaller and lighter batteries. That means lower voltage and current operation and better receiver noise. At the same time, in a highly competitive market, they want shorter design times."

Lok adds, "For the receiver, the most important thing is to be able amplify microvolts into millivolts, which requires small signal transistors that can handle say 3 to 10 mA but with low noise; while for the transmitter, the main thing is power amplification from a few milliwatts to between 0.5 and 3 W using two or three medium-power RF transistors with 25 mA to 2 A and high efficiency."

At the same time, radio frequencies allocated for mobile-telephone and other wireless networks around the world are creeping further into the microwave region, with public and private mobile networks operating now at around 2 GHz, and with future requirements for wireless local loops and LANs planned for the spectrum between 2.4 and 10 GHz.

Philips believes that the new range of silicon microwave ICs from the new process will go a long way toward the achievement of these goals. The process minimizes collector-base capacitance, and in small-signal transistors allows a single metal layer to be used for emitter and base connections.

This construction is in marked contrast to small-signal double-polysilicon processes used by other manufacturers that require the use of a double layer of metallization that increases manufacturing complexity and cost. For medium-power devices, it allows large-area metallization for the emitter which means the transistors can handle rela-



1. Two layers of polysilicon, one to connect with the base region on two sides, and another for the emitter contact, are used by Philips in this double polysilicon process that enables the development of low-cost microwave ICs. Because the final size of an active transistor is not defined by metal pitch, transistor base dimensions can be made as small as 100 nm using 0.8-µm design rules.

tively high current densities. Devices made on the new process will, according to Philips, offer a significant price and performance advantage over competing devices such as GaAs MESFETS.

Although initially targeted at mobile and cordless telephones, Philips expects silicon microwave ICs to find ready use in other applications where their high performance, low cost, and small package size will make them attractive. The company has in mind cable TV, instrumentation, and "unlicensed band" radio applications such as short-range telemetry from embedded sensors.

The Process

Performance goals for the new process include a high f_T, very low Miller capacitance for high gain, and very low base resistance for low noise. Project manager Paul Swinkels explains that to produce transistors with f_Ts of 25 GHz capable of operating at 3 V or less, you need base widths on the order of 100 nm. Philips' engineers hit on the idea of using polysilicon depositions to make the connections to deeply buried base- and emitter-active regions *(Fig. 1)*.

They used two layers of polysilicon; one to connect with the base region on two sides, and a second for the emitter contact. The final size of the active transistor is not defined by metal pitch, and as a result while 0.8-µm surface features can be made on the die, transistor base dimensions can be 100 nm as required for true high-frequency operation.

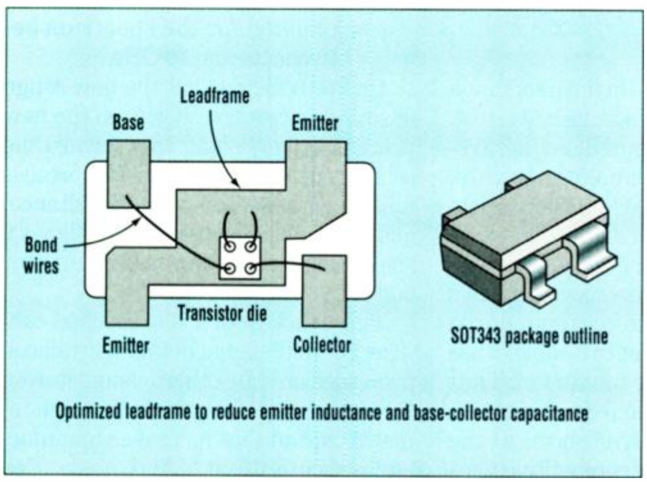
Polysilicon is deposited by low-pressure chemical vapor with precise control over the thickness of polysilicon grown over layers of silicon or SiO_2. In turn, that allows production of self-aligned vertical transistor structures.

Steep doping profiles are used to obtain the very narrow base widths required for realization of a high f_T while submicron emitter widths—typically 0.5 µm—that result from self-alignment inherent in the process ensure a high f_{MAX} and low base resistivity for good noise performance. Lateral connection to the base region by p^+ silicon also helps reduce base resistance, leading to noise performance of typically less than 1.2 dB.

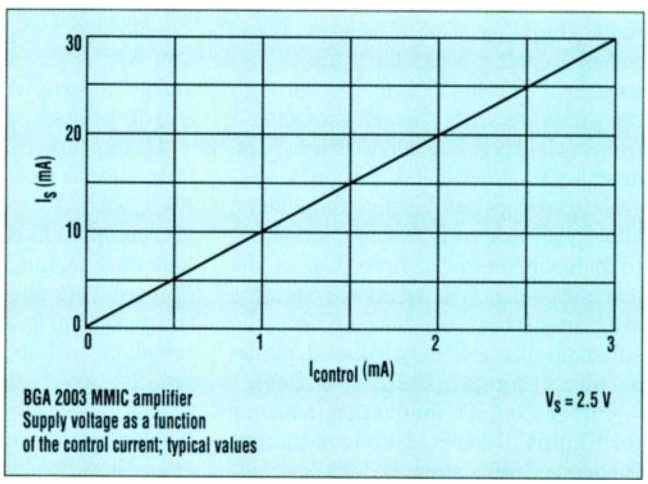
The Package

But producing these "intrinsic" high-frequency transistors is only half of the story. In a practical transistor, packaging plays an important role. "Intrinsically high transistor performance can be completely destroyed if bond-wire and lead-out arrangements in the device package are not carefully designed," says Swinkels. In practice, lead- and bond-wire inductance and collector-base capacitance are the most significant factors that limit high-frequency gain. For small-signal devices, the dominant contribution to collector-base capacitance comes from the bonding pads rather than the intrinsic transistor itself.

"If the transistor die is mounted conventionally with the substrate forming the collector connection, then bond pad capacitance is unacceptable," Swinkels says. And that's one area where the new Philips' double polysilicon process shows its effectiveness. By bringing the collector connection to the top surface of the die, it not only maintains a low value of "intrinsic" collector-base



2. This lead frame designed by Philips takes advantage of takes advantage of the company's bipolar double polysilicon process for high-frequency devices.



3. Linear control over collector currents from 0 to 30 mA is provided by the BGA2003 npn transistor. The device is built on Philips' double polysilicon process.

capacitance, but also minimizes the length of the emitter bond wire and reduces emitter inductance.

At the same time, for medium-power RF transistors, the critical specifications are power output, power gain and power-added efficiency (PAE). For a given power output, the most important factor is the ratio of collector current to base-collector capacitance The self-aligned double-polysilicon process achieves a low collector-base capacitance, while high-collector current capabilities can be achieved by increasing collector doping levels.

The submicron emitter width prevents current crowding effects and helps keep base resistance low, to prevent degradation of power gain. At the same time, the "collector-up" structure allows the emitter to be formed within the substrate, providing for grounded emitter circuit layouts which in turn allows heat-sinking arrangements to be optimized since conduction of heat from the emitter can be done directly from the emitter lead frame to a printed-circuit board. This layout provides power transistors that can operate at 1.8 GHz from a 3.5-V power supply with power gains greater than 11 dB and with PAEs that Swinkels claims can be as high as 60%.

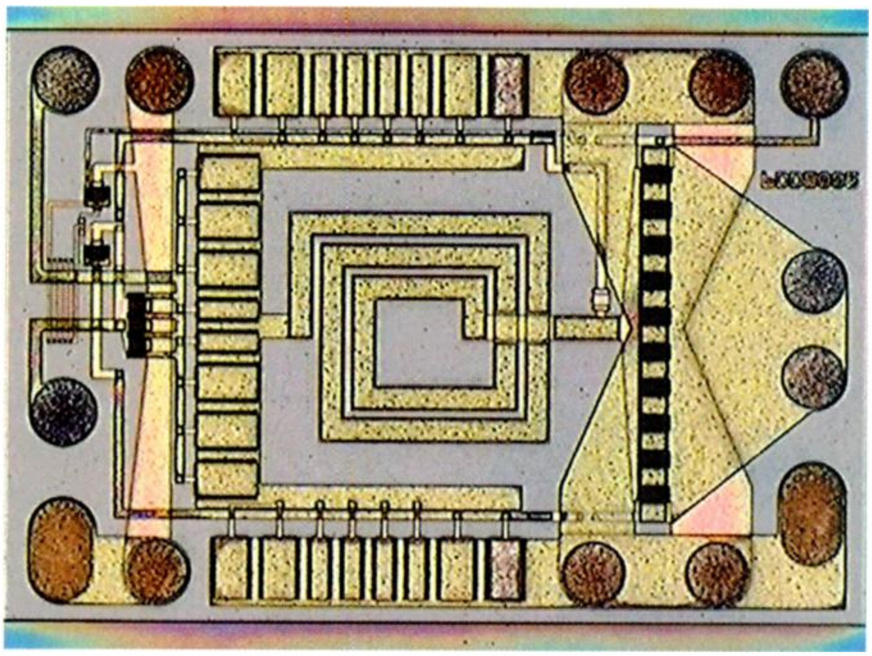
Heat Sinking

In practical terms, the double-polysilicon process also allows a designer more latitude in getting heat away from power amplifiers. The process allows for the deployment of contacts on the top surface of the die for best efficiency for optimum wire-bond length. So where appropriate, contacts can be arranged so that the transistor can be mounted on a grounded surface and thus allow heat to be dissipated more easily.

"With previous processes, the collector was live and heat sinking became quite critical especially at high frequencies and high power," Swinkels explains. "Heat sinking in mobile telephones is becoming very difficult. Ideally, the substrate of the transistor should be connected to ground. It depends on the application though. For example, CDMA at 1.9 GHz is about the worst case, requiring about 2 W of power dissipation for long periods of time. With a live collector through the back of the die, heat sinking becomes very difficult, if not impossible, because it introduces so many parasitics making matching and heat radiation very difficult."

The double-polysilicon construction makes it a lot easier for the set maker to work with. The epitaxial layer and very thin base regions gives the high f_T needed; the small base contacts and selectively implanted collector and buried layer with collector on top of the die all reduce the Miller capacitance and give a fairly high gain for the transistor. The self-aligned process and submicron emitters used mean a low base resistance and low noise. And, because existing silicon technology is used, low cost is possible.

Philips has designed a lead-frame layout to take advantage of this situation *(Fig. 2)*. The figure shows how this is applied for discrete transistor packages.



4. This two-stage MMIC power amplifier from Philips, the BGA2051, is optimized for cordless 1900-MHz DECT, PHS, and PWT telephone applications. Supplied in an 8-pin plastic surface-mount SO-8 package, it delivers 400mW at a 3.6-V supply and has 23-dB gain.

Integrated Circuits

The double-polysilicon process was introduced early in 1997 with a range of discrete small-signal and medium-power transistors. These served to reduce system costs associated with the use of discrete GaAs transistors or earlier types of silicon RF transistors, cutting component count and pc-board area for a typical cordless-telephone 1.9-GHz transmitter amplifier by some 50%.

"However, their use still requires a high degree of expertise in microwave circuit design and they still require the use of discrete passive components for biasing, temperature compensation, and so on," says Loek C. Colussi, senior development engineer at Philips Semiconductors Microwaves & RF division.

Having proved the polysilicon process, the next step for Philips is the design and introduction of functional circuit blocks. These will include a series of basic "building blocks" such as low-noise amplifiers, and mixer and buffer circuits to allow mobile-telephone designers to retain existing system architectures.

Colussi says that the initial plan is to take to what he calls a "small-scale integration approach." He explains the idea is to reduce time to design but without sacrificing design flexibility. "If we try to combine all these functions in one IC, then we may get a situation where the RF signal has to go off chip between stages for filtering for example. That involves a lot of additional components for decoupling and so on. When using small building blocks, a designer can follow the mainstream without degrading performance," he adds.

One of the first RF building blocks to be defined is one of the simplest and most flexible. It's basically an npn transistor combined with biasing and temperature-compensation circuits to form a self-contained general-purpose microwave amplifier. There are three versions, designated as BGA 2001, BGA 2002, and

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OPA340	High Speed, Rail-to-Rail I/O	S,D,Q	2.5 to 5.5	750	$0.52	11404	92
OPA237	Low Power, Single Supply	S,D,Q	2.7 to 36	170	$0.81	11327	93
OPA337	Single Supply, CMOS	S,D	2.5 to 5.5	450	$0.26	11410	94

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BGA 2003. The devices use the same four-lead SOT 343 package as the discrete transistors, but with one of the terminals used for a bias control signal.

The BGA 2003 makes the designer's job easier and reduces time-to-design because the temperature dependency of the collector current is now completely compensated. There is hardly any variation with temperature and process spread since the collector current is set within narrow limits. As a result, the designer doesn't have to worry about spread in current gain or changing transistor characteristics since that's all compensated internally. Integrating the bias circuit also provides an easy way to switch the transistor using the bias network control line.

With discrete designs, switching the transistor on and off in time-division multiple-access (TDMA) systems meant literally switching the collector supply. With the BGA 2003, the collector current can be switched from the bias control circuit, which requires a very low current, without disconnecting the transistor from the power supply. For the rest, it's still the same transistor so the designer still has access to the base, collector and the emitter so he or she can still make a flexible design in terms of operating frequency. Band-matching is done externally so a design can be optimized for low noise, power output or high gain, or a combination of these parameters.

Performance includes power gains of 19 dB for the BGA2001, and 21dB for the BGA2002/BGA2003 with noise figures of 1.5dB and 1.9dB, respectively, at 2 GHz. The BGA2001 and BGA2002 have a fixed bias current of 4 mA and 10 mA, respectively, at a 2.5-V supply, while the bias current of the BGA2003 is adjustable up to 3 mA by means of a control pin, providing linear control over collector currents from 0 to 30 mA *(Fig. 3)*.

Colussi admits that these devices are in effect "smart" transistors and as such represent the lowest level of integration. Nevertheless, their use eliminates many of the of the time-consuming calculations involved in designing with "simple" transistors and allows easy introduction of enhanced features. "For example, in a receiver that needs to work over a very large dynamic range, the bias level can be set to vary with the signal input level and save battery life for longer standby time" he adds. They can be used in a wide range of applications such as a low-noise amplifier, a mixer, wideband applications such as analog and digital cellular telephones, PHS and DECT cordless telephones, radar detectors, satellite television tuners, and high-frequency oscillators.

Three more circuits that integrate what Colussi describes as "real building blocks" include a low-noise amplifier, a mixer and a power amplifier. These will provide true 50-Ω matched input and output facilities.

The BGA 2051 MMIC power amplifier is a two-stage device optimized for cordless-telephone applications such as DECT, PHS, or PWT that operate in the 1900-MHz band. It can deliver an output power of 400 mW at a supply voltage of 3.6 V. Its output is switched for TDMA applications by means of a pulsed voltage applied to a control pin. Gain is 23 dB It is supplied in an 8-pin plastic surface-mount SO-8 package. *(Fig. 4)*. The BGA2021 mixer MMIC is primarily intended for applications in the receiver side of wireless systems and can operate over a frequency range from 0.5 to 2.5 GHz The internally balanced structure ensures good isolation. It is available in a six-pin SOT-457 surface-mount package.

Also under development is a multichip module that will in effect form a complete transmitter "front end" for TDMA operation in the 860 to 915-MHz band such as GSM. The BGY 241 operates with a nominal supply of 3.5 V and provides an output of 35 dBm. It's a three-stage amplifier in a SOT-482A leadless package. It comprises a MMIC amplifier that drives an npn silicon power transistor both mounted on a metallized ceramic substrate.

Price And Availability

Engineering samples for all devices are expected early in first quarter 1998 except for the BGY 241 TDMA amplifier which will be available in engineering samples during second quarter 1998. Pricing has yet to be fixed, but Lok promises that they will provide bill of materials savings compared with similar-performance functions made with discrete devices.

Contact Pieter Lok, RF innovation manager, Philips Semiconductors, Building BY2, Gertstweg 2, 6534 AE, Nijmegen, The Netherlands; e-mail: Pieter.Lok@nym.sc.philips.com. **CIRCLE 542**

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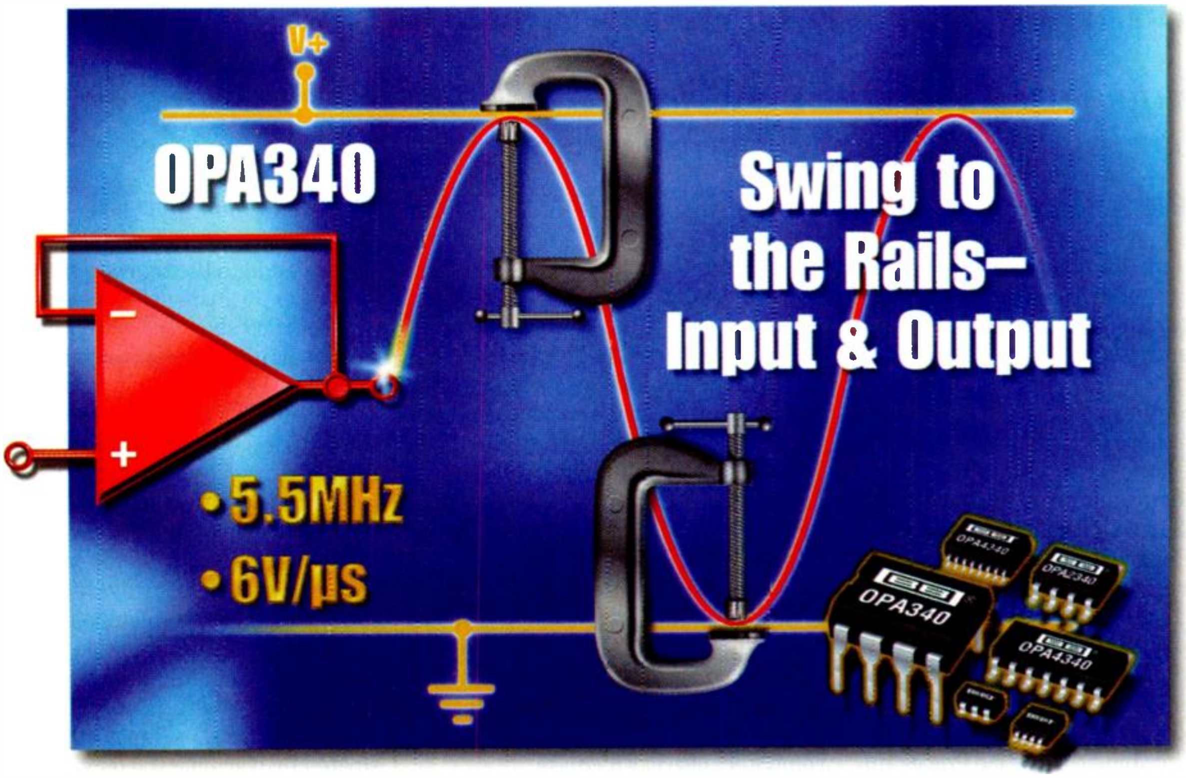

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- Quiescent Current....................750µA/Channel
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  - OPA2340 (dual)....................MSOP-8, SO-8, 8-pin DIP
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Notebook Computer Makers Address Power Challenges

Manufacturers Are Uniting Behind The Mobile Power Initiative, A Coordinated Industry Program.

REX C. PEAIRS, Intel Corp., 2200 Mission College Blvd., MS SC9-15, Santa Clara, Calif. 95054; (408) 765-8080.

Anyone who has ever worked at any time with laptop computers has probably noticed that the heat that's generated out of them can make your lap pretty toasty. If current trends continue, within the next couple of years, they could get way too hot for anyone's lap.

To address this problem, Intel Corp., Santa Clara, Calif., has launched the Mobile Power Initiative. It is a cooperative program that unites industry leaders in addressing all of the areas that impact notebook system power: the hardware, the operating system, and applications.

This article is the first of a three-part series describing the Mobile Power Initiative. This particular article will focus on the hardware aspects of the initiative describing power targets and power saving techniques for notebook computer subsystems. Subsequent articles will focus on how the operating system and application software impacts notebook power, and also will identify ways to make them more power-friendly.

Problems On The Horizon

Notebook computers are incorporating many features contained in high-performance desktop systems, including high-performance processors, second-level cache, better graphics, DVD drives, and new I/O buses like the Universal Serial Bus (USB).

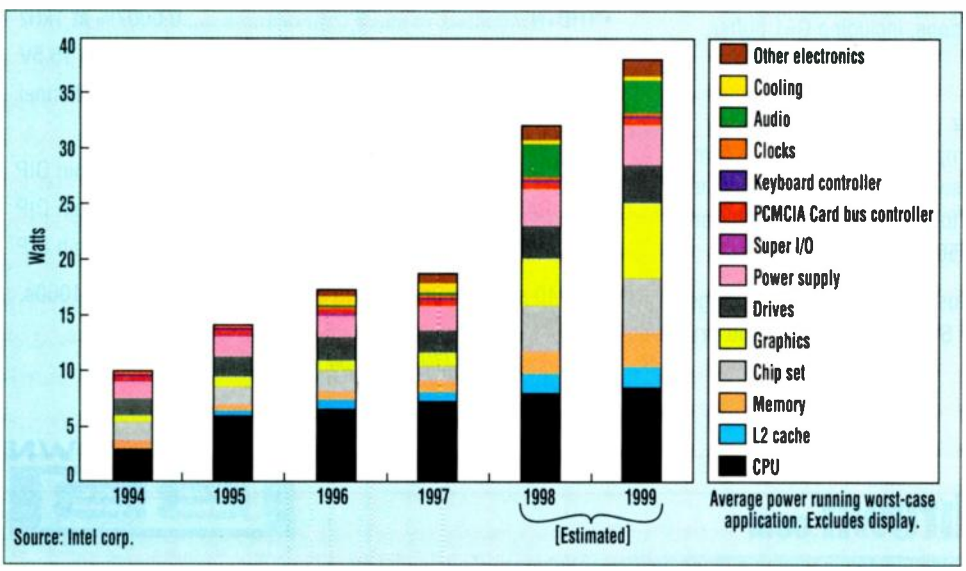
Projecting this trend over the next few years to include features such as larger LCD screens, accelerated 3D graphics, more system memory, and 1394-based I/O devices shows that the power required to run new notebook computers also will increase.

Shown is the growth in full-featured notebook interior power since 1994 and the projected power growth through 1999 if nothing is done to manage power consumption *(see the figure)*. Notebook interior power includes all components inside the notebook main chassis. It excludes the LCD panel power since it does not add to the thermal energy dissipated in the main notebook chassis.

The trend shows power dissipated in notebook interiors increasing by 90% between 1994 and 1997 and projects power by another 85% by 1999. If notebook power consumption continues unmanaged, it will soon outpace notebook thermal capabilities, limiting future system features and performance.

At the same time, notebook cooling techniques also have evolved, albeit more slowly. Current notebook systems measuring 8 fi by 11 in. with base-unit thickness (excluding lid) between 0.75 and 1.5 in. can dissipate about 23 to 25 W.

The heat from inside a notebook is dissipated by warming the outside surface (skin) of the plastic over the ambient air and by using a fan and heat exchanger. Most fan designs can remove about 4 to 6 W of heat, and the remainder is passively dissipated by natural convection and radiation from the outside surface. Due to ergonomic constraints limiting notebook computer skin temperature to approximately 15°C over ambient air temperature, future systems will likely remain constrained in the same thermal envelope. As a result, projected system power is unmanageable and requires reducing notebook system power consumption.



Unmanaged notebook computer power trends as seen by Intel in its Mobile Power Initiative.

Mobile Power Initiative

As mentioned earlier, the Mobile Power Initiative addresses the three areas that impact system power: platform hardware, operating system, and application software. Application software consumes power by using system resources. Some programs use resources inefficiently and don't allow idle devices to enter low-power states.

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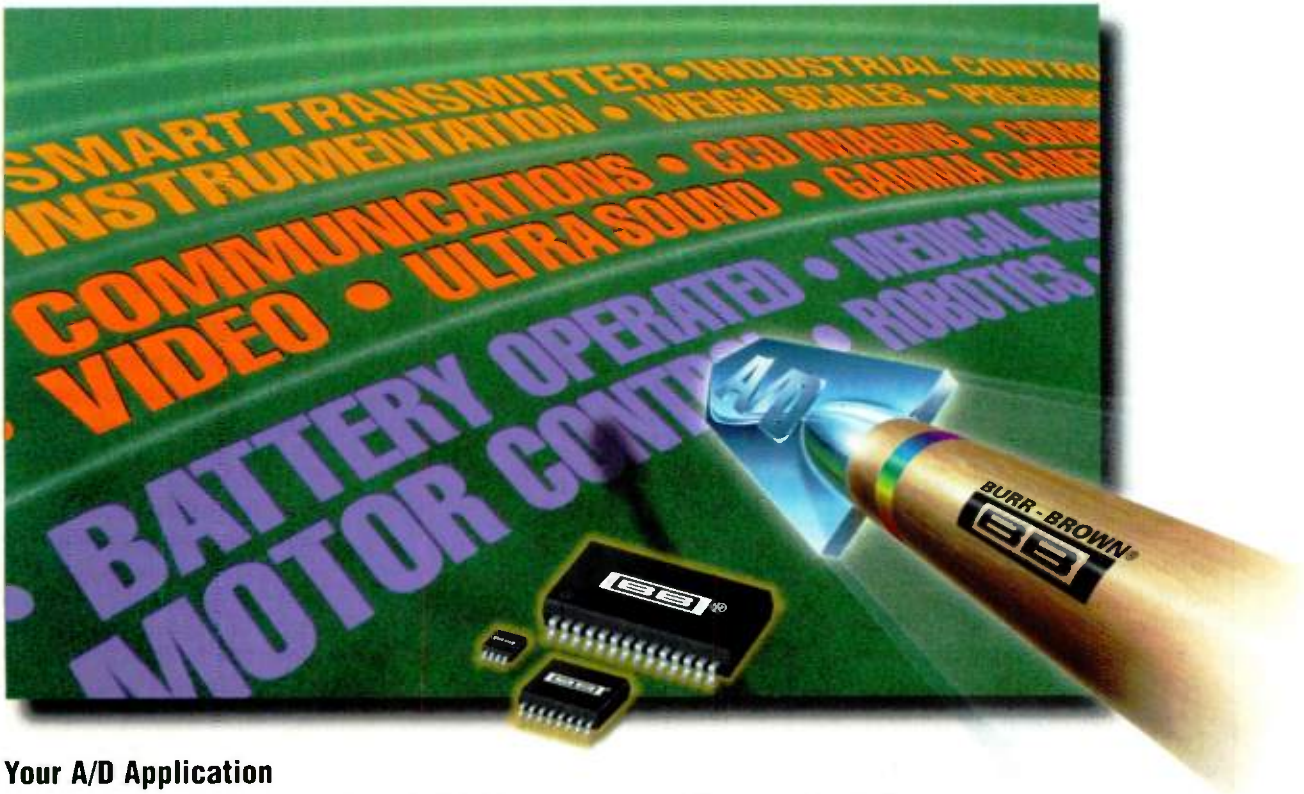

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ADS1214	±0.0015	±20mV to ±320mV	22	16	1.4	$7.25	11368	82

HIGH-SPEED A/D CONVERTERS **preliminary information*

Product	Resolution (Bits)	Speed (MHz)	Power (mW)	SNR (dB)	DNL (LSB)	SFDR (dBFS)	Supply (V)	Price (1kpcs)	FAX*LINE* # 1-800-548-6133	Reader Service #
ADS800	12	40	390	64	±0.6	61	+5	$29.00	11286	83
ADS803	12	5	116	69	±0.3	82	+5	$9.55	11398	84
ADS824*	10	75	315	59	±0.5	70	+5	$8.50	11403	85
ADS930/931	8	30	66/63	46/48	±0.4	51/49	+3/+5	$3.37/$3.27	11349	86

GENERAL PURPOSE A/D CONVERTERS **no missing code*

Product	Resolution (Bits)	INL (LSB)	DNL* (Bit)	Sample Rate (kHz)	Power (mW)	SINAD (dB)	THD (dB)	Price (1kpcs)	FAX*LINE* # 1-800-548-6133	Reader Service #
ADS7813	16	±2.0	16	40	35	87	−90	$20.00	11302	87
ADS7817	12	±1	12	200	2.3	71	−83	$5.18	11369	88
ADS7822	12	±0.75	12	75	0.54	71	−82	$4.64	11358	89
ADS7825	16	±2.0	16	40	50	86	−90	$28.46	11304	90

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TABLE 1: 1999 SYSTEM CONFIGURATION ASSUMPTIONS

- Mobile PentiumII processor or next generation
- 512 Kbyte pipeline burst level two cache
- Graphics controller
  - AGP 2x interface
  - 4 Mbyte frame buffer
  - 1024 x 768 x 24 bit/pixel resolution
  - MPEG-2 H/W assist (motion comp., YUV 4:2:0)
  - Enhanced 3D acceleration
  - LCD and CRT dual screen support
  - LVDS or Panel Link display interface
  - TV output
- 13.3-in. color TFT LCD display
- Memory subsystem
  - 64-Mbyte RDRAM memory
- I/O subsystem
  - I/O controller with integrated timers, counters, etc.
  - 3.3-V 33 MHz PCI bus
  - Fast IR
  - System Management Bus (SM Bus) controller
  - Universal Serial Bus (USB) controller
  - Parallel and serial ports
  - Keyboard controller
  - ACPI microcontroller with SM Bus system battery interface.
- 1394
  - 1 S400 Mobile Device Bay port
  - 1 S400 walk-up port
- 2 USB ports
  - 1 Mobile Device Bay
  - 1 external USB connector
- Storage media
  - Floppy drive
  - IDE hard drive
  - 1394 DVD-ROM in device bay
- CardBus
  - 2 power managed slots
- Audio
  - Sound blaster S/W emulation
  - Waveable synthesis (downloadable samples)
  - 3D positional sound
  - AC3/MPEG-2 decode
  - Full duplex G.723.1 encode/decode with acoustic echo cancellation
  - Host controller
- Software modem data pump
- PCI Docking
- LAN on motherboard

To address application power, monitoring and analysis tools are available to identify and correct power-wasting code.

The operating system manages resources requested by applications. In this capacity, it has a system-wide view of which resources are being used and which are idle. Intel, Microsoft, and Toshiba have co-authored an industry power management specification called the Advanced Configuration and Power Interface (ACPI) to utilize this operating system knowledge to improve system power management.

At the cornerstone of the initiative are the Mobile Power Guidelines that provide achievable power targets for system hardware components to keep overall notebook power within the 23- to 25-W thermal limit. They also give recommendations on achieving these targets, such as voltage reduction and low-power design techniques.

Meeting these targets ensures that mobile PC systems in 1999 will contain all the features and performance users demand, while holding power within manageable thermal limits. As a result, users will get higher performance and more power-efficient systems. Hardware component vendors and OEMs will benefit from cost reductions due to lower power components, lighter-weight thermal solutions, and higher product reliability.

Component Power Targets

Identifying component power targets that result in a thermally manageable system requires identifying system configuration and usage assumptions. High-end, full-featured systems implementing the latest technology are assumed here, since they will be pushing the thermal envelope. It also is assumed that solving the thermal problem for high-end systems will automatically solve it for full-sized mid-range and entry-level systems. Depicted are the configuration assumptions for systems shipping in 1999 specified in the Mobile Power Guidelines *(Table 1)*.

Because not all components are simultaneously active at full power, we

TABLE 2: 3D GAME AND MPEG-2 SUBSYSTEM UTILIZATION ESTIMATES AND 1999 AVERAGE THERMAL POWER TARGETS

	3D Game Utilization	3D Game Power (W)	MPEG-2 Utilization	MPEG2 Power (W)
CPU core	80%	7.9	65%	6.5
L2 cache	50%	1.6	40%	1.4
Memory controller	67%	1.2	50%	0.9
System memory	50%	1.4	50%	1.4
Graphics subsystem	75%	2.4	75%	2.4
I/O subsystem	I/O Ctrl 25%, KBC 75%, uCtrl 30%	0.5	I/O Ctrl 60%, KBC 0%, uCtrl 5%	0.6
Audio	30%	1.5	30%	1.5
Hard drive	Spin-up 2%, Rd 5%, Idle 31%, Stdby 63%	0.7	0%	0.0
DVD drive	Spin-up 4%, Rd 30%, Idle 6%, Stdby 60%	2.3	Spin-up 0%, Rd 100%, Idle 0%, Stdby 0%	3.9
1394	60%	0.9	100%	0.9
USB	0%	0.0	0%	0.0
CardBus	0%	0.1	0%	0.1
LAN	5%	0.4	5%	0.4
Power supply	88% efficient	2.1	90% efficient	2.2
Charging		0.1		1.0
Cooling	100%	0.5	100%	0.5
Other	100%	0.3	100%	0.3
Total system power		**23.9**		**24.0**

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PCM1723 features an on-board phase-locked loop (PLL) which generates a 256/384fs digital audio system clock from a standard 27MHz MPEG-2 video clock. Priced from $3.95 in 1000s.

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Products	Description	Bits	Dynamic Range	SNR	THD+N	Maximum Sample Rate	Supply Voltage	Package	FAX*LINE*# (800) 548-6133	Reader Service #
PCM1717/18	DAC	16/18	96dB	100dB	–90dB	48kHz	+2.7 to +5V	20-Pin SSOP	11289/11325	96
PCM1719	DAC	16/18	96dB	100dB	–88dB	48kHz	+5V	28-Pin SSOP	11343	97
PCM1720	DAC	16/20/24	96dB	100dB	–90dB	96kHz	+5V	20-Pin SSOP	11333	98
PCM1723	DAC	16/20/24	94dB	96dB	–88dB	96kHz	+5V	24-Pin SSOP	11344	99
PCM1727	DAC	16/20/24	92dB	94dB	–88dB	96kHz	+5V	24-Pin SSOP	11407	100
PCM1725	DAC	16	95dB	97dB	–84dB	96kHz	+5V	14-Pin SOIC	11373	101
PCM1800	A/D	20	95dB	95dB	–88dB	48kHz	+5V	24-Pin SSOP	11387	102
PCM3000	CODEC	18	96dB	98dB	–90dB	48kHz	+5V	28-Pin SSOP	11342	103

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TABLE 3: MOBILE SYSTEM COMPONENT CORE VOLTAGE TARGETS

	1997	1998	1999
CPU core	1.8 V	1.6 V	1.6 V or lower
L2 cache	3.3 V	3.3 V	3.3 V
Memory controller	3.3 V	3.3 V	1.8 V
System memory	3.3 V (EDO/SDRAM)	3.3 V (EDO/SDRAM)	2.5 V (RDRAM)
Graphics controller	3.3 V	2.5 V	1.8 V
Graphics frame buffer	3.3 V (EDO/SDRAM)	3.3 V (EDO/SDRAM/RDRAM)	3.3 V or Integrated
I/O controller	3.3 V	3.3 V	2.5 V
LCD Logic	5 V	5 or 3.3 V	3.3 V
Backlight inverter	Battery voltage	Battery voltage	Battery voltage
FLASH EPROM	3.3 V	3.3 V	3.3 V
Audio (digital)	3.3 V	3.3 V	2.5 V
Audio CODEC	5 V	5 V	3.3 V
Super I/O	3.3 V	3.3 V	2.5 V
1394 controller	None	None	2.5 V
CardBus controller	3.3 V	3.3 V	2.5 V
LAN	3.3 V (PC Card or dock)	3.3 V (PC Card or dock)	3.3 V
MODEM DSP	3.3 V	3.3 V	Soft modem
MODEM CODEC/DAA	5 V	5 V	3.3 V

must define the system usage scenarios that generate the worst-case thermal power likely to occur. Power testing while running several applications showed playing an MPEG-2 movie as the worst-case power application in our test suite. Extrapolating this data to 1999, it is expected that the worst-case power applications will be 3D games and MPEG-2 video playback.

The 3D-game scenario assumes scenes are stored on a DVD drive, the hard drive is accessed occasionally, and audio is active at 30% amplifier power. An on-board LAN is connected and is assumed idle, as are the CardBus slots. The MPEG-2 movie scenario assumes the same conditions as the 3D game except that movie data is continuously read from the DVD drive and the hard drive is powered-off.

Power is specified in terms of peak power, idle power, and average power while running 3D-game and MPEG-2 applications. Peak power is the highest power a subsystem will draw at nominal V_{CC} and maximum performance (i.e., the CPU doing floating-point calculations at top frequency with most data hitting the level-1 cache, DRAM reading at peak bandwidth, etc.). This assumes the subsystem is utilized at 100% capacity and draws maximum power at maximum performance. Idle power is the power a subsystem draws at nominal V_{CC} when not processing data. This is defined as 0% utilization.

During normal system operation, most subsystems are utilized at a percentage of their maximum capacity and power. For most subsystems, power consumption is assumed to scale linearly with utilization between idle power and peak power. Average thermal power for a subsystem running a particular application can be estimated by:

Subsystem average thermal power = [(subsystem peak power ↔ utilization) + (subsystem average power ↔ (1 - utilization)]

Power consumption for some components, such as an audio accelerator or 1394 interface, does not scale linearly with utilization. Here, power consumption was estimated individually and summed with the rest of the subsystem.

The worst-case system thermal power is the sum of the average thermal power for each subsystem while running the worst-case power application. Shown is estimated subsystem use for 3D-game and MPEG-2 movie scenarios and average thermal power targets proposed for 1999 systems *(Table 2)*.

Power-Reduction Methods

Meeting these power targets and improving notebook system performance is accomplished by methods including voltage reduction, component optimization, improvements in device power management, and software optimization. Power consumed in CMOS circuits is proportional to frequency and voltage as shown by:

Power ∝ [(capacitance ↔ frequency ↔ (voltage)^2] + [(voltage ↔ (dc current + leakage current)]

The dc and leakage currents tend to be small for CMOS circuits—CFV^2 dominates the equation. So, reducing the frequency reduces power linearly. However, performance is reduced linearly. Reducing voltage has the advantage of reducing power as the square of the voltage. Components optimized for lower-voltage voltage operation also benefit from improved performance since they can operate at higher speeds. Thus, voltage reduction yields the biggest component power improvement.

Industry coordination in moving components to lower voltages will help minimize the power planes required and reduce system cost. Depicted are proposed mobile component core-voltage and interface bus-voltage targets through 1999 *(Table 3)*.

Rex Peairs holds a bachelors degree in computer engineering from San Jose University. He is a senior hardware engineer with Intel's Mobile and Handheld Products Group, Santa Clara, Calif.

How Valuable	Circle
Highly	536
Moderately	537
Slightly	538

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READER SERVICE 109

Desktop EDA Will Redefine Tool Access And Integration

Unix, Mid-Range EDA, Mid-Range Windows NT, And Windows Desktop EDA Solutions Vie To Be The Designer's Platform Of Choice.

NICK MARTIN, Protel Technology Inc., 4675 Stevens Creek Blvd., Suite 200, Santa Clara, CA 95051; (408) 243-8143 or (800) 544-4186; fax: (408) 243-8544.

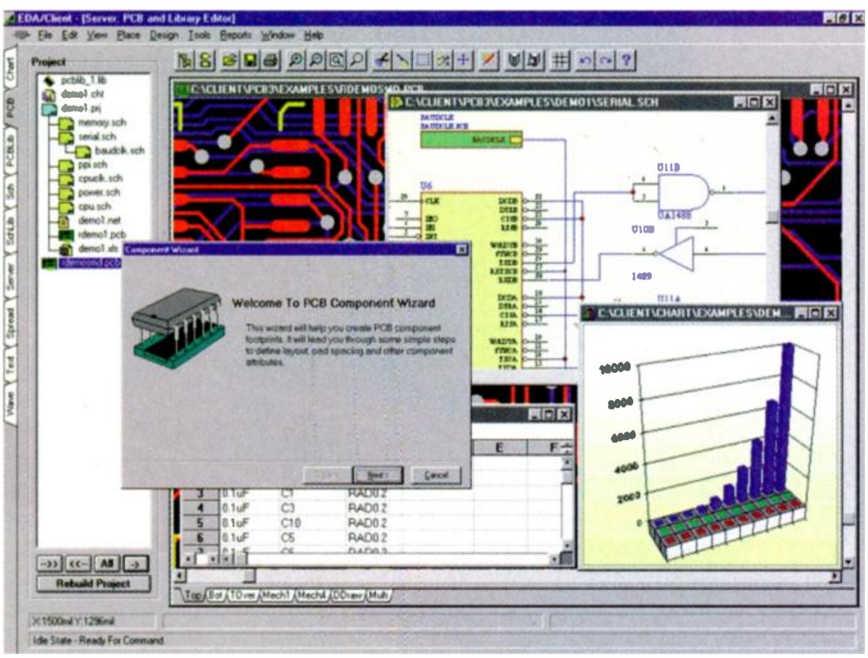
In the movie *Monty Python and the Holy Grail*, a troll guards a bridge across a deep chasm. To cross the bridge, the crusaders must each answer an absurd riddle. Failure to provide the right answer results in the victim's instant jettisoning into the abyss. In today's EDA marketplace, choosing a board-level design tool strategy is a lot like answering the troll—one wrong answer—and you're in deep trouble.

Designers are increasingly trapped between the limitations of today's methodology and pressure to move the design flow onto an ever faster track. In the electronic OEM arena, where technology seems to move at a continually accelerating pace, package density, interconnects, and ever-higher frequency domains are pushing users and tools to their limits. A point-and-shoot strategy, adding new design tools incrementally to solve new problems, breaks down as the integration of new and existing tools desynchronizes. Therefore, it's no surprise that engineers cite "most-effective functionality for the user's design flow" as the first priority for tool selection over price, ease-of-use, or other performance criteria (*Electronic Design's* "1996 EDA Market Study," p. 122). In other words, EDA needs to move from a tool-centered process to a design-centered process. Over time, EDA tools will be valued more by their success in addressing the total design environment than by an ability to deliver a level of specific EDA functionality.

As tool development shifts rapidly toward the desktop, and away from workstation-based tools, it's clear that there's a distinct generational split between traditional workstation platforms and desktop computing. As EDA tools migrate to what has become the Windows platform, user's expectations for these tools will change. The dynamics of desktop computing, driven by a mass market, differ dramatically from the engineering workstation market.

Unlike their workstation counterparts, Windows EDA tools coexist with general-purpose software on the desktop *(see the figure)*. Running alongside spreadsheets and word processors, interoperability issues expand from inter-tool to environmental. Desktop EDA tools must support PC-level standards, including de facto standards, such drag-and-drop editing and the ability to move data between applications via the Windows clipboard. Tools that successfully address these standards provide the first level of normalization of the total computing environment, where tools begin to work transparently with non-engineering applications.

Design team expectations regarding access tools and new technologies also change fundamentally in this desktop scenario. Engineers may have been content to share a dedicated design workstation in the past, but desktop tools imply access at every desktop in the organization. Of course, accessibility issues also include the ease with which tools can be learned and used. That factor is defined by the way other desktop applications adhere to interface standards, and the way they are packaged for user-installation, including tutorial-based documentation and on-line help.



EDA tools can coexist with general-purpose software within Protel's EDA/Client environment. Here, pc-board and schematic layouts are open with spreadsheet and chart documents, and a component wizard is running in the foreground.

It is estimated that at least 70% of EDA end-users are already using at least some PC-based tools. This figure is not surprising because nearly all engineers and designers have PCs on their desktop today. The way the EDA landscape looks today, the bulk of these users have already moved their tools to the Windows platform, are in the process of moving to Windows, or are planning for a move to Windows NT. Unix-based EDA companies, which have dominated the design tool market for two decades, have either announced or released their first Windows tools.

Where workstation-based tool development has resulted in a restricted market, the desktop-EDA industry has enjoyed the benefits of an exploding personal computing market. Object-oriented programming and standardized platforms like Windows, client/server computing, and Rapid Application Development technologies have transformed this process from a craftsman/cottage industry into an industrial model built upon code reusability and modularity. The changing economics of software development is supporting the rapid proliferation of new applications. It allows developers to target specialized markets, including electronics design tools. From the end-user's perspective, the desktop model is exciting because it has the potential to speed the delivery of new technologies.

Platform Options

The organizational decision to adopt one design platform over another is now based on a limited number of distinct options. These options include full-solution Unix tools, mid-range EDA solutions, mid-range Windows NT solutions, and Windows desktop-EDA point tools.

In full-solution Unix tools, a single vendor provides the core tools and defines the level of tool integration. The high cost and long-term return on investment limit this option to a small group of customers. Expectations regarding high-end design functionality are high, and there is a large service/consulting component in the lifetime cost calculation.

Mid-range EDA solutions straddle the workstation and PC platforms. These tools are more likely to provide meaningful cross-platform integration and open architecture, but this can be limited by the built-in dependencies that exist in a multi-vendor environment. The distribution and support model for these tools allows end-user cost, but still restricts the size of this market.

A mid-range Windows NT solution is another viable platform option. Vendors from all ends of the EDA market are currently converging on a premium Windows position that potentially replaces the mid-range solutions described above. This approach is staked on Windows NT workstation's acceptance as a desktop replacement for Unix. While offering a more robust and secure platform for networking, NT's progress has been hampered by slow delivery of hardware drivers and software that exploits it's native 32-bit operating system.

The last option is Windows desktop EDA point tools. This option consists of shrink-wrapped, ready to install and use, out-of-the-box products which are generally dedicated to a single EDA application such as schematic entry, board layout, PLD programming, or analog simulation. Suites of tools, with a level of tool-to-tool integration are provided by most vendors, but the quality of integration, particularly with third-party tools, is difficult to predict. However, the distribution and support model for these tools keeps costs low, making them accessible to organizations of any size.

Medium-term EDA space is expected to evolve into a predominantly Windows/Windows NT environment, as new and growing companies increasingly opt for the economics of desktop engineering. But the questions remain, "What kinds of solutions will these companies need, and which EDA tool developers are best positioned to service this need?"

Because the smaller EDA companies are built upon a business model that uses economical development and delivery mechanisms, they are able to effectively change the size of the market, spreading development costs over an expanded user base.

Tool Integration

Tool integration is another serious challenge for the traditional EDA development model. Rebellion of end-users against proprietary tools has led to some industry attempts at standardization. The results of this effort have been mixed. At best, standardized formats, such as Electronic Design Interoperability Format (EDIF), become restrictive pipes through which data can flow from system to system.

Desktop EDA has grappled with tool integration, as well. No company has the resources needed to develop and deliver a complete design solution for every user. From the beginning, the desktop point tools have had to provide built-in support for netlist and database translation. This support is driven by the potential expansion of a tool's market if it's compatible with another vendor's product. End users like the flexibility and lack of dependence upon a single vendor, but struggle to manage integration on their own.

Providing links between tools is dependent upon maintaining version synchronization as the tools are updated. Developers are unlikely to support each other's efforts to maintain compatibility—especially if they view the other parties as direct competitors. The tool user ends up falling into the inevitable cracks.

The likely success of Windows thus poses a new integration paradox. Small companies can move quickly to bring new technology to market at an accessible price, but they don't have the resources to provide a complete design solution. They also lack the dominance to impose standards across the industry.

This problem is not exclusive to EDA. Inter-tool communication is a concern for all business applications. Microsoft is responding to this need with evolving support for open standards such as ActiveX and OLE which can provide broadly accepted protocols for integration of all applications, not just engineering tool integration. Desktop EDA vendors are already exploiting this potential by linking their design tools to general purpose applications such as spreadsheets, word processors, and databases.

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nents so that they can be developed and delivered independently of each other in an open setting, under standards that come from the environment. Under this model, client and server modules can be developed and upgraded independently.

It has been clear for some time that Windows will impose a new set of standards and expectations. All EDA developers will be forced to abandon their proprietary methods on several fronts. The need for efficient development will drive developers to use emerging software technology.

Likely features of this new generation of tools include a truly open system with a fully exposed API, which allows access to system processes and data; documented database formats; structured macro languages; and end-user development kits with source code examples. Other features include predefined macros and wizards which encapsulate design task expertise, can be user-modified, and can automate coding.

Exposing an application's processes and data via an API allows virtually limitless customization of tools by both third-party developers and by skilled end-users alike. This approach can completely remove dependence on developers to provide and maintain tool integration, transferring ownership of the integration process directly to the marketplace. An industry has already grown up around this model in the broad computing marketplace, where systems integrators and client/server developers add value to off-the-shelf applications. Engineers are already among the best prepared of any professional group to seize the power of these implicitly open environments where hard distinctions between design tools and software developments begin to blur.

Releasing control over tool integration is potentially risky to developers because it creates a truly vendor-independent environment where developers will have to compete to continuously add value to their own products. However, the potential to totally redefine the whole tool delivery process creates huge opportunities to create new applications for design technology and new markets. Ultimately, open EDA integration provides a platform upon which the end-user organization can gain its own design expertise, either for reuse or distribution.

Emerging networking and communication technologies will bring the process full circle, where security, performance, and other benefits formerly restricted to Unix environments have gained commodity status on networked PCs. Nearly 90% of engineers are now using the Internet as a tool. The broad computing market is actively exploiting this new global connectivity, empowering the worldwide electronic design community with the potential to support collaboration between engineers and developers on a real-time basis. A clear trend is already emerging in the area of data-book information and device-model libraries. On-line distribution of component data and part libraries, for example, allows the engineer immediate access to new technology without the previous time-dependency on traditional publishing and distribution. This kind of scenario illustrates the movement of development away from specific tools, and toward solutions that only occur at the environment level.

Moving from a tool-centered to a task-centered approach is the first step toward resynchronizing EDA development with the many exciting changes that are occurring with desktop hardware and software. Engineers will demand the high level of finish, integration, functionality, and value that they have come to expect from commercial applications.

Being out of phase with traditional practices and strategies for EDA tool development may well be the strongest attribute of desktop EDA. The broad software market provides a much better model for this necessary evolution than the inwardly focused, proprietary norms of traditional EDA. This emerging, globally linked, real-time engineering community is the ultimate beneficiary of this revolution.

Nick Martin is the founder of Protel Technology Ltd. Previously, he worked in the Physics Department of the University of Tazmania, Australia.

HOW VALUABLE	CIRCLE
HIGHLY	546
MODERATELY	547
SLIGHTLY	548

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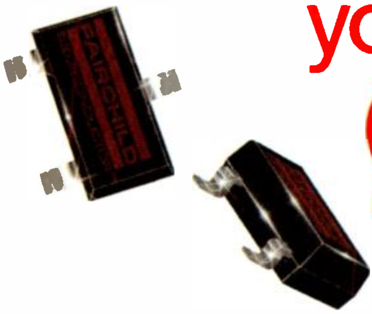

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Zero Standby • NM93CxxLZ • V_{CC}: 2.5V - 5.5V • Iccstdby: <1μA • 256bit - 16Kbit • X8 or 16 org	**Zero Standby** • NM24CxxLZ • V_{CC}: 2.5V - 5.5V • Iccstdby: <1μA • 256bit - 16Kbit	**Zero Standby** • NM25CxxxLZ • V_{CC}: 2.5V - 5.5V • Iccstdby: <1μA • 256bit - 16Kbit

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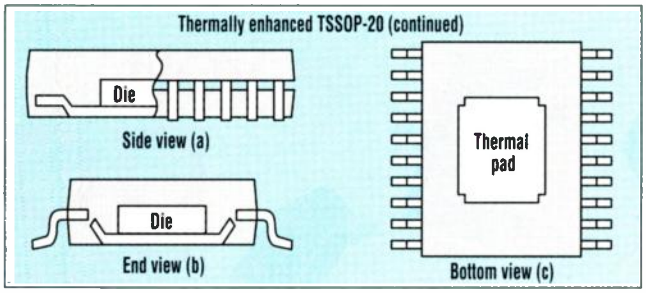
Thermal Pad Raises SMD Power-Handling Capability

By Raising The Power Level At Which Heat Sinks And Fans Are Required, The Pad Also Saves On Space, Cost, And Dissipation.

Patrick Mannion

With the drive toward miniaturization not likely to slow down any time soon, surface-mount devices are under increasing pressure to dissipate ever-rising power levels in ever-shrinking packages. While handling the heat generated by these devices is often simply a matter of adding more heat sinks or blowing more air, in many situations there are serious space, power consumption, and cost issues that tend to narrow a designer's options. What these designers need is an inexpensive, easy-to-implement solution that won't take up a lot of space.

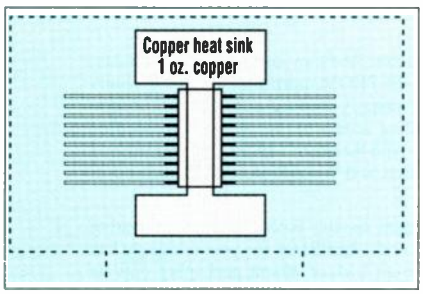
Texas Instruments Inc. (TI), Dallas, has answered the call by modifying its TSSOP-20-based line of low-dropout voltage regulators to include a thermal pad that gives a more effective thermal coupling of the chip to the printed-wiring board (PWB) (*Fig. 1*). Called the PowerPAD, the proprietary package is formed using a lead-frame design and manufacturing technique to provide the user with a direct connection to the heat-generating IC.



1. Formed using a lead-frame design and manufacturing technique, the PowerPAD package gives a more effective thermal coupling of the heat-generating chip to the PWB to get the heat out to the awaiting heat sink quickly and efficiently—without raising the cost of the package.

Some key features of the device include process compatibility, with no customer retooling required, high moisture resistance, despite having an exposed die, and, of course, low cost.

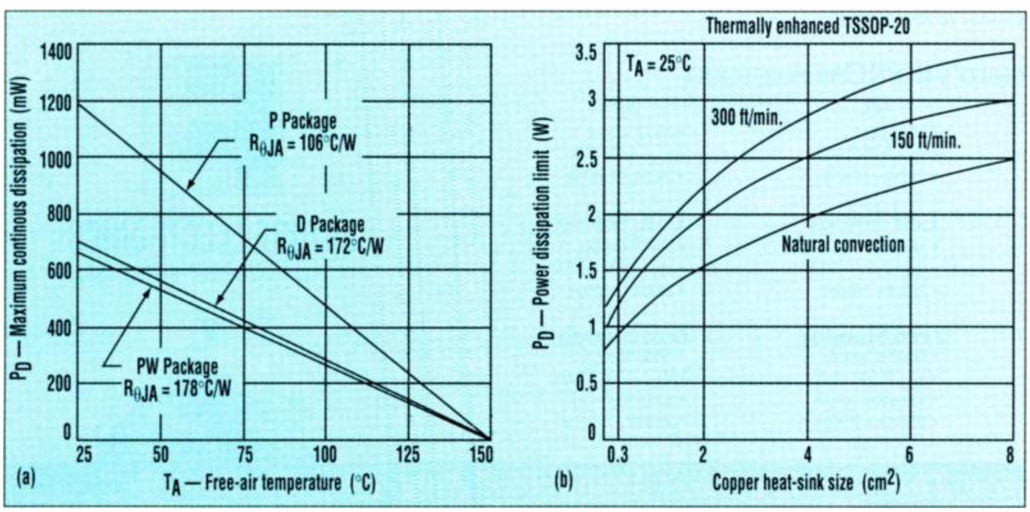
TI's approach is the second prong of the standard three-pronged attack usually taken to tackle thermal issues. The first is to improve the power-dissipation capability of the PWB design, while the third is to introduce airflow in the system. Closely coupling the chip to the PWB completes the strategy and allows fine-pitch, surface-mount technology with thermal performance comparable to much larger power packages.



2. A typical 20-lead TSSOP package depends on thermal pastes to connect the package to the copper heat sink below.

For a typical 20-lead TSSOP package, thermal enhancement means adding 1-oz. copper to the PWB to conduct heat away (*Fig. 2*). This method allows the standard package, under natural convection and with suitable conductive between the board and the device body, to dissipate approximately 700 mW at an ambient temperature of 25°C (*Fig. 3a*).

With the thermal pad connecting



3. The standard TSSOP-20 package, in free air and with suitable conductive between the board and the device body, can dissipate approximately 700 mW at an ambient temperature of 25°C (a). With 8 cm^2 of copper, the PowerPAD-enhanced package can dissipate up to 2.5 W, again at 25°C (b). As the copper area decreases, the device's power-handling capability goes down accordingly. The effect of adding air flow also is shown.

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the die directly to the PWB, the power-dissipation capability of the package is tied even more closely to the thermal parameters of the PWB. With 8 cm^2 of copper, and under free-air (natural convection) conditions, the PowerPAD-enhanced package can dissipate up to 2.5 W, again at 25°C (*Fig. 3b*). As the copper area decreases, the device's power-handling capability goes down accordingly. The effect of adding air flow is also shown.

Mounting Information

Because the thermal pad is directly connected to the IC substrate, the heat-sink surface that is added to the PWB can be a ground plane or left electrically isolated. Since the pad is not a primary connection, the importance of the electrical connection is not significant. The object here is to complete the thermal contact between the thermal pad and the PWB.

The thermal pad itself is fully intended to be soldered at the time the component is mounted. Although voiding in the thermal-pad to solder connection is not desirable, up to 50% voiding is acceptable. Thermal analysis shows that there is no significant difference resulting from the variation in voiding percentage.

The PowerPAD has already been introduced into a number of the company's power products. These include the TPA0102, 0103, and 1517 line of audio amplifiers, its high-speed video-amplifier products, and its TPS71H-series of low-dropout voltage regulators. According to the company, there is no cost premium for a PowerPAD-enhanced TSSOP-20 versus a regular TSSOP-20. While TI holds the patent for the design, it is considering licensing it to interested parties in the very near future.

PRICE AND AVAILABILITY

The PowerPAD can be used in a number of applications at various price points. For further information, readers should contact Texas Instruments Inc., Literature Response Center, P.O. Box 17228, Denver, CO 80217; Customer Response (800) 477-8924; Internet: http://www.ti.com. **CIRCLE 532**

HOW VALUABLE	CIRCLE
HIGHLY	533
MODERATELY	534
SLIGHTLY	535

ANALOG DESIGN SOLUTIONS 1

Ultralow-Noise LDO Voltage Regulators

Communication and VCO circuits require well regulated, low noise supply lines that can switch on and off quickly. They also need small size, high precision, and low power ICs.

MIC5205/06 low-dropout linear regulators can improve noise performance by 20dB over other regulators, making them ideal for voltage-controlled oscillator (VCO) and RF circuits.

Both are low-dropout PNP regulators that include a reference bypass pin for additional noise reduction. A single 470pF capacitor, connected from the bypass pin to ground, reduces output noise by $V_{OUT}/1.24V$ (12dB for the 5V part) and creates a noise pole below 100Hz.

With better than 1% output accuracy and ground current of less than 0.6mA at a 100mA load, the MIC5205/06 are ideal for hand-held battery-powered applications.

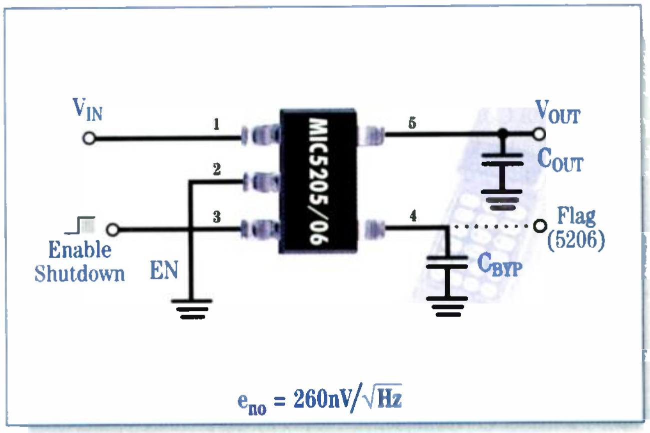
The MIC5205/06 are efficient, accurate, ultralow-noise regulators with typical output noise of $260nV/\sqrt{Hz}$. To maximize battery life, the dropout voltage is typically 10mV at light loads. At the rated 150mA output, dropout voltage is only 165mV.

Key Features

- Ultralow noise
- 150mA output current
- 1% output accuracy
- Wide choice of output voltages
- "Zero" off-mode current
- Current, thermal and reverse battery protection
- Fast transient response
- Ultra-tiny SOT-23-5 and MSOP-8 packages

Prolongs Battery Life

The MIC5205/06 extend operating life by prolonging battery charge. It maintains regulation with as little as a 50mV differential between input and output and offers an on-chip on/off control that reduces power drain to less than 1µA. In sleep mode, quiescent current drops to nearly zero, further extending battery life.

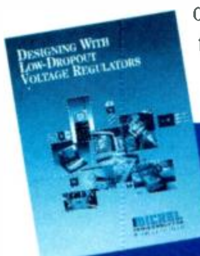


Protection

Additional safety features include reversed battery protection, current limiting and overtemperature shutdown. The MIC5206 also provides an Error Flag to indicate output voltage faults such as low battery, overcurrent, or overtemperature conditions.

Fixed or Adjustable Voltages

The MIC5205/06 are available with fixed or adjustable output voltages. Standard fixed voltages are 3.0V, 3.3V, 3.6V, 3.8V, 4.0V and 5.0V. All parts have 1% initial accuracy and operate over a junction temperature range of -40°C to +125°C.



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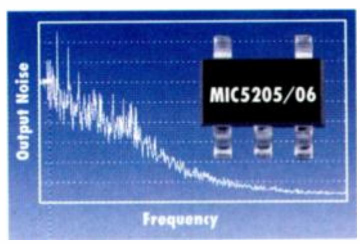
Designed for Ultralow-Noise

The MIC5205/06 were designed for excellent low-noise performance but have even better performance with an optional external capacitor. This capacitor (C_{BYP}) is inserted into the voltage divider that sets the loop gain necessary to achieve a specific output voltage. Although gain is a necessary part of the feedback that makes a regulator work, it also "amplifies" noise. The capacitor reduces the loop gain at high frequencies to reduce high-frequency noise.



Fits Anywhere

Both of these new regulators are available in Micrel's IttyBitty™ SOT-23-5 five-lead packages and include a logic compatible Enable pin. The MIC5206 is also available in the new Micrel Mini8™ 8-lead MSOP package.

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The Wireless Symposium and Exhibition, Feb. 9-13. Santa Clara Convention Center, Santa Clara, CA. Contact Bill Rutledge, Penton Publishing, 611 Rte. 46 West, Hasbrouck Heights, NJ 07604; (201) 393-6259; fax (201) 393-6297; instant faxback (800) 561-7469; Internet: http://www.penton.com/wireless.

Sixth Annual Automated Imaging Association Business Conference, Feb. 10-12. Buena Vista Place, Orlando, FL. Contact Automated Imaging Association, P.O. Box 3724, Ann Arbor, MI 48106; (313) 994-6088; fax (313) 994-3338.

Asia-South Pacific DAC (ASP-DAC '98) and EDA TechnoFair (EDATF), Feb. 10-13. Pacifico Yokohama Convention Center, Yokohama, Japan. Contact ASP-DAC '98 Secretariat, c/o Convex Inc., Ichijoji Bldg., 2-3-22 Azabudai, Minato-ku, Tokyo, 106 Japan; +81 3-3589-3355; fax +81 3-3589-3974; e-mail: convex@po.iijnet.or.jp.

IEEE Applied Power Electronics Conference and Exposition (APEC '98), Feb. 15-19. The Disneyland Hotel, Anaheim, CA. Contact Pamela Wagner, Courtesy Associates, 655 15th St., N.W., #300, Washington, DC 20005; (202) 639-4990; fax (202) 347-6109; e-mail: pwagner@courtesyassoc.com.

Conference on Optical Fiber Communication (OFC '98), Feb. 22-27. San Jose Convention Center, San Jose, CA. Contact Lisa Myers, OSA Conference Services, 2010 Massachusetts Ave., N.W., Washington, D.C. 20036-1023; (202) 416-1980; fax (202) 416-6100; e-mail: ofc.info@osa.org.

Design, Automation, and Test in Europe Conference and Exhibition (DATE '98), Feb 23-26. Le Palais des Congres de Paris, Porte Maillot. Contact European Conferences, 11C Wemyss Pl., Edinburgh EH3 6DH, UK; +44 131-225-2892; fax +44 131-225-2925.

38th Israel Conference on Aerospace Sciences, Feb. 25-26. Tel-Aviv & Haifa. Contact Technion-Israel Institute of Technology, Haifa 32000, Israel; 972-4-8292713; fax, 972-4-8231848; e-mail: alice@aerodyne.technion.ac.il.

MARCH 1998

Computer Telephony Conference and Exposition '98, Mar. 3-5. Los Angeles Convention Center, Los Angeles, CA. Contact Computer Telephony '98, 1265 Industrial Highway, Southampton, PA 18966; (215) 355-2886; fax (215) 355-4112.

International Verilog Converfence and VHDL International User Forum (IVC/VIUF), Mar. 16-19. Santa Clara Convention Center, Santa Clara, CA. Contact MP Associates, 5305 Spine Rd., Suite A, Boulder, CO 80301; (303) 530-4562; fax (303) 530-4334; e-mail: lee@mpa-net.com; Internet: http://www.hdlcon.org.

IEEE Aerospace Conference, Mar. 21-28. Snowmass Conference Center, Snowmass, CO. Contact Mike Johnson, 2225 Roscomare Road, Los Angeles, CA 90077-2222; (310) 472-8019; e-mail: johnson@ee.ucla.edu.

MARCH 1998

Second Intellectual Property in Electronics Seminar (IP '98), Mar. 23-24. Westin Hotel, Santa Clara, CA. Contact John Whitaker, Miller Freeman Technical Ltd., +44 181-316-3297; e-mail: ed98@cityscape.co.uk.

PCB Design Conference West, Mar. 23-27. Santa Clara Convention Center, Santa Clara, CA. Contact Molly Knox, Miller Freeman, (408) 448-6173; e-mail: mknox@mfi.com.

INFOCOM '98, Mar. 28-Apr. 2. Hotel Nikko, San Francisco, CA. Contact Ramesh Nagarajan, Lucent Technologies, 101 Crawford Corner Rd., Rm. 3M-318, Holmdel, NJ 07933; (732) 949-2761; fax (732) 834-5906; e-mail: rameshn@lucent.com.

IEEE International Reliability Physics Symposium, Mar. 30-Apr. 2. Reno Hilton Hotel, Reno, NV. Contact Ann N. Campbell, M/S 1081, Sandia National Labs., P.O. Box 5800, Albuquerque, NM 87185-1081; (505) 844-7452; fax (505) 844-2991; e-mail: ancampbe@sandia.gov.

IEEE International Parallel Processing Symposium/IEEE 9th Symposium on Parallel and Distributed Processing (IPPS/SPDP), Mar. 30-Apr. 3. Delta Orlando Resort, Orlando, FL. Contact Viktor Prasanna, EEB-200C, Department of EE Systems, University of Southern California, Los Angeles, CA 90089-2562; (213) 740-4483; fax (213) 740-4418; e-mail: prasann@ganges.usc.edu.

Sixth Embebbed Systems Conference Spring, Mar. 31-Apr. 2. Navy Pier Festival Hall, Chicago, IL. Contact Miller Freeman Inc., 600 Harrison St., San Francisco, CA 94107; (415) 905-2354; fax (415) 905-2220; Internet: http://www.embedsyscon.com/.

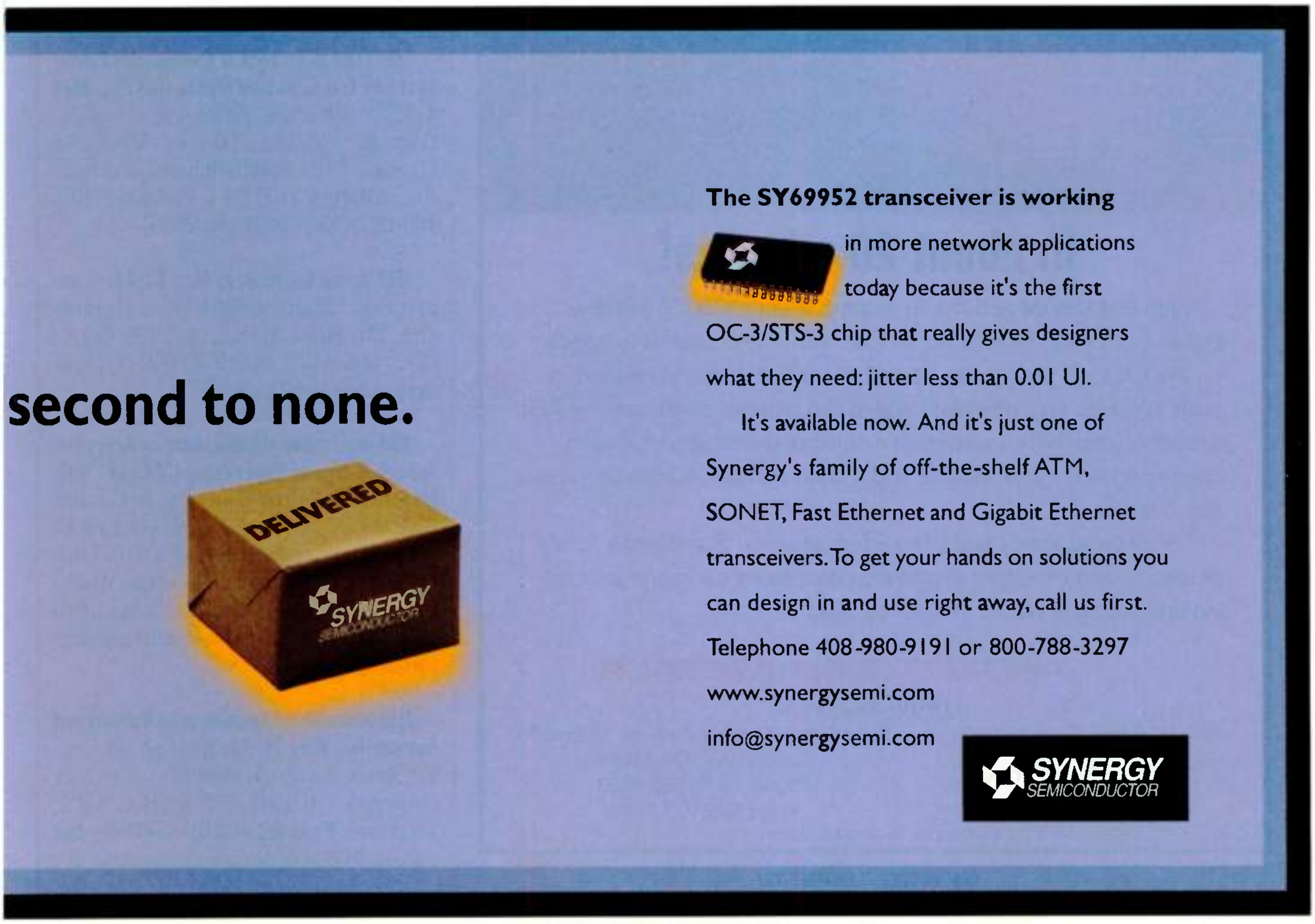
APRIL 1998

20th IEEE International Conference on Software Engineering, Apr. 19-25. Kyoto International. Conference Hall, Kyoto, Japan. Contact Koji Torii, Graduate School of Information Sciences, Nara Institute of Science & Technology, 8916-5 Takayama-cho, Ikoma-shi, Nara-ken 630-01, Japan; +81 7437-2-5310; fax +81 7437-2-5319; e-mail: torii@is.aist-nara.ac.jp.

DSP Spring Design Conference, Apr. 21-23. Santa Clara Convention Center, Santa Clara, CA. Contact Liz Austin, Miller Freeman Inc. (888) 239-5563, (415) 538-3848; e-mail: dspworld@mfi.com; Internet: http://www.dspworld.com.

Southeastcon '98, Apr. 24-26. Hyatt Regency, Orlando International Airport, Orlando, FL. Contact Parveen Ward, ECE Dept., University of Central Florida, Orlando, FL 32816; (407) 823-2610; fax (407) 823-5835; e-mail: pfw@ece.engr.ucf.edu.

16th IEEE VLSI Test Symposium, Apr. 26-30. Hyatt Regency Monterey, Monterey, CA. Contact Rob Roy, Intel Corp., MS:JFT-102, 5300 Elam Young Pkwy., Hillsboro, OR 97124-6497; (503) 264-3738; fax (503) 264-9359; e-mail: robroy@ichips.intel.com.



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APRIL 1998

IPC Printed Circuits Expo '98, Apr. 26-30. Long Beach Convention Center, Long Beach, CA. Contact Dan Green, The Institute for Interconnection & Packaging Electronic Circuits, 2215 Sanders Rd., Northbrook, IL 60062-6135; (847) 509-9700 ext. 371; fax (847) 509-9798.

MAY 1998

Conference on Lasers & Electo-Optics & The International Electronics Conference (CLEO/IEC), May 3-8. The Moscone Center, San Francisco, CA. Contact Amy Hutto, OSA Conference Services, 2010 Massachusetts Ave. N.W., Washington, DC 20036-1023; (202) 416-1980; fax (202) 416-6100; e-mail: cleo. info@osa.org.

IEEE International Conference on Evolutionary Computation, May 3-9. Ankorage, AK. Contact Patrick K. Simpson, Scientific Fishery Systems Inc., P.O. Box 242065, Anchorage, AK 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@akaska.net.

IEEE International Conference on Neural Networks (ICNN '98), May 3-9. Anchorage, AK. Contact Patrick K. Simpson, Scientific Fishery Systems Inc., P.O. Box 242065, Anchorage, AK 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@akaska.net.

IEEE World Congress on Computational Intelligence, May 3-9. William A. Egan Civic and Convention Center, Anchorage, AK. Contact Patrick K. Simpson, Scientific Fishery Systems Inc. P.O. Box 242064, Anchorage, AK 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@alaska.net.

Seventh IEEE International Fuzzy Systems Conference, May 3-9. Anchorage, AK. Contact Patrick K. Simpson, Scientific Fishery Systems Inc., P.O. Box 242065, Anchorage, AK 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@alaska.net.

IEEE/IAS Industrial & Commercial Power Systems Technical Conference (I&CPS), May 4-7. Edmonton, Alberta, Canada. Contact Marty Bince, Modicon Canada Ltd., 5803 86th St., Edmonton, Alberta T6E 2X4, Canada; (403) 468-6673; fax (403) 468-2925.

IEEE Radar Conference, May 12-14. Contact Scott Ramey, 2501 West University, MS 8056, McKinney, TX 75070; (972) 952-4409; fax (972) 952-3071; e-mail: sramey@ti.com.

IEEE International Conference on Acoustics, Speech & Signal Processing (ICASSP '98), May 12-15. Seattle Convention Center, Seattle, Washington. Contact Les E. Atlas, Department EE (FT 10), University of Washington, Seattle, Washington 98195; (206) 685-1315; fax (206) 543-3842; e-mail: atlas@ee.washington.edu.

IEEE International Conference on Robotics and Automation, May 16-21. Katholieki Universiteit, Leuven, Belgium. Contact Georges Giralt, LAAS-CNRS, Toulouse, France, +33 61-33-63-48; fax +33 61-33-64-55; e-mail: giralt@laas.fr.

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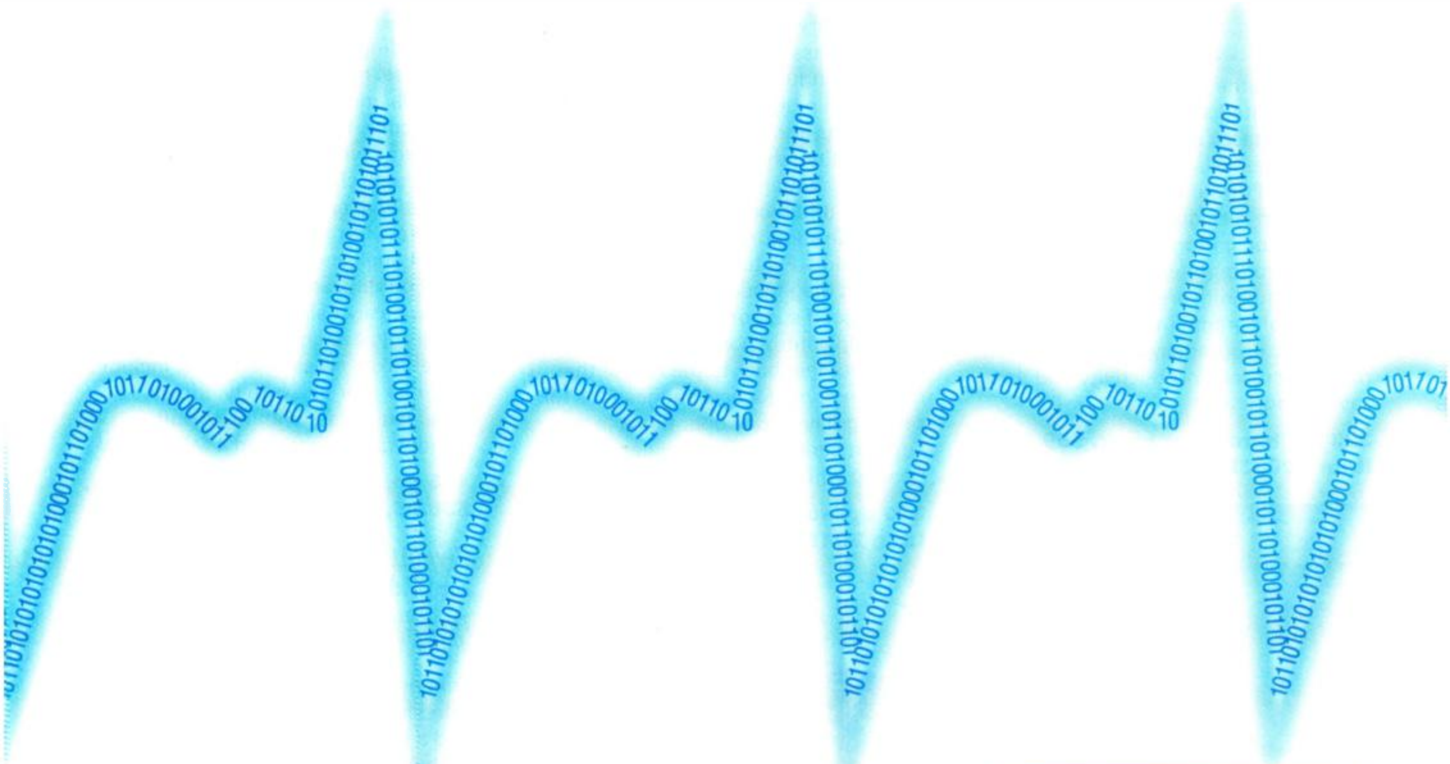

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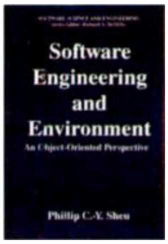

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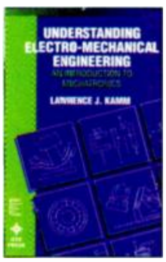

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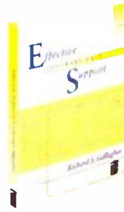

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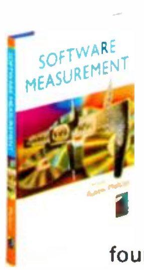

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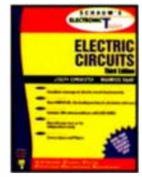

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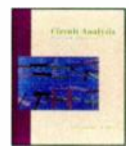

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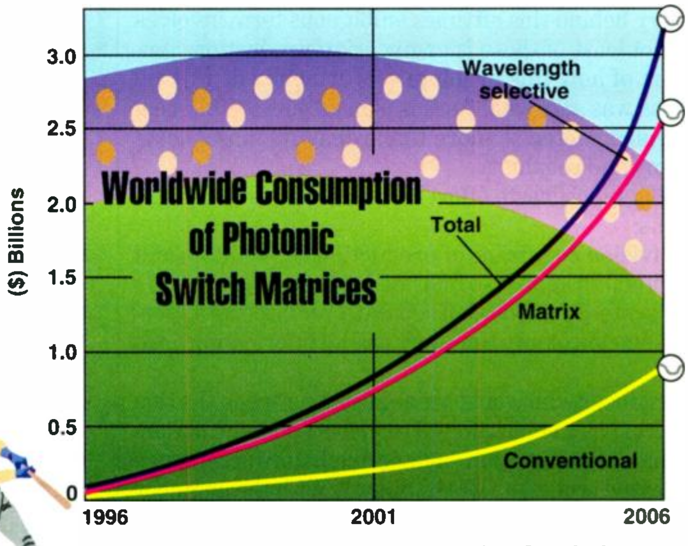
MARKET FACTS

Switch Hitting In Photonics

Following the growth in fiber-optic communication networks, worldwide consumption of photonic switches and switch matrices used in these networks will fly out of the ballpark from $94 million in 1996 to $3.2 billion in 2006. These figures come from a new report by ElectroniCast Corporation, "Photonic Switch and Matrix Technology and Market Global Forecast." The report says that the drive behind this gargantuan expansion is the continued skyrocketing of the telecommunications industry and the loyal use of switches in the increasing private data network sector. Telecommunication equipment only absorbed 19% of the photonic switch and balanced I/O plus MxN matrix global consumption, but the prediction is that telecom value will fly through the roof, rising to over 40% by 2001. Although most of the 1996 switch market comprised conventional switches such as 1x2, 2x2, and 1xN configurations, future growth will occur in complex switch matrix systems. Use of 1xN and MxN photonic switches should increase with the dynamic reconfiguration of the active wavelengths in each network fiber. North America had 72% of worldwide market share in 1996, in terms of photonic switch and matrix consumption. The value of the fiber-optic photonic switch consumed by North America in 1996 totaled $68.3 million, according to the report. The report also predicts a 54% growth per year over the next five years. This growth will be pushed by a further decline in average switch and switch matrix prices. On the production side, North America will take long strides in growth as well. Production of photonic switches and switch matrices will jump from $76.7 million in 1996 to $2.29 billion in 2006. Since the trade balance is swinging in the direction of North America, more foreign producers will build production facilities in the region. In terms of the technology, optical switches are garnering millions of dollars in research and development. The technologies most researched are the use of optical switches in nonlinear optical switches, polymeric film, semiconductor devices, and movable mirrors micromachined in silicon wafers. Developments in wavelength-selective switching, tunable/switchable wavelength transmitters or filters, and demultiplexing to single wavelength per fiber for space switching are now taking place. The report discusses the new markets created by the expansion of network bandwidth and capacity expected over the next 10 years. This requires the strengthening of central office cross-connect (DCS) and trunk-add/drop-multiplex capabilities. The cost of this capability can be reduced through a selective optical bypass in the signal flow around the DCS, and a wavelength-selectable optical add/drop multiplexer. As predicted in the report, major service interruption costs will soar from $400 million in 1996 to over $1.5 billion in 2006. Despite falling charge rates per gigabit/kilometer of service, the throughput carried by each cable also will increase. Fibers also are predicted to change with counts increasing from 1 in 1996 to 20 in 2006, to the average data rate per wavelength quadrupling. Due to the costs associated with network disaster, fiber makers are working to ensure more redundant routes and cranking out big, fast, automated matrix switches. Finally, future applications of photonic space switches will be positively impacted by the resurgence of high-performance optoelectronic ICs.



Art: L.Gravell

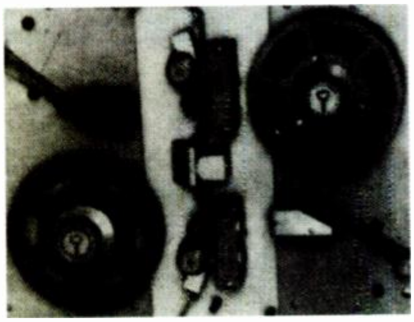
Source: ElectroniCast Corporation

For more information on the report's findings, contact ElectroniCast Corporation by phone at (650) 343-1398; fax (650) 343-1698; e-mail: electronicast@msn.com.—**DS**

40 YEARS AGO IN ELECTRONIC DESIGN

Paper Tape Reader: Fast Start, Stop

Capable of handling paper tape strips or reels with equal facility, this perforated tape reader can operate at speeds of up to 750 characters per sec, with less than 5 msec start or stop time. At 300 characters per sec it stops in the space following the stop character. All standard 5, 6, 7, or 8 level tapes are handled and 11/16, 7/8, or 1-in. wide tape can be used interchangeably. The unit includes highly stable reading heads using silicon photodiodes; transistorized output drivers for low impedance output, and magnetic amplifier reel servos. Digitronics Corp., Dept. ED, Albertson Ave., Albertson, L.I., N.Y. (*Electronic Design, Dec. 15, 1957, p. 83*)



Paper tape readers still were being honed to deliver higher levels of performance, but with magnetic technology improving rapidly, it already was becoming clear that paper tape technology would have a limited lifetime.—SS

Make Prototypes Compatible With Production, By Stephen P. Sims, Filtron Co., Inc., Flushing, N.Y.

Although one of the most important topics in electronics today is reliability, many fail to realize that the story behind this ofttimes ambiguous term involves many phases of the industry. Not least of these is engineering-production compatibility. Following is a report of how this problem was attached at Filtron Company, Inc., and what success was achieved. As this plan attains its full measure of anticipated results , it is expected to more than repay its initial costs through greater rf filter economy and reliability.

In broad outline it was felt that much waste effort could be eliminated by employing the following three plans:

1. Having an engineering division cognizant of production capabilities and constantly serviced by an individual to keep it so informed.
2. Utilizing a manufacturing system composed of separate yet integrated sections, with each section able to divulge, at any time, any and all information as to its progress.
3. Employing a production engineer who would act as liaison between the two main divisions. In addition to acting as a vehicle for all requests and information, his task would include passing on all designs from engineering before acceptance by production. On more complicated orders, he works directly with the engineer while the prototype passes through the design stage.

Because of the possible returns, management, production, and engineering collaborated to form these departments as close to the planned model as possible. And today, these are working realities, whose functions are independent, yet related as part of an integrated whole.(*Electronic Design, Dec. 1, 1957, p. 90*)

This article, presented here in somewhat abbreviated form,shows that the wall that separates engineering and production was put up a long time ago. But even 40 years ago, some groups were attempting to breach the wall.

Finally, a personal note: This wraps things up, not only for this column in 1997, but for my career as an engineer and magazine editor: As of Nov. 1, 1997 (the deadline for this column), I've retired... Well, not totally retired—I'll be doing a couple of projects for Electronic Design next year: I'll still put together this column for each issue, and I'll manage the annual Bob Pease Supplement, which will be published with the August 3, 1998 issue. I'd still like to hear from readers regarding this column; if you see anything here that you want to take issue with, complain about, or expand on, you can send an e-mail message to me at scrupski@worldnet.att.net.—Steve Scrupski

Another Contest

This contest stuff must be going around. Microchip Technology is sponsoring Design98, a contest offering over $35,000 in cash and prizes for the best engineering designs based on the company's PICmicro 8-bit one-time-programmable (OTP) microcontrollers. The contest is being held in conjunction with *Circuit Cellar Ink* magazine, a publication specializing in practical technical information for designers and builders of microcomputer hardware and software.

There are three judging categories for the design challenges: PIC12CXXX, PIC16CXXX, or PIC17CXXX. For Best Overall prize, the winner receives $5000 in cash and a Hewlett-Packard HP54645D Mixed-Signal Oscilloscope. In each of the categories mentioned above, First, Second, and Third Prizes garner $3000, $2000, and $1000, respectively.

Then, there are the other prize winning categories, all must incorporate any of the following Microchip devices:

- 24C00 world's smallest serial EEPROM (SOT-23 package)
- HCS300 KEELOQ code-hopping encoder
- PIC12C5XX world's smallest microcontroller (8-pins)
- PIC16C924 microcontroller with LCD driver
- PIC16F84 8-bit enhanced flash microcontroller
- PIC17C756 64-/68-pin microcrontroller with 10-bit analog-to-digital converter

The prize for winning designs in any of those categories is $500. The deadline for entries to the contest is March 2, 1998. Winners will be announced at the Embedded Systems Conference East on March 31, 1998. Additionally, winners will be featured in *Circuit Cellar INK*'s May 1998 issue.

For more information on *Circuit Cellar INK* or to obtain rules, an entry form, or Design98 facts, contact the magazine at 4 Park St., Vernon, CT 06066; (860) 875-2199; Internet: http://www.circuit cellar.com.—**DS**

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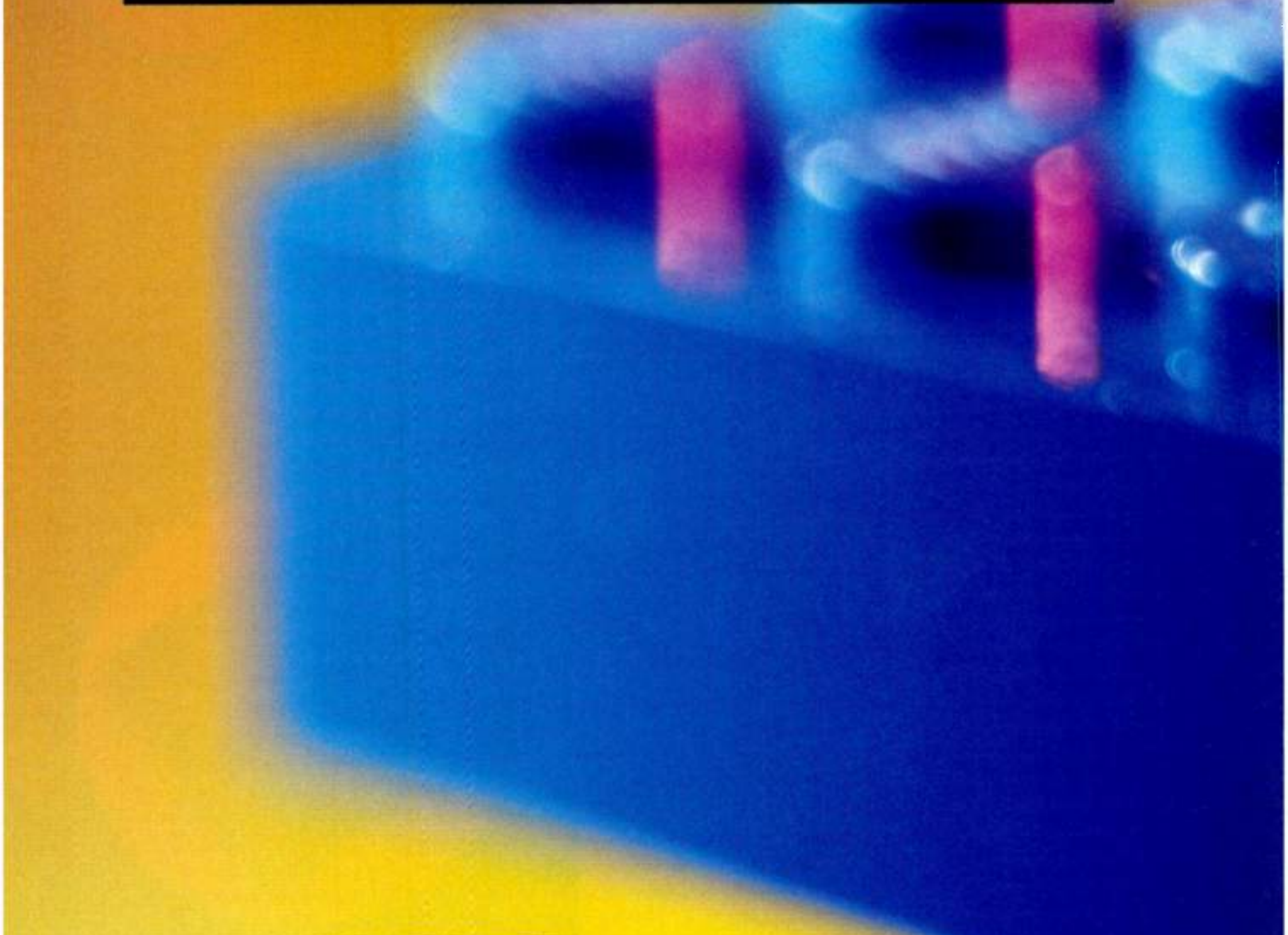

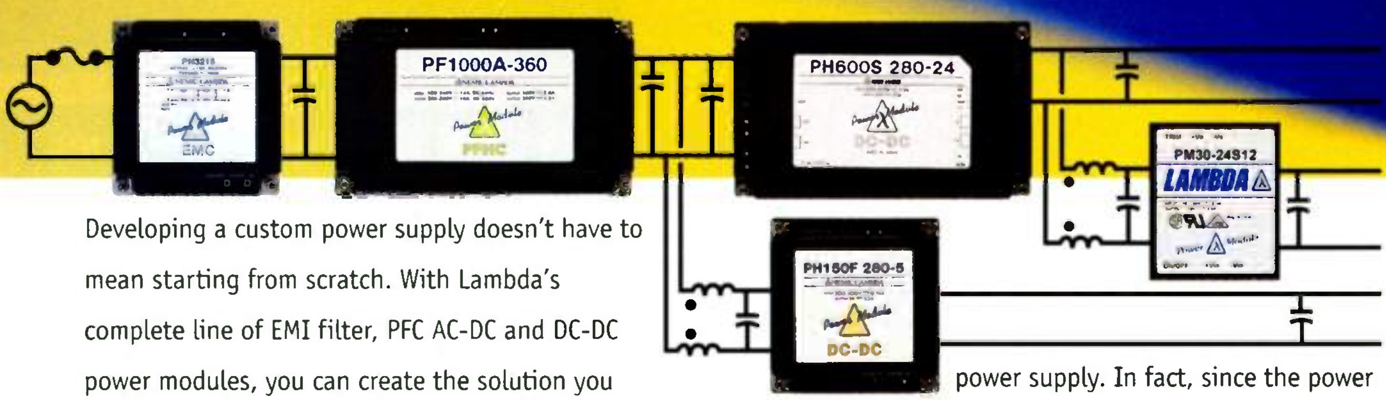

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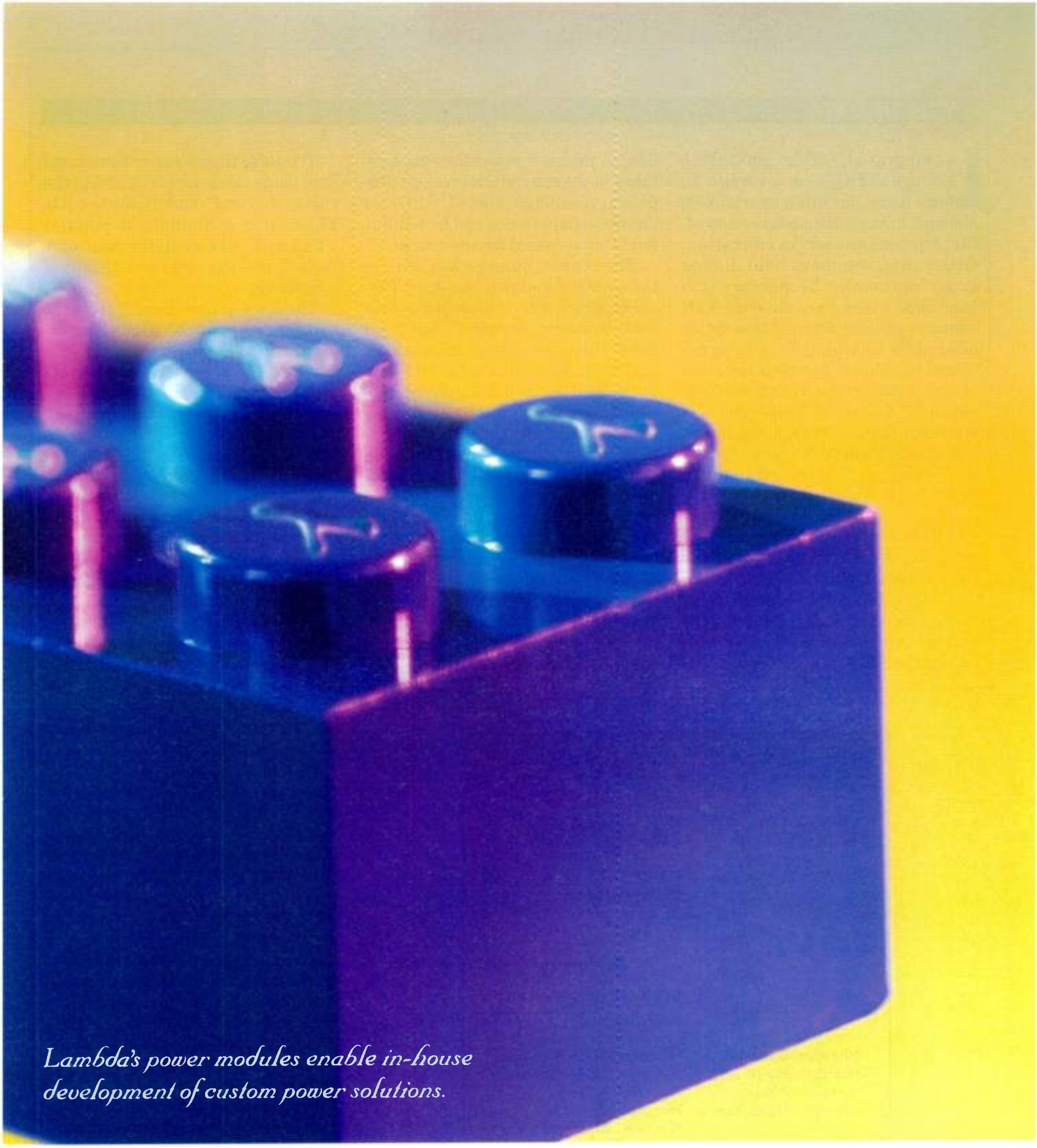

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READER SERVICE 177

Y2K UPDATE

Looking at the Year 2000 Date Change (Y2K) issue coverage, an important, but often overlooked, element of the entire conversion effort that stands out is education. Other than seminars held during large Information Technology (IT) meetings, where does a novice Y2K manager go for guidance? One option offered by Learning Tree International is a three-day course called "Implementing the Year 2000 Conversion." Learning Tree's courses are held in major cities, listed below, and at individual facilities.

The course is designed to teach project managers how to put together an effective strategy for tackling their company's conversion, how to choose the right Y2K solution for their environment, how to make the date-field changes and calculations via automated and manual techniques, how to decide which service vendors and tools will do the job, and how to prevent programming mistakes in the conversion process. Surprisingly enough, some COBOL or database experience can be helpful, but is not required for the course.

The course, number 285, breaks the conversion down into six different categories: Overview of the Year 2000 Problem, Scoping Your Year 2000 Problem, Upgrading Your Code, Working with Tools and Vendors, Testing and Phaseover, and Contingency Planning. Beginning with the overview, the instructors introduce the Y2K problem, the consequences, commonly encountered failures, and guidelines for the process. Next, course participants are taught how to perform a software inventory, analyze business impact, and find source code. Techniques are then discussed regarding the methods of upgrading the problem code. Importantly, Learning Tree emphasizes "getting it right the first time."

The topic that seems to stump and stop many managers is choosing the right tools and vendors for the job. The course examines the popular Y2k tools, how to build your own toolset, and the risks and pitfalls of upgrading.

The testing process of Y2K is the most critical portion of the conversion. Now that we're nearly into 1998, all the emphasis for the next year-and-a-half will be on testing and contingency planning (OK, some emphasis will be on the legal issues that will be popping up like sunflowers on a hot late August day). The "Implementing the Year 2000 Conversion" course will help managers validate their solutions, decide when they've tested enough, run pilot projects, comply with standards, and plan for future maintenance.

In the contingency planning section, administrators will learn how to protect against potential losses of resources, deal with running out of time, form a post-conversion recovery team, and manage date-tagging and configuration control.

Hands-on experience with COBOL code includes observing compliance failure modes, applying the 28-year rollback patch, implementing an entire compliance solution, testing all the aspects of the solution, automating compliance changes, and applying the solution across an integrated environment.

The one-semester-hour credit course takes place in Ottawa, Canada on January 21-23; New York, New York on January 27-29; Washington, D.C. on February 3-5; Boston, Mass. on February 10-12; and Toronto on February 18-20.

Pricing varies, but the standard tuition is $1695. Check with your company, though, since many companies have Training Advantage Tuition Agreements with Learning Tree, which brings the tuition down to $1525. People who've taken courses with the Learning Tree have previously received substantial discounts.

Contact Learning Tree International, Reston Town Center, 1805 Library Street, Reston, VA 20190-5630; (800) 843-8733; Internet: http://www.learningtree.com.—**DS**

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(WHEN A PIECE OF TECHNOLOGY LIKE THIS COMES ALONG, WE'RE GOING TO SUPPORT IT.)

GREENLOOK

American Microsystems Inc. (AMI), an ASIC supplier for communication and industrial applications, has recently signed a memorandum of understanding (MOU) with the U.S. Environmental Protection Agency (EPA) to voluntarily control and reduce the emission of perfluoro compounds (PFCs) from its manufacturing plants into the atmosphere.

With this action, AMI joins other members of the semiconductor industry, along with the EPA, in attempting to find ways to measure, control, and reduce PFC emissions. PFCs used and generated during semiconductor manufacturing operations, such as chemical-vapor deposition-chamber cleaning and the plasma etching of materials such as nitride, oxide, and polysilicon, are suspected to contribute to global warming together with other "greenhouse gases" such as methane and carbon dioxide. The MOU represents part of an ongoing environmental, health, and safety commitment to the world community under ISO 9001 and 14000 standards.

Besides semiconductor manufacturing, PFCs also are emitted from magnesium production, electrical transmission, and distribution systems. They're also by-products of aluminum smelting operations.

The MOU specifies a three-year period during which AMI will research and determine an effective strategy for PFC emissions reduction. During this period, the company will continue tracking and reporting on emissions of six gases including nitrogen, trifluoride, sulfur hexafluoride, fluoroform, perfluoromethane, and perfluoropropane. This feat is accomplished by inventorying processes, chemical purchases and use, studying each equipment type for emissions by process and, where possible, actually measuring the emissions. AMI intends to use the data to optimize internal processes and methods for PFC emission minimization and elimination.

For its part in the MOU, the EPA will develop a clearinghouse of information and data on successful strategies for reducing PFC emissions. The EPA also will conduct a preliminary assessment of the possibility for substitutes to these products and report them to the industry.

AMI is undertaking this voluntary effort to prevent even the low-level PFC emissions from growing to substantial levels as semiconductor manufacturing grows worldwide. The semiconductor industry's reliance on PFCs has increased significantly in the past several years. Based on current trends, this reliance is expected to continue to increase. The three primary factors are:

1. The increasing worldwide demand for semiconductor devices.
2. Increased PFC use in precision manufacturing applications as a result of the increase in semiconductor devices. Substitutes that satisfy the PFCs' unique performance characteristics either have not yet been identified, or are not yet available. Consequently, recycling, abatement, and other control options are still in the early stages of development.
3. Through these voluntary efforts, it is hoped that the United States' semiconductor industry can remain competitive in a global market while seeking environmentally sound solutions to the overall reliance on PFCs.

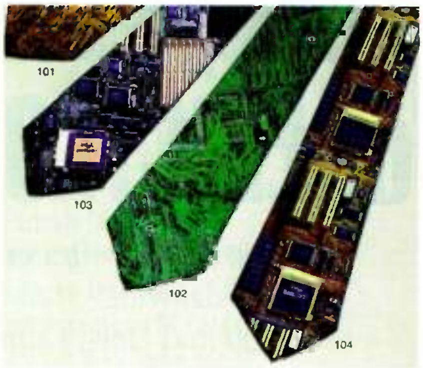
According to David A. Bunzow, AMI's environmental, health, and safety manager, "Although relatively small amounts of PFCs are used by AMI in its manufacturing, we share a commitment to work toward reducing these emissions and, if possible, toward replacing them with compounds that do not trigger global warming concerns or other potential adverse effects. AMI strictly adheres to and often goes beyond federal and state regulations regarding the potential release and reporting of applicable atmospheric pollutant emissions."

For further information, readers are encouraged to contact AMI, 2300 Buckskin Road, Pocatello, ID 83201; (208) 233-4690; Internet: http://www.amis.com.—**MS**

Nifty Gifties For Your Favorite Geeks Are On The Web

I hate to admit it, but I'm a last-minute holiday shopper. I do bake cookies in advance, but I have a tough time finding good gifts for friends and family. People tend to appreciate handmade gifts, hence the cookies, but sometimes I stumble upon things that instantly make me think of someone in my life.

One company that makes it easy for folks who spend lots of time on the Internet is Softwear.Com. The two-year-old company sells a line of high-tech ties, Transistor Sister high-tech jewelry for women, and notebooks with recycled circuit-board covers. The web site, *http://www.software.com*, features detailed photographs and descriptions



of the ties, and supports e-commerce.

The ties are reasonably priced, either $29 or $39, depending on the design. All of the women's jewelry is priced under $20. The notebooks wear $15 price tags.

According to Charles Duff, president of Software.Com, the big challenge in producing the ties is technical in nature. It takes 18 minutes to print a tie, despite using the largest color output plotters. Still, they can only take orders of 300 or less to be cost effective and keep the price low.

The biggest sellers include the gold Pentium tie and the blue Microsoft Natural keyboard tie. One caveat, though, in order to support the design of the tie, the design of the board is not entirely true to life. Forgive them—they're cool ties.

For more information on the gift items, contact Softwear.Com, 714 Ashbury Ave., El Cerrito, CA 94530; (510) 526-6922; fax (510) 526-5387; e-mail: cduff@ix.netcom.com.—**DS**

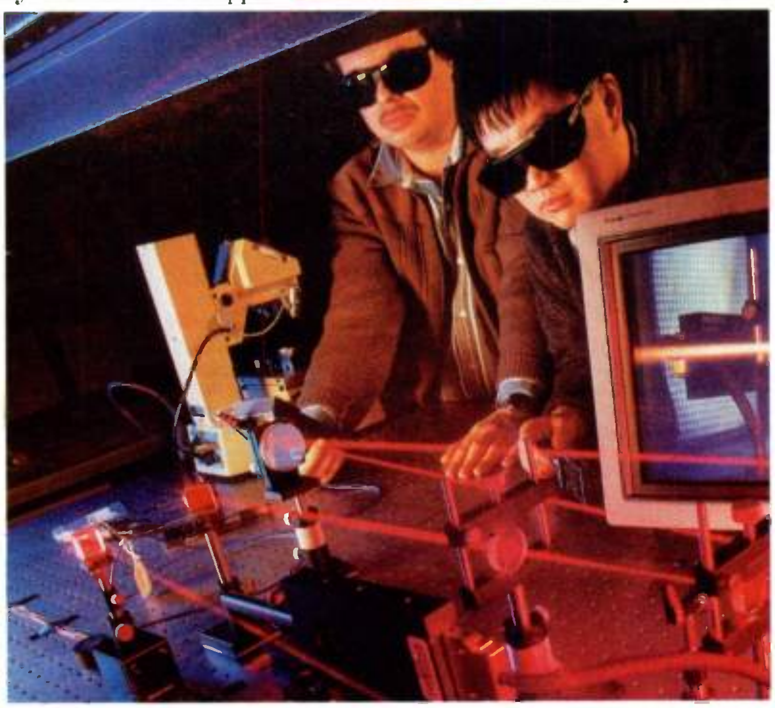
Moving Toward The Light: New Optics Developments Reshaping Electronics

As Optical Technologies Move Into The Mainstream, Innovative Meldings Of Electronics And Photonics Will Bring Changes To Many Electronic Products—And Their Designers.

Lee Goldberg

SPECIAL REPORT

Electro-optic technology is in the middle of an increasingly rapid migration from the laboratory to our living rooms. As the stuff we design gets smaller, faster, and lower-powered, electrons are simply not as efficient as photons for certain types of tasks. Thanks to recent developments in photonic technologies, we can expect to see lightwave-based devices finding many more real-world applications within the next few years. Although the photon has played a leading role in science-fiction movies and novels (e.g., the crystal memory devices of the Krell race in the Sci-Fi movie classic, *Forbidden Planet*), it has remained at the periphery of the average electrical engineer's world.



Art Courtesy of: Toby Richards for NEC Laboratories

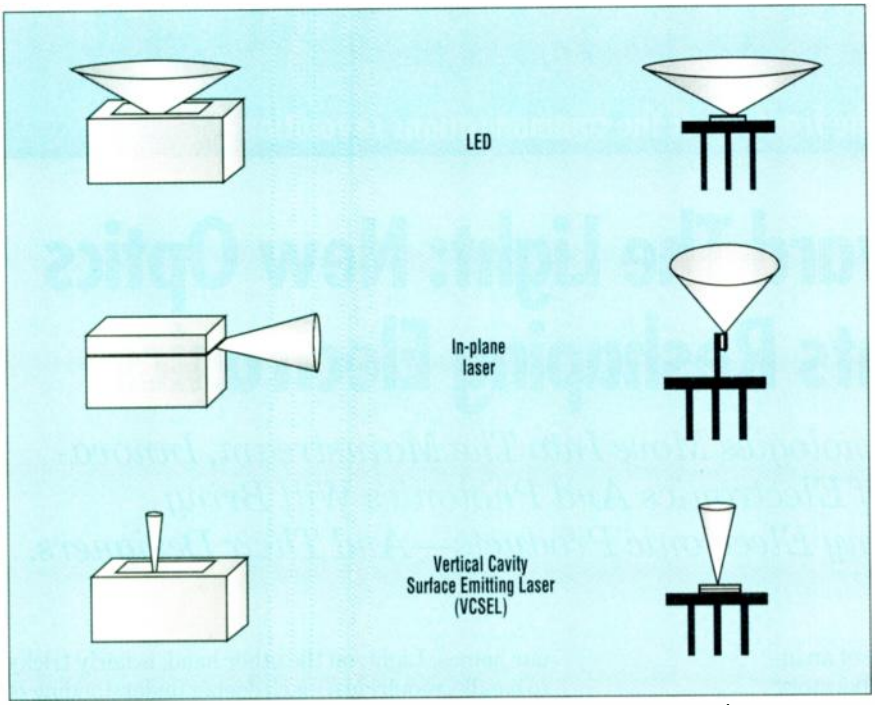
The Apps Gap

For most of this century, the electron has enjoyed the spotlight in control, computing, and communications, while the photon was relegated to playing an important, but supporting, role in indicators, sensors, and fiber-data connections. This application gap owes itself to a number of factors. Perhaps most important is that electrons are relatively easy to manipulate. Long before we discovered quantum theory or even the structure of the atom, we were using electrons from primitive batteries and dynamos to spin motors, send telegraphic messages, and light our homes. Light, on the other hand, is fairly tricky to handle, requiring a much deeper understanding of physics before you can do much beyond filtering a beam or bending it in different directions. Although optical connections have long been the best choice for transmitting high-speed data over any reasonable distance, we have usually relied on electrical devices for their amplification, switching, and termination.

Now, applied quantum theory and advanced materials science are beginning to allow us to perform many of the tricks with light that we have routinely done with electricity. Solid-state lasers, integrated optics, and optical amplifiers are beginning to find their way into applications which were deemed unfeasible than a decade ago. Recent developments such as these will serve to further blur the line between electrical and optical systems design.

Viva VCSELs

In the opinion of Dr. Yao Li, a research scientist at NEC Laboratories, Princeton, N.J., one of these breakthrough developments is the Vertical Cavity Surface-Emitting Laser (VCSEL). Developed in Japan during the mid-eighties, VCSELs form emitters on the surface of a semiconductor. The vertical laser cavities are created by surrounding light-emitting quantum wells with dozens of



1. This series of cross-sections contrasts the edge-based structure of conventional LEDs versus the planar structure of VCSELs.

1/4-wavelength thick layers of film that act as mirrors. Previously, the structures of lasers were formed at a chip's edge, requiring each emitter to be formed, diced, and placed in a carrier separately *(Fig. 1)*. Owing to their planar structure, VCSELs can be produced in higher volumes at a lower cost by employing many of the photolithographic and processing techniques already developed for other types of devices.

Beside their reduced cost, Dr. Li explains that VCSELs have several advantages over previous device structures. The ability to form precisely spaced arrays of light sources on a single chip makes it possible to make inexpensive multichannel, parallel fiber-optic transmitters that don't require the individual placement and alignment of each source. Companies like Motorola Semiconductors are already making 10-bit-wide 850-nm laser arrays that support optical links of up to 1 km in length.

As the speed of traffic between computers and their peripherals hits the multi-Gbit/s range, we can expect to see VCSEL-driven short-haul fiber-optic cables being deployed as 16- or 32-bit-wide data pipelines. In another twist of this concept, NEC is already working on a 64-bit optical channel. It uses a borescope - an optical image pipe, which is a bundle of carefully aligned fibers typically used for looking into tight areas such as jet engines or clogged arteries, to carry 64 bits of parallel data generated by an 8-by-8 monolithic VCSEL array.

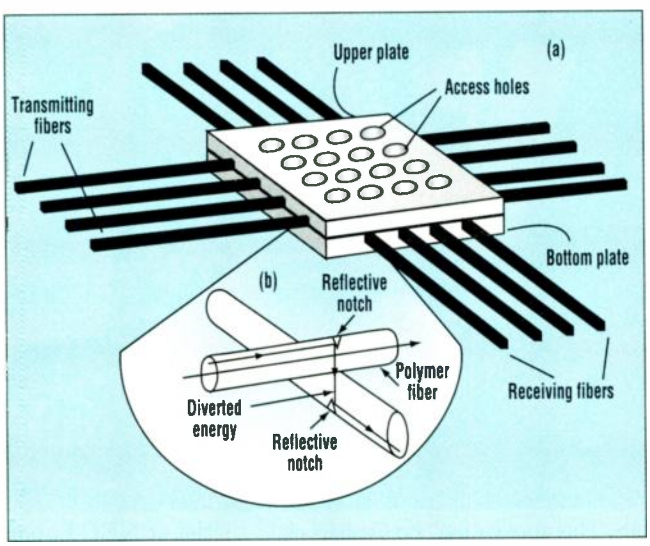
Another advantage of VCSELs is the more uniform light pattern that they emit. Because they are not reliant on a pinched-edge geometry, the emitters can be formed to produce a nearly perfect conical beam. This means that a very simple lens can be used to efficiently direct the light into a fiber for transmission. This gives VCSEL arrays another cost advantage over the more complex lenses required to correct the pattern of conventional emitters.

VCSELs are finding many other uses. In addition to providing low-cost, high-intensity light sources for industrial and automotive applications, monolithic emitter and detector arrays also will become important components in some of tomorrow's optical switching systems.

Polymer Optics

While somewhat less glamorous, the advances that are being made in optical fiber and connection hardware may have even more profound impacts on where and how the technology is used. Glass is great stuff for long-haul fiber runs. It has very low loss and can be made precisely enough to support single-mode transmission, allowing it to carry a signal tens of kilometers before needing amplification. On the other hand, glass fibers are relatively expensive to produce. Worse yet, the tiny, brittle fibers are difficult to cut cleanly or splice, making terminations a fairly expensive, complicated sort of business.

Polymers, at first glance, would not seem to be an ideal optical medium. They are fairly lossy, and are only capable of carrying a signal about 100 meters. Polymer fibers do have many redeeming qualities, however, especially for high-volume, local-area applications. Perhaps of most immediate significance, they are very inexpensive and much easier to handle. Unlike their brittle glass cousins, their softer polymer material can endure tight bends without damage. Eventually, this will help find its way into applications where space is at a pre-



2. A passive crossbar repeater can be easily constructed using signals created in a polymer fiber (a). By notching the fiber with a heated blade at 45°, a reflective surface can be placed in the beam's path (b). This allows a portion of its signal to be diverted through the fiber's wall. A similar notch in a second fiber allows it to capture and direct the beam to a new destination.


CAPTAIN, WE'VE GOT AN ENTIRE SQUADRON OF RAIDER SHIPS APPROACHING FROM THE ZYLINK QUADRANT.
LT. REED, WHAT'D THE G2 REVEAL ABOUT THE RAIDER FIGHTERS?
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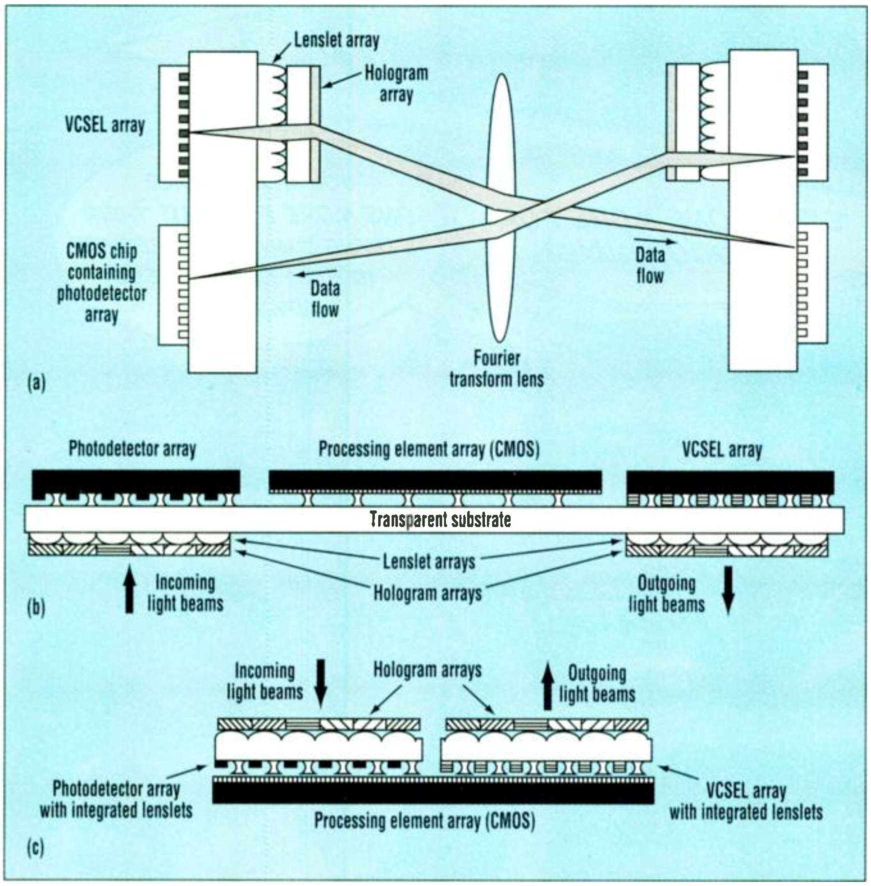
mium, such as chip-to-chip communications. For these reasons Dr. Li, and his associate Dr. Jan Popelek, are devoting much of their time to development of technologies that exploit the unique properties of polymer optical cables.

Among other things, they have discovered that the material's soft nature also allows it to be cut and formed easily, allowing connections to be made using simpler methods in less time. Also, the wider fibers (0.5 to 1.0 mm typically) are easier to handle and require less precision when being aligned with a transceiver. The lower precision of the parts required for terminating plastic fiber may bring the cost of a bidirectional OC-3 (155-Mbit/s) link into the $20 range within the next couple of years. These inexpensive couplers also could provide an optical extension of the IEEE 1394 "FireWire" twisted-pair serial bus, currently being used to link consumer VCRs, cameras, computers, and other multimedia gear. With an ability to carry FireWire's 100- to 400-Mbit/s traffic much further than its current twisted-pair medium, plastic optical cable could be the ideal technology for making room-to-room connections between consumer electronic systems.

Polymer's softness also allows it to be precisely nicked with a heated cutting tool, creating a small reflective surface within part of the fiber's interior. This angled "mirror" creates a "leak" by directing a portion of the light out the fiber's side, which can be coupled to a second fiber *(Fig. 2)*. Depending on how they are cut and placed, these couplings can be unidirectional or bidirectional. Up to 400 unidirectional taps have been placed successfully in a single fiber, making it easy and inexpensive to distribute broadcast signals such as cable television. Bidirectional cross-connect matrices also can be formed. Applications for these devices include passive star hubs in optical networks *(Fig. 2, again)*.

While still in the early stages of development, this "leaky fiber" technology also shows great promise for making computers faster and less expensive. An inexpensive optical backplane could be created using a bundle of notched fibers to distribute parallel data to computing elements at multigigabit rates.



3. The "smart-pixel"-based free-space optical interconnect system under development at University of Colorado at Boulder (a). Lenslets are used to focus the VCSEL transmitter's outputs, while a holographic steering mechanism directs data to a selected detector in the receiving side. The prototype system integrates transmitter, detector, and processing electronics on a transparent substrate (b), but further refinements should allow both optic elements to be directly attached to the processor chip itself (c) to form a compact smart pixel element.

Optical Clocks?

Besides moving data faster within computers, fiber optics also may be used to make the computing elements run faster, using optical distribution of clock signals. Currently, the fastest commercially available computers run with clock speeds approaching 500 MHz. At these speeds, even slight differences in the length or capacitance of a circuit board trace can create a picosecond or more of delay, resulting in unacceptable clock jitter. Even when these problems are solved, the presence of high-frequency clock signals throughout the system only compounds the designer's headaches with their attendant EMI and cross-talk.

Some day soon, however, embedded optical fibers embedded in a computer's pc board may bypass these problems by delivering clock signals to each chip at the speed of light, unaffected by capacitance-induced delays. Even without any other advances in semiconductor technology, optical clocks could make it possible for a supercomputer, or even a high-end workstation to run at cycle speeds approaching a gigahertz.

Smart Pixels?

Another promising way to speed up computer bottlenecks is the optical backplane technology under development at the University of Colorado, Boulder, where Dr. John Neff is working on a free-space interconnect system. Intended as a board-to-board pipeline for connecting high-speed processing elements, the prototype version employs an 8-by-8 "smart pixel" array (SPA). In such an array, each pixel has its own driver, detector, and routing electronics, as well as some signal processing capability.

Each pixel element (PE) in the UC Boulder prototype has its own 1-bit, 20-MHz processor that can perform 16 logic functions and 4 kbits of off-chip RAM. Although they are capable of

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general purpose computing, they were designed specifically for performing signal processing functions such as fast Fourier transforms (FFTs). Depending on the application, the SPA can either serve as a simple pipeline between processing elements, or actually perform some computation tasks on the streams of data it is passing.

An optical interconnect uses two SPAs facing each other, usually at a distance of about an inch. Each SPA has a lenslet array and a holographic optical interconnect element (HOIE) placed over each VCSEL photoemitter. The HOIE is a four-level hologram containing 64 individual phase holograms (one per VCSEL) that diffract, or "steer," the VCSEL beams *(Fig. 3a)*. Although both SPAs are identical, the hologram implements a 2-D, nonseparable perfect shuffle interconnection scheme that permits any two channels in the array to talk to each other.

Since the processes and materials for fabricating VCSELs and photodetectors are not compatible with those used for LSI CMOS logic, three different chips must be assembled to form a SPA. The first SPAs are being fabricated as a hybrid circuit, bonding separate emitter, detector, and processing chips onto a transparent (glass or sapphire) substrate *(Fig. 3b)*. The next generation of SPAs will most likely bond the VCSEL and photodetector arrays directly to CMOS the processing element, creating a much more compact and inexpensive package *(Fig. 3c)*.

Given the fact that the project is heavily funded by the Defense Advanced Research Projects Agency (DARPA), the initial applications for this technology will be for performing the complex signal analysis required to extract images from phased-array and synthetic-aperture radar (SAR). One of the places Dr. Neff expects SPA backplanes to excel is in the "corner turn" function.

Optical clocks could make it possible for a supercomputer, or even a high-end workstation to run at cycle speeds approaching a Gigahertz.

The corner turn problem occurs because each element within an array processor used in digital SARs must exchange intermediate results with every other processor in the array every time it begins processing the data set on another axis (a task of gargantuan proportions that grows as an N^2 function, where N= the number of processors exchanging data). It is not too hard, however, to imagine many civilian applications for optical interconnects. These might include accelerating compute-intensive medical image processing and high-speed video rendering systems, as well as serving as data conduits within fractional-terabyte-class telecommunications switches.

With all the electro-optic advances reshaping the face of computing and communications, you have to wonder about the radically different kinds of products that might soon be possible. Even though *Electronic Design's* crystal ball is currently in the shop for a memory upgrade, we still can get a good idea at what the future might hold by taking a look at the massively parallel, optically switched processor core under development by a new industry consortium.

Putting It All Together

Based out of the University of California, San Diego (UCSD), a team of academic and industry researchers are using a novel combination of advanced electrical, optical, and materials technologies to leapfrog over the barriers that limit today's computing and switching systems.

Today's switches and computers face similar technical barriers to achieving the next level of performance. Surprisingly, many of these bottlenecks are found not in the semiconductor chips themselves, but in the connections between them. It turns out that the propagation delay and capacitive loading in even the most sophisticated printed-circuit board (pc-board) traces can severely impact the execution speed of a processor or switching circuit. Also, the problem compounds as connection topologies get larger and more complex, adding orders of magnitude more signals to overloaded pc boards and backplanes.

Teaming with Irvine Sensors, Costa

For Further Information

If you want to learn more about polymer optics or CdF3-based optical storage, contact the NEC Research Institute Inc., 4 Independence Way, Princeton, NJ 08540; (609) 951-1555.

If our short discussion of optical interconnects caught your attention, you may want to contact the Optoelectronic Computing Systems Center at the University of Colorado at Boulder, Campus Box 525, Boulder CO 80309-0525; (303) 492-7967.

For more information about the free-space optical processor project, contact the University Of California San Diego's (UCSD's) ECE Dept., 9500 Gilman Dr., La Jolla, CA 92093; (619) 534-4943, Internet: http://soliton.ucsd.edu/3doesp/.

Details on the chip-stacking technologies used in the tera-switch are available from Irvine Sensors Corp., 3001 Redhill Ave., Bldg. 3, Costa Mesa, CA, 92626; (714) 444-8840; Internet: http://www.irvinesensors.com/novalog.com/microsensors.com.

More information on the switch's bump-bonded optical I/O transceivers may be obtained from the Honeywell Technology Center, 3660 Technology Dr., Minneapolis, MN 55418.

For further information on detectors, emitters, fiber optics, optical storage, and many related topics, you can visit the publications section of the Optical Society of America's web site at http://www.osa.org, or contact them directly at 2010 Massachusetts Ave., N.W., Washington, DC 20036-8130; (202) 223-8130, fax (202) 223-1096.

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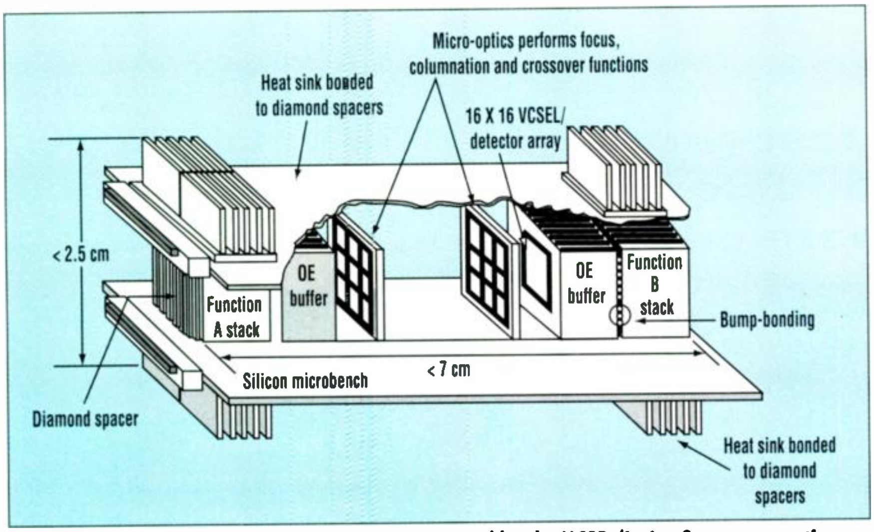

4. The free-space optical interconnect system proposed by the UCSD/Irvine Sensor consortium employs the optical transpose interconnection system (OTIS) in its switching system. The 8-by-8 free-space optical switch uses a pair of VCSEL/detector arrays, rotated 90Υ from each other, allowing a direct beam path between any row and column. The switching architecture will initially be used to connect processor elements in massively parallel computers, but it also can form the heart of a terabit-level switching network.

Mesa, Calif., and Honeywell Corp., Minneapolis, Minn., UCSD scientists Dr. Philipe Marchand and Dr. Sadik Esner are currently developing a switching structure that uses a combination of stacked chip and 3-D interconnect technology to reduce signal paths lengths, and a free-space optical switch to reduce connection complexity.

Initially intended for use as a high-speed array for performing fast Fourier transforms, the proposed unit will have its processor chips bonded one on top of another to form a stack. Each chip in the stack communicates with its neighbors using electrical interconnects deposited on the side of the stack, greatly reducing the length of the runs. This does not, however, support the density of a set of global connections between all processors required for many complex array operations.

To achieve this complete connectivity, each processor will be connected to a node on a 16-by-16, VCSEL-based free-space optical interconnect (FOSI) matrix that is bump-bonded to the processor chip stack *(Fig. 4)*. Depending on the processor it wants to talk to, the transmitting processor selects one of a column of 16 emitters. A holographic beam steering network, known as OTIS (Optical Transpose Interconnection System) is used to direct it to the desired receiving node on a second FOSI element placed about 4 cm away.

On the other side of the assembly, a second VCSEL/detector array receives the incoming beam and sends it to a high-speed electrical switch matrix built into a set of stacked chips. The signal is then passed back to the appropriate VCSEL transmitter and on to the detector associated with the destination processor. While it may seem complicated, this free-space-based architecture manages to eliminate the N^2 complexity problems that give designers of large, multiple-element systems such trouble.

The elimination of wiring not only does away with most of the propagation delays associated with electrons, it also permits a dense connection topology that might not be physically possible otherwise. As Dr. Marchand is fond of saying, "The light beams don't have to worry about bumping into each other." Once the technology is proven on the 16-by-16 test bed, Marchand is confident that the architecture can be practically scaled to implement switching structures of 64 by 64, 128 by 128, or even larger.

Of course, many obstacles remain to development of even this simplified prototype. Several challenges surround the construction of the ultra-dense stacked chip arrays that will form the processor and switching matrices. Already employed for high-density memory and processor applications, chip stacking is cutting-edge but nothing new. In this case, however, each processor chip is expected to dissipate around 5 W, creating one very hot little cube! To get the heat out to the edge of the assembly, each chip will be interleaved with a thin slice of diamond, providing a very efficient thermal path. The edges of these heat wicks will be bonded to a conventional heat sink and cooled by a simple forced-air system.

The actual assembly of the unit will also present its own challenges. In a system with such close tolerances, alignment of each component could be a difficult, time-consuming operation. Dr. Marchand explains that the consortium is currently experimenting with techniques that will enable them to create a micromachined silicon optical bench that will serve to hold the elements of the system in alignment. Wherever possible, self-keying of critical alignments will be used, but new techniques for mechanical fine-tuning also are under development.

Connections with the outside world represent another major hurdle. Rather than use wires to get data in and out of the processor array, the team chose to use a fiber optic bundle that will be coupled to a series of emitter/detector pairs. Developed from commercial technologies by Honeywell, Minneapolis, Minn., these optical transceivers each will be capable of handling 1-Gbit/s traffic. To save both space and connection distance, the optical I/O chips will be bump-bonded to connections printed on the exterior of the chip stacks.

While the first application will be to demonstrate the feasibility of constructing a fast Fourier engine, the same architecture can be easily modified to function as a massive telecommunications switch. Conceivably, a 32-by-32 switching array would have a theoretical capacity approaching a terabit/s. Not bad for a device expected to be not much bigger than a cellular telephone!

Optical Memories: Almost Reality

While 3-D optical cube memories were jokingly alluded to earlier, they are no longer simply in the realm of science fiction. The technology of the Krell race may soon be upon us, if developers from NEC and several other research organizations have their way.

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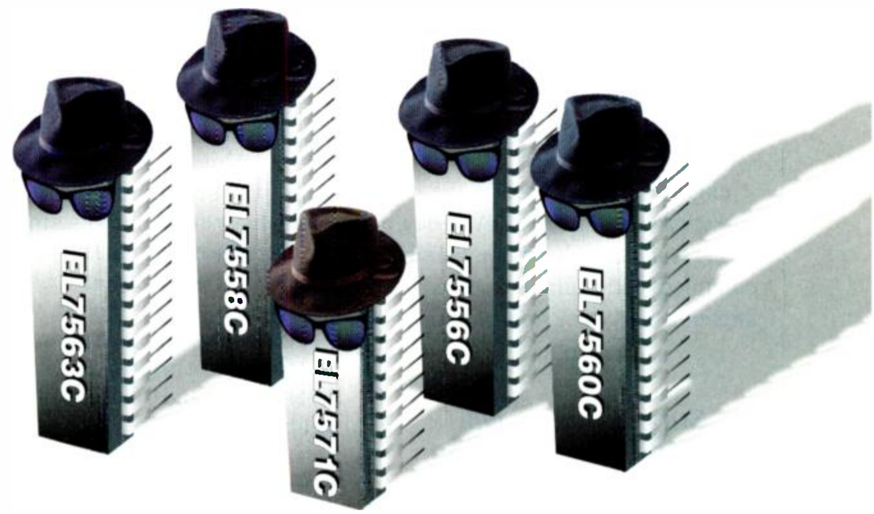

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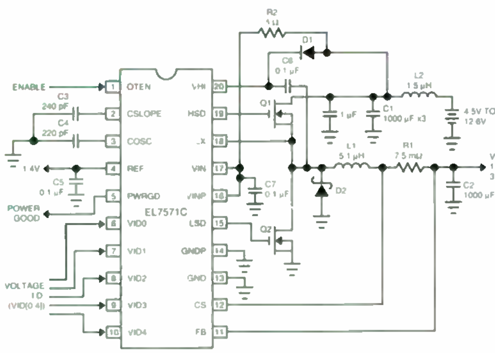

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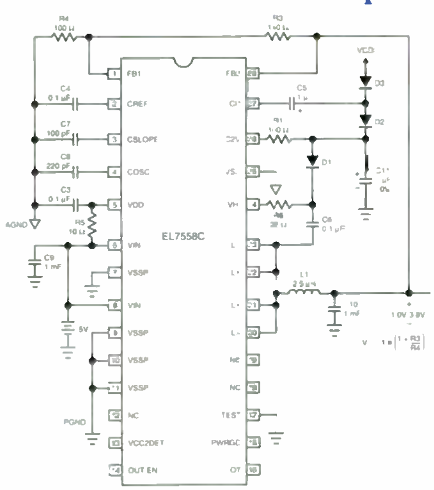

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According to Ian Redmond, a scientist at NEC's Princeton, N.J., research facility, most optical storage systems under development today use a relatively simple principle. Like other holography apparatus, they employ two light sources, an unmodulated reference beam, and a modulated data beam. When the beams are swept across the storage medium, the heat from the lasers creates small alterations in the crystalline structure.

Once the beam is gone, the resulting disturbances are frozen within its structure like any hologram, leaving a 3-D trail of interference patterns representing 1's and 0's. Readout is accomplished by sweeping the reference beam along the same path. Using different writing angles, multiple pages can be stored. In theory, a cubic centimeter of optical medium could store 10 to 50 Terabytes of data. In practice, however, it's a whole bunch more complicated, requiring some very creative thinking on the part of some of the best materials scientists, physicists, and electrical engineers.

Currently, many of the problems with optical storage center around the characteristics of the storage medium. Much like Thomas Edison's struggles to find a durable filament for his incandescent light bulb, scientists are hard at work examining the properties of hundreds of materials. Their goal is to identify crystal compounds which are stable enough to hold data at near-room temperature, but still susceptible to alteration using relatively low energy levels. Toward this end, IBM's T.J.Watson Labs have just completed a landmark effort to catalog and evaluate the read and write characteristics of a large group of candidate materials. Their next step will be to evaluate a number of potentially promising read/write techniques.

Most materials in use today need very low temperatures to operate. While early devices needed to hover around absolute zero, researchers have found materials that could be run at much warmer temperatures. NEC, for example, is working with cadmium fluoride, a substance that operates well at a relatively toasty −70° C. NEC believes that CdF_3 offers many advantages over the lithium niobate crystals being used in most E/O storage systems today. It seems that CdF_3 has a higher sensitivity, allowing the use lower-powered lasers. It also maintains its refractive differences better after stimulus, with more distinct changes , allowing higher densities and smaller angular differences between pages.

Another serious problem that NEC researchers are tackling is the fact that reading the memory also tends to erase it. It seems that even passing a lower-powered read beam through the crystal tends to slightly re-melt the structure and degrade the data pattern. Data in current systems can survive around 10,000-to-100,000 read cycles before it fades away like the fur on a well-loved Teddy Bear. Nevertheless, most authorities are hopeful that this problem can be overcome, perhaps by using different frequencies for read and write.

Since current technology does not allow a memory crystal to be selectively erased and rewritten, the first practical optical storage units will probably function as much like today's optical WORM (write once, read many times) drives, only holding thousands of times more data.

Even before the properties of the storage media are sorted out, engineers are already working out read/write mechanisms that will permit access to multiple pages of data. Candidate technologies for beam-steering include LCD optical modulators, VCSEL arrays, and MEMS-based moving microreflectors. Chances are that within the next five to ten years, we will begin to see storage units based on the work being done today.

This Just In...

Many others have recognized the potential of OE storage and are scrambling to develop their own technologies. While details are still sketchy, at least one consortium is attempting to develop an optical storage technology based on organic compounds that operate at near-room-temperature conditions. Without putting his life at risk, this correspondent can disclose no further details. Stay tuned to this section for the inside scoop some time early next year.

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Operating at 155 Mbits/s, the VSC7902 is intended for single-ended applications, while the VSC7903 comes in a dual-ended version. The 622-Mbit/s VSC7911 and VSC7912 have single and differential outputs, respectively. Applicable for SONET and SDH transmission systems, optical transceiver modules, and other demanding applications, the transimepdance-amplifier topology provides high sensitivity and bandwidth. The simplified die format and on-chip 50-Ω output matching circuits simplify design and layout issues.

Available now, the VSC7902 and VSC7903 cost $8.00 in lots of 10,000. The VSC7911 and VSC 7912 cost $25 in similar quantities.

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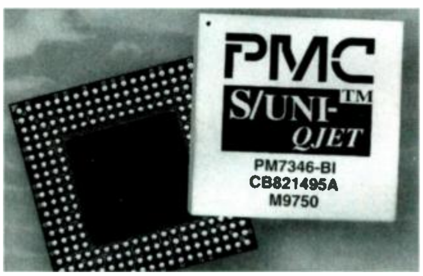
Versatile Quad-Port Framer Processes PPP, Frame, And ATM Traffic At T3/J3 Rates

Intended for use in high-density port adapters in applications such as remote access concentrators, Frame Relay switches, ATM switches, and DSL access multiplexers (DSLAMs), the PM7346 S/UNI QJET is a four-channel framer/processor. It can support Frame Relay or PPP traffic at J2, E3, and T3 rates, as well as perform ATM cell processing.

The QJET reduces component count, power requirements, and cost-per-channel in high-density applications by providing four J2 (6.3 Mbits/s), E3 (34.4 Mbits/s), T3 44.7 Mbits/s), and four ATM cells on a single device. It can be independently configured on a per-port basis. Programming options include an ATM channel device, or as a packet processor interface, providing a four-channel solution for J2 Frame Relay, J2 ATM, E3 ATM, E3 Frame Relay, T3 ATM, and/or T3 Frame Relay.

As an ATM physical-layer device, the S/UNI-QJET's internal framer handles T3, E3, and J3 rates in conjunction with other PLCP-framed or direct cell-mapped ATM processors. In the receive direction, the ATM cell processor performs cell descrambling, HCS error detection, idle cell filtering, and header descrambling, as well as counts both idle and assigned cells on a one-second basis. It supports a 50-MHz, 8- or 16-bit wide UTOPIA Level 2-compliant interface with parity support and multi-PHY control signals. For each channel, rate decoupling between the line and ATM layer devices is provided by a four-cell FIFO in both transmit and receive directions.



As a Quad J2/E3/T3 framer, the device can generate gapped transmit and receive clocks. This makes possible a glueless interface to a data-link-layer device that accesses payload data bits only. It provides integral transmit and receive HDLC controllers, with a deep 128-byte FIFO, that process data link messages.

If its internal framers are bypassed and only the cell processing blocks are activated, the QJET can be used as a Quad ATM cell delineation device. In this mode, rates of up to 54 Mbits/s can be supported on each channel. In addition, the processor can be configured to provide a quad cell processor for direct connection to available ADSL modems.

The CMOS device operates on 3.3 V and has 5-V-tolerant inputs. Housed in a compact 27 by 27 mm square 256-pin SBGA package, the PM7346 S/UNI QJET will be made available late in the fourth quarter of 1997. Pricing will be $185 each in quantities of 5000 pieces.

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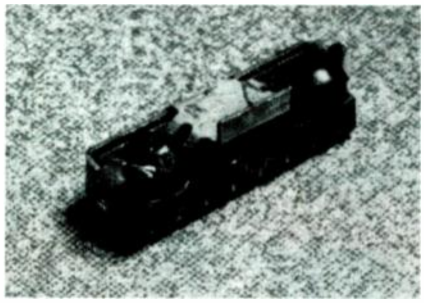
(continued on page 78)

PRODUCT FEATURE

(continued from page 76)
Mbits/s) and medium-range (up to one meter) links, while its companion is targeted at applications requiring shorter link distances (20 to 30 cm) and slower data rates (115 kbits/s). Both parts are able to operate on supplies as low as 2.7 V and have an extensive array of power-management features.

Targeted at mobile, handheld products such as sub-notebook computers, personal digital assistants, and imaging equipment (e.g., digital cameras and image printers), the HDSL2100 combines a low 5.3-mm profile with 4-Mbit/s speed. This high data rate makes it practical to design equipment that can exchange high-resolution electronic photographs, digital images, large databases, and other files over a low-power infrared link.

The transceiver's compact form factor makes it easy to incorporate it into today's ultra-small "slimline" laptop computers. Operating in compliance with the IrDA physical-layer specification 1.1, the transceiver's package also contains an integrated EMI shield This helps to ensure reliable IR link operation when the notebook computer is being used near RF-generating equipment, such as cellular phones.



The HDSL2100's variable-output power feature is an advanced energy-management tool that can help stretch the limited battery capacity available in most compact applications. Much like a cellular phone, the transmitter can adjust its power to the minimum level required to maintain reliable transmission. This allows LED drive currents as low as 35 mA at close distances. Even at its maximum range, the device only draws 350-mA peak drive current.

Among the other features included are a single-receive output option and a mode-select pin to switch between the unit's slow speed range (9.6 to 115 kbits/s) and its high-speed mode (0.576 to 4.0 Mbits/s). Prototype samples of the HDSL2100 are available now upon request.

Also sampling now are prototypes of a new ultra-compact IrDA transceiver, believed to be the world's smallest device of its kind. Intended for palmtop applications in pagers and cellular phones, it employs new packaging technology to achieve the title of smallest commercially available product of its kind.

The tiny device meets the just-approved IrDA physical-layer low-power option standard revision 1.2a, which was specifically developed to meet the needs of short-haul, medium-speed applications with severe power limitations. Capable of transfer speeds reaching up to 115 kbits/s, it provides cellular phones, pagers, and small handheld computers with the ability to "beam" electronic files containing "business cards," telephone book and calendar entries, e-mail, and real-time audio between devices.

The transceiver's package measures 2.5 mm high, 8.0 mm wide, and 2.85 mm deep. This was achieved by using a packaging technology called sheet casting. It also features integrated EMI shielding and an ultra-low power (50 nA) standby mode. Operating current for the device is a very low 25 mA.

Both of these parts, available in production some time in January 1998, are sampling now. Pricing for the HDSL 2100 will be under $4 each, when ordered in large production quantities. The ultra-small transceiver will sell for under $2 in similar volume quantities.

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After much thought and discussion, our editors have developed a new tag line that is about as direct and to the point as one can possibly get. It describes who we are and what we do. These four words tell our readers and advertisers what *Electronic Design* is all about:

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STANDARDS WATCH

DVD And 1394: Perfect Together

Richard Nass

I've been saying it for a while now—the success of the IEEE 1394 bus will be closely tied to the success of DVD. The next killer application for the PC will have something to do with video. It may be videoconferencing, or some sort of playback, akin to the Gateway Destination. But it will definitely involve video. What better medium to transport that video than the 1394 bus, with its current 400-Mbit/s specification, with a roadmap going to 1 Gbit/s and beyond. And what better medium to store the information, but DVD, with its 4.7 Gbytes of capacity, with much higher capacities coming shortly.

Also known as Firewire, the 1394 bus signals a convergence between PCs, consumer audio, and video products. Sony has been bundling a 1394 interface on its video cameras for a few years. In fact, Sony now ships three 1394-compliant camcorders—the DCR-VX1000, DCR-VX700, and DCR-PC7. However, there isn't much that the camera's 1394 link can connect to. Adaptec Inc., Milpitas, Calif., offers a board-level product that connects 1394 to a PC's PCI bus. The board, designated the 8920, will sell for $299 when it becomes available next month. It contains one external 1394 connector.

IEEE 1394 employs small, inexpensive cables and simple connectors to carry multiple channels of digital audio and video data and control information to a series of interconnected devices. The easy connection method is further enhanced by "hot-plug" and "plug-and-play" capabilities. Hot plug means that a peripheral can be connected even when the system is powered on, while plug-and-play means that the system needn't be restarted to configure the newly connected peripheral. The system will self-configure the new device. This is a giant step forward in the march to make a PC operate like most pieces of consumer electronics. (Can you imagine having to remove the cover of your stereo receiver to plug in a new tape deck?)

To enable a 1394 connection, two ICs are required—a physical layer and a link layer. The physical-layer chip is a mixed-signal device that supports multiple 1394 ports, and includes logic needed to perform arbitration and bus-initialization functions. The link layer transmits and receives the data packets.

One beauty of the 1394 is that it offers peer-to-peer communications, meaning that two peripherals can communicate with each other without routing information through a central node. For example, two camcorders can connect, communicate, establish a logical video connection, and dub video data from one another directly. But, using the PC as the "middle man" could simplify the connection with video-editing software and a user interface to simplify the function being performed.

By the looks of the 1394 developments, it's now up to the DVD players to make this interface-storage medium marriage work. The DVD-ROM standard seems to be a stable one. Walk through your local video-rental store and you'll see that movies are now shipping on DVD disks. The current crop doesn't offer much more than a similar VCR tape, but they will as film producers get a handle on what to do with the space that's available on a disk.

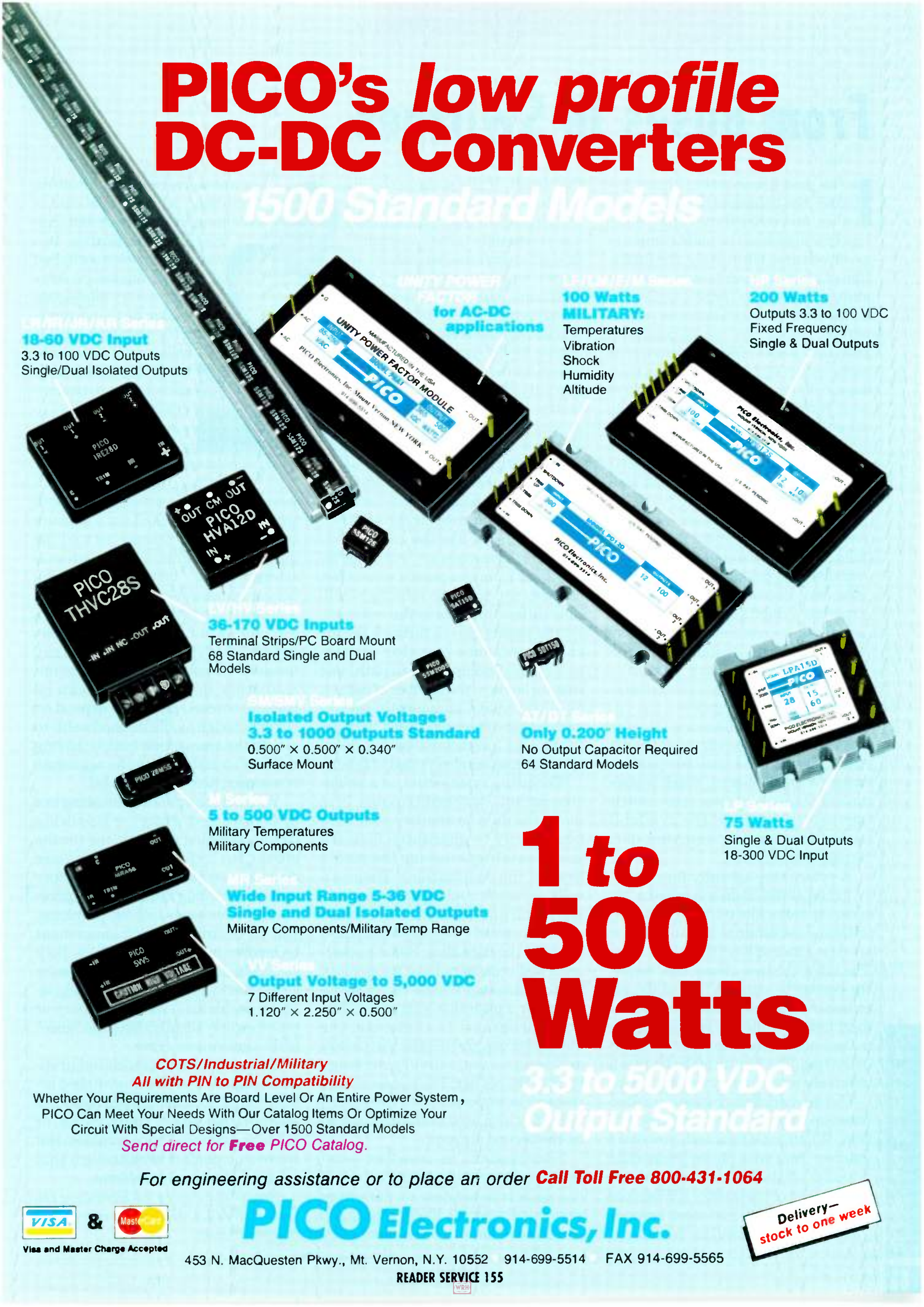
There's no sense shipping a movie on a DVD that doesn't offer anything more than what's available on a VCR tape. There must be a compelling reason to buy the disks as well as the players. Some enhancements that will soon be available include better sound, multiple camera angles, different-rating versions of a movie, multiple languages, character information, even different endings for individual tastes.

That's all well and good, but it's DVD-RAM, with the ability to write to the disk as well as read, that really excites me. As of now, two "standards" were in the works, each backed by a significant group of industry players. In addition to the write capability, each version offers a capacity far beyond traditional CD-ROMs.

Panasonic Computer Peripheral Company, Secaucus, N.J., announced that it will begin shipping DVD-RAM products next month. The company is in the camp with the DVD Forum members, whose offering will store 5.2 Gbytes on a double-sided disk (a 2.6-Gbyte single-sided disk also will be available). The company predicts that over 80 million DVD products will ship by the end of the decade.

Panasonic's drive, the LF-D101, will sell for $799, with the media costing $39.95 for 5.2 Gbytes and $24.95 for 2.6 Gbytes. And, the drive can read from disks written in most standard formats, including DVD-RAM, DVD-ROM, CD-ROM, CD-R, and CD-RW.

While the Panasonic drive is a leap forward in technology, it does lack a feature that I feel is essential to its success—a 1394 connector! Instead, the designers of the LF-D101 chose to employ a SCSI interface; probably because the installed base of SCSI host adapters far outweighs the installed base of 1394-enabled PCs. However, the move does seem fairly short-sighted. It's unlikely that we'll see cameras shipping with SCSI connectors on them, and as stated previously, the 1394 cameras are already here.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READER SERVICE 155

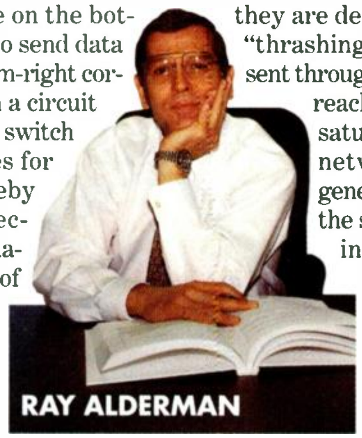
From Buses To Switches

In the past few months, I have discussed the behaviors of buses, rings, cubes, and other three-dimensional topographies used to build computer architectures. Ultimately, the limitation of all those architectures is their ability to scale to large numbers of nodes without degradation in performance. Buses can't scale past four processor nodes efficiently, even with cache-coherent protocols. Rings start degrading in performance somewhere near six or seven nodes. Cubes and other 3D architectures saturate at eight or more nodes. So, how can we build an architecture that can scale to a large number of nodes and still have a high level of performance?

The answer is crossbar switches. Two basic switch fabrics are used to build a computer architecture: circuit-switched and packet-switched crossbars. But, like buses and rings, each structure exhibits some aberrant behaviors that create scalability problems. Any circuit-switched architecture has three primary latencies: connection (the address cycle), disconnection (the "tearing-down the circuit" latency), and blocking (blocked because another node is using the circuit). The same is true for packet-switched architectures, which replace those latencies with new ones: switching (selecting one of the available paths) and routing (moving data through those paths).

A typical topography for circuit-switched architectures is called a "fat tree." It looks like a Christmas tree, with one crossbar at the top, two at level two, four at level three, and so on. The taller the tree grows, the "fatter" the bottom becomes. A typical six-way crossbar uses four paths to connect to local nodes, while the remaining two paths would connect to other crossbars in the tree. The beauty of the fat tree is that it allows scalability to many nodes.

Circuit-switched crossbar architectures operate like the telephone system. When making a call, you dial a number from your phone (connection latency). If the line is busy, you are blocked (blocking latency). When you complete the call, you must hang up (disconnection latency) to "tear-down" the circuit. If the node on the bottom-left corner wants to send data to the node at the bottom-right corner, you must establish a circuit through every crossbar switch between the two nodes for each transaction, thereby multiplying the connection and disconnection latencies by the number of crossbars between the two participants. The fatter the tree, the greater the latency. The trick to making an efficient fat tree is to localize the data-sharing between nodes through the least possible number of crossbars.


RAY ALDERMAN

Packet-switched architectures, however, work like the Internet. If two e-mail messages are sent at different times from one person to another, chances are that the messages will take different paths in the network. As the packet moves through the architecture, each crossbar creates switching (finding an open path) and routing latency (the number of paths it must traverse). Consequently, packet-switched architectures aren't very deterministic (predictable packet delivery within a bounded period of time).

The primary objective of a primitive packet-switched crossbar is to move the data to another point, not necessarily to guarantee forward progress (always moving the packet toward the destination). Theoretically, a packet could go into the network and not reach its destination unless forward-progress algorithms monitor the data flow. Some packet-switched crossbars have no memory to store messages while the crossbar waits for a path that guarantees forward progress. In that case, the blocked crossbar deletes the packet and sends a nondelivery message back to the sender. The packet is then re-sent in hope that the necessary paths are available to the destination on the second attempt.

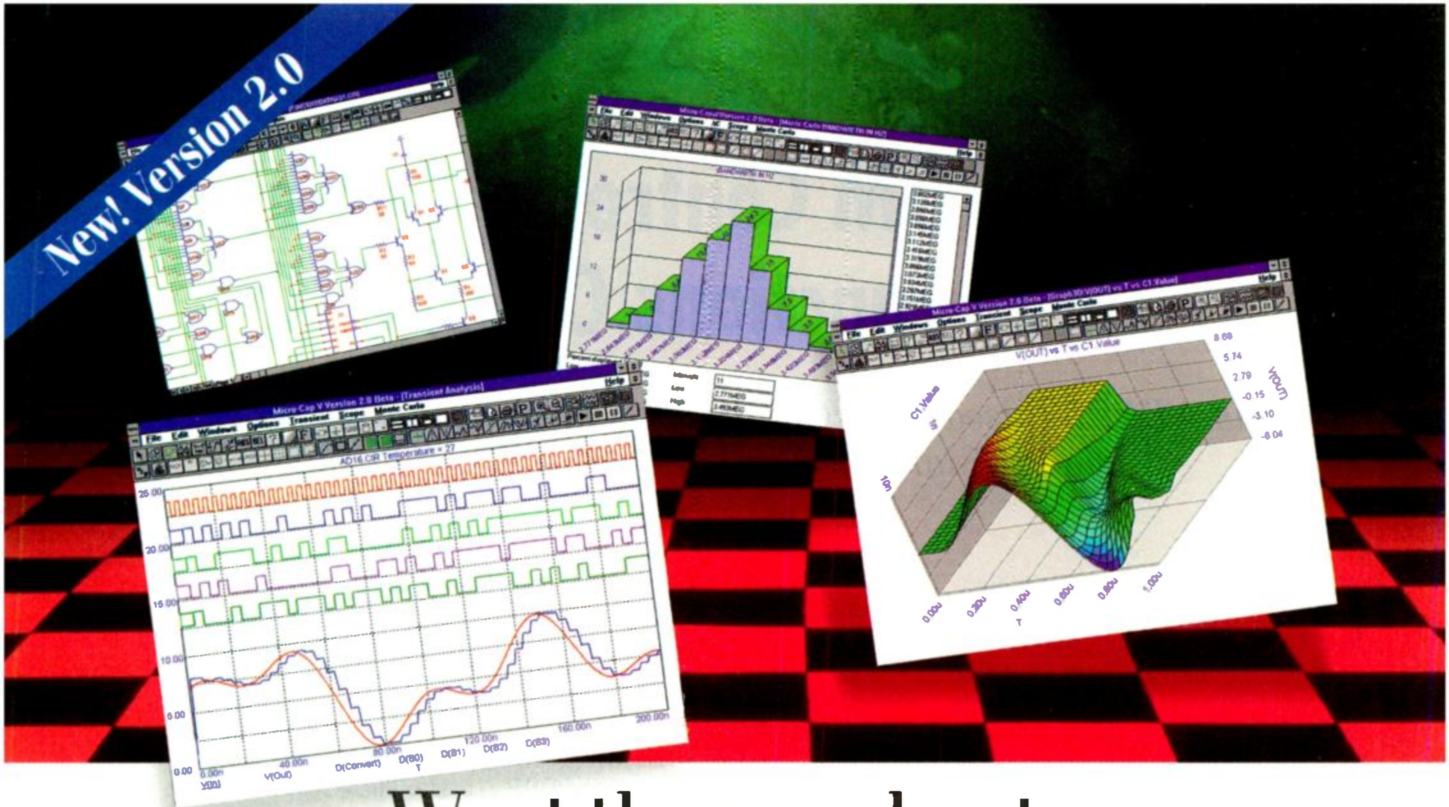
Some applications cause "hot spots" in the packet-switched architecture. If one node is dependent on data from several others, it's likely that many packets will have to be re-sent before they are delivered. This results in "thrashing" where lots of data is sent through the network, but little reaches its destination. In a saturated packet-switched network, deleted packets generate a retry message to the sender, further saturating the network until it collapses. To eliminate the problem, memory is added to each packet-crossbar switch to store data until paths are available.

This "network meltdown" behavior can't happen in a circuit-switched network, where the worst-case scenario is that nodes are blocked until ongoing transactions are completed and the paths are available. This situation is called "lockout." Before any packet can be sent in a circuit-switched network, a complete path between a sender and a receiver must be established. So, circuit-switched crossbars don't need any memory for packets that can't be immediately delivered. Ultimately, packet-switched networks depend on having enough available bandwidth to satisfy the transaction load, or having memory available when the aggregate transaction limits are exceeded.

Whether experiencing thrashing in a packet-switched network or lockout in a circuit-switched network, the results are similar: architectural performance degrades precipitously. Adding memory reduces thrashing and instituting priority protocols eases lockout problems. But these are latency management techniques, not complete solutions. Both techniques are similar to adding cache coherence to a bus to solve blocking-latency problems—adding memory or priorities only slightly raises the "knee" of the performance curve.

Even with their associated problems, packet- and circuit-switched architectures can scale to more nodes in a system than buses, rings, cubes, or other nonswitched topographies. But there's no perfect architecture that solves all the latency problems.

Ray Alderman is the Executive Director of VITA. He can be reached at exec@vita.com.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PRODUCT INNOVATION

24X CD-ROM Controller Combines Three Functions On One IC

This ATAPI-Based Chip Combines A High-Performance Servo, A Digital-Signal Processor, And A Block Decoder.

Richard Nass

OEMs always want higher integration. Whether it's a system, a board, or even a chip, they always want more functionality in a smaller package. Designers of CD-ROM drives are no exception. The drives continue to shrink in both size and weight—features that grow in importance as the drives migrate to portable platforms.

To help build smaller and lighter CD-ROM drives, designers at Oak Technology Inc., Sunnyvale, Calif., developed a highly integrated drive controller. The company's OTI-9325 is a three-in-one IDE/AT Attachment Packet Interface (ATAPI) CD-ROM controller. ATAPI is an extension of the IDE/ATA interface. It allows a DVD or CD-ROM drive to share the host PC's ATA bus with existing drives.

The 9325 chip combines a servo, a digital-signal processor, and a block decoder *(Fig. 1)*. The part employs DSP techniques wherever possible to minimize the amount of analog circuitry required. The only functions that are still handled in the analog domain are a comparator and a digital-to-analog converter (DAC).

The device supports 1X through 24X disk speeds. Programmed I/O (PIO) Mode 4 and Multiword DMA Mode 2 is supported. Multiple constant linear velocity (CLV) speeds can be handled, from 1X to 16X.

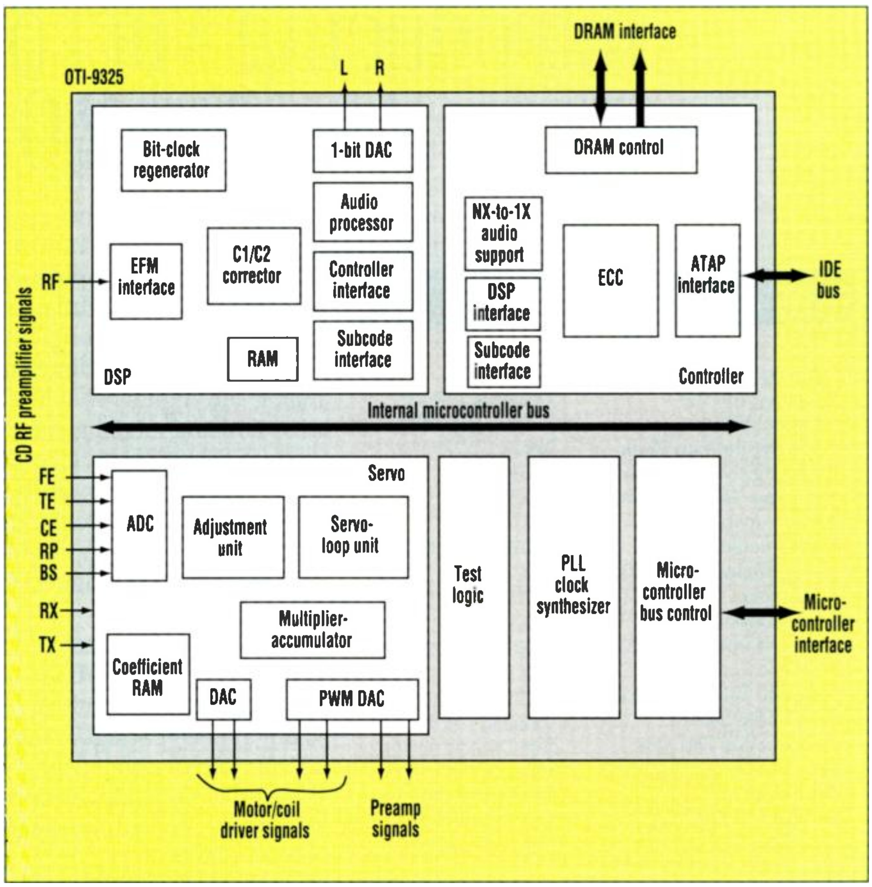
Keep It Quiet

Minimizing the amount of analog circuitry increases immunity to system noise. The analog circuitry of both the DSP and the servo offer a high level of accuracy. In addition, the DSP design reduces the C1/C2 error rates and increases the seek time and accuracy. The 9325 maintains a high level of compatibility with existing software by employing Oak's ATAPI block decoder, the OTI-912. By using this functional block, high-performance data throughput is maintained without compromising error-correction effectiveness.

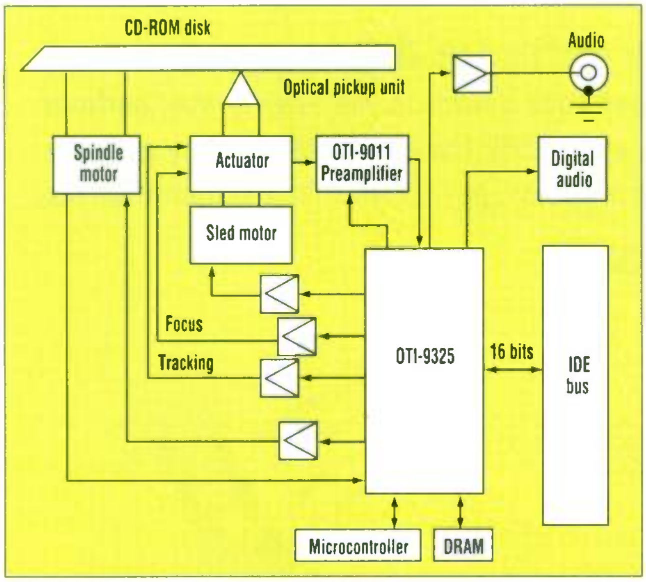
The DSP block of the chip converts the analog RF data received from the preamplifier into digital data. The data is then eight-to-14 modulation (EFM) encoded and C1/C2 error-corrected. The DSP takes advantage of an advanced data-slicing technique, as well as digital asymetry control. Because the asymetry-control loop is done digitally, it offers easy programmability for frequency and gain.

The data-clock recovery section incorporates a digital phase-locked loop (PLL), which enables a controlled response to defects, thereby resulting in higher accuracy and a faster recovery specification. Unlike an analog PLL, the digital PLL is less susceptible to noise and doesn't require external parts. These features result in higher accuracy and faster data recovery.

When employing the 9325, the only major function that's needed to build a complete drive is a preamplifier *(Fig. 2)*. There's a direct connection to a microcontroller, memory, and a 16-bit connec-



1. The OTI-9325 CD-ROM controller is a three-in-one part that combines a servo, a digital-signal processor, and a block decoder. All that's needed to build a drive is a preamplifier.



2. A CD-ROM can be built by connecting the 9325 IC to an external DRAM buffer memory and a local microcontroller. A 16-bit ATAPI host interface makes for an easy connection to the host system.

tion to the IDE bus. The fast-page-mode of EDO DRAM can be employed. Segmented memory is supported for sophisticated caching schemes.

The parts count is further reduced by employing a single 33.8688-MHz crystal. Also, system design can be simplified by employing the OTI-9011 preamp. A single- or triple-beam optical pickup unit (OPU) can be used.

The 9325's servo block controls the optical pickup focus and tracking, the spindle-motor speed, and the sled movement. And the IC offers an improved focus and wobble tolerance. The only portion of the servo loop not handled digitally is the I/O. Interfacing to those signals is done by integrated analog-to-digital (ADC) and DAC elements, resulting in higher resolution and sample rates than previous controllers. The internal digital filter, gain, and constant-parameter functions also have been implemented with a higher degree of precision. Offset, balance, and gain calibration are automated for the focus and tracking servo loop. These features result in a one-track reseek after detection of a target block.

The chip is fabricated on a low-power, 0.35-µm, 3.3-V process. It's housed in a 160-pin PQFP. The part is tolerant with a 5-V I/O. Enhanced power-management modes help further reduce the chip's power consumption.

PRICE AND AVAILABILITY

The OTI-9325 three-in-one IDE/ATAPI CD-ROM controller is available immediately. It sells for under $10 each in lots of 10,000.

Oak Technology Inc., 139 Kifer Ct., Sunnyvale, CA 94086; (408) 737-0888; http://www.oaktech.com. CIRCLE 528

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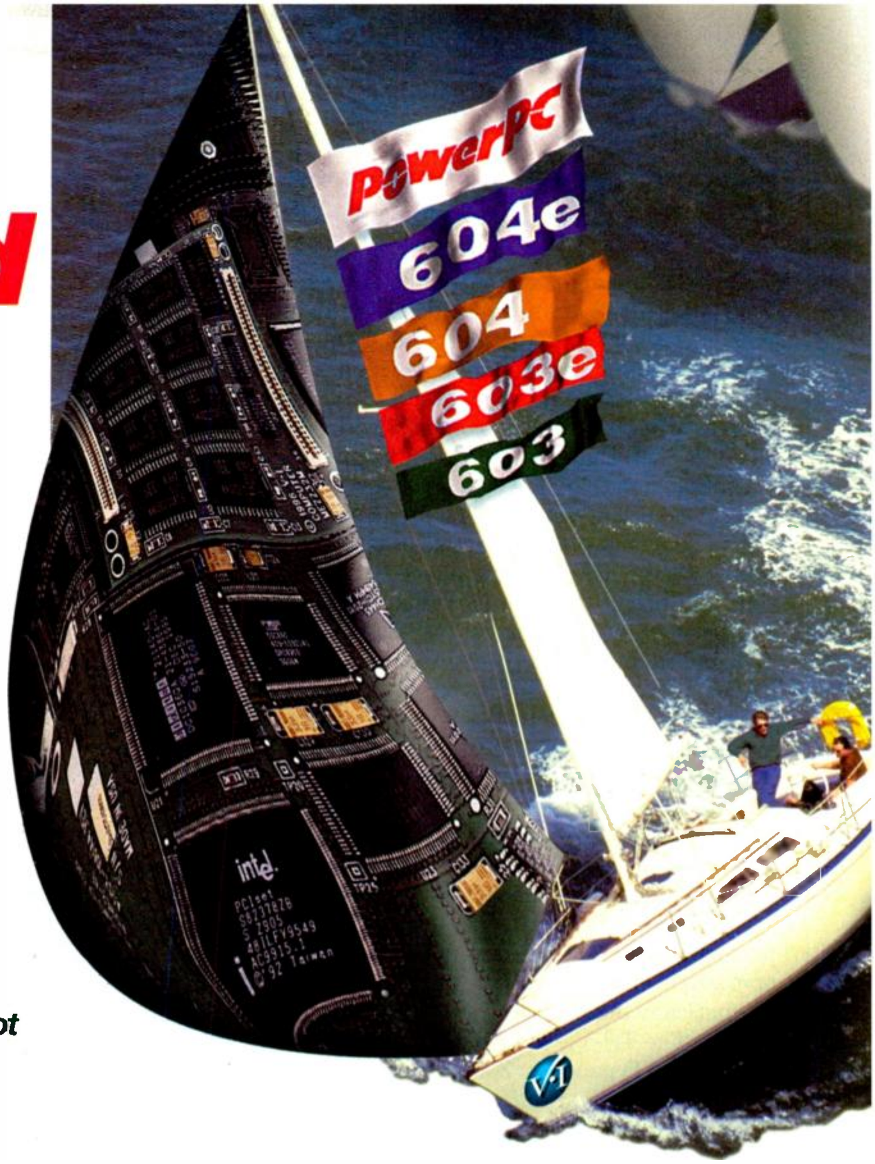

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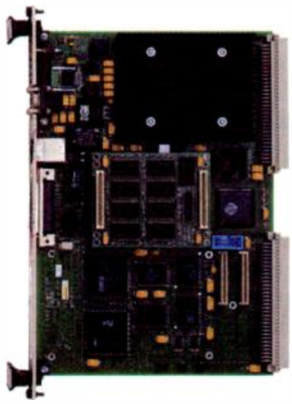

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READER SERVICE 172

WHAT'S ON BOARD

The picoJava processor core, developed by Sun Microsystems, Mountain View, Calif., has been licensed by Fujitsu Ltd., Tokyo, Japan, and its subsidiary Fujitsu Microelectronics Inc., San Jose, Calif., for use in systems such as web appliances, home and mobile communications, and computing devices. The picoJava I core will be incorporated by Fujitsu into its own picoJava-based processor designs that the company with use internally and offer to the merchant market. Fujitsu's low-power technologies, together with the optimized execution of native byte code by a picoJava I core, helps extend battery life and save on code memory. The company intends to capitalize on these capabilities and incorporate the core into consumer and communication devices such as web-phones, cellular phones, and network computers. The picoJava I core thus brings the interoperability advantages of the Java environment to end-user oriented products. Fujitsu has recently positioned the Java platform at the center of its network computing efforts and is currently porting the JavaOS onto its offerings based on the Sparclite platform. Contact Sun on the web at http://www.sun.com, and Fujitsu at http://www.fujitsumicro.com, or telephone (408) 922-9000.

Aimed at the high-end of mobile computing systems, the 3D Rage LT Pro graphics accelerator is the first available device to employ the advanced graphics port (AGP) interface to maximize the transfer data rate between the frame buffer and graphics controller. The chip, developed by ATI Technologies Inc., Thornhill, Ontario, Canada, also is the first to incorporate a 65-MHz, low-voltage differential logic interface to the display panel—a key to delivering high-performance while minimizing power consumption and pin count. The chip operates in either the AGP 1X or 2X modes (66 or 133 MHz, respectively) and dramatically increases the amount of textures that can be displayed on the screen. The Tri-View output capability allows the chip to simultaneously drive an LCD panel, an SXGA monitor, and an NTSC/PAL display. The 3D Rage LT Pro delivers a 2D WinBench rating of 130 and a 3D WinBench rating of 250. Workstation-quality 3D performance is achieved using an on-chip floating-point hardware set-up engine and an on-chip 4-kbyte cache. Additional 3D support features include bilinear and trilinear filtering, Z-buffering, advanced edge antialiasing, and special effects such as alpha blending, fog, and texture lighting. For top-notch 2D performance, the 64-bit graphics engine accelerates bitBLT, line draws, polygon/rectangle fills, bit masking, monochrome expansion, panning/scrolling, and scissoring, and includes hardware support for icons and cursors. Samples of the chip are available now, and in quantities of 10,000 units, the chip sells for $35 each. Contact Azzedine Boubguira at (905) 882-2600, or on the web at http://www.atitech.ca.

New versions of the popular Winstone, WinBench, and 3D WinBench graphics benchmarks have been released by the Ziff-Davis benchmark operation, Research Triangle Park, N.C. The benchmarks include updates to the application software suite used in the evaluation, and an update on the base-level hardware used to execute the application suite. Benchmark levels examined include system, subsystem, and component areas, and the benchmark types include application-based examples, playback of captured keystrokes, simulated operations, synthetic/profiled operations, and inspection tests. Results are normalized to 10.0 on the base machine, which is a Dell Dimension P133 with 32 Mbytes of RAM, running Windows NT 4.0. Because the applications have been updated, results on the benchmark tests are not comparable to last year's results. WinBench 98 also includes many additional tests for FPU, CD-ROM, full-motion video (Cinepak, Indeo 3.2, Indeo 4.1, and MPEG-1), and DirectDraw evaluation. Similarly, 3D WinBench tests include many changes from last year's suite. To do the testing, DirectX 5.0 is required. To obtain a copy of the benchmarks or to get the latest updates, access the company's web site at http://www.zdbop.com.

Industrial SBC Boasts 100Base-T Connectivity

100Base-T connectivity is one of the key features of the VIPer821, a 233-MHz industrial single-board computer. The board, which fits a half-size ISA form factor, is suited for high-end industrial automation, networking, telecommunications, and medical systems. The flexible design permits integration into an ISA passive backplane or into an embedded environment. Other features include up to 256 Mbytes of DRAM, on-board 64-bit PCI graphics, a CompactFlash connector, USB support, and standard I/O options. Operating-system support includes MS-DOS, Windows 3.1, Windows 95, Windows NT, OS/2 Warp, SCO Unix, and Novell Netware.

***Teknor Industrial Computers Inc.,** 616 Cure-Boivin, Boisbriand, Quebec, Canada J7G 2A7; (800) 354-4223 or (514) 437-5682; Internet: http://www.teknor.com.* **CIRCLE 485**

Digital PRML Read Channel Handles 240 Mbits/s

PRML read-channel data rates up to 240 Mbits/s are possible using the 88C2020 user-selectable EPR4 and PR4 channel controllers. The chip includes a Viterbi detector and a choice of 16/17 or 8/9 Endec functionality. The 88C2020 is a low-power device that employs the company's proprietary MSP (Mixed-Signal Processing) technology. The chip offers the speed of analog PRML ICs with the functionality of digital PRML designs. In addition, the digital 0.5-micron CMOS technology offers a small form factor and a lower cost. The part is housed in an 80-pin TQFP package. The 88C2020 is built with self-calibration circuits that can adjust for normal CMOS process variations. Samples of the 88C2020 digital read channel are available now, with production quantities scheduled before the end of the year. In large quantities, the chip sells for less than $6.

***Marvell Semiconductor Inc.,** 525 Almanor Avenue, Sunnyvale, CA 94086; (408) 524-2488; Internet: http://www.marvell.com.* **CIRCLE 486**

Full-Function Notebook PC Weighs Just 2.4 Lbs.

Just because a notebook computer is "full-featured" doesn't mean it has to be heavy. The AMiTY CN is built with a 133-MHz Pentium processor, 48 Mbytes of DRAM, a 1.2-Gbyte hard-disk drive, weighs just 2.4 lbs., and

measures 9.3 by 6.7 by 1.34 in. Other features include a 7.5-in. passive LCD with VGA resolution, dual Type II PC Card slots, an infrared port, a speaker, and a microphone. The keyboard offers a 16-mm key pitch and a 2-mm stroke. Connections are available for an external keyboard or CRT display. The lithium-ion batter lasts about 2 hours on a charge, and needs about 3 hours for a full recharge. An optional high-capacity lithium-ion battery lasts for 7.5 hours. The AMiTY CN lightweight notebook computer sells for $1995.

Mitsubishi Electronics America Inc., *5665/5757 Plaza Dr., P.O. Box 6007, Cypress, CA 90630; (714) 220-2500; http://www.mitsubishi-mobile.com.*
CIRCLE 490

Chip Puts Ultra2 SCSI On The Motherboard

Ultra2 SCSI doubles the performance of UltraSCSI from burst rates of 40 to 80 Mbytes/s. However, in certain environments, that enhanced performance would be limited by the bandwidth of today's standard 32-bit PCI bus. To eliminate any potential bottlenecks, the AIC-7891 PCI-to-Ultra2 SCSI controller is a 64-bit device. Applications that are poised to take advantage of this technology include CAD, financial analysis, and desktop publishing. The chip lets motherboard OEMs integrate the 64-bit technology directly onto the board. Also available is an evaluation kit that includes an AIC-7891-based evaluation board, Windows NT drivers, installation software, cables, and documentation.

Adaptec Inc., *691 South Milpitas Blvd., Milpitas, CA 95035; (408) 945-8600; http://www.adaptec.com.*
CIRCLE 491

Audio ADC Can Operate At 24 Bits

Audio-system developers can upgrade their 20-bit designs to 24 bits without making a significant cost trade-off using the CS5360 analog-to-digital con-

verter (ADC). The chip performs sampling, analog-to-digital conversion, and antialias filtering with any external assist. The chip is suited for such platforms as digital mixing consoles, effects processors, digital audio tape, and multitrack recorders. The easy upgrade comes because the part is pin-compatible with the CS5335 20-Bit converter. The CS5360 operates at +5 V and features a 105-dB dynamic range, a 0.0025 dB pass-band ripple, and an 85-dB stop-band attenuation. A high-pass filter removes the dc offset at the converter's input. The CS5360 24-bit ADC sells for $7.50 each in 1000-piece quantities. Samples are available now, with production beginning in the first quarter of next year.

Cirrus Logic Inc., *Crystal Semiconductor Products Div., 3100 West Warren Ave., Fremont, CA 94538; (510) 623-6423; http://www.cirrus.com.*
CIRCLE 492

CompactPCI SBC Holds PowerPC CPU

A 166-, 200-, or 240-MHz PowerPC 603e microprocessor is the basis of the SmartEngine/603cPCI, a single-board computer that fits a single-slot 6U Eurocard form factor for the CompactPCI standard. The board supports most popular real-time operating systems, including VxWorks, C-Executive, pSOS, and Nucleus. A PMC expansion connector lets users customize the board for specific applications. Interfaces are included for the PCI bus, an Ethernet LAN, and SCSI peripherals. Up to 128 Mbytes of DRAM can be employed, as well as 256 or 512 kbytes of secondary cache memory. Available now, the SmartEngine/603cPCI SBC sells for $1876 with a 166-MHz processor and 16 Mbytes of DRAM.

Smart Modular Technologies Inc., *4305 Cushing Pkwy., Fremont, CA 94538; (510) 623-1231; Internet: http://www.smartm.com.* **CIRCLE 493**

USB Controllers Built To Simplify Design-In

Using the 8x931 family of USB controllers, designers can build smart hubs for attaching PC peripherals. The two parts in the family are based on the MCS 51 hardware device. The 8X931Hx hub controller can be embedded in a monitor or other peripheral that requires hub functionality. It supplies five downstream ports, and one embedded and four external connections. The 8X9931Ax is aimed at high-speed peripherals, such as imaging devices or forced-feedback units. The low-power IC can also be employed in portable applications. Both chips contain 256 bytes of on-chip data RAM, support isochronous and non-isochronous data-transfer modes, and are available in ROMless or 8-kbyte ROM versions.

Intel Corp., *2200 Mission College Blvd., P.O. Box 58119, Santa Clara, CA 95052; Internet: http://www.intel.com/design/usb*
CIRCLE 494

Laser Printer Handles 35 Pages/Minute

The L5035 LaserLine industrial-strength laser printer combines a 35-page/minute output with a 300-dot/in. resolution. The printer permits on-command switching between continuous forms or cut sheets either through the data stream or on the printer's control panel. Unlike conventional laser printers that employ heat or pressure to fuse the toner to the media, the *(continued on page 90)*

(continued from page 89)
L5035 uses a two-lamp process to bond the toner to the page by warming the paper to open its pores, and then melting the toner right into those pores. Paper weights can range from 17 to 40 lb., and from 7 to 16 in. wide. Available immediately, the L5035 LaserLine printer sells for $33,995.

***Printronix Inc.**, 17500 Cartwright Road, P.O. Box 19559, Irvine, CA 92623; (714) 863-1900; Internet: http://www.printronix.com.* **CIRCLE 495**

Faster Spin Rate Leads To Faster Access

By spinning the disk at 10,020 rpm, the Ultrastar 9ZX hard-disk drive features an average seek time of 6.3 ms. In addition, the maximum sustained data rate is 17 Mbytes/s. Thanks to a fifth-generation digital PRML read channel, the maximum media data rate is 205 Mbits/s. The 9.1-Gbyte drive, built with six platters, also contains a 1-Mbyte segmented cache buffer. The drive's Magnetoresistive Extended (MRX) head sends out stronger signals signal than the previous generation MR heads, resulting in a higher areal density (1.136 Gbits/in.^{2}). The integrated Drive-Temperature Indicator Processor (Drive-TIP) automatically monitors disk-drive temperature and alerts the user when the recommended temperature has been exceeded. The nonoperating shock is rated at 140 Gs. The drive consumes 16.5 W in idle mode and 19.3 W when reading or writing. Various interfaces are available, including Ultra SCSI, Ultra2 SCSI, SSA, and Fibre Channel-Arbitrated Loop (FC-AL). The UltraSCSI drive is shipping now; the Ultra2 SCSI version will be available in the first quarter of next year, and the SSA and FC-AL models will ship in the second quarter.

***IBM Corp.**, Storage Systems Div., 5600 Cottle Rd., San Jose, CA 95193; (800) IBM-7777; Internet: http://www.ibm.com/storage.* **CIRCLE 496**

OEMs Can Customize Remote Pointing Device

As a remote input device, the IRC-TC can help lower OEM design times and engineering costs. The IRC-TC is a wireless device that handles typical mouse functions. Such a peripheral is typically employed in conjunction with a multimedia PC, an LCD projector, or a television-computer convergence system. It contains two fully configurable keypads up to 23 keys. Graphic overlays or LED status indicators can occupy the space of unused keys. The keypads also can be customized by the OEM. Other features include a pressure-sensitive 360-degree pointing button, left- and right-mouse click buttons, and a click-trigger case design that lets the user "point and click" on a screen object. Options include backlighting for all the keys and an integrated laser pointer.

***Interlink Electronics Inc.**, 546 Flynn Rd., Camarillo, CA 93012; (805) 484-8855; http://www.interlinkelec.com.* **CIRCLE 497**

Data-Acquisition Module Works With Sharc DSP

Eight independent 500-kHz analog-to-digital conversion channels are supplied on a mezzanine module that conforms to the bitsi I/O mezzanine format. In addition to the simultaneously sampling ADC channels, the module contains four 100-kHz digital-to-analog-conversion output channels. The module attaches to a baseboard employing the Sharc DSP chip. The data-acquisition module is best suited for industrial-control applications that require intensive I/O and digital-signal processing. The input channels perform 12-bit data conversions, while the output channels convert 14-bit data. The differential inputs enhance the noise immunity, while the overvoltage protection is useful for the industrial settings. A host of development tools also are available. Prices for the data-acquisition module start at $1495.

***Bittware Research Systems**, 33 North Main St., Concord, NH 03301; (603) 226-0404; http://www.bittware.com.* **CIRCLE 498**

CPU-To-PCI Bridge Operates At 50 MHz

The QSpan bus bridge chip connects MPC8XX and Motorola embedded processors to the PCI bus at a frequency of 50 MHz. While maintaining pin and functional compatibility with the previous-generation part, the 50-MHz QSpan can operate at either 5 or 3.3 V, allowing for smaller and lower power designs. By employing deeper FIFOs and separate FIFOs for read and write operations, increased data rates can be obtained for getting data into and out of local memory. A direct connection can be made between the PCI and the MC68360 (QUICC), MPC860 (PowerQUICC), MPC850, MPC821, MPC801, and MC68040 embedded processors.

With a minimal amount of glue logic, the chip can connect the PCI bus to the PowerPC602, PowerPC603, PowerPC603e, MC68302, and MC68030 processors. A host of development tools are available, including evaluation boards, executable models, and a reference design. Available now, the 3.3-V part costs $25.20, and the 5-V chip sells for $24, both in lots of 10,000.

***Tundra Semiconductor Corp.**, 603 March Rd., Kanata, Ontario, Canada K2K 2M5; (800) 267-7231 or (613) 592-0714; http://www.tundra.com.* **CIRCLE 499**

New Card Adds Sound To STD32 Platform

The ZT 8944 is an STD32 card that offers 16-bit stereo audio using the Analog Devices Sound Port Controller chip. The card provides an FM-synthesizer capability and is compatible with the SoundBlaster and AdLib standards, as well as any applications that run under Windows 95. An on-board EEPROM permits control of an additional IDE device, such as a hard-disk or CD-ROM drive. Traditional I/Os populate the board, including an MPU-401 MIDI port, line in and out, and a microphone input. The ZT 8944 audio card, which is available now, goes for $285.

***Ziatech Corp.**, 1050 Southwood Dr., San Luis Obispo, CA 93401; (805) 541-0488; http://www.ziatech.com.* **CIRCLE 500**

UPDATE ON DEMULTIPLEXING HIGH-SPEED DATA

Demultiplexing Eases Capture Of High-Speed Data

Using A Logic Analyzer's Demultiplexing Capability Allows You To Acquire Data At Up To Twice Its Normal Synchronous Capture Rate.

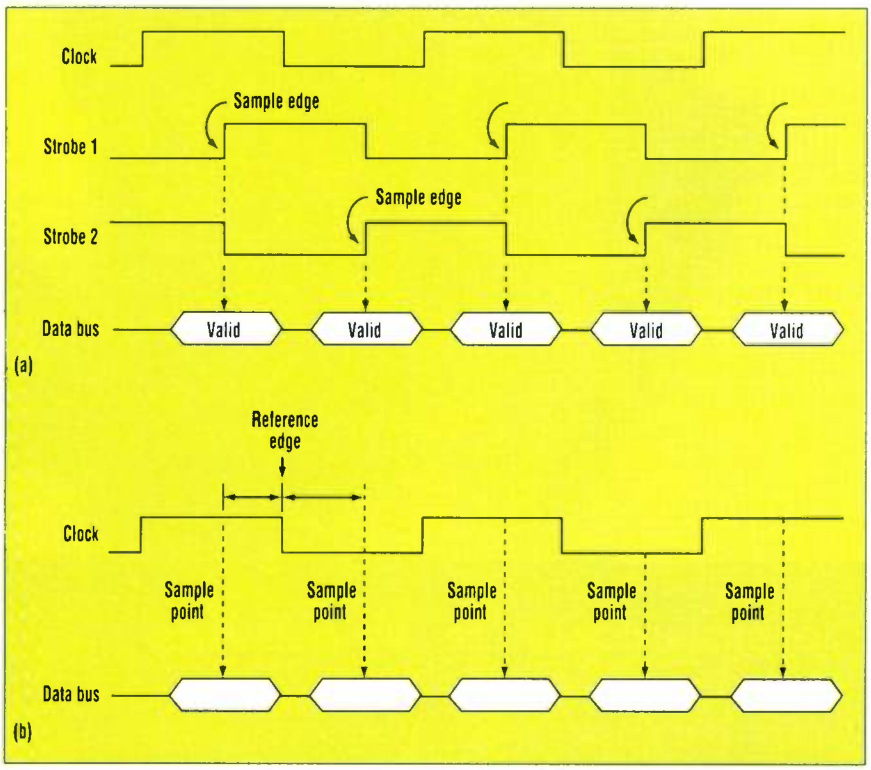
JAMES M. FENTON, Tektronix Inc., MS 39-345, 13975 S.W. Karl Braun Dr., Beaverton, OR 97077; (503) 627-1228.

In today's world of microprocessors and high-speed data buses, the equivalent synchronous bus speed is now crossing the 200-Mtransfer/s barrier. In order to further increase the bandwidth of the data bus, microprocessor manufacturers are increasing the bus frequency and using data transfer techniques such as "double pumping" of the data bus. Double pumping means that two data samples are transferred across the bus in one clock cycle.

Although double pumping is effective in boosting bandwidth, the technique also offers unique challenges in the design of interface circuitry to capture the bus data. The use of multiple data transitions in one clock cycle and the increase in bus frequencies make it essential to validate the integrity of the bus to ensure that it is operating correctly. To that end, acquiring double-pumped data synchronously requires designers to reach into their logic analyzer's bag of acquisition tricks.

Some of the tried-and-true methods of acquiring data transfers at this speed include increasing the synchronous acquisition capability of the logic analyzer (buy a faster synchronous acquisition module and sample on both clock edges) or build a custom fixture to demultiplex the data. You also could use multiple high-speed data-acquisition modules or the built-in demultiplexing capability in your logic analyzer. This article will discuss the use of demultiplexing capabilities built into logic analyzers to acquire data on buses operating at or above a 200-Mtransfer/s equivalent rate.

One advantage of acquiring and storing data using demultiplexing is the ability to capture data at up to twice the synchronous data-acquisition rate specification of the logic analyzer. Another advantage is that demultiplexing provides twice the number of samples acquired as the memory depth of the logic analyzer. Demultiplexing also provides half the signal loading on a high-speed bus because it does not re-



1. The most common way to demultiplex data employs two different clock or strobe edges to control when the data bus is sampled (a). A technique that allows users to capture data at up to twice the logic analyzer's specified synchronous acquisition rate uses only one clock edge, with sampling accomplished at different times relative to that edge.

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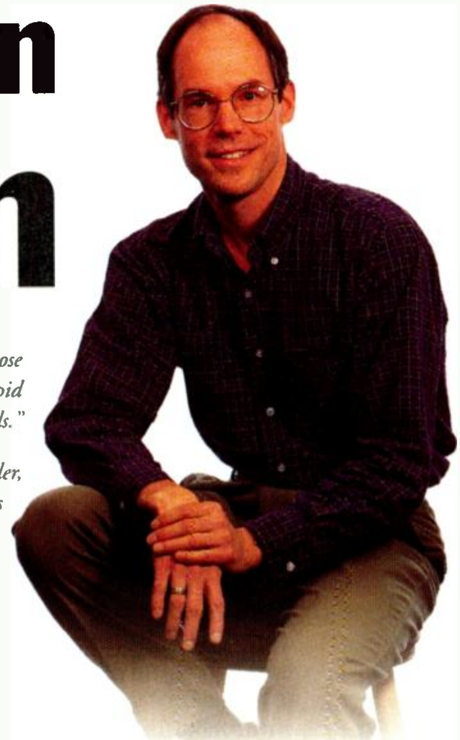

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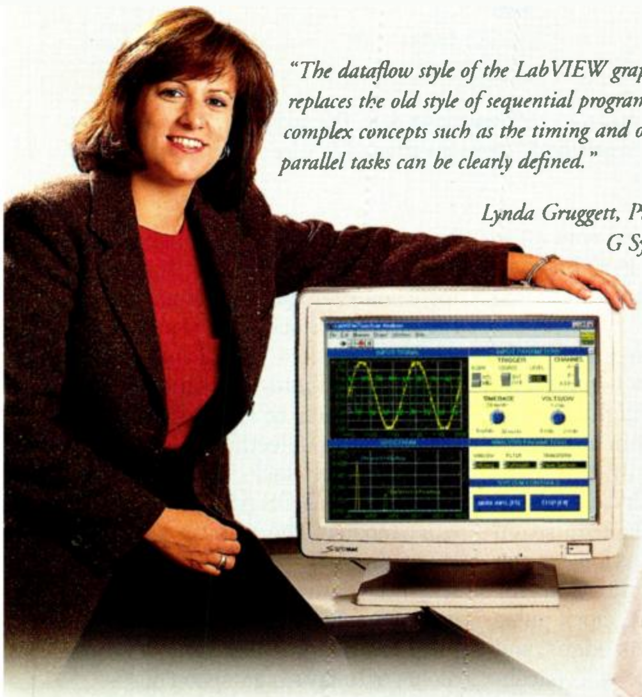

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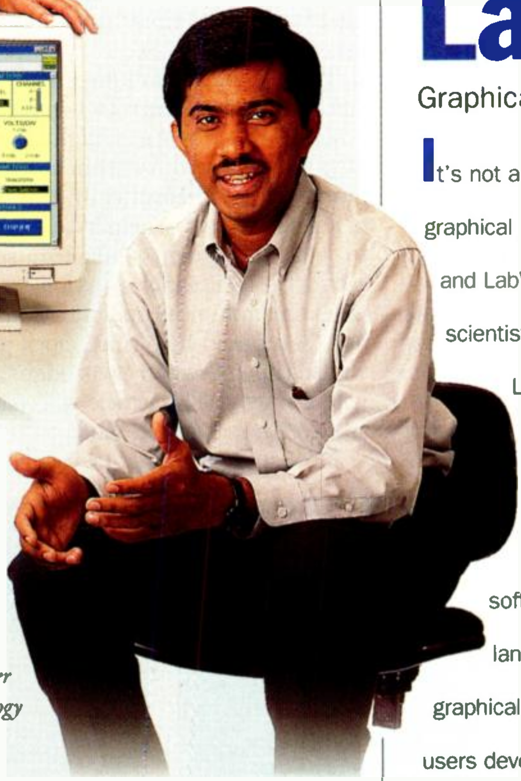

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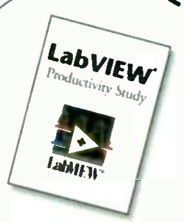

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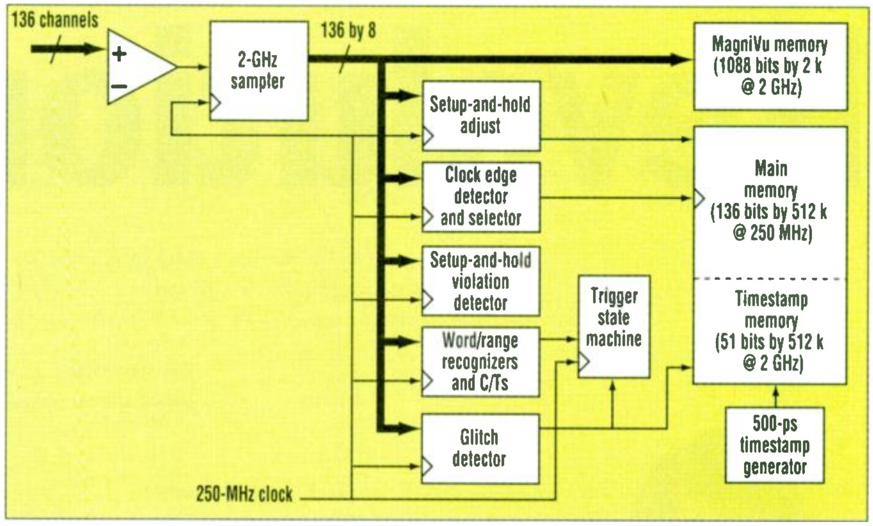
READER SERVICE 154

quire double probing of the bus.

On the other hand, there are some drawbacks to acquiring data using demultiplexing. First, the channel width is cut to half of the available channels on the logic analyzer. Second, you must interpret the timing and data packet order within a given logic analyzer sample.

Interpreting the timing relationship and how the data is stored in the logic analyzer requires an understanding of how data is displayed in the waveform and listing displays. You can easily get confused if you don't keep track of when the data channels are sampled relative to the reference timing edge and the order of the samples. Considering its advantages and disadvantages, for certain applications demultiplexing provides an irreplaceable technique for acquiring data from high-speed synchronous buses.



2. Most state-of-the-art logic analyzers can demultiplex data. One such architecture illustrates how a programmable setup-and-hold circuit steers the sampled data by acquiring it at different times relative to the clock edge.

Splitting Up Data

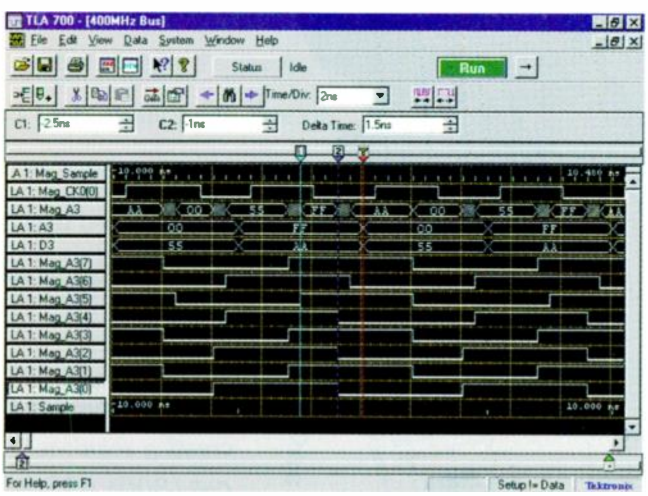
Demultiplexing is a hardware-based way to channel or split data into two paths by sampling one data bus at different times. Data from the 32-bit bus is sampled at two different times and steered onto two different data paths: "A" and "D".

There are many different ways to demultiplex data. The most common method uses two different clock or strobe edges to control when the data bus will be sampled *(Fig. 1a)*. Another method involves the use of only one clock edge, but the data bus is sampled at two different times relative to that clock edge. This method employs programmable setup-and-hold control to allow individual channels to be sampled at different times relative to one master clock *(Fig. 1b)*.

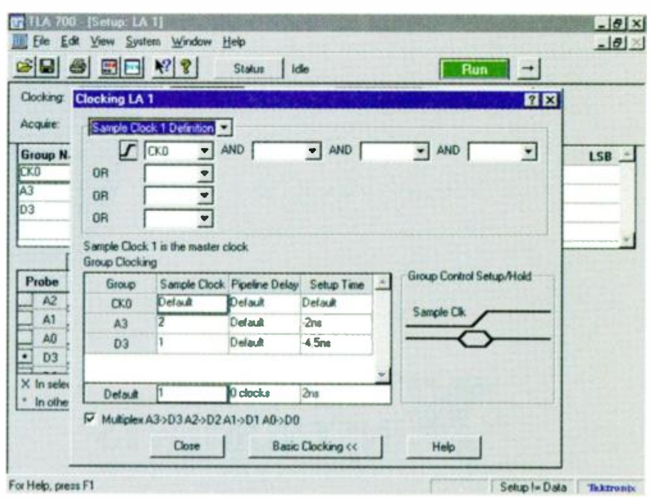
This second technique, using only one clock edge to control when the data is sampled, is a more straightforward way to acquire data from a double-pumped bus. Theoretically, this technique allows you to acquire data at up to twice the synchronous acquisition rate of the logic analyzer, as long as you meet the minimum specifications for data setup-and-hold time, clock pulse width, time between clock edges, and voltage swing. This article will concentrate on the second method.

Most state-of-the-art logic analyzers have the ability to demultiplex data. An example hardware architecture of a logic analyzer that can demultiplex using only one clock edge is shown *(Fig. 2)*. The samplers within the programmable setup-and-hold time circuitry steer the data to the different data paths at user-selectable times relative to the master clock. This capability is supplied by CMOS ASICs on the acquisition module. The user can select which channels will be used and can program when the data is sampled. This flexibility allows users to tailor the data sampling times for the tight timing requirements of today's high-speed buses.

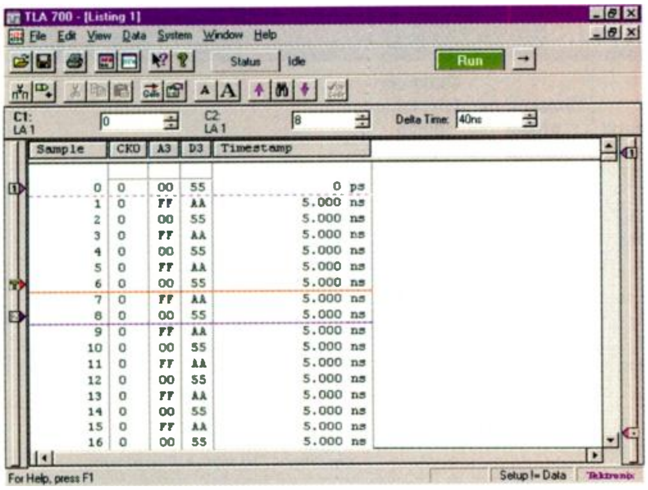
Within the logic analyzer, there are demultiplex target channels that may



3. An example of a waveform acquisition shows the sample clock's tick marks every 500 ps (top trace), the master clock (second trace), and the bus from which the analyzer will acquire data (third trace).



4. Using the timing relationship determined from the information in Fig. 3, the user enters different setup times for the two data groups. A3 is sampled at –2 ns, and D3 at –4.5 ns.



5. The captured data also can be shown with the timestamp information. In this case, the timestamp value was selected to indicate the difference between successive samples—5 ns.

be controlled by the user interface or may be "hard-wired" in the hardware. You need to keep track of which channels receive the first sampled data and which channels receive the second sampled data.

Step-By-Step Procedure

The best way to illustrate the advantages and disadvantages of demultiplexed data acquisition in logic analysis of high-speed data buses is to go through the six-step procedure designers should follow. The example involves capture of data with a 00-55-FF-AA pattern running at 400 Mtransfers/s.

Step 1: Study the bus timing requirements.

The user must understand the timing relationship between the master clock and when the data is valid on the bus. When data is being double pumped on the bus, the data may be valid only before or after the rising edge of the master clock. Knowing when the data is valid will help you approximate when the bus should be sampled. This information should be available from the vendor in either the component or bus-timing specification.

Step 2: Make the appropriate channel assignments.

The user must identify which of the logic analyzer's data channels will be used to acquire the double-pumped data. Most logic analyzer specifications delineate which channels are demultiplexed from and which channels are demultiplexed to. It's important to keep track of this information so you can properly identify what is going on in the waveform or listing display for the data packets (sequence of data information).

Step 3: Make the connections to the system under test.

The connections to the system under test require special precautions. Operating at these speeds demands a good knowledge of high-speed design rules. The connections should not introduce stubs and should have a very low capacitance. Components such as the Mictor connector, which have a low capacitance and high density, are a good choice for a high-speed data bus interface connector. Ideally, connectors like the Mictor⇓from Amp Inc., Harrisburg, Pa.⇓should be designed into the layout so that the connection to the bus is a simple matter.

Once the connection to the bus is in place, you can check the signal integrity using a high-speed oscilloscope. Some logic analyzers provide this capability in the same box. When you feel comfortable with the signal integrity, you can check the timing of the data.

Step 4: Perform a high-speed asynchronous acquisition.

If the exact timing of the data bus is not known, performing a high-speed data acquisition will help identify the relationship between the data-valid time and the master clock. In fact, the timing may vary from system to system, so performing this acquisition may be the only way to be sure of the actual timing.

In the example system, the first line of the waveform display (Mag_Sample) shows the high-speed sample clock's tick marks, which occur every 500 ps *(Fig. 3)*. The second waveform is the master clock (Mag_CK0(0)), which in the example is running at 200 MHz. The third waveform line (Mag_A3) is the bus from which the analyzer will acquire data.

Step 5: Adjust the setup-and-hold window to capture the data correctly.

Now that you know what the timing relationship is, you need to select the appropriate setup-and-hold time window for the two data-valid times relative to the master clock edge. In the example setup, you can see that relative to the first rising edge of the master clock, the data-valid time for the data 00 is from –2 ns to –3.5 ns *(Fig. 3, again)*. Data group A3 is assigned to capture data 00 from the bus. Relative to the first rising edge of the master clock, the data-valid time for the data 55 is from –4.0 ns to –6.5 ns. Data group D3 is assigned to capture this data.

Now the user can set the logic analyzer's programmable setup-and-hold window to acquire data at the appropriate times. Data group A3 is set to –2 ns for the setup time relative to the master clock, and data group D3 is set to –4.5 ns for the setup time *(Fig. 4)*. Now the analyzer is programmed with two different times to sample the data relative to one clock edge.

Step 6: Perform the demultiplexed synchronous acquisition.

With the setup times programmed, you can now perform the demultiplexed synchronous data acquisition from the bus. Referring to the waveform diagram again, lines four and five display the demultiplexed data from the 400-Mtransfer/s bus. Group A3 contains the 00-FF portion of the pattern and group D3, which is the demultiplex target group, contains the 55-AA portion of the pattern.

A listing of the same waveform data along with the timestamp information shows that the 00 value in the first sample went into group A3 and the 55 data went into group D3 *(Fig. 5)*. The second sample indicates that the analyzer acquired FF into group A3 and AA into group D3. In this example, the timestamp value was selected to display the difference between successive samples, which in this case was 5 ns.

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LOGIC ANALYZERS

LOGIC ANALYZERS

Manufacturer	Model/ price	Maximum timing/state sample rate (MHz)	Timing/state channels	Memory/ channel	Timing/state trigger levels	Minimum detectable glitch (ns)	Remarks
Boulder Creek Engineering 133 Mission St. Suite 104 Santa Cruz, CA 95060 (408) 460-3710 fax (408) 460-3715 e-mail: bryan@bcreek.com	POD-8020/ $1295	100/66	18/18	64 k	1/1	10	PC-hosted through serial port.
	POD-8040/ $2495	200/100	32/48	128 k	4/4	5	PC-hosted through serial port or USB; disassembly for 6811 and 8051 microcontrollers.
Embedded Performance Inc. 1860 Barber Ln. Milpitas, CA 95035 (408) 437-7800 fax (408) 435-7970	DS 4000/ $15,000	n.a./50	n.a./256	64 k	n.a./*	n.a.	Distributed emulation analyzer combines with debug monitor and source-level debuggers for full software development station. *50 events, 50 conditions, 16 states, five actions.
	CLAS 4000/ $15,000	100/50	96/394	4 k	15/15	3	Modular; controlled as a SCSI device from a Macintosh or a Sun workstation.
	CLAS 4000D/ $20,000	100/50	96/394	4 M	15/15	3	Deep-memory version of CLAS 4000, 32 M maximum.
	T-100/ $35,000	2000/250	32/32	4 k	2/2	1.5	Includes 250-MHz, 32-channel pattern generator and external PC controller.
	CLAS 4000G/ $60,000	1000/n.a.	64/n.a.	8 k	2/n.a.	1	Controlled as a SCSI device from a Macintosh or a Sun workstation.
Hewlett-Packard Co. Test and Measurement Org. P.O. Box 50637 Palo Alto, CA 94303-9512 (800) 452-4844 www.hp.com/go/logicanalyzer	HP 54620A/ $2995	500/n.a.	16/n.a.	2 k*	2/n.a.	3.5	Oscilloscope-like interface with high-speed display. *8 k with glitch detector off.
	HP 54620C/ $3995	500/n.a.	16/n.a.	2 k*	2/n.a.	3.5	Same as HP 54620A but with a color display.
	HP 1664A/ $4990	500/50	34/34	4 k	10/12	3.5	Built-in 3.5-in DOS drive, transitional timing; LAN interface optional.
	HP 54645D/ $4995	400/n.a.	16/n.a.	1 M	2/n.a.	5	Mixed-signal oscilloscope with two DSO channels and 16 logic-timing channels.
	HP 1663C/ $5990	500/100	34/34	4 k	10/12	3.5	See HP 1664A.
	HP 1662A/ $7990	500/100	68/68	4 k	10/12	3.5	See HP 1664A.
	HP 1661C/ $9990	500/100	102/102	4 k	10/12	3.5	See HP 1664A.
	HP 1672D/ $10,400	250/100	68/68	64 k	10/12	3.5	LAN interface standard; 1-M memory optional.
	HP 1660C/ $11,990	500/100	136/136	4 k	10/12	3.5	See as HP 1664A.
	HP 1663CS/ $12,950	500/100	34/34	4 k	10/12	3.5	Same as HP 1663C, plus 1-Gsample/s, 250-MHz integrated oscilloscope.
	HP 1671D/ $13,400	250/100	102/102	64 k	10/12	3.5	LAN interface standard; 1-M memory optional.
	HP 1662CS/ $14,950	500/100	68/68	4 k	10/12	3.5	Same as HP 1662C, plus 1-Gsample/s, 250-MHz integrated oscilloscope.
	HP 1670D/ $16,400	250/100	136/136	64 k	10/12	3.5	LAN interface standard; 1-M memory optional.
	HP 1661CS/ $16,950	500/100	102/102	4 k	10/12	3.5	Same as HP 1661C, plus 1-Gsample/s, 250-MHz integrated oscilloscope.
	HP 1660CS/ $18,950	500/100	136/136	4 k	10/12	3.5	Same as HP 1660C, plus 1-Gsample/s, 250-MHz integrated oscilloscope.
	HP 16500C/ $9500	—	—	—	—	—	Five-slot mainframe for HP 165XX-series cards; hard drive, GPIB, RS-232, LAN support, Centronics standard.

LINEAR TECHNOLOGY DESIGN NOTES

Battery Backup Regulator is Glitch-Free and Low Dropout

Design Note 170

Mitchell Lee and Todd Owen

A new class of linear regulator has been developed for battery backup applications. It eliminates both the losses associated with steering diodes, the glitches and battery-to-battery cross conduction inherent in MOSFET switching schemes and the poor regulation inherent in dual regulator schemes previously used for this purpose. See the comparison detailed in Table 1.

Figure 1 shows a simplified block diagram of the LT®1579 dual input regulator. The regulator features 300mA output capability and low dropout. Two batteries, or a battery and an AC-derived power source, are connected to V_{IN1} and V_{IN2}. The relative voltage of these two sources plays no role in determining which input supplies power to the load: the primary input (V_{IN1}) is normally used to power the output, and the secondary input (V_{IN2}) takes over as a backup when the primary source fails. Unlike diode steering circuits, this allows batteries of any voltage to serve as primary or backup. Either battery can be removed and replaced without disturbing the output voltage.

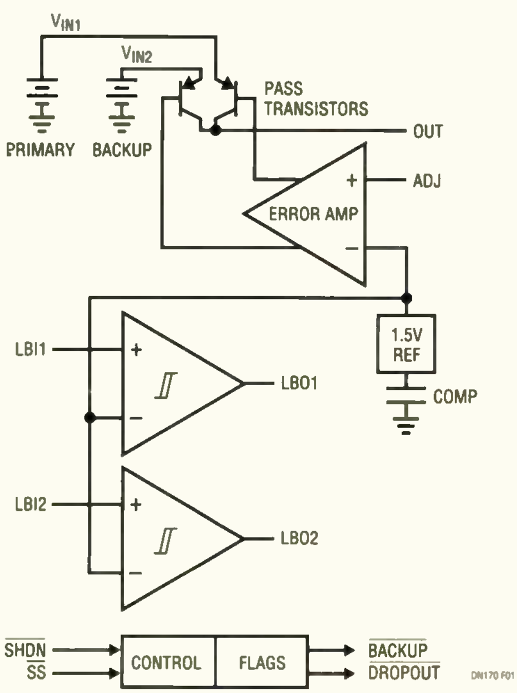

Figure 1. LT1579 Block Diagram

Several other important features are included to simplify integration of the LT1579 into a battery-backed system. Again referring to Figure 1, two logic flags, $\overline{\text{BACKUP}}$ and $\overline{\text{DROPOUT}}$, are useful for monitoring the status of the regulator. $\overline{\text{BACKUP}}$ goes low when V_{IN1} fails and V_{IN2} takes over, whereas $\overline{\text{DROPOUT}}$ indicates that both V_{IN1} and V_{IN2} have failed.

Two comparators independently monitor the condition of the batteries. In contrast to $\overline{\text{BACKUP}}$ and $\overline{\text{DROPOUT}}$, the low-battery detectors give advance warning of impending battery failure. Secondary Select ($\overline{\text{SS}}$) overrides V_{IN1}'s priority over V_{IN2}, forcing the regulator to abandon the primary battery in favor of the backup.

The primary battery normally supplies the load until its terminal voltage is nearly equal to the output voltage; however, some battery types may be damaged if discharged this far. $\overline{\text{SS}}$, used in conjunction with a low-battery detector, allows the regulator to abandon the primary battery at a higher, nondamaging end-of-discharge voltage.

Table 1. Backup Method Comparison

	LT1579	STEERING DIODES	MOSFET SWITCHING	TWO REGULATORS
Guaranteed Battery-to-Battery Isolation	✓	✓		
Prioritized Inputs	✓		✓ (Needs Circuitry)	
Seamless Switching	✓	✓		✓
Seamless Regulation	✓			
Logic Override	✓		✓	
Battery Disconnect	✓		✓	✓

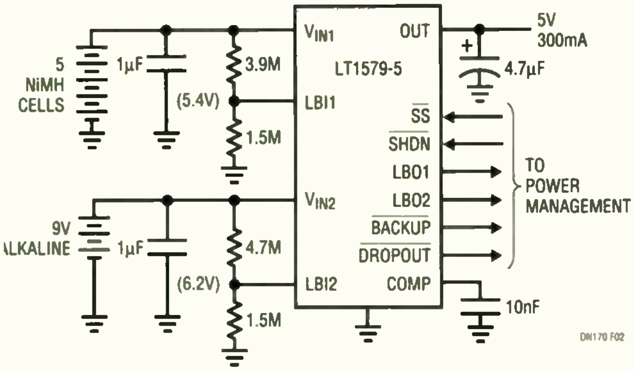

Figure 2. A 9V Battery Backs Up Five NiMH Cells

One last feature is SHUTDOWN; this turns the regulator off and reduces total drain from both inputs to less than 7µA.

Figure 2 shows a typical application of the LT1579 with primary power supplied by five NiMH cells and backup provided by a 9V alkaline. Both low-battery comparators are used; they report the condition of the primary and backup batteries to a microprocessor. The BACKUP and DROPOUT flags keep the microprocessor apprised of the regulator's status. In addition to the fixed 5V version shown, 3V, 3.3V and adjustable versions are also available.

9V snap terminals are easily reversed by the end user during installation of the battery. No harm is done to the LT1579 because both inputs are reverse-battery protected. No current is drawn from the reversed battery and no excess current is drawn from the adjacent battery. Best of all, the load never knows the difference. The regulator continues to deliver the correct output voltage throughout the entire event.

Figure 3 shows a typical sequence of events for the circuit of Figure 2. Initially, both batteries are fully charged and all status flags (LBO1, LBO2, BACKUP and DROPOUT) are high. Load current, assumed to be 100mA, is drawn from the primary battery at V_{IN1}. After a period of time, V_{IN1} begins to falter. At point A, V_{IN1} = 5.4V and LBO1 goes low, predicting the eventual depletion of the primary battery. When V_{IN1} enters dropout (B), BACKUP goes low and the regulator begins to gradually transfer the load to the backup battery at V_{IN2}. By time C, the primary battery has dropped below the point where it can deliver useful current to the output and all load current is supplied by the backup battery.

The backup battery reaches its low voltage threshold at point D, signaling impending doom. This is the last chance for the system to alert the user, store critical data, shed load and find ways to survive until the batteries are replaced or recharged. In Figure 3 the relentless load continues unabated and discharges the backup battery. The regulator can no longer maintain its 5V output at point E and a logic low appears on the DROPOUT pin. Now the output falls below 5V and some current is once again drawn from the primary battery.

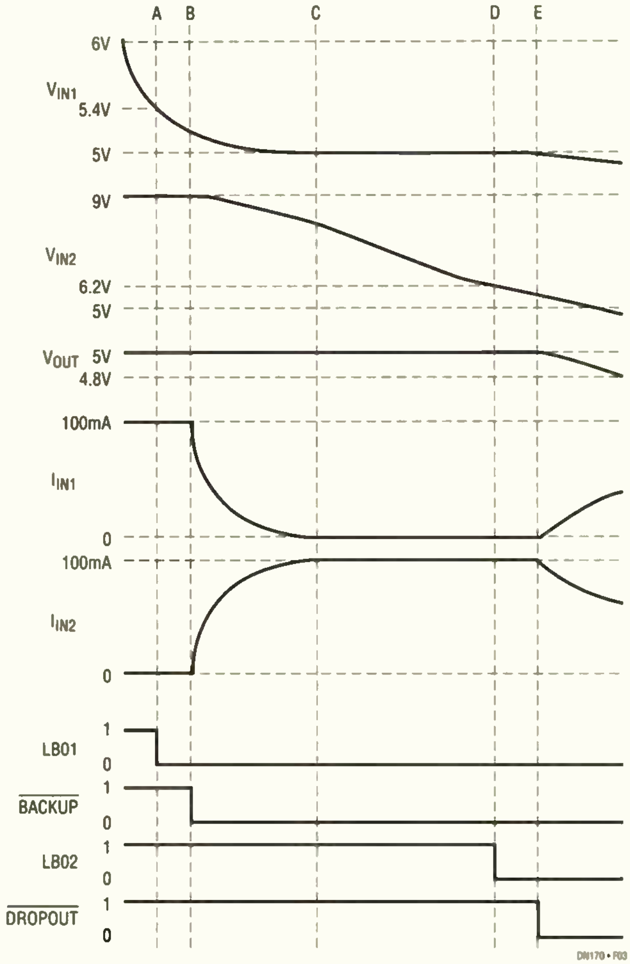

Figure 3. Typical Event Sequence for the Circuit of Figure 2. The Time Scale is Distorted for Purposes of Illustration

The LT1579 integrates a complex current steering function into one chip and can significantly reduce board space and design time while adding a number of useful power management features. It is ideally suited for battery- or line-operated equipment that relies on a backup battery for reliability and uninterrupted service. The output is unaffected by battery changes or power cycling, and status flags allow implementation of a very complete power management system with minimal external components.

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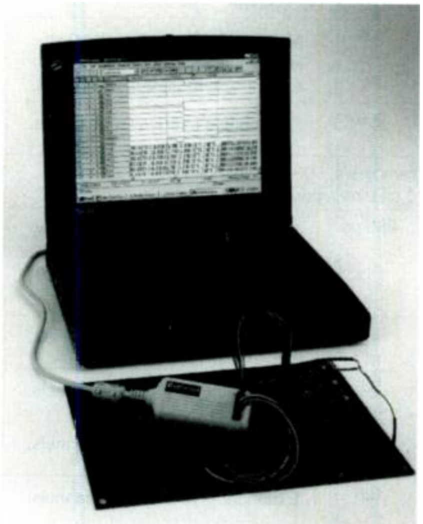
dn170f LT/TP 1297 340K • PRINTED IN THE USA

LOGIC ANALYZERS

	HP 16500C/ $9500	—	—	—	—	—	Five-slot mainframe for HP 165XX-series cards; hard drive, GPIB, RS-232, LAN support, Centronics standard.
	HP 16505A/ $6580	Prototype anayzer: large-screen, multiwindowed analysis and display processor that provides local or remote analysis capability for HP 16500C mainframe.					
	HP 16522A/ $6580	Pattern-generator card: 200 Mvectors/s, 248,000-vector memory, 40 channels, up to 200 channels with expansion cards.					
	HP 16533A/ $9130	Digital scope card: Two channels, 1 Gsamples/s, 250-MHz bandwidth, 32 ksamples/channel, up to 20 channels per system.					
	HP 16550A/ $9630	500/100	102/102	4 k	10/12	3.5	Multiple disassembly with 10 selectable filters; symbol download; expandable to 204/204 channels.
	HP 16554A/ $11,220	250/70	68/68	500 k	10/12	3.5	Expandable to 204/204 channels.
	HP 16534A/ $12,035	Digital scope card: Two channels, 2 Gsamples/s, 500-MHz bandwidth, 32 ksamples/channel; up to 20 channels per system.					
	HP 16517A/ $14,025	4000/1000	16/16	64 k (128 k)	4/4	250 ps	Typical channel-to-channel skew 250 ps; real-time setup-and-hold time violation triggering; up to 80 channels with expansion cards.
	HP 16555A/ $14,040	500/110	68/68	1 M	10/12	3.5	Expandable to 204/204 channels.
	HP 16556A/ $14,535	400/100	68/68	1 M	10/12	3.5	Expandable to 340/340 channels.
	HP 16555D/ $15,765	500/110	68/68	2 M	10/12	3.5	Expandable to 204/204 channels.
	HP 16556D/ $16,250	400/100	68/68	2 M	10/12	3.5	Expandable to 340/340 channels.
Hitachi Denshi America Ltd. 371 Van Ness Way Torrance, CA 90501 (310) 328-6116 fax (310) 328-6252	VC3120/ $2100	100/25	32/32	8 kwords	4/4	5	9-in. LCD display; RS-232, printer support standard; GPIB optional.
	VC3130/ $2837	100/25	48/48	8 kwords	4/4	5	Same as VC3120 plus signature analysis, analog display mode, and performance analysis.
Link Instruments Inc. 369 Passaic Ave. Suite 100 Fairfield, NJ 07004 (201) 808-8990 fax (201) 808-8786 sales@LinkInstruments.com www.LinkInstruments.com	LA4240-32K/ $1350	200/100	40/40	32 k	16	10	PC-based; digital pattern generation up to 100 MHz simultaneously with logic analysis; C programming library.
	LA4540-128K/ $1900	500/100	40/40	128 k	16	10	See LA4240-32K.
	LA4280-32K/ $2000	200/100	80/80	32 k	16	10	See LA4240-32K.
	LA4580-128K/ $2800	500/100	80/80	128 k	16	10	See LA4240-32K.
	LA45160-128K $7000	500/100	160/160	128 k	16	10	See LA4240-32K.
NCI 6438 University Dr. Huntsville, AL 35806 (205) 837-6667 fax (205) 837-5221	PA485/$1695	50/50	48/48	4 k	16/16	n.a.	Windows-based PC-card; needs microprocessor-specific disassembly pod ($420-$595).
	PA600-64K/ $2995	400/50	48/48	64 k	15/15	3.5	Linkable to 96 channels; transitional timing; custom applications with Visual Basic; 256-K memory optional.
	PA600-256K/ $3995	400/50	48/48	256 k	15/15	3.5	Same as PA600-64k with 1-M memory optional.
Tektronix Measurement Business Div. Literature Distribution Center P.O. Box 1520 Pittsfield, MA 01202 (800) 426-2200	TLA704/ $24,000	2000/200	272/272	512 k	16/16	2	Modular (two-module max); Windows 95 interface; integrated four-channel, 1-GHz DSO modules; simultaneous timing/state acquisition by one probe; high-density probe optional.
	TLA711/ $39,000	2000/200	680/680	512 k	16/16	2	Same as TLA704 with five-module limit.

PC-Based Logic Analyzer Samples At Up to 200 MHz

The palm-sized Pod-A-Lyzer 8040 connects to a PC through an RS-232 or Universal Serial Bus (USB) port to deliver 32 channels of timing analysis at 200 Msamples/s or 48 channels of state analysis at 100 MHz with 128k



of memory per channel. As a PC peripheral, the 8040 works within the Windows environment along with the user's compiler, debugger, and other design tools. The analyzer comes with software trace support for the Intel 8051 and Motorola 68HC11 microcontrollers and with an EJTAG port. After connecting the unit to the target CPU, users select the processor type and the 8040 produces a software trace list. The license-free software can be distributed and used by everyone on the design team to view, print, copy, and analyze the acquired data on their own PC. The 12.5-Mbyte/s USB port provides fast data transfer between the analyzer and the PC. The Pod-A-Lyzer 8040 costs under $2500 and will begin shipping in the first quarter of 1998.

***Boulder Creek Engineering**, 133 Mission St., Suite 104, Santa Cruz, CA 95060; (408) 460-3710; fax (408) 460-3715; e-mail: sales@pod.com.*
CIRCLE 505

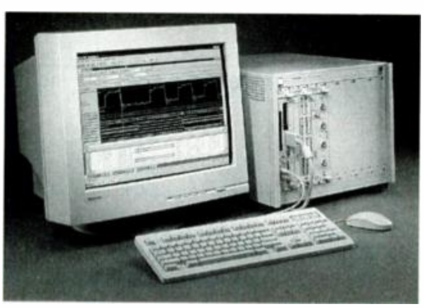
Inverse Assembler Works With ARM7 CPU

The HP E2493A multimode inverse assembler for the Advanced RISC Machines ARM7 CPU disassembles address and data bus binary information captured by an HP logic analyzer into assembly code. Enhanced filter capabilities present to the user only trace data that meets specified conditions. It performs disassembly to a user-supplied configuration even when few of the normal status lines from the ARM core are available, which is an advantage when designers must reduce the pin count on their ASICs. The inverse assembler operates with any combination of 8-, 16-, or 32-bit memory. HP also plans to adapt its processor probe to operate with the ARM7TDMI processor, which contains ARM's EmbeddedICE JTAG debug module. Developers will be able to use the probe to download code, display memory and register contents, and control program execution through single-stepping, setting or modifying breakpoints, or by running the code at full speed. Both the inverse assembler and probe work with the HP 16500C modular logic analysis system. The inverse assembler also works with HP benchtop analyzers. The HP E2493A multimode inverse assembler for the ARM CPU costs $1950. Delivery is in two weeks.

***Hewlett-Packard Co.**, Test and Measurement Org., P.O. Box 50637; Palo Alto, CA 94303-9512; (800) 452-4844 ext. 5544; http://www.hp.com/go/logicanalyzer.* **CIRCLE 506**

Modular Logic Analyzer Gets Added Microprocessor Support

Eight microprocessors have been added to the list of devices supported



by the TLA 700 series logic analyzers, bringing the total to more than 70. The newly supported devices include the Intel i960RP and RD embedded RISC processors for intelligent I/O applications, AGP2x accelerated graphics-port processor, and Pentium II MMX for desktop computing; the MIPS R5000; the Motorola MPC860 Power PC family for telecommunications and networking, MPC821 for palm-top processors, and MPC505 Power PC RISC processor; and the Siemens 80C167 embedded CISC processor for automotive applications. The TLA 700's modular design comes with up to 680 channels. Patented MagniVu sampling allows the analyzer to acquire up to 200-MHz state data and 2-GHz timing data simultaneously through one probe connection on all channels at all times. The instrument includes a digital oscilloscope and runs on a Windows 95 platform. TLA 700 prices with microprocessor support start at $18,500.

***Tektronix Measurement Business Div.**, Literature Distribution Center, P.O. Box 1520, Pittsfield, MA 01202; (800) 426-2200, press 3, code 1060.*
CIRCLE 507

New Software Adds Features To Palm-Size Logic Analyzer

Version 2.1 software for the palm-sized, 18-channel, 100-MHz Pod-A-Lyzer 8020 portable logic analyzer adds several features, including analog display of bused waveforms, user-defined symbols, logic pattern search, "auto run" capability, and a built-in pulse counter. The software offers an intuitive graphical user interface running under Windows 3.1, 3.11, 95, and NT, controlling the 8020 through a standard RS-232 serial port. Acquisition files can be shared via floppy disk or e-mail. The license-free software can be downloaded without charge from the company's internet site: http://www.pod.com. The Pod-A-Lyzer 8020 measures 3.5 in. by 1.5 in. and comes with a 64k sample buffer. The new software's pattern-search feature and find tool make it easier to find a specific logic condition⇓high, low, rising edge, or falling edge⇓ in the buffer. Synchronous acquisitions are possible up to 66 MHz.

***Boulder Creek Engineering**, 133 Mission St., Suite 104, Santa Cruz, CA 95060; (408) 460-3710; fax (408) 460-3715; e-mail: sales@pod.com.*
CIRCLE 508

Full-Featured Emulator Handles MPC860 PowerQUICC Family

The Orion/ADViCE in-circuit emulators for the Motorola MPC860 PowerQUICC family deliver full-scale, full-featured emulation for the EN, DC, DE, DH, and MH versions of the microprocessors. Pods for other members of the PowerPC family, including the MPC821, are scheduled for introduction early in 1998. The emulator uses the MPC860's on-chip debug features, including breakpoints for breaks with the cache on. This allows the instrument to monitor and trace instructions actually being processed by the execution unit and provide an execution flow trace when the cache is on. The user interface, MicroVIEW-G, is a full-featured GUI high-level debugger and emulator interface operating on either Unix Motif or Windows hosts. A multilevel event system offers superior execution control and non-intrusive, real-time trace capability. Full ADViCE systems start at $23,275, including 8k of trace and 256 kbytes of overlay memory, and Ethernet support. Up to 4.25 Mbytes of overlay are optional.

***Orion Instruments Inc.**, 1376 Borregas Ave., Sunnyvale, CA 94089; (800) 729-7700; (408) 747-0440; fax (408) 747-0688.* **CIRCLE 509**

Mid-Range PowerPC Emulator Includes Trace Memory

The SPS-1000 emulation tool for embedded PowerPC devices is a mid-range solution for designers who need features, like a trace buffer, that are not offered in standard background debug tools. The unit connects to the target system through a very flexible high-speed coaxial cable attached to a processor-specific pod. This connection allows features like 128 software breakpoints that can be set in ROM or RAM, address trigger point with delay for capturing trace data around a specific address of interest, trigger in/out lines, a 128k (512k optional) trace buffer that supports cache tracing and decoding, and flash device programming capability. Communication with the host computer is through a high-speed serial link. Included with the system is the SourceGate II source-level debugger software, which accepts the output file formats of all major compilers. The SPS-1000, with 128k of trace memory and the choice of MPC505-, MPC8xx-, or

PPC40x-specific pod costs $6990. Additional pods cost $3000. Delivery is in two weeks.

***Huntsville Microsystems Inc.**, P.O. Box 12415, Huntsville, AL 35815; (205) 881-6005; fax (205) 882-6701; http://www.hmi.com.* **CIRCLE 510**

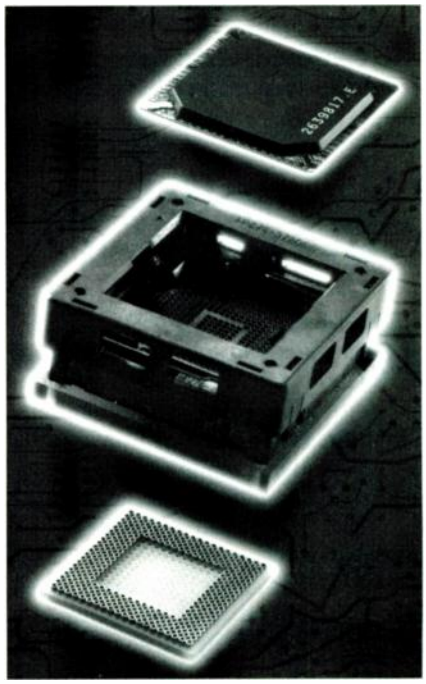
Probe Emulates PowerPC Through Logic Analyzer

A processor-specific probe combines with an inverse assembler and logic analyzer to provide emulation capability for the PowerPC 740 and 750 microprocessors from Motorola and IBM. The probe supplies run-control capability while the logic analyzer delivers real-time analysis functions. Together with a debugger connection, the setup provides a complete development and debug environment. Interfaces from third-party debugger vendors allow users to view source code, download code, set breakpoints, single-step through code, examine variables, and modify source-code variables. The probe is controlled over a LAN or RS-232 interface and links directly to the target system through a standard connector. The inverse assembler translates a trace captured by the logic analyzer into PowerPC 740/750 mnemonics and bus cycles captures, such as memory read/write interrupt acknowledge or I/O read/write. The HP E3454A PowerPC 740/750 processor probe costs $4495. The HP E2498A PowerPC 740/750 inverse assembler costs $1000, benchtop logic analyzers start at $5900, and modular analyzers start at $18,000. Delivery is in four weeks.

***Hewlett-Packard Co.**, Test and Measurement Org., P.O. Box 50637, Palo Alto, CA 94303-9512; (800) 452-4844 ext. 5554.* **CIRCLE 511**

BGA Adapter Socket Allows At-Speed Testing On Boards

The BGA Socket and Probing System II features a high-speed, plug-in design that improves performance compared to its predecessor, allowing designers to test and debug their new boards at-speed. The system is in the



same configuration as the BGA package footprint, so trace lengths and adapter height is minimal. Lead inductance is less than 2 nH. A burn-in ZIF socket allows up to 5000 chip insertions. Designers solder down the base unit, plug in the socket, and place the chip in the socket. For probing, the socket is plugged into a breakout board.The probe boards have a vertical clearance of 5 mm, which is higher than most SMT components. Prices for the BGA Socket and Probing System II start at $900.

***Emulation Technology Inc.**, 2344 Walsh Ave., Bldg. F, Santa Clara, CA 95051; (408) 982-0660.* **CIRCLE 512**

PRODUCT FEATURE

Software Improvements Accelerate Test Development, Execution Times

Version 5.0 of the virtual instrumentation development environment LabWindows/CVI offers a number of instrument driver improvements and multithreaded execution technologies that enhance program execution. Other upgrades include automated code development through interactive wizards, 3D data visualization for building advanced instrumentation systems, and an interactive dynamic link library debugging capability.

The new instrument driver wizard automatically creates VXI*plug&play*-compliant drivers that can cut test execution times by more than 50% in automated test programs. By using "run-time intelligence," the drivers allow the software to track the state of instrument settings at all times. Using this knowledge, the drivers make run-time decisions to eliminate redundant instrument commands to minimize bus traffic and instrument command processing and reconfiguration.

New wizards also simplify program development. The DAQ channel wizard interactively defines input transducers in a data-acquisition system so users don't have to handle transducer conversion algorithms and scaling in their program code. In addition, the ActiveX controller wizard simplifies ActiveX automation by automatically building code for controlling ActiveX (formerly known as OLE Automation) servers from LabWindows/CVI programs. Users can also control other software packages, like Visual Basic, Excel, LabVIEW, and Visual C.

For developers needing thread-level execution control, version 5.0 offers I/O, analysis, and user interface libraries. The libraries allow developers to separate the operations of their programs into different execution threads to maximize performance and improve CPU usage.

LabWindows/CVI Version 5.0 starts at $995 for PCs and $2995 for Sun Sparcstations and HP workstations.

National Instruments Corp.
6504 Bridge Point Pkwy.
Austin, TX 78730-5039
(800) 258-7022
fax (512) 794-8411
e-mail: info@natinst.com
http://www.natinst.com
CIRCLE 501
JOHN NOVELLINO

PCI Bus-Mastering Data Boards Offer 16 Channels To 333 ksamples/s

A series of four PCI bus-mastering data-acquisition boards feature 12-bit resolution and 16 single-ended (eight differential) channels. The boards have maximum sample rates of 150 ksamples/s or 333 ksamples/s. Also included on each board are four user counter-timers, and 23 digital I/O lines.

The boards share a common architecture, register map, connector, accessories, and software so users can easily upgrade systems when needed. The DT301 and DT302 have a 150-ksample/s digitizing rate. The DT303 and DT304 feature a 333-ksample/s rate. The DT302 and DT304 include two 12-bit analog outputs.

A 1024-location channel gain list allows users to acquire data from channels in nonsequential order and with different gains. Also, digital inputs can be read into the channel gain list, allowing monitoring of those inputs at up to 3 MHz. To focus on the specific area of interest, can acquire data using post-trigger mode, pre-trigger mode, or about-trigger mode (for data that's acquired both before and after the trigger).

Software support available includes DTx-EZ ActiveX controls for Visual Basic and Visual C++, interfaces to HP VEE and LabVIEW, and programmers' Software Development Kits for Windows 3.1, 95, and NT. Support of DT-Open Layers, a set of open standards for developing integrated software under Windows, ensures that applications can run on any similarly supported board with no changes in source code.

The DT300 boards come with Windows 3.1/95/NT device drivers and comprehensive hardware and software documentation. The DT301 costs $475; the DT302, $575; the DT303, $675; and the DT304, $775. OEM and quantity discounts are available.

Data Translation Inc.
100 Locke Dr.
Marlboro, MA 01752-1192
(800) 525-8528 or (508) 481-3700
fax (508) 481-8620
CIRCLE 502
JOHN NOVELLINO

Picture-Quality Analyzer Delivers Objective Results Automatically

The first commercially available picture-quality analysis system—the PQA200—quickly, automatically, and objectively measures the quality of video images and provides the user with a numerical value representing picture quality. The tester is useful for those who design and develop television equipment, create content, or deploy and operate compressed video systems. PQA200 measurements can be used for system or algorithm tuning and production line testing, and in applications from bit-rate optimization to end-to-end system testing.

The numeric result provided is called a picture-quality rating (PQR) and incorporates Sarnoff Corp.'s JNDmetrix technology, which was derived from years of research in developing the Just Noticeable Difference (JND) model of human vision. The goal was to achieve a strong correlation between PQR and human viewer trials. Also supplied are a peak signal-to-noise ratio; graphical, tabular, and summary data; and a *(continued on page 101)*

(continued from page 100)
JND map of the video under test. The map shows the operator the spatial location and severity of any picture problems.

The PQA200, which is based on a Windows NT server computer platform, consists of two main modules. One generates test sequences and the other compares those sequences against transported, reconstructed versions. The system offers an extensive set of standard reference scenes for out-of-service measurements and addresses the range of problems experienced by video users. Results typically are returned in less than a minute.

The PQA200, with standard 270-Mbyte/s serial component (CCIR 601) inputs and outputs, costs $49,900. Option 01, which supplies analog composite NTSC/PAL video inputs and outputs, goes for $7600. Both are available for order in the first quarter of 1998.

Tektronix Measurement Business Div.
P.O. Box 1520
Pittsfield, MA 01202
(800) 426-2200 (press 3, code 1054)
fax (413) 448-8002
CIRCLE 503
JOHN NOVELLINO

Upgraded Handheld DMMs Offer Better Overvoltage Protection

The Series III versions of the Model 70/20 family of handheld digital multimeters comply with the IEC 1010-1 safety category rating for withstanding power surges and high-voltage transients. The meters are ergonomically designed to ensure stable results in harsh environments and feature a tapered shape overmolding, and large high-contrast with a segmented bar graph for easy reading.

Models 79/77 III and 26/23 III meters have dual IEC 1010 ratings for overvoltage category III 600 V and overvoltage category II 1000 V. Models 75 and 21 III have overvoltage category III 600-V ratings, and Models 73 and 70 III have overvoltage category II 600-V ratings. The instruments are designed to help protect users against power surges and voltages transients up to 6 kV. Input ranges and functions are protected to the meter's rated voltage so that the unit won't blow a fuse or be destroyed if it's connected to a live circuit in the ohms setting.

Other enhancements include a user interface with easier access to the range and hold buttons. Also, batteries and fuses can be replaced without breaking the internal calibration shield, eliminating unneeded calibrations.

The top end 79 and 26 III meters measure ac and dc voltage and current and resistance to 40 MΩ, and offer true RMS, capacitance, frequency, low-ohms, millivolt, and microamp capabilities. All units do diode and continuity tests. Prices range from $109 to $219.

Fluke Corp.
P.O. Box 9090
Everett, WA 98206
(800) 443-5853
fax (800) 358-5332
e-mail: fluke-info@tc.fluke.com
http://www.fluke.com
CIRCLE 504
JOHN NOVELLINO

Software Integrates Test Strategies For Core-Based Designs

CTIntegrator is a comprehensive design-for-testability (DFT) software solution for integrating multiple core test methods within a system-on-a-chip (SOC) design. The tool targets the problems associated with test reuse in complex core-based ICs by assembling multiple core DFT techniques into a unified, top-level test environment.

The product addresses the issue of integration and accessibility of multiple cores in one chip. It simplifies the test task by allowing the use of several DFT methods, including built-in self-test, full scan, partial scan, and boundary scan. Also provided is an access mechanism to test cores that are delivered with precomputed test vectors, as is typical for legacy cores. Integrating the test structures and DFT techniques of the the multiple cores creates a comprehensive SOC test environment that takes full advantage of existing test patterns and fault coverage. CTIntegrator is a flexible tool that works with hard cores, firm cores, or soft cores.

As a front-end tool, CTIntegrator allows designers to develop a system-wide test access and test bus architecture described in VHDL or Verilog. The core first reads and analyzes core test requirements to establish a basis for the IC's overall test structure. It then synthesizes a test access infrastructure that links cores to chip-level test resources. Next, CTIntegrator translates core test vectors to chip boundaries, resulting in a chip-level test program. Chip-level test coverage is then immediately reported for the overall design.

CTIntegrator will initially support HP-PA, Sun Sparc, and Windows NT workstations. The tool will be available in May starting at $30,000 per seat.

Mentor Graphics Corp.
8005 S.W. Boeckman Rd.
Wilsonville, OR 97070-7777
http://www.mentorg.com.
CIRCLE 513
JOHN NOVELLINO

WE'D LIKE TO THANK OUR COMPETITORS FOR GETTING THE HELL OUT OF THE WAY.

Introducing the world's one and only 1-megabit Deep Sync™ FIFO. How dense can you get? Well, if you choose our competitors' synchronous FIFOs, you can't get very dense at all. If you choose Deep Sync FIFOs from Cypress, you get a full 1-Mbit density. You get 100-MHz speed with near-zero latency. You get a true dual-ported cell that allows asynchronous gating of the read and write clocks without requiring an FS pin. And you get industry standard architecture and pinouts–so our Deep Sync FIFOs drop right into your existing designs. Deep Sync FIFOs. Only from Cypress. When you're ready to get dense, don't bother talking to our competitors. Talk to Cypress.

Cypress (and only Cypress) Deep Sync FIFOs

Size	Part No.	Speed	I_{CC}(max.)	Leads/Package	Availability
128K x 9	CY7C4291	10ns	40mA	32/PLCC	Now
128K x 9	CY7C4292	10ns	40mA	64/TQFP	Now
64K x 18	CY7C4285	10ns	50mA	64/TQFP	Now
64K x 9	CY7C4281	10ns	40mA	32/PLCC	Now
64K x 9	CY7C4282	10ns	40mA	64/TQFP	Now
32K x 18	CY7C4275	10ns	50mA	64/TQFP	Now

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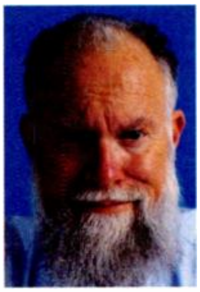
BOB PEASE

Bob's Mailbox



Dear Bob:

Re: Paul Leonard and his comments on trekking in the Sept. 15 "Bob's Mailbox." INSPIRATION is something that's desperately needed in today's electronics industry. And getting away from the computer, the desk, and drawing board and thinking about the great outdoors allows the brain to create, as opposed to reworking old ideas. And let's be honest—how many new ideas happen today? Most are squashed-up combinations of existing ideas. Where are today's Colpitts, Hartleys, Edisons, Morses, Bells, and Marconis?

Contemplate the ratio of the circumference of your head first to the circumference of the Earth, then to that of the solar system, and you may be able to cope with the ratio of head to galaxy, but at that point the brain says, "Hey, man, this is beyond conventional thought!" At this point, the brain may go into overdrive and creativity may occur. Or it gives up and looks for something it can comprehend. In the great outdoors, there really is nothing that can be consciously comprehended. How does a pinhead-size seed grow into a tree? I could at this point believe in God, but I prefer to accept that mankind's lack of comprehension requires a God to explain the unexplainable. After all, who believes in the *Rain God* today? OK, OK, so the great outdoor rain can be comprehended, but where were the two H_2 and the O_2 before the big bang, and where did they come from in the first place?

One of my best inspirations came in a forest north of the Arctic Circle as I enjoyed the midnight twilight. It was a blast of creativity that I guess was layered down under ages of routine miniaturization of existing circuits and repackaging of old ideas. And no, it is not for publication—if it works it will make enough money for me to go to Nepal and return to Finland (I hope).

At the end of August, I sat on a clifftop in West Wales looking over the ocean at a distant flash of a lighthouse on some isolated rock. And I wondered: was it transistorized timer operating a power semiconductor or lenses in a rotating metal frame floating on mercury round a constantly lit lamp? I'll never know for sure, but it made me think about old and new methods. Came up with several reasons why the floating on mercury was the better method.

(Yeah, but not far north of the arctic circle!!! Nor on Lake Superior, where it gets below –40YC—rigging a heater for the mercury might be too much work!—RAP)

And to Mike McGinn, who also commented on trekking in the same issue. Mike, about your list of "I can'ts." I hope that you write it in pencil and keep an eraser next to it. A girl I know has a terrible time with cardiac illness. Her list of "I can'ts" is written in pencil, except for the the top item which is "I can't give up until this list is empty" and written in ink.

On occasion, she manages to rub out a "I can't" and rewrite it in ink on the "I did" list. Against all odds she has made it to the age when portable, intelligent heart defibrillators are available, giving her more freedom of movement. One day, hopefully, a transplant may cure her. Until then, her eraser will be busy, but the list will grow. She told me that each "I can't" was read as "I can't yet." And if any reader doesn't carry an organ-donor card, why not ?

BERNARD GREEN
via e-mail

(Note to Mike: Fortunately, you ARE able to go hiking. You just can't go far from civilization where WHEELS and cheap electric power make your dialysis feasible.—RAP)

All for now. / Comments invited!
RAP / Robert A. Pease / Engineer
rap@webteam.nsc.com—or:

Mail Stop D2597A
National Semiconductor
P.O. Box 58090
Santa Clara, CA 95052-8090

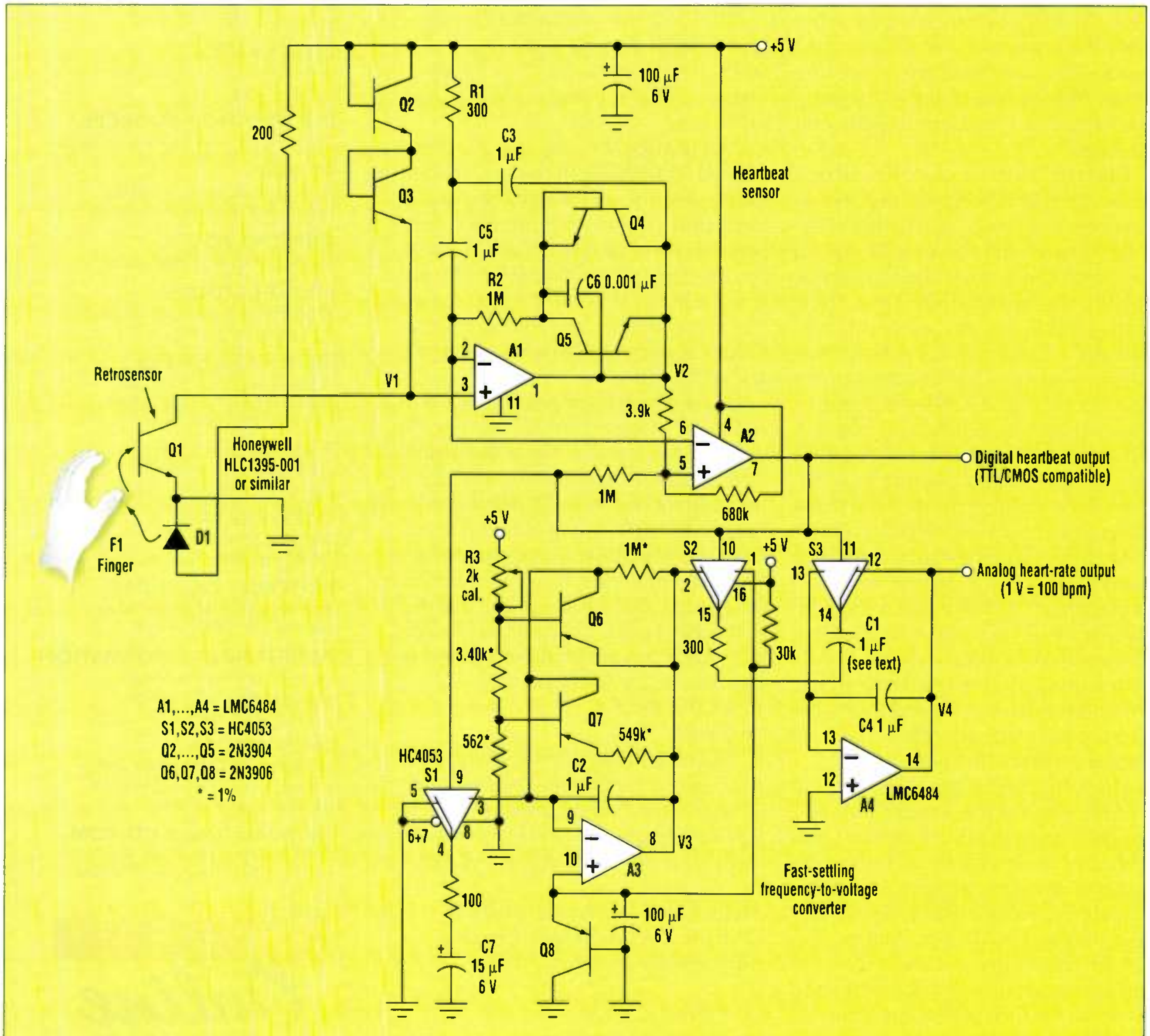
Circle 520

Build Your Own Optical Heart-Rate Sensor

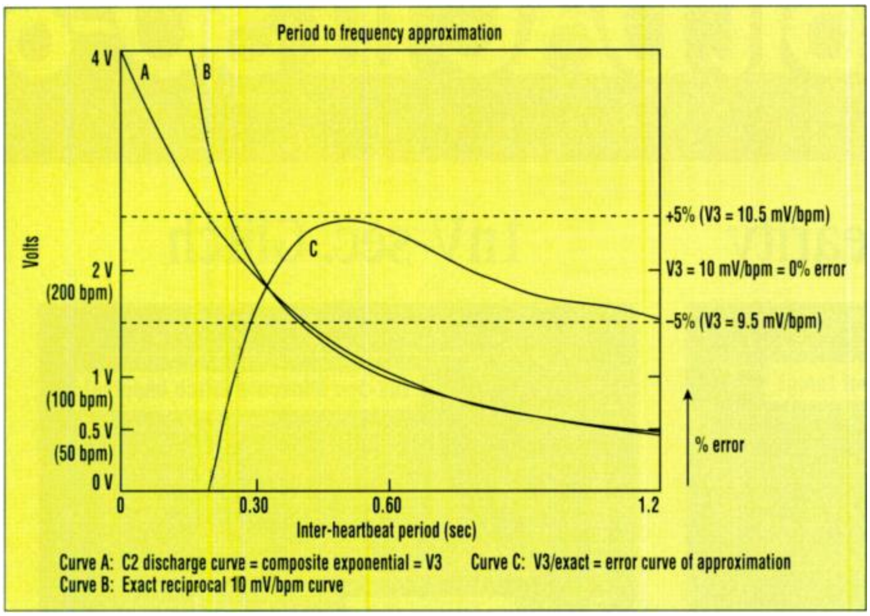
W. STEPHEN WOODWARD
Venable Hall, CB3290, University of North Carolina,
Chapel Hill, NC 27599-3290; e-mail: woodward@net.chem.unc.edu.

Plenty of noninvasive methods exist for electronically sensing the human heartbeat. The job can be done acoustically (stethoscope or Doppler), mechanically (sphygmomanometer), electrically (EKG), and optically. One handy optical technique presented here exploits the fact that tiny subcutaneous blood vessels (capillaries) in any patch of skin (fingertip, ear lobe, etc.) furnished with a good blood supply, alternately expand and contract in time with the heartbeat. An ordinary infrared LED/phototransistor pair can sense this rhythmic change as small but detectable variations in skin contrast *(Fig. 1, upper half)*.

When gently held against the skin (too much pressure will flatten the surface capillaries and suppress the pulsation effect), some of the radiation from D1 reflects back into Q1. Q1's photocurrent produces an ac signal across Q2 and Q3 of $\approx$500-μV p-p for every 1% change in skin reflectance. This logarithmic relation-



1. The upper half of this optical heart-rate sensor contains an infrared LED /phototransistor that senses rhythmic change as small variations in skin contrast. The lower half constitutes a "zero-ripple" frequency-to-voltage converter that's optimized for human pulse-rate measurement.



2. C2's discharge is nonlinear. R6, R7, and Q7 synthesize a composite exponential curve V3 that approximates the reciprocal relationship between pulse period and pulse rate.

ship is constant over many orders of magnitude of photocurrent. Consequently, reliable circuit operation is possible despite wide variations in skin contrast and light level. A1 and the surrounding discrete components comprise a high-gain adaptive filter that rejects ambient optical and electrical noise (mostly 60-Hz pickup) and presents a cleaned-up signal to comparator A2 so that it can extract a digital pulse-rate signal.

A2's TTL/CMOS-compatible output is suitable for direct input to a digital period-measurement circuit, and for such applications, that's all that's needed. But for some simple heart-rate display situations, an analog representation of pulse rate is convenient. So the lower half of Figure 1 illustrates an unusual, "zero-ripple," frequency-to-voltage converter (FVC) uniquely optimized for human pulse-rate measurement.

Most FVCs are characterized by an unavoidable trade-off between response time and output ripple. Usually, in order to have an acceptable output ripple of the order of a few percent, the settling time of the converter must be at least ten periods of the lowest expected input frequency. Normal human hearts usually beat at rates within the 4:1 range of 50 to 200 beats per minute (bpm) ∪0.83 Hz to ∪3.3 Hz. A conventional frequency-to-voltage converter (FVC) would therefore need an unpleasantly long (>10 second) output settling time. Some converters avoid this limitation but tend to be complex (ELECTRONIC DESIGN, *Feb. 21, 1994, p. 115)*.

The relatively simple "instant-settling" FVC in Figure 1 employs a period-to-rate approximation trick that works well in this application. To understand the idea, consider S1, which is arranged to alternately switch C7 between ground and A3's summing point. When a rising edge from A2 at S1 pin 9 connects C7 to A3 and C2, the resulting transfer of charge into C2 causes A3's output to slew positive until clamped by Q6. Adjusting R3 trims the clamp voltage and thereby sets full-scale calibration for the circuit.

C2 immediately begins to discharge back toward zero, but it doesn't do so linearly. Instead, R6, R7, and Q7 synthesize a composite exponential curve V3 *(Fig. 2)* that, from 285 (210 bpm) to 1250 ms (48 bpm), is a good approximation (within 5%) of the reciprocal relationship between pulse period and pulse rate. Thus, each time the digital signal from A2 returns high, V3 will equal the reciprocal of the time elapsed since the previous transition and, therefore, the actual instantaneous heart rate. S2, S3, and C1 then transfer V3 to sample/hold A4 for continuous output as V4 = 10 mV/bpm. If C1 = C4, only one charge transfer is needed for instant convergence.

However, normal hearts have significant beat-to-beat aperiodicity that sometimes causes V3 to jump around quite a bit. If desired, choose C1 < C4 to provide a degree of signal averaging and thus smooth this effect out. Q8 provides V_{be} and temperature compensation for the Q6 and Q7 breakpoint voltages. Thus, these transistors should be thermally coupled for good tracking. Notice that with an appropriate change of time constants, this circuit also has general potential as an optical tachometer for other difficult low-contrast applications.

Circle 521

Series LED Driver Operates On 3-V Input

FRAN HOFFART
Linear Technology Corp., 1630 McCarthy Blvd., Milpitas, CA 95035-7487.

The circuit described here consists of a constant current source with a voltage compliance of 30 V *(see the figure)*. It's capable of driving a series string of LEDs at currents up to 100 mA. A switching regulator using a SEPIC (single-ended primary inductance converter) topology drives the LEDs with a regulated constant current at efficiencies up to 79%. U1, an LT1512 switching IC, provides an output voltage of approximately 28 V to drive the LEDs. This device operates at 500 kHz and features an internal 1.5-A switch, voltage and current feedback pins, and a low quiescent-current shutdown mode. The circuit is designed to drive 16 series-connected red LEDs from an input voltage of 3 to 10 V.

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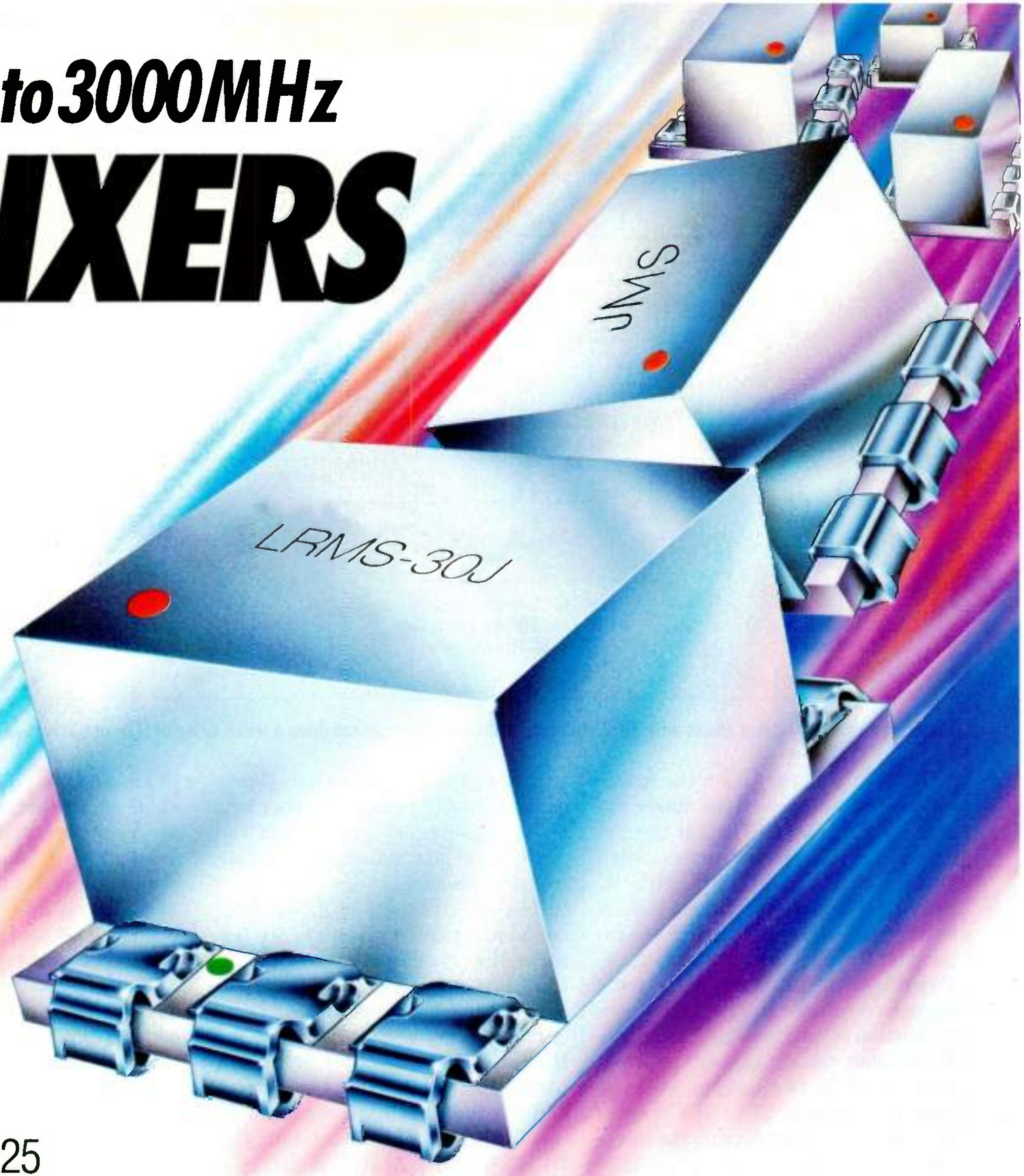

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JMS-1LH	+10	2-500	DC-500	5.75	55	45	8.45
JMS-1MH	+13	2-500	DC-500	5.75	60	45	9.45
JMS-1H	+17	2-500	DC-500	5.90	50	50	11.45
JMS-2L	+3	800-1000	DC-200	7.0	24	20	7.45
JMS-2	+7	20-1000	DC-1000	7.0	50	47	7.45
JMS-2LH	+10	20-1000	DC-1000	6.5	48	35	9.45
JMS-2MH	+13	20-1000	DC-1000	7.0	50	47	10.45
JMS-2H	+17	20-1000	DC-1000	7.0	50	47	12.45
JMS-2W	+7	5-1200	DC-500	6.8	60	48	7.95
JMS-5	+7	5-1500	DC-1000	6.0	50	30	9.95
JMS-5LH	+10	5-1500	DC-1000	6.0	50	35	10.95
JMS-5MH	+13	5-1500	DC-1000	5.7	57	35	11.95
JMS-5H	+17	5-1500	DC-1000	5.9	50	35	12.95
JMS-11X	+7	5-1900	5-1000	6.7	35	37	4.25*
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Notes: *10-49 qty. **LRMS-30J model is compatible with aqueous wash.

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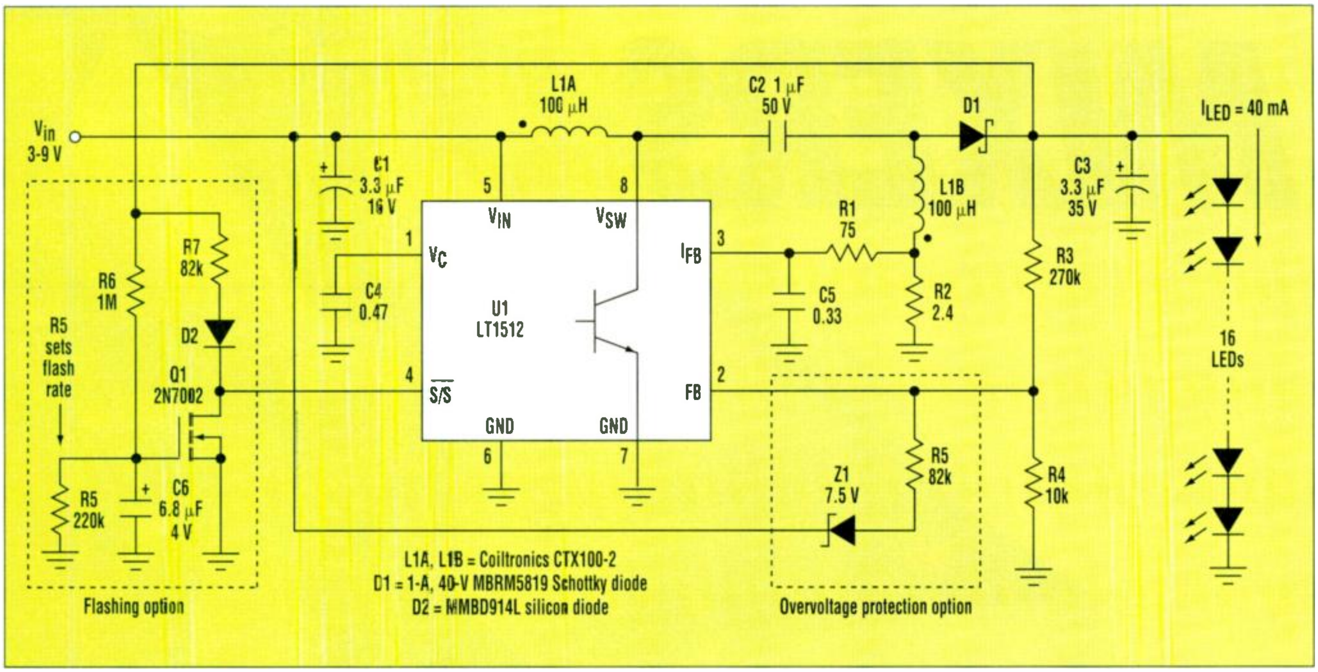

Featuring a constant current source with 30-V voltage compliance, this circuit can drive a series string of LEDs at currents up to 100 mA.

The limiting factor on the maximum input voltage and the number of series-connected LEDs that the circuit can drive is the maximum switch voltage rating of 40 V. In a SEPIC converter topology, the maximum voltage seen by the switch is the input voltage plus the output voltage. To protect the internal switch from excessive voltage, input overvoltage protection is provided by Z1 and R5. If the input voltage exceeds approximately 10 V, the output voltage (which is typically 27 to 30 V) begins decreasing, thus protecting the internal switch from exceeding the 40-V maximum switch rating. Input voltage can be as high as 25 V without damage, although the LEDs turn off as the input voltage exceeds 10 V.

The maximum number of LEDs that can be driven depends on the total voltage required by the series string of LEDs and the maximum input voltage (the forward voltage drop of different types of LEDs can range from 1.6 V to as much as 3.6 V each, depending on color, current, manufacturer, and other factors).

All surface-mount components can be used in this design, resulting in less than 0.8 in.^{2} of pc-board area. Good electrical and thermal pc-board layout practices are necessary because of the 500-kHz switching frequency and because of the power dissipated by the internal switch. Generous amounts of pc-board copper near U1's leads (except for the switch lead, pin 8) assist in conducting heat away from the package.

The inductor consists of two identical windings on a toroidal core (observe the phasing of the windings). Input and output capacitors can be either ceramic or tantalum, with ripple current rating greater than 150 mA RMS. Ceramic capacitors are recommended for the coupling capacitor C2 and the compensation capacitor C4 (use X7R ceramic material for C4). D1 is a 0.5- or 1-A, 40-V Schottky or ultra-fast recovery diode.

Looking at the diagram, circuitry for flashing the LEDs is contained within the dashed line. With the values shown, the LEDs are on for approximately 120 ms out of every second. Varying R5 between 68 kΩ and 5 MΩ changes the flash rate from fast (five flashes per second) to slow (one flash every three seconds). Other flash rates and/or duty cycles are possible by selecting different resistor and/or capacitor values.

U1 includes inputs for sensing both output voltage and output current. The average current through L1B and R2 is equal to the LED current. The sense voltage developed across R2 is used to regulate the LED current. Other LED currents can be programmed by selecting a resistor value for R2 that will develop 100 mV at the desired LED current. Programming resistors R3 and R4 limit the maximum output voltage to approximately 33 V in the event of an open LED connection.

When driving 16 red LEDs at 40 mA (30 V across the LEDs), the input current required is approximately 600 mA at 5 V in, and 200 mA at 8 V in. Flashing the LEDs at a 10% duty cycle will drop the average input current by a factor of 10. Pulling the shutdown pin low shuts the circuit down, drawing approximately 15 µA of quiescent current.

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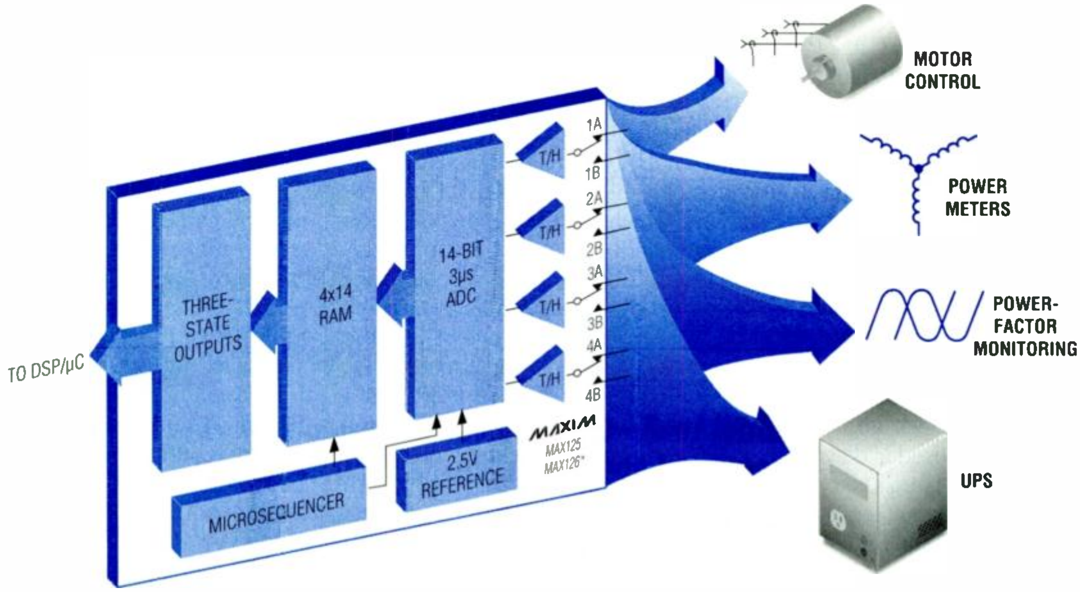

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Circle No. 132 - For U.S. Response
Circle No. 133 - For International

Circle 522

Add Remote/Local Control To Distributed Control System

S.V. NAKHE
Laser Program, CAT, P.O. CAT, Indore 452013, India;
fax: 91-0731-488401; e-mail: nakhe@cat.ernet.in.

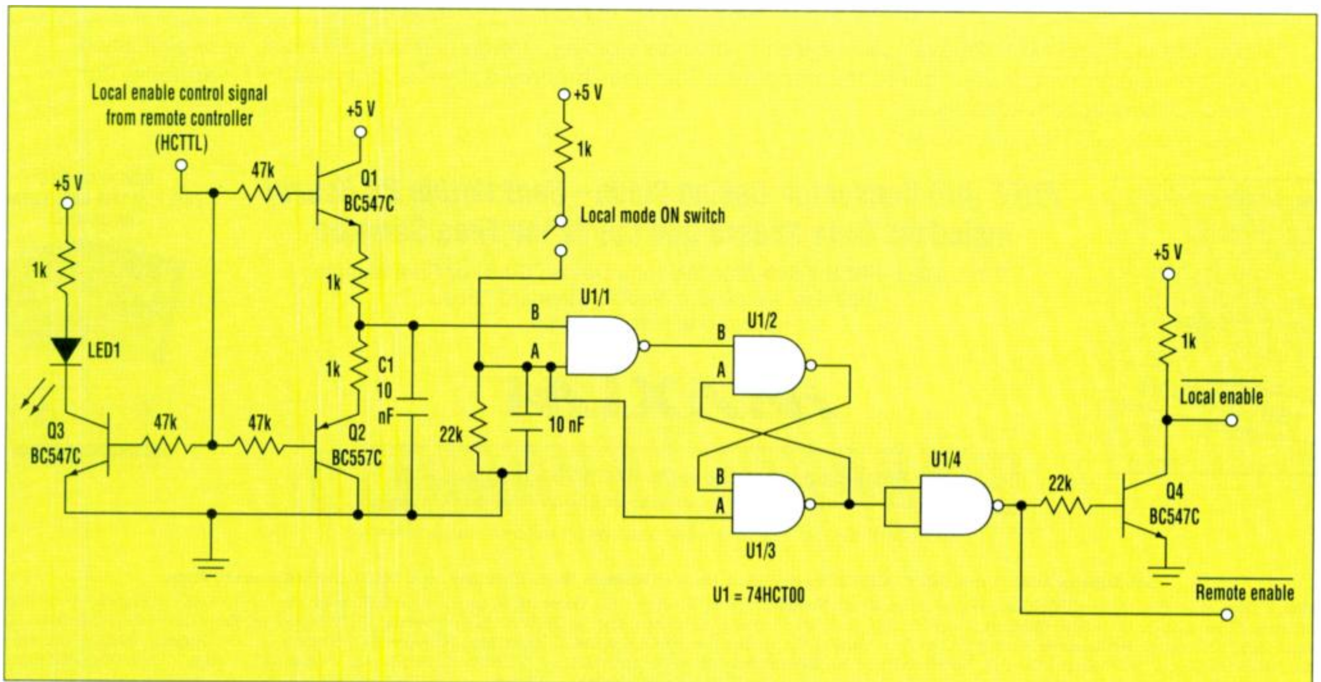
The circuit described here implements remote/local transfer of control for distributed-control-system equipment. I have used this circuit as a part of the electronic circuitry for the remote/local control of a laser system. The laser can be controlled from a remote computer system located away from the laser system, or from a local control unit that's actually mounted on the system.

The circuit should be used in distributed control systems that are controlled both locally and remotely. Such systems should normally run under remote control, and in this case, local control should be disabled. Local control is possible only with the permission of the remote controller. Also, once the equipment is put under local control, the remote system should not take over the control on its own unless the local control is released by the operator.

This circuit should be mounted in the equipment's local-control panel. In-system remote/local enable signals are connected to chip select pins of tristate buffers, which allow either remote or local commands to control the equipment.

U1/2 and U1/3 form a basic flip-flop, triggered by the logic function generated by U1/1. When the local enable control signal goes high, transistor Q1 is on and Q2 is off. Capacitor C1 charges to logic high level, and input B of U1/1 goes high. The input A of U1/1 and of U1/3 changes to a logic high when the local mode switch is closed. Then the output of U1/1 goes low and the output of U1/2 goes high, causing the output of U1/3 to go low. U1/4 inverts this signal and enables local mode. Now even if the local enable control signal goes low when S1 is closed (this happens if the remote computer tries to take over the control once the local mode is on), the local mode of the equipment control isn't disturbed. That's because the output of U1/2 and U1/3 remains unchanged to high and low state, respectively. Thus, once local mode is established, control can't be reclaimed by the remote computer unless it's released from local-control mode manually.

When the remote control is on (i.e. S1 is off and the local-enable-control signal is low), the A and B inputs of U1/1 are low, making the output high. Because the A input of U1/3 is low, its output is high and remote mode is on. In this case, if switch S1 is closed, the A input of both U1/1 and U1/3 goes high. However, the outputs of U1/1, U1/2, and U1/3 don't change. Consequently, once the equipment is in remote mode, it can't be put in local mode without permission of the remote controller. Permission to go into local mode is given by making the local-enable signal high. A panel indicator (LED1) may be used to indicate the status of the local-enable control signal.



Mounted on a local control panel, this circuit implements remote/local transfer of control for distributed-control-system equipment.

First In 100-W Power-Supply Series Now Available

The Labpac B 301/S1 is the first unit in a series of 100-W power supplies with output voltages up to 250 V. It's equipped with a digital presetting of the voltage and a DPM for measuring voltage and current. With an output voltage of 25 V, the output current of the secondary switcher supply is 4 A; at 5 V the maximum output current is 16 A. In the power boost mode, these values can be increased for short times to 8 A and 20 A, respectively up to a maximum of 300 W. Within the range of 0 to 19.99 V, output-voltage-meter resolution is 10 mV. The Labpac B 301/S1 automatically switches this resolution to 100 mV once the voltage reaches 20 V or more.

All secondary step-down switch-mode power supplies need a good overvoltage protection, because a failure of the switch could lead to a high and uncontrollable output voltage. To prevent this, the B 301/S1 has several protecting circuits that are aimed at handling "every conceivable failure." The ripple and regulation at 10 mV and 0.01% is said to be "almost as good as with linear supplies." Load regulation is 0.03% and load transients recover within 250 µs.. AV

***Oltronix**, Grillenweg 4, 2500 Biel 6, Switzerland; phone: +41-32/342 44 45.* **CIRCLE 480**

IC Controls Analog Functions Of Communications Devices

The UBA1707 IC brings the "analog" functions of cordless-phone base stations and telephone answering machines under full digital control. The IC provides all of the line interface and analog speech-processing functions necessary in these applications—an on-chip loudspeaker amplifier, microphone amplifier, and electronic hook switch control. The chip can adapt to different telephone line standards, allowing manufacturers to produce a single "universal" pc-board assembly that's usable in telephone equipment worldwide.

To meet the specific requirements of telephone standards worldwide, its line interface can be programmed into voltage or current regulation modes with independent control of the equipment's dc and ac set impedance. Operation at dc line voltages as low as 1.2 V allows several telephones to operate in parallel on the same line. The transmit amplifier of the UBA1707 handles input signals with amplitudes of up to 350 mV with a line current of 15 mA, or up to 750 mV with a line current of 90 mA for less than 2% THD. The biMOS device is available in a 28-lead SO or 28-lead SSO package at volume prices (1 million per year) for approximately $1.15 each. AV

***Philips Semiconductors**, P.O. Box 218, 5600 MD, Eindhoven, The Netherlands; phone: +31 40 272 20 91, fax +31 40 272 48 25.* **CIRCLE 481**

Battery Disconnect Switch Comes In Single Small-Outline Package

According to Temic, the Si4720CY is the first battery disconnect switch to be used with NiCd, NiMH or lithium ion cells integrating p-channel MOSFETs and a level-shifted gate drive within one package—a 16-pin, surface-mount, small-outline package. The integrated level-shifted gate drive circuit and the p-channel MOSFETs together offer the reverse-blocking capabilities necessary in power-supply designs when several different types of batteries are used or when an insulation from the recharge current is required during the recharge period. Both cases are common with portable computers and portable measuring instruments.

Because both internal p-channel MOSFETs work in a high-side switch configuration, the Si4720CY allows design engineers to eliminate about a dozen discrete components. Both switches within the Si4720CY can be used separately for such functions as monitoring the battery recharging or switching between battery and ac adaptor. However, they also can be employed together with Schottky diodes, which are needed to achieve the reverse-blocking capabilities required when switching between two battery packs. With voltages of 10 V and currents of 1 A, the typical on-resistance of the bidirectional blocking/conduction switch is 0.0155-Ω, while the leakage current at 10 V is specified to be 1 µA. AV

***Temic Telefunken Microelectronic GmbH**, P.O. Box 35 35, 74025, Heilbronn, Germany; phone: +49-7131/67 29 45; fax: +49-7131/99 33 42.* **CIRCLE 482**

Smart Pointers Help Speed 8051 Embedded Development

A novel 8051 ANSI C compiler, developed by Crossware, features smart pointers that produce efficient code without requiring the programmer to declare specific pointer types. The smart-pointer technology avoids the added programming effort required when using special 8051-specific keywords in code. Smart pointers work out from the context in which they're used and which memory area(s) they're required to point at. Then they configure themselves to the most appropriate pointer type. Another feature of the compiler is the linker, which performs a full type-check across the complete program. The compiler is available for both DOS and Windows 95/NT 4.0. RE

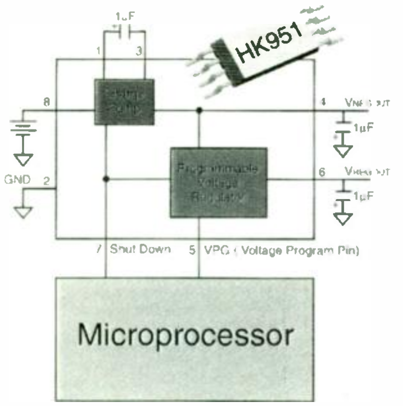
***Crossware Products**, St. John's Innovation Centre, Cowley Rd., Cambridge, CB4 4WS, United Kingdom; phone: +44 (0) 1223 421263; fax: +44 (0) 1223 421006; Web: http://www.crossware.com.* **CIRCLE 483**

Edited by Roger Engelke

Circle No. 136 - For U.S. Response
Circle No. 137 - For International

Low-Noise, Adjustable DC-DC Converter Biases GaAs FETs

Specifically designed to provide the negative bias for GaAs FETs used in cellular phones, the HK-951 dc-dc converter comes with a programmable, internal, 5% linear regulator with a noise



ripple of 1 mV. The converter accepts inputs of 2.6 to 6.4 V, uses a 150-kHz charge pump with a maximum output of 15 mA, and can be controlled from the output of a digital-to-analog converter of a microprocessor, or by a resistor divider. A shutdown pin drops power consumption to below 1 µA. The converter also can be used for controlling LCD contrast. Packaging is in an eight-pin SSOP. Pricing is $1.65 each per 1000. PM

Shoreline Electronics Inc., *2098 B Walsh Ave., Santa Clara, CA 95050; Will Bateson, (408) 987-7733; fax (408) 987-7735.* **CIRCLE 460**

2-W DC-DC Converters Have Dual Outputs

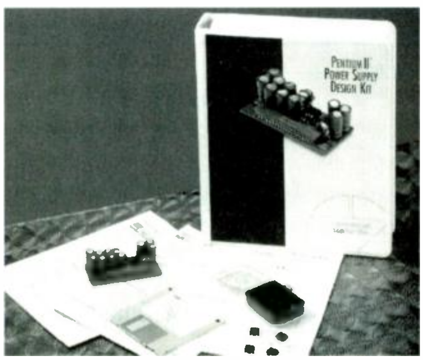
Comprising six models, the RM Series of dc-dc converters are dual-output devices that handle up to 2 W. The converters have input-voltage options of

5, 12, and 24 V and output options of ±12 and ±15 V. Packaged in a 24-pin DIP, the devices measure 1.25 by 0.8 by 0.4 in. and have an input-to-output isolation and capacitance of 850 V and 50 pF, respectively. The efficiency is 58%. Other features include an output noise 50 mV and a line and load regulation of 0.5%. Pricing for the 5-V-input version is $23.13 per 1000. PM

Calex Mfg. Co. Inc., *2401 Stanwell Dr., Concord CA 94520; Stu Williams, (800) 542-3355; fax (510) 687-3333.* **CIRCLE 461**

Pentium II Design Kit And MOSFETs Save Up To 20%

The IRVRM2 Pentium II Design Kit includes an integrated compensation loop, internal pull-up resistors, and 20-V HEXFET power MOSFETs to reduce the component count by up to



20%. Aimed at 233- to 266-MHz processors, the kit's MOSFETs have an $R_{DS\,(on)}$ ranging from 0.013 to 0.023 Ω, depending on the gate-source voltage, and a drain current of 37 to 56 A. The kit is available free of charge. PM

International Rectifier, *100 N. Sepulveda Blvd., El Segundo, CA 90245; Sales Dept., (310) 322-3331; fax (310) 252-7166.* **CIRCLE 462**

Distributed-Power Front Ends Are Bellcore Compliant

The FE series of 500-W to 6-kW, ac-dc, distributed-power front ends target redundant, N+1, and battery backup

systems. The modules are available in two racking systems, featuring multiple input rails to enhance fault tolerance. Other features include remote diagnostics, and overvoltage and overtemperature protection. Pricing is $0.70/W in 100-piece quantities. PM

Lambda Electronics, *515 Broad Hollow Rd., Melville, NY 11747; Kenneth Knizek, (516) 694-4200; fax (516) 752-2627.* **CIRCLE 463**

100-W, Open-Frame Switcher Is Smallest To Date

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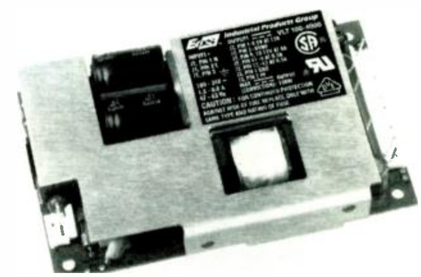

5 by 1 in., the supply has an efficiency of 87%, a universal input, UL, CSA, VDE, and CE approvals, and is convection-cooled. Pricing is $57 each.

EOS Corp., *906 Via Alondra, Camarillo, CA 93102; Kevin Gero, (805) 484-9998; fax (805) 454-5854; e-mail: info@eoscorp.com; Internet: http://www.eoscorp.com.* **CIRCLE 464**

Modular VRLA Battery Targets Telecom And UPS Applications

Featuring gelled electrolyte, the Dynacel/DGX valve-regulated, lead-acid battery comes in a tubular plate and is capable of 1200 cycles at 80% depth of discharge to 1.75 V per cell. The tubular positive plate construction uses vertical lead spines surrounded by a lead tube held in place by a fiberglass wrap. This design presents 60% more surface area than a similar flat plate, making better use of the paste material. The battery is rated from 170 to 4080 Ah. Pricing starts at $4488 with delivery in eight weeks. PM

Yuasa-Exide Inc., *P.O. Box 14145, Reading, PA 19612-4145; Andrea Friedman, (800) 538-3627; fax (610) 372-8613; e-mail: andreaf@ptd.net; http://www.yuasa-exide.com.* **CIRCLE 465**

125mA NEGATIVE SUPPLY USES ONLY TWO 1µF CAPS

1MHz Charge Pump Fits in 0.06in², Inverts 2V to 5.5V Input

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- **Selectable Switching Frequency:** 500kHz/1MHz (MAX1681) 125kHz/250kHz (MAX1680)
- **Uses Small Capacitors** (1µF for the MAX1681)
- **125mA Output Current**
- **3.5Ω Output Impedance**
- **Inverts or Doubles V_{IN}**
- **2.0V to 5.5V Input Range**
- **1µA Shutdown Current**

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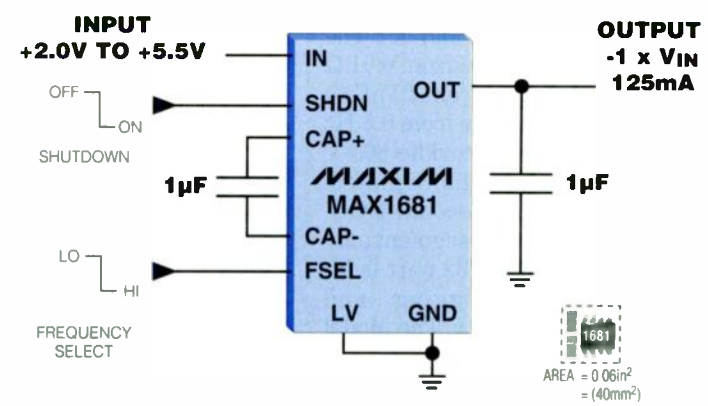

Boost or invert 2.0V to 5.5V with an ultra-compact circuit. The MAX1681, in an 8-SO package, delivers 125mA using only two tiny ceramic capacitors and no inductors.

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Small, Benchtop DMM Delivers 50,000 Counts At 0.25%

The Model 5490 digital multimeter offers 50,000-count resolution and 0.25% accuracy in a compact full-function benchtop instrument. Measurement capabilities include dc voltage to 1000

V at 0.25% accuracy, ac voltage with true RMS (ac or ac+dc), and overvoltage protection. Current ranges are from 500 mA to 10 A (ac and dc). The unit measures resistance from 0.01 Ω to 50 MΩ, capacitance from 10 pF to 50,000 µF, and frequency from 0.5 Hz to 500 kHz. The meter provides 600-V dc capacitance and resistance protection. Besides the 50,000-count LCD, the display includes a 34-segment analog bar graph. An RS-232 port is included for data logging and record/printout capability. The Model 5490 costs $675. JN

***B+K Precision**, 4353 W. Lawrence Ave., Chicago, IL 60630; (773) 725) 9252; fax (733) 725-9385; http://www.bkprecision.com.*
CIRCLE 466

PC Scope Card Digitizes To 10 Msamples/s At 16 Bits

The CompuScope 1016 is an ISA-bus plug-in card that delivers 16-bit sampling at speeds to 10 Msamples/s with a 5-MHz bandwidth and an 85-dB spurious-free dynamic range. Because the single-channel card's sampling rate is faster than the ISA-bus transfer rate, the unit comes with memory that can store up to eight million samples for later transfer to the user's computer. In Multiple Record mode, the CompuScope 1016 allows "stacking" of acquisitions from successive triggers. The included GageScope software allows users to run the card like an oscilloscope with no further programming. The software will store, analyze, and print acquired data and convert it to an ASCII format for export to other applications. The CompuScope 1016-256K costs $8995. Software drivers in LabVIEW, LabWindows CVI, HP VEE, and Matlab cost $250 each. The DLL for Windows 3.1 and Windows 95 and the Windows NT device driver cost $250 each. JN

***Gage Applied Sciences Inc.**, 1233 Shelburne Rd., Suite 400, South Burlington, VT 05403; (800) 567-4243; (514) 337-6893; fax (800) 780-8411 or (514) 337-8411; e-mail: prodinfo@gage-applied.com; Internet: http://www.gage-applied.com.*
CIRCLE 467

ISDN "Server In A Box" Offers Full Simulation Capability

The ISDN 3500 International Flash Emulator and Protocol Analyzer is a complete ISDN server in a box. The portable, standalone instrument simulates the ISDN protocols for North American (NI-1), Europe (European

Telecommunications Standards Institute), and Japan (Nippon Telephone & Telegraph). Included are codesets 0, 5, 6 and 7, and NETwork and ESCape message types. The unit provides the services of a two-line central office switch for both U and S/T interfaces.

Emulating end-to-end, real-time ISDN-BRI calls, the ISDN 3500 performs complete call-handling procedures without a switch, PBX, or PC development system, thus eliminating the variables inherent in testing over telephone company lines. In addition, a protocol-analyzer mode offers the ability to develop, monitor, and diagnose layer 2 and 3 interaction from the telephone company. The unit's flash memory permits downloads of software upgrades. The ISDN 3500 is available immediately for $7500, which includes Protocol Analyzer for Windows software, an ISDN-BRI Protocol Reference, an RJ-11 serial cable, an RJ-11-to-DB-9 adapter, and manual. JN

***Merge Technologies Group Inc.**, 211 Gateway Rd. West, Suite 201, Napa, CA 94558-6274; (800) 824-7763 or (707) 252-6686; fax (707) 252-6687; e-mail: merge@mergetech.com; Internet: http://www.mergetech.com.*
CIRCLE 468

Simultaneous FIB/SEM System Eases Wafer Defect Correction

The DualBeam XL830 focused ion beam/scanning electron microscope (FIB/SEM) workstation is the latest in a family of three-dimensional defect review, analysis, and characterization

tools. The system's new SEM column delivers 3-nm resolution from 1 to 30 kV and balanced-field, in-lens detection to ensure exceptional topographic detail, down to hole visibility, and enhanced grain boundary imaging.

The FIB column is optimized for fast, precise milling. The operator can quickly mill through the wafer's surface layers to uncover and access subsurface defects. Successively milling into a defect or particle while taking high-resolution SEM images at various depths (and analyzing surface and internal points for elemental composition) provides complete 3D defect characterization. The system's Predictive User Interface makes operation easy by keeping the submicron defect in the field of view during various operations and viewing from various angles. Call for price and availability information. JN

***FEI Co.**, 7451 N.W. Evergreen Pkwy., Hillsboro, OR 97124-5830; (503) 640-7500; fax (503) 640-7509.* **CIRCLE 469**

Windows-Oriented GUI Targets Embedded Applications

DOS Buttons is a software development tool that lets users build Windows-like user interfaces for DOS applications. Interfaces can include windows, buttons, and display bars, but without the cost and overhead associated with full-blown windowing systems. Programmers can quickly add GUIs that accept keyboard, mouse, touch screen, and pen input while occupying only a small amount of memory. Embedded DOS applications include handheld data collection, field service and personal-communication devices, factory instrumentation, and process control panels.

DOS Buttons provides a set of customizable graphical elements. The window elements can be located anywhere on the screen and assigned any size, color, or label. Within a window, programmers can incorporate pop-up windows, text, display bars, keypads, and a variety of buttons. There also is a set of graphical primitives, such as arcs, circles, and lines, that let programmers create their own GUI elements.

The button elements in DOS Buttons can be either momentary push or two-position (single or double action). The code executed by a button push can depend on a button's position. DOS Buttons also provides thermometer-like display bars for high-speed scrolling or display of data. The bars can be used for display or moved with a mouse for input.

DOS Buttons is integrated with Communication Intelligence Corp.'s PenDOS used for developing pen-centric applications. PenDOS also lets the DOS GUI accept, compress, and store handwritten input. Optimized for embedded environments, DOS Buttons occupies about 50 kbytes in the run-time environment. Production royalty is $1 per copy with a 100-copy minimum. TW

***Annasoft Systems**, 11838 Bernardo Plaza Court, San Diego, CA 92128; (619) 674-6155.* **CIRCLE 470**

Compiler Supports New Embedded C++ Spec

Embedded C++ (EC++) is the specification for a subset of C++ that's specifically designed for embedded systems. The EC++ specification was drafted by a technical committee initiated by several Japanese semiconductor manufacturers and later joined by U.S. companies. Now the first compiler product is appearing in the form of the C++/EC++ developed by Green Hills Software. It will initially be available for the Motorola 68k and PowerPC families of processors. Other versions for the Hitachi SH, MIPS, Coldfire, and NEC V800 processors will follow later this year.

EC++ supports many of C++'s object-oriented facilities, which enhance code reuse and simplify the partitioning and maintenance of complex code. However, it omits a number of features that aren't considered essential for embedded development. Ultimately, these may significantly increase code size and reduce run-time efficiency. Such features include multiple inheritance, virtual base classes, exception handling, run-time type identification and mutable specifiers.

In traditional C++ compilers, the run-time overhead associated with these features often is incurred whether they are actually used or not. Others are useful to the programmer, but require skilled use. Otherwise, they will lead to inefficient and bloated code.

The C++/E++ is fully integrated with the Green Hills MULTI development environment, which includes a window-oriented editor, an RTOS-aware debugger, run-time error checker, and project/version control. Price for the Windows 95, WindowsNT version is $3900. The Unix versions are priced at $5400. TW

***Green Hills Software Inc.**, 30 West Sola Street, Santa Barbara, CA (805) 965-6044.* **CIRCLE 471**

Toolkit Glues HTML GUI to Embedded C Code

One supposedly easy way to web-enable embedded devices is to add one of the many embedded HTTP servers that are becoming available. However, actually linking data fields and the like in an HTML page to the underlying C code that runs the device involves a non-trivial amount of work. WebControl lets you add Web-based management to an embedded device that separates development of the HTML-based user interface from the device's underlying C code.

WebControl provides a rapid integration tool with a "knowledge accumulator" that allows you to identify resources, such as C variable names, that you may want to link with HTML resources (e.g., a data entry field). A system of markup tags (called MagicMarkups) enables dynamic linking of the device's native attributes to HTML files. Then a glue code generator produces code that can be linked with the device's C code, which is recompiled and run on the device, thus interfacing the HTML GUI to the device code.

WebControl also includes a ready-made web server that features separation of HTML and C source code, runs in less than 30 kbytes of memory, and is extensible to support emerging standards like Java and ActiveX.

The WebControl developer's kit is priced starting at $35,000. TW

***Rapid Logic**, 100 Webster St., Suite 101, Oakland, CA 94607; (510) 267-0737; http://www.rapidlogic.com* **CIRCLE 472**

Windows-Based IDE Supports GNU Tool Chain

A Windows-based visual development environment is now being offered for the GNU compiler and debugger technology developed by Cygnus Solutions , Sunnyvale, Calif. GNUPro 2.0 Cygnus is packaging the IDE for integration with microprocessor manufacturers' evaluation boards, game manufacturers, set toolbox platforms, and the development environments offered by real-time OS vendors.

The GNUPro 2.0 IDE integrates with Cygnus' technology that includes a visual make file with project selection and the ability to launch compiler options, a graphical debugger with assembler, linker/loader utilities, compiler flags and assembler dialog boxes for warnings, optimization selections, and configuration of compilers and assemblers.

The initial release of GNUPro 2.0 will be bundled with two Motorola evaluation boards—for the MPC 600 and MPC 800, respectively. Support for a broad range of embedded processors will follow. The Motorola packages will be available from Motorola's RISC products division. Pricing starts at $695. TW

***Cygnus Solutions**, 1325 Chesapeake Terr., Sunnyvale, CA 94089; (408) 542-9600; http://www.cygnus.com.*
CIRCLE 473

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Capacitors Available On-line

Capacitors On-line is the second in a planned series of Internet-based services from Time Electronics, Hauppauge, N.Y. Engineers and purchasers can log onto the site at http://www.time.avnet.com/caonline/ca.htm to access the company's inventory of capacitors from manufacturers including AVX, Mallory, Murata, Philips, Roederstein, Vishay/Sprague, United-Chemi-Con, and Vitramon. Once there, they can "build" capacitor part numbers by entering the specifications they need. A graphical-user interface also allows customers to search a database of thousands of capacitors by part number. Cross referencing of manufacturers helps speed up the users inquiry.

Time's first Internet service was Connectors On-line. Future services will handle military connectors, resistors, switches, relays, fans, and motors. Time is a member of Avnet's OEM Marketing Group.

Arrow Handling Tantalum, Ceramic Caps From Kemet

Arrow Electronics Inc., Melville, N.Y., has completed a worldwide distribution agreement for tantalum and ceramic capacitors manufactured by Kemet Corp. Arrow said the agreement will strengthen Kemet's global presence, particularly in Europe and Asia.

"Our two organizations have meshed very well in quickly establishing selling strategies, logistics, systems interfaces, and availability of Kemet products for Arrow customers," according to Kemet president Terry R. Weaver

"We believe this will be an important addition to our line card," said Stephen P. Kaufman, chairman and chief executive officer of Arrow. "We are pleased with the pace at which Kemet's field organization has moved to support all of our worldwide locations."

Sterling Inks All-Location Pact With Thomas and Betts

An all-location distribution agreement has been signed by Sterling Electronics Corp., Houston, Tex., and Thomas and Betts Corp., the Memphis-based maker of interconnect products. The agreement also includes Marsh Electronics and Sterling/Semad, which are wholly owned subsidiaries of Sterling Electronics.

Sterling began working with Thomas and Betts earlier this year when the manufacturer acquired Augat Inc., whose products Sterling had been distributing for more than 30 years. "During this short period we have been quite impressed by their growth strategies and the long-term commitment to a position of leadership in the connector industry," said David Goforth, Sterling's senior vice president of connector marketing. "Our plan will be to work closely with all levels of the Thomas and Betts organization to aggressively seek new business for both companies."

Jack Killoren, Sterling's senior vice president of marketing, called the agreement a significant step. "Thomas and Betts' continuing investment in acquisitions and new product development, coupled with Sterling's focus on connector marketing, provide significant growth opportunities for both companies," he said.

Specialty Glass Maker Signs Up Firms In Four Locales

Four distributors have been added by LightPath Technologies Inc., Albuquerque, N.M., which produces patented Gradium glass products for high-performance industrial, medical, consumer, telecommunications, computer network, and photonic applications. The company expects the distribution agreements to open up new markets in Silicon Valley, Canada, Scandinavia, and Italy.

Marcon Sales Inc., Milpitas, Calif., will market Gradium products to its diverse electronics-industry customer base, targeting OEMs of IC inspection equipment and videoconferencing and closed-circuit cameras. In Canada, Melles Griot Canada Inc. will sell to corporate and OEM clients, as well as to universities and government research facilities. Permanova Lasersystem AB will sell Gradium lenses to industrial and scientific laser markets in Sweden, Denmark, Norway, and Finland. In Italy, A-Tek will distribute to customers in industrial laser, infrared camera, optical component, and sensor applications.

Gradium glass can precisely steer light internally, collect and concentrate energy, and separate wavelengths carrying high-speed data. It can be manufactured cost-effectively in all sizes and volumes, notes LightPath.

Western Canada Office Opened By Capstone

Capstone Electronics Corp., Aurora, Colo., has opened a sales office in Calgary, Alberta, Canada. The new office is strategically located to serve four western provinces: Alberta, British Columbia, Manitoba, and Saskatchewan.

"Our newest location is serving a large customer base that needs a reliable, service-oriented distributor of passive, electromechanical, and connector components," said Kim Corcoran, Capstone's recently appointed regional director. "Capstone is able to offer customers in Western Canada next-day service from our centrally located warehouse in Denver." Corcoran had been North American sales manager with Farnell Electronics Services, which was acquired earlier this year by Capstone's parent company, Arrow Electronics Inc.

The company appointed Peter Bond as general sales manager of the Calgary branch. Bond has been with Capstone as a field sales representative for the past two years.

Capstone operates 11 regional centers and one ISO-certified connector assembly supercenter.

Bisco Adds Sales Facility

Bisco Industries Inc. recently open a sales office in Woodland Hills, Calif. The Orange, Calif.-based distributor of electronic components and fasteners now has 12 sales facilities and five distribution centers throughout the U.S. According to Ali Sar, sales manager for the new office, "As a local vendor, we have a great opportunity to better service our customers." The office is located at 6324 Variel Ave., Woodland Hills, CA 91367. For more information, call (818) 610-0011 or (805) 643-9879.

Avnet Plans For Succession

Leon Machiz, chairman and chief executive officer of Avnet Inc., Great Neck, N.Y., will retire as CEO next June 26 and as chairman at the conclusion of his term in November 1998. Roy Vallee, currently Avnet's vice chairman, president, and chief operating officer, will succeed Machiz as chairman and CEO. Vallee has held a number of executive positions since joining Avnet in 1977. Machiz has headed the company since 1988. During that time, Avnet tripled its sales and net income and expanded its operations from North America to Europe, the Asia-Pacific region, and South Africa.

People On The Move

Sheryl McCormick has been promoted to general manager of the Dallas sales office of Sterling Electronics Corp. She has been with the Houston-based company for five years, most recently as field sales representative in the Dallas area...Kimberly Maidrand has been promoted to facility sales manager for Bisco Industries' San Diego office. She has worked for Bisco since the opening of the San Diego office two-and-a-half years ago and has been assistant sales manager...All American Semiconductor Inc., Miami, Fla., has promoted three executives. Howard Flanders was named executive vice president. He has been with the company for six years and will retain his duties as chief financial officer. John Jablansky was named senior vice president of product management. A 15-year employee, he has been vice president of product management. Sam Wiggins was named vice president and controller. He has been with the company for five years as controller.

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March 23	2/10/98
April 6	2/24/98
April 20	3/10/98
May 1	3/21/98
May 13	4/2/98
May 25	4/14/98
June 8	4/28/98
June 22	5/12/98
July 6	5/26/98
July 20	6/9/98
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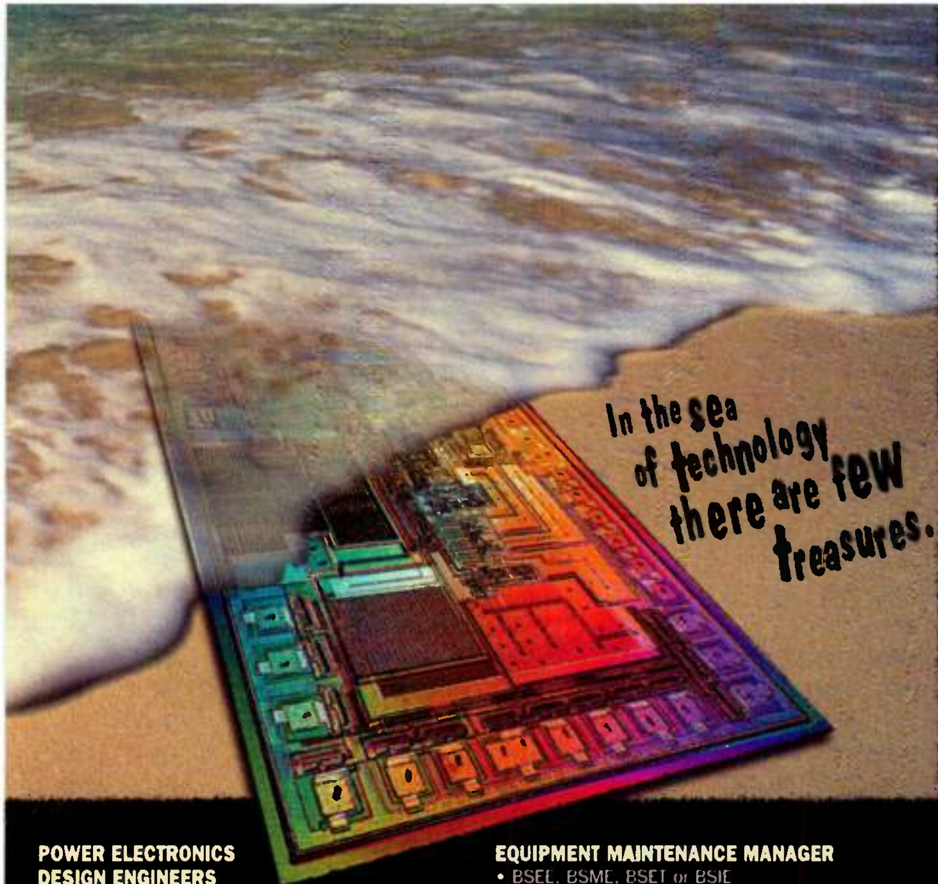

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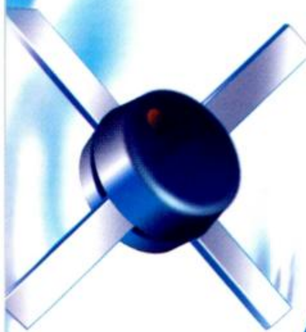
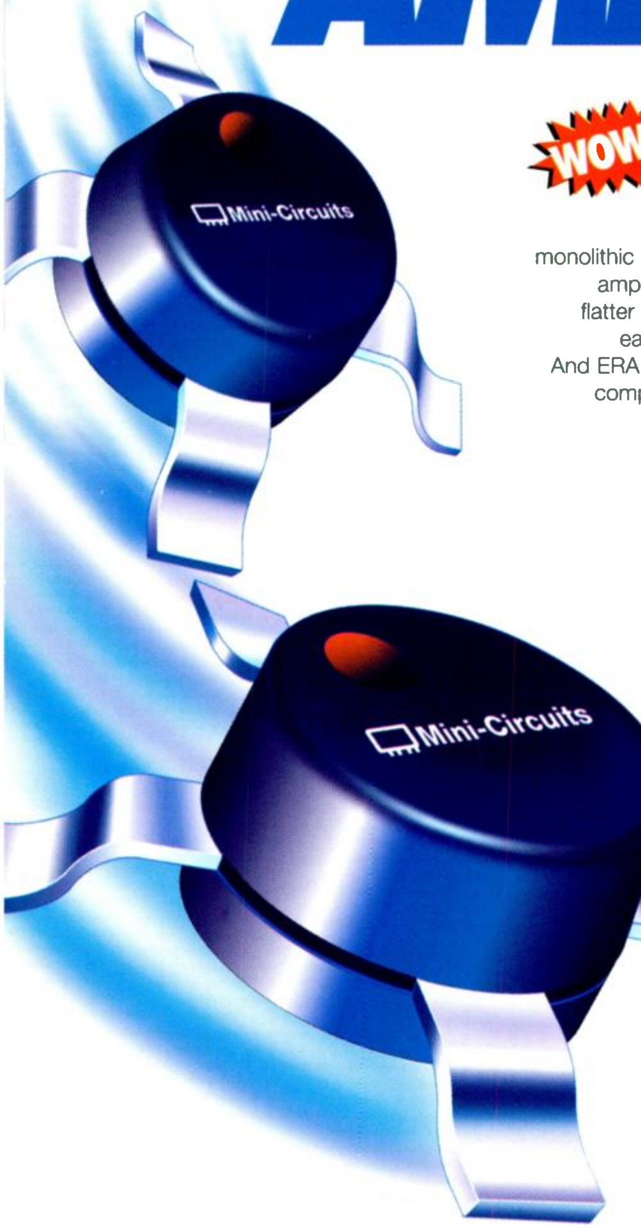


NEW ERA AMPLIFIERS



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ERA-1SM	DC-8000	11.8	11 3	5.5	26 0	40	1 85
ERA-2	DC-6000	15.6	12 8	4 7	26 0	40	1 95
ERA-2SM	DC-6000	15.2	12 4	4.6	26 0	40	2 00
ERA-3	DC-3000	20.8	12 1	3.8	23 0	35	2 10
ERA-3SM	DC-3000	20.2	11 5	3.8	23 0	35	2 15
ERA-4	DC-4000	13.5	▲17.0	5 5	▲32.5	65	4 15
ERA-4SM	DC-4000	13.5	▲16.8	5.2	▲33.0	65	4 20
ERA-5	DC-4000	18.8	▲18 4	4.5	▲33.0	65	4 15
ERA-5SM	DC-4000	18.5	▲18.4	4.3	▲32.5	65	4 20
ERA-6	DC-4000	11.3	▲18.5	8 4	▲36 5	70	4.15
ERA-6SM	DC-4000	11.3	▲17.9	8 4	▲36 0	70	4.20

Note: Specs typical at 2GHz, 25°C. Exception: ▲ indicates typ. numbers tested at 1GHz
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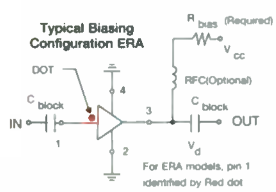
ERA-1 ERA-1SM
ACTUAL SIZE

Typical Biasing Configuration ERA



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