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ELECTRONIC DESIGN

TECHNOLOGY • APPLICATIONS • PRODUCTS • SOLUTIONS

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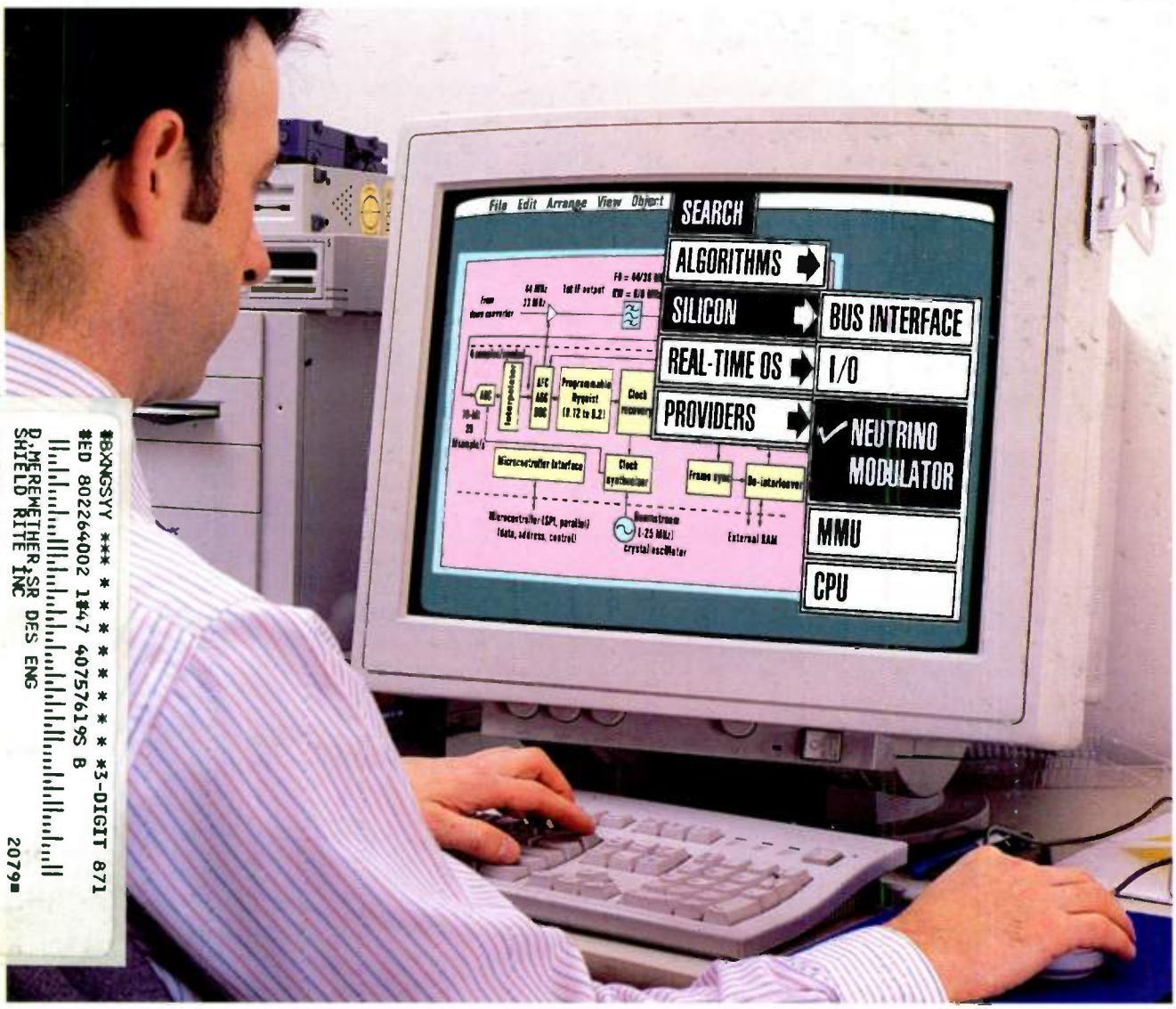
JANUARY 12, 1998



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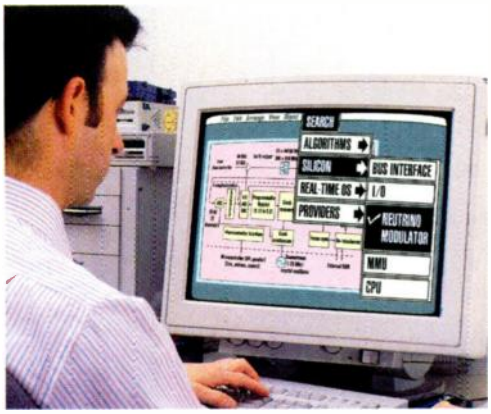
January 12, 1998 Volume 46, Number 1

EDITORIAL OVERVIEW



1998 Technology Forecast: Intellectual Property 41

TECH INSIGHTS

TECH INSIGHTS

DEPARTMENTS

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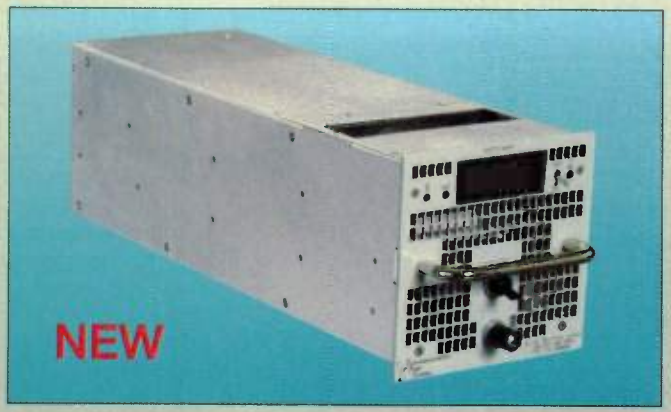

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January 12, 1998 Volume 46, Number 1

EDITORIAL OVERVIEW

TECH INSIGHTS

PIPS

PIPS

BOARDS & BUSES

QUICKLOOK

COVER ILLUSTRATION BY: BRUCE JABLONSKI

Jesse H. Neal Editorial Achievement

1967 First Place Award	1978 Certificate of Merit
1968 First Place Award	1980 Certificate of Merit
1972 Certificate of Merit	1986 First Place Award
1975 Two Certificates of Merit	1989 Certificate of Merit
1976 Certificate of Merit	1992 Certificate of Merit

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64Mb	x4, x8, x16

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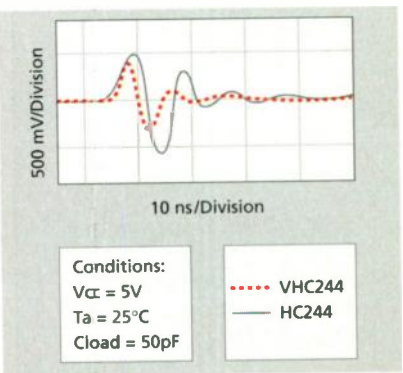
Specification Comparison

VHC	HC
8mA drive	4mA drive
8.5ns max prop delay (5.3ns typical at 25°C)	24ns max prop delay (11ns typical at 25°C)
40uA max static current	80uA max static current
PDIP, SOIC, TSSOP package	PDIP & SOIC package
74VHCxx	74HCxx
Over-voltage protection	No
3V AC performance guaranteed	No

Ground Bounce: V_{OLV}/V_{OLP}



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JANUARY 1998

Annual Reliability & Maintainability Symposium/Product Quality & Integrity (RAMS), Jan. 20-22. Anaheim Marriott, Anaheim, CA. Contact V.R. Monshaw, Consulting Services, 1768 Lark Lane, Cherry Hill, NJ 08003; (609) 428-2342.

Photonics West, Jan. 24-30. San Jose, CA. Contact The SPIE Exhibits Dept., P.O.Box 10, Bellingham, WA 98227-0010; (360) 676-3290; fax (360) 647-1445; e-mail: exhibits@spie.org.

Seventh Security Symposium, Jan. 26-29. Marriott Hotel, San Antonio, TX. Contact USENIX Conference Office, 22672 Lambert St., Suite 613, Lake Forest, CA 92630; (714) 588-8649; fax (714) 588-9706; e-mail: conference@usenix.org; Internet: http://www.usenix.org.

IEEE Power Engineering Society Winter Meeting, Jan. 31-Feb. 5. Tampa, FL. Contact Jim Howard, Tampa Electric Co., P.O. Box 111, Tampa, FL 33601; (813) 228-4653; fax (813) 228-1333; e-mail: j.howard@ieee.org.

FEBRUARY 1998

Developer's Conference & Interoperability Workshop, February 2-4. Hyatt Regency Hotel and Conference Center, Kauai, Hawaii. Contact Ellen Gooch (212) 226-2042, ext. 228; e-mail: egooch@usar.com.

IEEE International Solid-State Circuits Conference (ISSCC '98), Feb. 5-7. San Francisco Marriott, San Francisco, CA. Contact Diane Suiters, Courtesy Associates, 655 15th St. N.W., Washington, DC 20005; (202) 639-4255; fax (202) 347-6109; e-mail: isscc@courtesyassoc.com.

Portable by Design, Feb. 9-13. Santa Clara Convention Center, Santa Clara, CA. Contact Rich Nass, Electronic Design, 611 Route 46 West, Hasbrouck Heights, NJ 07604; (201) 393-6090; fax (201) 393-0204; e-mail: portable@class.org.

The Wireless Symposium and Exhibition, Feb. 9-13. Santa Clara Convention Center, Santa Clara, CA. Contact Bill Rutledge, Penton Publishing, 611 Rte. 46 West, Hasbrouck Heights, NJ 07604; (201) 393-6259; fax (201) 393-6297; instant faxback (800) 561-7469; Internet: http://www.penton.com/wireless.

Gigabit Ethernet Conference (GEC '98), Feb 10-12. San Jose Wyndham Hotel, San Jose, CA. Contact Aurelia Cassidy, Conference Pros, P.O. Box 9126, San Jose, California 95157; (800) 351-6000; fax (408) 526-9195; e-mail: conference_pros@compuserve.com.

Sixth Annual Automated Imaging Association Business Conference, Feb. 10-12. Buena Vista Place, Orlando, FL. Contact Automated Imaging Association, P.O. Box 3724, Ann Arbor, MI 48106; (313) 994-6088; fax (313) 994-3338.

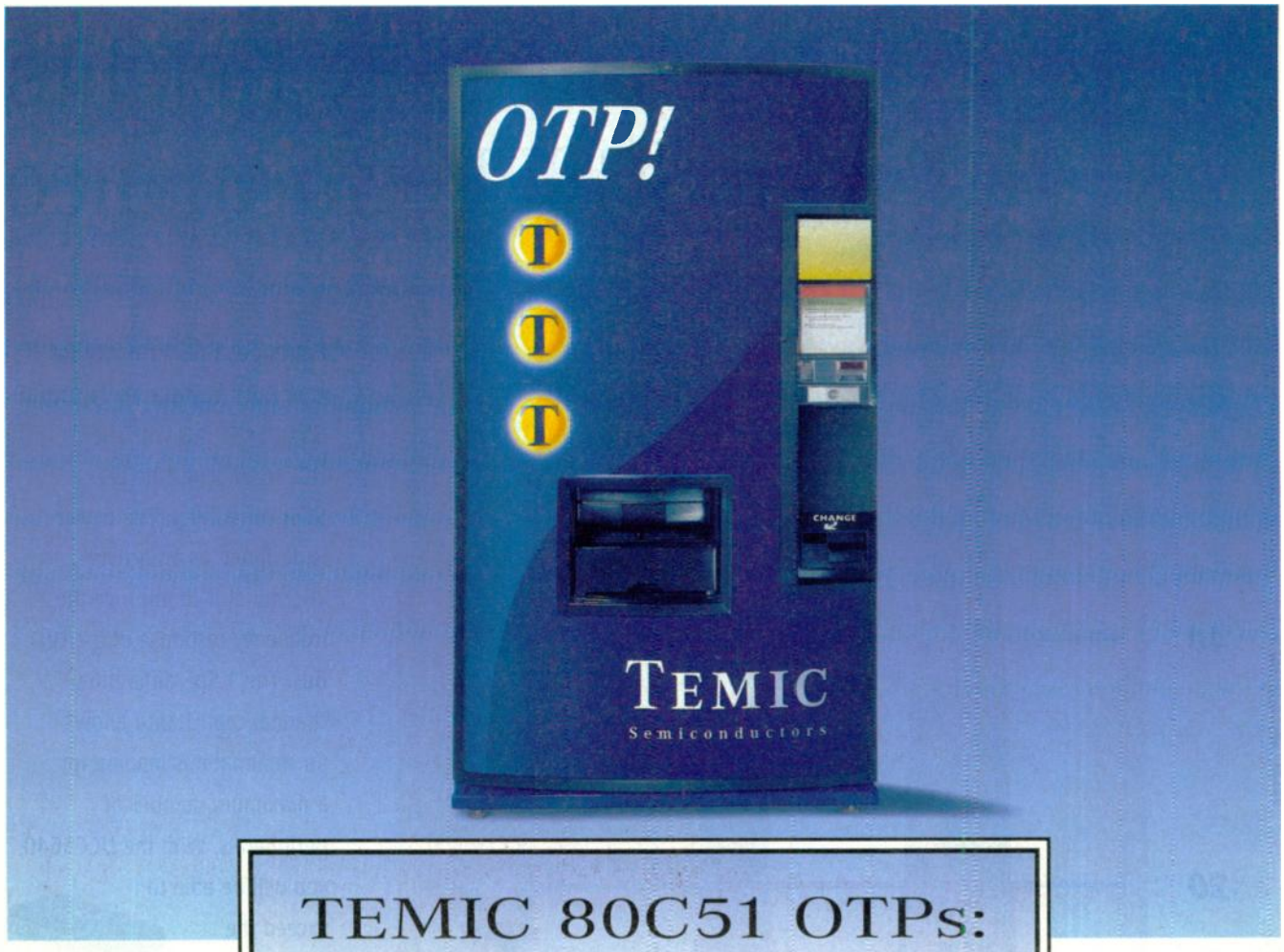
Asia-South Pacific DAC (ASP-DAC '98) and EDA TechnoFair (EDATF), Feb. 10-13. Pacifico Yokohama Convention Center, Yokohama, Japan. Contact ASP-DAC '98 Secretariat, c/o Convex Inc., Ichijoji Bldg., 2-3-22 Azabudai, Minato-ku, Tokyo, 106 Japan; +81 3-3589-3355; fax +81 3-3589-3974; e-mail: convex@po.iijnet.or.jp.

IEEE Applied Power Electronics Conference and Exposition (APEC '98), Feb. 15-19. The Disneyland Hotel, Anaheim, California. Contact Pam Wagner, Courtesy Associates, 2000 L St. N.W., Suite 710, Washington, D.C. 20036; (202) 973-8664; fax (202) 331-0111; Internet: http://www.apec.conf.org.

Conference on Optical Fiber Communication (OFC '98), Feb. 22-27. San Jose Convention Center, San Jose, CA. Contact Lisa Myers, OSA Conference Services, 2010 Massachusetts Ave., N.W., Washington, D.C. 20036-1023; (202) 416-1980; fax (202) 416-6100; e-mail: ofc.info@osa.org.

Design, Automation, and Test in Europe Conference and Exhibition (DATE '98), Feb 23-26. Le Palais des Congres de Paris, Porte Maillot. Contact European Conferences, 11C Wemyss Pl., Edinburgh EH3 6DH, UK; +44 131-225-2892; fax +44 131-225-2925.

38th Israel Conference on Aerospace Sciences, Feb. 25-26. Tel-Aviv & Haifa. Contact Technion-Israel Institute of Technology, Haifa 32000, Israel; 972-4-8292713; fax, 972-4-8231848; e-mail: alice@aerodyne.technion.ac.il.



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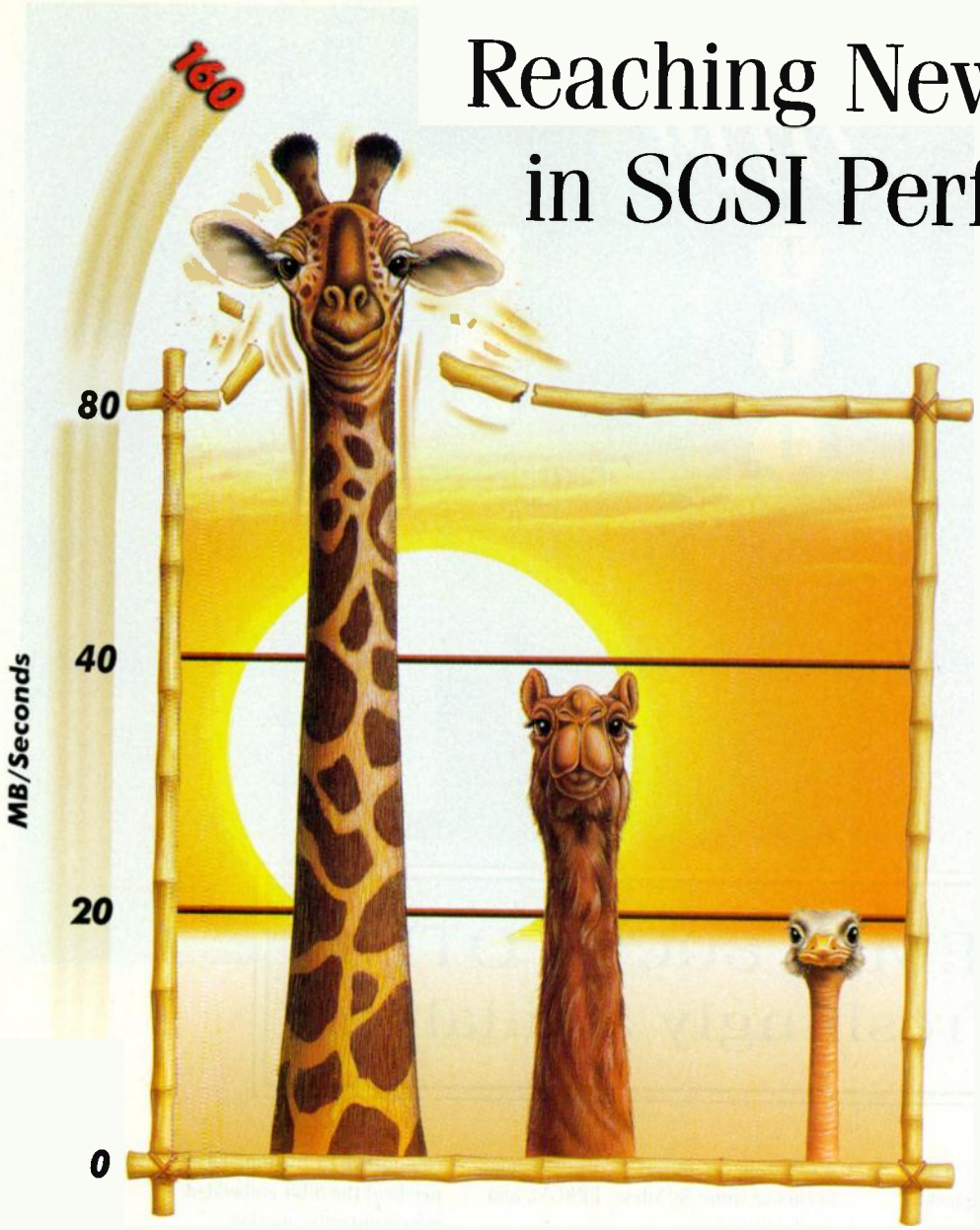

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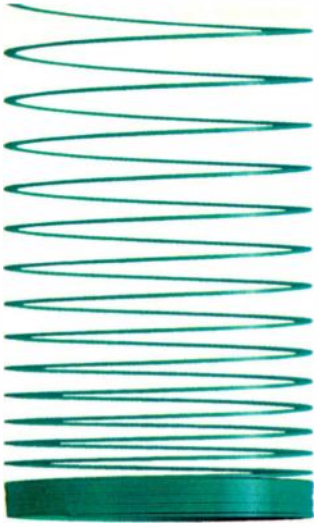
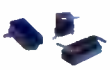
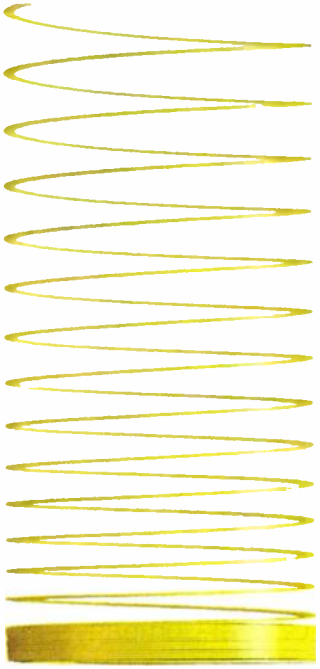
Designer's Kit C108





Mini Springs

2.5 - 43 nH
Q up to 210, IDC up to 3.0 A
Designer's Kit C102



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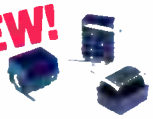

Midi Springs

22 - 120 nH
Q up to 150, IDC up to 3.5 A
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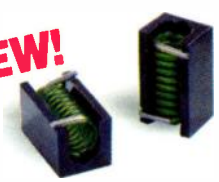
NEW!



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MARCH 1998

Computer Telephony Conference and Exposition '98, March 3-5. Los Angeles Convention Center, Los Angeles, California. Contact Computer Telephony '98, 1265 Industrial Highway, Southampton, Pennsylvania 18966; (215) 355-2886; fax (215) 355-4112.

International Verilog Converfence and VHDL International User Forum (IVC/VIUF), March 16-19. Santa Clara Convention Center, Santa Clara, California. Contact MP Associates, 5305 Spine Rd., Suite A, Boulder, Colorado 80301; (303) 530-4562; fax (303) 530-4334; e-mail: lee@mpa-net.com; Internet: http://www.hdl-con.org.

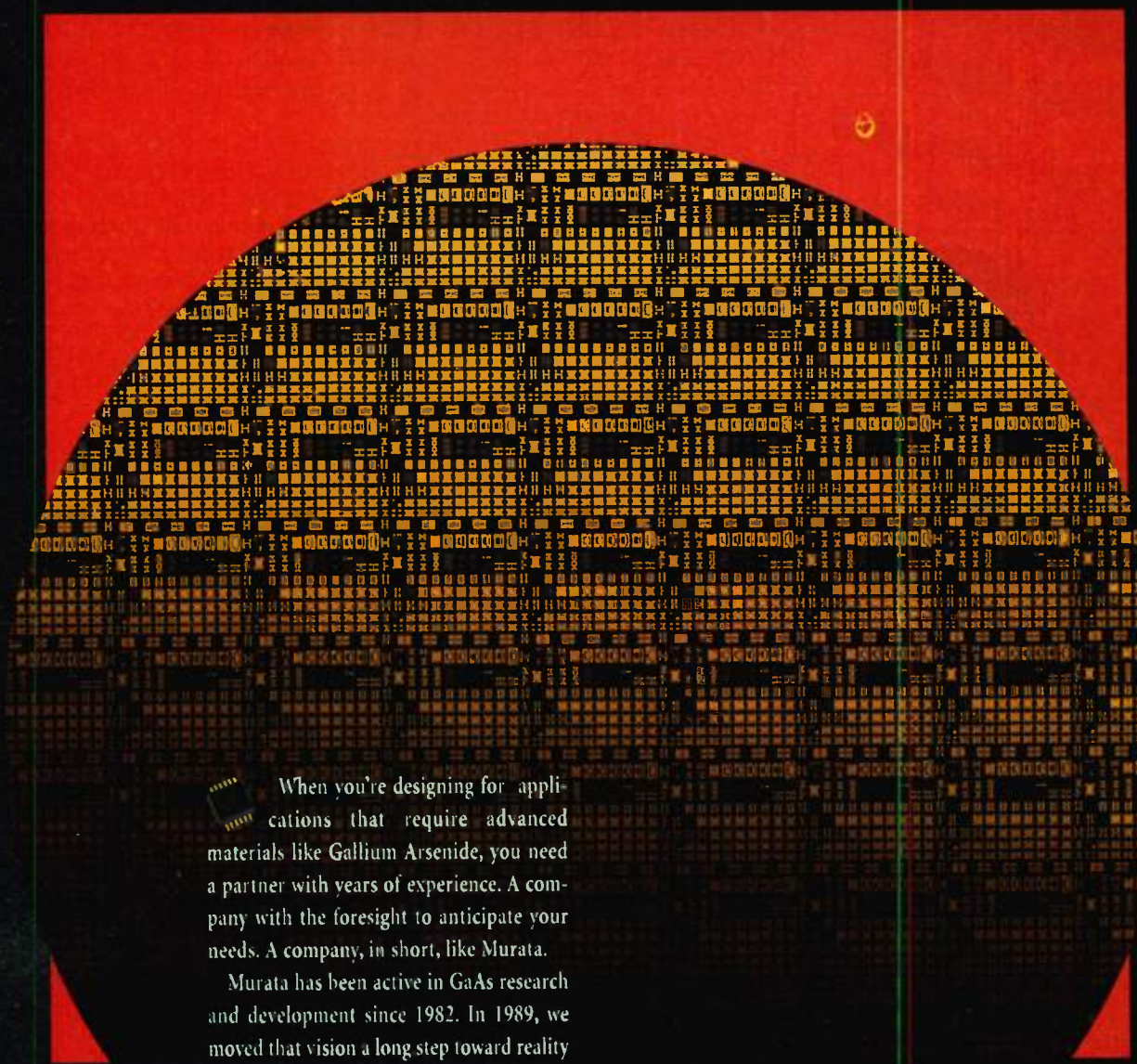
IEEE Aerospace Conference, March 21-28. Snowmass Confernce Center, Snowmass, Colorado. Contact Mike Johnson, 2225 Roscomare Road, Los Angeles, California 90077-2222; (310) 472-8019; e-mail: johnson@ee.ucla.edu.

Second Intellectual Property in Electronics Seminar (IP '98), March 23-24. Westin Hotel, Santa Clara, California. Contact John Whitaker, Miller Freeman Technical Ltd., +44 181-316-3297; e-mail: ed98@cityscape.co.uk.

PCB Design Conference West, March 23-27. Santa Clara Convention Center, Santa Clara, California. Contact Molly Knox, Miller Freeman, (408) 448-6173; e-mail: mknox@mfi.com.

INFOCOM '98, March 28-April 2. Hotel Nikko, San Francisco, California. Contact Ramesh Nagarajan, Lucent Technologies, 101 Crawford Corner Road, Room 3M-318, Holmdel, New Jersey 07933; (732) 949-2761; fax (732) 834-5906; e-mail: rameshn@lucent.com.

IEEE International Reliability Physics Symposium, March 30-April 2. Reno Hilton Hotel, Reno, Nevada. Contact Ann N. Campbell, M/S 1081, Sandia National Labs., Post Office Box 5800, Albuquerque, New Mexico 87185-1081; (505) 844-7452; fax (505) 844-2991; e-mail: ancampbe@sandia.gov.



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What's In Store For '98

As we begin the new year, I thought it would be an appropriate time to share with you the latest news on the many exciting new additions and changes coming your way in 1998.

Because *Electronic Design* is growing, we've both added and promoted staff to key positions in order to meet the challenge of consistently delivering to you more exclusive articles, features, reports, and supplements.

First, we've beefed up our commitment to covering analog technology by bringing on board one of the premier editors in the electronic magazine business. Many of you will instantly recognize the name of veteran writer/editor Ashok Bindra. For the last 15 years Bindra was Senior Technical Editor at *EE Times*. His experience and knowledge in covering analog and other emerging technologies gives our magazine the best one-two analog team in the business, as Bindra joins Frank Goodenough, our renowned, long-time Analog & Power Editor.

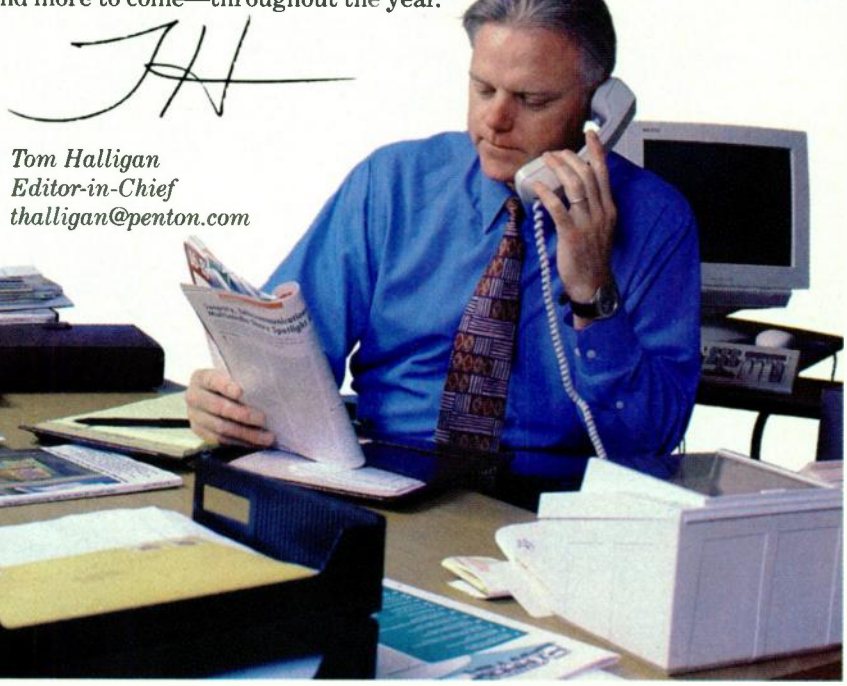
John Novellino, our Test & Measurement Editor for the past 10 years, has been promoted to Managing Editor in charge of Special Projects. Novellino's solid editing, writing, and managing background will afford us the opportunity to enhance and grow our current and planned supplements, and ancillary publications. Additionally, we've promoted Deb Schiff from Copy Editor to Chief Copy Editor, replacing Mike Sciannamea, who was promoted to Web Editor.

Sciannamea joins our newest team of editors and technical managers who are charged with relaunching our web site later this month. I'll be sure to let you in on their progress in my next editorial. The other members of our new web staff include: Donna Policastro, Web Manager; John Lynch, Web Designer; and Deb Bloom, Webmaster.

And, it doesn't end there. In the following month, we are relaunching a new and expanded *Electronic Design China*. Recognizing that design engineers in China need a single, all-encompassing technical source of information, our relaunch will allow for a quick expansion. It also will provide our China-based editorial team with greater editorial resources from our U.S.- and European-based editorial teams.

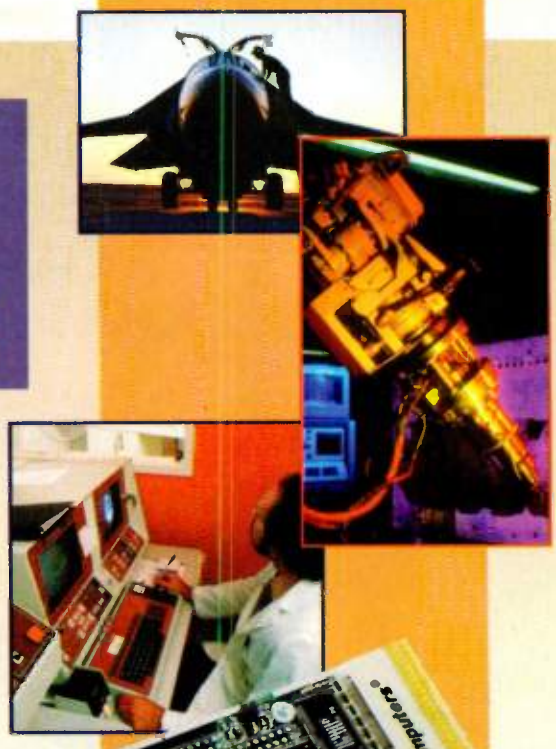
Finally, you will see more inclusive directories, and expanded sections launched throughout the year that will supplement our 26 issues per year.

Hope your '98 is as full and rich as ours! I'll keep you posted with periodic status reports on all of these new projects—and more to come—throughout the year.



Tom Halligan
Editor-in-Chief
thalligan@penton.com

Pentium Power in a 3U cPCI Processor.



PEP, the company that puts more industrial computing power into less space than any company in the world, has done it again with the remarkable new CP310. Everything about it is designed to maximize your industrial computing power, functionality and versatility. Here's how:

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Fear Of Commitment Stalls IC Progress

At the recent Surface Mount International conference in September, Bruce Freyman, vice president of Laminate Products at Amkor/Anam, Chandler, Ariz., headed a well-rounded discussion of the various market and technical issues facing IC designers and packagers today. It was during the Q&A period that followed, however, that the true state of the market was defined. And it isn't good—at least as far as the designer is concerned. Key among the attendees' concerns were the general confusion caused by the the variety of IC packaging options available, the lack of technical information on their reliability, and the lack of a basic infrastructure to support any given IC package.

The confusion surrounding the many packages available is perfectly understandable, considering the alphabet soup of acronyms now proffered by most packaging houses to describe their product line. From dual in-line packaging (DIP) to very-small outline packaging (VSOP), and the hundred or so in between, sorting through the pros and cons of the ever-growing and changing list has become somewhat of a specialty in itself, and has kept many a designer and analyst alike up at night.

That the list is changing so fast is a clear indication of the rapid rate of development in this area, development spurred on by consumer demand for more features at a lower cost, in a smaller space, and with lower power consumption and less weight. With the cry for greater portability, the latter three rise to the top of the list and are the key driving forces behind many of today's custom developments. Thanks to these forces, many houses are researching and developing chip-scale packages (CSPs) and ball-grid arrays (BGAs) with up to 1000 I/Os, with pad pitches down to 60 μm.

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Developing such packages is all well and good, but density without reliability is not good. While many houses expound upon their capabilities and successes with respect to reliability, none seem willing to share their failures. The result of intense competition, this dearth of information has slowed product development as each packaging house repeats the failures and mistakes of their peers due a lack of shared knowledge. Fortunately, attempts at addressing this problem have been made. JPL, Pasadena, Calif., has its BGA testing program where various packages are tested, under neutral conditions, and reliability figures generated. In addition, the Chip Scale Packaging Task Force, based out of Molndal, Sweden, is well into its charter of examining the issue of reliability of CSPs, PGBAs, thin-quad flat packs (TQFPs), and thin small-outline packages (TSOPs), both in the context of overall assembly, as well as board-level reliability.

Until the results of the basic research become known, many designers are reluctant to commit to any specific offering, especially considering how secretive many packaging houses are about their technology roadmap. This issue leads to the third attendee concern, and something of a Catch-22 situation. Until designers/customers commit to a given package, the infrastructure necessary to bring that package to market at a reasonable cost will not arise. But with costs still so high, and reliability so uncertain, designers are unwilling to make that commitment. Clear and irrefutable facts concerning reliability are going to be necessary before designers migrate en masse toward a particular package.

To help with this situation, the "Mobile System Packaging Concerns" session at *Electronic Design/Microwaves & RF's* upcoming Portable by Design/Wireless Symposium conference, to be held at the Santa Clara Convention Center, Santa Clara, Calif., Feb. 10-12, will be adding a number of IC packaging topics to its regular lineup of thermal- and mechanical-related papers. For *Electronic Design's* part, the June 8 issue's PIPS Packaging focus will be featuring a special Packaging and Interconnections supplement to expand upon the issues and technologies only briefly mentioned here. If you feel that you or your company could add to the discussion, please feel free to contact me at *pmannion@penton.com*.

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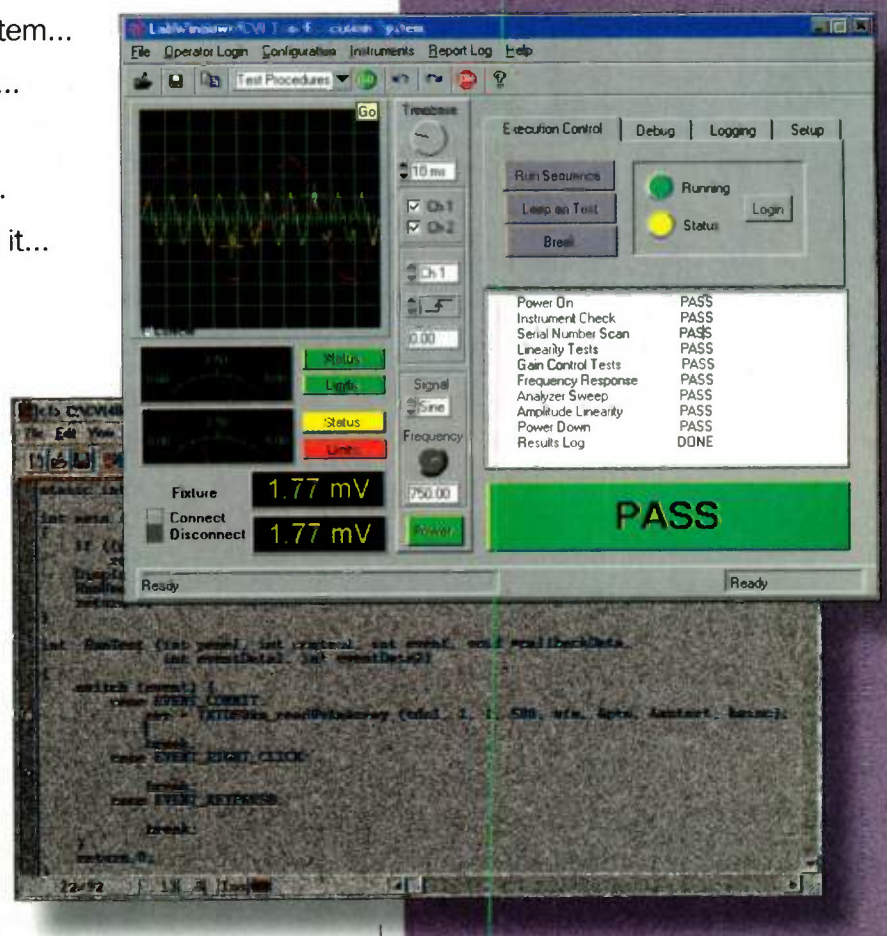

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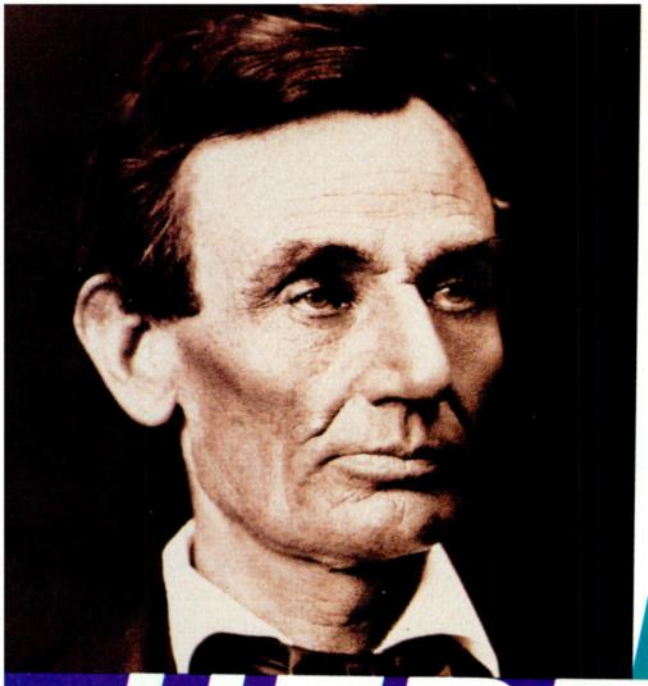

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Linking Design, Process, ATE Standards Will Boost IC Yields

As the bipolar process finally gives way to CMOS commonality in terms of design rules, architecture and fabrication processes will become easier to implement. The result will be an environment favorable to the development of a single design, monitor, and test network, according to James T. Healy, president and CEO of Genus Corp., a manufacturer of semiconductor fab equipment. With manufacturers of design tools, process diagnostic equipment, and automated test equipment working together, a path to the "known-perfect-device" will be imaginable, said Healy in his keynote address at the International Test Conference in Washington D.C.

Healy's credentials include stints with Fairchild Semiconductor Corp. and GenRad Semiconductor Test Inc. He was a cofounder and president of Trillium Corp. (which was later absorbed into LTX Corp.), and before joining Genus was president and CEO of Credence Systems.

Because of the differences in the tools employed, the semiconductor manufacturing environment is unstable and often thought of as chaotic, said Healy. Unlike other mature industries where factories are optimized for efficiency and yield, semiconductor manufacturing has taken a back seat to design and process, so cycle times are weeks rather than days.

What's needed, says Healy, are open architectures and common interfaces potentially driven by proprietary software. Coupled with effective planning and scheduling, this standardization would generate vast improvements in productivity and yield. But improved productivity through yield management goes beyond ATE. It must also involve design and process diagnostic tools. Simulation outputs must be able to be used to drive tester hardware. "To do this effectively may require a fundamental change in tester architecture," he said. "Additionally, certainly in the short term, a coalition between DFT, process diagnostics, and ATE is required." JN

Joint Effort To Develop Flash-Array-Embedding Technology

A newly formed technology partnership will work to create a flash technology for embedding flash arrays with standard CMOS logic and commodity memories. Tower Semiconductor, San Jose, Calif., and Saifun Semiconductor, Migdal Haemek, Israel, will focus on developing a nonvolatile memory technology based on Saifun's proprietary flash-memory concept.

So far, the two organizations have successfully passed the feasibility tests of what they believe to be the smallest flash cell in the industry. Once qualified for production, the technology is expected to enable the implementation of ultra-high-density flash-memory arrays as large as 128 Mbits using a 0.5-μm CMOS process.

Tower will have an exclusive license for semiconductor contract manufacturing using the flash technology. It's currently investigating other potential joint development efforts for the purpose of delivering products based on this new flash technology. For additional information, contact Tower Semiconductor at (408) 551-6500. CA

Metal-System Advances Simplify Copper, Aluminum Deposition

To ease the volume production of copper-based metallization systems for ICs, an integrated process sequence that first deposits a tantalum or tantalum-nitride film (a barrier layer) and then a thin "seed" layer of copper, can be performed using physical vapor deposition. The integrated process sequence can be done on a single ion-metal plasma system thanks to process development done by Applied Materials Inc., Santa Clara, Calif. The resulting layers provide excellent step coverage due to the conformal nature of the film deposition technique.

The tantalum or tantalum-nitride films are both thin and have a low resistivity: less than 500 Å thick and less than 250 mW-cm. The films have low internal stresses and can conformally coat the entire interconnect via hole or trench structure. In addition, tantalum-based films provide good barrier properties and effectively guard against copper's tendency to diffuse into silicon or silicon dioxide. By keeping the wafer under an ultra-high vacuum between the barrier and seed-layer deposition steps, the tantalum film has no chance to oxidize, ensuring it will maintain its low resistivity and provide good adhesion to the copper seed layer. The seed layer provides an atomically-smooth and cohesive copper interface that encourages the correct grain growth during the subsequent bulk copper fill step. The copper seed layer has a resistivity of less than 1.9 mW-cm.

In a second development, Applied has created a warm-aluminum process capability that employs an aluminum low-pressure seed source. Such an aluminum deposition technology allows the use of physical vapor deposition to fill via holes with widths as small as 0.25 mm and aspect ratios as high as 4:1 at process temperatures of less than 430°C. The low process temperature will minimize any effect the late-stage processing has on previously processed layers on the chip, which is critical as more and more layers of aluminum are employed on the chip surface.

To achieve the via-hole filling, the company employs a Vectra Ion Metal Plasma chamber to deposit a thin diffusion barrier layer of titanium or titanium nitride in the via hole. Then the system moves the wafer to an aluminum low-pressure seed chamber to deposit—while using a low temperature—a thin "seed" layer of aluminum. A "warm aluminum" step completes the process by filling the via holes with bulk aluminum, thus planarizing the structure. That seed layer is critical to the

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Now, it would have been nice to have each of the MIPS partners say a few words about their individual strengths. But frankly, each partner has their own virtues and just way too many strong points to mention in one ad. (That, and the fact that they couldn't agree on who would go first.) So to simplify matters, just remember this: each partner is turning out incredible versions of this open, scalable architecture.

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processing, because it determines the effectiveness of the subsequent bulk fill.

The enhanced technology in the low-pressure seed chamber provides a highly-directional deposition that results in a 2.5-fold improvement in bottom coverage versus previous aluminum approaches. The new chamber design increases the distance between the aluminum target and the substrate, thus giving the sputtered atoms a more vertical trajectory when they hit the wafer. Floating shields are used in place of conventional grounded shields to increase the concentration of ions at the center of the plasma, permitting the chamber to sustain the plasma at much lower pressures (0.35 mTorr). For further details, surf into Applied's web site at: *http://www.appliedmaterials.com.* DB

Safer, More Reliable Weapons Targeted By New Partnership

In an effort to assure increased weapons safety and reliability, Sandia National Laboratory, Albuquerque, N.M., has partnered with the Ensign-Bickford Company (EBCo), Simsbury, Conn. It's been claimed as one of the largest contracts ever awarded by Sandia's Manufacturing Development Engineering (MDE) program—the two-year effort is backed by $10 million in funding.

This partnership expands on earlier cooperative work between the two organizations and will focus on enhancing the safety and reliability of explosive components used in national defense weapons systems, as well as in civilian applications. Once all is said and done, expectations are that a number of different components and other explosive systems will be developed to replace the aging components now in the U.S. nuclear weapon stockpile.

The undertaking will utilize several technologies either developed or refined by the two organizations. One technology is the semiconductor bridge (SCB), a low-energy igniter developed and patented by Sandia in 1987. It has proven particularly useful for civilian and national defense applications through its demonstrated ability to ignite explosives in an extremely fast (several microseconds), precisely timed, and safe manner.

For further details, call the Media Relations Department of Sandia National Laboratory at (505) 844-8066, or check out its web site at *http://www.sandia.gov.* CA

Co-Design Group Looks To Close Gap Between System, HW/SW

Co-design is considered by many to be one of the keys to successful system-level integration. Unfortunately, the technology that makes co-design a workable concept is still in its infancy. Recognizing this discrepancy, Mentor Graphics, Wilsonville, Ore., has partnered with a number of research facilities to accelerate the development of new technology for system-level co-design. Joined together in the research initiative referred to as the Co-Design Consortium, members will work toward bridging the gap between system-level and hardware/ software design flows. This will be done by gathering requirements directly from advanced users, funding specific university research and prototype development based on industry-leading tools, and incorporating the results rapidly into commercial design-automation products.

Research members include Princeton University, which is exploring architectural co-synthesis for distributed embedded systems; Stanford University, currently working on system level behavioral design; the University of Washington, focusing on work in co-design space and exploration and interface synthesis; and Germany's University of Tubingen, which is investigating methodology for rapid analysis and optimization of embedded systems. Mentor Graphics contribution to the consortium stems from its work in behavioral architectural exploration and hardware/software co-verification at the system level for complex systems. All research efforts will be leveraged to develop a complete environment for large-scale, high-level design of electronic systems with hardware and software components. Mentor's web site is *http://www.mentorg.com.* CA

Consumer Microelectronics Design Center Opens

A design center for the development of consumer microelectronics recently began operations, thanks to a partnership formed between SGS-Thomson Microelectronics, Paris, France, and Daewoo, Seoul, Republic of Korea. The design center is located at Daewoo's Seoul facility and is equally owned and operated by both companies.

When fully operational, the center will house a staff of 60 design engineers. They will be involved with developing ICs for existing consumer-electronics applications and future products for digital and high-definition TV (HDTV), digital VCR and DVD, telecommunications, computing, and other products agreed upon by the two companies.

For SGS-Thomson, the center will provide important feedback on customer needs, which will serve as a guide in the development of ICs specifically tuned to particular applications. Daewoo, on the other hand, gains advanced IC design expertise crucial to the future development of state-of-the-art analog and digital consumer products. Both companies hope that the center will serve as an example of how key consumer-electronic products will be developed in the 21st century. Contact JP Rossomme of SGS-Thomson Microelectronics at +781-259-2534. CA

Edited by Roger Engelke

32-BIT 486 µP FOR EMBEDDED APPLI-CATIONS.

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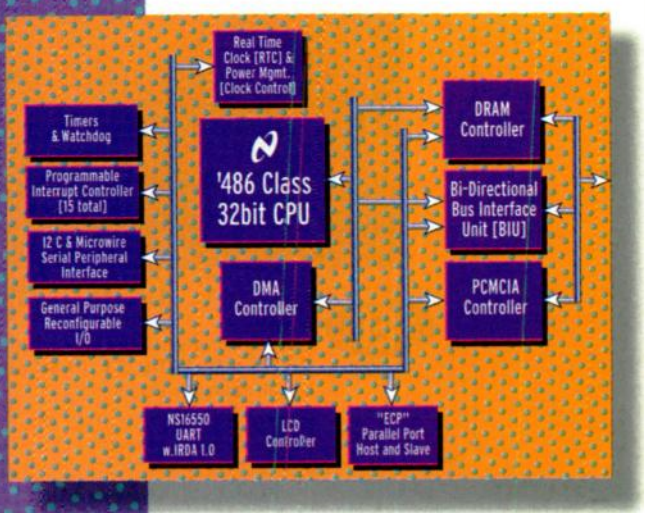

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Embebbed Systems Conference Spring, Mar. 31-Apr. 2. Navy Pier Festival Hall, Chicago, IL. Contact Liz Austin, Miller Freeman Inc., (888) 239-5563; (415) 538-3848; esc@mfi.com.

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20th IEEE International Conference on Software Engineering, Apr. 19-25. Kyoto International. Conference Hall, Kyoto, Japan. Contact Koji Torii, Graduate School of Information Sciences, Nara Institute of Science & Technology, 8916-5 Takayama-cho, Ikoma-shi, Nara-ken 630-01, Japan; +81 7437-2-5310; fax +81 7437-2-5319; e-mail: torii@is.aist-nara.ac.jp.

DSP Spring Design Conference, Apr. 21-23. Santa Clara Convention Center, Santa Clara, California. Contact Liz Austin, Miller Freeman Inc. (888) 239-5563, (415) 538-3848; e-mail: dspworld@mfi.com; Internet: http://www.dspworld.com.

Southeastcon '98, Apr. 24-26. Hyatt Regency, Orlando International Airport, Orlando, FL. Contact Parveen Ward, ECE Dept., University of Central Florida, Orlando, FL 32816; (407) 823-2610; fax (407) 823-5835; e-mail: pfw@ece.engr.ucf.edu.

16th IEEE VLSI Test Symposium, Apr. 26-30. Hyatt Regency Monterey, Monterey, CA. Contact Rob Roy, Intel Corp., MS:JFT-102, 5300 Elam Young Pkwy., Hillsboro, OR 97124-6497; (503) 264-3738; fax (503) 264-9359; e-mail: robroy@ichips.intel.com.

IPC Printed Circuits Expo '98, Apr. 26-30. Long Beach Convention Center, Long Beach, CA. Contact Dan Green, The Institute for Interconnection & Packaging Electronic Circuits, 2215 Sanders Rd., Northbrook, IL 60062-6135; (847) 509-9700 ext. 371; fax (847) 509-9798.

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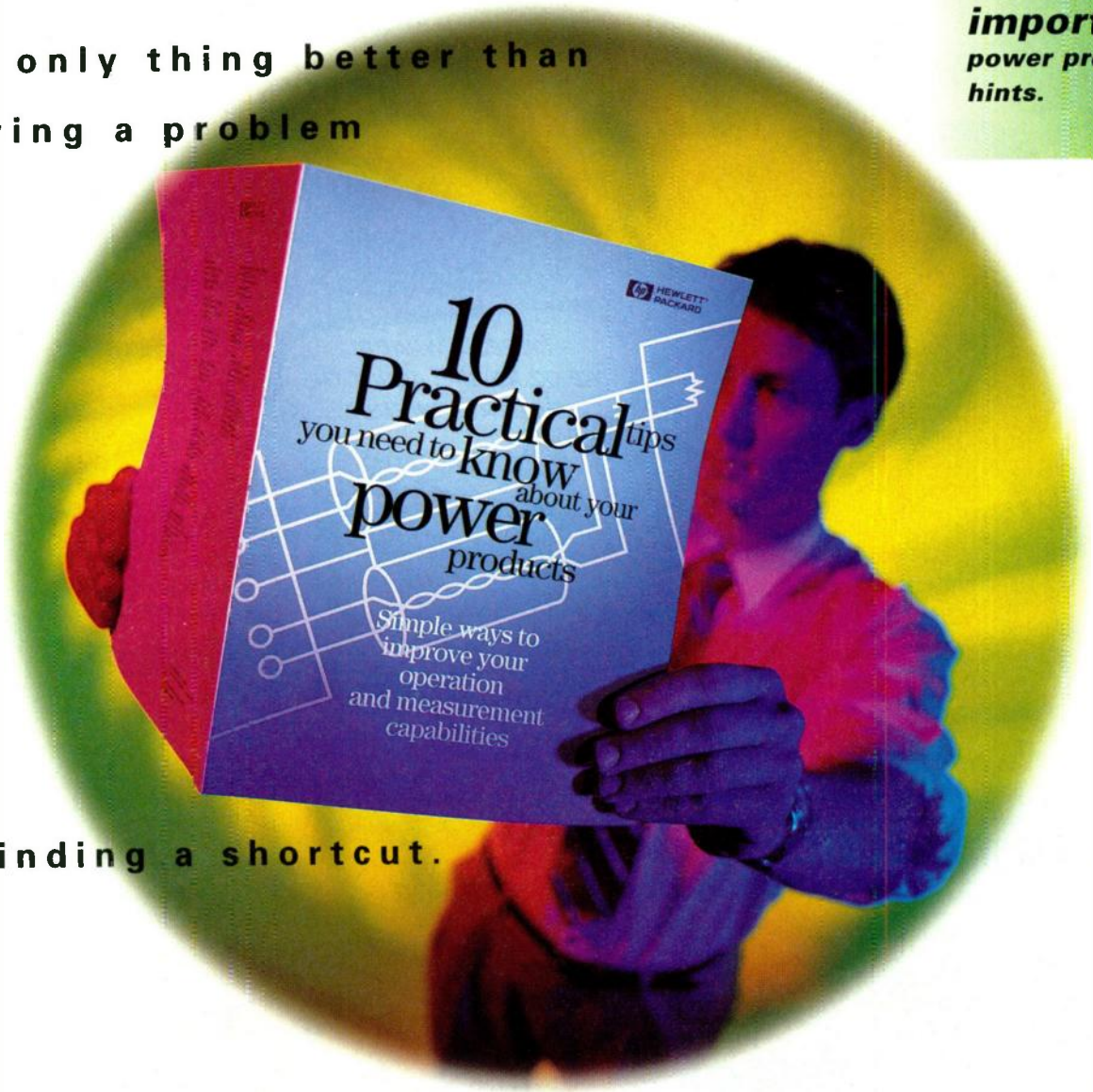

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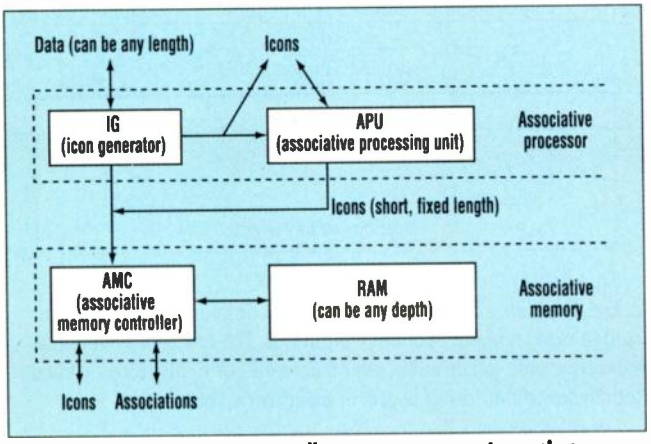
Associative Processing Architectures Promise To Accelerate Communications Switching And Other Pattern-Based Applications

Thanks to a new class of computing architecture, computing and communications products may be able to deliver order-of-magnitude increases in performance and evade the technical bottlenecks that are beginning to dog the industry. Rather than simply using a general-purpose computer or an ASIC that processes each byte sequentially, the new associative architecture allows groups of data within a large array to be identified and operated upon simultaneously. These associative recognition and manipulation operations are based on proprietary number theory discoveries, occur in singular events, and process large blocks of data in singular events, rather than a long sequence of instructions.



1. An associative processor rapidly creates compact icons that contain the important characteristics of the data stream. These are used by the associative processing unit and the associative memory controller to identify multiple data elements that contain characteristics that are needed for a pattern match.

Developed by Neo-Core, a technology development corporation located in Colorado Springs, Colo., this technology could find applications wherever pattern-intensive processes are employed. These include fast table lookups, complex filtering functions, and pattern recognition. According to Chris Brandlin, Neo-Core's chief technology officer, such architectures could find their way into a variety of communications products by accelerating switching and routing decisions, data-scrubbing functions, and database indexing and searching by orders of magnitude. Medical and industrial imaging devices, as well as artificial vision systems, could economically implement fast, accurate image and pattern recognition functions using associative technology.

This associative processing technique is becoming increasingly important as the speed and complexity of the tasks we perform grows with each passing year. For example, as gigabit connections become commonplace, the short pole in the tent is no longer the capacity of the bit pipes, but the speed of the switches, routers, filters, and other elements that direct and massage the data during its travels. Until now, fast CPUs and ASICs have been employed for these tasks. As bandwidth demands increased, clock speeds were cranked up and data path widths grew from 16, to 32, to 64 bits, and even wider. Clearly, clock speed and bus width cannot be expanded forever and an alternative solution must be developed.

A computer typically searches for information using a series of sequential processes. Information is stored in memory and queried one memory location at a time. In associative processing, the computer puts up a data object, and if it is recognized by the associative memory, an association is returned in response. In other words, data objects (keys) are recognized, not merely found. Current solutions include using content-addressable memories and distributed processor architectures to speed up sequential operations, but they don't always provide an ideal answer. Neo-Core contends that their associative processing technique can be faster and more cost-effective.

A simple example of associative processing would be to give 100 slips of paper to 100 people. Five of these slips have an X on them and are distributed secretly and randomly. Now, find out who has the five Xs. If you approach this problem like a computer, you would ask each person, one at a time, to show you a slip. By the time you find all five Xs, you will have polled all or nearly all 100 people.

Neo-Core's Brandlin says that there is a better way. Just yell, "Everybody with an X raise your hand!" Five hands shoot up, and you have your answer. This is association, and computers typically do this sort of operation badly.

Data in the real world makes the process of association difficult. First, data objects are rarely randomly distributed, and the pathology of most databases creates difficult challenges for system designers. Also, many data objects (or keys) are large in their natural form. In typical computer systems, these keys are boiled down to small data items to make them more manageable. The industry is trying to develop ways to deal with unorthodox data types that don't lend themselves to being represented as words or keys.

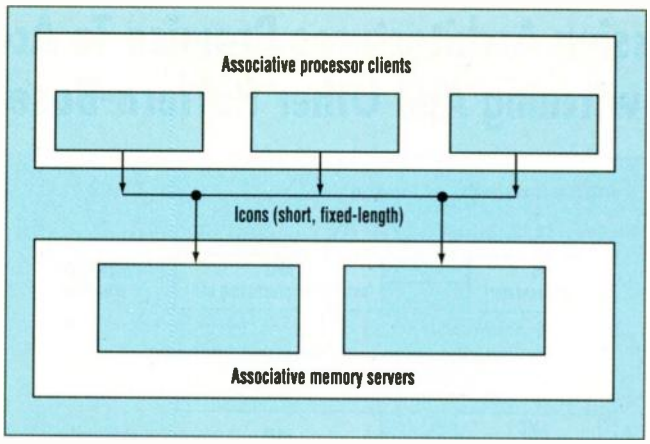
The first step in associative processing is to produce information icons from data. An icon generator (IG) must deal with data streams of any length and configuration. The resulting icons are relatively small, fixed-length codes (or symbols) containing the logical properties of the original data. Because information icons are small (often a single computer word), they can be processed more efficiently than data. Icons also can be built and used incrementally, allowing data streams to be analyzed (with intermediate icon values) on the fly. This is ideal for applications where data locations are unclear.

Data input often needs to be massaged to achieve the desired results. An icon that represents data can be manipulated, just like the data itself, for the same results and with far less processing. These manipulations are executed by the associative processing unit (APU). Neo-Core's associative processing system has a variety of logical icon manipulations. These include:

- Concatenation of icons
- Removal of information from icons

(from the beginning or end)
• Replacement of information in icons (any part, anywhere)
• Combination of icons (either full or partial)

The associative processing system is divided into an associative processor and an associative memory *(Fig. 1)*. In the prototype system, the associative processor is contained in a single IC. It accounts for only a small percentage of the hardware, but it does most of the work. It is responsible for iconization of data and logical manipulation functions. The associative memory generally consists of an ASIC and RAM modules. One associative memory can be shared by several associative processors. The associative memory only needs icons to operate. The original data (because it has been processed by the associative processor) is not needed.



2. In a distributed application, multiple associative processors can be used to feed multiple associative memories. The connections between the components can be either over a network, or tightly coupled via a backplane, printed-circuit board, or an intra-chip bus.

In a client/server system where associative processors are in the client machines and the associative memory is in the server, network traffic is substantially reduced. Work is distributed between computers, relieving server processor load. When long data blocks need to be iconized in a multi-processor computer (in pattern-recognition systems, for example), multiple associative processors can be tightly coupled to a single associative memory *(Fig. 2)*.

Looking at the diagram of the basic associative processor system (APS), it becomes clear that icons can be retrieved and restored by the host, allowing iconization to be accomplished separately from other associative processes *(Fig. 2, again)*.

The icon generator and associative processing unit generally reside in a single ASIC. The associative memory controller is implemented in an ASIC as well. The amount of RAM needed is governed by icon size and the number and size of associations (which can be data, a pointer, or an implied pointer requiring no storage for association data at all). The length of data objects to be associated has no bearing on the amount of RAM needed. In the case where long data blocks need to be iconized in a multi-processor computer (pattern-recognition systems, for example), multiple associative processors can be tightly coupled to a single associative memory.

One of the first applications for multiple associative processors may be for breaking open network-routing bottlenecks. Today, routers employ fast processors that must read the address in a packet header and sequentially search through its routing tables to find out what to do with the packet. In theory, packet forwarding for an Internet protocol router could be boosted from a top speed of 250,000 packets/s for sequential list matching functions to 30 million packets/s for an associative-processor-based router.

According to a noted communications technology analyst, networking companies are relatively conservative about the core technologies they use in their products. This may delay the rollout of associative processors in the network arena, but Brandlin and company expect to produce the same results in other areas such as artificial vision systems for automated vehicles. Surprisingly, however, some of the first commercial applications for this new technology may be scanning on the fly high-speed data streams for viruses.

Robert Moore, Neo-Core's networking specialist, has defined a vertical virus-scan application that can be implemented in an antiviral network-interface card (V-NIC). Using a first-generation associative processor, the card can perform a real-time scan for known virus signatures on live data streams running at Sonet OC-3 (155 Mbits/s) speeds. Moore anticipates that future generations of hardware will be capable of recognizing and disabling viruses in 622-Mbit/s or Gigabit Ethernet lines.

Since this technology has such a wide variety of applications, Neo-Core will license it to firms who can make the best use of it within a given market. They expect that the bulk of their alliances will involve board-level licensing for vertical applications, although they will consider licensing of a Verilog-core for exceptional situations where a fully optimized solution is required for maximum performance.

For more information on associative processing technologies, their applications, and licensing opportunities, contact Neo-Core, 2864 South Circle Drive, Suite 1200, Colorado Springs, CO 80906; telephone (719) 576-9780, fax (719) 576-0790; Internet: http://www. neocom.com.

Lee Goldberg

Chemical Sensor Enables Real-Time pH Distribution Measurement

Chemical sensors are garnering a lot of attention. By their nature, they have the potential to measure characteristics on a molecular and atomic level. They also hold the promise of uncovering information that could be of significant importance in medicine and microbiology. Though the chemical sensor field is still in its infancy, there's much ongoing research in academic and industry circles.

One such research effort is taking place at Hamamatsu, Kyoto, Japan, on a charge-coupled device-based pH imaging sensor with a linear output response. The device offers the ability to observe, in real-time, the transition of a

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Device	Gates	Logic Elements	Embedded RAM	Performance Improvement -2 Speed Grade (1)	Performance Improvement -1 Speed Grade (2)	Supply Voltage
EPF10K30A	30,000	1,728	12 Kbits	40%	123%	3.3 V
EPF10K50V	50,000	2,880	20 Kbits	40%	110%	3.3 V
EPF10K100A	100,000	4,992	24 Kbits	35%	107%	3.3 V

1. Estimated performance with -2 speed grade using MAX+PLUS II v. 8.1 compared with -3 speed grade using MAX+PLUS II v. 8.0.
2. Estimated performance with -1 speed grade using MAX+PLUS II v. 8.2 compared with -3 speed grade using MAX+PLUS II v. 8.0.

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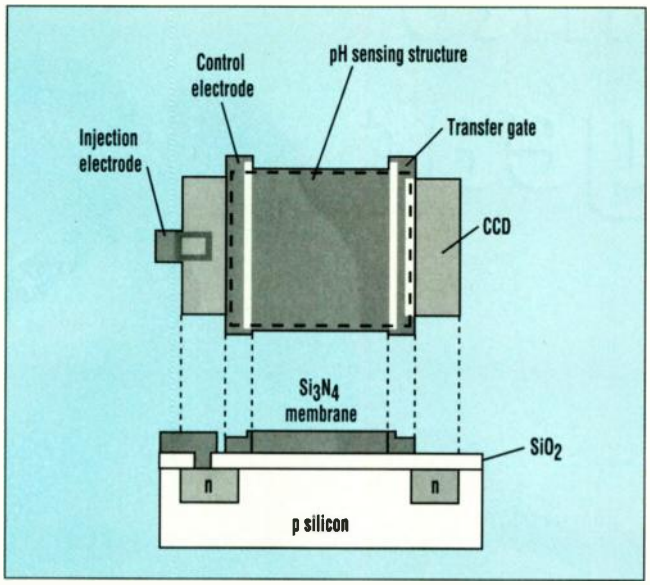
distribution of the pH in a solution. Researchers believe that this capability will allow them to finally unlock much of the unknown phenomenon, such as the atomic and molecular characteristics, of different solids, and observe the metabolic activity of microorganisms. Such devices have been proposed previously, but until now they had failed to observe a real-time pH distribution.

Compared with other proposed pH imaging sensors, Hamamatsu's device offers both a high resolution of less than 10 µm, and a speed that's higher than today's TV rate. Each pixel of Hamamatsu's proposed device is composed of a number of component pieces, including a control and injection electrode, a pH sensing structure made from silicon-nitride/silicon-dioxide/silicon ($Si_3N_4/SiO_2/Si$), a CCD, an input diode, and a transfer gate *(see the figure)*. A film made of Si_3N_4 acts as the pixel's membrane. A potential well, formed in the silicon substrate under the sensing structure, changes according to the density of hydrogen ions in a solution, and equates to the value of the pH. With the pixel's transfer gate turned off, the potential well is determined by the value of pH in a solution.



This schematic diagram illustrates the composition of one pixel in Hamamatsu's CCD pH imaging sensor.

When in operation, a potential difference between the pixel's control electrode and sensing structure creates a charge packet. When the input diode is pulsed, the potential well floods with charge and, as a result, overflows. The charge corresponding to the pH value at the sensing structure remains in the charge packet. When the transfer gate is turned on, the charge transfers to the charge-coupled device (CCD). This charge, along with all the other charges from each pixel in the image sensor, can then be read out using conventional CCD techniques.

To date, a test device, comprising eight pixels and a four-phase CCD has been fabricated. The sensing part of the device measures 100 by 100 µm. When tested, the device exhibited a linear output signal with a sensitivity of 45 mV/pH, and an operating frequency of 2 kHz.

Researchers are continuing to work on this CCD pH imaging sensor device, focusing their efforts on reducing its pH-sensitive area. Using refined fabrication equipment, the researchers believe they can reduce it from 100 by 100 µm to less than 5 by 5 µm.

For more information, contact Hamamatsu at (81) 53-478-1324; fax (81) 53-478-1348.

Cheryl Ajluni

Space Shuttle Ultra-Low-Temperature, Zero-Gravity Experiment Is Designed To Shed Light On The Future Of Electronics Miniaturization

What happens to a material when it is confined to ultra-low temperatures in zero gravity? The answer may come from an experiment known as the confined helium experiment (CHeX) conducted by researchers at Stanford University, Stanford, Calif. The experiment was scheduled to be launched on the space shuttle Columbia this past November. Its purpose is to determine what happens to a material when it is confined to such narrow dimensions that it begins to behave as if it has only two dimensions, rather than three. Stanford University physicist John Lipa, who's been exploring the esoteric nature of liquid helium for 20 years, is the principal investigator on the experiment. His work could have important ramifications for microelectronics miniaturization. Project co-investigators are Ulf Israelsson, Talso Chui, and Frank Gasparini at Caltech's Jet Propulsion Laboratory (JPL), Pasadena, Calif.

In most materials, this confinement effect surfaces at extremely small dimensions—thicknesses of a few atomic widths. It arises from the fact that fundamental particles have a dual nature, acting sometimes like solid objects, and other times like a packet of waves. A particle contained within a layer, one that is so thin that the waves associated with it come in contact with both edges, is restricted to moving in only two dimensions. This constraint can change the physical properties of the material. In the case of an electron, electrical properties of the material are affected.

Given that transistor line widths in today's ICs are about 0.2 µm and plans are to reduce this by a factor of 10 or more in the next decade, that is about the size where it is expected these confinement effects will appear in metals and semiconductors. Preliminary indications are that this effect tends to have a depressing effect on properties like electrical conductivity. According to the researchers, this could have serious consequences for the microelectronics industry. A large confinement effect could slow or block further size reductions, forcing the industry to develop a new technology to reach smaller-size scales.

Scientists have several competing theories for how the confinement effect might work, but there is little direct evidence of its exact nature and magnitude. That is where helium comes in. It has some unique qualities that make it an ideal substance in

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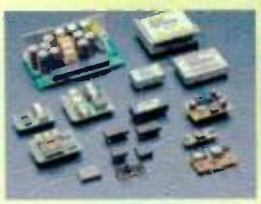

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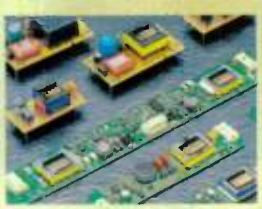

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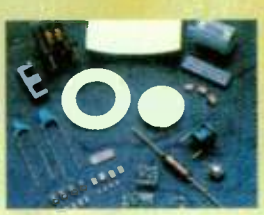

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which to observe this effect.

Helium is the only substance that remains a liquid at absolute zero, a temperature of 273°C below zero. At a temperature of about 2°C above absolute zero, it becomes a superfluid, a material without resistance to current flow.

As it is cooled to the point where it turns from an ordinary liquid into a superfluid, its confinement effect increases by a factor of 10,000 or more. As the effect increases, the distance at which helium atoms sense boundaries increases from a few atomic widths to thousands of atomic widths. This makes it possible to measure the confinement effect cleanly and directly with current technology.

Lipa and his colleagues designed an experiment that consists of more than 400 silicon wafers. The thin wafers, which are two inches in diameter, are stacked together in a column. The surface of each wafer contains a micromachined recess with a depth of 50 µm. When the column is immersed in about two cubic inches of chilled helium, the liquid forms thin layers between the wafers.

Confinement is expected to affect a number of a material's physical properties. The CHeX experiment is designed to measure its impact on helium's heat capacity. To make these measurements, the scientists have developed some of the world's most precise thermometers. They can measure temperature changes in liquid helium of less than a billionth of a degree. As a result, they can record changes in energy as small as a fly's landing on a table.

The thermometers and much of the other hardware originally were developed for an experiment that flew on the shuttle in 1992. Called the Lambda Point Experiment, the original investigation determined the way in which bulk-helium's heat capacity changes as the material makes the transition from normal to superfluid state. As they cool the confined helium to the superfluid transition point, the researchers expect its heat capacity to diverge from that of the three-dimensional helium. The direction and magnitude of that divergence will provide them with a direct measurement of the strength and nature of the confinement effect. The experiment must be done in zero gravity. On Earth, the variations in pressure caused by gravity are enough to obscure the divergence.

There are three leading theories that attempt to predict the confinement effect: the renormalization group theory by Volker Dohm of the University of Aachen in Germany; a Monte Carlo-based theory by Efstratios Manousakis at the University of Florida; and a vortex ring dynamics theory by Gary Williams at the University of California at Los Angeles. Each makes slightly different predictions for the size of the effect and how it varies in different materials. The results of the CHeX experiment should help refine these theories.

For more information, contact Professor John Lipa at (650) 723-4562; e-mail: jlipa@leland.stanford.edu.

Roger Allan

1998 TECHNOLOGY FORECAST

Exploring the ramifications of intellectual property issues for electronic designers

Intellectual property (IP), a term that is familiar to most book, magazine, and other types of publishers, has now invaded electronics technology. It is presently one of the hottest issues facing designers of present and future ICs, subsystems, and systems. The issue is taking on greater urgency as the need to greatly reduce system design times increases, caused by increasing pressures for a faster time-to-market. With predefined circuit blocks now available for engineers to design their chips and circuits, and the certainty that such blocks will become even bigger "systems-on-a-chip," a host of legal and technical issues have arisen that must be addressed. We're already seeing the formation of organizations like the Virtual Socket Interface Alliance (VSIA), whose goal is to make "system-on-a-chip" design a practical reality by the mixing and matching of "virtual components." However, the proliferation of such "super chips" also has brought with it two seemingly irreconcilable issues: the need for the security of IP black-box models, and the designer's need to know about what's going on inside these black boxes.

To shed light on IP's future, Electronic Design has decided to examine IP in all of its aspects for electronics technology and attempt to "forecast" its future. To do that, it has invited the opinions of leading industry figures, as well as those of its staff editors. The following articles try to answer IP questions such as when does a design idea, be it in hardware, software or both, become IP? How do you leverage IP for the most efficient design? What EDA tools are needed to meet future IP demands? How do you best test IP cores and "systems-on-a-chip?" In short, just where is IP heading and what are its ramifications for both the designer and the manufacturer?

One thing is becoming increasingly clear: continued progress in electronics technology may very well hinge on how well we address key IP issues of concern. These include a movement away from a culture of "silicon craftsmanship" to one of "system-on-a-chip" thinking; a greater acceptance of increased "re-use" of IP design cores and blocks; and a move away from concurrent logic and physical design to concurrent system and chip design. Such demands are sure to pose a tremendous challenge to electronic designers and silicon IC manufacturers.

Gazing At The New Age Of Intellectual Property

The IP Revolution Will Change The Way Engineers Do Their Work, Along With Significant Shifts In Corporate Business Models.

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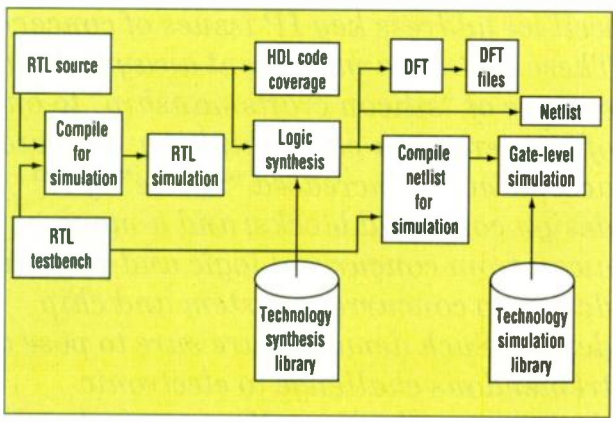
Wilsonville, OR 97070-7777;
(503) 685-7000.

PIERRE OUELLETTE
Author of high-technology science-fiction books.

This particular summer, the third in the new millennium, is unusually hot in Akmola, the relocated capital of Kazakhstan, a former republic of the Soviet Union. A 25-year-old man sits at his old Pentium-fueled desktop computer and stops to wipe the sweat off his brow before continuing to type another line of HDL. He is oblivious to the sweltering heat in his tiny apartment, and focuses intently on the content of the code on the screen, where he is making the final changes to comply with the Virtual Library that will ultimately represent his work.

The young man is brilliant, as was his father, a nuclear physicist at the closed nuclear city of Arzamas-16, before the diaspora of the Russian scientific community. As the young man looks through an open window at the rows of old apartments across the street, he recalls the genesis of his current intellectual property (IP) project. A year ago, he was browsing the latest research papers on a stunning breakthrough in the generation and modulation of neutrinos, ephemeral subatomic particles that slice effortlessly through nearly all forms of matter. At last, a technology existed that would allow point-to-point communication directly through the mass of the Earth, obviating the need for satellites.

The big stumbling block in this nascent technology was that the system required encoding conventional digital data into a neutrino stream, and then decoding it at the receiving end. The necessary functionality was extremely dense and convoluted, and required several pc boards full of deep submicron (DSM) devices.



1. During the design cycle, intellectual property flows through a complex set of tools and processes on its way to working silicon.

But after studying the problem for several months, the young man devised an ingenious solution that cut the hardware requirements down to a few hundred thousand gates—small enough to be used routinely as an IP block in the latest generation of DSM designs.

Now the young man has completed coding his solution in HDL, and is ready to enter it into the global market for IC-based intellectual property.

In San Jose, a product manager employed by a vertical semiconductor company is desperately searching for a solution to her latest crisis. Lately, there has been an R&D stampede to develop handheld communication devices that take advantage of the new neutrino technology. Obviously, the first company to market with volume shipments of such products will reap incredible profits. But, the catch is size and power consumption. All current solutions are board-level products consuming nearly 20 W.

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parameters consistent with the system architecture? Are there adequate synthesis scripts available? Is the design fully testable in a manufacturing environment?

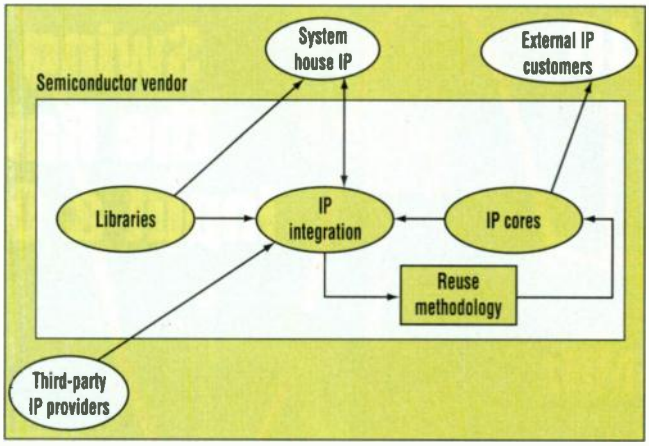
The challenge of IP compatibility fundamentally begins with interface issues on the chip. The advent of deep submicron is producing vast arrays of silicon capable of embracing an amazing diversity of subsystems. Soon, a single chip will contain multiple CPUs, each with its own cluster of functional blocks, much like states within a system-level federation. While this enormous functional capacity offers exciting creative opportunities to designers, it also produces many interesting interconnect problems.

One given is that each basic CPU type will have a unique bus structure, and any modification in the immediate neighborhood of the CPU will have serious performance consequences. At the same time, it is not practically possible to design a piece of IP to simultaneously accommodate all these native buses. The problem is compounded by signal propagation issues, such as transmission line effects and parasitic capacitance, which play a very large role in system performance at the submicron level.

While the interface issue may be complex, it is most certainly solvable. A combination of new standards and technologies hold the key. On the standards front, a set of formal data format definitions, both logical and physical, will eventually arise to automatically mediate between buyers and sellers of intellectual property. The work on the Virtual Socket Interface (VSI) is a precursor to this type of standard.

On the technology side, a new class of electronic design automation (EDA) tools will emerge that will be devoted to automatically building the interface between functional blocks on the new generations of super chips. These tools will resolve logical, physical, and protocol parameters to create and optimize subsystem interfaces. This new EDA technology will require place-and-route tools that can assess and accommodate the physical configurations of transistors and metal layers and their impact on interconnect performance in terms of signal propagation. It also will require tools that resolve logical problems, such as the specific configurations of address, data, and control lines.

Finally, this new technology will require that these tools deal with the software-based protocol issues governing the high-level conversations between subsystems.



3. Large-scale silicon vendors will employ reuse methodologies that enhance the value of their intellectual property, and form external links to the IP market as a whole.

The IP market must also be viewed from the perspective of tools and flows. Any given piece of IP may find its way into a great variety of design flows, each with its own particular configuration of tools. One of the principle challenges in the evolution of the IP market will be to construct commonly understood methodologies that govern the way IP flows through the design cycle. The basic elements in a generic design flow demonstrates some of the many issues involved in integrating a piece of soft-core IP into a design *(Fig. 1)*.

The content and structure of the RTL is the first consideration. The code should be partitioned in a way that accommodates logic synthesis, and facilitates clock management. The code should be simple in its overall structure, with well-structured subunits that use registers on the inputs and outputs to simplify timing issues. Clocking schemes should be synchronous and avoid the gating of clock signals. Other issues include naming conventions and consistent port ordering.

The RTL code needs to be accompanied by an RTL test bench demonstrated to exercise all the code in the file. (Eventually, the code also will have to be exercised within the context of the target system.) Command files also must be provided that govern both the compilation and simulation of the RTL code. A complete synthesis script defining both commands and constraints during the synthesis process also is required. Once a gate-level netlist has been produced, command files must be available to manage Design-For-Test (DFT) procedures such as test insertion and automatic test-pattern generation. Finally, the netlist needs to be run through logic simulation and static-timing analysis to guarantee its performance and functionality before final release.

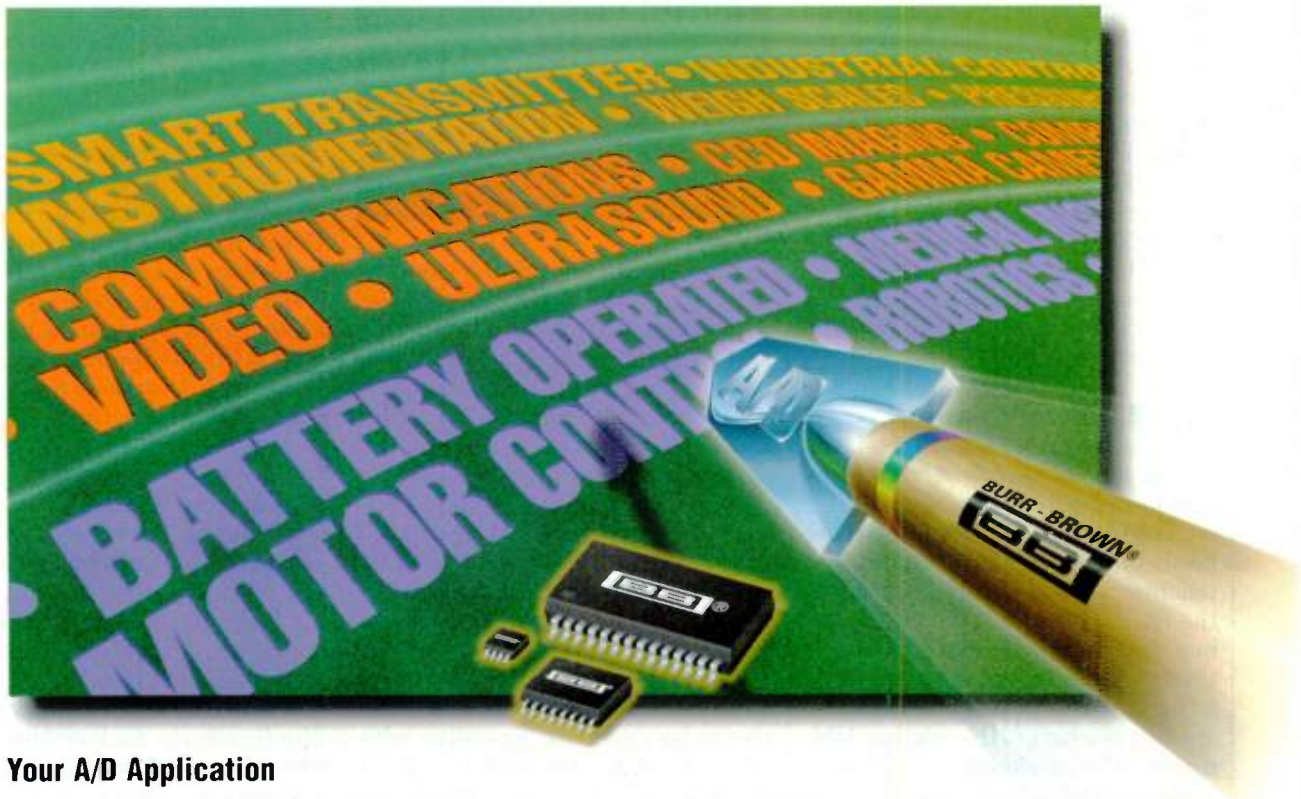
Obviously, this combination of tools and flow also represents a complex challenge for IP providers and buyers. Typically, a piece of soft-core IP will be developed in one design environment and then marketed for use in many others. For the IP market to flourish, there needs to be some common understanding that transcends these differences and creates a bridge from IP creators to IP consumers.

The Silicon API

One proven vehicle for constructing this bridge comes from the software world in the form of an application programming interface (API). The difference here is that the ultimate target of the API would be functional silicon instead of executable object code. For this reason, the interface can be termed the Silicon API. Contained within this interface would be a detailed, yet generic, design methodology that considers every procedure and tool in the design cycle and how they interrelate. This methodology would then become a superstructure used to delineate specific tools and procedures, and their interrelationships. Consequently, it would help define the specific nature of the Silicon API.

The Silicon API, once established, would allow IP designers to develop their circuitry with a very specific set of deliverables in mind, including all of the requirements previously men-

Target Your A/D Application



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Product	INL (% FSR)	Input Range	Resolution (Bits at 10Hz)	Resolution (Bits at 1kHz)	Power Dissipation (mW)	Price (1kpcs)	FAX*LINE* # 1-800-548-6133	Reader Service #
ADS1210	±0.0015	±312mV to ±5V	24	20	26	$9.60	11284	80
ADS1212	±0.0015	±312mV to ±5V	22	16	1.4	$7.25	11360	81
ADS1214	±0.0015	±20mV to ±320mV	22	16	1.4	$7.25	11368	82

HIGH-SPEED A/D CONVERTERS **preliminary information*

Product	Resolution (Bits)	Speed (MHz)	Power (mW)	SNR (dB)	DNL (LSB)	SFDR (dBFS)	Supply (V)	Price (1kpcs)	FAX*LINE* # 1-800-548-6133	Reader Service #
ADS800	12	40	390	64	±0.6	61	+5	$29.00	11286	83
ADS803	12	5	116	69	±0.3	82	+5	$9.55	11398	84
ADS824*	10	75	315	59	±0.5	70	+5	$8.50	11403	85
ADS930/931	8	30	66/63	46/48	±0.4	51/49	+3/+5	$3.37/$3.27	11349	86

GENERAL PURPOSE A/D CONVERTERS **no missing code*

Product	Resolution (Bits)	INL (LSB)	DNL* (Bit)	Sample Rate (kHz)	Power (mW)	SINAD (dB)	THD (dB)	Price (1kpcs)	FAX*LINE* # 1-800-548-6133	Reader Service #
ADS7813	16	±2.0	16	40	35	87	–90	$20.00	11302	87
ADS7817	12	±1	12	200	2.3	71	–83	$5.18	11369	88
ADS7822	12	±0.75	12	75	0.54	71	–82	$4.64	11358	89
ADS7825	16	±2.0	16	40	50	86	–90	$28.46	11304	90

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tioned, and many more—all defined by the interface itself. On the far side of the Silicon API, buyers would know precisely what to expect as deliverables, and could anticipate in advance any specific adjustments that would have to be made for the specific tools and flows.

Is it reasonable to imagine a future with a universal Silicon API that brings order and predictability to the IP marketplace? Who would create and maintain such an interface? Who would extend it to cover new tools and methodologies? Who would ensure that it remains aligned with emerging industry standards, such as the Virtual Socket Interface?

New Business Models

The answers to these questions beg the larger question of future business models in the brave new world of intellectual property. Obviously, there needs to be some kind of mechanism that brings order and predictability to the IP market so that all parties will benefit. Past experience indicates that while industry standards play an important role in this process, they are only one part of the solution. Ultimately, the marketplace will come into play and help define what services and products are required to streamline the deployment of intellectual property.

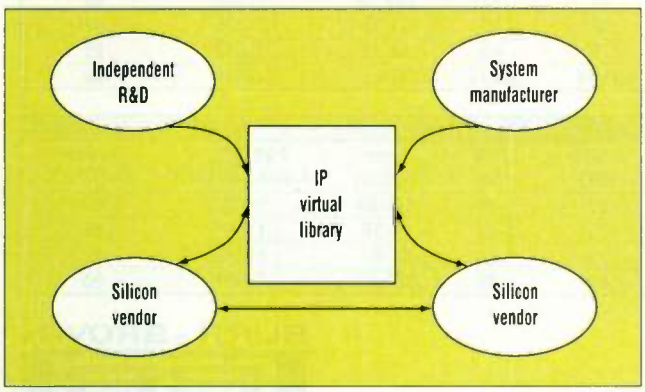
To build a workable scenario for how these products and services might evolve, let's first consider a future model for the high-level flow of IP within the industry. In the accompanying figure, the term "silicon vendor" is used to cover the entire range of ASIC technologies *(Fig. 2)*.

A more exotic approach might involve "embedded alarms" in the code, which would be set off...

The other blocks are the independent IP providers (our young man in Akmola, or R&D facilities), and the system manufacturers, who are gradually moving to super-chip solutions, with entire systems being implemented on single piece of silicon. In this model, everyone does business with everyone else. First and foremost, there will be a heavy exchange of IP among silicon vendors, reflecting a trend already in place through numerous cross-licensing agreements.

There also will be IP transactions between independent IP providers and systems houses that seek their particular expertise, as well as with silicon vendors, who seek to expand their internal IP libraries. However, these transactions are "unqualified" in the sense that there is no guarantee of plug-and-play compatibility as the IP moves from one design environment to another. Further exchanges will occur between silicon vendors and systems houses seeking to externally market certain IP solutions they have created.

Since the heaviest exchanges are now between silicon vendors, it is worth exploring their internal processes in relation to IP, and determining how they fit into the larger flow just described. Shown are the basic elements in ASIC development processes *(Fig. 3)*. Internal libraries of functional primitives are used by in-house designers and external customers, who assemble and integrate this material into higher-order intellectual property that forms the primary value in IC products. In addition, third-party IP providers also may contribute to this process.



4. A Virtual Library that qualifies, certifies, and supports intellectual property will bring order to a potentially chaotic market. This will optimize IP market flow.

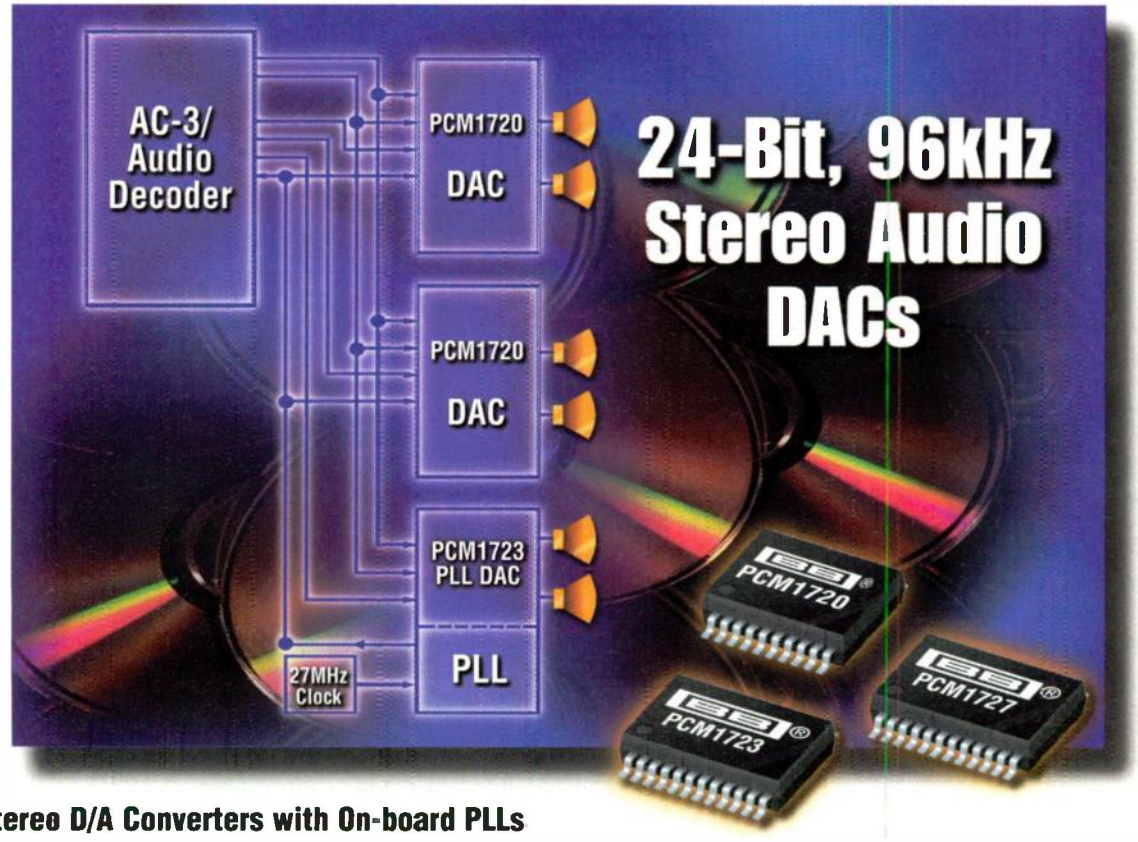
The challenge for silicon vendors is to develop and sustain an internal reuse methodology that is generally consistent with the industry as a whole. Once this is accomplished, three benefits result. First, the IP is optimized for internal reuse. Second, the IP now has market value that allows it to be easily sold externally. Third, this uniform reuse methodology can act as a filter to qualify incoming intellectual property from external sources.

Now the question becomes: Can all these exchange paths exist without some form of filtering bringing true "play-and-play" capability to the use of intellectual property? The answer is probably not. There needs to be some kind of entity that acts as an intermediary to ensure that the trade in intellectual property can transcend the barriers of tools, flows, and methodologies.

For the sake of illustration, let's call this source a Virtual Library *(Fig. 4)*. The figure shows how the market flows shown in Figure 2 would be rearranged to allow for a Virtual Library able to certify that IP from any source meets the necessary criteria for "plug and play" in target designs. In fact, this IP qualification/certification source would not need to be a single organization. Multiple organizations could provide the Virtual Library function, as long as they anchored their service around a common methodology. At present, EDA vendors are among the likely candidates to evolve into this kind of endeavor because of their long exposure to tools, flows, and IP library development.

The engineering manager at the semiconductor company now activates a hyperlink embedded in the data sheet for the neutrino modulator. It takes her to a Virtual Library that has chosen to represent the young man's product and ensure that it meets all the criteria required by the semiconductor company's design methodology. Fortunately, the young man anticipated this part of the marketing process and prepared his intellectual property in accordance the

DVD/MPEG-2 Solutions



New Stereo D/A Converters with On-board PLLs

Burr-Brown's new line of stereo audio D/A converters with single or dual PLLs simplifies DVD and MPEG-2 system clock design, as well as reduces external components and board space.

These D/A converters are complete with 8X oversampling digital interpolation filters. The digital filters include selectable features such as soft mute, digital attenuation, and digitial de-emphasis. The DACs employ 3rd order delta-sigma modulators, and can accept 16-, 20-, 24-bit input data in either normal or I^2S formats.

PCM1723 features an on-board phase-locked loop (PLL) which generates a 256/384fs digital audio system clock from a standard 27MHz MPEG-2 video clock. Priced from $3.95 in 1000s.

PCM1727 contains an on-board dual PLL to derive a variety of audio clocks needed for DVD. PLL-1 derives a fixed 33.8688MHz (768fs, fs=44.1kHz) system clock. PLL-2 derives both the 384fs (fs=44.1k/48kHz) system clock and the 768fs system clock, all from an external 27MHz reference frequency. Priced from $4.95 in 1000s.

Products	Description	Bits	Dynamic Range	SNR	THD+N	Maximum Sample Rate	Supply Voltage	Package	FAX*LINE*# (800) 548-6133	Reader Service #
PCM1717/18	DAC	16/18	96dB	100dB	–90dB	48kHz	+2.7 to +5V	20-Pin SSOP	11289/11325	290
PCM1719	DAC	16/18	96dB	100dB	–88dB	48kHz	+5V	28-Pin SSOP	11343	291
PCM1720	DAC	16/20/24	96dB	100dB	–90dB	96kHz	+5V	20-Pin SSOP	11333	292
PCM1723	DAC	16/20/24	94dB	96dB	–88dB	96kHz	+5V	24-Pin SSOP	11344	293
PCM1727	DAC	16/20/24	92dB	94dB	–88dB	96kHz	+5V	24-Pin SSOP	11407	294
PCM1725	DAC	16	95dB	97dB	–84dB	96kHz	+5V	14-Pin SOIC	11373	295
PCM1800	A/D	20	95dB	95dB	–88dB	48kHz	+5V	24-Pin SSOP	11387	296
PCM3000	CODEC	18	96dB	98dB	–90dB	48kHz	+5V	28-Pin SSOP	11342	297

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Virtual Library's Silicon API, thereby vastly streamlining the process of qualifying it for sale. The manager is delighted to find that the young man's IP conforms to the same Silicon API that her company is using internally to harvest its own IP. As a result, the neutrino modulator will be exceptionally easy to integrate into her design environment and quickly available.

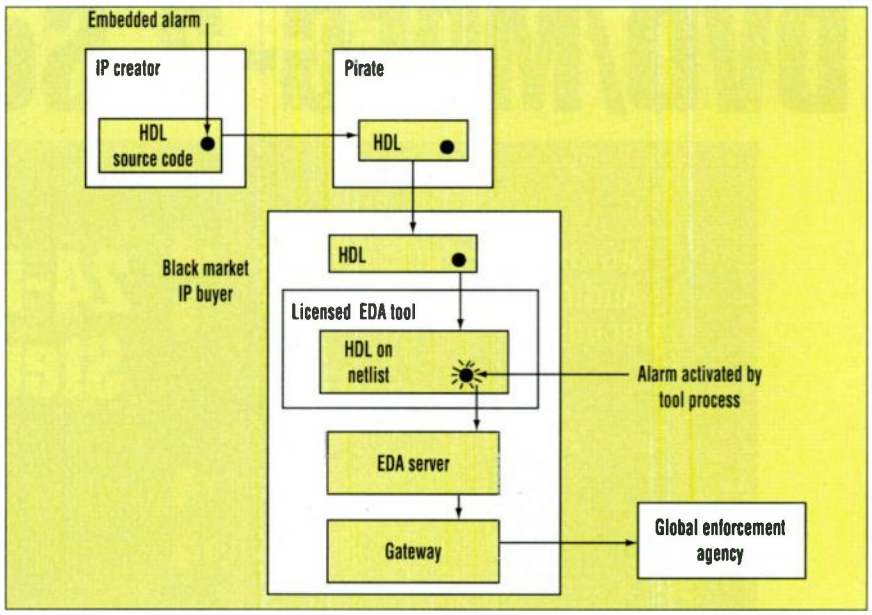
The Virtual Library contacts the young man via e-mail and informs him of the pending transaction with the semiconductor company. He is elated, in spite of the heat. By the time winter swoops down upon the area, the temperature will plummet to forty degrees below zero, and the apartment will become an icebox. But he will no longer live here. He will live in one of the new developments in the suburbs. He decides to go out and celebrate in the bar of the hotel in the main square, where the presidential palace and the ministerial complexes are located. The bright lights. The laughing patrons. The hard currency. He can't wait. Before he leaves, he goes to check his e-mail one last time.

He is horrified by what he reads.

In a recent article in the *Harvard Business Review*, economist Lester Thurow wrote extensively on the future of intellectual property in the Information Age and its impact on patent and copyright laws. One of his key points centered on the futility of such laws when they are unenforceable, arguing that laws that can't be enforced are not really laws at all. In the case of IC-based intellectual property, the barriers to effective enforcement are considerable.

Once an HDL-based soft core winds its way through synthesis, netlist, and physical layout, it becomes a microcosm of nearly inscrutable geometries embedded with millions of others on a piece of silicon only a few centimeters square. How do you spot pirated work? How do you trace it back to its source? In short, how do you prevent IP laundering, in the same vain as money laundering?

Currently, there are no simple answers to these important questions. But clearly, the future of IP is critically dependent on the development of copyright enforcement technology capable of spotting what human perception might never notice. One possible solution is the inclusion of some kind of "digital watermark" in the code, similar to the techniques now used to protect and identify digital imagery on the Internet.



5. One form of protection for intellectual property is the inclusion of "embedded alarms" that are set off by IP's interaction with various EDA tools.

Another would be some type of universal registry where all IP is recorded and assigned a unique identification code. A more exotic approach might involve "embedded alarms" in the code, which would be set off when it was run through various EDA tools in the design cycle. Once the alarm was triggered, the tools would report it to a local network monitor, which in turn could notify the owner of the IP, an appropriate enforcement agency, or both *(Fig. 5)*. In any case, the long-term future for the IC-based intellectual property market will be no better than the technology devised to enforce the basic rights of ownership.

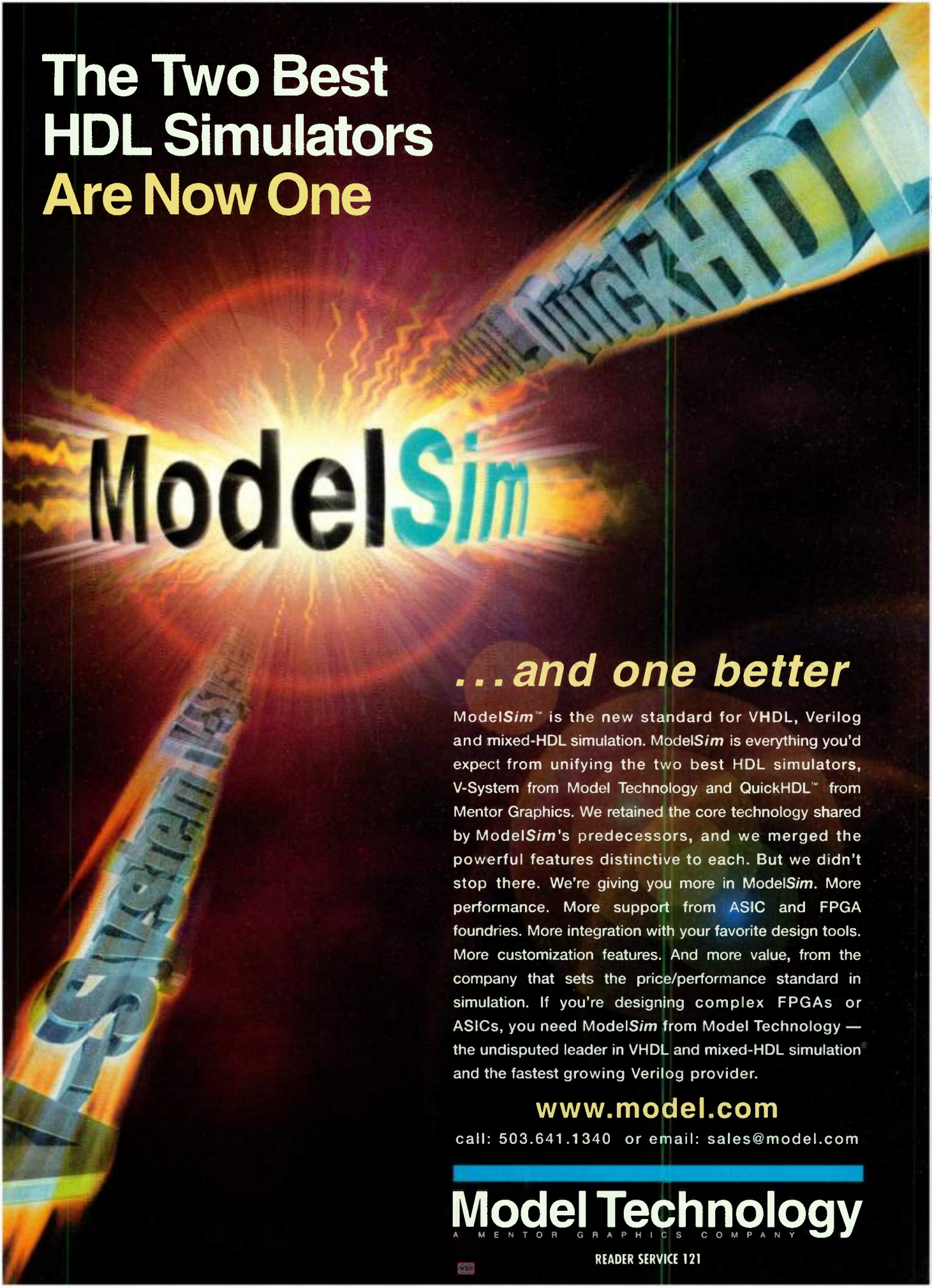
The young man can't believe it. He has e-mail notifying him that the embedded trigger in his code set off an alarm that has been uploaded to the Virtual Library firm that represents his neutrino modulator. It seems that somehow someone has pirated a copy of his source and attempted to run it on an HDL simulator, automatically passing the alarm along through predetermined channels. The culprit is a small, rogue firm in New Guinea with dubious credentials and ownership. But, even as the young man sinks despondently onto his lumpy old couch, a second e-mail arrives from the Virtual Library. Local authorities have agreed to raid the facilities of the offending firm, and seize the stolen code as evidence.

The young man sighs in relief. Life is good after all. On to the bright lights, the laughing patrons, the hard currency.

Walden Rhines is president and chief executive officer of Mentor Graphics. He holds a Bachelor of Science degree in Metallurgical Engineering from the University of Michigan, a Master of Science and a PhD in Materials Science and Engineering from Stanford University, and a Master's of Business Administration from Southern Methodist University.

Pierre Ouellette is a published author of two science-fiction novels, "The Deus Machine," and "The Third Pandemic." He is currently working on this third novel. He holds a Bachelor of Science degree in geography from Portland State University.

How Valuable	Circle
Highly	557
Moderately	558
Slightly	559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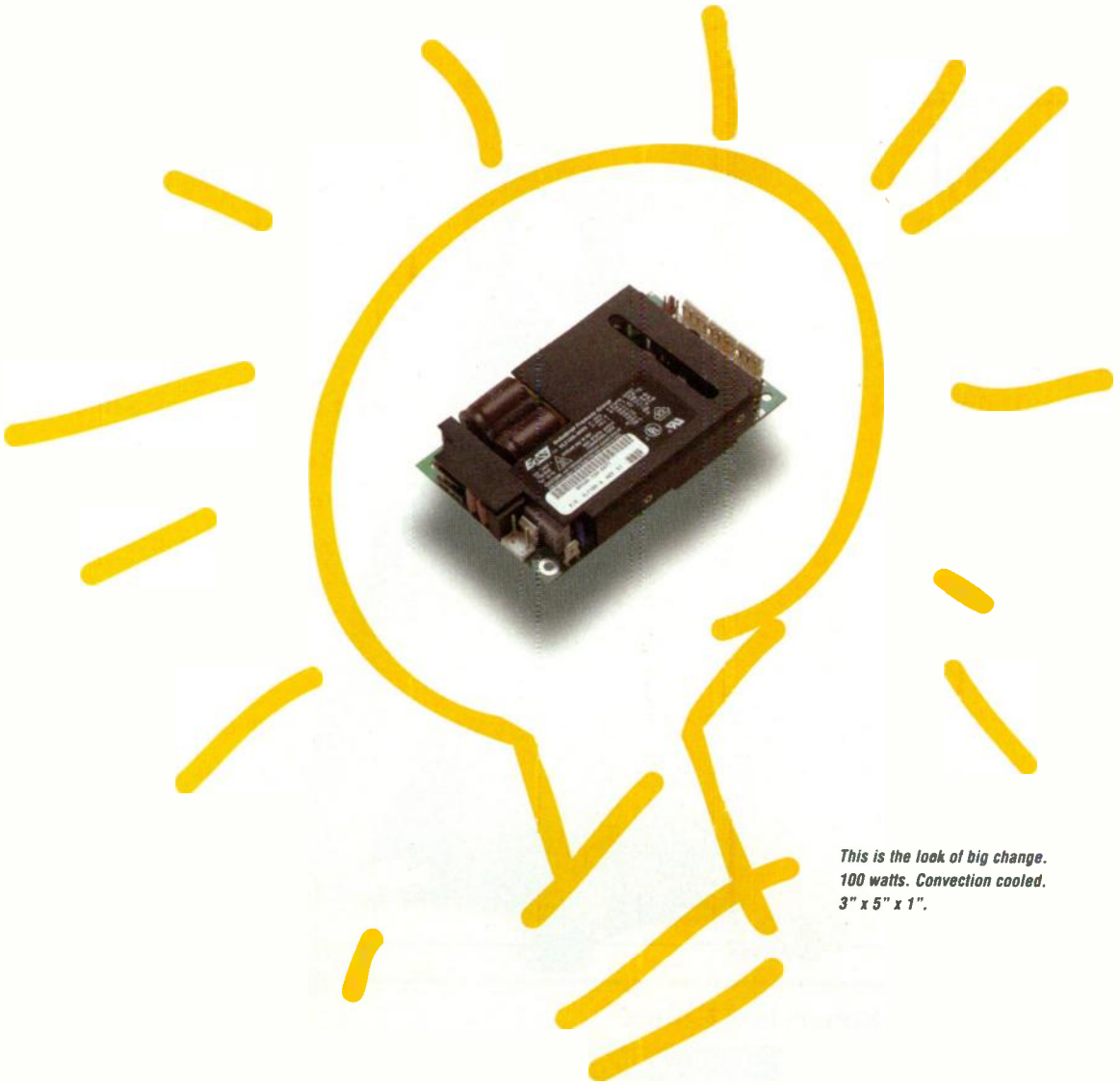

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Device	Reset Threshold	Active Low Reset	Active High Reset	Manual Reset	Watchdog	Secondary Sense Voltage	Package
DS1232LP	5V - 5% or 10%	✓	✓	✓	✓		8-pin DIP 8-pin SOIC
DS1705/6 DS1706x	5V - 5% or 10% 3.3V - 5%, 10% or 20%	✓ or	✓	✓	✓	✓	8-pin DIP 8-pin SOIC
DS1707/8 DS1708x	5V - 5% or 10% 3.3V - 5%, 10% or 20%	✓	✓	✓		✓	8-pin DIP 8-pin SOIC
DS1810-13 DS1815-18	5V - 5%, 10% or 15% 3.3V - 10% or 20%	✓ or	✓	✓*			SOT-23 TO-92
DS1832	3.3V - 10% or 20%	✓	✓	✓	✓		8-pin DIP 8-pin SOIC
DS1834	5V - 5% or 10% and 3.3V - 5%, 10% or 20%	✓ &	✓	✓			8-pin DIP 8-pin SOIC

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IP Fuels A Transformation Of Culture, Companies, And Cooperation

System And Chip Design Will Take Place Concurrently, And Today's Silicon Designers Will Become Tomorrow's System Integrators.

STEVE GLASER
Cadence Design Systems,
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If you don't believe that things must change, just stop and think about what design will be like 10 years from now. Approximately 0.07-µm process technology will yield over 200 million transistors of capacity. Communications, multimedia, and embedded computing subsystems will be operating together on chip, and include analog, digital, hardware, and a lot of software. Consumer markets will force multiple designs to be pipelined, with first architectures and associated designs to be developed in under nine months, with derivatives in under two months.

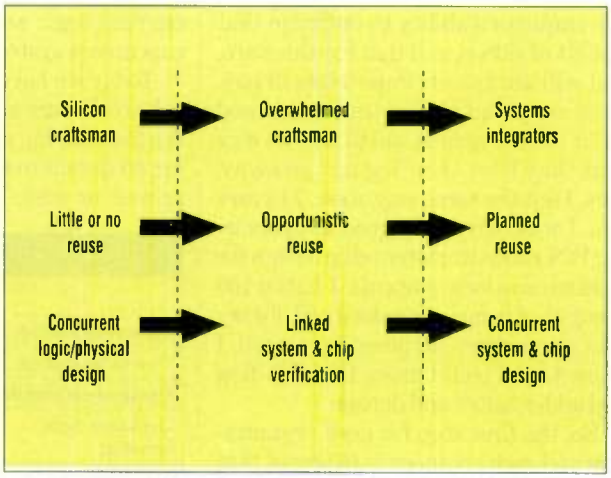
As a result, companies will be forced to specialize. They will focus on the things they do best, and partner with other companies for the components or services needed to bring the whole solution to market in a competitive time frame. Clearly, no one company will be able to do it all. Some companies will provide excellent branding and distribution value, some architecture and application software expertise, while others will provide only state-of-the-art virtual hardware or firmware components. Still others will provide advanced process technology with high-value, highly coupled processor cores.

In the 80s and 90s, we saw the PC industry go through a similar evolution. It moved from the (mostly) vertically-integrated IBM and Apple, to channel specialists like Dell combined with Microsoft for the OS. Adobe handled applications, application-specific signal processor (ASSP) vendors such as Chips and Technologies handled chip sets, and service specialists such as SCI were called for PC board assembly. As the complexity of the problem grew and the industry matured, standards such as PCI and common hardware reference platforms emerged to facilitate the industry growth and the growth of focused specialists. In 10 years, we will certainly see similar standards move into the chip domain, such as those developed by the Virtual Socket Interface (VSI) Alliance, and de facto integration-platform standards (e.g., on chip buses) tailored for high-volume, mature, system-chip applications. In the most mature markets, these standards will even facilitate the equivalent of today's low-tech, low-cost overseas systems and pc board integrators, who will simply be plugging virtual components into virtual sockets.

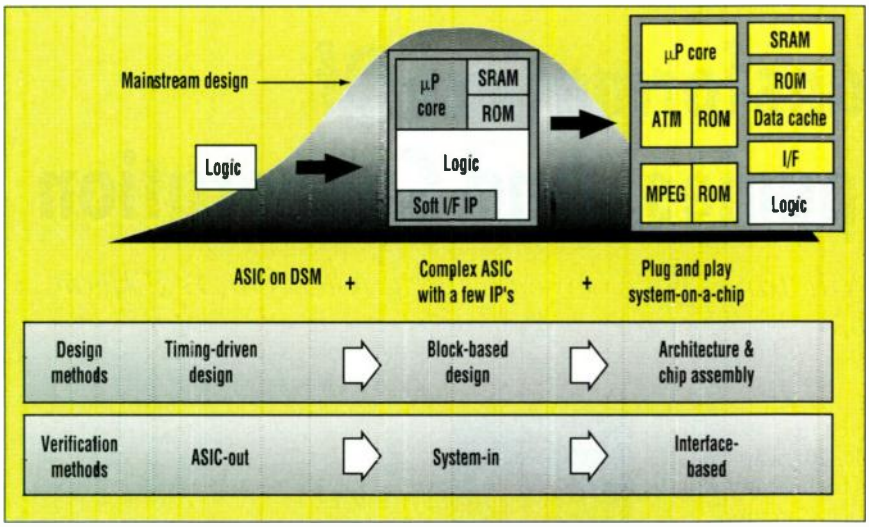
Sounds crazy? Don't believe we can make it happen? There are certainly many technical and business hurdles to overcome. Well, when you have hundreds of billions of dollars of semiconductor investments and the next trillion dollars of growth in the electronics industry at stake, you find a way. It's not because we want this to happen, it's because this must happen. How else will we bring evermore attractive products to the price/performance level that fickle consumers demand? How else can we leverage this silicon capacity?

No, at 0.35 µm with one or two virtual components on board, companies won't find a way. But, once 0.18 µm comes, with $3 to $4 billion fab investments behind it and the promise of realizing the first Dick Tracy watch, people will find a way. Unfortunately, 0.18 µm is not far away *(see the table)*. It's coming online in 1999 and will move into the mainstream in the high-growth electronics markets by 2001.

It is clear that industry discontinuities don't happen overnight. Today, if you polled the average engineer, who is struggling to realize a design comprising gates in the



1. As the concept of intellectual property (IP) takes hold, it will change not only designer's job description, but the design process as well. Tomorrow's IP-based designs will rely on systems integrators, planned reuse, and concurrent system and chip design.



2. Design methodologies will progress from timing-driven designs to architecture and chip assembly. Similarly, design verification will move from ASIC-out techniques to interface-based approaches.

hundreds of thousands, you would likely get a very different prediction of the future than the one described above. Even the senior executives are only now starting to come to grips with the changes that are occurring. As a result, they are assigning special task forces to think about the problem in more detail. These task forces are arguing every day in war rooms about the different technical and business hurdles that they must overcome. Many are skeptical about wasting time in these seemingly endless planning cycles.

They know that only their engineers, not third-party IP garage shops or design service providers, can design the best building blocks and integrate them into silicon. They also know that formalized interface standards hinder the engineer's ability to optimize that last bit of silicon, and that royalties are, and will always be, impossible to pay. They are proud of what they've learned so far in their career, and there's no way that they'll let this "leg up" go away. Hey, I felt the same way about 14 years ago. I was extremely good at optimizing P/N ratios in custom chip design for communications systems. I hated the thought of using a standard cell library that some other engineer developed. I knew that I could make that flip-flop and adder faster and denser.

So, the first step for each organization and each engineer, is to accept that we are in the middle of a transition. When you are in the middle, it's easy to be confused. There are great arguments both for and against change. Rather than fight change, we must map out the incremental path from where we are today to where we want to be in the future. We believe that there are three key stages to this evolution: the acceptance and cultural evolution stage, the intracompany mobilization stage, and the intercompany or industry-wide change.

Becoming Systems Integrators

It is clear that we can't make progress toward developing the technology and business infrastructures of the future unless we accept that we must make three fundamental cultural and organizational changes. We must: move from silicon craftspeople to systems integrators, move from no reuse to planned reuse, and move from concurrent logic and physical design to concurrent system and chip design.

Today we have a silicon craftsperson culture. We are always crafting the best devices, paying special attention to selected details to optimize performance, power, or cost. But let's think about what systems on silicon means. Today, a consumer-electronics systems engineer focuses on developing the best architecture and integrating the best commercial components with very few proprietary components and software. And, that engineer also must meet the deadlines for Comdex and/or Christmas. Sure, the engineer could develop every component from scratch, but the company would be out of business within a year. These consumer-electronics companies survive today because they have systems integrators, who only focus on differentiating value. As these systems move into silicon, the craftspeople of today must become systems integrators of tomorrow.

By thinking of ourselves as systems integrators, we can start to tackle the challenge of developing internal standards, design methodologies, and the right corporate partnerships and business models for success. With that end in mind, we can map out an evolutionary path from where we are today to the future *(Fig. 1)*.

As we have move into a time where reuse is becoming necessary, rather than optional, we still see very little or no reuse occurring. The reuse that does occur is usually opportunistic, in that it serves only as a starting point for endless modification and reverification. Today's NIH (not-invented-here) mentality leads designers to feel that they can always do better (which they usually can), while they point to a lack of tools to solve the reuse problem. However, the main issue is that we haven't really adopted the concept of reuse as a new foundation of our business, yet. As stated, we are in the middle of a transition.

Therefore, we still have many valid arguments about why it won't work. We don't actively work to change the incentives and culture of our internal organization, nor provide the stan-

ANTICIPATED DESIGN EVOLUTION

	1997	1998	1999
Process technology	0.35 µm	0.25 µm	0.18 µm
Cost of fab (billions)	$1.5 to 2.0	$2.0 to 3.0	$3.0 to 4.0
Design cycle (months)	18 to 12	12 to 10	10 to 8
Derivative cycle (months)	8 to 6	6 to 4	4 to 2
Silicon complexity	200 to 500 kgates	1 to 2 Mgates	4 to 6 Mgates
Applications	Cellular, PDAs, DVD	Set-top boxes, wireless PDA	Internet appliance, portable products
Primary IP sources	intragroup	intragroup	intercompany

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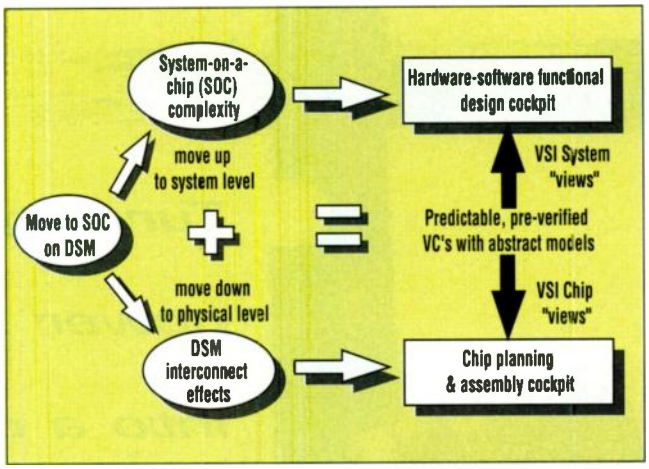
dards and infrastructure to facilitate reuse. We also don't actively work with outside suppliers, who do need active subcontractor management and cooperation if they are to be shaped into a quality virtual-component supplier.

Reuse is not for free. For example, ASSP vendors live or die by how reuseable they make their designs. This includes designing to industry function and interface standards, creating some level of programmability, and productization of designs via characterization, documentation, reference designs, development systems, and support. Like everything else, you usually get what you pay for, in working with both internal and external virtual-component suppliers.

Leading companies are already looking at reorganizing to create organizations that run on the incentive system. They'll create reuseable components, and those responding to the incentives will integrate the best internally and externally developed components into end applications. Most half steps have been disappointing or failed completely. These types of organizational and cultural changes will be required to move companies from no reuse to well-planned reuse.



3. Looming on the horizon is a technology dichotomy. There is a need to move up to higher levels of abstraction to deal with design complexity. At the same time, dealing with the unpredictability of deep-submicron interconnects mandates a move closer to the physical level.

Concurrent Designs

Most of our focus in the IC world today is on managing the transition to deep-submicron process technologies. We are trying to create a more concurrent logic and physical design process that anticipates the effects of interconnect throughout the chip-design flow. The transition to system-on-a-chip will require a change in the way companies think about design, and organize for design. There must be a move to a concurrent system and chip design process.

For example, as we start to embed system functions like processors into silicon, we quickly discover that the choice of block greatly affects the system and software performance. We find that the systems engineers must consult closely with the IC engineer when making the choice. As we decide to put embedded DRAM on board, we find a similar occurence. The use of embedded DRAM has huge architectural implications for the system performance, and likewise, the very wide data buses have huge implications for the chip implementation. When it comes to verification, we see another example where the chip test bench must now be developed by the systems engineer. This engineer is the only one that really understands the very complex system environment. Yet, the implementation engineer must plan out a functional verification strategy that includes hardware and firmware in the context of this same environment.

It is clear that the current approach to IC design needs to change. The reliance on tight, concurrent working relationships between IC and systems experts will fundamentally change the way design organizations and teams are created. And as these teams become ever-more geographically dispersed and span corporate boundaries, it also will fundamentally change the way we communicate.

Intracompany Mobilization

Once companies begin to change their culture, organization, and communications structure, they will be ready to move on to develop a potentially effective intracompany mobilization plan. The key to this stage is to map out the product development methodology evolution, spanning system, chip, hardware, and software boundaries, and leveraging both internal and external suppliers. The methodology roadmaps will coincide with categories of device types being developed. The adoption of the methods will be driven by the associated economic and time-to-market pressures of the business. To be effective, an incremental series of steps will be identified, with each step building on the previous step's foundation.

The ASIC methodology foundation (labeled "timing-driven design") must first be established for deep sub-micron *(see Fig. 2)*. The timing-driven design is where physical design, leveraging design planning technology, is done in parallel with the logic design to manage interconnect. Verification at this stage is still done with traditional HDL simulators, with test vectors created "out" around the boundaries of the ASIC.

The second methodological shift supports the embedding of selective reuseable system building blocks, such as a microprocessor or standard peripheral. It also supports a new level of logic complexity. This design methodology is called block-based design. It requires partitioning based on clean functional interfaces and physical interconnect considerations (versus synthesis tool partitions). A new hierarchical design flow through physical levels also is needed. In addition, to accommodate the increasing complexity and inclusion of embedded processors, a shift from ASIC-out to system-in verification is required. System-in verification involves the early full-system-level modeling of designs and complex system environments at a behavioral level. The implementation of various system functions in silicon are then verified in context of this system model (test benches are passed down). In addition, high-speed processor models and hardware prototypes or emulation combine to support hardware-software coverification.

Finally, to evolve the support to true "plug-and-play" system-on-a-chip, the methodology begins to move to a higher level of abstraction and center around interfaces. Predictable, preverified virtual components will be modeled at a high level so that the design can focus on system evaluation, architecture, and functional integration of virtual components. Standard integration platforms (and associated interface standards such as on-

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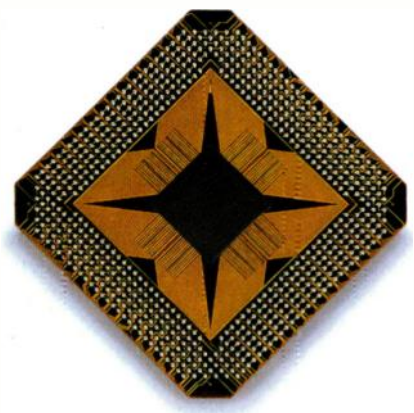

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chip buses and test buses) will allow blocks to communicate and be rapidly assembled into implementations. In addition, the exponentially increasing complexity of verification will be managed by breaking apart the problem—partitioning the verification of blocks from the verification of interfaces.

The Methodology Evolution

Note that at each stage, the form of the IP development and reuse approach must evolve to fit into the chip development and integration approach. Initially, companies using block-based design will tend to leverage a fairly opportunistic source reuse approach, usually using RTL as a starting point for a block that is then modified, implemented, and reverified. Companies then increase reuse productivity by moving to more planned reuse techniques, where the functional core is designed in a predictable, preverified manner (firm or hard). Later it is coupled with standardized interfaces based on an application-specific integration platform (on-chip buses, test buses etc.).

Clearly, the entire design, verification and reuse methodology evolution must ultimately address the technology dichotomy. We must move up in abstraction to deal with complexity, while moving closer to the physical level to deal with the unpredictability of deep-submicron interconnect *(Fig. 3)*. This task is accomplished by the development of predictable (firm and hard) virtual components with abstract models that can be trusted in system-level design.

With the aforementioned changes in our culture, organizations, and intracompany product development methodologies, we will build the foundation for broader change across the industry. Today, we have two key industry initiatives with a focus on building the infrastructure for future. These include the VSI Alliance for the technical infrastructure, and Reusable Application-Specific Intellectual Property Developers (RAPID) for the business infrastructure. These organizations are slowly building tremendous momentum, as more companies begin to understand the ramifications of this ongoing transition. The leading companies are taking the output from these organizations as starting points for their internal infrastructure development efforts. For example, companies will start with the VSI 1.0 specification as a basis for internal virtual component standards. They will define data formats based on their own preferred tools and flow, and define design interfaces based on their application-specific integration platforms and their chip development methodologies. This process results in a proprietary VSI application guide.

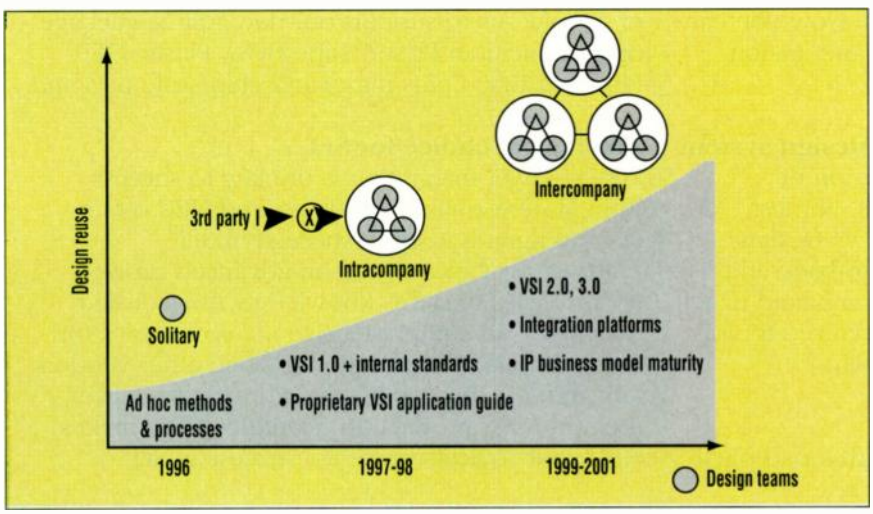
As time evolves, we will see companies use more of the public standards both internally and with their suppliers *(Fig. 4)*. In the next few years, de facto standards will emerge that can be incorporated into the formal VSI and RAPID specifications. As a result, around the year 2000, we should see reasonably efficient licensing and utilization of virtual components across corporate boundaries. Eventually, as new consumer applications mature, we will even see selective standard integration platforms and associated interface standards facilitate true plug and play of virtual components developed from multiple sources.

Certainly corporate specialization, hardware and software virtual components, a third-party IP/virtual-component industry, independent design-service providers, and corporate and industry standards are all part of our destiny. Some of us are busy creating this future while others are fighting it—all within the same company and sometimes between companies.

We must accept that there are first some fundamental changes that must occur in how we think; resulting in fundamental changes in our culture and organizational incentives. We can then effectively mobilize our own companies to evolve product development methodologies and standards necessary to manage the exponentially growing design complexity. Finally, with this common foundation in place within our companies, we will accelerate the development of a truly efficient set of technical and business standards across companies.

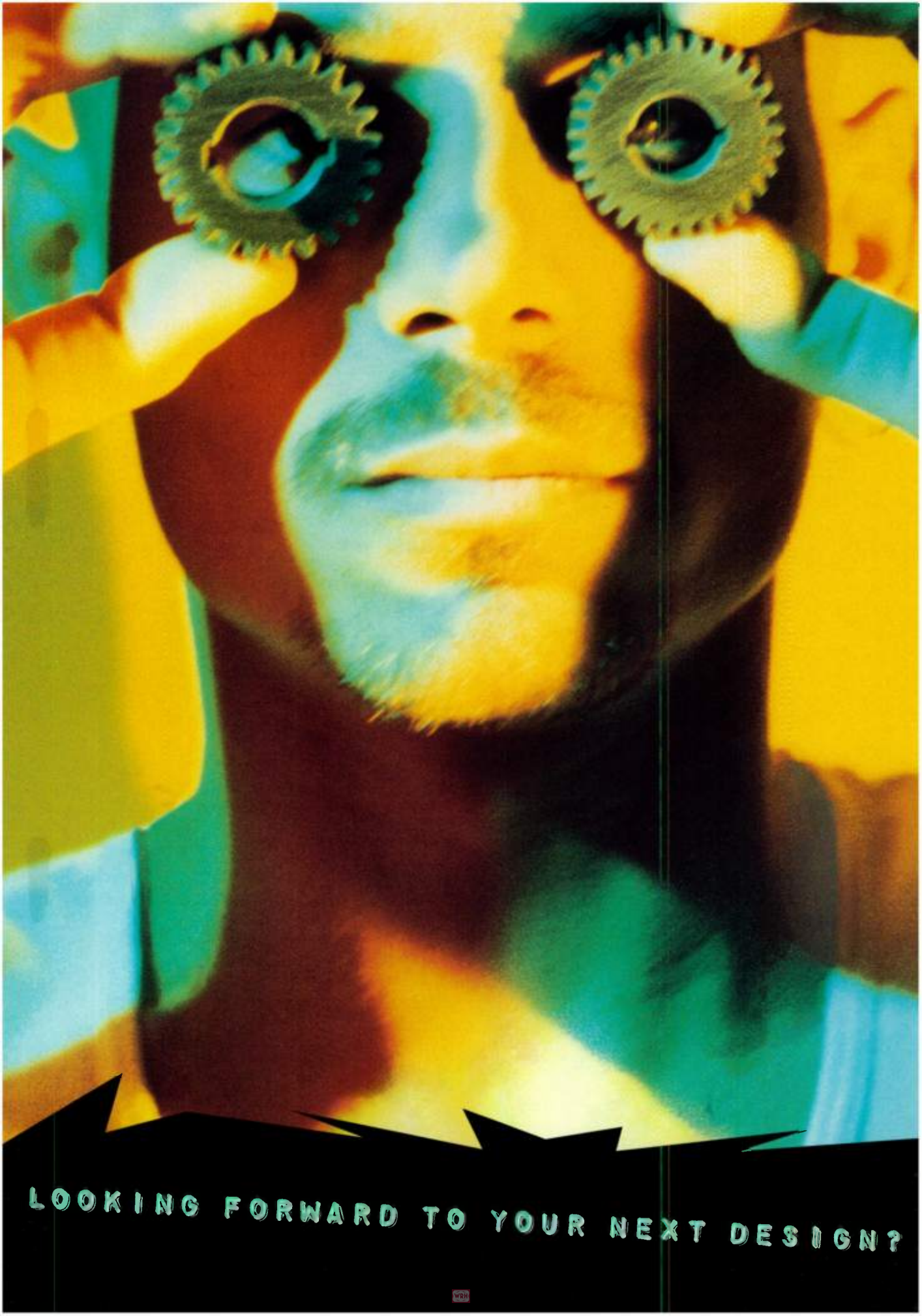
So, expect huge changes ahead in culture, companies, cooperation. Together, these changes will facilitate the development of new consumer products at price/performance levels never thought possible. And they will facilitate the utilization of silicon capacity and realization of silicon margins necessary to fund more generations of multibillion dollar fabs. Ultimately, these steps will facilitate the next trillion dollars of growth in our electronics industry, and lead to societal breakthroughs that improve all of our lives.

Steve Glaser is vice president of marketing, system-on-a-chip, for Cadence Design Systems. He holds a BSEE from the University of California, Santa Barbara, and an MBA from the University of British Columbia, Canada.



4. Widespread availability of IP will bring about a transition from intracompany to intercompany standards. By the year 2000, reasonably efficient licensing and utilization of virtual components across corporate boundaries should be in place.

How Valuable	Circle
Highly	560
Moderately	561
Slightly	562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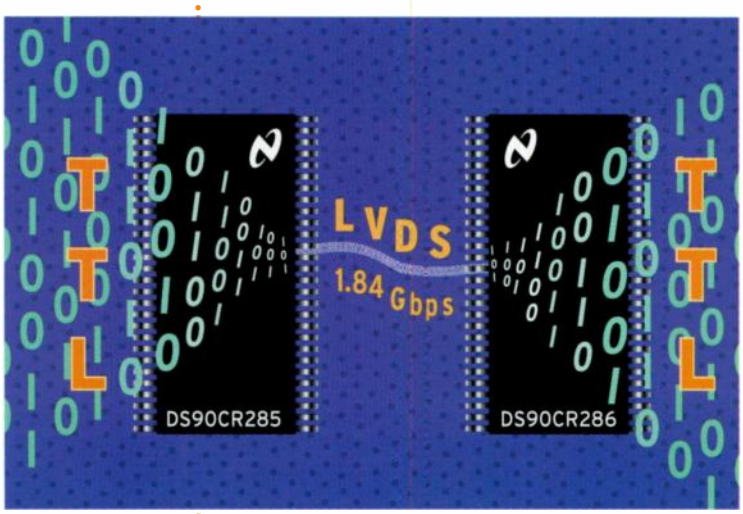

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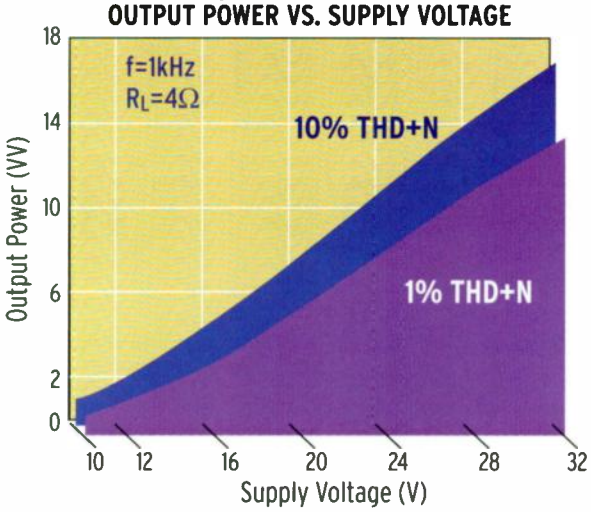

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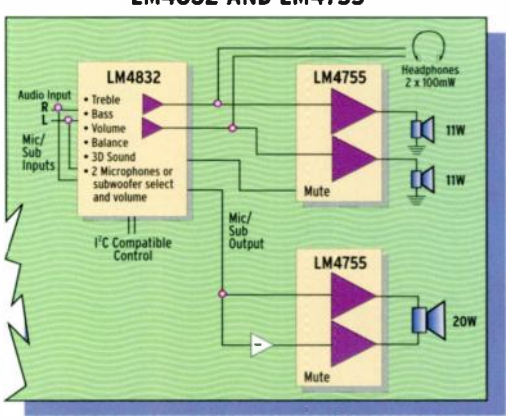

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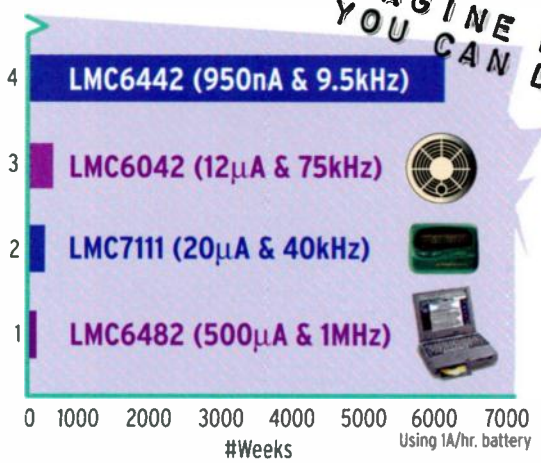

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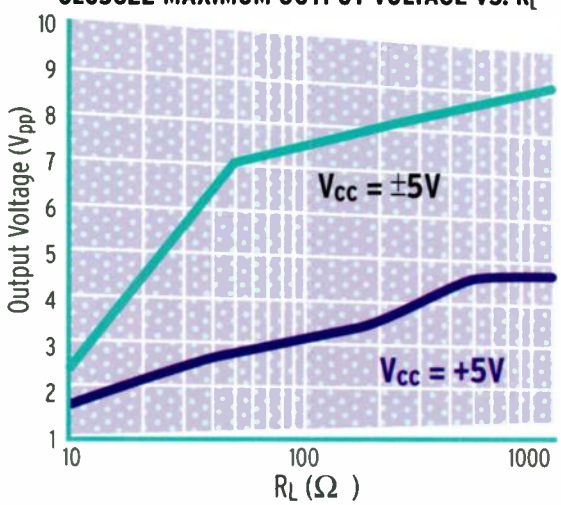

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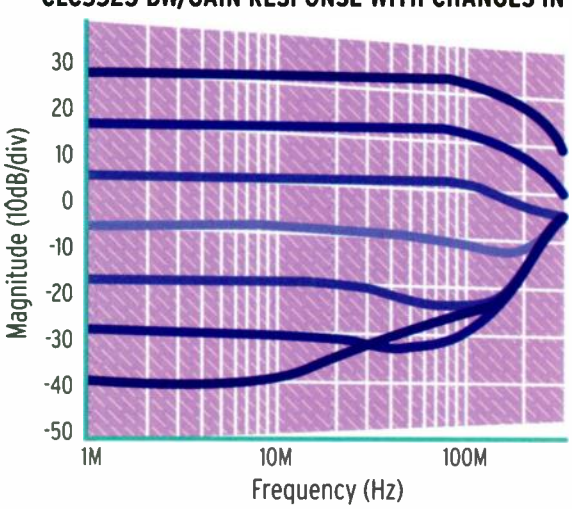

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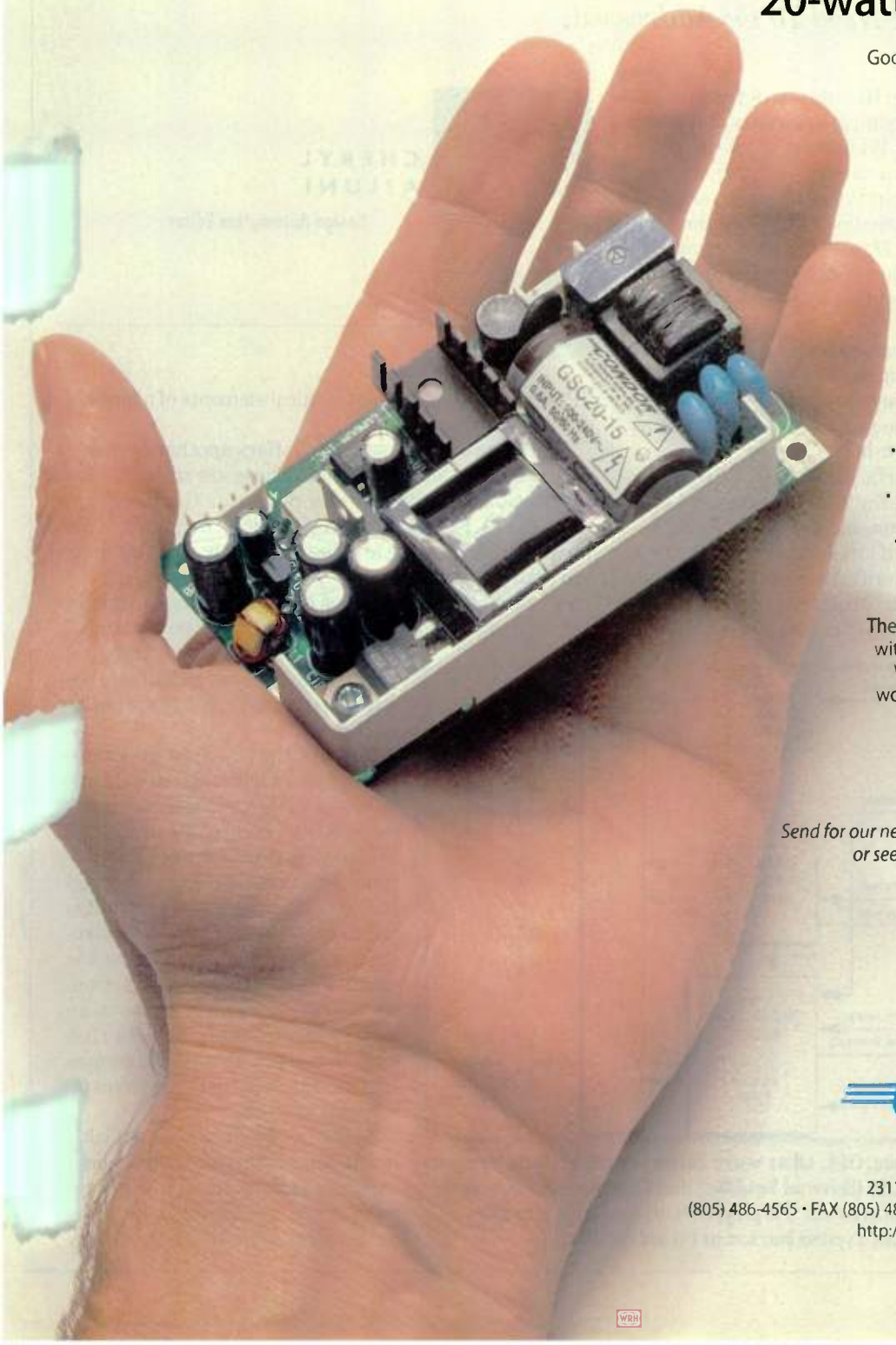

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CHERYL AJLUNI
Design Automation Editor

Let's start at the beginning: How do you define intellectual property (IP)? The simple answer is that it depends on who you talk to. While most people in the industry agree that "IP" is a catchy and high-valued phrase, it is not very descriptive of the business that most electronic design automation (EDA) vendors engage in *(see "Design reuse, IP, and the name game," p. 65)*. For this reason, a number of other more definitive terms have evolved in attempting to explain what IP is really supposed to mean.

IP typically refers to ideas, concepts, or algorithms that can be made functional in hardware and/or software *(Fig. 1)*. In legal terms, it's any nontangible property or asset of a company that is the result of creativity, such as patents, copyrights, and know-how.

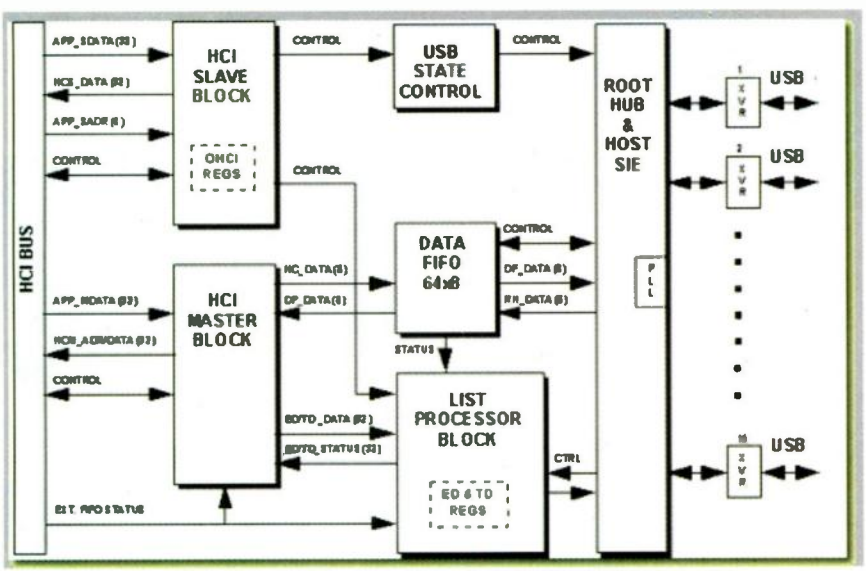
The Virtual Socket Interface Alliance (VSIA), San Jose, Calif., has another definition. It defines what it refers to as Virtual Components (VC) as pre-implemented, reusable modules of intellectual property that can be quickly inserted and verified to create a single-chip system. As Doug Fairbairn, president of the VSI Alliance, San Jose, Calif., explains, "To simply use the term IP neglects one of the most critical elements of a block of IP; that it be reusable."

Dataquest, San Jose, Calif., offers another option—System-Level Macros (SLMs). These are silicon implementations of virtual components. Gary Smith, Dataquest's EDA analyst, has a unique definition of his own: "It's [IP] as close to being completely undefinable as anything I know of."

While it is true that IP has many incarnations, most in the industry seem to agree on the driving forces behind it, and that it will have a huge impact on the types of EDA tools being offered today *(see "The promise of IP," p. 70)*.

Perhaps the two most prevalent driving forces behind IP would have to be the design gap and consumer demands on electronic products. While the demand for more sophisticated devices is matched by manufacturing technology and capacity, it is not matched by available design resources. To make matters worse, the consumer market is driving electronics system providers to cut costs, increase functionality and shorten time-to-market. To respond, companies must develop entire systems on a single silicon chip.

Synopsys, Mountain View, Calif., points out that this increase in silicon capacity and decrease in time-to-market are causing the industry to focus on reusable IP. The company



1. Sand Microelectronics, Santa Clara, Calif., offers what's known as a soft intellectual-property core. This core, referred to as the USB (Universal Serial Bus) Host Controller core, can be easily integrated into a PC or workstation to provide USB peripherals. Its main usage is to allow designers to create a bridge between a system bus, such as PCI and the USB.

indicates that designers are now able to fit more on a chip, but have less time to design and develop it. For example, an average 1-mm^2 chip requires 230 man-years to create from scratch.

This simply is not a realistic option for today's time-crunched designers. The use of IP seems to be the only solution, but it is one that comes with a huge price tag. While the cost of IP will eventually come down, the changes that it will cause to EDA tools as we now know them, and to the EDA industry as a whole, are guaranteed to be dramatic.

EDA Roadblocks

Although IP sounds like the answer to the design of large, complex devices, the truth is that it brings up a number of technical, business, legal, and protection issues that designers did not have to face before. Although some will argue that the technical issues are the easiest to fix, if they are all not adequately addressed, there is little doubt that widespread proliferation of IP and IP-based design will be hampered.

According to Cadence's Fairbairn, "The VC user asks four straightforward questions; and today, there are no easy answers. How do I find VCs? How do I evaluate VCs? How do I buy VCs? How do I use VCs? Even the seemingly simple task of finding out what is available can prove to be a challenge due to the lack of established market channels. When you do find it, it is difficult to evaluate one VC against others, or to verify that it will work in your system."

Perhaps the most daunting technical issue facing designers using IP is verification. This stems from the fact that the integration of IP blocks makes for a large, extremely complex design. As a result, verification of the blocks and of the design is an even greater challenge. This verification problem is not inherent in the IP blocks themselves, but rather with the designers who feel compelled to tweak a synthesizable design rather than use it as purchased. Any change to the IP, no matter how minor, means that the IP block is suspect and must be completely reverified. The other difficulty stems from verifying the entire assembled system, which may contain numerous blocks of IP all coming from different vendors *(Fig. 2)*. Finding a methodology to address all the subtle differences between the IP blocks can be quite daunting.

To deal with these issues, IP users are looking to ASIC vendors to obtain IP solutions and characterize them for their processes. The downside to this is that the IP becomes part of the ASIC vendor's library, and is not portable. While this might be an immediate and acceptable solution for the IP user because the ASIC vendor assumes most of the risk of using IP, the disadvantage is that the user is then locked into a particular ASIC vendor/process. And, since the ASIC vendor can only provide a limited amount of integration services, the potential to create a bottleneck in the production cycle is high.

So what is the solution? To enable these more sophisticated verification

Design Reuse, IP, And The Name Game

About the same time that MIS (management information systems) became IT (information technologies), IP took center stage as the new corporate asset. In that broad context, understanding, managing, and protecting IP, the tangibles and intangibles, became a new crusade. As the dynamics in the chip design market started to open the way for systematized design reuse, IP was still a hot term. That's pretty much why it got picked up as the nomenclature. So came IP onto the IC design scene; it brings an image of importance; it sounds valuable; it conjures intuitive notions; and it is broad enough to encompass any sort of knowledge of expertise that might be applied to improve productivity. But who is the biggest winner in IP so far? The honorable law firm of Wilson, Sonsini, Goodrich, & Rosati. This ought to be more than a red flag to the engineering community.

If we used another name, for example, something like LSI Logic's megacells from ten years ago, Gary Smith's suggested system-level macros, or VSIA's virtual components, would we devote a third or more of our technical conferences on the subjects of legal issues and business practices? Would a lawyer ever be invited as the keynote speaker? Undoubtedly not! We are being distracted from the truly critical issues.

There is much too great a preoccupation with protection as an issue, probably because of the chosen name. Certainly protection of value is a concern, but the schemes being considered are much more expensive and much more elaborate that those that protect $100-K software packages. As an example, you can change the CPU ID of a Sun workstation in about two minutes. There have been no publicized cases of third-party IP vendors being ripped off, and companies risking the investment in systems-on-a-chip implementations are very unlikely to jeopardize the millions of dollars involved by illegal action. Certainly the technical barriers we face today that are blocking efficient, widespread reuse far outstrip the threats presented by theft.

What is the essence of what we would like to embody in the name?

Productivity—mechanisms to improve time-to-market for mega-sized systems-on-a-chip designs.

Value—acknowledgment of true value being delivered and a desire to build a viable marketplace.

Diversity—many forms of expertise that can be sold to speed systems-on-a-chip designs.

So what is a better alternative? Well I don't know, but sometimes changing a name is the easiest way to start changing behavior. How about Engineering Expertise Reuse Information? Wouldn't that be EERI...?

Contributed by Steve Carlson, vice president of marketing, Escalade Corp., Santa Clara, Calif. For further information, contact the company at (408) 654-1600, or check out its web site: http://www.escalade.com. Carlson can be reached via e-mail at steve@escalade.com.

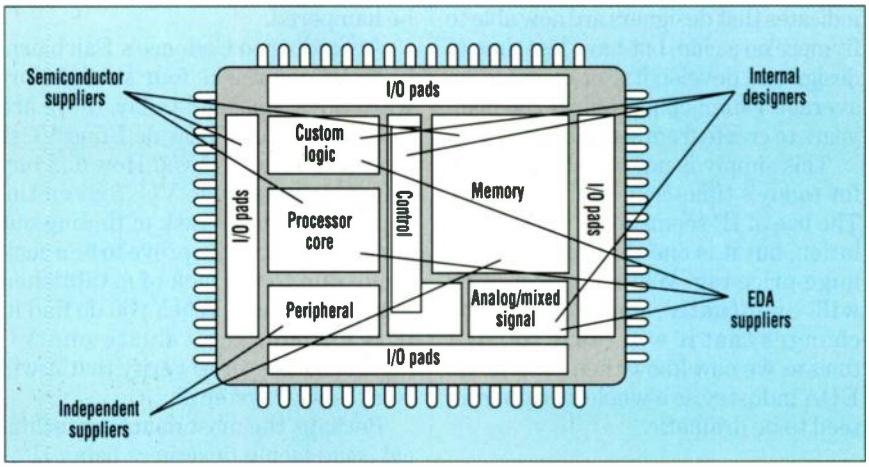
strategies, complex IP needs to be supported with a variety of simulation models. Synopsys and Viewlogic (the latter recently acquired by Synopsys), are now working to address the verification issue by developing a number of modeling tools and solutions that will simplify and improve verification and protection of IP. These tools will allow the creator of IP blocks to build and distribute simulation models to support the kind of sophisticated verification environment needed for SoC (system-on-a-chip) design.

But this is only the tip of the iceberg. Current design languages (Verilog and VHDL) were developed with a simulation paradigm in mind—not a verification or reimplementation scenario based on automated synthesis or generation techniques. As a result, EDA companies have had to define their own descriptions of design intent/constraints. This representation of design intent/constraints needs to be carried throughout the design flow in any IP-dominated SoC verification environment. Also, at VDSM (very deep submicron, or less than 0.18 µm), event-driven timing simulation peters out and is unable to cope with the number of critical interconnect paths to be resolved. What's needed is a purely static design methodology approach—in other words, static timing verification.

Another issue that needs addressing is how to make IP reusable. To accomplish this task, a standard design methodology for the development of a reusable design and standard interfaces are imperative. Without these standards, designers will never know what they are getting and will be forced to struggle with integration issues.

Addressing The Issues

It is not surprising that these standards have yet to be defined, considering the IP industry's infancy. Not to be overlooked, however, is the effort by the VSIA to address all of the issues surrounding the making of SoCs with mix-and-match IP a reality. Standards are certainly on the top of VSIA's task list. In fact, established working groups are now working on the challenge of defining the technical issues and standards to address standard IP development and use in SoC designs. VSIA is working in six key areas to define the interface standards that will allow the plug-and-play of virtual sockets. These include:



2. As the use of IP becomes more prevalent, it will become commonplace to see designers incorporating multiple cores of IP into a single design, as depicted in the diagram. This poses unique issues of how the designer will be able to integrate the cores if they all come from different vendors and how will the designer verify the entire system. These questions are now the subject of intensive scrutiny by a number of EDA vendors.

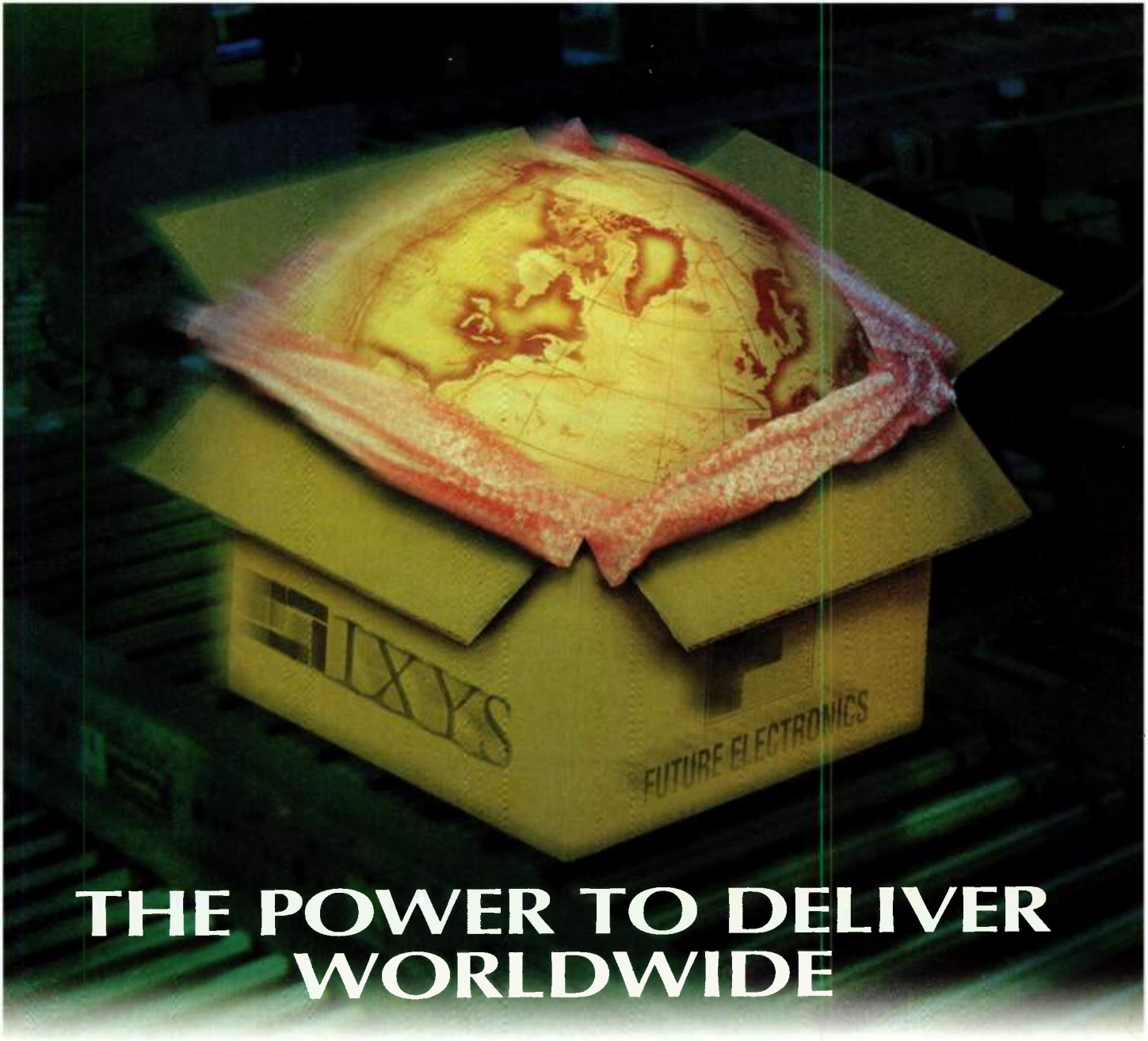
- Test standards and design guidelines for test structures, test methods for VCs, and test infrastructure.
- Standards-based solutions for IP protection that balance necessary levels of security with customer VC usability.
- VC standards that enable the implementation and verification of the VC and the system chip containing the VC.
- Standards and guidelines to facilitate the integration and test of mixed-signal VCs in a largely digital system chip.
- On-chip bus specifications for the design, integration, and testing of multiple functional blocks on a single piece of silicon.
- Standards to enable the VC user to evaluate and select the various VCs that are to be used for the system chip within the context of the overall system-chip specification.

A critical element of effective design reuse is a standard interface among design components, such that multiple cores of IP can be implemented in the same design. Without these standard interfaces, designers will find it very difficult to connect various IP elements, especially in the area of IC design. While the VSIA is trying to establish standards in this area, many EDA vendors are developing their own methodologies and tools for implementing SoC designs using IP from various sources.

As Christy Adkinson, product marketing manager, Cascade Design Automation, Bellvue, Wash., points out, "In addition to the interface standards that address system-level requirements that are needed, migration tools that enable IP (cores and megacells) to be reused in different process technologies or different designs, and standard data formats that are widely recognized by the majority of design tools (GDSII, SDF), also is a must." Despite the work in these areas, progress is slow, and results are expected to come on an incremental basis.

Two other critical issues that must be addressed by the EDA industry are the development of tools that can work at higher levels of abstraction for both specification and verification, and a design reuse methodology. Mike Walsh, president and CEO of Omniview, San Mateo, Calif., explains, "The design component needs to be comprehended if it is going to have value from a reuse perspective. What's needed are tools that work at higher levels of abstraction that can map down to lower level tools and do the actual physical implementation."

Ideally, this new class of tools will work at the architectural level of design. Other requirements include the ability for these tools to provide reasonably accurate estimates of eventual system performance, and global search engines at the architectural level that can provide an environment for design



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reuse and component selection.

Walsh also notes that the "value of a design reuse environment is directly proportional to the level of abstraction of the design—the higher the level of abstraction at which a designer can work, the more value that can be achieved by design reuse." Two promising technologies being investigated to address the abstraction issue are constraint theory and performance modeling at the architectural level.

On the design reuse environment or methodology side, the need for new tools is more critical. Today, designers attempting to reuse IP manually link blocks of IP, which is a labor-intensive, time-consuming process. As Brian Barrera, director of marketing for the IP Division, Mentor Graphics, Wilsonville, Ore., explains, "The design reuse methodology is a serious issue because standards for data formats from VSIA will not address the differences between simulators, test tools, and synthesis tools. What is required is a methodology for guaranteeing that a core will work in a variety of tool flows. Otherwise, designers will have a standard set of models that won't work with their tools."

Complicating the matter is that integrating a large netlist into a layout has become a serious problem for DSM designs, primarily because neither place-and-route nor floorplanning tools are keeping pace with the reality of DSM. The methodology for moving from synthesis to layout requires new tools and new flows.

The good news is that there are proposed solutions to address some of these issues in the works. According to John DiFerdinando, vice president of marketing, Summit Design, Beaverton, Ore., "We're looking at providing a solution to the long-standing industry need to generate a standalone model from existing VHDL/Verilog descriptions. This allows designers to share executable specs with no risk of disclosing the actual source of the model. This would be an environment where multiple IPs can be integrated in a similar format and entire systems can be built using existing IP components."

Cadence suggests that the answer lies in the use of key technologies such as block-based timing characterization, chip assembly tools that support the efficient integration of large complex blocks while addressing the signal integrity issues associated with DSM design, and verification environments that support models and testbenches that are linked across multiple design abstraction levels. System-level design tools that support IP evaluation and integration at high levels to deal with design complexity and size, yet are linked to implementation paths, also are essential. Any new design technologies and associated methodologies must span across the hardware, software, digital, and analog ranges.

Mentor Graphics and Synopsys have joined the effort to address the issue of IP integration and interface standards and are now working on the development of a design reuse methodology. The methodology has the goal of defining how to develop IP that works with a variety of tools. To date, a draft manual has been developed and is under review by actual design teams that have completed large chip designs using IP.

A QuickUse Initiative that addresses the issue of integrated functionality with other IP, its availability, and its protection, also is underway. Participants include Aptix Corp., San Jose, Calif., GateField Corp., Fremont, Calif., and Mentor Graphics. Charged with the task of solving the critical and time-consuming IP integration issues, it makes IP available in a secure format by placing it on encrypted, nonvolatile ICs like the proposed GateField ProASIC technology. It can be combined with other IP and new design blocks and physically prototyped and exercised on an Aptix reconfigurable prototyping platform.

In effect, the initiative provides the designer a simple path from design concept to silicon using IP. Ralph Zak, Aptix's president and CEO, adds: "IP providers must work with individual foundries or ASIC manufacturers for the physical implementation, or work with foundries that support foundry independent technology as is being worked on by Synopsys."

The legalities and protection of IP are major areas of concern for those wishing to utilize IP in the design process. But, it is one that will no doubt be resolved, at least in part, by the development of new business models and pricing structures. The problem is that IP suppliers want to be able to sell or license IP to designers, without the risk that this IP will be used without authorization, reverse-engineered, or tampered with; potentially causing the failure of the whole design.

On the other hand, to design in the IP, the designer must be able to see or know certain things. The issue of protection is especially problematic for soft IP since its source code contains all of the value, yet is trivial to e-mail around the world. The bottom line is that designers want to know that if they purchase IP, there is some sort of warranty that will guard them against something going wrong with their purchase.

The question is: How does the industry find an efficient way to protect the IP while also revealing enough information so it can be used easily? There really is no simple answer. Synthesis tools today require source code and IP customers need access to the source in order to debug at the gate level. One train of thought suggests that EDA tools need to evolve to the point where designers no longer feel they need source-code visibility to create and verify SoC designs. Other proposed solutions for protection involve encryption techniques *(see the "IP Protection" article from Modeling Technology, p. 108)* such as those being worked on by VSIA. Most IP providers also are working on their own methods of protection. EDA tool vendors, for their part, are working on ways to handle encrypted design content.

Another issue facing EDA tool vendors is how to deal with the interconnect barrier. As Martin Walker, president and CEO of Frequency Technology, San Jose, Calif., explains, "The future of chip performance will be dictated by the interconnect. However, the interconnect behaves differently in every different design process. Therefore, for IP to be truly useful, it will be critical to have an accurate analysis of the interconnect's performance in each process." Once this interconnect information is obtained, designers will be able to gain a better, more accurate understanding of the chip's performance. With chip performance a determining factor in its value, such a capability is essential in an IP-dominated design.

One proposal is the development of a technology that enables a true 3D analy-

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stream, and well-defined inter-company industry standards and inter-company IP will be readily available.

So what's going to happen down the road? Devices and functions will continue to grow, along with increased time-to-market demands and shorter design cycles. Systems integration on silicon will become more mainstream. Logical IP will become more routine. And, compiled models will most likely evolve to provide better support for licensing and a more reliable implementation.

Most of this sounds easy enough to deal with, but the fact is that as designers are forced to integrate more functions on the same device, the design process will need to be abstracted to a higher level. Cores also will need to be provided that can efficiently work at these levels of abstraction. And, as Roman Iwanczuk, director of the CORE Solutions Group, Xilinx, Inc., San Jose, Calif., explains, "As designs become larger, the issue of connectivity between cores and buses also increases in importance."

As many people in the EDA industry aptly point out, the goal of IP is to have plug-and-play capability, in much the same way pc-board designers currently have. These designers simply plug standard parts into pc boards with the expectation that they will work properly in whatever system context they are used. John Cornish, design consulting manager for Palmchip Corp., San Jose, Calif., says that "chip designers will come to view IP blocks as 'black box' functions just as system-level designers view discrete standard parts today. IP users will never need to investigate the inner workings of the block; they will just expect it to function according to specification in the target process and ASIC library."

Having this plug-and-play IP capability would free designers to focus on how IP blocks are integrated to provide the most product differentiation. By comparison, many designers today are forced to focus on differentiation through how the blocks are built. This plug-and-play capability will likely occur earlier than three to five years within most companies, while becoming more commonplace for inter-company exchange in the three-to-five-year time frame.

In the next few years, larger, more complex designs, dominated by IP, will force IC designers to take account of physical process information much earlier in the design process. According to Luke Collins, program coordinator for the IP 98 Conference, "At the same time, design descriptions will need to be divorced from that constraint in order to be freely sharable." Potential solutions to such requirements might include different description methods and greater use of hybrid fixed-function field-programmable-function arrays.

Another issue that will arise is the notion of IP maintenance. IP maintenance, the way we think traditionally of maintenance, is an expensive and time-consuming proposition. But, have you ever wondered what will happen when the target technology changes and designs can no longer easily be ported between processes? Reuse standards must be developed to address the inevitable changes in the tools and methodologies. Data formats also will be necessary, but they alone will not be sufficient to solve the problem.

The fact is that designers must become more proficient at working out system-level issues such as standards compliance and system-interconnect performance. In addition, solutions such as a virtual prototyping methodology must be fast enough to process enough vectors to verify compliance to system-level standards. To deal with system-interconnect performance, EDA vendors will look to solutions such as an automatic interface synthesis from a selection of bus and point-to-point interface schemes.

On the business side, EDA vendors expect the development of standardized business models in the next three to five years. As Cadence's Fairbairn explains, "The time to sign contracts won't exceed the time to do the actual design. In fact, it will become significantly shorter." This is crucial since it means that large catalogs of IP will be widely available. Designers will be able to browse IP databooks and select appropriate blocks for their design.

With the expectation that most, if not all, of these databooks will be on the World Wide Web, designers can download basic technical information and contact the IP provider to make arrangements to use a selected piece of IP. And, as the use of IP changes from offering a market advantage to a performance advantage, designers will need to have the capability to evaluate IP performance. Just as a system designer today might evaluate a graphics controller from various vendors, in three to five years, designers will need the ability to evaluate graphics controller cores.

Obstacles For IP Adoption

Assuming it is only a matter of time before the technical and business issues surrounding the use of IP get squared away, many in the EDA industry suspect that its widespread adoption and use will still be slow going. Part of the reasoning is that a shift in the mindset of designers is needed to help proliferate IP growth, and many designers are reluctant, if not downright unwilling to give up, as Mentor's Barrera refers to it, "the not-invented-here syndrome." Attitudes like that will change once designs pass the 200-kgate mark; designers will then be forced to use IP simply out of necessity. Nevertheless, a change in the way system architects and project managers today think about IP will help to make the transition a much easier path for designers.

Changing the way designers think is only one factor that threatens to limit the widespread adoption of IP and IP-based design. Another key obstacle is the mainstream acceptance of standards. Without standards, it's doubtful that there will be a supply of quality, usable, portable IP available to designers. And, without standardized methodologies and standards governing how IP can be interfaced into these methodologies, it would be virtually impossible to allow interoperability between IP cores and EDA tools to work with these cores.

IP also requires an enterprise commitment on the part of the user. The IP needs to be preserved, organized, and stored in an environment that provides an easy means of reusing it. The only way to accomplish this is with a standardized methodology.

But, as Jeff Garrison, product marketing manager, Synplicity, Mountain View, Calif., notes, "There is serious resistance to the acceptance of standards by all the EDA vendors since the systems-on-a-chip design methodology is threatening their existing business.

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The solution to widespread acceptance of IP still remains for the industry to get behind and fully support open standards that are not based upon any proprietary information."

Ease of integration of IP into SoC designs, along with the ability to quickly understand its functionality to meet your needs, are other obstacles facing IP proliferation. To address the issue of integration, it is clear that IP-centric EDA tools will be a necessity. As for understanding and verifying IP, one way to deal with this will be the ability to generate a standalone model or one that can be used with a Verilog or VHDL simulator. While understanding and verification are issues facing the ability for designers to design with IP today, three to five years from now these issues will become even more prevalent, primarily because as designs grow more complex, so does the time and effort it takes to verify them.

Assurance on the reliability of IP suppliers, and a business model that makes IP use easy and fair for both the user and the producer, also must be addressed. If you are a designer purchasing IP from a supplier, you'd expect to get a production proven core; after all, having to verify the entire IP block would likely take longer than if you just developed the block from scratch. Some of this will be resolved by industry maturity, as companies establish themselves as credible players and IP users grow to develop trust in their IP suppliers.

According to Alistair Greenhill of Advanced RISC Machines (ARM), Cambridge, U.K., "Some organization will have to evolve, similar to the performing rights in the record industry, that administers the distribution of royalties. Without this type of commercial business model, generations of new IP will be suppressed."

While the comparison to the music industry may seem strange, it's a view shared by others in the EDA industry. Andy Graham, president and CEO of Si2, San Jose, Calif., for example, sees it this way: "What's needed is a shared medium of exchange, increasing valuation of silicon-independent IP, and business trust among complementary industry roles. A good example of such a relationship can be seen in the music industry where, for example, the music artist creating content (IP) has a well-established medium of exchange (record companies), established valuation (ASCAP royalties), and business trust (i.e., an artist doesn't need to manufacture his own CDs—it's not his business). To the extent that semiconductor companies become like record producers and IP developers like artists with EDA companies as enablers, the value triangle will be very powerful for consumers."

Another obstacle not to be overlooked is cost. This is an especially prohibiting factor for FPGA users. Most designers utilizing FPGAs are small to medium-sized companies who have limited resources. These designers are struggling with make vs. buy decisions. Part of the solution seems to lie in understanding on the part of the designer of the true value of IP in terms of their time-to-market. For some designers, this realization is only a matter of time and experience. Others, however, will always see price as an obstacle, especially for the smaller company designer wanting to use leading-edge IP. For this group, help comes from the fact that today's hot IP will eventually become tomorrow's commodity product.

FPGA users are not the only designers faced with issues of high cost. As Hitoshi Yamakawa, manager of strategic planning, Excellent Design, Kanagawa, Japan, points out, "Currently, the cost of IP is too expensive to use in system LSI designs. It is rare to find applications that have enough device quantity to use such expensive IP from the standpoint of a set maker. This is because the cost of the IP is calculated from the production cost of the set. Sometimes this cost is quite different from the reasonable IP cost quoted by an IP provider."

There are short-term solutions to deal with this high cost; standardized business models and licensing schemes, for example, but long-term development of a common-demand supply base will be required.

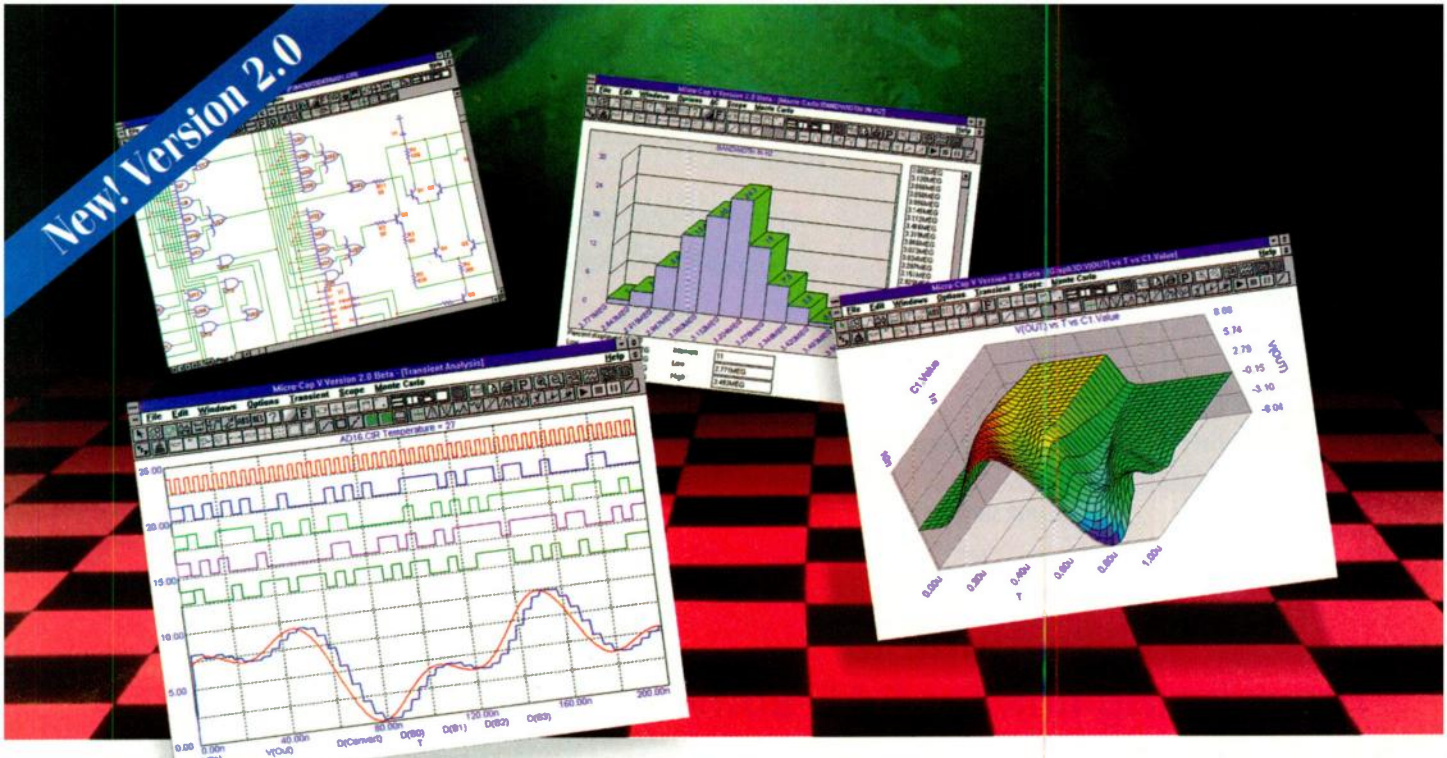
Not to be overlooked is good engineering talent. What's needed is for the EDA industry to actively participate in the education of pre-graduates to help ensure they are instructed in the proper ways to design and to use available design-automation tools. Just teaching them the basics won't work anymore, because the magnitude of the problems future designers will be forced to deal with is overwhelming. They will need to be trained with a mindset toward systems design, heavily populated with IP cores. Some EDA companies, recognizing this issue, have set up agreements with colleges to provide students first-hand access to EDA tools. Perhaps the next step might be student workshops on design methodologies.

The Future Of EDA

It's apparent that IP is here to stay. It will change the way designers design, regardless of whether that involves ASICs, FPGAs, ICs, pc boards, or PLDs. And it will change the way design tools look and feel. There are those that believe that the technical issues that need to be addressed by EDA tools are relatively straightforward, compared to the mass of issues related to IP protection, indemnity, and cost. As Jeff Lewis of Artisan Components, San Jose, Calif., suggests, "These issues may even be all ironed out within 12 to 24 months." But the fact remains that in ironing out these technical issues, the EDA industry and its tools will be changed forever. In fact, some suggest that in ten years, the commercial IP industry will be far larger than the EDA industry.

One way EDA tools will change is in their inclusion of IP as a central part of any design methodology. In fact, EDA vendors will have to support IP in much the same way they've had to support libraries in the past, forcing the adoption of industry and de facto standards. Design methodologies will mature toward system design, rather than circuit design; in addition, they will gain dominance over the traditional point-tool-dominated EDA industry. Consulting services will begin to play a larger role in the overall design process, as a way to help EDA tool users manage the huge discontinuities that arise from IP authoring and implementation. But this is only the beginning.

As Jeff Lewis asserts, "Today, IC design is primarily 'gate banging.' with a little IP sprinkled in. Design in a few years will be just the opposite. Synthesis is the primary tool today for creating ICs; but it will assume a much less important role in the system chip era. And, the same is true for



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gate-level place-and-route and gate-level simulation. What will become important are the system simulators, the virtual prototyping tools, the hardware-software co-design and co-verification environments, and the physical implementation tools that are geared toward stitching large blocks together."

Ultimately, as the IP industry continues to emerge, many EDA vendors may be forced to choose between continuing down the path of providing design tools, or foregoing their past to test the water on the IP side of the fence. Synopsys points out that as methodologies are set in place and system-level design with IP moves forward, it will open up a whole new arena at which new design tools can be targeted. And, as some of the top EDA companies change their focus to becoming IP or service providers, they may position themselves out of the EDA market.

This certainly is one possible change that will take place in the industry. But there are others who would suggest that an EDA industry division between vendors providing tools suited for IP authoring, and vendors providing tools for IP evaluation and integration, is a more likely scenario; at least according to Cadence's view of the world.

On the other hand, Dataquest's Gary Smith feels that "the real hit will be taken in the semiconductor world." And, in fact, there are many who agree, arguing that while IP is often viewed as being a derivative of the EDA business, it is really a derivative of the semiconductor business.

Milan Gandhi, CEO of Indus, Santa Clara, Calif., sums it up by saying, "The EDA industry is traditionally a software development industry, but with the advent in IP work, they are moving closer to their end users (designers). It is this change that will force the EDA industry, system design houses, and the semiconductor industry into a tight relationship in order to meet the needs of future designers."

How Valuable	Circle
Highly	536
Moderately	537
Slightly	538

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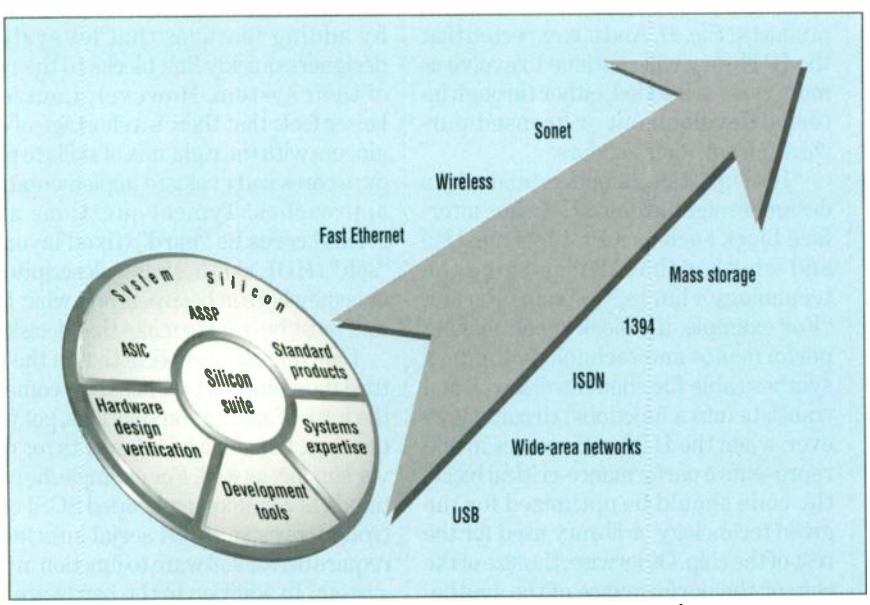
Digital ICs Editor

Predesigned Circuit Blocks Can Greatly Reduce System Design Time While Allowing System Designers To Best Use Their Expertise.

The accelerating pace of system development has forced system designers to find ways to design, verify, and test chips in record time. To accomplish that task, system engineers, circuit designers, and the companies that support them have created a groundswell of capabilities and tools in all aspects of intellectual property (IP) that relate to circuit design. In the chip-design industry, such IP often refers to blocks of circuitry that can be reused, saving time and design resources. Such blocks are offered by ASIC suppliers, created by the customer, or designed by independent companies that specialize in creating popular circuit blocks that can be sold or licensed.

To ensure that circuit blocks are reusable, many aspects of process technology, and design, test and simulation tools must come together to allow functions to be well specified. Functions must be able to migrate from one company's design system to another, and from one process generation to another. Today, it is not enough to just design a circuit and provide a netlist that can be synthesized, or to create a fully designed and laid-out function. That's especially true for complex blocks that contain tens of thousands of gates. Many of the complex functions require additional supporting information such as timing simulation models, test vectors, or even embedded test logic, to ensure that they will perform as desired in the final circuit.

The need for predesigned blocks increases as chip complexities go well beyond megagate density levels, with no letup in demand in sight over the next few years. No longer can companies afford the luxury of a two-year development cycle for complex circuits for which designers have a productivity of only few hundred verified gates per day. Predesigned blocks can raise the productivity level, allowing companies to use their system expertise to create unique functions rather than redesign commodity functions.



1. Building-block cores and standard-cell elements make up the Silicon Suite from Lucent Technologies. They're supported by systems expertise, development tools, and hardware design verification tools. Additional complex building blocks such as Fast Ethernet, USB, 1394, Sonet, and other functions also are continually being added.

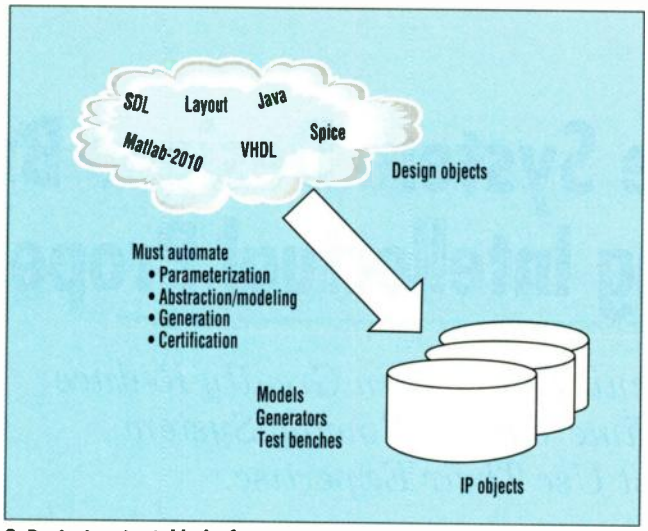
Predesigned functions also can shorten the overall design cycle by many months, potentially reducing a two-year design cycle to six months or less. This is critical as equipment market lifetimes continue to shrink in the computer and consumer markets. No longer can a manufacturer introduce a system and expect to market it for a year. Typical lifetimes are hitting less than nine months until the next upgraded model is expected. In another year or two, a six-month interval between model generations would be considered very long.

The most fundamental IP consists of the basic cell libraries offered by all of the suppliers of gate arrays, standard-cell, and even programmable-logic circuits. These libraries comprise simple elements such as gates, multiplexers, counters, and I/O cells. They're typically supplemented by logic-synthesis tools; complex, predesigned function cores

(CPUs, DSPs, MPEG decoders, 1394 and USB interfaces, PCI master and slave interfaces); and function compilers. There are many other functions, some designed internally and some developed by independent third-party companies as well.

Over the next few years, the size of cores will increase. That will place significant stress on design tools, unleashing and constraining the designer's ability to craft new functions. Industry efforts to make the cores transferable from company to company and process to process are progressing thanks to the creation of the Virtual Socket Interface Alliance—an organization formed by companies from all aspects of the semiconductor, EDA, and test industries. The VSIA is trying to guide an industry-wide effort to better define blocks of IP, and craft some standards to define the way they connect to each other and are tested (*see "The VSI Alliance: The Journey From Vision To Production," p. 86).*

Once such standards are in place, designers will have more freedom to combine IP blocks to rapidly assemble system chips. However, time-to-market demands often constrain designers by limiting how much on-chip innovation they can include due to the longer design time required for unique circuitry.



2. Designing circuit blocks for reuse requires more than just creating circuit netlists or other functional descriptions. Design objects must be encapsulated with models, test vectors, and other information.

Nothing's Perfect

Today's state of the art in core design, though, still requires some tweaking, according to Tony Parker, ASIC product line manager for Lucent Microelectronics, Allentown, Pa. His group had purchased high-level IP for inclusion in Lucent's Silicon Suite design system. The IP was supposed to shorten their entry into a new market segment. In reality, they found that it didn't save much design time because they had to tweak the design once it was implemented at the gate level. Until standards are in place, the safest route according to Kevin Kolwitz, director of ASIC libraries and design systems at Bell Laboratories, Murray Hill, N.J., is to actually run some wafers with evaluation circuits for parametric information. This information is especially critical if cells are being moved to a new process and must be regenerated using compilation tools, or in the case of older cells, compaction tools that reduce the size of the physical layout.

Lucent's Silicon Suite design approach starts with the company's collection of basic cells and IP blocks, surrounded by systems expertise and the development tools and hardware design verification tools Lucent created and purchased. Together they will be used to create various levels of system silicon—standard products, application-specific standard products, and full-custom products *(Fig. 1)*. And it is expected that the IP library will continue to evolve as more cores are added, either through internal development or licensed/purchased from other vendors.

"It's important to understand why a designer might acquire IP (a bus interface block such as a PCI bus master) and whether that IP is pushing the technology's limits," explains Parker. "For example, if a block is not pushing performance and technology limits, a synthesizable file should work well and translate into a functional circuit. However, when the HDL code comes in and represents a performance-critical block, the code should be optimized for the given technology or library used for the rest of the chip. Otherwise, the size of the chip or the performance of the synthesized blocks may not meet expectations."

With today's chips becoming tomorrow's cores, and multichip systems becoming multicore, high-integration chips, additional care must be paid to floorplanning and timing-driven layout techniques, warns Parker. System chips must be treated like the pc boards of the past, with corner-to-corner delays taken into account. Designers also must deal with both local routing in the blocks and global routing issues across the chip.

Cores must be designed for manufacturability. Insertion of scan-test logic will become a requirement rather than an option. Additionally, core logic must be encapsulated with information such as its behavioral model, timing information, and test vectors. Thus, when the core is delivered, the user has a complete description of the block from the basic functional level to the final test vectors. Even better, suppliers of cores could provide a full netlist or even functional silicon, allowing for better performance evaluation..

When cells are designed for heavy reuse, it pays to invest in documentation and encapsulation agrees Richard Lautzenheiser, director of strategic marketing, peripheral electronics at Symbios Logic, Fort Collins, Colo. However, for cells that don't have heavy reuse, alternatives to full documentation must be developed to minimize cost overheads. One challenge is to design cores for reuse by adding features that let system designers quickly link blocks to the rest of their system. However, Lautzenheiser feels that there's a shortage of engineers with the right mix of skills to produce cores and evaluate implementation approaches. Typical questions are: Should cores be "hard" (fixed layout), "soft" (HDL synthesizable description), or somewhere in between, and what factors must be used to make that decision?

Lautzenheiser expects that in the future more support will have to come in the form of application solutions, not just the core, but software elements for driver support as well. For example, he continues, at Symbios, embedded SCSI controller cores and 1394 serial interfaces require driver software to function in the system. In addition to the hardware IP, Symbios also provides software IP to simplify a system designer's task of integrating silicon into the total system.

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codesign effort that takes into account behavioral and architectural trade-offs, and both software (programmable) solutions versus hardwired solutions, explains Professor Jan Rabaey of the University of California at Berkeley. He developed a hyperspreadsheet used to perform trade-off analysis for complex DSP functions. Such a tool requires that IP blocks be very well defined so that they will behave as expected after rigorous simulations.

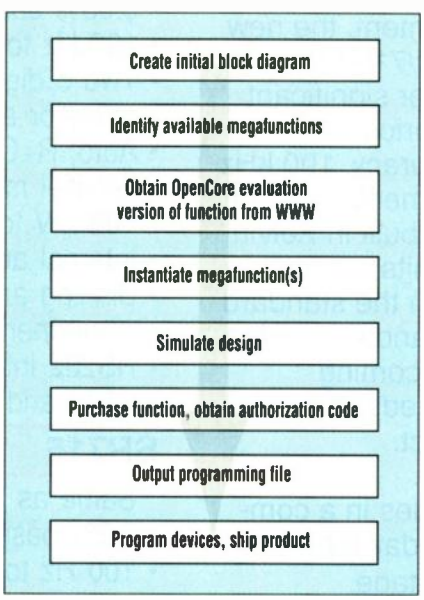
To accomplish that task, Rabaey also feels that blocks should be encapsulated. But, the encapsulation process must be automated to make it practical to do on just about every complex block. As a result, the parameterization, abstraction and modeling, generation, and certification must all be automated so that designers need only feed in a design object description of the function and receive an IP "object" for use in future designs *(Fig. 2)*.

Part of what Rabaey proposes is to separate the function of the blocks from the interblock communications required. Software tools could then provide automated interface synthesis by finding common data-transfer modes between various IP blocks. That, in a sense, raises the abstraction level of the problem and allows designers to define several levels of application programming interfaces (APIs) above the hardware interface (the electrical connections). These interfaces would be fine-grain, coarse-grain, and application APIs.

In an ASIC, just about any circuit function and any way of connecting transistors can be considered IP, and as such are subject to potential licensing and exploitation. As mentioned earlier, basic cell libraries gate-array, standard-cell, and programmable-logic vendors offer are the simplest form of IP that designers have been leveraging for the past quarter century. The same ASIC suppliers that offer basic libraries—LSI Logic, Milpitas, Calif.; Lucent Technologies; Symbios Logic; VLSI Technology, San Jose, Calif.; and many others in the U.S., Asia, and Europe—have raised the complexity of the blocks they offer. Some have designed the larger blocks themselves, while at the same time leveraging the design expertise of other companies like ARM Ltd., Cambridge, U.K.; The DSP Group, Santa Clara, Calif.; Sand Microelectronics, Santa Clara; Sican Microelectronics, South San Francisco, Calif., Virtual Chips Division of Phoenix Technology Ltd., San Jose, Calif.; and VAutomation, Nashua, N.H. to add a wider variety of complex functions to their libraries.

High-density, FPGA suppliers are a good example of the ability to leverage IP. Most such suppliers have some type of cell library and a companion list of available megafunctions that can be configured in the arrays. Some megafunctions are based on synthesizable HDL descriptions, while other performance-critical blocks such as a high-speed PCI core, are often supplied as fixed configuration patterns to ensure the desired performance.

Altera's director of product marketing, Robert Beachler explains, the design system uses an approach Altera calls OpenCore, which lets engineers "try before buying" various megafunctions. Encrypted cores can be downloaded from Altera's web site and then instantiated for compilation and simulation, allowing designers to evaluate their features and performance. If the blocks meet performance requirements, designers can purchase the function and receive an authorization code to gain access to the programming file they must include in the overall design file. Once integrated into the design file, the FPGA can be programmed and used in the system *(Fig. 3)*. Additionally, for complex functions, the company also provides after-purchase support. For PCI cores, it ships an actual board that has the programmed interface and software drivers. The support is part of Altera's megafunctions partners program (AMPP) that includes independent third-party developers. Many of AMPP cells are not directly sold by Altera; it just refers customers to AMPP clients. Some AMPP cells are available for downloading, while others are not. However, all AMPP members have access to the encryption engine if they would like to post their functions on Altera's or their own web site.



3. The OpenCore design system developed by Altera allows designers to try the desired cores before buying. Designers can download the encrypted core, instantiate it in their circuit design, and perform the circuit simulation. If it is acceptable, designers can then purchase the core, unlock the encrypted file, and add it to the programming file.

In addition to the well-known U.S. and overseas ASIC suppliers such as IBM, Endicott, N.Y.; LSI Logic; VLSI Technology; SGS-Thomson Microelectronics, Lincoln, Mass.; NEC Electronics, Santa Clara, Calif.; and Toshiba Electronics America, San Jose, Calif., large IC makers like Motorola, Tempe, Ariz.; National Semiconductor, Santa Clara, Calif.; and Texas Instruments in Dallas, are all moving to system-on-a-chip design approaches using large blocks of IP (embedded powerPC cores, DSP and x86 building blocks, and other functions). However, rather than offer a generic service to customers like the ASIC suppliers offer, they've distributed their design capability across all market segments so that each group can more readily create application-specific chips.

Such a system-chip approach is typical of what companies will require well past the turn of the millennium. But, to accomplish this, they must internally do the same things that a commercial vendor must do—design the cores for reuse. And, to do that, the large companies must define and standardize a set of design rules that will allow circuits to migrate from one product line to another.

That's not an easy task. Motorola, for example, has spent several years establishing what it calls unified design rules—a common set of layout rules and guidelines for crafting logic blocks that can then be transferred across manufacturing lines. Without such efforts, cores would be locked into a specific process line and could not be shared.

In the past, sharing was not practical because each product division typically had different design rules and incom-

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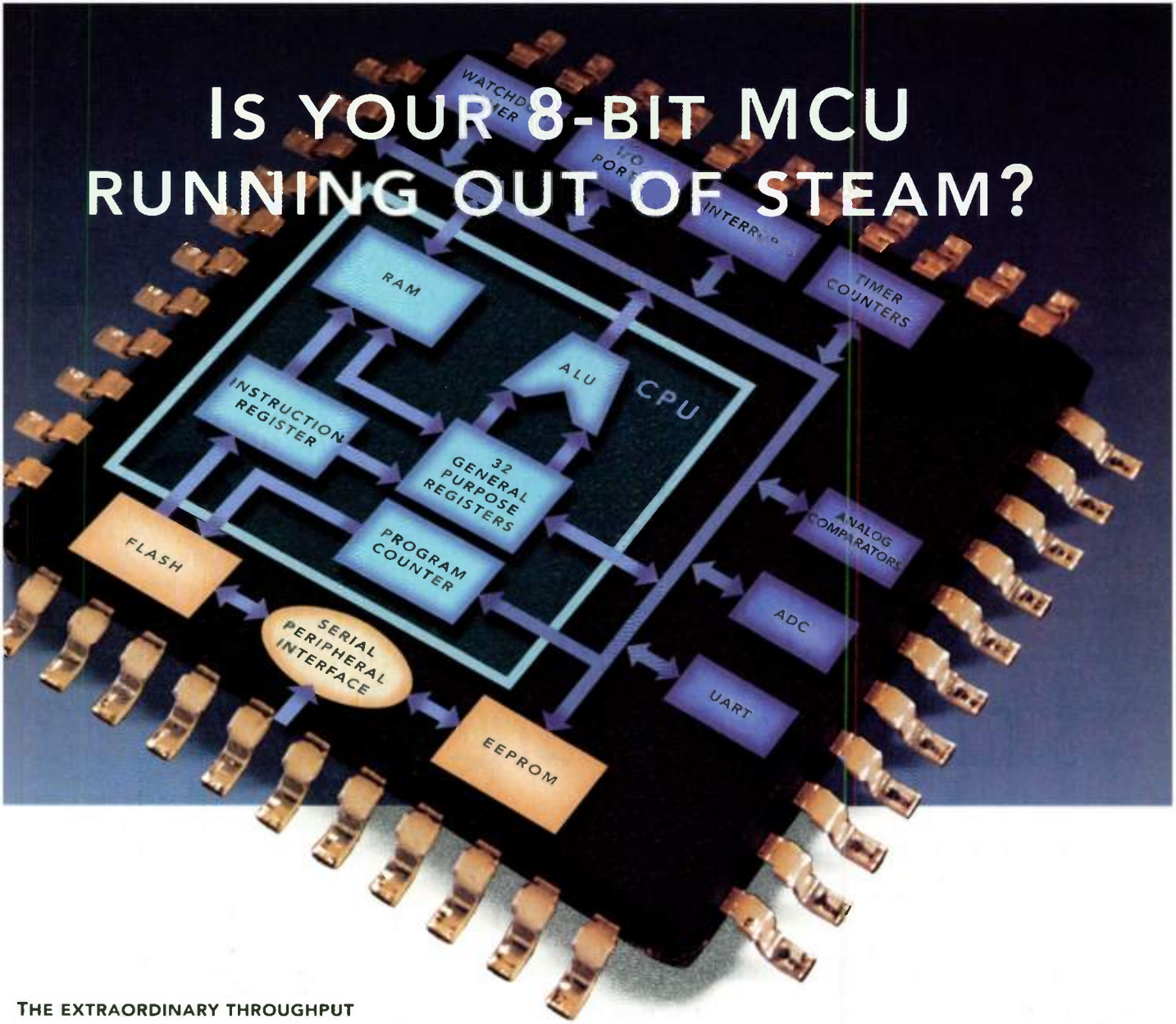

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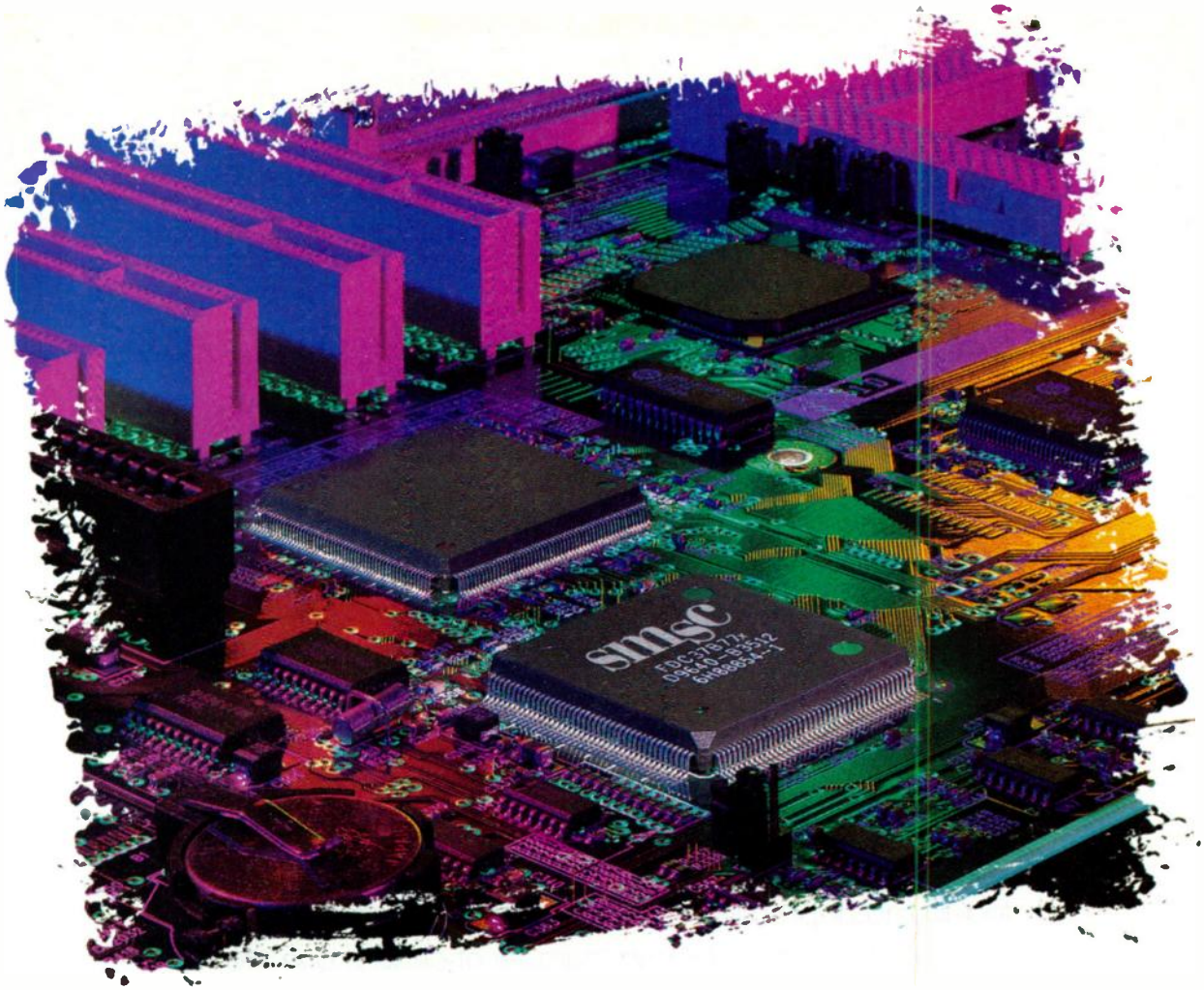
patible processes due to cost and yield requirements and targets. Although hitting those targets is still important, sharing has become a critical part of Motorola's key interests as the company reorganizes its divisions to service specific market segments, rather than offer generic product families such as microcontrollers, gate arrays, etc.

Most of the well-established independent providers of IP cores offer rigid blocks of predesigned functions. ARM, for example, licenses its 32-bit CPU megacells as "black boxes" locked to a specific manufacturer's process to ensure core performance. Sand, VAutomation, and Virtual Chips, on the other hand, offer HDL descriptions of many of the cores, allowing designers to implement the core on any technology that lets them compile the core.

In ARM's scenario, those that license the core have little leeway in modifying the logic or moving it to a new process. To overcome that restriction, designers at LSI Logic re-implemented the core as a synthesizable block. To ensure that the core would meet performance requirements of the applications, the synthesis tools are targeted for 0.25-µm design rules. The small features actually allow the core to operate at speeds faster than the initial black box version of the core.

Software and technology suppliers such as Aspec Technology and Artisan Components, both in Sunnyvale, Calif., offer fundamental building-block libraries as well as more complex functions. Aspec's Open Design Implementation Technology lets designers integrate DSP blocks, support logic, and analog functions, all on one chip while maintaining an open-tool environment. That allows firms such as National Semiconductor to select the best-in-class EDA tools to do their designs. Aspec also developed an approach called QuickPort, which allows companies to rapidly transfer design files from foundry to foundry so that they can add more sources of supply as demand for their product increases. The company builds this capability on top of its high-density family architecture of gate arrays, standard cells, and embedded arrays.

How Valuable	Circle
Highly	539
Moderately	540
Slightly	541



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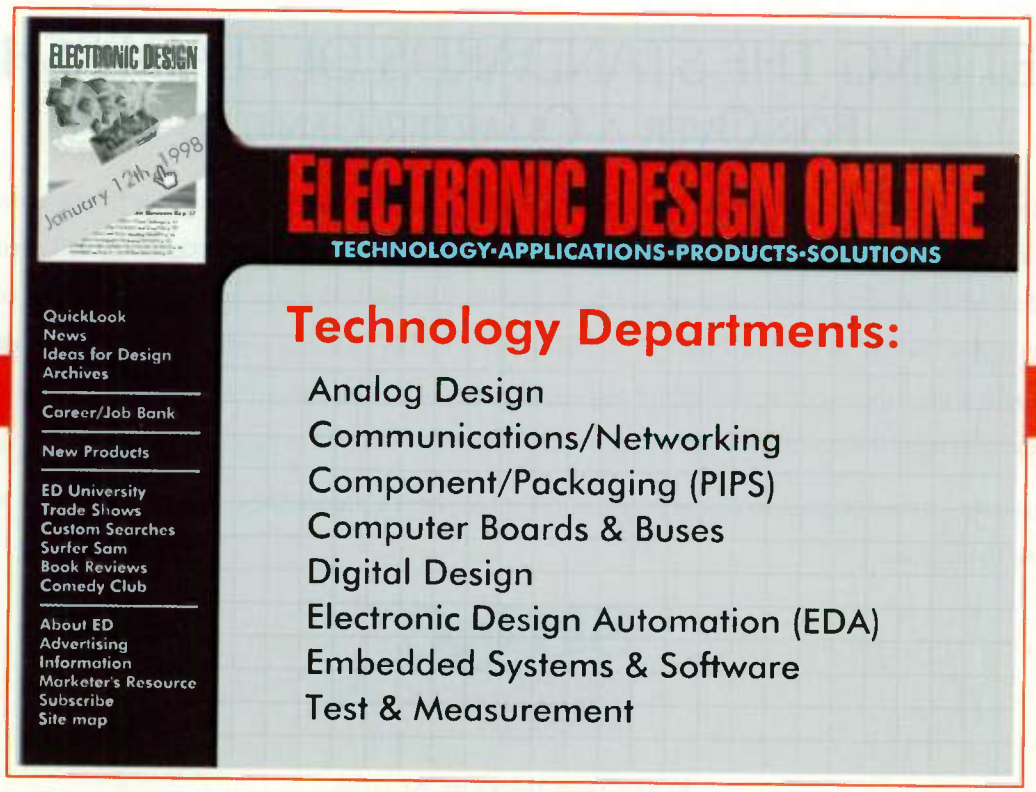

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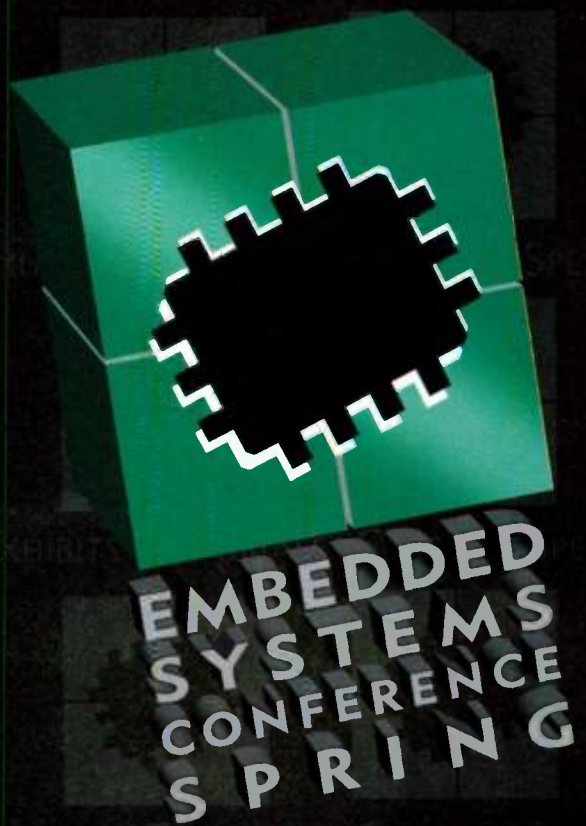

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Breaking down the major technical barriers to system-on-a-chip design was the reason the Virtual Socket Interface (VSI) Alliance formed a little more than a year ago. Since then, it has made substantial progress and impact on the industry. The alliance received its initial direction from the vision set down by its founders: Make system-on-a-chip design a practical reality by enabling the mix and match of component blocks (virtual components or VCs) from multiple sources on a single chip.

Based on that statement, the alliance defined its mission as the development and promotion of a unifying vision for the system-chip industry, and the creation of open technical standards required to allow mixing and matching of VCs (megacells, cores, compiled blocks, etc.) from multiple sources.

We have already seen major developments in the industry, which show that the VSI vision is indeed taking hold. VC startups continue to blossom, and even large, existing companies are adapting their business models to enter this fast-expanding market. Recent announcements of major IC providers creating "virtual component alliances" are another indication of the exciting developments in this space. EDA companies are adjusting their tools and flows in anticipation of the release of VSI specifications. Many are adjusting their business strategies to take advantage of the need for additional expertise in this newly developing market. Furthermore, system integrators are investing millions of dollars in making changes to their design flows and enlisting the help of service providers in accelerating their pace of development.

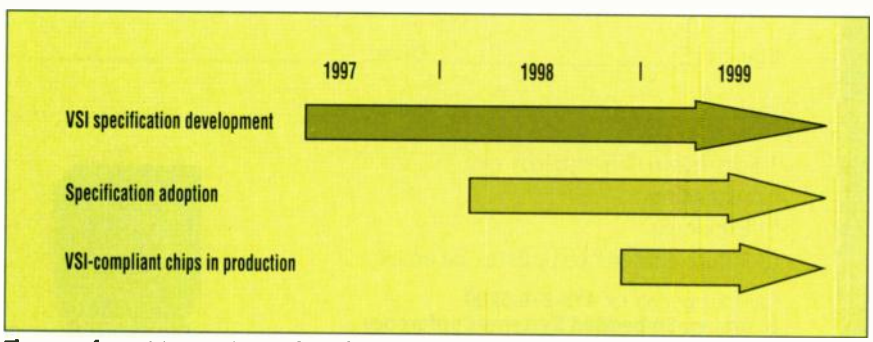
We've passed the point of inflection. Activity surrounding the development and use of VCs is increasing exponentially. It will be a challenging, but rewarding ride for those who are aggressive and pick the right strategies. Being part of the VSI Alliance provides access to information and trends essential to such strategy selection.

Year One: Develop Specifications

To achieve such lofty goals, the alliance has developed a technical plan (an architectural document) outlining its approach to mixing and matching VCs (the Virtual Socket Interface). It also has identified the technical standards needed to achieve this goal. The document describes the concept of separation of authoring and integration of VCs as the industry moves to system-on-a-chip designs. The initial version of the architectural document was released in March 1997, but since then, there have been a number of new developments and modifications. As a result, the VSI Alliance is preparing a second version for release in March 1998.

After creating the roadmap, the alliance then set up six Development Working Groups (DWGs) to address different elements of the VSI, as well as additional issues such as mixed-signal blocks, on-chip buses, and intellectual property (IP) protection. Each of the DWGs has made substantial progress. Two DWGs have released specifications for member review, while the others plan to release specifications in the first half of 1998. If they are adopted, the first VSI-compliant chips could go into production by late 1998 *(see the figure)*.

As the alliance moves into its sec-



The move from vision to VSI-compliant chips in production will require about three years. Time will be needed to define and adopt the specifications, and then produce ICs based on those specifications.

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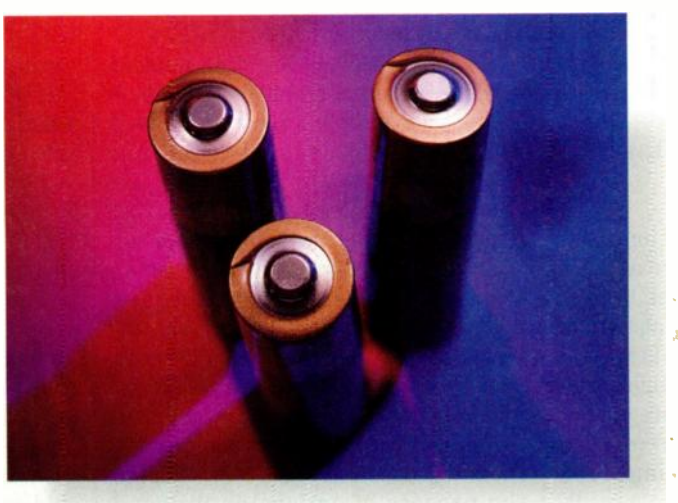

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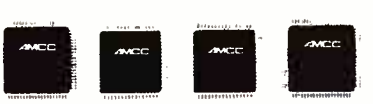

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ond year, it is adding new efforts aimed at adoption of the specifications. Additionally, the alliance will continue to accelerate its pace by further developing these specifications while the industry gears up for their adoption.

To increase the rate of adoption, the alliance will drive a number of programs. For example, in mid-1997 the organization chartered a marketing committee to take the specifications in the pipeline, and work with the DWGs to help ensure their acceptance and adoption. The marketing committee has the following goals:

- Ensure that the specifications address the user's needs
- Develop a publicity program to ensure industry-wide awareness
- Drive the pilot programs to demonstrate the efficacy and usefulness of the specifications
- Work with early adopters to assure rapid adoption and proliferation
- Develop programs for VSI Alliance members that ease the task of assimilation of the new technology

Adoption of the specifications is as major an undertaking for the alliance as it is for the industry. Each type of company will have a different kind of challenge. EDA companies will need to modify certain elements of their products to either read or generate new or modified data formats. There may, in some cases, be an additional impact on their tools and design flows as a result of aligning with the VSI focus on separation of VC authoring from system chip integration.

VC providers will need to augment their deliverables and/or modify the data formats with which they describe their components. They may need to make more substantial changes to align with standards in the areas of on-chip buses and in the area of test approaches.

System chip integrators will need to optimize their design flows around the new standards, while test equipment suppliers may need to change or optimize their software. In some cases, they will need to make hardware adjustments, to work most effectively with an assembly of VCs on a single chip.

Although each of these companies will have changes to make, the benefits will outweigh the investments required. EDA vendors will have fewer data formats to generate and support. VC providers will have their task vastly simplified because they can sell a standard VC to a wide variety of users with a higher likelihood of success. System-chip integrators will be able to simplify or even automate more of their design flows. They will see decreased design times, reduced integration expenses, and fewer design and layout bugs.

It's critical that all industry participants realize the need for adoption of VSI specifications. Companies that expect to remain competitive in the system-chip arena will have to work aggressively to apply what is available today and position themselves to use of what will come down the pipe. Many of the standards can and should be applied now, although complete adoption will likely take many months to come to reality.

Due to normal product development schedules, it is likely that specifications issued early in 1998 will not be adopted and included in fully released tools and design flows until late 1998 or 1999. Exceptions to this rule will include VSI Alliance members who have been actively participating in or monitoring DWG activity, and those who have been simultaneously aligning their internal development efforts with the direction and choices of these DWGs. This competitive advantage accorded to VSI Alliance members can provide them with as much as a year's lead in the process of understanding and adopting these specifications, resulting in significant benefits.

DWG Activity Update

The DWGs are the heart of the VSI Alliance organization. These groups of 10 to 20 people comprise volunteers whose job it is to:

- Identify the critical technical issues in their area which impact the ability to author, exchange, and mix VCs
- Survey the available solutions, both public and proprietary, that may be available to address those issues
- Identify or develop the best solution to those technical issues

The Steering Working Group defines the broad charters of the DWGs, while giving them leverage to identify and set the priorities and solutions for the most imperative issues. One of the largest DWGs is the Implementation/Verification group—it has the largest number of standards to deal with. This group's charter encompasses all the design and verification formats associated with design from RTL through physical layout. They have divided their work into three major phases, with the first phase dealing with the standards associated with "hard" VCs. This specification has been completed and is now being reviewed by the membership. The alliance expects to release this specification to the public in February.

The Phase 2 specification is already in definition. It focuses on soft VCs and addresses a number of more controversial data format options. This group is working with several existing groups to get the best possible input and eliminate any duplication of effort. These groups include the Open Verilog and VHDL International (OVI and VI) standards groups as well as the tool interoperability subgroup of the EDA Industry Council. Phase 3 work, which is scheduled to begin later this year, will deal with "firm" VC data interchange standards.

The Mixed Signal DWG is the other group that already has released its specification for member review. They have defined an extension to the original architectural document as well as a number of data format standards and design guidelines. These standards and guidelines promise to ease the problem of integrating analog blocks onto digital system chips. Because true system chips must almost always include some sort of analog blocks to allow interface to the real world, such standards and guidelines are of particular importance.

The On-Chip Bus DWG has tackled a particularly difficult problem. The group had to segment bus requirements into three different performance ranges. These include a high-speed processor bus (including connections to memory), a system bus, and a peripheral bus. The processor bus in most designs was most likely to be very specific to the processor and not a high priority for standardization. The system and peripheral buses are the ones likely to connect to the broadest range of VCs and are deemed to have the highest need and priority for standardization.

This segmentation left the team

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with a plethora of possible alternatives. They listened to presentations from companies who promoted the adoption of their buses as the standards. Many of these buses had more similarities than differences, which led the group to think about some sort of higher-level standard that might be more flexible and meet more requirements than a single specific bus selection.

The DWG chose to first identify the attributes required for any on-chip bus standard. The team will publish this first set of attributes to the VSI Alliance membership in the first quarter of this year. Simultaneously, the group is working to see if a transaction-level protocol would be more appropriate than a single specific bus. VC suppliers would design their components to interface to this transaction-level standard, while users would design a simple and standard "wrapper" or interface. This wrapper would connect their specific bus to the transaction-level standard. Essentially, component suppliers could define components which would interface to a wide range of buses, while system-chip integrators could use a variety of buses.

Representation

The VSI Alliance is the most diverse organization of its kind, represented by EDA, semiconductor, virtual component, system, test equipment, and design service companies. While this diversity is one of VSI's major strengths, it also can be a challenge when the goal is to establish standards in the system-chip test area. Each type of company brings a different, though not necessarily conflicting, perspective. Developing a common terminology and consistent objectives were the first necessary steps for the Manufacturing and Test DWG. Outlining the challenges from each perspective was the next task. Then came prioritizing the tasks and getting people behind a common plan.

Now this group is specifying appropriate solutions. It has articulated eight key problem areas that must be solved and has agreed on specification development in three areas: test-interchange formats, VC-authoring guidelines, and VC-integration guidelines. The initial focus will be on the first two specifications. Close cooperation with related IEEE standards efforts also are in progress.

Protecting intellectual property (IP) is a broad and complex topic. There are, of course, legal protections (contracts, NDAs, etc.) and technical protection mechanisms (e.g. encryption). The IP DWG is addressing only the question of technical protection, although legal protection is clearly an important tool which each company must evaluate with the help of legal council.

On the technical side, there is the fundamental trade-off between protection and ease of use. A vendor may want to completely protect his IP and not allow the end user or designer to view it in any kind of usable form. The customer, on the other hand, may have a legitimate desire or need to view or modify the source data, especially to identify and resolve problems. As a result, the DWG is examining a layered approach to describe various levels of protection, allowing vendors and users to strike the right balance between protection and usability. Expect to see initial results from this group available for VSIA member review in the second quarter of this year.

The System-Level Design DWG has been the most challenging of VSI's standard-setting group efforts. Our industry's terminology and evolution of tools here is significantly behind that of the other areas. Like the Test DWG, this group spent a significant amount of its early efforts defining terminology and sharing and aligning different views on design representations, priority of problems, etc.

One area in which this DWG has decided not to invest effort is the development of any kind of new system-level design language. This effort is a long-term one, which is not in sync with VSI's more practical and short-term focus. Users should expect the first output of this group to deal with common terminology and a classification of different levels of model abstraction. The first real specification will focus on processor model standardization, including data formats, tool interfaces, and standard libraries. Most of these results should be available for member review in the second quarter of this year.

Pilot Project Goals

To achieve the objective of being able to mix and match VCs, the VSI Alliance recognized the importance of pilot projects to exercise, test, and validate the specifications and methodologies. Working with industry to prove the VSI specification formats and methodologies is an important phase in the development of efficient standards. Pilot projects can help advance technology, validate or prove VSI standards, suggest specification architecture and detail enhancements, and encourage the adoption of the VSI specifications. Accelerating the ease of design reuse is an important benefit for the company doing the pilot activity. Useful feedback complements the VSI Alliance's efforts to meet industry challenges and needs.

VSIA pilots have been defined as an independent or collaborative exercise of one or more of the VSI interface formats or design practices in any of the following activities:

- Design (authoring) of a VC block
- Mixing and matching of VCs
- Integration of a soft, firm, or hard VC block
- Design verification or testing of integrated VCs
- Design tool interoperability using VSI standard formats
- Verification of VSI specification

Pilots can be suggested by any interested party, and executed individually or collaboratively by one or more companies. A company may choose to include proprietary content in its planning and feedback to VSI, but is not required to do so. The company also may choose to work with the alliance to publicize the pilot effort and its results.

The following is a sample of the information which would be valuable to the alliance. Actual information to be provided can be some, all, or more than the following:

Pre-Pilot Information:
- Company(s) engaging in pilot
- Intent of pilot
- Scope of pilot
- Expected value to pilot participants
- Success criteria
- VSI specifications used/impacted
- Timeline

Post-Pilot Feedback
- Flow/methodology
- Level of success
- Obstacles and challenges

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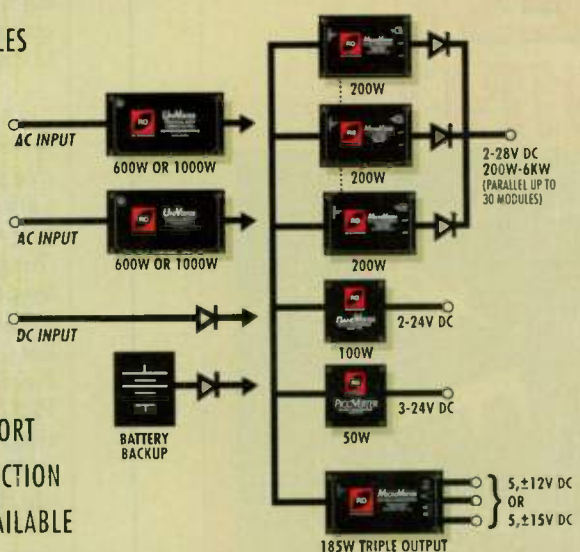

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READER SERVICE 219

- Recommended changes
- Ranking of suggested changes (minor, major, cosmetic)
- VSI specification actually affected
- Actual time

The VSIA has developed a short document that provides guidelines and basic information for those considering a pilot effort. It's available on the VSI web site at *http://www.vsi.org*. Additionally, VSI has in place a Pilot Committee to promote, encourage and assist pilots by providing definition, feedback criteria, procedures, and a point of contact for pilot activities.

In some cases, a pilot may be run at the request of a specific VSI DWG. Then, the appropriate DWG works closely with the pilot company to help define the pilot feedback which would be the most useful. The DWG also evaluates the results and modifies the relevant specification, if needed. The impact of the pilot effort on the specification would be shared with the pilot company. In this way, a pilot effort can have a tangible effect upon the VSI standards for design reuse. Other, less specific, pilot efforts are encouraged and the alliance will work with the pilot company to outline the feedback requirements of VSI and to provide value to the company engaging in a VSI pilot.

Douglas Fairbairn is currently the president of the VSI Alliance and the vice president of strategic programs at Cadence. Prior to his alliance duties, he was the general manager of the Alta Group of Cadence, focusing on system-level design solutions for wireless, multimedia, and network hardware markets. Before joining Cadence Mr. Fairbairn also was a co-founder of both VLSI Technology Inc. and Redwood Design Automation (now part of Cadence).

Diana Anderson is corporate strategy director at Cadence and heads up the VSI committee for pilot programs. Having worked in the EDA business for 20 years, Ms. Anderson's broad experience is applied to solving technical and business issues related to virtual component authoring and integration.

How Valuable	Circle
Highly	533
Moderately	534
Slightly	535

Defining Where IP Fits In Future Communications Design

Despite Its Growing Pains, Intellectual Property Will Play A Key Part In Developing The System Chips To Power Tomorrow's Communications Products.

TONY PARKER
Lucent Technologies Microelectronics Group, 555 Union Blvd., Allentown, PA 18103; (800) 372-2447.

Intellectual Property (IP) is a hot subject in the communications industry. Today, technology developers are winning the productivity race with new technologies that add significant integration capacity on chips faster than designers can exploit the capability. And new competitive pressures for rapid time-to-market and the promise of systems-on-a-chip increase the need for cost-effective solutions. IP—in the form of ASIC blocks variously called cores or macrocells—provides the building blocks to help make system-level silicon a practical reality, and allow designers to keep pace with rapidly advancing semiconductor technologies.

The allure of IP is inviting—predefined high-level functional blocks that can be combined into integrated circuits (ICs) that yield great functionality and value. Companies can combine standard functions and custom logic to create a differentiated solution. What's more, properly designed IP is reusable, providing a path to the future with new technologies and new capabilities. The benefit is clear—reduced time-to-market through faster design cycles, minimized risk through the use of proven designs and ASIC methodologies, and cost-effective solutions through highly integrated chips.

The System Is The Chip

Shown is one possible system-level integration for a GSM cellular handset *(Fig. 1)*. Today's cellular phones have several ICs. New process technologies and the increased availability of cores will allow them to be combined into a single baseband engine that combines memory, digital signal processing (DSP), microcontroller, voiceband and baseband codecs, and custom logic (for product differentiation) into a single chip. The resulting "superchip" will allow reduced size, weight, cost, and power consumption. From the consumer's viewpoint, the phone will allow greater capabilities in function and convenience. What's more, 1.8-V operation will extend standby battery life to perhaps 500 hours.

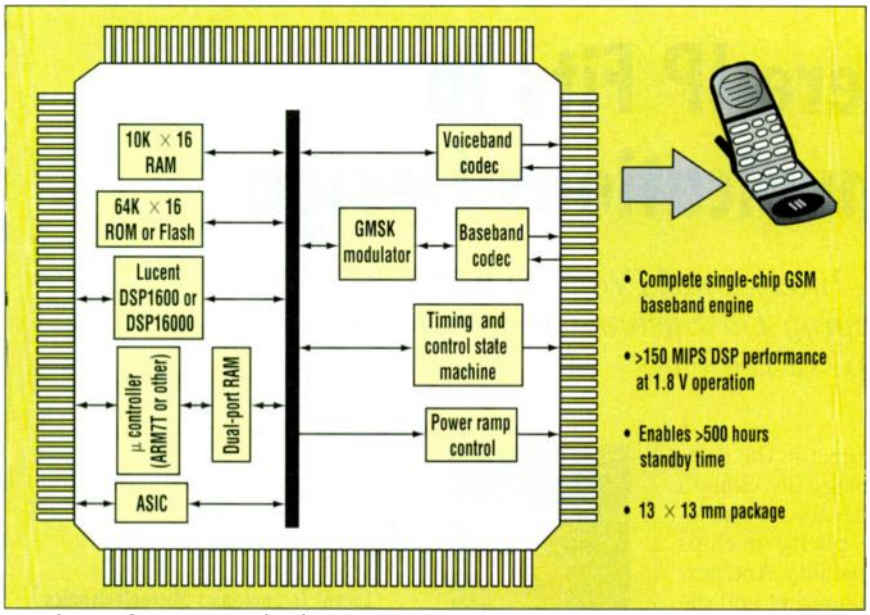
The system-level GSM example is not a reality yet. But, it certainly points to the potential that IP can play in increasing functionality, reducing size, and providing more "bang for the buck."

Interest in IP is driven, in part, by semiconductor processing technologies and their ability to achieve higher levels of integration (and higher operating frequencies). Most major IC vendors are now moving from 0.35-µm fabrication processes to 0.25-µm processes, with 0.18-µm technologies on tap for the turn of the century. In conjunction with this possibility is the reduced operating voltages. Lower operating voltages are critical to increased integration because of performance and power concerns.

At reduced voltages and process geometries, technology developers can design smaller transistors with thinner gate oxides that can be switched at faster speeds and lower power. For digital circuitry, power is estimated as the product of toggle frequency, capacitance load and operating voltage squared ($P = fCV^2$). Because the voltage is squared, reducing voltage has the most significant impact on lowering total chip power. However, life gets more complicated with analog circuitry. In fact, just reducing the voltage and geometry has little effect on lowering power or size for analog circuitry.

This realization has many analog designers looking at new and innovative ways to tackle this issue. One of the most talked-about approaches is the use of DSP techniques that leverage the digital benefits. An example of an area that is experimenting with DSP techniques is Ethernet transceivers, devices used in most wired LANs. At 10 Mbits/s, the preferred approach is analog, which offers the best area, power, and performance. As complexity and performance increase at 100 Mbits/s, the use of DSP techniques are being considered, but it appears that analog techniques still offer the best solution, even if you consider a 0.25-µm approach.

As you look ahead to gigabit applications, however, the complexity of the analog algorithms increase to the point that a predominately DSP hybrid approach may be the best solution to achieve a manufacturable product. Using DSP techniques to replace such functions as the



1. In the near future, system-level integration of a collection of pre-verified functional cores could allow the implementation of a GSM cellular handset's entire baseband section on a single chip.

receive equalizer, timing recovery, filters, and AGC blocks makes sense, but high-speed analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and line drivers will still be needed to provide an interface to the outside world.

Make, Buy, or Partner?

IP comes from three main sources: independent third-party providers, semiconductor houses, and OEMs who develop their own IP embedded in ASICs. Following are some questions that should be considered when making the make, buy, or partner decision:

- *Strategic importance to my company.* Is the macrocell a cornerstone to future products ?
- *Complexity of design being acquired.* How difficult is the macrocell to design and develop? Is the solution pushing technology limits?
- *Risk assessment.* Is the IP core a proven design? Or is it a new design?
- Understanding of the resources and skills required?
- Understanding of a product's market and application?
- Understanding of who is responsible if the chip doesn't work? What if the design misses chip performance or area targets?
- *Understanding of IP legal issues up-front.* Patent infringement? Indemnification? Ownership?
- Compatibility and product design methodology?
- Design for manufacturability?

If the company believes the IP is strategic, nine times out of ten, they will develop it themselves. The exception might be if they lack application (new market) or technical (mixed signal design) expertise, and possibly resources. Partnering is then normally pursued, but it is important to define the roles up-front and contractually capture deliverables and product rights. The importance of partnering is becoming more pervasive as the size and complexity of communication superchip increase. The question becomes: who do I partner with?

The use of third-party suppliers is often limited to simple complexity or more complex new market entry functions that may preceded standards like Gigabit MACs. Most third-party vendors work at the functional behavioral level and provide RTL descriptions with embedded test benches. This allows for easy transfer to potential customers using an ASIC methodology. However, this is just the beginning of the design process.

The importance of partnering is becoming more pervasive as the size and complexity of communication superchips increases.

Those who are familiar with coding HDL or VHDL know that the quality of the scripts can greatly impact the efficiency of the gate-level implementation and performance that the devices can achieve. Until you have actual;ly synthesized the design into its component gates, you won't know if critical paths are being met.

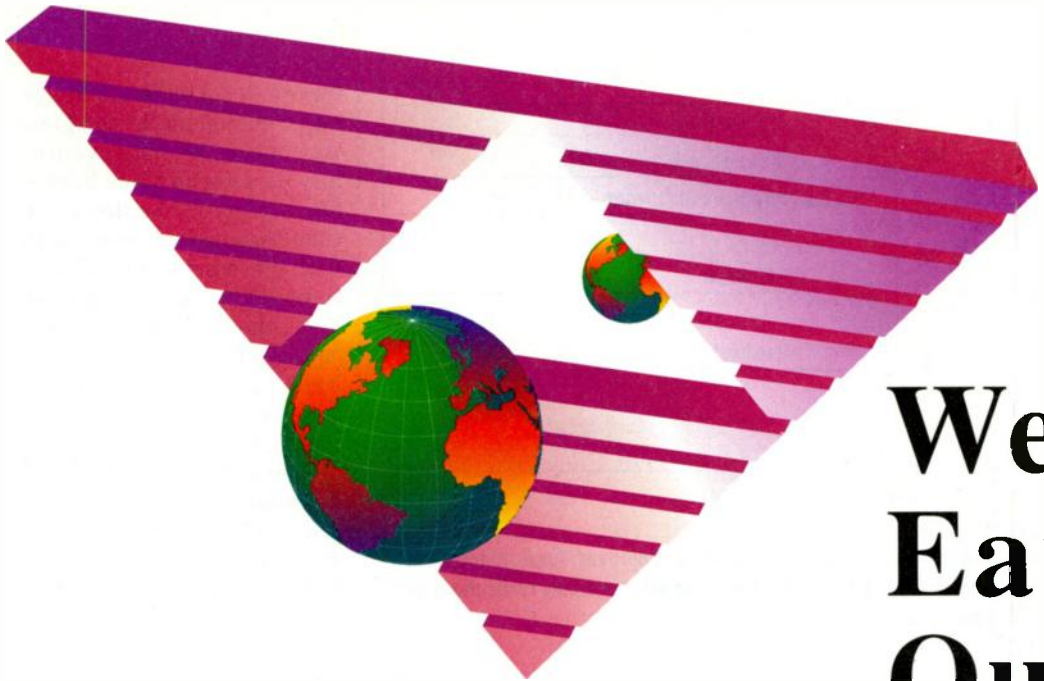
In the long run, however, it is the chip vendor who becomes central to successful use of IP. The chip vendor wants and needs you, the designer, to succeed. In order for them to be successful, you have to achieve production with a robust working chip. IP provided by the chip vendor who is capable of system-level integration is typically fully tested at speed and optimized for their libraries.

The deliverables include a complete set of test vectors; kit parts are often provided for system validation. But, the chip supplier is only as good as their understanding of your application. The best suppliers of IP tend to be those companies who also market standard products in the communication market and offer exceptional ASIC capability.

IP: The Fast Track to Standards

The communications industry is standards driven and IP can help accelerate the adoption of standards. Standards-based IP can be more readily brought to market and thereby achieve wider acceptance faster. This is typically done by offering pre-standard silicon that enables systems to be developed that test the effectiveness of the standard in satisfying the end customer needs. An important aspect of this approach is to be able to quickly modify the chip as the final standard evolves. The top-down ASIC design methodology lends itself to this circumstance very well.

System-level chips will often be heavily dependent on standards-based cores. An integrated 10/100 Ethernet NIC card consists of a handful of cores for the transceiver, MAC,



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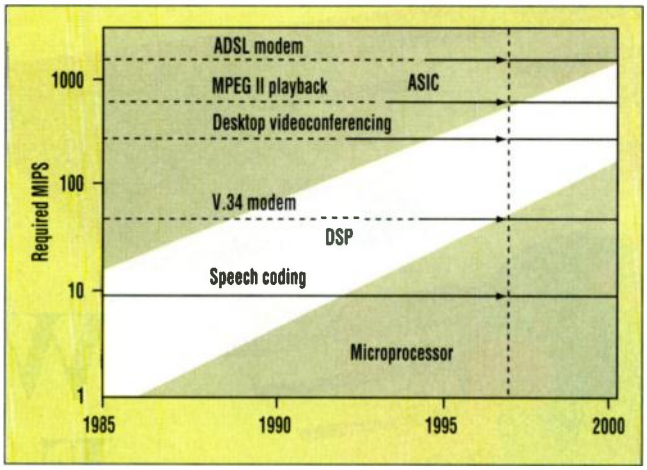
FIFO, memory, and host bus interface. There is minimal differentiation beyond the memory management and bus interface. At the same time, it is possible to create a design that requires only minimal to track a changing market. For example, one can easily substitute different host interface cores as the application moves, from a PCI interface to a CardBus interface.

An ATM ASIC, because of the complexity of ATM, may have only a single core and little custom logic. Many semiconductor houses today use ASIC methodologies to design most standard products anticipating the need to later support the design as an ASIC core. If not for the market, then for themselves. Today's standard products are tomorrow's cores, so why not design them as cores in the first place? By designing standard functions as macrocells, it will be easier in the future to migrate designs to new process technologies, lower voltages, and so forth. This fosters reuse through a clear roadmap to new technologies and lower costs.



2. Applications migrate as technology improves. Applications move from dedicated hardware to DSPs to software-only realizations on a general-purpose microprocessor.

Product Differentiation Issues

Application expertise becomes important to the partnership. How well does the IP provider understand the application? In addition, application expertise goes beyond an understanding of the standards themselves to a system-level view. A transceiver, for example, must accommodate both interaction with other subcircuits and the vagaries of real-world cabling, including suboptimal installation, cable impairments, noise, and so forth. Without a deep understanding of the application, a supplier can produce a core that, while meeting specifications, does not have the additional tolerances to provide truly robust performance in the real world.

Application expertise also fosters interoperability. Early versions of even standards-based products often show interoperability problems between equipment from different vendors. Core-based designs will lessen the minor incompatibilities by providing better-defined and better-tested functions that can be enhanced or modified quickly. At the same time, a system-level view promotes product differentiation.

While standards promote interoperability from the interface viewpoint, there is still plenty of room for differentiation in switching engines, backplane designs, and other areas concerned with both hardware and software. The availability of standards-based cores, in fact, may free designers to spend more time with product differentiation. Macros must integrate gracefully with proprietary and custom logic.

Analog Challenges

While the idea of block-level designs that translate easily to the gate level and to layout is appealing, there remains the problem of adding different processes to a chip. Building an all-digital CMOS chip is one thing. It is another matter however, to integrate digital CMOS, precision analog, memory (SRAM, DRAM, and flash), DSPs, and high-frequency biCMOS. Some cores must be hardwired to maintain performance. Analog and mixed-signal cores are very sensitive to layout, and changes can significantly affect performance. Still, such integration is essential to large, system-level chips. One approach is a modular process using a base digital CMOS with add-on modules.

Higher complexity in the chip requires much more cooperation between the involved parties. This includes developing things like common system-level understandings and common methodologies. As such, cores may eventually be seen as black boxes. On one level, the designer then becomes concerned only with the interface of the block to other logic. At a higher level, the designer will see a collection of macros and become interested only at the chip level.

Just as HDL allows a higher level of abstraction in defining a chip, so will cores allow a higher level of abstraction. One possible danger in this trend is that working at a higher level causes one to lose insight into the device. The risk of IP is that the consumer of ASICs get further away from the architecture that lies at the heart of the product. That said, IP still can simplify design. System-level designs require high-end methodologies, including behavioral simulation, chip floorplanning, and timing-driven layout. Since these tools increasingly work at a higher level of abstraction, IP becomes defined in software. Keeping in mind some of the concerns discussed above about the need to tune IP for a given process, one can still envision IP becoming a shopping list: "I want 12 10/100 Ethernet ports, a gigabit uplink, and SNMP management."

A Foundation For The Future

Whatever the approach to core development, the goal is the same: creating system-level chips which will lower costs and allow greater functionality per unit area. This may translate into a smaller, lighter, cell-phone, a more powerful network switch, or a low-cost, high-value PC.

The possibilities of IP and system-level integration lie in helping us realize the communications potentials already envisioned. As the PC becomes both a computer and a communication device, we will see a shift in basic I/O as a highly integrated superchip handles more of the functions by integrating serial buses and network access. Today's serial and parallel ports will be replaced by Universal Serial Bus (USB) and IEEE 1394 "Firewire" as low-speed and high-speed buses will serve every communication need from

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on-line access to desktop telephony. The move will distribute the intelligence among the host computer and peripherals. On one hand, devices will increasingly be closed boxes, providing less flexibility and fewer headaches for the user. On the other hand, these same boxes will be more powerful, more intelligent, and easier to use and configure.

As the power of RISC cores and DSP cores continues to increase, functions will migrate from hardware to software. As communication speeds increase, the signal processing algorithms are ever more complex. Applications migrate as technology improves: from dedicated hardware to DSPs to software-only on a general-purpose microprocessor *(Fig. 2)*.

Many observers see the key to communications as one of bandwidth. But, put in another way, it is providing low-cost bandwidth, and is driving down costs to make implementation practical and available to the widest base of users. High-speed access to the home, for example, is possible, but not yet economically attractive on a widespread basis.

IP Breeds New Methodologies

To realize these benefits, we will need new technologies to handle the complexities and reduce design time. Designs must be modeled at the behavioral level for high-level simulation. Gate-level verification has compute times too lengthy for practical application across the board. Even with well-behaved cores, high-level verification is required. Co-simulation at the behavioral level and gate level allows partners to proceed in parallel on a design. Co-simulation has often been hampered by incompatibilities when one company used VHDL and another used Verilog. New tools bridge the gap between the two HDLs and allow simulation at a very high level of abstraction.

Static-timing analysis is a must for timing verification. Full chip simulation at the gate level with back-annotated delays can take a significant amount of analysis time. A more efficient approach is to use static-timing analysis to debug all the circuit performance before running a final simulation.There are specific circuit-design techniques that make it easier to use static-timing tools. The key element is proper control of the clock structure to minimize the number of clock nets and clocking interfaces.

An HDL-based, synchronous clocking-structure approach maximizes the likelihood of being compatible to using scan- and static-timing techniques. To get the most benefit from these tools, a structured clocking scheme is required. When performing system-on-a-chip integration, not only is it essential that the custom logic conform to this approach, it also is imperative that any macrocells being used are compatible with scan and static timing. In addition, these are critical checklist items that macrocells must support. Without supporting scan and static timing, the development process will become unwieldy.

A difficult task is to verify whether a block or section of circuitry conforms to synchronous techniques. There is a need for design automation tools that can critique a database to gauge its compatibility with these methods and perform a host of circuit connectivity checks that can identify areas that may violate synchronous design techniques. This can help minimize circuit style issues from propagating downstream in the process.

Systems-On-A-Chip Today!

IP will drive system-level silicon. But to exploit the many advantages of the system-on-a-chip, you will need to carefully gauge your needs, the capabilities of your supplier, and the availability of cores. Whether you are growing your own core library or taking advantage of the ever-growing portfolios, understand that integrating complex cores into working silicon is still a nontrivial task that requires new tools and close relationship with suppliers. IP cores are not yet Lego blocks, but they are powerful ways to reduce costs, improve performance, and shorten your time-to-market.

Tony Parker is ASIC Product Line Manager at Lucent Technologies, Allentown, PA. He holds a BSEE from Bradley University, Periora, Ill.

How Valuable	Circle
Highly	545
Moderately	546
Slightly	547

JOHN NOVELLINO

IP Integrators Seek Solutions For Test Access And Bandwidth

Managing Editor
Special Projects

Successful Implementation Of New Test Techniques Will Determine How Quickly IP Cores Enter The Mainstream And Allow System-Chip Development.

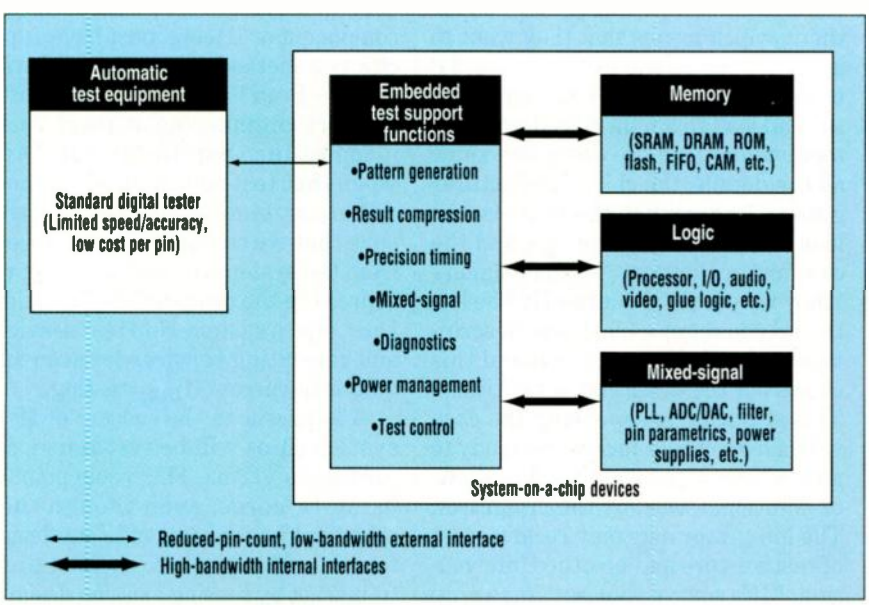
Core-based ICs that use purchased intellectual property (IP) and constitute entire systems-on-a-chip are the wave of the future. There isn't much doubt about that. The question is how fast will these massive, highly complex ICs sweep the industry. The answer, as is often the case in technology sea changes, depends a lot on how fast design and test engineers can create suitable ways to test the chips.

Major issues in the pipeline that still have no definitive solutions include how to access the individual cores within a complex chip, how to isolate the cores when necessary, and how to ensure compatible data exchanges when multiple vendors are involved. There's no shortage of test methods. But which test methods are best for specific cores in specific ICs? Compounding the problem is the fact that the cores will have many more pins than are needed or economically feasible for the overall IC.

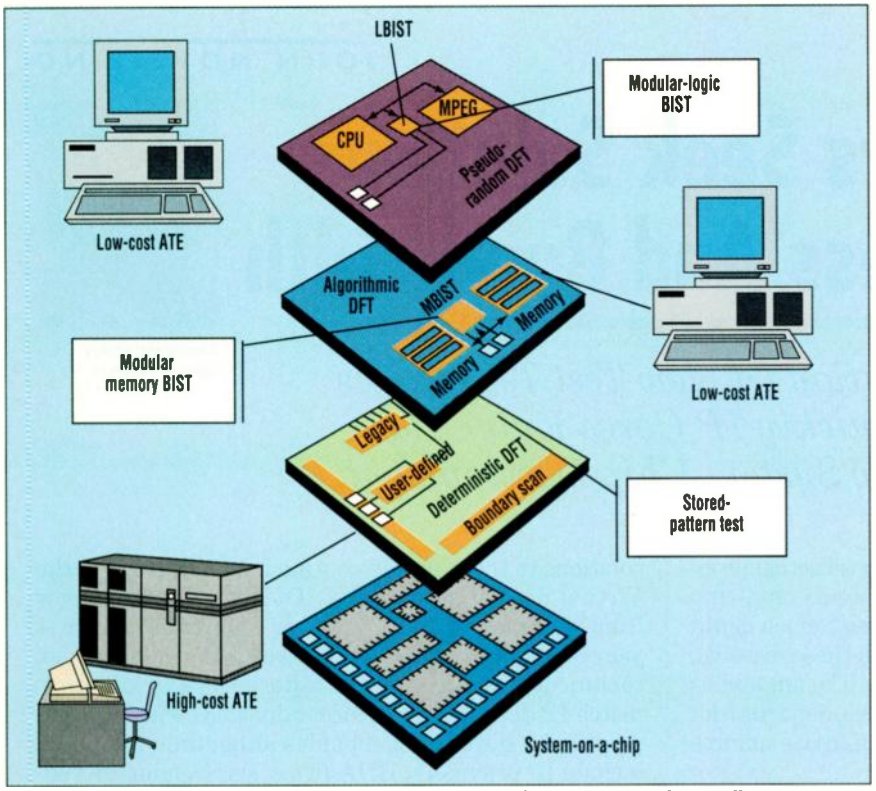
Fortunately, there are people who are working on solutions to these problems. One industry group is the Virtual Socket Interface (VSI) Alliance, which grew from 35 to more than 150 member companies in its first year of operation. The VSI alliance is developing open technical standards to allow designers to mix-and-match IP designed by different divisions within a company or by different companies altogether. Members include IP providers, EDA firms, semiconductor vendors, and system companies.

Among the alliance's six development working groups is the Manufacturing-Related Test DWG, chaired by Rudy Garcia, strategic products marketing manager at Schlumberger's ATE Division, San Jose, Calif. Garcia prefers the term "virtual components" because it is more specific than IP and stresses the analogy to real components on pc boards. A number of companies are already using their own macros or cores on new chips, having created their own test methods and infrastructure, he notes. "But when you open it up to a world where you have multiple companies offering virtual components and multiple companies purchasing and integrating them, without standardizing how to do that you would have chaos," he explains. Standardized tests, therefore, will be an enabling technology if system chips are to succeed.

As things stand now, one core provider may give an integrator test vectors in Verilog, another vectors for a Trillium machine, and a third vectors for a Teradyne tester. And the integrator might have his own format for in-house cores, explains Garcia. "We need to define a format to exchange data so that neither the virtual-component provider nor the system integrator has to spend their lives converting from one format to another and possibly introducing errors in the



1. One problem in the testing of complex system ICs is that future cores will have more inputs and outputs than there are I/O pins on the chip. This design would eliminate the use of multiplexing to access the cores' I/O pins at the chip boundary.



2. Mentor Graphics believes that for some time into the future, system chips will require a modular test approach with several types of tests available in order to completely test the digital portions of the IC.

process," he says.

It's important to note that the alliance is trying to identify suitable existing standards rather than invent its own, according to Larry Rosenberg, chairman of the VSI technical committee and a consultant coordinating all the VSI activities for Cadence Design Systems, San Jose, Calif. "We don't want to become a standards body," says Rosenberg. "We want to define what the problems that need to be solved are and, from what's out there, to identify good solutions for them. Where the solutions aren't quite perfect we want to work with the bodies that have created them to improve them to meet the needs of our constituent companies."

A useful comparison is a system-on-a-chip using IP cores versus a system-on-a-pc-board using discrete ICs, according to Rob Aitken, research and development project manager at Hewlett-Packard's IC Business Division. When you buy chips from a vendor, they've been tested and you can be pretty sure they work he explains. "When you get an IP design, you really don't have a clue because you have to manufacture it," he says, "So it has to be tested completely."

IP Owners Keeping Secrets

One roadblock to those tests is that the owners of the IP blocks typically want to maintain some protection for them, which means that they want to keep access to the details of an IP block to a minimum. That security issue can lead to a multitiered arrangement where the core designers know all the details, the chip manufacturer gets to know what the transistors look like and where they go, and the core integrators or system designers know very little about the IP. The latter may just get a black box description: put this in on one end and this comes out the other end, says Aitken. This situation is especially the case with a hard core, which is one ready to go to silicon without any modifications or additional work by the integrator. The integrator may only receive a set of test vectors and no other information. "It's sort of like getting a chip with a test program and the vendor saying, 'Here's all you need,'" he says, "Except that it's lacking the access to get that test applied."

One solution to the test problem has been the use of multiplexers on the core fed directly to the chip's I/O pins. This design essentially creates a mode where the chip's boundary is the same as the core boundary. That technique faces major technical hurdles in the future, says Aitken. First, the number of cores used on a chip is increasing and the amount of multiplexing is becoming unmanageable. Second, core complexity is rising dramatically, so that cores will have more pins than the chip does, and the integrator will not be able to bring them out to the chip boundary. Also, timing issues arise due to the length of path delays.

"I think it's becoming increasingly obvious that this business of multiplexing signals onto the pins just isn't going to work with any significant number of cores, especially with hierarchical cores, where you buy a core from somebody and it contains a core from somebody else," says Aitken. "So what people are looking to now is some kind of scan-based approach, similar to boundary scan. That's what various standards groups are looking into," he says *(see "Test access proposal for core-based ICs," page 102).*

Hard cores, which are gradually being replaced by soft cores that can be modified by integrators, will be around for some time. And because they must be testable after manufacture in a system chip, each virtual component or IP core must have a specific test methodology associated with it, notes Prab Varma, vice president of product engineering at Duet Technologies Inc., San Jose, Calif. "And when that test component is embedded in a system chip, we need to make sure that we can provide test access from the system-chip ports or test resources to the components," he adds. Duet offers system-chip test services and consulting services for scan and quiescent current (I_{DDQ}) testing.

A key issue in the success of IP in system chips will be test reuse, according to Varma. The whole point of using IP cores, even though they might not be the most efficient design for a specific chip, is to shorten time-to-market by reusing existing designs. Without test reuse, much of that time-to-market savings will be dissipated. So core designers and integrators

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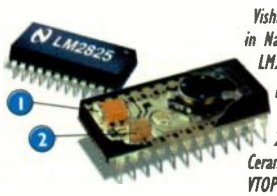

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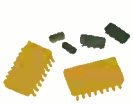

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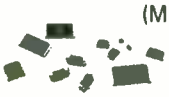

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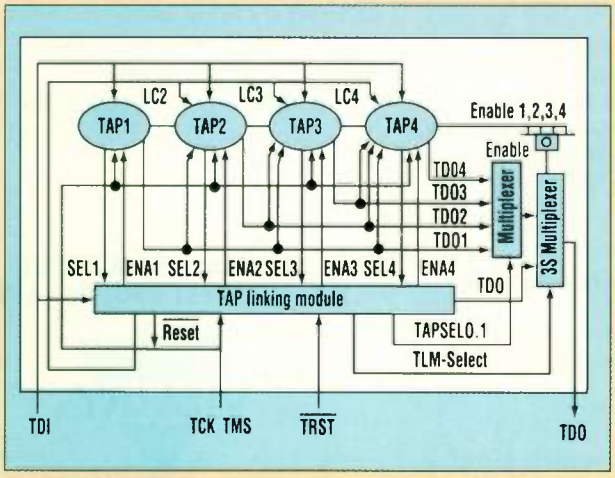
Test Access Proposal For Core-Based ICs

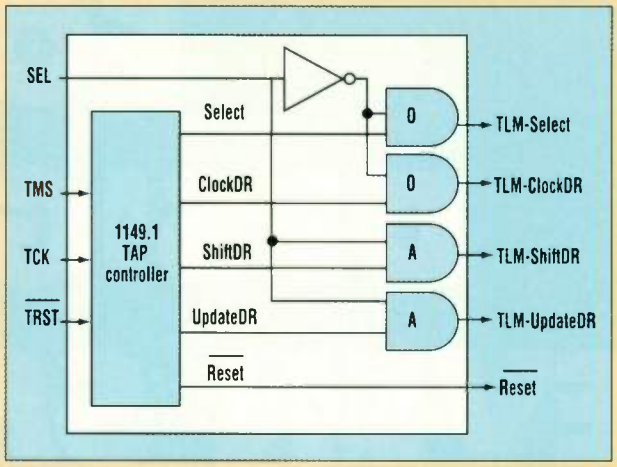
Several efforts are underway to develop methods to access IP cores so they can be quickly and economically tested when designed into complex ICs. One architecture developed by Texas Instruments (TI), Dallas, Tex., allows cores with or without IEEE-1149.1 test-access ports (TAPs) to be accessed either individually or in selected groups for testing via the IEEE-1149.1 test bus. The technique was described by Lee Whetsel in a paper entitled "An IEEE-1149.1-based test access architecture for ICs with embedded cores," presented at the International Test Conference recently in Washington, D.C. TI has submitted the approach to the IEEE-P1500 Core Test Access standards working group for technical review.

A typical, complex, core-based IC may include a TAP designed to supply access to one or more non-TAP cores and several TAPs designed into cores. A problem then, in gaining test access to IP cores is translating the multitude of pins from the cores to the relatively few pins of the IC. A key element of TI's proposed architecture, therefore, is a TAP linking module (TLM) located between the multiple TAPs and the IC's 1149.1 test pins. The TLM is an interconnect layer that allows one or more of the TAPs to be connected to the test pins for scan purposes *(Fig. A)*. The TLM also can enable background BIST functions independent of foreground test-access operations.

Because it can be accessed by all the TAPs on the chip, the TLM can be considered a "community" test data register, according to Whetsel. Communication between the TLM and the TAPs is via select (SEL) and enable (ENA) signals. On power up or test reset, the TLM defaults to connecting TAP1 to the test pins, so the IC appears to have one TAP, as required by 1149.1. A special instruction scanned into each TAP's instruction register sets the TAP's SEL signal. In accordance with the standard, the SEL signal is high during the falling edge of the test clock signal (TCK) in the UpdateIR state. This technique causes



A. One architecture for providing test access to cores that may or may not have IEEE-1149.1 test access ports (TAPs) adds a TAP linking module to the circuit to serve as an interconnect layer.



B. The tap-linking module's TAP controller includes an IEEE-1149.1 TAP controller and gating to enable or disable the data register scan control outputs of the TLM TAP controller.

the TLM to be selected as the data-register scan path between the IC's test data in (TDI) and test data out (TDO) pins. A data-register scan operation shifts data through the TLM from TDI to TDO.

The TLM contains a TLM TAP controller, a shift register, decode logic, and a link-update register. The TLM TAP controller is always enabled to track the state of the test bus protocol on the TCK and TMS pins. But the TLM TAP controller's outputs are enabled only during a data-register scan operation, and only if the SEL input from the currently enabled TAP is high *(Fig. B)*. The TLM TAP controller includes an 1149.1 TAP controller and gating to enable or disable the data-register scan-control outputs of the TLM TAP controller.

The TI proposal requires several modifications of each TAP controller to allow interfacing with the TLM. The controller must include an input for the ENA signal from the TLM. The reset input to the controller, which normally is connected to the $\overline{\text{TRST}}$ pin, is wired to the TLM's $\overline{\text{Reset}}$ output in order to allow global reset of all TAPs. The port's instruction register must include a SEL output to the TLM and at least one new instruction to allow setting the SEL output high to enable scan access for the TLM. Also, a multiplexer on the TAP's TDI input supports the linking of multiple TAP's in one scan path.

Whetsel notes that the proposed architecture meets not only current needs for core access, but also future requirements. Like TAPs, the TLMs designed into ICs would be inseparable parts of the design. So just as today's ICs with TAPs are evolving into cores with TAPs, future ICs with TLMs may evolve into cores with TLMs. Removing them in the transition from IC to core would require redesign and prevent reuse of test schemes based on the TAPs and TLMs.

Whetsel can be reached at l-whetsel@ti.com.

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must come up with a test infrastructure, which must permit not only test access, but isolation when needed.

"We have the problem of providing test access, but at the same time we have the problem of providing test isolation," continues Varma, "so that when we test one component, that component doesn't interfere with others." He says, "We must make sure that it doesn't cause bus faults or unsafe states in other components on the chip."

A somewhat different perspective comes from Bernd Koenemann, a senior director at LogicVision Inc., San Jose, Calif., and the company's representative to the alliance test group. While the question of where the IP blocks come from is certainly important, Koenemann believes more fundamental questions must first be addressed: What is in the block and how should it be tested, regardless of who designed it?

A Growing Bandwidth Gap

Koenemann cites the Semiconductor Industry Association's roadmap for IC development and how it puts the test problem in focus. Packaging costs are predicted to drop from 1.4 cents per pin in 1995 to 0.8 cents per pin by 2010, nearly a factor of two. But nonrecurring engineering (NRE) cost per transistor is supposed to drop from 0.0003 cents in 1995 to 0.00001 cents in 2010, a 30-fold decline. "To make a long story short, we see a widening gap between I/O bandwidth for getting data in and out of the chip versus the compute power and the I/O bandwidth for stuff in the chip," he says.

Because there will be a different economic environment, future IP cores will likely not be direct copies of ICs once meant for pc-board mounting. Instead, they will be extensively redesigned to take advantage of the on-chip bandwidth, and that will have a profound impact on testing. "If I'm going into a consumer product, for cost reasons I may have a 200-pin package, but a 1000-bit-wide memory inside the chip," says Koenemann. "So this simply means that it's going to be increasingly difficult in the future to get the I/O bandwidth needed between external test equipment and the very bandwidth-consuming internal elements," he says *(Fig. 1)*.

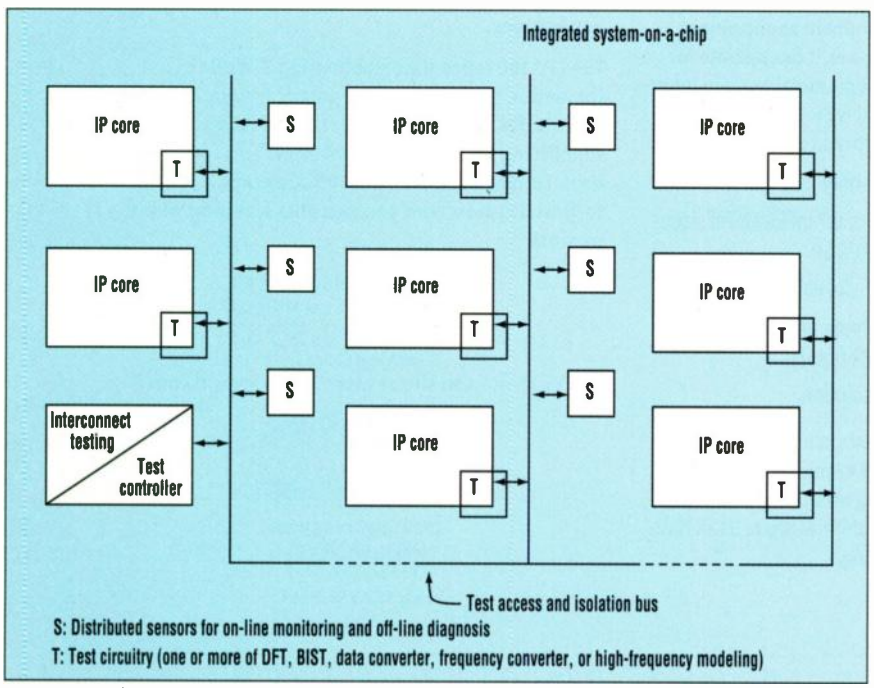
LogicVision is banking on embedded test functions being the way IP cores will be tested in the future. "Actually adding hardware into the silicon, into these cores, is going to be the key way to solve this problem," says Robert Smith, the company's vice president for marketing and business development. "A couple of the larger ATE vendors have come out and said that this is going to be part of their roadmap for the future because there's not going to be any other economical way for testers to tackle these problems," Smith says.

Embedded test structures will be used not only for digital blocks, but also for parametric testing of mixed-signal and analog blocks, according to Smith. He cites work done by the IEEE-1149.4 committee on an analog test bus that will allow measurements to be made on-chip and then sent off-chip for external evaluation. "It's very clear that embedded test is going to become a way of life," says Smith. "That's really the only way that the on-chip test problem is going to be solved—in concert with external machines that can take advantage of the on-chip hardware."

The changing economics of the semiconductor industry are also advancing the cause of design-for-test (DFT) techniques in core-based designs. Because decreased time-to-market is so important to the economic success of new designs, the costs of DFT schemes are becoming less of an issue, according to Mark Olen, product line manager for the DFT Group in Mentor Graphics' Silicon Systems Division, Wilsonville, Ore. The fact that gates are becoming less expensive and pins relatively more expensive also works in favor of DFT, especially built-in self-test (BIST), he says.

There's still more that can be done, however. Olen says Mentor is working on increasing pattern compression and throughput, using fewer vectors, and requiring less test data for full and partial-scan techniques. Also needed are more programmability for algorithmic pattern generation and field programmability for memory BIST controllers. "What we have to do is drive all of this technology to be able to reduce even further any of the obstacles," he adds.

Considering the wide range of trade-offs inherent in choosing a technique for IP core DFT, vendors should supply ASIC integrators with three choices of techniques: deterministic tests, algorithmic pattern generation, and pseudorandom pattern generation, according to Janusz Rajski, chief



3. Because of the increased power-dissipation levels in system chips, higher temperatures may cause reliability problems. This reliability issue may require the use of sensors connected to the test access circuitry via a test bus.

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X1000 Gain
16 upper & lower
BW limits

NEW

Model 1855
DC-100 MHz
X10 Gain
Very fast
recovery
from overdrive

Preamble 1800 Series stand-alone differential amplifiers are designed to function as signal conditioning pre-amplifiers for your oscilloscope, spectrum or network analyzers.

Model 1855 combines Gain, High CMRR, Very Fast Overdrive Recovery and Wide Common Mode Range to simplify direct measurement of such difficult signals as a switching supply upper gate drive.

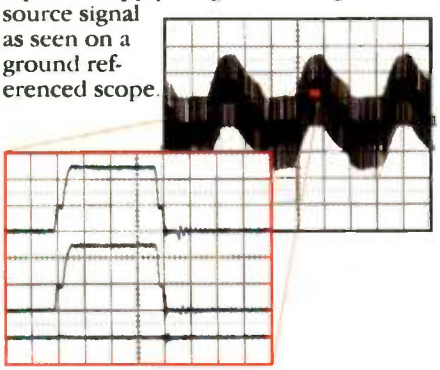
Model 1822's X1000 Gain can extend your scope's sensitivity to 1μV/div and includes a full complement of upper and lower bandwidth limits. Strain gauge, bio-medical and other physical parameters are well within the reach of the 1822.

Preamble XC Series Differential Probes give the user a choice of X1, X10, X100 and X1000 attenuation factors and circuit loading as low as 92 meg/4.5 pF. They facilitate differential measurements from microvolts to kilovolts

The **1800 Series** sport the industry's widest common mode range; limited only by the probe's voltage rating.

Measurements in off-line switching power supply primaries become safe, accurate and easy-to-make.

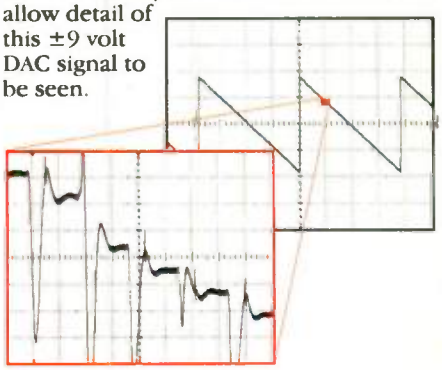
CONVENTIONAL
A power supply's highside FET gate to source signal as seen on a ground referenced scope.



DIFFERENTIAL
The 1855 rejects the line voltage and high dv/dt signal, cleanly displaying the upper and lower gate drive signals.

Preamble's 1800 Differential Amplifier Series low noise, wide common mode range and Precision Offset Generator allow minute portions of very large signals to be examined with 5½ digit resolution. The generator acts as a precision position control and extends your scope position range to over ±150,000 divisions; the industry's tallest display!

CONVENTIONAL
A scope lacks sufficient position range and lacks the ability to recover from overdrive to allow detail of this ±9 volt DAC signal to be seen.



DIFFERENTIAL
The 1800 Series allow the individual DAC steps to be examined at any point on the wave-form and measured to 5½ digit resolution.

PREAMBLE INSTRUMENTS

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scientist in Mentor's System Design Division. Deterministic testing is the conventional technique using stored patterns generated by automatic test-pattern-generation programs and working in conjunction with tools for scan insertion. Algorithmic and pseudorandom patterns are used for memory BIST and logic BIST, respectively.

Multiple Methods Needed

"We believe that for quite a while you will need combinations of all three of these techniques to be able to completely test the digital parts of system ASICs," says Rajski *(Fig. 2)*. For example, there are some very good, popular cores that should be useful for at least a couple of years, but which don't meet the design rules mandated by BIST. As a result, they will require stored vectors to test. Other designs must be tested for delay faults, which require stored patterns to cover critical paths, says Rajski. In still other applications, an integrator may use BIST to cover problems such as stuck-at faults and transition faults, but then target path-delay faults with deterministic patterns. Fault diagnosis and other issues also may require the use of deterministic patterns. "We won't be able to test system ASICs effectively without any one of these techniques," adds Rajski, "They're all essential."

The continued use of deterministic patterns means that traditional ATE equipment is not going away any time soon. Its role and capabilities will be changing, however. In refuting the talk at some design houses that the advent of VSI and BIST, and other DFT methods mean the end of "big iron," Bill Bottoms, president of Credence Systems Corp., Fremont, Calif., says it's exactly the reverse. "If we don't use these techniques to enhance the productivity of testing, then there is no way that industry growth will not be damaged," he says.

The problem as seen by Bottoms, whose company manufactures that big iron—traditional ATE, is that fab facilities can now build a billion transistors in parallel on a wafer, while testing of those transistors still goes on pretty much one at a time. He sees IP cores bringing certain advantages to the test problem. That is, if designers use the DFT capabilities available to them and ATE manufacturers find ways to leverage the resources of the tester.

Tester vendors must do two things to make their products more cost-effective for their customers. "We believe testers will need to have the ability to control the BIST resources that are on-board the silicon," says Bottoms. "You may need BIST resources that are not exercised all the time on every chip, maybe because of time considerations, maybe for power reasons," he says.

"You also will need to understand how BIST technology works on the particular chip, so when you have a failure in a block you can use more conventional test resources to diagnose that failure and provide feedback to the fab or the design people to help them correct the problem," he continues. "And, generally BIST tools tell you only that it passed or failed."

Key to the success of IP in system chips will be test reuse. Without it, time-to-market savings will be dissipated.

Bottoms notes that BIST techniques are getting better, and the area penalty BIST exacts on the silicon is going down, partly because BIST implementations are leveraging the resources of testers instead of competing with them. But it will be some time before BIST is the primary strategy for testing advanced circuits. Memories will go first because they're relatively easy to test and there's not much binning activity required. "But it will take some time for BIST to migrate into analog circuits and to take over a significant part of the load for random logic circuits," says Bottoms. "It will probably be quite significant over a three-year period, but it'll probably be 10 years before it really meets its full potential."

High Frequencies A Problem

Another concern is the increasing mixed-signal or analog content of system chips based on IP cores. The problems of access and greater complexity remain, but with added issues raised by frequencies that are now hitting the gigahertz range. The IEEE-1149.4 analog test bus will help, but it will be frequency-limited, according to Bozena Kaminska, technical officer at Beaverton, Ore.-based Opmaxx Inc. Opmaxx specializes in mixed-signal and analog test solutions. The 1149.4 approach will experience problems at a frequency of about 300 MHz, so further work is needed, she says.

Kaminska also notes that the new system chips will use more power, so higher temperatures will cause reliability problems. "Power, temperature, and other parameters will eventually need to be monitored on system chips," she says. "Already there are companies that have started to address this issue, and there will be many more." A probable solution is the inclusion of power and temperature sensors into future test access ports *(Fig. 3)*.

The lack of test procedures for interconnects between IP cores is even more critical when mixed-signal and analog blocks are involved. "With interconnects, again it depends on frequency," says Kaminska. "The tests can be defined by only time-related parameters, but as the frequency increases more and more parameters must be considered. Probably most of the research effort should be concentrated to cover interconnect testing," she says.

Kaminska raises further concerns about compatibility problems between digital and analog IP blocks. The digital test vectors and analog stimuli will have to travel through both types of circuitry. "What is the possibility of propagating digital vectors through analog or mixed-signal blocks and analog or mixed-signal stimuli through digital blocks?" she asks. Kaminska continues, "This will be necessary because even if we have BIST and other DFT techniques we will still need some stimulation and some access between blocks."

How Valuable	Circle
Highly	551
Moderately	552
Slightly	553

Here's What's Coming In The Next Two Months

Be sure to check out the best cutting-edge information for engineers and engineering managers, every two weeks. Here's the line-up of some of the important topics featured in our February and March issues.

February 9, 1998 Issue

- **PIPS:** Interconnects
- **Computer Boards & Buses:** Standards: Microcontroller Boards, Graphics, PCMCIA, Peripherals
- **Advanced Semiconductor Devices:** ISSCC
- **Analog Design:** Power Control

February 23, 1998 Issue

- **Test & Measurements:** European Design Automation & Test Conference Preview
- **Embedded Systems:** Embedded Development Tools, RTOSs, Software/Hardware Intergration
- **Analog Design:** CCD Conversion Products
- **Digital Design**

March 9, 1998 Issue

- **Analog Design:** Commodity ADCs
- **PIPS:** Passive Components
- **Electronic Design Automation**
- **Test & Measurement:** Update: Communications Test

March 23, 1998 Issue

- **Digital Design:** High-Performance DRAMs
- **Computer Boards & Buses:** VMEbus
- **Communications/ Networking Technology:** Information Appliances
- **Embedded Systems:** Embedded Systems On The Internet

ELECTRONIC DESIGN

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Core Proliferation: Security And Protection Issues With IP Integration

Black-Box IP Models Must Address The Security Needs Of Vendors, But Designers Want To Know What's Going On Inside Those Models.

KEVIN CURTIS
Model Technology Inc.,
8905 S.W. Nimbus Ave.,
Beaverton, OR 97005;
(503) 641-1340.

Imagine this: You walk into a bookstore and ask for a copy of *Gone With The Wind*. The clerk pulls it out from under the counter and says, "We'd be happy to sell you a copy of *Gone with the Wind*, but we can't let you read it. We'll tell you the names of the characters, their relative relationships at the beginning and end of the book and a few of their critical behaviors. If you have any specific questions, such as whether Richmond was actually burned by the Yankees, we'll respond as quickly as possible on our telephone hotline. That will be $49.95."

Developers working to integrate purchased cores into system-level macros (SLM) face just this situation when they receive black-box models of components. Design reuse and intellectual property (IP) sourcing are supposed to make life easier and bring products to market faster. But the security and protection needs of IP vendors—who don't want to give away the store by revealing too much of their proprietary parts—often conflict with designers, who need to know what's happening inside those black boxes.

The question of how to balance the security needs of vendors while fulfilling the information needs of developers is proving to be a major barrier to the success of design reuse. Until that question is answered, an active third-party market for IP cannot reach its full potential. A key aspect of fulfilling the need is the ability to provide protected IP models that can support a complete design flow. For IP that can be simulated, the ideal scenario is a model that utilizes a protection mechanism that everyone trusts, an IP model format that is fully portable and language independent, and the ability to run this model on all language-compliant simulators.

Protecting Ownership

"The battle for intellectual property creation, integration, and production is analogous to copyright authoring, publication, and printing in the traditional book publication business," says Erach Desai, vice president, EDA Research, Soundview Financial Group. In a time when the printed word was the only form of IP, Stanford, Calif. Western societies developed an elaborate system of laws allowing authors to share their work and be paid for it.

The industrial age introduced the concept of patent rights, in which unique machine capabilities could remain the property of their inventors while the machines themselves were sold for profit. Patents remain a powerful tool to protect hardware innovators, but today's market in the buying and selling of virtual electronic components has yet to develop a comparable set of common laws. In this complex world, where hardware is created first in the mind of designers and then on their computers, the legal precedents to protect virtual components have not yet been established.

Software developers struggle with this issue, developing increasingly sophisticated schemes to maintain control of their code while profiting from the sale of products. Computer hardware developers, however, have until recently been insulated from the problem, with designs protected by the secrecy of black boxes and the legal shelter of patent laws.

In the hardware world, secrecy meant profitability, and the secrets of a company's most valuable proprietary designs were protected with more vigor than the crown jewels. That was fine, as long as proprietary chips remained inside their black boxes. The relationship between different chips on a board was well defined, allowing a developer's best technology to be built into products for sale. The worth of the design was proven by the superior market performance of the products it powered.

But what happens when the real value comes from selling the ideas inside the black box? Attracted by the potential profits of IP sales, and driven by the fear of being left behind in the system-on-a-chip revolution, today's hardware vendors can't just sell chips any more—they need to sell their ideas. "A fact of life is that most system-level macros will be modified in the design process. That's why black-box SLMs have lost their popularity. We need to figure out how to produce white-box

Talented Students Across the Nation are Recognized in the 1997 Student VLSI Design Contest

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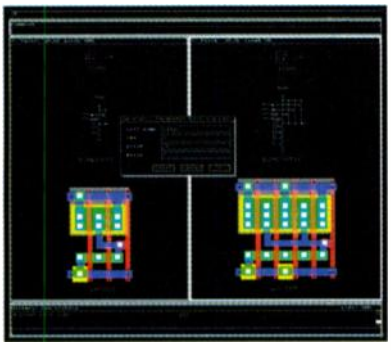
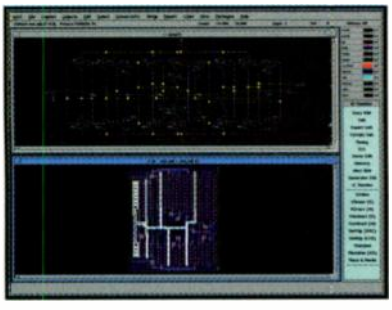


Novice Category – Duke University

Duke University senior Dennis Kim earned first-place honors in the novice category for his entry entitled, "A Second Order Sigma-Delta Modulator." The thrust of this work was the utilization of mixed-signal CMOS VLSI technology to develop a sigma-delta architecture to be used for high-resolution analog-to-digital conversion in the next-generation Ultrasound scanner system. Kim relied on Mentor Graphics' IC Station® in developing his project.



Experienced Category – University of Toronto

Steve Jantzi, a University of Toronto Ph.D. candidate, was awarded first place in the experienced category for his entry entitled, "A Quadrature Bandpass Delta-Sigma Modulator for Digital Radio." The primary focus of this work was the implementation of small, inexpensive, low-power communication devices that are robust, testable and capable of handling multiple communications standards. Jantzi employed Mentor Graphics' GDT® suite of tools in his work.

Winners: Novice Category

1. **Duke University** - Dennis Kim • Design: "A Second Order Sigma-Delta Modulator"
2. **University of Notre Dame** - Dominic Bartek, Islamshah Amlani, Xiaoming Wang, Yumin Zhang, Pengcheng Zou • Design: "Static RAM with Multiple Sensing Schemes"
3. **University of Michigan** - John Brown Wei, Matthew Peter Gerlach, David Grant Overholt, Rahul Bharat Desai, Heidi Lee Best • Design: "Implantable Cardioverter Defibrilator"
4. **Duke University** - Alan Whitehurst, John Choi, Michael Cresante • Design: "A 5-Bit Analog-to-Digital Converter"
5. **University of Minnesota** - Gurprit S. Chandhoke, Sarvesh Shrivastava • Design: "A Digital Serial Systolic Modular Multiplier for the RSA Cryptosystem"

Winners: Experienced Category

1. **University of Toronto** - Steve Jantzi • Design: "A Quadrature Bandpass Delta-Sigma Modulator for Digital Radio"
2. **Princeton University** - Martin Benes • Design: "A High-Speed Asynchronous Decompression Circuit for Embedded Processors"
3. **University of Michigan** - Keith Kraver • Design: "A 1.8 GHz, 25mV Phase Locked Loop with a Low Phase Noise Voltage Controlled Oscillator"

Congratulations to these students on their winning designs!

A special thank you to Electronic Design Magazine for donating this space to recognize these talented students.

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SLMs before system-level integration will take off," says Gary Smith, principal analyst, EDA Services, Dataquest.

As they work to find ways to share their designs, many vendors are carrying with them old ideas about control and secrecy. They believe that a company can profit from the sale of a design only if it maintains absolute control of the design information. Another opinion is that a free market for third-party design might not work. Some industry people believe that IP protection is iffy because it's hard to trace when elements have been used without a license. But, the bottom line is trust. "For IP business to work, trust and teamwork are essential ingredients for projects spanning companies, continents and cultures," says Robin Szby, chief executive officer, Advanced RISC Machines.

Thinking Outside the Black Box

Fortunately, the electronics industry is working toward creating standards that will make an open-IP marketplace possible. For example, the Virtual Socket Initiative (VSI) Alliance made solid progress toward open standards in its first year of operation. VSI signed up more than 150 members from the EDA, semiconductor, and IC design communities. The organization published an architectural document in March 1997, and sponsors six ongoing development working groups (DWGs): Implementation/Verification, Analog/Mixed Signal, IP Protection, On-Chip Bus, Manufacturing Test, and System-Level Design.

But the task is not simple. VSI specifications won't start to become public until later this year. The first two VSI specifications, one for mixed-signal virtual components and another for "hard" or technology-specific cores continue to undergo member reviews.

On issues of security and protection, the alliance has made little progress. The alliance committee working on legal protection issues has concluded that it's impractical to completely protect IC IP throughout the design cycle. The IP Protection DWG is working to define standards and interfaces, but according to Larry Rosenberg, chairman of VSI's Technical Committee, the group has determined "that in no way [does] it make sense to absolutely protect IP through the entire flow."

Instead, the group will probably recommend a hybrid proposal in which virtual components will be encrypted for use with some tools, but decrypted for others. The group also is exploring a variety of concepts for protection, including new research on "digital signatures" by Professor Miodrag Potkonjak of the University of California at Los Angeles (UCLA).

Another more upbeat example of developing industry standards is the ASIC Council's new Open EDA Library Initiative. The ASIC Council's technical committee has been working with various standards bodies since June 1997 to merge their efforts into a single, cohesive representation. The council operates under the auspices of the Silicon Integration Initiative (SII), the new name for what was once known as the CAD Framework Initiative. SII is an organization of silicon systems and tool companies that represents semiconductor vendors systems houses and EDA tool suppliers.

How to balance the security needs of vendors while fulfilling the information needs of developers is proving to be a major barrier to the success of design reuse.

The Problem With Standards

Unfortunately, concerns about patent infringement and control of proprietary information are still barriers to establishment of open standards. This struggle between the forces of patent protection and standardization is best demonstrated by the RTL standards effort carried out by Open Verilog International (OVI) and VHDL International (VI) working groups.

In the absence of overall industry security and protection standards, three general approaches to IP integration are in use today: custom design of the core and its target ASIC by a semiconductor vendor or consulting design services group; vendor integration of a customer's system logic with the vendor's core; and desktop core integration, in which the system designer builds the ASIC logic and, using standard EDA tools, integrates a vendor's core. The first two approaches allow the core vendor to maintain control of its own IP and eliminate the need for security measures.

Desktop developers, however, run into the protection/security problem when core suppliers require protection of their intellectual property, especially core netlists and layouts. As a result, developers who require a detailed simulation model of a component can face real problems attempting to integrate a core from a vendor who will not disclose the netlist. In the future, it is expected that all vendors will want to provide simulation models that can give developers what they need to do their job without revealing source code and signal names.

Another barrier confronted by system designers is the need to customize cores for a particular application. Cores also may require additional "glue" logic to integrate them into the final ASIC. Depending on the differences between core interfaces, this logic may require significant research, which ultimately may neither be optimal nor efficient.

A standard VHDL-based design might consist of a "hard" microprocessor core and reusable "firm" cores, as well as custom RTL logic. Hard cores are generally defined as having a predefined layout that cannot be modified by the system designer. One reason for hard cores is to protect the IP they represent. Another rationale is because their design is timing-critical and the layout must not be disturbed once it's finalized. In either case, the hard core is treated as a library element during the design cycle. Black-box models attempt to represent function and performance, without revealing the details of the design.

Firm cores are usually delivered as a mix of RTL code and a technology-dependent netlist, and included with the rest of the chip logic. In these cores, with the netlist visible to the designer, the design can be customized by the end user.

All the parties involved in this new marketplace are struggling to main-

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Sydney Opera House, Australia
Jutting into Sydney Harbor, the Sydney Opera House is a complex of theatres and halls linked together beneath its famous shells. The defined spherical geometry of the shells are a deviation from the original design, which proved to be structurally impossible to build. This final redesign enabled the roof vaults to be constructed in a pre-cast fashion, greatly reducing building time and cost, and ultimately enhancing use of space, for maximum performance.

READER SERVICE 302

tain control of critical parts of the process. IP vendors, chip designer, and foundries each have different security and protection goals, different areas which they want to control, and often, conflicting security requirements. This battle will become more fierce as the reuse of core logic becomes more financially critical.

In the meantime, the mechanics of defending IP rights are unsettled. Vendors have a powerful economic incentive to protect their property from unauthorized reuse; once it's gone, it's impossible to get it back. The legal community is virtually helpless.

Security and protection strategies vary among vendors, who must satisfy their IP customers while struggling with the conflict between protecting information and providing necessary data for chip design. Many are discovering that cores can be compiled in nonhuman-readable formats. In this form, the core's secrets are not revealed, but the model still contains all the critical information designers need for accurate simulation.

Fabricators, on the other hand, want to protect cores because they need to control manufacturability. They want to see IP shipped to designers in rock-hard form, because they know that adding modifications to cores and interfaces reduces the known good qualities of the cores and introduces more risk into the process. Knowing that nonfunctioning silicon makes everybody look bad, foundries prefer that developers do not make changes that could compromise the manufacturing process. At the FPGA level, such hard cores are working successfully, allowing these components to increase in their size and complexity at a much faster rate than other types of devices. Future advances in the compile speeds of HDL simulators will allow vendors to ship (and developers to work with) even more detailed simulation models of their hard cores that can be protected from the unwelcome intrusion of those who want to commit engineering larceny.

Seemingly at the bottom of the food chain are the developers who need access to data. They have to create and verify designs, which can be extremely difficult to do when a major component model is delivered as a black box. Even if there is no breakthrough or unusual technology in any one block and all have been verified individually, block interfaces are extremely complex.

"The technology today is really lacking. We need to move to some form of compiled-library approach where you can provide object code, for customer use, and it contains all the information they need without revealing the internals," says Andy Graham, president, Silicon Integration Initiative.

Without extremely high-speed simulators, the time required for simulation may be prohibitive. But regardless of the file sizes, designers like the freedom of RTL models that can be simulated quickly and resynthesized to make verification possible. With little control over the form cores take, designers need tools that can handle Verilog and VHDL components in the same design. They also wish for simulatable cores that are independent of platform and simulator version. Meeting these needs requires compatible data formats, test methodologies, and bus interfaces. Additionally, platform, language, and version independence are critical issues for parts libraries and for the simulators that must be able to combine third-party components.

Many efforts are being made to set a clear direction for the full proliferation of IP technology that will have a dramatic impact on designs of the future. Initiatives are making progress on a number of fronts, however there are many issues today that are unresolved. Technology innovations are setting examples which must be incorporated into an industry-wide standard. Without fully supported industry standards, that level of portability is limited. However, as industry groups work together to eliminate black-box barriers, new development tools will become more powerful while still protecting valuable IP secrets.

Kevin Curtis is general manager at Model Technology Inc., a wholly owned subsidiary of Mentor Graphics Corp. Curtis received his bachelor of science degree from Arizona State University and his MBA from the University of Oregon.

How Valuable	Circle
Highly	554
Moderately	555
Slightly	556

Intellectual Property Drives Medicine's Embedded Future

Here's A Look At Some Present (And Future) Technologies That Will Impact Our Lives In Really Meaningful Ways.

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(508) 881-1850;
e-mail: jlkrasner@sprintmail.com.

Listen up, fellow engineers. The future is today. If you possess an entrepreneurial spirit, you need to remember that although biotechnology and computer software products get rave reviews in the press, more individuals have become millionaires via medical devices that any other technology market. If you are an embedded software or hardware engineer, you can have it both ways. Medical devices have provided the greatest payoff for developers and users of intellectual property.

Consider: The neurosurgeon deftly opens the scalp and performs the expected craniotomy without incident. Separating the cerebral hemispheres and cutting through the thick band of fibers that communicate between the hemispheres, the tumor is visualized just where the CTscan and the magnetic imaging has shown it to be. The computerized imaging has shown that the tumor has grown deep into the older cortex, into delicate areas of the brain where there is no margin for error.

The surgeon can only see the top of the tumor and can not visually resolve how thick or thin the tumor is as he removes it from the only angle possible. That view is from top down. But this is not ordinary neurosurgery. Directly above the surgeon, a computer-based system is projecting an image of the tumor that is just underneath the area the surgeon is dissecting, onto the surgical field. Thus, the unseen portion of the tumor can be removed without destroying normal brain tissue.

Looking to the side, the surgeon can see a 3D side view of the tumor and the ongoing procedure. In this way, he monitors his progress and anticipates what he will encounter. With meticulous care the surgeon removes the entire tumor, sparing the critical adjacent brain tissue.

Elsewhere, a patient is discovered to have a malignant tumor behind his eyes. The growth is so large that it can't be surgically removed, and radiation will certainly leave the patient blind. For 30 minutes a day, five days a week, the patient is placed on a table, his head anchored by a plastic mesh mask while a computer aligns thousands of tiny radiation beams to fit the exact shape of the tumor, leaving normal tissue unharmed. With little pain and no side effects, the patient returns to work full-time while continuing two months of treatment that will cure his cancer. Other patients are similarly treated for tumors and cancers of the brain, spine, head, and neck.

In a small, computerized room in Fairbanks, Alaska, an Army surgeon slips on a virtual-reality helmet and associated gloves that are hard-wired to a bank of electronics. At his side are several hand-held devices that look similar to hemostats. Looking through the visual apparatus, the surgeon views the abdomen of a patient in the Saudi-Arabian desert who has had laparoscopic tubes placed in his abdomen by local paramedics. Using these "electronic hemostats," the surgeon in Alaska removes the patient's gall bladder as if he were standing next to and touching the patient. Following the surgical procedure, the local paramedic removes the apparatus and closes the superficial incisions. The physician comments that his sense of touch is even better with virtual reality than when he is directly performing surgery, but apologizes for the length of time taken for the procedure. He comments that his young residents (whom he calls Nintendo surgeons due to their superior eye-motor skills developed in playing computer games) could have done the job much better.

In Japan, a quadriplegic teenager is navigating his motorized wheelchair without apparent motion or assistance. The teen is wearing a headcovering, similar to those worn by skiers, but containing surface electrodes that are connected to an embedded computer board. The heuristic software, developed by artificial-intelligence researchers, has learned to interpret the brain waves that result when the teen merely thinks of the words "right," "left," "stop," "go," etc.

Other researchers will be working with paralyzed and bed-ridden patients to allow them limited, but significant control over their environment. Rehabilitation medicine will be on the threshold of a new awakening.

Before long, electronic devices that are used interactively with human perception (e.g., jet avionics displays, radar screens used by air-traffic controllers) may possess the ability to know when the human user is unable to effectively process information necessary for the safe operation. Known as cognitive overload, methods for measur-

Want To Go?

The Portable By Design Conference and Exhibition, held concurrently with the Wireless Symposium, takes place at the Santa Clara Convention Center, Santa Clara, Calif. The technical sessions run Feb. 10-13, while workshops take place Feb. 9. The keynote address and luncheon, featuring David Hancock, president and CEO of the Hitachi PC Corp., will be held on Feb. 10 at 11:30 a.m. For more information, contact Bill Rutledge at (201) 393-6259.

tems know that some knowledge of a battery subsystem is required to develop a battery-based system, it's often important to deal with the battery as a "black box," meaning that the most important element is how to deal with the signals that are coming from and going to the battery, not necessarily what's happening inside the battery itself. The "Battery subsystem session," chaired by David Heacock of Benchmarq Microelectronics, Dallas, Texas, deals with the battery as a "pins-out" subsystem, giving designers just the information needed to build a battery-powered system.

With customers demanding more functionality, smaller size, and greater reliability in their mobile systems, designers continue to wrestle with IC packaging, system cooling, and shock/vibration issues. To help designers meet this challenge, the "Mobile-system packaging concerns" session will discuss some of the latest IC packaging options, along with novel system-cooling techniques. In addition, an analysis of system behavior under severe shock will show attendees what to expect and how best to isolate a portable system from its effects.

"Portable-system software issues" covers a number of critical software topics that affect the design of portable systems. Among them are how to make efficient and modular operating systems that work with compact programs to minimize memory space and support the newest peripherals, such as flash memory. Other issues include using power-management software, which can play a vital role in maximizing battery life. In addition, network and Internet software will play a role in helping portable devices communicate. The last portion of the discussions will involve Java, as it appears destined to have a major influence on the design of portable and handheld systems.

Responsible Engineering

The session title says it all: "Designing for the environment doesn't have to be expensive." Within the next decade, we can expect to see environmental concerns becoming an integral part of the design process. Practices such as designing for recyclability and analyzing the environmental costs of producing a product will be as much a part of the engineer's responsibilities as designing for cost and manufacturability. In this session, attendees will meet with some of the pioneers in the Design For the Environment (DFE) movement who are charting the course of this emerging technology. In addition to providing an overview of the field, they will present an array of papers covering everything from "green computer" design to working with the new ISO 14001 environmental audit standard. Wherever possible, emphasis will be on practical solutions that can be implemented in a globally competitive business environment.

The common thread for the "Battery management" session is the Advanced Control and Power Interface (ACPI). Chaired by John Milios of USAR Systems, New York, N.Y., the session will focus on the role ACPI plays in system design, from the operating system, to smart batteries, the chip set, the SMBus, and embedded controllers.

Infrared ports are now popping up in the strangest places, including pay phones, cellular phones, fax machines, and medical equipment. The low cost, simplicity, speed, and versatility of infrared data transfer is quickly making it the wireless equivalent of the ubiquitous RS-232 port. Presenters in the session titled "Infrared data: A technology for universal connectivity" will introduce the fundamentals of infrared technology, as well as explore some of the latest developments in the field. Attendees also will have the opportunity to learn about several innovative applications of infrared data and how they can incorporate it into their next design. The session is chaired by Dr. Keming Yeh of ACTiSYS Corp., Fremont, Calif.

Designing for portable applications requires that designers make a number of critical decisions that will significantly impact the end product, not the least of which is identifying the most appropriate system, architecture, and bus. The session dubbed "Systems, buses, and architectural issues" will discuss some of the choices now available, how they can be implemented, and the benefits to be derived from such an implementation choice.

What good is a rechargeable battery if it can't be charged properly? The "Charging circuits session" will explore what techniques are available to charge different types of batteries, and how the charging techniques can be employed to get the fastest charge, while maintaining the maximum number of charge cycles for the battery.

It's no surprise that portable equipment contains a number of different components that are strictly governed by size, cost, and performance requirements. In fact, size and cost requirements often compete with demanding performance specifications. As a result, many low-power electronic components are designed and integrated into modules that combine different types of technology. This session, "Low-power analog circuit design," chaired by James Harrer of LG Infocom, San Diego, Calif., will attempt to identify the latest advances in components and integrated modules for use in the highly competitive portable marketplace.

Finally, with displays playing such an integral role in the proliferation of today's portable applications, it's becoming more critical than ever to develop components and technologies suited for such environments. "Displays for portable and handheld computers" will attempt to identify some of the latest display developments that address many of the needs of present portable applications, and some of the other, not yet viable, applications.

CONFERENCE PREVIEW

Technical Program Highlights A Variety Of Wireless Applications

The Sixth Annual Wireless Symposium Focuses On Practical Solutions For Component- And System-Level Designs.

Victor Perrote

Keeping up to date with technological progress is an essential part of any engineer's professional development, particularly in the constantly evolving and competitive wireless industry. Fortunately, technical professionals attending the sixth annual Wireless Symposium and Exhibition will be provided with a wide array of presentations and workshops that promise to satisfy their continuing-educational needs in this dynamic field.

Jointly sponsored by *Microwaves & RF*, *Wireless Systems Design*, and *Electronic Design*, the Wireless Symposium is scheduled to be held Feb. 9-13 at the Santa Clara Convention Center, Santa Clara, Calif. The conference features nearly 70 half-hour technical presentations and 14 workshops that will offer attendees the opportunity to learn from leading engineers in the wireless field as well as to exchange design ideas.

This year's keynote presentation, addressing the theme "Building on the wireless boom," will be given by Mark Golden, senior vice president of industry affairs for the Personal Communications Industry Association (PCIA), Washington, D.C. Golden directs the organization's legislative, regulatory, and industry development activities.

Attendees at this year's event also will be treated to three "visionary keynote" sessions that provide insight on topics of interest to the wireless and portable engineering community. Gilles Delfassey, vice president of the Texas Instruments Semiconductor Group, Dallas, Texas, and worldwide general manager of the company's Wireless Communications Business Unit, will cover the theme "Making wireless work in the next century." Bob Pease, veteran analog engineer at National Semiconductor, Santa Clara, Calif., and popular columnist for *Electronic Design*, will offer his views on the future of portable and wireless technology. Amory Lovins, director of research for the Rocky Mountain Institute, Snowmass, Co., will focus on energy-conservation issues in a session titled "Laptops to hypercars—the wide-ranging impact of portable technologies on traditional industries."

This year's meeting features the return of several popular courses. Randall Rhea, well-known in the high-frequency community as founder of computer-aided engineering (CAE) software developer Eagleware Corp., Stone Mountain, Ga., as well as Noble Publishing, Tucker, Ga., will be joined by Glenn Parker, chief engineer at Eagleware, to deliver a two-day workshop on "Active, digital, and RF filter design." The course describes time- and frequency-domain approaches as well as transfer functions, emphasizing practical design issues at frequencies from baseband to the microwave range.

In addition, Rhea will present a one-day workshop on "Oscillator design for wireless applications." This course covers such topics as S-parameter calculation, noise, biasing, broadband tuning, and linearity. Design examples based on quartz crystals, inductor/capacitor (LC) networks, surface-acoustic-wave (SAW) devices, and transmission lines also will be presented.

Also returning is a three-day workshop titled "Wireless RF circuit design." The first part of the workshop is a one-day course on small-signal and low-noise amplifiers taught by Dr. Les Besser of Besser Associates, Los Altos, Calif., a pioneer in the fields of microwave CAE and continuing education. Besser will address such topics as S-parameter analysis, noise-figure, matching, and stabilization. Design trade-offs will be examined with the help of graphical tools. The second part of the workshop is a two-day course on high-efficiency power-amplifier design. Presented by industry veteran Dr. Steve Cripps of Besser Associates, this course will examine design techniques for bipolar- and FET-based amplifiers, focusing on practical applications. Load-pull and linearization techniques will also be described.

Aimed at technical managers and marketing professionals, a two-day course titled "Wireless made simple" offers a tutorial-level overview of RF and wireless technology. Taught by Allan Scott of Besser Associates, the workshop will devote one day to RF principles, systems, and devices—with the second day focusing on wireless terminology and design. Modulation techniques, system functions (including error correction and voice coding), and wireless markets will be overviewed.

Returning for the sixth consecutive year, Professor Jack Holtzman of Rutgers University's Wireless Information Network Laboratory (WINLAB), New Brunswick, N.J., will offer a half-day course on the fundamentals of spread-spectrum modulation. The workshop reviews the implementation and benefits of spread-spectrum techniques on system design. Among the topics to be covered are system capacity, processing gain, code sequences, and power control.

Techniques for accurate evaluation of wireless signals will be explained in a one-day course titled "Measuring the wireless transmission spectrum" taught by Morris Engelson, long-time chief engineer at Tektronix, Beaverton, Ore., and now the president of Joint Management Strategy, Portland, Ore. Regarded by many as the "father of the spectrum analyzer," Engelson will discuss such topics as the measurement of digitally modulated signals, EMI, pulsed signals, and television signals, focusing on the

use of this versatile evaluation tool.

This year marks the introduction of several half- and full-day workshops to the Wireless lineup. For instance, Dr. Steven Best, director of engineering, and Dr. Naftali Herscovici, chief scientist at Cushcraft, Manchester, N.H., will deliver a one-day workshop on "Antenna and array design for wireless communications." This course covers topics such as electromagnetic-field analysis, selection of antenna types, propagation, and simulation. These concepts will be applied to the design of an actual antenna.

The complex transmission formats used in wireless communications systems will be explained in a one-day course titled "Introduction to digital modulation methods." Presented by Harold Walker, chief executive offer of Pegasus Data Systems, Middlesex, N.J., this workshop will review the latest advancements in digital modulation as well as the operation and implementation of these techniques. The characterization of systems using signal-to-noise ratio (SNR), carrier-to-noise (C/N) ratio, and bit-error rate (BER) will be discussed.

Also being offered for the first time is a one-day workshop on wireless transceiver design. Taught by Syed (Moti) Ahmed, president of Analog Communications, Flemington, N.J., this course will review the design and implementation of RF transceivers and their functional blocks—including the antenna, duplexer, receiver, transmitter, and synthesizer subsystems. Digital signal processing and modulation techniques also will be discussed.

Targeting prospective entrepreneurs, a half-day workshop titled "Strategic financing and high-growth business paradigms" will discuss such topics as market research, product penetration, market share, and strategic planning. Ken Schoniger and Al Juodikis of KC Press International, San Jose, Calif., will be joined by experts in technology and finance to share their views on these key business issues. The course aims to provide attendees with the tools needed to communicate with the investment community.

Another half-day workshop being given for the first time at the conference is "Phase-locked loops and frequency synthesis for wireless design engineers." Presented by Eric Drucker of Fluke Corp., Everett, Wash., this course will cover the fundamentals of phase-locked loop (PLL) analysis, design, and modeling while keeping mathematical theory to a minimum. Among the topics discussed are the effects of phase noise as well as real-world problems such as power-supply noise and isolation.

The technical sessions in the Wireless program run from Feb. 10-12. The sessions include "Cellular/cordless design," "Digital communications systems," "Modulation techniques," "Point-to-point and base-station design," "Materials and packaging technologies," "Test and measurement solutions," "Wireless data transmission," "Automotive and satellite systems," "Integrated-circuit solutions," "Wireless local-area networks," "Personal communications services," and "High-power design."

Victor Perrote is senior editor at Microwaves & RF magazine, a sister publication of Electronic Design.

PRODUCT FEATURE

Multimedia Graphics-Accelerator Chips Soup-Up Laptop Systems

By trimming the active power drain of forthcoming portable computers while providing users with advanced functions, the Lynx and LynxE graphics-accelerator chips give designers new features while reducing system complexity. Both chips, for instance, allow systems to simultaneously control two independent displays (LCDs, CRTs, TVs)—each display can show different content. Such a feature is promised in the forthcoming Windows 98 release by Microsoft. But with the Lynx family of controllers, designers needn't wait to have such a feature.

With the dual-screen capability, video conferencing would be easier to organize, and video presentations would allow the speaker notes to display on one screen while the presentation foil images appeared on the other, Also, with multitasking software, one screen can be used to work on a spreadsheet while viewing a web page on the other.

The SM910 Lynx and SM810 LynxE chips have the same basic core graphics accelerator, and operate from a 3.3-V supply. They can both support screen resolutions of up to 1280 by 1024 pixels and simultaneously display two independent motion-video windows.

The main difference between the two chips is that the lower-cost SM910 requires an external frame-buffer memory while the SM810 integrates 2 Mbytes of DRAM onto the chip to provide a lower-chip-count solution. The SM910 features a 64-bit DRAM interface that supports 1, 2, or 4 Mbytes of EDO DRAM, SGRAM, or SDRAM, and will come in a 256-lead plastic ball-grid array or thin quad-sided plastic package. The SM810, which also comes in a 256-lead BGA, employs a 192-bit-wide graphics interface—a 128-bit internal interface for the 2 Mbytes on the chip and a 64-bit expansion interface that allows users to add 2 Mbytes of graphics memory (EDO, SGRAM, or SDRAM).

The wide interface gives the LynxE a graphics memory bandwidth of 1 Gbyte/s using the 128-bit on-chip memory bus, and 1.8 Gbytes/s when the internal and external memory buses are combined. During normal LCD operation, the LynxE accelerator consumes less than 0.5 W by taking advantage of the company's VirtualRefresh architecture, which allows dynamic power management of the display. The less-integrated Lynx accelerator draws about 300 mW when active.

Both chips include a 135-MHz integrated 24-bit RAMDAC as well as a dual-clock synthesizer, an extended PLL that generates the virtual refresh clock, and an NTSC output that just requires an external NTSC/PAL analog encoder to display images on a TV screen. The chips support the VESA standard FPDI-2 low-voltage differential logic interface for LCDs, and the VESA DPMS and DDC-2 standards for the CRT interface. The host interface on the controllers consists of a fully compliant PCI version 2.1 port that serves as a bus master and performs burst writes and reads. In lots of 1000 units, the LynxE (SM810) processor sells for $42. The Lynx (SM910) graphics processor will sell for about $25 in similar quantities.

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CIRCLE 500
DAVE BURSKY

Synthesis Tool Provides Automated Flow For Datapath Design And Implementation

Datapath-intensive ICs have turned designers into number crunchers. The traditional way of dealing with datapaths has centered on a mix of time-consuming methods, such as manual handcrafting, gate-level or low-level RTL coding, and proprietary C programs or scripts. A tool developed by Synopsys now gives designers another option. The Module Compiler acts as a companion to the well-known Design Compiler tool, replacing the mix of solutions used today with an automated flow for datapath design and implementation.

Specifically targeted at the high-speed demands of multimedia, graphics, communications, and DSP applications, the tool offers faster, improved datapath logic performance. In fact, with its advanced datapath techniques, datapath design that used to take months can now be completed in weeks and even days. For example, the tool can synthesize 20,000 gates in two minutes and optimize in eight. These same techniques guarantee a 30 to 40% improvement in quality of results over more conventional datapath design solutions.

The Module Compiler tool comprehends high-level structural descriptions and automatically synthesizes them into gates. Its input, in the form of the Module Compiler Language, has the look and feel of Verilog HDL. However, it's better suited for the task of describing the synthesis and optimizations of datapaths. Designers are able to describe the implementation structure of a datapath at a high level with relatively few lines of code. And, the description of several structural variations can be indicated in the same code by using parameters, variables, and defines. Because the hardware description language is so direct and concise, the time it takes for datapath designers to progress from idea to implementation is shortened significantly.

The nature of the language also allows for quick modifications and makes design reuse easier. This is because it supports a very high degree of parametrization, allowing concise descriptions of structures that scale efficiently for reuse. As an added benefit, the Module Compiler tool uses the same technology libraries as Design Compiler, which makes the designs portable across 350ASIC libraries. The tool sells for $150,000.

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CIRCLE 501
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PRODUCT FEATURE

Low-Cost Static Timing Analysis Tool Provides Full-Chip ASIC Verification

Increasing design complexity has created huge challenges for designers when it comes to verification. In particular, designers are looking to new methodologies for gate-level verification to help them meet the challenges of high-density, deep-submicron ASICs. To aid in this battle, Mentor Graphics has developed SST (split-second timing) Velocity. The lower-cost, easy-to-use tool provides a method of gate-level static timing analysis for full-chip ASIC verification. Its high-performance capabilities, ability to fit into existing design flows, and ability to address the requirements of markets that have yet to benefit from existing static timing solutions, make it ideal for mainstream designers.

Traditionally, static timing analysis tools have been used because they don't require any test vector development, are fast, and can reduce risk of design failure. Despite these benefits, adoption of these tools has been slow because of three limitations: difficulty in sorting out false paths, the inability to handle a broad array of design styles and practices, and the fact that they're difficult to use. SST Velocity, designed around a node-based algorithm, overcomes these limitations.

SST Velocity can verify designs with complex clock schemes or multiple asynchronous clock domains. It also can locate critical paths, perform stack analysis, and analyze clock trees. During operation, it automatically rejects commonly encountered false paths, those that won't propagate a signal because of a side-input constant on a gate, and those resulting from loops in buses. Eliminating the remaining false paths is just as easy, since the tool's user interface walks designers through the verification process and pinpoints the source of the problem.

The SST Velocity tool, which sells for $37,000, is now available on Sun, Solaris and HP UNIX workstations.

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http://www.mentorg.com.
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Multitasking 3D/2D Graphics Engine Produces High-Quality DVD Video And Audio

The second-generation Mpact media processor, the Mpact 2 3DVD, is the first multitasking engine to provide accelerated 3D/2D graphics and control DVD systems. Capable of performing up to 6 billion operations per second, the Mpact 2 3DVD (jointly developed by Chromatic Research, LG Semiconductor, SGS-Thomson Microelectronics, and Toshiba America Electronic Components) is designed to operate with a host PC's x86/MMX CPU. This combination delivers high-performance 3D/2D graphics and theater-quality DVD video and audio, all at about the cost of a high-performance 3D accelerator.

To deliver high-performance 3D graphics, the processor employs a 35-stage 3D pipeline and a 500-MFLOPS setup engine. Dual Rambus RDRAM memory interfaces that address up to 8 Mbytes provide a bus bandwidth of up to 1.3 Gbytes/s, thus delivering better performance for large textures. The processor also sports a PCI/Advanced Graphics Port interface and full direct 3D software support. By incorporating support for DVD, the chip eliminates image-quality degradation that often results from the kluge that typically comes about when DVD subsystems are melded with standalone graphics subsystems. The Mpact processor can support MPEG video as a 3D texture and provide DVD native resolution playback (720 by 480 pixels) that's artifact- and defect-free.

For 2D graphics, the Mpact 2 3DVD processor delivers a Ziff-Davis benchmark WinMark'97 rating of 120 million (in a 266-MHz Pentium II system), and a 3D rating of over 200 million. To support textures, an on-chip cache provides the 3D rendering engine with high-speed access to the most-often-used textures. Additional 3D support includes features such as trilinear filtering to smooth flat, textured surfaces, and specular highlighting, which shows reflections from a light source on an object's surface.

The Mpact processor supports flicker-free, high-resolution color modes, including 1600 by 1200 pixels with a depth of 18 bits/pixel and a refresh rate of 85 Hz, as well as 1280 by 1024 pixels by 24 bits/pixel, also at an 85-Hz refresh rate. A high-speed, 24-bit, on-chip RAMDAC provides the RGB output signals for a monitor, and a separate video output signal can be fed right into an off-chip NTSC/PAL decoder. To handle the DVD playback, the processor also performs the de-interlacing needed for playback on a PC's non-interlaced monitor, thus eliminating jagged lines and motion artifacts.

On-chip scaling also allows the DVD video to be displayed in a window that can arbitrarily scaled to any size while maintaining image quality and frame rate. To compensate for the screen brightness differences between a PC monitor and a TV screen, the chip's Chromabright and Chromadjust controls allow users to adjust brightness, color, contrast, etc.

Samples of the Mpact 2 3DVD chip are immediately available from LG Semicon, SGS-Thomson, and Toshiba, while reference design boards and the Mediaware software are available from Chromatic. Prices for the chip will fall in the $35 to $45 price range.

Chromatic Research Inc.
615 Tasman Dr., Sunnyvale, CA 94089-1707; (408) 752-9100, or on the web at http://www.chromatic.com
CIRCLE 503
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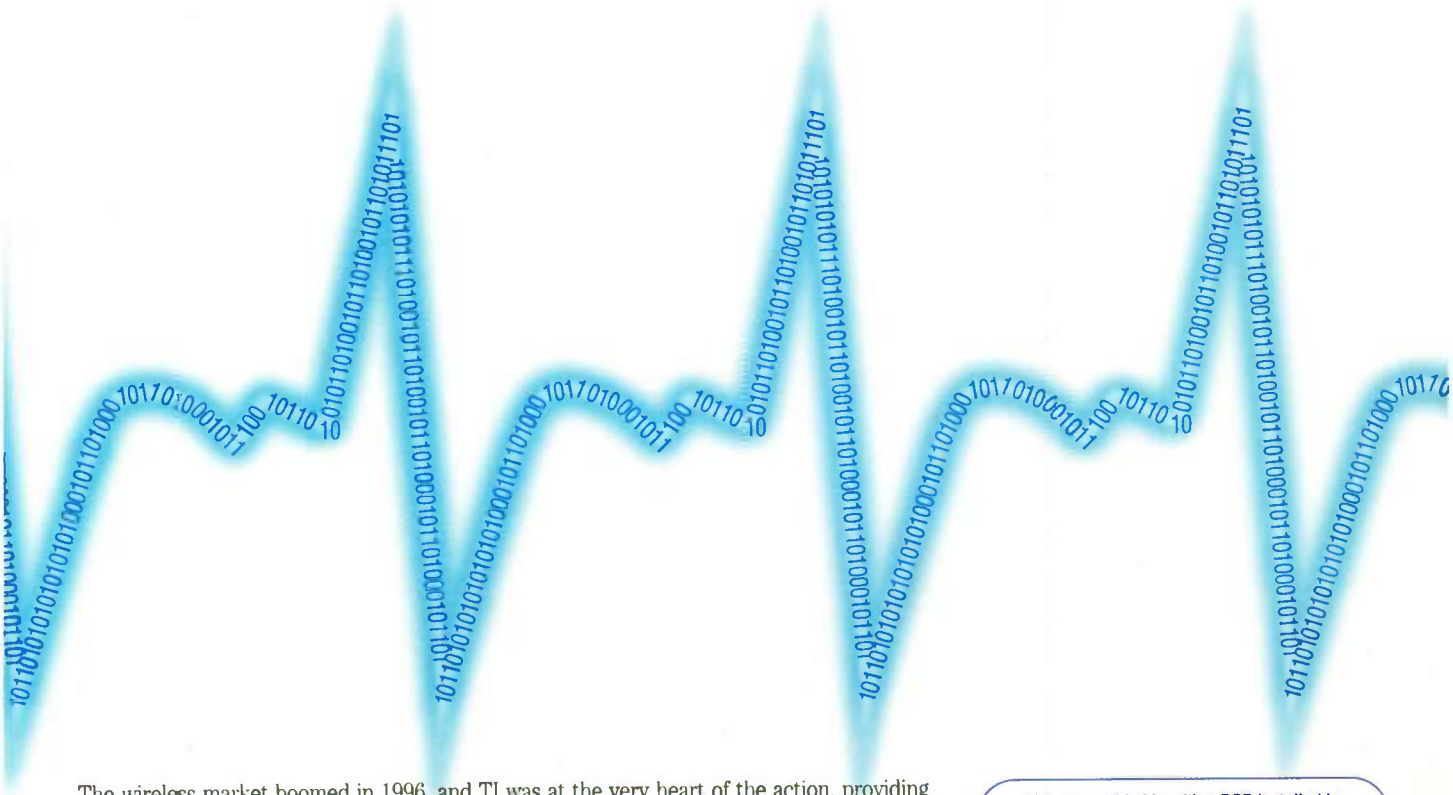

The wireless market boomed in 1996, and TI was at the very heart of the action, providing DSPs in more than 50% of the 48 million digital cellular phones manufactured.* In 1997, TI's continued commitment to the wireless market helped to lead digital cellular sales to well over 80 million. Today, TI is a leading supplier of system software and hardware solutions based on a broad portfolio of standard and customizable DSP, ASIC, mixed-signal and RF devices, giving designers all the support they need to address wireless standards worldwide.

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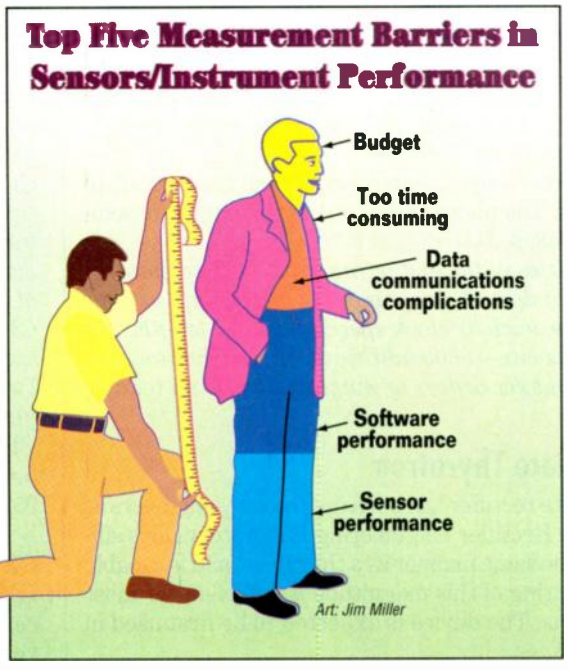
ELECTRONIC DESIGN QUICK LOOK

Edited by Mike Sciannamea and Debra Schiff

MARKET FACTS

Measuring The Future

A consistent element of providing a service or a product is quality. Customers demand it. Consumers count on it. If you are a manufacturer, you must produce a high-quality product or your sales will plummet. In the test instrument market, not only is the primary issue quality, but there's also speed of delivery and amount of product. According to a new study, "New Solutions Must Measure Up to Customer Demands," from Keithley Instruments, the next few years will show a dramatic change in instrument accuracy. Essentially, measurement instruments in the coming years will have to be six times more accurate than those available today. The race is on to find the new technologies that will enable the increase in accuracy, but the repeatability of those tests also is key. The study, tracking the measurement needs of 301 process and test engineers, asked participants what their current measurement practices are and what they expect to need over the next few years. Of utmost importance is resolution. Measurement devices must have 16-bit performance or better in the future, say 56% of study respondents. As it is, 35% of the participants say that they need that kind of resolution now. In the case of 18-bit performance, 6% of the engineers surveyed need it now, but that figure will expand to 25% in the future. In terms of accuracy, the respondents say that 0.1% of full-scale range accuracy or better is required for 3% of their current measurement applications, but expect that 18% of those applications will require that kind of accuracy in the near future. Speed is very important to the engineer using measurement equipment. Of the engineering professionals surveyed, 30.5% say that they will need over 1000 readings/second performance. That figure is in comparison to the 23% who say that they require that level of speed today. The group who say that they will need no less than 10,000 readings/second represents 12% of the study participants. Looking at another measurement practice, the study found an increase in the number of data points measured. A third of the engineers surveyed said that the typical task can require over 40 data points. But the real question here is: "What will it take to bring measurement instruments to where we need them to be in the future?" Respondents say that the limitations mostly lie in budget and time constraints. Additionally, a large monkey wrench in the works is data communications. Otherwise, sensor and software performance were seen as the top barriers to successful measurement. Glancing at the future of communications protocols, the respondents say that the most popular devices available are those that plug into serial ports, are Ethernet-based, or are compatible with the Universal Serial Bus (USB). USB stands out as a favorite in this year's study, as opposed to not even appearing as a choice in last year's study. A significant percentage of the study participants (20%) said that their choice of communication protocol for the future would be the USB. But there is a large audience (26%) for the nontraditional protocols such as DeviceNet, FieldBus H1, FireWire, HART, Interbus S, and Profibus. The study respondents nodded strongly in the direction of the Ethernet protocol (43%), but the traditional communication protocols such as the serial port (46%), 4-20 mA (35%), and the IEEE-488 (34%) took most of the recognition. The trend toward Ethernet as a data path for measurement data through a company surprised Keithley, as did the USB results. Both were not expected to have been accepted so quickly despite their high-speed solutions to measurement communications issues.

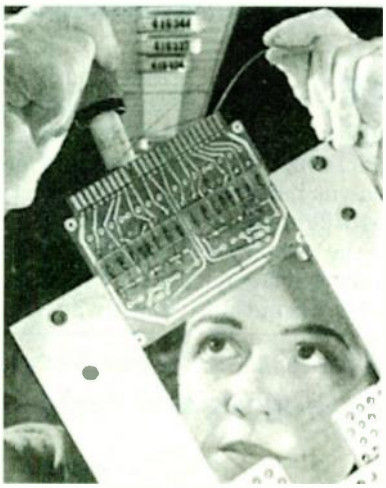


For more information on the study, contact Keithley Instruments, 28775 Aurora Rd., Cleveland, OH 44139-1891; (440) 248-0400; fax (440) 248-6168; Internet: http://www.keithley.com.—**DS**

40 YEARS AGO IN ELECTRONIC DESIGN

Airborne Digital Computer Now In Production

A miniaturized digital computer, small enough to fit into the cabinet of a 21 in. table model TV, is now in production by Hughes Aircraft Company. This assembly-line hardware is rated at 9600 additions or subtractions per minute and is designed for installation in jet interceptors. It will handle the aircraft through all phases of supersonic combat, from takeoff to touchdown.



While engaged in navigational operations the Digitair samples 33 analog and 28 digital inputs per sec while computing 14 analog and 16 digital outputs. Designed for rugged environment, it will operate over a range of ambients from –67 to + 160 F, and will withstand 15g shocks.

Built to make life easy for the Air Force technician, the new digital computer has a built-in self-testing unit. Through use of dialing devices the technician can determine if each part of the control system is working right. If not he can instantly substitute complete black boxes.

The Digitair has been flight-tested 1100 hours, can navigate, control target approach and bomb release, communications flight functions, direct armament and escape maneuvers, return the aircraft to its base in the proper landing order. The photo shows one of the plug-in assemblies. *(Electronic Design, Jan. 8, 1958, p. 5)*

This article lists a lot of capabilities in the last paragraph, but like many of the early articles about computers, it doesn't give some of the basic data we now use to judge computer performance, such as clock speed and word length. The one performance figure that it does cite—9600 additions or subtractions per minute, or 160 per second—is about six orders of magnitude behind today's computers.—**Steve Scrupski**

Solid State Rectifier Can Replace Thyratron

A commercially practical solid state rectifier has been operated by engineers at General Electric's Clyde, New York Rectifier Engineering Laboratory. This silicon-controlled rectifier operates in the same manner as a thyratron, and is capable of switching 1000 watts. A power rating of this magnitude is sufficient for most military and commercial applications. The device is expected to be first used in missiles.

Applications possible with this rectifier are the replacement of mechanical power converters and latching relays. Present operating models of the device have performed satisfactorily at temperatures of 150°C. a control load of 5 amps at 200 v has been switched in 1.5 µsec with an injected power of 15 mw.

The size of the silicon controlled rectifier is approximately twice that of a signal type transistor and 1/100 the size of a thyratron. The predicted life of the device is over 300,000 hours as compared to the 1000 hour life of a thyratron.

Wide commercial use of the device is expected. It can control the rise and fall current in a welding machine, lighting intensity, cooking heat in electric ranges, and motor speed control in appliances. Wide applications in the automotive industry are also anticipated. *(Electronic Design, Jan. 8, 1958, p. 7)*

The first SCRs were compared to thyratrons because that's what vacuum-tube era engineers understood. For today's engineer, we'd probably have to reverse the analogy—a thyratron, a gas-filled grid-controlled rectifier, was like an SCR.—**Steve Scrupski**

FREE STUFF

Hewlett-Packard (HP) has published a booklet that provides power-product engineers with helpful hints for enhancing power-product operation and using measurement capabilities. "10 Practical Tips You Need to Know About Your Power Products" includes shortcuts and recommendations such as using remote sensing to compensate for load-lead effects; eliminating noise from low-level measurements, using constant-current load with foldback power supplies; and characterizing ac inrush current. For a free copy, contact HP at (800) 452-4844, ext. 5421; Internet: http://www.hp.com. Be sure to request Literature #5965-8239E.

International Rectifier's (IR) new CD-ROM gives designers a tool to review the company's product and specification details. Designers can gather all the information they need, including nearly 600 data sheets; a product catalog; technical papers, including application notes and design tips; listings of worldwide distributors; IR sales offices and manufacturers representatives; and a free copy of Adobe Acrobat Reader. The free CD-ROM can be requested by contacting Carol Gajdos, IR Literature Dept., fax (310) 252-7171; e-mail: cgajdos1@irf.com. When requesting the CD-ROM, the desired platform must be specified (Windows 3.x, Windows 95, Windows NT, or Macintosh).

OZ Tek Inc.'s "Guide to Selecting IC Package Test Products" provides reference information for those involved in the quality assurance testing of standard and custom IC packages. Included in the guide is detailed information on test interface products such as sockets, receptacles, probes, adapters, burn-in interfaces, VLSI tester interfaces, plus a test configuration diagram showing how the various test products interconnect between the IC package under test and the test system. For a free copy of the guide, contact OZ Tek Inc., 3387 Investment Blvd., Hayward, CA 94545; (510) 782-2654; fax (510) 782-2656.

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Carlyle Taylor { *V.P. of Operations, Radiant Systems, Inc.*

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READER SERVICE 134

INTERNET NEWS

Given the international flavor of the Internet, it should naturally follow that people from all ends of the world ought to be able to access information at the same rate and quality as their counterparts on the opposite side of the Earth. Not true. One of the biggest complaints from Internet users everywhere is that their access is cut off at midstream.

To solve that problem and increase the speed of data traveling from one end of the connection to another, companies often virtually mirror their site. Mirrored sites are basically extensions of the original site that are set up in another location (often in another country where the company does business). These sites allow a more local access for users, cutting down the number of point-to-point connections between the user and the site being visited. The end result is faster transfer of data and more reliable transfers.

One company that's been capitalizing on this virtually mirrored site design is National Semiconductor. The company went to Digital Island (*http://www.digisle.net*), a global private network provider, to tighten up their Internet, intranet, and extranet services. Digital Island mirrored (what they call "overnet") National Semiconductor's Internet site in 16 countries.

It cost the company $4.0 million to install mirror sites in 10 countries. The fee for using Digital Island's global applications network is $400,000. Just in case you're really a stickler for numbers, National's site has over 40,000 pages of content, featuring over 27,000 products. And, visitors download about 10,500 data sheets and order 2,600 sample parts per day from the National site.

Digital Island used a distributed-star architecture, speeding up the access time for National's site visitors. Previously, the company had complaints of unreliable data transfer, specifically in the categories of sample ordering, technical manual downloads, and small-quantity ordering. The private network combines a single-hop architecture with an Internet applications engine.

Another interesting concept that seems to have yielded yet another industry buzzword is extranetting. In the case of National Semiconductor, the company embeds its Internet site into the intranet of its customers. This set up allows the company's customers worldwide to access National's product information without having to contact National's site and researching through it, or contacting the company's sales representatives. Essentially, the process is designed to save time.

National also uses a private extranet for its sales force and distributors. They have access to the company's technical information, sales materials, the latest pricing and incentives, and design opportunities. The sales force can monitor customers' interests worldwide via an analysis tool called Insight, from Accrue. Then, the company distributes the information throughout the private intranet via the Advisor. The Advisor is based on Lotus Notes Domino.Broadcast technology.

For more information on these developments, contact National Semiconductor Corporation, 2900 Semiconductor Dr., Santa Clara, CA 95052-8090; (408) 721-5000; Internet: http://www.national.com.

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All Power Trends' converters are available in surface-mount as well as through-hole versions. And you'll save more precious board space because our DC/DC converters are among the smallest in the market with footprints of only 1.9 square inches for the 3 - 7W converter pictured above and 2.3 square inches for the 15W converter. Power Trends' converters also support -40° to +85°C operation with 1500V isolation.

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Product Selector Guide

	Outputs		Input Voltage Range	
Power	Vo	Io	18 - 40V	36 - 75V
3W	2V	1.5A	—	PT4201
5W	3.3V	1.5A	PT4205	PT4202
6W	5V	1.2A	PT4206	PT4203
6W	12V	0.6A	—	PT4204
7W	+5V / -5V	1A ea	—	PT4301
7W	+5V / +3.3V	1A ea	—	PT4302
15W	3.3V	4.5A	—	PT4110
15W	5V	3A	PT4104	PT4101
15W	12V	1.2A	PT4105	PT4102
15W	15V	1A	PT4106	PT4103

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WRH

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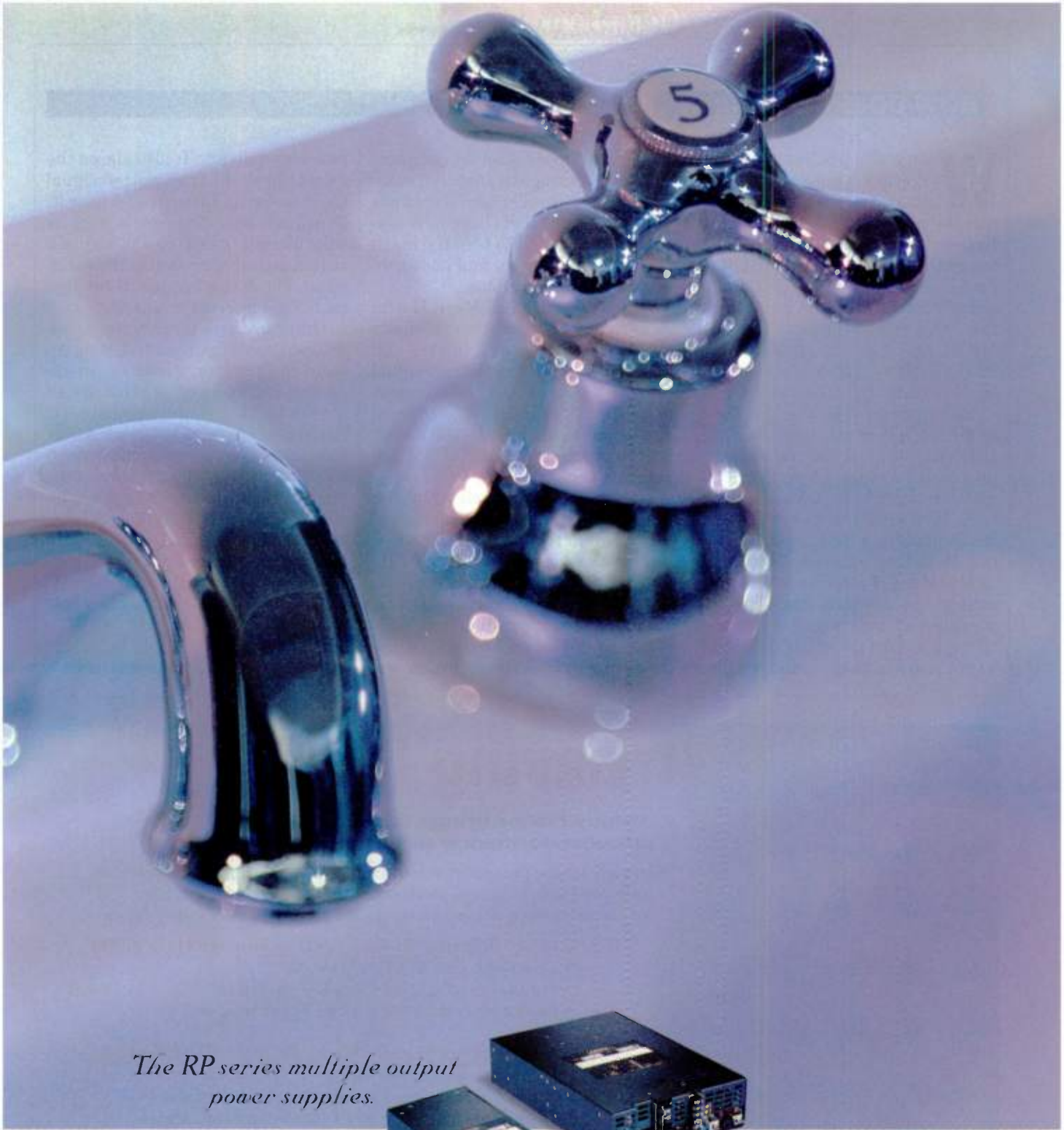
The RP series is the only power supply of its kind that complies with the EMC directive for CE marking, *and* comes with worldwide safety approvals including UL, CSA and TUV.



The RP series multiple output power supplies.

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READER SERVICE 177

HOW DOES IT SOUND?

When audio professionals put together a studio, there are usually two lists: the wish list and the need list. Often things like Synclaviers go on the wish list (due to price and/or availability), but as prices decrease and needs change, sometimes the wish-list items make it down to the need list. The DBMAX, Digital Broadcast Maximizer Mark II, is an example of a wish item that has made it to the need list.

It's capable of functioning in three different, but connected functions. DBMAX works as the transmission processor, dynamic equalizer, and mastering tool in broadcast applications. It also features 24-bit ADC and DAC converters. The Digital Broadcast Maximizer retails at $3995.

The Mark II includes a hardware analog-signal bypass function. This function allows signals to pass through, even if the unit is turned off. There also is a new equalizer with a multiband clipper function, compression and limiting, an adaptive automatic gain controller, and five bands of expansion. All of these new features are designed to help the maximizer with both pre- and post-production signal processing.

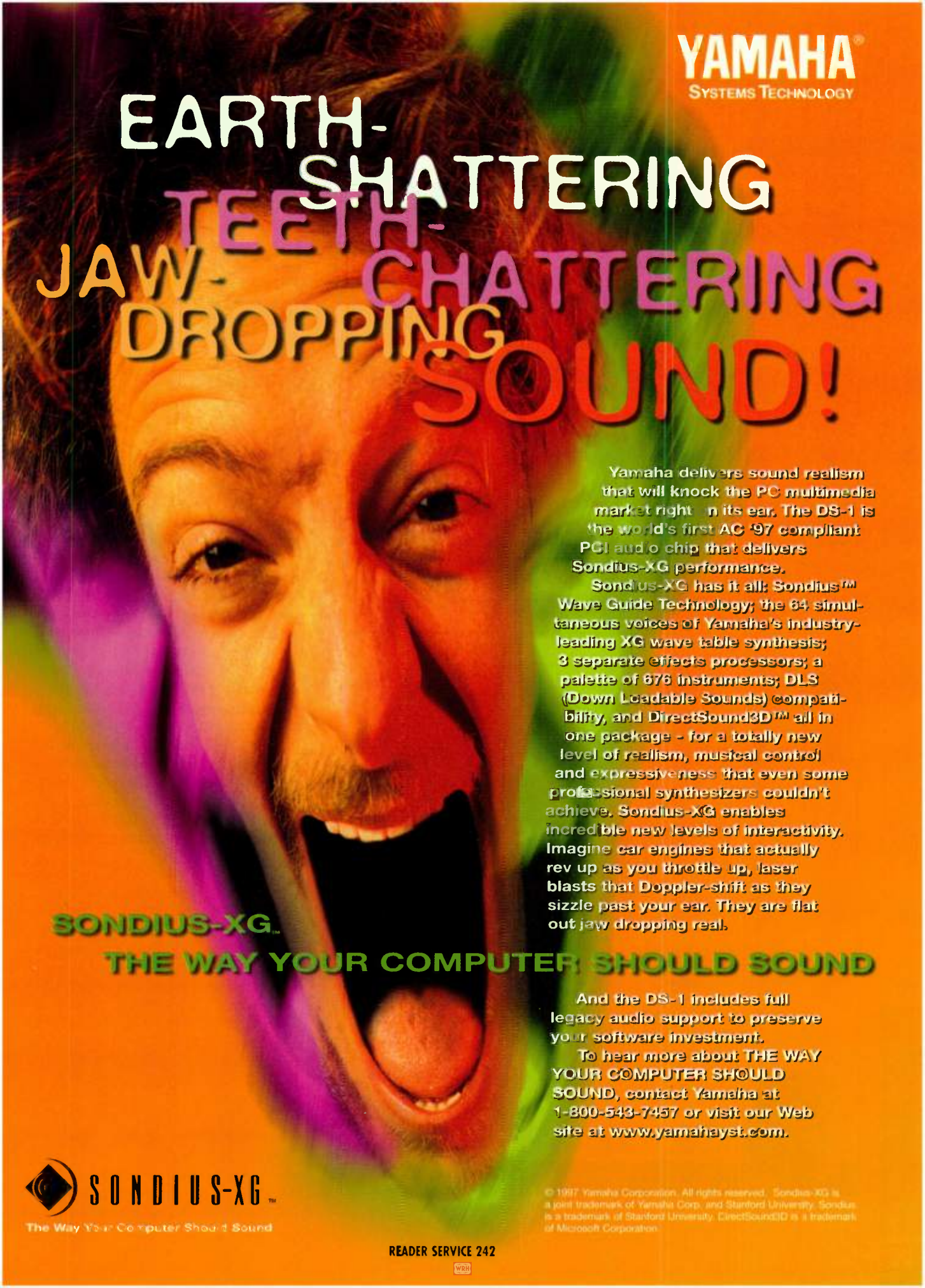
When the DBMAX Mark II acts as a transmission processor, it allows the user to produce a louder and more consistent signal. This signal leads to a larger area of audio coverage, especially handy in these days of expanding bandwidth. In this capacity, the processor is FM, AM, TV, and DAB compatible.

As a selective dynamic equalizer, the DBMAX serves to eliminate on-air problem frequencies. The frequency response is 10 Hz to 20 Hz +0/–0.2 dB. The dynamic range is >105 dB input and >96 dB output.

In broadcast productions, DBMAX Mark II works to beef up the mastering by providing a louder and punchier delivery. It also allows the user to hear the transmitted signal the way the audience would hear it. Broadcast-specific presets, such as commercials, news, music, and talk shows, are all optimized in the maximizer. The device handles 24-bit digital I/O and internal processing.

Other features include stereo adjust, automatic gain control, a three-band compressor, a limiter, an expander, and many others that are all able to be used simultaneously. TC Electronic's Wizard Program Assist function also comes with the processor, allowing easy identification of the presets. Digital inputs and outputs include: AES/EBU, SPDIF, and BNC World Clock Input. DBMAX only takes one rack space unit.

For more information, contact TC Electronic Inc., 790-H Hampshire Rd., Westlake Village, CA 91361; (805) 373-1828; fax (805) 379-7598; Internet: http://www.tcelectronic.com.—**DS**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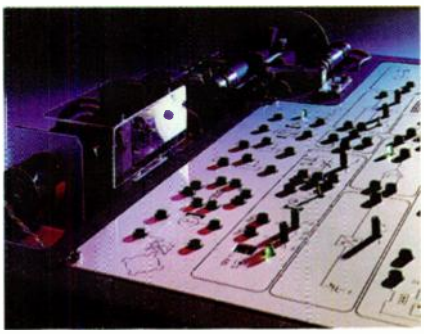
READER SERVICE 242
WRH

XTRA

Coming To Your Sensors

Sensor technology has become much more defined and prevalent in the last few years. In order to keep up with all the changes, professionals and students must have the proper tools to measure the characteristics found in the sensor's results. These individuals also need to be taught in a practical manner how the latest sensors function.

The first step in moving forward in sensor education is to shop around to examine the tools that are available. If a company's employees are willing to go back to school to study the latest developments in instrumentation, that company should make sure that the school has the most up-to-date equipment, and that the instructors are keeping themselves aware of the current and upcoming technologies.



One of the newest tools available to both companies and universities for sensor training is the Sensor and Instrumentation System (SIS) from TecQuipment. SIS includes a hardware unit that features 11 built-in sensors, an interactive CD-ROM, a dedicated textbook, automatic data-acquisition software, and student and lecturer guides. Parameters such as flow, height, level, position, pressure, proximity, speed, temperature, and volume can be measured using the SIS.

Following the recent trend of distance education, SIS was designed to be portable and easy to store. The hardware unit is completely self-contained, and features the most commonly used sensor types. Students also can develop combinations of sensors, signal-conditioning circuits, and power supplies in order to build working sensor circuits. The SIS tool is intended to help students and professionals fully understand the use of industrial sensors and their associated practices and techniques. Specific techniques include ac circuits and transformers, analog/digital systems, bridge circuits, comparative, optoreflective/ transmissive, passive/active, and potentiometric.

In the process of learning the technology, the individual using the system can use calibration graphs to see the effect of the the changes in each parameter on output of each sensor. By using these measurements, characteristics such as accuracy, deadzone, drift, hysteresis, lag, linearity, reliability, repeatability, resolution, and sensitivity can be examined.

After the experiments are completed, the student can then discuss comparisons between individual sensor performances. Importantly, errors can be checked and methods can be used to minimize their effect on output signal quality.

By making use of the interactive CD-ROM, the trainer can more effectively manage learning. If the student uses an oscilloscope or a PC with the experiments, data acquisition and control facilities can extend the range of capabilities of the SIS. The theoretical and practical experience of learning sensor technology in an interactive atmosphere promotes further experimentation, which eventually leads to the creation of new technologies.

For additional information on the SIS tool, readers should contact TecQuipment Ltd., Bonsall St., Long Eaton, Nottingham NG10 2AN, U.K.; 44 (0) 115 954 0140; Internet: http://www.tecquip.co.uk.—**DS**

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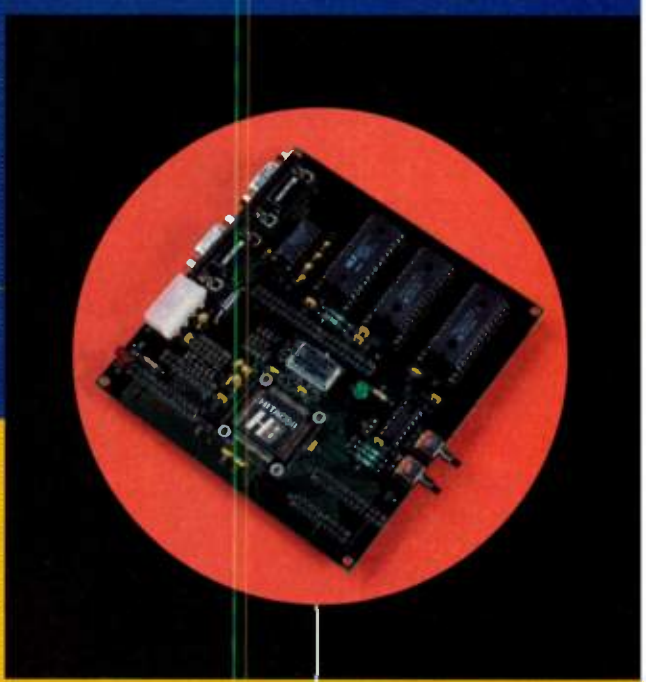

In today's hyper-competitive economy, nearly every single end-user product is being revamped to become more capable and user-friendly. If your job is to figure out how to do that, you may be asking some hard questions of your current system architecture.

Consider asking these same questions of an architecture that was developed for just this moment in time: the H8 line of embedded controllers. These 8- or 16-bit, register-based, RISC-like architectures offer efficient execution of high-level languages, record low power dissipation, an array of CPUs and large memories for complex programs. Choose from peripherals designed to enable today's target applications, including the industry's highest-density, on-chip flash for in-system programmability.

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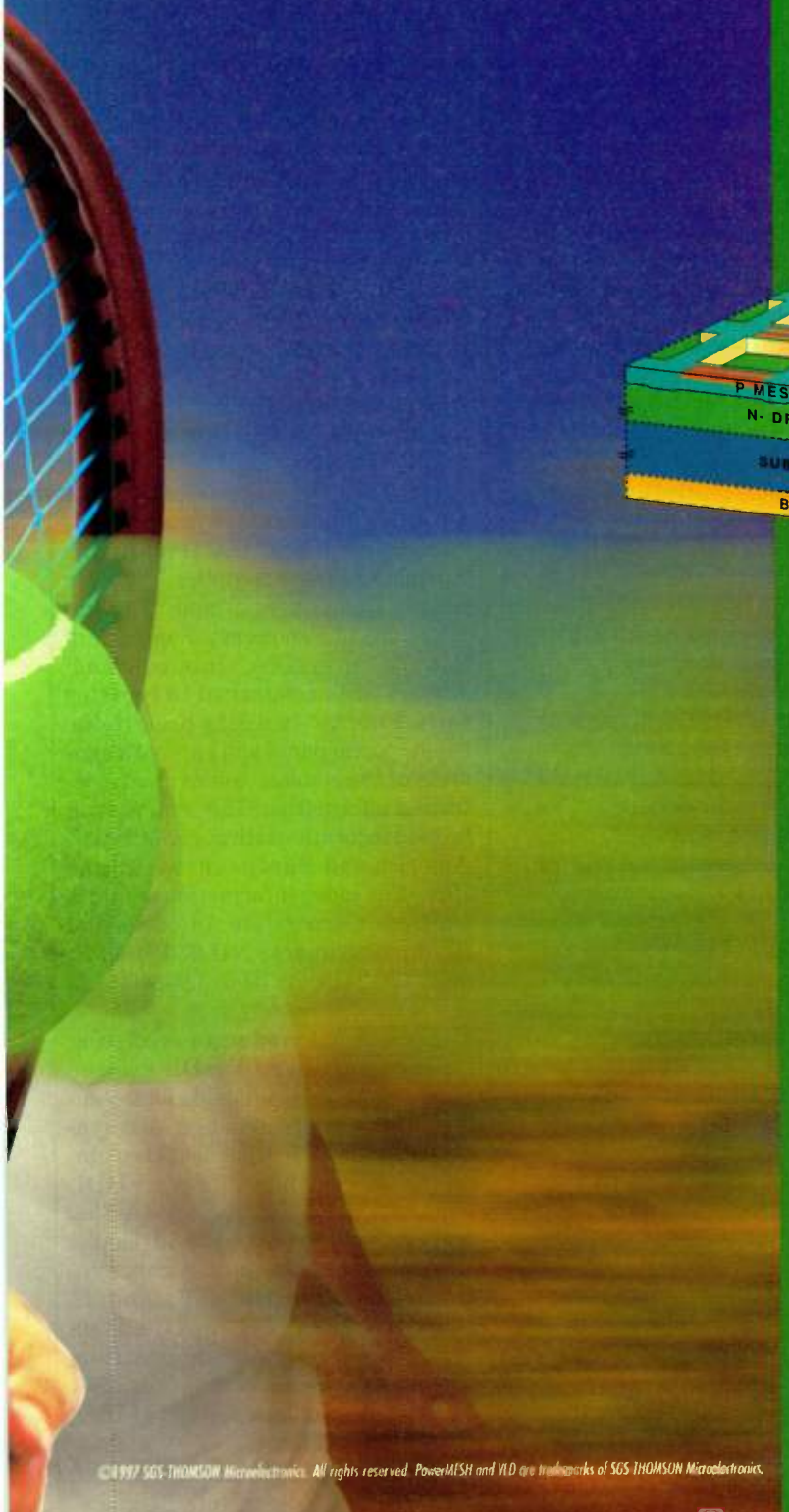
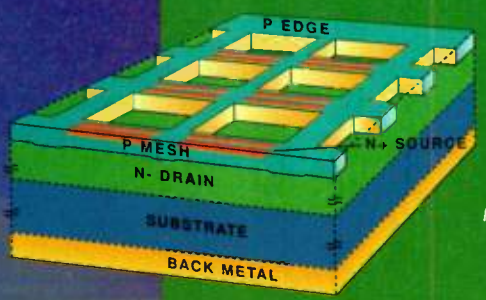


SGS-THOMSON introduces PowerMESH, the first significant improvement in PowerMOS technology in 20 years. Lower $R_{DS(on)}$ – even with a smaller silicon area – means lower conduction losses. Heatsinks can now be smaller, and power supplies can be more compact.



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EURO WATCH

ALFRED VOLLMER
FIELD CORRESPONDENT

Pasquale Pistorio, president and CEO of SGS-Thomson Microelectronics (ST), Stockholm, Sweden had a really great day this past September 18. Besides the fact that he and his wife gave birth to a daughter, Queen Silvia of Sweden presented him with the prestigious European Quality Award 1997 on behalf of the European Foundation for Quality Management (EFQM).

After accepting the award, Pistorio commented, "It is a great honor and reward for our company. This is not an award of methods, but an award of people. The most important issue is people."

The coveted European Quality Award honors total quality management and excellence in business performance. It has been granted annually since 1991 after a rigorous selection process by an independent jury of experts. It rewards companies that seek continuous overall improvement through implementation of the EFQM Model for Business Excellence.

ST is not the first semiconductor manufacturer to have won the prize. In 1995, Texas Instruments Europe won the EFQM award. One of the major reasons why ST won the award this year was the company's ability to coordinate processes within their manufacturing sites in Europe, Asia-Pacific, Africa, and the U.S., while it is financially headquartered in The Netherlands, with operational headquarters in France and the CEO's office in Switzerland.

The award ceremony took place at the Stockholm City Hall and was the culmination of a two-day quality seminar entitled "EFQM Forum for Business Excellence." And it wasn't just another one of those "meet and greet" conferences. Far from it. Attendance was staggering. Executives and leading employees of more than 600 European companies representing many aspects of technology made the trip to the Swedish capital to listen to speakers such as Carl Bildt, former prime minister of Sweden, Percey Barnevik, chairman of ABB, and Lars Ramqvist, CEO of Ericsson.

The topics discussed included issues regarding total quality management (TQM), quality assurance, and management. However, there were a few variations on the theme. For example, Per Grunewald, senior vice president of Elektrolux, and Franz Knecht from the Swiss Bank Corporation, gave an interesting lecture on "Growth Through Environmental Opportunities," where they explained that an environmentally friendly production not only pays off in moral values, but also in economics—an aspect that also was touched upon by Pasquale Pistorio.

When managers begin realizing that caring for the environment pays off in tremendous savings for the company, than you know it's a subject that's worth serious though. As a result, you will be reading quite a bit about "green engineering" in future issues of *Electronic Design* so you can keep up with the latest developments in this new area of technology. The new "GreenLook" column will provide you with the latest news on this exciting topic. And you'll be seeing a great deal of information coming from Europe, because the European sector of the industry is on the cutting edge of knowledge in terms of environmentally friendly design and production.

Alfred Vollmer is a correspondent for Electronic Design based in Munich, Germany. Readers may contact him via e-mail at Alfred_Vollmer@compuserve.com.

BACK TO SCHOOL

Learning Tree International is making available 10 new "hands-on" courses to interested students, along with their regular offerings of 100 multimedia computer-based training courses. Among the courses to be offered are "Visual C++ for C++ Programmers," "Introduction to Oracle8," "Windows NT 5 Workstation and Server," and "Developing and Managing Web Sites with Site Server." Courses are generally four to five days in length and will be held in various locations throughout North American through next April. For more information, contact Learning Tree International, 1805 Library St., Reston, VA 20190-9919; (800) 843-8733; fax (800) 709-6405; Internet: http://www.learningtree.com.

Unitrode Corporation is announcing its series of "Switching Power Supply Design Seminars." Among the topics for discussion are "A Unique Quadrant Flyback Converter," "Magnetics Design for Switching Power Supplies," "Power Supply Components," and "The Implications of Frequency Foldback in Power Conversions." Interested engineers are encouraged to register early. Four to six weeks prior to the event, participants will receive a synopsis of the seminar topics and registration information. The seminar will be held in locations throughout North America and Europe through June 1998. For more information, contact Unitrode Corporation, 7 Continental Blvd., Merrimack, NH 03054-4334; (603) 424-2410; fax (603) 424-3460.

Cypress Semiconductor is offering its first advanced VHDL classes taught by a programmable logic vendor. The design, simulation, and synthesis class will complement the company's series of introductory VHDL workshops. Registration fee is $99, and class size is limited to 30 people. Attendees are taught to write, synthesize, and functionally simulate source code for PLD and CPLD architectures. For more information, contact Cypress Semiconductor, 3901 N. First St., San Jose, CA 95134-1599; (408) 943-2600.

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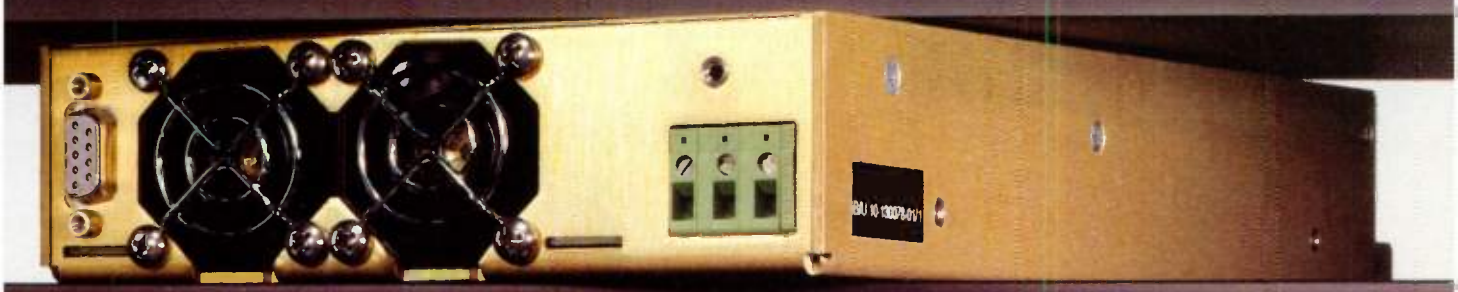
Up to 1500 Watts



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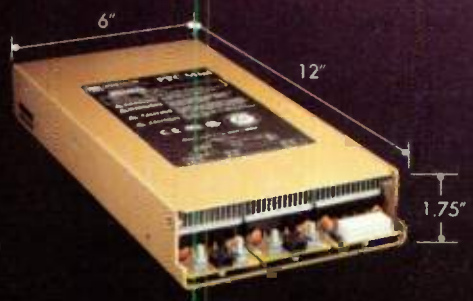
Off-line single phase input, Class B EMI, AC OK signal, enable/disable and sequencing interface. Powered by field-proven Vicor DC-DC converters, these units are factory configured for up to 6 outputs from 1 to 95 Vdc.



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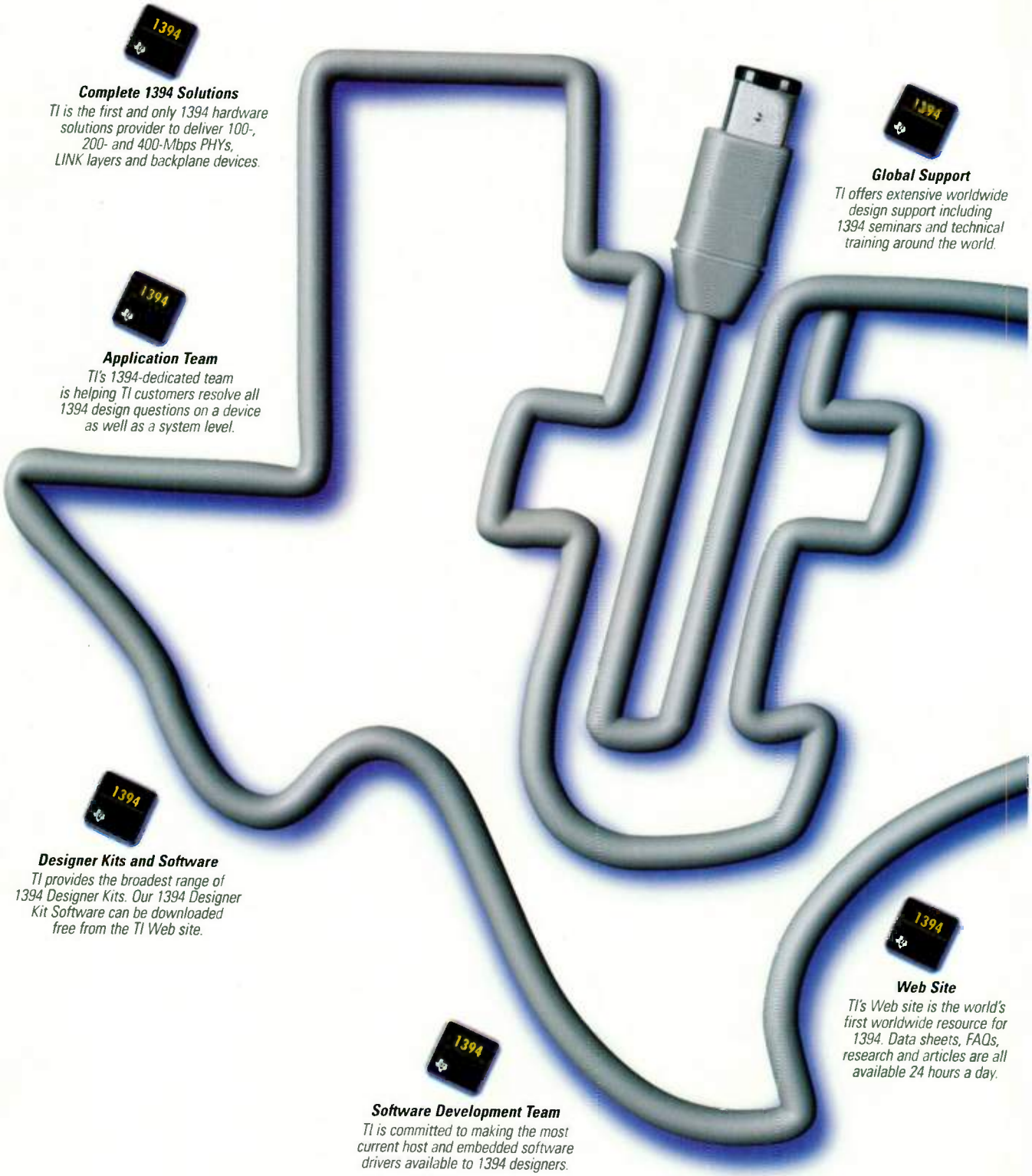

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TI provides the broadest range of 1394 Designer Kits. Our 1394 Designer Kit Software can be downloaded free from the TI Web site.

Web Site
TI's Web site is the world's first worldwide resource for 1394. Data sheets, FAQs, research and articles are all available 24 hours a day.

Software Development Team
TI is committed to making the most current host and embedded software drivers available to 1394 designers.

THIS JUST IN...

Data released by the Electronic Industries Association (EIA) reveals that U.S. exports of electronics equipment increased 10% in the first six months of 1997 over the same time period in 1996, reaching $74 billion.

As a result, the electronics trade deficit was reduced from $9 billion for the period year-to-date (YTD) June 1996 to $5.7 billion in 1997. From 1990 to 1996, electronics exports, as a percentage of total U.S. exports increased five percentage points to 22% in 1997.

Figures for the first six months of 1997 show that export sales have increased in every product category over 1996. U.S. exports of consumer electronics (CE), including domestically manufactured audio, video, and blank media products, increased 18% over YTD June 1996. The Asian and Latin American markets continue to account for a substantial portion of U.S. exports, comprising six of the top 10 export markets for consumer electronics. U.S. exports to Mexico, the second largest CE export market, have continued to accelerate since the recovery from the Peso crisis.

Improving on their already strong performance, the telecom market continues to thrive. U.S. exports of telecommunications equipment increased 19% in the first half 1997 over the same period in 1996. Major export markets for U.S. telecom equipment include Canada, Mexico, and Japan, which comprise 30% of total U.S. telecom exports. According to the EIA, the growth of the Internet and wireless communications along with the need to upgrade technology will fuel future growth in both domestic and foreign markets.

The largest increase of all the sectors was the area of U.S. exports of electron tubes, up 43% to just under $1 billion. Cathode ray tubes and computer display tubes accounted for the bulk of the increase.

In commenting on the first half figures, EIA President Peter F. McCloskey stated, "These figures demonstrate the vital role that exports play in the growing strength of our industry and of our nation's economy as a whole.

For more information on the study, contact the EIA, 2500 Wilson Blvd., Arlington, VA 22201-3834; (703) 907-7500; fax (703) 907-7501; Internet: http://www.eia.org.—**MS**

TIPS ON INVESTING

HENRY WIESEL
CONTRIBUTING EDITOR

If you think you're not wealthy enough to need an estate plan, think again. While you may not consider yourself wealthy, once you've accounted for your home, investments, jewelry, retirement account, and insurance policies, you may have accumulated assets that exceed the "Applicable Exemption" of $600,000 in 1997 (gradually increasing to $1,000,000 in 2006). And if you're worth over $600,000, you're subject to estate taxes that may range from 37% to 60%.

Combined with state taxes and income taxes on retirement plan distributions, your estate can be reduced by nearly 65% of its value (if the majority of your assets are in qualified plans or IRAs). Essentially, your heirs may receive only 35% of all you've accumulated. However, by following these basic estate planning steps, you may reduce this tax impact.

Prepare a will—A will is a testament to your life's work. Review it periodically so it keeps pace with changes in your circumstances as well as adjustments in tax laws

Use the Federal Unified Estate and Gift Tax Credit—The IRS gives each of us a tax credit of $192,800 in 1997, gradually increasing to $345,800 in 2006, to our beneficiaries free of estate and gift taxes. The Applicable Exemption can reduce your estate by the value of the property transferred as well as any subsequent appreciation on the property qualifying for the exemption.

Monitor retirement plan assets—Determine a strategy for dealing with the estate and income taxation of qualified retirement plans and IRA accounts. Seek advice from an attorney or a tax advisor.

"Gift away" what you don't need—If you have enough income from a certain portion of your holdings, consider a gifting program. Lifetime gifts to family members or other individuals can reduce estate taxes and shelter any asset appreciation. You may transfer up to $10,000 per person each year without incurring gift tax or reducing the Applicable Exemption; spouses together may gift up to $20,000 per person. (Gifts made to educational institutions for tuition or to medical care providers also are not subject to tax.)

Keep enough assets liquid to satisfy estate taxes—Generally, the IRS requires that any estate tax liability be satisfied within nine months of the date of death. There are four sources from which funds can be used to pay estate taxes: cash reserves, loans, liquidation of assets, or life insurance proceeds. Make sure your heirs won't have to sell investments because of a shortage of liquid funds.

Have a trustee of an irrevocable trust purchase your insurance policy—Usually, life insurance proceeds avoid probate and are exempt from income tax. But, they are subject to estate tax if you own the policy or have rights in the policy. Purchasing the policy within an irrevocable trust may prevent life insurance proceeds from being included in your taxable estate.

Meet with a Financial Consultant—Discuss your objectives with an advisor to develop an estate plan.

Henry Wiesel is a Vice President, Financial Consultant, and Qualified Pension Coordinator with Smith Barney. He may be contacted at 1040 Broad St., 2nd Floor, Shrewsbury, NJ 07702; (800) 631-3331, ext. 8563.

1997 EDA Market Study

The 1997 Electronic Design Automation (EDA) Study sponsored by *Electronic Design* magazine, provides critical survey information with a focus on EDA marketing executives and user/engineers. Conducted by the market research firm, EDA Today, L.C., results serve as strategic marketing opportunities for suppliers.

Survey results will present information on:

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- **Platform trends**
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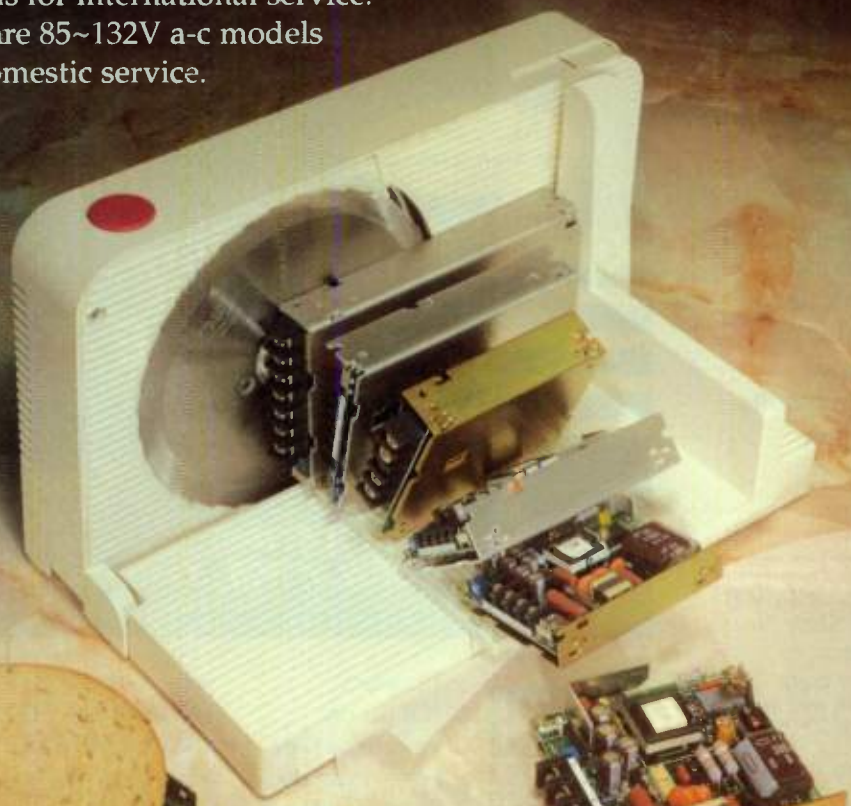
Kepco's FAW and FAK series skinny power supplies will fit your application. Available in ratings from 15~150 watts, these single-output models produce 5V to 48V of well-regulated d-c. The FAW are universal-input (85~264V a-c) models for international service.
FAK are 85~132V a-c models for domestic service.



This KEPCO product is backed by a firm **1-YEAR WARRANTY**

FAW/FAK POWER					
Nom. Volt	15W	25W	50W	100W	150W
5V	FAW, FAK	FAW, FAK	FAW, FAK	FAW	FAW
12V	FAW, FAK	FAW, FAK	FAW, FAK	FAW	FAW
15V	FAW, FAK	FAW, FAK	FAW, FAK	FAW	FAW
24V	FAW, FAK	FAW, FAK	FAW, FAK	FAW	FAW
28V				FAW	FAW
48V			FAW	FAW	FAW

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READER SERVICE 245

PIPS

- Power
- Interconnections
- Passives
- Switches & Relays
- Optoelectronics

Monitoring Lead-Acid Batteries In UPS Systems

Despite Much Research, There Still Is No Way To Monitor These Devices To Accurately Predict Their Inevitable Failure.

WILLIAM CANTOR, TPI, 24 Northbrook Dr., Suite A, Shrewsbury, PA 17361; (717) 227-0815; fax (717) 227-0621.

Large lead-acid batteries (>200 Ahr) are an essential component of any uninterruptible power supply (UPS) system. Unfortunately, these batteries have a built-in failure mechanism that will cause them to fail at any time over a two-to-15-year time span. The fact that they will fail is irrefutable. What remains up to the engineer is to determine the point when the battery begins to fail, and to plot a suitable course of action to prevent that failure from affecting system performance.

Unfortunately, the prediction of battery failure is not that easy and cannot be solved with a simple monitor. To date, there are no proven techniques, other than capacity testing, that can effectively predict battery capacity. Until a method is devised, there are several failure-related parameters that can be measured on lead-acid batteries to give some idea of that battery's state without subjecting it to a discharge test. The measurements fall into two distinct categories—preventative and predictive.

Predictive measurements are used to predict battery capacity. Measured parameters may include overall battery float voltage, ac ripple voltage, ambient temperature, or inter-cell connection resistance. Preventative measurements help the user prevent failures and increase longevity. Measured parameters include individual cell float voltage, individual cell temperature, or inter-cell (inter-unit) connection resistances (*see "Measurable parameters for preventative maintenance," below*).

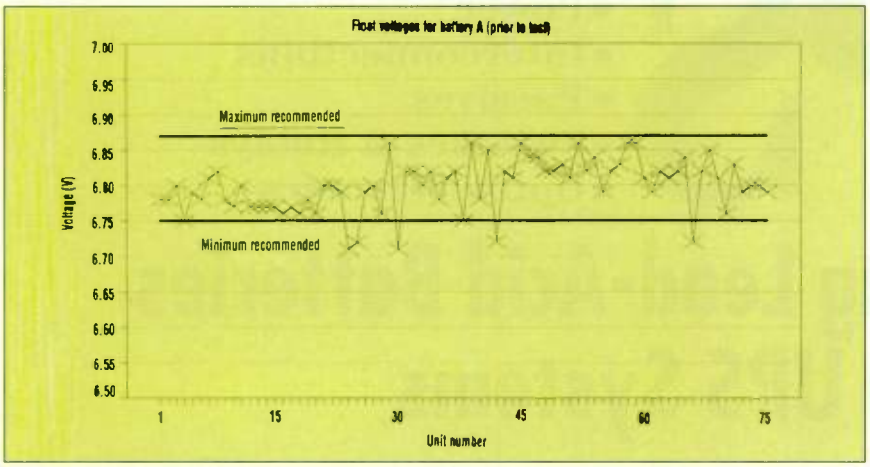
Battery life can be extended with the proper preventative maintenance, but they cannot be prevented from failing. Consequently, the predictive part of battery maintenance is much

Overall Battery Float Voltage—Overall battery float voltage is critical for battery longevity and to ensure proper charge. The float voltage should always be within the manufacturer's recommended range with respect to the battery temperature. Measurement of overall battery float voltage simply provides a continuous monitor of overall dc voltage.

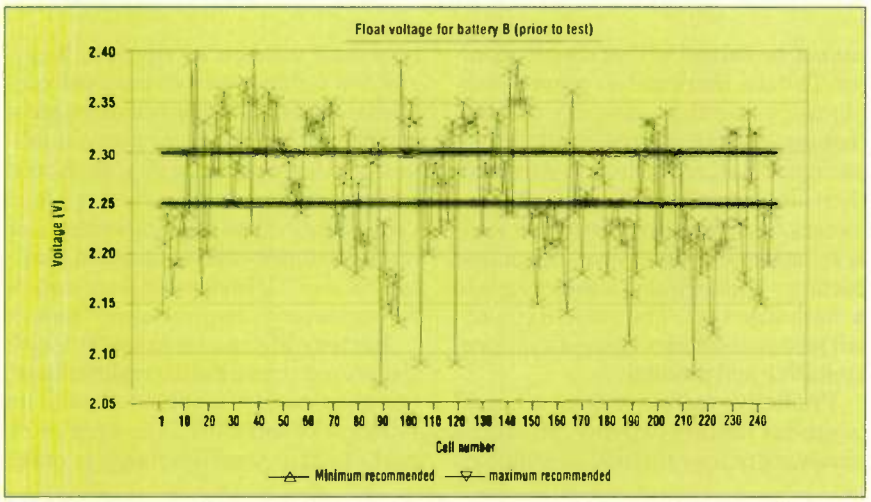
Ac Ripple Voltage—Excessive ac ripple voltage from the UPS system will cause the battery to fail prematurely. Although there is always some inherent ac ripple on the dc bus, certain levels can have a significant effect on battery life. Ac ripple voltage can be measured on the dc bus voltage.

Ambient Temperature—Temperature is critical to lead-acid batteries. High temperatures will reduce the life of the batteries, while cooler temperatures will reduce the capacity. If the temperature cannot be controlled, the float voltage may have to be adjusted with temperature changes. The temperature should be monitored in the direct vicinity of the battery in a central location to all of the cells.

Inter-cell (Inter-Unit) Connection Resistances—The most critical measurable parameter when it comes to preventative maintenance is inter-cell (or inter-unit) connection resistances. Since most UPS batteries are designed for high-rate, short-duration applications, these resistances have a significant impact on voltage drop and can affect the reserve time significantly. Since these systems can have currents over 1000 A, a high-resistance connection can heat quickly and may cause a fire. Monitoring these resistances may be somewhat difficult. Some of the large connections may be below 10 μΩ. A change of 5 μΩ may be significant, and any measurement needs to be at least this sensitive. The connection of the monitoring device to the post must be direct. A connection to the bolt on the post is unacceptable.



1. The simplest method of monitoring a lead-acid battery is to measure the float voltage (on-charge voltage) of each individual cell or unit. If the cell goes outside a preset limit, the cell may be failing. The float voltages for battery A are generally consistent, with only a few units slightly below the manufacturer's minimum recommended value.



2. It has been proven, however, that float-voltage measurement is not a reliable method of determining battery capacity. To illustrate this point, the float voltages of another UPS battery, battery B, were measured. Like battery A, battery B also was capacity-tested.

more critical. Although much effort has been put into measuring these parameters, each method has its faults to the extent that none can be relied upon to give a completely accurate picture of a battery's condition.

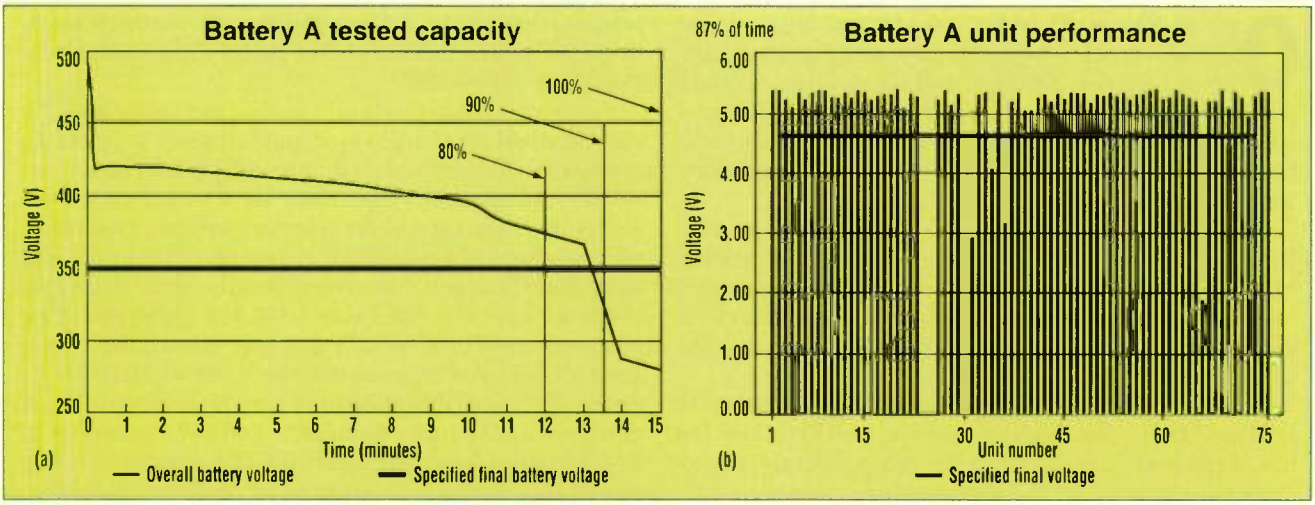
Predictive maintenance doesn't determine that the battery has failed, but instead determines when the battery is starting to deteriorate. Large battery systems usually cannot be replaced on a moment's notice. Even when they can, it is very expensive. The user must be provided with sufficient warning prior to battery failure.

In order to predict battery failure, the condition of the battery must be tracked over time to determine a negative trend. The failure point must be predicted and the user must be warned before the battery cannot support the load for the specified time, or before the battery capacity has dropped below a reliable value (typically 80% of rated capacity).

The simplest method of monitoring is to measure the float voltage (on-charge voltage) of each individual cell or unit. If the cell goes outside a preset limit, the cell may be failing. However, float voltage has been proven to be an unreliable method of determining battery capacity.

To illustrate this point, the float voltages of two UPS batteries, A and B, were measured *(Figs. 1 and 2)*. Both batteries were capacity-tested.

The float voltages for battery A are generally consistent, with only a few units slightly below the manufacturer's minimum recommended value.



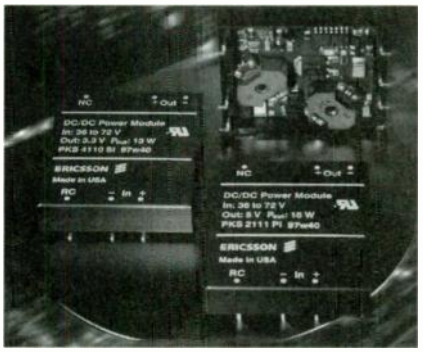
3. During the capacity test, all of the units were individually monitored and test results were generated for both the overall (a) and individual (b) cell performances, respectively. The voltage of three units was less than 0 V prior to the end of the test. This was not predicted by the float voltage.

PRODUCT FEATURE

Surface-Mountable DC-DC Converters Jump To 15-W Output

For many designers, the slow development of 10-W-and-above dc-dc converters that are compatible with standard surface-mount processes has been an ongoing source of frustration. Most in demand for distributed-power applications, the surface-mountable converter's progress has been hampered by the inability of standard pick-and-place equipment to handle the extra weight of the devices as they rise above 10 W.

Cognizant of this, Ericsson Components has introduced what it believes to be the first true surface-mount, 15-W, dc-dc converters. Designated the PKS SI line, the devices lower overall system cost by greatly increasing the number of applications that can take advantage of one-pass, fully automatic assembly and reflow soldering processes.



Key features of the devices include both 24- and 48/60-V inputs and a range of output voltages from 15 V down to 3.3 V. The 3.3-V output makes the PKS SI line particularly suited to high-end applications using advanced, low-voltage devices. Based on fixed-frequency switching technology, the converters have a transient response time of 200 µs and come in a package measuring 36.8 by 41.7 by 9.7 mm. With respect to thermal management, a ceramic substrate and a copper leadframe allow the devices to deliver the full 15 W without forced-air cooling or extra heatsinking in ambient temperatures ranging from –40° to 85°C.

Other features include automatic over-temperature shutdown, facilities for overvoltage protection, 1500-V dc isolation, built-in current limiting, and a reliability figure of four million hours MTBF at 40°C. Except for its surface-mount capabilities, the SI series is identical to the company's PKS PI series. Pricing is $37 each per 500.

Ericsson Components AB
Energy Systems Div.
164 81 Kista, Stockholm, Sweden
Stig Edwinsson (08) 721-6935
fax (08) 721-7001
eka.ekased@mesmtpse.ericsson.se
CIRCLE 465
PATRICK MANNION

Plug-And-Display System Combines Several Multimedia Functions Into One Connector

The MicroCross Plug-and-Display (P&D) connector from Molex combines the keyboard; mouse; game port; monitor; parallel printer; and DDC, USB, and 1394 serial communications into one single connector. The device offers design flexibility by allowing the display to be used as an I/O hub, thereby eliminating the wiring maze usually associated with multimedia systems. The connector also reduces cost by eliminating the need for two connectors (analog and digital) to support video I/O functions from the host system.

Fully compatible with VESA's P&D standard, the connector has a bandwidth of 2.5 GHz on RGB coax lines and will support rates of up to 2.0 Gbits/s on digital lines. Key features include full shielding and impedance control for RFI/EMI, a low-force helix contact design, and support for Transition Minimized Differential Signaling (TMDS) for video signals. Pricing for a right-angle, board-mount version in 30-µm gold is $2.00 each in quantities of 25,000.

Molex Inc.
2222 Wellington Court
Lisle, IL 60532

One-Million-Cell MOSFET Drives On-Resistance Down To 4 mΩ

To address high-current power-control requirements, Temic Semiconductor has introduced a 30-V TrenchFET with a maximum on-resistance ($R_{DS(ON)}$) of 4 mΩ. Able to handle up to 75 A, the device comes in either a TO-220 (SUP75N03-04) or D^2PAK (SUB75N03-04) package.

According to the company, only six of these 4-mΩ TrenchFETs are required in an application that typically required a dozen 8-mΩ devices. By eliminating the need to parallel MOSFETs, the TrenchFETs use less board space, reduce the number of interconnects, lower the cost of the board, and increase system reliability. Alternatively, the reduced on-resistance can be used to handle greater power with less heatsinking, again improving on reliability, cost, and space.

A key contributor to the new TrenchFET's performance is the use of an array of voltage clamps to control TrenchFET avalanche breakdown. The clamps improve on-resistance without sacrificing device ruggedness and help the device achieve a total-packaged resistance of 3.1 mΩ.

With the die resistance so low, Temic is focusing its future efforts on improving the packaging design to reduce the overall resistance even further. Pricing for the SUP75N03-04 and SUB75N03-04 is $4.36 each per 100,000. Delivery is eight to 10 weeks.

Temic Semiconductor
2201 Laurelwood Rd.
Santa Clara, CA 95054-1595
Joyce De Sorbo (800) 554-5565,
fax (408) 567-8995
http://www.temic.com
CIRCLE 467
PATRICK MANNION

Sealed and Unsealed Pendant Switches are rugged

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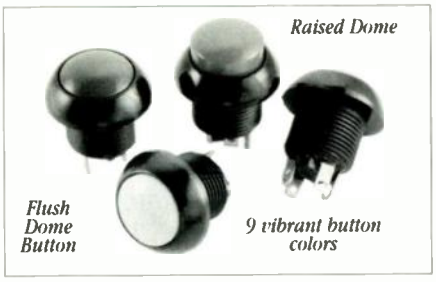

Colorful Sealed Contoured Dome Push Button Switches

Economical, all plastic button and housing, withstands extreme shock and vibration and features positive tactile feedback. Switches from computer level to 16 amperes.
Ask for OTTO P9 Dome.

READER SERVICE 96

Military & Commercial Grade Controls Grips

Series G control grips feature watertight sealed switches that withstand direct water spray and submission, with tactile feedback. Housing molded of non-reflecting, non-hydroscopic, rugged thermoplastic or cast aluminum, the housings withstand severe abuse. Controls current levels from computer level to 16 amperes.
Ask for OTTO Series G Grips.

READER SERVICE 97

Sealed & Unsealed Rocker Switches

Snap-in mounting fits industry standard panel cutouts for drop-in replacement. One & two-pole, standard & illuminated. Withstands extreme shock and vibration. Submersible to IP68. UV and solvent resistant. Switches to 16 Amps.
Ask for OTTO K series Rockers

READER SERVICE 98

Miniature & Subminiature Sealed & Unsealed Toggle Switches

Commercial and Military grades feature bat-handle, thumb, push-toggle; 2, 3, 4, & 5-way actuation; bushing or snap-in mount. Switches up to 16 amperes. Standard and custom. UL recognized and CSA certified.
Ask for OTTO T series Toggles

READER SERVICE 99

Stylish Push-button designed to survive in the wild, wet, hot, cold world!

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READER SERVICE 100

Miniature DC-DC Converter Outputs Up To 50 W

Measuring 0.42 by 2.4 by 2.3 in., the 50-W PicoVerter dc-dc converter module converts 48 V dc or 300 V dc to a single isolated dc output of 3.3, 5, 12, 15, or 24

V. Full power is delivered over the baseplate temperature range of –40° to 100°C. Nonshutdown overvoltage protection is provided, along with logic on/off, current limiting, and overtemperature shutdown. The devices use a fixed-frequency forward converter, and output voltage can be externally trimmed down to ±10%. UL, CSA, and TUV standards apply. Pricing is $95 each per 100.

RO Associates Inc., 246 Caspian Dr., P.O. Box 61419, Sunnyvale, CA 94088; Wayne Niederjohn, (800) 443-1450; fax (408) 744-1521; e-mail: wniederjohn@roassoc.com; Internet: http://www.roassoc.com/. **CIRCLE 468**

Compact, Configurable Power Supply Provides PFC

The PFC MegaPAC is a field-configurable, universal ac input, switching power supply with near unity power-factor correction. The supply has from one to 16 outputs and can output up to 1600 W from a package measuring 302.2 by 152.4 by 86.4 mm. Outputs are configured using standard Vicor components that are converted into ConverterPACs which slide into the MegaPAC chassis slots. Features include EMI/RFI filtering, output sequencing, an input power fail signal, an output power good signal, local or remote sense, and output overcurrent protection. Pricing is $0.75/W and delivery is eight weeks ARO.

Vicor Westcor Div., 560 Oakmead Pkwy., Sunnyvale, CA 94086; Vicor Express, (800) 735-6200; fax (508) 475-6715; e-mail: vicorexp@vicr.com; http://www.vicr.com. **CIRCLE 469**

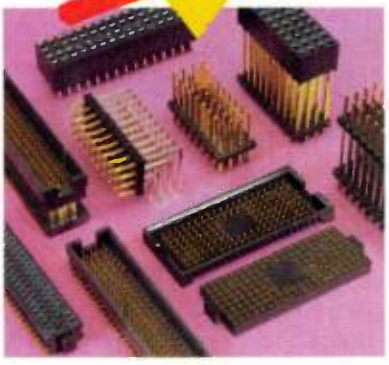
Miniature DC-AC Inverter Powers Backlit LCDs

The S Series dc-ac inverter measures less than 8 by 16 by 72 mm and is specifically designed for single-tube-backlit LCDs. The low-profile device comes with three dimming options—pulse-width modulated, resistive, and voltage controlled—and has an effi-

(continued on page 136)

WAY COOL!

Ultra High Density BOARD INTERFACE SYSTEMS



Samtec's multi-row interconnects on .025"(0,64mm), .050"(1,27mm) and .079"(2mm) pitch are *Way Cool* Solutions for increasing your board density. With Samtec Board Interface Systems we offer unique ways to go Card-to-Board, Board-to-Board and Off-Board...

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READER SERVICE 237

(continued from page 134)

ciency figure of 85 to 95%.

Endicott Research Group Inc., *2601 Wayne St., Endicott, NY 13760; Sales Dept. (800) 215-5866, ext.3011; fax (607) 754-9255; e-mail: sales@ergpower.com; Internet:http://www.ergpower.com.* **CIRCLE 470**

100-W Switching Supply Is Smallest To Date

Claimed to be the smallest open-frame power supply on the market, the VLT100 Series measures 3 by 5 by 1 in. and outputs up to 40 W. The supply is available with one main and three auxiliary outputs with various combinations of 5, –5, 12, –12, 15, –15, 24, and –24 V. Features include an efficiency rate of 87%, output currents of up to 12 A at 5 V, and line and load regulations of 0.3% and 1 or 5%, respectively. Other features include Molex connectors and

UL, CSA, VDE, and CE compliance.

Eos Corp., *906 Via Alondra, Camarillo, CA 93102; Alan Kashmola, (805) 484-9998; fax (805) 484-5854.*

CIRCLE 471

High-Rel DC-DC Converters Handle A Wide Power Range

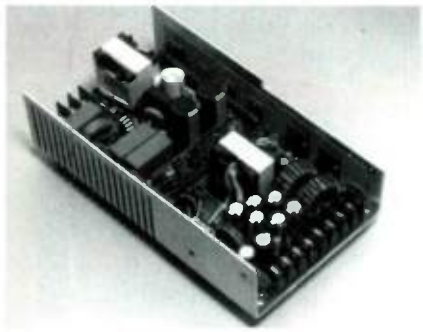
Designed for high-reliability applications, the NB series dc-dc converter has been extended to include 15-, 30-, and 45-W modules. Available with dual or triple outputs, the surface-mount devices measure 1.0 by 3.0 by 0.38 in., accept inputs of 14 to 40 V, and output 2, 3.3, 5, 12, or 15 V. Features include output voltage trimming, re-

mote on/off, and a fixed-frequency, flyback topology with an efficiency of greater than 80%. Pricing is below $120 in low quantities and delivery is from stock to 10 weeks.

Abbott Technologies Inc., *2727 S. La Cienga Blvd., Los Angeles, CA 90034; Sales Dept., (310) 202-8820; fax (310) 836-4926.* **CIRCLE 472**

300-W Supply Includes Power-Factor Correction

The UPF300 incorporates active power-factor correction to give a typical figure of 0.98. The supply also includes a universal input, measures 8 by 4.5 by 2 in., and includes an on-board FCC and



VDE Class B line filter. Each output can be configured for almost any voltage from ±2 V to ±48 V. Options include a power-fail/power-good signal. Pricing for a single-output version is $208, and for a dual-output model is $219, each per 100. Samples are currently available.

Digital Power, *41920 Christy St., Fremont, CA 94538-3158; Bruce Haug, (510) 657-2635; fax (510) 657-6634; http://www.digipwr.com.* **CIRCLE 473**

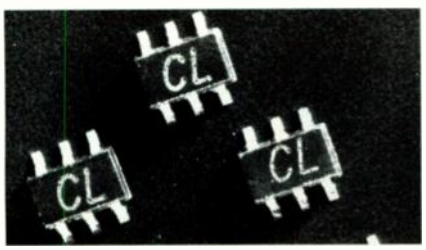
Low-Value Chip Resistors Handle High Power

The PLR1206, PLR2010, and PLR2512 chip resistors range in value from 0.010 to 1.0 Ω and are rated at 0.5, 1, and 2 W at 70°C, respectively. The operating temperature range is -55° to 150°C. The all-ceramic devices are compatible with automated assembly processes and target cellular, laptop, and other portable-equipment applications. Pricing is from $0.28 each per 10,000; delivery is from stock to five weeks.

IRC Inc., Advanced Film Div., *4222 South Staples St., Corpus Christi, TX 78411; Steve Wade, (512) 992-7900; fax (888) IRC-DATA.* **CIRCLE 474**

Diodes Come In SOT-363 Six-Pin Package

Targeting digital cellular and DECT handsets, Hewlett-Packard has repackaged its line of PIN and Schottky-barrier diodes in a SOT-363 (4.2 mm^2) six-lead package. Affected lines

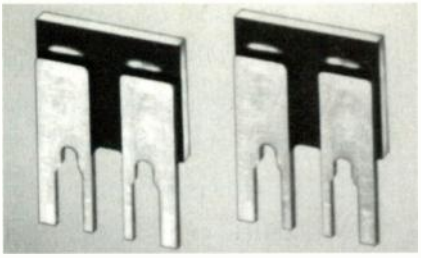


include the HSMP-389A PIN diode, the HSMS-280A, -281L, and -282A series diodes, along with the HSMS-285A line of Schottky-barrier diodes, and the -286A series of high-frequency, dc-biased, detector diodes. The -285A P-type diodes come with a maximum forward voltage of 150 mV at 0.1 mA, a typical tangential sensitivity of –56 dBm, and a voltage sensitivity of 40 mV/μW at 915 MHz. All diodes come in 100-piece quantities in anti-static bags. Pricing ranges from $0.33 to $1.46 each per 25,000.

Hewlett-Packard Company Inquiries, *5301 Stevens Creek Blvd., P.O. Box 58059, Santa Clara, CA 95052-8059; Sales Dept., (800) 537-7715, ext. 9968.* **CIRCLE 475**

Current-Sense Resistor Offers High Precision

The SR10 is a low-cost, 1%-tolerance,

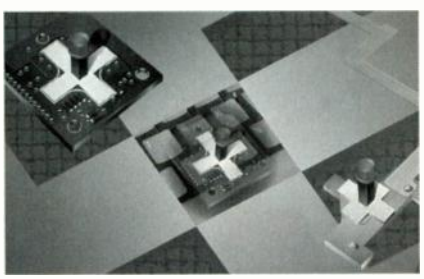


Kelvin-termination sense resistor that is rated at 1 W continuous at 70°C ambient. The device comes with heavy copper leads to maintain stable and cool operation at currents up to 11 A, with surge capability in excess of 600 A. The resistor comes in values from 0.008 Ω ±1% to 1.00 Ω ±1% with inductance values below 5 nH. Pricing for a 20-mΩ version is $0.59 each per 10,000; delivery is stock to seven weeks.

Caddock Electronics Inc., *17271 N. Umpqua Hwy., Roseburg OR 97470; Jim Skelton, (541) 496-0700, ext. 4538; fax (541) 496-0408.* **CIRCLE 476**

Multi-Axis Force Sensor Targets Computer Applications

Targeting computer applications, the the Aurora is a three-axis version of the company's line of multi-axis force



sensors. Available in two- and three-axis versions, this line of force sensors uses a sensing element comprising a ceramic substrate with a perpendicular post. As force is applied to the top of the post, the substrate microscopically deflects, producing strain couples in specific areas of the substrate. The magnitude of the strain in the X, Y, and Z axis determines the direction and rate of motion. Along with the Aurora, a robust, standalone version is available (Supra), as well as an Integrated Block design that combines the Aurora or Supra with the IBM Track Point or Track Point IV electronics and the Philips TPM 754 or 749 microprocessors in a single package. Pricing starts at $3.50, depending on the sensor version, cable length and style, and post height.

Bourns Inc., *1200 Columbia Ave., Riverside, CA 92507; Sales Dept., (909) 781-5070; fax (909) 781-5378; http://www.bourns.com.* **CIRCLE 477**

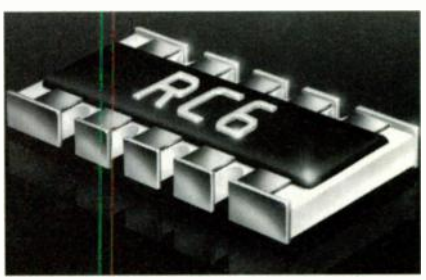
Resettable Fuses Protect USB-Equipped Systems

The PolySwitch RUSB line of resettable fuses provide overcurrent protection for USB-based computers and peripherals. The devices come with hold currents ranging from 1 to 2.5 A, low on resistance (0.140 W for the RUSB110), current-draw limiting to 5 A, and a maximum rating of 6 V at 40 A. Versions are available for self-powered and bus-powered individual port protection, as well as self-powered, ganged two-port protection. Pricing is under $0.30 each, depending on volume, and delivery is less than eight weeks ARO.

Raychem Corp., Electronics Div., *300 Constitution Dr., MS 110/7568, Menlo Park, CA 94025-1164; (800) 227-7040; Internet: http://www.raychem.com.*
CIRCLE 478

Thick-Film Resistor/Capacitor Arrays Form Low-Cost Filters

The Model RC6 thick-film resistor/capacitor networks come in a 2512-size chip array and form a low-cost filter-



ing solution for high-speed applications. The device comes in a 10-terminal leadless array with convex-type termination. The thick-film design minimizes crosstalk and damage from electrostatic discharge. Pricing is from $0.18 each per 100,000 and delivery is from six weeks ARO.

BI Technologies Corp., *4200 Bonita Place, Fullerton, CA 92835; Sales Dept., (714) 447-2300; fax (714) 447-2400; http://www.bitechnologies.com.*
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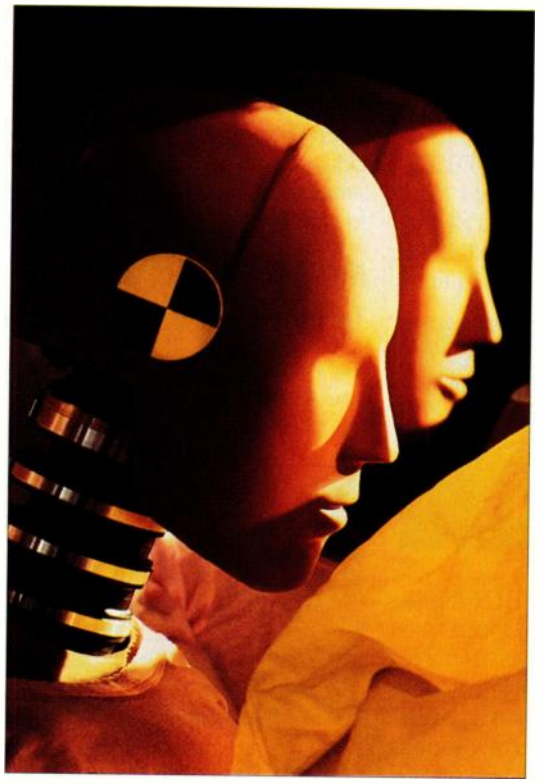

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READER SERVICE 115

STANDARDS WATCH

Standards Predicting Shouldn't Be "Dismal"

Michael Salameh, President, PLX Technology Inc.

Winston Churchill once called economics "The Dismal Science." Predicting the evolution and success of standards is an equally dismal and imperfect endeavor but, like practicing economics, it must be done. Many of us in the electronics business have to bet our companies on new emerging standards by developing systems, software, or ICs in anticipation of market demand. Accurate predictions and timely action on emerging standards have created enormously successful companies. On the other hand, failing to act until the success or failure of a standard is apparent also has destroyed many. To that end, I'd like to propose some guidelines for predicting the success of standards, and then apply them to one in particular, the I_2O architecture (Intelligent I/O).

I_2O is a standard message-passing architecture now being promoted by the leading suppliers of file servers, operating systems, and peripherals. It promises to dramatically improve the performance and scalability of servers, and also reduce the driver proliferation problem

The following guidelines may help in predicting the I_2O standard's success.

Guideline #1: To be successful, a standard must solve a clear, broad-based need. Five years ago, PCI was competing with VLbus to be the new high-speed PC interconnect architecture. VLbus had few silicon or architectural complexities, but it fell short because the improvements made to the PC were only marginal. Although PCI demanded an up-front silicon investment, it still won out because it addressed the pressing requirements of the PC world, such as performance, compatibility, and auto-configuration.

I_2O measures up well by this criteria. It solves the driver-proliferation problem that has long frustrated end users, operating-system vendors, systems suppliers, and peripheral makers. I_2O's improved scalability gives the PC-architecture servers an avenue to compete with proprietary high-end servers. I_2O also is attractive for high-performance embedded systems because it offers a sturdy and well-defined alternative to developing and maintaining proprietary message-passing protocols.

Guideline #2: Also known as "the 800-pound gorilla test." The early backing of one or more industry leaders greatly enhances the chances of success. The leader gives the standard credibility and momentum and provides early focus and consistency. VME had Motorola; PCI had Intel and Digital Equipment Corp. VLbus, by contrast, never enjoyed total support from a marquee name.

I_2O was architected by NetFrame in conjunction with Intel and Hewlett-Packard. The proof of concept and early versions of the specification were created by this group and a few others. What emerged was a well-considered, consistent, and focused specification backed by various industry leaders.

Guideline #3 (in contrast to #2): The standard must be open and free of domination by the 800-pound gorilla. Multibus II passed guidelines #1 and #2, but failed this one. By exercising to much control over the direction and implementation, Intel limited the adoption of Multibus II at the expense of the lower-performance but more successful open standard, the VMEbus. In recent years, however, Intel has been very creative in promoting subsequent standards such as PCI and USB. Intel gave these standards life and momentum by writing the initial specs, creating the proof-of-concept platforms, and rallying industry support. However, they were careful to transfer the specification's control to an open special interest group (SIG), thereby assuring the electronics world that specification evolution would be democratic.

I_2O also followed this model. After proving the concept, the pioneering group transferred control to the I_2O SIG, an organization that is open to any company.

Guideline #4: Success requires adequate enabling tools and components. System developers are more inclined to adopt the new standards if there's a sufficient variety of enabling chips, development systems, and software. PCI was well-supported early on by a variety of core-logic chip sets, peripheral chips, BIOS, bus-analysis systems, and software.

Last year, there were limited enabling options available for I_2O. However, a host of alternatives started appearing last Fall which give system developers many price/performance options. Now there are I_2O shells and real-time operating systems from Integrated Systems, PLX, and Wind River Systems. I_2O development tools are available for Intel, IBM, and Motorola RISC processors, and PCI and I_2O silicon is on the market. Three major network operating systems, Windows NT, NetWare and SCO Unix, are demonstrating I_2O.

In addition to the above, I_2O enjoys broad market appeal, industry-leader support, a democratic governing body, and the critical mass of enabling components and tools.

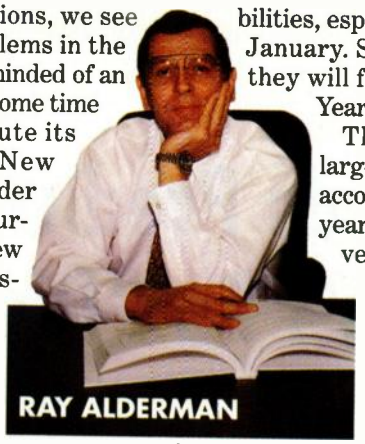
Y2K Problems In Embedded Systems

We've all read stories about the "Year 2000 (Y2K) Problems" with interest rate calculations at banks and insurance companies. But what effect will it have on embedded control systems, like PLCs, open-bus computer systems, or logic controllers? Nobody knows. It all hinges on hardware and software that use only the last two digits of the year in date-code calculations. We used two-digit year codes in the early days of microprocessors to save two lousy bytes of expensive memory when we were cramming our control programs into a 64-kbyte memory map on a Z-80 processor, and this convention continued when we went to 16- and 32-bit machines. Now it's coming back to haunt us.

How pervasive is this problem? Let's start by looking at some of the speculation concerning the basic utility companies—power generation and distribution, oil and gas pipelines, and telecommunications. The Electric Power Research Institute speculates that Y2K problems on the power grid could create a synchronized outage in North America that would make the recent blackouts in the West look like a glitch. The power grid is so tightly coupled that a tree falling on a power line in Oregon could cause havoc with power distribution in neighboring states. And it's not a simple matter of just restarting the systems. If the shutdown is caused by Y2K, we're deadlocked until that controller is taken off-line. There are thousands upon thousands of computerized control and monitoring systems hooked into the grid. Finding the culprit in a tightly-coupled system could be like looking for a needle in a haystack.

Another speculation is that the Alaskan pipeline will slow to a trickle on that fine New Year's morning of 2000. There are thousands of control and monitoring systems attached to that grid, too. But this time, the problem is worse. The oil in the pipeline is flowing under pressure across the frozen Alaskan landscape. As long as it's moving in the pipe, it doesn't gel because of the friction that is being created against the pipeline walls and the pressure in the line.

In telecommunications, we see the normal Y2K problems in the billing system. I'm reminded of an example I read about some time ago, but can't attribute its source. A family in New England bought an older home and moved in during the winter. Their new phone number was assigned, and the phone was connected within a few days. Immediately after connection, they began receiving hundreds of phone calls per week from an unknown location. When they picked up the receiver, they heard a series of clicks, but no voice on the other end.



The new homeowners contacted the phone company, who traced the calls to another house across town. Upon questioning by the "phone police," those residents denied making the calls and a search of the house was conducted, turning up a little black box attached to a float switch on an oil tank in the basement. The electronic controller inside was powered by the phone lines.

Before degree-day calculations were adopted by the oil companies to predict when customer's tanks needed filling, these controllers were placed on the tanks. When the float switch was activated, the black box would dial the number of the oil company and transmit a customer code requesting that oil be delivered. This older home had long been converted to natural gas and the tank was empty. The new homeowners across town had been assigned the phone number of the now-defunct oil company, and the float-switch controller was simply doing its job—requesting oil delivery. Everyone forgot that those controllers were still connected to the phone lines and would wake-up one day and pursue their programmed tasks.

I have no idea if these speculations and examples have any merit, but neither does anyone else. Almost everyone in the world is connected to these basic utilities in some manner, and a wide-ranging failure of these systems could create gigantic problems and liabilities, especially in the month of January. So we must find out if they will fail on this magic New Year's morning.

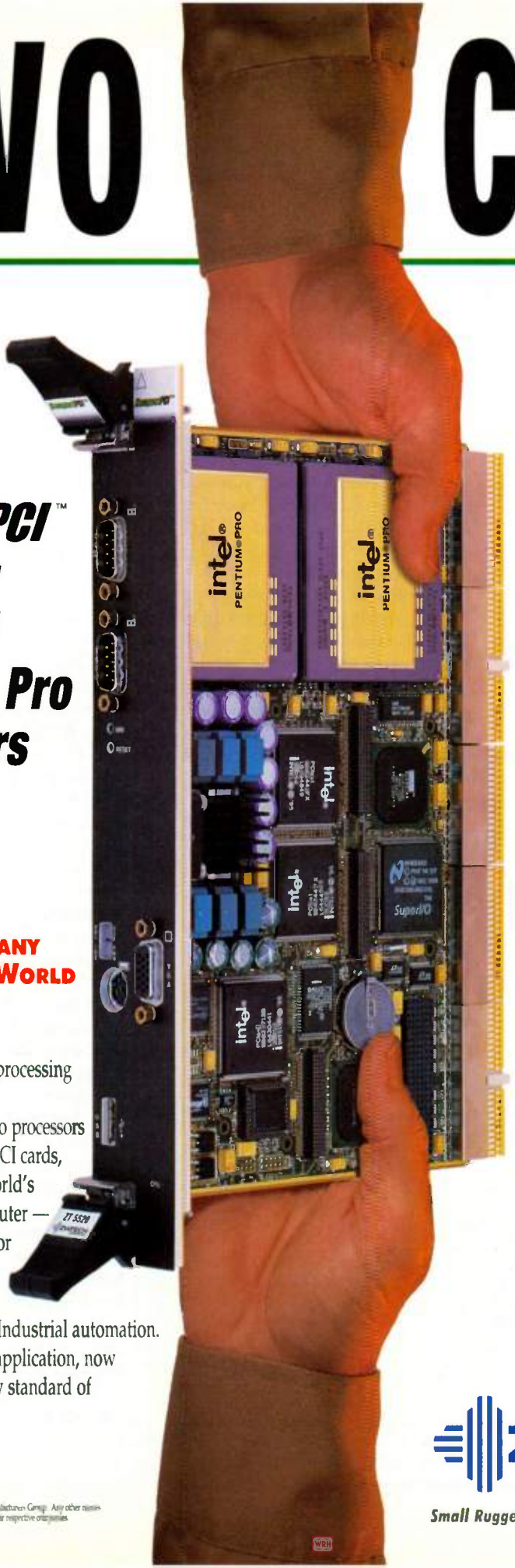
These utilities have a large and expensive job to accomplish in the next two years. First, a complete inventory must be taken of all embedded systems in their operation. Second, all control and monitoring systems that can have a catastrophic effect on services must be identified from that inventory. Third, those critical systems must be tested for Y2K problems and their potential effects. Fourth, those problematic systems must be fixed or replaced. And fifth, any changes to old systems and all new installations must be tested again to insure the Y2K problems are solved. There's no easier or cheaper way that I have seen to guarantee all these utilities will be operating properly on January 1, 2000.

So much for the engineering side of the equation. Now, let's look at the finances. The Electric Power Research Institute also speculates that the top 300 North American power-producing utilities will spend over $300 million collectively in the next 12 months taking inventory and testing their embedded systems for Y2K problems. Add to that another $300 million spent by the remaining 3000 small electric utilities, and the power industry could be writing checks for over a half-billion dollars chasing the Y2K gremlin.

Identifying and fixing the Y2K problems in embedded systems is a straightforward methodology. What concerns me is the little controller on the oil tank. How many small embedded boxes are still out there that we've forgotten about? In spite of all the time and money spent in the identification and correction process, one of those long-forgotten boxes could shut us down on that fine January morning. Keep your fingers crossed and hope that we've found all of them.

Ray Alderman is the Executive Director of VITA. He can be reached at exec@vita.com.

TWO COOL!



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How Much Universal Serial Bus Performance Do You Need?

Different Types Of Peripherals Require Different Levels Of Support And Performance. These Trade-Offs Determine The Device's Cost.

JEFFREY S. SCHAVER, Motorola Inc., 6501 William Cannon Dr. West, MS 0E50, Austin, TX 78735; (512) 891-6303.

By taking advantage of the Universal Serial Bus (USB), PC and peripheral manufacturers hope to improve the way the peripherals connect to and communicate with PCs. While using the USB technology in their products, designers are discovering that the cost of adding it to their existing product line can vary based on their particular USB connectivity requirements.

The USB supports automatic and transparent device configuration upon device attachment, and allows dynamic (hot) attach and detach to an already-powered system. In addition, the USB can supply a limited amount of power to devices connected to the bus, thereby allowing bus-powered devices. The official USB Specification Revision 1.0 is available from the USB Implementer's Forum, at their web site: *http://www.usb.org*.

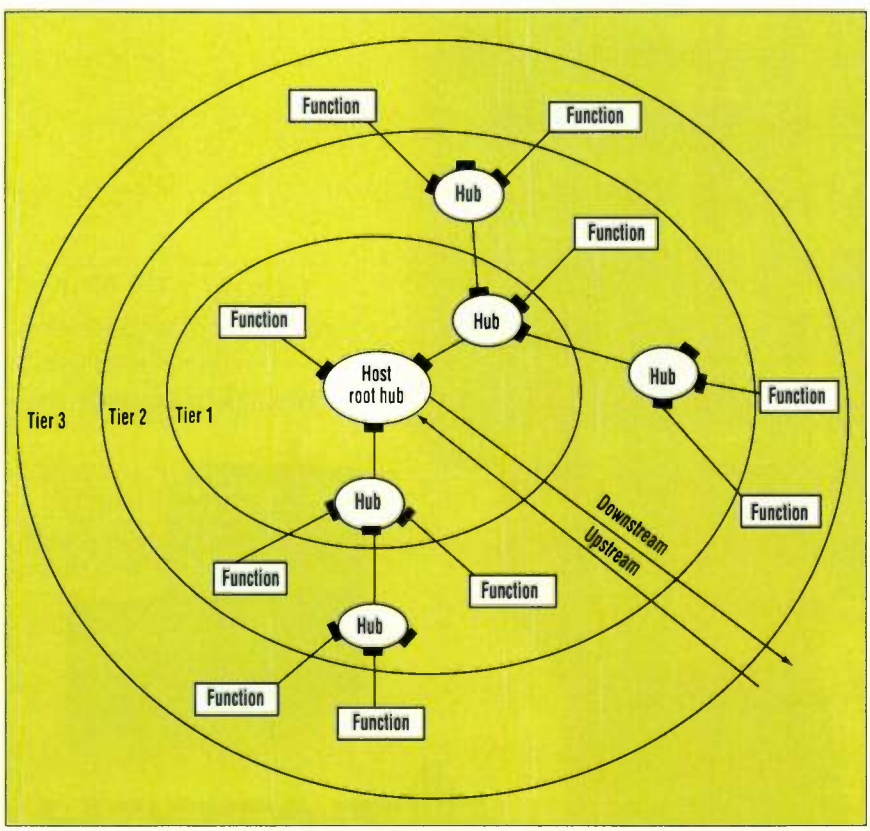
A number of new requirements in the PC industry drove the effort to develop the USB. One of the primary necessities was a better way to connect the PC to the telephone. This need was motivated by an ever-increasing demand for users to be able to move both voice and data from one location to another in a cheap and efficient manner. Another demand from the PC industry was for a standard peripheral connection that would be easy to use and consistent with the Plug-and-Play architecture. There also was a need for an expandable PC port, allowing connection of multiple of peripherals. In addition, the port had to be able to work well with peripherals requiring different bandwidths and data-delivery attributes.

Although USB operation appears simple to the end user (as it should), the underlying operation is more complex. A USB system consists of a host (the PC) with a root hub, interconnect, and devices. Devices consist of peripherals and hubs that provide additional USB connections. Hubs also can contain embedded functions.

The USB's physical topology is a tiered star with the host's root hub at its center (*Fig. 1*). The USB supports up to 127 peripheral devices with a maximum of five hub jumps from the host's root hub. Data can flow either from the host to a device (downstream) or from a device to the host (upstream).

Each device is dynamically assigned a unique address by the host upon connection to the bus during a process called enumeration. In addition, each device can have up to 16 sub-channels addressable by the host, called endpoints. Each logical connection between the host and an endpoint on a device (known as a pipe) is maintained independently of the others by the host. The pipes' attributes include bandwidth requirements, allowable data-packet payload size, transfer type, and whether communication with the endpoint is stream or message data.

The USB interconnect provides half-duplex serial communications between the host and devices at either 1.5 or 12 Mbits/s, depending on whether the host is communicating with a low-



1. The physical topology of the Universal Serial Bus (USB) is a tiered star. Data can flow either downstream from hub-to-function, or upstream from function-to-hub.

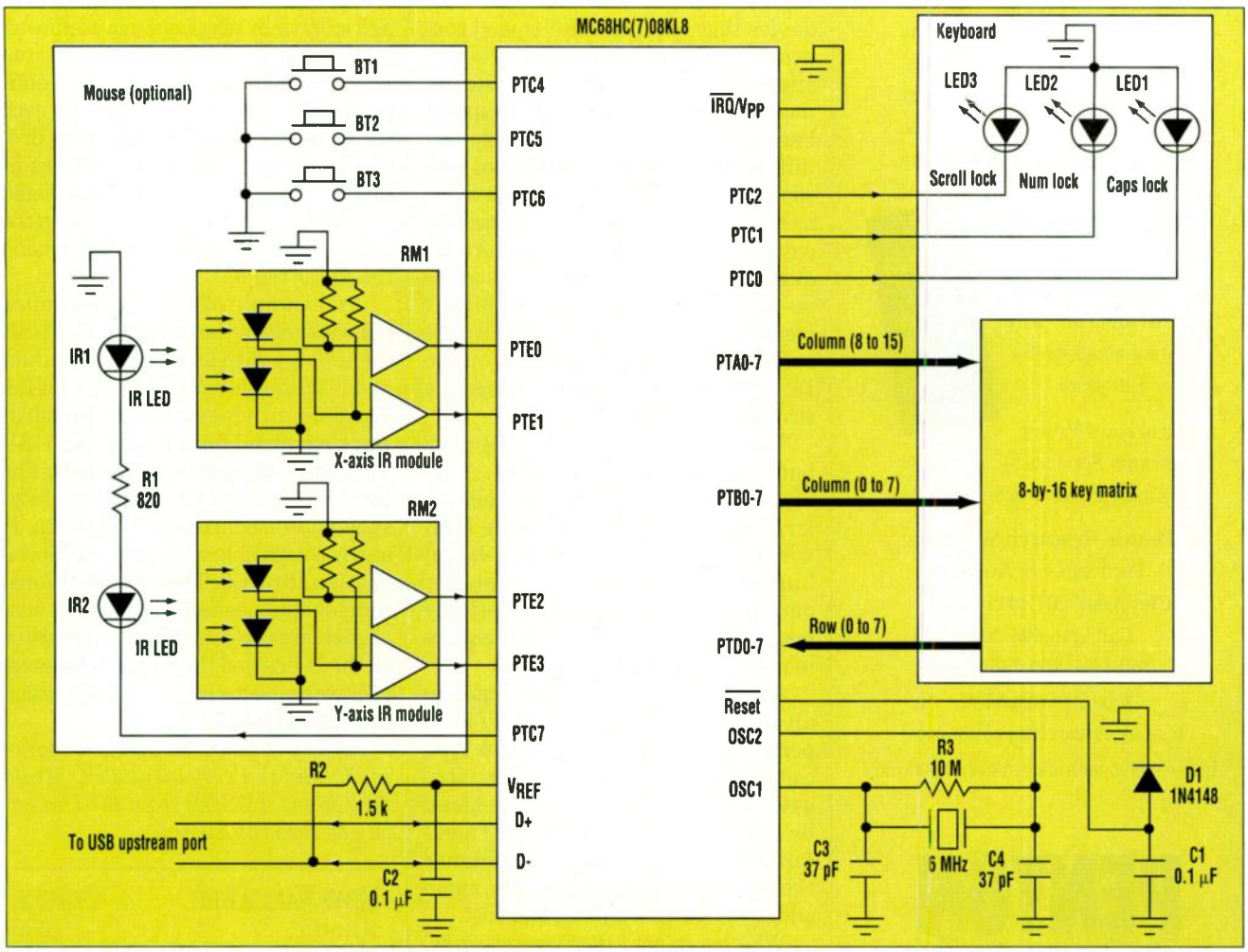
or full-speed device. Of the USB interconnect's four conductors, two are differentially driven between ground and 3.3 V, and carry data. One supplies a limited amount of power at 5 V to downstream devices that may require it, and the other connects to ground.

All transactions on the USB, including device configuration and data movement, are scheduled and initiated by the host and involve up to three data packets. The first (token) packet is always originated by the host. It is sent to a particular endpoint on a device, and describes the direction of the transfer, either host-to-device or device-to-host. The second packet consists of the data transfer, and is originated by either the host or device. The third is a handshake that's sent in the direction opposite of the data transfer. It lets the originator of the data transfer know if the data was received correctly. This transaction structure helps ensure that no data is lost.

A transaction can consist of only two packets. This transaction can occur when the host sends a token packet requesting data from a particular device's endpoint. Rather than having the endpoint reply with a data packet, it replies with a handshake packet that states that it has no data to transfer. It also can occur during certain time-critical transactions that require no handshakes, such as the transfer of digital-audio data. Additionally, built-in mechanisms such as cyclic-redundancy checks of packet fields, time-out recovery, and retry of certain transactions support robustness.

Above the transaction level, the USB supports four different transfer types: control, interrupt, bulk, and isochronous. Control transfers configure a device during its enumeration. Interrupt transfers send a small amount of data and need a guaranteed maximum latency for peripherals such as keyboards. Bulk transfers send a relatively large amount of data, but have no latency requirements and can wait for available bus bandwidth. Finally, isochronous transfers are employed by devices that require time-critical data and don't need transaction retry upon a delivery failure. Devices using isochronous transfers, such as digital speakers, are guaranteed a certain percentage of the bus bandwidth.

The host manages all access to the USB among devices within 1-ms units (frames). The host can allow up to 90% of a frame to be used by interrupt and isochronous transfers. All remaining bandwidth within a frame is divided up between control and bulk transfers. The host can dynamically change the allocation of bus bandwidth among devices from frame to frame. This feature is based on demands received from a peripheral's client software and changing



2. The MC68HC(7)08KL8 microcontroller, which integrates USB hub functionality, supports low-speed, non-isochronous USB data. Using the IC, a keyboard with an integrated pointing device can be built with the addition of only a 1.5-kΩ pull-up resistor and a 0.1-µF bypass capacitor.

device connectivity as the user attaches or detaches devices from the USB. When a device is attached and configured by the host, it communicates its transfer type and bandwidth requirements along with other configuration data to the host. The host then factors these requirements into its bus management. If a newly attached device requires interrupt or isochronous transfers and requests more bandwidth that is presently available, its access to the bus can be denied by the host.

One microcontroller or ASIC can provide all of the functionality required to connect most peripherals to the USB. But it can be more cost effective to implement an IC that supplies only the amount of USB technology that's required by the device—especially for peripheral makers in highly cost-competitive markets.

The cost of an IC with embedded USB connectivity can vary due to a number of factors, including speed. A device that requires a full-speed connection needs an IC that supports full-speed operation. They're typically more expensive than ICs that support low-speed-only connectivity. This cost difference is due to a number of reasons. Low-speed ICs can be built using a cheaper, lower performance technology and full-speed ICs may require additional sophisticated circuitry, such as on-board PLLs to operate at higher frequencies. These additional circuits require additional circuit area on the IC, which translates to increased die size and, ultimately, cost.

The size of on-board USB data buffers also affects an IC's cost. A device that must send and/or receive large amounts of data over the USB will need an IC with larger on-board buffers than a device with smaller data requirements. These relatively large on-board buffers also require more circuit area on the IC.

Another factor that contributes to an IC's cost is the number of supported endpoints. Each endpoint typically has a certain amount of circuitry associated with it that can't be shared by another endpoint on the IC. Therefore, the more endpoints, the higher the number of repeated circuits, again adding to the IC's die size and cost.

Whether or not a device needs an IC that includes hub functionality can significantly impact its cost. A hub repeater that manages connectivity between the host and downstream ports is needed on an IC that includes hub functionality. A hub controller also is needed on the IC that provides host access to the hub's control and status registers. Additional on-board transceivers also are needed for each down-stream port provided by the hub. Components that supply a means for the hub to manage power requirements on its downstream ports are required in a device with hub functionality, and must be factored into the device's overall cost.

A simple mouse or keyboard that has no hub functionality can operate using a low-speed connection with just two endpoints—each with a small 8-byte data buffer. This type of device requires a relatively low-cost microcontroller or ASIC with all of its USB functionality, as well as the majority of the circuitry needed to implement the integrated keyboard or mouse functions. Alternatively, a more complex peripheral such as a scanner or telephone can require an IC that supports a full-speed USB connection and a larger number of endpoints (with a large data buffer for each endpoint). In addition, any other processing power and/or circuitry traditionally required by such a device would potentially need to be integrated on the microcontroller or ASIC, again raising the cost of the IC.

An example of a microcontroller that can help in the integration of USB technology into an existing product line is Motorola's MC68HC(7)08KL8. The chip provides most of the hardware required for a low-speed USB connection needed by keyboards. The MC68HC(7)08KL8 supports low-speed non-isochronous USB data. It also is compatible with the USB Specification Rev. 1.0. The only additional components needed for the USB connection are the 1.5-kΩ pull-up resistor on the D-line and the 0.1-μF bypass capacitor connected to the 3.3-V regulator output pin (*Fig. 2*).

Jeffrey S. Schaver, an IC designer in Motorola's Personal and PC Media Div., holds a BSEE from the University of Texas at Austin.

How Valuable	Circle
Highly	530
Moderately	531
Slightly	532

LINEAR TECHNOLOGY

DESIGN NOTES

Maximize Dynamic Range with the LT1466L Micropower Rail-to-Rail Op Amp – Design Note 171

William Jett

Rail-to-rail amplifiers present an attractive solution for signal conditioning. For battery-powered or other low voltage circuitry, the entire supply voltage can be used by both the input and output signals, maximizing the system's dynamic range. Circuits that require signal sensing near either supply are straightforward to implement using rail-to-rail amplifiers. The LT®1466L dual and LT1467L quad combine rail-to-rail input and output operation with precision specifications. Requiring only 75µA of supply current, the LT1466L/LT1467L feature a maximum offset of 390µV. Unlike other rail-to-rail amplifiers, the input offset voltage of 390µV maximum is guaranteed across the entire rail-to-rail input range, not just at half supply. The resulting common mode rejection of 83dB minimum is much better than that of other rail-to-rail amplifiers. A minimum open-loop gain of 400V/mV into a 10k load virtually eliminates all gain error.

The following circuits demonstrate the LT1466L's rail-to-rail performance.

Variable Current Source

The current source shown in Figure 1 provides a near 0mA to 50mA output for a 0V to 2.5V control signal. Op amp A1 sets up a variable reference voltage referred to the positive supply; op amp A2 forces the voltage across the sense resistor (R3) to be equal to this voltage. Compliance of the current source is set by the supply voltage; the circuit will operate with voltages from 4V to 16V. The output resistance of the current source is greater than 10V/µA at full scale (50mA). Full-scale accuracy is set primarily by the resistor ratios. The V_{OS} of op amp A2 introduces a maximum error of 80µA or 0.16% of full scale.

High Side Current Sense Amplifier

The current sense amplifier shown in Figure 2 amplifies the voltage across a small value sense resistor by the ratio of the current source resistors (R2/R1). The LT1466L controls the low power MOSFET's gate voltage so that the sense voltage appears across current source resistor R1. The resulting current in Q1's drain is converted to a ground-referred voltage at R2. With the values shown, the output can be used to drive an ADC without additional buffering. Conversion gain is 2V/A. Resistor tolerances determine the gain accuracy; the V_{OS} of op amp A1 introduces an error of V_{OS}/R_S (2mA maximum with R_S = 0.2).

3.3V, 1kHz, 4th Order Butterworth Filter

The 4th order Butterworth filter shown in Figure 3 operates from supplies as low as 3V and swings rail-to-rail. The

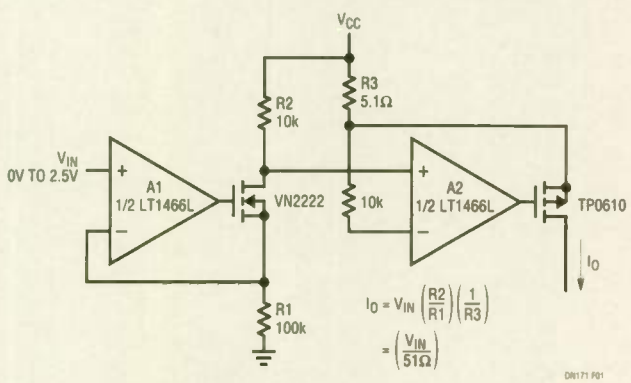


Figure 1. Variable Current Source

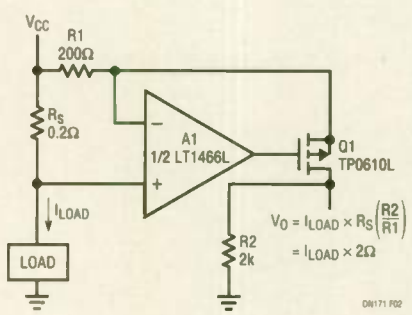


Figure 2. High Side Current Sense Amplifier

circuit has good DC accuracy and low sensitivities for the center frequency and Q. For amplifiers A1 and A3, the common mode voltage is equal to the input voltage, whereas amplifiers A2 and A4 operate in the inverting mode. Component values can be found from the following equations:

$$\omega_0^2 = 1/(R1 \bullet C1 \bullet R2 \bullet C2)$$

where:

$$R1 = 1/(\omega_0 \bullet Q \bullet C1) \text{ and } R2 = Q/(\omega_0 \bullet C2)$$

The DC bias applied to A2 and A4, half supply, is not needed when split supplies are available. The maximum output error is $2 \bullet V_{OS} + I_{OS} \bullet 42k \leq 930\mu V$. Total harmonic distortion (THD) with $V_{IN} = 1V_{RMS}$ and $V_S = 3.3V$ is 0.01% at 100Hz, rising to a 0.045% at 1kHz. Figure 4 shows the resulting frequency response.

Picoampere Input Current Instrumentation Amplifier

The instrumentation amplifier shown in Figure 5 features a typical input bias current of 200pA and includes a shield driver. Amplifiers A1A, A1D and A1C form a traditional three op amp configuration, and amplifier A1B both buffers the common mode voltage and cancels the input bias current of A1A and A1D. Input common mode range extends to within 300mV to 400mV of either supply.

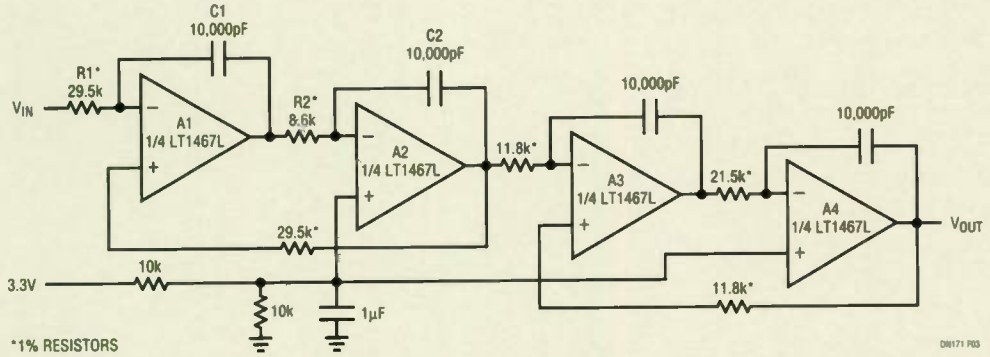


Figure 3. 4-Pole, 1kHz, 3.3V Single-Supply State Variable Filter Using the LT1467L

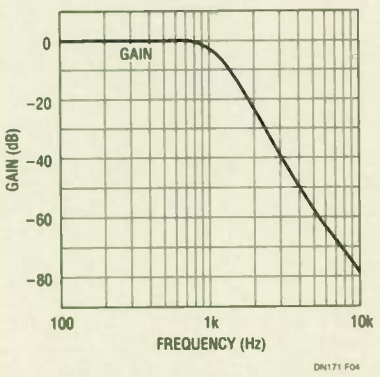


Figure 4. Frequency Response of 4th Order Butterworth Filter

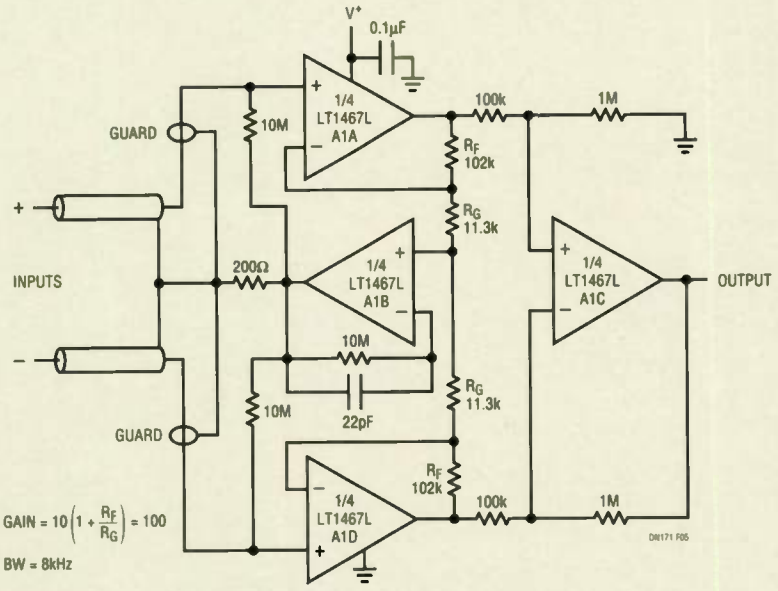


Figure 5. Instrumentation Amplifier

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WHAT'S ON BOARD

A USB controller that's fully compliant with the USB 1.0 specification has been added to the ASIC design library of Toshiba America Electronic Components Inc., San Jose, Calif. The core is fully verified and is a complete synchronous design capable of supporting the full speed 12-Mbit/s data-transfer rate. All standard USB commands are supported and the block also can handle one control endpoint and one bulk endpoint. The core ties into Toshiba's already available USB transceiver cells, and is flexible—it can find a home in computer peripherals, digital cameras, high-speed communications equipment, and many other products. The controller will initially be available in the company's 0.6-μm and smaller ASIC libraries (gate arrays, standard cells, embedded arrays, etc.) Supporting the core is a design kit that includes the synthesized netlist in Verilog or VHDL, test vectors, a product brief, and a reference guide. Contact Shawn Worsell at (800) 879-4963; Internet: http://www.toshiba.com/taec.

Platforms that ease the development of Windows CE hardware and software are springing up from multiple suppliers. VLSI Technology Inc., San Jose, Calif., offers both Hitachi SuperH and ARM RISC support, and Toshiba America Electronic Components Inc., San Jose, Calif., supports the MIPS processor family. The dual processor support offered by VLSI gives designers a choice between two popular RISC CPUs, each of which can be embellished with additional functionality using the company's ASIC design library to craft a highly integrated solution for the mobile, industrial, or consumer markets. In addition to the RISC cores, VLSI offers DSP cores, and various reusable circuit blocks for functions such as USB, 1394, IrDA, PCIbus, Ethernet, multimedia, graphics, 3D audio, and power management. And, to overcome the design problems when multiple processor cores are integrated on one chip, the company has created Vect, a multicore development system that lets designers craft chips that have two cores, such as a RISC processor and a DSP engine, operating asynchronously. A hardware development platform was developed by Toshiba for CE applications based on the TMP3912U, the latest member of the TX39 SystemRISC family of 32-bit RISC processors. The TX39 series was specifically developed for hand-held PC applications and operating systems. The reference board supports WinCE release 2.0 and includes all the hardware and software necessary to produce a complete Windows CE solution. Designers can evaluate the 78 MIPS RISC CPU, test user-specific hardware, develop new applications and drivers, and emulate and debug user code. The reference design has a typical operating power of 300 mW when operating at 74 MHz and 3.3 V. Included on the reference board are the CPU, memory, debug software, an LCD display, keyboard, power supply, microphone, speaker, serial ports (including IrDA), two PCMCIA slots, and an RJ-11 interface. Call VLSI Technology's Omer Wehunt at (408) 434-4000; Internet: http://www.vlsi.com; or Toshiba's David Barringer at (800) 879-4963; Internet: http://www.toshiba.com/taec.

Able to meet the performance requirements of the PC-100 specification for SDRAM in PCs, a family of memory modules with capacities of up to 128 Mbytes has been released by Smart Modular Technologies Inc., Fremont, Calif. The modules are designed around the 100-MHz memory bus specification and should work with the Intel's forthcoming 440BX chip set. The unbuffered DIMM modules are available in several memory-density options—32, 64, and 128 Mbytes, with the highest density version configured as a 16-Mword by 72-bit module for use in memory systems with ECC. To keep pace with the 100-MHz buses, the module's SDRAMs run in a standard two-bank environment and have a maximum of 10 ns to respond to either write or read requests, and provide 6-ns access, including all slew rates, clock skews, and flight times. The modules cost $8.50/Mbyte in OEM quantities. Call Bill Johnston at (510) 624-8104; Internet: http://www.smartm.com.

3U CompactPCI Card Holds PowerPC CPU

Designers of mid- to high-end, real-time systems can take advantage of the PowerCore CPCI-360x/-37x0 family of 3U CompactPCI boards. Built with a PowerPC microprocessor, the boards are suited for such applications as data and telecommunications and industrial controls. While the board operates with the PowerPC 603ev processor, it can be upgraded to a PowerPC 740. Features of the board include 8 Mbytes of on-board EDO DRAM (expandable to 128 Mbytes using a memory module), up to 4 Mbytes of flash memory, and compatibility with a host of real-time operating systems including Chorus/ClassiX, LynxOS, OSE, pSOSystem, VRTX, and VxWorks Tornado. The single-slot board is based on the company's modular PowerCore architecture which helps to reduce power. For example, with a PowerPC 603ev processor performing at 166 MHz, the board consumes less than 10 W of power, resulting in a cooler system.

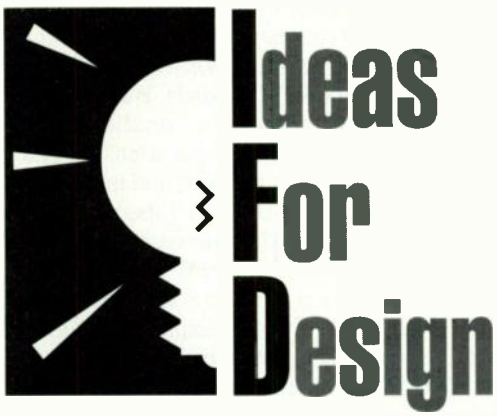
Force Computers Inc., *2001 Logic Dr., San Jose, CA 95124; (408) 369-6000; http://www.forcecomputers.com.*
CIRCLE 490

TCPR Low-Noise Read Channel Handles 200 Mbits/s

With the upward spiraling data-transfer rates in disk-drive interfaces, it's necessary for the read channels of those drives to keep pace. One way to do that is to employ the PCA8200, a PRML read channel IC that supports a data rate of up to 200 Mbits/s. The chip features trellis-coded partial response (TCPR) signal processing, which results in a 2-dB SNR improvement over traditional PRML. The architecture allows high recording densities while maintaining a high data rate and low error propagation. During operation, the device can be monitored using the channel-quality information. A high-speed test port is available for probing of various internal nodes. The PCA8200 is housed in an 80-pin MQFP. It sells for $8.50 each in lots of 10,000.

GEC Plessey Semiconductors, *1500 Green Hills Rd., Scotts Valley, CA 90144: (408) 438-2900; Internet: http://www.gpsemi.com.* **CIRCLE 491**

Got A Cool Circuit Idea?



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- Include schematics, charts, tables, code listings, etc.;
- Include name, company affiliation, address, phone/fax/e-mail

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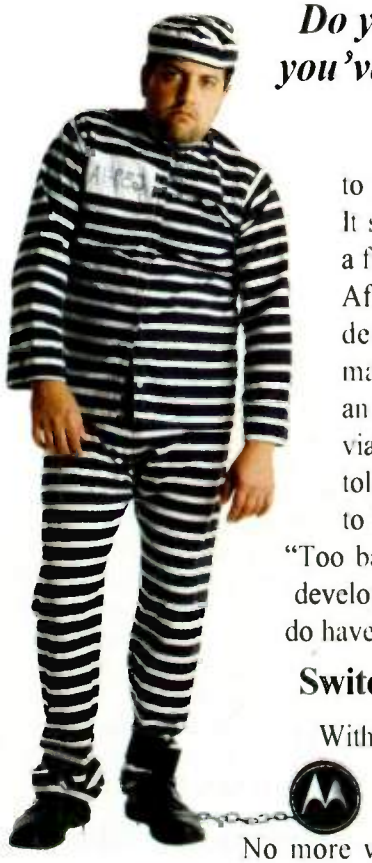

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Pointer Streamlines Portable PC Presentations

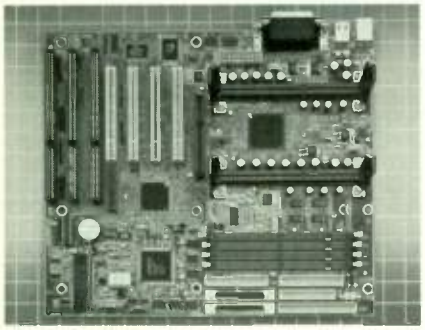
A wide range of cursor movement and precise control is available in the Grip Point, a handheld pointing device. Unlike a trackball or traditional pressure-operated pointing device, the Grip Point employs a navigation dome that

has a 30-degree range of motion (±15 degrees in all directions from the center of the dome) and a self-centering spring action. The user's thumb manipulates the navigation dome, while the left mouse button is operated by the index finger. The 55-g pointer comes with a 6-ft. cable with a mini-DIN connector. It's compatible with a Microsoft mouse driver. The Grip Point sells for under $40.

Fujitsu Takamisawa America Inc., *250 E. Caribbean Dr., Sunnyvale, CA 94089; (800) 380-0059; Internet: http://www.fujitsufta.com.* **CIRCLE 563**

Pentium II Motherboards Serve High-End Applications

The Intel 440LX chip set is at the heart of two motherboards designed for high-end networking, Internet server, and CAD/CAM applications.



The boards support the Ultra DMA 33 specification, pushing data-transfer rates up to 33 Mbytes/s and IDE-attached storage devices. The DPIILS2 and PIILS motherboards each integrate SCSI functionality directly on the boards. The former offers two Pentium II slots, while the latter can operate with one Pentium II processor, with CPU speeds ranging up to 300 MHz. In addition, the DPIILS2 offers dual Ultra Wide SCSI connections, allowing up to 30 devices to be connected. An Advanced Graphics Port (AGP) resides on each board, allowing for the connection graphics-intensive 3D accelerators. Using the four 168-pin DIMM sockets, system memory can range up to 1 Gbyte using EDO RAM or up to 512 Mbytes using SDRAM. The DPIILS2 motherboard sells for $699, while the PIILS model costs $399. Both units are available immediately.

Iwill USA Corp., *1542 Edinger Ave., #B, Tustin, CA 92780; (714) 258-4500.* **CIRCLE 564**

Low-Cost Chip Set Combines Modem And Audio Functions

Offering the flexibility desired by add-in board designers, the Rip-Tide chip set combines the functions of both PCI audio or modem chips. The chip set includes a full complement of modem functions, mainstream audio capabilities, and wavetable-synthesis features such as those needed for audio-intensive communications applications like 3-D multiplayer gaming and interactive music. RipTide supports all standard modem modulations including V.34 and K56flex, as well as Intel's Audio Codec 97 (AC97) 2.0 specification for next-generation PC audio and communications. The RipTide's codec also includes dedicated handset and microphone support, 3D spatialization and bass boost, and two-line modem support. As a result, it can be employed for personal communications, including e-mail, telephone answering machine, full-duplex speaker phone, simultaneous voice and data, Internet Phone, and Video Phone.

The scalable architecture permits placement on the motherboard, add-in cards, or custom form-factor designs. Legacy audio support (SoundBlaster) is included for mainstream audio applications. RipTide also features analog and digital joystick interfaces, an MPU-401 interface and game port, and sample-rate tracking ports. Driver support includes Windows 95, Windows NT 4.0 and WDM. Samples are available now, with volume production beginning in the second quarter. The basic two-chip solution costs $36 each in lots of 10,000 units.

Rockwell Semiconductor Systems Inc., *4311 Jamboree Rd., P.O. Box C, Newport Beach, CA 92658; (714) 221-4600; http://www.nb.rockwell.com.* **CIRCLE 565**

RAID Solution Optimizes Both Hardware And Software

By combining a tailored software environment with high-end hardware, the Catapult RAID solution can operate with a host of disk-array applications. The RAID software and PCI-to-UltraSCSI host adapter are scalable and portable across multiple operating systems, including DOS, Windows 3.1, Windows 95/NT, NetWare, OS/2, and various flavors of UNIX. Catapult supports RAID levels 0, 1, and 5, and features hot-swap and hot-spare functionalities, uneven striping, on-line capacity expansion, and dynamic caching. Catapult is scalable across multiple controllers, meaning that performance can be improved through host CPU and memory upgrades. The system accelerates disk I/O operations by reducing the number of driver layers an I/O command must go through before being accepted by a host adapter. For example, in Windows NT, Catapult offers a second entry point for a monolithic driver, thereby reducing three layers down to one, and ultimately reducing overhead.

Initio Corp., *2188-B Del Franco St., San Jose, CA 95131; (408) 577-1919; http://www.initio.com.* **CIRCLE 566**

Videoconference Over ISDN Under Windows 95 Or NT

Those using Windows 95 or NT for LAN- or ISDN-based videoconferencing capabilities need look no further than the Intel Business Videoconferencing 4.0. The latest version of this software, which takes advantage of the MMX technology, includes the ability to conduct Internet conference calls between companies with secure firewalls; to exchange high-resolution images in an album-like database; and control the

(continued on page 149)

(continued from page 148)
amount of bandwidth used in making a LAN-based connection. Intel Business Videoconferencing 4.0 complies with the H.320, H.323, and T.120 standards. The $1199 price tag includes the software, an audio-video board, an ISDN adapter, a camera, a headset with a microphone, and a desktop microphone with built-in echo cancellation.

***Intel Corp.**, 2200 Mission College Blvd., P.O. Box 58119, Santa Clara, CA 95052; (800) 538-3393 or (503) 264-7354; http://www.intel.com/proshare/conferencing.* **CIRCLE 567**

Fibre Channel Switch Supports AL, Point-To-Point Topologies

Simultaneous support for both arbitrated-loop (AL) and point-to-point network topologies is available from the AGS/8 eight-port Fibre Channel

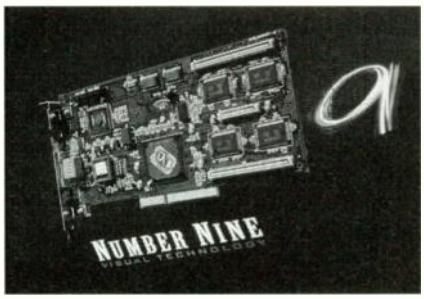
switch. Because the box employs a fabric architecture, switched storage isn't limited to a point-to-point topology. And, since all the ports support either direct fabric-attach or loop devices without any hardware upgrades, the switch can be configured with RAID or JBOD systems. Suitable applications include intranets, multimedia systems, visualization, transaction processing, and imaging.

The AGS/8 offers 1.063-Gbit/s full-duplex data-transfer speeds, low fabric latency, and support for all classes of Fibre Channel service, including Class 1, 2 (Internet protocol), 3, and Intermix. It also features environmental redundancy with N+1 fans and an optional power supply. User management can be handled with a web browser or a simple network management protocol (SNMP) console. AGS/8 boxes can be cascaded to increase the number of ports. Available now, the AGS/8 eight-port Fibre Channel switch sells for $2950.

***Arcxel Technologies Inc.**, 2691 Richter Ave., Suite 106, Irvine, CA 92606; (714) 475-4350; Internet: http://arcxel.com.* **CIRCLE 568**

Graphics Accelerator Can Handle 3D, 2D, and Video

Based on the company's 128-bit Ticket To Ride accelerator chip, the Revolution 3D graphics board combines high-performance 3D, 2D, and video capabilities. Supporting both Direct3D and OpenGL 3D protocols, the board han-



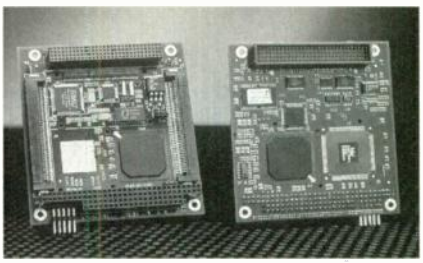
dles hardware texture-mapped triangles, 32-bit precision Z-buffering, fogging, specular lighting, dithering, and bilinear and trilinear filtering. The board also contains a 650-MFLOPS floating-point set-up engine, which is tightly coupled to the 3D drawing engine. Other features include 8 kbytes of texture cache and a 220-MHz RAMDAC. The standard configuration comes with 4 or 8 Mbytes of dual-ported WRAM, expandable to 16 Mbytes. The 4-Mbyte Revolution 3D board sells for $349, while the 8-Mbyte model costs $449. Both versions are available now.

***Number Nine Visual Technology Corp.**, 18 Hartwell Ave., Lexington, MA 02173; (617) 674-0009; Internet: http://www.nine.com.* **CIRCLE 569**

Pentium Module Fits Tiny Form Factor

The PC/104-Plus form factor, which measures 3.6 by 3.8 in., is still large enough to hold a Pentium microprocessor. The CoreModule/P5i contains all the functionality of an entire Pentium-based PC and is intended for use in embedded applications. Included on the module are a 133-MHz CPU, up to 64 Mbytes of DRAM, a battery-backed real-time clock, a parallel and two serial ports, an IDE interface, and a USB connector. The integration of both ISA and PCI buses lets designers employ off-the-shelf or custom expansion devices.

The CoreModule/P5i is built with



the ruggedness and reliability requirements needed for portable and mobile applications. The operating temperature ranges from –40 to +85°C (in the extended-temperature model), and shock and vibrations tolerances are 50 and 12 g, respectively. Power-management techniques, both in hardware and software, result in a low-power consumption; 10 W in the active mode. Samples will become available in the first quarter of next year. Production quantities, on the other hand, will be available in the second quarter.

***Ampro Computers Inc.**, 4757 Hellyer Ave., San Jose, CA 95138; (408) 360-0200; http://www.ampro.com.*
CIRCLE 570

Fiber-Optic Module Suits Shared-Memory Applications

The IP-FiberIO mezzanine module is a high-speed fiber-optic communication system that transfers data from node to node at speeds up to 10.6 Mbytes/s. The module conforms to the Type III IndustryPack standard. It requires neither drivers, protocol stacks, nor specialized software for operation. The low-cost mezzanine module is suited for a number of shared memory applications, such as flight simulators and industrial distributed control systems.

Unlike similar shared-memory products, which may be limited to a specific bus, the IP-FiberIO can be integrated into PCI, CompactPCI, VXI, and VME, as well as other bus architectures that use an IndustryPack carrier board. Available immediately, the IP-FiberIO IndustryPack mezzanine module is priced at $3875 each, with significant volume discounts available.

***GreenSpring Computers**, 181 Constitution Dr., Menlo Park, CA 94025; (415) 327-1200; Internet: http://www.greenspring.com.* **CIRCLE 571**

Circle 520

Program Gives Asymmetrical Spice Tolerances

ROBERT R. BOYD
314 Riverview Ave., Orange, CA 92865-1130.

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Address your Ideas for Design submissions to Ideas for Design Editor, Electronic Design, 611 Route 46 West, Hasbrouck Heights, NJ 07604; fax (973) 393-6242.

Spice is unable to accommodate asymmetric tolerances for worst-case analysis. However, the DISTRIBUTION statement available in Monte Carlo analysis can accommodate asymmetric tolerances by creating histogram bins. Asymmetric tolerances can easily occur for any component with temperature drift in unbalanced temperature environments. They also can occur in some capacitors.

The QBasic program shown will create 20 bins of Gaussian distribution with symmetric or asymmetric tolerances *(Listing 1)*. The program will print out the .DISTRIBUTION statement with bins for easy import to a Spice net list. The example problem is a component with –10% and +2% tolerances. The asymmetry is somewhat extreme, but it clearly illustrates the use of the program.

The program assumes 500 samples to ensure a reasonably accurate Gaussian curve. The output of the program is given *(Listing 2)*.

The program assumes the component is a resistor. For a capacitor, change the .MODEL statement as follows:

```
.MODEL CA CAP (C=1 DEV/ASYM=10%)
```

and correspondingly for an inductor. The output text file is placed in the root directory C:\ with the name "qbout.txt."

A histogram for this example is shown *(see the figure)*.

VOTE!

Read the Ideas for Design in this issue, select your favorite, and circle the appropriate number on the Reader Service Card. The winner receives a $300 Best-of-Issue award.

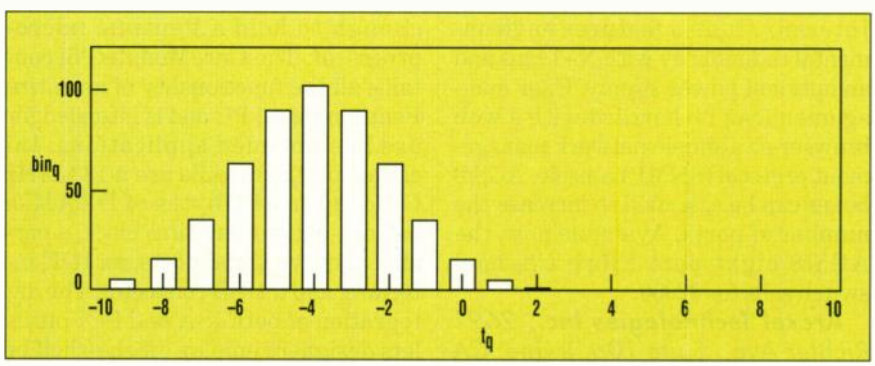
LISTING 1

```
DECLARE SUB Ndist (m1!, s1!, x!, y!)
' creates distribution statements for spice.
CLS : INPUT "Print to Screen or Text file (S/T)"; C1$
IF C1$ = "T" OR C1$ = "t" THEN
  Dev1$ = "c:\qbout.txt"
ELSE
  Dev1$ = "SCRN:"
END IF
OPEN Dev1$ FOR OUTPUT AS #1
CONST pi = 3.141593
INPUT "Component tolerance in percent; minus (comma) plus order?"; T1, T2
T1 = T1/100: T2 = T2/100: F1 = 1; IF ABS(T1) > ABS(T2) THEN F1 = 0
Rnom = 1000: Rlow = Rnom * (1 - T2): Rmin = Rnom * (1 + T1)
Rmax = Rnom * (1 + T2): Rplus = Rnom * (1 - T1): nb = 20
inc = 2/nb:  m1 = (Rmax + Rmin)/2: s1 = (Rmax - Rmin)/6: N = 500
IF F1 = 1 THEN Rplus = Rmax: Rmin = Rlow
intv = (Rplus - Rmin) / nb: x = -1: r = Rmin: DIM bins(nb + 1)
CLS : PRINT "Minus and plus tolerances are"; 100 * T1; "%";","; 100 * T2; "%"
PRINT #1, : PRINT #1, ".DISTRIBUTION ASYM";
FOR c = 1 TO nb + 1
   CALL Ndist(m1, s1, r, y): y = N * intv * y
   bins(c) = y: r = r + intv: PRINT #1, "("; : PRINT #1, x; : PRINT #1, ",";
   PRINT #1, INT(bins(c) + .5); : PRINT #1, ")";
   x = .1 * INT(10 * x + 10 * inc + .5)
   IF c MOD 5 = 0 THEN PRINT #1,  PRINT #1, "+";
NEXT c
PRINT #1, : PRINT #1, ".MODEL RA RES(R=1 DEV/ASYM =";
T = T1: IF ABS(T2) > ABS(T1) THEN T = T2
PRINT #1, ABS(100 * T); "%)"
CLOSE
END

SUB Ndist (m1, s1, r, y)
d = 1/(s1 * SQR(2 * pi))
ex = (r - m1) ^ 2/(2 * s1 ^ 2)
y = d * EXP(-ex)
END SUB
```

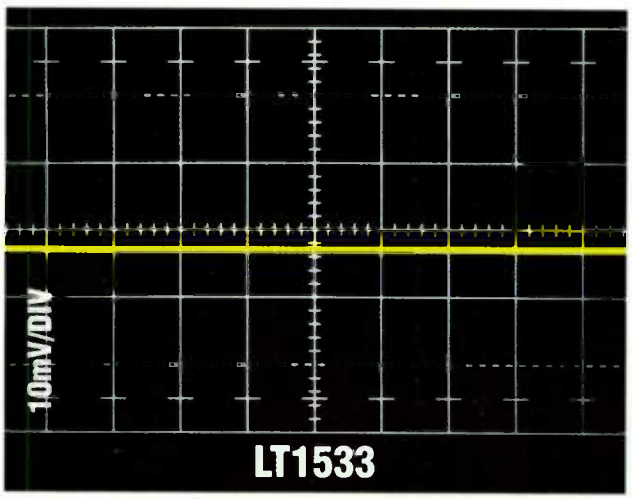
LISTING 2

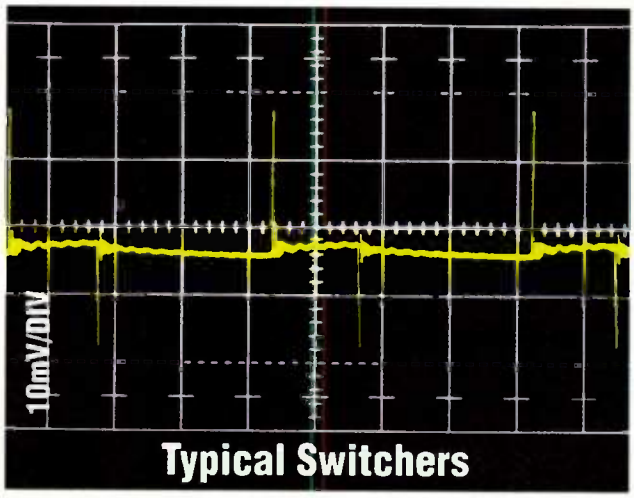
```
DISTRIBUTION ASYM (-1, 1) (-.9, 4) (-.8, 13) (-.7, 32) (-.6, 60)
+(-.5, 88) (-.4, 100) (-.3, 88) (-.2, 60) (-.1, 32)
+(0,. 13) (.1, 4) (.2, 1) (.3, 0) (.4, 0)
+(.5, 0) (.6, 0) (.7, 0) (.8, 0) (.9,0)
+(1, 0)
.MODEL RA RES(R=1 DEV/ASYM = 10%)
```



This histogram is for the example given in the article, which is a performed for a resistive component exhibiting unusually asymmetric –10% and +2% tolerances.

100µV Output Noise Switching Regulator





The Good.

The Bad & The Ugly.

LT1533: The First Switching Regulator with Lower Noise than a Linear Regulator.

The LT1533 DC/DC converter produces less than 100µV peak-to-peak output noise over a 100MHz bandwidth. The internal power switches allow user-adjustable voltage and current slew rates, resulting in dramatically reduced conducted and radiated EMI. Finally, a switching regulator that can coexist with noise sensitive applications such as precision instrumentation and wireless communications.

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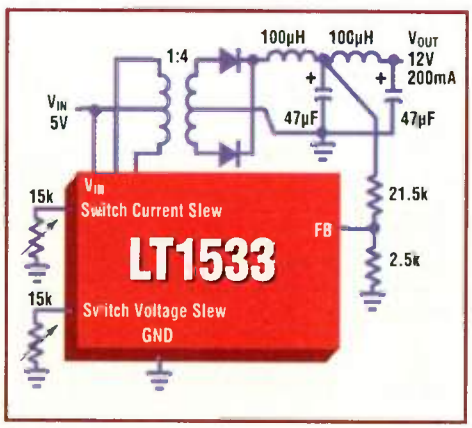

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Circle 521

Robust, Low-Cost Continuous Phase FSK Modulator

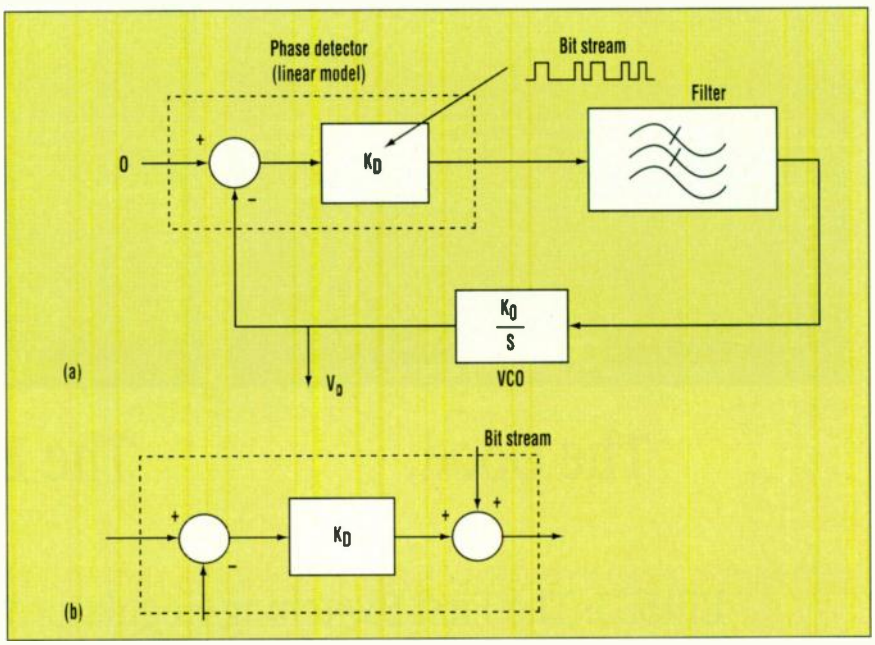
EDUARD BERTRAN
Universitat Politecnica de Catalunya, Dept. of Signal Theory and Communications, C/Jordi Girona, 1-3, 08034-Barcelona, Spain; phone: +34 3 4017074; fax: +34 3 4015910; e-mail: tsceba@eupbl.upc.es.

IFD WINNER

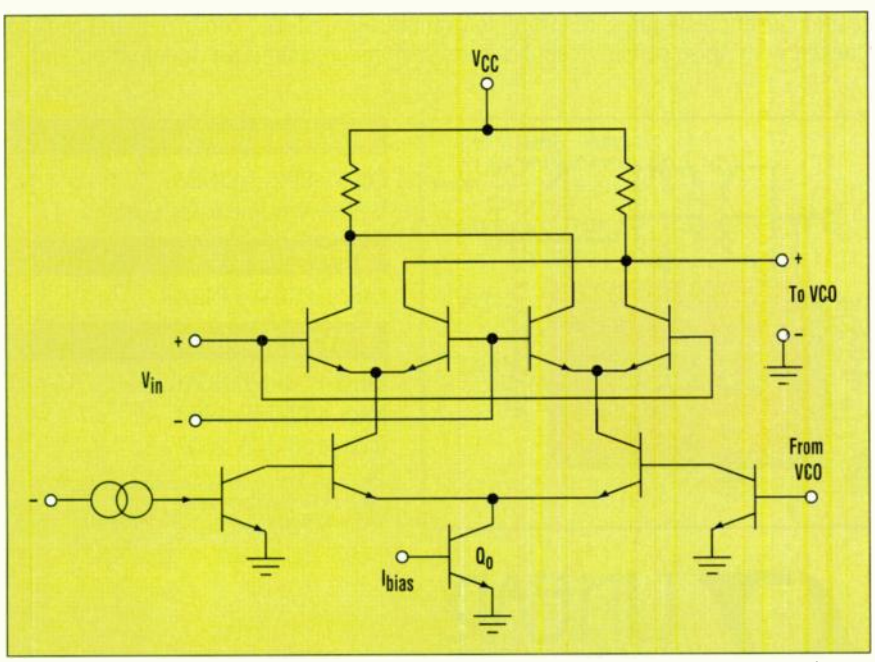
J. Jayapandian, IGCAR, Materials Science Div., Kalpakkam, PIN 603102, Tamil Nadu, India; fax: 0091-04114-40360; email: msd@igcar.ernet.in. The idea: *"Special BIOS Interrupt for Real-Time Data Acquisition and Control."* May 1, 1997 Issue.

In bandpass data transmission, one common way to design low-cost frequency-shift-keying (FSK) analog modulators is to use two independent oscillators that have outputs switched according to the binary input wave to be modulated. While this approach is simple, phase discontinuities during oscillator switching unnecessarily increases the bandwidth of the modulated signal. On the other hand, any any solution based on the synchronization of the oscillator increases the modulator cost.

A well-known alternative is the use of classical oscillators such as op-amp or transistor-based astables, CMOS oscillators, or "linear" oscillators (e.g., the Wien oscillator), where a capacitor value is switched under the control of the binary wave. Because the capacitor voltage can't change instantaneously, the result is a continuous phase FSK (CPFSK).



2. In this simplified X model of a PLL with zero input (a), the change of conversion gain is similar to having an offset in the phase-detector model output (b).



1. This double-balanced mixer is based on a constant-current source for a differential amplifier.

Another common solution involves the direct use of a VCO.

In both of these alternative cases, the design is very sensitive to power-supply variations and the tolerances among the IC's fabrication series or manufacturers. This sensitivity could be negligible in small production runs, but leads to problems in large factory productions of FSK modulators, which are usually solved by adding some adjustable circuit component. Apart from the augmented production cost due to this adjustment, experience shows that the adjustment margin can be different if the oscillator's IC is purchased from different manufacturers.

Shown here is a phase-locked loop (PLL) based alternative for CPFSK generation. It exploits the low sensitivity (or robustness) of the set composed of the phase detector and VCO with re-

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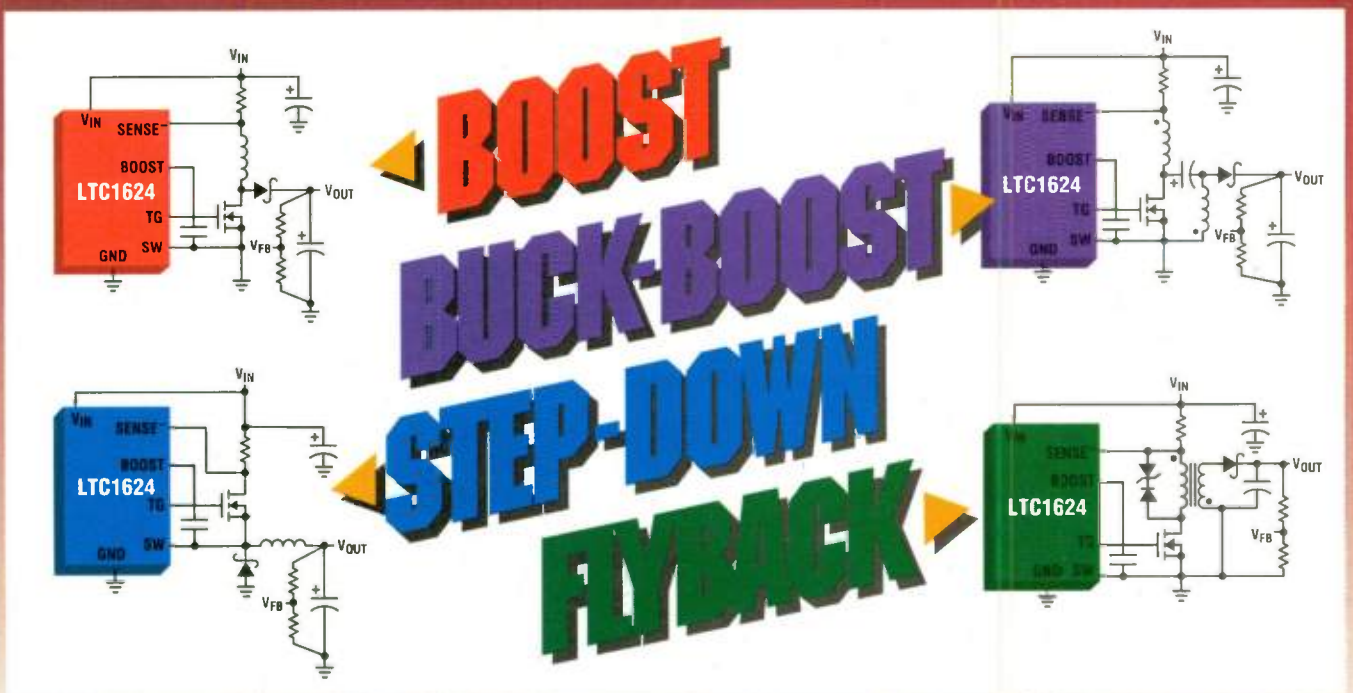

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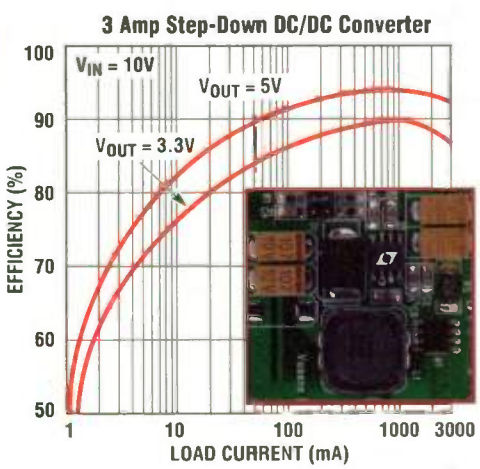

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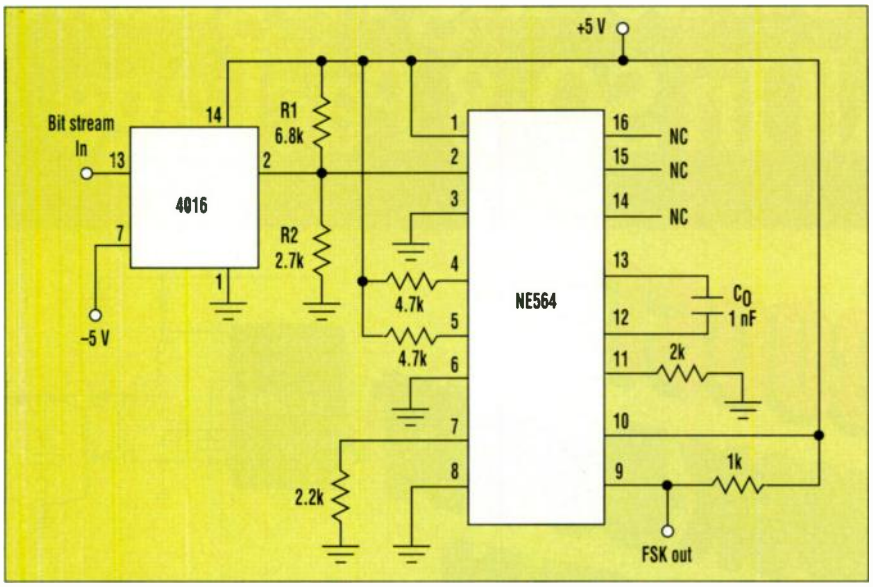


3. Based on the NE564 analog PLL, this circuit generates continuous-phase FSK signals.

spect to certain parameter variations, mainly in the lower part of its frequency band (compared with the sensitivity of other solutions, such as the direct use of the VCO). However, the main problem in using a PLL for FSK generation is that the PLL input is designed for sinusoidal waves, not for the bit stream to be FSK-modulated.

The proposed solution benefits from the double-balanced mixer commonly used as a phase detector in PLL circuits. This mixer is based on a constant-current source for a differential amplifier *(Fig. 1)*. By externally sinking or sourcing bias current at the transistor Q0, which acts as the current source, the conversion gain (K_D) of the phase detector is changed. In a simplified X model of the PLL *(Fig. 2a)* with zero input (regulation model), the change of conversion gain is similar to having an offset in the output of the phase-detector model *(Fig. 2b)*. This offset modifies the voltage input of the VCO of the PLL, so the VCO output frequency is varied under the control of the bit stream applied to the current source. This structure is similar to some phase-lock angle modulators. However, in the proposed idea, it's unnecessary to break the PLL with additional circuitry in order to introduce the modulating signal, hence a single analog PLL can be used.

Figure 3 illustrates a circuit based on the analog phase-locked loop NE564. The IC 4016 is a switch controlled by the binary signal to be FSK-modulated, which commutes the voltage at pin 2 of th NE564 between ground and 5 V × 2700Ω/(2700Ω + 6800Ω) = 1.42 V. This voltage at pin 2 modifies the current bias of the current source in the phase detector, and consequently the VCO output frequency varies without phase discontinuities. The VCO center frequency is fixed by C0, and the margin between the two FSK frequencies is adjusted by R1 and R2. For an FSK modulator with frequencies of 390 kHz for "MARK" and 560 kHz for "SPACE,' the component values are as shown in Figure 3.

In this design, the classical PLL low-pass filter has not been included, as its presence is unnecessary for FSK generation. In addition, the filter increases the transfer function sensitivity with respect to the VCO parameters.

Software Linearization Techniques For Thermistors

REX KLOPFENSTEIN JR.
King Industries Inc., 500 Lehman Ave., Bowling Green, OH 43403;
(419) 353-5311; fax (419) 352-1583.

Interfacing an NTC thermistor to a computerized data-acquisition system requires a resistance-to-voltage (or current) converter (bridge, voltage divider, etc.). It's also necessary to incorporate software routines to convert the ADC units of the data-acquisition system back into resistance values. Once the temperature readings are converted back into thermistor resistance values, the algorithm given here can be used to generate temperature readings.

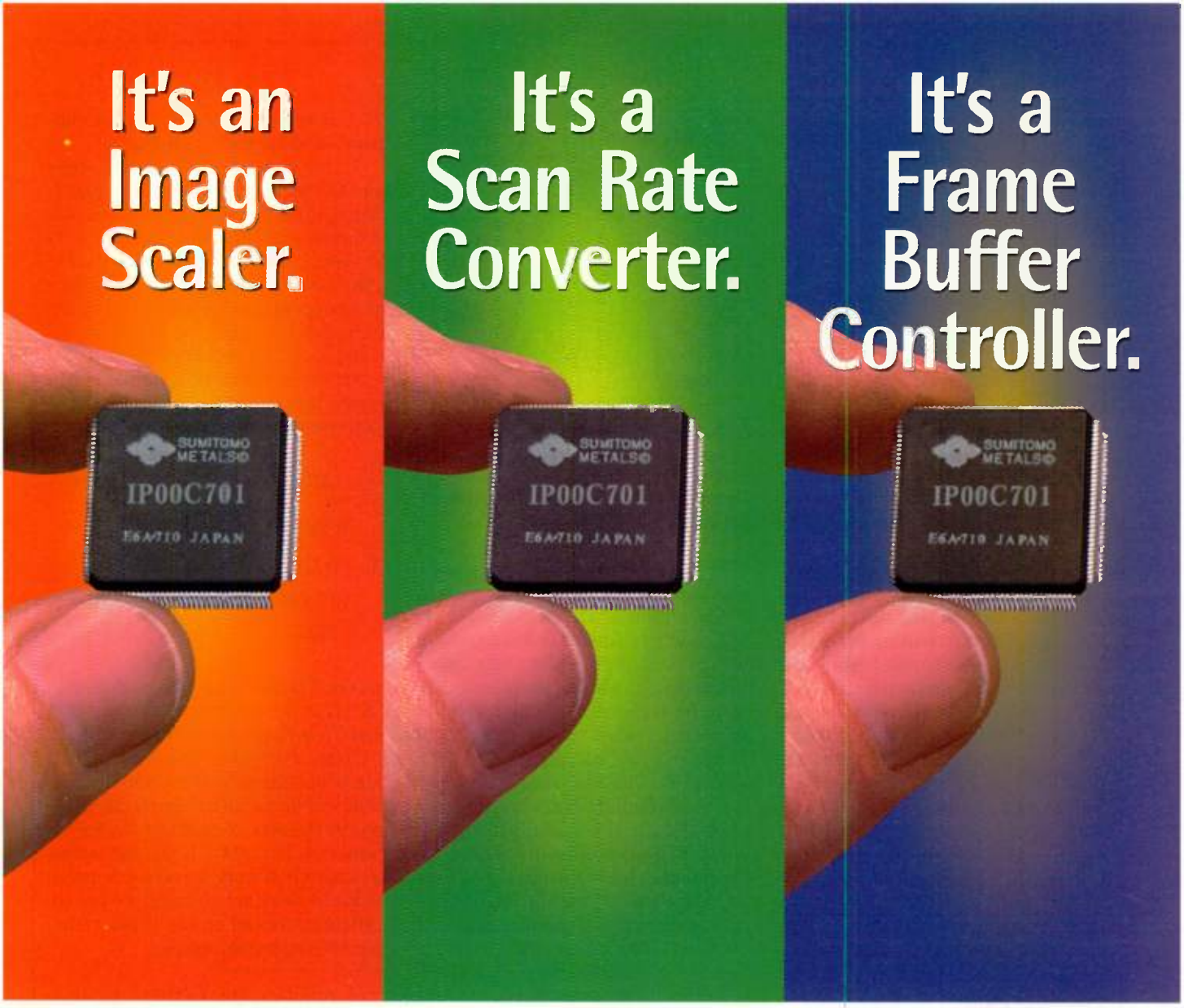
Steinhart and Hart developed an equation that can be used to linearize the resistance output of a thermistor:

$$\frac{1}{T} = A + B[\ln(R)] + C[\ln(R)]^3$$

where T is temperature (in Kelvin); R is resistance (in Ω); and A, B, and C are curve-fitting coefficients. To apply the Steinhart-Hart equation, it first is necessary to determine the numeric values of the curve-fitting coefficients (A, B, C). These coefficients can be determined by setting up three simultaneous linear equations using temperature and resis-

```
#include<math.h>

double temp_convert_c(double resistance)
{
        const double A=1.75E-3;
        const double B=339.9E-6;
        const double C=308.9E-9;
        return((1.0/(A+B*log(resistance)*C*log(resistance*resistance)))-273.15;
}
```



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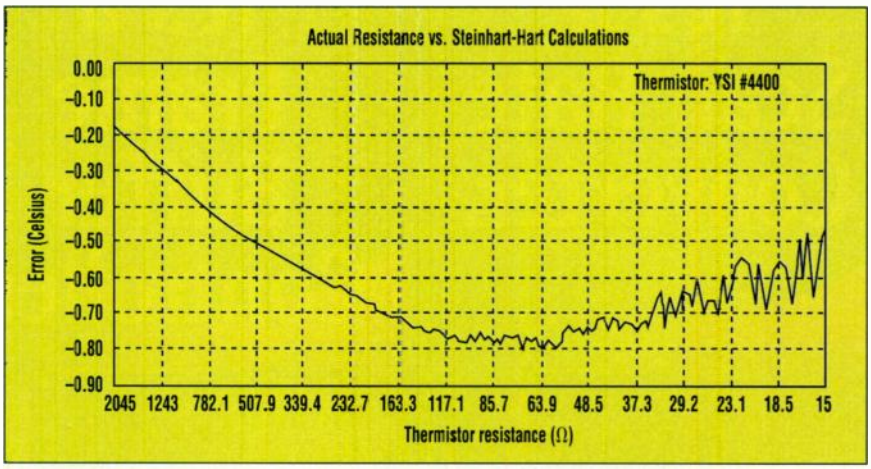

Shown is an error plot of the actual resistance of thermistor YSI #44001 versus the predicted resistance values calculated using the Steinhart-Hart linearization algorithm.

tance values from three temperature points (T1, T2, T3). These data points can be generated using temperature calibration equipment or extracted from data tables furnished by the manufacturer of the thermistor.

The Steinhart-Hart equation will generate temperature values with a ±0.02°C accuracy if the temperature data points span magnitudes of less than or equal to 100°C ($|T3 - T1| \leq 100°C$) and the data points are centered on the normal range of thermistor (T2 ≈ midpoint of temperature range). Once the curve-fitting coefficients are determined, this equation can be used to convert thermistor resistance values into equivalent temperature values.

To demonstrate the techniques necessary to linearize a thermistor using the Steinhart-Hart equation, a linearization algorithm was developed for a thermistor (YSI #44001), which operates in a temperature range of -50°C (223.15K) to 100°C (373.15K). The first step in developing the Steinhart-Hart linearization algorithm is the calculation of the curve-fitting coefficients. This is accomplished by selecting three temperature values that fall within the operation range of the thermistor (–50°C to +100°C). A third value of 25°C is selected because it's the midpoint of temperature range.

Using these temperature values and the associated resistance magnitudes, three linear equations are constructed with three unknowns: 2045 Ω @ –50°C; 100 Ω @ 25°C; and 15 Ω @ 100°C. Substituting these resistance and temperature values into three linear equations gets the following results: $A = 1.75 \times 10^{-3}$; $B = 339.9 \times 10^{-6}$; $C = 308.9 \times 10^{-9}$. Substituting the coefficients into the Steinhart-Hart equation results in:

$$\frac{1}{T} = 1.75 \times 10^{-3} + 339.9 \times 10^{-6} \ln(R) + 308.9 \times 10^{-9} \ln(R)^3$$

$$T_C = (1 / (1.75 \times 10^{-3} + 339.9 \times 10^{-6} \ln(R) + 308.9 \times 10^{-9} \ln(R)^3)) - 273.15$$

where T is the temperature in Kelvin (K), R is the resistance in ohms (Ω), and T_C is the temperature in Celsius (°C) *(see the figure)*. The software listing is an example of a C++ function that will linearize a thermistor. It requires the user to calculate the coefficients (A, B, and C). If one has access to a matrix library, a second function could be designed to calculate the coefficients based on the three resistance/temperature entries.

Circle 523

Measure Light Intensity With An 8-Bit Microcontroller

HARTONO DARMAWASKITA
Microchip Technology Inc., Standard Microcontroller & ASSP Div.,
2355 W. Chandler Blvd., Chandler, AZ 85224; (602) 786-7200.

Light sensors find their way into a host of interesting applications. For instance, a light sensor in a camera measures the amount of light that the film will be exposed to. Once the amount of light is known, the proper lens aperture can be calculated to make sure that the picture is taken with the proper amount of exposure.

In a smoke detector, a light sensor can be used to measure the amount of light transmitted by a known light source, such as an LED, through the air inside the sensor assembly. When the air becomes smoky, the amount of light received by the sensor changes. If the amount of light change goes above a preset threshold, then more than likely something nearby is burning, and a horn is activated to indicate there's a fire in the building.

There are many other applications for light sensors, such as flame detectors, security systems, lighting control, robotics, etc. In these applications, many of us think that since the sensor produces an analog output, interfacing this type of sensor to a microcontroller will require a conventional analog-to-digital converter. Actually, though, by using just a few discrete components, interfacing a light sensor to an A/D-less microcontroller is very simple.

Photodiodes and phototransistors are two of the most popular and low-cost light sensors. These devices are readily available in the $1 range. Both devices produce current outputs as a function of light intensity. The operating range of such devices varies depending on the manufacturer. Many of these sensors are equipped with built-in lenses tuned to particular wavelengths, so they're most effective for detecting or measuring light with those wavelengths. To get the best performance, the voltage across the

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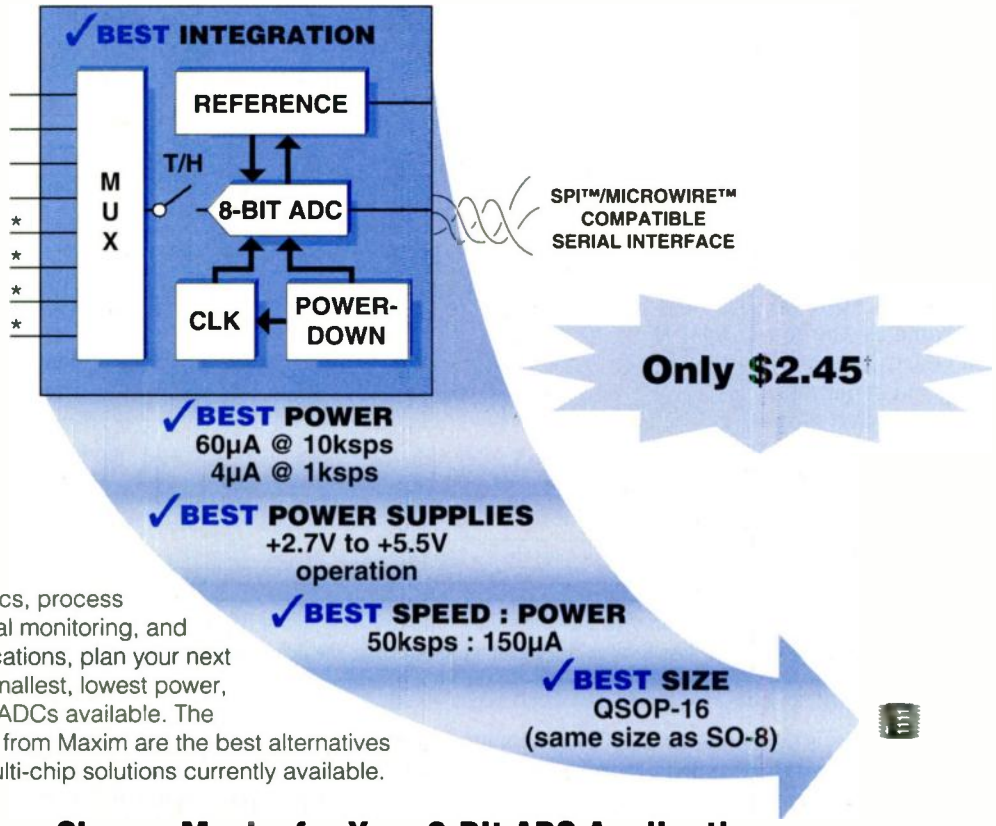

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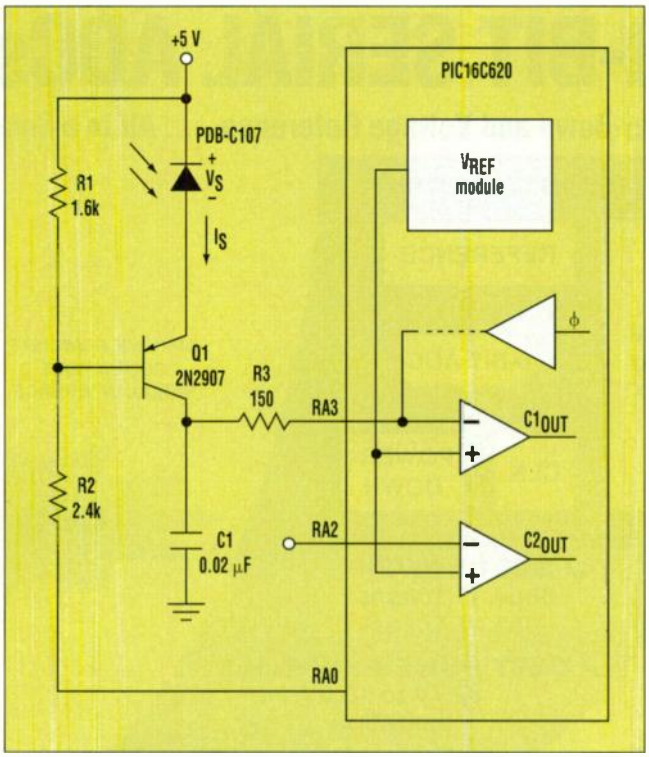
sensor must be held constant during measurement.

The circuit shown represents a very simple method of interfacing a light sensor to the PIC12C620 microcontroller *(see the figure)*. The light sensor selected in the example is Photonic Detectors' PDB-C107 (available through Digi-Key). The PNP transistor (Q1) and resistors R1 and R2 are used to provide a constant sensor voltage (V_S) within 1 to 1.3 V. The collector current of Q1 is approximately the same as the sensor current (I_S). Capacitor C1 integrates I_S and generates a voltage ramp with a slope that's proportional to the light intensity seen by the sensor.

The microcontroller has two voltage comparators and an internal voltage reference. One of the voltage comparators and the voltage reference are used to interface to the sensor circuitry. The second voltage comparator, left unused in this example, is available for other application-defined tasks, such as temperature measurement using a thermistor, ac-line zero-crossing detection, etc. The RA3 pin has multiple functions. It can be configured as a digital I/O, or an analog connection to the inverting input of the voltage comparator. Both RA3 and RA0 pins are used to control the sensor. Initially, the system is in an idle state, where RA0 is a high output to disable the sensor, and RA3 is a low output to discharge C1 through R3. This idle state helps minimize power consumption.



This circuit offers a simple way to measure light intensity using an A/D-less 8-bit microcontroller; in this case, the light sensor is interfaced to the tiny 8-pin PIC12C620 microcontroller.

To start a measurement, RA0 is set to a low output to activate the sensor circuitry. RA2 is now set to an input and connected to the voltage comparator's inverting input. The noninverting input of the comparator is connected to the internal voltage reference. The capacitor voltage then starts to ramp up. The microcontroller now begins its timer while monitoring the state of the comparator's output. When the capacitor voltage and the voltage reference are equal, the comparator output goes from a high to a low state.

As soon as the microcontroller detects this transition, it stops its timer. At this point, the measurement is completed, and the micro sets the RA3 and RA0 port lines back to the idle state. The time measured during the ramp is inversely proportional to I_S. The microcontroller can process this information to meet whatever the application's goal is, such as activating the horn in a smoke detector, running the motor in a robot, or simply sending the reading to the host computer.

Depending on the application, system calibration and linearization may be required. The size of C1 and the maximum measurement time depend on the light sensor, amount of light used in the application, and the internal voltage-reference setting.

In many other applications in which the measurement resolution and accuracy aren't critical, such as detecting whether the lamp is 25% or 50% on, an even lower-cost microcontroller without any analog peripheral (such as the 8-pin PIC12C508) can be used. Instead of utilizing a voltage comparator with an internal voltage reference, the capacitor voltage measurement can be done on a regular I/O pin. The microcontroller now will measure the voltage ramp from 0 V to its high input threshold voltage. The system measurement error, stability, and repeatability will directly reflect the threshold voltage variations due to the system's power-supply voltage, process variations, and the device temperature.

Circle 524

Inexpensive "Power OK" Signal For The PC

JIM HAGERMAN
Science & Technology International, 733 Bishop St., Suite 3100, Honolulu, HI 96813.

It's often handy to have an LED indicate "Power OK" status in electronic equipment. Single-supply designs need only a resistor and an LED to perform this function.

A personal computer, on the other hand, has four supply voltages (+5 V, −5 V, +12 V, and −12 V), requiring a more sophisticated circuit.

A typical approach would use a comparator for each supply voltage to be monitored. If the comparator selected has open-collector outputs, all comparator outputs can then be wire-OR'ed to create the desired OK signal. Performance with this type of arrangement is good but the circuit is relatively costly.

If accurate voltage monitoring isn't needed, then the simple and inexpensive circuit shown can be em-

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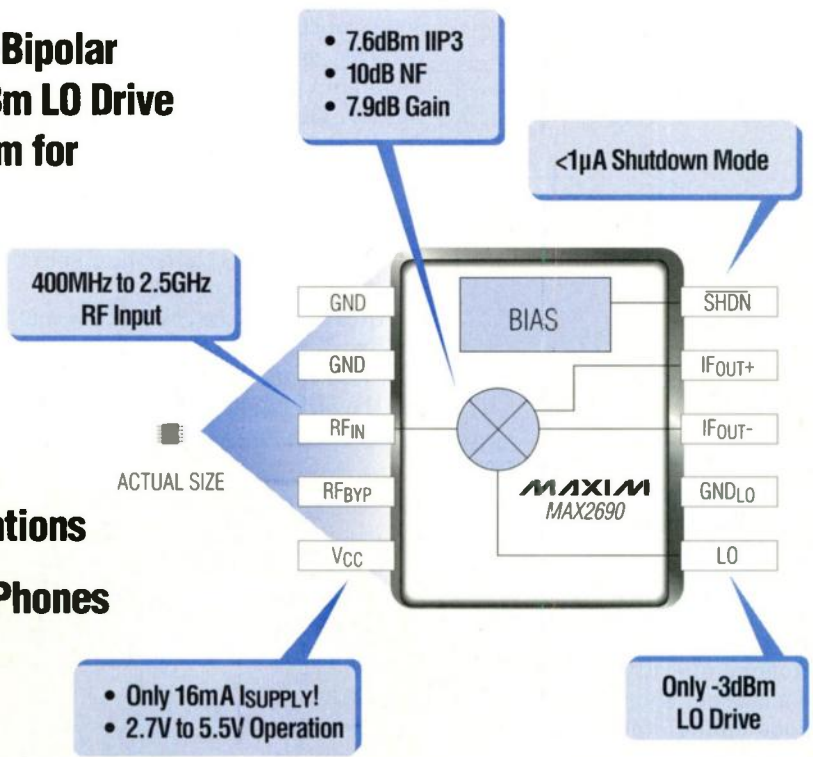

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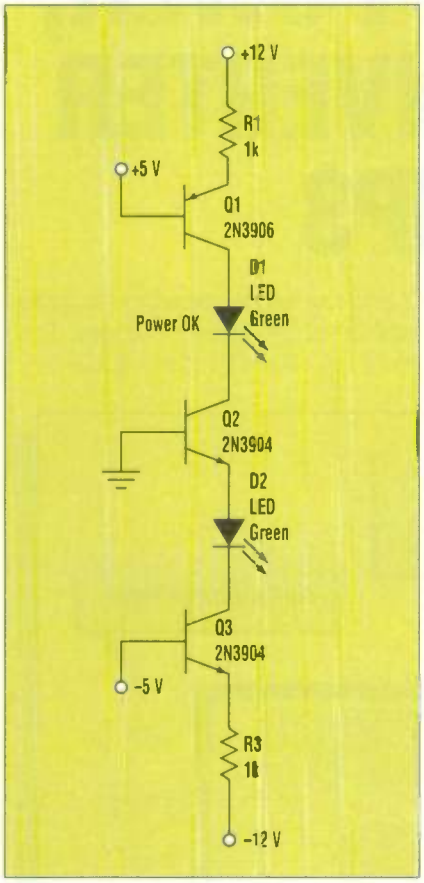


This simple "Power OK" indicator for personal computers is a low-cost alternative to traditional voltage monitors.

ployed *(see the figure)*. Each supply must be operational for LED D1 to be illuminated.

In normal operation, Q1 and R1 create a current source of about 6.3 mA (good enough for most LEDs). Similarly, Q3 and R3 create a 6.3-mA current sink. Q2 acts as a common-base amplifier to pass the current. If the current sink is greater than the source, then Q2 will saturate with the base current making up the difference. If source is greater than sink, Q1 will saturate. In either case, the Power OK LED D1 will be lit.

As the +12-V supply drops, D1 will gradually get dimmer and finally extinguishes when the +12-V supply voltage goes below +6 V. If the +5-V supply drops below about 1 V, then D1 will be illuminated.

Operation of the negative side is similar except that the threshold for the –5-V supply is at about –2 V. D2 can be replaced with a diode if desired. For higher thresholds, use two diodes in series for D1 and D2.

Circle 525

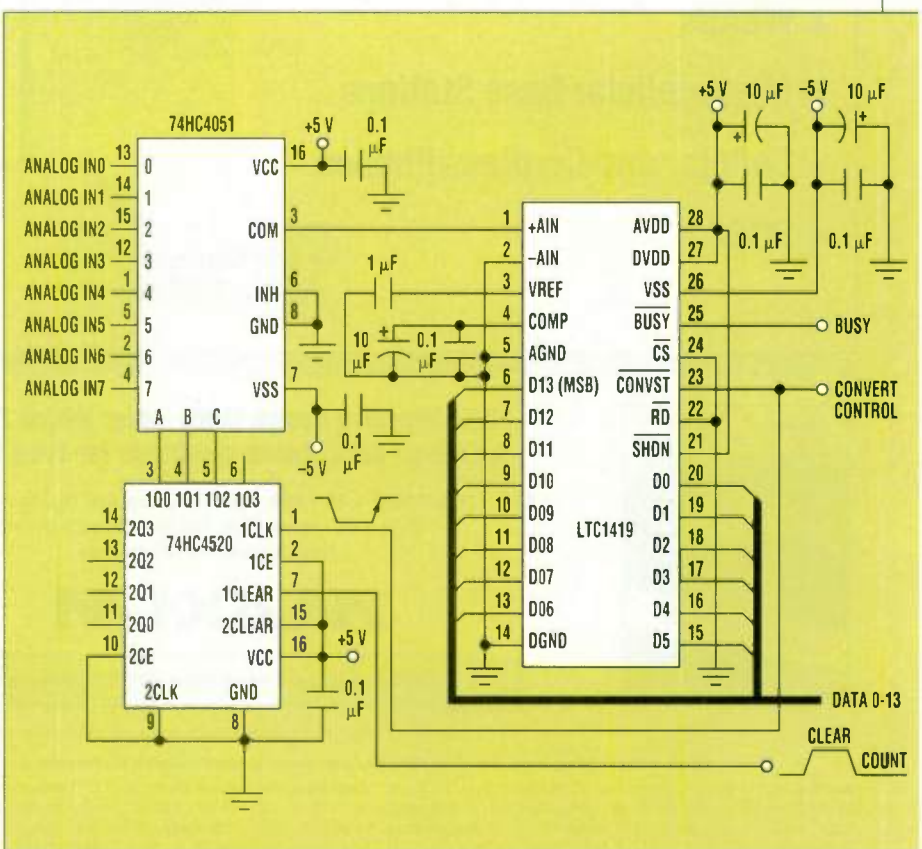
Multiplex A/D Inputs Without Software

KEVIN R. HOSKINS
Linear Technology Corp., 1630 McCarthy Blvd., Milpitas, CA 95035-7487.

The circuit described here uses hardware instead of software routines and multiple I/O ports to select multiplexer channels in a data-acquisition system. It features an 800-ksample/s 14-bit ADC (U1), which receives and converts signals from an 8-channel multiplexer (U2) *(see the figure)*. Three of the four output bits from a dual 4-bit binary counter are used to select a multiplexer channel. A power-on or processor-generated active high signal applied to U3's CLEAR pin resets the counter, selecting multiplexer channel 0.

After clearing the counter, the multiplexer's channel selection input is 000. This connects the channel 0 input to U1's S/H input. The falling edge of the convert start signal forces the ADC's sample -and-hold to acquire and hold the selected multiplexer signal. The rising edge of CONVST clocks the channel-selection counter. To ensure complete acquisition, CONVERT should be low for 300 ns.

As CONVST pulses increment the counter from 000 to 111, each multiplexer channel is individually selected, its input signal applied to U1's analog input, and an A/D conversion is initiated. After the multiplexer cycles through all eight input channels, the counter rolls over to zero and the process repeats. At any time, the input multiplexer channel can be reset to 0 by applying a logic high pulse to U3's CLEAR pin.



This simple standalone circuit requires no software and minimal I/O to sequentially sample and convert eight analog signal channels at 14-bit resolution and 100 ksamples/channel.

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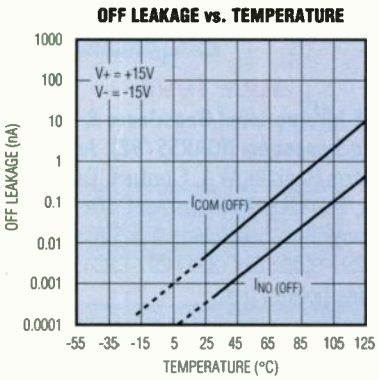

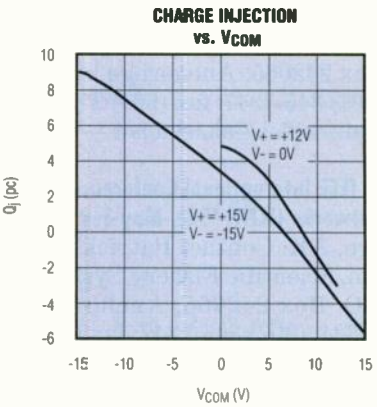

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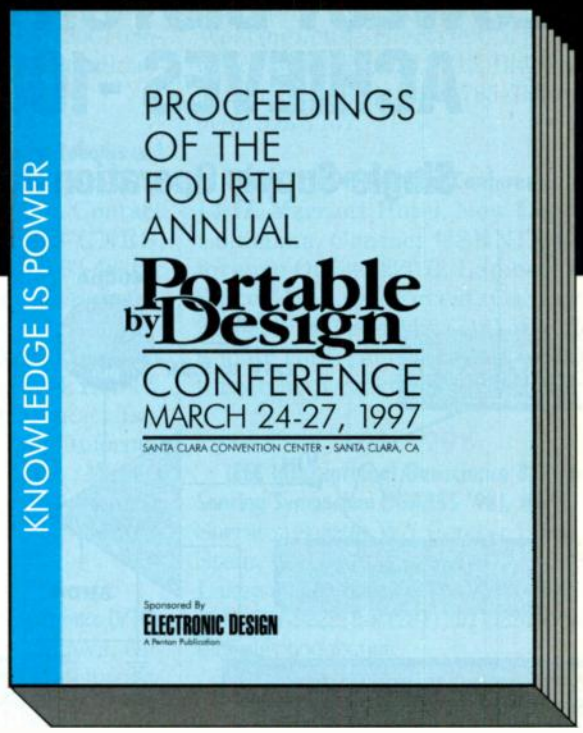

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BOB PEASE

What's All This Breadboarding Stuff, Anyhow?

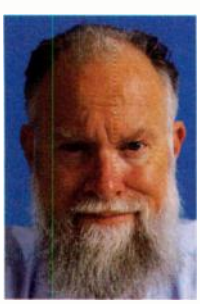
After I sent out a brief note, confirming that we rarely see anything written down about how to do breadboarding, the letters and e-mail started coming.

This e-mail's from Graeme Nisbet in Germany:

To: RAP
Subject: Breadboarding

Regarding the letter from Barry Lunt in "Bob's Mailbox" (Electronic Design, Aug. 18th, 1997), I have the following advice:

Get in touch with Wainwright Instruments in Germany (or your local distributor), and order some of the "Wainwright Prototyping System" kit. It consists of various sizes of double-sided board, along with a huge assortment of self-adhesive pieces of glass-fibre board with various package land patterns preetched onto the surface. They supply land patterns for just about any package you can think of—DIL, surface mount, discrete devices, you name it!



BOB PEASE
OBTAINED A BSEE FROM MIT IN 1961 AND IS STAFF SCIENTIST AT NATIONAL SEMICONDUCTOR CORP., SANTA CLARA, CALIF.

You also can purchase self-adhesive transmission lines (50 Ω, 75 Ω, 150 Ω, etc.), and low-profile tracks for power-supply distribution. These can be cut to the required length before being stuck down onto the ground plane. Creating a circuit requires you to stick down the appropriate land patterns, solder down the components, then wire up the circuit. You can create circuit boards very quickly, and it's good up to about 2 GHz.

I first used this product over ten years ago and I have NEVER used anything else since. I now use it for analog, digital, and RF boards. Keep up the good work in your column.

I promptly replied to Graeme, that I, myself, like to use strips of copper-clad for breadboarding. I had heard of the Wainwright stuff, but I could not guess where to find the distributor.

I also like to use wire-wrap sockets, tack soldered onto ground planes of copper-clad. I never use wire-wrap, but I just like the long, heavy, metal pins, as I can bend them over and get good access.

Shortly thereafter, I got this reply:

Hi Bob: Sorry for the delay, but I lost my Wainwright catalogue and had to contact the U.K. distributor for a new one. Anyway it has now arrived and the manufacturer's details are as follows:

Wainwright Mini-Mount-System
Aufbau von Versuchsschaltungen
Hartstr. 28c,
D-82346 Andechs
Germany
Tel. 0 81 52/3162
Fax. 0 81 52/40525

Graeme, We will try to find out if there is any local distributor, in the U.S.

This next e-mail comes from Ed Maddox, in Massachusetts:

To: Robert A. Pease
Subject: Breadboarding

First, a departure from the announced subject to say HELLO by way of the modern technology. My company won't spring for the expense of full net connections, but the e-mail is in use all the time.

I have never tried to record some breadboarding rules before, but here are a few of my construction guides extracted from memory.

1. Abandon the plug-in-the-lead variety of white protoboards when:

- *The frequency of interest exceeds 500 kHz or so. (And don't forget harmonics!)*
- *The design calls for capacitor values lower than 100 pF.*
- *An unexpected presence of 10 or 20 pF between points would be disturbing.*
- *Unexpected resistances of 0.5 Ω or so in the component paths would hurt.*
- *The circuit will have currents of over 100 mA.*
- *The operating voltage will exceed 150 V.*
- *You have anything else that one might have learned is a no-no.*

2. Try as the second level, the patterned-etched circuit boards which give you good locations for dip sockets and leaded components. They require a minimum usage of insulated wire connections, if you plan a little. It won't hurt to branch out into the air for later thoughts and changes, if you shorten the component leads for those cases where series inductance may get in your way, and/or stray capacity needs to be kept low.[1,2]

3. If you are going to go on up in the spectrum to 30 or 100 MHz and higher:

- *Start building over a ground plane of copper-clad glass epoxy, like circuit boards. A width of 2 to 3 in. by 8- to 10-in. long is a good start. Grounded leads are just tacked to the copper clad with solder.*
- *Up in this part of the spectrum with some gain (amplification), plan your signal flow with the input at one side, and a steady progress toward the other side of the ground plane. (Actually, this flow is good at any speed.)*
- *A total gain of 40 dB or more should be separated into 20-dB or smaller pieces by erecting vertical shield walls across the ground plane along the signal path. Notches in the bottom edge of the shield wall can pass the signal and supply lines, and the walls make good places to add supply bypass capacitors.*
- *Passing 100 MHz, it would be prudent to add one or two side-walls to the*

BOB PEASE

ground plane and shield walls. These are still all made of copper-clad circuit-board stock. The walls should be as high as the ground plane is wide. When you KNOW that your circuit will work, and you need to make an efficient product assembly, you can then tackle the challenge of reducing the need for shields and walls.

Notes:

1. When you allow yourself to branch into the air, you will be joining one of the World-Class Breadboarders—Robert A. Pease.

2. It is possible to construct a decent audio-frequency circuit on nothing more than bus wires running from side to side, with buses for the plus supply, logic supply, ground, and minus supply. Components are wired point-to-point, vertically from bus-to-other, or bus-to-bus. The components end up supporting the buses.

P.S. I had one that reached a 7-ft. length once. It contained a major portion of an audio-spectrum remote-control system with control to, and metering from, broadcast-station transmitters and similar systems.

Well, I promptly sent a hello back to Ed, agreeing with him on many items. But I added four more *caveats* to his part 1:

• I would avoid the solderless breadboards for frequencies that are above 50 kHz.

• I would beware when inductance would hurt, for example, if there is a lot of di/dt, such as in a switching regulator. Or, when a bypass capacitor must be right near an IC, and the long paths won't let you do that.

• I'd avoid them when leakage between nodes would be harmful, as the nylon is not necessarily a high impedance in warm, damp weather.

• I also pointed out to Ed that the care you put into your breadboard depends on what you plan to do with it when you get it running.

Then I got some more e-mails on this subject. (BOY, I am getting a LOT of e-mail these days!) This one is from Greg Lee:

To: RAP
Subject: Inquiry About Prototyping.

The "ARRL Handbook" and the "Art of Electronics" have excellent material on prototyping. Also Linear Technology's (blasphemy!) Application Note 47 is excellent. I'm glad to hear there are academic people concerned about this stuff.

I checked into the *ARRL Handbook*, and it does have several very good *practical* pages on this topic. Likewise Hurwitz and Hill's book—*The Art of Electronics*—has a very good chapter. More good advice. If you don't want to spend the money for this kind of info, get your Librarian to order them. Every good library should have those two books.

Then I got one more e-mail on this topic from: Mark Balch:

To: Bob Pease
Subject: Breadboarding Skills
What a coincidence!

• *Last week I hear that you're trekking with my father and Peter Owens.*

• *You write that "students are not learning about breadboarding skills."*

(Heck, most engineering students are not even able to get any lab courses at all, not to mention the NUANCES of breadboarding. /rap)

• *Practical EE education at the college level is a topic that I feel very strongly about. So, how could I not reply with my own opinions?*

Anyway, it's too bad that some academic institutions frown upon instructing students in "vocational topics" such as soldering and prototyping. There are many well-meaning professors and deans who seem to believe that presenting anything less than multidimensional Fourier transforms and deriving Biot-Savart's law is beneath the mission of higher education. I believe that the major purpose of an engineering education is to prepare a person to function as a capable engineer. Part of being an engineer is understanding how your circuits need to be constructed. It's great if you design a high-frequency amplifier, but you also need to build the thing to make it work.

I think that certain curriculums are missing the connection between EE theory and EE implementation. That critical bridge separates the world of the clean classroom from the development lab. There are too many EEs who graduate from college completely unaware of non-idealities, and who have little breadboarding experience. It is true that much of this knowledge can be acquired in the first years of one's career. However, this great disconnect between theory and implementation scares many graduates away from becoming engineers. Instead, many choose to pursue graduate degrees in lieu of work. The disconnect often intensifies, and instead of joining the engineering community, these people go back into academia as professors. This is not a good cycle. Perhaps colleges should hire as professors engineers with years of solid experience?

(Naw-how could they ever be so practical?? /rap)

As for solutions to this problem... The best solution is co-op where a student takes a bit longer to earn a degree, but spends a significant amount of time working for a real company producing a real product.

(Check. /rap)

The second best solution is an emphasis on interesting, relaxed lab work. Don't give eight canned lab projects to a student each semester. Sit down with each individual student and come up with a development path.

"So you find walkie-talkies interesting? How would you like to try and build your own? You start by building an oscillator..." But this approach requires a great investment of time and motivation on the part of the instructor. Is it a price that our higher education community wants to pay?

WELL—I sent Mark a nice long note indicating all the places I agreed with him. I asked him if he thought the world didn't need a "Pease-Balch College of Practical Electronics and Hard Knocks (and Breadboarding)." That may take a little time, though.

All for now. / Comments invited!
RAP / Robert A. Pease / Engineer
rap@webteam.nsc.com—or:

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READER SERVICE 190

Anniversary Time:

Looking Back To Beginnings.

This month's column date marks a couple of milestones in my publishing history. First of all, it is the first anniversary of this column's startup. Over the last year, we've seen 13 serial columns, composed of both short monthly types as well as two more lengthy ones within the Analog Special issues. January 1998 also marks another key date for me, as back in January of 1968, I had my very first ever article published, an "Idea for Design" piece within ELECTRONIC DESIGN.[1] So, this present column looks back at these two ELECTRONIC DESIGN beginnings with some considerations for the future.

Topics for Tools and Tips: Regular columns such as this one become rather unique vehicles of communication, for several good reasons. First, a column confines one to a narrow form of presentation, mostly due to finite space budget. Given that, it also forces the author to write more concisely and clearly just to get the point across. These factors, of course, hone down the list of eligible topics, as many analog design areas just can't be adequately covered in the slim format of a regular monthly column.

Planning ahead for such a column can be almost an exercise in futility. You may have very good intentions in doing so, but in the end, what really matters most is whether readers react to it. If they do, maybe it was your great planning and topic choice. But, if they just don't react, does that mean your planning was bad? Not necessarily so—maybe you just didn't manage to hit their hot button that month. But then, don't persist in missing those hot buttons, as that could mean you are uniformly bland!

Looking back over 1997, it has been a learning experience. Going in, I had imagined that readers would be most interested in topics related purely to analog design, such as the Analog Special issue circuits presented, the book reviews, and so on. But, while there were some good responses on these, by far the most numerous and lively replies resulted from the two "Computer Tech Support" columns, followed closely by the July 7 column on "EEs and the Audio Hobby."

Searching for what's behind the meaning of these spikes in reader response leads me to suspect that analog oriented readers aren't always thirsting solely for new design tricks. Maybe some things *do* supersede when they hit a hot button. If a topic comes by that touches on an everyday problem, particularly one that transcends regular duties, then this message can attract many more people. And, if the problem under discussion is sufficiently serious and widespread, then you just might see a veritable flood of responses.

I suspect that the "Computer Tech Support" columns fit this description, simply because more and more of us use PCs routinely, and have seen the dark underside of the PC world first hand. The PC support problems we all have aren't getting better, they are getting worse! I anticipate more discussions of these support issues in coming months, based on continuing feedback received since the November 3, 1997 column.

On the other hand, understanding hot/cold interests on audio-related topics is nowhere so clear cut. In fact, with the just-published audio-oriented topic in the November 17 Analog Special issue, the response has been far less than that of the July 7, 1997 column. It could be that this is simply due to the focus of the particular audio topic for the November 17 column, specifically slanted toward professional audio. I know that there is a great deal of audio interest out there. But, I also know that audio is an extremely broad topic, and pro-audio issues wouldn't necessarily be appealing to those involved on a hobby or entertainment basis. Perhaps you readers can tell me what the difference is.

Looking Back to Beginnings: Hopefully, our readers can forgive my immodesty in discussing an old circuit of mine which is now exactly 30 years young. When I realized that this column wasn't just marking a 1-year **Tools and Tips** anniversary, but it was also a 30-year anniversary of my first ever publication, this changed the perspective. I decided to look more closely at that old circuit, to see what it might still hold as worthy of current discussion.

The circuit in question has been excised from the ELECTRONIC DESIGN archives, and is reprised here in the Figure, just as in the original. I'm not going to repeat all that was said about it, but I will point out some fascinating points that actually make the technique described just as viable even today, using either today's parts, or alternately, original equivalents. **Question:** How many circuits designed 30 years ago can still be considered viable today?

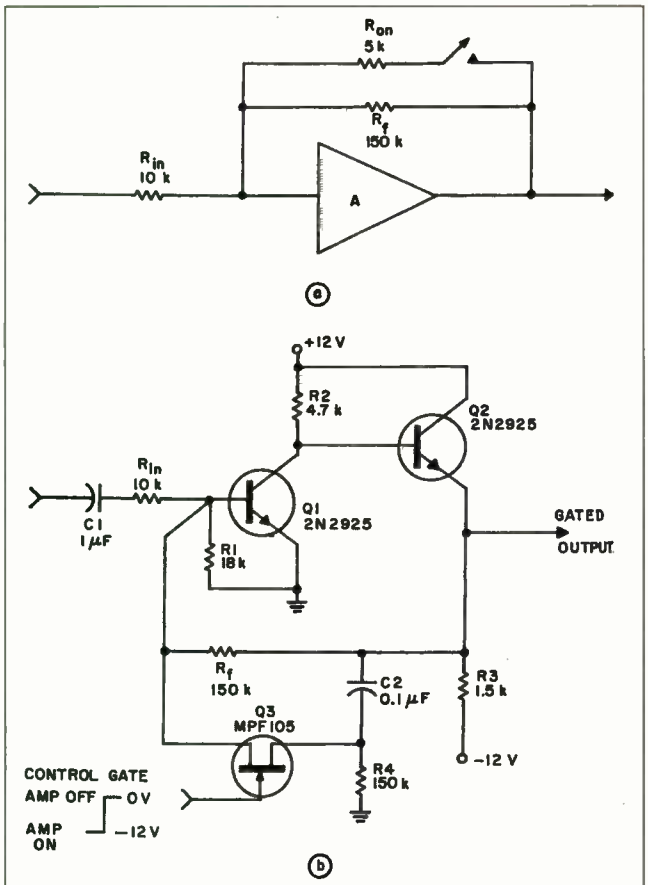
WALT JUNG

The premise of the original article was that standard junction FET devices, because of their moderately high "on" resistance (R_{on}), don't make very good video-switching elements used just by themselves. Generally, that's still true today. But, if the FET switch is configured to operate in the feedback path of an amplifier so that it effectively shunts a much higher resistance, then a moderate R_{on} in the FET won't necessarily be a problem. Further, the amplifier can provide a buffering effect at the input and output.

This concept is shown in functional form in the Figure (a), where the amplifier is shown generically. Note the absence of a (+) input reference terminal for this amp—it is inverting only, with the ground reference understood (its actually Q1's emitter, in the Figure (b).

But (Ahem!) I must confess to an unfortunate rookie mistake at this point. As you can see, the FET R_{on} shown is 5 kΩ. In general the R_{on} will be 1/gm, and for the device under discussion, the gm is specified as 2000 μmhos (for the still-available 2N5459, the JEDEC successor to the original MPF105). This works out for R_{on} to be 500 Ω, not 5 kΩ, so this FET is a much better switch than originally given

WALT JUNG



High-speed switching is possible with a FET connected as shown (b). Simplified schematic is in (a).

Since this circuit functions as an op-amp type inverting gain circuit, the ideal gain is R_f/R_{in}, where R_f and R_{in} are the amplifier's effective feedback and input resistances, respectively. Of course, overall performance is subject to the limitations of the rather modest amplifier, where the main virtue is low cost. R_f is dynamically switched by the FET, via the CONTROL GATE input.

The change is from 150 kΩ in the high gain, or amplifier ON state with the control input low, to the low gain or OFF state with the control input high, where R_f becomes 150 kΩ || R_{on}, or ~498 Ω.

Thus, the inverting gain is either about 15 times with the amplifier gated ON, or about 1/20 when OFF. This equates to a calculated dynamic gain reduction of about 50 dB. It is worth noting to anyone trying this type of circuit that there may be some variation in the FET R_{on}, since the FET channel is dc biased at one V_{BE}, and the control signal positive excursion is ~0V. This uncertainty can be eliminated, if desired, by use of a simple diode level shifter to the FET gate.

To quote from the original article, here are two of the key performance attributes of the circuit:

There's a low output impedance from Q3's emitter under all signal conditions—an advantage that is not possessed by conventional series or shunt choppers.

In addition, a constant input impedance, R_{in}, under all signal conditions—also not characteristic of series or shunt choppers.

TIP: So, what we have in this circuit is an old technique, but one basically just as viable today as it was 30 years ago. The circuit was originally designed when I worked for a small Maryland company, Maryland Telecommunications Inc. (MTI—no longer in business). As best I can establish, the use we then had for it was a gating circuit for a video-processing system, where the (b) circuit, driven by suitable horizontal and vertical sync derived timing signals, opened a controllable active video window over one central portion of the screen.

So yes, we were doing windows all the way back in 1968! And we had a lot of fun with video circuits back in those days. In digging out the history of this circuit, I appreciated helpful comments from a couple of MTI co-workers and good friends from back then, Dick Groom and Al Levin.

My January 1968 article was the first of a long series of "Ideas for Design" published in ELECTRONIC DESIGN. Later on, they were supplemented with many feature articles, and I'd venture the total list has grown to more than 60 by now.

Over these past 30 years, I have been fortunate to work with many different ELECTRONIC DESIGN editors, and with each the experience has been both pleasurable as well as professional. Let's hope we can keep it up!

Next month, we plan to get back onto a more conventional column schedule. As I hope will be clear from remarks above, your comments on future directions will be helpful. Here at the close of 1997, I'd like to take the opportunity to thank all of those readers who took the time to write within the past year, and hope that they (and more of you) will continue to do so in 1998. May you all have a prosperous new year, with fully successful analog designs, and be totally devoid of PC crashes and support problems!

Walt Jung is a corporate staff applications engineer for Analog Devices, Norwood, Mass. A longtime contributor to Electronic Design, he can be reached via e-mail at: Wjung @USA.net.

References:

1. Walter G. Jung, "Gated amplifier uses FET in feedback loop", ELECTRONIC DESIGN, January 4, 1968.

credit (note — the R_{on} error was corrected in a subsequent 1968 follow-up in ELECTRONIC DESIGN).

Despite the quoted R_{on} error, the complete circuit as shown in (b) worked quite well indeed, as you might expect. The original amplifier used 2N2925 general purpose NPN transistors for Q1-Q2, which were popular at the time. I don't know if they are even still available, as neither Newark and Allied now list them. But despite that, I'm also sure that 2N3904's in the same circuit would just work fine and do the job.

So, you could actually build this same circuit today for an active parts cost of a buck or less (much less if you find a inexpensive FET). Or, you could also spif it up by using a video op amp for the gain stage, making the new form of the circuit look a lot more like (a). This would allow for full dc coupling at both input and output, whereas the (b) form must be ac coupled. And it also would allow driving lower-impedance loads.

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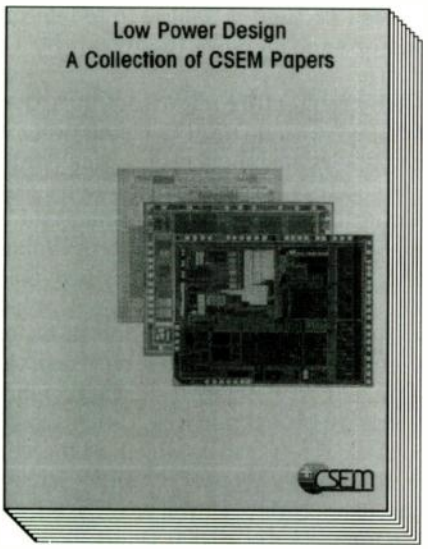

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Four-Port Repeater Chip Developed For Fast Ethernet

There's a new kid on the block in the family of IEEE 802.3-compliant high-speed networking products—the NWK954 unmanaged Fast Ethernet repeater IC. The four-port 100Base-TX repeater IC integrates complete controller and physical-layer (PHY) functionality onto one chip. This creates a 25% reduction in silicon cost compared to already existing conventional non-integrated solutions. The device, equipped with the manufacturer's NWK950 controller and four NWK939 transceivers, is cascadable and stackable, giving manufacturers a more cost-effective route to Fast Ethernet hub design.

The controller receives and retransmits data signals, detects collisions, and negotiates between ports in response to collision or fault conditions. The four NWK939 blocks provide complete PHY capability, including signal equalization and recovery of clock and data. The NWK954 repeater core passes 5-bit 100Base-TX symbols between the on-chip 100Base-TX transceivers and the expansion ports. The core provides a link/activity LED driver for each port, a receive error LED driver for each port, a single collision indicator LED driver, and a utilization/performance display on five LED drivers. Each twisted-pair port incorporates all of the functions required for 100Base-TX reception and transmission through standard 1:1 magnetics.

The NWK954 is driven with a single 25-MHz reference clock and implements power-saving features on unused ports. The chip is equipped with local and backplane expansion ports in order to cascade up to six NWK954s on the same circuit board. With the addition of a backplane driver/receiver, customers can stack up to 10 hubs to accommodate workgroups of up to 240 nodes. In any configuration, a hub will be compliant to Class II standard that allows two hubs per network segment. The NWK954 is packaged in a 128-pin PQFP and costs $29.50 (U.S.) in 1k quantities. AV

***GEC Plessey Semiconductors (GPS)**, 1735 Technology Dr., Suite 240, San Jose, CA 95110, USA; (408) 451-4700; fax: (408) 451-4710/4715.* **CIRCLE 492**

Two USB Controllers Offer 1.5- And 12-Mbit/s Transfer Speeds

The C500 family of 80C52-compatible microcontrollers has two new members—the C540U (4 kbytes of ROM) and the C541 (8 kbytes of ROM) both offer a USB implementation with two different transfer speeds, either 1.5 Mbits/s or 12 Mbits/s. The USB protocol supports the four different transfer types: control, interrupt, bulk, and isochronous. Control is used to read the information in the descriptors contained in the device registers, also called end points. The interrupt transfer type is used for such peripherals as game controllers, keyboards and mouse pointing devices. The bulk type is utilized by devices such as printers or scanners, while isochronous is dedicated to telecommunication transfer such as voice to guarantee a constant transfer rate.

The USB architecture allows hot insertion for true "plug and play" with no need to install proprietary drivers when a new peripheral is physically attached to the bus. In addition to the C540U's features, the C541U offers a programmable watchdog timer and asynchronous serial-communications interfaces. Volume prices of the devices are reported to be at about $3 (U.S.) for the C540U or $3.50 (U.S.) for the C541U. Placed in the price range of 8-bit controllers, the 16-bit controller C161RI offers a C166 core and a two-channel I^2C bus with multimaster capabilities and the possibility to address it with 10 bits at 400 kHz. With an integrated real-time clock, the IC can be waken from sleep mode at any time. It offers 3 kbytes of RAM, five timers, and an 8-bit, four-channel ADC as well as a UART and SPI interface. In quantities of 10,000, the IC is priced around $7.50 (U.S.). AV

***Siemens AG**, RK F/B3, 90713 Fuerth, Germany, fax: +49-911/978-3321.* **CIRCLE 493**

Remote Management System Handles Site Monitoring, Control

The RMS 4000 is a user-configurable remote-management system for site monitoring and control in local or remote installations of various sensors and equipment. Included is a microprocessor-controlled remote monitoring system for managing power and ancillary equipment, including the ability to communicate and alarm conditions or receive new operational parameters. The unit can manage the operational requirements of its own location without involving external communication—the system only communicates when an exception occurs, as defined by local settings, so that the transmission of irrelevant information and the danger of false alarms are minimized.

The system can be controlled locally from a simple terminal, or remotely via a modem or X25/frame-relay option. The level of intelligence and decision-making built into the system is variable, depending on the application. For many applications, including intruder, flood, fire, or temperature alarms and power condition monitoring, integrated solutions are available. Input and output analog, as well as digital signals of various formats, can be monitored and controlled. Front-panel push buttons and an illuminated LCD allow users to monitor and set up various operational parameters. RE

***Texcel Technology Plc**, Thames Rd., Crayford, Kent DA1 4SB, United Kingdom; phone: 011 44 1322 557722; e-mail: http://www.texceltechnology.demon.uk.* **CIRCLE 494**

Edited by Roger Engelke

WHAT DO THESE WORDS MEAN TO YOU?

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After much thought and discussion, our editors have developed a new tag line that is about as direct and to the point as one can possibly get. It describes who we are and what we do. These four words tell our readers and advertisers what *Electronic Design* is all about:

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This new tag line reflects how *Electronic Design* reports on both emerging and new *technology* garnered from the movers and the shakers of this global industry. We report on and analyze how new technology will work in various *applications*. We then report on and analyze new *product* introductions. Finally, we offer you, our readers, *solution* articles and design ideas that help you and your peer engineers to build better products in this very competitive arena. These four words also represent the stages in which you, the design engineer, work.

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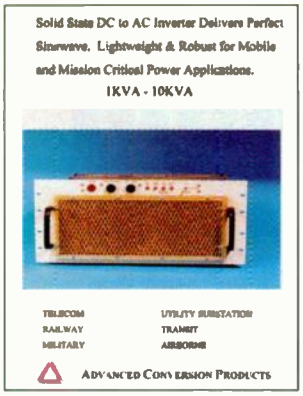

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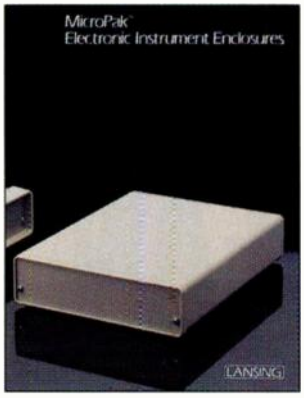

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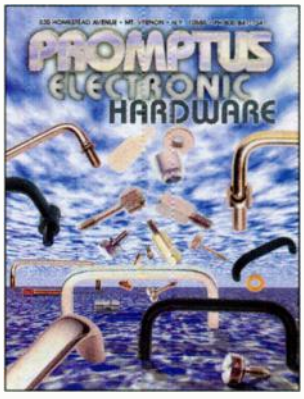

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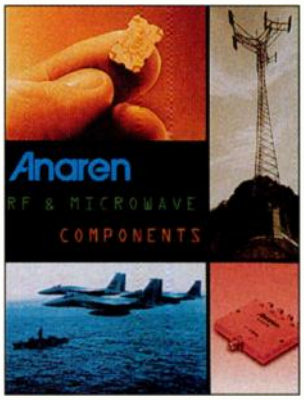

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Cell Libraries For 0.20- And 0.25-µm Design Now Open

Upgraded design libraries with improved design rules and performance specifications are available for the 0.20- and 0.25-µm (drawn) design-rule processes released earlier this year by VLSI Technology. The VSC9 and VSC10 processes, respectively, provide chip developers with circuit densities that pack about 40,000 and 54,000 gates per square millimeter.

The VSC9 and VSC10 design libraries will be available in the first quarter of 1998. They will allow designers to create single-chip system solutions thanks to a database of over 600 basic cells and a large selection of complex core functions, such as 32-bit processors, memory blocks, and many others.

The VSC9 technology is optimized for 2.5-V operation, but the I/O blocks are designed to handle 3.3-V interfaces. The VSC10 technology is optimized for 1.8-V operation and supports both 3.3- and 5-V tolerant I/O interfaces. DB

VLSI Technology Inc., *1109 McKay Dr., San Jose, CA 95131; (408) 434-3000, or on the web at http://www.vlsi.com.* **CIRCLE 572**

Graphics Chip Set Delivers 3X Performance Boost

The Voodoo 2 graphics chip set provides system designers with a 3X performance improvement over the company's previous Voodoo chip set. The expandable architecture of the Voodoo 2 chip set is supported by a 192-bit memory interface and a 2.2-Gbyte/s data bandwidth. The graphics compute engine in the chips performs over 50 billion operations/s. Consequently, chip set can deliver a graphics performance of 3 million triangles/s and 90 million dual-textured, bilinear-filtered, per-pixel MIP-mapped alpha-blended and Z-buffered pixels/s.

Included on the chips is a full floating-point hardware triangle setup engine to offload the host processor from the task of performing the graphics computations, thus freeing the CPU for other system tasks.

In the basic chip set are two texture processing units that simultaneously apply two textures to a triangle for single-pass, single-cycle rendering of effects such as trilinear filtering, sophisticated lighting, spotlights, and detail texturing. At the board level, multiple boards can be interconnected for even faster game playing. The chip set will automatically detect when a second chip set is present and set up the operations so that even and odd frames are drawn by different boards to speed the screen generation.

It's estimated that boards based on the Voodoo 2 chip set will be able to retail for less than $300. DB

3Dfx Interactive, *4435 Fortran Dr., San Jose, CA 95134; (408) 935-4322; or on the web at http://www.3dfx.com.* **CIRCLE 573**

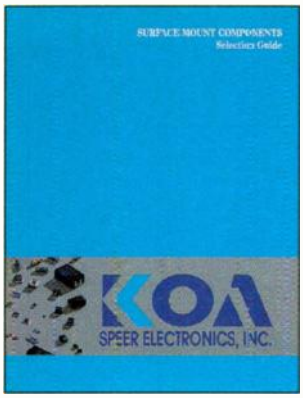
Flash CPLD Packs 128 Macro Cells, Programs In-System

With a complexity of about 6000 gates, the ATF1508AS complex PLD provides designers with 128 macrocells and the ability to configure the chip in the system over a serial interface. The flash-memory-based CPLD is pin-compatible with a like-density device currently available in the market, but offers more features in the macrocells and improved performance thanks to better on-chip connectivity and routing.

The chip operates from a 5-V supply but can interface to 3-V systems as well. It also offers several low-power options—for instance, the "L" version of the chip draws just 3 mA under normal operating conditions., and the chip has a near-zero standby current. The fastest speed grade of the ATF1508AS is specified at 7.5 ns. Four different package options are available, depending on I/O requirements—68, 84, 100, and 160 pins, which translate to 48, 68, 84, and 100 I/O pins, respectively.

Price for the 100-pin PQFP version in the 15-ns speed grade is $12.13 each in lots of 1000 units. The 10-ns version sells for $18.86 apiece in the same quantities. DB

Atmel Corp., *2325 Orchard Pkwy., San Jose, CA 95131; Ravi Pragasam, (408) 441-0311, or on the web at http://www.atmel.com.* **CIRCLE 574**



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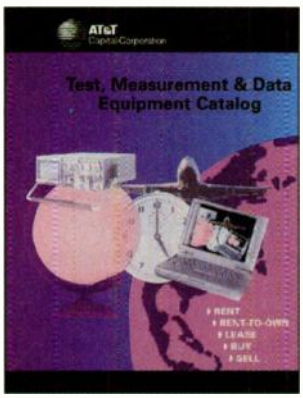

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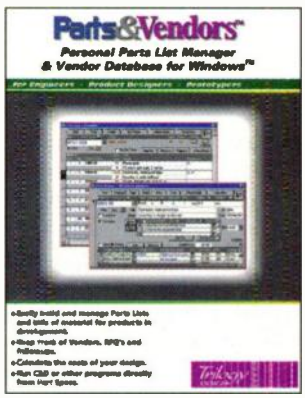

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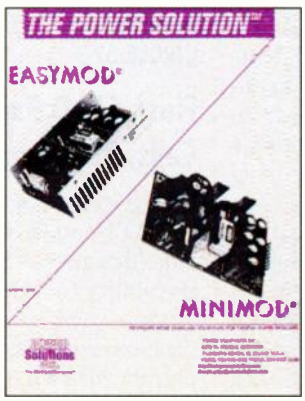

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PCB Design Tools Provide 3D Modeling, Thermal Analysis

Orcad has introduced three interfaces and two updated translators for its Windows NT-based Capture, Express and Layout design software tools. The interfaces allow designers to do either 3D modeling and thermal analysis. One of the interfaces, the IDF 2.0, can be used with 3D modeling software such as Parametric's Pro/ENGINEER. This bidirectional interface communicates pc-board outlines, floorplanning information, component location, and component height. As a result, a pc board can be created in a mechanical system, sent to Layout for initial placement, and then sent back to the mechanical system where it can be modeled and modified as necessary. Then the design is returned to the Layout tool, where all mechanical engineering change orders (ECOs) required by the modeling process can be incorporated into the design.

An IPC-D-356 interface delivers net-list information, component X-Y coordinates, reference designators, and pin numbers in an ASCII format to a bread-board tester and other test and assembly tools. A GenCAD interface addresses the issue of communicating accurate CAD data by delivering the entire pc board database in an ASCII form. This database is suitable for common fabrication and test development software such as Mitron's CB/Test.

All interfaces and translators require the 7.10 version 7.10 of either the Capture, Express, or Layout software tools. Customers with current maintenance agreements can receive them free of charge by downloading from *http://www.orcad.com.* CA

Orcad, 9300 S.W. Nimbus Ave., Beaverton, OR 97008; (503) 671-9500, http://www.orcad.com.

CIRCLE 575

Translation Tools Boast HDL Interoperability

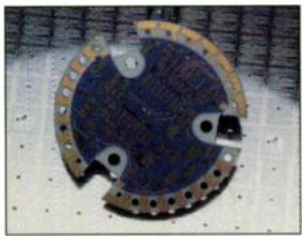
The Jaguar 2.2 analyzer, coupled with the VHDL-Bridge and VITAL-Bridge translation tools, give HDL-based chip and FPGA designers the flexibility to use any language of choice (Verilog or VHDL), as well as incorporate multiple languages in any design. The Jaguar 2.2 mixed-signal analyzer, based on a language-neutral net-list object model and a language-independent procedural interface, provides transparent support and access to structural Verilog, VHDL, and EDIF.

The analyzer delivers a common language front-end. As a result, designers can use both Verilog and VHDL from the beginning of their design flow, instead of just a subset, and be able move between VHDL and Verilog module instantiations. Verilog and VHDL language-dependent procedural interface functions allow the user to access language-specific behavioral information. The tool also boasts a 20% performance improvement over its previous version; support for the IEEE 1076 standard; complete syntax and semantic checks, including a check for RTL compliance; object model browser for debugging; and elaboration functions for fully instantiated designs.

The VHDL-Bridge translator serves as a front-end for VHDL-based tools, while at the same time providing an easy Verilog extension for working with VHDL design flows. The tool works by automatically translating synthesizable Verilog models into synthesizable VHDL models. In doing so, it performs synthesis policy checking against the EDA industry standard, register-transfer level (RTL) subset, and bi-directional name mapping.

The VITAL-Bridge tool also can serves asa front-end tool, enabling chip designers using Verilog-based tools to move their IP into a VHDL environment. All tools are now available on either UNIX or Windows platforms. Jaguar 2.2 has a starting U.S. list price of $20,000 for a development license. An end-user run-time license also may be purchased on an OEM basis. VHDL-Bridge 2.0 has a starting U.S. list price of $20,000. VITAL-Bridge 2.0 starts at $40,000. CA

Interra, 2001 Gateway Pl., Suite 440W, San Jose, CA 95110; (408) 573-1400; http://www.interrainc.com. **CIRCLE 576**



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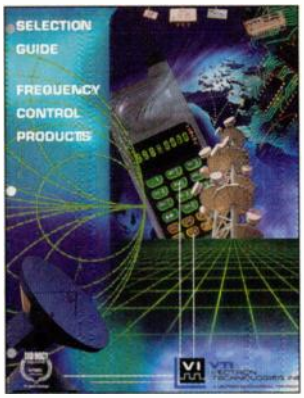

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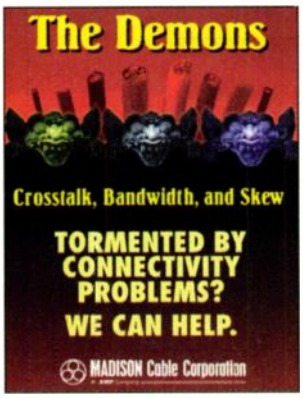

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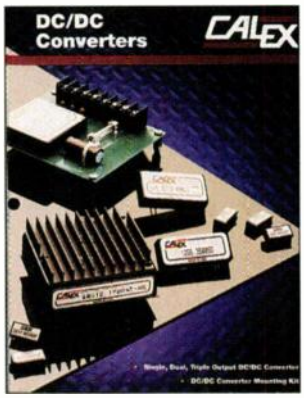

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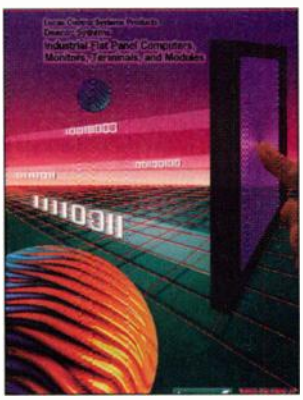

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MAGNETIC SHIELD CORPORATION

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CHIP RESISTORS AND CHIP ATTENUATORS

New literature describes a complete line of chip resistors for solder, wire bonding, and epoxy attachments. Included are specifications for new surface mount MICROWAVE 26 Ghz and very LOW VALUE chip resistors, along with 10 Ghz thin film attenuator. Many sizes are listed from 0.030" X 0.020" to 0.62" X 0.27". Available resistance ranges are from 0.022 ohms to 1,000 Gig ohm and power ratings up to 10W. Engineering kits are also described. Phone: 401-683-9700; Fax: 401-683-5771 or http://www.ims-resistors.com

INTERNATIONAL MANUFACTURING SERVICES

READER SERVICE 163

Software Tools Link Design And Test Of Microcontrollers

The TestDirect pattern generator and Digital VirtualTester pattern debugger from Integrated Measurement Systems will be available to users of the HP 83000 MCU series of microcontroller test systems. TestDirect automatically generates test patterns for automatic test equipment (ATE) using the designer's original testbench simulation environment. The result is reduced cost of test and shorter time to market.

The Digital VirtualTester combines EDA simulation and proprietary ATE data. As a result, it automates the verification and debug of IC test patterns and timing on engineering workstations without having to wait until first silicon and without using valuable ATE time. Time to market also is cut considerably.

The HP 83000 MCU series tests a wide range of microcontrollers and embedded controllers at a cost of less than $2000 per test channel. TestDirect and Digital VirtualTester for the HP 83000 MCU series start at $30,000 and $50,000, respectively. They are expected to be available in the second quarter of 1998. JN

***Hewlett-Packard Co.**, Test and Measurement Org., P.O Box 50637, Palo Alto, CA 94303-9512; (800) 452-4844 ext. 5588.* **CIRCLE 577**

Resistivity Meter Is Updated And Re-Introduced

The FPP-5000, the popular automatic resistivity meter used by semiconductor manufacturers to perform tests that ensure process accuracy during fabrication, has been updated and reintroduced as the FPP-5000-M. The four-point probe measures sheet resistance in ohms/square, slice resistance in ohms/centimeter, and film thickness in mils, microns, or angstroms. Using both rectification and thermal techniques, the instrument also can identify a wafer as N-type or P-type.

The FPP-5000-M is well-suited for epitaxial, diffused, ion-implanted, and metallized layers. It accommodates 6-in. wafers internally, and an optional handheld external probe is available for larger wafers. Also optional is an RS-232 interface for sending measurement data, and operator and wafer identification to a printer or host computer. The FPP-5000-M costs $12,500. JN

***Miller Design & Equipment**, San Jose CA; (408) 434-9544.* **CIRCLE 578**

Spectrum Analyzers Offer More Speed, Resolution

The MS2650B and MS2660B series of portable spectrum analyzers deliver better measurement capability, measurement time, and display resolution than previous models. The MS2650B analyzers cover 9 kHz to 3 GHz, and the MS2660B units range from 9 kHz to 8.1 GHz. The display update rate and personal test automation processing speed of both versions are 30% faster than previous models.

Software enhancements result in improved adjacent-channel power measurement and allow the addition of channel power measurement. The new liquid-crystal display has better resolution and permits brightness control from the front panel or through the GPIB. Now standard are a built-in frequency counter, FM demodulation waveform display, GPIB or parallel interface, and memory card interface. Four models are available at prices ranging from $11,550 to $20,000. JN

***Anritsu Wiltron Co.**, 685 Jarvis Dr., Morgan Hill, CA 95037; (408) 776-8300; fax (408) 776-1744; http://www.anritsuwiltron.com.* **CIRCLE 579**

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http://www.intel.com

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CIRCLE 250

ACCUTRACE INC.

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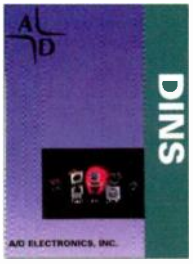
CIRCLE 252

HARTING INC. OF NORTH AMERICA

DINS

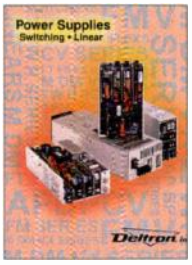


A/D Electronics' free Dins catalog features a variety of Dins in different configurations. 52 page catalog offers mini circular connectors, din sockets, CRT sockets, din plugs, 3&4 pin power connectors, terminal blocks, SCART sockets and plugs, battery holders, pin headers and mini toggle switches. Design engineers can obtain complete specs, dimensional drawings and evaluation samples upon request. 253-851-8005, F 253-851-8090, www.adelectronics. com

CIRCLE 253

A/D ELECTRONICS

NEW OEM POWER SUPPLY CATALOG



Deltron's full line catalog presents many new products including 1kW to 7.5kW T Series power factor corrected front ends for telecommunications systems, DeviceNet power modules, new generation modular F Series 0.99 power factor corrected switchers and Moduflex® M Series switchers. The catalog also details a full complement of time tested higrade industrial and commercial power supplies. For free copy call 800-523-2332 or fax 215-699-2310.

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This catalog enables design engineers to easily locate the correct adapters, clips and test accessories. The catalog includes a Ball Grid Array Reference Guide along with information on over 4000 ET products, including emulator tools, logic analyzer/scope adapters, programming adapters, production/test adapters, debugging accessories, prototyping adapters, field-configurable adapters and custom adapters. 1-800-ADAPTER
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IMAGINEERING

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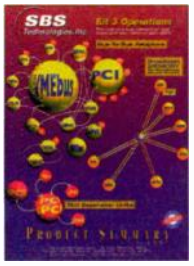

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BIT 3 COMPUTER CORP.

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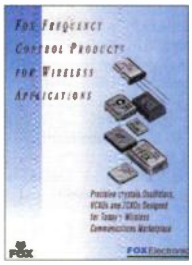

New Fox brochure cover s America's broadest range of frequency control products. Fox Electronics, 5570 Enterprise Parkway, Fort Myers, Florida 33905; 1-888-GET-2-FOX; Fax: 941/693-1554; e-mail: sales@foxonline.com; via the web www.foxonline.com. Note: Please forward all reader service inquiries to Customer Service, Fox Electronics, 5570 Enterprise Parkway, Fort Myers, FL 33905.

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FOX ELECTRONICS

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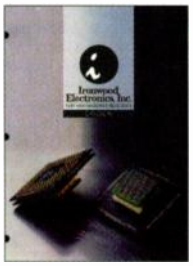

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IRONWOOD ELECTRONICS

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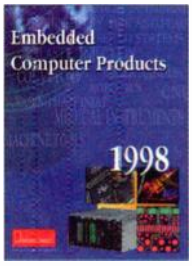
Bud Industries' new Standard Products Catalog provides technical data and ordering information on over 3,000 products ranging from large relay racks and cabinets to desktop and portable instrument cases including a full line of NEMA and other plastic enclosures. Also included is information on computer workstations, custom fabrication and a wide range of enclosure accessories.

CIRCLE 262

BUD INDUSTRIES, INC.

EMBEDDED COMPUTER PRODUCTS



Gespac's 1998 catalog features a full line of 3U embedded PCs, 68XXO SBCs, motion control and over 200 I/O functions. The G-windows GUI for real-time systems running. OS-9 is also offered. www.gespac.com or Phone 800-443-7722

CIRCLE 263

GESPAC INC.

Electronic Components/Hardware Guide

As an ISO 9002 manufacturer, Keystone Electronics offers more than 5,000 standard and custom components and hardware products for industry. These include: interconnect components; panel and printed circuit hardware; spacers and standoffs; insulating hardware; fuse clips and holders; battery holders and accessories; and custom manufactured, stamped, and more. This handy guide provides an overview of all Keystone major products. Tel: 718-956-8900.
e-mail: kec@keyelco.com

CIRCLE 264

KEYSTONE ELECTRONICS CORP

ELECTRONIC DESIGN CATALOG/LITERATURE REVIEW

1998 CHANNEL K CATALOG

Keithley Instruments' 1998 Channel K Catalog presents PC-based & standalone measurement solutions for benchtop, distributed, and portable applications in the lab or factory. These include real-time DA/controller boards, DA and communications PCMCIA cards; miniaturized instruments with built-in signal conditioning; motor controller boards; benchtop and board-level DMMS and VMMs; and more.

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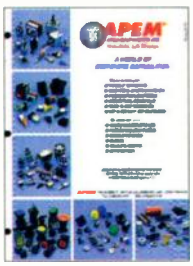

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APEM

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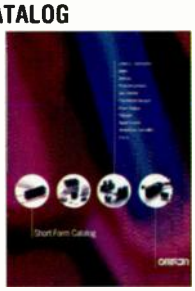

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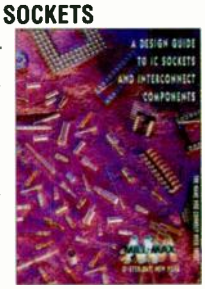

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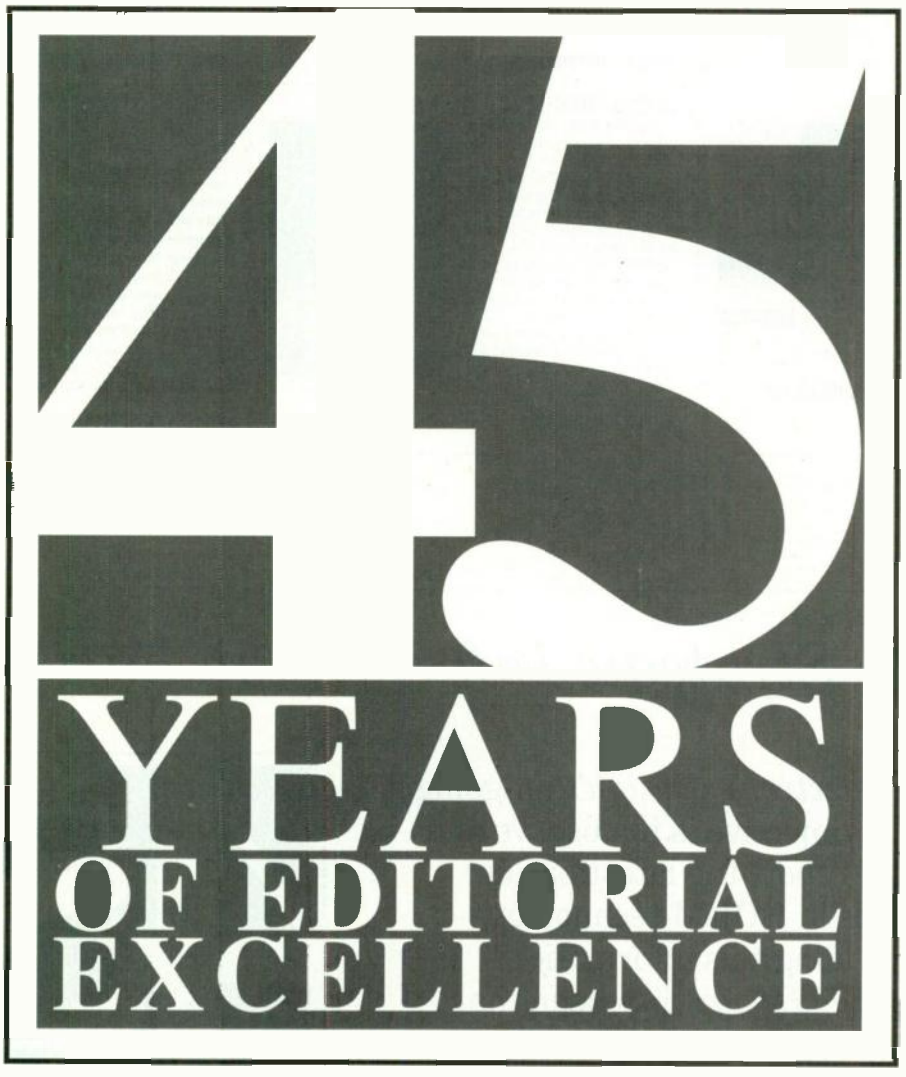

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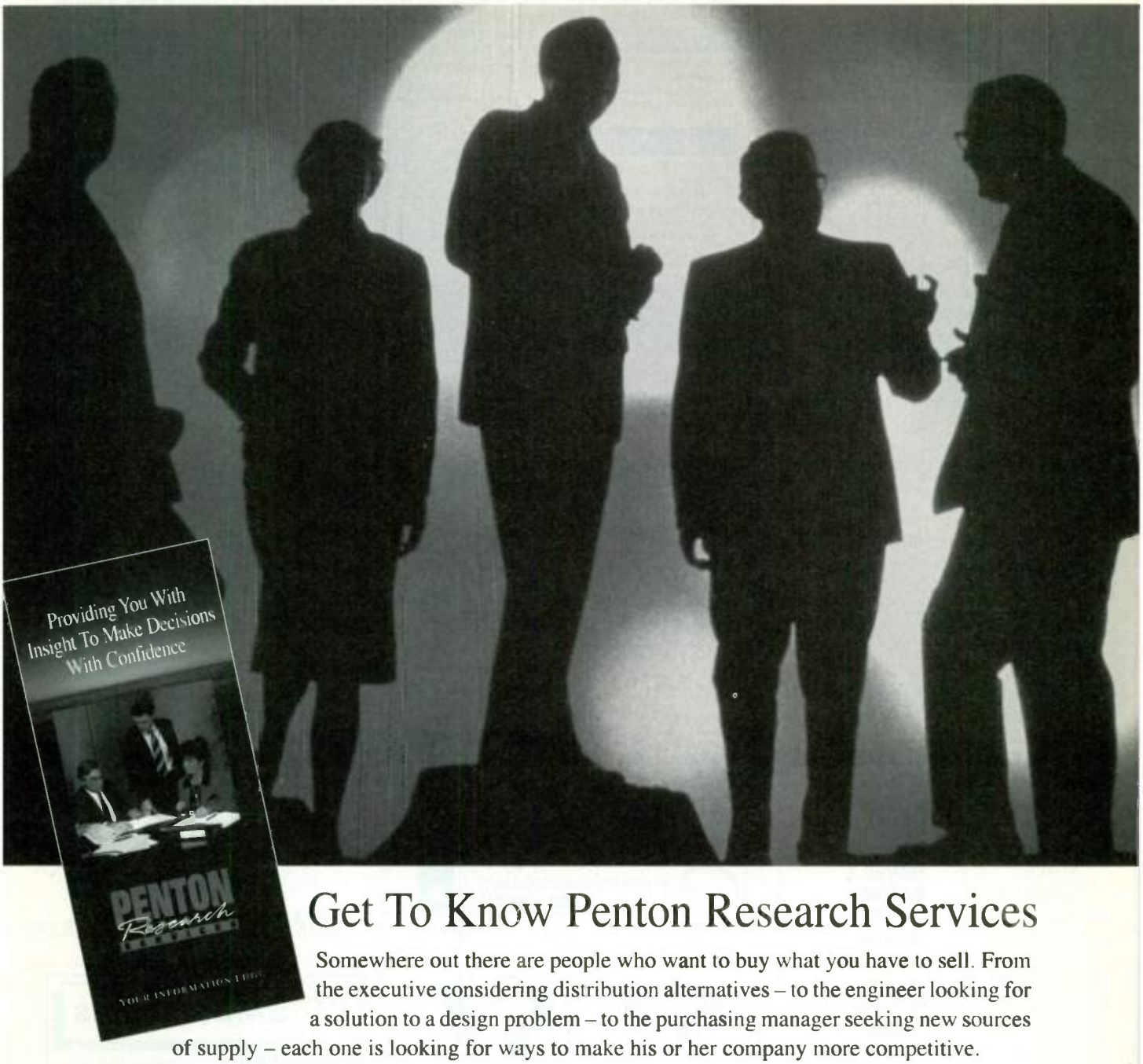

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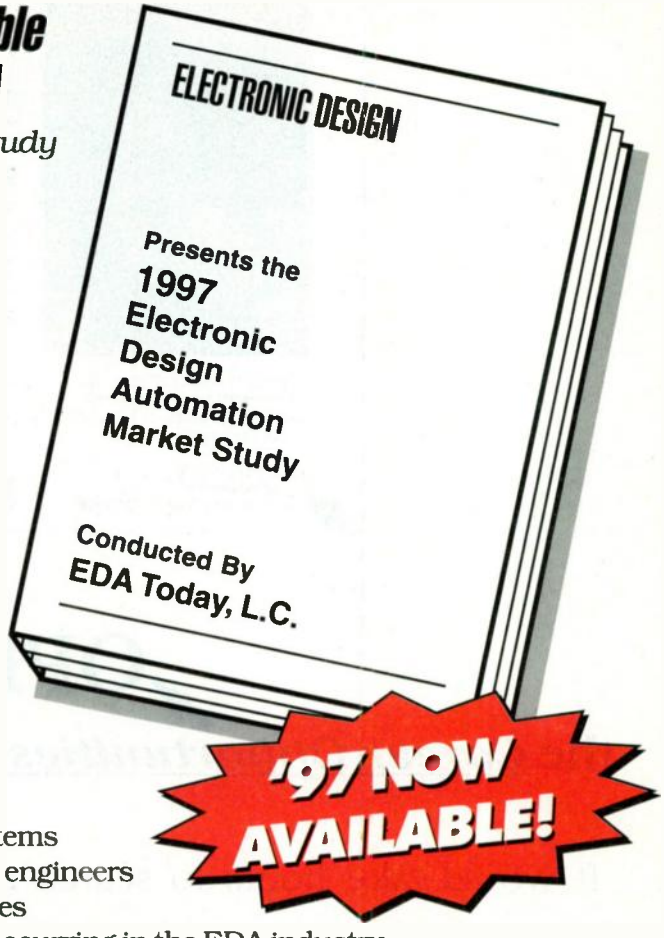

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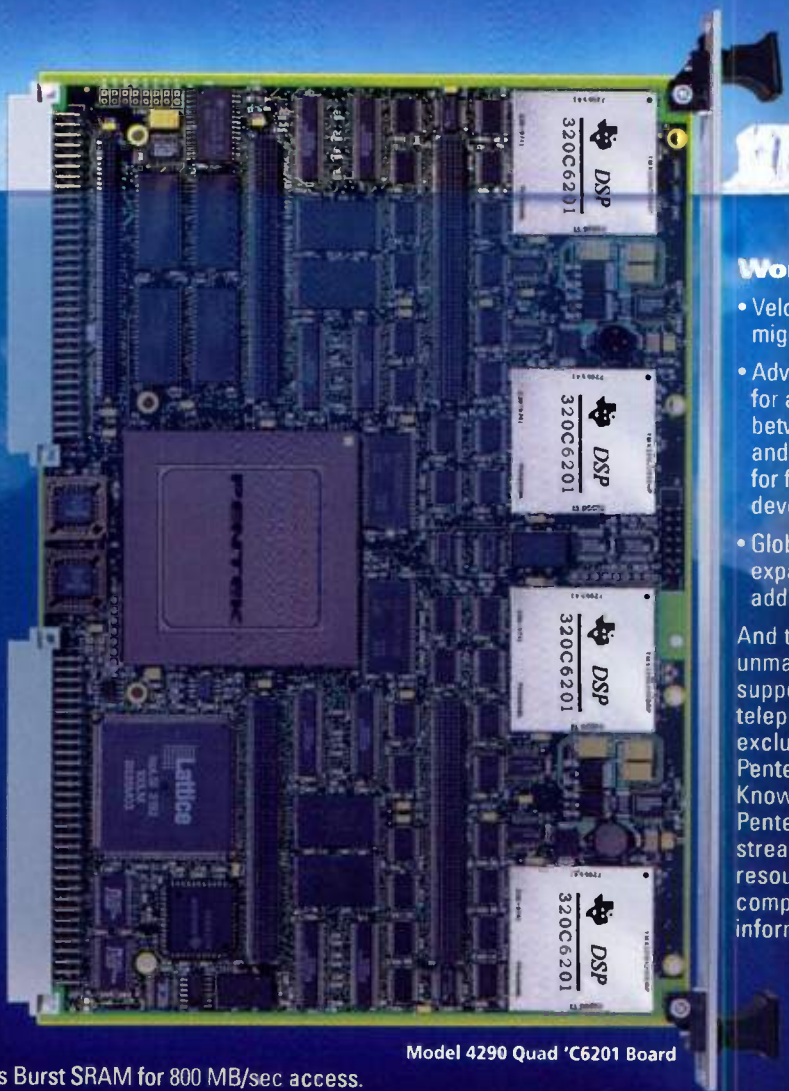

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