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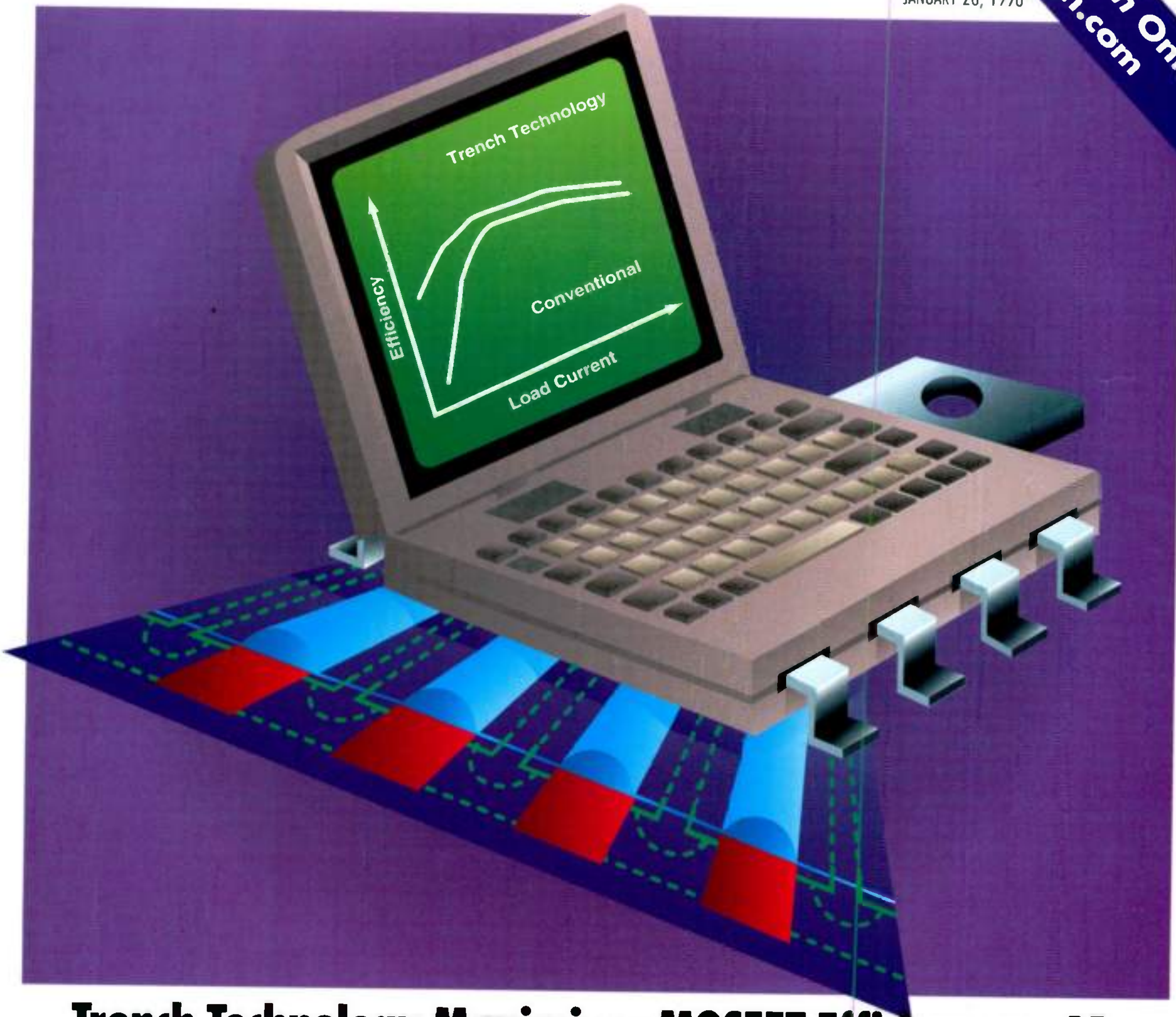

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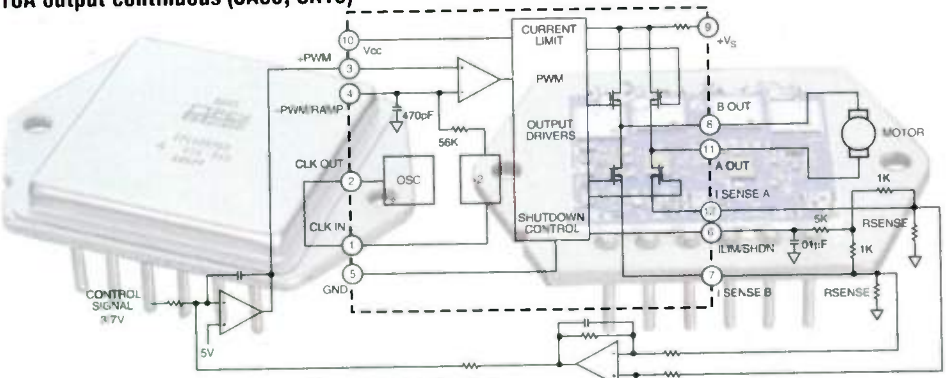

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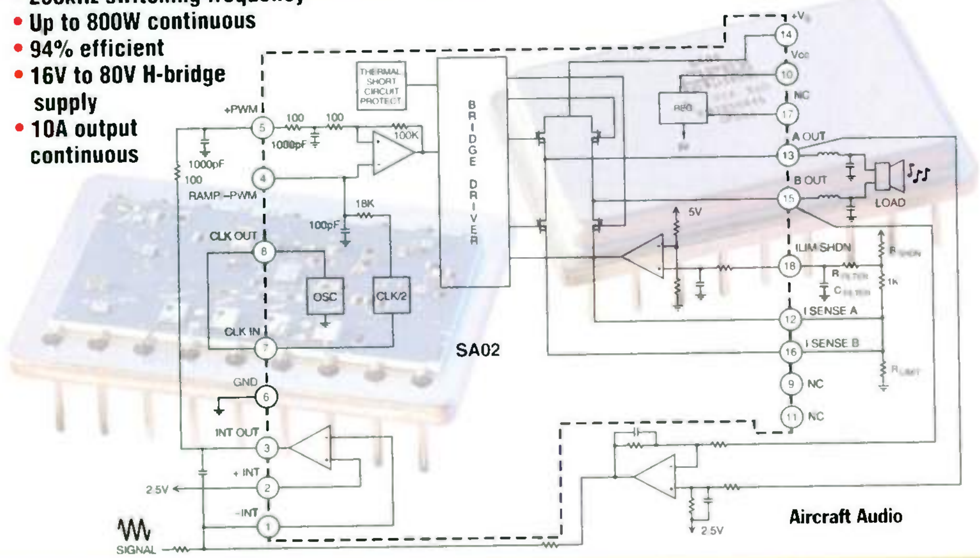

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EPF10K50V	50,000	2,880	20 Kbits	40%	110%	3.3 V
EPF10K100A	100,000	4,992	24 Kbits	35%	107%	3.3 V

1. Estimated performance with -2 speed grade using MAX+PLUS II v. 8.1 compared with -3 speed grade using MAX+PLUS II v. 8.0.
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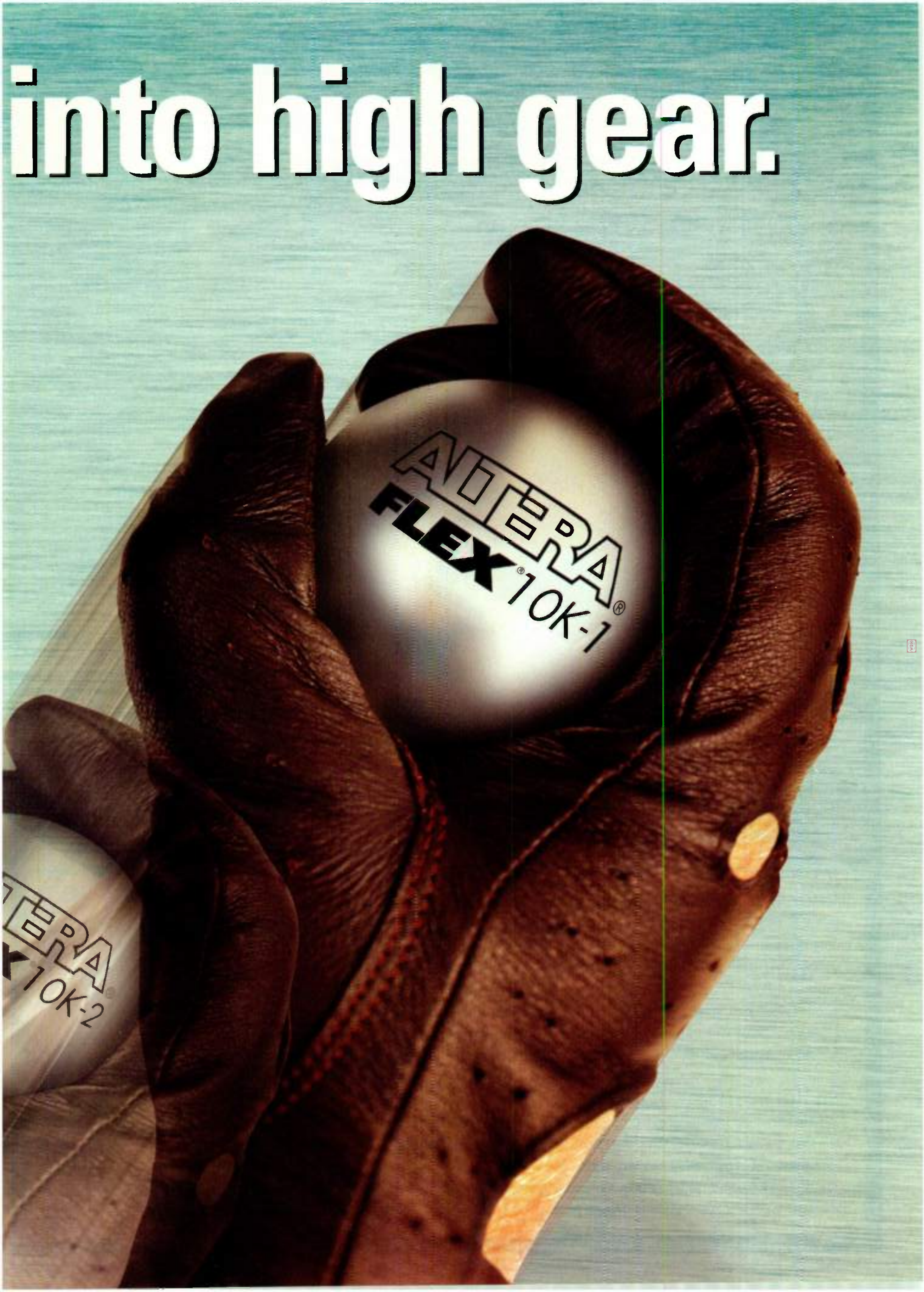
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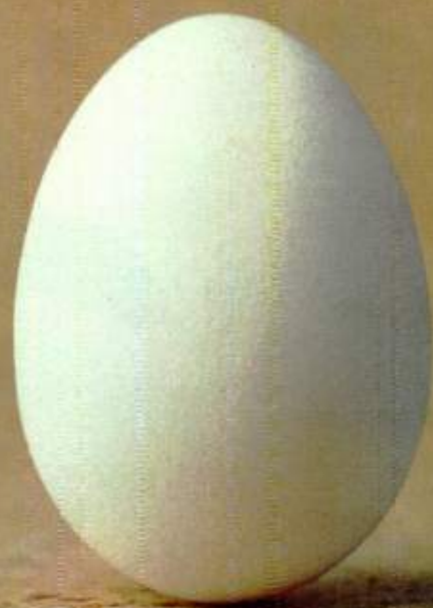

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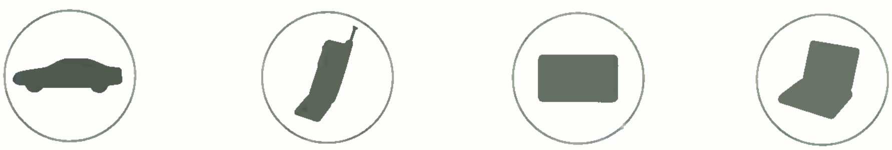

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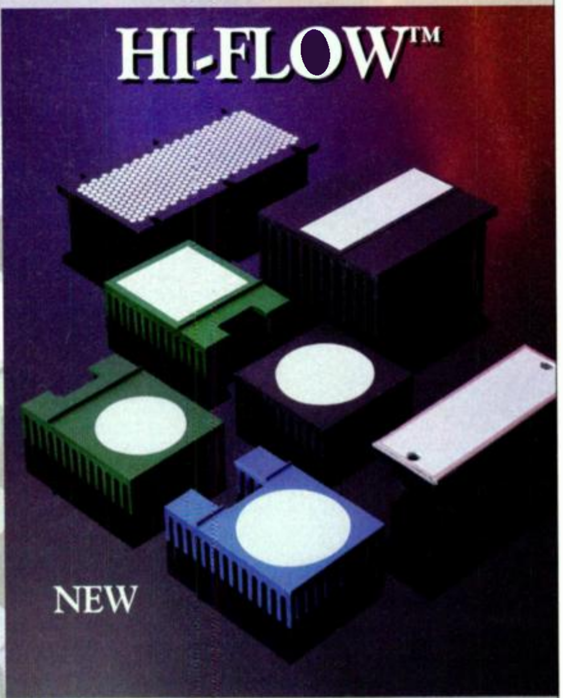

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Portable by Design, February 9-13. Santa Clara Convention Center, Santa Clara, California. Contact Rich Nass, Electronic Design, 611 Route 46 West, Hasbrouck Heights, New Jersey 07604; (201) 393-6090; fax (201) 393-0204; e-mail: portable@class.org.

The Wireless Symposium and Exhibition, February 9-13. Santa Clara Convention Center, Santa Clara, California. Contact Bill Rutledge, Penton Publishing, 611 Rte. 46 West, Hasbrouck Heights, New Jersey 07604; (201) 393-6259; fax (201) 393-6297; instant faxback (800) 561-7469; www.penton.com/wireless.

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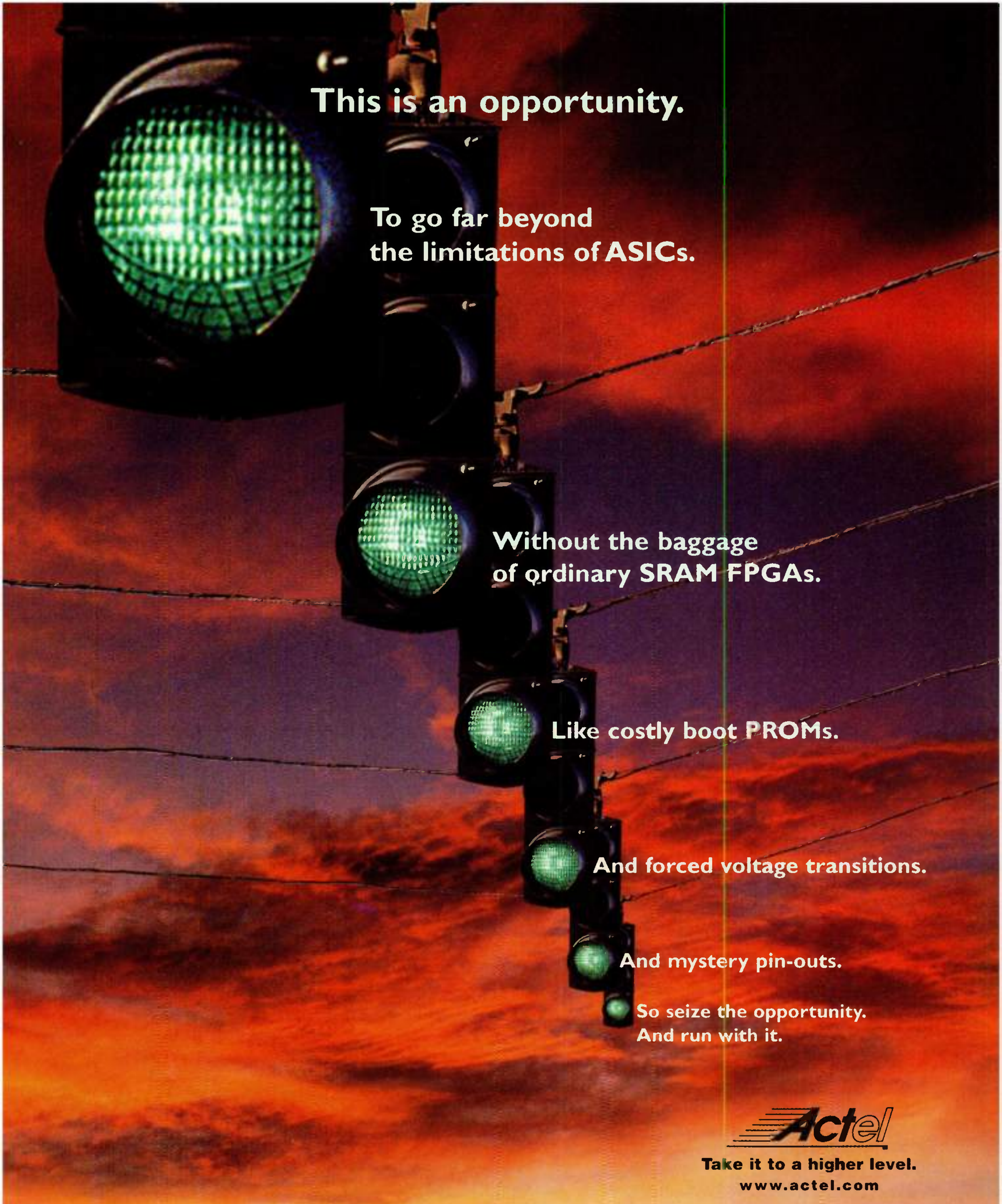
Sixth Annual Automated Imaging Association Business Conference, February 10-12. Buena Vista Place, Orlando, Florida. Contact Automated Imaging Association, Post Office Box 3724, Ann Arbor, Michigan 48106; (313) 994-6088; fax (313) 994-3338.

Asia-South Pacific DAC (ASP-DAC '98) and EDA TechnoFair (EDATF), Feb. 10-13. Pacifico Yokohama Convention Center, Yokohama, Japan. Contact ASP-DAC '98 Secretariat, c/o Convex Inc., Ichijoji Bldg., 2-3-22 Azabudai, Minato-ku, Tokyo, 106 Japan; +81 3-3589-3355; fax +81 3-3589-3974; e-mail: convex@po.iijnet.or.jp.

IEEE Applied Power Electronics Conference and Exposition (APEC '98), February 15-19. The Disneyland Hotel, Anaheim, California. Contact Pam Wagner, Courtesy Associates, 2000 L St. N.W., Suite 710, Washington, D.C. 20036; (202) 973-8664; fax (202) 331-0111; www.apec.conf.org.

Intel Developer Forum, February 17-19. San Jose Convention Center, San Jose, California. Contact Deborah Paquin, (916) 984-1921; deborahx_j_paquin@ccm.fm.intel.com; www.developer.intel.com/design/idf.



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Design, Automation, and Test in Europe Conference and Exhibition (DATE '98), Feb 23-26. Le Palais des Congres de Paris, Porte Maillot. Contact European Conferences, 11C Wemyss Pl., Edinburgh EH3 6DH, UK; +44 131-225-2892; fax +44 131-225-2925.

38th Israel Conference on Aerospace Sciences, Feb. 25-26. Tel-Aviv & Haifa. Contact Technion-Israel Institute of Technology, Haifa 32000, Israel; 972-4-8292713; fax, 972-4-8231848; e-mail: alice@aerodyne.technion.ac.il.

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Computer Telephony Conference and Exposition '98, March 3-5. Los Angeles Convention Center, Los Angeles, California. Contact Computer Telephony '98, 1265 Industrial Highway, Southampton, Pennsylvania 18966; (215) 355-2886; fax (215) 355-4112.

International Verilog Converfence and VHDL International User Forum (IVC/VIUF), March 16-19. Santa Clara Convention Center, Santa Clara, California. Contact MP Associates, 5305 Spine Rd., Suite A, Boulder, Colorado 80301; (303) 530-4562; fax (303) 530-4334; e-mail: lee@mpa-net.com; www.hdl-con.org.

IEEE Aerospace Conference, March 21-28. Snowmass Conferne Center, Snowmass, Colorado. Contact Mike Johnson, 2225 Roscomare Road, Los Angeles, California 90077-2222; (310) 472-8019; e-mail: johnson@ee.ucla.edu.

Second Intellectual Property in Electronics Seminar (IP '98), March 23-24. Westin Hotel, Santa Clara, California. Contact John Whitaker, Miller Freeman Technical Ltd., +44 181-316-3297; e-mail: ed98@cityscape.co.uk.

PCB Design Conference West, March 23-27. Santa Clara Convention Center, Santa Clara, California. Contact Molly Knox, Miller Freeman, (408) 448-6173; e-mail: mknox@mfi.com.

INFOCOM '98, March 28-April 2. Hotel Nikko, San Francisco, California. Contact Ramesh Nagarajan, Lucent Technologies, 101 Crawford Corner Road, Room 3M-318, Holmdel, New Jersey 07933; (732) 949-2761; fax (732) 834-5906; e-mail: rameshn@lucent.com.

IEEE International Reliability Physics Symposium, March 30-April 2. Reno Hilton Hotel, Reno, Nevada. Contact Ann N. Campbell, M/S 1081, Sandia National Labs., Post Office Box 5800, Albuquerque, New Mexico 87185-1081; (505) 844-7452; fax (505) 844-2991; e-mail:ancampbe@sandia.gov.

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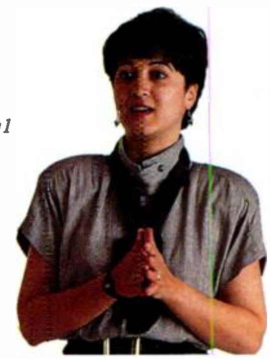

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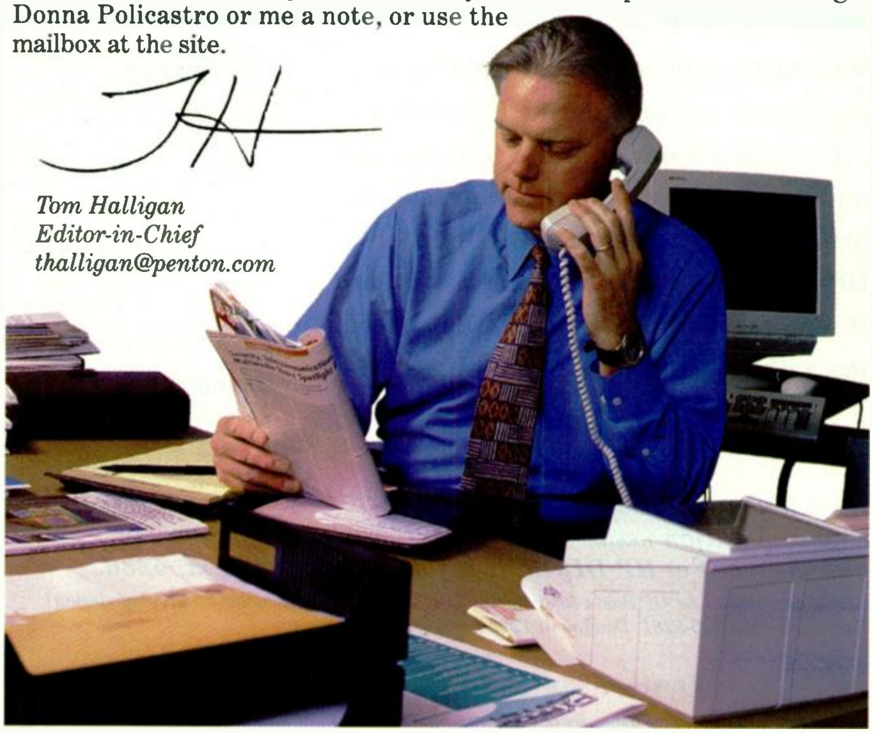

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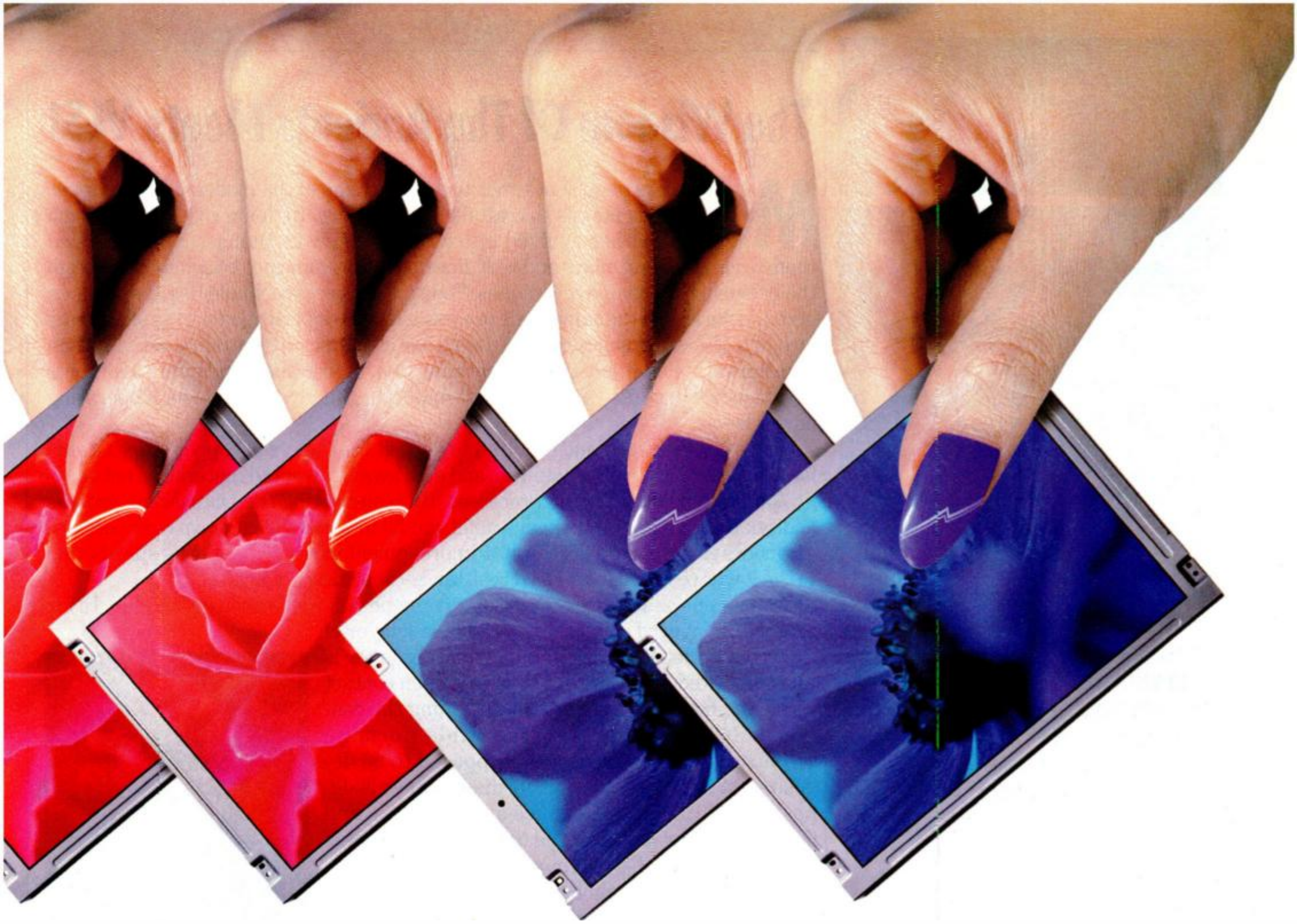

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The Wisdom Of The Ancients Meets VLSI

Metalworkers of ancient times took advantage of the malleability of copper and precious metals to craft delicate jewelry. In doing so, they created a process that has evolved into what we know as Damascene. It allowed them to create metal inlays and very fine detail that could not be achieved through the previously available techniques. Today, IC process technologies are using an updated version of the same basic process to form copper-based wiring on the surface of high-performance chips. Copper has a significantly lower resistance than other metals (aluminum, titanium, or tungsten, for instance) and offers additional performance benefits—it's a low-cost material, and it can handle high operating power levels.

However, the technique required to deposit thin layers of copper onto the surface of a chip, pattern the material, and etch away unwanted material, is not readily compatible with existing processes. By resurrecting the Damascene process and taking advantage of copper's ability to fill in holes and conform over corners, engineers can achieve a 20% to 40% improvement in circuit operating speeds, due to the lower resistance (reduced resistance-capacitance delays).

Damascene actually reverses the way metalization is formed on the chip. If, for example, a layer of copper is desired over a layer of interconnections, a thick oxide insulating layer is first deposited. Next, rather than just open contact holes, the metal wiring pattern (including the contact holes) is etched into the oxide, forming "trenches" wherever metal is supposed to be deposited. After the pattern is formed, copper is deposited, filling in all the holes and trenches, and forming a layer on top of the oxide. The surface is then the chemically/mechanically polished to remove the copper remaining on top of the oxide layer. At the finish, there are copper-filled routing channels and a very planar surface—thus designers can almost keep on depositing four, five, six, or more layers of metal interconnections.

DAVE BURSKY
DIGITAL ICs

Late last year, IBM Corp., Hopewell Junction, N.Y., presented details of its copper metalization process at the International Electron Devices Meeting (IEDM) in Washington, D.C., and demonstrated a 288-kbit high-speed SRAM fabricated with the process. Additionally, IBM will unveil details of a copper-based microprocessor at the international Solid State Circuits Conference in San Francisco, Calif. The microprocessor is a 480-MHz version of the PowerPC CPU that employs six levels of metal interconnects.

IBM isn't alone in its effort to leverage Damascene technology. At IEDM, an entire session was devoted to copper technology, with presentations by IBM, Motorola Inc., Austin, Texas; NEC Corp., Tokyo, Japan; and Mitsubishi Electric Corp., Hyogo, Japan. Most presentations focused on the use of the technology in fabricating circuits with minimum feature dimensions of 0.28 µm or smaller.

The Motorola presentation detailed a process that employs six levels of copper interconnects employed on a 1.8-V, 0.2-µm CMOS technology. NEC delivered two presentations, one on the use of a low-dielectric-constant hydrogen silsequioxane dielectric layer that, along with the use of Damascene copper processing, reduces parasitic capacitances, and the other examining the first formation of aluminum-copper interconnections through the use of chemical-vapor deposition techniques to improve the metal step coverage in circuits with small feature sizes. Mitsubishi researchers detailed a low-dielectric-constant intermetal dielectric (a k of 3 or less) formed by depositing H_2O_2 and methylsilane between the base and cap layers.

Much work still has to be done to optimize the technology, but it only took a few thousand years to reapply the Damascene technique in the first place. The use of Damascene manufacturing is, perhaps, a perfect illustration of human ingenuity—taking old technology and using it with modern updates to solve challenging problems. Now I wonder what they can do with the wheel. . *dbursky@class.org.*

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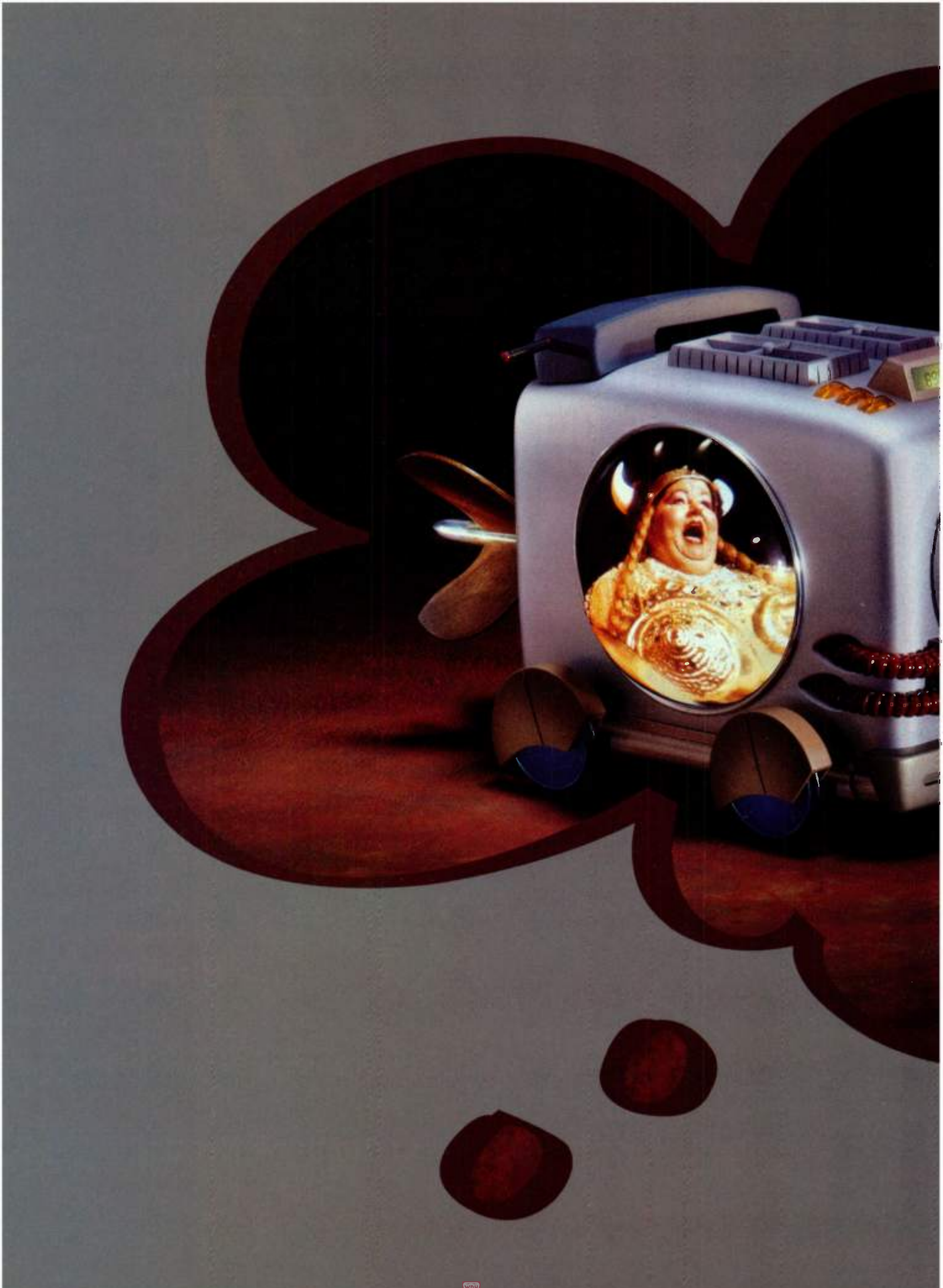

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Joint-Venture 64-Bit Processor Architecture Slated For 2000

A 64-bit RISC processor architecture to be developed jointly by Hitachi and SGS-Thomson Microelectronics is targeted for 1000-MIPS performance. First silicon is scheduled for 2000 with full production in 2001.

The processor core—dubbed SH-5 by Hitachi and ST50 by SGS-Thomson—will be targeted primarily at embedded applications in mass market electronics products such as multimedia PCs, set-top boxes for digital television, "PDAs" and mobile communications terminals, in car multimedia products, digital cameras and video games consoles. Matthew Trowbridge, general manager of marketing and business operations for Hitachi Europe Ltd., says that each company will be responsible for the design of peripheral cells for "system-on-a-chip" designs to address what it regards as its specialist market sectors. SGS-Thomson, for example, will offer specialized MPEG and AC3 cells for digital TV and audio applications. For Hitachi, the emphasis will be on products such as digital cameras, industrial applications, and the like.

Both STM and Hitachi will pool experience and knowledge gained with their current 32-bit processor designs, although Bob Krysiak, general manager and vice president of SGS-Thomson's 16/32/64 & DSP Division, stresses that the new processor will be designed from scratch as a 64-bit architecture device rather than as a revamped 32-bit design. In addition, SGS-Thomson will bring several years experience in the development of a 64-bit processor code named Chameleon. Although the company has produced its first silicon samples of the Chameleon processor, further development will be abandoned in favor of the ST50/SH-5 processor. PF

New Dual Automotive Bus Inching Closer To Fruition

After a series of meetings, representatives of the Consumer Electronics Manufacturers Association (CEMA), the Society of Automotive Engineers (SAE), and all three major U.S. automobile manufacturers have moved farther ahead on developing a dual-bus architecture that will allow multiple OEM and aftermarket devices to be installed easily, cost-effectively, and safely in future cars. A common effort for a universal automobile bus was considered essential because current automobile design cycles of three to five years preclude the use of the latest electronic devices in a car.

Last year, CEMA and its members began work on developing an open, standard interconnect method that would accommodate today's communication, entertainment, and intelligent transportation system (ITS) control systems. The open standard interconnect method will also offer provisions for future developments.

Working with aftermarket electronics manufacturers and CEMA, the SAE intelligent transportation system ITS data-bus subcommittee has released a preliminary version of a dual-bus architecture. The data-bus architecture will permit a wide variety of electronics subsystems to interoperate, share data, and perform control functions on any part of the vehicle. This would allow an aftermarket communication system to use the on-board global positioning satellite (GPS) to relay the ITS coordinates to a service center for repairs, or call for medical attention in the event that airbags were triggered in an accident. In other applications, a car's navigation computer could interact with the driver's laptop computer or personal digital assistant (PDA) to plan routes for salesmen or identify gas stations, restaurants, and tourist attractions within a specified area.

For more information, contact CEMA, 2500 Wilson Blvd., Arlington, VA 22201-3834; (703) 907-7674, fax (703) 907-7690. LG

Software Tool Eases Audio Power-System Design

The Audio Power Program devised by Texas Instruments, Dallas, takes the guesswork out of audio-system design by realistically simulating audio system operation under a variety of conditions. The program, part of the company's strategy to offer comprehensive audio power-amplifier solutions for developers, allows designers to determine power needs faster and more accurately than currently available techniques, leading to more cost-effective systems.

Common methods of estimating audio power requirements are based on a steady-state tone as a rule of thumb. This can sometimes lead to over-budgeting for power output. The Audio Power Program uses dynamic samplings of music and voice to calculate a variety of power-related characteristics of systems operation. Calling up multiple screens enables users to modify system parameters interactively and to compare output reports with ease.

Key features of the program include thermal analysis and computation modes for both linear and Class D-type amplifiers. The program's ability to condense the results of millions of calculations into reports issued in seconds goes a long way toward simplifying the iterative process and enhancing the precision of the overall audio power design. While the program works with all of the company's audio power amplifiers, it is particularly suited to the new line of power amplifiers in TSSOP packages. In this case, the heat-sink path is from a flow-solderable thermal pad on the bottom of the chip. The program is available, free of charge, from Texas Instruments' web site at: *www.ti.com/sc/docs/msp/pran/app_supp/analysis.htm.* PM

Edited by Roger Engelke

MARCH

IEEE International Parallel Processing Symposium/IEEE 9th Symposium on Parallel and Distributed Processing (IPPS/SPDP), Mar. 30-Apr. 3. Delta Orlando Resort, Orlando, FL. Contact Viktor Prasanna, EEB-200C, Department of EE Systems, University of Southern California, Los Angeles, CA 90089-2562; (213) 740-4483; fax (213) 740-4418; e-mail: prasann@ganges.usc.edu.

Embebbed Systems Conference Spring, Mar. 31-Apr. 2. Navy Pier Festival Hall, Chicago, IL. Contact Liz Austin, Miller Freeman Inc., (888) 239-5563; (415) 538-3848; e-mail: esc@mfi.com.

APRIL

20th IEEE International Conference on Software Engineering, Apr. 19-25. Kyoto International. Conference Hall, Kyoto, Japan. Contact Koji Torii, Graduate School of Information Sciences, Nara Institute of Science & Technology, 8916-5 Takayama-cho, Ikoma-shi, Nara-ken 630-01, Japan; +81 7437-2-5310; fax +81 7437-2-5319; e-mail: torii@is.aist-nara.ac.jp.

DSP Spring Design Conference, April 21-23. Santa Clara Convention Center, Santa Clara, California. Contact Liz Austin, Miller Freeman Inc. (888) 239-5563, (415) 538-3848; e-mail: dspworld@mfi.com; www.dspworld.com.

Southeastcon '98, Apr. 24-26. Hyatt Regency, Orlando International Airport, Orlando, Florida. Contact Parveen Ward, ECE Dept., University of Central Florida, Orlando, Florida 32816; (407) 823-2610; fax (407) 823-5835; e-mail: pfw@ece.engr.ucf.edu.

16th IEEE VLSI Test Symposium, April 26-30. Hyatt Regency Monterey, Monterey, California. Contact Rob Roy, Intel Corp., MS:JFT-102, 5300 Elam Young Pkwy., Hillsboro, Oregon 97124-6497; (503) 264-3738; fax (503) 264-9359; e-mail:robroy@ichips.intel.com.

IPC Printed Circuits Expo '98, April 26-30. Long Beach Convention Center, Long Beach, California. Contact Dan Green, The Institute for Interconnection & Packaging Electronic Circuits, 2215 Sanders Road, Northbrook, Illinois 60062-6135; (847) 509-9700 ext. 371; fax (847) 509-9798.

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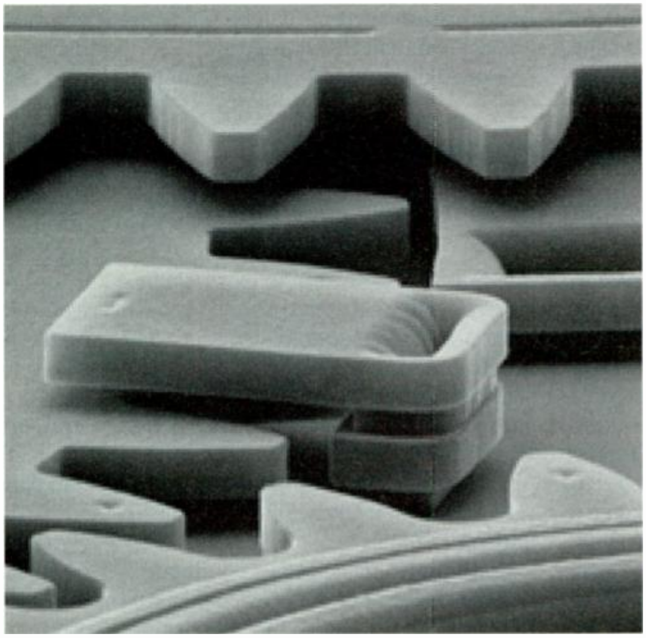
Conference on Lasers & Electo-Optics & The International Electronics Conference (CLEO/IEC), May 3-8. The Moscone Center, San Francisco, California. Contact Amy Hutto, OSA Conference Services, 2010 Massachusetts Ave. N.W., Washington, DC 20036-1023; (202) 416-1980; fax (202) 416-6100; e-mail: cleo.info@osa.org.

IEEE International Conference on Evolutionary Computation, May 3-9. Ankorage, Alaska. Contact Patrick K. Simpson, Scientific Fishery Systems Inc., Post Office Box 242065, Anchorage, Alaska 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@akaska.net.

Micromachined Polysilicon Transmission, The Size Of A Grain Of Sand, Increases Microengine Power By A Factor Of 3 Million

Scientists from Sandia National Laboratory, Albuquerque, N.M., have taken silicon micromachining technology to new levels of miniaturization. They've developed a microtransmission that significantly increases the power of a microengine. According to Sandia's scientists Steve Rodgers and Jeff Sniegowski, "the microtransmission can increase the power of its microengine by a factor of 3 million, theoretically generating enough force to move a 1-lb object. This is quite possibly the most force ever generated by a polysilicon micromechanical device."



Depicted here is a closeup view of Sandia's 3,000,000:1-ratio micromachined transmission. The distance across the photo equals about one-third the width of a human hair. It shows guides that prevent warping as conditions change.

Sandia began work on the microtransmission when it became apparent that due to a phenomenon known as stiction, micromachines need more power than previously thought necessary to overcome friction. Stiction refers to the adhesion and static friction that a stationary gear must overcome in order to begin movement. Often, it is caused by rusting that occurs after a gear is etched in silicon and the surface is allowed to oxidize into glass. The result is that microgears become bound to the stationary surfaces surrounding them. Water vapor and outgassing from epoxy materials also has been known to block the startup movement of a microgear.

Sandia's microtransmission is specifically designed to overcome this obstacle. It is no larger than a grain of sand, with gear wheels the diameter of a human hair. It comprises six identical intermeshing gearing reduction units, each with two dual-level gears operating at ratios of 3:1 and 4:1. Together, the two gears, designed to fit one on top of the other, form a 12:1 reduction ratio. A reversible gear makes it possible to either increase or decrease speed. A coupling gear also is included in the microtransmission to enable additional gear sets to be added in a modular fashion.

With a total of 29 intermeshing gears, the microtransmission can achieve a 3,000,000:1 gear reduction ratio in less than 1 mm^2 of silicon area *(see the figure)*. Its gearing is driven by a five-level micromachine powered by comb drives. Each level provides a small elevation that separates a gear or row of comb teeth so that they can move freely.

The microtransmission is made by etching away a sacrificial oxide layer. Each level enables thicker and stronger comb drives, and allows more gears to overlap each other, thereby compressing the amount of horizontal space needed. Sandia credits the development of the micromachine to its five-level polysilicon technology coupled with the laboratory's sophisticated design and processing knowledge.

Each drive consists of two comb-like structures, with the teeth of one lying between the teeth of the other. During operation, electric signals are alternately sent to the combs causing them to be attracted to each other, first on one side and then, the other. According to the scientists, the combs' motion is transmitted to a piston-like linkage moved by one of the combs. A second comb drive provides power at right angles to the first. The piston it drives, when timed with the force of the first piston, is sufficient to turn a drive wheel on the microengine.

While Sandia hopes to use the discovery to aid ongoing research into near-invisible locks for nuclear weapons, the microtransmission also may be useful for such things as optical telescopes, optical switching for telephone lines, and intercommunication aircraft sensors. The microtransmission also is being eyed for environmentally difficult applications such as satellites, where minimizing the weight of a payload is crucial. Additionally, it could be used in microsurgeries, where doctors often need to apply large forces to very small areas.

Sandia's scientists believe that the microtransmission also may serve to provide insight into basic engineering research and development on micromachines. One area that has baffled researchers is how to deal with frictional effects on such small machines. The problem is that to study these effects, a micromachine is needed that can withstand the application of a significant amount of force. Sandia's microtransmission, they believe, may serve as an ideal test structure from which researchers can determine qualities such as a micromaterial's fracture strength.

The microtransmission may one day provide an accurate measure of displacements on the atomic scale. In fact, as Sandia's scientists point out, a single revolution of the micromachine's drive gear can generate a calculated displacement of the output gear of only 0.8 Å. That's the same unit of measurement typically used to determine spaces between atoms.

To make its microtransmission technology as accessible as possible, Sandia plans to utilize the World Wide Web as a delivery mechanism. Companies and universities wishing to fabricate the device need only download a blueprint for the gears of a basic microtransmission unit. With this information, the user can then design as many intermeshing transmission systems as they need by simply duplicating the basic gear arrangement. This ability to "cut and paste" the gears is possible due to the modular nature of the assembly. And, because it is such a simple, low-cost task to accomplish, unique intermeshing transmission systems can be made using any common CAD program.

For additional information, contact Sandia National Laboratories at (505) 844-8066, or check out their web site at: http://www.sandia.gov. The Sandia Lab News Online Edition, which also contains information on the development, can be accessed at: http://www.sandia.gov/LabNews/LabNews.html.

Cheryl Ajluni

Electrical Process Measurements Boost Accuracy Of Extracted Interconnect Parasitics

The obstacles that arise from design in a deep submicron (DSM) environment of 0.25 µm and below come from the inability of modern electronic design automation (EDA) tools to accurately characterize, model, and extract interconnect parasitics. Hoping to fill in this tool gap, Frequency Technology, San Jose, Calif., has developed a unique technology to accurately characterize interconnect parasitics. Their solution, Verified Interconnect Process Parameters (VIPPs), will enable a design's RC interconnect parasitic information to be extracted and analyzed with an accuracy increase of 30 to 40% over what designers can get today.

The VIPP technology is a way of electrically measuring a process to identify parameters that will affect interconnect performance. In particular, the six parameters that are measured include critical dimension loss, metal thickness, dielectric thickness, sheet ρ, via resistance, and dielectric constants. These parameters are measured for each metal layer in a process, with a single VIPP being established for each parameter. Consequently, if a process has five metal layers, then 30 VIPPs will be needed to provide an electrically accurate physical process model. Once the VIPP's information has been obtained, it can be used as input for physical design tools, as well as place-and-route tools.

Although this sounds easy enough, the trick is in how the company is able to electrically measure the six parameters using proprietary techniques. The goal is to be able to measure a parameter thousands of times across a wafer, and from one wafer to another, to get an accurate picture of how much it varies.

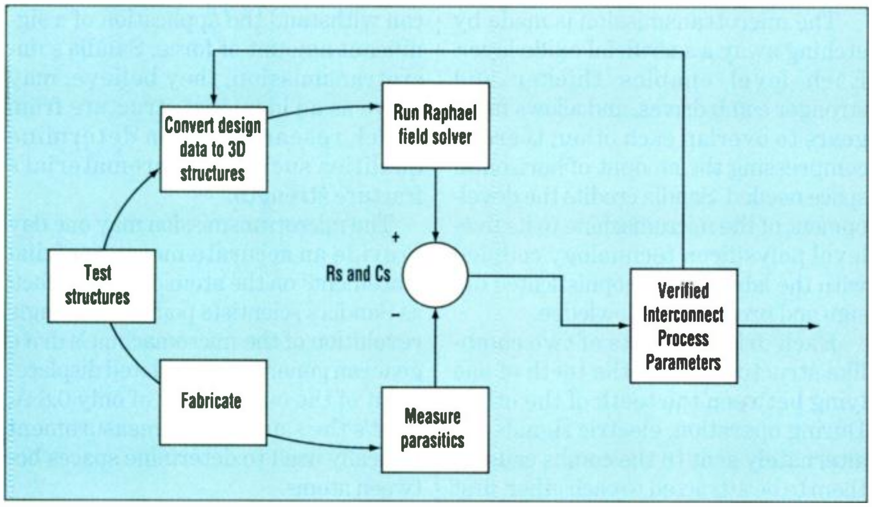
But just cutting up one wafer or many wafers for that matter, and testing them, is not an ideal solution. The real problem is that you can't measure the six parameters physically, so you have to develop a method of electrical measurement. Martin Walker, president and CEO of Frequency Technology, explains it this way: "In much the same way you might cut open a resistor and look at the carbon inside to figure out a value for resistance (R), as opposed to working out the voltage across it to figure out how big the resistance would have to be, electrical measurements must be made to determine the physical parameters of a process. In a way, what we are trying to do is the equivalent of testing, for example, the transistor, with the task of estimating the diameter of R."

To determine the VIPP, design rules for a particular process must first be obtained. This information is crucial to the development of process-specific, device-independent test structures which are used to probe and test wafers *(see the figure)*. With these test structures, hundreds of measurements per die site along with thousands of measurements per wafer can be made. Three-dimensional structures can then be created that are a prediction of what the actual structure would need to look like to, for example, produce the same electrical capacitances as the measured capacitances. Once the 3D structure has been determined, it is a relatively straightforward process to verify that the measured electrical performance and the prediction is the same. As Walker explains, "Because there are fewer variables compared to the enormous number of measurements, it's easy to make sure you have the right answer."

With Frequency's electrically accurate physical interconnect model technology, designers can predict how their actual process will affect their design. The hope is that once designers understand the impact of process on a design, they will be equipped with the assurance that their final design will be reliable and free from errors due to the use of inaccurate tools or information.

For further information, contact Frequency Technology at (408) 938-9300; Internet: http://www.frequency.com.

Cheryl Ajluni



This diagram represents the chain of events that must take place in order to determine a VIPP. The test structures used are basically hunks of metal that allow the electrical measurements of the various parameters to be made. Different structures are needed for each new process.

Laser-Based Technology Offers Time Savings For Parts Manufacturing

With the consumerization of the industry well underway, engineers everywhere are faced with the same problems: How do we get products out quicker, and how do we develop successive product generations in a variety of complex shapes and materials to address many different markets? Sandia National Laboratories, Albuquerque, New Mexico, thinks it may have a solution in LENS.

LENS (Laser-Engineered Net Shaping) is a manufacturing technology that uses computer-controlled lasers to weld air-blown streams of metallic powders into custom parts and manufacturing molds. Because the final product can produce a geometrically complex shape that is very close to the final product, the need to rough-machine the part is eliminated from the fabrication process. This equates to a substantial time savings in manufacturing—up to as much as a few weeks.

The technology, which was originally developed at Sandia for use in low-volume production of highly specialized nuclear weapons components, is now being seen as the predecessor to more conventional fabrication techniques such as rapid prototyping and rapid manufacturing. These techniques are used to help speed the process of idea conception to new product. But, they often require more time because they work by using lasers to heat plastics into liquid, and then form prototypes from the plastic.

By comparison, LENS uses nozzles to direct a stream of metal powder, that can be made up of a variety of different materials, at a central point. At the same time, that point is heated by a high-powered laser beam. Both the laser and jets remain stationary while the model and its substrate are moved, providing new targets on which to deposit metal. Layers are deposited sequentially—first on a substrate, and then on the built-up layers—until the desired cross-sectional geometry is completed with the production of a three-dimensional metal product.

The result of this process is that small quantities of high-density parts or molds can be easily fabricated. Traditionally, this has been a process often made more difficult because in high temperatures it's harder to form accurate, smooth objects from molten metals. Using LENS, the materials that are produced exhibit very-high-strength and high-ductility mechanical properties.

While researchers are still trying to work out problems with the technology, such as improving its dimensional accuracy, and achieving a better metal finish, it is now the focus of a $3-million, two-year Cooperative Research and Development Agreement (CRADA) aimed at commercialization. For more information, contact Sandia at (505) 844-8066, or http://www.sandia.gov.

Cheryl Ajluni

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DS1705/6 DS1706x	5V - 5% or 10% 3.3V - 5%, 10% or 20%	✓	or	✓	✓	✓	✓	8-pin DIP 8-pin SOIC
DS1707/8 DS1708x	5V - 5% or 10% 3.3V - 5%, 10% or 20%	✓		✓	✓		✓	8-pin DIP 8-pin SOIC
DS1810-13 DS1815-18	5V - 5%, 10% or 15% 3.3V - 10% or 20%	✓	or	✓	✓*			SOT-23 TO-92
DS1832	3.3V - 10% or 20%	✓		✓	✓	✓		8-pin DIP 8-pin SOIC
DS1834	5V - 5% or 10% and 3.3V - 5%, 10% or 20%	✓	&	✓	✓			8-pin DIP 8-pin SOIC

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Frank Goodenough

COVER FEATURE

Some 22 years ago, Siliconix (now Temic Semiconductor) announced its VMOS process, a process that produced DMOS power transistors with low on-resistance. Who would have thought then that die on-resistance for vertical-DMOS power-MOSFETs, would someday drop below package resistance (the leadframe resistance)? But that's exactly what Fairchild Semiconductor, Santa Clara, Calif. has accomplished. The company has developed an open-cell trench structure for MOSFETs that combines the advantages of a trench process, which offers the lowest drain-source on-resistance ($R_{DS(ON)}$), with those of a planar process, which offers relatively low $R_{DS(ON)}$ at an even lower cost *(Fig 1)*.

Until recently, power MOSFETs used a cellular design in which the number of cells per square inch of silicon (cell density) determined device on-resistance, which in turn, was a result of the channel resistance. The greater the cell density, the lower the on-resistance. A clamp diode is also used to protect the cell from avalanche damage. This clamp-diode design means that drain-source breakdown voltage is limited by the clamp diode, not the cell structure. This is not good for $R_{DS(ON)}$. In addition, as cell density increases, on-resistance approaches a brick wall as the resistance of the JFET region takes over. To overcome this limitation, several organizations have etched a trench from the FET's channel to the expitaxial region.

The initial approach—and to date the only approach—by most companies in the low-voltage power-MOS arena has been to move to a noncellular planar-strip structure which achieves similar or lower on-resistance than the more complex trench approach.

Not A Panacea

When looking at the total picture of where MOSFETs are used in power-supply designs, it becomes clear that $R_{DS(ON)}$ is not a panacea. Low specific $R_{DS(ON)}$ is generally achieved at the expense of a higher gate charge, which usually means lower dc-dc conversion efficiency.

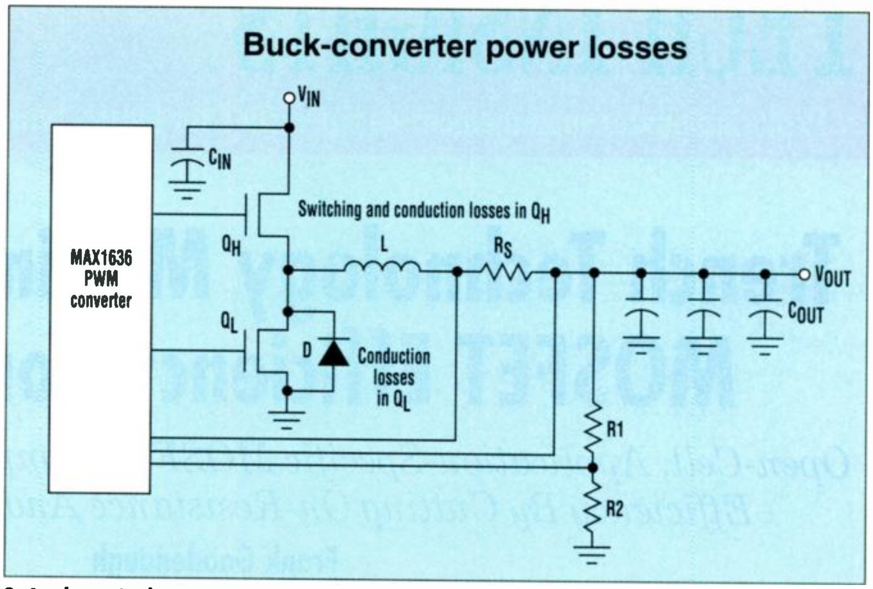
Power-device requirements have changed. In an era of increasingly smaller laptop and palmtop computers as well as personal digital assistants (PDAs), power efficiency is becoming more crucial as computer manufacturers try to make every last watt of precious battery power count.

The challenge to improve efficiency has increased as Intel Corp. and other makers of modern microprocessors have lowered their core operating voltage from 5 V to 1.8 V for next-generation CPUs. It looks as though the next digital subsystem will soon follow with bus voltages decreasing from 3.3 V to 1.5 V. This effort has dramatically saved power in the CPU core, and will save power in the rest of the digital subsystem in the future, which should help battery operating time in laptop computers. The result of this lowering of the voltage has forced power-supply designers to look again at the efficiency of dc-dc converters. That efficiency has dropped from the mid 90s, when the output was 5 V, down to the high 70s, thus offsetting some of the power savings.

Intel recently hosted a Mobile Power Symposium in San Francisco, Calif., to talk about the entire mobile power requirements, including dc-dc converter efficiency problems with low-voltage outputs. Discussions at this conference centered around the reduced efficiency, the reasons for this effect, and what can be done to regain some of the lost ground.

Increased switching losses of the high-side MOSFETs are partly to blame. As the input voltages have increased with the new lithium-ion batteries, and the output voltages have decreased, the switching losses have become a higher percentage of the total losses. The high-side switch operates at a low duty cycle so that conduction losses are less important than for the low-side switch *(Fig. 2)*. To reduce these losses specifically on the high-side MOSFET, Fairchild Semiconductor has developed a new silicon structure for MOSFETs called PowerTrench. These new MOSFETs improve switching speeds and total gate charge while maintaining $R_{DS(ON)}$.

In past designs, the same MOSFET was used everywhere, and in some cases the optimum circuit wound up using a relatively high resistance, which may be fine for fast-switching MOSFETs on the high-side switch. But the low-side switch should employ MOSFETs with a lower $R_{DS(ON)}$ for optimum efficiency.

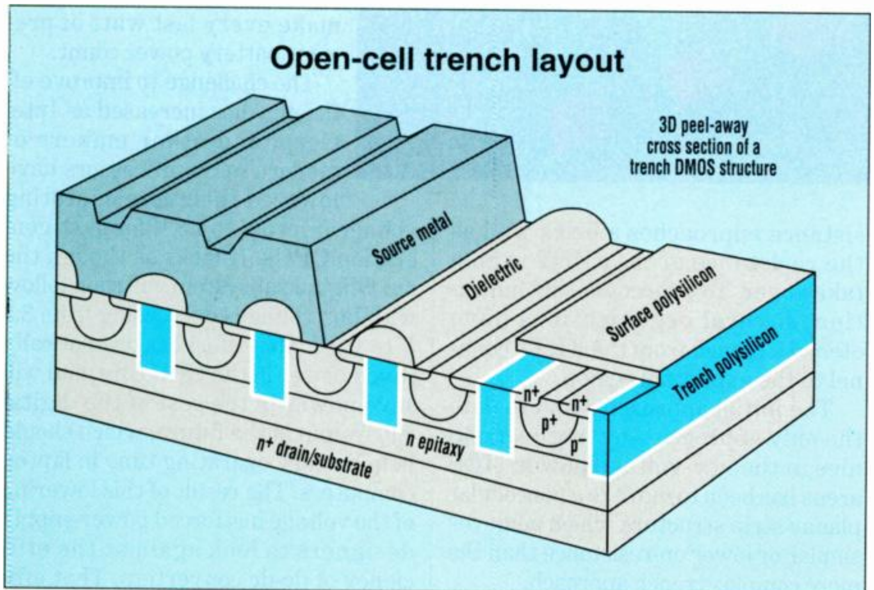


2. As shown in this MAX1636 PWM controller circuit from Maxim Integrated Products, increased switching losses on the high-side MOSFET Q_H have become a higher percentage of the total switching losses. Because Q_H operates at a low duty cycle, conduction losses for Q_H are less important than for low-side switch-MOSFET Q_L.

To lower the drain-source on-resistance, Fairchild uses an open-cell approach with trench strips. Unlike closed-cell designs with hemispherical junction features that produce higher electric fields, Fairchild's open-cell approach with its cylindrical structures reduces the electric field. The result is a higher breakdown voltage rating for a given silicon doping concentration *(Fig. 3)*.

It also cuts down on the amount of gate charge. A lower specific $R_{DS(ON)}$ is achieved by increasing the doping concentration in the epitaxial region. The clamping diode is not mandatory to handle electric fields at the trench bottom corner. Instead, each cell is structured to direct damaging avalanche current away from the sensitive gate oxide. In effect, Fairchild has developed an application-specific FET combining low on-resistance (which reduces conduction losses) with low gate charge (which cuts switching losses). The $R_{DS(ON)}$ rating for Fairchild's new MOSFETs is the same as that for the venerable Temic Si4420DY device, but with 40% less gate charge.

Fairchild's designers believe that the open-cell-trench approach is superior to a closed-cell method. They believe it is more rugged, and provides better yields (thus lower costs) and superior gate charge.



1. The figure shows a 3D peel-away cross-sectional view of Fairchild Semiconductor's trench-DMOS process for power MOSFETs. The process combines the low-cost advantages of a planar process with the low on-resistance advantages of a trench process. The result is power MOSFETs optimized for high dc-dc conversion efficiency.

High-Efficiency MOSFETs

Fairchild's new technology makes possible n-channel MOSFETs in two types of packages: the SO-8 and the SuperSOT. Available in the SO-8 package will be the FDS6670A which offers an on-resistance of just 8 mΩ (at a gate-source voltage V_{GS} of 10 V) combined with a gate charge of less

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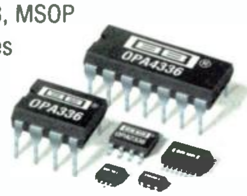

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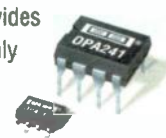

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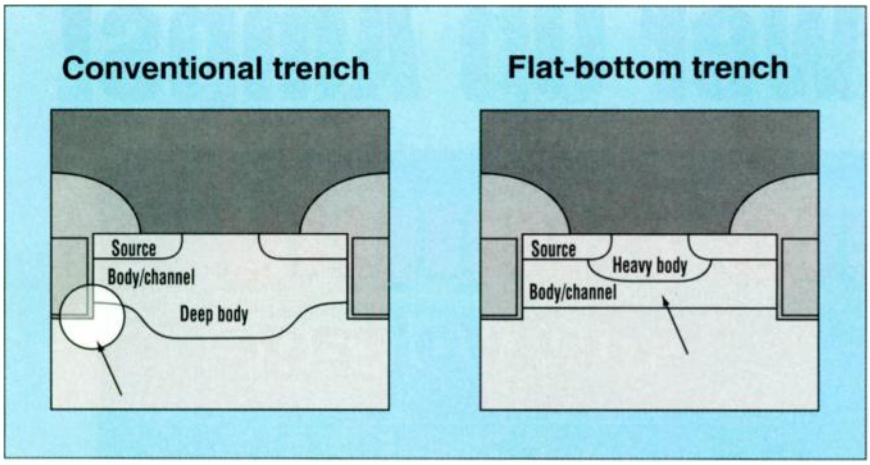

3. Unlike conventional trench processes which use a deep-body area to reduce electric-field-caused breakdown (left), Fairchild Semiconductor uses an abrupt, shallow heavy-body area (right).

then 62 nC and a drain current rating of 12.5 A. At V_{GS} of 4.5 V, on-resistance is 12 mΩ.

An even lower gate charge of just 42 nC is available in the same package as the FDS6680A, with an on-resistance of 9.5 mΩ at V_{GS} of 10 V (on-resistance is 14 mΩ at V_{GS} of 4.5 V). Drain current rating is 13 A. Both the FDS6670A and 6680A are rated at drain-source voltage V_{DS} of 30 V and dissipate 2.5 W.

What these numbers mean is that on average, a device like the FDS6680A ranges in efficiency from 88% (at 3.3 V) for output current of about 100 mA to 92.5% (at 3.3 V) for output current of 1.5 A. By comparison, efficiency for other popular industry MOSFETs ranges from a low of about 78% to 82%, to about 89% to 91% for the same conditions.

For those who need an even smaller footprint package (40% smaller), there's the SuperSOT n-channel device. It makes possible fitting the die in Fairchild's proprietary SuperSOT package which has a 40% smaller footprint then the industry standard SO-8. The FDR4420A-8 is a 30-V MOSFET with on-resistance of 9.5 mΩ (at V_{GS} of 10 V) and 15 mΩ (at V_{GS} of 4.5 V). Lower on-resistances of 25 mΩ are available in -6 versions, and 40 mΩ in -3 versions.

Price And Availability

The FDS6670A and FDS6680A single MOSFETs in SO-8 packages are available now at $2.45 and $1.75 each, respectively, in quantities of 1000. The single FDR4420A MOSFET in an 8-pin SuperSOT package is also available now at a price of $1.47 each in similar quantities.

Fairchild Semiconductor, 1322 Crossman Ave., Sunnyvale, CA 94089; Dave Schoenwald (408) 822-2000;. e-mail: www.fairchildsemi.com. **CIRCLE 490**

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OPA237	Low Power, Single Supply	S,D,Q	2.7 to 36	170	$0.81	11327	88
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Capacitive Sensors Offer Numerous Advantages

Don't Believe The Myths About The Problems With Capacitive Sensors And How Hard They Are To Use—They Do A Good Job In Many Applications.

LARRY K. BAXTER, 73 Eastern Point Blvd., Gloucester, MA 01930; (978) 623-4254; baxterl@pictel.com.

This article is based on material from the author's recently published book, Capacitive Sensors, *IEEE Press, Piscataway, N.J., 1997.*

Compared with competing optical, inductive, and piezoresistive transducers, capacitive sensors have many advantages, among them low cost and power usage, and good stability, resolution, and speed. They also have a near-zero temperature coefficient, can be optically transparent, and are easy to integrate into ICs or onto printed-circuit boards (pc boards). Capacitive sensors can detect motion, acceleration, flow, and many other variables, and are used in a wide range of applications.

But many engineers still distrust the technology. Some believe that capacitive sensors are affected by temperature and humidity, sensitivity to noise, difficulties in designing, instability, and nonlinearity. Capacitive sensors do need some specialized design know-how to avoid those hazards. Some sample designs and applications should help dispel this distrust.

Capacitive sensors come in one of three types. Fixed-plate versions maintain the relative position of the two plates, while the capacitive coupling changes as a result of different materials placed near the plates. A grounded conductive material will reduce coupling capacitance, and a high-dielectric material will raise it. These sensors are used for sensing wall studs or determining the composition of materials. An array of multiple fixed plates can form an x-y touch sensor to measure finger or stylus position in two dimensions or even to image fingerprints.

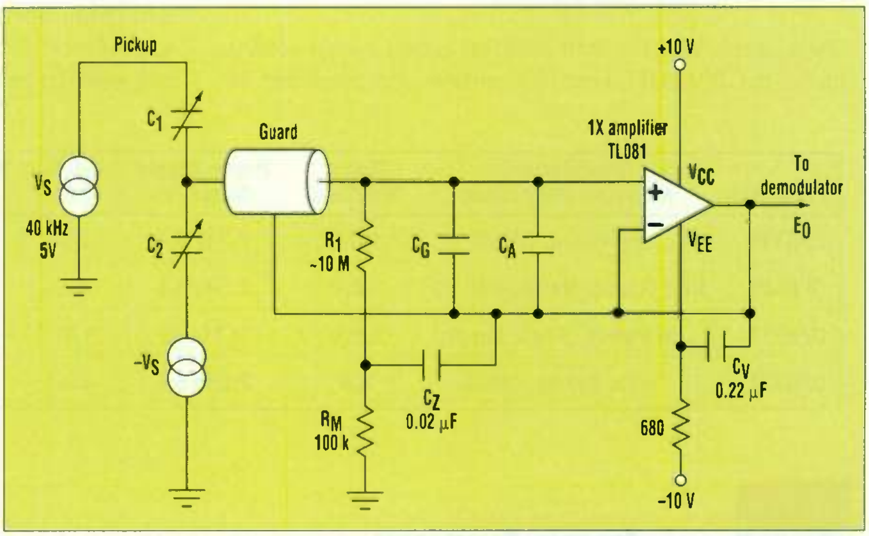
Another technique involves changing the spacing between the capacitor's parallel plates. This geometry's ability to accurately measure small motions down to 10^{-14} m makes it useful in electret microphones, tiltmeters, seismometers, and micrometers. Adding a third plate to sandwich the moving plate between two fixed plates, and driving the fixed plates while sensing the moving plate, increases the signal and provides shielding. This arrangement does not handle large motions well since capacitance drops to a difficult-to-measure value with large plate spacing.

The third type, which involves moving the parallel plates so their overlap area changes, can measure greater linear motions. Adding a second fixed plate above the moving plate again improves performance, as first-order spacing dependence is nulled out. To improve accuracy, multiple plate patterns are used, with a demodulator counting plates for a coarse position determination and interpolating between plates for a fine measurement, similar to optical encoders.

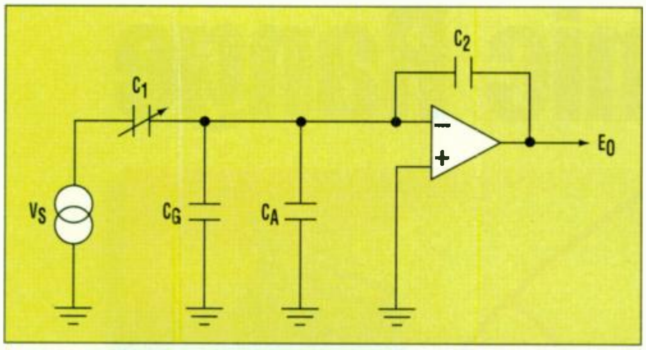
Ratiometric position sensing is better still. In this technique, the moving plate, C, is on one side of two fixed plates, A and B. The device measures the ratio of the capacitances C_{CA} and C_{CB}. This device is not sensitive to spacing. Adding two more fixed plates A' and B' on the other side of the moving plate, and then connecting A' to A and B' to B, makes the unit self-shielding and first-order insensitive to tilt.

Demodulation Methods

Several techniques are available to convert the capacitance or capacitance ratio to a voltage output. In the direct method, the plates are charged with a dc voltage and feed a very-high-impedance amplifier. This scheme is inexpensive and has good high-frequency response. But it doesn't work at dc unless the amplifier's impedance is infinite, and it is noisy because semiconductors



1. This typical unity gain follower amplifier configuration for ratiometric position sensing produces a linear output with area-variation motion. The two variable capacitors C_1 and C_2 represent ratiometric capacitances C_{CA} and C_{CB} discussed in the text.



2. A virtual-ground amplifier keeps the signal at virtual ground, placing shields at ground potential. The amplifier's common-mode input is not a problem and power rails do not need bootstrapping.

are noisy at low frequencies.

Another method uses the sense plates to create the C in an RC oscillator, and then measures the oscillator's output frequency or period. The result is a simple, low-noise demodulator that rejects low-frequency noise. But if stray capacitance is not nulled, it may swamp the sensor's capacitance, causing a low-amplitude and unstable output.

In a synchronous demodulator, the sensor plates are driven by a square- or sine-wave signal at, for example, 5 V and 100 kHz, rather than a dc signal. Some systems use two square waves at 0°and 180° phases, and a phase-sensitive demodulator. In these systems, the sensor is usually configured for ratiometric measurements for improved stability and precision. The ratiometric synchronous demodulator is the most accurate circuit, but it has the highest part count.

Practical Circuits

In a practical system, the capacitance to be sensed usually ranges from 0.01 pF for ICs to 2-3 pF for a pc board of a square centimeter. Impedance ranges from 1.59 MΩ at 100 kHz with a 1-pF sensor to 1590 MΩ at 10 kHz with a 0.01-pF sensor. The amplifier's input impedance should be much larger than the sensor's to avoid shunting the signal, and since typical operational amplifiers have input capacitances of a few picofarads, special low-capacitance amplifiers are needed. These amplifiers can be used with any of the three types of demodulators.

At these extremely high impedances, system noise is usually dominated by amplifier current noise rather than voltage noise. Amplifier voltage noise is generally restricted to a relatively narrow range, between 3 nV/√Hz and 60 nV/√Hz. But current noise is much more variable, with extremes of 0.2 fA/√Hz to 50 pA/√Hz.

The capacitive pickup amplifier will probably need a FET input stage, either a JFET or MOSFET, to get acceptably low current noise. MOSFET current noise is in the range of 0.2 fA-1 fA/√Hz and will not contribute to output noise with reasonably high sensor plate capacitances (0.5 pF) and excitation frequencies (100 kHz). JFETs are almost as good, 2 to 40 fA/√Hz, and usually have lower voltage noise and are less sensitive to electrostatic discharge. Bipolar transistor current noise can be over 50 pA/√Hz. With a sensor impedance of 100 MΩ and a bandwidth of 10 kHz, this level of current noise will produce over 100 mV rms of input-referred noise.

Designers have three circuit choices for the input amplifier: follower amplifier, virtual-ground amplifier, and all-over feedback amplifier. Their noise performance is similar, but each circuit offers different options for shielding and handling stray capacitance, and each has different amplifier common-mode requirements.

The typical unity-gain follower amplifier uses the ratiometric sensor configuration, with C_1 and C_2 representing C_{CA} and C_{CB} *(Fig. 1)*. The circuit has an in-band ratiometric response of:

$$E_o = V_s\left[\frac{C_1 - C_2}{C_1 + C_2}\right]$$

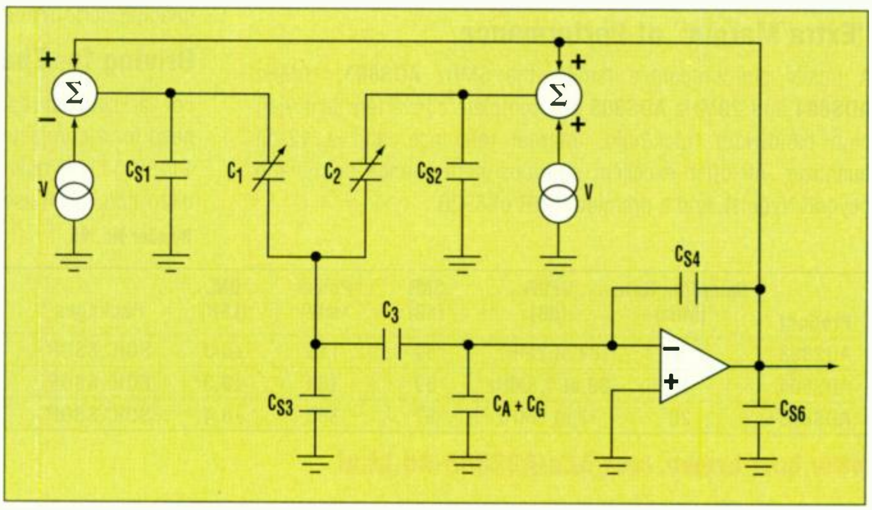
and it will produce a linear output with area-variation motion.

The response is independent of stray capacitances C_A, the amplifier's internal input capacitance, and C_G, the stray capacitance to ground. The former is bootstrapped out because the negative input follows the positive input exactly, and the latter is nulled by using a driven guard shield. The shield follows the input signal exactly so if the shield completely surrounds the input node no current can flow from the input through stray capacitance to ground.

Handling Stray Capacitance

Stray on-chip capacitance from the positive amplifier input to the substrate often can be handled by bootstrapping the negative power supply through C_V, but not all amplifier types are stable with this connection. Bootstrapping the positive power supply input doesn't work for most IC op amps, but positive supply bootstrap can be used for properly designed discrete amplifiers.

To set the amplifier's bias point, the designer can use an input resistor to ground. It must be large enough for



3. The advantages of both follower and virtual-ground amplifiers are combined in an all-over feedback amplifier. These include a grounded shield, a ratiometric (instead of an absolute) output, no common-mode range problems, and good stray capacitance compensation.

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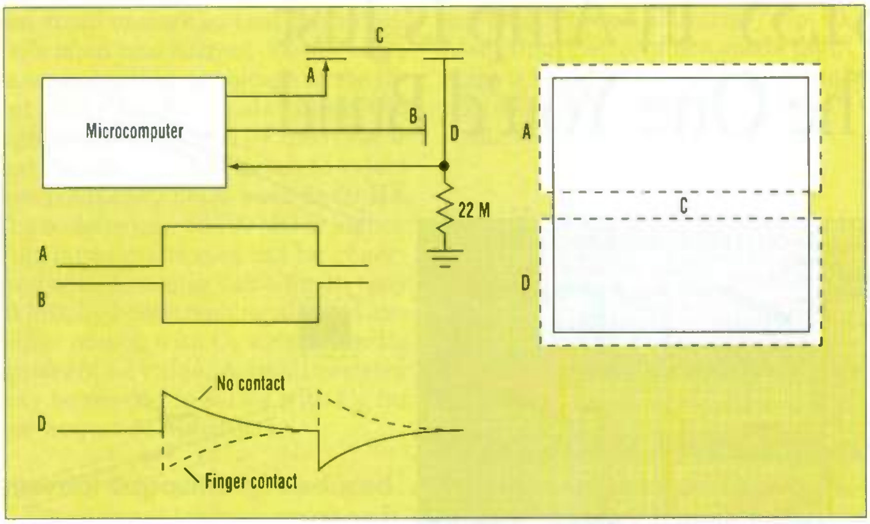
TECH INSIGHTS CAPACITIVE SENSORS



5. A good example of a capacitive-sensing application is a very simple finger-touch switch. Very few components are required to build the switch..

sion A is small. However, x-axis tilt is a problem. The preferred arrangement is a chevron pattern, which also compensates for first-order x-axis tilt *(Fig. 4c)*. If the pickup can be surrounded by driver plates, all tilt and spacing dependencies are reduced, shielding is improved, and the signal is larger.

Another problem is triboelectric charge. This electrostatic charge caused by friction can confuse capacitive sensors in two ways. First, the amplifier's very high input impedance means that even a tiny spark discharge can create a transient output that can be misinterpreted as a sudden large-amplitude input excursion.

In addition, if a sensor plate picks up an electrostatic charge, any mechanical spacing change due to vibration will be converted to an output voltage according to V=Q/C, where Q is the total electrostatic charge on the plates (unchanged by vibration) and C is the sensor capacitance, which changes inversely with spacing. This vibration-induced voltage can be very large, saturating the amplifier. Or if the vibration's frequency spectrum is close to the carrier frequency, the vibration will add to the output signal. The solution to this vibration sensitivity is to eliminate insulators from the region of the sensor plate gap, increase mechanical rigidity, and increase the carrier frequency.

Nanoampere leakage currents also cause problems. They degrade capacitive sensors by adding noise or by upsetting amplifier bias. The worst offender, surface pc-board conduction paths, can be handled effectively by adding ground (or driven-shield) etch paths around the amplifier input. For instance, the input node of the virtual-ground amplifier can be surrounded by a ground implemented as a printed circuit board trace surrounding the sensitive components and connected to ground. Solder mask should be relieved on top of this trace.

Discrete components also can produce leakage currents. Surface-mount MOSFETs all have an integral protection diode that degrades performance by adding current noise, so either diodeless through-hole MOSFETs (protected by a removable wire ring) or JFETs (no diode needed) are preferred. Electrolytic and high-value ceramic capacitors also are noisy and leaky; film or mica types should be used.

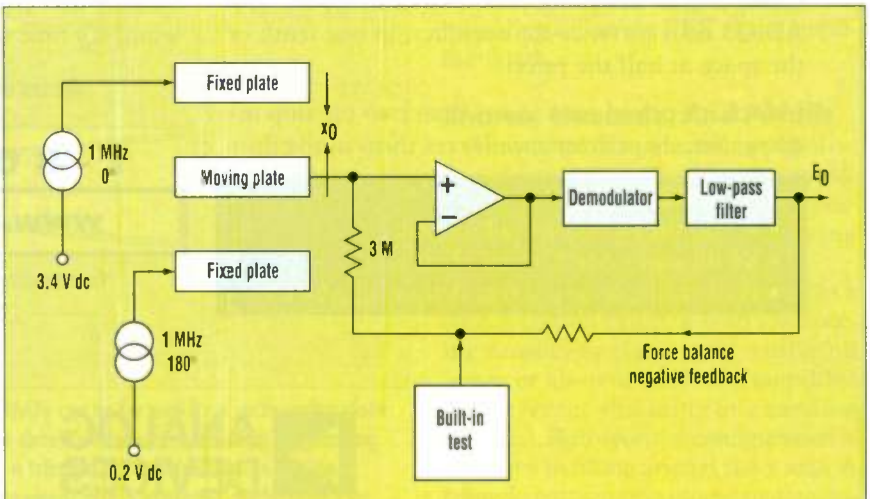
Sensor Applications

A good example of a capacitive-sensor application is a very simple finger-touch keyswitch with a low component count *(Fig. 5)*. A microcomputer generates a short positive pulse at plate A and a short negative pulse at plate B. With no finger present, the positive pulse couples through floating plate C to plate D, producing a positive transient at C, which is read by the computer. If a finger touches C, the positive signal path is interrupted, and enough of the negative pulse couples to D to produce a negative output.

The plates can be built on the product's pc board. If the microcomputer has a comparator or analog-to-digital converter (ADC) input, the circuit requires only one discrete component.

Capacitive sensors also can increase device integration. For instance, Analog Devices' ADXL50 is a surface-micromachined accelerometer with integrated signal processing, built on a 9 mm^2 chip. It measures acceleration in a bandwidth from dc to 1 kHz with 0.2% linearity, and it outputs a scaled dc voltage. The accelerometer is a force-balance device, using electrostatic force to null the acceleration force on the "proof" mass, with advantages in bandwidth, self test, and linearity.

Early accelerometers measured the displacement of a spring-suspended mass. Problems with this approach in-



6. Closed-loop operation coupled with high amplifier gain can be used to handle small sensor signal electrode capacitance values of just 0.1 pF, as is the case for Analog Devices' ADXL50 micromachined accelerometer IC. If the gain is high, the error caused by gain variations is negligible.

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Like all solid tantalum chip capacitors, the 593D is extremely stable under temperature changes and time. In addition, it has no end-of-life constraints or known wear out mechanisms for excellent reliability and stability.

The 593D features values ranging from 1.5µF to 330µF, and voltages from 6.3 to 50. This product is in an industry standard molded chip package for full compatibility with existing pad layout designs.

For a data sheet, call Vishay's FlashFax℠ Service at 800-487-9437. Document #510.

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Up to .10µF (100V)

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The Highest C-values Available in a Miniature Film Capacitor with 5mm Lead Spacing

Roederstein Electronics, Inc. has expanded its MKP 1840 series of metallized polypropylene film capacitors to include a miniaturized version with the highest C-values available with 5mm lead spacing. Fully auto-insertable, these capacitors allow the design engineer to take advantage of a much reduced printed circuit board footprint while maintaining the superior characteristics of the polypropylene dielectric.

Polypropylene's excellent stability, very low dielectric absorption, high insulation resistance and low dissipation factor make these capacitors ideally suited for use in designs where precision is required, such as audio and instrumentation applications. Most commonly these capacitors are used in oscillators, timing and LC/RC filter circuits, high frequency coupling/decoupling, cross-over networks, and sample and hold circuits.

Roederstein's MKP 1840 capacitors are also self-healing and do not exhibit a piezio-electric effect. The new 5mm lead-space capacitors are available in C-values up to .10µF and in a 100-volt rating. Larger sized capacitors are available in higher voltages and capacitance values up to 10µF. All are encapsulated in flame-retardant cases.

For a data sheet, call Vishay's FlashFax℠ Service at 800-487-9437. Document #707.

8200pF to .22µF (25V & 50V)

VISHAY VITRAMON®

0612 Capacitor Cuts Inductance by More Than Half

Selecting capacitors with low inherent inductance is always an important design consideration–particularly in high speed microprocessor and multi-chip module circuitry. Normally in the 0.8nH to 1.0nH range, this inductance can be cut by more than half with Vitramon's monolithic ceramic chip capacitor.

The Vitramon chip (VJ0612) provides standard inductance levels as low as 0.3nH. The package dimensions are 0.062"L x 0.126"W with thicknesses from 0.020" to 0.038". Standard capacitance range is from 8200pF to 0.22µF with tolerances of ± 5%, ± 10%, ± 20% and voltage ratings of 25V and 50V.

This combination—available in a robust, easily mounted package —makes the VJ0612 ideal for use in new designs where low inductance is important as well as for improving the performance of existing circuitry.

For a data sheet, call Vishay's FlashFax℠ Service at 800-487-9437. Document #50100.

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cluded the presence of a resonant peak, difficulty in achieving good dynamic range, and the need to carefully calibrate the force-vs.-displacement relationship.

Microscopic Movement

The proof mass in a force-balance device deflects only microscopically. The device detects and amplifies this displacement, then feeds back a force to restore the rest position. With a high-gain amplifier, the mass is nearly stationary and the linearity is determined by the linearity and precision of the voltage-to-force transducer rather than the suspension characteristics. Early versions used piezoresistive sensing of the displacement, but problems with temperature coefficient, dc response, and shock-induced zero shift caused a switch to capacitive sensing in most new accelerometers.

The ADXL50 uses a very small (1 mm^2) capacitive sensor element. To increase signal strength, the silicon micromachined electrode design uses 42 moving plates, each 2-µm wide, projecting from a center bar. On either side of each moving plate are fixed plates driven by a 0° and a 180° square wave. The gaps between the fixed and moving plates are 2 µm. The total electrode length is 10 mm, and the mass of the moving plate is 0.1 µg.

The total sensor electrode capacitance, neglecting fringe fields, is about 0.1 pF. This small value would require an extremely low amplifier input capacitance for accurate open-loop sensing, but with closed-loop operation the error contribution due to variations in gain is negligible if the demodulator gain is high *(Fig. 6)*. The open-loop change in capacitance with a 50-g acceleration is 0.01 pF, and the system can resolve a change of 20 aF ($20 \leftrightarrow 10^{-18}$ F), corresponding to a beam displacement of $20 \leftrightarrow 10^{-6}$ µm.

The amplifier is conventional, and the demodulator is a standard synchronous demodulator implemented in bipolar technology.

With a moving-plate dc bias level of 1.8 V, midway between the two fixed-plate dc levels, the electrostatic force on this plate is balanced. As the plate's mass is deflected by acceleration, E_0 provides a restoring voltage. The electrostatic restoring force is developed by changing the dc level on the moving plate through the 3-MΩ load resistor.

An older application of capacitive sensing is a computer graphic input tablet manufactured by Shintron Co., Concord, Mass. The tablet was developed in 1967, but the principles of its operation are still used today. It measured the x, y, and z movements of a small, capacitively coupled pickup stylus relative to a square-wave-driven resistive sheet that generated an electrostatic field over the 11-in. square tablet. Two different methods of producing the orthogonal field lines were investigated, and a phase-locked-loop demodulator was used with ratiometric response. Performance was good at large stylus-to-tablet separations.

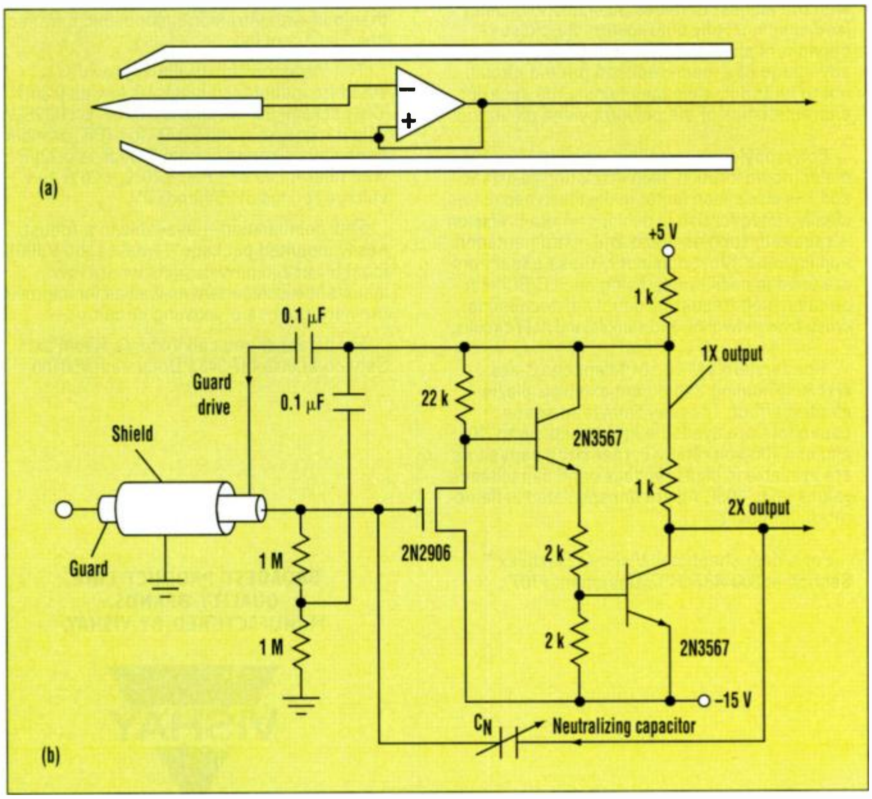
The tablet had a 1024-by-1024 resolution, 1% accuracy, and a sample rate of 100 x-y samples/s. The output format was 10-bit parallel digital, and maximum paper thickness was 0.5 in.

Driving a resistive sheet to measure a single axis is simple. If metallic electrodes A and B are placed along opposite sides of the sheet and fed with a 5-V square wave, the sheet will generate a linear ac voltage field just over its surface. A stylus using a small electrode will pick up a signal proportional to the y displacement when moved near the surface of the sheet. A circuit that measures signal amplitude can also measure the z position.

Two-Dimensional Complications

A two-dimensional system is more complicated. If metallic electrodes C and D are added to the remaining two sides, electrodes A and B will be shorted at the corners, or at minimum a very nonlinear field will be produced. One alternative is to drive the corners instead of the sheet's edges, and to use a medium-resistivity material on on the edges and a high-resistivity material for the sheet to produce an orthogonal, linear field.

To measure position in the y axis on this resistive tablet, electrodes A and B are connected together and driven with 100-kHz, 0° signal and electrodes C and D are connected together and driven with 100-kHz, 90° signal. As the stylus is moved in the y axis, the electrical angle will change from 0° to 90°, but displacement in x will not affect



7. The stylus pickup in a computer graphic input tablet uses a guarded coaxial construction with a 2-mm point exposed for writing and sensing (a). Discrete transistors and guarding and neutralization techniques are used for the pickup circuitry to minimize input capacitance.

the signal. The x-axis position is determined by driving electrodes A and D together and B and C together. Changes in z will change amplitude, but not phase.

Excluding small fringe effects, the field produced by this tablet will be linear and orthogonal if the ratio of the resistives is large. In practice, a large resistivity ratio may be difficult to obtain and a geometric compensation, a slight pincushion shape, will be needed to correct the nonlinearity caused by a low ratio. A linearity correction table can handle a large nonlinearity. The low-resistance strips can be dispensed with, for example, and the resulting over-50% nonlinearity measured and stored.

The stylus pickup used a guarded, coaxial construction with a 2-mm point exposed for writing and sensing *(Fig. 7a)*. It performed well up to 10 cm stylus-to-tablet spacing, at which distance its capacitance to the resistive sheet was less than 0.05 pF, and the signal amplitude was reduced to 10% of the amplitude at the surface due to fringe effects and unguarded stray capacitance. To achieve this performance, the amplifier's input capacitance had to be less than 0.1 pF, a level that attenuated the signal by 3X. The use of ratiometric position detection made this unimportant.

The pickup circuitry used discrete transistors and both guarding and neutralization techniques to minimize input capacitance *(Fig. 7b)*. The guard in the follower circuit did most of the input-capacitance cancellation. A small amount remained due to the finite amplifier gain and the FET's gate-to-drain capacitance. The adjustable neutralizing capacitor, with a value of 0 to 0.1 pF, nulled this residue. Parasitic capacitance is reasonably repetitive and stable, so the neutralizing adjustment is not sensitive to environmental factors once adjusted.

Larry Baxter is a consulting engineer at PictureTel Inc., Andover, Mass. He specializes in the design of electromechanical and electro-optic, analog, and video circuits. He received his BSEE degree from Rensselaer Polytechnic Institute, Troy, N.Y. He has been a founding partner at several companies, including ECHOlab Inc., Kronos Inc., and Everygame Inc.

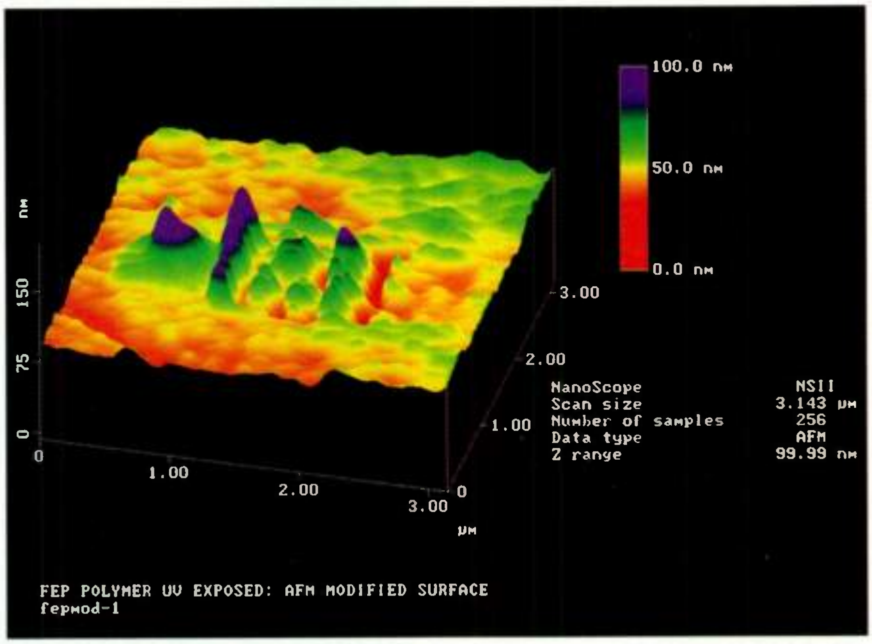
UPDATE ON MEMS TECHNOLOGY

Caltech's Jet Propulsion Laboratory Calls For A Sharing Of Failure-Mechanism Data Via A MEMS Assurance Consortium

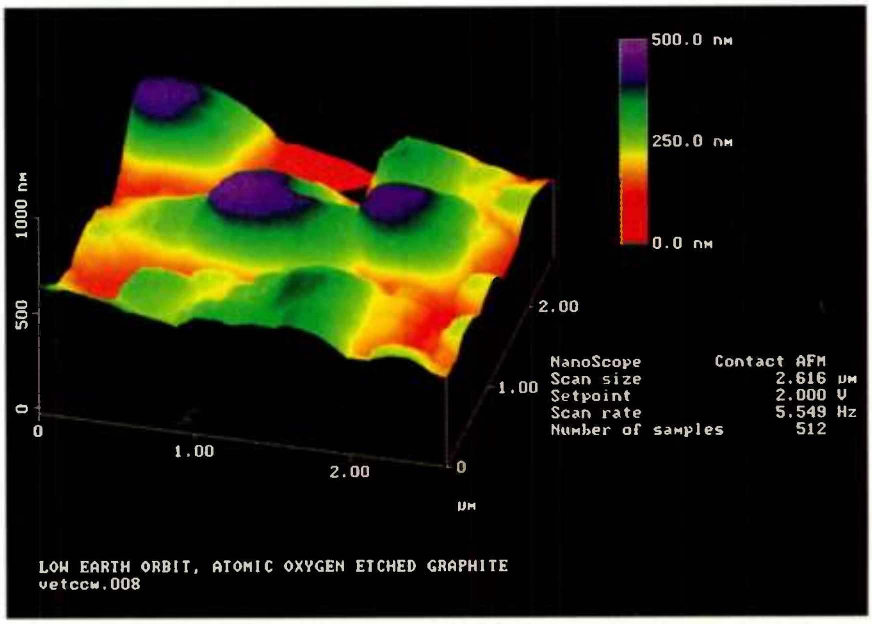
Three years ago, the Jet Propulsion Laboratory (JPL) of the California Institute of Technology (Caltech) formed a consortium of manufacturers and users of ball-grid array (BGA) packages. Its purpose was to study reliability and producibility problems associated with what was then an unproven high-density packaging technology. The failure-analysis results of that consortium's work proved to be far more impressive and useful for both the BGA industry and JPL. Inspired by this successful program, JPL has now decided to create a similar program that will address the MEMS technology sector on manufacturing issues, including reliability, packaging, testing, and failure-mode analysis.

"Our intent in creating this MEMS Product Assurance Consortium is to make available to the U.S. MEMS industry an opportunity to share our collective talents and resources, and to accelerate the growth of MEMs as commercial devices," explains Frank Hartley, senior technical staff member for Advanced Test and Measurement at JPL. "This is really a win-win situation," he adds. The program is free to consortium members. All they need to do is provide JPL with MEMS devices for evaluation, and actively participate in workshops where they can share ideas and knowledge with fellow consortium members.

For JPL whose business is the design, development, and manufacture of small-volume, ultra-reliable spacecraft, the benefits include reliability information gleaned from large-scale production lots. For industry members of the consortium, the benefits include reliability information resulting from the testing of MEMS devices under the extremes of space environments. This testing is performed by a JPL cadre with technical expertise and equipment unmatched, and sometimes unavailable in industry. One or two failures in hundreds of thousands of devices may be acceptable to industry for commercial uses, but for JPL, even one failure in a million devices is unacceptable when multimillion dollar



1. An atomic-force microscope (AFM) is an instrument that can not only image a material with angstrom-level resolution, it also can manipulate the material's surface. This image shows the AFM-manipulated surface of an FEP polymer that was exposed to UV radiation. The image's surface has a lower molecular-weight layer that was moved with the AFM, allowing the depth of the contamination layer to be measured. The instrument can provide valuable insights into a material's behavior when studying reliability issues.



2. The figure shows an AFM scan of a graphite crystal that was eroded in low-earth orbit by atomic oxygen. The sample was carried aboard the Atlantis Space Shuttle (NASA mission STS46). Atomic oxygen is the last trace of atmosphere that, when impinged at orbital velocities, can damage hardware. The AFM measured the surface roughness and morphology, giving insight to the erosion mechanism.

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FDC633N	FDC634P	35	70	SuperSOT™-6
FDR4410	FDR836P	11	25	SuperSOT™-8
NDS8410A	NDS8435A	10	21	SO-8
NDT455N	NDT456P	13	26	Power SOT
NDM3000*		70	125	SO-16

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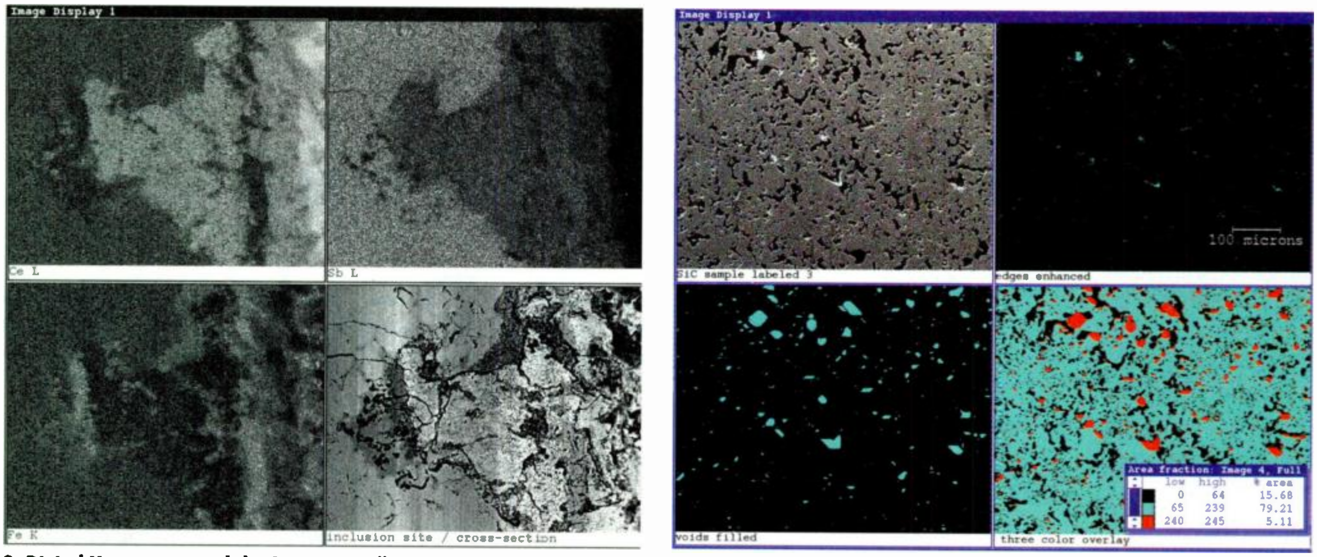


3. Digital X-ray maps and the SEM image illustrate numerous areas of differing stoiciometric composition which are present at the imaged inclusion site (left). A composite backscatter and secondary electron SEM image shows voids and inclusions in a single-phase bulk matrix. Image processing was used to generate a void image which was then overlaid on a binary image of the original micrograph (right). Area fractions of the three components could then be quickly measured.

spacecraft and probes are involved.

In response to the call for a MEMS consortium, leading industry MEMS companies have welcomed this proposal. These companies include Motorola, EG&G IC Sensors, Maxim Integrated Products, Honeywell, Analog Devices, Ford Motor Co., Delco, Texas Instruments, Silicon Systems, and Medtronics to name a few. Some companies initially expressed reservations about sharing their proprietary information or commercially sensitive issues with their competitors. However, JPL is working on an arrangement to satisfy such concerns, by not identifying product model numbers and manufacturers, and using generic classification of test results instead. In addition, for those companies with a desire to keep the test results of their products a secret, there's JPL's Technology Affiliates Program (TAP). TAP is an impartial, commercially noncompetitive, and confidential environment that provides the same JPL testing and analysis personnel and facilities.

Interest in tackling test and reliability issues for MEMS has been growing. Last August, JPL sponsored and hosted the first MEMS Reliability Workshop. It was attended by over 50 professionals who shared their common interest in gaining knowledge about poorly understood areas of reliability, testing, packaging and failure-analysis.

Spacecraft designed and built by JPL must endure the most arduous environments—environments that few, if any, commercially available MEMS devices ever face. These include temperatures ranging from absolute zero to 2000°C at atmospheric reentry, hundreds of thousands of gs in acceleration forces, and acoustic noise greater than 150 dB. They also include wide variations in pressure levels, high-energy cosmic-radiation bombardment, and no outgassing (no depositions on cold surfaces). Testing under such extreme environments is performed using space simulators and force-feedback vibration.

According to Steve Bolin, group supervisor for Quality Assurance Applications at JPL, "We have a wide array of measurement capabilities and expertise that could test for just about any conceivable failure mechanism or mode." Tests include Fourier-transform infrared, mass, atomic force, scanning tunneling, atomic spectroscopy, thermal analysis, ion and gas chromatography, and electron spin-resonance spectroscopy. JPL's analytical chemistry laboratory is capable of performing a wide range of tests spanning radiation testing, X-ray imaging, and propellant analysis.

An atomic-force microscope, for example, can be used to not only image a material, but to manipulate the material's surface *(Fig. 1)*. It can provide insights into erosion mechanisms in deep space *(Fig. 2)*. JPL's materials testing and contamination-control laboratory researchers have used a scanning electron microscope to produce digital X-ray maps of a material showing the differing stoichiomnetric compositions of the material. Voids and inclusions have also been shown *(Fig. 3)*.

Sometimes unique failure modes are discovered under the harsh test conditions that would normally not be discovered using conventional testing environments. Such was the case for the CCD imager used on the Hubble space telescope, when neutralizing electrostatic grids said to be used in a Class 100 environment, to attract micron-sized charge particles, were found sticking to the surface of the device.

For JPL, MEMS technology is crucial. It fits in with their mandate to make spacecraft smaller, lighter and more efficient. A typical space craft or probe uses a number of hardware valves, many of which often malfunction in space. Presently, there's a lot of R&D for using silicon MEMS to make more reliable valves. MEMS accelerometers and pressure sensors will also be widely used in space probes.

As this story went to press, the inaugural meeting of the MEMS Product Assurance Consortium was taking place at JPL, Dec. 18-19. For more information, contact JPL's Frank Hartley at (818) 354-3139.

Roger Allan

Design Conference Becomes Launch Pad For Portable Components

The Latest Products And Technologies Boasting Small Size And Reduced Power Are Unveiled At Portable By Design.

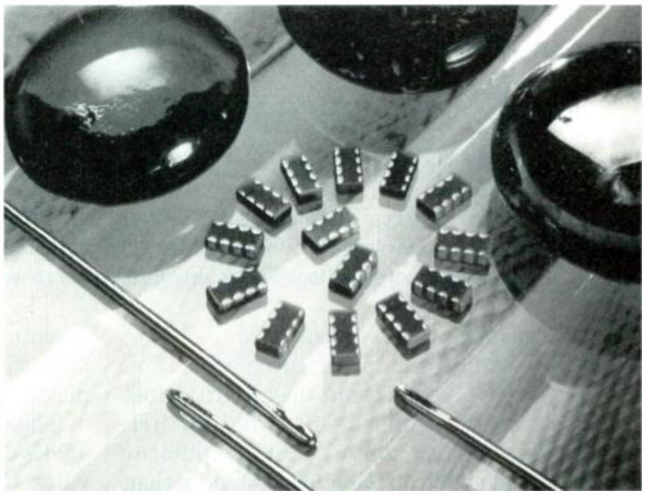
Richard Nass

If you crave the latest in portable products and technologies, the place to go is the Fifth Annual Portable by Design Conference and Exhibition, held at the Santa Clara Convention Center, Santa Clara, Calif., February 9-12. As in previous years, the exhibition proves to be the showcase for portable-component vendors to unveil their latest products. Such products range from batteries to displays to passive components.

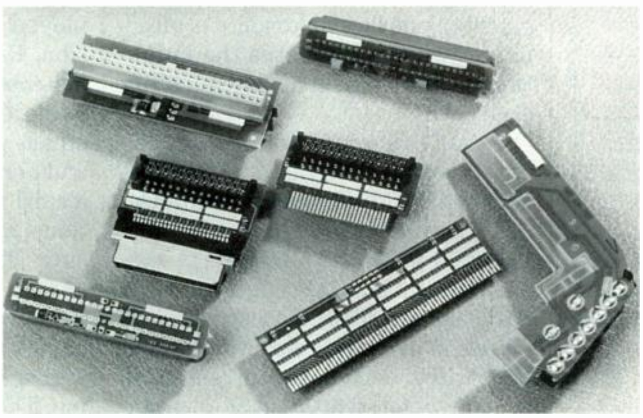
It's no secret that battery technology has come a long way recently. One example of that evolution is the Molicel lithium-ion battery, offered by NEC Electronics Inc., Santa Clara, Calif. The cylindrical and prismatic rechargeable batteries are aimed at consumer applications as well as portable devices. The batteries are deemed as replacements for traditional nickel-metal-hydride (NiMH) and nickel-cadmium (NiCd) batteries.

According to the company, the lithium-ion batteries incorporate a "smart" technology, called SBS, which means that it can measure, calculate, update, and communicate accurate battery-status and usage information to the host device. Running at 11.1 V nominal, the battery provides 45 Wh of energy. The SBS compliance also ensures that the battery can send its charging requirements to an SBS-compliant charger, allowing it to configure the charging supply with the necessary current and voltage. This helps maintain a full-charge potential. Most of the batteries are available immediately.

A second battery type hails from AER Energy Resources Inc., Atlanta, Ga. The company will display its line of zinc-air products at Portable by Design. The company's latest products are of the smaller variety, specifically for hand-held computers. For example, a prototype cell is about 70% smaller than its replacement. A battery pack containing three of these cells should provide up to five times the battery run time of two conventional AA alkaline batteries. As a result, users can get several weeks of run time between recharges.



1. A family of decoupling interdigitated capacitors offers inductance values as low as 175 pH. The devices work with components operating at speeds in excess of 300 MHz.



2. A line of surface-mount chip resistor networks can replace discrete resistors and arrays. The variable thick-film leaderless chip resistor networks offer a 25% to 35% space savings over SIP networks, discrete resistors, and arrays.

Displays promise to be another area of discussion at the conference. Kent Displays Inc., Kent, Ohio, will show its latest display, a one-eighth VGA Cholesteric LCD (ChLCD) module. The company claims that its ChLCDs offer better reflectivity, a 360° viewing cone, and exceptional daylight contrast—even in direct sunlight—all without the need for back lighting. Other features include a peak reflectivity of 40% and a 25:1 contrast ratio.

In addition, the ChLCD technology offers the power-management features needed for portable applications. ChLCDs are bistable, meaning that once an image is written to the display, it doesn't require the power-draining refresh cycles associated with standard LCDs to remain visible. In fact, the panel can hold an image indefinitely without consuming any battery energy, re-

3. A Miniature Card developed by Duel Systems, is available in 3.3-, 5-, and 3.3/5-V combinations. The matchbook-sized cards employ a two-piece design that snaps together for easy testing prior to welding.

gardless of the display size.

A line of interdigitated capacitors (IDCs) give circuit designers inductance values as low as 175 pH, whereas a conventional capacitor could have an inductance of more than 1200 pH. Developed by AVX Corp., Myrtle Beach, S.C., the decoupling capacitors are designed for use with high-speed microprocessors, digital-signal processors, and memory devices operating at speeds greater than 300 MHz *(Fig. 1)*.

The capacitors' low inductance is achieved by connecting the capacitor with a series of eight vias to the power and ground planes in an alternating (interdigitated) pattern. The geometry of these elements is alternated, which alternates the inductance values, ultimately canceling each out.

A wide range of doubly rotated crystals was designed by Oak Frequency Control Crystals, Whitby, Ontario. The family includes SC, FC, and IT cuts from 4.333 to 160 MHz in various conventional through-hole and SMD holders. The devices are suited for use in ovenized oscillator applications with oven temperatures from 60 to 110°C. They feature long-term stability (as low as 10 ppb/yr. aging) and improvements in phase noise, frequency-temperature stability, and vibration sensitivity when compared to equivalent AT-cut devices.

Portable by Design attendees will witness the debut of a line of surface-mount chip resistor networks which can replace discrete resistors and arrays. Manufactured by the Methode Development Company, Chicago, Ill., the variable thick-film leaderless chip resistor networks offer a 25% to 35% space savings over SIP networks, discrete resistors, and arrays *(Fig. 2)*. The leaderless design enables circuit miniaturization and offers a lower surface profile than many other surface-mount components.

The resistor arrays are printed on a 96% Alumina substrate. Multiple values of resistors can be printed on one substrate. Standard and custom-sized packages are available in either isolated or bused configurations. Tolerance ranges are ±1% to ±20% with a power capability of up to 0.25 W. Suitable applications include automotive electronics, PCs, cellular communications, and consumer electronics.

One technology that's starting to pervade portable electronics is the Miniature Card, which can be employed to record and store information. Removable and reusable, the matchbook-sized cards are employed in digital cameras, voice recorders, smart pagers, cellular telephones, and personal digital assistants. Such a card was developed by Duel Systems, San Jose, Calif. The card measures 38 by 33 by 3.5 mm, and is currently available in 3.3-, 5-, and 3.3/5-V combinations *(Fig. 3)*. The card's two-piece design snaps together for easy testing prior to welding. The top and bottom cases have a metal connect for built-in ESD protection. In addition, the steel and plastic frame doesn't rely on components for package strength.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RF Semiconductors Take Center Stage On The Wireless Show Floor

If It Amplifies, Attenuates, Oscillates, Or Radiates, You Should Be Able To Find It At The Wireless Exhibition.

Lee Goldberg

While those attending this year's Wireless Symposium will be spending much of their time at the technical sessions, there's still a strong draw to the exhibition floor. The show, hosted by Electronic Design and Microwaves and RF magazines, is packed full of new products which can improve the performance and profitability of nearly any wireless business endeavor. There's a good chance you'll "strike gold" when you take a stroll through the exhibit area.

The RF semiconductor is the centerpiece of this event, with plenty of new and exciting items for 1998. Anadigics, Warren, N.J., for example, is featuring its new AWT1902, a single-supply, integrated RF power amplifier for GSM-based applications in the PCS (1.9-GHz) and DCS (1.8-GHz) bands. This three-stage unit runs on a single 4.8-V supply and delivers 32-dBm output power with a typical power-added efficiency of 45%.

Another new RF power amplifier will make its debut at Wireless. Made by California Eastern Labs, Santa Clara, Calif., the UPC2771TB MMIC amplifier is aimed at cellular and other applications in the 900- to 1500-MHz band. It delivers 21-dB gain across its entire range and supplies output power of +12 dBm at 900 MHz, and +11 dBm at 1500 MHz. For compact applications, the UPC2771TB is housed in a six-pin super minimold or SOT-363 package.

Oneof the fastest growing niche markets in wireless it RF tagging. These devices can be used for everything from inventory control to vehicle tracking systems. EM Marin, Marin, Switzerland, will be displaying its P 4022 transponder at Wireless. This read-only, factory-programmed device has been optimized for induction-read tags. It uses the industry-standard "Supertag" anticollision protocol for individual identification. The device has a ROM capacity of 48 user bits, plus a 16-bit CRC word. Typically operating in the 110 to 150 kHz region, it can also be used within RF tags operating at higher frequencies.

Stepping back from the antenna a bit, RF Micro Devices, Greensboro N.C., has just rolled out a single-chip upconverter which combines a double-balanced mixer stage and an output amplifier stage. The RF2608 is intended for dual-mode cellular telephones, which employ both CDMA digital and AMPS or TACS analog modulation. The compact device is fabricated in GaAs and operates on supply voltages ranging from 2.7 V to 5.0 V. Only a few external capacitors are required for interstage matching. Pricing for 1000-piece orders is $0.98 each.

With The Increasing Importance Of Digital In Wireless, Much Of The Action Is Also Back At The Baseband.

Less complex, but equally important components, such as RF mixers, attenuators, and switches, also are in abundance at Wireless. One such device is the SKY-60LH, from Mini-Circuits, Brooklyn, N.Y. With a 2.5- to 6.0-GHz bandwidth, and a dc to 1.5-MHz IF response, the low-power device has a very-low conversion loss of -6.2 dB, an IP3 of 15 dBm, and 28 dB of L-R isolation. Housed in a compact surface-mount package, the high-performance device costs $16.95 in small quantities.

NJR Corp., Mountain View, Calif., will be exhibiting its NJG1506R, a low-loss, GaAs RF switch IC. With a range of 0.1 to 3 GHz, it exhibits a typical insertion loss of 0.3 dB at 1 GHz.

If your RF design requires attenuation of a signal, RF Power Components Inc., Bohemia, N.Y., might be able to help you. Offering a standard line of surface-mount attenuators, the three-port devices deliver signal drops from 1 to 30 dB at up to 8-W of power. The thick-film devices have extremely low VSWR and platinum-silver terminals.

Baseband Silicon Abounds

With the increasing importance of digital technologies in wireless communications, much of the action is back at the baseband. One significant player in this area is American Microsystems Inc., Pocatello, Idaho. They've used their new 3.3-V, high-density 0.5-mm digital-CMOS process to solve the kinds of challenges faced by today's RF designers. With a density of 6000 usable gates per square millimeter, the process is being used to create submicron gate arrays and standard cells which consume very little power and run at speeds sufficient to perform the complex processing tasks in a digital RF system. Initial applications of this technology will be a series of SRAMs, but other more complex parts and custom devices are expected in the near future.

Mororola's Semiconductor Products Div., Phoenix, Ariz., also will be exhibiting a formidable array of both RF and baseband products at Wireless. Of particular interest is its M-Core processor architecture, a low-power, 32-bit, micro-RISC solution for portable equipment applications

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  - *Enhanced Outputs*
  - *Zero Preload*
  - *End fan cover*
  - *Top fan cover*
  - *Rack Assemblies*

STOCKED MODELS - Available in 3 days.

Max Power	Output 1	Output 2	Output 3	Output 4	Model*
400W	5V @ 50A	12V @ 12A	12V @ 12A	5V @ 10A	FT46A2332-45P
400W	5V @ 50A	12V @ 12A	24V @ 6A	12V @ 6A	FT46A2363-45P
600W	5V @ 60A	12V @ 12A	12V @ 12A	5V @ 10A	FT46C2332-13P
600W	5V @ 60A	12V @ 12A	24V @ 6A	12V @ 6A	FT46C2363-13P

**400W models include power fail monitor, current limited modules, zero preload and end fan cover options. 600W models include the same options except fan cooling is built into the unit.*

UNITS FROM STOCKED MODULES - Available in 2 weeks.

FT 44 B 2 3 3 6 - YY X

- Series (FT)
- Configuration (44)
- Power Code (B)
- Output #1 Code (2)
- Output #2 Code (3)
- Output #3 Code (3)
- Output #4 Code (6)
- Sum of Option Codes (YY)
- Output #1 Variant (X)

Configuration: Allowable quad output configurations are 42, 44, 46 and 48.

Power Code: Choose Power Code A through D for 400-750W models.

Output Codes: Select any outputs from the shaded area on the Output Types table consistent with the configuration chosen.

Option Code: Specify Option Code. Refer to the Option table. Codes 02 (redundancy) and 16 (enhanced) are excluded from models available in 2 weeks. Fan cooling is built into 600 and 750W units.

OPTIONS

Option Code	Function
00	None
01	Power Fail Monitor
02	Redundancy
04	Current Limited
08	Zero Preload
16	Enhanced
32	End Fan Cover
64	Top Fan Cover

Replace the YY with the sum of the Option Codes.

MODEL SELECTION

Models are available in power ratings of 400 to 1000 watts, with corresponding code letters A through E. See Power Code chart.

Output modules are available in six types: J, K, L, M, N and P in nominal power ratings from 75 - 500 watts. Type M, N and P modules are variable power rated depending upon the unit power rating. The M, N and P Module table directly below shows the corresponding multiplier applicable to the output current ratings of the M modules and allowable power ratings for the N and P modules. For example, a 750 watt multiple will have its M type module configured to produce 120A @ 5V or 12A @ 48V. The voltage and current rating of output modules are listed in the table of output types. This table assigns an alpha-numeric code designating the nominal voltage rating of the module.

Power Code	Unit Power Rating	M Module Current Multiplier		N/P Module*
		Single Output	Multiple Output	Allowable Power Rating
A	400W	0.8	0.5	250W
B	500W	1.0	0.6	300W
C	600W	1.2	0.8	400W
D	750W	1.5	1.2	500W
E	1000W	2.0	1.5	750W

**When an N or P module is used as the main output, the allowable power and the module current ratings must not be exceeded.*

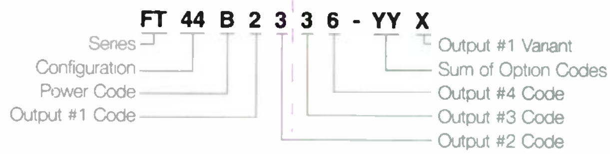
Output Types*						
Output		Module Type				
Code	Volts	J Amps	K Amps	L Amps	M Amps	N/P Amps
0	2	10	20	30	100	60
1	3.3	10	20	30	100	60
2	5	10	20	30	100	60
3	12	6	12	24	42	42
4	15	5	10	20	33	33
5	18	4	8	16	28	28
6	24	3	6	12	21	21
7	28	2.5	5	10	18	18
8	36	2	4	8	14	14
9	48	1.5	3	6	10	10
A	2.2	10	20	30	100	60
B	2.4	10	20	30	100	60
C	2.7	10	20	30	100	60
D	3	10	20	30	100	60
E	3.6	10	20	30	100	60
F	4	10	20	30	100	60
G	4.5	10	20	30	100	60
H	5.7	10	20	30	90	60
J	6.3	10	20	30	80	60
K	7	9	18	30	70	60
L	8	8	16	30	62	60
M	9	8	15	30	56	56
N	10	7	14	30	50	50
P	11	7	13	27	45	45
Q	13.5	6	11	22	37	37
R	17	5	9	18	30	30
S	19	4	8	16	26	26
T	21	4	7	14	24	24
U	23	4	7	13	22	22
V	26	3	6	12	19	19
W	29	3	5	10	17	17
X	32	2	5	9	16	16
Y	40	2	4	8	13	13
Z	44	2	4	7	12	12

Multiple output modules of a given type are arranged in ascending order by voltage magnitude in the same sense as the output number sequence in the configuration diagrams.
**Shaded ratings are stock.*

HOW TO ORDER

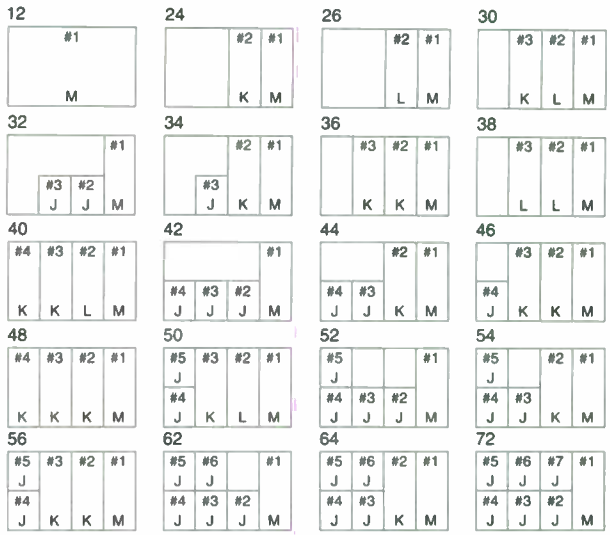
To form the proper model number defining a custom requirement, select the letters FS or FT to designate the series, then choose the desired configuration and list the configuration code. Insert the power code letter for the power level and follow with the output code numbers or letters for each specific output. Enter a dash and from the option table insert the sum of the option codes. Where lower power is desired for the main module, an N module can be substituted and is denoted by a letter N in the output variant position. In addition, when no preload is available for the main output, choose Option Code 08 and add a P in the output variant position. For an enhanced **main** and **current** limited auxiliaries, specify both 04 and 16 option codes.

HARMONIC CORRECTED 500W QUAD SWITCHER



OUTPUT CONFIGURATIONS

The boxes below are diagrammatic representations of the power supplies as viewed from the output end. The two-digit numbers above the boxes are the configuration codes.



Refer to the table below for allowable configurations by series.

Output Config	Unit Power Rating				
	400W	500W	600W	750W	1000W
12	•	•	• x	• x	x
24	•			• x	
26		•	• x	• x	x
30					x
32	•			• x	
34	•	•	• x	• x	
36	•	•	• x	• x	x
38					x
40					x
42	•	•	• x	• x	
44	•	•	• x	• x	x
46		•	• x	• x	x
48			x		x
50					x
52	•	•	• x	• x	x
54		•	• x	• x	x
56			x		x
62		•	• x	• x	x
64			x		x
72			x		x

- • *Represents allowable configurations for the FT Series.*
- x *Represents allowable configurations for the FS Series.*

SPECIFICATIONS

INPUT
90-264 VAC, 47-63 Hz.

POWER FACTOR
0.99 typical.

EMISSIONS
FCC 20780 Part 15/EN 55022, Class A Conducted. EN 61000-3-2, Harmonics. EN 61000-3-3, Voltage Fluctuations.

IMMUNITY
IEC 1000-4-2/EN 61000-4-2, Electrostatic Discharge. IEC 1000-4-3/EN 61000-4-3, Radiated Field. IEC 1000-4-4/EN 61000-4-4, Electrical Fast Transients. IEC 1000-4-5/EN 61000-4-5, Level 3 Surge. IEC 1000-4-6/EN 61000-4-6, Conducted Field.

INPUT SURGE
230 VAC - 38 amps max. 115 VAC - 19 amps max.

EFFICIENCY
75% typical.

HOLDUP TIME
20 milliseconds from loss of AC power.

OUTPUTS
See model selection table. Outputs are trim adjustable ±5%.

OUTPUT POLARITY
All outputs are floating from chassis and each other and can be referenced to each other or ground as required.

LINE REGULATION
Less than ±0.1% or ±5mV for input changes from nominal to min. or max. rated values.

LOAD REGULATION
±0.2% or ±10mV for load changes from 50% to 0% or 100% of max. rated values.

MINIMUM LOAD
Main output requires a 10% minimum load for full output from auxiliaries. Use Option 08 if no minimum load is available for mains up to 500 watts. Singles require no minimum load.

RIPPLE & NOISE
1% or 100 mV, pk.-pk., 20 MHz bandwidth.

OPERATING TEMPERATURE
0-70°C. Derate 2.5%/°C above 50°C.

COOLING
A min. of 10 LFS* for models without internal fans directed over the unit for full rating. Two test locations on chassis rated for max. temperature of 90°C. 600 watt, 750 watt and 1000 watt models have built-in ball bearing fans.
*Linear feet/second.

TEMPERATURE COEFFICIENT
±0.02%/°C.

DYNAMIC RESPONSE
Peak transient less than ±2% or ±200 mV for step load change from 75% to 50% or 100% max. ratings.

RECOVERY TIME
Recovery within 1%. Main output - 200 microseconds. Auxiliary outputs - 500 microseconds.

SAFETY
Units meet UL 1950, CSA 22.2 No. 950, EN 60 950, IEC 950.

ISOLATION
Conforms to safety agency standards.

INPUT UNDERVOLTAGE
Protects against damage for undervoltage operation.

SOFT START
Units have soft start feature to protect critical components.

OVERVOLTAGE PROTECTION
Standard on all outputs.

REVERSE VOLTAGE PROTECTION
All outputs are protected up to load ratings.

OVERLOAD & SHORT CIRCUIT
Outputs protected by duty cycle current foldback circuit with automatic recovery. Standard auxiliaries have additional back-up fuse protection. Options 04 and 16 have square current limiting with automatic recovery when overload is removed.

THERMAL SHUTDOWN
Circuit cuts off supply in case of local over temperature. Units reset automatically when temperature returns to normal.

FAN OUTPUT
Nominal 12 VDC @ 12 watts maximum.

INHIBIT
TTL compatible system inhibit provided. Option 16 has individual output inhibit.

REMOTE SENSING
On all outputs except standard and 04 Option outputs 75 watts or less.

SHOCK & VIBRATION
Shock per MIL-STD 810-E Method 516.4, Procedure I. Vibration per MIL-STD 810-E Method 514.4, Category 1, Procedure I.

MECHANICAL

CASE	SERIES	WATTS	H	x	W	x	L
1	FT	400W/500W	2.50"	x	4.93"	x	8.00"
3	FT	600W	2.56"	x	5.08"	x	10.03"
4	FS	600W	2.56"	x	5.08"	x	11.00"
5	FT	750W	2.63"	x	5.20"	x	10.03"
6	FS	750W	2.63"	x	5.20"	x	11.63"
7	FS	1000W	2.56"	x	7.13"	x	11.63"

OPTIONS

POWER FAIL MONITOR
Optional circuit provides isolated TTL and VME/VXI compatible ACFAIL signal providing 4 milliseconds warning before main output drops by 5% after an input failure. A SYSRESET signal following VME timing requirements is provided when an N module is used as a main output. Both logic signal outputs can sink current per the VME specification.

REDUNDANCY
Optional Or-ing diodes for hot pluggable N+1 redundant operation. For FT Series 500 watt & 750 watt models with 1-4 outputs. Main output current limited to 100 amps. Remaining outputs 16 amps max.

CURRENT LIMIT
Option provides on all outputs:
- Square current limit with auto recovery.
- Wireless droop current share for parallel or N+1 redundant operation.

ZERO PRELOAD
Optional circuit removes need for preload on main output to 500 watts.

ENHANCED
Option provides on all outputs:
- Square current limit with auto recovery.
- Single wire active current share for parallel or N+1 redundant operation.
- DC output good logic signal with LED indicator.
- Logic inhibit.
- Nominal 5V bias.
- Margining.

END FAN COVER
Optional cover with brushless DC ball bearing end fan which provides the required air flow for full rating.

TOP FAN COVER
Same as above with fan cover mounted on top of the power supply.

ACCESSORIES
RA50 and RA75 Series 2U high rack assemblies provide hot pluggable interface and hold up to 3 FT Series 500 watt or 750 watt units respectively.

Specifications subject to change without notice.

Deltron inc. POWER PRODUCTS
290 WISSAHICKON AVENUE, P.O. BOX 1369, NORTH WALES, PA 19454
PHONE: 215-699-9261 • FAX: 215-699-2310 • TOLL FREE: 1-800-523-2332
E-MAIL: sales@deltroninc.com • VISIT OUR WEB SITE: www.deltroninc.com

98703A

where battery life and cost are critical. Its universal load-store RISC engine executes 16-bit instructions and has a 32-bit internal data path for instructions and data. Capable of running on a 1.8-V supply, the processor core's architecture manages its power consumption on a clock-by-clock basis.

Of course, all the chips in the world are useless without the engineering expertise to make them into something useful. At the Wireless exhibition, designers will find tons of software, evaluation kits, and other tools that can help them through the toughest projects.

Designers can get a running start when designing applications requiring short-haul, low-power, low-speed data links, thanks to a pair of engineering development kits available from RF Monolithics Inc., Dallas, Tex. Both kits employ RF Monolithics' Virtual Wire technology. Virtual Wire supports transmission rates of up to 19.2 kbits/s over distances of 100 yards or more.

The kits are fully functional and only require an RS-232 serial interface to connect to a computer. The DR1005-DK operates at 433.92 MHz, and the DR1004-DK uses 916.5 MHz. Both kits implement a wireless media-access protocol and transparent error-correction techniques. Pricing is $400 for a kit which includes two protocol boards, two transceiver boards, antennas, batteries, driver software, and a complete royalty-free reference design.

For those directly involved with the design of high-frequency circuits, simulations are easier than ever. Written to run on a standard Windows 95- or NT-based PC platform, the Serenade 7.0 integrated software suite offers schematic, circuit-analysis, and layout capability in a single package with a unified graphical user interface. Its creator, Ansoft Inc., Pittsburgh, Penn., has endowed the package with design-capture capabilities, which permit analysis, optimization, and physical design, while keeping track of performance and manufacturability factors.

Testing and verification of CDMA-based products has just gotten much easier, thanks to a new automated test system offered by Telecom Analysis Systems, Eatontown, NJ. The turnkey system automatically tests a telepho e's adherence to the CDMA perfor ance standards specified for both ... cellular and PCS networks.

PRODUCT FEATURE

Dual-Axis IC Accelerometer Includes On-Chip Signal-Conditioning Circuitry

Following up on its ADXL50 accelerometer IC for automotive airbag applications, Analog Devices has introduced two devices with higher levels of integration and 1/5th the power-consumption levels of the first-generation device. The ADXL150 is a single-axis device, while the ADXL250 is a dual-axis device with signal-conditioning circuitry. These improved replacements for the ADXL50 offer lower noise, a wider dynamic range, and improved zero-g bias drift. Both devices have their sensitive axes in the same plane as the silicon chip.

The accelerometers feature an acceleration range of ±5 to ±50 g, an 80-dB dynamic range, a signal-to-noise ratio allowing resolution as low as 10 mg, and full-scale pin-programmable settings of ±50 g or ±25 g. Both feature a typical low noise of 1 mg/ $\sqrt{Hz}$ and power dissipation of just 1.8 mA per acceleration axis. Device scale factor can be increased from 38 mV/g to 76 mV/g by connecting a jumper between the IC's V_{OUT} and offset null pins. Zero-g drift has been reduced to just 0.4 g over the industrial operating-temperature range, a 10-fold improvement over the ADXL50.

The scale factor and the zero-g output level are both ratiometric to the power supply, eliminating the need for a voltage reference when driving ratiometric analog-to-digital converters, such as those found in most microprocessors. The only external component needed for operation is a power-supply bypass capacitor. Both devices can work from a power-supply voltage as low as 4 V.

The ADXL250 includes two sensors, oriented 90° apart. Both share the same on-chip clock-generation and demodulator/timing circuits. However, each sensor receives the clock signal via its own driver inverters and have completely independent signal channels following the sensor. A self-test pin is available to activate both sensors simultaneously, simplifying the interface to a microprocessor.

Both the ADXL150 and ADXL250 are available in a 14-pin hermetically sealed surface-mount Cerpak packages. They're specified to operate over the commercial operating-temperature range of 0 to 70°C and the industrial operating-temperature range of -40 to +85°C.

The ADXL150 costs $12.45 each and the ADXL250 is priced at $19.95 each in 100-unit lots. Both are available from stock.

Analog Devices
Ray Stata Technology Center
804 Woburn St.
Wilmington, MA 01887
(617) 937-1428
fax (617) 821-4273
http://www.analog.com
CIRCLE 491
ROGER ALLAN

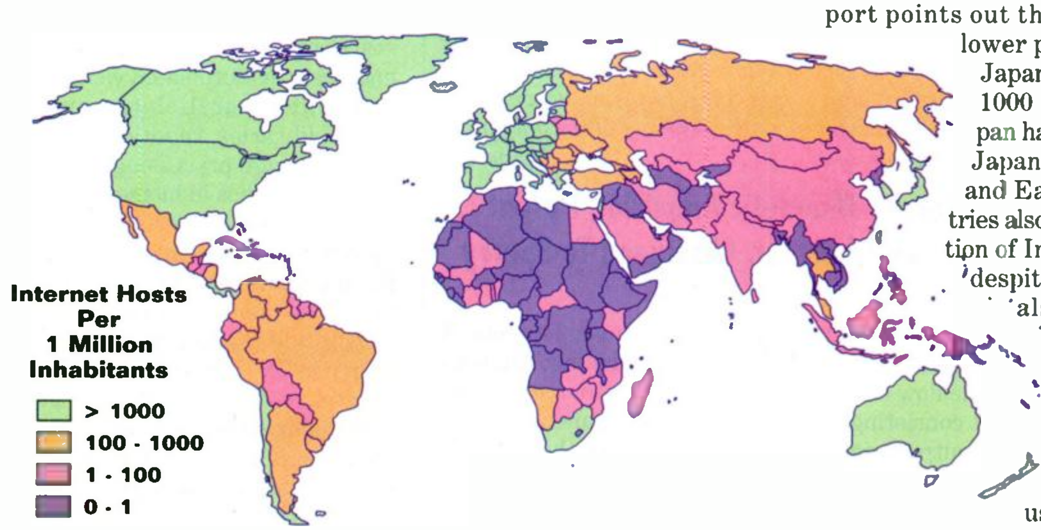
ELECTRONIC DESIGN QUICK LOOK

■ Edited by Mike Sciannamea and Debra Schiff

MARKET FACTS

Internet Vs. The Telecoms

The intrinsic difference between the Internet and the telecommunication services worldwide is that the Internet was born out of a completely unregulated network, while the telecoms are heavy with regulation. Internet expansion and evolution is exponential in its timing, while the telecoms are cautious and slow moving. A detailed look at the impact of the Internet on the planet's telecommunication concerns can be found in a new report from the International Telecommunication Union entitled, "Challenges to the Network: Telecoms and the Internet." According to the new report, Internet usage sits at about 60 million users worldwide, with about 16.1 million host computers serving that audience. Meanwhile, the number of telephone lines active on the planet at the beginning of 1997 was counted at about 741 million. So, here are all these Public Telecommunications Operators (PTOs) who don't function well using new technologies and services that don't fall under their control trying to deal with fast data transmission systems such as Asynchronous Transfer Mode (ATM). The report predicts that if the PTOs don't get on the ball and start to adapt to the head-turning changes that are taking place in telecommunication, they will be lost. The conflict breaks down into three main areas: ownership, pricing, and technology. Primarily, PTOs are run by their national governments, but there are a few major PTOs that are headed by foreign companies. At the same time, the Internet has no national boundaries. The PTOs then charge the Internet Service Providers (ISPs) full-circuit costs associated with connecting to an Internet backbone in a foreign country. This policy is in opposition to the PTO accounting rate system of half-circuit charging, however. Half-circuit charging consists of splitting the cost and revenue from a leased line or international call between the two or more PTOs providing network service. The report also examines the balance (or rather, imbalance) of Internet access around the world. Predictably, the wealthier nations see over 1000 ISPs per one million inhabitants, while developing nations can range between zero and 100 ISPs per one million inhabitants. But, there is a quandary surrounding income and the Internet. The report points out that Finland has a 40% lower per capita income than Japan, but have 60 ISPs per 1000 Finnish residents. Japan has 6 ISPs for every 1000 Japanese residents. Central and Eastern European countries also have a high concentration of Internet representation, despite low income levels. It also is quite clear that countries with poor telecommunication facilities or low numbers of telephones would have smaller numbers of Internet users. But, just because a country has had poor performance in the past doesn't mean that they will trail in Internet development in the future. Because many of these countries are starting from the ground level with their telecommunications initiatives, many of them will be building their networks with new, digital equipment. The advantage will be in their favor because Internet services depend so heavily on network digitization. The costs will weigh heavier on countries with large, antiquated networks that will need to move to digital.



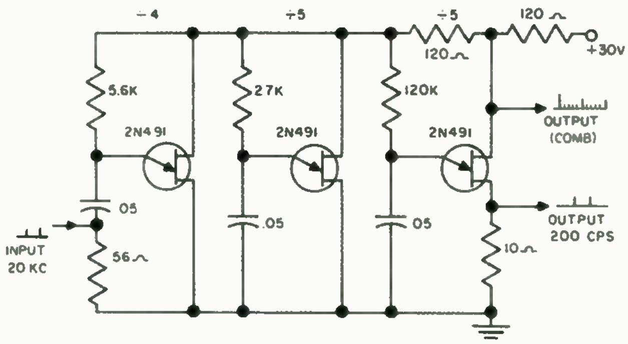
For more information, contact the International Telecommunication Union, Place des Nations, CH-1211 Genève 20, Switzerland; 41 22 730 51 11; fax 41 22 733 7256; Internet: http://www.itu.ch.—DS

40 YEARS AGO IN ELECTRONIC DESIGN

More Circuits Transistorized With The Silicon Unijunction Transistor

The silicon unijunction transistor is a three-terminal semiconductor device which exhibits open-circuit stable negative resistance characteristics. It is primarily useful in switching and oscillator applications. It can be operated in a number of different circuit configurations such that any of the three terminals can serve as a signal input or a load output.

The UJT will operate in a bistable, monostable, or astable fashion depending on how the static load lines intersect the emitter characteristics. In the bistable circuit configuration the unijunction transistor may be triggered from the low emitter current state by either raising the emitter voltage or lowering the base-two or base-one voltage. Similarly it may be triggered from the high emitter current state to the low emitter current state by lowering the emitter voltage or by raising the base-one voltage. (*ELECTRONIC DESIGN, Jan. 22, 1958, p.30*)



These are the opening paragraphs taken from a three-page article authored by two General Electric engineers, S.R Brown and T.P. Sylvan. The latter, Pete Sylvan, developed many UJT circuits and was a regular contributor to the "Ideas for Design" section. The circuit shown is a 100:1 frequency-divider circuit. Unfortunately, the text of the article does not discuss any of the four practical circuits it includes as illustrations, of which this is one.—Steve Scrupski

Patents: Bipolar Output Carrier Magnetic Amplifier, Patent No. 2,808,520. John Presper Eckert, Jr. (Assigned To Sperry Rand Corp.)

The magnetic amplifier uses a single output winding on the magnetic core. A carrier frequency source is coupled to one end of the output winding. An input winding on the core controls the flow of energy from the carrier source through the output winding. A circuit consisting of two independent branches is connected to the other end of the output winding so that energy from the source is selectively coupled simultaneously via the output winding to both of the branches. One of the branches has circuit elements for shifting the potential level of signals therein relative to signals in the other branch to effect signals of different relative polarities in the two output branches. (*ELECTRONIC DESIGN, Jan. 22, 1958, p. 113*)

J. Presper Eckert, along with John W. Mauchly, developed the first electronic digital computer, the Eniac, in 1946 at the University of Pennsylvania. The Eniac used 18,000 vacuum tubes running at a 100-kHz clock rate. It occupied a room 30 by 50 ft., and consumed 150 kilowatts. Eckert and Mauchly formed the first commercial computer company in 1948. In 1950, the two sold their Eckert Mauchly Computer Corp. to Remington Rand (later Sperry Rand), which introduced its Univac I in 1951.This patent reflects the status of magnetics as a mainstream computer technology in computers throughout the 1950's and 60's.—Steve Scrupski

Steve Scrupski is a former Editor-in-Chief of ELECTRONIC DESIGN. Now semiretired, he can be reached at scrupski@worldnet.att.net.

Columbia Gets Gift

Just in time for the spring semester, Columbia University, New York, N.Y., has received a generous $25 million gift from international businessman Z.Y. Fu. In recognition of the donation, Columbia is renaming its School of Engineering and Applied Science as, The Fu Foundation School of Engineering and Applied Science. The university expects that the money will transform the school, allowing it to produce more qualified students.

Fu decided to give such a large gift because Columbia has a very long association with Chinese professors and students. He continued to say that scores of Chinese students have attended the school and participated in the Fu Foundation Scholars program already in place at Columbia. Fu hopes that the school will continue to grow as an international leader in science and technology.

According to the school, the initial areas targeted for support are computer science, biomedical engineering, applied mathematics, and electrical engineering. Current research at Columbia in computer science includes automated vision environments, parallel computing, digital libraries, robotics, and natural language processing. The university's studies in biomedical engineering encompass orthopedics and musculoskelatal biomechanics, artificial organs, and cardiovascular prosthesis, amongst others.

Applied mathematics sees research in the fields of theory and application of dynamic systems, large-scale computation, and global climate modeling. The electrical engineering department has been a strong area at Columbia for over a century, and concentrates primarily on improving ways of speeding up and handling information through field work and research. Columbia is looking to apply Fu's gift toward enticing more qualified faculty and promising students to the fields mentioned above.

Contact the Office of Public Affairs, Columbia University, 535 W. 116th St., Room 304; New York, NY 10034; (212) 854-5573; fax (212) 678-4817; Internet: http://www.columbia.edu/cu.—**DS**

PowerPC™ Microprocessors have their place.

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A TOTALLY NEW VISION

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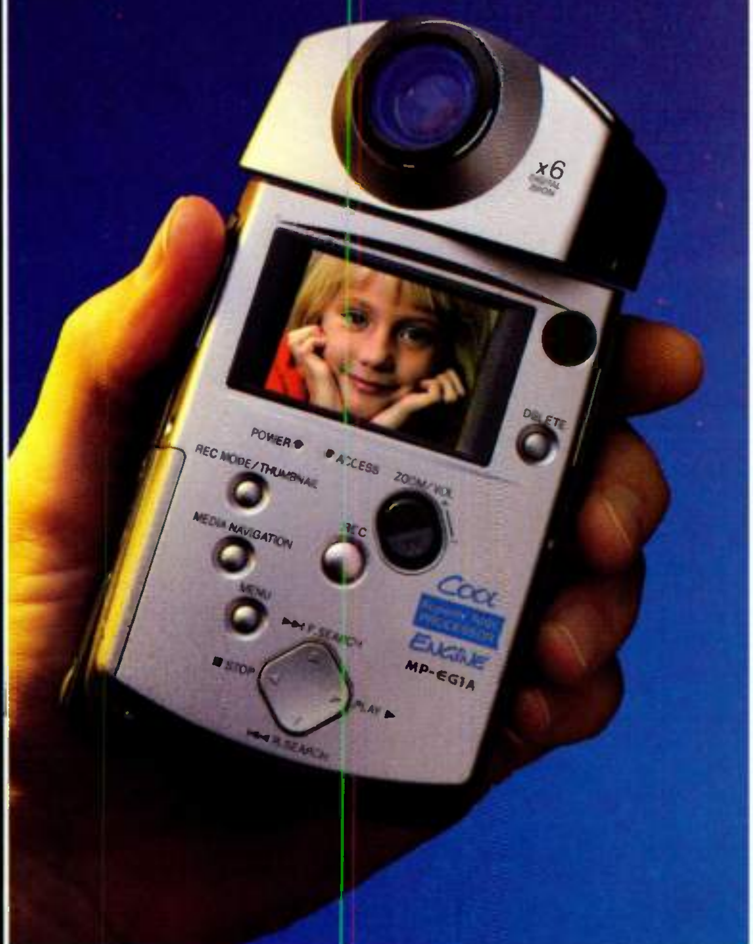


If your new product plans take you out into the world at large, a much more suitable architecture is the Hitachi SuperH RISC engine. It delivers blazing performance because it is designed from the ground up with portable devices in mind. You get low cost and low power, and high integration through a wide variety of on-chip peripherals such as MMU, MAC, direct interface to DRAM and on-chip Flash, to name a few.

All of which makes the SuperH RISC engine the world leader in units shipped for applications off the desktop.

In the area of image processing, the SuperH has found its way into digital still cameras made by Kodak, Polaroid and Casio, not to mention the world's first MPEG still and full-motion camera by Hitachi shown here – along with over 1500 other design wins worldwide. In fact, the SuperH has already become the de facto standard in Personal Access devices running Microsoft® Windows® CE.

Don't get us wrong. The desktop microprocessor has its place. But what about everywhere else?

To find out more about the SuperH RISC engine, phone **1-800-285-1601** or get on the Web and go to **www.hitachi.com/semiconductor**. Unlike certain vendors of desktop chips, we know our place in the world.

SuperH™
RISC engine

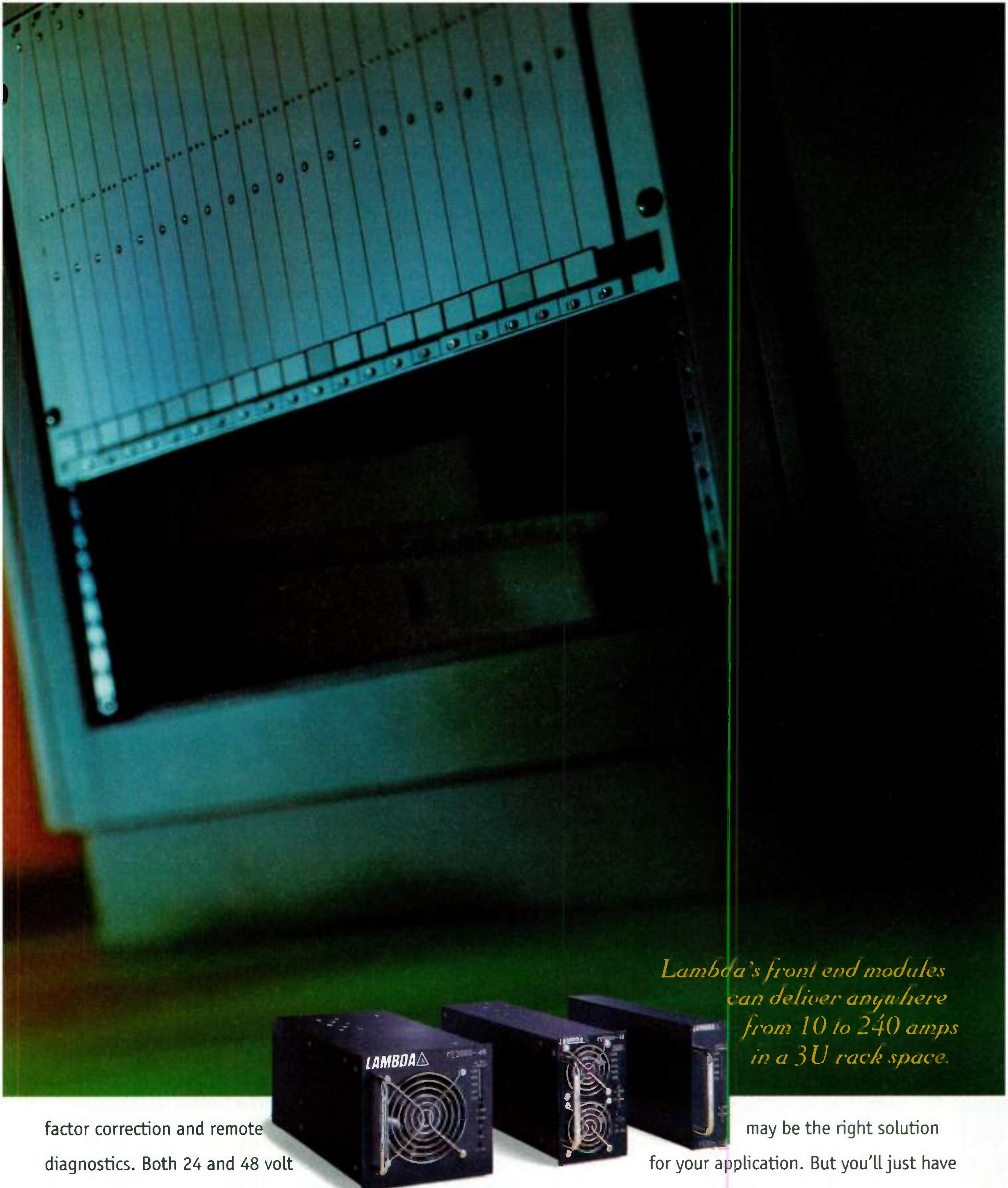
THE COOL ENGINE™ INSIDE

IT'S A HIGH-DENSITY WORLD, AND YOUR OLD RECTIFIERS JUST DON'T FIT IN.

It seems that everything about telecommunications is growing—including the power that systems require and, unfortunately, the space they take up.

Lambda addresses the problem with a series of modular power front ends that occupy up to 35% less space than their nearest competitors. The FE Series modules provide a solution that's scalable in 500, 1000, 2000 and 3000 watt units, and fits in a standard 3U rack shelf with optional Low Voltage Disconnect, battery temperature compensation and circuit breakers.

The modules are hot-swappable, and feature power



factor correction and remote diagnostics. Both 24 and 48 volt output versions are available.

There are plenty of other reasons why the FE Series may be the right solution for your application. But you'll just have to give us a call at 1-800-LAMBDA-4, ext. 8828, because, once again, space is limited.

LAMBDA λ

www.lambdapower.com/fe

READER SERVICE 177

BOOK REVIEW

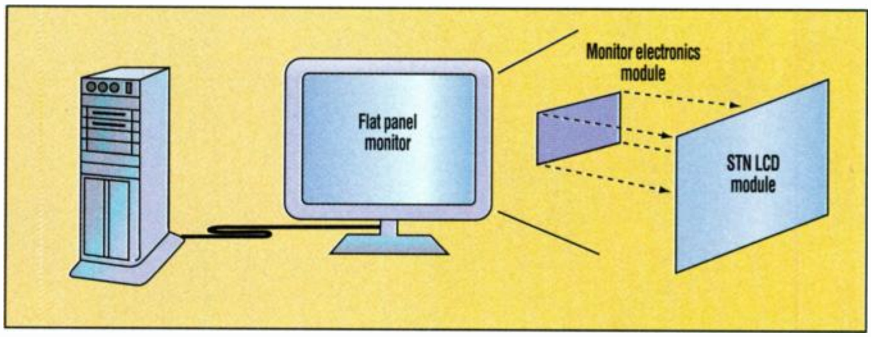
Designing Parts with SolidWorks will help readers learn the basic concepts of SolidWorks, a feature-based, dimension-driven, solid-modeling CAD program for Windows. Instead of text, each page of the book contains illustrations that demonstrate how to create realistic mechanical designs. The book is designed for CAD drafters who wish to learn more about solid modeling, but have yet to purchase a solids-based CAD system. The 320-page book is priced at $59.95. Contact CAD/CAM Publishing Inc., 1010 Turquoise St., #320, San Diego, CA 92109; (619) 488-0533; fax (619) 488-6052.

Fiber Optic Test and Measurement is a guide to measuring both current optical networks and those on the horizon. Readers will learn how to characterize all three basic components of a fiber-optic communication system: the optical transmitter, fiber medium, and optical receiver. Other topics include optical power measurements using several types of photodetectors; modulation measurements via frequency and time domain analyses; and testing digital fiber systems to SONET/SDH international standards. Contact Hewlett-Packard Professional Books, Prentice Hall Inc., Upper Saddle River, NJ 07458; Internet: http://www. phptr.com.

An Introduction to Classical Electromagnetic Radiation describes classical electromagnetic radiation starting from Maxwell's equations and moving on to show how fundamental concepts are applied in a wide variety of examples from areas such as classical optics, antenna analysis, and particle accelerators. Following introductory chapters that cover basic theory, the concept of a plane-wave spectrum is developed and applied to the radiation from apertures. Mathematical and physical explanations are enhanced by over 300 illustrations, and the book also contains 140 problems. The 653-page book is priced at $110 for the hardback edition, and $55 for the softcover edition. Contact Cambridge University Press, 40 West 20th St., New York, NY 10011-4211.

I See Your True Color Shining Through

Arithmos Inc. is introducing its Arithmos Display Engine (ADE) family of products. The Display Engine Architecture defines a new class of application-specific devices for flat-panel displays. These products represent the first VLSI integrated circuits (ICs) specifically designed to go into the monitor. These Display Engines incorporate algorithms to eliminate all artifacts present in older generations of of passive liquid flat-panel displays. The products are targeted for the PC industry that is looking for cost-effective flat-panel display monitor and notebook solutions at a far lower end-user cost than the costlier active matrix thin-film transistor (TFT) displays.



According to Dennis Sabo, president and CEO of Arithmos Inc., "A flat-panel display using Arithmos PerfectColor technology is easily distinguished from alternative products; images are brighter, crisper, and have 24-bit true color photo quality."

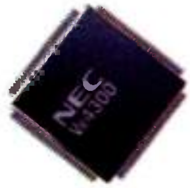
The first Arithmos products to incorporate PerfectColor technology are the ADE100 and ADE200. The ADE100 is designed for monitors with standard digital interfaces such as low voltage differential signaling (LVDS) and PanelLink Technology. The ADE200 will incorporate a unique proprietary algorithm that eliminates the effects of a noisy input signal such as would be found on a standard analog RGB monitor interface. Offering a high-quality interface to today's standard analog interface makes monitor designs using Arithmos product capable of interfacing directly with more than 100 million installed PCs throughout the world.

Both products offer similar features of 24-bit true color display, refresh acceleration up to 4x the input rate, and direct drive of all popular super-twisted nematic (STN) flat-panel displays available from all Japanese flat-panel manufacturers.

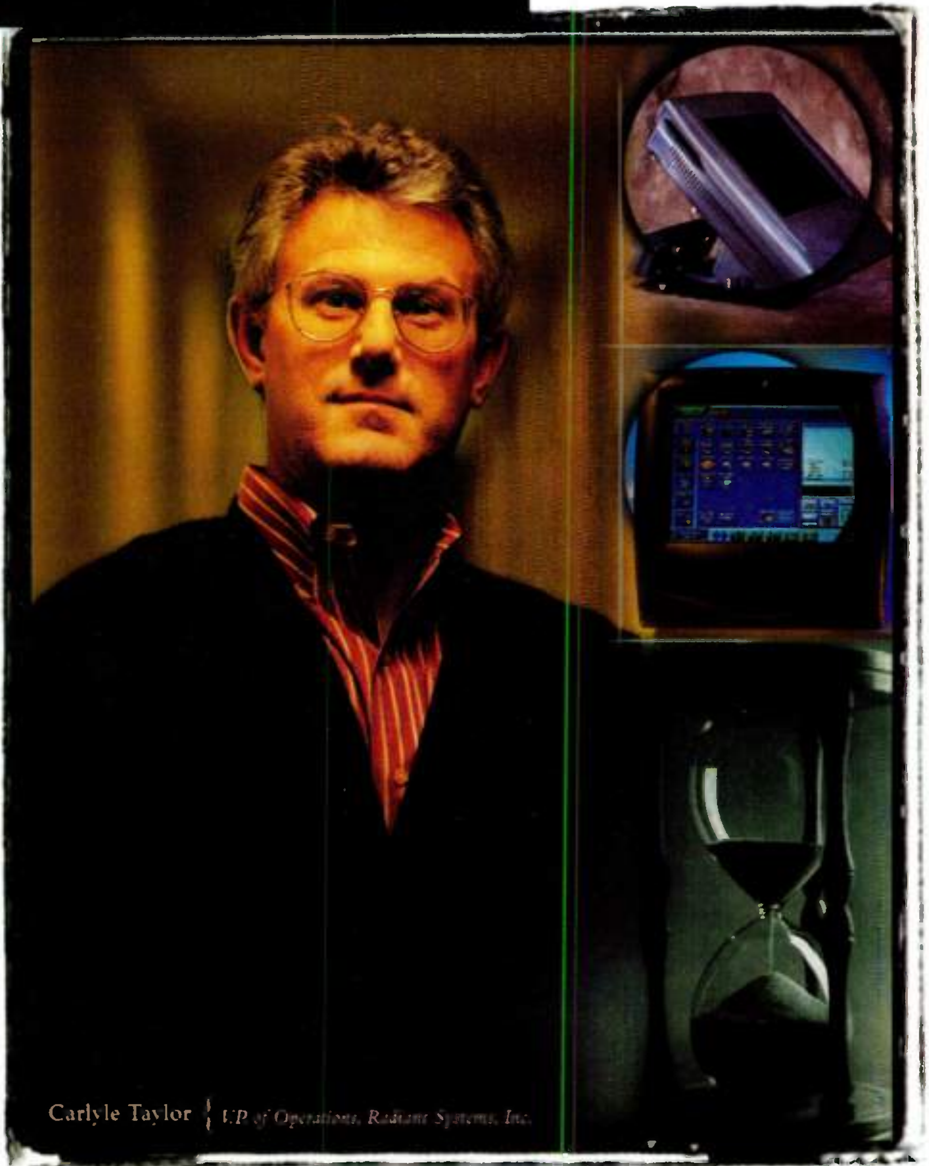
Arithmos has been working with a variety of flat-panel manufacturers to facilitate the integration of their display technologies into flat-panel monitors. The Display Engine solutions enable development of high-performance STN-based flat-panel monitors. Arithmos products can leverage readily available low-cost STN manufacturing capabilities to provide flat-panel monitor solutions that meet corporate PC users' price/performance expectations.

Products are now shipping in production quantities. Pricing for the ADE100 is $25 in 1000-unit quantities, and $28 for the ADE200 in similar quantities. For more information, contact Robert Soderberry, vice president of marketing, Arithmos Inc., 2730 San Tomas Expressway, Suite 210, Santa Clara, CA 95050; (408) 982-4490; Internet: http://www.arithmos.com.—**MS**

"WITH NEC PROCESSORS, WE CAN PUSH THE CLOCK WITHOUT HAVING TO PUSH OUR SANITY."



"With NEC's VR4300 processor, our latest Windows CE terminal went from concept to market in just three months."



"We have a pretty single-minded pursuit here at Radiant Systems: produce changes for the better by developing the most advanced products across a wide range of industries. And we have to do it in shorter periods of time. In fact, these days we go from concept to market in just three months.

"Well, just when you think you can't design any faster, you get hold of a product like NEC's VR4300™ MIPS® RISC processor and companion chip. They're the perfect price/performance solution for our MediaClient™ – a revolutionary Windows® CE multimedia retail terminal. And because of NEC's innovative I/D cache, the VR4300 is ideally suited for our demanding throughput needs. And it's a proven product, fully integrated, with plenty of room for future scalability.

"You get something else, too. You get an exceptional level of confidence working with a company like NEC. There's the technical support, the design support and, of course, the manufacturing clout.

"Any engineer will tell you these are incredible times. Fortunately, Radiant Systems isn't stuck somewhere in the middle of all these changes – we're actually making them happen.

"And NEC? Well, without a doubt, their purpose is to help you speed the design process by providing a total solution that gets you to market fast, maybe even ahead of schedule."

For more information about NEC's VR Series, call 1-800-366-9782. Ask for Info pack #197.

VR SERIES PROCESSORS | WINDOWS CE

NEC

FLIPPING THROUGH THE INTERNET ROLODEX

http://www.datel.com: When you stop in at Datel's new site, don't forget your Adobe Acrobat Reader. The site features over 120 downloadable data sheets that can be viewed in the .PDF file format. Visitors may choose between Switching DC-DC Converters, Digital Panel Meters and Instruments, Sampling Analog to Digital Converters and Data Acquisition Components, and Computer Analog I/O boards for complete listings of the company's products.

Other topics found at the site include new products, contacts, literature, and corporate information. There's a handy site index for visitors who like to get straight to the point, and a light-on-the-graphics approach that speeds up site access.

http://www.wlana.com: Clicking on this URL will bring visitors to the new Wireless LAN Alliance site. Featured are links to members' sites, explanations of how wireless LANs work, technologies, options, configurations, and a glossary. Also featured is a look into the IEEE 908.11 Wireless LAN Standard, specifically the Physical Layer Implementation, Infrared Physical Layer, and MAC Layer. Listings for component and system suppliers' sites also are found here. One unique aspect of the site is the User Stories section. Visitors can view testimonies from people in the health care, trading and banking, consulting and sales, restaurant and retail, warehouse and manufacturing, utilities, and education and research fields. Last, but not least, the Wireless LAN Alliance hosts a resource directory with LAN organization links, books, and links to other sites.

http://www.osa.org: The Optical Society of America's (OSA) new World Wide Web site is now featuring the first issue of the peer-reviewed scientific journal, "Optics Express." The new technology journal has original articles on new developments in all fields of optical science. OSA will archive "Optics Express" on-line and also will offer each volume on CD-ROM. With a completely electronic medium, authors of "Optics Express" material can include or publish within the multimedia realm. Video clips, high-quality graphics, and automatic links to "Optics Express" references can be used. In addition, articles feature keywords for electronic searches.

http://www.wl.net: If you're a 'net surfer interested in watching or keeping up to date with NASA Space Shuttle events, you might want to try this site. Sony Electronics, Microsoft, and WorldLink have teamed to bring interviews with astronauts, live footage, and archived events to the World Wide Web via WorldLink's site. Sony's DSR-130 DVCAM digital video camera uses Microsoft's NetShow 2.0 software to broadcast launches, transmit information from the Kennedy Space Center in Houston, Tex., and monitor live press conferences. The NetShow Server runs on a Compaq ProLiant 5000R.

http://www.sirf.com: SiRF's new site offers visitors a place to examine various scenarios that would be appropriate for global-positioning system (GPS) products. Internet users who set their browsers to this URL will find information on the SiRFstar architecture and its components, GRFI and GSP1 chip sets, and the GSW1 modular GPS receiver software. All of that information includes photographs and specifications. SiRF also includes a GPS white paper at the site and information concerning the future of GPS consumer applications. Corporate information with links to contacts can be found here as well as the latest press releases and press coverage. And, for those surfers looking to change careers, the site does host a list of current job openings and links to the company's Human Resources department.

http://www.eid.co.uk: Electronic Information Displays '97 hosts its site here. Registration can be done on-line, and links to transportation and hotels are readily available. Exhibitors also have their own pages.

OFF THE SHELF

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QUICKNEWS

Not Just Any Packets—Capitalizing on its variable packet writing technology, Smart Storage is now offering its SmartCD for recording 95 software package. SmartCD for 95 is designed to enable network users in a Windows 95 workgroup environment to share a CD recorder. Smart Storage already has SmartCD products that support Windows NT, NetWare, and UNIX environments.

Variable packet writing technology works by treating the transfer of data to a CD-ROM the same way data is saved to a floppy disk or hard drive. SmartCD is useful for those companies whose networks need additional storage space, perform frequent backups, or prefer to distribute their information on CD-ROM.

The 95 version of SmartCD uses a unique cache-file approach to sustain data throughput to the CD recorder. While the CD saving is taking place, networked users can simultaneously copy data to and from the same CD-storage device. DOS commands also are accepted by SmartCD.

One of the major issues companies often have with CD-ROM recording devices and software is that most of them require a premastering step in the process. Multisession recording produces more errors and overhead than variable packet writing technology. SmartCD does not require premastering, thus eliminating those worries.

SmartCD for recording 95 supports the ISO 9660 Level 1 standard, allowing all CDs created using variable packet writing to be accessed on any standard CD-ROM drive. Additionally, the new software allows users to protect their CDs with a password before finalizing the disc.

SmartCD for recording 95 is priced at $425. Resellers can be contacted through Smart Storage.

For more information, contact Smart Storage Inc., 100 Burtt Rd., Andover, MA 01810; (508) 623-3300; (508) 623-3310; Internet: http://www.smartstorage.com.

Gifts For The Gifted—Texas Instruments recently shared their plans to invest $25 million in high-performance digital signal processor (DSP) research at universities around the world. The DSP University Research Fund has now totaled over $50 million in research over the last 15 years. Over 900 universities worldwide use the company's DSPs for training purposes. Additional investments are planned.

Abstracts from universities interested in obtaining funding should conform to the basic criteria listed on the Texas Instruments home page: *http://www.ti.com.*

For more information, contact Texas Instruments, P. O. Box 17228; Denver, CO 80217; (800) 477-8924.

READER SERVICE 110

HOT PC PRODUCTS

Boca Research's Video Communication Suite is a digital videoconferencing solution that includes a digital camera and a 56-kbit/s modem. Also included in the package are Boca's new Internet broadcasting software, Cast-a-Vision; VocalTec's Internet Phone; Stefra's video capture and editing software; and Smith-Micro's VideoLink 324. Applications range from family reunions to contract negotiations between unions and managers.

The digital camera comes from Rockwell, who imbued it with high resolution. Conveniently, the camera plugs directly into the PC, cutting out additional power adapters or cables.

Rockwell also developed the video capture chip that's embedded within Boca's 56-kbit/s Internet modem. This feature eliminates the need for a separate video capture card, opening up another slot for users in their PCs. The modem comes with a speakerphone and a guaranteed upgrade to the 56-kbit/s technology standard as soon as it's approved by the International Telecommunications Union (sometime in early 1998).

Cast-a-Vision allows users to broadcast live audio and video over the Internet. It also allows users to broadcast captured screens, or any section of a computer screen, such as a spreadsheet or windowed application. Additionally, these captured elements can be broadcast live, as well, showing viewers at the other end live updates to the screen. Other features with Cast-a-Vision include caller-ID and -blocking, Internet chat, and password authentication. Broadcast sources can be VCRs, camcorders, laser disks, PC cameras, or digital camera outputs, and other sources.

The VocalTec Internet Phone comes equipped with whiteboarding and conferencing software. These tools allow users and teleconferencing participants to simultaneously create and alter shared documents, photos, and drawings on their own computers. Text chat allows a text record of the conversation to be recorded.

With Stefra's Video Control utility, users can capture live video and photo images and store them on their PCs. These images can then be edited by creating frames around them and pasting them into desktop publications. This feature is particularly handy in the case of the business professional that has to sit for long periods during budget meetings.

The entire Boca Video Communications suite is Plug-n-Play, requiring no power supplies or video cables. It requires IBM-compatible PCs, in the Pentium 75 MHz or higher range; 16 Mbytes RAM; Windows 95, and independent Internet account, sound card, microphone, and amplified speakers.

For more information, contact Boca Research Inc., 1377 Clint Morre Rd., Boca Raton, FL 33487-2722; (561) 997-6227; fax (561) 997-7189; Internet: http://www.bocaresearch.com.

The Dynacomp Engineering Tutorials CD-ROM contains nine educational modules designed to teach digital filtering and transformations. The tutorial is not applications-oriented, but targeted instead at refreshing practicing engineers. The new CD-ROM requires graphics capabilities and a display/read .PCX format images utility.

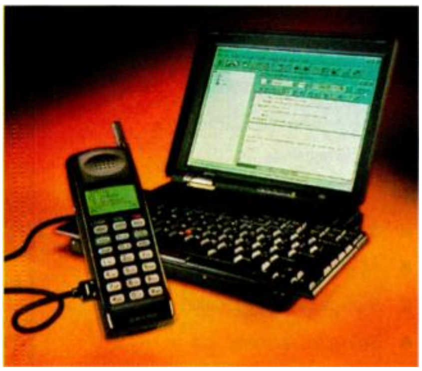
On the MS-DOS- and Windows-compatible CD-ROM, Dynacomp supplies a set of nine tools covering Fast-Fourier Transform (FFT), Inverse FFT, Digital Filter Design, Z-Transform, S-Plane Analysis, Bilinear Transforms, Phase-Locked Loops, Frequency Domain Filtering of Imaging, and Waveform and Image Correlation. Each module comes with the software and a complete manual for that topic. The CD-ROM is priced at $89.95.

For more information on the Dynacomp Tutorial, contact Dynacomp Inc., 4560 E. Lake Rd., Livonia, NY 14487; (716) 346-9788.

The PC Connection Kit for Windows 95 is a low-cost accessory that allows portable computers to also become wireless communicators. From the Personal Mobile Communications Division of Mitsubishi Wireless Communications, the kit uses software to automatically configure a Windows 95-outfitted PC to use a Mitsubishi MobileAccess telephone as a wireless modem. Essentially, it's an easy and painless way of getting to your corporate applications from wherever you might be assigned to go.

The kit works by installing a Wireless Modem Wizard, which, in turn, installs modem drivers for the MobileAccess phone. Users are guided through the configuration routine and connect with their networks.

The kit also includes a Phonebook Manager utility. Phonebook Manager allows the user to enter names and phone numbers into the MobileAccess electronic phonebook, and backs up the phone's contents into a PC file. Other data from personal information management software also can be imported into a MobileAccess phone.



MobileAccess' latest incarnation is the 120. The 9.6-oz. phone features a 4 by 12 alpha numeric LCD display, security protection, 99-number address book, call-timing system, fax and data modems, and many other useful communications tools. The 120 uses the 2.0 version of Unwired Planet's thin client in conjunction with MobileAccess' dual-mode capability to automatically switch between receiving data and voice calls.

MobileAccess users are protected with authentication and encryption techniques that are based on IS-91 fraud prevention standards and RSA data encryption.

For more information, contact Mitsubishi Wireless Communications Inc., Personal Mobile Communications Division, 1050 E. Arques Ave., Sunnyvale, CA 94086; (408) 730-5900; fax (408) 736-5912; Internet: http://www.mobileaccessphone.com.

Y2K UPDATE

With less than two years to deal with the Year 2000 Date Change issue (Y2K), it's evident that some companies simply aren't going to be ready for their computers and systems to go KABLOOIE. What I mean by KABLOOIE is that systems will fail. Most likely, financial records will be incorrect, companies won't be able to deal with customers because they'll be too busy trying to just open their systems. Essentially, it will be ugly, to say the least.

In order to handle the legal issues that will undoubtably arrive swiftly, the *http://www.Year2000.com* web site has recently added the Law Center. The Law Center section of the site connects visitors to two legal firms, Hancock Rothert & Bunshoft LLP; and Thelen, Marrin, Johnson & Bridges LLP. Both are San Francisco, Calif.-based law firms with over 100 attorneys on staff. Both also have formed specific Year-2000 teams to deal with Y2K-related issues.

This area of the site was designed to cover the legal, insurance, and accounting elements of Y2K. To help visitors, the site features articles dating back to November 1996 that deal with legal risks such as breach of contract, class action litigation, tort exposure, statutory exposure, customer fraud exposure, and directory liability. Original features and a question and answer section also are in the works for the Law Center.

But, what is stressed here is the issue of time. Again, less than two years is not a lot of time to bring a company into Y2K compliance. More importantly, in terms of the legal issues, if companies do not act quickly, they're inviting liability—especially directed toward officers and directors. The old rule applies here more than ever; an ounce of prevention equals a pound of cure.

For more information, visit the Law Center directly at the site: http://www.year2000.com/y2klaw-center.html.

I'm really not crazy about quoting the Gartner Group, frankly because *everyone* quotes the Gartner Group, but for the sake of Y2K information on IBM environments I will. According to the independent consultant agency, over a billion lines of source code for IBM environments are missing. If IBM code languages are your problem than, you might want to look into The Source Recovery Company.

Source Recovery is the result of 12 years of code decrypting by Frederick Brandes. Brandes, back in 1985, developed a library of pattern recognition algorithms to handle the locked code. Through research, he discovered that he could use the same methodology to recover mission source code from compiled object code. This technique led to a five-step code recovery process, a repository of code patterns, and a testing procedure.

The repository made it possible for an automatic analyzer to recover the underlying statements from machine code programs. The testing procedure is the guarantee that the code would actually work after being recovered. The really attractive part of all this technology is that it's automated. Basically, technicians can be trained to recover thousands of lines of code per day.

Source Recovery's technology works in the following five steps: disassembly, pattern matching, operand analysis, internals analysis, and supporting information. For those of you who may not be familiar with programming, here's a breakdown of how the steps work. In disassembly, binary object files are converted into hexadecimal files, then back into their original Assembler language. Then, the machine instructions are compared to known sets of COBOL instructions. To recover other program elements, operands discovered in the previous steps are analyzed for data in file descriptions, linkage sections, and working storage sections. Next, other internal areas of the program, including the working storage areas, are analyzed further. Finally, supporting information, such as file layouts, copybooks, etc. are examined.

Contact The Source Recovery Company, 20 Speen St., Second Floor, Framingham, MA 01701; (508) 626-9955; fax (508) 875-7873; Internet: http://www.source.recovery.com.—**DS**

GREENLOOK

It won't be business as usual when Amory Lovins, environmentalist and technical visionary, addresses a group of 7000 engineering professionals at a design conference this February. In his talk "From Laptops to HyperCars: The Wide-Ranging Impact of Portable Technologies on Traditional Industries," Dr. Lovins will illustrate how the lessons learned in the electronics industry can help reinvent many more mature "smokestack" industries, making them cleaner, more energy efficient, and much more profitable. His address will be the keynote speech for a session on environmentally responsible design, held at the Wireless/Portable Design Symposium and Exhibition, held Feb. 10-13 at the Santa Clara Convention Center, Calif.

Founder and codirector of the Rocky Mountain Institute, Snowmass, Colo., Lovins' nontraditional approaches to solving problems has enabled him to build bridges between the environmental, technical, and business communities. He has also built a reputation as an advisor to the energy, transportation, and building industries, providing them with practical insights on how to leverage environmentally friendly technologies and practices as competitive advantages.

One of the most recent spin-offs from the institute is the HyperCar project. Slated for production in early 2000, this new generation of ultra-light, composite-bodied, hybrid-powered vehicles are expected to get 150 mpg while delivering the performance, safety, and comfort of a conventional midsize sedan.

The green electronics design session will be held Feb. 11, from 8:30 a.m. to 12:00 noon. Dr. Lovins' talk will be held in the center's main auditorium Feb. 12, at 8:30 to 10:00 a.m. Readers should contact *Electronic Design's* main office (201) 393-6060 or write Lee Goldberg at : *leeg@class.org* for details on the conference or attending Dr. Lovins' lecture.

Lee Goldberg

TRUDEL TO FORM

JOHN D. TRUDEL
CONTRIBUTING EDITOR

Let me remind you of something: We create our own future. I believe that is true in many dimensions, but let's consider professional and technical matters. If you focus on fear and scarcity, you tend to get it. If you focus on abundance, you tend to get that, too.

(The notion extends further. A friend of mine, Mary Mannin Morrisey, has written a best-selling book, *Building Your Field of Dreams* about the subject.)

Many engineers are becoming excessively cynical, and I don't want to feed into that. Some fear that, like Dilbert, they can't have an impact. Some say that there is a conspiracy of power—from companies and the Government—that traps us. One reader warned that if I wrote more directly about the Patent Sell Out it would be "at the risk of being tossed down from my editorial pedestal and losing my corporate clients." It doesn't quite work that way. Sure, being entangled in fighting the Patent Sell Out has hurt my consulting practice, but only because it has consumed so much of my time.

Still, I *never* felt a need to choose sides between corporations and engineers. Why must I choose between serving the needs of my engineering readers and my corporate clients? By speaking truth about the dangers of the Patent Sell Out, I can serve them both.

Does not an attack on our constitutional right to profit from innovation harm both the corporate entity *and* the engineers and professionals tasked with new product development? I think so.

Much of the information that the media presents is false or superficial. PR and propaganda are largely about making your enemies (or customers) perceive the world the way you wish them to. The lobbyists, lawyers, and PR flacks cleverly framed the patent wars as the big dogs versus the small dogs. They also said it is a domestic issue.

Bruce Lehman's stated reason (in 1994) to destroy the most successful innovation system in the history of the world was to protect large firms from nasty little inventors who filed hidden "submarine patents," then sued and collected millions. In all the sound bites and hype, the fact that such submarines did not exist, and that no one knew how to make them exist or how they could benefit inventors now if they did exist, was ignored.

Lehman just tempted Tonya Harding-type managers and patent lawyers with the same things (greed and fear) that ambulance chasers and sleazy divorce lawyers use to scare clients and pocket more fees. And by framing it as a domestic squabble, Lehman even let Congress feel better about their practice of taking foreign "donations."

A different viewpoint often does wonders. Once you reject the charade and understand that the attack on the patent system was foreign-inspired and designed, a whole new reality unfolds. The pieces all snap into place.

In the Information Age, the key to wealth is innovation. Since that's what America has always done well, first and foremost we should safeguard our constitutional right to benefit from our innovations. The rest is just a simple matter of returning the cart and the horse to their proper juxtaposition.

If firms return innovation to their CTOs and engineers (instead of lawyers and lobbyists), a hopeful and prosperous future appears. It's a better future for both corporations and professionals, and a lot more fun than downsizing. There is even a place for clever firms that license or sell designs to their larger brothers. See? Isn't abundance better, and more calming, than fear?

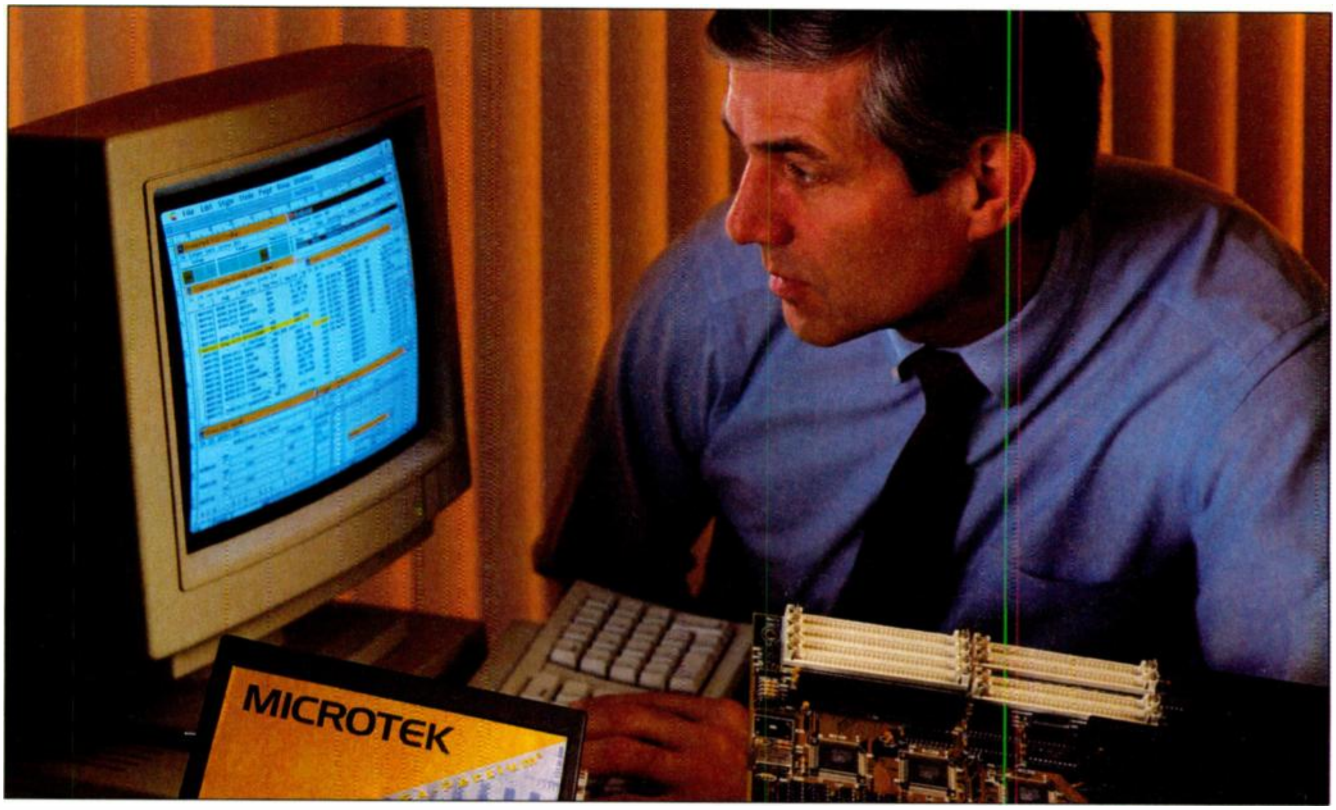
John D. Trudel, CMC, provides business innovation consulting to selected clients. Lectures, keynotes, and workshops also are available. He is the author of "High Tech with Low Risk." The Trudel Group, 33470 Chinook Pl., Scappoose, OR 97056; (503) 638-8644; fax (503) 543-6361; e-mail: jtrudel@gstis.net; Internet: http://www.trudelgroup.com.

FREE STUFF

Hewlett-Packard (HP) has published a new booklet that provides engineers with tips for enhancing power-product operation and using measurement capabilities. Available free of charge, "10 Practical Tips You Need to Know about Your Power Products" includes shortcuts and recommendations such as using remote sensing to compensate for load-lead effects; eliminating noise from low-level measurements, using constant-current load with foldback power supplies; and characterizing ac inrush current. To obtain a copy of the booklet, call HP at (800) 452-4844, ext. 5421; Internet: http://www.hp.com. Be sure to request Literature #5965-8239E.

International Rectifier's (IR) new CD-ROM gives designers a tool to review the company's product and specification details. Designers can gather all the information they need, including nearly 600 data sheets; a product catalog; technical papers, including application notes and design tips; listings of worldwide distributors; IR sales offices; and a free copy of Adobe Acrobat Reader. The free CD-ROM can be requested by contacting Carol Gajdos, IR Literature Department, fax (310) 252-7171; e-mail: cgajdos1@irf.com.

OZ Tek Inc. has published a "Guide to Selecting IC Package Test Products" to provide reference information for those involved in the quality assurance testing of standard and custom IC packages. The guide provides detailed information on test interface products such as sockets, receptacles, probes, adapters, burn-in interfaces, VLSI tester interfaces, plus a test configuration diagram showing how the various test products interconnect between the IC package under test and the test system. For a free copy of the reference guide, contact OZ Tek Inc., 3387 Investment Blvd., Hayward, CA 94545; (510) 782-2654; fax (510) 782-2656.



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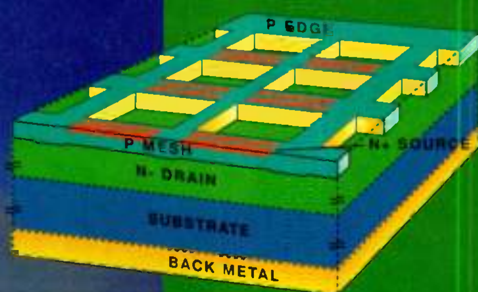
68360 • 68340 • 68F333 • 68332 • 68331 • 68330 • 68HC16 • 68328 • ColdFire

READER SERVICE 156

a smash hit

SGS-THOMSON introduces PowerMESH, the first significant improvement in PowerMOS technology in 20 years.

Lower $R_{DS(on)}$ – even with a smaller silicon area – means lower conduction losses. Heatsinks can now be smaller, and power supplies can be more compact.



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EYE ON ISO 9000

Amplifier Research (AR) has recently received ISO 9001 certification. The company designs, manufactures, and markets amplifiers, antennas, interference generators, and other products for RF and EMC testing. Contact AR, 160 School House Rd., Souderton, PA 18964-9990; (215) 723-8181; fax (215) 723-5688; Internet: http://www.ar-amps.com. **CIRCLE 485**

FabTech Inc. has achieved ISO 9001 registration. The company is a wafer foundry specializing in discrete technologies, EPI, and wafer polishing. Contact FabTech Inc., 777 N.W. Blue Parkway, Suite 350, Lee's Summit, MO 64086-5709; (816) 251-8800; fax (816) 251-8850. **CIRCLE 486**

Vitesse Semiconductor Corp. has received ISO 9001 certification. The company is a leading supplier of high-bandwidth communications integrated circuits. Contact Vitesse Semiconductor Corp., 741 Calle Plano, Camarillo, CA 93012; (805) 388-3700; fax (805) 987-5896; Internet: http://www.vitesse.com. **CIRCLE 487**

Andrew Corporation has received ISO 9001 registration. The facility designs and manufactures base station antennas, active wireless products, and associated accessories for worldwide shipment. Contact Andrew Corporation, 10500 W. 153rd St., Orland Park, IL 60462; (708) 349-3300; fax (708) 349-5222; Internet: http://www.andrew.com. **CIRCLE 488**

Phoenix International has achieved ISO 9001 certification. The company designs and manufactures electronic control, display, and sensor products for the OEM market. Contact Phoenix International, 1441 44th St., N.W., Fargo, ND 58102; (701) 282-9364; fax (701) 282=9365; Internet: http://www.phoeintl.com. **CIRCLE 489** **—MS**

JUST FOR THE KIDS

Never underestimate the power of a good toy. The Massachusetts Institute of Technology's Media Laboratory is living by that credo in its new Tools To Think With toys that are based on LEGO bricks. These tools are currently being showcased at Chicago's Museum of Science and Industry's LEGO Mindstorms learning center.

The new generation of toys is based on the idea that kids need to "play" with things, manipulate them in order to truly learn how things work. This idea system is in direct opposition to the current learning system in place in most schools in the U.S. that depends very heavily upon computers to feed the knowledge to the kids. The goal of the team at the Media Lab is to completely change the way in which learning takes place.

Back in 1984, MIT teamed with the LEGO Group, who funded the research, to connect LEGO blocks to desktop computers. Eventually, with the evolution toward smaller and faster electronics, MIT researchers learned how to embed tiny computers into the LEGO bricks, along with other toys. Now these toys have the capability to communicate with each other via these computers.

The Media Lab calls the computers "Crickets." Crickets are powered by 9-V batteries, and can control two motors and receive information from two sensors. Their communication is accomplished via an infrared system. The Cricket is the latest generation of Programmable Bricks from MIT.

The Programmable Brick, like the Cricket, is a portable computer embedded within a LEGO brick. It allows kids to build robots; create spaces that can be lit or dimmed when a person enters or exits a room; or make experiments that involve their physical selves, such as counting the number of steps they take in a day.

Some of the activities that MIT set up with the Crickets include networks of Crickets that are specifically positioned within an indoor environment so that they can collect and share data about room temperature variations, human traffic patterns, lighting, and other dynamic aspects of their environment.

Crickets are based on Microchip PIC 16C84 microprocessors. They are programmed in a dialect of the Logo programming language. Logo includes constructs such as 8-bit numeric operations, like if, global and local variables, motor and sensor primitives, a random number function, repeat and loop, timing functions, and a tone-playing function.

User programs are downloaded to the Cricket via the infrared communications system. Kids just press a button to run the downloaded programs. Crickets show their status (idle, running a program, etc.) with specific LEDs.

Cricket users also can design programs with an iconic version of Cricket Logo called Logo Blocks. These blocks can be dragged from a palette and assembled into a stack. Then they can be downloaded to the Cricket.

MIT's Cricket team is Fred Martin, Brian Silverman, Mitchel Resnick, Rick Borovoy, Kwin Kramer, and Robbie Berg. They do send a caveat, though, "at this stage, we do not plan to release the Cricket system to the public."

For more information, contact the Massachusettes Institute of Technology Room 5-111, Massachusettes Ave., Cambridge, MA 02139-4307; (619) 253-2700; e-mail: cricket-design@media.mit.edu.—**DS**

HOW DOES IT SOUND?

What would your next design be like if little hurdles like money, time, and resources suddenly ceased to exist? What if all your customers wanted out of your design was that it be the best it could possibly be—no matter what? And what if pigs could fly?

For most designers, all three of these occurrences dwell on the same plane of possibility—really close to zero. However, a lucky few have transcended these real-world limitations, have let loose the shackles of their constrained, oppressive, market-oriented existence, and have found refuge in that ethereal realm known as "High-End Audio Design." Out here, companies such as B&W Loudspeakers Limited, Worthing, UK, daily push sound reproduction to its limits. They search for the perfect speaker to help bring all of the thrill feelings and nuances of a live musical performance to every living space.

To this end, the company recently introduced the Nautilus System speakers. As much a product of art as they are engineering, the speakers use cutting-edge design theory and materials to reach a visual, as well as aural, milestone in speaker design.

The result of over a decade of research and development, the Nautilus System takes its design inspiration from two overriding principles: that a "lossy waveguide," or transmission line, holds the key to limiting the sound coloration caused by the radiation of the driver backwaves, and that greater sonic transparency can be achieved by limiting and gaining greater control over the range of frequencies over which a driver must operate.

The first of these principles has lead to the speaker's startling appearance. To remove unwanted cabinet resonance, the designers decided to put the driver out in front where it belongs, and then take the resonance away at the back through a tube (or waveguide) to infinity. This design required a total of four, exponentially tapered guides: one for the 25-mm aluminum-domed, high-frequency tweeter; one for each of the 50- and 100-mm mid-range drivers; and a curving, shell-shaped tube for the 300-mm bass driver. It is this shell-shaped that is the foundation for the speaker's unusual design. Because the bass driver's size is so large, it would take a tube up to 3-m long, with a total volume of 200 litres to dissipate the low-frequency back reflections. The typical closed-box bass cabinet was already ruled out due to a sonic mismatch between the mid-range and treble drivers.

Further research produced the Nautilus's curled-up, horn shape,

which takes its inspiration from the natural form of the ammonite nautilus. This design was found to perform as required, but still required a volume of less than 120 litres. The result is that each computer-designed, hand-made "cabinetless" speaker is a perfect example of form following function. Each uses a high-strength, durable resin, courtesy of Raceprep, well known for its work in materials for Formula One racing cars. The resin and takes up to nine days to make. A special paint and lacquer system, particularly designed for luxury-car manufacturers, and requiring 12 different applications, gives the speakers their rich, high-gloss finish.

To gain control over the drivers themselves, an external active crossover, based on fourth-order Bessel filtering, was used to generate the individual signals that would keep each driver comfortably within its operating range. Incorporating hand-made components, each network is individually fine-tuned to help achieve a flat frequency response for the speaker of ± 0.5 dB through the range of 25 Hz to 20 kHz. The speakers are rated for a -6-dB bandwidth of 10 Hz to 25 kHz.

But B&W's investment in time, money and effort doesn't just stop with the body and crossover. Every aspect of the speaker's design is the result of close scrutiny and engineering optimization. Magnetic fluid cooling prevents the metal-dome tweeters from overheating and affecting coil resistance. Kevlar driver cones give an extended frequency response and better damping. Cast-alloy frames provide durability and eliminate warping, and hollowed-out pole pieces in the tweeter and midrange allow rear-travelling sound waves to pass through the rare-earth magnets. In addition, the effective lack of a front baffle eliminates surface reflections that can distort the sound. When all is done, each system is individually tested and auditioned before leaving the factory.

To drive the speakers, B&W recommends the use of one stereo preamplifier and eight monobloc (or four stereo) power amplifiers per pair. Amplifiers of 100 W or more are recommended, with 500 W being optimum for the low-frequency drive unit.

While the litany of technical achievements are impressive, the whole is worth more than the sum of its parts. At a time when electronic designers are being crushed by time-to-market and cost pressures, it is those lucky few that are given free rein to max out their technical and artistic potential. The Nautilus System is the result of that, and consequently, is relegated to the chosen few who can afford its hefty $35,000 price tag.

Patrick Mannion

While developers have certainly not abandoned Unix, there has been a major movement toward Windows 95 and especially toward Windows NT as the development platform of choice. PCs have finally developed the power to rival Unix-based workstations at very competitive prices. Windows supports a huge selection of other software such as word processors, databases, and spreadsheets that engineers as well as other members of a business organization use in their work.

Beyond that, however, Windows has a number of built-in mechanisms, such as dynamic data exchange and Active X containers that make it easy to integrate tools from different vendors, and provide richly integrated visual work environments. Several embedded OS vendors, such as Accelerated Technology, have leveraged off Microsoft's own IDE, called Developer Studio and integrated a sub-environment called POWERplant Embedded Development Environment (EDE). The EDE gives access to cross-compilers and debuggers as well as to a simulator for the Nucleus real-time OS (RTOS). Developers can code and debug a good portion of their applications within the familiar Developer Studio environment before cross-compiling and downloading the code to the target system. Any other third-party tools that can be used under Developer Studio also are available to the embedded designer.

Several other embedded OS vendors have devoted significant resources to providing integrated development environments that accommodate their OSs and the tools they offer. They also feature the ability to integrate third-party tools. Integrated Systems has recently introduced pRISM+ to accommodate its pSOSystem. The pSOSystem itself is a richly modular OS environment built around the pSOS+ RTOS. pRISM+ is built around the common object request broker architecture (CORBA), which is an object-oriented communication mechanism that lets any tool written to its standards communicate with any other compliant object in the system. Third-party tools that are written to the CORBA standard and use Integrated Systems' published application programming interface (API) can work seamlessly within pRISM+.

Wind River Systems has developed an IDE, called Tornado, that uses dynamic link libraries (DLLs) for communication between host-based development tools and embedded target systems, and for reading different object module formats for debugging. Third-party and customer tools can interface to Tornado through its published API. Once a tool is adapted to Tornado, it can talk to any target that has a DLL connection plug-in.

In a similar approach, Microtec offers an XRAY integration kit for its widely used XRAY debugger. The debugger has a core that can accept DLLs for different processor architectures and different real-time OSs. In addition, a tool-specific DLL can interface XRAY to target-specific tool connections such as in-circuit emulators, ROM monitors, simulators, or background debug mode (BDM) ports. At the higher level, XRAY has an API that integrates it with Microtec's MasterWorks integrated device electronics (IDE), and hence to other tools integrated at the IDE level.

A number of RTOS offerings, such as Chorus, Enea OSE, and Eyring, take advantage of the GNU compilers and debuggers that are actively supported by Cygnus Solutions. While Cygnus does not supply a real-time OS, it is a major

Companies mentioned in this article, but not included in the table

Cygnus Solutions
19937 Landings Dr.
Mountain View, CA 94043
(415) 903-1474
http://www.cygnus.com
CIRCLE 530

Nematron
5849 Interface Dr.
Ann Arbor, MI 48103
(313) 994-1591
http://www.nematron.com
CIRCLE 531

Spyglass
1240 East Diehl Rd.
Naperville, IL 60563
(630) 245-6512
http://www.spyglass.com
CIRCLE 532

TABLE 1B: AVAILABLE EMBEDDED OPERATING SYSTEMS (COMPANIES A THROUGH F)

Company	OS	DOS-compatible file system	Intertask synchronization	Remote procedure calls	Remote debugging	ICE support	Modular	Networking support	Java support	File management	Object oriented
Accelerated Technology	Nucleas PLUS	Yes	Yes	No	No	No	Yes	Yes	Yes	Yes	Yes
Byte-BOS Integrated Systems	ByteBOS Multitasking OS	No	Yes	No	Yes	No	Yes	Yes	No	No	Yes
Chorus Systems	Chorus Jazza r1	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	Chorus ClassiX r3.1	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
CMX Co.	CMX-RTX	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes	No
Embedded System Products	RTXC	Yes	Yes	No	No	Yes	Yes	Yes	No	No	No
Enea OSE Systems	OSE	Yes	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes	No
Eyring Corp.	PDOS-pro	Yes	Yes	No	No	No	Yes	No	No	Yes	No
	PDOS	No	Yes	No	Yes	No	Yes	Yes	No	Yes	No
Forth Inc.	pF/X	No	No	No	No	No	Yes	No	No	Yes	No

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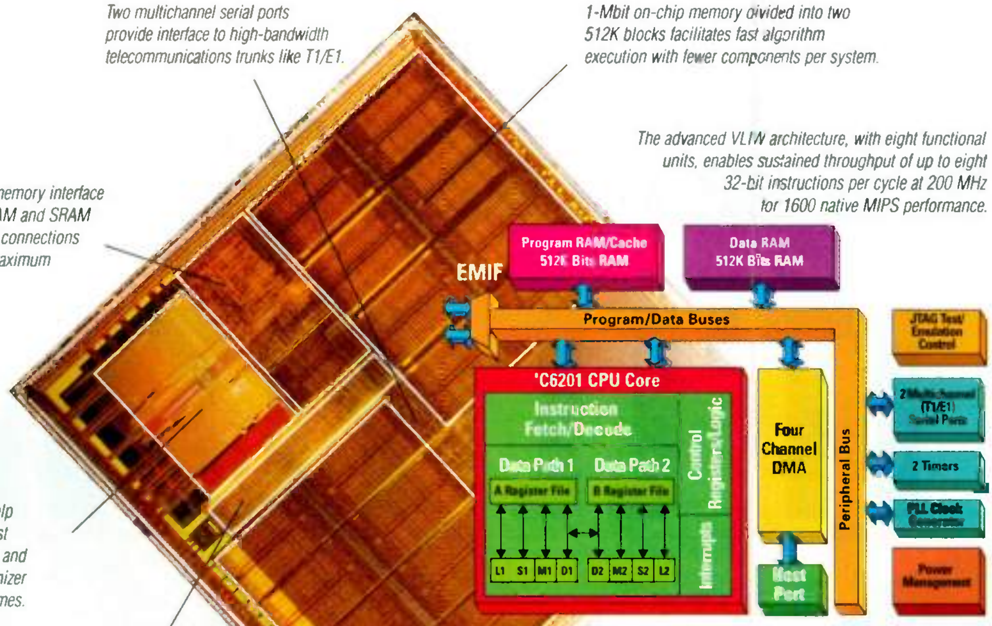

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DCT (8x8)	1.13 µs
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Dot product (N = 100)	0.29 µs
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FIR filter (24 tap, 64 outputs)	3.9 µs

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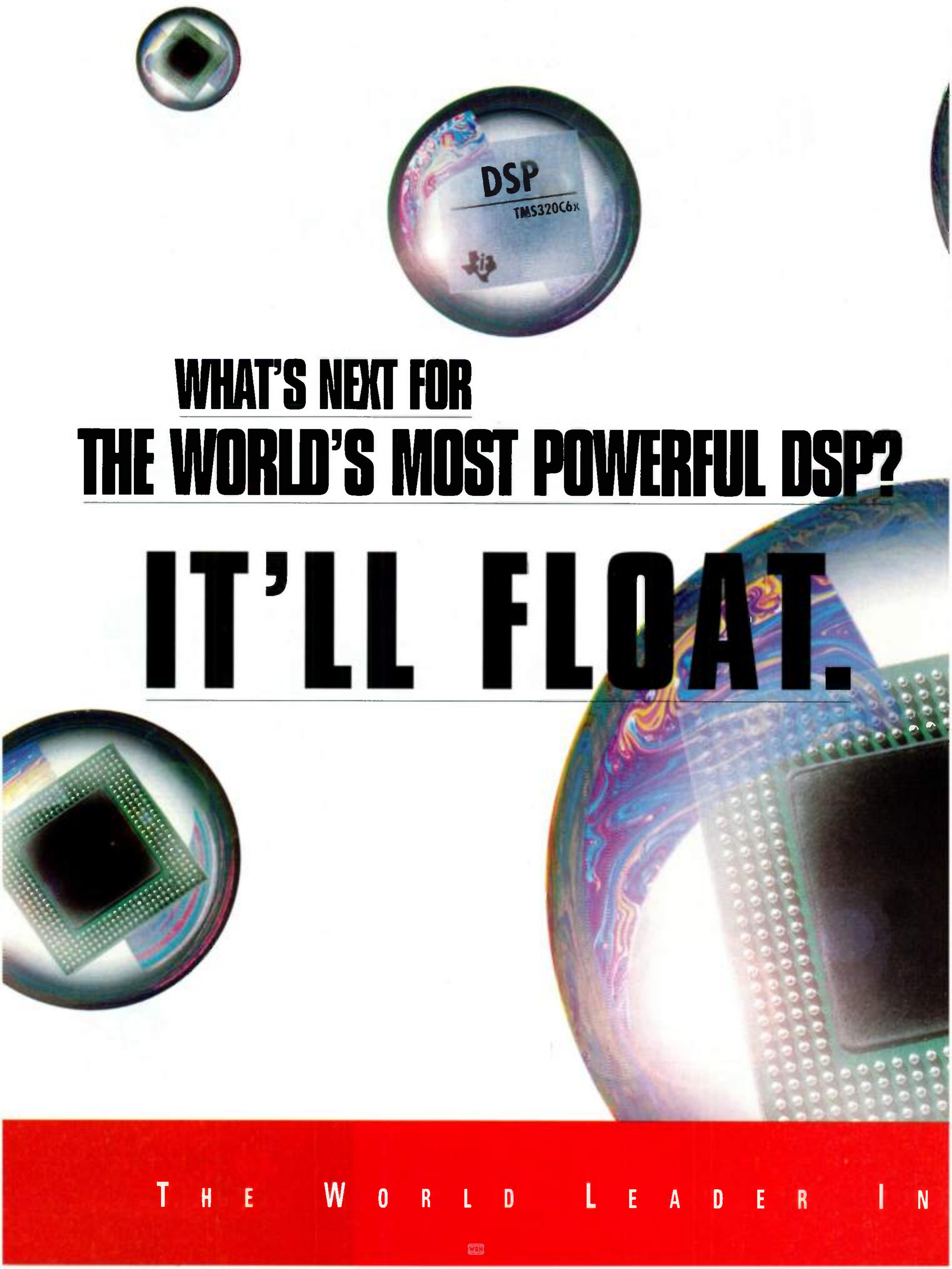

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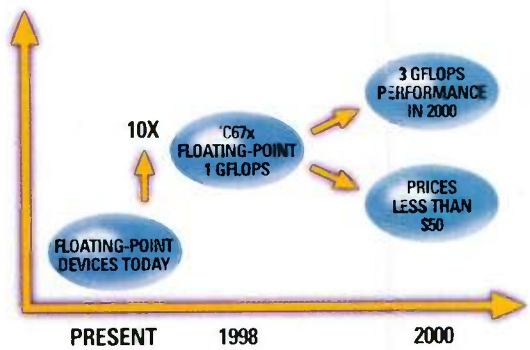

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DSP SOLUTIONS

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TABLE 1C: AVAILABLE EMBEDDED OPERATING SYSTEMS (COMPANIES A THROUGH F)

Company	OS	POSIX-compliant	Remote monitoring	Remote task creation	Kernel-aware debugger	PC-DOS/PC-Windows 95/PC-WindowsNT	Unix (flavor)	Kernel-only price	Development environment price	Royalties	Source code available
Accelerated Technology	Nucleus PLUS	No	No	No	Yes	Yes/Yes/Yes	SunOS, Solaris	$7,500-$12,500	Call	No	Yes
Byte-BOS Integrated Systems	ByteBOS Multitasking OS	No	No	No	No	Yes/Yes/Yes	All flavors	Call	----	No	Yes
Chorus Systems	Chorus Jazz r1	Yes	Yes	Yes	Yes	No/No/Yes	UnixWare, Linux, SunOS, HP-UX	----	$15k per seat	Yes	Yes
	Chorus ClassiX r3.1	Yes	Yes	Yes	Yes	Yes	Linux, Solaris SunOS, HP-UX	----	$11k per seat	Yes	Yes
CMX Co.	CMX-RTX	No	Yes	Yes	Yes	Yes/Yes/Yes	----	$1500	Included	No	Yes
Embedded System Products	RTXC	No	No	No	No	Yes/Yes/Yes	----	----	----	No	Yes
Enea OSE Systems	OSE	Yes	Yes	Yes	Yes	No/Yes/Yes	Solaris2	$8000	From $6000	Yes	Yes
Eyring Corp.	PDOS-pro	No	Yes	Yes	Yes	Yes/Yes/Yes	Not available	Call	Call	Call	Call
	PDOS	No	Yes	Yes	Yes	/Yes/Yes/No	SunOS	$700-$995	$1500-$6000	Yes	Yes
Forth Inc.	pF/X	No	No	No	Yes	Yes/Yes/Yes	----	Included	$1,995-$2,195	No	Yes

source of compilers and other tools for Unix-hosted embedded development.

APIs And Standards

Given the wide selection of embedded OSs, it follows that there is a crowd of different APIs. There also is a yearning among customers for some sort of standardization that would make porting code easier, and reduce the learning curve when moving to a different OS. Motorola, for example, has settled on RTEK for its 16- and 32-bit microcontrollers, although these processors are supported by a wide array of other OSs.

There has been a long and agonizing effort to define a standard for real-time extensions to POSIX, the common Unix API. Part of that debate has seen Unix programmers who wanted whatever real-time OS that emerged to be an actual real-time Unix that would run all POSIX-compliant code. The other side of the real-time POSIX struggle has been carried by those who wanted Unix compatibility, but were more interested in good, efficient, real-time features and performance. Companies such as Lynx Real-Time Systems have steadily kept the goal of a true POSIX API in sight. Lynx also has created a development environment called PosixWorks for development of LynxOS real-time embedded applications. PosixWorks runs on Unix hosts, and includes a multithreaded debugger and performance analyzer as well as support for the GNU tool chain.

IEEE Standard 1003.1 now incorporates real-time extensions that support threads, mutexes, signals, semaphores, queues, clocks, timers, and message passing. Recently, Microtec announced a new version of its VRTX RTOS, VRTX 5.0, that supports all the POSIX real-time mechanisms. The RTOS is compliant in the sense that any application written to it will run on a full Unix/POSIX system, but not all Unix applications will run under VRTX 5.0. The seekers of a real-time Unix seem finally to be settling into the idea of a real-time subset of Unix.

Efforts toward standardizing some embedded and/or real-time version of Win32 are at a far-less-developed stage. Win32 in its Windows CE incarnation is an embedded OS, but it does not have the deterministic mechanisms for real-time performance. Real-time extensions to Win32 would allow a designer to include the ability to run off-the-shelf Windows applications alongside embedded real-time code, or to select subsets of Win32 for specific products and applications.

However, since Microsoft has not shown any sign of defining real-time extensions to Win32, several companies have taken it upon themselves to do so. Phar Lap has implemented Win32 calls for its TNT Embedded Toolkit, and added a set of calls to support real-time mechanisms in the kernel. Three other companies, VenturCom, RadiSys and Nematron, have created real-time extensions to Windows NT. The problem, of course, is that each company's set of API extensions is unique—its method of achieving real-time performance is such that there can be no portability of Win32 real-time applications among them.

For example, the INtime product from RadiSys takes advantage of the Intel architecture's hardware-based memory protection, and treats the entire Windows NT OS as a single, low-priority task under the INtime RTOS. All Windows NT programs run as they normally would, but real-time tasks always have priority. In addition, the RTOS runs in its own protected memory space so that real-time tasks and drivers can't overwrite NT memory space, and NT kernel-level routines can't interfere with the real-time code.

Instead of adding a real-time kernel, VenturComm has modified the hardware abstraction layer (HAL) of Win-

TABLE 2A: AVAILABLE EMBEDDED OPERATING SYSTEMS (COMPANIES G through M)

Company	OS	Processor supported	Development environment	ROMable	Dynamic priority scheduling	Fixed priority scheduling	Protected memory	Shared memory	Multiprocessing	Internet support	Graphics support
Geoworks, 960 Atlantic Ave., Alameda, CA 95401 (510) 814-1660 CIRCLE 544	GEOS	x86, MIPS, portable to any 32-bit CPU	Microsoft Visual C/C++ on WindowsNT Java toolkit	Yes	Yes	No	Yes	Yes	No	Yes	Yes
Green Hills Software, 30 W. Sola St., Santa Barbara, CA 93101 ((805) 965-6044 CIRCLE 545	VelOSity	PowerPC, 68k, MIPS, x86, SH, V800, Alpha	Green Hills MULTI	Yes	Yes	Yes	Yes	Yes	Yes	No	No
	Integrity	PowerPC, 68k, MIPS, x86, SH, V800, Alpha	Green Hills MULTI	Yes	Yes	Yes	Yes	Yes	Yes	No	No
Industrial Programming, 100 Jericho Quadrangle, Jericho, NY 11753 (516)938-6600 CIRCLE 546	MTOS	x86, 68k, 683xx, Coldfire, PowerPC, R3000/4000	C/C++ compilers from Metaware, Watcom, Microtec, GNU, Diab Data, and Tasking; Debuggers from SSI, SDS, Microtec, XRAY, and Tasking	Yes	Yes	No	Yes	Yes	Yes	No	Yes
Integrated Systems, 201 Moffett Park Dr., Sunnyvale, CA 94089 (408) 542-1500 CIRCLE 547	pSOSSystem	68k, PowerPC, Coldfire, MIPS, i960, x86, ARM	pRISM+ development environment, BetterState, SystemBuild, and Xmath	Yes	Yes	Yes	No	Yes	Yes	Yes	Yes
JMI Software Systems, P.O.Box 481, 904 Shebly Ln., Spring House, PA 19477 (215) 628-0846 CIRCLE 548	C Executive	x86, 80186, 68k, 683xx, PowerPC, R3000/4000/5000, ARM, i960, SH, PA-RISC, 810/30, TMS320C30/31, Transputer	Variety of compilers for appropriate processors	Yes	Yes	Yes	Yes	Yes	No	Yes	No
Kadak Products, 206-1847 W. Broadway Ave., Vancouver, BC V6J1Y5 Canada, (604) 734-2796 CIRCLE 549	AMX	x86, 68k, 683xx, PowerPC, ARM, Z80, 80960, R3000, 29k	Depends on processor	Yes	Yes	Yes	No	No	No	Yes	Yes
Lynx Real-Time Systems, 2239 Samaritan Dr., San Jose, CA 95124 (408) 879-3900 CIRCLE 550	LynxOS	68030/40/60, PowerPC, MPC821/860, x86, microSparc, microSparcII	POSIXworks	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Microsoft, One Microsoft Way, Redmond, WA 98052-6399 (425) 882-8080 CIRCLE 551	Windows CE	ElanSC400, SH3, 486DX, Pentium, PowerPC 821, VR4101/02/4300, PR312500, TX3912	Windows CE embedded Toolkit (Visual C++5.0), Windows CE Toolkit (Visual Basic 5.0, C++ 5.0, & Visual J++ 1.1)	Yes	Yes	No	Yes	Yes	No	Yes	Yes
Microtec, 880 Ridder Park Dr., San Jose, CA 95131 (408) 487-7000 CIRCLE 552	VRTXsa	68k, PowerPC, x86	Spectra and X-RAY Pro	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	VRTXmc	68k, ARM	X-RAY Masterworks	Yes	No	Yes	No	Yes	No	No	No
Microware Systems, 1500 NW 118 St., Des Moines, IA 50325 (515) 223-800 CIRCLE 553	OS-9	x86, PowerPC, 68k, ARM	FasTrack and CodeWarrior for OS-9	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Motorola, 6501 William Cannon Dr., Austin, TX 78735 (800) 262-5486 CIRCLE 554	RTEK	68HC11/12/16, CPU32, MPC500/800	Cosmic, Introl, Hiware, SDS, Diab Data, and Microtec	Yes	Yes	No	No	Yes	No	No	No

TABLE 2B: AVAILABLE EMBEDDED OPERATING SYSTEMS (COMPANIES G THROUGH M)

Company	OS	DOS-compatble file system	Intertask synchro-nization	Remote procedure calls	Remote debugging	ICE support	Modular	Networkng support	Java support	File manage-ment	Object oriented
Geoworks	GEOS	Yes	Yes	No	Yes	No	Yes	No	Yes	Yes	Yes
Green Hills Software	VelOSity	No	Yes	No	Yes	No	Yes	Yes	No	No	No
	Integrity	No	Yes	No	Yes	No	Yes	Yes	No	No	No
Industrial Program-ming	MTOS	Yes	Yes	No	Yes	No	Yes	Yes	No	Yes	Yes
Integrated Systems	pSOSystem	Yes	Yes	Yes	Yes	No	Yes	Yes	Yes	Yes	Yes
JMI Software	C Executive	Yes	Yes	No	Yes	No	Yes	Yes	No	Yes	No
Kadak Products	AMX	Yes	Yes	No	No	Yes	Yes	Yes	No	No	No
Lynx Real-Time Systems	LynxOS	No	Yes	Yes	Yes	No	Yes	Yes	Yes	Yes	No
Microsoft Corp.	Windows CE	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No
Microtec	VRTXsa	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes	No
	VRTXmc	No	Yes	No	Yes	Yes	No	No	No	No	No
Microware Systems	OS-9	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Motorola	RTEK	No	Yes	No	No	Yes	Yes	No	No	No	No

TABLE 2C: AVAILABLE EMBEDDED OPERATING SYSTEMS (COMPANIES G THROUGH M)

Company	OS	POSIX compliant	Remote monitoring	Remote task creation	Kernel-aware debugger	PC-DOS/PC-Windows 95/PC-Win-dowsNT	Unix (flavor)	Kernel-only price	Develop-ment-environ-ment price	Royalties	Source code available
Geoworks	GEOS	No	No	No	No	No/No/Yes	----	----	----	Yes	No
Green Hills Software	VelOSity	No	Yes	No	Yes	No/Yes/Yes	----	Included with MULTI	Call	No	Yes
	Integrity	No	Yes	No	Yes	NoYes/Yes	----	Inlcuded with MULTI	Call	No	Yes
Industrial Program-ming	MTOS	No	No	No	Yes	Yes/Yes/Yes	SunOS, Solarix, HP-UX, AIX	$5000-$15,000	$5000-$15,000	Yes	----
Integrated Systems	pSOSystem	No	No	No	Yes	No/Yes/Yes	HP-UX, SunOS, Solaris	----	Starts at $7650	Yes	Some
JMI Software	C Executive	No	No	No	Yes	Yes/Yes/Yes	All flavors	$2500	Compiler+: is $1500 for kernel-aware option	No	Yes
Kadak Products	AMX	No	No	No	Yes	Yes/Yes/Yes	Portable	$1900-$7900	----	No	Yes
Lynx Real-Time Systems	LynxOS	Yes	Yes	Yes	Yes	No/No/No	LynxOS (POSIX)	----	$7000 per seat	Yes	Yes
Microsoft Corp.	Windows CE	No	No	Yes	Yes	No/Yes/Yes	----	Volume-based	Per toolkit	Yes	Yes
Microtec	VRTXsa	No	Yes	Yes	Yes	No/Yes/Yes	SunOS, Solarix, HP-UX	----	PC: $6750-$8910; Unix:: $7000-$12,545	Yes	Yes
	VRTXmc	No	No	No	Yes	No/Yes/Yes	SunOS	$1000	$4650	Yes	Yes
Microware Systems	OS-9	No	Yes	Yes	Yes	No/Yes/Yes	Solaris, SunOS	Call	$899-$3750	Yes	Yes
Motorola	RTEK	No	No	No	Yes	No/Yes/Yes	----	----	----	Yes	Yes

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TABLE 3A: AVAILABLE EMBEDDED OPERATING SYSTEMS (COMPANIES O through W)

Company	OS	Processor supported	Development environment	ROMable	Dynamic priority sched-uling	Fixed priority sched-uling	Pro tected memory	Shared memory	Multi proces-sing	Internet support	Graphics support
On Time, 88 Christian Ave., Setawket, NY 11733 (516) 689-6654 CIRCLE 555	RTKernel/ RTKer-nel-32	80x86	Borland, Microsoft, Watcom C, Borland Pascal/Delphi, and RTTartget-32	Yes	Yes	Yes	Yes	Yes	No	Yes	Yes
Phar Lap Software 60 Aberdeen Ave., Cambridge, MA 02138 (617) 661-1510 CIRCLE 556	TNT Embedded ToolSuite	x86, Pentium Pro, Pentium II SC300/400, NS486	Visual C++, Developer's Studio IDE, and Borland C++	Yes	Yes	No	Yes	No	No	Yes	Yes
Precise Software Technologies, 1740 Massachusetts Ave., Boxboro, MA 01719 (508) 264-4413 CIRCLE 557	Precise/ MQX	68k, MPC8xx, PowerPC, TMS32C3x-6x, R3000/4000, ARM, DSP56k, Coldfire, x86	SDS SingleStep, CrossView, Visual C++, CrossCode, TI, Code Composer, and InterTools	Yes	Yes	Yes	Yes	Yes	No	Yes	No
	Precise/ MQX+m	68k, MPC8xx, PowerPC, TMS32C3x-6x, R3000/4000, ARM, DSP56k, Coldfire, x86	SDS SingleStep, CrossView, Visual C++, CrossCode, TI, Code Composer, and InterTools	Yes	Yes	Yes	Yes	Yes	No	Yes	No
Psion Software PLC, 17-19 Harcourt St., London W1H 1DT England +44 171 2081800 CIRCLE 558	EPOC 32	ARM710, x86	Microsfot Visual C++, and GNU tools	Yes	Yes	No	Yes	No	No	Yes	Yes
QNX Software Systems Ltd., 175 Terrence Matthews Crescent, Kanata, Ontario K2M 1W8 Canada (613) 591-0931 CIRCLE 559	QNX	x86 and clones	Watcom C/C++ development tools	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Radisys, 5445 NE Dawson Creek Dr., Hillsboro, OR 97124 (503) 615-1100 CIRCLE 560	iRMX	486 and higher	Microsoft C/C++, SoftScope debugger and proprietary OMF-compliant tools	No	No	Yes	Yes	Yes	No	No	No
Spectron Microsystems, 315 Bollay Dr., Santa Barbara, CA 93117 (805) 968-5100 CIRCLE 561	SPOX and SPOXMP	TMS320C3x-6x, SHARC21060/61/62, Motorola 56156/66, NEC7716/17, Pentium	Integrated with compilers, linkers, debuggers, emulators and assemblers from DSP manufacturers	Yes	Yes	Yes	Yes	Yes	No	No	No
	IA-SPOX	Pentium	----	No	Yes	Yes	No	Yes	Yes	No	No
Tasking Inc., 333 Elm St., Dedham, MA 02026 (617) 320-9400 CIRCLE 562	Precise/ MQX	68k, PowerPC, TMS32C3x-6x, R3000/4000, ARM, DSP56k, Coldfire, x86	SDS SingleStep, CrossView, Visual C+, CrossCode, TI, and Code Composer	Yes	Yes	Yes	Yes	Yes	No	Yes	No
US Software, 7175 NW Evergreen Pkwy., Ste. 100, Hillsboro, OR 97124 (503) 844-6614 CIRCLE 563	SuperTask!	x86, 68k, ARM, PowerPC, MIPS, SPARC, SH, 80960, 80196, Z80, 64180, 68HC11/16, 8051	ANSI C compilers	Yes	Yes	Yes	No	Yes	No	Yes	No
Wind River Systems, 1010 Atlantic Ave., Alameda, CA 94501 (510) 748-4100 CIRCLE 564	VxWorks	x86, CPU32, 68k, 683xx, PowerPC, SPARC, ARM, SH, Coldfire, i960, R3000/4000, C16x, PA-RISC	Tornado Development Environment	Yes	Yes	No	No	Yes	Yes	Yes	Yes

dows NT, a piece of the code that was meant to be accessible to OEMs, to adapt NT to various hardware environments. The HAL modifications pass selected interrupts past the NT mechanism to a scheduler DLL written by VenturComm. The DLL sends them to the kernel that then runs high-priority interrupts ahead of other NT interrupts. The scheduler DLL is part of a real-time API (RTAPI), a set of proprietary calls that can be linked to Windows NT using VenturComm's Component Integrator tool. Since these real-time approaches to Windows NT are so different from most other embedded OSs, they were not included in the accompanying table.

Graphics And User Interfaces

The huge potential market in consumer products is what drives the attraction of an embedded form of Windows. Consumer products like cellular telephones, personal digital assistants (PDAs), handheld PCs, and networked information appliances will all require some form of graphical user interface, and Windows comes most frequently to mind. However, such devices do not need a full desktop version of Windows for their more specialized functions.

To address the needs of specialized handheld products, Windows CE has been modularized. It is now possible to include selected functional modules as well as a subset of the GUI. This puts Windows CE on a more level playing field with other embedded OSs that have similar capabilities. Some like OS/9 from Microware, QNX from QNX Software, and Psion Software have their own modular window-like GUIs. Psion's EPOC32 and the Geos OS from Geoworks are aimed specifically at handheld and portable devices that use a GUI. As long as such OSs can support data exchange with desktop Windows applications, they stand a good chance of competing with Windows CE on the basis of size, speed, and communications features as well as GUI functionality.

Java And The Internet

Actually, all an embedded OS needs to provide a window-like GUI is to support a level of Java that includes the abstract windowing toolkit (AWT) classes. The industry has not yet completely figured out how Java will ultimately fit into the big picture of embedded systems—especially those with real-time requirements. One clear advantage is that it can provide a GUI for embedded devices connected to the Internet or an intranet. The same GUI implemented as an applet on the embedded device can run with the same look and feel on any computer (Unix, PC, or Mac) that has a Java-enabled browser.

Such devices and their embedded OSs usually need to support two sets of code: the Java virtual machine and other code such as drivers and real-time algorithms. These other types of code actually operate the device and are mostly written in C or C++. This situation represents a bit of a dilemma. On the one hand, Java offers portability to a degree never before achieved by a programming language—especially valuable for open communicating devices. On the other hand, it is slow in the interpreted mode, and adding it to embedded real-time devices means that you have to support two sets of codes. Compiling Java to native machine code would give up cross-platform portability, but increase speed. It still would not result in deterministic behavior due to Java's automatic garbage-collection mechanism.

Still, several companies are licensing Java and producing native compilers, notably Cygnus Solutions, Mountain

TABLE 3B: AVAILABLE EMBEDDED OPERATING SYSTEMS (COMPANIES O THROUGH W)

Company	OS	DOS-compatble file system	Intertask synchro-nization	Remote procedure calls	Remote debugging	ICE support	Modular	Networkng support	Java support	File manage-ment	Object oriented
On Time	RTKernel/ RTKernel-32	Yes	Yes	No	Yes	Yes	Yes	Yes	No	Yes	Yes
Phar Lap Software	TNT Embedded ToolSuite	Yes	Yes	No	Yes	Yes	Yes	Yes	No	No	No
Precise Software Technologies	Precise/ MQX	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes	Yes
	Precise/ MQX+m	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes	Yes
Psion Software PLC	EPOC 32	Yes	Yes	Yes	Yes	No	Yes	Yes	Yes	Yes	Yes
QNX Software Systems Ltd.	QNX	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Radisys	iRMX	Yes	Yes	Yes	Yes	No	Yes	Yes	No	Yes	No
Spectron Micro-systems	SPOX and SPOXMP	Yes	Yes	No	Yes	Yes	Yes	No	No	No	No
	IA-SPOX	Yes	Yes	Yes	Yes	Yes	Yes	No	No	No	Yes
Tasking Inc.	Precise/ MQX	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes	Yes
US Software	SuperTask!	Yes	Yes	No	Yes	Yes	Yes	Yes	No	Yes	No
Wind River Systems	VxWorks	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

TABLE 3C: AVAILABLE EMBEDDED OPERATING SYSTEMS (COMPANIES O THROUGH W)

Company	OS	POSIX compliant	Remote monitoring	Remote task creation	Kernel-aware debugger	PC DOS/PC-Windows 95/PC-WindowsNT	Unix (flavor)	Kernel-only price	Development-environment price	Royalties	Source code available
On Time	RTKernel/ RTKernel-32	No	No	No	Yes	Yes/Yes/Yes	----	$550-$1950	RTTarget: $1700	No	Yes
Phar Lap Software	TNT Embedded ToolSuite	No	Yes	No	Yes	No/Yes/Yes	----	----	$4995	Yes	Yes
Precise Software Technologies	Precise/ MQX	No	Yes	No	Yes	Yes/Yes/Yes	SunOS, Solaris	$5800-$12,000	$9500-$25,000	No	Yes
	Precise/ MQX™	No	Yes	No	Yes	Yes/Yes/Yes	SunOS, Solaris	$10,000-$15,000	$14,000-$30,000	No	Yes
Psion Software PLC	EPOC 32	No	No	Yes	No	No/Yes/Yes	----	----	SDK included	Yes	----
QNX Software Systems Ltd.	QNX	Yes	Yes	Yes	Yes	No/Yes/Yes	QNX	$65	$845	Yes	Yes
Radisys	iRMX	No	No	No	Yes	Yes/Yes/Yes	----	Call	Call	Yes	No
Spectron Micro-systems	SPOX and SPOXMP	No	Yes	Yes	Yes	No/Yes/Yes	----	----	$4995 per seat	Yes	No
	IA-SPOX	No	No	Yes	Yes	Yes/Yes/Yes	----	----	----	Yes	No
Tasking Inc.	Precise/ MQX	No	Yes	No	Yes	Yes/Yes/Yes	SunOS, Solaris	$5800-$12,000	$9500-$25,000	No	Yes
US Software	SuperTask!	No	Yes	No	Yes	Yes/Yes/Yes	----	----	—	No	Yes
Wind River Systems	VxWorks	Yes	Yes	Yes	Yes	No/Yes/Yes	SunOS, Solaris, HP-UX	----	$16,000 first seat	Yes	Yes

View, Calif., and Microtec. Microtec has recently announced a suite of PersonalJava native compilers and a run-time system that work with its VRTX RTOS. The company also has announced a Java version of its XRAY debugger. XRAY, as noted above, can be adapted to work with a wide range of other embedded OSs and processors.

URL Addresses

Accelerated Technology:
www.atinucleus.com
Byte-BOS Integrated Systems:
www.bytebos.com
Chorus Systems:
www.chorus.com
CMX Co.
www.cmx.com
Embedded Systems Products
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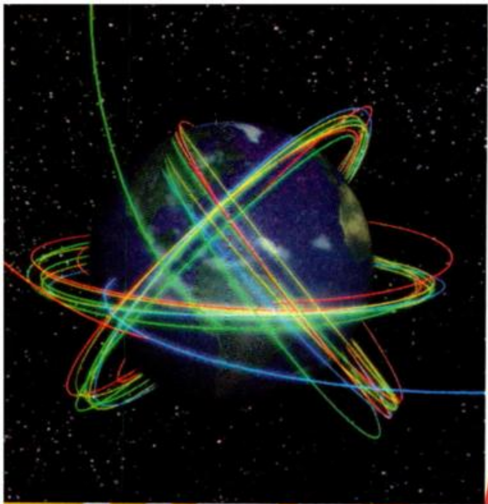

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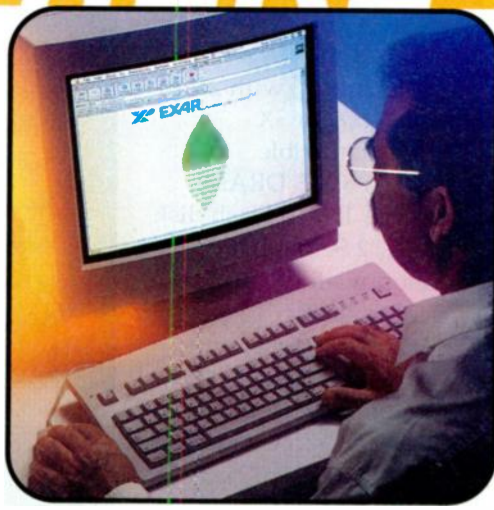

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Cygnus is extending its GNUPro Toolkit, used with many embedded OSs, to create a Java implementation that will work with a scalable run-time environment. The run time will only link in the run-time services actually required by the application. Cygnus also claims to be able to implement its services in a deterministic fashion that meets the demands of real-time applications. This would mean that Cygnus has found a way to implement deterministic garbage collection, one of the things that has been a major obstacle to the use of Java in real-time systems.

Java support is only one element needed to make embedded OSs. Many devices can be accessed and controlled without the need for a Java virtual machine or applets. By embedding an HTTP server along with the OS and run-time code, you can set up HTML pages that reside on the embedded device and can be accessed by any web browser. Using a compact RTOS and embedded HTTP server with several HTML pages, it is possible to implement a web-enabled device in about 2 Mbytes. The TCP/IP protocols and data buffering gobble up a good deal of that memory space. Phar Lap has demonstrated a small weather station that gives temperature and wind speed and direction for the HTTP server, the RTOS, the application code, and the communications protocols. There is an additional 0.5 Mbytes for HTML pages. The amount needed for HTML pages is, of course, dependent on the particular application. Phar Lap estimates that adding web capability to an existing embedded device would take between 300 kbytes and 500 kbytes of additional memory.

Some types of devices, such as personal digital assistants (PDAs), set top boxes, and Internet-enabled telephones, also can make use of embedded browser technology. As with GUIs, this often requires considerably less than the multimegabyte browsers made for desktop systems. Spyglass supplies a set of modular and scaleable Internet technologies that are targeted for use with embedded OSs. These tools include Device Mosaic, a scaleable and embeddable browser; and Microserver, a thin HTTP server that can scale down to 10 kbytes. Using Device Mosaic and Microserver, QNX Software was able to combine web capability with its POSIX-compliant RTOS and its Photon microGUI in less than 1.44 Mbytes of memory.

Embedded OSs are being harnessed for ever larger and more complex jobs. As the range of applications grows, the need for more and better tools, enhanced networking and communications capability, and the push for more standard interfaces will increase. There will never be a single standard API. For embedded OSs, the best we can expect will be a reduced number. A stronger set of standards will appear in the vast industry that is growing up around embedded OSs. This includes development tools, IDEs, programming languages, and object-oriented technologies necessary to handle the size and complexity of future embedded systems.

PRODUCT FEATURE

Object-Pattern Model Libraries Help Push Projects To The Starting Gate

Whether it's Rembrandt staring at a blank canvas or an engineer confronting a blank screen, getting started on a new project when there are no preexisting elements can be a time-consuming and frustrating experience. That also translates to costly experience. Normally, of course, engineers don't develop from scratch. They use modules of code from a previous project, modify existing corporate code assets, or get started with commercial class libraries. However, the "blank sheet syndrome" has been showing up more often in organizations that have recently shifted to an object-oriented methodology, because they start without previous work that fits the new methods.

Project Technology recognized this scenario when using model-based development—certain application areas have similar modeling problems repeated multiple times. Starting with a very general application model and then modifying it to suit the needs of a specific application can help reduce the "blank sheet syndrome" without having previously developed application code to draw from.

Project Technology has started to supply a series of what it calls ProjectStart model libraries that can be imported to its BridgePoint development tool. BridgePoint supports the Shlaer-Mellor object-oriented analysis (OOA) methodology that builds a model of the application and then translates it into a specific application platform (with specific hardware, OS, etc.).

ProjectStart model libraries are packages of object patterns that have repeated application within a specific industry, such as telecommunications. Each pattern is an executable graphical model consisting of 4 to 12 objects. A developer can pull up a model library and study it to determine its applicability to his or her particular application. Once a suitable pattern is selected, the developer can begin customizing and adding onto it to meet specific needs. At the very least, the developer begins the project by staring at *something* on the screen instead of nothing.

Beyond that, however, the generic pattern representation of the model libraries stimulates a more uniform way of constructing applications within an organization, which helps reduce the complexities of maintenance. Project Technology claims that the domain expertise of the people who developed the original patterns is an added advantage in helping a project get started on the right track. In addition, they offer numerous examples for less-experienced developers. When used with the BridgePoint tools, developers can use the tools' dynamic and static testing facilities to catch customization errors. The libraries come with test suites that give developers a start in how to customize the patterns supplied and to test the changes they make to them.

As an example of how generic modeling can be applied, take the problem of reserving a printer from a pool of printers on a multiuser system. The problem is similar to reserving a drive for a disk in an automated retrieval system, or selecting an outgoing circuit in a telephone system. The problem can be distilled to that of *competition for an unspecified instance* from a pool of instances.

This happens to be one of the model patterns supplied in the Telecom I model library. The ProjectStart model of this general problem includes an object information model, state models for each active object, and executable action language for each state of each state model. Each pattern comes with a user's guide containing examples of possible customizations.

Coupled with the announcement of the ProjectStart model libraries is an announcement of support for the Universal Modeling Language (UML) as a notation for translation-based development. UML originally evolved out of the Booch, Rumbaugh, Jacobson methodologies, which today comprise the major alternative to the Shlaer-Mellor approach.

The Booch, Rumbaugh, Jacobson approach supports elaboration-based software development. In this case, you build a graphical representation of the functionality of the code, generate some code, refine it, go back to the diagram and so on until the project is complete. The translation approach defines models, translation rules, and the translation engine separately, letting developers work on different domains of the system separately. This means that a given application can be ported to a different operating-system environment by using a different set of translation rules, rather than by rewriting the application. The adoption of UML will not end the rivalry between these two camps, but it will give them a common tool for graphical representation.

The first ProjectStart model library, called Telecom I,is targeted at the telecommunications industry. It contains nine commonly used modeling patterns, such as routing, routing with selection, and routing with least cost. In addition, telephone support is available. The Telecom I model library is available now and is priced at $3000 for three users. An instrumentation-modeling library will be available in the first quarter of 1998.

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Tool Provides Source-Level Trace Analysis for Code and Data

If code is defined as a means of moving and manipulating data within a system, then debugging requires that we know what the code is doing to the data. Traditional source-level debuggers can show this when you stop the system at a breakpoint or an error. However, finding the causes of bugs involves a tedious "break/analyze/rerun" cycle. In-circuit emulators used with traditional debuggers usually present useful data for correlating execution trace with assembly-level information, but correlating actual source code and source-level variables has been difficult.

Applied Microsystems has introduced a source-level trace analysis tool *(continued on page 94)*

(continued from page 92)
named CodeTRACE, which provides side-by-side views of real-time trace data and the corresponding source code and source-level variables. CodeTRACE works with the trace data collected by the Applied Microsystems CodeICE 68340/360 and SuperTAP 302 emulators. The trace data is collected in a file and downloaded along with the object file for use by the analysis tool.

The tool uses a proprietary disassembler technology along with the OMF file to correlate between trace and source. Using a proprietary inference engine, it's able to follow values stored in registers, track when they are modified, and correlate them with source-level variable names. CodeTRACE also has a search capability that lets you search back through an execution trace and find all instances where a given variable changed. The ability to capture a run lets you move forward and backward and observe the code's behavior as it occurred in real time. This can be very useful in today's complex applications where an error and its root cause may be widely separated in time.

For example, discovering that a crash was caused by some erroneous data value is the easy part. Finding out what caused that variable to have the wrong value can be quite involved. It might come from some subroutine that ran quite a bit earlier and which itself only executes under certain conditions. That subroutine, in turn, could have received some previous wrong data which caused it to generate the value that wound up in the subsequent variable. Then you have to find out how that happened.

There also are times where a variable may change as a result of register operations. While the fact that there was some register operation—a move or add between two registers—would show up on the bus, the resulting value would not and could not be captured by traditional trace. The CodeTRACE inference engine can keep track of changes to register values and correlate them with the current value of source variables. In addition, it keeps track of internal changes made by compiler optimizations or changes to variables inside the processor's cache.

You can set up a watch point window and assign almost any number of source variables to it. As you scroll back and forth through the trace, you can see where the variables change. There's a "backout" function that lets you click on a button and step backward in time from an error to the statement that caused that error. When you get back to an offending statement that has, for example, a wrong value, you can search until you find the first time that value was written to a variable. This is displayed in a statement execution window.

In addition to the current support for CodeICE 68340/360 and SuperTAP 302 emulators, CodeTRACE will expand to other emulator-specific tool sets in 1998. It runs on WindowsNT and SunOS hosts, and is priced at $2000.

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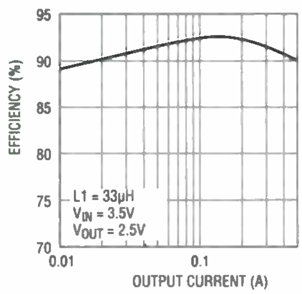
NEW!

The LTC1626 is the industry's first step-down DC/DC converter that operates over the entire voltage range of a single Lithium Ion cell. Its 2.5V to 7V supply range allows the LTC1626 to maximize battery life while maintaining excellent output regulation. An internal P-channel MOSFET allows load currents up to 600mA with up to 95% efficiency and 100% duty cycle operation allows extremely low dropout voltage. The LTC1626 incorporates Burst Mode™ operation to optimize efficiency at light loads, consuming just 160µA in standby and less than 1µA in shutdown.



Features:

- 2.5V to 7V supply range
- Low Q current: 160µA in standby, 5µA max in shutdown
- 100% duty cycle for low dropout operation

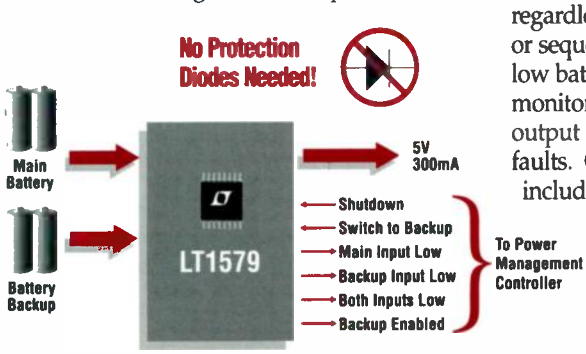
Circle No. 212

LTC1626: $3.50 ea. for 1K-piece Qty.

Dual Input UPS Low Dropout Regulator

Seamless Switchover From Mulitple Inputs

Operating from two independent power inputs up to 20V, the LT1579 produces an uninterruptible output voltage for loads up to 300mA with only 0.5V dropout. Automatic or logic-controlled input switching insures that the LT1579 maintains output regulation regardless of input voltages or sequencing. Integrated low battery comparators monitor both inputs and output flags warn of system faults. Other features include reverse battery protection, current limiting and reverse current protection.



Features:

- 0.5V dropout at 300mA load
- 3.5V to 20V supply range
- Control inputs and status flags interface to external logic or microcontroller
- 50µA quiescent current, 7µA in shutdown
- Adjustable and fixed 3V, 3.3V and 5V outputs

Circle No. 214

LTC1579: $4.15 ea. for 1K-piece Qty

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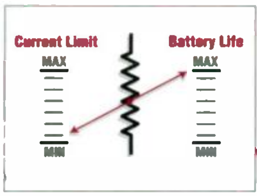
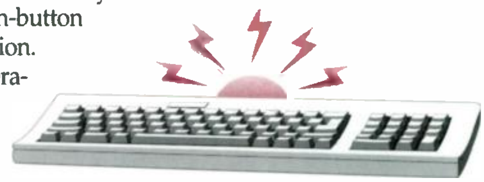
10µA I_Q Step-Down DC/DC Converter

The LTC1474 and LTC1475 are high efficiency step-down DC/DC converters with only 10µA of standby current, and precision programmable peak switch current limit (up to 400mA). The switch current limit peak can be reduced to match the needs of a low output current application. This improves system operating time from a battery supply, particularly Alkaline cells. The internal low-battery comparator is functional during shutdown.



Programmable Peak Switch Current For Extended Battery Life

The LTC1475 version easily implements push-button ON/OFF operation. Industrial temperature range versions are available.



4-cell to 3.3V Wireless Keyboard

Features:

- Very low standby current: 10µA typ
- 6µA shutdown current
- Adjustable and fixed 3.3V or 5V versions
- Programmable peak switch current limit
- Wide V_{IN} range: 3V to 18V
- High Efficiency: Over 92% possible
- Low battery detector active in shutdown
- Low dropout operation: 100% duty cycle
- Short-circuit protected
- 8-lead MSOP and SO packages
- $3.40 ea. for 1K-piece Qty.

Circle No. 215

33µA I_Q Micropower Boost Regulator

The LT1316 micropower boost switching regulator has a very low 33µA quiescent current and sports a programmable peak switch current limit adjustable from 25mA to 500mA. The shutdown current is just 3µA and the internal low battery detector is active in shutdown. The peak current limit is programmable using a low-cost external resistor. The benefit is that the peak current drawn from the battery can be set to match the needs of the load, saving precious battery energy. The LT1316 has a 30V switch voltage rating permitting high output voltages. These features make the LT1316 an excellent solution for portable battery-powered devices needing boost or SEPIC configurations and the longest battery lifetime.

Features

- 33µA quiescent current
- 3µA shutdown current
- Programmable peak switch current limit
- V_{IN} as low as 1.5V
- Low Battery Detector is active in shutdown
- 8-lead MSOP or SO packages
- 30V Switch voltage
- Adjustable output voltage

Circle No. 216

LTC1316: $2.45 ea. for 1K-piece Qty.

Regulated Charge Pump DC/DC Converters Saves Space and Cost

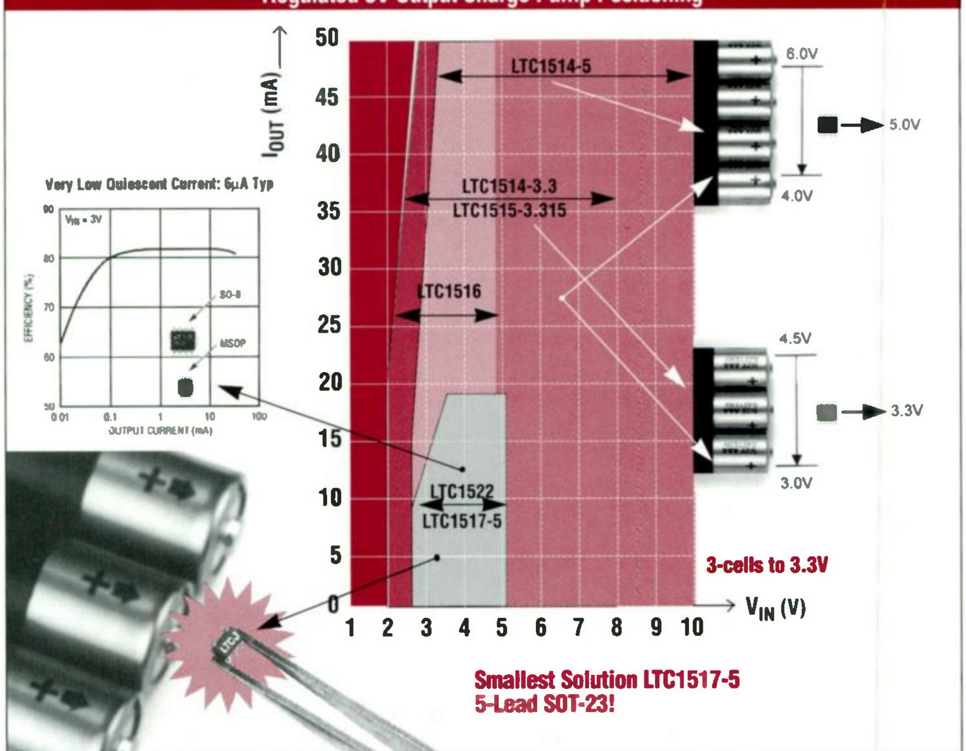
NEW!

LTC introduces a new family of switched capacitor DC/DC converters with regulated positive output voltage. These new devices allow small PCB footprint solutions with no inductors required! All these devices can boost the input voltage to a regulated 5V output. The LTC1514 and LTC1515 devices can step-up or step-down the input voltage to a regulated 5V or 3.3V. These devices include short circuit and thermal protection and can withstand a continuous short of the output to ground. All are micropower devices and when shut down the load is disconnected from the input. These devices are well suited to 2-, 3-, and 4-cell battery applications.

Circle No. 217

V_{IN} Range	Step Down	Step Up	V_{OUT}	Output Current	Quiescent I_Q/ Shutdown I_Q	Package	Significant Features	Device
2V to 8V 2.7V to 10V	✓	✓	3.3V, 5V	≤ 50mA	60µA / 10µA	SO-8	Low Battery Detector	LTC1514-3.3 LTC1514-5
2V to 8V 2V to 8V 2.7V to 10V	✓	✓	3V/5V, 3.3V/5V, ADJ	≤ 50mA	60µA / 1µA	SO-8	Power On Reset	LTC1515-315 LTC1515-3.315 LTC1515
2V to 5V		✓	5V	≤ 50mA	12µA / 1µA	SO-8	Short Circuit Protection	LTC1516
2.7V to 5V		✓	5V	≤ 20mA	6µA / NA	**SOT-23**	Smallest Size	LTC1517-5
2.7V to 5V		✓	5V	≤ 20mA	6µA / 1µA	**MSOP**, SO-8	Small MSOP	LTC1522

Regulated 5V Output Charge Pump Positioning



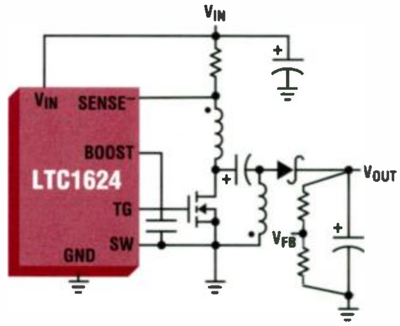
4-Cells to 5V: LTC1514 and LTC1515 are the smallest step-up/ step down solutions!

Universal N-Channel Switching Regulator

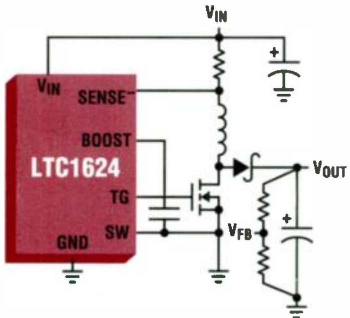
Cool!

The LTC1624 Can Be Used in All Standard DC/DC Converter Topologies

The LTC1624 is a current mode switching regulator that drives an external N-channel power MOSFET in all standard switching configurations including boost, step-down, buck-boost (SEPIC), inverting and flyback. Its fixed 200kHz operating frequency and 8-lead SO package minimize the total solution size for space limited applications. Operation from 3.5V to 36V allows the LTC1624 to be used in a variety of applications. Burst Mode™ operation provides high efficiency at low load currents and 95% duty cycle provides low dropout voltage for increased operating life in battery powered systems.



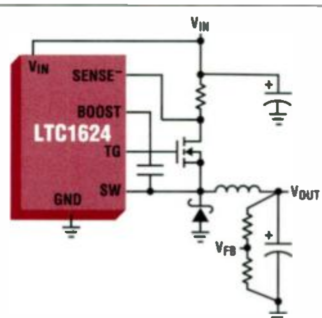
SEPIC Converter

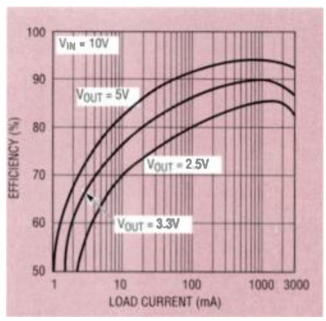


Boost Converter

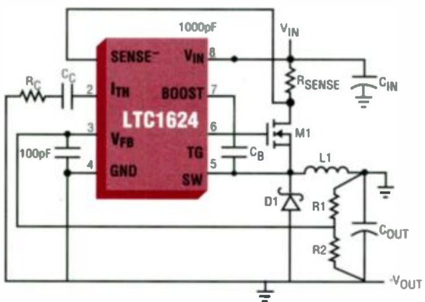
Circle No. 218

Features:
- Wide V_{IN} range: 3.5V to 36V
- Wide V_{OUT} range: 1.2V to 30V in step-down mode
- Low dropout operation: 95% duty cycle
- ±1% 1.19V reference
- Small SO-8 package

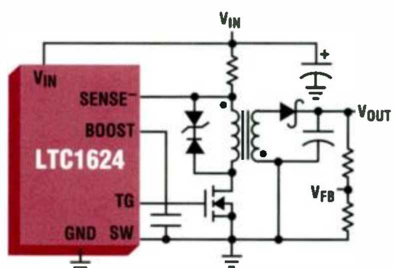




3 Amp Step-Down DC/DC Converter



Positive-to-Negative Converter



Flyback Converter

LTC1624: $3.50 ea. for 1K-piece Qty.

LINEAR TECHNOLOGY

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Single Cell to 3.3V at 75mA in MSOP Package

The LT1307 is a micropower 600kHz current-mode PWM boost converter that allows the use of all ceramic capacitors and a small 10µH inductor for a very small footprint solution. Its 1V minimum input voltage and low operating quiescent current make the LT1307 an excellent choice for battery-powered applications. The LT1307 is great for hand-held devices using 1, 2, or 3 cells to generate supplies for 3.3V or 5V logic, 12V flash memory or 28V LCD bias.

Features:
- V_{IN} as low as 1V
- 50µA quiescent current
- 3µA shutdown current
- 600mA internal switch
- 600kHz PWM with Burst Mode™
- Low Battery comparator
- Uses all ceramic capacitors
- 8-lead MSOP, SO and PDIP packages
- LT1307B is constant frequency at light load

Receive Pager

Cost-effective Solution for 1-,2-,and 3-cell Applications

Circle No. 219

LT1307: $2.05 ea. for 1K-piece Qty.

Single Cell to 3.3V at 300mA in SO-8 Package

The LT1308 micropower, fixed frequency boost DC/DC converter has a 2A switch in an SO-8 package and can generate 3.3V at 300mA from a single NiCd battery. Its adjustable boost output voltage can also be set up to 28V. The LT1308 features a power saving Burst Mode™ to maintain high efficiency over a broad 100µA to 300mA load range. The LT1308 is well suited for pulsed high current applications such as two-way pagers, PC Card modems, and digital cameras, as well as GPS receivers and battery backup supplies.

Features:
- Pin-compatible with LT1307 for simple power upgrades
- V_{IN} as low as 1V
- 100µA Quiescent current
- 3µA Shutdown current
- 600kHz current-mode PWM
- Low Battery Comparator
- 2A switch in an SO-8 package

Circle No. 220


2-Way Pager

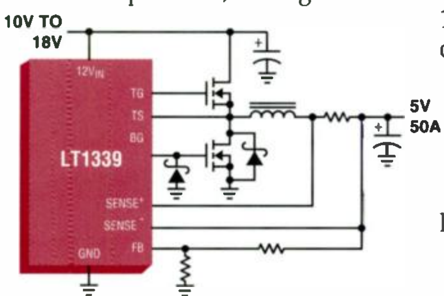
Smallest Footprint High Power Boost Solution Available


PC Card Modem

LT1308: $3.45 ea. for 1K-piece Qty.

Synchronous Buck Controller Delivers Module Power Without the Cost

The LT1339 is an easy to use current mode switching regulator controller that can deliver the power of a DC/DC converter "brick" without the high cost. Its robust N-channel synchronous MOSFET drivers can handle up to 10,000pF gate capacitance, making this device perfect for mainframe computer and network server applications requiring load currents up to 50A. Programmable average current limiting allows accurate control of the DC output current independent of inductor ripple, and the operating frequency can be synchronized up to 150kHz for precise control of switching harmonics. Other features include user-adjustable slope compensation, soft start and undervoltage lockout.



Also Available: LT1680: Boost Controller for high voltage, high current step-up applications

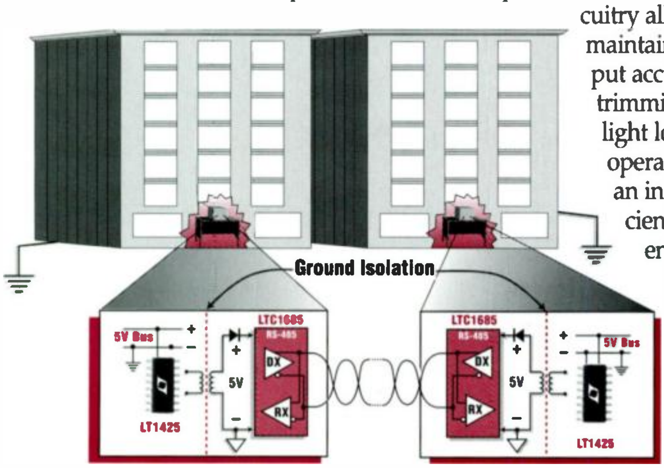
Features:
- High voltage: Operation up to 60V
- High current: N-channel synchronous drive handles up to 10,000pF
- Fixed frequency 150kHz operation, synchronizable
- Programmable average load current limiting
- 20-lead DIP and SO packages

Circle No. 221

LTC1339: $4.85 ea. for 1K-piece Qty.

Flyback Regulator Eliminates Optoisolators

The LT1425 is a monolithic flyback switching regulator that provides isolated output voltages without requiring a third winding or optoisolator. Advanced control circuitry allows the LT1425 to maintain ±2% typical output accuracy without user trimming, even at very light loads. A 275kHz operating frequency and an integrated high efficiency 1.25A switch enables the LT1425 to deliver output loads up to 6W without any external power devices.



Features:
- No transformer third winding or optoisolator required
- ±2% output accuracy without user trimming
- Resistor programmable output voltage
- Maintains output regulation at very light loads

Circle No. 222

LT1425: $2.90 for 1K-piece Qty.

Ultra Low Noise Switching Regulator

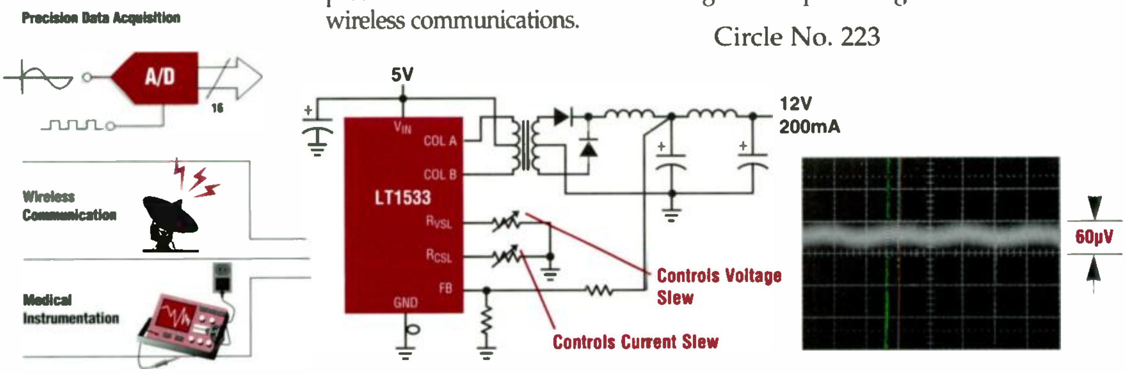
The LT1533 DC/DC converter produces less than 100µV output noise over a 100MHz bandwidth. The voltage and current slew rates of the internal power switches are user-adjustable, resulting in dramatically reduced conducted and radiated EMI – up to 40dB lower than most switchers. Finally, a switching regulator than can coexist with noise-sensitive applications such as precision instrumentation and wireless communications.

Features:
- Controlled voltage and current slew rates
- 20kHz to 250kHz fixed frequency operation, synchronizable
- Regulates positive and negative output voltages

Circle No. 223

Cool!

Up to 40dB Lower Conducted & Radiated EMI Than Most Switchers



LT1533: $4.95 ea. for 1K-piece Qty.

6A, 500kHz Switching Regulator Saves Space

The LT1370 is a high power current mode switching regulator that is ideal for space-limited applications. Its 500kHz operating frequency and low loss 6A/100mΩ internal switch allow the LT1370 to realize up to 90% efficiency using tiny external components. A 2.7V to 30V supply range permits it to be used in a variety of applications and it can be synchronized to an external clock source for improved management of switching harmonics. The LT1370 is available in 7-lead DD and TO-220 packages.

Features:
- Fixed Frequency 500kHz Operation
- Small inductor size: As low as 4.7µH
- Uses all surface mount components
- Wide input supply range: 2.7V to 30V
- Easy synchronization to external clock

500kHz Switching Regulator Reduces Size of DC/DC Conversion Circuits

BOOST SWITCHING REGULATORS

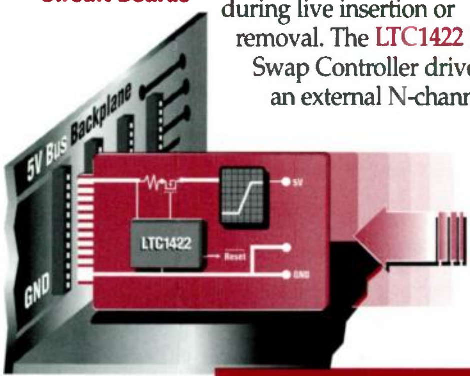
Switching Frequency (kHz)	Maximum Switch Current (A)						
	1.25 to1.5	2.5 to 3	4	5	6	7.5 to 8	10
40	LT1072	LT1071		LT1070			
60	LT1082		LT1271			LT1270	LT1270A
100	LT1172	LT1171	LT1269	LT1170			
150						LT1268	
250	LT1373						
500	LT1372	LT1371			LT1370	NEW!	
1MHz	LT1377						

Circle No. 224

LT1370: $6.15 ea. for 1K-piece Qty

Hot Swap Controller Allows Live Board Insertion

Simple Control for Hot Swapping Circuit Boards



Protect your board against system errors caused by power supply transients during live insertion or removal. The LTC1422 Hot Swap Controller drives an external N-channel MOSFET for a single supply from 2.7V to 12V and is flexible enough to handle -48V applications. Connection sense insures the board is properly seated before the supply ramps up and a supply monitor can be used to generate a system reset when the supply falls below a preset voltage. Ramp rates, reset threshold and current limit levels are all programmable, allowing maximum user control.

Features:

- Controls a single supply from 2.7V to 12V
- External N-channel MOSFET allows design flexibility
- Programmable ramp rates, reset threshold and current limit
- Small SO-8 package, requires few external components

Circle No. 225

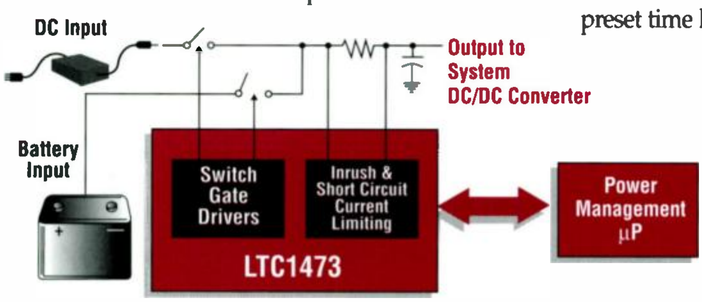
LTC1422: $2.75 ea. for 1K-piece Qty.

Smart Power Management for Dual Input Systems

Power Path Management for Systems with Multiple DC Sources

The LTC1473 PowerPath™ Controller provides a simple power management solution for systems that operate from multiple DC sources. It drives two sets of back-to-back N-channel MOSFET switches to route power from either source to the main system switching regulator without causing system resets. A unique 2-diode logic mode ensures correct system start-up regardless of the sequencing of the input sources and inrush current limiting ensures seamless operation during switch-over transitions. The LTC1473 also protects against system short circuits using a programmable timer to latch off the switches when the fault exceeds the preset time limit.

Also available: LTC1479 includes power management for two batteries, DC power source, charger and backup.



Features:

- All N-channel switching to reduce power losses and system cost
- Switches and isolates sources up to 30V
- Capacitor inrush and short circuit current limiting
- Small footprint: 16-lead narrow SSOP package

Circle No. 226

LTC1473: $3.55 ea. for 1K-piece Qty.

For more details, contact Linear Technology Corporation, 1630 McCarthy Blvd., Milpitas, CA 95035-7417, Web Site: www.linear-tech.com. (408) 432-1900. Fax: (408) 434-0507. For literature only: 1-800-4-LINEAR.

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LT/12/97

DSM Design Drives The Need For EDA Tool Accuracy

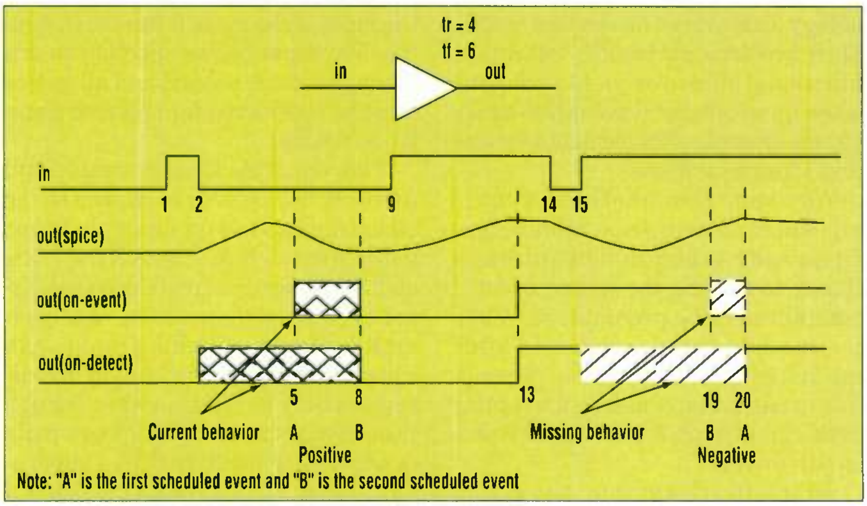
Changing Design Environments Requires Tighter Relationships Between EDA Tool Vendors, ASIC Vendors, And Tool Users.

STEVE WADSWORTH, American Microstructures Inc., 150 North 3rd St., Pocatello, Idaho 83201; (208) 234-9898, X3316; e-mail: wadswort@poci.amis.com.

In the ASIC industry, there's much discussion about design complexity, validation cycle time, tools, and overall design methodology. There are concerns that today's electronic design automation (EDA) tools cannot keep pace with the requirements placed upon them by growing design complexity. This gap is expected to widen further with each advancement in semiconductor technology that reduces feature size and allows for larger, faster, and more complex designs. Intellectual Property (IP), the Virtual Socket Interface (VSI), large megacells, cores, and a myriad of rapid design methodologies will only continue to put more pressure on these design tools.

Product life cycles and time-to-market are placing increased pressure on users to get designs done quickly. Design verification must be accurate since errors can cause delays and increase costs, causing the design to totally miss the market window. What's needed is a three-way partnership between users, ASIC vendors, and the EDA tool vendors. But the question is whether the EDA community is in sync with the leading technologies of today.

With system-on-a-chip and ASIC designs approaching 1 million gates, it is clear that the industry is not at rest. IP, VSI, and reusable logic will allow users to quickly put more complex functions together. But whether there are sufficient tools and methodologies in place to ensure successful designs and design verification is questionable. How well the industry provides these solutions will determine the overall success and growth potential of not only EDA tool vendors, but also ASIC vendors and tool users.



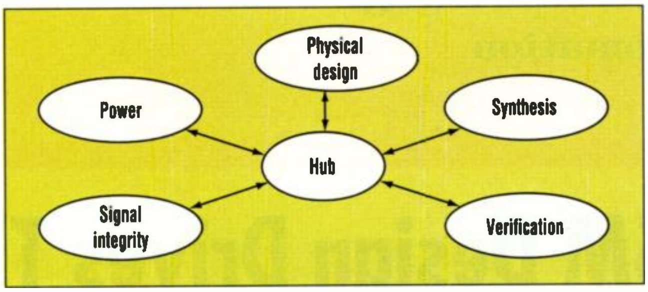
1. These timing examples show the results of narrow glitches being injected into a simple buffer. All delays are represented with simple values. The waveform includes the input, Spice, on-event, and on-detect representations of the output result. VITAL (and the latest Verilog standard) allows for both on-event and on-detect pulse propagation.

Design Styles

Design styles directly influence design methodology and tools. Design styles for digital circuits can be fully synchronous, asynchronous, or a mix of both. In this article, fully synchronous is defined as requiring all direct action signals such as clocks, sets, and resets, to originate at the pads.

Some consider fully synchronous to include only a single master clock, but even in designs with a single master clock, glitches can occur in decoded set or reset signals feeding sequential gates due to timing differences. This can result in potential circuit malfunctions that could cause manufacturing yield losses or even nonfunctional silicon. These types of designs are considered semi-synchronous.

Asynchronous designs usually have multiple clocks running various sections of logic or signals that can arrive at random intervals that are common in communication circuits. Most companies can dictate the design styles, especially if the types of circuits they develop lend themselves to a particular style.



2. At the present time, some standards committees and silicon vendors are proposing a common data model, shown here, in lieu of passing files between various point tools. This model would consist of a main "hub" to control the design steps and iterations.

It has long been considered that analog designs are difficult and that developing a digital design simply meant defining logic functions and making sure timing requirements are met. This is no longer the case, since digital designs are beginning to take on more analog characteristics. It is becoming more important to have a closer link between Spice and validation processes, especially with designs that are not fully synchronous. As long as designers develop asynchronous circuits and design complexities continues to rise, verification accuracy will continue to be a major industry focus.

Power consumption also is becoming important, especially in battery-operated applications. This is accomplished by lowering the supply voltage in addition to disabling certain portions of logic during operation. Both methods of power conservation can cause side effects and require accurate timing verification. Shrinking process technologies also can reduce noise immunity since narrow glitches can be detected and passed on by other logic functions. Wire interconnect, once considered an insignificant part of the overall delay, is now significant. While this new technology has enabled designers to build larger, faster, and more complex designs, it also has compounded the problem of design verification and physical design.

As designs continue to push performance, increase in complexity, and the use of deep submicron technologies, several technical issues continue to arise. The capabilities of all EDA tools are being pushed to the limit, making design verification challenging. With standardization of the two IEEE HDL languages (Verilog and VHDL), it is crucial to address the growing concerns for accuracy and capability. Other timing standards such as Standard Delay Format (SDF), and a new proposed Delay Calculator Language (DCL), also will assist in meeting the challenges of design verification. With the added focus on these standards, EDA vendors can put emphasis on value-added enhancements and not language semantics or simulator behavior. To get a deeper appreciation of these accuracy concerns, a more in-depth analysis of such issues as pulse filtering, signal skew, interconnect, delay selection, accurate delay modeling, and memory modeling is needed.

Pulse Filtering

Most simulators, including those compliant with VITAL and Verilog, allow for two different pulse-filtering modes: inertial and transport. The inertial mode, better suited to older technologies, filters out all input transitions smaller than the gate propagation value. As geometries continue to shrink, the transport delay mode has become more important. All pulses, no matter how short, are allowed to propagate to the device output, and many simulators allow the propagated pulse to contain an "X" state to indicate ambiguity in the signal value. This is important because during this region of uncertainty, the actual amplitude and duration of the signal is unclear and, depending on the technology, can cause the devices to fail. These problems can result in either nonfunctional silicon or yield problems when these glitches drive direct-action signals on sequential elements such as clocks, resets, and sets.

Any time that another event is scheduled on a device output before an already scheduled event has a chance to mature, the second event is considered to be preemptive. When the second event is scheduled after the first event, it is a positive preemptive event; when it is scheduled prior to the first event, it is a negative preemptive event.

In the first example, the rising event on the buffer at time 1 schedules a rising event on the output at time 5 (1 + 4) *(Fig. 1)*. At time 2, the narrow pulse closes, thus scheduling the output to return to its current state at time 8 (2 + 6). This is a positive preemptive event, since the second event is scheduled to occur after the first. If this signal were driving a clock input of a sequential device and the amplitude and duration met the criteria for minimum clock pulse width, there would be a potential for clocking in new unwanted data into the device. Even Spice simulations using a 0.8-µm process have indicated that narrow glitches around 80% of the required signal width can cause problems in sequential devices. The problem only gets worse with deep submicron technologies.

In the second example, the falling edge of the input signal at time 14 schedules the output to change at time 20 (14+6) *(Fig. 1, again)*. The rising edge at time 15 schedules the output to return back to its original high value at time 19 (15+4). Since the second event is scheduled prior to the first unmatured event, the new event is negative preemptive.

Unlike the positive preemptive pulse that is being caught by VITAL and Verilog simulators today, the negative preemptive pulses have been ignored. As shown by the Spice waveform, both events are real and are analog, not digital, in nature. Device delays given to the logic simulators ensure that the device output level is at the level to guarantee that it can effect the input of the gates it drives. In reality, this output begins affecting its driving gate much sooner, and all pulses must be considered for accurate simulation results.

This example is very simple and probably not as likely to happen as the situation caused on multiple input gates such as NANDs, ANDs, ORs, and NORs used to create decoded signal events. In these cases, nearly simultaneously switching inputs can cause the outputs to swing in one direction only to have another input's transition cause it to swing back to its original logic level. In fully synchronous circuits, this condition is not a significant problem, but in circuits that contain some asynchronous parts, it is a problem.

Due to the efforts of the Verilog

standards committees (OVI and IEEE 1364), the pulse problem has been corrected in Verilog. Some EDA companies have already released production versions of their simulators with these changes in early 1997. Several other EDA companies are in the midst of implementing the changes to bring their simulators into compliance. The VITAL standards committee is also finalizing the same changes for the 1998 reballot of the standard to ensure VITAL users have the same level of accuracy. As long as designers continue using design styles other than fully synchronous ones, it's imperative that standards committees address and implement changes to the language that will provide the required accuracy.

Negative Timing Constraints

Sequential devices not only have propagation delays, but certain timing relationships between various primary inputs, that must be met for stable operation. In some cases, these relationships can become negative, as in the case of hold times. This is the time that the data input must stay in a stable state from the active transition of the clock. Depending on how the device was built and modeled, this could become a critical relationship to maintain. Since digital simulators by nature do not maintain negative time, it is common practice to move all negative values to zero. Device performance and accuracy requirements have now required that simulators maintain this relationship and make the appropriate adjustments to all the remaining timing relationships.

Modeling And Skew

In older technologies, assumptions such as sharp signal edges, simple linear equations, and lumped wire interconnects were sufficient. With the signals looking more like "analog" sinusoidal waveforms and with the increasing role that interconnects are playing in the overall delay, it is important to have complex modeling equations for the delays.

What were once crude functional models of memory behavior have now become very accurate models of both the functionality and timing. Designs are using ever increasing numbers of memories to perform complex functions. Memories have gone from the simple synchronous single-port RAM to asynchronous, self-timed, multiport, ROMs, and EEPROMS. There is discussion of putting large embedded dynamic RAMs in logic devices. Memories once restricted to standard cell designs are now available for quick turn devices through embedded gate arrays. To ensure the entire design is functional, the memories must contain the same level of accuracy as any other cell in the library.

Signal skew has normally been associated with a design's master clocking scheme, but it also can include certain scan devices and other complex functions with special clock requirements. For this reason, signal skew is an integral part of the verification process.

Interconnects

In older technologies, a lumped capacitance for all device receivers on a net was considered sufficient. As technology has shrunk, wiring interconnect has become a significant portion of the overall delay. For deep submicron technologies, the time required for a signal to propagate from the signal driver to its receiver is at least as long as the device's internal switching time.

A new approach is required to accurately reflect the part that interconnect plays in the overall delay. One method being considered by ASIC vendors is called Elmore delay. This delay model takes into account the individual RC (resistance and capacitance) for each of the wiring segments. Parasitic extractors for 2-1/2D and 3D designs are also becoming necessary to provide accurate representation of the interconnect delay. Another issue facing verification accuracy is the multiple receiver/driver scenario. This is common within large clock or bus networks in which each receiver can be driven by multiple sources, and the actual device delays and individual interconnect delays are different depending on which driver(s) is/are active. Controlling interconnect delays also play an important role in balancing clock trees.

Delay Selection

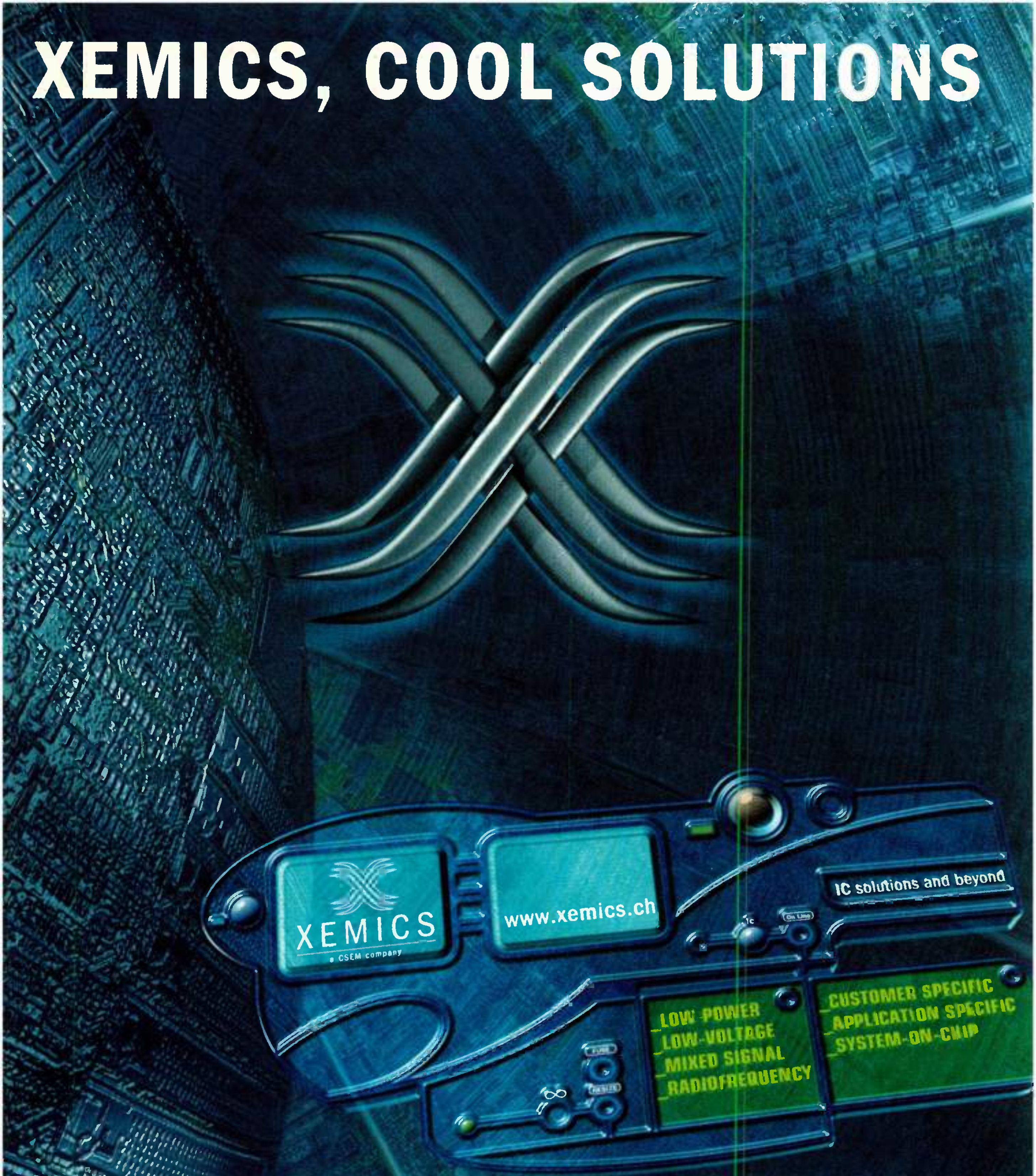
With devices getting faster, it is critical to select the appropriate delay. This is important when selecting the proper driver in a multiple receiver/driver situation, and in more complex functions when different timing arcs can cause an output to go to a particular state. When the longest path delay is scheduled first and subsequent inputs schedule the output to transition in the same direction, but at an earlier time, it is possible to get an erroneous early scheduled delay for the output transition. In some devices this would not become a problem, but in a more complex cells like an adder this can become a problem. Also, in more simple combinational gates like a 5-input NAND gate, the delay difference between the timing arc closest to the node and the one farthest from the node can be as much as 100%. In deep submicron designs where tens of picoseconds are counted, these differences in delay must be accounted for.

Verification Tools

With deep submicron designs, the front and back ends can no longer be decoupled. Finding a logic or timing problem during post-layout verification and going back to resynthesize the entire block effected may no longer be an option, since it may introduce additional problems with the respin. Incremental in-place optimization to minimize the iterations between the physical and logical design representations is considered a must. The tools must become better at predicting the final design characteristics at higher levels of abstraction to minimize these design iterations. Hardware/software co-verification also must become more mature for the system-on-a-chip concept to become a reality.

To achieve maximum productivity for developing large ASICs, designers must use logic-synthesis tools. The number of gates per day a designer can create with synthesis tools has been estimated to be at least 10X those designed using schematic capture. Whether a company elects to begin a development with synthesis at the behavioral level or at the RTL level depends on many factors such as the maturity of the relatively new behavioral compilers. Few floorplanners are available to end customers. What is available is usually offered by place-and-route tool vendors and are tightly coupled to only one router.

What this means is that the customer would be tied to one specific ASIC vendor or a group of vendors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that use that particular router. End customers will either be required to have floorplanners compatible with the ASIC vendor's place-and-route tools, or have a close relationship with the vendor such that the vendor will perform the early floorplanning of the device to ensure this tight front-to-back-end correlation.

As the challenges of deep submicron continue to mount, ASIC and EDA vendors have begun teaming up to develop tools. A tighter coupling between the physical and logical representations of the design at even the earliest stages of development is necessary for the end product to be developed successfully. Parasitic extraction, power analysis, and signal integrity are the result of some of these relationships. Having point tools alone may not be enough and a tight coupling between various tools is becoming increasingly necessary *(Fig. 2)*.

Developers of large ASICs are realizing that iterative cycles between pre- and post-synthesis as well as synthesis to physical design can be very costly and time consuming, with the potential of nonconvergence toward the target performance being high. Rather than doing a total re-spin through synthesis each time, in-place optimization is essential for controlling these design iterations. Whether this can be accomplished with a central data model or better ways of passing files has yet to be determined.

Logic Verification

Cycle-based simulators (CBS) are being touted as next-generation verification tools because of their superior performance over event-based simulators. There are some trade-offs, however, that must be made when using these tools. CBSs make the assumption that all timing in the circuit is met and only a functional verification is required. When CBSs are used, static timing verifiers also must be used to ensure that proper timing is met.

These new tools may require design style changes since only fully synchronous designs can be completely validated on a CBS, and not all synthesized designs are compatible with these simulators. EDA vendors and end-users who understand the whole picture recognize these limitations and caution the users on when and how to use cycle simulators. Used properly, they provide users with much faster verification cycles at little or no risk to design integrity, especially in the beginning of the design verification cycle.

According to several ASIC vendors, the percentage of fully synchronous designs they receive from the merchant market is less than 10%. About 80% of them are considered mostly synchronous, but for various reasons fall short of fitting into this elite group. The numbers for ASIC vendors, in which most designs were internal, were much higher since synchronous designs were mandated by the company. Most are still relying on accuracy achieved from commercial event-based (timing) simulators.

Unlike event-based simulators that have a minimum of 4 or 5 states to define the various logic values, most cycle-based simulators have only two states, "1" and "0," to boost performance. This can compromise simulation verification results, especially during the initialization phase, since the beginning states cannot take on the "X" or "U" value. Therefore, it may be unclear if any design flaws existed that could have prevented it from coming out of initialization or if such timing problems as glitches, bus contention, or floating buses, exist in the design.

Power compiler tools gate the clocks to conserve switching current in various portions of the logic that are not needed at a particular time. If not handled properly, this also can cause problems in a design that were otherwise considered synchronous. Since this seems to be the most widely accepted method of power conservation, simulation verification accuracy must be taken into account.

Designers must adopt new methodologies to capitalize on the benefits of cycle-based simulators. This methodology shift will not happen in the foreseeable future. As a result, giving attention to Spice-like accuracy in digital simulators remains important. Hardware accelerator and emulator companies and vendors of fast event-based simulators, such as Cadence, Avant!, Viewlogic, Mentor, and Model Technology, are banking on the fact that most designers are not going to—or may not be able to—change their design styles to fully synchronous ones, and thus will require fast event-based simulators.

Vendors of hardware emulators and hardware accelerators build special-purpose hardware that can achieve 10X to 100X performance at system and ASIC verification levels, yet maintain event-based accuracy. The demand has increased for these high-performance hardware and software solutions, a good indication that the requirement for event-simulation accuracy is alive and well. The design community must change design styles for the paradigm shift to the cycle-based/static timing verification approach to be successful.

Unlike event-based timing simulators, static timing tools do not require a set of stimulus to provide an indication of the circuit's timing. They do require the design to be fully synchronous for the results to be accurate. The purpose of these tools is to ensure that all device propagation activity occurs within a clock cycle. When asynchronous logic exists in the design, the tool cannot detect possible race conditions that can cause a glitch in the circuit and possible malfunction. Event-based simulators can provide full coverage of both timing and functionality including races, and glitches; providing they are given a complete set of input stimulus. Since it may not be possible to provide complete stimulus coverage, especially in large complex designs, static timing can provide additional verification protection.

Design Flows

Engineers need to evaluate each of the available design tools in conjunction with their design methodology and styles to determine a proper fit. In some cases, it may be necessary to alter current design methodologies to match the capabilities of the tool. Where adequate tools aren't available, users (especially silicon vendors) may be forced to develop the capability "in-house" where the silicon expertise resides. This also can create a tighter coupling between the process and tools as well as tool-to-tool integration. Using commercial solutions still remains a better solution where possible, even though the cost of integrating them into a given flow can be high in terms of time and money.

The one area where a company's design methodology may vary is the high-level design entry point, i.e., behavioral or data flow (RTL). This often depends on the application and the engineering expertise within the company. Hard-

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ware/software co-verification and full system verification also may dictate at which level to begin. Until recently, all behavioral representations of the design had to be "human-synthesized" due to the lack of available tools to perform the task. Some limited behavioral synthesis tools are now available, and it is expected that similar capabilities to those offered by RTL synthesis tools will be available as these products mature.

At the behavioral or RTL level, there's no real need for the accuracy of event-driven simulation, thus using a cycle-based simulator will provide adequate functional verification. The designs need to be split into approximately 10-kgate blocks to meet the limitations of most synthesis tools, however newer products on the market are claiming greater capacity. Configuration files are used to specify timing, power, and any other special requirements of the design.

Formal verification can be an excellent way to perform early design verification between this new structural representation of the design against its RTL predecessor. Design for test also must be considered at this point since testing of these large complex devices is becoming increasingly difficult and time consuming. Built-in self test (BIST) is now being considered for the entire ASIC due to testing complexities and time to validate production units. This is particularly applicable to complex IPs.

Once the design is synthesized into structural blocks, it can be subjected to analysis tools such as dynamic simulation, power analysis, and static timing. At this point, it's important to know if the design meets the criteria for fully synchronous designs. Some ASIC vendors like AMI have tools that analyze the design for not only design problems, but also to determine its compliance with fully synchronous design styles. For designs that meet the criteria, cycle-based simulation and static timing analysis can provide adequate validation.

For designs that do not, cycle-based simulators may still be an option for early validation, followed by full event simulation verification before releasing the design to the ASIC vendor. Since wire interconnect is a dominant part of the overall delay, floorplanners must become an integral part of the early synthesis steps as well as pre and post layout if design iterations are to be minimized. This applies to not only event-driven simulators, but also to static timing, and power- and noise-analysis tools.

The final sign-off validation requirements are still in the hands of the ASIC foundry which is responsible for ensuring the design is manufacturable. In the past, most ASIC vendors had either an internal proprietary "golden" simulator or used a commercial tool they trusted for final verification of the design. Now with the emergence of the HDL standards, most are providing sign-off support for various simulators that they have certified to be in compliance with the standards. With this in place, qualified customers can now perform the sign-off registration at their facility instead of passing off the design to the foundry, where registration differences may be found between the simulator the customer used versus the internal "golden" simulator. This puts the onus on the standards committees to ensure these languages are equal to the task.

What's Next?

Each new generation of technology will continue to bring with it new challenges that will likely require additional standards. One thing we must not do is to allow the release of standards to impact our ability to move forward. Both HDL language standards committess are preparing for a 1998 reballot. Silicon and tool vendors must work closely with the standards committees to ensure the standards keep pace.

Integrating the various EDA tools in a cohesive tightly coupled design environment may not be enough to ensure success. Silicon vendors may need to develop internal tools to augment those offered commercially. If the past 15 years are any indication of what this industry can do, the future looks bright as long as the team is working together.

Steve Wadsworth, Manager of Library Development for American Microsystems Inc., Pocatello, Idaho, has over 16 years of industry experience in test, design, and EDA tool management. He's the chair of the ASIC Task Force (subgroup under IEEE 1364) which is responsible for all timing aspects of the Verilog language, as well as a member of the VITAL TAG committee (IEEE 1076.4) and the IEEE SDF study group.

EDA WATCH

Closing The Silicon Reality Gap Is A Major Issue That Must Be Addressed

It has been widely accepted that interconnect is an important issue for sub-0.5-µm designs. In fact, interconnect has long been an issue for IC design. However, what has not been widely accepted is just how serious interconnect issues really are.

The majority of designs today rely on golden simulation or static timing analysis using extracted capacitance for design sign-off. However, as designs move into the sub-0.5-µm range, current methods of capacitance extraction are producing results with very poor correlation to silicon. If there is no change in the tools and methodology used today, the difference between the performance predictions given by EDA tools and actual measured silicon performance—the silicon reality gap—will rapidly increase as feature sizes decrease. Consequently, either more design or mask iterations will be needed to achieve timing goals, or designs will fail to fully exploit the performance the manufacturing process is capable of delivering. While this gap will never disappear, the current divergent trend is a major concern that must be addressed.

Inaccurate interconnect modeling is a major cause of the widening silicon reality gap. As process geometries shrink, the percentage contribution to system timing due to interconnect increases dramatically. In a 1-µm process, interconnect delay contributes only 20% of the total system delay. At 0.25 µm, interconnect delay may contribute over 70%. As a result, any inaccuracy in interconnect models at 0.25 µm will greatly influence timing predictions generated by EDA timing verification tools.

One reason why interconnect has become such a problem is that while feature sizes have decreased, wafer sizes have either stayed the same or increased. This has created a system-on-a-chip design methodology with designs composed of large functional units connected via long on-chip interconnects. Another reason stems from the fact that the minimum width and height of interconnect do not decrease linearly as feature sizes decrease resulting in longer, thicker, and taller wires that can no longer be modeled as simple capacitance loads.

Error Sources

One of the major sources of error in interconnect modeling is due to the creation of interconnect models from physical layout or parasitic extraction. Resistance of interconnect becomes an issue for designs using a 0.5-µm process; but usually only for global nets. As the process size decreases, the number of nets requiring RC (resistance and capacitance) extraction increases dramatically. For 0.25-µm designs, RC extraction is a necessity for nearly all nets.

The most accurate approach to interconnect extraction is to use a 3D-field solver that can usually predict RC effects to within a few percent of actual silicon. However, field solvers are computationally complex and can only be used effectively for very small pieces of interconnect.

The most common methods for full-chip parasitic extraction are based on 2D approaches. While they typically extract total net RC to within 20% of a 3D field solver model, they can have significant error (sometimes in excess of 50% from field solver results) on certain common interconnect structures. Because of the unpredictability of this error, 2D extraction cannot be relied on to close the silicon reality gap.

Capacitance lumped to ground is not sufficient to model long interconnects. As features sizes decrease, the relative amount of coupling capacitance to total capacitance increases. Coupling effects have a major impact on interconnect delays but coupling capacitance is difficult to extract accurately with current 2D or quasi-3D extraction tools. One possible solution for capturing all of these effects is 3D extraction. This option offers performance close to 2D extraction, but at the same time guarantees accuracy to within 10% of a field solver for any layout structure.

The other major source of error in interconnect modeling lies in the analysis of these models by delay calculators and timing analysis tools. The problem is that even if RC values can be accurately extracted, the result is a data explosion occurs that is virtually impossible to analyze using today's tools. Without sophisticated parasitic reduction techniques, the extracted RC network may be simply too large to analyze by timing or circuit analysis tools. It is not uncommon to have a 20X increase in the number of circuit elements; for a design of 10 million transistors that means 210 million total circuit elements (transistors and resistors). Even after a 90% parasitic reduction, analysis tools can suffer from a 5 to 20X increase in run-time. Many of today's tools cannot efficiently process such large RC networks.

To resolve the timing and noise impact of coupling, new analysis tools and design methodologies are needed. Methods for quasi-static analyses of cross-talk effects are being explored. These methods try to calculate the equivalent decoupled network that exhibits the same delay properties as the coupled net. The decoupled net can then be fed to an interconnect-savvy delay calculator to be converted into SDF for delay back-annotation. While this is not a complete solution, it is a good first step in managing the complex timing and noise issues introduced by coupling on long lines.

Another area where current design methodology falls short with respect to interconnect is in the timing characterization of cells. Today, all cells in a library are characterized over a range of capacitive loads. Whenever a cell drives a capacitive load, the resulting waveform follows a smooth almost linear curve. When the same cell drives a long distributed RC network, the waveform at the output of the cell has a linear ramp followed by a long flat tail and the waveform at the receiving end of the wire has a distinct exponential curve. These two waveforms must be modeled as a piecewise linear approximation.

The problem is that most static timing tools, including those used within synthesis and placement and routing, can only model linear slopes. The error incurred by a linear slope model can be as much as 50% for fast switching signals. This error also is propagated to the next stage of the design and hence can accumulate, resulting in erroneous timing optimization and verification. To re-

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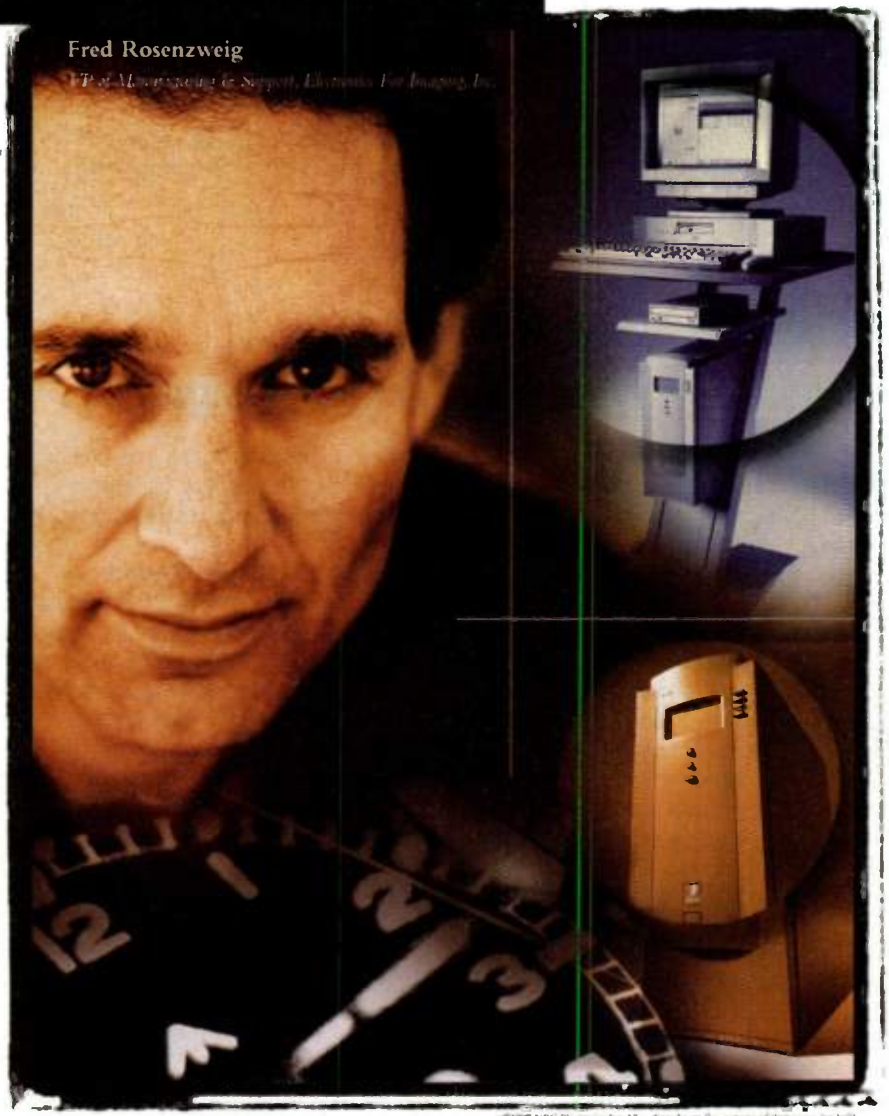

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solve the issues of inaccurate slope modeling, more sophisticated delay calculators are required.

Interconnect Impact

The bottom line is that interconnect is a huge headache for sub-0.5-µm design, with the most significant impact being levied on design productivity. All the increases in productivity brought about by advances in EDA tools such as synthesis and automatic placement and routing are in danger of being lost because the current design methodology is based on pre-layout interconnect estimation that has little correlation to the final silicon. Without close correlation to silicon, designs will either go through wasted iterations due to over estimation by the tools, or designs will fail in silicon due to under estimation. While designers have always allowed for some margin of error with tools, the error is growing well beyond an acceptable tolerance. Accurate extraction and analysis is essential for ensuring design correctness before manufacturing.

Contributed by Jim McCanny, executive vice president of sales and marketing for Ultima Interconnect Technology, Sunnyvale, Calif. He holds a bachelors degree in Computer Science and Mathematics from the University of Manchester, U.K.

For more information on this topic, contact Ultima at (408) 733-3380; Internet: http://www.ultimatech.com.

EDA WATCH

A Common Fabric Will Be A Key Element For System-On-A-Chip Designs

By the year 2000, system-on-a-chip (SoC) devices consisting of up to 12 million gates will be both possible and practical. Today, a single engineer can design only about 100 gates per day. Using this metric, it would take 400 engineering years to create just one SoC design. To successfully implement complex SoC designs, designers will need to extensively reuse intellectual property (IP) they develop or acquire.

Since it is unlikely that all the reusable blocks in a design will originate from a single source, a considerable amount of risk accompanies IP use. A typical 2-million-gate SoC ASIC, for example, might contain 10 IP blocks of 100-kgates—each from multiple vendors. While a typical 100-kgate ASIC has a 90% probability of working the first time, the 2-million-gate ASIC has only a 35% chance of working the first time. This is based solely on the risk associated with the 10 IP blocks!

SoC device designers face three main challenges. First, there's the aforementioned design risk. Second, ever-present time-to-market pressures define today's marketplace. Third, engineering resources are insufficient.

So, how will successful SoC design be accomplished? SoC design must employ a systematic design reuse strategy for creating and using IP, and a common fabric (or library technology) for the verification, integration, and distribution of IP.

Systematic Design Reuse

The first objective in a systematic design reuse strategy is to leverage your engineering resources as much as possible. If you're investing scarce engineering resources to design a block, the best way to leverage that activity is to design it specifically to be reusable. This is known as "design for reuse."

The second objective is to reduce the risk that the completed chips won't work. You must make additional efforts to create the design to be reusable, and this must be verified through implementation in silicon.

The third objective is to literally maximize reuse content. Today's business environment constantly challenges designers to reduce design time to meet shorter product cycles. A missed market window can kill a product line and impact a company's viability.

A Common Fabric

To reach these reuse objectives, a "common fabric" is needed. The ideal solution would enable the IP developer to create reusable IP blocks that can be easily ported to new processes, and enable SoC designers to easily integrate blocks from various sources into a single design. Industry-wide adoption of such a common solution for development, verification, implementation, and integration of reusable blocks would greatly enhance the deployment of IP and, consequently, simplify complex SoC design.

To merit widespread use, this common fabric would have to be suitable for both hard and soft forms of IP. Soft IP blocks are infinitely portable, but not as predictable as hard IP. Performance, area, power, and function are characteristics that only become definable when a library and process technology are targeted. Hard IP blocks are very predictable since a specific physical implementation can be characterized, but are hard to port since they are often tied to a specific process. The benefit of a common fabric would be that it enables the optimization of reusable blocks for both portability and predictability.

Other requirements for an ideal fabric include wide availability, synthesis efficiency, and the ability to take advantage of the capabilities of each of the targeted semiconductor processes. An example of one suitable "common fabric" solution is the Cell-Based Array (CBA) library technology. CBA is a metal-programmable architecture that provides the performance of a standard cell and is optimized for synthesis. A common set of CBA library elements have been characterized for each process and is now available at more than 60% of commercial ASIC foundries.

In support of the need for a systematic design reuse strategy that includes a common fabric, Synopsys, Mountain View, Calif., and Mentor Graphics, Wilsonville, Ore., have jointly created what is now referred to as the Design Reuse Partnership. The two companies have developed a design reuse methodology and are working to implement Mentor's Inventra IP cores in the CBA library technology. The goal of this effort is to effectively demonstrate how to create and distribute portable, predictable IP—and, ultimately, enable SoC design.

Contributed by Alan Aronoff, vice president and general manager of Synopsys' Silicon Architects, Mountain View, Calif.

For more information, contact Synopsys at (415) 962-5000; Internet: http://www.synopsys.com.

EDA WATCH

Hardware/Software Co-Design And Co-Verification Loom On The Horizon

Cheryl Ajluni

Designing these days is not an easy proposition, especially when you consider that neither electronic systems nor their development processes are homogeneous. Many electronic systems are heavily populated with software subsystems. As the complexity of electronic systems rise, so does the number of interfaces between them; providing fertile ground from which common sources of design, verification, and test problems throughout the development process can originate. Hardware/software (HW/SW) interfaces pose a particularly difficult problem because they're determined by two different engineering disciplines.

In general, two teams, software and hardware, start the process with a specification from which the functional partitioning of the design is derived. Each team begins developing their portion of the electronic system based on how they interpret the specification. The first time these differing interpretations are tested for consistency and accuracy occurs at system prototype integration.

While each subsystem may function error-free independently of one another, it's not always the case after they've been integrated. Mistakes in design interpretations, or assumptions made by one team during the design that were not properly communicated to the other, often results in costly expenditures of time, effort, and instrumentation. When a problem does occur, both teams are left to question how to proceed.

Traditionally, this design method has been acceptable, although time-consuming and headache-inducing. Designers were not faced with the same complexity and performance issues as they are today; back in the "old days," they had the luxury to deal with back-end interface HW/SW issues. Times have changed, though, and many designers now faced with shortened product life cycles and time-to-market pressures have been left to try and find a better way.

This problem is becoming increasingly evident on the consumer front, where getting a new product to market as quickly as possible can make or break a company. With so many products vying for the same consumer market, designers not only have to get their products out quicker than ever before, but with greater differentiation. This is one area where the ability to explore a variety of HW/SW subsystem partition options early in the design process is crucial.

HW/SW co-design promises to make this possible by allowing system designers to measure, not guess, performance of various functional system partitions before even getting into the design. By dealing with the design of hardware and software subsystems simultaneously, under a single methodology, HW/SW trade-offs can be made dynamically, as the design progresses.

The old microprocessor-centric view, whereby a system architect was responsible for integrating the hardware and software subsystems with a single tool, is changing. What's needed is a new methodology that allows hardware and software teams to work together from the start, thereby eliminating back-end integration issues altogether.

This methodology needs to incorporate not only issues of intellectual property (IP) use, test, and design of digital and analog components, but also must focus on defining, designing, and validating embedded systems containing substantial hardware and software content. Also needed is a HW/SW co-verification methodology that can work hand-in-hand with HW/SW co-design early in the design process, as a way of verifying that estimated system performance will match actual system performance.

The real dilemma lies in how to develop this co-design and co-verification methodology. What form will it take? How will it be implemented? To that end, many EDA tool vendors and IC-companies are working diligently to address these issues. Some have banded together in consortiums and through initiatives to provide designers answers to these questions. The year ahead promises to witness hard solutions to many of these tough issues.

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Tips For Using High-Speed DACs In Communications Design

Selecting The Optimal DAC Means Knowing How To Interpret Converter Specifications And Their Effect On System Performance.

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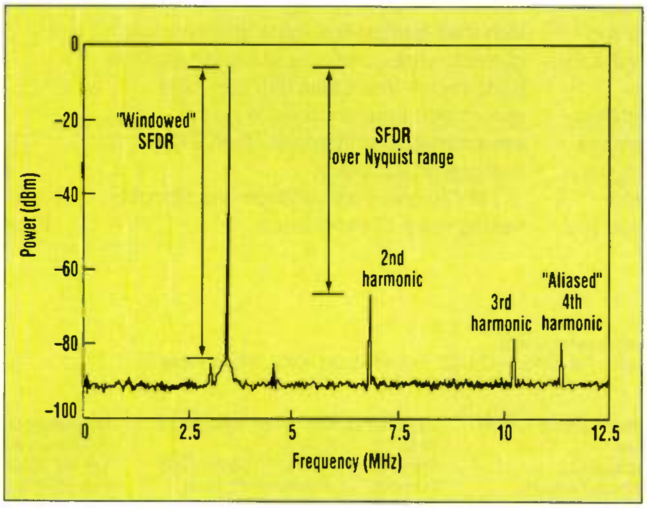
Editor's note: The following article is the first in a two-part series on using high-speed DACs in communications design. Part I focuses on evaluating DAC specifications. Part II will discuss various DAC system interface issues.

The burgeoning digital communications market has generated an unprecedented demand for a new generation of high-speed digital-to-analog converters (DACs). Many of these converters are being used in the transmit signal path to reconstruct the complex analog waveforms demanded by sophisticated digital modulation schemes. Advances in very-large-scale integration (VLSI) and digital-signal processing (DSP) technology now allow for more of the signal processing to be performed in the digital domain. There are many reasons behind the digital shift: higher spectral efficiency and capacity, improved quality, added services, software programmability, and lower power.

Synthesizing communication signals in the digital domain typically allows the characteristics of a signal to be precisely controlled, if not predicted. However, in the reconstruction process of a digitally synthesized signal, it's the DAC and its nonideal characteristics that often yields unpredictable results. In some cases, it's the performance of the DACs that actually determines whether a particular modulation scheme or system architecture can be implemented.

Unlike high-speed video DACs used to recreate images on high-resolution PC and workstation monitors, the performance of these converters are often analyzed in the frequency domain with secondary consideration to time domain and dc specifications. Selecting the optimum DAC for a given application requires an understanding of how to interpret various converter specifications and their effects on system performance. In addition, achieving the optimum performance while realizing other system objectives demands careful attention to various analog- and digital- interface issues *(to be covered in Part II of this article).*

Responding to the needs of these emerging markets, semiconductor vendors are releasing a new generation of CMOS and bipolar DACs that range from standard products of varying resolution, speed, and performance to more integrated products incorporating various DSP functions. These DSP functions may include digital interpolation filters, which reduce the complexity and cost of the required analog reconstruction filter, or complete application-specific digital modulators for quadrature or spread-spectrum modulation schemes.



1. This full-scale, single-tone spectral plot represents a single measurement point in which the DAC's amplitude, output frequency, update rate, and operating conditions are all uniquely specified.

Better Performance

Much design effort has gone into improving the frequency-domain (ac) and static (dc) performance of these devices, while meeting other system objectives such as single-supply operation, lower power consumption, lower cost, and ease of digital integration. Several semiconductor vendors have elected to focus their effort on designing high-performance DACs using a digital CMOS process. In fact, today's CMOS DACs have overcome many of the deficiencies associated with their predecessors, video DACs, and now provide performance

DESIGN NOTES

High Efficiency Linear and Switching Solutions for Splitting a Digital Supply – Design Note 172

Dave Dwelley and Gary Maulding

It can be inconvenient to generate a split supply in a typical digital system. The classic solution is to use a pair of resistors between 5V and GND to create a 2.5V "ground" for analog circuitry (Figure 1). Unfortunately, the resultant "ground" has a painfully high impedance and the resistors draw a large amount of supply current. The output can be buffered with an op amp to lower the impedance, but a specialized op amp is required to handle any significant bypass capacitance at the output. This Design Note presents two alternate methods of creating a split supply that can provide good transient response while conserving supply current.

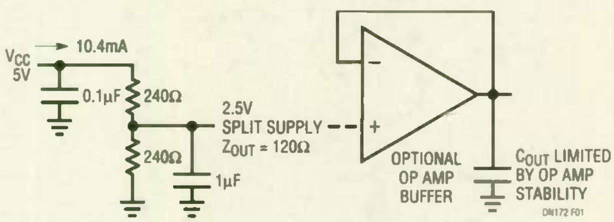


Figure 1. Resistor Divider Supply Splitter

The LT®1118 is a specialized linear regulator designed to source or sink current as necessary to keep its output in regulation. It can handle output capacitors of arbitrarily large size, improving output transient response. Available with a fixed 2.5V output (ideal for splitting 5V supplies), it draws only 600µA quiescent current typically and can source 800mA or sink 400mA, enough to satisfy most analog subsystems. The LT1118 requires only two external components (Figure 2) and features a DC output impedance below 0.1Ω under all loading conditions, far better than any practical resistor divider solution. The LT1118 draws only enough supply current to meet the demands of the load at the split supply, providing nearly 50% power efficiency over a wide range of load currents (Figure 3). Load transient response is excellent, with less than 5µs recovery time from a ±400mA current load step (Figure 4). At low current levels, the LT1118 is the optimum solution for splitting a digital supply.

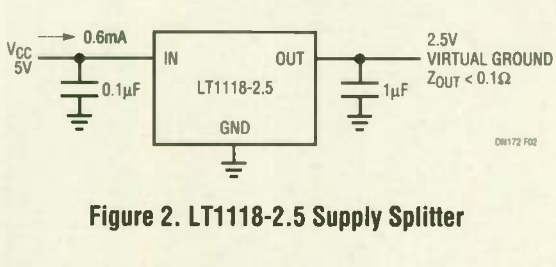


Figure 2. LT1118-2.5 Supply Splitter

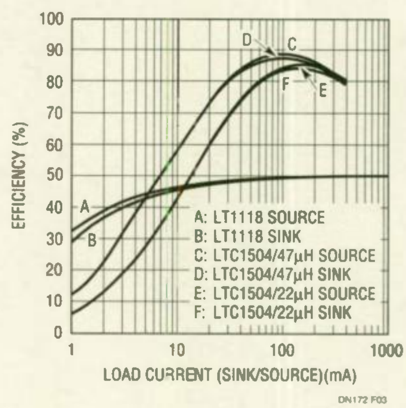


Figure 3. Efficiency vs Load Current for Linear and Switching Circuits

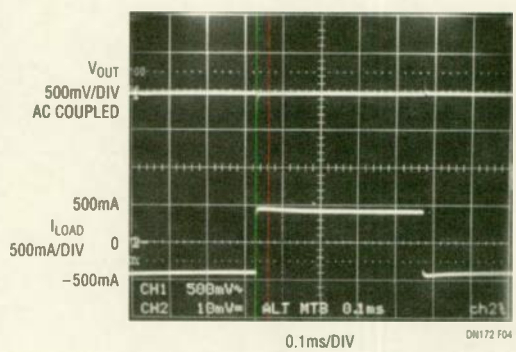


Figure 4. LT1118 Transient Response

ıt higher power levels, the 50% efficiency of the LT1118 ;an become a liability in power-sensitive or battery-pow- ɪred systems since half of all the power drawn from the ;plit supply is wasted heating up the LT1118. The LTC®1504 ıddresses this situation by providing as much as 90% ɪfficiency while sourcing or sinking up to 500mA. The .TC1504 is a synchronous switching regulator with on- ɔoard power switches. The continuous conduction, syn- :hronous buck architecture inherently sinks current as well ıs sourcing it, making the circuit an effective supply ;plitter. Quiescent current is 3mA with typical compo- ıents. This penalizes efficiency at low current levels when :ompared to the LT1118, but the intrinsic power conver- ;ion abilities of the inductor-based switching architecture ıllow power efficiencies approaching 90% above 100mA Figure 3 again). A typical LTC1504 circuit will draw only ;6mA from the 5V supply while sourcing 100mA from the ?.5V output—magic!

'he switching architecture of the LTC1504 requires a few nore external components than the LT1118 (Figure 5), and ɟenerates a small amount of output noise at the 200kHz ;witching frequency. Transient recovery is controlled pri- narily by the value of the external inductor. With a 47µH nductor, switching noise is minimal and the circuit recov- ɪrs from a ±400mA output load step in 30µs (Figure 6).

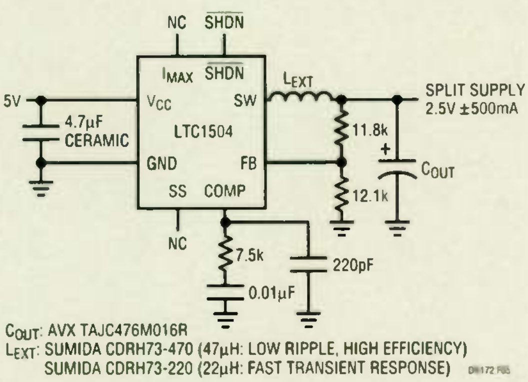


Figure 5. LTC1504 Supply Splitter

Switching to a 22µH inductor brings transient recovery time down to 15µs (Figure 7), but output ripple and quiescent current increase. The LTC1504 features a shut- down pin that drops quiescent current below 10µA when the split supply is not required.

Both the LT1118 and the LTC1504 provide superior supply splitting when compared to simple resistor- or regulator- based circuits. The LT1118 fits best where impedance requirements are critical at low current levels, or where low output noise is paramount. The LTC1504 is the best solution where efficiency, especially at high current levels, is the overriding concern. Both devices can also be used in similar applications where source/sink capability is impor- tant, such as SCSI or positive ECL supplies.

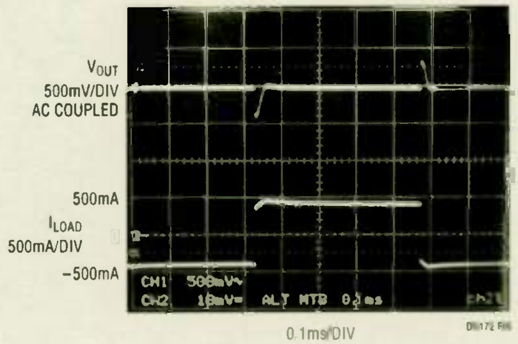


Figure 6. LTC1504 Transient Response with 47µH Inductor

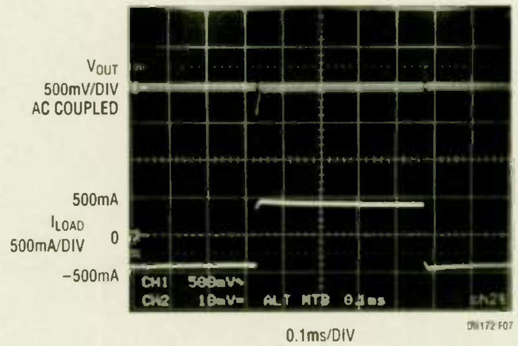


Figure 7. LTC1504 Transient Response with 22µH Inductor

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that's comparable, if not superior, to their bipolar or BiCMOS counterparts. As a result, system engineers are wise to keep informed about the latest trends and product releases that can affect how designers craft a next-generation system.

This renewed interest in high-speed DACs also has highlighted many shortcomings in the way these critical devices are traditionally described. As many engineers are learning through painful experience, selecting a DAC for any waveform- reconstruction application purely based on resolution, settling time, dc accuracy, and glitch impulse can often provide results far worse than anticipated.

Although certain observations can be made about the effects that the static (dc) and dynamic (time domain) specifications may have on a DAC's frequency (ac linearity) performance, the cumulative effect still remains impossible to predict, which is why simulation models do not currently exist. Because both static and dynamic nonlinearities will manifest themselves in the frequency domain, and contribute to a DAC's large- and small-signal distortion performance, a high-speed DAC should be primarily evaluated using specifications and characterization data pertaining to its frequency domain.

The frequency-domain performance of high-speed DACs has traditionally been characterized by analyzing the spectral output of reconstructed single-tone sine waves *(Fig. 1)*. Single-tone sine-wave characterization of any analog or mixed-signal component allows for the easy identification of its various nonlinearities. Until recently, most of this analysis was performed using only full-scale (in other words, 0 dBFS) sine waves at a few selected update rates, presenting limited insight into a DAC's performance in a real-world communications application.

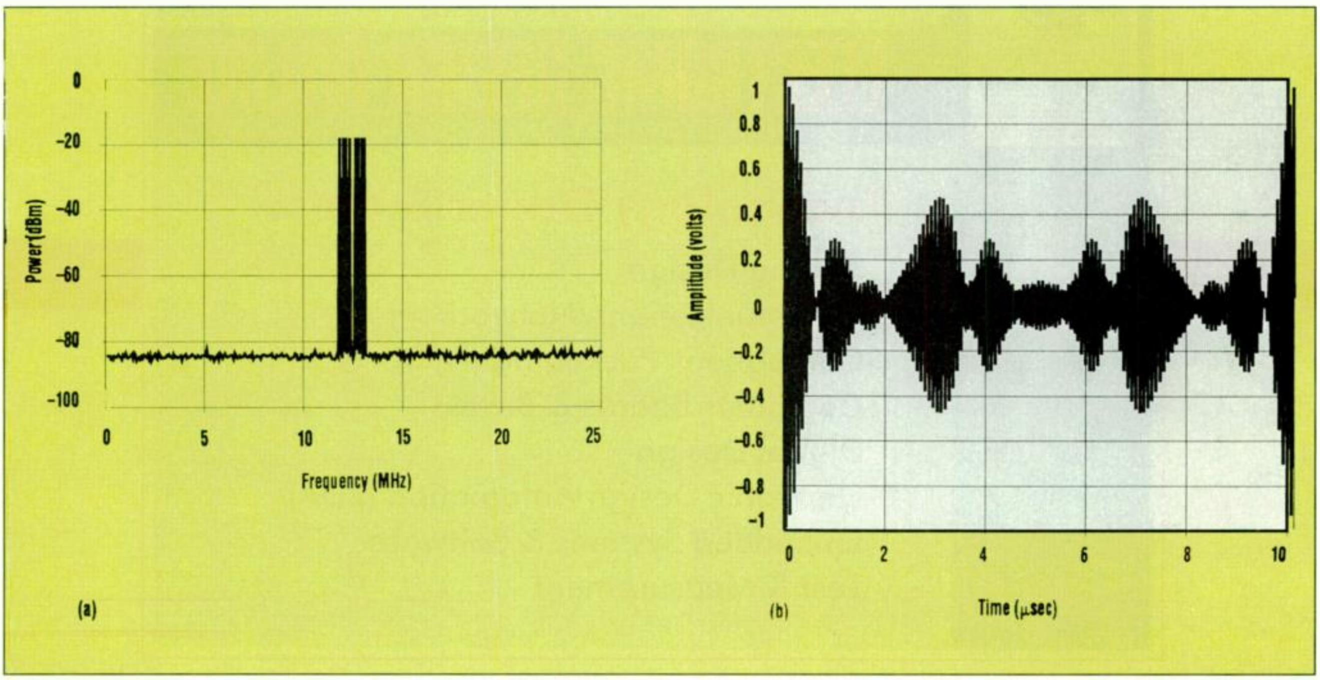
The spectral output of a DAC will contain both harmonic (including aliased harmonics) and nonharmonic spurious components that weren't part of the original digitally synthesized sine wave. Figure 1 represents a single measurement point in which the DAC's amplitude, output frequency, update rate, and operating conditions are all uniquely specified. Changing any of these conditions will often modify the nature of these spurious components. Consequently, multiple measurement points using different synthesized waveforms with varying DAC operating conditions must be taken, analyzed, and plotted to accurately ascertain a DAC's performance. All of this activity must be done while capturing any significant performance trends. To ease the selection process, the datasheets of more recently released converters will contain several pages of characterization curves.

Dynamic Range

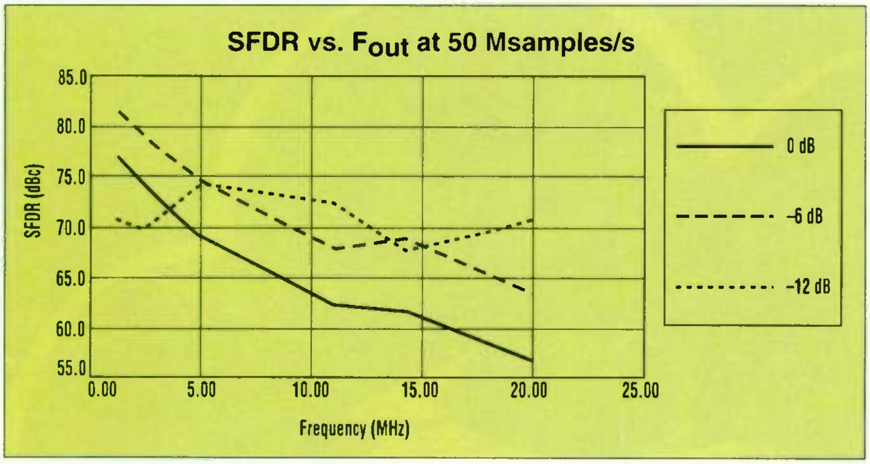
Spurious-free dynamic range (SFDR), perhaps the most-often-quoted DAC specification, defines the difference, in decibels, between the rms power of the fundamental and the largest spurious signal within a specified band. SFDR is usually specified over the full Nyquist region extending from dc to one-half the data-update rate ($f_{CLOCK}/2$).

Typically, the worst spur is harmonically related and constitutes more than 80% of the total harmonic energy. Therefore, total harmonic distortion (THD) is rarely plotted over frequency because it's often only 1- to 3-dB worse than the SFDR performance. However, THD characterization curves plotting the three most significant distortion components can sometimes be helpful in determining which specific nonlinearity(ies) (such as second- or third-order distortion) limits a DAC's performance. Then, the effects of that nonlinearity can possibly be avoided via careful placement of the reconstructed signal.

SFDR also can be specified over a narrowband or window that purposely excludes the worst spur. The useful-



2. The multitone spectral plot shows eight tones centered around one-half the Nyquist bandwidth, $f_{CLOCK}/4$ (a). A time-domain "snapshot" of the multitone waveform reveals the higher signal content around the midscale value (b).



3. Characterization curves show SFDR versus output frequency at 50 Msamples/s for a 12-bit CMOS DAC. The SFDR is measured relative to the single tone (-dBc), as opposed to its full-scale value (dBFS).

ness of this particular specification is relegated to those narrowband applications (for example, clock generation using direct digital synthesis) in which the DAC's full-scale output is operated over a limited spectral region, with the notion that the dominant "out-of-band" spurs can be filtered. In these applications, generating signals that are centered at either one-quarter or one-third the DAC's update rate will typically provide the worst-case performance due to the aliasing-back effect of the DAC's second or third harmonic. Thus, it may need to be avoided.

Signal-To-Noise Ratio

A DAC's noise performance also is becoming increasingly important in determining its suitability in various communication applications (such as spread spectrum). In these applications, the carrier-to-noise ratio (CNR) of the reconstructed waveform that includes the effects of both noise and distortion will directly affect the system's bit-error rate (BER). Although the effects of quantization (representation of an analog waveform with a digital word of finite resolution) on a DAC's noise performance can be easily predicted, the additive noise effects resulting from differential nonlinearity (DNL), digital feedthrough, and jitter are more difficult to predict.

Specifications and characterization curves that reveal the signal-to-noise ratio performance with and without distortion (SNR and SINAD) are beginning to appear on the datasheets of 8- and 10- bit DACs. For converters with 12-bit or higher resolution, the accurate characterization and testing of these important performance parameters becomes much more challenging.

As previously mentioned, full-scale sine-wave characterization data is useful, but is often still insufficient in representing a DAC's performance in a real-world communications application. The characteristics of the reconstructed multitone (carrier), spread spectrum, or QAM waveform are far different than a simple, full-scale sine wave. In fact, a DAC's spectral performance in a full-scale, single-tone waveform at the highest specified frequency (f_H) of a band-limited waveform is typically indicative of a DAC's worst-case performance for that given waveform. In the time domain, this full-scale sine wave represents the lowest peak-to-rms ratio or crest factor (V_{PEAK}/V_{RMS}) that this band-limited signal will encounter.

However, the inherent nature of a multitone, spread spectrum, or QAM waveform in which the spectral energy of the waveform is spread over a designated bandwidth will result in a higher peak-to-rms ratio when compared to the case of a simple, full-scale sine wave. As the reconstructed waveform's peak-to-average ratio increases, an increasing amount of the signal energy is concentrated around the DAC's midscale value. As a result, a DAC's small-scale dynamic and static linearity become increasingly more critical in obtaining low intermodulation distortion and maintaining sufficient carrier-to-noise ratios for a given modulation scheme. Hence, the systems engineer also must keep in mind the nature of the specific signal to be synthesized, and determine which DAC specifications and set of characterization data has the most relevance in their communications design.

An example of a band-limited multitone vector shows eight tones centered around one-half the Nyquist bandwidth, $f_{CLOCK}/4$ *(Fig. 2a)*. This particular multitone vector has a peak-to-rms ratio of 13.5 dB compared to a sine wave's peak-to-rms ratio of 3 dB. A snapshot of this reconstructed multitone vector in the time domain reveals the higher signal content around the midscale value *(Fig. 2b)*.

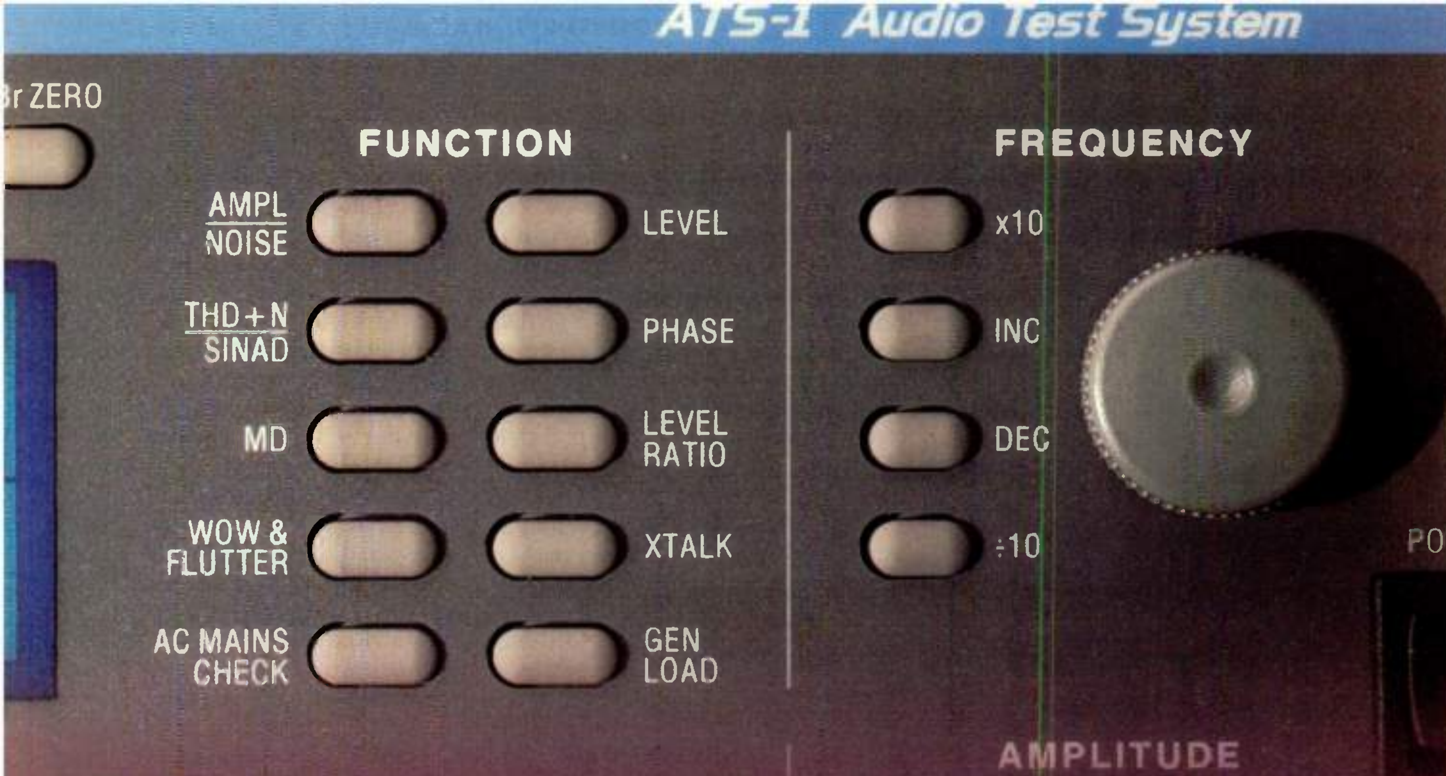
A DAC's small-scale linearity performance also is an important consideration in applications where additive dynamic range is required for gain control or predistortion signal conditioning. For instance, a DAC with sufficient dynamic range can be used to provide additional gain control of its reconstructed signal. In fact, the gain can be controlled in 6 dB increments by simply performing a shift left or right on the DAC's digital input word.

Intentional Predistortion

Other applications may intentionally predistort a DAC's digital input signal to compensate for nonlinearities associated with the subsequent analog components in the signal chain. For example, the signal compression associated with a power amplifier can be compensated for by predistorting the DAC's digital input with the inverse nonlinear-transfer function of the power amplifier. In either case, the DAC's performance at reduced signal levels should be carefully evaluated.

Characterization curves revealing a DAC's single-tone SFDR performance at different fixed update rates as both the output frequency and amplitude are swept, are useful for many communication applications because the DAC update rate is often fixed by design *(Fig. 3)*. Such a set of curves for the AD9762, a 12-bit member of Analog Devices CMOS TxDAC family, are shown in which the SFDR is measured relative to the single tone (−dBc) as opposed to its full-scale value (dBFS).

A more informative DAC datasheet will present several of these characterization curves at different sample rates



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(for example, 5, 25, 50, 100, and 125 Msamples/s) because high-speed DACs are often operated over a myriad of sample rates below their maximum specified rate. Note how the full-scale single-tone curve exhibits the fastest roll-off in SFDR performance as the frequency increases. This change is indicative of how quickly dynamic nonlinearities such as code-dependent glitch, slewing, and settling characteristics prevail over the static nonlinearities such as integral linearity.

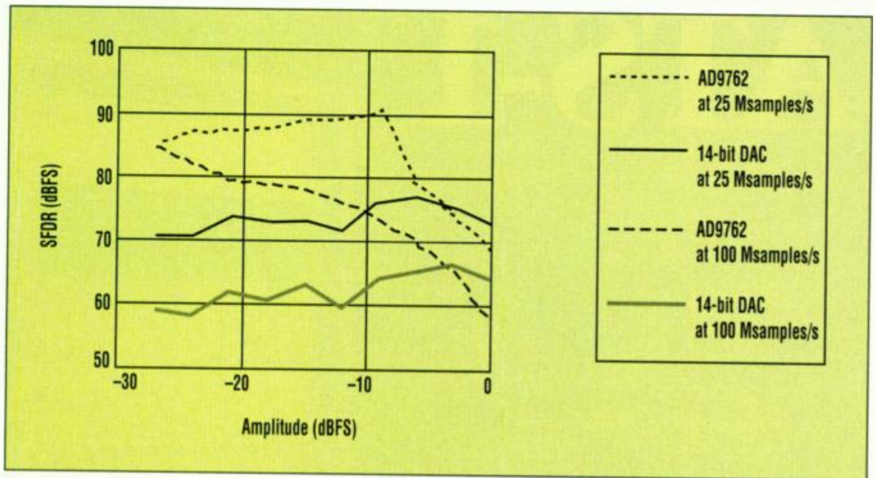
Perhaps equally intriguing is that the lower-level signals of –6 and –12 dBFS provide superior SFDR performance over a larger span of output frequencies. The performance levels suggest that operating some DACs with less than full-scale signals can actually be advantageous in meeting a particular system's SFDR requirements. In other words, for applications that require full-scale SFDR performance above 65 dBc over their full bandwidths, but yet only need 10-bits of resolution, a designer may want to consider selecting a 12-bit DAC, and use only one-half or one-quarter of its dynamic range.

Small-Scale Linearity

Maintaining decent small-scale linearity across the full span of a DAC's transfer function is essential to maintaining excellent multitone performance. Although characterizing a DAC's multitone performance tends to be application specific, much insight into the potential performance of a DAC also can be gained by evaluating its swept-power (amplitude) performance for single, dual, and multitone test vectors at different clock rates and carrier frequencies. The DAC is evaluated at different clock rates when reconstructing a specific waveform whose amplitude is decreased in 3-dB increments from full-scale (0 dBFS). For each specific waveform, a graph showing the SFDR (over Nyquist) performance versus amplitude can be generated at the different tested clock rates with the carriers-to-clock ratio remaining constant.

Analysis of a DAC's swept-amplitude-SFDR results can often lead to some surprising revelations that may at first appear counter intuitive. For instance, in comparing the SFDR-versus-amplitude performance between the AD9762, the 12-bit CMOS DAC, and a recently released 14-bit BiCMOS DAC, the BiCMOS has an advantage in resolution, settling time, dc accuracy, and glitch energy over the lower cost and lower power CMOS DAC *(Fig. 4)*. This comparison is based on the static linearity and dynamic specifications stated in each datasheet.

Both DACs were updated at 25 and 100 Msamples/s while reconstructing an output frequency of 5 and 20 MHz. In this case, the SFDR is plotted relative to a full-scale output to underscore how the SFDR performance of the AD9762 actually improves as the amplitude is reduced. In the meantime, the 14-bit BiCMOS performance remains relatively unchanged. At both 25 and 100 Msamples/s, the AD9762 begins to display superior SFDR performance for single-tones below –4 dBFS. For reconstructed amplitudes below –9 dBFS, the difference in SFDR performance between the AD9762 and the BiCMOS DAC can be as great as 10 to 15 dB, proving a DAC's resolution, static linearity, and dynamic specifications don't necessarily guarantee dynamic range! Multitone tests performed at similar update rates and output frequencies reveal that the AD9762 consistently shows better SFDR and intermodulation distortion performance.



4. Analysis of a DAC's swept-amplitude-SFDR results can often lead to some surprising revelations. This plot compares the SFDR-versus-amplitude performance of a 12-bit CMOS DAC and a recently released 14-bit BiCMOS DAC.

A multitone test vector may consist of several equal amplitude, equally spaced carriers that are each representative of a channel within a defined bandwidth similar to what is shown in Figure 2a. In many cases, one or more tones are removed such that the intermodulation distortion performance of the DAC can be evaluated. Nonlinearities associated with the DAC will create spurious tones of which some may fall back into the "empty" channel, limiting a channel's carrier-to-noise ratio.

In the case of multichannel (FDMA) communications applications such as cellular phone or cable television systems, this undesirable spur is often referred to as an "interferer." Other spurious components falling outside the band of interest also may be important, depending on the system's spectral mask and filtering requirements. Regardless, regulatory or standards bodies such as the FCC have placed strict limits on the amount of out-of-band noise and distortion a transmitter can generate.

The particular test vector shown in Figure 2a was centered around one-half the Nyquist bandwidth ($f_{CLOCK}/4$) with a passband of $f_{CLOCK}/10$. Centering the tones at a much lower region ($f_{CLOCK}/10$) typically leads to an improvement in performance, while centering the tones at a higher region ($f_{CLOCK}/2.5$) often results in a degradation in performance. In assessing a DAC's multitone performance, it also is recommended that several devices be tested under the same exact conditions to determine any performance variability among devices.

Paul Hendriks is an applications engineer for high-speed converter products at Analog Devices' Standard Linear Products Division. He holds a BSEE from McGill University.

Circle 520

Minimize Clock-To-Output Delays In CPLD Designs

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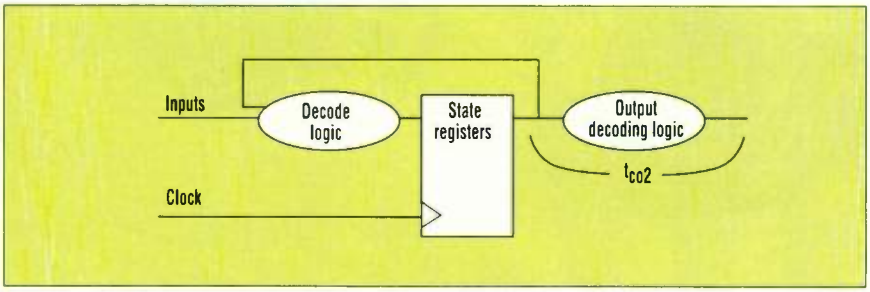
Minimizing clock-to-output (t_{co}) delays in a CPLD-based design may permit use of a slower, lower-cost CPLD. The example design shown is a state-machine implemented using a CPLD that operates as an interface between a memory-mapped peripheral and an Intel 80960 processor. The state machine controls the peripheral's chip-select, read, and write lines, as well as the 80960's ready-recover (RDYRCV) line.

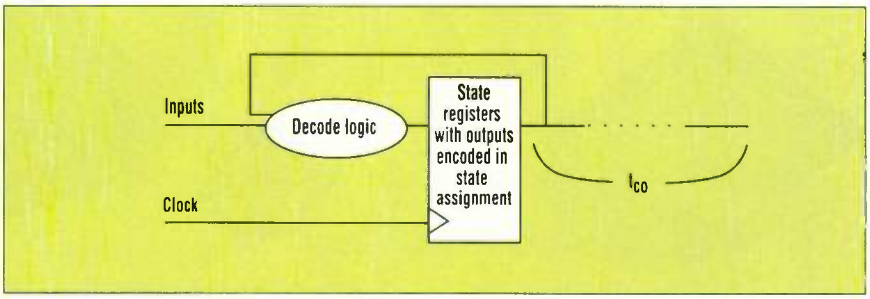
The example uses a Cypress CY7C371i CPLD. Because the state machine has to operate at 25 MHz, the slowest speed-grade variant of the part was selected. The initial implementation of the state machine shows clock-to-output delays of 24 ns, but the design requires the delays to be less than 15 ns. So what can we do now?

First, we realize that the 24-ns delays represent second-pass (t_{co2}) clock-to-output delays; that is, they're due to an additional pass through the CPLD's logic block to decode the outputs *(Fig. 1)*. So, a higher-speed (lower t_{co2}) CPLD can be used. A more clever approach, however, would be to encode the state-machine outputs within the state bits *(Fig. 2)*. This eliminates the need for output decoding logic and guarantees that the outputs are available at the 10-ns t_{co} specified on the data sheet for the slowest part (rather than at its 24-ns t_{co2}).

Encoding the outputs within the state assignments is a straightforward procedure. First create a table matching each state with the desired outputs *(see the table)*. Then identify the largest number of states with the same set of outputs⇓in our example, there are three (note the four 1's in Output rows 1, 8, and 15 in the table). Finally, create a unique encoding for each state: In this example, an additional two bits are required.



1. Output decoding requires a second pass through the CPLD logic block.



2. Encoded outputs eliminate the need for output decoding, resulting in a shorter clock-to-output.

STATE ASSIGNMENTS FOR OUTPUT ENCODING

	Outputs					
States	IO_CS	IO_RD	IO_WR	RDYRCV	Uniquifying bits	
address_idle	1	1	1	1	0	0
read_wait1	0	1	1	1	0	0
read_wait2	0	0	1	1	0	0
read_wait3	0	0	1	1	0	1
read_wait4	0	0	1	1	1	0
read_data	0	0	1	0	0	0
read_recover1	0	1	1	0	0	0
read_recover2	1	1	1	1	0	1
write_wait1	0	1	1	1	0	1
write_wait2	0	1	1	1	0	0
write_wait3	0	1	1	1	0	1
write_wait4	0	1	1	1	1	0
write_data	0	1	0	0	0	1
write_recover1	1	1	0	0	0	0
write_recover2	1	1	1	1	1	0

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Circuit Senses High-Side Current From Negative Supply

MICHAEL KRICKL
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The circuit shown monitors the flow of load current into a negative voltage source *(Fig. 1)*. This requirement often arises in private branch exchanges, in ISDN power supplies, when monitoring supply currents in the central-office supply of a telecom system, or when monitoring current from the negative supply rail of an audio amplifier.

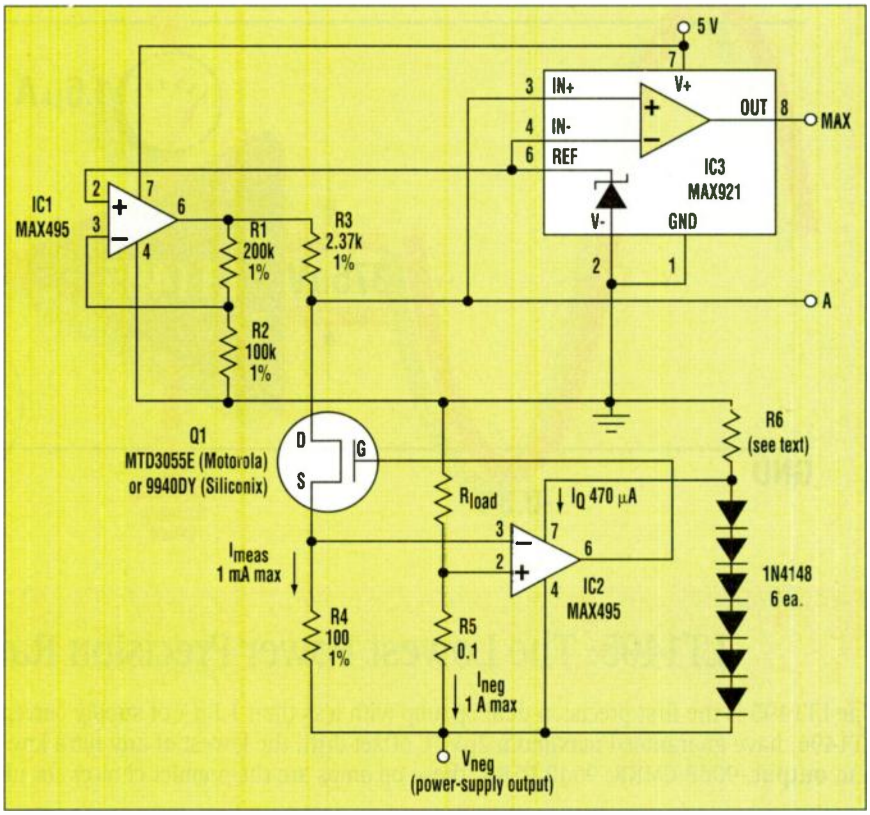
Ground-side current sensing is relatively easy, but most of these cases feature supply-side sensing and its associated design problems. Small current-sense voltages near the negative rail are difficult to measure; few op amps can handle the high voltages involved (approximately −48 V to −72 V). Fewer still offer the required rail-to-rail operation and the resulting current measurement signal must be transferred and level-shifted for suitable interfacing with a microcontroller.

The current-sense resistor (R5) is on the "hot side" of the load with a value that allows maximum load currents of 1 A. Its tolerance should be 1% for acceptable accuracy. You can easily set other maximum load currents (I_{NEGmax}) by adjusting the resistor's value:

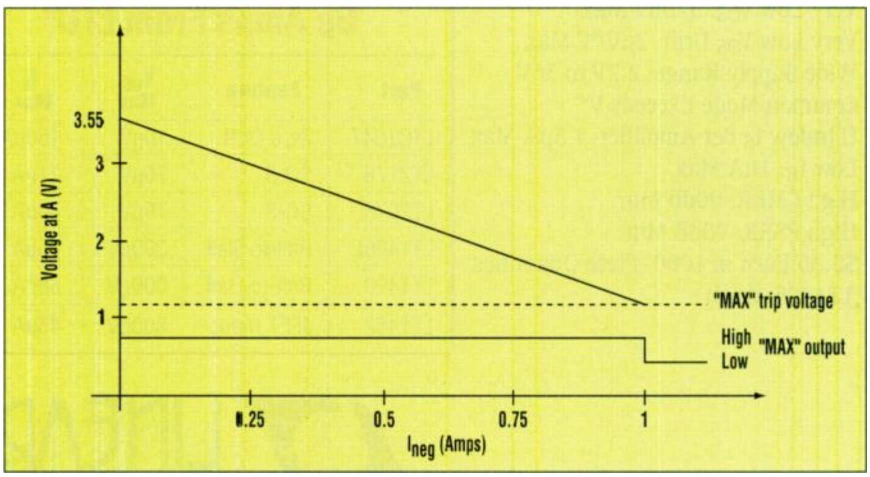
$$R5 = 100\ mV/I_{NEGmax}$$

The rail-to-rail operation of op-amp IC2 enables it to recognize the small positive voltage produced at its noninverting input by the load current through R5. IC2's gate drive to the MOSFET then causes an identical voltage to appear across R4. R4's value (100 Ω) is of similar tolerance but 1000 times that of R5, so its current is 0.001 that of R5. This R4 current flows through the MOSFET and R3. IC2's low offset value (500 µV maximum) has little effect on the accuracy of current through R3.

IC2's low quiescent current (170 µA maximum) and low operating voltage allow operation with a simple power supply. Six 1N4148 diodes in series produce sufficient voltage (4 V) to operate the op amp and provide adequate gate drive to the MOSFET. This arrangement also allows use of a single-supply op amp. For a given value of V_{NEG}, R6 should bias the diodes at about 500 µA:



1. This circuit monitors high-side load current into a negative supply, generating a digital alarm (MAX) when the current reaches its maximum.



2. The signal voltage "A" in Figure 1 varies with load current as shown, producing the digital warning signal (MAX) at the specified maximum. Polarity of this signal can be easily changed.

R6 = (4V – V_{NEG})/500 μA

(you also can use a 3.5V-to-6V Zener diode in place of the 1N4148s.)

Op-amp IC1 amplifies the 1.182-V reference in IC3 by a factor of three, producing an output of 3.55 V. Thus, as the load current (I_{NEG}) ranges from 0 to 1 A, the current in R3 ranges from 0 to 1 mA, producing a signal voltage (A) that ranges from 3.55 V down to 1.182V *(Fig. 2)*. This range ensures that "A" remains positive for maximum load currents.

Signal voltage "A" also connects to IC3, so the comparator output changes from high to low when the load current reaches its 1-A maximum. The polarity of this digital output can be changed by swapping the comparator's input connections.

Circle 522

Keyboard Scanner Provides System Supervision

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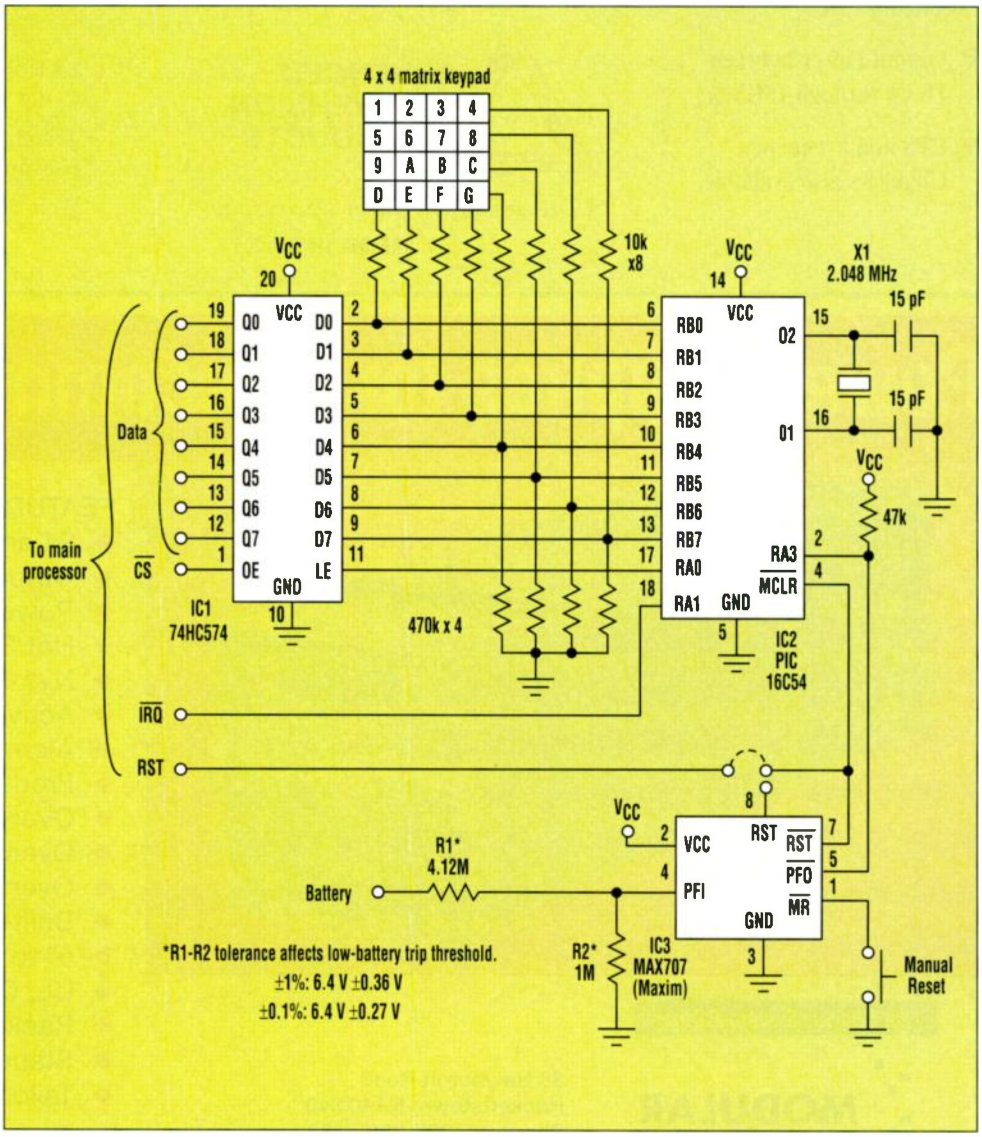
The circuit shown scans a numeric keypad while also generating 16-ms timing interrupts, low-line resets, and power-fail warnings for a larger system *(see the figure)*. The core of the circuit is a versatile PIC16C54 microcontroller augmented by a microprocessor supervisor (IC3).

In place of the microcontroller shown in the figure, most systems typically employ dedicated logic—a keyboard-interface IC such as the 74C922, a time-base generator such as the 74C4060, a 32-kHz crystal, and a microprocessor supervisor. The small and inexpensive PIC, however, offers design flexibility in exchange for some simple code development. *(see the listing)*.

The microprocessor supervisor generates active-high and active-low resets in response to a low V_{CC} voltage. It comes in 5-V and 3.3-V versions; the one shown is a 5-V type with a trip threshold of 4.4 V. It also monitors the battery via the power-fail input (PFI), with a trip threshold of 6.4 V set by R1 and R2. Battery status is read by the PIC at IC3's $\overline{\text{PFO}}$ output, and encoded as the MSB (RB7) of an 8-bit data word returned to the main processor every 16 ms.

Other data bits in this byte pertain to the keypad--a 4-by-4 matrix-type such as the Grayhill 84S-BC series. The PIC scans the keypad for contact closures by issuing consecutive "1"s on the low nibble of the bidirectional RB port (RB0-RB3) and watching for a tell-tale "1" on the high nibble. It then converts this row-column information to a 4-bit code, issues it on



As part of a larger processor-based system, this three-IC circuit scans the keypad and provides a time base interrupt signal while simultaneously monitoring V_{CC} and the battery voltage levels.

```
;..............................................................
;   BY:  John M. Wettroth, FAE
;        Maxim Integrated Products
;        Sunnyvale, CA
;..............................................................
;   assembled linked and loaded under: Parallax PASM V2.2 tools
;   (no parallax special mnemonics used)
;..............................................................
; DESCRIPTION:
;
; PIC16C54, 574 latch and Max707 supervisor provide keyboard scan
; function for 4 x 4 keypad, programmable timer ticks for IRQ and
; low voltage warning.  Slave system that gives periodic interrupts
; and keys to main processor.  Processor reads the 574 in its address
; space (mapped as i/o or data- single line read).  8-bit result
; contains 4-bit key code, power status and key held down status.
; IRQ timing is precise so that a single main IRQ routine can
; maintain system timers with the same ISR (saves an int).  Time is
; 16 ms for sample code here  Keyboard scan routine includes key
; debounce and multi-level hold timer for keyboard autorepeat functions.
;
; Format of 8-bit data returned:
;
; Bit positions:     7     6     5     4     3     2     1     0
;                | VCC | ---WHLS--- | -------------- KEYS -------------- |
;
;   VCC- Set if Vcc < 4.8 volts.  Could also be used for
;        low battery if PFI on Max707 is connected to raw
;        power and resistors are set appropriately.  Note:
;        PIC will operate down to 2.5 volts.
;
;   WHLS- 2-bit count value of how long key held
;        Multilevel keyboard autorepeat functions.
;        0 = 1 tick = new (1 tick debounce)
;        1 = 2-10  ticks.      <.16s
;        2 = 10-20 ticks.  .16-.32s
;        3 = > 20  ticks.      > .32s
;
;   KEYS- Keycode of key pressed 1-16.  Note: zero is no key.
;
; If zero is read then main processor should just do its timer
; maintenance routines.
;..............................................................
; PROCESSOR DECLARATIONS - set high ROM bits
; device type, osc type, watchdog timer, code protect
; 16C54      =XT ON,   =WDT OFF,    =UNPROTECTED CODE

 DEVICE  PIC16C54, XT_OSC,WDT_OFF, PROTECT_OFF

;*** DEFINE RESET ADDRESS VECTOR (1FF)
RESET    START             ;set reset vector to address at start

;status byte bits- carry and zero
CY       EQU    0          ;carry bit
ZR       EQU    2          ;zero bit
F        EQU    1          ;destination bit  x,d
;..............................................................
; I/O DECLARATIONS

; PORT MAPPING

; PORT A  bits

LATCH    EQU    0          ;to 574 clock- rising edge trig
IRQ      EQU    1          ;irq- neg true each tick
LED      EQU    2          ;unused
PFI      EQU    3          ;Max707 comparator in- low true
;
; PORT B
;
;keyboard read/latch write- no bits assigned
;
;..............................................................
; VARIABLE   DECLARATIONS

; general purpose transient variables
; note parallax debug steps on locations 08h-0fh
LPCTR    EQU    10H        ;loop counter 1
TEMP     EQU    11H        ;temp
KEY      EQU    12H        ;key value
WHLS     EQU    13H        ;wheels counter
;..............................................................
; end of declarations- code start
```

```
;..............................................................
; BEGIN CODE
;..............................................................
         org    0h         ;begin code

;..............................................................
;SUBROUTINE AREA- MUST BE LOCATED IN PAGE ZERO
;..............................................................
; *** check keyboard subroutine
; if current column is source of key pressed will return
; with non zero value- "row"- calling routine check zr
; immediately on return
; entry: w contains column value for port
; exit : w contains row value (zero if incorrect column)
;
CHKKB  MOVWF  RB          ;output value in w to port b
       NOP                ;wait a bit
       NOP                ;wait a bit
       NOP                ;wait a bit
       NOP                ;wait a bit
       MOVF   RB,W        ;get input value
       ANDLW  0F0H        ;mask high only
       RETLW  0           ;return- real
;*** end check keyboard

; subroutine- keyboard read
; main routine- scans keyboard, and checks low battery input
; builds value "key" which is output by main routine each tick
; entry:   none
; exit :   key value built to key variable
;
; first check for any key
KEYRD  MOVLW  000H        ;preload key variable with 0
       MOVWF  KEY         ;store in key
       MOVLW  0F0H        ;setup tris for outs on low bits
       TRIS   RB          ;put in tristate latches
       MOVLW  00FH        ;put all highs on low nibble
       MOVWF  RB          ;output on port
       NOP                ;wait a bit
       NOP                ;wait a bit
       NOP                ;wait a bit
       MOVF   RB,W        ;input from port to W
       ANDLW  0F0H        ;get high nybble- inputs
       BTFSC  STATUS,ZR   ;if zero is clear then key
       GOTO   NOKEY       ;no keys- clear wheels & process PFI
; a key is being pressed continue
       MOVWF  KEY         ;stash row in key for now (one bit set)
       SWAPF  KEY,F       ;swap nibbles to low nybble
; determine column of key - row has been stored in key variable
       MOVLW  00H         ;prestash col value
       MOVWF  TEMP        ;stash value in column variable
       MOVLW  01H         ;load high on bit 0 only
       CALL   CHKKB       ;output value and check inputs
       BTFSS  STATUS,ZR;if zero is clear then key
       GOTO   COLFND

       MOVLW  004H        ;prestash column value
       MOVWF  TEMP        ;stash value in column variable
       MOVLW  02H         ;load high on bit 1 only
       CALL   CHKKB       ;output value and check inputs
       BTFSS  STATUS,ZR ;if zero is clear then key
       GOTO   COLFND

       MOVLW  008H        ;prestash column value
       MOVWF  TEMP        ;stash value in column variable
       MOVLW  04H         ;load high on bit 2 only
       CALL   CHKKB       ;output value and check inputs
       BTFSS  STATUS,ZR ;if zero is clear then key
       GOTO   COLFND

       MOVLW  00CH        ;prestash column value
       MOVWF  TEMP        ;stash value in column variable
       MOVLW  08H         ;load high on bit 3 only
       CALL   CHKKB       ;output value and check inputs
       BTFSS  STATUS,ZR ;if zero is clear then key
       GOTO   COLFND

; column found- subroutine jumps here if column makes row high

; format key variable
COLFND INCFSZ WHLS,F      ;increment wheels variable
       GOTO   CCOL        ;continue
       DECF   WHLS,F      ;keep wheels at FF if large
CCOL   MOVLW  0FFH        ;load loop counter for row decode
       MOVWF  LPCTR       ;store in loop counter
RWLP   INCF   LPCTR,F     ;pre-dec loop variable- top
       BCF    STATUS,CY ;clear carry
```

RB1-RB4 (along with the rest of the byte), enables the latch (IC1), and issues an interrupt. If no key was pressed, the key code is all "0"s on RB0-RB4 (otherwise RB0 is a "1").

The duration of each contact also is measured by the PIC. A minimum 32-ms interval (two scans or ticks) verifies a valid closure and debounces the contacts. Closure duration is encoded as 0 to 1 tick, 2 to 10 ticks (<0.16 seconds), 10 to 20 ticks (0.16 to 0.32 seconds), or >20 ticks (>0.32 seconds), and returned to the system as data bits RB5 and RB6. This data enables the main processor to provide an auto-repeat function for the keypad.

Finally, the crystal-accurate 16-ms interrupts provide a time base for the processor that eliminates the need for a separate time-base generator and crystal. Other advantages (over the discrete CMOS MSI approach) include: flexibility—the software allows for easy changes in the keyboard code, auto-repeat time, debounce delay, interrupt rate, etc.. Board space—the PIC is available in a surface-mount package and IC3 comes in a tiny shrink SO-8 "µMax" package. Cost and reliability—the PIC uses a standard AT crystal instead of the fragile 32-kHz-type otherwise required.

```
        RRF     KEY,F       ;rotate row value mask n times
        BTFSS   STATUS,CY   ;if bit set then stop
        GOTO    RWLP        ;loop til found
        BCF     STATUS,CY   ;clear carry
        MOVF    LPCTR,W     ;get value- 0 to 3
        ADDWF   TEMP,W      ;add column value
        MOVWF   KEY         ;stash in key
        INCF    KEY,F       ;inc (1 to 16) 0 = none

;
; formatted key value stored- handle debounce and wheels
; Debounce - key must be held down for 2 samples- uses wheels count
; key held- count time held and or in mask with key for length
; wheels initialized at 234 and counts up- always incremented
;
; Note: code segment has hard coded values for auto-repeat
;       in place, bad form - assembler doesn't handle
;       arithmetic correctly in equates. Be careful if changed.
;
; debounce first
        BCF     STATUS,CY   ;clear carry
        MOVLW   0H          ;preload low wheels mask
        MOVWF   TEMP        ;stash
        MOVF    WHLS,W      ;make copy of wheels
        MOVWF   LPCTR       ;copy for trial subtractions
        MOVLW   235         ;normalize
        SUBWF   LPCTR,F     ;subtract to f 0-20
        BTFSS   STATUS,CY   ;check carry- set if >
        GOTO    NOKEY2      ;wait for next samp- return zero

; now check to see if zero- this is a new key
        BTFSC   STATUS,ZR   ;level one if now zero
        GOTO    WHLSDN      ;done. wheels = 0 but valid key

; do second level wheels- sub more
        MOVLW   20H         ;preload first wheels mask (1)
        MOVWF   TEMP        ;stash
        MOVLW   8           ;sub 8 more since valid
        SUBWF   LPCTR,F     ;subract result to f
        BTFSS   STATUS,CY   ;check carry- if set greater
        GOTO    WHLSDN      ;wheels done

; do third level wheels- sub more
        MOVLW   40H         ;preload mid wheels mask (2)
        MOVWF   TEMP        ;stash
        MOVLW   10          ;sub 10 more 11-21 total
        SUBWF   LPCTR,F     ;subract result to f
        BTFSS   STATUS,CY   ;check carry- if
        GOTO    WHLSDN      ;wheels done

; do fourth level wheels- sub more
        MOVLW   60H         ;must be hi wheels mask (3)
        MOVWF   TEMP        ;stash. fall through

WHLSDN  MOVF    TEMP,W      ;get mask value
        IORWF   KEY,F       ;or in and store in f
        GOTO    KBREX       ;exit- jump over reinit whls

;no row and column being pressed- reinit key timer whls
NOKEY   MOVLW   233         ;wheels init value- 20 ticks (preinc)
        MOVWF   WHLS        ;store and fall through to exit

;row and column but key value 0 because debounce not expired
NOKEY2  CLRW                ;clear w- first sample
        MOVWF   KEY         ;put out on key- will wait additional

; check low battery input, put in place and exit- done
KBREX   BTFSS   RA,PFI      ;check power fail input (low if low)
        BSF     KEY,7       ;set high bit if pfi is low
        RETLW   0           ;done

;*************************************************************
; END OF ALL SUBROUTINES
;*************************************************************

;*************************************************************
; NORMAL CODE- HIGH PAGE
;*************************************************************
        ORG     100H            ;high page normal code

START   CLRW                    ;clear ports preload
        TRIS    RB              ;set up TRIS B- all active
        TRIS    RA              ;set up TRIS A- some in some out
        MOVLW   235             ;wheels init value- 20 ticks (preinc)
        MOVWF   WHLS            ;store and fall through to exit
        MOVLW   0DH             ;init port a
        MOVWF   RA              ;output it- irq high
;
; system initialized
;
;
; prescale value for RTCC = 32
; with 2.048 mHz crystal, clock is 512kHz
;
; loop runs every 256 clocks/prescale value or 2kHz/prescale
; prescale of 64 gives 62.5 Hz freq or 16 ms tick rate
; this is rate that irq's are generated and basic kb scan rate
; note that key must be held for full 16 ms min to be "noticed"
; this is the debounce value

MAINLP  MOVLW   04H             ;option register- rtcc and 32 prescale
        OPTION                  ;put in option register

; basic paced loop structure- no interupts available!

; top of timing loop- wait for high bit of RTCC to go hi
WTBHI   BTFSS   RTCC,7          ;check timer count- high bit
        GOTO    WTBHI           ;hang til timer bit 7 high

; RTCC high bit just went high- read keyboard
        CALL    KEYRD           ;read keyboard

; wait for RTCC high bit to go low- output values

; keeps jitter and latency down to zero
WTBLO   BTFSC   RTCC,7          ;wait timer low again
        GOTO    WTBLO           ;hang til timer bit 7 low

        MOVLW   0H              ;make port b an output
        TRIS    RB              ;to TRIS register
        MOVF    KEY,W           ;get key value
        MOVWF   RB              ;put on on port
        BSF     RA,LATCH        ;high on 574 clock- kachunk
        BCF     RA,LATCH        ;high on 574 clock-
        MOVLW   0F0H            ;setup TRIS again for outs on low bits
        TRIS    RB              ;put in tristate latches
        BCF     RA,IRQ          ;low on irq output
        NOP                     ;irq response time?
        NOP                     ;irq response time?
        BSF     RA,IRQ          ;high on irq output- bigger kachunk
        GOTO    WTBHI           ;back to main loop

        ;Would prefer to jmp to mainlp but option write- resets prescaler.
        ;This causes small error in irq timing- future modification
        ;See databook on electrically noisy environments for issues.

;*************************************************************
; end of code
;*************************************************************
```

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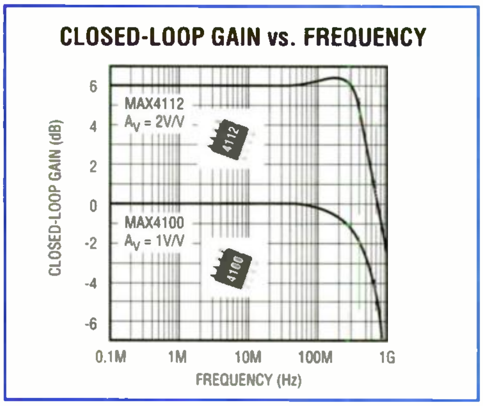

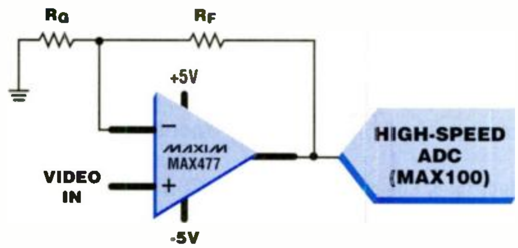

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† Notes: V_S = ±5V, R_L = 100Ω, f_c = 5MHz. †† 1000-up suggested resale single channel op amps, FOB USA.

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MAY

IEEE International Conference on Neural Networks (ICNN '98), May 3-9. Anchorage, AK. Contact Patrick K. Simpson, Scientific Fishery Systems Inc., P.O. Box 242065, Anchorage, AK 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@akaska.net.

IEEE World Congress on Computational Intelligence, May 3-9. William A. Egan Civic and Convention Center, Anchorage, AK. Contact Patrick K. Simpson, Scientific Fishery Systems Inc. P.O. Box 242064, Anchorage, AK 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@alaska.net.

Seventh IEEE International Fuzzy Systems Conference, May 3-9. Anchorage, AK. Contact Patrick K. Simpson, Scientific Fishery Systems Inc., P.O. Box 242065, Anchorage, AK 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@alaska.net.

IEEE/IAS Industrial & Commercial Power Systems Technical Conference (I&CPS), May 4-7. Edmonton, Alberta, Canada. Contact Marty Bince, Modicon Canada Ltd., 5803 86th St., Edmonton, Alberta T6E 2X4, Canada; (403) 468-6673; fax (403) 468-2925.

IEEE Radar Conference, May 12-14. Contact Scott Ramey, 2501 West University, MS 8056, McKinney, TX 75070; (972) 952-4409; fax (972) 952-3071; e-mail: sramey@ti.com.

IEEE International Conference on Acoustics, Speech & Signal Processing (ICASSP '98), May 12-15. Seattle Convention Center, Seattle, WA. Contact Les E. Atlas, Dept. EE (FT 10), University of Washington, Seattle, WA 98195; (206) 685-1315; fax (206) 543-3842; e-mail: atlas@ee.washington.edu.

IEEE International Conference on Robotics and Automation, May 16-21. Katholieki Universiteit, Leuven, Belgium. Contact Georges Giralt, LAAS-CNRS, Toulouse, France, +33 61-33-63-48; fax +33 61-33-64-55; e-mail: giralt@laas.fr.

IEEE Power Electronics, Specialist Conference (PESC '98), May 17-22. Sea Hawk Hotel & Resort, Fukuoka, Japan. Contact Tsutomu Ogata, NTT Integrated Information & Energy Systems Labs., Midori-cho, Musashino, 180 Japan; +81 422-59-2350; fax +81 422-59-2347; e-mail: ogata@ilab.ntt.jp

IEEE Vehicular Technology Conference (VTC), May 18-21. Westin Hotel, Ottawa, Ontario, Canada. Contact Tara Hennessy, Industry Canada, 300 Slater St., Ottawa, Ontario, K1A OC8, Canada; (613) 990-4711; fax (613) 952-5108; e-mail: hennessytara@ic.gc.ca.

48th IEEE Electronic Components & Technology Conference (ECTC '98), May 25-28. Sheraton Hotel & Towers, Seattle, WA. Contact Components Group, EIA, 2500 Wilson Blvd., Arlington, VA 22201; (703) 907-7536; fax (703) 907-7501; e-mail: judya@eia.org.

IEEE International Symposium on Circuits & Systems (ISCAS '98), May 31-June 3. Monterey Conference Center,Monterey, CA. Contact Sherif Michael, Department of Electrical & Computer Engineering, Naval Postgraduate School, Monterey, CA 93943; (408) 656-2252; fax (408) 656-2760; e-mail: michael@ece.nps.navy.mil.

JUNE

International Conference on Consumer Electronics (ICCE), June 2-4. Los Angeles Airport Marriott, Los Angeles, CA. Contact Diane Williams, Conference Coordinator, 67 Raspberry Patch Dr., Rochester, NY 14612-2868; (716) 392-3862; fax (716) 392-4397, e-mail: d.williams@ieee.org; www.icce.org.

IEEE/MTT-S International Microwave Symposium (MTT 98), June 7-12. Baltimore Convention Center, Baltimore, MD. Contact Steven Stitzer, Westinghouse Electric Corp., P.O. Box 1521, MS 3T15, Baltimore, MD 21203; (410) 765-7348; fax (410) 993-7747.

USENIX 1998 Technical Conference, June 13-17. Marriott Hotel, New Orleans, LA. Contact USENIX Conference Office, 22672 Lambert St., Suite 613, Lake Forest, CA 92630; (714) 588-8649; (714) 588-9706; e-mail: conference@usenix.org; www.usenix.org.

35th Design Automation Conference, June 15-19. Moscone Center, San Francisco, CA. Contact MP Associates, 5305 Spine Rd., Suite A, Boulder, CO 80301; (303) 530-4333; e-mail: dac-info@dac.com; www.dac.com.

JULY

IEEE International Geoscience & Remote Sensing Symposium (IGARSS '98), July 6-10. Sheraton Seattle, WA. Contact Tammy I. Stein, IGARSS Business Office, 2610 Lakeway Dr., Seabrook, TX 77586-1587, (281) 291-9222; fax (281) 291-9224; e-mail: tstein@phoenix.net.

IEEE Power Engineering Society Summer Meeting, July 12-16. Sheraton San Diego Hotel & Marina, San Diego, CA. Contact Terry Snow, San Diego Gas & Electric, P.O. Box 1831, San Diego, CA 92112; (619) 696-2780; fax (619) 699-5096; e-mail: t.snow@ieee.org.

SPIE's Annual Meeting & Optical Instrumentation Show, July 19-24. San Diego, CA. Contact SPIE Exhibits Dept., P.O. Box 10, Bellingham, WA 98227-0010; (360) 676-3290; fax (360) 647-1445; e-mail: exhibits@spie.org.

IEEE Nuclear & Space Radiation Effects Conference (NSREC '98), July 20-24. Newport Beach, CA. Contact Jim Schwank, Sandia National Laboratories, P.O. Box 5800, MS-1083, Albuquerque, NM 87185-1083; (505) 844-8376; fax (505) 844-2991; e-mail: schwanjr@sandia.gov.

AUGUST

AUTOTESTCON '98, Aug. 24-27. Salt Palace Convention Center, Salt Lake City, UT. Contact Robert Myers, Myers/Smith Inc., 3685 Motor Ave., Suite 240, Los Angeles, CA 90034; (310) 287-1463; fax (310) 287-1851; e-mail: bob.myers@ieee.org.

SEPTEMBER

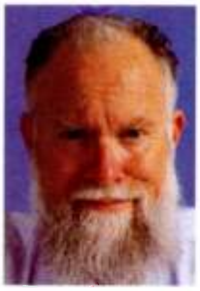
ICSPAT & DSP World Expo, Sept. 13-16. Toronto Metro Convention Center, Toronto, Ontario, Canada. Contact Liz Austin, Miller Freeman Inc., (888) 239-5563, (415) 538-3848, e-mail: dspworld@mfi.com; www.dspworld.com.

OCTOBER

The Vision Show, Oct. 6-8. San Jose Convention Center, San Jose, CA. Contact Automated Imaging Association (AIA), 900 Victors Way, P.O. Box 3724, Ann Arbor, MI 48106; (313) 994-6088; fax (313) 994-3338; e-mail: kerickson@automated-imaging.org; www.automated-imaging.org.

BOB PEASE

Bob's Mailbox



Hi Bob:

Hope all is well, and if you're on your trek, that you haven't fallen off a mountain trail. I've truly enjoyed reading your columns over the years. You seem to have that magic blend that most writers strive for—and the lucky ones reach. You are also a never-ending source of knowledge.

Having said that, I need to call upon your vast resources. Do you know of any listing of company logos that can help me identify who made a particular IC?

Usually, I'm pretty good at figuring out which company made what IC, and can scurry off to my data books, or the web to retrieve the relevant data sheet. But I've found one that has me stumped. The logo is a stylized letter, looking something like a cursive lowercase "d" in a circle with a flatted bottom—think Integrated Device Technologies, and you'd be close. I don't think they made it, though, as the part number (73K324L-28IH) doesn't match anything I could find.

So, great Guru of Arcania, can you point me to a logo listing that might help me in my quest? I shall remain ever-grateful, and promise not to bug you with trivial matters like this ever again! I had such a listing years ago, but lent it to someone who never gave it back. Boy, if I EVER see that guy again. . . Anyway, thanks, and I hope the pix you snap for the gentleman tethered to the kidney machine come out great.

JIM JERZYCKE
via e-mail

Just before we went to press, Mr. Jerzycke admitted that his technician observed, "That looks like the mark of Silicon Systems,"—and he was right. (Old D.A.T.A. book had good lists of semiconductor trademarks.)—RAP

Dear Bob:

In case you ever wondered why ignorance rises to the executive level, here is a simple explanation that is also mathematical proof:

Postulate 1: Knowledge is Power.

Postulate 2: Time is Money.

Physics teaches us the following formula for Power:

Power = Work/Time

If Knowledge = Power. And Time = Money (based on above postulates), then by substitution we get:

Knowledge = Work/Money

Solving for Money, we get:

Money = Work/Knowledge

Thus Money approaches infinity as Knowledge approaches zero, regardless of the work done. What this means is: The less you know, the more you make. I KNEW this could eventually be proven!

DENIS M. POIRIER
via e-mail

Hello, Denis. I love it! This is almost as good an argument as the question, "Which would you rather have, a crust of bread, or a hot roast-beef sandwich?"

Of course the correct answer is: "A crust of bread."

Why? Because everybody knows that a crust of bread is better than nothing, and nothing is better than a hot roast-beef sandwich.—RAP

Hi, Bob:

I've been thinking how (not so long ago) in the warm and fuzzy days of vacuum-tube equipment, we were accustomed to waiting for equipment to warm up before it could be used. Some equipment, like RF generators, took so long to stabilize, we left them on all the time. Then came analog solid-state equipment. It was ready to work instantly when you turned it on and off as needed.

But now that most everything is digital, you often have to wait for it to "boot up" instead of warm up. Recently, I had the privilege of learning how to use a fancy new audio analyzer. Just like a PC, you had to wait for it to go through a lengthy boot-up cycle.

(Not to mention the wonderful "self-calibration" cycle, one or more minutes?—RAP)

This wouldn't be so bad if you only had to do it once, but unfortunately, like a PC, it also had a habit of crashing without warning.

When it worked, it did a lot of nifty things. But it would occasionally just lock up—forcing you to power down and start all over again. There were other times when it would seem to be working, but not giving meaningful readings. The only solution, again, was to power down and reboot. Isn't progress wonderful?

KEN LUNDGREN
via e-mail

Yeah, computers are wonderful, except when they are trouble. Have you griped to the manufacturer? They may not respond, but at least you explained why you won't buy that brand of equipment again.—RAP

Dear Robert:

I read your article on Scrooge, and I remember playing a similar game with some friends. Their twist on the rules was that most "players" were teams of two, sitting adjacent to each other. One turned the cards while the other one played on the center. When I said "most," it was because one guy was so quick, and had such good vision and coordination, that his handicap was that he had to play alone against the teams of pairs. His day job? He was an air traffic controller.

BRUCE WALKER
via e-mail

Bruce your variation sounds very challenging, and we gotta try it. Yeah, our friend Willy could very well have been an ATC wizard, but he mostly wrote software.—RAP

All for now. / Comments invited!
RAP / Robert A. Pease / Engineer
rap@web team.nsc.com—or:

Address:
Mail Stop D2597A
National Semiconductor
P.O. Box 58090
Santa Clara, CA 95052-8090

Load-Correction Feature Hikes Accuracy Of LCR Meters

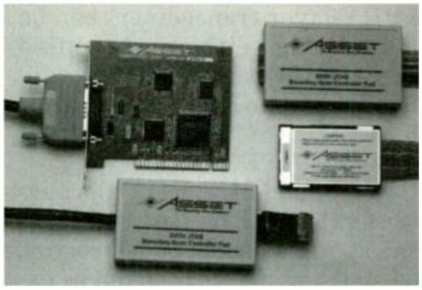
The 7400 Model B and 7600 Model B LCR meters include a new load-correction feature that improves measurement accuracy by using a calibrated device as a reference point to

correct for fixturing and cabling effects. Both instruments make frequency-swept measurements and provide graphical or tabular results to verify component or material response to changes in ac test frequency, voltage, or current without the need for complex programming or an external controller. The 7400 covers 10 Hz to 500 kHz, and the 7600 covers 10 Hz to 2 MHz. Both can measure and display any two of 14 impedance parameters, including inductance, capacitance, and resistance. The meters have a 3-1/2-in. floppy drive to store test results. They can run six different tests in sequence with varying conditions and limits. The 7400 Model B costs $8600, and the 7600 Model B costs $10,600. Delivery is in four weeks. JN

QuadTech Inc., 100 Nickerson Rd., Marlborough, MA 01752; (800) 253-1230; fax (508) 485-0295; Web: http://www.quadtechinc.com. **CIRCLE 590**

Controller Cards Bring JTAG To PCI and PCMCIA Hosts

A pair of controller cards for the PCIbus and PCMCIA interface expand the platform options available for users of IEEE-1149.1 (JTAG) boundary scan technology. The controllers allow boundary-scan test, diagnostics, and in-system programming systems like the company's ASSET product line to work on PCI-based hosts. Users can insert the cards into a standard PCIbus or PCMCIA slot. The appropriate cables connect the controllers to an ASSET pod, which in turn is connected to the user's unit under test. The pod ensures high



signal integrity over the four-wire JTAG boundary-scan path. Bundled with the ASSET Scan Developer system, the PCIbus controller costs $8995 and the PCMCIA version is $7995. JN

ASSET InterTech Inc., 2201 N. Central Expwy., Suite 105, Richardson, TX 75080-2718; (972) 437-2800; fax (972) 437-2826. **CIRCLE 591**

Instrument Acquires 30,000 Readings/s From Mixed Inputs

The SmartLink KNM-DCV12 data-acquisition instrument comes in configurations that accept up to eight single-ended, four differential, or two four-wire analog inputs. The device allows trade-offs between resolution and speed, delivering 12- to 16-bit resolution at from 5000 to 30,000 readings/s. All versions also have four digital I/O lines and one counter-timer input. If data speeds exceed that of the communications link to the host computer, an internal buffer can store up to 10,000 8-bit readings or 5000 16-bit readings. The unit accepts signals from various sensors and sources so voltage, resistance, RTD, thermistor, pressure, flow, weight, and digital information can be acquired by one device. Package size is only 1.1 by 1.3 by 6.7 in., and it can be linked to the host PC by several means, including Ethernet, RS-232, RS-422, RS-485, PCMCIA, USB, and modem. The instrument comes with the NetAcq startup software, which allows users to quickly start running. Prices for three to nine units start at $1215 for the KNM-DCV12 and from $896 for a one-channel version, the KNM-DCV11. Delivery is in one to two weeks. JN

Keithley Instruments Inc., 28775 Aurora Rd., Cleveland, OH 44139-1891; (888) 534-8453; (440) 248-0400; (440) 248-6168; e-mail: product_info@keithley.com; or on the Internet at: http://www.keithley.com. **CIRCLE 592**

Data-Acquisition Boards Get Windows 95/NT Drivers

Windows 95/NT drivers are now available for the PCI-20000 series of data-acquisition boards. The MasterLink 32 Library (part number PCI-20485S-1) supports all of the company's plug-in data-acquisition boards and comes free with the most popular units. The drivers allow users to develop native 32-bit acquisition and control applications that take advantage of the power and security features of Windows NT. Simple high-level commands are accepted by the drivers and appropriate hardware commands are sent from a kernal-mode driver under Windows NT or a VxD driver under Windows 95. MasterLink supports the most popular programming languages and compilers, and its API is identical to the MasterLink Libraries for DOS and Windows 3.x. Complete documentation and sample programs are included. The MasterLink 32 Library costs $300. An upgrade version (part number PCI-20458S-1U) for users of the DOS and Windows 3.x products costs $100. JN

Intelligent Instrumentation Inc., 6550 S. Bay Colony Dr., MS130, Tucson, AZ 85706; (800) 685-9911; (520) 573-0887; fax (520) 573-0522; e-mail: sales@instrument.com; or on the Internet: http://www.instrument.com. **CIRCLE 593**

Power Meter Displays Four Parameters At Same Time

The CP-210A digital power meter supplies simultaneous LED readouts of voltage, current, watts, and frequency. Dividing the watts readout by voltage times current provides the power factor of the unit under test. The instrument is suitable for testing switching power supplies, uninterruptible power supplies, and other equipment powered by an ac input. The meter measures inputs from 40 Hz to 5 kHz with two manually selected voltage ranges (300 or 600 V RMS) and three automatically selected current ranges (0.3, 3, and 30 A RMS). Wattage readings also are auto-ranging, to 9000 W (300 V) or 18,000 W (600 V). The meter measures 10.2 by 4.33 by 13.7 in. The CP-210A costs $615. JN

Technology Dynamics Inc., Mid-Eastern Industries Div., 100 School St., Bergenfield, NJ 07621; (201) 385-0500; fax (201) 385-0702. **CIRCLE 594**

Comm-Centric FPGAs Sport ATM Cores, RAM, And FIFOs

Custom FPGA-based communication applications now can be developed rapidly using a series of embeddable logic cores, memory, and FIFOs. The cores are pre-coded, pre-tested, and pre-verified building blocks that include an ATM physical-layer UNI 3.1 interface and an ATM UTOPIA I/II interface. Both functions can be integrated into the OR2CxxA family of FPGAs with other cores, such as synchronous or dual-port RAM, or a 4-by-1 signal processing multiplier.

Intended to support ATM traffic at speeds up to 155.52 Mbits/s, the UTOPIA core can accommodate 8- or 16-bit parallel data at clock rates of up to 50 MHz. It performs parity generation and checking for level I and II interfaces, as well as support for all multi-PHY modes. The physical-layer core complies fully with UNI 3.1 and features cell header detection and correction, cell payload scramble/descramble, idle cell insertion, out-of-cell and loss-of-cell delineation, and user-programmable cell filtering. Both cores can be implemented with either on-chip or off-chip FIFOs

All cores are supported by standard synthesis and simulations tools, as well as the ORCA foundry FPGA layout software. The design package for each core consists of VHDL source code, a VHDL test bench, scripts, and data files for behavioral and gate-level simulation, synthesis, and layout.

Available now, pricing is $30,000 for the ATM physical layer, and $7000 for the UTOPIA interface. LG

***Lucent Technologies Microelectronics**, Room 30L-15P, 555 Union Blvd., Allentown, PA 18103; (800) 372-2447 - Dept. R41; fax (610) 712-4106.*
CIRCLE 595

8-Port 10/100 Ethernet MAC Supports Flow Control, VLANs

The MAC8110 is an eight-port media access controller (MAC) intended for use in multiport network equipment such as bridges, switches, and repeaters. Each of the chip's eight ports has its own set of dual-port transmit and receive FIFOs and can implement full- and half-duplex flow control on a per-port basis. Connections to PHY-layer transceivers can be made through either a simplified seven-wire interface for low cost 10-Mbit/s applications, or via a standard 16-bit MII for autonegotiating 10/100-Mbit/s PHYs.

A 64-bit, 66-MHz FIFO permits transfers between the host and its network at over 4 Gbits/s. Status, control, and statistics information can be exchanged with the host system using the controller's 32-bit PCI bus interface. With an eye towards the future, the controller also supports large packets for VLAN tagging.

Developing managed solutions with the MAC8110 is easy and inexpensive because the controller collects a full set of CMIB statistics to support RMON functions. In addition, the controller's receive frame statistics can be appended as a 64-bit data word at the end of a frame and passed to the host via the FIFO interface. Other advanced features include programmable-sized data bursting for efficient packet transfer and half-duplex flow control using carrier sense deferral. Most major IEEE Ethernet standards are supported, including 802.3i, 892.3u, 802.3x, 802.3y, and 802.3, as well as ANSI's 8802-3 specifications.

Available now, the MAC8110 is packaged in a 352-pin BGA. Pricing is $40 each in small quantities, with discounts for larger orders. LG

***Oki Semiconductor**, 785 North Mary Ave., Sunnyvale, CA 94086-2909; (408) 720-1900; faxback: (USA) (800) OKI-6994, (Canada and Mexico) (609) 222-9716; http://www.okisemi.com.*
CIRCLE 596

10/100 Ethernet Switch Chips Handle RMON, QoS, And VLANs

The Xpress Flow 2001 series of 10/100 Ethernet switch chips and software employs a flexible architecture that enables designers to quickly develop custom products with advanced features. The programmable packet processor can support four levels of quality of service (QoS) control, perform full-duplex flow control, and implement other functions used in next-generation networks and VLANs. Engineered to support both Level 1 and 2 standard VLANs, the chip set can perform the tagging used to communicate between switches.

Thanks to its scalable architecture, the Xpress 2001 components can be used to construct a wide range of network products, ranging from an eight-port unmanaged Ethernet switch to a fully managed, 32-port switch with 24 Ethernet ports and eight Fast Ethernet ports. Using pre-developed software, designers also can incorporate SNMP and RMON capabilities into their products.

The Xpress 2001 chip set will be sampling during the fourth quarter of this year. Pricing will be $10 per Ethernet port and $30 per Fast Ethernet port, in quantities of 10,000. LG

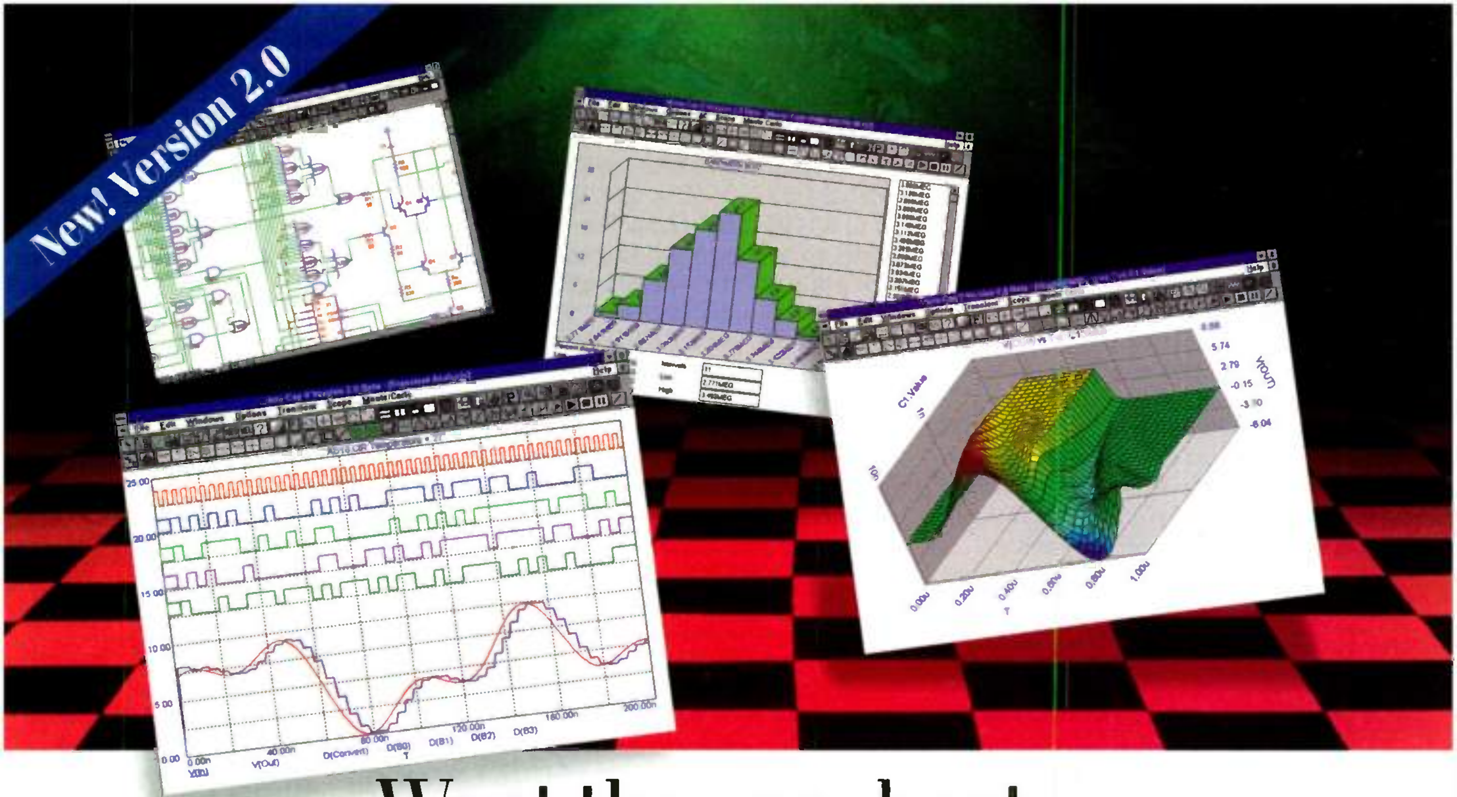
***Vertex Networks Inc.**, 16842 Von Karman Ave., Irvine, CA 92606-4950; (714) 252-8880; fax (714) 252-8868, http://www.vertex-networks.com.*
CIRCLE 597

PCI-Based ATM Adapter Has Hardware-Based ABR Logic

Intended for high-performance applications with mixed traffic types, the 5575 PCI-based, 155-Mbit/s ATM adapter features a highly optimized architecture and advanced traffic management features. Available in configurations for driving either Fiber or UTP, its hardware-based traffic-management logic allows it to respond quickly to changing network congestion. The custom-designed SAR complies with the ATM Forum's latest (4.0) traffic-management specification.

The card also can simultaneously handle multiple streams of available-bit-rate (ABR) and constant-bit-rate (CBR) traffic. Cell scheduling is performed on a per-VC basis for maximum utilization of available bandwidth. Packets are shipped across the host PCI bus in 128-byte bursts and can be reassembled either on or off the board. Advanced setup and management software makes configuring and troubleshooting the 5575 quick and easy. Drivers for most major operating systems (Windows, Netware, Apple, AIX, and Sun) are packaged with the software. Available now, pricing for the 5575 begins at $850 each, with discounts for higher volumes. LG

***Interphase Corp.**, 13800 Senlac, Dallas, TX 75234-8823; (214) 654-5000, fax (2140 654-5507; Internet: http://www.iphase.com.* **CIRCLE 598**



Want the very best in Analog/Digital simulation? Introducing Micro-Cap V Version 2.0

Micro-Cap V is a fast, precision, 32-bit analog/digital simulator with an intuitive fifth generation user interface, and a library of more than 10,000 pre-modeled parts. Based on Spice3 and PSpice™ it offers the best features and capability of both.

Its finely crafted simulation tools include schematic probing, during the run plotting, performance plots, 3D plots, multidimensional stepping, analog and digital behavioral modeling, an optimizing model generator, and Monte Carlo analysis. Compiled models, behavioral primitives, and a huge library of commercial parts make modeling of both analog and digital devices easy. New devices in Version 2.0 include BSIM 1.0, 2.0, and 3.3, sample and holds, Z transforms, and three new animation devices.

Download the free working demo at www.spectrum-soft.com.

We offer the very best in analog/digital simulation and we guarantee it with a 30 day money back guarantee!

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Features

Feature	
Mixed Analog/Digital	Yes
Analog Engine	Spice3 & PSpice™
Digital Engine	Native PSpice™
During the Run Plots	Yes
Analog/Digital Primitives	200+
Analog/Digital Parts	10,000+
Performance Plots	Yes
Parameter Stepping	Multidimensional
Optimizing Parts Modeler	Yes
3D Plots	Yes
Schematic Probing	Yes
Behavioral Modeling	Analog & Digital
Monte Carlo	Yes
Device Temperatures	Individually Set
BSIM Devices	Yes. 1.0, 2.0, and 3.3
Animation Devices	Yes
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Guarantee	30 Day Money Back
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Signal-Switching ICs Use Minimum Power

Four dual analog switches from Maxim Integrated Products are intended for use in battery-operated equipment. The MAX4541 has two normally open switches, the MAX4542 has two normally closed switches, and the MAX4543 has one normally open and one normally closed switch. The three ICs come in 8-pin DIP and SO packages. The MAX4544 also offers a SPDT configuration in a 6-pin SOT-23 package.

Power consumption for all switches is 5 µW, and maximum leakage current is 100 pA at 25°C and 2.5 nA at 85°C. Maximum on-time is 150 ns and off-time is 100 ns. Maximum charge injection is guaranteed at 5 pC, and all switches have a 2-kV protection against electrostatic discharge per Method 3015 of MIL-STD-883. Operating supply voltage is 2.7 to 12 V. When operating on 5 V, they exhibit a maximum on-resistance of 60 Ω (33 Ω typical), maximum 2-Ω matching between channels, and a 6-Ω on-resistance flatness over the analog input range. All control inputs are TTL/CMOS-compatible, and the MAX4543 and MAX4544 have guaranteed break-before-make switching. Available for the commercial and extended industrial temperature ranges, the switches have a starting price of $0.41 each in quantities of 1000. ML

***Maxim Integrated Products**, 120 San Gabriel Dr., Sunnyvale, CA 94086; (408) 737-7600.* **CIRCLE 599**

Full-Duplex Chip Set Forms WLAN Transceiver

The PRISM chip set comprises eight ICs that form a full-duplex, heterodyne receiver/transmitter with automatic gain control for wireless local-loop systems carrying voice and data signals. Operating in the carrier-frequency range of 1.7 to 2.7 GHz, the chip set performs amplification, downconversion demodulation, modulation, and upconversion. Its high bandwidth supports both voice and ISDN signals. Applications include wireless local-loop subscriber terminals and base stations, point-to-point microwave, wireless T1 and E1 links, and handheld data transceivers. All chips operate on power supplies from 2.7 to 5.5 V.

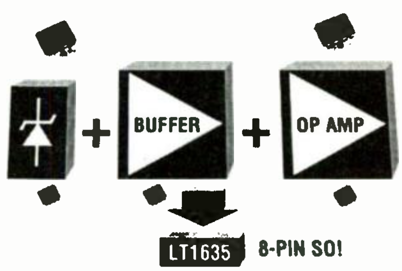
For receiver functions, there's a choice of two low-noise amplifiers: the HFA3424 (2.3 to 2.7 GHz) and HFA3421 (1.7 to 2.3 GHz). Both amplifiers have a 1.9-dB noise figure, 14-dB gain, consume 5 mA, and are each packaged in an 8-lead SOIC. Packaged in a 20-lead SOIC, the HFA3661 RF/IF downconverter operates across frequency ranges of 2.0 to 2.7 GHz and 10 to 400 MHz. The mixer provides an 11-dBm third-order intercept point and 23-dB conversion gain across the RF range. Baseband I and Q quadrature demodulation are provided by the HFA3761 demodulator, which integrates all IF and AGC functions. Operating from 10 to 400 MHz, it comes in an 80-lead TQFP.

The transmit chain includes the HFA3763 quadrature modulator with selectable low-pass shaping filters. Its 400-MHz AGC amplifier/attenuator range is 45 dB. Packaged in a 20-lead SSOP, the chips deliver a 6-dBm output and 1-dB compression. The last chip in the transmit chain is the HFA3926, a 2.0- to 2.7-GHz RF power amplifier with +28-dB gain and housed in a 28-lead SSOP. The chip set is completed with two HFA3524 dual synthesizers that generate RF and IF local-oscillator signals for the receive and transmit chains. Chip-set pricing is $56 in quantities of 100,000. ML

***Harris Corp.**, Semiconductor Sector, Melbourne, FL 32902-0883; 1-800-4-HARRIS.* **CIRCLE 600**

Small Rail-To-Rail Op Amp Includes Built-In Reference

Linear Technology's LT1635 rail-to-rail op amp comes in an SO-8 package and includes a precision voltage reference. It has an offset voltage of 1.3 mV (max), and the 200-mV reference voltage guarantees a maximum 100 ppm/°C drift. The part can operate from a single supply as low as 1.2 V, or from up to ±5 V using split supplies. It consumes 130 µA of supply current.



LT1635's input common-mode range includes ground and incorporates reversal protection to prevent false outputs from occurring when the input is below the negative supply. Gain bandwidth is 175 kHz, and the part is unity-gain stable with up to 1000-pF load capacitance. The LT1635 is available in volume in eight-lead SO and PDIP packages. Pricing starts at $1.85 in quantities of 1000 or more. LM

***Linear Technology Corp.**, 1630 McCarthy Blvd., Milpitas, CA 95035-7417; (408) 432-1900 or (800) 4-LINEAR; www.linear-tech.com.* **CIRCLE 601**

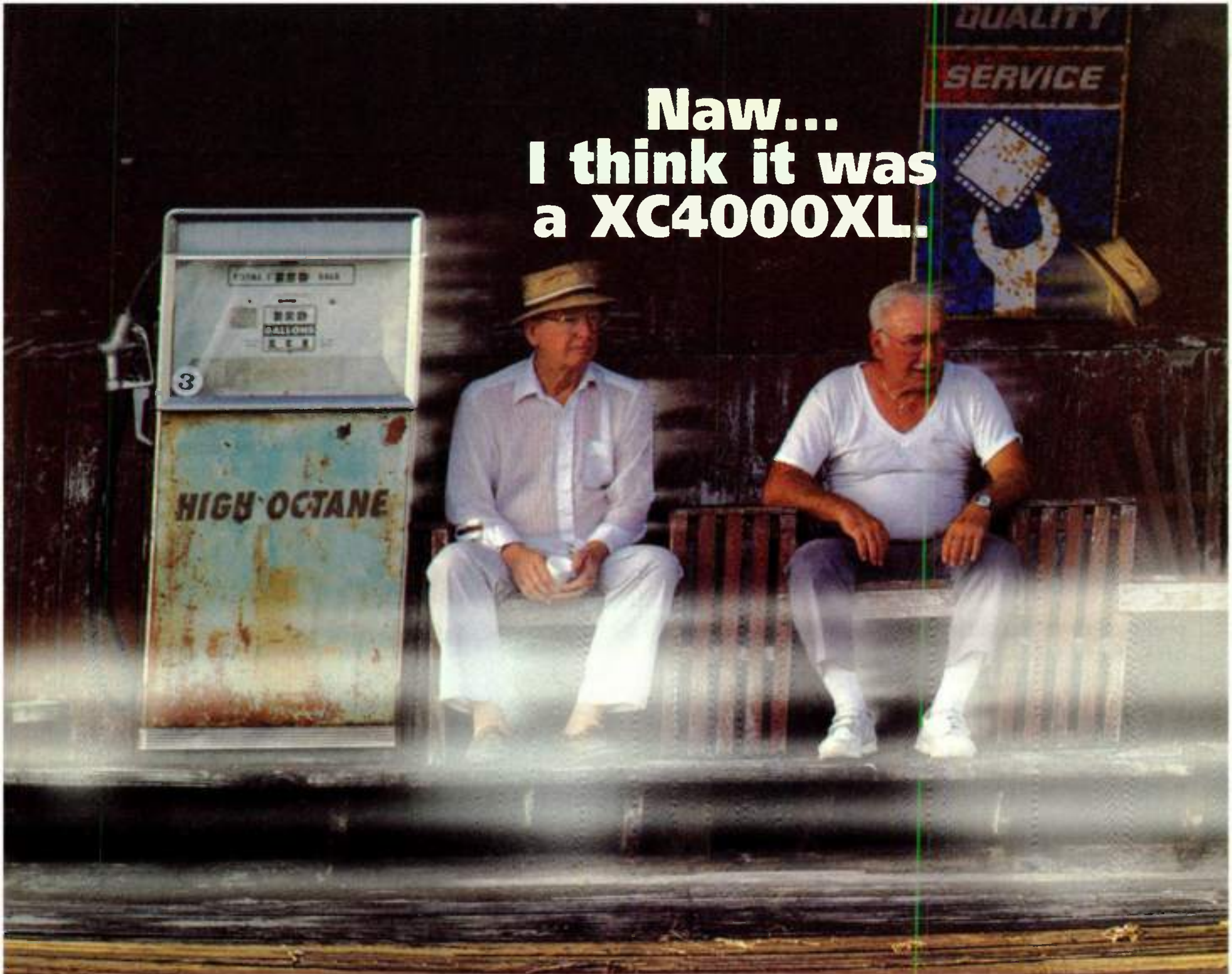
Tiny, Low-Voltage Op Amp Features Rail-To Rail I/O

The new OPA340 series of rail-to-rail CMOS op amps is optimized for low-voltage, single-supply operation. Rail-to-rail I/O and high-speed operation suit the part for driving sampling

ADCs. It's also very good for portable and audio applications. The OPA340 op amp runs on a single supply as low as 2.5 V with an input common-mode range that extends 500 mV beyond the negative and positive supplies. Output voltage swings to within 1 mV of the supply rails. The part offers a bandwidth of 5.5 MHz and SR of 6 V/µs, yet quiescent current is just 750 µA.

Single, dual, and quad versions are available in SOT-23-5, MSOP-8, and SSOP-16 surface-mount packages, respectively. The single and dual versions come in standard 8-pin DIP and SO-8 surface-mount packages. The quad version also is available in 14-pin DIP and SO-14 surface-mount packages. The OPA340 costs $0.46 in 100,000 quantities. Delivery is from stock. LM

***Burr-Brown Corp.**, P.O. Box 11400, Tucson, AZ 85734; (520) 746-1111 or (800) 548-6132; or on the web at www.burr-brown.com/.* **CIRCLE 602**



All across America the XC4000XL family is turning heads. Why? Performance. The kind of lightning fast speed you've come to expect only from a gate array. But now you can get that same performance in a high density programmable logic device. Plus all the inherent flexibility that's made Xilinx FPGAs the "time-to-market" choice of thousands of leading system designers.

180,000 gate XC4085XL with super high-performance. Available now!

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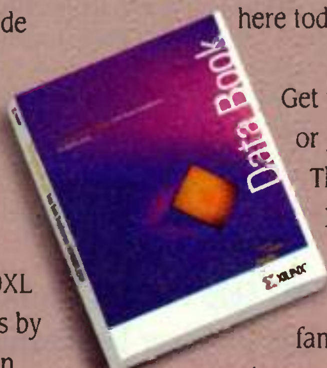
The XC4000XL family. They're fast, they're packed with logic, they're 3.3 volts and they're here today.



Don't be left sitting in the dust. Get the whole story at www.xilinx.com, or give one of our distributors a call. They'll send you a copy of our XC4000XL Data Book Supplement. Then you'll know why people are saying that the XC4000XL family is "quicker than a barefoot tapdancer in a room full of rattlesnakes."

*XC40125 on 0.25 micron geometry

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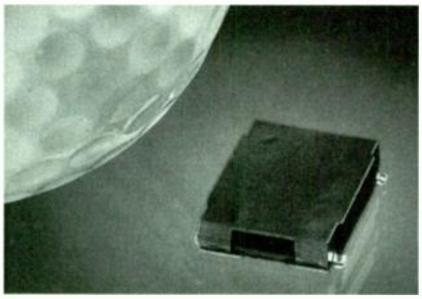
Surface-Mount Audio Transducers Lay Low

A family of low-profile surface-mount audio transducers are just 3 mm high, and have a footprint measuring 11 mm by 13 mm. The transducers feature a

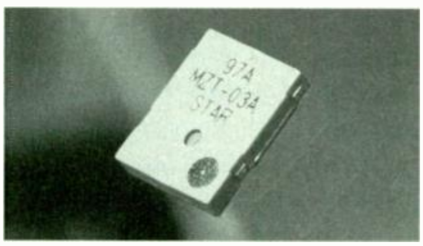


preliminary rating output of up to 96 dBA. Three models (SMT-831, SMT-833, and SMT-835) are respectively rated at 1.5, 3, and 5 V p-p. All have a side firing sound port. They are compatible with convection, IR, and vapor phase surface-mount assembly, and are available in tubes or reels. Sample quantities are shipped from stock, while production quantities are eight weeks ARO. Call for pricing. LM

Projects Unlimited Inc., *3680 Wyse Rd., Dayton, OH 45414-5802; (937) 890-1918; e-mail: sales@pui.com.*
CIRCLE 603

SMT Audio Transducers Are Compact And Lightweight

The MZT-03A surface-mount audio transducer is compact and lightweight, making it well suited for wire-

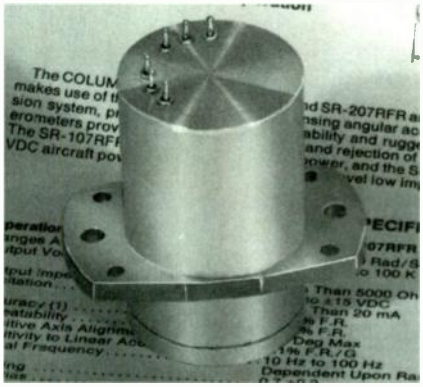


less telecommunications equipment. Its structure and housing allow for the reflow process. The part weighs 0.5 g and measures 10 mm wide by 12 mm long by 2 mm high. Sound output is 83 dB minimum at 10 cm, with a frequency of 2670 Hz. It operates at 3.6 V maximum between –20°C to +60°C. The MZT-03A transducer is available in tape-and-reel packaging for mass assembly and production needs. Call the company for pricing and availability information. LM

Star Micronics America Inc., *70-D Ethel Rd. West, Piscataway, NJ 08854; (800) STAR-OEM or (908) 572-9512; www.starmicronics.com.*
CIRCLE 604

Users Select The Range On Angular Accelerometer

The Model SR-107VFR angular accelerometer lets users change the scale factor and range to obtain optimum ac-



curacy and readout match. Full measurement range is adjusted from ±1 to ±100 radians/s^2 with a single external resistor change. And because virtually all angular acceleration measurements are either transitory or periodic, users also can select a dc blocking option and define the associated cutoff frequency. The accelerometer uses force balance fluid rotor technology, which produces high-level output with good accuracy, stability, and linear acceleration rejection. Call for information on pricing and availability. LM

Columbia Research Laboratories Inc., *1925 MacDade Blvd., Woodlyn, PA 19094; Robert R Reymos, (800) 813-8471 or (610) 872-3900; or at www.columbiaresearchlab.com.*
CIRCLE 605

SMT Chip Thermistors Have Gold Or Silver Terminations

Choose from either gold or silver terminations with the new NTC chip thermistors from Victory Engineering. The surface-mount thermistors meet MIL-R-23646 and MIL-STD-883 requirements, and mount on numerous substrates, such as ceramic, glass, epoxy, plastic, and fiberglass. Applications for the NTC thermistors include cellular phone, personal computer, and instrumentation designs.

Gold-terminated chips are designed for thermocompression and/or ball bonding, and may be mounted to the

substrate or printed circuit by epoxy bonding or soldering. Both gold and silver types feature long-term stability, fast response, and top and bottom electrodes. The chips are manufactured in 12 thermistor materials, and are available in values ranging from 50 Ω to 20 MΩ at 25°C. Pricing for the NTC chip thermistors starts at $2.75 each in quantities of 1000. Delivery is from stock to six weeks. LM

Victory Engineering Corp., *Victory Rd., Springfield, NJ 07081; (973) 379-5900.* **CIRCLE 606**

Miniature Absolute Pressure Sensor Boasts Low Cost

A new series of miniature absolute pressure sensors work very well in applications requiring highly accurate hysteresis, stability, and repeatability. The 24PC series of low-cost sensors offer three pressure-port configurations, and its package design incorporates a patented modular construction that withstands up to 60 psi. The low-power, unamplified Wheatstone bridge circuit design provides stable millivolt outputs over the 2-to-15 or 2-to-30 psi sensing ranges. Two termination styles are available: a four-pin inline and a two-by-two arrangement. Operating temperature range is –40ΥC to +85ΥC. List price is $15.65, and delivery is four to six weeks. LM

Honeywell Micro Switch Div., *11 W. Spring St., Freeport, IL 61032; (800) 537-6945; or on the web at: www.sensing.honeywell.com.*
CIRCLE 607

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Buyers Can Be Automatically Notified Of Product Changes

A common problem faced by manufacturers, distributors, and customers is how to disseminate or find notifications of changes to products. But a new service provided by the National Electronic Distributors Association (NEDA), in conjunction with Cogent Software, will automatically offer access to current data on product changes and obsolescence from multiple manufacturers.

When the Product Change Notification (PCN) service is fully operational, users can go to NEDA's web site, *www.nedassoc.org*, and set up their profile for automatic e-mail notification of the specific changes in which they are interested. Choices will include manufacturers, product types, and types of changes, which include obsolescence, molding, form/fit/function, shipping/packing materials, and others. Then, whenever the manufacturer posts a product change to the index, anyone requesting updates will receive an e-mail notice.

Users can click on a link in this e-mail to go to the specific PCN Index summary record. This record may include a link to the actual PCN if the manufacturer makes that information available online, a link to a list of distributor contacts, or a phone number to call for more information.

For more information, contact NEDA executive vice president Robin B. Gray Jr. at (312) 558-9114, e-mail: rgray@nedassoc.org; or Cogent Software at (800) 733-3380, e-mail: pcn@cogent.net.

Avnet Combines Canadian Units For A One-Stop Shop

A reorganization of Avnet Inc.'s Hamilton Hallmark, Pennstock, and Time Electronics operation into Avnet Canada results in the country's largest electronics distributor. Avnet Canada will offer more than 110 product lines and house technical specialists in semiconductors (interconnects, passives, and electromechanical) and RF and microwave communications. Other value-added services, such as integrated materials management, also are available.

"Customers want access to the broadest product offering possible. They want extensive technical support. And they want one source for both," says Steve Church, president of Avnet's OEM Marketing Group. He continues, "Avnet Canada seamlessly combines the resources of three of Canada's leading distributors into one convenient source."

Rochester Picks Up QSI's Discontinued Semiconductors

To ensure a continuing source of supply for customers, Rochester Electronics Inc., Newburyport, Mass., has agreed to buy all residual inventories of discontinued products from Quality Semiconductor Inc. (QSI). The agreement covers wafers as well as finished products. Tooling will also be available to Rochester, on a selected basis.

QSI designs, develops, and manufactures more than 1800 standard product variations in speed and package options aimed at networking, communications, and computer markets. Gil Jones, vice president of marketing at QSI, noted that discontinued products had become too important a customer-service issue to just put out an end-of-life notice and give customers a fixed amount of time to order. "We chose Rochester because they have made a business of what they call 'trailing-edge product,' and they are focused on continued service," Jones said.

Rochester's inventory includes devices from numerous leading semiconductor devices. The company can be reached at: (978) 462-9332; fax (978) 462-9512; www.rocelec.com.

Two Lines Added To Card At West Electronic Sales

West Electronic Sales has become the exclusive authorized representative for AMF Electronics and Arcoelectronics in southern California. AMF is a southern California-based contract manufacturer of custom and fabricated electronic products. The company recently expanded its capabilities to include turnkey assemblies for all outsourcing requirements. Arco, also based in southern California, manufactures lighted push-button switches and rocker switches. The two new lines join 13 other lines on West Electronic's card. For more information call (714) 375-0222.

Electro-Matic Products Wins Control Software Products

Electro-Matic Products Inc., Farmington Hills, Mich., has been named a distributor of a pair of control software products from Namatron Corp.'s NemaSoft subsidiary. The Paragon SCADA software supports 32-bit platforms with a client-server architecture, offering regulatory control solutions by enabling enterprise access to the plant floor. Paragon 5.0 is the first version to integrate components of the PC-based, open-architecture, control software, OpenControl—the other product now handled by Electro-Matic.

Paragon is used in a wide variety of process industries, including biotechnology, chemical, food and beverage, energy and building management, pharmaceutical, and textiles. The seamless integration of OpenControl as a fully distributed server creates a complete control solution.

Electro-Matic president Jim Baker said there is a high degree of synergy between his company and Nematron, in part because both focus on automation solutions for the automotive market. "The breadth of Nematron's new products will also allow us to give significant attention to other vertical markets, such as pharmaceutical, chemical, steel, rubber, food, and utilities," he said. "These other vertical markets offer Electro-Matic large opportunities for growth."

Analog ICs, Flash Memories, And TFT Displays Added At Bell

Bell Microproducts Inc. has signed agreements with Summit Microelectronics Inc. and IBM's Display and Embedded System business units, expanding the San Jose-based distributor's semiconductor offerings into analog peripheral devices and broadening its ATA flash-storage memory line. Summit's initial products include microcontroller peripherals, reset controllers, nonvolatile digital-to-analog converters, and three-channel 8-bit analog-to-digital converters integrated with EEPROM technology. Products from the IBM units, which are part of IBM Japan in Tokyo, include a new family of high-performance mass-storage ATA flash-based solutions in a 68-pin PCMCIA or a 50-pin small-form-factor package. Also included are several models of TFT LCD color monitors for a wide range of applications.

Components Firm Expands Presence In Pittsburgh Area

To strengthen its regional presence in the mid-Atlantic area, Shuster Electronics, Cincinnati, Ohio, has acquired CMD Electronics, Pittsburgh, Penn. Shuster distributes electronic components from its warehouse and sales operation in Cleveland, Ohio. The new Pittsburgh location will serve the needs of the western Pennsylvania market.

New Faces...

Cindy Eldridge was made general manager of Sterling Electronics Corp.'s San Jose sales location... Marc Gsand and Keith Duffy were named marketing directors at EBV Electronics, San Diego... Don Wagner was promoted to director of purchasing at Bisco Industries Inc., Orange, Calif... Bob Shreeve was made sales manager of Bisco's South Texas area... Darla Salazar was promoted to assistant sales manager at National Precision Products Co., Irving, Tex.

...And New Places

Airtechnics Inc, Wichita, Kan., has opened two new sales offices. One is at: 4250 Veterans Memorial Hwy., Suite 220, Holbrook, NY 11741; (516) 738-1830. The other is at: 5787 S. Hampton Rd., Suite 380, Lock Box No. 116, Dallas, TX 75232; (214) 330-5835.

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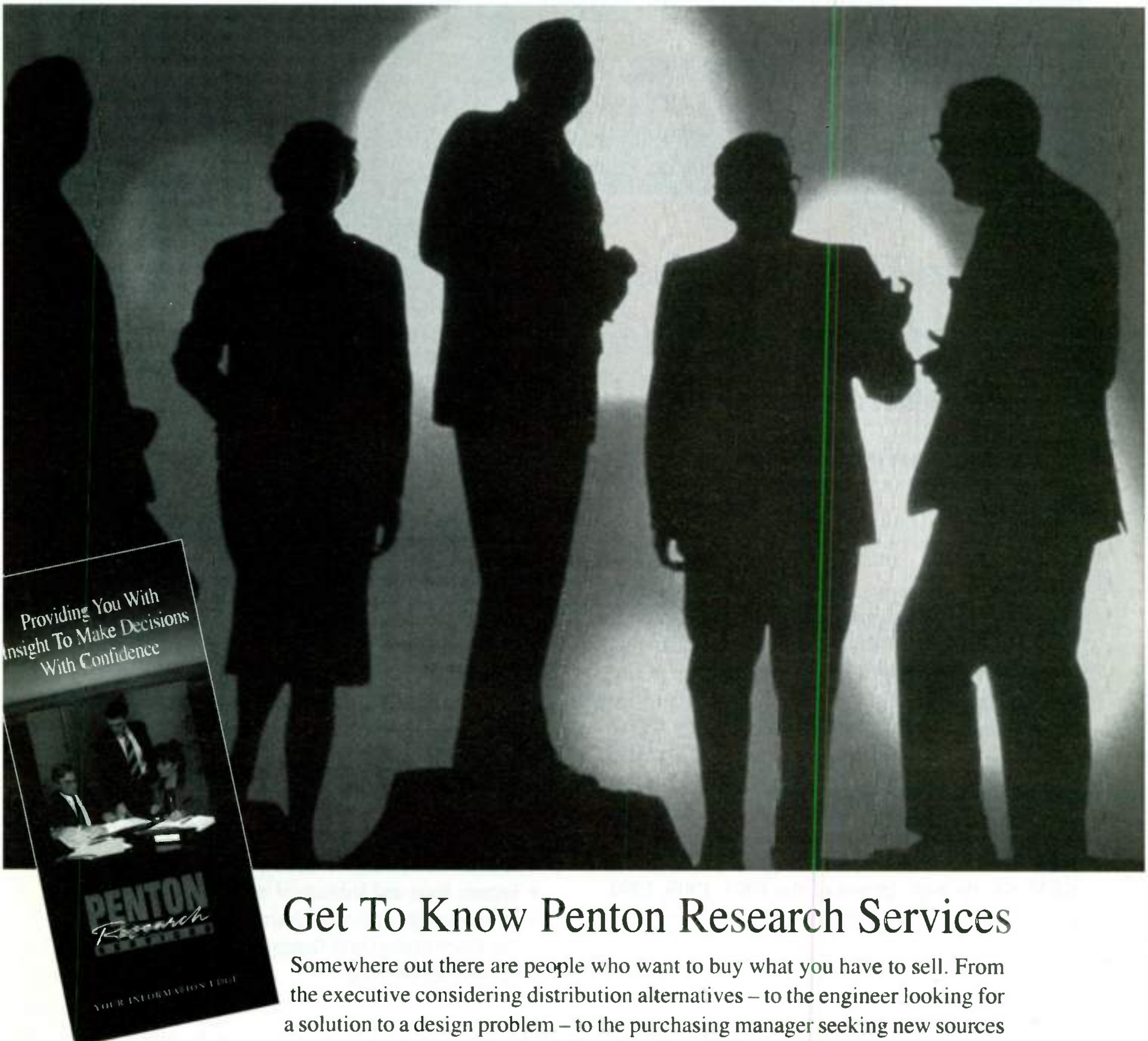

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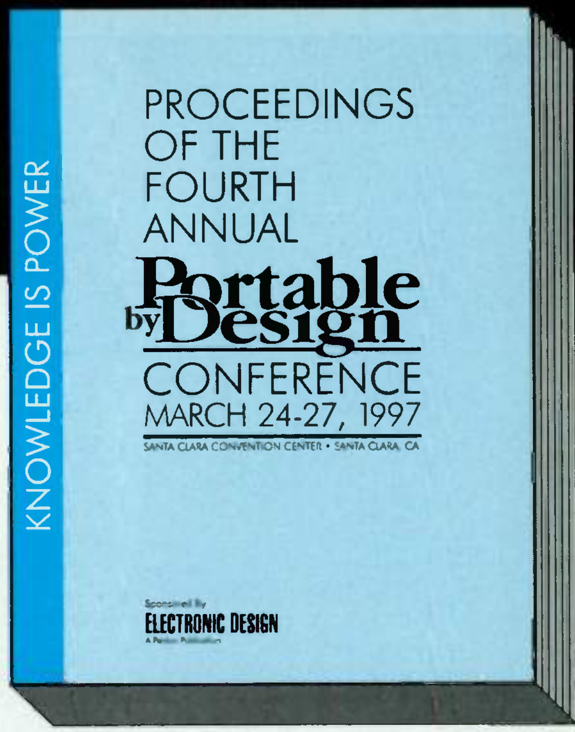

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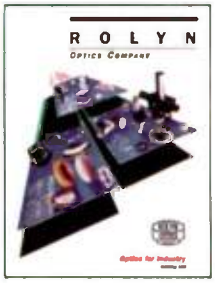

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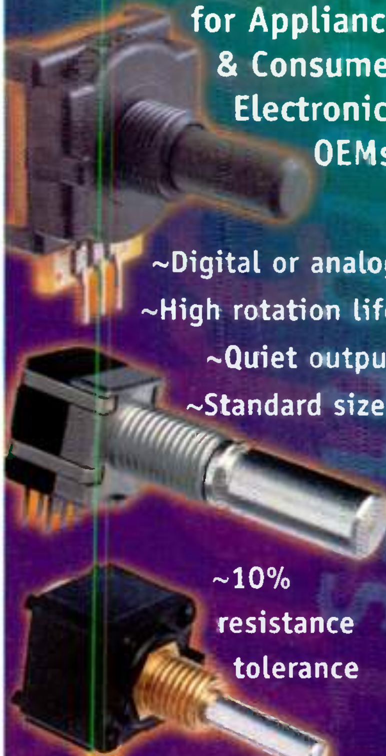

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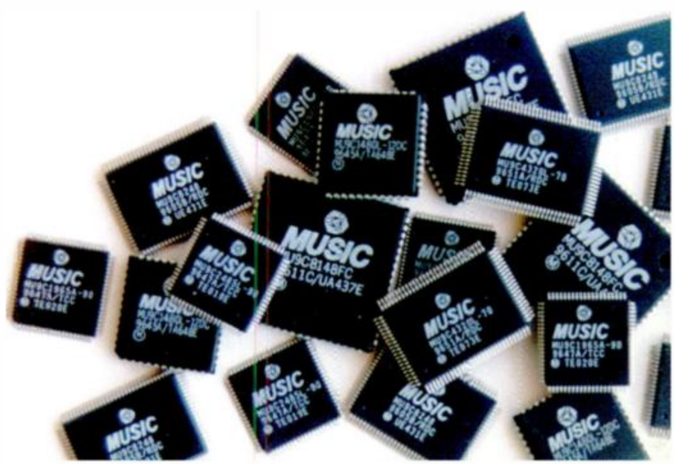

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