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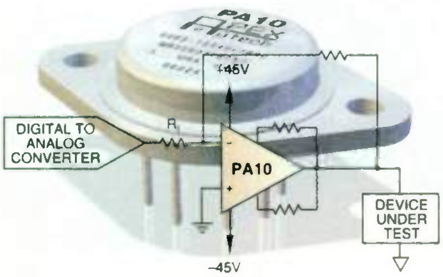

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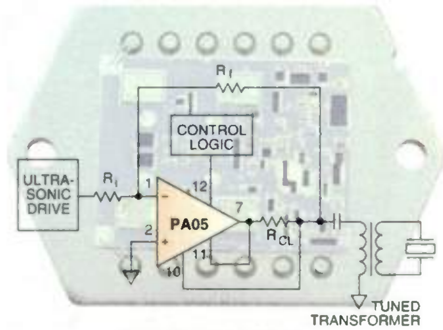

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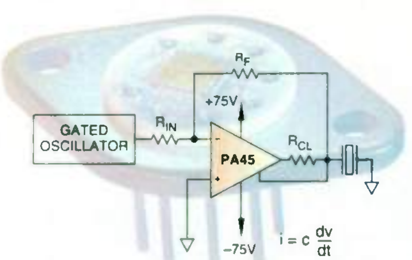

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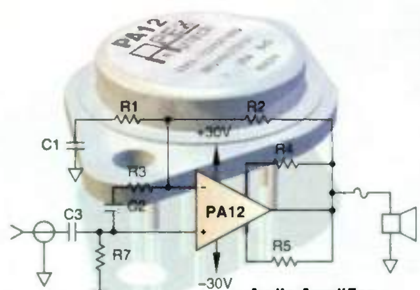

Audio Amplifier

KEY PRODUCT SPECIFICATIONS

Part #	$I_{O\ CONT}$	V_S	SR	P_D
PA03	30A	30V-150V	8V/µs	500W
PA04	20A	30V-200V	50V/µs	200W
PA05	30A	30V-100V	100V/µs	250W
PA10	5A	20V-90V	5V/µs	67W
PA12	10A	20V-90V	4V/µs	125W
PA45	5A	30V-150V	27V/µs	85W

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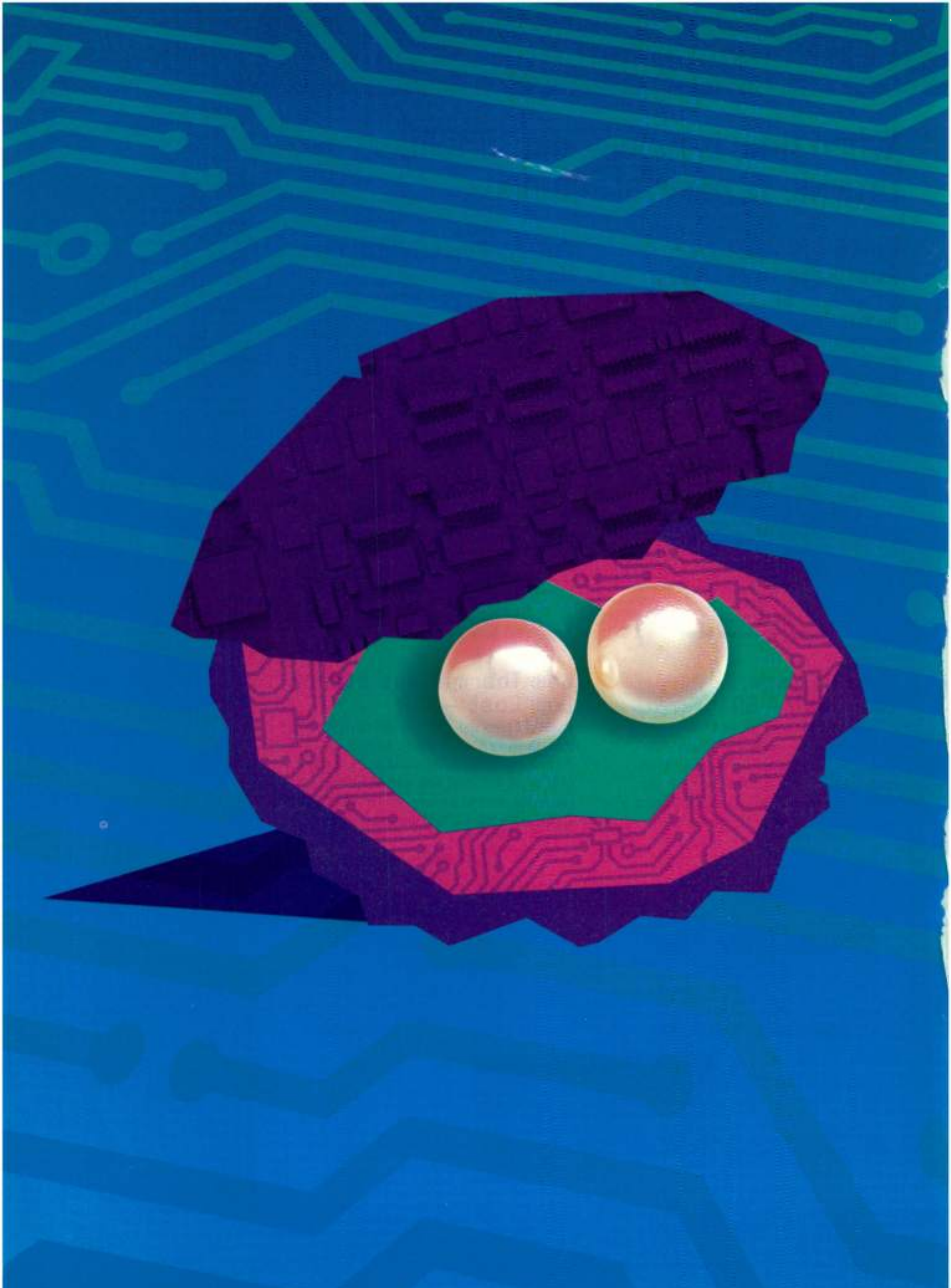

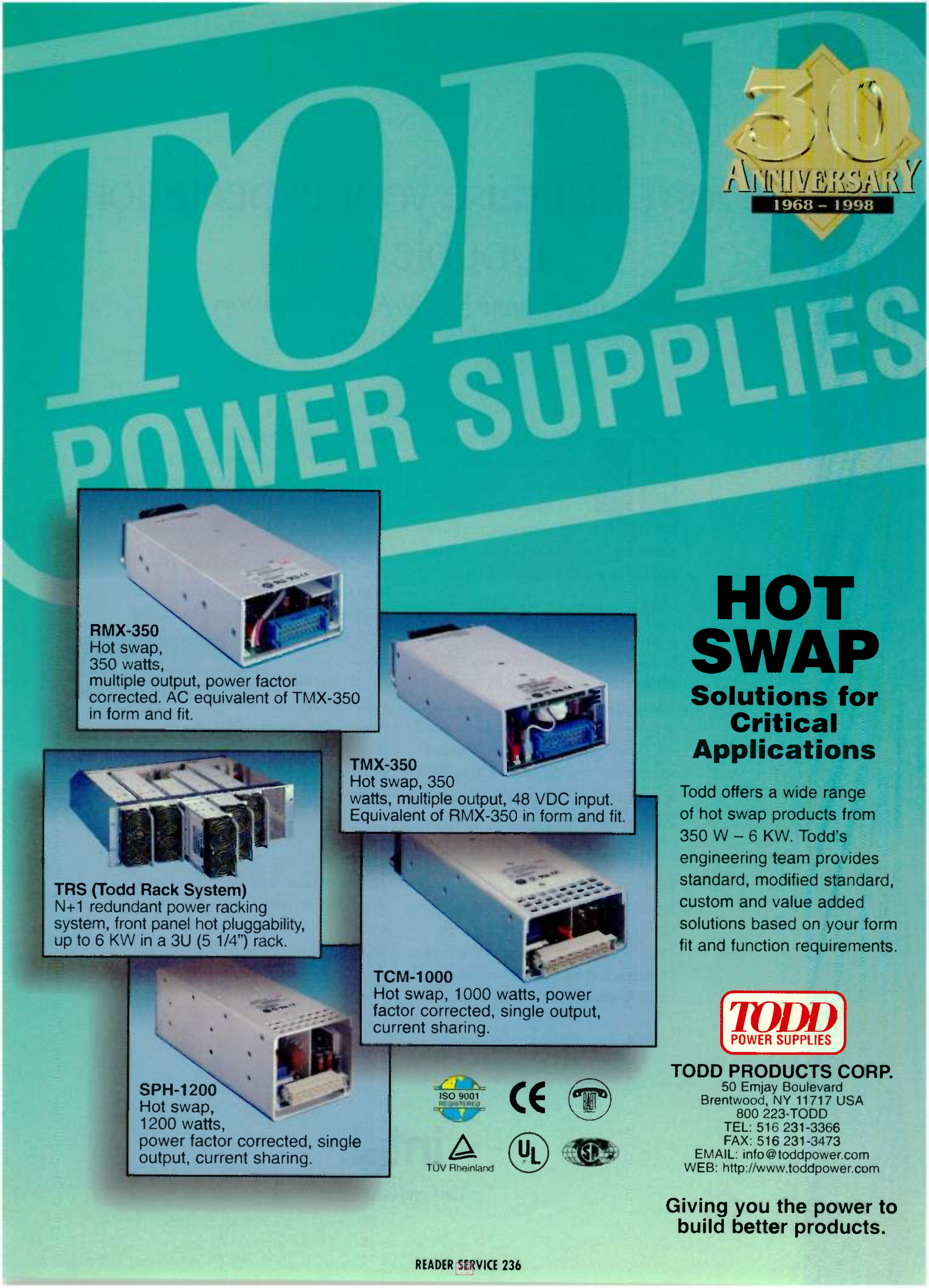
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TECHNOLOGY•APPLICATIONS•PRODUCTS•SOLUTIONS

February 9, 1998 Volume 46, Number 3

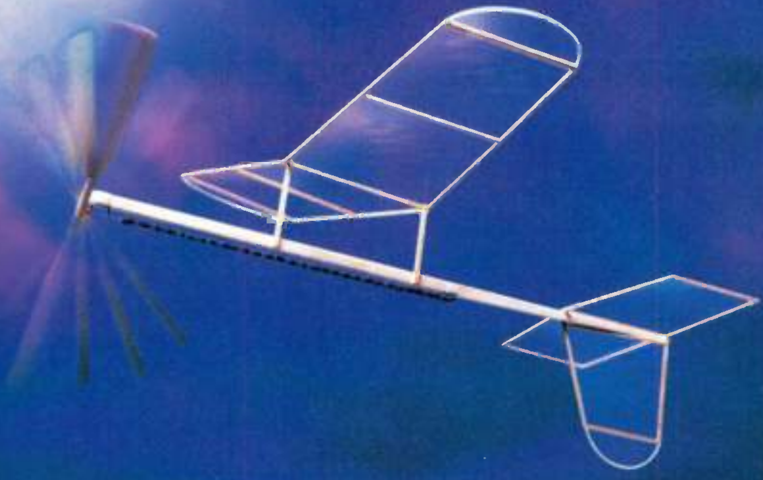
EDITORIAL OVERVIEW

TECH INSIGHTS

TECH INSIGHTS

DEPARTMENTS

ELECTRONIC DESIGN (ISSN 0013-4872) is published twice monthly except for three issues in May, three issues in August, three issues in October, and three issues in November by Penton Publishing Inc., 1100 Superior Ave., Cleveland, OH 44114-2543. Paid rates for a one year subscription are as follows: $100 U.S., $170 Canada, $180, $200 International. Periodicals postage paid at Cleveland, OH, and additional mailing offices. Editorial and advertising addresses: ELECTRONIC DESIGN, 611 Route #46 West, Hasbrouck Heights, NJ 07604. Telephone (201) 393-6060. Facsimile (201) 393-0204. Printed in U.S.A. Title registered in U.S. Patent Office.



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EC2	15.0 x 7.5 x 9.4mm	2c	140mW (Non-latch 3-12V)	60W (resistive) 125VA (resistive)
EE2	15.0 x 9.5 x 10.0mm			
EA2	14.2 x 9.2 x 5.4mm	2c	140mW (Non-latch 3-12V)	30W (resistive) 62.5VA (resistive)
EB2	14.3 x 9.3 x 7.5mm			

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February 9, 1998 Volume 46, Number 3

EDITORIAL OVERVIEW

ANALOG OUTLOOK

BOARDS & BUSES

PIPS

QUICKLOOK

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FDC633N	FDC634P	35	70	SuperSOT™-6
FDR4410	FDR836P	11	25	SuperSOT™-8
NDS8410A	NDS8435A	10	21	SO-8
NDT455N	NDT456P	13	26	Power SOT
NDM3000*		70	125	SO-16

*SO-16 Contains 3 N-Channel and 3 P-Channel die in one package

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Design, Automation, and Test in Europe Conference and Exhibition (DATE '98), Feb 23-26. Le Palais des Congres de Paris, Porte Maillot. Contact European Conferences, 11C Wemyss Pl., Edinburgh EH3 6DH, UK; +44 131-225-2892; fax +44 131-225-2925.

38th Israel Conference on Aerospace Sciences, Feb. 25-26. Tel-Aviv & Haifa. Contact Technion-Israel Institute of Technology, Haifa 32000, Israel; 972-4-8292713; fax, 972-4-8231848; e-mail: alice@aerodyne.technion.ac.il.

MARCH

Computer Telephony Conference and Exposition '98, Mar. 3-5. Los Angeles Convention Center, Los Angeles, CA. Contact Computer Telephony '98, 1265 Industrial Highway, Southampton, PA 18966; (215) 355-2886; fax (215) 355-4112.

International Verilog Conference and VHDL International User Forum (IVC/VIUF), Mar. 16-19. Santa Clara Convention Center, Santa Clara, CA. Contact MP Associates, 5305 Spine Rd., Suite A, Boulder, CO 80301; (303) 530-4562; fax (303) 530-4334; e-mail: lee@mpa-net.com; www.hdlcon.org.

IEEE Aerospace Conference, Mar. 21-28. Snowmass Conference Center, Snowmass, CO. Contact Mike Johnson, 2225 Roscomare Road, Los Angeles, CA 90077-2222; (310) 472-8019; e-mail: johnson@ee.ucla.edu.

Second Intellectual Property in Electronics Seminar (IP '98), Mar. 23-24. Westin Hotel, Santa Clara, CA. Contact John Whitaker, Miller Freeman Technical Ltd., +44 181-316-3297; e-mail: ed98@cityscape.co.uk.

PCB Design Conference West, Mar. 23-27. Santa Clara Convention Center, Santa Clara, CA. Contact Molly Knox, Miller Freeman, (408) 448-6173; e-mail: mknox@mfi.com.

Robot Safety Workshop, Mar. 24-26. The Westin Hermitage, Nashville, TN. Contact Brian Huse at RIA Headquarters, P.O. Box 3724, Ann Arbor, MI, 48106; (313)994-6088; fax (313) 994-3338; e-mail: bhuse@robotics.org; www.robotics.org.

Southcon/98, Mar. 24-26. Orange County Convention Center, Orlando, FL. Contact Electronic Conventions, (800) 877-2668 or (310) 215-3976; fax (310) 641-5117; www.southcon.com

INFOCOM '98, Mar. 28-Apr. 2. Hotel Nikko, San Francisco, CA. Contact Ramesh Nagarajan, Lucent Technologies, 101 Crawford Corner Rd., Rm. 3M-318, Holmdel, NJ 07933; (732) 949-2761; fax (732) 834-5906; e-mail: rameshn@lucent.com.

IEEE International Reliability Physics Symposium, Mar. 30-Apr. 2. Reno Hilton Hotel, Reno, NV. Contact Ann N. Campbell, M/S 1081, Sandia National Labs., P.O. Box 5800, Albuquerque, NM 87185-1081; (505) 844-7452; fax (505) 844-2991; e-mail: ancampbe@sandia.gov.

IEEE International Parallel Processing Symposium/IEEE 9th Symposium on Parallel and Distributed Processing (IPPS/SPDP), Mar. 30-Apr. 3. Delta Orlando Resort, Orlando, FL. Contact Viktor Prasanna, EEB-200C, Department of EE Systems, University of Southern California, Los Angeles, CA 90089-2562; (213) 740-4483; fax (213) 740-4418; e-mail: prasann@ganges.usc.edu.

Embedded Systems Conference Spring, Mar. 31-Apr. 2. Navy Pier Festival Hall, Chicago, IL. Contact Liz Austin, Miller Freeman Inc., (888) 239-5563; (415) 538-3848; e-mail: esc@mfi.com.

APRIL

20th IEEE International Conference on Software Engineering, Apr. 19-25. Kyoto International. Conference Hall, Kyoto, Japan. Contact Koji Torii, Graduate School of Information Sciences, Nara Institute of Science & Technology, 8916-5 Takayama-cho, Ikoma-shi, Nara-ken 630-01, Japan; +81 7437-2-5310; fax +81 7437-2-5319; e-mail: torii@is.aist-nara.ac.jp.

DSP World Spring Design Conference, Apr. 21-23. Santa Clara Convention Center, Santa Clara, CA. Contact Liz Austin, Miller Freeman Inc. (888) 239-5563, (415) 538-3848; e-mail: dspworld@mfi.com; www.dspworld.com.

APRIL

Southeastcon '98, Apr. 24-26. Hyatt Regency, Orlando International Airport, Orlando, FL. Contact Parveen Ward, ECE Dept., University of Central Florida, Orlando, FL 32816; (407) 823-2610; fax (407) 823-5835; e-mail: pfw@ece.engr.ucf.edu.

16th IEEE VLSI Test Symposium, Apr. 26-30. Hyatt Regency Monterey, Monterey, CA. Contact Rob Roy, Intel Corp., MS:JFT-102, 5300 Elam Young Pkwy., Hillsboro, OR 97124-6497; (503) 264-3738; fax (503) 264-9359; e-mail: robroy@ichips.intel.com.

IPC Printed Circuits Expo '98, Apr. 26-30. Long Beach Convention Center, Long Beach, CA. Contact Dan Green, The Institute for Interconnection & Packaging Electronic Circuits, 2215 Sanders Rd., Northbrook, IL 60062-6135; (847) 509-9700 ext. 371; fax (847) 509-9798.

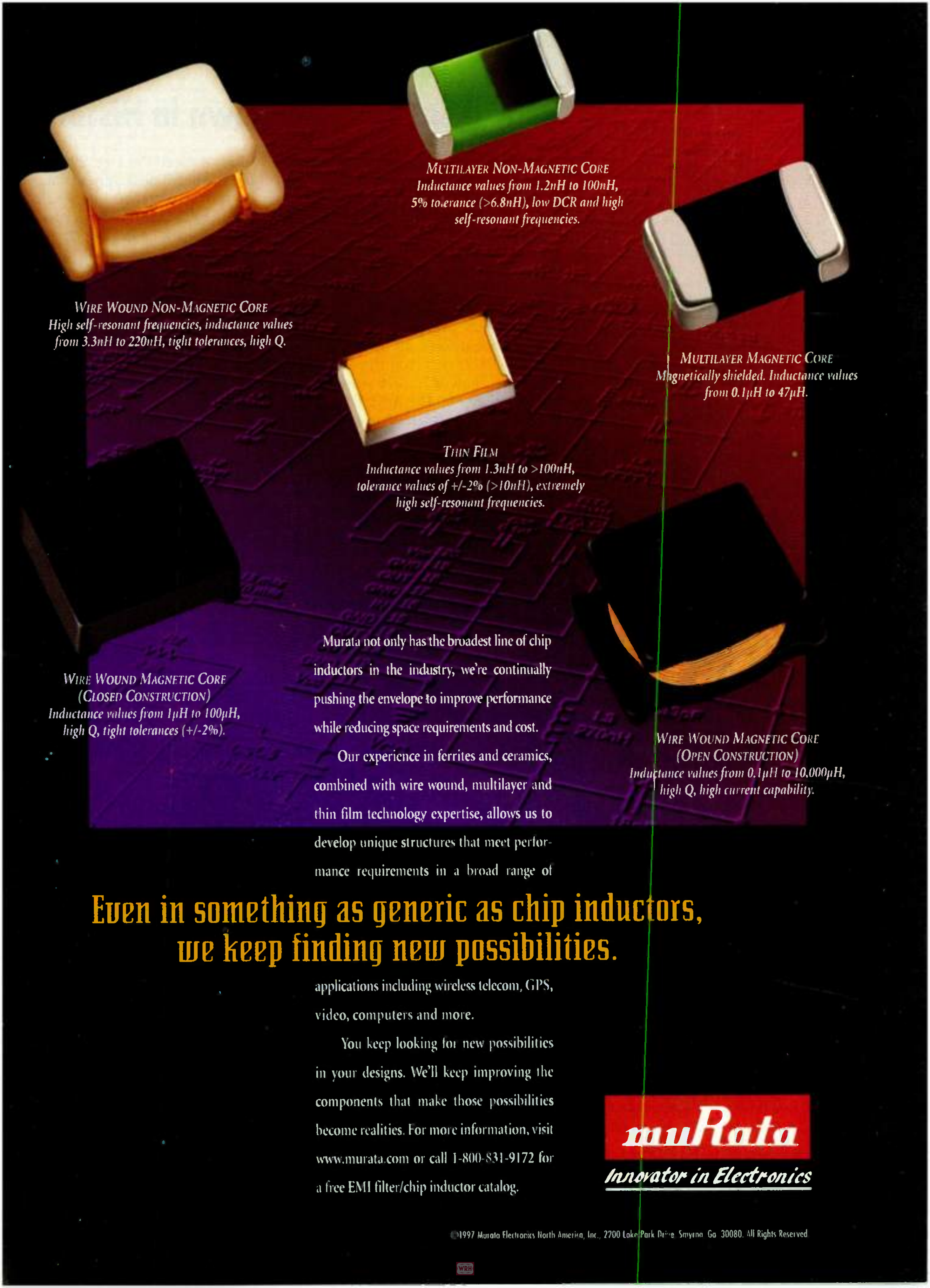
MAY

100th ACerS Annual Meeting & Exposition, May 3-6. Dr. Albert B. Sabin Convention Center, Cincinnati, OH. Contact The American Ceramic Society Customer Service Dept.; (614) 794-5890; fax (614) 899-6109; e-mail: customer-srvc@acers.org; www.acers.org.

Conference on Lasers & Electo-Optics & The International Electronics Conference (CLEO/IEC), May 3-8. The Moscone Center, San Francisco, CA. Contact Amy Hutto, OSA Conference Services, 2010 Massachusetts Ave. N.W., Washington, DC 20036-1023; (202) 416-1980; fax (202) 416-6100; e-mail: cleo.info@osa.org.

IEEE International Conference on Evolutionary Computation, May 3-9. Ankorage, AK. Contact Patrick K. Simpson, Scientific Fishery Systems Inc., P.O. Box 242065, Anchorage, AK 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@alaska.net.

IEEE International Conference on Neural Networks (ICNN '98), May 3-9. Anchorage, Alaska. Contact Patrick K. Simpson, Scientific Fishery Systems Inc., Post Office Box 242065, Anchorage, Alaska 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@alaska.net.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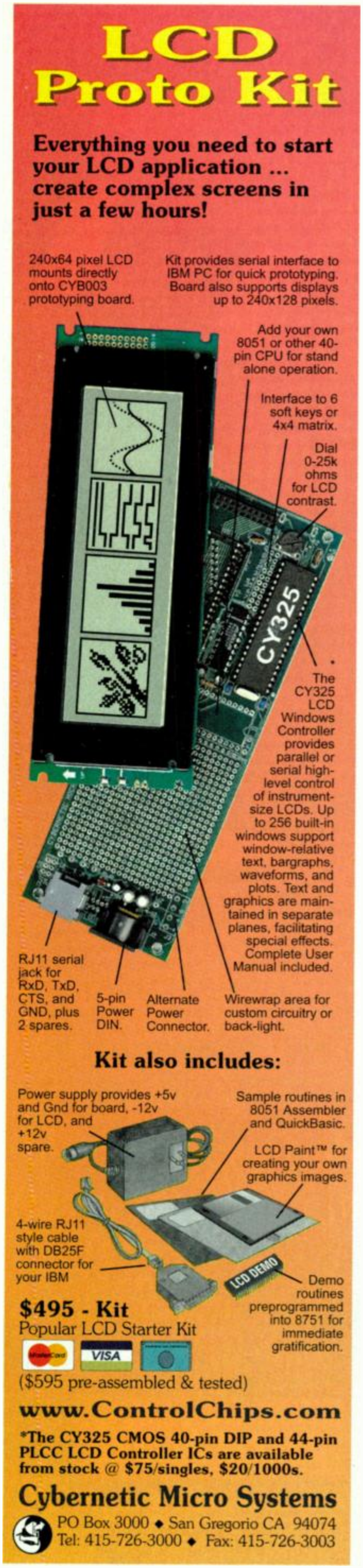


What It Takes To Go Down In History

I have to admit that I was surprised when I first noticed the Dec. 29, 1997 *Time* magazine cover shot of Andy Grove, and the headline that read "Man Of The Year." Maybe my surprise was due to the fact that the Intel chairman and CEO's digitally created chip-faced head was in the same supermarket magazine rack as pop magazines and trashy tabloids featuring Oprah, Lady Di, aliens, and Elvis (he died in December, 20 years ago?...maybe.)

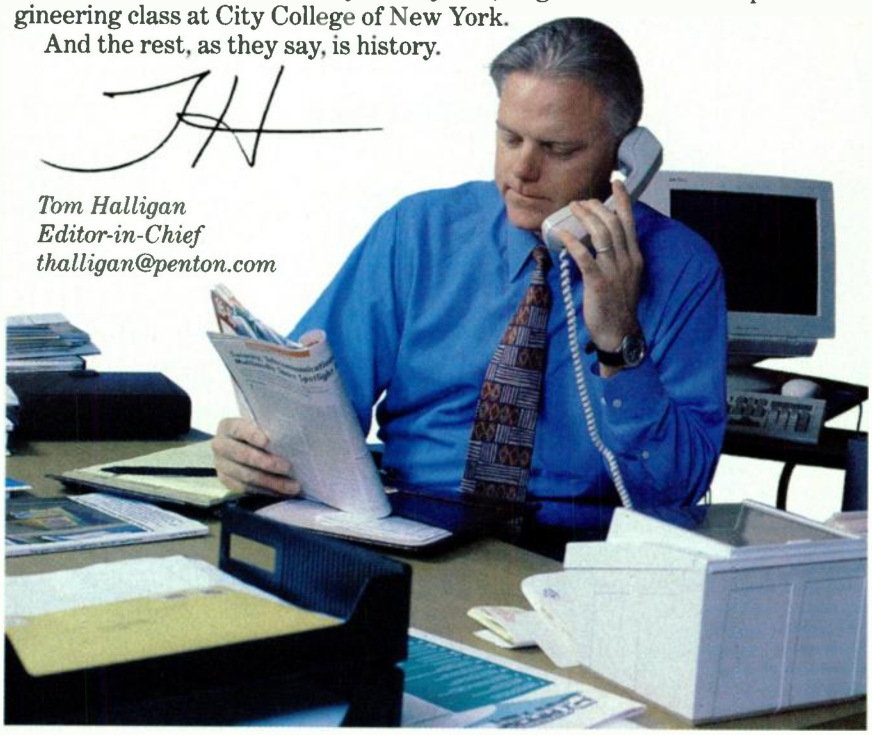
But I quickly realized that I had been surprised at the choice that *Time* had made. Grove is not the typical choice for the Man Of The Year distinction. In the magazine's 70-year history, the *Time* editors almost always gave the nod to do-good U.S. presidents and politicians, foreign heads of state, religious leaders, peacemakers, and social activists. However, Hitler (1938), and Stalin (1939 and 1942) received the award for their European escapades. Then, there was Khomeini in 1979—a surprise because he certainly was not considered a good guy by the American people at the time. And in 1982, the *Time* editors opted to skip a human entirely, and named The Computer as "The Machine Of The Year."

In an editorial discussing why *Time* selected Grove, the editors pointed out that "In a year filled with world-shaking events, the overriding story was the economy, but the driving force behind the economy has clearly been technology. And no one has done more to further technology's long march than...Andrew Grove." The editorial continued, "We consider the computer revolution one of the defining stories of our time...and that Andy Grove embodies both the energy of the business and technology industries that are shaping society today, and the vision and creativity that have always typified the American Dream."

I am pleased that *Time* selected Grove. It's an important statement that articulates a message that needs to be reinforced: Scientists and the creators of technology should be recognized for their contributions and positive influence on society.

The article detailing Grove's life before Intel also is a testament to the human spirit. Fleeing the Nazis, and later the Russians, from his native Hungary to avoid imprisonment or possibly death, Grove eventually made his way to the U.S. It didn't take long for the Hungarian refugee to grasp what the U.S. could offer, and in only three years, he graduated at the top of the engineering class at City College of New York.

And the rest, as they say, is history.



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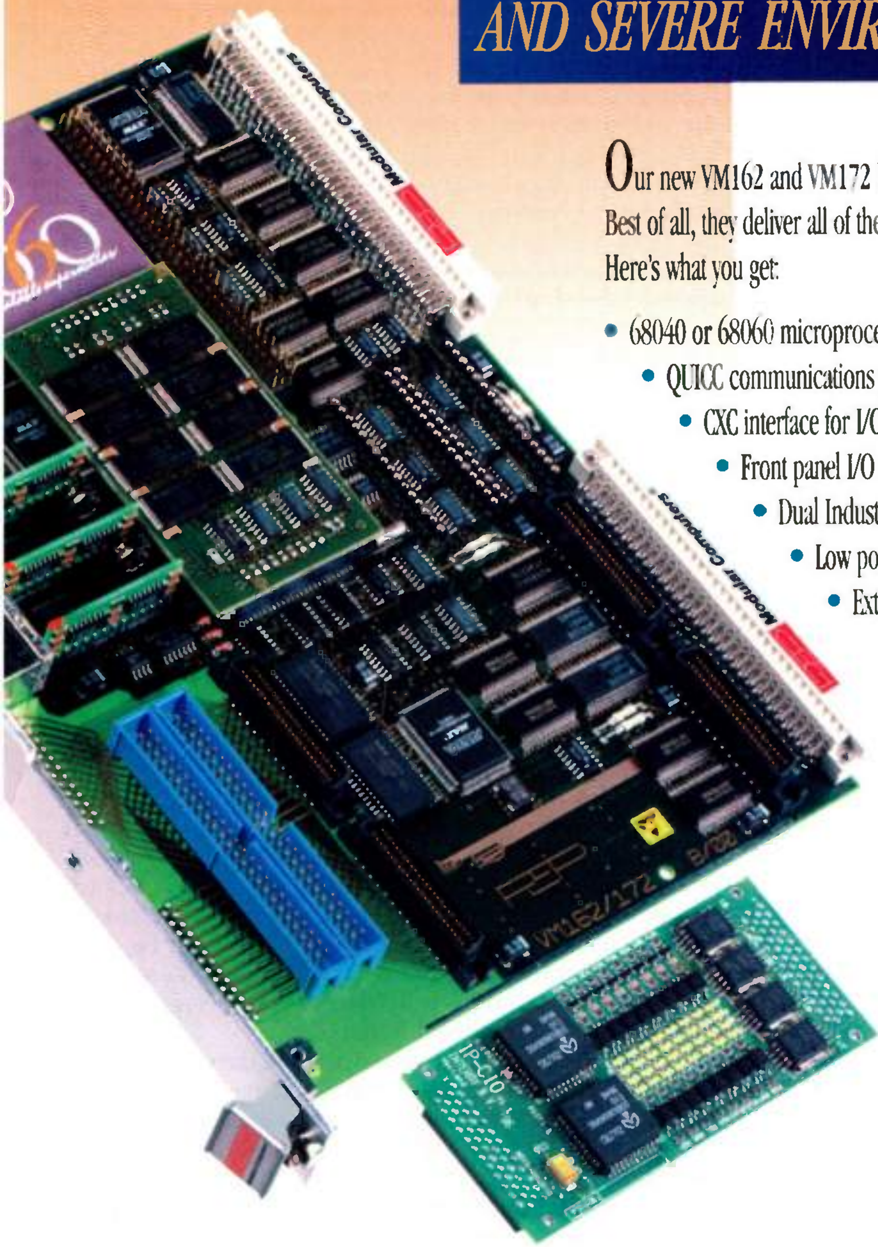

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READER SERVICE 207

Speed To Burn: The Push For Throughput

The delivery of powerful, hand-held computing and entertainment platforms that weren't even thought possible just a decade ago is now practical, thanks to embedded 16- and 32-bit RISC technology. Today, a CPU throughput of 10 to 20 MIPS represents moderate to lackluster performance, while throughputs of 30 to 100 MIPS are just barely deemed adequate to run some of the current applications in palm-top computers, portable instruments, and set-top boxes. And, for the next generation of consumer, computing, and industrial products, the computational needs will skyrocket to several hundred of thousands of MIPS (giga instructions/s, or GIPS).

Several companies are already well on their way toward developing such a next-generation processor. However, there are conflicting demands that force designers to make very careful design trade-offs. For instance, high speed and low power consumption are diametrically opposed requirements because CMOS power consumption increases as frequency increases. To counter that dilemma, designers are reducing the operating power-supply voltage.

But, if the process used to fabricate the silicon has not been optimized for the lower supply voltage, then designers must sacrifice some of the speed. If the process has been optimized, the circuit might actually be able to deliver higher performance, but then other issues crop up. For instance, when designers adjust transistor threshold levels to allow lower-voltage operation, the lower threshold levels may allow signal noise to corrupt circuit operation. The lower threshold levels also could increase standby current because subthreshold leakage currents can flow easier. And, of course, a lower operating voltage also limits the I/O pin voltage levels. Today's 2.5-V chips typically tie into 3.3-V interfaces with minimal problems, but as supply levels go even lower, a reduced interface level must be defined to allow the chips to communicate with each other.

DAVE BURSKY
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Solutions that will address most of these issues are starting to appear. They include circuits with dual-threshold-level operation to deal with the low-V_T issue, the reduction of the power-supply voltage to 2.5 V and lower, the use of copper interconnections to reduce on-chip RC delays, and the use of deep-submicron design rules (below 0.25 µm) to reduce parasitic losses and improve packing density. The results of these efforts—processors with throughputs of 200 to 400 MIPS that consume a few hundred milliwatts to about 2 W when going at full tilt—have started to appear.

With many of the embedded processors, the name of the game isn't just throughput, but the level of system integration possible. As finer-line processes come out, transistors are smaller and more interconnect levels are possible, leading to much higher levels of integration. It's no longer adequate to just include a first-level cache and a bus interface. Today's chips are approaching system-on-a-chip levels by incorporating many features that would otherwise require stand-alone chips to implement. Tomorrow's chips will have even more complex functions, like multiple CPU cores cohabitating on the same chip.

The need for higher throughput is almost a direct result of the more complex tasks we want equipment to perform. No longer is a simple calculation enough, especially if the processor must perform signal processing for speech recognition and telephony or other applications that haven't seen the light of day outside of a very large, compute-intensive system. And the need for still higher throughputs will not slow down. More companies want portable computers to do imaging and remote wireless communications, and provide smarter cellular telephones that handle e-mail and faxes, paging, and message storage. With leftover MIPS, designers can add in functions such as a calculator, alarm clock, and even computer games. Speech recognition comes next to allow hands-free dialing and control. Who knows what follows after that? Send me your ideas for extra features and when we get enough, we'll publish a summary. *dbursky@class.org.*

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READER SERVICE 113

Mixed-Signal Megacell Will Target Sensor Applications

In an effort to reduce overall product development time and ease time-to-market pressures facing mixed-signal and systems designers, American Microsystems Inc. (AMI), Pocatello, Idaho, has joined forces with General Electric's Research and Development division to develop a mixed-signal ASIC megacell. The analog-to-digital converter (ADC) will be optimized for end users with sensor-interface requirements or applications that require data acquisition and sensor data processing. These interfaces typically are found between analog sensors and digital signal processors (DSPs).

The ADC cell will be scalable from 8 to 16 bits, and is targeted for AMI's 0.6-µm linear process. It will include a third order sigma-delta modulator, which will be a full-custom mixed-signal cell, and a decimation filter consisting of standard cells and/or semi-custom digital circuits to be determined in the first phase of the filter design. The ADC will operate at 5 V and be able to offer extreme accuracy at very high data rates.

During development, the task of designing and simulating the ADC will fall to GE. They also will be responsible for offering support to AMI in the modulator's layout. AMI will perform layout and post-layout simulation of the modulator and decimation filter. Once completed, the ADC will be used by both companies in future developments and will be part of the AMI mixed-signal library. For further information, contact AMI at (208) 233 4690, or check out its web page at *www.amis.com.* CA

Companies Team to Extend UML For Real-Time Needs

Rational Software, Santa Clara, Calif., has teamed with Kanata, Ont.-based ObjecTime Ltd. to define a set of extensions to the universal modeling language (UML) that will serve the needs of real-time designers. UML is a combination of three major software-modeling methodologies and notations created by Rational's Grady Booch, Ivar Jacobson, and Jim Rumbaugh. The Object Management Group of Framingham, Mass., has chosen UML as the standard for object-oriented modeling for a broad range of applications.

UML was designed to be extensible. As a result, Rational has made an $8.9 million investment in ObjecTime, which has developed a methodology called real-time object-oriented modeling (ROOM). The idea is to take many of the concepts of ROOM and redefine them as extensions that are compatible with UML. In addition, some changes will need to be made to the way developers work with ROOM. ROOM lets you build an executable model that could generate source code. But you couldn't go into the source code, edit it, and automatically update the model. Rational's UML-based Rose tool supports "round-tripping," which does permit updating the source code by changing the model and updating the model by changing the source code.

Among the extensions that UML for Real-Time will bring to standard UML is a set of concepts for modeling complex layered architectures. It also will provide an extended set of mechanisms for dealing with time and real-time deadlines, including timed and prioritized messages. Finally, it will incorporate infrastructure concepts for modeling the underlying computing mechanisms that support real-time distributed applications. These include ways of dealing with failed tasks, resetting processors, and installing new hardware and software.

Rational Software can be reached at (408) 496-3600; *http://www.rational.com*, or call ObjectTime at (613) 591-3535; *http://www.objectime.com.* TW

Scottish Collaborative Looks To Advance Optical Computing

The Scottish Collaborative Initiative in Optoelectronic Sciences (SCIOS), a group of four Scottish universities headed by Heriot-Watt University, Edinburgh, Scotland, was formed to do research and development in optoelectronics. Says Andrew Walker, professor of modem optics at Heriot-Watt, "Our aim is threefold. We want to show how optical techniques can be used to carry large amounts of information between silicon chips in a very efficient manner, and to investigate new types of computers and processing systems which could take advantage of that capability. A third aim of the program is to develop the associated technologies, including semiconductor devices, optical components, and lasers."

The group already has evolved a hybrid approach, a device comprising a silicon chip and a special optoelectronic semiconductor chip—one on top of the other. This latter semiconductor is based on gallium arsenide, which is suitable for providing an interface between electrical and optical signals in both directions.

Using the "solder-bump flip-chip" technique, these novel "smart-pixel" devices are created literally by bringing together two elements of old and new. The gallium-arsenide chip is connected to the silicon chip by thousands of tiny solder connections that allow large amounts of data to be transferred off of the silicon. The device transmits optical signals by controlling the reflectivity of light. Laser beams shine onto the chip, and a signal is imprinted and passed on by the reflected beam. Once in the optical domain, these signals can be sent anywhere in the system with degradation.

Optical techniques avoid connection "bottlenecks" of information in massively parallel computing systems. Applications will include everything from military apps and engineering simulations to the control of telecommunications networks and even forecasting weather. RE

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System-On-A-Chip Design Gets Serious With New Center

There's little doubt in the EDA industry today that designs are migrating from single function chips to systems on a chip. However, the burning question remains: How we will get there? Cadence Design Systems Inc., San Jose, Calif., plans to not only answer this question, but speed the migration process thanks to a recent partnership agreement with Scottish Enterprises, Scotland's main economic development organization. The purpose of the collaborative effort will be to establish Scotland as the primary location for electronics companies to design advanced system chips.

To accomplish this goal, Cadence has broken ground on what will be its largest design center, to be located in Livingston, Scotland. By the year 2004, Cadence promises have the facility up and running, staffed by a team of approximately 1800 engineering professionals. The center will be used to perform actual chip design work for Cadence's worldwide customer base utilizing secure, high-bandwidth telecommunications links to more than a dozen other design centers in the company's Design Factory Network. It also will be used as an advanced research and development laboratory to develop next generation technologies and methodologies for system on a chip design.

As part of a larger initiative sponsored by Scottish Enterprises, government, industry, and academic a to address the growing needs of system on a chip design and designers, Cadence's design center will serve as the focal point for a new system on a chip campus. Also to be located at this campus, roughly a 55-acre site, will be a host of other industrial and academic activities. In particular, the campus will be home to the first ever educational facility to offer a curriculum for advanced chip design and a masters degree in systems on a chip design. To assist in this project Cadence has agreed to provide software and research support. The campus will focus on such system on a chip challenges as development, protection, and exchange of intellectual property building blocks in an efficient and secure manner. More specifically, issues having to do with the legal, tax, customs, educational, and technical implications of system design will be addressed.

For additional details on this effort check out Cadence's web site at *www.cadence.com*, or Scottish Enterprises at *www.scotent.co.uk*. CA

Library Modeling Standard Helps Ease Use And Reuse Of IP

Open Verilog International (OVI), Los Gatos, Calif., has recently approved a library standard for the Verilog HDL (Hardware Description Language). Known as the Advanced Library Format (ALF) standard, its main goal is to help facilitate the use and reuse of intellectual property. It accomplishes this by creating a single format that will allow HDL-based design libraries (VHDL and Verilog HDL) to be portable.

In particular, it specifies a library exchange format for multiple design and analysis tools, including synthesis, static timing, and power analysis, as well as power, logic and timing optimization. Developed by OVI's Technical Subcommittee, the standard enables all libraries developed using ALF to be translated for use with any design tool and for use in new applications. The ALF standard supports deep submicron designs using large ASIC cells, memory, and blocks.

The ALF standard's primary benefit is its ability to make intellectual property easier to use. The ALF standard accomplishes this by establishing common criteria for optimizing and translating models. The ALF standard also expands current library modeling to higher-level blocks, making them more accurate and extensible. In addition, it reduces the number of ASIC libraries for multiple vendors to one library and makes it possible for ASIC suppliers to generate and verify only one library format for their customers.

The ALF standard, version 1.0, is now available and can be downloaded from OVI's web site at *www.ovi.org*. Copies also can be obtained directly from the OVI office by calling (408) 358-9510. Each copy costs $50. CA

Crystal-Slicing Method Gives Boost To Blue-Laser Development

Scientists at Rensselaer Polytechnic Institute have come up with a way to grow aluminum-nitride crystals that are large enough to slice into semiconductor substrates. These crystals can be used to fabricate blue and ultraviolet lasers and blue and green LEDs.

Glen Slack, one of the research professors on the project, demonstrated that you can grow aluminum-nitride crystals in a tungsten crucible at 2300°C. They recently were able to solve a problem of the crucible not surviving for very long due to aluminum attacking the grain boundaries in the tungsten.

Semiconductor light sources have always been attractive because of their ruggedness and economy, says Leo Schowalter, professor and chair of physics at Rensselaer. However, LED color has been pretty much limited to red. Blue and green LEDs are needed if we're to create traffic signals, automobile lighting, flat-screen TV sets, and other applications where long life and high efficiency are important. Also blue and ultraviolet semiconducting lasers would make it possible to squeeze as much as 30 times more material onto a compact disk than can be done with the infrared lasers that are currently used.

For more information, call Leo Schowalter at (518) 276-6435; e-mail: *schowalt@unix.cie.rpi.edu*; or on the Internet at: *www.rpi.edu/~schowl/schowalt.htm*. RE

Edited by Roger Engelke

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READER SERVICE 180

HP Asks Voters To Reject Proposal To Add A High-Speed Extension To The IEEE-488 Interface Bus Standard

In a highly unusual move, Hewlett-Packard Co. has publicly called for the rejection of a revision of the IEEE-488 standard that would hike the speed of the very popular general-purpose interface bus (GPIB) by up to eight times. HP says the added capability, known as high-speed 488 or HS-488, has not been sufficiently tested and could cause disruptive errors during data transfers. But supporters of high-speed 488 say that just isn't true and the addition to the standard will cause no problems with the huge installed base of IEEE-488 equipment.

The IEEE's high-speed 488 working group has been hammering out the proposal for three years, with representation from HP, the company that invented the original GPIB (the HP-IB). Balloting was planned for sometime during the first quarter of this year and, in fact, may have already begun by press time. The group's chair, Robert Canik, replied to HP's initiative with a letter to the editors of technical publications. Canik, the GPIB R&D manager at National Instruments Corp., Austin, Tex., said the group's primary goals were compatibility with existing IEEE-488 equipment and software, and to boost performance by an order of magnitude.

"After three years of hard work and detailed simulation and testing, this working group has successfully met those goals and, as a majority, has voted to submit this robust specification for formal IEEE approval," said Canik. He notes that it is inappropriate to comment publicly on a standard in the balloting process, but "I feel compelled to stand up for the efforts of the working group, and not allow a single company to attempt to influence the outcome of the IEEE vote."

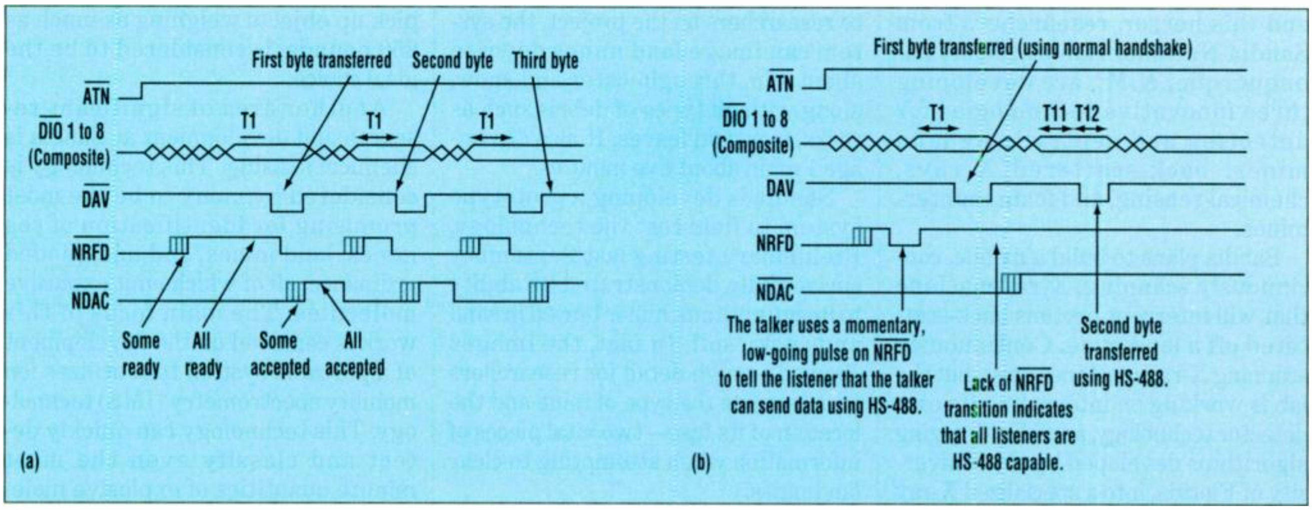
HP had said that the proposed revisions "threaten the integrity of the IEEE-488 standard—a worldwide, reliable communications standard for data transfer." According to the announcement, joining HP in opposition to high-speed 488 were Keithley Instruments GmbH, Germany; ines Inc., Englewood, Colo., which supplies GPIB interface cards; and ACEA, a test and measurement company from the Netherlands.

"Of paramount concern to HP and others is that HS-488 circumvents the IEEE-488 three-wire-handshake protocol and could compromise the standard's robustness, resulting in spurious noise, loss of data and loss of data error detection," said HP's announcement. "HS-488 offers a two-wire handshake protocol, which has not been proven effective in ensuring data integrity and has not been shown to be adequately tested in the field, especially in noisy environments," said the company. It also said that the three-wire handshake offers reliable synchronization of data transmissions, even in the harshest and noisiest environment.

"Members of standards committees know that when the industry considers changing a standard, a huge amount of interoperability testing needs to be performed," added Ned Barnholt, senior vice president and general manager of HP's Test and Measurement Organization. "The proposed revisions have not been adequately tested on-site, especially for noise immunity and interoperability. And very little documentation of such testing has appeared in the technical media."

Dave Richey, engineering manager for HP's Measurement Systems Div., said that the company had concluded that existing equipment will not work properly with the revised standard. "HP participated in the working group assuming problems would be shaken out before a vote was taken," said Richey, "That didn't happen." He added that there has been no public debate on the proposal, in accordance with IEEE procedures. The industry in general should be given adequate notice of the proposal and be allowed to comment on it before it goes to a vote, he said.

HP said that a better solution would



The IEEE-488 three-wire handshake requires a handshake for each byte transferred over the bus (a). The proposed HS-488 revision to the standard adds a source-synchronized transfer mode that uses only one handshake to establish the proper transfer speed (b). Once the compatibility of the talker and listener transfer speeds is established, no further handshaking is employed.

be an emerging PC-based standard, like universal serial bus (USB) or Firewire, "which have already undergone significantly greater interoperability testing than the changes proposed in HS-488." Richey noted that USB is an accepted standard that offers flexibility and low system costs. And, he added, "Firewire also shows great promise and offers far greater bandwidth than the proposed revisions. Why should our industry commit huge resources to a questionable extension of IEEE-488, when the computer industry is already developing excellent solutions for increased speed?"

Ron Wolfe, corporate marketing strategist at National Instruments, disputed HP's contention's about the handshake. The sole purpose of the handshake is to regulate data speed so the speaker doesn't send data faster than the listener can accept it. "All HS-488 does is add a source-synchronized transfer mode," said Wolfe. "It's the same exact technology that VME uses for VME block transfers. MXI bus uses it, and has been using it for years. SCSI uses it. SCSI 2 uses it. If you and I both know that you can take data as fast as I can send it, then we don't use the handshake for each byte," he says *(see the figure)*.

Compatibility is not a problem, Wolfe said. The protocol is handled at the hardware level, and no changes to software are required. If a system has both older IEEE-488 instruments and HS-488 versions, the high-speed units can talk to each other at the faster rate. The basic standard allows a speaker to communicate with multiple listeners at the same time. "If any one of those listeners is not high-speed capable, the talker defaults to the original three-wire handshake," he said. "It works just like it does now."

As for USB and Firewire, Amar Patel, instrument control product manager at National Instruments, said the former delivers no significant speed improvement and the latter is not ready for commercial use. He said USB's maximum transfer rate is the same as the theoretical maximum for GPIB, 12 Mbits/s (1.5 Mbytes/s). Regarding Firewire, he said, "It's at least one year away from commercially available products because there's still a lot of hammering out going on with the specification." Wolfe said that estimate was specifically for computer products. Instrumentation products would see even more of a wait.

Wolfe insisted that the revision to the standard should not cause any problems. "One thing that's important, nothing's changing about the way it works already. The changes are additions, a new mode. So it's not going to break anything," he said. "And it's totally optional. You can turn it on and turn it off. It's totally transparent. It's totally interoperable."

John Novellino

Chemical Detection And X Ray Techniques Will Improve The Detection And Elimination Of Land Mines

Land mines have risen to the forefront, as a global problem with dire consequences. Estimates count over 100 million land mines deployed in 68 countries. And, recent figures indicate that although 100,000 mines are cleared each year, another two million are laid in their place, killing or maiming roughly 2,000 people each month. Hoping to end this horror, researchers from Sandia National Laboratories, Albuquerque, N.M., are developing three innovative technologies for detecting and neutralizing land mines: back-scattered X rays, chemical sensing, and foam countermines.

Sandia plans to build a mobile, continuously scanning, X-ray machine that will intercept protons back-scattered off a land mine. Continuously scanning X-ray machines exist, but the lab is working on integrating its own detector technology, as well as imaging algorithms developed by the University of Florida, into a specialized X-ray machine optimized for the detction of land-mines.

In operation, the detector system records a higher response when the beam hits a plastic land mine, than when it simply strikes the soil. Of course, other materials in the soil will cause the detector to exhibit a higher response as well. To avoid a false positive reading, a microprocessor subsystem in the detector produces a real-time visual image for immediate observation and analysis. According to researchers on the project, the system can image land mines down to about 4 in. through water and snow, along with all types of debris such as rocks, logs, and leaves. It also can image 1 m^2 in about five minutes.

Sandia is developing a prototype system to field test the technology. Preliminary testing last September successfully demonstrated its ability to image antitank mines buried in sand and rocky soil. In fact, the images showed enough detail for researchers to determine the type of mine and the location of its fuse—two vital pieces of information when attempting to clear landmines.

Researchers caution, however, that a field-ready prototype is still roughly a year away, and it could be another year after that before a back-scattered X-ray mine detector is in actual use. While the initial prototype is expected to be integrated into a redesigned Humvee, a more suitable platform for the detector is being researched. A Remote TeleRobotic Vehicle for Intelligent Remediation (RETRVIR), an all-terrain vehicle with a robotic arm that can dig and pick up objects weighing as much as 250 pounds, is considered to be the ideal choice.

Another area of significant research and development at Sandia is chemical sensing. This technology is considered by many to be the most promising for identification of sea mines, land mines, and unexploded ordinance, all of which emit explosive molecules. The main focus of this work is centered on the development of a portable system that utilizes ion mobility spectrometry (IMS) technology. This technology can quickly detect and classify even the most minute quantities of explosive molecules. The system will also include Sandia's concentration technology, which has the potential to chemically

TECH BREAKTHROUGH

amplify a sample's strength by thousands of times.

Some of the work being done to support the chemical-sensing system involves modeling the environmental fate and transport (EF&T) of explosive signature molecules. The goal is to analyze how environmental conditions, such as temperature and precipitation, influence the movement of explosive molecules through the soil, air, and water. Researchers will look into how rainfall and soil temperature affect detection.

The chemical detector is expected to weigh no more than 20 pounds, and to be ready for field testing on sea mines by next spring. While the system's final design is still under development, it will most likely consist of a sensing tube extending from a box that can be inserted into the water. To make the system easy to operate, it may work by simply flashing a green light to indicate that the unit is sampling, but has found no explosives; a yellow light to indicate a small concentration of explosives has been found and that further sampling is required; or a red light to indicate a significant concentration of explosive has been detected.

Assuming the water field test is successful, the chemical detection technology should be in use by the military and available for licensing within another year. An IMS-based system for detecting land mines would probably be ready for field use a year or two after that.

In the area of foam countermine development, researchers are attempting to create a barrier to neutralize mines. Rigid polyurethane foam is now under investigation for this purpose. In recent field tests, the quick-hardening foam proves to be an effective cushion for vehicles and soldiers against land-and water-mine explosives. It successfully withstands the weight of trucks and tanks. Further work and tests are ongoing and focusing on experiments in the air, soil, and water.

For more information on Sandia's research and development into landmine detection and clearing, contact Sandia National Laboratories at (505) 844-8066, or check out the web site at www.sandia.gov.

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DS1232LP	5V - 5% or 10%	✓	✓	✓	✓		8-pin DIP 8-pin SOIC
DS1705/6 DS1706x	5V - 5% or 10% 3.3V - 5%, 10% or 20%	✓ or	✓	✓	✓	✓	8-pin DIP 8-pin SOIC
DS1707/8 DS1708x	5V - 5% or 10% 3.3V - 5%, 10% or 20%	✓	✓	✓		✓	8-pin DIP 8-pin SOIC
DS1810-13 DS1815-18	5V - 5%, 10% or 15% 3.3V - 10% or 20%	✓ or	✓	✓*			SOT-23 TO-92
DS1832	3.3V - 10% or 20%	✓	✓	✓	✓		8-pin DIP 8-pin SOIC
DS1834	5V - 5% or 10% and 3.3V - 5%, 10% or 20%	✓ &	✓	✓			8-pin DIP 8-pin SOIC

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Superscalar Processor Delivers 400 MIPS For DSP And Control Needs

Scalable DSP Engine Quickly Executes Complex Algorithms Thanks To Dual MACs, Dual ALUs, And A 200-MHz Clock.

Dave Bursky

COVER FEATURE

The increasing complexity of signal-processing algorithms used in communications systems has pushed most integer DSP chips to their limit. As a result, designers are being forced to employ multiple chips to execute the desired operations. With typical throughputs of 40 to 100 MIPS, such uniscalar DSP engines are performance-limited, especially in new communications applications such as GSM and other digital standards, as well as implementing key portions of algorithms such as Viterbi decoding. However, when multiple processors are used, system cost and power goes up, while simultaneously, programming complexity increases since the algorithms must be partitioned across multiple processors.

Some of the latest DSP chips have begun adding resources so that multiple execution units on a single chip can tackle more-complex communications algorithms. However, just adding more resources to an architecture doesn't always deliver the desired result, since the architecture may have limitations that place an upper cap on performance. That's where designers at ZSP Corp. saw the need for a scalable, superscalar digital-signal processor that was easy to program and could also handle system control operations. As a result, the superscalar 10X DSP architecture was crafted, and the first chip to result from the architectural definition is the ZSP16401. Its designers expect the processor architecture to deliver up to a 10-fold speed improvement over existing uniscalar 16-bit solutions, while reducing overall system power and cost.

The initial implementation, the ZSP16401, is optimized for communications infrastructure applications, such as in cellular base-station systems. At its core is the superscalar four-instruction-issue 16-bit integer engine that contains two independent 16-bit ALUs and two 16-bit single-cycle MACs *(Fig. 1)*. That core is surrounded with instruction and data caches, a dual-access 48-kword (96 kbytes) RAM for program and data storage, a pair of serial ports, two timers, a memory interface unit and DMA controller, a host-system interface, and a device emulation controller and JTAG test port. When clocked at 200 MHz and powered by a 3-V supply, the processor can deliver a sustained throughput of 400 MIPS while consuming less that 1.9 W.

An Evolving Processor

Besides its high throughput, ZSP's superscalar DSP engine was designed for scalability, both in terms of on-chip resources and future extensions to handle 32-bit integer and floating-point operations. Consequently, as new target market segments evolve, the processor also evolves, changing its mix of on-chip functions, adding new instructions, extending the ALU and multiplier data paths to 32 bits, and so on. In the meantime, the ZSP16401 will offer designers a host of resources that will make short work of most communications algorithms.

For instance, results from the dual single-cycle 16-bit MACs can be saved in a single 40-bit accumulator to handle operations such as (16 by 16) + (16 x 16)], thus maintaining signal precision and minimizing round-off noise. For high-precision computations, the two MACs can be "combined" to perform a 32-bit single-cycle operation and deliver a 40-bit result. Complex multiplies also can be handled with quick dispatch—just two clock cycles are required for a complete complex multiplication.

Special instructions incorporated into the DSP engine improve the circuit's ability to execute complicated algorithms quickly. The complex multiplication is just one example. Another is the inclusion of software support to perform Viterbi decoding through the use of a single-cycle add-compare-select instruction. Single-cycle bit-manipulation instructions also are part of the processor's repertoire to allow the chip to handle control and protocol operations. The processor's simple load/store architecture is easy to understand and there are almost no hidden machine states (few mode bits), thus keeping all operations visible to the programmer.

A large, on-chip dual-port SRAM provides 48 kwords of storage—40 kwords can be used as instruction or data storage, while the remaining 8 kwords are data-only memory, and are shared by the data unit and the DMA controller. Programmers have full control over use of the 40-kword block as to how much is used for instructions versus data. Also on the chip is a 2-kword boot ROM that supports the processor boot-up sequence and JTAG-based emulation.

The superscalar architecture includes multitasking support through a low-latency multilevel interrupt structure with programmable priority levels, and efficient context switching support. The on-chip DMA channel supports fast I/O transfers without cycle stealing—a feature not found on most other DSP chips. Up to 8 kwords of the dual-access RAM can be used for DMA transfers to the host peripheral interface, the serial ports, or the memory interface unit (MIU). The MIU supports off-chip memory expansion and provides a total address space of 128 kwords (64 kwords of external program space and 64 kwords of external data space). It also can support four decoded off-chip peripherals and provides independently-programmable wait states, accommodating peripheral functions and memories of any speed.

To achieve the high throughput, designers at ZSP exploited instruction-level parallelism, caching and pipelining, and used branch prediction. The register-based architecture allows all ALU instructions to use any register as a source or destination, and all multiplication or MAC instructions can use any register as a source, and a subset of the registers as their destination. As a result, most bottlenecks associated with accumulator-based approaches are eliminated and compilers can easily perform register reallocation and renaming to efficiently generate the executable code. Also, the ability to read and write the program counter allows the compiler to generate position-independent code.

The processor only has four functional mode bits, which helps reduce the compiler's complexity and eases the programmer's task. As previously mentioned, there are no hidden process states which gives complete state visibility to the compiler and programmer. Double-word loads and stores do not have any alignment restrictions, which also helps reduce code-generation complexity. Double-word load and store operations also provide an efficient mechanism for fast context switching, allowing the processor to quickly save its state. All memory accesses use loads and stores. Load and Store instructions with immediate offsets facilitate simple stack accesses (push and pop operations).

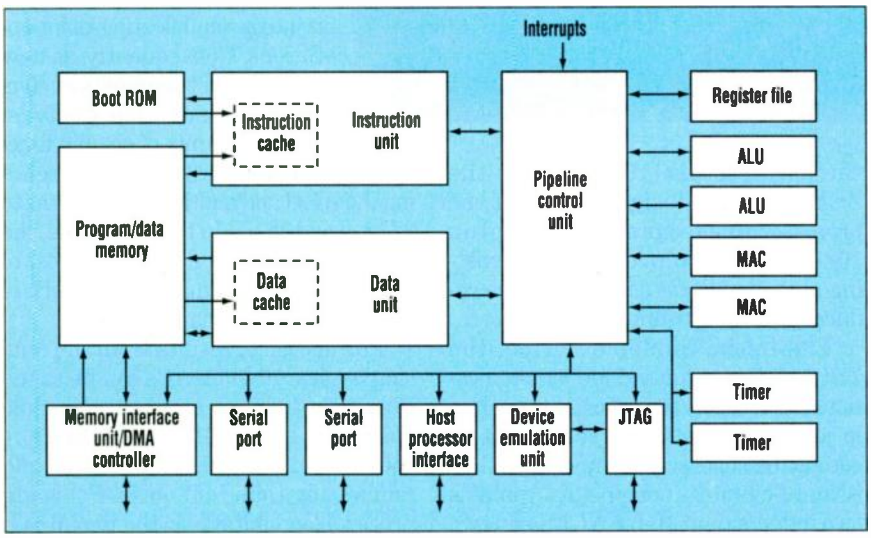
The processor's register file that supports the multiple ALUs and MACs consists of sixteen 16-bit general-purpose registers that also can be addressed as eight 32-bit registers. The functional blocks use the register file as the source and destination, but data also can be moved directly between any two operand registers. In addition, any register can be used as a stack pointer.

Control The Pipe

Supporting processor operations is a pipeline control unit that keeps track of multiple instructions in the pipeline, the interrupt requests, and other housekeeping functions. Five stages in the pipeline include a Fetch and Decode stage in which four instructions are fetched and decoded; a Group stage where up to four instructions are put into a group; a Read stage that reads the contents of the register file; an Execute stage during which the instructions are executed and memory is read; and a Write stage in which results are written into the register file.

As part of the Group stage, the pipeline control unit groups instructions by checking for and resolving data and resource dependencies. It also allows any functional unit to use the result from any other function unit in the next cycle (prior to the result being written into the operand register file).

Situated between the pipeline control unit and the dual-access RAM are the instruction and data units, each of which packs a small cache that helps buffer the data flow between the pipeline controller and the RAM. The instruction unit contains the cache, an instruction prefetch unit, an instruction fetch unit, and an instruction dispatch block. The instruction fetch block pulls in four instructions per cycle, while the prefetch unit takes advantage of branch-prediction logic and pre-fetches



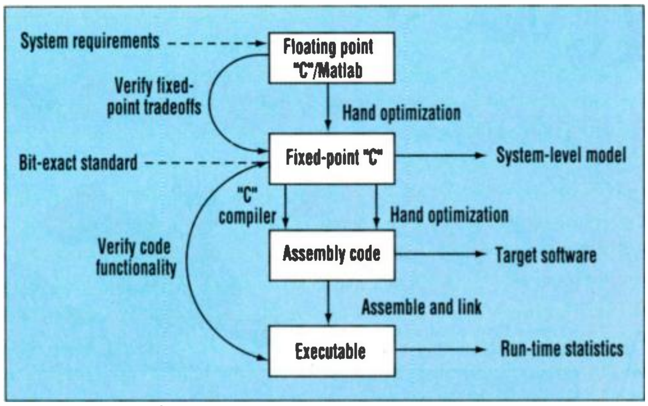
1. A superscalar DSP engine, the ZSP16401 developed by ZSP, can execute up to four instructions every clock cycle. The dual ALUs and dual MACs allow the processor to deliver up to 400 MIPS when the circuit is clocked at 200 MHz. An on-chip 48-kword dual-ported SRAM provides program and data storage.

READER SERVICE 202

instructions to minimize cache-miss penalties. Finally, the dispatch unit decodes and dispatches the four instructions to the processor pipeline for further processing.

Program loops can be executed from the instruction cache, reducing the number of accesses required to the RAM, thus reducing chip power consumption. And, thanks to the ability to prefetch instructions into the cache, loops of any size will execute efficiently.

The data unit consists of three sub blocks—the data cache, a data fetch unit, and a data pre-fetch unit. The data fetch unit pulls four 16-bit data words per clock cycle from the on-chip RAM, while the data prefetch unit helps manage the data to help maintain the high data throughput.



2. Software development for the ZSP processors is very straightforward. After system requirements are defined, the code is first developed in floating-point C or with a tool such as Matlab. Next, the code is converted into fixed-point C and then into assembly code and finally into executable code for loading into the chip's memory.

The processor can handle up to six external and ten internal interrupt sources, with the priority levels programmable for all interrupts except for the nonmaskable interrupt. Priority levels can be changed on-the-fly, allowing the circuit to adapt to changing system conditions and facilitating its use in real-time multitasking and multichannel systems.

To support control operations, the ZSP16401 includes four general-purpose I/O pins and two identical timers. Each I/O pin can be software configured to serve as an input or an output—inputs can be read or tested, outputs can be set, cleared, or toggled. The timers are programmable and can be configured for either one-shot operation or to deliver periodic interrupts. Each timer has 16-bit resolution and comes with a programmable 6-bit prescaler.

Moving data onto or off the chip can be done via the host peripheral interface or the high-speed serial ports. The serial ports are synchronous interfaces, each capable of transferring data at one-half the clock speed—100 Mbits/s for the 200 MHz processor version. Data is double-buffered to ensure transfer synchronization and data transfers can be done with 8- or 16-bit word lengths. Transmit and receive channels also can be independently clocked, allowing different speed transfers. For parallel transfers, the host processor interface provides an asynchronous 16-bit port with a maximum data transfer rate of 100 MHz. The bus supports Motorola- and Intel-style processor buses.

To ease system development and testing, the processor includes a full JTAG test port and on-chip full-speed emulation support. The four-wire serial port is IEEE 1149.1-compliant and provides full access to the device memory and registers as well as boundary-scan test capability. The port also can be used for in-system code and data downloads to test the chip or develop new software.

Simple Software

The simple RISC-like architecture of the ZSP 16400 DSP family leads to an easy- to-use development kit, the SDK16i, an integrated environment that consists of the typical tool suite—an assembler, linker, debugger, profiler, and compiler, with an optimizing compiler in development. All the tools, except for a simulator, are implemented by retargeting the Free Software Foundation's GNU tools. The tools are available for the Windows 95, Linux, and Solaris platforms. A hardware evaluation board provides designers with a versatile platform for application development. It packs two audio codecs, 128 kwords of SRAM and a flash ROM for program storage, buffering for the serial ports and host processor interface, and other resources. The company also spent much time developing a library of DSP functions and some full application software examples to provide designers with a headstart in doing their own code development.

The software development flow follows the industry's standard path, with the designer first outlining the system requirements and then developing a high-level version of the algorithms using either floating-point C language in a generic environment, or a program development environment such as Matlab. Once the code is developed, designers can convert to fixed-point C code as well as produce a system-level model that can be used to perform more advanced modeling of entire systems. Once code conversion is verified, the C code is compiled down to assembly code and finally turned into executable code *(Fig. 2)*. Alternatively, programmers can develop the code using assembly language, or a combination of compiler and hand optimization of the assembly code. This makes the software development process much simpler than that used for the high-throughput very-long-instruction-word processors.

The instruction set the ZSP16401 executes can loosely be grouped in seven basic categories: logic instructions;

```
           mov      %loop0, N - 1   /*perform this loop N times */

Dot_loop:  lddu     r4, r14         /*load two 16-bit operands into r5 and r4 */
           lddu     r6, r15         /*load two 16-bit operands into r7 and r6 */
           mac2.a   r4. r6          /*perform two mulitiplies and form a single 40-bit result */
           agn0     Dot_loop        /*branch if count ≥ 0; decrement count in %loop0 */
```

3. This code segment illustrates the simple structure for implementing a dot-product loop such as needed in correlation and convolution kernels. After the loop repetition parameters are defined, the loop consists of loading the data values and performing the multiplication and accumulation operation. After the first pass through the loop which requires three clock cycles, all four operations can be executed in a single cycle, allowing the processor to sustain a throughput of 400 Msamples/s.

arithmetic instructions; bit-manipulation operations; branch instructions; move instructions; memory-reference commands; and synthetic instructions and NOP (no operation).

A simple dot-product loop construct can be implemented with just four instructions that execute in a single cycle on the second through nth loop iterations, but requires three cycles on the first iteration (assuming the operands are located in the cache)—two cycles to load and one for the MAC with repeat *(Fig. 3)*. One additional instruction is initially required to specify the number of loops. If the operands must be fetched from the main memory, the time increases to seven cycles for the first iteration. Therefore, in one cycle, the processor performs four operand fetches, two 16-by-16-bit multiplications, and accumulates the products. As a result, the processor can deliver a sustained 400-Msample/s throughput—much faster than any traditional uniscalar DSP currently available. Other operations the processor can execute include FIR filtering at 2 taps/cycle, FFT butterflies in just 3.5 cycles/butterfly, and Viterbi trellis updates in just 1.25 cycles/node (a four-node update in five cycles).

As an example of the future needs of the wireless infrastructure market, consider the next-generation wideband CDMA cellular systems proposed for Japan and Europe. These systems are specified to have a maximum burst data rate of 2 Mbits/s. At such a data rate, the performance of today's programmable uniscalar digital-signal processors is not sufficient to perform operations such as channel error correction and source coding. Thus, manufacturers would be forced to use hardwired and less flexible solutions that carry considerable commercial risk in such a leading-edge system. By using a programmable solution such as the ZSP16401, manufacturers would be able to deal quickly and easily with modifications to the standards.

Price And Availability

Housed in a 160-lead PQFP, the ZSP16401 will sell for less than $50 apiece in quantities over 10,000 units. Samples are available from stock. A complete development board costs about $5000 (not including JTAG controller), and the software toolset sells for about $1500.

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The 1998 ISSCC Lives Up To Its Cutting-Edge Reputation

Roger Allan

With global communications as its theme, this year's IEEE International Solid State Circuits Conference (ISSCC), held Feb. 5-7 in San Francisco, Calif., was one of the largest conferences of its kind. As usual, the ISSCC continues to take on an international image, with over half of its presentations coming from overseas speakers. It featured 162 technical papers presented within 21 sessions, as well four evening panel sessions, six tutorials, and one short course. There was no shortage of leading-edge IC advancements including digital, analog, and mixed-signal devices. To help our readers navigate through many of the ISSCC's highlights, we've divided our coverage into four major areas: digital, communications, analog, and multimedia and sensor technologies.

In the digital arena, advances in memory and microprocessor ICs took the lead. Papers reported on gigahertz processors and gigabit-density memories. The latest DRAM, SRAM, and specialty memory developments also were unveiled at ISSCC.

In the IC-communications arena, ISSCC papers point to an increasing demand for higher-performance levels to satisfy wireless, network, and Internet technologies. Advances are also occurring in the development of on-chip passive components for RF communications, as well as in novel RF architectures.

Judging from many of the analog IC papers, CMOS seems to be the prevailing technology, particularly for low-power and high-speed ADCs and DACs. Nevertheless, for some applications, biCMOS is still needed to make devices that can operate at multigigahertz frequencies.

There were many important sensor and multimedia developments at the ISSCC, including sensors for imaging and touch. Multimedia progress seen at ISSCC included processors with throughputs of hundreds of MPOPS as well as many designed for the latest MPEG standard.

For a copy of the full "1998 ISSCC Digest of Technical Papers," which includes the speakers' slides, as well as a CD-ROM containing both the digest and slide supplement, contact the IEEE at the ISSCC web site, www.isscc.org, or write to Elizabeth Warner, Courtesy Associates, 2000 L St. N.W., Suite 710, Washington, D.C. 20036; (202) 973-8667; fax (202) 973-8722; e-mail: issscc@courtesyassoc.com.

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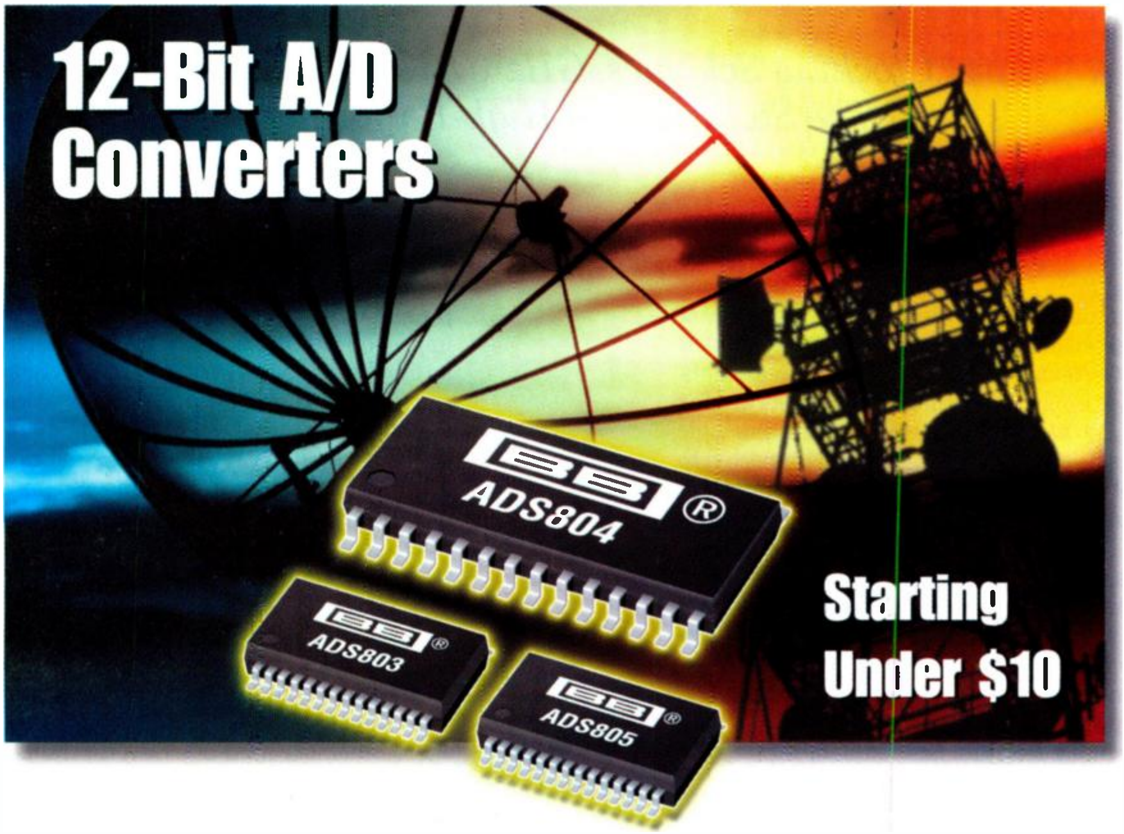

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Advanced Microprocessor And Memory ICs Bask In ISSCC's Glow

Novel Clocking Schemes, GHz CPUs, And Advanced Memory ICs Lead The Stampede Of High-Performance Breakthroughs.

Dave Bursky

SPECIAL REPORT

Processors operating at gigahertz clock rates and gigabit-density memories that keep pace with today's fast CPUs represent just a few of the digital technology developments trumpeted at the ISSCC. Advanced clocking techniques for high-speed systems and high-speed data-transfer schemes also were spotlighted, with system logic and both static and dynamic memories expected to operate at clock frequencies exceeding 600 MHz.

The past 10 years have witnessed the evolution of RISC architectures from simple scalar approaches to multi-instruction issue superscalar schemes that deliver hundreds of MIPS. In keeping with that trend, improvements in integration have researchers at IBM Corp., Rochester, Minn., looking beyond superscalar RISC in paper TP 6.1. According to David Luick, the paper's author, designers must look at a new set of design dynamics as physical, logical, and practical limits are encountered. And they must do this while new machine-independent languages reduce or eliminate many conventional constraints on instruction-set architectures and their associated microarchitectures.

In the future, highly parallel microarchitectures will drive logically shared resources (register files, L1 caches, etc.) to large numbers of logical ports. These resources will be implemented in a physically distributed fashion due to the dominance of wire delays and performance limitations of large N or N2 ported facilities. Execution units will be clustered and the compilers must be intimately aware of variable latency and path restrictions between clusters for good efficiency.

Forthcoming processors will be able to adapt to highly variable workloads, including history-based dynamic prefetching and trace-based path optimization. Also expected will be dynamic tuning of just-in-time-like compilation and recompilation. That will maximize parallelization as the machine "learns" each new application. Data-value prediction techniques also will prove to be highly productive when coupled with dynamic compilation.

Session 15, which detailed high-performance CPUs, offered up several building blocks toward the formation of the computer of tomorrow. A trio of presentations by IBM Corp. tackled three aspects of improvements to speed up program execution. In its first paper, IBM's Austin, Texas, division details a single-issue, 64-bit PowerPC integer processor that operates at internal clock speeds of up to 1.1 GHz when powered by a 1.8-V supply. Fabricated with 0.15-µm effective gate lengths and six layers of metal, the processor uses a four-stage pipeline and can execute 96 fixed-point ALU and load/store instructions (a subset of the PowerPC instruction set).

Trying multithreading to increase CPU performance, researchers from IBM's Rochester, Minn., laboratories created a version of the PowerPC architecture that executes two instruction-stream threads. As a result, it can hide the latency of memory accesses. Several trade-offs were made between chip area, the use of content-addressable memory, and the number of general-purpose registers. Consequently, for less than a 10% increase in chip area, processor throughput was improved by up to 30% for both uni- or multiprocessor configurations in AS/400 class systems.

Reduced RC Delays

Although smaller features allow circuits to run faster, thinner chip metal lines have higher resistances and the ensuing RC delays tend to limit circuit performance. To overcome that problem, the third IBM paper in Session 15 discusses a method that combines fine-line lithography and low-resistance copper-based interconnects. Employing 0.12-µm effective gate lengths and 0.2-µm features, designers at IBM's Burlington, Vt., facility fabricated a 32-bit PowerPC 750 dual-instruction-issue processor with six layers of copper metal (lowest-layer metal pitch is just 0.63 µm) on a chip that's just 40 mm^2. The copper layers are formed using a damascene process to keep manufacturing cost low and provide better connections to the vias than does the previous tungsten via and metal-etch-back approach used for aluminum interconnects.

Using copper drops the RC delays by about 30%. This allows the chip to operate at 480 MHz when

powered by a 2-V supply. At the high end of the temperature range—85°—the chip operates at over 500 MHz. In comparison, the 2.5-V version that used five levels of aluminum and tungsten local interconnections could only achieve an operating speed of just over 275 MHz. Furthermore, unlike the 1-GHz CPU described in the first paper, the PowerPC 750 is a full integer and floating-point processor with dual 32-kbyte on-chip caches and an integrated level-2 cache controller.

Speed is also the subject of the first of two papers by Digital Equipment Corp., Hudson, Mass., which details the design trade-offs in the stall-control circuits for 600-MHz instruction (integer and floating-point) queues designed into the Alpha microprocessor. The floating-point queue stall logic uses a one-hot encoding scheme to compare a queue free-entry count to an incoming instruction count. The less-complicated integer queue design employs a free-entry comparator, which saves about 35% of the area over that of logic used for the floating-point queue.

Pushing the speed of its P6 microprocessor to 450 MHz, Intel Corp., Hillsboro, Ore., details improvements made in the processor to lower operating voltage while increasing performance. This third-generation implementation packs 7.5 million transistors onto a 133-mm^2 chip. Its designers optimized it to operate from supplies between 1.4 and 2.2 V, allowing the chip to be used in both mobile and desktop applications. A 3.6-Gbyte/s back-side bus supports two L2 caches, with up to 2 Mbytes on separate cache chips.

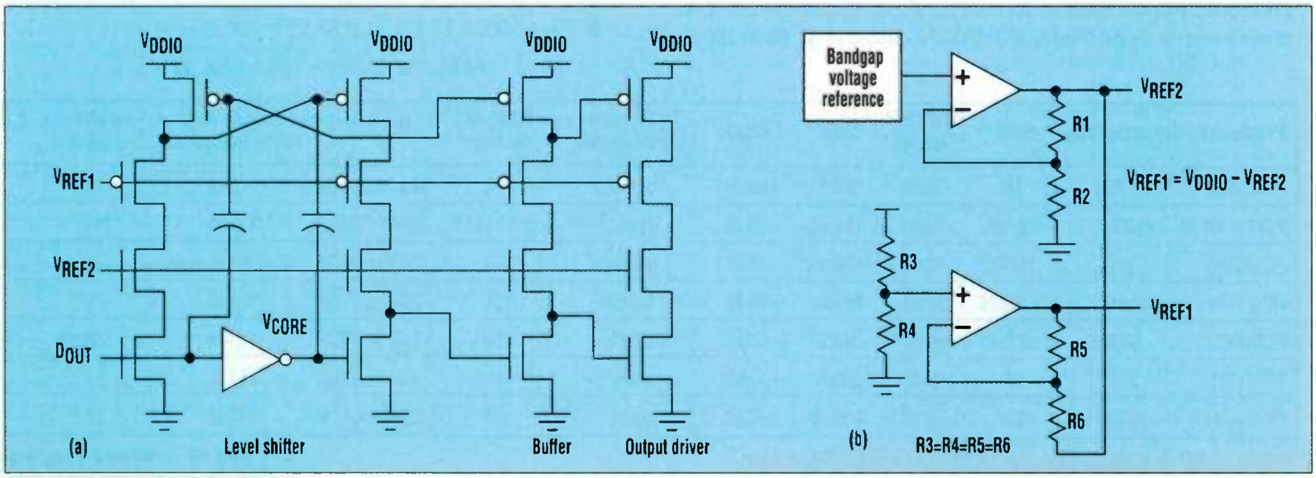
A higher-speed interface on a forthcoming version of the K6 processor is detailed by Advanced Micro Devices Inc., Sunnyvale, Calif. The x86-compatible CPU has a 100-MHz implementation of the Socket-7 bus (a 50% speed increase). With microarchitectural improvements, it delivers up to a 10% performance improvement without any internal clock-speed increase. Part of the architectural enhancements include instruction additions that support 3D graphics operations—19 floating-point vector operations. The instructions operate in a single-instruction/multiple-data fashion on 64-bit operands, much like MMX instructions. However, unlike MMX commands, operands consist of two sets of 32-bit single-precision values rather than integers.

During the process, designers were confronted with two issues. One was minimizing the amount of cycle time that would be occupied by uncertainties in crossing between the processor-clock and the bus-clock domains (where the processor clock is an integer or half-integer multiple of the bus clock). The other concerned the design of the I/O circuits to handle 3.3-V stresses, since the process was optimized for 2.1-V operation. To deal with timing issues, designers found a way to eliminate a latch used by the processor clock and reduce the hold-time. This was done by updating the processor-clock register only on processor-clock edges that don't coincide with a bus-clock rising edge.

Enhancing the I/O circuits required adding protection and speed-up circuits for a level shifter so that the internal 2.1-V logic can drive the 3.3-V I/O signals. The I/O block consists of a level shifter, a buffer, and an output driver *(Fig. 1a)*. To accelerate the circuit, capacitors were added to the level shifter, which allows the pMOS gates to couple up or down with the nMOS gate in the same stack. A bandgap voltage generator provides a constant reference voltage (independent of process, temperature, and supply voltage). That voltage is amplified and used to derive the two reference levels used by the I/O circuits *(Fig. 1b)*.

Targeted at low-power applications, the other presentation by DEC spotlights a 200-MHz version of the StrongARM processor. It consumes just 500 mW while delivering a throughput of about 230 Dhrystone MIPS. To minimize power consumption, the chip operates externally from 3.3 V, but internally runs from 1.5 V. About 2.5 million transistors make up the processor's integer ALU and multiplier, a 16-kbyte instruction cache, an 8-kbyte data cache, another 512-byte data cache, a memory-management unit, read and write buffers, and many on-chip peripherals.

To minimize power drain, several design principles were applied. For starters, wherever possible, standalone latches were avoided in favor of latches with logic embedded in them. That reduces circuit delays and lowers power consumption. The processor features three separate internal 1.5-V power-supply grids so that power-management modes can selectively turn on or off different portions of the chip. There's also a 3.3-V grid that supports the I/O



1. To interface the internal 2.1-V logic to the external 3.3-V world, designers at Advanced Micro Devices developed this three-stage level shifter. It includes speed-up capacitors to improve the speed of the level-shifting portion of the cell (a). A bandgap-based voltage reference is used to supply the dual reference levels needed to provide the key voltages to the level shifter (b).

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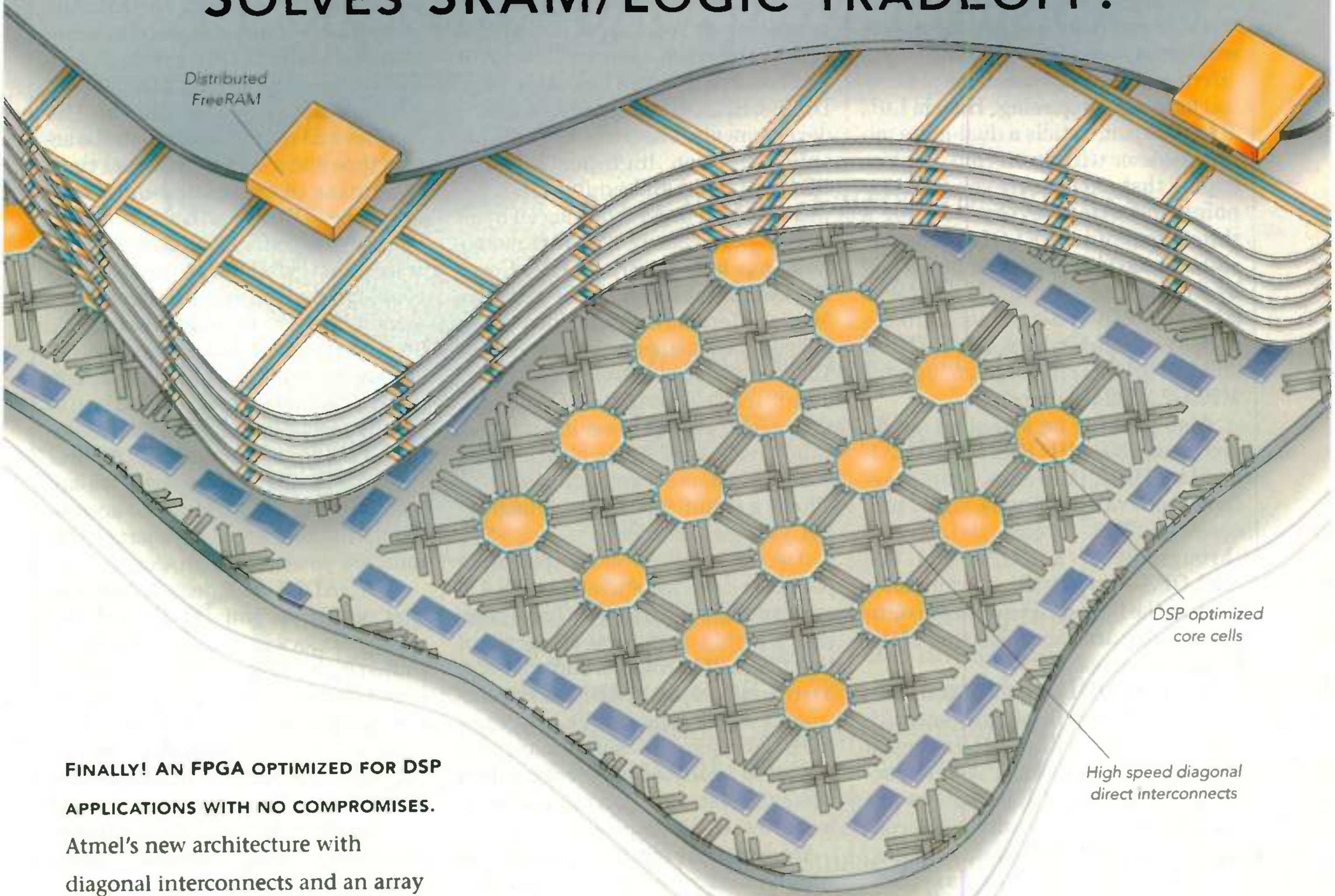

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AT40K10	10K–20K	576	4096	192	84 PLCC, 100 VQFP, 144 TQFP, 160 PQFP, 208 PQFP, 225 BGA, 240 PQFP
AT40K20	20K–30K	1024	8192	256	84 PLCC, 144 TQFP, 160 PQFP, 208 PQFP, 225 BGA, 240 PQFP, 304 PQFP, 352 BGA
AT40K30	30K–40K	1600	12,800	320	84 PLCC, 144 TQFP, 160 PQFP, 208 PQFP, 225 BGA, 240 PQFP, 304 PQFP, 352 BGA, 432 BGA
AT40K40	40K–50K	2304	18,432	384	84 PLCC, 144 TQFP, 2[illegible] PQFP, 225 BGA, 240 PQFP, 304 PQFP, 352 BGA, 432 BGA, 475 PGA

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Communications Applications Drive Novel Technologies At ISSCC

Increasing Reliance On Wireless, Network, And Internet Technologies Has Created A Relentless Demand For New Performance Levels.

Lee Goldberg

SPECIAL REPORT

The demand for faster, more versatile, and less expensive communications networks has greatly influenced the direction of electronics development over the past year. This fact was evidenced at ISSCC not only by the number of communications-related papers, but by the common themes they address. In fact, all three of the conference's plenary session talks have either communications or wireless themes.

In his talk, "GSM and beyond—the future of the access network," Johan Daneels director, industrial coordination, of Alcatel Telecom, Zaventem, Belgium, looks at the next generation of cellular/PCS technologies and speculates on the demands they would put on the semiconductor industry. Hitachi's general manager of its central research laboratory, Dr. Miciharu Nakamura, explores the future of semiconductors for wired systems in his paper "Challenges in semiconductor technology for multimegabit network services." Finally, Kanwar Chada of SiRF Technologies, Santa Clara, Calif., discusses the challenges he faced in lowering the cost and power of GPS systems. He explains that the task had proved even more formidable because it had to be accomplished while improving performance under the poor reception conditions found in many consumer applications.

Smaller, Smarter, Cheaper Silicon

As higher levels of integration are employed to reduce cost, space, and power requirements, many conventional notions about IC design are coming into question. This debate has resulted in a further blurring of the line between digital and analog systems, as well as interest in unusual RF architectures. Also of note, many conference papers concern themselves with the fact that "vanilla" bipolar silicon and CMOS are now being asked to perform jobs previously reserved for more exotic materials and processes. These and other innovations are making it possible to produce compact, low-cost, chips and chip sets for wireless products.

Two interesting papers on extending the frequency range of standard-process silicon devices managed to find their way into the communications arena. Paper 16.3, "A 3.5-mW, 2.5-GHz diversity receiver and a 1.2-mW, 3.6-GHz VCO in Silicon On Anything," by Philips Research Laboratories, Eindhoven, Netherlands, describes a new bipolar silicon IC technology called silicon on anything, which places active and passive devices on a standard bulk silicon wafer and then bonds its face to a good dielectric plate, such as glass *(Fig. 1)*. The silicon side of the sandwich is then etched away to reveal the buried oxide layer. A set of inverted bond pads enables the fabrication of low-power transistors and on-chip inductors, which have good electrical performance at 1 to 4 GHz.

Pushing the envelope a bit further, a group of researchers from the University of Florida in Gainsville present "4-GHz and 13-GHz tuned amplifiers implemented in a 0.1-µm CMOS technology on SOI and SOS substrates" (paper number 8.7). Employing partially-depleted silicon-on-insulator (SOI) and silicon-on-sapphire (SOS) nMOS transistors with floating bodies, the team delivered gains of 11 to 12 db for 4-GHz SOI devices, and 5 to 15 dB for 13-GHz SOS devices.

On-Chip Passive Breakthroughs

Some of the most intriguing breakthroughs are in the area of on-chip passive devices. Essential for interstage coupling, frequency generation, filtering, sampling, and other important functions, inductors, capacitors, and resistors must migrate back into ICs to realize maximum power, space, and cost savings.

IBM's Research Division presents "RF circuit design aspects of spiral inductors on silicon" (paper 16.1). In the paper, IBM explores the nuts-and-bolts factors affecting inductor design and performance. The effects of inductor area and crosstalk between devices are discussed, along with layout issues and design-optimization techniques.

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				Performance Improvement		
Device	Gates	Logic Elements	Embedded RAM	-2 Speed Grade (1)	-1 Speed Grade (2)	Supply Voltage
EPF10K30A	30,000	1,728	12 Kbits	40%	123%	3.3 V
EPF10K50V	50,000	2,880	20 Kbits	40%	110%	3.3 V
EPF10K100A	100,000	4,992	24 Kbits	35%	107%	3.3 V

1. Estimated performance with -2 speed grade using MAX+PLUS II v. 8.1 compared with -3 speed grade using MAX+PLUS II v. 8.0
2. Estimated performance with -1 speed grade using MAX+PLUS II v. 8.2 compared with -3 speed grade using MAX+PLUS II v. 8.0

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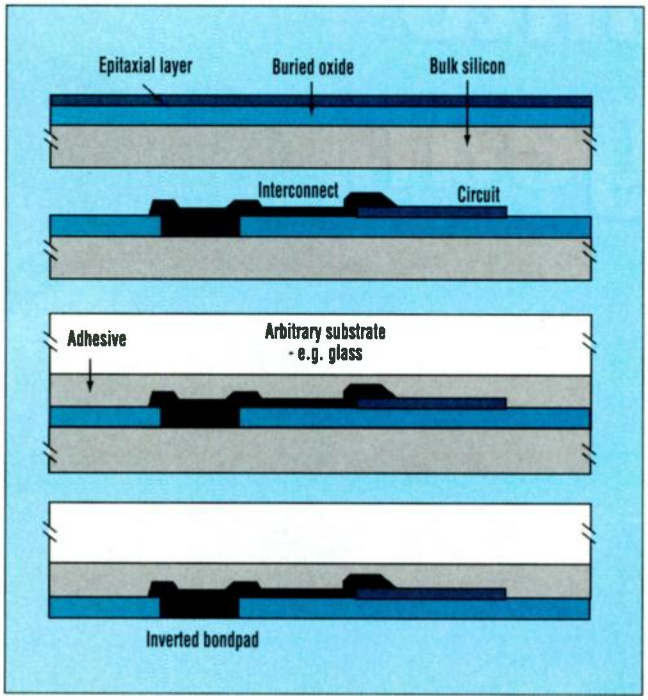
The ALTERA Advantage

A collaboration between Oregon State University at Corvallis, and Arizona State University at Tempe, yielded a development in on-chip passives. In paper 8.6, "A fully integrated CMOS 900-MHz LNA utilizing monolithic transformers," the team describes how they were able to develop a monolithic transformer which had significantly better electrical characteristics than can normally be obtained when fabricating simple on-chip inductors. This technology could prove useful anywhere there is a need for coupling amplification stages within an IC.

Perhaps the most imaginative approach to this endeavor came from Nippon Telephone's Wireless Systems Laboratories, Kanawaga, Japan. Their "K-band silicon MMIC amplifier and mixer using three-dimensional masterslice technology," (paper 16.4) describes how a standard silicon IC process can be used to fabricate 3D structures. By using a single oxide layer and four, 2.5-µm polyimide insulator layers, designers can now create highly isolated capacitors, inductors, and thin-film micro-strip (TFMS) transmission lines on a chip *(Fig. 2)*. As a bonus, the polyimide is well-suited for gold metalization, which further enhances the circuit's performance. Operating at 24 to 30 GHz today, the authors are confident that millimeter-frequency devices will soon be possible.

Another surprising development in on-chip passives comes from a team at the Center for Integrated Systems, Stanford, Calif. In paper 16.6, "Lateral flux capacitors (fractal capacitors)," the authors describe how they have fabricated a capacitor element using a fractal structure which exploits both the lateral and vertical electric fields within a chip. This technique allows them to increase unit capacitance per unit area, while reducing unwanted interactions with the substrate that cause parasitic effects. Using conventional 0.5-µm design rules and a classic fractal structure, the team was able to demonstrate a three-fold increase in capacitance per unit area.



1. The Silicon-on-Anything process developed by Philips Research allows the creation of on-chip passive components with very-high-quality factors. An insulator (typically glass) is bonded to the active surface of an IC. The substrate is then back-etched down to the buried oxide layer to expose the chip's inverted bond pads and eliminate parasitic coupling to the substrate.

Novel RF Architectures

Throughout the RF-related sessions, it has become apparent that the tried-and-true superheterodyne receiver architecture may not always be the best solution for an integrated wireless design. One popular alternative of late has been the direct-conversion, or zero-IF receiver. Although difficulties with linearity and spurious mixing products have kept it from many mainstream applications, its inherent simplicity would make it ideal for one-chip receivers.

In paper 3.1, "A 900-MHz transceiver chipset for two-way paging applications," researchers from Wireless Access, Santa Clara, Calif., and Motorola, Tempe, Ariz., demonstrate how they were able to develop a bipolar silicon front end and CMOS baseband chip that could have many uses, aside from pagers. Employing a modified direct-conversion architecture, the chip set's designers claim that the receiver is able to significantly reduce local-oscillator (LO) leakage and improve overall performance by downconverting the incoming signals to a very low IF before the carrier is thrown away.

This hybrid system also allows the signal amplification to be distributed between the RF, IF, and baseband stages. Thanks to their low cost and power, products like this can be expected to show up in embedded messaging applications ranging from PDAs to vending machines.

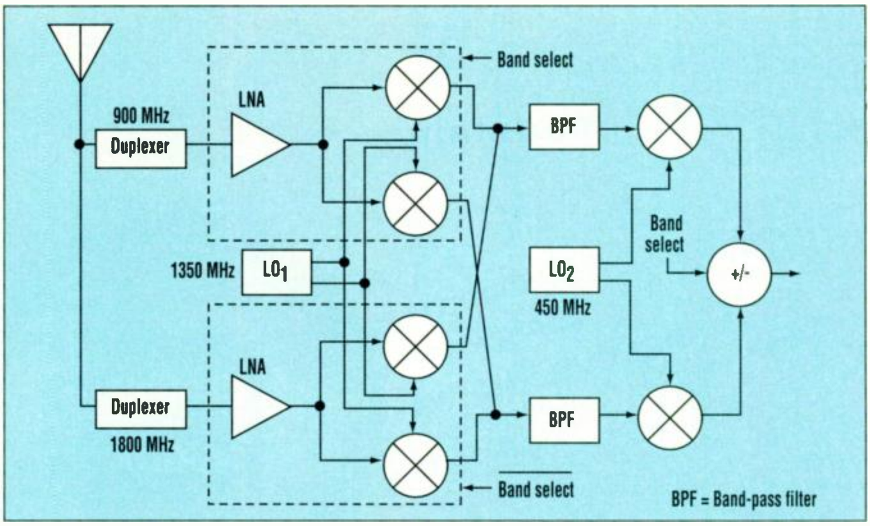
Direct conversion is a hot topic. In paper 8.3, "A direct conversion L-band tuner for digital DBS," Analog Devices Inc., Wilmington, Mass., presents a set-top-box tuner that uses direct conversion to reduce component count and eliminate the need for SAW filters between IF stages. To keep in-band interference low, the local oscillator is run at one-half the operating frequency, and doubled on-chip using a novel polyphase quadrature generator circuit. On-chip, digitally controlled attenuation allows the tuner to accept a wide range of input signal levels.

Another nontraditional receiver design has been introduced by a team from the University of California at Los Angeles, to meet the challenge of constructing a dual-band receiver for cellular (900-MHz) and PCS (1.8-GHz) operation. In paper 8.2, "A 900-MHz/1.8-GHz CMOS receiver for dual-band applications," they describe a chip intended for GSM-based wireless telephony. The chip uses a Weaver-type architecture to perform two consecutive quadrature down-conversion operations *(Fig. 3)*. This enables the receiver to select or reject either of two frequencies located symmetrically around a single low frequency without creating excessive in-band mixing harmonics.

Sometimes, older ideas have a way of being reborn in new technologies. This is exactly the case with a development presented by the Swiss Federal Institute of Technology in Lusanne. In paper 8.4, "A 2-V, 600-µA, 1-GHz, biCMOS super regenerative receiver," the authors describe how they

adapted an architecture that was popular for vacuum-tube radios, to modern wireless data applications. Intended for high-speed, short-haul links, the ultra-simple device can operate on a 2- to 3-V supply up to 100 kbits/s over a 300 to 1500-MHz carrier.

In paper 3.2, "A CMOS IF transceiver for narrowband PCS," presented by Crystal Semiconductor, Austin, Tex., the researchers developed a fully integrated IF stage that uses DSP techniques to reduce power consumption and the number of passive components used in handheld telephones. The receiver takes a 21.4-MHz IF input and converts it to a digital complex baseband that subsamples at 16.8 MHz to produce a 4.6-MHz product. It is then mixed down to 400 kHz and digitized by a complex bandpass Δ–Σ modulator to a 1-bit complex signal, which is decimated to 56 kHz by an integrator-comb filter.



3. This dual-band receiver takes advantage of the fact that the 900-MHz cellular band and 1800-MHz PCS bands are nearly harmonics of each other. The receiver's Weaver-type, single-sideband architecture performs two quadrature downconversions to produce a signal that contains mixing products from both bands, located symmetrically about the local-oscillator frequency. This design allows easy selection of the desired signal.

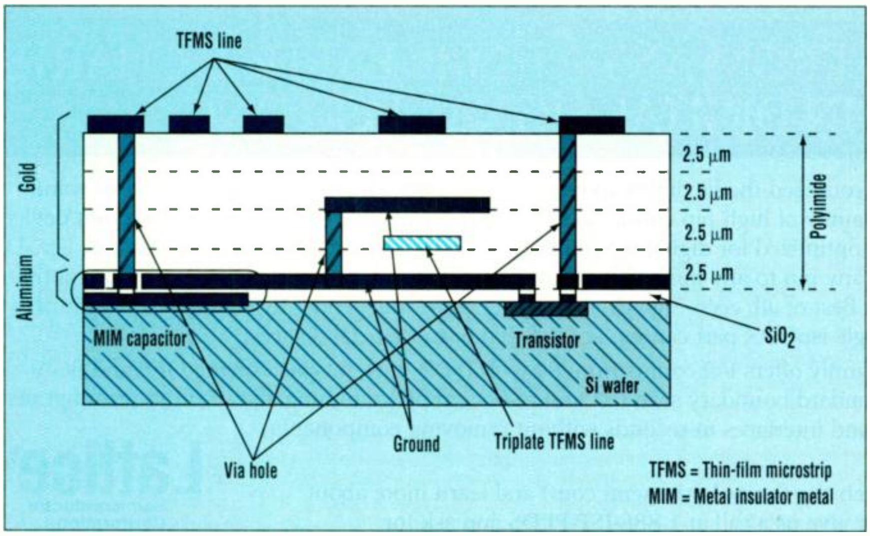
The transmit section accepts a digital, complex baseband signal and outputs a 69.4-MHz IF signal—and performs an inverse function on it. Careful attention to the upconversion and downconversion frequency plans allows the use of less accurate, less complex PLLs for frequency control, and minimizes image noise to keep the circuit within the tight FCC specifications for PCS operations.

Output stages are typically problematic, especially when efficiency and high linearity are required. Both Philips Research, Briarcliff Manor, N.Y., and Hewlett-Packard Laboratories, Palo Alto, Calif., address some of the problems plaguing designers as batteries shrink, operating frequencies rise, and modulation schemes become more complex. In paper 3.5, Philips researchers describe how they developed an inexpensive silicon driver amplifier circuit that incorporates a power control loop and filter with 25 dB of range, and a voltage regulator, to bias a low-cost discrete power device.

HP researchers have produced linear output from an amplifier run in its non-linear region by use of an envelope elimination and restoration (EER) scheme. This technology demonstrates a novel approach to boosting the efficiency of power amplifiers used in applications where high linearity is required. It's accomplished by decomposing an RF input into a low-frequency envelope and RF phase. A switching power supply amplifies the low-frequency component and feeds it into the power amplifier's power inputs. The RF component is then fed into the amplifier's signal input, resulting a switched-mode operation that delivers both high linearity and high efficiency.

At ISSCC, we can also see that work is beginning in earnest on producing cost-effective devices for use in the recently approved 5 GHz band. A team from Lucent's Bell Laboratories presented a paper entitled "A Fully Integrated 2.7 V, 0.35 µm CMOS VCO For 5 GHz Wireless Applications." (Paper 14.7). Among other items of interest, the paper describes how designers coax high performance out of MOS silicon by using the transistor's parasitic effects as working passive elemnets in the design.

Satellite communications is one of the wireless markets experiencing rapid growth. It's no surprise then, that there are more than a handful of papers concerning everything from



2. NTT's 3D Masterslice technology allows the fabrication of high-quality passive components on thin-film-microstrip (TFMS) transmission lines. Using a single oxide layer and four polyimide dielectric layers, it is possible to attain unusual geometries which provide high performance and levels of isolation from the substrate not possible with conventional technologies.

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satellite data to GPS navigation technologies coming from ISSCC.

Found In Space

A team from Stanford University's Center for Integrated Systems explores many solutions to the power constraints and reception problems anticipated for the next generation of embedded GPS systems in paper 8.1, "A 115-mW CMOS GPS receiver." They describe a GPS receiver architecture with a fully differential signal path. The chip integrates a low-noise amplifier, a set of double-balanced mixers, IF amplifiers, active filters, and 1-bit oversampled ADCs. When coupled with a DSP-based computation unit, the chip set can provide inexpensive, low-power GPS functionality for many embedded applications.

Satellite data is also hot, especially in high-bandwidth multimedia applications. With this in mind, researchers at Philips Electronics, Eindhoven, the Netherlands, introduced "A power-efficient, single-chip, OFDM demodulator and channel decoder for multimedia broadcasting," in paper 2.6. Their chip is intended to receive and decode orthogonal-frequency division multiplexed (OFDM) signals, a noise-resistant modulation scheme favored by many satellite applications, and recently chosen for the new digital audio broadcasting (DAB) standard. While the 4.5 million-transistor chip has been designed specifically for DAB applications, the low-power architecture and mixed-signal processing technology may lay an important cornerstone for other satellite-oriented products.

Galloping Gigabits

Wired communication technologies are also well represented at the conference. With cable modems, ADSL, and other last-mile transmission technologies gaining a foothold in residential broadband networks, it is no surprise that researchers from Broadcom Corp., Irvine, Calif., open session 13 (Datacom/telecom), with a paper on a 70-Mbit/s last-mile technology. Titled "A 70 Mbit/s variable-rate 1024 QAM cable receiver IC with integrated 10-bit ADC and FEC decoder," this variable-rate, QAM receiver uses a sampled-rate IF architecture, and incorporates a 10-bit ADC and a group of analog PLLs for clock generation. Intended for desk-top terminals and cable modem applications, the device has an on-chip FEC decoder which meets all European DVB/DAVIC standards for multimedia broadcast. Its variable-rate architecture lets it adjust to changing line conditions with symbol rates from 1 to 7 Mbaud/s.

The networking arena has seen a maturation of 100-Mbit/s technologies, and an intense focus on driving down the cost of 1-Gbit/s equipment. There also was significant activity surrounding efforts to commercialize technologies which can support data rates of 10 Gbits/s or greater .Session 19, "Multi-gigahertz serial data," illustrated many approaches for surmounting the 10-Gbit frontier. Among them is "A 4.25-Gbit/s CMOS Fibre Channel receiver," presented by NEC Corp.'s Silicon Systems Research Lab, Kanawaga, Japan. In paper 19.3, a transceiver is described which has an integral asynchronous binary tree-type 1:8 demultiplexer to allow it to be fed from multiple links running at lower speeds. To address the difficulties of distributing a clock fast enough to support a 4-Gbit/s transfer rate, its designers developed a parallel architecture, which is driven by a lower-speed multiphase clock. Since the transceiver is based on standard Fibre Channel technology and consumes only 60 mW, we can expect a close relative of this prototype to find its way into the next generation of networks.

NEC Corp, Kawasaki, Japan, delivers a paper titled "A 10-Gbit/s SiGe bipolar framer/demux for SDH systems." Fabricated in a SiGe bipolar process, this device employs data-shift selection to give its frame-detection control circuitry an extra timing margin—a critical feature as data-transmission rates approach 10 Gbits/s.

High-speed networks like this one will require switching networks that can handle them. For this reason, a group of technologists from Sweden's Royal Institute of Technology, Ericcson Microwave Systems, Mondial, Sweden, and Hughes Research Labs, Malibu, Calif., have collaborated on a new multi-Gigabit switching project. Their paper, "A 2-V, 120-mA, 25-Gbit/s 2-by-2 crosspoint switch in InP-HBT technology," describes an asynchronous switch that operates at 20 Gbits/s with no measured errors (paper 13.3).

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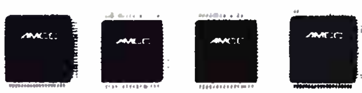

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CMOS Technology Prevails In Analog Designs At ISSCC

New Developments In Low-Power Devices And CMOS Technology Highlight The Future Of Analog ICs.

Cheryl Ajluni

SPECIAL REPORT

At this year's ISSCC, two major trends in analog design are taking center stage: the continuing growth of portable electronic systems requiring low-voltage and low-power building blocks, and the continuing move toward lower-cost CMOS processing. Both are characterized by demands for high speed (over a 100-MHz update rate) and high accuracy—digital-to-analog converters (DACs) with more than 10 bits of accuracy. There's also a call for for higher clock frequencies and wider signal dynamic ranges. Despite some lingering doubt as to whether pure CMOS devices can actually achieve the speeds needed, CMOS is the choice for many of the designs presented at this year's conference.

One example is the development of a CMOS stereo Δ–Σ DAC for portable digital-audio systems that consumes a mere 4.1 mW from a 1.5-V supply. As detailed in paper 4.2, "A 1.5-V, 4.1-mW dual-channel audio Δ–Σ digital-to-analog converter" from Asahi-Kasei Microsystems, Kanagawa, Japan, this development is of particular significance because low-power-consumption DACs are crucial to long battery life in audio playback equipment. The DAC's total power dissipation is five times less than any dual-channel audio DAC reported to date. The device achieves a 90-dB dynamic range over a 20-Hz to 20-kHz passband. The chip is fabricated in a 0.6-µm CMOS process that includes low-threshold devices and is just 5.3 mm^2 in size.

These results were achieved in part by using a multibit Δ–Σ modulator, which reduces quantization noise and is suitable for low-power implementations. It allows the use of a lower oversampling-ratio, and tolerates a relaxed out-of-band filtering specification. The device also uses 15-level quantization with third-order noise-sampling at 64 times the oversampling range. As a result, speed requirements are reduced, which enables 1.5-V operation and a corresponding reduction in power dissipation.

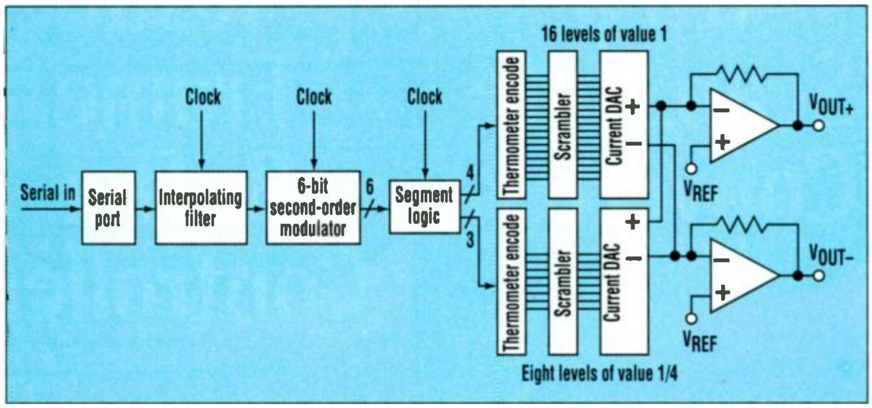
Another unique Δ–Σ 0.6-µm CMOS DAC development comes from Analog Devices, Wilmington, Mass. It addresses the need for low-cost DACs with a very high dynamic range for consumer products such as DVD systems. This DAC also promises to solve performance problems faced by today's more conventional Δ–Σ DACs. As detailed in paper 4.3, "An 11-dB SNR oversampling DAC with segmented noise-shaped scrambling," it uses a 6-bit modulator and a segmented noise-shaped scrambling to achieve a 113-dB dynamic range over a 20-kHz bandwidth *(Fig. 1)*. With full-scale inputs, it achieves 100-dB total harmonic distortion for a 2-V rms differential output. To obtain a high signal-to-noise ratio in a small die area, the DAC uses a continuous-time output stage. The result is a chip with a die area of 3.2 by 3.1 mm. A dual return-to-zero circuit eliminates errors caused by intersymbol interference.

An interesting element of this design is a technique known as segmented scrambling, which circumvents the problem of distortion caused by element mismatch. During operation, a 6-bit word is split into two smaller, individually noise-shaped subwords. The words are then individually scrambled by a noise-shaped scrambling technique and applied to two separate DACs.

BiCMOS Still Needed

High-performance LANs and wireless ATM systems require multigigahertz high-speed ICs. One such device is a multifunctional up/down converter, operating with a single bias voltage of 2.6 to 5.2 V. The IC, developed by NEC Corp., Kawasaki and Sagamihara, Japan, is made on a 0.4-µm, 22-GHz biCMOS process, and is presented in paper 23.6, "A 5-GHz-band biCMOS up/down-converter chip for GMSK modulation wireless systems." The chip is just 3.0 by 2.4 mm *(Fig. 2)*.

The chip uses a distributed single power supply to get an independently optimized, constant current source for each of its high-frequency circuits over a wide dc voltage range. A low-noise attenuating amplifier that requires no additional power dissipation is used. A high-gain, small-phase-variation limiting amplifier provides Gaussian-filtered minimum-shift keying (GMSK) modulation compliance. And, a frequency-doubling method keeps phase noise and power consumption of the local oscillator low. The chip also has ground line shielding for the circuits in each path to enhance electrical isolation



1. A 6-bit modulator and a segmented noise-shaped scrambling scheme allows this DAC design from Analog Devices to achieve a 113-dB dynamic range over a 20-kHz bandwidth. One of two channels used in the device is depicted here.

between down- and up-converter paths.

In paper 20.2, "A 100-MHz, 50-Ω, -45-dB distortion, 3.3-V CMOS line driver for Ethernet and fast Ethernet networking applications," from Plato Labs, San Jose, Calif., a fast-line driver for networking applications is proposed. The device can be used to drive cables with large, low-distortion sine waves for 10Base-T, and sharp-edged pulses for 100Base-T data communications. The device is based on a fully differential current-feedback architecture that allows it to achieve small- and large-signal closed-loop bandwidths over 100 MHz. The device is made on a 0.4-µm single-polysilicon, triple-metal p-well CMOS digital process without a capacitor module.

Researchers from the University of California at Los Angeles have devised a DAC that's optimized for frequency domain applications such as embedded systems products heavily populated with digital circuitry. The 10-bit device achieves a spurious-free dynamic range (SFDR) of 68 dB at 250 Msamples/s and a 20-MHz output signal. At 120 MHz, it comes close to the Nyquist frequency, achieving an SFDR of 57 dB. The DAC is fabricated on a 0.5-µm single-polysilicon, triple-metal digital CMOS process. Further details are summarized in paper 14.1, "A 10-bit 250-Msample/s CMOS DAC in 1 mm^2."

Many wireless applications, like cellular base stations, require a Nyquist-rate analog-to-digital converter (ADC) with a minimum SFDR of 65 dB and a sampling rate of 10 MHz. A key problem is the converter's nonlinearity, which limits its sensitivity to component matching, and thus, performance. Although calibration rectifies this situation somewhat, most techniques in use today can only be performed once or cause an interruption in the data flow to recalibrate the converter. Researchers at the Center for Integrated Systems at California's Stanford University have found a way around this problem through continuous calibration as presented in paper 9.4, "A continuously-calibrated 10-Msample/s 12-bit 3.3-V ADC." With this approach, a converter can function normally, despite the presence of environmental fluctuations and supply variations, because its errors are periodically corrected without interrupting its output. Operating in the analog domain, this calibration avoids the need for high-linearity calibration hardware or complex signal processing.

To test the technique, researchers applied it to a pipelined 10-Msample/s, 12-bit ADC, fabricated on a 0.5-µm, single-polysilicon, four-metal, CMOS process. Powered by a 3.3-V supply, the circuit can digitize a 4.8-MHz signal with a peak SFDR of 67 dB.

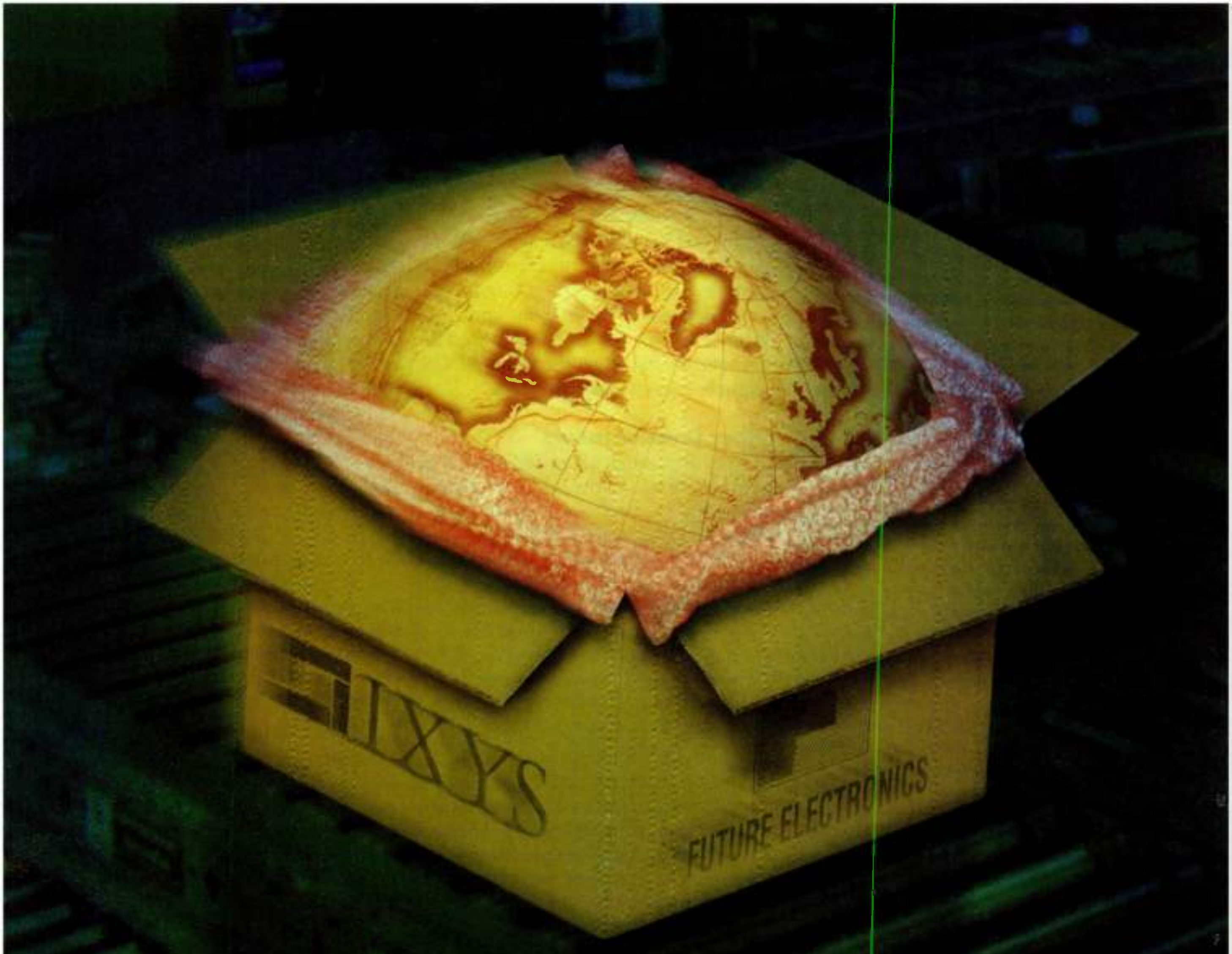
Researchers from Texas Instruments, Dallas, have identified a means of doubling the throughput of an ADC for a given analog power consumption. The approach, as highlighted in paper 9.5, "8-bit 75-Msample/s 70-mW parallel pipelined ADC incorporating doubling sampling," calls for the use of a double sampling technique in the residue signal path of a 1.5-bit-per-stage architecture. Residue amplifiers and sub-ADC comparators are shared between two time-interleaved channels, and the sampling capacitors in the second stage are scaled to reduce power consumption. This technique is used in an 8-bit parallel-pipelined ADC and results in a sampling rate of 75 Msamples/s and power consumption of 70 mW. The 3.3-V ADC measures 5.5 mm^2 and is made on a digital, four-metal CMOS process with no special mask layers for passive components.

Researchers at the University of California at Davis have devised a method for dealing with the limitations of ADC interface speed on the throughput rate of DSP systems operating on analog inputs. Their proposed solution is in paper 9.2, "Digital background calibration of a 10-bit 40-Msample/s parallel-pipelined ADC." It details a time-interleaved pipelined ADC that uses monolithic digital background calibration to overcome the effects of offset and gain mismatches between channels, all on one CMOS IC.

The method works by adding a calibration signal to the ADC input and processing it simultaneously. The advantage is that the calibration signal acts as dither, effectively improving system linearity. It is believed that these same techniques, coupled with a better match between the channel gains and offsets, can result in interleaved ADCs with more than 10-bit resolution.

In a similar paper, also from the University of California at Davis, "Analog background calibration of a 10-bit 40-Msample/s parallel-pipelined ADC," researchers propose a time-interleaved ADC that uses monolithic analog background calibration to help match the gains and offsets of component-pipelined ADCs. Traditionally, ADC sampling rates have been a limiting factor in the operational speed of signal-processing systems. While the sampling rate at the ADC interface can be increased using time-interleaved, multiple-component ADCs, mismatches in offsets, gains, and sampling times among the component ADCs limit ADC system performance. The approach proposed by the Davis researchers bypasses this effect by using an expandable adaptive-background-calibration technique for parallel ADCs, and a calibration loop that uses a mixed-signal integrator. The result is an ADC with an expandable architecture, requiring M+1 high-speed ADCs and one reference ADC to increase the sample rate by a factor of M.

The ADC uses a front-rank sample-and-hold to eliminate the effect of channel-timing mismatches. As a result, at any time, two of the three ADCs are processing the input in a time-interleaved fashion. The result is a conver-



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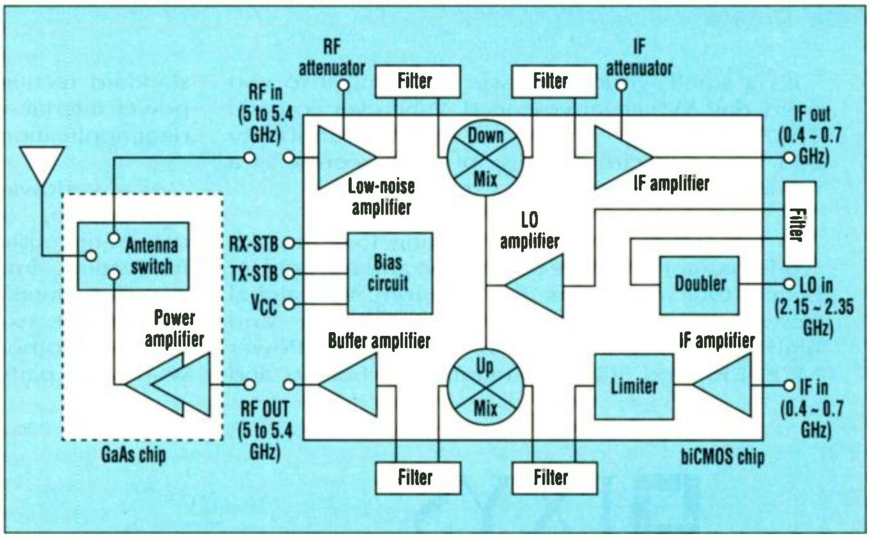
sion rate that's double that of each component ADC. The other pipelined ADC is connected in a calibration loop, where the gain and offset of the selected ADC is adjusted to match those of the reference ADC. After calibration is complete, another ADC replaces it in this "ping-pong" conversion mode. Subsequently, each ADC is periodically calibrated in the background while the other ADCs continue conversion of the input.

Other Developments

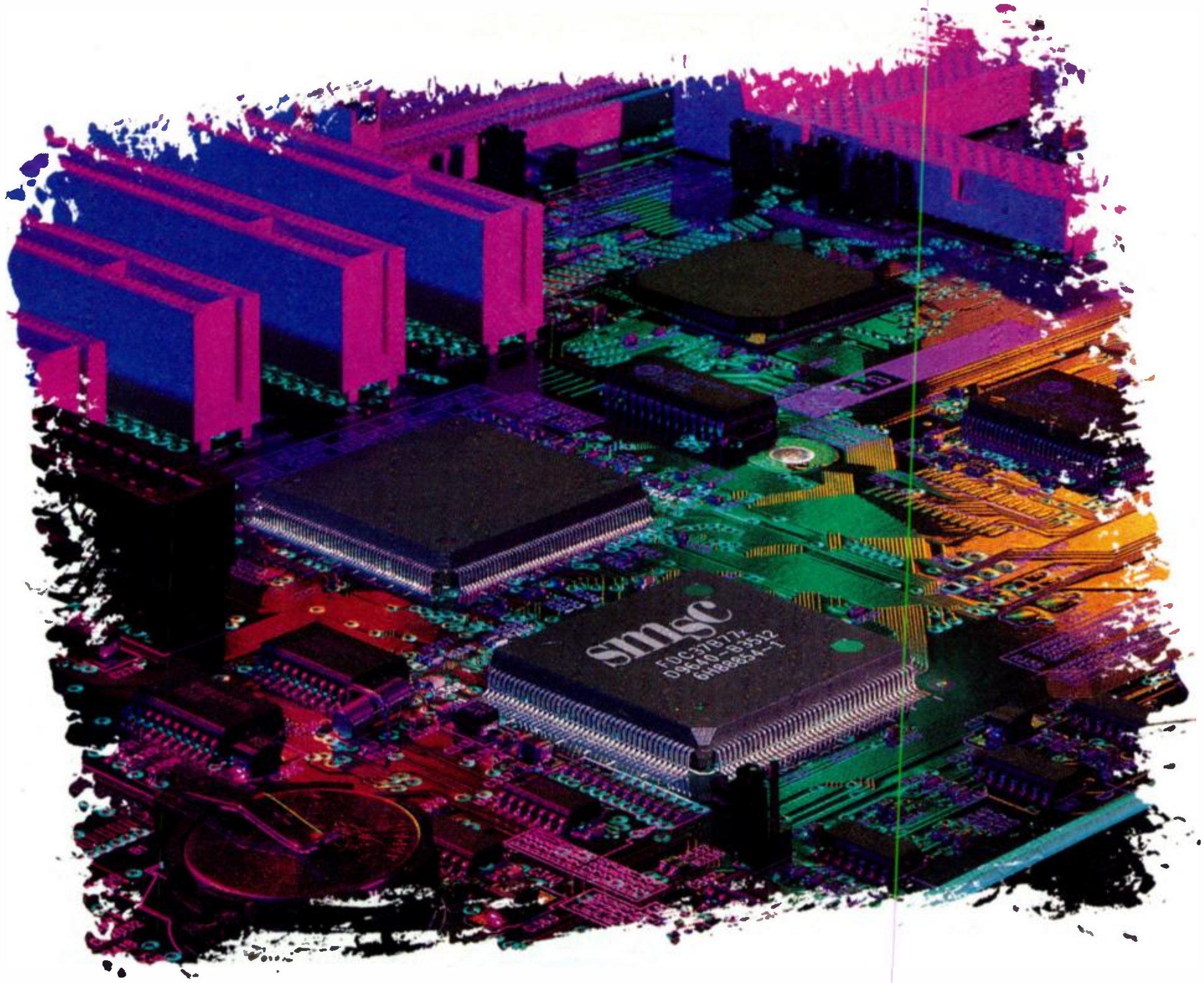
Recently, much attention has been paid to the use of direct-conversion and/or low-IF receivers as potential architectures to make a single-chip receiver. To do this, two technical issues must be overcome: the dc offset created by the self-mixing of the local oscillator signal for direct conversion, and a second-order intermodulation (IM2) for both receivers. The mixer, proposed in paper 23.3, "An I/Q active balanced harmonic mixer with IM2 cancelers and a 45° phase shifter," from Toshiba Corp., Kawasaki, Japan, is one way to overcome these issues. The dc offset change is eliminated by the self-mixing down to its noise level. And, because the device is an even harmonic type, in theory it does not produce problematic second-order distortion. As a result, the active I/Q mixer consisting of a second-order intermodulation canceler and a 45° phase shifter for direct down-conversion has two advantages: a small, self-mixing dc offset due to harmonic mixing; and a small, and frequency insensitive IM2. Also, the 45° phase shifter is low in element sensitivity.

An important building block in any electronic system is an ADC with low voltage and low-power capabilities. A switched op amp technique can be utilized to design switched-capacitor circuits at very-low supply voltage without using multithreshold technologies or voltage multipliers to drive the switches. With this approach though, switches can only be connected to well-chosen reference voltages. A proposed device from the Katholieke Universiteit Leuven in Belgium, provides for another option. Its device, as detailed in paper 4.6, "A 900-mV, 40-µW switched Δ–Σ op amp modulator with 77-dB dynamic range," uses a differential modified switched-op-amp integrator cell, which allows maximum overdrive of the two reference voltages for the switches.

Telescopic cascode op amps have a number of beneficial features including higher frequency and lower power consumption than other topologies. But, they also have a severely limited output swing. A device developed at the Massachusetts Institute of Technology in Cambridge, detailed in paper 20.4, "A ±2.45-V CMOS telescopic op amp," promises to help solve this problem with a much higher output swing than a conventional telescopic amplifier. The device can also maintain high common-mode and power-supply rejection ratios while ensuring constant performance. The op amp is implemented in 0.8-µm CMOS and is on a die of 600 by 630 µm.



2. This diagram shows the schematic for a 5-GHz-band biCMOS up/down converter chip from NEC. When combined with a GaAs power amplifier/antenna switch chip, this device becomes a complete front-end system.



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ISSCC Spotlights Sensor And Multimedia Applications

Advances In Imaging Technology, DSPs, CPUs, And Media Processors Offer A Look At Some Novel Applications.

Cheryl Ajluni

SPECIAL REPORT

At this year's ISSCC, quite a few novel applications have surfaced in the sensors and multimedia arenas. Sensor developments, which are overwhelmingly based on CMOS processes, range from active pixel and imaging sensors to giant magnetoresistive (GMR) sensors and detectors.

One development, which may serve as an alternative to CCDs used in cameras, is a single-chip CMOS NTSC video camera from VLSI Vision Ltd., Edinburgh, Scotland. As detailed in paper 11.2, "A single-chip, 306-by-244-pixel CMOS NTSC video camera," the device incorporates an image sensor array, sensor readout logic, ADCs and DACs, and a custom 300-MIPS processor for color reconstruction and NTSC encoding. Powered by a single 5-V supply and a 14.32-MHz crystal clock, it integrates approximately 580,000 devices on a 68-mm^2 die. The chip is implemented in a 0.8-µm single-polysilicon, double-metal CMOS process, and is coated with an RGB dye set (Bayer pattern).

At the heart of the NTSC video camera is a sensing device comprising an array of 306 by 244 photosensitive elements, each with a three-transistor active pixel. It is based on a standard CMOS n^+/p-well photodiode, voltage references and analog signal buffers. The digital part of the chip consists of a color reconstruction processor and an NTSC encoder. During exposure, the pixel's photocharge is read row-sequentially into a column structure. Using correlated doubling sampling techniques in conjunction with the read sequence, the systematic offset of each pixel is removed. The row of corrected values is then read through a programmable gain amplifier to a sample/hold stage that drives an onboard 8-bit half-flash subranging analog-to-digital converter (ADC). The resulting digital video stream is sent to the color processing engine where an NTSC encoded data stream is output for conversion to analog. This conversion takes place via a current-steering digital-to-analog converter (DAC) driving IV composite video into a 37.5-Ω load. All field exposures are timed to comply with 525-line, 29.97-Hz NTSC frame timing.

As active pixel sensor (APS) technology grows in popularity as a low-cost imaging option, much research is dedicated to new APS-based applications. One such application, a CMOS APS for an automotive stereo vision system, comes from the combined efforts of the Massachusetts Institute of Technology in Cambridge, Polaroid Corp., Cambridge, Mass., and National Semiconductor Corp., Santa Clara, Calif. The work is related in paper 11.5, "A 256-by-256 CMOS imaging array with wide-dynamic-range pixels and column-parallel digital output." The chip also contains 128 output circuits and associated test circuitry. Each output circuit comprises two bias current sources, two correlated double-sampling circuits, and one cyclic ADC that handles two columns and produces digital output at 30 to 390 frames/s.

The column-parallel double-sampling circuitry and the ADC enable frame rates of greater than 10 times the standard video rate. An eight-to-one digital multiplexer accepts outputs from four adjacent output circuits, and produces a single output, which is buffered and sent to a pin.

A key feature of the CMOS APS is its wide dynamic range. In an automobile, illumination has the potential to vary over a large range. To address this problem, a special clocking scheme for the lateral overflow gate is used to provide a dynamic range increase of 20×. Such a feature provides user adjustability, the ability to approximate any compression function, and digital control. As a result, it requires no fill-factor reduction or off-chip processing.

A micropower interface circuit for fluidic flow measurement in commercial gas meters is the result of a joint effort by Integrated Sensor Solutions, San Jose, Calif., and Nagano Keike Co., Ltd., Nagano, Japan. Detailed in paper 17.4, "A 16-µA interface circuit for a capacitive flow sensor," it was developed for a proposed national telemetered network, and is optimized to allow 10 years of continuous service for commercial gas meters without maintenance. This mixed-signal ASIC is composed of two main parts: a fluidic oscillation element and a differential capacitive pressure sensor. Operating within the range of 2.5 to 3.6 V and from -10° to +65° C with an active I_{DD} of 16 µA, the signal path is a first-order Δ–Σ

modulator followed by a three-pole, one-zero inverse impulse-response band-pass filter. The ASIC is implemented on a double-metal, double-polysilicon 1.5-μm CMOS process with EEPROMs.

It works by converting dynamic capacitive sensor readings from 1 to 150 Hz into digital pulses. The mechanism for measuring the flow is a chevron-shaped wall piece placed in a fluid vessel. Depending on the flow passage, the flow changes periodically—blocking itself from one side and forcing flow direction to the other side. When this occurs, the change generates fluidic oscillation, which is proportional to the fluid flow rate. Two holes in the vessel transmit differential pressure to a capacitive pressure sensor. The ASIC converts the capacitive signal to a digital pulse train and filters out all nonideal components related to the mechanical structure. The pulse train is then counted by a micropower host processor. The result, a measurement of gas consumption, can be made available over telephone lines for billing purposes.

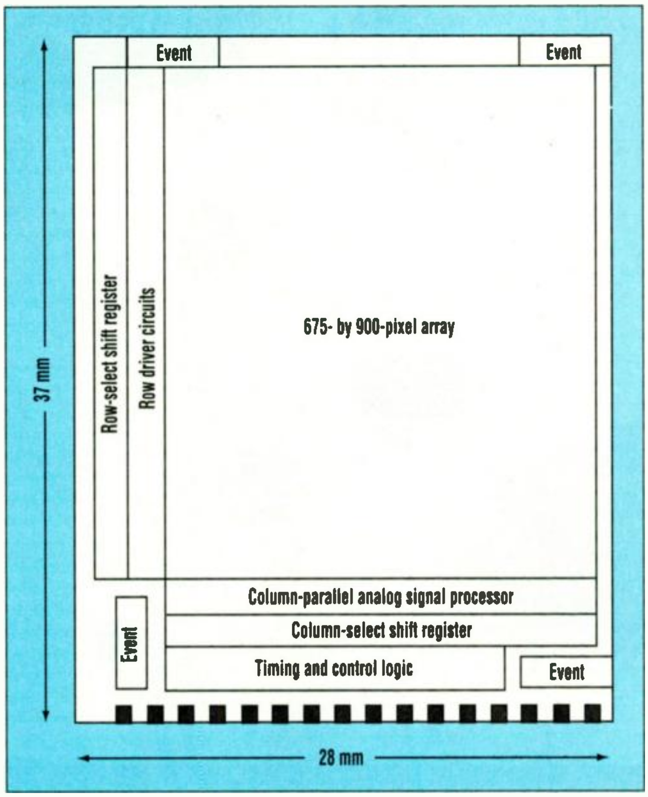
In a number of applications, such as a medical device that electrically contacts the human body circuits which employ multiple or distantly placed grounds, there's a requirement to have the devices electrically isolated. Isolation of these circuits often takes place via some form of complex or hybrid packaging with either optoisolators or rate-sensitive isolation elements such as capacitors or transformers. All of these have associated drawbacks. A novel technique for overcoming these drawbacks comes from Iowa State University in Ames and Nonvolatile Electronics Inc., Eden Prarie, Minn. It is detailed in paper 17.5, "Monolithic 4-20-mA isolating current replicator using GMR resistors." The technique calls for the addition of a few thin-film and insulator-deposition steps to a standard IC process. This method enables multiple isolated inputs on an otherwise conventional bipolar or CMOS process, and is very low in cost.

An isolated current replicator, used as an isolated receiver of 4-20 mA transducer data, was chosen for this technique because its output current closely matches the one present in an isolated input current. The device uses four magnetic-field-sensitive resistors in a bridge configuration, in conjunction with two on-chip current loops and a conventional bipolar op amp. The resistive sensors employ GMR material, which allows the sensors to display a high magnetic sensitivity. It's also easily incorporated into a conventional IC process. A current-carrying wire placed over the resistors provides the magnetic field. Two current loops are connected diagonally across resistors on opposite corners of the bridge. Any difference between them is reflected as a net bridge imbalance, and sent to the amplifier. An isolated and unknown current to be sensed is contained in one of the input loops. The other contains a counterbalancing feedback current from the on-chip amplifier, which balances the bridge by providing a feedback current equal to the one present in the isolated current-input line.

One of the more novel sensor applications at this year's ISSCC is a dental X-ray camera, developed by Photobit Corp., La Crescenta, Calif., and Schick Technologies, Long Island City, N.Y. Who among us has not dreaded having an X-ray taken at the dentist's office? Luckily, this new technology may finally make the process a little less awkward and uncomfortable. What they devised is a 675 (H) by 900 (V) photogate-type CMOS active p-channel APS camera-on-a-chip *(Fig. 1)*. As detailed in paper 11.3, "A large (37 by 28 mm) 600-kpixel CMOS APS dental X-ray camera-on-a-chip with self-triggered readout," it is implemented in a 1-μm single-polysilicon double-metal n-well process with a linear capacitor option. Measuring just 37 by 28 mm with a 40-μm pixel pitch, the device is placed in a patient's mouth for dental X-ray applications. These applications are possible through a combination of on-chip timing and control logic, fixed-pattern noise-suppression circuits, and an event-detection circuit for self-triggered readout.

For simplified packaging, the APS is coated with a scintillator and encapsulated in plastic. Its pads are all located on one side of the chip. Due to the use of a photogate pixel, with its p-channel implementation and well plug, the collection of direct X-ray-generated signal charges in the chip's substrate (the scintillator) is reduced. The chip is designed to have four event detectors. Each detector consists of a photodiode; source-follower; and a cross-coupled, strobed comparator, located at the four corners of the sensor to detect the onset of X-ray irradiation. This technique puts the sensor in the integration mode so that the remainder of the signal can be captured.

The sensor nominally operates in a stand-by mode, with all pixels held in reset. When an Arm signal reaches the sensor, the sampling of the event detectors is enabled. When X-ray irradiation is picked up by the event detector, all pixels are placed in the normal integration mode. Once integration finishes, the chip begins the readout sequence. When all rows are readout, the chip



1. The figure shows a block diagram of the dental CMOS active-pixel sensor developed by Photobit Corp. and Schick Technologies. This camera-on-a-chip consists of 675 (horizontal) by 900 (vertical) photogates. It allows fast and easy dental X-rays. Testing of this device has produced good results, and it is now in production for commercial use.

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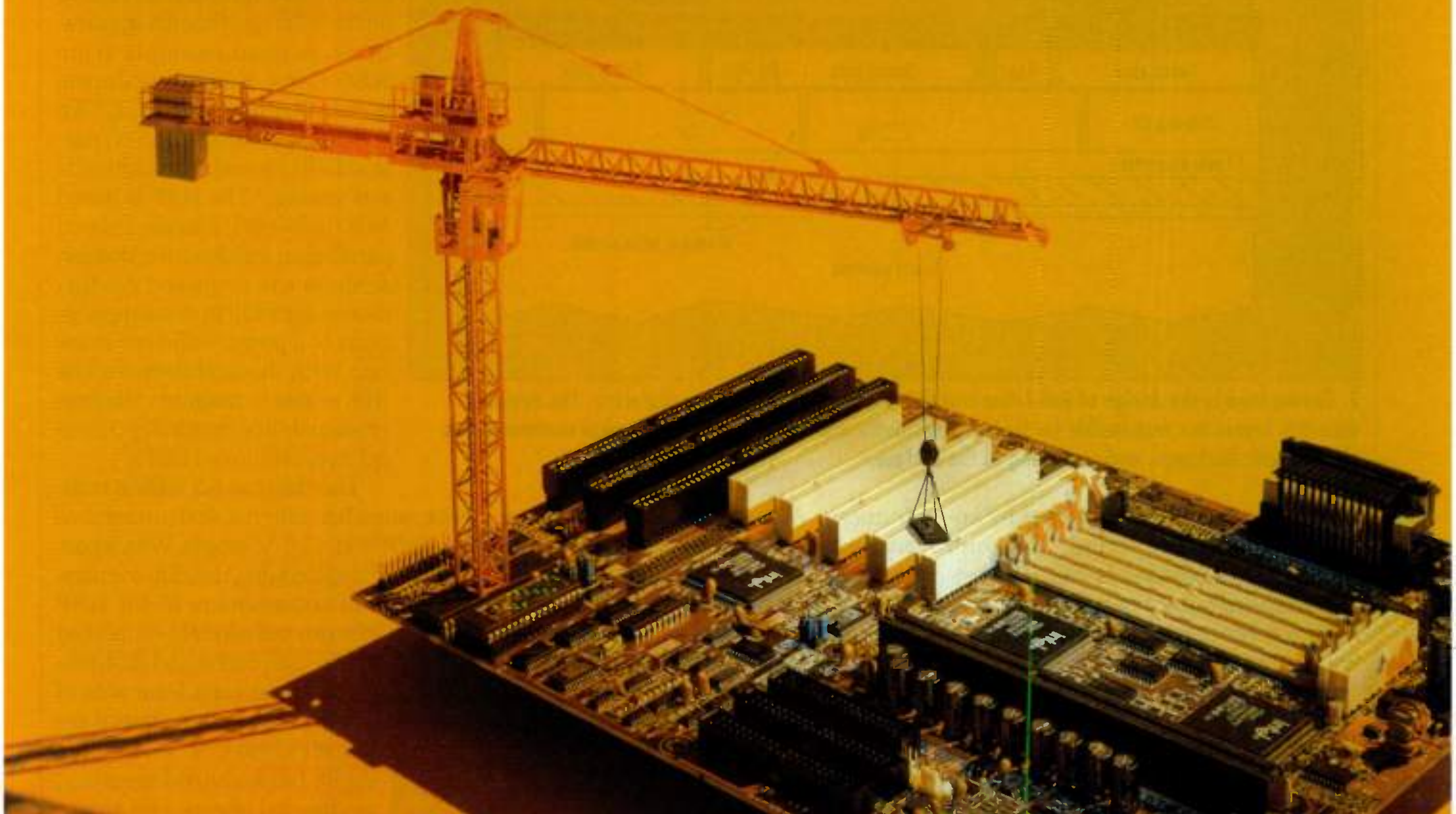

APPLICATIONS/TARGET PROCESSORS

	Pentium™ Class	Pentium™ Pro Class	Pentium™ II Class	General Purpose Embedded
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HIP6004			X	
HIP6004A			X	
HIP6006	X			X
HIP6012	X			X
HIP6014*			X	
Standard Buck				
HIP6003	X	X		
HIP6005			X	
HIP6005A			X	
HIP6007	X			X
HIP6008	X	X		
HIP6011	X			X
HIP6013	X			X
HIP6015*			X	

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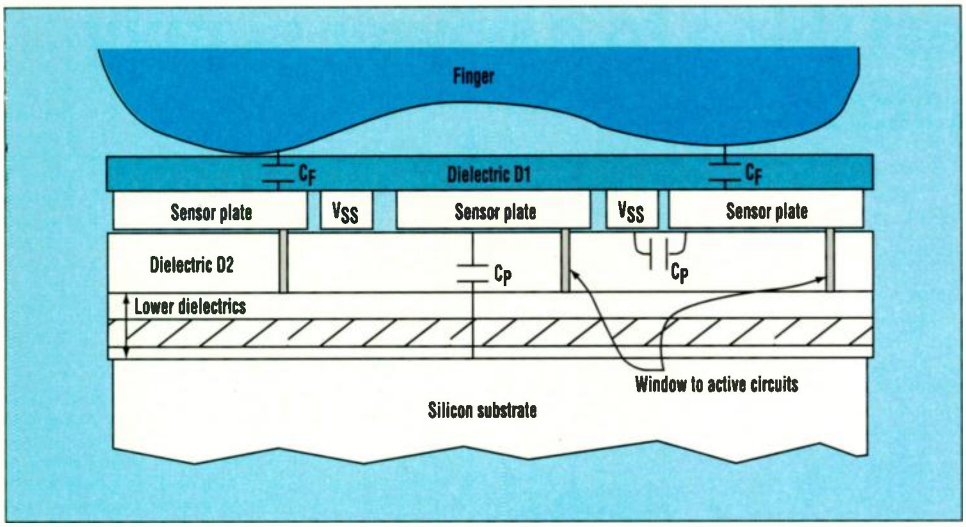
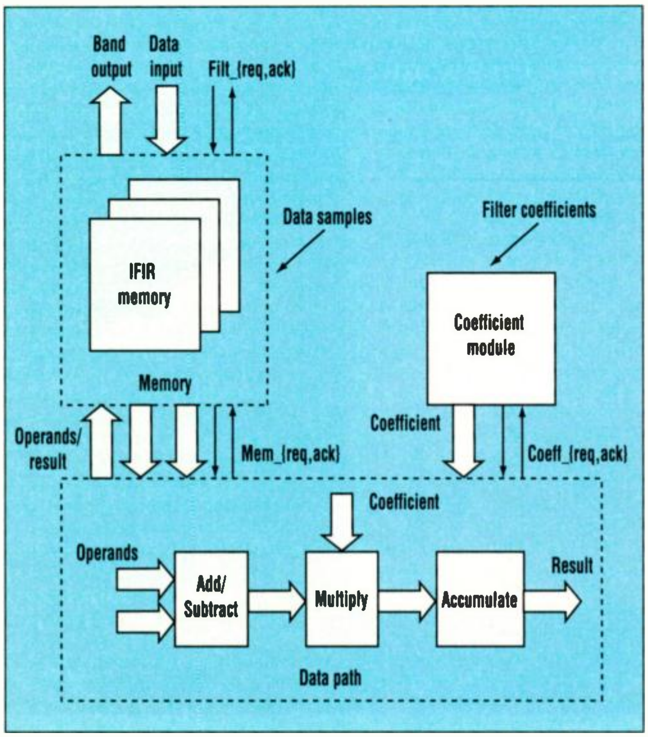


2. Shown here is the design of Bell Laboratories' fingerprint touch sensor dielectric. The device's dielectric layers are responsible for its high sensitivity and its resistance to chemical contamination, electrostatic discharge, and scratching of the surface.

goes into global reset, followed by another integration period. A second readout sequence then begins. The second frame of output data represents a dark reference frame that can be subtracted from the first frame. The chip finally returns to the standby mode.

Another interesting development comes from researchers at Bell Laboratories, Holmdel, N.J. Their sensor is highlighted in paper 17.7, "A robust, 1.8-V, 250-µW direct-contact 500-dpi fingerprint sensor." It provides reliable user authentication. The sensor's standard CMOS front-end processing maintains an effective barrier to chemical, physical and electrostatic intrusion.

The sensor comprises an array of 300 by 300 elements, each 50 by 50 µm, and is implemented in a single digital 0.5-µm, three-metal CMOS process *(Fig. 2)*. Its 272-mm^2 die dissipates less than 110 µW at 1.8 V standby, when no finger is touching the chip, and less than 250 µW at 60 frames/s during acquisition when a finger is present. This number can be reduced considerably by lowering the imaging frame rate. By comparison, commercial optical systems dissipate 2 to 3 W, while previous capacitive sensors dissipate 600 µW at 10 frames/s. An external 1-µA reference current is used to bias the sensor current sources. A row/column hierarchy of current mirrors is employed to distribute this current reference. It also improves tolerance to isolated manufacturing faults. The sensor requires only 1 µs of integration time. Row readout can be completed in 50 µs.



3. This filter-bank architecture for a digital hearing aid was developed by the Danish company Oticon and the Technical University of Denmark. This development successfully demonstrates that asynchronous circuit techniques can result in significant power-consumption reduction in signal-processing applications.

Multimedia And More

Many developments at the ISSCC also included advanced devices for multimedia applications. A good example from NEC Corp., Kanagawa, Japan, is detailed in paper 18.3, "An 800-MOPS, 110-mW, 1.5-V, parallel DSP for mobile multimedia processing." The DSP is based on a task-level, coarse-grained parallelism architecture, and can achieve the required performance for multimedia applications in a power-efficient manner. With this architecture, the chip is able to maintain the programmability capability inherent in conventional DSPs.

The chip has 5.2 million transistors on a 9.2-mm^2 die, and can achieve 800 MOPS at a 1.5-V supply. With a parallel DSP architecture, the chip contains four sets of autonomous 16-bit DSP cores. Each core has a locally-connected 64-kbit instruction cache and 32-kbits each of X/Y data memory. Four sets of data buses connect on-chip shared resources, such as a 128-kbit eight-bank shared memory, peripheral blocks, and an external data memory controller for each of the DSP cores.

Researchers from Digital Equipment Corp., Palo Alto, Calif., have developed a chip for microprocessor applications that encompass 2D and 3D graphics, high-resolution audio/video playback, videoconferencing, soft modems, echo cancellation, and other DSP applications. As detailed in paper 18.6, "A low-cost 30- MHz RISC CPU with attached media processor," the chip includes 3.3 million transistors and measures 60 mm^2. During operation, it dissipates less than 3 W at 300 MHz at a 2.0-V internal and 3.3-V I/O supply. The chip also has 333 separately conditioned clocks, and supports dynamic clock frequency switching for reduced operating power during low-performance demands. For battery- powered applications, the drive voltage (V_{DD}) can be

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reduced for less than 0.5 W operation at 150 MHz. The chip is pseudostatic and supports clock stop and I_{DDQ} testing.

The chip is based on the StrongARM 110 CPU, and is capable of more than two billion 16-bit operations/s. It's integrated with an attached media processor (AMP), a synchronous DRAM controller, and a separate I/O bus. The high performance comes from several enhancements to the StrongARM CPU and cache subsystem. The resulting chip offers performance high enough to support software-based MPEG-2 video and audio while using less than 40% of available processing resources.

Researchers from MIT have developed a novel encryption processor to evaluate an application's requirements while minimizing energy consumption. The processor, discussed in paper 7.2, "A 1-Mbit/s energy/security-scaleable encryption processor using adaptive width and supply," is based on a quadratic residue generator that works by performing repeated modular squarings. The result is a device that allows the level of quality and energy consumed to encrypt a bit, to be traded off dynamically, based on demand. Because transmitted data streams can often be partitioned into different priority levels, an energy-scaleable processor ensures that important information is adequately protected, while sacrificing some security (i.e. quality) for low-priority data to reduce total system energy.

Paper 2.4, "A 60-µW MPEG-4 video codec using clustered voltage scaling with variable supply voltage scheme," from Toshiba Corp., Kawasaki, Japan, claims that the codec is the first to implement essential functions in the MPEG-4 verification model Version 7. The device consumes 60 mW at 30 MHz—only 30% of the power dissipation of conventional CMOS designs. Low-power techniques in both circuit and architectural designs reduces power by 70%. Conditional clocking is also used and results in an average savings of 75% of the power dissipation of a clock system. This equates to 40% of total power dissipation.

A micropower voice-telephone decoder for portable button-battery applications comes from SGS Microelectronics and the University Of Bologna, both in Italy. Detailed in paper 7.3, "A 1-V, 350-µW voice-controlled H.263 video decoder for portable applications," it comprises three low-power logical units: a speech recognizer, a programmable system controller, and an H.263 decoder. An asynchronous peripheral bus connected to the system controller enables the system to be easily expanded, and is responsible for synchronization and different speed compensation.

During operation, system controller opcodes allow the start of the word acquisition and processing by the speech recognizer. The speech-recognition block performs isolated-word recognition upon which commands are issued by the system controller to control the behavior of the peripherals connected to the asynchronous peripheral bus. The controller can handle up to 16 peripheral units, one of which is an external standard alphanumeric LCD that gives the user access to textual output. It also provides a signal to shut down bus interfaces to conserve energy during long periods of inactivity. Connection between each peripheral unit and the controller is via a four-phase handshake. The chip integrates 650 k transistors in a 36-mm^2 area, and is made on a CMOS 0.35-µm, five-metal process.

Another interesting invention comes from researchers at Oticon, Hellerup, Denmark, and Technical University of Denmark in Lyngby. It's highlighted in paper 7.1, "An 85-µW asynchronous filter bank for a digital hearing aid." This asynchronous reimplementation of a seven-band interpolated FIR filter bank is part of Oticon's DigiFocus digital hearing aid *(Fig. 3)*. The circuit consumes less thar five times the amount of power of existing asynchronous designs such that, when processing typical data for less than 50 dB of sound pressure, power consumption is 85 µW. In addition, a filter-bank algorithm was developed to make this implementation architecture simple and power-efficient.

The filter bank is comprised of a tree consisting of complementary interpolated FIR filters and has seven frequency bands at the tree's leaves. With a minimal throughput requirement, the entire computation can be mapped onto a single add-multiply-accumulate data path. A control unit generates the address sequences for the memories and control signals for the datapath. The processing of one input sample requires a sequence of approximately 30 add-multiply-accumulate operations, corresponding to approximately 500,000 add-multiply- accumulate operations/s.

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IEEE International Conference on Acoustics, Speech & Signal Processing (ICASSP '98), May 12-15. Seattle Convention Center, Seattle, Washington. Contact Les E. Atlas, Dept. EE (FT 10), University of Washington, Seattle, Washington 98195; (206) 685-1315; fax (206) 543-3842; e-mail: atlas@ee.washington.edu.

IEEE International Conference on Robotics and Automation, May 16-21. Katholieki Universiteit, Leuven, Belgium. Contact Georges Giralt, LAAS-CNRS, Toulouse, France, +33 61-33-63-48; fax +33 61-33-64-55; e-mail: giralt@laas.fr.

IEEE Power Electronics, Specialist Conference (PESC '98), May 17-22. Sea Hawk Hotel & Resort, Fukuoka, Japan. Contact Tsutomu Ogata, NTT Integrated Information & Energy Systems Labs., Midori-cho, Musashino, 180 Japan; +81 422-59-2350; fax +81 422-59-2347; e-mail: ogata@ilab.ntt.jp

IEEE Vehicular Technology Conference (VTC), May 18-21. Westin Hotel, Ottawa, Ontario, Canada. Contact Tara Hennessy, Industry Canada, 300 Slater St., Ottawa, Ontario, K1A 0C8, Canada; (613) 990-4711; fax (613) 952-5108; e-mail: hennessytara@ic.gc.ca.

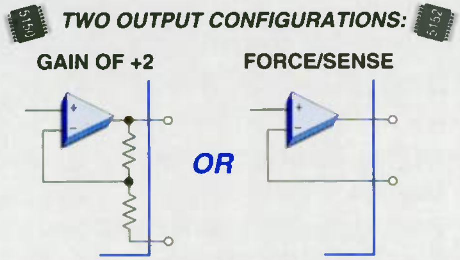
48th IEEE Electronic Components & Technology Conference (ECTC '98), May 25-28. Sheraton Hotel and Towers, Seattle, Washington. Contact Components Group, EIA, 2500 Wilson Boulevard, Arlington, Virginia 22201; (703) 907-7536; fax (703) 907-7501; e-mail: judya@eia.org.

Innovative DACs

FUTURE PRODUCTS

World's First 13-Bit VOUT Dual DAC Fits in the Space of an SO-8!

Highest Functionality and Lowest Power in Smallest Available Package



- **Two 13-Bit Dual VOUT DACs**
- **+2.7V or +5V Single-Supply Operation**
- **Separate Reference Voltage Inputs for Each DAC**
- **Draws Only 250µA/DAC**
- **3-Wire SPI™/QSPI™/Microwire™-Compatible Serial Interface**
- **Individual DAC Power-Down Control**

Maxim Offers Both 13-Bit and 12-Bit Versions

PART	RESOLUTION (BITS)	SUPPLY VOLTAGE (V)	OUTPUT CONFIGURATION
MAX5150*	13	5	Gain of +2
MAX5151*	13	2.7 to 3.6	Gain of +2
MAX5152**	13	5	Force/Sense
MAX5153**	13	2.7 to 3.6	Force/Sense

PART	RESOLUTION (BITS)	SUPPLY VOLTAGE (V)	OUTPUT CONFIGURATION
MAX5154**	12	5	Gain of +2
MAX5155**	12	2.7 to 3.6	Gain of +2
MAX5156**	12	5	Force/Sense
MAX5157**	12	2.7 to 3.6	Force/Sense

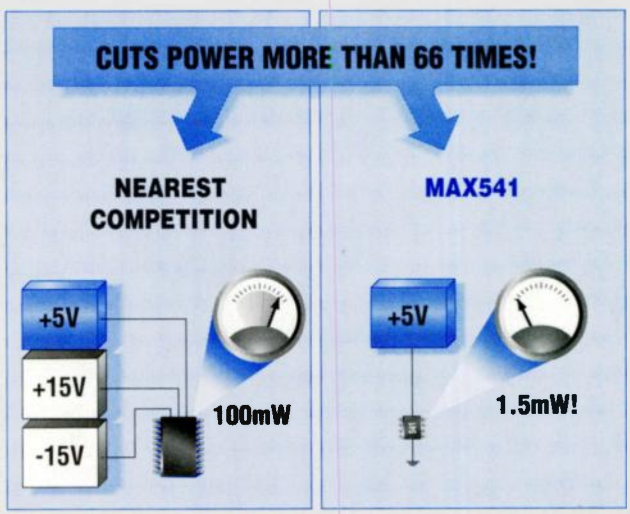
*Future product—available after July 1997
**Future product—available after August 1997

First 16-Bit VOUT DAC in an 8-Pin SO!

Ideal for industrial and instrumentation applications, the single +5V supply MAX541 DAC features low power, 16-bit accuracy with no adjustments, Schmitt trigger inputs for direct optocoupler interfacing, a 3-wire serial interface, and power-on reset. The 14-pin MAX542 has Kelvin sense connections for simplified layout requirements, and internal feedback resistors for bipolar operation (with an external op amp). For 14-bit applications, request the pin-compatible MAX544/MAX545.

- **High Accuracy:**
  ≤ ±1LSB (max) INL
  ≤ ±1LSB (max) DNL
- **Small Package: 8-Pin DIP/SO**
- **Low Power:**
  Single +5V Supply
  0.3mA Supply Current
- **High Resolution: 38µV per LSB**

SPI and QSPI are trademarks of Motorola, Inc.
Microwire is a trademark of National Semiconductor Corp.



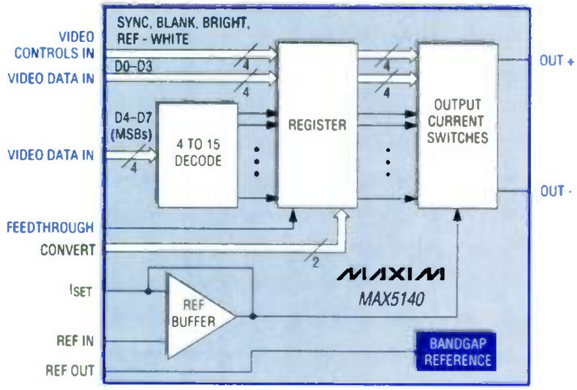
PART	RESOLUTION (BITS)	INL (LSB)	PACKAGE	FORCE/SENSE CONNECTIONS
MAX541	16	1, 2, or 4	8-pin DIP/SO	—
MAX542	16	1, 2, or 4	14-pin DIP/SO	Yes
MAX544	14	0.5 or 1	8-pin DIP/SO	—
MAX545	14	0.5 or 1	14-pin DIP/SO	Yes

MAXIM

NEW World's Fastest Complete 8-Bit Video DACs

Drive Ultra-High-Resolution Color Displays at 90Hz Update Rates!

The MAX5140 (400MHz) and MAX5018 (275MHz) allow the high, flicker-free screen refresh rates necessary in critical 8-bit color applications. They provide outstanding performance in EVGA and super-high-resolution (2,048 x 2,048) monitors and workstations. The MAX5140's high-accuracy on-board bandgap reference can be used to drive two other MAX5140s in RGB applications.



- **High-Speed ECL Video Inputs**
- **Feedthrough Control Allows Flexible Operation**
- **Complete Video Controls are Built-In**
- **Differential Current Outputs Can Drive 50Ω or 75Ω Cable**
- **Internal Precision Bandgap Reference**

- **Fastest!**
  - **The new MAX5018 (275MHz) and MAX5140 (400MHz) are the fastest video DACs available**
- **Best Features!**
  - **Complete video controls built-in: sync, blank, bright, and reference white**
  - **Stable (100ppm) bandgap reference for accurate color**
  - **Operate from a single -5.2V supply**
- **Best Performance!**
  - **Low, 4pV-s glitch energy ensures color purity**
  - **Fast, 600ps output rise time**

Ultra-Fast Monolithic 12-Bit

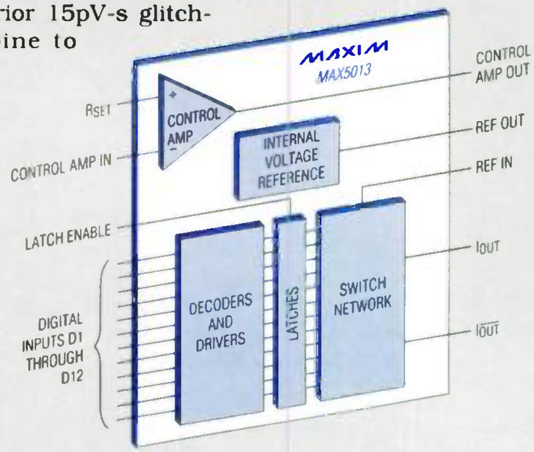
Maxim's MAX555 12-bit DAC delivers precise dynamic performance, exceptional signal purity, and low glitch energy at ultra-high update rates (to 300Msps). With 72dB spurious-free dynamic range (SFDR), the MAX555 improves dynamic range in RF and DDS applications. The complementary 50Ω outputs and low 15pF output capacitance directly drive a 50Ω transmission line and simplify output filtering.

Evaluation Kit Speeds Prototyping and Design
Order MAX555EVKIT

NEW World's Best, Low-Cost 12-Bit High-Speed DACs

Deliver Premium Performance in Signal Synthesis Applications

The new MAX5012 and MAX5013 12-bit, 100MHz DACs are the cost-effective choice for applications in imaging, direct digital synthesis, and waveform generation where accuracy and performance are essential. These devices are pin-compatible with the AD9712/13, with significantly improved AC performance. Superior 15pV-s glitch-energy level and fast 13ns settling time combine to produce excellent SFDR of 72dB at 20MHz (with 5.01MHz update rate). Choose the MAX5013 with standard TTL outputs, or the MAX5012 for ECL interfaces. Both are available in two performance grades and packaged in a space-saving 28-pin PLCC package.



Highest Performance:

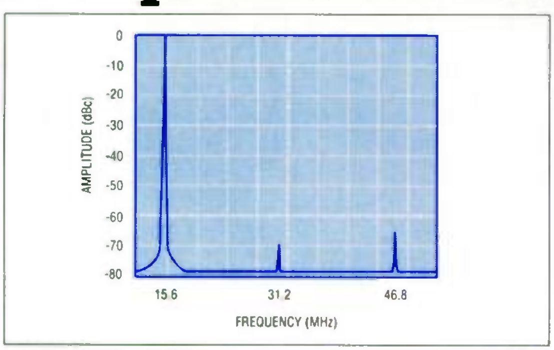
- **1/2 LSB DNL**
- **Lowest Glitch Energy**
- **Fast 13ns Settling Time on Differential Outputs**
- **Low-Power Operation—640mW**

Best Features:

- **Internal Bandgap Reference (50ppm Stability)**
- **40MHz Multiplying Bandwidth**
- **On-Board Master/Slave Latches Minimize Output Glitch Energy**
- **Single -5.2V Supply (MAX5012)**

PARAMETER	MAXIM	COMPETITION	BENEFIT
Glitch Energy	15pV-s	28pV-s	Low SFDR/THD
Settling Time	13ns	27ns	Low SFDR
Internal Data Latches	Master/Slave	Transparent	Improved AC performance
Power	640mW	725mW	Less drain from power supply

DAC Updates at 300Msps



SFDR is 64dB at 250Msps (f_{OUT} = 15.6MHz), improving to 72dB at 50Msps (f_{OUT} = 3.1MHz).

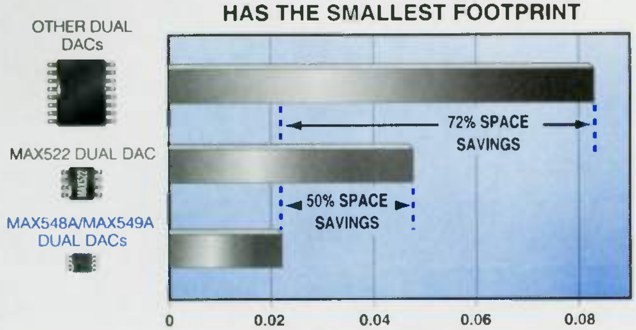
- **SFDR of 72dB at 50Msps, 64dB at 250Msps**
- **Complementary 50Ω Outputs**
- **10MHz Reference-Input Multiplying Bandwidth**
- **Single -5.2V Supply**
- **ECL-Compatible Logic Inputs**

μMAX DACs: World's

NEW World's Smallest, Lowest Power 8-Bit DACs Operate Down to +2.5V

The MAX548A/MAX549A/MAX550A are low-power, 8-bit single and dual DACs available in ultra-small 8-pin μMAX packages. They operate from a single +2.5V to +5.5V supply and require only 75μA operating current per DAC (V_{DD} = 2.5V, includes reference current). This combination of ultra-small size and low power makes these devices well suited for portable and other space- or power-constrained digital adjustment applications. The MAX548A/MAX549A/MAX550A are controlled via a 3-wire serial interface that is compatible with SPI™/QSPI™ and Microwire™. Each features a shutdown mode that reduces the supply current below 1μA.

THE MAX548A HAS THE SMALLEST FOOTPRINT



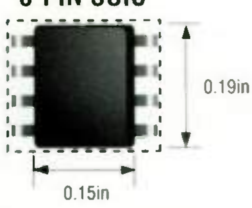
- 8-Pin μMAX or DIP Package
- Single (MAX550A) and Dual (MAX548A/MAX549A) Versions
- Operate from +2.5V to +5.5V
- Consume <0.2mW (MAX550A, V_{DD} = 2.5V)
- 1μA Shutdown Mode
- 3-Wire Serial Interface
- Power-On Reset Clears All DAC Latches

PART	μMAX PACKAGE	REFERENCE	NO. OF DACs	ASYNCHRONOUS LOAD INPUT	DOUBLE-BUFFERED INPUT
MAX548A	✓	$V_{REF} = V_{DD}$	2	✓	✓
MAX549A*	✓	EXT	2	—	✓
MAX550A*	✓	EXT	1	✓	✓

*The MAX549A and MAX550A are double-buffered pin- and software-compatible enhanced versions that directly replace the MAX549B and MAX550B.

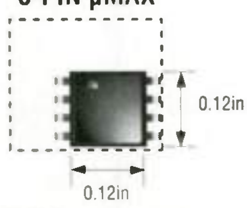
The μMAX Advantage:

8-PIN SOIC



AREA = 0.04in²

8-PIN μMAX



AREA = 0.02in²

μMAX DACs Use **50%** Less Board Space

(ACTUAL SIZE)

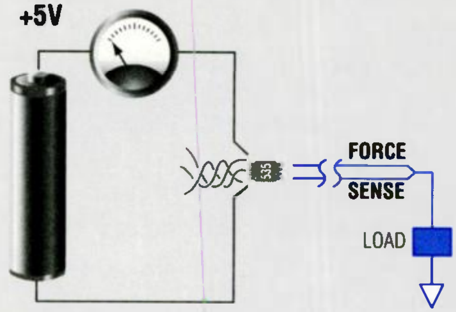
SPI and QSPI are trademarks of Motorola, Inc.
Microwire is a trademark of National Semiconductor Corp.

Smallest DAC Package

World's Smallest, Lowest Power 13-Bit VOUT DAC Has Configurable Output

Can Drive 5kΩ Loads or 4–20mA Loops

- **Single +5V Operation**
- **Low Power Dissipation: 1.5mW**
- **4µA Power-Down Mode**
- **Rail-to-Rail® Output**
- **3-Wire Serial Interface**
- **16µs Settling Time**



The MAX535 is the smallest, lowest power 13-bit voltage-output DAC available. The device operates from a single +5V supply and draws only 300µA of current (excluding the reference current). Several features make it ideal for industrial and instrumentation applications, including a space-saving 8-pin µMAX package, a rail-to-rail output, and a power-on reset function that resets the DAC output to 0V.

PART	RESOLUTION (BITS)	SUPPLY VOLTAGE (V)	8-PIN µMAX
MAX535	13	5	✓
MAX5351	13	3.3	✓
MAX5352	12	5	✓
MAX5353	12	3.3	✓

The user has access to the negative input of the output buffer amplifier, and can configure the output to provide gain (using two external resistors) or to drive 4–20mA loops. The amplifier's output and negative input terminals can also be used as force and sense pins for remote sensing applications.

In power-down mode, the reference input is high-impedance, allowing minimal current consumption even when the external reference remains active. This reduces the supply current to 10µA in power-sensitive high-resolution applications.

Smallest Low-Power 10-Bit DAC Fits in 8-Pin µMAX

Drives 5kΩ Loads or 4–20mA Loops

- **+5V (MAX5354) or +3.3V (MAX5355) Operation**
- **10-Bit Resolution**
- **Low 300µA Supply Current**
- **Pin-Compatible 12-Bit Upgrades: MAX5352/MAX5353 (see table above)**

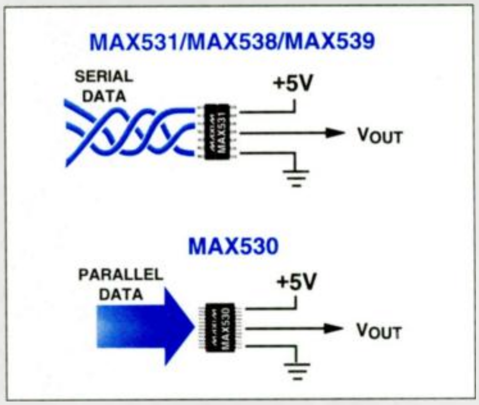
For general-purpose 10-bit applications, the +5V MAX5354 and the +3.3V MAX5355 single voltage-output DACs provide true 10-bit accuracy (±1LSB INL and DNL) while using the least amount of board space—0.02in^2. Features include power-on reset, a 10µs settling time, and a rail-to-rail output swing.

Rail-to-Rail is a registered trademark of Nippon Motorola Ltd

12-Bit "µ-DAC™"s Offer Small Size and Lowest Power

"µ-DAC"s Offer:

- µ-Power:
  - Single +5V and ±5V (MAX530/MAX531) Operation
  - 160µA Supply Current (MAX538/MAX539)
- µ-Size:
  - Complete 1-Chip Solution
  - 8-Pin SO (MAX538/MAX539), 14-Pin SO (MAX531), or 24-Pin SSOP (MAX530)
- Rail-to-Rail Voltage Output
- 4-Quadrant Multiplication
- Internal 2.048V Reference (MAX530/MAX531)

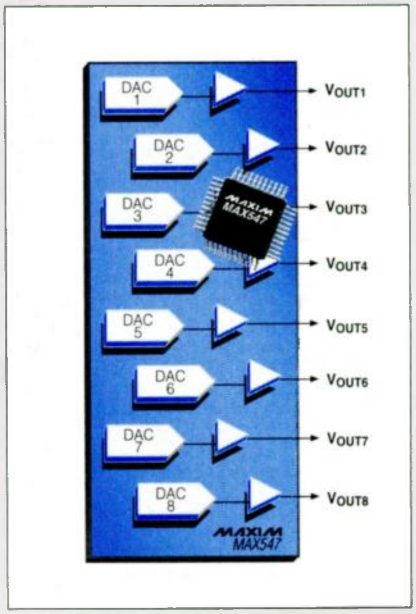


µ-DAC is a trademark of Maxim Integrated Products.

Fit 8 13-Bit DACs and 8 Op Amps in Less than 0.5in²

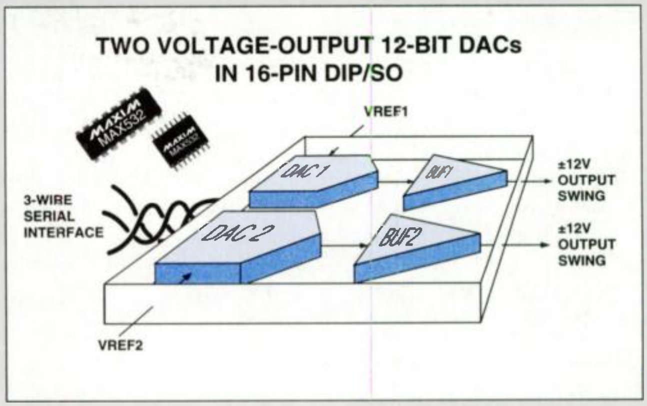
- One IC Replaces 8 Op Amps and 8 DACs
- Guaranteed 13 Bits Monotonic over Temperature
- Unipolar & Bipolar Output Ranges from ±5V Supplies
- Double-Buffered, High-Speed Digital Inputs

Multichannel high-performance solutions are now easier to design, and fit in a smaller space than before—thanks to Maxim's MAX547. Each of the eight independent DACs in the MAX547 can be configured for either a bipolar or unipolar output range, and each guarantees full 13-bit performance without adjustments. Settling to ±½LSB in 5µs, voltage outputs swing ±4.5V with ±5V supplies. All converter outputs are automatically reset to analog ground on power-up by internal reset circuitry. An external command to the asynchronous $\overline{CLR}$ input also resets the outputs. The digital inputs are double-buffered, enabling independent or simultaneous updates via the parallel high-speed microcontroller interface. The MAX547 comes in 44-pin PLCC or plastic flatpack packages, in commercial or extended-industrial temperature ranges.



Dual, Serial VOUT MDAC has ±12V Output Swings

The MAX532 combines two precision, voltage-output 12-bit DACs with a fast 3-wire serial interface and ±10mA output amplifiers. The 6MHz serial interface frees microprocessor pins and minimizes the number of package pins, so the MAX532 uses less board space than parallel-interface parts. This dual multiplying DAC (MDAC) comes in small 16-pin DIP and SO packages. The MAX532 achieves full specified 12-bit performance (±½LSB max integral nonlinearity over temp.) without external trims.



The serial interface minimizes digital-noise feedthrough from the MAX532's logic pins to its analog outputs, and simplifies optocoupler-isolated or transformer-isolated applications. Its interface is SPI™, QSPI™, and Microwire™ compatible. A serial output (DOUT) allows cascading of two or more MAX532s.

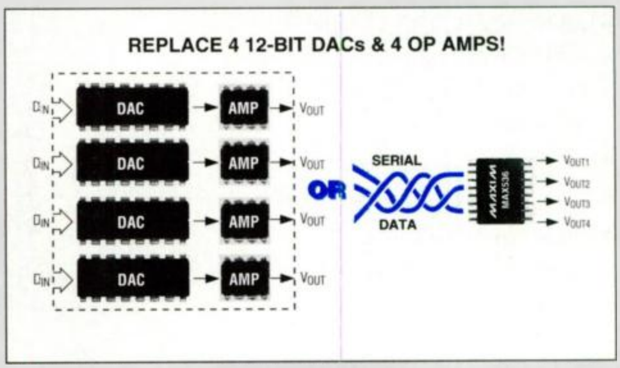
Applications include digital offset/gain adjustment, ATE, machine control, and waveform reconstruction. A and B grades are available.

SPI and QSPI are trademarks of Motorola, Inc.
Microwire is a trademark of National Semiconductor Corp

Quad 12-Bit DACs Are the Fastest, Smallest, and Most Accurate

1LSB TUE and 3µs Settling in a 16-Pin SO

- **Serial (MAX536/MAX537) or Parallel (MAX526/MAX527) Versions**
- **Low Noise (50µVRMS)**
- **Power-On Reset**
- **±5V Operation (MAX527/MAX537)**



10-Bit DACs

First 10-Bit VOUT DACs Draw Only 150µA from a Single +5V Supply!

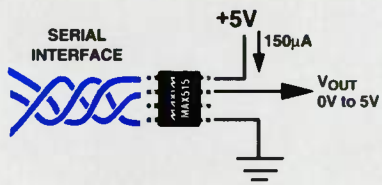
Upgrade Your 8-Bit DAC to 10 Bits—Free!†

With the MAX503/MAX504/MAX515 low-power 10-bit DACs, you can upgrade performance without increasing cost. These devices provide four-times the accuracy of 8-bit devices, yet are aggressively priced to compete with 8-bit solutions. The MAX503/MAX504/MAX515 operate with a single +5V supply and draw as little as 150µA supply current (MAX515). Other features include rail-to-rail voltage outputs, an on-board reference (MAX503/MAX504), serial or parallel interface (see table below), and power-on reset. In addition, pin-compatible 12-bit upgrades are available for applications requiring greater accuracy.

FEATURE	MAX503	MAX504	MAX515
Supply Voltage (V)	+5 or ±5	+5 or ±5	+5
Reference	Internal	Internal	External
Interface	Parallel	Serial	Serial
Package Size	24 SSOP/Narrow DIP	14 SO/DIP	8 SO/DIP
Pin-Compatible 12-Bit Upgrade	MAX530	MAX531	MAX539

† MAX515 priced from $2.50/1000 pc., FOB USA.

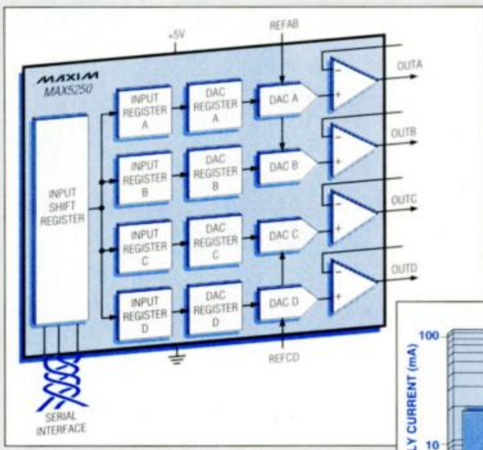
8-PIN SOIC SAVES SPACE!



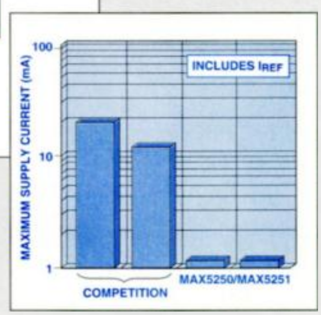
Lowest Power 10-Bit Quad DACs Draw 90% Less Current

New +3V/+5V DACs for Process Control, Instrumentation, and Communications

- **+3V (MAX5251) and +5V (MAX5250) Operation**
- **10-Bit Quad DAC in 20-Pin SSOP**
- **20µs Settling Time**
- **3µA Power-Down Mode**
- **Power-On Reset**
- **Rail-to-Rail Outputs**



20-Pin SSOP



The serial MAX5250/MAX5251 are the lowest power 10-bit quad DACs (MAX5251: 3mW, +3V; MAX5250: 6mW, +5V). They are also the smallest (SSOP-20). These devices have many features that simplify programming and implementation: rail-to-rail outputs, access to the amplifier's negative input for varied output configurations, a programmable logic output, and a data output for daisy-chaining.

World's First 2-Wire 8-Bit DACs Save µP I/O Lines!

The MAX517–MAX521 single +5V, 8-bit DACs feature a 2-wire interface that allows multiple DACs and other devices (including 2-wire EEPROMs) on the same bus. The MAX517/MAX518 are single and dual DACs available in an 8-pin package. The dual MAX519 allows up to 15 additional DACs on the bus. The MAX520 is an ultra-low-power quad DAC, requiring only 4µA supply current, and the MAX521 is an octal DAC in a small 24-pin SSOP package.

- **Simple 2-Wire Interface**
- **Single +5V Supply**
- **Rail-to-Rail Outputs**
- **10µA Shutdown Mode**
- **I²C™ Compatible**

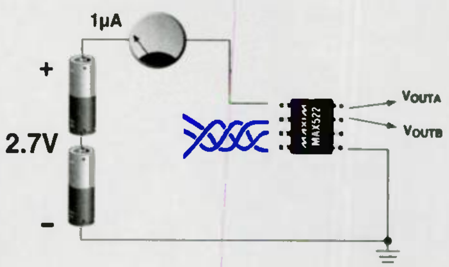
I²C is a trademark of Philips Semiconductors.

DEVICE	NO. OF DACs	NO. OF REFERENCE INPUTS	PACKAGE
MAX521	8	5	20 DIP, 24 SO/SSOP
MAX520	4	4	16 DIP/SO
MAX519	2	2	16 DIP/SO
MAX518	2	0 ($V_{REF} = V_{DD}$)	8 DIP/SO
MAX517	1	1	8 DIP/SO

First +2.7V, 8-Bit V_{OUT} DAC Shuts Down to 1µA

The MAX522 is a low-power, dual, 8-bit voltage-output DAC in a small 8-pin package. Its supply current is less than 1mA (V_{DD} = 3.6V) and it features a 1µA power-down mode.

- **Ideal for Low-Power Applications:**
  - **Digitally Adjustable RF Bias Circuits**
  - **Digital Gain and Offset Corrections**
- **Guaranteed Monotonic Over Temp.**
- **Serial Interface Compatible with Microwire™, SPI™, QSPI™**
- **Guaranteed +2.7V to +5.5V Operation**
- **Triple-Output Versions Available (MAX512/MAX513)**



SPI and QSPI are trademarks of Motorola, Inc.
Microwire is a trademark of National Semiconductor Corp.

+5V Quad DACs Swing Rail-to-Rail

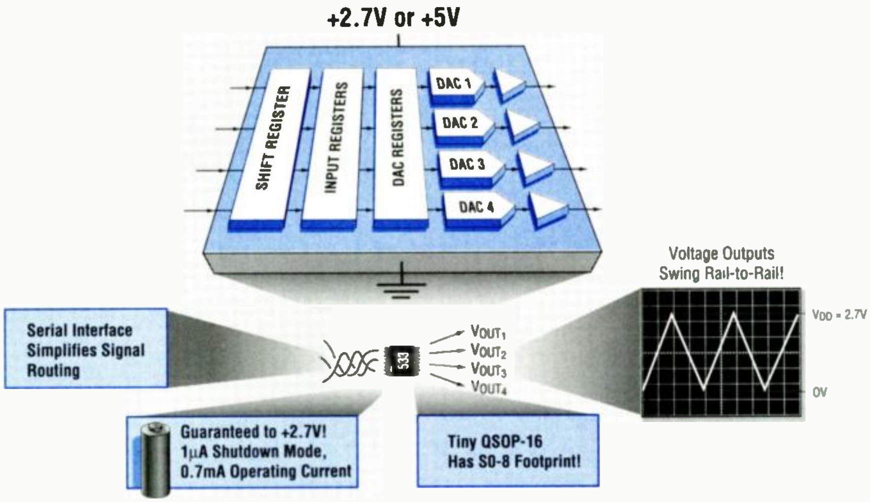
V_{OUT} Range Includes V_{SS} and V_{DD} with +5V or ±5V Supplies

The MAX505/MAX506 8-bit, parallel-interface quad DACs can trim voltages, set thresholds, and attenuate analog signals from a single +5V or dual ±5V supplies. Total unadjusted error is ±1LSB (max) over temperature, with no external components or trims required. Pin and functionally compatible with the industry-standard MX7225/MX7226, these devices have been improved to provide 5V operation with rail-to-rail output swing. The MAX505 contains double-buffered logic inputs, allowing all outputs to be updated simultaneously. Each DAC has a separate rail-to-rail reference input for full flexibility. Available packages include 24-pin SSOP, SO, and DIP. The MAX506 has a single common reference input shared by all four DACs, resulting in fewer package pins (20-pin DIP/SO).

8-Bit DACs

Lowest Power Quad 8-Bit DACs Have SO-8 Footprint!

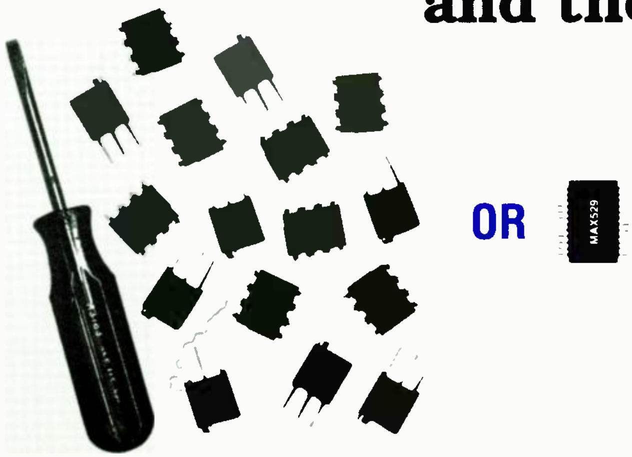
Ideal for Portable and Battery-Powered Applications



- **Smallest Size: 16-Pin QSOP**
- **Lowest Power: 0.5mW per DAC (MAX533)**
- **Asynchronous Load and Clear Inputs**
- **Power-On Reset**

The new MAX533 and MAX534 quad 8-bit DACs with rail-to-rail output buffers are guaranteed to operate from a single +2.7V (MAX533) or +5V (MAX534) supply. They are the smallest, lowest power devices of this type available.

Digitally Trim System Errors while Eliminating 8 Trim Pots, 8 Op Amps... and the Screwdriver!



- **Eight VOUT DACs with Output Buffers**
- **SSOP Uses Only 0.1in² of Space**
- **Only 71¢†/Output**
- **3-Wire Serial Interface**
- **Single +5V Operation (MAX529)**
- **Wide Output Swings (17Vp-p) (MAX528)**

† Based on 1000 pc. price of $5.65, FOB USA.

MAXIM

Single D/A Converters

Part Number	Resolution (Bits)	Output Type*	Settling Time (µs)	Reference**	Data-Bus Interface (Bits)	Supply Voltage (V)	Features	Price† 1000-up ($)
MX7224	8	V	5	Ext	µP/8	+12 to +15 & -5	Single or dual supplies	3.16
MAX517	8	V	6	Ext	Serial, 2-wire	+5	2-wire interface	2.10
MAX550A	8	V	***	Ext	Serial	+2.5 to +5.5	8-pin µMAX, 2.5V, <0.7mW (upgrade to MAX550B)	1.45
MX7523	8	I	0.15	MDAC	Logic	+15	Low-cost 8-bit DAC	2.60
MAX7624	8	I	0.25	MDAC	µP/8	+12 to +15	Improved MX7524	2.26
MX7524	8	I	0.4	MDAC	µP/8	+5 to +15	Low-cost 8-bit DAC	2.52
MAX5354	10	V	10	Ext	Serial	+5	+5V, 10-bit, 8-pin µMAX	2.70
MAX5355	10	V	10	Ext	Serial	+3.3	+3.3V, 10-bit, 8-pin µMAX	2.90
MAX503	10	V	25	Int/MDAC	µP/8	+5 or ±5	Ultra-low power, complete DAC	2.95
MAX504	10	V	25	Int/MDAC	Serial	+5 or ±5	Serial version of MAX503	2.80
MAX515	10	V	25	Ext	Serial	+5	Ultra-low power, 8-pin DIP/SO	2.50
MX7520	10	I	0.5	MDAC	Logic	+15	Low-cost 10-bit DAC	2.80
MX7530	10	I	0.5	MDAC	Logic	+15	Low-cost 10-bit DAC	2.80
MX7533	10	I	0.6	MDAC	Logic	+15	Low-cost 10-bit DAC	2.84
MAX501	12	V	5	MDAC	µP/8	±12 to ±15	4-quadrant multiplying DAC	5.65
MAX502	12	V	5	MDAC	µP/12	±12 to ±15	4-quadrant multiplying DAC	5.65
MAX507	12	V	5	Int	µP/12	±12 to ±15	Complete 12-bit DAC with reference	7.65
MAX508	12	V	5	Int	µP/8	±12 to ±15	Complete 12-bit DAC with reference	7.65
MX7845	12	V	5	MDAC	µP/12	±15	4-range, 4-quadrant multiplying DAC	6.26
MX7245	12	V	10	Int	µP/12	±15 or +12 to +15	Single or dual supplies with reference	8.33
MX7248	12	V	10	Int	µP/8	±15 or +12 to +15	8-bit interface MX7245	8.33
MAX5352	12	V	14	Ext	Serial	+5	+5V, 12-bit, 8-pin µMAX, 1.5mW	4.20
MAX5353	12	V	14	Ext	Serial	+3.3	+3.3V, 12-bit, 8-pin µMAX, 0.9mW	4.20
MAX530	12	V	25	Int/MDAC	µP/8	+5 or ±5	Ultra-low power, flexible output range	5.45
MAX531	12	V	25	Int/MDAC	Serial	+5 or ±5	Serial version of MAX530	5.45
MAX538	12	V	25	Ext	Serial	+5	8-pin DIP/SO, ultra-low power, 0V to 2V output	4.85
MAX539	12	V	25	Ext	Serial	+5	8-pin DIP/SO, ultra-low power, 0V to 5V output	4.85
MX565A	12	I	0.25	Int	Logic	±15	10V buried-zener reference	9.68
MX566A	12	I	0.35	Ext	Logic	-15	No internal reference	9.04
MX7521	12	I	0.5	MDAC	Logic	+15	Low-cost 12-bit DAC	5.00
MX7531	12	I	0.5	MDAC	Logic	+15	Low-cost 12-bit DAC	5.08
MX7541A	12	I	0.6	MDAC	Logic	+15	12-bit data bus	5.72
MAX543	12	I	1	MDAC	Serial	+5 to +15	12-bit multiplying DAC in 8-pin DIP/SO	4.80
MAX551	12	I	1	MDAC	Serial	+5	Smallest I_{OUT} DAC, 10-pin µMAX, CLR pin	††
MAX552	12	I	1	MDAC	Serial	+2.7 to +3.6	Smallest I_{OUT} DAC, 10-pin µMAX, CLR pin	††
MAX7645	12	I	1	MDAC	µP/12	+15	Improved MX7545	5.60
MX7541	12	I	1	MDAC	Logic	+15	12-bit data bus	5.07
MX7545A	12	I	1	MDAC	µP/12	+5 to +15	Improved MX7545	6.03
MX7548	12	I	1	MDAC	µP/8	+5 to +15	8-bit data bus with latches	6.06
MX7542	12	I	2	MDAC	µP/4	+5	4-bit data bus with latches	7.52
MX7543	12	I	2	MDAC	Seria	+5	12-bit multiplying DAC	7.52
MX7545	12	I	2	MDAC	µP/12	+5 to +15	12-bit data bus with latches	5.00
MAX535	13	V	20	Ext	Serial	+5	+5V, 13-bit, 8-pin µMAX, 1.5mW	4.95
MAX5351	13	V	20	Ext	Serial	+3.3	+3.3V, 13-bit, 8-pin µMAX, 0.9mW	5.50
MAX544	14	V	***	Ext	Serial	+5	5V, 14-bit, low power, 8-pin SO	7.90
MAX545	14	V	***	Ext	Serial	+5	5V, unipolar or bipolar, low power, 14-pin DIP/SO	7.90
MX7534	14	I	1.5	MDAC	µP/8	+12 to +15	Double-buffered inputs	13.37
MX7535	14	I	1.5	MDAC	µP/8 or 14	+12 to +15	Double-buffered inputs	15.00
MX7536	14	I	1.5	MDAC	µP/8 or 14	+12 to +15	No external resistors needed	14.66
MX7538	14	I	1.5	MDAC	µP/14	+12 to +15	Low-cost 14-bit DAC	8.88
MAX541	16	V	***	Ext	Serial	+5	5V, 16-bit, low power, 8-pin DIP/SO	9.95
MAX542	16	V	***	Ext	Serial	+5	5V, 16-bit, unipolar or bipolar, low power, 14-pin DIP/SO	9.95

* V = voltage, I = current
** MDAC = 4-quadrant multiplying capability, Int = internal reference, Ext = external reference
*** Settling time depends on internal resistive ladder and external load impedance.

† Prices provided are for design guidance and are for the lowest grade commercial temperature parts (FOB USA). International prices will differ due to local duties, taxes, and exchange rates.
†† Future product—contact factory for pricing and availability. Specifications are preliminary.

Multiple D/A Converters

Part Number	Resolution (Bits)	Output Type*	Settling Time (μs)	Reference**	Data-Bus Interface (Bits)	Supply Voltage (V)	Features	Price† 1000-up ($)
DUAL								
MAX518	8	V	6	Int (V_{DD})	Serial, 2-wire	+5	2-wire interface, 8-pin SO	2.25
MAX519	8	V	6	Ext	Serial, 2-wire	+5	2-wire interface, separate reference inputs	2.35
MAX522	8	V	70	MDAC	Serial	+2.7 to +5.5	Low-power dual in 8-pin SO	2.25
MAX548A	8	V	***	Int (V_{DD})	Serial	+2.5 to +5.5	2.5V, 8-pin μMAX, low power	1.65
MAX549A	8	V	***	Ext	Serial	+2.5 to +5.5	2.5V, 8-pin μMAX, low power (upgrade to MAX549B)	1.65
MX7528	8	I	0.18	MDAC	μP/8	+5 to +15	Data latches for both DACs	3.79
MX7628	8	I	0.35	MDAC	μP/8	+12 to +15	Data latches for both DACs	3.80
MAX5158	10	V	10	MDAC	Serial	+5	Low power, dual, QSOP-16 pkg.	††
MAX5159	10	V	10	MDAC	Serial	+2.7 to +3.6	Low power, dual, QSOP-16 pkg.	††
MAX532	12	V	4	MDAC	Serial	±12 to ±15	16-pin DIP/SO	8.45
MX7837	12	V	4	Ext	μP/8	±12 to ±15	Dual V_{OUT} DAC with 8-bit data bus	12.18
MX7847	12	V	4	Ext	μP/12	±12 to ±15	Dual V_{OUT} DAC with 12-bit data bus	12.18
MAX5154	12	V	14	MDAC	Serial	+5	Low-power dual DAC in QSOP-16 pkg.	††
MAX5155	12	V	14	MDAC	Serial	+2.7 to +3.6	Low-power, dual DAC in QSOP-16 pkg.	††
MAX5156	12	V	14	MDAC	Serial	+5	Low-power, dual, force/sense pins, QSOP-16 pkg.	††
MAX5157	12	V	14	MDAC	Serial	+2.7 to +3.6	Low-power, dual, force/sense pins, QSOP-16 pkg.	††
MX7537	12	I	1.5	MDAC	μP/8	+12 to +15	Dual DAC with 8-bit data bus	11.23
MX7547	12	I	1.5	MDAC	μP/12	+12 to +15	Dual DAC with 12-bit data bus	11.40
MX7549	12	I	1.5	MDAC	μP/4	+15	Dual DAC with 4-bit data bus	12.97
MAX5150	13	V	16	MDAC	Serial	+5	Low-power dual DAC in QSOP-16 pkg.	††
MAX5151	13	V	16	MDAC	Serial	+2.7 to +3.6	Low-power, dual DAC in QSOP-16 pkg.	††
MAX5152	13	V	16	MDAC	Serial	+5	Low-power, dual, force/sense pins, QSOP-16 pkg.	††
MAX5153	13	V	16	MDAC	Serial	+2.7 to +3.6	Low-power, dual, force/sense pins, QSOP-16 pkg.	††
TRIPLE								
MAX512	8	V	60	MDAC	Serial	+5 or ±5	Low power with shutdown, 14-pin narrow SO	2.85
MAX513	8	V	70	MDAC	Serial	+2.7 to ±3.6	For 3V systems	2.85
QUAD								
MAX500	8	V	4	Ext	Serial	+12 to +15 & -5	16-pin DIP/SO, three reference inputs	5.70
MX7225	8	V	4	Ext	μP/8	+12 to +15 & -5	Double buffered, separate reference inputs	14.14
MX7226	8	V	4	Ext	μP/8	+12 to +15 & -5	Single buffered, single reference input	11.80
MAX505	8	V	6	MDAC	μP/8	+5 or ±5	Rail-to-rail outputs, separate reference inputs	5.95
MAX506	8	V	6	MDAC	μP/8	+5 or ±5	Rail-to-rail outputs, single reference input	6.10
MAX509	8	V	6	MDAC	Serial	+5 or ±5	Rail-to-rail outputs, four reference inputs	5.35
MAX510	8	V	6	MDAC	Serial	+5 or ±5	Rail-to-rail outputs, one reference input	5.19
MAX533	8	V	6	Ext	Serial	+2.7 to +3.6	2.7V, low power (1.9mW), serial, 16-pin QSOP	2.80
MAX534	8	V	6	Ext	Serial	+5	Low-power, +5V, quad DAC in 16-pin QSOP	2.80
MAX520	8	V	***	Ext	Serial, 2-wire	+5	2-wire interface, separate reference inputs	2.85
MAX5250	10	V	10	Ext	Serial	+5	5V, 1mW/DAC, serial, 20μA power-down, 20-pin DIP/SSOP	4.95
MAX5251	10	V	10	Ext	Serial	+3 to +3.6	3V, 0.6mW/DAC, serial, 20μA power-down	4.95

* V = voltage, I = current
** MDAC = 4-quadrant multiplying capability, Int = internal reference, Ext = external reference
*** Settling time depends on internal resistive ladder and external load impedance.
† Prices provided are for design guidance and are for the lowest grade commercial temperature parts (FOB USA). International prices will differ due to local duties, taxes, and exchange rates.
†† Future product—contact factory for pricing and availability. Specifications are preliminary.

Multiple D/A Converters (continued)

Part Number	Resolution (Bits)	Output Type*	Settling Time (µs)	Reference**	Data-Bus Interface (Bits)	Supply Voltage (V)	Features	Price† 1000-up ($)
QUAD (continued)								
MAX526	12	V	3	Ext	µP/8	+12 to +15 & -5	Quad voltage-output DAC, available in DIP/SO	19.44
MAX527	12	V	3	Ext	µP/8	±5	±5V version of MAX526	16.56
MAX536	12	V	3	Ext	Serial	+12 to +15 & -5	Serial version of MAX526	15.95
MAX537	12	V	3	Ext	Serial	±5	Serial version of MAX527	15.95
MAX5253	12	V	16	Ext	Serial	+3 to +3.6	3V, 0.6mW/DAC, serial, 20µA power-down	11.35
MAX525	12	V	20	Ext	Serial	+5	1mW/DAC, serial, 20µA power-down, 20-pin DIP/SSOP	11.95
MAX514	12	I	1	MDAC	Serial	+5	Quad current-output DAC, available in DIP/SO	14.25
OCTAL								
MAX528	8	V	5	Ext	Serial	+5 to +15, +15 & -5 or +5 & -15	µP-selected buffered and unbuffered output	6.90
MAX529	8	V	5	Ext	Serial	+5 or ±5	Single +5V supply MAX528	5.65
MX7228	8	V	5	Ext	µP/8	+5 to +15 & -5 or +15	Single or dual supplies	11.95
MAX521	8	V	6	Ext	Serial, 2-wire	+5	2-wire interface, five reference inputs	4.95
MAX547	13	V	5	Ext	µP/13	±5	Unipolar or bipolar, four reference inputs	29.60

High-Speed D/A Converters

Part Number	Resolution (Bits)	Output Type*	Settling Time (ns)	Reference**	Data-Bus Interface (Bits)	Supply Voltage (V)	Features	Price† 1000-up ($)
MAX5140	8	I	3	Ext	Parallel	-5.2	400MHz high-resolution video DAC with controls	‡
MAX5018	8	I	4.5	Ext	Parallel	-5.2	165/275MHz video DAC with controls	‡
MAX555	12	V	0.5	Ext/MDAC	Parallel	-5.2	300MHz update rate, 72dB SFDR	‡
MAX5012	12	V	13	Ext	Parallel	-5.2	High-speed, 12-bit, 100MHz DAC with ECL inputs	‡
MAX5013	12	V	13	Ext	Parallel	+5, -5.2	High-speed, 12-bit, 100MHz DAC with TTL inputs	‡

* V = voltage, I = current

** MDAC = 4-quadrant multiplying capability, Int = internal reference, Ext = external reference

† Prices provided are for design guidance and are for the lowest grade commercial temperature parts (FOB USA). International prices will differ due to local duties, taxes, and exchange rates.

‡ Contact factory for pricing.

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Perspective On Time-To-Market

BY RON KMETOVICZ
President, Time to Market Associates Inc.
P. O. Box 1070, 100 Prickly Pear Rd., Verdi, NV 89439; (702) 345-1455; fax (702) 345-0804;
e-mail:kmetovicz@aol.com.

RON KMETOVICZ
CONTRIBUTING EDITOR

Quality—the pursuit of process perfection and the manufacture of products with decades of life—provides considerable benefit to business, but it also has an infrequently discussed dark side. It just may not be in the best interest of a company to have products last too long.

As I scan my office, equipment nearly a decade old performs many vital functions. An old Phone Mate 600 reliably receives and sends faxes. A Canon PC 65 copier serves its intended application without any malfunction. A QMS-PS 410 printer keeps my business press in full operation. A MAC SE-30 still produces much of the black and white artwork used in my business; and a host of smaller items make their contributions as required.

These old machines now have personalities—I know how to extract maximum benefit while dealing with their less-than-desirable properties. Now, while I have no assurance of the life remaining, I am confident that a few years will pass before anything breaks. Manufacturers, who have a vested interest in my equipment turning tail, would prefer a sudden, timely, lightning strike! Could this stuff be too good?

From personal satisfaction and financial perspectives, the products I've come to know and respect have done their jobs. Friends and associates routinely view my business, seeing with their own eyes what I use, and many ask what I think. Naturally, I talk positively about the items that serve me well, which definitely contributes to the word-of-mouth advertising process in a supportive way. And maybe, I've even developed a bit a brand loyalty.

I know that any item that breaks goes to the dump. But, while grateful for the service, I probably would have been just as content at the four- or five-year point. The products did not have to live this long.

For the most part, style, functionality, and performance now drive product obsolescence. Obviously, these tactics did not work on me. For others, a style change alone does it. They toss the old device for a new model that looks different. Some require more functionality, while the most resistant demand more performance. And at each step along the way, most expect the price to come down a bit too!

Market-savvy product-development organizations use these techniques effectively to send perfectly good products to the scrap heap before they reach the end of their useful life. But the rush for smaller, faster, and cheaper products may be slowing. As it does, wear mechanisms take on a greater degree of importance.

From a time-to-market perspective, product development organization leaders must give serious thought to product life issues while new products are in design. Make sure you know when they will wear out or how you will make them obsolete. Bring a cross-functional team together to address this topic. Hold fast until they arrive at a solution that meets your business needs and the desires of your customers.

The future success of your business, not to mention the engineering teams' future employment prospects, depends on taking this topic very seriously.

READER SERVICE 227

ITS: Your Foul Weather Friend

Each year, Winter's arrival brings changes to the weather that make driving more difficult. In some areas, heavy snowfall and avalanche hazards can make driving a downright dangerous proposition. The key to staying safe and sound is knowing how to modify your driving to accommodate these changes.

Unfortunately, weather conditions, especially in mountainous regions, change very rapidly. During these times, radio stations—a driver's primary source of communication—generally don't broadcast weather reports frequently enough to keep travelers up to date on the latest road conditions. As a result, drivers in these areas are stuck in a hazardous guessing game that could end in tragedy.

Nowhere is this situation more evident than on a 40-mi. stretch of Interstate 90, east of Seattle Washington, known as Snoqualmie Pass. Bad weather coupled with the road's layout, heavy truck traffic, and drivers' unfamiliarity with the landscape, makes driving at the posted 65 mph speed limit inappropriate. It often leads to a high accident rate during the winter months.

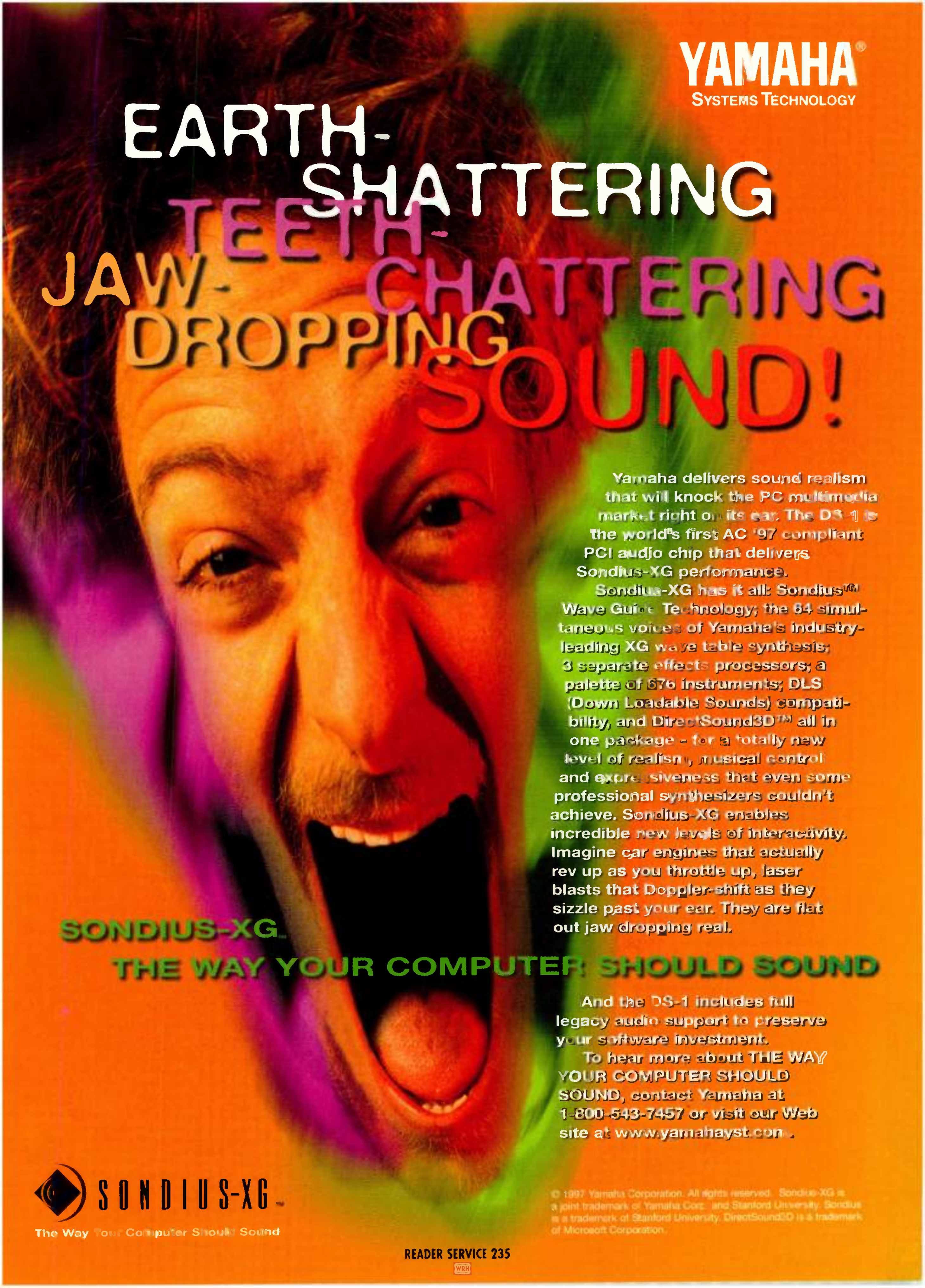
As part of a nationwide Intelligent Transportation System (ITS) program geared toward making travel safer, the Snoqualmie Pass area has been selected as a test case to determine how to improve driver safety. The Federal Highway Administration, the Washington State Department of Transportation (WSDOT), and the University of Washington have banned together to develop Travel Aid. Travel Aid is a new information system designed to reduce accidents. If successful, the project is expected to be duplicated, in part, if not whole, in other areas plagued by similar problems with inclement weather.

Travel Aid offers a dynamic speed capability. What this means is that a driver can get immediate information on weather conditions and the speed he or she should maintain to travel in the safest manner possible. It works by collecting information from a number of sources. Wide-aperture radar tracks vehicle speeds, and six weather stations monitor temperature, humidity, precipitation, wind, and specific road surface conditions. This information is then transmitted to a control center where safe speeds are calculated, confirmed by the WSDOT, and transmitted back to the driver via nine variable message signs.

As part of the Travel Aid system, surveillance cameras that let Internet users view real-time traffic conditions also will be installed. Travel speed information will be available later this year at the *www.SmartTrek.org* web site.

To obtain more information contact Smart Trek, Pacific Rim Resources, 600 University Street, Suite 2010 Seattle, WA 98101; (206) 623-0232 ext. 202; fax (206) 623 0781.

Cheryl Ajluni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READER SERVICE 235

XTRA

When I think about a 763-mph performance by an experimental car, VROOOM comes to mind. My thoughts turn to the potential of the car's breaking apart as it surpasses the land speed record and breaks through the sound barrier. But this machine stayed intact. Why? Lots of Permabond epoxy resins.

Castrol's Thrust Supersonic Car (shown at right), fitted with two Rolls Royce jet engines (yielding about 50,000 lb. of thrust—and a boatload of vibration), was treated with four of Permabond's adhesive products. These high-tech epoxy resins were used in and on the car because bolts, rivets, and welded joints simply weren't going to hold it together during the experiment. One of the primary sources for loosening of bolts is constant vibration.


Photograph courtesy of Castrol

Permabond, a division of National Starch and Chemical Company, supplied three adhesives and a pretreatment product (not to mention technical support) for the Thrust Supersonic Car project: SIP, the Self-Indicating Pretreatment; A130 Threadlock; E32; and ESP110.

SIP is a kit that shows the user if a surface has been suitably prepared for the bonding process. If a surface has not been properly prepared, the bonding will not hold.

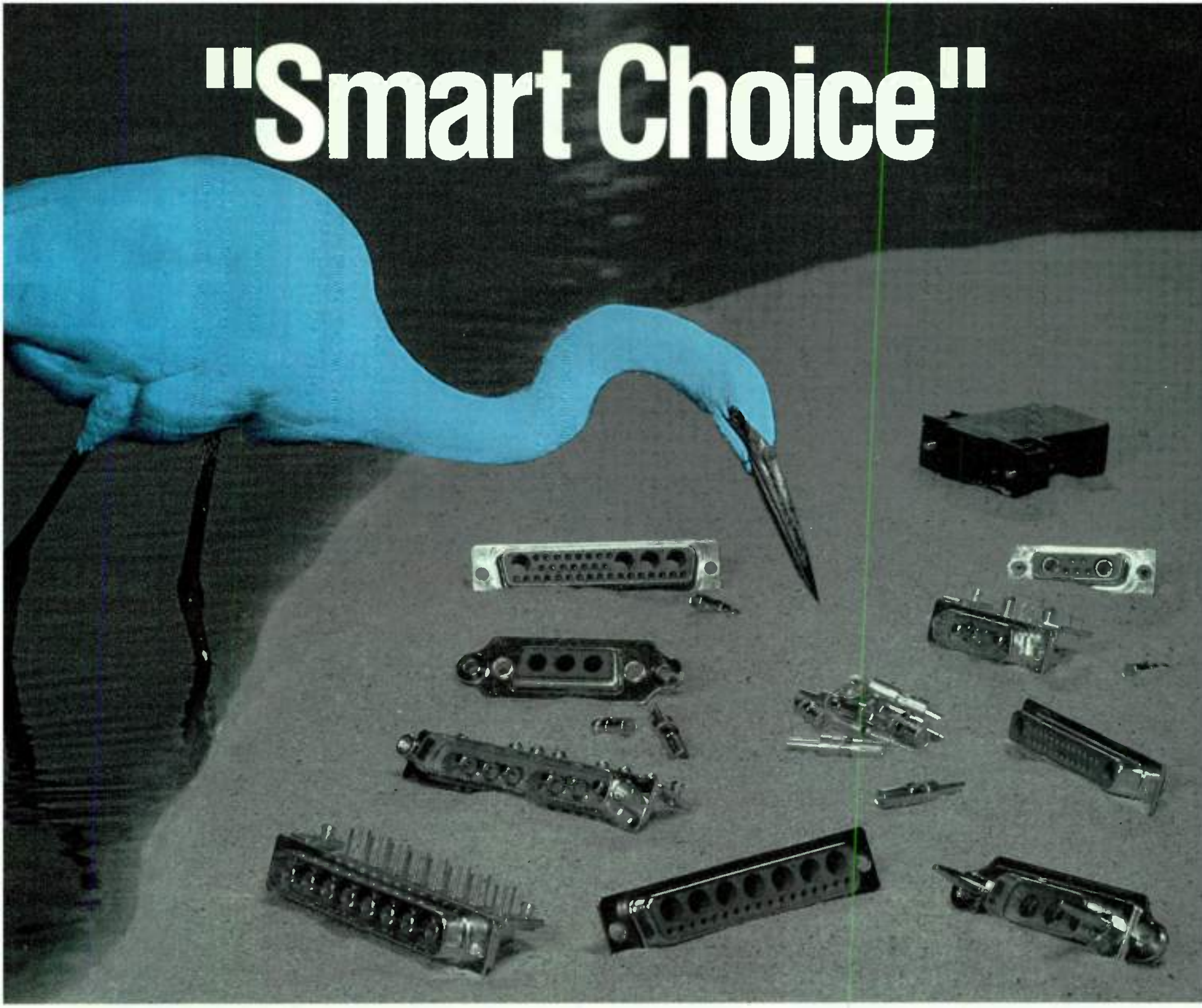
A130 Threadlock adhesive is specific to locking nuts and screws where the panels may be removed. Even supersonic speeds won't loosen nuts and screws that have been sealed with this adhesive.

The E32 two-part epoxy was used in bonding the panel work onto the main welded box beam core of the supersonic car. This hardy adhesive is dispensed from side-by-side cartridges, and was used throughout the building of Thrust. E32 is not recommended for excessive temperature resistance.

ESP110, on the other hand, is a very-high-strength, maximum durability adhesive that can take the high temperatures generated by those jet engine afterburners. The high-speed video tape of the testing showed that even when a panel may have been suffering from considerable heat and vibration, the areas bonded by ESP100 displayed no movement at all.

The Thrust Supersonic Car is made from such materials as aluminum, steel, titanium, and carbon and glass fiber composites. All are bonded by Permabond adhesives.

For more information, contact Permabond, 480 S. Dean St., Englewood, NJ 07631; (800) 653-6523 or (800) 370-9647 (helpline); fax (201) 567-3747; www.permabond.com.—**DS**



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READER SERVICE 154

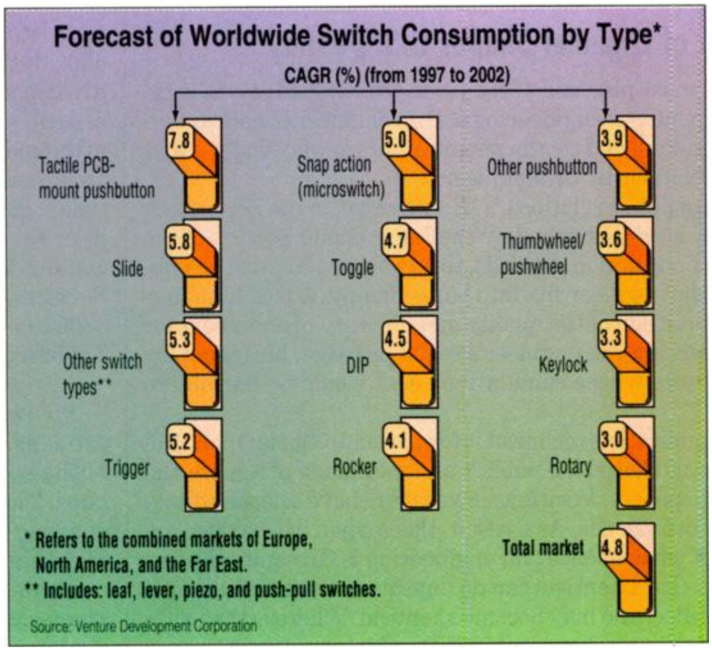
ELECTRONIC DESIGN QUICKLOOK

■ Edited by Debra Schiff

MARKET FACTS

Switching Places In The Market

The market for electromechanical switches is growing slower than many major switch providers have expected. Switch consumption in Europe, North America, and the Far East combined, is about $3.1 billion. Overall, that market is forecast to grow at 4.8% annually, reaching $4 billion in 2002. This figure represents a slight decrease in worldwide switch consumption growth, when compared to the prior five year period between 1992 and 1997, which saw 5% annual growth, according to a recent report by Venture Development Corporation (VDC), entitled "The World Market for Switches in Electronics." The report projects the following compound annual growth rates (CAGRs) for consumption over the next five years in these markets: Europe 1.5%, North America 4.0%, and the Far East 6.9%. The slowdown in switch consumption growth is due in part to slow economic turnarounds in Europe, and recent downturns in Far Eastern markets. Another contributing factor is the introduction of alternate technologies to address switching needs, displacing switches in applications. Though switch alternatives such as switch pads, touchscreens, and software solutions are increasingly being introduced, electromechanical switches still provide inexpensive and reliable methods of implementing switching functions. These advantages, in many instances, will continue to supersede selection of newer, more aesthetically pleasing technologies. Three particular switch types dominate the scene, accounting for 63% of total switch consumption in 1997. These are: snap-action (microswitches), pushbutton, and slide switches. The highest growth rate (7.8%) is forecast for tactile pc board mount pushbutton (tact) switches. Though these make up only 29% of pushbutton sales, the compactness, reliability, and versatility of these switches will keep demand high. Electromechanical switches are used in a wide variety of applications. The leading industry segments for consumption are: consumer electronics, appliances, communications equipment, computers/peripherals, and industrial controls. Switch sales for these applications will total $2.6 billion in 2002. VDC's study uncovered several trends which are shaping the industry and intensifying competition among the world's switch manufacturers. Automated production and other advancements are allowing manufacturers to turn out smaller, more reliable switches. The introductions of the half-pitch DIP switch and the tact switch are evidence of this trend. Shifting manufacturing operations to lower labor cost countries, and/or moving closer to the major consuming industries is seen to lower costs and raise profits, as price-based competition intensifies. Switch manufacturers usually follow one of these business strategies: Some firms offer broad lines of switches, covering many applications, and in many cases, wide geographic markets; and many firms offer narrow lines of switches, often only one type, selling for limited or specialized applications. The former can provide switches in abundance, as required by OEMs producing large quantities. The latter tend to be smaller suppliers serving niche-market applications. They avoid the difficulty of competing on a price basis with the broad-line suppliers of standard or low-end switches.

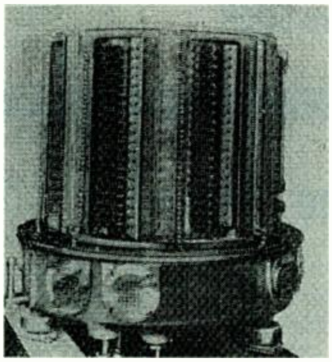


John Gordon is a project manager/industry analyst for VDC, a marketing research firm specializing in electronic technology. Gordon holds a BS in Medical Sciences from Northeastern University, Boston, Mass. and an MBA from Bentley College, Waltham, Mass. He can be reached at (508) 653-9000, ext. 126 or by e-mail: jgordon@vdc-corp.com.

40 YEARS AGO IN ELECTRONIC DESIGN

Magnetic Storage Drum

A total storage of 15,000,000 binary bits in a drum measuring 15-in. in diameter and 14-in. high is the primary feature of this unit. Called the HD (high density) file drum, the unit consists of the drum, driving and lubrication system, track-selection mercury relay matrix, linear readout preamplifier, and final writing amplifier. Average random-access time provided to any data is 180 msec. The complete drum has 320 tracks, 20 of which are used as spares. The recording heads are assembled in pairs. Mating surfaces of the head pole pieces are optically lapped, and a lubrication system is provided to ensure a very small uniform separation between the heads and the drum surface, and therefore, a very high recording density. The matrix of relays used for track selection are a pressurized, mercury-wetted-contact type. Laboratory for Electronics, Inc., 75 Pitts St., Boston 15 Mass. *(Electronic Design, February 5, 1958, p.52)*



It was big (about a 15-in. cube) and slow (about 180-ms access time), but at almost 2 Mbytes, this magnetic drum memory was starting to give a glimmer of significant storage capacity.—Steve Scrupski

Editorial: Public's View of Engineer Shapes U.S. Destiny

Scientists and engineers must play one of the most predominant roles in future society. Our destiny depends on engineering and on engineers being understood by our government leaders, and by the people at large, who shape public policy. This calls for public relations by the engineer.

In advocating a program of public relations, T. E. Garrigan, in the September issue of the *Pulse of Long Island* (published by the Long Island Section of the IRE), says "...the future of our nation depends, to a great extent, on the public's understanding of how the engineer fits into our economy. A lack of understanding can lead to a deterioration of the quality and quantity of engineers for the future; it can lead to lowering the engineer's social prestige, his monetary remuneration and other factors whose cumulative effect would be harmful to the whole nation."

There is a need for communicating technical information to the layman. Recent surveys report that, by and large, the public's understanding of science and engineering comes from newspapers. Very few newspapers have science editors who know anything at all about science. As a result, the layman has no deep appreciation or clear picture of what science and engineering is. In some respects he's too gullible; he assumes that scientists can do anything once they set their minds to it. Of course, if he reflects he may become skeptical. Where is that color TV set that he read he was going to have in 1957? We think engineers can do something about this themselves. We congratulate the Long Island IRE members who are, among other things, giving programs for the non-technical public. John R. Pierce packed the auditorium with his fascinating, yet informative discussion "Fancies and Fallacies of Space Travel." They are also slanting publicity releases concerning members and activities to the average citizen. Each engineer is encouraged to actively participate in at least one community activity.

Garrigan says, be a good citizen and you will be a better engineer. We agree.—JAL *(Electronic Design, February 5, 1958, p.25)*

Managing editor Jim Lippke's call for engineers to get involved in the community is probably just as valid today as it was 40 years ago, if not more so, with technology so much more pervasive today.—Steve Scrupski

Steve Scrupski is a former Editor-in-Chief of ELECTRONIC DESIGN. Now semiretired, he can be reached at scrupski@worldnet.att.net.

OFF THE SHELF

Electronic Display Measurement is a guide to the most reliable techniques, methods, and instruments available for measuring electronic displays. Supplemented with an extensive bibliography, industry standards, equations, and tables, the book includes an appendix of equipment manufacturers and nearly 100 illustrations and charts. Readers are shown how to measure luminance, contrast, quality, uniformity, and other characteristics. The 326-page book is priced at $69.95. Contact John Wiley & Sons Inc., 605 3rd Ave., New York, NY 10158-0012; (212) 850-6336; www.wiley.com.

Thermal Management Handbook covers thermal management issues in electronic packaging. The book addresses areas such as measuring thermal properties of different materials; assessing heat loss in active devices, in conductor traces, and at high frequencies; determining temperature at a given point or region in an electronic assembly; conducting thermal analysis of common configurations found in electronic assemblies; and cooling of electronic circuits. The 650-page book is priced at $89.50. For more information, contact McGraw-Hill Inc., Customer Services, P.O. Box 545, Blacklick, OH 43004-0545; (800) 722-4726; fax (614) 755-5645; mcgraw-hill.com.

Spark Discharge provides a comprehensive, systematic description of the spark breakdown of long gas gaps. The book discusses the nature of a long spark, physical peculiarities of relevant gas discharge processes, methods and results of experimental studies, and analytical and numerical models. Featured topics include an overview of the phenomena underlying the mechanism of spark discharge; substantiated methods to solve problems in high-voltage engineering and lighting; and illustrative material to help readers understand details of the space-time pattern of the process. The 304-page book is priced at $99.95. For more information, contact CRC Press, 2000 Corporate Blvd., N.W., Boca Raton, FL 33431-9868; (800) 272-7737; fax (800) 374-3401; www.crcpress.com.

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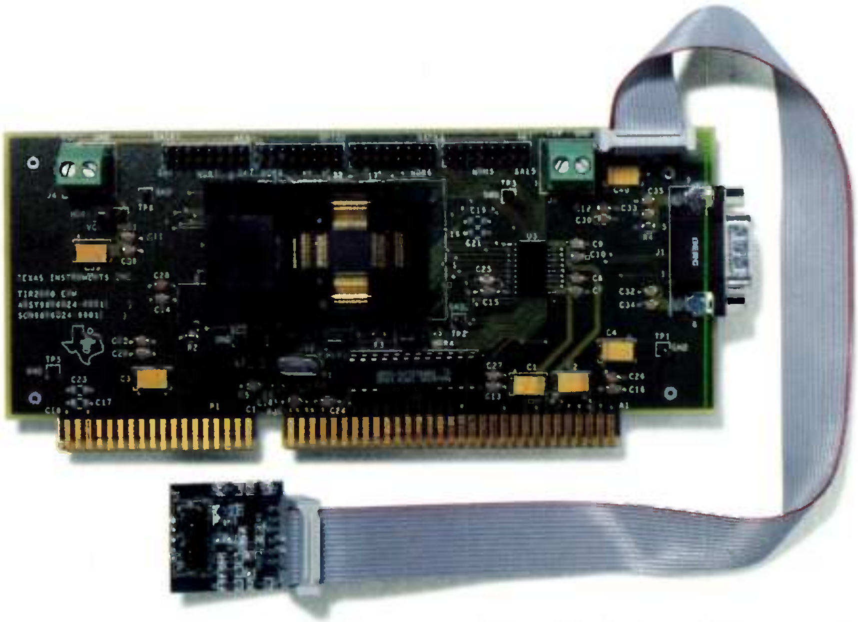

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The TIR2000 infrared data controller from TI combines with the TSLM1100 receiver/LED driver to form the first fully compliant 4-Mbps IrDA system solution. The TIR2000 works seamlessly with the TSLM1100 to support all IrDA data rates, including 4 Mbps, which is critical for applications such as file transfers from a digital camera to a PC or printer. Plus, TI's IrDA evaluation module (EVM) is the fastest way to get designers started on their IR designs. The module also comes with driver software for use with Microsoft® Windows® 95.

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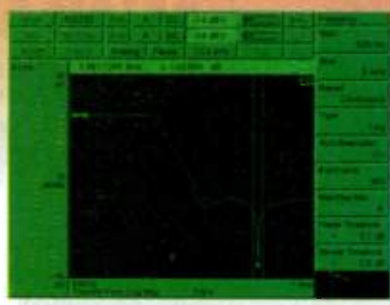

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MEETINGS

MAY

IEEE International Symposium on Circuit Systems (ISCAS '98), May 31-June 03. Monterey Conference Center,Monterey, California. Contact Sherif Michael, Department of Electrical & Computer Engineering, Naval Postgraduate School, Monterey, California 93943; (408) 656-2252; fax (408) 656-2760; e-mail: michael@ece.nps.navy.mil.

JUNE

International Conference on Consumer Electronics (ICCE), June 2-4. Los Angeles Airport Marriott, Los Angeles, California. Contact Diane Williams, Conference Coordinator, 67 Raspberry Patch Drive, Rochester, New York 14612-2868; (716) 392-3862; fax (716) 392-4397, e-mail: d.williams@ieee. org; www.icce.org.

IEEE International Conference on Communications (ICC '98), June 7-11. Atlanta,Georgia. Contact Debra Jordon, general secretary; fax (404) 881-6057; e-mail: icc98@comsoc.org. www.comsoc.org/confs/icc/98.

IEEE/MTT-S International Microwave Symposium (MTT 98), June 7-12. Baltimore Convention Center, Baltimore, Maryland. Contact Steven Stitzer, Westinghouse Electric Corp., Post Office Box 1521, MS 3T15, Baltimore, Maryland 21203; (410) 765-7348; fax (410) 993-7747.

USENIX 1998 Technical Conference, June 13-17. Marriott Hotel, New Orleans, LA. Contact USENIX Conference Office, 22672 Lambert St., Suite 613, Lake Forest, CA 92630; (714) 588-8649; (714) 588-9706; e-mail: conference@usenix.org; www.usenix.org.

35th Design Automation Conference, June 15-19. Moscone Center, San Fr cisco, CA. Contact MP Associa 5305 Spine Rd., Suite A, Boulder, C 80301; (303) 530-4333; e-mail: da info@dac.com; www.dac.com.

JULY

IEEE International Geoscience & Re Sensing Symposium (IGARSS '98), July 6 . . Sheraton Seattle, WA. Contact Tammy I. Stein, IGARSS Business Office, 2610 Lakeway Dr., Seabrook, TX 77586-1587, (281) 291-9222; fax (281) 291-9224; e-mail: tstein@phoenix.net.

MANAGING THE DESIGN FACTORY

Once upon a time there was a talented group of engineers who worked for an insecticide company. The Marketing Department was constantly complaining that Engineering did not know how to kill bugs.

"We'll show them," said the engineers, and they whipped up a fabulous chemical that would kill any bug known to mankind. "Here, try this," said the engineers, smiling. "We must to do a field test," said the marketeers, and they flew off in fancy jet planes to test the pesticide.

DON REINERTSEN
CONTRIBUTING EDITOR

A few weeks later they came back gloating. "It does not kill bugs," they sneered. Being good marketeers, they also offered to solve the problem by saying, "You just need to make it stronger." The engineers said, "We don't think we should do that. It had to work. It will kill any bug known to mankind. Where did you find these customers? Are they forgetting to take the cap off the container?"

Good sense prevailed, and they decided to check the facts. An engineer asked one customer what was wrong. Here's how the conversation went:

"It doesn't kill bugs," said the customer.

"How do you know?" asked the engineer.

"Well, I spray them and they just walk away as if nothing happened. Even when I soak them with the stuff they just walk back inside the wall."

"But, they've been poisoned. They are going to die!"

"Well, they look pretty healthy to me."

"But, do you ever see them again?"

"I don't know," said the customer. "Frankly, the bugs all look the same to me."

"How could I convince you that it was working?"

"Well, when you get them with a real insecticide, they roll over on their backs and wiggle their legs in the air."

In fact, the way a customer judges whether an insecticide works is by what the bug does right after it's sprayed. You can produce a 100% fatal insecticide, but if doesn't make the bugs roll over and die a painful death, you won't sell a can of it. A bad insecticide designer will assume that the problem is to kill bugs. A good one will add a short-acting neurotoxin to knock out the bug's nervous system while the poison kills it.

It's critically important to know how a customer judges your product performance. For every stated need ask, "How do you know you've gotten what you want?" You will find that customers often judge product success by characteristics that have nothing to do with the stated problem.

Don Reinertsen is president of Reinertsen & Associates, a consulting firm specializing in product development management. He can be reached at (310) 373-5332 or e-mail: DonReinertsen@compuserve.com.

@IEEE

In what has been termed as the "era of the young guns," the Institute of Electrical and Electronics Engineers (IEEE) has begun to develop a set of programs that address the needs of older engineers in the U.S. The primary issue is that these experienced professionals are being faced with a corporate culture that favors the younger, more recently trained in new technology worker. And, they need the kind of support that only the world's largest society of engineers can offer.

"Things are getting worse," says Chris Currie, external communications supervisor at IEEE, "Companies are targeting the young workers and putting the older ones out to pasture." There are rising numbers of older engineers who are being involuntarily retired. But, IEEE is determined to come up with some solutions. Currently, they're in the committee stage. All of the committees that have anything to do with careers (i.e. Workforce, Employment Assistance, Career Maintenance and Development, etc.) are gathering to try to develop projects and, of course, standards.

The new proactive approach taken by Paul Kostek, president-elect of IEEE for 1998, is one of meeting needs and creating programs. The thrust of this new movement is, "to help [the displaced 50 and over year olds] focus on managing their own careers."

The new plans for 1998 will definitely focus on teaching older workers how to market themselves in a changing workforce. One aspect of career development that has changed over the years is the resume. "They need to look more carefully at their skills," says Kostek. They also need to maintain their skills through continuing education, keeping up on the latest industry publications, and investigating what the Internet has to offer. Most importantly, the senior workforce has to monitor the marketplace.

The approach the IEEE is taking with these programs is more entrepreneurial. To support that direction, there is an alliance of IEEE consultants' networks. Teaching these prospective business owners how to sell their own wares, make contracts, and generally make the transition into ownership is also on the IEEE's list of projects. Additionally, the committees who have been meeting have developed a Best Practices list involving the corporations who treat their older workers with the most respect and fairness. Anyone interested in these projects should check out the 1998 Professional Activities Conference to be held at the Sheraton Crescent Hotel, Phoenix, Ariz., April 30-May 1.

Contact IEEE at (202) 785-0017 or visit the web site: http://www.ieee.org/usab.—DS

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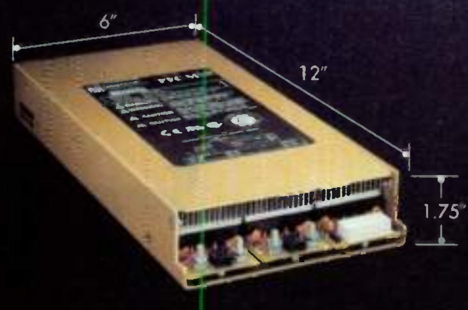

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THE ENVELOPE, PLEASE

Competition is always healthy for business, but sometimes it's healthy for the consumer as well—and not just in terms of saving money. When companies start competing for awards in optimum and creative pollution prevention, we all end up winning. In this case, it's the Evergreen Award.

The Environmental Protection Agency gives the Evergreen Award to companies in the Pacific Northwest that fulfill three primary criteria: documented achievement in pollution prevention, a commitment to the environment, and a history of environmental leadership. The idea is to teach companies in that region (and others) that it is possible to achieve economic prosperity while preserving the environment for generations to come.

The Evergreen Award also coincides with the newest ISO initiative, 14001. ISO 14001 is the international standard for the documentation and implementation of environmental management. Three elements of the new ISO standard include pollution prevention, compliance with environmental regulations, and continuous improvement.

The most recent Evergreen Award winner is Micron Technology. Micron was the first Northwest company to be certified for ISO 14001. The company successfully reduced hazardous and solid wastes, air emissions, and water discharges.

The award was given to Micron on September 15, 1997, kicking off Pollution Prevention week (Sept. 15-21). Pollution Prevention week is a national campaign to encourage government, individuals, industry, and institutions to squash pollution before it starts. The aim is to improve the local environment's quality.

Nominations for the Region 10 Evergreen Award are accepted from environmental regulatory agencies and independent businesses.

For nomination information, contact the United States Environmental Protection Agency, Region 10, 1200 Sixth Ave., Seattle, WA 98101; (800) 424-4372; e-mail: gangmark.carolyn@epamail.epa.gov.

—DS

OFF THE SHELF

Fundamentals of Nonlinear Digital Filtering presents and evaluates current methods and applications in nonlinear digital filtering. The book covers dozens of classes of filters, and includes basic ideas, definitions, algorithms, and impulse and step responses for each. Results are presented to allow comparisons of filtering operations. Readers are aided in selecting the best algorithm for the particular problem. Also, it provides benchmark information on the performance of current methods. The 288-page book is priced at $79.95. Contact CRC Press, 2000 Corporate Blvd., N.W., Boca Raton, FL 33431-9868; (800) 272-7737; fax (800) 374-3401; Internet: http://www. crcpress.com.

RF and Microwave Circuit Design for Wireless Communications addresses the modulation schemes and higher frequencies required of today's wireless communications circuits. Covering cutting-edge developments in mixer circuits, frequency synthesizers, amplifier design, noise, and the future of wireless communications, the book helps readers design applications for digital cellular telephony, wireless LANs, PCS, GaAs and high-speed silicon bipolar IC technology, and low-power RF circuit technology. The 411-page book is priced at $89. Contact Artech House Publishers, 685 Canton St., Norwood, MA 02062; (800) 225-9977, ext. 4030; fax (781) 769-6334; Internet: http://www.artech-house.com.

Discover Intranets is written for nontechnical managers who want an overview of the technology, and information technology professionals who want to learn more about the content side of the digital world. Part I, "Are You Ready for an Intranet?" gives tips on justifying the resources needed to implement a system. Part II, "How to Create and Maintain an Intranet" dives into the nuts and bolts of creating a system. Part III, "Advanced Intranet Features" shows readers how to keep their system on the cutting edge. The book is priced at $19.99. Contact IDG Books Worldwide Inc., 919 E. Hillsdale Blvd., #400, Foster City, CA 94404; (415) 655-3000; fax (415) 655-3299.

READER SERVICE 125

READER SERVICE 243

FLIPPING THROUGH THE INTERNET ROLODEX

http://web2.airmail.net/gbeene/winplace.html: The world according to Gary Beene is a Visual Basic (VB) one. His web site is divided into four sections: Community, Microsoft, Hardcore, and Training. The Community section is dedicated to the Who's Who of VB, VBSites, and SIGs (user groups). The Microsoft area features links to the company's VB, VB for Applications, VBScript, ActiveX, Developers, and Summary pages. Hardcore lists links to books, magazines, files, vendors, USENET groups, BASIC information, and Access information. In the Training section, visitors to the site can find help for beginners, tutorials, TV/Radio facts, and other related sources. The newest development at Gary Beene's Visual Basic World is the addition of WinPlace. WinPlace is a downloadable tool that allows designers to place MCM/Hybrid components on a substrate, and look at that layout in 3D. Beene wrote the program so that potential customers could manipulate the layout before the final design was assigned.

http://www.syntelinc.com/y2kconsultant/: Visitors to Syntel's Y2K Consultant Online site will find tools and resource information to address the Year 2000 Date Change issue. Because of the lack of information regarding Y2K, Syntel divided it's consulting site into two parts: Resource Information and Helpful Tools. After registering at the site, visitors can follow the resource path to find an Executive Overview, Frequently Asked Questions, and Getting ROI (return on investment) for the Y2K Project. In Helpful Tools, the site viewer can download a Request for Proposal template for external service provider bids and a customizable project estimator tool. Project Estimator first looks at the COBOL code, then the non-COBOL platforms, and finally the databases and files. It also provides estimates for both on-site and off-site solutions. Additionally, site visitors will find information on Method2000, Syntel's 10-phase approach to Y2K compliance.

http://www.anadigics.com: Surfing to Anadigics' site yields a wealth of communications information. Visitors to the home page should keep their Real Audio handy, because such items as third quarter updates given through conference calls are easily available at the site. The Corporate Information section features an interview with CEO Ronald Rosenzweig that can be viewed via streaming video. Anadigics flies their ISO 9001 flag at the site, with a full description of the process. Links to a host of industry resources and communications headlines from Newspage (*http://www.newspage.com*) can be found in the Links and Industry Headlines section at the site. Throughout the site, visitors will find a button marked Technical Glossary, which can be quite handy. Also at the site is a tour visitors can take of the new Fab. Of course, if you're purely puttering around the web looking for job openings, you've come the right place—Anadigics has a Human Resources section that's ripe with opportunities. Most notably, Engineering Tools section offers visitors a generic receiver model that uses a Java applet. This model allows users to calculate gain, dynamic range, noise figure, and other system parameters by inputting certain values. In addition, the site also houses a Javascript-based tool, the Transimpedance Amplifier Tool, which calculates the bandwidth, sensitivity, and optical overload when visitors enter photodiode and filter parameters.

http://www.cdw.com: Dropping in on the Computer Discount Warehouse (CDW), visitors can shop for the new desktop or notebook computer with the element of comparing different systems side-by-side. Up to five systems can be compared at a time. Currently, CDW's database includes about 40 features for over 500 desktop and portable computers, as well as servers for the side-by-side comparison. Over 16,000 products are available to search and order on line. Both Macintosh and PC systems are handled at the site. For the value-conscious shopper, there is an extensive Coupon section that lists pages of mail-in rebates from all the major manufacturers (and some of the minors, too). CDW updates the pricing and stock information continually.

GREENLOOK

Last October, residents of Santa Clara County, Calif., were asked to recycle their used computer equipment by dropping them off at designated computer retail locations, including Fry's Electronics, Computer City, and OfficeMax.

The collection and recycling project was made available through a public/private partnership that included Unisys Corp., Envirocycle Techneglas, Berman's Diversified Industries, the U.S. Environmental Protection Agency (EPA), the California Environmental Protection Agency, the U.S. Environmental/Recycling Hotline, the California Newspapers Association, Santa Clara County, and the City of San Jose.

"There's still some value in those old computers, and reusing and recycling them sure beats throwing them into landfills," said Felicia Marcus, the EPA's western regional administrator. "We are urging everyone to take an important step toward conserving our natural resources by going to their garages and attics, digging out their dusty old machines, and recycling them."

The project was part of a nationwide computer recycling pilot program to determine the feasibility of collecting, transporting, and recycling computer equipment collected from individual households and small businesses. The equipment was taken from the collection points to Berman's Diversified Industries, a de-manufacturing facility located in the San Jose area. Berman will either re-market or recover and recycle materials and components.

"The cleanup is proving to be a convenient means of assisting Californians with information on participation in environmentally friendly programs such as recycling old computers," said Peter M. Rooney, California Secretary for Environmental Protection. "This is a common sense way to help protect the environment and add economic value through recycling products that otherwise would add to landfill waste."

The recycling centers accepted computer equipment such as CPUs, monitors, keyboards, printers, peripherals (mice, cords, external storage devices, etc.), and internal computer parts (hard drives, floppy drives, CD-ROMs, power supplies, cards and chips, etc.).

For more information on this or similar projects, contact the U.S. Environmental/Recycling Hotline at (800) CLEANUP; Internet: http://www.1800cleanup.org.

A new process from Bell Labs is making it possible for Lucent Technologies to improve the recovery and recycling of an important natural resource—germanium—from the waste products of optical-fiber manufacturing and to save millions of dollars at the same time.Bell Labs is the research and development arm of Lucent Technologies.

In optical-fiber manufacturing, a silicon-containing vapor, such as silicon tetrachloride, and a germanium-containing vapor, such as germanium tetrachloride, undergo a high-temperature chemical reaction with oxygen to produce silicon oxide—germanium oxide glass.

The precise use of these vapors allows control of the refractive-index profile of an optical fiber, so the lightwave signals traveling through the fiber will stay within the fiber's core for hundreds of miles. This use of germanium accounts for more than 35% of today's global industrial consumption.

Optical fiber, hair-thin, ultrapure glass, is used in communications systems to carry voice, data, and video signals that have been converted into the ones and zeros of digitized information and transmitted as pulses of light.

The process is part of a system that removes all hazardous wastes from the gases exhausted from fiber manufacture.

Optical fiber is about 96% silicon oxide (the main component of sand) and about 4% germanium dioxide, with small amounts of other elements.

For more information on the process, see Lucent's web site at http://www.lucent.com.—**MS**

On-Line Gaming Goes Professional

I never thought I'd be writing this, but there's now a league of professional on-line game players. AMD, the flash memory and programmable logic manufacturer, now wears the hat of sponsor of the AMD Professional Gamers League (PGL). The season opened November 3 with a qualifying match at 3COM Park at Candlestick Point. Other sponsors of this new professional sport include the Total Entertainment Network (TEN) and Ziff-Davis.

TEN, holding on-line rights to over 30 games, is a gaming network supported by many gamers on the Internet. It's got some big supporters in Ameritech; Goldman Sachs; Kleiner, Perkins, Caufield, and Byers; and Vertex Management to name a few. More than half of the games are exclusive to TEN and were developed by popular game publishers such as Apogee, Blizzard, Bungie Software, GT Interactive, Maxis, MicroProse, Sierra Online/Papyrus, and SSI.

Cash and prizes for the league's first year total over $250,000. This first season of gaming will include two categories: Action and Strategy. The Action category is presently represented by id Software's Quake. In the Strategy category, Westwood Studio's Command and Conquer: Red Alert game will challenge the participants. The PGL expects that more games and categories will be added next season.

In order to game within the PGL, players must subscribe to TEN's service and register for the PGL at the league's web site: *http://www.pgl.net*. The league is designed to be like any major league in that there are star players; referees; spectators; sponsors; and, of course, the endorsements. Not only will there be individual competition, but team gaming as well. To complete the new sports entertainment concept, the PGL has a governing board and a commissioner.

For more information, contact AMD, One AMD Place, P. O. Box 3453, Sunnyvale, CA 94088-3453; (408) 749-5703; Internet: http://www.amd.com.—**DS**

DESCRIPTION

The FT and FS Series are comprehensive lines of ultra compact power factor corrected models derived from our Moduflex® family of switching power supplies. This series utilizes advanced technology to produce a high quality input current wave form that is compliant to the harmonic requirements of EN61000-3-2. Based on modular construction, "off the shelf" modules permit high volume manufacturing with an outstanding quality level assuring timely delivery at a competitive cost.

Three classes of output modules are available. The **STANDARD** outputs allow short duration surge currents on all auxiliaries for hard starting loads. Optional **CURRENT LIMITED** outputs have square current limiting and feature wireless droop current sharing. Optional **ENHANCED** outputs have square current limiting, one wire star point current share, output good logic signal with LED, nominal 5V local bias, individual inhibit and margining. For requirements that cannot provide minimum load on the main output, the **ZERO PRELOAD** option is available for main outputs up to 500 watts.

DELIVERY

Choose stocked units or construct a model number using stocked modules for fast delivery. Otherwise, form a model from the adjacent page to meet your specific requirements. Contact factory for deliveries on models derived from non-stocked modules.

FEATURES

- 0.99 power factor.
- 5.5 watts per cubic inch.
- 1-7 outputs, 400-1000 watts.
- 120 kilohertz MOSFET design.
- Universal input.
- UL, CSA, TÜV (IEC, EN), CE.
- FCC, EN Class A EMI.
- IEC, EN Immunity.
- All outputs:
  - *Adjustable*
  - *Fully regulated*
  - *Floating*
  - *Overload and short circuit protected*
  - *Overvoltage protected*
- Standard features include:
  - *System inhibit*
  - *Fan output*
- Options and accessories include:
  - *Power fail monitor*
  - *Redundancy*
  - *Current Limited Outputs*
  - *Enhanced Outputs*
  - *Zero Preload*
  - *End fan cover*
  - *Top fan cover*
  - *Rack Assemblies*

STOCKED MODELS - Available in 3 days.

Max Power	Output 1	Output 2	Output 3	Output 4	Model*
400W	5V @ 50A	12V @ 12A	12V @ 12A	5V @ 10A	FT46A2332-45P
400W	5V @ 50A	12V @ 12A	24V @ 6A	12V @ 6A	FT46A2363-45P
600W	5V @ 60A	12V @ 12A	12V @ 12A	5V @ 10A	FT46C2332-13P
600W	5V @ 60A	12V @ 12A	24V @ 6A	12V @ 6A	FT46C2363-13P

**400W models include power fail monitor, current limited modules, zero preload and end fan cover options. 600W models include the same options except fan cooling is built into the unit.*

UNITS FROM STOCKED MODULES - Available in 2 weeks.

FT 44 B 2 3 3 6 - YY X

- FT — Series
- 44 — Configuration
- B — Power Code
- 2 — Output #1 Code
- 3 — Output #2 Code
- 3 — Output #3 Code
- 6 — Output #4 Code
- YY — Sum of Option Codes
- X — Output #1 Variant

Configuration: Allowable quad output configurations are 42, 44, 46 and 48.

Power Code: Choose Power Code A through D for 400-750W models.

Output Codes: Select any outputs from the shaded area on the Output Types table consistent with the configuration chosen.

Option Code: Specify Option Code. Refer to the Option table. Codes 02 (redundancy) and 16 (enhanced) are excluded from models available in 2 weeks. Fan cooling is built into 600 and 750W units.

OPTIONS

Option Code	Function
00	None
01	Power Fail Monitor
02	Redundancy
04	Current Limited
08	Zero Preload
16	Enhanced
32	End Fan Cover
64	Top Fan Cover

Replace the YY with the sum of the Option Codes.

MODEL SELECTION

Models are available in power ratings of 400 to 1000 watts, with corresponding code letters A through E. See Power Code chart.

Output modules are available in six types: J, K, L, M, N and P in nominal power ratings from 75 - 500 watts. Type M, N and P modules are variable power rated depending upon the unit power rating. The M, N and P Module table directly below shows the corresponding multiplier applicable to the output current ratings of the M modules and allowable power ratings for the N and P modules. For example, a 750 watt multiple will have its M type module configured to produce 120A @ 5V or 12A @ 48V. The voltage and current rating of output modules are listed in the table of output types. This table assigns an alpha-numeric code designating the nominal voltage rating of the module.

Power Code	Unit Power Rating	M Module Current Multiplier		N/P Module*
		Single Output	Multiple Output	Allowable Power Rating
A	400W	0.8	0.5	250W
B	500W	1.0	0.6	300W
C	600W	1.2	0.8	400W
D	750W	1.5	1.2	500W
E	1000W	2.0	1.5	750W

**When an N or P module is used as the main output, the allowable power and the module current ratings must not be exceeded.*

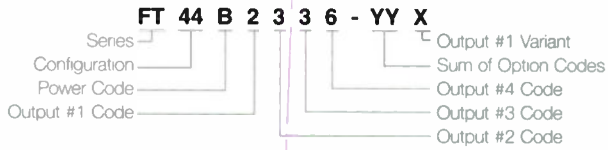
Output Types*						
Output		Module Type				
Code	Volts	J Amps	K Amps	L Amps	M Amps	N/P Amps
0	2	10	20	30	100	60
1	3.3	10	20	30	100	60
2	5	10	20	30	100	60
3	12	6	12	24	42	42
4	15	5	10	20	33	33
5	18	4	8	16	28	28
6	24	3	6	12	21	21
7	28	2.5	5	10	18	18
8	36	2	4	8	14	14
9	48	1.5	3	6	10	10
A	2.2	10	20	30	100	60
B	2.4	10	20	30	100	60
C	2.7	10	20	30	100	60
D	3	10	20	30	100	60
E	3.6	10	20	30	100	60
F	4	10	20	30	100	60
G	4.5	10	20	30	100	60
H	5.7	10	20	30	90	60
J	6.3	10	20	30	80	60
K	7	9	18	30	70	60
L	8	8	16	30	62	60
M	9	8	15	30	56	56
N	10	7	14	30	50	50
P	11	7	13	27	45	45
Q	13.5	6	11	22	37	37
R	17	5	9	18	30	30
S	19	4	8	16	26	26
T	21	4	7	14	24	24
U	23	4	7	13	22	22
V	26	3	6	12	19	19
W	29	3	5	10	17	17
X	32	2	5	9	16	16
Y	40	2	4	8	13	13
Z	44	2	4	7	12	12

Multiple output modules of a given type are arranged in ascending order by voltage magnitude in the same sense as the output number sequence in the configuration diagrams.
**Shaded ratings are stock.*

HOW TO ORDER

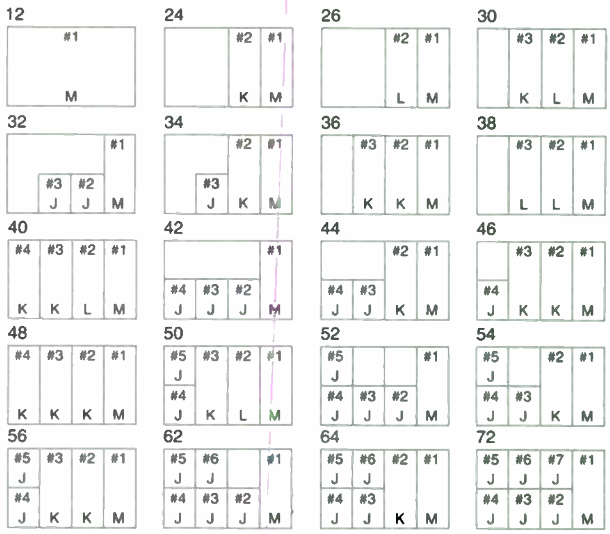
To form the proper model number defining a custom requirement, select the letters FS or FT to designate the series, then choose the desired configuration and list the configuration code. Insert the power code letter for the power level and follow with the output code numbers or letters for each specific output. Enter a dash and from the option table insert the sum of the option codes. Where lower power is desired for the main module, an N module can be substituted and is denoted by a letter N in the output variant position. In addition, when no preload is available for the main output, choose Option Code 08 and add a P in the output variant position. For an enhanced **main** and **current** limited auxiliaries, specify both 04 and 16 option codes.

HARMONIC CORRECTED 500W QUAD SWITCHER



OUTPUT CONFIGURATIONS

The boxes below are diagrammatic representations of the power supplies as viewed from the output end. The two-digit numbers above the boxes are the configuration codes.



Refer to the table below for allowable configurations by series.

Output Config	Unit Power Rating				
	400W	500W	600W	750W	1000W
12	•	•	• x	• x	x
24	•			• x	
26		•	• x	• x	x
30					x
32	•			• x	
34	•	•	• x	• x	
36	•	•	• x	• x	x
38					x
40					x
42	•	•	• x	• x	
44	•	•	• x	• x	x
46		•	• x	• x	x
48			x		x
50					x
52	•	•	• x	• x	x
54		•	• x	• x	x
56			x		x
62		•	• x	• x	x
64			x		x
72			x		x

- • *Represents allowable configurations for the FT Series.*
- x *Represents allowable configurations for the FS Series.*

SPECIFICATIONS

INPUT
90-264 VAC, 47-63 Hz.

POWER FACTOR
0.99 typical.

EMISSIONS
FCC 20780 Part 15/EN 55022, Class A Conducted. EN 61000-3-2, Harmonics. EN 61000-3-3, Voltage Fluctuations.

IMMUNITY
IEC 1000-4-2/EN 61000-4-2, Electrostatic Discharge. IEC 1000-4-3/EN 61000-4-3, Radiated Field. IEC 1000-4-4/EN 61000-4-4, Electrical Fast Transients. IEC 1000-4-5/EN 61000-4-5, Level 3 Surge. IEC 1000-4-6/EN 61000-4-6, Conducted Field.

INPUT SURGE
230 VAC - 38 amps max. 115 VAC - 19 amps max.

EFFICIENCY
75% typical.

HOLDUP TIME
20 milliseconds from loss of AC power.

OUTPUTS
See model selection table. Outputs are trim adjustable ±5%.

OUTPUT POLARITY
All outputs are floating from chassis and each other and can be referenced to each other or ground as required.

LINE REGULATION
Less than ±0.1% or ±5mV for input changes from nominal to min. or max. rated values.

LOAD REGULATION
±0.2% or ±10mV for load changes from 50% to 0% or 100% of max. rated values.

MINIMUM LOAD
Main output requires a 10% minimum load for full output from auxiliaries. Use Option 08 if no minimum load is available for mains up to 500 watts. Singles require no minimum load.

RIPPLE & NOISE
1% or 100 mV, pk.-pk., 20 MHz bandwidth.

OPERATING TEMPERATURE
0-70°C. Derate 2.5%/°C above 50°C.

COOLING
A min. of 10 LFS* for models without internal fans directed over the unit for full rating. Two test locations on chassis rated for max. temperature of 90°C. 600 watt, 750 watt and 1000 watt models have built-in ball bearing fans.
*Linear feet/second.

TEMPERATURE COEFFICIENT
±0.02%/°C.

DYNAMIC RESPONSE
Peak transient less than ±2% or ±200 mV for step load change from 75% to 50% or 100% max. ratings.

RECOVERY TIME
Recovery within 1%. Main output - 200 microseconds. Auxiliary outputs - 500 microseconds.

SAFETY
Units meet UL 1950, CSA 22.2 No. 950, EN 60 950, IEC 950.

ISOLATION
Conforms to safety agency standards.

INPUT UNDERVOLTAGE
Protects against damage for undervoltage operation.

SOFT START
Units have soft start feature to protect critical components.

OVERVOLTAGE PROTECTION
Standard on all outputs.

REVERSE VOLTAGE PROTECTION
All outputs are protected up to load ratings.

OVERLOAD & SHORT CIRCUIT
Outputs protected by duty cycle current foldback circuit with automatic recovery. Standard auxiliaries have additional back-up fuse protection. Options 04 and 16 have square current limiting with automatic recovery when overload is removed.

THERMAL SHUTDOWN
Circuit cuts off supply in case of local over temperature. Units reset automatically when temperature returns to normal.

FAN OUTPUT
Nominal 12 VDC @ 12 watts maximum.

INHIBIT
TTL compatible system inhibit provided. Option 16 has individual output inhibit.

REMOTE SENSING
On all outputs except standard and 04 Option outputs 75 watts or less.

SHOCK & VIBRATION
Shock per MIL-STD 810-E Method 516.4, Procedure I.
Vibration per MIL-STD 810-E Method 514.4, Category 1, Procedure I.

MECHANICAL

CASE	SERIES	WATTS	H	x	W	x	L
1	FT	400W/500W	2.50"	x	4.93"	x	8.00"
3	FT	600W	2.56"	x	5.08"	x	10.03"
4	FS	600W	2.56"	x	5.08"	x	11.00"
5	FT	750W	2.63"	x	5.20"	x	10.03"
6	FS	750W	2.63"	x	5.20"	x	11.63"
7	FS	1000W	2.56"	x	7.13"	x	11.63"

OPTIONS

POWER FAIL MONITOR
Optional circuit provides isolated TTL and VME/VXI compatible ACFAIL signal providing 4 milliseconds warning before main output drops by 5% after an input failure. A SYSRESET signal following VME timing requirements is provided when an N module is used as a main output. Both logic signal outputs can sink current per the VME specification.

REDUNDANCY
Optional Or-ing diodes for hot pluggable N+1 redundant operation. For FT Series 500 watt & 750 watt models with 1-4 outputs. Main output current limited to 100 amps. Remaining outputs 16 amps max.

CURRENT LIMIT
Option provides on all outputs:
- Square current limit with auto recovery.
- Wireless droop current share for parallel or N+1 redundant operation.

ZERO PRELOAD
Optional circuit removes need for preload on main output up to 500 watts.

ENHANCED
Option provides on all outputs:
- Square current limit with auto recovery.
- Single wire active current share for parallel or N+1 redundant operation.
- DC output good logic signal with LED indicator.
- Logic inhibit.
- Nominal 5V bias.
- Margining.

END FAN COVER
Optional cover with brushless DC ball bearing end fan which provides the required air flow for full rating.

TOP FAN COVER
Same as above with fan cover mounted on top of the power supply.

ACCESSORIES
RA50 and RA75 Series 2U high rack assemblies provide hot pluggable interface and hold up to 3 FT Series 500 watt or 750 watt units respectively.

Specifications subject to change without notice.

Deltron inc. POWER PRODUCTS
290 WISSAHICKON AVENUE, P.O. BOX 1369, NORTH WALES, PA 19454
PHONE: 215-699-9261 • FAX: 215-699-2310 • TOLL FREE: 1-800-523-2332
E-MAIL: sales@deltroninc.com • VISIT OUR WEB SITE: www.deltroninc.com

Standards And Specs For In-Seat Power On Aircraft Still In The Clouds

You May Now Have A Chance To Assist In Deciding How Airlines Will Supply In-Flight Power To Laptops And Other Passenger Electronics.

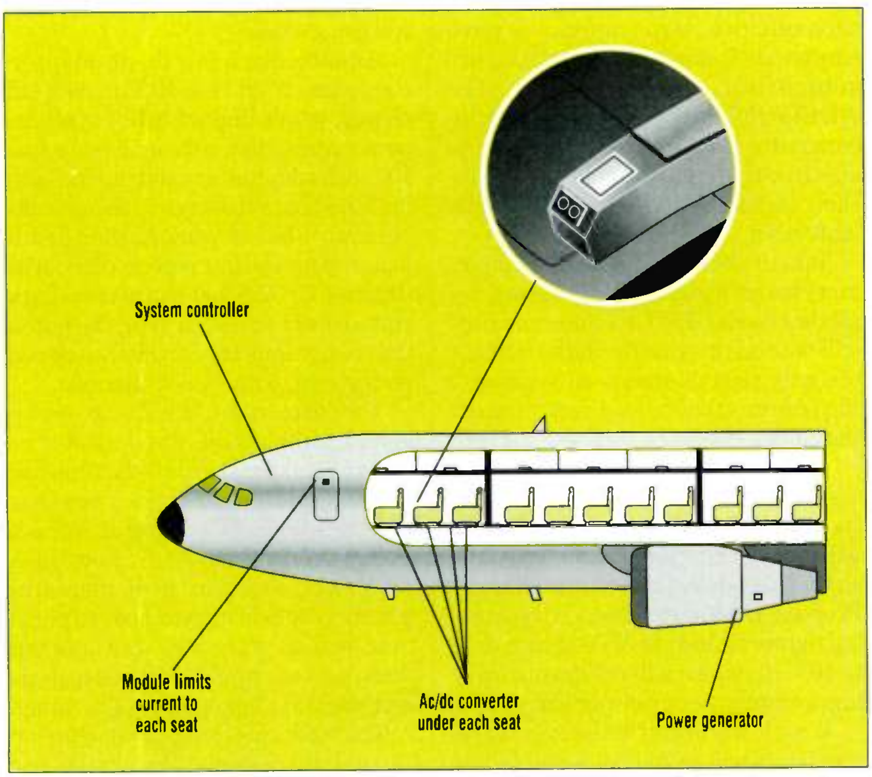
PATRICK H. POTEGA, Passenger Electronic Device Association (PEDA), 6320 Canoga Ave., Woodland Hills, CA 91367; (818) 887-3123; fax (818) 883-5706.

The face of mobile computing is changing. Freedom from having to carry multiple battery packs while flying with a laptop, in particular, is close to becoming a reality. In the next few years, a handful of airlines, most notably Delta and American, will be outfitting selected aircraft with power ports in first class and business class seats.

However, as with any new technology, a few kinks have to be worked out. Surprisingly, in such a highly regulated industry like commercial aviation, the specs for in-seat power have yet to be defined, even after two years of beta testing. Furthermore, it appears that the specs are actually happening after the fact, and that they are being drafted using the installed base of product as "justification" of how things should be in the future. This has the flavor of some "reverse-engineering" of the spec. Sound engineering, and often common sense, are being put aside in favor of keeping one or two airlines happy.

While select airlines are constantly rolling out new planes with an In-Seat Power Supply System (ISPSS) that was the only product offering in the aviation marketplace a year ago, the Airlines Electronic Engineering Committee (AEEC) is just now setting an output voltage standard for that power port. Other power system vendors have stepped forward and proposed changing the existing 15-V dc system to a range of 11 to 16 V, or even moving the aircraft-standard voltage out of the SAE car-voltage range.

Surprisingly, even though the in-flight power system was supposedly designed with the road warrior in mind, and is advertised as laptop-traveler friendly, the specification issues don't appear to reference how laptops work, and at what voltages. Instead, the AEEC's Cabin Equipment Interfaces (CEI) Subcommittee is approaching the ARINC Specification 628, Part 2, as an exercise as to whether or not an aircraft power system at the seat should look like or mimic a cigarette lighter in an automobile.



1. In-flight power is provided to passenger's computers via a connector on their seat armrest. The system controller is responsible for managing and distributing the limited amount of power produced by the jet engine's integral generators.

A Typical Installation

A typical aircraft ISPSS installation (like those identified as Proposals "B" and "C" in Table 1) is relatively straightforward. Illustrated is an overview of the system components

(Fig. 1). The engine-driven generator provides electrical power to the entire aircraft. A segment of the airplane's total electrically generated power is allocated to the ISPSS. The Federal Aviation Administration (FAA) mandates that 100 W per passenger seat is the allowable maximum. Some older aircraft types were not designed for today's power-hungry devices in the passenger cabin, so there are airframes that have load schedules that may deliver less than 100 W to each ISPSS as input.

The 400-Hz, 115-V ac power from the generator's bus is controlled by a load-limit module that restricts the allowable current the ISPSS has available. This current-restrictor governs the total power allocation to all passenger seats. One reason why airlines are installing power ports only in first and business class seats is because there simply isn't enough power on the bus to support more than 100 to 120 seats with laptop power ports simultaneously.

A system controller, accessible by the cabin or flight crews, is used to manage power distribution to each seat. In every seat, there is an ac-dc converter that outputs 15 V dc to the power ports. The armrest usually has two electrical receptacles, one for each passenger.

These under-the-seat power supplies are constantly in standby mode. When a passenger plugs in a laptop, two of the four power pins in the AEEC-approved Hypertronics D-series connector short to indicate it is in-use, and the power supply wakes up *(Fig. 2)*. A small LED indicates that power is available.

The passenger accesses the aircraft power system with a dc-dc adapter. This adapter converts the 15-V dc output of the seat's power port to the laptop's input voltage. Some airlines are opting for a loaner program, and are providing passengers with a limited selection of power adapters. Most airlines require passengers to provide the correct dc-dc converter.

Power management is rather rudimentary. The system controller monitors the seat-by-seat utilization of the power ports. As more passengers "plug in," the manufacturer's pre-set limit of 90% utilization is reached, and all seat ports not in use are disabled. It is difficult to calculate how many laptops any aircraft will actually accommodate. Even though the airplane features 120 power ports, a smaller group of high-powered (60 W, or more) ports could max out the system before all the plugs are used. Since the system may lock out any laptops on standby or sleep mode, airlines may find themselves dealing with unhappy passengers who are competing with one another for the power system's attention.

TABLE 1: PROPOSED ISPS SYSTEM SPECIFICATIONS

Features	Proposal "A"	Proposal "B"	Proposal "C"
Output voltage	Auto-configures to any 3-24 VDC output voltage	13 VDC +/-2	15 VDC +/-1
Max available power	93 Watts (FAA maximum = 100W)	75 Watts	75 Watts
PFC (Power Factor Correction)	1.0	1.0	.8
Power management	APM-style	Limited (On/Off only)	Limited (On/Off only)
"Black-out"/Fault protection	Yes	No	No
Adapter required	No	Yes (Third-party)	Yes (Third-party)
In-seat connectors supported	None required (optional Hypertronics available)	Hypertronics and car adapter	Hypertronics and car adapter
Allows battery charging	No	Yes (No disable)	Yes (No disable)

Now There Are Three

While the airlines have not had much choice of vendors who supply ISPSS technologies, two companies have thrown their hat into the ring and are submitting proposals to the AEEC/CEI Subcommittee. This subcommittee is charged with writing the specifications and standards for anything electrical or electronic in the aircraft cabin.

Table 1 also depicts the most important characteristics of the three proposals that the AEEC/CEI Subcommittee will vote on this month. In the interest of clarity, the table has been confined to the features that most directly impact the laptop.

Systems B and C are so similar that they will be considered here as one in the same. The only differentiator that will impact the specification is a subtle shift in the power port's output voltage. Proposal B wants to broaden the existing tightly defined 15-V dc output to 11 to 16 V dc, which will not dramatically impact laptop design or performance.

What it will impact is the overall system performance and power utilization of the aircraft's power grid. The present power delivery system is load-limited at the main bus to 100 W (or less) per seat. As suggested, over time, this may impact the number of users who can access power. By lowering the voltage, from 15 to 11 V, there will be a decrease in system performance. This will be created by an increase in dc-dc conversion inefficiencies, as the intermediate dc-dc adapters boost to the higher voltages (18 to 20 V dc) required by many notebook computers. Power losses by boosting to 19 V dc, from a base reference of 11 V, rather than from the present 15 V, will exact a toll.

Admittedly, a few dc-dc adapters converting from 11 to 19 V, at 80% efficiency, won't impact cabin systems' power utilization. But, with more than 100 such adapters running inefficiently for 4 to 5 hours at a stretch, the aircraft's generator has to work harder just to make up for the lost power. With an estimated 178,320,000 hours of in-flight laptop operation each year, the potential energy impact of an inefficient converter design can be considerable.

The adapters are fall into two classes here. The automobile dc-dc adapter is a generic, inexpensive unit that one may find at an auto-parts store. These low-cost units typically operate at 70% efficiency at loads below 1 A. Above 1 A, the power losses are even more dramatic, so 70% is more a best expectation, instead of the 50% or worse that these devices would experience in the real world at a laptop's 2- to 4-A rating.

The other class of dc-dc adapters are supposedly designed for aviation use. These are more power-friendly, as a group, but not all of the five manufacturers of these devices are created

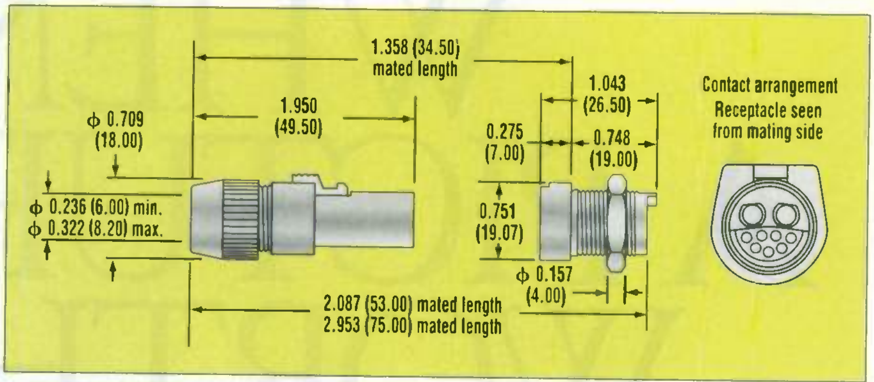
equal. The efficiency profiles of the three systems under consideration are shown *(Table 2)*. We have seen "airline-standard" adapters with a total power limited to 20 W, so the corresponding chart may be optimistic for specific models and brands.

The chart represents a typical power system, and the baseline for available wattage is the FAA-mandated, 100-W maximum per seat. Systems B and C suffer from not only very low inherent conversion efficiencies (75 to 80%), but also the downstream losses created by connector losses of 2 to 5% (more on this later). The connector loss reduces that 100 W to 71 W, then the intermediate dc-dc adapter relinquishes another 15 to 30% of the available power to each seat.

System A has a definite edge in the power-efficiency arena. By avoiding voltage losses across inadequate car connectors, and by not using secondary adapters, the maximum 93 W from the power bus is passed on to the laptop. How does this happen?

All commercial aircraft have two "standardized" voltages throughout the cabin. There is a 110-V ac service available, as well as 28 V dc for lighting and other low-voltage cabin applications. So why wasn't the in-seat power established at the same 28-V dc standard? It seems absurd to pay the huge efficiency penalty of boosting from today's 15 V dc at the passenger seat. An Apple PowerBook at 24 V dc, for example, could almost operate at 28 V dc without any external adapter, since its supply has a voltage tolerance of 2 volts

Since it is always converting downward in voltage, System A uses the aircraft's 28-V system to optimize its power efficiency. The benefit is that it automatically configures itself to match



2. Mechanical details of the Hypertronics connector that has been approved for delivering in-flight power.

the required input voltage of the "Personal Electronic Device" (PED, the term used in the aviation industry for any passenger-provided electrical or electronic equipment). The range of its output voltages also is important. Because the system can deliver power at levels in the 3- to 10-V range, this technology can fine-tune itself to power a PDA/HCE, in increments of .375 V.

Let's turn to other system features that are depicted in Table 1. PFC (Power Factor Correction) is quite good with Systems A and B, but System C is only a moderate performer with a PFC of 0.8. A more significant differentiator that notebook system engineers and designers should be aware of is the power management capabilities of the three contenders. System A uses an APM-style power management technology, so that the power at each seat on the plane is optimized at all times. Power-hungry PEDs and low-current-drain passenger equipment are distinguished by system A. This solves the dilemma of having to restrict the number of seats that can have active power ports at any time, as well as the total number of power ports on the aircraft. This allows those who travel coach class on aircraft equipped with System A to have the same opportunity to access the power system as those in first and business classes.

Systems B and C don't really have any power management, since both technologies employ a strictly "GO/NO-GO" approach. As seen in System C, when the load schedule exceeds 90% of the pre-determined capacity of the generator's bus, power is simply withdrawn from any inactive seats. To avoid this "use-it-or-lose-it" scenario, some savvy passengers will probably learn to set their notebooks in a continuous-loop diagnostics mode, and let the laptop sit there and do endless HDD read-writes when not in use. Even manually disabling any of the laptop's APM features during flight will guarantee that the notebook doesn't go into a sleep or standby mode, which the ISPSS could incorrectly identify as an inactive port.

One can imagine the consequences of having a laptop booted and with multiple apps open, only to have the power plug pulled. In this situation, the notebook's internal battery may or may not save the

TABLE 2: SYSTEM EFFICIENCY COMPARISON

Proposed system	ISPS Power Conversion Efficiency	Power Output (Max Watts)	Car Connector Loss[3]	Power Available To Adapter	Car DC/DC Adapter Efficiency[4]	Aviation DC/DC Adapter Efficiency[5]	Power Available To Laptop
"A"	90-93%[1]	93	N/A	N/A	N/A	N/A	90-93 Watts
"B"	75%	75	2-5%	71	70%	80-85%	50/56 Watts
"C"	75%	75[2]	2-5%	71	70%	80-85%	50/56 Watts

[1] System A's efficiency can increase to about 95%, if its APM (Advanced Power Management) feature is enabled.
[2] System C features a load-limit select module, which pre-sets how much current a particular aircraft's electrical system can sustain. On some aircraft, there may be less than 75 Watts available, since the individual airline can dictate the power resources.
[3] Variants in connector loss relate to the integrity of the mechanical contacts of a car adapter plug. Age, number of insertion cycles, quality of materials, etc., all impact voltage loss.
[4] Car adapters are primarily designed for low-power applications, such as cellular phones or to operate a portable audio CD player. Above 1 amp, their 70% efficiency degrades quickly, up to their maximum current rating of 3 amps.
[5] Aviation adapters are supposedly custom-designed to meet the power requirements of mobile computing, yet some of these adabpter are rated at only 20 Watts.

day. We'll also discuss some reasons why there may not even be a battery in the laptop while it's on a commercial airliner. The power management of System C goes even deeper into areas of notebook-user risk. Quoting from the specifications of System C: "Should the passenger connect to the system and exceed the system capability or cause a fault condition, the output of the socket will be automatically disabled." The description of this power management approach is best expressed as "ON/OFF only" in our comparison chart *(Table 1, again)*.

Food For Engineering Thought

There are several situations that can trip the "kill switch" in Systems B and C. One is to have the laptop up and running, then insert a power-hungry PC Card, or an external peripheral, such as a CD-ROM drive. Power system engineers and laptop designers should pay careful attention to "worst-case" scenarios for total-system loads.

According to the specifications, any combination of hardware devices creating power demands that extend into the 50- to 55-W range can potentially trigger a shut-down in the ISPSS under the seat *(Table 2)*. In Table 1, we have a line identified as "black-out" protection, which indicates a situation which few mobile computer system engineers have thought about—having the external power source go unexpectedly offline. Don't assume that the laptop's battery will be there as a life preserver. The passenger may very likely be boarding a plane after a long, battery-draining session of computer work in the waiting area of the airport.

Based on the picture of limited power in Table 2, with nonexistent power management and no fault-tolerant capabilities to protect the notebook (especially its data and OS), here are some suggested approaches to "airline-proof" your notebooks:

1. Consider setting your battery's drop-out threshold voltage high enough to allow a "reserve" for emergencies, such as the ISPSS unexpectedly turning off, either in its fault-tolerant mode, or simply by not recognizing the laptop's power management when the equipment is in a sleep mode (which could be mistaken for an inactive seat port). Also, the audible prompt associated with low-battery states is almost impossible to hear over the high level of ambient noise on an airplane, unless you crank up the volume on the speakers for such alarms.

2. Ironically, your software and/or hardware power management technologies may be inappropriate for airline use where Systems B or C are in place. As noted, if your laptop does too good a job of conserving power, the associated risk is that the ISPSS designs of Systems B and C could be fooled into thinking that the local seat power supply unit is in its "ON-but-not-in-use" mode. Think about having a user-selectable "Airline Travel" mode for power management. This might include leaving high-current-drain devices like the screen's backlight on. Perhaps there should also be a utility which keeps the hard drive or floppy motors duty cycling.

3. If you do your own modified version of an OS, give serious consideration to a solid data-recovery mode. Windows NT, for example, usually puts you back to the same place after a power failure, while Windows 95 doesn't always allow such an elegant recovery.

If System A becomes the official standard for the airline industry, we can all breathe a little easier. Its power management actually enhances the energy-saving features in today's laptops, and it has fault-tolerant modes that eliminate any risk of a "black-out" at any time during the flight.

Adapters and Connectors

As seen in Table 2, intermediate dc-dc adapters have a definite negative impact on the total available wattage to the laptop. Of the five adapter vendors coming into the marketplace, their average power efficiency falls in the 80 to 85% range (that's being generous). So, if a typical adapter is used, the available wattage to the laptop's power-in port is a miserly 50 to 56 W. Connect one of today's "bells and whistles" multimedia machines to a power-limited adapter, and there's going to be an unhappy passenger. The dc-dc adapters that have overload protection usually rely only on resettable (or replaceable) fuses.

While Intel has proposed initiatives to the laptop industry to voluntarily limit the power consumption of notebooks to 25 W by 1999 (and that battery packs provide 44 W of power), the real-world trend seems to be going in the opposite direction. In 1994, notebooks averaged about 12 to 20 W, and that doubled in the last three years. Driven by "fat" software code, and consumer demand for desktop performance (especially in video and audio), it is anticipated that the average power consumption of notebooks in the 1998-1999 time frame will consistently be in the 50- to 70-W range. There are already laptops in today's marketplace that operate at well above 70 W.

In light of this, it appears that these secondary adapters are antithetical to continued laptop development because they severely restrict the available power to the equipment, while their inefficiency generates noticable heat.

On the Hot Seat

With all the problems associated with upconversion, you might ask: "What if the adapter were an inverter, and the output to the PED was 110 V ac?" What a neat idea it seemed when Toshiba and one or two other laptop manufacturers did away with the ac-dc "brick" by embedding it right in the notebook. In the office, at home, or in the car, there are no real safety concerns with a mobile computer that requires only an ac tape recorder cord as a power interface. But, at 30,000 feet, who wants an inverter's hot ac cord in one's lap, just as the person in the next seat spills a drink on you?

Another uncomfortable point to consider is that the use of nonmanufacturer-authorized power devices could harm a laptop's internal circuitry, and possibly cause data corruption or loss. Equally troubling for the passenger, it may void the product's warranty.

TABLE 3: DIAMETER OF RECEPTACLE AND LIGHTER PLUG

Volts	Inside Diameter, B, mm	Plug Body Diameter, mm
6	21.34 to 21.46	21.08 to 21.23
12	20.93 to 21.01[a]	20.73 to 20.88
12	21.41 to 21.51[b]	21.13 to 21.23

[a] Receptacles providing bimetal finger contact to the outer periphery of the heating element cup.
[b] Receptacles providing bimetal finger contact to the inner periphery of the heating element cup.

Table 1 indicates two connector variants. The Hypertronics connector is a DIN-style connector that is specific to airline power ports *(Fig. 2, again)*. It's well-engineered mechanically and electrically, and has been used in medical applications for 14 years. The AEEC has endorsed and approved it as the official in-seat power port interface.

Unfortunately, marketing-department thinking has influenced the AEEC, when a standard car adapter was proposed last year as an acceptable alternative to the Hypertronics connector. Why? Because the aviation-based companies who were out selling in-seat power were promoting a system that offered passengers the convenience of a power port connector that was interchangeable with a passenger car's.

Connector companies, as well as car and aircraft adapter manufacturers, have not cast any thumbs-up votes for the automotive-style connector. Mechanically, it's an inelegant, unsophisticated affair. Despite their shortcomings, the AEEC Subcommittee was informed that, even though it had (on two occasions) voted against the car adapter interface, the car connector would still be part of the specification.

Not until the "electronic age" did the simple car cigarette-lighter receptacle have any "high-tech" application. As a matter of fact, the SAE Spec J563 still officially describes the receptacle as a "cigar lighter," which tells its age and original application.

SAE J563, in part, inadvertently fosters some of the mechanical instability of the plugs that fit into the specified dashboard receptacle. The SAE's dimensional specification for the "Cigar Lighter" is shown *(Table 3)*.

The specification stipulates that any male plug manufactured as the "A" variant of the 12-V receptacle (20.93-21.01 mm) is not going to fit snugly in the "B" variant of the 12-V female receptacle (21.41-21.51 mm). At least one manufacturer of car adapters makes a small sleeve that decreases the I.D. of the "B"-size receptacles. Without this sleeve, this company's "A"-size male plugs tend to go askew and short out in a "B"-size receptacle. The "A"-size receptacles have been popular in U.S.-manufactured cars, while European cars typically have the larger-orifice "B"-size receptacles.

U.S. passenger vehicles are now coming on the market with two receptacles. There's the smaller "A"-sized, 12-V receptacle, with the classic heating element for smokers, and the second outlet is the larger "Euro-style" "B" variant. Electrically, these car plugs are prone to shorts and contact failures, and they often have significant voltage drops across the connector when there is not a very snug mechanical fit, as has been indicated by the 2 to 5% connector-related power loss *(Table 2, again)*.

The SAE standard allows a maximum current of 8.0 A, which is well above the 2.5 to 4 A typical of notebook computers. Unfortunately, some "gray market" adapters that have voltages in the laptop range are designed for light-duty 500- to 700-mA range applications, such as cellular phones and other car accessories (personal CD-players, etc.). Put one of these low-power adapters between a 15-V-dc, 5-A in-seat power port and a high-powered laptop drawing 50 to 75 W and you can expect sparks to fly. In a $16 adapter you'll be lucky to find even a fuse for protection. These are some of the reasons why the AEEC voted down the car connector—twice.

Proposal "A" in Table 1 shows some promise for resolving many issues, including the connector. The car connector dilemma disappears with this system. Everything the passenger needs to interface with the in-seat power system is already on the plane. There is a Hypertronics connector available as an option, and that is only to allow airlines who have existing hardware at the seat to still use those power ports, but they are strictly alternate power outlets. Only a straight-through power cord is required when a Hypertronics receptacle is used.

About The Pending Vote

Anyone can go to an auto-parts or RV equipment store and purchase an inexpensive, noncertified, dc-dc (or dc-ac) adapter. What budget-minded road warrior wouldn't be tempted by a $16 gray-market car adapter, instead of the $89 to $129 "aircraft" adapters? The AEEC, the airlines, and the cabin crew are all powerless to prevent just that. The present specs may even invite it.

What has driven this 15-V standard, and the newly proposed 11- to 16-V spec, is a misdirected marketing opportunity. The message to the passengers from the airlines (and some factions of the AEEC rules-making committee), is that the power port should be the same interface as that of a car. What any engineer should see as too much of a temptation for laptop users to court potential electrical disaster, is seen by airline marketing as "passenger convenience."

In-Flight Safety For Batteries

While Table 1 lists a variety of system features, the AEEC vote will only focus on the first two items—system output voltage and the connector. But one of the three competing companies (proposal "A") is reflecting the concerns of the mobile computing industry by presenting a proposal to eliminate battery charging on aircraft.

To add to laptop maker's concerns, the Department of Transportation (DOT) is looking into battery safety on aircraft. Various sources have indicated that recent DOT meetings are focused on battery safety not as a matter of whether to charge or not, but whether or not potentially toxic battery materials should be allowed on aircraft at all.

Passenger exposure to battery venting, or heavy-metals contamination of the cabin interior may place severe restrictions on our laptop customers' rights to bring batteries onto an airplane. If the mere presence of batteries at 30,000 feet becomes illegal, the whole issue of charging becomes a moot point.

If the DOT's final resolution is one of "better safe than sorry," and batteries are banned on aircraft, the need for an optimized and sophisticated on-board power source becomes even more critical to the mobile computing passenger. If laptops can only fly without a battery pack, then the integrity and advanced features of a well-thought-out ISPSS will be the only safety net available to laptop users.

As an engineer in the mobile computer industry, it might be wise to not commit to any design or development which may be impacted by the in-flight power programs. Right now, everything is up in the air (pardon the pun), so what you may be considering as appropriate for your equipment to be "compliant" with any airline initiatives relating to voltages and/or connectors is probably based on premature and potentially inaccurate information.

The three proposals before the AEEC/CEI Subcommittee will, in a significant way, shape the future of mobile computing travel. Right now, there

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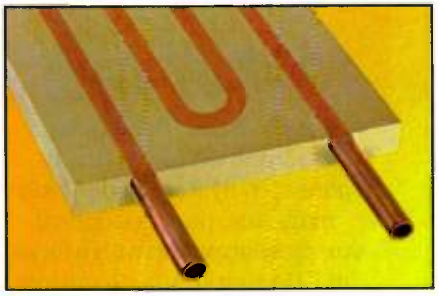

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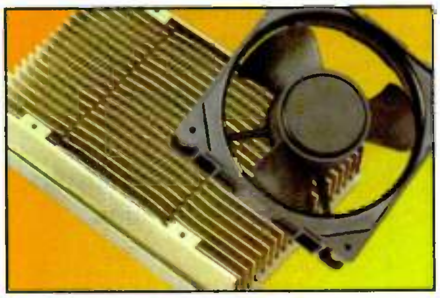

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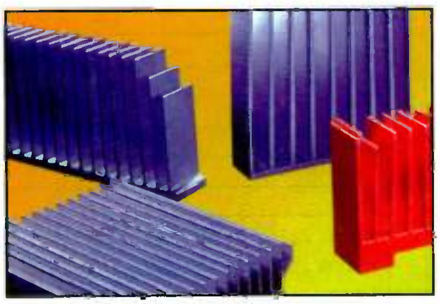

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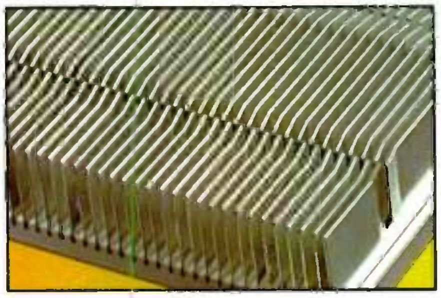

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is no guarantee that 15 V dc is the approved or even recommended voltage for the in-seat power port. It could wind up being 20 V, 18 V , 12 V, or other voltages within the "normal" laptop range, or it may be 28 V.

Your Opinion Counts

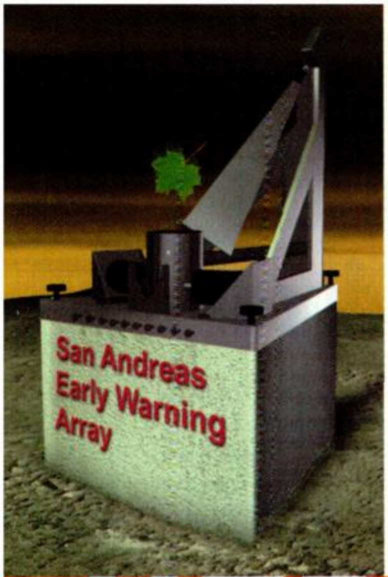
The laptop industry didn't get much of a chance to vote on the ISPSS technologies that are already in place. You however, still have a chance to voice your opinion about the next generation of systems.

This month, the AEEC committee will be voting on the voltage and connector issues. The day before the official vote, attendees of the Portable By Design Conference, in Santa Clara, Calif., will have the opportunity to participate in a "straw poll" on the same issues. To be held Wednesday, Feb. 11, between 2:00 and 5:00 p.m. at the battery-management session, your inputs will be hand-carried to the AEEC meeting for review. *Electronic Design* will report on the outcome of the vote.

A working group within the AEEC/CEI Subcommittee has spent some three months gathering information from a variety of sources, including the laptop manufacturers. This fact-finding task force has put all of its research into a white paper, which has been distributed to the AEEC/CEI membership weeks prior to the Feb. 10-12 voting session. Copies of the white paper are available to any interested parties. To receive a copy, contact the Passenger Electronic Device Association (PEDA), 6320 Canoga Ave., Woodland Hills, CA 91367; (818) 887-3123; fax: (818) 883-5706).

PEDA was founded in response to the ongoing airline activities which involve mobile computing, so that there is a unified body of representatives from the notebook manufacturing sector, the battery industry, the adapter vendors, and other related PED industry segments.

Patrick H. Potega is the acting director of PEDA (the Passenger Electronic Device Association), a group of battery vendors, laptop manufacturers, dc-dc adapter providers, and other interested parties. Through PEDA, they work together to represent the interests and needs of the mobile computing community to the commercial aviation industry.



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Self-Programming Microcontroller Networks Sensors And Transducers

Single Chip Performs Signal Conditioning, Data Conversion, And Control Functions For Data-Acquisition Systems.

Milt Leonard

Designing networked control systems with various types of sensors and transducers in space- and cost-constrained industrial control applications involves dealing with complex relationships between interface circuits, signal-conditioning and conversion circuits. In addition, one also must consider the problems associated with calibration, linearization, and communications. Equally challenging is the use of nonvolatile memory as a transducer electronic data sheet (TEDS). These issues are addressed by the IEEE 1451.2 standard that defines a standard interface and communication protocol for transducers and sensors in measurement and control systems.

Existing microcontrollers fall short of fully implementing the standard in silicon, either because of limited functionality or prohibitive cost. For example, the standard transducer interface module (STIM) portion of the standard specifies the sensor interface electronics, signal conditioning, data conversion, calibration, linearization, basic communication capability, and a nonvolatile 565-byte TEDS. Some microcontrollers with integrated 8- or 10-bit analog-to-digital converters (ADCs) or comparator-based slope conversion can implement most of the STIM functionality, but are limited in conversion speed and accuracy. Moreover, few available controllers have economically integrated analog conversion together with high-density EEPROM because of the additional process complexity requirements of both functions.

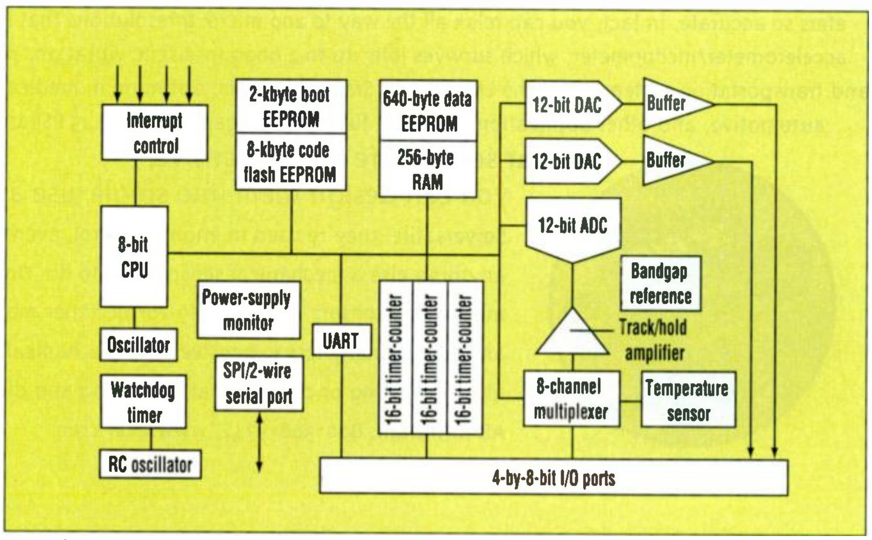
These limitations are overcome by the ADuC812 MicroConverter from Analog Devices, which integrates the key STIM elements with 12-bit, 5-µs data conversion on a single chip for high-accuracy, fast-conversion-time applications such as battery monitoring, pressure and temperature measurement, gas monitoring, and leak detection. In a typical application, the ADuC812 conditions and converts signals from various types of sensors, sends signals to actuators and display devices, and communicates with the host microprocessor over signal and control lines.

The ADuC812 microcontroller consists of an 8-bit 8052 CPU, four 8-bit I/O ports, 256-byte SRAM, seven interrupts, power-supply monitor, watchdog timer, and two serial ports *(Fig. 1)*. Also on the chip are an RC oscillator, two 12-bit digital-to-analog converters (DACs), a 12-bit self-calibrating ADC, three-16-bit timer-counters, an 8-channel multiplexer, a UART, temperature sensor, a bandgap reference, and 10.5 kbytes of EEPROM. Maximum operating frequency is 16 MHz for 1.3-MIPS performance.

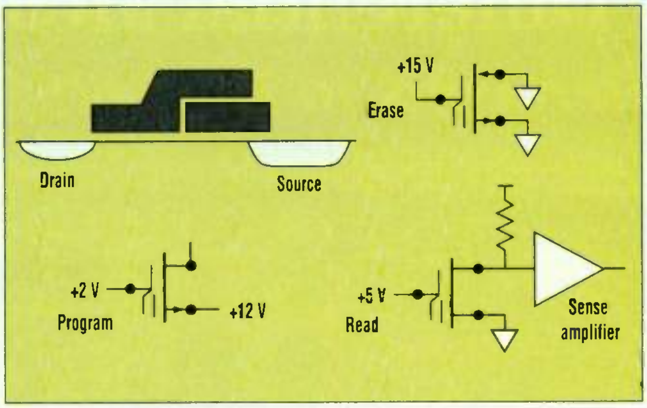
The 5.0-by-5.5-mm chip with embedded EEPROM is fabricated on a 0.6-µm CMOS, 2-metal process and operates from a 2.7- to 5.5-V single supply. At 5 V, the chip draws 12 and 5.5 mA in normal and idle modes, respectively. At 3 V, it draws 8 and 3 mA, respectively. Powerdown current is less than 1 µA. Low power consumption and a small footprint enable 4- to 20-mA loop-powered smart-transducer applications and comounting of the STIM and transducer.

DAC Innovations

A new technique is used in the DACs to get less than 1-LSB differential nonlinearity (DNL), less than 4-LSB integral nonlinearity (INL) and ±2-LSB accuracy in a small area. This allows the integration of two DACs and eliminates the need to tie up valuable timer/counters for more traditional pulse-width modulated (PWM) analog outputs. The DACs use a multiplying-string architecture with buffered voltage outputs and polysilicon resistors, with a main DAC of 64 resistors (6 MSBs) and a sub-DAC (6 LSBs). Settling time is 4 µs. Other string



1. Analog Devices' ADuC812 MicroConverter is a mixed-signal device with a digital section comprised of an 8052 CPU core, flash memory arrays and RAM. The analog section includes two DACs and an 8-channel ADC. For reprogramming, a serial downloader in the bootstrap EEPROM receives new code over the UART serial port and begins the reprogramming sequence.



2. The split-gate EEPROM cell used in Analog Devices' ADuC812 is programmed by channel hot-electron injection from the source and erased by Fowler-Nordheim tunneling between the floating-gate polysilicon and control-gate polysilicon. Fabrication requires just three extra masks over standard CMOS processing.

DACs use area- and power-consuming buffers between the main and sub-DAC to eliminate loading errors, which become significant at higher resolutions. The ADuC812's DAC eliminates these buffers by including this step error in the DAC transfer function. Conversion time is 10 µs.

The ADC is a successive-approximation-register (SAR) type. Its 12-bit charge-redistribution DAC consists of an MSB array of eight binary-weighted capacitors and a 4-bit LSB array. Each of the eight bits in the main array are calibrated by adjusting the value of its capacitor with a binary-weighted capacitor trim array. Offset and gain capacitors also can be calibrated. ADC calibration coefficients default to 12-bit-accurate factory numbers which are preloaded in registers by the microcontroller during the execution of a power-up loader held in bootstrap memory. If required, these numbers can be overridden by a software in-situ calibration, allowing the user to null out ADC errors as well as system errors such as transducer offset. INL and DNL are under 1 LSB and conversion time is 5 µs.

The input multiplexer accepts up to eight analog inputs. A ninth channel selects the on-chip temperature sensor which generates a voltage derived from the on-chip bandgap reference.

Older microcontrollers lacking EEPROM use polysilicon resistor strings as the core ADC element for typical 8-bit accuracy. Those quoting a programmable ADC resolution of 14 or 16 bits typically integrate an on-chip comparator and rely on the user to use high-accuracy external resistors and capacitors to implement a dual-slope converter. However, the cost of these components can exceed that of the controller IC.

Furthermore, with conversion times in the millisecond range for resolutions higher than 10 or 12 bits, these slope converters are too slow for the requirements of high-speed applications. Twelve-bit ADCs with EPROM calibration require large cells for sufficient coupling ratios for programming and are usually one-time programmable. A further limitation is that user in-situ calibration on a system level is not possible.

Another key to reaching the high level of integration is the use of a low-complexity, split-gate EEPROM cell design for nonvolatile memory *(Fig. 2)*. Using polysilicon-polysilicon erasure eliminates the need for more complex tunnel-oxide processing required for erasure in other EEPROM technologies. The result is a simple modular addition to a standard CMOS process.

This process module consists of a second gate oxide, a floating gate, and three additional implant masks for the 15- and 20-V devices in the charge pump and high-voltage switches. By comparison, other nonvolatile memories typically involve six or seven extra masking steps over CMOS for the memory cells, polysilicon-polysilicon capacitors, thin-film resistors, or special process additions for the ADC. Since both program and erasure are self-limiting on the ADuC812, there's no need for complicated control logic to prevent over-erasure as required in other nonvolatile memories.

With an endurance rating of 10,000 erase/programming cycles and data retention specified in multiples of 10 years, the EEPROM is partitioned into three sections. The 640-byte TEDS data memory is a 320-by-16-bit flash EEPROM array for general scratchpad use. Its erase sector size of 32 bits or 4 bytes facilitates software data manipulation. It also increases endurance since each byte experiences just one disturbance due to the programming of a neighboring byte on the same row. Sector size in the main 8-kbyte flash EEPROM array is 64 bytes. This memory only holds program code and is programmed with standard memory programmers or by in-circuit programming.

Self-programming in the ADuC812 is implemented with the bootstrap memory, which is an additional 2-kbyte EEPROM containing functions such as power-up initialization, serial downloader, on-chip emulator, and manufacturers' ID and calibration coefficients for sensors and transducers. The serial downloader accepts new program hex code over the UART serial port, starts up the charge pumps, erases the 8-kbyte code memory area, and then programs the new code.

Conversely, most other microcontrollers with in-situ programming capability require the chip to be slaved to a second microcontroller or need a hard-coded boot ROM loader. Furthermore, most current emulation schemes use hardware breakpoints involving area-consuming registers and address comparator designs, and require external clips or pods.

In-situ self-programming and calibration with nulling of transducer offset and gain errors provide valuable new capability for code upgrades and transducer recalibration in remote or inaccessible locations. Self-programming also is used in on-chip emulation to program break points (jump-to-emulation instruction) into the code memory—that is, software breakpoints with no hardware overhead. This further enables in-situ full-speed emulation without needing external clips or pods, which is of special benefit to users debugging hardware-software analog-accuracy problems on target boards.

The ADuC812 MicroConverter is supported by a development system that includes documentation, applications board, plug power supply, serial port cable, and software. Provided on a 3.5-in. floppy disk, the software consists of an assembler, simulator, debugger, serial downloader and example code.

PRICE AND AVAILABILITY

Packaged in a 44-pin PLCC or 52-pin PQFP, the ADuC812 MicroConverter is priced at under $10 each in OEM quantities. Production quantities will be available in the second quarter.

Analog Devices, 804 Woburn St, Wilmington, MA 01887-3462. For further information, contact Tremont Miao at (718) 937-1222; e-mail: tremont.miao@analog.com or tramm@aol.com. CIRCLE 531

STANDARDS WATCH

The Approaching Convergence Of PC-TV

John Frederick, Compaq Computer Corp.

The TV and PC are converging to create a new category of entertainment products. They will give consumers more options by combining the best features of each in a truly converged environment that's as easy to use as a standard TV. The computing power of a "PC Theater" coupled with a large-screen, progressively-scanned display make this an excellent living room platform for the digital media and interactive services available now, as well as in the future.

As this new product category grows, consumer electronics (CE) companies will include monitor functionality in their televisions. At the same time, PC makers will add TV functionality to their computers. This increased functionality in both the TV and PC increases the value to the consumer.

Because there are no standards for this category, products from different manufacturers will be incompatible. For consumers to have confidence in this new product, and for this new category to grow, open industry standards based on today's technology must be established. Such standards will allow companies from both the PC and CE industries to develop compatible PC-Theater products. Consumers must be able to select a display and a PC from different manufacturers and use them together as a system without needing custom cables and complicated setup procedures. In addition, the standards must be compatible with existing standards, so PC Theatre displays and computers may be used with standard PC and CE products.

Last year, a consortium consisting of Compaq, Hitachi, Intel, Mitsubishi Electric, NEC Technologies, Philips Electronics, Thomson Consumer Electronics, and Toshiba announced the PC Theater Initiative and support for standards that will be created for this product category. The primary focus of this initiative is to develop interoperability standards between PCs and large-screen displays capable of displaying high-quality progressively scanned video.

This Video Electronics Standards Association (VESA) committee was established to address the new interoperability standards and to work with other standards bodies, such as the Consumer Electronics Manufacturers Association (CEMA). CEMA has set up a committee to develop similar PC Theater standards, and will be using several VESA standards as building blocks for its standard. The goal of both organizations is to develop a compatible set of system-to-display interface standards. The object of the VESA PC-Theater Interconnectivity standard is to provide the necessary information to build a PC-Theater computer or display by culling all the required standards, providing any additional specification information required, and specifying the operation of each device.

A PC-Theater system comprises the PC and the large-screen display. The display is the same size as a typical TV and has the same functionality as a standard VGA monitor. In addition, the display may support enhancements for showing TV video. Optionally, it could offer all the functionality of a standalone TV, including the ability to display standard interlaced TV video.

The PC is a typical multimedia system with a fast microprocessor, DVD/CD-ROM drive, modem, TV tuner, USB, and audio-video subsystem capable of combining PC and TV audio and video. The PC also may support IEEE-1394 (Firewire). In addition, a set-top box could be substituted as the computing device.

The input devices must be wireless so users can control the system from the comfort of their sofas. A typical remote could be used for watching TV, while a second remote with a pointing device could be used for both PC and TV functions. A wireless keyboard is recommended for the PC functionality, and wireless gamepads and joysticks for playing video games.

Both the PC and display have connector panels with standard audio, S-video, and composite video jacks for connecting typical CE devices such as VCRs, DSS systems, DVD players, and audio systems. The PC Theater Interconnectivity Standard contains several key points. One connector will be defined to allow a single cable to carry all of the required signals between the PC and the display. Automatic configuration will eliminate most user intervention.

The display will be driven by the PC using standard analog or digital computer signals. The PC and display support two different viewing modes—one for displaying PC graphics, and the other for TV video. The PC and display will support USB software so the PC can control the display. In addition, all user input is passed to the PC for processing.

For more information on the PC-Theater Standard, contact VESA at (408) 435-0333, or on the Internet at http://www.vesa.org.

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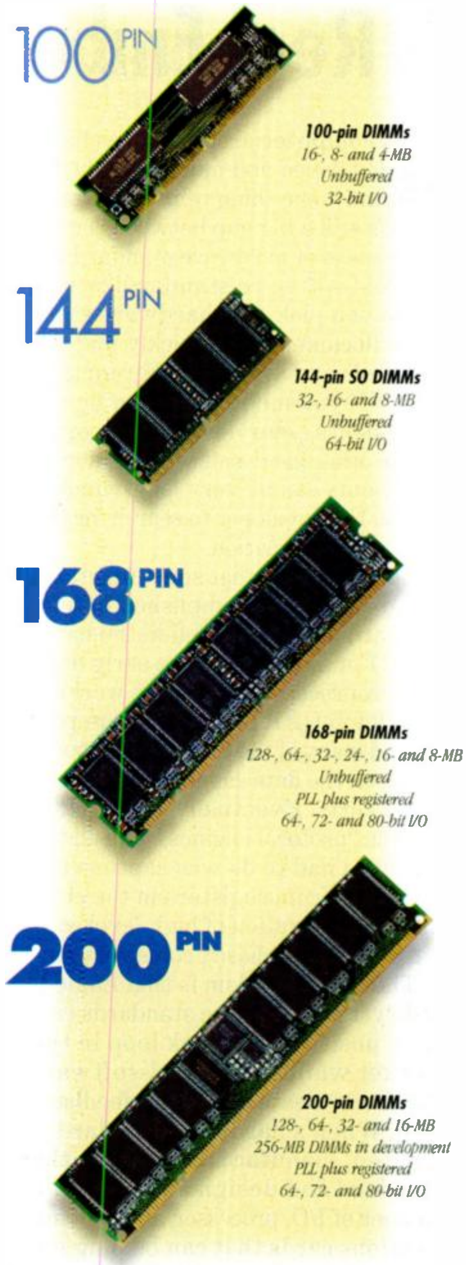

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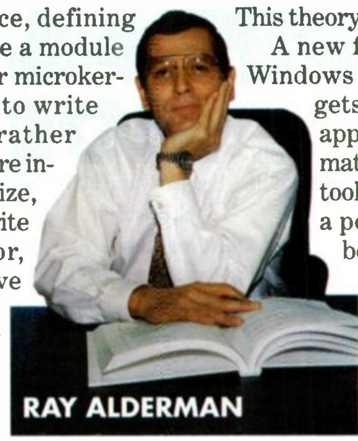
A Real Embedded-Software Standard?

As computer architectures have developed and mutated over the years, one thing remains certain: There's still a big gap between the effectiveness of hardware standardization and software standardization. When you pick up a hardware standards document, you quickly find the protocols and a timing diagram that says, "If you meet these timing requirements, your design will work." On the other hand, software standards documents can be very long-winded, forcing the developer to search for the pertinent information.

Consider, too, that some functions that once were accomplished in software are now embedded in the hardware. For example, in the early days of microprocessors, we were working with dumb UARTs, and software performed many of the bit-stripping operations on the data coming through the serial ports. Eventually, the UARTs became "protocol engines," and all the software had to do was capture the hard data from registers in the chip. But the integration of high-level software into silicon hasn't come very far.

The basic problem is that embedded-system hardware standards create a positive feedback loop in the market while embedded-software standards create a negative feedback loop. When a hardware standard is created, manufacturers adopt the standard and design and market a number of I/O, processor, and communications cards that can be plugged into a backplane. OEM users adopt that modular hardware standard because they can buy these cards from different manufacturers and build systems without doing the complex hardware designs. Manufacturers then design and market more interface and CPU cards as the technology changes, and the positive feedback continues for both the manufacturer and the user. In this way, hardware standards create markets for products that comply with the standards.

Embedded-software standards seem to work the opposite way. When a software interface standard is created, users of that standard often write their own software instead of buying it. For instance, defining certain standards. like a module interface for a modular microkernel, motivates users to write their own modules rather than buy them. The more interfaces you standardize, the more code users write and avoid paying for, thus creating a negative feedback loop.


RAY ALDERMAN

Here's my theory for why this happens: Hardware is made from atoms and hardware manufacturers know they have some level of variable cost associated with the components they use to build computers. They can minimize these variable costs, but they can't eliminate them. Software, on the other hand, is not made from atoms. It's an intangible part of the end-product, so why should you pay for a software component that you can't see or touch? So while it's impossible to eliminate the variable cost of your hardware components, you can reduce the variable cost of your software to near zero.

Consider an operating system as an example. If you're a large OEM who uses hundreds or thousands of copies of an OS in your end product, your eye is on the variable cost of that software. If someone will sell you a basic OS with well-defined module interfaces, you can hire 20 software engineers and write the disk I/O subsystem or the network I/O subsystem and amortize that fixed cost over all the products you ship. In other words, you can take most of your software costs as fixed costs, not variable costs. They're easier to swallow that way if you're in high-volume production.

As a result, when an OS is modularized and the module interfaces are documented in a well-defined standard, the larger OEM software users tend to "do it themselves," because it starts making sense to eliminate any variable costs in your product—starting with the software costs. Ultimately, the more software standards we have for embedded systems, the more software the OEMs will write themselves, and the less they'll buy.

This theory works up to a point.

A new factor is the advent of Windows CE and Java. CE targets traditional embedded applications, while Java is maturing into a productive tool. If CE shapes-up to be a powerful real-time embedded kernel, and Java develops into a super-productive embedded system language, the worm will turn and we'll have a positive feedback loop working in the embedded -software markets.

If at some point they can buy an inexpensive copy of CE and Java "applets" for a few bucks, many OEM users of embedded software might actually buy the modules instead of writing them. And because CE and Java run on various CPUs, it might not matter which processor they use.

CE has the opportunity to establish a common API in the embedded world, along with a standardized tool chain and a standardized module-interface definition. This scenario simply consolidates all the 100 or so kernels and tool chains out there in the market into one.

But Java can do the same thing that Ada did 10 or 20 years ago. Ada started out as a language, and programmers wrote and shared libraries for different software functions until Ada became an environment. Then the library functions were integrated into a kernel, and Ada became an operating system, an environment, and a language all rolled into one.

What we may be witnessing with CE and Java is the de facto establishment of two future embedded-software standards. The only difference I see is that CE is a "write-it-once,-port-it-to-everything" technology, while Java is a "write-it-once,-run-it-on-everything" technology. If we could squeeze the best from each technology, we'd have "Java-juiCE," the best of both worlds and a single embedded-software standard. But that's wishful thinking.

Ray Alderman is the executive director of VITA. He can be reached at exec@vita.com.

Employ Multiple-DSP Design For Six-Channel Dolby Digital Encoding

Today's High-End Audio Platforms Are Increasing In Complexity, Fueling The Move To DSP-Based Systems.

JERRY PURCELL, Momentum Data Systems, 17330 Brookhurst St., #140, Fountain Valley, CA 92708; (714) 378-5805.

The design of digital signal processing (DSP) systems for today's high-end audio authoring applications is rapidly moving from the relatively simple realm of single-processor subsystems to more complex multiprocessor architectures. To a great extent, this upward migration in commercial authoring systems is being driven by the evolution of more sophisticated consumer audio systems. While multichannel stereo sound has existed since the early Bell Labs experiments of the 1930s, the use of several separate soundtrack channels to maximize the listeners' experience has traditionally been used only in higher-end applications, such as cinema.

When stereo sound first made it into the home market in the late 1950s, it was limited to two channels because that was the most that early phonograph technology could accommodate. For almost three decades, the two-channel home stereo remained an accepted standard despite continuous improvements to the media used for recording sound. On the other hand, film makers long ago came to regard four channels (left, center, right, and surround) as the minimum necessary to create a convincing, lifelike sound experience for the listener. During the 1980s, the motion picture industry widely adopted the Dolby ProLogic format as the accepted commercial standard for matrix-encoding four channels onto two soundtracks. With the rise of the home video market, Dolby encoding also opened the door for richer home stereo experiences, with Surround Sound systems taking advantage of the four-channel cinematic encoding included in home video formats.

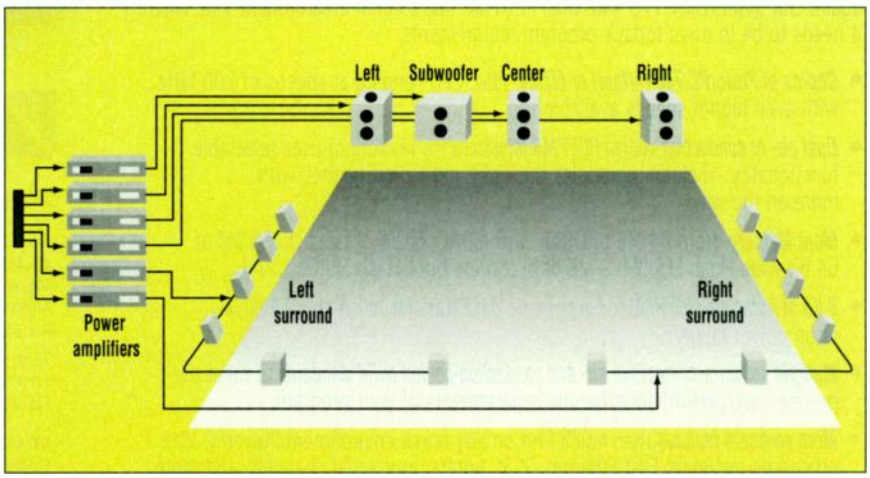
Today, both the consumer and cinematic audio industries have now shifted into high gear with digital formats, which greatly expand the options for widespread delivery of multichannel sound. Once again, the industry has turned to Dolby for its standard, with Dolby Digital (also known as Dolby AC-3) becoming the de facto method for today's six-channel digital sound encoding. Dolby Digital expands on previous-generation four-channel systems by providing two independent surround channels plus a separate subwoofer channel for special effects. These new features, combined with full-fidelity right, left, and center channels, enable Dolby Digital to deliver enhanced "perceptual encoding," designed to give the listener a lifelike experience *(Fig. 1)*.

Dolby Digital Encoding

While Dolby Digital greatly enhances the audio experience of the end user, it places significant challenges on the designers of high-performance DSP encoding systems. For instance, Dolby Digital employs 20-bit dynamic-range digital signals over a 20-Hz to 20-kHz frequency range, with the bass-effects channel operating in the 20- to 120-Hz range. Sampling rates of 32 kHz, 44.1 kHz, and 48 kHz are supported, and data rates can range from 32 kbits/s for a single channel to 640 kbits/s for multiple channels. The most typical applications of Dolby Digital include 192 kbits/s for two-channel and 384 kbits/s for six-channel distribution.

From a system designer's standpoint, there's enough compute power in one 24-bit DSP (such as the Motorola 56301) to handle the encoding tasks for two-channel Dolby Digital. This allows for a relatively simple two-channel board design that can focus mainly on combining the DSP with appropriate digital-audio receiver and transmitter functions, interfacing it to the authoring system's PCI bus, and providing enough SRAM to support the encoding functions *(Fig. 2)*.

Higher data rates are required for professionally-oriented six-channel



1. The Dolby Digital (Dolby AC-3) standard is employed for six-channel digital sound encoding. It adds two independent surround channels plus a separate subwoofer channel for special effects.

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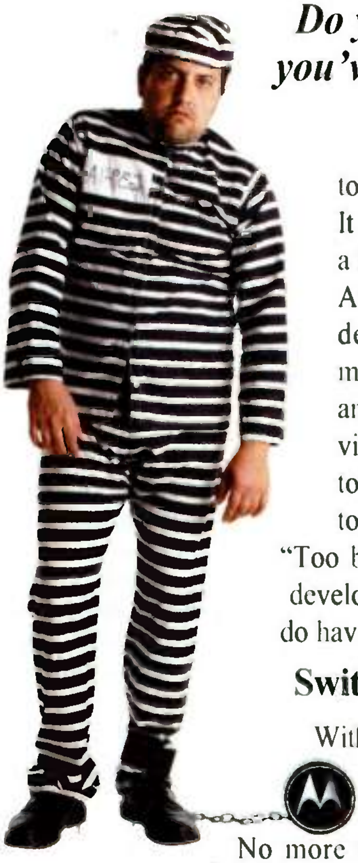

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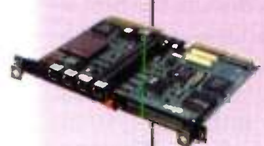

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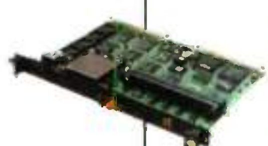

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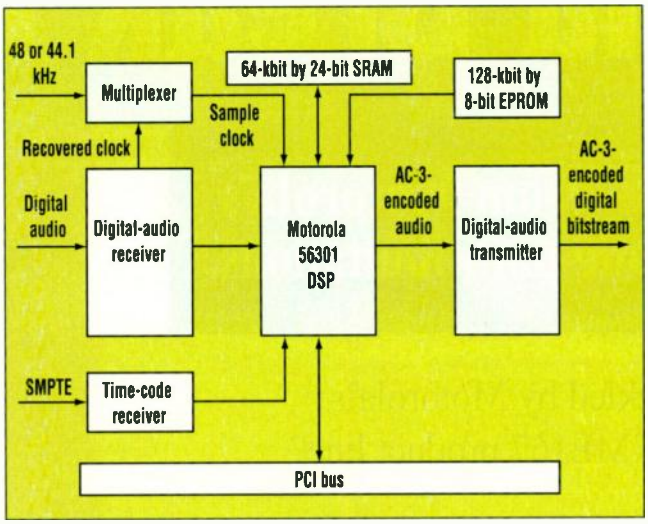
authoring systems that create the audio for today's cinematic, MPEG, and DVD titles. For these high-end authoring systems, at least three 24-bit DSPs are needed to handle the encoding task, thereby complicating the designer's challenge. Some of the key issues in the design of a multi-DSP six-channel encoding system include: creating an efficient architecture to balance data throughput, PCI bus interface, and I/O requirements; handling interprocessor communications; deciding on unshared verses shared memory; and resolving interprocessor clock and timing issues.



2. Using a 24-bit DSP (Motorola 56301) to handle the encoding tasks for two-channel Dolby Digital, there's enough compute power left for digital-audio receiver and transmitter functions. The DSP connects directly to the authoring system's PCI bus.

Architectural Issues

When creating a design, the first issue that must be addressed is establishing the basic architecture for the encoding subsystem. Because most professional audio authoring systems are built around a high-end Windows-based PC, designing the six-channel Dolby-encoding subsystem as a PCI plug-in card is a primary requirement. Secondly, significant I/O challenges are dictated by the need to bring in six separate channels of digital audio information, plus SMPTE time-code reference data. Then the Dolby-encoded results have to be output as one digital-audio bit-stream.

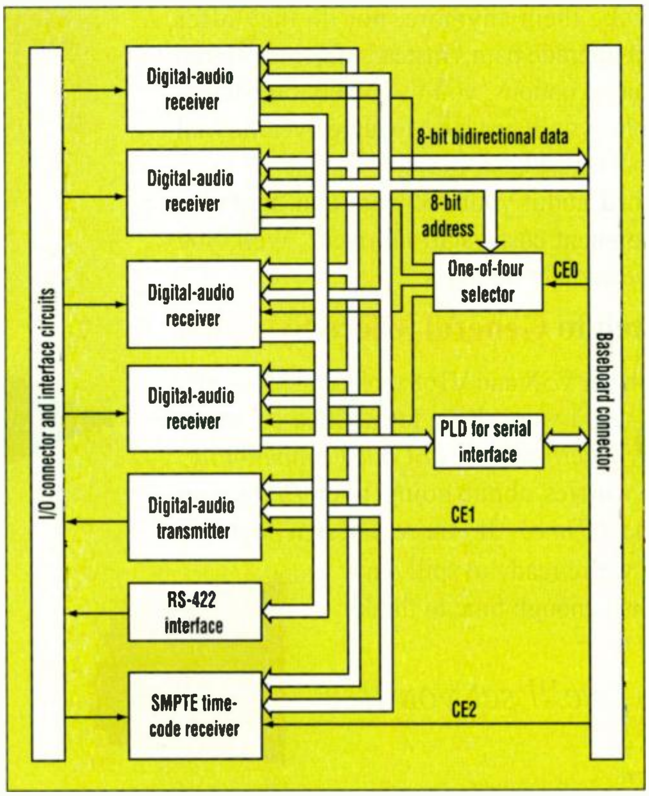
From an architectural standpoint, the requirement to interface directly to the PCI bus, and the heavy I/O demands make a master/slave DSP arrangement a more viable alternative to using a symmetric multiprocessor configuration. The bus specifications for PCI require that main processors for a plug-in card use a controlled-impedance clock line from the bus interface that's precisely 1.5-in. long, with all other lines less than 1.5 in. In practical terms, this dictates that all master processors must be within 0.5-in. of the card edge containing the PCI bus interface.

Using one master DSP to supply the sole interface to the PCI bus, and to control the other two DSPs as slaves simplifies the board's physical layout and the logical interface to the PCI bus. Instead of having to employ a separate PCI bridge chip to control a subsidiary bus on the plug-in card, one master DSP lets the design take advantage of the Motorola 56301's built-in PCI interface. This arrangement saves significant parts cost for the overall system.

The master/slave architecture also allows for a relatively straightforward I/O design. Using one master DSP for all I/O activity lets the master shelter both of the slave DSPs from outside interrupts. This technique allows for maximum data-flow throughput between the three DSPs.

In the reference design, a basic architectural decision was made to handle all I/O through a separate daughterboard attached to the main PCI subsystem. The daughterboard operates through an interboard connector to the master DSP's high-speed serial port. It allows the master processor to directly control all I/O activity on the daughtercard. A daughterboard was used primarily because the multiple stereo-input connectors (either S/PDIF or AES/EBU) and digital-audio receivers required more physical space than the main PCI card could support. In addition, the daughtercard allows the system to be tailored to the specific I/O needs of various OEMs, without requiring alterations to the main PCI card *(Fig. 3)*.

A key design challenge on the daughterboard involves the smooth meshing of the output streams from the three digital-audio (DA) receivers. Because the DA receivers are each designed to be the only device using a particular data channel, the daughtercard layout had to incorporate a programmable logic device (PLD) that combined their outputs into one stream for transmission to the master's Extended Synchronous Serial



3. In the reference design, a daughterboard is employed to handle all I/O. It connects through an interboard connector to the master DSP's serial port. This configuration allows the system to be tailored for specific I/O needs without any modifications to the main PCI card.

Interface (ESSI) serial port. The PLD sends a separate frame synchronization signal to control each DA receiver, so that their combined output is effectively interleaved on the serial port. On the output side, the daughterboard is designed to accommodate either a digital-audio transmitter stream or an RS-422 bit stream. These options make the output convenient to use with applications ranging from DVD authoring to direct broadcasting.

Designing For Extensibility

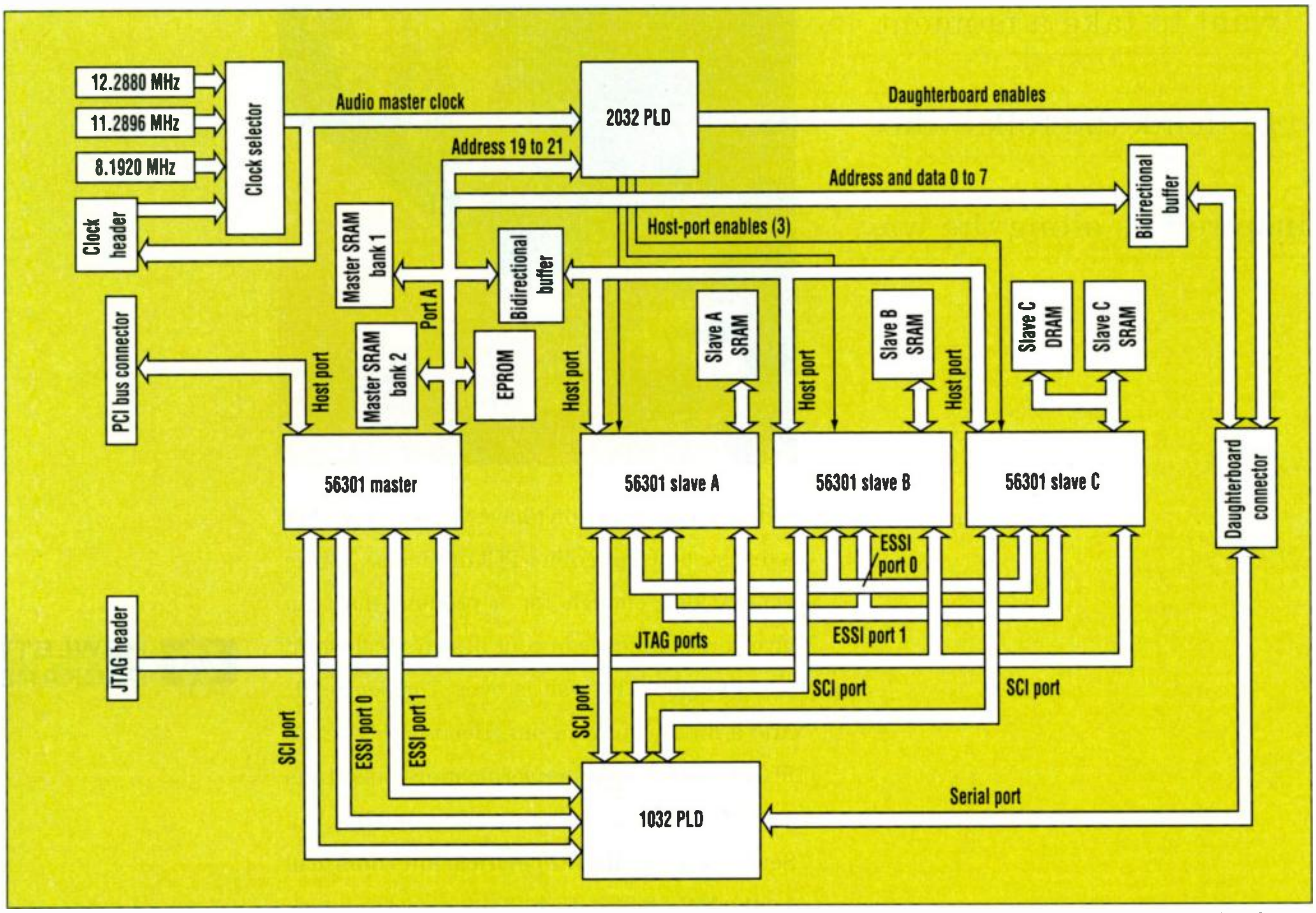
Another architectural decision is to lay out the PCI board with an option for a fourth 56301 chip, in addition to the master DSP and the first two slaves. Although the throughput demands of six-channel Dolby encoding can be effectively handled by three 56301s, the option for adding a third slave gives the board potential extensibility for future applications, such as eight-channel encoding or MPEG authoring systems. It also enables the design to be used for various general-purpose encoding applications by OEMs that need to interface to custom daughterboards. Also, in the interest of extensibility, the daughterboard is designed to accommodate up to four stereo digital-audio receivers, although only three are needed for six-channel operation. This design allows the same basic design to be used for eight channels in the future.

Once a decision is made to go with a master/slave configuration, the next challenge is to determine the best method for passing data between processors. While the slaves don't necessarily need to communicate with one another, the master processor does need to efficiently pass data and control information to and from each slave. Interprocessor communication was ultimately accomplished by mapping the 32-bit host processor ports for each slave directly into the peripheral space for the master processor *(Fig. 4)*.

Although the six-channel Dolby encoding application only requires data flow to and from the master to each processor, the board also is designed to allow future applications to use direct communications between the slave DSPs, if necessary. An option is built-in for the slaves to interface with each other through the 56301's ESSI serial ports. However, the master isn't connected to this serial communications ring because its ESSI ports are dedicated to handling the daughterboard I/O interface as described above. For future or custom OEM applications, this option could provide a data-flow pipeline in which the master passes to Slave A through the host port, which then passes to Slave B and/or C through the serial ports. The results are ultimately passed back to the master over the last slave's host port.

Shared Vs. Unshared Memory

The only alternatives to communicating over the host port consist of building an on-board PCI bus or communicating through shared memory. Both options are costly and/or cumber-



4. Data is passed between microprocessors by mapping the 32-bit host processor ports for each of the three slaves directly into the peripheral space for the master processor. This process occurs through the PLD.

some when compared to direct host-port communications links. Use of the host ports to treat each slave as a 24-bit peripheral allows the transfer of a 24-bit word every 37 ns, using two wait states, which essentially equals the performance of using true dual-port shared memory, at a significantly lower parts count and cost. Instead of requiring three 8-bit wide dual-port memory chips per slave DSP, the host-port mapping only needs two chips for data and address buffering in the host's peripheral space. In addition, the straightforward nature of the host-port mapping simplifies the overall system design and improves its reliability.

Clock Management

One of the key issues in any high-speed multiprocessor system is the design of the robust clock-management, timing, and synchronization mechanisms. Precise interprocessor clock synchronization is required to enable all of the master and slave DSPs to run at full speed and to minimize the need for unnecessary wait states.

This issue is addressed by having the master provide a common clock signal for all of the slave processors. Each Motorola 56301 contains an internal PLL, which can multiply a reference frequency, under software control, to establish its own clock. In the reference design, the master 56301 multiplies a 10-MHz reference crystal by eight to obtain an 80-MHz clock. That common 80-MHz clock is then output by the master to each slave DSP, which uses its PLL to generate its required 80-MHz operating clock. While each slave could independently calculate its own clock from the reference crystal, the sharing of a common clock from the master ensures precise synchronization with minimal skew.

System Initialization

To make the operation of the Dolby encoding subsystem transparent to the user, the board is automatically initialized in two steps—at system boot-up and at applications start-up. The master processor first boots from the system EPROM as part of the system initialization. The master processor then boots up the slave processors only when it receives instructions from the Dolby AC-3 encoder application running on the host CPU.

This application-driven boot-up of the subsystem ensures that the hardware is always configured exactly to the user's session requirements, such as the data rates and sampling parameters, as dictated by the user's menu-driven selections in the application GUI. Therefore, despite the complex level of multi-DSP processing that occurs at the hardware level, this layered software/hardware architecture lets the user focus on the high-level application rather than the underlying DSP process.

Jerry Purcell, president of Momentum Data Systems, holds a PhD in Applied Mathematics and Engineering from Claremont College Graduate School, Claremont, Calif., an MSEE from California State University, Long Beach, Calif., and an MA in Mathematics from the University of Washington, Seattle.

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WHAT'S ON BOARD

A low-power implementation of the PowerPC 603 processor, the 603e, features high-reliability upscreening that allows the processor to operate over the full military temperature range of -55 to 125°C. Available from White Microelectronics, Phoenix, Ariz., the processor can operate at clock frequencies ranging from 80 to 100 MHz, and comes in two package options, a 240-lead, 1.23-in.^{2} ceramic quad flatpack, or a 256-contact ball-grid array that measures 0.827-in./side. The 32-bit PowerPC 603e is a superscalar processor that can issue and retire three instructions per clock cycle. On chip are five independent execution units, and dynamic power management to continually minimize power draw. Dual 16-kbyte data and instruction caches are four-way set associative and each includes a memory management unit. Prices for the WC64P603E-XXM start below $500 in lots of 100 units. Call Philip Farahmand at (602) 437-1520, or on the web at www.whitemicro.com.

With a 100-MHz maximum operating frequency, the TurboClock family of timing circuits from Quality Semiconductor Inc., Santa Clara, Calif., offers multiple outputs with skews between 200 and 250 ps. The circuits include four clock-output pairs that are precisely programmable with up to 18 ns of delay in steps of 750 ps to 1.5 ns, with 750-ps resolution. Jitter is less than 200 ps peak-to-peak, thanks to an on-chip loop filter that also eliminates five-to-eight external components. Five chips in the family offer outputs that can be multiplied by two or four, while others are divided by one-quarter or one-half, or phase adjusted or inverted. The CMOS circuits also demand less power than their biCMOS competitors, consuming just 20 mA in standby mode. They can operate from a 3.3- or 5-V supply. Housed in either PLCCs or QSOPs, samples of the QS599X TurboClock chips sell for $4.66 in lots of 10,000 (750-ps resolution models). Call Deepak Savandatti, (408) 450-8016.

Meeting all the requirements for an AC-97 audio codec, the WM9701 from Wolfson Microelectronics Ltd., Edinburgh, Scotland, achieves a signal-to-noise ratio better than 92 dB—well beyond the 85-dB rating in the AC-97 specification. The chip also can operate at lower supply voltages than called for in the spec, 3.3 V, making it suitable for portable systems. The lower operating voltage also keeps the operating current low, just 34 mA. Housed in a 48-lead TQFP, the WM9701 sells for $3.95 apiece in lots of 100,000 units. Contact John Urwin, (44) (0) 131 667 9386, or on the Web at www.wolfson.co.uk.

A higher speed grade of FPGA—found in the XC4000XL-09 and XLT-09—provides a 15% increase in operating speed over existing FPGAs from Xilinx Inc., San Jose, Calif. The higher speed lets the company offer its next-generation PCI-interface logic cores, which provide 32-bit, 33-MHz operation, allowing designers to build PCI subsystems that can deliver the maximum sustained bandwidth. The LogiCORE 2.0 PCI cells are available as a master (initiator and target), and slave (target only). Cores can be configured and downloaded from the company's core generator on their web site (*www.xilinx.com/products/logicore/pci/pci_sol.htm*). The PCI master core can be licensed for $8995, while the slave goes for $4995. A CD-ROM also is available with all the design files. Prices start at $51.45 apiece in 100-unit quantities.

A pair of 16-Mbit synchronous graphics DRAMs give designers two choices: either a high-performance series-stub-terminated logic interface for operation at speeds up to 143 MHz, or an LV TTL interface for operation at speeds between 100 and 125 MHz. Developed by Samsung Semiconductor Inc., San Jose, Calif., the KM4132G513 SSTL SGRAM and the KM4132G512 LV TTL SGRAMs are organized as 512 kwords by 32 bits, operate from 3.3-V supplies, and come in 100-lead PQFPs or TQFPs. The LV TTL memory has operating and standby currents of 180 and 2 mA, respectively, while the SSTL device has respective currents of 200 and 3 mA. In lots of 1000, the 100-MHz KM4132G512 sells for $16 apiece, while the 143-MHz KM4132G513 SGRAM sells for $19 each. Call Mueez-Ud Deen, (408) 954-7000.

DVD Reference Designs Gets Designs To Market Quickly

If you're planning to build a DVD platform, one place to turn is the DVD reference design offered by Toshiba America Electronic Components. The design is based on the company's Timpani I single-chip DVD processor for PC-based playback. The chip integrates all of the functionality needed for high-quality, 30-frame/s DVD playback, including MPEG-2 video decoding and mixing, copy-protection processing, sub-picture decoding, and audio, video, and PCI interfaces. The reference design comes with a Timpani-based board, application software, drivers, and a DVD drive. The reference board costs $250.

Toshiba America Electronic Components Inc.*, 9775 Toledo Way, Irvine, CA 92618; (800) 879-4963; Internet: www.toshiba.com.taec.*

CIRCLE 490

Touchpad Adds Internet Browsing Features

The latest in a series of touchpads, called the Power Cat, is geared toward Internet surfers. The device is built with the company's GlideExtend technology that lets users reposition the finger and continue to drag an item, eliminating the "end of pad" problem. In other words, when the user's finger reaches the zone at the outer edge of the pad, the finger can be removed and repositioned for continued dragging.

The Power Cat can scroll effortlessly through a document or Web page. Users place their fingers on the textured area at the right side of the pad, and then glide them up or down to scroll. Horizontal scroll also is available. In addition, areas for "back" and "forward," typical navigation icons, have been added to the pad. The buttons correlate directly to the same buttons on an Internet browser. A signature-capture utility and stylus ship with the Power Cat, letting users add their signature, draw simple pictures, or add notes to a word-processing document. The Power Cat retails for $79.

Cirque Corp.*, 433 W. Lawndale Dr., Salt Lake City, UT 84115; (801) 467-1100; www.cirque.com.*

CIRCLE 491

Board Lets Users Connect USB Devices To Legacy PCs

Most of the PCs that ship today come bundled with USB ports. The associated peripherals will start to ship in large quantities very soon. However, what does that mean to the huge installed base of PCs that don't contain USB ports? Without some kind of retrofit board, it means that all of those PCs are shut out from using the latest USB-based peripherals. To combat that problem, the SYM60800 is a PCI-to-USB host adapter that lets users connect USB devices to their PCs through the PCI bus. The board is easy to install and contains no jumpers. It's supported by Microsoft's OHCI standard drivers. One 12-Mbit/s hot-plug port is supplied for either bus- or self-powered peripherals.

Symbios Logic Inc., 2001 Danfield Ct., Fort Collins, CO 80525; (800) 856-3093 or (970) 223-5100; Internet: www.symbios.com.
CIRCLE 460

Bridge Chip Connects TI DSPs To PCI Bus

Designers who use the Texas Instruments TMS320C80 and TMS320C82 digital signal processors can take advantage of the Eighty-X PCI bus bridge. The chip forms a bridge between the DSP and the PCI bus, giving the system access to PCI's performance, time-to-market, and cost benefits. Targeted applications that will benefit from this type of connection include high-end video conferencing, imaging systems, and machine vision. A full suite of development tools, called the Eighty-X Toolbox, is available. It includes an evaluation board with driver software, executable Verilog models and IBIS models, and a reference design. Limited samples of the Tundra Eighty-X DSP-to-PCI bridge are available now. Production prices will be $28 each in lots of 10,000.

Tundra Semiconductor Corp., 603 March Rd., Kanata, Ontario, Canada K2K 2M5; (613) 592-0714 or (800) 267-7231; www.tundra.com.
CIRCLE 461

48X CD-ROM Controller Integrates PHY

CD-ROM designers looking for a way to save valuable real estate can take advantage of the SYM13FW301, a CD-ROM controller with an integrated PHY. The 1394 interface handles 400 Mbits/s. It contains a high-performance buffer manager with a bandwidth that supports 48X data streaming from the disk into the buffer, with simultaneous 400-Mbit/s 1394 data transfer out of the buffer. In addition, it offers full-speed, on-the-fly error-correction code with flexible user control. Algorithms ensure that no gaps or overlaps occur in the audio data as it's stored in the buffer. Housed in a 100-pin TQFP, the SYM13FW301 CD-ROM controller costs under $10 in large volumes. Samples will be available in March, as well as an evaluation board, firmware, and *(continued on page 111)*

(continued from page 110)
documentation. Volume production is planned for the third quarter.

Symbios Logic Inc., 2001 Danfield Ct., Fort Collins, CO 80525; (800) 856-3093 or (970) 223-5100; Internet: www.symbios.com.
CIRCLE 462

DVD Card Targets Upgrade Kits, System Integrators

Designed for upgrade kits and system integrators, the Hollywood 2 DVD card can turn a PC into a full-featured home theater, supporting all of the standard DVD formats as well as the MPEG-2 interactive titles. Using the card, video can be output simultaneously to a PC display and a television. Audio is available through the PC's sound card in a stereo format. The Hollywood 2 card works with a 133-MHz Pentium system without any other special hardware except the DVD drive itself. Dolby Digital AC-3 5.1-channel audio is supported in software. The graphical user interface, called DVD Station, comes bundled with the card. It provides the DVD navigation and control.

Sigma Designs Inc., 46501 Landing Pkwy., Fremont, CA 94538; (510) 770-0100; www.sigmadesigns.com.
CIRCLE 463

Utility Helps Build ACPI-Compliant Systems

PC OEMs can shorten their time to market and save development costs by employing the ACPI Builder, a Windows-based utility that provides a comprehensive ACPI (Advanced Configuration and Power Interface) development environment. ACPI improves system power management and plug-and-play capability using operating-system-directed functions. ACPI Builder lets designers build ACPI-ready systems by ensuring that the correct hierarchy is used. Employing a graphical user interface, the utility comes with an ACPI source-language (ASL) syntax checker and automatically builds ACPI machine language. Various ASL libraries are included.

SystemSoft Corp., One Innovation Dr., Natick, MA 01760; (508) 651-0088; www.systemsoft.com.
CIRCLE 464

Low-Cost PHY Chips Transfer 400 Mbits/s

A family of 400-Mbit/s physical-layer interface (PHY) chips helps peripheral designers build high-end devices, such as hard-disk drives, printers, and cameras. The chips perform the transceiver functions of initializing the 1394 communications link, arbitrating for access to the channel, and actually placing data packets on the media. The different family members will be available with two, three, four, or six 1394 ports. The parts' power-savings capabilities include a device power-down mode and an inactive-port disable. The PHYs will interface directly to the company's 1394 link-layer chips, eliminating the need for glue logic. In addition, the parts comply with the Device Bay Initiative, which defines a standard modular design for PC chassis slots for peripheral equipment. Production volumes will be available during the second quarter. The chips' pricing starts at under $5.

***Texas Instruments Inc.**, Semiconductor Group, SC-97074, Literature Response Center, P.O. Box 172228, Denver, CO 80217; (800) 477-8924, ext. 4500; www.ti.com.* **CIRCLE 465**

Configurable USB Controllers Offer Multiple Design Options

A family of USB controllers gives system and peripheral designers access to USB cores that are both synthesizable and optimized for a 0.5-µm CMOS process. The USBX controllers are aimed at applications such as digital cameras, printers, mice, keyboards, PC speakers, joysticks, and scanners. By combining multiple variants of USB controllers with user programmability employing an on-chip gate array (up to 10,000 gates depending on implementation), designers can incorporate their own proprietary functions. For example, designers can choose a simple USB core consisting of a serial interface engine, a USB interface-transceiver, and 5000 programmable gates. Or a more integrated version could contain all of the above plus a 16-bit processor, ROM, RAM, a PLL and clock generator, and other general-purpose I/O.

All three members of the USBX product family use the same USB interface transceiver with a serial throughput of 12 Mbits/s. The transceiver's driver portion is differential, while the receiver section consists of a differential receiver and two single-ended receivers. The base-configuration, called the USB1, consists of the USB transceiver interface, the serial interface engine, and 5000 programmable gates.

The USB2 and USB3 incorporate additional processing power, enabling the design of intelligent peripherals that can preprocess data prior to passing it to the host PC. The USB2 also has a 16-bit processor with special-purpose instructions for USB transaction processing and control data processing. The code for the 16-bit processor resides in a masked ROM or external memory. The part also has 1 kbyte of RAM, 4 kbytes of ROM, an I²C interface, general-purpose I/O, EEPROM, a UART, and optional PLL circuitry. The USB3 adds an 8-channel 10-bit analog-to-digital converter, PWM output support, and a watchdog timer. It also contains 3 kbytes of internal SRAM buffer memory, 8 kbytes of ROM, and 8000 gates of configurable logic.

The USBX controllers are available in QFP, LQFP, BGA, DIP, flip-chip, and other package types. Pin counts are standard and vary according to device and design. An evaluation board also is available, as well as a set of software tools and debuggers. Prices range from $2 to $10, depending on configuration.

***Kawasaki LSI USA Inc.**, 2570 North First St., Suite 301, San Jose, CA 95131; (408) 570-0555; www.klsi.com.* **CIRCLE 466**

Hard-Disk Controller Embeds FC-AL Transceivers

Fibre Channel hard-disk drives have finally started to descend onto the electronics marketplace. To that end, the FTEC440 is a device that can connect those drives to the host. The IC is a single-chip dual-loop Fibre Channel (FC) transceiver and hard-drive controller. The chip supports two 100-Mbyte/s copper FC Arbitrated Loops (ALs) without the need for any external transceivers. Dual 8- or 10-bit interfaces also are supplied for use with external copper or optical transceivers.

Designed for drives with MR heads, the FTEC440 supports all aspects of headerless operation on-chip. Usable capacity is maximized by allowing servo-burst sector splitting in any part of the format. The chip can correct error bursts up to 40 bytes long and maintains data and format integrity regardless of the erasure location.

An on-chip RISC engine allows for customized and automated FC-AL sequences and reduces host CPU overhead. The buffer manager supports 4 Mbytes of SDRAM with a 267-Mbyte/s peak transfer. The FTEC440 is housed in a 256-pin BGA.

***QLogic Corp.**, 3545 Harbor Blvd., Costa Mesa, CA 92626; (800) 662-4471 or (714) 438-2200; www.qlc.com.* **CIRCLE 467**

Reference Design Provides Sub-$1000 PC

System designers can easily build a sub-$1000 platform using a reference design offered by Cirrus Logic. Offering VCR-like simplicity in a sealed-chassis format, the architecture is optimized for Microsoft Windows 98 and targets the convergence of information, communications, and entertainment. This is achieved by integrating audio, 2D and 3D graphics over AGP, and a modem. The hardware-accelerated feature set includes AC-3 audio, TV output, DVD support, 56-kbit/s telephony, external USB and 1394 support, and ACPI/On-Now functionality.

***Cirrus Logic Inc.**, 3100 West Warren Ave., Fremont, CA 94538; (510) 623-8300; www.cirrus.com.* **CIRCLE 468**

32X CD-ROM Drive Transfers 4.8 Mbytes/s

It seemed like just yesterday that CD-ROM drives had reached the 8X plateau, meaning that the disk spins at 8X the rate of the original drives. Now, those speeds have increased to 32X, as evidenced by the FX320S. The drive features a data-transfer rate of 4800 kbytes/s and an average access time of 85 ms. The high level of performance is partly due to a 256-kbyte buffer. The drive's caddyless design is built with an auto-balance mechanism to minimize media-induced vibration. It supports the latest industry standards and is built to a standard half-height, 5.25-in. form factor, mountable in either a horizontal or vertical format. Available now, the FX320S 32X CD-ROM drive sells for $199.

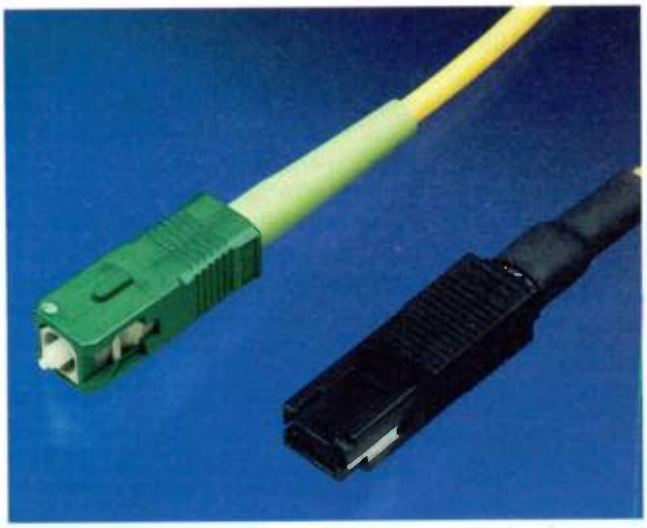
***Mitsumi Electronics Corp.**, 5808 W. Campus Circle Dr., Irving, TX 75063; www.mitsumi.com.* **CIRCLE 469**

Higher Density And Lower Cost Enhance Fiber-Optic Components

Strengthened By These Essential Ingredients, Fiber-Optic Technology Begins To Bubble Over As Copper Runs Out Of Steam.

MICHAEL S. PEPPLER, AMP Incorporated, P.O. Box 3608, Harrisburg, PA 17105; (800) 522-6752; www.amp.com/fiberoptics.

The advantages of using fiber-optic technology in data networking are clear. Fiber offers high bandwidth, high signal density, low crosstalk, immunity to EMI, and near-zero insertion force. Despite these advantages, fiber's high cost, relative to a copper solution, combined with the reluctance of many network managers to adopt a new technology, has slowed the implementation of fiber at the desktop. In fact, rather than migrating to a better overall solution for the long term, many managers are instead opting for creative solutions to improve the capabilities of the lower-cost copper implementation.



1. High-density array connectors, which incorporate MT-ferrule technology, have come a long way in reducing the cost and space requirements of a fiber-optic network. These connectors can typicaly accommodate two-to-12 fibers on 250-µm centerlines, and come with the option of being stacked on a 10-mm center.

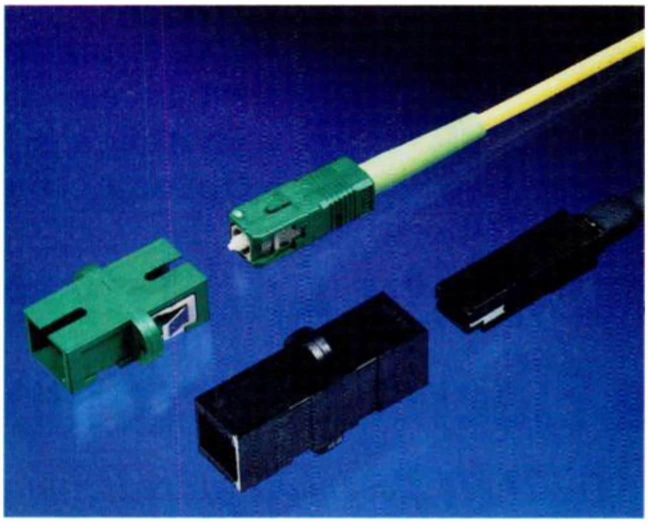
Recognizing this trend, fiber-optic component and connector manufacturers are working to reduce the installation costs of their technology by reducing the package size of their components and making them easier to use. In addition, by adhering to a new inteconnection standard for fiber-optic connectors, manufacturers hope to eliminate much of the confusion and compatibility problems surrounding these devices.

Several years ago, copper offered an installed cost that was much lower than fiber. But, with advances in the technology and greater acceptance, the cost of implementing a fiber-based systems has come down considerably. The telecommunications industry, for example, has implemented fiber as a matter of course for intermediate- to long-range communications networks. Fiber is also receiving greater acceptance within building networks to provide faster data rates within data-wiring closets.

Still, fiber's greater reliability, which translates into lower cycle-life, maintenance, and repair expenses, has not convinced many data networking managers. They continue to implement copper networks because there's a lower initial cost. In addition, these copper networks are often based on the newer, high-speed copper technologies, with signal encoding, to push for gigabit/s speeds overruns of up to 100 m, thus pushing the crossover point from copper to fiber further out. Regardless of the improvements in copper, many managers recognize that the reliability and bandwidth offered with fiber solutions is more attractive for the long term.

With that in mind, original equipment manufacturers (OEMs) are investigating ways to reduce manufacturing costs to effectively offer fiber alternatives. One approach to reducing manufacturing costs is to attack the challenge at the component level. To appeal to network managers, fiber-component makers must develop products with the same profile, plug-in convenience, and ease of use as the more-familiar copper components. Fiber components that offer the same—or smaller—dimensions and interconnectivity not only allow fiber implementation without additional manufacturing costs, they also give the end-user a familiar-looking piece of equipment.

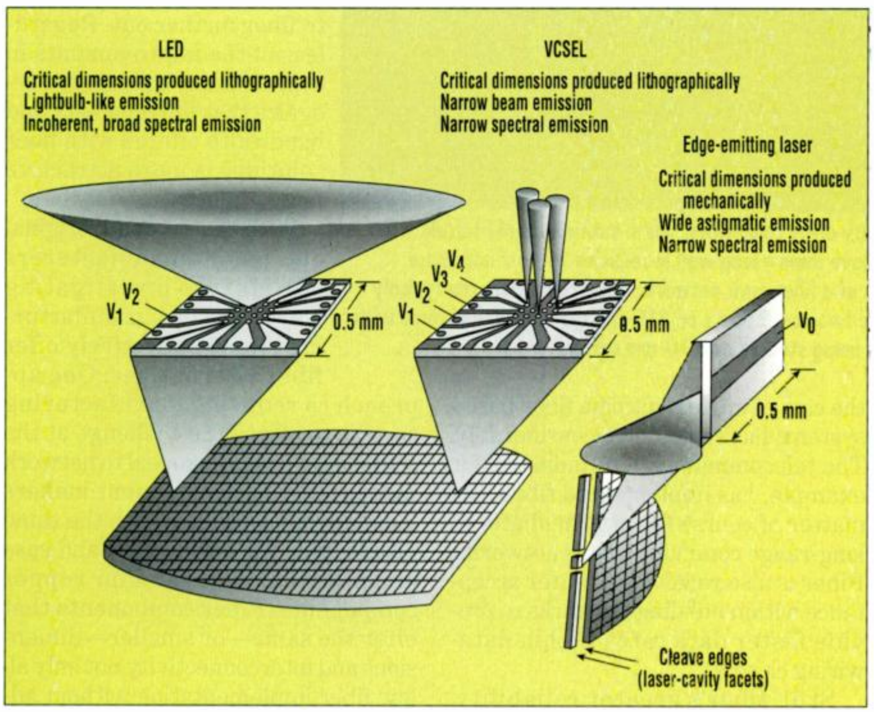
Shrinking the size of fiber components while increasing performance is a considerable undertaking. Reducing the size of one component may affect its ability to interoperate with other components within a system. Also, reducing the size of a component such as a connector will have little effect if the manufacturer cannot also reduce the size of the transceiver and other related components. By embracing reduced packaging as an overall design theory, and by applying new technology throughout all component offerings, manufacturers can reduce component size, the number of components required, and the bottom-line manufacturing costs of fiber-based systems. The end result being lower cost to the consumer.



2. Array connectors not only offer the same plug-in convenience that electrical backplanes have long provided, they also offer greater flexibility by allowing fiber-optic transceivers to be placed anywhere on the board. They also permit the designer to use a considerably smaller bulkhead adapter. The connectors also have form-and-fit compatibility with existing electrical backplane connectors to enable mixed optical/electrical connections.

Multiple Fibers

For many component manufacturers, examination of packaging technologies begins with the fiber connector. While copper connectors are packing circuits in contact areas under 5 mm, fiber-optic packaging has been too bulky to offer this type of density. Instead, OEMs have had to implement several fiber connectors to offer the number of circuits available in a single copper connector, thereby increasing costs by requiring more components.



3. Because VCSELs combine surface-emitting features with the fast operation (Gigabits/s), narrow spectral width, and low beam divergence of lasers, they make an attractive light source for next-generation transceivers.

To increase fiber density for data-networking backplane-oriented systems, component providers have introduced array connectors which have multiple fibers encased within a single ferrule *(Fig. 1)*. Incorporating MT-ferrule technology, designed by Nippon Telegraph & Telephone (NTT) in 1987, array connectors can accommodate two-to-12 fibers on 250-µm centerlines, and can be stacked on 10-mm centerlines for multiconnector applications.

Array connectors are being implemented in data centers to simplify and replace bus and tag wiring, creating an easily managed, structured system to replace the rat's nest typically found under the floors of computer rooms. In backplane applications, array connectors allow daughterboards to be easily plugged into the backplane to provide higher speeds.

These connectors not only offer the same plug-in convenience that electrical backplanes have long provided, they also provide greater flexibility. They allow fiber-optic transceivers to be placed anywhere on the board and provide for a considerably smaller bulkhead adapter *(Fig. 2)*. The connectors also have form-and-fit compatibility, with existing electrical backplane connectors to enable mixed optical/electrical connections.

In premises cabling and data-networking applications, array connectors are being introduced as an alternative to modular plugs and jacks. These array connectors offer the same density as copper modular jacks in the same footprint, therefore OEMs of communications panel outlets can design systems that accommodate both copper and fiber ports. This enables the adoption of fiber in sites that were formerly copper-only installations.

Arrays With VCSEL Technology

Optoelectronic manufacturers are working to provide array transceivers, which will feature multiple lasers and detectors, that will enable parallel transmission of data in a single data-link housing. Unfortunately, finding a way to cost-effectively place mul-

tiple lasers in a single housing has proven difficult. Recently, component providers have found one solution in the vertical cavity surface-emitting laser (VCSEL).

VCSEL light sources at 850-nm are designed specially for short-range multimode fiber communication, and use laser technology to achieve faster data rates through a system or backplane. Because VCSELs combine surface-emitting features with fast operation (gigabits/s), narrow spectral width, and low beam divergence of lasers, they make an attractive light source for next-generation transceivers *(Fig. 3)*.

In addition, VCSELs reduce fabrication costs by making testing possible at the wafer stage. They reduce component manufacturing costs because they can be used in array chips. Together with low-cost molded-optics technology, VCSEL light sources will encourage the design of more compact and cost-effective fiber boards.

Planar Waveguide Circuits

In order to lower transceiver costs, the VCSEL arrays can be on higher density centerlines than the 250-µm centerlines for fiber-ribbon cable. Research funded under the DARPA 93-46 Polymer Optical Interconnect Technology (POINT) program has led to the demonstration of transceivers with VCSEL arrays on a 140-µm pitch that can run in excess of 1 Gigabit/s.

New passive alignment techniques have been demonstrated for polymer waveguides to VCSEL arrays with 1-µm alignment tolerances—inspiring even smaller component footprints. In this case, the waveguides are 50-µm-by-50-µm rectangular waveguides on a 100-µm pitch. Interconnect schemes have been demonstrated that have up to 144 channels (250 signals per board-edge inch) at the daughtercard-to-backplane interface, with near-zero insertion force.

This method of planar-waveguide-circuit production also permits faster system assembly and lets semiconductor manufacturers reduce production costs by implementing batch manufacturing techniques such as photolithography and wet and dry etching. Because the manufacturing process is extremely accurate, time-consuming active alignments are not required. Together, these factors help to reduce the cost of component manufacturing, which reduces the cost of the component to the OEM.

Adherence To Standards

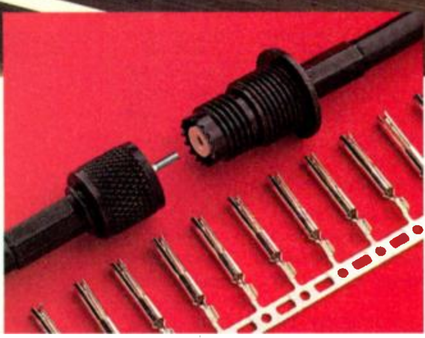
New packaging designs usually mean diverse implementations of components required for fiber-optic communications. To retain ease of implementation for OEMs, component providers must ensure that the packaging they offer adheres to industry standards. The International Electrotechnical Commission (IEC, *www.iec.ch*), is a standards and conformity assessment body for all fields of electrotechnology. Specifically, Subcommittee SC 86B develops fiber-optic connector-interconnection standards that are accepted by system and component manufacturers for global applications.

But, while the IEC standards dictate the interface dimensions for components, the standards wars are usually fought on the level of the applications standard. For example, manufacturers of hubs and switches battle over the types of connector interface that should govern their systems. Premises wiring and panel-outlet providers may support a different type of connector interface for their particular systems.

Because the new array connectors being introduced allow for mixed optical/electrical signals, the two worlds need not agree. A data network could have a panel outlet with an array connector that feeds into a cable leading into a different type of connector on the hub or switch. Adherence to standards is still important, but the same standard not need apply to all parts of a data or communications network to be successfully deployed.

Mike Peppler is the associate director of Product Marketing for AMP's Global Communications Business unit. He owns several product engineering patents and has garnered numerous awards for electro-optic product training and development from industry and corporate groups. His education credits include degrees in engineering and physics, and guided wave-optics from the Institute of Optics at the University of Rochester.

Wherever you may roam, AMP has the RF reach to cover you.



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READER SERVICE 206

PRODUCT UPDATE: CONNECTORS

Manufacturer	Device	Description	Price and delivery	CIRCLE
3M Electronic Products Div. Austin, TX Sales Dept. (800) 225-5373 ext.111	4 by 20 board-to-board connector	This high-density, four-row by 20-pin board-to-board connector allows designers to stack boards in space-constrained applications. Features include 0.050- by 0.050-in. pin spacing, a shrouded header to reduce bent-pin problems, and dual wipe sockets to improve contact.	$5.28 each per 5000	553
Aromat Corp. New Providence, NJ Sales Dept. (800) AROMAT9 Fax (908) 771-5658 www.aromat.com	P5KS series	Based on the company's bellows-type contact, these board-to-board connectors have from 20 to 160 contacts per connector. The devices have a 4.6-mm body thickness, come in stacking heights from 4 through 9 mm, and have a contact pitch of 0.5 mm. Rated at 60 V ac/dc at 0.2 A, the connectors come on tape-and-reel packaging.	$0.95 each per 10,000; six to eight weeks	554
Bomar Interconnect Products Inc. Ledgewood, NJ Bob Behrent (201) 347-4040 Fax (201) 347-2111	V-Brite RF connector	Available in pc-board-mountable BNC and TNC versions, these small-footprint, low-profile devices snap and lock into place, and are supported both above and below the pc board. The 50-Ω connectors have a VSWR of 1.15:1 and are available with a Teflon insulator.	$1.50 each per 1000	555
Comm Con Connectors Inc. Duarte, CA Bob Famum (626) 301-4200 Fax (626) 301-4212 www.commcon.com	Low-profile headers	These low-profile headers measure only 0.130 in. from the top of the pc board to the tip of the pin. Made from high-temperature, molded plastic with a maximum rating of 260°C, the devices are available in single- and double-row designs.	$0.02 per contact in high volumes	556
Detoronics Corp. South El Monte, CA Sales Dept. (626) 579-7130 Fax (626) 579-1936	DPPHOO3-50P	Designed for remote or blind installations where space is limited and quick connection is required, these receptacles use a straight push/pull action to connect or disconnect the unit. Standard devices come with #20 eyelet contacts, ferrous-alloy shells, and tin plating. Features include a high vacuum rating and hermetic sealing.	Three-conductors, $9.97 each per 100; stock to four weeks	557
Elco Corp. Myrtle Beach, SC Sales & Marketing (803) 946-0414 Fax (803) 626-5186 www.avxcorp.com	5087 Series	Part of the company's Super Microleaf 0.5-mm-pitch, board-to-board connectors, these devices come with up to 140 positions in stacking heights as low as 2.0 mm. The surface-mountable devices include a redundant shroud insulator for mechanical stability, and come packaged on tape and reel.	$0.06 per mated line per 10,000; eight weeks	558
Hollingsworth Corp. Irvine, CA Jim DePriest (714) 855-6404 Fax (714) 855-8264	5014 Series	These SCA-II connectors accommodate all SCSI-3 data, control, auxiliary, and power signals. The 80-position, board-to-board system features guide posts for blind mating, integral ground contacts, leaf-spring contacts on a 0.050-in. pitch, and a trapezoidal housing.	$2.50 each per 5000; six weeks ARO	559
Kycon Inc. San Jose, CA Wendy Wuerth (408) 494-0330 Fax (408) 494-0325 www.kycon.com	ST-2550-5N-TR	Targeting audio applications in the computer and multimedia arenas, these surface-mount, 2.5-mm, right-angle stereo jacks are made from high-temperature polyacetal plastic. The jacks are available with three, four, or five positions, and come on tape-and-reel packaging.	$0.54 each per 5000; six to eight weeks ARO	560
LEMO USA Santa Rosa, CA Karen Dias (800) 444-LEMO Fax (707) 578-0869 www.lemo.ch	Rugged connectors	Designed for both engine-management and data-logging applications, these rugged connectors feature a scoop-proof, push-pull, self-latching system, color-coded keyway identification, and an integral heatshrink-boot adapter. The connectors come in an aluminum-alloy shell with an anthracite conductive finish, and can withstand temperatures from -65° to 200°C. Sealing against moisture and contaminating fluids is included. Current ratings range from 2 to 10 A.	$40 per mated pair per 100; stock to eight weeks	561
Molex Inc. Lisle, IL Sales Dept. (800) 78-MOLEX Fax (630) 969-1352	1.5-mm SMT Wire-to-Board Connector System	Occupying up to 30% less space than the equivalent 2.0-mm-pitch versions, this low-profile SMT design comes in a single row with terminal locking windows and friction locks. The headers are polarized and fully shrouded. Rated at 1 A, the system's terminals accept 26-AWG wire and feature a dual-point contact.	Six-circuit, vertical header, $0.23 per 10,000; six weeks	562
Nemal Electronics International Inc. North Miami, FL Sales Dept. (305) 899-0900 Fax (305) 895-8178 E-mail: nemal@internetco.net www.nemal.com	UHF plug	This two-piece plug for RG217/U coaxial cable allows for direct connection to equipment with UHF-type receptacles. The connector features a gold-plated center contact, teflon insulation, and a knurled body.	$12.75 each per 100	563
Samtec Inc. New Albany, IN Danny Boesing (800) SAMTEC9 Fax (812) 948-5047 E-mail: info@samtec.com www.samtec.com	TMM Series	This high-density, four-row, 2-mm header interfaces with the company's standard and elevated 2-mm socket strips. Available in both right-angle and straight-pin versions, the strip has up to 50 pins per row and uses a black liquid-crystal polymer for high-temperature reflow.	$0.025 per contact; three days or less	564
Thomas & Betts Corp. Memphis, TN Sales Dept. (800) 888-0211 www.tnb.com	Eurostyle PCB connectors	Offered as a lower-cost option, these pc-board connectors complete the electrical connection by tightening the screw directly against the signal wire where it enters the connector's contact area. Featuring captive screws, the connectors come in a variety of styles and ratings.	Four-terminal, 5-mm pitch, $0.31 each per 10,000; stock to 10 weeks	565
Trompeter Electronics Inc. Westlake Village, CA Sales Dept. (800) 982-2629 Fax (818) 706-1040 www.trompeter.electronics.-industry.net	ADRMF70	Using a concentric design, these right-angle, TRB male-to-female adapters target telemetry and ground-support 1553 data-bus applications where cable management, strength, and security are a priority.	$35.70 each per 1000; stock	566

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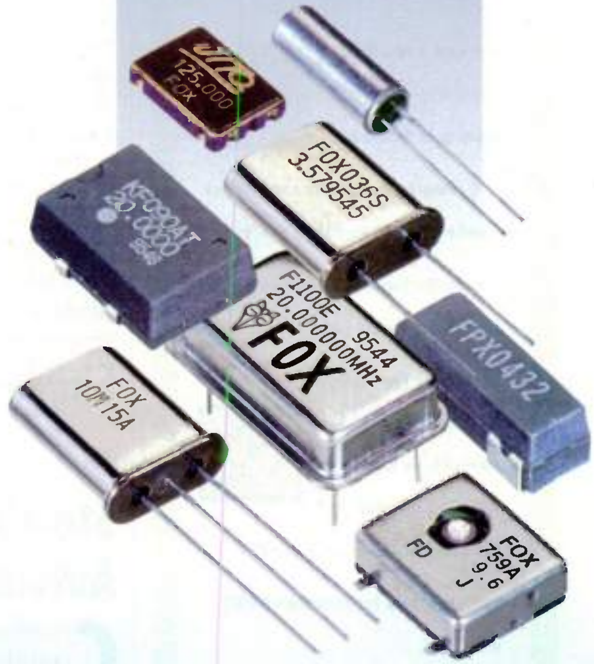

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READER SERVICE 162

PRODUCT FEATURE

Sockets And Pins Lend Flexibility, Lower Cost, And Ease Testing Of BGA Devices

To readily insert and remove BGA devices for both commercial and testing applications, Aries Electronics Inc., Frenchtown, N.J., has introduced a line of sockets and pins that either grip the balls of a regular BGA or replace the balls altogether to improve reliability and lower cost. Called the BallLock and SnapAdapt, respectively, the socket and pin arrangement comes with varying degrees of backward compatibility to cater to prior, current, and upcoming BGA designs.

The BallLock contact has been incorporated into a standard socket and comprises a two-fingered mating half to grip the balls of the BGA, and a lower half that's a solder ball. This half can be attached to the BGA footprint using normal paste screening. A key feature of the BallLock is the elimination of the lid, which usually holds a removable BGA in place for testing applications. The clamping action of the two-fingered contact is sufficient.

The socket has a profile of 0.050 in., uses UL 94V-0 FR-4 material, and uses beryllium-copper-alloy contacts. The per-contact inductance and capacitance at 100 MHz is less than 1 nH and 1 pF, respectively. The contact resistance is 10 mΩ, rising to 20 mΩ after 10 cycles. The insertion and removable forces, per contact, are 50 g and 20 g, respectively. Durability is 10 cycles maximum, rising to 50 cycles when used with the SnapAdapt pin.

The SnapAdapt pin itself comes in two versions. One version is designed for use in a BGA adapter that converts regular BGA packages into socketable "hard-ball" terminations, while adding only 0.150 in. to the device's profile when mounted in the BallLock socket. The other version is surface-mounted directly under BGA-oriented devices in place of the regular solder ball. The pins add only 0.100 in. to the package's profile, again when used with the BallLock socket. The brass-alloy pins are plated with gold over nickel and are rated for current levels of up to 1 A. Pricing for the BallLock, long-version SnapAdapt, and short-version SnapAdapt is $0.067, $0.02, and $0.01 per pin, respectively.

Aries Electronics Inc.
P.O. Box 130
Frenchtown, NJ 08825
Frank Folmsbee (908) 996-6841)
fax (908) 996-3891
www.arieselec.com
CIRCLE 500
PATRICK MANNION

Single-Pin Connector Developed As Standard For Automotive Airbags

Conscious of the many obstacles encountered when installing the typical airbag, often done without visual feedback, Thomas & Betts, Memphis, Tenn., has introduced a single-pin squib connector that is similar in concept to a coaxial connector. The connector replaces the commonly used two-pin variety that come out at 90° off the airbag and which cannot be detached without using a shorting clip. These are keyed to prevent the bag from misfiring. The single-pin squib connector requires no keying, so it's much more flexible upon installation.

The connector comprises a gold-plated contact made over a centered pin. The second circuit is constructed at the grounding plate at the base of the squib, with its contact surface available across 360° of rotation during installation. Features include allowance for electronic diagnosis of the interface mating and locking, and for disconnection of the airbag assembly from the pyrotechnic device. Industry compliance includes the United States Council for Automotive Research (USCAR) and the Electrical Wiring Component Applications Partnership (EWCAP). Pricing for the connector ranges from $0.50 to $1.00.

Thomas & Betts Corp.
1555 Lynnfield Rd.
Memphis, TN 38119

LINEAR TECHNOLOGY DESIGN NOTES

New 16-Bit SO-8 DAC Has 1LSB (Max) INL and DNL Over Industrial Temperature Range – Design Note 173

Jim Brubaker, William C. Rempfer and Kevin R. Hoskins

The new LTC®1595/LTC1596 16-bit DACs from LTC provide the easiest to use, most cost effective, highest performance solution for upgrading industrial and instrumentation applications from 12 bits to 16 bits. They feature:

- ±1LSB (max) INL and DNL over the industrial temperature range
- Ultralow, 1nV-s glitch impulse
- ±10V output capability
- Small SO-8 package (LTC1595)
- Pin compatible upgrade for industry standard 12-bit DACs (DAC8043/DAC8143 and AD7543)

NICE FEATURES OF THE 16-BIT DACS

These new CMOS current output DACs use precision thin-film resistors in a modified R/2R architecture. They have SPI/MICROWIRE™ compatible serial interfaces and draw only 10µA from a single 5V supply. They generate precision 0V to 10V or ±10V outputs using a single or dual external op amp. The LTC1596 has an asynchronous clear input and both devices have power-on reset.

Because the LTC1595/LTC1596's INL is five times less sensitive to op amp V_{OS} when compared to 12-bit devices, systems using the DAC8043/DAC8143 or AD7543 can be upgraded to true 16-bit resolution and linearity without requiring more precise op amps.

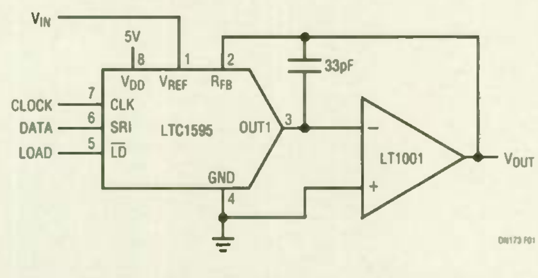

Figure 1. With a Single Op Amp, the 16-Bit DAC Performs 2-Quadrant Multiplication with ±10V Input and Output Ranges. A Fixed –10V Reference Generates a Precision 16-Bit 0V to 10V Unipolar Output

16-Bit Accuracy Over Temperature Without Autocalibration

Autocalibrated DACs achieve their 16-bit accuracy at the cost of additional autocalibration circuitry that increases size and cost, requires cumbersome calibration overhead for the user and, because of poor linearity drift, requires DAC recalibration every time the temperature changes.

By eliminating autocalibration, the LTC1595/LTC1596 offer a better choice. Figure 2 shows the outstanding 0.25LSB (typ) integral nonlinearity (INL) and differential nonlinearity (DNL). This accuracy and very low drift guarantee a 1LSB (max) INL and DNL specification over the industrial temperature range without autocalibration.

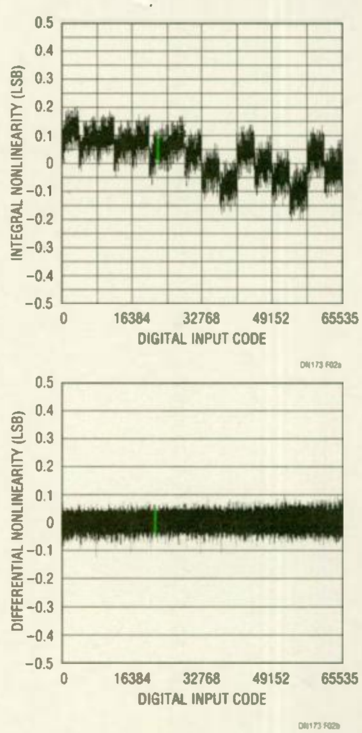

Figure 2. The Outstanding INL and DNL (≤ 0.25LSB Typ) and Very Low Drift Allow a Maximum 1LSB Specification Over Temperature

Jltralow 1nV-s Glitch

\ new proprietary deglitcher brings great benefits to preci-ɜion applications because it reduces the output glitch mpulse to 1nV-s, ten times lower than any other 16-bit ndustrial DAC, and makes the glitch impulse uniform for ɪny code. Figure 3 shows the output glitch for a midscale ransition with a 0V to 10V output range.

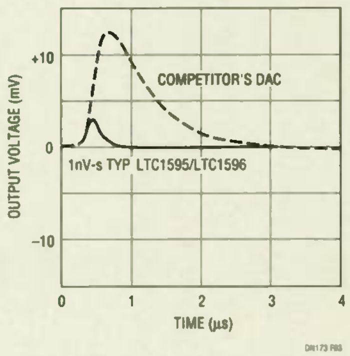

Figure 3. The Output Glitch is Less Than 1nV-s, Ten Times Less Than the Best 16-Bit Industrial DACs

ʼrecision 0V to10V Outputs with One Op Amp

The LTC1595 can be configured to generate 0V to 10V by ɪpplying –10V to the V_{REF} pin as shown in Figure 1. This ;ircuit can also perform 2-quadrant multiplication where he reference is driven by a ±10V input signal and V_{OUT} ;wings from 0V to $-V_{REF}$.

The LTC1595/LTC1596 allow designers to choose an op amp that optimizes an application's accuracy, speed, power and cost. An LT®1001 provides excellent DC precision, low noise and low power dissipation (90mW total for Figure 1's circuit). For higher speed, the LT1122 will provide settling to 1LSB in 3µs for a full-scale transition (Figure 4).

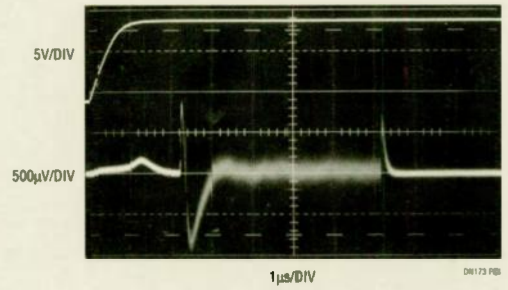

Figure 4. The LTC1595/LTC1596 with an LT1122 Settles in 3µs for a Full-Scale Change. The Top Trace Shows the 0V to 10V DAC Output and the Lower Trace Shows the Gated 3µs Settling Waveform

Precision ±10V Outputs with a Dual Op Amp

Figure 5 shows a bipolar, 4-quadrant multiplying application. The reference input can vary from –10V to 10V and V_{OUT} swings from $-V_{REF}$ to V_{REF}. Using a fixed 10V reference results in a precision ±10V bipolar output. Use a pack of matched 20k resistors (the 10k resistor is formed using two parallel 20k resistors) for good bipolar gain and offset. Substituting the LT1124 for the LT1112 provides faster settling.

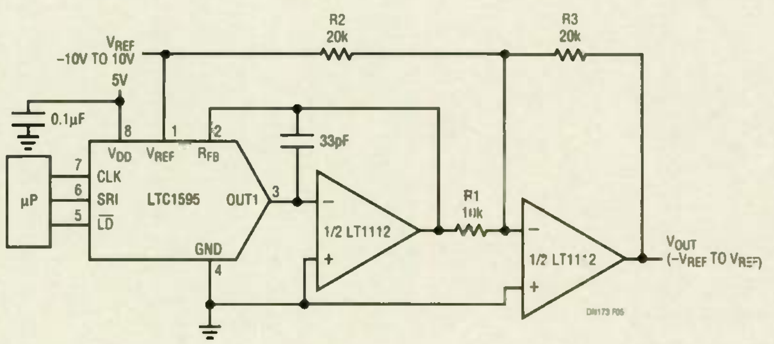

Figure 5. The LTC1595 and the LT1112 Dual Op Amp Achieve 4-Quadrant Multiplication and a 16-Bit ±10V Bipolar Output with 10V Reference

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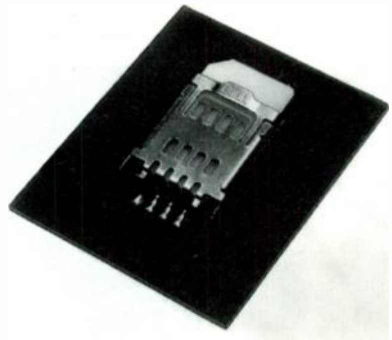
INTERCONNECTS

Ultra-Compact SIM Socket Meets GSM Standard

Measuring 2.75 by 30.6 by 17.4 mm, the ID1 is offered as the world's smallest Subscriber Identity Module (SIM) socket to date. The sockets meet the requirements of plug-in SIM cards compatible with the GSM standard and are available in standard tray packaging or embossed-type packaging for automatic mounting. Pricing is $1.39 each per 500 and delivery is from six to eight weeks.



Hirose Electric (USA) Inc., 2688 Westhills Court, Simi Valley, CA 93065; (805) 522-7958; fax (805) 522-3217. **CIRCLE 502**

High-Density Interconnect Is PCI-Compatible

The Small Peripheral Component Interconnect (SPCI) is a high-density PCI-bus interconnect that's fully compatible with the PCI standard. The 108-contact connector offers all of the benefits of a PCI card-edge connector in a PC Card package. Neither the pin header, frame, nor straddle-mount receptacle require shielding. Pricing is $3.40 for the pin header, $2.22 for the receptacle, and $0.53 for the frame. Delivery is from six to eight weeks.

AMP Inc., P.O. Box 3608, Harrisburg, PA 17105-3608; Product Information Center (800) 522-6752. **CIRCLE 503**

SMT Interconnects Come On 2-mm Grid

Available in both single- and dual-row pin header and mating sockets, this line of surface-mount connectors come with a pitch of 2 mm. The gull-wing, SIP interconnects can be ordered in lengths of three or four pins in a single row up to 2

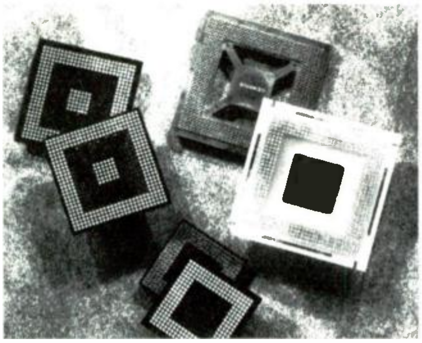
(continued on page 123)

(continued from page 122)
by 50 pins for a total of 100. Also available with pitches of 0.050 and 0.100 in., the connectors use machined brass pins and sockets plated in gold or tin. Every socket comprises a beryllium-copper multi-finger contact for compliancy and reliability. Pricing for a 50-position, tin-plated, surface-mount header is $4.70 each per 1000. Delivery is two weeks.

Mill-Max Mfg. Corp., 190 Pine Hollow Rd.,P.O. Box 300, Oyster Bay, NY 11771-0300; Sales Dept. (516) 922-6000; fax (516) 922-9253. **CIRCLE 504**

BGA Adapter Offers Alternative To Direct Attach

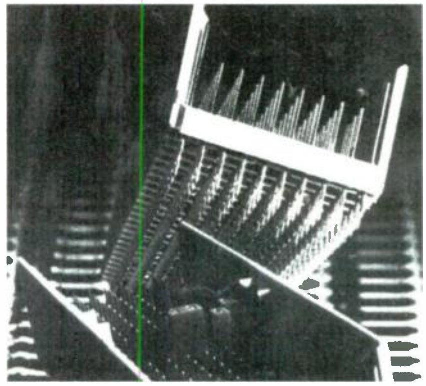
The BGA Socketing System is a dependable, field-tested method for BGA device upgrade, replacement, repair, and testing BGA devices. The system allows the BGA to be soldered to an adapter so that it can be converted to a pinned device. The system achieves a co-planarity of 0.006 in. Features include a wide range of footprints, eutectic solder balls, tape-and-reel packaging, and an optional extractor slot. Pricing is from $0.05 to $0.15 per pin.



Advanced Interconnections, 5 Energy Way, P.O. Box 1019, West Warwick, RI 02893; (800) 424-9850; (401) 823-8723; www.advintcorp.com. **CIRCLE 505**

2-mm Hard-Metric Connectors Expand To 10 Rows

Originally introduced with seven rows, the ERmet 2-mm Hard Metric Connector line has been expanded to 10 rows. Providing up to 200 signal pins and 50 dedicated ground pins in a 50-mm-long press-fit connector, the device weighs in with a total of 127 pins per linear inch. The connectors are compatible with IEC 1076-4-101/R and include CompactPCI and VME64 Extensions. Other features include three-level sequenced mating and signal rise times down to 150 ps. Pricing is $8.75 for the male connector.



ERNI Components Inc., 12701 North Kingston Ave., Chester, VA 23836; Michael Munroe (804) 530-5012; fax (804) 530-5232. **CIRCLE 506**

Surface-Mount Suppressors Handle High Currents

Designed to tackle the three-pronged problem designers face concerning EMI compliance, high current levels, and limited space, the XCB-1812 series of surface-mount EMI suppressors handle currents of 1.5, 3.5, or 5.0 A. All use multilayer technology and have impedance levels of 125 Ω at 100 MHz for the 1.5- and 3.5-A version, and 80 Ω at 100 MHz for the 5.0-A version. The maximum DCR ratings for the three devices is 0.10, 0.05, and 0.01, respectively. Measuring 4.50 by 3.20 by 1.50 mm, the devices are flow and reflow solderable and have an operating temperature range of –55° to 125°C. Pricing is approximately $0.09 each per 100,000; delivery is from stock to four weeks.

Associated Components Technology Inc., 13932 Nautilus Dr., Garden Grove, CA 92843; Erik Dieckhoff (800) 234-2645; fax (714) 636-8276; e-mail: actsales@ix.netcom.com; www.act1.com. **CIRCLE 507**

Warning Transducer Targets Automotive Applications

The TMX-12S is an audio transducer designed as a warning device for automotive applications. Providing a continuous output, the transducer features a wide frequency range and can

produce a chime output with the aid of external circuitry. The device outputs an 85-dB (min) signal at 10 cm, operates off 14 V (max), has a rated frequency of 1 kHz, and weights 10 g. Its operating temperature range is –40 to 85°C. Pricing is from $1.50 to $2.50.

Star Micronics America, Inc., 70 Ethel Rd. West, Piscataway, NJ 08854; Sales Dept. (732) 572-9512 ext.512; fax (908) 572-5095. **CIRCLE 508**

Low-Cost Radio-Frequency Transistor Is Compact

The AT-38043 is a low-cost npn silicon bipolar transistor that's ideal for use as a driver transistor in GSM Class IV as well as AMPS, ETACS, or 900-MHz NMT cellular handsets. Packaged in a 4.2-mm^2 SOT-343/SC-70, four-lead, surface-mount package, the device

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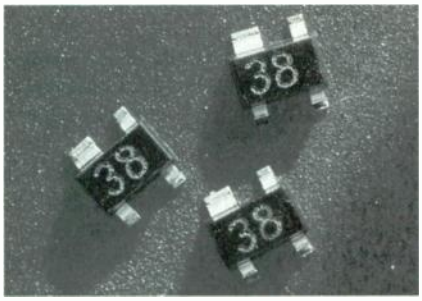
outputs up to 25 dBm of power at 4.8 V. It achieves this with 60% collector efficiency and 15-dB power gain at 900 MHz. At 3 V, the transistor provides



21.5 dBm output power and 50% collector efficiency at 1900 MHz. Pricing is $0.85 each per 10,000 to 24,999.

Hewlett-Packard Company, *3175 Bowers Ave., M/S 88U, Santa Clara, CA 95054-9929; Components Response Center (800) 537-7715, ext. 9971.* **CIRCLE 509**

High-Temperature Capacitors Snap Into Place

The KMM series of snap-in capacitors have an operating temperature range of –25° to 105°C. The devices feature a capacitance range of 39 to 3300 μF, and a voltage range of 160 to 450 V dc. Their rated lifespan depends on case size,

ranging from 2000 to 3000 hours at 105°C at the rated ripple current. The case size ranges from 20 by 20 mm up to 35 by 60 mm; the standard mounting style is a snap-in, two-terminal configuration. Three- and four-straight-pin terminal styles are available. Pricing ranges from $0.80 to $5.10, and delivery is from four to six weeks.

United Chemi-Con, *9801 West Higgins Rd., Rosemont, IL 60018; Sales Dept. (847) 696-2000; fax (847) 696-0857; www.chemi-con.com.* **CIRCLE 510**

Metal-Clad, Wirewound Resistor Handles High Power

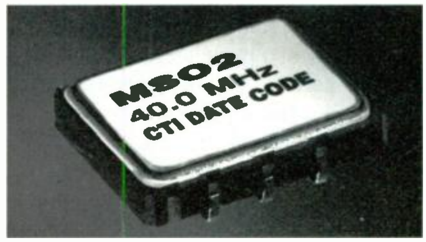
The IR-F is a wirewound, metal-clad resistor that comes in seven power ratings ranging from 100 to 500 W. The resistance range is 0.1 Ω to 5.87 kΩ and the dielectric strength is 1500 V ac —3000-V-ac and 4000-V-ac versions are available. Options include stacking

and standard or non-inductive windings. Pricing is from $36.27 each per 100 for a 100-Ω, 500-W model.

Isotek Corp., *435 Wilbur Ave., Swansea, MA 02777; Bill Poisson (508) 673-2900; fax (508) 676-0885; www.isotekcorp.com.* **CIRCLE 511**

Clock Oscillator Meets Telecom Requirements

With tight tolerances of ±20 ppm over the temperature range of 0° to 70°C, the MSO2 line of surface-mount clock oscillators suit telecommunications applications. The devices come in a ceramic package with six J leads and include an enable/disable function. Features include an operating frequency range of 1.5 to 40.0 MHz and a TTL-



/CMOS-compatible output. Pricing is $8.87 each per 1000.

Champion Technologies Inc., *2553 N. Edgington St., Franklin Park, IL 60131; Sales Dept. (800) 888-1499; fax (847) 451-7585.* **CIRCLE 512**

Circle 520

Window Comparator Features Independent Adjustments

RONALD MANCINI
Harris Semiconductor, P.O. Box 883, M/S 58-095, Melbourne, FL 32902.

Window comparators, sometimes called limit comparators, determine when the input voltage is within a preselected range. The output voltage usually goes to a TTL high when the input voltage is within this preselected range. A typical window-comparator circuit consists of two comparators with two reference adjustments—one for the low trip level and one for the high trip level. If the reference voltages are derived from the same resistor-divider string, hysteresis can't be added without having the trip levels interact. If the reference voltages are independently derived, they can drift in different directions. This causes the window to widen or possibly disappear.

The window comparator shown circumvents these problems with independent trip and window adjustments *(Fig. 1)*. The HA2841 op amp (selected because it has high-speed and low-input currents) adds the input signal to the trip voltage developed by R_T. The window width voltage (R_W) is summed into the output of the op amp as an offset voltage.

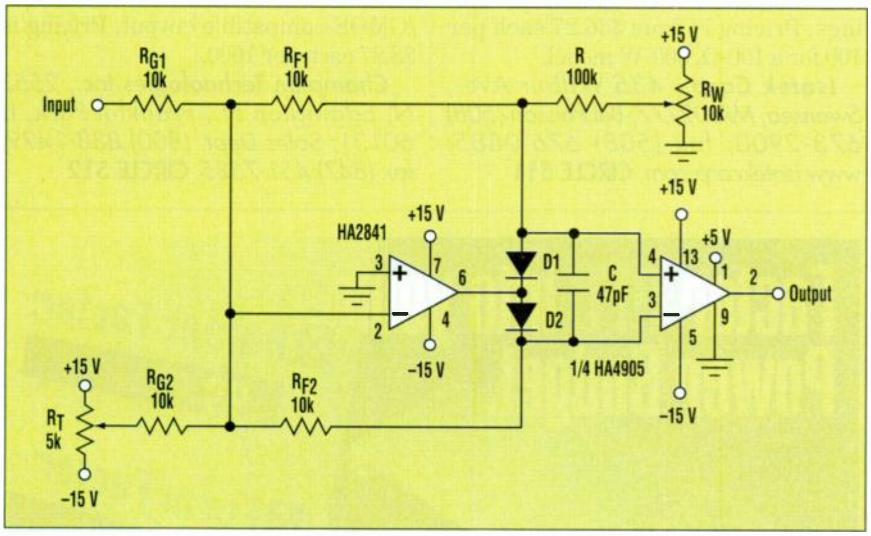
The op amp has two feedback loops, each of which contain a steering diode, D1 or D2. The high open-loop gain of the op amp ensures that one diode will always be forward-biased unless R_W supplies the feedback current. Thus, when the sum of the input voltages (closed-loop gain is one) and I_{RW} passes through zero, the current flow switches from one diode to the other. The output comparator senses the polarity switch across the diodes and the comparator output voltage changes.

The HA4905 comparator has inputs that can work from 15-V supplies. As a result, the input voltage swing is matched to the op amp's output voltage swing. Even though the input section of the HA4905 is connected to 15 V, the output section can be connected from +5 V to ground, thus offering a TTL-compatible output voltage.

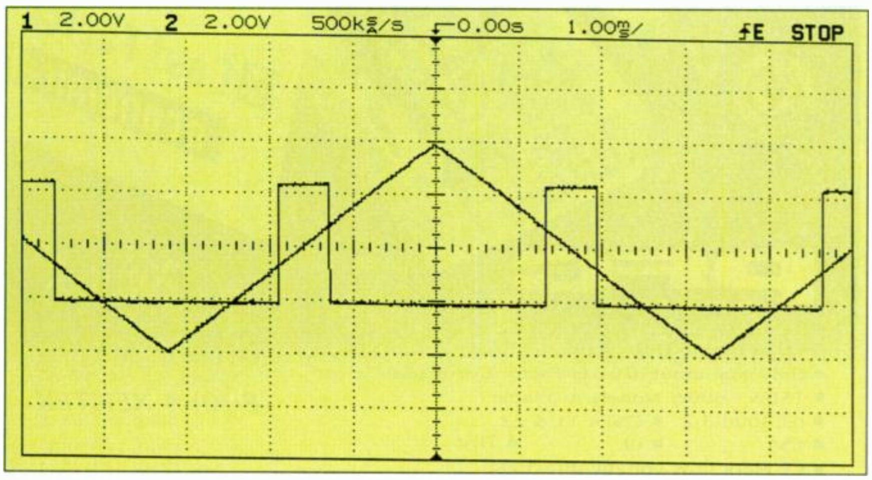
R_T sets the trip point at any point between the power supplies, and R_W sets the window width from zero, when the center tap voltage is zero, to about 90% of the input waveform. The trip point should be set first, then the window can be set to the desired width. Because the adjustments don't interact, the trip point stays constant as the window width changes.

Resist the temptation to change the comparator to an op amp. This is poor practice for any circuit that requires high-speed performance because the op-amp output would saturate, causing uncontrolled time delays. The comparator is subject to multiple switching caused by high-frequency noise riding on slow-rising input signals. This multiple switching is eliminated by the capacitor (C), which is placed across its input leads. Effectively, C couples the high-frequency noise to both comparator leads, enabling it to be rejected by the comparator's common-mode rejection capability. Notice that no multiple switching effects are occurring in the waveform *(Fig. 2)*.

This circuit yields a window comparator with independent adjustments, temperature stability, wide



1. This unusual window comparator provides hysteresis on both thresholds yet the adjustments for the upper and lower thresholds do not interact with each other.



2. These input and output waveforms demonstrate that the output waveforms don't exhibit the multiple switching effects typically produced by high-speed comparators and slow-rising signals.

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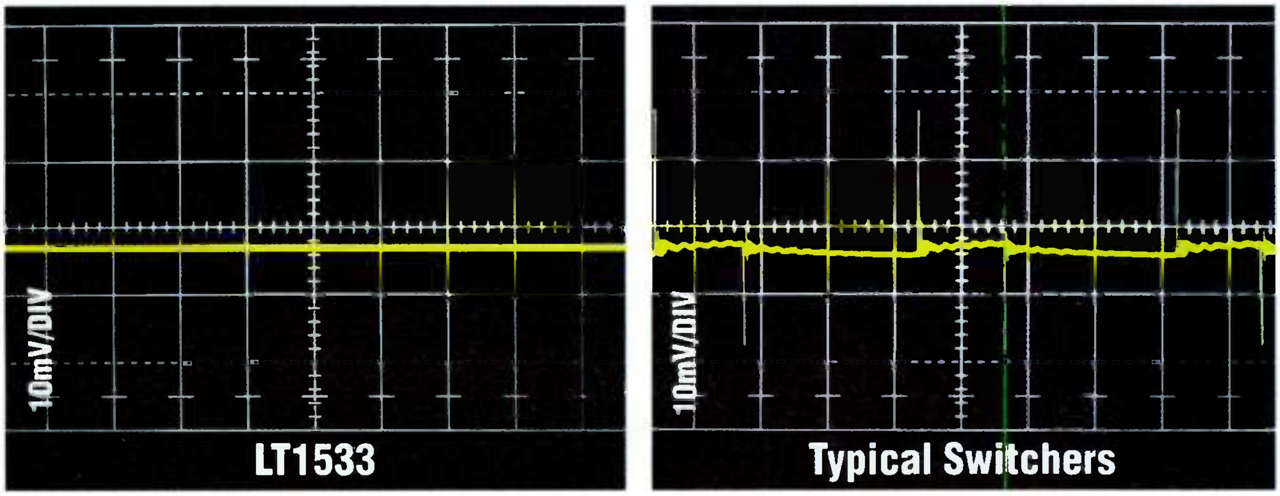

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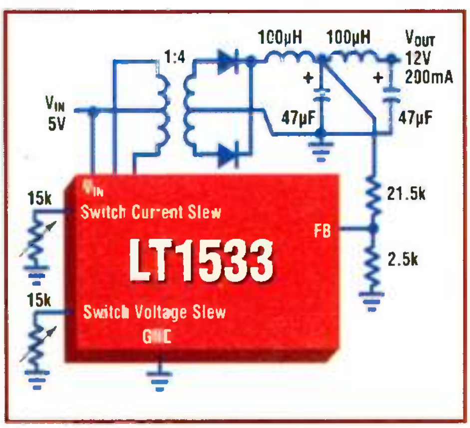

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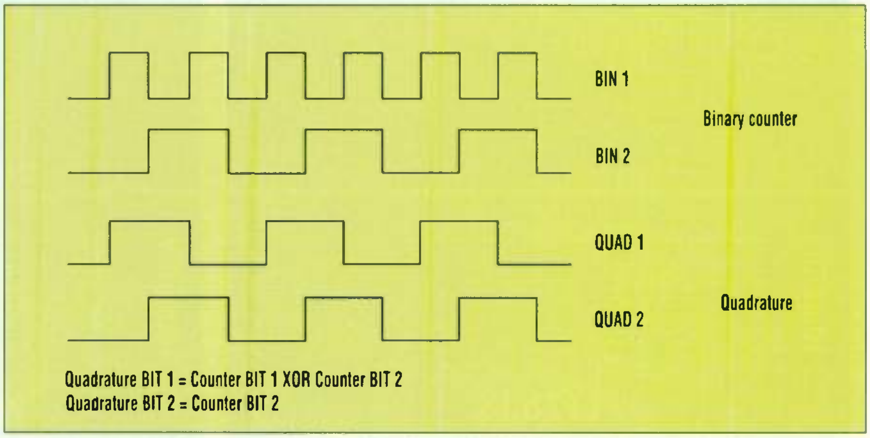
Circle 521

Single-Chip Quadrature Generator

LES WOLFF
6166 Manzanillo Dr., Goleta, CA 93117; (805) 964-1046.

A quadrature generator can be useful in a number of applications, such as motion control and signal processing. The idea presented here describes a very simple and inexpensive implementation of a quadrature generator using a single 8-pin IC, the Microchip PIC12C508 *(see the figure)*.

This also represents one of the first published examples of proven assembler code for the new PIC12C508 microprocessor, and can be used as a basis for other programs *(see the listing)*.



Just a single 8-pin IC is used in this simple implementation of a quadrature generator.

The algorithm for generating the quadrature signal is quite simple. The process is initiated by starting a free-running binary counter (COUNT) and by incrementing this register in an endless loop. Bits 1 and 2 (Bin 1 and Bin 2 in the Timing Diagram) of the 8-bit counter register are then used to directly generate the quadrature outputs.

Bin 2 of the counter is transferred directly to quadrature output Quad 2. Bin 1 and Bin 2 of the counter are then logically exclusive-OR'ed to generate the quadrature output, Quad 1. Quad 1 and Quad 2 are clocked to the output simultaneously to prevent the creation of any output glitches due to intermediate logic states.

The frequency of the quadrature outputs in this program is approximately 10 kHz, using the internal 4-MHz clock of the PIC12. The output frequency can be increased by utilizing bits 0 and 1 of the counter register. Decreasing output frequency involves either operating on the higher bits of the counter register or by adding firmware delays to the program's counter loop. A sinusoidal output can be generated by adding a low-pass filter to each of the output signals.

```
;Title:          Quadrature Generator
;File Name:      Quad2.asm
;Processor:      PIC12C508
;Clock Freq:     4 MHz
;Description:    Generates a two channel, square wave quadrature signal
;                with a frequency of about 10 kHz.
;
        processor 12C508 ; define processor
;
        #include "p12c508.inc" ; include standard assembler routines
;
        _CONFIG  _CP_OFF&_WDT_OFF&_IntRC_OSC; turn code protect off
;                                           turn watchdog timer off
;                                           select internal RC oscillator
;
; specify boot vector
;
BOOTC508      equ     0x0000  ; the 12C508 boots up at address 0x0000
;
; define memory locations of variables
COUNT           equ     009     ; free running counter
BIT1            equ     00A     ; temporary register for bit 1
BIT2            equ     00B     ; temporary register for bit 2
;
LOAD_OPTION movlw   0xDF        ; zero bit 5 of option register to
            option              ; disable timer 0 clock source

;
LOAD_TRIS movlw     0x08        ; define GPIO 0-2,4 & 5 as outputs; 3 as input
          tris      GPIO        ;
;
GEN-QUAD  movf      COUNT,0 ; load count value
          andlw     0x02    ; mask bit 1
          movwf     BIT1    ; save bit 1
          movf      COUNT,0 ; load count value
          andlw     0x04    ; mask bit 2
          movwf     BIT2    ; save bit 2
          rrf       BIT2,0  ; shift bit 2 right
          xorwf     BIT1,0  ; XOR bit 2 value with bit 1 value
          iorwf     BIT2,0  ; recall bit 2 value, OR with synthesized quadrature bit
          movwf     GPIO    ; output new quadrature value
          incf      COUNT,1 ; increment counter

     goto    GEN_QUAD

     end
```

Circle 522

Pulse-Width Measurement Made By Microcontroller With MFT

ABEL RAYNUS
Armatron International Inc., 2 Main St., Melrose, MA 02176; (617) 321-2300; fax: 617-321-2309.

The Multifunction Timer (MFT) used in low-end Motorola microcontrollers (68HC705J1A, 68HC705K1, etc.) is much more simplified when compared to its predecessors. It doesn't perform the three traditional main timer functions: Timer Overflow (TOF), Input Capture (ICF), and Output Compare (OCF). Instead, the MFT provides only the Timer Overflow feature. The absence of the Input Capture (ICF) capability, with its easily manipulated change of the positive and negative edges of the captured signal, makes accurate pulse-width measurement non-obvious.

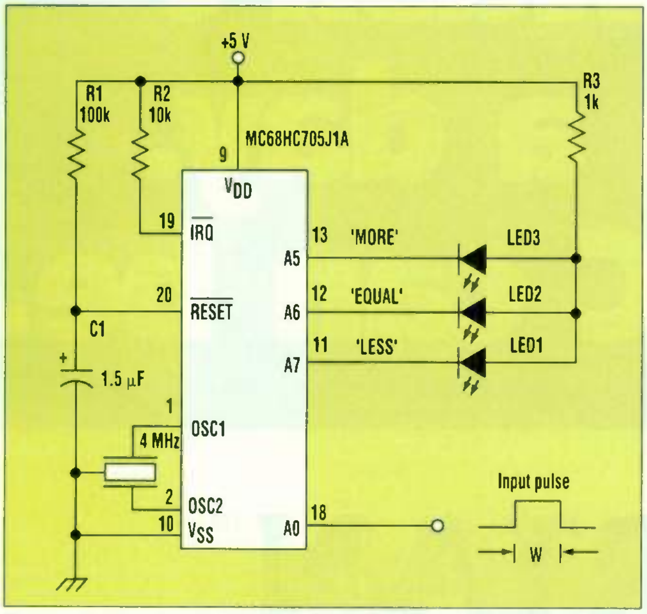
The idea described here demonstrates a way to overcome this deficiency of low-end MFT using a simple software solution. The Pulse Width Detector measures the width of an input pulse (W), compares it with the given value (W_0), and indicates the result by illuminating one of corresponding LEDs: "More", "Equal", or "Less" *(see the figure)*. The assembler program for the Pulse Width Detector is given *(see the listing)*.

The Pulse Width Detector takes advantage of the fact (unfortunately, not mentioned in all Motorola manuals) that, when Port A pins are employed as edge-sensitive external interrupt inputs, these pins can be used simultaneously as regular level-sensitive input pins.

Using this method, the measurement procedure becomes straightforward. The rising edge of a measured pulse on pin A0 causes an interrupt. The interrupt service routine activates the counter W, which counts until a high level exists on pin A0. The falling edge of the measured pulse stops the counting, and counter W contains the pulse-width information.

This kind of detector was used in Armatron's wireless data-transmission system to recognize pulse-width variations from W*TR to (W+1)*TR, where W (the contents of the counter W) = 0,1,2,....255. TR (time resolution) is determined by period of the timer W increment, which depends on the counter loop duration (9 µs) and the constant N (end of the loop condition). The time resolution should be chosen according to design objectives. In our

```
*******************************************************
* nolist
$include "std-j1a.asm"
* list
*******************************************************
        org     MOR
        fcb     %00100      ;pA0-pA3 IRQ enable
* I/O PORTS and CONSTANTS
data    equ     pA0         ;pos.edge Ext. Interrupt
LED3    equ     pA5         ;pin 13
LED2    equ     pA6         ;pin 12
LED1    equ     pA7         ;pin 11
N       equ     55T         ;Time resolution 0.5ms
* VARIABLES
        org     RAM
W       rmb     1           ;pulse width counter
T       rmb     1           ;time 0.5ms counter
* INITIALIZATION
        org     ROM
init    rsp                 ;reset stack pointer to $ff
        lda     #$fe        ;pA0 ExtInt input
        sta     ddrA
        lda     #$f0        ;set all LEDs off
        sta     prtA
        clr     W
        clr     T
        bset    IRQE, TSCR  ;ExtInt enable
        cli                 ;interrupt enable
a0      wait                ;wait for interrupt
        bra     a0
*******************************************************
ExtInt:
        clr     W
        clr     T
e0      brset   0, prtA, e1 ;High level ?
        lda     W
        cmp     #2
        beq     e2
        bhi     e3
        bclr    LEDl, prtA  ;LED1 on
        bset    LED2, prtA  ;LED2 off
        bset    LED3, prtA  ;LED3 off
        bra     e4
e1      inc     T
        lda     T
        cmp     #N
        bne     e0
        clr     T
        inc     W
        bra     e0
e2      bclr    LED2, prtA
        bset    LED1, prtA
        bset    LED3, prtA
        bra     e4
e3      bclr    LED3, prtA
        bset    LED1, prtA
        bset    LED2, prtA
e4      bset    IRQR, ISCR  ;IRQ reset
e5      rti                 ;return from ExtInt
*******************************************************
        org     VECTORS
        fdb     e5          ;Timer Interrupt unused
        fdb     ExtInt      ;set IRQ address
        fdb     e5          ;SWI unused
        fdb     init        ;set restart address
.end
*******************************************************
```



Using a simple software solution, this circuit can overcome functional deficiencies encountered using low-end Multifunction Timers (MFTs).

detector, N = 55, which yields TR= (9 µs × 55) + 0.5 µs = 0.5 ms. The maximum time measured is limited only by the number of counter W stages used.

Because this idea requires only one external interrupt pin, the techniques are usable with most microcontrollers. Other possible applications are multiwidth pulse detection, pulse-width decoding, width-to-digit conversion, and so on.

Circle 523

RS-232 Port Powers Frequency Counter

GARY SELLANI
Maxim Integrated Products, 120 San Gabriel Dr., Sunnyvale, CA 94086; (408) 737-7600.

As a source of power, the EIA-232 port has found its way into many applications unrelated to data communications—most notable being the serial mouse. An unusual innovation among RS-232-powered systems is the frequency counter, as seen in the figure. This circuit hard-limits the signal and, by driving a handshake line such as CSR, uses the resulting high/low information to trigger the interrupt of a PC's COM port. The COM port data lines aren't used because the UART framing would interfere with edge detection.

If the computer can measure the time between interrupts it can measure the signal's frequency. This technique is useful in simple telemetry, in which the frequency represents a voltage, and in more complicated situations such as the demodulation of a baseband signal from a radio receiver. Many shareware programs available on the Internet use this technique.

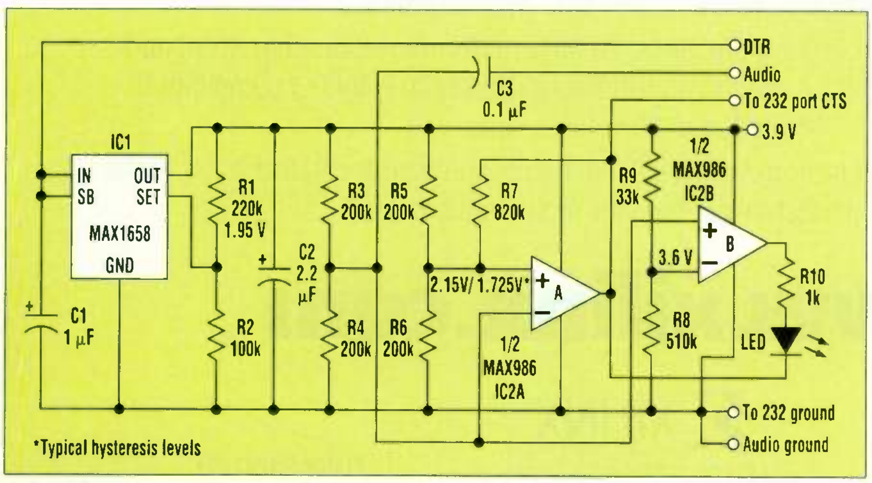
The output levels delivered by EIA-232 transmitters have scaled down over the years. Equipment has evolved from bipolar line drivers powered by external supplies to CMOS line drivers powered by on-board dc-dc converters (pioneered by the MAX232). Many of these later-generation CMOS chips meet the ±5-V specification for transmitter voltage by a margin of no more than 1 V.

The newer ICs work fine in the intended EIA-232 applications, but their minimal voltage levels pose a challenge to designers intent on stealing power for other applications. As a further complication, the frequency counter operates on 4 V, but also must withstand ±15 V (in case it gets plugged into an older PC).

The circuit shown meets all of these requirements. IC1 is a low-dropout regulator that generates a 4-V supply rail from the EIA232's DTR signal. IC1 can withstand the full 15-V transmitter voltage, and its "reverse-battery" protection can also handle the maximum negative voltage (–15 V), which eliminates the need for a blocking diode and its associated voltage drop.

IC1 powers the dual comparator IC2. Comparator "A" is used to hard-limits the input signal, and comparator "B" detects whether the signal is approaching the supply rail. Comparator "A" compares the ac-coupled audio to a pseudo-ground created by R3 and R4, and drives the EIA-232 port's CTS pin.

The comparator's output drive is sufficient to pull the EIA-232 receiver's worst-case low input impedance (3 kΩ) above the receiver's required minimum (3 V) input voltage even when powered by 3.9 V. The



By hard-limiting an audio signal, this RS-232-powered circuit enables a microcontroller to measure the time interval between transitions. Using this data, the microcontroller is able to measure the signal's frequency.

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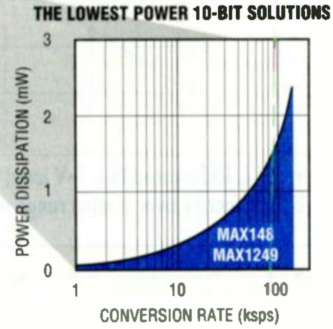

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near-ground output of comparator "A" violates the ±3-V minimum for signal levels at EIA-232 receivers, but the circuit works because the trip thresholds in these receivers are roughly TTL-compatible.

Resistors R5, R6, and R7 provide ±0.2-V of hysteresis (10% of the signal swing). If the signal reaches 3.6 V, the "B" comparator trips, causing current flow in the LED that indicates when there's excessive input voltage. Input voltages beyond the supply rail cause current flow in the protection diodes, but not false outputs from the comparators.

Most of this circuit's supply current drives either the LED or the EIA-232 input. The circuit never does both tasks at once, so the peak supply current is about 3 mA. The CMOS ICs themselves consume very little power. Typical supply currents are 30 pA for IC1 and 14 pA per comparator in IC2.

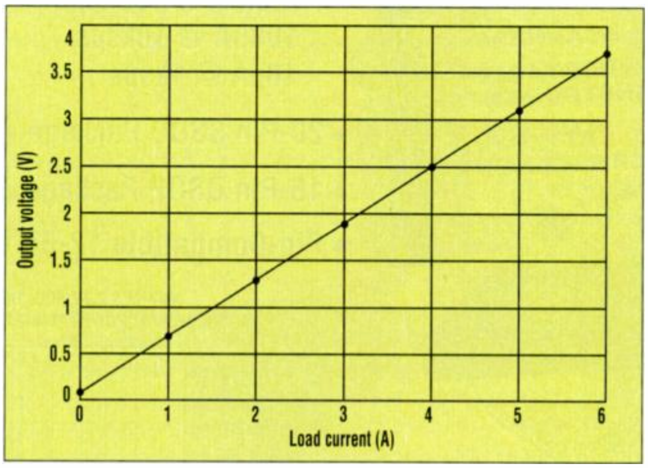
Circle 524

Battery-Charger IC Doubles As Current Sensor

CRAIG VARGA
Linear Technology Corp., 1630 McCarthy Blvd., Milpitas, CA 95035-7487.

It's always fun to try and find applications for an IC which its designer never intended. The circuit shown here is one such design. Many applications require a circuit that provides a ground-referenced output voltage that's proportional to a measured current. Frequently, the current must be measured with a shunt in the positive rail that may be well above ground and, worse yet, may vary considerably with time.

The LT1620 was originally intended as a controller for a synchronous buck regulator in battery-charger applications. In its normal operating mode, this IC mirrors a current signal down to a 5-V reference supply. By adding a single small-signal MOSFET and a few resistors around the LT1620, it's possible to again mirror this signal to provide a ground-referenced output.

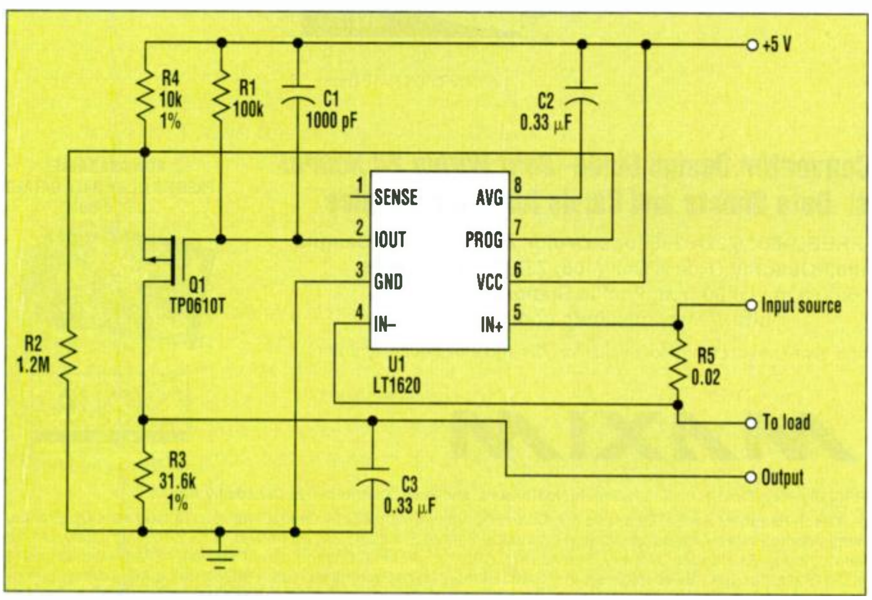


2. Referenced to a 5-V input source, the circuit exhibits excellent linearity over a wide range of load and input voltages.

Circuit operation is as follows: The LT1620 produces a voltage between the V_{CC} pin and the average (AVG) pin, which is 10 times the voltage across the sense resistor R5 *(Fig. 1)*. C2 filters this voltage. An internal op amp is provided with its non-inverting input on the AVG pin (pin 8), its inverting input on the PROG pin (pin 7), and its output on the IOUT pin (pin 2).

With the circuit connected as shown, this amplifier will force enough current through R4 to make the voltage drop on R4 equal to the voltage across C2. This current is mirrored down through R3 and filtered by C3, producing a clean, ground-referenced, dc output voltage. Resistor R2 is intended to cancel a small built-in offset in the LT1620's amplifiers. The output voltage obeys the following relationship: $V_O = I_O(R5)(R3)(10)/R4$. Changing the value of R3 allows different scale factors to be selected.

The circuit yields excellent linearity over a wide range of load and input voltages. The curve shown was measured with the sense resistor referenced to a 5-V input source *(Fig. 2)*. The curve looks the same even at inputs over 25 V, so only one curve is presented. The maximum input voltage is 36 V. There's a small offset at no load. However, in a typical microprocessor-based data-acquisition system, a simple two-point calibration is all that's required to attain excellent absolute accuracy.



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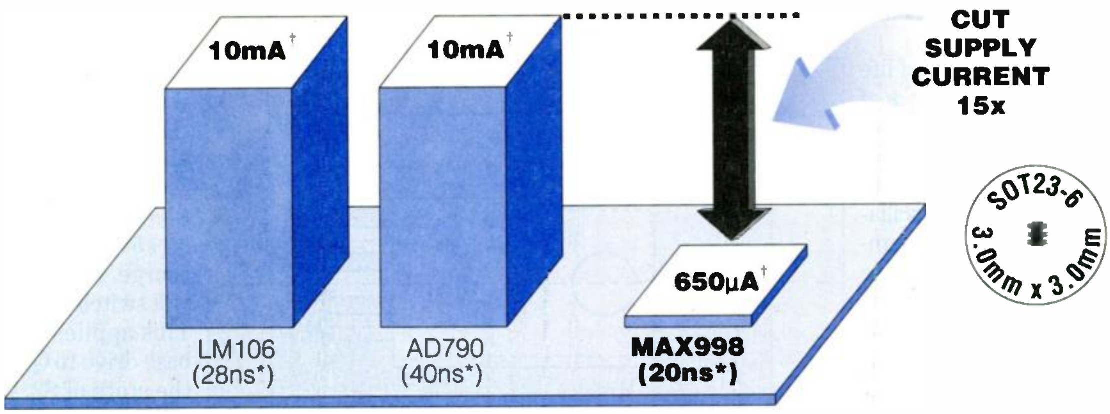

*Typical propagation delay † Maximum supply current per comparator

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Circle 525

Self-Heated Transistor Thermostats Individual Components

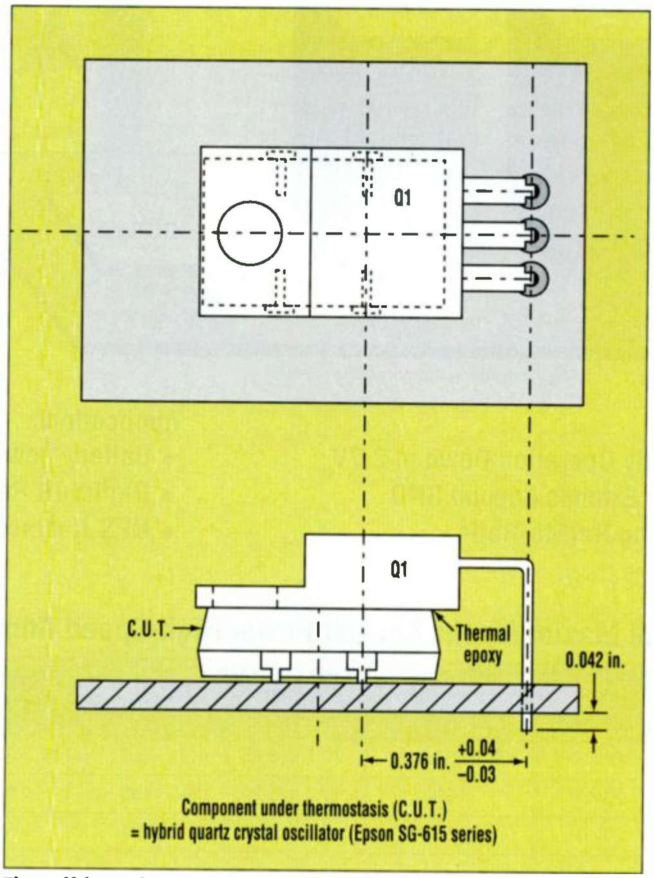
W. STEPHEN WOODWARD
Venable Hall, CB3290, University of North Carolina,
Chapel Hill, NC 27599-3290; Internet: woodward@net.chem.unc.edu.

An unavoidable fact of life is that all parameters of all electronic components drift with temperature. Even the best voltage references, op amps, crystal oscillators, etc., have non-zero temperature coefficients. These effects can be handled by compensation methods, but in demanding applications, the only solution may be controlling the temperature of the component with a constant-temperature component oven.

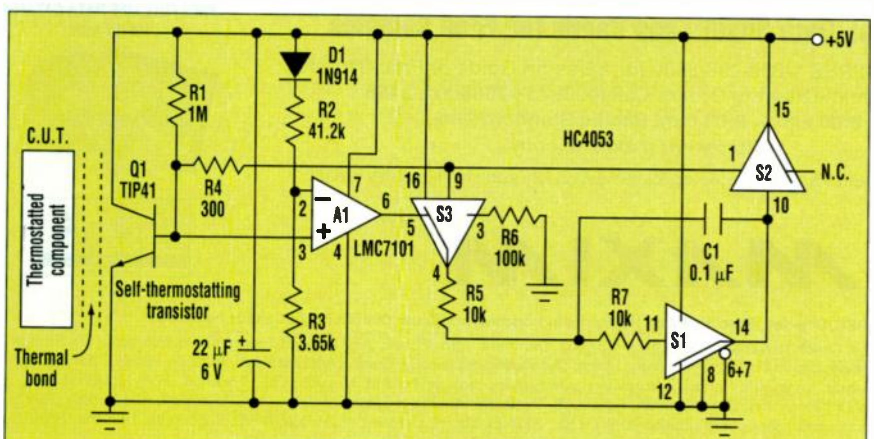
Ovens tend to be relatively large (they must be at least big enough to hold the heated part) and thirsty, so they become to difficult to fit into miniature, power-efficient designs. The idea presented here can't eliminate these problems, but it helps in minimizing both. It's based on two ideas: First, multiplexing a power transistor so it alternates between temperature measurement and heating, and thereby control its own temperature. Second, close thermal coupling (e.g., via thermal epoxy) of the transistor to the "Component Under Thermostasis" (CUT). Thus, when the transistor thermostats itself, it also thermostats the CUT bonded to it.

To follow circuit operation, first assume Q1 is slightly above set-point temperature *(see the figure)*. Then its V_{BE}, and therefore A1 pin 3, will be less than the set-point voltage at A1 pin 2, and A1 pin 6 will sit at approximately 0 V. This holds the multivibrator S1 pin 11 low. S1 pin 14 also will be low, and S2 will be OFF, so no base drive flows to Q1. Q1 will gradually cool until the relationship at A1's inputs reverses. A1 pin 6 then will go to +5 V and C1 will start to charge. About 700 µs later, S1 will switch ON, turning S2 on. This applies about 10 mA of base drive to Q1, and reverses the state of S3, which begins the discharge of C1 through R6. This state lasts for approximately 10 ms and deposits about 0.05 joules of heat in Q1. C1 then recharges and the cycle repeats until Q1 returns to set point, thus establishing a feedback loop that tends to hold Q1's base-emitter junction at a constant temperature, which is roughly 55°C for the circuit values shown.

Just because Q1's junction temperature stays constant doesn't mean the CUT's does! In fact, the inevitable thermal resistance of the bond between Q1 and the CUT will allow some "playthrough" of ambient temperature variations into the CUT's temperature. D1 serves to compensate for this effect by effectively increasing Q1's set-point temperature by about 1°C for every 14°C decrease in ambient temperature. For the typical case of an eight-pin DIP package bonded to Q1, this does a good job of canceling heat loss and holding the CUT's temperature "rock" steady. Even without any special effort at insulation, the small size of the Q1 + CUT assembly, and near 100% efficiency of Q1 as a heater, hold power demand to about 700 mW against a 25°C ambient. Warm-up takes less than one minute.



This self-heated transistor helps to minimize the problem of components that drift with temperature by "thermostatting" them.



A power transistor is used to perform both heating and temperature measurement functions.

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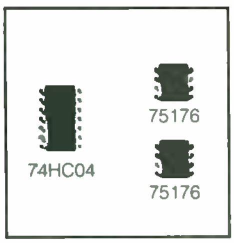

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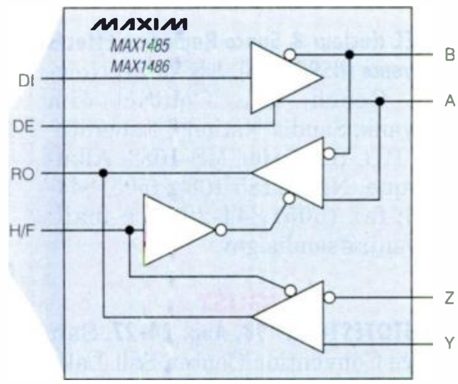

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JULY

IEEE Power Engineering Society Summer Meeting, July 12-16. Sheraton San Diego Hotel & Marina, San Diego, CA. Contact Terry Snow, San Diego Gas & Electric, P.O. Box 1831, San Diego, California 92112; (619) 696-2780; fax (619) 699-5096; e-mail: t.snow@ieee.org.

SPIE's Annual Meeting & Optical Instrumentation Show, July 19-24. San Diego, California. Contact SPIE Exhibits Dept., Post Office Box 10, Bellingham, Washington 98227-0010; (360) 676-3290; fax (360) 647-1445; e-mail: exhibits@spie.org.

IEEE Nuclear & Space Radiation Effects Conference (NSREC '98), July 20-24. Newport Beach, CA. Contact Jim Schwank, Sandia National Laboratories, P.O. Box 5800, MS-1083, Albuquerque, NM 87185-1083; (505) 844-8376; fax (505) 844-2991; e-mail: schwanjr@sandia.gov.

AUGUST

AUTOTESTCON '98, Aug. 24-27. Salt Palace Convention Center, Salt Lake City, UT. Contact Robert Myers, Myers/Smith Inc., 3685 Motor Ave., Suite 240, Los Angeles, CA 90034; (310) 287-1463; fax (310) 287-1851; e-mail: bob.myers@ieee.org.

SEPTEMBER

ICSPAT & DSP World Expo, Sept. 13-16. Toronto Metro Convention Center, Toronto, Ontario, Canada. Contact Liz Austin, Miller Freeman Inc., (888) 239-5563, (415) 538-3848, e-mail: dspworld@mfi.com; www.dspworld.com.

OCTOBER

The Vision Show, Oct. 6-8. San Jose Convention Center, San Jose, CA. Contact Automated Imaging Association (AIA), 900 Victors Way, P.O. Box 3724, Ann Arbor, MI 48106; (313) 994-6088; fax (313) 994-3338; e-mail: kerickson@automated-imaging.org; www.automated-imaging.org.

IEEE International Conference on Systems, Man, & Cybernetics, Oct. 12-14. Hyatt Regency La Jolla, La Jolla, CA. Contact M.A. Jafari, Dept. of Industrial Engineering, Rutgers University, P.O. Box 909, Piscataway, NJ 08855; (908) 445-3627; (908) 445-5467; e-mail: jafari@gandalf.rutgers.edu.

NOVEMBER

Embedded Systems Conference, Nov. 1-5. San Jose Convention Center, San Jose, CA; Contact Liz Austin, Miller Freeman Inc.; (888) 239-5563; (415) 538-3848; e-mail: esc@mfi.com; www.embedded.com.

Photonics East & Electronic Imaging International Exhibition, Nov. 1-6. Boston, MA. Contact SPIE Exhibits Dept., P.O. Box 10, Bellingham, WA 98227-0010; (360) 676-3290; fax (360) 647-1445; e-mail: exhibits@spie.org.

Voice, Video & Data Communications Conference & Exhibition, Nov. 1-6. Boston, MA. Contact SPIE Exhibits Dept., P.O. Box 10, Bellingham, WA 98227-0010; (360) 676-3290; fax (360) 647-1445; e-mail: exhibits@spie.org.

IEEE Global Telecommunications Conference (Globecom '98), Nov. 9-13. Sydney, Australia. Contact Sam Reisenfeld, School of Electrical Engineering, University of Technology, Sydney, P.O. Box 123; Broadway, NSW 2007, Australia; +61 2-330-2435; e-mail: samr@trnasmit.ee.uts.edu.au.

DECEMBER

12th Systems Administration Conference (LISA '98), Dec. 6-11. Marriott Hotel, Boston, MA. Contact USENIX Conference Office, 22672 Lambert St., Suite 613, Lake Forest, CA 92630; (714) 588-8649; (714) 588-9706; e-mail: conference@usenix.org; www.usenix.org.

JANUARY 1999

Annual Reliability & Maintainability Symposium (RAMS), Jan. 19-21. Washington Hilton, Washington, DC. Contact V.R. Monshaw, Consulting Services, 1768 Lark Lane, Cherry Hill, NJ 08003; (609) 428-2342.

IEEE Power Engineering Society Winter Meeting, Jan. 31-Feb. 4. New York, NY. Contact Frank Schink, 14 Middlebury Lane, Cranford, NJ 07016; (908) 276-8847; fax (908) 276-8847.

FEBRUARY 1999

Photonics West, Feb. 6-12. San Jose, CA. Contact SPIE Exhibits Dept., P.O. Box 10, Bellingham, WA 98227-0010; (360) 676-3290; fax (360) 647-1445; e-mail: exhibits@spie.org.

IEEE International Solid-State Circuits Conference (ISSCC '99), February 15-17. San Francisco Marriott, San Francisco, California. Contact Diane Suiters, Courtesy Associates, 655 15th St., N.W., Washington, DC 20005; (202) 639-4522; fax (202) 347-6109; e-mail: isscc@coutesyassoc.com.

Portable by Design, February 21-25. Santa Clara Convention Center, Santa Clara, California. Contact Rich Nass, Electronic Design, 611 Route 46 West, Hasbrouck Heights, New Jersey 07604; (201) 393-6090; fax (201) 393-0204; e-mail: portable@class.org.

The Wireless Symposium and Exhibition, February 21-25. San Jose Convention Center, Santa Jose, California. Contact Bill Rutledge, Penton Publishing, 611 Route 46 West, Hasbrouck Heights, New Jersey 07604; (201) 393-6259; fax (201) 393-6297; instant faxback (800) 561-7469; www.penton.com/wireless.

MARCH 1999

Southeastcon '99, Mar. 25-29. Marriott Resort Hotel, Lexington, KY. Contact Don Hill, 1676 Donelwal Dr., Lexington, KY 40511-9021; (606) 257-8487; fax (606) 323-1034; e-mail: d.w.hill@ieee.org.

MAY 1999

IEEE/IAS Industrial & Commercial Power Systems Technical Conference (I&CPS), May 3-6. Nuggett Hotel, Sparks, NV. Contact Kerry Flannigan, Sierra-Nevada Power Co., P.O. Box 10100, Reno, NV 89520; (702) 689-4848; fax (702) 689-4139.

JUNE 1999

IEEE/MTT-S International Microwave Symposium (MTT '99), June 13-18. Anaheim, CA. Contact Robert Eisenhart, 5982 Ellenview Ave., Woodland Hills, CA 91367; (818) 716-1995; fax (818) 713-1161.

JULY

IEEE Power Engineering Society Summer Meeting, July 18-22. Edmonton, Alberta, Canada. Contact Dave Fraser, Edmonton Power Capital Square, Edmonton, Alberta, T5J 3B1, Canada; (403) 448-3554; fax (403) 448-3192.

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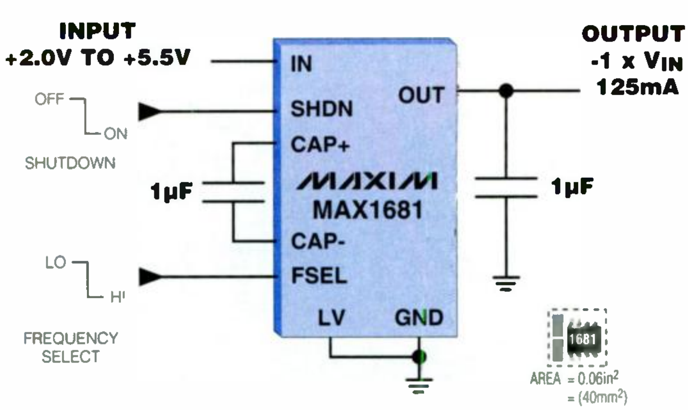

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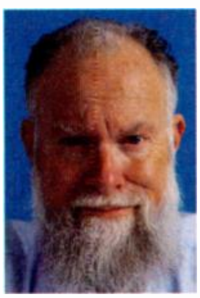
BOB PEASE

What's All This Motorcycling Stuff, Anyhow?

Once upon a time, in the era 1950 to 1960, I rode my bicycles a lot. I probably rode 20,000 miles or more. Heavy old bicycles, light touring bikes, racing bikes. Track machines with a single fixed gear and no free wheel. Tandems. I knew how to handle a bicycle pretty well. But I knew nothing about motorcycles. I never even rode a motorcycle—until three days ago.

I noticed some signs when I was in Kathmandu, in April of 1996: "Motorbikes for Rent." But I did not ask about the details. This year, I decided to inquire. In Pokhara, a guy quoted me a price of 300 rupees per day. But I was just curious; I was not going to rent a motorbike there. After our successful trek, when I got back to Thamel (the tourist area of Kathmandu), I went up the main street from our hotel (the Potala Guest House) toward the top of the hill. There was a big sign, "Honda Motorbikes, 250, 125, 50 cc for Hire." I inquired. The guy had no 50 or 125 ccs, but only 250 ccs, and he said they were 1200 rupees per day. That's 20 bucks! Not cheap, and I told him so, and walked out.



BOB PEASE
OBTAINED A BSEE FROM MIT IN 1961 AND IS STAFF SCIENTIST AT NATIONAL SEMICONDUCTOR CORP., SANTA CLARA, CALIF.

Then at the top of the hill, I inquired, and they had a rate of 500 rupees for a Yamaha. I figured I could live with that price—$8 per day. The fact that I had never ridden a motorcycle before was not a concern. I could do some on-the-job training. No problem. After all, a clutch is a clutch, right? And a cycle is a cycle. I knew I could handle THOSE details. After that, I wasn't going to sweat the small stuff.

They held my passport as security—they didn't deal with credit cards. They didn't pay much attention to my driver's license, though they did look at it. Then, they helped me get the engine started. I figured out which lever was for the clutch, and which one for the brake.

NOTE: When I was a kid, the right-hand brake on a bicycle was always the front brake, and I liked that, as my right hand was stronger, and I could control the braking best with my right hand on the front brakes. More recently I have been finding that, alas, most new bicycles have the front brakes controlled by the left-hand brake lever. Why the change? I assumed that was because motorcycles have the front brakes controlled by the left-hand lever. WRONG. Motorcycles use the right hand for the front brakes. The left hand is used for the clutch. Minor surprise. (Why did bicycles change?)

Also, I immediately found that even though the signs said "Motorbike," this was a real motorcycle. The speedometer went all the way up to 120 km per hour (though I did not). Even though its engine was just 135 cc, it was a full-sized machine, and it probably weighed 250 lb. Fortunately, I'm a big, strong guy, and did not have any trouble keeping my balance.

I started down the streets of North Thamel, and the manager came along by bicycle to show me where I should buy some gas, because the fuel tank was empty. I filled it up with about $6.40 for 10 liters. Then I started north for the Ring Road.

Anybody who has never been to Kathmandu might think that its "Ring Road" is a circumferential road like Route 128 around Boston, or the Ring Road (motorway) around London, a divided highway, limited access, with two or three lanes in each direction. Not quite so. This road is about three lanes wide, TOTAL, and is usually filled with at least four lanes of traffic. Often, a truck will go to pass a bicycle, and a motorcycle will go to pass the truck, and a sedan will honk to pass as soon as he can get his passing lane. And what if the oncoming traffic consists of a bus passing a bicycle passing a water-buffalo? All in three lanes? (Not to mention an occasional wandering cow or a herd of goats.) Let's just say that the traffic on Kathmandu's Ring Road has no relationship to any traffic pattern in the USA or Europe.

However, when the Ring Road was NOT full, it was one of the widest, straightest, and smoothest roads in the whole valley. Later I got the little Yamaha into fourth gear, and wound it out to 50. Wow, that seemed really fast! Then I realized it was 50 km per hour, barely 33 mph. But that was still plenty fast for me. I never did find any roads long enough, straight enough, or empty enough for me to push it up above 45 mph.

I chose some less-travelled roads to get out to the Ring Road, and as I went, I learned how to ride that cycle. I discovered how to shift, and how to use the front and back brakes. And, how to use the horn. I never did find out how to get it surely into neutral. The procedure that seemed to work sometimes, did not work ALL the time. But, no harm.

I never did figure out how to operate my camcorder while riding. It's too bad—and it's also probably a good thing, not to try to do two complicated things at once.

My primary objective that day was to go to Nagarkot, which is a small town on a high ridge about 20 km northeast of Bhaktapur, which is 10 km southeast of Kathmandu. This place is supposed to have a good view of the mountains. I wandered southeast around the city until I hit the electric, trackless trolley lines going to Bhaktapur. Then, I went down along that road to the east. After a while I jogged off to the north, and then cut back east, to take the road toward Nagarkot. It was actually well marked by a sign in English, "Nagarkot, 20 km." The road started out fairly straight, through pleasant farmland, and then started curving up through the foothills. I had to pay a little bribe when some local guys put a rope across the road. They were raising funds to finance a local recreation center. I also had to pay a toll of 2 rupees (3 cents) to go up the road to Nagarkot. The road was not narrow, not scary, not bumpy, and not steep. It was sort of like Mt. Hamilton Road in San Jose—upgrades and curvy, with not a lot of traffic.

After a few villages, I began to get good views. But rather than stop early and take pictures, I decided to go up to the top and take pictures, then take more on the way down. There were several tourist hotels and restaurants that were advertising themselves as I came into the town of Nagarkot. I just kept going up through pastures and then forests.

Soon I was following only one other motorcycle. The road turned from good tar to dirt. He kept going. I followed. The road got a little steeper, and a little rougher, and I had to use good judgement to pick a route up the rough road. Sometimes I followed the other bike, and sometimes he let me go ahead.

I learned, as I went, how to make a motorcycle go up a fairly steep hill. I must say, even at 6 or 8 mph, that little Yamaha had pretty good guts and torque. In general, it would not quit. All I had to do was keep applying a lot of throttle and keep it steering around the worst bumps and ruts.

After about a mile, I was near the top, as it leveled off, and I could see the summit tower. I came around a corner—and there were a dozen big buses, a dozen cars, and a few dozen motorcycles, all parked. It was NOT the end of the road, but the road did start down to the south, and I did not want to go farther. I parked, and took a walk. There were many people, sightseeing and picnicking on the Saturday afternoon.

The summit area was quite brushy and wooded. I followed several small trails. At first I thought I might have sneaked through small trails to an area where a fee was required, but later I found that was not so. There was an area with a small (40-ft.) fire tower. I did not go up there, as maybe a fee or ticket was required. I took some pictures from the heliport area.

The complete facade of the Langtang peaks and a great continuous wall of peaks to the north, northeast, and east was quite glorious, (Raamro). And the great peaks in the northwest, Ganesh Himal and Manaslu also were beautiful. Even though the day had started fairly hazy down in Kathmandu, it was quite clear up there. I gazed off to the east—a GREAT wall of mountains. Later I learned that Mt. Everest is visible amidst the far eastern peaks. But it is not very high on the horizon, as it is so far away that peaks that are closer appear higher.

I took several photos with my 35-mm camera, some views with my camcorder, and finished off the last few shots on my panoramic camera. THEN, I noticed the views of the Annapurnas and of Dhaulagiri in the far west. The Annapurnas stood as spires; Dhaulagiri was like a big wall, probably 80 miles away. As I had been studying its visage from close up for a week, I recognized it instantly. (The view of Dhaulagiri was good from the top of the hill at Nagarkot, but not from down in the town.)

But now I have no question that one can see HUNDREDS of kilometers in various directions from Nagarkot. Even if you do not rent a motorcycle, you can easily hire a taxi to take you out to Nagarkot for a half day. A rate of about $50 would not be bad if split between two or three people. But for best viewing, you should plan to get there for daybreak, and the early morning viewing when the clouds are less likely to hurt your views.

Could you actually arrange to hire a taxi at 4 a.m. and get out to Nagarkot by daybreak? Maybe, maybe not. You could always ask. You might have to go out in the evening and stay overnight. There are inexpensive buses, if you are not in a hurry.

My primary reason to rent a motorbike was NOT just to duck the high price of car rental in Nepal. In Nepal, as in other Asian countries, renting a car includes the hire of a driver. Hertz or Avis will cheerfully rent you a car (with driver), at rates of perhaps $100 to $200 per day. Last year, I decided to hire a taxi from a good guy named Gobal for an all-day 200 km trip to the Tibet border at Kodari. I specifically hired this guy with his taxi because I had ridden with him, and he was careful, thoughtful, and considerate, which I cannot say of all drivers in Nepal. It was a very good trip, and $80 covered the whole day. If you want to hire a good driver, go to the Potala Guest House and ask for Gobal.

But, I was not just trying to avoid cars, drivers, or costs. I wanted to rent a motorbike for the adventure, to see what would happen. Nepal is an amazing place. Especially if you are open to opportunities as they arise.

I rode back down to Thamel. The rental place was surprised and delighted to see their machine in one piece, as they obviously expected this KLUTZ to wreck their motorcycle. I told them I wanted to rent it the next two days. On Sunday I rented it again, but I only rode a few miles, downtown to buy some glasses, and then up to Batbhateni to talk with some engineers at Lotus Energy.

On Monday, I got an early start at 6:45 a.m., to avoid the heaviest traffic. I drove far south along the Ring Road to get to the small town of Beresshi, and continued up to St. Xavier's School. Peter Owens (of the trek) had told me that one could go up a road to the hill of Pulchowki, which means, Place (Chowk) of Flowers (Pul). He did not caution me how rough the road was, only that it went up to 9,000 feet, with a great outlook over the valley.

So, up I went. The road was alternately paved and gravel, and then with loose stones. It was not really very STEEP, but it was not an easy road. Any good car with good ground clearance (even my VW Beetle) could have easily made it up, but the motorcycle had problems as it kept bouncing over the loose rocks. It was not very stable at all.

I discovered out that just trying to STEER was not very effective, as the wheels were (effectively) not on the ground. But using my feet to dab at the ground worked pretty well. All the while, I toiled up the hill, at nearly full throttle, at 5 mph. I had to stop and back down a couple times, and then restart to go up. I saw no other vehicles or people on the way up, but at the top I met a family with six children and two kids. When they tied the small goats to the Hindu shrine at the top, I pieced together why THEY were there.

I walked around the top. There was an antenna farm for radio and TV, as

well as Hindu and Buddhist shrines. Again, the view of the mountains was very impressive, though not quite as clear as the previous days. But the valley was hazy, and looking over it was quite interesting. I could see across to Nagarkot where I had been two days earlier.

The descent was not easy, but I used my rear brakes A LOT, my front brakes a little, and got down OK. On the way down I saw three other motorcycles going up, and each seemed to have some struggles. I could see places with gravel torn up as they tried to get going on the steep upgrade. Note: In 13 km (40,000 ft.) the road ascends about 3000 ft—plenty steep enough. There also is a hiking trail that is much shorter and more direct, but it would have taken me ALL DAY, to hike it.

As I descended the paved road through Beresshi, I heard several noisy mills where polyester fabric was being woven. There are more than two dozen looms in little old brick buildings. I never saw any such looms in any other area of Nepal.

By this point I was very weary of sitting, and went back to my hotel. I went to Lakshminarayanan's Restaurant, and ordered a beer and some Chinese Chop Suey. (The menu said chopusy, but I knew what they meant.) Then I took a nap, three hours.

Later, I went down to New Road to pick up my new glasses, and up to Lotus Energy to pick up my modified Khukri knife and sign off some paperwork. Then I returned the motorcycle to the rental place.

When they inquired, I merely told them that I had gone up to Trisuli Bazaar. They were impressed. I mean, I didn't want them to think that I had trashed their bike. I also didn't want to explain why I took it up Pulchowki.

But when I told Peter, Jai, and Buddi that I had ridden the motorbike up Pulchowki, they were really impressed. Jai could not quite believe that I had never ridden a motorcycle before, yet had ridden up Pulchowki. But that's the truth. I have the pictures to prove it.

I wouldn't recommend this to everyone—that they learn to ride a motorcycle in Nepal. As I have ridden many thousands of miles bicycling, under every difficult condition, I had had some preparation. Because I know how to slip my clutch by foot, I could figure out how to do it by hand, too. As I knew how to navigate around Kathmandu by sight, and by memory, I did not get lost too often. That's a good thing, as there are almost no street signs in Kathmandu. In fact, most of the streets do not even have any names. So I just navigated by internal guidance. (But I also had good maps.) And, as I was a student of the traffic in Nepal, I figured out that riding smoothly and steadily, even though I could not be aware of all the traffic bearing down on me, meant I had a chance to not get run over. And I also knew enough, not to take chances.

On Sunday evening we were going over to supper at a restaurant in the Thamel area, Thamel House. Of course, this was a building without a number, on a street without a name. Jeevan said, "I could direct you to get to the right place if I ride behind you." I replied, "Maybe so, but I would NOT recommend this, as I want you to get there ALIVE." So I drove over on my own and had no trouble finding the place. The weight of another rider swaying around behind me was a new experiment I did not want to take! Not at night. Not with a guy whose life I valued.

So much for experiments. I learned a lot. I did not kill myself, nor cows, chickens, pedestrians, or bicyclists. Though I might have scared a few of each.

And now that I am back in California, am I going to take up motorcycling or buy a cycle? Absolutely not. Much too dangerous!

All for now. / Comments invited!
RAP / Robert A. Pease / Engineer
rap@webteam.nsc.com—or:

Mail Stop D2597A
National Semiconductor
P.O. Box 58090
Santa Clara, CA 95052-8090

P.S. A friend of mine suggested that people who want to take up motorcycling without killing themselves should read *Motorcycling Excellence: The Motorcycle Safety Foundation's Guide to Skills, Knowledge, and Strategies for Riding Right*. It costs about $25. I have just ordered a copy, ISBN 1-884313-01-9, and I am going to read it.

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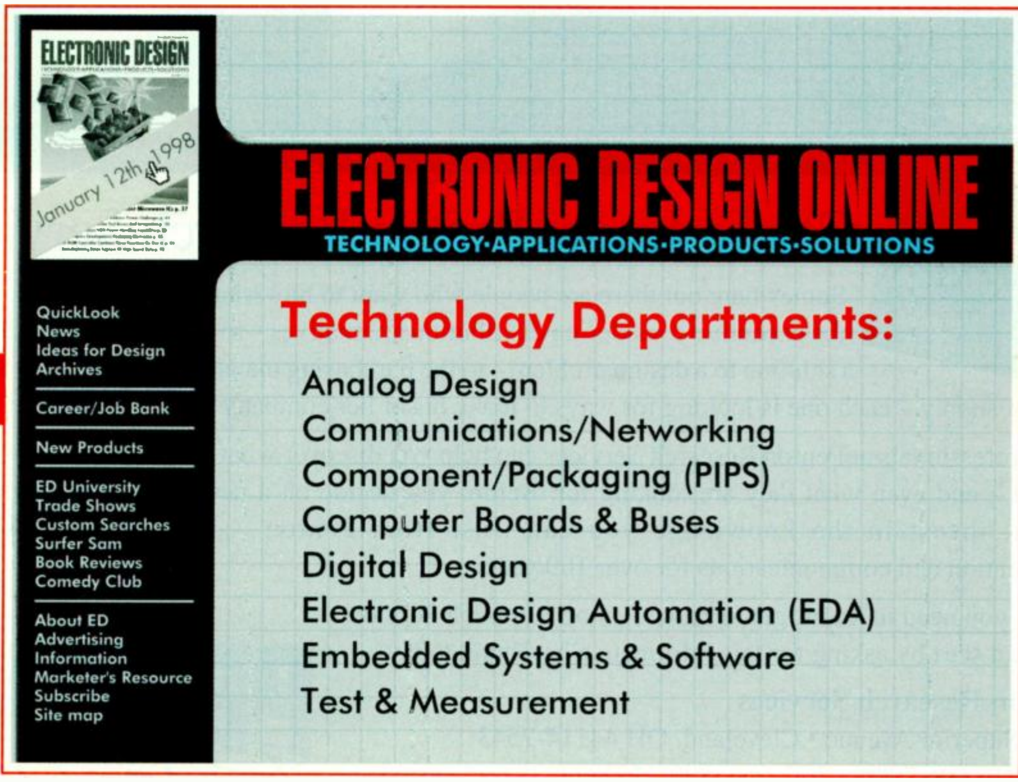

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Add Some Spice To Your Analog Designs

This month's column takes a look at some books with high EE interest, specifically a couple on Spice (Simulation Program with Integrated Circuit Emphasis).[1] As the name implies, Spice was originally developed specifically for IC design, but has long since been used much more generally. Today, the many Spice variants are considered general-purpose electronic circuit design tools, but they are also used in broader ways, such as control system design.

Without question, the capabilities of early Spice simulators have been greatly enhanced. Spice today provides many powerful and useful features, such as Monte Carlo and worst-case analysis, circuit optimization, sophisticated display, and graphical output features, etc. Currently, some simulation packages go so far as to offer a completely integrated design *program suite*. They include schematic capture and pc-board layout tools, in addition to the basic simulator. And, quite obviously, any simulator's performance is tied directly to the power of the host machine, a factor which provides today's 300-MHz-processor machines with some potent computational savvy.

Surely it behooves the wide-awake designer to be fully aware of this simulation power, so as to best harness it for his/her designs. This awareness, in turn, implies some measure of understanding of how Spice and Spice-like simulators work. And, here's where the well-focused and well-documented experiences of others can aid greatly.

Spice books: If you are like me, you've probably noticed that there are a lot of books out there on Spice and Spice-related simulators. You may also have wondered just which books are the good ones. I, myself, have wondered those same thoughts, and have spent money on Spice books, not always finding a full measure of satisfaction. Nevertheless, I hope the Spice books described here are ones that you'll find useful.

Ron Kielkowski of RCG Research Inc., has been presenting a series of three-day workshops on MicroSim's PSpice since 1993, and he seems to have furnished at least some of the answers.[2] He has written two Spice-related books, which are oriented to the SPICE2G.6 version, the most widely used (and also the last Fortran-based) Spice release from the University of California at Berkeley. They are reviewed below.

Inside SPICE: Overcoming the Obstacles of Circuit Simulation, 1994, ISBN: 0-07-911525-X, is a $50.00, 188-page, 6- by 9-in. hardcover book with six chapters, 200 illustrations, an index, and a 3.5-in. floppy diskette with programs. It is available from McGraw-Hill [*www.mhhe.com/engcs/electrical/*, or (800) 262-4729].

SPICE: Practical Device Modeling, 1995, ISBN: 0-07-911524-1, is a $55.00, 272-page, 6- by 9-in. hardcover book with six chapters, five appendices, 302 illustrations, an index, and a 3.5-in. floppy diskette with programs. It is also available from McGraw-Hill.

WALT JUNG

Both of Kielkowski's books simply radiate the fact that he is deeply involved with his topics, and knows them thoroughly. One clear example of this is the fact that he distributes his very own 32-bit, PC-compatible SPICE2G.6 program along with the two books. This program is RSPICE, as well as RGRAPH, a graphical processor. These programs and other specialized utilities are used as live demos, in conjunction with the book, and illustrate the various points made within the text.

The six chapters of *Inside SPICE* include: "What is Spice?," "Understanding Circuit Simulation," "Nonconvergence," "Numeric Integration, Timestep Control," and "Spice Options." Kielkowski does a good job of stating this book's raison d'être, both in the preface and first chapter, and indeed, throughout the book. Simply stated, Spice can be extremely difficult and frustrating when the reasons behind a failure to run or a nonconvergence aren't at all obvious. As the saying goes, "Not user-friendly." In fact, a balky Spice program can evoke a feeling that all such computer operations are best left to masochists.

But, the goal of a design simulation is to learn more about how a circuit performs. Sometimes it may take further effort on the part of the designer to first learn how the simulator works. At which point, he or she is better equipped to give it the correct input, so that Spice can then produce the expected and desired output.

This is the basic premise of *Inside SPICE*, that is, once you better understand how Spice works internally, you'll be much better able to make it do your bidding. You can then avoid the "obstacles," which are those items Kielkowski lists as often causing simulations to fail. These are the topics of Chapters "Nonconvergence," "Numeric Integration," and "Timestep Control."

As a preface to appreciating nonconvergence, Kielkowski discusses the matrix math operating basis of Spice in Chapter 2, "Understanding Circuit Simulation," and how nonlinear elements, in particular, influence convergence sensitivity. With this background, the reader is ultimately ready to absorb the topics of the three obstacle chapters, and more fully appreciate all of the user-adjustable Spice settings which can influence a simulation. The book concludes with a chapter on the various Spice option settings that are available.

One should appreciate that this Spice book goes far beyond a typical user's manual listing of the Spice statements and their modifiers. It does, in fact, give the reader a deeper appreciation of what's going on under the Spice simulator's hood, and offers many useful suggestions as to how to keep things fine-tuned. The bottom line is that *Inside SPICE* has the potential of being useful to anyone using Spice.

WALT JUNG

SPICE: Practical Device Modeling (hereafter referred to as "*Modeling*") deals with the practical problem of getting the appropriate models to use with Spice. These models might be any one or more of the following passive or active devices, as noted by these chapter headings: "Practical Device Modeling;" "Modeling Resistors, Capacitors, and Inductors;" "Modeling Diodes and Zener Diodes;" "Modeling the Bipolar Junction Transistor;" "Modeling the Junction Field Effect Transistor;" and "Modeling the Power MOSFET."

Models are basic to the operation of any Spice simulator, and it isn't always realistic to use simplistic models, even for passive parts. Why? Because almost all passive parts have parasitic elements which modify their behavior with varying temperature, applied voltage, or frequency, etc. So, simulations which take these parasitics into account are more complete and accurate. But, a snag here is that with some notable exceptions, few passive component vendors currently offer Spice models for their parts.[3] Hopefully, this situation will change for the better as time progresses.

Active part models are in better shape, because many libraries distributed with popular simulators include IC-vendor-supplied macromodels and simulator-vendor-generated models for many transistors and diodes. This situation, however, is not universal, nor is it complete, and often a model may need to be developed.

Kielkowski's *Modeling* solution for the unavailable model problem is to simply roll your own (at least for those parts as mentioned above). To aid in this process, he has developed a number of utility programs which help to match measured device data and model curves, yielding a useful model for a given part. His goal for the end model is one with a "5% RMS error," with respect to the real part.

The models developed in *Modeling* are subcircuits. As this name implies, they are smaller domain circuits consisting of various Spice elements, both active and passive as required. These elements are interconnected to represent, at the outer terminals, the part being modeled with respect to dynamic changes in current, voltage, frequency, and temperature.

It is a fascinating study to see the development of the various models in the chapters of this book. Even the simpler passive-part models allow good insight into the development, for example, as with a model for a real capacitor. This model would include a nominal capacitance shunted by a leakage resistance, in series with an inductance and series resistance. Temperature-related effects can be added, by modifying both the nominal capacitance and series resistance as a functions of the temperature.

To achieve this, Kielkowski shows us how to use an interconnected combination of controlled sources in the form of an Analog Behavioral Model (ABM). An ABM is a subcircuit which can be configured to perform addition, subtraction, multiplication, and so on. This trick allows the temperature characteristics of a capacitor to be modeled. Of course ABMs are very useful models on their own, and the book's Appendix D is devoted to a series of them. There, ABMs are complete working entities, ready to be applied within larger circuits.

But, of course, the bulk of the book is devoted to the much more detailed processes of model development for diodes and transistors—both bipolar and FET. Familiar parts such as the 1N752 and 2N2222 are used as examples. The developmental processes used give good results.

Throughout these modeling developments, continuous use is made of the supplied modeling software tools, as mentioned above. This technique, alas, brings up the one unfortunate caveat which must be stated of these two books in their present format. These software tools are *DOS-based* utilities, which was understandable for the pre-Windows 95 days of 1994. But, present-day PC users are likely to be using Windows 95, which makes it rather cumbersome to use the tools as designed, with their special DIR structure and CONFIG.SYS-loaded ANSI.SYS driver.

For test purposes, I was able to install the RSPICE software on my Windows 95 machine, but it does not run from a DOS window under Windows 95. It does, however, seem to run just fine, after rebooting from Windows 95 into DOS mode.

The software certainly does offer a low-cost entry into Spice experiences. If desired, one can also purchase three levels of support for this software, at prices ranging from $29.95 to $89.95.

In discussing these operating-system compatibility issues with the author, I learned that an new edition for *Inside SPICE* is planned for introduction sometime around March. This new edition will feature Windows 95-compatible software, so my suggestion to interested readers is watch for this update.

TIP: I enjoyed reviewing these two books, and anticipate gleaning useful material from them for some time to come. And, that's speaking as one who has used Spice on and off for about 12 years. I haven't as yet, taken one of the Kielkowski Spice courses, but hope to do so in the future.

In both of these books, the author's interest and dedication to the topics shows strongly. This fact is communicated to the reader with a style which is direct, clear, and no-nonsense. I can see both books becoming practical tools, and can also easily recommend them as references.

Future topics: On Spice in particular, I'm interested to learn of the general appeal of simulation as a design tool. Are the current simulator tools and available models adequate for your needs? Are integrated packages (suites) of schematic capture, simulators, and pc-board design the way to go? What are the problems you see in these areas? Let's hear from you on these, or other items.

Walt Jung is a corporate staff applications engineer for Analog Devices, Norwood, Mass. A longtime contributor to ELECTRONIC DESIGN, *he can be reached via e-mail at: Wjung @USA.net.*

References:

1. L. Nagel, *SPICE2: A Computer Program to Simulate Semiconductor Circuits*, Report # ERL-M520, University of California at Berkeley, 1975.

2. RCG Research Inc., P.O. Box 509009, Indianapolis, IN 46250-0900, (800) 442-8272 or (317) 877-2244.

3. Tantalum Electrolytic Capacitor SPICE Models, Kemet Electronics, Box 5928, Greenville, SC 29606, (803) 963-6300.

PACKAGING

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The CPU-Cool K1 is a processor cooling kit designed to keep a 300-MHz Pentium II processor well below Intel's 70°C spec (local ambient at 45°C). The kit comprises a high-capacity fan integrated into a patented heatsink with deep-ribbed air channels for efficient heat transfer and special mounting posts for fan alignment. The 2.1-by-3.7-by-1.1-in. kit is priced at $14. PM

***PC Power & Cooling Inc.**, 5995 Avenida Encinas, Carlsbad, CA 92008; Janice Kisiel (760) 931-5700; fax (760) 931-6988.* **CIRCLE 590**

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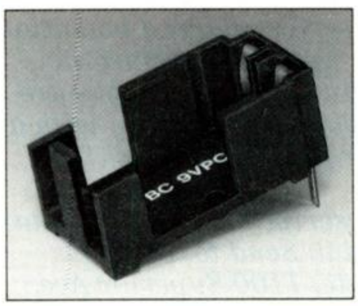

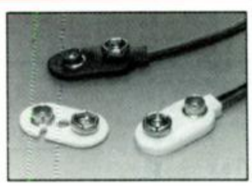

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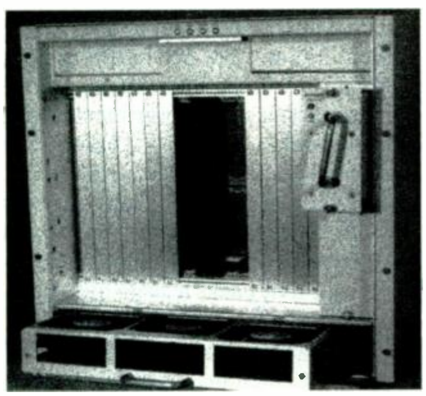
(continued from page 149)
V dc. The maximum airflow and static pressure ranges from 0.19 to 0.52 m^3/min. and 8.5 to 51.2 Pa, respectively. The fans use a dual-ball-bearing design

for stability and meet all UL/CSA, VDE, and CE requirements. Pricing is $10 and delivery is from stock to 16 weeks. PM

***NMB Technologies Inc.**, 9730 Independence Ave., Chatsworth, CA 91311; (800) 662-8321; fax (818) 341-8207; www.nmbtech.com.* **CIRCLE 592**

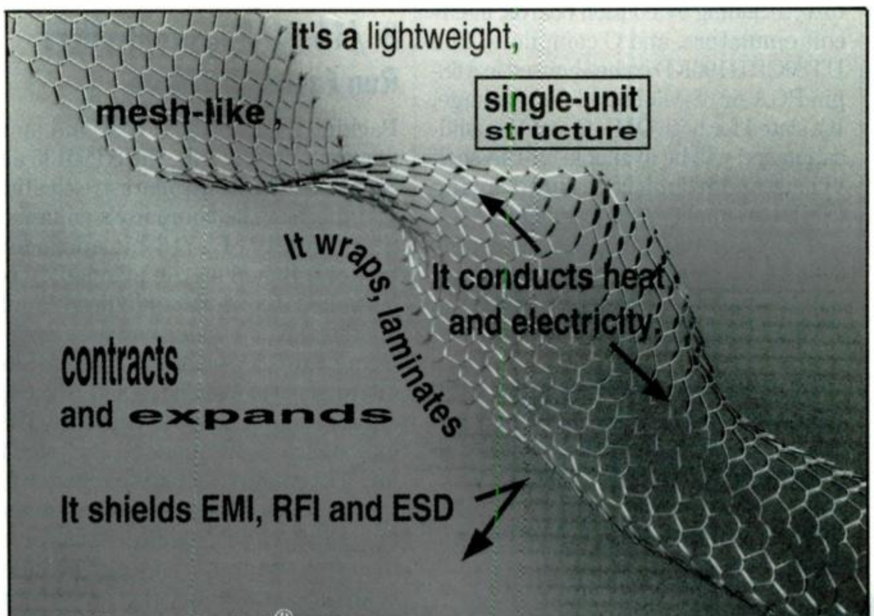
16-in.-Deep Enclosure Is CompactPCI-Compatible

The Series 2240 is a 16-in.-deep CompactPCI enclosure that holds up to 15 6U cards. The enclosure features front-pluggable, dual 350-W, redundant and hot-swappable power supplies and front



air intake through removable/washable filters mounted in a hinged panel. The air is then exhausted out the rear. A front plug-in fan tray directly cools the CPCI cards. Other features include EMI/RFI shielding up to 2 GHz, as well as provisions for two 5.25-in. (half-height) media. Pricing is from $4450 and delivery is from stock.

***Vector Electronic Company**, 11115 Vanowen St., North Hollywood, CA 91605; Erica Skier (800) 423-5659; fax (818) 985-7708; e-mail: inquire@vectorelect.com; Internet: www.vectorelect.com* **CIRCLE 593**



Radiation-Hard 16-Bit MCU Operates At 20 MHz

The first 16-bit radiation-hardened microcontroller, called the UT80CRH196KD, is based on the basic 80C196 MCU architecture and is implemented in UTMC's commercial RadHard epitaxial CMOS wafer process. The processor can operate at clock rates of up to 20 MHz and includes 1 kbyte of on-board single-event-upset hardened SRAM, software and hardware timers, synchronous and asynchronous UARTs, high-speed capture inputs and outputs, and three pulse-width-modulated outputs. The internal ALU supports fast 16-bit multiplies, 32- and 16-bit divides, and logical and arithmetic operations.

The rad-hard process allows the MCU to handle doses of 100 krads (Si), with a LET threshold of 40 MeV-cm^2/mg, which is ideal for space applications ranging from low-earth to geosynchronous orbits. For system development, designers can use commercially available development tools compatible with the MCS-96 architecture, including evaluation boards, in-circuit emulators, and C compilers. The UT80CRH196KD comes housed in a 68-pin PGA or 68-lead quad flat package. It's slated for both QML Q and V qualification and will be available off-the-shelf via a standard microcircuit drawing (SMD) to simplify procurement.

In lots of 100 units, the processor sells for $3000 apiece, and a prototype will be available in the first quarter of 1998. Production is slated for the third quarter. DB

***UTMC Microelectronic Systems**, 4350 Centennial Blvd., Colorado Springs, CO 80907; (719) 594-8000, or on the web at http://www.utmc.com.* **CIRCLE 594**

Smart-Voltage Flash Memory Packs 32 Mbits On A Chip

Available in both 16- and 32-Mbit densities, the smart-voltage flash memories operate with erase/write voltages of 3, 5, or 12 V and support the common-flash-interface (CFI) software. The chips also are available in reduced-area ultra-thin chip-size packages as well as standard SSOPs and TSOPs. The chips are the result of a joint development effort between Sharp and Intel to develop a family of flash memories based on a 0.4-mm process technology for NOR-based flash memories.

The 32-Mbit chip represents the first NOR-based memory to pack 32 Mbits on one chip. The 16-Mbit LH28F160S3/S5, and the 32-Mbit LH28F320S3/S5 operate with read/write/erase voltages as low as 2.7 V, and have read speeds as fast as 130 ns at 2.7 V and 90 ns at 5 V. Write performance also is fast—just 2 ms/byte at 5 volts. In the read mode, the chips consume just 25 mA at 3 V or 50 mA at 5-V. Included are block lock and an enhanced suspend function to provide features suitable for handheld and power-sensitive applications, such as memory cards, PDAs, digital still cameras, and other products.

In 1000-unit quantities, the 16-Mbit chip sells for $15 each, while the 32-Mbit chip goes for $30 apiece. Samples of the 16-Mbit chip are immediately available, while the 32-Mbit circuit will become available in the mid first quarter of 1998. DB

***Sharp Electronics Corp.**, 5700 N.W. Pacific Rim Blvd., Ste. 20, Camas, WA 98607; (360) 834-2500, or on the web at http://www.sharpmeg.com.* **CIRCLE 595**

8-/16-Bit Microcontrollers Run Faster, Do More

Packing a faster CPU core and more powerful peripherals, the ST90135 and ST90158 microcontrollers are the first members of the company's enhanced ST9+ family of 8-/16-bit microcontrollers. Based on the previously released ST9 core, the enhanced family operates over a wider voltage range—from 2.7 to 5.5 V—and can execute 8-bit instructions in just 250 ns and 16-bit operations in 375 ns (both with a 16-MHz internal clock frequency). Included in MCU's core are a 256-byte register file that contains 224 general-purpose registers that can freely be used as accumulators, address pointers, or index registers, and an instruction set that has high-level-language support features such as two-operand instructions and various complex addressing modes.

The 16-bit instruction set includes fast multiply and divide commands and comprehensive move, search, loop, and bit-manipulation operations. One key capability allows the bit manipulation operations to address any bit in any register to perform a Boolean operation—a valuable capability in real-time control applications.

The ST90135 comes with options of 16, 24, or 32 kbytes of ROM, EPROM, or one-time programmable (OTP) storage, and respective on-chip RAM capacities of 512, 768, and 1024 bytes. The ST90158 packs 48 or 64 kbytes of ROM, EPROM, or OTP memory and 768 or 2048 bytes of RAM. Additional functions on the chips include up to nine fully reprogrammable 8-bit I/O ports, two 16-bit prescalable timers, up to three 16-bit multifunction timers (each with an 8-bit prescaler, 12 operating modes, and DMA capabilities), a powerful interrupt controller, and an 8-channel/8-bit ADC.

Both MCUs are available with specifications guaranteed for either commercial or industrial temperature ranges. In 100-k unit lots, the prices for the microcontrollers range from $6 to $9 apiece. DB

***SGS-Thomson Microelectronics Inc.**, 55 Old Bedford Rd., Lincoln, MA 01773; Tony Keirouz, (781) 259-0300; www.st.com.* **CIRCLE 596**

64-Bit RISC CPU Delivers 260 MIPS, 100 MFLOPS

Able to run at clock rates of 200 MHz, the IDT79RV4700 64-bit RISC processor can deliver a throughput of 260 Dhrystone MIPS and 100 MFLOPS (peak). The CPU is compatible with the MIPS IV instruction set and performs 64-bit integer, and floating-point operations and packs 64-bit registers and a 64-bit virtual address space. On-chip resources include 16-kbyte data and instruction caches and a flexible memory-management unit that packs a large fully-associative translation look-aside buffer.

The processor operates from a 3.3-V supply, and includes dynamic power-management circuitry and a standby operating mode to reduce system power when the chip is idle. The high throughput of the chip allows companies to implement functions such as a 16-port, 100-Mbit/s layer-3 switch to run at wire speed because the CPU can process 320,000 packets/s. Available in either a 179-lead PGA or 208-lead metal quad sided flat package, the RV4700 sells for $130 apiece in lots of 10,000 units (MQUAD package). DB

***Integrated Device Technology Inc.**, 2975 Stender Way, Santa Clara, CA 95054-3090; Phil Bourekas, (408) 492-8661; www.idt.com.* **CIRCLE 597**

Integrated Analog Front End Cuts Cost Of xDSL Systems

The AFE1124 is a low-cost mixed-signal IC that provides all of the necessary analog circuitry needed to interface most DSL-based transceivers to a standard copper telephone line. Intended for use in switches, routers, T1/E1 products, and other telecom products, the analog front end supports xDSL technologies from PairGain, Mentalink, and others. Due to its programmable clock and scalable data-rate function, it can be used for speeds from 64 kbits/s (DS0) to 2 Mbits/s (E1).

In addition to an on-chip pulse former and line-conditioning circuitry, it contains a set of 14-bit ADCs and DACs that communicate via a serial interface with the digital signal processors that are typically used to perform the DSL mod/demod functions. Power consumption is only 250 mW, running at either 3.3 or 5 V. Housed in a 28-pin SSOP, the AFE1124 is available now. Pricing is $9 each in 1000-piece orders. LG

***Burr Brown Corp.**, P.O. Box 11400, Tuscon, AZ 85734; attn: Mike Pawlik (800) 548-6132; fax (800) 548-6133; www.burr-brown.com.* **CIRCLE 598**

PHY/MAC Chip Designed For DOCSIS Cable Modems

The LBT 4040 is a single chip that integrates both the media-access-control (MAC) and the physical-layer (PHY) functions for MCNS data over cable service specification (DOCSIS) standard-compliant cable modem applications. The device incorporates all of the functionality of the LBT 4030, a highly programmable cable modem physical-layer transceiver that supports two-way data communication over hybrid fiber-coax networks.

In addition to performing all 64/256 QAM modulation/demodulation and line-equalization functions at the PHY layer, the LBT 4040 also handles the complex time-slotted MAC protocol that forms the basis of the DOCSIS cable data standard. Available during the second quarter of this year, pricing for the LBT 4040 will be under $40 each in production-level quantities. LG

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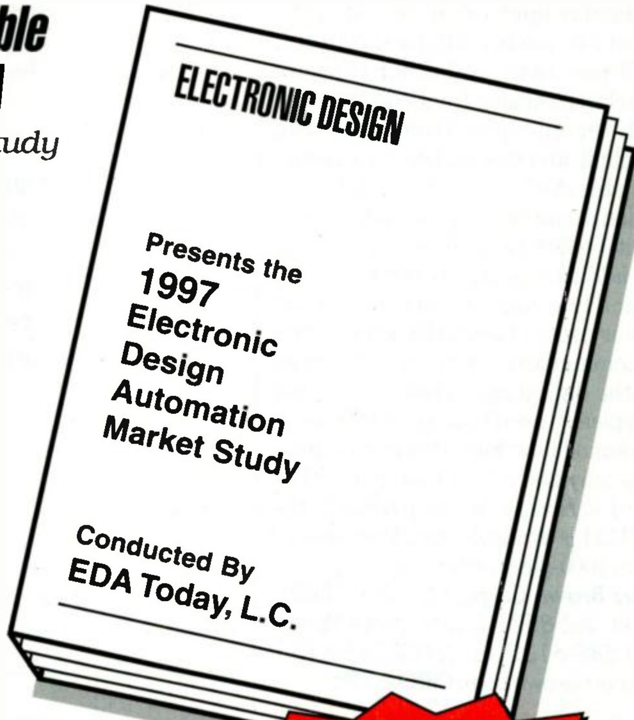

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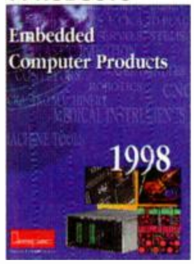

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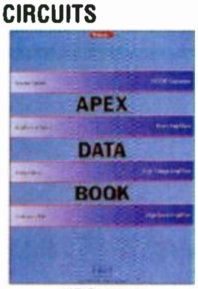

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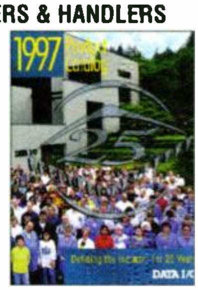

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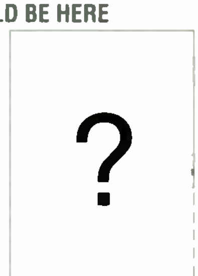

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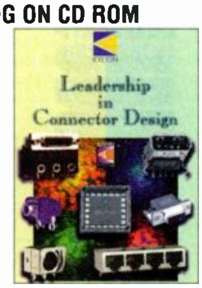

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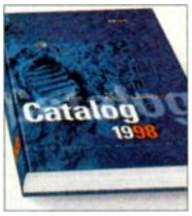

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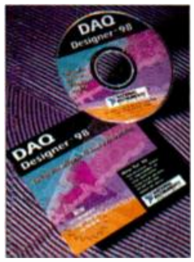

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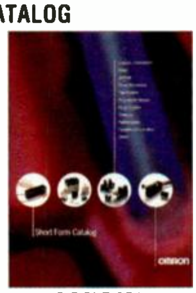

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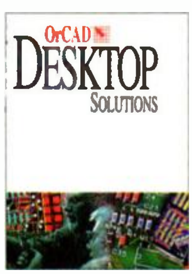

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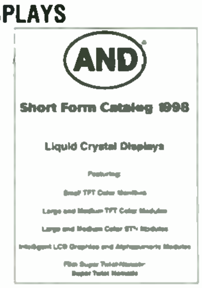

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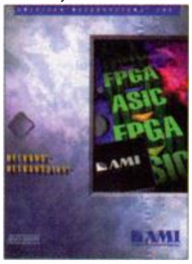

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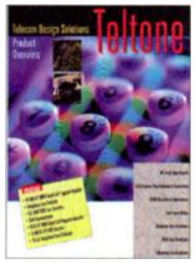

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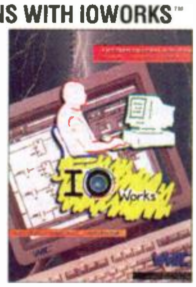

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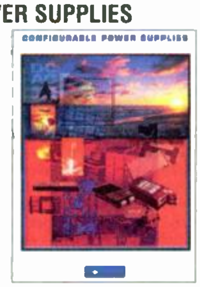

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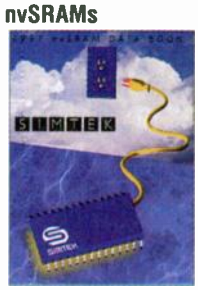

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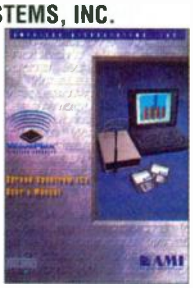

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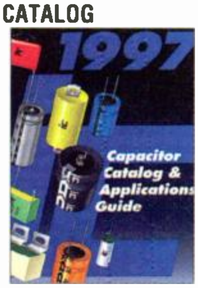

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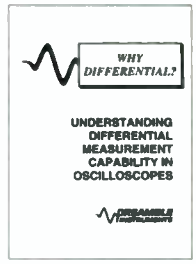

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IFD Guidelines:

- 1 to 1-1/2 pages of single-spaced typewritten text;
- Include schematics, charts, tables, code listings, etc.;
- Include name, company affiliation, address, phone/fax/e-mail

Send your Ideas For Design to:

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