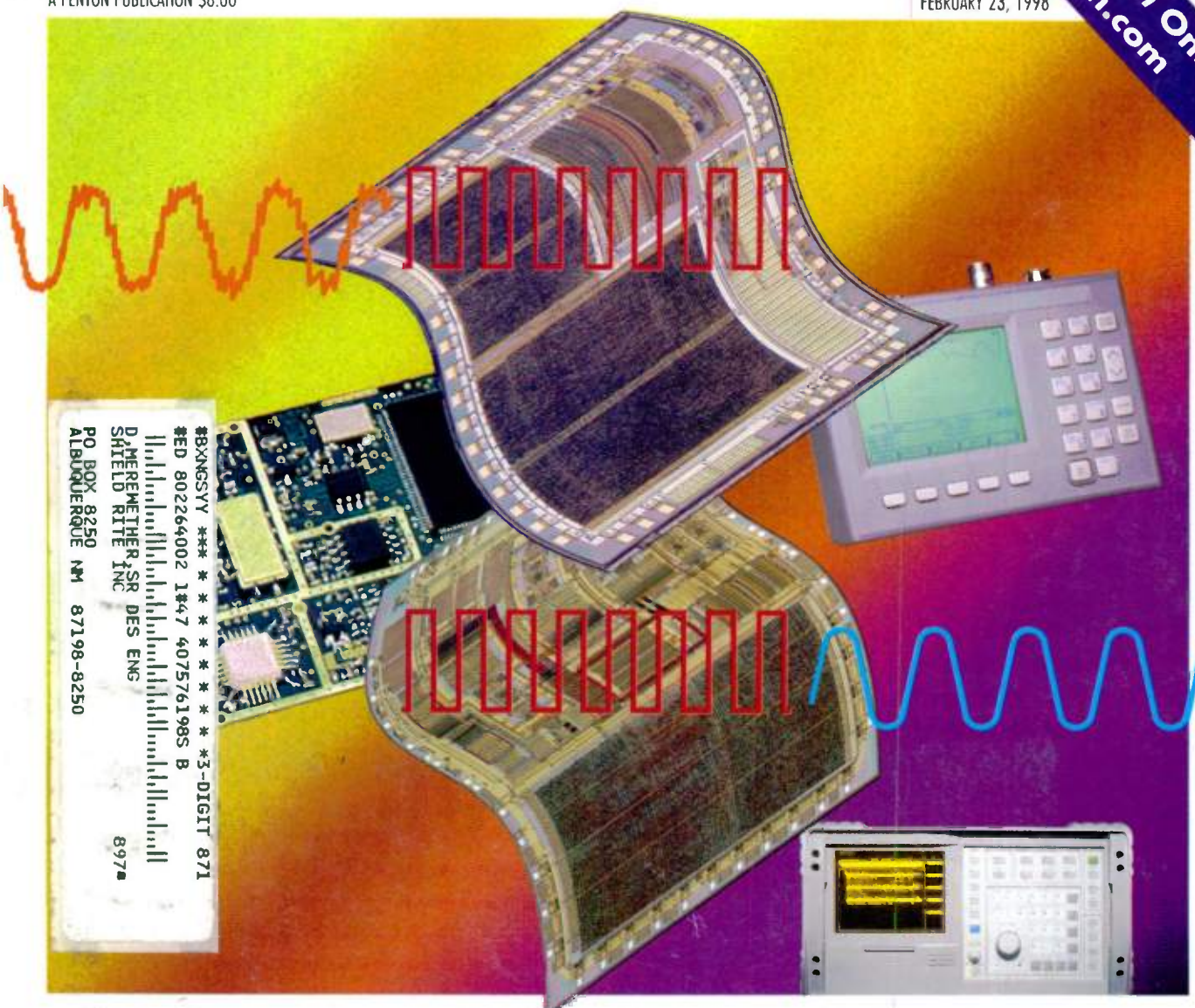
Periodicals Postage Paid

ELECTRONIC DESIGN

TECHNOLOGY • APPLICATIONS • PRODUCTS • SOLUTIONS

A PENTON PUBLICATION $8.00

FEBRUARY 23, 1998



CMOS Converters—High Performance At Low Cost p. 69

Shift into high gear.

FLEX 10K-1 2x faster. Shipping now.

Shift to a new level of performance with Altera's high-speed FLEX 10K-1 devices.

Altera has taken the highest density programmable logic family to the next level of performance. Now you can shift even more of your gate array designs to FLEX® 10K programmable logic.

The fast track just got faster.

The combination of a continuous FastTrack™ Interconnect and a unique embedded array architecture ensures the optimum level of FLEX 10K performance. The new 0.35-micron FLEX 10K-1 devices and enhancements to Altera's MAX+PLUS® II software combine to provide performance improvements of more than 100%. For example, the following table shows performance comparisons for three of the most popular FLEX 10K devices.

Device	Gates	Logic Elements	Embedded RAM	Performance Improvement		Supply Voltage
				-2 Speed Grade (1)	-1 Speed Grade (2)	
EPF10K30A	30,000	1,728	12 Kbits	40%	123%	3.3 V
EPF10K50V	50,000	2,880	20 Kbits	40%	110%	3.3 V
EPF10K100A	100,000	4,992	24 Kbits	35%	107%	3.3 V

1. Estimated performance with -2 speed grade using MAX+PLUS II v. 8.1 compared with -3 speed grade using MAX+PLUS II v. 8.0
2. Estimated performance with -1 speed grade using MAX+PLUS II v. 8.2 compared with -3 speed grade using MAX+PLUS II v. 8.0

Setting the pace with low power and packaging options.

FLEX 10K-1 devices offer 3.3 V supply voltage and numerous package options to fit your design needs.

Accelerate your design process with MAX+PLUS II.

The MAX+PLUS II development system offers a completely integrated development flow and an intuitive Windows-based graphical user interface, making it easy to learn and use. Also, MAX+PLUS II interfaces with all leading EDA design tools. You can work in the design environment you know best and implement your design in the FLEX 10K-1 device you choose.

It's time to shift gears.

Experience the industry-leading FLEX 10K-1 density and performance. Visit the Altera web site to download Device Model Files that support FLEX 10K-1 devices and to order a free literature pack.

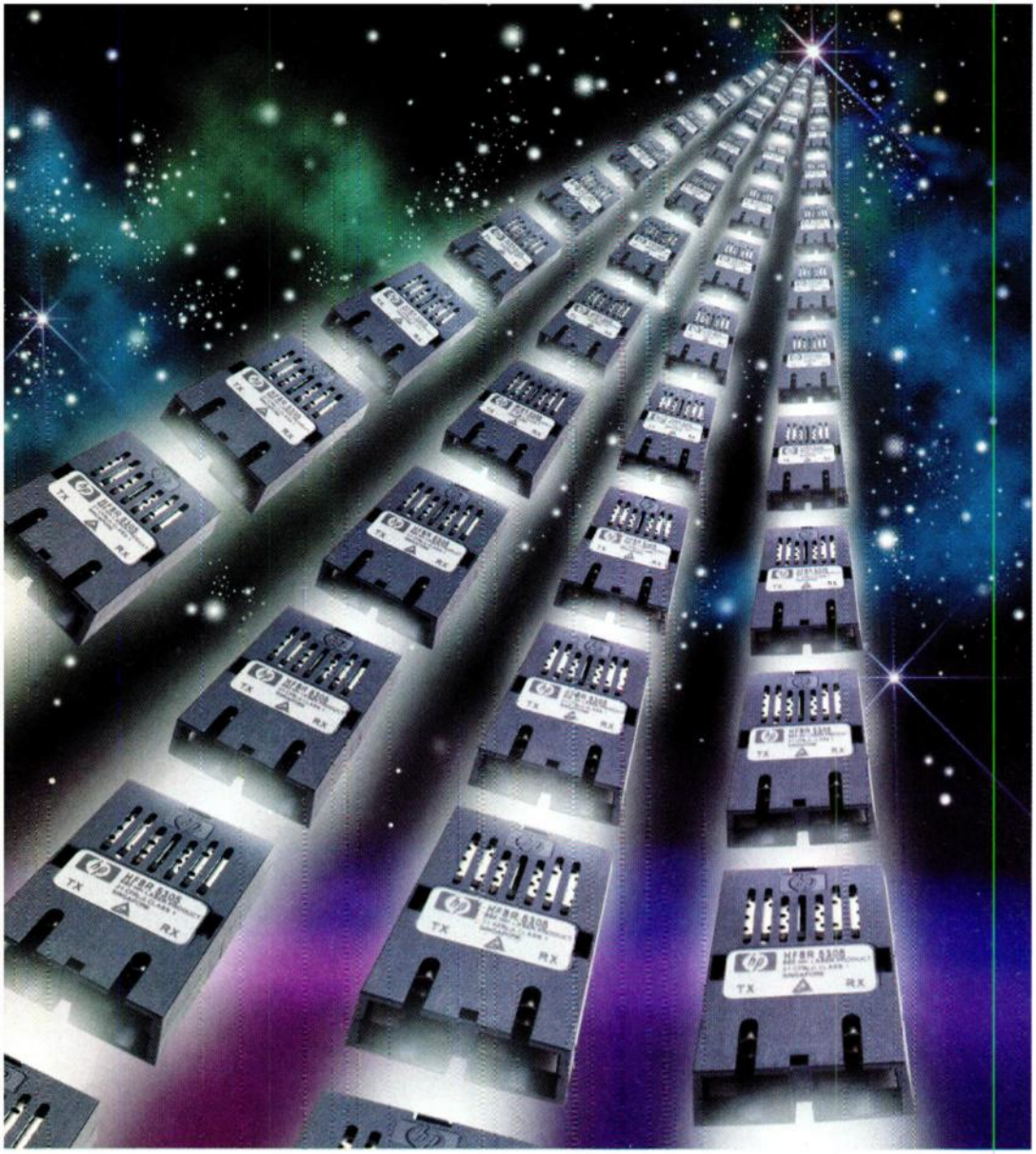
www.altera.com/shift

(800)-9-ALTERA

The ALTERA Advantage

For specific pricing and availability, contact Altera or your local distributor.

WRH



See us at OFC

CSSD9802

Reach the stellar speeds of Gigabit Ethernet.

HP is ready in volume with the full range of Gigabit Ethernet components that meet your needs for high-performance design.

Now you can deliver your systems to the universe because HP is shipping the Gigabit Ethernet products you've been waiting for.

HP's complete physical-layer solution includes short-wavelength (SWL) VCSEL and long-wavelength (LWL) F.P. laser transceivers, 10-bit SERDES ICs, and hot-pluggable SWL, LWL, and copper GBICs. You can also increase your port density with our small form factor transceivers. All this means you can choose exactly the components you need, and get your product to market at virtual light speed.

Which is exactly why leading Gigabit Ethernet networking companies choose HP. These companies know that when you buy a fiber optic component from HP, you get more than just a part. You get a partner - one that's fully committed to your success, with the superior quality, responsive distributor service, and helpful applications support you've always come to expect from HP.

To find out more, just transport yourself over to our website.

www.hp.com/info/gigabit

HEWLETT® PACKARD

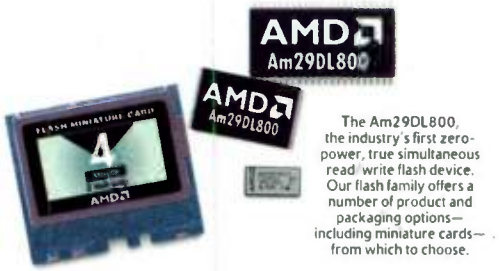
Expanding Possibilities

READER SERVICE 137

For the latest technical data, application briefs and how to order evaluation boards visit our website. Or call 1-800-537-7715 ext. 9976

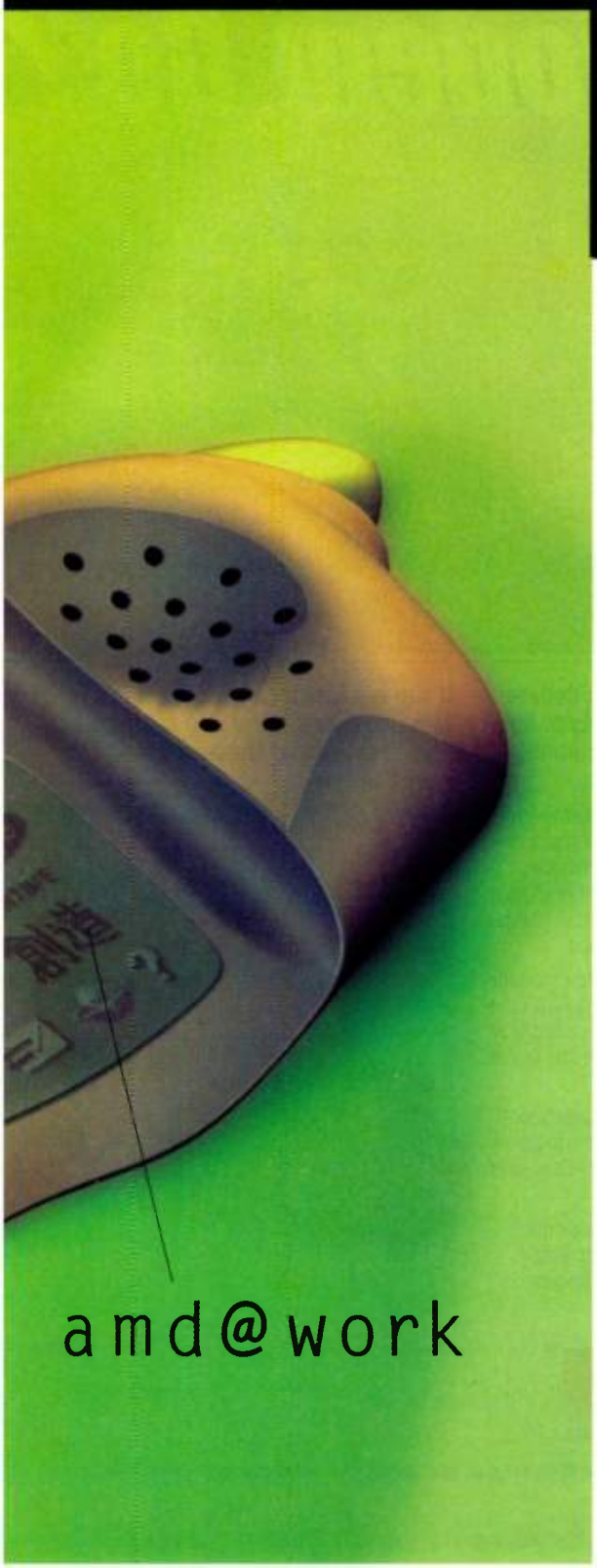
Simplify. Integrate.

Amaze.



The Am29DL800, the industry's first zero-power, true simultaneous read/write flash device. Our flash family offers a number of product and packaging options—including miniature cards—from which to choose.

True Simultaneous Read/Write Flash.



amd@work

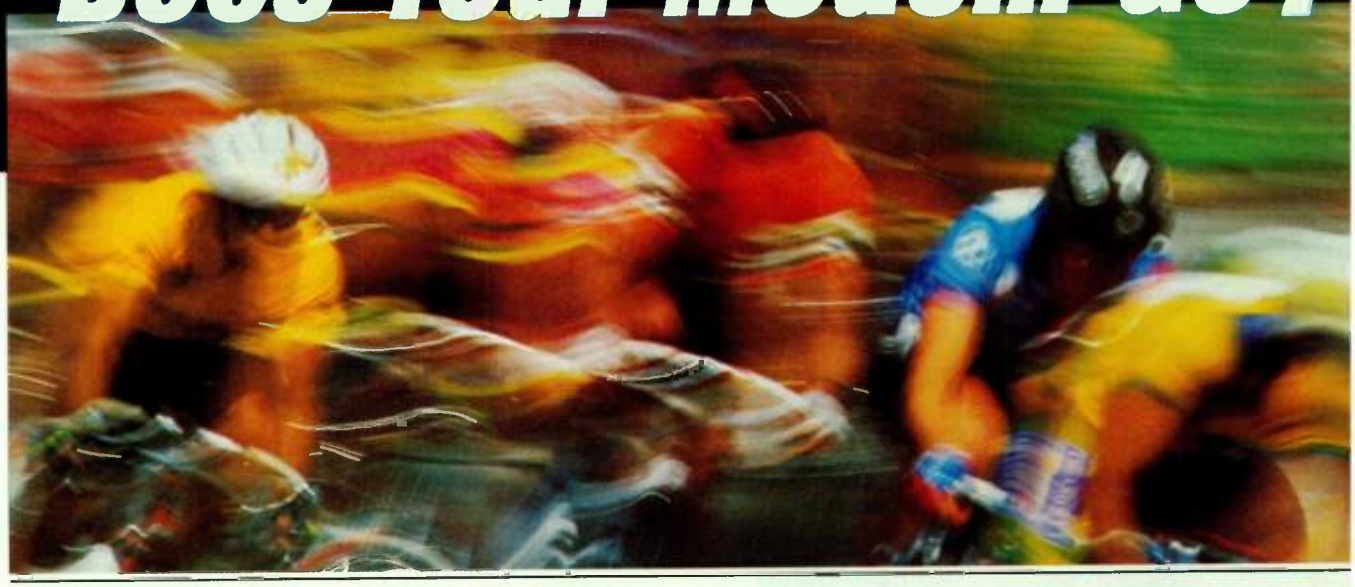
In design, it's certain simplifications, certain perfect little integrations that give you the opportunity to really shake things up. Take for example, the Am29DL800, AMD's zero-power, 2.7-volt-only flash memory device. Now designs that had required multiple memory devices—like EEPROM, SRAM, EPROM or ROM—can achieve the power and simplicity of a single chip solution. The very solution you'll find driving a whole new generation of advanced high-performance (90ns) communication and embedded systems. What you won't find however, is any latency period between read and write operations. Power consumption is also exceptionally low. So you can keep designs compact and nimble. And have plenty of room to integrate that most alluring quality of all: the amazing. To find out more of what's possible with AMD's family of flash products and the architecture of the future, give us a call at 1-800-222-9323 or visit our Web site.

This remarkable concept cell phone/PDA from Gingko Design isn't yet available, but the flash technology that's making it possible is. Today. From AMD.

AMD

www.amd.com

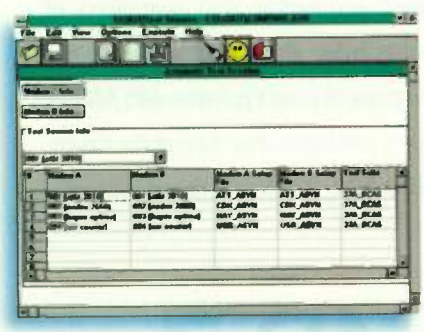
How Fast Does Your Modem Go?



In the hotly contested modem business, you need the tools that will put your product in the winner's circle.

TAS has been providing advanced test and evaluation solutions to modem industry leaders *for over twelve years.*

With the advent of *new* modem technologies **such as 56K,** *accurate and repeatable testing is more important than ever!*



Now TAS modem test systems deliver even more power and flexibility to help ensure the success of your product.

- ***TAS Series II PLUS*** *and 100 Series Telephone Network Emulators are the "gold standard" of modem testing worldwide. These advanced instruments provide accurate, repeatable emulation of telephone exchange conditions, analog impairments, and digital transmission facilities.*
- ***The TAS 240*** *Subscriber Loop Emulator tests your modem's ability to deal with the wide variety of central office to subscriber connections — an especially critical factor for V.34 and 56K modems.*
- ***Gemini & Gemini-PC*** *data analyzers thoroughly test the throughput and error-rate performance of external, PC-Card, and controller-less modems.*
- ***TASKIT® Software*** *automates the entire testing process and gives you comprehensive performance reports.*

If you are testing or evaluating subscriber or central site modems, give your product the best chance to win the race.

Go with the advanced modem test and evaluation solutions from TAS.

tasi®

Telecom Analysis Systems, Inc.

34 Industrial Way East ▪ Eatontown, NJ 07724-3319 ▪ Phone: (732) 544-8700 ▪ FAX: (732) 544-8347 ▪ Email: sales@taskit.com ▪ Internet: http://www.taskit.com

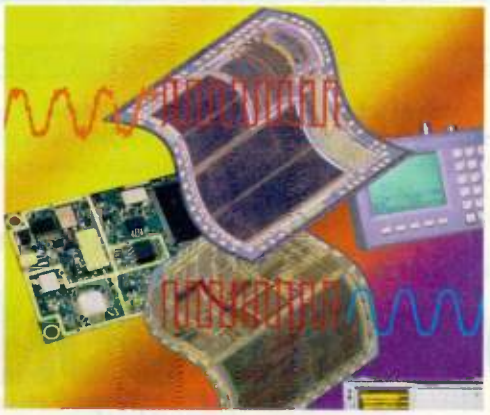
READER SERVICE 194

ELECTRONIC DESIGN

TECHNOLOGY • APPLICATIONS • PRODUCTS • SOLUTIONS

February 23, 1998 Volume 46, Number 4

EDITORIAL OVERVIEW



TECH INSIGHTS

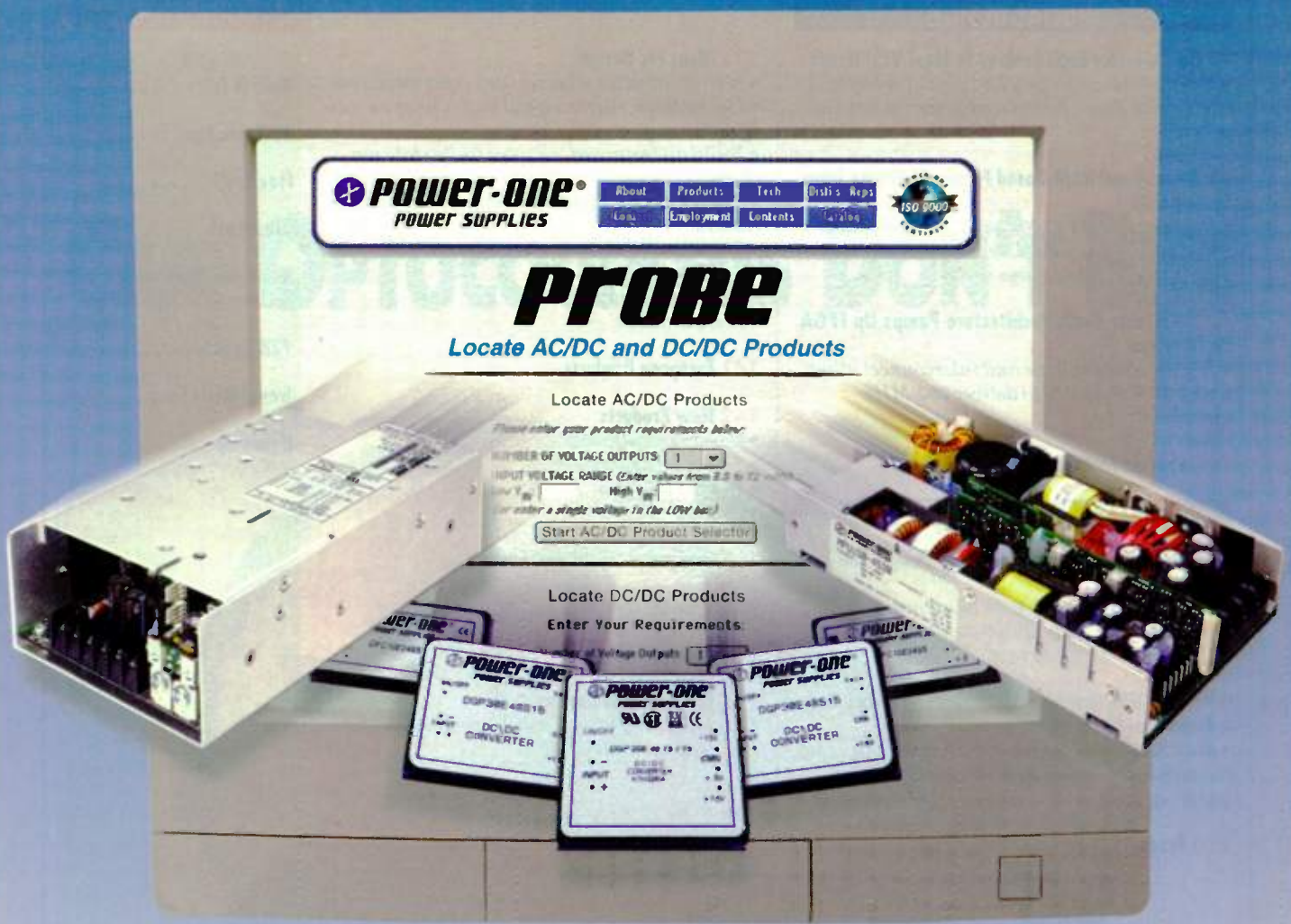
ANALOG OUTLOOK

DEPARTMENTS

ELECTRONIC DESIGN (ISSN 0013-4872) is published twice monthly except for three issues in May, three issues in August, three issues in October, and three issues in November by Penton Publishing Inc., 1100 Superior Ave., Cleveland, OH 44114-2543. Paid rates for a one year subscription are as follows: $100 U.S., $170 Canada, $180, $200 International. Periodicals postage paid at Cleveland, OH, and additional mailing offices. Editorial and advertising addresses: ELECTRONIC DESIGN, 611 Route #46 West, Hasbrouck Heights, NJ 07604. Telephone (201) 393-6060. Facsimile (201) 393-0204. Printed in U.S.A. Title registered in U.S. Patent Office.

One Powerful Web Site.

Power-One's on-line PROBE helps you select the right power supply for your application.



www.power-one.com

AC/DC and DC/DC — One to 4000 Watts	
DC/DC Converters	Over 100 Models from 1-30 Watts
AC/DC Linears	Over 70 Models from 6-280 Watts
AC/DC Low-Power Switchers	Over 100 Models from 30-250 Watts
AC/DC Mid-Power Switchers	Over 30 Models from 225-550 Watts
AC/DC High-Power Switchers	Over 10 Million Configurations from 500-4000 Watts

power-one®
power supplies

740 Calle Plano • Camarillo, California 93012
(800) 765-7448 • FAX (805) 388-0476

READER SERVICE 178

WRH

The industry's *only* 1- to 24-bit

Switch Solution

Fairchild Switch is ***the*** drop-in bus switch alternative.

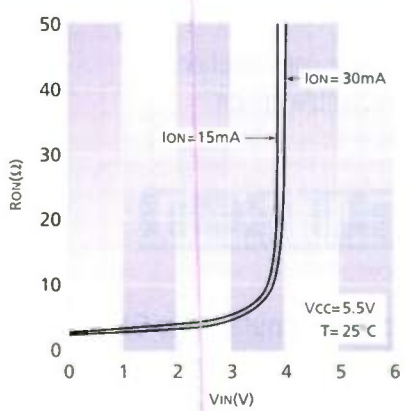
- Get configuration flexibility in the broadest portfolio on the market
- Plug in to live insertion capabilities
- 5V to 3.3V translation protects signal integrity
- Select from SOIC, TSSOP, SSOP, QSOP, SOT23 and SC70 package options
- Choose the reliable supplier delivering cost-effective bus switch alternatives

Fairchild Switch Portfolio

	Function	Part Number
Bus Switch	1-bit Bus Switch	NC7SZ384
	1-bit Bus Switch w/ Diode	NC7SZD384
	1-bit Digital Switch	NC7SZ66
	4-bit Bus Switch	FST3125
	4-bit Bus Switch	FST3126
	8-bit Bus Switch	FST3244
	8-bit Bus Switch	FST3245
	8-bit Bus Switch	FST3345
	10-bit Bus Switch	FST3384
	10-bit Bus Switch w/ Precharged Outputs	FST6800
	24-bit Bus Switch	FST16211

	Function	Part Number
Bus Exchange	Quad 2-1 Mux Switch	FST3257
	Dual 4-1 Mux Switch	FST3253
	10-bit Bus Exchange	FST3383
	18-bit Bus Exchange	FST16209
	24-bit Bus Exchange	FST16212
	24-bit Bus Exchange	FST16213
	16 to 32-bit Mux Switch	FST16232
	16 to 32-bit Mux Switch	FST16233

Typical Resistance



FREE

Technical Specification Booklet & Product Line Card

1-800-215-5289 x27

www.fairchildsemi.com/offers

FAIRCHILD SEMICONDUCTOR™

READER SERVICE 128

ELECTRONIC DESIGN
TECHNOLOGY • APPLICATIONS • PRODUCTS • SOLU

NORTH AMERICAN EDITION

READER SERVICE 125

MARCH 1998

International Verilog Conference and VHDL International User Forum (IVC/VIUF), March 16-19. Santa Clara Convention Center, Santa Clara, California. Contact MP Associates, 5305 Spine Rd., Suite A, Boulder, Colorado 80301; (303) 530-4562; fax (303) 530-4334; e-mail: lee@mpa-net.com; www.hdl-con.org.

IEEE Aerospace Conference, Mar. 21-28. Snowmass Conference Center, Snowmass, CO. Contact Mike Johnson, 2225 Roscomare Road, Los Angeles, CA 90077-2222; (310) 472-8019; e-mail: johnson@ee.ucla.edu.

Second Intellectual Property in Electronics Seminar (IP '98), Mar. 23-24. Westin Hotel, Santa Clara, CA. Contact John Whitaker, Miller Freeman Technical Ltd., +44 181-316-3297; e-mail: ed98@cityscape.co.uk.

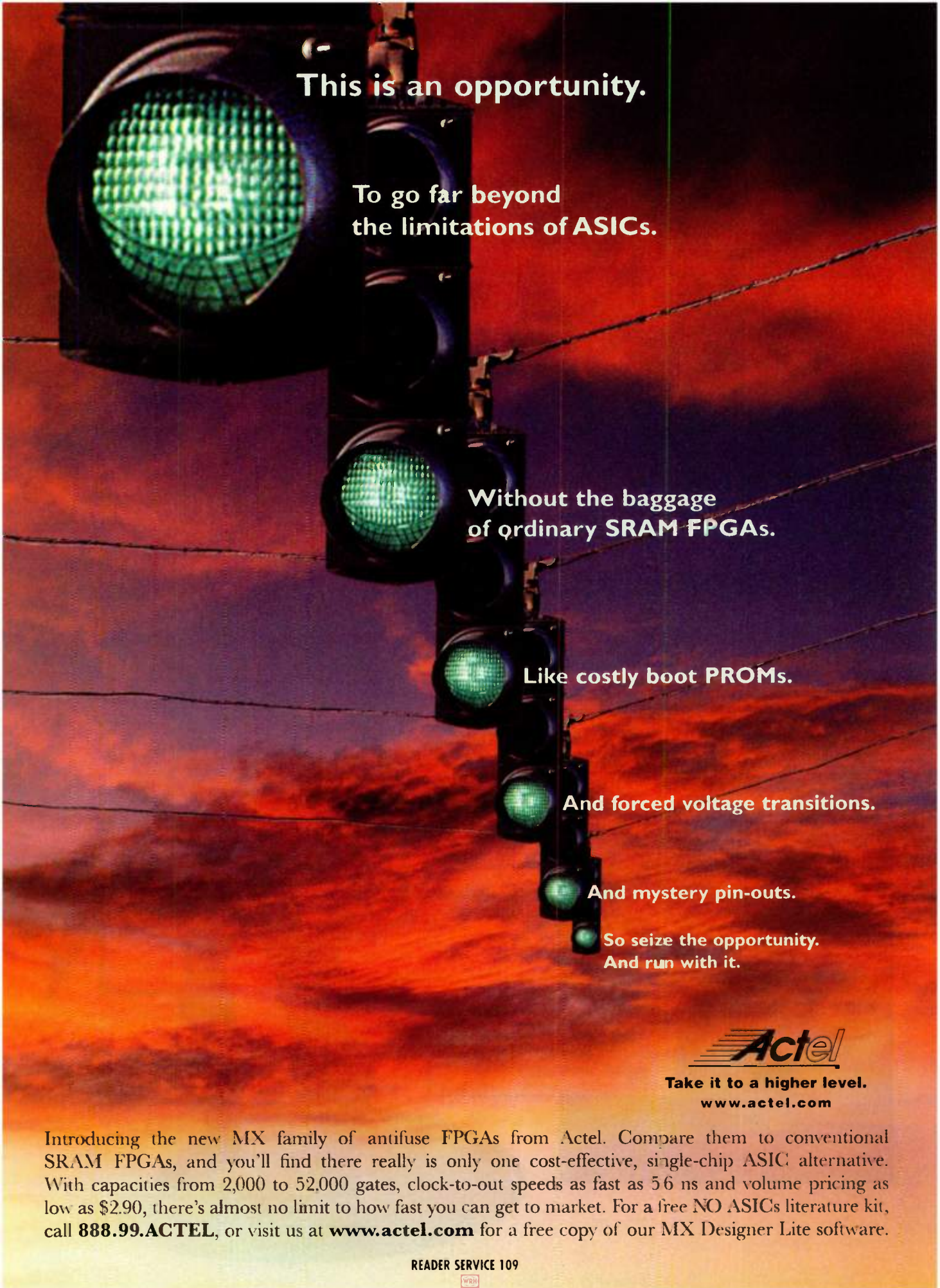
PCB Design Conference West, March 23-27. Santa Clara Convention Center, Santa Clara, California. Contact Molly Knox, Miller Freeman, (408) 448-6173; e-mail: mknox@mfi.com.

Robot Safety Workshop, March 24-26. The Westin Hermitage, Nashville, Tennessee. Contact Brian Huse at RIA Headquarters, Post Office Box 3724, Ann Arbor, Michigan 48106; (313)994-6088; fax (313) 994-3338; e-mail: bhuse@robotics.org; www.robotics.org.

Southcon/98, March 24-26. Orange County Convention Center, Orlando, Florida. Contact Electronic Conventions, (800) 877-2668 or (310) 215-3976; fax (310) 641-5117; www.southcon.com

First Conference On The PC & Automation, March 26-27. Paris, France. Contact Interbus Club USA, Post Office Box 25141, Philadelphia, Pennsylvania 19147, (888) 281-2871; www.interbus-club.com.

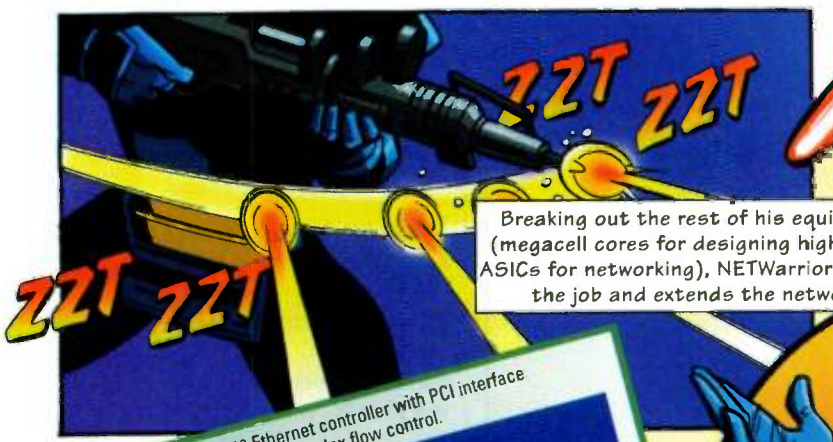
INFOCOM '98, Mar. 28-Apr. 2. Hotel Nikko, San Francisco, CA. Contact Ramesh Nagarajan, Lucent Technologies, 101 Crawford Corner Rd., Rm. 3M-318, Holmdel, NJ 07933; (732) 949-2761; fax (732) 834-5906; e-mail: rameshn@lucent.com.


This is an opportunity.
To go far beyond
the limitations of ASICs.
Without the baggage
of ordinary SRAM FPGAs.
Like costly boot PROMs.
And forced voltage transitions.
And mystery pin-outs.
So seize the opportunity.
And run with it.
Actel
Take it to a higher level.
www.actel.com
Introducing the new MX family of antifuse FPGAs from Actel. Compare them to conventional SRAM FPGAs, and you'll find there really is only one cost-effective, single-chip ASIC alternative. With capacities from 2,000 to 52,000 gates, clock-to-out speeds as fast as 5.6 ns and volume pricing as low as $2.90, there's almost no limit to how fast you can get to market. For a free NO ASICs literature kit, call 888.99.ACTEL, or visit us at www.actel.com for a free copy of our MX Designer Lite software.
READER SERVICE 109


Adventures In Communication Design™
On a distant world, between the near and far future, disaster strikes—followed by a frantic call for help...
THOOM!
John, the network's down! Need super...net... design...r. Need NETWar-rio...
Just grab my gear. Get my Oki super tools and... Darn. 'Cause of cell phones, a superhero can't find a decent phone booth to change in these days!
Need a Super Network Designer, do they?
John Dataman, best network design engineer on the planet, assumes his secret identity to become... NETWarrior...arrior...arrior!!!
OKI ATM
OKI 8-Port Ethernet MACs
OKI ASICs
OKI laser diodes

Using his Oki laser diodes, **NETWarrior**™ pulses through the network speeding data along its fiber optics.

With an 8-Port Ethernet MAC capable of full and half duplex flow control, **NETWarrior** deflects data into multiple streams maximizing the Ethernet's bandwidth.



Breaking out the rest of his equipment (megacell cores for designing high-speed ASICs for networking), NETWarrior finishes the job and extends the network.

8-Port MAC	10/100 Ethernet controller with PCI interface full and half duplex flow control.
ASICs	Silicon Architecture CBA. 0.35µm SOG and Embedded Arrays. Up to 1.5 million gates. 500 pin BGA. Single port MAC core. 1 Gbit MAC*
Laser Diodes	WDM and instrument applications. to OC48 direct modulation lasers and 10 GHz GaAs Logic for fiber communications. Over 100mW for "OTDR" instruments. Monitor lasers from 1.3µm to 1.6µm.

* Currently in development

OKI ComICs™ is brought to you by OKI Semiconductor. Super Solutions for all your Ethernet LAN and Wireless (WLAN) designs—Laser diodes, 8-Port Ethernet MAC and 1394, PCI and USB ASIC cores. OKI—your one-stop Com(munication) IC source.

OKI ComICs™

www.okisemi.com

Oki Semiconductor

READER SERVICE 173

WRH

MARCH

IEEE International Reliability Physics Symposium, March 30-April 2. Reno Hilton Hotel, Reno, Nevada. Contact Ann N. Campbell, M/S 1081, Sandia National Labs., Post Office Box 5800, Albuquerque, New Mexico 87185-1081; (505) 844-7452; fax (505) 844-2991; e-mail: ancampbe@sandia.gov.

IEEE International Parallel Processing Symposium/IEEE 9th Symposium on Parallel and Distributed Processing (IPPS/SPDP), March 30-April 3. Delta Orlando Resort, Orlando, Florida. Contact Viktor Prasanna, EEB-200C, Department of EE Systems, University of Southern California, Los Angeles, California 90089-2562; (213) 740-4483; fax (213) 740-4418; e-mail: prasann@ganges.usc.edu.

Embedded Systems Conference Spring, Mar. 31-Apr. 2. Navy Pier Festival Hall, Chicago, IL. Contact Liz Austin, Miller Freeman Inc., (888) 239-5563; (415) 538-3848; e-mail: esc@mfi.com.

APRIL

China Telecom 2000 Conference, Apr. 7-8. Holiday Inn Capitol, Washington, D.C. Contact Information Gatekeepers, (800) 323-1088; (617) 232-3111; fax (617) 734-8562; e-mail: igiboston@aol.com; www.igi-group.com.

20th IEEE International Conference on Software Engineering, Apr. 19-25. Kyoto International Conference Hall, Kyoto, Japan. Contact Koji Torii, Graduate School of Information Sciences, Nara Institute of Science & Technology, 8916-5 Takayama-cho, Ikoma-shi, Nara-ken 630-01, Japan; +81 7437-2-5310; fax +81 7437-2-5319; e-mail: torii@is.aist-nara.ac.jp.

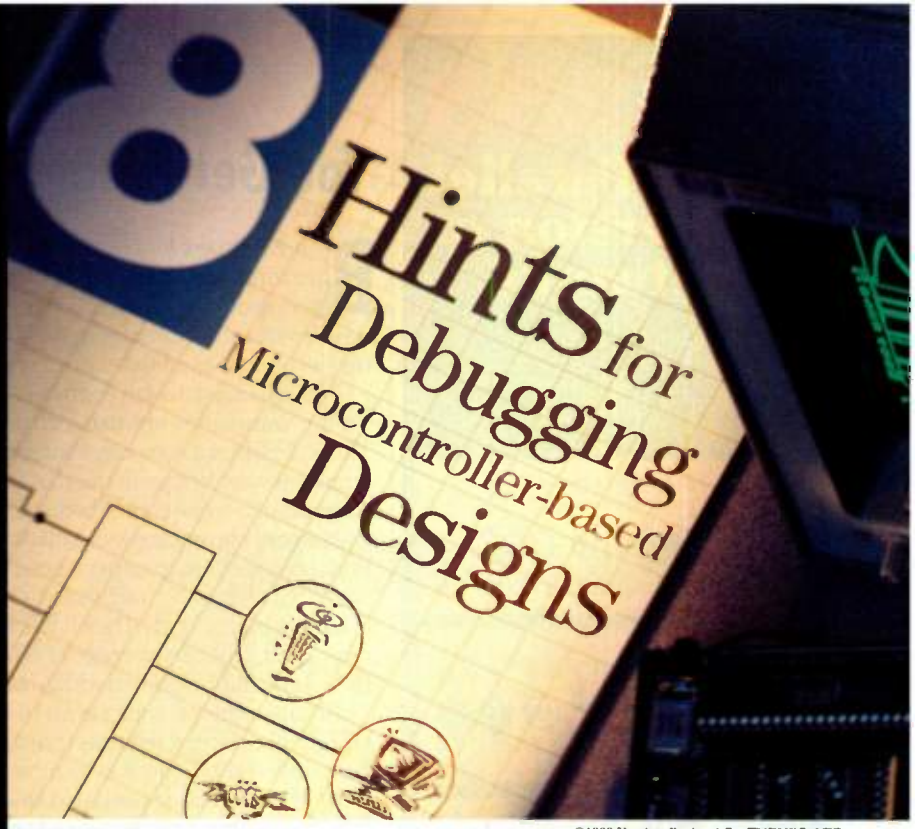
DSP World Spring Design Conference, April 21-23. Santa Clara Convention Center, Santa Clara, California. Contact Liz Austin, Miller Freeman Inc. (888) 239-5563, (415) 538-3848; e-mail: dspworld@mfi.com; www.dsp-world.com.

Southeastcon '98, April 24-26. Hyatt Regency, Orlando International Airport, Orlando, Florida. Contact Parveen Ward, ECE Dept., University of Central Florida, Orlando, Florida 32816; (407) 823-2610; fax (407) 823-5835; e-mail: pfw@ece.engr.ucf.edu.

16th IEEE VLSI Test Symposium, April 26-30. Hyatt Regency Monterey, Monterey, California. Contact Rob Roy, Intel Corp., MS:JFT-102, 5300 Elam Young Parkway, Hillsboro, Oregon 97124-6497; (503) 264-3738; fax (503) 264-9359; e-mail: robroy@ichips.intel.com.

IPC Printed Circuits Expo '98, Apr. 26-30. Long Beach Convention Center, Long Beach, CA. Contact Dan Green, The Institute for Interconnection & Packaging Electronic Circuits, 2215 Sanders Rd., Northbrook, IL 60062-6135; (847) 509-9700 ext. 371; fax (847) 509-9798.

8 Priceless Hints Free



1. Tracking down elusive glitches
2. Unscrambling serial I/O
3. Verifying PWM dead time in motor controllers
4. Isolating software problems with an advanced logic probe
5. Using arbitrary waveforms for bit-error testing
6. Resolving hardware/software integration problems
7. Correlating software and analog outputs in a CAN controller
8. Debugging an MCU-based CCD camera controller

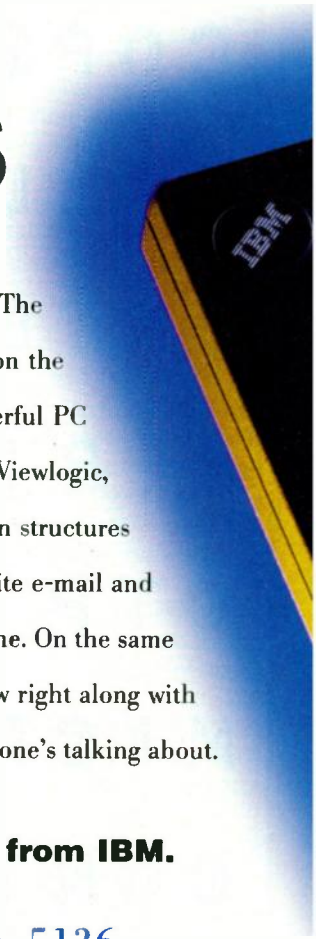
To receive a free copy of *8 Hints for Debugging Microcontroller-based Designs*, call HP at 1-800-452-4844, Ext. 5697.

As industry deadlines become shorter, the pressure to debug your 8- and 16-bit designs becomes more challenging. You don't have time to reinvent solutions to design problems that have already been solved. That's why HP's *8 Hints for Debugging Microcontroller-based Designs* is invaluable to 8- and 16-bit designers looking for creative shortcuts to common problems in their design process. What's more, every one is a real-life solution submitted by an engineering expert just like you. For example, a hint submitted by a product definition engineer for Siemens shows how to use time-qualified triggering to measure pulse-width modulation in MCU-based motor control designs. So the next time you're attacking a problem, make sure *8 Hints for Debugging Microcontroller-based Designs* is in your arsenal.

READER SERVICE 151

HEWLETT PACKARD

IBM IntelliStation Blazes New Trails



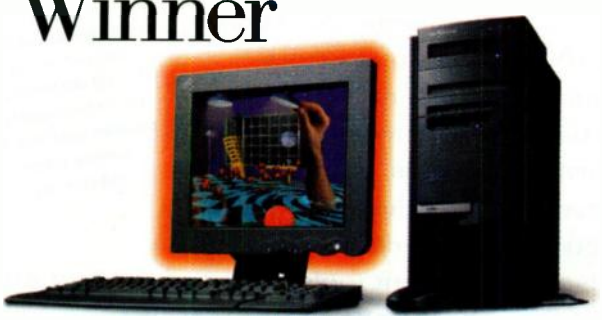
Make no mistake, someday it will happen—the world's first billion transistor chip. The designer might even be you. And when you design it, you'll probably want to create it on the IBM IntelliStation™. That's because IntelliStation combines all the capabilities of a powerful PC together with a number-crunching workstation. Add programs like Cadence, Mentor and Viewlogic, now on Windows NT®, so you can design, zoom, pan and navigate your .06 micron silicon structures using eye-popping 2D/3D graphics. You can run your project management programs, write e-mail and access powerful digital libraries and even the Internet. And do all this at the very same time. On the same high-resolution monitor. Want a highly flexible, extremely manageable system that'll grow right along with you? Then get more information on IBM IntelliStation—the hot new trailblazer that everyone's talking about.

Find out about the intelligent Windows NT workstation from IBM.

1 800 426-7255 ext. 5136

www.pc.ibm.com/us/intellistation/go

PCWEEK BEST OF COMDEX Winner

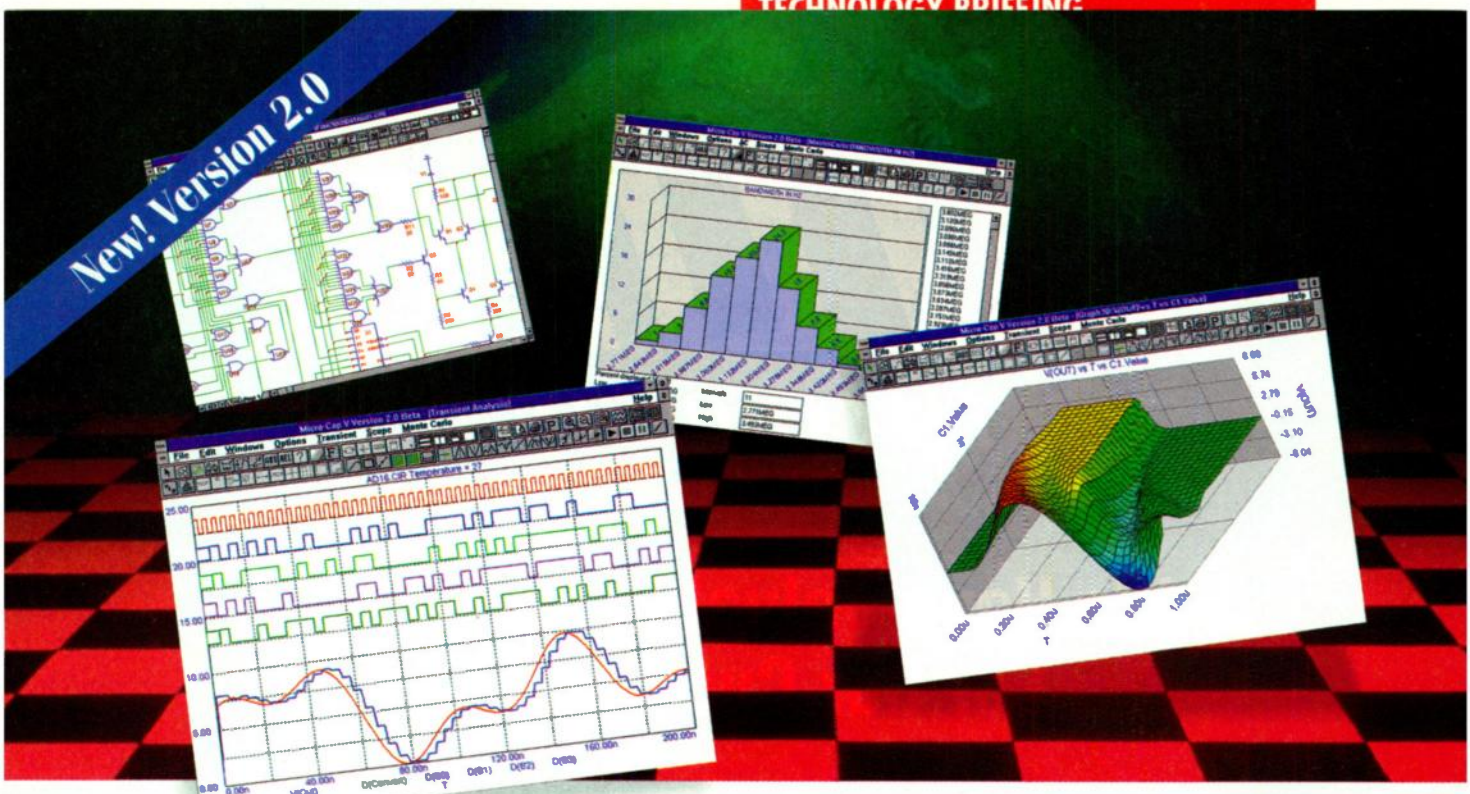


A frightening amount of power: Up to two 300MHz[1] Pentium® II processors • 512KB on-board L2 cache • 512MB SDRAM • Up to 9.1GB[2] Wide Ultra SCSI with S.M.A.R.T. • Your choice of graphics accelerators: PERMEDIA 2 or Intergraph Intense3D Pro 2200/T

IBM IntelliStation.

Nothing gets in the way of a good idea.

[1]MHz denotes internal clock speed of the microprocessor only; other factors also affect application performance. [2]GB=1,000 million bytes when referring to hard-drive capacity. Accessible capacity may be less. IBM, IntelliStation and Solutions for a small planet are trademarks or registered trademarks of International Business Machines Corporation. The Intel Inside logo and Pentium are registered trademarks and MMX is a trademark of Intel Corp. Microsoft and Windows NT are registered trademarks of Microsoft Corporation. Other company, product and service names may be trademarks or service marks of others. PCs referenced in this ad ship with an operating system.



Want the very best in Analog/Digital simulation? Introducing Micro-Cap V Version 2.0

Micro-Cap V is a fast, precision, 32-bit analog/digital simulator with an intuitive fifth generation user interface, and a library of more than 10,000 pre-modeled parts. Based on Spice3 and PSpice,™ it offers the best features and capability of both.

Its finely crafted simulation tools include schematic probing, during the run plotting, performance plots, 3D plots, multidimensional stepping, analog and digital behavioral modeling, an optimizing model generator, and Monte Carlo analysis. Compiled models, behavioral primitives, and a huge library of commercial parts make modeling of both analog and digital devices easy. New devices in Version 2.0 include BSIM 1.0, 2.0, and 3.3, sample and holds, Z transforms, and three new animation devices.

Download the free working demo at www.spectrum-soft.com.

We offer the very best in analog/digital simulation and we guarantee it with a 30 day money back guarantee!

You can't lose. Call us for a free brochure and working demo or download the demo from our Web site.

Micro-Cap V runs on PCs under all Windows systems from 3.1 and up. Cost is $3495 complete.

Features

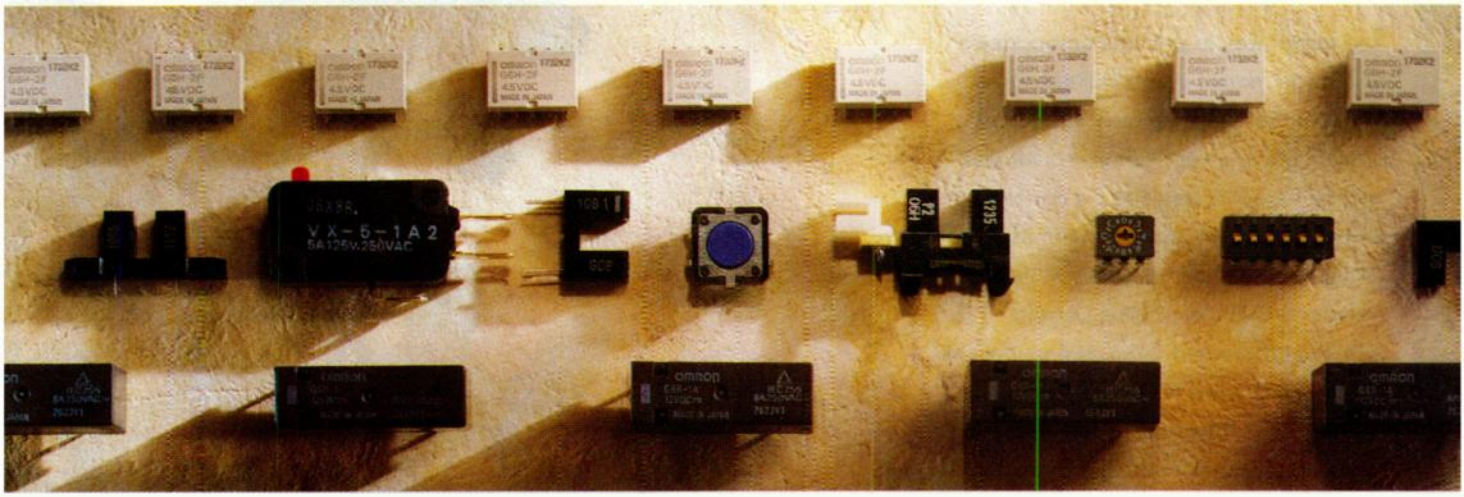
• Mixed Analog/Digital	Yes
• Analog Engine	Spice3 & PSpice™
• Digital Engine	Native PSpice™
• During the Run Plots	Yes
• Analog/Digital Primitives	200+
• Analog/Digital Parts	10,000+
• Performance Plots	Yes
• Parameter Stepping	Multidimensional
• Optimizing Parts Modeler	Yes
• 3D Plots	Yes
• Schematic Probing	Yes
• Behavioral Modeling	Analog & Digital
• Monte Carlo	Yes
• Device Temperatures	Individually Set
• BSIM Devices	Yes. 1.0, 2.0, and 3.3
• Animation Devices	Yes
• Import/export Netlists	Yes
• Guarantee	30 Day Money Back
• Technical Support	By EEs for EEs

spectrum

Spectrum Software

Phone 408-738-4387
FAX 408-738-4702
Internet www.spectrum-soft.com
E-mail sales@spectrum-soft.com

If You Think Omron Only Makes Relays, Read Between Our Lines.



It's true we're the world's number one relay supplier. So it's not surprising to learn that design engineers and specifiers know us for our relays.

But we also manufacture the world's most complete line of switches and photomicrosensors.

For years we've been building all types of switches, photomicrosensors, and relays for leading companies that manufacture telecommunications products, home and office electronics, computer peripherals, appliances, and HVAC equipment, just to name a few.

Proven reliability makes Omron relays, switches, and photomicrosensors the preferred choice of design engineers and specifiers worldwide.

What does all this mean? That's simple. Our expertise has led to the development of standard components for all kinds of applications. And when you can fit a standard switch to your custom application, you're looking at a considerable cost savings. Plus you'll see your design go into production that much faster.

In switches alone, we have basic switches, mechanical keyswitches, rotary and in-line DIP, thumbwheel and rocker switches, amplified and non-amplified photomicrosensors, PCB mount and connector-ready photo-microsensors, as well as lighted and oil-tight pushbuttons.

And everything Omron makes is 100% tested, available to you world-wide, and backed up by outstanding technical and distribution support.

To find out if Omron has the component solution you're looking for, call now to receive our Standard Products Catalog or visit our web site at http://www.oei.omron.com. For a directory of techinical data sheets, call *ControlFax* at 1-847-843-1963 and ask for document #50.

If you respond to innovation and more efficient ways of doing business, it's a story worth reading.

1-800-55-OMRON

ASK FOR OUR STANDARD PRODUCTS CATALOG. IT'S FREE!

OMRON

WE HAVE THE FUTURE IN CONTROL

READER SERVICE 174

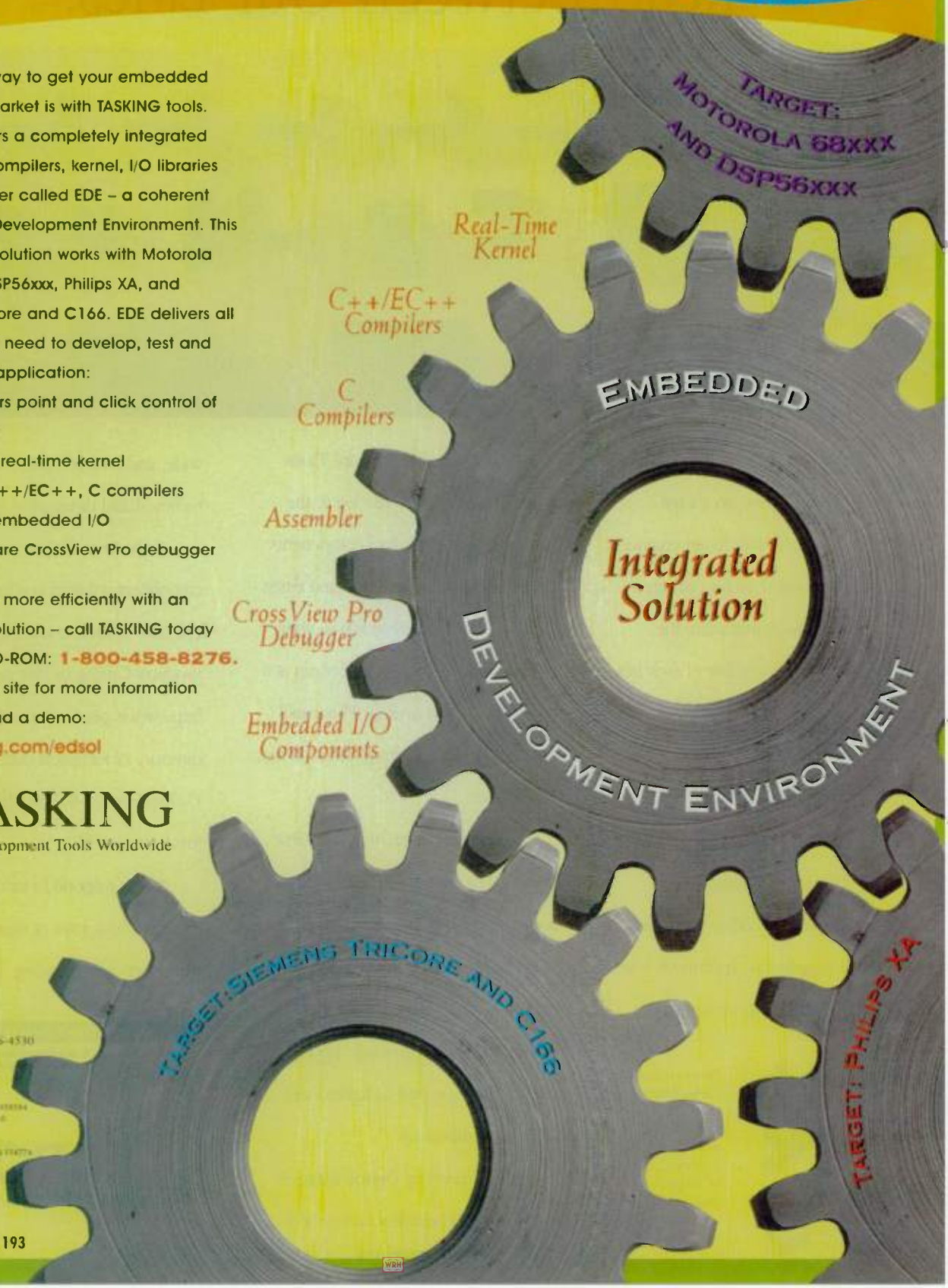
Get Your Embedded Systems Development In High Gear.

EC++ FOR 68K NOW!

The fastest way to get your embedded systems to market is with TASKING tools. TASKING offers a completely integrated solution of compilers, kernel, I/O libraries and debugger called EDE – a coherent Embedded Development Environment. This end-to-end solution works with Motorola 68xxx and DSP56xxx, Philips XA, and Siemens TriCore and C166. EDE delivers all the tools you need to develop, test and debug your application:

- EDE delivers point and click control of the toolset
- Scaleable real-time kernel
- Efficient C++/EC++, C compilers
- Extensive embedded I/O
- Kernel aware CrossView Pro debugger

Start working more efficiently with an integrated solution – call TASKING today for a FREE CD-ROM: **1-800-458-8276.** Visit our Web site for more information and download a demo: **www.tasking.com/edsol**



TASKING
Quality Development Tools Worldwide

TASKING, Inc.
333 Elm Street
Dedham, MA 02026-4530
Tel: 781-320-9400
Fax: 781-320-9212

READER SERVICE 193

Electric-Vehicle Charging Stations Currently Under Construction

The California Air Resources Board has mandated that 10% of all new vehicles sold in California in 2003 will be zero-emission vehicles. With this date quickly approaching, the only cars so far that can meet this standard are electric vehicles (EVs). EVs are estimated to be 97% cleaner than existing gasoline-powered cars, including power-plant emissions, and cost roughly 60 cents per hour to operate. While all major car manufacturers are either currently producing such vehicles or plan to demonstrate vehicles throughout the year, key to their successful utilization on the road is their recharging ability, just as one might fill up their car on a tank of gasoline. This requires the strategic placement of EV charging stations to service the needs of EV drivers.

Toward that end, Southern California-based Edison EV and Hilton Hotels Corp., Beverly Hills, Calif., have joined forces in a project funded by General Motors to equip participating Southern California-area Hilton hotels with EV recharging stations. These stations will allow drivers of the EV1 electric vehicle who recharge overnight roughly three and a half hours of charge time, enabling 70 to 90 miles of drive time the following day. Visitors who receive a temporary "top-off" charge while, for example, dining or attending a meeting at the hotel, can extend their driving range by 50% or more. The charging service is complimentary to guests and visitors.

While 11 installations at various Southern California-area Hilton hotels, including the company's corporate office in Beverly Hills, Calif., have already been completed, it's expected that 1998 will witness additional installations. This move is intended to bolster the already rapidly growing EV infrastructure being developed in California. In fact, with many major rental car companies expected to soon begin offering EVs for rental, project participants believe that the idea of Hilton allowing guests who have rented EV1 cars to "charge up" will help solidify future EV infrastructure growth. For further information on this project, check out the following web sites: *www.edisonx.com*, *www.gmev.com*, or *www.hilton.com*. CA

HDSL.2 Telecom Standard Achieves Provisional Approval

HDSL.2, a new communications standard that could significantly cut the cost of deployment for T1/E1 (1.5/.0 Mbit/s) lines, is nearly ready Once approved, the standard would enable bidirectional transmission of T1 and possibly E1 traffic across a single pair of standard-issue twisted-pair copper lines. By cutting the number of wire pairs required for a high-speed line in half, telecommunication providers will be able to double the capacity of their existing infrastructures. The initiative for the new standard was spearheaded by a consortium of telecom electronic manufacturers, including ADC, Adtran, Level One, and Siemens Microelectronics.

In early January of this year, the American National Standards Institute's (ANSI's) T1E1.4 committee issued a provisional agreement for the specifications in the proposed technologies and specifications that would define HDSL.2. The elements agreed upon were line code, spectral shaping, system performance, and forward error correction. These elements represent the core technologies of HDSL.2, and their approval is expected to accelerate the remainder of the development process. For further information on HDSL.2, contact Level One Communications, 9750 Gothe Rd., Sacramento, CA 95827; Internet: *www.level1.com*. LG

MCM-L Module Includes Built-In Capacitors, Inductors, Resistors

Improved electrical performance, reduced assembly cost, and greater packaging efficiency are some of the advantages attained by integrating passive elements (resistors, capacitors, and inductors). Until now, though, this technology has yet to be developed for the low-temperature fabrication process compatible to MCM-L technology.

At the Georgia Institute of Technology, Atlanta, Ga., a low-cost and fully integrated passive module has been fabricated for the first time using the low-temperature PWB-compatible fabrication process. The passive RLC module includes 12 integrated resistors (5 to 80 Ω), four capacitors (14 to 160 pF), and four inductors (145 to 650 nH).

The integrated resistors were patterned with evaporated metal (a low-temperature screen-printing process is currently being evaluated). The capacitor dielectric was made using a low-cost photodefinable epoxy filled with high dielectric constant (approximately 17,800 in sintered form) and finer (about 1 μm size) ferroelectric ceramic powder, while the inductors used a nickel-zinc ferrite powder/polyimide composite. Spin-coating and screen-printing technology were utilized for the fabrication of capacitors and inductors. The inductors were protected with and EMI shielding material. The dimension of the RLC module is 10 by 8 by 0.07 mm.

According to Dr. Rao R. Tummala and Mark G. Allen, both of the School of Electrical and Computer Engineering (ECE), the fabrication technology was relatively inexpensive and PWB-compatible. "The use of epoxy could further reduce the overall material cost," says Tummala. "The module was electrically tested and the measured component values were comparable with the desired values."

For more information, call (404) 894-9097 or (404) 894-9419; or e-mail at: *rao.tummala@ece.gatech.edu* or *mark.allen@ece.gatech.edu*. RE

Considering how much each partner adds to the MIPS architecture,

"In the MIPS RISC game, it's not whether Philips wins or loses. It's finding new ways to let our partners down gently."

"When our partners get a design win, we all win. When LSI Logic wins, we gloat. But just a little."

"I think IDT once lost a design win to one of our partners. But then again, I may have just imagined it."

"It's not like NEC calls our MIPS partners to say, WE WON, WE WON after getting the design win. Okay, so we did it once."

"Toshiba has never actually lost a design win. We prefer to think of it more as sharing with our other MIPS partners."

When promoting the world's #1 RISC architecture, the MIPS® partners are, "rah rah go team." But when it comes to getting the design win, well, that's when the loving stops. See, they might be partners, but they're also competitors.

Now, it would have been nice to have each of the MIPS partners say a few words about their individual strengths. But frankly, each partner has their own virtues and just way too many strong points to mention in one ad. (That, and the fact that they couldn't agree on who would go first.) So to simplify matters, just remember this: each partner is turning out incredible versions of this open, scalable architecture.

it's surprising they can be humble after getting a design win.

Which means the partner you select will give you the perfect embedded processor for your design. You can also expect the broadest range of industry leading tools. So your idea gets to market faster. And it gets there for less than those conventional embedded processors.

If you'd like to see the online version of this heartfelt corporate harmony, visit www.TeamMIPS.com.

Partners working together. Each with their own strengths. Competitors fighting for your business. May the best company win.

www.TeamMIPS.com

Integrated Device Technology, Inc. | LSI LOGIC | NEC | Philips Semiconductors | TOSHIBA

MIPS RISC CERTIFIED POWER

Only MIPS RISC embedded processors offer you the most incredible choice of price/performance, manufacturing expertise and development tools.

SiliconGraphics
MIPS Group

Speedy Virtual Interface Over ATM Networks Made Practical

A high-speed PCI-based interface card for PCs or workstations called MINI (Memory-Integrated Network Interface), makes it practical to run video, multimedia, and cluster applications over ATM (asynchronous transfer mode) computer networks. Developed by Sarnoff Corp., Princeton, N.J., MINI incorporates concepts from the just-announced Virtual Interface (VI) Architecture standard.

MINI can send and receive data over ATM networks at approximately five times the bandwidth of current 100Base-T Ethernet technology. It also achieves 10 to 50 times lower latency, reducing considerably potential delays in starting data transmission. The result is a huge increase in overall communication performance, along with a substantial reduction in processor cycles required for data movement.

Under MINI, an application such as a network browser or videoconferencing tool can request exclusive access to one or more "virtual network interfaces." Once the connection is established, the operating system is no longer involved. Conventionally, by contrast, computers treat a network connection as just another shared resource, and keep the OS involved as a middleman throughout the connection. OS intervention slows down the communication process by adding to the load on the processor. For further details on MINI, contact Sarnoff's Tom Lento at (609) 734-3178; fax (609) 734-2040; e-mail: *tlento@sarnoff.com.* RE

Thermal Imaging Enhances Vehicle Battery Management

Batteries remain the single-most expensive and technologically challenging obstacle on the road to practical, cost-effective hybrid-electric vehicles. Considering the high cost of the batteries used in these vehicles, it's essential that they last beyond their typical three-to-five-year lifespan. Overtemperature conditions, such as those encountered as a result of overcharging, greatly shorten battery life through accelerated corrosion, chemical imbalances, and thermal strains on electrode materials. Consequently, any advances that help prevent this condition can bring about an order-of-magnitude improvement in battery life.

Recognizing this, researchers at the Southwest Research Institute, San Antonio, Texas, are focusing on thermal imaging to analyze battery behavior under certain conditions. One of these conditions is fast charging that's completed in under 20 minutes or at extreme temperatures. To date, thermocouples have been used to monitor a battery's temperature, but getting enough of these devices on a battery to monitor it effectively is extremely difficult and financially prohibitive. Thermocouples also may not register peak temperatures, making it difficult to detect a battery nearing its heat limit.

As an alternative to thermocouples, thermal imaging has proven effective by its ability to detect temperature differences of up to 5°C between the hottest and coldest regions of a battery under test. Thermocouples, on the other hand, detected only 2° or 3°C differences. According to Ed Bass, a research engineer at Southwest, this temperature difference, if left undetected under fast-charge conditions, can reduce battery life by an order of magnitude. With precise temperature monitoring now available, battery management techniques now have the information necessary to greatly extend the life of available chemistries. Contact Ed Bass at (210) 684-5111, fax (210) 522-3547; *www.swri.org.* PM

Aerogels Could More Than Double Computing Speeds

Researchers at the Semiconductor Research Corp. Center for Advanced Science and Technology (CAIST) at Rensselaer Polytechnic Institute, Troy, N.Y., are creating and studying aerogels, which are substances so porous that they're more air than solid material. When used as insulators on computer chips, these porous materials could more than double the speed of computing.

Good insulators—materials with a low dielectric constant—let designers place lines close together and do not slow down the signal. Silicon dioxide, the material now used on most chips, has a dielectric constant of about 4. Decreasing that number to 2 could at least double the speed of computers. Polymers, which are also being studied by CAIST researchers, could bring the number down to about 2.5. Air, the perfect insulator, is rated at 1.0. However, you can't hold chips together with air, thus the probe into aerogels.

CAIST researchers are producing detailed studies of the aerogels and the processes by which they're created, as well as computer models to predict their performance and final properties. Three members of Rensselaer's Isermann Chemical Engineering Department have successfully created highly porous silica films that are between 65% and 90% air, with a dielectric constant ranging from 2.3 to 1.4. The team has shown that it can control porosity and thickness. The new films apparently don't create problems by absorbing water during processing, and they stand up well to high temperature.

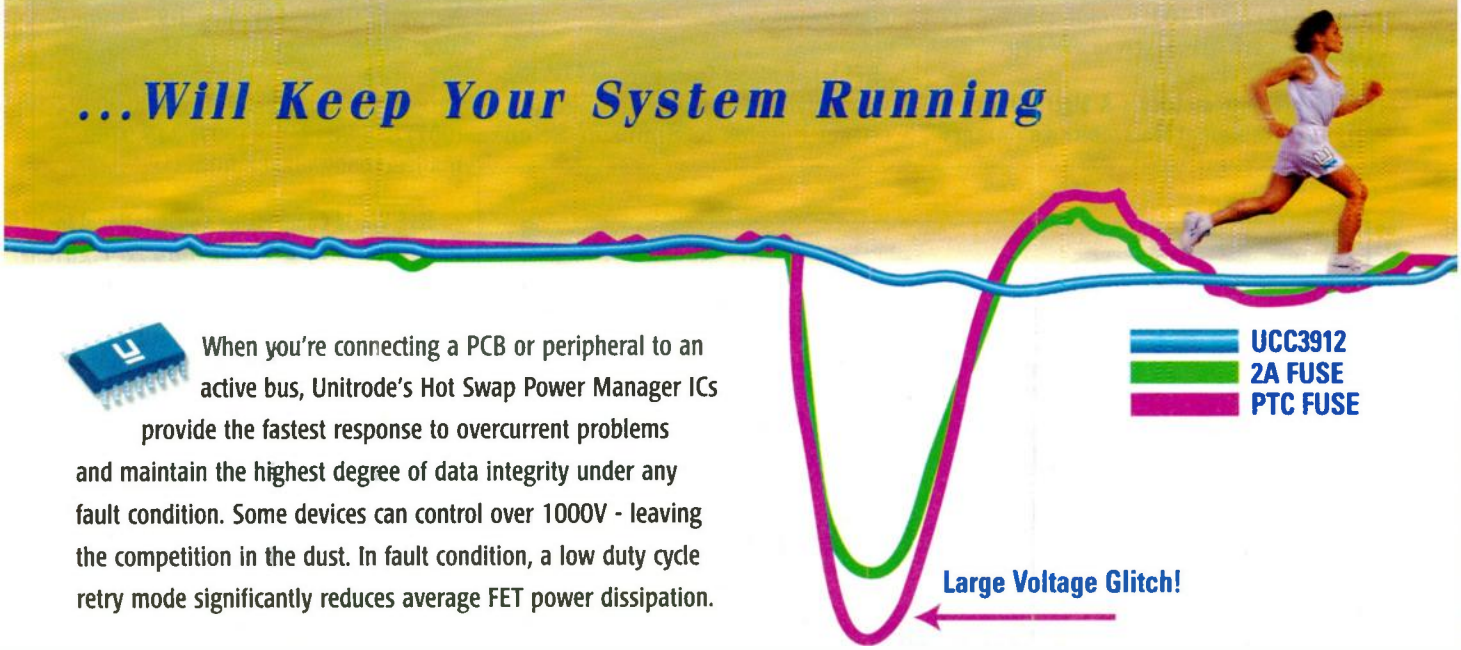
Also, Texas Instruments announced last month that it has demonstrated the successful combination of copper wiring with a similar substance, xerogel. The company estimated that within a decade, combining xerogel with copper wires and new designs could result in devices that are ten times faster than today's best chips.

To find out more, surf into Rensselaer's web site at *www.rpi.edu/dept/NewsComm/Renss_news/tips/.* RE

Edited by Roger Engelke

The Broadest Selection of Hot Swap Power Manager™ ICs

...Will Keep Your System Running



When you're connecting a PCB or peripheral to an active bus, Unitrode's Hot Swap Power Manager ICs provide the fastest response to overcurrent problems and maintain the highest degree of data integrity under any fault condition. Some devices can control over 1000V - leaving the competition in the dust. In fault condition, a low duty cycle retry mode significantly reduces average FET power dissipation.

Full System Operation During Board Hot Swap

PARTS WITH INTERNAL MOSFET

Part Number	Voltage Range	Maximum Current	RDSon
UCC3912	3 to 8V	4A	0.15Ω
UCC3915	7 to 15V	5A	0.15Ω
UCC3916	SCSI TermPower	2A	0.22Ω
UCC3918	3 to 6V	5A	0.075Ω
UCC3920	-3 to -15V	4A	0.1Ω

PARTS WITH EXTERNAL MOSFET

Part Number	Voltage Range	Power Limit
UC1914	4.5 to 35V	Yes
UCC3917	7 to >1000V	Yes
UCC3919	3 to 8V	Yes
UCC3913	-7 to>-1000V	Yes
UCC3921	-3 to>-1000V	Yes

Unitrode's Hot Swap Advantages

- Floating Topology for High Voltage Applications
- High Speed Active Current Limiting Prevents Interruption of Power or Data Flow
- High Speed Overcurrent/Fault Response
- Automatic Fault Retry or Latched Fault Mode
- True Power Limit Control for External FET Devices
- Fault Output Indication
- Shutdown Control

For samples and application information, give us a call today.

UNITRODE

The Linear IC Company Everyone Follows

TEL: (603) 429-8610

http://www.unitrode.com • FAX: (603) 424-3460 • 7 Continental Boulevard • Merrimack, NH 03054

READER SERVICE 201

MAY

100th ACerS Annual Meeting & Exposition, May 3-6. Dr. Albert B. Sabin Convention Center, Cincinnati, OH. Contact The American Ceramic Society Customer Service Dept.; (614) 794-5890; fax (614) 899-6109; e-mail: customersrvc@acers.org; www.acers.org.

Conference on Lasers & Electo-Optics & The International Electronics Conference (CLEO/IEC), May 3-8. The Moscone Center, San Francisco, CA. Contact Amy Hutto, OSA Conference Services, 2010 Massachusetts Ave. N.W., Washington, DC 20036-1023; (202) 416-1980; fax (202) 416-6100; e-mail: cleo.info@osa.org.

IEEE International Conference on Evolutionary Computation, May 3-9. Ankorage, AK. Contact Patrick K. Simpson, Scientific Fishery Systems Inc., P.O. Box 242065, Anchorage, AK 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@alaska.net.

IEEE International Conference on Neural Networks (ICNN '98), May 3-9. Anchorage, AK. Contact Patrick K. Simpson, Scientific Fishery Systems Inc., P.O. Box 242065, Anchorage, AK 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@alaska.net.

IEEE World Congress on Computational Intelligence, May 3-9. William A. Egan Civic and Convention Center, Anchorage, AK. Contact Patrick K. Simpson, Scientific Fishery Systems Inc. P.O. Box 242064, Anchorage, AK 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@alaska.net.

Seventh IEEE International Fuzzy Systems Conference, May 3-9. Anchorage, AK. Contact Patrick K. Simpson, Scientific Fishery Systems Inc., P.O. Box 242065, Anchorage, AK 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@alaska.net.

IEEE International Symposium on Electronics & the Environment, May 4-6. Oak Brook, IL. Contact ISEE Conference Registrar, 445 Hoes Lane, Piscataway, NJ 08855-1331; (732) 562-3875; fax (732) 981-1203; e-mail: j.slaven@ieee.org.

IEEE/IAS Industrial & Commercial Power Systems Technical Conference (I&CPS), May 4-7. Edmonton, Alberta, Canada. Contact Marty Bince, Modicon Canada Ltd., 5803 86th St., Edmonton, Alberta T6E 2X4, Canada; (403) 468-6673; fax (403) 468-2925.

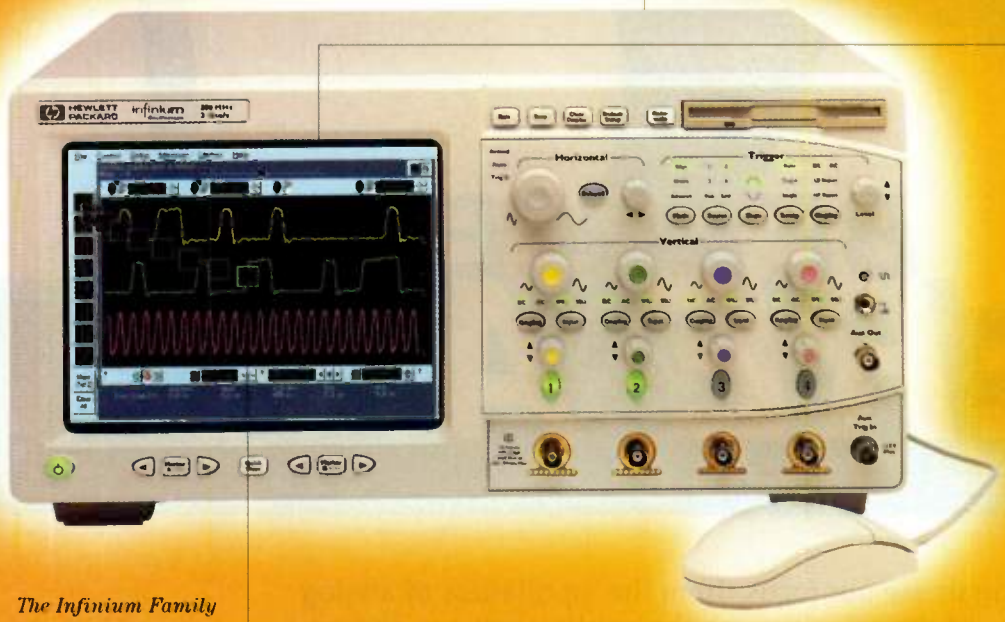
IEEE Radar Conference, May 12-14. Contact Scott Ramey, 2501 West University, MS 8056, McKinney, TX 75070; (972) 952-4409; fax (972) 952-3071; e-mail: sramey@ti.com.

IEEE International Conference on Acoustics, Speech & Signal Processing (ICASSP '98), May 12-15. Seattle Convention Center, Seattle, Washington. Contact Les E. Atlas, Dept. EE (FT 10), University of Washington, Seattle, Washington 98195; (206) 685-1315; fax (206) 543-3842; e-mail: atlas@ee.washington.edu.

Great.

You forgot how to measure that rise time.

Now you've got to waste 10 seconds relearning it.



The Infinium Family
*Starting at $9,995**

Windows® 95–based graphical interface

- *500-MHz to 1.5-GHz bandwidth*
- *Up to 8-Gsa/s sample rate*
- *2- and 4-channel models*

Drag-and-Drop measurements

Some call it the forgetting curve. The last time you used your scope, you spent a lot of time learning how to measure the rise time of the third edge. But now you can't remember how you did it—and that means you have to waste even more time figuring it out all over again.

Unless you've got the new Infinium oscilloscope from HP.

Infinium's Windows 95–based graphical user interface lets you make those difficult measurements quickly (even if it's been months since you touched a scope). There's a powerful built-in help system that's always there when you have more questions—even tough ones. And with an analog-like front panel, Infinium finally makes simple functions simple again.

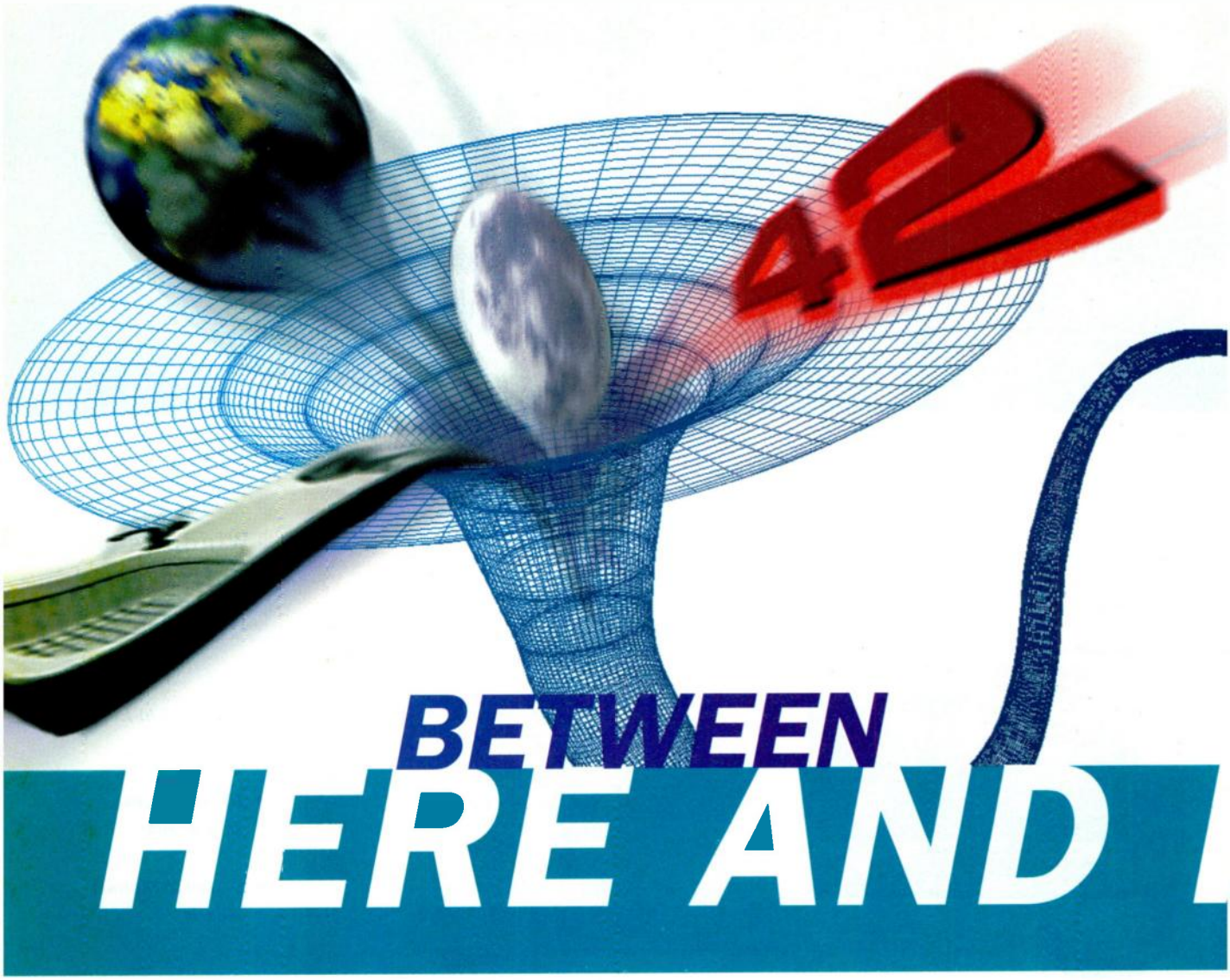
To find out how you can spend less time fighting your scope, call HP Direct at **1-800-452-4844, Ext. 5695**. We'll send you a FREE Infinium CD-ROM or brochure and answer questions about our demo program. Or, check out our Web site: **www.hp.com/info/Infinium15**

Then you can forget the forgetting curve.

HEWLETT® PACKARD

US list price. ©1998 Hewlett-Packard Co. TMEMD804/ED Windows is a U.S. registered trademark of Microsoft Corporation.

READER SERVICE 152



BETWEEN HERE AND

At Exar, mixed signals are our focus, from the infiniteness of analog to the singularity of digital, although the applications are diverse:

We've recently released a single chip compliant with every serial protocol on Earth. Don't design a router without it. At the same time, we released single-chip solutions for video and scanning systems. And at no extra charge, we threw in signal conditioning, gain, and digitization functions without increasing the footprint or power demands.

And we've practically pioneered the silicon sensing device.

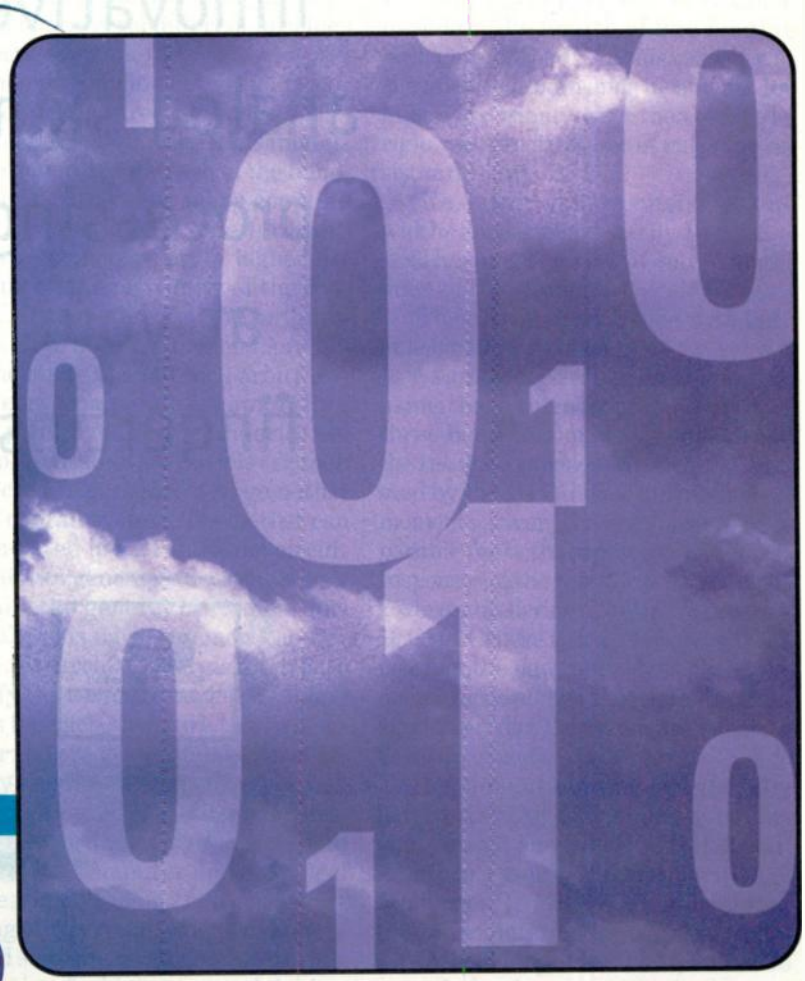
Ours is accurate down to 0.15 PSI, which is about 20x more sensitive than the next best solution. The only thing more lop-sided than its performance advantage over the competition, is its price advantage.

So it makes us wonder what the rest of the world is doing?

More important, what are you doing?

If it's anything to do with sensing, converting, or communicating analog and digital signals, it's easier with Exar, AD Infinitum. 800-366-9742, www.exar.com.

Come to think of it, that wasn't so hard.



ERE IS THE ~~HARD~~ PART.

Exar

EXAR

AD INFINITUM™

READER SERVICE 127

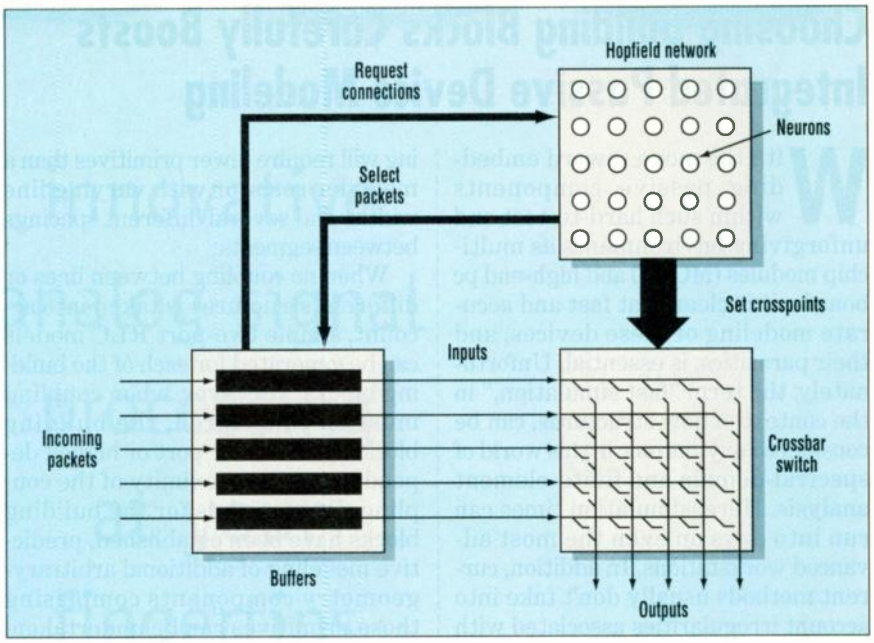
they call the Universally Reconstructable Artificial Neural (URAN) network, is arranged so that any neuron can be interconnected with any other via programmable "synapses."

Rod Webb, manager of the URAN team at BT Laboratories, says that prototype devices have been designed to simulate high-speed crossbar switches. Devices have been made with varying sizes of neuron arrays, including versions with 81-by-81 and 108-by-108 matrices.

The devices are programmed by setting voltage levels at the intersection of the synapse interconnections so as to "weight" them according to a particular problem algorithm. "It's similar in concept to setting the precision potentiometers to represent variable values in an analog computer," Webb says. The device is scalable, so bigger arrays can be made by "tiling" the URAN chips.

An early project is to simulate a crossbar switch programmed to make decisions on the routing of data packets through the network from 100 independent inputs to a similar number of outputs. The idea is to optimize the configuration of the switch in real time to take into account varying traffic flows. Webb says the project involves a Hopfield network controlling a crossbar switch and selecting data packets to be launched into the switch from among those waiting in the input buffers *(see the figure)*.

There is a neuron corresponding to each switch crosspoint, and packets may be taken out of the buffers in any order.



British Telecom and Korea Telecom jointly developed a neural network IC that may be used in a crossbar packet switch controller.

Each packet is addressed to one of the outputs. Although this is not a practical example, it does demonstrate the problem of choosing one setting from an enormous number of possibilities that arise in real switches and networks.

In a real network, according to Webb, the device can make decisions on network reconfiguration to meet traffic demands much faster than conventional software-controlled systems. He says that trials have shown that the URAN device can learn to reconfigure itself in less than 100 µs. Another potential application for URAN is in broadband mobile communications networks, where the rapid and dynamic reallocation of radio channels could greatly increase the efficiency and capacity of cellular telephone networks, continues Webb.

The URAN device has already been produced in research quantities, and BT will soon be using it in a variety of network applications on an experimental basis. But Webb reckons it could be another five years before the device is ready for commercial production and deployment in real networks.

Contact Rod Webb at rod.webb@bt-sys.bt.co.uk.

Peter Fletcher

CMOS Motion Detector Also Provides A Simultaneous Video Output

The ability to detect motion with CMOS active-pixel sensors (APS) is not new. On the other hand, accomplishing this task while simultaneously allowing normal video output is. This dual capability it is at the center of an ongoing effort at Nikon Corp.'s Semiconductor Device Center, Tokyo, Japan. The research focuses on the development of a 256-by-256 smart image sensor that can provide both on-chip motion detection and high-quality video output through via a buried charge accumulator and sensing transistor array (BCAST) pixel architecture.

The need for such a device is rooted in the specific performance requirements of the continually growing global communications marketplace. These requirements include high-quality images, increased functionality, miniaturization, and low cost. The need to be able to generate analog video signals also exists, because the signals often contain critical information associated with a variety of sources. They also are useful for achieving the advanced feature capabilities found in global communications applications.

Nikon's motion-detector image sensor consists of motion processing and video circuitry, a pixel array, and associated components. The motion processing circuit includes two sample-and-hold circuits (S/H), two inverters that act as a voltage comparator, and logic functions. While a pixel is being read out, one S/H circuit's output is compared to the comparator's threshold voltage. Motion is detectable if the difference between the two exceeds a specified sensitivity constant.

The video circuit consists of a source-follower amplifier and a S/H circuit. The S/H circuit uses a correlated double sampling (CDS) technique that significantly reduces the pixel reset and 1/f noise, as well as the threshold variation

In 1983, Galil introduced the first digital, single-axis motion controller without tachometer feedback.

TODAY WE MOVE THE WORLD

Today, more than 200,000 Galil motion controllers are at work worldwide, helping to build semiconductors, textiles, medical equipment and manufacturing products. Our revolutionary innovations have grown into the world's most complete line of high-performance motion controllers for steppers and servo motors. Up to 8 axes of motion, including linear and circular interpolation, gearing and ECAM for ISA, Compact PCI, VME and RS232 standalone environments. All with uncommitted I/O and memory for user-defined programs.

Let the value in Galil controllers move you, too.

CALL 1-800-377-6329 TODAY
FOR YOUR FREE PRODUCT GUIDE, INCLUDING A TECHNICAL REFERENCE ON MOTION CONTROL.

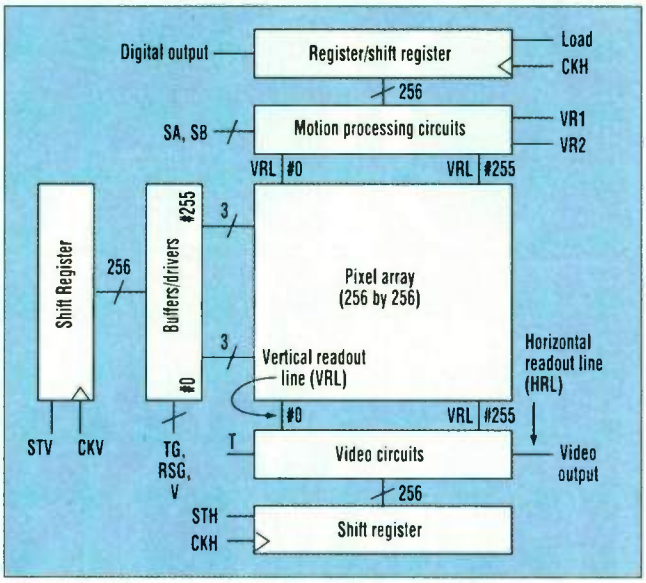
Visit us at www.galilmc.com

GALIL

READER SERVICE 131

known to be a cause of fixed-pattern noise (FPN). The FPN, which is suppressed by the CDS circuitry, is 76 dB

Nikon's sensor is fabricated on a 2-µm twin-tub CMOS process. Each of the sensor's pixels consist of a buried photodiode (BPD) to accumulate the holes generated by the incident light; an n-channel JFET for read-out of signals from the pixel with a source-follower operation; and a row-select transistor. The sensor's pixel size is 18.8 by 18.8 μm^2, and the array has a fill factor of 35%. A transfer gate is used for transferring the holes to the JFET gate. A rest gate resets and controls the JFET gate. All gates in the pixel are p-channel MOS transistors.



The video circuitry in the new motion detector uses a correlated double-sampling technique that significantly reduces pixel reset noise, 1/f noise, and threshold variation.

When the sensor is operating, the pixel's signal is output to a vertical readout line containing a motion processing and a video circuit. Here, it is simulataneously split into digital and analog signals by the motion-processing and video circuits, respectively. The digital signal is then output from the chip through a horizontal/shift register, while the analog signal is output from the chip through a horizontal readout line. All sensor control signals are applied from an external signal generator.

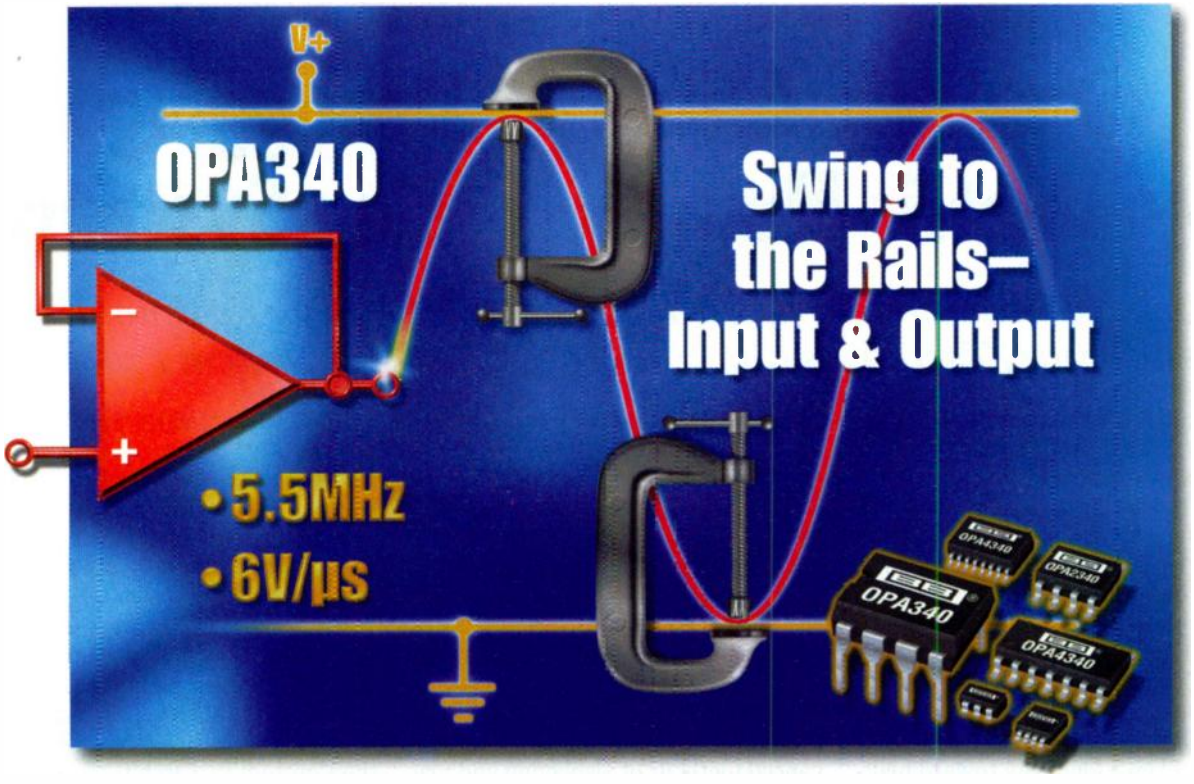
At a minimum, the sensor has a total power dissipation of 100 mW at about 5 V and 60 frames/s. Random noise on its output node is 69 µV rms, and dynamic range is 78.2 dB. The digital output signal's minimum sensitivity of motion detection is about 1.7% of saturation, with saturation being equivalent to 560 mV. Additionally, it is characterized by a conversion gain within the pixel of 14 µV/hole, a peak quantum efficiency equivalent to 0.28, and a maximum frame rate of 240 frames/s.

For additional information on this development or ongoing research into its potential commercialization and performance improvements, contact Nikon Corp. at +81 3 3773 1110 or by fax at +81 3 3773 1167.

Cheryl Ajluni

Precision PLUS™

1mV–Rail-to-Rail!



Squeeze Close to the Rails...

Burr-Brown's new **OPA340** series CMOS op amps provide the best rail-to-rail performance. Output swings to a mere 1mV from the supply rails with 100kΩ loads. With 10kΩ loads, output swings to within 10mV—better than what you're using now. And input common-mode range extends 500mV beyond the supply rails, so it works in all your circuit configurations, including G=1 buffer.

It's Fast, Too!

With 6V/µs slew rate and 5.5MHz bandwidth, the OPA340 is not just another *sloooow* CMOS amplifier. Its excellent dynamic performance and wide input/output swing make it great for driving A/D converter inputs. It's also suited to a wide range of portable and battery operated equipment...only 750µA supply current.

Single, dual and quad versions, plus a wide range of packages including SOT-23, MSOP, SSOP, SO and DIP, give you true design flexibility.

Key Specifications:

- Rail-to-Rail.....Input and Output
- V_{OS}.....500µV max
- Bandwidth.....5.5MHz
- Slew Rate.....6V/µs
- THD+N.....0.0007% at 1kHz
- Supply Range.....+2.5V to +5.5V
- Quiescent Current.....750µA/Channel
- Package Options:
  - OPA340 (single).....SOT-23-5, SO-8, 8-pin DIP
  - OPA2340 (dual).....MSOP-8, SO-8, 8-pin DIP
  - OPA4340 (quad).....SSOP-16, SO-14, 14-pin DIP

OPA340 series is priced from $0.52/channel (quad) in 1000s.

FAX*LINE*# 11404 • READER SERVICE 80

www.burr-brown.com

BURR - BROWN®

Burr-Brown Corporation • P.O. Box 11400 • Tucson, AZ • 85734-1400 • Call **(800) 548-6132** or use **FAX*LINE* (800) 548-6133** • **http://www.burr-brown.com/**

Distributors: Anthem: (800) 826-8436 • **Digi-Key Corp:** (800) 338-4105 • **Insight Electronics:** (888) 488-4133 • **J.I.T. Supply:** (800) 246-9000 • **Sager Electronics:** (800) 724-3780 • **SEMAD (Canada):** (800) 567-3623

Don't Be Afraid Of Debugging Symmetric Multiprocessing Systems

Using Conventional Logic-Analysis Tools And The Pentium Pro Architecture, These Tips Can Help You Tame Your System Problems.

MICHAEL PATTERSON AND JOHN FRIEDMAN, Hewlett-Packard Co., P.O. Box 50637, Palo Alto, CA 94303-9512; (800) 452-4844.

The day when you'll be responsible for designing a system involving symmetric multiprocessing (SMP) may be closer than you think. Clearly, multiprocessor systems are becoming more commonplace. And, having the up-front knowledge about what hooks should be designed into your system, and what it will take to get your design through the debug and verification phase will go a long way toward making your efforts in this new and exciting area a success.

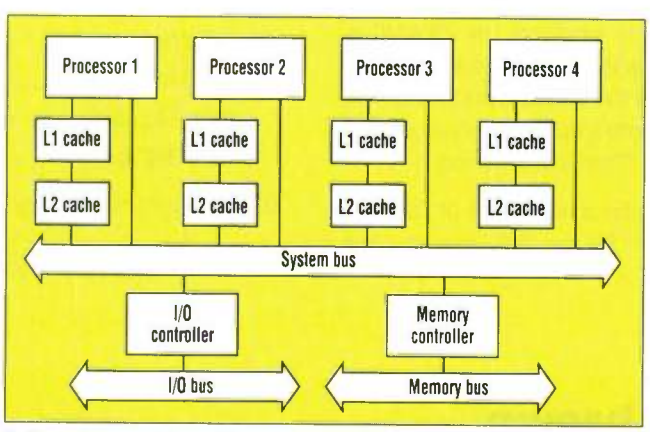
Unquestionably, SMP systems can be intimidating at first glance, with endless complexities and possibilities for failure. Fortunately, traditional debugging tools are still quite useful for multiprocessing systems. If you know how to use them properly, you can track and discover the root causes of most difficult problems.

Understanding the need for debugging your SMP systems before you begin your design can greatly improve effectiveness. If you know which tools you'll need for debugging, and the design hooks into your hardware required to use them effectively, you will be able to predict accurate schedules and budgets, and possibly even cut down on debugging time.

For example, your logic analysis system will need all of the features used in a single processor system, as well as processor-specific probes designed for multiprocessing systems. These probes have new features designed to find problems like transaction tracking, interrupt handling, I/O and memory access difficulties, data corruption, and cache coherency problems. Also, deep acquisition memory and time-correlation between multiple-analysis systems are required for a multiprocessor debugging setup. Advanced methods of displaying and manipulating the information are useful for handling the large amount of data acquired in the process.

Processor-specific run-control tools also have the ability to operate symmetric multiprocessing systems. The SMP run-control tool needs to be able to control how the processors run, stop, and step in a way that will give the most information with the least amount of interference and intrusion. The ability to set breakpoints on each processor using registers is required, and the ability to read or write memory through a specific processor in the system can help solve coherency problems.

Through answering some of the tough questions that come up in debugging SMP systems, this article will concentrate on the shared-memory multiprocessor design most recently used in the Pentium Pro architecture. In this design, all processors share a common bus with other agents, using arbitration to decide who owns the bus at any time. Physical memory and access to I/O is identical for each processor, although each processor has its own first and second-level cache. If the processors didn't have their own caches, the system bus would quickly become overloaded with memory requests. Unfortunately, this means that some information never reaches the bus, requiring caching to be turned off. However, turning off caching can hide some of the problems you are trying to debug *(fig. 1)*.



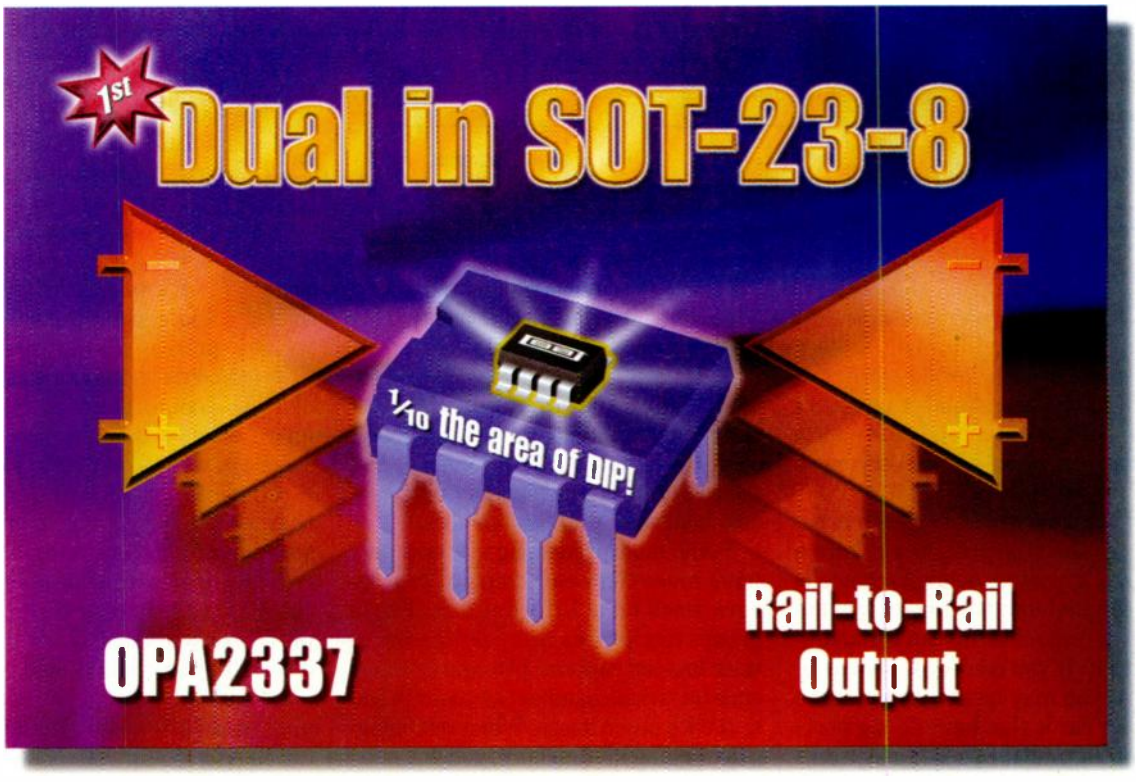
1. Typical symmetric multiprocessing systems connect several processors to a common system bus. They each have their own memory cache. In this instance, the system contains four processors.

Setting Up For Debug

How do you set up a logic analyzer and run-control system for debugging a multiprocessing system? Only a single logic analyzer and probe are needed for the system bus because it is shared by all the processors in shared-memory SMP systems. This setup is the same as the one used for

Precision PLUS™

World's Smallest Op Amps



More Op Amps... Less Space!

The **OPA2337** is the world's smallest dual...two complete high performance op amps in one tiny SOT package! Beware of impostors; this is a real SOT-23 body with eight fine-pitch (0.025") leads. How's your eyesight?

Single supply operation with rail-to-rail output (within 10mV!) makes the OPA2337 perfect for portable equipment and all general purpose applications. Quiescent current is only 450µA yet it can handle your dynamic signals (1.5MHz, 1V/µs). And it's CMOS with only 10pA input bias current.

Burr-Brown offers a complete selection of micropackage op amps. Check our brief listing below and find more on our web site, including *SpeedPLUS* 400MHz+ op amps.

Products	Description *(all are rail-to-rail output)*	Single Dual/Quad	Power Supply Single (V)	I_Q/Ch. (µA)	Price/Ch. (1k+)	FAX*LINE*# (800) 548-6133	Reader Service #
OPA336	*micro*Power, CMOS	S,D,Q	2.3 to 5.5	20	$0.47	11380	88
OPA340	High Speed, Rail-to-Rail I/O	S,D,Q	2.5 to 5.5	750	$0.52	11404	89
OPA237	Low Power, Single Supply	S,D,Q	2.7 to 36	170	$0.81	11327	90
OPA337	Single Supply, CMOS	S,D	2.5 to 5.5	450	$0.26	11410	91

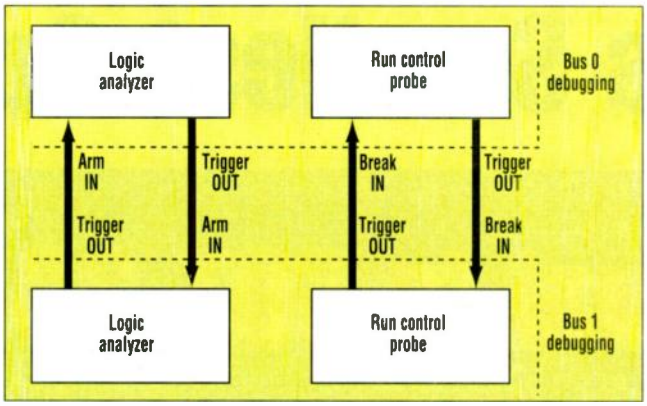
www.burr-brown.com

BURR - BROWN®

Burr-Brown Corporation • P.O. Box 11400 • Tucson, AZ • 85734-1400 • Call (800) 548-6132 or use FAX*LINE* (800) 548-6133 • http://www.burr-brown.com/
Distributors: Anthem: (800) 826-8436 • Digi-Key Corp: (800) 338-4105 • Insight Electronics: (888) 488-4133 • J.I.T. Supply: (800) 246-9000 • Sager Electronics: (800) 724-3780 • SEMAD (Canada): (800) 567-3623

debugging single-processor systems. But, additional logic analyzers may be needed for probing additional buses for I/O or memory.

The logic analyzer probe attaches at a single processor socket. Because the bus on a symmetric multiprocessing system is shared, most information that you might want to collect from any processor will be available at the logic analyzer probe, no matter where it's physically attached. This simplifies the connection to the system bus and minimizes the additional electrical load. SMP processors will have some signals that aren't shared, so you may need to select a specific processor if you are trying to sample these signals.



2. In debugging multiple buses, each bus needs its own tools. These tools must to be able to communicate with each other for an accurate view of how the two buses relate. This diagram shows how tools used to debug a two-bus system would be attached.

Only one run-control system is required, because the processors share a single debug port. A debug port needs to be designed into the target system so the run-control setup can communicate with it. If you can't design in a debug port, you may be able to purchase interposer cards that have debug ports on them. In multiprocessing systems that use JTAG for their debug ports, all the processors and other devices on the board are connected into a single chain that can be accessed through the debug port. It is important that your connections are correct, otherwise damage may result when the processor probe is attached to the system.

The run-control software needs to know which devices (and their order) are on the debug port to interpret the data correctly. This information is known as a "scan chain." In some run-control systems, the scan chain is determined automatically by sending identification queries to all locations on the chain that can contain an agent. If you allow the run-control unit to "autodetect" a scan chain, make sure you know that the operation is safe. Some devices may not be built to the correct specifications of the scan chain, and could be damaged by the commands used while autodetecting. Make sure that you know all of the devices on your board, then your run-control system can detect those devices without damaging them. On most modern Intel-designed boards, the only devices on the scan chain are the processors, which are safe to autodetect. Again, if you did not design the board, and you aren't certain, contact the board's designer or manufacturer, and ask them what your scan chain is.

Some multiprocessing systems may have more than one group of processors, each on a different bus. These groups can have as many processors as their bus can support, plus one agent on each bus which handles the communication with other buses. When setting up a debugging system here, you will need multiple analyzers and run-control units, one hooked into each group. On Hewlett-Packard systems, for example, you can use BNC cables to link the two run-control systems together (connecting the Trigger Out of one to the Break In of the other) and break the entire system. You can either use BNC cables to attach two separate analysis systems together, or use two separate cards to create a cross-trigger to correlate traces on both buses *(fig. 2)*.

Running And Stepping

What does it mean to "Run Until" and "Step" in an SMP system? In a single processor system, Run Until and Step are used to control the execution of the system so you can see what changes small parts of code make to the system. Step advances a program one instruction at a time, and is usually supported in the processor itself. Run Until advances the program to a predetermined point usually set as a breakpoint in the processor. Your run-control system can be used to Step, or to set breakpoints as locations to Run Until. In some processors that don't have the Step function built in, a simulated Step can be made by setting a breakpoint on the instruction after the current one.

In a symmetric multiprocessing system, both functions are more complex. Ignoring the possibility of finding the processor your program is running on for the moment, what do you do with the other processors while the processor you have selected is stepping? There are two usable possibilities: Run them or Stop them.

Running the processors while stepping the selected processor is the closest you can come to the normal operation of the system. In many cases, this is the only option available. For example, other processors may be handling an interrupt request; writing to memory that is vital for your primary processor's operations; or even performing a critical, uninterruptible operation. On the Pentium Pro system, the boot processor will mark other processors dead if they haven't notified it that they have started by a specific time. Stopping those processors while stepping the boot processor will cause them to be marked dead. In any of these cases (and many others), out-of-sync processors could either crash the system, or hide the problem you are trying to find.

There are some cases where it is better to stop the other processors. By stopping them, you can ensure that only the target processor is performing operations. There are a few common situations when this is useful. One is when an operating system runs a single process on a single processor. You can keep track of a particular program's activities without it being modified by another processor. Additionally, you can use this mode when you need to examine the activity of a single processor for a few steps. One caveat, though, your system may be unstable after operating in this mode.

No matter what you do while you are stepping a processor in an SMP system, it is possible that your Step will cause the processors to go out-of-sync. Figure 3 shows a four-processor system that was stopped when T=1. Processor one was then stepped while the others were run. Processors two and four were in the middle of executing an instruction

Solutions PLUS™

Puzzled by Sensor Solutions?

Choose Your Piece!

From one piece to a complete mixed signal solution, **Burr-Brown** can help you unlock the solution to your sensor application puzzle.

Visit our website for complete data sheets detailing sensor/signal conditioning solutions.

DELTA SIGMA A/D CONVERTERS

Product	INL (% FSR)	Input Ranges	Resolution (Bits at 10Hz)	Resolution (Bits at 1kHz)	Power Dissipation (mW)	Price (1kpcs)	FAX*LINE* # 1-800-548-6133	Reader Service #
ADS1212	±0.0015	±312mV to ±5V	22	16	1.4	$7.25	11360	96
ADS1214	±0.0015	±20mV to ±320mV	22	16	1.4	$7.25	11368	97

GENERAL PURPOSE A/D CONVERTERS **no missing codes*

Product	Resolution (Bits	INL (LSB)	DNL (Bit)	Sample Rate (kHz)	Power (mW)	SINAD (dB)	Price (1kpcs)	FAX*LINE* # 1-800-548-6133	Reader Service #
ADS7813	16	±2.0	16	40	35	87	$20.00	11302	98
ADS7817	12	±1	12	200	2.3	71	$5.18	11369	99
ADS7822	12	±0.75	12	75	0.54	71	$4.64	11358	100
ADS7825	16	±2.0	16	40	50	86	$28.46	11304	101

INSTRUMENTATION AMPLIFIERS

Product	Description	I_Q (µA)	Offset Voltage (µV) max	Offset Drift (µV/°C) max	I_B (nA) max	Price (1kpcs)	FAX*LINE* # 1-800-548-6133	Reader Service #
INA122	Single-Supply, *micro*Power	60	250	3	24	$2.50	11388	102
INA128	Precision, Low Drift	700	50	0.5	5	$3.38	11296	81
INA125	On-Board V_{REF}	460	250	2	20	$2.10	11361	82
INA126	Low Cost MSOP Package	175	250	3	25	$1.60	11365	83

OPERATIONAL AMPLIFIERS

Product	Description (all are rail-to-rail output)	Single/Dual Quad	Power Supply Single (V)	I_Q (µA)	Price/Ch. (1kpcs)	FAX*LINE* # 1-800-548-6133	Reader Service #
OPA241	*micro*Power, Precision	S	2.7 to 36V	24	$1.06	11406	84
OPA336	*micro*Power, CMOS	S, D, Q	2.3 to 5.5V	20	$0.47	11380	85
OPA340	High Speed, Rail-to-Rail I/O	S, D, Q	2.5 to 5.5V	750	$0.55	11404	86

www.burr-brown.com

BURR-BROWN®

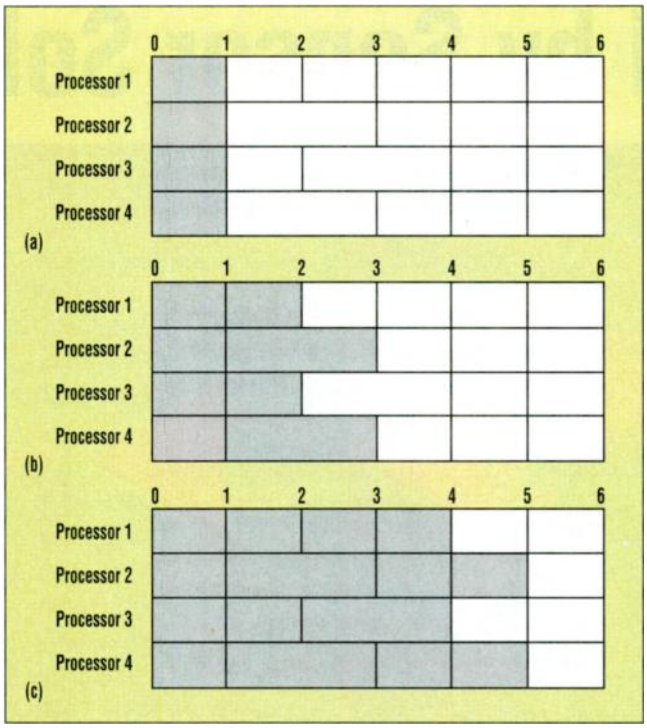
Burr-Brown Corporation • P.O. Box 11400 • Tucson, AZ • 85734-1400 • Call (800) 548-6132 or use FAX*LINE* (800) 548-6133 • http://www.burr-brown.com/

Distributors. Anthem: (800) 826-8436 • Digi-Key Corp: (800) 338-4105 • Insight Electronics: (888) 488-4133 • J.I.T. Supply: (800) 246-9000 • Sager Electronics: (800) 724-3780 • SEMAD (Canada): (800) 567-3623

when processor one completed its Step, and since they can't be stopped in the middle of an instruction, they continued until they could stop. When the system was run again, a snapshot at T=4 shows that the processors never got back in synchronization. In some operating systems, the timing of the processors is crucial. A processor that is ahead or behind where it should be could miss a vital piece of information, or send needed data too late. Luckily, most operating systems aren't that picky about the synchronization of the processors.

The Run Until problem is more complex. The goal of Run Until is to stop the execution of a process when it reaches a certain point. Unfortunately, it is difficult to tell which processor will execute the process. You can set either a hardware or software breakpoint on each of the processors where you want to stop, and set your run-control tool to break all of the processors when any of them break. At this point, you can run all of the processors. When the system stops, one of the processors will be stopped at the specified location, and the others will be stopped where they would be during normal operation.

The single processor concepts between Step and Run Until do not translate perfectly into SMP, but with the proper tools you should be able to modify these ideas to work in your symmetric multiprocessing system.

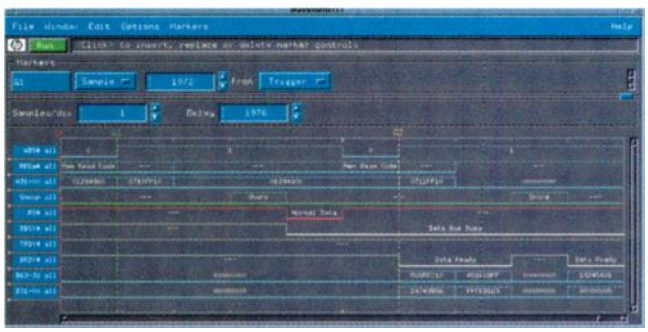


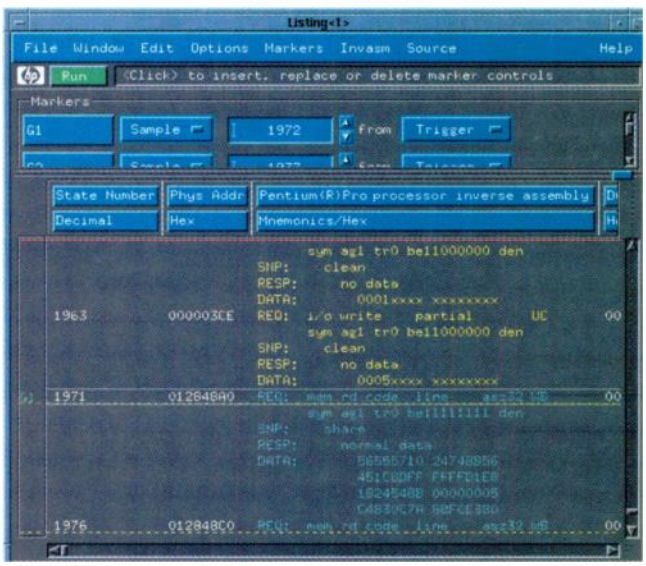
3. In this example, all four system processors were stopped at T=2. However, processors Two and Four had to complete their current instruction, effectively placing them one clock ahead (a). When the processors run again, it's obvious that they don't regain synchronization (b). In fact, they never do synchronize with each other (c).

Watching The Processor

How do I observe activity for a given processor? Unlike single-processor system buses of the past, most SMP buses are organized using transactions. A processor interacts differently with its surrounding components when transactions are used instead of cycles. For example, in a simple processor's read cycle, an address is transmitted, and the memory system returns the requested data. This cycle can complete in as few as two system clocks. SMP transactions can be much more complex. The same transaction on an SMP system starts with the processor grabbing the bus through arbitration, initiating the read request with an address, checking for cache coherency through snooping, receiving the data, and finally waiting for an indication that the transaction has completed successfully. Error detection and correction may require additional time.

The key difference between single- processor and SMP buses is that transaction-oriented buses tend to have features that allow outstanding transactions to be heavily overlapped. A four-way SMP system bus might allow eight or more transactions to be outstanding at any given time. In contrast, single-processor cycle-oriented buses only allow one cycle to execute at a time. These systems often allow the last cycle to complete on the first clock of the new cycle. These bus design optimizations are potentially complex, but pale in comparison with their SMP transaction-oriented cousins.

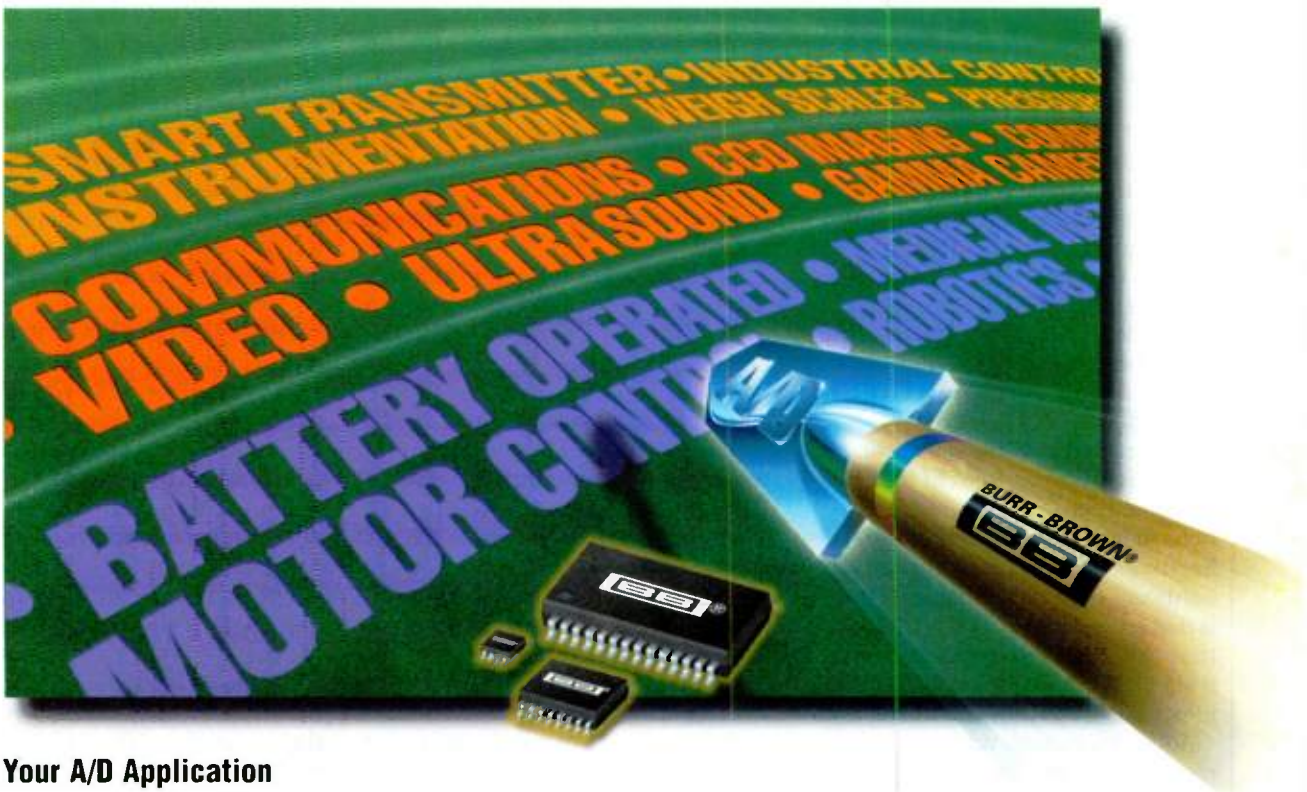




4. For a low-level view of the activity on the system bus, raw system data is displayed as it occurs in time relative to the system clock (a). This view of system activity helps designers understand and debug issues like transactions that terminate early or not at all. Reconstructed transactions yield a higher-level view of bus activity (b). This "unraveled" display of bus transactions is derived by post-processing the raw data into complete bus transactions. Now high-level issues like functional and addressing errors, and data corruption can be debugged.

Converters PLUS

Target Your A/D Application



Target Your A/D Application

Don't let your design project fall short of its mark! Let **Burr-Brown's** broad line of delta-sigma, high speed, and general purpose A/D converters help you to hit your mark every time! For a complete range of possibilities, target our website.

DELTA-SIGMA A/D CONVERTERS

Product	INL (% FSR)	Input Range	Resolution (Bits at 10Hz)	Resolution (Bits at 1kHz)	Power Dissipation (mW)	Price (1kpcs)	FAX*LINE* # 1-800-548-6133	Reader Service #
ADS1210	±0.0015	±312mV to ±5V	24	20	26	$9.60	11284	103
ADS1212	±0.0015	±312mV to ±5V	22	16	1.4	$7.25	11360	104
ADS1214	±0.0015	±20mV to ±320mV	22	16	1.4	$7.25	11368	105

HIGH-SPEED A/D CONVERTERS **preliminary information*

Product	Resolution (Bits)	Speed (MHz)	Power (mW)	SNR (dB)	DNL (LSB)	SFDR (dBFS)	Supply (V)	Price (1kpcs)	FAX*LINE* # 1-800-548-6133	Reader Service #
ADS800	12	40	390	64	±0.6	61	+5	$29.00	11286	106
ADS803	12	5	116	69	±0.3	82	+5	$9.55	11398	107
ADS824*	10	75	315	59	±0.5	70	+5	$8.50	11403	232
ADS930/931	8	30	66/63	46/48	±0.4	51/49	+3/+5	$3.37/$3.27	11349	233

GENERAL PURPOSE A/D CONVERTERS **no missing code*

Product	Resolution (Bits)	INL (LSB)	DNL* (Bit)	Sample Rate (kHz)	Power (mW)	SINAD (dB)	THD (dB)	Price (1kpcs)	FAX*LINE* # 1-800-548-6133	Reader Service #
ADS7813	16	±2.0	16	40	35	87	–90	$20.00	11302	234
ADS7817	12	±1	12	200	2.3	71	–83	$5.18	11369	235
ADS7822	12	±0.75	12	75	0.54	71	–82	$4.64	11358	236
ADS7825	16	±2.0	16	40	50	86	–90	$28.46	11304	237

www.burr-brown.com

BURR - BROWN®

Burr-Brown Corporation • P.O. Box 11400 • Tucson, AZ • 85734-1400 • Call **(800) 548-6132** or use **FAX***LINE* **(800) 548-6133** • **http://www.burr-brown.com/**

Distributors. Anthem: (800) 326-8436 • Digi-Key Corp: (800) 338-4105 • Insight Electronics: (888) 488-4133 • J.I.T. Supply: (800) 246-9000 • Sager Electronics: (800) 724-3780 • SEMAD (Canada): (800) 567-3623

Why all the complexity? The reason is simple— bus bandwidth. When just one processor is on the bus, its only competition is with a DMA agent or, maybe, a smart I/O agent. With SMP systems a single processor will have to compete with other processors and agents, requiring transaction-oriented buses.

Now, with all that said, you should be able to appreciate the difficulty in tracking a specific processor, let alone a specific transaction, on the system bus. Fortunately, there are ways to handle this. Agents on the SMP system bus, such as the processors, the memory controller, and the I/O controller, have to be able to unravel the bus. Logic analyzer probes and special processor-specific software can unravel the SMP bus in the same way.

Where and how the unraveling occurs affects what kind of measurements you can make. There are two options to unravelling the bus — do it in hardware or do it in software. The hardware approach's main advantage is that triggering on a specific agent, or transaction, or sequence of such events is simple. Unfortunately, this approach is expensive and time consuming to develop. Triggering with software is more difficult and limited, but the solutions are often more flexible and available sooner.

Let's explore the software-tool approach because it is cheaper, and appears long before hardware tools are available. It should be noted that even mainly software-based tools require processor-specific hardware. The probes themselves can be very tricky to design due to system-bus loading constraints. Extra signals and hardware tracking often are needed to unravel the bus with postprocessing software. Luckily, these extra signals can make other useful measurements possible.

The software approach uses the captured trace of bus activity and generated signals to unravel the transactions and display them as aligned transactions. Figure 4 shows a waveform display of the raw bus activity *(a)* and a listing display of the unraveled transaction *(b)*.

The waveform view shows the bus exactly as it occurred in time relative to the system clock. This is useful for understanding and debugging low-level bus issues like transactions that terminate early or not at all.

The listing view shows complete transactions in an "unraveled" format. Unraveling is when the listing postprocessing software processes the raw data into complete transactions. This is useful for observing and debugging high-level issues like functional and addressing errors, and data-corruption problems.

Triggering on simple events like a memory write to a certain location, or an I/O read from a certain device are simple to set up with the software- based approach because transaction address and type information are uniformly given in an early phase of most transactions. Triggering on specific data values for certain transaction types can be much more difficult, if possible at all. To track these types of measurements, the approach used in *"How can I look at auxiliary buses?"* described later, is much more straightforward.

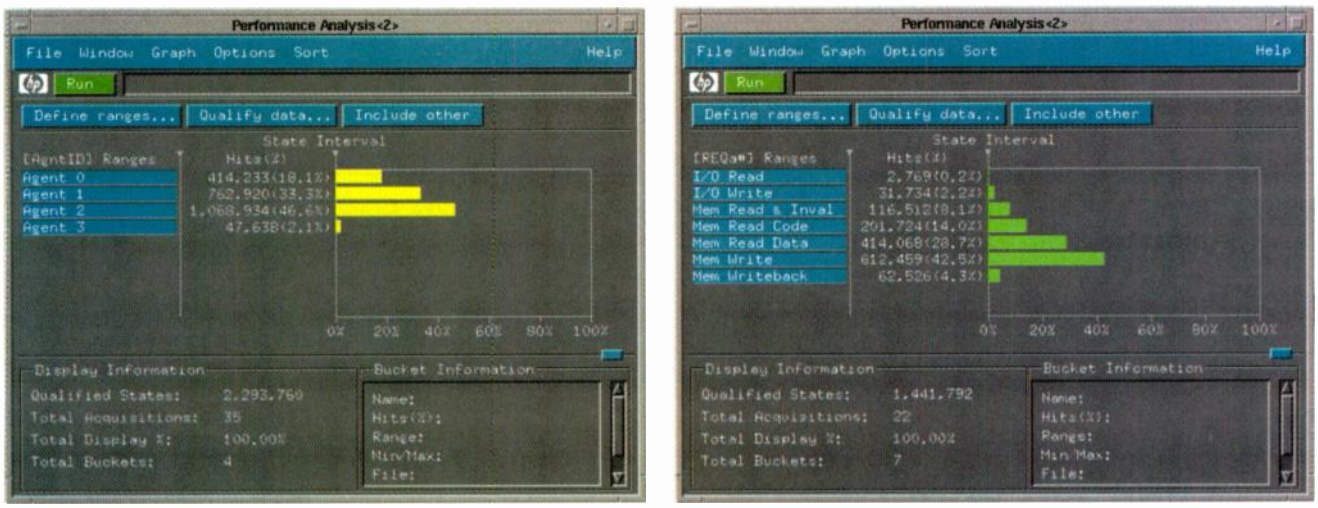
Load Balancing

How can I track load balancing for the different processors and quantify system performance? A useful set of measurements involves statistical data about the target SMP system. The information about how different processors are loaded, how much bus bandwidth is idle, or how a change to the system affects the system performance can be obtained through a logic analyzer and probe, in conjunction with system-performance-analysis software.

Statistical data can be gathered by capturing states that provide processor-identification and cycle-type information *(fig. 5)*. System performance analysis, specifically processor utilization distribution, can be used to observe distributions of bus events *(fig. 5a)*. It also can be used to quantify system-performance variation based on hardware changes. For example, it could show what happens when a replacement I/O device is accessed.

Figure 5b provides a similar view of the different transactions occurring on the system bus. This information can be used to identify performance and functional problems. For example, if 95% of the transactions are data writes, a software problem might exist—or at least software will need to be tweaked for performance. A hardware problem may be present if 95% of the cycles are retry transactions.

The measurements shown here were obtained by using the logic analyzer and



5. System performance analysis can be used to observe distributions of bus events. One view shows a processor utilization distribution (a). Bus events can also be observed with a transaction-type distribution (b).

SMART®
Modular Technologies

EMBEDDED COMPUTERS

MEMORY MODULES

FLASH MEMORY CARDS

COMMUNICATIONS PRODUCTS

R5000 3U CompactPCI

FREE TRIAL

SMARTengine™/50cPCI 3U

CPU	200-MHz 64-bit MIPS R5000 RISC processor
Bus	CompactPCI, 3U form factor
Memory	Up to 128 MB interleaved DRAM
NVRAM	8 or 32 KB
EPROM	256 KB
Flash	1, 2, or 4 MB of flash memory
I/O	Multi-protocol serial ports Parallel port 10BaseT Ethernet Supports 7 PCI slots in a CompactPCI back panel
RTOS	Supports multiple RTOS including VxWorks, Nucleus, and C-EXECUTIVE

The SMARTengine/50cPCI 3U brings the power of the R5000 CPU to telecommunications and data communications applications where space is at a premium. We can speed you to market with our off-the-shelf boards and provide a fast 60- to 120-day turnaround on prototypes tailored to a perfect fit for your application.

FREE evaluation

SMART offers qualified companies the opportunity to evaluate the SMARTengine/50cPCI 3U for a limited time at no cost.* This trial period also gives you a chance to try out our technical and applications support and see that SMART really is the perfect fit as your long-term technology partner. Contact SMART today to discuss your embedded computing needs.

Toll-free 1 800 956 SMART (1 800 956 7627)
Tel 510 490 0732 **Fax** 510 623 1434
World Wide Web www.smartm.com
E-mail info@smartm.com

* Some restrictions apply.

SMART

MODULAR TECHNOLOGIES, INC.

SMART Modular Technologies, Inc., is a leading manufacturer of specialty and standard memory modules, flash memory cards, communications products and embedded computers. SMART offers more than 500 products and is the supplier of choice for leading OEMs. Headquartered in Fremont, California, SMART has design centers in California and India; manufacturing plants in California, Puerto Rico, and Scotland; and sales offices throughout the world.

Silicon Valley Headquarters

Puerto Rico

Scotland

READER SERVICE 189

analysis probe to capture only the phase of each transaction where the cycle type, or processor ID was present.

In the first case, #bqual was generated by the logic analysis system to detect the Request B phase. Then, #bqual was used, so only processor identification information was gathered. The trigger system was set up to only capture states when #bqual was asserted. This represents the Request Phase B of the transaction, where the processor ID information was valid. (For discussions on Request Phase A, B, and other Pentium-Pro-specific data, refer to *Pentium Pro Processor System Architecture*, by Tom Shanley, Addison-Wesley Developers Press, ISBN: 0-201-47953-2.) Applying symbolic information to the appropriate combinations of these signals provided a higher level view of the information. Using a system-performance-analysis (SPA) tool with the captured data gives the result shown.

The second display in Figure 5 was obtained in a similar way. The trigger specification was altered to capture only the Request A phase of each transaction, instead of the Request B phase. The Request A phase provides enough cycle type information to obtain the second display. More statistical accuracy can be obtained by running these measurements repetitively and accumulating data with each run. Even greater accuracy can be reached by utilizing deep analyzer traces.

Tracking Data Corruption

How can I look at auxiliary (e.g., I/O, PCI, EISA, UMB) buses to track data-corruption problems? Monitoring auxiliary buses in an SMP system is critical to effectively debugging such problems as when the data is correct at one point in the system, but corrupted as it moves to another bus. Using a logic analyzer to observe data on one bus, and then on a subsequent bus, is a great way to track down these data corruption problems.

The PCI and system buses make good examples for this point. Suppose the data from an I/O write in your system ends up at the target I/O device incorrectly. The problem can be tracked by observing the transaction on the system bus and the PCI bus. Each bus is probed and connected to its own analyzer. Then, the measurement is time-correlated so that the resulting displays show the activity on both buses as intermingled.

A trigger on the system bus analyzer turns on the system bus I/O write. A similar trigger is set up on the analyzer connected to the PCI bus. Observing the acquisition should verify the problem and identify the trouble bit(s). An oscilloscope can be added to the problem signals and triggered by the Arm Out signal of the logic analyzer so that the analog characteristic of these data lines can be investigated.

Michael Patterson has been an R&D engineer in Hewlett-Packard's Logic Analyzer lab for two years. He has a BS in Computer Science from Iowa State University, Ames.

John Friedman has been an R&D engineer in Hewlett-Packard's Logic Analyzer lab for eight years. He has a BSEE from the University of Colorado at Boulder.

CODE Composer version 3.0

PERFORMANCE
= you and your equipment

Check out our new site

www.go-dsp.com

GO DSP
A Texas Instruments Company

High Performance DSP Tools

- IDE
- Leading Edge GUI
- Open Plug-In Architecture
- Visual Project Management
- C-Source & ASM Debugging
- File I/O
- Signal Probe Points
- Graphical Signal Analysis
- Multiprocessing
- Interactive Profiling

"Code Composer is probably the most sophisticated, comprehensive development environment... comparable to the best of any microprocessor development systems... There's presently nothing else I know of in the DSP marketplace that compares with it."

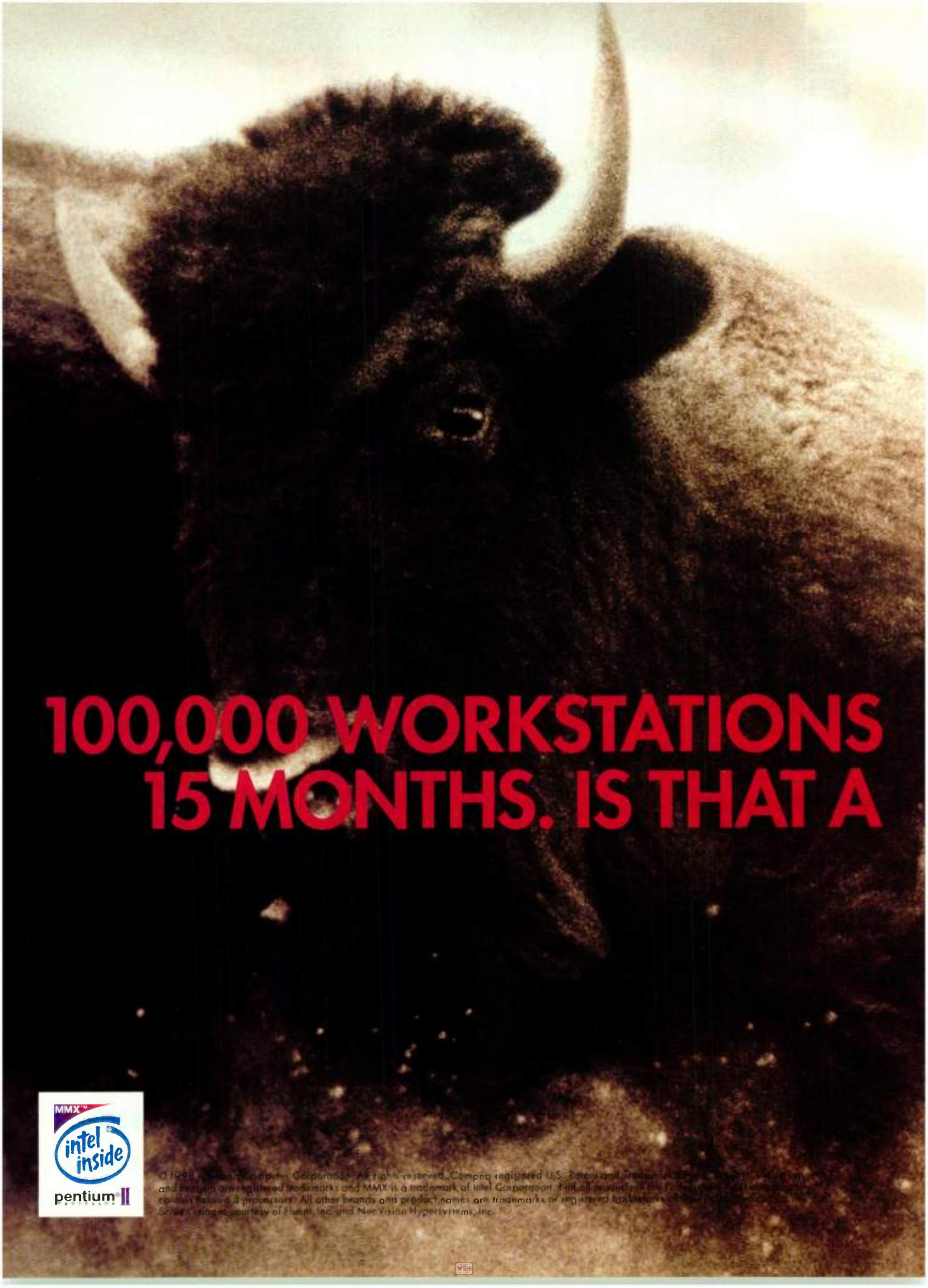
Desktop Engineering, May 1997

READER SERVICE 135

UNIX
Simulator
Emulator
3rd Party Board Support

TMS320 'C3x, 'C4x, 'C5x, 'C2xx, 'C54x and 'C6x
MS-Windows™ 3.11, 95 and NT

GO DSP Corporation
tel (+1) 416-599-6868 fax (+1) 416-599-7171

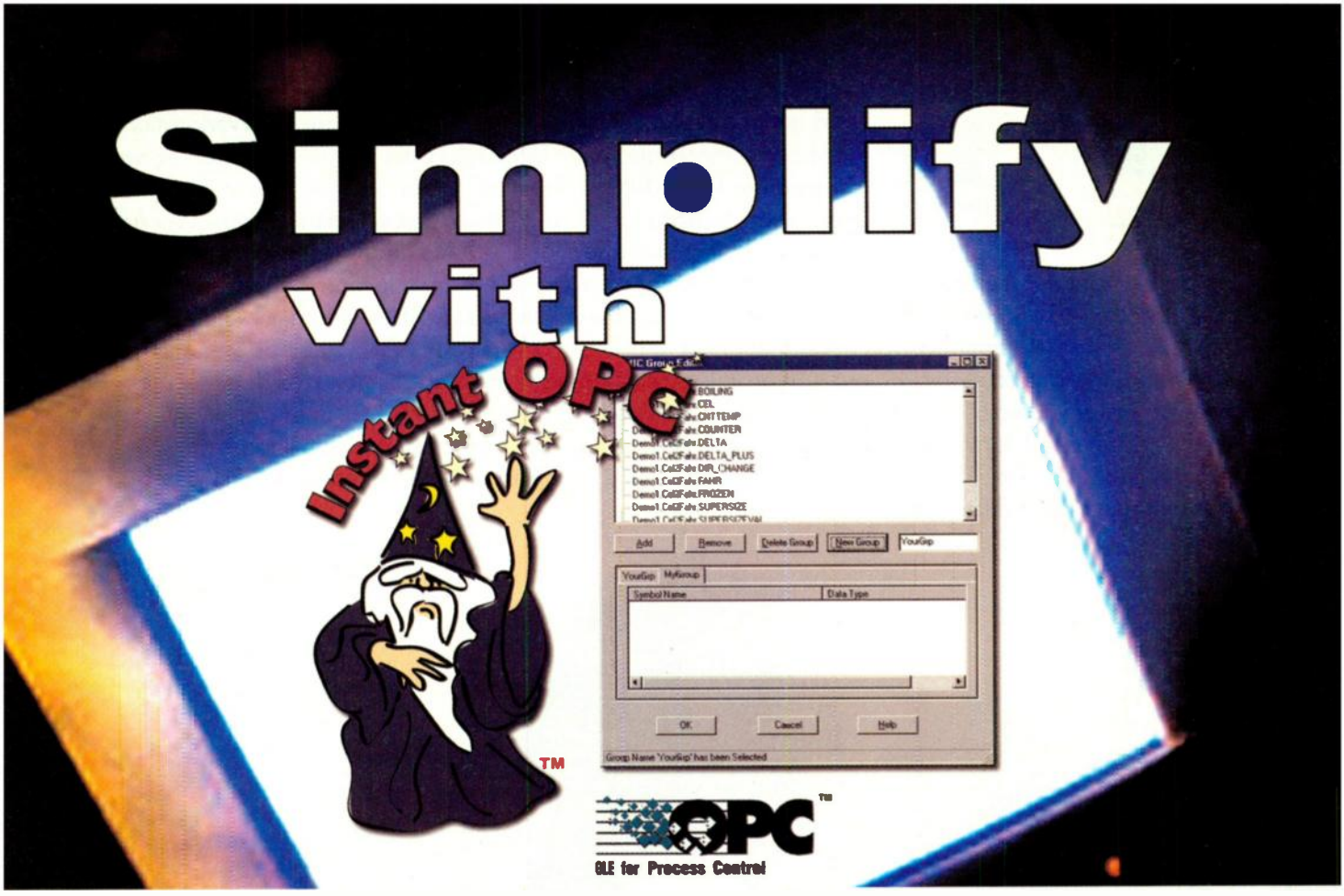

100,000 WORKSTATIONS
15 MONTHS. IS THAT A
MMX
intel inside
pentium II

Whatever you decide to call it, the shift from proprietary UNIX workstations to industry-standard Compaq Professional Workstations has been remarkable. Only 15 months after entering the market, we shipped our 100,000th workstation. A feat that took Silicon Graphics eight years to accomplish and Sun Microsystems six years. Our full range of Compaq Professional Workstations is optimized to run the most demanding business, technical and creative applications thanks to our innovative Highly Parallel System Architecture. This industry-standard architecture delivers 1.07GB/s of application memory bandwidth, giving performance you never thought possible from a Windows NT® system. So you can run your demanding applications without compromise. Leading-edge applications like Verilog-XL Turbo, Specctra, Allegro, Quad XTK and Board Station, plus all of your day-to-day business applications, eliminating the need for a second machine. All at a lower total cost of ownership than traditional UNIX workstations.* Would you expect less from the world's leading provider of computers? Visit us at www.compaq.com/products/workstations.

COMPAQ

SOLD IN THE FIRST TREND OR A STAMPEDE?

READER SERVICE 122



No OLE or OPC experience required!

VMIC's *Instant OPC* makes OPC easy to implement for client applications. Easy-to-use functions simplify the OPC interface by browsing the defined tag database, and reading and writing tag values. VMIC's *Instant OPC* product is a Dynamic Link Library (DDL) with supplied examples and test applications. *Instant OPC* works with Visual Basic®, C, and C++.

Benefits Include:

- No OLE or OPC experience required
- Compatible with any OPC server
- Automatically creates groups at run time
- Allows lower level C++ code
- Source code included for user customization
- Conforms to OPC Specification 1.1
- Easy to use: Fewer than six functions are needed to create a complete real-time data connection

Instant OPC is a part of VMIC's flexible family of PC-based control software called IOWorks®. Users running IOWorks on any standard PC under Windows NT® OS can combine device drivers, communication interfaces, monitoring and control products, and third-party application development tools into a completely integrated development and real-time execution environment.

IOWorks is compliant with IEC-1131-3 and key Microsoft® technologies such as OLE, OPC, ODBC, and DDE offering plug-and-play compatibility with most leading software products.

IOWorks is easily compatible with third-party hardware because it interfaces to open standard buses and operating systems.

Want to know more about IOWorks? Call today for a FREE interactive demo CD and evaluation copy !

Call Today. It's FREE!

800 322-3616

Winner of National Manufacturing Week's ***Best New Product Award***

VMIC
12090 S. Memorial Parkway
Huntsville, AL 35803-3308
205 880-0444 • FAX 205 882-0859
www.vmic.com • info@vmic.com

Gear Up For The Arrival Of Behavioral Design Methodology

System-Level Design And Growing Complexity Spur Another Look At Behavioral Abstraction And Synthesis.

Cheryl Ajluni

SPECIAL REPORT

With complexity skyrocketing and system-level design pushing to the forefront, the search for new methodologies to handle the accompanying issues shifts into high gear. Verification, shrinking design geometries, parasitic effects, timing, and interconnects all need solutions, and fast.

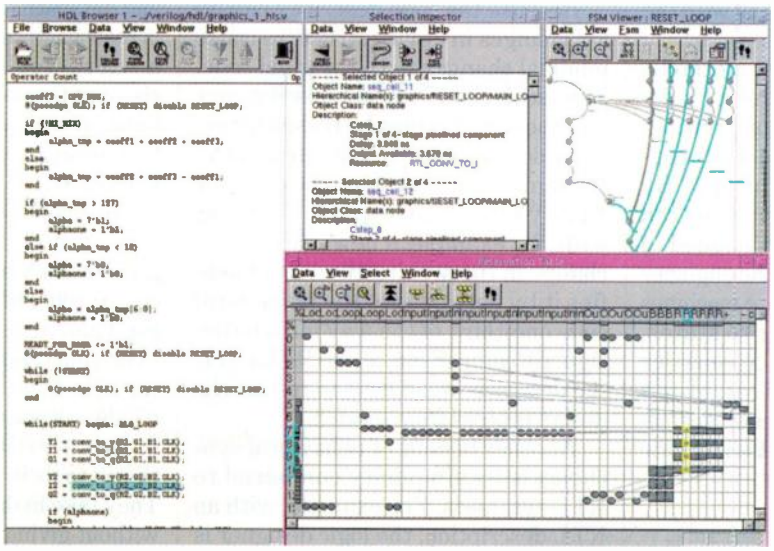
One answer is to boost the level of design abstraction. This way, decisions about system functionality and architecture can be made earlier on in the cycle, without damaging design costs or time-to-market. The behavioral level looks to be this next stage of abstraction. And, although behavioral synthesis isn't new, the idea of moving up a notch to that level is just starting to take hold.

Simply put, it is a means of modeling complex behaviors. Essentially, there are two ways to do bigger designs. The first way involves hierarchically partitioning the design into smaller design problems. Traditionally, this approach works quite well, but when it comes to systems on a chip, it runs out of steam.

The only way to deal with this limitation—and the second way to do a bigger design—is through abstraction. With this approach, you build up very simple abstractions; in effect, a conceptual partition, as opposed to a physical one. As a result, you now have a behavior that defines the details of a design specification that focuses on functionality. With the abstraction, you can not only achieve a "big-box" hierarchy, but you can break the box apart with pieces that can actually be built.

There are a few different languages that can be used for behavioral abstraction. High-level design languages (HDLs), for example, that include Verilog and VHDL are used for behavioral modeling. But, more often than not, the languages of choice for most designers are C or C++. The use of C models provides the added benefit of fast execution speed. This feature makes it a good choice for modeling critical functions such as DRAM and SRAM models, as well as developing test benches and firmware instance models.

As Paul Washkewicz, product marketing manager, HP EEsof, Westlake Village, Calif., explains, "If you look at a cellular telephone today, it would take too long to simulate because of its complexity using standard HDLs. Instead, C models are written to simulate the behavior of the telephone," he says. "At the behavioral level you can put a system together and validate it in a short amount of time. Architect gurus also make use of this technique for partitioning designs," says Washkewicz.



Art Courtesy: Synopsys

Today, many designers use C to model small pieces of a design that can't be validated reasonably using current techniques. The mixed behavior part of the design gives the designer increased productivity, and the register-transfer level (RTL) lets the designer work faster and with a lot less die area. While some hope that designers will eventually move the whole process into the behavioral level, it's more likely that this mixed behavior/RTL way of designing will continue until the behavioral limitations are overcome or silicon is so efficient, fast, and cheap that the limitations simply won't matter anymore.

System-level and RT level designers use behavioral for very different reasons. If you're a system-level designer, you look for a path to implementation, and use behavioral synthesis to get you there. If, on the other hand, you work at the RT level, using behavioral to raise the level of abstraction will allow you to do more complex designs.

Utilizing behavioral, regardless of the reason, causes the introduction of an intermediate step into

TECH INSIGHTS BEHAVIORAL-LEVEL ABSTRACTION

Why, then, would a designer migrate to a higher level of abstraction if the risk of incurring design errors increases. Many designers simply don't have a choice. They're forced to go to a higher level of abstraction due to complexity. It's the only way to be able to handle bigger chunks of logic. According to Walker, "to deal with the increased potential for errors, designers will need to combine the behavioral level with the physical or back-end of the design driving the design process."

Going Mainstream

Limitations aside, one of the largest obstacles facing the industry, ironically, is the widespread acceptance of the need for behavioral-based tools. The problem is that the use of such tools requires a major change in design methodology. In fact, many believe this change will be similar in magnitude to the change required for the industry to migrate from a bottom-up to a top-down design methodology.

In particular, designers will need to come to terms with what it means to do systems design. Once this hurdle is passed, they will, as Synopsys, Mountain View, Calif., believes, begin the migration by starting to adopt high-level synthesis. One of the primary ways the industry hopes to make this transition easier is through education at the systems-design level.

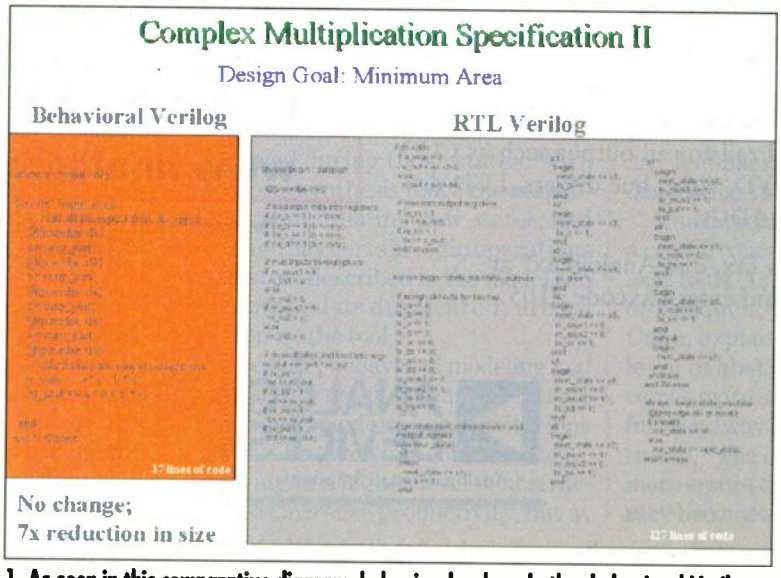
Designers need to think differently about the design problem. They have to begin to think of design in terms of the big picture, and they will need to learn a new coding style. To that end, a host of resources that include literature on behavioral synthesis, seminars, web site information, consulting services, and in-depth customer training, are some of the avenues being offered by current EDA tool vendors with behavioral-based tool offerings. Many believe that this type of methodology shift will be taught at the academic level, ensuring that graduates entering the work force are equipped with the knowledge they need to succeed in today's high-paced design environments.

Then, there's the development of a behavioral-specific language, and subsequent tools based on this language. Additionally, there is some movement toward behavioral Verilog that would consist of extensions to add more commands to the existing Verilog HDL.

An interesting question in the discussion of a behavioral language, as Prem Jain, founder and president, CAE Plus, Austin, Texas, points out is, "whether to start from C or HDL." As he explains, "There is more software in C today, than in HDL. System IC development needs desperately the behavioral languages for verification requiring higher speed of simulation, communication among hardware designers, and communication among embedded software and hardware designers." Jain continues, "The problem is that concurrent behavior present in many systems designs is difficult to deal with and requires graphics to communicate. Architects can, for example, draw pipelines graphically, while HDL developers use timing diagrams after simulation to debug concurrency. Sequential behavior is quite large and is best described textually." Jain contends that the solution is to use C for extension and graphics to capture structure and timing. The graphics can then be translated into C for high-speed simulation.

Even if the EDA industry decides to adopt a behavioral-specific language, it may still be a few years off. In the meantime, designers may continue to use C. Once the behavioral language is established, Verilog and VHDL HDLs won't necessarily be eliminated. On the contrary, because the behavioral language will still need to be verified against implementation, HDLs will remain an interface between behavioral and VHDL/Verilog languages.

Widespread acceptance of behavioral tools also means an expansion of their capabilities for use in a wide range of designs. As Bob Beachler, director development tools marketing, Altera, San Jose, Calif., points out, "While behavioral synthesis is good for ASICs, ICs, and FPGAs, it is not yet good enough for programmable logic. Because programmable logic is already under a performance handicap, the area/performance limitations of behavioral tools hurts them even more than FPGAs." He continues, "For behavioral technology to be mainstream for programmable logic, behavioral compilers must be able to comprehend the differences between gate-array and programmable-logic architectures. Different algorithms are needed to capture the nuances of the architecture and minimize the performance/area hardships. Companies like Synopsys, Synplicity, and Exemplar have developed algorithms for programmable logic, but they need to tailor the output of the RTL that puts out behavioral synthesis results so that it can be used by a programmable-logic synthesizer." What's needed is an RTL description tailored to RTL coding that programmable-logic synthesizers can use.



1. As seen in this comparative diagram, behavioral code, whether behavioral Verilog or C, is much more compact than the more traditional RTL Verilog version.

Today's Solutions

One company that's sitting right in the middle of all the flurry is Synopsys, Mountain View, Calif. With its Behavioral Compiler tool already on the market, the company has pushed very hard to bring behavioral tools to the EDA mainstream. Targeted at market segments such as network

Imagine Being Able To Look At A Digital Design Problem This Way.

This view of system behavior was provided by the HP 16700C logic analysis system and the HP 10505A prototype analyzer.

Multiple measurement windows display various domains—all time-correlated—on your large screen display. You can also view the same domain's data simultaneously in different modes.

Well you can, using a simple technique Hewlett-Packard calls cross-domain analysis. It allows you to view time-correlated measurements at multiple points in your system—from signals to source—all on the same display. So you can quickly pinpoint the root cause of a problem, and speed up the entire prototype integration process.

Only HP's family of digital design tools can give you this kind of insight. And we secure your digital design tools investment with upgrade packages, trade-in programs, scalable, modular instruments, and forward-compatible measurement modules.

For more information, call HP DIRECT for the new Digital Design and Debug Tools Catalog at **1-800-452-4844, Ext. 5378.** Or visit www.hp.com/go/info/imagine

HEWLETT® PACKARD

READER SERVICE 198

applications, graphics, multimedia, digital communications, and signal/ image processing, the tool works well in data-flow-intensive applications. It gives designers a path from behavioral to gates, and in effect, something that is synthesizeable. The Behavioral Compiler tool gives the designer a view to logic synthesis so he or she could build a gate-level design. Ultimately, this ensures that the designer is building an architecture that can be implemented. As a result, there's a high level of predictability.

Despite the capabilities of the tool, Synopsys faced resistance to its adoption. Users did not understand what the tool actually does and why. To combat this problem, the company came out with a tool known as Behavioral Compiler (BC) View. As a GUI to the Behavioral Compiler tool, it shows the user what's going on inside. It also allows cross-correlation between various functions. With BC View, designers can debug a design and gain access to previously unaccessible detail. It takes the mystery away from the tool, allowing the user to tweak it for design improvements.

Synopsys does not believe that everything will move to the behavioral level at the present. There will be a common synthesis engine, but it will support mixed This method is good for those working with IP or just blocks. It is what the company considers to be the intermediary step to full adoption. And, while that doesn't mean that old RTLs will go away, it does mean that designers can spend their time figuring out what to design, and not how to design it.

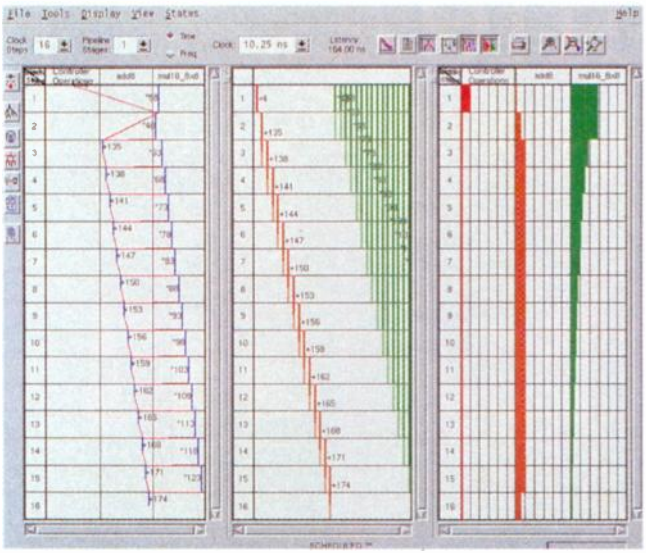
Cadence's Alta Group, Sunnyvale, Calif., works in the system-level design area and specifically focuses on the consumer electronics industry to address system-level chips. Cadence believes the industry needs to move more of the verification tasks to higher levels of abstraction, and provide technologies that allow for smarter verification.

Cadence offers a system-in approach for verification that comprises full modeling of systems and operating environments with Alta tools. Additionally, they extract a realistic chip test bench from the system model through the industry-standard Open-Modeling Interface (OMI).

Key to this solution is Alta's Visual Architect behavioral synthesis tool, which converts system-level behavioral HDL to RTL HDL for synthesis and datapath tools *(Fig. 2)*. For the system designer who wants tools that allow behavioral language to flow to behavioral synthesis, there's the HDS-Behavioral HDL algorithm design-capture tool. The results of that tool can flow directly into the Visual Architect tool. This setup effectively enables more intuitive graphical design entry into behavioral synthesis for system-level functional blocks.

Cadence also has extended behavioral technology to its EnWave solution, such that it is now applicable for designing digital communications systems on a chip. The solution includes a comprehensive library of executable and synthesizeable building blocks for conceptual exploration at the fixed-point level, and automatic generation of behavioral HDL for an accelerated path from concept to implementation. As a result, it expedites the path to digital hardware by enabling systems designers to create virtual prototypes, optimize performance, and conform to standards for digital communications devices.

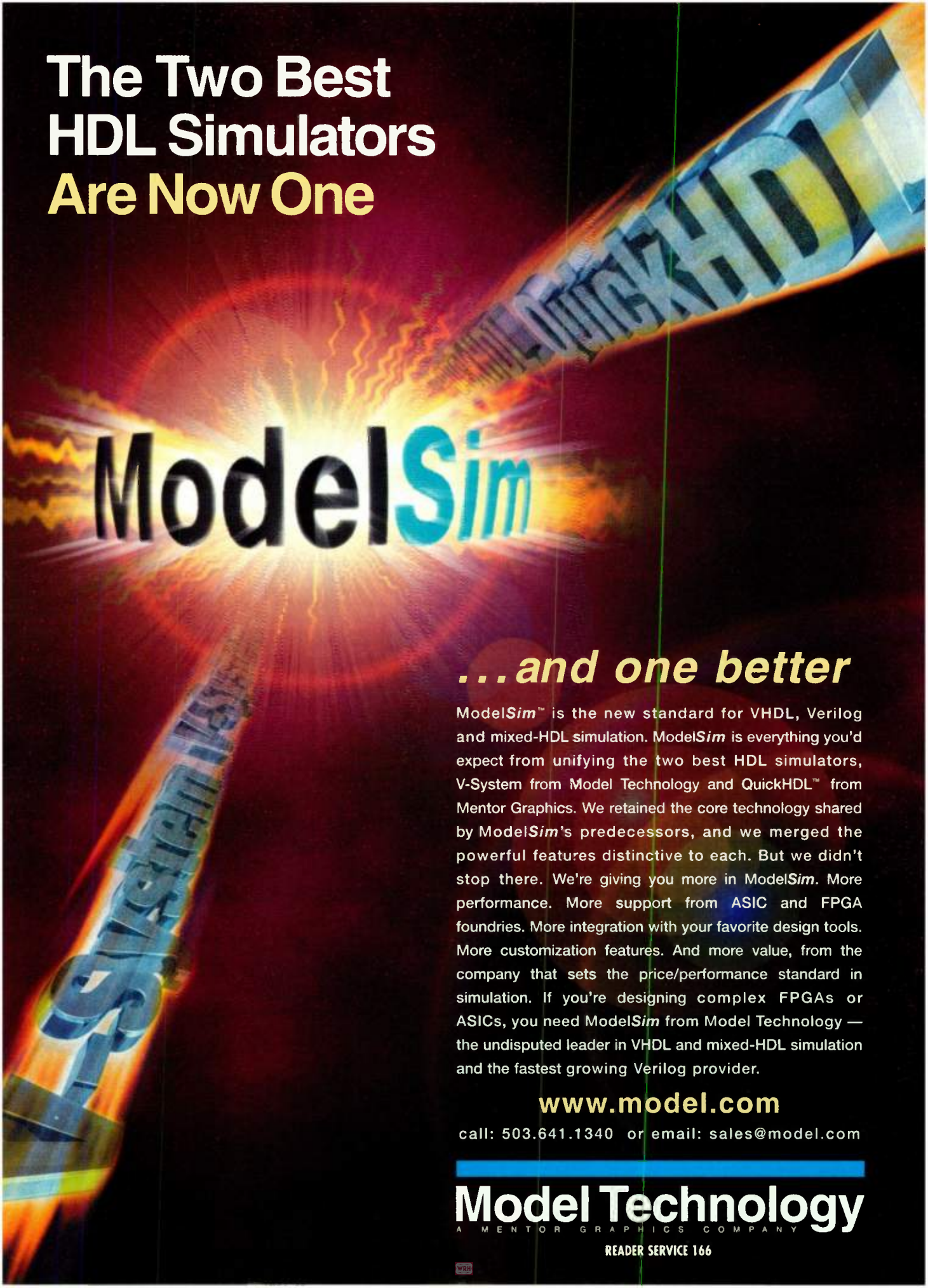
HP EEsof has taken a very similar approach to Cadence's. It has chosen to focus on DSP designs as a way of narrowing the scope of the behavioral problem. As the concept of raising the level of abstraction gains more industry acceptance, the company will be able to take its success and expertise in the behavioral DSP market and expand to other application areas of design. As Washkewicz explains, "The end goal is the same. We all want to see behavioral technology utilized in more of the design process, but the approaches used to get to this point are different." HP EEsof's offering, DSP Synthesis, behaviorally synthesizes schematics. Because the company has the advantage of being the user as well as the developer, it has taken the opportunity to optimize the tool's performance.



2. Visual Architect's full-color graphs make it easy to interpret critical design data at a glance. The interactive visual data format helps users explore ASIC architectural design alternatives and make intelligent trade-offs that directly affect area and speed.

Precedence, Campbell, Calif., also offers a behavioral-level capability with its high-level procedural modeling interface, Precedence C Model Client (PCMC). PCMC is utilized by Precedence's SimMatrix electrical simulator backplane. Specifically designed to address the use of one or more C-language models in hardware/software and system-on-a-chip designs, it permits C-language models to control commercial simulators or the design-verification session. PCMC allows the designer to drive a simulator with a C model, and provides an interface to both proprietary or commercially available simulators. It also enables multiple C models to be instantiated in one design. The PCMC interface comes free of charge with the purchase of SimMatrix 1.7.

The idea of behavioral-related technology stems from the fact that the design and verification problem has too many dimensions. Although some behavioral technology is already available, it mainly addresses communications and multimedia applications. It is not a technology that answers all of today's EDA challenges, nor will it be in the future. But, over time the technology will improve and it will inevitably gain wider acceptance. Until then, behavioral-based tools will need to continue to try to prove themselves in a large number of designs. And, EDA tool vendors will need to continue refining the tools' capabilities to make them as easy-to-use as possible.


The Two Best
HDL Simulators
Are Now One
QuickHDL
ModelSim
...and one better
ModelSim™ is the new standard for VHDL, Verilog and mixed-HDL simulation. ModelSim is everything you'd expect from unifying the two best HDL simulators, V-System from Model Technology and QuickHDL™ from Mentor Graphics. We retained the core technology shared by ModelSim's predecessors, and we merged the powerful features distinctive to each. But we didn't stop there. We're giving you more in ModelSim. More performance. More support from ASIC and FPGA foundries. More integration with your favorite design tools. More customization features. And more value, from the company that sets the price/performance standard in simulation. If you're designing complex FPGAs or ASICs, you need ModelSim from Model Technology — the undisputed leader in VHDL and mixed-HDL simulation and the fastest growing Verilog provider.
www.model.com
call: 503.641.1340 or email: sales@model.com
Model Technology
A MENTOR GRAPHICS COMPANY
READER SERVICE 166

UPDATE ON SiGe ICs

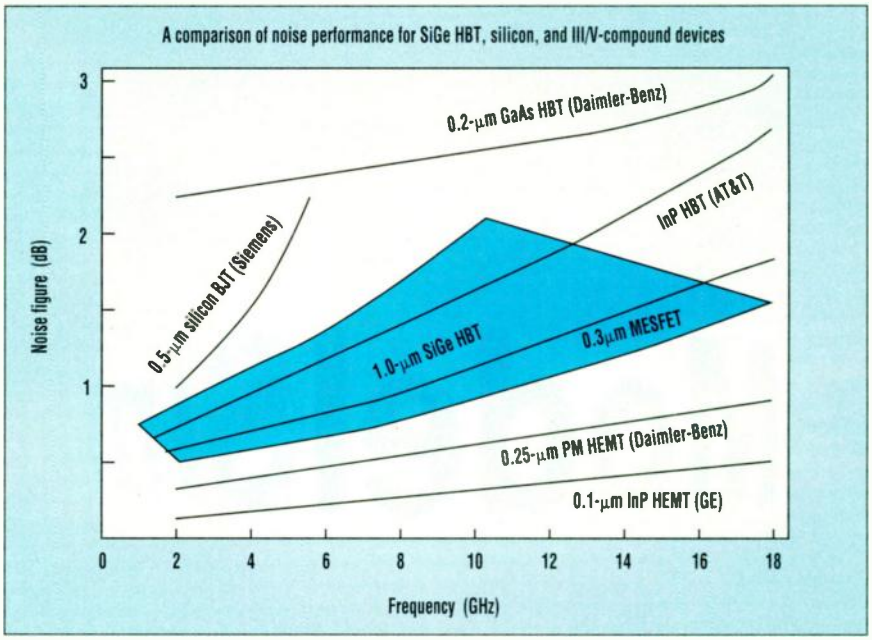
Temic Semiconductors Begins Mass Production Of Silicon Germanium Chips

While most solid-state scientists were still discussing silicon germanium (SiGe) semiconductors as a major topic at ESSDERC '97, Telefunken Mikroelectronic GmbH (Temic), Heilbronn, Germany, is now ramping up mass production of SiGe chips, the first semiconductor manufacturer to do so. Even though these ICs have the about same electrical features as gallium-arsenide (GaAs) chips, they can be manufactured at about one-fourth the cost. They also can be produced in a more environmentally friendly way than GaAs devices, whose entire production process is paved with highly toxic substances.

According to Dr. Frank Heinricht, chairman of the Integrated Circuits Div. at Temic, the company intends to become the leader in high-frequency ICs by applying its SiGe knowledge. Temic is currently increasing its production of SiGe ICs for mobile communications applications. These chips offer the same, and sometimes better, performance as GaAs ICs in the range of 1 to 5 GHz, but at significantly lower cost. To manufacture the ICs, Temic uses a heterojunction-bipolar-transistor (HBT) structure *(Fig. 1)*.

Temic's engineers developed two different types of HBTs: those optimized for speed, and others optimized for power. Optimization is achieved by the use of selective ion implantation.

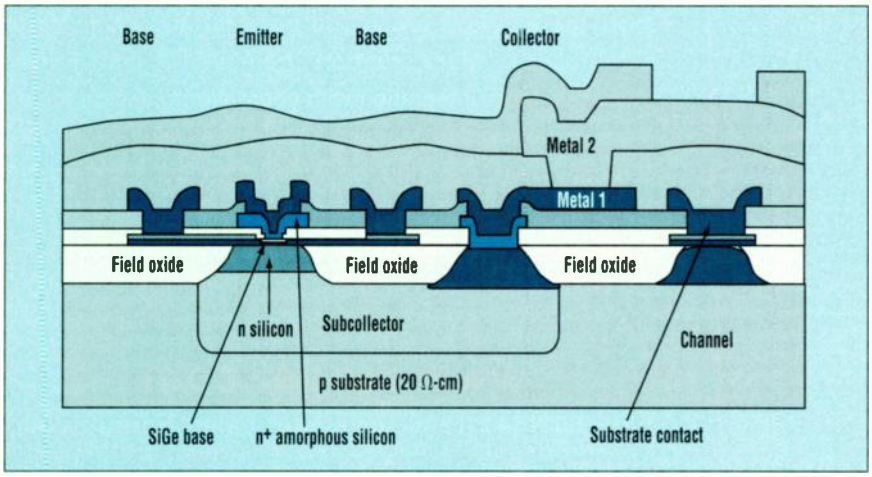
SiGe power transistors offer a high breakdown of 6 V, but a relatively low transit frequency of 30 GHz. However, a frequency of 30 GHz is an excellent value, considering that one of the best silicon RF processes available, the B6HF process from Siemens Semiconductors, offers a transit (-3-dB) frequency of 25 GHz. SiGe transistors optimized for speed offer a transit frequency of 50 GHz at a breakdown of 3.5 V. In the lab, Temic's scientists have even achieved transit frequencies of 116 GHz, however, such frequencies were only for experimental devices, and not for production purposes.



2. Noise performance for SiGe HBTs is superior to that of ICs made of silicon and III/V compounds.

The company points out that their SiGe devices set other performance milestones as well. For example, noise performance (1/f) is better than with GaAs ICs *(Fig. 2)* Current amplification is typically 150, while base resistance is specified at 140 Ω. The power-delay product is typically below 1 fJ. Furthermore, SiGe allows the use of cheaper packages because its thermal conductivity is higher than that of GaAs. Additionally, unlike GaAs ICs, SiGe components do not require a negative bias voltage.

Temic uses a relatively high percentage of germanium with the relationship between silicon and germanium being 80:20. By comparison, other manufacturers of SiGe devices use a triangular germanium profile with only 15% germanium. Temic's HBTs work with a base which is doped higher than the emitter, more than $4 \leftrightarrow 10^{19}/cm^3$ while the emitter is doped with just $2 \leftrightarrow 10^{18}/cm^3$. As a result, even with a very thin base of less than 20 nm, base resistance remains acceptable for transit frequencies of 80 GHz.



1. This figure shows a cross section of a silicon-germanium (SiGe) heterojunction-bipolar-transistor (HBT) structure used by Temic Semiconductor. The process on which this device is made is optimized for both speed and power performance.

The company has achieved transit frequencies of more than 50 GHz, with emitter widths of 0.8 µm. As a result, RF power applications benefit because the current for every emitter finger may be more than doubled compared to the other approaches.

A special feature of Temic's SiGe technology is the fact that two different collector variants can be manufactured simultaneously on the same chip. This leads to the aforementioned different combinations of breakthrough voltages and transit frequencies of 50 GHz at 6 V.

Even RF noise performance in the new SiGe process is almost as good as with III/V semiconductors in the frequency range up to 5 GHz. Over 0.9 to 2.4 GHz, SiGe low-noise amplifiers offer a noise of less than 2 dB, with power amplifications of more than 20 dB.

Temic is using 6-in. wafers and about 19 mask steps to make production-lot SiGe ICs. As Heinricht says, although this capability is not new, it represents a significant improvement in Temic's existing RF bipolar UHF5S process.

To make the devices, Temic uses a technique developed by Damler-Benz AG's Research Labs, Stuttgart, Germany, where thin SiGe layers are grown on a silicon substrate. Temic applies a reduced-pressure chemical-vapor-deposition (CVD) process, a step also used for silicon epitaxy. Using an existing technology combined with proven process steps "eliminates the risk connected with introduction of a new technology," Heinricht says. "Our new SiGe is about 95% identical to our proven and qualified bipolar RF technology," he adds.

According to Heinricht, several manufacturers of mobile telephones have decided to use the SiGe ICs. Temic sees these ICs as particularly useful for dual- or triple-band GSM mobile telephones, working with frequencies of 900, 1800, and/or 1900 MHz, which are set to enter the mass market in about a year. And, because SiGe technology also can be used to make passive components such as resistors, capacitors, and inductors, it's capable of making entire high-frequency RF ICs for mobile communications—a market which Temic sees as soon starting to explode.

Contact Frank Bracke, Temic Semiconductors, P.O. Box 3535, 74025 Heilbronn, Germany; +49 7131 67 2945; fax +49 7131 99 33 42; e-mail: frank.brack@temic.de.

Alfred Vollmer

PRODUCT FEATURE

Algorithms, Accelerator Combine To Form Powerful Audio Subsystem

By merging a host of DSP algorithms with a high-end audio processor, designers at Analog Devices and EuPhonics have created a cost-effective 64-voice polyphony wavetable synthesizer for Windows applications. The EuSynth/Wave64 with Dynamic Interprocessor Voice Allocation (DIVA) developed by Euphonics runs on the Analog Devices' SoundMax 64 accelerator.

The DIVA technology is a dynamically scalable 64-voice wavetable synthesizer that supports Microsoft's DirectMusic API. It accelerates the first 32 voices, placing the primary burden on the SoundMax 64. Spillover voices (above the first 32) are directed to the host processor.

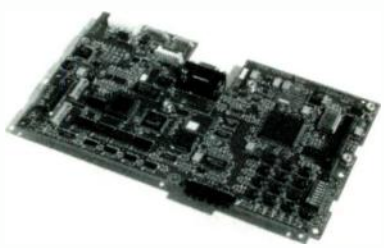
The SoundMax 64, which can handle most sound-related applications, suits both desktop and notebook applications due to its small footprint. The 128-lead device is housed in a PQFP, and measures 14 by 20 mm. The chip offers a 90-dB system signal-to-noise ratio for digital audio playback and mixing, as well as independent recording and playback sample rates. A PCI bus master with a 72-stream scatter-gather direct-memory-access engine accelerates DirectMusic and other various effects.

Analog Devices Inc.
Ray Stata Technology Center
804 Woburn St.
Wilmington, MA 01887
(781) 937-1428
www.analog.com.
CIRCLE 500
RICHARD NASS

Intelligent Controller Supports Analog Active-Matrix LCDs

The InSynctive intelligent controller supports NEC's family of analog active-matrix liquid-crystal displays (LCDs), including the latest 20.1-in. panel. Resolutions range from 640 by 480 to 1280 by 1024 pixels. Among the applications that make a nice fit with the board-panel combination are engineering workstations, medical and video imaging, and federal systems.

With its 32-bit processor design, the controller automatically determines the correct screen resolution and sizing for the target display, and allows for fine tuning of the signal



sampling point to eliminate ghosting, banding, and other artifacts that often plague analog liquid-crystal displays. The controller is built with a Personality Module Interface that lets OEMs customize a display for their particular needs.

The InSynctive controller accepts a VGA-type analog video input in various screen formats, produces a synchronous pixel clock, and outputs the analog signal with the appropriate screen formatting. When the video signal ceases, the board powers down the entire display and shuts off the backlight to ensure a smooth system shutdown.

Available immediately, the InSynctive intelligent controller sells for $415 in large quantities.

Opus Systems
10050 Bubb Rd.
Cupertino, CA 94014
(408) 342-1060
www.opus.com
CIRCLE 501
RICHARD NASS

Sparc-Based Workstations Boast "Personal Computer Prices"

A series of Sparc-based workstations claim performance that's above and beyond what's offered in a PC-NT equivalent, but with better or equal pricing. The three boxes all run the gamut of Solaris applications, currently around 12,000. At the low end is the Darwin Ultra 5 workstation, which is built with a 270-MHz UltraSparc IIi processor. It can hold up to 512 Mbytes of RAM, has integrated 10- or 100-Mbit Ethernet functionality, and three PCI slots. Pricing starts at less than $5000. Suitable applications for the Darwin 5 include software development, EDA, and digital-content creation.

The mid-range system in the family is the Darwin 10, which is designed with a 300-MHz UltraSparc IIi processor. Its spec sheet boasts up to 1 Gbyte of RAM, 8 Gbytes of hard-disk space, 4 PCI slots, integrated 10- or 100-Mbit Ethernet functionality, and a price tag below $10,000. Typical applications for the Darwin 10 include MCAD and simulation. Benchmarks for this platform are 11.7 SPECint95 and 12.8 SPECfp95.

Lastly, at the high end is the Ultra 60, which starts at less than $20,000. It can hold one or two 296-MHz UltraSparc II processors. It features 2 Gbytes of RAM, 2 Mbytes of cache, and up to 18 Gbytes of internal storage. Its two PCI buses can hold four cards, three at 33 MHz and one at 66 MHz. Dual UPA graphics slots are available, each running at 120 MHz. Applications for the Ultra 60 workstation include EDA, imaging, animation, modeling, and digital-video content creation. In addition, the platform runs all Windows applications and performs transparent file sharing between PC and Solaris environments.

Sun Microsystems Inc.
2550 Garcia Ave.
Mountain View, CA 94043
(415) 960-1300
www.sun.com.
CIRCLE 502
RICHARD NASS

Many are sold on our data acquisition system after seeing only one piece of data.

Whether you need a data logger or an automated test solution, the HP 34970A offers you uncompromised functionality and performance. And the features you need to get the job done. Like built-in HP-IB and RS-232 interfaces. A standard three-year warranty. And a price tag that fits within your budget.

PERFORMANCE

- 6 ½ digits resolution (22 bits)
- Built-in signal conditioning measures thermocouples, RTDs, & Thermistors; ac/dc Volts & Current; Resistance; Frequency & Period
- Scanning up to 250 channels per second
- Non-volatile 50,000 reading storage with timestamp

THREE-SLOT FLEXIBILITY

- Multiplexing and Actuation
- Digital I/O, Analog output, Event counting
- RF switching up to 2 GHz
- 4 x 8 Matrix switching

WINDOWS® SOFTWARE

- HP BenchLink Data Logger application included
- HP VEE and LabVIEW® drivers available

"I'll tell you more about how the HP 34970A can meet all your data acquisition needs—for an unbelievably low price. Just give me a call at ***HP DIRECT, 1-800-452-4844;** Ext. 5286.***"

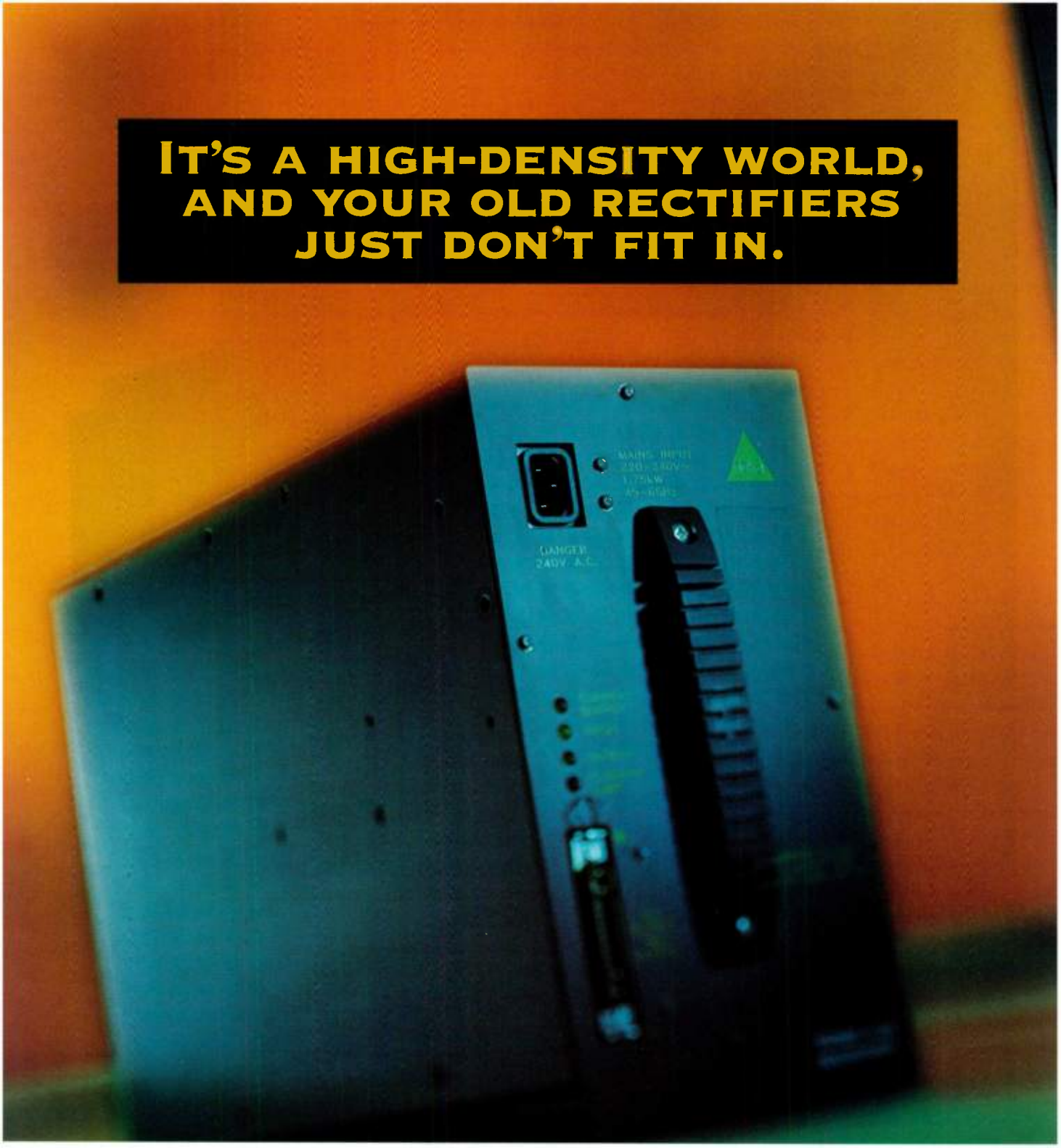
Check out our on-line HP Basic Instruments (BI) Catalog at http://www.hp.com/info/bidaq1
Faxback: 1-800-800-5281, Document 12254.

HEWLETT PACKARD

**U.S. list price*
***In Canada, call 1-800-387-3154, program number TMA125.*

READER SERVICE 150

IT'S A HIGH-DENSITY WORLD, AND YOUR OLD RECTIFIERS JUST DON'T FIT IN.



It seems that everything about telecommunications is growing—including the power that systems require and, unfortunately, the space they take up.

Lambda addresses the problem with a series of modular power front ends that occupy up to 35% less space than their nearest competitors. The FE Series modules provide a solution that's scalable in 500, 1000, 2000 and 3000 watt units, and fits in a standard 3U rack shelf with optional Low Voltage Disconnect, battery temperature compensation and circuit breakers.

The modules are hot-swappable, and feature power

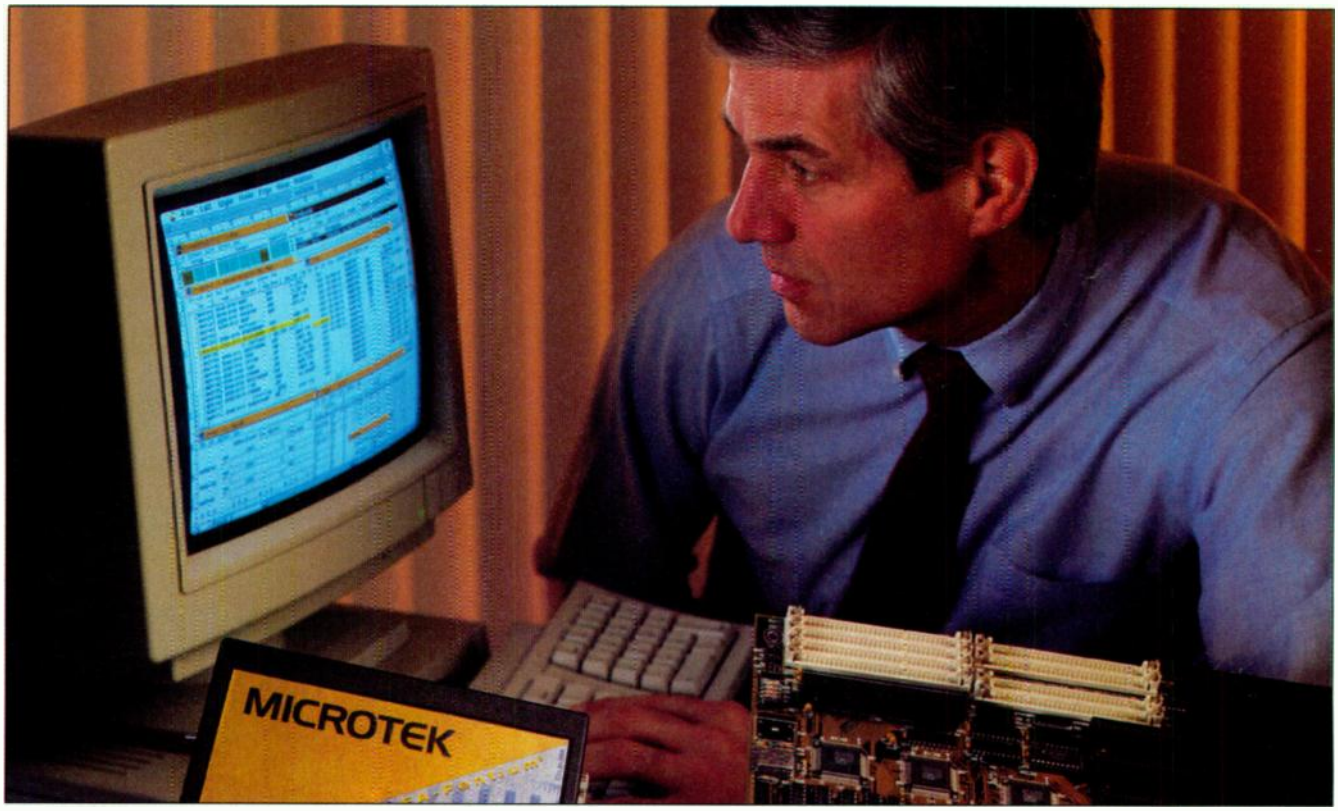
factor correction and remote diagnostics. Both 24 and 48 volt output versions are available.

There are plenty of other reasons why the FE Series may be the right solution for your application. But you'll just have to give us a call at 1-800-LAMBDA-4, ext. 8828, because, once again, space is limited.

LAMBDA

www.lambdapower.com/fe

READER SERVICE 177

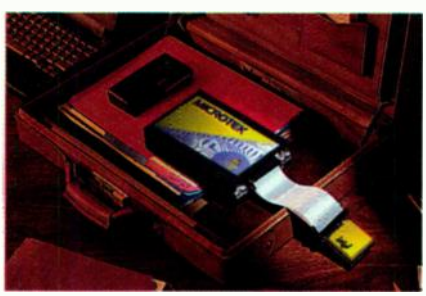


"If I could find it, I could fix it."

SEE your code at work. Find timing conflicts fast that are invisible with logic analyzers and software debuggers.

Microtek In-Circuit Emulators combine a state-of-the-art source level debugger with the most advanced event trigger and trace system available.

160-bits Wide by 256k Trace with Clock-edge Resolution.
With this much trace and smart triggering, you can record virtually every event. And events can be followed right back to their source code without stopping the target.



Smaller is Better.
Compare today's Microtek In-Circuit Emulators that fit in your briefcase, with the traditional "chassis" of just two years ago. The difference is remarkable! The PowerPack®EA for the Pentium® processor is only 7.2" x 4.6". And the probe tip is smaller than your business card, so it fits into the tightest targets.

Call for FREE ICE Tips AppNotes:

1 (800) 886-7333

www.microtekintl.com
Phone: (503) 645-7333
Fax: (503) 629-8460

SWAT™ Software Analysis Tool

- Fast, easy code validation for design engineers.
- Built into Microtek In-Circuit Emulators.
- Code Coverage and Performance Analysis offer you design spontaneity without instrumenting your code!

CODE CHANGES

MICROTEK
IN-CIRCUIT EMULATORS

NEW PRODUCTS
Three Emulators for Pentium® Processors
SWAT™ Software Analysis Tool
Two National NS486™ Emulators
High-Performance 80C186 Emulator

Microtek In-Circuit Emulators for the following processors:

Pentium®• Intel486™• National NS486™• Intel386™EX • 386DX • 386CX/SX • 80C186 • 8051
68360 • 68340 • 68F333 • 68332 • 68331 • 68330 • 68HC16 • 68328 • ColdFire

READER SERVICE 165

ELECTRONIC DESIGN QUICKLOOK

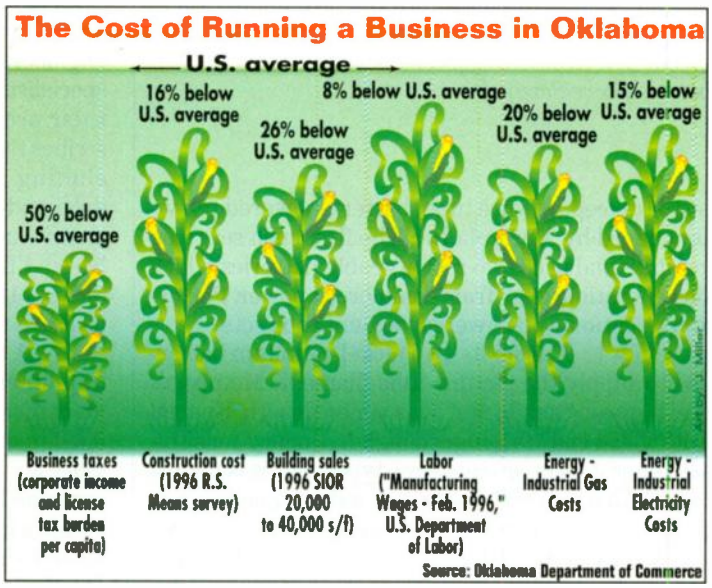
Edited by Debra Schiff

MARKET FACTS

Where The Corn Is As High As An Elephant's Eye

OK, so every time someone says Oklahoma, you think of the song from the famous musical of the same name. Well, it's time we redefined that state for you. According to numbers provided by the Oklahoma Department of Commerce, if a company is looking to expand or relocate, it should definitely consider Oklahoma. The College of Business at Arizona State University, Phoenix, released the Blue Chip Job Growth Update late in 1997, announcing that United States' total nonagricultural job growth from Sept. 1996 to Sept. 1997 adds up to 2,750,000 jobs. That number represents a 2.28% change. In the same time period, Oklahoma saw a 2.79% change, and a job growth of 38.1 thousand jobs in the nonagricultural market. According to the study, Oklahoma is ranked ninth in total nonagricultural job growth. Nevada ranked first. Wyoming was ranked 50th. As far as manufacturing job growth is concerned, Oklahoma ranked eighth. The state saw job growth in this sector as a 4.4-thousand job increase. Washington state ranked first in manufacturing growth, while Hawaii took 50th place. The U.S. saw a job growth increase of 18,661,000 jobs in manufacturing during that time period. In the service industries, Oklahoma placed seventh, with a 4.68% change from Sept. 1996 to Sept. 1997. Service-job growth in Oklahoma totaled 17.4 thousand jobs during that time. The U.S., comparatively, counted 1,216,000 new jobs in the service sector. Utah ranked first, while Wyoming ranked 50th in service job growth. According to the Oklahoma Department of Commerce, average industrial electric bills are far less costly in Oklahoma than in some major cities, and much lower than the U.S. average. Chicago's energy costs are $476,542, in comparison to Oklahoma City's tab of $242,813. You don't want to even look at Akron's fee of $526,744. Dallas spends $352,209 on it's average industrial electric bill, which is a bit lower than the U.S. average bill of $405,000. Major electronics companies with offices in Oklahoma include Lucent Technologies, The VAC Corporation/Siemens, and Seagate in Oklahoma City; Rockwell International and Lawrence Electronics in Tulsa; and Hitachi in Norman. Suppliers and purchasers who've moved facilities to Oklahoma include Phillips Petroleum, TDK Ferrites Corp., Allied Signal, American Foundry Group, and Mobile Chemical Company. And, the Business and Industry Training Services Division of the Oklahoma Department of Vocational-Technical Education offers free customized industrial training. Then, there's the Oklahoma Quality Jobs Program and the Small Employer Quality Jobs Program, recently installed this year. Basically the programs provide annual cash-back payments of 5% of gross payroll. The small businesses are eligible for up to five years, while the big companies can collect for up to 10 years. To qualify for the Small Employment program, firms must hire new full-time employees working 25 hours or more, have no more than 90 full-time employees at the time of program enrollment, can project and will hire a minimum of 10 new employees within the first year after enrollment, have or will have at least 75% of total sales to out-of-state customers or buyers, pay at least 80% of the new employees an annual wage that equals or exceeds 150% of the per capita average income of the county in which the jobs are located, and offers a basic health care plan.

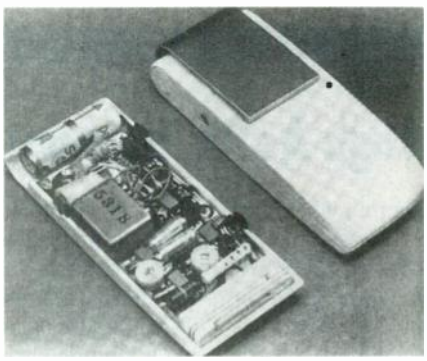
For more information, contact the Oklahoma Department of Commerce, P.O. Box 26980, Oklahoma City, OK 73126-0980; (800) 588-5959.—**DS**



40 YEARS AGO IN ELECTRONIC DESIGN

Pocket-Radio Signaling

A small, pocket-radio receiver under development at Bell Telephone Laboratories, 463 West St., N.Y., may result in city-wide personal radio signaling. Reporting in the current issue of *Bell Labs Record*, the new service is being tested in the Allentown-Bethlehem area of Pennsylvania. The system serves to indicate to a customer that some party is trying to reach him. The customer carries a small radio receiver in his pocket or clipped onto his belt. Upon receiving a radio signal with the proper code, the radio will emit an audible tone of sufficient loudness to inform the user that he is being called. He then goes to a telephone and calls a predesignated number where he is given the message.



These receivers, manufactured by the Stromberg-Carlson company, weigh approximately 8 oz., and will fit into a coat pocket. They employ a single 4-volt battery, having a life of about 900 hours. This is sufficient to provide about six months of service under normal conditions. The receiver uses four transistors—a surface-barrier transistor as a super-regenerative detector, two pnp junction transistors as audio amplifiers, and one npn junction transistor connected as a blocking oscillator, which is triggered when the proper code is received. *(Electronic Design, February 19, 1958, p. 10)*

And thus the beeper was born.—Steve Scrupski

Transistorized TV

An experimental all-transistor (except picture tube) battery-powered television receiver was recently announced by Motorola Inc. The first such set to be described, it employs 31 transistors and uses two rechargeable batteries which provide six hours of continuous operation away from commercial power. Performance is stated equivalent to conventional ac-powered vacuum-tube sets.

Although the new set draws only 12 W from its two nickel-cadmium batteries, a quarter of this is needed to supply the picture-tube filament. Motorola's Neil Frihart stated that their biggest "headache" was tuner design. Special transistors were required in the "head end" to get good high frequency sensitivity. Motorola wouldn't disclose tuner design or transistor types, but it is understood that a 41.25 mc sound and 45.75 mc video i-f are used, and designed to give somewhat greater gain than present commercial sets to compensate for lower tuner sensitivity. Batteries occupy only about 250-in^3. total, with a weight of less than 10 lb. Battery life is based on about 2000 recharging cycles minimum. A total charge takes just two hours while the set is connected to commercial power.

High-voltage is supplied to the picture tube anode at 20,000 V. Originally designed as a square-wave oscillator, Motorola engineers found that the high voltage supply worked better driven. The oscillator is now driven from the horizontal output at the scanning frequency of 15,750 cps. First, 12 V ac is stepped up to 2500 V, then quadrupled to the anode operating voltage. Horizontal scanning is accomplished by a switching type circuit with power fed to the yoke during retrace.

So far, only two sets have been built. While Motorola's aim is to produce a production model of a battery-portable TV, they don't expect to have a model available at a practical price until about 1960. (*Electronic Design, February 5, 1958, p. 5*)

The article doesn't mention the most basic benefit of semiconductors in TVs—reliability. No more trips to the local five-and-dime's tube tester to check out suspect tubes when the TV went on the fritz.—Steve Scrupski

Steve Scrupski is a former Editor-in-Chief of ELECTRONIC DESIGN. *Now semiretired, he can be reached at scrupski@worldnet.att.net.*

FREE STUFF

A free primer on Internet compression and encryption technology is now available. *The First Book of Compression and Understanding the Raw Materials of the Internet* includes a foreword by cryptography expert and privacy advocate Bruce Schneier. The 24-page booklet includes topics such as why compression and encryption are needed on the Internet; how the two technologies work together; and how to make and break codes. Contact Hi/fn, 2105 Hamilton Ave., Suite 230, San Jose, CA 95125; (408) 558-8066; fax (408) 558-8074; www. hifn.com.

A wall poster that graphically displays the contents and interrelationships of asynchronous transfer mode (ATM) signaling subsystems is now available from Harris & Jeffries Inc. The reference guide is intended as a time-saving tool for ATM product engineers, developers, and software specialists who use ATM signaling in their product lines. The guide describes the call message content—including setup, release, inquiry, drop-and-add party, and other functions—required in a standards-based ATM signaling system. It also defines the functional components that are required when developing UNI 3.0, 3.1, and 4.0 ATM signalling implementations. The poster also identifies the messages and timers used in certain scenarios, and provides an overview of the information contained in signaling messages. To obtain a free poster, contact Harris & Jeffries Inc., 888 Washington St., Dedham, Mass., 02026-6031; (781) 329-3200; (781) 329-4148; www.hjinc.com.

A free white paper that provides a detailed comparison of State Language versus Relay Ladder Logic, and sequential function charts for machine automation applications is now available to those interested in comparing the two language frameworks. Contact Control Technology Corp., 25 South St., Hopkinton, MA 01748; (508) 435-9595; fax (508) 435-2373; www.control.com.

TI DSP SOLUTIONS.

THE HEART OF THE WIRELESS WORLD.

The wireless market boomed in 1996, and TI was at the very heart of the action, providing DSPs in more than 50% of the 48 million digital cellular phones manufactured.* In 1997, TI's commitment to the wireless market helped to lead digital cellular sales to well over 80 million. Today, TI is a leading supplier of system software and hardware solutions based on a broad portfolio of standard and customizable DSP, ASIC, mixed-signal and RF devices, giving designers all the support they need to address wireless standards worldwide.

But the best is yet to come. So contact TI. Because when it gets right down to the heart of the matter, true success is getting to market not only faster, but with a far more competitive product. And TI has the wireless solutions to take you there.

TI is #1 worldwide with a DSP installed in every other digital cellular phone shipped.

Speed your designs to market with flexible wireless solutions, including digital, analog and software.

Build your wireless future with TI's global manufacturing capacity.

For more information call
1-800-477-8924, ext. 4081

www.ti.com/sc/4081

* Source: Dataquest 1997

READER SERVICE 186

14-9757

THE WORLD LEADER IN DSP SOLUTIONS

TEXAS INSTRUMENTS

GREENLOOK

The Institute for Interconnecting and Packaging Electronic Circuits (IPC), has been honored with an Environmental Champions award from *Chemical Engineering* and *Environmental Engineering World* publications. The organization and its affiliates were recognized for their voluntary participation in the Environmental Protection Agency's (EPA) Design For The Environment (DfE) printed-wiring-board (PWB) project.

The PWB project was launched in 1993 when IPC formed a relationship with the EPA. Partners in this project include the University of Tennessee, the Microelectronics and Computer Technology Corporation (MCC).

IPC was recognized specifically for its efforts with the DfE Making Holes Conductive (MHC) project. MHC evaluated various technologies for metallizing plated-through holes. The most common MHC technology is the electroless copper process which uses formaldehyde and other hazardous chemicals, as well as large quantities of water.

The MHC project participants identified seven alternative technologies for testing: nonformaldehyde electroless, various carbon and graphite processes, palladium and tin-palladium, and a conductive polymer. Then, they developed a test vehicle, designed the testing protocol, and executed the workplan. The DfE project participants also published five major documents and eight case studies on various pollution prevention techniques. A draft document, "Cleaner Technologies Substitute Assessment" (CTSA), details the results and data from the DfE MHC project.

HR Industries has already implemented the conductive polymer process for its new facility. It can produce 200 PWB panes a day using 60,000 gallons of water and yielding 2 ft^3 of waste sludge. The previous plant had used 100,000 gallons of water and produced 15 ft^3 of sludge to produce only 1000 PWB panels.

For more information, contact Christopher Rhodes at the IPC, 2215 Sanders Rd., Northbrook, IL 60062-6135; (847) 509-9700, ext. 306, fax (847) 509-9798, e-mail: rhodch@ipc.org.

Lee Goldberg

Go for the winning combination with Illinois Capacitor.

IC puts it all together with world class quality, fast delivery and applications support.

Designing and building today's sophisticated circuits are complex enough without worrying about sourcing the right capacitors. When you choose Illinois Capacitor, you'll always be assured of the highest levels of performance.

No other manufacturer can provide IC's winning combination of 100% burn-in testing, fast delivery, value added services and in-depth applications engineering support. With state-of-the-art technology, competitive pricing and a broad line to choose from, we're easy to work with.

Go for the winning combination. Call IC or your local IC distributor today.

Samples available upon request.

Ask for our FREE Capacitor Engineering Guide.

READER SERVICE 140

ILLINOIS CAPACITOR, INC.®

3757 W. Touhy Ave., Lincolnwood, Illinois 60645
(847) 675-1760 • Fax (847) 673-2850

THE SOURCE FOR QUALITY, PERFORMANCE AND DELIVERY.

MANAGING THE DESIGN FACTORY

Why Specifications Must Change

DON REINERTSEN

As long as there have been engineers, there have been staffs who have offered to help engineers do their jobs. And, as long as there have been staffs, there have been written reports saying that it's bad to change a product specification during development. "Your projects are always late and over budget," the staff observes, "and we will help you find out why. We will independently analyze the situation and objectively determine the root cause. By the way, what do you think the root cause is?"

Smart engineers know the right answer to this question. You can tell the truth and avoid any personal responsibility by saying, "Isn't it obvious? Marketing changed the specification." The staff will believe this every time. The logic is flawless. Changing specifications causes rework. Rework causes delays and extra spending. Delays and extra spending are bad. Therefore, logic dictates that changing specifications is bad. The staff concludes that the key to eliminating both delays and extra spending is to prevent the specification from changing.

Is there a chance that this conclusion is, well, rather shallow? In fact, there are three fallacies to this logic. First, not all specification changes cause added work or delay—sometimes they reduce work. In the early stages of design, it is easy for a design team to naively agree to do the impossible. Only later do they discover that they signed up to break the laws of physics. In such cases, requirements relief is a powerful tool to prevent wasted effort and delays. If you only look at specification changes that cause rework and delay, you will conclude that all specification changes are bad.

The second fallacy is the idea that all changes that cause rework and delays should be eliminated. In fact, you can only judge a specification change compared to its alternative. For example, what happens when an OEM customer says, "I know I asked for a 100-MHz part, but I've decided that I now need a 120-MHz part. If I can't get one from you, you lose the order." Now in this case, it's true that a specification change may cause expensive rework and delays. However, the alternative is to sell nothing. When the overall benefit of a change exceeds its overall cost, you should make the change—even if it adds work and time.

The third and most subtle fallacy is that it is useful to conclude whether specification changes on the whole are either "good" or "bad." In reality, specification changes lie along a continuous spectrum from "extremely good" to "extremely stupid." To blindly permit all specification changes is as dumb as it is to blindly deny them. All cases must be handled individually.

We do not need to eliminate specification changes; we need to eliminate stupid specification changes. The real root of the problem is not specification changes; it's that companies lack a rational system for handling specification changes. Without such a system they either abdicate their responsibilities and let specifications change continuously, or overreact and try to eliminate all specification changes.

Ensure that all relevant and available information is used to generate the original specification. Since most of the good stuff is stored in people's heads, the specification should be created by a cross-functional team. Then, develop a process to react rationally and quickly to new information that becomes available during development. Remember, if you can't change a product specification during development, you're stuck with what you knew at the beginning of the process. This a great way to design products that the market used to want.

Don Reinertsen is president of Reinertsen & Associates, a consulting firm specializing in product development management. He can be reached at (310) 373-5332 or e-mail: DonReinertsen@compuserve.com.

Y2K UPDATE

Now into the countdown phase of Year 2000 (Y2K) compliance, some companies have decided to scrap the entire measure, choosing instead to just refurnish their offices with new or used equipment that's already compliant. This solution can be quite expensive, but when a company's livelihood is on the line, cost is no object. However, there is one company that is making the big buys easier to swallow by offering a handy online resource.

Affiliated ReMarketing Web Inc. (ARW) has been running their business-to-business used computer site on the web for three years. Their philosophy is that because millions of computers are expected to be bought and sold in order to reach Y2K compliance, there ought to be a fast and easy way to do it.

The site, *www.remarketing.com*, lists inventory of used mainframes, routers, workstations, PCs, etc. Over 200 used computer dealers (about 25% of the used computer industry) sells their wares from the site. Additionally, site visitors can sell their old computers by simply adding their listing to the database.

Shoppers at the site can find their computers by searching by manufacturer, model number, or type. Computer listings feature descriptions, quantity, price, contact information, and other facts relevant to a potential purchase. Some listings show whether they are Y2K compliant or not, but if you're specifically searching for compliant systems, there are direct links to IBM's "Year 2000 Product Readiness" page and Digital's "Digital Year 2000 Ready" page.

There are options at the site leasing computers. If this is a direction that you might choose, click on "Competitive Lease Quote," or "Directories of Dealers/Lessors" (hardware and software) for estimates. Also, there are exporters and maintenance companies affiliated with the site.

For more information, contact ARW Inc., P.O. Box 14264, RTP, NC 27709; (919) 933-8533; fax (919) 933-8813.—**DS**

Behold, The Dawn Of A New Era In CE Mark Testing!

C'mon - the new dawn!

KeyTek EMC Test Systems have been setting the industry standards since 1975.

Forget all the marketing hype - KeyTek EMC Test Systems are multi-capability **design tools** that enable Design Engineers to **reduce time-to-market cycles**.

They also make CE Mark **self-certification** remarkably easy - anyone can do it.

Well, maybe not Marketing.

CUSTOMER-CONFIGURABLE SYSTEMS

KeyTek's no-nonsense EMC systems are used by engineers worldwide for affordable and flexible in-house EMC testing during design, certification and production stages. Remarkably easy to use, KeyTek's systems are the right tools for testing to both regulatory (CE Mark) and company driven standards. KeyTek design tools make it easy for engineers to shorten design cycles and increase product quality and reliability, a competitive edge every company can justify.

AFFORDABLE & EFFICIENT DESIGN TOOLS

RF IMMUNITY & EMISSION TEST SYSTEMS

SIMULATORS FOR ESD, EFT, SURGE, MAGNETIC FIELDS, DIPS & INTERRUPTS

Call or e-mail KeyTek to learn how you can do EMC Testing!

1 800 753 9835, ext. 198

Tel: 978 275 0800 • Fax: 978 275 0850

E-Mail: sales@keytek.com • www.keytek.com

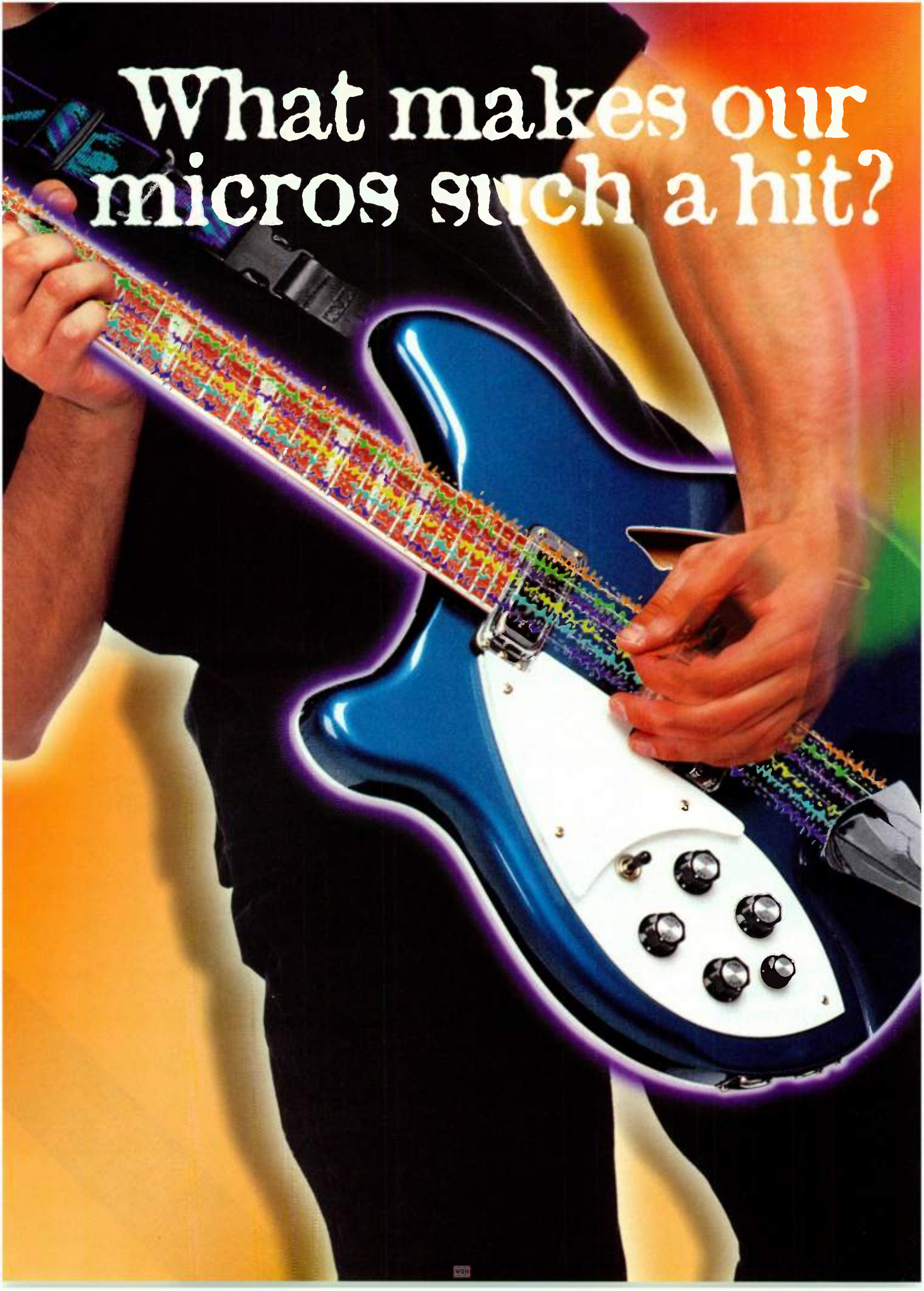
KeyTek

A Thermo Voltek Company

NATIONAL DESIGN ENGINEERING Show and Conference March 16–19, 1998 • McCormick Place • Chicago

See Us At Booth 8559

READER SERVICE 145


What makes our micros such a hit?

Rock Solid Noise Immunity

SGS-THOMSON ST62 micros deliver more performance in less space for less money. Even the core is optimized for cost-effective operation.

That's more than enough to make them a hit. But when you add ESD protection and legendary rock-solid noise immunity, our ST62s sound almost too good to be true MCUs.

But they're for real. All ST62s contain ROM and RAM. All have an EPROM counterpart. Some versions offer on-board EEPROM for calibration. Each ST62 includes an 8-bit timer with 7-bit programmable prescaler as well as multifunction, individually programmable I/O ports. Devices with high current capability to directly drive LEDs or TRIACs, along with a wide range of peripherals such as ADC, PWM and LCD drivers. SCI and SPI are also available. A wide voltage range allows the ST62 to be powered directly from battery or mains with minimum external components. Plus what you'll recognize as the industry's most extensive family of support tools.

So don't just string along with any old micros. Rock with the hottest numbers in the industry. ST62. They just might make you a star. To find out more fax 781-259-9442, or write SGS-THOMSON, 55 Old Bedford Rd., Lincoln, MA 01773. Visit our web site at http://www.st.com

SAVE $62 ON AN ST62 STARTER KIT

Save up to $62 on an ST62 Starter Kit. Includes demo board, EPROM samples, plus all the hardware and software needed to complete your design. Limited time offer. Fax or write now for details.

SGS-THOMSON MICROELECTRONICS

Bringing Microelectronics to Life™

For More Info Turn Page

READER SERVICE 142

Travel Made Easy

Want to buy a gift for the person who has everything? How about a portable driver information system that goes for just under $400.00. This product, which hails from Ultradata Systems Inc., St. Louis, Mo., promises to provide navigation, directions, and a host of related services across the country at the push of a button.

Aptly known as TravelStar, the information system can be easily transported in a briefcase. The unit consists of a car-radio-sized terminal and a GPS receiver the size of a computer mouse. The user simply attaches the receiver to the car's windshield and it's ready to go.

TravelStar works by using (Global Positioning Satellite) GPS signals to identify a driver's latitude and longitude coordinates, direction of travel, current interstate, or any other specific location on any road in the continental U.S. Then, by selecting a category, such as gas, food, or lodging, the driver can access directions to nearby services. This information is presented to the driver in an easy-to-understand textual format.

Based on the company's patented data-compression technology, TravelStar also allows the user access to literally thousands of services stored in the terminal's memory. This feature is crucial because even when GPS signals are blocked, the user can still access preprogrammed directions between over 250 metro areas. Additionally, the user can acquire information on distance, drive time, and heading information to one of more than 7000 towns in the U.S.

The user can also take advantage of enhanced service offered by Westar Mobile Services. Turn-by-turn directions, emergency services, roadside assistance services, and concierge services are available by simply calling the Westar Support Center. Additionally, annual plug-in module updates and detailed city plug-in modules, will be available to the user at just under $50.

Although it's an ideal gift for the business traveler unfamiliar with the roads in certain areas, TravelStar does have one drawback—it makes it virtually impossible to use the old excuse "I took a wrong turn," the next time you're late for that important business meeting, job interview, date, or dinner at your mother-in-Law's house.

For more information on the TravelStar call (800) 747-2605 or fax (314) 997-1281. Ultradata Systems is located at 9375 Dielman Industrial Dr., St. Louis, MO 63132.

Cheryl Ajluni

We partner with you to get the job done right and on-time.

Deltron provides:

- On-site engineering assistance
- Prototypes in two weeks
- J.I.T. delivery

PERFORMANCE GUARANTEED

VR • CV • V Series
Hi-Rel Power Supplies

- 200K - 1 Million Hrs. MTBF
- 120 - 700 Watts
- 1 - 4 Outputs
- Low Cost

Deltron inc.
POWER PRODUCTS

VR SERIES HI-REL SWITCHERS

Single Output • 300-700 Watts

DESCRIPTION

VR Series World Class switching power supplies are a family of single output models designed for applications requiring ***Ultra Reliability*** and ***Low Cost!*** These supplies have actual demonstrated MTBF ratings up to 1 million hours. The time tested design has been continually updated to take advantage of the latest technological improvements in circuits and components resulting in the fine performance of these supplies.

MODELS & RATINGS

Max Power	Output	Model
300W	5V @ 50A	VR300AXX
	12V @ 25A	VR300BXX
	15V @ 20A	VR300CXX
	24V @ 12A	VR300DXX
	48V @ 6A	VR300EXX
500W	5V @ 80A	VR500AXX
	12V @ 40A	VR500BXX
	15V @ 30A	VR500CXX
	24V @ 20A	VR500DXX
	48V @ 10A	VR500EXX
700W	5V @120A	VR700AXX
	12V @ 58A	VR700BXX
	15V @ 46A	VR700CXX
	24V @ 29A	VR700DXX
	48V @ 15A	VR700EXX

FEATURES

- *UL, CSA, TÜV (IEC, EN), CE.*
- *5.5 watts per cubic inch.*
- *80% typical efficiency.*
- *1,000,000 hrs. demonstrated MTBF.*
- *Stock delivery.*
- *Full complement of options.*

VR OPTIONS

Option Code	Function
00	None
01	Power Fail Monitor
02	Auto Ranger
04	Pilot Bias
08	Screen Cover
16	End Fan Cover
32	Top Fan Cover

To order, replace "XX" in model number with sum of Option Codes desired.

CV SERIES ENCLOSED SWITCHERS

Single Output • 360-600 Watts

DESCRIPTION

The CV Series is a line of low profile, fan cooled power supplies which utilize Deltron's field proven V Series components. CV units are single output models in a rugged enclosed package nominally 3 inches in height and 5 inches in width. With power ratings of 360 to 600 watts, these units are a space saving alternative to 5 x 8 inch shoe box modules.

MODELS & RATINGS

Max Power	Output	Model
360W	5V @ 72A	CV360AXX
	12V @ 30A	CV360BXX
	15V @ 24A	CV360CXX
	24V @ 15A	CV360DXX
	28V @ 13A	CV360JXX
	48V @ 7.5A	CV360EXX
500W	5V @ 100A	CV501AXX
	12V @ 42A	CV501BXX
	15V @ 33A	CV501CXX
	24V @ 21A	CV501DXX
	28V @ 18A	CV501JXX
	48V @10.5A	CV501EXX
600W	5V @ 120A	CV601AXX
	12V @ 50A	CV601BXX
	15V @ 40A	CV601CXX
	24V @ 25A	CV601DXX
	28V @21.5A	CV601JXX
	48V @12.5A	CV601EXX

FEATURES

- *UL, CSA, TÜV (IEC, EN), CE.*
- *4 watts per cubic inch.*
- *80% typical efficiency.*
- *200,000 hrs. demonstrated MTBF.*
- *Heavy duty enclosed chassis.*
- *Full complement of options.*

CV OPTIONS

Option Code	Function
00	None
02	Power Fail Monitor
04	Thermal Shutdown
08	Logic Inhibit
16	Auto Ranger

To order, replace "XX" in model number with sum of Option Codes desired.

V SERIES OPEN FRAME SWITCHERS

Single & Quad Outputs • 120-600 Watts

DESCRIPTION

V Series World Class switching power supplies are a family of single and quad output models designed for a wide variety of commercial and industrial applications. These industrial workhorses have demonstrated MTBF ratings greater than 500,000 hours. A proprietary proportional drive circuit prevents excess switch saturation and permits higher switching frequency operation. This makes possible increased reliability and a compact size.

One of the unique features of the V Series is a dual loop regulation system. This system provides a tightly regulated main output and eliminates cross regulation in the auxiliaries.

FEATURES

- *UL, CSA, TÜV (IEC, EN), CE.*
- *4.8 watts per cubic inch.*
- *80% typical efficiency.*
- *500,000 hrs. demonstrated MTBF.*
- *High power auxiliaries.*
- *High peak current capability.*
- *Full complement of options.*

SINGLE OUTPUT

Max Power	Output	Model
120W	5V @ 25A	V120AXX
	12V @ 10A	V120BXX
	15V @ 8A	V120CXX
	24V @ 5A	V120DXX
180W	5V @ 36A	V180AXX
	12V @ 15A	V180BXX
	15V @ 12A	V180CXX
	24V @7.5A	V180DXX
250W	5V @ 50A	V250AXX
	12V @ 21A	V250BXX
	15V @ 17A	V250CXX
	24V @ 11A	V250DXX

Max Power	Output	Model
270W	5V @ 54A	V270AXX
	12V @ 22A	V270BXX
	15V @ 18A	V270CXX
	24V @ 12A	V270DXX
360W	5V @ 72A	V360AXX
	12V @ 30A	V360BXX
	15V @ 24A	V360CXX
	24V @ 15A	V360DXX

Max Power	Output	Model
500W	5V @100A	V501AXX
	12V @ 42A	V501BXX
	15V @ 33A	V501CXX
	24V @ 21A	V501DXX
600W	5V @120A	V601AXX
	12V @ 50A	V601BXX
	15V @ 40A	V601CXX
	24V @ 25A	V601DXX

Other voltages, e.g. 2V, 3.3V, 28V, and 48V available on special order.

QUAD OUTPUT

Max Power	Output 1	Output 2	Output 3	Output 4	Model
225W	5V @ 30A	+12V @ 6(12)A	-12V @ 4A	-5V @ 4A	V225AXX
	5V @ 30A	+12V @ 6A	-12V @ 4A	+24V @ 4(8)A	V225BXX
	5V @ 30A	+15V @ 6(12)A	-15V @ 4A	-5V @ 4A	V225CXX
	5V @ 30A	+15V @ 6A	-15V @ 4A	+24V @ 4(8)A	V225DXX
	5V @ 30A	+12V @ 6(12)A	-12V @ 4A	+12V @ 4A	V225EXX
300W	5V @ 40A	+12V @ 4A	-12V @ 4A	-5V @ 3A	V300AXX
	5V @ 40A	+12V @ 4A	-12V @ 4A	+24V @ 3(5)A	V300BXX
	5V @ 40A	+15V @ 4A	-15V @ 4A	-5V @ 3A	V300CXX
	5V @ 40A	+15V @ 4A	-15V @ 4A	+24V @ 3(5)A	V300DXX
	5V @ 40A	+12V @ 4A	-12V @ 4A	+12V @ 3(5)A	V300EXX
325W	5V @ 45A	+12V @ 8(16)A	-12V @ 6A	-5V @ 4A	V325AXX
	5V @ 45A	+12V @ 8A	-12V @ 6A	+24V @ 4(8)A	V325BXX
	5V @ 45A	+15V @ 8(16)A	-15V @ 6A	-5V @ 4A	V325CXX
	5V @ 45A	+15V @ 8A	-15V @ 6A	+24V @ 4(8)A	V325DXX
	5V @ 45A	+12V @ 8(16)A	-12V @ 6A	+12V @ 4A	V325EXX
400W	5V @ 50A	+12V @ 8A	-12V @ 8A	-5V @ 4A	V400AXX
	5V @ 50A	+12V @ 8A	-12V @ 8A	+24V @ 4(6)A	V400BXX
	5V @ 50A	+15V @ 8A	-15V @ 8A	-5V @ 4A	V400CXX
	5V @ 50A	+15V @ 8A	-15V @ 8A	+24V @ 4(6)A	V400DXX
	5V @ 50A	+12V @ 8A	-12V @ 8A	+12V @ 4(6)A	V400EXX
500W	5V @ 60A	+12V @ 10A	-12V @ 10A	-5V @ 5A	V500AXX
	5V @ 60A	+12V @ 10A	-12V @ 10A	+24V @ 5(8)A	V500BXX
	5V @ 60A	+15V @ 10A	-15V @ 10A	-5V @ 5A	V500CXX
	5V @ 60A	+15V @ 10A	-15V @ 10A	+24V @ 5(8)A	V500DXX
	5V @ 60A	+12V @ 10A	-12V @ 10A	+12V @ 5(8)A	V500EXX
600W	5V @ 80A	+12V @ 10(20)A	-12V @ 10A	-5V @ 5A	V600AXX
	5V @ 80A	+12V @ 10A	-12V @ 10A	+24V @ 5(10)A	V600BXX
	5V @ 80A	+15V @ 10(20)A	-15V @ 10A	-5V @ 5A	V600CXX
	5V @ 80A	+15V @ 10A	-15V @ 10A	+24V @ 5(10)A	V600DXX
	5V @ 80A	+12V @ 10(20)A	-12V @ 10A	+12V @ 5A	V600EXX

V OPTIONS

Option Code	Function
00	None
01	OVP protects all auxiliaries
02	Power Fail Monitor
04	Thermal Shutdown
08	Cover
16	Logic Inhibit
32	Post Regulator for output 4

To order, replace "XX" in model number with sum of Option Codes desired.

NOTES:

1. *Numbers in parentheses ( ) are peak ratings for short duration service such as motor starting.*
2. *Output 1 is floating and can be either polarity.*
3. *Quads require 10% of maximum power distributed among auxiliary outputs for optimum performance.*
4. *Outputs can operate to no load with slight increase in specifications.*

SPECIFICATIONS

INPUT
90-132 VAC or 180-264 VAC, 47-440 Hz.
Consult factory for 400 Hz. operation.

EMISSIONS
FCC 20780 Part 15/EN 55022, Class A Conducted.
EN 61000-3-3, Voltage Fluctuations.

IMMUNITY
IEC 1000-4-2/EN 61000-4-2, Electrostatic Discharge.
IEC 1000-4-3/EN 61000-4-3, Radiated Field.
IEC 1000-4-4/EN 61000-4-4, Electrical Fast Transients.
IEC 1000-4-5/EN 61000-4-5, Level 3 Surge.
IEC 1000-4-6/EN 61000-4-6, Conducted Field.

INPUT SURGE
17 amps peak from cold start for models up to 250 watts and VR300, 68 amps for other models, from nominal 110 or 220 VAC.

EFFICIENCY
80% typical.

HOLDUP TIME
20 milliseconds after loss of nominal AC power.

OUTPUTS
See table of models.

LINE REGULATION
±0.1% for line change from nominal to min. or max. rating with 20% min. load on the measured output.
±0.05% with post regulator and no min. load.
Singles to no load.

LOAD REGULATION

5V main/singles	±0.2%		
-5V aux.	±3%	**Post Regulated Outputs**	
±12V aux.	±2%	Option 32	±0.05%
±15V aux.	±2%		
+24V aux.	±1.5%		

for load change from 60% to 20% or 100% max. rating.
With post regulator to no load. Singles to no load.

CROSS REGULATION
±0.2% for load change on the main 5V output from 75% to 50% or 100% max. rating with 20% min. load on the measured output.
±0.05% with post regulator and no min. load.
Not applicable to singles.

CENTERING

5V main/singles		±5% trim adj.
Aux. 1 and 2		±5% trim adj. tracking
Aux. 3:	-5V	±3%
	+12V	±2%
	+24V	±1%

with all outputs loaded to 50% max. ratings and output #2 set precisely at its rated value. With post regulator ±3% trim adj.

RIPPLE & NOISE
1% or 100 mV, pk.-pk., 20 MHz bandwidth.

OPERATING TEMPERATURE
0-70°C. Derate 2.5%/°C above 50°C.

COOLING

Models	Forced Air
V120, V180, V225, V250, V270, V300, VR300, V360	30 CFM
V325, V400, V500, VR500, V501, V600, V601, VR700	60 CFM

TEMPERATURE COEFFICIENT

5V main/singles	±0.02%/°C
Auxiliaries	±0.05%/°C
With post regulator	±0.02%/°C

DYNAMIC RESPONSE
Peak transient less than ±2% or ±200 mV for step load change from 75% to 50% or 100% max. ratings.

RECOVERY TIME
Less than 400 microseconds on main/singles output.
Less than 50 microseconds on post regulated auxiliaries.

SAFETY
Units meet UL 1950, CSA 22.2 No. 950, EN 60 950, IEC 950.

DIELECTRIC WITHSTAND
3750 VRMS input to ground.
3750 VRMS input to output.
700 VDC output to ground.

SPACING
8 mm primary to secondary.
4 mm primary to grounded circuits.

LEAKAGE CURRENT
0.75 mA at 115 VAC, 60 Hz. input.

INPUT UNDERVOLTAGE
Proprietary proportional drive and low voltage lockout protects against damage for undervoltage operation.

SOFT START
Units have soft start feature to protect critical components.

OVERVOLTAGE PROTECTION
Standard on main output/singles. Optional on auxiliaries.

REVERSE VOLTAGE PROTECTION
All outputs are protected up to load ratings.

OVERLOAD
Outputs short circuit protected by current foldback with automatic recovery. Post regulators have individual current foldback protection.

REMOTE SENSING
On singles/5V mains which are fully isolated from all auxiliaries.

SHOCK & VIBRATION
Shock per MIL-STD 810-E Method 516.4, Procedure I.
Vibration per MIL-STD 810-E Method 514.4, Category 1, Procedure I.

MECHANICAL

MODELS	H	x	W	x	L
VR300	2.50"	x	4.85"	x	8.50"
VR500, VR700	2.75"	x	4.85"	x	10.50"
CV360, CV501, CV601	3.15"	x	4.85"	x	12.63"
V120, V180, V250	2.50"	x	4.75"	x	8.50"
V270, V360, V501, V601	2.50"	x	4.75"	x	10.50"
V225, V325	2.50"	x	5.00"	x	10.50"
V300, V400, V500, V600	2.75"	x	5.00"	x	13.00"

OPTIONS & ACCESSORIES

POWER FAIL MONITOR
Optional monitor provides a TTL signal 2 ms. min. prior to loss of output power with outputs fully loaded from 100VAC/200VAC line loss.

THERMAL SHUTDOWN
Special circuit cuts off supply in case of local over temperature. Unit resets automatically when temperature returns to normal. Standard on VR Series. Optional for CV and V Series.

COVERS
Optional end and top fan covers for VR Series.
Optional safety/EMI cover for V Series.

INHIBIT
TTL logic inhibit input. Standard for VR Series. Optional for CV and V Series.

PILOT BIAS
Optional for VR Series only. SELV 5V @ 1A source for external use with provision for operating the inhibit either with a switch or TTL Logic. Either NO or NC can be selected.

AUTO RANGER
Special circuit provides automatic operation at specified input ranges without strapping. Optional for VR and CV Series. For V Series specify AR-1 accessory.

POST REGULATOR
Optional for output #4 on V300, V400, V500, V600 models. Ratings available are -5V @ 4A, +12V @ 3A, or +24V @2A.

Deltron inc.
290 WISSAHICKON AVENUE, P.O. BOX 1369, NORTH WALES, PA 19454
PHONE: 215-699-9261 • FAX: 215-699-2310 • TOLL FREE: 1-800-523-2332
E-MAIL: sales@deltroninc.com • VISIT OUR WEB SITE: www.deltroninc.com

SO REAL.

SO SMALL.

TI INTRODUCES WORKSTATION GRAPHICS CAPABILITIES FOR PCs.

Now the visual reality of workstation graphics is possible for the PC. TI's TVP4020 (PERMEDIA® 2) is the industry's complete graphics solution. The TVP4020 is the only graphics processor to deliver 3-D, 2-D, AGP, PCI and TI's award-winning 230-MHz RAMDAC on the same fully integrated device. An external memory of up to 8 Mb allows designs to be modified based on the application.

Plus, robust software drivers support Direct 3-D, OpenGL and Heidi for both Microsoft® Windows® 95 and Windows NT™, so it's compatible with the newest PC games. With all this and flexible frame and texture allocation, the TVP4020 delivers for the ultimate in immersive play.

For more information, contact us at:
***1-800-477-8924, ext. 5051**, or*
www.ti.com/sc/3D

READER SERVICE 187

SIGNAL & ANALOG

TEXAS INSTRUMENTS

HEADS UP

Ever Heard Of Low-Temperature Polysilicon Displays? You Will

Flat-panel displays represent both a bright spot and a trouble spot for major Asian producers. It is one of the few industries to show growth, but has been subject to boom and bust cycles—the next of which should materialize in 1998 for 12.1-in.-sized displays.

A new process is moving into production that could help cushion the next blow, however. It's called low-temperature polysilicon (LTPS) processing, and it's likely to become the next major innovation to sweep through the LCD industry.

CHRIS CHINNOCK

Signs of this new technology are already showing up in Japan. Camcorders from Panasonic are specifically advertising that they're "made with low-temperature polysilicon processing." Both direct-view and projection products for entertainment, communications, and computer applications are expected to use these displays, so add LTPS to your lexicon.

What LTPS does is allow manufacturers to fabricate both on-screen transistors and off- screen driver electronics on a single substrate, using the same fabrication processes. By contrast, today's active-matrix process uses amorphous silicon processing to make the on-screen transistors. Amorphous silicon does not have the electrical characteristics to allow fabrication of the driver electronics, however. These circuits are fabricated in traditional IC foundries, and the chips are interconnected to the LCD. LTPS displays eliminate these discrete components and the assembly costs associated with connecting them to the LCD. The result is a higher performance display made at lower cost.

Polysilicon displays are fabricated by converting amorphous silicon. An an excimer laser is used to melt and recrystallize it. This technique improves the electron mobility by a factor of about 100, allowing smaller on-screen transistors. Smaller transistors allow designers to choose between producing a brighter display, due to a smaller aperture ratio, or maintaining the brightness and reducing the size of the backlight. The latter option produces a lighter, smaller, and less power-hungry display.

LTPS also allows higher resolution and more reliable displays. Tape-automated bonding, which connects the discrete drivers in amorphous displays, is the primary source of reliability problems.

But the most compelling reason to adopt LTPS processing is profitability. The flat-panel-display market-research firm DisplaySearch, Austin, Tex., recently completed an analysis of the LTPS process. According to their calculations, LTPS displays below 11-in. will be cheaper than those made using the traditional amorphous-silicon processing. A 6-in. VGA display, for instance, would be 17% to 27% cheaper, while a 2-in. VGA display would be as much as 40% to 60% cheaper than a comparable amorphous-silicon product (a 2-in. VGA amorphous-silicon display can not be produced, however—another benefit of LTPS).

LCD manufacturers also are looking to LTPS to reinvigorate older manufacturing lines. Their "generation two" lines were built several years ago to produce 10.4-in. displays. But the market has moved on to 12-in. and larger displays as the volume leaders. Unfortunately, these older lines cannot make the larger displays at a competitive cost, and demand for the smaller displays has been weak.

So manufacturers can either mothball these older lines or convert them to LTPS. Many producers have decided that conversion is a better option, but some, like Toshiba and Sony are building new lines for LTPS.

Where will these new LTPS displays go? Toshiba and Mitsubishi have announced that they plan to develop LTPS displays for the laptop market, presumably a 12.1-in. or 13.x-in. display. Other vendors, such as Sanyo, Sharp, Sony, and Matsushita are targeting smaller-sized display applications such as camcorders, digital camera viewfinders, projection, and autonavigation. Even emerging Korean LCD suppliers LG Electronics and Samsung are talking about LTPS.

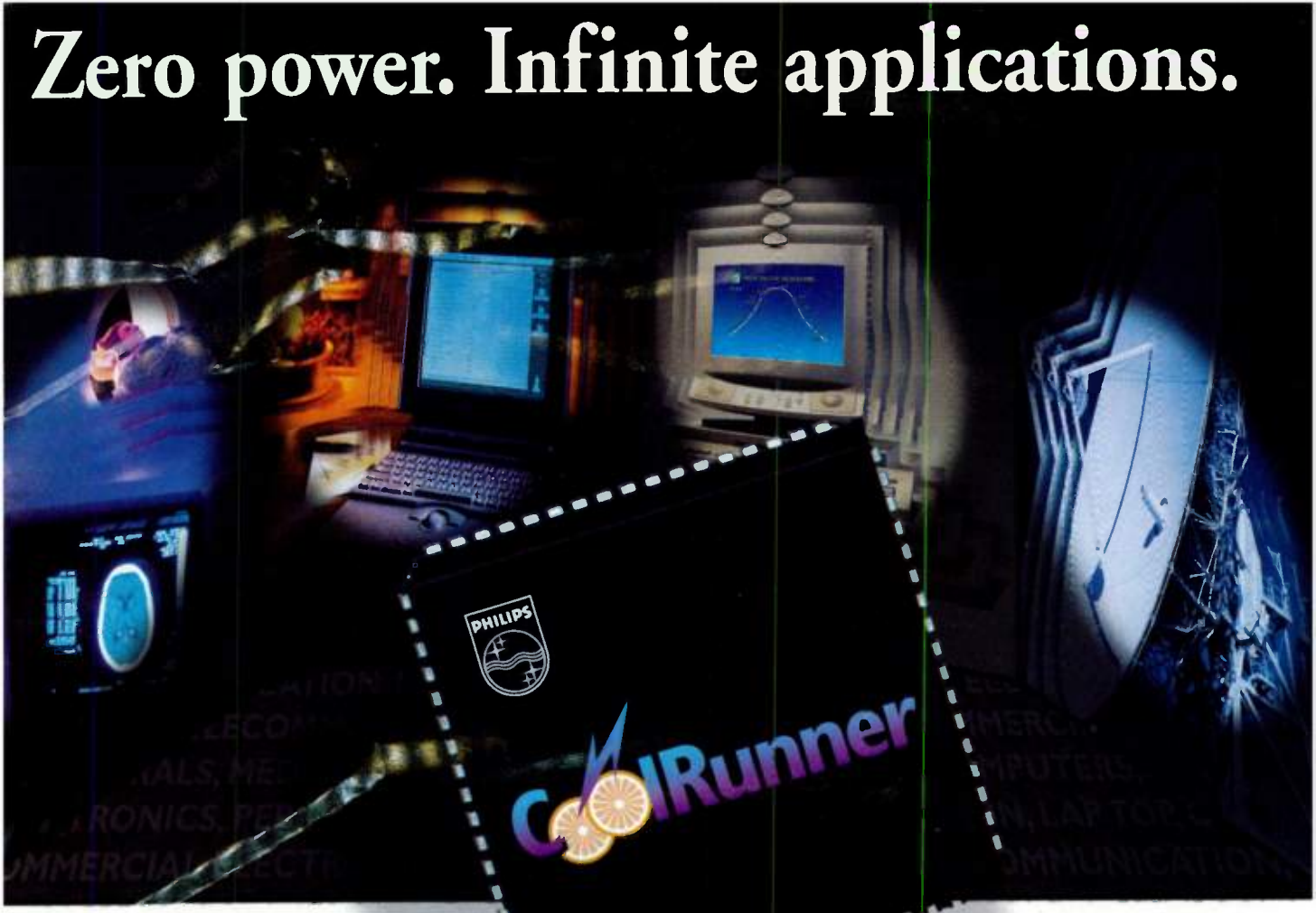
While most of these vendors are tight-lipped about their plans, equipment suppliers are optimistic. For example, excimer laser supplier Lambda Physic, notes that they are now seeing customers ordering second and third laser annealing systems. XMR Corporation, a supplier of polysilicon-laser-conversion equipment, sees a similar trend in the supply of production-grade machines. According to Ben Goldfine, XMR's director of sales and marketing, "Most of the LTPS process development has now been done. We see 1998 as the year of transition into full volume production."

DisplaySearch's projections seem to back this up. President Ross Young predicts LTPS capacity to grow 1130% over the next two years, and in five years, 40% of the market for small to medium-sized flat panel displays will be LTPS products. "That's $4.8 billion in display business," says Young.

So the die seems to be cast for manufacturers to embrace LTPS processing. Hurdles could yet emerge as they ramp to full production, but these will probably be jumped.

Chris Chinnock has an electrical engineering degree from the University of Colorado and reports on flat-panel displays and other emerging technologies. His company, Technical Marketing Service, provides writing, marketing, and public relations services to technology companies. Chinnock can be reached at (203) 849-8059; fax (203) 849-8069; e-mail: chrischinnock@compuserve.com.

Zero power. Infinite applications.



If you think using CPLDs means sacrificing power, Philips and Future Electronics are going to change your mind. Going from zero to infinity in the blink of an idea is no longer a designer's fantasy. Now your CPLD solution is real, fast, and very cool.

With CoolRunner™ 3V and 5V CPLDs, featuring Fast Zero Power (FZP™) — only from Philips — you can significantly increase performance while reducing power by up to 75%. And with guaranteed pin-locking and wide input logic blocks, the CoolRunner XPLA™ is the architecture that makes sense for all your In-System Programming needs - prototyping, production, production code changes, and infield system upgrades. There's no expensive sockets, no separate steps to programming before assembly. So instead of thinking about losing power, think about your prototyping and manufacturing possibilities.

Contact Future Electronics before you design in your Philips CPLDs. As a worldwide leader in electronic components distribution, we have been delighting customers for almost 30 years with innovation, imagination... and powerful partners such as Philips. We'll change your way of working.

PHILIPS

Let's make things better.

www.coolpld.com

FUTURE ELECTRONICS

Call 1-800-FUTURE-1 Ext. 2255

http://www.future.ca

THE AMERICAS · EUROPE · ASIA/PACIFIC

"Experience The Service That Wins The Awards... Worldwide"

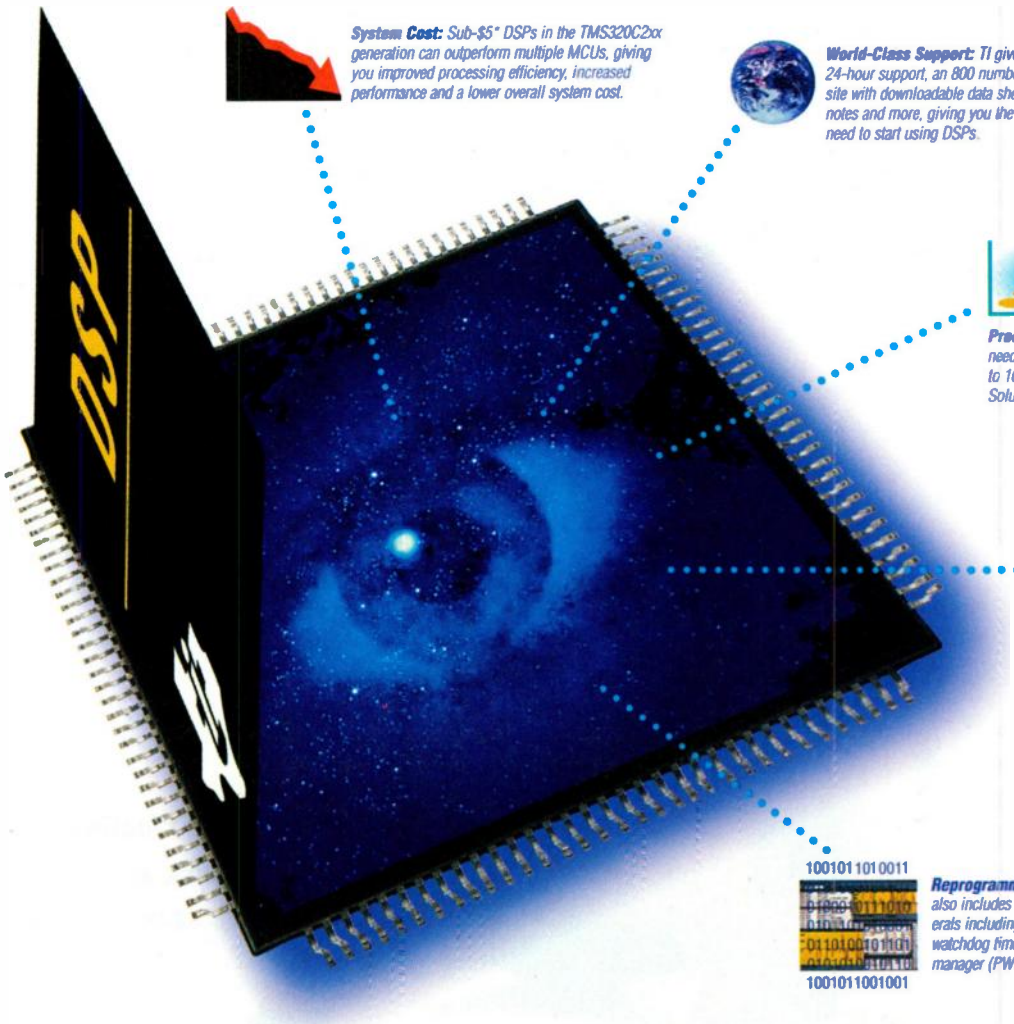
CoolRunner, FZP and XPLA are trademarks of Philips Electronics North America Corporation

1465

READER SERVICE 130

CHANGING FROM MCUs TO DSPs REQUIRES A LITTLE GIVE AND TAKE.

THE WORLD LEADER IN



System Cost: *Sub-$5* DSPs in the TMS320C2xx generation can outperform multiple MCUs, giving you improved processing efficiency, increased performance and a lower overall system cost.*

World-Class Support: *TI gives you 24-hour support, an 800 number and a Web site with downloadable data sheets, application notes and more, giving you the backup you need to start using DSPs.*

Product Selection: *TI has the DSP you need now and in the future. From 20 MIPS to 1600 MIPS, TI is the #1 supplier of DSP Solutions worldwide.*

Third-Party Development: *TI's extensive network of over 300 third-party suppliers gives you all the products, development platforms and software algorithms you need to get up and running quickly and easily.*

100101101 0011

Reprogrammability: *The TMS320C2xx generation also includes DSPs with on-chip controller peripherals including up to 32K words of flash memory, watchdog timer, SPI, SCI and CAN Ports, event manager (PWM) and 10-bit A/D converters.*

1001011001001

WE GIVE. YOU TAKE.

DSP Solutions from Texas Instruments give you an easy way to transition to the power and performance today's market demands. With 20 MIPS and control code execution that's up to 10X faster than a typical MCU, TI DSPs give you more than extra bandwidth — they give you the increased performance, energy efficiency and ability to reduce your overall system costs. Add our third-party support, reprogrammability and broad portfolio of DSP Solutions based on our TMS320 DSP family, and TI DSPs give you a product road map to the future, today.

What's more, from our 800 number to our Web site to our DSP Starter Kit for only $149, TI is there. Giving you everything you need to meet your changing market. So contact us today because it's all right here. And it's yours for the taking.

Call ***1-800-477-8924, ext. 4091,*** *or visit us at*

www.ti.com/sc/4091

*100,000 quantity

D S P S O L U T I O N S

TEXAS INSTRUMENTS

We've Bred an Integrated Watchdog/Reset That Will Make Other CPU Supervisors Howl

Lower Cost

Introducing the DS1232LP Low Power MicroMonitor chip, an upgrade for the industry-standard DS1232 that fully integrates the watchdog and reset functions to operate together. Unlike other devices, this puppy doesn't put you through the hassle of wire ANDing or using gates to tie the watchdog and reset together. So your design job is easier.

And the DS1232LP collars the competition when it comes to power— a mere 50µA vs. 200+µA for other devices.

Lower Power

With the MicroMonitor's tolerance and time delay inputs, you can adjust voltage trip level and vary the timeout.

Best of all, we took a bite out of the price. The DS1232LP costs less than its predecessor, the industry-standard DS1232!

For more information, give us a bark at (972) 371-4448.

CPU Supervisor Family

Device	Reset Threshold	Active Low Reset	Active High Reset	Manual Reset	Watchdog	Secondary Sense Voltage	Package
DS1232LP	5V - 5% or 10%	✓	✓	✓	✓		8-pin DIP 8-pin SOIC
DS1705/6 DS1706x	5V - 5% or 10% 3.3V - 5%, 10% or 20%	✓ or	✓	✓	✓	✓	8-pin DIP 8-pin SOIC
DS1707/8 DS1708x	5V - 5% or 10% 3.3V - 5%, 10% or 20%	✓	✓	✓		✓	8-pin DIP 8-pin SOIC
DS1810-13 DS1815-18	5V - 5%, 10% or 15% 3.3V - 10% or 20%	✓ or	✓	✓*			SOT-23 TO-92
DS1832	3.3V - 10% or 20%	✓	✓	✓	✓		8-pin DIP 8-pin SOIC
DS1834	5V - 5% or 10% and 3.3V - 5%, 10% or 20%	✓ &	✓	✓			8-pin DIP 8-pin SOIC

*Optional

Looking for other functions? We've got a whole litter of devices to choose from.

DALLAS SEMICONDUCTOR

Visit our Web site at http://www.dalsemi.com/

4401 South Beltwood Parkway, Dallas, Texas 75244-3292 ❖ Phone: 972-371-4448 ❖ Fax: 972-371-3715

READER SERVICE 124

CMOS Data Converters Usher In High Performance At Low Cost

A 16-Bit ADC And A 14-Bit DAC Use Innovative Architectures And On-Chip DSP To Deliver Breakthrough Performance.

Lisa Maliniak

A growing trend over the past decade has been the switch from analog to digital signal-processing systems. The driving force behind this shift is the ability to implement sophisticated adaptive algorithms in the digital domain that would be virtually impossible to do with analog circuits. Furthermore, as the information age matures, it's increasingly clear that most of the information traffic is in the form of digital bits—although that information usually must be converted to analog form before it's of any use to the average person.

However, there are some fundamental stumbling blocks in this analog-to-digital migration proccess. As system designers seek to do more and more of the filtering, frequency translation, modulation, demodulation, and other processing tasks in the digital domain, the performance requirements on the data converters in terms of sampling rate, dynamic range, and analog bandwidth can become extreme.

Using innovative architectures and on-chip digital-signal processing (DSP), designers at Analog Devices have developed two high-performance data converters designed to meet the stringent demands of high-speed digital processing systems. The devices are a 16-bit analog-to-digital converter (ADC) and a 14-bit digital-to-analog converter (DAC).

The AD9260 16-bit, monolithic ADC achieves higher than 100 dB of spurious free dynamic range (SFDR) performance at input signals greater than 1 MHz. The second device, the AD9774, is an interpolating DAC that has SFDR performance of more than 75 dB out to and beyond 12.5-MHz output frequencies. Both data converters are targeted at the new generation of systems that will rely on increasingly sophisticated DSP approaches to extract information from a hostile, noisy environment *(see "Digital Echo Cancellation: Modems That Talk And Listen At The Same Time," p. 72).*

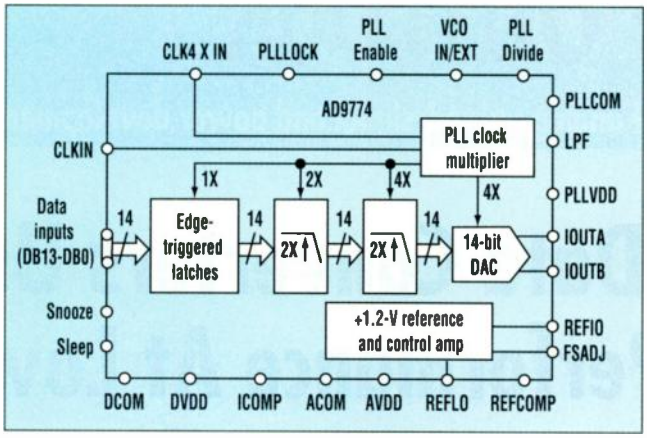
System Changes

To understand the changes that occur when moving from an analog to a largely digital system, consider the partitioning of a traditional signal-processing chain on the receiving end of signal transmission. The analog signal from an antenna or transducer is extensively processed in the analog domain. This typically includes filtering away unwanted interfering signals, applying gain to the desired signal, and translating down to a more easily processed frequency. After all of this signal conditioning is provided in the analog domain, the desired signal is delivered to an ADC of relatively low performance, and the digitized recovered signal is passed to the digital signal processor or microprocessor.

However, a system can be partitioned to shift most of the signal processing to the digital domain. As advances in digital VLSI technology have reduced the cost of high-speed digital processing, many system architects are looking to replace conventional hard-wired analog processing with more sophisticated, adaptive digital schemes. For the receive path, this means that the ADC moves up the signal chain, closer to the antenna or transducer. The interfering signal sup-

pression and other processing functions are now performed digitally, after analog-to-digital conversion.

As a result, the ADC must effectively capture not only the desired signal, but all of the interfering signals as well. These interferers must be digitized without corrupting the desired signal through aliasing. In other words, the sample rate of the converter must be higher than that of the traditional analog approach to avoid aliasing an interferer back onto the target signal.



2. The Analog Devices AD 9774 DAC integrates a complete, low-distortion, 14-bit CMOS DAC core with a 4↔ digital interpolation filter, a voltage reference, and 4↔ PLL clock multiplier.

In addition, amplitude corruption must also be avoided. The ADC needs sufficient dynamic range so that it doesn't clip the strongest interferer, and still has a low enough noise floor to recover the weakest desired signal. Low quantization noise is not enough—the converter must be sufficiently linear so that harmonics and intermodulation products from strong interferers will not mask weak target signals. The difference in performance requirements can be dramatic: a conventional AMPS base station receiver, for example, might require a six- to eight-bit ADC at a sample rate of 100 ksamples/s, while a digital-radio implementation would require a 14-bit, 65-msample/s converter with an SFDR of over 80 dB.

Unwanted Image Energy

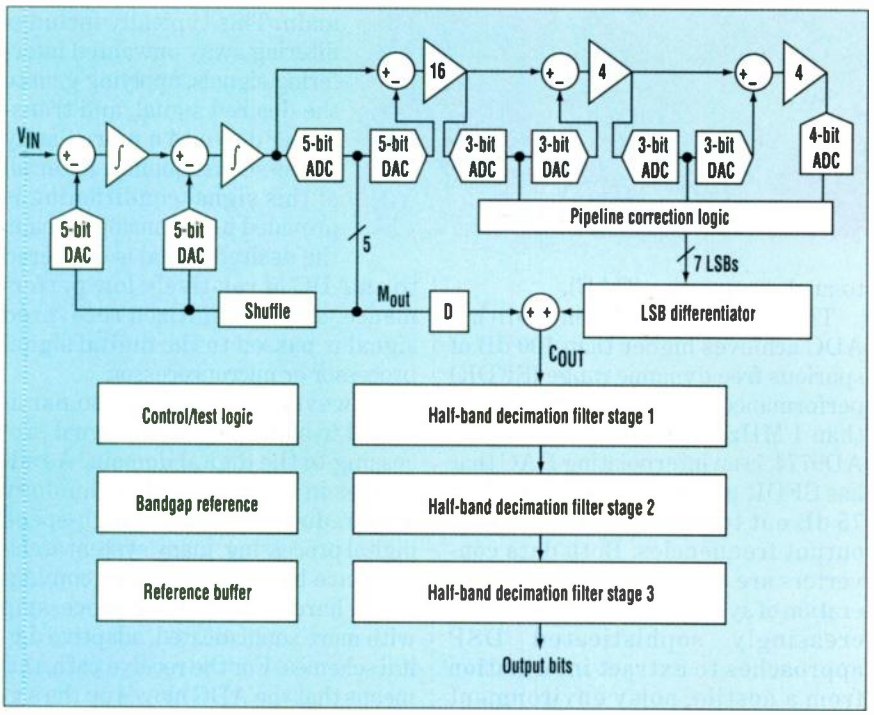
While DACs tend not to face the strong interferer problem, they typically produce unwanted image energy at their analog outputs. That in turn necessitate the use of extensive analog filtering before delivery of the signal to the transducer or antenna. Once again, the use of expensive analog signal-conditioning circuitry may be replaced with a lower-cost DSP approach, if a sufficiently linear, high-speed converter is available. For example, in many systems, the linearity of the power driver circuit may be the performance limiter. Some sophisticated systems will actually use complicated adaptive algorithms to predistort the signal in the digital domain to precompensate for the distortion of the power amplifier. Using these kinds of system tricks typically requires an extra 10 to 20 dB of dynamic range in the DAC.

16-Bit Monolithic ADC

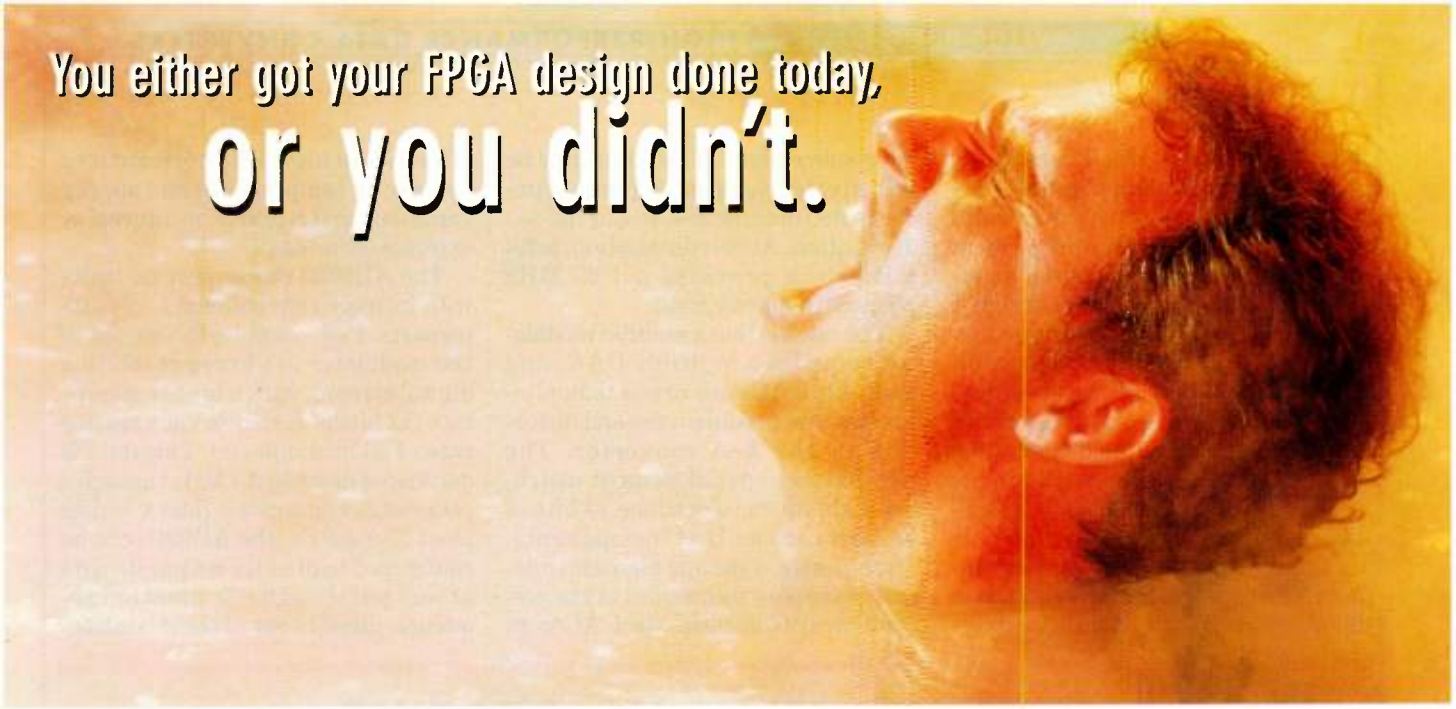
Analog Devices is introducing two monolithic converters that combine on-chip DSP and mixed-signal converter cells to provide the speed, dynamic range, and linearity required by emerging high-speed digital-processing systems. The company claims the 16-bit AD9260 ADC is the first monolithic converter to offer 1 MHz of effective Nyquist frequency bandwidth at greater than 14 effective bits. Performance specifications include total harmonic distortion (THD) of –96 dB, SFDR of 100 dB, and a signal-to-noise ratio (SNR) of 88.5 dB *(see the table)*. These specifications are achieved by converters that are made on a conventional low-power CMOS process.

The AD9260 is built with an innovative Σ–Δ-based architecture. These architectures have become very popular for high-dynamic-range ADCs in audio and other low-frequency industrial applications. Σ–Δ modulators allow quantization noise to be spectrally shaped, or pushed to frequencies outside the signal band where it can be attenuated by digital filters. This suppression of quantization noise allows fundamentally linear one-bit DACs to be used in the ADC's feedback loop, thereby avoiding the trim or calibration that's normally required for a converter with greater than 10- or 12-bit resolution.

Unfortunately, a single-bit modulator generates so much quantization noise that a large (32-to-64↔) oversampling ratio is typically required to get to 16-bit or higher performance. While



1. The Analog Devices AD9260 ADC uses a cascaded Σ–Δ pipeline. The on-board three-stage digital decimation filter reduces front-end antialias filtering requirements.



New FPGAs will land you in hot water if you're not prepared.

Only VeriBest DESTINATION FPGA™ delivers vendor-specific, mixed schematic/HDL design today that's fully scaleable to tomorrow.

DESTINATION FPGA enables you to make the transition to higher density FPGAs... with no limitations on how far you can go. In one easy-to-learn and use solution, you get high-performance desktop HDL design at a low, introductory price of just $4,995.

Design support for up to 100K gates market-ready in absolutely the fastest way possible!

Here is a cost-effective, vendor-specific solution, optimized to harness the performance of emerging FPGAs. DESTINATION FPGA establishes a high-density design standard that gets the job done faster and with greater confidence than ever before. And there is no risk, with six months of free support and a 30-day money-back offer.

VERIBEST DESTINATION FPGA
THE AWARD-WINNING VERIBEST DESIGN SYSTEM PLUS SYNOPSYS FPGA EXPRESS

SUPPORTS WINDOWS 95® AND WINDOWS NT®

ALL THIS FOR JUST $4995!

Hey! Keep up with the hardware technology or someone else will.

Check it out at www.destinationfpga.com.

Call 1.888.482.3322 and get movin'!

VERIBEST
INCORPORATED

READER SERVICE 204

FASTEST PROCESS GETS AHEAD!™

a 10-MHz master clock is reasonably painless for an audio application, 64↔ oversampling on a 1-MHz bandwidth would require a modulator to run at over 128 msamples/s—hardly an attractive option for a system designer wishing to attain 100 dB performance.

The AD9260 combines a multibit modulator with a 12-bit pipelined ADC to produce a Σ–Δ modulator with only 12 bits of effective quantization noise *(Fig. 1)*. This device allows the in-band quantization noise to be suppressed to the 16-bit level, with only an 8↔ oversampling ratio. The onboard three-stage digital decimation filter reduces front-end antialias filtering requirements. This filter may be selectively bypassed to provide undecimated data, or 2↔, 4↔, or full 8↔ decimation. At 8↔ decimation, a 20-MHz clock provides a 1.25-MHz Nyquist frequency band.

The catch is that a multibit modulator requires a multibit DAC, and multi-bit DACs are prone to nonlinearities that produce noise and distortion in the Σ–Δ converter. The AD9260 uses special element-matching techniques to produce 14 bits of linearity in the DAC components. Then it uses dynamic element-mismatch shaping techniques in the element array to linearize the DAC to an effective 16 bits. This performance holds over temperature and supply variations, and requires no internal or external calibration.

The AD9260 shares certain traits with its more conventional Σ–Δ counterparts. For example, the output of the modulator is a lower-resolution digital stream, with a higher sample rate (12 bits of resolution at a smaple rate of 20 msamples/s). This data is decimated down to 2.5 MHz through a series of 2↔ decimation filters. Unlike most Σ–Δ ADCs, the AD9260 can be configured to directly output its data at any point in the decimation sequence: directly out of the modulator

DIGITAL ECHO CANCELLATION: MODEMS THAT TALK AND LISTEN AT THE SAME TIME

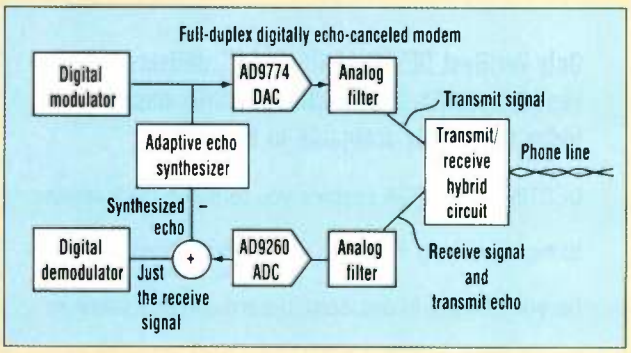
One of the more interesting next-generation system innovations is the digitally echo-cancelled modem. Most modem functions require bidirectional communication, which can be achieved in a variety of ways. The simplest is half-duplex, where the modem alternates between the transmit and receive mode. At any point, information is only flowing in one direction on the wire.

More sophisticated systems may use frequency division multiplexing (FDM). In this kind of system, information traveling in one direction is confined to lower frequencies, while information traveling in the other direction must stay in higher frequencies. The information is separated through the use of appropriate filters. This technique allows for simultaneous transmit and receive, but reduces the available bandwidth in each direction. In fact, because there are always filter transitions, some of the total bandwidth is lost and virtually unusable, creating a less-than-optimal use of the channel capacity.

The ultimate modem should be able to simultaneously transmit and receive over the same frequency space. Is this possible? It is possible with a full-duplex digitally echo-cancelled modem *(see the figure)*.

A signal is digitally modulated, then put through a DAC on the transmit path. The transmitted signal is placed on the telephone line through the hybrid circuit, which attempts to drive the transmit signal and sense the receive signal. The hybrid presents the received signal to the receive ADC, rejecting the transmit signal. Unfortunately, impedance variations in the line keep the hybrid from perfectly rejecting the transmit signal. The receive path actually sees the receive signal plus an image of the transmit signal. This image is called the near-end echo. For long lines, this near-end echo may be 40-50 dB stronger than the desired receive signal.

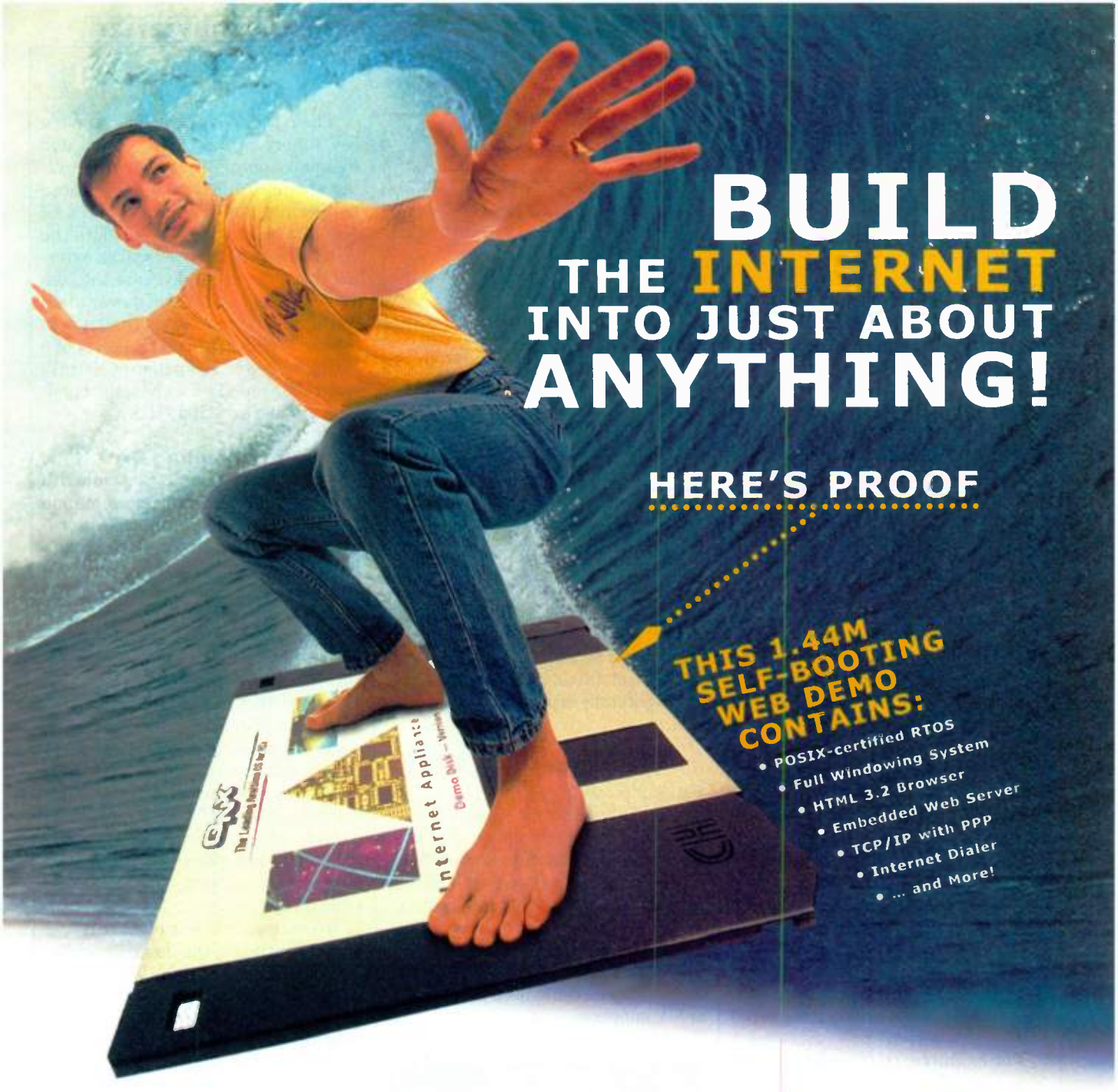
Because the transmit signal is known, it's possible to synthesize a digital representation of this echo. The actual



shape and phase of the echo is a strong function of the line impedance, which can vary from one line to the next, and even change with temperature. Typically, the echo synthesizer must be adaptive.

The synthesized echo can then be subtracted from the digitized signal, leaving only the receive signal to be presented to the digital demodulator. Of course, to make this possible, the DAC must cleanly synthesize the desired signal. In fact, high-resolution (i.e. 14+ bits), oversampled DACs, such as the AD9774, may be required to minimize the effects of quantization noise. In addition, the ADC must have sufficient dynamic range to capture the strong echo and the weak receive signal without clipping the echo (which would cause distortion and ruin the signal), or without losing the weak receive signal in the converter's quantization noise. Depending on the modem application, this requires anywhere from 5 kHz to 1 MHz of bandwidth and up to 90 dB of dynamic range. This type of modem is one of the most popular applications for the AD9260 ADC.

Contributed by Dave Robertson, staff design engineer in Analog Devices' high-speed converter group.



The Internet Appliance Toolkit (IAT) includes:

- everything on the demo, plus
- visual application builder
- built-in internationalization
- Watcom C/C++ compilers
- drivers for hundreds of PC peripherals
- embedded filesystems
- demo apps with source files
- scalable fonts
- embedded OEM pricing
- ... and much more!

Build the Internet into smart phones, set-top boxes, photocopiers, kiosks, printers, PLCs ... anything!

Better yet, build it on time. The IAT™, used to create this demo, comes with everything you need, from rapid application development tools to Internet apps to source code. Build a custom browser in days, not months!

And talk about performance. With the IAT and QNX you can use low-cost x86 platforms to deliver incredible speed and reliability. Believe it!

Download your free 1.44M demo today!

www.qnx.com/iat

or call:

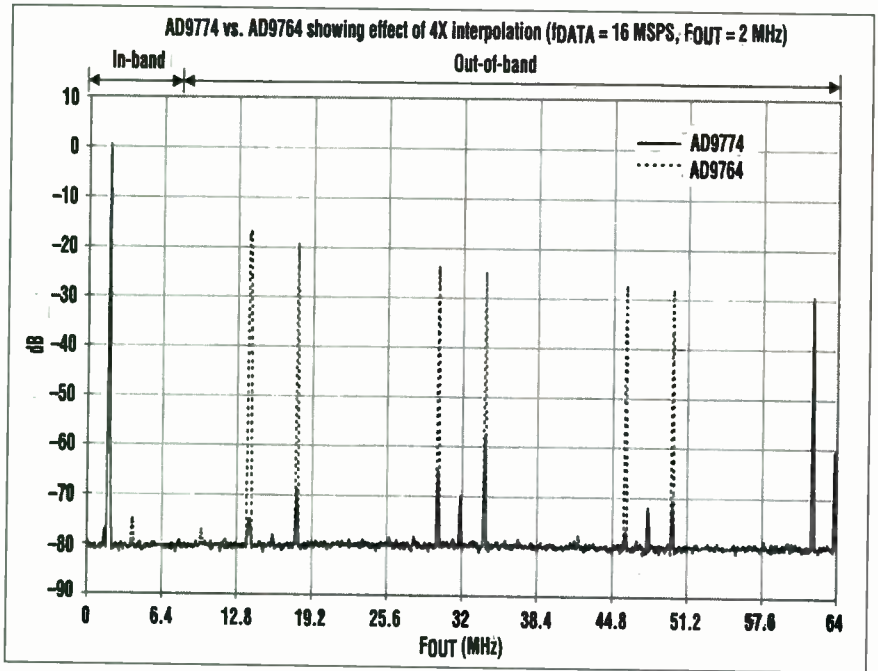
800 676-0566 (ext. 2261)

QNX®

The Leading Realtime OS for PCs

QNX Software Systems Ltd., 175 Terrence Matthews Crescent, Kanata, Ontario, Canada K2M 1W8 Voice: 613 591-0931 Fax: 613 591-3579 **Europe:** 49 Dove Park, Chorleywood, Hertfordshire, WD3 5NP Voice: (44)(0)1923 284800 Fax: (44)(0)1923 285868

READER SERVICE 181



3. Comparing the output spectrums of the Analog Devices AD9774 and AD9764 DACs clearly illustrates the benefits of interpolation. This plot superimposes the AD9774 interpolating DAC's 2-MHz output signal on an uninterpolated DAC's output. The out-of-band images are suppressed as expected, but even the in-band SFDR is significantly improved. SFDR is improved to greater than 80 dB.

in the form of 12 bits at 20 msamples/s; or 16 bits at 10 msamples/s, 5 msamples/s, or 2.5 msamples/s out of the various decimator stages.

Of course, a high-performance converter is of relatively little use if it can't be effectively integrated into a high-speed processing system. The AD9260 has several features designed to enhance its usefulness and flexibility. Wherever practical, support functions have been integrated onto the converter.

For example, the bandgap reference and reference buffer have been integrated onto the converter. This integration is important because improperly controlled impedance levels at the reference inputs to high-speed converters may turn out to be the limiting factor in distortion performance.

The analog input has been configured for a differential input, with a 4-V p-p differential span. It features excellent common-mode rejection out to frequencies above 10 MHz, providing the best possible chance to reject board and system noise at the input to the converter. The 8↔ oversampling of the AD9260 simplifies the antialiasing filtering requirements of the converter, because the first serious alias band is above 18 MHz when clocked at 20 msamples/s.

The digital interface is also configured for flexibility and ease of use. Read and Chip Select pins allow flexible interfacing. A Data Available pin provides an appropriate latching signal to latch the output data, regardless of which decimation ratio is being used. Furthermore, the digital power supply may be configured for either 3- or 5-V supplies.

AD9260 ADC PERFORMANCE SUMMARY

Resolution	16 bits
Sample rate	20 MHz
Oversampling rate	8X
Input noise	0.68 LSB rms
Signal-to-noise ratio	88.5 dB
Total harmonic distortion (100 kHz)	-96 dB
Spurious-free dynamic range (100 kHz)	100 dB
IM3 (975 kHz, 1 MHz, -9 dB)	-95 dBc
Power dissipation	585 mW
Power supplies	5-V analog, 3-V digital
Process	0.6-µm double-polysilicon double-metal CMOS

The AD9260 requires just a single 5-V supply for its analog voltage, and dissipates only 585 mW when operating at a full 20-MHz clock. For those requiring less than 1.2 MHz of Nyquist bandwidth, the clock to the AD9260 may be reduced and an external resistor used to decrease the converter's bias current and power dissipation. This power reduction is essentially linear down to a clock of 5 MHz and power dissipation of 150 mW (providing an effective Nyquist bandwidth of just over 200 kHz).

14-Bit Interpolating DAC

DACs don't have to contend with the strong-interferer phenomenon that drives the dynamic range requirements on ADCs. But they do have a series of their own unique problems. In the circuit world, the DAC problem has typically been considered easier than an ADC. In the high-speed signal-processing domain, however, this rule of thumb proves to be faulty. One important reason is that the ADC sample-and-hold amplifier (SHA), generally the most critical component for distortion performance, need only be accurate at the instant the input sample is taken. If the SHA slews or distorts while acquiring the input signal, it does not affect performance as long as this has settled by the sampling instant.

In contrast, when using a DAC for signal synthesis, the linearity of the output throughout the clock cycle contributes equally to the distortion performance. This situation has created an interesting phenomenon—it's easier to find an ADC that can sample (or even undersample) a 10-MHz analog input with 75-dB SFDR, than it is to find a DAC that can synthesize a 10-MHz signal with 75-dB SFDR. The reconstruction filters required after most DACs further contribute to distortion and phase nonlinearity. The AD9774 converter integrates digital interpolation filters with a highly linear CMOS DAC to provide effective solutions to both problems. Analog Devices claims that the AD9774 is the first DAC to achieve SFDR greater than 76 dB for output signals up to 13 MHz.

The AD 9774 integrates a complete, low-distortion, 14-bit CMOS DAC core with a 4↔ digital interpolation fil-

BORN. TO BE WILD.

Announcing the birth of DSP16210, the most significant Digital Signal Processor to hit the communications market since we invented the first DSP.

Conceived by Bell Labs specifically for next-generation communications applications, DSP16210's more efficient processing lets it effortlessly handle a variety of functions in any digital wireless standard, using up to five times less power and memory than the most advanced DSP on the market today.

Proven software tools and high-performance processing enable DSP16210 to radically reduce development time and system costs, making it the perfect DSP for rack modems and smaller remote base stations that can be deployed anywhere you can imagine with a savings of up to 50% in electronics costs. To learn more about how the DSP that was designed from the start to be the soul of communications can help you create products beyond your wildest dreams, call 1-800-372-2447 (Ext. 955). Or visit www.lucent.com/micro

READER SERVICE 154

ter, a voltage reference, and 4↔ phase-locked loop (PLL) clock multiplier *(Fig. 2)*. The two-stage 4↔ digital interpolation filter helps improve passband distortion by allowing the system designer to use less-expensive, less-complex analog reconstruction filters with poles placed further away from the critical signal passband.

Data can be input at rates up to 32 MHz. The AD9774 generates three interpolated data words in between each input data word, updating the DAC core at 4↔ the input data rate (128 MHz for a 32-MHz input word rate). A PLL clock multiplier is integrated onto the AD9774 so that users needn't produce the higher clock rate.

The benefits of interpolation are clearly visible by comparing the output spectrums of both the AD9774 DAC and a noninterpolating DAC *(Fig. 3)*. The output spectrum of the AD9774 DAC synthesizing a 2-MHz output signal superimposed on an noninterpolated DAC's output shows the out-of-band images are suppressed as expected, but even the in-band SFDR is significantly improved. The SFDR is improved to greater than 80 dB *(Fig 3, again)*. The AD9774 is designed for flexibility, making it suitable for use across a wide range of frequencies and applications. It can run on either 3- or 5-V supplies, or a 3-V digital and 5-V analog supply.

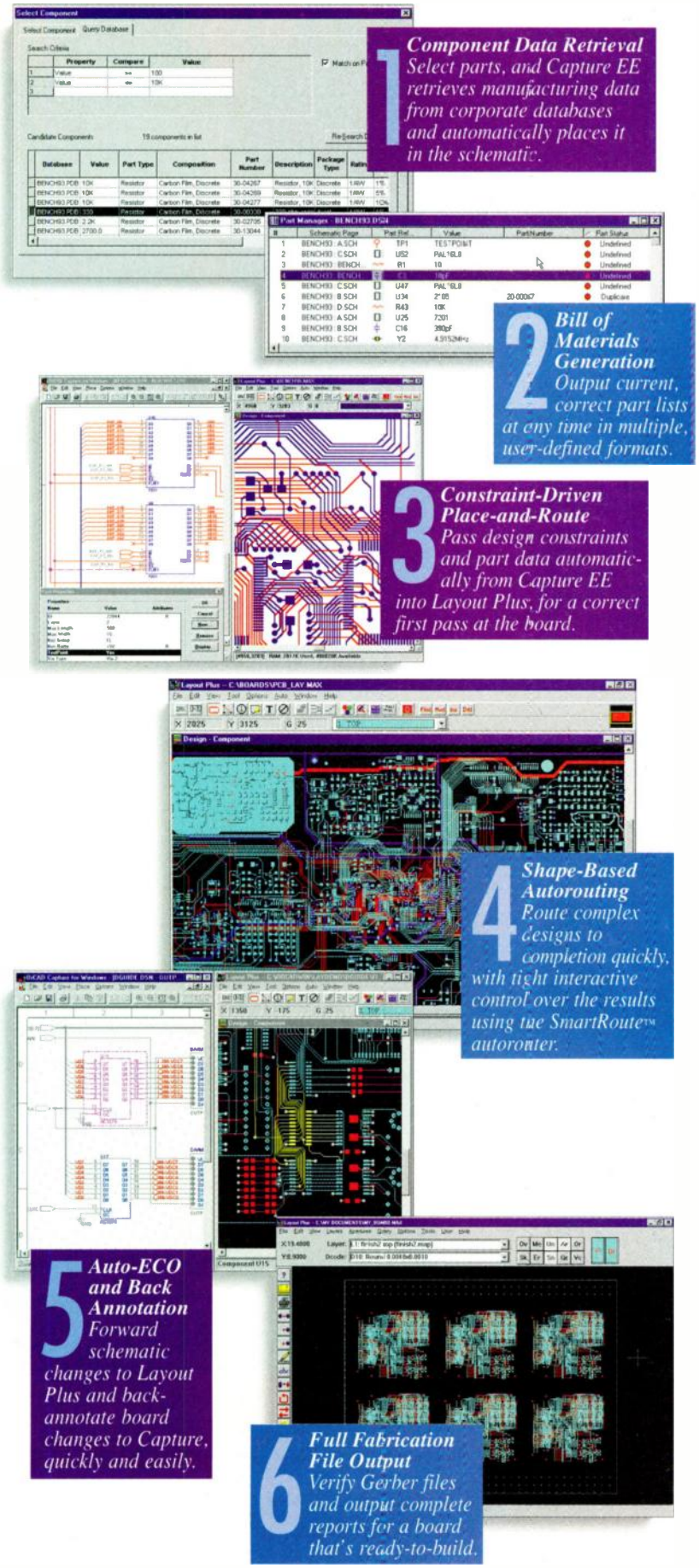
Differential current outputs can be used either single-ended or differentially, and can even directly drive a ground-referenced transformer. The PLL clock multiplier operates over a wide frequency range, supporting input frequencies from below 1 msamples/s up to 32 msamples/s. The AD9774 also features an on-chip reference and a power-down sleep mode that drops the part's power dissipation to 25 mW on a 3-V supply.

Price And Availability

The AD9260 ADC comes housed in a 44-pin MQFP surface-mount package, and costs $39.90 each in 1000-unit quantities (price valid at press time). The AD9774 DAC also is available in a 44-pin MQFP package, and is priced at $24.95 each in 1000-unit quantities. Both devices are specified over the -40 to +85°C industrial temperature range.

Analog Devices Inc., Ray Stata Technology Center, 804 Woburn St., Wilmington, MA 01887; (781) 937-1428, www.analog.com.

CIRCLE 531



What's The Fastest Track To A Finished Board?

OrCAD Capture *EE*™ and OrCAD Layout Plus® for Windows NT®.

With OrCAD's new solution for PCB design you'll save time, reduce re-work and have a ready-to-build board faster.

You can select from pre-approved parts easily and generate complete bills of materials that include manufacturing data. Tight integration between schematic and board layout lets you drive the design from the schematic and update engineering changes automatically. You'll start with the right information, minimize component errors, eliminate unnecessary design turns and get your board out the door faster.

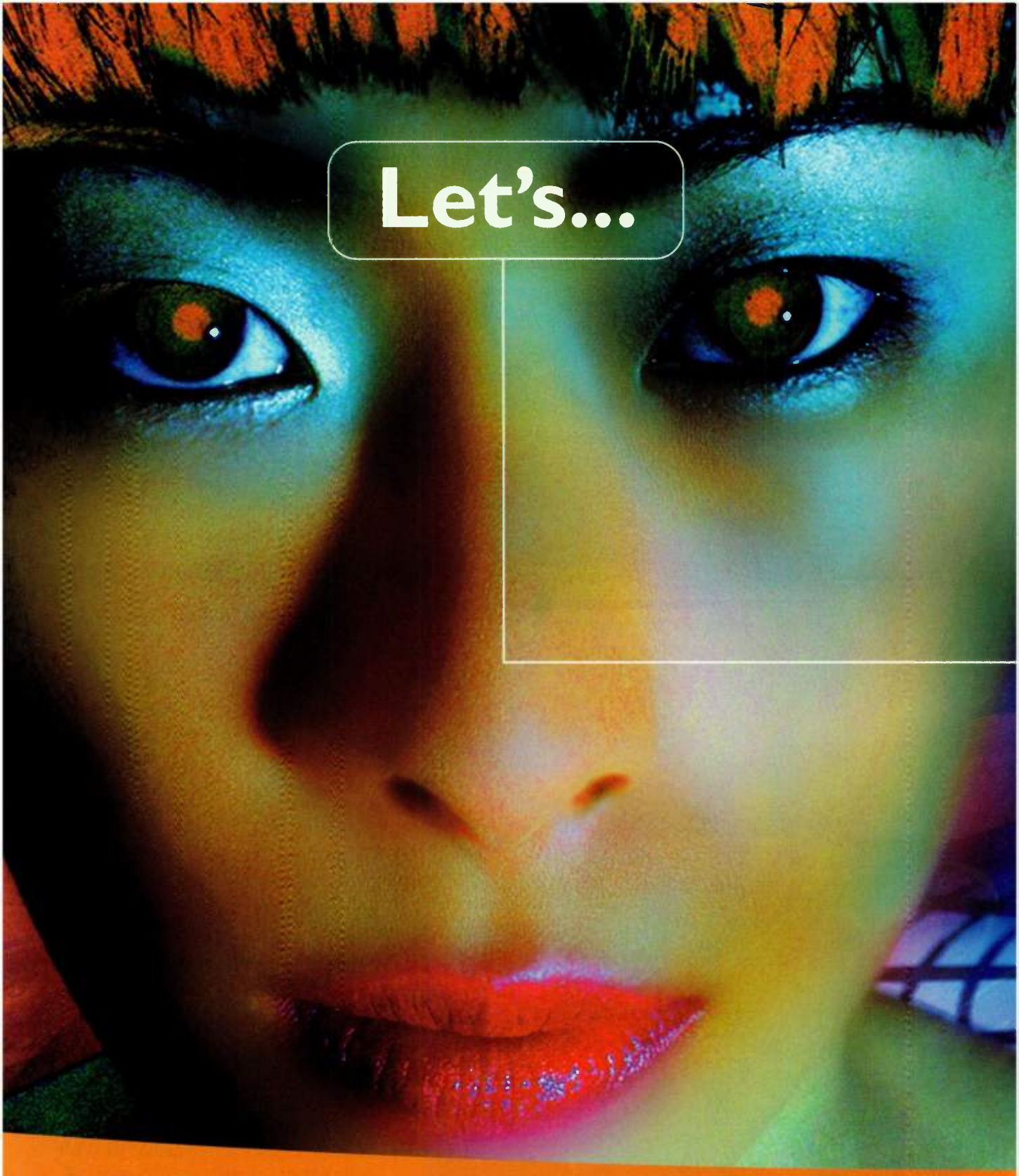
Get on the fast track to board design. Call for a free demo CD. Visit our website at www.orcad.com or call OrCAD DIRECT at 1-800-671-9506.

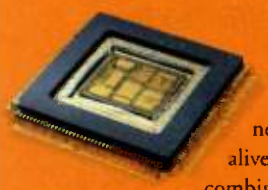
OrCAD®

Bringing Electronic Design to the Desktop

READER SERVICE 175

WRH





Who's putting tomorrow together?

People with vision, who can take today's PC and expand it with a world of new possibilities. People whose minds are alive to the true potential of multimedia, combining video communication, interactive television, digital sound and more into a single package. If that's the race your imagination's running, we're rightalongside you.

Because at **Philips Semiconductors** we're setting the pace with dedicated solutions for desk-top video processing and video conferencing systems, we're pioneering the latest advances in optical technologies like DVD, and offering a vast array of digital audio processing ICs. And we're first with USB and IEEE1394 silicon - providing hot plug and play for all your peripherals.

We also offer leading edge videographics for PC applications, integrated solutions for mobile computing, monitors, cameras and speakers. And

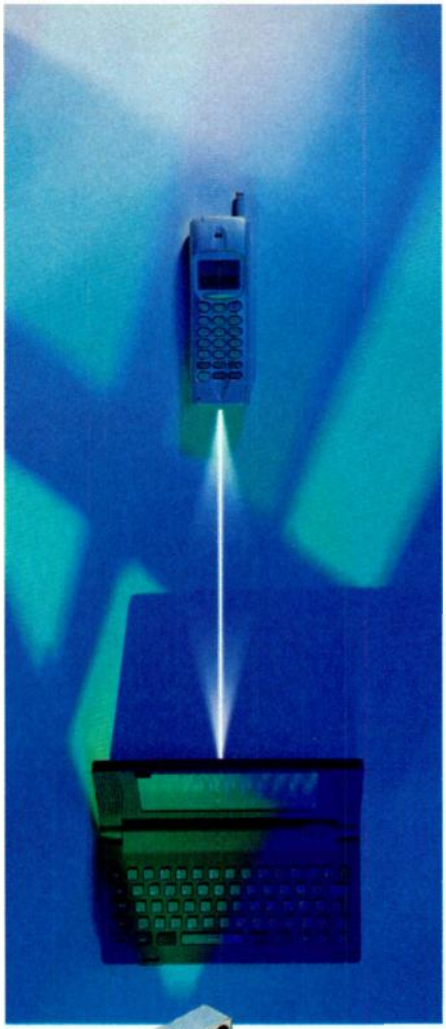
smartcard solutions including today's most advanced cryptocontrollers, for secure payment and access to services. Almost more possibilities than you can imagine. Run with them and who knows how far you can go. See the future today at www.semiconductors.philips.com and finally make PCs into a true multimedia tool.

USA tel. +1-800-447-1500, ext.1317. Europe fax. +31-10-284-3181, quote "pc". Asia fax. +852-2811-9173, quote "ED".

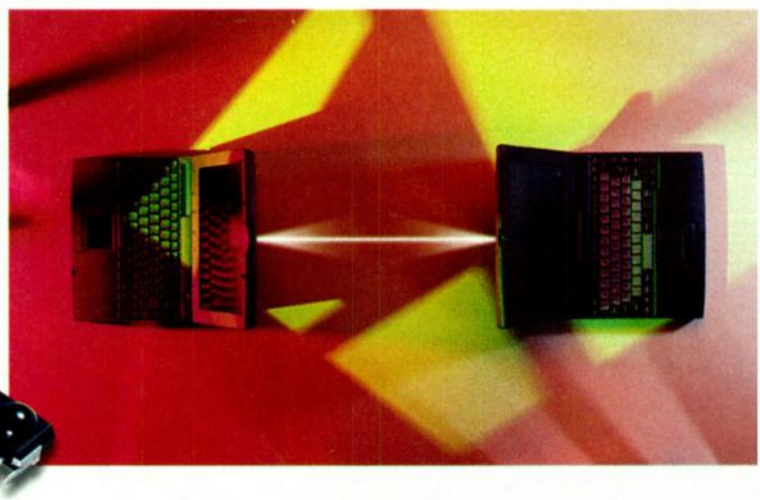
READER SERVICE 209

PHILIPS

Let's make things better.



Save space, save power– with IrDA link modules from NEC



Infrared data transfer has become an essential feature of portable information products. The most efficient way to incorporate this function in your system is to specify space- and power-saving transceiver modules from NEC. We offer two types, both of which conform to Infrared Data Association (IrDA) standards.

Our NL1100 transceiver module conforms to IrDA ver. 1.0 and 1.1. It provides reliable transmission at data rates from 2.4kbps to 4.0Mbps over distances up to 1m. Our module features low LED drive current: 300mA at 1m. Measuring only 6.9 x 13.2 x 6.5mm, the sturdy molded package shuts out ambient light and permits IR reflow soldering (twice). We also offer an optional shield case. The NL1100 is ideal for notebook PCs, digital still cameras and printers.

We'll soon introduce our NL1000 transceiver module that conforms to IrDA ver. 1.0. It transfers data at rates from 2.4kbps to 115.2kbps over distances up to 1m. The NL1000 features low operating voltage and current: 3.3V and 130µA. It comes in a shield case measuring only 3.8 x 9.6 x 4.0mm and permits IR reflow soldering (three times). The NL1000 is an optimum solution for PDAs, pagers, cellular phones and handy terminals.

Decreasing size, weight and power consumption while improving functionality are the keys to success in portable information products. For more information on how our new IrDA link modules meet these goals, contact NEC today.

MEMBER IrDA

Infrared Data Association

just imagine

NEC MULTIMEDIA

NEC

For fast answers, call us at: USA California Eastern Laboratories Tel:1-408-988-3500.Fax:1-408-988-0279. GERMANY Tel:0211-650302. Fax:0211-6503490. THE NETHERLANDS Tel:040-445-845.Fax:040-444-580. SWEDEN Tel:08-638-0820.Fax:08-638-0388. FRANCE Tel:1-3067-5800. Fax:1-3067-5899. SPAIN Tel:1-504-2787.Fax:1-504-2860. ITALY Tel:02-667541.Fax:02-66754299. UK Tel:1908-691133.Fax:1908-670290. HONG KONG Tel:2886-9318.Fax:2886-9022. TAIWAN Tel:02-719-2377.Fax:02-719-5951. KOREA Tel:02-551-0450.Fax:02-551-0451. SINGAPORE Tel:253-8311.Fax:250-3583. AUSTRALIA Tel:03-8878012.Fax:03-8878014. JAPAN Tel:03-3454-1111.Fax:03-3798-6059.
On the Internet at http://www.ic.nec.co.jp/index_e.html

READER SERVICE 171

High Integration Simplifies Signal Processing For CCDs

CMOS ICs Offer Complete Analog Signal Processing For CCD Imaging To Lower Overall Cost, Power Consumption, And Size.

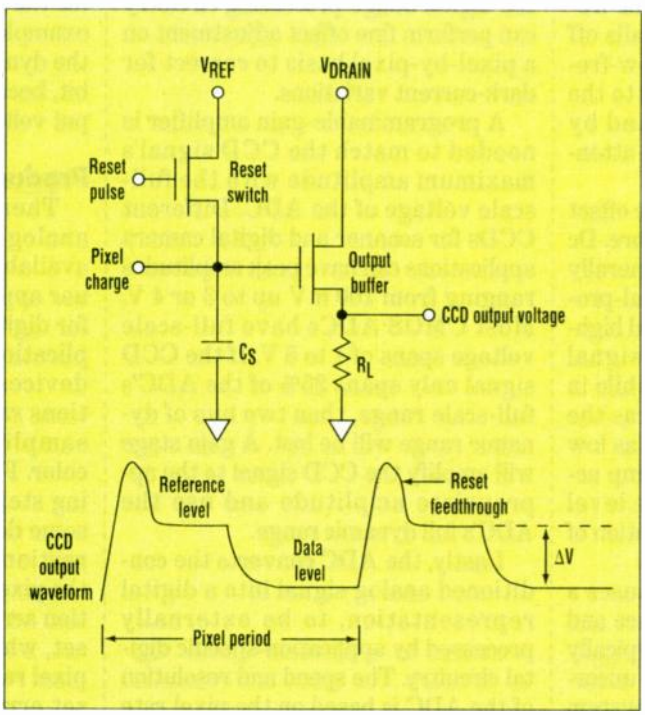
ERIK BARNES, Analog Devices Inc., 804 Woburn St., Wilmington, MA 01887; (781) 937-1428; fax (781) 821-4273.

The charge-coupled device (CCD) is the image sensor of choice for most consumer-oriented imaging applications. Traditionally, the device's unique analog signal-processing chain has been implemented using standard linear components—op-amps, analog-to-digital and digital-to-analog converters (ADCs and DACs, respectively), analog multipliers, and analog switches. Recent advances in semiconductor design and technology have allowed a number of companies to introduce a single integrated circuit (IC) to handle all of the signal-processing steps required, from the CCD output right through the analog-to-digital conversion. The devices retain the performance of traditional designs, yet provide substantial savings in cost, power, and size. Before taking full advantage of these devices however, it is important to fully understand what they can and cannot do.

The markets for scanners, digital still cameras (DSC), and camcorders have become extremely competitive. In all three, prices are falling as the imaging companies compete for market share. Typically, consumers demand that each new generation of products offer higher performance for the same price as previous models, or at least give comparable performance at a lower cost. With cameras in particular, smaller size and longer battery life are key selling points.

For semiconductor manufacturers, this means that the 8-bit ADC that was adequate for low-end scanners in the past, is now being replaced by a 10-bit converter. With camcorder and DSC applications moving to higher-resolution CCD arrays with higher pixel rates, these same manufacturers must produce the analog processing circuitry required to operate at the higher sampling rates needed to maintain proper readout times and frame rates.

Semiconductor companies are now offering integrated solutions for CCD signal processing that combine all of the necessary front-end analog circuitry. Although this yields an obvious reduction in size and potential cost savings, high integration alone will not help designers meet all of the consumer's requirements. To help the designer more effectively address all of their needs, these devices are being implemented using low-cost, low-power, standard CMOS processes. This approach is possible because semiconductor companies have improved their capabilities in CMOS analog circuitry, eliminating the need for proven, but costlier BiCMOS and bipolar implementations. The remaining challenge for the semiconductor companies is to achieve the performance level required for the different imaging applications.



1. The CCD output stage converts each pixel charge to a voltage level at the sense capacitor, C_S. The voltage on C_S is reset before each pixel to the reference level, causing the reset-feedthrough glitch to occur. The amount of light sensed by each pixel is measured by the difference between the reference and data levels.

Processing The Signal

To understand what the integrated signal processing components have to offer, consider the typical CCD output waveform *(Fig. 1)*. One period of this signal consists of a reset feedthrough level, a reference level, and a data level. The voltage difference between the reference and the data levels contains the light information for an individual pixel. To accurately process and digitize the CCD signal, the integrated signal processing components perform several basic operations. These are: correlated double sampling (CDS), dc restoration (clamping), gain, offset, and analog-to-digital conversion.

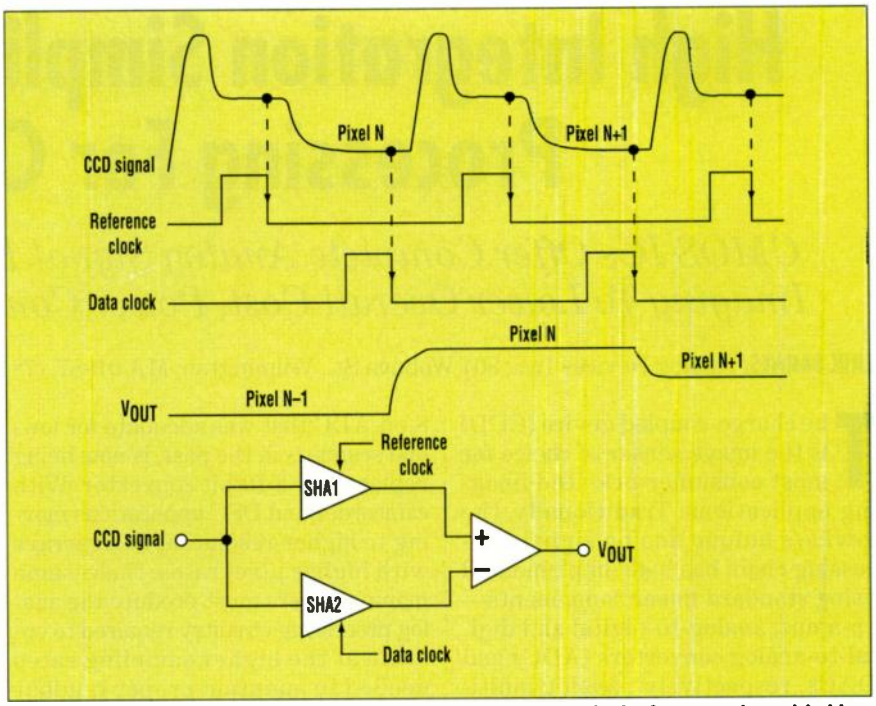
CDS is one of the most important steps in processing the CCD waveform. The operation serves two important purposes: it calculates the difference between the

reference and data levels of the CCD signal, and it reduces some of the noise components in the CCD signal. Conceptually, the CDS is a differential-in-time amplifier, because it takes two separate samples of the input signal and outputs the difference between them *(Fig. 2)*. There are varied topologies being used to perform this operation.

By taking two samples of the CCD signal and subtracting them, any noise source that is correlated between the two samples will be removed. Furthermore, a noise source that is not correlated, but is slowly varying between the two samples, will be reduced in magnitude. Noise introduced in the output stage of the CCD shown in Figure 1 consists primarily of kT/C noise from the charge-sensing node, and 1/f and white noise from the output amplifier. The kT/C noise from the reset switch's ON-resistance is sampled on the sense node, where it remains until the next pixel. It will be present during both the reference and data levels, so it is correlated within one pixel period, and will be removed by the CDS. The CDS will also attenuate the 1/f noise from the output amplifier because the frequency response of the CDS falls off with decreasing frequency. Low-frequency noise introduced prior to the CDS from power supplies and by temperature drifts will also be attenuated by the CDS.

A typical CCD signal has a dc offset of anywhere from 3 to 9 V or more. Dc offsets of this magnitude are generally incompatible with CMOS signal-processing ICs. In most scanner and high-end camera systems, the signal processors use 5-V supplies, while in camcorders and digital cameras the signal processors use supplies as low as 2.7 V. An on-chip input clamp accomplishes the necessary dc level shift, and only requires the addition of an external coupling capacitor.

The CCD's dark current causes a difference between the reference and data levels of the CCD signal, typically ranging from 10 to 80 mV. If left uncorrected, this offset will reduce system dynamic range, particularly after gain is applied. The signal-processing component applies analog offset adjustment to correct the average level of the offset, thereby retaining the dynamic range. With the majority of the offset removed in the analog domain, the digital image-processing circuitry can perform fine offset adjustment on a pixel-by-pixel basis to correct for dark-current variations.



2. The CDS samples the CCD signal twice during each pixel period. The first sample-and-hold amplifier (SHA1) samples the reference level, and the second sample-and-hold amplifier (SHA2) samples the data level. The difference amplifier subtracts the two samples, giving a measure of the light intensity and reducing noise.

A programmable-gain amplifier is needed to match the CCD signal's maximum amplitude with the full-scale voltage of the ADC. Different CCDs for scanner and digital camera applications can have peak amplitudes ranging from 100 mV up to 3 or 4 V. Most CMOS ADCs have full-scale voltage spans of 1 to 5 V. If the CCD signal only spans 25% of the ADC's full-scale range, then two bits of dynamic range will be lost. A gain stage will amplify the CCD signal to the appropriate amplitude and use the ADC's full dynamic range.

Lastly, the ADC converts the conditioned analog signal into a digital representation, to be externally processed by application-specific digital circuitry. The speed and resolution of the ADC is based on the pixel rate and resolution of the application. A CCD with a maximum dynamic range of 55 to 60 dB would require at least a 10-bit ADC, while one with a dynamic range of 65 to 70 dB would require at least a 12-bit ADC. Additional resolution may be needed to allow headroom for the digital image processing. For example, 6 dB of digital gain reduces the dynamic range of the ADC by one bit, because only half of the ADC's input voltage range can be used.

Product Variations

There are two general types of analog front-end (AFE) products available—those targeted for scanner applications and those targeted for digital camera and camcorder applications. For the scanner market, devices are available with resolutions ranging from 8 to 12 bits, and sampling rates of 1 to 4 MHz per color. Features include the processing steps listed earlier. In addition, some devices may offer shading correction, which changes the gain at the pixel rate to correct lens attenuation across a scanned line; digital offset, which changes the offset at the pixel rate to correct for odd/even offset errors and fixed-pattern offset variations; programmable threshold detectors, for scanning black-and-white only documents; and programmable timing generators, which allow the user to program the linear

Turning your power system into a competitive advantage.

Performance

Flexibility

Reliability

Economy

2nd Generation

Advanced power semiconductor packaging and thermal management provide high power density with low temperature gradients, while extensive use of silicon integration results in 1/3 the part count of a first generation converter. Wide ranges of input and output voltages and multiple mounting options will offer the design engineer the flexibility required in contemporary electronic systems.

800-735-6200 • www.vicr.com

VICOR

Component Solutions For Your Power System

23 Frontage Road Andover, MA 01810 / Tel: 978-470-2900 • Fax: 978-475-6715

READER SERVICE 205

CCD timing signals and the CDS sampling clocks. Other operating modes are sometimes included which allow the parts to process the outputs of contact image sensors (CISs) in addition to CCDs.

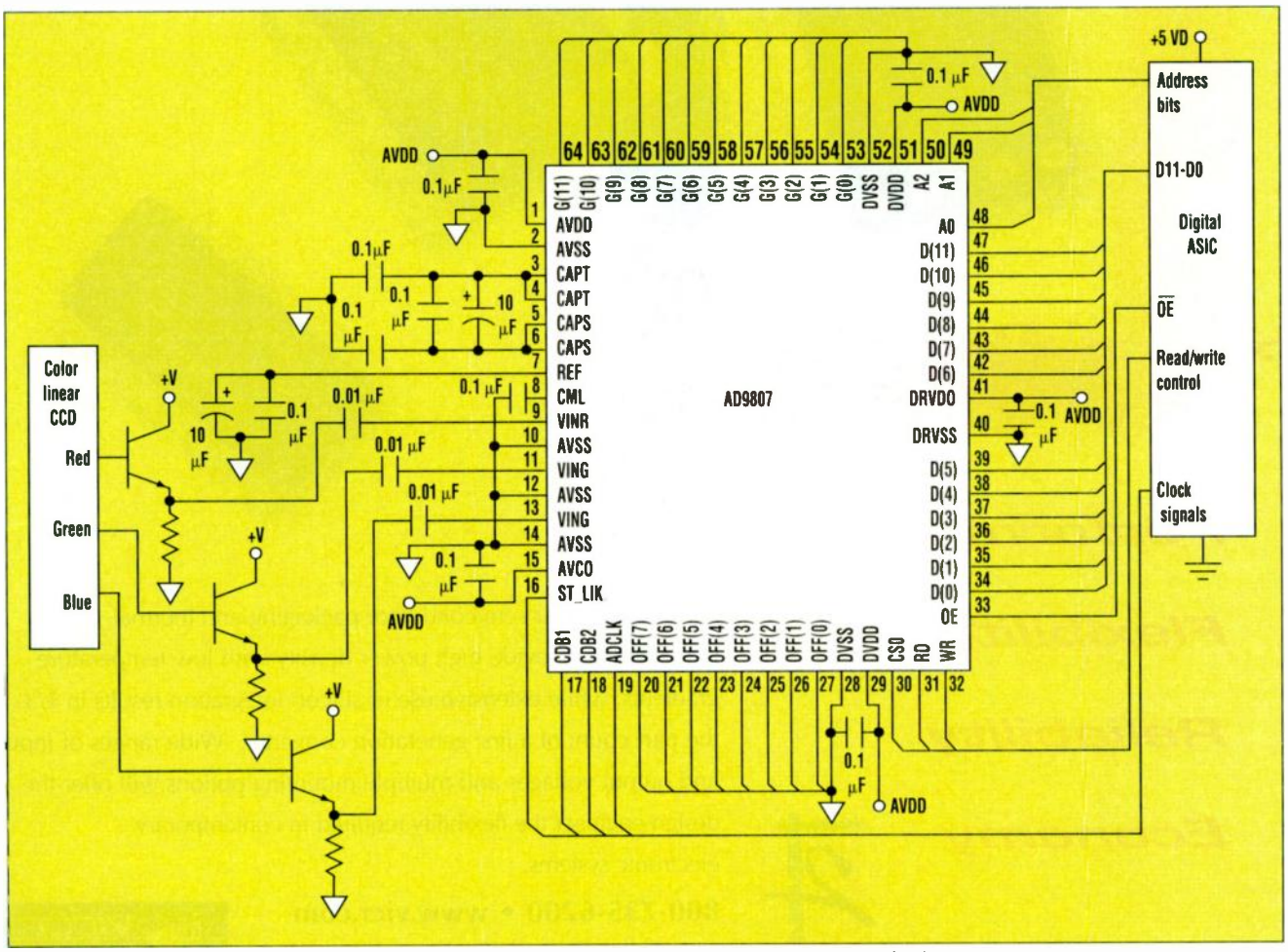
Scanners use color linear sensors, which have three CCD outputs representing the red, green, and blue information. Depending on the CCD used, the amplitudes of each color will be different due to differences in the spectral responsivity of each color. A separate programmable-gain-amplifier (PGA) stage will be needed for each color, so that the amplitudes may be individually adjusted to match the ADC's input range.

AFE products intended for digital camera and camcorder applications offer 8- to 10-bit resolution, and emphasize lower power (with 3-V supplies) and higher sampling rates (>10 MHz). A single-channel architecture is sufficient to interface with the output of an area-array CCD. The input ranges are smaller than the scanner products, to accommodate the lower output voltages of area CCDs. The programmable gain ranges are larger in order to be compatible with the wide range of lighting conditions in which a camera will be used (a scanner operates under more-controlled lighting conditions). The offset correction is implemented with an on-chip closed-looped configuration to correct the average offset of each line from the CCD in real time. This is different than the linear CCD approach, in which the individual pixel offsets are calibrated. This is not practical in most camera designs because of the memory and processing overhead that would be required to correct the entire area array.

Design Considerations

While it may seem like integrated CCD signal processors eliminate much of the system design effort, there are still some important decisions to make before choosing a device for a specific application. For example, these devices don't suit all imaging applications. Currently, 12 bits is the limit for the integrated products. Many high-end CCD applications require 14 or even 16 bits of resolution. These applications must still rely on discrete implementations. Many of the products cannot directly accommodate two other types of imaging sensors, such as CISs and CMOS imagers. These imaging sensors, while not currently up to the performance level of the CCD, potentially offer a lower system cost, and are now being used in some lower-end applications. A designer may wish to consider using an AFE, which can be used directly with CIS or CMOS sensors, to allow a future design path for lower-cost products.

When comparing different AFE products for a specific application, consider the minimum required features. The number of possible devices will usually be narrowed down based



3. The AD9807 processes the color CCD's outputs and sends the digitized data to the system ASIC for further image processing.

IMAGINE A LOGIC ANALYZER NO BUG CAN ESCAPE.

Heard the buzz? New Tektronix® logic analyzers let you measure signal activity down to a ridiculous 500 picoseconds — no, that's not a typo — on all channels. What's more, you can see state and timing measurements on the same screen. Simultaneously. And make all your measurements through the same probe instead of four jillion. So even the most radical designs can be ruthlessly debugged. For inescapable proof, call 1-800-426-2200 (press 3 and request code 3010), or visit www.tek.com/mbd/ad?1013

Tektronix®

WRH

on whether the application is a scanner or a camera. Further consideration should then be given to the required sampling rate, the programmable gain range, the amount of available offset correction, and the ease of which the device can be interfaced with the rest of the system. Examine the characteristics of the analog inputs. Is there an input clamp to facilitate capacitor coupling to the external CCD buffer amplifier, and is the input range compatible with the CCD signal? Check the timing requirements for compatibility with the system timing generator. If the device requires a digital interface to program the gain and offset levels, be sure that it will be compatible with the system ASIC. Power-supply requirements also should be considered.

Of equal or greater importance to the above factors is the AFE's level of performance. Careful attention should be given to the performance specifications in the data sheet and the operating conditions under which they are tested. Integrated devices have different configurations and system settings, so it is important to understand how the device has been characterized by the manufacturer. Noise and linearity are two areas of particular interest in imaging applications.

Noise in the AFE consists of wideband noise from all of the analog circuitry and the ADC, and quantization noise from the ADC. Standalone ADCs usually specify a signal-to-noise (SNR) or signal-to-noise plus distortion ratio, but these types of measurements are not entirely useful in imaging applications. The converter SNR is tested with a sinewave input, and includes the effects of analog distortion, distortion and spurs from integral and differential nonlinearity (INL and DNL, respectively), quantization noise, and thermal noise. Sometimes multiple data records are averaged, reducing the contribution of thermal noise. The distortion numbers are not of interest in imaging applications because CCD signals are not sinusoidal in nature, and the front end of the ADC samples the CCD signal only during a relatively slow-moving portion of the waveform. Instead of using a traditional converter SNR measurement, consider the contribution from wideband noise, quantization noise, and DNL errors. If the noise specifications given for a particular AFE are unclear or nonexistent, the wideband AFE noise can be measured using a "grounded-input histogram test." Here, the inputs to the device are grounded, and a histogram is taken of the output data. The standard deviation of the histogram will give the RMS noise level of the device, not including the ADC quantization noise. A low-noise AFE can have a thermal noise level comparable to or less than the RMS quantization noise of its on-board ADC.

AFE noise is important because it can impact the system dynamic range. Dynamic range is determined by comparing the maximum signal that can be processed to the minimum signal level that can be resolved in the system. Noise from the CCD, from the analog signal processing, and from the ADC will contribute to overall system noise level. Assuming that the CDS will reduce the kT/C and 1/f noise contribution, the CCD random noise can usually be found from the CCD manufacturer—specified as "noise floor" or "random noise" in millivolts or electrons RMS. Note that wideband noise introduced by the CCD and additional amplifier stages will not be reduced by the CDS. If the input signal to the CDS is not band-limited to the Nyquist frequency, which it typically is not, to achieve the necessary settling accuracy, then wideband noise will be aliased. Though a complete analysis on the subject is beyond the scope of this article, there is an important trade-off involved in setting the analog signal bandwidth—too much and the noise may be unacceptable; not enough and the settling time may be unacceptable.

CCD fixed-pattern noise due to variations in the dark current of each pixel can be very objectionable in images, and should be included in the noise calculation if it is not reduced through calibration techniques. Noise also will be introduced by the external CCD buffer amplifier, though this can be minimized. The noise contribution from the AFE can be found on the product's data sheet, or measured using the grounded input histogram test. The ADC's resolution will determine the quantization noise level, which is calculated by dividing the weight of one LSB by $\overline{12}$. Adding all the noise sources in a root-sum-of-squares fashion gives:

$$n_{TOTAL} = \sqrt{(n_{CCD})^2 + (n_{FPN})^2 + (n_{AFE})^2 + (n_{ADC})^2}$$

This equation can be used in approximating the achievable dynamic range, to see if the AFE being considered is a good match for the CCD. Be sure to refer all noise sources to the same point in the signal chain when making the total noise calculation. To refer all noise sources to the ADC output, the CCD noise sources should be multiplied by the gain of the processing stages, and the AFE noise specification should be output-referred. Alternatively, all noise sources can be referred back to the CCD output, by dividing the ADC quantization noise and AFE output noise by the front-end gain. Understanding which noise sources are dominant will help in the selection of an appropriate AFE.

The AFE's linearity will also affect system performance. The nonlinearities of a real ADC can cause artifacts in the digitized image. DNL is very important, because the human visual system is good at detecting edges or discontinuities in an image. DNL is the variation in code width for the ADC. Poor DNL causes uneven gradations or "steps" in adjacent luminosity levels. A true 10-bit system demands DNL of better than 1 LSB at the 10-bit level, with 0.5 LSB preferable to avoid degradation of image quality. Products with DNL poor enough to cause missing codes can cause image artifacts in the digital processing and should be avoided. INL is also important but less demanding than DNL in terms of LSB size. The human visual system is less adept at distinguishing gradual nonlinearity which is spread out over the entire grey-scale range. However, large INL can contribute to errors in the color processing algorithms of a particular system, resulting in color-related artifacts in the image.

After selecting a possible AFE for the application, thoroughly evaluate the device to explore its true performance under specific operating conditions. Unlike the use of discrete components, the integrated approach does not allow the evaluation of each

HEY! WHAT'S THE SMALL IDEA?

This is the look of big change.
100 watts. Convection cooled.
3" x 5" x 1".

We're onto something big. Our new power supplies are so small they're going to set new standards. And they're going to start changing the way you think about power supplies, too.

Think about the advantages of designing with a 100 watt power supply that measures just 3" x 5" x 1". Think about a whole new generation of power supplies that are significantly smaller, run cooler and more reliably, and deliver more power per square inch than any other power supplies around. Now think about calling us. We'll show you just how small the power supply industry is going to be. ***(800) 293-9998.***

EFFICIENT POWER CONVERSION

Eos Corporation
906 Via Alondra, Camarillo, CA 93012

(805) 484-9998 Fax: (805) 484-5854
Email: info@eoscorp.com
http://www.eoscorp.com

READER SERVICE 126

separate processing stage. Many manufacturers provide evaluation boards for their products to simplify this step of the design.

Application Example

An example of the Analog Devices' AD9807 used in a scanner design is shown in Figure 3. The CCD outputs are buffered with emitter followers or op amps to drive the signals from the CCD board through a flat cable to the main board. There the signals are capacitor coupled into the AD9807's analog inputs, and dc restored by the on-chip clamp circuits. The AD9807 processes and digitizes the signals to 12-bits. The digital outputs are then sent to the system ASIC where the digital image processing is performed. The timing signals are generated by the ASIC. Grounding, decoupling, and layout are critical, as with any high-speed application. In this circuit, a common ground plane is used under the AD9807. If a separate analog and digital ground is used on the main board, the grounds should not be split under the AFE, to prevent digital noise from coupling through the IC into the analog signal path. Instead, the entire AFE should be placed on the analog ground plane.

Future Integration

Additional integration seems logical to continue the low-cost, highly integrated strategy. Now that good analog performance is possible with standard CMOS processes, it should be possible to integrate some or all of the back-end digital processing of the imaging system. As the level of complexity goes up, power and ground management on the chip is critical to minimize digital noise coupling into the analog circuitry. Inclusion of such features as a SCSI interface on-chip is particularly challenging, due to the large driver currents required.

Erik Barnes is a senior applications engineer with Analog Devices' High Speed Converter Group. During Barnes' five years with the company, he has supported amplifier and converter products. Currently he specializes in signal-processing ICs for imaging applications. Barnes received his BSEE from Tufts University in Medford, Mass.

AT 166 MHZ, YOU CAN FEEL THE POWER OF OUR 4-MEG SRAMS.

Partial Selection	Access Time (ns)	Max. Freq.
256K x 18 pipelined	3.5 to 4.0	166 MHz
128K x 36 pipelined	3.5 to 4.0	166 MHz
256K x 18 flow-through	7.5, 8, 8.5, 10	117 MHz
128K x 36 flow-through	7.5, 8, 8.5, 10	117 MHz

Designers building the next generation of hot products for applications such as networking, communications and servers have high speed on their minds. ■ Galvantech is shipping high speed, high performance SRAMs today. Our 4-Meg synchronous burst SRAMs operate from a 3.3V power supply and deliver mind-blowing access times. The chips feature low standby power, sleep mode and support for the popular processors powering today's ultra-high performance devices. ■ Our high speed synchronous and asynchronous product line includes 1-Meg, 2-Meg and 4-Meg devices in a variety of organizations. The pipelined version of our 4-Meg achieves frequencies up to 166 MHz--with faster versions on the way! ■ If you want fast access to fast SRAMs, visit **www. galvantech.com today. Or call 408.566.0688 x 888.**

Galvantech

READER SERVICE 132

FLUKE

The industry-leading Fluke 80 Series III digital multimeters just got better.

Since their introduction, Fluke 80 Series digital multimeters (DMMs) have led the industry in versatile performance, accuracy, and rugged durability. Now the *new* Fluke 80 Series III DMMs push that lead even further. With a host of new features that increase accuracy, improve safety, and make the new 80 Series III easier than ever to use. Look at everything they have to offer:

- An LED backlight on *all* models for easier reading under virtually any light conditions
- New LCD display with larger digits and better viewing angle for easy reading from a distance
- MIN/MAX to record the minimum, maximum, and average reading over time. The 87 and 87/E now offer new 250 μS peak MIN/MAX for true peak transient capture
- $4^1/_2$-digit resolution to detect subtle changes (87, 87/E)
- Significantly improved basic dc accuracy on all models
- CAT III 1000V safety rated (IEC 61010-1) to withstand power surges
- Battery access door that enables change of batteries without breaking the calibration seal
- Lifetime warranty

Fluke. *Keeping your world up and running.*

Pending Pending

See for yourself at your nearest distributor.
Call **1-800-44-FLUKE** for the name of your nearest distributor. Or visit **www.fluke.com/handheld**

How to beat a leader.

READER SERVICE 129

Bus Interface Logic Evolves To Meet VLSI Needs

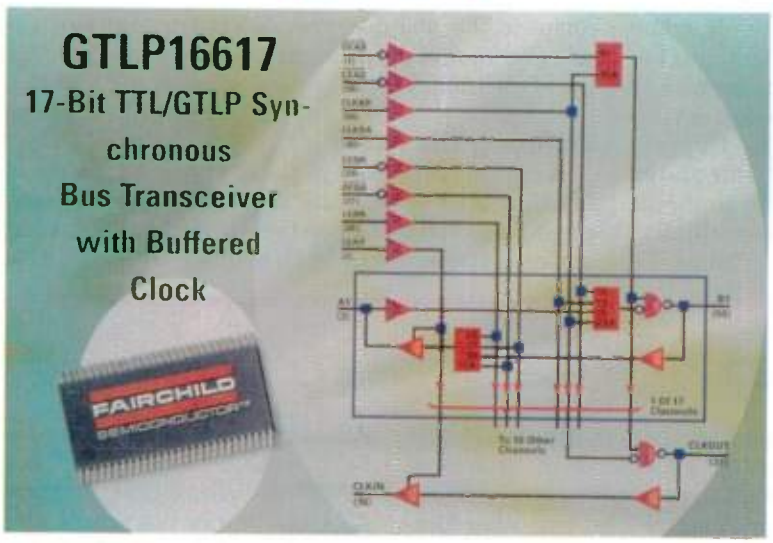
Current Advances In VLSI Circuit Interfaces Are Driving Down Delays And Power In Bus Support Logic.

Dave Bursky

SPECIAL REPORT

The wide variety of standard logic families created to meet the needs of system designers has been disappearing as programmable logic and other ASIC approaches swallow up most of the system logic. However, the myriad of applications and system requirements they entail continually demand that new interface support circuits be created to buffer, level shift, latch, or multiplex the signals on the various buses. All of these interface options have resulted in a veritable Tower of Babel when it comes to making some sense out of all the family names and associated capabilities *(see "The Alphabet Soup", p. 92).*

As operating voltage levels decrease while system speeds increase, still lower-voltage bus buffers, latches, and registers must be used to provide the drive while minimizing propagation delays and power consumption. Some of the latest efforts in that area comes from the low-voltage logic alliance formed by Fairchild Semiconductor, Motorola Semiconductor, and Toshiba America Electronic Components, which has drafted specifications for the VCX family of 2.5-V logic devices. This new generation of logic circuits is the industry's first multiple-voltage family compatible with both 3.6-V and next-generation 1.8-V supply operating specifications. The circuits also will offer the shortest propagation delays of any 2.5-V devices.



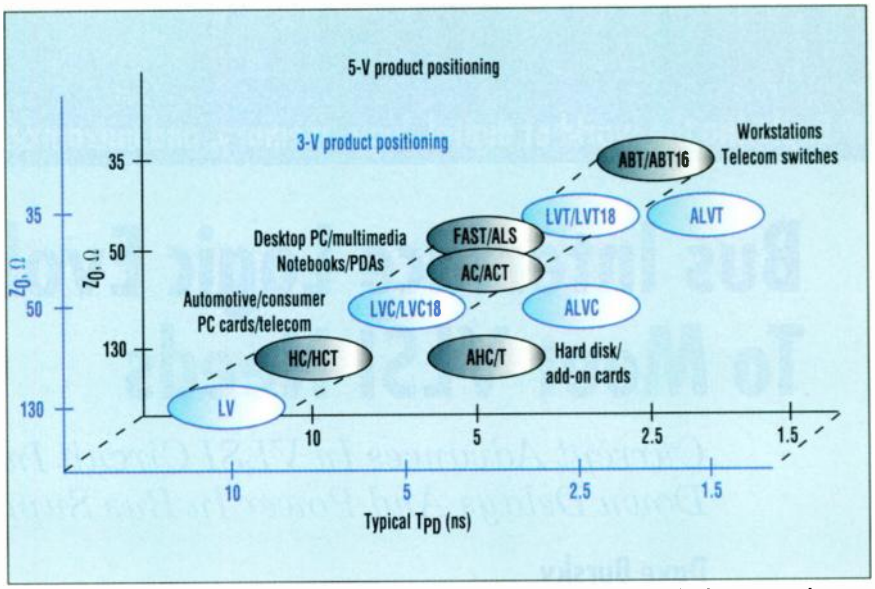
Art Courtesy: Fairchild Semiconductor

The initial circuits in the family include the 74VCX16244, 16373, 16245, and 16374—all 16-bit-wide devices that provide bus buffer, bus latch, bus transceiver, and register functions, and all extensions of the original 74244, 245, 373, and 374 octal devices that were introduced several decades ago. Propagation delays of the circuits are as little as 2 ns when operating at a power supply of 3 V. Such delays are the shortest for any CMOS logic family, and come close to matching the speeds of the best biCMOS circuits. Inputs are tolerant for signal levels of up to 3.6 V, yet can interface to either pure 2.5-V levels, mixed 2.5/3.3-V signals, or 1.8-V logic signals, permitting the circuits to support the design of systems that may intermix circuits that operate at voltages of 3.3, 2.5, or 1.8 V.

In addition, to support for live insertion and withdrawal, the circuits include high-impedance levels on the inputs and outputs, even with the power off. The circuits also will support high static drive currents. When operating from a 3-V supply, the chips can handle ±24-mA loads, ±18-mA loads when operating from a 2.3-V supply, and ±6-mA loads when operating from a 1.8 V supply. The ability to handle the smaller signal swings is supported by both noise and EMI reduction circuitry.

In the overall logic family genealogy, the new LVX series would form a new position that shows

it delivering higher performance than previous-generation biCMOS circuits such as the ABT series. A general positioning of the most commonly used logic families for both 3- and 5-V versions was developed by Philips Semiconductors; shown in a single dual-axis graph are the relative performance and impedance characteristics of many logic families *(Fig. 1)*.



1. Although not a complete positioning display of all logic families, this dual-axis graph developed by Philips provides the relative performance positioning among many of the popular 5- and 3-V logic families.

Equivalent Devices

Although the low-voltage alliance initially included only three companies that promised to make their chips work interchangeably, other companies are welcome to either join or to implement equivalent devices with matching characteristics. In some cases, companies such as Philips and Texas Instruments (TI) already have logic families that come close and may only have to tweak a characteristic or two to bring them into full specification compliance.

For system requirements that are not as delay sensitive, Toshiba and other companies have the LVX and LCX series, which offer typical delays of 4.7 and 5.2 ns, respectively, when operating from supply voltages between 3.0 and 3.6 V. Many companies also offer similar-performance devices and still slower circuits—Cypress Semiconductor, Hitachi, Integrated Device Technology (IDT), Motorola, National Semiconductor, Quality Semiconductor, Pericom, Philips, TI, and others have multiple logic families from which to choose. Some of the characteristics of several multisourced families are summed up by Pericom *(see the table)*. Although not complete, the table does provide a capsule overview of the main characteristics of each family listed.

Reducing The Noise

A critical issue when working with fast signals is the switching noise and ringing that takes place on the wiring between the buffer or latch and the destination. Slew-rate control as well as termination resistors in the logic circuits helps minimize signal reflections. That's exactly what designers have included in the VCX families—many of the devices, such as the 74VCX162244, a 16-bit buffer/line driver, and the 74VCX162245 bidirectional transceiver from Fairchild, have 25-Ω resistors in series with each output pin to reduce noise. The chips also have a quiescent current of just 20 μA and a maximum propagation delay of only 3.4 ns. The QS74LCX and FCT

Alphabet Soup

The abundance of bus-interface levels and signaling requirements has created a multitude of "standard" logic interface families to provide the level shifting, latches, registers, buffers, multiplexers, and other functions required to glue the VLSI chips and memory together. Here's a sampling of most of the logic families in use:

AHC/AHCT: advanced high-speed CMOS logic (T refers to TTL levels).
ABT: advanced biCMOS technology.
ABTE/ETL: advanced biCMOS technology/enhanced transceiver logic.
AC/ACT: advanced CMOS logic (T refers to TTL levels).
ALB: advanced low-voltage biCMOS.
ALS: advanced low-power Schottky logic.
ALVC: advanced low-voltage CMOS technology.
AS: advanced Schottky logic.
BCT: biCMOS technology.
64BCT: 64-series biCMOS technology.
BTA: bus termination arrays.
BTL/FB: backplane transceiver logic/FutureBus.
CBT: crossbar technology.
CBTLV: low-voltage crossbar technology.
74F: fast logic.
GTL: Gunning transceiver logic.
HC/HCT: high-speed CMOS logic.
HSTL: high-speed transistor logic.
LS: low-power Schottky logic.
LV/LVC: low-voltage CMOS technology.
LVT: low-voltage biCMOS technology.
S: Schottky logic.
SSTL: stub-series terminated logic.
TTL: transistor-transistor logic.

CompactPCI®

Visualize your embedded system WITH GESPAC

GESPAC has the total solution for your *CompactPCI*® Embedded Computer System. Fully configured and tested, including pre-loaded software.

- Pentium or PowerPC CPU
- 10/100 MB/S Ethernet
- Super VGA for LCD and CRT
- 4 and 8 Slot Backplane
- Prototyping Board
- IEEE 1394
- High Speed Data Aquisition
- Frame Grabber
- Industry Pack
- Signal Conditioners (A/D Digital TCD)

PowerPC™
PowerPC 603e
106 PCI and local memory controller
PREP / ARC compliant design & BIOS

Pentium®
- Pentium MMX 75 MHz to 200+ MHz
- TRITON II Chipset
- 16 KBytes of internal cache
- 256 KBytes of Level 2 cache

Gespac

Windows NT® pSOS® WindRiver®

Innovative Embedded Solutions

http://www.gespac.com

International
18 Chemin des Aulx
1228 Geneva
Switzerland
Tel: (41 22) 794 3400
Fax: (41 22) 794 6477

North & South America
50 West Hoover Ave.
Mesa, AZ 85210
1-800-4-GESPAC
Tel: (602) 962 5559
Fax: (602) 962 5750

Japan
Minami Aoyama
1-15-18, Minato-ku
Tokyo 107
Tel: (81 3) 3470 0640
Fax: (81 3) 3478 8648

France
E.T. de St Aubin
Rte de l'orme des Merisiers
91195 Gif-sur-Yvette
Tel: (33 01) 69 85 33 73
Fax: (33 01) 69 85 36 60

Germany
Amberg Haus
Kurt-Blaum-Platz 2
63450 Hanau bei Frankfurt
Tel: (49 0) 6181 24052
Fax: (49 0) 6181 24051

PCI INDUSTRIAL PICMG COMPUTERS

READER SERVICE 133

families from Quality Semiconductor include 8-, 16-, 18-, and 32-bit parts with built-in resistors in both latched and registered transceivers and buffer/line drivers.

Fast High-Drive Buffers

Combining biCMOS technology with advanced low-voltage TTL interface, Philips has crafted the fastest high-drive buffers, the ALVT series, which offers operation from 2.5-to-3.6-V power supply levels with full I/O compatibility up to 5.5 V. The circuits in the family provide 16-bit-wide bus interfaces and can drive loads of up to 64 mA per line—ideal for heavily loaded backplanes or buses. The circuits also offer live-insertion/extraction capability and all data inputs include a bus-hold feature that eliminates the need to pull up to a valid logic level lines that are unused or floating.

Delivering the highest performance at a power supply voltage of 3.3 V, Philips again claims the speed crown with its advanced low-voltage CMOS logic (ALVC) family. Circuits in the family have propagation delays of 2.1 ns, can operate from powr-supply levels ranging from 1.2 to 3.6 V, and can drive up to 24 mA on each I/O line as well as drive transmission lines with impedances down to 50 Ω. The buffers have almost zero static current consumption thanks to the all-CMOS construction. And, like the ALVT series, the chips also have the bus-hold feature.

A COMPARISON OF FOUR POPULAR LOGIC FAMILIES

Family/feature	FCT3245	LPT245	LVT245	LCX245
Technology	0.5 and 0.8-µm CMOS	0.6-µm CMOS	0.8-µm biCMOS	0.8-µm CMOS (0.6-µm for Pericom)
5 V I/O tolerant	No	Yes	Yes	Yes
Operating voltage	2.7-3.6 V	2.7-3.6 V	2.7-3.6 V	2.7-3.6 V
Ambient operating temperature range	-40 to +85°C (0 to +70°C)*	-40 to +85°C	-40 to +85°C	-40 to +85°C
Speed at 3.3 V±0.3 V	7.0/4.6 ns	7.0/4.6/4.1 ns	4.0 ns	7.0 ns
Drive (current output high/low)	-8/24 mA	-24/24 mA	-24/48 mA	-24/24 mA
Icc standby	10 µA	10 µA	90-190 µA	10 µA
VOLP noise	<0.8 V	<0.8 V	<0.8 V	<0.8 V
Package offerings	SOIC, QSOP, DIP, SSOP20	SOIC, SSOP20, TSSOP, DIP	SOIC, SSOP20, TSSOP	SOIC, SSOP20, TSSOP
Suppliers	IDT, QSI, Pericom	Pericom, Harris	TI, Philips, Motorola Hitachi (preliminary)	Motorola, Toshiba, National, Pericom

*QSI only

Reducing The Levels

In the dual worlds of ASICs and CPUs, designers are taking every opportunity to reduce the power supply level to shave down the operating power. As the supply levels go down, so do the signaling levels. To maintain good signal integrity, new interface standards are required such as the modified form of Gunning transceiver logic, GTLP, which uses an output low level of 0.65 V, a 1.5-V output high level, and a receiver threshold that's set for 1.0 V.

The first devices for this interface include the GTLP16616 and GTLP16617 from Fairchild, which provide asynchronous and synchronous bus operation, respectively. The transceivers provide a 17-bit interface, with the GTLP providing registered operation using D-type flip-flops that operate in either latch or transparent modes for the data path, and a GTLP translation of the clock signal that synchronizes the chip to

Directory Of Suppliers Of Bus Support Logic Circuits

Cypress Semiconductor Corp.
3901 N. First Street
San Jose, CA 95134-1599
(408) 943-2600
www.cypress.com
CIRCLE 544

Fairchild Semiconductor Corp.
333 Western Ave.
South Portland, ME 04106
(207) 775-8749
www.fairchildsemi.com
CIRCLE 545

Hitachi America
2000 Sierra Point Pkwy.
Brisbane, CA 94005
(800) 285-1601
www.halsp.hitachi.com
CIRCLE 546

Integrated Device Technology
2975 Stender Way
Santa Clara, CA 95054
(800) 345-7015
www.idt.com
CIRCLE 547

Motorola Semiconductor
5005 E. McDowell Rd.
P.O. Box 20903
Phoenix, AZ 85072
(800) 441-2447
sps.motorola.com/logic
CIRCLE 548

National Semiconductor Corp.
2900 Semiconductor Dr.
Santa Clara, CA 95054
(408) 721-5000
www.nationalsemi.com
CIRCLE 549

Pericom Semiconductor Corp.
2380 Bering Dr.
San Jose, CA 95131
(408) 435-0800
www.pericom.com
CIRCLE 550

Philips Semiconductors
811 East Arques Ave.
Sunnyvale, CA 94086
(408) 991-4942
www.philipslogic.com
CIRCLE 551

Quality Semiconductor Inc.
851 Martin Ave.
Santa Clara, CA 95050
(408) 450-8000
www.qualitysemi.com
CIRCLE 552

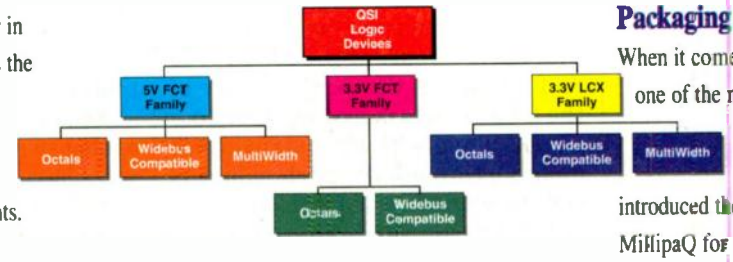
Texas Instruments Inc.
13500 N. Central Expressway
Dallas, TX 75265
(800) 336-5236
www.ti.com/sc/docs/asl/families
CIRCLE 553

Toshiba America Electronic Components
9775 Toledo Way
Irvine, CA 92718
(714) 455-2000
www.toshiba.com/taec/components
CIRCLE 554

The Logic Performers

For the best-performing logic devices to make your system sing, you need the exceptional performance logic from QSI.

Quality Semiconductor, a leader in advanced FCT logic, now offers the industry standard LCX logic as well as the fastest available C speed LCX logic for 3.3-volt and mixed 3.3V/5V environments.



FCT Logic

QSI is the recognized leader in high-performance logic. The 25-ohm resistor output was introduced by QSI to offer designers exceptional low-noise and low ground bounce performance. QSI constantly makes improvements to its logic products to help designers improve their total system performance.

LCX Logic

QSI now offers the most user-friendly family of choice. LCX is the 3.3-volt family with 5-volt tolerant inputs and outputs. QSI offers the 25-ohm resistor output and Bus Hold to give designers greater flexibility. The C speed of this family provides the designer an upgrade path for better competitive advantage.

Packaging Innovation

When it comes to packaging, QSI is considered one of the most innovative. QSI introduced the QSOP package— now the accepted industry standard. We've also introduced the QVSOP for 16-bit logic and the MillipaQ for 32-bit logic, the smallest packages available in the industry.

Check out our Website or call our toll-free number, **1-800-609-3669**, for a copy of the FCT or LCX databooks.

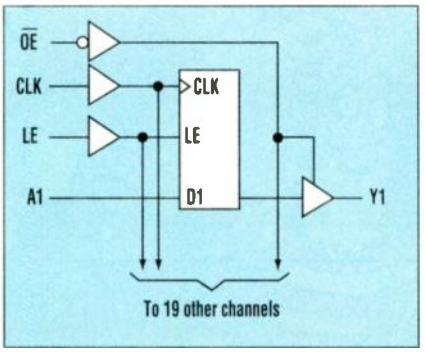
http://www.qualitysemi.com

QUALITY SEMICONDUCTOR, INC.®

Quality • Service • Innovation

U.S.A. Headquarters: 851 Martin Avenue, Santa Clara, CA 95050, 408-450-8000, Fax: 408-496-0773, http://www.qualitysemi.com
European Headquarters: Suite A, Unit 6, Mansfield Park, Four Marks, Hampshire, GU34 5PZ United Kingdom, 44-(0)1420-563333, Fax: 44-(0)1420-561142
U.S. and Canadian Distributors: Arrow Electronics, Bell Milgray Electronics, Nu-Horizons, Zeus Electronics, Inc.

READER SERVICE 182



2. A 20-bit latched stub-series terminated logic buffer (1 bit shown) provides designers with a means to convert low-voltage TTL levels on the circuit's inputs to the SSTL signal levels on the output.

system. The wide bus interface also pushes up the package pin count for the transceiver, which comes in a 56-lead shrink small-outline package, or a 56-lead TSSOP. In addition, the A-side port can handle source or sink currents of 32 mA.

Another specialty interface gaining popularity, especially in memory address bus area, is the Stub series-terminated logic. Available from TI is a 20-bit bus driver, the SSTL16837, that can drive 3.3-V address buses from a low-voltage memory controller. The circuit translates the typical low-voltage TTL (LVTTL) signals from the memory controller to the SSTL signals that are used by the SDRAM memory array input pins. The basic circuit of the LVTTL to SSTL buffer is the same for each of the 20 bits—clock and latch-enable signals along with the data/address input go through the latch (which is set up either in a latch or flow-through mode) and the circuit provides an SSTL signal out *(Fig. 2)*.

Specialty functions such as very wide I/O paths—20 bits and more—as well as new functions that reduce the chip count when working with multiple buses also are of high interest to designers. A 12-bit to 24-bit registered bus exchanger with three-state outputs is one such chip that designers at Hitachi have created. The HD74ALVCH16270 provides the interface when data must be transferred from a narrow high-speed bus to a wider, lower-frequency bus. The circuit provides synchronous data transfers between the two ports.

Complementing the bus exchanger is a 12-bit to 24-bit registered bus transceiver (the HD74ALVCH16269), which serves in applications where two separate ports are multiplexed onto or demultiplexed from a single port. Such a function is particularly useful as an interface between synchronous DRAMs and high-speed microprocessors.

A family of digital crossbar circuits, typically used for bus data exchanges is available from TI. These digitally controlled switches are the first in the industry to operate at 3.3 V and can help simplify the design of systems that require data movement across multiple buses. Included in the family is the SN74CBTLV3245, a low-voltage octal bus switch. Complementing that chip will be a 20- and a 24-bit bus switch, and 18- and 24-bit bus exchange circuits. The crossbars have near zero propagation delay (250 ps) and a very low on-resistance—less than 5 Ω typical. The devices also have a high-current-drive capability, delivering up to 64 mA to handle heavily loaded buses.

Providing some simple signal switching for buses and other signal paths, the Quickswitch family of bus-switch circuits developed by Quality Semiconductor and now available from several sources provides designers with devices that can be used like on-off switches to route bus signals from point to point. Larger Quickswitch devices also can be used to route or multiplex entire buses.

Somewhat reminiscent of the early analog switches, the Quickswitch devices have been optimized to handle digital signals, and can be switched on and off very quickly. Additionally, the Quickswitch elements can be used for level shifting, allowing 3.3-V logic to tie into 5-V systems and vice versa.

As system designs get more highly integrated, even to the point of embedding blocks of DRAM on the logic chips, single-chip solutions may eventually obviate the need for many of the interface and buffer circuits. While some chips will become total systems-on-a-chip, many other systems will still be partitioned into multiple chips. But in the future, all will operate at voltage levels of 2.5 V and still lower levels, ensuring continual development of new generations of interface logic.

Announcing a Technology Breakthrough

OUR NEW STEL-2176 IS THE *key* TO *cost effective* SUBSCRIBER *cable* MODEMS

Features

- 16/64/256 QAM receiver — Highest acquisition speed
- QPSK/16 QAM transmitter
  - — Direct digital synthesis modulator for broadband RF transmission (U.S. patent #5,412,352)
  - — High performance, efficient utilization of upstream spectrum
- Compatible with MCNS, IEEE 802.14, DAVIC/DVB standards
- Integrated 10 bit/165 MHz DAC and 10 bit ADC
- On-board dual mode Annex A & B FEC
- 0.35 micron, 3 volt CMOS technology

The fully integrated STEL-2176 Digital Modulator/Demodulator ASIC provides an extremely cost effective means for receiving 16/64/256 QAM signals and for sending QPSK and 16 QAM modulated signals. The STEL-2176 is designed specifically for the reception and transmission of data over broadband coaxial cable networks for Internet access, interactive CATV and digital telephony-over-cable applications. It provides optimal spectral shaping and fine tuning resolution across an output bandwidth of up to 65 MHz. The STEL-2176 is worldwide standards compliant.

As a companion product, the STEL-9257 provides QPSK demodulation at the headend. Contact us today for complete information on the STEL-2176 modem "super-chip" and other companion products for HFC Cable.

STANFORD TELECOM

480 Java Drive, Sunnyvale, CA 94089
Tel: (408)745-2660 Fax: (408)541-9030
e-mail: tpg.marketing@stelhq.com Internet: www.stelhq.com

READER SERVICE 192

READER SERVICE 141

ured as 32-words by 1-bit or 16-words by 2-bits, while the dual-port block comes only as a 16-word by 1-bit block.

As mentioned earlier, the configurable logic blocks are very similar to those in the XC4000 series. Each contains two flip-flops (with independent clock enables), dedicated arithmetic support logic (high-speed carry logic), and dual four-input Boolean-logic truth tables. Other resources available include eight global low-skew clock or signal-distribution networks, internal three-state bus capability, and a low-power segmented routing architecture. The I/O buffers have individually-programmable output slew-rate control to maximize performance and reduce signal noise. Additionally, input registers have a zero hold time, simplifying system timing.

The high system speed possible with the Spartan chips allows them to handle most system support functions such as PCI and USB interfaces, DSP cores, RISC processors, microcontrollers, and other functions. Additionally, the I/O cells are fully PCI-compliant. Furthermore, many predesigned functions such as Viterbi decoders, Reed-Solomon error-checking logic, UARTs, and other functions are available in the company's LogiCORE library or through the AllianceCORE partners program.

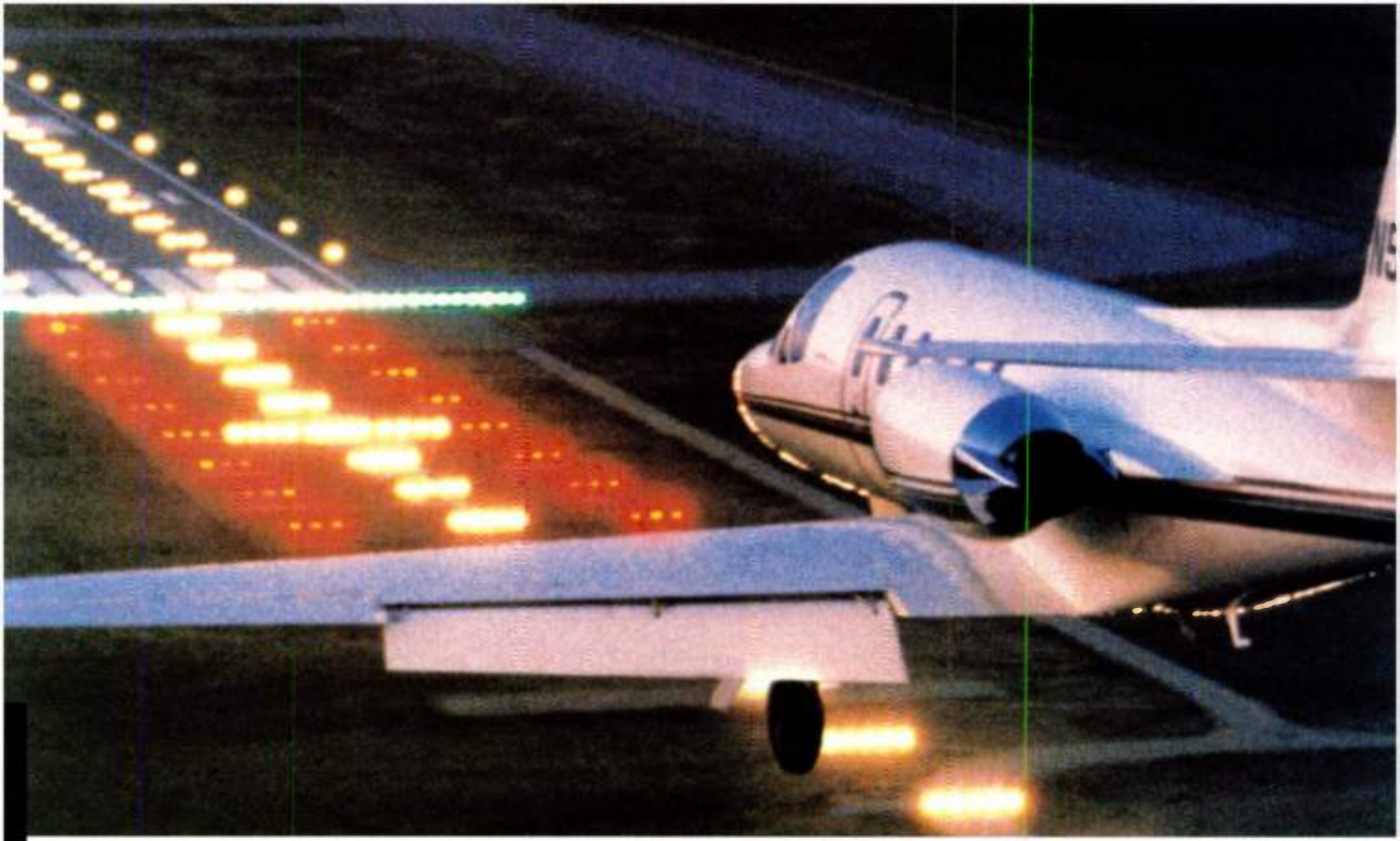
In addition to the library support, the Spartan family is fully supported by the company's Foundation development tools. These include a fully integrated, shrink-wrapped software package, and the Alliance series that supports over 100 PC and engineering workstation third-party development systems. The tools provide fully automatic mapping, placement, and routing. They also include an interactive design editor for design optimization.

Price And Availability

Samples of the Spartan XCS20, XCS30, and XCS40 are immediately available. The XCS05 and XCS10 will be ready late in the first quarter. In lots of 100 k units, the chips will sell for $3.95 to $19.95 each by late 1998. Samples of the XL 3.3-V version will be available in late 1998. In mid-1999, they will sell for $2.95 to $9.90 apiece. The development tool suites start at $495. Some of the third-party core providers include Cast Inc., White Plains, N.Y.; Integrated Silicon Systems Ltd., Belfast, Ireland; Memec Design Services, Mesa, Ariz.; T7L Technology Inc., North York, Ontario, Canada; and the Virtual IP Group, Sunnyvale, Calif.

Xilinx Inc., 2100 Logic Dr., San Jose, CA 95124; (408) 559-7778; www.xilinx.com.

CIRCLE 529



THIS IS A BAD PLACE TO DISCOVER YOUR RTOS IS ONLY 68.3% TESTED.

If you're designing avionics systems, the last thing you want to worry about is whether your software is going to be 100% reliable under real-world operating conditions. But the last thing you want to spend your time doing is getting your RTOS up to compliance with certification standards.

That's why we've made VRTX® certifiable under the FAA's tough RTCA/DO-178B Level A standard for 100% testing and code-coverage analysis, requirements traceability, configuration management and documentation.

VRTX has been developed and maintained following engineering practices and procedures which are ISO 9001-approved, so you know it's reliable enough for any mission-critical application (and even those that aren't so mission-critical). And VRTX is backed by the Spectra® integrated development environment, a suite of commercially supported tools—including Microtec's industry-leading XRAY® debugger and C&C++ compilers—that were all developed to the same rigorous ISO guidelines.

So don't take chances with your RTOS. For more information about VRTX for avionics applications—or anywhere high reliability for embedded software is required—visit our Web site or call us at **1-800-950-5554 for your free demonstration CD-ROM.**

READER SERVICE 229

VRTX

www.mentorg.com/microtec

Mentor Graphics

THE POWER TO CREATE™

MICROTEC DIVISION

Variable-Grain Architecture Pumps Up FPGA Performance

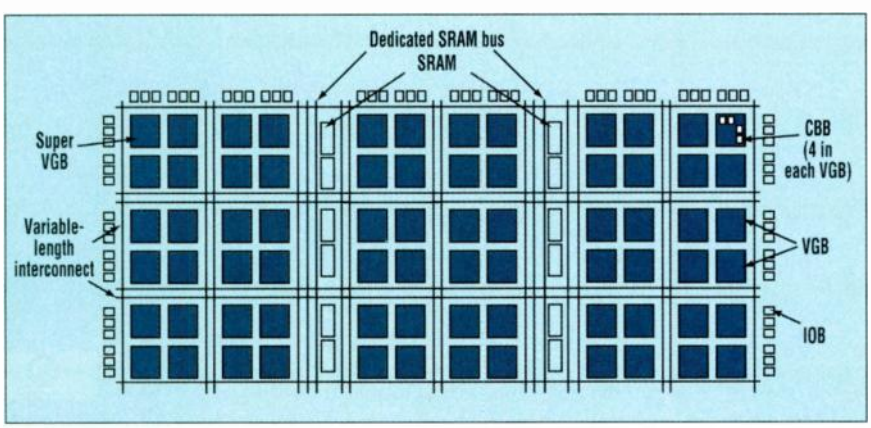
Highly Efficient Logic And Interconnect Allow A New FPGA Family To Deliver 250-MHz Operation.

Dave Bursky

Although SRAM-based FPGAs offer designers tremendous flexibility, they traditionally required lots of tweaks to coax maximum performance out of the logic configurations. By applying its most-advanced 0.18-µm CMOS four-layer-metal process, designers at Vantis developed a high-performance FPGA family with on-chip dedicated SRAM capable of delivering pipeline speeds of 250 MHz. Initial capacities up to 36,000 gates are being provided (functionally equivalent to 50,000 gates when on-chip memory is included). Furthermore, the architecture can be extended to chips that pack up to 250,000 gates and 64 kbits of memory. Future process enhancements by the year 2000 that shrink the gate length and add a fifth layer of metal interconnect promise chips with gate counts of half a million, 128 kbits of memory, and over 800 I/O lines.

Based on a novel variable-grain architecture Vantis recently developed, the VF1 series can deliver system speeds 50 to 100% faster than any other RAM-based FPGAs. Some of that increase can be attributed to the use of a shallow-trench isolation scheme to isolate the adjacent n- and p-type wells, permitting high packing densities and minimizing parasitics. The trench technology also is the foundation for the highly planar multilevel metal interconnects (four levels) used to implement a variable-length interconnect scheme that provides predictable performance and first-time-fit layouts. The variable-length-interconnect lets layout tools create the optimal length for every net, and provides high-speed direct connectivity to minimize connection lengths for optimized on-chip routing.

With densities starting at about 12,000 gates, the family targets high-performance complex systems that might normally be developed using a methodology based on HDLs such as Verilog or VHDL. To support the methodology and still remain friendly to synthesis and automatic layout tools, Vantis crafted the new variable-grain architecture that allows basic cell groupings to implement from 3-input to 32-input functions.



1. Appearing somewhat like a checkerboard, the top-level architecture of the variable-grain block field-programmable gate arrays developed by Vantis includes multilevel hierarchy logic blocks, dedicated rows of SRAM blocks, and a ring of I/O buffer cells surrounding the logic and memory blocks. Only the top half of this six by six array of Super VGBs is shown.

The highest level of the family architecture is somewhat similar to most FPGAs—the chip contains an array of large logic blocks referred to as super variable-grain blocks laid out in almost checkerboard fashion. Interspersed with the blocks are rows of dedicated high-speed 5-ns-access single- or dual-port SRAM blocks, and surrounding the entire array are I/O buffers *(Fig.1)*.

Each RAM block is 32 words by 4 bits and has dual ports (one read and one read/write) that allow an application to read from one port while writing into the other, or read from both ports simultaneously. Registers on the I/Os allow memory blocks to be used in pipelined systems without consuming logic resources from within the array. Larger memory arrays can be formed by concatenating the blocks to obtain the desired word width and depth.

Initially, the family will include four members—the VF1012, 1020, 1025, and 1036—that will respectively pack 12, 20, 25, and 36 kgates of logic and 3584, 4608, 5120, and 6144 bits of SRAM. The chips will offer maximum I/O pin counts of 172, 208, 244, and 292, respectively, although each version will be available in various pin-count package options (from 144-lead TQFPs to 352-lead BGAs) to offer pin-compatible upgrades and various cost points. According to Vantis, since logic and memory capabilities are counted separately, the actual gate count is equivalent to higher-gate count numbers used by other FPGA suppliers who provide an estimated gate count. For example, the VF1036 is estimated to be functionally equivalent to 50 kgate devices from other FPGA suppliers.

The actual variable-grain architecture consists of three levels. At the lowest level is the configurable building block (CBB), which consists of dual, three-input look-up tables (LUTs), multiplexers, a register, and the configuration/interface logic *(Fig. 2a)*. Next level up are the variable-grain blocks (VGBs) each of which has four CBBs, special wide gating to combine two or more

All the LCD features you need for outstanding FA systems

Factory environments vary widely. That's why NEC TFT LCD screens let you pick the optimum features for your application. Features include a 12.1" size, 800 x 600 resolution, ultra-wide viewing angle and high luminance. Touch-sensor panels are attachable.

Whatever your requirements for FA systems, we have a TFT LCD screen that will make your system look its best. For further information, contact NEC today.

Features	Large screen High luminance	High resolution	Ultra-wide viewing angle	High luminance Wide viewing angle	
Model number	**NL8060AC31-12**	**NL8060AC26-11**	**NL6448AC33-24**	**NL6448AC33-27**	**NL6448AC33-18**
Screen	12.1"	10.4"	10.4"	10.4"	10.4"
Pixel numbers	800 x 600	800 x 600	640 x 480	640 x 480	640 x 480
Display colors	262,144	262,144	262,144	262,144	262,144
Luminance	250cd/m² typ.	190cd/m² typ.	190cd/m² typ.	250cd/m² typ.	200cd/m² typ.
Viewing angle	Up 35°/down 55° Right/left ±60°	Up 20°/down 45° Right/left ±45°	Up/down ±80° Right/left ±80°	Up 55°/down 40° Right/left ±60°	Up 30°/down 20° Right/left ±45°

Operating temperature: 0°C to +50°C A backlight inverter is attached to all models.

The right components to build your reputation

On the Internet at http://www.ic.nec.co.jp/compo/lcd/index_e.html

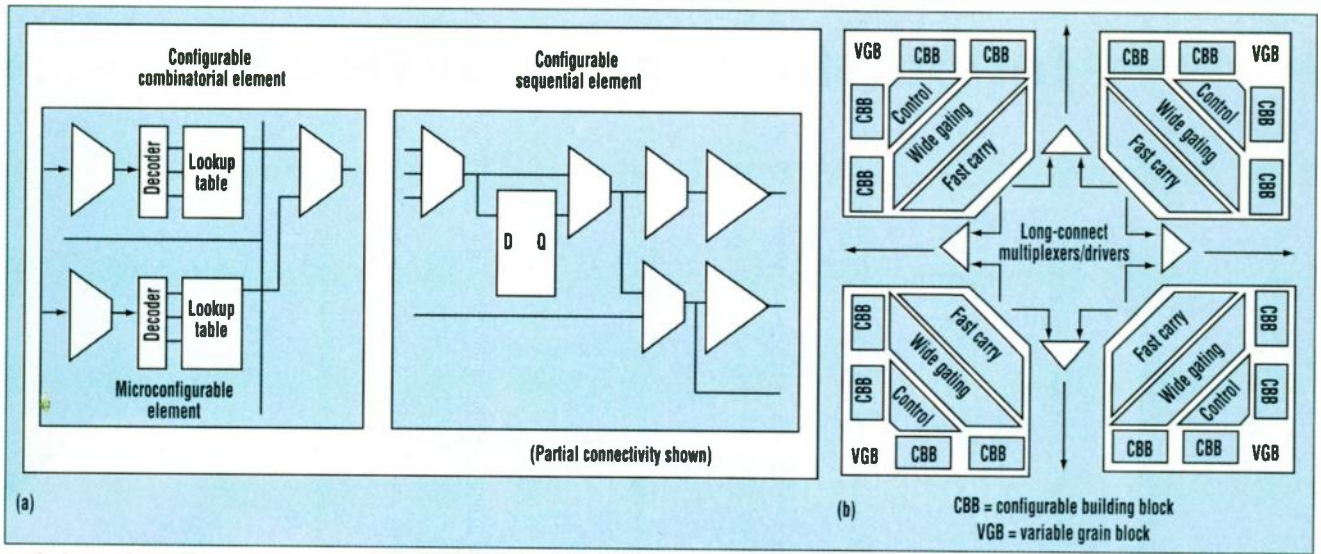
For fast answers, call us at: USA Tel:1-800-366-9782.Fax:1-800-729-9288. **GERMANY** Tel:0211-650302.Fax:0211-6503490. **THE NETHERLANDS** Tel:040-445-845.Fax:040-444-580. **SWEDEN** Tel:08-638-0820.Fax:08-638-0388. **FRANCE** Tel:1-3067-5800. Fax:1-3067-5899. **SPAIN** Tel.1-504-2787.Fax:1-504-2860. **ITALY** Tel:02-667541. Fax:02-66754299. **UK** Tel:1908-691133.Fax:1908-670290. **HONG KONG** Tel:2886-9318.Fax:2886-9022. **TAIWAN** Tel:02-719-2377.Fax:02-719-5951. **KOREA** Tel:02-551-0450.Fax:02-551-0451. **SINGAPORE** Tel:253-8311.Fax:250-3583. **AUSTRALIA** Tel:03-8878012.Fax:03-8878014. **JAPAN** Tel:03-3798-6148.Fax:03-3798-6149.

just imagine

NEC MULTIMEDIA

NEC

READER SERVICE 172



2. The lowest level of the logic hierarchy of Vantis' variable-grain FPGAs consists of the configurable building block—a logic cell that contains two triple-input look-up tables and a configurable sequential element (a). Groups of four CBBs and some associated control logic, fast-carry logic, and wide gating control form a variable grain block. Four such VGBs are combined along with long-connect multiplexers and drivers to form a Super VGB (b).

CBBs into more complex functions, high-speed carry logic to build high-performance adders/subtractors, and common control logic. The top level consists of super variable grain blocks (SVGBs), each of which has four VGBs that can be combined to create even more complex high-performance functions using local-interconnect resources *(Fig. 2b)*.

By keeping all the connections within an SVGB, very high speed circuits can be implemented since wire delays are minimal. To ensure the circuits operate at high speeds, the chip includes a pair of 200-MHz PLLs to aid in system clocking and signal deskewing. Thus, internal fully pipelined circuits can clock at 250 MHz, while external buses can operate in excess of 150 MHz. Internally, the shortest path delay from one input pin to one output pin is as short as 6 ns, while the longest pin-to-pin delay is 12 ns. With such short delays, internal functions such as a 16-bit counter can be clocked at over 170 MHz, a 32-bit address decoder can operate at 88 MHz, and a 24-bit accumulator can run at 142 MHz. Overall, Vantis estimates that the VF1 arrays will deliver about a 2:1 performance improvement versus other comparable-density FPGAs.

Each CBB is subdivided into three sections—a microconfigurable element consisting of the three-input input decoder and LUT, the configurable combinatorial element which has two microconfigurable elements and some additional logic, and a configurable sequential element which contains the register/latch and configuration logic. Bit patterns loaded into each LUT define the output generated by each input combination. Also, one of the CBB outputs can either be latched or can bypass the latch to provide a direct output, while the second CBB output is a non-latched, direct output. Both of the outputs can be connected to a variety of interconnect resources. When four-input functions are required, the two triple-input microconfiguration elements can be combined to form a single 16-bit LUT.

Just as LUTs can be combined in a CBB to form wider-input functions, multiple CBBs in a VGB can be combined with local interconnections. Thus, four 3-input LUTs can be combined to form a 32-bit LUT, allowing all possible combinations of five inputs to be decoded. At the extreme, all CBBs in a VGB can be combined into a single 64-bit LUT that decodes a 6-bit input value.

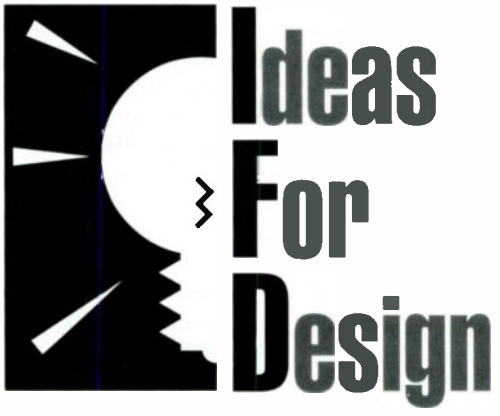
However, in many applications, not all possible combinations of a set of inputs must be decoded. As a result, configuring CBBs in combinations other than those already mentioned can save device resources. For example, two CBBs in a VGB can be configured as separate 4-input elements with their outputs multiplexed to generate an 8-input function using only two CBBs. Since each CBB decodes 16 combinations of four inputs, this configuration decodes 32 possible combinations of eight inputs. Configurations up to 32 inputs wide can be implemented in this manner.

At the highest level, the super VGB consists of four mirrored VGBs with four sets of shared long-connect multiplexers and drivers. The VGBs' symmetrical arrangement in the SVGB improves logic density and minimizes interconnection length when implementing complex functions. The shared drivers allow the SVGB to connect to other SVGBs, to embedded memory, and to the I/O buffers on the chip's perimeter. Each set of shared drivers contains four drivers that can be used to connect the SVGB to other parts of the chip and the I/O buffers. Either a single VGB or two VGBs can access a shared driver within the SVGB, and two VGBs within an SVGB may be combined to make a logic function with up to 32 inputs using only two levels of logic and a shared driver—a very efficient implementation that reduces propagation delays.

Flexible Wiring

For the most efficient signal routing between VGBs and SVGBs, VF1 devices include many local interconnection options to make possible many complex functions using only the interconnection lines within the VGBs and SVGBs. Some routing options include the inter-VGB direct-connect lines, which wire certain outputs of a VGB to the inputs of eight nearby VGBs (two above, two below, two to the left and two to the right, except for those VGBs

Got A Cool Circuit Idea?



You get *Electronic Design*. What do you turn to first? Ideas For Design (IFD)? You're not the only one — our own studies as well as those conducted by independent surveying firms continually show that Ideas For Design is one of the most highly-read sections in the most widely-read electronics publication. And because of its popularity, we have decided to expand the section.

THAT MEANS MORE IDEAS FOR DESIGN EVERY ISSUE!

We need your ideas, and you have them, so here's a chance to tell the world (literally) about the great circuit design you've had on the drawing board.

Not only is it possible to get your name and idea in print for our 165,000-plus readers, but if it gets published, you'll be in line to receive an honorarium of $100. On top of that, your idea has a chance to be voted by your peers as "Best of Issue," which receives an honorarium of $300.

IFD Guidelines:

- 1 to 1-1/2 pages of single-spaced typewritten text;
- Include schematics, charts, tables, code listings, etc.;
- Include name, company affiliation, address, phone/fax/e-mail

Send your Ideas For Design to:

IFD Editor
Electronic Design
611 Route 46 West
Hasbrouck Heights, NJ 07604
or:
Fax: 201/393-6242
e-mail: xl_research@.compuserve.com
or: rogere@csnet.net

ELECTRONIC DESIGN
TECHNOLOGY·APPLICATIONS·PRODUCTS·SOLUTIONS

at the perimeter of the array, which directly drive the I/O buffers). Also available are variable-length interconnect resources, which provide programmable interconnections that may span from two VGBs to the entire chip.

The variable-length interconnect resources provide designers with four types of wire resources that run in both horizontal and vertical channels between the SVGBs. The types include 16 long-connect lines that run from edge to edge on the chip in the horizontal and vertical channels, four octal connect lines that span eight VGBs both horizontally and vertically, four quad-connect lines that span four VGBs (two SVGBs) both horizontally and vertically, and eight double-connect (or twin) lines that span two VGBs within a single SVGB. Long-connect lines can also be used to implement three-state buses. Octal-, quad-, and double-connect lines cannot. Special switch boxes at the intersections of the horizontal and vertical groups of lines provide interface points for signals to switch between horizontal and vertical paths.

As mentioned earlier, the flexible routing allows Vantis' design support tools to optimize, map, and place-and-route the cells for first-time-fit results. The flexible interconnect structure also simplifies pin-locking (allows the external pin functions to remain the same when the internal logic is reconfigured or updated, eliminating pc-board redo) or density shifting (moving from one device to a different-density device while maintaining the same pinout).

Providing the interface to the outside world, I/O buffers surround the entire logic array and can be configured with 3.3- or 5-V I/O levels. Each buffer is fully programmable and contains independent I/O logic sections that share only a common I/O pad and set/reset logic. Separate input and output enable signals allow an I/O buffer to function as both an input and an output pin. The input section consists of an input buffer, a latch, and configurable logic that connects the buffer to the appropriate interconnect lines. The output section includes programmable interconnections, an output latch, and an output buffer with slew-rate control.

Besides routing the signals around the chip, keeping them in lockstep becomes extremely important as operating frequencies go up. To aid in the timing challenge, a pair of embedded PLLs can be used to deskew clocks from one chip to another, and to synthesize on-chip clocks by using the system clock as a reference frequency. The PLLs can be used to synthesize on-chip clocks that are multiples of the system clock, up to a maximum of 200 MHz. Four on-chip global clock lines distribute timing signals with minimal skew and delay.

Defining the arrays' logic configuration is typically done with high-level tools since for circuits with complexities above about 10,000 gates, HDLs and synthesis tools provide the most-efficient approach. Since the VF1 series was designed with such tools in mind, the suite of Vantis design tools as well as third-party tools all operate efficiently and produce good first-time results.

The design flow typically consists of two parts. The first part might typically consist of third-party front-end development tools for design capture, simulation, synthesis, and timing analysis. Designs are then transferred to the Vantis tools in either a generic EDIF or Vantis-specific format. In the second part, the actual design is done with the Vantis physical design tools that take the synthesized logic and map it to the FPGA, perform timing calculations, placement and routing, and create the programming configuration file.

The Vantis tool suite consists of a design manager, a graphical-user interface (GUI), and a logic editor and viewer. The tools are timing driven, employing the timing-constraint files provided by the third-party front-end tools to generate the timing files needed for more detailed timing analysis and simulation. Supporting the design tools will be a selection of high-value reusable cores, the first of which will be PCI interfaces that provide both 33- and 66-MHz master and target system options. Also available will be a library of parameterized modules to provide many basic extendible logic functions.

Price And Availability

Samples of the VF1 family FPGAs will be available in the second quarter of this year, with volume production slated for the third quarter. Prices for the arrays start at $46 apiece in volume quantities (second half 1998 pricing). The Design Direct software starts at $1495.

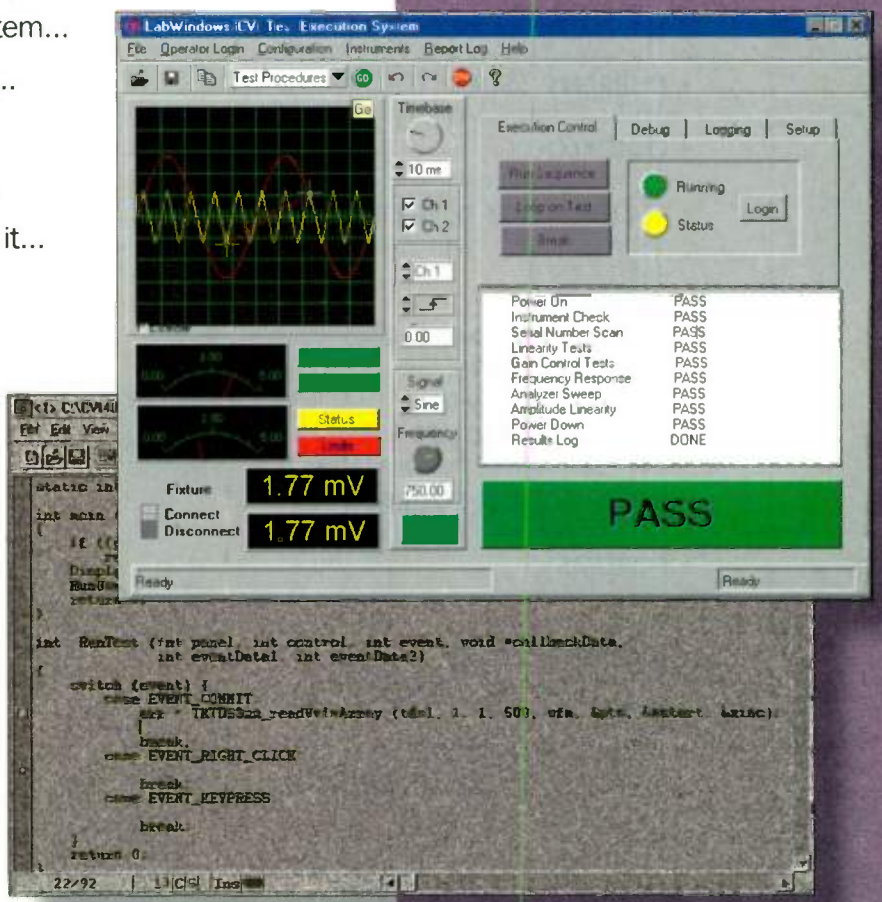
Vantis, An AMD Company, P.O. Box 3755, 995 Stewart Dr., Sunnyvale, CA 94088; Andy Robin, (408) 732-0555; www.vantis.com.

CIRCLE 530

Build on a Rock Solid Test Foundation

LabWindows™/CVI
Virtual Instrumentation Tools for C/C++

When you need to build a BIG test system...
When you can't afford to get locked in...
When it has to be fast...
When you need a solution that works...
When your production line depends on it...
When your job is on the line...



Why look anywhere else?

- ✔ Standard ANSI C Programming
- ✔ Lightning-fast code generation
- ✔ Open development environment
- ✔ VXI*plug&play* driver standard

For data acquisition, GPIB, and VXI instrument control, analysis, and user interface tools, LabWindows/CVI has everything you need under one roof.

Put LabWindows/CVI to Your Test!

NATIONAL INSTRUMENTS™
The Software is the Instrument™

U.S. Corporate Headquarters
Tel: (512) 794-0100 • Fax: (512) 794-8411
info@natinst.com • www.natinst.com
Worldwide network of direct offices and distributors.

Call today for your FREE LabWindows/CVI Evaluation Version
(800) 661-6063
(U.S. and Canada)

READER SERVICE 168

PRODUCT FEATURE

Single-Chip MPEG-2 Encoder Exhibits Low Cost

While MPEG decoder chips have started to appear as mainstream products over the last year, encoders continue to remain at the high end as complex and costly items. That's about to change, though, with the introduction of the CXD1922Q, a real-time MPEG-2 encoder. The part combines MPEG-2 encoding, a system controller, and motion-estimation circuitry all on one IC. The low-power device is aimed at consumer electronics, video servers, communications, and DVD applications.

The CXD1922Q supports 720- by 480-pixel images at 30 frames/s for NTSC data. The maximum encoding rate is 15 Mbits/s. The chip offers a search range of –288 to +297.5 horizontal pixels and –96 to +95.5 vertical pixels, at half-pixel accuracy, allowing for encoding of fast-moving scenes. The chip also supports dual prime encoding for low bit-rate applications. The integrated controller handles such functions as timing, complex motion control, and bit-rate control.

Housed in a 208-pin QFP, the CXD1922Q supports a 16-bit controller-host interface and requires 32 Mbits of SDRAM. Samples are available now for $600.

Sony Semiconductor Company of America
3300 Zanker Rd.
San Jose, CA 95134
(800) 228-SONY; (408) 955-6572
www.sony.com/semi.
CIRCLE 490
RICHARD NASS

Aeroflex Microprocessors and Memory Provide...

Cutting Edge Technology ◆ Increased Life Span ◆ Orderly Migration ◆ Footprint & Pinout Compatibility

Your Total Microelectronics Solutions For Industrial—Military & Space—for 30 Years!

■ MIPS BASED RISC MICROPROCESSORS

2.5V & 3.3V CORE • 3.3 & 5V TOLERANT I/O • STANDARD THRU-HOLE & SMT FOOTPRINTS • CERAMIC

Primary Cache (L1) Products

- R4430 (64 Bit) 25-100 MHz
- R4700 (64 Bit) 100-135 MHz
- R5000 (64 Bit) 100-180 MHz
- NEW • RM5230 (32 Bit) 100-200 MHz
- NEW • RM5260 (64 Bit) 100-200 MHz
- NEW • RM5270 (64 Bit) 100-200+ MHz

Secondary Cache (L2) Products

- R4430 (64 Bit) 1M of SC, 25-100 MHz
- NEW • RM5270 (64 Bit) 2M of SC, 100-200+ MHz
- NEW • RM7000 (64 Bit) 256K of on chip SC, 100-250 MHz

Tertiary Cache (L3) Products

- NEW • RM7000 (64 Bit) 256K of SC, 2M of TC, 200-250 MHz

■ STANDARD MEMORY

3.3V AND 5V • STANDARD THRU-HOLE & SMT FOOTPRINTS • CERAMIC • PLASTIC

SRAM

- 512K x 8 Bit, 15-45 ns
- 128K x 32 Bit, 15-45 ns
- 512K x 32 Bit, 17-45 ns
- 1 M x 32 Bit, 17-45 ns

SYNC DRAM

- NEW • 1 M x 96 Bit, 15-45 ns

FLASH

- 128K x 8 Bit, 60-150 ns
- 512K x 8 Bit, 60-150 ns
- 1M x 8 Bit, 70-150 ns
- 128K x 32 Bit, 60-150 ns
- 512K x 32 Bit, 60-150 ns
- NEW • 1M x 32 Bit Boot Block 80-120 ns
- NEW • 2M x 32 Bit, 90-150 ns

MIXED MEMORY MODULES

- NEW • 128K x 16 Bit, SRAM & FLASH
- NEW • 512K x 16 Bit, SRAM & FLASH
- NEW • 512K x 32 Bit, SRAM & FLASH

EEPROM

- NEW • 128K x 32 Bit, 150-300 ns

ISO-9001 CERTIFIED

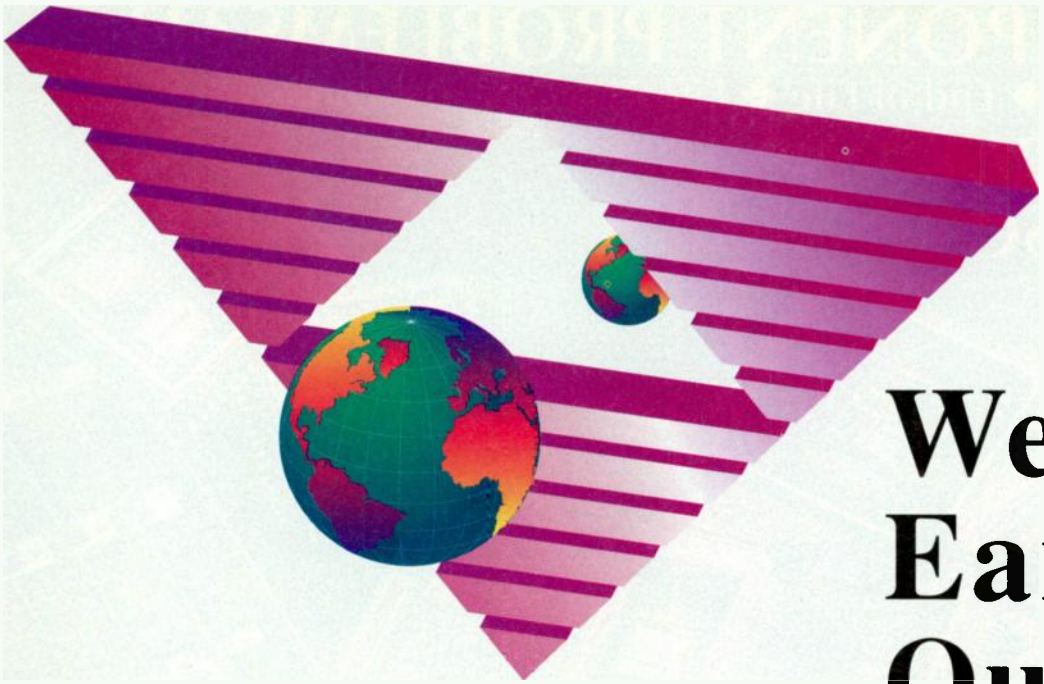
AEROFLEX

The Future In Microelectronics

CIRCUIT TECHNOLOGY

35 South Service Road • Plainview, New York 11803
TEL: 516-694-6700 • FAX: 516-694-6715 • http://www.aeroflex.com/act1.htm

READER SERVICE 111



We've Earned Our Stripes!

THERMAL MANAGEMENT • MIXED SIGNAL • POWER MANAGEMENT

We're doing what it takes to turn promises into reality, and customers are noticing. In fact, in a recent article about TelCom Semiconductor, one of our customers described TelCom by saying that our commitment was absolute and our execution flawless. Pretty high praises we know, but that's the standard we set. We're TelCom Semiconductor, the user-friendly analog source.

We can help solve your system and circuit problems with our broad portfolio of application specific standard products. So whether you're trying to navigate around power management or data acquisition problems, or simply keep your system running smoothly, we can help. Our rapidly growing company reacts quickly to meet your short cycle times and development schedules – that's why major OEMs work with us.

Get to know us by visiting our web site at http://www.telcom-semi.com to check out our growing product line and get a FREE copy of our latest Selection Guide, or for more information call 1-800-888-9966. You'll see why we've earned our stripes.

FREE!

www.telcom-semi.com
1-800-888-9966

TelCom Semiconductor, Inc.
Analog & Mixed Signal

READER SERVICE 227

DATE '98 Reflects Changes In Design And Test Philosophies

Shifts From Circuit-Level To System-Level Design, And From Testability To Built-In Self-Test Show Up At The Paris Event.

Peter Fletcher

Billed by its organizers as the largest event of it's kind ever to take place in Europe, DATE '98 (Design, Automation, and Test in Europe) boasts impressive statistics. With 120 technical papers to be presented at the conference, together with workshops, tutorials, and "fringe meetings," the organizers expect to attract about 1000 delegates to Paris for the Feb. 23-26 event.

DATE '98 is the integration of several conferences and shows on design, design automation, and test that have arisen more or less piecemeal throughout Europe over the years. It's the combination of the European Design & Test Conference (which was already a mix of EDAC, the European Test Conference, and EuroASIC) and EuroDAC, which was held jointly with the EuroVHDL conference. According to Patrick Dewilde, conference chairman, "At last Europe has got its act together, and we now have a single conference and exhibition devoted to design, automation, and test."

The list of organizations and institutions that have pledged actual and moral support to the show almost guarantees that it will make a good complement to the Solid-State Circuits series. "All the major institutions and associations are supporting this event," notes Dewilde. "It is bringing together the whole community from the learned academic through to the practicing design community. It provides support and interest in topics ranging from electronic system design methodologies to testing, verification, and design reuse at all levels, from that of senior management to the newest student."

Dewilde points out that the quality of the conference is assured because out of nearly 500 submissions only 120 papers were selected for the technical program. In addition to the conference itself there will be a users forum, with electronic design examples as a separate track; a major exhibition; tutorials; keynote speeches; hot topic sessions; panel sessions; vendor sessions; and lots of fringe meetings.

Shifting Emphasis

Themes that stand out from the program show a shifting emphasis in the design community, according to Dewilde, from circuit level to system level, from pure CMOS design to heterogeneous design, from testability to built-in self-test (BIST), and from hardware to embedded software. "Classical issues are as alive and useful as ever—in particular simulation, layout synthesis, and verification—due to the new frontiers in speed and scale offered by microelectronics technology moving into the deep-submicron dimensions," he adds. "DATE '98 will make a shift in application domains apparent. Embedded systems-on-a-chip are becoming the ideal of the day, complete with embedded communication functions at the level of ATM, or immense embedded memories and DSP-oriented massive processing for multimedia applications," continues Dewilde.

Now that it's been coordinated into one event, the plan is to stage DATE annually toward the end of the first quarter. The timing aims to avoid clashes with related events, which traditionally take place in the fall. The show locale will alternate between Paris and Munich.

In addition to the main conference *(see the table)* there will be six preconference tutorials occurring on Monday, Feb. 23. Three tutorials of three hours each will be held in parallel in the morning (tutorials A, B, C) and in the afternoon (tutorials D, E, F). Participants must enroll for the day, and may combine any of the morning tutorials with any of the afternoon tutorials.

The state of the electronics industry, with its growing emphasis on embedded systems, is reflected in the tutorials at this year's conference. Peter Marwedel of Dortmund University, Germany, will present a session on "Compilers for embedded processors" (tutorial A). Such processors come in the form of discrete devices as well as in the form of core processors. They are available both from vendors and system companies. Applications can be found in most segments of the embedded-system market, such as automotive electronics and telecommunications. These compilers require extremely efficient processor architectures, optimized specifically for a certain application domain or even a certain application.

Marwedel will present techniques to easily retarget compilers to new architectures. These techniques are motivated by the need for domain- or application-dependent optimizations of processor architectures. The scope for such optimizations should not be re-

stricted to hardware architectures. It should include the corresponding work on compilers as well. The tutorial will show how compilers can be generated from descriptions of processor architectures. Presented techniques aim to bridge the gap between electronic CAD and compiler generation.

Another session will cover "Design, verification, and test of core-based system chips" (tutorial B). The leaders, Yervant Zorian of Logic Vision, San Jose, Calif., and Sujit Dey of the University of California, San Diego, note that the key to the success of the system-on-a-chip design is the development and use of predesigned, precharacterized, and preverified functional blocks called cores or intellectual property.

Designing Systems-On-A-Chip

System-on-a-chip design methodologies using cores will be described, including required software and hardware development support, software and hardware estimation tools, and issues in system-level integration. Validation methodologies currently used to verify the correctness of such systems will be discussed, including emulation, in-circuit emulation, compliance test environments, instruction-set simulation, and hardware-software cosimulation. The tutorial will also cover the test-related issues. Finally, it will discuss the recent challenges and adopted strategies to implement an integrated test strategy from embedded cores to a system-on-a-chip.

A third related session, "ILP compilation techniques for embedded systems" (tutorial E), will review the basic issues and advances in instruction-level parallelism (ILP). Alex Nicolau and Nikil Dutt of the University of California, Irvine, note that software, already a significant component of embedded systems, will dominate the design of future systems, and that compilation technology will be needed for the effective use of that software.

The tutorial will focus on the capabilities, limitations, and status of ILP compilation techniques for embedded systems. Included will be compiler techniques for ILP, including trace scheduling, superblocks, percolation scheduling, software pipelining, and memory disambiguation. In the context of embedded-system design, the session will describe memory-related optimizations, including register allocation, instruction and data caching, data reorganization, and alignment. Next, the intrinsic phase coupling and ordering problem between the compiler subtasks of instruction selection, scheduling and register allocation will be presented. Then the tutorial will delve into approaches to code generation that combine these subtasks into a unified framework that allows design trade-offs to be made "on-the-fly" during compilation.

Minature Intelligent Systems

Then, there is "Microsystems technology and applications," (tutorial F) by J. Malcolm Wilkinson of Technology for Industry in the United Kingdom. Wilkinson describes microsystems as "intelligent miniaturized systems comprising sensing, processing, and/or actuating functions, normally combining two or more electrical, mechanical, or other properties on a single chip or multichip hybrid." They offer increased functionality, improved performance, and reduced system cost.

The tutorial will provide an overview of the evolution, types, fabrication, and application of modern microsystems, including examples of technological strategies suitable for direct use in small- and medium-size high-tech companies. Topics will include specialized and low-cost processes; 3D and 2D structures; novel materials for optical, magnetic, biological, and thermal sensors; special packaging techniques like flip-chip and anodic bonding; microsystems design and manufacturing flow; CAD tools; and packaging and test issues.

Other tutorials include a session on "Design techniques for low-power-systems," (tutorial C) presented by Christian Piguet of CSEM, Neuchatel, Switzerland. Piguet notes that low-voltage and low-power digital design has to be performed at several levels, such as architecture, logic, and basic cell levels, while looking for reductions in activity, capacitance, frequency, and supply voltage. Comparisons of energy-efficient ar-

Enhanced JTAG Solution Allows Testing For Interconnect Delay Defects At Speed

An intellectual-property-based solution allows testing and diagnostics of board-level interconnects at the board's full operating speed, enabling users to check complex boards for delay defects. The solution, jtag-XLi, adds enhanced IEEE-1149.1-compatible boundary-scan cells and specialized at-speed interconnect (ASI) controller blocks to ASICs. The technique is completely transparent to IEEE-1149.1 (JTAG) testing, so a board can contain a mixture of chips with jtag-XLi technology and conventional JTAG technology.

In conventional JTAG testing, 2.5 test-clock (TCK) cycles are needed to launch data from one chip and receive it at another. Because TCK is typically limited to 20 to 40 MHz, the effective test frequency available is 8 to 16 MHz. As a result, many board manufacturers use functional testing or in-circuit testing (ICT) to check for interconnect delay faults, which are flaws that increase the travel time of a signal along an interconnect line. But ICT is very difficult with complex boards, and functional tests can be time-consuming.

The new at-speed boundary-scan cells consist of standard JTAG cells augmented with specialized logic and a system-clocked flip-flop. For at-speed testing, the enhanced cells are controlled by at-speed versions of the standard update and capture signals, in this case generated by the ASI test controller. A board-level synchronization signal also is routed between the ASI controllers on the chips involved in the interconnect test to ensure that all ASI controllers are aligned to the same system clock cycle.

If purchased as an option to the company's icBIST product, jtag-XLi costs $15,000 per chip design. As a standalone product, jtag-XLi costs $25,000. It will be available in the second quarter of this year.

LogicVision Inc., 101 Metro Dr., San Jose, CA 95110; (888) 584-2478; fax (408) 467-1180; e-mail: info@logicvision.com; www.logicvision.com. **CIRCLE 532**

LINEAR TECHNOLOGY

DESIGN NOTES

10Mbps Multiple Protocol Serial Chip Set: Net1 and Net2 Compliance by Design – Design Note 174

David Soo

Introduction

With the increase in multinational computer networks, comes the need for the network equipment to support different serial protocols. When the designer becomes occupied with the details of the interface specification, there is always the possibility that one small detail will be missed. This compliance headache causes designers to seek out a cost-effective, integrated solution.

The LTC®1543, LTC1544 and LTC1344A have taken the integrated approach to multiple protocol. By using this chip set, the Net1 and Net2 design work is done (see Figure 1). In fact, Detecon Inc. documents compliance in Test Report No. NET2/102201/97. With this chip set, network designers can concentrate on functions that increase the end product value rather than on standards compliance.

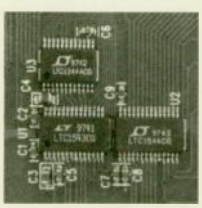


Figure 1. The LTC1543, LTC1544 and LTC1344A Multiple Protocol Serial Chip Set

Review of Interface Standards

The serial interface standards V.28 (RS232), V.35, V.36, RS449, EIA-530, EIA-530A or X.21 specify the electrical characteristics of each signal, the connector type, the transmission rate and the data exchange protocols. In general, the U.S. standards start with RS or EIA and the equivalent European standards start with V or X. The single-ended standard, V.28 (RS232) has a lower data rate than the other differential standards. The current maximum RS232 data rate is 128kbps. As for the V.35, V.36, RS449, EIA-530, EIA-530A and X.21 standards, the maximum data rate is 10Mbps.

Typical Application

Like the LTC1343 software-selectable multiprotocol transceiver, the LTC1543 and LTC1544 use the LTC1344A for switching resistive termination. The main difference between these parts is the functional partition: the LTC1343 can be configured as a data/clock chip or a control-signal chip using the CTRL/CLK pin, whereas the LTC1543 is a dedicated data/clock chip and the LTC1544 is a control-signal chip.

Figure 2 shows a typical application using the LTC1543, LTC1544 and LTC1344A. By just mapping the chip pins to the connector, the design of the interface port is complete. The chip set supports the V.28 (RS232), V.35, V.36, RS449, EIA-530, EIA-530A or X.21 protocols in either DTE or DCE mode. Shown here is a DCE mode connection to a DB-25 connector.

The mode select pins M0, M1 and M2 are used to select the interface protocol, as summarized in Table 1. There are internal 50µA pull-up current sources on the mode select pins, DCE/DTE and the INVERT pins. The protocol may be selected by plugging the appropriate interface cable into the connector. The mode pins can be routed to the connector and are unconnected (logic 1) or wired to ground (logic 0). If all the mode-select pins are not connected (logic 1), the chip set enters the no cable mode in which the chip set lowers the supply current to less than 700µA and three-states the driver and receiver outputs, and the LTC1344A disconnects the termination resistors.

Table 1. Mode Selection

Mode Name	M2	M1	M0
Not Used	0	0	0
EIA-530A	0	0	1
EIA-530	0	1	0
X.21	0	1	1
V.35	1	0	0
RS449/V.36	1	0	1
V.28/RS232	1	1	0
No Cable	1	1	1

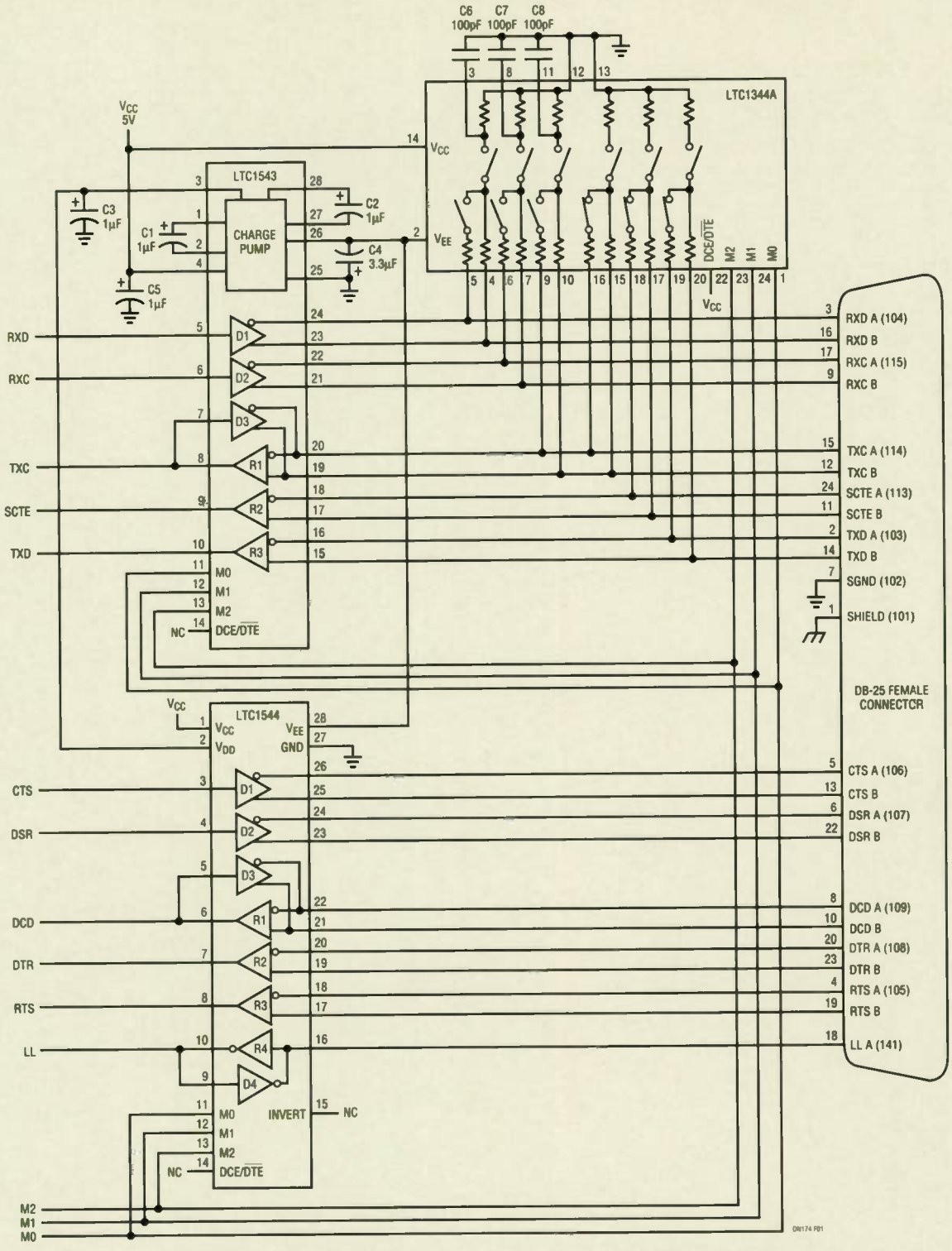


Figure 2. Controller-Selectable Multiple Protocol DCE Port with DB-25 Connector

For literature on our Interface Products, call **1-800-4-LINEAR**. For applications help, call (408) 432-1900, Ext. 2453

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417• (408) 432-1900
FAX: (408) 434-0507• TELEX: 499-3977 • www.linear-tech.com

dn174f LT/TP 0298 340K • PRINTED IN THE USA

1998 Design Automation And Test In Europe Conference (DATE)

Monday, Feb. 23

Tutorials
∞A: Compilers for embedded processors
∞B: Design, validation and test of core-based system chips
∞C: Design techniques for low-power systems
∞D: Formal verification
∞E: ILP compilation techniques for embedded systems
∞F: Microsystems technology and applications

Meetings
∞EDAA meeting
∞P1149.4 mixed-signal test bus
∞P1500 embedded core testing
∞IFIP Working Group 10.5/ECSI SIG on VHDL

Tuesday, Feb. 24

Meetings
∞European Test Workshop '98
∞CENELEC/TC17 Working Group 2: HDLs
∞Mixed-Signal Testing Technical Activities Committee and Benchmark Development Group
∞IEEE design and test roundtable
∞The use of reuse of embedded test technology within the telecommunications industry

Official opening and keynote addresses
∞Design and test challenges behind systems-on-silicon
∞Design methodologies for the information age: Moving up the totem pole
∞Build-in quality for systems chips and beyond

Session 1A
Design optimization of building blocks
Session 1B
Hardware/software partitioning and communication synthesis
Session 1C
Asynchronous and hybrid VHDL-based design
Session 1D
Data path and FPGA testing
Session 1E
System-level design (designer track)
Session 2A
Design methods for high-performance applications
Session 2B
Scheduling in embedded systems
Session 2C
Advanced techniques for VHDL design
Session 2D
Novel BIST approaches
Session 2E
ASIC (designer track)
Session 3A
Architectures for image processing
Session 3B
Scheduling and analysis of hardware/software systems
Session 3C
Extensions to VHDL
Session 3D
Error detection and error design verification
Session 3E
Hot topic—IP-based system-on-a-chip design

Wednesday, Feb. 25

Session 4A
Design reuse methodologies
Session 4B
Flat and timing-driven processor design
Session 4C
Hot topic—reconfigurable systems
Session 4D
Digital simulation and estimation
Session 4E
Layout design (designer track)
Session 5A
Synthesis of reprogrammable and reconfigurable architectures
Session 5B
Partioning and routing
Session 5C
Panel—formal verification: A new standard CAD tool for the industrial design flow
Session 5D
Simulation for high-level design
Session 5E
Test and testability: Industrial methodologies (designer track)
Session 6A
Architectural synthesis
Session 6B
Timing and crosstalk in interconnect
Session 6C
Panel—next-generation system design tools
Session 6D
I_{DDQ} and memory testing
Session 6E
IPs and cores (designer track)
Session 7A
Microsystems
Session 7B
Interconnect modeling
Session 7C
Design for manufacturability—embedded tutorial
Session 7D
Sequential circuit testing
Session 7E
Design resuse: The role of the VSI Alliance

Thursday Feb. 26

Session 8A
Issues in behavioral synthesis
Session 8B
Formal equivalence checking using decision diagrams
Session 8C
Hot topic—silicon debug of system-on-chips
Session 8D
Characterization and verification of analog circuits
Session 8E
FPGA design tools (designer track)
Session 9A
Benchmark circuits, technology mapping and scan chains
Session 9B
Physical-to-gate-level design for low power
Session 9C
Hot topic—memory and embedded logic
Session 9D
Analog circuit modeling and design methodology
Session 9E
PCB/MCM and system design (designer track)
Session 10A
Combinational logic synthesis
Session10B
High-level power estimation
Session 10C
Petri nets and dedicated formalisms
Session 10D
Mixed-signal test and DFT
Session 10E
Rapid hardware/software systems prototyping (designer track)
Session 11A
Sequential logic synthesis
Session 11B
High-level power optimization
Session 11C
System architecture design
Session 11D
Simulation and test tools for analog circuits
Session 11E
Timing, power, and layout optimization (designer track)

LabVIEW Graphical Instrument Software Gets A Major Facelift

Multithreading And ActiveX Capability Bring The Graphical Instrument Programming Language Up To Date.

John Novellino

The use of powerful software technologies like ActiveX, Java, and multithreading can greatly enhance an application. These technologies, however, can be very difficult to employ in many development environments. Designers are then left with the unattractive choice between a more powerful final product or a faster time-to-market.

In an effort to eliminate this tradeoff, National Instruments Corp. has substantially revised its popular LabVIEW graphical instrument software. LabVIEW Version 5.0 adds several new capabilities and makes other powerful technologies easy to use in data-acquisition, test and measurement, and analysis applications. And, current LabView users will be glad to hear that one of the new features is a multistep "Undo."

The new Undo capability is a feature that LabVIEW users have been requesting for some time. National notes that although Undo is a common function and simple to implement in word processors and spreadsheets, it's a very sophisticated and challenging utility to add to a graphical programming language. In fact the LabVIEW development team spent more than three years creating a versatile, extensive undo capability.

Other enhancements in LabVIEW 5.0 include:

- Multithreading
- Instrument wizards
- An ActiveX container
- Automation servers
- Distributed computing tools
- Translation and documentation tools
- Graphical differencing tools
- Programmable menu bars

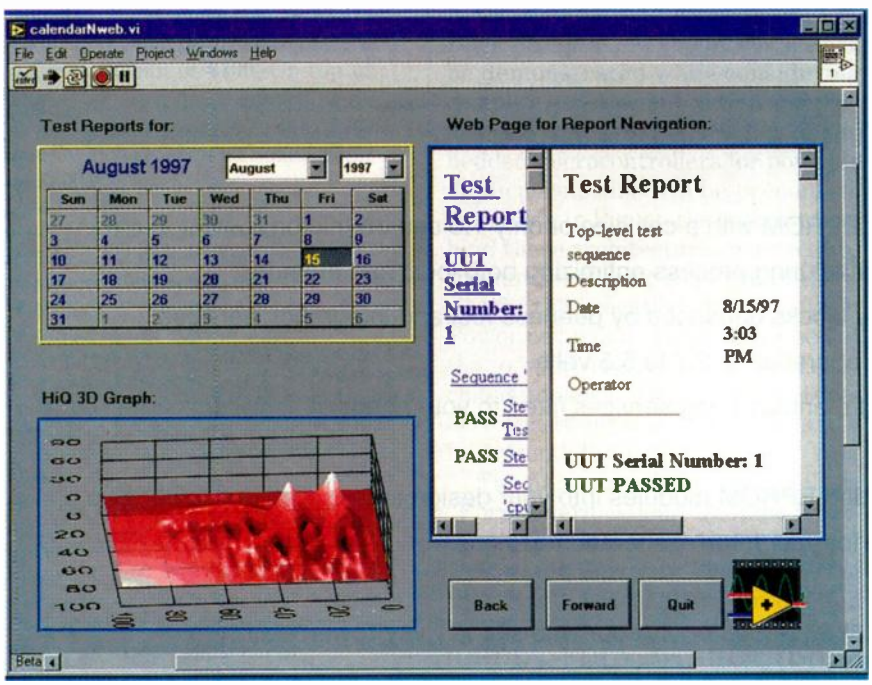
The software supports Windows NT, 95, and 3,1; Mac OS; Solaris; HP-UX; and Concurrent PowerMAX.

Multithreaded operating systems such as Windows NT and 95 and Sun Solaris offer more efficient CPU use, better system reliability and user interface response, and improved performance. Users can also take advantage of multiprocessor machines. But few applications are actually multithreaded because the technology is difficult to implement, according to National Instruments.

But multithreading is built into every virtual instrument or program developed in LabVIEW, and all of the complex tasks of thread management are built into the LabVIEW execution system. So, users don't even need to know what multithreading is to take advantage of it. Expert users, however, can take control of specific threads, including changing thread priorities, by using a straightforward dialog-box option. Furthermore, users can make any existing LabVIEW virtual instrument multithreaded by merely loading their existing programs into version 5.0.

Back in version 4.1, National added data-acquisition wizards to provide users with a way to create data-acquisition programs with just a few mouse clicks and no programming knowledge. The wizards generate the program and create a block diagram that can be modified as needed.

Version 5.0 extends the wizards to instrument control. No programming is needed. The wizard identifies and tests the instruments connected to the system, then automatically installs instrument drivers and generates appli-



1. As an ActiveX container, LabVIEW 5.0 allows users to drop any ActiveX control or document onto a virtual instrument front panel. Examples include web browsers, calendar controls, and HiQ Notebook graphs. The reusable ActiveX controls improve development efficiency.

YOU CAN'T STOP TIME.
BUT WHAT IF YOU COULD MAKE IT STAND STILL?

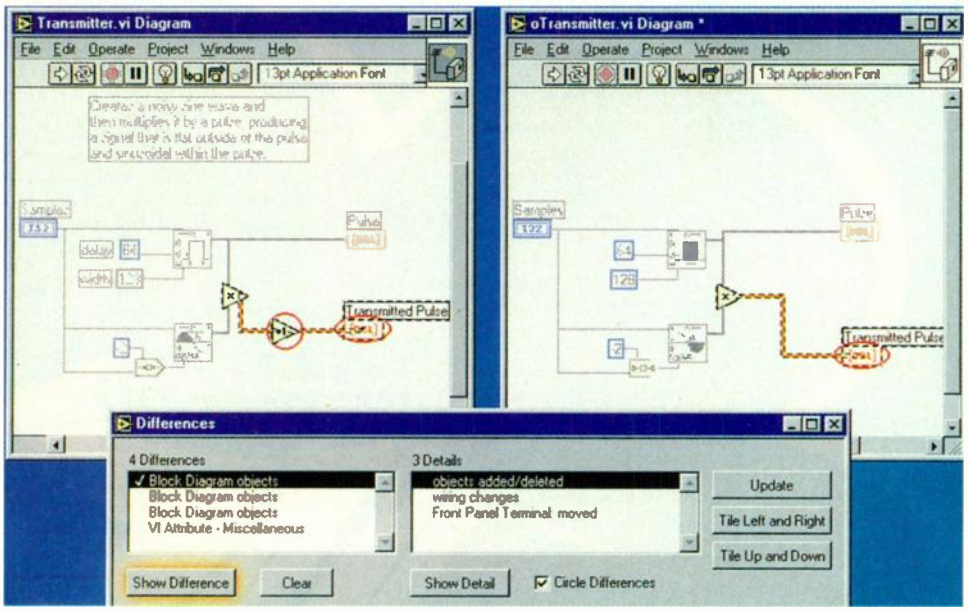
A new 500 mile per hour train can take a couple miles to stop. Yet a new 400 MHz microprocessor can stop in less than a nanosecond. If, that is, you happen to have a Tektronix® TDS oscilloscope. With its InstaVu™ technology, it can freeze even the fastest of designs...capturing 400,000 waveforms per second, 100 times that of other scopes. It's really like freezing a moment in time. Or stopping a train on a dime. To get onboard, call us at 1-800-426-2200 (press 3 and request code 3009), or visit us at www.tek.com/mbd/ad?1012

Tektronix®

cation examples that use the drivers. A program can be up and running with only a few mouse clicks. To ensure flexibility, the wizard creates the application with source code.

The new version also enhances the data-acquisition wizards. The company added analog output, digital I/O, and counter-timer capabilities to the data-acquisition channel wizard. Additionally, the wizards are now available on the Macintosh platform.

LabVIEW 5.0 also is an ActiveX container, meaning that users can drop any ActiveX control or document onto a LabVIEW front panel, edit it by clicking on it, and control it within a programming environment using a graphical approach on the block diagram. Among the large number of controls and documents available are National's ComponentWorks control, web browser controls, a HiQ Notebook, Excel spreadsheets, Word documents, and calendar controls *(Fig. 1)*.



2. The new graphical differencing tool compares two LabVIEW programs and identifies differences between them. Users can click on an item in the resulting list to go to the appropriate location and view the difference.

Code Sharing Possible

The reusability of ActiveX controls improves development efficiency and allows code sharing throughout an organization. Software developers can easily integrate these reusable objects, written in other languages, directly into a LabVIEW virtual instrument with no complicated programming.

An automation server added to version 5.0 allows users to remotely call LabVIEW programs from outside the LabVIEW environment. As a result, users can call a LabVIEW virtual instrument from any ActiveX Automation client, such as a program written in C, Visual Basic, or Microsoft Excel. In fact, a user can control the entire LabVIEW development environment from another program.

In some applications, users want their programs to execute on multiple machines, either to break up computationally intensive routines or because data must be collected from several locations. These distributed systems can require a lot of overhead code to pass data between the machines or to execute calls on remote machines.

With LabVIEW 5.0, however, users just write their initial programs, load them onto the machines where they'll be executed, and then write a simple program to call them at a specified location. When this controller program is executed, it reads the target location and executes the desired function there. The ActiveX interface makes the server launch LabVIEW if it is not already open, so the target does not need to keep it running. Users can elect to display the program as it runs on the target machine or have it execute in the background.

New tools added to version 5.0 can automatically create software documentation in HTML and RTF formats. One mouse click can generate a user manual, function reference manual, or online help system. For international applications, users can export text associated with a program to a file for translation, and then import it back into the program. For multilingual capability, users can choose from a list of languages at run time, and LabVIEW will load the appropriate translated file. The entire application will then run in the selected language.

To simplify the development of large applications, National added a graphical differencing tool that can compare two LabVIEW programs and identify differences between them. This tool also should make revision control easier. The tool generates a list of the differences between two programs. Users can then click on an item in the list, and LabVIEW will go to the corresponding location and highlight the difference *(Fig. 2)*. To speed up the comparison, users can choose to view all the differences, only cosmetic differences, or only functional differences. Previously, differencing tools were available only for text-based programs.

Important considerations when developing a software application are who will use the product and what type of technical background he or she might have. Training time can be shortened significantly if the developer creates user interfaces similar to those of the operating system. LabVIEW has always allowed users to create custom menus, but the latest version makes it a lot easier. Within a programming environment, developers can create custom menu bars that work like those found in many operating systems and common applications, like Microsoft Word.

Price And Availability

LabVIEW 5.0 will be available during the first quarter of this year. Prices remain at $995 for Windows NT, 95, and 3.1 for PCs, $1995 for Mac OS computers, $2995 for Sun and HP workstations, and $4995 for Concurrent PowerMAX systems. A Windows or Macintosh upgrade is $295. A Unix upgrade is $395.

National Instruments Corp., 6504 Bridge Point Pkwy., Austin, TX 78730-5039; (800) 258-7022; (512) 794-0100; fax (512) 794-8411; e-mail: info@natinst.com; www.natinst.com. **CIRCLE 528**

Coverification Tool Allows Debug, Test, Integration Before Silicon Arrives

The CoreTAP coverification development platform allows designers to debug, test, and integrate microprocessor-core-based ASICs before silicon availability. The small, portable, networked instrument offers real-time visibility 30% to 50% earlier than normal in the design cycle by showing the interaction of intellectual property, physical hardware, and embedded software on the microprocessor core.

CodeTAP was developed jointly with Viewlogic Systems Inc., and together with Viewlogic's Eaglei software toolset, provides simultaneous hardware simulation, software test, and software debug. The initial version is for the ARM 7 processor. Other processor-specific versions will follow this year.

CoreTAP's simulation features include functional and cycle-accurate simulation of the processor and the bus. This capability exceeds the accuracy provided by instruction-set simulator technology. Simulation support also is available for real and virtual hardware and other bus masters that vie for control of a common bus. With its ability to synchronize real to virtual time, CoreTAP enables the RTOS kernals to be ported and tested prior to silicon, without kernal modification.

The evaluation toolset includes 32 Mbytes of memory and 2 Mbytes of flash memory. An LCD display interface permits testing of driver software and hardware common to system-on-a-chip applications. Also included are a serial channel that can act as an iRDA driver or debug port, an Ethernet channel that provides for TCP/IP drivers and supplies a fast link to the hardware simulation environment, and a PCMCIA interface to develop driver software.

The unit's instrumentation features include header connections to the address, data, and control signals needed to support the CodeTEST universal pod. Also, a JTAG-style debug connection supports in-circuit emulators and a header-style connector accommodates logic analyzers. CoreTAP can also be connected to software verification tools, such as Applied Microsystems' CodeTEST products.

Prices for the CoreTAP coverification tool start at $20,000. Delivery is in eight weeks. Eaglei is available from Applied Microsystems or Viewlogic starting at $40,000.

Applied Microsystems Corp.
5020 148th St.
P.O. Box 97002
Redmond, WA 98073-9702
(425) 882-2000
e-mail: info@amc.com
www.amc.com
CIRCLE 470
JOHN NOVELLINO

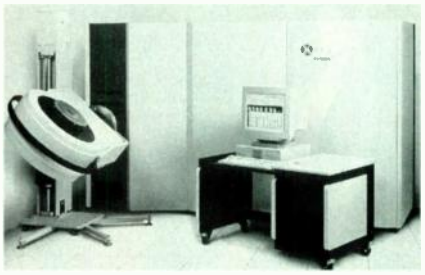
IC Test Series Covers Many Types Of High-Performance Applications

Two test systems, the Fusion DS for multimedia applications and the Fusion HT for advanced mixed-signal applications, are the first configurations to employ the recently announced Fusion technology for system-on-a-chip ICs. The Fusion technology allows advanced mixed-signal, VLSI digital, digital signal processing, RF, memory, power, and time measurement testing on one platform.

Fusion DS handles fast, digitally intensive applications like 100BaseT transceivers and high-speed serial interface devices for PCs. It can be configured with 512 pins of 250-/500-MHz non-multiplexed digital capability. Options include FlexWave, a 250-/500-MHz timing subsystem with independent, per-pin event-based waveform generation. Also available is HSDC, a high-speed data-channel capability for testing fast serial interfaces used by protocols like FibreChannel, FireWire, and PanelLink.

The HiPerII high-performance pin electronics option delivers higher bandwidth source and measure capability, plus 50-mV minimum swings. Another option, HiPerPhase, is a differential I/O mode of the HiPerII pin that can drive accurate differential waveforms and perform a true differential comparison on device-under-test (DUT) output signals for testing of fast communication devices.

Fusion HT targets advanced mixed-signal applications like wireless RF devices, smart power devices, and



consumer video and audio ICs. Options include a 4.3-GHz capability, HiPer technology, and PowerPulse, which allows users to deliver up to 160 A to the DUT at a full-power bandwidth greater than 1 MHz.

The Fusion platform is supported by enVision++, an operating system that will run applications previously developed for LTX's Delta or Synchro testers. The system also is an enabling technology for creating and managing test intellectual-property software modules that encapsulate test expertise into a library of test methods for use in multiple applications. enVision++ combines the flexibility of the original enVision system with the power of Cadence, LTX's test language for mixed-signal ICs. Additionally, Fusion offers the company's Virtual Test Suite, which allows offline simulation of the total tester environment, so engineers can begin test development before first silicon is available.

Fusion DS is scheduled to be available in the second quarter of this year. Fusion HT is scheduled to be available during this quarter. Call for price information.

LTX Corp.
University Ave.
Westwood, MA 02090-2306
(888) 463-6589
(781) 461-1000
fax (781) 326-4883
www.ltx.com
CIRCLE 471
JOHN NOVELLINO

www.hitex.com

Catch a star from the universe...

Design your embedded application with your favorite chip. Professional tools and expert tips from Hitex make your product development fast and easy. Your product will get off the ground immediately.

We offer entire tool chains for 15 different chip architectures from all leading manufacturers. Typically the tool chain includes Assembler, Compiler, Simulator, Debugger and In-circuit emulator. Free technical support from our experts is included in the one-year warranty period of our emulators.

Starter Kits for many controllers, CAN and USB are available. Check our web pages or contact us to order your free information package now!

...and become one with our tools

Benefit from our world-wide support:

Australia Tel: +61-2-654-1873 · **Austria** Tel: +43-1-2597270/20 · **Belgium** Tel: +31-77-3078438 · **PR China** Tel: +86-10-62383376 · **Czech Republic** Tel: +420-2-66316661 · **Denmark** Tel: +45 43424742 · **France** Tel: +33-1-39611414 · **India** Tel: +91-22-8520817 · **Israel** Tel: +972-3-6492001 · **Italy** Tel: +39-434 640113 · **Japan** Tel: +81-423-71-1121 · **Netherlands** Tel: +31-77-3078438 · **Russia** Tel: +7-812-2646159 · **Singapore** Tel: +65-7496168 · **South Korea** Tel: -82-2-7830022 · **Spain** Tel: +34-1-3194697 · **Sweden** Tel: +46-8-74C4580 · **Switzerland** Tel: +41-1-3086666 · **Taiwan** Tel: +886-2-7057090

hitex

DEVELOPMENT TOOLS

Hitex USA
2055 Gateway Place
Suite 400
San Jose, CA 95110
Tel. (800) 454-4839
Tel. (408) 298-9077
Fax (408) 441-9486
Email info@hitex.com

Hitex Germany
Greschbachstraße 12
D-76229 Karlsruhe
Tel. +49-721 96 28-133
Fax +49-721 96 28-149
Email Int.Sales@hitex.de

Hitex UK
Warwick University,
Science Park
GB-Coventry CV47EZ
Tel. (01203) 692066
Fax (01203) 692131
Email Sales@hitex.co.uk

Hitex Asia
Blk. 3006
Ubi Road 1, #04-386
Singapore 408700
Tel. (65) 7452551
Fax (65) 7454662
Email hitexasia@pacific.net.sg

READER SERVICE 138

Circle 520

Microcontroller Incorporates Eight Interrupts

PAUL A. KEMP
NASA Johnson Space Center, 2101 NASA Rd. 1, Mail Code EP6, Houston, TX 77058; (713) 483-9436; fax (713) 483-1340.

The method presented here provides a microcontroller with eight real-time interrupts instead of just one without giving up any of the processor's standard I/O lines. This design uses a microcontroller's built-in SCI (Serial Communications Interface) to read the eight interrupt status lines. The only requirement is that the SCI provide a clock, data-input line, and an external control line.

A Motorola 68HC811 was used to prototype and test this design. A 74HC165 parallel-to-shift register loads the status of the eight real-time interrupt lines and then serially shifts the data to the microcontroller. The 74HC30 eight-input NAND gate senses all eight interrupts.

Any one or more of the eight interrupt lines going to an active low state will cause the NAND gate to produce an active high signal *(see the figure)*. Then the signal gets inverted and sent to the real-time interrupt pin on the microcontroller (in this case, the 68HC811's XIRQ). At this time, the software instructs the microcontroller to drive its SS (Slave Select) line low, causing the status of the interrupt lines to be loaded into the 74C165. The software then drives the SS line high again and initiates a read of its serial input line (MISO on the 68HC811). Once the status of the eight interrupt lines are read, the software examines the data sequentially to determine which interrupt service routine to execute.

One advantage of this scheme is that multiple interrupts can be captured simultaneously and serviced in terms of priority. IRQ1 is given highest priority in this design, while IRQ8 is given lowest priority. The software written for the 68HC811 also uses the RS-232 interface. It displays the interrupt currently being serviced *(see the listing)*.

VOTE!

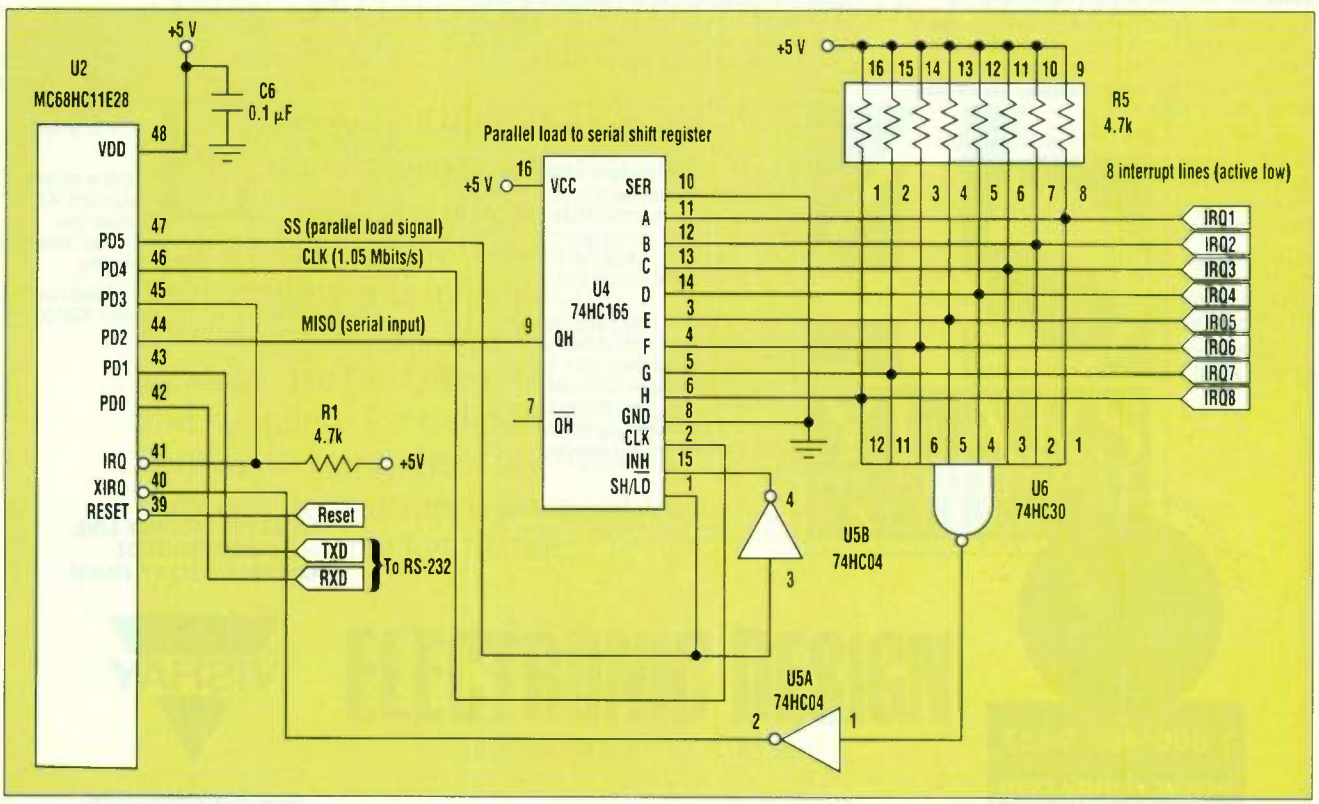
Select your favorite Idea for Design in this issue and circle the appropriate number on the Reader Service Card. The winner receives a $300 Best-of-Issue award.

IDEAS WANTED

Address your Ideas for Design submissions to:

Ideas for Design Editor
Electronic Design
611 Route 46 West
Hasbrouck Heights, NJ 07604

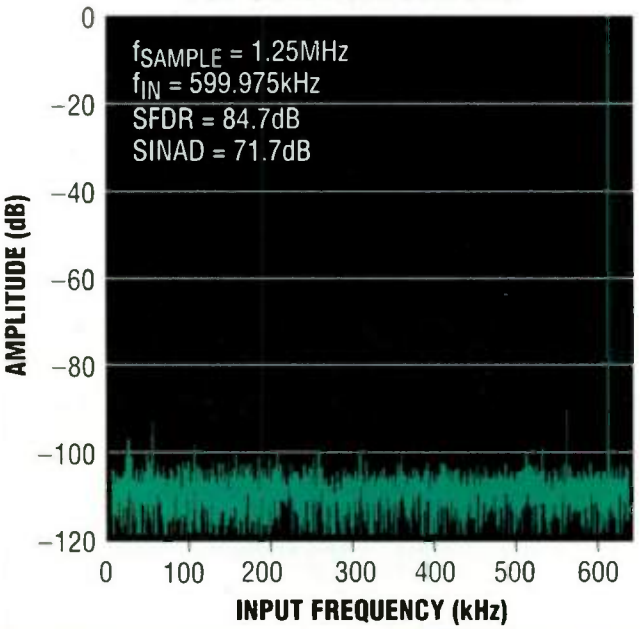
FAX: (201) 393 6242



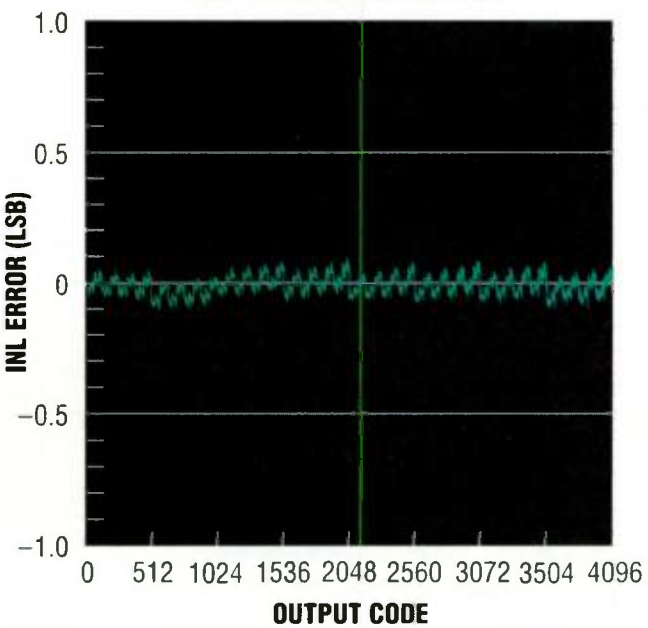
By using the microcontroller's SCI, this design can provide eight real-time interrupts instead of just one without sacrificing any of the standard I/O lines.

Best 12-Bit 1.25Msps ADC.

For Communications



For Instrumentation

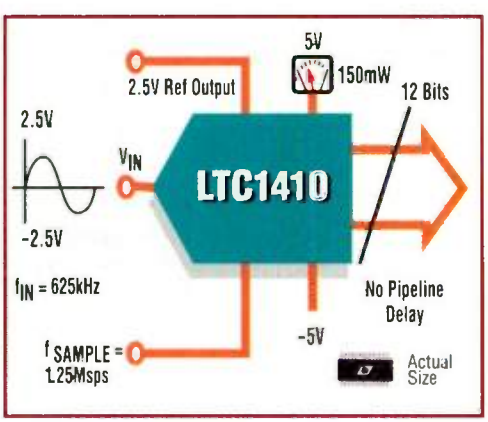


LTC1410: The Best AC Specs for Communications, The Best DC Specs for Instrumentation.

The LTC1410 is the best all-around high speed, 12-bit ADC. Excellent linearity (±1LSB-MAX, INL and DNL) delivers the precision required for instrumentation. Outstanding AC performance and ±2.5V input range maximizes your high-speed communication system's range. Plus a latency-free architecture captures event-driven data without pipeline delay. All this capability for so little!

Features

- 1.25Msps Sampling Rate
- ± 1LSB(MAX) DNL and INL
- 71dB SINAD and 84dB SFDR at Nyquist
- 20MHz Full Power Bandwidth
- Internal or External Reference
- No Pipeline Delay
- 28-Lead SO and SSOP
- Single 5V Supply Available (LTC1415)
- $10.90 Each For 1000-Piece Quantities



Free Sample

Call: 1-800-4-LINEAR
Visit: www.linear-tech.com

Free CD-ROM

Call: 1-800-4-LINEAR

More Information

Lit: 1-800-4-LINEAR
Info: 408-432-1900
Fax: 408-434-0507

LINEAR TECHNOLOGY

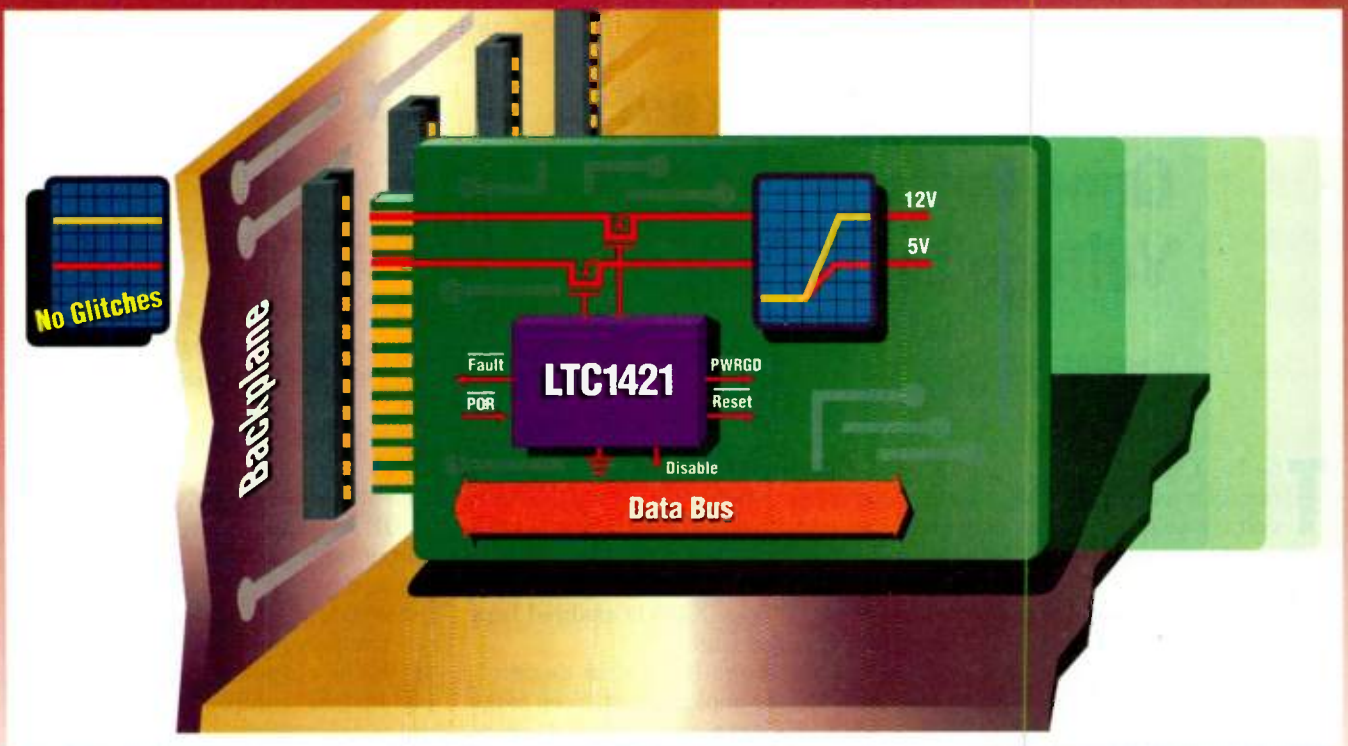
FROM YOUR MIND TO YOUR MARKET
AND EVERYTHING IN BETWEEN

READER SERVICE 148

Data Sheet Download
www.linear-tech.com/go/LTC1410

```
*****************************************************************
*   Program:      8INTs.ASM
*   Author:       Paul A. Kemp
*                 NASA Johnson Space Center
*   Processor:    Motorola M68HC811E2
*
*   This software is used to support the 74HC165 Parallel to Serial Shift
*   Register in serially loading the status of 8 real-time interrupt lines. It
*   sets up the SCI (Serial Communications Interface), provides a case-
*   structured routine for interrogating all 8 interrupt lines and sets up a
*   9600 Baud RS-232 port set for 8 data bits, 1 stop bit and no parity.
*****************************************************************
        include "equ_1000.s"    ;Equates for all 68HC11 internal regs
BEGIN   equ     $F800           ;Beginning of EEPROM

*   PortD Defines the Serial Peripheral Interface to the 74HC165:
*   PD5 Parallel load signal (SS); H = Inhibit, L = Load parallel data
*   PD4 Clock (1 Mbit/s)
*   PD2 Master Input Slave Output. Serial data comes in on this line

********** M68HC811E2 Initialization **********
        org     $F800           ;EPROM starts at F800h
        lds     #$0030          ;Initialize stack in RAM at 0030h
        jsr     DELAY           ;Allow IRMU instrumentation board
                                ;to settle
        ldx     #$1000
        ldaa    #$30
        staa    baud,x          ;Baud rate set for 9600
        ldaa    #$0C
        staa    sccr2,x         ;Async Transmit and Receive enabled
        bclr    sccr1,x,$10     ;Set for 1 start bit, 8 data bits, 1 stop bit
        ldaa    #%00101111
        staa    portd,x         ;Set parallel load line high and clock low
        ldaa    #%00111000
        staa    ddrd,x          ;Configure SPI
        ldaa    #%01011100
        staa    spcr,x          ;SPI = master, E/2 clock,
                                ;CPOL = 1, CPHA = 1
        ldy     #START          ;Point to beginning message
        jsr     SEND            ;Transmit message

********** Main Program **********
MAIN    clra                    ;ACCA <= 00
        clrb                    ;ACCB <= 00
        tap                     ;CCR <= 00 (X bit for XIRQ enabled)
        jmp     MAIN
********** End Main Program **********

********** Send ASCII Character String Subroutine **********
SEND    ldaa    0,y             ;ACCA <= char @ $0000 + (IY)
        brclr   scsr,x,$80,*    ;Wait until TDRE bit has cleared
        staa    scdat,x         ;Serial data register <= character
        iny                     ;IY <= IY + 1
        ldaa    0,y             ;ACCA <= next character
        cmpa    #$04            ;See if last character has been sent
        bne     SEND            ;If last character is alive
                                ;  then send another
        rts

********** Delay Subroutine **********
DELAY   pshx                    ;Stack <= contents of IX
        ldx     #$FFFF
DIM     dex
        bne     DIM
        pulx
        rts

********** IRQ Interrogation Routine **********
XIRQ    bclr    portd,x,$20     ;Drive SS low (load IRQ line status)
        bset    portd,x,$20     ;Drive SS high
                                ;(74HC165 latches data)
        staa    spdat,x         ;Initiate serial data xfer
                                ;by writing to SPDR
WAIT1   ldaa    spsr,x          ;ACCA <= ( SPI Status Reg. )
        bpl     WAIT1           ;read SPSR until SPIF flag is set
        ldab    spdat,x         ;ACCA <= IRQ status information
        bitb    #$01            ;Check to see if bit0 in ACCB is set
        bne     CHK2            ;Branch to check IRQ2 status
        jsr     IRQ1            ;Jump to IRQ1 interrupt service
CHK2    bitb    #$02            ;Check to see if bit1 in ACCB is set
        bne     CHK3            ;Branch to check IRQ3 status
        jsr     IRQ2            ;Jump to IRQ2 interrupt service
CHK3    bitb    #$04            ;Check to see if bit2 in ACCB is set
        bne     CHK4            ;Branch to check IRQ4 status
        jsr     IRQ3            ;Jump to IRQ3 interrupt service
CHK4    bitb    #$08            ;Check to see if bit3 in ACCB is set
        bne     CHK5            ;Branch to check IRQ5 status
        jsr     IRQ4            ;Jump to IRQ4 interrupt service
CHK5    bitb    #$10            ;Check to see if bit4 in ACCB is set
        bne     CHK6            ;Branch to check IRQ6 status
        jsr     IRQ5            ;Jump to IRQ5 interrupt service
CHK6    bitb    #$20            ;Check to see if bit5 in ACCB is set
        bne     CHK7            ;Branch to check IRQ7 status
        jsr     IRQ6            ;Jump to IRQ6 interrupt service
CHK7    bitb    #$40            ;Check to see if bit6 in ACCB is set
        bne     CHK8            ;Branch to check IRQ8 status
        jsr     IRQ7            ;Jump to IRQ7 interrupt service
CHK8    bitb    #$80            ;Check to see if bit7 in ACCB is set
        bne     DONE            ;Done interrogating interrupt status
        jsr     IRQ8            ;Jump to IRQ8 interrupt service
DONE    ldaa    #%00101111
        staa    portd,x         ;Set parallel load line high, clock low
        rti                     ;Return from interrupt

********** IRQ1 Subroutine **********
IRQ1    ldy     #IRQ?
        jsr     SEND            ;Send IRQ service message
        ldaa    #'1'            ;ACCA <= ASCII "1"
        brclr   scsr,x,$80,*    ;Wait until TDRE bit has cleared
        staa    scdat,x         ;Serial data register <= character
        jsr     DELAY
        rts

********** IRQ2 Subroutine **********
IRQ2    ldy     #IRQ?
        jsr     SEND            ;Send IRQ service message
        ldaa    #'2'            ;ACCA <= ASCII "2"
        brclr   scsr,x,$80,*    ;Wait until TDRE bit has cleared
        staa    scdat,x         ;Serial data register <= character
        jsr     DELAY
        rts

********** IRQ3 Subroutine **********
IRQ3    ldy     #IRQ?
        jsr     SEND            ;Send IRQ service message
        ldaa    #'3'            ;ACCA <= ASCII "3"
        brclr   scsr,x,$80,*    ;Wait until TDRE bit has cleared
        staa    scdat,x         ;Serial data register <= character
        jsr     DELAY
        rts

********** IRQ4 Subroutine **********
IRQ4    ldy     #IRQ?
        jsr     SEND            ;Send IRQ service message
        ldaa    #'4'            ;ACCA <= ASCII "4"
        brclr   scsr,x,$80,*    ;Wait until TDRE bit has cleared
        staa    scdat,x         ;Serial data register <= character
        jsr     DELAY
        rts

********** IRQ5 Subroutine **********
IRQ5    ldy     #IRQ?
        jsr     SEND            ;Send IRQ service message
        ldaa    #'5'            ;ACCA <= ASCII "5"
        brclr   scsr,x,$80,*    ;Wait until TDRE bit has cleared
        staa    scdat,x         ;Serial data register <= character
        jsr     DELAY
        rts

********** IRQ6 Subroutine **********
IRQ6    ldy     #IRQ?
        jsr     SEND            ;Send IRQ service message
        ldaa    #'6'            ;ACCA <= ASCII "6"
        brclr   scsr,x,$80,*    ;Wait until TDRE bit has cleared
        staa    scdat,x         ;Serial data register <= character
        jsr     DELAY
        rts

********** IRQ7 Subroutine **********
IRQ7    ldy     #IRQ?
        jsr     SEND            ;Send IRQ service message
        ldaa    #'7'            ;ACCA <= ASCII "7"
        brclr   scsr,x,$80,*    ;Wait until TDRE bit has cleared
        staa    scdat,x         ;Serial data register <= character
        jsr     DELAY
        rts

********** IRQ8 Subroutine **********
IRQ8    ldy     #IRQ?
        jsr     SEND            ;Send IRQ service message
        ldaa    #'8'            ;ACCA <= ASCII "8"
        brclr   scsr,x,$80,*    ;Wait until TDRE bit has cleared
        staa    scdat,x         ;Serial data register <= character
        jsr     DELAY
        rts
```

Hot Swap Safely!



LTC1421: It works on either side of the connector!

The LTC1421 Hot Swap™ controller handles up to 4 supplies during live insertion, limiting inrush current by ramping the supplies at a programmable rate. It provides protection for electronic circuit-breaker applications. Connection sense insures the board is seated before supplies ramp and the data bus is disabled until the supplies are valid. The LTC1422 controls a single supply in an SO-8 package.

Features

- Up to 4 Supply Voltages with 1 Chip
- Can Operate in -48V Supply System
- User-programmable Switch Turn-on Time
- Connection Inputs Detect Board Insertion or Removal
- Programmable Electronic Circuit Breaker
- Power-On Reset
- $4.90 Each for 1000-Piece Quantities (LTC1421)

Available in SO-8

Free Samples

Call: 1-800-4-LINEAR
Visit: www.linear-tech.com

Free CD-ROM

Call: 1-800-4-LINEAR

More Information

Lit: 1-800-4-LINEAR
Info: 408-432-1900
Fax: 408-434-0507

LT, LTC and LT are registered trademarks and Hot Swap is a trademark of Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417

LINEAR TECHNOLOGY

FROM YOUR MIND TO YOUR MARKET
AND EVERYTHING IN BETWEEN

READER SERVICE 149

```
********* Begin Variable/ASCII String Data Area **********************
START   fcb     13T,10T,
                '8 Real-Time Serially Multiplexed Interrupts',$04
IRQ?    fcb     13T,10T,'Now servicing IRQ',$04
********* End Variable/ASCII String Data Area ************************

                org     $FFF4
                fdb     XIRQ        ;Address for XIRQ subroutine
                fdb     BEGIN,BEGIN,BEGIN,BEGIN,BEGIN
*
*               10T = ASCII Line Feed
*               13T = ASCII Carriage Return
```

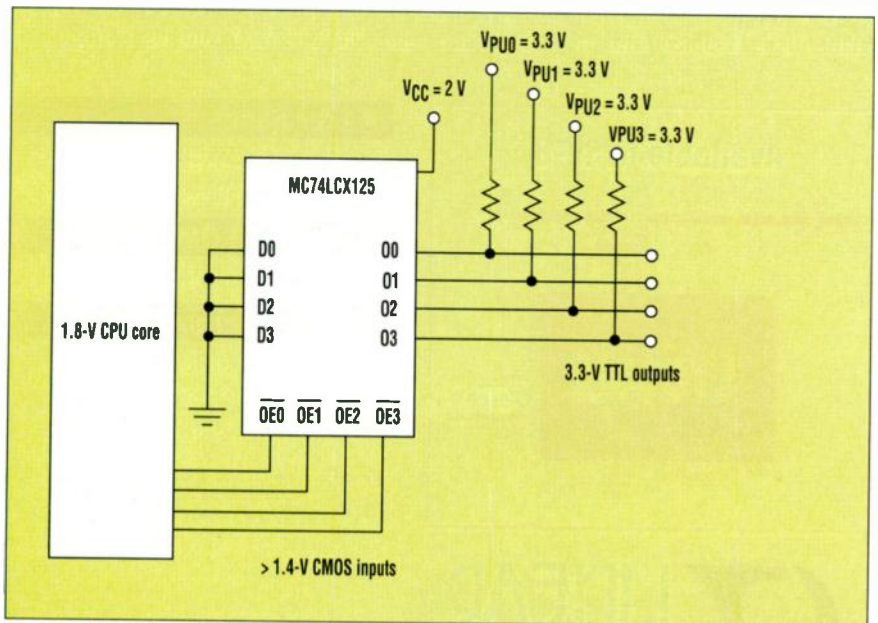

Overvoltage-Tolerant Quad Buffer Used As Voltage Level Shifter

LANCE PACKER
Motorola Inc., Semiconductor Components Group,
2501 South Price Rd., G375, Chandler, AZ 85248.

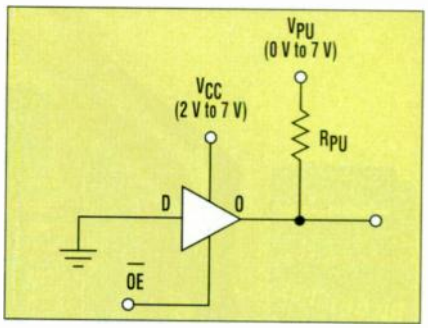
The LCX standard logic product family was designed with overvoltage-tolerant inputs and outputs, enabling users to easily interface LVTTL and 5-V TTL buses. Because the LCX outputs are overvoltage-tolerant when disabled, system designers can take advantage of this overvoltage tolerance to design a nifty and inexpensive voltage level shifter. With all of the mixed voltage designs in the world today, there may be several different voltage interfaces or bridges required on a single board (e.g., 3 V to 5 V, 1.8 V to 3 V, etc.).

The MC74LCX125 is a quad buffer with overvoltage-tolerant inputs and outputs. Because each of the four bits have individual output-enable pins, they can be enabled/disabled separately. The LCX125 is enabled Low and disabled High.

The voltage-level-shift design is very simply implemented. Each of the LCX125 data inputs are tied to ground *(Fig. 1 and Fig. 2)*. The outputs are tied to a chosen pull-up voltage (or various voltages) through separate pull-up resistors (values can be mixed or matched depending on desired speed/power requirements).



1. In this level-shifter configuration, signals from the 1.8-V CPU core are translated to allow interfacing with a 3.3-V TTL-level peripheral bus.



2. Here, one bit of the MC74LCX125 quad buffer is set up as a level-shifter.

The output enable ($\overline{OE}$) inputs are substituted for the data inputs. When an $\overline{OE}$ input is Low, the corresponding output is enabled *(see the table)*. Since the input pin is tied to ground, the output is pulled Low (by the LCX125 output transistor). When the $\overline{OE}$ input is High, the output is disabled and the pull-up takes control. Because the output is overvoltage-tolerant, the pull-up voltage can be taken as high as 7 V (absolute maximum rating on a disabled LCX output) without causing any stress on the part or any unwanted loading at the interface.

Though LCX reliability with a disabled output isn't guaranteed beyond 7 V, the LCX125 level shifter could actually function well beyond 7-V pull-up. The minimum recommended operating voltage is 2 V for an LCX part. Therefore, by using the MC74LCX125, level shifting can be accomplished for various power supplies and pull-up voltages from 0 to 7 V. The pull-up voltage can be greater than or less than the supply voltage. The supply voltage for the LCX125 should be kept between 2.0 and 5.5V. LCX is CMOS, so the V_{IH} levels must be kept greater than 70% of V_{CC} (1.4V min for V_{CC} =2V). The minimum accepted input voltage is 1.4 V, while 7 V is the maximum input voltage. The outputs depend on the pull-up voltage, and can be anything between 0 and 7 V.

Briefly mentioned above was the user's ability to control the speed of

REDUNDANT POWER

REDUNDANT POWER

MP1350 Series

- -48V/25A
- +24V/50A
- 110/220VAC Input
- 5.25" (3U) Height

MP3600 Series

- -48V/65A
- +24V/125A
- 220VAC Input
- 7" (4U) Height
- 16" Depth
- DC-DC Models

MP Series Features

- Power Factor Correction
- Active Current Sharing
- Hot Bus Plug-In
- Monitoring and Alarms
- Optional Metering
- Racking Systems
- Standard Products
- Tailored Solutions

MODULAR POWER SYSTEMS

36 Newburgh Road
Hackettstown, NJ 07840

Phone: 908-850-5088

www.transdev.com
info@mailer.transdev.com

Fax: 908-850-1607

A Division of Transistor Devices, Inc.

CERTIFIED ISO 9001 QUALITY SYSTEM

READER SERVICE 200

the "propagation delay" from a Low level to a High level (it's actually a Low to High impedance or t_{PLZ}), and the amount of current through the pull-up resistor when the output is static Low. The speed of Low-to-High transition is based entirely on the RC load on the disabled output.

The higher the resistor value (and capacitance value), the longer the delay and lower the current. The lower the pull-up resistance, the faster the switch, but the static Low current increases. There is zero current in the case of a static High level, regardless of the pull-up resistance, so the design could be maximized based on that knowledge. The static output current (I_{OL}) is simply the pull-up voltage (V_{PU}) minus the static low voltage (V_{OL}) divided by the pull-up resistor value (R_{PU}): $I_{OL} = (V_{PU} - V_{OL})/R_{PU}$.

The High-to-Low transition depends on the ability of the MC74LCX125 to quickly sink the I_{OL} current. The LCX125 is specified to sink a minimum current of 24 mA (at V_{CC} = 3 V). This is a static specification. The dynamic switching capability is much greater.

Testing of the ac parameters shows delays of about 9 to 11 ns for the t_{PLZ} with a 250-Ω pull-up resistor and 50-pF load. The output is measured at 50% V_{CC}, regardless of the V_{CC}. The delay varied little due to the supply voltage or the pull-up voltage. The t_{PZL} varies substantially with power supply voltage and pull-up voltage. The delay was faster at lower pull-up voltages and, of course, faster with an increase of supply voltage. Depending on the voltage conditions, the measured values are 2.4 to 11.8 ns. The 2.4-ns result was measured with V_{CC} = 5.0 V and V_{PU} = 1.5 V. The slowest delay was measured with V_{CC} = 1.8 V and V_{PU} = 6.0 V.

An MC74LCX125-based voltage level shifter application is flexible in design and easy to implement. The voltages, currents and propagation delays are almost entirely left to the discretion of the designer.

Circle 522

Build An Improved, Simpler Finite State Machine

STEVE CLARK
Cambex Corp., 360 Second Ave., Waltham, MA 02154.

The two improvements suggested here pertain to the "*Build a Simple Finite State Machine*" Idea for Design submitted by Giovanni Romeo (ELECTRONIC DESIGN, *July 7, 1997, p. 149*). First of all, the schematic doesn't show a register latch on the EPROM inputs. The outputs of a 27C256 EPROM will exhibit glitches during transitions of the inputs. With the free-running clock shown in the schematic, the output register will occasionally catch these glitches. This causes state-machine failures if the inputs aren't synchronized to the clock.

Secondly, there doesn't seem to be much reason for this application to invent a state machine language as described in the text. The following C code implements the function described in the article *(see the listing)*. The code is simpler to understand, and took less than an hour to write and debug. It was compiled under Borland C 3.1.

```
//
//Improved Finite State Machine
// author: Steve Clark

#include <stdio.h>

// define legal state values
#define  S_STOP    0x00
#define  S_UP1     0x08
#define  S_UP2     0x04
#define  S_UP3     0x02
#define  S_UP4     0x01
#define  S_DOWN1   0x11
#define  S_DOWN2   0x12
#define  S_DOWN3   0x14
#define  S_DOWN4   0x18

// define legal input values
#define  I_UP      0x2
#define  I_DN      0x1

main()
{
    long i, cur-state, in, next_state;
    int c;
    FILE *fil;

    fil = fopen( "eprom.bin" , "w" );

    for (i=0; i<32768L; i++)
      {

       cur_state = (i & 0xFF);
       in = (i >> 8L);

switch (cur_state) {

    case S_STOP:
      if (in == I_UP) next_state = S_UP1;
      else if (in == I_DN) next_state=S_DOWN1;
      else next_state = S_STOP;
      break;

    case S_UP1:
      if (in == I_UP) next_state = S_UP2;
      else if (in == I_DN) next_state=S_DOWN2;
      else next_state S_STOP;
      break;

    case S_UP2:
      if (in == I_UP) next_state = S_UP3;
      else if (in == I_DN) next_state=S_DOWN4;
      else next_state S_STOP;
      break;

    case S_UP3:
      if (in == I_UP) next_state = S_UP4;
      else if (in == I_DN) next_state=S_DOWN3;
      else next_state = S_STOP;
      break;

    case S_UP4:
      if (in == I_UP) next_state = S_UP1;
      else if (in == I_DN) next_state=S_DOWN2;
      else next_state = S_STOP;
      break;

    case S_DOWN1:
      if (in == I_UP) next state = S_UP1;
      else if (in I_DN) next_state = S_DOWN2;
      else next_state = S_STOP;
      break;

    case S_DOWN2:
      if (in == I_UP) next_state = S_UP4;
      else if (in == I_DN) next_state = S_DOWN3;
      else next_state = S_STOP;
      break;

    case S DOWN3:
      if (in == I_UP) next_state = S_UP1;
      else if (in == I_DN) next_state = S_DOWN2;
      else next_state = S_STOP;
      break;

    case S_DOWN4:
      if (in == I_UP) next_state = S_UP2;
      else if (in == I_DN) next_state = S_DOWN2;
      else next_state S_STOP;
      break;

    default:
      next_state = S_STOP;
    }
    // convert to 8-bit binary value
    c = next_state;
    putc (c, fil);
  }
  fclose(fil);
}
```

WORLD'S LOWEST POWER SOT RESET ICs CONSUME ONLY 500nA!

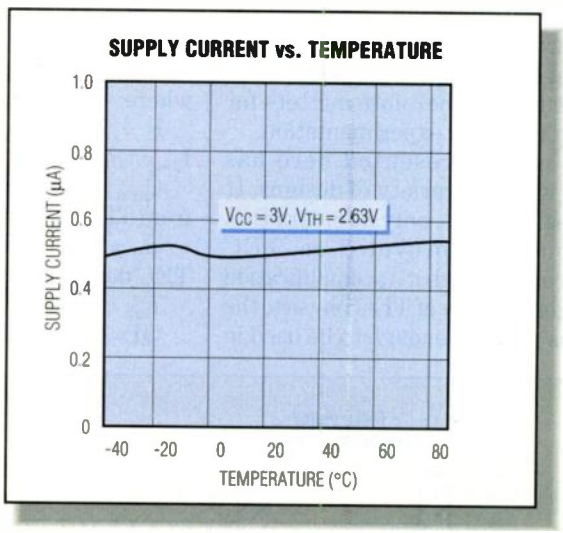
Perfect for Portable Equipment and Battery-Operated Systems

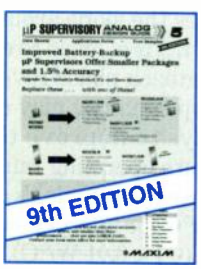
Save space and enhance the battery life of your portable 3V/3.3V system with the MAX6326/MAX6327/MAX6328. These precision power-on reset ICs consume only 500nA supply current over temperature. Reset threshold voltages are available from 2.63V to 3.08V, in approximately 100mV increments. Look for lower reset threshold voltages in the future.

- **500nA Supply Current**
- **Precision 140ms Timeout Delay**
- **No External Components Required**
- **Precision Monitoring of 3V and 3.3V Power-Supply Voltages**
- **Fully Specified Over Temperature**
- **Guaranteed $\overline{\text{RESET}}$ Valid to V_{CC} = 1V**
- **Pin-Compatible with MAX809/MAX810**
- **3-Pin SOT23 Package**
- **Low Cost**

PART	ACTIVE-LOW $\overline{\text{RESET}}$	ACTIVE-HIGH RESET	OPEN-DRAIN $\overline{\text{RESET}}$
MAX6326	✓		
MAX6327		✓	
MAX6328			✓

1) Contact factory for minimum order quantities.
2) Sample quantities are generally held for the following versions: MAX6326UR31, MAX6326UR29, MAX6326UR26, MAX6327UR31, MAX6327UR29, MAX6327UR26, MAX6328UR31, MAX6328UR29, MAX6328UR26.





FREE* µP Supervisory Design Guide—*Sent Within 24 Hours!
Includes: Data Sheets and Cards for Free Samples

CALL TOLL-FREE 1-800-998-8800 for a Design Guide or Free Sample
For Small-Quantity Orders Call (408) 737-7600 ext. 3468
6:00 a.m. – 6:00 p.m. Pacific Standard Time
http://www.maxim-ic.com

MAXIM

NOW AVAILABLE!
FREE FULL LINE DATA CATALOG ON CD-ROM

For Small-Quantity Orders Call (408) 737-7600 ext. 3468

MasterCard® and Visa® are accepted for evaluation kits and small-quantity orders.

Distributed by Allied, Arrow, Bell, CAM RPC, Digi-Key, Elmo, Hamilton Hallmark, Nu Horizons, and Zeus. Distributed in Canada by Arrow.

Austria, Maxim GmbH (Deutschland); **Belgium**, Master Chips; **Czech Republic**, Spezial-Electronic KG; **Denmark**, Arrow-Exatec A/S; **Finland**, Berendsen Components Oy; **France**, Maxim France, *Distributors:* Maxim Distribution, ASAP; **Germany**, Maxim GmbH, *Distributors:* Maxim Distribution, Spezial Electronic GmbH; **Ireland**, FMG Electronics; **Italy**, Maxim Italy, *Distributor:* Esco Italiana Electronics Supply; **Netherlands**, Koning En Hartman; **Norway**, Berendsen Electronics; **Poland**, Uniprod, Ltd.; **Portugal**, ADM Electronics, S.A.; **Russia**, Spezial-Electronic KG; **Spain**, Maxim Distribución, ADM Electronics S.A.; **Sweden**, Egevo AB; **Switzerland**, Maxim Switzerland, Laser & Electronics AG; **Turkey**, Interex (U.S.A.); **U.K.**, Maxim Integrated Products (U.K.), Ltd., *Distributors:* Maxim Distribution (U.K.), Ltd., 2001 Electronic Components, Eurodis HB Electronics; **Ukraine**, Spezial-Electronic KG.

Circle No. 155 - For U.S. Response
Circle No. 156 - For International

Circle 523

Simple Design Equations For Thermoelectric Coolers

W. STEPHEN WOODWARD
Venable Hall, CB3290, University of North Carolina, Chapel Hill, NC 27599-3290; e-mail: woodward@net.chem.unc.edu.

Thermoelectric coolers (TECs) are versatile temperature control devices . They're best thought of as solid-state heat pumps in which the direction and rate of heat flow can be manipulated by controlling the magnitude and polarity of the TEC drive current—the "Peltier Effect." Trouble is, simple and accurate (or even usefully approximate) design equations for TECs are hard to find. TEC selection, sizing of heatsinks, and design of control circuits are therefore matters for guesswork and/or experimentation.

The model presented here has served well in a variety of designs. It requires, as input, only numbers that are routinely provided in TEC datasheets. Though it's a simplification of the gory details of TEC physics, the model is realistic enough to be used in most TEC design applications.

The model predicts TEC thermal load temperature (T1) as a function of load heat production, TEC data-sheet numbers, heatsink parameters, TEC drive current, and ambient temperature (T3). It looks like this:

$$T1 = (-P*I_{tec} + I_{tec}^2*R_p/2 + Q1)/(C1 + C_p) + (Q1 + I_{tec}^2*R_p)/(C_h + T3)$$

where:

P = Peltier constant = $(Q_{max} + I_{max}^2*R_p/2)/I_{max}$

Q_{max} = maximum heat transfer from TEC data sheet (watts)

R_p = TEC resistance = V_{max}/I_{max} = TEC data sheet drive ratings

I_{tec} = TEC drive current (amperes)

Q1 = heat produced by thermal load (watts)

C1 = conductivity (watts/°C) of thermal load to ambient

C_p = TEC thermal conductivity = $Q_{max}/\Delta T_{max}$ from TEC data sheet

C_h = heatsink thermal conductivity to ambient

T3 = ambient temperature

Typical TEC design example numbers might come from a Melcor (Trenton, N.J.) type "F 0.45-32-05": P = 4.07 W/A, R_p = 4.8 Ω, C_p = 0.026 W/°C. If we assume a routine application in which a zero-dissipation load such as a photovoltaic detector (Q1 = 0 W, C1 = 0.01 W/°C) needs to be thermostatted at 0°C, a good question might be: Suppose we select a moderate-sized heatsink with C_h = 0.2 W/°C. What is the warmest ambient temperature against which the 0° setpoint can be held? Plugging these numbers into the model, the equation predicts that T3 = ∪35.2°C at I_{tec} = 0.62 A will be the limit.

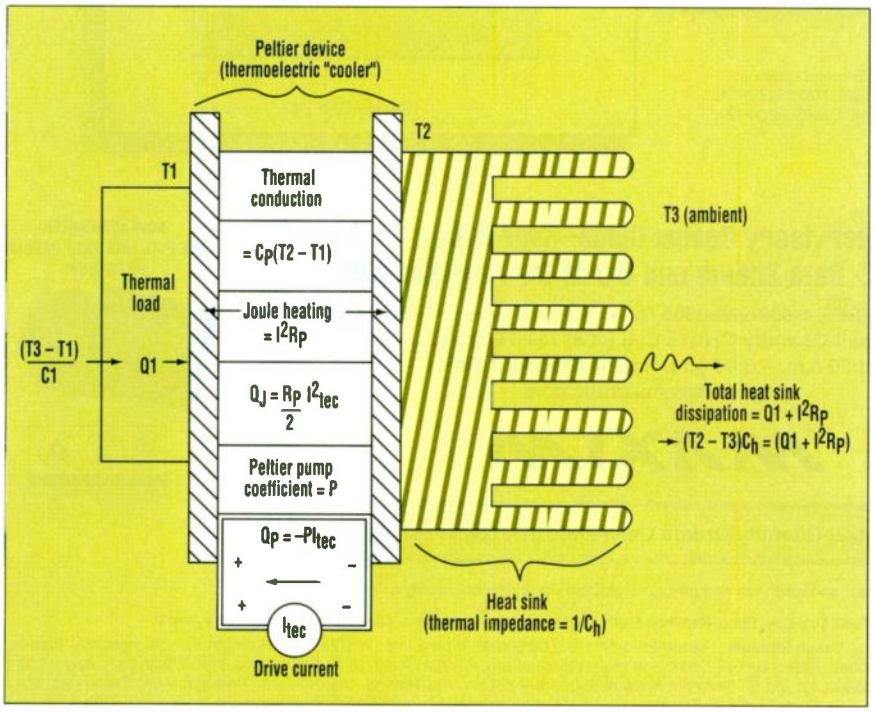
But what if the system needs to operate in warmer (T3 ∪ 40°C) ambients? Melcor rates this TEC (I_{max}) for 0.8 A and a ΔT of up to 67°C. Can't we hold the setpoint against hotter ambients just by driving the TEC a little harder than 0.62 A?

Surprisingly, the answer is a resounding "No!" If I_{tec} increases from 0.62 A to 0.8 A, the heatsink will warm up by approximately 8°C and overwhelm the effect of additional Peltier heat transport. Consequently, T1 will move in the wrong direction and actually *rise* by 3°C. In this example, T1 versus I_{tec} reverses the slope around I_{tec} = 0.62 A, and if I_{tec} is allowed to exceed this limit, feedback phase reversal and control-loop runaway may occur. The only ways to improve the ambient temperature operating range are to either increase the heatsink's capacity (C_h > 7.2 W/°C) or improve load thermal insulation (C1 < 0.01 W/°C).

Actually, an important prediction (and little-known fact) that comes out of this model is that reversal of the steady-state T1 versus I_{tec} relation at:

$$I_{tec} = (P*C_h)/\{R_p[C_h + 2(C1 + C_p)]\}$$

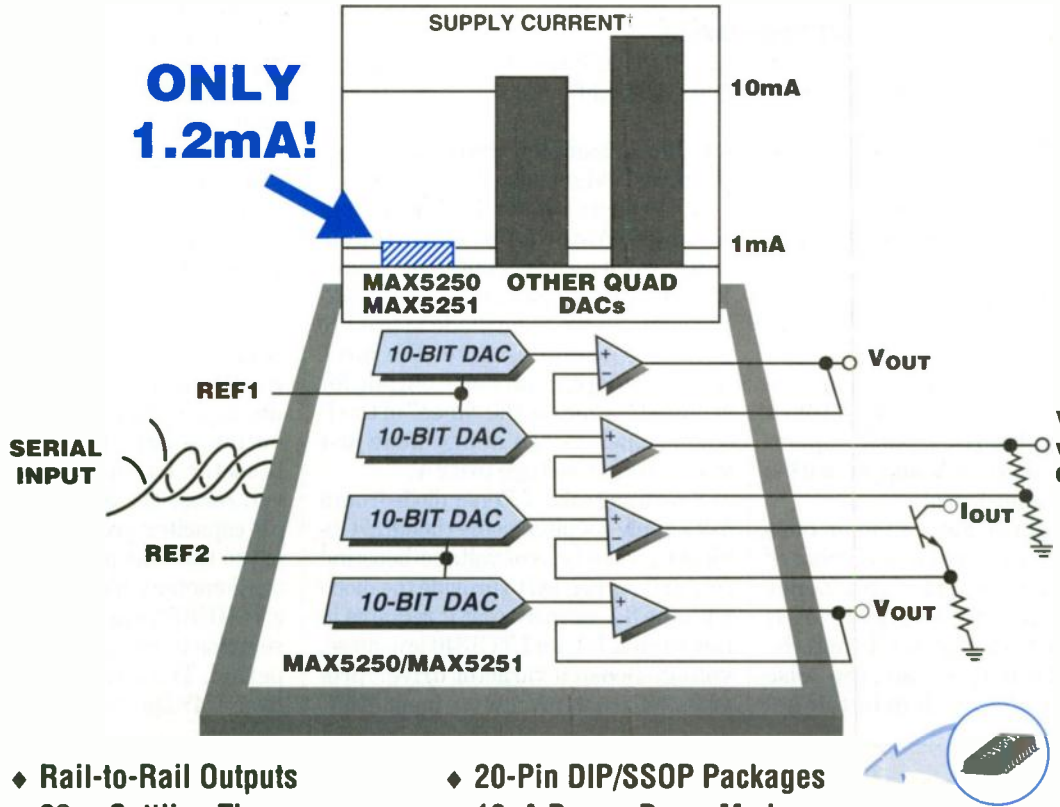
will occur for all load/TEC/heatsink combinations. It's critical to limit I_{tec} to this maximum-cooling value. Otherwise, the risk of thermostat latchup will always be lurking around.



Useful in most thermoelectric-cooler (TEC) design applications, this simplified model of TEC physics and its accompanying equations provide a more practical approach to the troublesome problems of TEC selection, sizing of adequate heatsinks, and control-circuit design.

10-BIT QUAD DACs CUT CURRENT BY 10x

3V and 5V DACs Use Less Than 300µA/DAC for Instrumentation and Communications



- Rail-to-Rail Outputs
- 20µs Settling Time
- Power-On Reset
- 20-Pin DIP/SSOP Packages
- 10µA Power-Down Mode
- +3V (MAX5251) and +5V (MAX5250) Operation

For lowest power 10-bit applications, select the +5V MAX5250 or the +3V MAX5251 quad DAC for your next design. These devices require less than 300µA/DAC, and feature power-on reset, rail-to-rail outputs, power-down, and direct access to the amplifier's inverting input (for varied output configurations).

† Supply current includes the external reference current for MAX5250/1.

FREE* D/A Converter Design Guide—*Sent Within 24 Hours!

Includes: Data Sheets and Cards for Free Samples

CALL TOLL-FREE 1-800-722-8266 for a Design Guide or Free Sample
For Small-Quantity Orders Call (408) 737-7600 ext. 3468
6:00 a.m. – 6:00 p.m. Pacific Standard Time
http://www.maxim-ic.com

MasterCard® and Visa® are accepted for evaluation kits and small-quantity orders.

NOW AVAILABLE!
FREE FULL LINE DATA CATALOG ON CD-ROM

MAXIM

Distributed by Allied, Arrow, Bell, CAM RPC, Digi-Key, Elmo, Hamilton Hallmark, Nu Horizons, and Zeus. Distributed in Canada by Arrow.

Austria, Maxim GmbH (Deutschland); **Belgium**, Master Chips; **Czech Republic**, Spezial-Electronic KG; **Denmark**, Arrow-Exatec A/S; **Finland**, Berendsen Components Oy; **France**, Maxim France, *Distributors*: Maxim Distribution, ASAP; **Germany**, Maxim GmbH, *Distributors:* Maxim Distribution, Spezial Electronic GmbH; **Ireland**, FMG Electronics; **Italy**, Maxim Italy, *Distributor:* Esco Italiana Electronics Supply; **Netherlands**, Koning En Hartman; **Norway**, Berendsen Electronics; **Poland**, Uniprod, Ltd.; **Portugal**, ADM Electronics, S.A.; **Russia**, Spezial-Electronic KG; **Spain**, Maxim Distribución, ADM Electronics S.A.; **Sweden**, Egevo AB; **Switzerland**, Maxim Switzerland, Laser & Electronics AG; **Turkey**, Interex (U.S.A.); **U.K.**, Maxim Integrated Products (U.K.), Ltd., *Distributors:* Maxim Distribution (U.K.), Ltd., 2001 Electronic Components, Eurodis HB Electronics; **Ukraine**, Spezial-Electronic KG.

Circle No. 157 - For U.S. Response
Circle No. 158 - For International

Circle 524

Single-Supply Random Code Generator

RICHARD MARKELL
Linear Technology Corp., 1630 McCarthy Blvd., Milpitas, CA 95035-7417; (408) 432-1900; fax (408) 434-0507.

With the proliferation of satellite receivers, cable systems, and Internet commerce, there's a real need for secure encryption. A pseudorandom code generator that filled the bill several years ago is now considered "hackable" by many knowledgeable people.

Presented here is a truly random code generator that operates from a single supply. The circuit allows operation from a single 5-V supply with a minimum of adjustments.

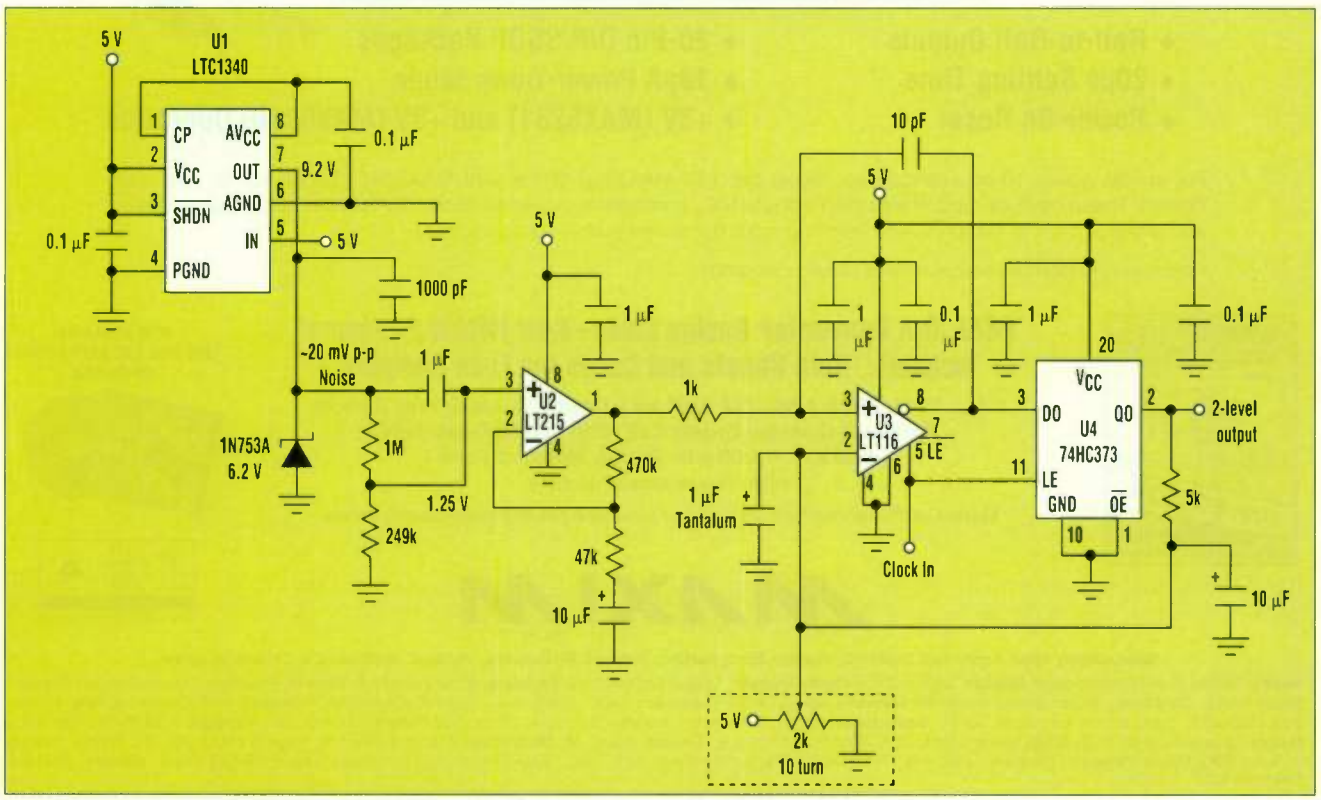
The circuit produces random ones and zeros by comparing a stream of random noise generated in a Zener diode to a reference voltage level. If the threshold is set correctly and the time period is long enough, the noise will consist of a random but equal number of samples above and below the threshold setting.

The circuit shown is the random noise generator *(Fig. 1)*. Optimum noise performance is obtained from a 1N753A Zener diode, which has a 6.2-V Zener "knee." The diode is used to generate random noise. We have found that optimum noise output for this diode occurs at the "knee" of the I-V curve, where the Zener diode just starts to limit voltage to 6.2 V.

Operating a 6.2-V Zener diode from a 5-V supply required some thought. Obviously, some type of voltage-boosting scheme was needed to provide the diode with the 8 V or more that it requires in this circuit. U1, an LTC1340 low-noise, voltage-boosted varactor driver, provides 9.2 V at 20 µA from an input of 5 V. This is the optimal Zener current for noise output from the diode (at 20 µA the output is about 20 mV p-p).

The 1M and 249k resistors bias the input to op amp U2 to 1.25 V to match the input common-mode range of comparator U3. The 1-µF capacitor provides an ac path for the noise. Note: Be careful where you place any additional capacitors in this part of the circuit, or the noise may be unintentionally rolled off. This is one circuit where noise is desirable.

U2 is an LT1215 23-MHz, 50-V/µs dual op amp that can operate from a single supply. It's used as a wideband, gain-of-eleven amplifier to amplify the noise from the Zener diode. U3, an LT1116 high-speed, ground-sensing comparator, receives the noise at its positive input. A threshold is set at the negative comparator input and the output is adjusted via the 2k potentiometer for an equal number of ones and zeros. The 5k resistor and the 10-µF capacitor provide limited hysteresis so that the adjustment of the potentiometer isn't as critical. Latch U4, a 74HC373, ensures that the output remains latched throughout one clock period. The circuit's output is taken from U4's Q0 output.

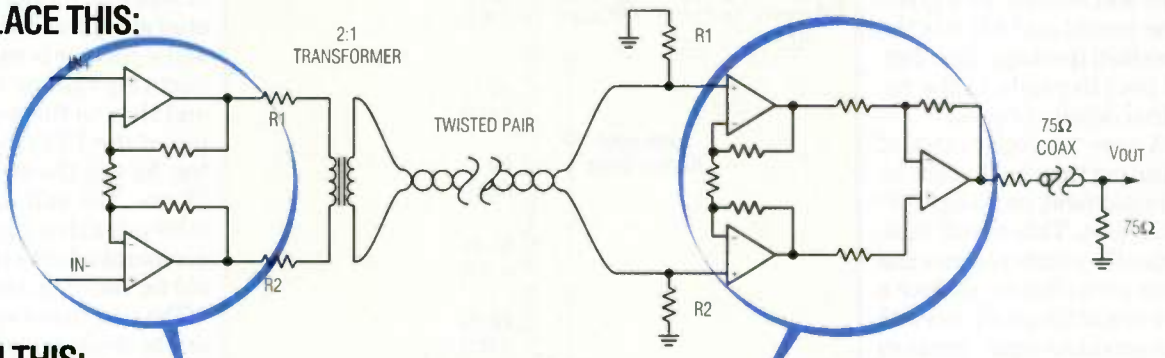


1. This truly random code generator operates from a single 5-V supply, and requires minimal adjustments.

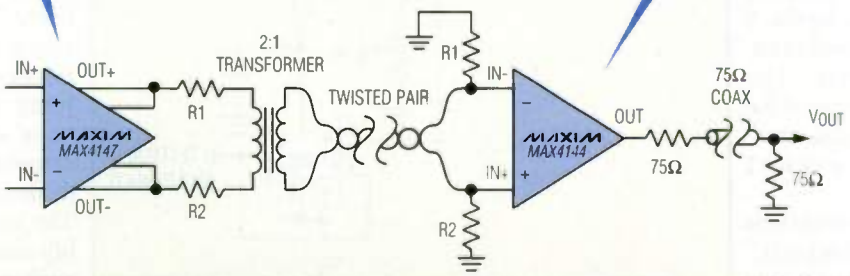
NEW LINE DRIVERS AND RECEIVERS SIMPLIFY VIDEO, RF/IF TRANSMISSION

Ideal for Noise-Immune Interconnection of Signals Over Twisted Pair

REPLACE THIS:



WITH THIS:



Eliminate 12 Extra Components with Maxim's Small Line Drivers and Receivers

DIFFERENTIAL LINE DRIVERS									
PART	-3dB GAIN FLATNESS (MHz)	0.1dB GAIN FLATNESS (MHz)	SLEW RATE (V/µs)	SFDR @ 10kHz (dBc)	CMR @ 10MHz (dB)	DG/DP ERROR (%/°)	OUTPUT CURRENT DRIVE (mA)	PACKAGE	PRICE† ($)
MAX4142*	300	70	2700	-82	70	0.008/0.03	80	14 SO	2.50
MAX4147	300	70	2000	-82	70	0.008/0.03	160	14 SO	2.50
DIFFERENTIAL LINE RECEIVERS									
PART	-3dB GAIN FLATNESS (MHz)	0.1dB GAIN FLATNESS (MHz)	SLEW RATE (V/µs)	SFDR @ 10kHz (dBc)	CMR @ 10MHz (dB)	DG/DP ERROR (%/°)	VOLTAGE NOISE DENSITY (nV/√Hz)	PACKAGE	PRICE† ($)
MAX4144	130	30	1000	-90	70	0.03/0.03	12	14 SO	2.40
MAX4145	180	90	600	-92	75	0.01/0.06	3.8	14 SO	2.40
MAX4146	70	50	800	-82	90	0.12/0.07	3.5	14 SO	2.40

*Future product—contact factory for availability. †1000-up recommended resale, FOB USA.

FREE* Op Amp/Video Design Guide—*Sent Within 24 Hours!

Includes: Data Sheets and Cards for Free Samples

CALL TOLL-FREE 1-800-376-6650 for a Design Guide or Free Sample
For Small-Quantity Orders Call (408) 737-7600 ext. 3468
6:00 a.m. – 6:00 p.m. Pacific Standard Time
http://www.maxim-ic.com

MasterCard® and Visa® are accepted for evaluation kits and small-quantity orders.

NOW AVAILABLE!
FREE FULL LINE DATA CATALOG
ON CD-ROM

MAXIM

Distributed by Allied, Arrow, Bell, CAM RPC, Digi-Key, Elmo, Hamilton Hallmark, Nu Horizons, and Zeus. Distributed in Canada by Arrow.

Austria, Maxim GmbH (Deutschland); **Belgium**, Master Chips; **Czech Republic**, Spezial-Electronic KG; **Denmark**, Arrow-Exatec A/S; **Finland**, Berendsen Components Oy; **France**, Maxim France, *Distributors:* Maxim Distribution, ASAP; **Germany**, Maxim GmbH, *Distributors:* Maxim Distribution, Spezial Electronic GmbH; **Ireland**, FMG Electronics; **Italy**, Maxim Italy, *Distributor:* Esco Italiana Electronics Supply; **Netherlands**, Koning En Hartman; **Norway**, Berendsen Electronics; **Poland**, Uniprod, Ltd.; **Portugal**, ADM Electronics, S.A.; **Russia**, Spezial-Electronic KG; **Spain**, Maxim Distribución, ADM Electronics S.A.; **Sweden**, Egevo AB; **Switzerland**, Maxim Switzerland, Laser & Electronics AG; **Turkey**, Interex (U.S.A.); **U.K.**, Maxim Integrated Products (U.K.), Ltd., *Distributors:* Maxim Distribution (U.K.), Ltd., 2001 Electronic Components, Eurodis HB Electronics; **Ukraine**, Spezial-Electronic KG.

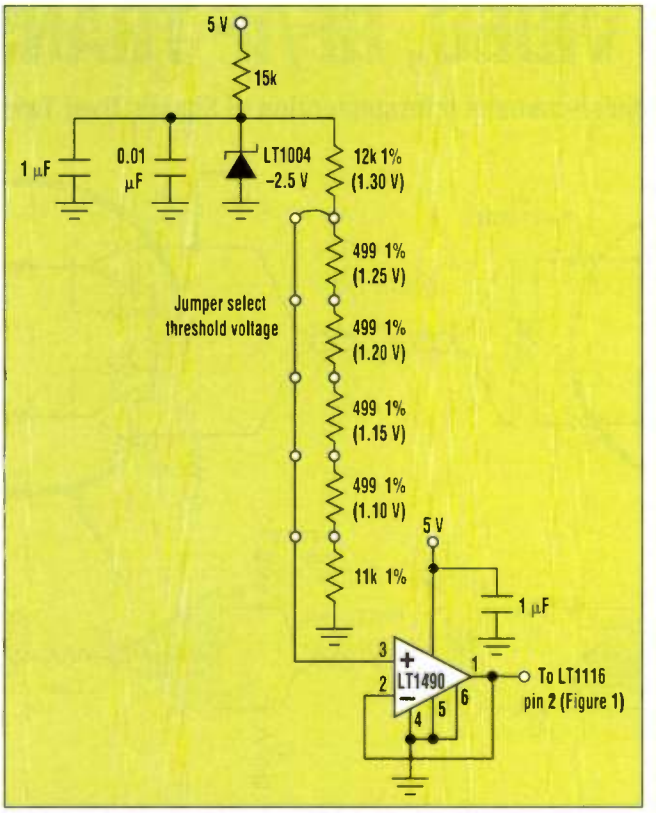
Circle No. 159 - For U.S. Response
Circle No. 160 - For International

There's also a way to adjust threshold without manual knobs or potentiometers. In this case, the microprocessor counts the number of ones and zeros over a given time period and adjusts the threshold (perhaps via a digital pot) to produce the required density of ones.

A more "analog" method of adjusting threshold might be to implement an integrator with reset. This circuit integrates the number of ones and zeros over time to produce a zero result for an adjustment that produces equal numbers of ones and zeros. Again, a digital pot could be used to adjust threshold, with the threshold being decreased for the case of "not enough ones" and increased for the case of "too many ones."

After many conversations with the "cyber illuminati," the circuit in Figure 2 was devised. This circuit can be used to replace the pot shown in the dashed box in Figure 1. In operation, an LT1004-2.5 is used as a reference at the front end of a precision voltage-divider string. A series of voltages is generated along the divider string and a jumper is used to connect this voltage to a buffer and then to the negative input of the LT1116 comparator. As was the case with the 2k pot, the voltage at pin 2 (the negative input of the comparator) sets the threshold for the comparator.

The selection of voltage taps on the resistor string is arbitrary. They were selected to allow a good adjustment range (defined as allowing jumper adjustment to 50% ones and 50% zeros) for a sample of ten 1N753A Zener diodes used to produce noise. The jumper could (and probably should) be replaced with analog switches controlled by a microprocessor in medium- to high-volume applications.



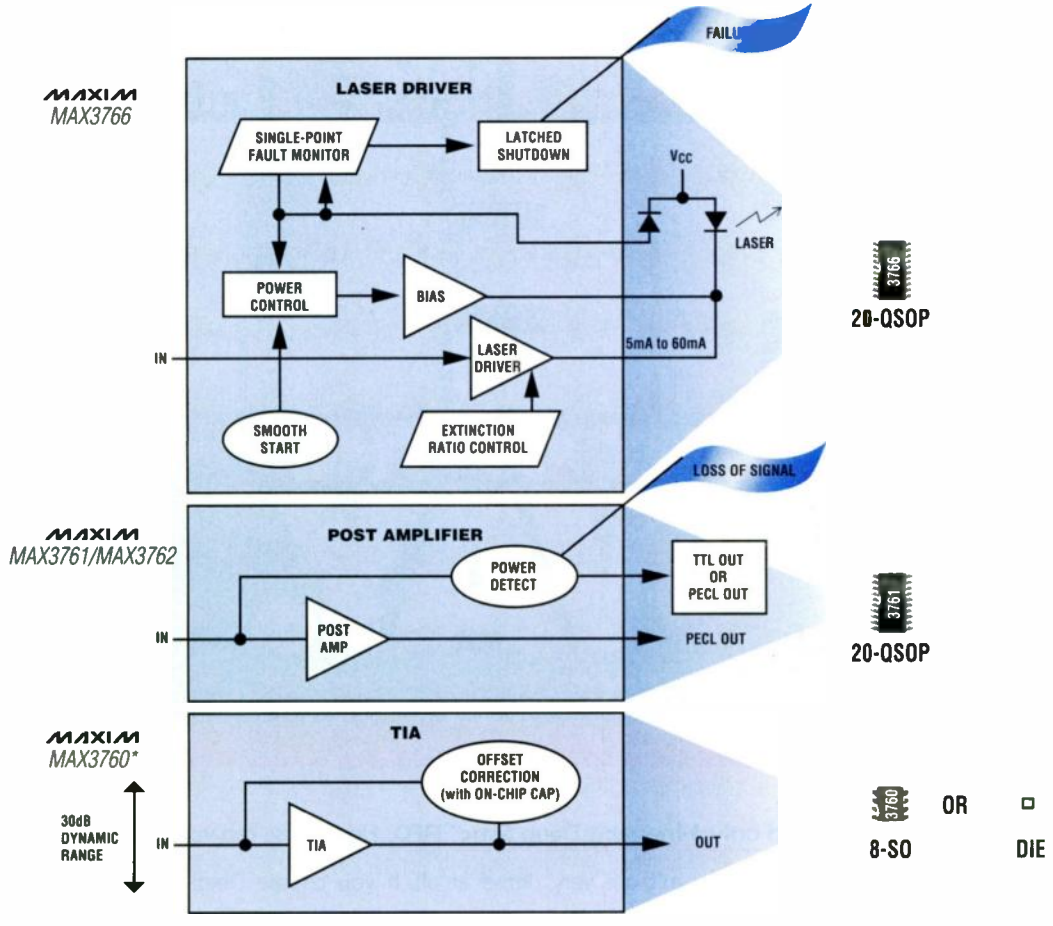
2. Adding this circuit offers a more "digital" method of adjusting the threshold. It replaces the potentiometer in the dashed box in Figure 1.

THE ONLY COMPLETE 622Mbps LAN FIBER OPTIC CHIPSET

YOU GET:

- **10 Functions Needed for 622Mbps LANs!**
- **60mA Laser Driver with LASER SAFETY Circuits!**
- **4mV Sensitivity Limiting Amp!**
- **30dB Dynamic Range TIA with -3dB Overload!**

No Additional Design Necessary: We've Done It All For You!



*Future product—contact factory for availability.

CALL TOLL-FREE 1-800-998-8800 for a Design Guide or Free Sample
For Small-Quantity Orders Call (408) 737-7600 ext. 3468
6:00 a.m. – 6:00 p.m. Pacific Standard Time
http://www.maxim-ic.com

1998 EDITION!
FREE FULL LINE DATA CATALOG
ON CD-ROM

MAXIM

For Small-Quantity Orders Call (408) 737-7600 ext. 3468

MasterCard® and Visa® are accepted for evaluation kits and small-quantity orders.

Distributed by Allied, Arrow, Bell, CAM RPC, Digi-Key, Elmo, Hamilton Hallmark, Nu Horizons, and Zeus. Distributed in Canada by Arrow.

Austria, Max m GmbH (Deutschland); **Belgium**, Master Chips; **Czech Republic**, Spezial-Electronic KG; **Denmark**, Arrow-Exatec A/S, **Finland**, Berendsen Components Oy; **France**, Maxim France, *Distributors*: Maxim Distribution, ASAP; **Germany**, Maxim GmbH, *Distributors:* Maxim Distribution, Spezial Electronic GmbH; **Ireland**, FMG Electronics, **Italy**, Maxim Italy, *Distributor.* Esco Italiana Electronics Supply; **Netherlands**, Koning En Hartman; **Norway**, Berendsen Electronics; **Poland**, Uniprod, Ltd , **Portugal**, ADM Electronics, S A , **Russia**, Spezial-Electronic KG; **Spain**, Maxim Distribución, ADM Electronics S A.; **Sweden**, Egevo AB, **Switzerland**, Maxim Switzerland, Laser & Electronics AG, **Turkey**, Interex (U.S.A.); **U.K.**, Maxim Integrated Products (U.K.), Ltd., *Distributors:* Maxim Distribution (U.K.), Ltd., 2001 Electronic Components Eurodis HB Electronics; **Ukraine**, Spezial-Electronic KG.

Circle No. 161 - For U.S. Response
Circle No. 162 - For International

WE'D LIKE TO THANK OUR COMPETITORS FOR GETTING THE HELL OUT OF THE WAY.

Introducing the world's one and only 1-megabit Deep Sync™ FIFO. How dense can you get? Well, if you choose our competitors' synchronous FIFOs, you can't get very dense at all. If you choose Deep Sync FIFOs from Cypress, you get a full 1-Mbit density. You get 100-MHz speed with near-zero latency. You get a true dual-ported cell that allows asynchronous gating of the read and write clocks without requiring an FS pin. And you get industry standard architecture and pinouts–so our Deep Sync FIFOs drop right into your existing designs. Deep Sync FIFOs. Only from Cypress. When you're ready to get dense, don't bother talking to our competitors. Talk to Cypress.

Cypress (and only Cypress) Deep Sync FIFOs

Size	Part No.	Speed	I_{CC}(max.)	Leads/Package	Availability
128K x 9	CY7C4291	10ns	40mA	32/PLCC	Now
128K x 9	CY7C4292	10ns	40mA	64/TQFP	Now
64K x 18	CY7C4285	10ns	50mA	64/TQFP	Now
64K x 9	CY7C4281	10ns	40mA	32/PLCC	Now
64K x 9	CY7C4282	10ns	40mA	64/TQFP	Now
32K x 18	CY7C4275	10ns	50mA	64/TQFP	Now

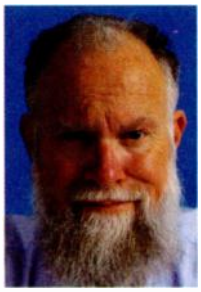
For a free literature pack call 800 858 1810 or fax 408 943 6848 and ask for Kit #D032 or see us at www.cypress.com/fifo.

CYPRESS

BY ENGINEERS. FOR ENGINEERS.

BOB PEASE

Bob's Mailbox



Readers of this column may remember the letter from Mike McGinn that appeared in the Sept. 15, 1997 Mailbox. Mike had everything he needed to go trekking with Bob—except a working kidney. So, it is with a great deal of pleasure that we present his most-recent communication.—ED

Hi Bob:

Thanks for the inspiration. On October 20, while recovering from hernia surgery, I got the call I was waiting for. The installation took six hours (which, I understand, is better than NT) and the kidney worked as soon as it was hooked up. I was out of the hospital in 10 days.

I don't know if someone who has not gone through this can appreciate how much it changes your life. Little did I realize how depressed I had become on dialysis, but the fact that I used to go around thinking, "This is my life in hell," should have been a clue. Now my marriage is better, my life is better, and I can do more with my six year old son. It's a whole new life. I can probably even go hiking now, but my strength is not all back yet. It was truly a happy holiday season in my house. We have much to be grateful for.

MIKE McGINN
via e-mail

Mike, we sure hope you can resume vigorous hiking soon. If you're permitted to do it, it's really good for your legs—and your head. Best wishes —RAP.

Dear Bob:

If one more note on prototyping won't kill you, read on...

1. Amusement: Jameco Electronics sells the "Wideband 100-MHz Prototype Board" *(catalog 974, p. 84)*. It consists of the white plug-in-the-leads breadboard inside an aluminum box (7.4 by 5.1 by 1.5 in.) with four BNC connections on two of the ends. I bought one for $59.95 (don't worry—I don't actually use it!) and have it hanging in my office. I show it to the students who come through here and discuss under which conditions you can actually get away with using it. It is amazing how many do not realize how much stray capacitance is built into those white boards. And, I cannot count the number of times I have been told "No, that is a resistor, *not* an inductor," when the resistor is sticking up 1 in. off the board. (Actually, the quality of the proto-board in the Jameco box is pretty good when compared to the Radio Shack version, but 100 MHz??? I'll try to remember to send you the test results next month.)

2. Strange-behavior department: I spent nearly 13 years at Sandia National Laboratories before coming to Kansas State University. I run a department (chief engineer and "pointy-haired boss" rolled into one!) here that supports all of the research groups on campus with custom electronics, sensors, and data acquisition systems. I employ a small full-time staff and about eight EE students part-time. It is nearly the only exposure the students get to "practical" engineering issues.

To their credit, most of them eat it up and recognize the value in and need for this experience. However, I have observed an interesting phenomena here (and at Sandia). The first time a new hardware engineer has to actually build what they design, they go into overload, sometimes for as long as four weeks! Having to specify resistor type, tolerance, wattage, capacitor dielectric, cap. tolerance, cap. package, IC package, heat sink style, connector type (and plug vs. socket), and so on, for a large design overwhelms them.

I even saw a very talented engineer give up hardware and shift to software (surely software has equivalent "loose ends"?) because he couldn't get over it. Then they figure out some ground rules, make some guesses, talk to some old guy and realize that many of the components in a large design just aren't that hard to spec and they move on. Have you observed such behavior?

3. Regarding practical training for engineering students, I don't have an answer, but I sympathize with the engineering schools. A good engineer needs to understand the theory so that they can extend their knowledge to "non-cookbook" situations, but at the same time, they *must* get their hands dirty to see where the theory can be applied. Do I want to spend my life laying out printed circuit boards? No! Did I need to do it a few times so that I really understand the compromises, problems, and gotcha's? Sure did, and because I have a good foundation in theory, I am a better engineer. But most companies are putting a lot of pressure on engineering schools to produce engineers specifically trained for their *current* employment needs. I argue that this is just as bad as producing a theoretician.

4. My favorite prototyping materials are Vector 8007 and 4112-4 boards. They are about 4.5 by 6.5 in., have a ground plane on the top, and various pad patterns on the bottom. I use very short pieces of 24 ga. wire where I cannot use the component leads to interconnect and keep the wire close to the surface of the board. Add standard copper clad to make shields, boxes, etc. The Vector boards work great for through-hole technology, and I have used them (with care) up to about 150 MHz. If memory serves, they are about $35 each, from Newark and others (not cheap, but very nice to work with).

TIM J. SOBERING
via e-mail

Surely there must be a good way to say "unless noted, all capacitors 0.01µF = ceramic disk type X5U; all resistors are 1% RN55D..." Keep it simple and standard. I have heard of cases where a white solderless board was used to make an experiment that ran up to 100 MHz. But it would be WRONG to count on it. There must be a better way, and you have defined one.—RAP

All for now. / Comments invited!
RAP / Robert A. Pease / Engineer
rap@web team.nsc.com—or:

Address:
Mail Stop D2597A
National Semiconductor
P.O. Box 58090
Santa Clara, CA 95052-8090

Preamble, the Performance Leader in Differential Measurement.

Microvolts to Kilovolts!

Model 1822
DC-10 MHz
X1000 Gain
16 upper & lower
BW limits

NEW

Model 1855
DC-100 MHz
X10 Gain
Very fast
recovery
from overdrive

Preamble 1800 Series stand-alone differential amplifiers are designed to function as signal conditioning pre-amplifiers for your oscilloscope, spectrum or network analyzers.

Model 1855 combines Gain, High CMRR, Very Fast Overdrive Recovery and Wide Common Mode Range to simplify direct measurement of such difficult signals as a switching supply upper gate drive.

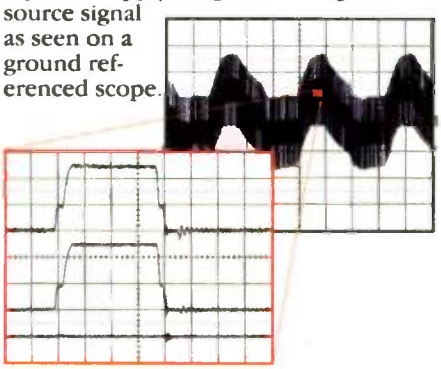
Model 1822's X1000 Gain can extend your scope's sensitivity to 1μV/div and includes a full complement of upper and lower bandwidth limits. Strain gauge, bio-medical and other physical parameters are well within the reach of the 1822.

Preamble XC Series Differential Probes give the user a choice of X1, X10, X100 and X1000 attenuation factors and circuit loading as low as 92 meg/4.5 pF. They facilitate differential measurements from microvolts to kilovolts

The **1800 Series** sport the industry's widest common mode range; limited only by the probe's voltage rating.

Measurements in off-line switching power supply primaries become safe, accurate and easy-to-make.

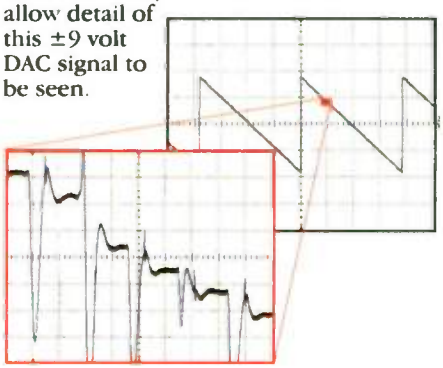
CONVENTIONAL
A power supply's highside FET gate to source signal as seen on a ground referenced scope.



DIFFERENTIAL
The 1855 rejects the line voltage and high dv/dt signal, cleanly displaying the upper and lower gate drive signals.

Preamble's 1800 Differential Amplifier Series low noise, wide common mode range and Precision Offset Generator allow minute portions of very large signals to be examined with 5½ digit resolution. The generator acts as a precision position control and extends your scope position range to over ±150,000 divisions; the industry's tallest display!

CONVENTIONAL
A scope lacks sufficient position range and lacks the ability to recover from overdrive to allow detail of this ±9 volt DAC signal to be seen.



DIFFERENTIAL
The 1800 Series allow the individual DAC steps to be examined at any point on the wave-form and measured to 5½ digit resolution.

PREAMBLE INSTRUMENTS

Preamble Instruments, Inc
P.O.Box 6118
Beaverton, OR 97007-0118
(503) 646-2410, 800-376-7007
FAX: (503) 646-1604

READER SERVICE 179

12-Bit ADC First To Feature A 55-MHz Sampling Rate

The TDA 8768 is a 12-bit analog-to-digital converter that's claimed to be the first 12-bit converter to offer a sampling rate of 55 MHz. It can be used in combination with the TDA 9901, a special amplifier working with weak or variable input signals to ensure reliable operation. Optimized for telecommunications applications such as base stations and professional imaging systems, or medical ultrasound scanners, the TDA is the first product in a new family of 55-MHz ADCs. A related product, the TDA 8767, is available in three versions with 10-, 20-, and 30-MHz sampling frequencies. Since it's an integrated bipolar IC, the chip offers differential or single analog inputs, and a differential nonlinearity of ±0.6 LSB without missing code. Its applications include video digitizing, HDTV, the PC market, imaging systems, telecommunications, and various industrial applications. AV

***Philips Semiconductors**, International Fulfillment and Sales Support Center for TDA 8768/8767/9901, P.O. Box 5006, 2900 EB Capelle a/d Ussel, The Netherlands.* **CIRCLE 503**

Intelligent Batteries Provide Current Condition Parameters

Due to their integrated intelligence and the provision for data exchange, smart batteries provide an up-to-date overview of their current condition, their remaining operation time, the remaining capacity, the charging/discharging cycles already used, and the remaining life. An integrated chip also controls and optimizes the power management of the batteries. Power consumption is permanently adjusted as a result of the continuous data flow between the battery and the device to be powered. Based on the status report provided by the battery to the power-consuming unit, certain functions may simply be switched off or turned down. As a result, the user automatically achieves longer operating times per battery charge.

Thanks to the versatile data exchange with the charger, different battery systems, such as NiMH (nickel metal hydride), NiCd (nickel cadmium), or Li-Ion (lithium ion), can be employed. The charger automatically recognizes which kind of battery system is present. It knows how much energy should be charged and how to charge. This, in turn, helps to maximize the life of the batteries while completing charging within the shortest time possible. In addition, different types of battery data, such as manufacturer, type, and chemical system, can be called up. Furthermore, significant events like extreme temperatures or very high currents can be stored. AV

***Varta AG**, Am Leineufer 51, 30419 Hannover, Germany; phone: +49-511/7903-0; fax: +49-511/7903-717.*

CIRCLE 504

TrenchFET Claims Lowest On-Resistance for Power MOSFETs

A new TrenchFET is claimed to offer the industry's lowest on-resistance for power MOSFETs. The devices, available in TO-220 or D^2PAK packages, feature a maximum on-resistance of 4 mΩ. They're able to work with maximum currents of 75 A. Dubbed SUP75N03-04 (TO-220) and SUB75N02-04 (D^2PAK), the devices are mainly intended for 30-V applications in the automotive industry (e.g., for power-train control or body control). Due to the fact that MOSFETs won't need to be connected in parallel when TrenchFETs are employed, system designers can save board space, decrease the number of connections, and increase the reliability of the system. The new technologies offer 32 million transistor cells on every square inch, which means almost tripling the former maximum cell density. AV

***Temic**, P.O. Box 35 35, 74025 Heilbronn, Germany; phone: +49-7131/67-28 31; fax: +49-7131/67-2423.* **CIRCLE 505**

0.25-μm CMOS Process Eligible For Prototyping To Schools, Labs

In cooperation with SGS-Thomson Microelectronics, Circuits Multi-Projets (CMP) has unveiled a high-performance deep submicron 0.25-μm CMOS process. The HCMOS7 process is available for prototyping to educational institutions and research laboratories, on a cooperation basis. No commercial designs are ready as of yet, but it's expected that commercial versions will become available on a commercial basis for small volume production in the near future.

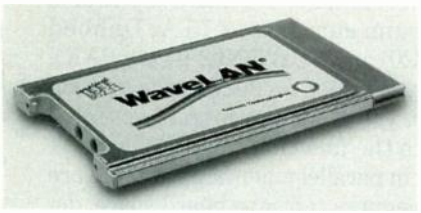
Gate length of the HCMOS7 shallow trench isolation process is 0.25 μm drawn, and 0.2 μm effective. It has up to six metal-layer levels with fully stackable contacts and vias. Power supply is 2.5 V, and threshold voltage is V_{TN} = 0.5 V, V_{TP} = −0.5 V. Full custom designs are supported using Virtuoso layout editor and LAS synthesizer. The layout verifications (DRC, ERC, extraction, LVS) are fully supported for Diva and Dracula. Transistor-level simulations are only supported under Eldo Level 59. Standard-cell designs are supported using Verilog/VHDL descriptions for synthesis and simulation. Synthesis is supported under Synergy or Synopsys, while simulation is supported under Verilog-XL, Leapfrog, and VSS. Among the various CAD software versions supported are: Cadence/OPUS version 4.3.4.50.106; Cadence/Dracula version 4.3.0996; and Eldo version 4.4.1. RE

***Circuits Multi-Projets**, 46 avenue Felix Viallet, 38031 Grenoble Cedex, France; phone: +33 4 76 57 45 00; fax: +33 4 76 47 38 14; e-mail: cmp@archi.imag.fr; Internet: tima-cmp.imag.fr.* **CIRCLE 506**

Edited by Roger Engelke

First 802.11-Compliant Wireless LAN PC Card

The WaveLAN OEM PC Card is a fully integrated wireless LAN transceiver. Intended for commercial, industrial, and medical applications, it's the first device of its kind to be fully compliant with the IEEE's 802.11



wireless LAN standard. Designed for easy integration by system designers and developers, it can be used to quickly implement point-of-sale, data collection, wireless server, and messaging systems. It also can be easily integrated into notebook computers.

With a maximum data rate of 2 Mbits/s, the OEM PC Card incorporates a 2.4-GHz direct sequence spread spectrum (DSSS) radio, an IEEE 802.11 MAC controller, and a standard type-2 interface within its PC Card form factor. Two antenna connections are provided to enable antenna selection and spatial diversity options. Important features built into the card include multichannel roaming to permit multi-cell connections, use of the 802.11 protocol's RTS/CTS signaling to increase range, and automatic rate selection to ensure reliable connections.

The card uses advanced digital-signal-processing techniques to provide greater resistance to interference and a wider range of coverage than the basic requirements of the 802.11 standard. Thanks to its software-based architecture, it can easily be upgraded with new features or updates to the standard. In addition, it draws only 300 mA during transmit, greatly extending battery life over many other solutions.

Available during the first quarter of 1998, the WaveLAN OEM PC Card will be priced at $330 each in OEM quantities. LG

Lucent Technologies WaveLAN Div., *Zadelstede 1-10 Nieuwegein, Netherlands, 343-1JZ; (800) WAVELAN; www.wavelan.com.* **CIRCLE 560**

Family of 10/100-Tx PHY ICs Offers Unique Features

The 80220 and 80221 are fully integrated, single-chip CMOS solutions for both 100Base-TX and 10Base-T networking environments. They offer network switch, hub, and adapter card designers significantly higher performance with additional unique features not available in other PHY solutions.

Key performance features of the new PHYs include typical bit-error rates (BERs) of less than 10-12 across 140 meters of CAT 5 cable, and extremely low transmit jitter of ±0.35 nS. This gives designers much improved interoperability at longer cable lengths. The products are fully characterized for incremental cable length performance to guard against short or random cable length interoperability problems.

Both the 80220 and 80221 incorporate a Flow Control feature. It eases the common congestion problems by automatically transmitting a JAM packet that causes the remote unit to back off and allow the receive end to clear its buffers. Both devices have drivers for up to four LEDs, which can be programmed from five different event options. The 80221 includes an additional two LED drivers to indicate transmit and receive activity. Both chips boast a low, 0.75-W typical power consumption. Also available is the Performance Package and Design Kit, which contains data report summaries and other useful design information.

Package options include a 44-lead PLCC, and a 64-lead 1.4-by-10-by-10-mm LQFP. The 80220 and 80221 Physical Layer ICs are currently shipping in volume production with pricing of $9.00 each in 25K unit OEM quantities. LG

Seeq Technologies Inc., *47200 Bayside Pkwy., Fremont, CA 94538; (510) 226-7400; fax (510) 657-2837; www.seeq.com.* **CIRCLE 561**

ATM Chip Enables Low-Cost, Multiuser Broadband Services

The Helium ATM processor chip and its companion software packages form a powerful set of building blocks that can be used to construct multiple-user endpoint devices, such as Ethernet, ATM, or USB gateways; xDSL; fiber to the curb (FTTC); fiber to the home (FTTH); and electric subscriber line data networking equipment. The Helium chip, coupled with its software modules, greatly simplifies the construction of a gateway between the xDSL line and up to six ATM, USB, or Ethernet ports (in any combination). In conjunction with a PPP driver module, the Helium chip provides native bridging, (remote access) routing, and switching functionality.

The Helium ASIC owes its versatility to a combination of three functions usually found on separate devices: an Ethernet controller, a standard USB (universal serial bus) interface, and a 48MHz ARM 710 processor. In addition, the Helium has several advanced I/O features, such as an HDLC block for packet mode applications and a Utopia 2 interface. This allows Helium to connect to multi-physical interface chips, giving it a wide range of applications and connectivity options to Ethernet and ATM hub and switch chips.

To speed development, there's a wide range of "integrated software on silicon" modules bundled with the Helium chip. One module includes a full complement of ATM Forum standards-based software, including UNI signaling, protocol stacks, host drivers for PC, and several OSI layer-3 functions. Other modules enable the communication processor to implement the point-to-point protocol (PPP) over ATM in client, server, and other environments.

The Helium chip will be available in the first quarter of this year, with production quantities coming in the second quarter It costs less than $50 in bulk quantities. LG

ATM Ltd., *2933 Bunker Hill La., Santa Clara, CA 95054; (408) 566-1000; fax (408) 980-8250; e-mail: info@atminc.com; www.atml.com.*

CIRCLE 562

802.11-Compliant MAC Chip Enables Wireless Data Apps

The Am79C930 PCnet Mobile is a single-chip, programmable wireless LAN media access controller (MAC) that's designed to support fixed and mobile wireless data applications. Its integrated flash-memory interface allows it to support the IEEE 802.11 wireless data protocol. The chip is designed to support both direct-se-

(continued on page 144)

Rome wasn't built in a day. Your ASIC can be.

The industry's first and only true ASIC alternative.

Fully programmable, 40,000 system gates, 80 MHz performance, on-chip RAM, and complete software and core support starting at under $3.00. Fully PCI compliant in both 5 and 3.3 volt versions.

Bottom line? The ASIC of tomorrow is available today, and your local distributor is the perfect forum to learn more about it.

www.xilinx.com

XILINX®

The Programmable Logic Company℠

READER SERVICE 208

(continued from page 142)
quence (DS) and frequency-hopping spread-spectrum RF, as well as infrared physical layers. An integrated host interface circuit supports both PCMCIA and ISA plug-and-play configuration parameters.

The device can operate on both 3.3- and 5-V power supplies, and has a low-power mode to conserve battery life in portable equipment. Using the PCnet Mobile, designers will be able to deliver fully functional, 802.11-compliant, PCMCIA-based wireless data products for a total parts and labor cost of $90 to $100.

Recent improvements to the design have added 802.11 standard compatibility as well as support for access points that allow mobile users to seamlessly access wired data networks. A full spectrum of licensable device driver software is available, enabling designers to easily communicate with most Windows operating systems (NT 4.0,'95 OSR2, and NDIS 2/3 for workgroups), as well as Novell networking software. NDIS 4 and NT 5.0 support should be available in early 1998, as well as advanced power management and enhanced RSA-based security features.

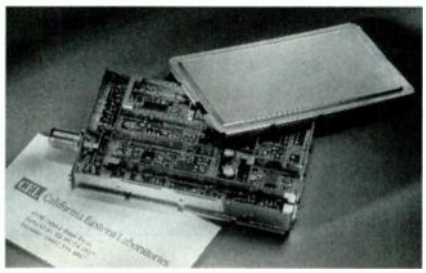
Available now, the Am79C930 PCnet Mobile costs $21 each in quantities of 10,000. The 802.11 protocol firmware binary files are provided free of charge with the purchase of the chips. Additional software drivers for the various operating systems carry a one-time licensing fee of $9000. LG

***AMD Inc.**, P.O. Box 3453, Sunnyvale, CA 94088-3453; (800) 222-9323, (408) 749-5703; www.amd.com.*
CIRCLE 563

Two-Way RF Transceiver For MCNS Cable Modems

The ISG2000 is a complete two-way, MCNS-compliant RF transceiver module intended for cable modem products. No bigger than a business card, it's designed to interface directly with a standard modem's QAM mod/demod ICs to provide a complete drop-in RF solution that saves space, cuts development and manufacturing costs, and shortens time to market.

The sealed module's 100% solid-state design eliminates coils and the hand-tuning they typically require. With an upstream frequency range of 5 to 42 MHz, and a downstream range of 91 to 860 MHz, the ISG2000 covers the entire standard cable band. RF input level range is –15 to 15 dBm, and RF gain can range from 25 to 75 dB. Available now, the ISG2000 is priced at less than $30 each in volume quantities. LG



***California Eastern Labs**, 4590 Patrick Henry Dr., P.O. Box 54964, Santa Clara, CA 95054-1817; attn: Richard Bay-Raymond (408) 988-3500; fax (408) 988-0279;' www.cel.com.* **CIRCLE 564**

Evaluation Kit For 155-Mbit/s ATM SAR Is Now Available

Two evaluation kits have been made available to assist in the development of products based on the TC3585AF 155-Mbit/s ATM SAR and the TC35821F SONET/SDH framer ICs. These complete solutions are based on producible reference designs and include an evaluation card, reference schematics, and pc-board art for both fiber and copper UTP applications. Software provided with the kit has drivers for Windows '95 and NT operating systems and a benchmark utility.

The TC3585AF 155-Mbit/s ATM SAR performs all functions necessary for the SAR function. It features hardware-implemented available bit rate (ABR) control logic and support for a PCI bus interface. The chip's unique DMA regime performs the actual SAR in host system memory, reducing the amount of RAM required for a complete solution.

Available as the TCREF101 with a UTP copper interface, and the TCREF102 with a fiber interface, both boards are available now. In single units, the TCREF101 costs $99 each, while the TCREF102 costs $139. LG

***Toshiba Electronic Components Inc.**, 1060 Rincon Circle, San Jose, CA 95131; (800) 879-4963; Internet: www.toshiba.com.taec.* **CIRCLE 565**

Sub-$5 DSP Packs 100 MIPS In Cordless Phones, TADs

Specifically designed to cut the cost of consumer electronics, the DSP1609 digital signal processor brings 100 MIPS of signal-processing power to communication applications, such as telephone-answering devices (TADs), cordless phones, and modems. Fabricated in 0.3-µm technology, the parallel pipeline processor's architecture is optimized for communication applications. Included is an on-chip instruction cache, two 36-bit accumulators, and the ability to perform a 16-by-16 bit multiply with a 36-bit accumulation in a single clock cycle.

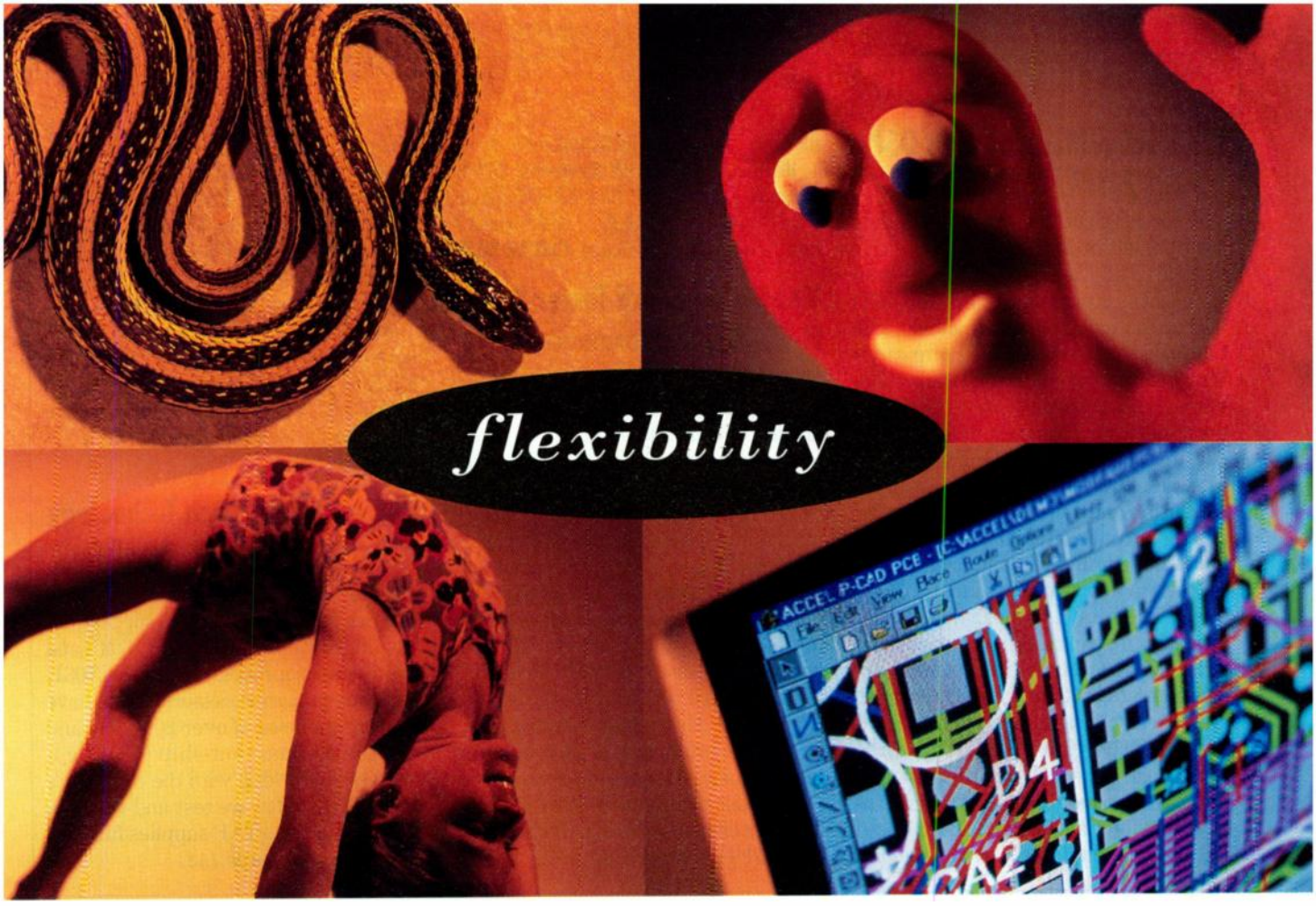
Its on-chip bit manipulation unit (BMU) can save precious instruction cycles by independently performing multibit shifts, XOR comparisons, and block transfers. A programmable phase-locked loop, a watchdog timer, and two interrupt timers also are incorporated.

Developed as a modular core, the DSP can be modified or inserted into a larger ASIC for high-volume custom applications. It can support code-intensive tasks, thanks to its large 24-kword internal program ROM, and 2 kwords of on-chip static RAM. On-board flash memory also is available. An on-chip DRAM control interface and two 64-kword address spaces enable it to interface to a wide mix of external memory and peripheral devices. The DSP 1609's dual-channel serial I/O (SIO) port allow it to easily communicate with host systems and execute boot ROM transfers.

Capable of running on either 3.3 or 5 V, the digital signal processor consumes only 3.3 mW/MIPS and 9.5 mW/MIPS, respectively. Using the low-power "stopclk" function, standby power can be as low as 66 µW. The device is a code-compatible extension of the Lucent DSP 16xx family and can make use of an extensive line of development tools. Both a complete reference design and development kit are available.

Housed in either a 28-pin SOJ or a 44-pin PLCC, the DSP 1609 costs $4.95 each, in quantities of 10,000 pieces. LG

***Lucent Technologies Microelectronics**, Dept. AL500404200, 555 Union Blvd., Allentown, PA 18103; (800) 372-2447, fax (215) 778-4106; Internet: www.lucent.com.micro.* **CIRCLE 566**



It moves with you. Presenting ACCEL EDA™ - the PCB design software for Windows® designed with flexibility in mind. Powerful tools to build today's toughest designs yet configurable to your own exacting standards. Critical design rules flow smoothly throughout the entire design — you set the rules, ACCEL EDA responds. That's Correct By Design confidence. Plus the flexibility to tailor a "best of breed" EDA system with seamless interfaces to Viewdraw,® Specctra® and CAM350.™

Call for your free eval software with multimedia tour, or to arrange an on-site demo.

Turn us inside out. Installation, training, support — the service provided by ACCEL and its worldwide value-added partners is personalized for you.

Call Us Today. See how the flexibility in ACCEL EDA helps you run circles around your competition.

ACCEL Technologies, Inc.
800 488-0680 Sales
619 554-1000 Service
619 554-1019 Fax
sales@acceltech.com
www.acceltech.com

READER SERVICE 108

Mezzanine Module Gives DSP Boards Fast I/O Capability

The bitsi DAQ I/O mezzanine module supplies eight independent 500-kHz analog-to-digital channels with simultaneous sampling and four 100-kHz digital-to-analog output channels. The module, for use with the company's DSP boards based on the Analog Devices SHARC processor, is designed for applications that require intensive I/O functions as well as DSP capability. The bitsi DAQ samples inputs at 12-bit resolution and converts 14-bit data for analog output. Differential inputs enhance noise immunity, and overvoltage protection allows use in industrial systems. The bitsi I/O mezzanine standard is optimized to match the SHARC's I/O capabilities. The interface consists of 32 data bits, 20 address bits, 10 control signals, two DMA channels, six SHARC link ports, and three serial ports. The DSP boards come is a number of standard bus platforms, including CompactPCI, ISA, PCI, and PC/104. The bitsi DAQ is available immediately starting at $1495. JN

Bittware Research Systems, *33 N. Main St., Concord, NH 03301; (603) 226-0404; (603) 226-6667; http://www.bittware.com.* **CIRCLE 567**

VXI-Based Board Tester Packs Flexibility, Performance

The Endeavor functional board-test systems are VXI-based for flexibility and are designed to eliminate the problems associated with in-house development and fabrication of single-purpose testers. Modules include a 5.5-digit multimeter, 250-MHz counter, 250-MHz oscilloscope, 2.5-MHz arbitrary waveform generator, and three relay multiplex/switch modules. Digital testing is performed by the IO50, a 64-channel intelligent digital I/O module with on-board processor and memory-backed pins for timing and handshake. It can be configured for any standard logic family. Also included are a receiver base that houses all of the electrical interconnections, a modularized and GPIB-programmable power source for the unit under test, an integrated vacuum delivery system, and a 20-column printer. The system fits in a 19-in. rack measuring 5 ft. high and 3 ft. deep, and including a Pentium-based controller and VGA monitor. Endeavor system prices start at $100,000. JN

Interface Technology Inc., *300 South Lemon Creek Drive, Suite A, Walnut, CA 91789; (909) 595-6030; fax (909) 595-7177; e-mail: info@InterfaceTech.com; http://www.InterfaceTech.com.*

CIRCLE 568

PowerPC Emulation Technology Includes Network Accessibility

The PowerTAP emulation technology was designed specifically to support debugging of Motorola PowerPC 603E and 750/740 microprocessors and EC603E embedded microprocessors, which have core frequencies of over 200 MHz and use the common-on-chip (COP) coprocessor. Working with the company's CodeTEST software test and verification tools, PowerTAP supplies full con-

(continued on page 148)

System Two

A New Standard For Audio Testing

Leading edge performance has been a defining feature of Audio Precision products since the inception of our company in 1984. Thousands of our System One audio analyzers are in use worldwide, selected by design engineers for high performance and by test engineers for our comprehensive programmable analog and digital audio measurement capabilities.

Now our System Two true Dual Domain audio analyzer joins the System One, setting a new standard for performance and flexibility in audio frequency test & measurement.

System Two is a true Dual Domain analyzer. Other test instruments may have both analog and digital inputs and outputs ... but they're not true Dual Domain! They rely on performance-limiting converters to pass analog signals back and forth to a DSP core of digital-only hardware. Passing signals through a/d or d/a converters for every measurement robs the test instrument of performance. System Two includes separate, independent hardware for direct audio measurements in both domains, plus additional and extensive interface measurement capability including jitter measurements, eye patterns and all other parameters described in AES3, the serial audio interface standard.

The new standard of System Two is represented by performance specifications such as guaranteed analog generator and analyzer residual THD+N of -108 dB, guaranteed analog signal flatness of ±0.01 dB for the generator and analyzer; and 24 bit digital signal generation with 48 bit FFT dynamic range.

From aircraft to automobiles, satellites to cell phones, headsets to hearing aids, System Two represents a new standard for audio frequency test & measurement applications. Compare for yourself - our worldwide force of representatives will be pleased to provide comprehensive specifications and a true Dual Domain on-site demonstration.

Audio precision

Audio Precision
PO Box 2209
Beaverton, Oregon 97075-3070
Tel: (503) 627-0832 FAX: (503) 641-8906
US Toll Free: 1-800-231-7350

INTERNATIONAL DISTRIBUTORS: ***Australia:*** IRT Electronics Pty Ltd., Tel: 2 439 3744; ***Austria:*** ELSINCO GmbH, Tel: (1) 815 04 00 ***Belgium:*** Trans European Music NV, Tel: 2 466 5010 ***Brazil:*** INTERWAVE LTDA., Tel: (21) 325-5351; ***Bulgaria:*** ELSINCO Rep. Office Sofia, Tel: (2) 958 12 45; ***Canada:*** GERRAUDIO Distribution, Tel: (416) 696-2779; ***China, Hong Kong:*** A C E (Int'l) Co. Ltd., Tel: 2424-0387, ***Croatia:*** ELSINCO Rep. Office Zagreb Tel: 1 68 09 14; ***Czech Republic:*** ELSINCO Praha spol. s r.o., Tel: (2) 49 66 89, ***Denmark:*** npn Elektronik aps, Tel: 86 57 15 11; ***Finland:*** Genelec OY, Tel: 77 813 311; ***France:*** ETS Mesureur, Tel: (1) 45 83 66 41; ***Germany:*** RTW GmbH & Co. KG., Tel:221 70913-0, ***Greece:*** KEM Electronics Ltd., Tel. 1 67 48514/5 ***Hungary:*** ELSINCO Budapest KFT, Tel: (1) 269 18 50 ***India:*** Electro Dynamics, Tel: 512 364713; ***Israel:*** Dan-El Technologies, Ltd., Tel: 3-647 8770; ***Italy:*** Audio Link s.n.c., Tel: 521 648723; ***Japan:*** TOYO Corporation, Tel: 3 [5688] 6800, ***Korea:*** B&P International Co., Ltd., Tel: 2 546-1457; B&P (Kumi Office), Tel: 546 53-7347/8. ***Malaysia:*** Test Measurement & Engineering Sdn.(Selangor), Tel: 3 734 1017; Test Measurement & Engineering Sdn. (Penang), Tel: 4 6422088; ***Netherlands:*** Heynen B.V., Tel: 485 496 111; ***New Zealand:*** Audio & Video Wholesalers, Tel: 7 847-3414; ***Norway:*** Lydconsult, Tel: 47-69-178050; ***Poland:*** ELSINCO Polska sp. z o.o., Tel: (22) 39 69 79, ***Portugal:*** Acutron Electroacustica LDA, Tel: 1 9414087 / 9420862; ***Singapore:*** TME Systems Pte Ltd., Tel: 747-7234; ***Slovakia:*** ELSINCO Slovensko, s.r.o., Tel: (7) 784 165; ***South Africa:*** SOUNDFUSION MFG., Tel: 11 477-1315, ***Spain:*** Telco Electronics, S. A., Tel: 1 531-7101 ***Sweden:*** TTS Tal & Ton Studioteknik AB, Tel: 31 52 51 50; ***Switzerland:*** Dr. W.A. Gunther AG, Tel: 1 910 41 41; ***Taiwan R.O.C.:*** Double Advance Tech., Tel: 2-596 0696, ***Thailand:*** Massworld Company Ltd., Tel: 2-294-4930; ***United Kingdom:*** Thurlby Thandar Instruments, Ltd., Tel: (1480) 412451

(continued from page 146)
trol of the processor, source-level trace, performance analysis, and code coverage. A network-accessible interface allows designers to monitor and reset the target system remotely. PowerTAP's "crash-proof" control of the processor permits up to 1024 software breakpoints per session and supports both examination and modification of target memory and processor registers. The emulator can debug code in cache, ROM, RAM, or flash memory. PowerTAP is initially available for HP, Windows/NT, and HP hosts. A typical system price for a PowerTAP on a PC host is $7995 for single units. Delivery is in six weeks. JN

***Applied Microsystems Corp.**, P.O. Box 97002, Redmond, WA 98073-9702; (425) 882-2000; e-mail: info@amc.com; Internet: http://www.amc.com.*
CIRCLE 569

VXI Matrix Card Switches 0.5 A, 125 V At 400 MHz

The VXI-based 1260-51 RF matrix switch card can switch up to 0.5 A and 125 V, and features a 400-MHz bandwidth. Users can configure the card as six 2 ↔ 6 matrices, three 2 ↔ 12 matrices, or one 2 ↔ 36 matrix. The card's advanced path switching feature simplifies programming. The user specifies only the two ports to be connected and the 1260-51 automatically selects the optimum path. VXIplus&play drivers also simplify system integration. Like all models in the 1260 series, the 1260-51 is messaged-based and can be configured as a complete system with control accomplished by a daughterboard mounted on one of the cards in the system. The VXI local bus transmits the control signals from the daughterboard to all other cards in the system. This allows access to features like nonvolatile memory for storing relay configurations, relay monitoring for confidence checking of all relays, and scan mode for synchronous scanning of multiple test points. Delivery is in eight to 12 weeks. Call for pricing. JN

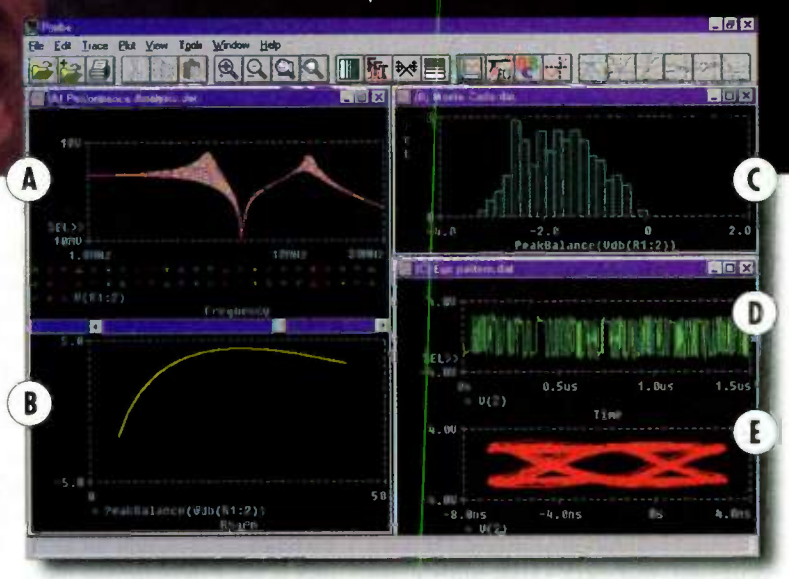
***Racal Instruments Inc.**, 4 Goodyear St., Irvine, CA 92618; (800) 722-2528; fax (714) 859-7139; http://www.racalinst.com.* **CIRCLE 570**

Personality Module Supplies Z382 Emulation Support

A Personality Pak and Pod for the Model 8800 emulator/analyzer allows the instrument to provide emulation for the Zilog Z382 communications processor. Four versions accommodate different connection options. Solder-down assemblies are available for both PQFP and TQFP packages. A unique precision test connector allows proprietary Clip-On Emulation for a soldered-in processor. Customized cables also are available for connection to the Zilog evaluation board. The instrument supports zero-wait-state emulation of the Z382 to 20 MHz, with up to 256 software breakpoints and 65,535 hardware breakpoints. Trace memory is 64k and up to 2 Mbytes of flexible overlay memory is available. Complete Model 8800 systems with Z382 support start at $12,840. Delivery is in two weeks. JN

***Orion Instruments Inc.**, 1376 Borregas Ave., Sunnyvale, CA 94089; (800) 729-7700; (408) 747-0440; fax (408) 747-0688.* **CIRCLE 571**

Why Just Simulate Your Design...



Understand It!

All simulators produce reams of data. But only one presents the data in a format that enables you to quickly and easily understand it—**MicroSim PSpice.**® It's used by more engineers than all other analog simulators combined. Here is one reason why.

With a click of the mouse, MicroSim PSpice extracts data from a whole set of analog waveforms and displays the data on a single screen. MicroSim PSpice A/D even displays mixed analog/digital simulation results together. You can immediately see the effects of changing several different variables all at one time. You can explore the relationship between changes in your circuit and changes in its behavior in order to determine performance trade offs. With MicroSim PSpice, you can spend your time creating better designs.

MicroSim PSpice

Extract performance from many simulations (A) to see how complex circuit behavior varies with component value changes (B)

Histograms (C) show production yields with component tolerances

Macros and functions allow you to measure performance (E) from complex waveforms (D)

MicroSim®

Setting the standard for Desktop EDA™

Contact MicroSim at 1.800.245.3022 *or* 714.770.3022

You can visit our Web site: http://www.microsim.com *E-mail:* sales@microsim.com

READER SERVICE 300

Synchronous, 4-Mbit Flash Memory Offers Burst I/O

Available with either a 16- or 32-bit interface, a 4-Mbit flash memory provides synchronous operation with a burst operating mode to provide high-speed data transfers. The industry's first x16/x32 configurable flash-memory chip, the TMS28F033 operates at bus speeds of up to 40 MHz and can burst data at rates approaching 100 Mbytes/s. Part of the memory—24 kbytes—can be protected and used to hold secure code (write-protected). The chip thus offers designers both synchronous and asynchronous protocol, a burst data read capability, hardware-selectable data-bus width, 3- or 5-V user-selectable input-output interface, linear or interleaved burst access, and software configurable latency for data-burst accesses. The TMS28F033 comes housed in an 80-lead PQFP, is available in sample quantities, and sells for $14.40 apiece in 100-unit lots. DB

***Texas Instruments Inc.**, Semiconductor Group, SC-97084, Literature Response Center, P.O. Box 172228, Denver, CO 80217; (800) 477-8924, ext. 4500, or on the web at http://www.ti.com/sc/docs/news/1997/97084.htm.* **CIRCLE 572**

Set-Top-Box Reference Platform Speeds Designs

The Horizon development board provides designers with a full-featured evaluation platform for its second-generation Vista chip set for set-top boxes. The board includes a fully-programmable software API that allows designers to build in features and services to meet various market demands.

The second-generation chip set reduces the chip count by 50% versus the first-generation chip set. It consists of the VES1893 analog-ready satellite receiver chip, the VES2700 integrated set-top controller (the chip is based on an ARM CPU core and includes MPEG 2 transport, DRAM control, a telephone modem, an IEEE 1394 interface, DVB decryption, and peripheral I/O support), and the VES6100 MPEG2 audio/video decoder with video encoder and on-screen display output. The features allow designers to create rich on-screen displays that combine overlay text, graphics, hyperlinks, drop-down, and pop-up menus. Additionally, the embedded ARM processor on the VES2700 reduces the command lag to near zero.

The Horizon board includes the chip set along with DRAM, SRAM, Flash memory, video memory, an infrared remote-control interface, plus connections for smart cards, serial and parallel communications, and other features . In OEM quantities, the second-generation Vista chip set sells for less than $39. To obtain the reference platform, contact the company. DB

***VLSI Technology Inc.**, 1109 McKay Dr., San Jose, CA 95131; David Tahmassebi, (408) 474-5506; Web: www.vlsi.com.* **CIRCLE 573**

Synchronous DRAMs Pack 64 Mbits, Run At 125 MHz

Available in standard 54-lead thin, small-outline packages, 125-MHz versions of a 64-Mbit synchronous DRAM are now available from Micron Technology. The memories operate from a 3.3-V supply and are offered in three configuration options: 16 Mwords by 4 bits (MT48LC16M4A2TG), 8 Mwords by 8 bits (MT48LC8M8A2TG), and 4 Mwords by 16 bits (MT48LC4M16A2TG). The memories are manufactured with the company's 0.25-µm DRAM process and will offer designers one of the fastest options for high-performance systems. In addition to individual chips, the company also offers 64-and 128-Mbyte DIMMs that are designed for operation at 100-MHz bus speeds. The DIMMs are available in organizations of 8 Mwords by 64 or 72 bits, and 16 Mwords by 64 or 72 bits. Prices for the memory chips are similar to prices for 64-Mbit EDO-style DRAMs. Module prices are slightly higher than equivalent-capacity EDO modules. DB

***Micron Technology Inc.**, 2805 East Columbia Rd., Boise, ID 83706-9608; Kit Fawcett, (208) 368-4000; www.micron.com.* **CIRCLE 574**

Surface-Mount SRAM/Clock Modules Ease Manufacturing

The PowerCap family of nonvolatile SRAM and timekeeping modules provides package options for surface-mount assembly and even permits battery replacement. The modules are designed for direct reflow soldering and offer memory capacities from 8 kwords by 8 bits up to 512 kwords by 8 bits. A two-piece design in the PowerCap modules allows the units to be reflow soldered at temperatures exceeding 220°C without damage to the batteries, which are typically rated for temperatures of only up to 85°C.

To deal with the high temperatures, the two-part module has a base that only contains the integrated circuitry, and an upper assembly, which contains the battery, that is snapped onto the base after

the reflow soldering. By separating the two, not only can the batteries be added at the last minute to minimize any current drain until the product is shipped, but the approach also allows the battery to be removed and replaced if something should go wrong with the battery.

PowerCap assemblies are available for the DS12xx, DS13xx, and DS164x families of nonvolatile SRAMs, nonvolatile SRAMs with built-in battery monitor and system power monitor logic, and nonvolatile SRAMs with timing functions, respectively. The internal SRAMs are available in access-time options of 70 and 100 ns for all but the timekeeping modules, which have access times of 120 or 150 ns. All modules are 34-lead devices and act as drop-in replacements for the company's previous-generation low-profile module package.

When assembled, the entire PowerCap unit is just 0.25-in. tall and has a footprint of less than 1-in.^{2}. In lots of 10,000 units, the battery portion sells for $3.00 or $4.38 (memory-only and memory+timekeeping, respectively), while the base unit starts at $6.62 to $13.18 for the lowest-capacity memory options. DB

***Dallas Semiconductor**, 4401 S. Beltwood Pkwy., Dallas, TX 75244-3292; Drew Jenkins, (972) 371-4448; www.dalsemi.com.* **CIRCLE 575**

LISTEN TO THE FUTURE!

Hear what the AK5392 can do for your next digital audio system!

Excellent digital audio sound starts with the ADC, and the AK5392 breaks new ground. With 116dB dynamic range and harmonic distortion below –105dB, the AK5392 provides far better performance than any monolithic audio ADC ever!

HiDS™ HIGH DYNAMIC SOUND

Until now, the leading audio ADC required two chips (in one package) and consumed almost 1W. The AK5392 is completely monolithic, using about half the power while providing higher reliability and lower cost – all with outstanding audio purity.

The AK5392 is only one of AKM's high-end digital audio products providing High Dynamic Sound (HiDS). Our product range includes ADCs, DACs, integrated ADC/DAC codecs, and even devices with on-chip DSP – ***if you have an idea for a new high-performance digital audio system, AKM can provide the converters to make it succeed!***

Let AKM help you get your next project to market on time and at the right price. With a comprehensive digital audio product line, innovative mixed-signal technologies, extensive internal fab capacity, and worldwide service and support, AKM can help make the future of your products bright!

AKM Digital Audio IC Sampler

	Bits	Channels ADC	Channels DAC	Comments
AK4324	24	–	2	105dB, 96kHz, 24-bit DAC
AK4526	20	2	6	Six 96kHz, DACs with stereo ADC
AK4540	16	2	2	AC'97 Compliant Codec for PC applications
AK5392	24	2	–	116dB 24-bit ADC using only 500 mW
AK7712A	20	2	4	Integrated codec with fully programmable on-chip DSP

The table provides an overview of the AKM HiDS digital audio product range. For more information on any of these or other AKM ICs, call us toll-free at **1-888-AKM-SEMI (1-888-256-7364)** or visit our website at **http://www.akm.com**. Make sure to ask for a free copy of our new Multimedia Audio Data Book!

AKM AKM Semiconductor, Inc.

USA: AKM Semiconductor, Inc.
2001 Gateway Place, Suite 650 West, San Jose, CA 95110
Phone: (408) 436-8580 • Fax: (408) 436-7591
E-mail: ICinfo@akm.com

Japan: Asahi Kasei Microsystems Co., Ltd.
TS Building, 24-10, Yoyogi 1-chome
Shibuya-ku, Tokyo 151
Phone: +81-3-3320-2062 • Fax: +81-3-3320-2072

Europe: Asahi Kasei Microsystems Co., Ltd.
22 The Courtyards, Hatters Lane, Croxley Business Park
Watford Herts, WD1 8YH, United Kingdom
Phone: +44 (0)1923-226988 • Fax: +44 (0)1923-226933

ISO 9001 Registered Company
Certificate Number FM31868

READER SERVICE 112

Line Driver/Receiver Offers High Current Output, Low Distortion

By implementing current feedback amplifiers in a 30-V complementary bipolar (CB) process with dielectric trench isolation, Texas Instruments Inc. has readied the THS6002. It's a dual line driver/receiver chip that delivers high output current for driving and receiving signals over low-impedance telephone lines. In fact, the THS6002 incorporates four isolated amplifiers on-chip, with two configured as differential line drivers, and the remaining two serving as differential line receivers.

Each amplifier offers 200-MHz input bandwidth with a slew rate of 1000 V/µs. While the THS6002's driver is rated to provide 400-mA peak output current with average capability of 66 mA (rms) into a 100-Ω line, the receiver assures very low total harmonic distortion (THD). The THD for the receiver is specified at –70 dBc. The amplifiers have high output voltage capability. And they can be configured for both single-ended and differential outputs. Typical differential output for the driver section of THS6002 is 23 V. Because each of the four amplifiers has its own power-supply pin, the crosstalk is significantly minimized.

Although, the THS6002 is being aimed at ADSL applications, it's suited for a variety of xDSL, cable, and other telephone networks. For thermal efficiency, the THS6002 comes in TI's thermally enhanced 20-pin PowerPAD package. Sampling now, the THS6002 is slated for production in the second quarter. Pricing is $5.67 in 1000-piece quantities. AB

***Texas Instruments Inc.**, Semiconductor Group SC-98002, Literature Response Center, P.O.Box 172228, Denver, CO 80217; 1-800 477-8924, ext.4500; www.ti.com/sc/opamp.* **CIRCLE 576**

Low-Cost 24-Bit Audio ADC Allows For System Upgrades

Crystal Semiconductor now offers a 24-bit, high-performance audio analog-to-digital converter (ADC). The low-cost CS5360 lets designers upgrade their existing 20-bit systems without any cost penalty. The CS5360, which is pin-compatible with the company's CS5335 20-bit ADC, performs sampling, analog-to-digital conversion, and antialias filtering. It operates on a 5-V supply and features 105-dB dynamic range. Other key specifications include 0.0025-dB passband ripple, 85-dB stopband attenuation, and 105-dB interchannel isolation. The CS5360 costs $7.50 each in 1000-unit quantities. LM

***Cirrus Logic**, Crystal Semiconductor Products Div., 4210 S. Industrial Dr., Austin, TX 78744; (512) 442-7555 or (800) 888-5016; www.crystal.com.* **CIRCLE 577**

DC-DC Converters Stuff Efficiency In A Small Package

National Semiconductor has 0.5-A versions of its high-efficiency Simple Switcher step-down power converters. The new devices, which come in SO-8 packages, feature efficiency ratings up to 96%, suiting them for battery-powered designs in which cool operation, long life, and small size are required.

The two parts—LM2671 and LM2674—are rated at 0.5-A output with only pc-board traces used as a heat sink. In addition, the higher frequency of the switchers, 260 kHz, lets designers build a power supply with five low-profile, surface-mounted components. Voltage options for the parts include 3.3, 5, and 12 V, as well as adjustable. The LM2671 and LM2674 are available in both the SO-8 surface-mount and 8-lead DIP packages. Pricing ranges from $2.48 to $2.94 in 1000-piece quantities. LM

***National Semiconductor Corp.**, 2900 Semiconductor Dr., Santa Clara, CA 95052-8090; (408) 721-5000; www.national.com/pf/LM/.* **CIRCLE 578**

Regulated DC-DC Converter Offers Low-Noise Output

The HK951 is a regulated, low-noise negative dc-dc converter with a maximum output current of 15 mA. The programmable negative voltage is developed using three low-cost 1-µF capacitors in a charge-pump configuration. To accommodate most battery setups, the HK951 accepts an input range of 2.6 to 6.4 V. For added flexibility, the output can be controlled using the output from the digital-to-analog converter of a microprocessor or a resistor divider. The programmable internal 5% linear regulator provides a negative voltage with a low-noise output ripple of 1 mV. The linear regulator has a dropout voltage of 0.2 to 0.4 V, depending on the load. The HK951 is available in an SO-8 package. Call for pricing. LM

***Shoreline Electronics Inc.**, 2098-B Walsh Ave., Santa Clara, CA 95050; (408) 987-7733; e-mail: ShoreElec@aol.com.* **CIRCLE 579**

Supply-Voltage Supervisor Works With 2.5-V Systems

The TLC7725 supply-voltage supervisor IC monitors and controls 2.5-V systems. Operating from 16 µA of supply current, the device is ideal for DSP-based cellular phones and a variety of other battery-powered systems.

The IC supervises power-supply lines during both power-up and power-down. On power-up, it issues a reset condition to the system's processor when the supply voltage reaches 1 V. When power is removed from the system, the IC issues a reset condition to the system's processor when the voltage drops below the 2.5-V sense threshold. The TLC7725 comes in an 8-pin TSSOP, SOIC, or plastic DIP. Pricing is $0.75 in 1000-piece quantities. LM

***Texas Instruments Inc.**, Semiconductor Group, SC-97059, Literature Response Center, P.O. Box 172228, Denver, CO 80217; (800) 477-8924, ext. 4500; www.ti.com.* **CIRCLE 580**

Dual Instrumentation Amp Comes In A Tiny Package

The INA2126 is a dual instrumentation amplifier (IA) that offers two complete precision IAs on a single chip. Each IA includes two precision op amps and feedback resistors. The two-op-amp per channel design provides good performance with low quiescent current (175 µA/channel), and a wide operating voltage range of ±1.35 V to ±18 V. Gain can be set from 5 V/V to 10,000 V/V with one external resistor. Laser-trimmed input circuitry provides low offset voltage (250 µV max), low offset voltage drift (3 µV/YC max), and excellent common-mode rejection. The INA2126 is available in SSOP-16 fine-pitch surface mount, SO-16, and 16-pin DIP packages. Pricing starts at $0.95 per channel in 100,000-unit quantities. LM

***Burr-Brown Corp.**, P.O. Box 11400, Tucson, AZ 85734; (520) 746-1111 or (800) 548-6132; Internet: www.burr-brown.com/.* **CIRCLE 581**

Now you only need *One* module for your Isolated Power Factor Corrected AC-DC applications...

STANDARD SIZE

(4.6" X 2.5" X .5")

- Power Factor Corrected
- Up to 200 Watts DC Power
- Universal AC Input Voltage (85 to 265 VRMS, 47-400 Hz)
- 9 to 48 VDC Isolated Regulated Outputs
- 380 VDC Tap Available

See PICO's full Catalog immediately on the Internet
http://www.picoelectronics.com

or send direct for
FREE 160 pg. PICO Catalog
featuring DC-DC Converters, AC-DC Power Supplies, Transformers, Inductors

For immediate engineering assistance – ***Call Toll Free (800) 431-1064***

PICO Electronics, Inc.

143 Sparks Avenue, Pelham, NY 10803-1837 • 914-738-1400 • FAX 914-738-8225
Internet: http://www.picoelectronics.com • **E-Mail: HLSC73A@prodigy.com**

VISA MasterCard

READER SERVICE 176

Burr-Brown Names Distributor For Discontinued Product Lines

Insight Electronics has become the exclusive worldwide distributor of Burr-Brown Corp.'s discontinued products. Shifting sales responsibility to a distributor will improve customer service for these products and give Burr-Brown's internal sales channels more time to focus on the demand created for its many new products, according to the Tucson, Ariz.-based IC manufacturer. Dennis Bourque, director of marketing at Insight Electronics, said, "This agreement allows Insight Electronics to support customers from design phase to product end of life. It's important that our customers know that the prices will remain stable and they will have long-term support."

The company cited two reasons for selecting Insight. "First, Insight has the ability to provide improved customer service for our customers purchasing discontinued products, and help in the selection of replacement products," said Joe Stoupa, Burr-Brown's North American distribution manager. "Second, Insight's Customer Development Center at their corporate headquarters in Diego has the staff and technical experience to support our international customers in the same manner as our domestic customers," Stoupa says.

For more information within the U.S., contact Insight at (800) 677-7716. International customers can call (800) 677-6011, or fax the distributor at (619) 677-3165. Products can also be ordered online through the distributor's home page at *www.insight-electronics.com*. Burr-Brown's web site at *www.burr-brown.com* also lists local Insight Electronics offices.

Pioneer Adds Online Services, Picks Up Hyundai LCD Line

A new web site feature offers 24-hour-a-day price and availability information on Pioneer-Standard Electronics Inc.'s lines of industrial and end-user electronic components and computer products. The company also signed on to distribute Hyundai Electronics America's entire line of LCD products.

To access the price and availability feature on the Cleveland-based distributor's web site (*www.pios.com*), customers click on the Industrial Electronic Division icon. They then enter any portion of a part number and select a specific manufacturer from the on-screen list. These clicks open a page that shows the full manufacturer name, Pioneer part number, product description, availability, and suggested resale price. Users can request a quote, data sheet, or sample by clicking on the part number.

The agreement with Hyundai means that Pioneer now handles a full-range of LCD products. Included are LEDs; monochrome passive-matrix displays for pagers, VCRs, cellular phones, and copy machines; and state-of-the-art active-matrix displays for laptop computers.

"We formed this partnership with Hyundai in direct response to the steady growth in market demand for leading-edge LCD technology," said Jim Jefferies, vice president of marketing for Pioneer's Industrial Electronics Div. "We believe the relationship will be mutually advantageous. Hyundai strengthens Pioneer's product offerings, especially in the realm of active-matrix displays," he said.

Microsemi Discrete Line Handled By Semi Dice

Semi Dice Inc., Los Alamitos, Calif., is now distributing Microsemi Corp.'s line of discrete components. Mitch Myers, Semi Dice president and COO, said that the distribution agreement is in response to an industry demand for Microsemi's products.

"Microsemi has one of the premiere discrete lines available, and we are very pleased to be working with them," said Myers. His company has been distributing die components since 1976. For more information on the Semi Dice line, call (800) 345-6633.

Microsemi, Santa Ana, Calif., supplies discrete semiconductors for information systems, telecommunications, space, military, medical, and industrial applications.

Pick-And-Place System Gets Japanese Distributor

Kaijo Corp., Tokyo, Japan, has agreed to distribute the APS-1 pick-and-place system and related products from Quad Systems Corp. in Japan, and to Japanese customers outside of Japan.

The APS-1 can be configured for a wide range of advanced SMT and semiconductor die-attach processes, including direct-chip attach and flip-chip bonding on BT, FR-4, polyester, polyimide, lead frame, and ceramic substrates. Options also allow the system to place both bare die and SMT devices on the same substrate in one pass.

"We are pleased to join forces with Kaijo," says David Smith, the president and CEO of Quad Systems. "This alliance will make Quad's line of SMT offerings available to a greater number of circuit manufacturers worldwide," he says.

Avnet Computer Offers Compaq's High-End Servers

Avnet Computer has added Compaq Computer Corp.'s high-end, enterprise-level, ProLiant and ProSignia servers to its line. Company officials said that Compaq was looking to leverage Avnet's experience in providing technically complex solutions in the RISC/Unix marketplace.

Avnet will benefit from the distribution agreement by adding Compaq to its list of offerings from Digital Equipment, Hewlett-Packard, and IBM. The distributor also will be able to maximize its network integration and migration services by leveraging Compaq's leadership in Microsoft Windows NT server and desktop computing environments. Avnet Computer president Andy Bryant said that customers have been asking for Compaq-based solutions. "This new alliance strengthens our offerings and furthers our position as a multivendor solutions integrator," he added.

Information technology professionals in sophisticated computing environments want a technology partner that can support them as their needs grow, according to Bob Fernander, vice president of enterprise marketing at Compaq North America. "By forming this alliance with Avnet computer, we offer the expertise and dedication to customer satisfaction that our customers need to confidently deploy Compaq systems within their organizations," he said.

WHAT DO THESE WORDS MEAN TO YOU?

TECHNOLOGY • APPLICATIONS PRODUCTS • SOLUTIONS

After much thought and discussion, our editors have developed a new tag line that is about as direct and to the point as one can possibly get. It describes who we are and what we do. These four words tell our readers and advertisers what *Electronic Design* is all about:

TECHNOLOGY•APPLICATIONS•PRODUCTS•SOLUTIONS

This new tag line reflects how *Electronic Design* reports on both emerging and new *technology* garnered from the movers and the shakers of this global industry. We report on and analyze how new technology will work in various *applications*. We then report on and analyze new *product* introductions. Finally, we offer you, our readers, *solution* articles and design ideas that help you and your peer engineers to build better products in this very competitive arena. These four words also represent the stages in which you, the design engineer, work.

It's remarkable how these four simple words reflect our dynamic mission to the industry.

ELECTRONIC DESIGN

TECHNOLOGY•APPLICATIONS•PRODUCTS•SOLUTIONS

Business Briefs

SciTech International, Chicago, Ill., has reorganized its distribution channels to better focus on its mission to market technical software and hardware to resellers. The operation, which was previously known as SciTech Select Distribution, is now named Technical Distribution Co. (TDC). "Reseller sales have grown over 100% during the last year, and we feel this change will establish a more independent business unit," says Barry Moltz, SciTech's CEO. "TDC's creation will allow our wholesale distribution effort to better serve its customers," he says. TDC can be contacted at: (800) 622-3320 or (773) 486-9399; fax (773) 486-1787; e-mail: info@technicaldistribution.com.

Avnet's Global Technical Distribution Group (GTDG) has expanded its operations into the Asian RF/microwave, fiber-optic, and other specialty electronics markets with the purchase of Excel-Max Communication Pte., Ltd. in Singapore. Excel-Max, which will be renamed Avnet GTDG Singapore, serves the Singapore, Malaysia, and Thailand markets. It had sales of about $3 million in its last fiscal year.

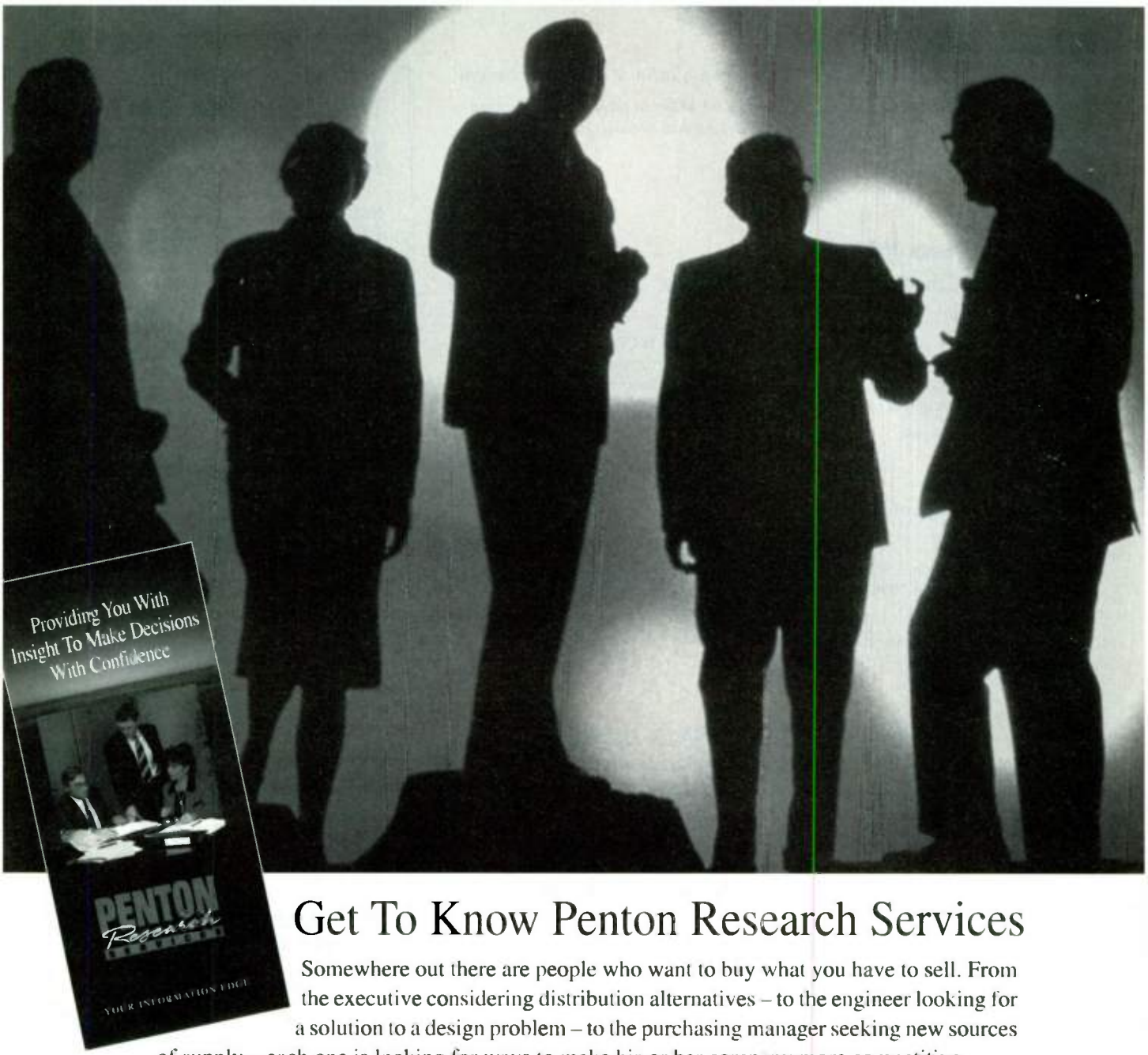
Coghlin Electric/Electronics of Westboro, Mass., has acquired Armor Electronics, Tewksbury, Mass., a distributor of electronic components and a value-added assembler of custom battery packs. Bob Rikeman, formerly president of Armor Electronics, will become general manager of the Armor Div. of Coghlin Electric/Electronics. Coghlin is a single-source supplier of electrical and electronic components in the New England market.

Bisco Industries Inc. has opened its 13th facility in the U.S. The new office is at 321 West Ben White Blvd., Austin, TX 78704; (512) 448-4550; fax (512) 448-4862. Bisco offers components and fasteners, primarily serving the electronic, fabrication, and aerospace industries.

People On The Move

Mark James has been promoted from sales representative to sales manager at Bisco Industries Inc.'s Sacramento, Calif. facility...Kristine Albers has been promoted from sales representative to assistant sales manager at Bisco's Brookfield, Wisc. facility.

Need To Know What They Know?



Get To Know Penton Research Services

Somewhere out there are people who want to buy what you have to sell. From the executive considering distribution alternatives – to the engineer looking for a solution to a design problem – to the purchasing manager seeking new sources of supply – each one is looking for ways to make his or her company more competitive.

The professionals at Penton Research Services can help you discover what they buy and why, from whom – and even what they are looking for. Before you decide on a new product or marketing effort, invest in the knowledge you can trust from Penton – a leader in business information and communications for over 100 years.

When you need to know, get to know Penton Research Services.
You can start by asking for this informative brochure, today.

Penton Research Services
1100 Superior Avenue • Cleveland, OH 44114-2543
Call: 216.696.7000 Toll-free: 800.736.8660
Fax: 216.696.8130
E-mail: research@penton.com
http://www.penton.com/corp/research

PENTON
Research
SERVICES
Your Information Edge

Low-Power Design

Center Suisse d'Electronique et de Microtechnique SA & Electronic Design

This collection of papers focusing on the minimization of power consumption features general tutorials, digital circuits, devices and analog circuits of low-power systems.

Softciver book, $125.00, Item B4023PM

Portable By Design 1997,

Proceedings of the Fourth Annual Conference

Electronic Design

An overview of the conference topics including MCUs & CPUs for portable devices; battery technologies; IR-based wireless communications; thermal & mechanical considerations; and more. Ideal for design engineers of portable, nomadic, mobile and transportable products.

Softcover book, $175.00, Item P2365PM

Electronic Design on CD-ROM

Electronic Design

Includes all the articles, illustrations and line drawings that appeared on the pages of ED between 1990 and 1994. Complete with search engine and hypertext links.

CD-ROM , $95.00, Item C1612PM

The editors of ELECTRONIC DESIGN are actively seeking and reviewing book manuscripts for article series and/or a potential book publishing project. Authors of electronic original equipment/products/systems books are invited to submit a chapter outline along with a brief description of their work for publishing consideration.
Please include a brief description of primary target market and sales potential. Send to: Product Manager, Penton Institute, 1100 Superior Ave., Cleveland, OH 44114.

Clearance Items... While Supplies Last! 10% Off Original Prices

Standard Handbook for Electrical Engineers, 13th Edition

Hardcover book, WAS $110.50 - NOW $99.45, Item B2000PM

Web Page Design: A Different Multimedia

200 pp, softcover book, WAS $24.95 - NOW $22.45, Item B2421PM

C++ for Professional Programmers with PC & UNIX Applications

556 pp, softcover book, WAS $42.95 - NOW $38.65, Item B2456PM

Patterns of Software Systems Failure and Success

292 pp, softcover book, WAS $44.95 - NOW $40.45, Item B2461PM

Object-Oriented Modeling and Design

528 pp, softcover book, WAS $60.00 - NOW $54.00, Item B2557PM

The Year 2000 Software Crisis: Challenge of the Century

522 pp, softcover book, WAS $39.95 - NOW $35.95, Item B2720PM

Please Add $5.00 shipping for first book and $1.00 for each additional book.

Subtotal $_____
Add State Sales Tax $_____
Shipping & Handling $_____
TOTAL $_____

Item #:
_____/_____/_____
_____/_____/_____

Check/MoneyOrder (U.S. Currency made payable to *The Penton Institute*)

Foreign orders — Please call for rates

Sales Tax:

CA	8%	IL	6.25%	NY	8%
CT	6%	MA	5%	OH	7%
FL	6%	MN	6.5%	PA	6%
GA	6%	NJ	6%	WI	5.5%

CANADA....7%

ED PPM

Penton Institute

10 DAY MONEY-BACK GUARANTEE

Name: _____ Title: _____ E mail: _____

Company: _____ Telephone: (____) _____ Fax: (____) _____

Company Address (no P.O. Boxes): _____ City: _____ State: _____ Zip: _____

Account No.: _____ Expiration Date: _____ Bill Me _____ P.O. #: _____

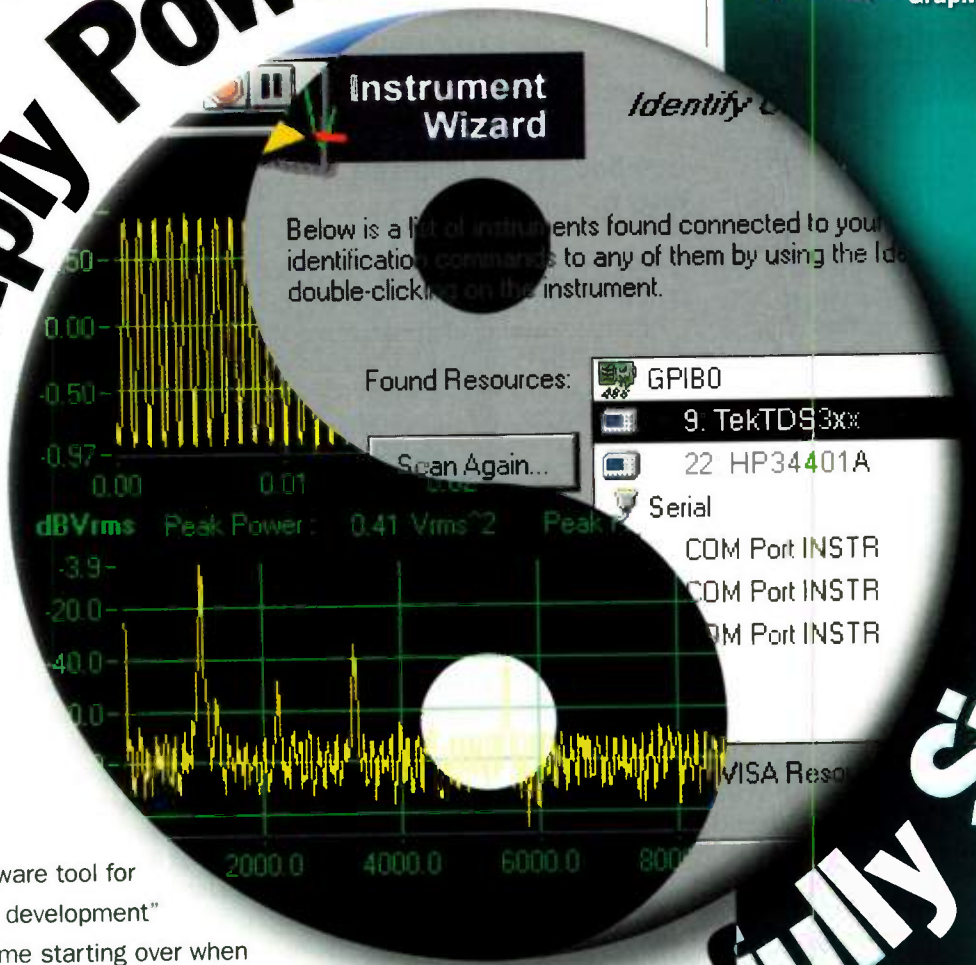
Signature (required): _____ Circle type of Charge: MC VISA AMEX DISC

PHONE 1-800-223-9150 • FAX 216-696-4369• http://www.penton.com
The Penton Institute • 1100 Superior Avenue • Cleveland, Ohio 44114-2543

NEW! LabVIEW 5.0

Simply Powerful

LabVIEW™
Graphical Programming



Powerfully Simple

Why buy a software tool for "rapid application development" and then waste time starting over when your tool simply isn't powerful enough?

With LabVIEW 5.0, there are no compromises. LabVIEW has the simplicity of a graphical development environment AND the power of a complete programming language. With just a few mouse clicks, you can create complete measurement and automation solutions with the new development wizards. You also get powerful 32-bit multithreading technology, distributed computing tools, and compatibility with all industry-standard ActiveX controls.

Discover true productivity with LabVIEW, the industry-leading software package for instrumentation.

www.natinst.com/labview

Call today for your FREE fully functional LabVIEW 5.0 Evaluation Package
(800) 661-6063
(U.S. and Canada)

NATIONAL INSTRUMENTS™
The Software is the Instrument™

U.S. Corporate Headquarters
Tel: (512) 794-0100 • Fax: (512) 794-8411 • info@natinst.com
Worldwide network of direct offices and distributors.

READER SERVICE 117

Push-Pull Solenoids Have You Coming And Going

Bicron Electronics Co., Canaan, Conn., has issued a new four-page brochure detailing its line of small, push-pull tubular solenoids. Such devices can be used in a broad range of applications wherever a short stroke with high force and low power is required. Selection criteria, photos, dimensional drawings, typical force curves, and power requirements are given for five different models ranging from 0.45 in. diameter to 1 in. diameter. Call (860) 824-5125; e-mail: *info@crn.com*; *www.solenoid.com*. RE

CIRCLE 507

It's A Terminal Block Party Thanks To New Catalog

The MAGNUM Euro-Mag Terminal Blocks, the newest product line from Bussmann Circuit Components, Chicago, Ill., are detailed in a 17-page catalog. Complete specifications, illustrations, and ordering information are included. The terminal blocks are available in various center spacings, such as 3.81, 5.00, and 5.08 mm. All blocks have full agency approvals are are available in horizontal, vertical, and 45° angle wire orientations. An easy-to-use guide cross-references the Euro-Mag blocks to several other European-style terminal blocks. For more information, call (708) 867-4600; fax (708) 867-2211. RE

CIRCLE 508

Mammoth Instrumentation Catalog Measures Up

The new, full-color 1998 *Instrumentation Catalog* from National Instruments, Austin, Texas, contains 864 pages detailing more than 600 software and hardware products for measurement and automation applications. Featured are tutorials on data acquisition, GPIB, VXI, and industrial communications; product line overviews; and selection guides. The comprehensive tutorials are supported by application examples. Product highlights include PXI modular instrumentation, Fieldpoint distributed I/O, computer-based instruments, and a new line of motion-control devices. For a free copy of the catalog, call (800) 433-3488 or (512) 794-0100; fax (512) 794-8411; e-mail: *info@natinst.com*; *www. natinst.com*. RE

CIRCLE 509

Gas-Booster Catalog-On-Disk Isn't Full Of Hot Air

Available free on computer disk is Haskel International Inc.'s (Burbank, Calif.) new catalog of air-driven gas boosters. The catalog combines technical data with a selection guide. Formatted for MS-Windows, the disk prompts customers to specify desired performance parameters such as gas type, flow rate, and pressure. It then recommends the most suitable booster, using graphic illustrations. Dimensions, materials, and connections are detailed, coupled with performance graphs. For further information, call (818) 843-4000; fax (818) 841-4391; e-mail: *pduffy@haskel.com*; *www.haskel.com*. RE

CIRCLE 510

Rulers And Scales And Layout Tools, Oh My!

Products for applications that require accurate measurement, inspection, layout, drafting, and so on are described in a new 32-page catalog from GEI International Inc., Syracuse, N.Y. The range of devices runs from simple rulers to sophisticated optical microscopes capable of measuring as small as 0.0005 in. Over 400 different styles and types of rulers are covered, with scale lengths from 2 in. to 196 in. The magnifier and measuring-device section includes linen testers, microscopes, collimators, depth gauges, thickness gauges, optical comparators, etc. To get the free catalog, call (315) 463-9261; fax (315) 463-9034. RE

CIRCLE 511

Frequency Accuracy Is The Rule In Application Note

Anritsu Co., Morgan Hill, Calif., has issued an application note titled "Understanding Frequency Accuracy in Crystal Controlled Instruments." Described in the note is frequency accuracy for test equipment such as synthesized signal generators, network analyzers, frequency counters, spectrum analyzers, etc., that uses quartz crystal time-base standards. Uncertainties from effects like temperature, time, and gravity are discussed. Straightforward methods are presented to determine overall frequency uncertainty. Call (408) 778-2000; fax (408) 778-0239. RE

CIRCLE 512

Hook Up With Unique Interconnect Solutions Guide

A guide that's a paradigm for solving interconnect challenges. That's what Emulation Solutions, Sunnyvale, Calif., is offering in its new *InterConnect Reference Guide*. Provided among its 28 pages is in-depth coverage of the company's full product line support and a "how-to" on specifying interconnect solutions. Instead of a traditional phonebook catalog, this guide details pertinent information for selecting the right adapter. The range of adapters includes emulators, and programmer, logic-analyzer, prototyping, and production adapters. The free guide can be obtained by calling (408) 745-1524, or by going into their web site at: *www.adapters.com*. RE

CIRCLE 513

News Flash: Broadcast Product Guide Has Arrived

Trompeter Electronics Inc., Westlake Village, Calif., has published its first *Broadcast Product Guide* for audio and video applications. Included over the course of its 28 pages is detailed information and selection charts on patch jacks and patching accessories, standard and custom panels, connectors, and cable assemblies. The free guide is setup to become an easy-to-use tool for selecting standard and digital components for broadcast stations, Electronic News Gathering (ENG) and remote vans, and transmitters and towers, as well as wireless systems. Call (800) 982-COAX or (818) 707-2020; fax (818) 706-1040; *www.trompeter.com*. RE

CIRCLE 514

ELECTRONIC DESIGN ONLINE

TECHNOLOGY·APPLICATIONS·PRODUCTS·SOLUTIONS

Get Immediate Online Access To Worldwide Technology

Electronic Design Online has been created for you, the design engineer, as the world's most comprehensive technical information resource and solution center. It offers a compendium of topics—from the contents of current *Electronic Design* issues including all the articles, schematics, and QuickLook features to ED University, Pease Porridge, Career/Job Bank, and more. Link up to our web site today for online forums, direct links to industry organizations and advertisers, trade show previews, industry surveys, technology archives, and humor. In addition, you can now utilize ED JetLINK, the industry's fastest "drill down" tool to find application- and market-specific product solutions and vendors with a minimum number of clicks in one site visit.

www.elecdesign.com

E-Z Does It

I have been reading *Electronic Design* for over 20 years now and generally enjoy the magazine. Like most engineers, I receive so much information that I have begun to "skim," meaning that I check the index for articles of interest rather than reading cover to cover.

My company, in fact, the last three companies I have been with, do not rush to "state-of-the-art" technology. We still use through-hole parts and are quite happy with them. The division in which I work produces medical devices. They each sell from $10,000 to $30,000 a piece and we normally sell from 100,000 to 200,000 pieces a year. I hope you will keep in mind the "small and not-quite-so-sophisticated" user, since I believe that we are not alone out there.

Alan Cross-Hansen
Senior Electrical Engineer
E-Z-EM
acrossh@ezemsp.com

With This Ring...

I have read Ray Alderman's column "From Buses To Rings" *(Nov. 3, 1997, p. 92)* with great interest. I was surprised that the IEEE Standard 1596 (Scalable Coherent Interface, or SCI), which is based on rings, was not mentioned.

From a standard with merely academic interest (e.g., data acquisition for CERN), to products with industrial applications, it has shown quite impressive growth. Superconductor manufacturers like Data General, Sequent, or HP/Convex are currently applying it. But with PCI plug-in boards from Dolphin, it also is ready for embedded- or PC-based systems.

The fact that SCI is an established standard will allow the mixed use of products from different manufacturers. ISS *(http://www.iss-us.com)* has announced an ASIC core and PCI boards, and Lockheed Martin will build a switch. Therefore, rings are already available for the desktop with up to 1 Gbyte/s per link.

Andreas Doering
doering@iti.mu-luebeck.de

Ray Alderman responds: The column I wrote on rings was just an introduction. I didn't go into all of the derivations like SCI or Sebring. They have added mechanisms to manage some of the latencies introduced by basic ring topologies. The column was written to show some of the problems with such a topology.

Rings are not mainstream architectures at the desktop or other segments of the computer industry. First, all rings are loosely coupled architectures with severe latency problems, as compared to other techniques of hooking nodes together. Rings could solve the multiprocessor problems with PCI, but at the expense of nondeterministic behavior. Second, rings are not particularly scalable compared to switched fabrics like circuit-switched or packet-switched crossbars.

If you can live with nondeterminism, not passing interrupts through the ring, and low scalability, then rings are appropriate. You can do the same architecture with a network topology and protocol for less cost, and get the same performance results depending on the protocols you use. Ultimately, a single ring suffers from a single point of failure and low survivability. To solve this problem, designers use counter-rotating multiple rings.

In addition, not too many people are excited about SCI for a number of reasons. It's an academic architecture when you look at its popularity in the market. Rings perform well in broadcast mode doing WRITES, but not well when doing READS. Adding state machines to translate protocols (like PCI to a ring topology) simply introduces more latency, but your software doesn't need to have complex drivers to "program the hardware." My opinion is that rings are interesting to play with, but not practical in mainstream computing markets. There are other technologies and topologies that are higher in performance, cheaper, and more deterministic.

It IS Easy Being Green

Re: Designing for the Environment, or "Green Engineering"

I like it. But, I don't think it's all that big of a deal. Important, yes. Hard, no. The answers are simple, like recycling, and using the most efficient design the budget will allow. Coming from a long line of Scotsmen, I hate throwing things out, even a few milliwatts.

[Green engineering] means building things that don't break, at least not very often. Some products I designed 20+ years ago are still in service. If things don't break, the customer stays happy. He or she keeps the gizmo longer and I don't have to spend time fixing it. When the customer needs another one, guess who gets the business? Happy customers are repeat customers.

It takes a bit longer to design, and costs a bit more. The bean counters may get upset, but in the long run, you win. One unhappy customer wipes out all the money you saved on that cheaper part.

It means designing for recycling. (I wish the nuclear power industry had thought about this.) Eventually, everything dies and gets thrown out. And the world turns into a garbage dump. We have to recycle.

We don't need a bunch of regulations, just common sense. That may be a bit like asking for an honest politician...

Tim Conrad
Principal Engineer

Corrections

On page 27 of the Oct. 13, 1997 issue, the incorrect contact information was given regarding the Technology Newsletter item entitled "Computer Telephony Group Seeks Open DSP Interface." The correct contact information is as follows: Martin Lippman, vice president of marketing, Commetrex, (770) 449-7775, ext. 370; e-mail: mlippman@commetrex.com.

On page 148 of the same issue, the product module featuring the GT Plus Oncore GPS Receiver from Motorola contained incorrect phone and fax numbers. The correct phone number should be (888) 298-5217. The correct fax number should be (847) 714-7325.

We apologize for the errors.—*Ed.*

Letters to the Editor, including the writer's name, address, and daytime phone number, should be sent to: **Letters Editor, Electronic Design, 611 Route 46 West, Hasbrouck Heights, NJ 07604; fax (201) 393-0204; e-mail: debras@csnet.net.** *Letters may be edited for space and clarity. Names and other information will be withheld upon request.*

DSP World Spring Design Conference

April 21-23, 1998
Santa Clara, CA

DSP World Spring Design Conference will offer hands-on, practical instruction in commercial applications such as **communications, multimedia, transportation, industrial, and many more!**

Covering topics such as:

- **Embedded Parallel Processing Satellite Modems**
- **Software Radio: Using DSP to Implement Radio Systems**
- **Selecting DSP Processors for Wireless Communications Applications**
- **DSP-Enhanced Digital Radio Systems for Multi-Channel Voice and Data Reception**
- **Advanced Digital Receiver Design for Paging and Narrowband PCS**

...and more!

Be sure to check out our website at www.dspworld.com!

Send me more information!

I am interested in:
☐ attending ☐ submitting an abstract
☐ exhibiting

DE982

April 21-23, 1998
Santa Clara, CA

Name _____

Title _____

Company _____

Address _____

City _____ State ____ Zip _____

Phone _____ Fax _____

Email _____

Phone: 888.239.5563 • Fax: 415.278.5200 • Mail to: DSP Spring Design Conference • Miller Freeman, Inc.
525 Market Street, Suite 500 • San Francisco, CA 94105-2713

Your First Computer. Your First Car. Your First Product.

We've been with you every step of the way.

Without Teradyne products, some of the greatest innovations in technology may never have occurred. Because Teradyne plays an integral role in testing and developing new technology, we've been a part of virtually every innovation that's had a dramatic effect on your life . . . and career path. As the world's largest supplier of automated test equipment (ATE) and software for the electronics and telecommunications industries, we've grown 100-fold, from sales in 1971 of $13 million to sales in 1996 of $1.2 billion. And we've been involved in a wide spectrum of areas over the past 40 years, including automotive, telecommunications, wireless, peripheral, and consumer products. When you join a company with our level of success, cutting-edge resources are never further than arms' length. And neither are the many, unique outlets in which to apply your talents. We've always been a part of your life . . . now become a part of ours.

Applications Engineers

Several exciting career opportunities are now available for enthusiastic professionals to perform customer applications support of Teradyne's Analog, Memory and Advanced Mixed Signal products. The right candidates will utilize their superior project management skills in performing the following responsibilities: application specific test program development; software, design/debug, Analog/Digital, hardware design and debug, test strategy, and program creation for advanced semiconductor devices; interface design, and development of system-level design ATE solutions.

Requirements:

- MSEE/BSEE/BSEET or BSCS (or equivalent experience)
- 2+ years' experience with IC testing in either a manufacturing, design or Fab environment.
- UNIX, C/C++ and Sun
- Project management skills

Preferred Skills:

- Knowledge of ATE linear/mixed signal devices
- 2-3 years' experience as a test engineer or ASIC design engineer

Pre-Sales Applications Engineers

We are currently looking for enthusiastic professionals to support our sales staff for major accounts. You will be responsible for establishing technical differentiation and strategic planning on accounts with sales team. Mixed signal, Memory, Digital, In circuit test, Analog, VLSI/AISI, ATE Engineering experience.

Requirements:

- MSEE/BSEE/BSEET or BSCS (or equivalent experience)
- 2+ years with IC testing or design in a manufacturing, design or fab environment
- UNIX/C

Sales Engineers

Enthusiastic professionals are needed to sell Teradyne products and services in assigned territories. You will be responsible for integrating account strategy established with division and support groups, utilizing TQM in account management processes.

Requirements:

- MSEE/BSEE/BSEET or BSCS (or equivalent experience)
- 3+ years' experience in capital equipment sales

Service Technicians/Engineers

In this position, you will support our customer base both on- and off-site.

Requirements:

- BSET/BSEE
- ATE/Service experience (strong Electrical/ Mechanical aptitude)

These opportunities are available in the following locations:

Irvine, Folsom and Sunnyvale, CA; Portland, OR; Chandler and Tempe, AZ; Austin and Richardson, TX; Burlington, VT; Waltham, MA; Boise, ID; and Manassas, VA.

If interested in opportunities on the **West Coast**, please forward resume to: **Teradyne, Inc., Attn: ED2, 820-A Kifer Road, Sunnyvale, CA 94086.** Or call: **(408) 732-8770, x. 240.** Fax: **(408) 735-7141.** E-mail: **Kelly_Carlson@notes.teradyne.com.**

If interested in opportunities on the **East Coast**, please forward resume to: **Teradyne, Inc., Attn: ED2, 186 Third Ave., Waltham, MA 02154.** Or call: **(781) 890-2080, x. 271.** Fax: **(781) 487-2248.** E-mail: **personnel.waltham@teradyne.com.**

Take the first step . . . and make your first truly rewarding career move with Teradyne. We offer a competitive salary and benefits package, including profit sharing, 401(k), 100% educational assistance, and stock purchase plan.

TERADYNE

Visit our web site at: **www.teradyne.com.**

An Equal Opportunity Employer.

Technical Training: There's No Substitute For A Well-Trained Individual

Vic Rossi, Jr.

Many engineers, managers, and supervisors are responsible for the operation of complex systems which perform complicated processes. These processes, often run by people, produce products that must measure up to marketplace-competitive levels, meet quality standards, and satisfy customer demands. A key element in producing a competitive product is recognizing the importance of well-trained technical personnel.

There is absolutely no substitute for a knowledgeable, well-trained technical staff, and the absence of which will seriously impact a business. Unfortunately, in many industries, including high-tech electronics companies, the work force is not always provided with adequate technical training to address daily, routine requirements. Even when training is provided, the skills involved are, for a variety of reasons, never properly learned and/or applied.

The most significant difficulty associated with technical training is that it looks easy to develop and present. It also looks like virtually anyone can do it. These are common, but incorrect assumptions. The development of effective training programs requires a significant amount of talent, time, and effort on the part of the trainers, and commitment on the part of management to initiate the program and see it through to completion.

Training is much more than taking a body of technical information and presenting it to the work force. Training programs based on this presumption are doomed to disappointing results. The target audience, the adult student, is far too complex to allow this simple approach.

Effective technical training is the result of analyses, thought, preparation, and commitment. And, while this may appear to be quite a load to carry, the final dividends are well worth the time and effort. It is a generally accepted fact that if waste or rework can be reduced by 5%, net profit can be increased by at least 50%. This alone should draw the interest of most management personnel.

Training Basics

To understand the factors of the training process, we must take a look at some fundamental concepts of training. First, all operations (also called functions) such as changing a tire, playing a round of golf, wiring a motherboard, or assembling a chassis, comprise a series of individual, sequential tasks which are observable and have both a start and a finish. Each task can also be broken down into elements. Close observation of a capable employee performing his or her work assignments will reveal that these divisions of work actually exist: operation, task, subtask, and subtask element.

Performing of tasks is based upon information components (knowledge), and performance components (skills). You may know how to drive a golf ball 275 yds, but you might not have the skill to do so. Essentially, all operations and their tasks are based on the knowledge and skills of the individuals performing them. To put this fact into the context of technical training, knowledge is taught in the classroom, while skills are taught at work stations, or reasonable simulations of work situations. On-the job-training, is the skill-learning process conducted under real work circumstances. It can be divided into: task performance, knowledge, and skills.

Let's look at the golf analogy once again. Tiger Woods can consistently drive a golf ball 280 yards because he knows how to, and has perfected the skill through intense practice sessions. Gary Player once disclosed that he had hit more than 1.5 million balls on the practice tee over the course of his golfing career. Arnold Palmer once stated that tournaments are won on the practice green, not on the golf course. Learning a skill—any skill—requires practice, which becomes an integral part of technical training.

The process begins with detailed task analyses of the operations targeted to be trained. Task analyses are written records of operations as they are performed. By using them, those task requirements can be accurately covered during training sessions.

Generally, task analyses include a list of tasks, subtasks, and elements observed during an operation. This is usually a two-step process which involves the initial observations and a verification by several experts in the task. Before proceeding in the training development process, task analyses must be checked for incorrect information, unauthorized activities, and other factors which could jeopardize the accuracy of the training documents.

Task analyses also are used to write comprehensive and effective standard operating procedures. In this case, the analyses should be limited to only the task involved, otherwise they become too detailed and must be revised frequently. The task analyses, and later the training lesson plans, should be organized to the system's operational cycle. They should include equipment setup, startup, normal operations, troubleshooting, preventive maintenance, process documentation, and other topics as appropriate.

There are two purposes for segmenting system operations into integral parts. First, it simplifies the information collection process by handling several manageable parts rather than one potentially unmanageable whole. Second, organizing the topical information into sections and subsections assists the student in organizing the new information into the existing body of

knowledge they bring into the situation. An elephant can be eaten one bite at a time, but trying to eat the whole animal all at once would result in absolute failure. In effect, we are dividing the technical-training elephant into bite-sized pieces.

A Training Plan

The entire training experience should be guided by a comprehensive plan developed prior to the onset of any formal effort. Basically, the plan is the rulebook by which the training game is played. It is a multifaceted document which addresses everything from determining the need for training to the means of evaluating the effectiveness of the training. Because the success of a training effort depends largely upon the accuracy and completeness of the plan, it is best to bring in a professional to assist in its creation.

Briefly, the plan must include sections which describe how to define and address the need for training. Some problems may result from other issues such as management problems, interpersonal relations, or absence of supervision. The plan also describes individual roles in the process, such as trainers, and what attributes should they bring to the effort. Also, the plan maps the design of the training lesson plans, and what criteria will be used to evaluate their effectiveness.

The training plan must clearly state who will be responsible for managing its implementation, how work schedules will be juggled to allow time off for training, as well as access to equipment to be used in training. The plan must also address other training issues, such as rewards for successful completion, changes generated in personnel performance records, assignment of room space for training, and any other issue directly related to the program.

Training Process

To implement elements of the plan, trainers must be recruited, screened, and prepared to participate in a process called "train the trainer." With the proper attitude, professional credibility, communication skills, technical knowledge, and the desire to help others, almost anyone can become a trainer—given the correct instruction and guidance. It is far easier to convert one of your own technical people into a trainer than it is to have a trainer learn all the technical knowledge needed to work in your environment.

Generally, it takes about a week to present all the information that a trainer should know and apply in the training environment. Add to that a week of practice under the watchful eyes of an experienced trainer and your instructors should be able to handle the classroom situation.

Correctly designed and developed lesson plans will make the trainer's job relatively easy. Each lesson should include a statement of purpose; instructions for the trainer, such as lesson length and time required for the on-the-job training segment; and a list of objectives to be met for a particular lesson. A list of support materials, such as visuals, samples, examples, and other items to be brought into the classroom should also be listed in the lesson plan. The purpose of the lesson plan is to guide the trainer, as well as provide the necessary topical information.

Learning assessments, in the form of progress evaluations, are given at the end of each lesson to determine if learning has, indeed, occurred. Progress evaluations should include from 10 to 20 multiple-choice and true-false questions. And, the questions should not be overly difficult to answer correctly. The purpose here is to promote learning, not stifle it by failure.

These evaluations should not be called "tests" because that word seems to scare people. This is particularly true of trainees who haven't been in a classroom situation for 10+ years. The progress evaluation is used not only to determine the trainee's performance, but the trainer's ability to present information in a manner which promotes learning. Individuals should be allowed to correct their own evaluations before moving to on-the-job training.

On-The-Job Training

On-the-job training consists of applying knowledge learned in the classroom to the skills necessary for individuals to perform their assigned operations. It involves a three-step process: telling individuals how to perform a task, showing them how to correctly perform the task, and then allowing them time to practice performing the task.

To implement, control, and manage the on-the-job training process, a task checklist from the training materials is used. As each task is completed, the tell, show, and practice portions are circled to keep track of where that trainer stands in the process. This method allows the trainer to continue the next training session where the first left off. It also eliminates duplication of effort should another trainer become involved.

Next, a performance demonstration is conducted, during which the trainee must successfully complete the task without any assistance. As with the classroom progress evaluation, records of successfully completed performance demonstrations should become part of the trainee's personnel file.

Both the progress evaluation and the on-the-job training checklist are important management documents because they show which members of the staff are qualified to perform specific operations. This should significantly reduce waste, rework, and other undesirable results of having unqualified personnel assigned to perform critical operations. Nothing can be more disconcerting to a manager than to assign a critical operation to someone lacking the required degree of knowledge or skill to perform up to accepted standards.

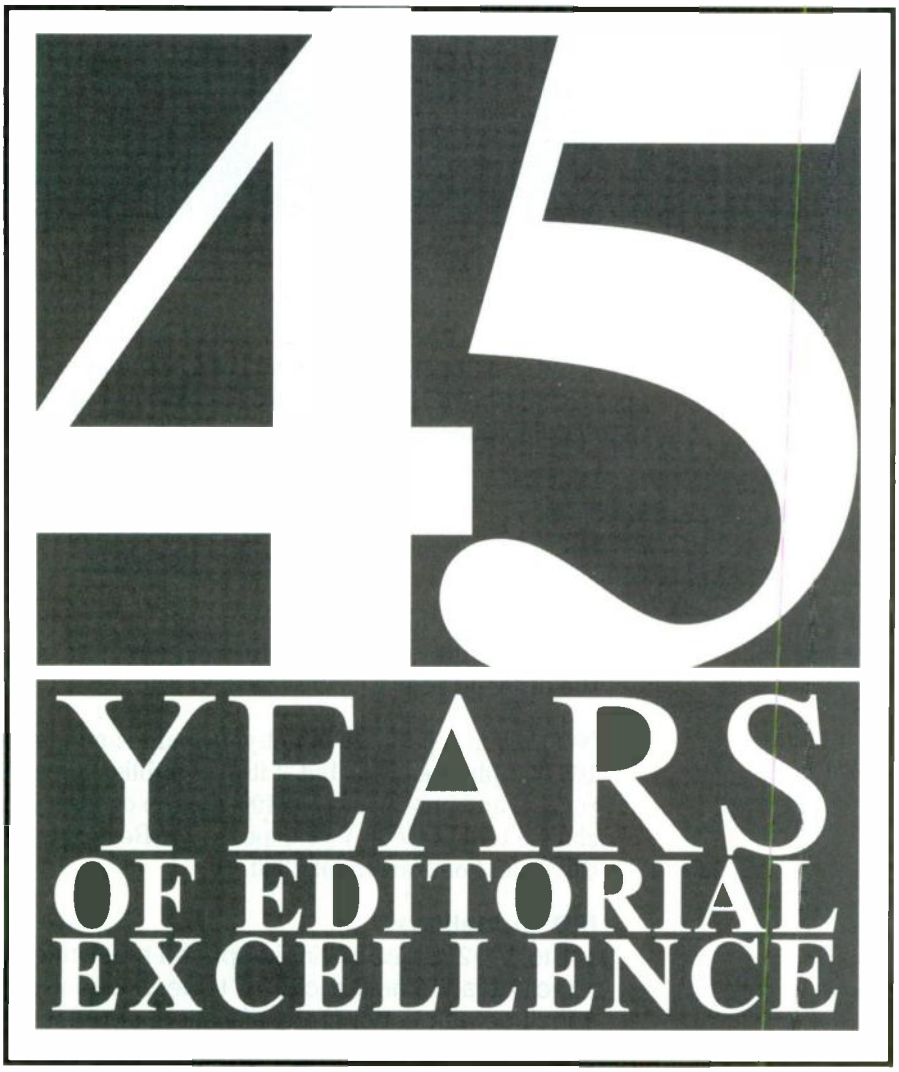
Effective technical training programs are worth the time, effort, and expense required for their correct design and implementation. In addition to having a profound impact on the success of any company, training also fulfills a basic need in the adult trainee. While most of us are concerned about the money we make in performing of our professions, there is also satisfaction derived from a job done well.

Satisfaction also plays a similar role in the daily activity of our employees and is derived from a sense of accomplishment, workplace involvement, and potential for growth. The successful completion of a training program provides that sense of accomplishment, workplace involvement, and certainly offers potential for growth within the company.

Vic Rossi, Jr. is an independent instructional design consultant with nearly 20 years of technical training experience in a wide variety of high-tech business and industrial applications. Rossi may be reached at (610) 942-9438.

ELECTRONIC DESIGN

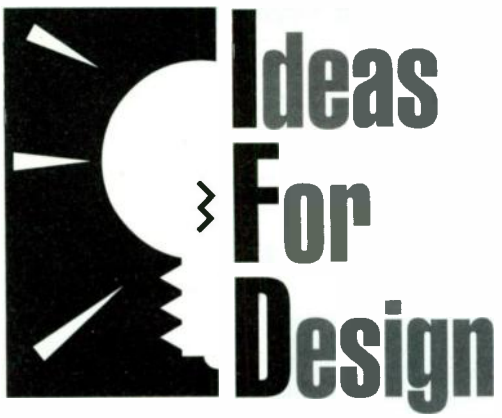
Your Strategic Information Partner



Electronic Design's on-going objective is to observe and report the latest breakthroughs in EOEM technology. By providing this information, *Electronic Design* has been the strategic partner of system designers and suppliers for the past 45 years, helping to bring them together so they can deliver more competitive products to market faster.

A PENTON PUBLICATION

Got A Cool Circuit Idea?



Flex Your Creativity In Electronic Design

You get *Electronic Design*. What do you turn to first? Ideas For Design (IFD)? You're not the only one — our own studies as well as those conducted by independent surveying firms continually show that Ideas For Design is one of the most highly-read sections in the most widely-read electronics publication. And because of its popularity, we have decided to expand the section.

THAT MEANS MORE IDEAS FOR DESIGN EVERY ISSUE!

We need your ideas, and you have them, so here's a chance to tell the world (literally) about the great circuit design you've had on the drawing board.

Not only is it possible to get your name and idea in print for our 165,000-plus readers, but if it gets published, you'll be in line to receive an honorarium of $100. On top of that, your idea has a chance to be voted by your peers as "Best of Issue," which receives an honorarium of $300.

IFD Guidelines:

- 1 to 1-1/2 pages of single-spaced typewritten text;
- Include schematics, charts, tables, code listings, etc.;
- Include name, company affiliation, address, phone/fax/e-mail

Send your Ideas For Design to:

IFD Editor
Electronic Design
611 Route 46 West
Hasbrouck Heights, NJ 07604
or:
Fax: 201/393-6242
e-mail: xl_research@.compuserve.com
or: rogere@csnet.net

ELECTRONIC DESIGN
TECHNOLOGY·APPLICATIONS·PRODUCTS·SOLUTIONS

Laptop T1/E1 Analyzer

- Comprehensive Test & Analysis of T1/E1 Lines with a Notebook PC
- Connect via Type-II PCMCIA slot or Enhanced Parallel Port
- Full/Fractional BERT
- Time/Spectral Displays
- Record/Playback Disk Files
- Signalling Simulation/Analysis
- Digital and Analog Drop and Insert
- PCM TIMS
- Scripted Control Test and Simulation

GL Communications, Inc.

841-F Quince Orchard Blvd.
Gaithersburg, MD 20878
Phone: 301-670-4784
Fax: 301-926-8234
E-Mail: gl-info@gl.com
Web: www.gl.com/glcomm/

GL COMMUNICATIONS CIRCLE 423

DECISION IS YOURS!

as to who gives you the best value?

QUANTITY	2	5	10
DOUBLE (ISO IN) 30	$250	$330	$415
60	290	390	450
90	330	420	500
120	360	470	540
4 LAYER (ISO IN) 30	649	790	900
60	749	850	900
90	795	995	1200
120	850	1095	1350

5 DAY TURN PRICE

QUANTITY	2	5	10
6 LAYER (ISO IN) 30	$770	$995	$1250
60	870	1150	1350
90	960	1300	1600
120	1000	1450	1800
8 LAYER (ISO IN) 30	950	1275	1595
60	1025	1495	1875
90	1290	1725	2150
120	1405	1875	2325

EXTRAS • Photoplotting • Gold • Testing

Services

- Same Day Prototype
- Instant Quotes
- SMOBC & LPI
- Scored Panels
- Electrical Testing
- Prototype to Production
- Complete CAD/DFM
- Gold/Nickel Plating
- Blind & Buried Vias
- SMT & Thru Hole Assembly
- UL Approved

Accutrace inc.

CALL US TODAY AT: 1-800-600-6611 408-748-9600
FAX: 408-748-1982 MODEM: 408-748-9605
www.accutrace.com E-mail: info@accutrace.com

ACCUTRACE INC. CIRCLE 417

1998 Direct Action Card

Reach Over 130,000 Qualified Leads With This Cost-Effective Medium.

BLACK & WHITE	1X RATE	3X RATE	6X RATE
Advertisers	$2,956	$2,833	$2,732
Non-advertisers	$3,181	$3,040	$2,906

COLOR RATES 2-Color, add $307 4-Color, add $612

ELECTRONIC DESIGN

PENTIUM® II & SOUND SBC

For Intel Pentium® II 233 ~ 333MHz CPU
Creative Sound Blaster, Ultra DMA/33 IDE
DiskOnChip® Flash Disk, E² Key™ Function
PICMG Standard Complied
Full Line CUP Cards: 286SX Pentium® Pro

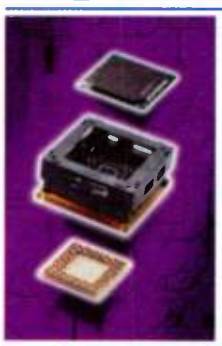
ACE-932A/T Advanced 300W IPC Power Supply

- -20°C ~ 70°C Operating Temp.
- -12V/3A Output
- Auto-Ranging 115VAC/230VAC Input (ACE-932A)
- -40V to -70VDC Input (ACE-932T
- UL/CSA/TÜV/CE approved
- MTBF > 14 years

ICP ACQUIRE INC.
650-967-7168 Fax: 650-967-5492 www.icpacquire.com.tw

ICP ACQUIRE INC. CIRCLE 405

High-Speed BGA Adapters



- Less than 2nH lead inductance for higher speed
- Prevents time-consuming board revisions
- Eliminates need to design-in additional signal access points
- Low profile for minimal clearance
- Easily Removable
- Rapid, new design capabilities
- New Lifetime Guarantee on all manufactured stock items

EMULATION TECHNOLOGY, INC.
World Leader in Adapters, Clips, and Test Accessories

1•800•ADAPTER
2344 Walsh Avenue, Bldg. F Santa Clara, CA 95051
TEL 408•982•0660 FAX 408•982•0664
www.emulation.com

EMULATION TECHNOLOGY CIRCLE 404

REPEAT IT! REPEAT IT!
REPEAT IT!

You've developed a strong image for your market and you'd like to advertise your message in the industry's strongest publication. The recent Adams Study found that *Electronic Design* has the largest average issue audience among the industry's twenty leading publications-and *Electronic Design* was found to be the leading publication for technical information among design engineers. Now's the time to project your image and reach the strongest specifying/buyer audience in the industry-165,000 strong. That's 165,000 opportunities for qualified leads. If you repeat your ad every issue (62 times), you can have 4,290,000 opportunities all qualified.

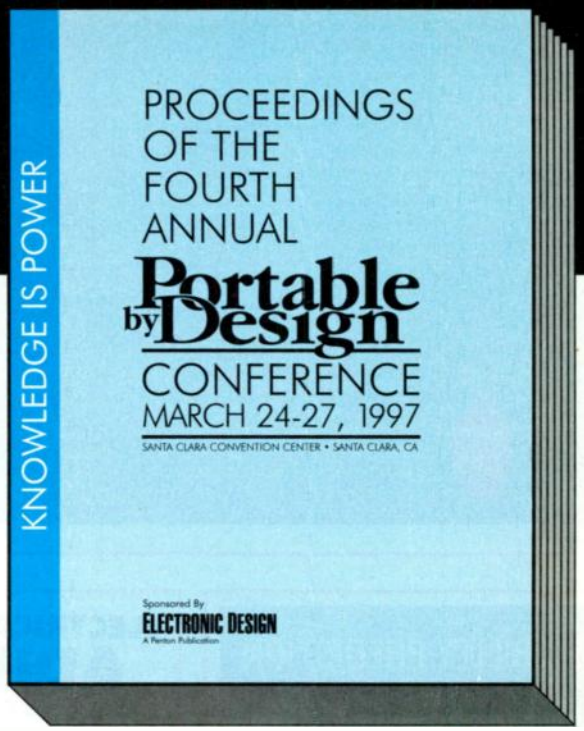
For more information, call Kimberly Stanger advertising representative at 201/393-6080 Fax: 201/393/0204

ELECTRONIC DESIGN

1998 CALENDAR

Issue Date	*Closing*
January 12	12/2/97
January 26	12/16/97
Febuary 9	12/30/97
Febuary 23	1/3/98
March 9	1/27/98
March 23	2/10/98
April 6	2/24/98
April 20	3/10/98
May 1	3/21/98
May 13	4/2/98
May 25	4/14/98
June 8	4/28/98
June 22	5/12/98
July 6	5/26/98
July 20	6/9/98
August 3	6/23/98
August 17	7/7/98
September 1	7/22/98
September 14	8/4/98
October 1	8/21/98
October 12	9/1/98
October 22	9/11/98
November 2	9/22/98
November 16	10/6/98
December 1	10/21/98
December 14	11/3/98

1997 Proceedings NOW AVAILABLE



A valuable tool for design engineers of portable, nomadic, mobile and transportable products.

The 1997 *Proceedings Of The Fourth Annual Portable By Design Conference,* sponsored by *Electronic Design,* is now available for today's portable OEM designer. The information in the proceedings will help you stay on the cutting edge of today's innovative portable technology with over 500 pages of vital, timely, and usable information—all bound in one handy reference book. This valuable tool can be yours for $175 per copy, plus $10 S&H. If you order now, you can receive the 1994, 1995, 1996 and 1997 Proceedings for $295 plus $28 S&H. Single copy issues of the 1994, 1995, 1996 Proceedings are available for $100 each, plus $10 S&H.

The following is a sample of topics from the 1997 Fourth Annual Portable By Design Conference:

- Defining and Overcoming End-User Battery Frustrations
- MCUs and CPUs for Portable Devices
- Designing With Current and Future Battery Technologies
- CPU Power Supply Voltages: How Low Can They Go?
- Software: System Management and PC Card Issues
- RF-Based Wireless LAN and WAN Technologies
- Smart Battery Management Architectures Addressing Multiple Battery Chemistries
- IR-Based Wireless Communications
- Systems, Buses, and Architectural Issues
- Thermal and Mechanical Considerations
- Low-Power Analog Circuit Design
- PC Cards and Other I/O

Portable by Design Proceedings Order Form

- ☐ 1997 Proceedings: $175 + $10 s/h; # of copies ____
- ☐ 1996 Proceedings: $100 + $10 s/h; # of copies ____
- ☐ 1995 Proceedings: $100 + $10 s/h; # of copies ____
- ☐ 1994 Proceedings: $100 + $10 s/h; # of copies ____
- ☐ 1994/95/96 & 1997 Proceedings: $295 + $28 s/h; # of copies ____

NAME _____

TITLE _____

COMPANY _____

ADDRESS _____

CITY _____ STATE ____ ZIP _____

Amount _____ + Tax*_____ = Total _____

*Sales Tax (CA, CT, FL, GA, IL, MA, MN, NJ, NY, OH, PA, WI, Canada residents add appropriate sales tax)

Make checks payable to:
PORTABLE BY DESIGN

☐ Check Enclosed
☐ MasterCard ☐ Visa ☐ American Express

ACCT. NAME _____

EXPIRATION DATE _____

ACCT. # _____

SIGNATURE _____

Please return this form to:
PORTABLE BY DESIGN • 611 Route 46 West • Hasbrouck Heights, NJ 07604 or call: 201/393-6075 • Fax: 201/393-6073

ELECTRONIC DESIGN ENGINEERING CAREERS

RATES: $190 PER COLUMN INCH, COMMISSIONABLE TO AGENCIES

MATERIALS

Ad material to: Penton Publishing, Classifieds Dept.
Attn.: Jon Eggleton, 1100 Superior Ave., Cleveland, OH 44114

SALES STAFF

Recruitment Sales Rep.: Jon Eggleton
(800) 659-1710, (216) 931-9832
FAX: (216) 696-8206

CAREER OPPORTUNITIES

BIOMEDICAL ENGINEER

Allegheny University of the Health Sciences, a member of the Allegheny Health, Education and Research Foundation is currently recruiting a Biomedical Engineer to work full-time in the Cardiovascular Research Institute, providing state-of-the-art software development and analog engineering support services for the ongoing research and instrumentation program. ***Required:*** Qualified candidates must have a BS degree in Biomedical or Computer/Electrical Engineering. For immediate consideration, submit your resume to

ALLEGHENY UNIVERSITY HOSPITALS
ALLEGHENY GENERAL HOSPITAL
Human Resources (5)
320 East North Avenue
Pittsburgh, PA 15212
Equal Opportunity Employer
Smoke-free and drug-free workplace

CAREER OPPORTUNITIES NATIONWIDE
Engineers & Tech's - Perm. Only

Cellular & Wireless Systems, RF, PCS, Microwave, Antenna, Network, Software, Sales, Dig. & Analog, Many more. Resume to: Peter Ansara, c/o ABF, PO 239, W. Spfld., MA 01090. Tel (413) 733-0791 Fax (413) 731-1486 or pa@ansara.com See our web site: http://www.ansara.com

ELECTRONIC DESIGN

Visit us on the INTERNET:
http://www.penton.com/corp/classifieds
or E-mail us at:
careerlink@penton.com

ELECTRONIC DESIGN

Chairman and CEO: Thomas L. Kemp
President and COO: Daniel J. Ramella

Group President: James D. Atherton

Vice President Ancillary Product & Sales: Drew DeSarle

Publisher: John French
Hasbrouck Heights, NJ; (201) 393-6060
National Sales Manager: Russ Gerches
Hasbrouck Heights, NJ; (201) 393-6045
Director Of Marketing: Walker Johnson
San Jose, CA (408) 441-0550, FAX: (408) 441-6052
Production Manager: Eileen Slavinsky
Hasbrouck Heights, NJ; (201) 393-6093
Marketing Research Administrator: Deborah Eng.
Hasbrouck Heights, NJ; (201) 393-6063

Advertising Sales Staff
Hasbrouck Heights: Judith L. Miller
Sales Asst.: Judy Stone Rodriguez
611 Route #46 West, Hasbrouck Heights, NJ 07604;
Phone: (201) 393-6060, Fax: (201) 393-0204
Boston & Eastern Canada: Ric Wasley
Sales Support: Karen Harrison
60 Hickory Drive, Waltham, MA 02154;
Phone: (617) 890-0891FAX: (617) 890-6131
North California/Colorado: Mark Alden (408) 441-0550
Chicago/Midwest: Lisa Zurick
Sales Assistant: Dawn Heiti
180 N. Stetson Ave., Suite 2555 Chicago, IL 60601;
(312) 861-0880 FAX: (312) 861-0874
North California/Utah/N.Mexico/Arizona:
James Theriault (408) 441-0550
Los Angeles/Orange County/San Diego: Ian Hill
Sales Asst: Patti Kelly 16255 Ventura Blvd.,
Suite 200 Encino, CA 91436;
(818) 990-9000 FAX: (818) 905-1206
San Jose:
Jeff Hoopes, Mark Alden, James Theriault
Sales Support: Liz Torres & Rachel Ross 2025 Gateway Pl.,
Suite 354 San Jose, CA 95110;
(408) 441-0550 FAX: (408) 441-6052 or (408) 441-7336
Pacific N.W. & Western Canada:
Jeff Hoopes (408) 441-0550
Texas/Southeast: Bill Yarborough
908 Town & Country Blcd. Suite 120. Houston, TX 77024;
Phone: 713-984-7625. FAX: 713-984-7576
Telemarketing Manager: Kimberly A. Stanger
Electronic Design Website Sales
Direct Connection Ads & Direct Action Cards (201) 393-6080
Direct Connection Ads & Direct Action Cards:
Judy Stone (201) 393-6062
General Manager, European Operations: John Allen
36 The Green, South Bar Banbury. Oxford OX 16 9AE, U.K.
Phone: 44 (0)-1- 295-271003 FAX: 44 (0)-1- 295-272801
Netherlands, Belgium: Peter Sanders,
S.I.P.A.S. Rechtestraat 58 1483 Be De Ryp,
Holland Phone: 011-31-299-671303 Fax: 011-31-299 671500
France: Fabio Lancellotti
Defense & Communication
10 Rue St. Jean 75017 Paris France
Phone: 33-142940244. FAX: 33-143872729
Spain/Portugal: Miguel Esteban
Pubäcidad Internacional Pza.
Descubridor Diego de Ordas,
1 Escalera, 2 Planta 2D 28003 Madrid, Spain
Phone: 91/4416266 FAX: 91/4416549
Scandinavia: Paul Barrett
I.M.P. Hartswood, Hallmark House.
25 Downham Road, Ramsden Heath,
Billir-cay, Essex, CM 11 1PV, UK.
Phone:44(0)-1-268-711560, Fax:44(0)-1-268-711567
Germany, Austria, Switzerland: Friedrich Anacker
InterMedia Partners GmbH Deutscher Ring 40
42327 Wuppertal, Germany
Phone: 49 (0) 202 271 690 Fax: 49(0) 202 271 6920
Hong Kong: Kenson Tse
IDG International Marketing Services
Suite 25F, One Capital Place,18 Luard Road,Wanchai, Hong Kong
Tel: 852-2527-9338 Fax: 852-2529-9956
Israel: Igal Elan, Elan Marketing Group
22 Daphna St., Tel Aviv, Israrl
Phone:972-3-6952967 FAX: 972-3-268020
Toll Free in Israel only: 177-022-1331
Japan: Hirokazu Morita,
Japan Advertising Communications
Three Star Building 3-10-3-Kanda Jimbocho
Chiyoda-Ku, Tokyo 101, Japan
Phone: 3 3261 4591. FAX:3 3261 6126
Korea: Young Sang Jo,
Business Communications Inc.
K.P.O. Box 1916, Midopa Building 146
Dongiu-Dong, Chongo-Ku, Seoul, Korea
Phone: 011-82-2-739-7840 FAX: 011-82-2-732-3662
Taiwan: Charles Liu, President,
Two-way Communications, Co., Ltd.
12F/1, No.99, Sec.2
Tun-Htwa South Road, Taipei, Taiwan.
Phone: 011-886-2-707-5828;FAX: 011-886-2-707-5825
United Kingdom: John Maycock
John Maycock Associates
Provincial House
Solly St. Sheffield S1 4BA
Phone: 0114-2728882. FAX: 0114-2728881

INDEX OF ADVERTISERS

Domestic*
International **

Move Mammoth Amounts of Packets Faster with Masks and MUSIC CAM

Layer 3 Switching IP CIDR at 4.5M Address/Sec

Layer 3 switching and high speed routers demand processing rates of millions of addresses per second. Applying CIDR prioritization, **MUSIC CAM** takes full advantage of IPv4 address hierarchy to move data more efficiently. 4.5M address/sec can be attained using **MUSIC CAMs**. This is faster than any standard LAN wire speed - including Gigabit Ethernet.

Now: Fast Addresses, Faster Data **MUSIC CAM** (Content Addressable Memory) accelerates address processing by minimizing list searches. Exact matches for MAC addresses or best match for IPv4 CIDR are produced in a short, constant time frame regardless of list size. With a compare speed *as fast as 50ns* and up to 7 mask registers, **MUSIC CAMs** exceed the processing rates required by high speed networks. **Today.**

Lower Cost Per Port **MUSIC CAMs** deliver the highest ratio of wire speed ports to each search engine: 48 ports of 100 Mb Ethernet or 4 ports of Gigabit Ethernet. Combine up to 8K depth, 128 bit word width, and 16 or 32 bit I/O, and you can build the exact address processor you need. Starting at $5/K word, you can achieve up to 4.5M address/sec using current **MUSIC CAMs** technology. Really.

USA	Voice 888-CAM-MUSIC
	Fax 908-979-1035
In Europe: Holland	Voice +31 45546 2177
	Fax +31 45546 3738
In Asia: Manila	Voice +6392 549 1480
	Fax +6392 549 1024

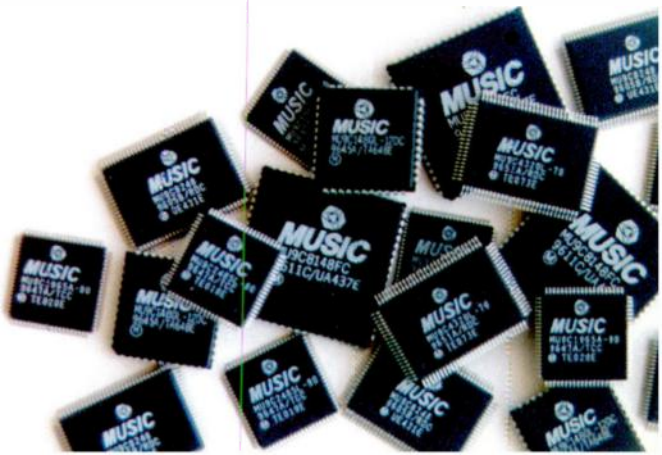
Email info@music.com
Internet http://www.music.com

Distributors in USA:

Sager Electronics	**800-SAGER800**
All American	**800-573-ASAP**

MUSIC SEMICONDUCTORS

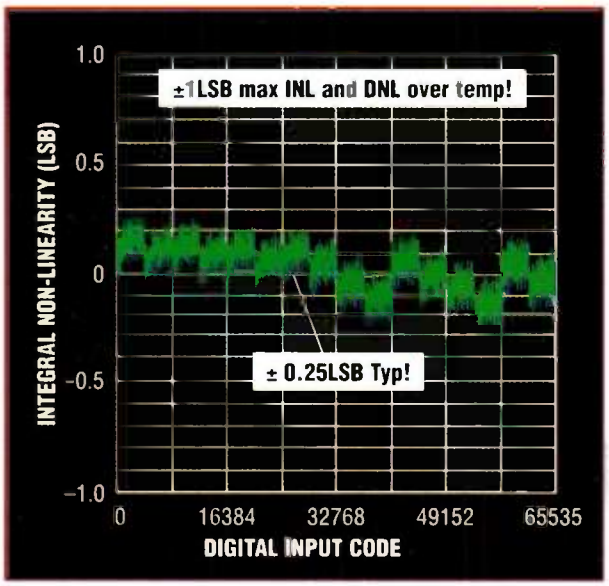
CAMs World Leader™



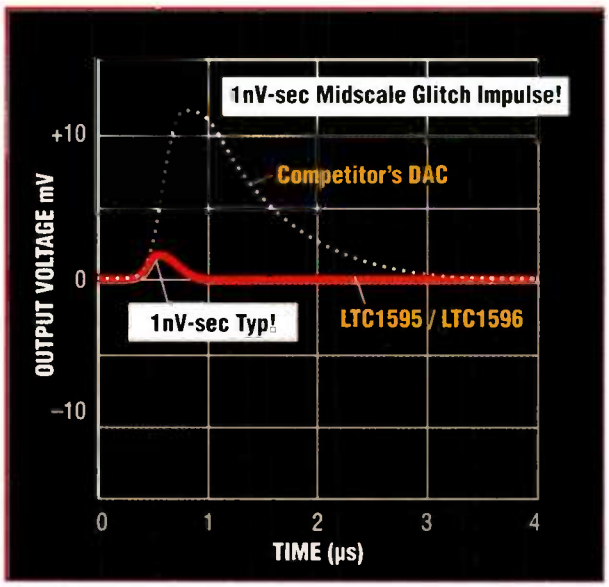
READER SERVICE 167

Real 16-Bit DAC in SO-8

± 1LSB Max Linearity



1nV-sec. Glitch



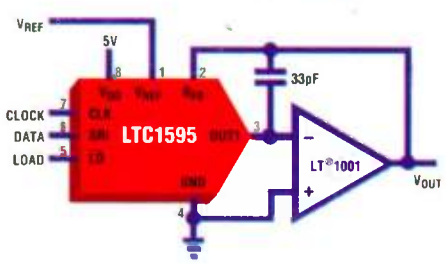
LTC1595: New Multiplying DAC Has 16-Bit Accuracy Over Industrial Temperature Range.

This new 16-bit DAC guarantees ±1LSB integral and differential non-linearity (INL/DNL) over the full -40°C to 85°C industrial temperature range. The 1nV-sec mid-scale glitch impulse is much lower than any other 16-bit industrial DAC. Available in SO-8 or SO-16 versions, the LTC1595/LTC1596 are pin-compatible upgrades for the industry standard DAC8043/8143 and AD7543. These are the best choices for real 16-bit industrial and instrumentation applications.

Features

- True 16-Bit DAC (1LSB MAX INL/DNL over Temp.)
- Low Power: 10µA MAX
- Built-In Deglitcher: 1nV-sec Glitch Impulse
- 4 Quadrant Multiplying Capability
- 3 µsec Voltage Output Setting Time (with LT1122 Op Amp)
- Plug-In Upgrade for 12-Bit DAC8043/8143 and AD7543
- Clear Pin, Daisy Chain Output (LTC1596)
- $12.25 Each in 1000-Piece Quantities

Precision 0-10V Output with One Op Amp



Free Samples

Call: 1-800-4-LINEAR
Visit: www.linear-tech.com

Free CD-ROM

Call 1-800-4-LINEAR

More Information

Lit: 1-800-4-LINEAR
Info: 408-432-1900
Fax: 408-434-0507

1630 McCarthy Blvd., Milpitas, CA 95035-7417

LINEAR TECHNOLOGY

FROM YOUR MIND TO YOUR MARKET
AND EVERYTHING IN BETWEEN

READER SERVICE 147

Data Sheet Download
www.linear-tech.com/go/LTC150