SUPPLEMENT TO

ELECTRONIC DESIGN

TECHNOLOGY▪APPLICATIONS▪PRODUCTS▪SOLUTIONS

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MARCH 9, 1998

EMBEDDED SYSTEMS IN ELECTRONIC DESIGN 1998

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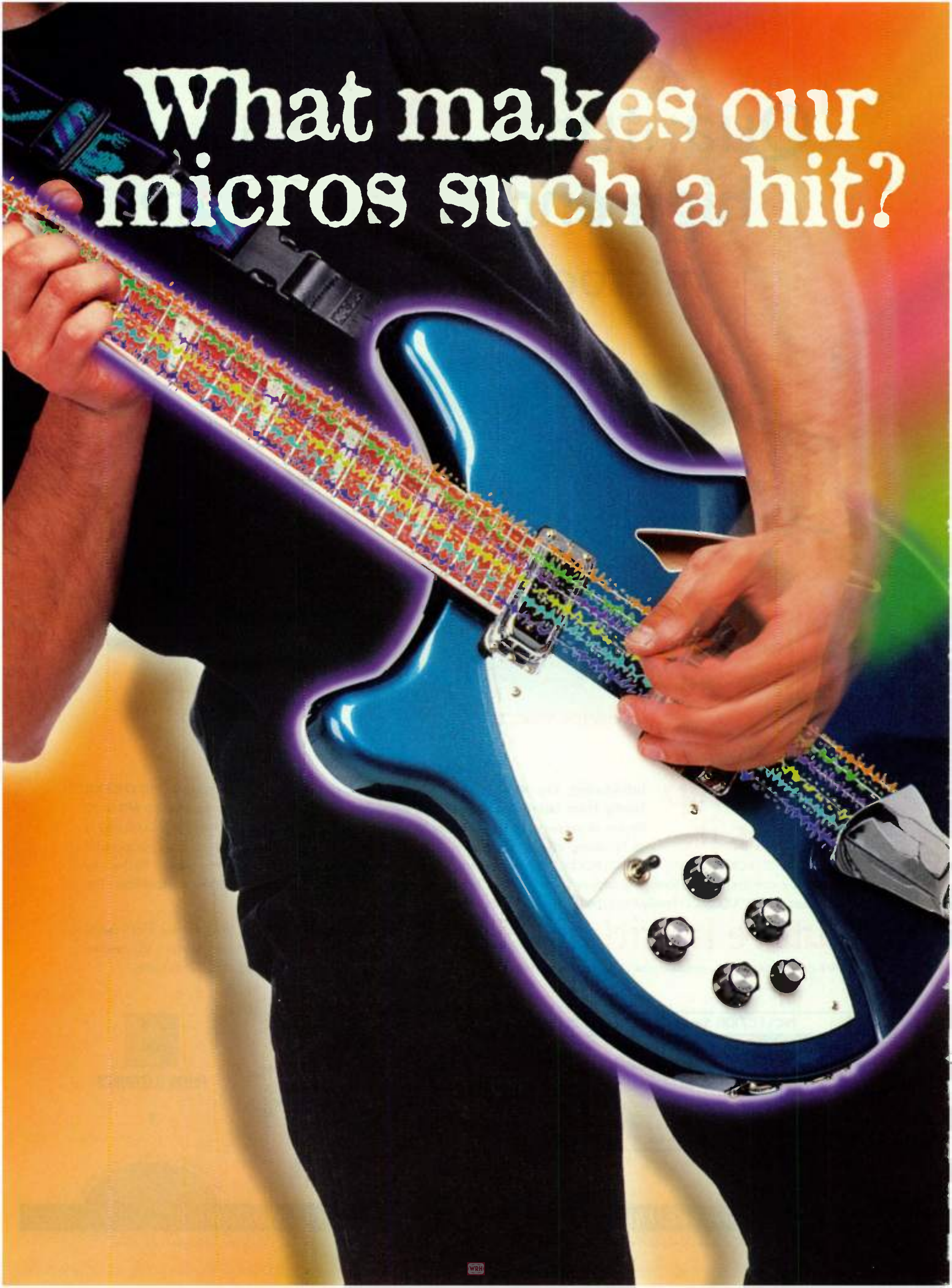
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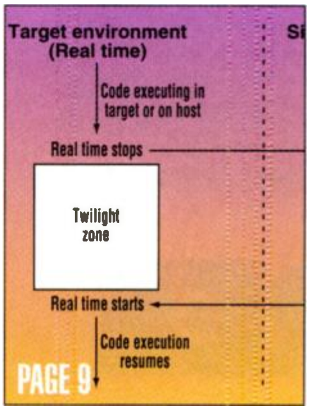
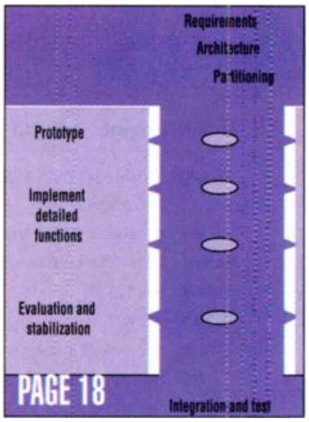
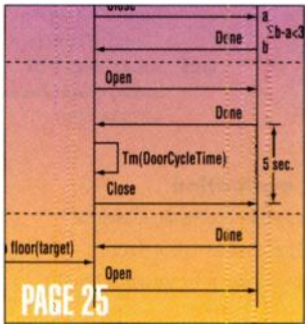
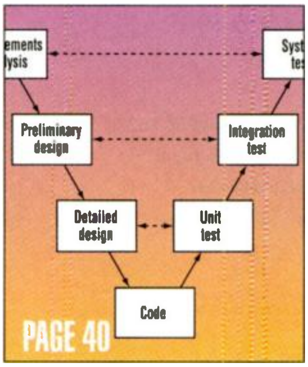
Embedded Systems Features









Departments

Editorial

Anyone who's paid any attention at all knows that embedded systems have invaded our lives in the last few years. (And I mean "invaded" in the nicest way possible.) Whether we're among the increasing number of design engineers working on either the hardware or software side of an embedded system or just users of the marvelous end products that make our professional and leisure time so much more productive and fulfilling, we've come to appreciate the wonders of embedded computers.

As an introduction to this edition of ELECTRONIC DESIGN's supplement on embedded systems, it's helpful to look at some figures that show where the industry will be heading. Worldwide, embedded merchant computer boards racked up $2.43 billion in shipments in 1996, according to a study by Venture Development Corp. (VDC) sponsored by ELECTRONIC DESIGN and VDC. That figure is expected to climb to $4.57 billion in 2001.

In terms of system sales, 46.7% of respondents said they sold fewer than five systems in 1996 and only 2.8% said they sold 5000 or more. For 2001, however, only 25.2% said they expected to sell fewer than five systems, and 12.7% expected to sell 5000 or more.

Some very interesting responses resulted from the question about the length of the development cycle for their current project. We often hear that 18 months is about the life of many products these days. That's borne out by the 62.9% of replies that said the length of their development cycle was 18 months or less. But 44.5% of those answering the question said their development cycle was 12 months or less. As for the future, 66.7% said they expect development cycles to be shorter. Somehow, 5.2% optimistically believed future development cycles would be longer.

As for the future, 66.7% of those answering the question said they expect development cycles to be shorter.

The articles we've reprinted in this ELECTRONIC DESIGN supplement should help engineers meet these increasingly tighter schedules. Two of the articles deal with co-verification, which employes techniques that make it possible to verify both hardware and software before a prototype is available. Another article deals with the unified modeling language. Finally, we've included an article on the need for software developers to invest in the proper test tools to ensure the quality of their product, and what they should expect from tool suppliers.

JOHN NOVELLINO
Managing Editor, Special Projects

New Techniques Give Hardware And Software Designers Greater Visibility Of The Internal Workings Of Increasingly Complex Embedded Systems.

ARNOLD S.BERGER
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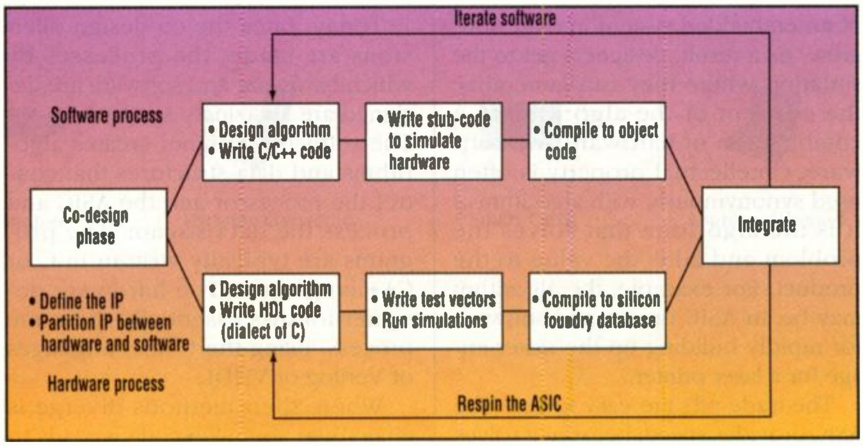
Co-Verification Handles More Complex Embedded Systems

THE TREND TOWARD MOVING INCREASING AMOUNTS OF EMBEDDED SYSTEM COMPLEXITY TO ASIC DEVICES HAS HAD A SIGNIFICANT EFFECT ON THE USE OF THE CLASSIC IN-CIRCUIT EMULAtor (ICE). The problem is reduced visibility into the system's operation as designers hide more of the system functionality from the embedded software and bus-level trace views of the system. To address the issue of internal visibility, new techniques are being developed to blend the capabilities of the traditional ICE with the functionality of an HDL simulator. By combining these tools with the appropriate interface software, a very unique and powerful design methodology is created.

Since its introduction in the late 1970's, ICE has been the tool-of-choice for embedded system debugging and hardware-software integration. Many engineers have developed a love-hate relationship with the ICE. Those "ICE boxes" were often cranky and difficult to use, but no one would argue with the high degree of functionality and visibility that an ICE brought to embedded system development. By tightly integrating microprocessor run control, memory over-



1. BEYOND THE CO-DESIGN *phase, the differences between the design processes for hardware (in this case, an ASIC design using HDL-based tools) and software are disappearing.*

the ASIC) is compared with the expected behavior of the system.

The testing of an ASIC and verifying its functionality can be extremely labor intensive. About half the total time spent developing an ASIC is actually design work, while the rest of the effort is devoted to functional verification and developing test vectors for the silicon foundry to use in manufacturing test. Even with this effort, only about half the ASICs work is correctly in-circuit the first time.

IMPROVE EFFICIENCY

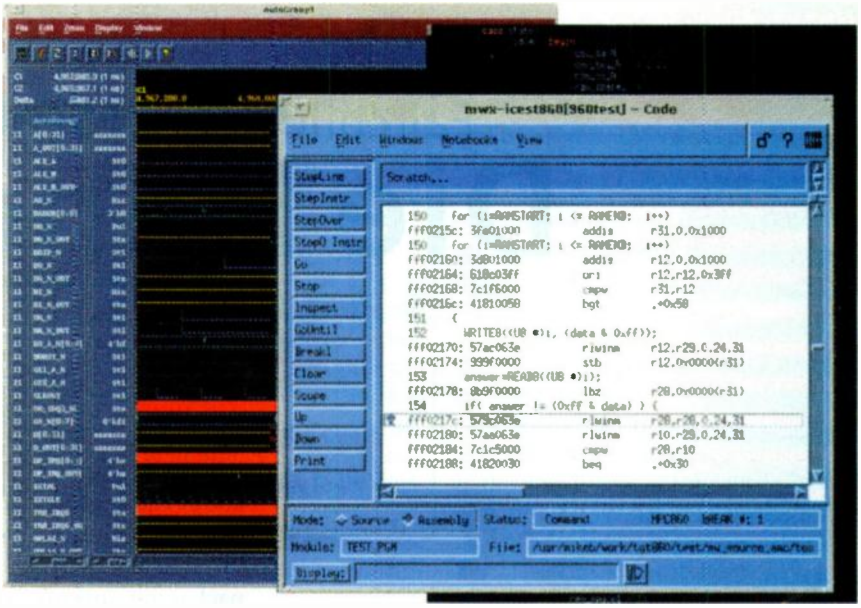
Clearly, there was a need to improve the efficiency of this process. Several companies have introduced similar tools that attempt to address this problem from different angles. The general architectural flow is to create a translation and communications software package that takes software instructions as its input and turns those variables into test vectors that are compatible with HDL simulators.

For example, Viewlogic Corp.'s EAGLEi automatically creates test vectors for a simulator from C or C++ code executing natively on the host computer. Special library functions replace the memory or I/O calls that would be used in the actual target system *(see code listings a and b)*. Remote procedure calls (RPCs) link the executing user's program on the workstation to the Eagle software, called a Virtual Product Console (VPC).

What if designers could use an ICE in a real target system with these co-verification tools? Suppose that the ICE could somehow recognize when the actual processor was attempting to access the ASIC device as if the ASIC actually existed. Could the emulator become the bridge that we've been looking for? Several advantages come to mind immediately:

- The actual code—C, C++, or assembly language—could be used without changing. This is extremely important if legacy code is involved.
- The actual processor would provide the stimuli and response, so processor behavior would be correct at all times.
- The emulator could provide a real-time trace of all actual system activity, bus level or source level, and the simulator could provide the complementary trace information for the ASIC's internal hardware design.

Designers would have absolute control of the target microprocessor. The emulator's unique claim is that it can absolutely rein in an out-of-control microprocessor. Thus, the emulator, through its ability to provide processor run control, gives designers overall system control and observability.



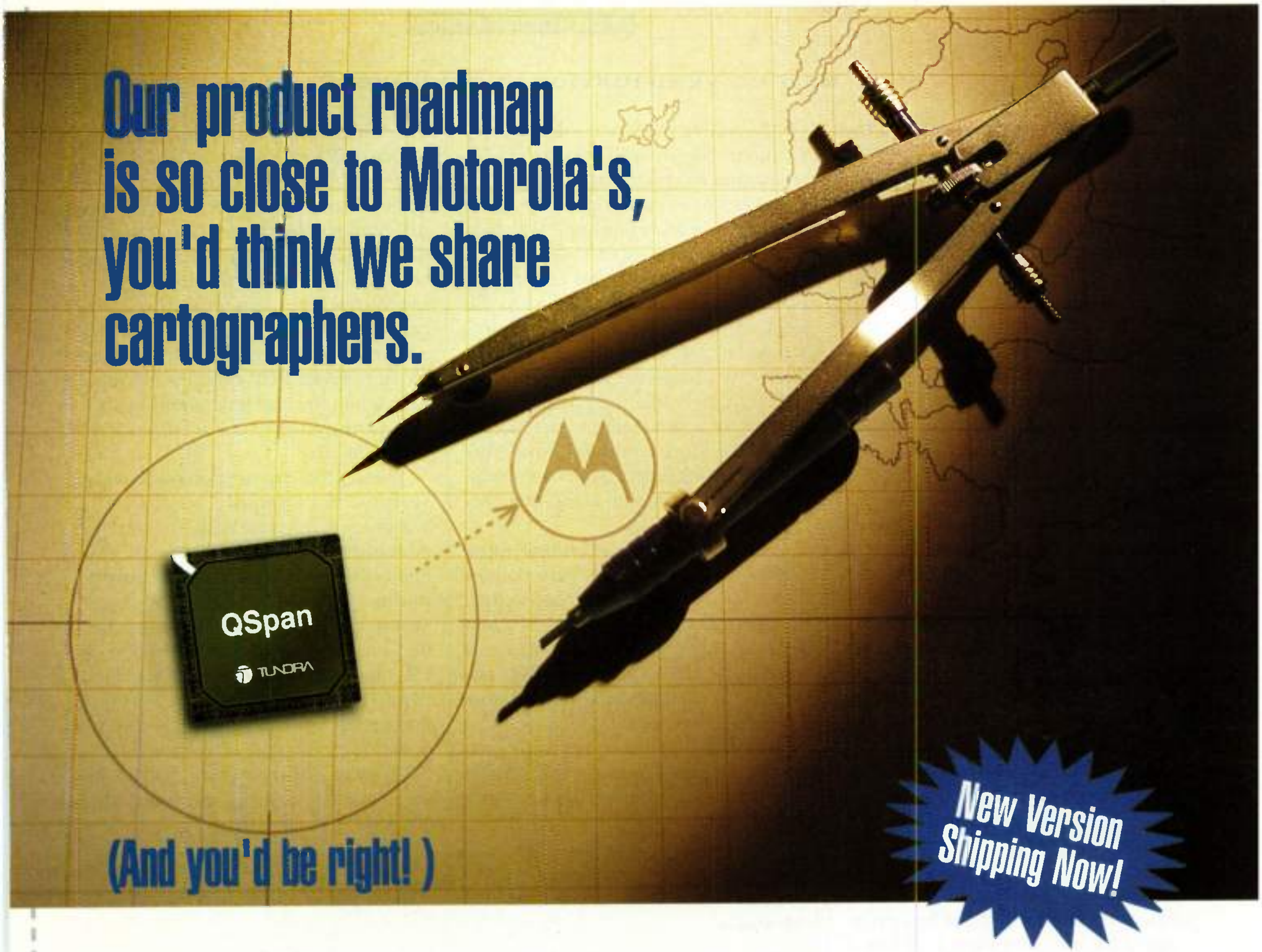
3. THESE RESULTS *from an interactive hardware and software debugging session show a waveform view from the VCS simulator (left window), the Verilog source window from the VCS simulator (right background), and the results from the MWX-ICE debugger (foreground).*

EMULATOR MODIFICATION

These compelling advantages led to an effort to modify a generic 68040 emulator for that purpose. The effort was successful as a proof-of-concept experiment, but several technical and customer-satisfaction issues required an alternative solution.

The end result was a device called the VSP-TAP (Virtual Software Processor-Target Access Probe). It works with an emulator or microprocessor, but it is a wholly separate device. It sits between the processor and the target system, much like a preprocessor module for a logic analyzer. The VSP-TAP monitors the activity on the pins of the microprocessor and detects when virtual accesses or interrupts are occurring. It then puts the processor in a wait state and sends the pin information to the simulation, which is running concurrently on the host computer. The interface software sends back an acknowledgment of the transaction. If the transaction is a write, the processor is released and code execution continues as before. If the transaction is a read operation, the VSP-TAP must continue to hold the processor in a wait state until the results of the read are available. This could be on the order of milliseconds or days, depending upon the complexity of the simulation.

Developing the virtual/real system around emulation-independent hardware allows the designer to put together different types of co-verification environments. For example, with a VSP-TAP and an emulator connected to the target, the emulator provides the run control, trace, and overlay memory, while the VSP-TAP supplies the virtual/real interface and the communications with the simulation running on the host. Another arrangement can use the VSP-TAP in a system in which the processor itself is used, with no ICE. The debugger would reside on a host computer, and a remote debug kernel would run in the target system. A ROM emulator could act as a



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LAN communications device for the debugger, but it is not necessary if a separate serial channel is available.

It is important to remember that most emulators expect that they can always regain control of the microprocessor. The assumption is that if a bus cycle hangs or aborts and the processor goes "into the weeds," the emulation circuitry can bring it back into the emulation control mode. This is significant because often when the processor is under emulation control, such as single-stepping or pausing-execution flow, it is running a real program at real speed. The program just happens to come from the emulator's control system background memory, not the target system's memory or the emulator's overlay memory.

However, many emulators will monitor certain pins of the processor, looking for state changes on these pins. If the ICE does not detect activity on these pins within a certain time period, it will attempt to assert control over the processor by generating an NMI or RESET to the processor. Unfortunately, this will ruin the program flow since the processor is not hung-up because of a defect, but is simply suspended in an extended bus cycle, waiting for the simulation to return a value.

This problem can be difficult to detect because the time-out generators are not standardized, nor are they tightly controlled. Typically, an RC circuit is used for this purpose, so one time it might time-out at 104 ms and another time at 97 ms. Also, differing amounts of LAN traffic could easily force a simulation to fail on one occasion and not on another.

This condition also is true for a debug kernel. Most debuggers use some kind of time-out mechanism to allow them to regain control of the processor. If this circuit times out due to an extended wait state, then simulation results will be erratic.

Consequently, for a co-verification and debug environment to exist, the debug tools must be aware that the microprocessor will exhibit unanticipated behavior. In this case, very long wait states on some bus cycles.

A second issue involves the number of processors used. Some emulators use two devices: A control processor manages the overall emulation circuitry, and an emulation processor (often called a bond-out) does the actual emulation. Some emulators, however, employ one processor to both emulate the target processor and control the emulation communications with the host computer. These instruments would be at a disadvantage if the user could not control the emulator for periods of time while the processor was waiting for a simulation transaction to complete. Consequently, emulators that use a single processor are unsuitable for use with simulation environments.

Another potential problem is more general and goes to the very core of the use model for real-time and virtual-time interfacing. What happens when a virtual transaction begins and real time stops, then vice versa? The answer is that real time and virtual time cannot overlap *(Fig. 2)*.

This means that the user cannot assume that real-time events will be properly serviced all of the time in a mixed real and virtual environment. The VSP-TAP, for example, is basically a passive device until a virtual access is detected. Then, it acts to extend the bus cycle of the processor until the virtual transaction occurs. Thus, any real-time target activity that is being controlled by the processor and monitored by the emulator can progress normally, and the emulator is an ideal tool for dealing with these interrupt-driven, real-time events. It is only when the real-time interrupts occur during the virtual accesses that problems arise.

These problems are potentially very serious. An example would be a watchdog timer generating a rest or an NMI after failing to be serviced. The key is that the designer must be aware of the operational mode of the target system and the emulator to insure that they are compatible with the notion of real time and virtual time not overlapping. There appears to be a need among users for a way to allow real time and virtual time to peacefully co-exist, so work is being done on creating some form of overlapping time support.

Code Listings

Listing a

```
void ramTest(unsigned int u32stAddr, unsigned int u32endAddr) {
    unsigned int u32addr, u32data, *p32data
    for (u32addr = u32stAddr; u32addr < u32endAddr; u32addr += 4)
        {
        u32data = ~u32addr;
        *(unsigned int *)u32addr = u32data;
        *p32data = *(unsigned int *)u32addr;
        if (*p32data != u32data) {
            /* error */
        }
    }
}
```

Listing b

```
void ramTest(unsigned int u32stAddr, unsigned int u32endAddr) {
    unsigned int u32addr, u32data, *p32data
    for (u32addr = u32stAddr; u32addr < u32endAddr; u32addr += 4)
        {
        u32data = ~u32addr;
#ifdef EAGLE_VSPLINK
        vspMemWrite32(u32addr, u32data);
#else
        *(unsigned int *)u32addr = u32data;
        *p32data = *(unsigned int *)u32addr;
#endif
        if (*p32data != u32data) {
            /* error */
        }
    }
}
```

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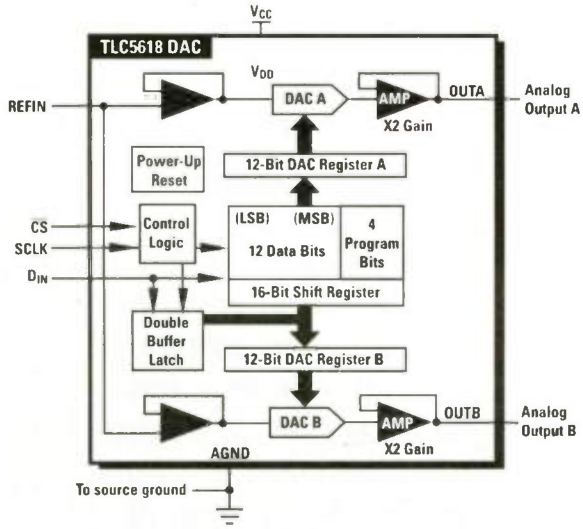

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TEXAS INSTRUMENTS

A more subtle issue involves using an emulator to interface to a virtual target system to run real code against a virtual ASIC. This situation arises when the target hardware hasn't been completed but the software team wants to move ahead by exercising their code against the virtual ASIC. They decide to use the emulator as their target execution environment by running the code in the emulator's overlay memory. This provides all of the functionality, with the exception of target system stimuli, needed to execute real code against the virtual hardware.

However, many emulators do not drive pin activity to the bus during internal memory accesses. This would prevent the VSP-TAP from detecting the virtual accesses and the system would fail. This is especially true if the overlay memory mapper circuitry was not flexible enough to deal with small regions dedicated to ASIC interfacing.

Finally, the co-verification system must be reliable and robust. Simulations often run for long periods of time. Although the processor and target may run at full speed, the simulator—VHDL or Verilog—may run very slowly, perhaps only 10 to 100 clock cycles per second. And, since simulators are expensive programs, floating licenses are valuable corporate assets. As a result, a simulation may very well be set to run over a weekend. If it does run over the weekend and the target system locks up or the emulator glitches, there must be a mechanism in place that will at least keep track of the system state up to the failure point so that a record of what happened can be reviewed by the design team.

Since emulators are generally designed to be interactive in their use model and simulators are designed to run in a batch mode, this can be the source of incompatible behavior between the software-design environment and the hardware-design environment. Thus, emulators that can run remote macro commands that upload the state of the system at periodic intervals would be very useful. This would indicate, for example, when the processor became hung-up waiting for a virtual access to return from the ASIC.

The value of the hardware-software co-verification use model, with the emulation and simulation environments functioning in parallel, can be shown. It can be shown by examining an example problem from several different perspectives.

In the example, the application code and the ASIC are being designed and tested in parallel. After an overnight build of the software, the latest revision hangs up during accesses to a certain register within the ASIC. It isn't clear from examining the VHDL code and the C code where the problem lies.

The emulator is set to run until the hang-up occurs. The real-time trace captures the fact that the processor accesses the ASIC and the virtual ASIC returns a value, but the processor goes into an endless polling loop waiting for the ASIC to provide the proper signal. The target is restarted but this time the emulator stops code execution just prior to the virtual access. Once the emulator enters pause mode, the software designer single-steps the processor into the virtual access.

The in-circuit emulator, the pre-eminent tool for hardware-software debug, can find new value as part of a hardware-software co-verification design and debug environment.

On the hardware side, the designer watches the test vector come across into the simulator and watches the ASIC simulation flow until the result vector is sent back to the interface. The vector comes back to the processor as a 32-bit data word, and the software designer sees that the bit position assigned for the status of that operation comes back as false, even though the hardware designer insisted that it was sent out as true.

The last processor the hardware designer worked with was a Motorola 68030 and this design uses an Intel i960HX. Of course, it is the ever popular little-endian, big-endian mixup. The byte order was reversed because Motorola and Intel processors use different endian methods. Both designers—hardware and software—thought that they understood the specification, yet this was missed.

How each designer approaches the problem depends on his or her perspective. Suppose that the software designer is running in a mixed real and virtual target and the simulator is running on a different workstation located somewhere else, although they are joined via a common LAN. To the software designer, the virtual accesses appear the same as the real ones. The software designer sees data coming back from the ASIC and uses the emulator exactly as it was used in the past to debug the target.

In the same situation, the hardware designer sees test vectors coming into the simulator as if they were designed as actual test vectors, rather than operational code. The hardware designer can single-step, run to a source statement, look at an internal node, and do all of the operations that were previously done with a vector file. However, this time the vector generator is the real software. In a co-verification setup, the design team can display both the hardware and software debug environment on screen at the same time *(Fig. 3)*.

Obviously, the in-circuit emulator, a pre-eminent tool for hardware-software debug, can find new value as part of a hardware-software co-verification design and debug environment. But since this technology is still in its infancy, vendors are still discovering what the issues are for designers who adopt these techniques. One such issue is real-time operating systems (RTOSs). An RTOS, by its very nature, could become problematic in such an environment. However, with some simple extensions, RTOS/emulation/simulation compatibility should be rather straightforward to achieve.

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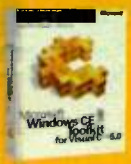

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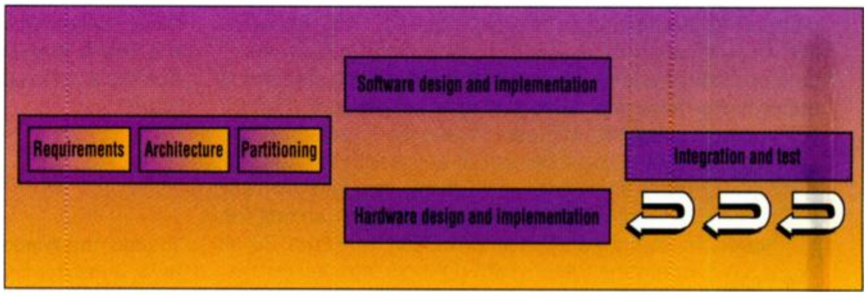
Hardware And Software Co-Verification—Key To Co-Design

IT'S NOT NEWS THAT IN THE PAST DECADE THE COMPOSITION OF EMBEDDED SYSTEMS HAS UNDERGONE DRASTIC CHANGES. EVERYONE IN THE EDA INDUSTRY IS AWARE OF LOWER CPU PRICES, advanced ASIC technology, and shorter time-to-market windows. However, the combination of these trends dramatically increased the critical need for comprehensive hardware/software co-verification. As a result, current system design methodologies are measurably strained and sometimes pushed to obsolescence, forcing designers to reexamine modern design practices.

Advances in manufacturing technology and the turning of microprocessors and microcontrollers into commodities instigated dramatic decreases in complex, 32-bit CPU prices, with embedded system designers being the principal beneficiaries. Enormous computing capacity has suddenly become available to be used in previously underpowered systems. These CPUs, seen mostly in high-end computing, routinely started showing up in printers, telephones, appliances, and autos.

The appeal of high-end processors was so strong that many design teams overlooked the inherent challenges associated with the surrounding hardware and software. Elaborate external interfaces presented by these 32-bit processors called for complex interface logic to handle communications between the CPU and ASICs. Where assembly language drivers and diagnostics were commonplace in the 8- and 16-bit CPUs, the 32-bit machines demanded more volu-

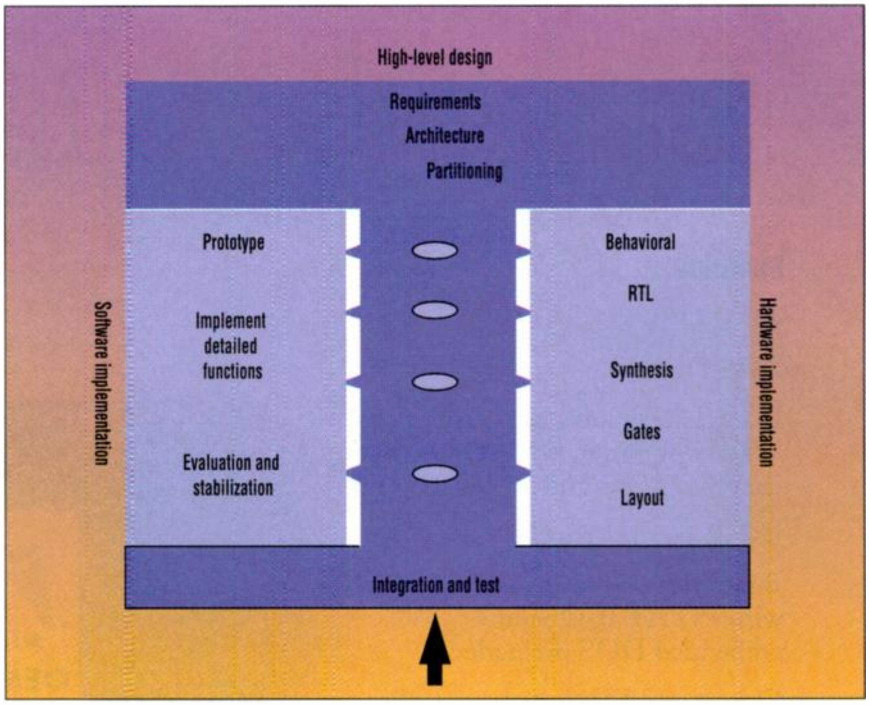


1. THIS DIAGRAM DEPICTS *the product phases of a typical embedded system development project. In addition to responding to market trends, designers are forced to reexamine this design process to perform comprehensive verification of their designs.*

minous and complex software to manage all the resources that new CPUs brought into the game.

The fact that 32-bit CPUs utilize complex hardware structures such as pipelines, caches, and pre-fetch buffers, made writing the software in assembly language impractical. The software had to be written in C or C++ to take advantage of optimizing compilers. Simple schedulers and microkernels had to be replaced with sophisticated real- time operating systems (RTOS). While the hardware surrounding the CPU had to incorporate increasingly sophisticated interface logic, the software component of embedded systems also increased in both size and complexity.

ASIC vendors started providing sizable functional blocks such as embedded cores in conjunction with the traditional ASIC library elements. The high ASIC gate capacity and preexisting cores provided the possibility of creating large scale systems-on-silicon that, in extreme cases, include a CPU core, a DSP core, and up to 500,000 gates of custom logic. Clearly, the growth in size and complexity of ASIC content in embedded systems has placed a huge validation burden on the design teams. These changes also have made some of the existing tools and practices obsolete. Very large ASICs demand high memory usage and high computational throughput in simulation. Traditional use of logic and HDL-based simulation technologies is no longer adequate as the sole verification strategy. Because maximizing the chances of first-time success is crucial, many ASIC design teams are forced to reevaluate their verification strategies *(Fig. 1)*.



2. BY MOVING SYSTEM *integration forward in the design cycle, as illustrated above, the risk of finding bugs late in the design process, when they are more difficult and more costly to fix, can be significantly decreased.*

SOLUTION DRAWBACKS

During the design and implementation phase of a hardware/software project, different organizations address the hardware and software components of the design. For the most part, the design proceeds simultaneously, but the software team is limited in what it can complete without a physical prototype of the target design. What they can do is complete the high-level design of the software and some of the algorithm development and validation. But much of the debug and integration work cannot even begin until a hardware prototype is available.

Consequently, most designs are performed in a serial fashion. The hardware is designed, validated, and prototyped. Then the software is debugged and integrated on that prototype. The problem with this approach is that once the hardware is prototyped, changes are expensive and time-consuming to implement.

In theory, Integration and Test are the final series of checks prior to the release of the system to manufacturing. In practice, it is the first time that completed hardware and independently developed software come together as a system. At this time, numerous issues surface: misinterpretations of interface definition, out-of-date specifications, poorly communicated changes, and ineffective performance modeling. In many cases, the real software and integration debugging begins only after the hardware has been built. This debug and integration can take up to half of the project schedule.

As problems are uncovered in the integration phase, developers look for the fastest and most inexpensive ways to fix those problems. Given time and cost requirements, hardware problems are often fixed by changing the software. Unfortunately, only so much can be done in software, and the functionality or performance goals of the product may be compromised with a software solution. Occasionally, there may be programmable logic elements in the circuit that can be reprogrammed to work around hardware problems, but again, this method is working around the problem, not fixing it.

To fix these problems without the time and expense of changing the hardware, they must be discovered before hardware prototypes are created. The software must be run on the hardware while it is still in simulation, that is, a virtual prototype. Before virtual prototyping can be accomplished, the designer must be able to simulate hardware at speeds sufficient to make software execution feasible. In most cases, this means that overall simulation performance must be increased by a factor of at least 1,000 times over the current execution speeds of tradi-

tional simulation products (one to ten instructions per second). Then, the debug and development environments for the hardware and software must be brought closer together.

TRUE CO-VERIFICATION AVAILABLE

A comprehensive hardware/software co-verification environment would alleviate the problems mentioned above. Higher performance can be achieved by moving some or all of the code and data space of the program into the software domain, partitioning the design. In this manner, the memory references related to reading and writing of data in the software domain are not simulated in the hardware simulator. Removing this work from the hardware simulator can greatly improve the performance of the system. The disadvantage is that the effect of those memory references cannot be seen in hardware simulation.

While the presumption that code and data references are uninteresting is correct (most of the time), there are times when all bus activity is significant from the perspective of hardware simulation. There is a commercial product, Mentor Graphics' Seamless CVE, that maintains comparable levels of performance, and provides greater accuracy by allowing the designer to dynamically repartition the memory.

When memory references and their effects are not important, the designer can map those memory references in the software domain. At a later time in the same simulation, those memory references can be remapped into the hardware domain. This technique allows the designer to make trade-offs between the level of performance and the level of detail expected in the hardware simulation.

INTEGRATION AND SIMULATION

Seamless CVE simulates the entire system by integrating software and hardware simulation with debug tools. To create a hardware/software co-verification environment, the tool synchronizes the software and hardware simulators. It also provides system-wide debug features such as setting breakpoints in both the software and hardware domains. Performance optimizations speed the co-simulation process by reducing the load of software operations on the logic simulator.

One of the more crucial issues that must be addressed in any viable hardware/software co-verification process is the logic simulator speed. The problem arises due to the fact that the typical logic simulation performance on a large (100,000 gates to 500,000 gates) design is approximately ten clocks or cycles per second (one instruction per second). Compare this performance, for example, with the 100,000 instructions/second of Seamless CVE's XRAY-Sim for software simulation and debug. You can begin to see the problem. Simply synchronizing the two simulators in a lock-step fashion would result in limited performance. A simple way to address this issue is to offer the user a number of optimization techniques.

As an example, Seamless CVE offers an instruction-fetch optimization that works by directing fetch operations to the memory-image server, thus eliminating these cycles from the logic simulator's work load. A memory read/write optimization works in a similar fashion by directing reads and writes for a specified address space to the memory-image server. The memory-image server can process these operations 10,000 times faster than a logic simulator. Early in the co-verification process, all memory operations should be directed to the logic simulator to verify the proper operation of the memory sub-system. As verification of a given address space is completed, the user can then choose whether or not to optimize that space.

As the co-verification progresses, larger amounts of memory can be optimized, further speeding software execution. In effect, the optimizations move memory from the slow-access environment of the logic simulator to the fast-access environment of XRAY-Sim and the memory-image server. The memory-image server maintains a coherent view of memory contents whether or not that address space has been optimized. This technology fully supports the use of shared memory, where the processor writes to a location that is later read by an ASIC or other hardware.

SIGNIFICANT IMPROVEMENTS

The results of these optimizations are dramatic. A co-simulation that may run at 5 instructions/second on a logic simulator will likely run at 50 instructions/second in this co-verification process, with no optimizations enabled. The result of instruction fetch and memory read/write optimizations is a 10-100X improvement in co-simulation performance. Furthermore, these optimizations maintain full synchronization between the software and hardware simulators.

Clock optimization achieves an additional 10-100X speedup by withholding clocks from the logic simulator during optimized memory operations. One application of the optimizations is to speed software-intensive operations such as initializing a real-time operating system. This time-consuming task is primarily directed at establishing the structures in memory required to support the RTOS. This co-verification process speeds through the operation in minutes while a logic simulator requires weeks to perform the same task. After the RTOS has been initialized, the user may choose to reduce the level of optimization to perform a detailed analysis of the hardware design.

SEEING SOFTWARE EXECUTION

Often the debugging power of a verifying process is just as important as its accuracy and performance. In one case, a user had tried to isolate a problem in the hardware/software interface of the design. Using a logic simulator and a hardware model for the i960h microcontroller, system software was compiled and loaded into RAM modeled by the logic simulator. The hardware model then executed the embedded application. After two-and-a-half hours of logic simulation a state machine in one of the ASICs was caught in a loop and would not exit. The hardware and software teams tried to isolate the problem for three weeks with no success.

Without seeing the software execution, there was not enough information to isolate the problem. Once this hardware/software co-verification soft-

CO-DESIGN

ware was installed at the customer's site on the Seamless CVE, it took only one hour to isolate and fix the problem. The software had initialized a register in the state machine to the wrong value. Setting a breakpoint in the state machine and noting where the software was when the break point was hit isolated this problem. By using this co-verification process, a three-week problem was reduced to a one-hour problem.

Trends such as increasing software content, design complexity, and time-to-market pressures, are driving design engineers to consider new ways of validating their systems. Clearly, it is extremely expensive to find and fix significant hardware/software integration problems late in a project. Virtual prototyping offers the promise of finding integration problems earlier in the design cycle. This technique, in turn, reduces the duration of the Integration and Test phase *(Fig. 2)*.

There are three principal reasons an organization should consider switching to a hardware/software co-verification-based design methodology. If all three attributes fit the design organization, then a co-verification strategy should be seriously considered.

The first reason is if the design group is building a 32-bit CPU into an embedded system. Software implementation for 32-bit CPU systems utilizes high-level languages, preexisting components (drivers, diagnostics, etc.), and a sophisticated RTOS—typically leading to profound increases in software size and complexity. In turn, verification complexities are introduced that usually do not exist in 8- and 16-bit systems where software is frequently a single thread of assembly language code.

The second aspect to consider is whether large amounts of original hardware are used in the system. As mentioned earlier, large-scale ASICs strain the simulation tools that are used to validate the hardware. The number of events that have to be serviced by a logic simulator can become overwhelming for 100,000 to 500,000 gate designs, forcing the validation strategy to focus only on the most common and compact testing scenarios. In other words, fairly exhaustive validation that is possible for designs smaller than 50,000 gates, is

CO-DESIGN

no longer a viable option.

The third key attribute is the intense pressure on the embedded system design teams to meet tight deadlines and hit narrow market windows. While in mature markets, such as automotive and consumer, the electronic subsystem may not be in the critical path, dynamic market participants can ill afford major schedule slips that frequently result from having to change boards or ASICs during the Integration and Test phase of the design process.

Today's system design cycle time is dominated by software and hardware/software interface issues. Through the use of virtual prototyping techniques, design teams can realize significant time savings by catching hardware/software interface bugs prior to building a physical prototype. Availability of a tool such as Seamless CVE has demonstrated that a practical architecture for implementing a virtual prototype environment is now possible. Co-verification using a virtual prototype allows these integration tasks to begin before the hardware prototype is built. Optimization algorithms allow large amounts of software to be verified in concert with the simulated hardware before a hardware prototype is built and debugged.

The key to success lies in the intelligent kernel that enables the engineer to optimize performance and accuracy while maintaining synchronization between software and logic simulation. While hardware/software co-verification is only one component of a larger overall hardware/software co-design methodology, it's a crucial component that leverages existing verification tools and techniques to provide practical value for current designs.

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General-Purpose Programming UML Provides A Common Means Of Expressing Objects, Their Behavior, And Interactions With Users.

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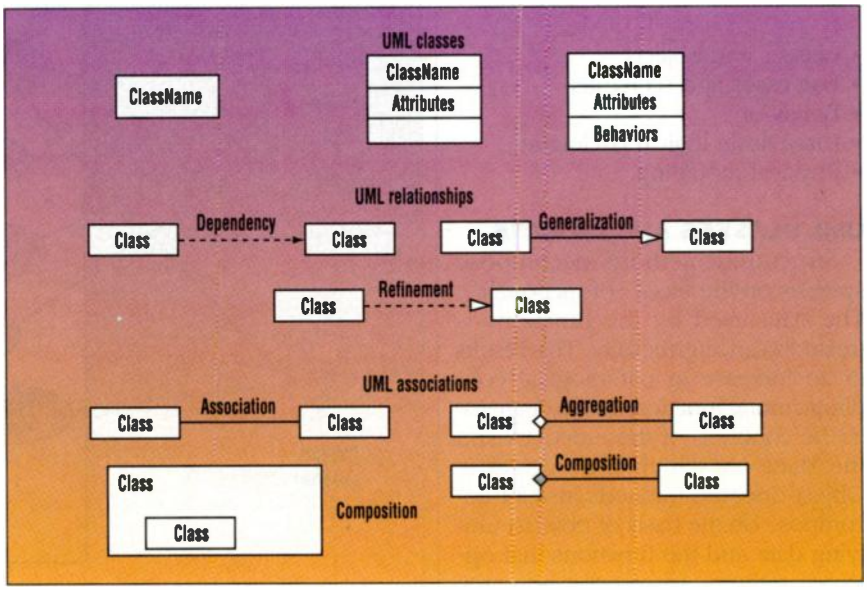
Designing Real-Time Systems With The Unified Modeling Language

A COUPLE OF DECADES AGO, IN A GALAXY FAR, FAR AWAY, THERE WAS A PITCHED BATTLE BETWEEN THE FORCES OF STRUCTURED METHODS AND THE DENIZENS OF HACKERDOM. The structured forces won, clearly and decisively, because structured methods are better. The principles of structured methods—functional decomposition, information hiding, and abstraction—allowed larger systems to be written in less time with fewer defects. More recently, there was a similar battle between the structured stalwarts and the revolutionary object-oriented (OO) guard. That battle also has been decided, again in the favor of the upstarts, and again because the newer methods are better.

Object-oriented methods provide an even better decompositional strategy with much better encapsulation and abstraction. There are case studies of



1. DEPICTED ARE UML CLASSES, *relationships, and associations. A full description of a class includes its name, attributes and behavior at run time. Relationships between classes include dependency (parent/child), generalization, and refinement. Associations show how one class uses the services of another.*

large-scale systems in which the conclusion of the developers was that the products could not have been developed using structured methods. The size and scope of the products was just too large to have ever been achieved using traditional approaches. While the majority of new desktop software is being developed using object-oriented methods, only a small percentage of embedded systems currently use objects. According to International Data Corporation (IDC), in 1995, over 55% of the OO analysis and design market was using methodologies that now comprise the Unified Modeling Language (UML).

The UML is a third-generation OO modeling language. It adapts and extends previously published works, and contains improvements and suggestions. UML is being proposed to the Object Management Group as standard notation for object-oriented development. Since UML is meant to be used universally for the modeling of systems, it applies as well to real-time systems as it does to standard desktop software applications. It provides a rich set of notations and promises to be supported by all the major CASE tool vendors (e.g., Rational's ROSE, i-Logix's Rhapsody, Cayenne's ObjecTeam, etc.).

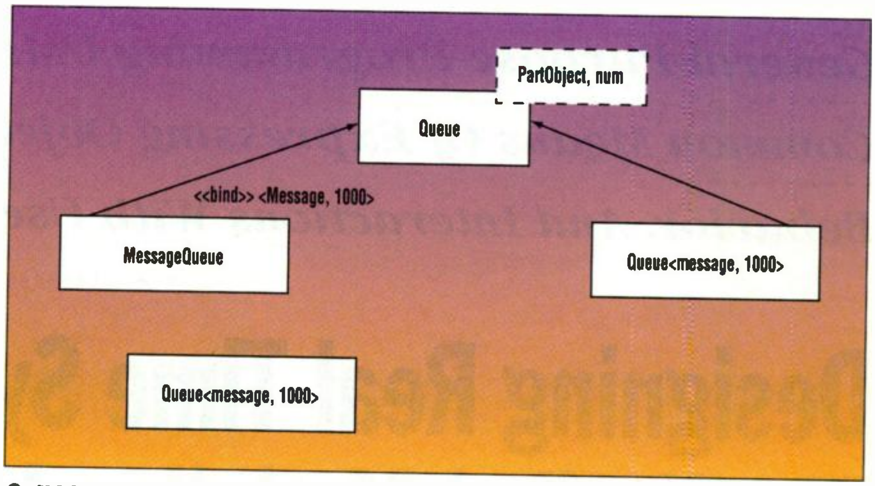
UML provides notation and semantics for a number of various models:

- Classes and objects;
- Use cases and scenarios;
- Behavior;
- Large scale logical packaging;
- Physical modeling.

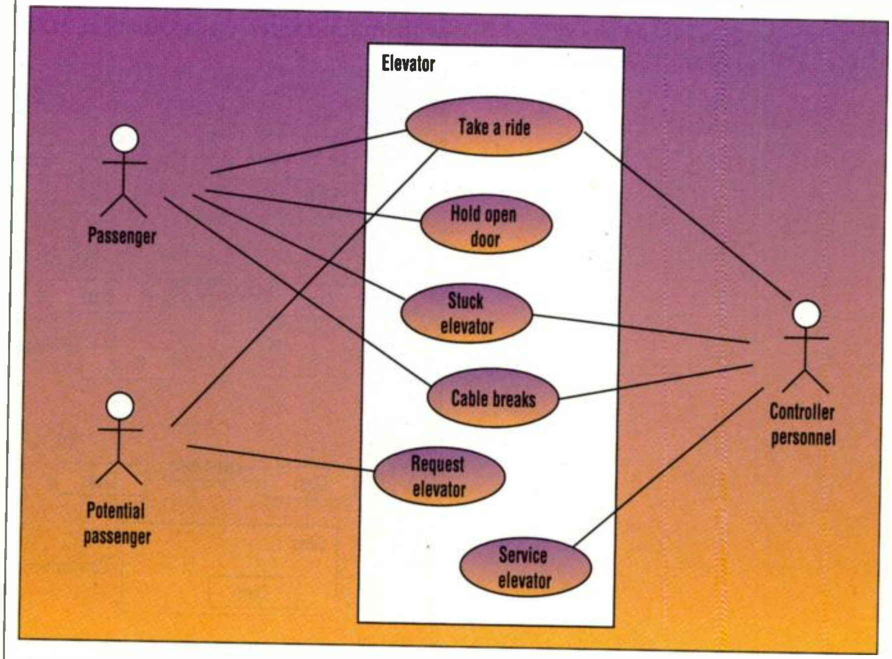
UML CLASSES AND OBJECTS

Structured methods decompose systems on the basis of functionality. The data used by the functions is treated as an afterthought. This results in an increase in pathological coupling among functions and a decrease in the cohesion of the functions and the data on which they operate. Object-oriented methods instead decompose on the basis of objects, unifying data and the functions that operate on them. An object is an entity that contains information and the functions and operations that apply to it. In the real-time world, objects can be things like a flow sensor, a robot arm joint, or an elevator *(Table 1)*.

The class of an object defines its internal data structure and set of operations. When an object of some class is created, every object has exactly the same definition. That is, every object instantiated from the same class has exactly the same data items and operations. For example, every object of the Flow Sensor class has the data items Flow and Total Volume, as well as the operations Get Flow( ), Get Volume, and Zero( ). Different flow sensors have their own instances of the Flow and Total Volume variables, so that between different objects of type Flow Sensor the values of Flow and Total volume will differ. Thus, each object instantiated from the same class is identical to all other in-



2. IN REFINEMENT, AN INCOMPLETELY *specified class is given enough information to have a unique name and parameterized values on which to operate. One technique uses the «bind» stereotype. UML provides stereotypes as a way to extend the expressiveness of UML itself and to more clearly specify the designer's intent. Stereotypes may be indicated by placing them between symbols that look like this (« »), as in «bind», or by using special icons.*



3. A USE-CASE DIAGRAM *of an elevator system shows the ways users will interact with it. Each ellipse is an actual use case—some specific interaction with the system. The stick figures represent potential roles of users. Actor icons also could represent nonhuman elements such as other systems.*

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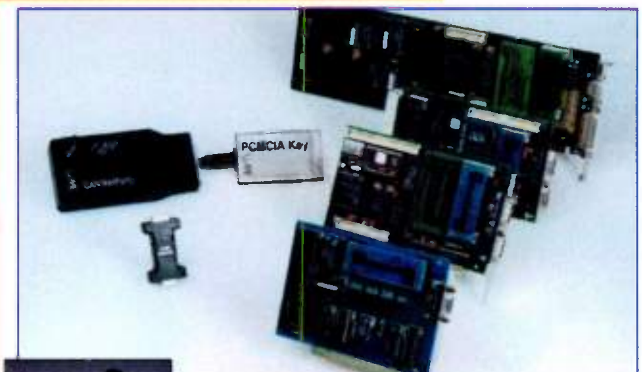

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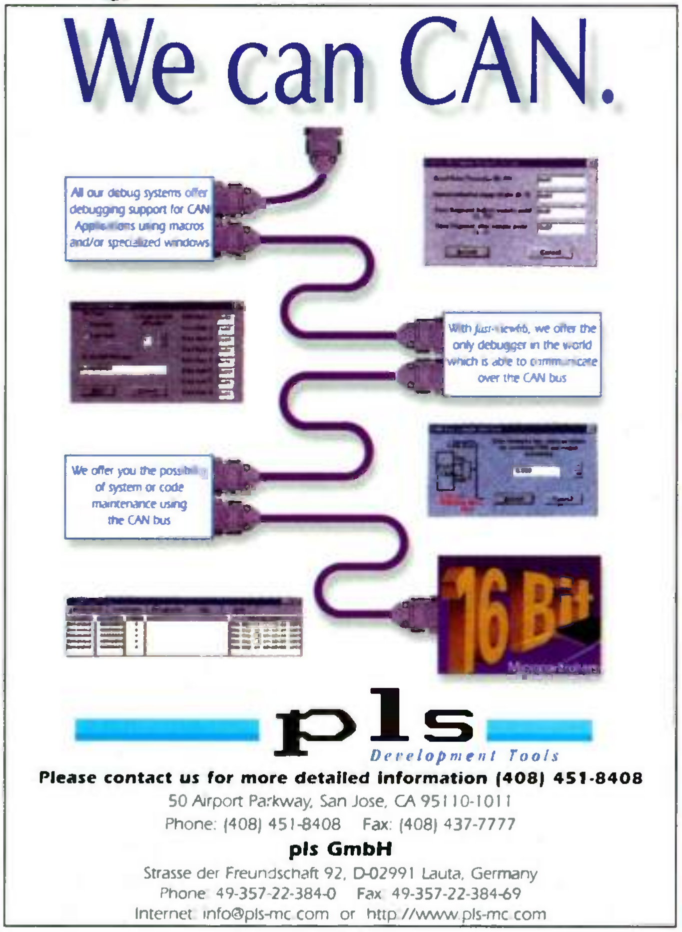

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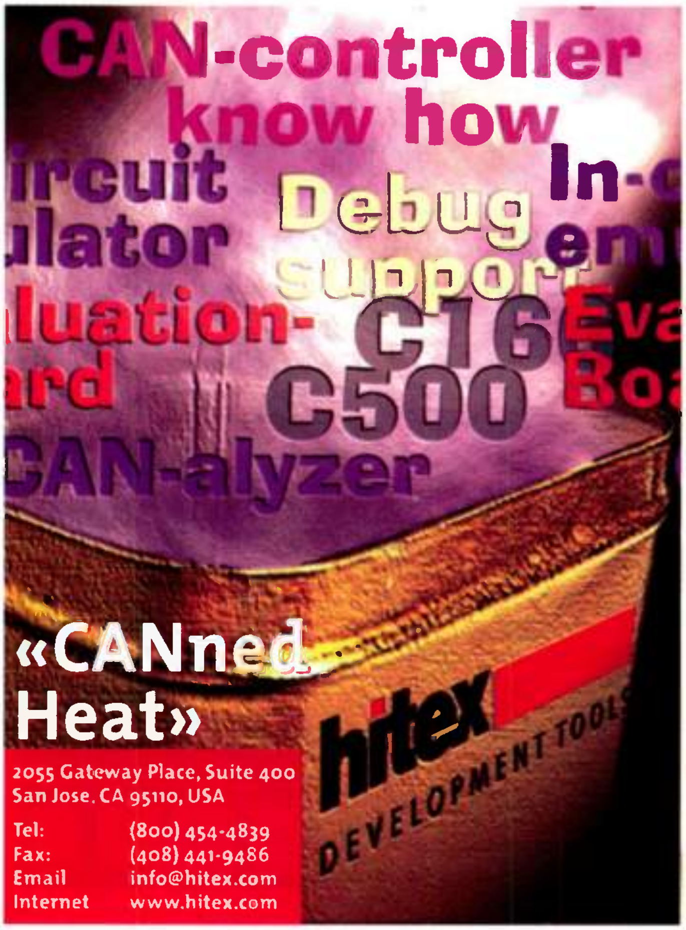

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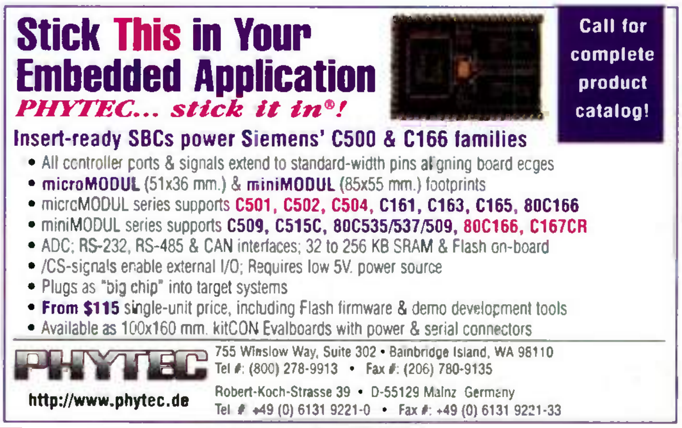

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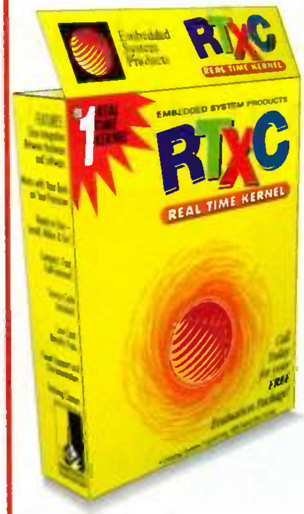

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stances in terms of structure (data and behavior), but differs in terms of current values and current behavior. Most of the time, this subtle distinction between type and class can be ignored except in languages that make the distinction visible, such as Java.

The key representation for object-oriented systems is the class diagram. Class diagrams show the important classes in the system and how they relate to each other. The notation uses rectangular boxes to visually indicate classes. From these classes, software objects will be created at run-time to perform the duties of the system. Some boxes display more information than others. The simple box contains only the name of the class. The 3-segment boxes give the name of the class in the top segment, a list of attributes in the middle segment and a list of operations in the bottom segment. The lists of attributes and operations shown need not be complete, since the complete definition of the class is held in the object repository provided by your CASE tool. The lines connecting the boxes represent some association between classes whose instances must communicate. UML distinguishes several different kinds of class relationships and associations *(Fig. 1)*.

UML RELATIONSHIPS

In UML, the term relationship is used to identify some connection between classes. One class can be a specialized version of another—this relationship is called generalization. For example, you might have a sensor class and it might be specialized into attitude sensor, direction sensor, and speed sensor. Generalization is one of the most powerful facilities of object-oriented methods because it allows programming by difference. One class is defined in terms of another and defined only by the differences. This relationship also is known as inheritance, subclassing, and parent-child relationship.

A generalization relationship means that one class inherits behavior and structure from the other; that is, one class specializes or extends the other. In UML, the more generalized class is called the base class or superclass while the more specialized class is called the derived class or subclass. A subclass inherits all the data and behavior of its superclass. It may specialize those behaviors or extend them by adding new data and operations. A Motor class might have operations Power( ) and Speed( ). A DC Motor will specialize the motor behavior by applying voltage to control the motor speed. A Stepper Motor can specialize the behavior by adjusting the step frequency. A Stepper Motor can extend its superclass by adding a Zero( ) operation.

Implementing generalization is straightforward in C++. For example,

```
class sensor {
protected:
    int value;
public:
    virtual int getValue(void);
};

class AttitudeSensor : public Sensor {
public:
        virtual int getValue(void);
};
```

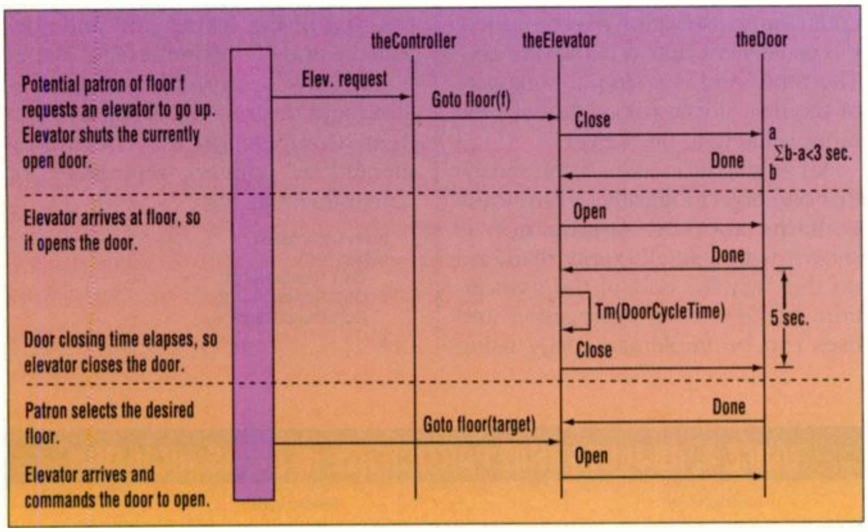
The AttitudeSensor child class can then redefine the getValue( ) operation to do something suitable for an attitude sensor. Because AttitudeSensor is a subclass of sensor, it has a value attribute and a getValue( ) function, inherited from its superclass. We define it again in the definition of AttitudeSensor so that we can change its behavior.

Implementing generalization in a structured language such as C is less obvious and requires the use of ad hoc coding rules. The simplest way is to use a struct to represent the data portion of the class and use a function pointer to implement the virtual methods, which in C++ are functions that may be overridden by subclasses. The subclass may then point to a different function. The function itself is implemented with an additional first parameter indicating the instance of the struct to which the pointer applies:

```
struct sensor {
    int value;
    int (* getValue)(sensor *this);
};

typedef sensor AttitudeSensor;
```

A refinement relationship describes a parameterized class (templates in C++ and generics in Ada) and the class that is created is the result of instantiation. Parameterized classes are an incomplete class specification, so no objects may be directly instantiated from a parameterized class. The refined class includes the definition of the undefined portions of the parameterized class. The undefined portions can be base types or numeric values. Container classes are most often implemented as parameterized classes. The container defines the containment behavior and structure, which is then refined to contain



4. IN A SEQUENCE DIAGRAM *of the elevator scenario, vertical lines represent objects and the messages passed between objects are shown using horizontal or diagonal arrows. Following the diagram left to right and down gives an exact sequence of messages and events that takes place between objects. For time-critical scenarios, timing notations can be included along the left margin.*

a specific type. A vector, for example, can define vector behavior without knowledge of the types of objects stored. The class can be refined to a vector of 1000 integers, and this class can be instantiated.

Figure 2 shows a parameterized Queue class that is in itself incompletely specified. To be complete, the type of object being queued as well as the maximum number of queued objects must be specified. Three ways to show the refinement relation appear in the figure. The first is with an explicit listing of the parameterized values on the refinement relationship itself along with the «bind» stereotype. This allows the refined class to be named, such as MessageQueue. Another means is to include the parameterized values between angled brackets that follow the name, as in Queue<message, 1000>. Lastly, the refinement relationship itself may be inferred by the presence of the parameterized values in the angled brackets, so it need not be shown. These latter two notations are useful when the refined class itself is anonymous, a common C++ idiom.

A dependency relationship means that a class depends on some service of another class, but does not have an internal reference or pointer to it. For example:

```
Class FilteredWaveform: public Waveform{
public:
      virtual int GetSample(void) {
            int x = Waveform::GetSample( );
            int pos = insert(x); // insert into internal
queue wf
            return Smooth(wf, pos); // external
function
```

In this example, the FilteredWaveform GetSample( ) operation does not have a pointer or a reference to the Smooth function, but just "knows about" it. This knowledge allows its methods to be called even without a pointer.

UML ASSOCIATIONS

A normal association implies that a client class uses some facilities of a server class. The lifetimes of the objects participating in the association are not bound together. Although an unadorned line is assumed to be a bidirectional association, by far the most common arrangement is that the client knows about the server, but not vice versa. A sensor object might act as a server to a number of clients. The sensor has no idea which objects may ask for the information, but the client objects know how to invoke the facilities of the sensor. To indicate unidirectional navigation, an open arrow may be added at the server end of the association.

Associations may be named, as in "contains" or "controls." Because the association is always named from one object's perspective, a standalone arrowhead indicates the perspective. The roles of the objects may be named by putting role labels next to the classes where the association connects. Although role names for both ends of any association may be added, it is usually enough to name one end. The other end is a simple conjugate of the first. If one role is "client," the other is likely to be "server."

An aggregation association means that one object logically or physically contains another. Aggregation is shown with a small empty diamond on the "whole" end of the association. In C++, both aggregation and uses can be implemented by using either a pointer or a reference to the server or part object, as in:

```
Class Sensor {
private:
      Converter* ADC_Channel1;
      Converter& ADC_Channel2;
protected:
      int CalConst;
      int Value;
public:
      sensor(converter*C1,C2);
      virtual int get(void);
      int Calibrate(int cal);
};
```

UML allows sharing of an aggregated object by more than one owner object.

Composition is a stronger form of aggregation. It implies that there is exactly one owner object and the life of the aggregate object begins after the creation of the owner and ends before the end of the owner. The owner is explicitly responsible for the creation and destruction of the component. Composition may be implemented by pointers, references, or containment as in:

```
class Composite {
public:
   Obj1 *component1;
   Obj2 &component2;
   Obj3 component3;
};
```

TABLE 1. OBJECTS IN A UNIFIED MODELING LANGUAGE

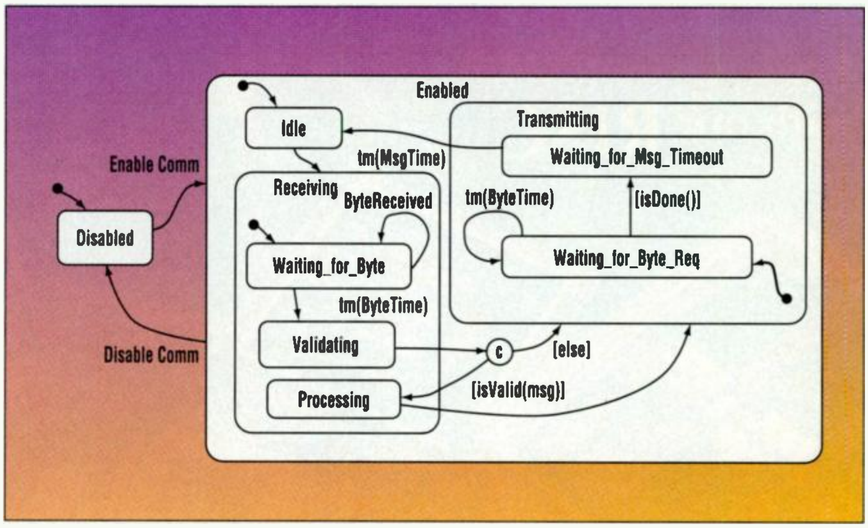
Object	Data	Operations
Flow Sensor	Flow	Get Flow( )
	Total volume	Get Volume( )
		Zero( )
Robot arm joint	Position	Step Foward( )
		Step Backward( )
		Get Position( )
Elevator	Floor location	Get Position( )
	Direction	Get Direction( )
		Add Destination( )
		Emergency Stop( )
		Alarm( )

TABLE 2. OBJECTS THAT PARTICIPATE IN AN ASSOCIATION

Multiplicity	Description
1	Exactly one object participates
*	0 or more objects participate in the role
x..y	A range of objects participate in the role, e.g., 3..6
x,y,z	A list of possible numbers of participants, e.g., 1,3,5,6,9

The number of objects that participate in an association are known as that association's multiplicity. Often one instance of a class sends messages to one instance of another. This is a "1 to 1" association. Equally often, one instance of a class sends messages to more than one instance of another. This is called a "many to 1" relationship. UML multiplicities are shown at each end of the class association *(Table 2)*.

Objects communicate by sending messages to one another. The presence of an association necessarily implies that the objects communicate in this way. The concept of messaging is an abstraction of object communication. Object messaging may be implemented in terms of function calls (most common), a real-time operating-system (RTOS) message and event posting, or bus messaging. Abstracting object communication allows you to ignore the implementation details of object communication until design. In design, these messages will result in acceptor operations being defined in the receiving object(s) in the simplest case. Or they will be interfaces to an RTOS or communication protocol stack when the objects are in different threads or processors.



5. IN THIS NESTED STATE *chart, the substates "idle," receiving," and "transmitting" are nested within the state "enabled." This nesting can go down to any level. The © is a conditional connector allowing the conditional expressions to control the transition.*

USE CASES AND SCENARIOS

Use cases are broad-stroke descriptions of how a system will be used *(Fig. 3)*. They provide a natural high-level view of the intended functionality of the system that is understandable regardless of the technology used to implement it. This makes use cases invaluable for talking with customers and marketing executives who must specify the system to be implemented.

The large rectangle shows the boundaries of the system under development. The objects (shown using the UML-defined actor stereotype icon) arranged around the system are external objects that interface with the system. The ellipses inside the system rectangle indicate the use cases themselves.

Use cases are isomorphic with function points. This means that use cases per se are not object-oriented. They are, in fact, a functional view of the system. Generally, this means that use cases cannot be uniquely elaborated to an object view. Nevertheless, the use case diagram is a useful view for capturing and communicating high-level requirements.

A use case is a general pattern or strategy of system use. Consider the use case "Take a ride" from the elevator use case diagram *(Fig. 3 again)*. There are many instances of this use case, such as when the elevator is at the floor when called, below the floor but going the right direction, or above the floor going the wrong direction. A use case always represents many different specific threads of interaction. These specific threads are called scenarios. Every scenario is a specific instance of a use case.

An example of a scenario from the "Take a ride" use case would be:

1. Elevator is Idle and above; the target destination is above.
2. Elevator is Idle and on the current floor; target destination is above.
3. Elevator is going up and is above the summoning floor; target is above the summoning floor.
4. Elevator is going up and is below the summoning floor; target is above the summoning floor.5. Etc.

This is a particular path through the system functionality, but dozens of distinctly different scenarios are possible. UML provides two notations for modeling scenarios: The sequence diagram and the collaboration diagram.

Sequence diagrams use vertical lines to represent objects. Messages passed between objects are shown using horizontal or diagonal arrows as in the "Take a ride" scenario *(Fig. 4)*. Time flows from the top of the page down. Unless specifically annotated, only the sequence of messages is shown, not exact time.

The textual annotations along the left edge of the diagram help explain the diagram. For real-time designs, exact timing must often be specified. UML allows textual annotations to be added to sequence diagrams when timing is important. There are two different notations used to specify timing. The first uses short horizontal lines with a time indication between them. The second labels the messages "a" and "b" and specifies a timing expression between curly braces. The timing specification is a constraint and UML notation places all constraints within curly braces.

Other extensions are used as well. Some are specified in the UML Notation Guide and others are provided as elaborations. For example, Rhapsody, the object-oriented CASE tool available from i-Logix, lets you specify the current state on the sequence diagram as well, providing an obvious visible linkage between the scenario models and the state dia-

grams. The other notation for modeling scenarios is the collaboration diagram. This diagram specifies the order of messages, and allows timing annotations as well. Sequence is more prominent in the sequence diagram but structure is more obvious in the collaboration diagram. Arrows attached to the messages indicate the direction the message is sent. The numbers on the messages indicate the order in which they are sent.

Real-time systems care a great deal how messages are handled between concurrent processes. UML provides icons that can be added to any message to indicate its concurrent behavior. The symbols are taken from Booch's earlier work.

These symbols can be added to the message to indicate how the concurrent processes are synchronized during the message:

- Simple—Simple synchronization merely denotes that the synchronization has not yet been specified.
- Balking—A balking rendezvous means that if the receiving task is not ready, the sending task aborts the message and continues.
- Asynchronous—An asynchronous rendezvous means the sender sends the message and continues without waiting for the receiver to get the message.
- Time-out—A time-out rendezvous indicates that the sender will wait for the receiver to be ready for the message up to some fixed time before aborting the message transmission process.
- Synchronous—A synchronous rendezvous means that the sender waits until the receiver is done processing the message before continuing. This is commonly implemented as a standard function call.

BEHAVIOR

UML behavioral models are based on finite state machines using the Harel statechart notation and semantics. Harel statecharts can more clearly depict complex behavior than the more common Mealy-Moore state models because they support:

- Nesting of states;
- Concurrency;
- Guards on transitions;
- Propagated events;
- Actions on transitions;
- Actions on state entry;
- Actions on state exit;
- Activities occurring as long as a state is active.

The single most important conceptual tool developed over the last 4000 years is the idea of decomposing difficult large problems into simpler smaller ones. Because Mealy-Moore state models don't provide either hierarchical or orthogonal decomposition, they don't "scale up" gracefully to large problems. As state machines get more complex, it becomes more and more difficult to represent them using flat models. Support for orthogonal components is necessary to provide the ability to model concurrency.

Consider a simple class that has three attributes:

- tColor color (eRed, eBlue, eGreen)
- Boolean ErrorStatus (TRUE, FALSE)
- tMode tMode (eNormal, eStartup, eDemo)

What is the "state" of an instance of this class? It is composed of the various possible values of each variable. There are 18 possible states. This example illustrates a well-known problem with Mealy-Moore state models—state explosion. To describe orthogonal components using a flat model, each combinatorial set of the component states forms a new state.

The other means of decomposition is the nesting of states. Just as objects or functions can be composed into smaller and smaller pieces, states can be nested within other states. The semantics of orthogonal components dictate that when the object is in a state with orthogonal components, it must be in exactly one state for each currently active orthogonal component. The inclusion of orthogonal components makes UML state diagrams expressive in terms of concurrency, while the nesting makes them much more readable.

In the example of a communication controller, the states Disabled and Enabled are at the same level of abstraction *(Fig. 5)*. However, Enabled is decomposed into three primary substates: Idle, Receiving, and Transmitting. These latter two states also are "rich" and are further decomposed. While in the Receiving state, the communication controller can be Waiting for Byte. In this state, it is receiving a byte stream. If a time-out occurs before the next byte arrives, the controller assumes that the stream is done and then it transitions to the Validating state.

Within the "receiving" state, once "validating" is done, and if the received command is valid, it enters the Processing state during which it acts on the received message. When processing is done, the controller goes to the Transmitting state to send an ACK response. If the command is not valid, then it transitions to the Transmitting state immediately so that it can return a NAK. Nesting states in this way allows states to be decomposed, allowing the developer to break down large complex state machines into hierarchical structures.

Transitions are more elaborate in UML than even in the Harel notation. The UML syntax for transitions is:

name(argument list)[guard] ^ event list / action list(argument)

Let's examine each of field in turn.

- The name is the name of the transition. Often, this is the only thing specified for the transition.
- It has an optional argument list to indicate when data is present in the transition. This argument list is enclosed within parenthesis like a standard function call.
- The guard is shown in square brackets. A guard is a condition that must be met for the transition to be taken.
- The event list is a command-separated list of events that will be propagated as a result of this transition. This is largely how concurrent state machines communicate.
- Lastly, the action list specifies a comma-separated list of functions that will be called as a result of the action being taken. Each may have an argument list as well.

The syntax for transitions is rich and

DESIGNING WITH THE UML

allows the triggering events to carry data, propagate other transitions, and initiate actions. For example, all of the following are valid state transitions:

- JustDoIt
- JustDoIt(x)
- JustDoIt(x: int)
- JustDoit(x) [x>0]
- JustDoIt [y<10] / print(y)
- JustDoIt(x,y)[x>y+10] ^Nike.MakeMoney(MuchoDinero)/print(y)

UML provides a number of advanced notations and semantics where they are required. They don't have to be used, but like parachutes, they are nice to have when you really need them.

A stereotype is the metaclassification of an element of the UML. It identifies the type of the element within the UML metamodel. For example, predefined UML class stereotypes include Signal, Exception, Interface, Metaclass, and Utility. Predefined task stereotypes include Process and Thread.

The primary advantages of stereotypes are: They make it possible to refer to the type of the element, as in "That class is an Exception class;" and they allow UML to be extensible by the user of the method by definition of additional stereotypes. Stereotypes are indicated with the element name and are enclosed by symbols that look like this (« ») or by special icons.

Real-time systems are often delivered on custom platforms, and the engineer must develop not only the software, but the hardware components as well. The hardware devices must be bound together with the portions of software they will run. UML provides deployment diagrams to show the organization of the hardware and the binding of the software to the physical devices. Deployment diagrams show various hardware devices (called nodes) and their physical interfaces. The type of the hardware device is given by its stereotype, such as Processor, Device, Display Memory, or Disk.

For large-scale development, UML supports the concept of packages. A package is a grouping of inherently cohesive entities. The class model can be packaged by area of concern, such as User Interface, Device I/O, and so on. UML uses a tabbed folder to represent a class package. Packages can contain things other than classes. Implemented code can be packaged into subsystems that represent deployed software components. Stereotypes are used to clarify the type of package («category» for the class model or «subsystem» for the code model).

UML is a third-generation, feature-rich object-oriented modeling language that is particularly appropriate for real-time systems. It provides support for the classes and object, and many kinds of associations among them, such as aggregation, uses, dependency, inheritance, and instantiation. Use cases are directly provided along with scenario modeling for detailed description of required system behavior. Enhanced finite state-machine modeling supports a number of real-time features including concurrency, event propagation, and nested states. The method itself is extensible though the definition of additional stereotypes.

UML is a powerful modeling language and has more notation and semantics than presented in this brief introduction. Interested readers are referred to forthcoming books on UML for more information. Notational guides and other information can be obtained from Rational Software's web site (www.rational.com) or the i-Logix web site (www.ilogix.com).

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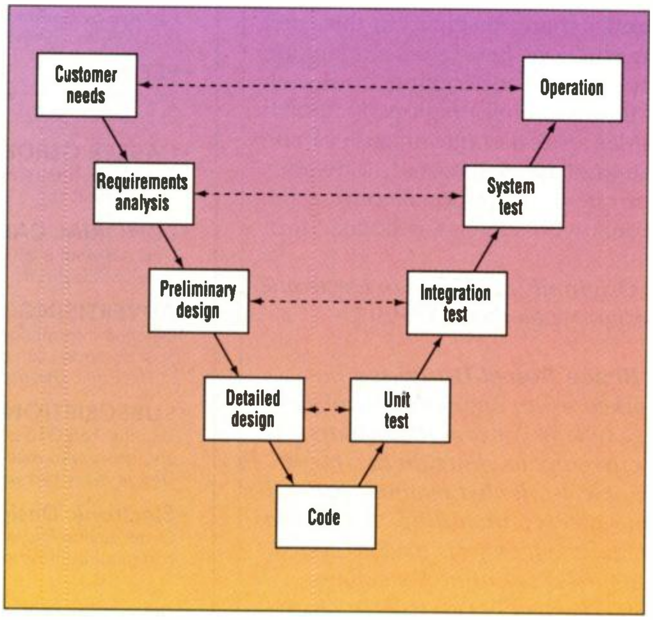
Embedded Systems Software Developers Must Invest In Quality With Rigorous Testing While Demanding Reliable Tools From Their Vendors.

TOM BARRETT
EMBEDDED SYSTEM PRODUCTS INC.

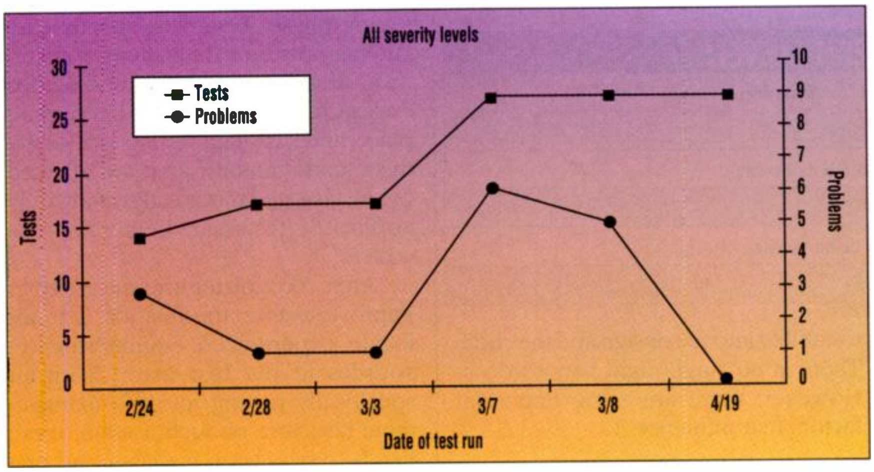
Dancing With Devils: Or Facing The Music On Software Quality

TALK TO ALMOST ANYONE MAKING END-USER EMBEDDED SYSTEM PRODUCTS OR TOOLS TO MAKE THOSE PRODUCTS AND YOU GET THE DEFINITE IMPRESSION THAT SOMETHING IS AMISS. The product developer tells horror stories about the lack of experienced talent, slipping schedules, missed market windows, exorbitant labor costs, and tool chain failures. The tool manufacturer tells similar tales and adds his or her own concerns about low sales margins and high engineering and customer support costs. No one is pointing any fingers yet, but it is obvious that the symbiotic relationship between tool manufacturers and product developers is reaching a crisis stage.



1. A CONTROLLABLE TESTABILITY *process tracks the product development cycle, also known as the V-cycle model for its shape. Unit tests test individual code modules at the detailed design level. At the top and toward the end of the development cycle, operation testing determines if the product actually fulfills the customer's needs.*

Consider the product developer's situation. To stay in business, the developer has to fulfill the market's almost insatiable demand for new products. Software has displaced hardware as the main cost area and product development teams are increasing in size. Industry estimates suggest the ratio of software to hardware engineers on projects is now about 7 or 8 to 1. Developers need reliable tool chains and components that work because their product development cycles are measured in months. Product life cycles grow constantly shorter and new products come about through incremental improvements to existing products. The "clean sheet" design approach is rare. The developer sees software for his PC being sold cheaply, and expects the embedded system development tools to be similarly priced. On top of those pressures, the demand for engineering resources is so great that scarcity is now the rule. Six-figure salaries and a



2. CHANGES IN THE *test suite or the code under development can lead to the discovery of an increased number of problems. This can be a good thing. As the number of problems diminish under a stable code and test suite base, confidence in the reliability of the software increases.*

platter of perks are commonplace for even mildly competent software engineers.

Now, take a look at the tool manufacturer's situation. To stay in business, he has to meet a similar set of insatiable demands from product developers for capable and efficient development tools. Semiconductor manufacturers produce new processors almost weekly, thereby compounding the demand from product developers who want to use the latest and greatest silicon. And like the product developer, the development cycle is measured in months, with tool lives correspondingly short. Similarly, new tools come about through incremental improvements to existing tools. With engineering resources coming from the same talent pool as those for product developers, scarcity is compounded, driving cost higher.

Notice anything similar? There is little difference between the two. Each is, at once, both a tool user and a product developer. They experience the same problems; if one fails, the other feels the blow. They dance to the music of the market, too often whispering promises without fulfillment, sizzle without steak. Yet, in spite of their mutual dependency, they seldom talk of their mutual expectations.

On the surface, those expectations are quite simple. The tool user expects the tool manufacturer to provide more powerful tools to aid in the development of more complex products. And, he expects the tools to work. Similarly, the developer's customers expect powerful applications and they expect the embedded systems they buy to work. The developer and the tool manufacturer both expect the user to buy the tool or the product at a price fair enough to get an acceptable return on investment.

But there are problems in this relationship. A lot of tools just don't work; their performance doesn't match their hype or their support is inadequate. These tools endanger the user's product development, making them understandably reluctant to pay much. By receiving a low price, the tool manufacturer lacks the means to improve the product. Tool manufacturers can't afford to build fancier and more powerful tools when costs continue to increase and users want to pay less and less. Such is the essence of a standoff. They have unwittingly become each other's devil, and somehow, the dance must end.

For the dance to end, there must be a change in this admittedly gloomy scenario. One possible change would be of a fundamental nature, for it would end the tool-manufacturers' role as the tool-users' devil. If tool manufacturers adopt a user-oriented position focusing on better, more reliable tools, the dance will end. Through that action, the tool users will become partners in the efforts. However, one should not expect a major change in the relationship as long as the basic nature and expectations of the tool manufacturer and the tool user remain unchanged.

The tool user expects the tool manufactuer to provide more powerful tools to aid in the development of more complex products.

Software manufacturers at all levels can meet the challenge by making significant improvements in their products. The vehicle for those improvements is the product-testing process. By thoroughly testing their products to ensure they work correctly and reliably, both developers and tool manufacturers can provide the needed assurances. Simply stated, better testing can make better tools, and better tools along with testing make better products. Unfortunately, performing better testing is more easily said than done. It can be a tedious and expensive process, but everyone will have to do it if the dance is to ever end.

USING THE PRODUCT LIFE CYCLE

Testing can follow many paths. Consequently, there probably is no single "right" way to do it. One thing, however, is certain: Testing has to be done somewhere during the product's life cycle. Understanding what happens during a particular phase of life provides insight into how to test the product at that stage, as well as the cost of finding and correcting problems. The typical life-cycle model (and there are many variations) usually includes four main phases: Specification, Development, Testing, and Operation *(Fig. 1)*.

These four phases and their constituent activities form the V cycle model of product life. On the left side of the V, activities are shown as top-down processes moving from the abstract at the top to specific at the bottom. Time is the horizontal axis and represents the phases of the life cycle. Product requirements and specifications are produced during the specifi-

PROBLEM SEVERITY LEVELS

Severity index	Meaning
1	Suggestion/enhancement request
2	Reasonable alternatives exist. Fix if possible
3	Workaround is cumbersome
4	No workaround possible. Fix before release
5	Must fix NOW

cation phase. The development phase includes both design and coding activities.

On the right side of the V, the activities are shown as bottom-up processes whose vertical scale goes from implementation at the bottom to validation at the top. The testing phase includes unit and integration tests, as well as performance and operational system tests. At the top of the V on the right side is the operation phase of the product. In the operation phase, it is often customary to submit the product to one or two forms of user-related testing, usually called "alpha" and "beta" testing, before declaring it a released product.

This model implies two important cost benefits to the manufacturer. First, tests needed by each level allow the tester to constrain the test code to the type needed, thereby reducing the costs associated with overlapping tests or test duplication. Secondly, the sooner testing starts, the sooner it produces benefits. The cost of testing depends on where the product is in the life cycle. By beginning testing at the unit test level and moving upward, problems get isolated and corrected at the level where their cost is minimized and they do not affect the next higher level's testing. While it is understandable that the same type of testing doesn't necessarily apply in all cases, the intention is to show how a controlled testing process makes it possible to deliver a thoroughly tested and verified software product that can work out-of-the-box.

Testability determines how efficiently a product can be tested. If there is an opportunity for a "clean sheet" design, it is important to induce testability into the design and the code. There is no single right way to do it. However, there are some important factors that influence it.

CREATING A TESTABILITY PROCESS

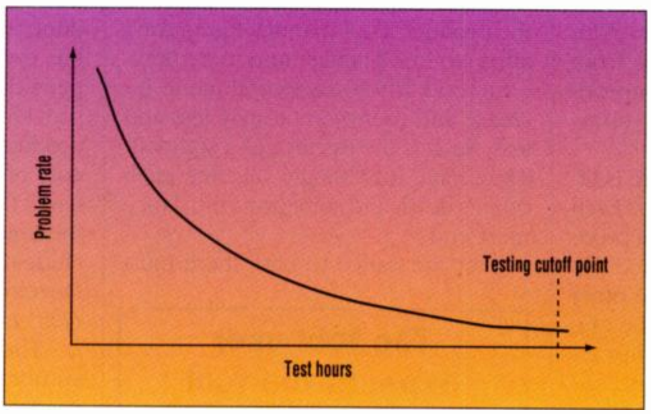
First of all, design and implementation should be performed in such a way that any testing is controllable. If tests can't be controlled, it is difficult to conduct testing as a coherent process. Second, the implementation of the code must be done in such a way that tests can make meaningful measurements in order to verify correct operation. Third, the design and code must be understandable to the testers. At some point during the testing phase, testers will need to have access to the code in order to develop test cases. If they can't understand what they are to test, the test process is going to be in trouble.

While testability is built in primarily during the development phase, the cost benefits don't appear until the testing phase. Testers frequently execute test cases as they attempt to verify and validate the design and related code. Changes to code are commonplace, and it is smart testing to test only those code modules that are affected by the changed module. Running only applicable tests can help minimize costs.

After recognizing the necessity to improve testing, the first job is to allocate experienced engineering resources to the test team. Without specifically getting into the management structure of such a team, there needs to be a team manager and one or more test design and development engineers. Besides designing and creating the test procedures, testers run the tests, identify problems, prepare problem reports, and submit them to the developer. The developer makes the modifications and resubmits the code to the testers. The process repeats until the tests do not detect any problems or until they meet some test termination criteria.

To achieve the best results from a product test effort, the engineers developing and running tests should not be the same people as those who are doing the design and development. This is needed to eliminate bias in the testing. These engineers are expensive assets, so it is just as vital that they be deployed productively. That comes from knowing what to do.

An important part of improving testing is to do some homework about what is possible. There are many good software engineering books and articles dealing with the subject of testing. A review of some of them will show that there are different methods of testing designed to meet different ends. By reviewing the methods, the team can select the type of testing that will do the best job for the product being tested in accordance with its cost/benefit constraints. There are many types of tests and thorough testing is expensive and time-consuming. It is best to do only what is necessary in order to avoid reaching a point of diminishing returns.



3. AT SOME POINT, *a decision must be made that testing is sufficient to release the product. This is usually a function of the number of new problems and their severity discovered after a given amount of testing. This number will seldom be zero, but a given length of time with no new problems, weighed against cost considerations, will usually indicate a testing cutoff point.*

It also is important not to confuse debugging with testing. A developer uses debugging to get code working so that it can operate at a primitive level. At that point it is not necessarily operating correctly. Testing identifies the problems and ultimately proves the code is correct.

CATEGORIES OF TESTS

There are essentially two categories of tests in common use: Static and dynamic. A third, based on formal mathematical approaches, is not widely used and will be excluded from this discussion.

Testers use static methods, sometimes called static analysis, to examine a product for problems without actually running the code. It is an easy and inexpensive way of finding errors of omission and syntactical problems. Reading code and comparing it to design documents is an example of this type of testing. Code reviews and walkthroughs are another.

Dynamic methods are much more important once a code module has been implemented and debugged. Testers use dynamic methods to test the response of a product to a set of known conditions. Most testing done during the testing phase of a product life cycle is of this type. The most common approaches consist of a series of test cases—called claims—in which each test case employs the seven steps as follows:

1. Statement of initial or given conditions.
2. Selection and design of method for the test case.
3. Selection of inputs.
4. Specification of expected results.
5. Execution of the test case.
6. Comparison of actual results to expected results.
7. Logging of test result.

Dynamic methods can result in a large number of test cases, which means that a lot of test code has to be developed and maintained. While it is possible to accomplish this through manual methods, the volume and structure of the test code cries out for some type of automated process. Automation returns cost benefits quite rapidly as it radically lowers the amount of engineering hours spent developing and maintaining test code. Maintenance of test code should not be overlooked as a cost area because it must change as the product changes. In addition, test designs may be flawed and have to be reworked. Integrating maintenance with an automated process to keep test code up to date saves time and money.

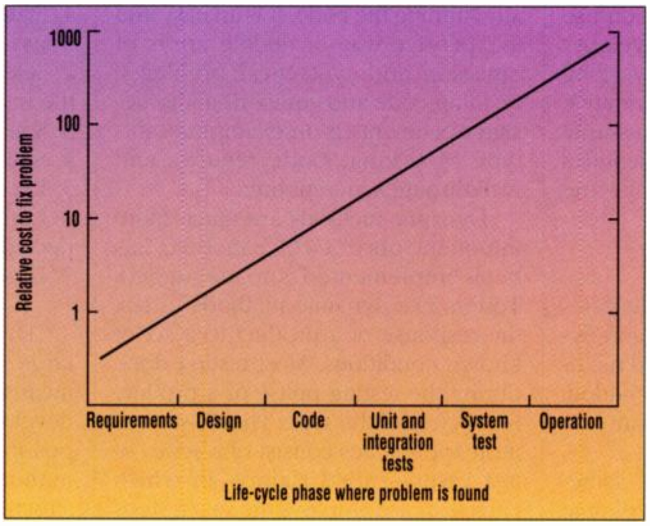
Referring to the V cycle product life model, consider the types of dynamic tests employed during the testing phase *(Fig. 1, again)*. Unit tests are intended to exercise code modules as they are debugged. Test designers use the detailed design specifications and other documentation about inputs and outputs to establish the test cases needed to prove the module's fundamental correctness. The testers design and develop these tests using a "black box" approach. To them, the product code is opaque—a "black box."

Unit tests don't need to be run all that often. They are useful when testing a new code module or when there are modifications to the product. The latter use is the one that is most prevalent because any new version or release of a compiler can have bugs. (Yes, bad tools can even cause problems in testing.) These tests help to remove that unknown from the equation. Unfortunately, with this methodology, there are many opportunities to miss conditions that need testing. However, there are other tests that can further validate the product.

CHECKLIST FOR PROSPECTIVE USER

Question	Reason for asking
How long has the company been in business?	Time in business can indicate company stability
Is the company the product developer?	Better technical support comes from the product's developer
How long has the product been on the market?	It takes time to develop a thoroughly tested, reliable product
What is an estimate of the product's installed base?	When coupled with its age, it gives an indication of a product's market acceptance
How many people are in the company?	This gives a clue about a company's overhead
How many engineers are in the company?	The ratio of engineers to total employees indicates if the company has a technical or marketing orientation
How many products does the company support?	The ratio of products to engineers gives an indication about product knowledge and the depth of support
With which tool chains is the product interoperable?	It gives an indication of the company's willingness to meet the customer's needs
Does the company have an internal independent test team?	An independent test team gives more credibility to the testing process
How many engineers are involved in testing?	The ratio of testing engineers to the total number of engineers gives an indication of testing commitment and capability
What kind of test processes do you employ?	This shows what kind of reliability to expect from the product
Do you employ automated procedures for performing and maintaining test code?	This indicates how well the company uses its test engineering resources
Do you perform characterization tests?	This indicates the availability of product performance data
Can your testing process stand up to the scrutiny of government entities such as the FDA, FAA, or CSA?	This is a good indication of a company's testing standards and thoroughness
Do engineers who developed the product handle technical support?	This shows that first-hand knowledge is best
How much time do you spend on customer support?	This indicates overall quality, robustness, and reliability of the product
What kind of warranty do you provide?	This indicates the company's perception of its product

When proven code modules have passed unit testing, they can be integrated into larger elements and tested for conformance with the preliminary product specification. Integration tests can include some or all of the product's code modules. The test team develops these tests using a "white box" methodology, which opens the code for the development of test cases. Due to such openness, the "white box" method is the opposite of the "black box" approach. The purpose of "white box" tests is to test all of the minor variations that are missed during "black box" tests and ensure proper code coverage.



4. FINDING AND FIXING *problems early in the development cycle is the best way to keep down the cost of development and meet time-to-market demands. The cost in time and money increases exponentially as problems turn up later in the cycle.*

System testing involves making a series of product-level tests to prove that it meets the documented requirements. The goal of this testing is to ensure functionality, as well as identify and correct remaining problems. Test code can be quite large, easily consisting of hundreds or thousands of test claims.

Depending on the nature of the product, several types of test approaches are commonly used for system testing because different types of tests are needed to fully test the product. For example, it is common to run test suites that only test failure scenarios in order to test the ability of the product to recover.

Another approach, stress testing, probes the limits of the product by putting it under heavy input loading. High-frequency inputs are where a lot of product designs fall apart. Stress tests are intended to find out where the product breaks down and the degree to which it can recover. The theory is that if it can hold together under such stress, it will probably do so for a user.

Stress tests are much different from the other tests. For one thing, they can be very processor-specific. Second, their design and what can be done with them depends largely on the capabilities of the processor board used for the test. It's pretty free-form and doesn't lend itself easily to an automated process, but the tests give a great deal of confidence.

Yet another important test approach is that of configuration, or scalability testing, which exercises the product in different configurations to prove that it can work. For a single product configuration, the preceding system test procedures can be fairly arduous and time consuming. However, if the product is configurable, the magnitude of the testing can quickly increase to an unmanageable size.

Ideally, such testing must include all possible configurations. However, in a highly configurable product, it is quite possible to have millions of possible configurations. Such a large number makes it impossible to test them all. A viable solution is to generate a set of product configurations that represent likely models customers would use. Assuming their representative nature, it is not unreasonable to take a position that if the set of configurations pass all claims in all test approaches, the tests are sufficient to prove correctness.

The trick to configuration testing is making the test procedure smart enough to recognize the configuration under test. Tests must be organized into modules that reflect the configuration's capabilities. If a capability exists in the configuration, there should be a module that can test it. This is a very tedious development, but it provides the essence of the test suite.

The testing process described is tedious but fairly straightforward. Be aware, however, that it has a hidden requirement. When determining the test conditions necessary to set up a particular claim, it is illegal to use a capability of the product that has not been previously tested and found to be correct. To do otherwise essentially invalidates the implementation of the claim. As in algebra, it is impossible to provide a singular solution to an equation involving more that one unknown. This is one of the realities of testing that causes the gnashing of teeth.

Whenever a test detects a problem, the tester should, as part of the problem report, assign it a number indicating its severity. The assignment of the severity levels is somewhat arbitrary, and there can be as many or as few of them as the test team decides *(Table 1)*.

To keep track of testing progress, it is advisable to maintain some data about it. The amount and type of data depends on the product being tested, but for each type of test in the procedure, a minimal set should consist of the following:

- Date of the test.
- The number of test cases (claims) in the test suite.
- The number of problems detected by severity level.

This data should be collected each time there is a test run. When presented in graphical form, it can show a great deal about the testing process *(Fig. 2)*. For example, the tests run on March 7 show a significant increase. Because the number of problems previously had been low, it would be reasonable to assume one of two possible causes. First, because the increase in the number of tests indicates a revision of the test suite, it is possible the 10 additional tests found more problems. Alternatively, there could have been a new version of the product introduced that day and it induced additional problems in previously tested modules of the product.

At some point, testing must cease because it will eventually reach the point of diminishing return. Is it possible to finish the testing process before reaching that point? There are statistical and mathematical methods detailed in the software engineering literature on how to determine when it is time to quit. Both types essentially rely on the amount of problems found as a function of test time *(Fig. 3)*. Mathematical formulas exist to calculate projections about product quality deliverable to the user. The concept is based on the probability of additional problems existing as test time increases without finding a problem. If the results indicate zero errors, it's time to stop testing and release the product.

OPERATIONAL PHASE TESTS

Having passed all of the rigors of unit, integration, and system testing, a product is often submitted to some form of customer-related testing. These are usually referred to as "alpha" and "beta" tests.

Alpha tests are ordinarily not performed by an actual customer but by the product's manufacturer using some form of simulation of the expected customer usage. Alpha tests are optional and are oftentimes not used at all. In fact, in a controlled product life cycle in which the product's requirements accurately reflect customer needs, alpha tests become unnecessary because their functions are integrated into system testing.

Many times, a product is often submitted to a set of customers or potential customers for the purpose of having them use the product under actual working conditions. The idea is that such "beta users" will use the software over some period of time and report back to the factory any occurrences of operational anomalies as well as suggestions for improvements. That may have once been possible when the economics of development were less brutal than today.

It is rare to find a user with resources to spare for beta testing, especially when such testing has a high probability of requiring the use of expensive engineering time. Applying engineering resources on beta-test projects rarely benefits meeting a user's development schedule. Consequently, good intentions about testing a "beta release" often give way to the realities of operating a business, and the intended testing either doesn't happen or is done superficially.

Simply stated, the beta user is not a controllable asset when it comes to testing. Moreover, in the case of development tools for embedded systems, the market is too small to justify extensive beta testing. An embedded-systems tool manufacturer cannot ship out a new tool to 10,000 or even 20,000 "beta sites" to prove the product works. Unlike the personal computer market, the sites just don't exist.

Conversely, the developer of an embedded product can't ship thousands of units that may or may not work properly. The hardware costs alone would be prohibitive and the possible scenarios would be ludicrous. Imagine a manufacturer shipping 2000 pacemakers to beta sites and then wondering why he hasn't heard back from the users! The solution is to control the test process completely using test methodologies that thoroughly verify correct operation.

It is rare to find a user with resources to spare for beta testing, especially when such beta testing has a high probability of requiring the use of expensive engineering time.

CHARACTERIZATION TESTS

Characterization of a product is simply a term for measuring its performance. This is especially true with a product that is highly configurable and where different configurations can yield different performances. The performance figures produced by a characterization suite tell the user if the software can handle the job required by the application.

When dealing with a configurable product, the characterization suite must be automated to about the same extent as the configuration test suite. It must be able to characterize any configuration of the product and provide performance results to the user or developer. The report of results is essential in that it assures the user not only that the configuration works, but also how well it performs.

In the case of selecting development tools, interoperability is an important aspect of software development today. It means that the elements of the tool chain work together. A tool chain encompasses all types of tools used to develop products for the embedded-systems market, including the obvious ones such as a real-time operating system (RTOS), compilers, linkers, simulators, and debuggers and emulators. For the developer, tool interoperability is a money issue because it bears directly on the cost of using the tools. Most developers today do not have uncommitted time in their work schedules that permit hacking with tools that don't work properly. If the tools don't work together, there are two choices: Spend many extra, unnecessary, hours of engineering time trying to complete a new product, or, buy another tool that does have interoperability with other tools. With the latter choice, the user has a better chance of making the market window.

MARKET REALITIES

To help bring about the end of the dance, we all must understand that the embedded-systems market is not the personal computer market. Although some developers of end-user embedded systems have large markets, their situation is still not similar to the PC software market. Embedded-systems tool manufacturers certainly do not have a large market. There aren't millions or tens of millions of users over which to amortize the cost of tool development and promotion. A successful tool has its volume measured in hundreds or thousands of units. And, unlike the PC software market, where the bar for "good enough" can be quite low, tools for the embedded-systems developer require a higher standard. End-user products built using such tools often have mission or life-critical requirements to them, and the tools used to build those products need to be better than PC quality.

It is no longer just a technical question of what a tool does but equally a question of the economic impact of its use. Tool quality influences the success or failure of the developer who uses it. Absent reliable tools, even a well-managed development and testing process can founder. When a tool fails to deliver the expected performance, the cost of the failure can quickly exceed the cost of the tool. It is the wise user who looks at more than just the selling price of the tool. What he doesn't see can cost him dearly.

Even if we disregard the costs of schedule slippage and lost opportunity and just consider the direct cost of engineering time alone, bad tools are expensive. For any tool failure, it is almost certain that the developer is going to spend engineering resources trying to figure out the problem. There is, after all, the possibility that the failure can be one of improper use of the tool. But it can take hours, days, or even weeks for engineers to diagnose the problem. And during that time, the tool user has had a lot of conversation with the tool-manufacturer's support staff trying to diagnose the problem. The failure is expensive for all concerned.

Tool providers have a perspective that permits a view from both sides of the street: As a tool manufacturer and as a tool user. As the former, it is often necessary to work with the same tools the customers use—the same compilers, emulators, and debuggers. As a tool user, the position of the tool manufacturer is a little further upstream than his customers. The tool manufacturer often feels the pinch sooner than his customers do when a tool he is using fails. Just like their customers, the tool manufacturers pay for the tool failure because he will inevitably spend valuable engineering resources trying to find out what the problem is. Schedules slip, costs go up, and market opportunities suffer.

ECONOMIC CONSIDERATIONS

Make no mistake about it, thorough testing of a software product is an involved process. It takes lots of time and people to do it. Does it make sense for application developers and tool manufacturers to get on that bandwagon? There are benefits to those who do. Forgetting for the moment a higher sales price, the relative cost to fix problems as a function of the phase of the product life cycle increases logarithmically *(Fig. 4)*. Note that the scale is logarithmic. Costs are lower the earlier problems are found. That is one of the main purposes of a controlled approach to testing.

There are other benefits as well. A thoroughly tested software product requires less routine maintenance and less customer support. That represents lower engineering costs and those savings go straight to the bottom line. Moreover, at least one study has

SOFTWARE QUALITY

shown that companies perceived as having high-quality products have returns on investment as much as double those lacking that perception. That suggests an improved competitive position, increased market share, and higher sales.

The question for which tool manufacturers have to get an answer is this: Will tool users pay more for the better tool, one that works and is well tested with verified conformance to requirements? Some of them certainly won't, but others will demand it. There are always those whose budgets are tight or who are inveterate gamblers. To them, low prices are important because they are willing to accept the risk of the untested tool. Some will accept the change rapidly while others will do it only reluctantly as they come to realize it will save them money at the same time it is reducing their risk.

Even today, when it is common to see engineering costs of $1000 per day, it is not uncommon to see a user squander valuable engineering time in repeated attempts to make a cheap, poorly tested tool meet his requirements. Where is the economic soundness in risking such an open-ended expense in order to keep from paying an additional amount for a better tool that can minimize the risk?

If a user has a tight schedule or must maximize productivity of development personnel, a well-tested tool, even though it has a higher price, will be a cost-effective choice. It also will reduce his own time and expense testing and fixing problems. The developer who can focus on implementing his application has a better return on investment than one who spends valuable time hacking on an untested tool trying to make it work properly.

Assuming there is a change to a more customer-oriented position among some but not all tool manufacturers, how does the potential user know what he is bargaining for? He certainly wants more than just sizzle; he wants the steak, too. What are the questions to ask the tool vendors? That is admittedly a very broad question, but a checklist integrating user-specific issues with some specific questions in can be a starting place *(Table 2)*. Asking these questions should get a prospective user a reasonably good picture of the tool manufacturer and his commitment to and capability of delivering a high-quality, reliable product. Don't settle for less, or the dance will continue.

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***Tom Barrett** is president of Embedded System Products Inc. He has been a consultant and contractor in embedded systems, on-line systems and real-time systems since 1968. He holds a BS in mathematics from the University of Texas.*

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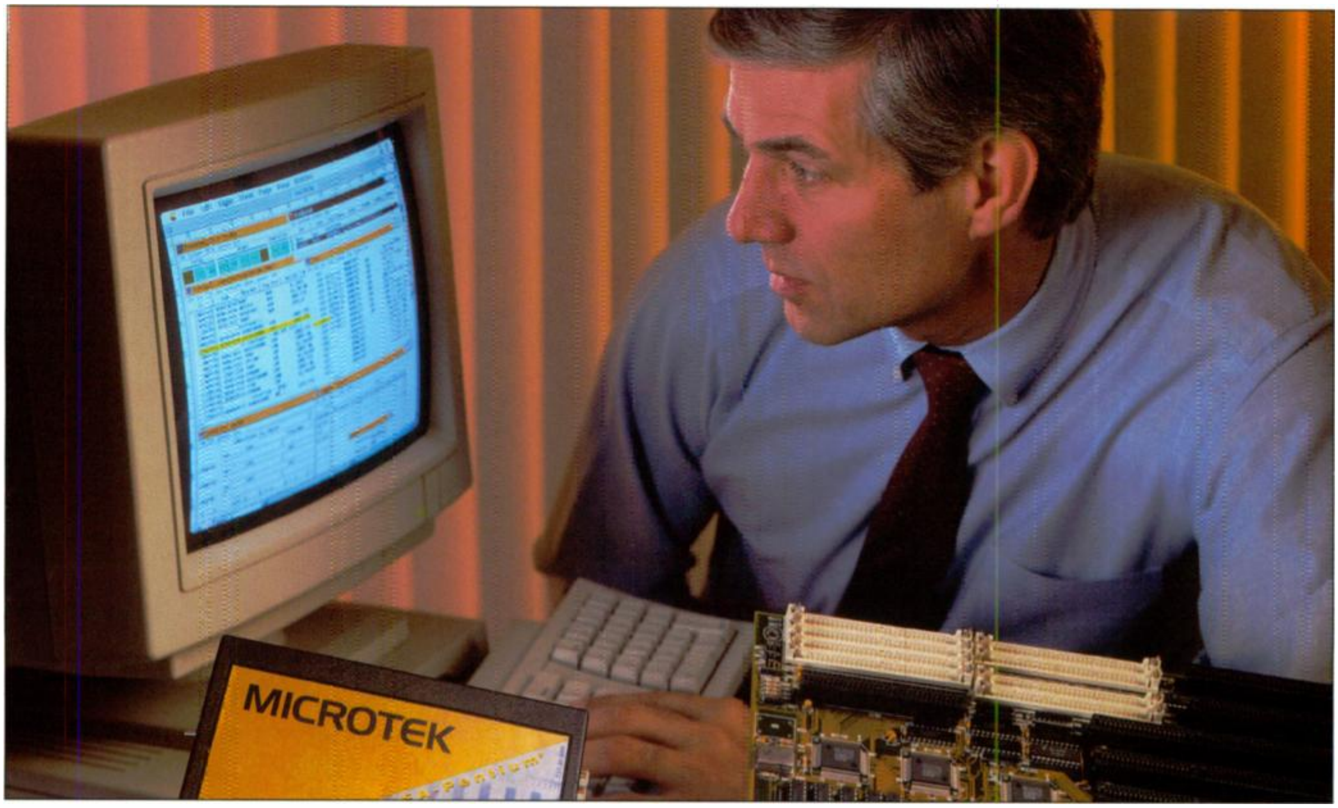

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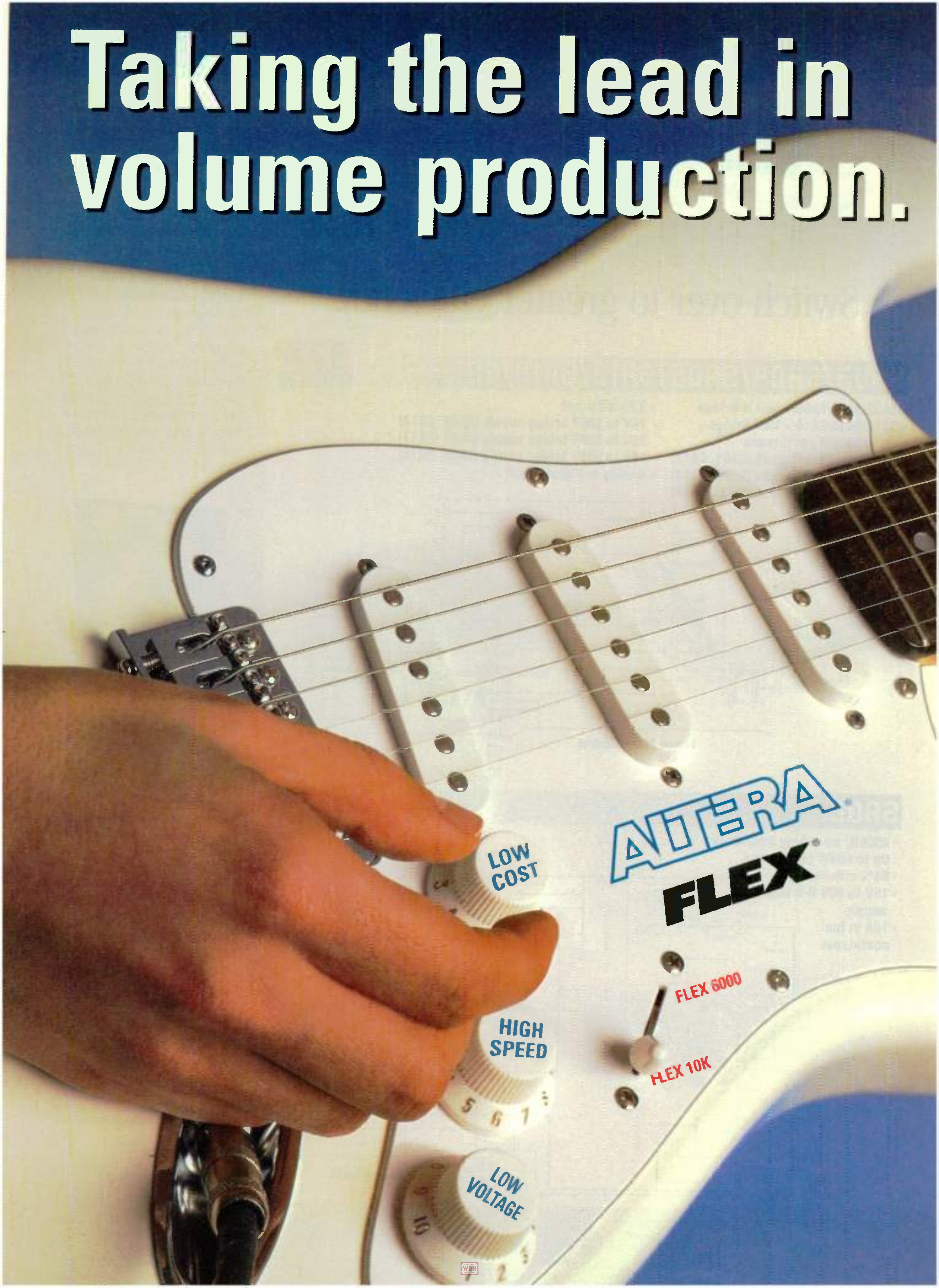
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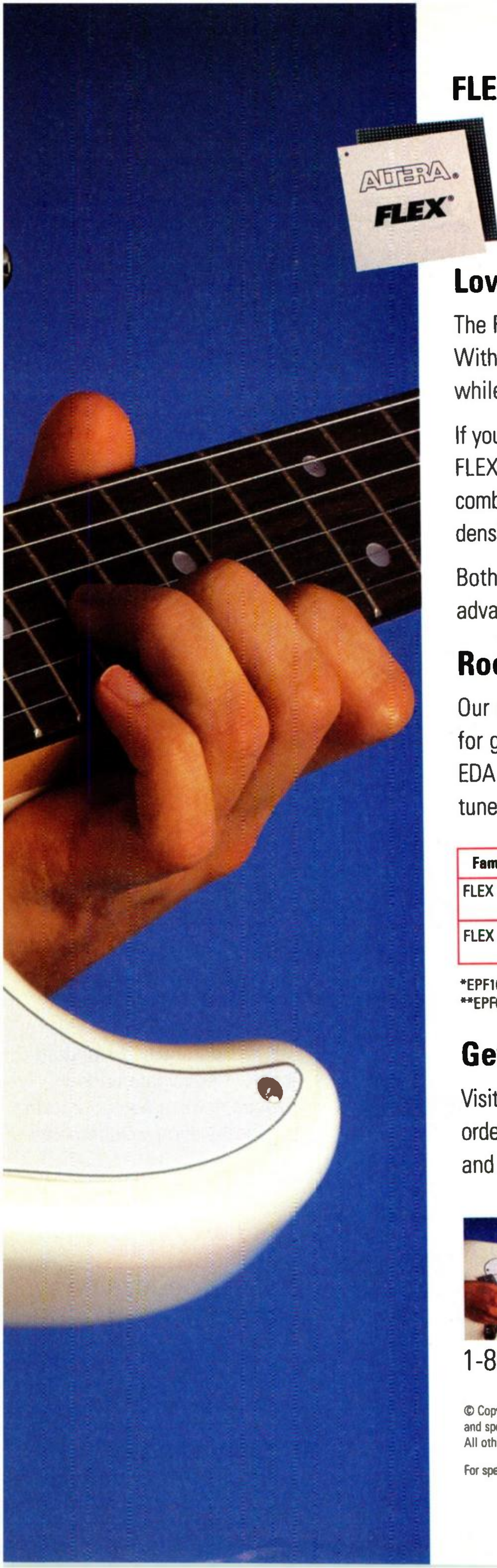

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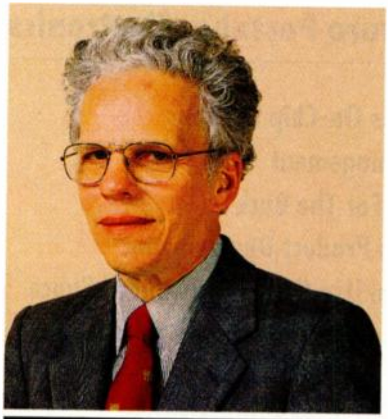
Frank Goodenough: 1925-1998

On Friday February 13, one of the best-known and most-respected individuals in electronics trade journalism, Frank Goodenough, bade us farewell after a long and courageous battle with cancer. His illustrious career as both a talented design engineer and an eminent technology journalist spanned more than 50 years, culminating in his position as *ELECTRONIC DESIGN*'s Analog and Power Technology Editor.

In the annals of our business, Frank was a legend when it came to the analog, mixed-signal, and power design engineering communities. For nearly two decades, he reported on developments in those fields with a knowledge that was unequaled. He put close to 100 major developments in those fields exclusively on the cover of *ELECTRONIC DESIGN*. As a technology journalist, he received the Jesse Neal Award for editorial excellence.

Frank had many close friends in the analog, mixed-signal, and power design engineering, academic, marketing, and public relations communities, many of them industry "movers and shakers" and legends in their own rights. Their names read like a *Who's Who* in the electronics industry. It was about two years ago that Frank was honored and roasted by *ELECTRONIC DESIGN* in Silicon Valley for his contributions to electronic trade journalism. That was an event that drew a couple of hundred notables from the electronics industry.



FRANK GOODENOUGH
1925-1998

Frank was the personification of the fountain of youth and the eternal optimist. He was biologically nearly 73 years of age (he was born Mar. 28, 1925, in White Plains, N.Y.), but his boundless energy and enthusiasm for his work and life was that of a 17-year old, and was, indeed, infectious. He was in touch with us constantly, even during his final days of his heroic battle with his illness, wanting to know what was happening in the analog, mixed-signal, and power areas. To the end, he was forever giving us his precious advice on the happenings in those areas.

Frank's knowledge of those fields was no accident, having worked for nearly four decades in those communities as a brilliant design engineer. Before joining the industry, he attended the Massachusetts Institute of Technology, and graduated from Drexel Institute of Technology with a BSEE.

Frank was a man with many interests and a genuine zest for life and all it had to offer him. His children remember him as seeker of information and knowledge, someone who was always questioning the nature of the world around him. He taught them that there are no dumb questions, and that the search for answers is a worthy endeavor.

As the only child of Frank Hamilton Goodenough and Clara Vorris Goodenough, he distinguished himself as an electrical engineer at such leading industry companies as Lockheed Electronics, Teledyne Philbrick, Brown and Root, and Analog Devices. He worked for two years at NASA, designing telemetry systems for the Apollo space program. He also worked as Section Head for Project Mohole, where he discovered acoustic interference between different sonars and developed a solution to the problem.

Frank brought his love for life to everything he did. He loved good food and wine, especially sharing it with friends and family. Dancing also was a passion, and he was a graceful and energetic partner. He loved poetry and many kinds of music, but the outdoors was his greatest source of enjoyment. He enjoyed archeology and geology. He loved hiking, and passed this enjoyment along to his children. Frank liked lively discussions of almost any kind. He had an interest in philosophy and a terrific sense of humor.

Frank was married for 42 years to Barbara Thompson Goodenough of Newton, MA. He is survived by her and their four children, Paula of Pittsfield, MA; Steven of Newton, MA; Sandra of Scituate, MA; and Theodore of West Bridgewater, MA; as well as six grandchildren.

This wonderful friend will be sorely missed by all who knew him. He may be gone from the scene, but he will always be with us in our hearts.

In accordance with his wishes, donations can be made to the Restless Leg Syndrome Foundation, 4410 19th St. NW, Suite 201, Rochester, MN 55901-6624; or Good Samaritan Hospice, 310 Allston St., Brighton, MA 02146.

Roger Allan
Executive Editor

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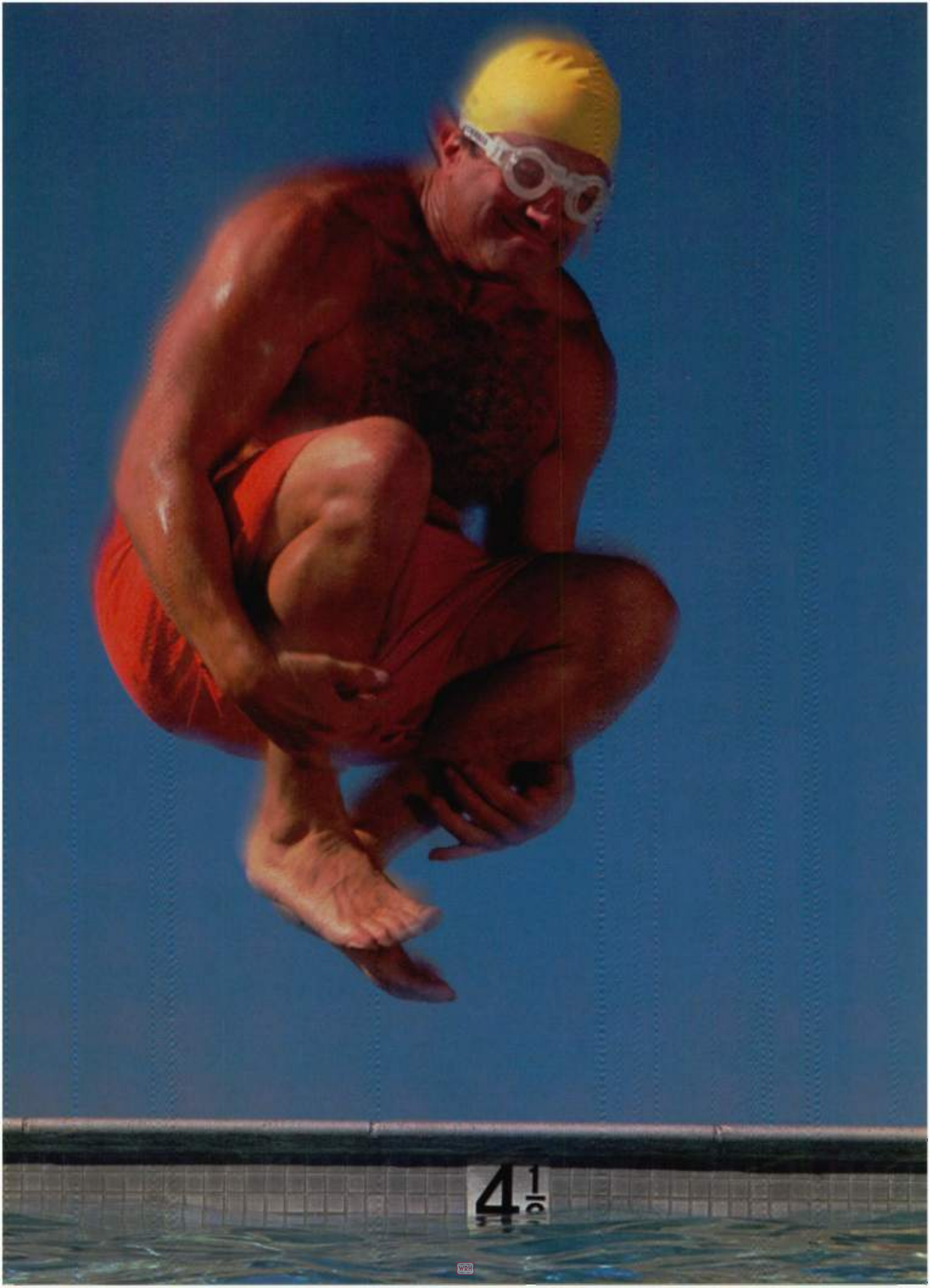
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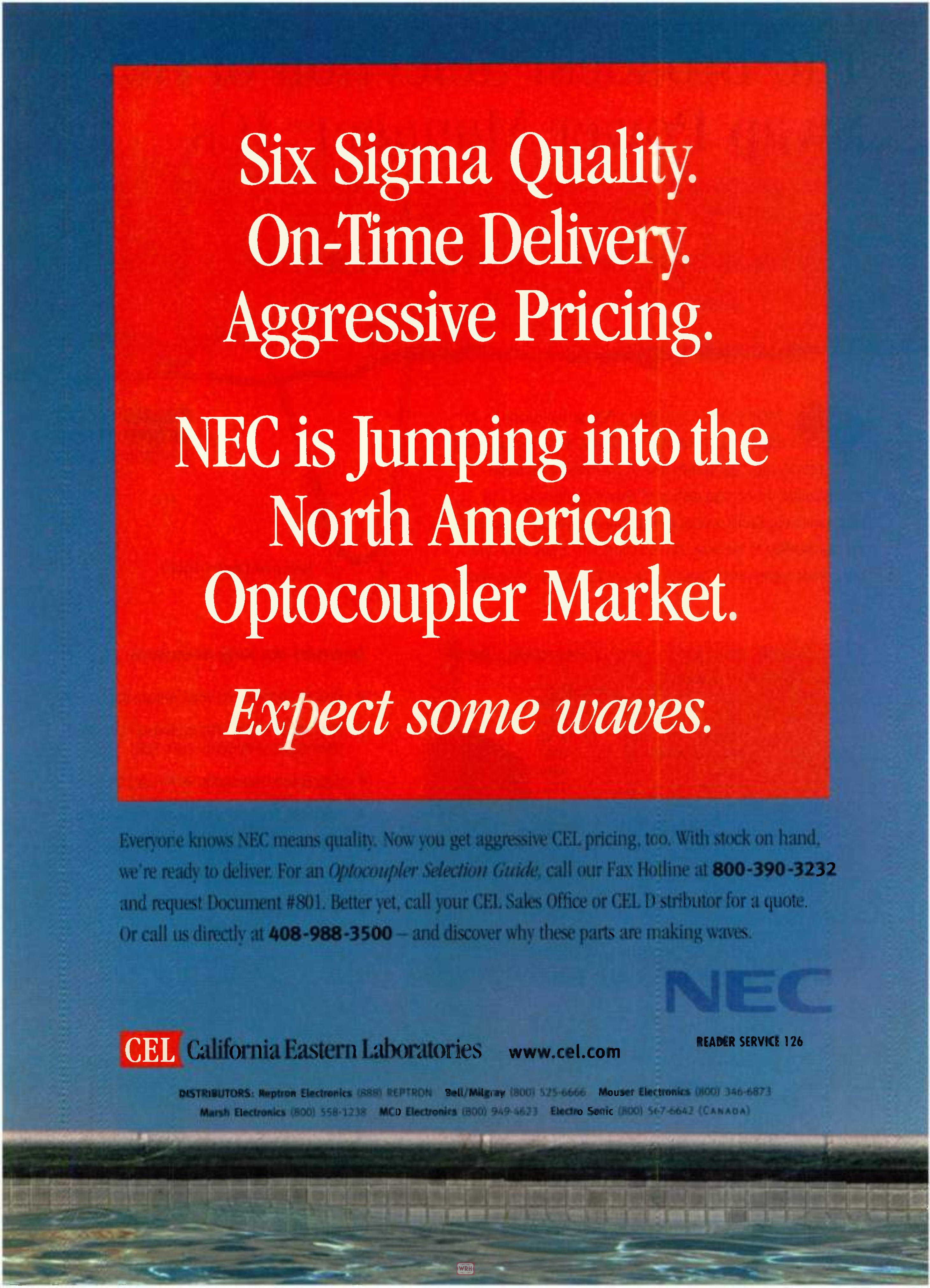

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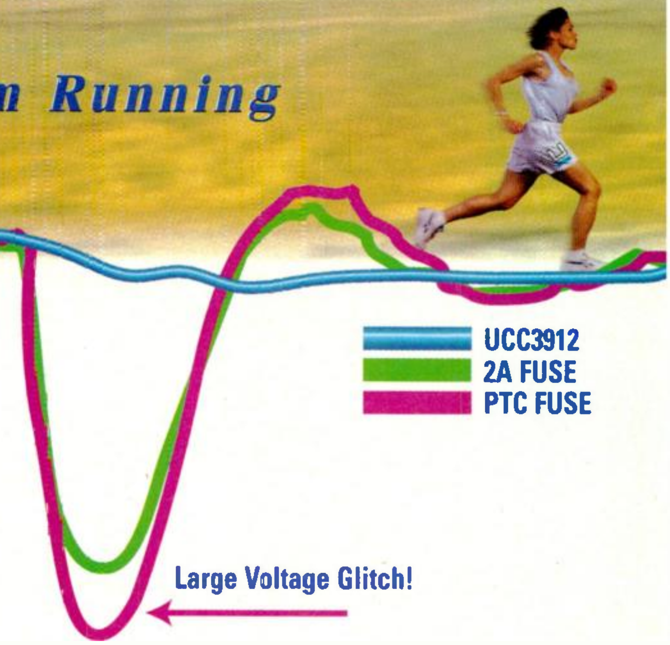

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Reach Out And Confuse Someone

One of my San Jose-based editors is lobbying me to upgrade his analog cellular phone to a spiffy new digital model. Of course, "upgrade" is a synonym for "Sure it costs more, but it has improved performance, a smaller footprint, and the to-die-for features that I just have to have."

In California, a cellular phone is not a business perk—it's a survival tool. Anyone who has ever crawled along the congested Silicon Valley freeways at rush hour can testify to the need for a cell phone. Because today's consumer advertisements push the benefits of digital cellular phones over their analog predecessors, I decided to do a little homework on the pros and cons of the two phone camps.

I picked up the February issue of *Popular Science*, which contained an article on cell phones. Next, I read a pile of press releases from manufacturers, and visited a local mobile phone store. From that research, it appears that the cellular manufacturers and resellers have followed the automobile leasing business model when it comes to jargon and confusing bottom-line costs.

Digital phones are touted as offering greater security, longer talk time, and better sound quality. They also offer such standard features as messaging, Internet access, and Caller ID. But not all digital phones speak the same language, so you run into problems when you're calling outside your service area. Analog cell phones, however, offer the broadest coverage area. But, digital phones also have dual-mode capabilities, so you can use your digital phone outside your service provider area, albeit, without the digital perks.

Once the coverage problems are worked out, pure digital phones will be the mainstay. But does that mean an end to analog technology? No. The folks at Texas Instruments made the point to me recently, that in their view, as digital technology advances, it drives the demand for more advanced mixed-signal/analog technology. And, there is the push to integrate digital and analog technologies on a single piece of silicon. If anything, we should see more advances as manufacturers work to improve analog ICs' performance, functionality, and packaging.

Now, if I can only get a grip on roaming fees, service costs, incoming call costs, monthly minute costs, and all the other annoying charges that service providers tack onto the cost of the phone. Then, I might just approve my editor's request.

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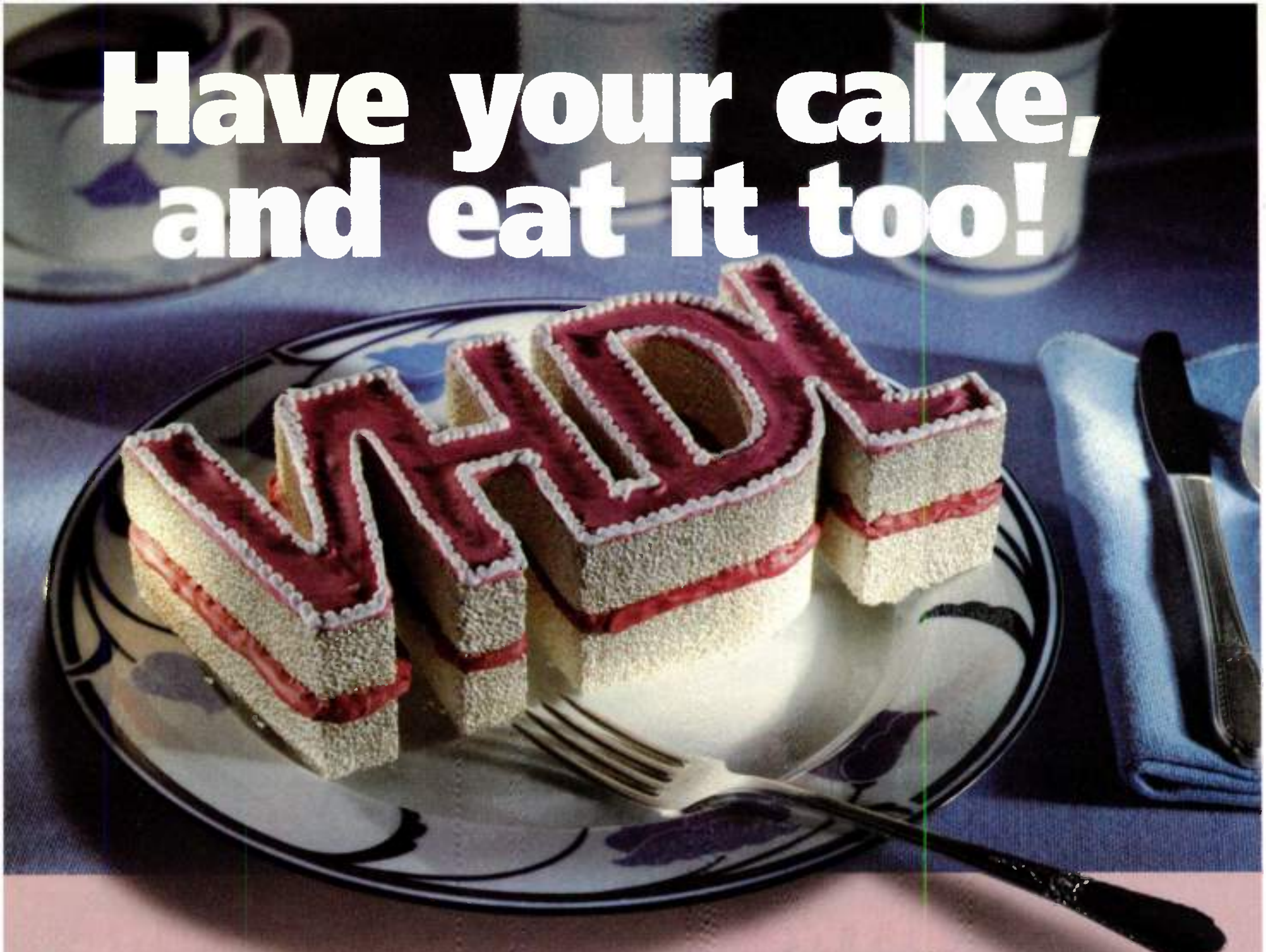

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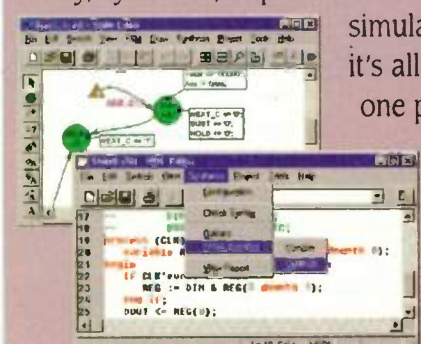

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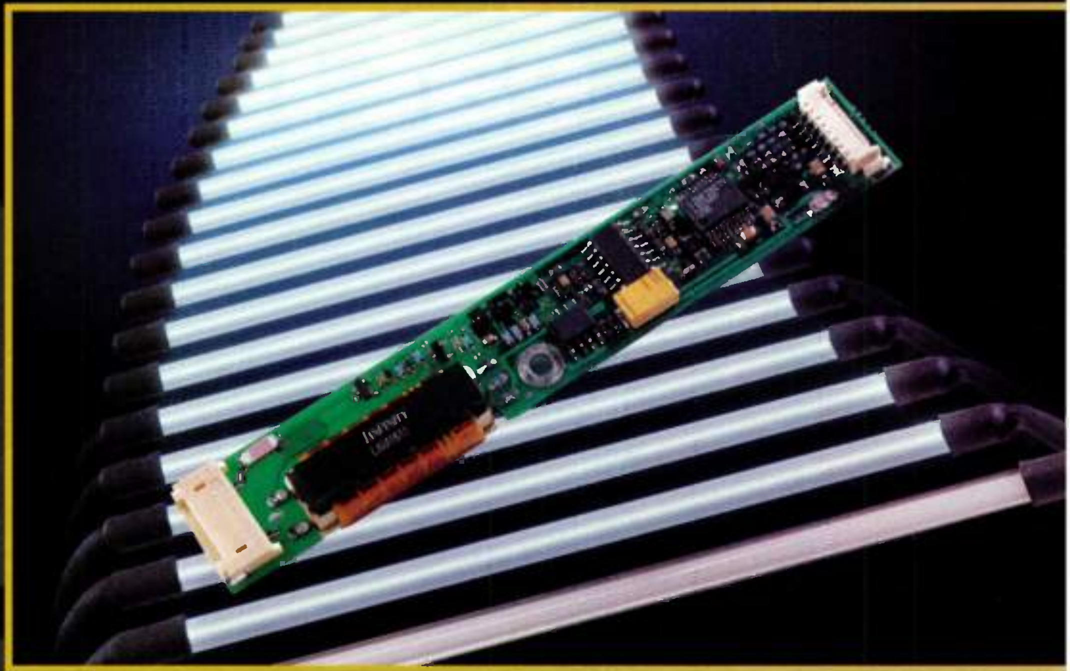

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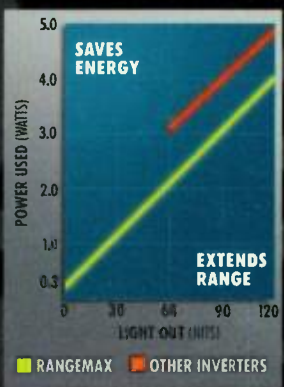

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Alternate UV Lithographic Technology Sought By Group

In an effort to maintain the U.S.'s leadership role in the area of advanced lithography, the EUV (LLC), (Extreme Ultraviolet Limited Liability Company), San Jose, Calif., and Silicon Valley Group (SVG), also of San Jose, have joined forces to develop advanced lithography equipment for production of 100-nm devices. In particular, the alliance will further investigate the feasibility of EUV lithography as an alternative to conventional optical lithography. Using extreme ultraviolet as a light source is expected to allow manufacturers to produce semiconductor chips with feature sizes of 0.1 µm or smaller. Such an advance also should make it possible to manufacture more powerful computer chips.

Under the terms of the agreement EUV (LLC) will provide SVG with vital EUV lithography insight. SVG, in turn, will offer its technical and equipment manufacturing expertise in an attempt to refine EUV technology. Also taking part in this effort is the Department of Energy's Virtual National Laboratory—a group representing Sandia National Laboratories, Lawrence Livermore National Laboratories, and Lawrence Berkeley Laboratories. Their responsibility will be to supply the proof of concept test system for EUV lithography. The system, to be built at Sandia National Laboratories over the next two years, will demonstrate the lithographic potential of the technology.

EUV (LLC) is currently comprised of three semiconductor manufacturer members—Intel Corp., Advanced Micro Devices, and Motorola. The group anticipates broadening its membership base as development efforts continue. For additional information on this alliance, contact SVG at (408) 441-6700, or check out its web site at *www.svg.com.* CA

Automated Test-Cell Solutions Under Development

Automated test solutions that offer high throughput and test-access capability are becoming essential for electronics manufacturers competing in a high-volume, intense time-to-market arena. Addressing this need, Hewlett-Packard, Palo Alto, Calif., and JOT Automation, Oulu, Finland, have joined forces to develop automated solutions for electronic-manufacturing test cells.

Under the terms of the agreement, JOT—a developer of solutions for complex printed-circuit-board transport and handling problems—will develop and manufacture board handlers designed specifically for HP 3070 test systems. Hewlett-Packard will, in turn, develop next-generation solutions for board-test problems. Both companies will work to combine their expertise in such technology areas as test-cell management software and HP 3070 system integration, including fixture and test-software integration. It's hoped that by combining product lines and associated technologies, test-package solutions will be created to successfully meet test-cell-automation requirements in a number of different test industries.

For more information on this joint venture check out JOT Automation's web site at *www.jotgroup.com*, or visit HP's site at *http://hp.com/go/tmdir.* CA

Color Field-Emission Displays Emerge From Laboratories

After many years of being a laboratory curiosity, field-emission displays will shortly be commercially available in both color and monochrome versions. At the recently held DisplayWorks conference in San Jose, Calif., researchers at Motorola Inc., Tempe, Ariz., demonstrated its first FED—a color 5.1-in. diagonal flat panel with quarter VGA resolution (320-by-240 color pixels).

FEDs are based on the same concept used in CRTs—electrons are emitted from a cathode and accelerate through a vacuum using a high-voltage (5 kV or so) to strike a phosphor-coated anode and cause various colors of light to be emitted. However, unlike the CRT, which has a single hot-cathode source whose emitted electronics are "swept" across the screen by deflection circuits, FEDs consist of an array of millions of electron-emitting microtips that form the cold cathode. Hundreds of microtips are dedicated to driving each pixel. Thus, barring a catastrophic failure of an entire row or column, individual pixels have a lot of built-in redundancy, and the resulting images are very crisp.

The distance between the microtips and the anode is just a millimeter or so, which allows designers to create very thin panels. The filament-free nature of the cold-cathode structure enables the displays to operate at low temperatures (as low as -45°C) and at relatively high temperatures (up to 85°C) with minimal reliability issues.

Late last year, PixTech, Santa Clara, Calif., demonstrated a monochrome quarter-VGA-resolution FED that can produce up to eight gray shades. The panel features a diagonal of 5.2 in. (4.8 by 4 in.) and a thickness of just 0.79 in. The company also has color FED panels with quarter, half, and full VGA resolution in development. They will be able to display true TV colors and full-motion video with resolution that can't be distinguished from a CRT showing a VHS video tape. Display brightness for standard monochrome versions is about 70 fL (with high-brightness versions able to deliver up to 150 fL), while the color panels deliver an image with a brightness of about 200 NITS. The emissive displays also have a wide viewing angle—typically over 160°, horizontally and vertically.

For more information, check out the Pixtech's web site at *www.pixtech.com* or contact Motorola at (602) 755-5500. DB

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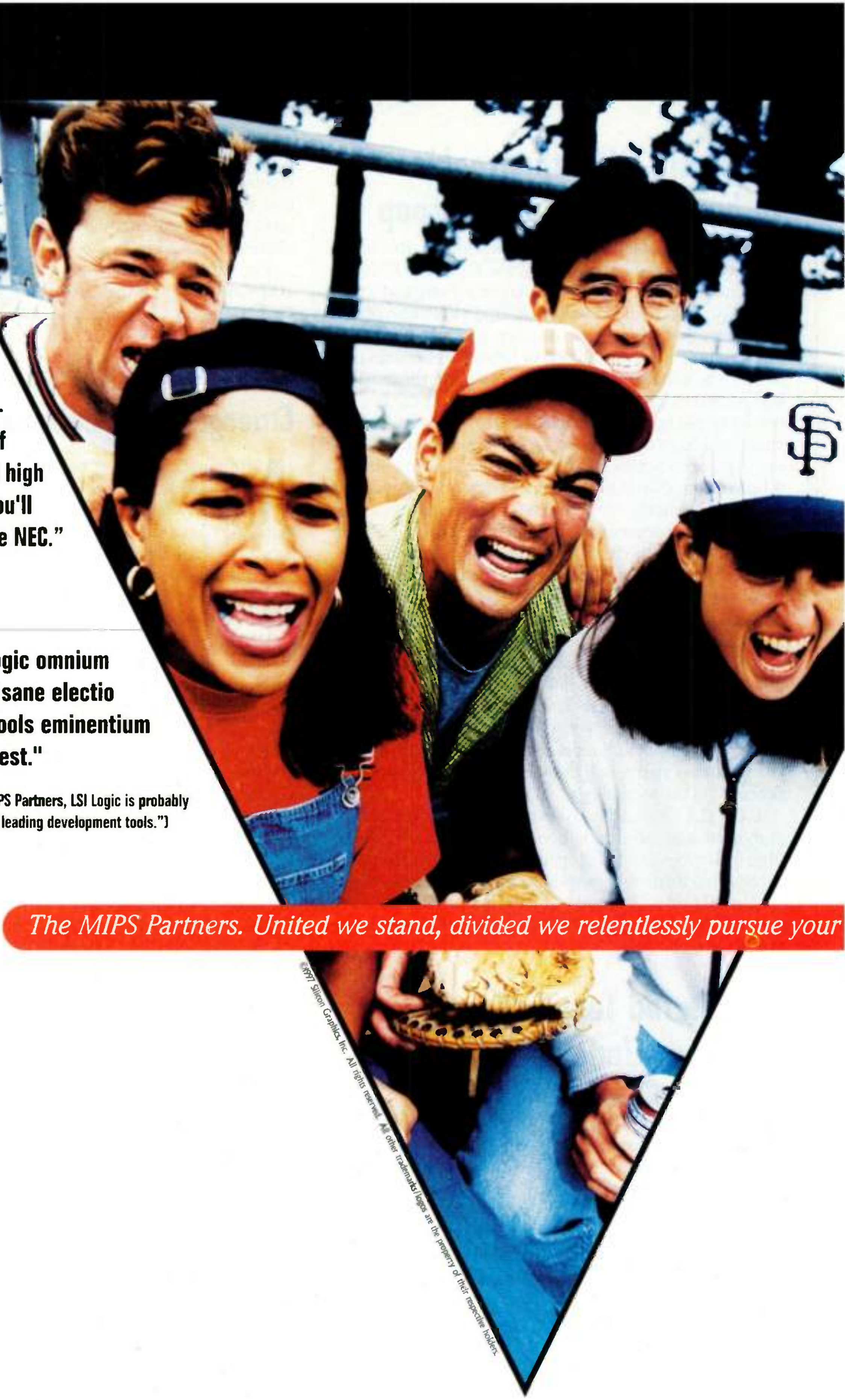

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Photonics Association Formed To Boost Research, Developments

A new organization charged with helping to facilitate the promotion of research and achievements in the field of photonics has been formed in Colorado. Known as the Colorado Photonics Industry Association (CPIA), it will bring together professionals in industry, education, and the government who work in photonics-related areas in research, development, and manufacturing. The formation of this organization is particularly apropos in Colorado, because it has blossomed into a hot bed for research and development in the photonics industry.

Based in Denver, the CPIA will seek to leverage ongoing photonics activity to encourage collaboration and transfer of technological information between its members. Specific goals of the CPIA focus on four key areas. First is to represent Colorado's photonics industry nationally, as well as on a global basis. Second is to help in the development of educational funding, with the aim of meeting future staffing needs. Third is to provide meetings with guest speakers, reduce exhibition fees at conferences, and a scholarship program. And, finally, they plan to maintain a database of company, university, and national laboratory capabilities.

The CPIA is now accepting memberships. Additional information regarding membership, current members, or CPIA directives, can be obtained by contacting (303) 833-4333. CA

Audio Products Should Create A Stir In Home Entertainment

The future of home entertainment, whether in the form of computers, DVD players, digital television receivers, or improved set-top boxes, promises to be exciting thanks to developments in digital multichannel audio technology. Hoping to capitalize on these developments Altec Lansing Technologies Inc., Milford, Pa., and Zoran Corp., Santa Clara, Calif., have entered into a strategic alliance to develop high-quality home-entertainment audio products at prices affordable to both OEM manufacturers and consumers.

Under the terms of the agreement. Altec will use its own patented side-firing speaker design combined with Zoran's ZR38600 Digital Audio Signal Processor technology to create a new family of products featuring Dolby Digital AC3 surroundsound audio reproduction systems. Zoran's ZR38600 high-performance processor is capable of real-time single-chip decoding of Dolby Digital AC3 5.1 channel and MPEG2 digital algorithms, as well as Dolby Surround/Pro-Logic data streams. Due to its high processing power, it may be able to serve as the engine for future sophisticated signal processing.

Both companies feel this alliance should culminate in products that offer greater flexibility in meeting a wide range of multichannel digital-system requirements at a low cost. For further information, contact Altec Lansing Technologies at (800) 258-3288 or at *www.altecmm.com*. Or contact Zoran at (408) 919-4111 or *www.zoran.com*. CA

Monitoring Technique To Develop Vias Uses Micromachined Sensor

High-yield multichip-module manufacturing on large-area substrates—that's one of the goals set forth by the Packaging Research Center (PRC) at the Georgia Institute of Technology in Atlanta. To achieve that goal, the PRC's Intelligent Large Area Manufacturing team is looking at microsensor technology for process monitoring. One novel technique has already been developed by associate professor Dr. Gary May and graduate student Michael Baker. It monitors film thickness in plasma etching, which is critical for the plasma de-scum step. That occurs at the conclusion of via formation using photosensitive polymer dielectrics.

According to May, the plasma de-scum step is crucial to ensure that the via is fully opened. If the via is improperly "de-scummed," the residue that remains after the via is exposed can increase the resistivity of the connection between the metal layers.

The lower-cost sensor allows direct, non-intrusive, and real-time measurement of each etch rate. The prototype sensor correlates film thickness with the change in resonant frequency that occurs in a micromachined platform during etching. The platform is suspended over a drive electrode on the substrate's surface and then is electrically excited into resonance. As material is etched from the platform, its resonant vibrational frequency shifts by an amount proportional to the amount of material etched, allowing the etch rate to be inferred.

As a proof-of-concept experiment, researchers fabricated a platform consisting of DuPont 2611 polyimide. The sensor was driven into resonance electrostatically, and the shift in resonance was detected by monitoring the change in impedance between the drive electrode and platform as the drive frequency is swept. To enhance filtering of the sensor signal in the noisy plasma environment, the platform is designed so that the ratio of the plasma frequency to the fundamental mode of vibration is approximately 400:1. The prototype was etched in a Plasma Therm 700 series etching system in a CHF_3/O_2 plasma. Electrical contact was made with the sensor using a feed-through attached to the vacuum line beneath the process chamber to facilitate in-situ excitation and measurement. May says the sensor was shown to offer high resolution (approximately 1300 Hz/µm) and a near linear correlation between film thickness and resonant frequency.

For more information, contact Gary May at (404) 894-9420, or e-mail at *gary.may@ece.gatech.edu*. RE

Edited by Roger Engelke

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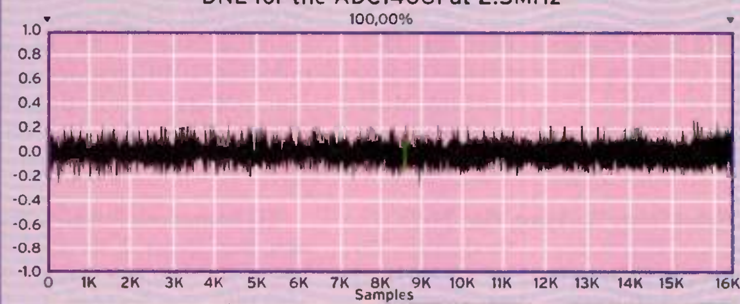

Part Number	Resolution	Conversion Rate	Power Consumption	DNL (LSB, typ)	Packages
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Southcon/98, Mar. 24-26. Orange County Convention Center, Orlando, FL. Contact Electronic Conventions, (800) 877-2668 or (310) 215-3976; fax (310) 641-5117; www.southcon.com

First Conference On The PC & Automation, Mar. 26-27. Paris, France. Contact Interbus Club USA, P.O. Box 25141, Philadelphia, PA 19147, (888) 281-2871; www.interbusclub.com.

INFOCOM '98, Mar. 28-Apr. 2. Hotel Nikko, San Francisco, CA. Contact Ramesh Nagarajan, Lucent Technologies, 101 Crawford Corner Rd., Rm. 3M-318, Holmdel, NJ 07933; (732) 949-2761; fax (732) 834-5906; e-mail: rameshn@lucent.com.

IEEE International Reliability Physics Symposium, Mar. 30-Apr. 2. Reno Hilton Hotel, Reno, NV. Contact Ann N. Campbell, M/S 1081, Sandia National Labs., P.O. Box 5800, Albuquerque, NM 87185-1081; (505) 844-7452; fax (505) 844-2991; e-mail: ancampbe@sandia.gov.

IEEE International Parallel Processing Symposium/IEEE 9th Symposium on Parallel and Distributed Processing (IPPS/SPDP), Mar. 30-Apr. 3. Delta Orlando Resort, Orlando, FL. Contact Viktor Prasanna, EEB-200C, Department of EE Systems, University of Southern California, Los Angeles, CA 90089-2562; (213) 740-4483; fax (213) 740-4418; e-mail: prasann@ganges.usc.edu.

Embedded Systems Conference Spring, Mar. 31-Apr. 2. Navy Pier Festival Hall, Chicago, IL. Contact Liz Austin, Miller Freeman Inc., (888) 239-5563; (415) 538-3848; e-mail: esc@mfi.com.

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China Telecom 2000 Conference, Apr. 7-8. Holiday Inn Capitol, Washington, D.C. Contact Information Gatekeepers, (800) 323-1088; (617) 232-3111; fax (617) 734-8562; e-mail: igiboston@aol.com; www.igigroup.com.

20th IEEE International Conference on Software Engineering, Apr. 19-25. Kyoto International Conference Hall, Kyoto, Japan. Contact Koji Torii, Graduate School of Information Sciences, Nara Institute of Science & Technology, 8916-5 Takayama-cho, Ikoma-shi, Nara-ken 630-01, Japan; +81 7437-2-5310; fax +81 7437-2-5319; e-mail: torii@is.aist-nara.ac.jp.

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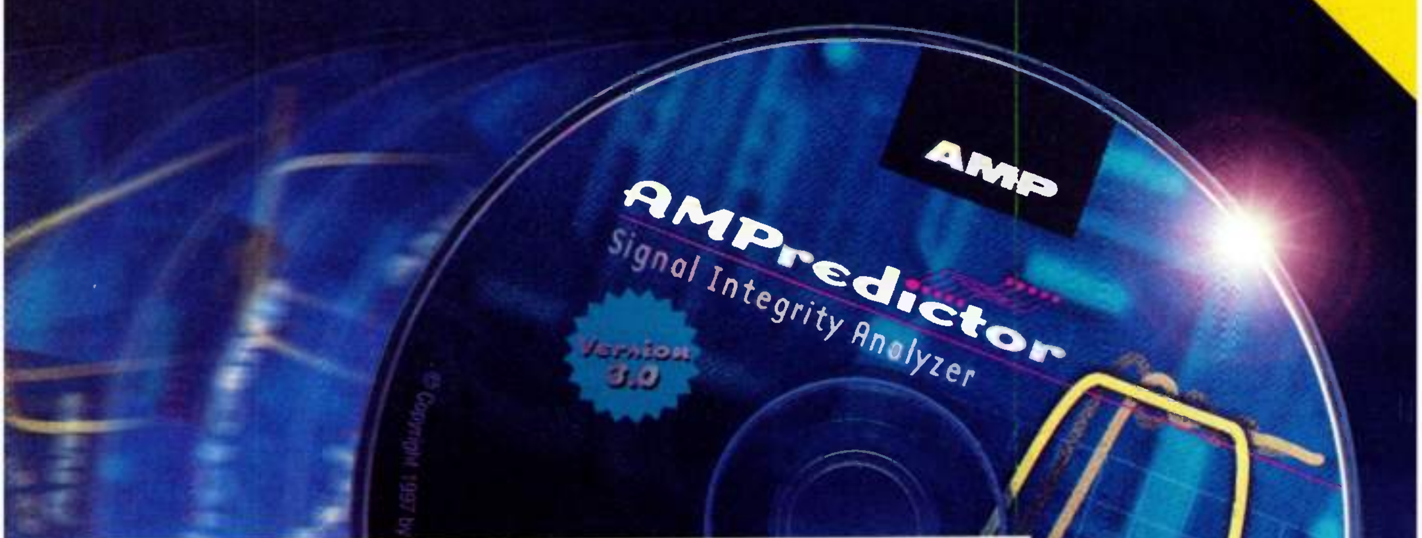

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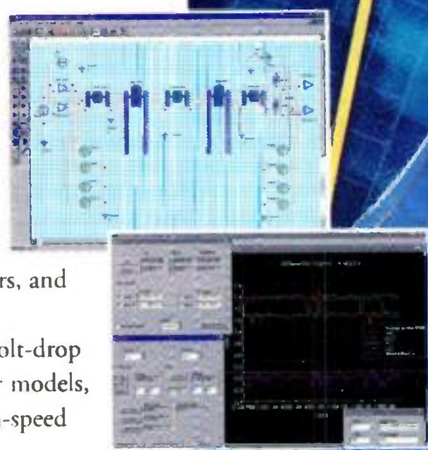

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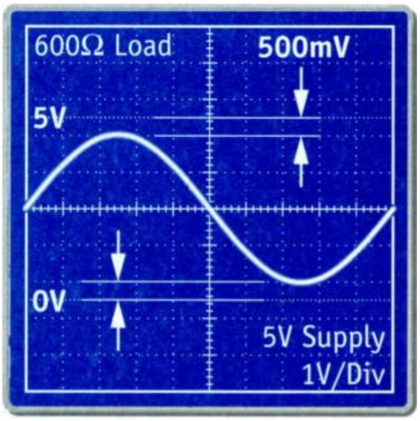

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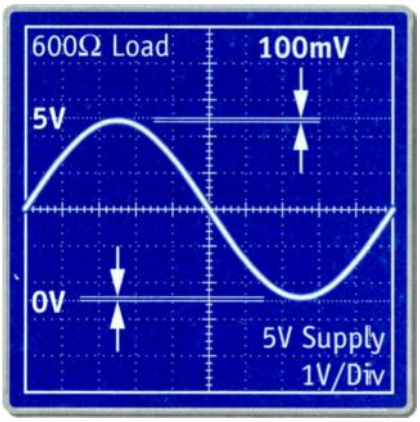

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Silicon Micro-Aligner Trims Cost And Yields Perfect Optical-Fiber Alignment

This silicon-based, active micro-aligner promises a low-cost, in-package solution for keeping spliced optical fibers or fiber/laser diode interfaces in perfect alignment. Demonstrated for the first time in February, at the Photonics West Conference in San Jose, Calif., by The Boeing Company, St. Louis, Mo., and MCNC, Research Triangle Park, N.C., the three-axis device exhibited movement of greater than 10 µm on all three axes.

In fiber-optic-based systems, the packaging and fiber-to-fiber splice alignment costs tend to dominate the overall expense of assembly. That has, to some extent, limited the use of fiber-optic based systems. However, with this prototype microelectromechanical system (MEMS), designers will have a device that fits into a standard 14-pin optoelectronic hermetic butterfly package. It measures less than 5 by 4 by 0.5 mm, and is expected to cost just a few dollars per fiber splice.

This performance would allow assemblies to achieve alignments with accuracy errors of less than 0.2 µm. They also could do the alignment in less time than any machine-automated approach, explains John Haake, a senior project engineer for Smart Structures and Systems at Boeing. When mass produced, commercial versions can be fabricated on chips as small as 1 by 1 mm, which would allow thousands of in-package micro-aligners (IPMAs) to be built on one wafer.

The IPMA employs a novel thermal-actuator technology based on nickel-surface micromachining to achieve large forces (about 10 µN) and significant displacements. The device eliminates the need for an expensive and limited-throughput alignment robot. It could free designers from the constraints associated with packaging photonic circuits, while providing maximum performance because fibers would be optimally aligned.

Although other alignment techniques have employed electromagnetic, thermal, electrostatic, piezoelectric, and shape-memory alloys, this is the first MEMS-based solution small enough to fit in the hermetic packages. The IPMA chips contain both mechanical and electronic functions, and can be mass produced to provide a low-cost solution.

On the experimental IPMA chip described by Haake at the conference, the actuators were micromachined into the silicon using a technique called LIGA (a German acronym that refers to lithography, plating, and molding). Although the experimental chip only has three actuators, one for each axis, the LIGA technique would allow designers to place dozens or even hundreds of active nickel structures on a single chip.

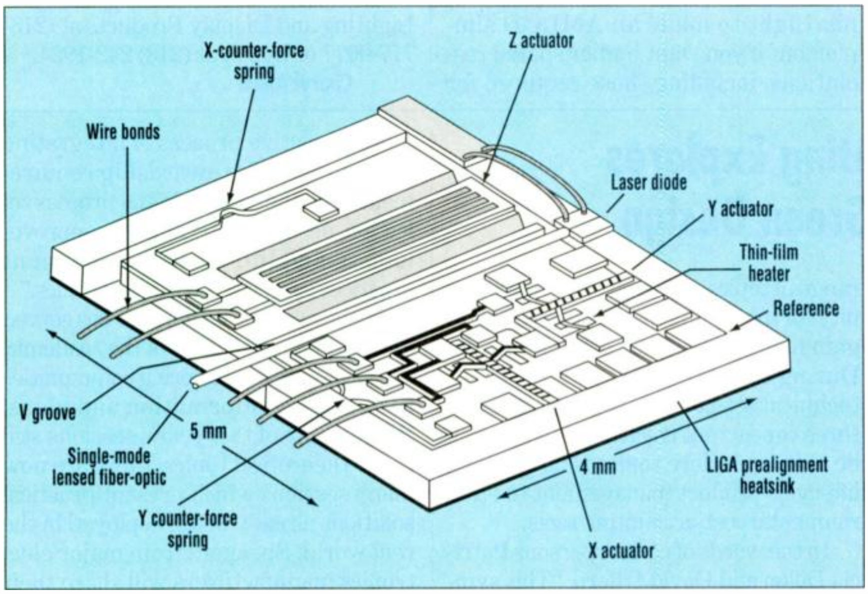
Along with the actuators, the chip uses counter-force springs for the X- and Y-axis movement, thin-film heating elements for the actuators, and a V-groove slot for initial positioning of the fiber *(see the figure)*. The structures are all formed on a region of silicon referred to as a stage. This area is formed by first depositing a silicon-nitride layer on the silicon using plasma-enhanced chemical vapor deposition. Next, the stage region is separated from the rest of the chip by bulk-etching around its perimeter. A low-stress low-pressure CVD (LPCVD) silicon-nitride layer, patterned on both sides of the wafer, protects the silicon stage from the etching.

Surface micromachined layers are then patterned to form the thermal-isolation structures and microheaters for the thermal actuators. A thick electroplated nickel layer is patterned using the LIGA technique, which employs synchrotron-based deep-X-ray lithography to define the structures. LIGA allowed the designers to define high-aspect-ratio structures. These are crucial to obtaining actuation in the plane of the IPMA chip. They also aid in defining corresponding spring structures with high in-plane compliance and high out-of-plane stiffness. LIGA also allows plating heights thick enough to form passive fixturing guides for the fiber and precise edge-reference structures.

Following LIGA patterning, the movable portions of the nickel structure are released via sacrificial etching. The silicon is then subjected to anisotropic etching to cut away the stage from the rest of the chip, and thermally relieve the thin-film heaters. Here the silicon-nitride layer is used as an etch mask. This leaves the stage suspended by nickel springs defined by the LIGA processing, and very responsive to the three thermal microactuators.

The work on this project was done under an Army Research Office contract funded by the DARPA-Defense Sciences Office. For more information on the IMPA chip, contact Daniel Davison at (314) 233-5416 or e-mail: daniel.davison@boeing.com.

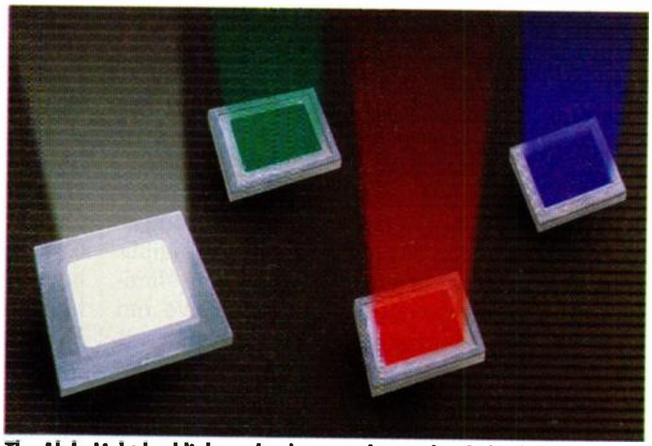
Dave Bursky



The three-axis MEMS micro-aligner, developed by Boeing and MCNC for fiber-optic systems, uses thermal actuators to move the fiber by as much as ±10 µm in the X, Y, and Z axes.

New Backlight Device Promises Increased AMLCD Performance At A Lower Cost

Although active-matrix, liquid-crystal displays (AMLCDs) have long been a dominant technology in the display industry, they are now being stretched to their technological limits by advances in digital devices. While some researchers have turned their development efforts toward potential replacements for AMLCDs, many continue to try to improve the basic AMLCD technology. To that end, a team at Teledyne Lighting and Display Products, Hawthorne, Calif., has developed a small-aperture backlight illuminator that promises to enhance AMLCD resolution significantly, while decreasing costs.



The AlphaLight backlight technology can be used to light the primary colors and white areas sequentially. Developers believe that its performance, coupled with its low cost, will change the way many active-matrix liquid-crystal displays are implemented.

The technology, known as AlphaLight, can be used to sequentially light the three primary colors—red, green, and blue (RGB)— as well as white light up to a distance of approximately 2500 fL *(see the figure)*. It operates with either a constant or pulse-width-modulated low-voltage dc drive, and can be individually color addressed at on/off times of less than 100 ns. The illuminator produces light in the 470 to 660 nm wavelength range, without distortion or discontinuity, and with a luminance uniformity of 3% over a lit surface. Developers say the technology also has achieved a 15,000:1 full dynamic range dimming capability.

AlphaLight operates instantly with no ac noise. It does not require warm-up or overvoltage start-up when first addressed. Additionally, it needs no inverters or transformers, as do electroluminescent (EL) or fluorescent lamps. As a result, the AlphaLight backlight is much easier to integrate in display systems than conventional backlight technology. According to David Pelka, one of the inventors of AlphaLight, "You can not only use AlphaLight to make an AMLCD simpler, but if you want higher spatial resolutions, including those required for formatting HDTV, this looks like the best way to do it—and do it with current TFT deposition capabilities."

The technology is designed to be used in conjunction with color-sequential imaging (CSI) techniques. This not only accounts for the increased resolution, but enhanced operational life and product portability as well. In fact, using AlphaLight sequential color illumination, an AMLCD dot matrix with individually multiplexed pixels can produce a fully saturated color video, graphics, and information display.

Each pixel is filled during its "on" cycle as opposed to being split into separate pieces, assigned a primary color, and then filled in with that assigned color, as is the case with nonemissive color AMLCDs. The net effect of this approach is that the fill factor, and as a result, the resolution, increases.

Because it eliminates the need for costly color filters, and uses a simplified on-glass thin-film transistor architecture, the AlphaLight technology is much less complicated and expensive to manufacture than conventional AMLCDs. Additionally, the technology enables the elimination of up to 75% of the drive and address circuitry commonly found in modern AMLCDs.

For information, contact Teledyne Lighting and Display Products at (213) 777-0077 or by fax at (213) 242-1924.

Cheryl Ajluni

IEEE Environmental Meeting Explores Practical Solutions For Green Design

Now in its sixth year, the IEEE International Symposium on Electronics and the Environment (ISEE) has starting moving away from theoretical topics to more practical solutions. The pioneering conference seeks to prepare engineers and technical managers to address the environmental concerns that will shape the electronics industry during the next century.

The ISEE, which will be held May 4-6 at the Hyatt Regency Hotel in Oakbrook, Ill., deliberately presents a broad range of topics, allowing a rare opportunity for management and design staff to gain insight into each other's worlds. During the three-day conference, 18 technical sessions will be presented in three concurrent tracks. Attendees will be able to explore topics ranging from life-cycle product management to environmental cost-accounting tools.

In the words of cochairpersons Patricia Dillon and David Ufford, "This symposium goes beyond mere compliance with regulations and laws to champion a more proactive process of integrating environmental stewardship requirements into the materials and process selection, design and technology improvements, and life-cycle management practices associated with electronics."

In the past, the conference has served as a forum for members of the academic, corporate, and engineering communities to exchange information and ideas. While many of this year's sessions still cover theoretical topics, there are now many sessions which present practical solutions already being deployed in the real world. Speakers from major electronics manufacturers will share their experiences in implementing environmentally friendly practices within the

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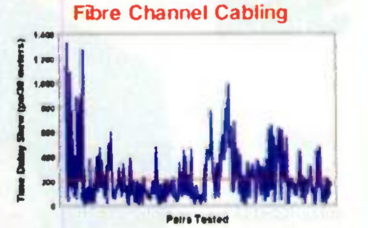

Other fibre channel cable designs create unacceptably high skew — the entire length must be inspected to find skew <200ps/30m.

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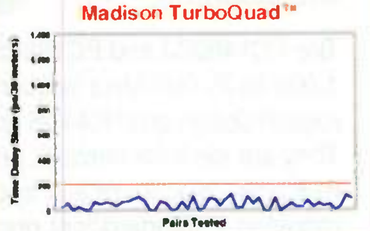

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highly competitive electronics industry.

The conference's first day features three half-day workshops. One will provide an overview of design-for-environment (DFE) tools. A second tutorial will provide an overview on tools available for pollution prevention and sustainability. The third half-day session examines the issues and technologies involved with recycling electronic products at the end of their useful life.

During the rest of the conference, designers will find an abundance of sessions that contain information they can apply directly to their work. In session six, "Design for the environment applications—Part 1," William Trumble and Jane Brydges of Nortel Corporation, Ottowa, Canada, will present their paper "Technical progress in printed wired assembly using Nortel's no-lead solder assembly process." In the same session, N. F. Nissen of the Fraunhofer Institute for Reliability and Microintegration, Berlin, Germany, will discuss his paper, "Evaluating environmental factors for prelayout board design."

On Tuesday and Wednesday, designers will be able to attend presentations on topics like "Materials selection for life-cycle design," presented by Julie Stuart and Renata Mealy of Ohio State University, Columbus, and "An expert system for ranking of DFE strategies," by a team from Delft University of Technology, Delft, The Netherlands.

Many manufacturers are already discovering that a product need not become a waste-disposal problem if some careful up-front planning is done during its design. In sessions 15 and 18, "End-of-life, parts 1 & 2" (Tuesday 8:30 to 10:30 a.m., and Wednesday 10:45 a.m. to 12:15 p.m.), participants will learn ways they can begin to design their own products for reuse or recyclability. Some of the more interesting papers to be presented at these sessions will include, "How product characteristics determine end-of-life strategies" and "Linking demanufacturing operations with product DFE initiatives."

With five years of serious work behind them, ISEE's sessions are now full of real-world examples of green engineering practices. Sessions 8 and 16, "Design-for-environment tools parts, 1 and 2" (Tuesday, 2:00 to 3:00 p.m., and Wednesday, 10:45 a.m. to 12:15 p.m.), will let participants see the latest modeling and decision-making software techniques. Session 14, "Design case studies," (Wednesday, 8:30 to 10:30 a.m.) will examine real-world design issues for many types of systems.

Technical managers responsible for implementing environmentally friendly policies and practices will also have a chance to look at some of the most important topics emerging today. Discussions of environmental stewardship (sessions 10 and 13), cradle-to-grave product management (session 12), and supplier management (session 7), will help concerned managers begin to evaluate their role in the DFE equation.

Both IEEE members and non-members are invited to attend this event. Contact the IEEE registrar at 455 Hoes Lane, Piscataway, NJ 08855-1331; (732) 562-3875, fax (732) 981-1203; www.ieee.org.

Lee Goldberg

Tiny Op Amp Targets Miniature Portable Electronics

An Advanced Submicron Silicon-Gate biCMOS Process Houses This General-Purpose Op Amp In A Flea-Size SC70 Package.

Ashok Bindra

COVER FEATURE

Like other electronic components, op amps also continue to get better in performance, smaller in size, and lower in price. This is all dictated by compact cellular handsets, pocket-size pagers, digital cameras, and other portable consumer electronics, which are constantly evolving to offer higher performance without cost penalties. Consequently, semiconductor vendors are constantly enhancing processes, refining architectures, and improving manufacturing.

To meet the stringent needs of these applications, National Semiconductor has redesigned the ubiquitous work horse of the industry, the LM324, which has served the requirements of analog designers for the last twenty five years. The result is a low-voltage, single-supply op amp, the LMV321, in a micro-miniature five-lead SC70-5 package.

Silicon Dust

The company calls it the "flea size" package and likens the tiny op amp's development to giving designers microminiature "silicon dust" components to work with. National Semiconductor claims that it is the smallest available package for a standard op amp *(see "Wait and See," p. 42)*. The LMV family is being aimed at compact portable electronics, where space and power consumption are key drivers, says Erroll Dietz, design manager for amplifiers at National Semiconductor's Analog Product Group based in Santa Clara, Calif.

To be sure, the SC70 is not a brand new package. Several logic devices are being offered in this package today. At dimensions of 2.0 by 2.1 by 1.0 mm, the SC70-5 is approximately half the footprint of the conventional SOT23-5 package. In fact, with these dimensions, the LMV321 approaches the size of the chip resistors and capacitors, as well as discrete transistors. As a result, this tiny package allows designers to insert the new op amp closer to the signal source in tight portable designs, thereby minimizing noise pick-up and improving signal integrity.

This miniaturization of the LMV family is made possible by National Semiconductor's advanced 0.8-µm silicon-gate biCMOS process that combines the speed of bipolar transistors with the low-power attributes of CMOS circuits *(Fig.1)*. And, all this is achieved without incurring higher cost. In fact, the reduction in the size of the op amp's die has enabled National Semiconductor to lower the cost of the LMV321 op amp by about 50% over comparable CMOS parts.

The sub-micron biCMOS process the op amp is made on has shrunk the LMV321's die size to 17 by 17 mils, allowing the company to place the chip in the micro-miniature SC70 package *(Fig.2)*. In order to fit the die in this package,the bond pads have also been reduced to 2.8 mils^2. The need for smaller bond pads has also pushed the wire-bonding technology employed, as well as stretched the wafer dicing process to new widths.

ESD Protection

Despite finer device geometry, the process incorporates a proprietary energy spreading technique that provides reasonable ESD protection for such a tiny op amp. An efficient en-

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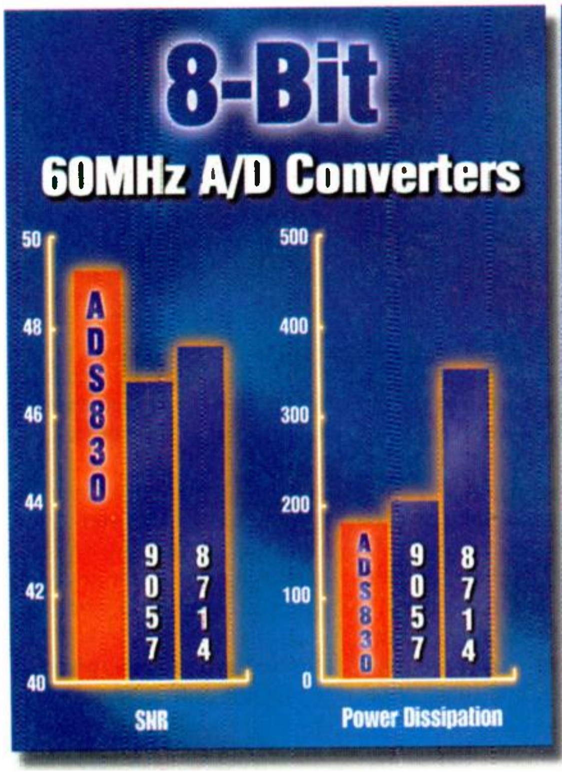

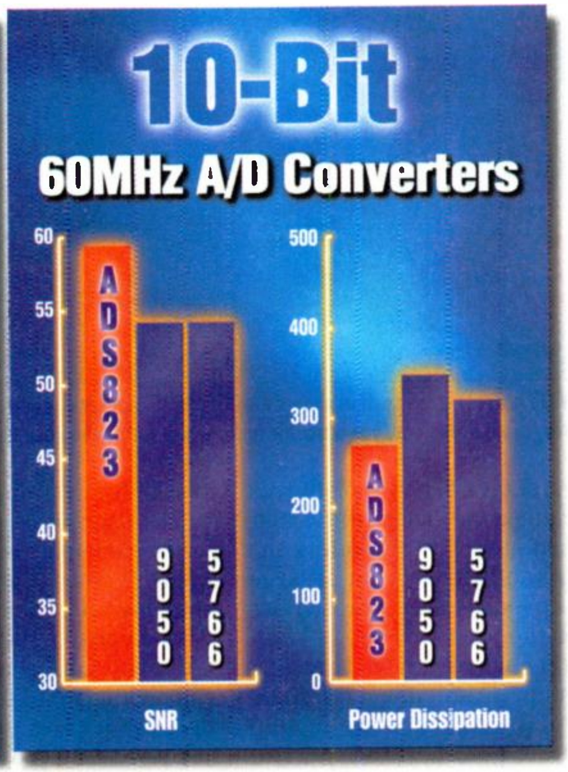

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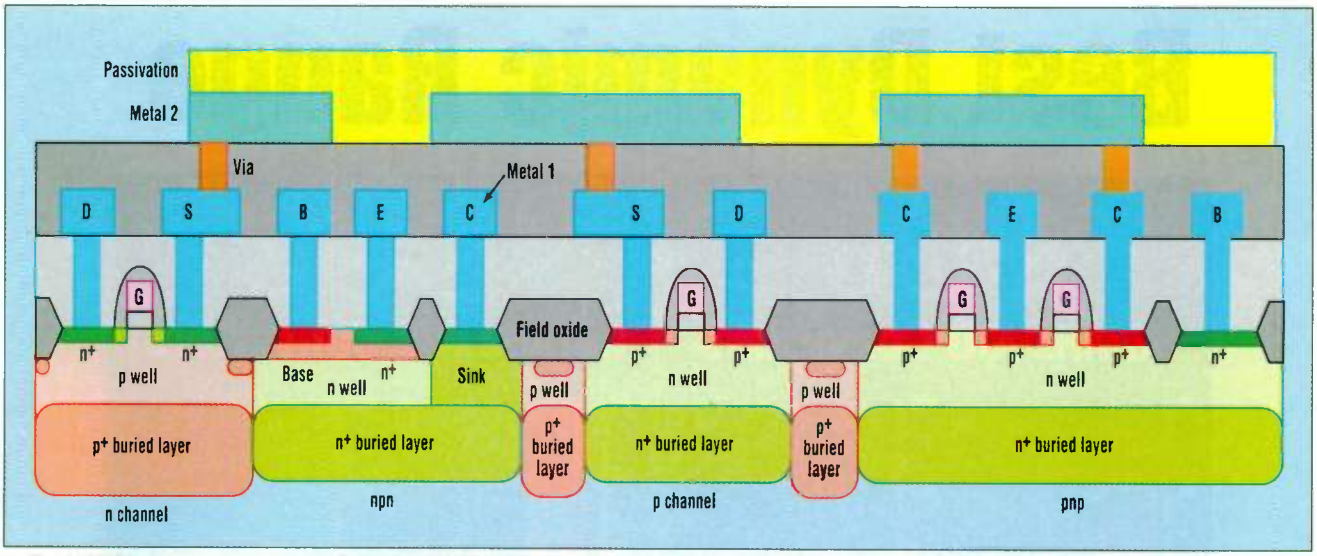

1. The biCMOS process cross section shows nMOS, pMOS, npn, and pnp transistors. The pnp transistors are basic lateral structures formed from pMOS source/drain diffusions. The parasitic gate, which forms the base on the lateral pnp transistors, is tied back to their source.

ergy dissipative transistor in this scheme clamps the electrostatic voltage to a safe level by spreading the heat energy efficiently over as large an area as possible. This approach also alleviates the problems due to localized heating, which can be damaging to aluminum interconnects. Consequently, under human body simulation, the LMV321 is rated to withstand 900 V, while the machine model indicates a tolerance of 100 V However, according to National Semiconductor, its designers have developed structures that pass over 2 kV of human body model discharges.

The finer process has also lowered the single-supply requirements of the LMV321 down to 2.7 V, thereby guaranteeing operation from 2.7 to 5.5 V. By comparison, the existing standard LM324 op amp operates over a supply voltage range of 5 to 32 V. In addition, the LMV321 provides rail-to-rail operation with no crossover distortion down to 2.7 V (*Fig.3*). The rail-to-rail output swing sets the dynamic range of the output, which is particularly important when the op amp is running on low supply voltages. Additionally, the amplifier offers a gain-bandwidth product of 1 MHz and a slew rate of 1 V/µs, while drawing typically only 130 µA of current under no-load conditions from a power-supply voltage of 5 V.

Redesigned Architecture

Besides an improved speed-power ratio, the biCMOS process has also allowed the manufacturer to implement matched input bipolar transistors to minimize input offset levels and errors, while reducing the 1/f noise. In fact, to realize well-matched transistors, the LMV321 uses pnp transistors

Wait And See

While National Semiconductor has taken the pioneering step in further shrinking the package size for general-purpose op amps, other major competitors in the analog world are not sitting idle. They are keenly watching the introduction of the popular single op amp in the tiny SC70 package, which approaches the size of chip resistors and capacitors. However, before they commit to such a miniaturized form, these semiconductor vendors want to see the response of the analog designers to the SC70-5.

Meanwhile, major players like Maxim Integrated Products, Linear Technology Corp., Analog Devices, Texas Instruments and Burr-Brown have opted for the SOT23 as a proven miniature package for their respective op amps. For instance, Maxim has released its single micropower op amp, the MAX4240, in a 5-pin SOT23-5. With beyond the rails input and rail-to-rail output capabilities, the MAX4240 operates from a single +1.8 V to +5.5 V or dual ±0.9 V to ±2.75 V supplies. It has an input common-mode range that is guaranteed to exced either rail by 200 mV , while the output typically swings within 9 mV of the rails with a 100-kΩ. load. Plus, this amplifier provides a 90-kHz gain-bandwidth product, and uses only 10 µA of supply current. In fact, this ultra-low power device is designed to operate from two AA cells.

Linear Technology is also suporting the SOT23 for its precision high-speed op amps. And, Burr-Brown has unveiled a single-supply, CMOS-based dual op amp, the OPA2337, in a SOT23-8. Accordong to Burr-Brown, the SOT23-8 offers a 75% smaller foot-print than the industry standard SO-8. The manufacturer has also developed a single op amp version in a 5-pin SOT23-5 package. The trend is toward the SOT23-5 for single op amps, says Burr-Brown's strategic marketing engineer Howard Skolnik. No matter how small it gets, it is going to get smaller with time, notes Skolnik.

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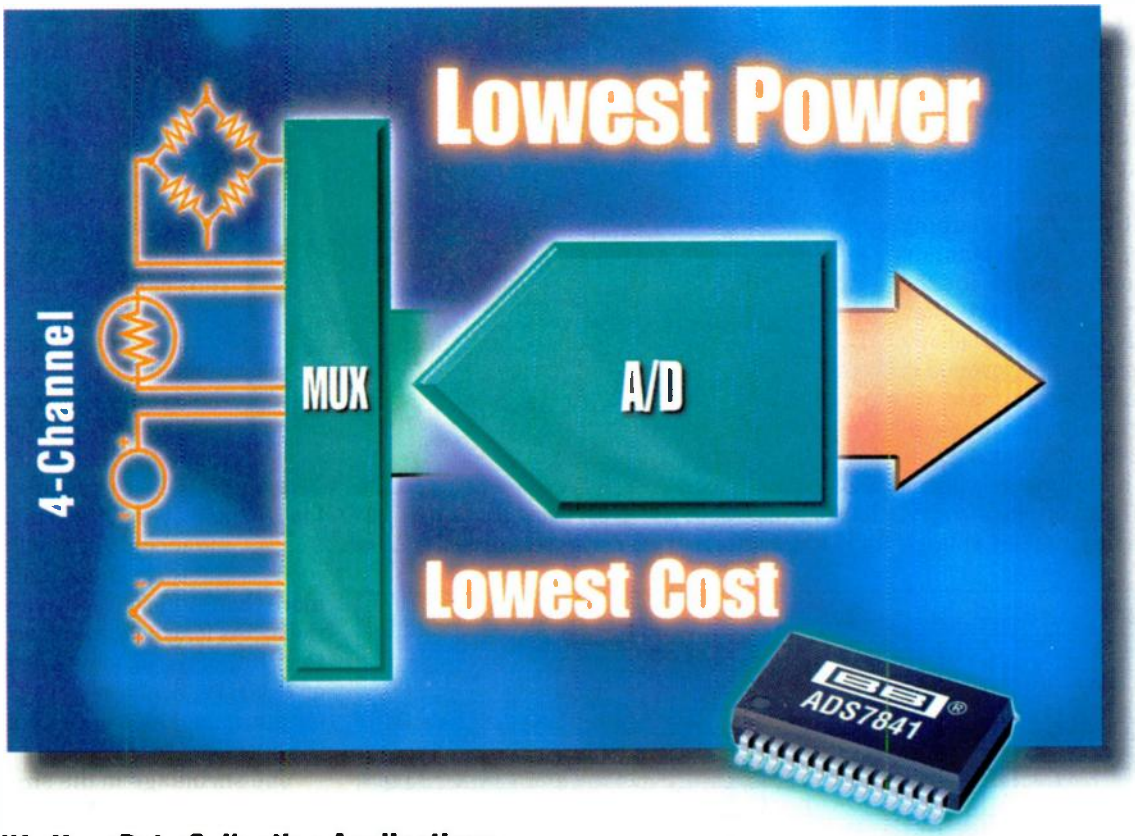

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Burr-Brown's family of 12- and 16-bit, 4-channel, A/D converters continues to grow and provide you with the best price/performance options available on the market. These converters feature an on-board multiplexer, and are complete with internal clock, S/H amplifier, and internal voltage reference. All offer low power, parallel and serial outputs, and a continuous conversion mode that allows you to sample sequentially through all four channels. Plus, the serial interface also provides a low-cost isolation solution for remote data acquisition. With conversion rates up to 200kHz and power dissipation under 15μW in shutdown mode, these products are ideal for battery operated systems such as personal digital assistants, portable data loggers, and measurement equipment.

ADS7841 Key Specifications:

- Single Supply: 2.7V to 5V
- 4-Channel Single-Ended or 2-Channel Differential Input
- Up to 200kHz Conversion Rate
- Serial Interface
- Alternate Source for MAX1247
- 16-Lead SSOP Package

Product	Resolution (Bits)	Channels	INL (LSB)	NMC*	Sample Rate (kHz)	Power (mW)	SINAD (dB)	Price (1kpcs)	FAX*LINE#* 1-800-548-6133	Reader Service #
ADS7824	12	4	±0.5	12	40	50	73	$12.30	11303	87
ADS7825	16	4	2	16	40	50	86	$28.46	11304	88
ADS7832	12	4	±0.75	12	117	14	71	$16.00	11332	89
ADS7841	12	4	±1	12	200	3	72	$4.59	11420	90

**No Missing Codes*

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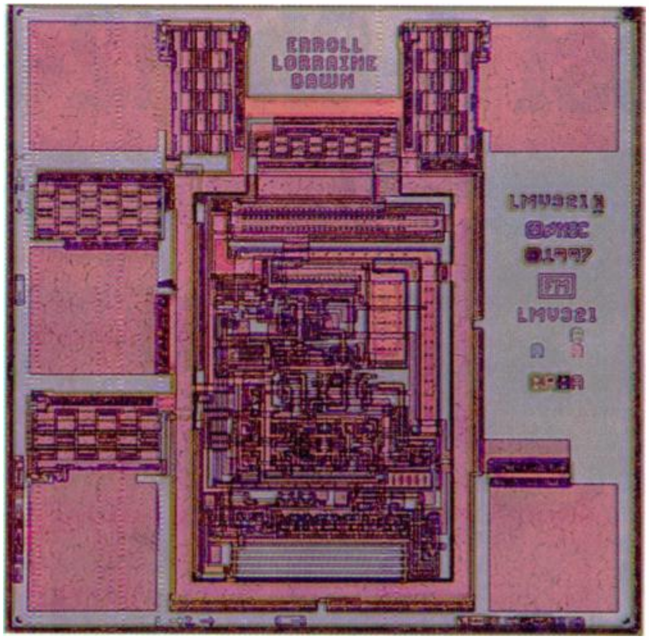
BURR - BROWN®

Burr-Brown Corporation • P.O. Box 11400 • Tucson, AZ • 85734-1400 • Call (800) 548-6132 or use FAX*LINE* (800) 548-6133 • http://www.burr-brown.com/

Distributors: Arrow: (800) 777-2776 • Digi-Key Corp: (800) 338-4105 • Insight Electronics: (888) 488-4133 • J.I.T. Supply: (800) 246-9000 • Sager Electronics: (800) 724-3780 • SEMAD (Canada): (800) 567-3623 instead of pMOS transistors (*Fig.4*). Furthermore to retain the ac and dc characteristics of the popular LM324 all the way down to 0 2.7 V, the LMV321 implements a differential folded cascode circuit at the input.This allows the designer to operate at lower voltages with a very wide input common-mode voltage range, notes Dietz. Typically, at a 2.7-V supply voltage, the input common-mode voltage range for the new part is -0.2 to +1.9 V. Consequently, the LMV321 allows direct sensing near ground in single-supply operation.

Other key features of LMV321 op amp at a 2.7-V supply include a maximum input offset voltage of 7 mV, average input offset voltage drift of 5 µV/°C, typical input offset current of 2 nA, a common-mode rejection ratio (CMRR) of 63 dB, and a power-supply rejection ratio of 60 dB.

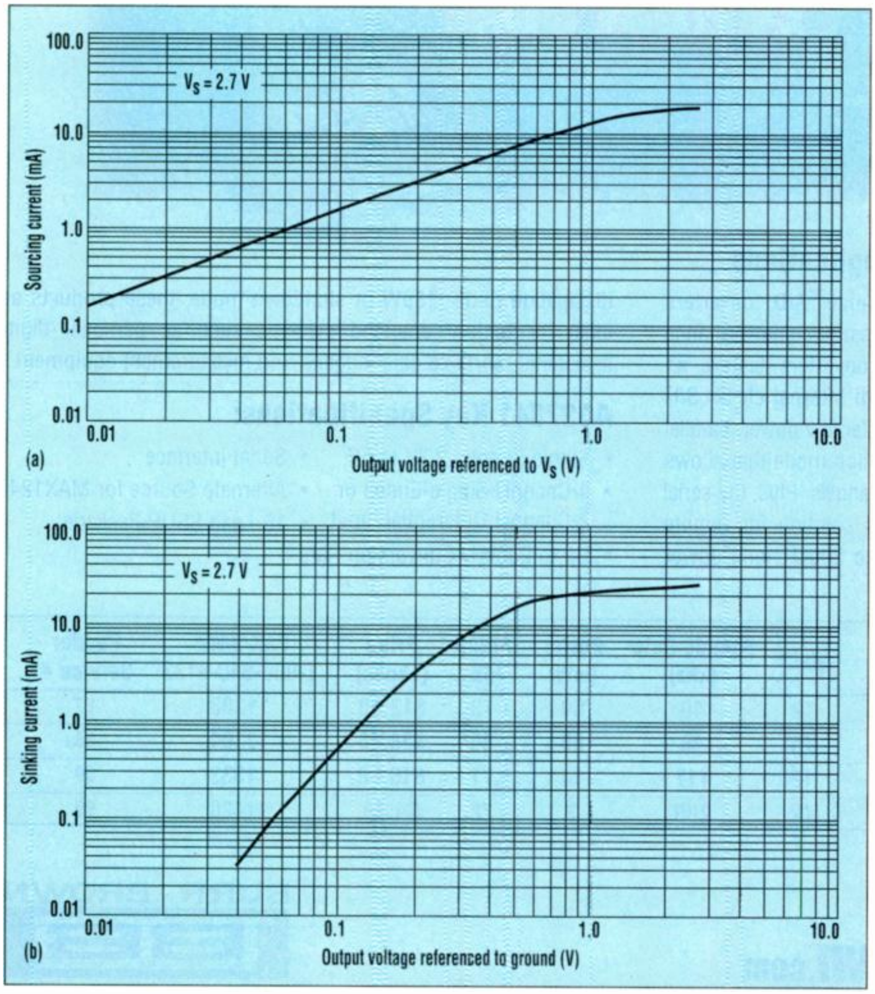


2. The 0.8-µm biCMOS process has shrunk the die of the LMV321 to 17 by 17 mils. And the bond pad size has beeen redued to 2.8 mils^2.

The typical input bias current of the new op amp is 15 nA at a 5-V supply and 11 nA at 2.7 V. Thus a 100-kΩ resistor will cause 1.1 mV of error voltage at a 2.7-V supply. However, this error due to the amplifier's input bias current can be reduced by balancing the resistor values at both the inverting and non-inverting inputs, according to the op amp's manufacturer.

While the open-loop gain of the redesigned op amp is only 15,000 in the sinking mode and over 100,000 in the sourcing mode, National Semiconductor's Dietz believes it is more than sufficient for many applications. "As long as the gain error is less than 10% of the offset voltage, the gain of 15,000 is adequate" says Dietz. The output impedance of the amplifier in the open-loop mode is 500 Ω

The shrinkage in die size has also permitted National Semiconductor to produce dual and quad versions of the single LMV321 in comparatively smaller packages. While the dual LMV358 comes in an 8-lead mini SOIC package, the quad LMV324 is housed in a 14-pin TSSOP. Both, the dual and quad versions provide true single-supply operation and retain the ac and dc characteristics of the LMV family.



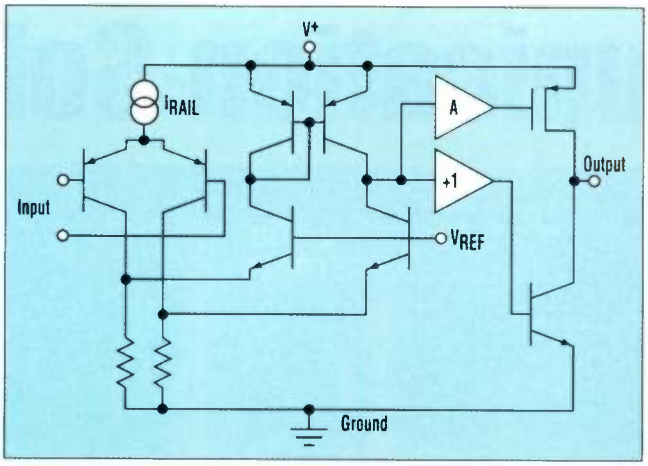
3. The National Semiconductor tiny op amp offers high source (a) and sink (b) currents at low voltages to permit a rail-to-rail swing at the output.

Challenging Issues

Although, the SC70 package looks attractive, it also poses many challenges to the analog designer Key among them are thermal issues, mechanical reliability, and parasitic influences. The smaller package presents higher thermal resistance. Consequently, the thermal resistance (θ_{jA}) of the SC70-5 package is 440°C/W. Such a high value warrants proper thermal design, ensuring that the part is not overheated and operates within the specified temperature range. The thermal resistance drops significantly as the package size increases. For example, the thermal resistance offered by the 8-pin miniSOIC package is

235°C/W, and the 14-pin TSSOP package presents 155°C/W.

While the part is compatible with existing pick-and-place machinery, its mechanical reliability requires assurance. Toward that end, National Semiconductor has subjected the LMV321 to thermal cycling and other life tests. According to National Semiconductor, the LMV321 in an SC70-5 package passed without any rejects when subjected to 1000 temperature cycles from -65 to +150°C. This test evaluates the device's ability to withstand both the extremes of rated temperatures, as well as rapid changes in temperature.



4. To achieve well matched transistors at the input, the op amp uses PNPs instead of pMOS transistors. While the output is a combination of pMOS and npn to obtain higher output current.

Additionally, the LMV321 also underwent humidity and parametric stability tests, and emerged without any failures,asserts the manufacturer. To determine the tolerance to humidity, the package is subjected to moisture resistance test of Method 1004. In this test, which is considered destructive, the package is subjected to 10 cycles, during which the temperature is varied from 25°C to 65 °C at a relative humidity of 90% when the temperature is stabilized. Each cycle is for a duration of 24 hours. During this test, the part is tested electrically for degradation, and examined visually for any damage. The parametric stability test indicates the op amp"s ability to perform consistently over time. This capability is analyzed via burn-in. Since parasitic effects are critical with such a small size, the signal traces must be routed in a manner that minimizes ac and dc parasitic effects on the input of the amplifier.

Price And Availability

The LMV321/358/324 op amps are in production and are available now. The single op amp LMV321 in an SC70-5 package is priced at 27 cents. Likewise, the dual version LMV358 in an 8-pin miniSOIC package is priced at 27 cents, and the quad LMV324 version in a 14-pin TSSOP package is priced at 30 cents. All prices are for 1000-piece quantities.

National Semiconductor Corp., 2900 Semiconductor Dr., Santa Clara, Calif. 95052-8090. Telephone 1-800 272-9959 or visit their web site at www.national.com

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- 250 - 1500 Watts
- 1 - 7 Outputs
- AC and DC Inputs
- Competitive Prices

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POWER PRODUCTS

WRH

M ▪ DM ▪ VX SERIES MODUFLEX® SWITCHERS

DESCRIPTION

Moduflex® Series form a comprehensive line of open frame power supplies assembled from standard "off the shelf" modules. The design features "State of the Art" topology, a meticulous thermal structure and the use of high efficiency circuits and components to attain the desired power density. The modular system concept reduces manufacturing to submodule assembly, capable of high volume production with a superior quality level at moderate costs.

M Series are available in output power ratings from 250-750 watts. **DM Series** are available with a 48VDC input and output power ratings of 400 and 600 watts. **VX Series** units consist of four specialty units with output power ratings of 500, 750, 1000 and 1500 watts having the VXI standard voltages and currents.

Three classes of output modules are available. The **STANDARD** outputs allow short duration surge currents on all auxiliaries for hard starting loads. Optional **CURRENT LIMITED** outputs have square current limiting and feature wireless droop current sharing. Optional **ENHANCED** outputs have square current limiting, one wire star point current share, output good logic signal with LED, nominal 5V local bias, individual inhibit and margining. For requirements that cannot provide minimum load on the main output, the **ZERO PRELOAD** option is available for main outputs up to 500 watts.

DELIVERY

Choose stocked units or construct a model number using stocked modules for fast delivery. Otherwise, form a model from the adjacent page to meet your specific requirements. Contact factory for deliveries on models derived from non-stocked modules.

FEATURES

- UL, CSA, TÜV (IEC, EN), CE.
- 6 watts per cubic inch.
- 1-7 outputs, 250-1500 watts.
- AC & DC input models.
- VXI rated specialty models.
- 120 kilohertz MOSFET design.
- All outputs:
  - *Adjustable*
  - *Fully regulated*
  - *Floating*
  - *Overload and short circuit protected*
  - *Overvoltage protected*
- Standard features include:
  - *System inhibit*
  - *Load proportional DC fan output*
- Options include:
  - *Auto ranger*
  - *VME/VXI Monitor*
  - *End fan cover*
  - *Top fan cover*
  - *Current Limited Outputs*
  - *Enhanced Outputs*
  - *Zero Preload*
- Fast delivery.
- Replaces expensive high density systems using potted modules.

STOCKED MODELS - Available in 3 days.

Max Power	Output 1	Output 2	Output 3	Output 4	Model*
425W	5V @ 50A	12V @ 12A	5V @ 10A	12V @ 6A	M44R2323-47P
425W	5V @ 50A	24V @ 6A	12V @ 6A	12V @ 6A	M44R2633-47P
600W	5V @ 60A	12V @ 12A	12V @ 12A	5V @ 10A	M46C2332-47P
600W	5V @ 60A	12V @ 12A	24V @ 6A	12V @ 6A	M46C2363-47P

**Models shown in table include power fail monitor, auto ranger, current limited modules, zero preload and end fan cover options. 600W models Case #3.*

UNITS FROM STOCKED MODULES - Available in 2 weeks.

M 44 B 2 3 3 6 - YY X

- M — Series
- 44 — Configuration
- B — Power Code
- 2 — Output #1 Code
- 3 — Output #2 Code
- 3 — Output #3 Code
- 6 — Output #4 Code
- YY — Sum of Option Codes
- X — Output #1 Variant

Configuration: Allowable quad output configurations are 42, 44, 46 and 48.
Power Code: Choose Power Code P, R, A through D for 250-750W models.
Output Codes: Select any outputs from the shaded area on the Output Types table consistent with the configuration chosen.
Option Code: Specify Option Code. Refer to the Option table. Codes 02 (redundancy) and 16 (enhanced) are excluded from models available in 2 weeks.

OPTIONS

Option Code	Function
00	None
01	Power Fail Monitor
02	Auto Ranger
04	Current Limited
08	Zero Preload
16	Enhanced
32	End Fan Cover*
64	Top Fan Cover

*Replace the YY with the sum of the option codes. *600 & 750 watt units require Case 5.*

MODEL SELECTION

Models are available in power ratings of 250 to 1500 watts, with corresponding code letters P, R and A through D. See Power Code chart. Contact factory for 1000 and 1500 watt models.

Output modules are available in six types—J, K, L, M, N and P in nominal power outputs from 75-500 watts. Type M, N and P modules are variable power rated depending upon the unit power rating. The M, N and P Module table directly below shows the corresponding multiplier applicable to the output current ratings of the M modules and allowable power ratings for the N and P modules. For example, a 750 watt multiple will have its M type module configured to produce 120A @ 5V or 12A @ 48V. The voltage and current rating of output modules are listed in the table of output types. This table assigns an alpha-numeric code designating the nominal voltage rating of the module.

Power Code	Unit Power Rating	M Module Current Multipliers Single Output	M Module Current Multipliers Multiple Output	N/P Module* Allowable Power Ratings
P	250W	0.5	0.3	175W
R	425W	0.85	0.5	250W
A	400W	0.8	0.6	250W
B	500W	1.0	0.8	300W
C	600W	1.2	1.0	400W
D	750W	1.5	1.2	500W

**When an N or P module is used as the main output, the allowable power and the module current ratings must not be exceeded.*

Output Types*

Output Code	Output Volts	J Amps	K Amps	L Amps	M Amps	N/P Amps
0	2	10	20	30	100	60
1	3.3	10	20	30	100	60
2	5	10	20	30	100	60
3	12	6	12	24	42	42
4	15	5	10	20	33	33
5	18	4	8	16	28	28
6	24	3	6	12	21	21
7	28	2.5	5	10	18	18
8	36	2	4	8	14	14
9	48	1.5	3	6	10	10
A	2.2	10	20	30	100	60
B	2.4	10	20	30	100	60
C	2.7	10	20	30	100	60
D	3	10	20	30	100	60
E	3.6	10	20	30	100	60
F	4	10	20	30	100	60
G	4.5	10	20	30	100	60
H	5.7	10	20	30	90	60
J	6.3	10	20	30	80	60
K	7	9	18	30	70	60
L	8	8	16	30	62	60
M	9	8	15	30	56	56
N	10	7	14	30	50	50
P	11	7	13	27	45	45
Q	13.5	6	11	22	37	37
R	17	5	9	18	30	30
S	19	4	8	16	26	26
T	21	4	7	14	24	24
U	23	4	7	13	22	22
V	26	3	6	12	19	19
W	29	3	5	10	17	17
X	32	2	5	9	16	16
Y	40	2	4	8	13	13
Z	44	2	4	7	12	12

*Multiple output modules of a given type are arranged in ascending order by voltage magnitude in the same sense as the output number sequence in the configuration diagrams. *Shaded ratings are stock.*

HOW TO ORDER

To form the proper model number defining a custom requirement, select the letters M or DM to designate the series, then choose the desired configuration of output modules and list the configuration code. Insert the power code letter for the power level and follow with the output code numbers or letters for each specific output. Enter a dash and from the option table insert the sum of the option codes. Where lower power is desired for the main module, an N module can be substituted and is denoted by a letter N in the output variant position. In addition, when no preload is available for the main output, choose Option Code 08 and add a P in the output variant position. For an **enhanced** main and **current limited** auxiliaries, specify both 04 and 16 option codes.

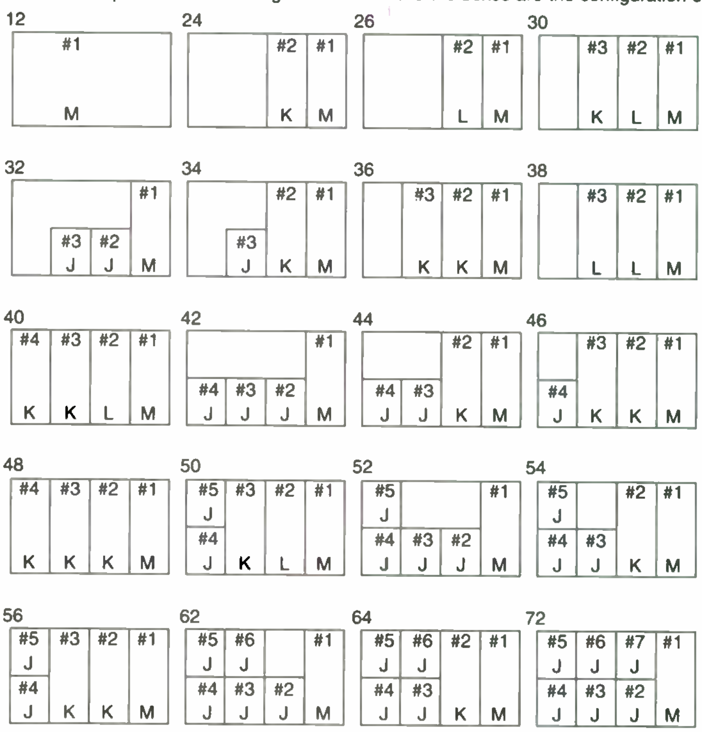
MODUFLEX 400W QUAD SWITCHER

D M 44 A 2 3 3 6 - YY X

- D — DC Input
- M — Series
- 44 — Configuration
- A — Power Code
- 2 — Output #1 Code
- 3 — Output #2 Code
- 3 — Output #3 Code
- 6 — Output #4 Code
- YY — Sum of Option Codes
- X — Output #1 Variant

OUTPUT CONFIGURATIONS

The boxes below are diagrammatic representations of the power supplies as viewed from the output end. The two-digit numbers above the boxes are the configuration codes.



Refer to the table below for allowable configurations by series.

Output Configuration	250W	400W	425W	500W	600W	750W
12	x	• x	x	x	• x	x
24	x	• x	x	x	• x	x
26					• x	x
30					• x	x
32	x	• x	x	x	• x	x
34	x	• x	x	x	• x	x
36		• x	x	x	• x	x
38					• x	x
40						x
42	x	• x	x	x	• x	x
44		• x	x	x	• x	x
46		• x		x	• x	x
48		• x			• x	x
50						x
52		• x	x	x	• x	x
54		• x		x	• x	x
56		• x			• x	x
62		• x		x	• x	x
64		• x			• x	x
72		• x			• x	x

• Represents allowable configurations for the DM Series.
x Represents allowable configurations for the M Series.

SPECIFICATIONS

INPUT
90-132 VAC or 180-264 VAC, 47-63 Hz. Strappable. 40-60 VDC for DM Series.

EMISSIONS
FCC 20780 Part 15/EN 55022, Class A Conducted. EN 61000-3-3, Voltage Fluctuations.

IMMUNITY
IEC 1000-4-2/EN 61000-4-2, Electrostatic Discharge. IEC 1000-4-3/EN 61000-4-3, Radiated Field. IEC 1000-4-4/EN 61000-4-4, Electrical Fast Transients. IEC 1000-4-5/EN 61000-4-5, Level 3 Surge. IEC 1000-4-6/EN 61000-4-6, Conducted Field.

INPUT SURGE
34 amps peak from cold start for units under 400 watts, 68 amps for other models.

EFFICIENCY
75% typical.

HOLDUP TIME
20 milliseconds after loss of nominal AC power. 3 milliseconds for DM Series.

OUTPUTS
See model selection table. Outputs are trim adjustable ±5%.

OUTPUT POLARITY
All outputs are floating from chassis and each other and can be referenced to each other or ground as required.

LINE REGULATION
Less than ±0.1% or ±5mV for input changes from nominal to min. or max. rated values.

LOAD REGULATION
±0.2% or ±10mV for load changes from 50% to 0% or 100% of max. rated values.

MINIMUM LOAD
Main output requires a 10% minimum load for full output from auxiliaries. Use Option 08 if no minimum load is available for mains up to 500 watts. Singles require no minimum load.

RIPPLE & NOISE
1% or 100 mV, pk.-pk., 20 MHz bandwidth.

OPERATING TEMPERATURE
0-70°C. Derate 2.5%/°C above 50°C.

COOLING
A min. of 6 LFS* for models under 400 watts, 10 LFS for others, directed over the unit for full rating. Two test locations on chassis rated for max. temperature of 90°C. For convection ratings consult factory.
*Linear feet/second.

TEMPERATURE COEFFICIENT
±0.02%/°C.

DYNAMIC RESPONSE
Peak transient less than ±2% or ±200 mV for step load change from 75% to 50% or 100% max. ratings.

RECOVERY TIME
Recovery within 1%. Main output - 200 microseconds. Auxiliary outputs - 500 microseconds.

SAFETY
Units meet UL 1950, CSA 22.2 No. 950, EN 60 950, IEC 950.

ISOLATION
Conforms to safety agency standards.

INPUT UNDERVOLTAGE
Protects against damage for undervoltage operation.

SOFT START
Units have soft start feature to protect critical components.

OVERVOLTAGE PROTECTION
Standard on all outputs. VX Series - standard on main output.

REVERSE VOLTAGE PROTECTION
All outputs are protected up to load ratings.

OVERLOAD & SHORT CIRCUIT
Outputs protected by duty cycle current foldback circuit with automatic recovery. Standard auxiliaries have additional backup fuse protection. Options 04 and 16 have square current limiting with automatic recovery when overload is removed.

THERMAL SHUTDOWN
Circuit cuts off supply in case of local over temperature. Units reset automatically when temperature returns to normal.

FAN OUTPUT
Nominal 12 VDC @ 12 watts maximum.

INHIBIT
TTL compatible system inhibit provided. Option 16 has individual output inhibit.

REMOTE SENSING
On all outputs except standard and 04 Option outputs 75 watts or less.

SHOCK & VIBRATION
Shock per MIL-STD 810-E Method 516.4, Procedure I. Vibration per MIL-STD 810-E Method 514.4, Category 1, Procedure I.

MECHANICAL

CASE	WATTS	H	x	W	x	L	
1	250W/425W	2.50"	x	4.15"	x	8.00"	
2	400W/500W	2.50"	x	5.05"	x	9.00"	
3	600W/750W	2.50"	x	5.20"	x	9.63"	
4	600W/750W	2.50"	x	6.50"	x	9.63"	Config. 40 & 50 only.
5	600W/750W	2.50"	x	6.00"	x	9.63"	Option 32 only.
6	1000W	5.00"	x	5.05"	x	10.40"	
7	1500W	5.00"	x	5.20"	x	11.00"	

OPTIONS

POWER FAIL MONITOR
Optional circuit provides isolated TTL and VME/VXI compatible ACFAIL signal providing 4 milliseconds warning before main output drops by 5% after an input failure. A SYSRESET signal following VME timing requirements is provided when an N module is used as a main output. Both logic signal outputs can sink current per the VME specification.

AUTO RANGER
Optional circuit provides automatic operation at specified input ranges without strapping. Not applicable to DM Series.

CURRENT LIMIT
Option provides on all outputs:
- Square current limit with auto recovery.
- Wireless droop current share for parallel or N+1 redundant operation.

ZERO PRELOAD
Optional circuit removes need for preload on main output. Available for mains up to 500 watts.

ENHANCED
Option provides on all outputs:
- Square current limit with auto recovery.
- Single wire active current share for parallel or N+1 redundant operation.
- DC output good logic signal with LED indicator.
- Logic inhibit.
- Nominal 5V bias.
- Margining.

END FAN COVER
Optional cover with brushless DC ball bearing end fan which provides the required air flow for full rating.

TOP FAN COVER
Same as above with fan mounted on top of the power supply.

Specifications subject to change without notice.

Deltron inc.
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Commodity ADCs Pile More Functions On-Chip For Less

Combining Innovative Circuits With Submicron Processes, Analog IC Suppliers Are Driving 16-bit Converters Down To $5.

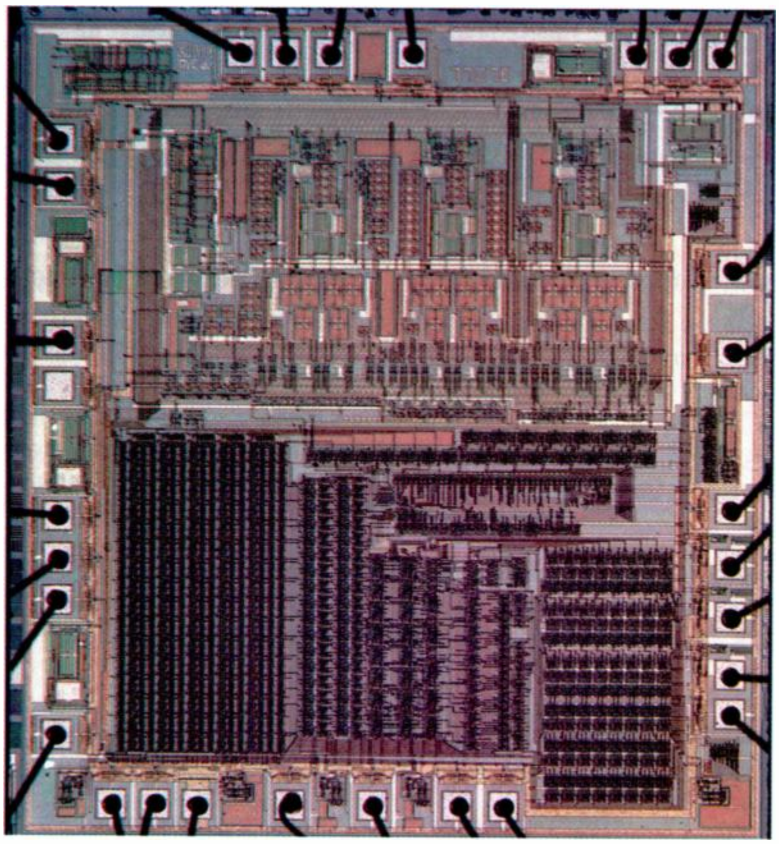
Ashok Bindra

SPECIAL REPORT

With the widespread proliferation of microcontrollers and digital signal processors (DSPs) in price-sensitive consumer, industrial, and communications applications, engineers demand more from general-purpose analog-to-digital converters (ADCs). In fact, more for less is becoming the norm of the day. Designers ask for better resolution, faster sampling, multiple channels, simpler interfaces, lower power, and smaller packages. And, of course, at an affordable price.

Meanwhile, mixed-signal semiconductor manufacturers continue to advance their processes and tweak their manufacturing procedures to balance the right combination of features to satisfy user needs as best as they can. Consequently, in last few years, ADCs have seen significant gains in performance as their prices have eroded, propelling converters with over 12-bit resolution to commodity status.

This erosion in ADC prices has prompted designers to move up the resolution ladder, as they begin to improve their designs with 10-, 12-bit, and higher-resolution ADCs. In fact, some are now eyeing 14- and 16-bit converters, as these devices begin to emerge with competitive pricing.



Art Courtesy: Maxim Integrated Products

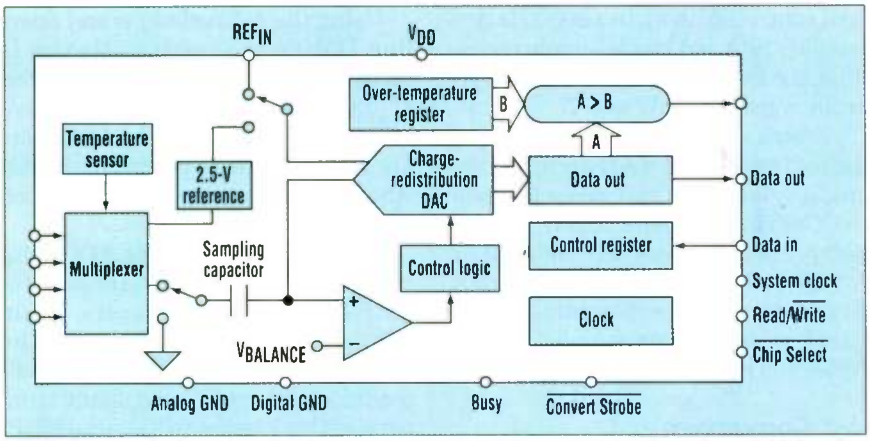
As processes advance, semiconductor suppliers integrate more functions and seamless interfaces on-chip, around the converter without incurring cost. At the same time, they drive the supply rail to lower voltages to cut power consumption. In fact, analog system designers are shying away from split supplies, instead turning to single-supply designs. The emergence of highly integrate[d] optimized single-supply 10-, 12-bit, and highe[r] resolution single-chip ADCs is making the desig[n]ers' tasks much easier. This trend enables them [to] further lower system cost by significantly redu[c]ing the overall system component count.

On-Chip Temperature Sensor

Recent introductions reflecting this change a[re] Analog Devices' two new families of 10-bit ADCs. The AD741x and AD781x are based on a successive-approximation-register (SAR) architecture and a 0.6-µm CMOS (*Fig.1*). Besides offering special interfaces for easy linking with standard microcontrollers, these ADCs also come with an on-chip bandgap temperature sensor.

Aimed at thermal management applications ranging from PCs to automobiles, the on-chip temperature sensor allows accurate measurement of th[e] ambient temperatu[re.] Analog Devices say[s] the device offers an accuracy within ±2°C over a wide temperature range of -55°C to +125°C. The accuracy is attributed to a novel circuit employing two transistors that convert temperature changes into precise voltage readings.

Plus, it contains an over-temperature interrupt pin and an on-chip digital register, enabling the user to program a set point. As a result, an alarm function can be incorporated into the design. The alarm is activated when the temperature exceeds the selected value. This condition is determined by comparing



1. This functional schematic of Analog Devices' AD7817 shows a 10-bit, four-channel ADC with an on-chip temperature sensor, a 2.5-V reference, and a flexible serial interface that's compliant with most microcontrollers. The single-supply operation range is 2.7 to 5.5 V.

the on-chip over-temperature register with the ADC code for the sensor.

While the maximum time for converting a temperature reading into digital code is 20 µs, the SAR-based device takes only 10 µs to convert an analog signal into a digital representation. While 741x members come with an I^{2}C-compatible serial bus interface, AD781x models implement an on-chip serial peripheral interface (SPI) that's compatible with other interfaces such as the queued SPI (QSPI) and Micro-Wire.

These converters are also designed for low-voltage, battery-powered portable applications, where low power consumption is a key requirement. Both the AD741x and AD781x families operate from a single 2.7- to 5.5-V supply, and come with an on-chip voltage reference of 2.5 V ±1%. Further power conservation techniques include automatic Power-Down and Sleep modes. For instance, the automatic Power-Down enables AD781x members to consume only 60 µW at a throughput of 1 ksamples/s. And, in the Shut-Down mode, the ADCs typically consume only about 2 µW.

Analog Devices' Mike Britchfield, marketing manager for general-purpose converters, calls the 741x and 781x ADCs "complete digital-temperature-sensor and thermal-monitoring systems on a single chip." On the horizon, he adds, are 1.8-V versions. These are driven by battery-powered applications, where the desire for cutting power consumption never fades.

Several packaging options are available for the devices. For example, the AD7817 and AD7417 are encased in narrow-body, 16-pin SOIC, as well as TSSOP packages. The other family members come in standard 8-pin SOIC and micro SOIC packages. In quantities of 1000, the AD7416 and AD7816 are each priced at $1.25. Likewise, AD7417 and AD7817 ADCs cost $3.50, and AD7418/7818 each carry a price tag of $2.75 each, all in 1000-piece quantities.

Integrating transducers with ADCs on-chip, however, was pioneered by National Semiconductor, with the release of their LM75. The LM75 is a temperature sensor with an on-chip 9-bit ADC, an I^{2}C interface, a comparator, and a MOSFET, and is priced at $1.40 each in 1000-unit lots. Since then, National has expanded its temperature-sensing portfolio to address the diagnostic needs of microprocessor-based systems. The latest addition is the LM80, a system-monitoring device that checks temperature, voltage and fan speed.

Integrated ADCs

Another proponent of the SAR architecture met with a fine-line CMOS process for low-cost ADCs is Texas Instruments (TI). Employing this strategy, TI is pushing the performance envelope of 10-bit parts in smaller packages and lower voltages, with on-chip digital trimming and a variety of flexible interfaces.

The company's new 10-bit ADC chip, the TLV1572, is designed to work with its 16-bit fixed-point TMS320C2XX DSP family. This part

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is tailored to provide a glueless serial interface to DSPs with minimum interference, says Tony Chang, senior systems engineer at TI. It gives the user both dc and ac specifications at lower voltages, he adds. Also, he continues, the TLV1572's operation from 2.7 to 5.5 V makes it suitable for both 3- and 5-V systems.

Like the others, the TLV1572 also has an automatic Power-Down mode to conserve power even further. It provides high-speed serial conversions at 1.25 Msamples/s for DSPs in motor control, mass storage, and automotive applications.

To utilize such a device efficiently, the user must implement proper circuit layout, says Tom Lahutsky, new product development manager for data converters at TI. He adds, "It is important to return digital current to digital ground and analog current to analog ground to reduce overall system noise." Concurrently, Lahutsky says, TI is expanding this product portfolio with a variety of speed options to give designers a choice of selecting the right combination of resolution and speed for their applications. A 10-bit parallel ADC, the TLV1562, is also in development, according to the manufacturer. The TLV1572 is housed in an 8-pin SOIC, and carries a price tag of $4.20 each in lots of 1000.

Burr-Brown, Exar, and Sipex also are breaking new ground in performance. Recently, Burr-Brown released a family of 10-bit, 40- to 70-MHz sampling ADC ICs with several user-friendly options on-chip. Targeting medical imaging, communications, and video digitizing, the pipelined CMOS ADS822/823/824 family offers options like an internal/external reference, a flexible input range of 2 or 1 V p-p, and either a single-ended or differential input for additional spurious performance. And, it operates from a single 5-V supply. Furthermore, it employs digital error correction to provide excellent differential linearity for demanding imaging applications. Housed in a 28-lead SSOP, it starts at $6.80 each in 1000-unit lots.

For battery operated systems like PDAs, data loggers, and data-acquisition systems, Burr-Brown has crafted four-channel 12-bit sampling ADCs. These devices feature on-chip multiplexers and serial/parallel interfaces and control. With up to a 200-kHz conversion rate and single supply operation, the new ADS7841/7842 units typically consume 2 mW at 5 V.

Exar's engineers are exploiting a time-interleaved SAR architecture and a 0.6-µm CMOS process for their ADCs. This technique allows them to integrate system-level 10-bit solution with a 40-Msample/s conversion rate. It also offers improvements in dynamic performance to serve applications in video and medical ultrasound imaging.

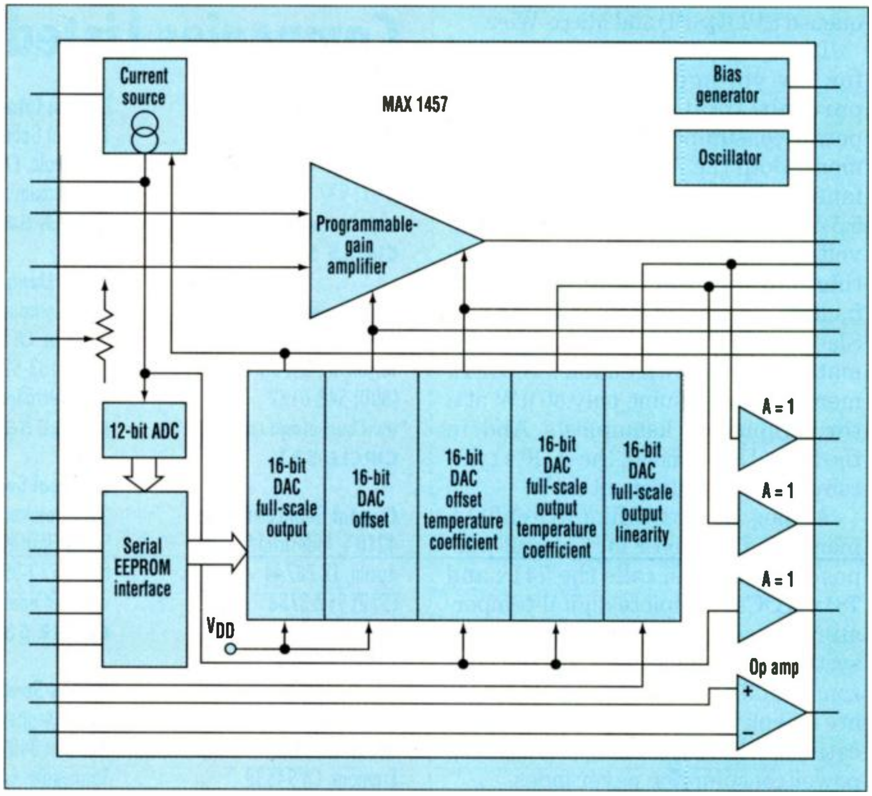
Δ-Σ Converters

While many firms are exploiting the benefits of SAR architectures and CMOS processes, Maxim Integrated Products and Crystal Semiconductor Products, a Division of Cirrus Logic, are pushing higher-resolution converters, based on a Δ-Σ architecture, to new low-price points. Only a few years ago, 16-bit and beyond resolution Δ-Σ ADCs would have been classified as specialized converters for high-end use. As a result, they were priced much higher. That scenario is rapidly changing. Today, these companies are touting parts under $5, in volume production.

Using the Δ-Σ technique and finer-line CMOS processing, Maxim is readying a family of highly integrated 12- and 16-bit ADCs optimized for sensor applications. The MAX1400 units are expected to be priced under $5, when they go into volume production next quarter.

In the works is a 12-bit ADC solution, the MAX1457. Aimed at piezoresistive pressure transducers, strain gauges, and accelerometers, the MAX1457 combines front-end signal-conditioning circuitry and digital trimming with a 12-bit ADC, a serial EEPROM interface, and an uncommitted op amp on the same chip. This design simplifies the job of calibrating and correcting the sensor's output signals (*Fig.2*). According to Maxim, the MAX1457 is tailored to provide an accurate ratiometric output with a minimum number of external components.

To achieve an accuracy within 0.1% of a sensor's repeatable errors, the MAX1457 incorporates 16-bit digital trimming. This method compensates for temperature errors by adjusting the offset, the full-scale output, the offset temperature coefficient, the full-scale out-



2. Maxim's MAX1457 is a 12-bit, Δ-Σ ADC optimized for digitizing sensor signals accurately. It uses five 16-bit DACs for digital trimming and compensating temperature errors. The calibration and compensation coefficients are stored in an external EEPROM.

put temperature coefficient, and the full-scale output nonlinearity of silicon sensors. Maxim says that the on-chip op amp can be used to increase the overall circuit gain, facilitating the implementation of a two-wire, 4 to 20 mA transmitter. The device accepts sensor outputs from 5 mV/V to 30 mV/V. The on-board serial interface is compatible with the Micro-Wire interface, and links directly to an external EEPROM. All calibration and compensation coefficients are stored in the external EEPROM.

The MAX1457 integrates three traditional sensor manufacturing operations into one automated process, thereby simplifying the development and manufacture of sensor products, says Ali J. Rastegar, Maxim's director of IC development. For example, he adds, prior to this development, the user had to first pretest the transducer, then perform calibration and compensation steps separately. And, finally, it must be retested again for data verification. The MAX1457 automates the calibration and compensation process to save the designer time and money, notes Rastegar. "For the first time, a designer can see the true performance of the sensor," he asserts.

Another Δ-Σ version in the works is the MAX1460, a true 16-bit ADC for low-voltage and low-power designs, according to Ali Foughi, Maxim's director of product development and definition. Designed to operate from voltages down to 2.4 V, the MAX1460 consumes less than 400 µA when fully operational. It will last on a lithium battery for 10 years, states Foughi. A similar device, with 128 bits of EEPROM on-chip, the MAX1458, also is coming down the line from Maxim.

Slated for release in the second quarter, the MAX1457 comes in a 28-pin small-outline package, and a 32-lead TQFP. The other MAX1400 devices are also planned for release in the next quarter. The MAX1400 family is the result of Maxim's acquisition of MCA Inc. last year.

Integrating the right mix of peripherals and functions to achieve the right price-performance ratio requires a good understanding of the application needs, says Mike Paquette, Crystal Semiconductor's director of marketing for data acquisition. "Each application has a unique requirement," he adds. Also, Paquette continues, maintaining the level of performance at low voltages is a real challenge in the analog world.

Combining this approach with advances in 0.6-µm CMOS processing, Crystal has successfully crafted an inexpensive Δ-Σ 16-bit ADC, the CS5529. Offering single-conversion settling time, this programmable 16-bit converter can handle negative input signals. Made possible by the design, the CS5529 allows two modes of operation: a single 5-V supply or dual ±2.5-V supplies. The on-board charge pump allows the use of low-level signals, according to the manufacturer. In addition, it integrates a 6-bit latch output on the same die. That setup allows control of two analog, and up to four digital devices such as switches, multiplexers, and references without extra isolation cost. The CS5529 also uses a three-wire serial interface that is compatible with the SPI and Micro-Wire interfaces.

Other on-chip features of the CS5529 include self- and system-calibration circuitry, programmable output word rates, and power consumption of only 2.5 mW. The part minimizes power consumption by running the analog circuits at 5 V and digital functions at 3 V, according to Paquette.

The CS5529 is housed in 20-pin plastic DIP and SSOP packages, and is priced at $3.80 each in lots of 1000. An evaluation board with the system schematic is also available to designers.

Based on a similar design methodology and process technology, Crystal's 24-bit family with an on-board multiplexer is also forthcoming. There are three different flavors with a similar digital interface, the CS5522, 5524, and 5528, for two, four, and eight channels of multiplexing, respectively. All of the devices will be made available in pin-to-pin-compatible packages, enabling the designer to go easily from one part to another as application requirements change. However, initially, 24-bit models may be twice as expensive as the CS 5529s.

Also driving 16-bit Δ-Σ ADCs to the commodity line is Analog Devices. The company is preparing complete 16-bit programmable analog front ends for low-frequency measurements. The AD7705/06 are two- and three-channel solutions, respectively, that accept low-level signals directly from a transducer to provide 16 bits of serial data with no missing code. Operating from a single 2.7- to 3.3-V or 4.57- to 5.5-V supply, the AD7705/06 ADCs consume less than 450 µA at 3 V. Packaging options include 16-pin DIPs, SOICs, or TSSOPs.

8-Bit Video

For many video and imaging applications, 8-bit ADCs continue to dominate the scene. Suppliers continue to drive the sampling frequencies of these ADCs. They also continue to push their ADCs' dc and ac characteristics to higher levels, while achieving excellent dynamic performance and lower power consumption from a smaller package. However, for applications that demand better than 8-bit resolution, ADC manufacturers deliver 10- and 12-bit solutions, but compromise on speed. Additionally, the cost seems to rise with the resolution.

National Semiconductor's just released the 8-bit ADC1175, pipelined video ADC. Sampling at 20 MHz, it consumes only 55 mW from a 5-V supply. Available in 24-pin SOIC or TSSOP packages, it carries a price tag of $2.80, in lots of 1000.

For those applications requiring 12-bit solutions, National has unveiled the pipelined subranging ADC12081 and ADC12181, running at 5 and 10 MHz, respectively. The 12-bit answers cost much more—the ADC12081 in a 32-lead TQFP is priced at $9.55, while the ADC12181 costs $10.95. Both prices are for 1000-piece quantities.

Other major contenders in the low-cost video-ADC race include Signal Processing Technologies (SPT), Micro Linear, and Philips Semiconductors. Philips, in fact, has driven the sampling rate of its 8-bit devices to 80 MHz. And, SPT has taken the wraps off a 40-Msample/s 8-bit ADC with excellent dynamic performance. Operating on a single 5-V supply, the SPT7734 comes in a 28-lead SOIC and a 32-lead TQFP. It sells for $3.95 in quantities of 1000.

This drive toward higher integration and better performance is also turning low-cost, single-chip ADCs into data acquisition systems. These new systems deliver total solutions requiring minimal external components. However, it is up to the user to pick the right solution from the sea of low-cost system level ADCs.

NEC ENTERS FLASH MEMORY MARKET WITH 8Mb DEVICE.

Flash memories are the fastest-growing segment of the memory market and NEC is launching a major drive into the field. The first NEC offerings are 8Mb devices for cellular phones, digital still cameras, PDAs and networking products.

The new 8Mb flash memories feature a single 3V power supply. They have a boot-block organization with x8-bit or x8/16-bit output. Designed for speed, they offer 120ns (max) access time and over 100,000 program/erase cycles. Packages are a 40-pin TSOP 1 for the x8 device, and a 48-pin TSOP 1 for the x8/16 device.

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On the Internet at http://www.ic.nec.co.jp/index_e.html

ory technology and production. The move into flash memories is significant because the company has a proven record of becoming a high-quality, high-volume player in the markets it enters. Large-capacity flash memories for file applications are the next in a long series of product introductions that NEC plans for flash memory users.

Capacity	Device	Data width	Supply voltage	Access time	Package
8M bits	PD29F008L	x8 bits	2.7V~3.6V	120ns	40-pin TSOP 1
	PD29F800L	x8/16 bits	2.7V~3.6V	120ns	48-pin TSOP 1

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The Next-Generation System Power Management

Part II Of A Three-Part Series On The Mobile Power Initiative Focuses On The Advanced Configuration And Power Interface.

NEIL W. SONGER, Intel Corp., 2200 Mission College Blvd., MS SC9-15, Santa Clara, CA 95054; (408) 765-5997.

In the first article of the series "Notebook Computer Makers Address Power Challenges" *(ELECTRONIC DESIGN, DEC. 15, 1997, P. 44)*, the historical trends concerning power were reviewed. Basically, the power dissipated in mobile-PC interiors has increased by 90% from 1994 to 1997. If the current mobile-PC power trends continue, the power will increase another 85% from 1997 to 1999. In comparison, battery capacity is projected to increase around 45% during the same time period.

If nothing is done to address rising platform power, batteries would have to be even larger to keep the same battery life we enjoy today. These power trends are making mobile-PC design more difficult, and requiring a system-level approach to solving these issues.

To address this problem, Intel Corp. has launched the Mobile Power Initiative. It is a cooperative program that unites PC industry leaders in addressing all of the areas that impact mobile-PC system power: the hardware (covered in the first article), the system power management (covered in this article), and application software (covered in a future article).

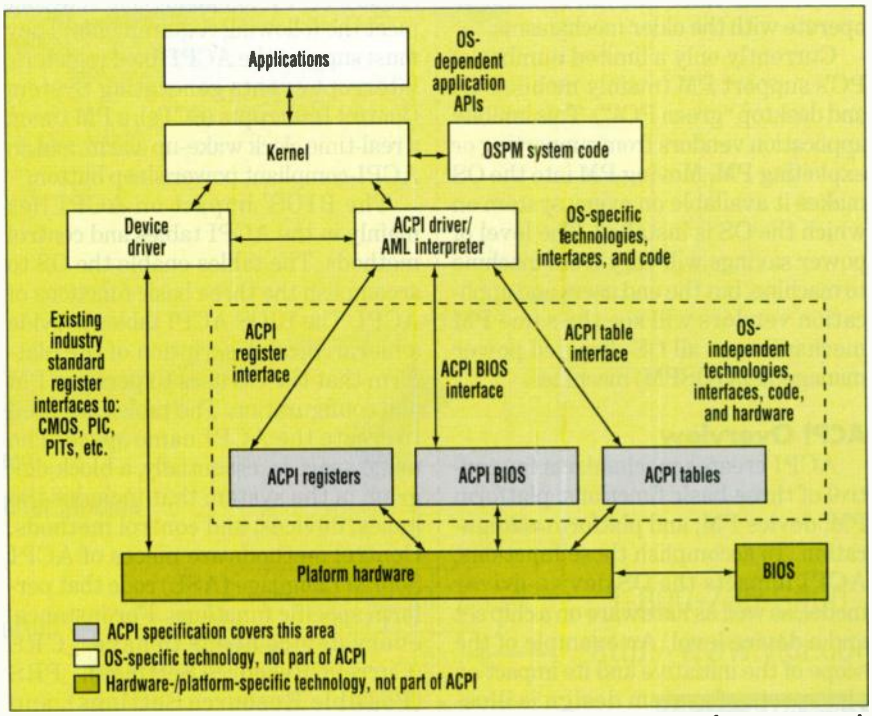
A Historical Perspective

One of the first real breakthroughs in mobile power management occurred in 1989 with the introduction of Intel's SL technology (first seen on the 386SL, and still included in all of today's Intel Pentium processors with MMX technology). This technology created a new mode for the CPU called System Management Mode (SMM). SMM allows embedded code within the BIOS to slow down, suspend, or shut down part or all of the system platform, and even the CPU itself, thereby preserving and extending battery life.

At a system level, there are timers for every hardware device that needs to be power managed. These timers keep track of how long it has been since the device was last accessed. When this timer reaches a preset time (usually configured by the BIOS) the device is power managed (put into a lower power state). This technology worked very well in its time, but as systems became more complex, the timers would need to be programmed based on what was happening at the system level. This lead to the next advance in system power management.

In 1991, Intel and Microsoft introduced Advanced Power Management (APM) as a means of integrating the operating system (OS) into the power management loop. This was done to allow communication between the OS and the SL power management (PM) code embedded within the BIOS. APM creates an interface between the OS and the BIOS. When APM was first introduced, it contained interfaces to address all of the known problems with timer based power management. Unfortunately, as systems continued to evolve, new interfaces became necessary to handle the changing hardware.

It soon became apparent that the industry would need to either continually update these interfaces, adding cost, complexity, and backward compatibility issues to both the BIOS and the OS, or find another mechanism to advance system-level PM. To address this, a more general control of PM was required.



1. Broad in scope, the Advanced Configuration and Power Interface (ACPI) specification is geared toward control of three basic functions: platform power management, device power management, and platform configuration.

CPU into a lower-power state) on an Intel-processor-based PC. C2 is a power state that provides more power savings over C1 with increased latency to enter and exit. The OS uses the C2 latency information provided in the ACPI tables to determine when C2 should be used instead of C1. C3 also is a lower-power state with increased latency. The OS, again, uses the C3 latency from the ACPI tables to determine when C3 can be used instead of C2.

The most dramatic benefits of ACPI will come from the OS' ability to dynamically and intelligently enter the most aggressive C state possible based on the current system usage. The ability to use C states as part of the System Working state (G0) was never possible before ACPI. Past PM architectures used the C states only when the CPU was idle or in System Sleeping states. ACPI C states can be used much more frequently.

The next global state is the G1 or System Sleep state. You will notice that this state is broken into four separate circles S1 through S4. S1 is defined as a low-latency sleeping state, where no system context is lost. In legacy terms, this sleeping state is comparable to a Power On Suspend.

S2 also is a low-latency sleeping state, but here the CPU and system cache context is lost. The OS is responsible for maintaining this information. Comparing it to legacy systems, S2 is a hybrid of the Power On Suspend state in which the CPU and cache are shut down to save more power.

A low-latency sleeping state, S3 loses all system context except for system memory. The OS and device drivers are responsible for restoring all of the device context except for what is in the chip set and memory, which is the hardware's responsibility. S3 is similar to legacy Suspend to RAM. S4 is the lowest-power, longest wake-up latency sleeping state supported by ACPI. To achieve the lowest possible power, it is assumed that all the devices have been powered off. S4 is similar to Suspend to Disk.

The G2/S5 state is Soft Off. The important difference about this state is that it is not a system sleeping state (i.e.: no device context is saved). From a hardware standpoint, the G2/S5 and S4 states could be identical. The difference being that when the S4 state is exited the system resumes, and when the G2/S5 state is exited the system does a full boot.

The last global state, G3 or Mechanical Off, is a state where no electrical current is running through the circuitry. This state is required to ensure a safe state in which the machine can be safely maintained/or and repaired.

The ACPI specification supports motherboard devices and other devices not covered by any bus PM specifications or device-class PM specifications. ACPI implementation allows the system designer to concentrate on providing hardware and software support for these nonstandard or value-added machine features. Only system-board-specific value-added functions need to be described through ACPI. For example, the PCI bus is defined by the PCI bus-class specification, and is natively enumerated by the operating systems PCI bus driver. Therefore, unless there are unique power or configuration functions associated with a specific device on the PCI bus, the PCI bus driver can handle both the configuration and PM of any PCI devices.

ACPI, through the use of the ACPI name space, along with OEM-provided control methods, is meant to be flexible and extensible enough to grow and adapt with the PC in the future.

End-User Benefit

With ACPI, the end-user benefit is closely related to the goals of the instantly available PC concept. From the computer user perspective, the PC is off and quiet when not in use, and returns to fully operating capability when needed. Many system components, including hardware and software, must contribute in order to obtain the desired system operation. Consistent and reliable behavior can only be achieved through OSPM, which can control the power policy and coordination across a wide-range of computer types (server, desktop, mobile PC, and network computer).

To achieve the desired operation, software components such as applications, drivers, and firmware (BIOS) are all affected. As an example, when the user pushes the Power button at the end of the day on an ACPI-compliant system, it will enter an S3 (Suspend to RAM) or S4 (Suspend to Disk) state. The next morning, when the user comes into work and presses the Power button, the system will resume (~ 3 to 5 s for S3 and ~ 10 to 15 s for S4) instead of rebooting (~ 1 to 2 min).

Other benefits the user will see are smarter PM and improved battery life for mobile PCs. With ACPI, mobile users will no longer have their systems prevented from entering low-power system-sleeping states because they had enabled a screen saver. ACPI will also address the other extreme: the system performing a PM feature when it is not appropriate. A good example can be found today, when giving a presentation on a mobile computer the screen will blank if a key has not been pressed within a certain time. This type of issue will no longer be a problem with ACPI.

The PnP aspects of ACPI also will benefit end users. It won't make configuration errors disappear, but it should prevent days and/or nights of unsuccessful computer upgrades.

Availability

ACPI support is required as part of PC98 compliance in April 1998. Systems will begin featuring hardware support for ACPI as early as January 1998, with provisions for BIOS upgrades when Windows 98 or NT 5.0 testing has been completed. According to Microsoft, Windows 98 is currently scheduled for release in the first half of 1998, and NT 5.0 in the second half of 1998.

Intel, Microsoft, and the major BIOS vendors are all providing support for OEM's to ensure there will be no hardware road blocks to the release of ACPI-compliant systems. Intel, Microsoft, and Toshiba, to help speed development of ACPI-compliant systems, have hosted ACPI Implementation Workshops. Microsoft is providing a Hardware Compatibility Test that checks for ACPI hardware compatibility. Intel provides three tools focusing on testing system power with different levels of accuracy: Intel Power Monitor, Intel Power Management Analysis Tool, and Intel Power Analyst. For more information on these tools and the Intel Mobile Power Initiative please visit *http://developer.intel.com/design/mobile/intelpower.*

Neil W. Songer is a senior system architect at the Intel Mobile and Handheld Product Group. Previously, he worked at IBM as a system designer. Songer holds a BSEE from the Georgia Institute of Technology.

Embedded Battery Identification Chip Supplies Real-Time Data To Controller

The DS2437 is a complete data-acquisition system on a chip. The battery ID device, which collects battery information in real time, supplies all of the battery data needed by a host system to ensure that the battery doesn't overcharge or discharge. Developed by Dallas Semiconductor, the chip can be embedded in the battery pack, where it senses temperature, voltage, current, and charge going in or going out, and then supplies that information in real time to the battery controller.

The circuit provides 40 bytes of EEPROM nonvolatile storage that can be used to hold critical safety and performance data such as chemistry, capacity, and manufacturer. With this information, the battery controller can optimize the battery system for multiple chemistries, suppliers, capacities, and usage history.

The DS2437 thus serves as a mini data-acquisition system, acquiring operating and condition data from the battery pack. Temperature is measured by a direct-to-digital temperature sensor that eliminates the need for thermistors in the battery pack. The ability to measure temperature over a –55 to +125°C in 0.03125°C increments allows the host to confirm safe charge conditions and determine the charge cut-off point.

An on-chip analog-to-digital converter measures battery voltage and current, allowing the system to make end-of-charge and end-of-discharge determinations. An integrated current accumulator provides a gas-gauge function by keeping a running total of all current going into and out of the battery. Also on-board is a crystal-controlled oscillator, which supplies real-time functions such as elapsed time and time-of-day.

Information between the host microprocessor and the chip is sent over a one-wire interface (plus ground) that minimizes the number of connections required between the host and the battery pack. As a result, with the addition of a power-supply pin, just three connections to the host are required to provide the complete interface. The chip can operate with an external supply that spans 2.7 to 10 V and consumes less than 50 µA typical on standby, and just 250 µA typical when active (maximum currents of 0.1 and 1 mA, respectively).

The DS2437 isn't linked to any one battery chemistry and can thus be used with NiCd, NiMH, sealed lead acid, rechargeable alkaline manganese, lithium ion, and lithium polymer, as well as other chemistries. Applications for the chip span a wide range of end products—cellular phones, PCs, PDAs, handheld instruments, portable power tools, entertainment electronics, etc.

In lots of 10,000 units the DS2437 sells for $3.95 apiece and is available from stock.

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0.027-In.-Thick Touchpad Sensor Combines Pen Input With Mouse Functions

The VersaPad touchpad sensor designed by Interlink Electronics supports pen input for handwriting recognition applications, as well as signature verification on PCs, keyboards, cell phones, two-way pagers, and other handheld equipment. At just 0.027 in. thick, the sensor is claimed to be the thinnest device in its class. VersaPad also provides traditional mouse control functionality.

Handwriting recognition is a key application for the sensor. Adding the unit to a notebook PC, for example, can help redefine the role of the PC's input device to include pen applications (e.g.,text character capture). The company has enlisted the support of Communication Intelligence Corp., Redwood Shores, Calif., to integrate its handwriting recognition software with the VersaPad sensor.

Signature capture and verification are both supported by the sensor as well. Interlink has partnered with PenOP Inc., New York, N.Y. to combine use of that vendor's CyberSIGN signature-capture software with the VersaPad sensor.

VersaPad's software, called VersaPoint, incorporates the WinTab interface for connecting graphics tablets to PCs. VersaPoint includes features such as graphics capture, which allows users to paste hand-drawn graphics into their application.

Two standard sizes are available: 25.5 mm by 25.5 mm (active area) for cell phones and two-way pagers, and 55.5 mm by 39.5 mm (active area) for notebook PCs and keyboards. For custom applications, the sensor is scaled to meet the requirements of most pen applications. To minimize thickness, VersaPad's electronics needn't be part of the module. The 0.7-mm touchpad can be mounted directly onto a device and connected via the pad's integrated tail to the remote electronics.

Both fingertip and stylus input modes are supported, with optimal touchpad resolution of 1000 lines/axis. VersaPad firmware supports 200 counts/inch. Hardware interfaces include PS/2, RS-232, and custom types.

Using the suggested support circuitry design, power consumption ranges from 2 to 5 mA during use. After about two seconds of non-use, the sensor slips into a sleep mode that consumes 0.1 µA VersaPad automatically wakes up upon sensing touch and immediately starts transmitting data again. The sensor resists moisture, harsh chemicals, ESD, and EMI, and has a tested lifetime of five million strokes (118 miles of pen input).

The OEM Sample Kit includes everything necessary to test and integrate the sensor. The kit sells for $150.

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Scientists finding OKI Communications IC in Mars rock puzzled by sign of highly intelligent life. Design engineers are ecstatic.
Fearing for the fate of his new communications system, the mayor looks to a Super Designer for a WLL solution.
With GaAs and guts, POWER SAW™ god of communications, sees everything's compatible. Or else...
In the city, Echo-Echo is making every phone conversation sound like heavy metal in a trash can...
UH-OOOOOOOO-ULG-UMP-SLURP-SLURP-SLURP! Ha-Ha-Ha
...Pow R. Waster is sucking up so much energy he could be arrested for assault on a battery...
...and frequency interference is creating cross-talk.
Hello? Where? You? Are you? What?
Goodbye. There. Is this? Huh?
Thrown everything at 'em and they're still coming! Well, being a Super Designer means having Super Friends.

And, a fast way to reach them!
Hey guys! The OKI Support Call. Let's go.
Pow. R. Waster's mine. Hey Waster. My 3V's outlasting your 5V! How's that for a CODEC moment!
www.okisemi.com
Get a whiff of this GaAs! That oughta stop you "freqs" from mixing it up and making cross-talk.
Cancel me this, Echo-Echo. What's so quiet you can't hear it? You! My 55ms does it every time... You're outta my WLL!
Con-grat-u-lations!!! Super "D."
GULP!!! Hope he's not thinking of running for mayor!
Capt. CODEC says, "Visit our OKI Website to get my Capt. CODEC T-shirt. It's free for Super Designers like you."
OKI ComICs™ is brought to you by OKI Semiconductor. Super solutions for all your wired and wireless communications designs— Echo Cancellers, CODECs, SAW filters, GaAs amplifiers and mixers, 8-port MACs, ASICs and more. OKI—your one-stop Com(munication) IC source.
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ELECTRONIC DESIGN QUICK LOOK

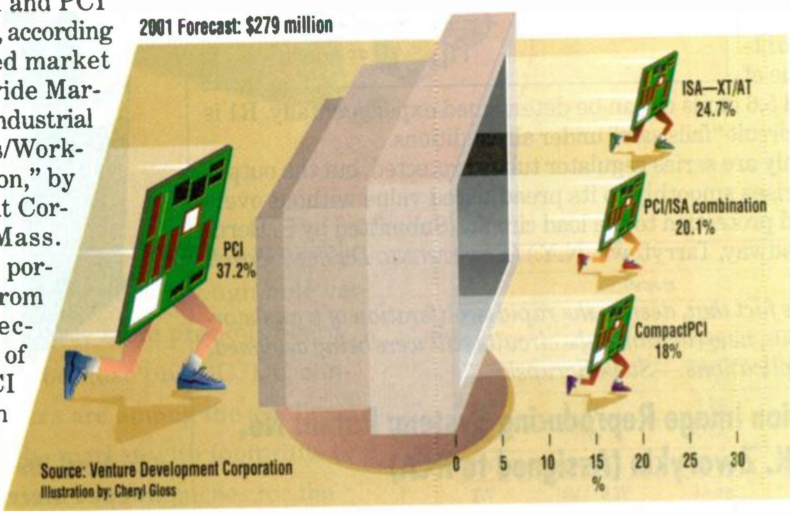
Edited by Debra Schiff

MARKET FACTS

PCI And CompactPCI Chase ISA Out Of Industrial Computers

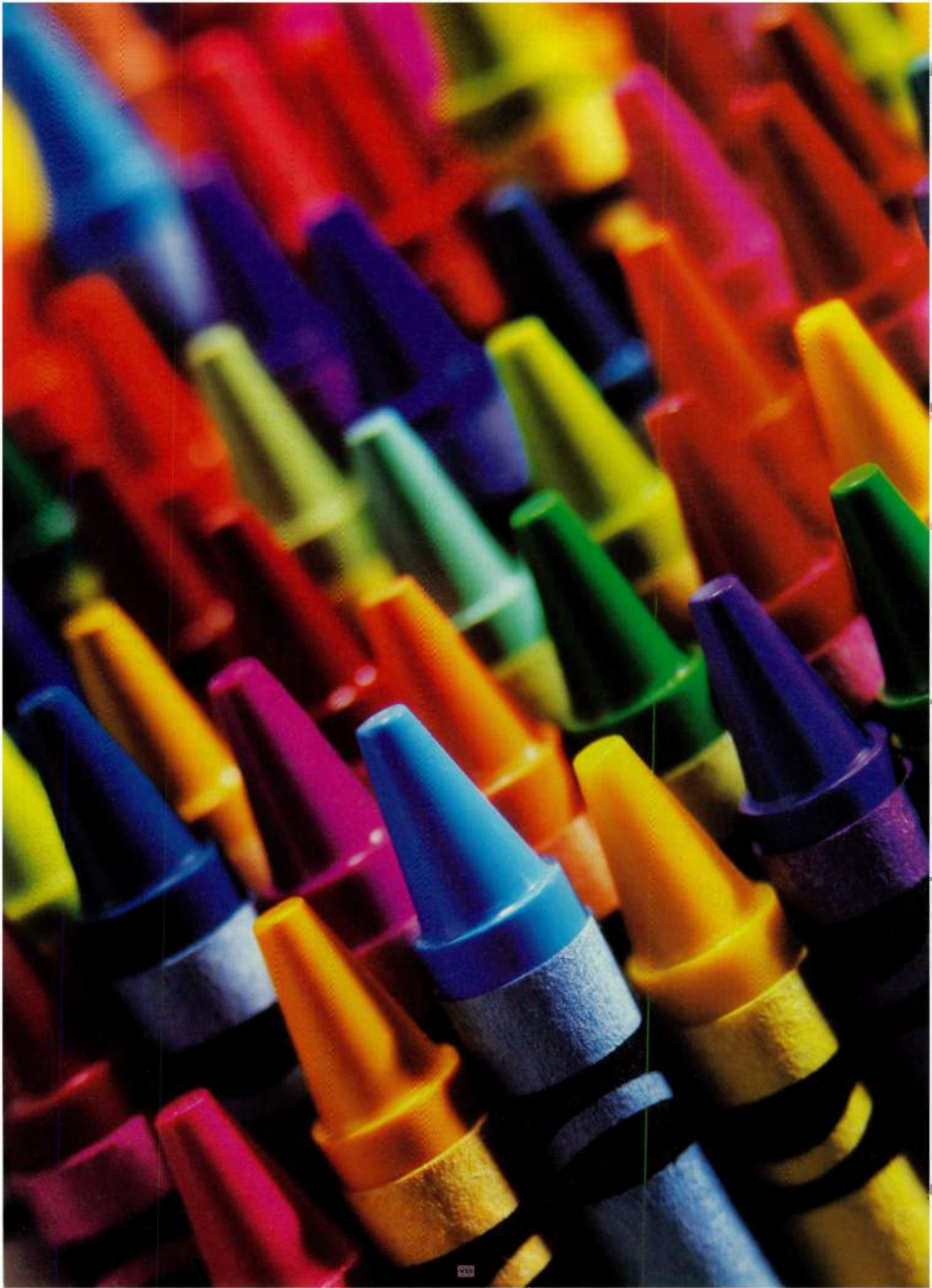
Primary bus architectures for passive-backplane single-board computer (SBC)/CPU boards used in ruggedized/industrial PCs worldwide are predicted to undergo an enormous shift in the near future, thanks to the increasingly rigorous demands of today's industrial workplace. It won't be long before the traditional leading architectures like ISA and PCI/ISA take a back seat. Relative newcomers such as CompactPCI and PCI will become dominant, according to a recently released market report, "The Worldwide Market for Ruggedized/Industrial Personal Computers/Workstations, Third Edition," by Venture Development Corporation, Natick, Mass. Adoption of PCI/ISA portends a move away from "ISA-only" architecture. The emergence of PCI and CompactPCI for exclusive use in the near future will unquestionably hasten the death of the ISA market. When Intel proposed the Peripheral Component Interconnect (PCI) bus scheme in 1992, the company intended it to be used for motherboard connections between CPUs and high-speed peripherals. However, PCI quickly evolved into an add-in card-connection bus scheme. It continues to transform, with at least six PCI variations available, and more planned. The report predicts that PCI's existing market share of 15.9% for passive-backplane SBC/CPU boards in industrial PCs will expand to more than one-third by 2001. PCI's success in the marketplace is a direct result of the careful balance between performance and flexibility. The bus offers a 32-bit pathway, which runs at a clock rate of 33 MHz. This pathway provides a 132 Mbytes/s peak-burst bandwidth. The bus is processor-independent, allowing it to work with any CPU or peripheral. The bus also is extensible. Revision 2.1 of the PCI specification includes definitions for 64-bit PCI and 66-MHz clock options. All these features account for a comparatively higher speed and throughput. CompactPCI, the star architecture of the future, is forecast to more than quadruple its share of the IPC/workstation market over the next four years. By 2001, it should own almost one-fifth of the world market for passive backplane SBC/CPU boards used in industrial PCs.

Ruggedized PC Workstation Passive Backplane SBC/CPU Board Shipments Worldwide



CompactPCI uses standard Eurocard mechanical components and metric connectors, providing a system optimized for rugged applications. In addition, it is electrically compatible with the PCI specification 2.1 (33 MHz), allowing the use of inexpensive PCI integrated circuits and software. A majority of the end users surveyed in the report mentioned reliability as a crucial factor in the selection of a ruggedized computer. This is where CompactPCI has taken the lead over PCI. CompactPCI boards have connector and card guides that firmly hold the boards in position. They also have a faceplace that features an injector/ejector mechanism. The boards can be solidly screwed into the card cage. Boards also can be mounted vertically, allowing for natural-convection cooling, which is often assisted by forced-air cooling. Most importantly, the pin-and-socket connector of CompactPCI boards is considered to be more reliable than the edge connector of the standard PCI boards. Meanwhile, the writing is on the wall for ISA and PCI/ISA.

Dinender Sharma is a research director for Venture Development Corporation, a market research and consulting firm, specializing in electronic technology. Sharma holds an MMS in management studies from BITS, Pilani, India, and an MBA from Northeastern University, Boston, Mass. He can be reached at (508) 653-9000, ext. 124 or by e-mail: dsharma@vdc-corp.com.



INTERNET NEWS

It's nearly Spring, and you know what that means—time for Spring Internet World 98. Held March 9-13 at the Los Angeles Convention Center, Los Angeles, Calif., this conference is a great opportunity for Information technology (IT) specialists to get a jump on the competition. Over 200 workshops and sessions will be focusing on coming technologies, applications, and issues dealing with today's and tomorrow's Internet.

As with every Internet World show from Mecklermedia, the Exhibit Hall features the Internet World Café, a fun place to take a coffee break after walking the show floor for a few hours. This Exhibit Hall also has a Microsoft Partner Pavilion, Oracle Partner Pavilion, Sun Microsystems/Java Partner Pavilion, Novell Partner Pavilion, IBM Show Network, and E-mail Center.

Sometimes people only go to the show just to see the keynote speakers. In this case, the choices are Lewis E. Platt, chairman/CEO/president of Hewlett-Packard; Edward J. Zander, president of Sun Microsystems; Jerry Yang, co-founder of Yahoo!; and Stewart Alsop, partner at New Enterprise Associates, a venture capital firm.

Then, there are others, such as yours truly, who prefer the Hands-On Workshops. These training sessions are limited to 30 participants, so reserve your seats early. The following workshops are given at Spring Internet World: Webmaster HTML Fundamentals, Electronic Commerce Fundamentals, Web System Administration, Internet Security and Firewall Systems, Java Primer, Web Scripting, and Java vs. ActiveX.

There also will be special TCP/IP Technology Workshops at the conference. These PING-centered workshops, as are the others mentioned above, are sponsored by Net Guru Technologies. TCP/IP Infrastructure: Foundation for Enterprise Networks, UNIX and Windows NT Internetworking, Managing Networks Using SNMP, Web Server Performance Analysis and Tuning, Routing in Enterprise Networks, and Migrating to IPv6 will all take place from Monday March 9 through Friday March 13, at Spring Internet World.

The marketing specialists can all be found at the Adweek Forum, a two-day sales and marketing intensive blitz that takes place on Monday and Tuesday, March 9 and 10, respectively. Other highlights include Java, Commerce, and Security Day (March 9); the two-day Internet News and Entertainment Summit (sponsored by KPMG, MSNBC, and internetnews.com); and the Knowledge Management Forum.

The quickest way to register is via the web: *www.internet.com* or e-mail: siwreg98@mecklermedia.com, but you can call (800) 632-5537 or fax (203) 226-6976 for information, as well.

—DS

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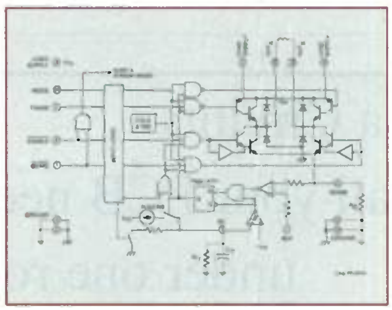

Dual Full-Bridge PWM Motor Driver — A2919

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E-Mail Goes Mainstream

There probably aren't many people who think that having access to e-mail is a bad thing—even if it is just as an option to avoid the high cost of a long-distance phone call. The problem is that for most people, having access to e-mail means having to purchase a computer. And, if you're a professional who happens to travel, it means having to lug around a heavy, lap-top computer. But, thanks to Ultradata, there is now another option.

The company has developed a handheld, portable e-mail system that allows the user to send and receive e-mail from any phone line in the continental U.S. It does not require any prior computer knowledge to operate, nor a computer. And, it retails for just under $200, which along with a monthly fee of about $10, gives the user unlimited e-mail access.

Besides sending and receiving e-mail, E@sy Mail, can also receive personalized information including stock quotes, weather reports, horoscopes, lottery numbers, and sport scores. It also operates as a multifunction organizer and appointment book, with its own alarm system, as well as calendar, calculator, fax, and clock .

The E@sy Mail portable e-mail, organizer, and information services device is targeted at the first time e-mail user and those who don't want to be saddled with a portable computer to access their e-mail.

It is very easy to operate, as easy as using the phone. To send a message, the user simply plugs the unit into any regular RJ-11 connector. With the press of a button the unit automatically dials a local access number to establish an Internet connection. The e-mail is then sent and received within a matter of minutes. At the same time, information or other e-mail messages can be received in much the same manner.

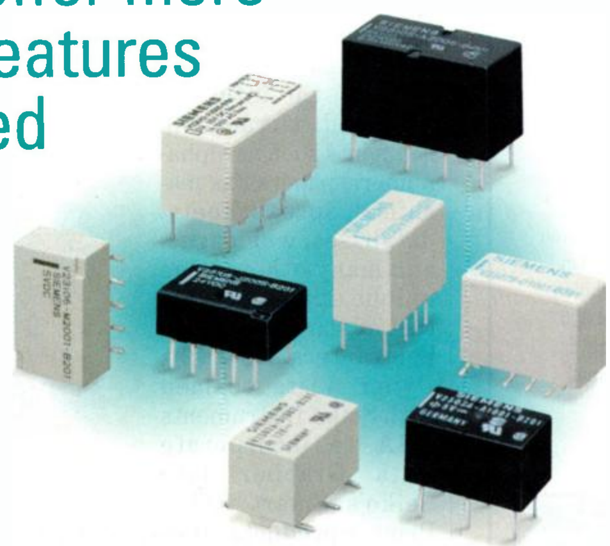
Its case measures just 7 by 3 by 1 in., and weighs a mere 11 oz; making it suitable for a briefcase, purse, or even a pocket. When open, E@sy Mail can either lie flat or be adjusted by the user for optimal viewing of its liquid-crystal display (LCD). An ergonomically designed keypad and function keys, with the standard cursor and functional shortcuts provide simplified input access. The LCD is can provide up to eight lines by 40 characters of text. It is powered by three AA batteries and can run for up to 20 hours.

For more information on the product call 800-747-2605.

Cheryl Ajluni

SIEMENS

Our new low-signal relays offer more of the features you need



You wanted more, and we've got it

Your designs demand more, so we're providing more! We've expanded our line of low-signal relays. New models provide just the features you need for application in telecommunications equipment, computer peripherals, security systems, office automation and more. These relays offer:

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Series	V23026	V23106	V23079	V23105	V23042
Contacts	SPDT	DPDT	DPDT	DPDT	DPDT
Dim. (mm)	13 x 7.9 x 6.9h	14 x 9 x 5h	14.5 x 7.2 x 9.9h	20 x 9.8 x 12h	20.1 x 10 x 10.6h
Contact Rating	30W 60VA	30W 62.5VA	60W 62.5VA	60W 125VA	50-150W 250VA
Nominal Coil Power	30-150mW	100-200mW	70-140mW	150-300mW	75-360mW
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Fax Doc. #	8026	8106	8079	8105	8042

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Sometimes Grabby Is Good

For a while web casting and push technology were "the next big thing." Then everyone got sick of having their desktops flooded with information that they simply didn't use. Now, the trend is to take that information and divide it up into usable segments, trashing all the inappropriate stuff in the process. But, the trick is to have that task completely automated.

Cyber Vista, a company that specializes in Internet and intranet information task management technology, has defined specific software that will grab, as they put it, online information exactly the way the user wishes. Data Grabber, the information-collecting technology, goes out to web sites, e-mail, online services, FTP sites, databases, search engines, and third-party servers to pull the technology that's been requested.

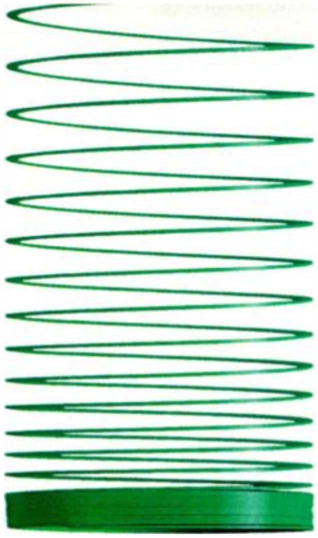
When the information has been collected, it is processed, reformatted, and delivered to all kinds of environments such as alphanumeric pagers, fax machines, spreadsheets, databases, web pages, and many others. One unique application for the software is in PC-label printers. Recently, Cyber Vista teamed with Seiko Instruments USA to incorporate Data Grabber into Seiko's Smart Label Printer products. Models 120, 220, and EZ30 (shown here) will be the first label makers to use the task agents to collect online information.

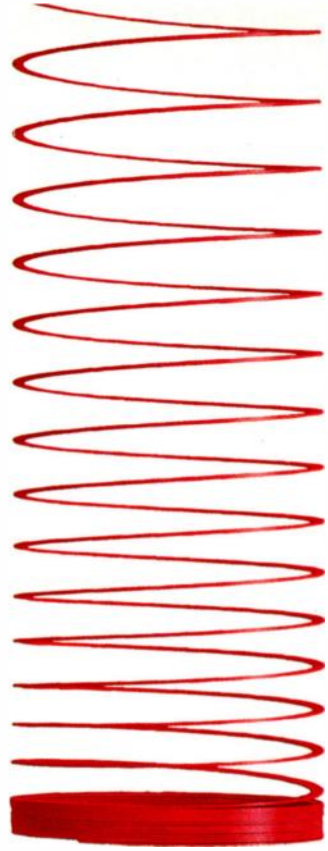
The companies decided that there was a definite need for a label printer that could automatically verify addresses and other data before it printed the labels. Also handy is the tool's ability to collect air schedule options or driving directions for package labels. The Data Grabber task agents have been customized for Seiko's label printers application.

The Data Grabber Maximizer allows users to strengthen their firewall security, automate existing applications (in the case of redundant tasks), retrieve e-mail from multiple locations simultaneously, automatically update and distribute software, and amongst a host of other features, update credit reports.

Cyber Vista also has introduced a "lite" version of Data Grabber, which is available as a free download from the company's home page: *www.cybervista.com*. Data Grabber Player Lite comes with four task agents and a tutorial. These task agents, like those in the label printer, have been specially customized for the application. Users who download Data Grabber Player Lite will be able to monitor any web site for changes, track any five selected stocks, demonstrate Windows APIs for technical users, and retrieve and present the lowest air fares at specified dates and times.

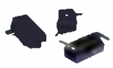
Contact Cyber Vista, 1650 Borel Pl., Suite 121, San Mateo, CA 94402; (650) 372-0800; fax (650) 372-5605; e-mail: sales@cybervista.com.—**DS**



Micro Springs

1.65 - 12.55 nH
Q up to 200, IDC up to 1.2 A
Designer's Kit C108



Mini Springs

2.5 - 43 nH
Q up to 210, IDC up to 3.0 A
Designer's Kit C102

NEW!

Midi Springs

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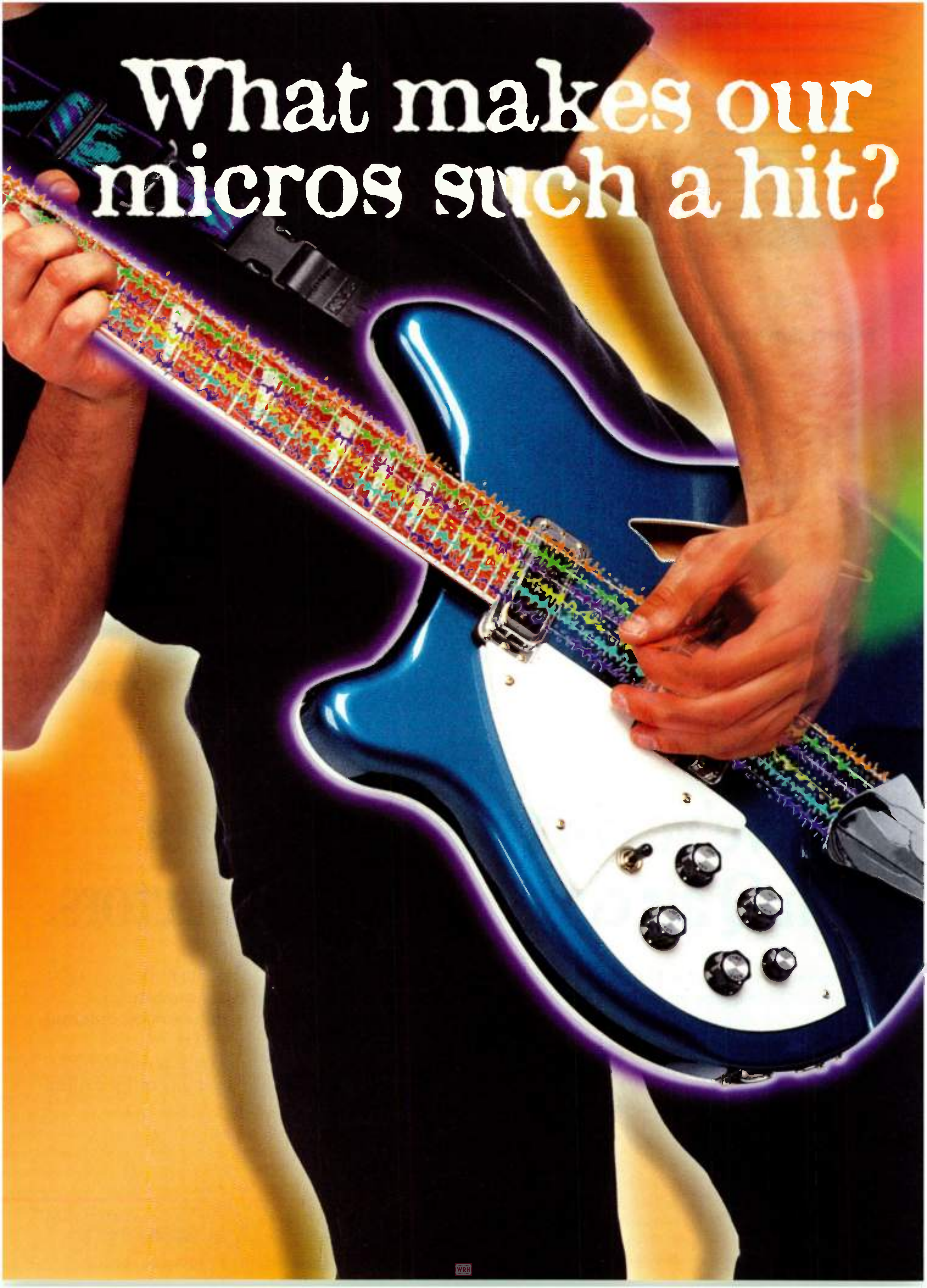
What makes our micros such a hit?

MANAGING THE DESIGN FACTORY

Features Are Free

At a meeting in Asia recently, I heard a marketeer argue eloquently that electronic products had entered the brave new age where features are free. Of course, this is the age that marketing people have been waiting for since the first marketeer emerged from the caves with a designer bone in his nose. He argued that feature content was shifting from hardware to software, and that software features add little to unit cost. In fact, the unit cost of the system changes so little when we add features that for all practical purposes they are free. Well, as anyone who has ever accepted a "free" kitten knows, many things that are free actually carry with them certain hidden costs. This is certainly true of free features. As you may suspect, the true price we pay for a free feature does not show up in unit's manufactured cost. Instead, it typically shows up in up in three other areas.

DON REINERTSEN

First, and probably most importantly, free features lengthen our development programs, and on projects where a month of cycle time can be worth millions of dollars, this is hardly free. Most development projects are already a full-time effort. When we add features, we add work, and work takes time. Marketing needs more time to prepare the specification. Every feature has details, and the customer needs to help us resolve these details. We may decide to add an item to a menu, but somebody needs to specify where it will go, how it will work, and find out what the customers really want.

But this is only part of the work. Engineers will have to spend time implementing this feature. Next, testers will write a test program for the feature. Testing will reveal bugs that need to be corrected and retested. Ironically, the testing burden of incremental features is usually enormous, because each incremental feature raises system integration and test time geometrically. In fact, for most companies, the biggest cycle-time impact usually comes from added testing on the critical path of the program.

Say we decide to add a mouse in addition to the pull-down menus. Now, most of the test cases in the test suite will need to be modified. New test cases will have to be added. And, unlike the design of the feature, which we only do once and pay for once, the testing burden will be paid every time we run the test suite. Since this can occur tens of times during the design, we can pay a huge price in cycle time for testing our free features.

But, delay is not the only hidden cost of these free features. Along with delay comes the second hidden cost, an increase in development expenses. What looked like a free feature is actually absorbing marketing, engineering, and testing resources that we may need desperately for another project.

The third hidden cost is the most subtle. While free features may not show up in manufactured cost they may still show up in the cost to the consumer. I remember working with a computer supplier who decided to add a sophisticated and complex security system on their system. Customers thought it was nifty, but complaints came in from the sales force and the distribution channel. The free feature had to be configured and explained to the customer. This added time to the sale and reduced their productivity. Even free features need to be communicated, demonstrated, and supported.

Beware of the free feature. Make sure that every feature carries its own weight. Even the most trivial enhancement may carry years of hidden costs.

Don Reinertsen is president of Reinertsen & Associates, a consulting firm specializing in product development management. He can be reached at (310) 373-5332 or e-mail: DonReinertsen@compuserve.com.

@IEEE

In its ever-exhaustive efforts to help the engineer in his or her career path, the Institute of Electrical and Electronics Engineers (IEEE) has now added another useful tool to its cache. "Salary Benchmarks: A Personal Workbook," allows electrical, electronics, and computer engineers to find exactly what they're worth in today's market. The work book is based on IEEE-USA's "1997 Salary & Fringe Benefits Survey: Executive Summary," *(ELECTRONIC DESIGN, July 21, 1997, p. 135).*

There are two models in the workbook for determining salary information. They both ask you to calculate your level of experience as of January 6, 1997, discounting time spent in full-time study in either undergraduate or graduate schools. They also send you to a "Base Incomes" table to match up your years of experience with the Median Base Income From Primary Sources.

Next, calculate your adjustments. These take into account such factors as degrees, specialty, job function, employer size and type, line of business, and region. Essentially, this is where the two versions of the salary estimation calculations diverge. There are more subtle definitions of the levels of engineering responsibility in the second method.

The final step is the same for both methods: calculate the final comparison for the specified situation. Here you "multiply your base income estimate by the product of all the adjustment factors to get the middle-income estimate." Then add in the Consumer Price Index to balance your salary, adjusting for growth in engineering pay scales between January 1997 and today.

The workbook is priced at $14.95 for members and $19.95 for nonmembers.

For more information, contact IEEE-USA, 1828 L St., NW, Suite 1202, Washington, D.C. 20036-5104; (202) 785-0017; fax (202) 785-0835; e-mail: c.currie@ieee.org.—**DS**

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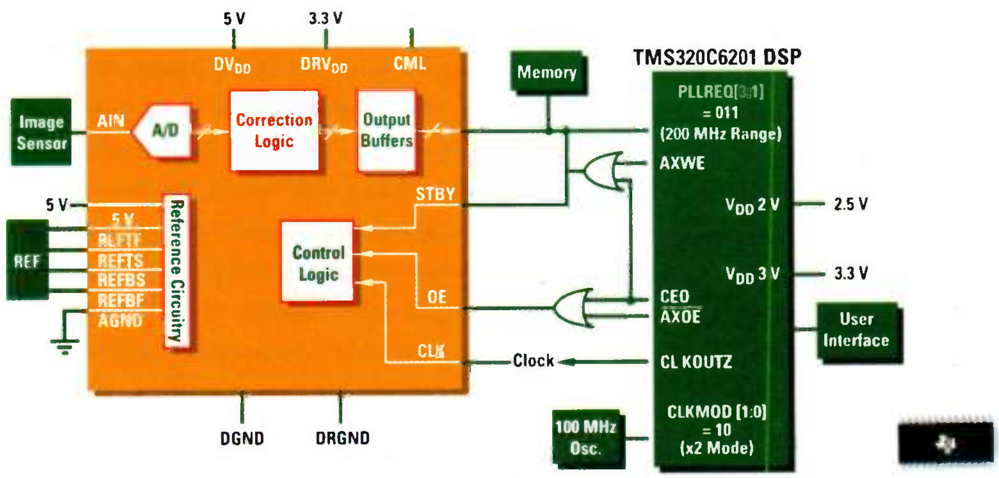

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- 2X the impedance of the reference input

*Price is per device in quantities of 1,000.

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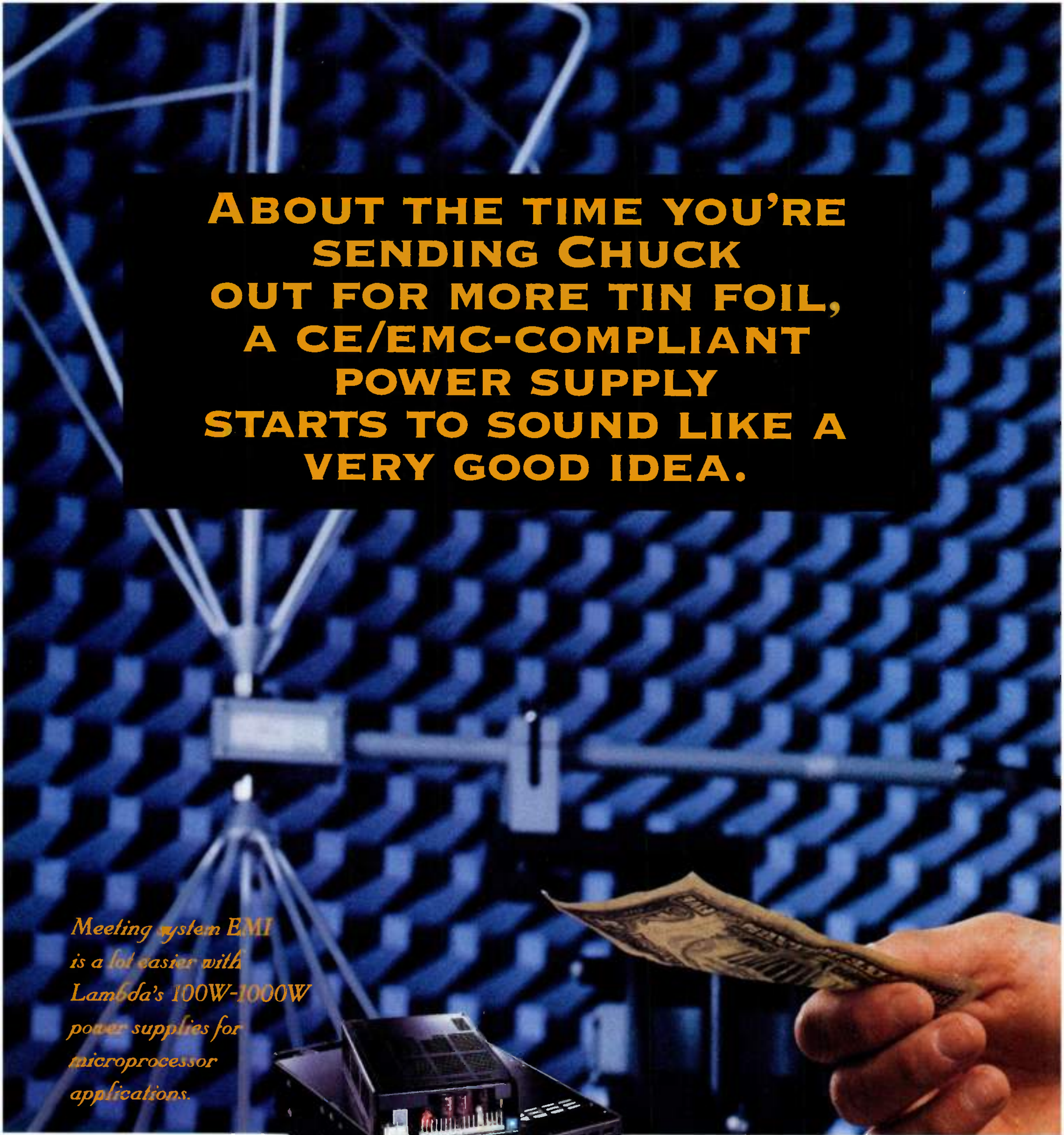
1836

MIXED SIGNAL & ANALOG

TEXAS INSTRUMENTS



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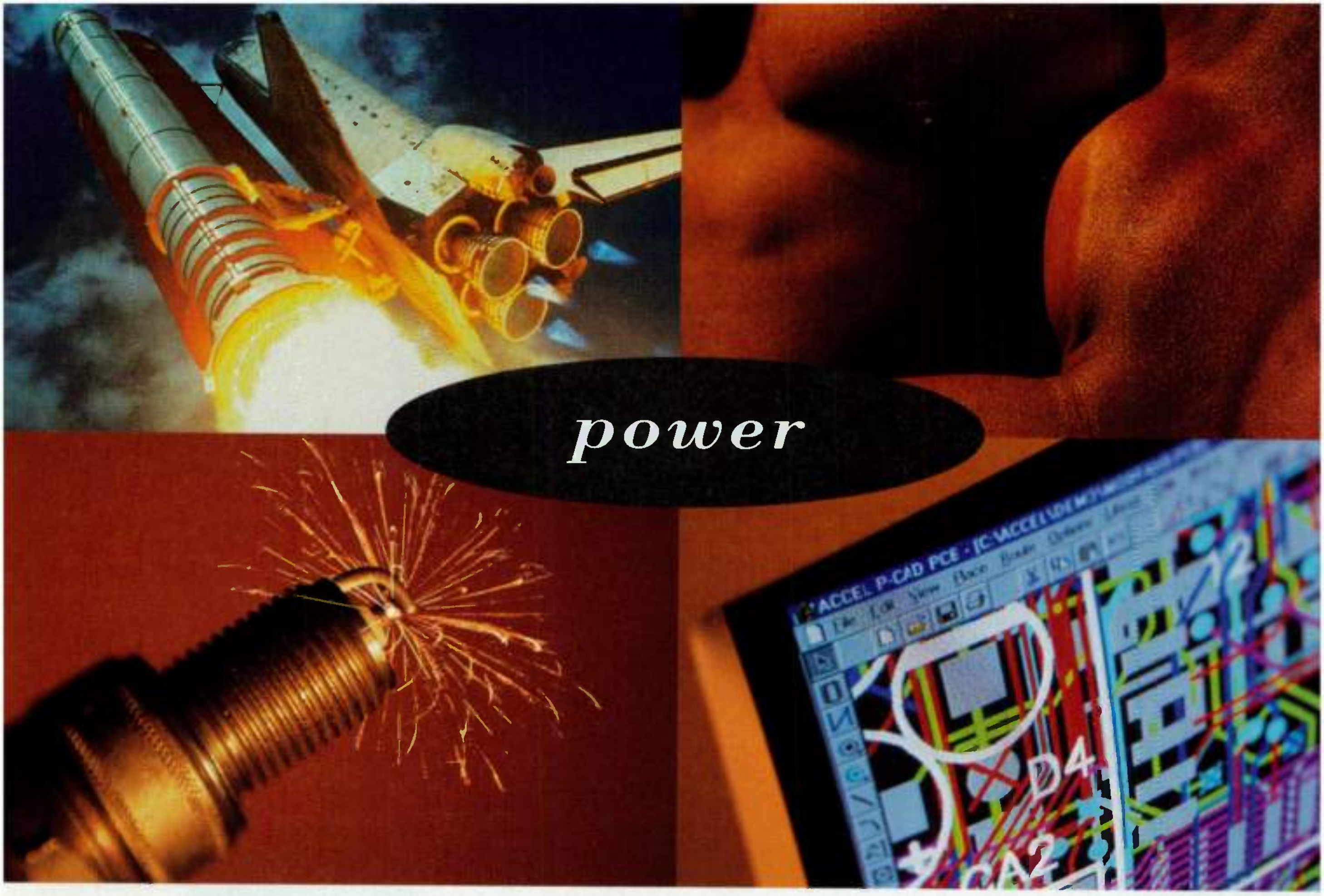

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Cheryl Ajluni

SPECIAL REPORT

As technology changes, the challenges designers must face grow dramatically. Designers and companies developing products to compete in the consumer marketplace are continually faced with questions of how to keep pace with the dynamically changing design environment, let alone excel. Accomplishing this task by harnessing the power of today's technology without increasing design risks, costs, and time-to-market, is an enormous challenge.

Advanced technologies offer a myriad of opportunities for designers to differentiate their products, push the limits of current design performance levels, and cut costs. But they also increase project risks significantly. As a result, many designers have turned to using design services now offered by a host of EDA tool vendors and independent service houses. These centers, equipped with the knowledge of how to design, verify, and test complex systems, offer viable design alternatives to supplement traditional EDA methodologies *(see "Design services are business reality," p. 70)*.

Art Courtesy: Praegitzer Industries Inc.

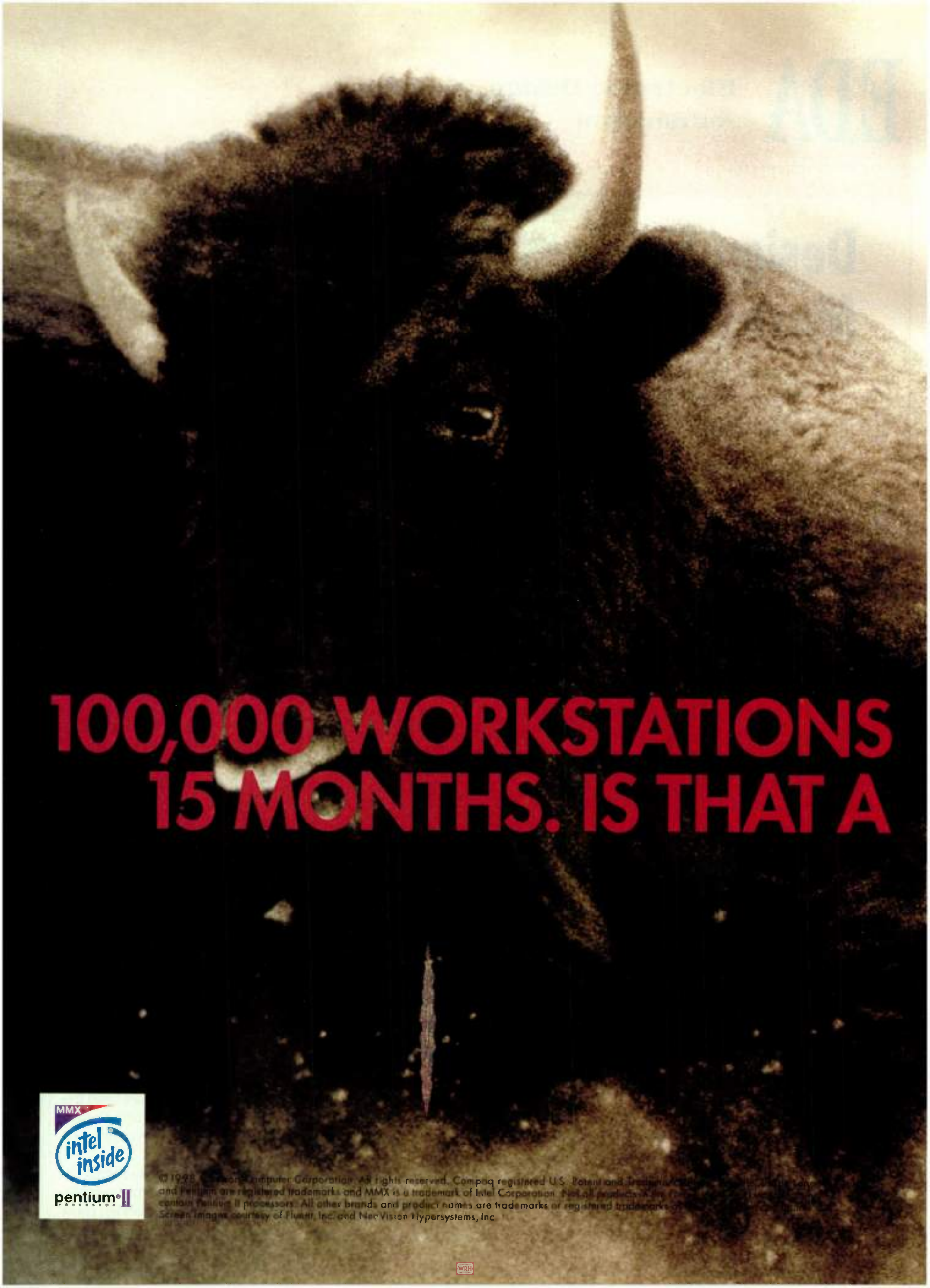
What's The Point?

The concept of design services isn't new, although it has taken on a stronger connotation in recent years *(see "The ABC's of design service," p. 74)*. The question is: Why? According to Mike Baird, president, Willamette HDL, Beaverton, Ore., "There are three major reasons: lack of manpower, lack of expertise in particular areas, and lack of specialization."

Ten years ago, when many companies were downsizing, it would have been hard to imagine the scenario we are faced with today: not enough engineers to go around. But this fact alone has contributed to the need for design services, which, among other things, offers companies a means of quickly supplementing manpower on an as-needed basis.

The lack of expertise in particular areas often becomes apparent when a company deems a new technology or methodology necessary for a particular project. An example might be using an HDL instead of schematics. And, even if a company decides to migrate to a new technology or methodology, there's no guarantee its engineers will know how to use it. In addition, the process of training engineers is often lengthy, making it difficult at times for a company to meet stringent time-to-market pressures. Design services address this need by helping to ease the transition to new technologies, tools, or methodologies. And, in areas of specialization not used frequently enough by a company to justify bringing the technology in-house, such services offer a more cost-effective option.

EDA tool vendors have not kept pace with the rapid changes required for current and future generations of electronics products. As Tom Beckley, presi-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dent and CEO, Xynetix, Fishers, N. Y., explains, "Today's tool architectures are dated, integration standards are neither embraced nor designed into the tools, and ease of use, by definition, is a major challenge given the varied designs that each EDA tool is tasked to do. Even more important, though, is the process change underway in the design environment at electronics companies. Design complexity is forcing electrical engineers to solve more and more problems (signal integrity, EMI, thermal, etc.) simultaneously and earlier in the design cycle."

In many cases, technology has become so complicated companies find themselves with problems they just can't fix. Such challenges, as well as process, organizational, and electronics complexity, have made the design process difficult and time-consuming.

The bottom line is that many companies want to get a bigger "bang for their buck," and design services offer a practical way to make this happen. The rapidly growing adoption of design services is not really a paradigm shift, but rather a sign of maturity and of companies beginning to focus on their core competencies while outsourcing everything else. As Sena Reddy, executive vice president of operations, MMC Networks, Sunnyvale, Calif., explains, "Ten years ago, if you wanted to build a fabless company and went to an investment banker for financing, he would have thought you were crazy. On the other hand, if you went to an investment banker today and said you wanted to build a fab, he would probably throw you out of his office. It's the same parallel with design services and a sign that the world has become centers of competencies."

Benefits

Of all the benefits derived from using design services, one of the most important is time-to-market. This is quite apparent in the consumer and communications markets. Here, time-to-market is a driving factor, exasperated by the fact that there are many different combinations of possible derivative products a company can develop.

Design service organizations also can help accelerate a company's entrance into new markets. As Peter San-

Design Services Are A Business Reality

The economics of downsizing and the attention to core competencies continue to change the business paradigm in electronics. It takes a tremendous amount of expertise to get a product designed in today's environment. This convergence of business economics with design reality has made design services a major trend in electronics. It may be the only way to continue to meet time-to-market demands.

Consider the following scenario: In addition to what most of us consider to be core competencies of product architecture and hardware design expertise, designers also must have design process expertise, which encompasses design methodologies, test strategies, HDL coding techniques, and CAD tool integration and management.

Hiring consultants, or the ability to work from a home office, was once discouraged. Now, they are encouraged. With the arrival of the Internet, the World Wide Web, electronic mail, and fax machines, the virtual office is a reality, along with virtual project teams comprised of internal and external resources.

Our industry is now outsourcing critical and not-so-critical parts of the design process—everything from design concepts, design, validation and test, to layout, manufacturing, and training. Requirements can be strategic or tactical, but typically depend on where help is needed to implement the design strategy.

As design consultants and trainers, we've observed successes and areas for improvement. Some services are more readily outsourced, while other core competencies best remain part of the internal design organization.

In our experience, electronics companies are employing design consulting experts to devise and implement strategies for functional verification, modeling and system-level simulation methodologies. Strategies for database management, CAD-tool integration, or set-up and development of use models also are being outsourced. Out-of-house expertise is used to develop functional tests and test vectors.

Outsourcing, as a viable business tactic, is receiving validation from the successful teaming of in-house design professionals with design consulting firms. As an example, a U.S.-based electronics company devised a creative solution, combining its team of design professionals with out-of-town design consulting for a critical design project. The company's internal expertise was in product architecture and hardware design. The design consulting firm brought experience in system-level simulation, functional verification strategies, test-fixture development, and CAD-tool integration.

The internal and external teams worked well together because, from the outset of the project, management outlined responsibilities, reporting structures, and areas of expertise. For the most part, communication between teams was done via telephone and e-mail. Consultants did not work at the company site. Data was transferred via electronic mail, fax, and file transfer protocol (ftp). The finished product—an Intel processor and an ASIC with a printer, LCD, memory, audio, and serial interfaces—was successfully released on time and within budget.

In closing, let me offer you a glimpse of things to come. Willamette HDL had a recent experience where our design team never visited the customer's Seattle, Wash., site. We were hired for the four-month project on a recommendation by another contract engineer. We developed and delivered a functional validation strategy, the test bench, and models for the test bench for a complex ASIC design. All communication was done via electronic mail, telephone, fax and ftp of the data. The only face-to-face meeting was by happenstance—an engineer on the project vacationing in Portland, Ore., stopped in to meet us.

Contributed by Mike Baird, president, Willamette HDL, Beaverton, Ore. For more information on this topic, see the company's web site at www.whdl.com.

tos, director of design services marketing, Cadence Design Systems, San Jose, Calif., explains, "If you are a world leader in televisions and want to go into the communications market, but know nothing at all about communications, you might go to a design service provider to help you learn about this particular technology area."

In fact, design services are being viewed by CEOs as a tool to help accelerate business plans. As Michael Burstein, president, Gambit Automation Design, San Jose, Calif., explains, "It's analogous to the concept behind manufacturing facilities. You don't wait until you can do everything needed to get a product to market, like manufacture it, to start a company. You simply find a company to do the manufacturing for you."

Another benefit of design services stems from the idea that purchasing and maintaining design methodologies, including hardware platforms and specific EDA design tools, is time-consuming and costly. Many smaller companies simply don't have the needed resources. As an alternative, the company can establish its core competency and utilize design services organizations to add value through specialization with different design processes and the use of design tools.

One difficulty that companies are facing is maintaining a well-qualified staff of engineers who are current with the latest technologies. Besides the shortage of qualified engineers, many long-time company employees who do the same thing year after year tend to grow stagnant. In effect, they get "cubby holed" and lose their competitive edge. Often, it is not even by their own choice; they just don't have the time to learn new skills. Because they specialize in using the latest and best EDA tools and work on cutting-edge designs, design services providers are forced to keep abreast of technology and tool developments to remain successful.

It is often less expensive to hire a design services organization than a staff of captive designers. While designers are crucial during the company's peak time when developing a commercial product, what happens during the downtime when product development has ended? It some cases, it may be cheaper to maintain a small staff of designers and farm out portions of the design during peak times. Even when companies have the financial resources to hire engineers for a particular project, they sometimes don't want to make the long-term commitment of carrying these employees through the company's downtime. Of

The ABCs Of Design Service

Design service is defined as any type of service provided to a company toward the development, testing, or manufacturing of a product. It entails the execution and nuts and bolts of a design, as well as the knowledge of how to drive a design. Design service organizations use EDA tools and other tools such as mechanical computer-aided design (MCAD), to design ICs, packages, pc boards, and multichip modules (MCMs).

Tom Beckley, president and CEO, Xynetix, Fishers, N.Y., explains that "there is a distinction between design services and EDA professional services that are generally focused on promoting the use and deployment of EDA products. For instance, Xynetix focuses on implementation services (fast-track consulting, etc.), process optimization services (assessment and flow recommendations coupled with process characterizations), and knowledge transfer services (product training/tutorials and advanced tool implementation programs), but I wouldn't call these design services."

The type of design work farmed out to a design service organization depends on a company's need, or lack of expertise in a particular area of design. Typically, most of the work done by design service organizations focus on the layout portion of a design as it tends to be less mission critical. This often includes, as Mike Baird, president, Willamette HDL, Beaverton, Ore., explains, "the minor or well-defined pieces of the actual design work, design verification and testing, some QA activities, model development, and physical layout work. In addition, we see companies bringing in 'experts' on the process side of things to consult when such expertise is lacking in the company. This is done usually with the goal of building up this expertise in house for subsequent projects." On the other hand, architecture, logic design, and product planning, are often kept in-house, as this constitutes the core knowledge of a company's business and technology.

There are as many different types of design services as there are design services organizations. Larry Saunders, principal, SEVA Technologies, San Diego, Calif., divides it into four different categories: the independent consultant, body shops, small service companies, and captive consultant groups. Saunders says that "the body shops operate in much the same way as an employment agency; they place designers in a specific company for a set contract period. The next step up from this is when the designers working at these 'agencies' have gained enough of a reputation to get jobs on their own. These people typically go off and start there own design services companies consisting of a small number of designers that take on service projects. The captive consultant groups—the largest type of design service organization—consists of companies like Cadence and Mentor Graphics."

While each these four different types of design service organizations have their own unique methods of operation, there are two trains of thought on how to approach the task of providing design service. In one approach—outsourcing—engineers are either sent into a company to do design work on-site as part of the company's design team, or the company provides the design service organization a design description or netlist which it then uses to complete the assigned task at its own facility. With the second approach—knowledge sourcing, as coined by Mentor Graphics—design service organizations work hand in hand with a company to not only help it complete a design, but teach its designers how to do the design task for themselves should the need arise in the future. Regardless of which approach is espoused by a design service organization, they all have the same end goal: to hire themselves and their expertise out to companies at a price.


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CAS latency		2, 3		
Burst length		1, 2, 4, 8, full page		
Speed grade (Frequency)		-70 (143MHz), -80 (125MHz), -10 (100MHz)		
Supply voltage		3.3±0.3V		
Interface		LVTTL/SSTL_3		
Refresh cycle		4K/64ms		
Package		54-pin, 400-mil TSOP (II)		

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course, as Cadence points out, the decision to utilize design services is not always related to cost, but rather time, measured with regard to the value of gaining a significant market share by getting to market first.

For those companies not concerned with cost, design services can provide a unique competitive advantage. A company totally driven by time-to-market, for example, might farm out a design to more than one service provider. The first provider to deliver a chip goes directly to fabrication. It's a win-win situation for all involved. The company gets its product to market quickly, and all the service organizations get paid for their efforts.

Not to be forgotten is the benefit to EDA tool vendors. A design service provides EDA tool vendors with a way to expand their businesses by getting in on the ground floor of an industry that, by all accounts, is still in its infancy. More importantly, next-generation EDA tools cannot be developed in a vacuum. Design services offer opportunities for tool vendors to work with other designers to see how they use existing tools, what they would like to see in future tools, and what their future tool needs will be. Gambit's Michael Burstein explains that this is a crucial benefit since "in the future, EDA tool vendors offering design services will differentiate themselves by the advanced tool technology they offer, and the development of this technology will be aided through insight gained in the design service projects in which they participated."

Risks Of Use

There are risks that any potential user should know about prior to making the decision to farm out part or all of a design. One of the most common and potentially disastrous risks is hiring a design services organization that does not have appropriate experience. Although one might assume that by simply checking resumes for past successes and experience this problem could be avoided, nothing could be farther from the truth. Part of the problem, as Larry Saunders, principal, Seva Technologies, San Diego, Calif., explains, is that "there are no licenses required for this type of work, and most consultants would rather die than tell you they can't do something." In many cases, by the time a company finds out that the design services organization it hired can't get the job done, it's often too late, and it has already missed its time-to-market window of opportunity.

While lack of experience is more of a risk when dealing with one-man operations, it's a risk every potential user of design services should be on the lookout for. And, how does a company looking to hire a design services organization protect themselves? As Saunders explains, "The customer needs to verify the service provider has done what he claims he can do. This means conducting a skillfully positioned interview. You can't just look at a resume. Instead, ask the service provider for an interview and ask them to demonstrate their skills. For example, ask them to write the code that describes a flip-flop acceptable to a Synopsys tool, or ask to see a sample of a particular design task. You will know fairly quickly whether or not they can do what they claim." If the provider has overestimated his skill, at least you will have found out up front, before investing time and money in a proposition that will likely not turn out as planned.

According to Synopsys, Mountain View, Calif., "in traditional design services, the largest risk is around design ownership and its retention. The legal issues regarding intellectual property (IP) and residual ownership must be fully explored and security guaranteed. Clearly, customers are concerned that the design services company is in a position to enable their competition." Many companies with their own in-house design groups fear that by farming out part of a design, they will lose control of the technology. While this may be true to an extent with traditional outsourcing design services, most companies solve the problem by keeping their core competencies in-house. Another way around this risk is to use a knowledge source-based design services organization such as Mentor Graphics.

Assuming you hired a properly skilled service provider that protects your core competencies, the next step is to ensure that it's not so overwhelmed with other projects that yours will be "put on the back-burner." If the service provider is overloaded, it may lack the resources to complete the task or mismanage the job altogether; neither of which are ideal scenarios for a company fighting huge time-to-market pressures.

Another difficulty that might arise is if either the company hiring the service provider or the provider themselves underestimates the magnitude of the task. As MMC Network's Sena Reddy explains, "Some engineers are brilliant; everything to them is simple, but to everyone else on the team, it's not. If the effort needed to complete a task by all

Companies Listed In This Report

Cadence Design Systems
555 River Oaks Pkwy.
San Jose, CA 95134
(408) 943-1234
www.cadence.com
CIRCLE 553

Gambit Automated Design
1101 S. Winchester Blvd.
Suite C-120
San Jose, CA 95128
(408) 345-3555
gambit@gambit.com
CIRCLE 554

Mentor Graphics
8005 S.W. Boeckman Rd.
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www.mentorg.com
CIRCLE 555

MMC Networks, Inc.
1134 E. Arques Ave.
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www.mmcnet.com
CIRCLE 556

Praegitzer Industries Inc
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Dallas, OR 97338
(503) 623-9273
www.pii.com
CIRCLE 557

SEVA Technoloies
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Suite D
San Diego, CA 92129
(619) 538-6283
www.seva.com
CIRCLE 558

Synopsys Inc.
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Mountain View, CA 94043
(415) 962-5000
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CIRCLE 559

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Ste 625
Beaverton, OR 97005
(503) 590-8499
www.whdl.com
CIRCLE 560

Xynetix Design Systems
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Fishers, NY 14453
(716) 924-9303
www.xynetix.com
CIRCLE 561

members of the design services team is not well assessed prior to starting the job, the potential for job failure is high."

According to Willamette HDL's Mike Baird: "The biggest risk a design services user faces is that the service company does not deliver what the user wants. This can be a nondelivery either in terms of time-frame or in quality, or even what was needed. Interestingly enough, if you talk to the design services companies regarding those projects, you would find that often they would point back to the hiring company as providing poor or changing requirements, or just simply not providing adequate information."

One way to minimize this risk is by ensuring a good line of communication between the service provider and the hiring company. Having technically competent engineers for a given project isn't enough for a service company. What's also needed is strong project management that will facilitate communication with the hiring company. In fact, the design services industry, realizing the importance of good communication, has resorted to the use of milestones to address this risk. In this manner, risk mitigation can be built directly into the project contract to protect both the hiring company and the service provider.

Another reason why companies may be leery of utilizing design services is the fear of the "sales pitch." Some worry that approaching a captive consulting group for design services might result in pressure to buy the vendor's EDA tools. But this usually is not the case. Most EDA tool vendors offering design services are fully prepared to work with whatever design methodology and tools the company has embraced, regardless of where they came from. As Cadence's Peter Santos points out, "This is the only way to operate since most clients still work with a best-in-class mentality which means that they typically have tools from a number of different vendors. To be successful, we have to be able to work with all of them."

And, in fact, there is some advantage in going to the vendor that sold you a tool for design services; after all, who would be better at trying to squeeze as much performance as possible out of the tools if not the tools' inventor themselves? And, if the reason a company wants to use design services is to get their EDA tools working or with help in running their tools, then going to the tools vendor would be a logical move. On the other hand, if the problem is to design an ASIC, then a company might want to go to an independent contractor or a small design service organization. The choice of what type of design service organization a company employs comes down to the company's need.

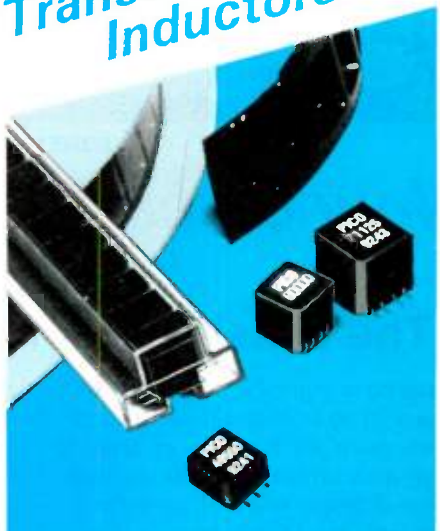
Service Costs

Pricing for design services is a difficult subject to broach. If the service providers can complete their task, such as verifying a design to get it to market as quickly as possible, then the company that hired them stands to make a substantial amount of money. But how do you charge for this service? In a perfect world, what many service providers would like to receive as payment is a percentage of what their customers save by using their service. Unfortunately, this is not always the case. In fact, there really is no set business model for the price of this type of service.

What most service organizations end up charging is based on a host of factors that include the hiring company's culture, value-based pricing, and time and materials needed to complete a task. Some design service organizations offer a fixed fee but, generally, it's for specific services that have been and are done many times. Others charge on a results-based model, whereby the customer pays the service organization as certain milestones are achieved. In general, it's safe to say that most pricing today is customized to a customer's particular needs and requirements.

The Bottom Line

While the design services industry has come a long way since its beginnings as a means of helping customers understand and run EDA tools, its present incarnation is still just scratching the surface of a market that's expected to grow. More companies will begin to use design services for assistance with the design process. The trend is already prevalent in certain areas of EDA such as pc-board design, where, for example, many companies farm out pc-board layout for their boards. But, as Steve Smith, vice president, Praegitzer Design, Dallas, Ore., points out, "While more companies are getting on the outsourcing bandwagon, higher-end companies still tend to keep everything inside."



MEETINGS

APRIL

DSP World Spring Design Conference, Apr. 21-23. Santa Clara Convention Center, Santa Clara, California. Contact Liz Austin, Miller Freeman Inc. (888) 239-5563, (415) 538-3848; e-mail: dspworld@mfi.com; www.dspworld.com.

Southeastcon '98, April 24-26. Hyatt Regency, Orlando International Airport, Orlando, Florida. Contact Parveen Ward, ECE Dept., University of Central Florida, Orlando, Florida 32816; (407) 823-2610; fax (407) 823-5835; e-mail: pfw@ece.engr.ucf.edu.

16th IEEE VLSI Test Symposium, Apr. 26-30. Hyatt Regency Monterey, Monterey, CA. Contact Rob Roy, Intel Corp., MS:JFT-102, 5300 Elam Young Pkwy., Hillsboro, OR 97124-6497; (503) 264-3738; fax (503) 264-9359; e-mail: robroy@ichips.intel.com.

IPC Printed Circuits Expo '98, Apr. 26-30. Long Beach Convention Center, Long Beach, CA. Contact Dan Green, The Institute for Interconnection & Packaging Electronic Circuits, 2215 Sanders Rd., Northbrook, IL 60062-6135; (847) 509-9700 ext. 371; fax (847) 509-9798.

MAY

100th ACerS Annual Meeting & Exposition, May 3-6. Dr. Albert B. Sabin Convention Center, Cincinnati, Ohio. Contact The American Ceramic Society Customer Service Dept.; (614) 794-5890; fax (614) 899-6109; e-mail: customersrvc@acers.org; www.acers.org.

Conference on Lasers & Electro-Optics & The International Electronics Conference (CLEO/IEC), May 3-8. The Moscone Center, San Francisco, CA. Contact Amy Hutto, OSA Conference Services, 2010 Massachusetts Ave. N.W., Washington, DC 20036-1023; (202) 416-1980; fax (202) 416-6100; e-mail: cleo.info@osa.org.

IEEE International Conference on Evolutionary Computation, May 3-9. Ankorage, AK. Contact Patrick K. Simpson, Scientific Fishery Systems Inc., P.O. Box 242065, Anchorage, AK 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@alaska.net.

EDA WATCH

Understanding The Roles Of CSM, PDM, And ERP In Product Development

The world of product manufacturing has undergone a revolution in recent years. Consumers can claim credit for a big part of it, with their disdain for yesterday's technology and their incessantly growing appetite for the fastest, latest, and greatest stuff.

Product leadership is now measured in months instead of years, which has led to the incredible shrinking product lifespan. As Eric Upin, a principal of market analysis firm Robertson, Stephens & Co., recently said, "Products have become like produce: If they don't get to market quickly, they rot and become useless." To shrink design cycles sufficiently, we must increase the amount and reuse of third-party components, and increase design reuse.

Three Key Systems

Bridging the design, manufacturing, and procurement groups are three key information management systems: Component and Supplier Management (CSM), Product Data Management (PDM), and Enterprise Resource Planning (ERP). These systems enable the three organizations to share data and collaborate intelligently on the all-important task of bringing quality products to market quickly and cost-effectively. To accomplish this task though, it is important to understand not only the roles of each of these systems, but how they can work together to dramatically reduce product costs, improve quality, and cut time to market.

While all three systems span the product lifecycle, each system plays a primary role at a particular point. In the ideal manufacturing environment, the systems are closely integrated, yet each is still a very independent entity.

CSM systems bridge the gap between design and procurement. They provide decision support software and content databases to help designers select optimal parts based on both business and technical criteria, and to promote the reuse of designs as well as preferred parts. They also provide procurement staff with the means to manage parts and suppliers, to consolidate vendors, to realize volume discounts, and to source from a point-of-need. CSM systems complement the transaction-oriented PDM and ERP systems.

PDM systems link design and manufacturing. They enable management of product data vaults and structures and configurations, and ensure that the right design information is conveyed to manufacturing at the right time. They manage the key release and engineering change orders (ECOs) that move the product throughout its lifecycle.

ERP systems bridge manufacturing and procurement, ensuring that procurement provides the right quantities of the right parts at the right times to the right factories. Typical functions within ERP systems include order entry and purchasing execution, inventory management, master production scheduling, materials requirements planning (MRP), and workload and capacity planning.

Where The Savings Begin

The pervasiveness of components in finished products means that a CSM system can make or break manufacturers. In some industries, the component choices designers make in the first 10% to 20% of the design cycle lock in 70% to 80% of end product costs. Studies have shown that it costs only $1 to make a change in the conceptual phase of a product. But this cost rises to $10 during the simulation or analysis stage, $1000 during prototype testing, and $10,000 once the product gets to manufacturing. Clearly, choosing the right component the first time around is critical to keeping costs down and squeezing through the ever-shrinking market windows.

But that's only part of the cost story. The industry average for introducing a new part into the system—including testing; supplier evaluation; management approval; incoming inspection; adding to stock inventories; and entering specifications, schematics, and system documentation—ranges from $15,000 up to $25,000, with a complex component that requires design libraries and test procedures costing up to $250,000. In many companies with less-than-optimal CSM systems, 5% to 10% of the total parts in the company's database—amounting to tens of thousands of parts—are exact duplicates or functionally equivalent parts. Multiplying out the loss is a painful ordeal.

A strong CSM system is critical to cutting time-to-market. It is estimated that designers spend, or waste, 10% to 30% of their time using inefficient CSM tools, digging through bulky paper databooks with inconsistent data and hard-to-compare parts lists. Or, they could be struggling with CD-ROM systems which are difficult to access enterprise-wide and tough to keep up-to-date. This is time that manufacturers can ill afford to waste in their race to market.

Keeping Products On Target

PDM systems provide a tool to organize and manage product information. They also provide workflow features to route designs to appropriate individuals for sign-off.

By organizing product development information and processes, PDM systems cut product costs by managing and automating the engineering review and release and change processes. They also reduce manufacturing errors and cycle time by ensuring that the latest, most current product information is accessible. This is especially important in today's global environment where engineering groups and factories are geographically dispersed.

The ideal manufacturer has tightly integrated his PDM and CSM systems. According to Ed Miller, president of analyst group CIMdata, "A tight integration between PDM and CSM means greatly enhanced help is provided to engineers at the right time in the change process. CSM systems [help] engineers search, compare, and select the best components from the best suppliers up-front, avoiding downstream waste and unnecessary ECOs," says Miller. He con-

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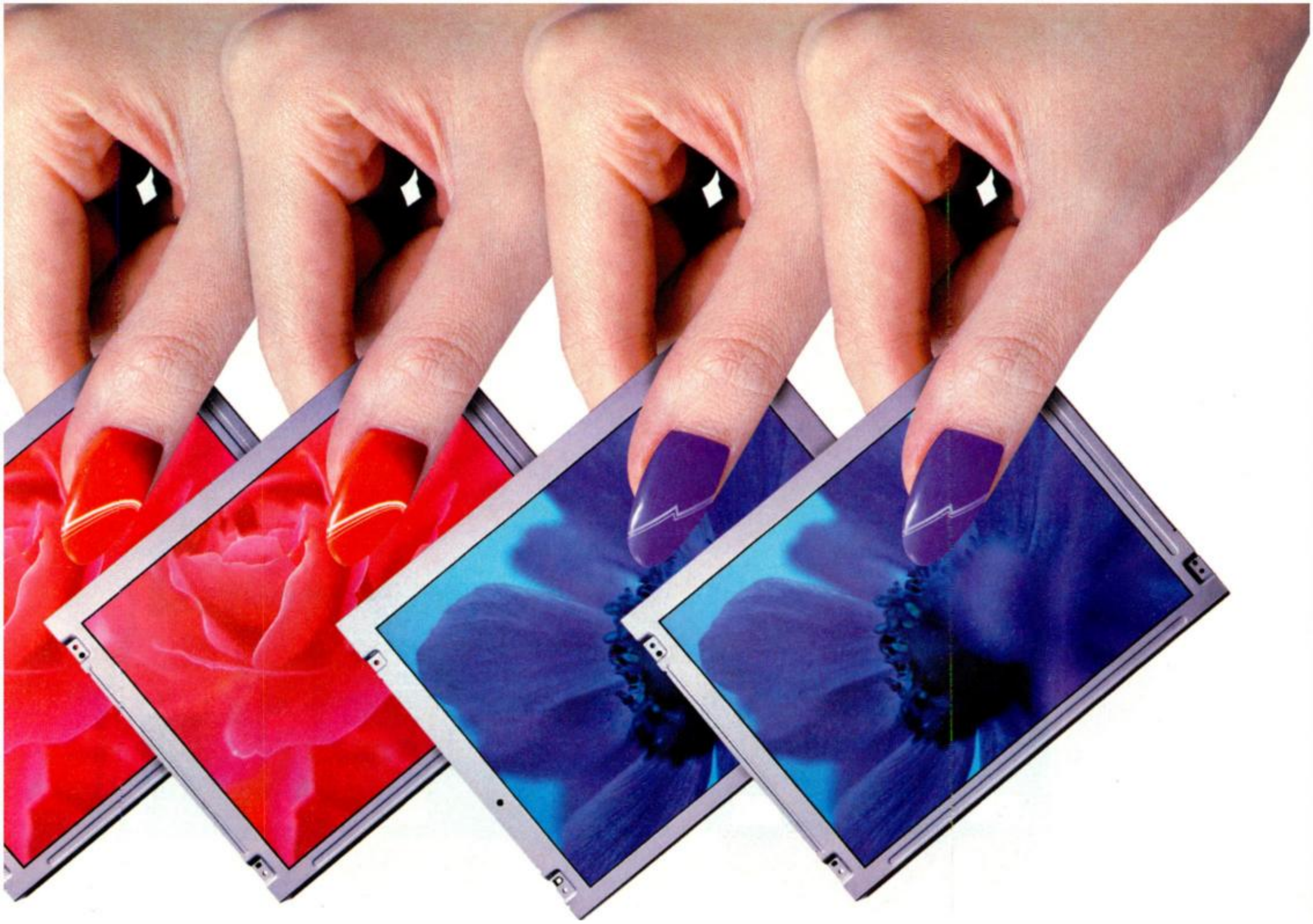
Our analog-interface models are ideal for standalone LCD monitors. Featuring unique technology for analog signal processing from input to driver, our analog-interface screens give you full color with continuous gray-scaling. To slash your development time and cost, we provide CRT monitor-compatible interface boards. They permit direct connection with your computer's standard RGB monitor interface. Analog technology also reduces EMI. For demanding applications, our "Super-

On the Internet at http://www.ic.nec.co.jp/compo/lcd/index_e.html

For fast answers, call us at: USA Tel:1-800-366-9782.Fax:1-800-729-9288. GERMANY Tel:0211-650302.Fax:0211-6503490. THE NETHERLANDS Tel:040-445-845.Fax:040-444-580. SWEDEN Tel:08-638-0820.Fax:08-638-0388. FRANCE Tel:1-3067-5800. Fax:1-3067-5899. SPAIN Tel:1-504-2787.Fax:1-504-2860. ITALY Tel:02-667541. Fax:02-66754299. UK Tel:1908-691133.Fax:1908-670290. HONG KONG Tel:2886-9318.Fax:2886-9022. TAIWAN Tel:02-719-2377.Fax:02-719-5951. KOREA Tel:02-551-0450.Fax:02-551-0451. SINGAPORE Tel:253-8311.Fax:250-3583. AUSTRALIA Tel:03-8878012.Fax:03-8878014. JAPAN Tel:03-3798-6148.Fax:03-3798-6149.



Super-Fine TFT
Analog interface
14.1" screen
1024 x 768 pixels
Full color
Ultra-wide viewing angle
NL10276AC28-02

Analog interface
14.1" screen
1024 x 768 pixels
Full color
NL10276AC28-01

Digital interface
15" screen
1024 x 768 pixels
262,144 colors
NL10276AC30-04

Digital interface
14.1" screen
1024 x 768 pixels
262,144 colors
NL10276AC28-05

# of interface, size and color

Fine TFT™ screens feature a radically expanded viewing angle of ±80 degrees, up/down and left/right.

Digital-interface models

If you're designing a desktop PC with integrated LCD screen, our digital-interface models are the optimum solution. They feature a low voltage differential signaling interface (LVDS), and display 262,144 colors.

NEC is the only vendor who offers both analog- and digital-interface models. Whatever your requirements for systems, we have a TFT LCD screen that will make you look your best. For more information, contact NEC today.

The right components to build your reputation

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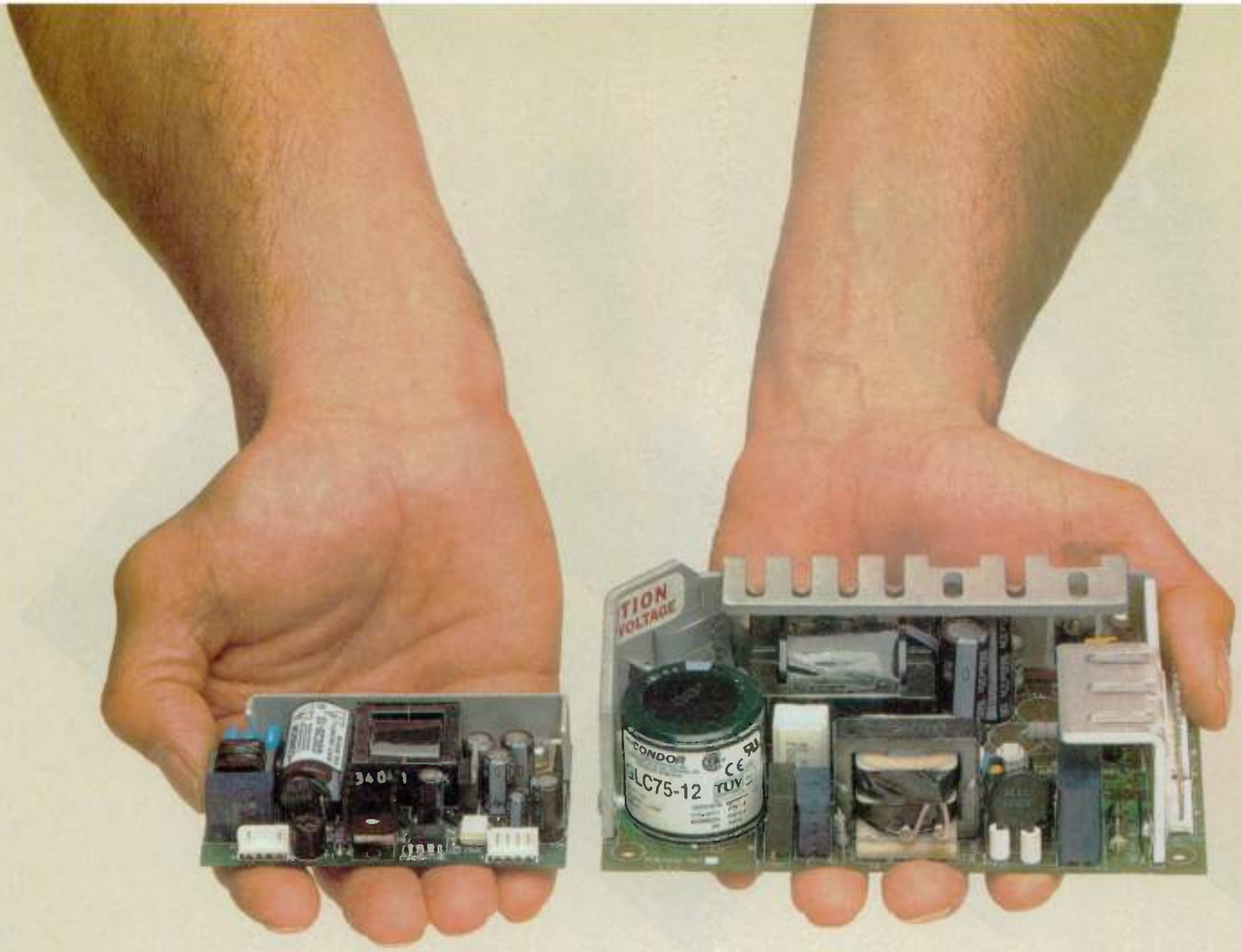

On one hand...

We introduced the GSC20–the world's smallest 20-watt D.C. switcher.

- Extremely small footprint—no bigger than a business card (only 2.00" x 3.50" x 0.68")
- 90-264VAC input
- EMI FCC Class B, CISPR22B
- Standard overvoltage protection
- Fixed-frequency operation
- Approved to UL 1950, IEC950, CSA 22.2 No. 234 Level 3 and EN60950
- Full burn-in; 2-year warranty

An ISO 9001 Certified Company

On the other hand...

Our new, 110-watt GLC75 is another compact innovation!

- High-density, small footprint (just 3.40" x 5.75" x 1.56")
- Five single-output models (5 to 28 volts)
- Power-fail signal *standard*
- Universal input: 90-264VAC
- Built-in EMI filtering to FCC Class B, CISPR 22B
- Overload protection with auto restart
- Optional "L" bracket available
- 2-year warranty
- Approved to UL 1950, IEC950, CSA 22.2 No. 234 Level 3 and EN60950
- CE marked to LVD

Call Condor today for a free catalog on our full line of D.C. power supplies, including the industry's largest selection of medically approved switchers and linears.

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tinues, "PDM systems reduce ECOs by managing and automating the product release and change processes, and integrating them with full product configurations."

Right Place At The Right Time

Once a product goes into production, the manufacturing systems take over. What were formerly known as materials requirements planning (MRP) systems are now modules of larger ERP systems.

ERP's mission is to manage the procurement and delivery of components, raw materials, and other resources to the right place at the right time. They leverage demand forecasting and order scheduling to ensure high customer satisfaction, minimum inventories, and maximum factory productivity at the lowest possible cost.

Systems Integration

While there have been attempts to extend the capabilities of ERP and PDM systems into CSM, to date these have been costly and inadequate. Why? The fact that the first iteration of Aspect's VIP Reference Database required some 500 person-years of development shows a sense of the resource commitment required for an effective system. It's a massive effort, not to be undertaken lightly. For the manufacturer, this means they must obtain the best CSM, PDM, and ERP systems, and integrate like crazy.

Today there are many CSM, PDM, and ERP processes underway in corporations all around the world. Design reuse alone is saving companies thousands of designer hours and millions of dollars. CSM, PDM, and ERP have proven themselves critical tools for success in the lightning-paced market of the late.

Contributed by James Althoff, senior vice president and chief technology officer for Aspect Development Inc., Mountain View, Calif. He holds a BS in Mathematics from Florida State University and an MS in computer science from the California Institute of Technology.

For more information, check out Aspect Development's web site at www.aspectdv.com, or contact Larry Rice at 650-526-3329.

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READER SERVICE 243

Novel Data-Management System Helps Facilitate Design Project Flow

Virtually nothing is more time-intensive during the design process than data management. It's a burdensome, often monotonous task that most designers dread. Unfortunately, it's unavoidable, and is key to getting a product done right the first time. Offering a different approach, ACCEL Technologies, San Diego, Calif., recently introduced ACCEL PDM (Product Data Management). It's a web-based product data-management software system that consists of individual solutions for managing product data and design project flow. The system also aids in file distribution.

Debuting initially from the ACCEL PDM system are ACCEL Design Flow, a tool for project management and reporting; and ACCEL View Center, a tool that offers web-based access, viewing, and distribution of design files. Additional solutions are expected to be released during 1998, and they will focus on other PDM problem areas. Not only will they home in on EDA-related data management issues, but those pertaining to industry sectors such as financial services, health care, textiles, lumber, and a host of others.

The ACCEL Design Flow tool relieves much of the burden of product data documentation by tracking projects (along with their associated tasks), and the flow of data, throughout the design cycle. Because it gives multiple design teams on demand equal access to the same data files, it's ideal for networked users. The Design Flow tool defines projects by a set of tasks and sub-tasks that must be accomplished for the project to be complete.

The ACCEL View Center complements the Design Flow tool by creating a custom Intranet web site. The site manages distributed access of design files for a variety of viewing functions. Files stored at the Intranet site are in either a native schematic and PCB file format, or a standard PDF file format.

Both the ACCEL Design Flow and ACCEL View Center offerings from the ACCEL PDM system are available now. A native 32-bit application, ACCEL PDM operates on the Windows 95 or Windows NT platforms. The Design Flow may be licensed for network use.

Pricing depends on tool configuration. Contact ACCEL Technologies directly for specific pricing information.

ACCEL Technologies, Inc.
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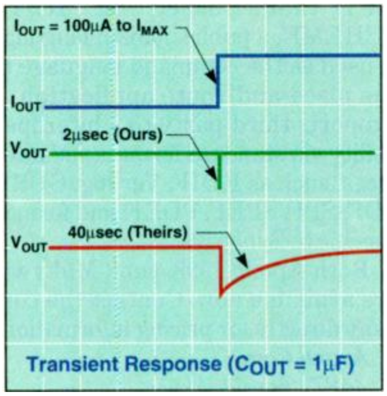
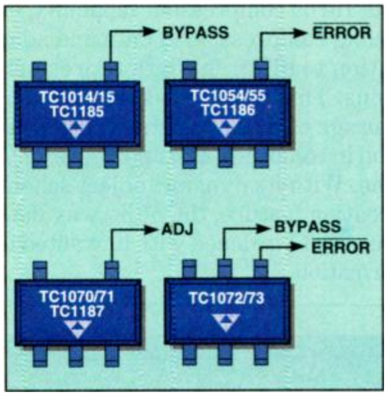
CHERYL AJLUNI

TelCom's New CMOS LDOs vs. Bipolar LDOs... No Contest

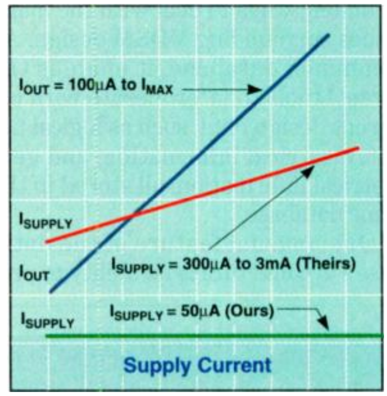
FASTER!



SMARTER!



LOWER POWER!



TELCOM SEMICONDUCTOR, INC. LOW-OUTPUT CURRENT LINEAR REGULATORS

Wasting Battery Current!

TelCom Semiconductor, Inc.'s CMOS LDO family supersedes a wide variety of popular bipolar regulators, delivering superior performance at lower supply current levels. They deliver equal or better performance as their bipolar equivalents, at ***significantly higher levels of efficiency***. A typical bipolar regulator has ground currents equal to 1 to 2 percent of the output load, whereas TelCom's LDOs have zero ground current, ***resulting in total operating current orders of magnitude lower than their bipolar counterparts.***

TelCom's LDOs can be placed in a shutdown mode, further enhancing their effectiveness in low-power applications. In shutdown, ***the regulator's total current draw, including input current on the Shutdown pin, is less than 0.5µA***. The Shutdown pin's input leakage current on a bipolar regulator alone can be as high as 15µA!

This low-power operation makes TelCom's family of LDOs ***ideal for upgrading*** bipolar LDOs in cellular phones, pagers, PDAs, laptops, hand-held meters, and other portable applications.

TelCom's LDOs are available with fixed or adjustable outputs, ***supporting load currents up to 50mA, 100mA and 150mA***. They also are available in space-saving SOT-23-5 and SOT-23-6 packages, making them ideal for applications in tight quarters. Shutdown capability, thermal protection, and current limiting are standard in every device. ***Adjustable output, Error Flag, and noise bypass capability are provided on select devices.***

For more information call us at: 1-800-888-9966 or Visit us on the Web at: http://www.telcom-semi.com

Part #	Shutdown	Reference Bypass Input	Error Output	Adj.	Package Options	Output Voltage* (V)	Max. Output Current (mA)	Max. Input Voltage (V)	Active Supply Current (Typ. µA)	SHDN Current (Typ. µA)	$V_{DROPOUT}$ @ Max. I_{OUT} (Typ. mV)	Output Voltage Accuracy (Typ. %)
TC1014	√	√	—	—	SOT-23A-5	2.5, 2.7, 2.85, 3.0, 3.3, 3.6, 4.0, 5.0	50	6.5	50	—	85	±0.5
TC1015	√	√	—	—	SOT-23A-5	2.5, 2.7, 2.85, 3.0, 3.3, 3.6, 4.0, 5.0	100	6.5	50	0.05	180	±0.5
TC1054	√	—	√	—	SOT-23A-5	2.5, 2.7, 2.85, 3.0, 3.3, 3.6, 4.0, 5.0	50	6.5	50	0.05	85	±0.5
TC1055	√	—	√	—	SOT-23A-5	2.5, 2.7, 2.85, 3.0, 3.3, 3.6, 4.0, 5.0	100	6.5	50	0.05	180	±0.5
TC1070	√	—	—	√	SOT-23A-5	2.2 → V_{IN}	50	6.5	50	0.05	85	—
TC1071	√	—	—	√	SOT-23A-5	2.2 → V_{IN}	100	6.5	50	0.05	180	—
TC1072	√	√	√	—	SOT-23A-6	2.5, 2.7, 2.85, 3.0, 3.3, 3.6, 4.0, 5.0	50	6.5	50	0.05	85	±0.5
TC1073	√	√	√	—	SOT-23A-6	2.5, 2.7, 2.85, 3.0, 3.3, 3.6, 4.0, 5.0	100	6.5	50	0.05	180	±0.5
TC1185	√	√	—	—	SOT-23A-5	2.5, 2.7, 3.0, 3.3, 5.0	150	6.5	50	0.05	270	±0.5
TC1186	√	—	√	—	SOT-23A-5	2.5, 2.7, 3.0, 3.3, 5.0	150	6.5	50	0.05	270	±0.5
TC1187	√	—	—	√	SOT-23A-5	2.2 → V_{IN}	150	6.5	50	0.05	270	—

Note: *Custom Output Voltages Available – Contact TelCom Semiconductor, Inc.

TelCom Semiconductor, Inc.

Analog & Mixed Signal

1-800-888-9966

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READER SERVICE 194

(continued from page 91)
to finding ways to deal with the many issues surrounding VDSM design. As a common database, it enables the Avant! tools to interoperate with coherent design data, such as logical net list, electrical information, and geometrical information, all stored in the same database.

One unusual feature of the database's architecture is its ability to preserve point tool performance. It also has Turbo compression capability, enabling compression of data and adaptation to different data representations. This feature assures efficient storage of massive parasitic information in compressed binary representation. With its dynamic object scheme creation feature, the Milkyway database isn't burdened with unwanted information.

Milkyway offers a user-friendly GUI that's based on Tcl/Tk. SCHEME, a public domain language, is used as the command language by the place-and-route application. It supports third-party tool interoperability via standard formats and interfaces, such as EDIF, Verilog, GDSII, SDF, SPF, SPEF, PDEF, and formats specific to Synopsys.

Both Apollo 1998.4 and Milkyway are available now. Contact the company directly for pricing information.

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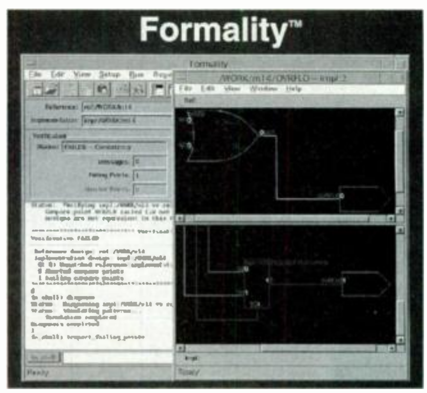
Formal Verification Tool Handles Million-Gate Designs

It's an undisputed fact that as designs increase in complexity and capacity, traditional gate-level simulation begins to fall apart. Such simulation can no longer provide a level of verification acceptable to most designers in terms of both performance and speed. This breakdown of technology has opened the door for companies who think they've a better alternative. For instance, Synopsys has unveiled a formal verification tool, called Formality, that can perform equivalence checking of million-gate SoC designs.



While other formal verification tools generally have difficulty working *(continued on page 96)*

EV KIT AVAILABLE

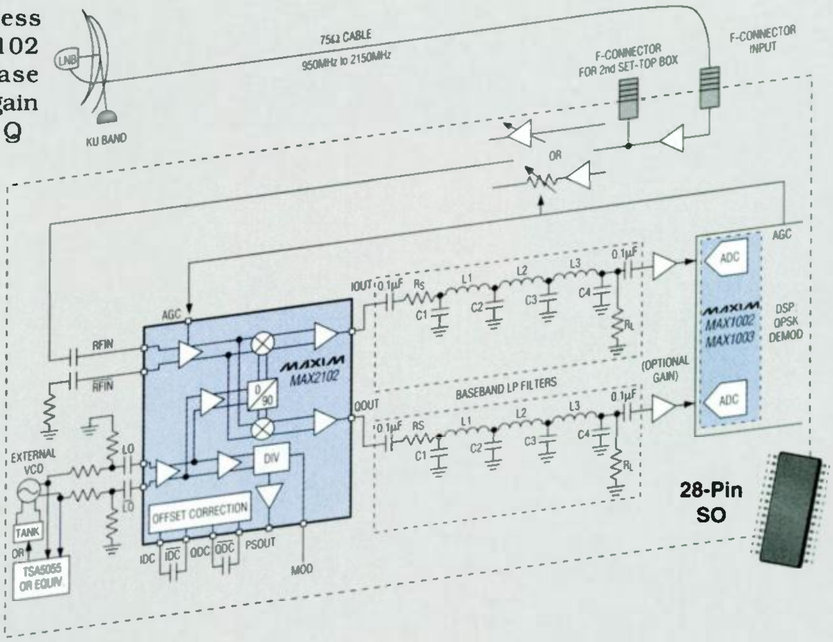
Tuner on a Chip Replaces Canned Tuners

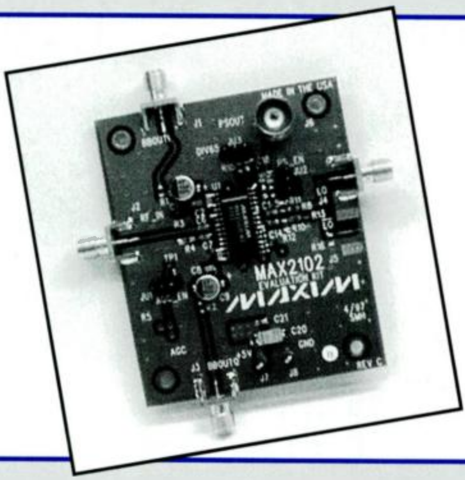
Design a Tuner Directly on Your Board

The new MAX2102 directly tunes L-band signals to baseband using a broadband I/Q downconverter. Its operating frequency range spans from at least 950MHz to 2150MHz. Included on-chip is an LNA with AGC, two downconverter mixers, an oscillator buffer with 90° quadrature generator and prescaler, and baseband amplifiers.

Designed on Maxim's GST-2 high-frequency bipolar process (with f_T = 27GHz), the MAX2102 achieves ±3° quadrature phase accuracy and less than 0.5dB gain mismatch between the I and Q channels for the entire frequency range.

An input IP3 of +6.5dBm allows a single, discrete preamplifier to serve as the interface to a 75Ω cable. The front end accepts carrier levels of -69dBm to -19dBm, and integrates a VGA with more than 50dB dynamic range. A large automatic gain-control (AGC) range is necessary to accommodate rainfall attenuation effects, differences in cable lengths, and less-than-perfect DBS parabolic-dish-antenna alignment. Channel selection in the baseband is performed by discrete, low-cost, lowpass LC filters, typically with 5th-order or 7th-order response.





Evaluation Kit Available Now!

Order the MAX2102EVKIT-SO

The preassembled and tested MAX2102EVKIT simplifies product evaluation. The board includes RF input, LO input, and I/Q baseband output SMA connectors for fast evaluation in a 50W environment. It allows testing of the 50dB AGC range, and permits observation of the dual-modulus prescaler output.

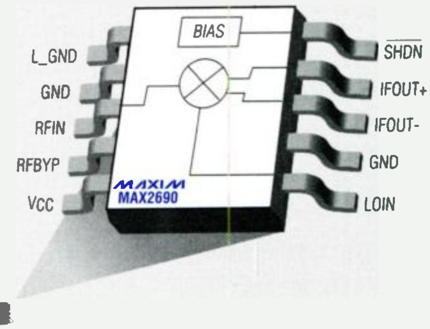
FUTURE PRODUCT

2.5GHz, +7.5dBm Input IP3, Downconverter Mixer Operates from +2.7V to +5.5V

EV KIT AVAILABLE

Designed on Maxim's 27GHz f_T bipolar process, the MAX2690* provides superior performance for wireless applications, including wireless LANs, 2.4GHz ISM, PCS, and cellular and cordless phones.

- **40MHz to 2500MHz RF Input**
- **10MHz to 500MHz IF Output**
- **+2.7V to +5.5V Supply Operation**
- **1µA Shutdown Mode**
- **High Linearity: +7.5dBm IIP3**
- **6dB to 10dB Power Gain**
- **Low Power Consumption: 15mA (independent of voltage)**
- **10-Pin µMAX Package**
- **9.5dB Noise Figure**
- **Differential IF Port**



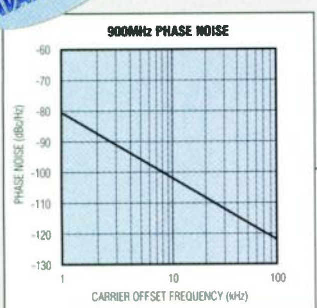
10-Pin µMAX

* Future product—contact factory for availability.

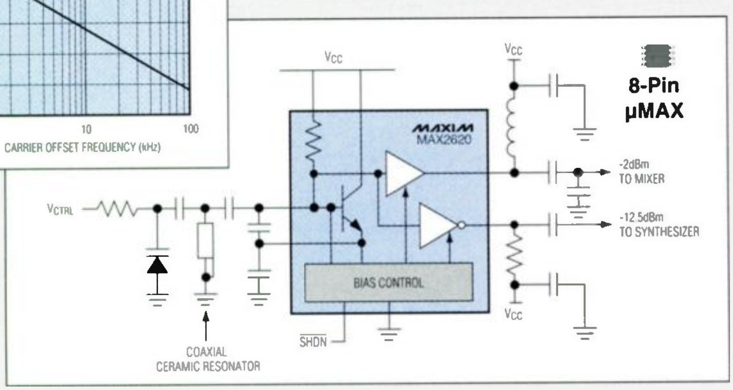
Lowest Phase-Noise RF Oscillator is Low-Cost Alternative to VCO Modules

EV KIT AVAILABLE

-110dBc/Hz Phase Noise at 25kHz Offset Suits Your 3V Cellular Phone Design!



The MAX2620 is a low-noise RF oscillator that can operate from 10MHz to 1050MHz. The oscillation frequency is set by an external varactor-controlled ceramic resonator or LC tank. The IC features a low-noise transistor, two buffer amplifiers, and biasing circuitry—including power-save circuitry that reduces the supply current from 9mA during operation to 0.1µA in shutdown mode. The MAX2620 boasts superior supply pushing of just 71kHz per volt of supply change, making it less sensitive to the sudden supply-voltage changes of TDMA systems. Its miniature 8-pin µMAX package and 3V operation make the MAX2620 ideal for portable wireless applications, such as cellular and cordless phones.



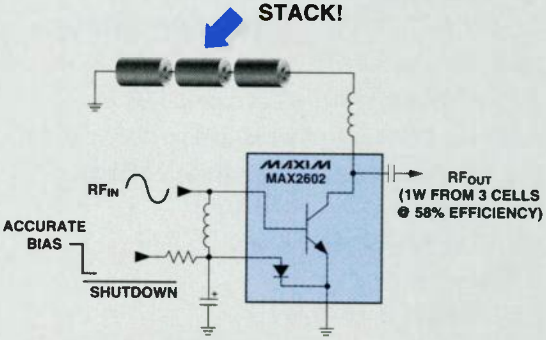
1W RF Power Transistors for True Single-Supply Operation

EV KIT AVAILABLE

Deliver 1W at 900MHz with 58% Efficiency: Eliminate Drain Switch and Negative Bias

The MAX2601/MAX2602 RF power transistors are optimized for use in portable wireless equipment operating from three NiCd/NiMH cells or one Li+ cell. Constructed with Maxim's silicon bipolar process, they eliminate the need for drain switches, negative bias generators, and power-sequencing circuitry. With 11.5dB gain at 900MHz, the MAX2601/MAX2602 are ideal as the final stage of a discrete or module class-C or class-AB RF power amplifier. They come in a thermally enhanced 8-pin SO package, allowing continuous operation. In addition to the power transistor, the MAX2602 includes a thermal- and process-matched diode, which simplifies the bias circuitry in class-AB amplifiers.

- **58% Efficiency with 3.6V Supply**
- **11.5dB Gain at 900MHz**
- **Thermally Enhanced Package**
- **Output Power: +30dBm (3.6V)**
  +29dBm (3.0V)
- **True Single-Supply Operation**



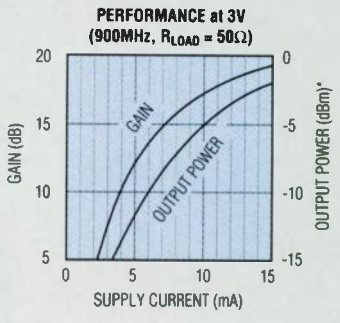
The MAX2601/MAX2602 eliminate the need for a drain switch, negative bias generator, and power-sequencing circuitry in a 1W, 900MHz RF power amplifier.

3V, 1GHz RF Amplifiers Add Shutdown and Bias Control

EV KIT AVAILABLE

Upgrade INA-30311 Designs to Save Power with a 0.1µA Shutdown Mode

Maxim's new family of 3V, low-noise wideband amplifiers offers features unavailable from the industry-standard INA-30311. The MAX2631/MAX2633 add an on-chip shutdown feature, which reduces current consumption to less than 0.1µA to save power in time-division duplex radios such as cellular, cordless, and PCS phones. The MAX2632/MAX2633 incorporate an on-chip bias adjustment feature, which allows the simultaneous control of output power, gain, and supply current with a resistor. This allows you to achieve the required gain and output power at the minimum supply current. Maxim also offers second-source wideband amplifiers for 3V and 5V applications (see table). All devices are internally matched to 50Ω and are available in tiny SOT packages.



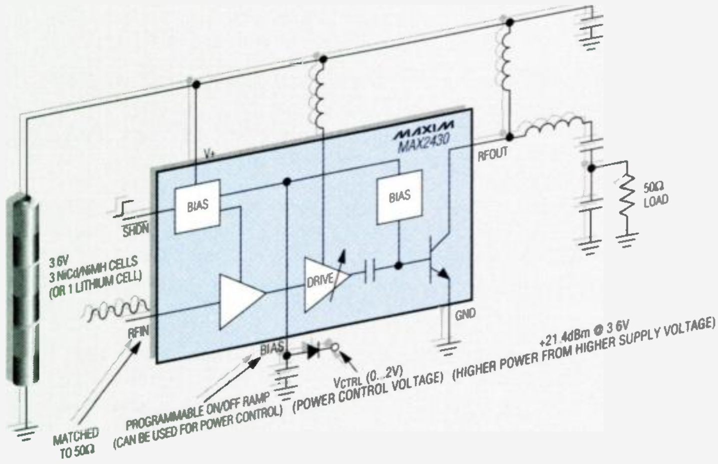
*Output power is shown at the 1dB compression point.

Part	Supply Voltage (V)	Supply Current (mA, typ)	Gain (dB) @ Frequency (MHz)	Features	Package	Industry Standard
MAX2630	2.7 to 5.5	6.6	14 @ 900	3V	SOT143	HP INA-30311
MAX2631	2.7 to 5.5	6.6	14 @ 900	Shutdown	SOT23-5	Maxim Proprietary
MAX2632	2.7 to 5.5	6.6	14 @ 900	Bias Control	SOT23-5	Maxim Proprietary
MAX2633	2.7 to 5.5	6.6	14 @ 900	Shutdown + Bias Control	SOT23-6	Maxim Proprietary

EV KIT AVAILABLE

900MHz Power Amplifier Delivers 21.4dBm from 3 Cells (3.6V)!

Power Amp Runs from +3V to +5.5V Supply: Perfect for 900MHz ISM-Band Applications and as a Predriver for Cellular Power Amplifiers



Applications Include:

- **900MHz Cordless Phones**
- **ISM-Band Applications**
- **Cellular Power-Amplifier Predriver**
- **Wireless LANs**

16-Pin Narrow SO (available now)

16-Pin QSOP (available after September 1997)

- **21.4dBm Output from 3.6V (3 Cells); 20dBm from +3V Supply**
- **Silicon Bipolar Design—True Single-Supply Operation**
- **>30dB Gain**
- **15dB Power Control Range (with 3.6V Supply)**
- **Input Matched to 50Ω**
- **Programmable RF Power-Envelope Ramp Time**
- **Logic-Level Shutdown Control (1µA Typical Supply Current)**
- **Thermally Enhanced, 16-Pin Narrow SO Package (available now)**
- **Ultra-Small 16-Pin QSOP Package (available after September 1997)**

The MAX2430 RF power amplifier operates from a +3V to +5.5V supply and delivers 21.4dBm at 900MHz from a +3.6V supply. This capability enables this low-cost device to serve as an output amplifier for cordless telephones and other ISM applications, and as a predriver for higher-power applications such as cellular telephones.

Designed for class-AB operation, the MAX2430 consists of a large power transistor driven by a capacitively coupled gain stage and a driver stage. The input impedance is matched to 50Ω (VSWR ≤ 1.5) and the overall power gain is typically greater than 30dB. To save power during the "idle slots" in time-division multiple-access (TDMA) transmissions, a TTL/CMOS-compatible command ($\overline{SHDN}$ low) can throttle the MAX2430 supply current to below 10µA.

Bypassing the BIAS input pin through an external capacitor to ground programs the RF output ramp rate during turn-on and turn-off. By applying an external voltage (from 0V to 2V) through a diode to the BIAS input pin, the maximum output power can be varied over a range of greater than 15dB.

The MAX2430 comes in a 16-pin narrow SO package. An ultra-small 16-pin QSOP packaged version will be available after September 1997.

The World's First

The Key to Making Your DECT

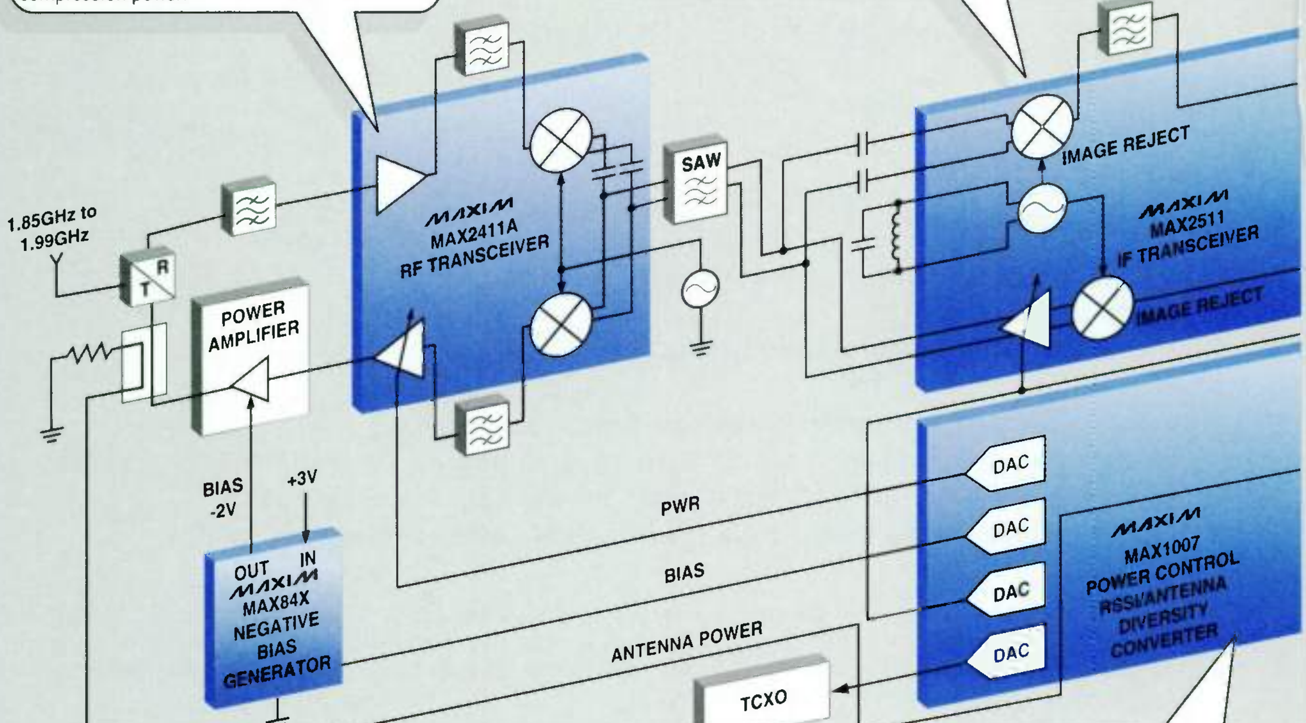
The **MAX2411A*** performs RF front-end amplification and frequency conversion in both receive and transmit modes. Its unique differential IF interface allows a single SAW filter to serve as a receive and transmit IF filter.

The MAX2411A has a 3.2dB combined down-converter noise figure and a -12.5dBm input IP3. The receive current is only 20mA with a 3.0V supply, and can be reduced below 1μA in shutdown. The transmit section includes an upconverter mixer, followed by a variable-gain power-amplifier predriver with +6dBm 1dB compression power.

The **MAX2511** performs IF frequency conversion, receive gain, transmit frequency conversion, and gain-control functions. The receive mixer input and the transmitter output interface directly to one differential SAW IF filter to save space and cost.

The low-noise receive mixer has a unique image-rejection feature to keep spurious signals or image noise from mixing to the second IF. The RSSI output has excellent dynamic range (>90dB monotonic) and linearity (±2dB error over an 80dB range).

The transmit image-reject mixer generates a clean output spectrum to minimize filter requirements. It is followed by a variable-gain amplifier with +2dBm maximum output power.



The **MAX1007*** provides for both measurement and control of numerous radio signals. Its 8-bit ADC enables peak detecting and measuring of RSSI and PS (power sense) signals. Its internal conditioning circuit converts a PS signal into a DC signal, which is then converted by the ADC. For antenna diversity, the power detector circuit compares two RSSI signals.

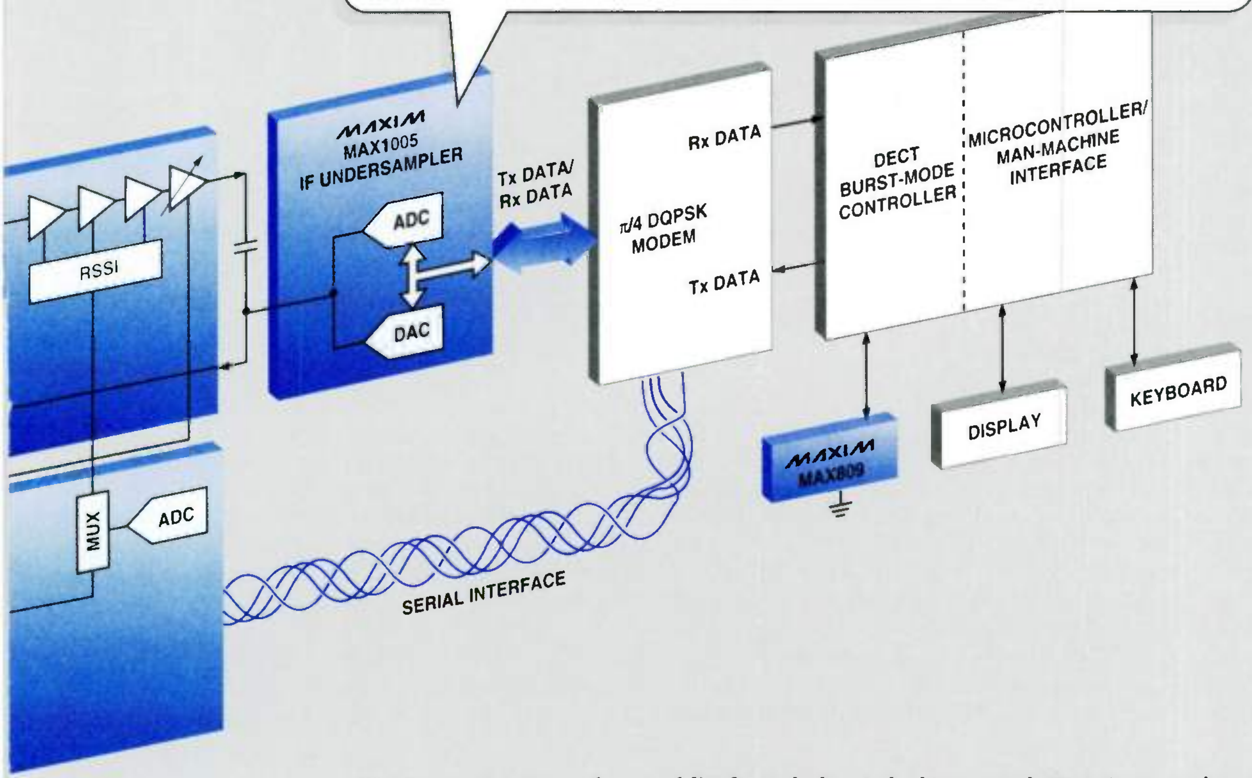
The MAX1007 also includes four DACs. XDAC is designed to tune varactor diodes, while SDAC and KDAC adjust power-amplifier output power levels. GDAC provides bias control for GaAs amplifiers. All of the DACs are double buffered, allowing for simultaneous updating of the outputs.

*Future product—contact factory for availability.

PWT1900 Chipset
Design Ready for the U.S. Market

The **MAX1005*** includes an Rx ADC and Tx DAC plus voltage reference. In Rx mode, the ADC undersamples the data signal bandwidth centered on the IF. The ADC's 15Msps conversion speed provides for 10-times oversampling of a 1.5MHz data signal. The wide input converter bandwidth provides for IFs in excess of 10.7MHz.

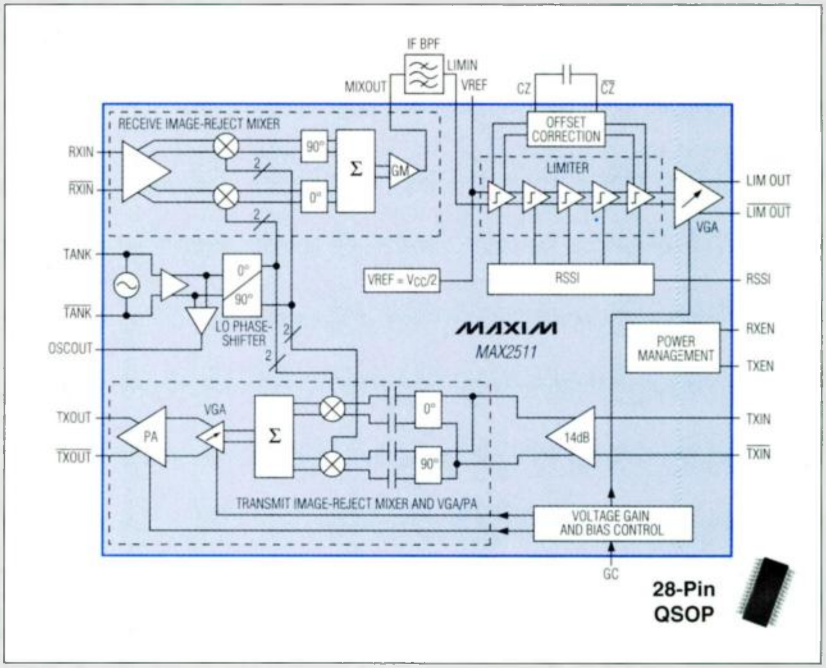
The MAX1005 requires very little power (13mA in Rx mode, 5.5mA in Tx mode) while providing a high level of signal integrity. Supply voltage operation is guaranteed down to +2.7V and multiple shutdown modes are provided, including a 1µA (max) full shutdown mode. Wakeup time from partial shutdown is just 2.5µs, providing for power savings even during short periods of idle time.



Maxim announces the world's first dedicated chipset solution to comply with the PWT1900 (TAG-6) U.S. PCS air interface standard. Based on proven DECT (Digital European Cordless Telephone) technology, the PWT1900 standard is ideal for toll-quality wireless PBX, PCS, and wireless local loop (WLL) applications. Maxim's PWT1900 chipset provides an easy-to-implement adaptation of existing DECT platforms using GFSK (Gaussian Frequency Shift Keying) to the π/4 DQPSK modulation specified in the PWT1900 standard for operation in the U.S.

EV KIT AVAILABLE

High-Integration-Level IF Transceiver has Widest Dynamic Range and Image-Reject Mixers



The MAX2511 performs the IF frequency conversion, receive gain, transmit frequency conversion, and gain-control functions in Maxim's PWT1900 chipset. The input of the receive mixer and the output of the transmit VGA (variable-gain amplifier) interface directly to one differential SAW IF filter to save space and cost. The first IF frequency can range between 200MHz and 500MHz.

The low-noise receive mixer has a unique image-rejection feature to keep spurious signals or image noise from mixing to the second IF frequency (typically around 10.7MHz). This feature allows a wideband front-end spanning over the entire U.S. PCS band without compromising performance. The mixer is followed by a wide-dynamic-range IF buffer that can drive an external filter. This signal is then fed into a limiting amplifier with 90dB of gain and a variable-gain output stage designed to drive the input of an analog-to-digital converter. The RSSI output has excellent dynamic range (>90dB monotonic) and linearity (±2dB RSSI relative error over an 80dB range).

The transmit image-reject mixer generates a clean output spectrum to minimize filter requirements. It is followed by a 40dB variable-gain amplifier, which maintains IM3 levels below -30dBc. Maximum output power is 2dBm.

An on-chip VCO with buffer amplifier further simplifies system design. Like the MAX2411A, the MAX2511 features four power-supply modes for advanced system power management. The device is available in a space-saving 28-pin plastic QSOP package.

- **Operates from Single +2.7V to +5.5V Supply**
- **Image-Reject Downconverter Mixer**
- **90dB Gain Limiting Amplifier with Adjustable Output Level**
- **RSSI Function with 90dB Dynamic Range**
- **Silicon Bipolar Design**
- **Image-Reject Upconverter Mixer**
- **+2dBm Transmit Amplifier with 40dB Gain Control Range**
- **On-Chip Oscillator with Voltage Regulator and Buffer**
- **Low-Power Shutdown Mode**

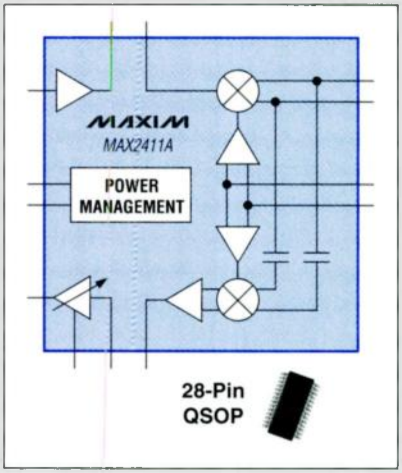
FUTURE PRODUCT

World's First 1.9GHz Silicon-Bipolar RF Up/Downconverter with LNA & Variable-Gain PA Driver

Part of the Maxim PWT1900 chipset, the MAX2411A* performs RF front-end amplification and frequency conversion in both receive and transmit modes. Its unique differential IF interface allows a single SAW filter to serve as a receive and transmit IF filter. This eliminates the need for an extra, costly SAW filter.

The MAX2411A's 1.9GHz low-noise amplifier has 16dB gain and a 2.5dB noise figure. Its receive mixer (9dB noise figure and 8dB gain) yields 3.2dB combined downconverter noise figure and -2.5dBm input IP3. The receive current is only 20mA with a 3.0V supply and can be reduced to less than 1µA when pulling the logic-compatible enable pins low. The transmit section includes an upconverter mixer that generates -11dBm at 1dB compression, followed by a power amplifier (PA) predriver with 14dB gain and +5dBm 1dB compression power. The predriver's gain is adjustable over a >20dB range for system gain and output power adjustment.

The MAX2411A comes in a 28-pin miniature plastic QSOP.



* Future product—contact factory for engineering samples.

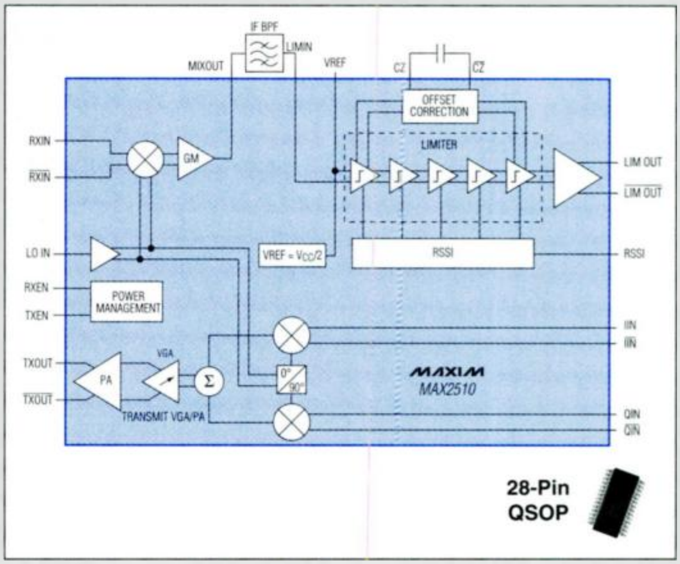
FUTURE PRODUCT

Most Complete IF Transceiver for PCS Has Widest Dynamic Range

EV KIT AVAILABLE

MAX2510*:

- **Operates from Single +2.7V to +5.5V Supply**
- **Unique, Wide-Dynamic-Range Downconverter Mixer**
- **90dB Gain Limiting Amplifier Directly Drives CMOS Input**
- **RSSI Function with 90dB Dynamic Range**
- **I/Q Transmitter with 42dB Sideband Rejection**
- **+2dBm Transmit Amplifier with 40dB Gain Control Range**
- **Low Supply Current (13.5mA Rx, 18.5mA to 32mA Tx)**
- **Low-Power Shutdown Mode (<1µA)**



* Future product—contact factory for engineering samples.

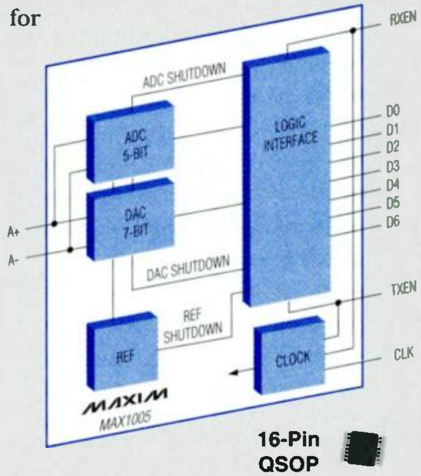
Ultra-Low-Power IF Undersampler: TDMA Ready!

The MAX1005* includes an analog-to-digital converter (ADC) and digital-to-analog converter (DAC) plus voltage reference for time-division duplex (TDD) applications. In receive (Rx) mode, the ADC is used to sample IF. The ADC's fast 15Msps conversion rate and wide input bandwidth allows for use of undersampling techniques. In the PWT1900 application, the ADC converts a 1.5MHz bandwidth signal centered at an IF of 10.7MHz. In transmit (Tx) mode, the DAC converts digital data from the modem into an analog IF Tx signal at 15Msps.

The MAX1005 use very little power (13mA in Rx mode and 5.5mA in Tx mode) while providing a high level of signal integrity. Supply voltage operation is guaranteed down to +2.7V and multiple shutdown modes are provided, including a 1μA (max) full shutdown mode. Wakeup time from partial shutdown is just 2.5μs, providing for power savings even during short periods of idle time.

The MAX1005 and MAX2511 combination provides a significant cost savings. These devices are designed to cut component cost and size by using the same IF filter for both Tx and Rx filtering.

- **15Msps, 5-Bit ADC with 4.5 ENOB**
- **15Msps, 7-Bit DAC with 28dB SFDR (at 10.7MHz Output)**
- **Low-Noise Internal Reference**
- **Single-Supply Operation (+2.7V to +5.5V)**
- **Low Power:**
  - **13mA typical at 15Msps (Rx mode)**
  - **1μA max in Shutdown**
- **Small Height and Footprint: QSOP-16**



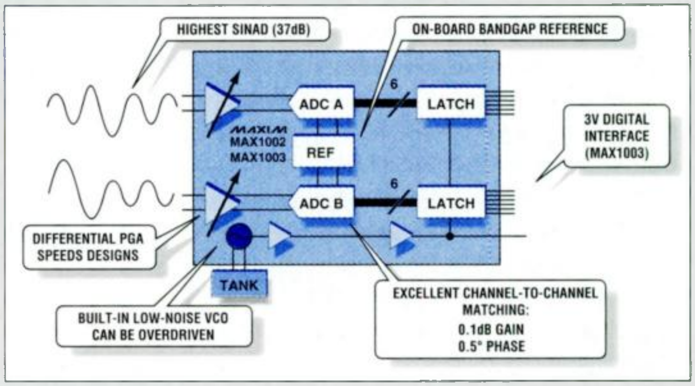
* Future product—contact factory for engineering samples

Highest Performance, Dual 6-Bit 60Msps/90Msps ADCs

Improve Your Demodulator Performance

The MAX1002/MAX1003 dual analog-to-digital converters (ADCs) digitize the analog baseband I and Q vector outputs of QPSK and QAM-16 (16-position quadrature amplitude modulation) IF downconverters or tuners into two parallel, 6-bit, offset binary-coded digital outputs. They operate at sampling rates of 60Msps (MAX1002) and 90Msps (MAX1003) while achieving typical integral and differential nonlinearity of less than 0.25LSB.

These ADCs are designed for use in direct-broadcast satellite (DBS) receivers, MMDS and HFC cable modems, and wireless data communications.



For the highest dynamic performance and best design flexibility with low power dissipation, choose the MAX1002/MAX1003 for your next-generation DBS/DVB or QPSK receiver application.

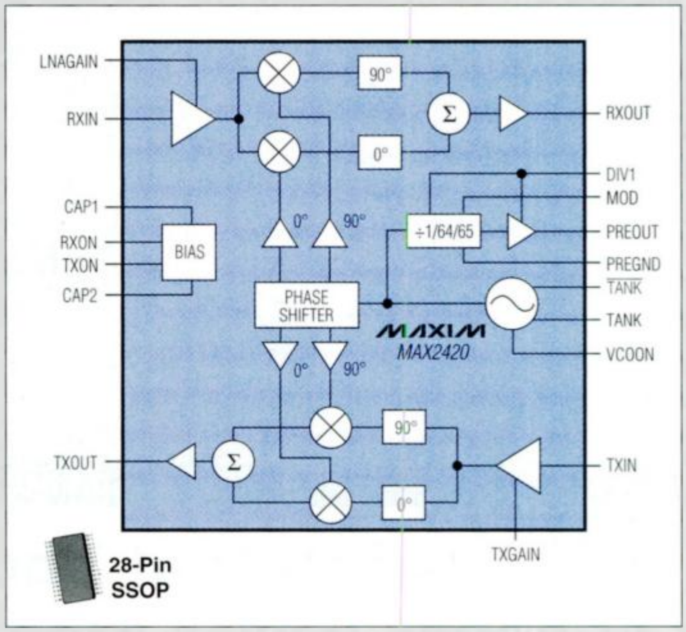
FUTURE PRODUCT

Image-Reject RF Transceiver Ideal for Low-Cost 900MHz Radios

EV KIT AVAILABLE

High Integration Level and Image Reject Simplify System Architecture, Saving Cost and Space

The MAX2420* RF transceiver is designed for applications such as cordless phones, wireless modems, and RF transceivers. The device includes a programmable-gain low-noise amplifier, image-reject downconverter, VCO, divide-by-64/65 prescaler, transmit variable-gain amplifier, image-reject upconverter, and PA driver—all on a single IC! Typically only a low-cost CMOS PLL synthesizer, an IF amplifier, and a power amplifier are needed to complete a 900MHz two-way radio transceiver.



The MAX2420 includes a multitude of functions needed in a 900MHz radios, saving cost and space.

The image-reject feature allows the use of a very low IF frequency without adding steep filters or compromising receiver performance due to interference at the image frequency. This eliminates the need for a second frequency conversion, saving cost and space. On the transmit side, the image-reject mixer greatly reduces filtering requirements . . . or eliminates filters altogether.

The MAX2420's low-noise amplifier, with 1.8dB noise figure, yields excellent combined downconverter noise figure of just 4dB with -17dBm input IP3. LNA gain is adjustable to increase receiver dynamic range (up to +2dBm input IP3). The internal VCO exhibits phase noise of just -84dBc/Hz at 10kHz offset. The prescaler can either be used in divide-by-64/65 mode in conjunction with a CMOS PLL, or in buffer mode with a BiCMOS synthesizer. The transmitter includes a variable-gain amplifier with more than 36dB of control range, the image-reject upconverter, and a 0dBm amplifier that can be used either to drive an external power amplifier or to drive the antenna directly.

The MAX2420 is optimized for 10.7MHz receive and transmit intermediate frequencies. Future members of this product family will be optimized for IFs of 45MHz, 70MHz, and 110MHz. Further members of the family will replace the transmit image-reject mixer with a balanced mixer, which can be used as a balanced modulator or LO buffer. Receive-only versions will also be available. The MAX2420 comes in a 28-pin SSOP package.

*Future product—contact factory for availability

Wireless/RF Products

Part Number	Supply Voltage (V)	Input Frequency (MHz)	Input Bandwidth (MHz)	I/Q Gain Balance (dB)	I/Q Phase Balance (degrees)	AGC Range (dB)	Pins-Package Options*	Features	Applications	Price† 25,000-up ($)
SATELLITE RECEIVER PRODUCTS										
MAX2101	4.75 to 5.25	400 to 700	60	0.5	1.5	40	100-MQFP	I/Q demodulator with dual 5th-order Butterworth filters, 10MHz to 30MHz bandwidth, and dual 6-bit ADCs	DBS, VSAT	11.49
MAX2102	4.75 to 5.25	950 to 2150	120	0.5	3(max)	50	28-SO	Direct downconversion tuner IC, tunes L-band directly to baseband I and Q outputs	DBS, DAB	4.00

Part Number	Supply Voltage (V)	Supply Current (mA)	IF Frequency (MHz)	IF Bandwidth (MHz)	I/Q Gain Balance (dB)	I/Q Phase Balance (degrees)	Pins-Package Options*	Features	Applications	Price† 1000-up ($)
MODULATORS AND DEMODULATORS										
MAX2450	2.7 to 3.3	5.9	70	9	0.45	3	20-SO, 20-QSOP	70MHz I/Q modulator/demodulator with on-chip VCO and quad generator, shutdown mode	Cellular, ISM, WLANs	3.99
MAX2451	2.7 to 3.3	5.5	70	9	0.45	3	16-SO	70MHz I/Q demodulator with on-chip VCO and quad generator, shutdown mode	Cellular, ISM, WLANs	3.23
MAX2452	2.7 to 3.3	4.1	70	15	0.45	3	16-SO	70MHz I/Q modulator with on-chip VCO and quad generator, shutdown mode	Cellular, ISM, WLANs	3.23

Part Number	Supply Voltage (V)	Input IP3** (dBm)	Noise Figure (dB)	Transmit Output (dBm)	RF Frequency (MHz typ)	IF Frequency (MHz typ)	Pins-Package Options*	Features	Applications	Price† 1000-up ($)
UPCONVERTERS AND DOWNCONVERTERS										
MAX2420/1/2	2.7 to 4.8	-17/-8/+2	4	0	800 to 1000	10/46/70	28-SSOP	Image-reject up/downconverter with VCO, prescaler, 30dB transmit VGA, programmable-gain LNA, and 0dBm PA predriver; high-side LO injection	Cordless phones, cellular phones, ISM spread spectrum, RF transceivers	††
MAX2426	2.7 to 4.8	-17/-8/+2	4	-3	800 to 1000	70	28-SSOP	Image-reject up/downconverter with VCO, prescaler, balanced transmit modulator, programmable-gain LNA, and 0dBm PA predriver; high-side LO injection	Cordless phones, ISM spread spectrum, RF transceivers	††
MAX2440/1/2	2.7 to 4.8	-17/-8/+2	4	—	800 to 1000	10/46/70	28-SSOP	Image-reject downconverter with VCO, prescaler, and programmable-gain LNA; high-side LO injection	Cordless phones, ISM spread spectrum, RF receivers	††
MAX2460	2.7 to 4.8	-17/-8/+2	4	0	800 to 1000	10	28-SSOP	Image-reject downconverter with balanced transmit modulator, VCO, prescaler, programmable-gain LNA, and 0dBm PA predriver; low-side LO injection	Cordless phones, ISM spread spectrum, RF transceivers	††
MAX2662	2.7 to 5.5	12(OIP3)	9	-1	40 to 2500	10 to 500	SOT23-6	Low-noise, low-voltage upconverter with 15mA supply current, 1µA shutdown	Hand-held receivers, WLANs, ISM PCS, portable phones	††
MAX2670	2.7 to 5.5	10(OIP3)	9	-8	40 to 2500	10 to 500	SOT23-6	Low-noise, low-voltage upconverter with 9mA supply current, 1µA shutdown, buffered LO	Hand-held receivers, WLANs, ISM PCS, portable phones	††
MAX2672	2.7 to 5.5	12(OIP3)	9	-1	40 to 2500	10 to 500	SOT23-6	Low-noise, low-voltage upconverter with 15mA supply current, 1µA shutdown	Hand-held receivers, WLANs, ISM PCS, portable phones	††
MAX2673	2.7 to 5.5	12(OIP3)	9	-1	40 to 2500	10 to 500	8-µMAX	Low-noise, low-voltage upconverter with 15mA supply current, 1µA shutdown, differential inputs	Hand-held receivers, WLANs, ISM PCS, portable phones	††
MAX2690	2.7 to 5.5	7.5	9.5	—	40 to 2500	10 to 500	10-µMAX	Low-noise, 95dB NF, low-voltage downconverter with 15mA supply current, 1µA shutdown, differential IF port	Hand-held receivers, WLANs, ISM PCS, portable phones	††

* Package Options: MQFP = Modular Quad Flat Pack, SO = Small Outline, SSOP = Shrink Small-Outline Package, QSOP = Quarter Small-Outline Package

** Depending on LNA gain setting.

† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

†† Future product—contact factory for pricing and availability. Specifications are preliminary.

NOTE: IF = Intermediate Frequency, I/Q = In-Phase/Quadrature-Phase, VGA = variable-gain amplifier

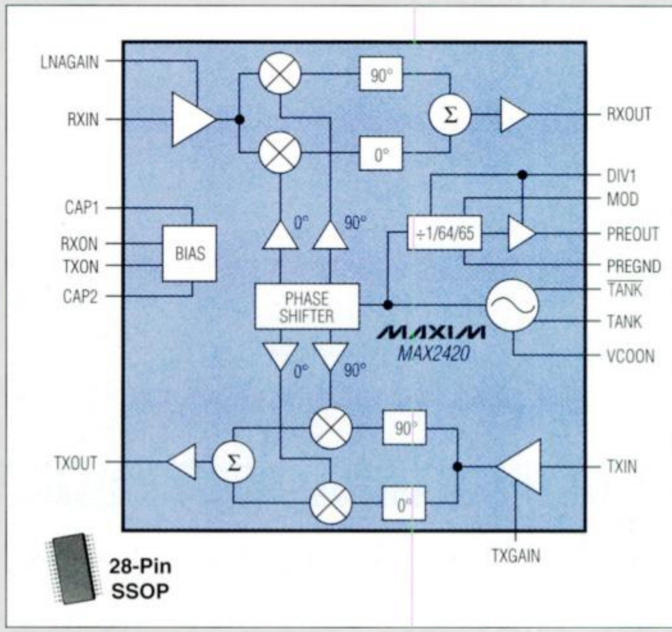
FUTURE PRODUCT

Image-Reject RF Transceiver Ideal for Low-Cost 900MHz Radios

EV KIT AVAILABLE

High Integration Level and Image Reject Simplify System Architecture, Saving Cost and Space

The MAX2420* RF transceiver is designed for applications such as cordless phones, wireless modems, and RF transceivers. The device includes a programmable-gain low-noise amplifier, image-reject downconverter, VCO, divide-by-64/65 prescaler, transmit variable-gain amplifier, image-reject upconverter, and PA driver—all on a single IC! Typically only a low-cost CMOS PLL synthesizer, an IF amplifier, and a power amplifier are needed to complete a 900MHz two-way radio transceiver.



The MAX2420 includes a multitude of functions needed in a 900MHz radios, saving cost and space.

The image-reject feature allows the use of a very low IF frequency without adding steep filters or compromising receiver performance due to interference at the image frequency. This eliminates the need for a second frequency conversion, saving cost and space. On the transmit side, the image-reject mixer greatly reduces filtering requirements . . . or eliminates filters altogether.

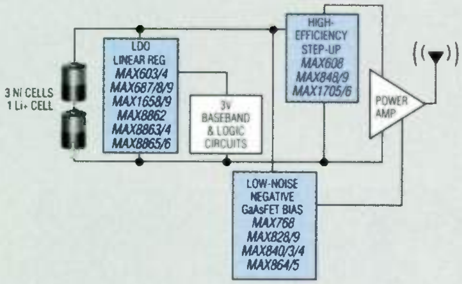
The MAX2420's low-noise amplifier, with 1.8dB noise figure, yields excellent combined downconverter noise figure of just 4dB with -17dBm input IP3. LNA gain is adjustable to increase receiver dynamic range (up to +2dBm input IP3). The internal VCO exhibits phase noise of just -84dBc/Hz at 10kHz offset. The prescaler can either be used in divide-by-64/65 mode in conjunction with a CMOS PLL, or in buffer mode with a BiCMOS synthesizer. The transmitter includes a variable-gain amplifier with more than 36dB of control range, the image-reject upconverter, and a 0dBm amplifier that can be used either to drive an external power amplifier or to drive the antenna directly.

The MAX2420 is optimized for 10.7MHz receive and transmit intermediate frequencies. Future members of this product family will be optimized for IFs of 45MHz, 70MHz, and 110MHz. Further members of the family will replace the transmit image-reject mixer with a balanced mixer, which can be used as a balanced modulator or LO buffer. Receive-only versions will also be available. The MAX2420 comes in a 28-pin SSOP package.

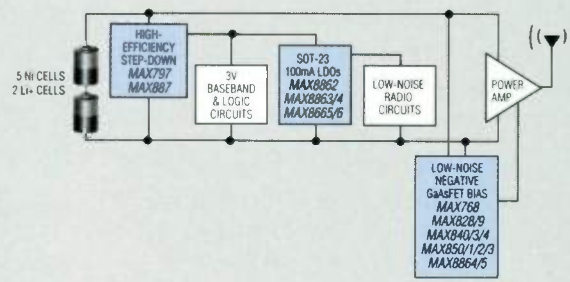
*Future product—contact factory for availability

Complete Power-Management Solutions for Wireless Systems

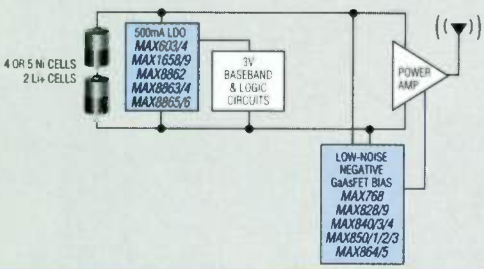
1 Li+ GSM & JAPANESE DIGITAL PHONE SUPPLY



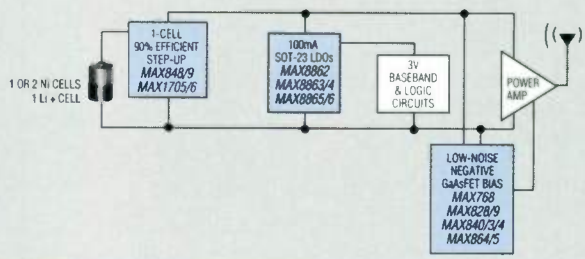
2 Li+ CDMA PHONE SUPPLY



4-CELL AMPS PHONE SUPPLY



1-CELL CORDLESS & PCS PHONE SUPPLY



FEATURED PRODUCT

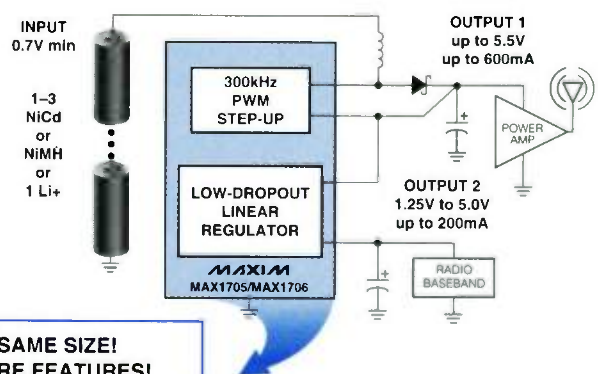
NEW

Dual-Output Phone DC-DC Supplies Power Amp and Low-Noise Circuits

95% Efficient, Low-Noise Step-Up Delivers 800mA from 1–3 Cells

MAX1705/MAX1706:

- **0.7V to 5.5V Input Range**
- **1.1V Guaranteed Start-Up**
- **Step-Up Output (2.5V to 5.5V adj.)**
- **Linear Regulator Output (1.25V to 5.0V adj.)**
- **1µA Shutdown Current**
- **Pushbutton On/Off Control**
- **MAX1705 EV Kit Speeds Designs**



SAME SIZE!
MORE FEATURES!

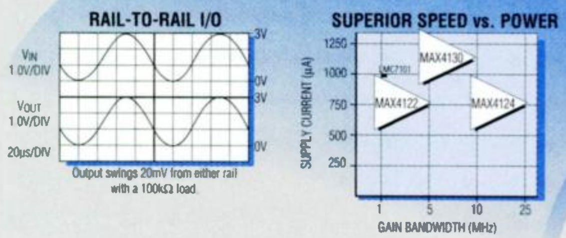
8-Pin SO 16-Pin QSOP

MAXIM

Highest Speed Rail-to-Rail® I/O Op Amps in a SOT23 Package

Single-Supply Operation Down to 2.7V, GBWs from 5MHz to 25MHz

The MAX4122–MAX4134 rail-to-rail I/O op amps simplify low-voltage designs. The three families feature gain-bandwidth products of 5MHz, 10MHz and 25MHz ($A_V \geq 10V/V$) and are guaranteed to operate down to a +2.7V single supply. Rail-to-rail capability allows the inputs to extend beyond the supply rails and the output to swing within 20mV from either rail (R_L = 100kΩ)!



Device	Amplifiers per Package	Shutdown	Supply Voltage (V)	Minimum Stable Gain (V/V)	Gain Bandwidth (MHz)	Supply Current per Amp (µA, max)	V_{OS} (µV, max)
MAX4122/4123	Single	Yes	+2.7 to +6.5	1	5	750	600
MAX4124/4125	Single	Yes	+2.7 to +6.5	10	25	750	600
MAX4126/4127	Dual	Yes	+2.7 to +6.5	1	5	750	750
MAX4128	Dual	No	+2.7 to +6.5	10	25	750	750
MAX4129/4134	Quad	No	+2.7 to +6.5	1	5/10	750/1050	1500
MAX4130/4131	Single	Yes	+2.7 to +6.5	1	10	1050	600
MAX4132/4133	Dual	Yes	+2.7 to +6.5	1	10	1050	750

Single-Supply, 300MHz Op Amps Offered in a SOT23-5 Package

0.1dB Gain to 50MHz with Rail-to-Rail Outputs

This new family of rail-to-rail op amps combines low power consumption, single-supply operation, and wide bandwidth in a tiny 5-pin SOT23 package. This combination of features makes the MAX4212–MAX4222 op-amp family ideal for a variety of battery-powered instruments, high-speed ADC preamps, and video applications. They employ a voltage-feedback architecture, but their specifications are typical of current-feedback amplifiers.

Part	No. of Amps	Min. Stable Gain (V/V)	-3dB Bandwidth (MHz)	0.1dB Gain Flatness (MHz)	Slew Rate (V/µs)	Diff. Gain/Phase Error (%/°)	Output Swing (V)** (R_L = 10kΩ)	Shutdown	Packages
MAX4212/4213	1	1	300	50	600	0.02/0.02	0.05 to 4.95	Yes	5-pin SOT23, 8-pin SO/µMAX
MAX4214*/4215*	1	2	300	50	600	0.02/0.02	0.05 to 4.95	Yes	5-pin SOT23, 8-pin SO/µMAX
MAX4216/4217*	2	1/2	200	35	600	0.02/0.02	0.05 to 4.95	No	8-pin SO/µMAX
MAX4218/4220	3/4	1	200	35	600	0.02/0.02	0.05 to 4.95	Yes	14-pin SO, 16-pin QSOP
MAX4219*/4222*	3/4	2	200	35	600	0.02/0.02	0.05 to 4.95	Yes	14-pin SO, 16-pin QSOP

* Future product—available after November 1997
** V_{CC} = +5V, V_{EE} = 0V.

Part Number	Supply Voltage (V)	Input Frequency (MHz)	Input Bandwidth (MHz)	I/Q Gain Balance (dB)	I/Q Phase Balance (degrees)	AGC Range (dB)	Pins-Package Options*	Features	Applications	Price† 25,000-up ($)
SATELLITE RECEIVER PRODUCTS										
MAX2101	4.75 to 5.25	400 to 700	60	0.5	1.5	40	100-MQFP	I/Q demodulator with dual 5th-order Butterworth filters, 10MHz to 30MHz bandwidth, and dual 6-bit ADCs	DBS, VSAT	11.49
MAX2102	4.75 to 5.25	950 to 2150	120	0.5	3(max)	50	28-SO	Direct downconversion tuner IC, tunes L-band directly to baseband I and Q outputs	DBS, DAB	4.00

Part Number	Supply Voltage (V)	Supply Current (mA)	IF Frequency (MHz)	IF Bandwidth (MHz)	I/Q Gain Balance (dB)	I/Q Phase Balance (degrees)	Pins-Package Options*	Features	Applications	Price† 1000-up ($)
MODULATORS AND DEMODULATORS										
MAX2450	2.7 to 3.3	5.9	70	9	0.45	3	20-SO, 20-QSOP	70MHz I/Q modulator/demodulator with on-chip VCO and quad generator, shutdown mode	Cellular, ISM, WLANs	3.99
MAX2451	2.7 to 3.3	5.5	70	9	0.45	3	16-SO	70MHz I/Q demodulator with on-chip VCO and quad generator, shutdown mode	Cellular, ISM, WLANs	3.23
MAX2452	2.7 to 3.3	4.1	70	15	0.45	3	16-SO	70MHz I/Q modulator with on-chip VCO and quad generator, shutdown mode	Cellular, ISM, WLANs	3.23

Part Number	Supply Voltage (V)	Input IP3** (dBm)	Noise Figure (dB)	Transmit Output (dBm)	RF Frequency (MHz typ)	IF Frequency (MHz typ)	Pins-Package Options*	Features	Applications	Price† 1000-up ($)
UPCONVERTERS AND DOWNCONVERTERS										
MAX2420/1/2	2.7 to 4.8	-17/-8/+2	4	0	800 to 1000	10/46/70	28-SSOP	Image-reject up/downconverter with VCO, prescaler, 30dB transmit VGA, programmable-gain LNA, and 0dBm PA predriver; high-side LO injection	Cordless phones, cellular phones, ISM spread spectrum, RF transceivers	††
MAX2426	2.7 to 4.8	-17/-8/+2	4	-3	800 to 1000	70	28-SSOP	Image-reject up/downconverter with VCO, prescaler, balanced transmit modulator, programmable-gain LNA, and 0dBm PA predriver; high-side LO injection	Cordless phones, ISM spread spectrum, RF transceivers	††
MAX2440/1/2	2.7 to 4.8	-17/-8/+2	4	—	800 to 1000	10/46/70	28-SSOP	Image-reject downconverter with VCO, prescaler, and programmable-gain LNA; high-side LO injection	Cordless phones, ISM spread spectrum, RF receivers	††
MAX2460	2.7 to 4.8	-17/-8/+2	4	0	800 to 1000	10	28-SSOP	Image-reject downconverter with balanced transmit modulator, VCO, prescaler, programmable-gain LNA, and 0dBm PA predriver; low-side LO injection	Cordless phones, ISM spread spectrum, RF transceivers	††
MAX2662	2.7 to 5.5	12(OIP3)	9	-1	40 to 2500	10 to 500	SOT23-6	Low-noise, low-voltage upconverter with 15mA supply current, 1µA shutdown	Hand-held receivers, WLANs, ISM PCS, portable phones	††
MAX2670	2.7 to 5.5	10(OIP3)	9	-8	40 to 2500	10 to 500	SOT23-6	Low-noise, low-voltage upconverter with 9mA supply current, 1µA shutdown, buffered LO	Hand-held receivers, WLANs, ISM PCS, portable phones	††
MAX2672	2.7 to 5.5	12(OIP3)	9	-1	40 to 2500	10 to 500	SOT23-6	Low-noise, low-voltage upconverter with 15mA supply current, 1µA shutdown	Hand-held receivers, WLANs, ISM PCS, portable phones	††
MAX2673	2.7 to 5.5	12(OIP3)	9	-1	40 to 2500	10 to 500	8-µMAX	Low-noise, low-voltage upconverter with 15mA supply current, 1µA shutdown, differential inputs	Hand-held receivers, WLANs, ISM PCS, portable phones	††
MAX2690	2.7 to 5.5	7.5	9.5	—	40 to 2500	10 to 500	10-µMAX	Low-noise, 95dB NF, low-voltage downconverter with 15mA supply current, 1µA shutdown, differential IF port	Hand-held receivers, WLANs, ISM PCS, portable phones	††

* Package Options: MQFP = Modular Quad Flat Pack, SO = Small Outline, SSOP = Shrink Small-Outline Package, QSOP = Quarter Small-Outline Package
** Depending on LNA gain setting.
† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.
†† Future product—contact factory for pricing and availability. Specifications are preliminary.
NOTE: IF = Intermediate Frequency, I/Q = In-Phase/Quadrature-Phase, VGA = variable-gain amplifier

Part Number	Supply Voltage (V)	Frequency Range (MHz)	Output Power (mW)	Power Control (dB)	Class	Pins-Package Options*	Features	Applications	Price† 1000-up ($)
TRANSMITTERS AND POWER AMPLIFIERS									
MAX2402	4.75 to 5.5	800 to 1000	100	40	AB to B, adj.	20-SSOP	Power amplifier with balanced modulator, linear modulation to 2V, shutdown mode	ISM spread spectrum, DS, FH, BPSK, ASK, FSK	3.78
MAX2430	3 to 5.5	800 to 1000	125 @ 3.6V	15	AB	16-SO, 16-QSOP**	True single-supply power amplifier, power on/off ramp control, more than 32dB gain, shutdown mode	900MHz cordless phones, ISM spread spectrum	2.97
MAX2601	2.7 to 5.5	DC to >1000	1W	—	AB/C	8-SO	3.6V, 1W power transistor in a thermally enhanced plastic package	AMPS phones, two-way paging, CDPD, ISM radios	2.32
MAX2602	2.7 to 5.5	DC to >1000	1W	—	AB/C	8-SO	3.6V, 1W power transistor with an on-chip thermally matched bias diode	AMPS phones, two-way paging, CDPD, ISM radios	2.38

Part Number	Supply Voltage (V)	IF Frequency 1st/2nd (MHz)	RSSI Range (dB)	Tx Power Control (dB)	Image-Reject Mixers	Features	Applications	Price† 1000-up ($)
INTERMEDIATE-FREQUENCY PRODUCTS								
MAX2510	2.7 to 5.5	30 to 500/ 1 to 25	>90	40	No	IF transceiver with downconverter mixer, limiting amplifier, transmit I/Q mixers, and VGA	PCS phones (PWT 1900, PAC, PHS), wireless local loop, RF transceivers	††
MAX2511	2.7 to 5.5	200 to 450/ 10.7	>90	40	Yes	IF transceiver with image-reject downconverter, limiting amplifier, transmit image-reject mixer, and VGA	PCS phones (PWT 1900, PAC, PHS), wireless local loop, RF transceivers	5.94

Part Number	Supply Voltage (V)	Frequency Range (MHz)	Gain (dB) @ I_C (mA)	P1 (dBm)	Noise Figure (dB)	Pins-Package Options*	Features	Applications	Price† 1000-up ($)
GENERAL-PURPOSE RF PRODUCTS									
MAX2611	4.5 to 6.5	DC to 1100	18.5 @ 16	3	3.5	SOT143	Wideband gain block, low noise and high output capability	Satellite receivers, TV, tuners, wireless LANs, ISM radios	0.66
MAX2630	2.7 to 5.5	100 to 1000	13.7 @ 7	-11	3.8	SOT143	3V LNA with internal biasing	Portable phones, wireless LANs, ISM radios	0.70
MAX2631	2.7 to 5.5	100 to 1000	13.7 @ 7	-11	3.8	SOT23-5	3V LNA with shutdown. No external bias resistor.	Cordless phones, wireless LANs, ISM radios	0.74
MAX2632	2.7 to 5.5	100 to 1000	13.7 @ 7	-11	3.8	SOT23-5	3V LNA with bias control	Cordless phones, wireless LANs, ISM radios	0.74
MAX2633	2.7 to 5.5	100 to 1000	13.7 @ 7	-11	3.8	SOT23-6	3V LNA with shutdown and bias control	Cordless phones, wireless LANs, ISM radios	0.79
MAX2650	4.5 to 5.5	DC to 1000	19 @ 18	0	3.6	SOT143	5V low-noise amp with internal biasing	Satellite receivers, TV, tuners, wireless LANs, ISM radios	0.66

Part Number	Supply Voltage (V)	Frequency Range (MHz)	Supply Current (mA)	Phase Noise (dBc/Hz)	Output Power (dBm)	Pins-Package Options*	Features	Applications	Price† 1000-up ($)
OSCILLATORS									
MAX2620	2.7 to 5.25	10 to 1050	9	-110 (at 25kHz offset from 900MHz carrier)	-3 (2 outputs) 0 (differential)	8-μMAX	Low voltage, lowest phase noise, dual outputs, superior isolation	Digital and analog cellular and cordless phones, PCS, pagers, ISM radios	1.98

* Package Options: MQFP = Modular Quad Flat Pack, SO = Small Outline, SSOP = Shrink Small-Outline Package, QSOP = Quarter Small-Outline Package

** Available after September 1997.

† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

†† Future product—contact factory for pricing and availability. Specifications are preliminary.

NOTE: IF = Intermediate Frequency, I/Q = In-Phase/Quadrature-Phase, VGA = variable-gain amplifier

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MAXIM

(continued from page 94)
with designs over 200K gates, Formality is able to verify designs in excess of 2 million gates. The tool is particularly well suited for use with designs in which each integrated circuit is larger than 100,000 gates or equivalent. The logic has been synthesized using the Design Compiler synthesis tool, and traditional gate-level simulation is expected to run for several days.

The Formality formal verification tool reduces both design cycle time and the cost of finding and fixing bugs. It accepts VHDL and Verilog library input, and can perform either RTL-to-gate, gate-to-gate, or RTL-to-RTL verification.

As a complement to the company's PrimeTime static-timing-analyzer tool, it extensively verifies a design's functionality at an order of magnitude faster than with gate-simulation. Due to its tight integration with the Design Compiler tool, the tool offers support for more than 350 synthesis libraries and design files. It also interprets synthesis design data.

One unusual feature of the tool is that it makes flexible verification possible. The tool contains multiple proprietary verification solvers, or algorithms, for proving equivalence. Similar tools, on the other hand, rely on a single solver to perform this function. Consequently, as Formality analyzes a design, it's able to heuristically determine the most efficient algorithm to employ on a given section of design. The algorithm then is applied automatically to the design's structure. As a result, the Formality tool can provide support for a broad range of design styles.

Because it uses multiple verification solvers, it's able to try several different approaches to solve difficult verification problems. And, with its ability to automatically manage hierarchy, end users can verify designs where the hierarchy doesn't match.

Another feature of the Formality tool is that it allows for fast and easy debugging. It provides users with powerful diagnostic analysis and schematic debugging for easy isolation and diagnosis of problems. All debugging information is presented graphically in the context of the original design source, as opposed to a symbolic representation. This provides users with error diagnosis in a familiar format.

During debug, error candidates are computed to find mismatched logic and pinpoint the likely source of the logical difference. Failing vectors also are generated and displayed graphically to demonstrate how the logic in the two designs propagates differently. Designers thus will be able to localize and correct bugs at a much faster rate.

The Formality formal verification tool is available now. In U.S. dollars, it sells for $100,000.

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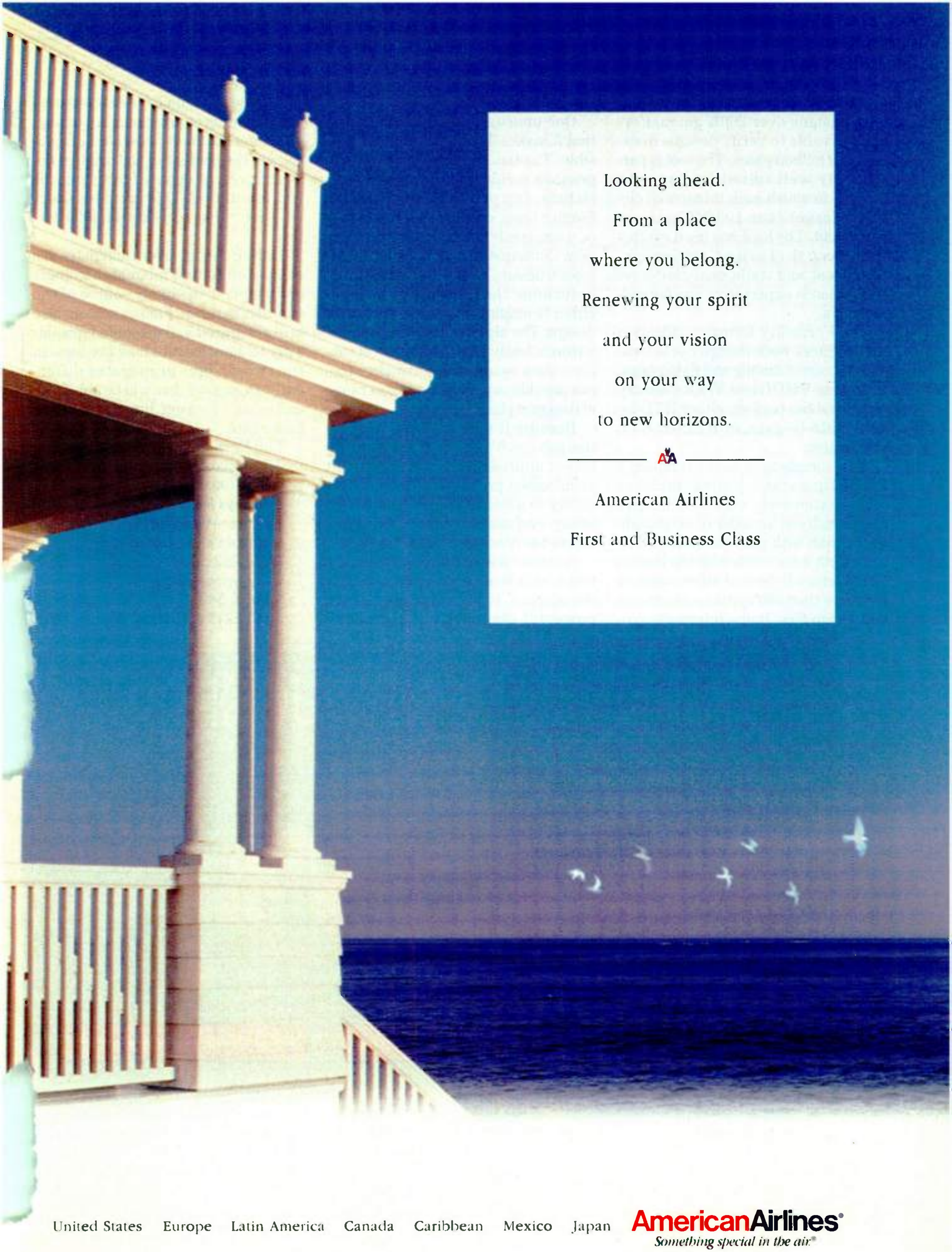


READER SERVICE 112

Planar Transformers Make Maximum Use Of Precious Board Space

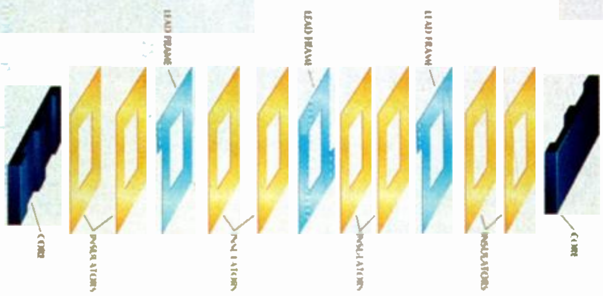
With Their Low Profile And High Density, Planar Devices Help Designers Meet Demands For Ever-Smaller Power Supplies.

SIMON CHOINA, Signal Transformer, 500 Bayview Ave., Inwood, NY, 11096-1792; (516) 239-5777; fax (516) 239-7208.

Power supplies have limited the minimum size that electronic systems can attain, relying as they do on large transformers with large ferrite cores and magnet wire windings. By their very design, planar transformers ease this limitation and allow designers to achieve the low profiles required for pc-board mounting in space-constrained applications. In addition, their construction endows them with more unit-to-unit repeatability, high power-density capability, higher-frequency operation, and high efficiency. While the disadvantages are few, it is important to understand the device's basic construction to fully appreciate its capabilities and potential drawbacks.

Wire-Free Design

Planar transformers are so compact because they are made from copper leadframes and flat, continuous copper spirals instead of copper magnet wire wound around conventional ferrite cores. The spirals are etched on thin sheets of dielectric material and stacked on flat, high-frequency ferrite cores to form the transformer's magnetic circuit (*Fig. 1*). Next, the core material is bonded with a low-grain-diameter epoxy to minimize core losses. High-temperature (130°C) insulators, such as Kapton, within the stack of spirals ensure high isolation between windings. While the leadframes are used to mechanically secure the transformer in place (because it is of low mass), for high-shock/vibration applications, the flat ferrite cores can be bonded to the pc-board using double-sided polyester tape. Connections to the outside circuit, such as the power semiconductors, are made by standard pc-board pins.



1. Planar transformers achieve their compact, low-profile features from their basic construction. They comprise copper leadframes and flat, continuous copper spirals instead of copper magnet wire wound around conventional ferrite cores. The spirals are etched on thin sheets of dielectric material, such as mylar or Kapton. Then, they are stacked on flat, high-frequency ferrite cores to form the transformer's magnetic circuit. High-temperature insulators within the stack of spirals ensure high isolation between windings.

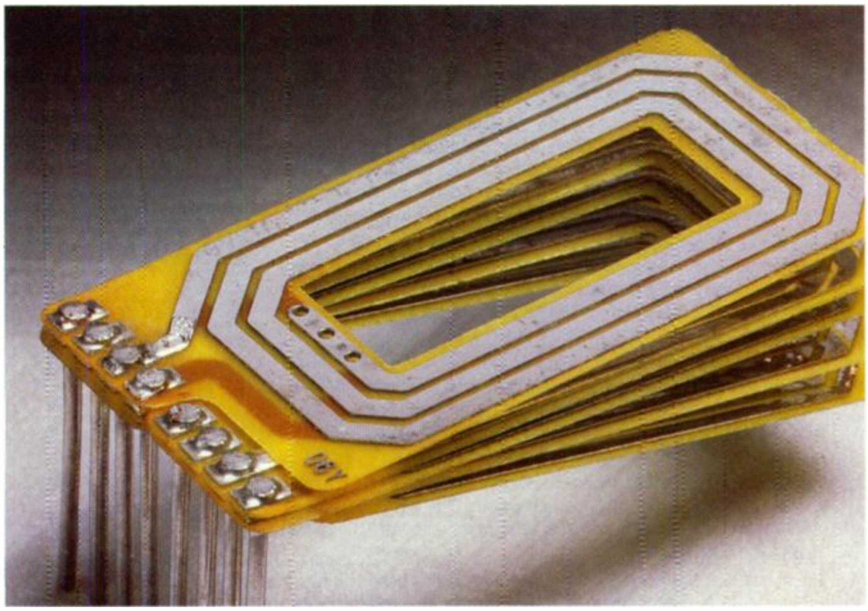
Mechanical Features

It is this construction that gives the planar transformer its characteristically low profile, which usually ranges from between 0.325 to 0.750 in. This makes them especially attractive to power-supply manufacturers working within tight space restrictions.

The planar transformer's pc-board construction means that once the circuit-board components are designed and stamped for a planar device, the windings of subsequent transformers in a production run will be spaced exactly the same distance from each other (*Fig. 2*). This design allows planar transformers to be manufactured with automated assembly equipment, greatly improving device unit-to-unit repeatability and yield in production runs with tight specifications. Conventional transformers are manufactured with copper wire wound around ferrite cores. Irregularities in the spacing of the windings, along with the vagaries of manual assembly, can contrive to produce wide variations in device performance.

The uniformity and predictability of planar transformers has the added advantage of making them simpler to model than conventional transformers. This especially applies when using computer-aided-engineering (CAE) tools such as SPICE modeling.

With excess weight an on-go-



2. The transformer's pc-board construction, with conductive lines formed from copper cladding on high-current, circuit-board materials, allows planar transformer to be manufactured with automated assembly equipment, yielding excellent unit-to-unit repeatability.

ing problem in the typical power-supply design, the planar's ability to reach weights as low as 0.6 oz. per 100 W has made it a key component in many lightweight designs.

While the planar transformer has many advantages, its development was initially hampered by the need for custom cores, pc-board windings, and isolators. However, this attitude is changing as the devices gain acceptance.

Electrical Characteristics

Planar transformers offer efficient operation at high switching frequencies, typically reaching 97% efficiency at switching frequencies through 500 kHz. Their maximum operating frequency can reach as high as 1 MHz (with low flux density). The flat windings are the key to their high efficiency and high-frequency operation. The windings also greatly improve the device's power-density capabilities.

Because conventional transformers generally rely on round-wire windings around a ferrite core, the copper conductor is not efficiently used. This is due to a phenomenon known as skin effect. Skin effect occurs when induced currents and magnetic fields cause current in a round conductor to concentrate near the thin outer surface—or skin—of the wire, especially at higher frequencies. As a result, the total current-carrying area is less than the full wire area, making the ac resistance greater than the dc resistance by an amount determined by the skin thickness.

In a planar transformer, however, the "windings" are actually flat conductive traces formed on copper-clad pc-boards. As a result, the current tends to concentrate toward the outer edges, but it still flows through the entire conductor, with improved overall current density compared to a cylindrical (wire) conductor. The end result is that a planar transformer, with its flat windings, can achieve higher efficiency in much smaller sizes than conventional wire-wound transformers.

Planar construction also minimizes parasitic reactances, such as interwinding capacitance and leakage inductance (typically under 0.5%). The low leakage inductance is achieved by splitting, which puts part of the primary winding in one place, such as the top, part of the winding at the bottom of the stack, and then evenly sandwiching the secondary windings on both sides of the stack.

In wound designs, leakage inductance is difficult to control. The low stray capacitances and leakage inductances go a long way toward reducing high-frequency ringing in a planar transformer's output voltage. This construction—with conductive circuits stacked on dielectric sheets—also allows a planar transformer to achieve good primary-to-secondary and secondary-to-secondary dielectric isolation. The devices can accommodate a wide range of input voltages, and can be specified with one, two, or three outputs. They also meet or exceed the performance requirements of offline converters

Designing With Planars

Because current-carrying capability is a concern in an SMPS, planar transformers typically employ 4-oz. copper-clad circuit boards for their internal winding forms. The same grade of circuit board is a minimum requirement for other sections of an SMPS. The copper used in a 4-oz. copper circuit board is 5.6 mils thick, or 2.8 mils from the center to the surface. In a circular conductor, the current skin depth for copper at 70°C can be obtained from the equation:

$$S = 6.61/\sqrt{f}$$

where S is the skin depth in centimeters, and f is the operating frequency. This works out to be a little over 5 mils at an operating frequency of 250 kHz. It appears to leave little room for error with 4-oz. copper boards.

However, the planar cross section of 4-oz. copper must be converted to circular mils (as with wire tables) to make for a more meaningful examination of skin depth and current density for a given operating frequency. A circular mil is the area occupied by a circle with the diameter of 0.001 in. Just divide the area in square inches by 0.785×10^{-6}.

At higher current densities (and output power levels), 4-oz. copper may not be robust enough. Most circuit-board manufacturers offer heavier copper cladding, usually as a special order. Pc-boards can also be paralleled to double the wire size.

Simon Choina is a senior engineer with Signal Transformer, specializing in high-frequency devices. He received his electronic education in "Bosmath" by Technion in Haifa, Israel, and finished his degree in New York city in 1986. He joined Signal in 1979 after three years with Power Magnetics.

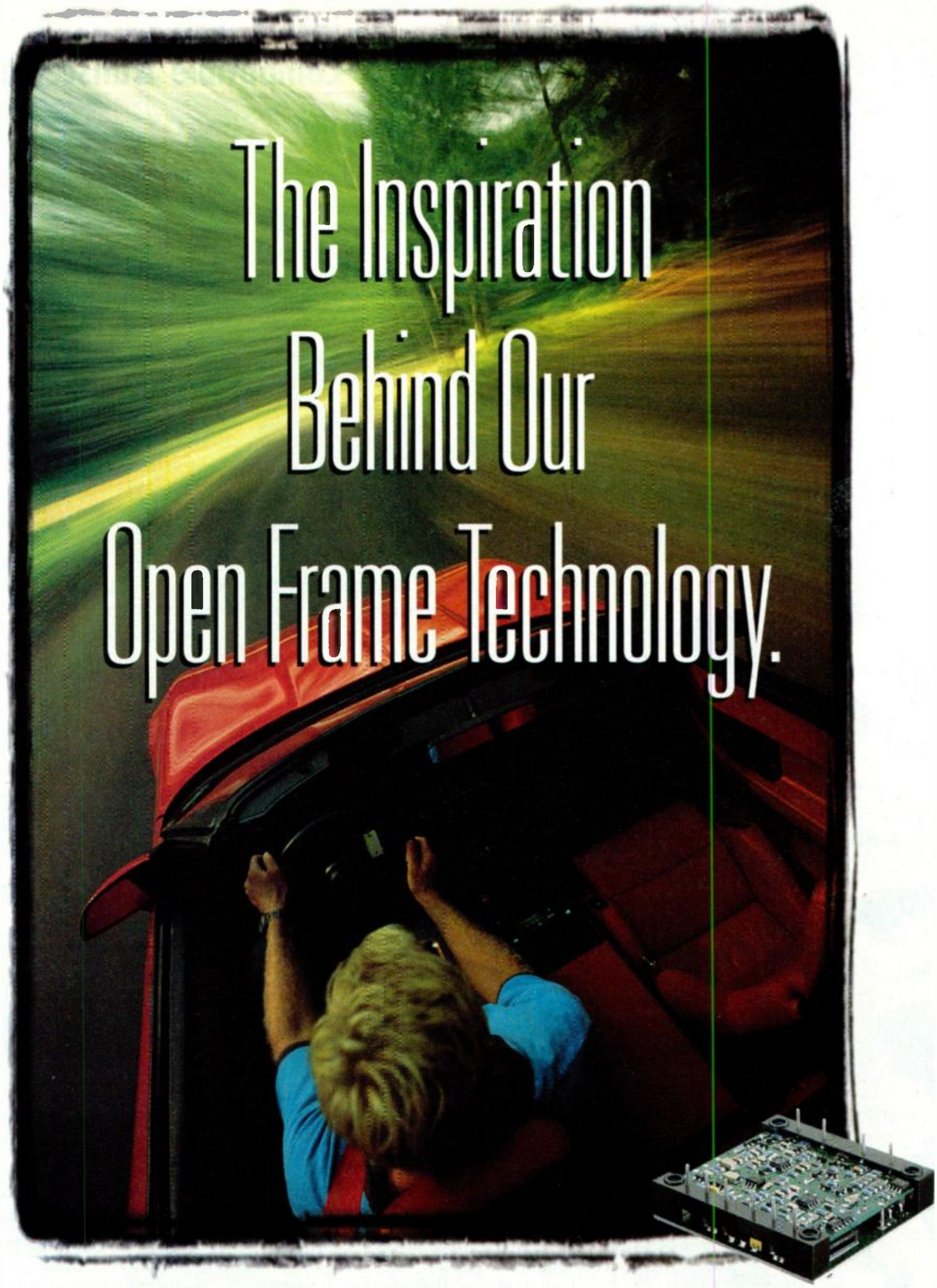
References:

1. Pressman, A., *Switching Power Supply Design*, McGraw-Hill, 1991.

2. Meeldijk, V., *Electronic Components, Selection And Application Guidelines*, Wiley, 1996.

PRODUCT UPDATE: COMPONENTS

Manufacturer	Device	Description	Price and delivery	CIRCLE
		INDUCTORS		
Prem Magnetics Inc. McHenry, IL Sales Dept. (815) 385-2700 Fax (815) 385-8578 www.premmag.com	SPT-049 transformer	This low-profile transformer is designed specifically for V.34 modems in both the U.S. and Europe. Measuring 0.520 by 0.460 by 0.390 in., the device uses supplementary insulation and is designed for dry-circuit applications. The primary-to-secondary creepage distance is 2.5 mm (min) and the hi-pot rating is 1500 V rms for one minute.	$3.00 each in high quantity	562
Valor Electronics Inc. San Diego, CA Yves Collier (619) 537-2619 Fax (619) 537-2525 ycollier@valorinc.com	ST517XT Series transformer	Targeting PBX and central-office use, this T1/E1, quad-port transformer module is surface mountable and comes with four receive and four transmit transformers. The module meets ITU-T G.703 specs and is isolated to 1500 V rms. The 40-pin package measures 28.2 by 15.9 by 5.7 mm, and has a crosstalk figure of -65 dB.	$4.98 each per 10,000	563
BI Technologies Corp. Fullerton, CA Sam Kung (714) 447-2656 Fax (714) 447-2400	HM76 Series surface-mount inductor	Available in values ranging from 1.0 to 1000 µH, this surface-mount inductor uses a high-performance ferrite in a drum-core configuration. The device can handle up to 9.8 A, has a resistance as low as 10 mΩ, a profile down to 3.23 mm, and an operating temperature range of 25° to -80°C. Class B insulation is included.	$0.45 each per 10,000	564
	LC Series inductor-capacitor network	This device incorporates a ladder network of inductors and capacitors to improve over T-type EMI filtering methods. The low-pass network uses a monolithic construction in a 1206 case, and has a sharp cutoff at 10, 22, 47, or 100 MHz.	$0.20 each per 100,000; stock	565
Pulse San Diego, CA Gene Vicino (619) 618-1242 Fax (619) 674-8262 www.pulseeng.com	Self-leaded, SMD chokes	These self-leaded, surface-mount, common-mode chokes handle from 1.50 to 14.40 A, operate up to 1 MHz, and have a dc resistance of 4.41 to 295.60 mΩ. Available in a high-reliability, self-leaded package, the devices have an operating temperature range of -30° to 120°C and a dielectric strength of 500 V rms.	$0.63 each per 10,000	566
	P0581, 2, 3, 4, and 5 current-sense and gate-drive transformers	Offering up to 3000 V rms of isolation for currents up to 36 A, these current-sense transformers (P0581, 2, and 3) come in through-hole versions with turns ratios of 50:1, 100:1, or 200:1. The through-hole gate-drive transformers (P0584 and 5) come in two- or four-gate versions, also with 3000-V rms isolation. The leakage inductance is 500 nH. Both transformers operate at frequencies from 50 to 500 kHz	Current sense, $0.99; gate drive, $1.14 each per 10,000	567
		CAPACITORS		
High Energy Corp. Parkesburg, PA J. Rounce (800) 332-2985 Fax (610) 593-2985 www.highenergycorp.com	Type CN high-power capacitor	Designed for a working life of up to 20 years, this film-type capacitor, with copper-top and base terminals, replaces mica or ceramic units in induction applications. The device has a capacity range of 200 nF to 6 µF and comes in voltages of up to 650 V at 1200 A. Its operating frequency range is 10 kHz to 800 kHz, at temperatures up to 65°C.	$195 each for 10; eight weeks ARO	568
Voltronics Corp. Denville, NJ Nicholas Perrella (973) 586-8585 Fax (973) 586-3404 E-mail: info@voltronicscorp.com	Low-temperature trimmer	Operable in cryogenic temperatures down to 4°K, these precision multiturn trimmer capacitors are available with maximum values of 1 to 180 pF, in a wide variety of sizes. Dielectrics are glass, quartz, sapphire, air, and PTFE.	From $9 each; stock to four weeks	569
		CIRCUIT PROTECTION DEVICES		
Littelfuse Inc. Des Plaines, IL (800) 999-9445 Fax (847) 824-3024 www.littelfuse.com	1812 PTC resettable fuse	This positive-temperature-coefficient, resettable fuse has a full-faced termination design, and complies with USB standards for peripheral-to-computer connections. The device measures 0.179 by 0.127 by 0.020 in., and comes in a variety of current ratings.	$0.30 each, depending on quantity	570
Semtech Corp. Newbury Park, CA Tom Dugan (805) 498-2111 Fax (805) 498-3804 E-mail: NPSMTCHTD@aol.com	RailClamp Series protection diode array	These diode arrays protect external ports, and are designed for voltages of 3.3, 5, 12, or 15 V. Able to suppress electrostatic discharge, electrical fast transients, and lightning-induced transients, the devices use eight surge-rated steering diodes and a transient-voltage suppressor diode in a single package to protect up to four lines. Standards compliance includes IEC 1000-4-2, -4-4, and -4-5.	$1.49 each per 10,000	571
SGS-Thomson Microelectronics Inc. Lincoln, MA Sales Dept. (617) 259-0300 Fax (617) 259-9423 www.st.com	TD230 electronic circuit breaker	This electronic circuit-breaker IC comprises two n-channel power MOSFETs connected as low-resistance switches between the dual-rail power supply and the circuit to be protected. Excess current will trip the MOSFET in around 5 µs. Features include automatic restart, suitability to 2.7-, 4.5-, or ±18-V supplies, and SO16 packaging.	$2 each per 100,000	572
		SEMICONDUCTORS		
Advanced Power Technology Bend, OR Thomas Loder (800) 522-0809 Fax (541) 388-0364 www.advancedpower.com	SOT-227-packaged, low-resistance MOSFET	Available in an SOT-227 package, this high-voltage MOSFET uses the company's Power MOS V process to realize an on resistance as low as 7 mΩ. The rise and fall times for a 500-V, 50-mW device are 20 and 7 ns, respectively. Other features include 100- to 1200-V breakdown, up to 225 A drain current, and a thermal resistance of 0.18.	From $20; stock to eight weeks	573
KDI/Triangle Corp. Whippany, NJ Carl Schraufnagl (973) 887-8100 Fax (973) 884-0445	SWM-1100-1 and 1200-1 broadband diode switches	Using a microstrip soft substrate for the RF circuit, and thick-film hybrid drivers, yields an insertion loss for these diode switches of 1.5, 2.0, and 2.75 dB, over the operating frequencies of 4, 10, and 18 GHz, respectively. The devices have an isolation of 60 dB up to 10 GHz, and 50 dB at 18 GHz. Both run off 5 V dc at ±100 mA.	SWM-1100-1, $345; SWM-1200-1, $414; stock	574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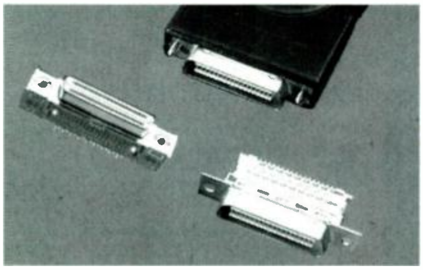
Behind Our
Open Frame Technology.

Universal I/O Connector Gives DSU/CSU Connectivity

This universal I/O connector provides a multi-serial, multi-protocol WAN attachment over a single, high-density connector system. The device provides connectivity to a DSU/CSU and includes a 72- and 160-position cable plug and pc-board connector. The plug has insulation displacement contacts arranged with 0.050-in. centerline spacing using a four-row mating interface. The plug terminates 28- and 30-AWG stranded wires using a benchpress or high-speed applicator. Other features of the connector include a profile of 0.374 in., board-lock hardware, EMI shielding, and standard 4/40 threads. Pricing is $0.042 per line for the cable plug, and $0.052 per line for the pc-board receptacle, in quantities of 10,000.



***AMP Inc.**, P.O. Box 3608, Harrisburg, PA 17105-3608; Product Info. (800) 522-6752; www.amp.com.*
CIRCLE 575

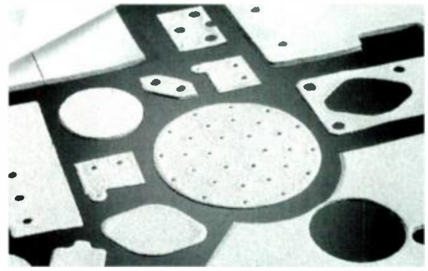
RS-232-To-1-Wire Adapter Has A True Ground

Designed to mate with the serial DB9 port of a PC, the HA3 is an RS-232-powered converter that converts from RS-232 to 1-Wire protocol. Able to drive up to 200 1-Wire devices at cable lengths of up to 2000 ft. using CAT-5 twisted-pair cable, the device measures 2.275 by 1.215 in. A DDE driver is included. Pricing is $69.95.

***Point Six Inc.**, 138 E. Reynolds Rd., Suite 201, Lexington, KY 40517; (606) 271-1744; fax (606) 271-4695; www.pointsix.com.*
CIRCLE 576

Gap Filler Improves On Thermal Conductivity

Therm-A-Gap A574 is a thermally conductive elastomer that replaces air gaps between the item to be cooled and its heat spreader. The elastomer consists of a soft silicone loaded with ceramic particles.. The thermal impedance ranges from 1.10 to 2.86°C-in.^{2}/W for thicknesses from 0.040 to 0.200 in. Pricing starts at $0.25 per in.^{2}



***Chomerics, Div. of Parker Hannifin Corp.**, 77 Dragon Ct., Woburn, MA 01888; (781) 935-4850; fax (781) 933-4318; www.chomerics.com.*
CIRCLE 577

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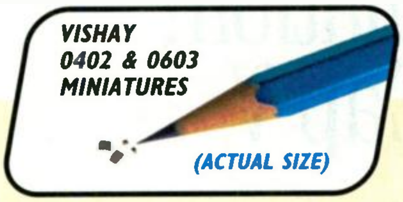

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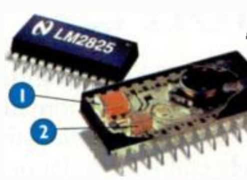

Vishay miniatures at work in National Semiconductor's LM2825 DC-DC converter:
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Low-value power metal strip chip resistors available in sizes 1206, 2010 and 2512. Provides resistance values down to .01 ohms plus or minus 1% tolerance, with ratings from .25 to 2 watts. *FlashFax™ Document #1005*

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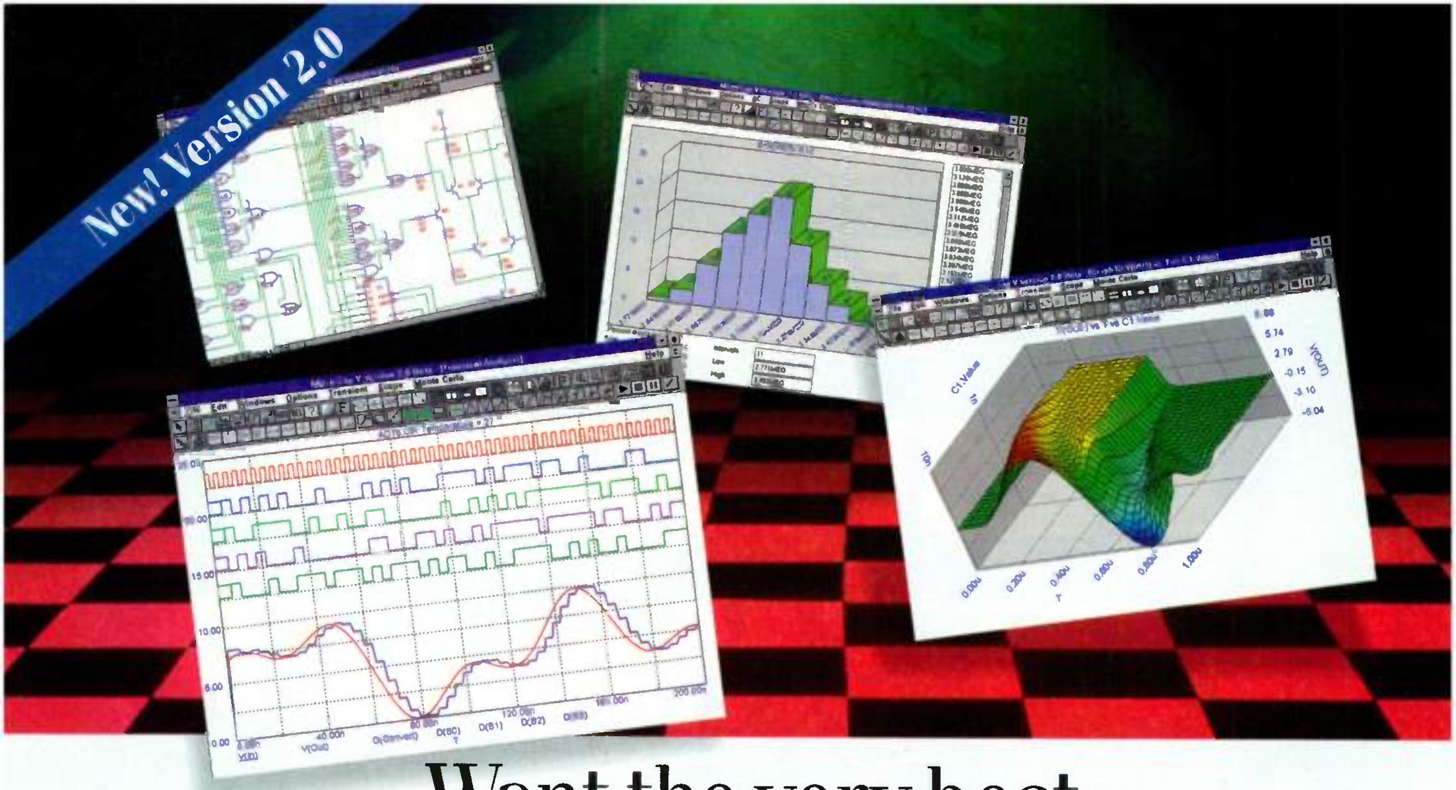

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• Digital Engine	Native PSpice™
• During the Run Plots	Yes
• Analog/Digital Primitives	200+
• Analog/Digital Parts	10,000+
• Performance Plots	Yes
• Parameter Stepping	Multidimensional
• Optimizing Parts Modeler	Yes
• 3D Plots	Yes
• Schematic Probing	Yes
• Behavioral Modeling	Analog & Digital
• Monte Carlo	Yes
• Device Temperatures	Individually Set
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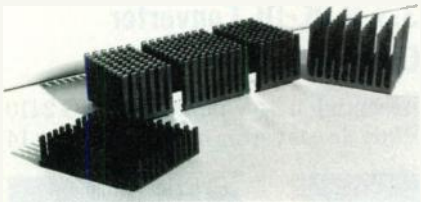
PACKAGING & INTERCONNECTS

Heatsinks Cool Pentium II And Pentium Pro Processors

Designed specifically for the Pentium II and Pentium Pro processors, this line of extruded heatsinks measures 2

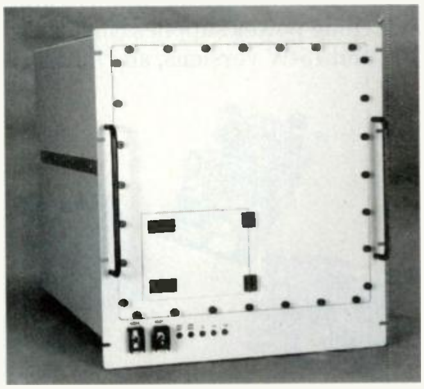


by 5 by 1.5 in. Backed by quick turnaround, the devices come with secondary options such as drilling, tapping, chromating, anodizing, silk-screening, and painting. Pricing for a Pentium II version is $15; for a Pentium Pro version it's $6 per sample. Tooling and prototyping take up to five weeks.

ACK Technology Inc., 7372 Walnut Ave., Unit D, Buena Park, CA 90620; (714) 739-5797; fax (714) 739-5898. CIRCLE 578

10-Slot, 6U VMEbus Enclosure Is Rugged

The FS-8019 is part of the company's line of FULLspectrum, rugged, VMEbus enclosures and accommodates up to ten 6U slots or eight 9U slots. Other backplane configurations



can be supplied. The chassis comes with mounting for up to two half-height SCSI peripherals, is wired with a 1-kW power supply, and consists of solid, seam-welded, aluminum alloys with stainless-steel hardware throughout. Pricing starts at $12,950.

AP Labs, 5871 Oberlin Dr., San Diego, CA 92121; Steve Gills (619) 546-8626; fax (619) 546-0278; www.sd.aplabs.com. CIRCLE 579

Heatsinks Improve Dissipation Capacity By Up To 20%

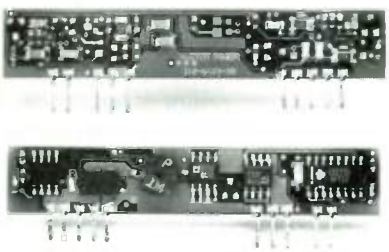
Designed for high-power semiconductors, the PolarCap line of heatsinks incorporate minute breaks and disruptions in the fin surface to disrupt the flow of air over the fin. In addition, the device uses impingement airflow to reduce total air-temperature rise and lower static pressure to increase the volume of airflow. According to the company, the combination results in a 20% improvement in heat-dissipation capacity over conventional fin heatsinks. Pricing, with the fan included, is $77.16 each per 100.

Aavid Thermal Technologies, One Kool Path, P.O. Box 400, Laconia, NH 03247; (603) 224-9988; fax (603) 528-1478; www.aavid.com. CIRCLE 580

POWER

Low-Voltage Converters Respond In Under 5 µs

The MM5020 Series of 6-A dc-dc converters locally convert 4.50- to 5.50-V inputs to 1.30 to 3.50 V with a response time of under 5 µs. Using Switch

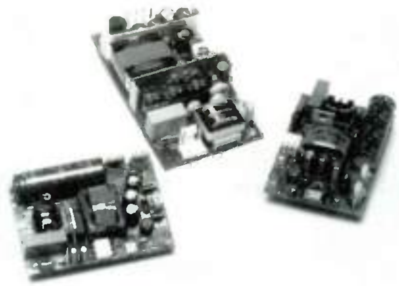


Power Inc.'s V^2 control architecture, the devices have an output ripple of 50 mV p-p, a load/line regulation of ±0.05%, and output voltage set-point accuracy of ±5%. The efficiency is 90% and overall dimensions are 2.50 by 0.45 by 0.35 in. Additional features include N+1 redundancy and parallel operation. Pricing is $20 each per 1000; delivery is eight weeks.

Microelectronic Modules Corp., 2601 S. Moorland Rd., New Berlin, WI 53151; (414) 785-6506; fax (414) 785-6516. **CIRCLE 581**

Open-Frame Switchers Are Ultra-Miniature

The OFM family of open-frame switching power supplies come in 5-, 10-, and 15-W versions, and measure



2.28 by 1.77 in. (5-W version). Outputting 5- to 24-V dc, the supplies plug into standard module pinouts and come with on-board output adjustment and a power-good LED. Pricing is $17 each in quantity; delivery is two to four weeks.

Astrodyne, 300 Myles Standish Blvd., Taunton, MA 02780; Paul Charette (508) 823-8080; fax (508) 823-8181. **CIRCLE 582**

3.3-V DC-DC Converter Outputs Up To 46 W

Accepting a 24-V input, the PKG 2410 PI dc-dc converter outputs 3.3 V at 14

A without additional heatsinking up to 60°C, with only 1-meter/second air *(continued on page 110)*

(continued from page 108)
flow. The 46-W device delivers line and load regulaion of 10- and 35-mV, respectively, and a typical ripple of 60 mV p-p. The integrated control electronics give a load transient response of 100 µs. Measuring 75 by 63.5 by 11 mm, the converter has a typical efficiency of 79.5%. Other features include 1500-V-dc isolation, overvoltage protection, output current limiting, remote control, and thermal shutdown and restart. Pricing is $60 each per 500; samples are available from stock.

***Ericsson Components AB**, S-164 81 Kista, Sweden; Patrick Le Fevre +46 8 721 6263; fax +46 8 721 7001; e-mail: eka.lefe@mesmtpse.ericsson.se.*
CIRCLE 583

Miniature PFC Supply Has User-Selectable Outputs

The PFC Mini is a 1.75-by-6-by-12-in. power-factor-corrected power supply with up to six user-selectable, isolated outputs. The supply accepts inputs of 85- to 264-V ac or 100- to 380-V dc, and

can deliver up to 1500 W. Pricing starts at $0.60 per watt.

***Vicor Westcor Div.**, 560 Oakmead Pkwy., Sunnyvale, CA 94086; Sales Dept. (408) 522-2580; fax (408) 774-5555; www.vicr.com.* **CIRCLE 584**

N-Channel MOSFETs Exhibit Low RDS(ON)

The FS100VSJ-03 is part of the company's line of logic-level, n-channel, surface-mount, power MOSFETs that have an $R_{DS(ON)}$ of 4.7 mΩ. The 100-A, 30-V device uses a trench gate process that allows for a cell density of up to 17 million. It comes packaged in a TO-220S. The line features versions ranging from 30 to 150 V, and from 0.1 to 100 A. Pricing is $5.14 each per 1000. Samples are available from stock, while delivery in quantity is from 8 to 12 weeks.

***Powerex**, 200 Hillis St., Youngwood, PA 15697; (800) 451-1415.*
CIRCLE 585

Medical-Grade UPS Gives Battery-Reserve Indication

The Life-Guard UPS is a medical-grade UPS with battery-reserve indication. Available with ratings of 400 and 1000 VA, the device has line-voltage isolation to over 120 dB and a leakage current of under 500 µA. Other features include hot-swap battery packs, ten minutes of power backup at full load, and overvoltage protection. Pricing for the 1000-VA version is $1500; delivery is four to six weeks.

***Xentek Power Systems Inc.**, 1770 La Costa Meadows Dr., San Marcos, CA 92069; Fernando McLean (760) 471-4001; fax (760) 471-4021; Internet: www.xentek.com.* **CIRCLE 586**

POWER

Point-Of-Use Transfer Switch Enhances Supply Reliability

The SmartSwitch line of point-of-use transfer switches enhance ac-line reliability in mission-critical applications. The device provides rapid switching

between two independent ac power sources with a transfer time of 2 to 6 ms. Features include automatic transfer under fault conditions, diagnostics, hot-swappability, LED indicators, and ETL listing to UL 1008 for safety. Pricing is from $5500, and is available now.

__Liebert Corp.__, 1050 Dearborn Dr., P.O. Box 29186; Columbus, OH 43229; Sales Dept. (800) 877-9222; www.liebert.com. **CIRCLE 587**

DC Programmable Supplies Target Test And Measurement

Available in six models, from 16 to 160 V ac, the Pro-T Series of dc programmable power supplies take a 10-kW, three-phase input and yield an efficiency of up to 80% at full power. Tar-

geting high-power burn-in and automatic test applications, the supplies feature SCR-controlled regulation, full remote control and monitoring, and overvoltage protection. The programming speed is 150 ms (typical, with load), the regulation is under 0.1%, and the rms ripple is under 20 mV. Other features include an IEEE-488.2 or RS-232C interface, EMI filters on the input, and optional CE marking. Pricing is from $4935.

__Sorensen__, 9250 Brown Deer Rd., San Diego, CA 92121; Sam Lewis (619) 458-0246; fax (619) 458-0237; e-mail: saml@elgar.com. **CIRCLE 588**

Pc-Board-Mounted Converter Outputs Up To 15 kV

The MM Series of high-voltage dc-dc converters come in four package sizes with output voltages from 300 V up to 15 kV, at 1.5 or 2.5 W. Reversible modules also are available. All models take input voltages of 9-, 12-, or 24-V dc, and input currents of less than 1 A.

(continued on page 112)

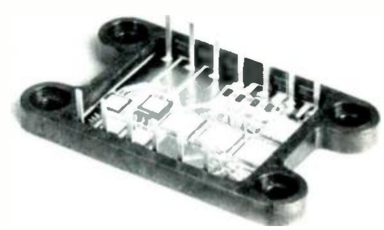
(continued from page 111)

Features include built-in arc protection, an external feedback loop, full encapsulation, and wave solderability. Pricing is from $55 each; delivery is from stock to six weeks.

***Spellman High Voltage Electronics Corp.**, 475 Wireless Blvd., Hauppauge, NY 11788; (516) 630-3000; fax (516) 435-1620.* **CIRCLE 589**

PFC Module Saves On Space And Cost

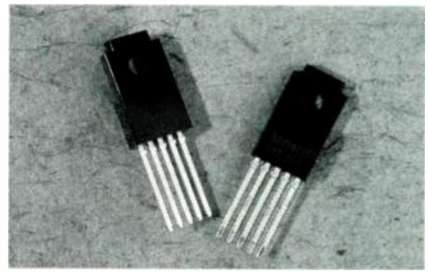
The Model 7720 is a power-factor-correction hybrid module that saves on space by including the rectifier bridge, along with an ultra-fast output diode and four 500-V, 0.01-W FETs. Designed for the front end of supplies in the 1200- to 2500-W range, with minimum input voltages of 84 to 168 V, the module incorporates internal temperature-sensing protection. The device has a profile of 0.200 in., standard, 0.200-in. pitch, and mounts directly to the heatsink with a bolt-on, four-hole frame. It can handle up to 20 A rms with efficiencies of over 90%. Pricing is $35 each in quantity; delivery is six to eight weeks.



***BI Technologies Corp.**, 4200 Bonita Pl., Fullerton, CA 92835; Janet Vaniman (714) 447-2371; fax (714) 447-2400; e-mail: jvaniman@ni.net.* **CIRCLE 590**

Voltage-Regulator IC Combines Two Circuits Into One

To minimize cost and board space, the BA41W12ST five-terminal voltage regulator combines an 8-V, 1-A and a 5-V, 500-mA circuit into a single device. Packaged in a TO220FP-5 package, the device comes with power management that allows unnecessary circuits to be turned off and ensures a standby current of less than 10 µA.

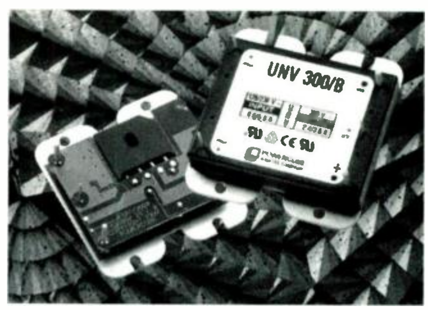


Other features include a maximum power-supply voltage of 35 V, a power dissipation of 2000 mW, and an operating temperature range of –40° to 85°C. Pricing is from $0.70 each per 10,000; delivery is 14 weeks.

***Rohm Corp., Rohm Electronics Div.**, 3034 Owen Dr., Antioch, TN 37013; Sales Dept. (888) 775-ROHM; fax (615) 641-2022; Internet: www.rohmelectronics.com.* **CIRCLE 591**

Auto-Ranging AC-DC Converters Output 1100 W

The UNV300/B is an auto-ranging ac-dc converter that can accept voltages from 85 to 265 V ac, at frequencies of 47 to 440 Hz, and output up to 300 V dc at power levels up to 1100 W. With an efficiency of 97%, the supply requires no heatsinking for applications requiring 300 W or less over the operating temperature range of –55° to 100°C. All are UL, VDE, and CE certified. Pricing is $45 each per 100; delivery is in 30 days.



***Powercube**, 9340 Owensmouth Ave., Chatsworth, CA 91311; Customer Service (800) 866-3590; fax (800) 866-3589.* **CIRCLE 592**

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1508AL	-20	Low	5	PLCC, TQFP	44
1500ABV	-12	Standard	3	PLCC, TQFP	44
1508AS	-7 -10	Standard	5 (3 volt I/O)	PQFP, TQFP, PLCC	84 (PLCC), 100 (PQFP), 100 (TQFP), 160 (PQFP)
1508ASL	-20	Low	5 (3 volt I/O)	PQFP, TQFP, PLCC	84 (PLCC), 100 (PQFP), 100 (TQFP), 160 (PQFP)

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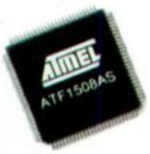

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State-Of-The-Art AWGs Shuffle The Cards On Telecom Testing

If You've Considered And Rejected An Arbitrary Waveform Generator In The Past, It May Be Time For A Second Look.

BRUCE VIRELL, Tektronix Inc., P.O. Box 500, M/S 38-303; Beaverton, OR 97077-0001; (503) 627-1191; e-mail: bruce.virell@tek.com.

The telecommunications market is demanding and dynamic, with twin forces–rapid expansion and quality expectations–creating an enormous challenge for designers. These engineers work at the cutting edge of network and wireless technology. At the same time, they must produce advanced products at lower costs, and on schedules that are measured in months, and sometimes only weeks. Moreover, the product must work right the first time, with no exceptions, otherwise the opportunity for market domination can be completely lost.

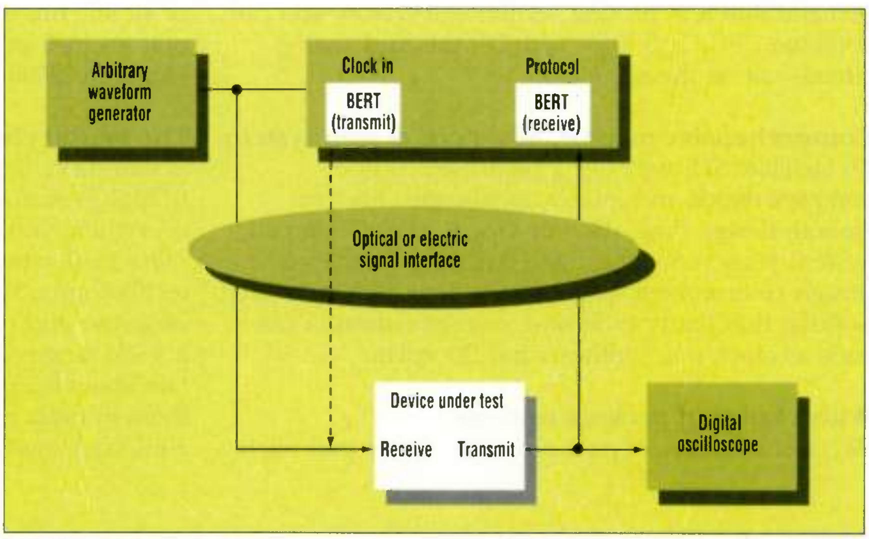
Aware of these relentless demands, telecommunications designers rely heavily on simulation to ferret out the hidden flaws in a device before it goes into production. Simulation does not, however, provide a complete picture of a system's real-world performance. There are just too many variables—both in design and manufacturing—to effectively simulate a product's behavior without the aid of hardware.

The best way to thoroughly examine a design is to couple simulation with rigorous prototype testing. This is accomplished by completely characterizing the device or system on both the physical and protocol layers. The designer also must stress test the product to ensure its operation under such adverse conditions as jitter, bit-pulse impairments, code violations, and noise.

Using an arbitrary waveform generator (AWG) to quickly create an unlimited range of waveform stimuli is one of the best ways to enhance prototype testing of a telecom system. Unlike a bit-error-rate tester (BERT), an AWG can go beyond ideal signals and generate the anomalies, intersymbol effects, jitter, and signal degradation that occur in the real world, helping the telecom designer fully determine the performance of a product under actual operating conditions.

For example, acceptable data communications signal tolerances for network physical-layer testing are well defined by industry standards. However, most current protocol analyzers or BERTs do not test bit pulse extremes as defined by the industry pulse-mask standards. An AWG, on the other hand, simulates serial data signals and tests a device with the pulse extremes to standards. This limit testing is extremely useful in verifying that a device or system truly conforms to a telecom standard.

It is important to note that an AWG does not eliminate the need for a BERT or protocol analyzer. The reason behind this is that a 1-GHz AWG's analog output supports physical-layer testing of communications data rates up to 250 MHz, providing four points per cycle. Instead, an AWG complements existing test tools such as a BERT and digital storage oscilloscope (DSO), helping to extend the range of testing that a designer can perform.



1. An arbitrary waveform generator does not eliminate the need for a bit-error-rate tester, but it can be synchronized with one and used to stimulate a telecommunications device.

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This is possible because modern AWGs seamlessly interact with other test and measurement instruments, exchanging pertinent information between them *(Fig. 1)*.

An AWG can be synchronized with a BERT, and used to stimulate a device under test (DUT), with the BERT receiving, analyzing, and displaying the output from the system. A typical prototype test scenario is as follows: First, the designer uses the BERT to perform protocol testing. Then, moving to the physical layer, the designer either selects from the AWG internal library, or downloads simulation vectors directly into the AWG.

Using the isolated bit-pulse impairment features of a modern AWG, the generator then creates those vectors needed for "what if" scenarios and stress testing of the prototype. The AWG creates serial-data signals, for example, to determine if the DUT complies with the specified telecom pulse-mask standard. The designer also quickly tests for different loading and possible worst-case scenarios, such as fading in a wireless design. Testing for peak or region shifting and all types of jitter or jitter modulation can also be performed, including tests for low- and high-frequency jitter, and jitter on an individual or isolated bit.

Streamline Debugging

If there is a performance issue, an AWG significantly streamlines the task of isolating and debugging the problem. In conjunction with a BERT and a DSO, the AWG creates a full debugging environment, eliminating the need for special or custom debug circuitry, or combinations of multiple signal generators. First, the DUT can be stimulated with the BERT's transmitter section. If an error occurs, the advanced logic or mask triggering capabilities of the DSO will trigger and capture the aberrant behavior. In this way, the conditions that caused the error can be recreated by the AWG on a repetitive basis, enabling the designer to quickly zero in on the source of the error. This combination is particularly powerful when the error-generating events occur infrequently.

With all they have to offer, you would think that AWGs would be part of every telecom designer's suite of test tools. But the fact is they are not.

Until just a few years ago, AWGs did not offer the performance required for telecom applications. Fortunately, today's AWGs change all that. The newest AWGs deliver the advanced capabilities required for telecom testing—up to 250-MHz data standards using the analog outputs, and up to 1-GHz parallel data rates when using the digital output. Many new electrical telecom standards now exceed 1 GHz, such as fiber-distributed data interface (FDDI) and Ethernet. Optical standards are going way beyond that, making it is absolutely essential that an AWG be able to keep pace.

Modern AWGs also supply sufficient vertical resolution (some up to 10 bits at 1 GHz) to allow telecom designers to go beyond idealized square waves, and precisely create extreme, real-world conditions such as high-frequency jitter and noise. Using these examples of worst-case telecom signals, the designer can quickly determine the robustness of an application.

Along with enhanced throughput and vertical resolution, leading-edge AWGs support extremely long record lengths. These deep memories let the designer recreate the message stream more completely with its pulse shape and information content. Longer record lengths eliminate having to sacrifice simulation accuracy by providing enough storage capacity for fast, detailed waveforms.

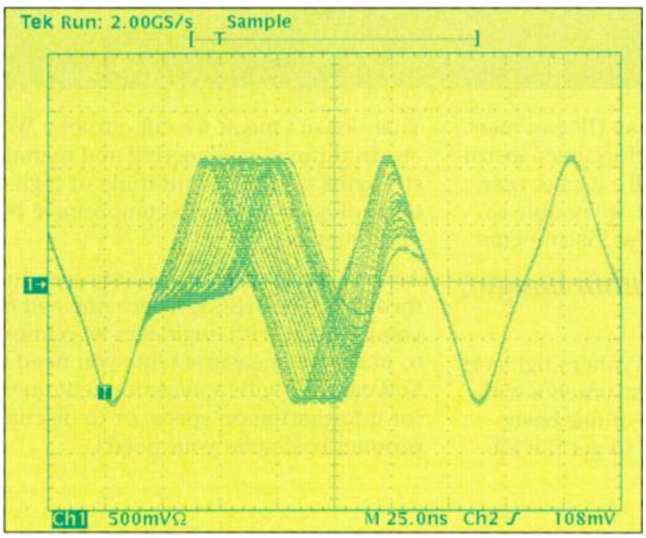
Some of the newest AWGs go beyond simply improving overall performance by providing specialized features tailored for telecom applications. A few even have built-in telecom standards. The AWG 500 Series from Tektronix, for example, supports DS1, DS3, STS1, and many more standards. New, emerging standards also can be added using a floppy disk or the built-in Ethernet port.

Real-Time Sequencing

Along with standards, the leading-edge AWGs provide real-time sequencing that allows for essentially infinite record lengths. Sequencing capability has been around for some time. Basic sequencers execute simple functions like looping, which allows for the limited repetition of waveforms in memory. More advanced sequencers also allow the concatenation of multiple signals to form more complex waveforms. However, both of these types of sequencers require their content be compiled and stored into memory as a single waveform file. To execute 64,000 repetitions of a waveform that has been constructed from 1,000 data points would, when compiled, require a 64 Mword memory.

That's not the case with a real-time sequencer, which requires only 1000 words of memory to store the defining wavepoints. The AWG then uses an internal counter to perform 64,000 loops on the record. This type of architecture can be compared to a computer routine capable of executing loops, jumps, Go Tos, and similar instructions. Thus, memory requirements are significantly reduced, and the effective record length can handle almost infinite data stream lengths.

With a real-time sequencer, the AWG provides yet another advantage to telecom applications: the ability to respond immediately to error conditions from the DUT. With a dedicated 4-bit jump (error) input, the AWG provides up to 16 different programmed states through the sequencer, which can respond with predefined jumps to subroutines within the memory. A com-



2. A problem-causing signal like this example of isolated bit-pulse jitter can be created easily with modern AWGs.

plete characterization procedure can, therefore, be designed around a sequence that iteratively widens or narrows a nominal pulse toward a mask's outer violation boundary until an error condition is detected through either the DUT, BERT, or DSO. The AWG sequencer might then respond by jumping to a debug routine. In this case, the AWG brings a high level of repeatability and automation to an otherwise difficult characterization task.

The primary output of the AWG is, of course, analog, even when the desired signal is essentially a serial data stream. Frequently, however, telecom devices also require concurrent testing of digital trigger, gate, or clock inputs. For this reason, modern AWG architectures also provide from 10 to 24 channels of phase-synchronous digital output with clock speeds up to 1 GHz, and pattern depths of up to 4 Mwords.

Other telecom-related capabilities now available include built-in digital filtering. With this feature, designers can apply different filter distributions to the output and edit in the frequency domain. As a result, the telecom designer can quickly create "what-if" signal response conditions to fully exercise the prototype device or system. These filters also can be used to band-limit the AWG's built-in random noise generation when stress-testing the system. With the AWG 500 Series, this noise generation is truly random, as opposed to pseudo-noise generation, which is constrained by the generator's clock resolution. Some AWGs even provide comprehensive telecom jitter generation—from worst-case, single-bit to overall jitter—making it easier for the designer to create precise timing and amplitude impairments caused by jitter *(Fig. 2)*.

Testing A SONET Chip

All these waveform generation capabilities make AWGs extremely useful for thoroughly characterizing a telecom system during the prototype stage. The discussion that follows illustrates a real-world application. The example involves a stress test of a SONET transceiver chip designed for the STS-1 standard, where an AWG can be used to simulate the electrical signal prior to optical conversion. This particular chip was part of a larger system designed for the telecom market.

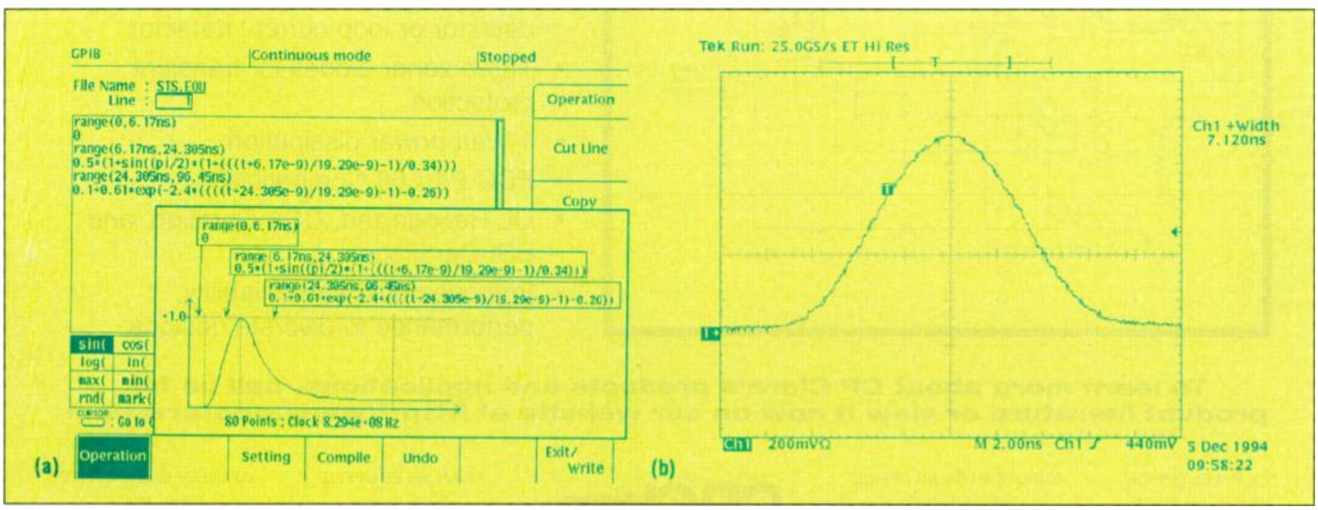
First, a BERT was used for the initial tests on the chip, which demonstrated infrequent, excessive bit-error conditions. The BERT did not, however, provide a clear reason for the failure, and due to the infrequency of the problem it was impossible to isolate or debug the cause. At this point, designers begin tracing back through the design to find the root of the occasional high error rates. While BERTs and protocol analyzers provide error counting and pass/fail test results, they do not provide the critical insight about the device's electrical signal that caused the error.

The designers first suspected a physical-layer problem, and decided to stress the circuit under test with an AWG. Their goal was to create signals that, when applied to the test circuit, would increase the frequency of error conditions. This would be accomplished by testing with a data stream where elements were constructed from a series of varying pulse shapes. These pulse shapes are designed to stress the circuit to STS-1 Bellcore mask standards.

Telecom signal creation using an AWG consists of three steps. First, we choose the desired nominal pulse shape, STS-1 in our example. Second, we select either an ideal data stream from the built-in AWG library or download a simulation with the appropriate timing elements. Finally, we use the super position capability of the AWG to convolve the two signals to form the final test signal.

The testing in our example started with a bit stream constructed with the STS-1 nominal pulse shapes selected from the AWG's internal library. The results provided infrequent error conditions similar to those observed with the BERT transmitter output.

Next, the equation editor was used to define the two outer zones of the STS-1 wide pulse mask *(Fig. 3)*. The waveform stressed the wide portion of the Bellcore mask standard. To do so, the wide pulse created was significantly longer than the pulse template because the template allowed the trailing end of the waveform to have a dc offset. Several unit intervals were used after the end of the defined pulse template to bring the dc level back down to zero so that there would be no nonphysical abrupt transitions in the resulting waveform after convolution.



3. To stress test a telecommunications device, nominal pulses like this STS-1 signal can be called from the AWG's library of waveforms (a), then widened using the generator's waveform editor until the device under test no longer passes the pulse accurately (b).

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Finally, using the graphic editor, the designers generated a waveform that stressed the narrow limits of the standard. Note the difference in the time scale between the wide pulse in Figure 3b and the narrow pulse shown in Figure 3a. The built-in waveform definition capability, like the convolution and equation editor, made it possible to develop and complete new tests in just a matter of hours as data became available on the type of waveforms that were causing the problems. Previously, designers would have had to laboriously piece these waveforms together using unwieldy text editors.

With these waveforms, the designers were able to efficiently test the chip to the limits of the STS-1 standard, and to observe how the device behaved under these stress conditions. The output from the AWG was connected to the SONET transceiver chip using a 75-ohm terminator. The output of the transceiver was connected to a BERT to measure the bit error rate.

Using the AWG-generated input, the evaluation testing clearly showed that the problem stemmed from a defect in the transceiver chip design. The errors were due to the chip's inability to accept a valid signal at the widest limit of the STS-1 Bellcore mask. After determining that, the designers were able to quickly rectify the problem. Without the AWG, the designers could have spent days, or even weeks, trying to find the design defect. By identifying problems like this one early in the design cycle, the designers gained confidence in the robustness and reliability of their final telecom product.

These examples demonstrate that telecommunications designers who have considered an AWG in the past, and found them lacking, should reconsider adding a state-of-the-art AWG to their bench. The newer instruments' functionality and ease of use provide a much more effective and efficient means for fully characterizing and debugging telecom designs.

Bruce Virell is a marketing manager for the AWG Signal Sources Group in Tektronix's Measurement Business Div. He received BS degrees in both engineering and business administration from the University of Portland, Ore.

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READER SERVICE 123

WRH

(continued from page 124)
nal power supply. The ORR24 costs $10,495. The SD-44 is priced at $5995. Delivery is in four weeks.

***Tektronix Measurement Business Div.**, P.O. Box 1520, Pittsfield, MA 01202; (800) 426-2200, press 3, code 1073; (413) 448-8002; Internet: www.tek.com/Measurement.*

CIRCLE 594

Video Analyzer Features Improved CPU, Jitter Analysis

The DVA184C Video BitAlyzer has been enhanced with improved CPU performance, a larger color LCD touch screen, and more hardware features for jitter analysis. New audio analysis software can test embedded auxiliary data, including AES/EBU digital audio. The instrument also features automated quality-control reporting and remote-control capabilities. Five new screen views display embedded packet summary, embedded packet details, embedded audio control, embedded audio PCM data, and embedded audio waveforms. The DVA184C permits multi-standard 525- and 625-line operation with both 4:3 and 16:9 aspect ratios and 270- or 360-MHz clock rates. Other features include a built-in multi-standard test pattern generator with still-store features; jitter inspection for stress testing; and a jitter FFT view that identifies systematic jitter interferences. The unit is certified for use in the European Union. Call for price and availability information.

***SyntheSys Research Inc.**, 3475-D Edison Way, Menlo Park, CA 94025; (650) 364-1853; (650) 364-5716; Internet: www.synthesysresearch.com.*

CIRCLE 595

Unit Offers Stimulus, Response For Digital Test In One Unit

The HP 81200 data generator/analyzer supplies stimulus and measurement capabilities for functional and parametric test in one mainframe. The instrument operates at speeds of 200, 330, or 660 Mbits/s with accuracy suitable for characterizing and verifying CMOS, biCMOS, and ECL devices. After comparing the captured data with the expected results, the analyzer displays errors, either highlighted in a state list or displayed as a bit error rate. Vectors can be loaded via GPIB or from ASCII files transferred to the built-in hard disk. A Windows NT based-interface and editor function simplifies modification of existing vectors or writing of new vectors. The unit stores one million vec-
(continued on page 128)

Manufacturers Of Communications Test Equipment

(cont. from p. 124)

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CIRCLE 503

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CIRCLE 504

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CIRCLE 508

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CIRCLE 509

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CIRCLE 510

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CIRCLE 511

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CIRCLE 513

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Research Triangle Park, NC 27709
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ATM, BER, ISD, JIM, LAN, OPM, OTR, PRO, WAN
CIRCLE 514

KEY

ATM: ATM test equipment
AUD: Audio analyzers
BER: Bit-error-rate testers
BSA: Broadband spectrum analyzers
CER: Cellular radio test sets
CMT: Communication mask testers
CSA: Communication signal analyzers
DDA: Digital data transmission analyzers
DMT: Digital modulation testers
DPG: Digital pulse generators
DSA: Dynamic signal analyzers
FLO: Fault locators
ISD: ISDN test equipment
JIG: Jitter generators
JIM: Jitter measurement equipment
LAN: LAN analyzers
MOA: Modulation analyzers
MTS: Microwave test sets
NOG: Noise generators
NWT: Network test sets
OEC: Optical-to-electrical converters
OPM: Optical power meters
PMR: Power meters
PRO: Protocol analyzers
TIA: Time-interval analyzers
TDR: Time-domain reflectometers
TLS: Telephone-line simulators
TRA: Transmission analyzers
VID: Video analyzer
WAN: WAN analyzers

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READER SERVICE 145

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tors, but the memory can be segmented to set up a sequence of loops for longer patterns. Pause segments are available so that dead times can be established without wasting memory. The unit performs logical EXOR addition of two or four channels to simulate events like glitches and irregular pulse widths and then measure maximum allowable distortion. A modular architecture permits flexibility in configuring the system. Prices range from $21,000 for a two-channel, 200-Mbit/s unit to $470,000 for a 120-channel, 660-Mbit platform. Delivery is in eight weeks.

Hewlett-Packard Co., Test and Measurement Org., P.O. Box 50637, Palo Alto, CA 94303-9512; (800) 452-4844, ext, 5662. **CIRCLE 596**

Dual Generator Allows Easier CDMA Testing

The 2026Q is an enhanced multi-source signal generator designed as a fully integrated radio-signal receiver for testing CDMA cellular and PCS handsets. The unit has two calibrated, combined RF output sources. They eliminate the need for mechanical switching and additional RF combining or signal conditioning for tests like dual-tone interference and successful hand-offs between channels and between cellular, DCS, and PCS bands.

In compliance with IS-95A, the 2026Q provides outputs from 800 MHz to 2.0 GHz at a combined output range of –127 to –13 dBm. The generator features a calibrated signal path for test set output and a return path from transceiver to the test set receiver input. This ensures high isolation between each of the transmit and receive paths between the test set, interfering signal sources, and transceiver under test. Each source can be modulated from an internal or external source in am, fm, pm, pulse, and 2/4-level FSK modes. The 2026Q costs $22,995. Delivery is in eight weeks.

Marconi Instruments Inc., 13600 Heritage Pkwy., Fort Worth, TX 76177; (800) 233-2955; (817) 224-9200; fax (817) 224-9201; Internet: www.marconi-instruments.com. **CIRCLE 597**

VXI Products Include Improved Mainframes, FireWire Interface, M-Module Carrier

A new family of VXIbus products is aimed at reducing the cost of VXI-based systems. At the same time, customers will be able to customize tests and increase the speed at which data move from VXI instruments to PCs. The products include four C-size mainframes, two improved B-size mainframes, an IEEE-1394 PC-to-VXI interface, a B-size M-module (mezzanine) carrier, and a C-size relay multiplexer.

The new 13-slot C-size mainframes feature a higher-performance fan, and front-panel monitor lights to check power-supply, fan, and backplane communication operation. A front-panel connector offers access to diagnostic information. The HP E8401A ($3695) has 550 W of usable power and the HP E8403A ($6395) 1000 W. The HP E8402A ($6395) and HP E8404A ($7495) supply 550 W and 1000 W, respectively, with enhanced monitoring.

A menu-driven, full-color LCD on the front allows users to check temperatures, voltages, currents, power, and fan speeds. It also shows system messages, warnings, usage history, and maintenance timer and RS-232 settings, using numeric, strip-chart, and histogram readouts.

The two nine-slot, B-size mainframes have dual fans for improved cooling to support more demanding modules, like multimeters and mezzanine modules. Both the HP E1300B ($2495) and HP 1301B ($3195), which comes with a keyboard and display, have HP-IB (GPIB) interfaces.

The HP E8491A PC-to-VXI interface ($2495) uses the IEEE-1394 FireWire technology, which transfers data at up to 400 Mbits/s and allows hot plug-in of other IEEE-1394 devices. Included are a one-slot C-size module, a 4.5-m cable, an IEEE-1394 interface card for a PCI-based PC, and a library of I/O software for Windows 95 and NT.

The HP E2250A M-module carrier ($1195) brings the industry-standard M-module technology to HP's B-size products. The carrier holds up to four M-modules.

The HP E8462A 256-channel relay multiplexer ($2995) is a one-slot C-size card that uses nonlatching armature relays handling up to 250 V and 125 W. A mix of various topologies can be used on one card, including two-, three-, and four-wire configurations.

Hewlett-Packard Co.
Test and Measurement Org.
P.O. Box 50637
Palo Alto, CA 94303-9512
(800) 452-4844, ext. 5706
CIRCLE 598

JOHN NOVELLINO

Multifunction Unit Tests CDMA Radios

The MS8606A digital mobile radio transmitter tester combines a transmitter tester, spectrum analyzer, power meter, and software to analyze signals in CDMA systems in the 300-kHz to 3-GHz range. The instrument–which complies with IS-95/-97/-98 standards–can make measurements using only an antenna port connection if rho is equal to or greater than 0.9. It makes the measurements in less than two seconds. In external trigger and short code search mode, the analysis takes less than four seconds. The unit measures frequency, timing error, code domain power, transmitter power, occupied bandwidth, and spurious emission. An audio measurement option can be used for TACS, J-TACS, and AMPS transmission evaluations. The MS8606A costs $26,500 and the CDMA software is $5000. Delivery is in six to eight weeks.

Anritsu Co., 1909 N. Glenville, Dr., Richardson, TX 75081; (800) 267-4878; (972) 644-5353; fax (972) 671-1877. **CIRCLE 599**

Software Turns A PC Into A Protocol Analyzer

Serialtest Async for Windows 95 is a software package that allows any PC to function as a full-featured serial data and protocol analyzer for testing

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DESIGN NOTES

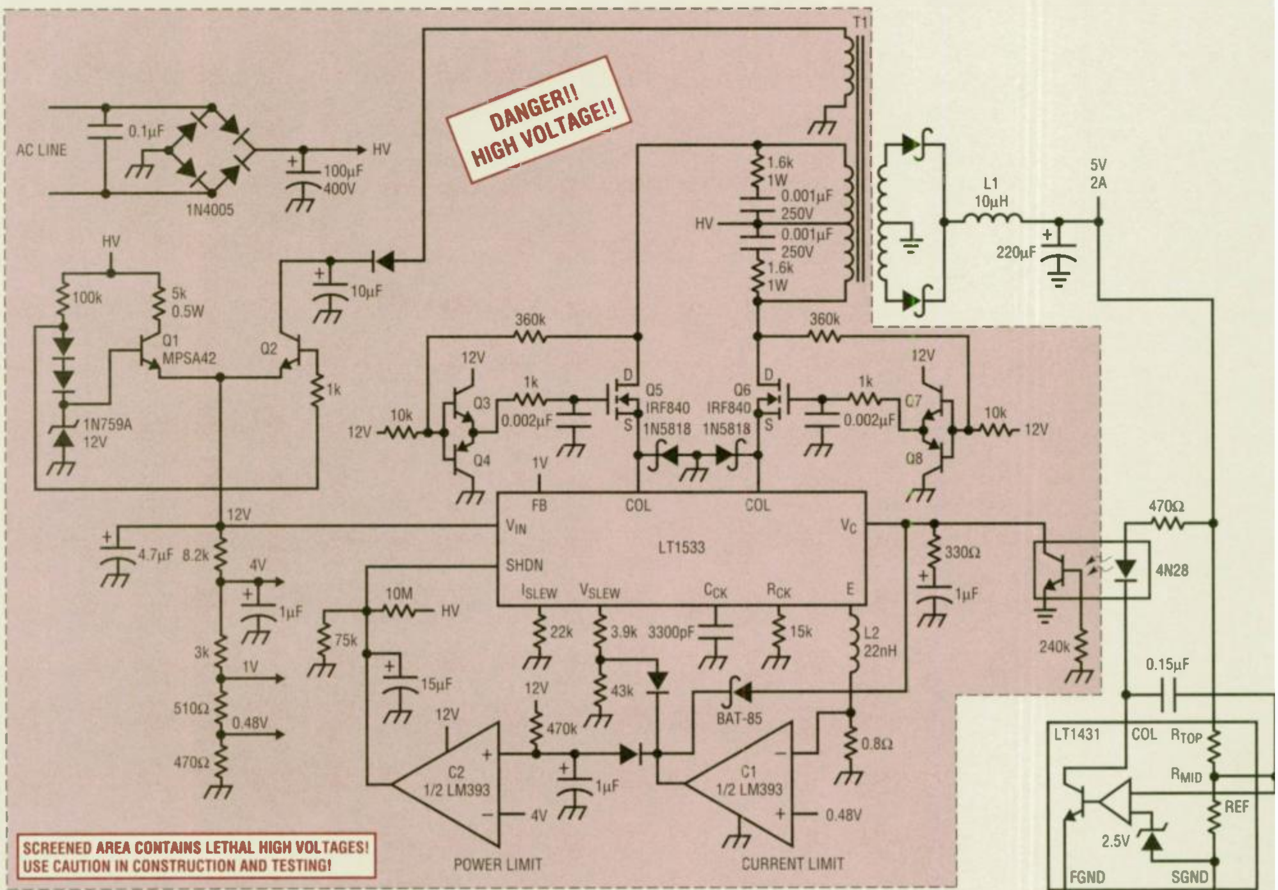
Off-Line Power Supply Does Not Require Filtering to Meet FCC Emission Requirements – Design Note 175

Jim Williams

Introduction

Off-line power supplies require input filtering components to meet FCC emission requirements. Additionally, board layout is usually quite critical, requiring considerable experimentation even for experienced off-line supply designers. These considerations derive from the wideband harmonic energy generated by the fast switching of traditional off-line supplies. A new device, the LT®1533 low noise switching regulator, eliminates these issues by continuous, closed-loop control of voltage and current switching times.[1] Additionally, the device's push-pull output drive eliminates the flyback interval of conventional approaches. This further reduces harmonics and smooths input current

[1] In depth coverage of this device, its use and performance verification appears in LTC Application Note 70, "A Monolithic Switching Regulator with 100μV Output Noise," by Jim Williams.



L1 = COILTRONICS UP-4
L2 = COILCRAFT B07T
NPN = 2N3904 UNLESS OTHERWISE NOTED
PNP = 2N3906
T1 = COILTRONICS CTX02-13978-X3

(Schottky diode symbol) = 20CJQ045(I.R.) UNLESS OTHERWISE NOTED
(diode symbol) = 1N4148
(ground symbol) = AC(HOT) RETURN
(ground symbol) = OUTPUT COMMON

Figure 1. 10W Off-Line Power Supply Passes FCC Emission Requirements Without Filter Components

drain characteristics. Although intended for DC/DC conversion, the LT1533 adapts nicely to off-line service, while eliminating emission, filtering, layout and noise concerns.

Circuitry Details

Figure 1 shows the supply. Q5 and Q6 drive T1, with a rectifier filter, the LT1431 and the optocoupler closing an isolated loop back to the LT1533. The LT1533 drives Q5 and Q6 in cascode fashion to achieve high voltage switching capability. It also continuously controls their current and voltage switching times, using the resistors at the I_{SLEW} and V_{SLEW} pins to set transition rates. FET current information is directly available, although FET voltage status is derived via the 360k–10k dividers and routed to the gates via the NPN-PNP followers. The source wave shapes, and hence the voltage slewing information at the LT1533 collector terminals, are nearly identical in shape to the drain waveforms.

Q1, Q2 and associated components provide a bootstrapped bias supply, with start-up transistor Q1 turning off once T1 begins supplying power to Q2. The resistor string at Q2's emitter furnishes various "housekeeping" bias potentials. The LT1533's internal 1A current limit is too high for effective overcurrent protection. Instead, current is sensed via the 0.8Ω shunt at the LT1533's emitter pin (E). C1, monitoring this point, goes low when current limit is exceeded. This pulls the V_C pin low and also accelerates voltage slew rate, resulting in fast limiting while minimizing instantaneous FET stress. Prolonged short-circuit conditions result in C2 going low, putting the circuit into shutdown. Once this occurs, the C1–C2 loop oscillates in a controlled manner, sampling current for about a millisecond every second or so. This action forms a power limit, preventing FET heating and eliminating heat sink requirements.

Performance Characteristics

Figure 2 shows waveforms for the power supply. Trace A is one FET source; traces B and C are its gate and drain waveforms, respectively. FET current is trace D. The cascoded drive maintains waveshape fidelity, even as the LT1533 tightly regulates voltage and current transition rates. The wideband harmonic activity typical of off-line supply waveforms is entirely absent. Power delivery to T1 (center screen, trace C) is particularly noteworthy. The waveshapes are smoothly controlled, and no high frequency content is observable.

Figure 3, a 30MHz wide spectral plot, shows circuit emissions well below FCC requirements. This data was taken with no input filtering LC components and a nominally nonoptimal layout.

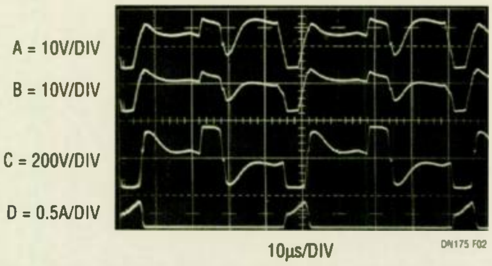


Figure 2. Waveforms for One of the Power Supplies' FETs Show No Wideband Harmonic Activity. LT1533 Provides Continuous Control of Voltage and Current Slewing. Result is Smoothly Controlled Waveshapes for FET Source (A), Gate (B) and Drain (C). FET Current is Trace D

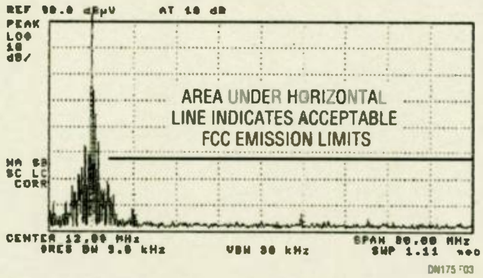


Figure 3. 30MHz Wide Spectral Plot Shows Circuit Emissions Well Below FCC Requirements Despite Lack of Traditional Filter Components

Output noise is composed of fundamental ripple residue, with essentially no wideband components. Typically, the low frequency ripple is below 50mV. If additional ripple attenuation is desired a 100μH–100μF LC section permits <100μV output noise. Figure 4 shows this in a 100MHz bandpass. Ripple and noise are so low that the oscilloscope requires a 40dB low noise preamplifier to even register a display (see footnote 1).

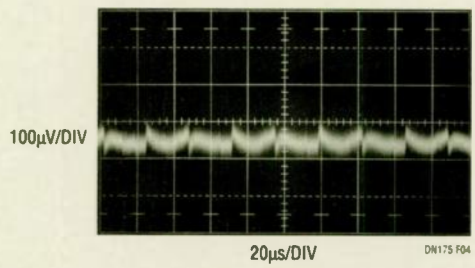


Figure 4. Power Supply Output Noise Below 100μV (100MHz Measurement Bandwidth) is Obtainable Using Additional Output LC Section. Without LC Section Wideband Harmonic is Still Absent, Although Fundamental Ripple is 50mV

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LINEAR TECHNOLOGY

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asynchronous serial data transmissions. To save time, users can review the data while it's being captured to a buffer or file. A statistics window summarizes activity on the link, presenting information on characters per second and utilization (current, average, and peak). The Windows 95 version comes with a quick start guide that outlines the screens and shows how they correspond to the older DOS version. Protocols supported include PPP, SLIP, and TCP/IP. User-defined or customized protocols also are supported through the use of the optional PDAedit tool. Serialtest Async costs $395, including the cable set. The upgrade from the DOS version to the Windows 95 version is $125. A Windows NT version was scheduled for release during the first quarter.

Frontline Test Equipment Inc., P.O. Box 7507, Charlottesville, VA 22906-7507; (804) 984-4500; fax (804) 984-4505; www.fte.com. **CIRCLE 600**

Analog Line Simulator Tests Data Services

The Model 3410 analog services telephone-line simulator is a PC-based development system for caller ID, facsimile, and specialized data services. The system, which works with DOS or Windows 95, supports all of the major standards for caller ID worldwide and a variety of modem and fax standards. It incorporates telephone-line impairments, such as white noise, long or short loop simulation, and variable line current feed. DSP technology precisely simulates numerous standard tones, call progress tones, and nonstandard single, dual, or triple tones. Frequencies, levels, and signal-to-noise ratio are programmable within 1-Hz and 1-dB accuracy. Included are a player/recorder that supports 16-bit linear PCM, μ-Law/A-Law, and ADPCM, and a signal-analysis meter. The unit features an isolated telephone battery feed with programmable line current from 15 to 80 mA. A software-controlled ring generator simulates ringing signals from a number of countries. Call for price and availability.

Rochelle Communications Inc., 8906 Wall St., Suite 205, Austin, TX 78754; (512) 339-8188; fax (512) 339-1299; e-mail: info@rochelle.com; Internet: www.rochelle.com. **CIRCLE 601**

500-MHz Analog Scope Writes At 5 div./ns

The TS-8500 analog oscilloscope features a dc-500-MHz bandwidth and a 5-div./ns writing speed. The scope, which can update displays as fast as 1 million times/s, uses a scan-converter tube to achieve exceptionally high brightness. It also allows storage of high-speed single-shot phenomena. Sensitivity is 2 mV/div. The four-channel, 10-trace instrument has full TV triggering with field and line selection for HDTV, NTSC, and PAL/SECAM; a sweep time of 500 ps/div. to 500 ms/div.; and cursors. A display persistence function allows real-time and stored waveforms to be superimposed. Dual time-base delay lets users zoom and examine two portions of a waveform in real-time. An NTSC video output of the waveform is available. Users can save up to 256 panel setups for future use. The TS-8500 costs $12,495. Delivery is within 16 weeks.

Iwatsu America Inc., Test and Measurement Div., 430 Commerce Blvd., Carlstadt, NJ 07072; (201) 935-8486; fax (201) 935-8533; e-mail: iwatsu@access.com; www.iwatsu.com. **CIRCLE 602**

Arbs Feature 1-Gsample Clocks, Comm Menu

A pair of arbitrary-waveform generators offer 1-Gsample/s clock rates, 10-bit vertical resolution, and up to 4-Mbyte/channel memories, along with application-specific capabilities for use in fields like communication test. The one-channel AWG 510 and two-channel AWG 520 also feature a 10-bit digital output. The sources can simulate real-world signal degradations such as noise, jitter, and fading.

An integrated hardware noise generator creates truly random white noise. Jitter can be simulated with timing resolution to 2 ns. Two application menus allow users to output data streams with isolated bit-pulse shapes to industry standards. In addition to the disk-drive menu, a new communications menu accesses 20 nominal signal standards–like DS2, OC3, and FC266E–immediately displaying amplitude, width, timing, and pattern. Waveform-editing features include a graphical editor, several digital and analog editors, and a script editor. Users also can build waveforms from multiple segments with the units' real-time sequencing capability. Prices start at $21,995 for the AWG 510 and $28,995 for the AWG 520. Delivery is in four weeks.

Tektronix Inc., Measurement Business Div., P.O. Box 1520, Pittsfield, MA 01202; (800) 426-2200, press 3, code 1069; www.tek.com/Measurement. **CIRCLE 602**

Emulator Handles 8051 Family At Up To 30 MHz

The Cactus-8051 emulates more than 30 variants of the 8051 family of microprocessors using a set of target adapters. The low-cost unit offers all of the features of higher-cost units except real-time trace. It supports processor speeds to 30 MHz at zero wait states, includes 128k of emulation RAM for code downloads, and features 100 hardware breakpoints. Users can stop immediately or defer the stop until a particular hardware breakpoint occurs up to 65,000 times. The emulator comes with a source-level debugger that provides the shell needed to debug C and assembly-language code. All compilers are supported. The Cactus-8051costs $1250.

Softaid Inc., 8310 Guilford Rd., Columbia, MD 21046; (800) 433-8812; (410) 290-7760. **CIRCLE 603**

A/D Modules Connect To PCs Through USB

The Personal Daq modules are the first in a family of USB-based data-acquisition products. Special power-management circuitry allows the two full-featured modules to draw less than 2 W, so they can be powered through the USB with no external power supply needed. The Personal Daq/55 offers 22-bit analog-to-digital resolution, 10 single-ended (five differential) analog or thermocouple channels, 16 software programmable ranges (±30 mV to ±20 V full scale), 500-V optical isolation, eight digital I/O lines, and two frequency/pulse inputs.

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The Personal Daq/56 supplies twice the channel capacity. The systems accept volts, frequency, and digital inputs with no additional hardware needed. Expansion modules and the USB's hub capability allow large systems with multiple units. The modules come with DaqView graphical display and data-acquisition software, which requires no programming to configure a system. The Personal Daq/55 costs $695, and the Personal Daq 56 is $995. The PDQ1 expansion module with 20 single-ended channels and 16 digital I/O channels, and the PDQ2 with 40 single-ended channels are each $495.

IOtech, 25971 Cannon Rd., Cleveland, OH 44146; (440) 439-4091; fax (440) 439-4093; e-mail: sales@iotech.com; www.iotech.com.

CIRCLE 604

JTAG-Based Emulator Accesses i960RX/HX Debug Facilities

The EMDT/960Rx/Hx emulator uses the IEEE-1149.1 (JTAG) port on the Intel i960RX and HX processors to gain access to the devices' debug facilities. The emulator eliminates the need for external pods, which reduces cost and electrical loading of the target system and allows the instrument to automatically support any clock speed at which the processor runs. Use of the JTAG interface also ensures the user of processor access even if the device "hangs" or otherwise runs out of control. Users can download programs and data to any part of the system RAM through the JTAG port without the need for a resident loader program or ROM emulator. In addition, the ISA-bus-compatible JTAG controller board can be used for boundary-scan inteconnect testing of the prototype design or of the final product in manufacturing. The EMDT/960Rx/Hx comes with a full-featured Windows-based source-level debugger and costs $6950. JN

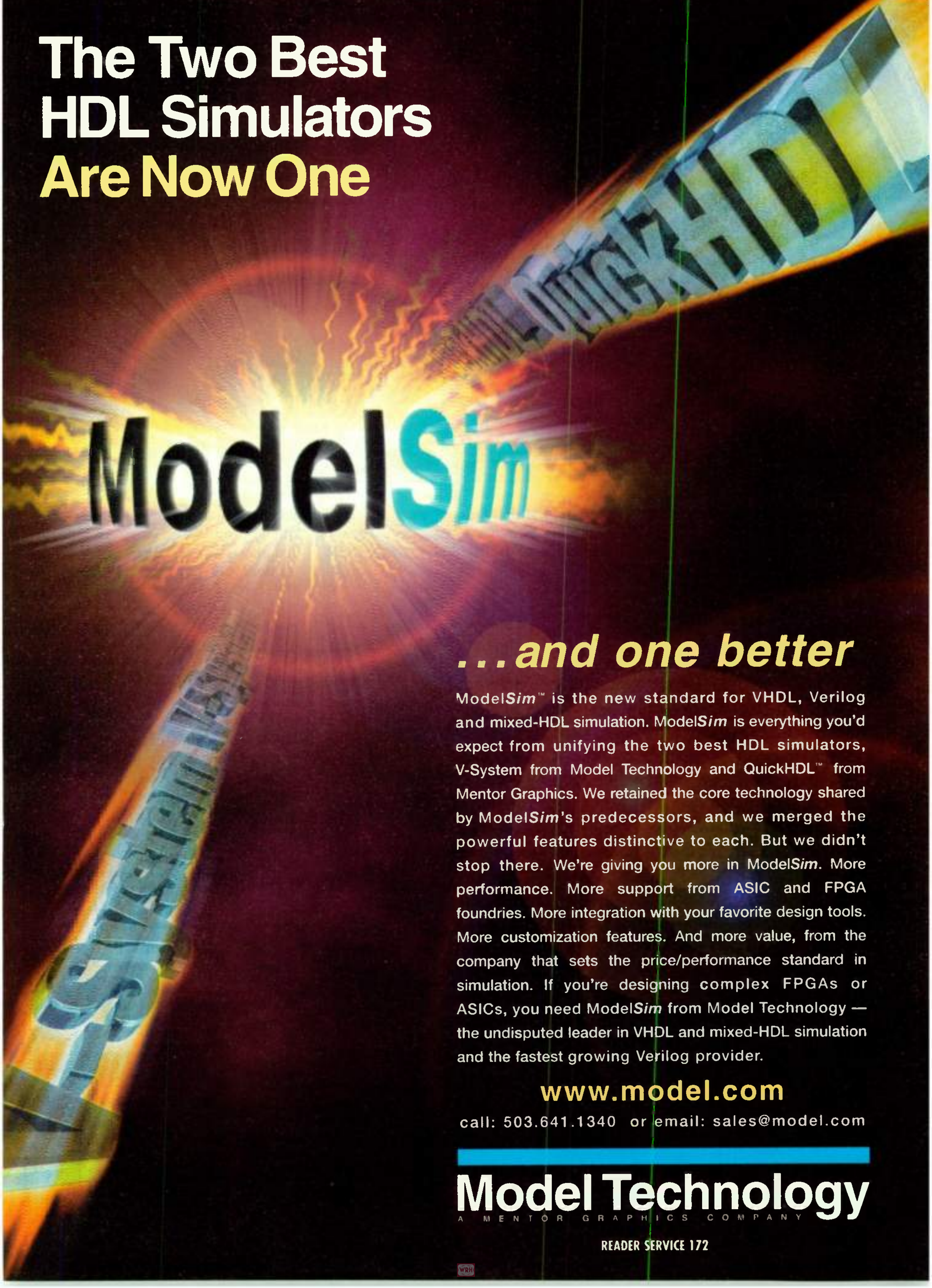
Corelis Inc., 12607 Hiddencreek Way; Suite H, Cerritos, CA 90703-2146; (562) 926-6727; fax (562) 404-6196. **CIRCLE 605**

Thermocouple Data Module Plugs Into PC Parallel Port

The AD-TDA8 is a thermocouple data-acquisition module that plugs into the parallel port of Windows-based computers. The eight-channel unit, which samples at up to 15 samples/s, supports type J (–50 to +800°C), K (–50 to +1000°C), and T (–25 to +500°C), thermocouples. Resolution is ±1°C, and accuracy at 25°C is ±1°C. Users need only to plug the AD-TDA8 into the PC's parallel port, load the included software, and connect the thermocouples. The module consumes 50 mW, which it gets from the parallel port's signal lines. An optional screw-terminal panel simplifies termination of the thermocouples. The AD-TDA8 costs $170 and the screw-terminal panel accessory is $30. Both are available from stock.

Keithley Instruments Inc., 28775, Aurora Rd., Cleveland, OH 44139-1891; (888) 534-8453; (440) 248-0400; fax (440) 248-6168; e-mail: product_info@keithley.com; www.keithley.com.

CIRCLE 606



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Circle 520

PC Signal Generator Uses A C++ Class

OSCAR RAMOS
Ciudad Universitaria, Agencia Postal 4, Ciudad Universitaria, 5000 Cordoba, Argentina, phone: (0054-51) 333037; fax: (0054-51) 334158.

Described here is a class used in the generation of audio frequency sinusoidal signals and white noise using a PC. The generator hardware must include a DAC of no more than 16-bit resolution and must use the double-buffered memory technique. This means that while one DMA channel transfers the data from one buffer (buffer1) to the converter, the CPU refreshes the other buffer (buffer2) with new data. Also, each time that the DMA finishes an operation on a buffer, an interrupt to the CPU must be generated. The buffers must be allocated in contiguous memory locations.

To produce sinusoidal waves, a fractional-N synthesizer is emulated by the class *(see the figure)*. The adder inputs are fed by a constant Index number and by the output address accumulator. The adder generates a new address equal to the sum of the previous address and the Index number, synchronized with the sampling frequency clock (SamFrq). The most weighted outputs of the address accumulator are connected to the ROM address lines, which contains the samples of a sinusoidal waveform period. The ROM data lines are connected to the DAC, reproducing an analog signal corresponding to the ROM samples. The adder rate is:

$$f_{adder} = SamFrq*Index/adder\_size$$

```
void interrupt mayIntFunc(void)
{
unsigned points = BufferSize / 2;
unsigned i;
        for (i=0; i < points; i++)
            BufferPtr[Buffer Index Base + i] = Gen -> getValue();
        BufferIndexBase = BufferIndexBase ? 0 : BufferSize / 2;
}

Where:
        BufferSize: Size of DMA buffer (buffer1 + buffer2)
        BufferPtr: Pointer to DMA buffer
        BufferIndexBase: Offset (zero for buffer1 and BufferSize/2 for buffer2)
        Gen: Pointer to EdGen object
```

If SamFrq/adder_ size = 1 (condition1), the output frequency is equal to the Index. When adder_size = ROMsize*factor, then:

$$factor = SamFrq/ROMsize$$

Given the sampling frequency and the ROMsize, factor is the value that makes (condition1) true. The output signal frequency is equal to the Index number. The frequency resolution of the generator is fixed by the variable type of the Index.

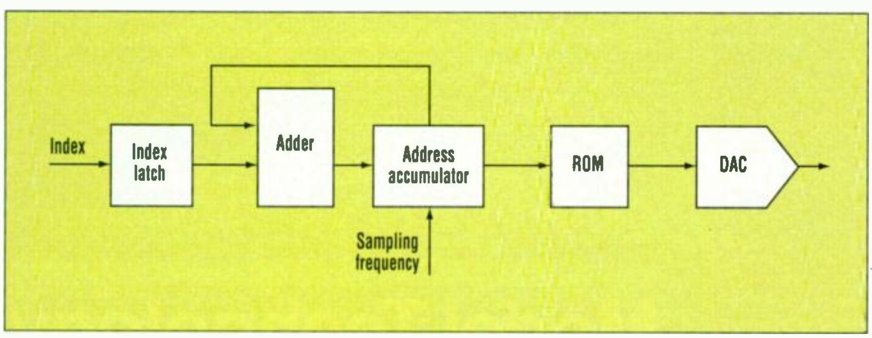
The function int random (int value-1) from Borland is used to generate white noise. It returns a random integer, between 0 and –1.

The C++ class EdGen is declared in the EdGen.h file *(Listing 1)*. The class could be initialized in two modes—noise or tone—according to the constructor used. In the noise mode, the default constructor must be used. The tone constructor takes three unsigned integers as arguments: sampling frequency, tone frequency, and tone initial phase. The last one is a default argument and may be used to initialize the starting phase of the tone.

An object initialized in one mode can be changed "at flight" to the other one, overwriting the public data member SignalType. However, if the object was initialized in the noise mode, the member function InitTone must be called before changing to the tone mode. The member function gelvalue returns a new value for the tone or noise each time it's called. The members functions setToneFrq and getToneFrq may be used to set or get the tone frequency without stopping the generation. These functions are useful to produce frequency sweeps.

As mentioned previously, the hardware must generate an interrupt to the CPU at the end of each DMA transfer. A sample interrupt service routine is shown *(Listing 2)*.

If the hardware has several channels, independent objects EdGen can be created for each channel.



A fractional-N synthesizer is emulated by a class to produce sinusoidal waves.

IFD WINNER

J. Jayapandian, IGCAR, Material Science Division, Kalpakkam. PIN 603102, Tamil Nadu, India; msd@igcar.ernet.in. The idea: *"Use A FET As A Linear Temperature Sensor."* May 27, 1997 Issue.

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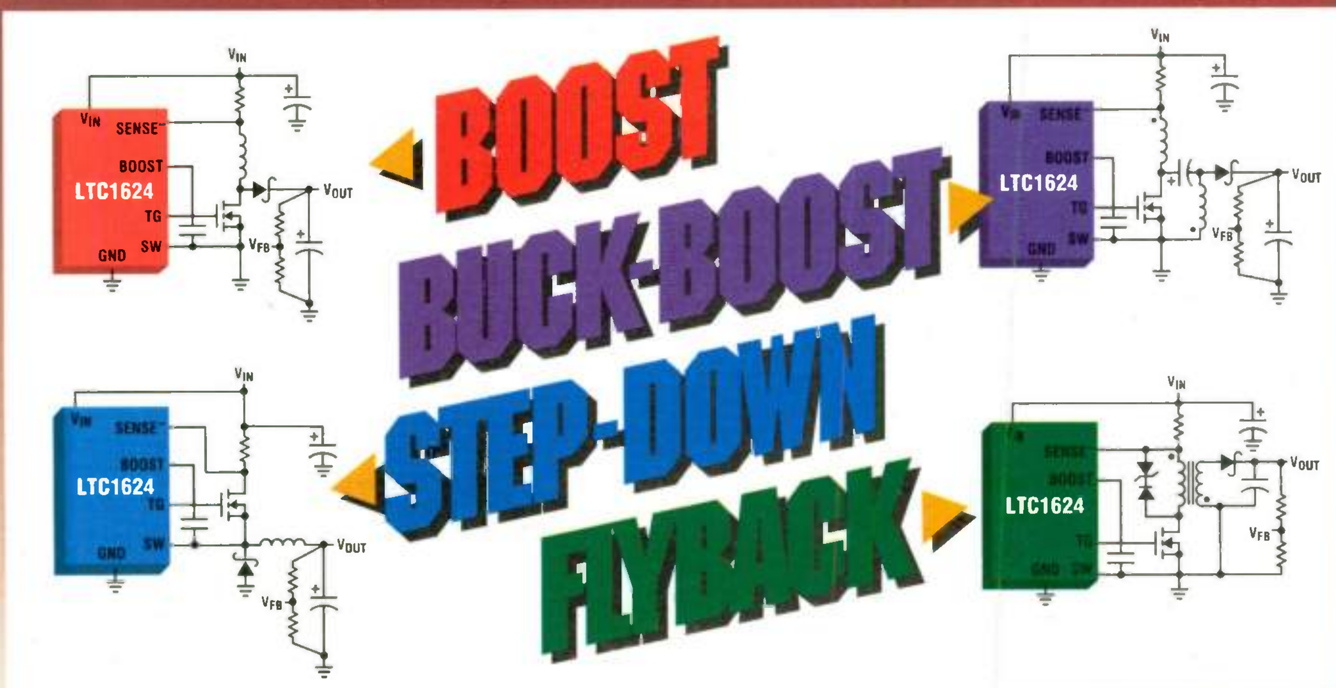

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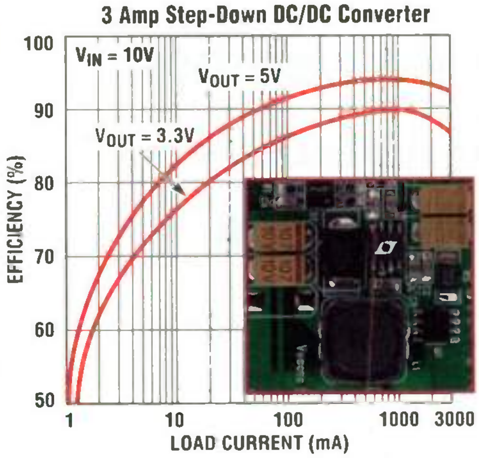

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```
//------ ---------------------------
// Include file of edgen.cpp
// by Oscar Ramos
//---------------------------------
#ifndet _cplusplus
#error Must use C++ for the type EdGen
#endif

#if !defined ( _EDGEN_H)
#define _EDGEN_H
const unsigned      Sin = 0,
                    Noise = 1;
const               MinToneFrq = 20,
                    MaxToneFrq = 20000;
class EdGen
{
private:
        unsigned SamFrq;
        unsigned Index;
        unsigned address;
        float factor;
public:
        int   SignalValue;
        unsigned SignalType;
        EdGen( unsigned samfrq, unsigned fo, unsigned phase=0 );
        EdGen( ) {SignalType = Noise;}
        void InitTone( unsigned samfrq, unsigned fo, unsigned phase=0 )
                {EdGen::EdGen(samfrq, fo, phase);}
        void setToneFrq( unsigned fo );
        unsigned getToneFrq( ) { return Index;}
        int getValue():
};
#endif
//------- end of EDGEN.H -------

//---------------------------------
// File edgen.cpp
// by Oscar Ramos
//---------------------------------
#include <math.h>
#include <stdlib.h>
#include "edgen.h"
const char          NoError = 0,
                    Error = 1;
const float         AliasingFactor = 2;
//ROM size
const unsigned      ROMsize = 1000;
//ROM pointer
int*                ROMPtr;
//Definitions of non-member EdGen function
int                 InitToneValues():

EdGen::EdGen( unsigned samfrq, unsigned fo, unsigned phase)
{
        if( ROMPtr == 0 )
                InitToneValues();
        SamFrq = samfrq;
        Index = fo;
        address = phase;
        factor = (float) SamFrq/(float) ROMsize;
        SignalType = Sin;
}

int EdGen::getValue()
{
        unsigned        idx = 0;
        switch( SignalType ) {
                case Sin:
                        if ( address >= SamFrq )
                                address -= SamFrq;
                        idx = (unsigned) ( (float) address/factor );
                        address += Index;
                        SignalValue = ROMPtr[ idx ];
                        break;
                case Noise:
                        SignalValue = random( 0x7FFF );
                        break;
                default:
                        SignalValue = 0;
        }
        return SignalValue;
}

void EdGen:: setToneFrq( unsigned fo )
{
        if ( fo <= MinToneFrq )
                Index = MinToneFrq;
        else if ( fo >= (float) SamFrq/AliasingFactor )
                Index = (float)SamFrq/AliasingFactor;
        else Index = fo;
}

int InitToneValues()
{
        double  angle = 2*M_PI/ROMsize;
        int     I =7;

        ROMPtr = new int[ ROMsize ];
        if ( ROMPtr == 0 ) return Error;
        for ( i = 0; i < ROMsize; i++ )
                ROMPtr [i] = (int) (0x7FFF*sin( angle*i ) );
        return NoError;
}
// end of file EDGEN.cpp
```

Circle 521

Servo-Motor Acceleration Control Via Armature Current Integration

W. STEPHEN WOODWARD
Venable Hall, CB3290, University of North Carolina, Chapel Hill, NC 27599-3290; e-mail: woodward@net.chem.unc.edu.

Whenever the speed of a dc servo motor must be controlled with absolute accuracy, there's no substitute for tachometer-based feedback combined with a full-blown servo loop. But in other applications, adequate steady-state precision and sometimes superior dynamic performance can be had by taking advantage of the built-in physical constants of the motor itself.

For example, the fact that every permanent magnet dc motor has a fixed relationship between RPM and armature back-EMF means that a fair job of constant speed operation can be accomplished merely by driving the motor from a well-regulated power supply. Even better speed regulation can be achieved, sometimes rivaling that offered by tachometer feedback, by adding a positive-feedback term to the drive voltage that's proportional to armature current. If this term is adjusted so as to cancel armature resistance (approximately equal to rated-voltage/locked-rotor-stall current), motor speed will remain nearly constant over a wide range of loads.

Similarly, a stable data-sheet-specified relationship exists in every PM motor between armature current and output torque and therefore between armature current and acceleration. It follows that a constant maxi-

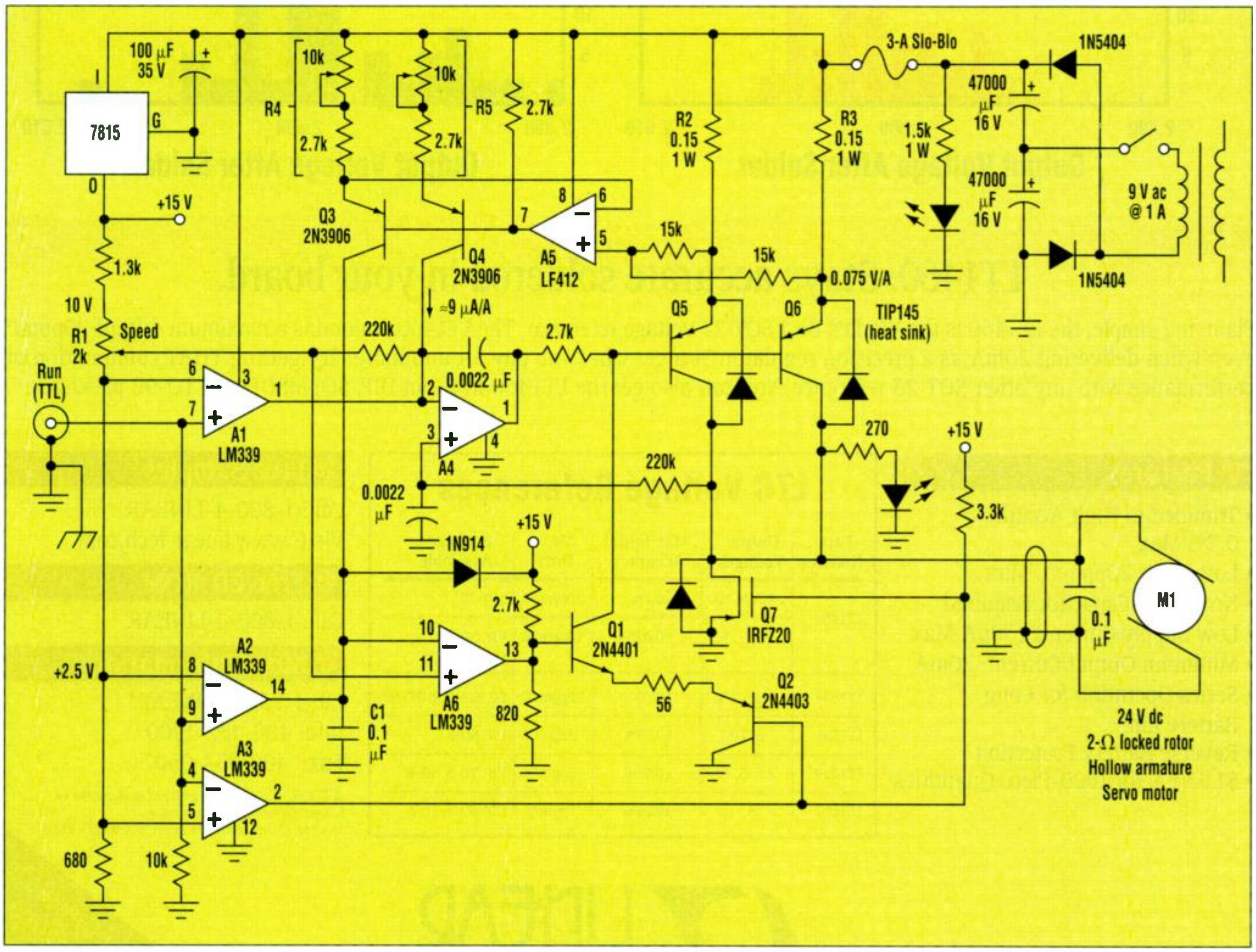
mum-rate spin-up to a specified speed can be achieved by applying full supply voltage until the integrated charge passed by the armature equals a value proportional to the setpoint speed.

This is the control principle employed in the figure. When TTL-/CMOS-compatible input RUN goes high, comparators A1 and A3 enable power amplifier A4+Q5+Q6, turning on the drive to motor M1. Simultaneously, comparator A2 releases the reset on armature current integration capacitor C1. Armature current monitor A5+Q3 injects a current onto C1 that's proportional to armature current as sensed by emitter resistors R2 and R3 with the constant of proportionality adjusted by R4. Comparator A6 compares the resulting C1 voltage ramp to the setpoint pot R1 (SPEED). So long as V(C1) < V(R1), A6 holds the motor drive Darlingtons Q5 and A6 in saturation, thus applying the full unregulated supply voltage to M1.

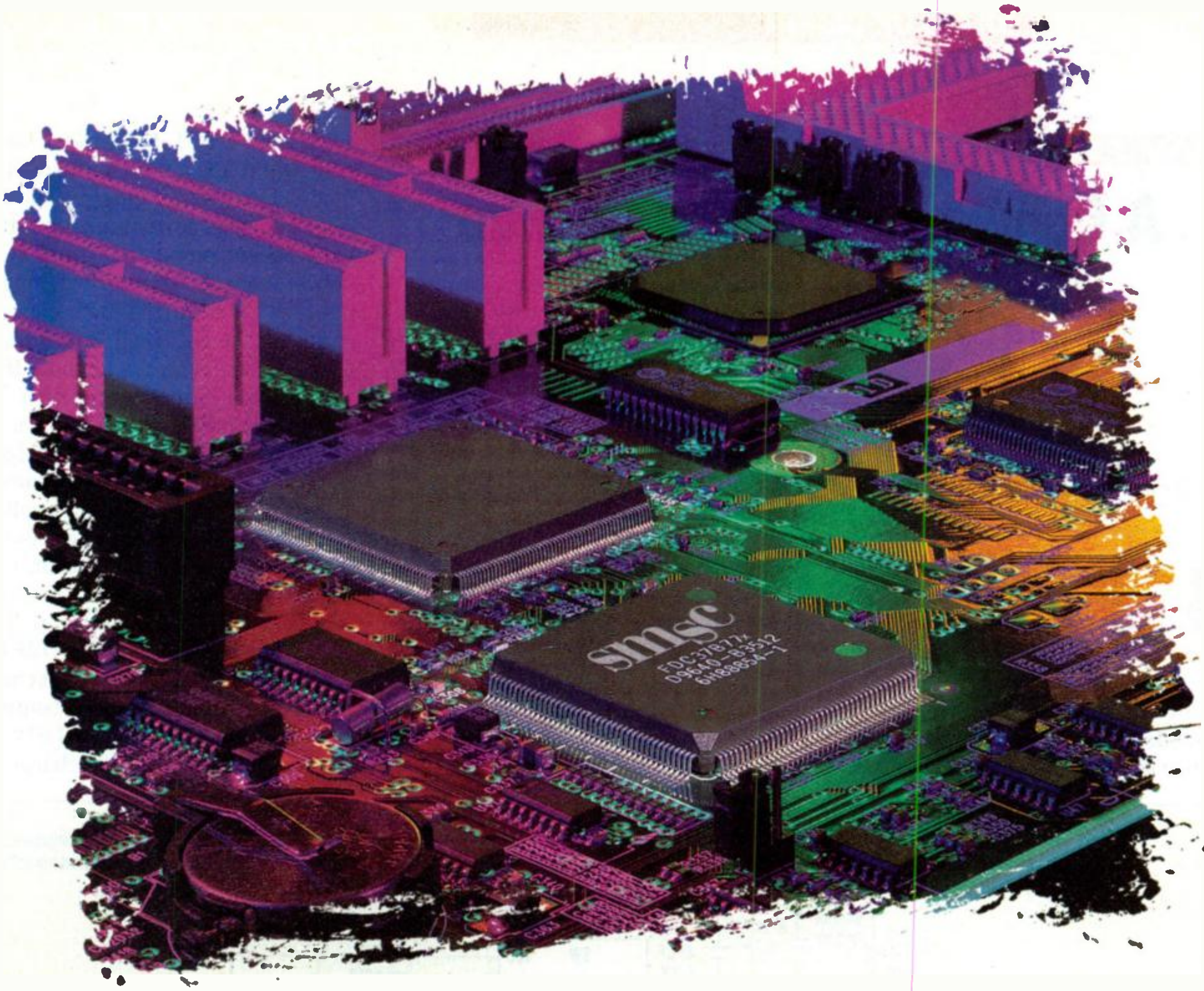
This full-throttle acceleration phase continues until C1's integrated charge causes V(C1) = V(R1). A6 pin 13 then goes low, turning off Q1 and passing control of the Q5 and Q6 Darlingtons over to A4. A4 then strives to hold M1's speed constant by applying the armature-voltage tricks described in the first paragraph. Feedback from M1 to A4 pin 3 provide basic voltage regulation, while the current-proportional signal from R5 and Q4 provide armature-resistance-canceling positive feedback. Properly adjusting R4 will result in overshoot-free initial spin-up, while careful trimming of R5 provides constant motor speed against changes in load friction. When the RUN control logic input returns low, Q7 effectively shorts across the motor armature to provide dynamic braking and ensure rapid M1 deceleration.

This circuit was designed for service in a magnetic resonance research application in which a liquid sample must be held stationary during excitation with RF pulses, and then spun up to 1200 to 3600 RPM as quickly as possible. The 24-V hollow-rotor dc motor used for M1 achieves loaded acceleration rates approaching 1,000,000 RPM/sec. Spin-up times in the single-digit-millisecond range are therefore easily achieved. Deceleration performance is similarly enthusiastic.

The magnetic resonance application entailed only a relatively low duty factor for motor operation. Therefore, the simple power supply illustrated (augmented with buckets—about 7 J—of energy-storage capacitance to satisfy the big startup surge) was adequate.



A maximum-rate spin-up to a specified speed can be achieved by applying full supply voltage until the integrated armature current equals a value proportional to the setpoint speed. This particular circuit was designed for a magnetic resonance research application.



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Circle 522

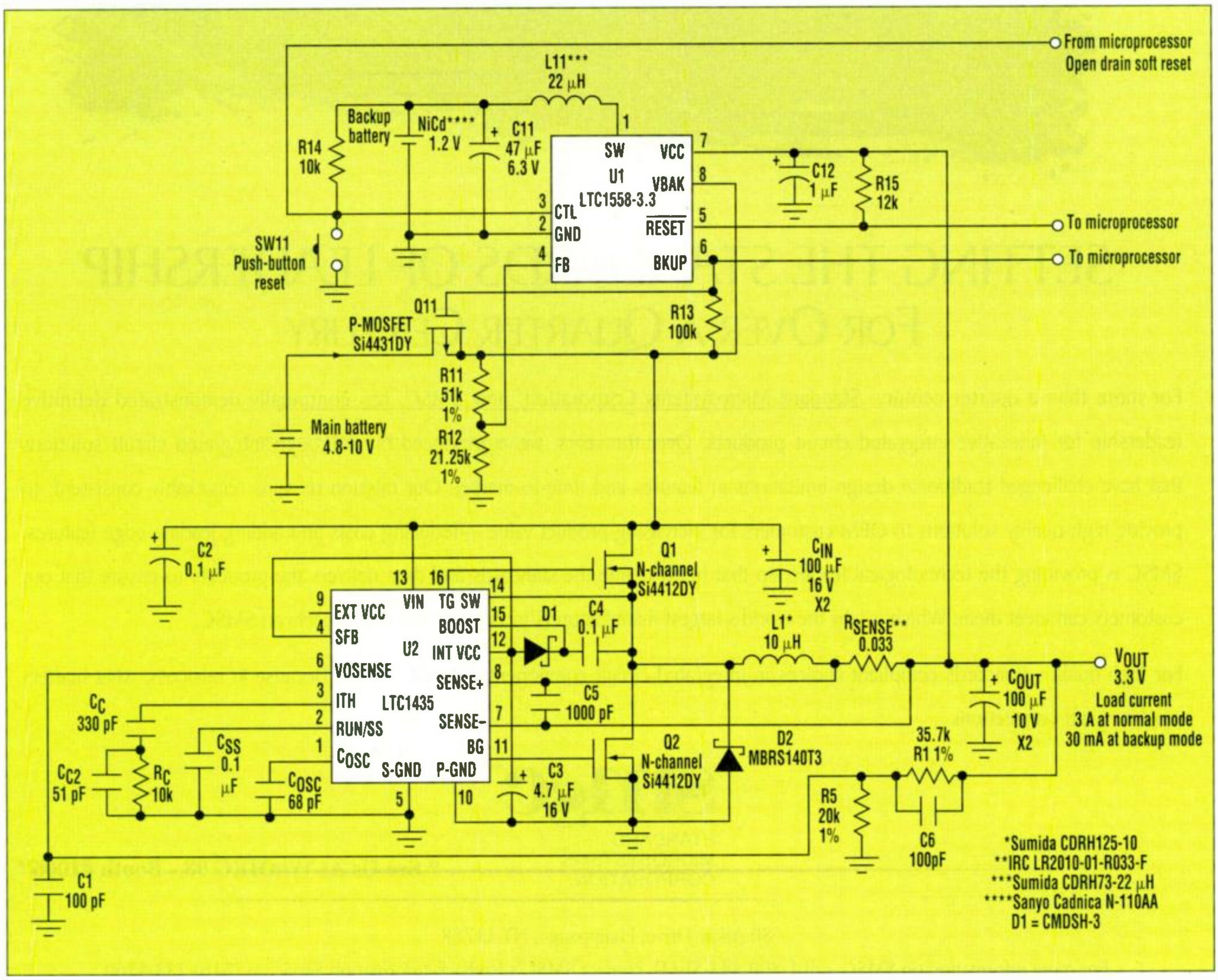
A Complete Battery Backup Solution Using A Rechargeable NiCd Cell

L.Y. LIN and S.H. LIM
Linear Technology Corp., 1630 McCarthy Blvd., Milpitas, CA 95035-7417; (408) 432-1900; fax (408) 434-0507.

Battery-powered systems, including notebook computers, personal digital assistants (PDAs), and portable instruments, require backup systems to keep the memory alive while the main battery is being replaced. The most common solution is to use an expensive, nonrechargeable lithium battery. This solution requires low-battery detection, necessitates battery access, and invites inadvertent battery removal.

The circuit presented here eliminates these problems by permitting the use of a single, low-cost 1.2-V rechargeable nickel-cadmium (NiCd) cell *(Fig. 1)*. U1, an LTC1558 battery backup controller, has a built-in fast/trickle-mode charger that charges the NiCd cell when main power is present. It provides backup power to U2, an LTC1435 synchronous step-down switching regulator. The backup circuit components consist of the NiCd cell, R11-R14, C11-C12, L11, and Q11. SW11 and R15 provide a soft or hard reset function.

During normal operation, U2 is powered from the main battery, which can range from 4.8 V to 10 V (for example, a 2-series or 2-series times 2-parallel Li-Ion battery pack, or the like) and generates the 3.3-V system output. U1 operates in standby mode. In standby mode, U1's BKUP (backup) pin is pulled low and p-channel MOSFET is turned on. The NiCd cell is fast charged by a 15-mA current source connected between the U1's V_{CC} and SW pins. Once the NiCd cell is fully charged (ac-



1. This battery backup system uses the LTC1435 synchronous step-down switching regulator as the main system regulator.

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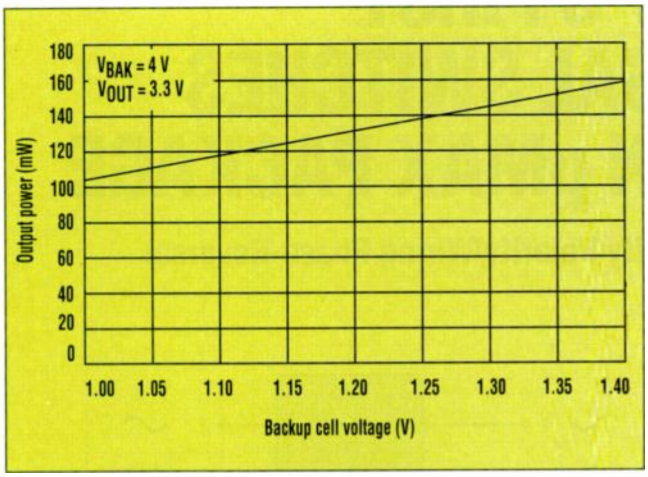
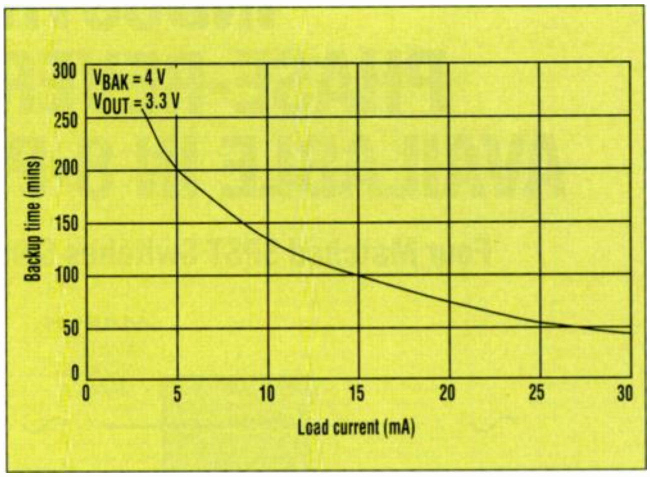
Circle No. 158 - For International



2. Shown is the maximum 3.3-V output power available versus the backup voltage on the NiCd battery.



3. Results shown here are the backup time versus the 3.3-V output load current using a Sanyo Cadnica N-110AA cell.

cording to U1's gas-gauge counter), U1 trickle charges the NiCd cell. R14 sets the trickle-charge current according to the formula $I_{(TRICKLE)} = 10 \times (V_{NiCd} - 0.5)/R14$. The trickle-charge current is set to overcome the NiCd cells' self-discharge current, thereby maintaining the cells' full charge.

The main battery voltage is scaled down through resistor-divider R11-R12 and monitored by U1 via the FB pin. If the voltage on the FB pin drops 7.5% below the internal 1.272-V reference voltage (due to discharging or exchanging the main battery), the system enters backup mode.

In backup mode, U1's internal switches and L11 form a synchronous boost converter that generates a regulated 4 V at V_{BAK}. U2 operates from this supply voltage to generate the 3.3-V output voltage. The BKUP pin is pulled high by R13 and Q11 turns off, leaving its body diode reverse-biased. The BKUP pin also signals the system microprocessor. C11, a 47-µF capacitor, provides a low impedance bypass to handle the boost converter's transient load current. Otherwise, the voltage drop across the NiCd cells' internal resistance would activate the U1's undervoltage-lockout function. Figure 2 shows the maximum output power available at the 3.3-V output versus the NiCd cell voltage.

Over 100 mW of output power is achieved for a NiCd cell voltage greater than 1 V. Figure 3 shows the backup time versus the 3.3-V load current using a Sanyo Cadnica N-110AA cell (standard series with a capacity of 110 mAh). Over one hour of backup time is realized for less than 80 mW of 3.3-V output power.

When a new battery pack is inserted, Q11's body diode forward-biases. Once the voltage at the FB pin increases to more than 6% below V_{REF}, the boost converter is disabled and the system returns to normal mode. The BKUP pin pulls low and turns Q11 back on, allowing the new battery pack to supply input power to U2. U1 now replenishes the charge removed from the NiCd cell through the internal charger and gas-gauge counter.

Circle 523

Digital Logic Interface For Power-MOSFET Control

V. LAKSHMINARAYANAN
12/46 Udani Layout, Cambridge Rd., Ulsoor, Bangalore-560 008, India.

Power MOSFETs have become increasingly popular for use in numerous high-power applications. But the major drawback of a typical industrial power MOSFET is that it requires a minimum gate threshold voltage of about 4 V (preferably about 8 V for conducting the rated drain current). This makes it difficult to directly interface a power MOSFET to digital logic such as TTL. The circuit presented in this design idea makes it possible to directly interface a power MOSFET to digital logic, including microprocessor-based systems. The circuit doesn't use any custom MOSFET drivers, transformers, or inductors to boost the voltage to the required level.

The circuit consists of a 555 timer configured as an astable-multivibrator with a frequency around 70 kHz. ON/OFF control of the astable is achieved using the Reset pin (pin 4) as a control input. When the Reset pin of the timer is HIGH it oscillates; when it's LOW, the oscillations are inhibited. The output of the astable feeds a diode-capacitor voltage doubler consisting of diodes D1 and D2 and capacitors C3 and C4.The output of the voltage doubler is about 8.5 V.

The digital logic control input is interfaced to the timer's Reset pin through a 4N35 optocoupler. The optocoupler provides isolation between the logic circuit and the high-voltage load circuit. When the digital logic input is HIGH, the input diode of the optocoupler is OFF and its output transistor is also OFF. This pulls the Reset pin of the timer HIGH and it oscillates, generating a voltage of about 8.5 V at the output of the voltage doubler circuit. The

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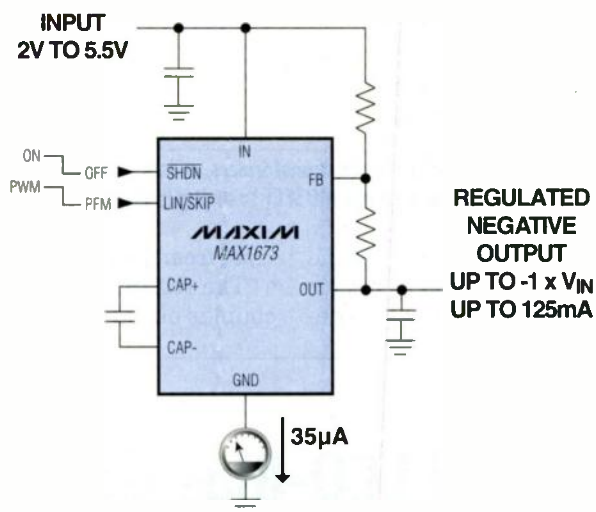
  - **Up to 125mA Output Current**
- **2V to 5.5V Input Range**
- **Select Pulse-Skipping or Constant 350kHz Operation**
- **35µA Quiescent Supply Current (Pulse-Skipping Mode)**
- **1µA Shutdown Current**

Regulated Negative Supply Needs Only 35µA



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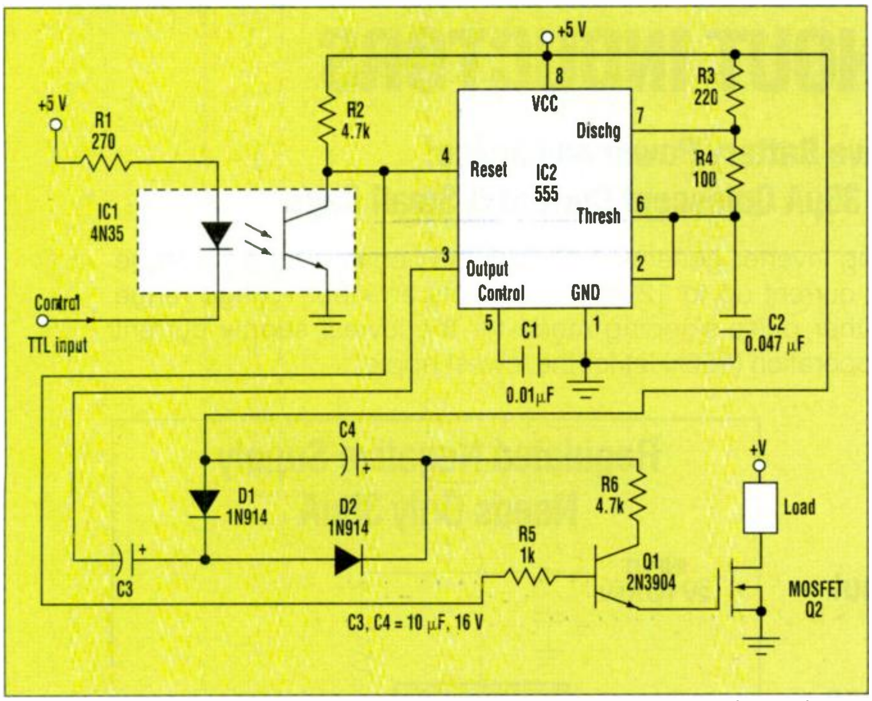


Without using any custom MOSFET drivers, transformers, or inductors, this digital-control circuit allows a direct interface of a power MOSFET to digital logic.

output of the optocoupler also feeds the base terminal of the 2N3904 transistor switch, whose collector supply is derived from the voltage doubler output.

The HIGH logic state of the optocoupler output turns the transistor ON. About 8 V is available at the gate terminal of the MOSFET, which is sufficient to turn it ON and allow conduction of the rated drain current through the channel. When the control logic input to the optocoupler is LOW, its input diode conducts and the output transistor is ON. This pulls the Reset pin of the timer LOW, the astable oscillations are inhibited, and the transistor switch is turned OFF. Because there are no oscillations from the timer, the voltage doubler doesn't generate any voltage. With the transistor switch being OFF, no voltage appears at the MOSFET gate and the device is non-conducting.

Therefore, when the control logic input is HIGH, the MOSFET is ON. When it is LOW, the MOSFET is OFF, accomplishing direct control by the digital logic in the interface circuit. The load in the MOSFET circuit could be a stepper-motor winding, a solenoid coil, etc.

Because the interface circuit doesn't use any coils or transformers, it avoids EMI problems. Also, since no custom MOSFET driver is used, it's a low-cost option as well. This interface can find use in many industrial applications.

Circle 524

Regulated LCD-Bias Generator Requires No Inductor

GARY HURTZ
Maxim Integrated Products, 120 San Gabriel Dr., Sunnyvale, CA 94086; (408) 737-7600.

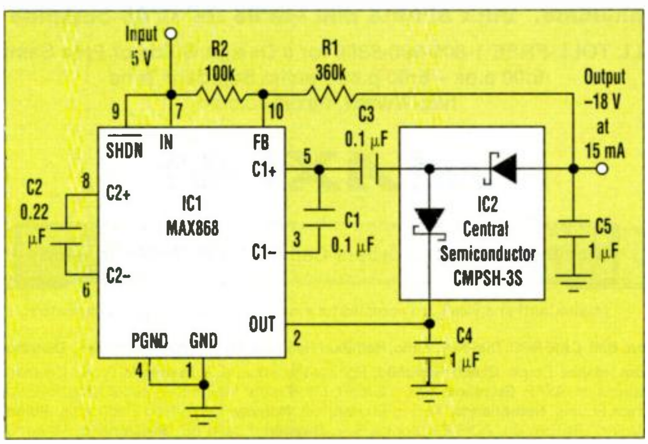
A stringent height limitation on pc boards employed in PDAs and palmtop computers requires using expensive, low-profile inductors in switchmode power supplies. As an alternative, however, you can replace certain switchmode circuits with one based on a charge pump *(see the figure)*. The example shown generates a regulated negative voltage suitable for biasing an LCD.

IC1 contains a regulated, inverting charge pump that produces output voltages as high as $-4\ V_{IN}$, in which the supply voltage V_{IN} can range from 1.8 V to 5.5 V. The IC regulates V_{OUT} via pulse-frequency modulation (PFM), with a maximum frequency of 450 kHz. The chip's low quiescent current (30 µA) provides excellent light-load efficiency without sacrificing full-load capability.

Inserting an external, discrete charge pump (consisting of C3, C4, and the Schottky diodes) in the feedback path of IC1 produces an "inverter-quadrupler" circuit. Its regulated output level is set by the ratio of feedback resistors R1 and R2:

$$V_{OUT} = -V_{IN}\ (R1/R2)$$

Configured as shown, the circuit provides up to 15 mA at V_{OUT} = −18 V, with 76% efficiency and 60 mV of output voltage ripple. Lower V_{OUT} allows higher output currents: V_{OUT} = −15 V yields 20 mA; while V_{OUT} = −12 V yields 30 mA.



Adding a few inexpensive components in the feedback path of IC1 enables the generation of regulated output voltages as high as −4 V_{IN}.

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MEETINGS

MAY

IEEE International Conference on Neural Networks (ICNN '98), May 3-9. Anchorage, Alaska. Contact Patrick K. Simpson, Scientific Fishery Systems Inc., P.O. Box 242065, Anchorage, Alaska 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@alaska.net.

IEEE World Congress on Computational Intelligence, May 3-9. William A. Egan Civic and Convention Center, Anchorage, Alaska. Contact Patrick K. Simpson, Scientific Fishery Systems Inc. Post Office Box 242064, Anchorage, Alaska 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@alaska.net.

Seventh IEEE International Fuzzy Systems Conference, May 3-9. Anchorage, Alaska. Contact Patrick K. Simpson, Scientific Fishery Systems Inc., Post Office Box 242065, Anchorage, Alaska 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@alaska.net.

IEEE International Symposium on Electronics & the Environment, May 4-6. Oak Brook, IL. Contact ISEE Conference Registrar, 445 Hoes Lane, Piscataway, NJ 08855-1331; (732) 562-3875; fax (732) 981-1203; e-mail: j.slaven@ieee.org.

IEEE/IAS Industrial & Commercial Power Systems Technical Conference (I&CPS), May 4-7. Edmonton, Alberta, Canada. Contact Marty Bince, Modicon Canada Ltd., 5803 86th St., Edmonton, Alberta T6E 2X4, Canada; (403) 468-6673; fax (403) 468-2925.

IEEE Radar Conference, May 12-14. Contact Scott Ramey, 2501 West University, MS 8056, McKinney, TX 75070; (972) 952-4409; fax (972) 952-3071; e-mail: sramey@ti.com.

IEEE International Conference on Acoustics, Speech & Signal Processing (ICASSP '98), May 12-15. Seattle Convention Center, Seattle, Washington. Contact Les E. Atlas, Dept. EE (FT 10), University of Washington, Seattle, Washington 98195; (206) 685-1315; fax (206) 543-3842; e-mail: atlas@ee.washington.edu.

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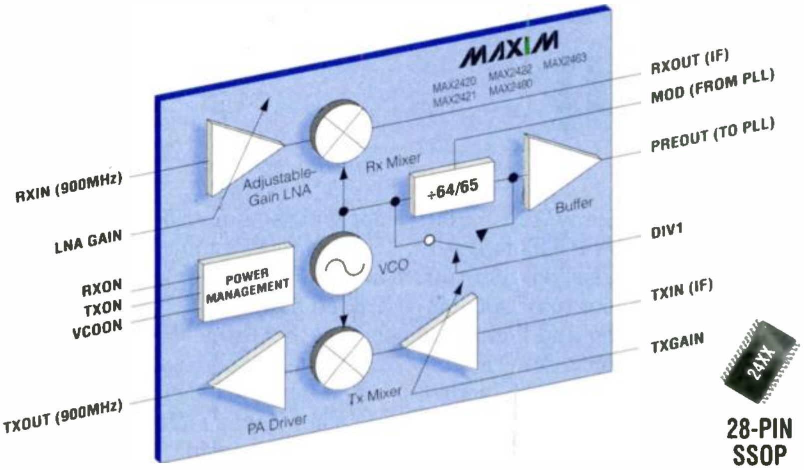

The MAX24xx family of image-reject RF transceivers perform a multitude of front-end functions in 900MHz radio transceivers, saving cost and space.

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MAX2421	46	✔	✔		High Side
MAX2422	70	✔	✔		High Side
MAX2424	10.7	✔		✔	High Side
MAX2426	70	✔		✔	High Side
MAX2440*	10.7	✔			High Side
MAX2441*	46	✔			High Side
MAX2442*	70	✔			High Side
MAX2460	10.7	✔	✔		Low Side
MAX2463	110	✔	✔		Low Side

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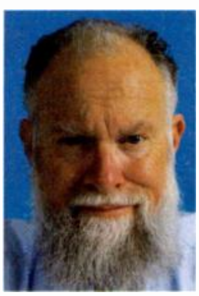
Circle No. 167 - For U.S. Response
Circle No. 168 - For International

BOB PEASE

What's All This International Business Travel Stuff, Anyhow? (Part II)

As I was saying in my Aug. 4, 1997 column "What's All This International Business Travel Stuff, Anyhow?" I was about to do some international traveling and lecturing. I'd be traveling to South America and Asia, giving a version of the lecture that I had given in more than a dozen places here in the States. And, I wanted to bring an extra set of foils (overhead transparencies) with subtitles translated into the appropriate foreign languages.

The Subtleties of Subtitles? Nobody thought that making up the subtitles was a terribly *bad* idea. But nobody thought it was a terribly *good* idea either. Folks had never seen them done before.



BOB PEASE OBTAINED A BSEE FROM MIT IN 1961 AND IS STAFF SCIENTIST AT NATIONAL SEMICONDUCTOR CORP., SANTA CLARA, CALIF.

Most people said, "If you just talk slowly, that will be OK, when you are talking about technical stuff." Of course, part of the problem is that I also talk about nontechnical stuff. But, often the foil on screen helps explain what I am talking about, with drawings, as well as words in the English language. And those words *may* or *may not* be helpful.

The final decision not to bring a set of subtitles was determined by the amount of help I would have needed to make up the subtitles. Also, there was the weight of the foils—the main set weighed over 5 lbs for 400 foils. Carrying two more sets in Spanish and in Portuguese would have overloaded my poor little briefcase. I just had better things to do, more important than making subtitles, and I ran out of time. So much for a good theory.

When I was lecturing in Brazil, I just told Rogerio, "If I talk too fast, take off your shoe and throw it at me, to remind me to slow down." But I guess I never did go too fast. I had a lot of fun in Brazil and Argentina. In retrospect, I feel badly that I never went out of my way to talk too fast, and force Rogerio to throw his shoe at me!

Gotta Think Fast! I put on some very good lectures in Argentina and Brazil. In Sao Paulo, we had well over 100 engineers at our big lecture. They all knew how to laugh in the right places! In Buenos Aires, the number of attendees was smaller because the university students had finals that week. It was not that we picked the wrong day; there was no day that week that would have been very good. But, the high quality of the audience made up for the moderate quantity. I got into a spirited conversation with one student who asked, "Mr. Pease, we students cannot breadboard everything. Yet, you tell us we should not trust Spice. What should we do, in reality?"

Good question! I paused and thought about it, and started to build my reply. "For your first or second round of study, there is no harm in using Spice. I prefer to use pencil and paper, but you can use Spice if you prefer. Then when you have a design that Spice says is OK, that would be a good time to build a breadboard, to confirm if and where Spice is telling you some truth. Suppose you have checked out the performance of the breadboard, *and* the Spice runs, to get reasonable results or acceptable agreement. Then, when you optimize the final schematic you may be able to easily modify your first breadboard to check out the final version. Does that sound reasonable?"

As we thought about this, I realized I had to tie up loose ends. I suggested, "What if you find a place where Spice does NOT tell the truth? You should document this, as a warning to other students and engineers. Write up a book of such discrepancies." Then I continued to expand these new solutions, "Make up that 'book' on a computer—maybe on intranet at your university—so all students can see it." He agreed this was a pretty good idea.

Maybe all students should keep such a book. Computers are getting pretty cheap these days for storing and disseminating information. That is NOT the same as saying that computers are cost-effective for circuit analysis. I learned a lot from these eager students.

Gotta Have FUN! In that Aug. 1997 column, I mentioned a very good travel book whose name I'd forgotten. The author, Frank Perkins, was kind enough to send me another copy: *Travel Adventures on the Company's Nickel*, ISBN 0-9648512-0-2. I'll recommend this as good reading, especially for people who travel a lot; it might give you some good ideas. If you mention that you read this in "Pease Porridge," you can order it for $12 from Oak Publishing, Dept. PP, 5225 Crane Rd., Melbourne, FL 32904.

After all, as I mentioned previously, there are times when you might plan to go home as soon as you have finished your overseas work. But if you take a day or two of well-deserved vacation before you come home, you'll be glad you did. I know a couple times I should have, and I regret not doing it. I'll be smarter next time. The cost-benefit ratio is too good not to. I mean, if I am finished with work on a Friday night, should I jump on the first plane home? Or should I spend the weekend in an amazing place, and get on a Sunday night flight? I know the answer to that.

Besides, sometimes staying an extra day or two can save your company a LOT of money on your flight. Ask

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your travel agent for advice and guidelines. I often stay over a Saturday night to save $300 or $500 or MORE. Air fares are *so* nonlinear these days!!

Make sure your tax and/or travel experts can tell you about traveling taxes. If you take N days of vacation after N+1 days of work, will you have to pay tax on that, because it's not a business trip? What is your company's policy? More importantly, what is the IRS' policy?

Lecture Time... After I returned home, I had to give a lecture at WESCON. My old friend Jack Leddy had asked me to lecture on a suitable topic about International Business for the IEEE. Of course, I talked about various items we have discussed previously, and much more. I showed them my best check-list for business travel, which is now posted on the web. Go to my web site at: *www.national.com/rap* and look for *LISTS*. Or you could go directly to: *www.national.com/rap/List/0,1150,35,00.html.*

At this lecture I gave out a *BUSHEL* of advice on international travel, such as:

•Be sure to reconfirm your flight. If you do not call the airline after you arrive in a foreign country, they may pretend they have no space for you to return, because you forgot to tell them you would want to go home.

•Be aware of different procedures for stowing your spare batteries, keys, metal, and penknife before you get to the X-ray inspection. In the U.S., putting them in your briefcase is usually OK. But for international travel, put your jack-knife and extra batteries in your *checked* baggage, otherwise, they may be confiscated. However, make sure you do have some good batteries in your camcorder or computer. Security guards often want you to demonstrate that they WORK.

•Inquire about the customer and his problems or complaints before you leave, so you don't walk into a buzzsaw. Insist that you be warned if there are any problems that have been making this customer unhappy. Maybe you can't solve them before you leave, but at least you'll be aware of them.

•Know how to reach colleagues in your home plant or office. Keep a good set of phone numbers, in case you have to call at an odd time to leave a message.

•Know how to run your e-mail, modem, or voice-mail from overseas. Have at least two phone charge cards.

•Also consider using a telex, a TWX (still in use in some parts of the world), or maybe a video-conference. You might even use the snail mail, international air mail, or an outfit such as DHL, FedEx, or UPS. Some of these are quite expensive, but they could STILL save you a lot of grief and money. In some cases, telephone calls make sense.

•Plan how to communicate before you leave. Know what your customer's expectations are. Nothing annoys me more than a customer who DEMANDS that we send an engineer to his plant, even before he explains the problem. When we get there, it turns out the problem is something we could have solved better and quicker from home.

•Be sure to get good advice on how to make phone calls at reasonable rates. When you are on the road, doing business long distance, you *still* have to be able to communicate. Maybe by modem. Maybe by telephone. You probably already know that hotels like to tack on surcharges of 50% to 200%. On a $30 phone call, that gets expensive really *fast*. The pay phone in the lobby is less likely to gouge you.

Eat, Drink, And... What else do you have to do, after you decide to travel? EAT, DRINK, and SURVIVE. (Not a trivial deal.) Find a place to stay. Ride and travel around. Negotiate. Communicate. Travel home. Communicate MORE. All the while, try to avoid making your hosts (or customers) unhappy. And, as I said before, LEARN.

What to drink? In my lecture, I mentioned that, when traveling overseas, you have to drink something, but be careful to not drink too much—unless it's pure water. Drink plenty of water on the plane. Keep well hydrated.

You should also bring iodine tablets or solution, so you can purify the local water. This can work much better than going thirsty, drinking the local water, or buying bottled water. The local water may be legally pure, but the local flora might not agree with your tummy. And, I wouldn't want to be alarmist, but some bottled water has been found to have enough bacteria to make your insides unhappy. Iodine can help avoid such problems.

Avoid ice cubes, unless you can make your own out of pure water. (But you can always brush your teeth using beer.) In Nepal, our hotel provided large urns of boiled water at each floor, so we could fill our canteens with safe water.

One time I went out for a walk with an engineer in a small South-American city. He offered me a treat—some sugar cane juice. The juice vendor fed the big pieces of raw (not TOO dusty) cane through a crusher. The juice ran out of the cane and all over the cane and down through the machine.

I thought about it. Would I dare to insult the customer by refusing to drink this sweet stuff? I decided to risk it, and sipped it down. Not bad. And, I never did get sick. But, if somebody offers you something from conditions that are slightly less than sanitary, you should have a good, *polite* excuse ready: "Oh, my tummy is feeling very wobbly today. Thanks, but, NO thank you."

What To Eat? While we were trekking in Nepal, we were very careful to eat only foods that were safe, on dishes that had been washed scrupulously clean and rinsed with chlorine water. But after the trip, I ate some of the local dhal-bhat (rice with lentils). Why not? The rice has been boiled and the lentils have been boiled; the only way you could get in trouble is if the dishes were not properly washed. But the lunch was very tasty, and I had no problems. Still, I preferred to drink my beer from the bottle, *not* from a glass.

I would never do this, and you shouldn't do it, either: Don't brag, "I like my chilis *REAL* hot!" You might discover that the local restaurants have chilis (or curries) hotter than anything you've ever met in your life! You sure would be embarrassed if you had to be hospitalized.

Remember, curries and chilis are measured, like earthquakes, on an open-ended scale. There is substantially *no limit* of how hot they may be. Or do you want to find out? Do *YOU* want to be a calibrator? *Several* peo-

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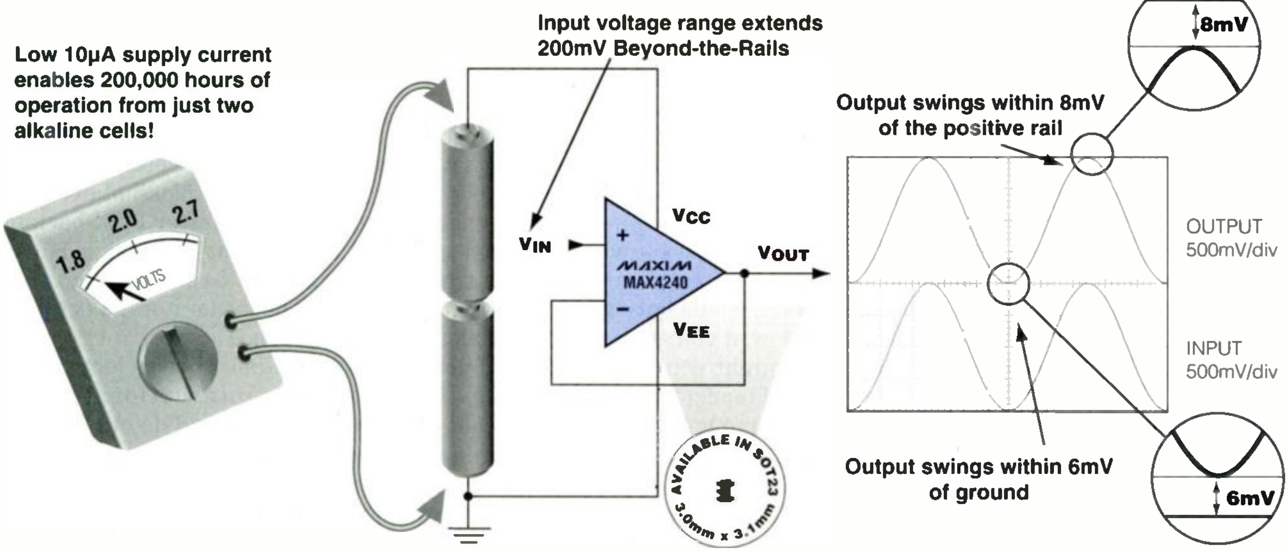

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MAX4241	1	90	+1.8 to +5.5	12	Yes	Yes	Yes	8-pin SO/µMAX
MAX4242	2	90	+1.8 to +5.5	12	—	Yes	Yes	8-pin SO/µMAX
MAX4243	2	90	+1.8 to +5.5	12	Yes	Yes	Yes	14-pin SO, 10-pin µMAX
MAX4244	4	90	+1.8 to +5.5	12	—	Yes	Yes	14-pin SO

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ple told me that this happened to one of their friends.

Where To Stay? Perhaps your company's local-office secretary or the customer's secretary can make reservations. Either way, be sure to keep good notes of your reservations and confirmation number. (Not to mention, car rental information.) On more than one occasion, I have moved from hotels that are too fancy and pricey, to digs that are less pretentious. Don't be too surprised if doing that makes you more comfortable—or puts you in a quieter neighborhood. The money saved is probably not as important.

Communicate At Home And Away... In my lecture, I expanded on the ways that even people who do NOT travel, have to be prepared to help and communicate with foreign customers. You never know who will be on the line when your phone rings—could be someone from Ghana, Germany, or Greece. Each business climate has its own customs. No matter if you're traveling or at home, you still have to be able to change gears quickly when that phone rings.

I recommend the great new book: *Kiss, Bow, or Shake Hands* by Morrison, Conaway, and Borden. It covers many areas such as cultural overviews, behavior styles, negotiating techniques, protocol, and business practices in 60 countries.

This book reminds me about many aspects of travel that make a lot of sense, if you happen to think of them. Here are some examples: Don't assume that customs or words that work in one area, work in another. Don't assume that all Spanish is "Spanish." The phrases that work in Spain are often DIFFERENT in Mexico, and even more different in Argentina, even though they all speak "Spanish." If any book purports to teach you "Spanish," a fair question is, "Yes, but WHOSE Spanish?"

The English language also is quite amazing in its variations between the U.S. and England—not to mention Australia or Scotland. Gestures that are OK in one part of the world are often NOT OK in other places. So if you want to avoid insulting your hosts or customers, a book such as this one is very important.

The book also has sections on how to negotiate in each country. I don't have to tell YOU how to negotiate deals—YOU already know that—but the book reminds us that strategies that work in one country, may be counter-productive in other countries.

The book runs about $20; ISBN 1-55850-444-3, published by Bob Adams.

Other Books... Other travel books that are very useful are those the *Lonely Planet* series. These can help you travel gracefully in a large number of areas. Any good bookstore can get you the book you want, but in a case like this, I like to look up what is available from Amazon Books at *www.amazon.com*. It may be easier to tell if you want what they have, on the computer, compared to the trouble you would have at a bookstore.

Now, if you are a starving student, you might want to get most of your travel books from a library. But the first time you waste an hour (not to mention *a day*) going somewhere recommended by an out-of-date travel book, you'll have wasted more than the cost of a new book, several times over. Students would hate to admit that. But if you are traveling on business, there is no excuse for wasting a lot of time because you're using out-of-date information. (Of course, even the *newest* book becomes obsolete fairly quickly. You must inquire locally to confirm that what you plan to do is really feasible. There might be a road out, or a boat service that's changed.)

Which Bookstore? Recently I wanted to buy a book on motorcycle safety. I went to a good little book store and asked them to search for it. They could not find it. When I got back to my computer, I searched for it at Amazon Books, and it turned up in 10 seconds flat. So, I ordered it from Amazon.

I do like to do business with real, local book stores. But, if a REAL bookstore is bleating because it is losing business to bookstores on the Internet, it has no leg to stand on when it cannot search for a book properly.

More Lectures... The same week as my WESCON lecture, I was flying to Nepal for our trek. Should I give a lecture there, before I came home? Our international marketing people said it would be a waste of time, because nobody in Nepal is buying many semiconductors. Well, I thought, all the more reason to explain what linear ICs are about. Not to mention the explanations of, "How to tell when your (digital) computer is lying—and what to do about it."

So I asked some colleagues at Lotus Energy in Kathmandu (they make rechargeable solar-powered systems of all sizes) to get out the publicity, and I hired a hall. We got 80 people to show up. Some were engineers, some were professors at the university. About one-third of the audience were students. Some were technicians or other professionals who work around electronics.

We had a very pleasant evening, on Dec. 5, the day after I got back from my trek, at the Mountain Hotel in Kathmandu. I remembered to talk slowly. The moderator did not have to throw his shoe at me.

Why didn't I give a lecture in India? The international experts thought we would do our best business there by selling microprocessors, for which "only a few lines of software would be required." So they would obviously not need any advice on analog systems or circuits. They decided there would be no point in my giving any lectures in India. Sigh...

On The Way Home... To be sure, it's good if you can write your trip report while you are on the flight home (or, even better, on the drive back from the customer's location), before you forget the important details. Will a 100-MHz Pentium laptop computer be helpful? Maybe, if you can type at faster than 10 MHz. Personally, I prefer a small, laptop word processor such the Alphasmart Pro, which weighs barely 2 lb, and on which you can type for 60 hours or 128 kbytes, whichever comes first. I bought one for about $290. The only thing wrong with it is that my wife borrowed it, and she really likes it. She hates to give it back. To find out more about the Alphasmart, call the company at (408) 252-9400, or look up *www.alphasmart.com*.

What happened to my old Tandy Model 102? I found that its usable memory of 25 kbytes is just too small to be practical for more than a short weekend trip. So, it's basically retired.

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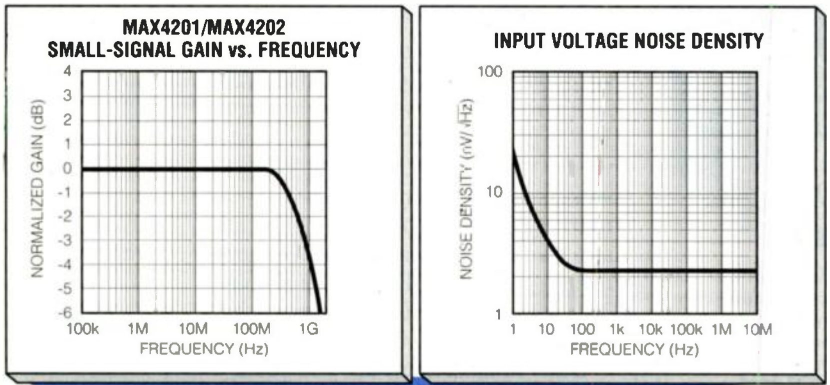

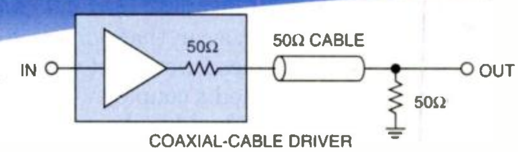

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MAX4201	1	50	780	280	2.2	4200	2.1	5 SOT23, 8 SO
MAX4202	1	75	780	280	2.2	4200	2.1	5 SOT23, 8 SO
MAX4203	2	—	530	130	2.2	4200	2.1	8 µMAX/SO
MAX4204	2	50	720	230	2.2	4200	2.1	8 µMAX/SO
MAX4205	2	75	720	230	2.2	4200	2.1	8 µMAX/SO

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Circle No. 169 - For U.S. Response
Circle No. 170 - For International

BOB PEASE

boards. Or a rock. Check that before you leave. (Adapters are available at Radio Shack and many travel stores.)

Make sure you have the correct adapters to run on 220 V. I almost bought a "universal" battery charger, until I read the fine print. It said that it only runs on 115 V! (My Sony battery charger will operate from 115 or 230 V, or anywhere in between.)

Jet Lag? Do you know how to beat jet lag? I like to just take a small nap, when I get tired (which would be the *wrong* time to go to bed for the night). Next, I need a GOOD LOUD alarm clock to wake me up from my nap. Then, I stay up to my ordinary bed-time, good and late. As a result, I wake up in the morning at a good time. This is like hitting a PLL with a big PULSE to force it into lock with a change of phase.

Travel Around... How are you going to get around? In some places you can rent a car, that *you* can drive. (Other places I would not want to.) As I mentioned a couple months ago, in Kathmandu, I hired a good car, with a good driver, for about $80 a day. Whereas a month earlier, I rented a car at JFK airport in N.Y., and even though I returned it where I got it, they soaked me $80. Of course, you could always rent a motorcycle... NO, I am NOT serious about that.

How Should I Pay? Know how to use your PLASTIC. I was not able to get cash out of money machines in Buenos Aires, but next year I bet I can get some at the airport. I used to have a four-digit password for my money card. Then, one day, my bank forced everybody to change to a five-digit number. But, in some overseas money machines, only four-digit passwords are accepted. When I complained to my bank about this, they permitted me to change back to a four-digit password. Many restaurants and businesses overseas now accept plastic, but not all. So check before you run up a big bill.

As one of my travel agents likes to point out, "Bring half as much clothing and twice as much money." But I was recently staying in a hotel that charged $11 to launder a shirt. Fortunately, I had enough shirts to last me to my next city, where laundry rates were much more reasonable. (In Kathmandu, the charge to launder a shirt was about $0.47.)

When You Have To GO! What's the difference between a hole in the floor, and a toilet? In some parts of the world, not much. To figure out how to attack this problem, consider *Going Abroad—The Bathroom Survival Guide* by Eva Newman. ISBN 0943-400929. About $13 from Magellan's, (800) 962-4943.

Highway Robbery? When somebody points out, "Sir, look, OH MY! There is mustard all over your coat!" what should you be thinking? You should be EXTREMELY careful because a gang of thieves is trying to distract you, and make off with your wallet or your camera. It's a well-known scheme. Somebody tried it on me, right across from the Sheraton in Buenos Aires.

They did NOT get my camera nor my camcorder nor my wallet. For more information, you might read *Foiling Pickpockets and Bag Snatchers and other Travel-Related Crimes/Scams.* Send a check for $3.95 to: Travel Companion Exchange, Pickpocket Reprint, Box 833, Amityville, NY 11701. I sent for this a few days ago, but haven't had a chance to read it yet. I wonder if they will include the story of the old Yankee sea captain who kept fish-hooks in his pocket to discomfit pickpockets?

Strange Customs? I'm putting this at the end, but YOU shouldn't do that: Make sure you understand what U.S. Customs says, *before* you leave. Don't buy something that may be illegal or is liable to be confiscated when you return. I hope these ideas will help you survive any overseas trips—and prosper in your international business, too!

All for now. / Comments invited!

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National Semiconductor
P.O. Box 58090
Santa Clara, CA 95052-8090

Circle 550 if you can't get e-mail, and want a copy of RAP's "Business Travel Checklist," by mail.

Circle 551 if you want a copy of RAP's "Maxi-Report" on trekking around Annapurna. (mail or e-mail)

Circle 552 if you might be interested in a VHS format videotape of RAP's 1997 lecture; 3.7 hours; $15.95.

Reader Feedback:

A Mailbag And Book Review

This month's column takes a look at the mail, plus a new edition of a popular op amp book. It's been a while since we've shared the mail with you in "Tools And Tips." In the interim, a variety of letters have crossed my desk, including some that focus on older columns.

E-mail Starter Kit (Feb. 3, 1997): This column had a carryover dialogue. Dave Bunin, of KBI Systems, had written to me last March with a special e-mail query. He sought an Internet-compatible e-mail system suitable for a small (<50 employees) company operating on a LAN. I didn't know of such a system, so I could only answer him in very general terms at the time.

More recently, Dave wrote back to tell me that he had indeed found a system which met his company's needs, namely a package called WIG (Workgroup Internet Gateway), from Sareen Software, P.O. Box 140029, Nashville, TN 37214; (615) 902-0000; or *www.sareen.com.*

This program allows users of a common workgroup to send/receive Internet e-mail via a Windows PC. One machine on the LAN requires an Internet connection, and it sends/receives messages to/from an ISP. WIG supports the widely used mail standards, such as the familiar SMTP and POP3 services, and both MIME and UUENCODE encoded attachments.

Also on e-mail, correspondents may have noted my use of new addresses, to segregate business and column mail. Past addresses are still valid, but *Walt_Jung@CSI.com* is preferred.

Analog's Shrinking World (April 1, 1997): In another carryover, consultant Wilton Helm wrote on surface-mount (SM) technology in analog designs.

Walt, glad to see your column in ELECTRONIC DESIGN. *I got your op-amp cookbook many years ago (20, I think), and learned to appreciate your practical sense of engineering.*

Since you asked twice now, I'll give a dissenting opinion on analog SM. I am a consultant doing hardware and software designs that range from control circuits through microwaves, often with embedded processors.

I disagree that SM is a bad thing for audio and analog in general. Sure it's a bit of a pain to prototype, and in some situations, harder to do thermal management in high-power situations. But, the high-frequency (HF) performance gains due to lowered parasitics makes it worth any pain.

For starters, op amps generally have wider, flatter response curves (same die) just because of less bond wire, lead frame inductance, and pin capacitance. That is even before putting them on a pc board. Add the wonders of 1206 resistors and capacitors, and it can make a real performance difference. And, general-purpose analog devices such as op amps now work in HF applications.


WALT JUNG

The first use of chip capacitors, resistors, and other SM devices was in RF devices, where parasitics couldn't be tolerated. Thankfully, miniaturization demands have now migrated these devices down, covering most solid-state parts.

As for prototyping pains, I learned many years ago not to breadboard or to wire wrap anything critical. Not only does prototype behavior differ so much from the finished product to be of minimal use, it's too expensive. I test what subcircuits I need, using prototype boards or pc-board material and a Dremel tool. Then, I build my first prototype on the computer using pc-board software, and have a few made. They may not be perfect—in fact, whole sections may need redoing—but the resulting cut and jumpered board mimics the finished product a lot more faithfully than any other prototype form I know.

As a bonus, I have a near-finished set of artwork on the computer awaiting final changes. The cost of making a few boards is about two days of engineering time, less than the cost of tacking something together or wire wrapping. CAD time is mostly recovered with the production artwork; with luck it is 90% done. Keep up the interesting columns.

Hi Wilton, thanks for your thoughts on the column. I'm glad that you find my *IC Op Amp Cookbook* practical.

I'm rather surprised that no one else has taken up my challenge regarding the analog merits of SM. But let's take your points on SM as part of a larger, overall analog design world picture.

Your perspective isn't really all that far from what I expressed in the Sept. 2, 1997 column, or the "good" side of SM active device performance. We both agree smaller packages are better here, and it has led to the use of relatively straightforward designs using op amps into the hundreds of MHz. This is something I'd never have thought possible 15 years ago.

But, if speed-related performance is all we want here, how about no package, like individual hybrid chips? This is the ultimate HF performance with multiple analog ICs. Perhaps you've been down that road as well. Even SOTs add parasitics vis-a-vis bare chips.

Unfortunately, analog isn't composed of just video and RF applications. There are still tons of lower-frequency applications that can be very demanding. But, with the current trends in packaging and IC developments, I don't necessarily see them continuing to be solved as well in the future—that is, as well as they are now using highly mature analog parts such as the OP07 series.

A trend accompanying SM packaging is lower system supplies, down to 3 V or less. This has already led to lowered maximum operating voltages, as smaller geometry and faster processes allow less $V_{S(MAX)}$ while producing the tiny parts you and others like. But suppose 10 years from now you need to handle a 120-dB dynamic range on a 3-V supply system. How hard do you think that would be, compared to today's world, using a ±15-V amplifier such as the AD797? Back to discretes? What size reduction?

The general point is that trends such as ever-descending size and supply voltage ultimately have a price. We are already quickly migrating to this point with 12-V or less devices. I don't know what performance we'll

WALT JUNG

have left when 1- to 2-V supplies are standard!

The passive SM RC components with low HF parasitics aren't always best for nonlinearities. Or, if you use high-quality NPO ceramic chip caps for lowest ac errors, you are limited to about 0.01 µF in electrical size. That's a serious constraint if you need a low THD+N 100-Hz LP filter!

The breadboard issue is a very tough nut to crack, and you've evolved your way with prototypes. Good! This likely came after learning what you could and couldn't do. The bottom line is that you have a degree of confidence entering a new design, and a time budget estimate.

But, this scenario is of little help to someone much-less experienced, as he or she lacks the broad-based, real-world experiences which help you to gauge things beforehand. A new engineer has been taught Spice simulation, which as you likely know, can be both good and bad. For larger mixed-signal systems, simulation can be impossible without device models. And no simulation will be 100% accurate without detailed model information on the board-level parts and interconnections.

This leaves the general picture regarding breadboarding pretty much as I had stated in the column. It is difficult, but can be helped some by manufacturers' evaluation boards. In the long run, they will always be insufficient for specific customer uses, so good breadboards are now more important than ever.

These are just a few thoughts to bounce back to you and the readers, to stimulate further thinking and response. Thanks for the interest and taking the time to write.

Computer Tech Support (Aug. 4, 1997, Revisit Nov. 3, 1997): These columns drew the greatest amount of mail, indeed too much for this article. Look for a special column on this hot-button topic next month.

Practical Circuits for Quiet Audio Transmissions (Nov. 17, 1997 Analog Special): A couple of readers wrote with queries on instrumentation amps in general, but without specific relevance to circuits in the article. James Davis, currently engineer for Duke University radio station WXDU, related his 1968 war story of installing common-mode isolation steps taken with setting up the same station. Transformer isolation was indeed a requisite to handle this case!

TIP: Although the Nov. 17 article didn't go into any depth on special design requirements for RFI prevention and cures, this point certainly is (or should be) a priority, for any audio or precision dc circuit operating within RF fields.

Franklin Miller, president of Sescom Inc., 2100 Ward Dr., Henderson, NV 89015-4249; (702) 565-3400; or *www.sescom.com* was helpful both before and during the course of preparing the article. His company's products are worth mention for all-around utility. Not only do they make a broad line of audio transformers, they also provide off-the-shelf and custom audio chassis. They also make various items useful in electronic prototyping and breadboarding, not just for audio, but also for wideband circuits. One example is the PSB series, various-sized assemblies of copper-clad pc boards and metal side rails. When completed, these fit into a clean, RF-tight box suitable for housing small circuits, etc.

Op Amp Books: Reader mail on the column's various book reviews has been generally positive. That said, I'll also admit that I can hardly resist any new book on op amps, particularly when a new revision of a useful prior edition appears. Sergio Franco's revised textbook on op amps is now out, and I've had a chance to look it over. It is *Design with Operational Amplifiers and Analog Integrated Circuits, Second Edition*, ISBN 0-07-021857-9, 668 pages with index, from McGraw-Hill. There also is a dedicated web site located at *www.mhhe.com/engcs/electrical/franco/*. Note that Amazon.com lists it at $92.50, *www.amazon.com.*

One could say that this new edition is much like the first, which it is. But it is more up-to-date and expanded in some key areas. It also has very good general coverage of op amps and other analog applications, such as active filters. As a bonus, there is extended coverage on other popular analog and mixed-signal ICs, such as timers, VCOs and function generators, V/Fs, DACs and ADCs, switching regulators, and PLLs.

A chapter heading summary of the book is as follows: 1. Operational Amplifier Fundamentals, 2. Circuits with Resistive Feedback, 3. Active Filters: Part I, 4. Active Filters: Part II, 5. Static Op Amp Limitations, 6. Dynamic Op Amp Limitations, 7. Noise, 8. Stability, 9. Nonlinear Circuits, 10. Signal Generators, 11. Voltage References and Regulators, 12. D-A and A-D Converters, 13. Nonlinear Amplifiers and Phase-Locked Loops

This book is used in the author's senior EE course at San Francisco State University, Calif., and it has 176 worked examples and 526 challenging end-of-chapter problems, in classic textbook style. The difference between this book and some other textbooks is that this one is more attuned to current design practices.

This current interest is evident in the treatment given throughout the text, such as the use of Spice simulations and graphics, to demonstrate various points. There also are updated sections on modern op-amp designs, for example, the use of current-feedback amplifiers, as well as the voltage-feedback type. The active-filter portion of this book comprises two complete chapters, and is a remarkably clear and lucid presentation. It also is expanded, and includes standard and more-advanced topology filter types. Among these are compensated state-variable filters, popular Sallen-Key filters, GICs and FDNRs, switched-capacitor types, and sensitivity analysis, etc., as well as some advanced analysis techniques in filter design (the use of Laplace synthesis in conjunction with PSpice).

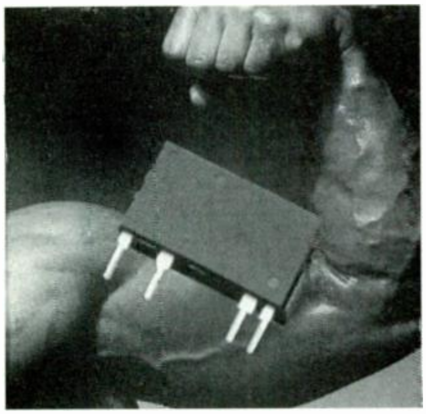
TIP: This new book is considerably improved over its previous edition, and could serve as a good general overview of op-amp and related analog theory for designers. While certainly not an applications manual, *Design with Operational Amplifiers and Analog Integrated Circuits*, strikes a balance between the purely theoretical and workable circuits, yet still retains the instructional guise of a textbook.

That's it for another column. Enjoy, and stay in touch.

Walt Jung is a corporate staff applications engineer for Analog Devices, Norwood, Mass. A longtime contributor to ELECTRONIC DESIGN, he can be reached via e-mail at: Walt_Jung@CSI.com.

High-Sensitivity PhotoMOS Relay Handles Up To 6 A

With an on-resistance of less than 500 mΩ, the AQZ264 and AQZ262 photo-MOS relays need as little as 3 mA to handle ac or dc loads from 400 V at 1 A, to 60 V at 6 A, respectively. Housed in



a four-pin, 1.693- by 0.354- by 1.260-in. package, the devices have a leakage current of 10 μA. Maximum input ratings include 50 mA (1-A peak) forward current, 3-V reverse voltage, and 75-mW power dissipation. The isolation voltage is 1500 V ac and the operating temperature range is –20° to 85°C. Pricing is $15 each per 1000; delivery is from stock to 12 weeks. PM

Aromat Corp., 629 Central Ave., New Providence, NJ 07974; Sales Dept., (800) AROMAT9; fax (908) 771-5658; www.aromat.com. **CIRCLE 463**

Hybrid, Solid-State Relays Target PCMCIA Modems

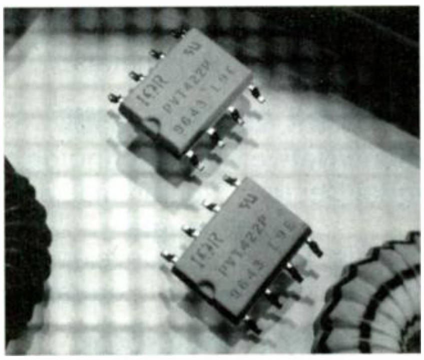
The PS7241-AT1 (dc input) and PS7241-AT5 (ac input) are solid-state-relay hybrids that combine both the relay and an optocoupler in a single 8-

pin SOP. The devices have an on-resistance of 30 Ω (max) and an isolation voltage of 1.5 kV. Other features include dial-pulse generation, on/off hook control, ring-signal detection, and loop-current sensing. The relays meet UL, CSA, and BSI standards, and can operate without degradation in performance up to 80°C. Pricing is $1.75 each per 1000. PM

California Eastern Labs, 4590 Patrick Henry Dr., P.O. Box 54964, Santa Clara, CA 95054-1817; (408) 988-3500; fax (408) 988-0279; www.cel.com.
CIRCLE 464

Microelectronic Relays Come In Thin, Surface-Mount Form

Measuring 2 mm high, the PVT422P Series microelectronic relay comes in a surface-mount package. The device has a maximum load-voltage-handling

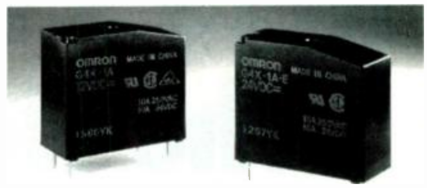


capability of ±400 V (dc or ac peak) and handles a maximum load current of 120-mA per channel, with an on-resistance of 35 Ω (max). The device requires 2-mA actuation current and has an input-to-output isolation level of 3750 V rms. Packaged in an 8-pin DIP, the relay is available in tape-and-reel form. Pricing is $2.23 each per 25,000; delivery is six to eight weeks. PM

International Rectifier, 100 N. Sepulveda Blvd., 8th. Floor, El Segundo, CA 90245; (310) 252-7105; fax on demand (310) 252-7100; www.irf.com.
CIRCLE 465

Low-Cost, Pc-Board Mount Relay Exhibits Versatility

The G4X is a pc-board mount relay for consumer and industrial applications. The UL-, CSA-, and VDE-approved device incorporates Class B coil insulation and is available in 10- and 16-A versions with flux protection or plastic sealing. Available coil voltages are 9, 12, 18, and 24 V. Pricing is $1.89 each per 1000; delivery is from stock.



Omron Electronics Inc., One East Commerce Dr., Schaumburg, IL 60173; (800) 55-OMRON; fax (847) 843-8081. **CIRCLE 466**

Quiet Relay Aims For Automobile-Cabin Applications

The FTR-P2 is a high-power automotive relay capable of handling up to 25-A continuous, or 35-A inrush. Featuring a 50-dB noise level and an internal H-bridge configuration, the relay measures 21 by 18 by 16.5 mm, and is available with 0.3-mm contact gaps. Contact materials comprise silver, tin oxide, and indium oxide. The coil-voltage ratings are 9, 10, and 12 V dc, and the coil power is 450 mW. The operating temperature range is –40° to 85°C. Pricing is $2 each per 1000; delivery time is 12 weeks. PM

Fujitsu Takamisawa America Inc., 250 E. Caribbean Dr., Sunnyvale, CA 94089; (800) 380-0059; fax (408) 745-4971; www.fujitsufta.com.
CIRCLE 467

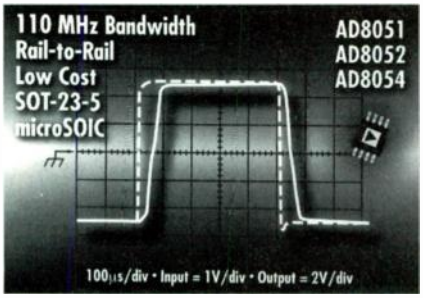
Rugged, Pushbutton Switches Handle Up To 8 A

Available with contact ratings of 4 A at 250 V ac, or 8 A at 125 V ac, the 1200 Series pushbutton switches come with solder lug, screw, or screw-with-clamp terminals. The devices include a robust, 12-mm threaded bushing that mounts in a panel hole slightly larger than 0.5 in. The switch body measures 0.551 by 0.669 by 0.472 in. Options include actuator style and finish. The switches have a contact resistance of 10 mΩ (max), an insulation resistance of 1000 MΩ, a dielectric strength of 2000 V rms, and an operating temperature range of –20° to 55°C. Pricing for a normally open version, the 1213A2UU, is $1.89 each per 1000. PM

APEM Components Inc., 134 Water St., P.O. Box 544, Wakefield, MA 01880-4444; Mel Hallah (781) 246-1007; fax (781) 245-4531; www.apem.com. **CIRCLE 468**

Rail-To-Rail Amp Combines High Speed And Low Cost

A new family of rail-to-rail op amps from Analog Devices doesn't force designers to trade off between speed and price. The AD8051/52/54 op-amp family is particularly well suited for applications requiring low supply voltage and rail-to-rail output, such as CCD imaging, DVD, or buffering ADCs. The family operates with +3- to +12-V single supplies, and may also be used with ±5-V dual supplies. Typical performance is 0.2 to 4 V on a +5-V supply, bandwidth of 110 MHz or more, and slew rate of 140 V/µs.



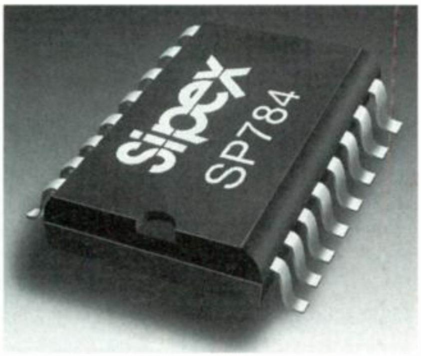
The single amplifier is offered in an SOT 23-5 or standard SOIC package; the dual version comes in a microSOIC or SOIC package; and the quad amplifier is available in a 14-lead SOIC or TSSOP. In 10,000-piece quantities, the AD8051, AD8052, and AD8054 amplifiers cost $0.79, $1.47, and $2.62, respectively. LM

***Analog Devices Inc.**, Ray Stata Technology Center, 804 Woburn St., Wilmington, MA 01887; (617) 937-1428; Internet: www.analog.com.*
CIRCLE 469

DC-DC Converters Offer Three Modes Of Operation

Two new dc-dc converters from Sipex Corp. offer three selectable modes of operation. The SP782 and SP784 converters are based on the company's patented charge-pump design. Both parts can operate either as a voltage doubler and inverter, a voltage inverter, or be put in low-power shutdown mode. The converters' programmable features let users supply voltages that are suitable for RS-232 (±10 V) and RS-423 (±5 V) drivers. Battery-powered applications benefit from on-chip power-management circuitry and the low-power shutdown mode that consumes less than 60 µA of supply current.

Both converters are fabricated in low-power biCMOS technology. The devices are offered in either a 16-pin plastic DIP or a 16-pin SOIC package. Pricing for the SP782 and SP784 is set at $1.50 and $2.00 in 1000-piece quantities. Delivery is from stock to six weeks. LM



***Sipex Corp.**, 22 Linnell Circle, Billerica, MA 01821; (978) 667-8700; www.sipex.com.*
CIRCLE 470

High-Speed FET Driver Has Four High-Current Outputs

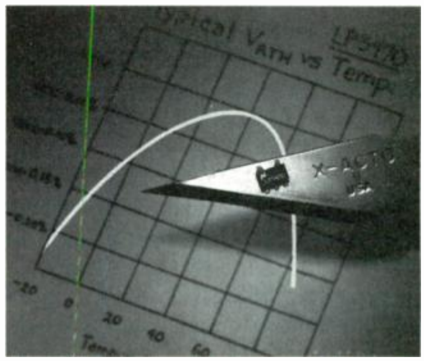
Unitrode's UCC3776 is a high-speed, high-current quad-output driver IC intended to drive the gates of power MOSFETs in various switch-mode power-supply, motor-drive, and power-management applications. The outputs can be paralleled, making the part a dual 3-A driver for two-switch applications. In secondary-side applications, the drivers can be incorporated into synchronous switching converters.

Switching losses are minimized because each of the four outputs can deliver 1.5 A of peak gate drive current for rapid turn-on, and will sink 2 A for improved turn-off. Features include undervoltage lockout, an enable function, and polarity selection for choosing inverting or noninverting input-to-output commands. The UCC3776 comes in a 16-pin DIL or 28-pin PLCC package. Pricing is set at $2.85 each in !000-piece quantities. Delivery for production quantities is 12-14 weeks. LM

***Unitrode Corp.**, 7 Continental Blvd., Merrimack, NH 03054; (603) 424-2410; www.unitrode.com.*
CIRCLE 471

POR Voltage Monitor Guarantees ±1% Accuracy

The LP3470 power-on-reset (POR) voltage monitor features a guaranteed accuracy of ±1% over –20 to +85°C. Guaranteed reset is valid down to V_{CC} = 0.5 V. The micropower LP3470 voltage monitor comes housed in a SOT23-5 package, and is designed to generate a reset output whenever the voltage supply falls below preset specifications. Flexibility is provided with an adjustable reset time-out period.



Designers can choose from among six standard reset threshold voltages: 2.63, 2.93, 3.08, 4.00, 4.38, and 4.63 V. In addition, E^2PROM technology enables the part to be programmed for more than 50 different threshold voltages between 2.4 and 5.0 V. These threshold voltages come in 50-mV increments. The LP3470M5 is available now in production quantities. Pricing for the monitor is set at $0.70 each in 1000-unit lots. LM

***National Semiconductor Corp.**, 2900 Semiconductor Dr., Santa Clara, CA 95052-8090; (408) 721-5000; www.national.com/pf/LP/LP3470.html.*
CIRCLE 472

Compact Pressure Transducer Can Withstand An Explosion

The Series 420X pressure transducers and transmitters are now available in compact, stainless-steel NEMA 4X, 7, 9 explosion-proof housings suitable for use in Class I, Division I Groups A, B, C, and D hazardous locations. All parts

come with the standard 1/4-14 NPT male pressure connection.

Three models are currently offered: Series 423X is a 5-V transducer, Series 426X is a 10-V transducer, and Series 425X is a 20-mA transmitter. All models are available for process pressure ranges from 0-15 psia to 0-10,000 psig. Accuracy is rated ±0.25% full scale, including linearity, hysteresis, and repeatability. Stability is rated at ±0.5% of full-scale output. The parts are designed to withstand up to 50 g of shock and 15 g of vibration as designated in MIL-STD-202. Call for pricing and availability. LM

***Barksdale Inc.**, 3211 Fruitland Ave., Los Angeles, CA 90058; (800) 835-1060 or (213) 589-6181.* **CIRCLE 473**

Pressure Transducer Family Offers A Variety Of Options

A wide variety of options makes the DeltaPlus family of differential pressure transducers suitable for many applications. The product line offers a set of standard configurations and a range of options so that designers can meet their exact specifications. Designers also can choose from various pressure parts, electrical terminations, signal outputs, and mechanical configurations.

DeltaPlus transducers feature accuracies of ±1% or ±0.25%, and a full-scale range as low as 10 inches of water over an operating temperature from –40° to 225°F. Standard output is 0-100 mV, or you can choose from internally amplified voltage and current outputs. The welded, stainless-steel units can be configured for wet/wet or wet/dry applications, and with in-line or right-angled pressure ports. The

DeltaPlus differential pressure transducer family is shipping now. Prices start at $600. LM

***Sensotec Inc.**, 2080 Arlingate Ln., Columbus, OH 43228; (800) 848-6564.* **CIRCLE 474**

Linear Hall-Effect Sensor Is User-Programmable

Users can program the offset, temperature coefficient, and sensitivity of the MLX90215VA linear Hall-effect sensor. The device provides instrumentation performance in a single CMOS IC. Applications include linear-position, angular-position, and current sensing.

With the MLX90215VA, users are able to trim the offset in a complete system to an initial error of ±0.01%, and ±0.4% over the automotive temperature range of –40° to +150°C. Because most other system components have a temperature dependence, the sensor includes a programmable temperature coefficient. The automotive-temperature-range MLX90215VA costs $3.00 in 10,000-piece quantities. A lower-temperature version is available for less money. Samples also are available through the company's sales department. LM

***USMikroChips**, 15 Sutton Rd., Box 837; Webster, MA 01570-0837; (508) 943-9430; www.usmikro.com; e-mail: usmikro@aol.com.* **CIRCLE 475**

Temperature Switch Combines Accuracy And Noise Protection

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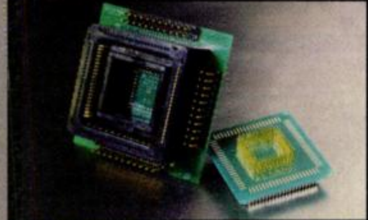

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April 20	3/10/98
May 1	3/21/98
May 13	4/2/98
May 25	4/14/98
June 8	4/28/98
June 22	5/12/98
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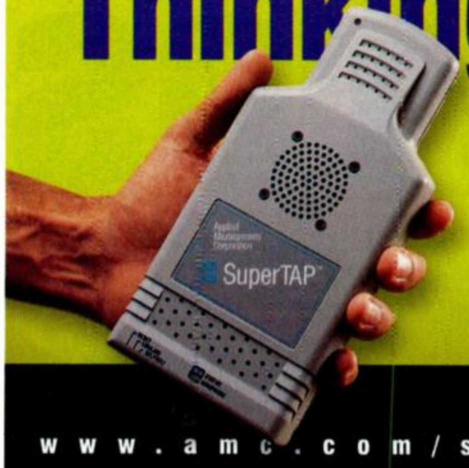

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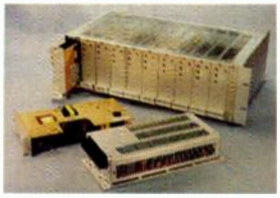

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