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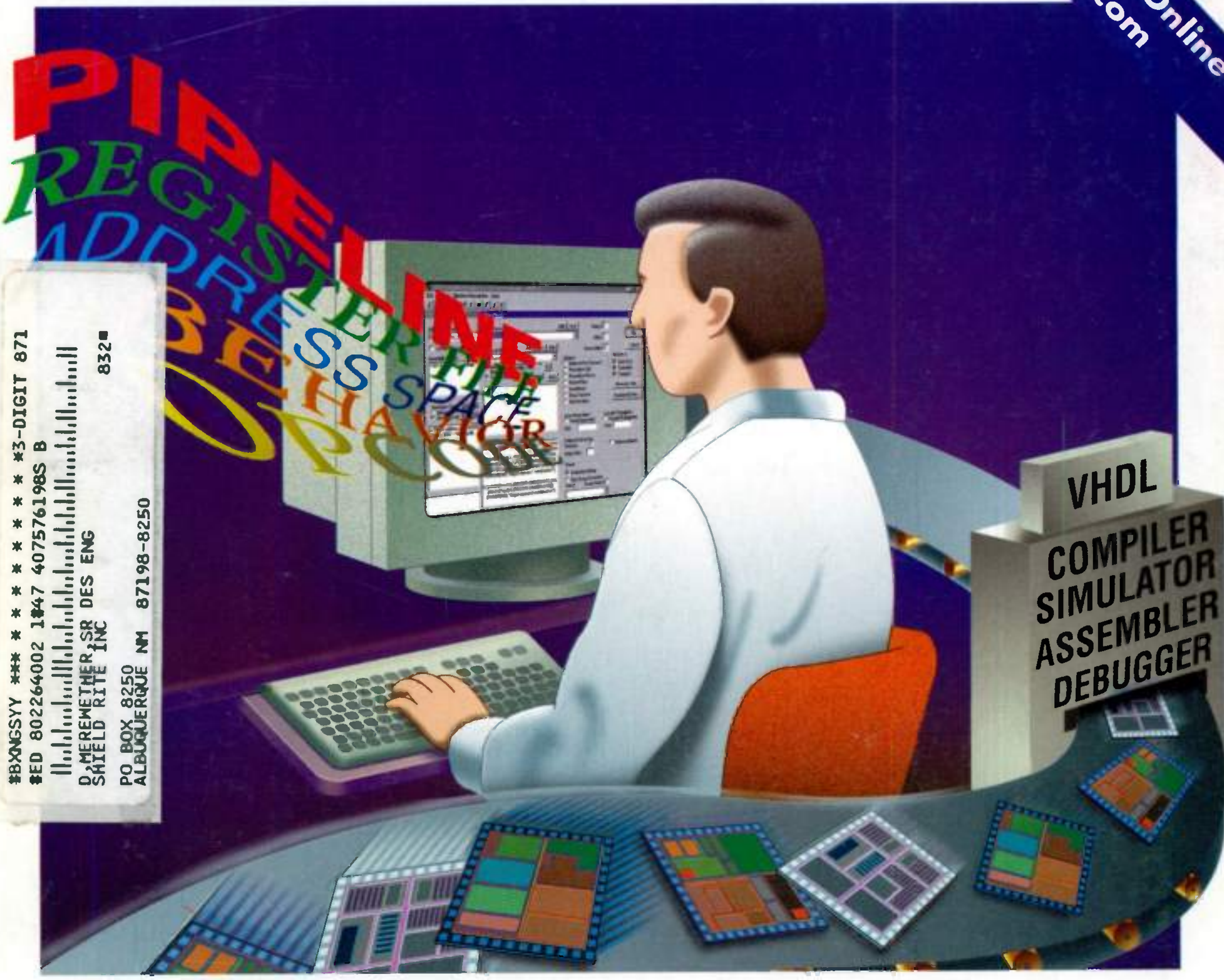
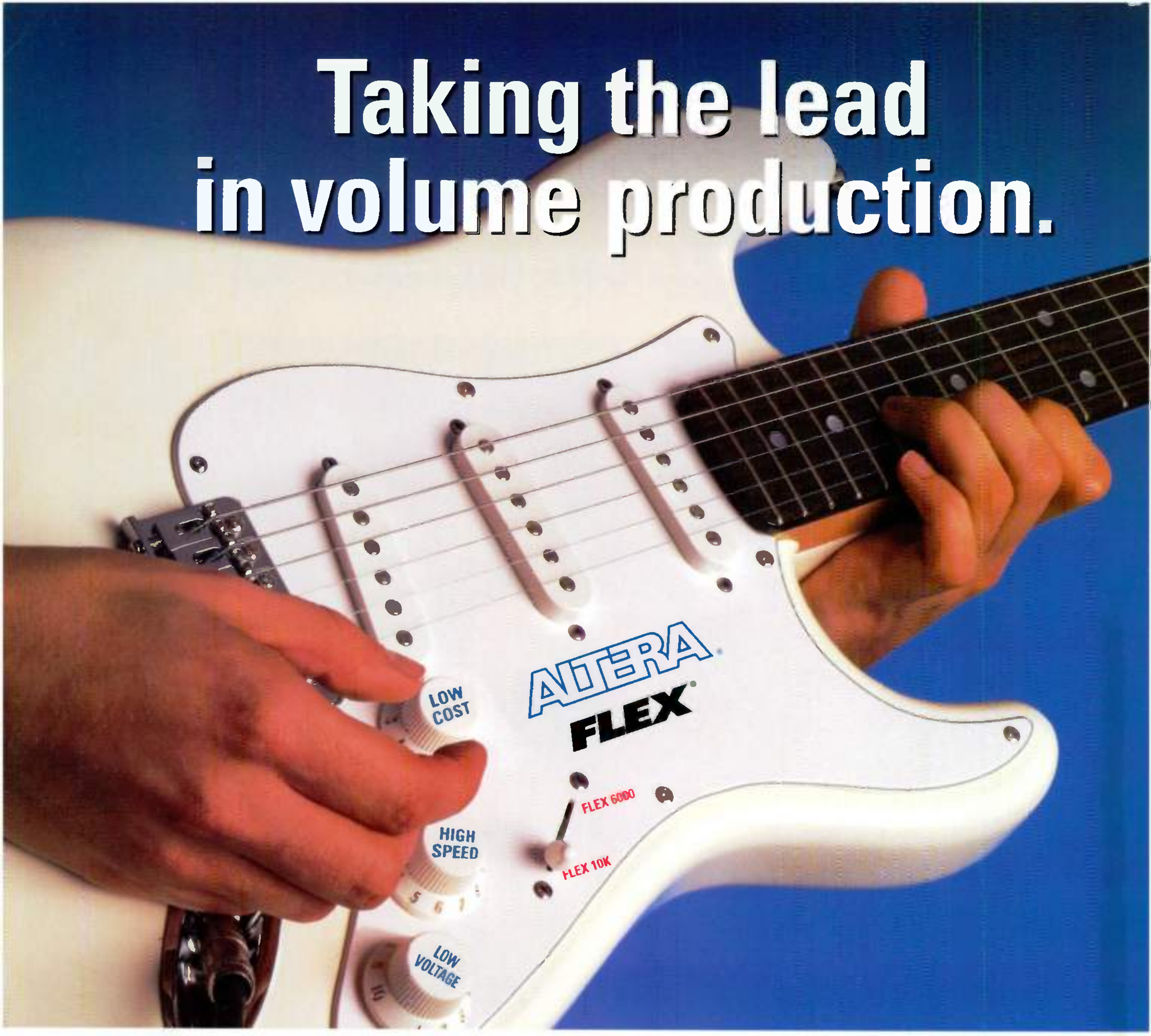


Processor Architecture Tools Grow From One Source p. 44

Taking the lead in volume production.



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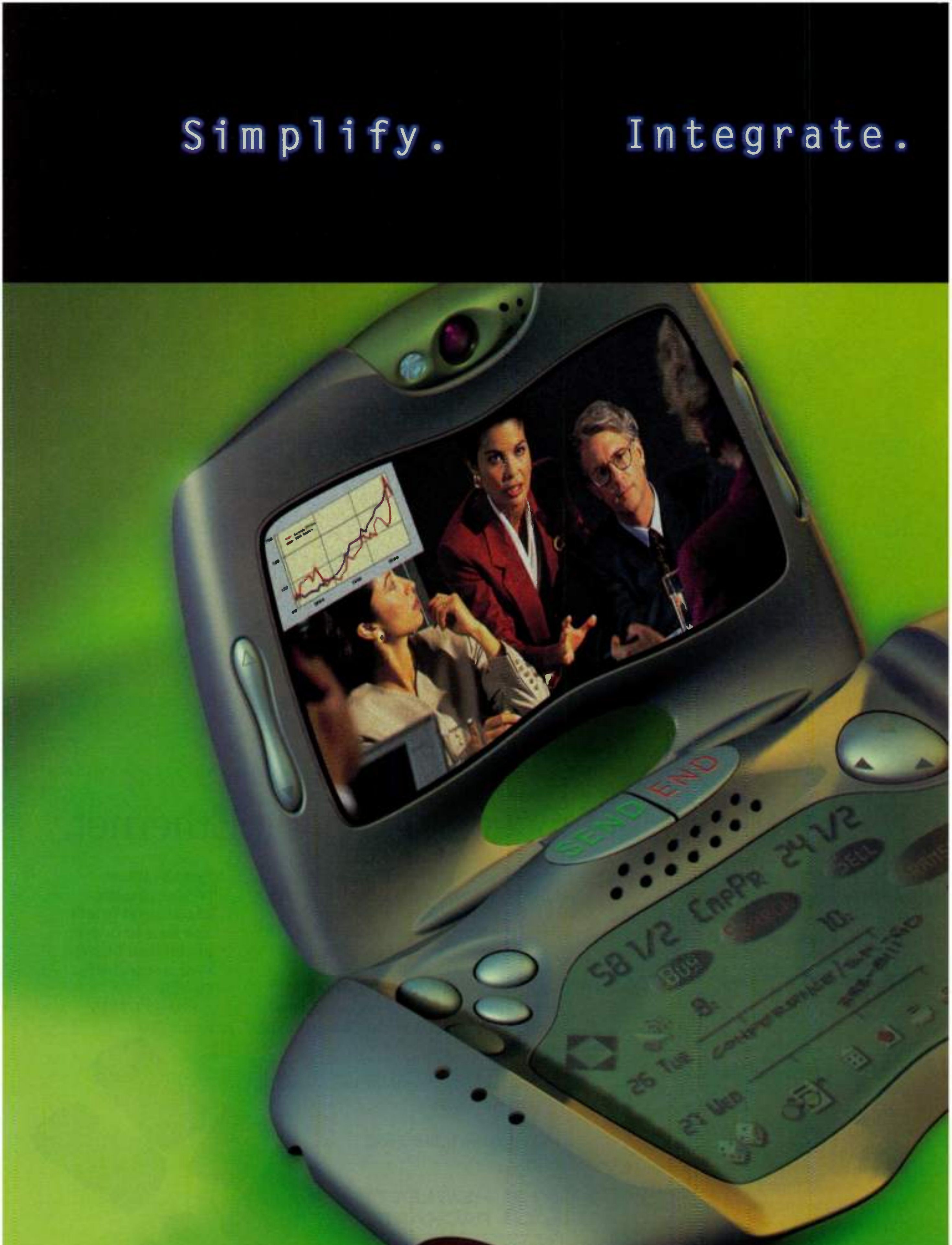
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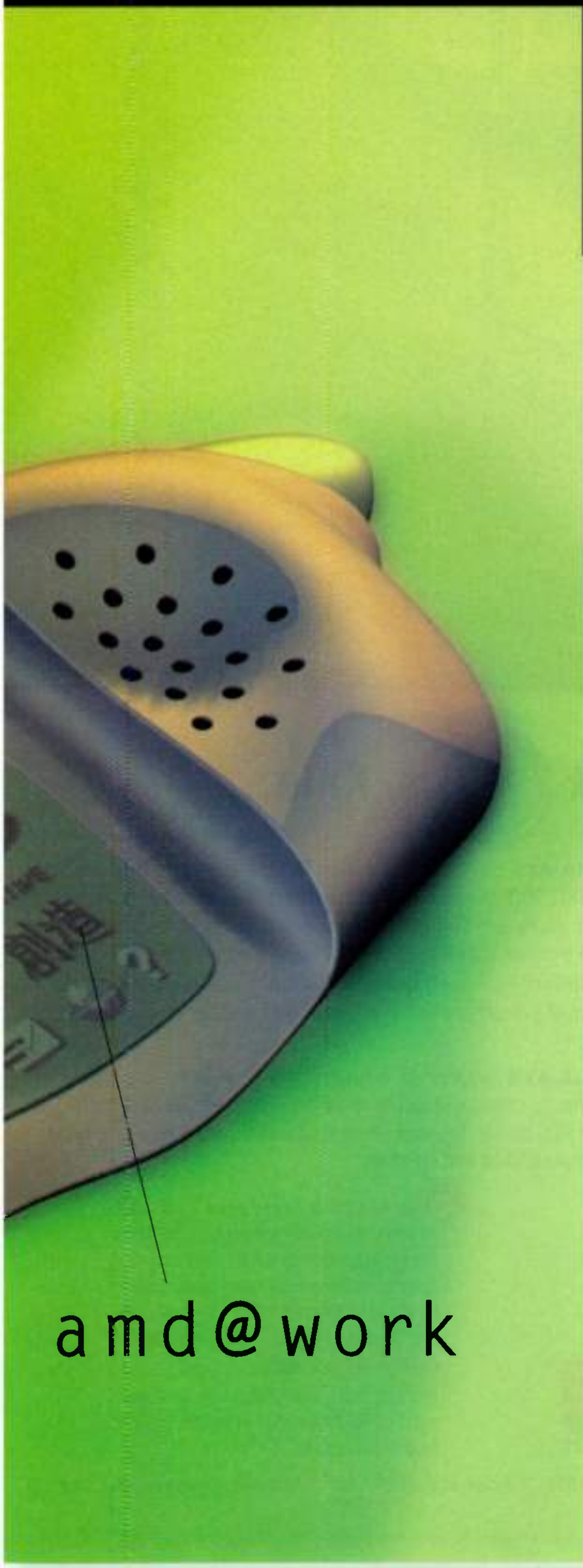

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ELECTRONIC DESIGN

March 23, 1998 Volume 46, Number 7

EDITORIAL OVERVIEW

ELECTRONIC DESIGN (ISSN 0013-4872) is published twice monthly except for four issues in May, three issues in February, three issues in August, three issues in October, and three issues in November by Penton Publishing Inc., 1100 Superior Ave., Cleveland, OH 44114-2543. Paid rates for a one year subscription are as follows: $100 U.S., $170 Canada, $180, $200 International. Second-class postage paid at Cleveland, OH, and additional mailing offices. Editorial and advertising addresses: ELECTRONIC DESIGN, 611 Route #46 West, Hasbrouck Heights, NJ 07604. Telephone (201) 393-6060. Facsimile (201) 393-0204. Printed in U.S.A. Title registered in U.S. Patent Office.

ELECTRONIC DESIGN

March 23, 1998 Volume 46, Number 7

EDITORIAL OVERVIEW

BOARDS & BUSES

QUICKLOOK

COVER ILLUSTRATION BY:
BRUCE JABLONSKI

Jesse H. Neal Editorial Achievement

1967 First Place Award	1978 Certificate of Merit
1968 First Place Award	1980 Certificate of Merit
1972 Certificate of Merit	1986 First Place Award
1975 Two Certificates of Merit	1989 Certificate of Merit
1976 Certificate of Merit	1992 Certificate of Merit

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China Telecom 2000 Conference, Apr. 7-8. Holiday Inn Capitol, Washington, D.C. Contact Information Gatekeepers, (800) 323-1088; (617) 232-3111; fax (617) 734-8562; e-mail: igiboston@aol.com; www.igigroup.com.

20th IEEE International Conference on Software Engineering, Apr. 19-25. Kyoto International Conference Hall, Kyoto, Japan. Contact Koji Torii, Graduate School of Information Sciences, Nara Institute of Science & Technology, 8916-5 Takayama-cho, Ikoma-shi, Nara-ken 630-01, Japan; +81 7437-2-5310; fax +81 7437-2-5319; e-mail: torii@is.aist-nara.ac.jp.

DSP World Spring Design Conference, April. 21-23. Santa Clara Convention Center, Santa Clara, California. Contact Liz Austin, Miller Freeman Inc. (888) 239-5563, (415) 538-3848; e-mail: dspworld@mfi.com; www.dspworld.com.

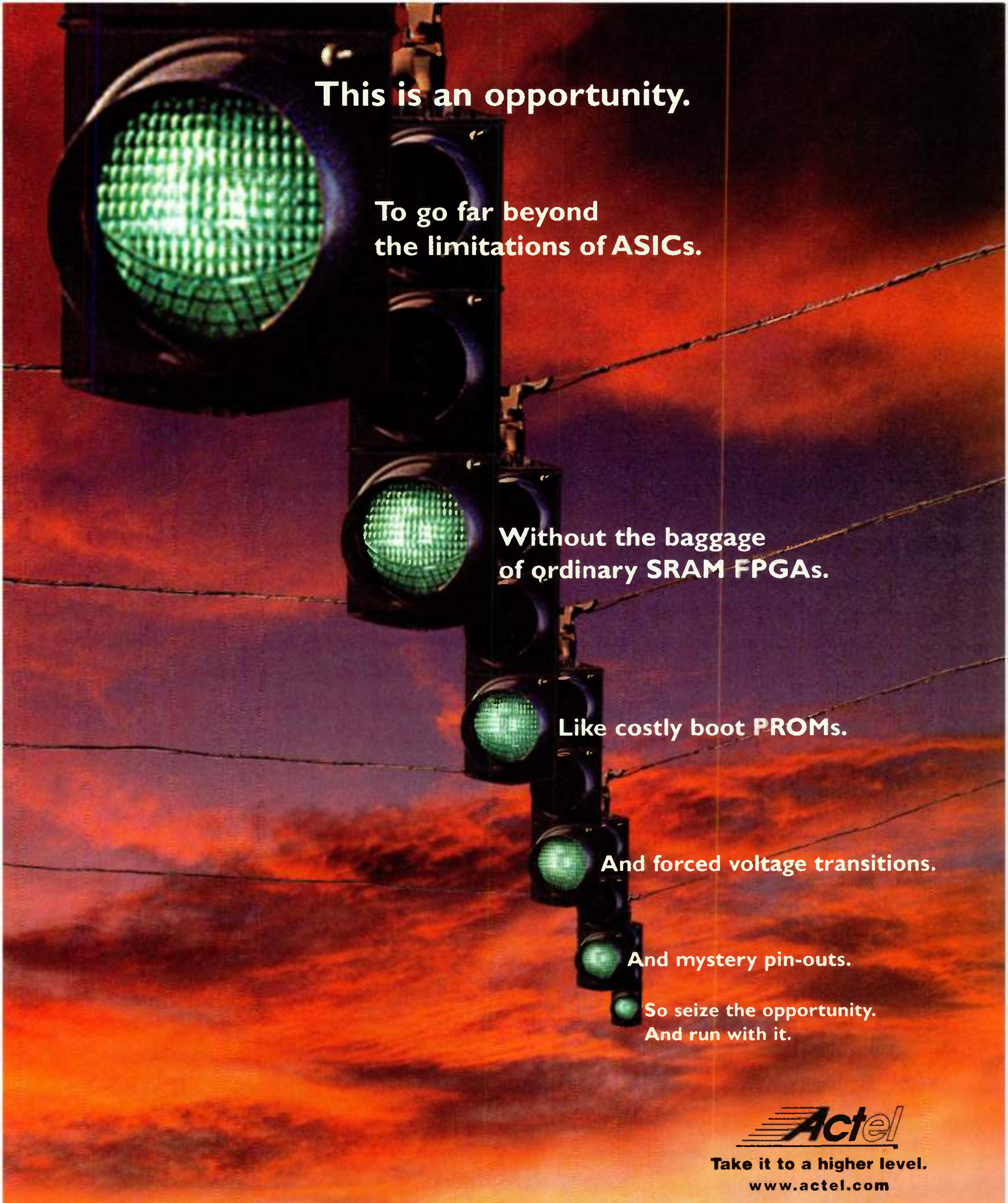
Southeastcon '98, April 24-26. Hyatt Regency, Orlando International Airport, Orlando, Florida. Contact Parveen Ward, ECE Dept., University of Central Florida, Orlando, Florida 32816; (407) 823-2610; fax (407) 823-5835; e-mail: pfw@ece.engr.ucf.edu.

16th IEEE VLSI Test Symposium, Apr. 26-30. Hyatt Regency Monterey, Monterey, CA. Contact Rob Roy, Intel Corp., MS:JFT-102, 5300 Elam Young Pkwy., Hillsboro, OR 97124-6497; (503) 264-3738; fax (503) 264-9359; e-mail: robroy@ichips.intel.com.

IPC Printed Circuits Expo '98, Apr. 26-30. Long Beach Convention Center, Long Beach, CA. Contact Dan Green, The Institute for Interconnection & Packaging Electronic Circuits, 2215 Sanders Rd., Northbrook, IL 60062-6135; (847) 509-9700 ext. 371; fax (847) 509-9798.

MAY

100th ACerS Annual Meeting & Exposition, May 3-6. Dr. Albert B. Sabin Convention Center, Cincinnati, Ohio. Contact The American Ceramic Society Customer Service Department; (614) 794-5890; fax (614) 899-6109; e-mail: customersrvc@acers.org; www.acers.org.



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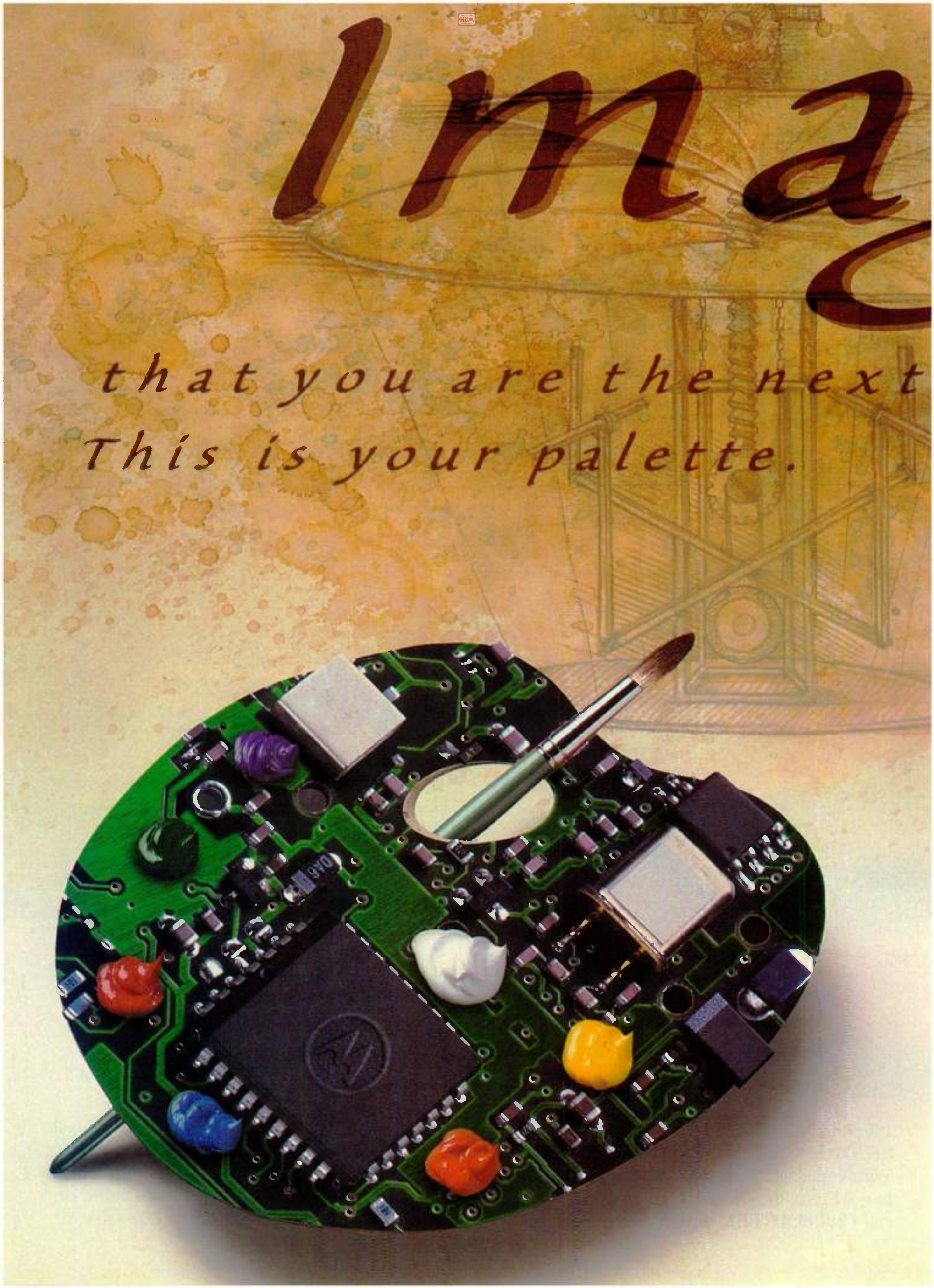
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Conference on Lasers & Electo-Optics & The International Electronics Conference (CLEO/IEC), May 3-8. The Moscone Center, San Francisco, CA. Contact Amy Hutto, OSA Conference Services, 2010 Massachusetts Ave. N.W., Washington, DC 20036-1023; (202) 416-1980; fax (202) 416-6100; e-mail: cleo.info@osa.org.

IEEE International Conference on Evolutionary Computation, May 3-9. Ankorage, Alaska. Contact Patrick K. Simpson, Scientific Fishery Systems Inc., Post Office Box 242065, Anchorage, Alaska 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@alaska.net.

IEEE International Conference on Neural Networks (ICNN '98), May 3-9. Anchorage, Alaska. Contact Patrick K. Simpson, Scientific Fishery Systems Inc., Post Office Box 242065, Anchorage, Alaska 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@alaska.net.

IEEE World Congress on Computational Intelligence, May 3-9. William A. Egan Civic and Convention Center, Anchorage, AK. Contact Patrick K. Simpson, Scientific Fishery Systems Inc. P.O. Box 242064, Anchorage, AK 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@alaska.net.

Seventh IEEE International Fuzzy Systems Conference, May 3-9. Anchorage, Alaska. Contact Patrick K. Simpson, Scientific Fishery Systems Inc., Post Office Box 242065, Anchorage, Alaska 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@alaska.net.

IEEE International Symposium on Electronics & the Environment, May 4-6. Oak Brook, Illinois. Contact ISEE Conference Registrar, 445 Hoes Lane, Piscataway, New Jersey 08855-1331; (732) 562-3875; fax (732) 981-1203; e-mail: j.slaven@ieee.org.

IEEE/IAS Industrial & Commercial Power Systems Technical Conference (I&CPS), May 4-7. Edmonton, Alberta, Canada. Contact Marty Bince, Modicon Canada Ltd., 5803 86th St., Edmonton, Alberta T6E 2X4, Canada; (403) 468-6673; fax (403) 468-2925.

Custom Integrated Circuits Conference (CICC), May 11-14. Westin Hotel Convention Center, Santa Clara, California. Contact CICC, 101 Lakeforest Blvd., Suite 270, Gaithersburg, MD 20877; (301) 527-0902; fax (301) 527-0994.

IEEE Radar Conference, May 12-14. Contact Scott Ramey, 2501 West University, MS 8056, McKinney, TX 75070; (972) 952-4409; fax (972) 952-3071; e-mail: sramey@ti.com.

IEEE International Conference on Acoustics, Speech & Signal Processing (ICASSP '98), May 12-15. Seattle Convention Center, Seattle, WA. Contact Les E. Atlas, Dept. EE (FT 10), University of Washington, Seattle, WA 98195; (206) 685-1315; fax (206) 543-3842; e-mail: atlas@ee.washington.edu.

IEEE International Conference on Robotics and Automation, May 16-21. Katholieki Universiteit, Leuven, Belgium. Contact Georges Giralt, LAAS-CNRS, Toulouse, France, +33 61-33-63-48; fax +33 61-33-64-55; e-mail: giralt@laas.fr.

IEEE Power Electronics, Specialist Conference (PESC '98), May 17-22. Sea Hawk Hotel & Resort, Fukuoka, Japan. Contact Tsutomu Ogata, NTT Integrated Information & Energy Systems Labs., Midori-cho, Musashino, 180 Japan; +81 422-59-2350; fax +81 422-59-2347; e-mail: ogata@ilab.ntt.jp

IEEE Vehicular Technology Conference (VTC), May 18-21. Westin Hotel, Ottawa, Ontario, Canada. Contact Tara Hennessy, Industry Canada, 300 Slater St., Ottawa, Ontario, K1A OC8, Canada; (613) 990-4711; fax (613) 952-5108; e-mail: hennessytara@ic.gc.ca.

Fourth PC Developers' Expo & Conference, May 18-22. San Jose Convention Center, San Jose, CA. Contact Anna Brooks (800) 690-3858 or (619) 673-0870; fax (619) 673-1591; www.annabooks.com., e-mail: expo@annabooks.com.

48th IEEE Electronic Components & Technology Conference (ECTC '98), May 25-28. Sheraton Hotel & Towers, Seattle, WA. Contact Components Group, EIA, 2500 Wilson Blvd., Arlington, VA 22201; (703) 907-7536; fax (703) 907-7501; e-mail: judya@eia.org.

IEEE International Symposium on Circuits & Systems (ISCAS '98), May 31-June 03. Monterey Conference Center,Monterey, California. Contact Sherif Michael, Department of Electrical & Computer Engineering, Naval Postgraduate School, Monterey, California 93943; (408) 656-2252; fax (408) 656-2760; e-mail: michael@ece.nps.navy.mil.

JUNE

POF World '98 (Plastic Optical Fiber), June 1-4. Providence Convention Center, Providence, Rhode Island. Contact Information Gatekeepers Inc., 214 Harvard Ave., Boston, Massachusetts 02134; (617) 232-3111; fax (617) 734-8562; www.igigroup.com.

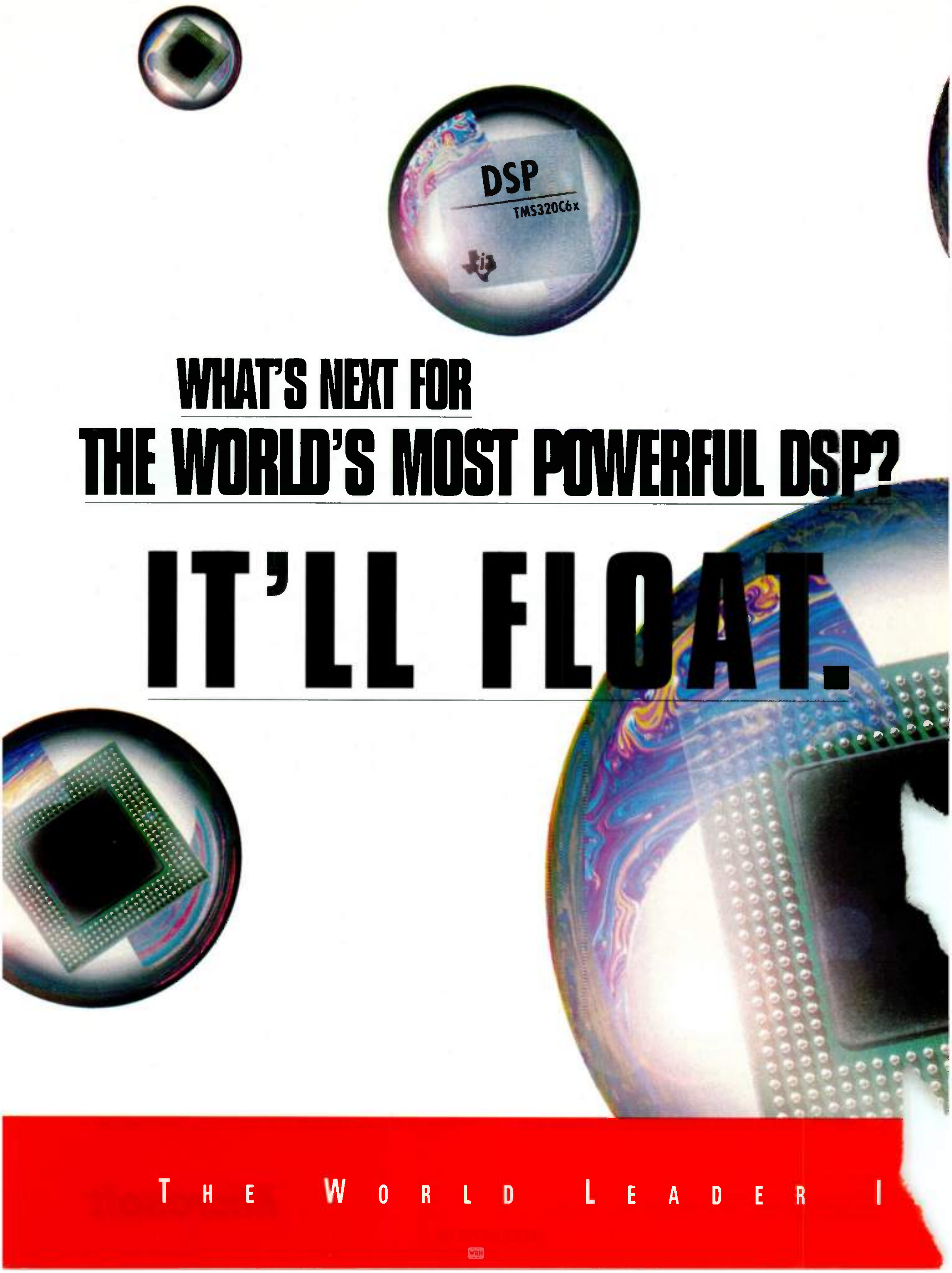
International Conference on Consumer Electronics (ICCE), June 2-4. Los Angeles Airport Marriott, Los Angeles, Califonria. Contact Diane Williams, Conference Coordinator, 67 Raspberry Patch Dr., Rochester, NY 14612-2868; (716) 392-3862; fax (716) 392-4397, e-mail: d.williams@ieee. org; www.icce.org.

IEEE International Conference on Communications (ICC '98), June 7-11. Atlanta,Georgia. Contact Debra Jordon, general secretary; fax (404) 881-6057; e-mail: icc98@comsoc.org. www.comsoc.org/confs/icc/98.

IEEE/MTT-S International Microwave Symposium (MTT 98), June 7-12. Baltimore Convention Center, Baltimore, Maryland. Contact Steven Stitzer, Westinghouse Electric Corp., P.O. Box 1521, MS 3T15, Baltimore, MD 21203; (410) 765-7348; fax (410) 993-7747.

USENIX 1998 Technical Conference, June 13-17. Marriott Hotel, New Orleans, Louisiana. Contact USENIX Conference Office, 22672 Lambert St., Suite 613, Lake Forest, California 92630; (714) 588-8649; (714) 588-9706; e-mail: conference@usenix.org; www.usenix.org.

35th Design Automation Conference, June 15-19. Moscone Center, San Francisco, CA. Contact MP Associates, 5305 Spine Rd., Suite A, Boulder, CO 80301; (303) 530-4333; e-mail: dac-info@dac.com; www.dac.com.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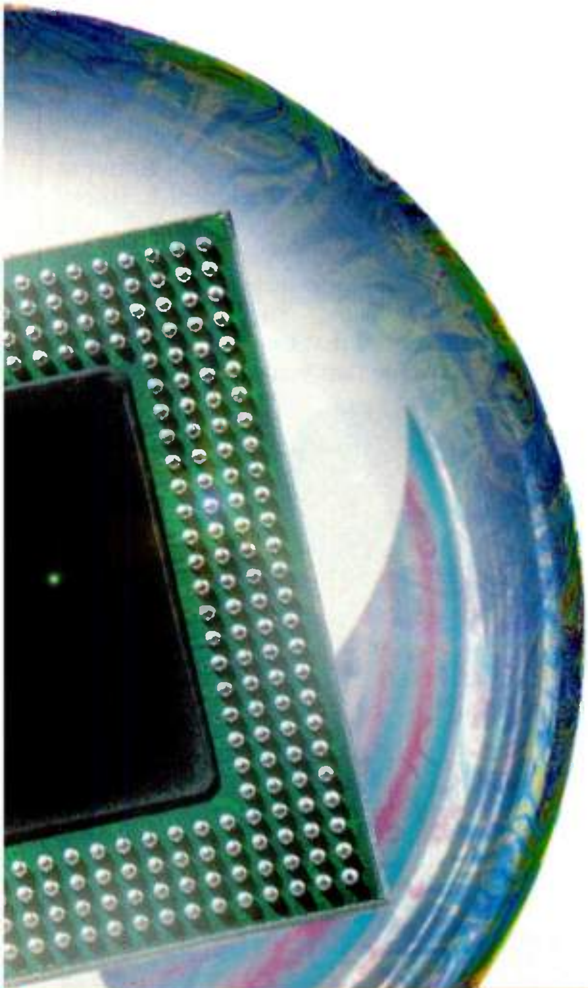

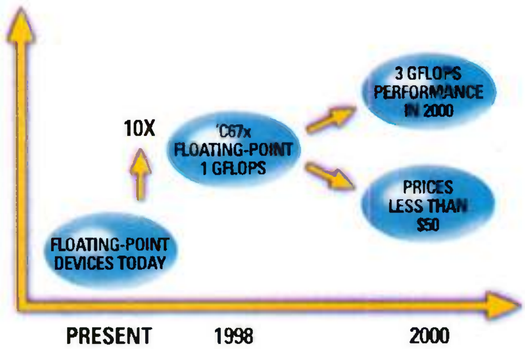

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EDITORIAL

Child And Desposito Join The Team

I'd like to take this opportunity to introduce you to our newest Technology Editors, Jeff Child and Joseph Desposito. Child, former long-time Senior Editor at *Computer Design* magazine, joins *Electronic Design* as Computer Systems Editor. Desposito comes to us from Weka Publishing Inc., where he served as Editor of two consumer publications, *Electronics Repair Manual* and *Modern Electronics Manual*. He will be serving as Test and Measurement Editor.

Child takes over the duties of former Technology Editor, Rich Nass, who has been promoted to Managing Editor of our new launch, Penton's *Embedded Systems Development* magazine, which debuts this month. Desposito replaces long-time *Electronic Design* Test and Measurement Editor, John Novellino, who has been promoted to Managing Editor, in charge of Special Projects.

Based in our New England office, Child brings solid credentials and years of experience covering computer systems. He is well-known throughout the industry and, as an engineer, brings to *Electronic Design* the in-depth technical knowledge to cover this important technology beat. During his career, he has consistently reported on single-board computers, bus architectures, memory, semiconductors, microprocessors, DSPs, Analog ICs, debuggers, emulators, network technology and broadband communications. Prior to his tenure at *Computer Design*, Child worked for ADAC Corp., as a designer/draftsman, and at Wang Laboratories as a quality assurance auditor.

Desposito's experience and background in test and measurement stems from his eight years as Senior Project Leader at *PC Magazine*'s PC Labs. He developed testing scripts and coordinated the testing of microcomputers, peripherals, and software. Desposito also authored product review articles and technology overviews. Prior to that assignment, He was Technical Editor at *Creative Computing Magazine*, and earlier served as Technical Editor of *Popular Electronics/Computers & Electronics*. Desposito also has written articles for *MicroComputer Journal*, *PC Magazine*, *Computer Telephony*, *Personal Computing*, and other electronics and high-tech publications. He will be based in our Hasbrouck Heights, N.J. office.

All of us here at *Electronic Design* are excited that two top professionals have joined our growing team of editors. I know that you will reap the benefits of their articles in the coming years.

Tom Halligan
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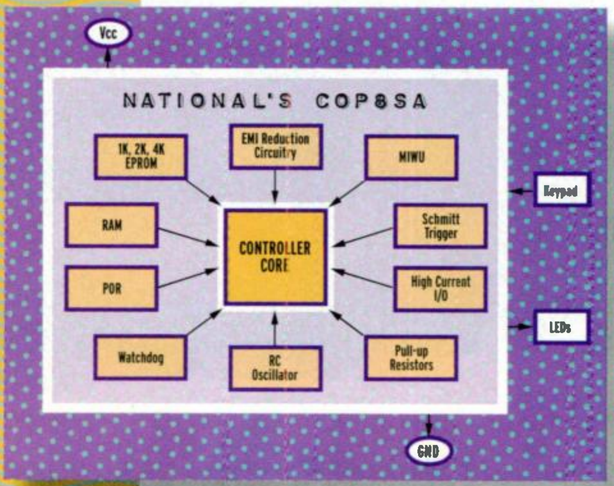

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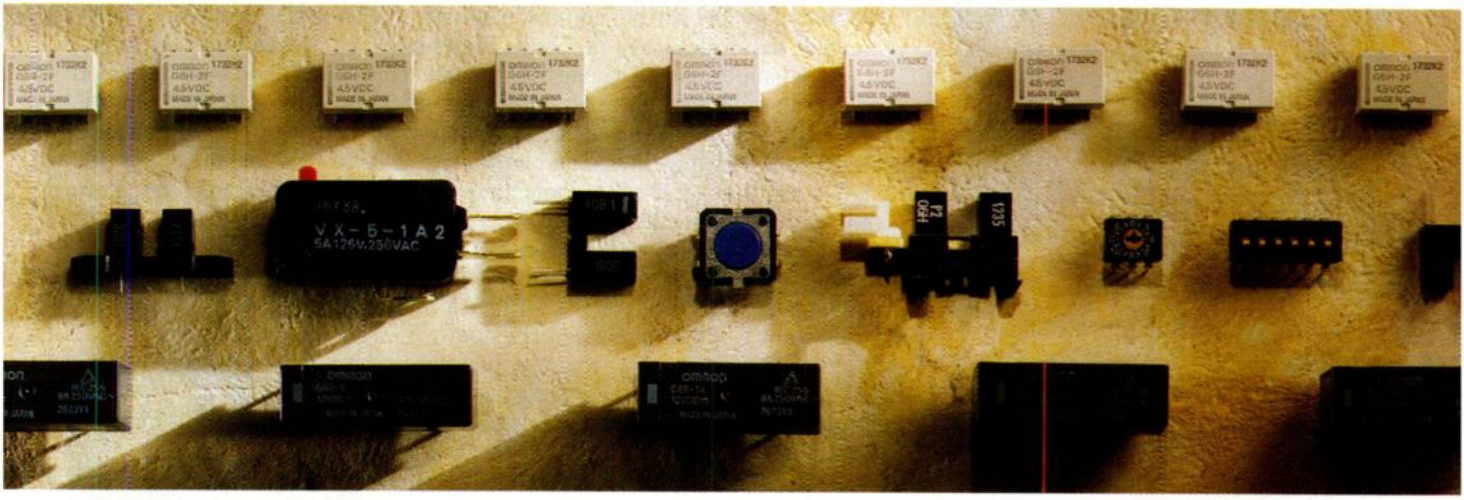

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To Benchmark Or Not To Benchmark?

I think we can all agree that on the surface, benchmarks sound like the perfect solution to an age-old dilemma: evaluating EDA tools. There's only one problem—many EDA vendors, for a variety of reasons, refuse to take part in them. Some would argue that these vendors are afraid their tools' performance won't match up against the competition's. Of course, if you ask companies that have refused to take part in a benchmark why, they will most likely tell you that they feel the benchmark is unfair.

A perfect example is the pc-board benchmark conducted as part of the PCB Design Conference. Although it was held this year, it had been canceled in the past, due to lack of interest on the part of EDA tool vendors. Even this year's benchmark failed to see the inclusion of a number of companies with significant tool offerings in the pc-board area. There's still an lack of participation, despite the fact that the benchmark was developed to help end users get information on specific capabilities of participating vendors' tools, as opposed to a test to determine the best overall pc-board EDA tool.

You would think that EDA vendors would jump at a chance to validate their tool claims and placate the majority of end users who complain that what they want is not always what they get when they purchase EDA tools. It's exactly this reasoning that has prompted many EDA tool vendors in recent years to become more "customer friendly."

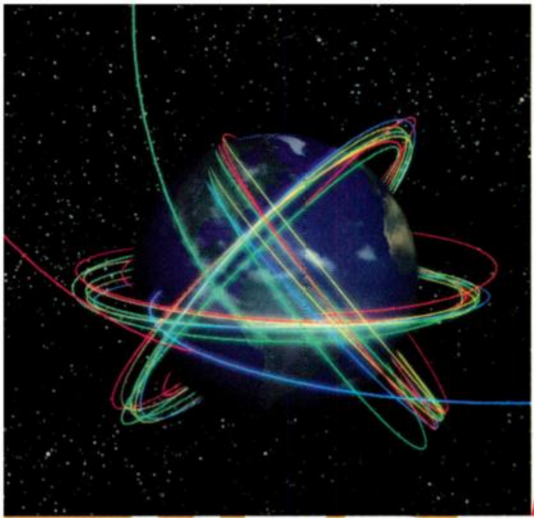

CHERYL AJLUNI
ELECTRONIC DESIGN AUTOMATION

But, if EDA companies honestly want to address end-user needs and concerns, and the end users have voiced their need for an easy way to evaluate tools, why aren't the tool vendors taking part in benchmarks? If they feel a particular benchmark is unfair, then why not come together as an industry (with other EDA tool vendors who also believe a benchmark is unfair), and develop one that they can all agree is fair. It seems like such a simple concept doesn't it? If you are committed to meeting the needs of your customers, it would make sense to do this.

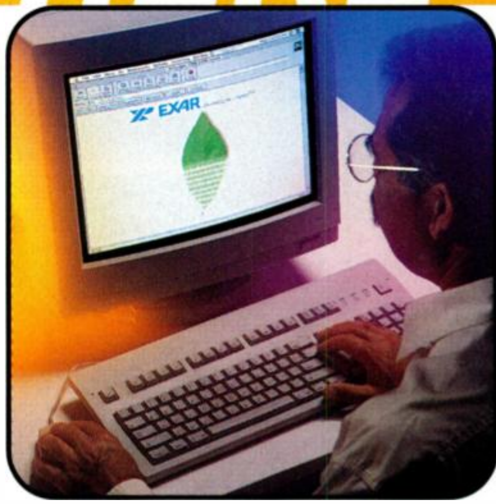
Think again. Life is never that easy. Instead, many designers today are forced to turn elsewhere to get that critical evaluation information. They rely on recommendations from colleagues, their own benchmarks, or on the vendor's claims of expected tool performance. Unfortunately, benchmarks done by potential users are often incomplete because designers don't have the time to invest in obtaining high-quality, accurate results. And, trust in a vendor's claims—well let's just say that vendors don't blatantly lie about their tools' performance. They will, of course, inflate the truth or shade it to favor themselves. But, then again, aren't we all just a little bit guilty of this one? Some people call it advertising.

It's like those beer commercials where the two nerdy guys open the can of beer and suddenly they are surrounded by beautiful women falling all over them. We all know this doesn't really happen. But the implication is still there, that if you drink the beer you will become one of the "in crowd" and it will be easier for you to get the beautiful girl. It's a textbook advertising scheme. And, it works. Otherwise, you'd see those ads disappear.

When all is said and done, the fact remains that designers want and need a method for evaluating EDA tools. They especially need one that is fair and offers insight into what significant or unusual features a tool offers. This way, the designers can choose for themselves which tool they want to use depending on what critical elements they may need and how well they stack up in the market. After all, not everyone likes anchovies on their pizza, but I dare you to find one pizzeria that doesn't offer it as an option. Why? Because some people do like anchovies, and a good rule of business is, and always will be, "Give the customers what they want!" Now only if EDA tool vendors understood this... *cjajluni@class.org.*



BETWEEN HERE AND HERE IS THE ~~HARD~~ PART. Exar



The hard part of digital communications all depends on the type of system you're designing.

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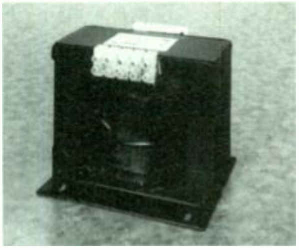
High Power International Transformers



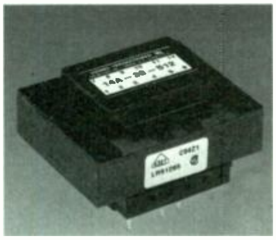
Signal's HPI transformers incorporate unique coil construction that complies with international safety standards that results in a smaller and lighter transformer. The HPI transformers operate from 2000 VA to 3500 VA, have dielectric strength of 4000 VRMS Hipot, and leakage current that meets medical applications.

The transformers are recognized to UL 506 and certified to CSA C22.2 #66, VDE 0550 and TUV IEC 950.

CONTACT: Signal Transformer Co., Insilco Technologies Group, 500 Bayview Ave., Inwood, NY 11096-1792. Phone: (516) 239-5777; fax: (516) 239-7208.

READER SERVICE 92

International Printed Circuit Transformers



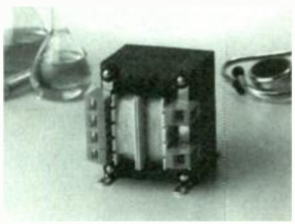
Signal Transformerís One-4-All™ (14A) printed circuit mount transformers are designed for use in international low power applications. Recognized to UL 506 and certified to CSA C22.2 #66, VDE 0805 / EN 60950, and IEC 950, the transformers also have the creepage and clearance necessary to comply with international safety standards.

With an operating power range of 2.5 VA to 56 VA, the transformers are used in low power applications and provide high isolation of 4000 VRMS Hipot.

CONTACT: Signal Transformer Co., Insilco Technologies Group, 500 Bayview Ave., Inwood, NY 11096-1792. Phone: (516) 239-5777; fax: (516) 239-7208.

READER SERVICE 93

More-4-Less™ International Transformers



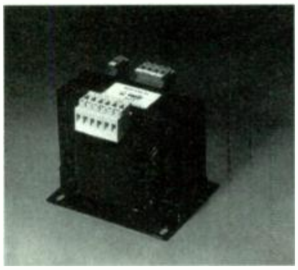
Signal's M4L Series high-power, isolation transformers satisfy UL, VDE, IEC, and CSA transformer requirements for low power isolation in numerous applications.

The M4L Series transformers comply with UL 544, the standard for both medical and dental equipment, and UL 506, the standard for specialty purpose transformers with 250 volt or less input. They are available in models from 300 VA to 1,000 VA, are extremely compact, and lighter than conventionally wound transformers.

CONTACT: Signal Transformer Co., Insilco Technologies Group, 500 Bayview Ave., Inwood, NY 11096-1792. Phone: (516) 239-5777; fax: (516) 239-7208.

READER SERVICE 94

Multi-Purpose International Transformers



Signal Transformer's Multi-Purpose International Series (MPI) high-power transformers operate from 200 VA to 900 VA and feature higher volumetric efficiency than conventional 50/60 Hz transformers.

Featuring unique coil construction and winding methods, the MPI transformers have exceptionally good isolation of 4000 VRMS Hipot and low leakage current. They also have a 5 mil thick copper Faraday shield to reduce common mode noise. Faston/screw type shock-proof terminals are used on the series.

CONTACT: Signal Transformer Co., Insilco Technologies Group, 500 Bayview Ave., Inwood, NY 11096-1792. Phone: (516) 239-5777; fax: (516) 239-7208.

READER SERVICE 95

"Smart Trailers" To Talk With Drivers Via Spread Spectrum

A recent technology demonstration proved the feasibility of using spread-spectrum signals carried over a semi-trailer's existing lighting wiring to provide truck drivers with vital safety information. Using spread-spectrum power-line carrier communication, the system emulates an industry-standard 9600-baud RS-485 transceiver. This enables two-way communication between a truck and its trailer across the standard SAEJ560-style connectors found in all commercial trailers without adding any extra wiring. this was the culmination of an engineering project, known as power-line carrier for trucks (PLC4TRUCKS), was undertaken by Intellon Corp., Ocala, Fla., under the direction of an industry consortium of truck, trailer, and truck-component manufacturers. The project was organized to help the truck industry comply with a federal mandate to give semi-rig truck drivers a way to monitor the status of the anti-lock braking systems (ABSs) in their trailers by the year 2001.

In addition to monitoring the ABS and other safety functions, the new system enables a low-cost means to monitor and control refrigeration units, load-leveling devices, and other active systems that might reside within a trailer. The temperature and condition of cargo also can be easily monitored via the trailer-to-cab data link. For further information, contact Intellon Corp., 5100 W. Silver Springs Rd., Ocala, FL 34482; (352) 237-7416; fax (352) 237-7616; *www.intellon.com.* LG

Telemedicine Project Holds Trial Operations In Mozambique

The first telemedicine service in Mozambique was recently inaugurated, making it one of the first of its kind on the African continent. The pilot project was established as part of the Internation Telecommunications Union's (ITU) Telecommunication Development Bureau (BDT) project to evaluate how information technologies can be most effectively used for expanding health-care services in developing countries.

The service will enable two hospitals in the towns of Beria and Maputo to use standard equipment to exchange medical images and lab test results. Conferencing via voice and exchange of written text or graphics also will be supported. Low-cost standard equipment used in the project will make it possible to expand the reach and scope of the services they can offer, including medical consultation, pathology diagnosis, education, and emergency services. BDT director Ahmed Laouyane explained that "Telemedicine will help extend specialist care to those currently without easy access to medical institutions or the specialists they actually need."

For further information, contact Leonid Androuchko, Telecommunication Department Bureau, ITU, Place des Nations, CH-1211, Geneva 20, Switzerland; phone: +41 22 730 5433; fax: +41 22 730 5484' e-mail: *androuchko@itu.int.* LG

Novel Direct Conversion Receiver Reduces Component Count

By demonstrating specifications with a sensitivity of-104 dB, a 1-GHz bandwidth, an IP3 of +15 dB, and a 5-dB noise figure, a new direct-conversion-receiver architecture is setting its sights on becoming a key building block for wireless systems. While the details are still sketchy, pending patent filings, the new design promises to reduce both component count and power requirements in applications such as audio, video, and data links; cellular phones; pagers; cordless phones; and cordless computer peripherals. Prototype versions of the receiver have been fabricated in both CMOS and GaAs. Early tests show that it can substantially reduce parts count in most applications. The circuit's developers, ParkerVision Inc., claim that it only takes five components, worth about $5, to implement a 900-MHz radio. Using a conventional approach with that same radio, parts count soars to around 30, and it would have a BOM of $12.

At a recent demonstration, a prototype receiver IC was shown to receive a wideband signal centered around 980 MHz with almost no discernable amplitude or phase distortion while drawing less than 10 mA of 3.5-V power. Requiring no narrowband LNA front end, the receiver can convert two or more signals down to its baseband simultaneously. If this seems like science fiction, parties interested in licensing the technology or purchasing components will soon be able to obtain test results from an independent lab. Contact Joe Scovron at Parker Vision Inc., 11000 S.W. Stratus, Suite 330, Beaverton, OR 97008; (503) 526-5891; fax (503) 526-5893 for more information. LG

1394 Group Aims To Make Firewire, GPIB Compatible

If members of the 1394 Trade Association have their way, the IEEE-1394 (Firewire) protocol will eventually be able use the same test program code as the IEEE-488 (GPIB) protocol. Association members, with Keithley Instruments Inc. and 3A International Inc. among the leaders, convinced the association to form an Instrumentation, Industrial Control Product Design Work Group (IIWG). Their first order of business is to figure out how IEEE-488 commands can be used with IEEE-1394-based systems. This would allow the same test code to be used with both protocols.

Because Firewire features higher data rates, easier

“We all offer the leading development tools. But at IDT, we suggest choosing your MIPS partner alphabetically.”

“We all give you great price/performance. But the rational, reasonable, sensible choice is LSI Logic. Logically speaking, of course.”

“You get a wide choice of MIPS partners. LSI, NEC, IDT, NEC, Toshiba, NEC, Philips. Did I mention NEC?”

“Before you choose a partner for this open architecture, consider this: the last three letters of MIPS are the last three letters of Philips. Spooky.”

system integration, lower costs, and the convenience of plug-and-play with hot swapping, it could become as common as GPIB in measurement and control systems, according to Keithley. Keithley staff engineer Gary Sakmar and 3A International president Andreas Schloissnik say that IEEE-1394's high bandwidth and integration into PCs and operating systems will benefit any data-acquisition or control application. The association is inviting companies involved in the development and use of measurement and control systems to sign up and discuss protocols related to measurement units, industrial controllers, test systems, and related services.

For more details on the work group, contact Sakmar at Keithley Instruments, (440) 248-0400; fax (440) 248-6168; e-mail: *sakmar_gary@keithley.com*. For information on the 1394 Trade Association, contact Richard Davies, (415) 777-4161, e-mail: *ipra@netcom.com*. JN

Orbital Messaging System Deployment Underway

Two recent successful launches that placed a total of 10 small communication satellites into low-earth orbit have brought the ORBCOMM global messaging system to the threshold of commercial operation. Eight of the 100-lb. spacecraft were launched into a 45°, 810-km orbit using a single Pegasus XL air-launched rocket. The other two were piggy-backed as secondary payloads on a Taurus launch vehicle. When they complete their on-orbit checkout and enter service, the new arrivals will bring the ORBCOMM fleet up to a total of 12 satellites out of its planned 36-unit constellation.

Designed for remote access using low-cost, low-power VHF transceivers, the system will let users send and receive text messages between any Internet node or any other ORBCOMM receiver at a cost of 1 cent per character or less. Even in this partially developed state, the satellites will be able to deliver inexpensive, two-way global messaging service during approximately one-half of any given day.

For further details, contact Magellan Systems, 960 Overland Ct., San Dimas, CA 91773; (909) 394-500; fax (909) 394-7050; *www.magellangps.com*. LG

Portable Voltage Standard Nearing Completion

The Primary Standards Laboratory at Sandia National Labs, Albuquerque, N.M., is responsible for assuring the accuracy of measurements for the Department of Energy by certifying standards and developing measurement techniques. In fact, each year the laboratory performs over 2000 certifications of top-level standards. Now, as a result of a three-year project funded jointly by Sandia and the National Institute of Standards and Technology (NIST), Boulder, Colo., researchers have found a way to make this certification process easier.

What they developed is a compact, fully automated calibration system for dc reference standards and digital voltmeters known as the portable Josephson Voltage Standard. The standard is based on a Josephson Array Chip fabricated by Hypres Inc., Elmsford, N.Y. It calls for all system electronics to be integrated into a single 13-cm-high, rack-width box that's controlled by a laptop computer. The result is a standard that's not only three times lighter and seven times smaller than the more conventional laboratory systems, but it features an accuracy of better than 0.02 parts per million—much more accurate than the larger laboratory voltage standard. And, because the standard is portable, it can be easily circulated among the nine different NASA labs, as opposed to being constrained to one facility.

A prototype of the system has been built. It's cooled by liquid helium with a 100-liter Dewar sufficient to operate the system for up to eight weeks. To date it has already successfully passed two field tests held this past year at the NASA White Sands Test Facility in Las Cruces, N.M., and at the NASA Kennedy Space Center in Florida. Currently the system is being circulated among NASA's nine labs to train and debug any problems that might show up during day to day operation.

For further information on the portable voltage standard, check out the Sandia National Laboratory web site at *www.sandia.gov*. CA

ATSC Restates Definitions For HDTV And SDTV Standards

The Executive Committee of the Advanced Television Systems Committee (ATSC) has approved a statement regarding the identification of the HDTV and SDTV transmission formats within the ATSC Digital Television Standard. An excerpt of the statement is as follows:

"There are six video formats in the ATSC DTV standard which are 'High Definition Television.' They are the 1080-line by 1920-pixel formats at all picture rates (24, 30, and 60 pictures per second), and the 720-line by 1280-pixel formats at these same picture rates. All of these formats have a 16:9 aspect ratio.

The remaining 12 video formats, while representing some significant improvements over analog NTSC, are not High Definition Television. They are referred to as 'Standard Definition Television.' These are the 480-line by 704-pixel formats in 16:9 widescreen and 4:3 aspect ratios, at the picture rates listed above, and the 480-line by 640-pixel format at a 4:3 aspect ratio, at the same picture rates."

For more information, contact the ATSC at (202) 828-3130; fax (202) 828-3131; e-mail: atsc@atsc.org; www.atsc.org. RE

Edited by Roger Engelke

The Broadest Selection of Hot Swap Power Manager™ ICs

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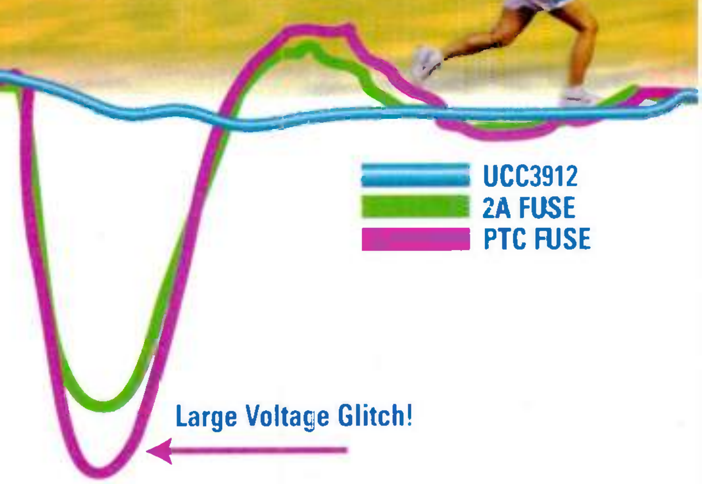

When you're connecting a PCB or peripheral to an active bus, Unitrode's Hot Swap Power Manager ICs provide the fastest response to overcurrent problems and maintain the highest degree of data integrity under any fault condition. Some devices can control over 1000V - leaving the competition in the dust. In fault condition, a low duty cycle retry mode significantly reduces average FET power dissipation.

Full System Operation During Board Hot Swap

PARTS WITH INTERNAL MOSFET

Part Number	Voltage Range	Maximum Current	RDSon
UCC3912	3 to 8V	4A	0.15Ω
UCC3915	7 to 15V	5A	0.15Ω
UCC3916	SCSI TermPower	2A	0.22Ω
UCC3918	3 to 6V	5A	0.075Ω
UCC3920	-3 to -15V	4A	0.1Ω

PARTS WITH EXTERNAL MOSFET

Part Number	Voltage Range	Power Limit
UC1914	4.5 to 35V	Yes
UCC3917	7 to >1000V	Yes
UCC3919	3 to 8V	Yes
UCC3913	-7 to>-1000V	Yes
UCC3921	-3 to>-1000V	Yes

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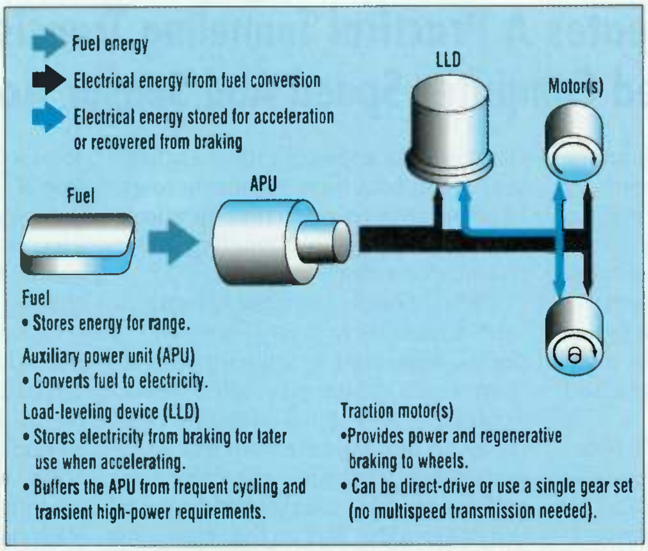
READER SERVICE 122

sedans, while using fuel at the equivalent of 80 to 150 miles-per-gallon (MPG).

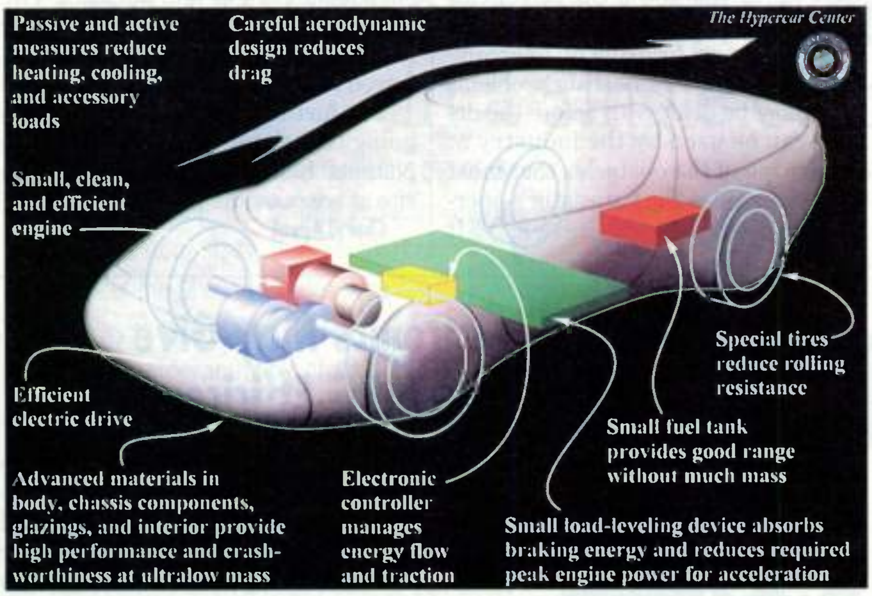
In a keynote address at the Wireless Symposium/Portable By Design conference, held last month in Santa Clara, Calif., Lovins explained how his team intends to deliver on such fantastic-sounding claims by re-engineering the automobile manufacturing process using lessons from the portable electronics industry. The result should be a next-generation vehicle at close to the same price of a conventional sedan.



2. The hybrid-electric power train converts fuel into motive force using a high-efficiency auxiliary power unit that drives electric motors mounted on each wheel. The car would also employ a load-leveling device (a battery, super capacitor, or flywheel) to store excess power for use when needed for acceleration and extended uphill climbs. The LLD also permits recovery of energy during braking.

A quick look at conventional autos reveals that most of the energy they use never reaches the drive wheels. The engine itself is only 15% to 20% efficient. Wind resistance, rolling friction, and braking inefficiency eat up much of that 15% to 20%, leaving less than 2% of the energy expended being used to actually propel passengers. Preliminary studies showed that much higher efficiencies were possible.

Dubbed the "hypercar" by its creators, the proposed vehicle will capitalize on the combined effects of several technologies to produce its anticipated performance. First, a super-strong molded carbon/aramid fiber-composite body will reduce the size of the engine required to push the car around *(Fig. 1)*. Next, a low-drag aerodynamic shape, an actively tuned suspension, and low-rolling-resistance tires will further minimize power requirements. This lower power requirement will allow the use of a much smaller, lighter, high-efficiency power plant.



1. A cutaway of the proposed hypercar reveals its energy-saving features and the advanced electronics that will make them possible. Improved aerodynamics and energy recovery techniques also play an important part in the overall energy-saving plan.

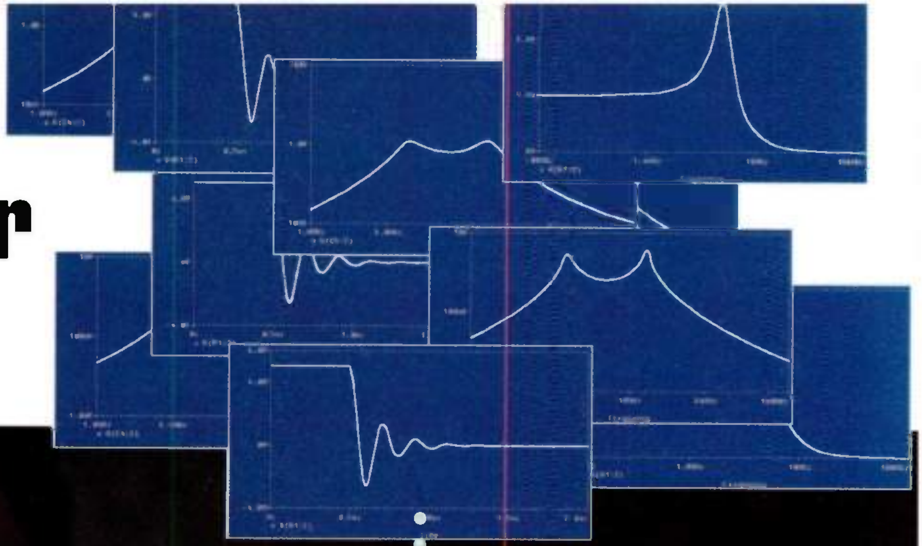
The first hypercars will use a hybrid-electric propulsion system that will burn either gasoline or natural gas. Their highly tuned, constant-speed internal combustion engines will produce the electricity for the drive motors mounted on each wheel *(Fig. 2)*. A small storage system (battery, flywheel, or super capacitor) will store surplus energy for use when extra power is needed for quick acceleration or maintaining speed on long hills. Using today's technology, a five-passenger vehicle, complete with air conditioning, a good entertainment system, and lively acceleration, would deliver fuel economy of 80+ MPG, according to Lovins.

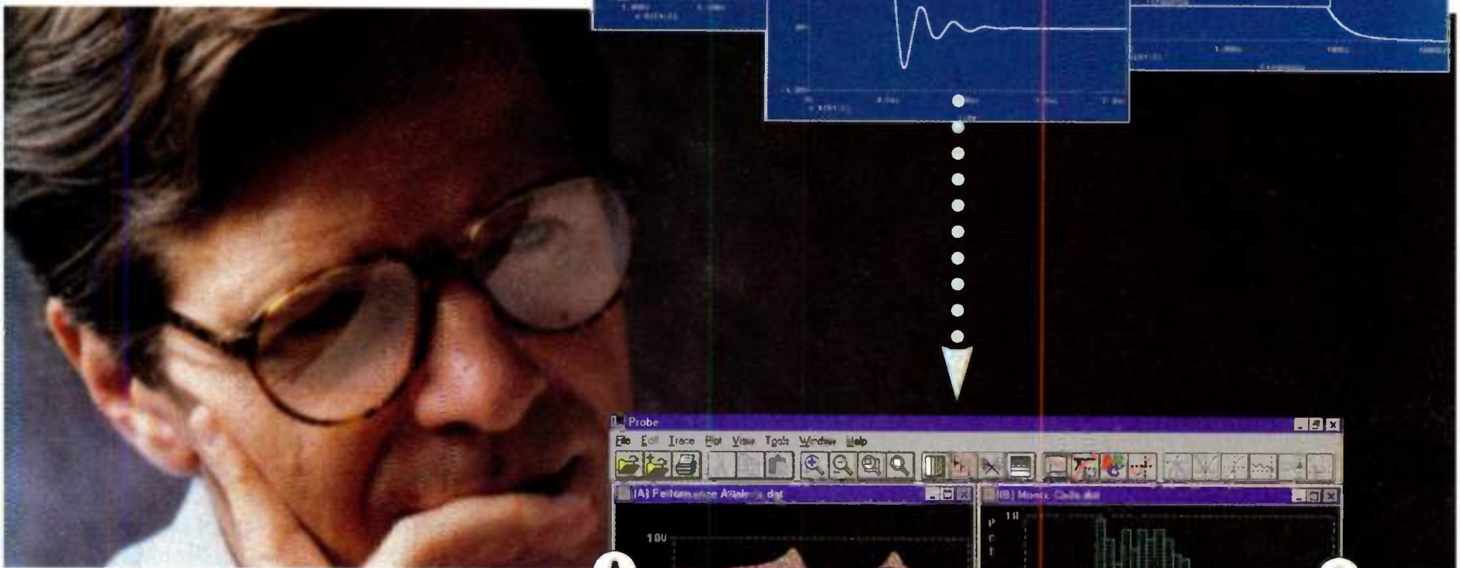
Subsequent generations of vehicles may use high-efficiency fuel cells to extract electricity directly from natural gas or hydrogen. Other candidate power plants include Stirling-cycle thermal engines and compact gas turbines. If practical, the car will use its own waste heat recovery to generate electricity and drive its heating and cooling systems. When fully optimized, Lovins predicts hypercars will have equivalent fuel efficiencies approaching 200 MPG.

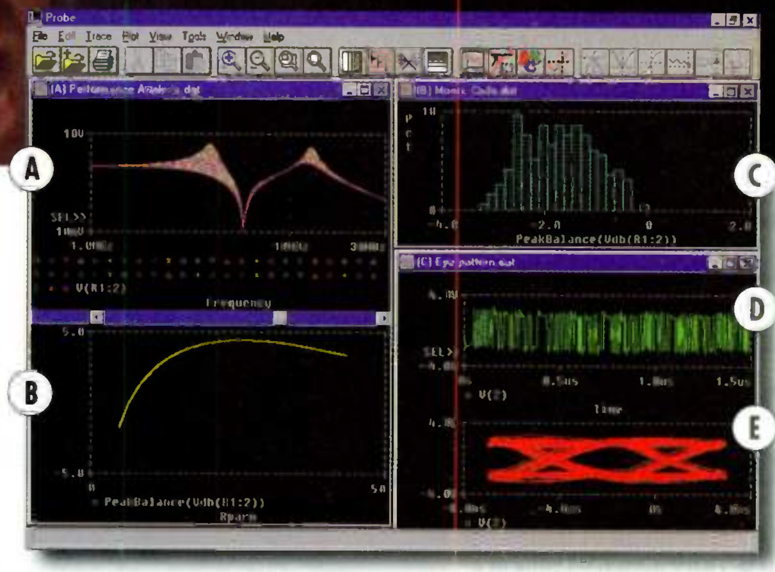
One key to achieving extreme efficiency from these vehicles is that their electronics subsystems will be designed to work in concert with each other, as well as with the car's mechanical system. The car's operating system will permit interaction between its subsystems, thanks to an open hardware and software architecture. This will allow manufacturers to add their own unique features to their product while maintaining basic interoperability with the vehicle as a whole. Communication between all systems will be over military-style, dual-redundant, polymer fiber-optic links, greatly reducing the mass and volume of wiring required in the vehicle.

This concept of "whole-vehicle electronics" will allow the engine and drive train components to interact with each other, as well as the car's actively tuned suspension system. For example, the suspension system will

Why Just Simulate Your Design...







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READER SERVICE 300

Extract performance from many simulations (A) to see how complex circuit behavior varies with component value changes (B)

Histograms (C) show production yields with component tolerances

Macros and functions allow you to measure performance (E) from complex waveforms (D)

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sense the weight and location of passengers in the car, and adjust the suspension's stiffness on each wheel accordingly. Likewise, it will pass on the data to the engine and braking systems so that they can optimize their control algorithms around specific load parameters. The suspension will also work with the steering and antilock braking systems to increase traction and handling by distributing loads to where they are most needed. During hard cornering, the control system will drive each wheel's motor independently to perform dynamic steering. During braking, energy will be recovered and stored in the load leveling device for use in subsequent accelerations *(Fig. 2, again)*.

Virtually every area of the car will represent business opportunities for electronics companies. Sophisticated electronics will be required for the car's motor-control and energy-management system. Postage stamp-sized "radar-on-a-chip" modules will be embedded into the body structure to provide proximity warning, collision-avoidance, and airbag activation. The same on-board radar also may be used to partially automate parking in tight spaces.

Even the humble dashboard will use advanced electronics to save cost and deliver superior performance. The car's "virtual display" panel will be similar to the "glass cockpits" found in most commercial and military aircraft. Drivers will be able to customize the flat-panel display, selecting the size and style of the "soft gauges," and arranging them in a way most comfortable to them. Malfunctions, navigation updates, and incoming communications will command the driver's attention by overriding the normal display configuration.

While the hypercar may seem like something out of a science fiction novel, Lovins and his associates are quite determined to making it a reality in the near future. This spring, the Hypercar Center will host a design exercise that will produce plans for a prototype vehicle. Open to all interested parties, the design team roster already includes an impressive list of large and small companies from the automotive, electronics, computer, and aerospace industries. Significant interest also has been demonstrated by auto parts manufacturers who are eager to acquire a larger piece of the automotive profit pie.

Construction of the prototype will probably begin later this year. Preliminary costs for the engineering test bed are anticipated to be $8 to $12 million, plus in-kind donations of parts and materials from various suppliers. Once the prototype is proven, plans call for a pilot production facility to be established. While tooling costs for producing the molded-composite chassis/body structure will be much lower than for a steel vehicle, current estimates are that it will take about $3 billion dollars to get the facility operational. Most of the needed funds are already committed—much of it from electronics, automotive, and parts manufacturers and energy suppliers—making production start-up around the turn of the century quite possible.

Lovins contends that the immediate, dramatic improvements in performance he proposes will actually cost less than incremental changes because the hypercar will require a complete rethinking of the design and function of the product. He calls this process "tunneling through the cost barrier," a technique his team has used to reduce energy consumption in buildings.

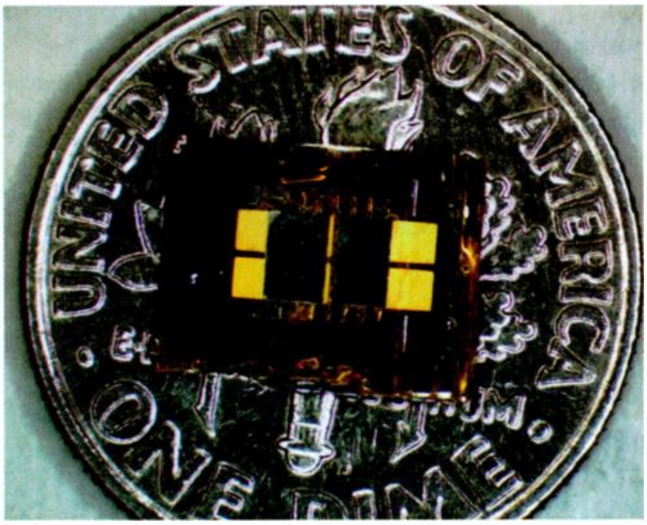
For further information about the hypercar project, contact the Hypercar Center at the Rocky Mountain Institute, 1739 Snowmass Creek Rd., Snowmass, CO 81654-9199; (970) 927-3851; fax (970) 927-4178; Internet: www.rmi.org.

Lee Goldberg

Batch Processing Yields High-Current, Low-Cost, Magnetically Operated Relays That Can Be Mounted On Circuit Boards

A new type of magnetically actuated microrelay that can be batch processed using established micromachining techniques has far-reaching implications for automobile electronics, test equipment, and other areas. Because their fabrication techniques are compatible with standard microelectronic processing, the devices can be integrated onto circuit boards.

The devices' design allows similar configurations to be used for both normally on and normally off, as well as for multipole relays. Developed by researchers at the Georgia Institute of Technology, Atlanta, Ga., the devices also feature small size, low contact resistance, and the ability to switch large loads *(see the figure)*.



Able to be batch processed, the magnetically actuated microrelay features a low contact resistance and the ability to switch large loads.

According to William Taylor, a researcher at the School of Electrical and Computer Engineering, "The significance of a magnetically actuated relay is that you can achieve larger forces and a greater air gap between contacts when compared to electrostatic relays. The larger gap holds off a higher voltage, which allows you to switch higher voltages than would be allowed with other types of relays." Microrelay devices

also require lower actuation voltages than their electrostatic counterparts.

The microrelays operate at voltages of less than 5 V, allowing them to be driven by digital logic circuits. Their contact resistance of less than 100 mΩ allows them to switch currents of up to 1.2 A. The devices range in size from 3 by 4 mm up to 7 by 8 mm, and are less than 200 µm high. Several configurations are available to meet the voltage, current, and actuation-force requirements of different applications.

The microrelay, which is fabricated using standard polyimide-mold electroplating techniques, consists of an integrated planar meander coil and one or more pairs of relay contacts positioned above the coil. A movable plate, made from a magnetic nickel-iron material, is surface micromachined above the contacts. When current is applied to the coil, the magnetic flux generated pulls the nickel-iron plate down until it touches the contacts, thereby closing the circuit.

The normally closed version works in the opposite way, using a permanent magnet to hold the actuating plate down and the contacts closed. When current is sent through the relay's coil, the plate moves up off the contacts, opening the circuit. The permanent magnet for this type of relay is not currently made through micro-machining techniques, and therefore must be added during the fabrication process.

The fabrication process itself begins with an oxidized silicon wafer. The researchers then deposit a seed layer, and electroplate a lower magnetic core, adding an insulating polymer mold above that. Then a coil is electro-deposited and coated with an insulator. The fabrication is completed by alternating steps of polymer mold deposition and electroplating. Every step uses photolithographic techniques to build 100 or 500 relays on a wafer. Then they can just be cut up like semiconductor chips.

Microrelays manufactured with this process have been tested to 850,000 operating cycles without failure. A patent has been filed and Georgia Tech is looking for a commercial partner to license the technology. For more information, contact Mark Allen, associate professor, at (404) 894-9419, or e-mail him at mark.allen@ece.gatech.edu.

Patrick Mannion

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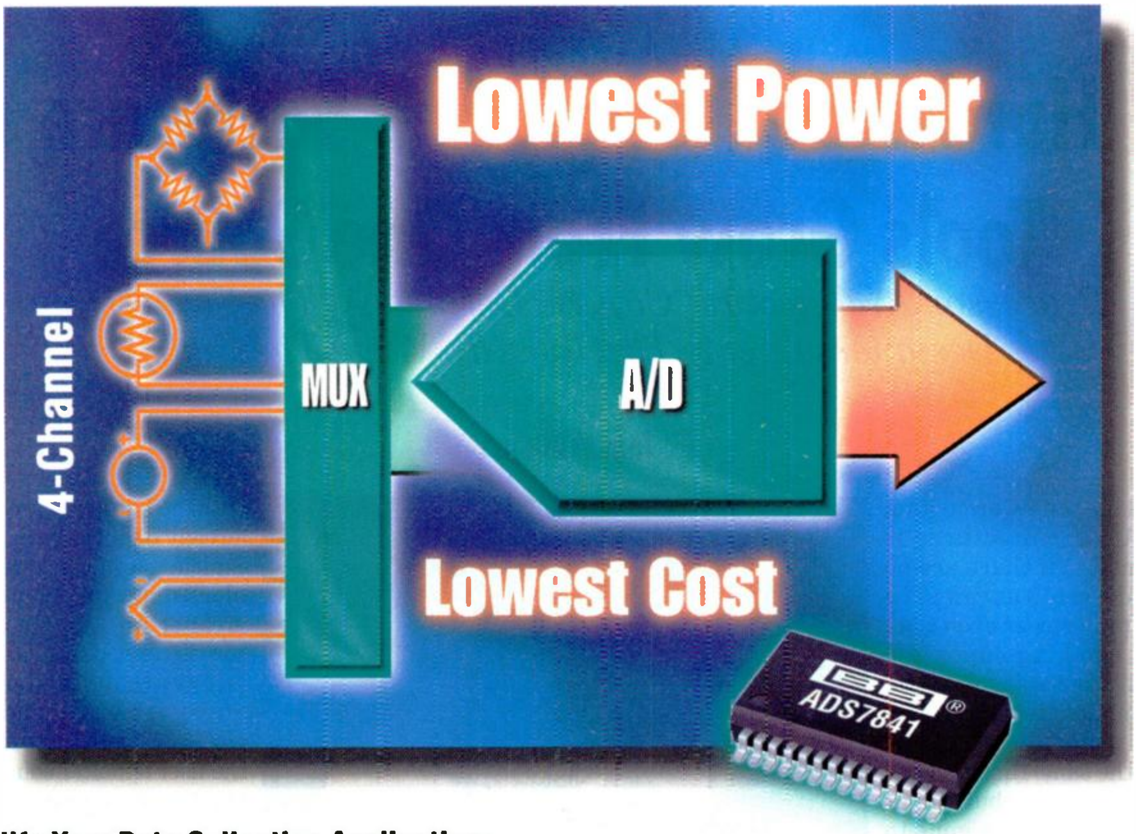

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ADS7841 Key Specifications:

- Single Supply: 2.7V to 5V
- 4-Channel Single-Ended or 2-Channel Differential Input
- Up to 200kHz Conversion Rate
- Serial Interface
- Alternate Source for MAX1247
- 16-Lead SSOP Package

Product	Resolution (Bits)	Channels	INL (LSB)	NMC*	Sample Rate (kHz)	Power (mW)	SINAD (dB)	Price (1kpcs)	FAX*LINE*# 1-800-548-6133	Reader Service #
ADS7824	12	4	±0.5	12	40	50	73	$12.30	11303	87
ADS7825	16	4	2	16	40	50	86	$28.46	11304	88
ADS7832	12	4	±0.75	12	117	14	71	$16.00	11332	89
ADS7841	12	4	±1	12	200	3	72	$4.59	11420	90

**No Missing Codes*

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Hardware Design And Software Tools Grow From One Source

Processor Architecture Can Be Defined At The Same Time Designers Create The Tools To Write The Code.

Tom Williams

COVER FEATURE

Creating a new or custom CPU architecture is pointless if there are no tools to develop software. The fates of projects, or even companies, can hinge upon the availability of a suite of assembler, compiler, debugger, and, hopefully, other development tools at the same time that the silicon makes its debut. Major manufacturers have gone to Herculean lengths to forge partnerships with tool developers that will orchestrate the design of both the silicon and the software.

Now, a single tool called SD/ToolSmith from Production Languages Corp., Fort Worth, Texas, is able to track the development of a processor architecture. It also generates a full set of basic development tools that are specific to that architecture, based on the architectural description. In the near future, SD/ToolSmith also will generate a register-transfer-level (RTL) VHDL description from the same architectural definition, and coordinate it with the development of the software tools.

Currently, the tools that can be produced by SD/ToolSmith include an assembler, a compiler, a debugger, and a cycle-accurate simulator. These tools can all be incorporated into a customizable graphical-integrated-development environment (IDE) that operates under the Windows operating system.

Deriving Instructions

At the core of SD/ToolSmith is the description of a processor's instruction-set architecture (ISA). The ISA can be thought of as an assembly-language programmer's perspective of the hardware. By making observations about the hardware block diagram, it is possible to derive the ISA description. From that you can produce the instruction-set description, the syntax by which the hardware operates.

Traditionally, a tool designer starts with the hardware architecture already defined. With SD/ToolSmith, users can start with a block diagram of a processor architecture. As that architecture is refined (e.g., as the registers are defined or as the ALU and other units are defined), the user simultaneously develops the instruction set along with the hardware design.

Facts about the architecture imply certain things about the way the instructions will work. For example, let's say a simple processor has two source buses connecting the ALU, multiply/accumulate unit (MAC) and register file (*Fig. 1*). Alternatively, it can fetch one of its operands from data RAM via the address bus. That means that two operands can be fetched simultaneously from three possible sources, for any instruction among these units, such as an ADD instruction. If there is, however, only one source bus, then only one operand can be an access to data RAM.

Given this simple fact of the layout of the units, an instruction that has two source operands, one of which can also be an access to data RAM, must be able to support the following operand combinations:

- register, data RAM
- register, register

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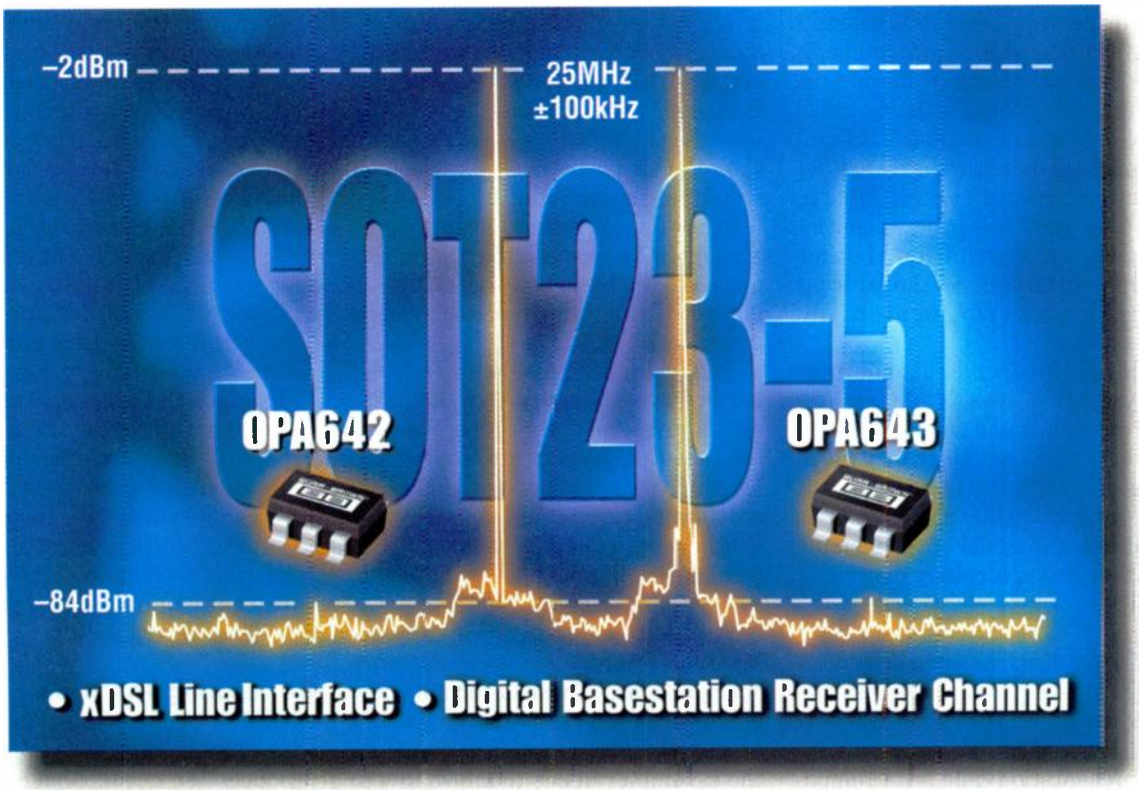
Communication Solutions



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Using a unity gain stable voltage feedback architecture with two internal gain stages, OPA642 achieves exceptionally low harmonic distortion over a wide frequency range (–95dBc at 5MHz). Its fast settling (13ns), low voltage noise, and high output current drive make the OPA642 ideal for high dynamic range applications such as high resolution imaging, wireless communications, data acquisition, and professional audio. Other specs include 0.007%/0.008° dG/dP, and 90dB common-mode rejection.

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OPA643 achieves low harmonic distortion over a wide frequency range by using a de-compensated voltage feedback architecture with two internal gain stages. Internally compensated for gains ≥+3 with 800MHz gain bandwidth product, OPA643 is particularly suited for wideband transimpedance amplifiers, moderate gain IF amplifier applications, and very low distortion ADC driving.

Key Specifications:	OPA642	OPA643
Low Distortion	–95dBc at 5MHz	–90dBc at 5MHz
Low Noise	2.7nV/√Hz	2.3nV/√Hz
Gain Bandwidth Product	210MHz	800MHz
High Open-Loop Gain	95dB	95dB
High Output Current	±60mA	±60mA
Pricing from (1000s)	$3.75	$3.75

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- register, register indirect
- data RAM, register
- register indirect, register

If the word length for this ADD instruction is 32 bits, it must have fields to store the supported addressing modes for each operand; the immediate, or direct, address; and the opcode. The opcodes, of course, indicate which instruction is to be executed. This simple example shows how hardware design and instruction definition can evolve together. This process continues through the definition of other functional units such as the address generator, program counter, and pipeline.

Defining the opcode also defines exactly what it does. Thus, adding source operand 1 and source operand 2 with carry will set the carry bit in the flag's register, and place the result on the destination bus at the address in the destination field of the instruction. All of this is formally described in detail.

A Unifying Representation

As the description of the instruction-set architecture is progressively refined, it is captured in a formal textual representation called the Temporal Hierarchical-Instruction-Set Language (THISL). The layout of the instructions and a functional description of their behavior is expressed in THISL. These descriptions are part of the definition of the functional units that make up the processor architecture *(Fig. 2)*.

The THISL description of the ADD instruction in the example is included in the THISL segment defining the ALU, which in turn, is part of the code defining the entire processor architecture. Note that the format of Figure 2 looks much like what one would expect to find in an assembly language reference manual.

The THISL file is created by entering the machine description derived from the hardware architecture into SD/ToolSmith using the data entry dialogs appropriate for the various elements of the machine. For example, they would include the register resources and register resource classes, tokens, addressing modes, instruction groups, and instructions, such as the ADD example described earlier. This file also is where mnemonics needed to generate an assembler are assigned to the opcodes.

In entering the machine description, it is important to go through each instruction, and define what happens in each stage of the pipeline. For example, a jump instruction may or may not have a condition code. If it does have one, it would place the jump address in the program counter only if the condition was true. Otherwise, it would do so immediately. After the machine description has been entered through these dialogs, the system can generate the basic body of the underlying code from which the tools can be generated.

SD/ToolSmith considers any architecture to be "pipelined" in the sense that a given instruction's semantics are executed in a series of clock cycles. Normally, we think of a pipelined architecture only when these cycles overlap. The more general concept of a pipeline is necessary, however, to gain cycle-accurate simulation.

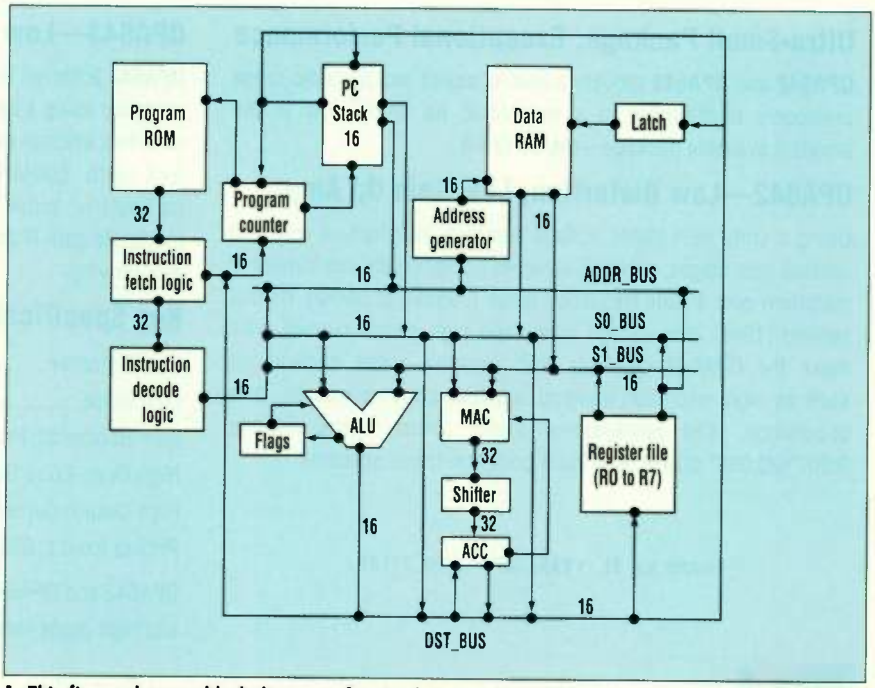
An additional step, prior to creating an assembler, involves defining "pack actions." These determine how values are placed into and extracted from instruction fields. In addition, the assembler needs to know how to translate an ASCII character or string into the proper binary form. These pack actions, as well as the functions assigned to opcodes, eventually manifest as microcode within the processor.

Although they may seem like abstractions, a register file and an ALU, which are defined in terms of bit fields and operations, also represent physical entities. These entities can be described by hardware definition languages, such as VHDL, and eventually synthesized as silicon using a variety of processes. As such, functional elements defined in THISL can be saved in libraries for used in future designs. They can either be used as is or edited for special needs.

Production Languages eventually intends to provide the ability to graphically wire together predefined functional elements. In addition, future versions will have the capability of automatically generating an RTL VHDL representation of the architecture that can be used to produce a gate-level description.

Generating The Tools

SD/ToolSmith does not generate an assembler as an executable file, but produces a source file that can be com-



1. This figure shows a block diagram of a simple instruction-set architecture. The diagram serves as the starting point for deriving the machine description. Details about the architecture, such as the buses connecting the ALU, MAC, and register file, have implications for the number and kinds of instructions needed for the various functional units.

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OPA2650 is a high speed, dual, low power (50mW/ch.), voltage feedback op amp featuring 360MHz bandwidth and 12-bit settling time in only 20ns. Its low distortion is ideal for communications. Its wide bandwidth and voltage feedback design make it ideal for active filter applications. OPA2650 is especially suited to high resolution video, CCD imaging and ultrasound due to its excellent pulse settling and DC precision.

OPA2650 is internally compensated for unity gain stability, and has a fully symmetrical differential input due to its "classical" op amp circuit architecture. OPA2650 is also available in single (OPA650) and quad (OPA4650) versions.

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Maximize your design options with OPA2650 and OPA2658 now available in MSOP-8 packaging. The same high performance and low power optimized for portable design!

Product	Bandwidth (MHz)	Slew Rate (V/µs)	I_Q (mA)	Package	FAXLINE# (800) 548-6133	Reader Service #
OPA2650	360	240	±11	8-pin DIP, SO-8, MSOP-8	11266	85
OPA2658	800	1700	±10	8-pin DIP, SO-8, MSOP-8	11269	86

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piled and linked using the Microsoft Visual C++ Developer Studio. First, it checks the machine description for errors, then begins the build process. Since the machine description is hierarchical, the system can walk that hierarchical tree structure and build context-sensitive "grammars," which are used as the basis for an assembler, a compiler, and a simulator. These grammars are read by an attributed predicated code generator (APCG) which polls the underlying THISL code based on the grammar to produce the C source files for the tool.

All this underlying grammar-building, parsing, and code generation is transparent to the user. Once the source files are loaded into the Visual C++ project and the Microsoft tools are configured, the final executable file can be built and the assembler is tested.

SD/ToolSmith can build either a bit-accurate or a cycle-accurate simulator. A bit-accurate simulator is useful for programmers because it models the processor's behavior at the instruction-set level, and hides what goes on in the pipeline. In addition, a bit-accurate simulator is faster than a cycle-accurate simulator. A cycle-accurate simulator, which does completely model the pipeline, is needed to compare expected behavior against a VHDL model.

To generate a simulator, you must decide which type you want and then add architectural semantics to the basic machine description. Architectural semantics describe the exact behavior of each entity in the machine description. They may include such things as the order of the phases in the pipeline, or the conditions under which data is placed on a given bus during a read instruction. Architectural semantics are at a much lower level of abstraction than the functional unit semantics described earlier.

The code generation for the simulator is straightforward, as in the case for the assembler. The Build Tool dialog box lets you select either the bit-accurate or cycle-accurate simulator, and generate the source files.

The SD/ToolSmith compilers consist of several predesigned machine-independent modules. The first is a front end that parses source code to an intermediate pseudocode. A machine-independent optimizer then produces an optimized set of pseudocode using general compiler optimization techniques. The optimized pseudocode is then run through a machine-dependent back end, which performs machine-level optimizations. Afterward, the back end produces assembly source code. The back-end module is based on the target machine description.

To produce a debugger, SD/ToolSmith uses a predesigned generic debugger that is adapted to the particular machine description by scripting files. The files are based on a debugger configuration file that is produced during the generation of the simulator, which is, of course, specific to the machine description.

To customize the debugger for the user, you can write subroutines that have display functions to show the contents of hardware entities, such as a hardware stack. The debugger would call the routine, such as stack_display, which would call the stack functional unit and get its value. The value is then sent to a routine that actually displays it. In fact, process internals such as stacks and registe can be displayed in a customized u interface under Windows. In a similar manner, all the tools can be given either a command-line or a Windows-based user interface.

Because the debugger is the most interactive tool, it is the one that makes the greatest use of a visual environment. Production Languages supplies a Windows-based debugger shell that can be customized to show exactly the registers, counters, and other elements within a given processor architecture. You can even design custom icons to represent things like breakpoints. However, all the tools can be given a command line interfa or be assembled into an integrated d velopment environment (IDE).

Once all the tools have been fitted with their own graphical interfaces they can be assembled into an environment under a single IDE control panel The IDE has a database that is specifi to the target processor and identifies all the tools used for that processor. In addition, it maintains information

ALU Instruction Group

ADD Instruction

Syntax:
ADD scr0,src1,dest

Description
Add scr0 to src1 and place result in dest.

Format:

0 1 2 3	4 5 6 7	8 9 10 11	12 13 14 15	16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
0 0 0 1	dest	scr0	scr1	IMM16

Execution semantics:

Fetch	Decode	Read	Execute	Write
		S0_BUS = scr0; S1_BUS = src1;		

			DST_BUS = S0_BUS + S1_BUS;
			c = S0_BUS[15:15] & S1_BUS[15:15];
			z = DST_BUS = = 0;
			n = DST_BUS[15:15] != 0;
			v = S0_BUS[15:15] & S1_BUS[15:15] &
			-DST_BUS[15:15];	

				dest = DST_BUS;

2. Shown here is the definition of the ADD instruction. The THISL code listing in the semantics section defines the behavior of the instruction, such as how the different bits in the flags register are affected. This listing, along with listings for other instructions in the ALU group combine to describe the ALU functional unit. The information that generates this code is entered in dialog boxes when entering the machine description.

M ▪ DM ▪ VX SERIES MODUFLEX® SWITCHERS

DESCRIPTION

Moduflex® Series form a comprehensive line of open frame power supplies assembled from standard "off the shelf" modules. The design features "State of the Art" topology, a meticulous thermal structure and the use of high efficiency circuits and components to attain the desired power density. The modular system concept reduces manufacturing to submodule assembly, capable of high volume production with a superior quality level at moderate costs.

M Series are available in output power ratings from 250-750 watts. **DM Series** are available with a 48VDC input and output power ratings of 400 and 600 watts. **VX Series** units consist of four specialty units with output power ratings of 500, 750, 1000 and 1500 watts having the VXI standard voltages and currents.

Three classes of output modules are available. The **STANDARD** outputs allow short duration surge currents on all auxiliaries for hard starting loads. Optional **CURRENT LIMITED** outputs have square current limiting and feature wireless droop current sharing. Optional **ENHANCED** outputs have square current limiting, one wire star point current share, output good logic signal with LED, nominal 5V local bias, individual inhibit and margining. For requirements that cannot provide minimum load on the main output, the **ZERO PRELOAD** option is available for main outputs up to 500 watts.

DELIVERY

Choose stocked units or construct a model number using stocked modules for fast delivery. Otherwise, form a model from the adjacent page to meet your specific requirements. Contact factory for deliveries on models derived from non-stocked modules.

FEATURES

- UL, CSA, TÜV (IEC, EN), CE.
- 6 watts per cubic inch.
- 1-7 outputs, 250-1500 watts.
- AC & DC input models.
- VXI rated specialty models.
- 120 kilohertz MOSFET design.
- All outputs:
  - *Adjustable*
  - *Fully regulated*
  - *Floating*
  - *Overload and short circuit protected*
  - *Overvoltage protected*
- Standard features include:
  - *System inhibit*
  - *Load proportional DC fan output*
- Options include:
  - *Auto ranger*
  - *VME/VXI Monitor*
  - *End fan cover*
  - *Top fan cover*
  - *Current Limited Outputs*
  - *Enhanced Outputs*
  - *Zero Preload*
- Fast delivery.
- Replaces expensive high density systems using potted modules.

STOCKED MODELS - Available in 3 days.

Max Power	Output 1	Output 2	Output 3	Output 4	Model*
425W	5V @ 50A	12V @ 12A	5V @ 10A	12V @ 6A	M44R2323-47P
425W	5V @ 50A	24V @ 6A	12V @ 6A	12V @ 6A	M44R2633-47P
600W	5V @ 60A	12V @ 12A	12V @ 12A	5V @ 10A	M46C2332-47P
600W	5V @ 60A	12V @ 12A	24V @ 6A	12V @ 6A	M46C2363-47P

**Models shown in table include power fail monitor, auto ranger, current limited modules, zero preload and end fan cover options. 600W models Case #3.*

UNITS FROM STOCKED MODULES - Available in 2 weeks.

M 44 B 2 3 3 6 – YY X

- M — Series
- 44 — Configuration
- B — Power Code
- 2 — Output #1 Code
- 3 — Output #2 Code
- 3 — Output #3 Code
- 6 — Output #4 Code
- YY — Sum of Option Codes
- X — Output #1 Variant

Configuration: Allowable quad output configurations are 42, 44, 46 and 48.
Power Code: Choose Power Code P, R, A through D for 250-750W models.
Output Codes: Select any outputs from the shaded area on the Output Types table consistent with the configuration chosen.
Option Code: Specify Option Code. Refer to the Option table. Codes 02 (redundancy) and 16 (enhanced) are excluded from models available in 2 weeks.

OPTIONS

Option Code	Function
00	None
01	Power Fail Monitor
02	Auto Ranger
04	Current Limited
08	Zero Preload
16	Enhanced
32	End Fan Cover*
64	Top Fan Cover

*Replace the YY with the sum of the option codes. *600 & 750 watt units require Case 5.*

MODEL SELECTION

Models are available in power ratings of 250 to 1500 watts, with corresponding code letters P, R and A through D. See Power Code chart. Contact factory for 1000 and 1500 watt models.

Output modules are available in six types—J, K, L, M, N and P in nominal power outputs from 75-500 watts. Type M, N and P modules are variable power rated depending upon the unit power rating. The M, N and P Module table directly below shows the corresponding multiplier applicable to the output current ratings of the M modules and allowable power ratings for the N and P modules. For example, a 750 watt multiple will have its M type module configured to produce 120A @ 5V or 12A @ 48V. The voltage and current rating of output modules are listed in the table of output types. This table assigns an alpha-numeric code designating the nominal voltage rating of the module.

Power Code	Unit Power Rating	M Module Current Multipliers Single Output	M Module Current Multipliers Multiple Output	N/P Module* Allowable Power Ratings
P	250W	0.5	0.3	175W
R	425W	0.85	0.5	250W
A	400W	0.8	0.6	250W
B	500W	1.0	0.8	300W
C	600W	1.2	1.0	400W
D	750W	1.5	1.2	500W

**When an N or P module is used as the main output, the allowable power and the module current ratings must not be exceeded.*

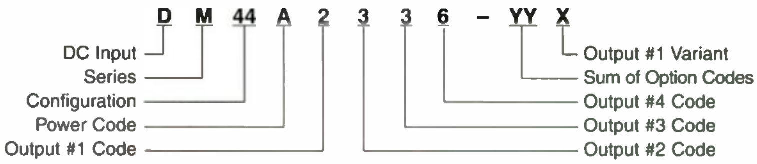
Output Types*						
Output Code	Output Volts	J Amps	K Amps	L Amps	M Amps	N/P Amps
0	2	10	20	30	100	60
1	3.3	10	20	30	100	60
2	5	10	20	30	100	60
3	12	6	12	24	42	42
4	15	5	10	20	33	33
5	18	4	8	16	28	28
6	24	3	6	12	21	21
7	28	2.5	5	10	18	18
8	36	2	4	8	14	14
9	48	1.5	3	6	10	10
A	2.2	10	20	30	100	60
B	2.4	10	20	30	100	60
C	2.7	10	20	30	100	60
D	3	10	20	30	100	60
E	3.6	10	20	30	100	60
F	4	10	20	30	100	60
G	4.5	10	20	30	100	60
H	5.7	10	20	30	90	60
J	6.3	10	20	30	80	60
K	7	9	18	30	70	60
L	8	8	16	30	62	60
M	9	8	15	30	56	56
N	10	7	14	30	50	50
P	11	7	13	27	45	45
Q	13.5	6	11	22	37	37
R	17	5	9	18	30	30
S	19	4	8	16	26	26
T	21	4	7	14	24	24
U	23	4	7	13	22	22
V	26	3	6	12	19	19
W	29	3	5	10	17	17
X	32	2	5	9	16	16
Y	40	2	4	8	13	13
Z	44	2	4	7	12	12

*Multiple output modules of a given type are arranged in ascending order by voltage magnitude in the same sense as the output number sequence in the configuration diagrams. *Shaded ratings are stock.*

HOW TO ORDER

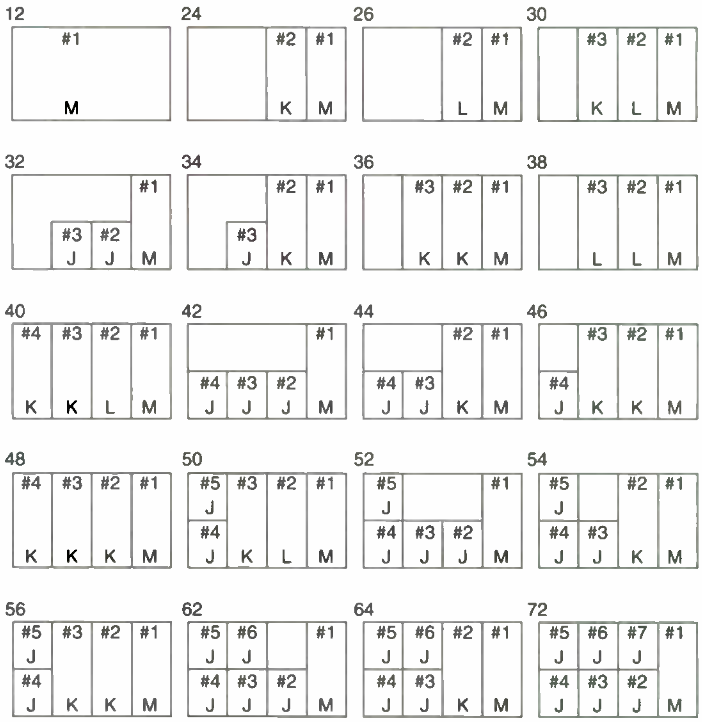
To form the proper model number defining a custom requirement, select the letters M or DM to designate the series, then choose the desired configuration of output modules and list the configuration code. Insert the power code letter for the power level and follow with the output code numbers or letters for each specific output. Enter a dash and from the option table insert the sum of the option codes. Where lower power is desired for the main module, an N module can be substituted and is denoted by a letter N in the output variant position. In addition, when no preload is available for the main output, choose Option Code 08 and add a P in the output variant position. For an **enhanced** main and **current limited** auxiliaries, specify both 04 and 16 option codes.

MODUFLEX 400W QUAD SWITCHER



OUTPUT CONFIGURATIONS

The boxes below are diagrammatic representations of the power supplies as viewed from the output end. The two-digit numbers above the boxes are the configuration codes.



Refer to the table below for allowable configurations by series.

Output Configuration	Unit Power Rating 250W	400W	425W	500W	600W	750W
12	x	• x	x	x	• x	x
24	x	• x	x	x	• x	x
26					• x	x
30					• x	x
32	x	• x	x	x	• x	x
34	x	• x	x	x	• x	x
36		• x	x	x	• x	x
38					• x	x
40						x
42	x	• x	x	x	• x	x
44		• x	x	x	• x	x
46		• x		x	• x	x
48		• x			• x	x
50						x
52		• x	x	x	• x	x
54		• x		x	• x	x
56		• x			• x	x
62		• x		x	• x	x
64		• x			• x	x
72		• x			• x	x

• Represents allowable configurations for the DM Series.
x Represents allowable configurations for the M Series.

SPECIFICATIONS

INPUT
90-132 VAC or 180-264 VAC, 47-63 Hz. Strappable. 40-60 VDC for DM Series.

EMISSIONS
FCC 20780 Part 15/EN 55022, Class A Conducted.
EN 61000-3-3, Voltage Fluctuations.

IMMUNITY
IEC 1000-4-2/EN 61000-4-2, Electrostatic Discharge. IEC 1000-4-3/EN 61000-4-3, Radiated Field. IEC 1000-4-4/EN 61000-4-4, Electrical Fast Transients. IEC 1000-4-5/EN 61000-4-5, Level 3 Surge. IEC 1000-4-6/EN 61000-4-6, Conducted Field.

INPUT SURGE
34 amps peak from cold start for units under 400 watts, 68 amps for other models.

EFFICIENCY
75% typical.

HOLDUP TIME
20 milliseconds after loss of nominal AC power. 3 milliseconds for DM Series.

OUTPUTS
See model selection table. Outputs are trim adjustable ±5%.

OUTPUT POLARITY
All outputs are floating from chassis and each other and can be referenced to each other or ground as required.

LINE REGULATION
Less than ±0.1% or ±5mV for input changes from nominal to min. or max. rated values.

LOAD REGULATION
±0.2% or ±10mV for load changes from 50% to 0% or 100% of max. rated values.

MINIMUM LOAD
Main output requires a 10% minimum load for full output from auxiliaries. Use Option 08 if no minimum load is available for mains up to 500 watts. Singles require no minimum load.

RIPPLE & NOISE
1% or 100 mV, pk.-pk., 20 MHz bandwidth.

OPERATING TEMPERATURE
0-70°C. Derate 2.5%/°C above 50°C.

COOLING
A min. of 6 LFS* for models under 400 watts, 10 LFS for others, directed over the unit for full rating. Two test locations on chassis rated for max. temperature of 90°C. For convection ratings consult factory.
*Linear feet/second.

TEMPERATURE COEFFICIENT
±0.02%/°C.

DYNAMIC RESPONSE
Peak transient less than ±2% or ±200 mV for step load change from 75% to 50% or 100% max. ratings.

RECOVERY TIME
Recovery within 1%. Main output - 200 microseconds. Auxiliary outputs - 500 microseconds.

SAFETY
Units meet UL 1950, CSA 22.2 No. 950, EN 60 950, IEC 950.

ISOLATION
Conforms to safety agency standards.

INPUT UNDERVOLTAGE
Protects against damage for undervoltage operation.

SOFT START
Units have soft start feature to protect critical components.

OVERVOLTAGE PROTECTION
Standard on all outputs. VX Series - standard on main output.

REVERSE VOLTAGE PROTECTION
All outputs are protected up to load ratings.

OVERLOAD & SHORT CIRCUIT
Outputs protected by duty cycle current foldback circuit with automatic recovery. Standard auxiliaries have additional backup fuse protection. Options 04 and 16 have square current limiting with automatic recovery when overload is removed.

THERMAL SHUTDOWN
Circuit cuts off supply in case of local over temperature. Units reset automatically when temperature returns to normal.

FAN OUTPUT
Nominal 12 VDC @ 12 watts maximum.

INHIBIT
TTL compatible system inhibit provided. Option 16 has individual output inhibit.

REMOTE SENSING
On all outputs except standard and 04 Option outputs 75 watts or less.

SHOCK & VIBRATION
Shock per MIL-STD 810-E Method 516.4, Procedure I. Vibration per MIL-STD 810-E Method 514.4, Category 1, Procedure I.

MECHANICAL

CASE	WATTS	H	x	W	x	L	
1	250W/425W	2.50"	x	4.15"	x	8.00"	
2	400W/500W	2.50"	x	5.05"	x	9.00"	
3	600W/750W	2.50"	x	5.20"	x	9.63"	
4	600W/750W	2.50"	x	6.50"	x	9.63"	Config. 40 & 50 only.
5	600W/750W	2.50"	x	6.00"	x	9.63"	Option 32 only.
6	1000W	5.00"	x	5.05"	x	10.40"	
7	1500W	5.00"	x	5.20"	x	11.00"	

OPTIONS

POWER FAIL MONITOR
Optional circuit provides isolated TTL and VME/VXI compatible ACFAIL signal providing 4 milliseconds warning before main output drops by 5% after an input failure. A SYSRESET signal following VME timing requirements is provided when an N module is used as a main output. Both logic signal outputs can sink current per the VME specification.

AUTO RANGER
Optional circuit provides automatic operation at specified input ranges without strapping. Not applicable to DM Series.

CURRENT LIMIT
Option provides on all outputs:
- Square current limit with auto recovery.
- Wireless droop current share for parallel or N+1 redundant operation.

ZERO PRELOAD
Optional circuit removes need for preload on main output. Available for mains up to 500 watts.

ENHANCED
Option provides on all outputs:
- Square current limit with auto recovery.
- Single wire active current share for parallel or N+1 redundant operation.
- DC output good logic signal with LED indicator.
- Logic inhibit.
- Nominal 5V bias.
- Margining.

END FAN COVER
Optional cover with brushless DC ball bearing end fan which provides the required air flow for full rating.

TOP FAN COVER
Same as above with fan mounted on top of the power supply.

Specifications subject to change without notice.

Deltron inc.
290 WISSAHICKON AVENUE, P.O. BOX 1369, NORTH WALES, PA 19454
PHONE: 215-699-9261 • FAX: 215-699-2310 • TOLL FREE: 1-800-523-2332
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about all the files related to software development projects.

The next step for SD/ToolSmith is a closer link to VHDL. Not far off is the ability to automatically generate RTL-type VHDL code from the full machine description. Another goal is reverse engineering VHDL to produce the information that can then be used to automatically produce tools for existing designs.

A future version will actually generate the machine description in VHDL, rather than the THISL code. Because the whole system is centered around an RTL-level representation of the architecture, this should be fairly straightforward.

Other goals include the growth of libraries of functional units such as ALUs, register files, and FPUs that can be represented at block diagrams. At that point, designing a custom processor would be a matter of drag-and-drop and wiring the icons together. Making whatever modifications needed for more detailed customization should be a matter of editing existing functional units.

The ability to simultaneously design a hardware processor and derive its instructions to automatically generate a suite of software development tools could change the economics of processor development. Presently, companies have to form alliances with tool developers or, at best, have separate teams working on the architecture and the tools. When the architecture team hits a snag and has to go back and redo part of the design, the tools team has to throw out part of its work and start over.

SD/ToolSmith and tools like it that may appear in the future, put the generation of the software tools into the hands of the chip designers. At the same time, such a capability makes small, low-volume designs that were previously economically prohibitive now feasible.

Price And Availability

SD/ToolSmith is available now. Pricing begins at $250,000 for a single-use stand-alone license. Multiple-use, multiple-user technology transfers, depending on complexity, will run five to six times the cost of a standalone single-use license.

Production Languages Corp., 403 West Loop 820, Suite 185, Fort Worth, TX 76108 (817) 367-6030. www.plcorp.com. CIRCLE 485

Designing The Next Step In Internet Appliances

Web-Enabled Information Appliances Are Showing Up In Many Places, But The Challenge Is Supplying Web Pages With Dynamic Content.

BILL PEISEL, Osicom Technologies Inc., 411 Waverley Oaks Rd., Bldg. 227, Waltham, MA 02154; (800) 243-2333; fax (781) 647-4474; e-mail: bpeisel@osicom.com.

As electronic devices evolve, they are becoming more intelligent and complex. In addition, the need for people to interact with them is becoming much greater. One obvious choice for person-device interaction is use of the ubiquitous web browser. More electronic devices are being designed today to be network accessible through a web browser. Such devices are often referred to as web-enabled information appliances or Internet appliances.

While benefits of merely web-enabling a device are large indeed, to fully tap the power of the Internet, the device capabilities must go beyond web enabling. For an Internet appliance to be practical and versatile, it must include a variety of hardware and software subsystems. Hardware subsystems must include a processor, an Ethernet controller, a memory and I/O controller, and support logic. Software subsystems, as a minimum, must include an RTOS, a web server (HTTP server), a TCP/IP protocol stack, and an e-mail and FTP server. Today's conventional design approaches dictate that the engineer choose and integrate these discrete hardware and software subsystems from a multitude of choices (and vendors) into an elegant, cost-effective solution.

Until now, such a conventional approach has been cost and time prohibitive for most engineers outside the computer industry. As recently as three years ago, web servers still ran only on high-end Alpha or Sun computers with massive disks. As a result, network-enabling was limited to people-centric applications—people connected to the Internet or Ethernet through computers.

Over the past few years, peripherals such as printers, faxes, and disk drives have been web-enabled, but the power of the Internet and Ethernet remains largely untapped by all devices that have anything to do with information, measurement, or control. Examples of such potential applications abound in a broad range of industries and consumer products; from digital video cameras and medical devices to industrial and building control systems.

Today's Web Devices

Recent advances in system-on-silicon technology promises to change all that. Embedded technology has evolved far enough to let web-servers run on single board computers with flash memory as their mass storage. Known as "thin servers" and "thin clients," embedded versions of web servers, such as Spyglass MicroServer, are now readily available. This shrinking of technology has allowed these smart devices, now embedded with a web server, to be accessible through a familiar web browser. Complete network connectivity system-on-silicon, such as the NET+ARM chip, can significantly reduce design time and lower the unit cost of network-enabling products. These compact, low-cost solutions will enable engineers, even from noncomputer industries, to quickly transform their products into fully functional Internet appliances.

With the rapidly increasing popularity of the World Wide Web, embedded systems designers are discovering the advantages of enabling their devices to work on the web. One typical application is to allow the device to be configured using a web browser. Another application is the addition of status reporting by the device utilizing web content. Web content is defined as Hypertext Markup Language (HTML) pages images and applets sent by the device in response to Hypertext Transport Protocol (HTTP) requests from web browsers.

Use of Internet technology doesn't have to stop with mere web-enabling. As we shall discuss shortly in two example applications, for these devices to be practical, they need to handle messaging, data transfer, and diagnostics.

Messaging can be implemented using Internet e-mail protocols such as standard SMTP and POP3. Reliable and error-free data transfer is easy to implement using standard

Web-enabled internet appliances can be easily controlled from a standard web browser. As this HTML page from a printer illustrates, the user can setup the printer, view its status, get help, and order supplies.

FTP, which can be used to either upload periodic measurement data to a specified host or download software for revision updates. The diagnostics are usually part of a user application software, which, for example, may monitor temperature, pressure, or flow in measuring devices or status such as "paper jam" in a printer. The alerts generated from the diagnostic program use messaging to inform people, and data transfer capability can upload files containing error logs for further analyses.

A Code Example

Step 1: Design desired HTML page(s) using an HTML editor of choice. This particular example was generated by hand using a text editor. The following page is stored in a file named testpage1.htm.

```
<HTML><BODY>
<H1>NET+ARM Test Page</H1>
This HTML page contains both static and dynamic content as well as a form for the end user to fill in.<BR>
Unit Configuration Information<BR>
IP Address: _NZZA_IP_ADDRESS<BR>
Change Unit Configuration<BR>
<FORM ACTION="ip_config" METHOD="POST">
Enter IP Address <input type=text size=12 maxlength=12 name="ip_address"><BR>
<input type=submit name="Submit" value="Submit">
</FORM>
</BODY></HTML>
```

Step 2: Use an HTML conversion tool, supplied by Osicom or some other vendor, to generate embedded application source code. The code in this example is written in C.

Contents of testpage1.c:

```
void
IP_ADDRESS (unsigned long handle)
{
}
void
ip_config (unsigned long handle)
{
}
void
Send_testpage1 (unsigned long handle)
{
 /* Static portion of the page displayed as is. */
   HSSend (handle, "<HTML><BODY>\n");
   HSSend (handle, "<H1>NET+ARM Test Page</H1>\n");
   HSSend (handle, "This HTML page contains both static and dynamic content as well as a form for ");
   HSSend (handle, "the end user to fill in.<BR>\n");
   HSSend (handle, "Unit Configuration Information<BR>\n");
   HSSend (handle, "IP Address: ");
   /* Dynamic portion handled by IP_ADDRESS shell routine. */
   IP_ADDRESS (handle);

  /* Forms portion of HTML page. */

   HSSend (handle, "Change Unit Configuration<BR>\n");
   HSSend (handle, "<FORM ACTION=\"ip_config\" METHOD=\"POST\">\n");
   HSSend (handle,  "Enter IP Address <input type=text size=12 maxlength=12
      name=\"ip_address\"><BR>\n");
   HSSend (handle, "<input type=submit name=\"Submit\"
      value=\"Submit\"></FORM></BODY></HTML>\n");
}
```

Step 3: Implement the body of the IP_ADDRESS and ip_config routines.

```
void
IP_ADDRESS (unsigned long handle)
{
   char buffer[256];
   sprintf (buffer, "%d.%d.%d.%d", 199, 92, 187, 10);
   HSSend (handle, buffer);
}
void
ip_config (unsigned long handle)
{
   char buffer[256];
   char ipaddrbuffer[32];
/* Use NET+ARM HTTP Server API routine to retrieve value of "ip_address" submitted by end user. */
   HSGetValue (handle, "ip_address", ipaddrbuffer, 32);
  /* Reply to browser user. */
sprintf (buffer, "IP Address changed to %s", ip_address);
HSSend (handle, buffer);
}
```

The requesting user sees "IP Address changed to 199.92.187.22" on the screen after submitting the form from testpag1 with "199.92.187.22" entered into the text field. By utilizing the conversion tool NET+ARM customers only spend their time implementing the web portions specific to their device. This results in a very large time savings in their application development time.

Before we examine the designing of an Internet appliance, let us look at two application examples that show the dramatic benefits that are possible when a device is transformed into an Internet appliance.

Today, most printers can be connected to Ethernet or the Internet as a shared resource. A long-time problem for customers and vendors is the difficulty of installation and configuration for network printing. Each vendor provides proprietary software which runs on some but not all platforms. Furthermore, each vendor's graphical-user interface (GUI) has a different look and feel, making it difficult for one person to use products from multiple vendors.

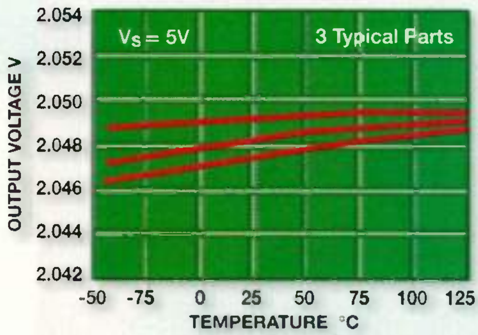
One solution is to embed an HTTP server in the printer. This enables HTML screens to display information that can be viewed through a browser. The user benefit: the GUI now becomes a familiar web-browser, which enables the user to interact with a printer remotely. The vendor benefit: the GUI needs to be written only once for it to work on all platforms. Shown is an example of a typical HTML page from a printer *(see the figure)*.

Now that the printer is web-accessible, some of the parameters that can be set or viewed include printer IP address; default gateway; subnet address; AppleTalk name and zone; Novell printer server name, which directory services tree to attach to; which paper tray to use; type of paper; amount of toner; number of pages printed; and printer status, such as ready, in-use, or paper-jam. All these parameters can now be accessible to any authorized person across the network.

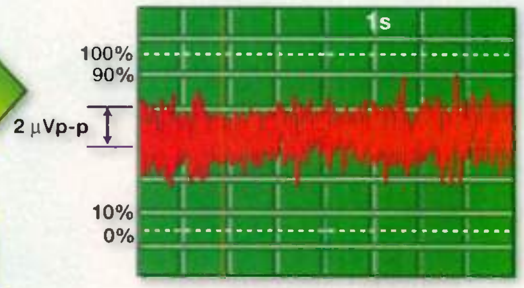
Adding messaging or e-mail capability can further extend the functionality of the shared printer. For example, when the toner is low, the printer can send an e-mail message directly to the supplier to deliver the toner cartridge. By adding diagnostic capability, the printer can now alert the office manager whenever there is "paper jam" through an e-mail. Finally, data transfer capability such as FTP can allow vendors to download firmware upgrades and bug fixes directly to the printer.

Let's look at a hypothetical design of a flow meter used to monitor the amount of a substance moving through it. It needs to record the flow at various

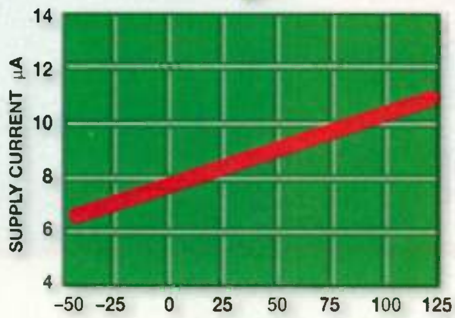
The Low Power Of Bandgap And High Accuracy Of Buried Zener, All From One Point Of Reference.



Vout vs. Temperature



0.1 Hz to 10 Hz Noise



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256K x 18 flow-through	7.5, 8, 8.5, 10	117 MHz
128K x 36 flow-through	7.5, 8, 8.5, 10	117 MHz

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READER SERVICE 121

Lucent Digital Cellular Telephone 6720

Centurion International has developed antennas for many Lucent Technologies Inc. wireless terminals which meet Bell Labs specifications.

times and send an alert to intended recipients when the flow is "too high" or "too low." By network-enabling the meter, some of the parameters that can be configured remotely during the installation using a browser are:

- Low Flow-Level Alarm Limit;
- High Flow-Level Alarm Limit;
- Who to notify in case of failure;
- How often to record flow amount;
- Where to store flow data.

With an embedded FTP server, the meter can transfer the flow data to a specified file on a specified computer. An outbound SMTP e-mail server can send an alert to any number of recipients that can be specified depending on the nature of the alert. The message also can be sent to any specified mailbox, including a pager. Having received an alert, the service technician can remotely log into the meter using its IP address, run additional diagnostics, and even reconfigure the meter or download new firmware to resolve the problem without ever leaving his office. What these two examples point out is that the possibilities are limited only by the imagination of the design engineer!

Design Challenges

Although embedded technologies are making web-enabled devices much easier to design, several challenges still remain. One of the most serious is supporting dynamic web content on a ROM-based system.

To incorporate web content into an embedded device, an HTTP server is first incorporated into the device. This server processes HTTP requests and responds with web content. The next challenge is to incorporate the actual web content into the HTTP server.

Commercial web servers operating on Unix or Windows NT platforms have large file systems stored on disks which make incorporating web content fairly straight forward since various pages and images can be added to a known directory that then makes the web accessible. Embedded devices usually only have read only memory (ROM) with no file system. The web content in this case has to be incorporated directly into the embedded device application stored in ROM. There are various approaches to incorporating web content into the embedded source code.

Someone proficient in writing HTML by hand can develop HTML pages by adding various HTML markup tags along with text content in a text editor. These same pages can then be incorporated into an embedded device by writing application code to physically send back the HTML page. The page is stored in a large character buffer in the device and is sent back utilizing a network application programming interface such as sockets.

This approach has the following limitations. The tools for generating HTML pages have advanced to the level that web masters do not generate HTML pages by hand because using a tool is much more efficient and removes a significant amount of the tedium involved in working with the markup tags.

Static HTML pages, those whose content never changes, is only a small part of the possible web content provided by a web server. Dynamic content, whereby the web content changes over time is common place and necessary for status reporting. Forms processing, accepting user input and acting on it, also is commonplace and necessary to make configuration changes in an embedded device. An HTML generation tool does not solve the problem of providing dynamic content or forms processing. Application code in the commercial web server (written in Perl, C++, or Java) is necessary for both of these types of web content.

The problem then for embedded devices is how to incorporate static content, dynamic content, and forms processing into the embedded HTTP server source code. The solution to this problem parallels that taken for commercial web servers. Embedded system designers are writing conversion tools that automatically convert web content into application source code. Static pages are converted into the necessary program calls to send back the HTML, image and applet content that does not change over time. For dynamic content, proprietary non-HTML markup tags are inserted into the HTML source using an HTML editor. The conversion tool recognizes these tags and produces shell routines and calls to the routines in the application source code.

The embedded designer is then responsible for implementing the routine such that the appropriate dynamic content is returned when the routine is called. The conversion tool also recognizes HTML forms and adds then necessary shell routines to be called when forms data is sent back to the embedded web server.

The embedded web server typically has an application programming interface which makes it easy to retrieve the Common Gateway Interface data supplied by the browser in response to a forms submission. The embedded designer is responsible for filling in the shell routine with the code necessary to handle the data and send back the appropriate reply.

By utilizing a conversion tool the process for incorporating web content into an embedded device is reduced to the following set of steps.

1. Generate web content using an HTML editor of choice. For dynamic content pages, proprietary tags are inserted where the dynamic portions are to appear.
2. Use a conversion tool to convert the HTML pages, images, and applets into embedded application source code.
3. Implement the generated shell routines that are specific to the overall application running in the embedded device.
4. Compile and link the resulting source code.

The embedded device can now serve web content that is static and dynamic. In addition, the embedded device also can process forms data returned in response to end user submissions.

The following example illustrates the first three steps in the above process for Osicom's NET+ARM product *(see "A Code Example," p. 52)*. Along with firmware to support an e-mail and FTP server, it comes bundled with an embedded HTTP server, and an application programming interface (API) into the HTTP server. This is a conversion tool that converts HTML pages, images and applets into source code. The basic techniques however, may be easily adapted to the development of any platform with similar capabilities.

Bill Peisel is the vice president of Engineering, Embedded Networking Solutions Division of Osicom Inc., Waltham, Mass. He holds a BSEE from Pratt Institute, and an MSEE from Northwestern University.

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CONFERENCE PREVIEW

Embedded Systems Conference Covers A Wide Perspective

Comprehensive Technical Program Explores The Use Of PC Technology And The Internet, And Techniques For Better Project Management.

Lisa Maliniak

These days, embedded systems developers need to take a step back and look at the big picture. Team-based product development is forcing engineers and embedded programmers to broaden their knowledge beyond very specific technical issues.

With that in mind the Embedded Systems Conference Spring offers the opportunity for professionals at all levels to focus on important technologies and receive a solid grounding in the broader issues, including software-hardware integration, management, and testing.

The sixth annual Embedded Systems Conference Spring is being held for the first time at Chicago, Ill.'s Navy Pier. The show features 87 classes and tutorials on a wide range of topics that include new adaptations of PC technology for embedded systems, building in web functionality, project management, and design-for-test methodologies.

Running from March 31-April 2, the conference brings together 67 industry experts and over 170 exhibitors to the biggest embedded-systems event held outside of California's Silicon Valley. Vendors on the exhibition floor will showcase their hardware, software, and services for embedded applications.

The conference opens with a day of tutorials on Tuesday, Mar. 31. Seven full-day sessions offer in-depth instruction on topics such as real-time performance, programming languages, and fuzzy logic for automotive applications.

Other conference tutorials include an overview of embedded controller area networking (CAN), which provides low-cost, reliable, fast communications in automotive and industrial applications, and an introduction to digital-signal-processing (DSP) theory and practice.

On Wednesday and Thursday (April 1 and 2), the conference features 80 technical classes presented by top engineers and researchers. The conference's program includes popular classes from previous programs as well as 39 new classes.

In addition to the conference's tutorials and classes, each conference day begins with "Birds of a Feather" discussion groups, where attendees meet for breakfast and share their opinions on current trends and experiences with specific projects. Other conference events include a keynote speech by consultant and author Jack Ganssle on the future of embedded systems development.

On Wednesday evening, a special guest lecture will be conducted by Hewlett-Packard's Ned Barnholt. He'll talk about the consumerization of digital systems.

Embedded PC Technology

A variety of classes address the latest adaptation of PC technology for use in embedded systems. These include discussions on CompactPCI architecture, Universal Serial Bus (USB), and off-the-shelf BIOS for use in embedded applications. New for this year is a two-part class called "CompactPCI and telecom applications." The class explores the cPCI architecture in depth to see if it can live up to its on-paper potential in the field of communications. Interface products, operating systems, driver-level support, and packaging options will all be discussed.

Four classes address USB in embedded applications. Two of those classes dissect USB from the device and host side, respectively. "Understanding USB: device-side issues" provides an overview of USB from a device standpoint, with an emphasis on the software issues that must be understood when dealing with the protocol. The class covers topology, communications flow, and enumeration process. "Understanding USB: host-side issues" will teach designers how an embedded device interacts with the USB host. Topics include host-controller interfaces, the new Windows Driver Model, and the USB System Driver.

"Adapting off-the-shelf BIOS for embedded systems" is a new class that will focus on issues involved in using a PC-style BIOS as the firmware for an embedded x86 platform. It will highlight the difference between a standard BIOS and the embedded variety. Attendees also will learn about the available I/O methods for headless systems.

Software topics at the show cover C and C++, Windows CE, Java, and real-time kernels. There's a class on writing efficient code for small microcontrollers, and eight different classes are offered on Java and Internet-related topics. These include "Implementing web-based management of networked devices" and "Java CPU for emerging Internet appliances."

Evaluating C++

The class to consider if you're unsure about C++ is "How to evaluate C++ as a language for embedded programming." As a superset of the C language, C++ offers additional support for large-scale software development without sacrificing C's ability to stay close to the hardware. Therefore, it seems like a natural choice for programming embedded systems. Unfortunately, many potential users are wary of the complexity and frequent hidden costs of C++. This class separates the real problems from the imagined ones, and describes methods for adopting C++ that reduce risk. Rather than tell developers that C++ is the right choice for their application, this class provides the information to

Embedded Systems Conference Spring Technical Program

Tutorials
Tuesday, Mar. 31
8:30 A. M. - 5:30 P.M.

101 Stepping up to C++
102 Fuzzy logic and neurofuzzy applications in automotive engineering
103 Guaranteeing real-time performance using RMA
104 Java for C++ programmers
105 Real-time unified modeling language
106 Introduction to DSP theory and practice
107 Embedded controller area networking (CAN)

Classes
Wednesday Apr. 1
8:30-10:30 A.M.

211 Implementing web-based management of networked devices
212 Starting your project with a great plan
213 Real-time development with the Shlaer-Mellor method, Part 1
214 Commercial support for embedded C++
215 Incorporating Windows CE into an embedded system from start to finish
216 Developing device drivers in a hardware/software co-simulation environment
217 Designing small-scale embedded systems with the mITRON kernel
218 CompactPCI and telecom applications, Part 1
219 The How-to's of flash: Implementing downloadable firmware, Part 1
220 Writing PERC programs for embedded real-time applications

10:30 A.M. - 12:00 noon

221 How to evaluate C++ as a language for embedded programming
222 Mixed C and Java in embedded systems
223 Real-time development with the Shlaer-Mellon method, Part 1
224 Fuzzy logic
225 Real-time design patterns
226 Writing efficient programs for the Motorola M.Core architecture
227 Bring the web to the world: Adding web functionality to almost anything
228 CompactPCI and telecom applications, Part 2
229 The how-to's of flash: Implementing downloadable firmware, Part 2
230 Writing PERC programs for embedded real-time applications, Part 2

2:00-3:30 P.M.

231 Manipulating hardware in C and C++
232 Adopting programming conventions
233 Analysis patterns speed time-to-market
234 Advanced DSP architectures
235 Safety-critical systems
236 Microprocessors for consumer electronics, PDAs and communications
237 Understanding USB: device-side issues
238 Debugging interrupts
239 Embedding an ARM RISC core into a complex ASIC
240 A V6 under the hood: 1Pv6 technology for embedded platforms, Part 1

4:00-5:30 P.M.

241 Reducing run-time overhead in C++ programs
242 DSP lifecycle software development issues
243 Applying a contamination model to testing an embedded system
244 Fuzzy logic in automotive engineering
245 Windows CE in embedded applications
246 Writing efficient code for small microcontrollers
247 Understanding USB: host-side issues
248 Adding off-the-shelf BIOS for embedded systems
249 Internet technologies for embedded systems
250 A V6 under the hood: 1Pv6 technology for embedded platforms, Part 2

Classes
Thursday Apr. 2
8:30-10:00 A.M.

311 Multitasking design and implementation issues in embedded systems, Part 1
312 Embedded software development using high-powered DSPs
313 Designing user interface software for embedded systems
314 Fuzzy logic and neurofuzzy applications in industrial automation
315 Scalable kernels: Deign techniques and issues
316 Java for real-time systems: The treads that bind
317 Build or buy? Decisions in selecting bus bridges for embedded systems
318 Real-time characteristics of Windows CE
319 Trends in debugging technology
320 Software tool planning in an ever-changing world

10:30 A.M.-12:00 noon

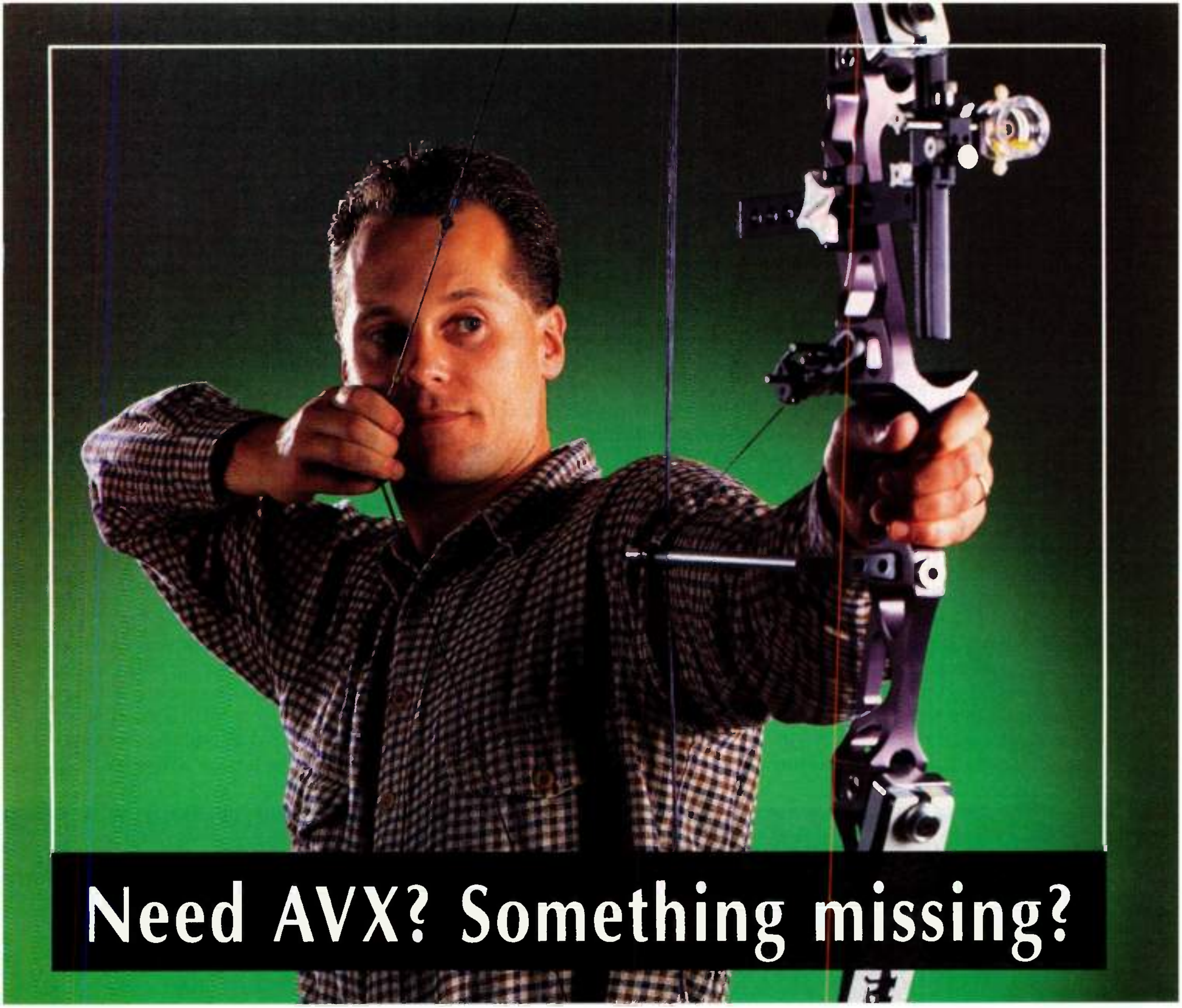
321 Multitasking design and implementation issues in embedded systems, Part 1
322 Statistical approaches to testing software
323 Calculus by the numbers
324 Fuzzy logic and neurofuzzy technologies in appliances
325 State machines and state charts, Part 1
326 Java CPU for emerging Internet appliances
327 Flash memory technology and techniques
328 Implementing secure communication protocols for embedded systems
329 Integration of SDL and UML for real-time applications
330 Software strategies for Hot Swap CompactPCI

2:00-3:30 P.M.

331 RTOS design: How your application is affected, Part 1
332 Inside real-time kernels
333 The alphabet from S to Z, Part 1
334 USB-based microcontrollers in telecom peripherals for PCs, Part 1
335 State machines and state charts, Part 2
336 Conquering common problems encoutered in debugging 683xx systems
337 Developing with embedded Java
338 Integrated debugging of multiple cores on a single die
339 Managing outsourced embedded systems development
340 Evaluation criteria for designing an ATM and frame relay communications product, Part 1

4:00-5:30 P.M.

341 RTOS design: How your application is affected, Part 2
342 Designing real-time kernels
343 The alphabet from S to Z, Part 2
344 USB-based microcontrollers in telecom peripherals for PCs, Part 2
345 Hardware/software tradeoffs in microcontroller-based system design
346 Real-time trace in the 32-bit embedded RISC market
347 Web interface development for embedded systems
348 Using C++ efficiently in embedded applications
349 Controlling radio-frequency inter-fer ence and electromagnetic radiation in pc-board designs
350 Evaluation criteria for designing an ATM and frame relay communications product, Part 2



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help them make the decision.

No matter what programming language is chosen, upcoming embedded applications are likely to have a graphical-user interface (GUI) based on HTML and Java. Designers must avoid proprietary solutions and face the challenge of creating advanced applications that meet open standards. "Mixing C and Java in embedded systems" is a class that describes how to add an HTML and Java-based GUI to an embedded applications written in C or C++. This class reviews the required system software, network protocols, and data formats. Attendees also will learn the general software-development methodology, including communication between the applets and the rest of the embedded application. Developers should come away from the class knowing how to build powerful GUIs in Java without requiring a Java virtual machine as part of their embedded software.

"Implementing web-based management of networked devices" will instruct designers on how to use existing web browsers to interface to a network. Network devices typically use the Simple Network Management Protocol (SNMP) for management, monitoring, and control. But SNMP has limitations and imposes certain development requirements that are not always practical to implement. Designers should capitalize on the robustness of web browsers such as Netscape Navigator and Internet Explorer that can provide a graphical interface to a network product without having to implement a client.

Designers attending "Java CPU for emerging Internet appliances" will learn the ins and outs of the microJava-501 embedded processor that's intended to implement the Java paradigm in hardware. The microprocessor is designed to accelerate Java code, and is tailored for network appliances, Internet TV, and kiosks running in the Java environment. This class will describe each functional block on the chip, and will include application examples.

Another Internet-related class is "Bring the web to the world: adding web functionality to almost anything." Consumer electronics manufacturers are ramping up to embed web accessibility into their devices. But simple connectivity is not enough—devices need to truly leverage the vast array of information that exists online. Televisions and games consoles can run thin browsers that function much like their larger PC-based forerunners, but solutions also must be in place for devices with limited memory and storage, such as pagers, phones, and some PDAs. This class lays out the various options open to add web functionality to any embedded systems product.

Ideas For Management

For project managers and team members who are expected to understand management issues, there are classes on creating project plans, managing outsourced systems development, and implementing programming conventions. One such class is "Starting your project with a great plan." This new class will explain how to modify an existing process, giving control of the product-development methodology to project teams. Using a case study of an embedded-product development organization, attendees will learn to separate what they need to do when developing an embedded product (procedures) from how they should do it (the development plan). The methods described will improve any team's organization and ease SEI or ISO 9000 audit anxiety.

Many companies are now outsourcing part or all of their embedded-systems design and development. "Managing outsourced embedded systems development" will explore the reasons behind outsourcing, its potential drawbacks, selection criteria, working with the outsourced developers, and strategies for making the outsourced project a success. The steps in developing a project—proposal, requirements definition, analysis and design implementation, and testing—will be examined in detail.

Many attendees will find "Adopting programming conventions" a useful class. Enormous productivity gains can be had by having a project team or corporation adopt common and consistent programming conventions. This class shows techniques for organizing project directories, naming files, laying out code, naming variables, and more.

Fuzzy Logic Picks Up Speed

Fuzzy logic is picking up speed in embedded applications. It's the subject of no less than four classes at the show. An interesting new class, simply called "Fuzzy logic," demonstrates the implementation of fuzzy logic in an embedded control system using the Philips XA microcontroller. Most control applications involve the specifications of a relationship between sensor signals and actuator outputs. Fuzzy logic lets designers use linguistic rules to specify a nonlinear mapping between the two, thus providing a framework for programming an embedded system. Using a multi-joint robot system as a testbed, the class instructor shows how to implement fuzzy logic on the XA controller. The fuzzy-logic robot can carry out goal-oriented motor sequencing behavior.

Fuzzy logic also is the topic of "Fuzzy logic in automotive engineering." This class showcases the power of this technology, emphasizing how it can inject products with engineering expertise in a very short time. Design methodologies, tools, and code speed/size requirements are discussed using three case studies that focus on automotive applications.

The first case study shows how fuzzy logic and conventional design techniques can complement each other in anti-lock braking systems. The second case looks at an engine-control system and the engineering process of building a fuzzy logic system. Lastly, the class will examine the design of an automatic gearbox control. This case study gives an outlook into future user-adaptive systems and confirms that fuzzy logic is an enabling technology.

For more information about the Embedded Systems Conference Spring, call (800) 789-2223 or (817) 255-8050; or inquire on the Internet at www.embedded.com (click on Embedded Systems Conferences).

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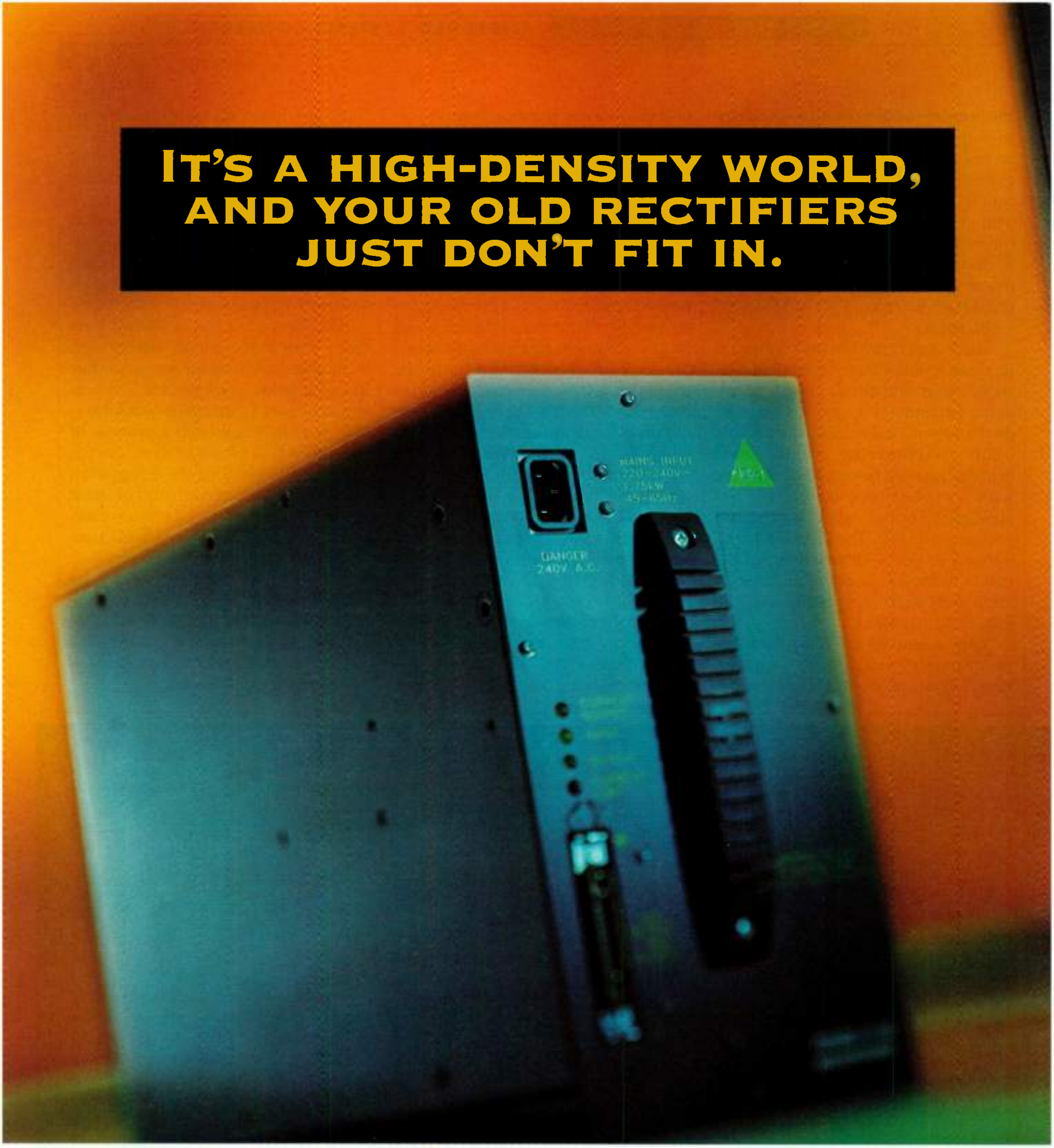

It seems that everything about telecommunications is growing—including the power that systems require and, unfortunately, the space they take up.

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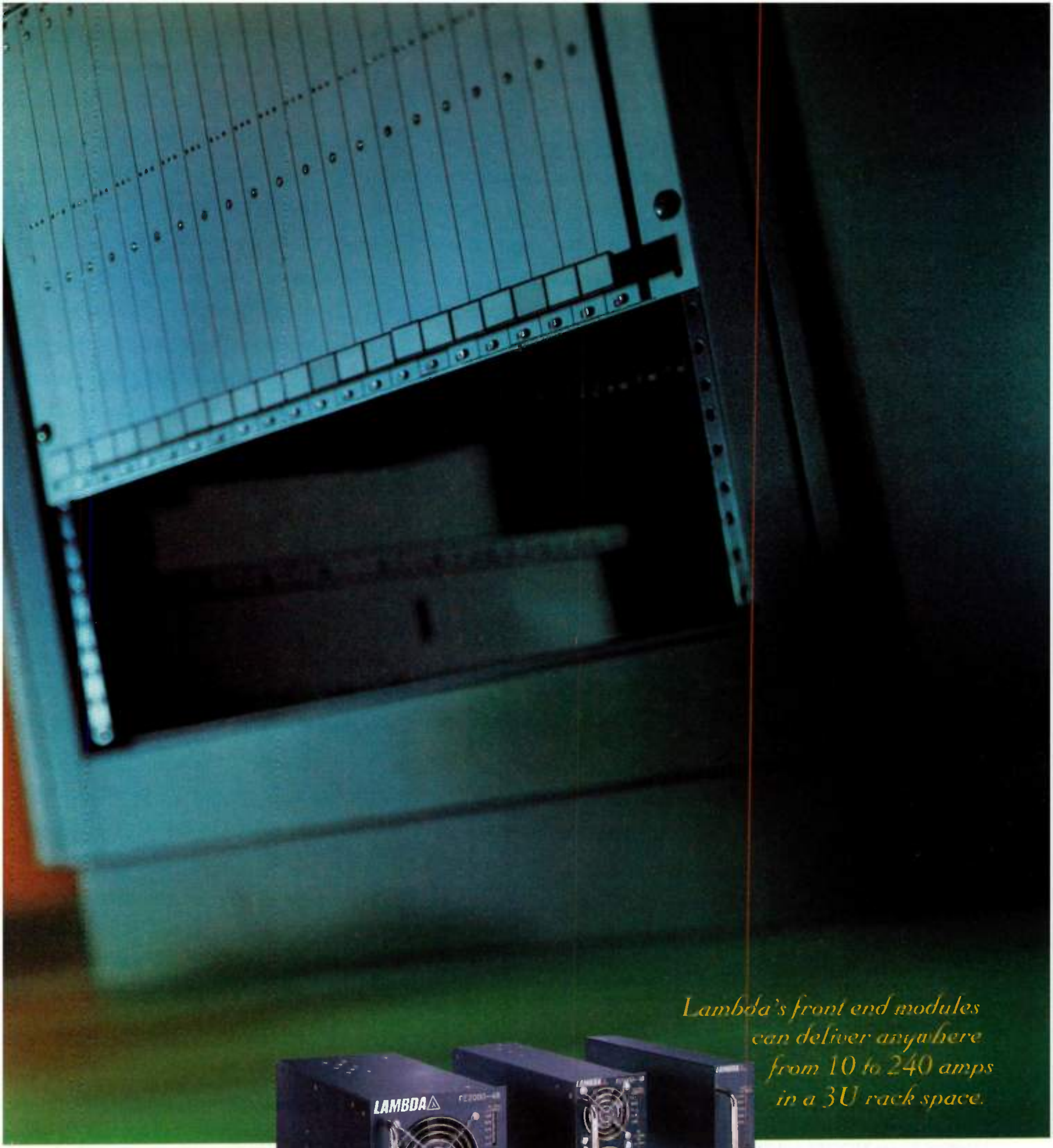

factor correction and remote diagnostics. Both 24 and 48 volt output versions are available.

There are plenty of other reasons why the FE Series may be the right solution for your application. But you'll just have to give us a call at 1-800-LAMBDA-4, ext. 8828, because, once again, space is limited.

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READER SERVICE 177

ELECTRONIC DESIGN QUICK LOOK

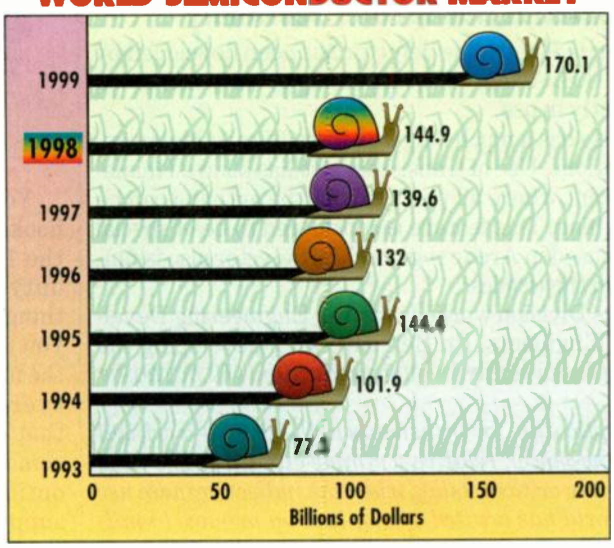
■ Edited by Debra Schiff

MARKET FACTS

Very Slow Growth Ahead For Semiconductors In 1998

It may seem to be obvious to most, but the Asian financial crisis is going to hurt the 1998 semiconductor industry a lot harder than originally thought. Other factors, according to a new report from Pathfinder Research, "1998—On The Cusp," include excess capacity, rapidly falling costs, and weaker end markets. Pathfinder does not like having to say it, but its prediction for the year is that the market will be flat. In fact, the company is pegging the semiconductor market's growth at only 3.8% in 1998. That number pans out to $144.9 billion in revenues, as compared to 1997's $139.6 billion in revenues and 5.8% growth. Within the semiconductor market, says Pathfinder, there has been a wide discrepancy in growth. From 1996 to 1997, the MPC and MPR segments grew at 29.2% and 20%, respectively. Meanwhile, the memory sector suffered with -15% growth. Logic only saw 7.5% growth during the same time period. In 1998, however, the new report says that will not be any dramatic growth from any sector. MCU, memory, MPR, and logic are expected to top out at 9.4%, 4.3%, 4.2%, and 4.2%, respectively. MPU semiconductors are projected to grow at a rate of 3.8% for 1998. One of the major contributors to this flat market is excess capacity. It begins with the giant investment companies have been making over the past year. According to Pathfinder, "when a $130 billion industry invests $45 billion a year, it is too much." But, the semiconductor industry has been doing this for the last three years! And, it's been showing up in the Asian markets because investment has not been keeping in line with revenues. Additionally, capacity has been greatly increased because output has been increasing steadily. How? Smaller chips. Smaller chips as a result of smaller dimensions and more metal layers. Also, with higher yields, greater throughput, and larger wafers, fab outfits have just been cranking out product at rates never seen before. Looking at the other side of high capacity, die costs are falling as rapidly. Sure, lower costs increase operating profits, but what they're really doing is lowering the overall price of the semiconductor. Memory, microperipherals, and FPLDs, especially, are suffering from this dilemma. There are two ways to go with low prices: rapid growth or sinking profits. We're seeing the latter. Another factor that the study examines is the end market. On the PC side, the market is so healthy that the $1000 PC is now wearing a $700 price tag. These are those same Pentiums that we bought when they first came out for nearly $2000. But, because the lion's share of the elements that make up our PCs come from Asian markets (things like monitors, storage, DRAMs, you name it), prices could be dropping even further with buyouts and other drastic measures. In terms of the semiconductor market, the PC has a great impact. The less expensive the PC, the lower the semiconductor content. "A $2500 PC might have 40% chip content, or $1000. A $1000 PC might have 30% chip content, or $300," says the report. Therefore, if OEMS only put low-priced chips into low-cost models, the semiconductor market will see a dip. On the hopeful end, data communications is still a sunny market for chips. It is a slower market than in the past, but competition is increasing between companies. As that market matures, however, semiconductor companies design their chips especially for the networks. In the DRAM market, exploding production and the Asian financial crisis have led to a fight for revenues. In the meantime, DRAM manufacturers are making other products.

WORLD SEMICONDUCTOR MARKET

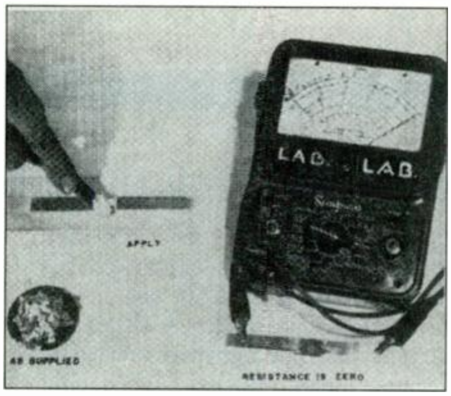


Contact Pathfinder Research, 1620 Old Oakland Rd., D-207, San Jose, CA 95131; (408) 437-1905; fax (408) 437-8929; e-mail: editor@pathfinder-research.com.—DS

40 YEARS AGO IN ELECTRONIC DESIGN

Conductive Adhesive

These conductive adhesives are epoxide-based materials which are supplied in paste form, and can be cured rapidly at moderate temperatures to produce rigid, low-electrical-resistance solids. They can be used where soldering is impractical due to heat or because solder will not wet and adhere to conductive plastics or nichrome wire. Adhesion is excellent to metals, plastics, glass, and ceramics. Bond strength is about 2000 psi. Conductivity of resultant compositions compares with that of metals. No solvent is present. Once cured, they can be used from - 65° to 500° F.



The adhesives, trademarked Eccobond, are as follows: Type 56 C is a two-component paste, cured at 120° F, with a volume resistivity of 0.1 ohm/cm; Type 58 C is one component, cured at 300° F, with the same resistance; Type 60 L is a two-component paste, cured at room temperature, with resistance of about 300 ohms/cm. Emerson & Cuming, Inc., 869 Washington St., Canton, Mass. *(ELECTRONIC DESIGN, March 19, 1958, p. 95)*

Conductive-epoxy technology is still going strong (no pun intended). You might also note the ohmmeter in the photo—it's the 1950's version of an all-time favorite lab instrument, the Simpson Multimeter. —Steve Scrupski

Transistorized Land Mine Detector Has Greater Sensitivity

A new light-weight, transistorized land mine detector has been developed by Texas Instruments Inc. for the U.S. Army, with reportedly greatly increased sensitivity over detectors currently in use.

The transistorized detector also has a much longer battery life and higher reliability under rugged field conditions. Use of transistors also has allowed miniaturization of the device to the point where all parts except the antenna can be carried under the operator's clothing. This feature is considered to be of special importance when the detector is used in Arctic regions. The detector also is fungus proof for advantageous use in the tropics.

Texas Instruments' Apparatus Division worked with the Engineering Development Laboratories, Corps of Engineers, Ft. Belvoir, Va., in developing the transistorized detector. The unit is currently in pilot production. (*ELECTRONIC DESIGN, March 19, 1958, p. 13*)

This was an ideal military application for transistors in the 1950s—a critical need that could be satisfied by low-power, relatively simple circuitry. The need for devices like this one is even more critical today, when the indiscriminate use of land mines throughout the world has created a long-lasting menace to millions of civilians.—Steve Scrupski

New Literature: How To Ruin Transistors

Information on how NOT to use transistors is contained in a new type of "how-to-do-it" booklet. A dozen ridiculous cartoons can help rush you through the coffee break. General Transistor Corp., 91-27 138th Pl., Jamaica, N.Y. (*ELECTRONIC DESIGN, March 5, 1958, p. 165*)

Sometimes the most effective instructional technique is to dramatize the effects of doing things incorrectly—and it's even better if you can do it with humor. I could be wrong, but it seems that back in the '50s and '60s, there was a lot more engineering humor floating around. —Steve Scrupski

Steve Scrupski is a former Editor-in-Chief of ELECTRONIC DESIGN. Now semiretired, he can be reached at scrupski@worldnet.att.net.

HOT PC PRODUCT

Wouldn't it be helpful if we could communicate directly with our vehicles, instead of having to go to a mechanic to have them checked out diagnostically first? An exciting new development from B&B Electronics, the Model 232SAER interface adapter, works with both desktop and laptop PCs to communicate with heavy-duty vehicle on-board diagnostic systems *(see below)*. It works by converting the SAE J1708 specification for serial communications between computer diagnostic systems in heavy-duty vehicle applications to the RS-232 specification so that your PC can read it.

Let's say you own a very big truck. You're already running late, spilling your morning beverage on your coat as you hastily climb into the truck. The thing won't start. Not only will it not start, but it won't even turn over.

You dig out your 232SAER and hook your laptop up to the truck via the 1708CAB tinned-ended heavy-duty cable, trying not to curse the thing that will get you to work, take you to the grocery store, and out to the movies later on. Your PC picks up over 20 categories of possibilities that could be causing your truck to remain unanimated. Taking out the optional 120-V ac to 12-V dc power supply (because you know you'll be there a while), you work your way through the categories until you find the reason for the problem.

The RS-232 side of the converter is DB-25 female, and configured as a DCE device. The 232SAER is priced at $59.95, the power converter is priced at $14.95, and the 1708CAB is priced at $49.95.

Contact B&B Electronics, 707 Dayton Rd., P.O. Box 1040, Ottawa, IL 61360; (815)433-5100; fax (815) 434-7094; www.bb-elec.com.—**DS**

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* Source: Dataquest 1997

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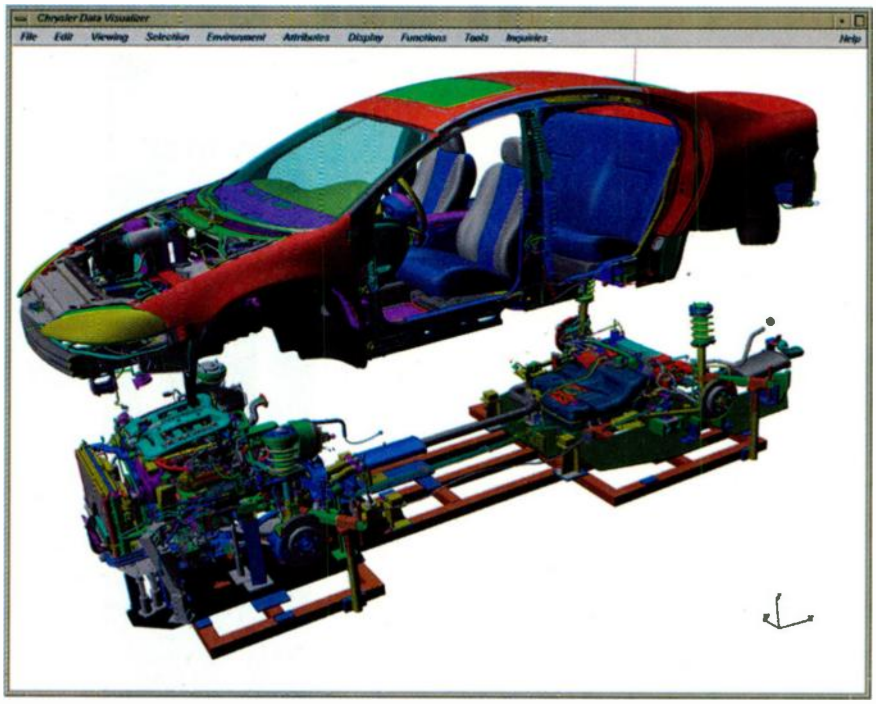
THE WORLD LEADER IN DSP SOLUTIONS

TEXAS INSTRUMENTS

First A Paperless Society, Now Paperless Cars

If you've ever thought that buying a car was difficult, try designing one. Granted, things have gotten a little easier since the days of Henry Ford, especially in light of the latest CAD tools, but at the same time, with the number of different car, van, and truck platforms coming out each year, the design process has become increasingly more complex. One potential solution that has already been put to the test is a new way of designing automobiles that is being called a "paperless car" design.

What Chrysler, one of the "big three" automakers, has been able to do is devise a method for designing cars that virtually eliminates the need for a paper trail. It incorporates Silicon Graphics workstations, Dassault Systemes CATIA software, and Chrysler's own Data Visualizer (CDV) software and digital prototyping technology known as digital model assembly (DMA). Cars in the Data Visualizer design process are shown below and above right and left. Key to the success of such a methodology was finding a graphics engine powerful enough to generate interactive images, with multiple processors for analysis. Silicon Graphics workstations provided this capability, making it possible to graphically visualize the large number of models that define an entire vehicle.

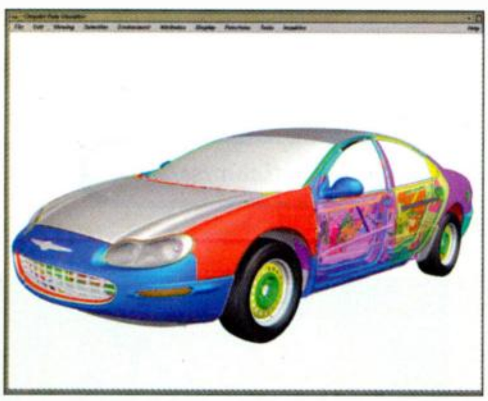


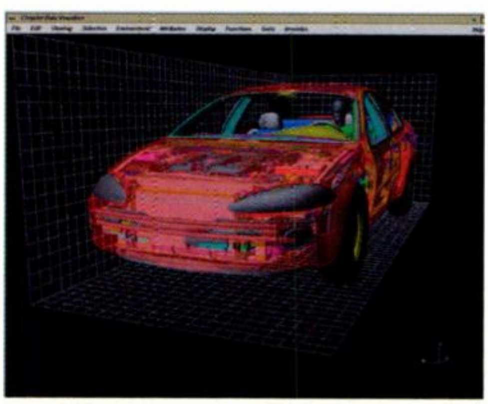
This visualization capability is significant because—well, as the old saying goes, a picture is worth a thousand words. As a result, design team members can review design changes and issues in real time, often at coordination meetings with interactive images projected on the wall. The images allow the designers to clearly communicate what the real issues are. Then the group can resolve those issues in minutes. By comparison, the old way of doing things, using a physical mock-up, would have taken on average 12 weeks to complete.

Chrysler, having fully adopted this innovative approach to car design, recently announced the design of the first paperless cars; its next-generation of full-size sedans including the 1998 Chrysler Concord, the 1998 Dodge Intrepid, and the 1999 Chrysler 300M and LHS. With its paperless car design, Chrysler shaved eight months off the design cycle. The new technique reduced the design and engineering cycle time from 39 to 31 months, while at the same time, increasing the quality of the automobiles produced.

Chrysler was also able to eliminate the need for reliance on inefficient paper drawings; expensive clay models; and visualization and analysis of such activities as model reduction, animation, interference, fits, assembly processing and vehicle configuration. Much of this has been replaced by digital prototyping.

For its new line of vehicles, Chrysler created and analyzed more than 5500 digital parts. It identified and resolved over 1500 interference, fit, and design issues prior to the building of the first physical prototype vehicles for the Intrepid and Concorde. And, it was able to verify the processing required to install the power train and chassis into the body prior to actual installation. As a result, the '98 LH vehicle fit the first time. During the building of the '98 LH, it took the company three weeks to get the power train and chassis installed because there were so many interferences.





For more information, contact Silicon Graphics, 2011 N. Shoreline Blvd., Mountain View, CA 94043; (650) 960-1980; fax (800) 758-5804, ext. 795806; www.sgi.com.

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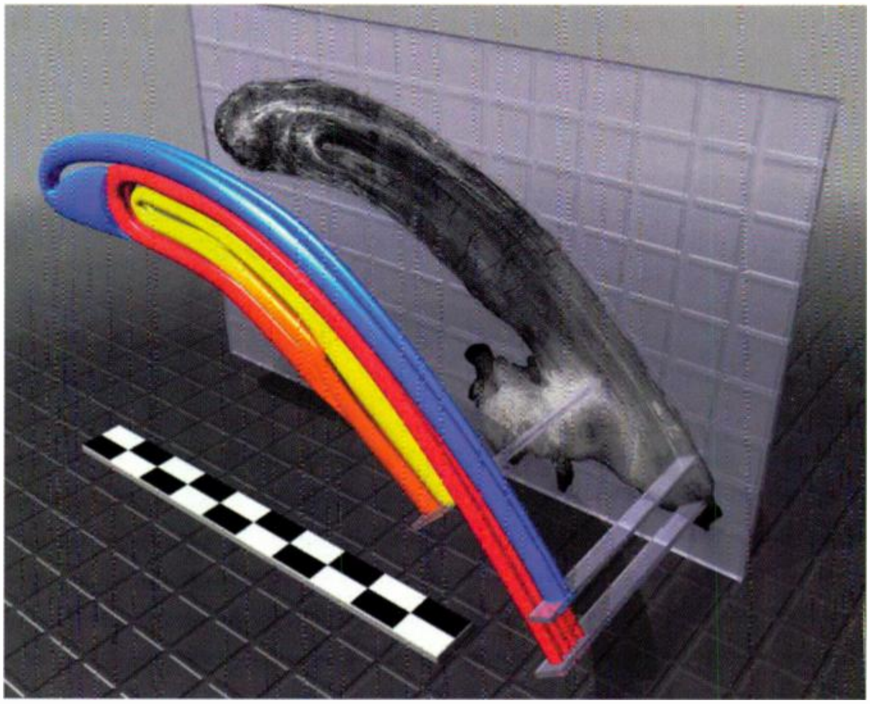
READER SERVICE 233

Parasaurolophus Dinosaurs Find A Voice

You can't help but be caught up in the dinosaur craze that's been going on the past few years, spurred on by modern day movies like "Jurassic Park" and "The Lost World." Even if you haven't seen, or at least heard about these movies, it's probably a safe bet you've been to a Natural History museum sometime in your life—even if it was just a school field trip in the third grade.



Dinosaurs fuel our imagination. We speculate about what they might have looked like, using fossilized bones to reconstruct their forms in much the same way you would put together a jigsaw puzzle. But, have you ever wondered what they sounded like? Until now, scientists could only guess because the technology needed to recreate the sound simply did not exist.

Scientists at Sandia National Laboratories and the New Mexico Museum of Natural History and Science have recently shed light on this mystery. Now, roughly 75 million years after dinosaurs ceased to walk the earth, they have once again found a voice. Using Digital Paleontology, scientists were able to recreate the voice of the Parasaurolophus dinosaur. And, as they previously guessed, the sound is very much like a resonating low-frequency rumbling sound that can change in pitch.

Just as a human voice can be distinguished from an animal's or another human's, scientists believe that this dinosaur had a very distinctive voice. Some have suggested that the sound may have been birdlike and that the large bones in the dinosaur's ears allowed them to hear lower frequencies than humans.

This quest to find the Parasaurolophus's voice began in August 1995, when a 4.5-ft. long skull fossil was discovered in northwest New Mexico. The skull included a nearly complete bony tubular crest with air cavities that extended back from the top of the dinosaurs head. This crest is what was believed to allow the dinosaur to produce a distinctive sound.

Scientists set out immediately to reconstruct the skull. Once this was complete, they began creating a three-dimensional model of the dinosaur's crest using computed tomography (CT) scans. This technique allowed scientists to analyze the inside of the crest without having to physically cut through it or damage it in any way.

The scans were then fed into a powerful computer, which used the numerically formatted input to reconstruct an undistorted crest. In the much same way the size and shape of a musical instrument dictates what its pitch and tone will be, the size and shape of the dinosaur's crest shows the natural frequency of the sound waves the dinosaur pumped out. In the final stage of the process, the computer simulated the act of blowing air through the dinosaurs crest to amplify the tones it was capable of making.

Additional information on this exciting discovery can be obtained by contacting John Arnold, Public Relations officer of the New Mexico Museum of Natural History and Science at (505) 841-2826, or by e-mail at tom@nmmnh-abq.mus.nm.us. For further details or to hear the dinosaurs voice check out the Sandia National Laboratories' web page: www.sandia.gov/LabNews/LabNews.html.

Cheryl Ajluni

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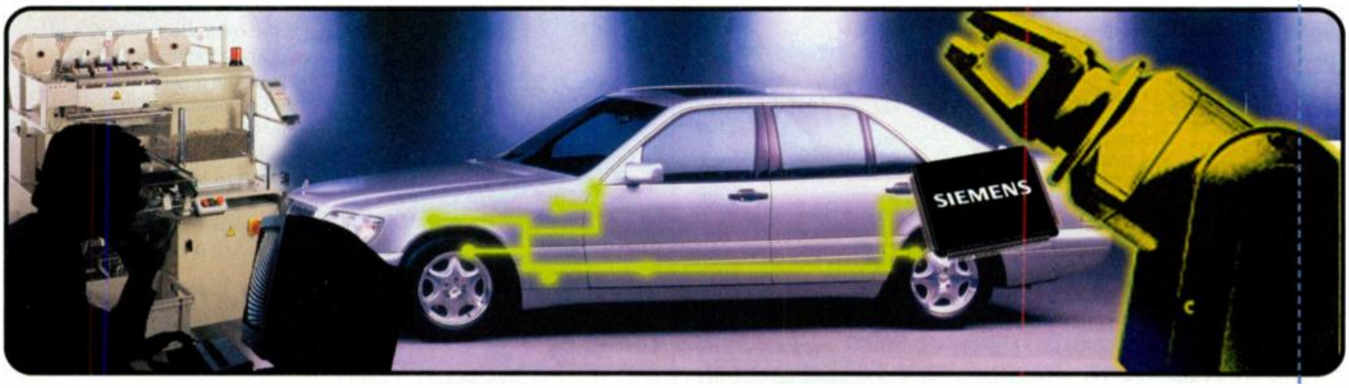

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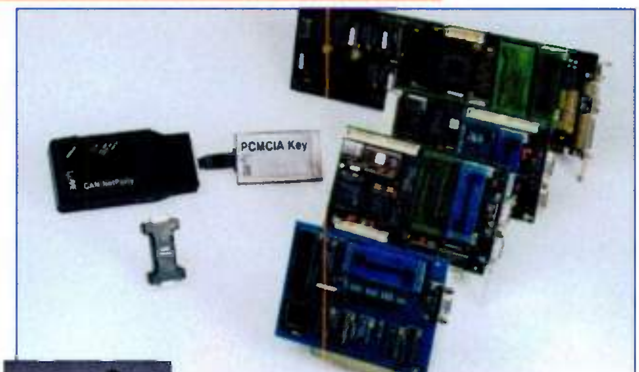

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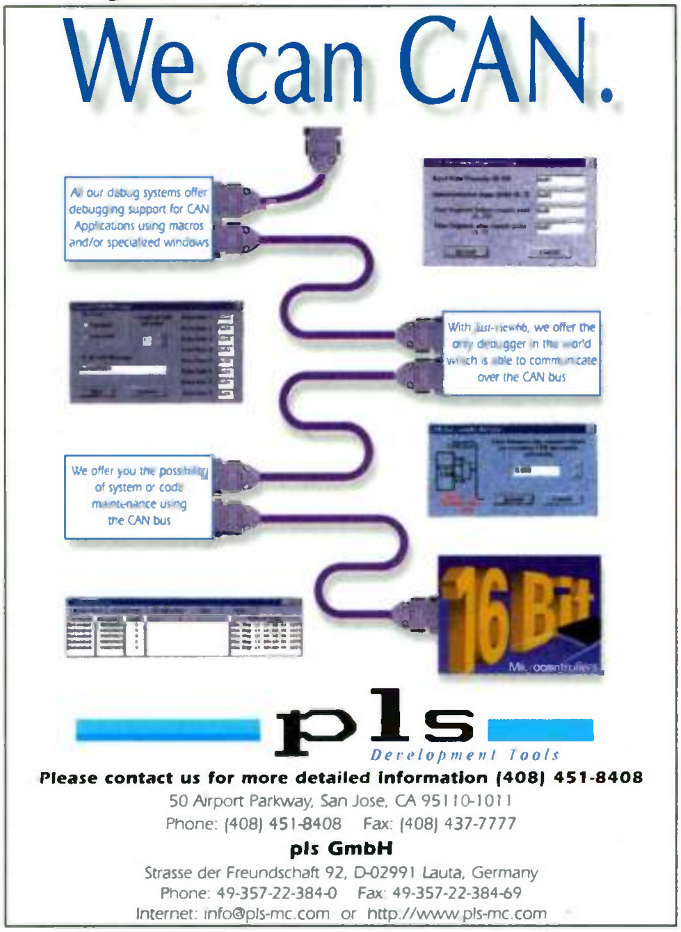

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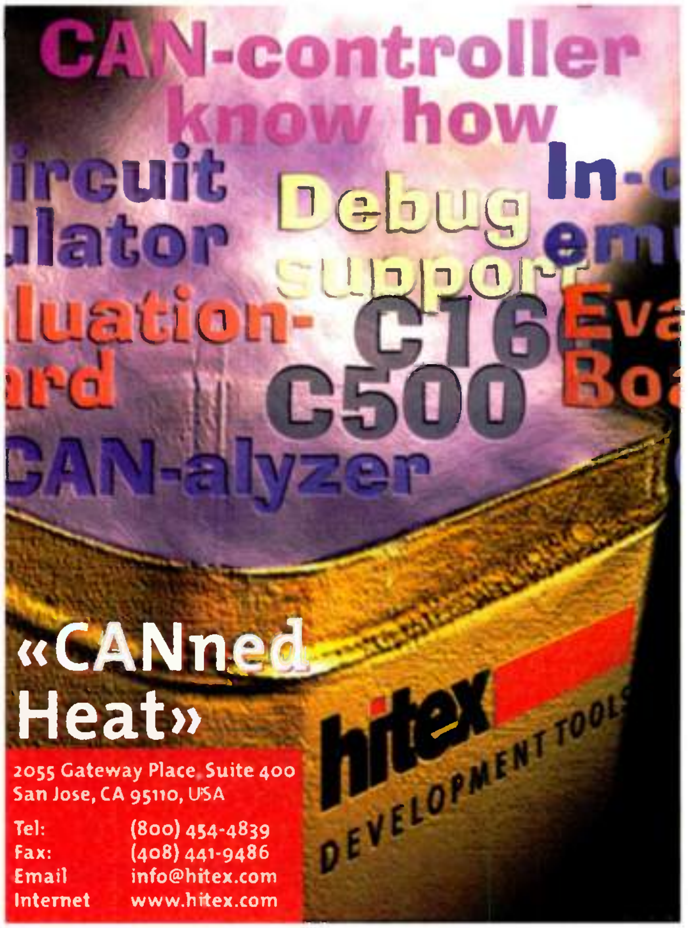

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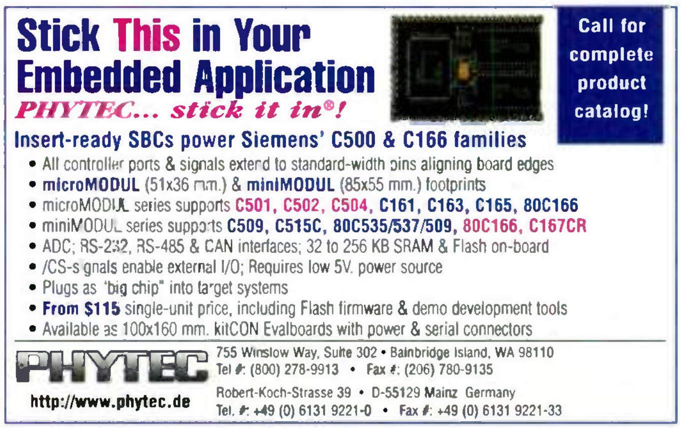

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Industry Council Approves Privacy Principles

Electronic privacy, once solely the concern of cloak-and-dagger types, has now become a mainstream issue. The Information Technology Industry Council (ITI), Washington, D.C., has adopted guidelines for good business practices to encourage the protection of personal data in the digital age. In an attempt to head off potentially restrictive government regulations, the ITI has released its own set of voluntary industry guidelines.

Comprising leading electronics manufacturers, ITI's stated goal is to work with industry groups, consumers, and policy makers in a global initiative to develop international consensus on privacy in an online environment. As more of society becomes "wired," it is becoming apparent that everything from birthdays to credit card transactions can be easily accessed for legal or illegal purposes.

ITI's guidelines stress that appropriate protection and management of personal data is a critical element in enabling consumers to realize the potential of global electronic commerce. The principles define personal data as any information relating to an identified or identifiable individual.

Market-Based Initiatives

In its policy statement, the document explains that "collectors and users of personal data, both private and governmental, and the individuals who provide their personal information, share the responsibility for fair and secure use of individually identifiable information." To address these issues, the paper proposes the use of market-led initiatives to develop policies that protect personal data. These initiatives "should strike a balance between the societal, economic, and individual benefits derived from the free flow of information, and protection of individuals' personal data."

Because personal data varies in the level of sensitivity and need for protection, the paper recommends "industry-by-industry approaches." It says that they "offer the best balance between societal and individual benefits and rights," The authors justify this approach by explaining that "attempts to protect all data equally and without discrimination will limit individual choice, prevent full participation in the global information society, and impose needless complexity and cost."

The full text of the ITI Privacy Principles follows:

ITI has adopted these principles for the protection of personal data in electronic commerce for the guidance of ITI members. These principles will serve as a foundation upon which member companies can build their own privacy policies, tailored to their particular business operations.

Information technology companies and online service providers, in addition to demonstrating commitment to these principles in their own business practices, should take the lead in making available to consumers the tools and functionalities that enable privacy choices in response to market demand.

These principles reflect the new challenges and opportunities offered by the advent of the global online marketplace and ITI's public policy positions.

Providing Information on Data Protection Policies

Collectors and users of personal data should give individuals easily understood information about their policies regarding the collection, use, and disclosure of personal data.

Notifying and Empowering the Consumer

Individuals have the right to be informed about, and exercise reasonable control over, the collection and use of their personal data. ITI member companies are developing market-driven technological solutions enabling individual data providers to exercise choice and control over their personal data. In many cases, electronic technologies offer greater personal data protection.

Limiting Data Collection

Collectors and users of personal data should limit the collection of personal data to that which is needed for valid business reasons, and any such data should be obtained by lawful and fair means.

Ensuring Data Accuracy

Collectors and users should strive to maintain the accuracy of the personal data held, including establishing, where appropriate, mechanisms allowing individuals to have the opportunity to review and correct their personal data in defined and secure circumstances.

Enabling Informed Choice

At the time of collection of personal data, collectors and users should furnish individuals with information on the intended use of such data, and with mechanisms permitting the exercise of choice on its disclosure.

Safeguarding Security

Collectors and users of personal data should take appropriate steps to ensure that personal data is protected from unauthorized access and disclosure, including limiting access to such data only to those employees with a business need to know.

Educating the Marketplace

Collectors and users of personal data, and particularly IT companies with expertise to share, should support and participate in consumer education efforts about the importance of fair information practices and privacy protection. Individuals should use their powers of choice in the marketplace to safeguard their personal data and that of their children.

Adapting Privacy Practices to Electronic and Online Technologies

To the maximum extent possible, privacy principles and practices should be the same regardless of the specific technologies employed for data collection and use. Individuals should have a reasonably consistent expectation of privacy in both electronic and paper-based environments.

Informed Choice Is Key

ITI President Rhett Dawson, explained that the IT industry principles, "The Protection of Personal Data in Electronic Commerce," stress informed choice, shared responsibility, and strengthened security as the best means to enable consumers to protect their privacy. "ITI has adopted these principles for the guidance of its member companies as they develop and implement their own personal data protection policies," Dawson explained.

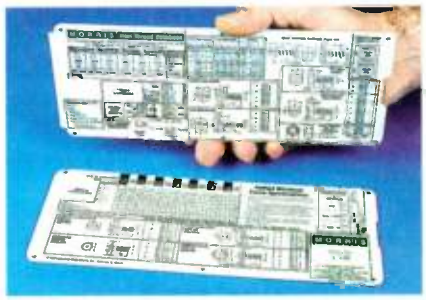
For more information, contact Janet Goebel, the Information Technology Industry Council, at (202) 626-5725 or at www.itic.org.

Lee Goldberg

XTRA

I know this is way before my time, but you might remember carrying around slide rules to do the work that we now accomplish with a computer. Then again, you might be like me. I have memories of my father's TI calculator in which you could plug "modules" that had different programs and formulas. The display was red LEDs, 10 characters long.

The thing about this calculator that made it useful for me was that it also came with these tiny slides that could fit into a space right below the display. Some of these slides had formulas printed on them in gold (not shiny gold, but a flat, '70s gold). I could not have gotten through Advanced Math without it. There are many tools that engineers (and nonengineers) use that are designed to carry as much useful information as possible, in the smallest space available.



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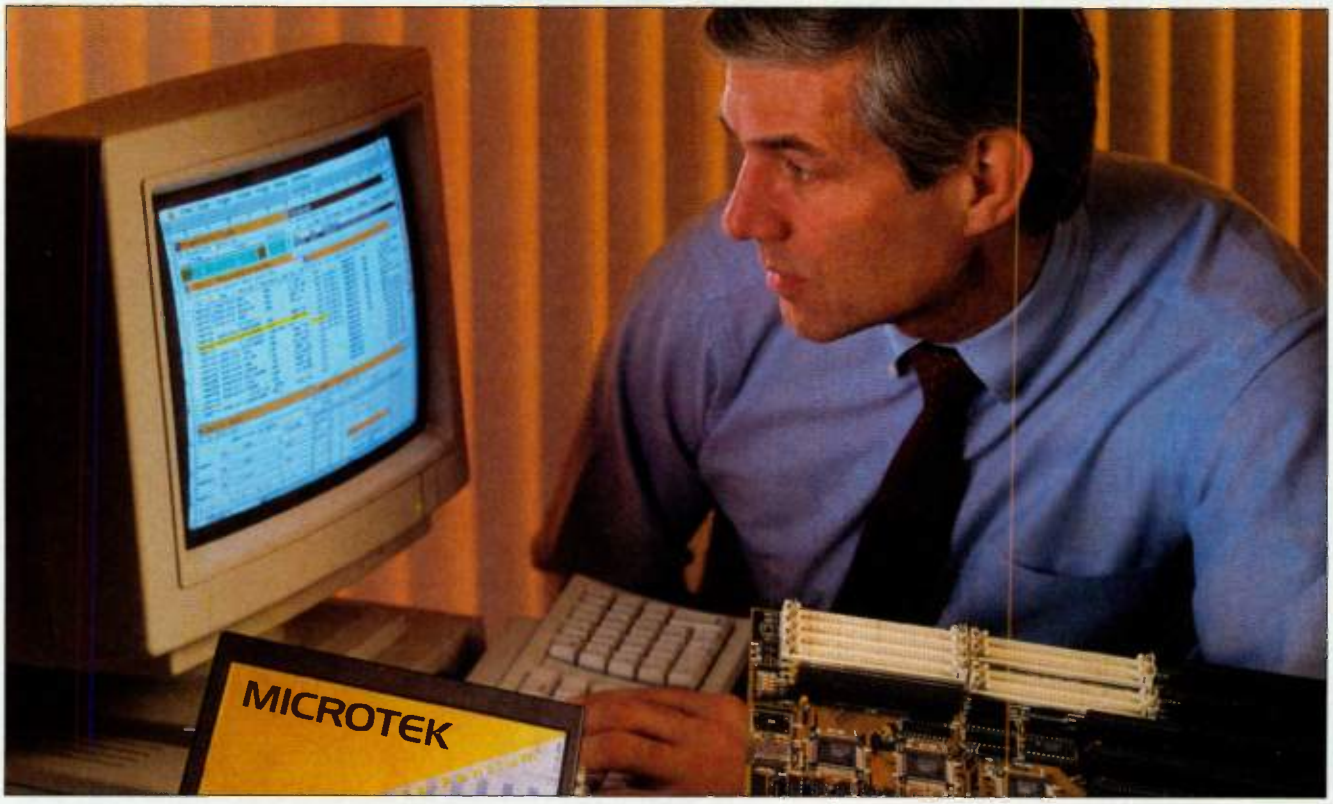

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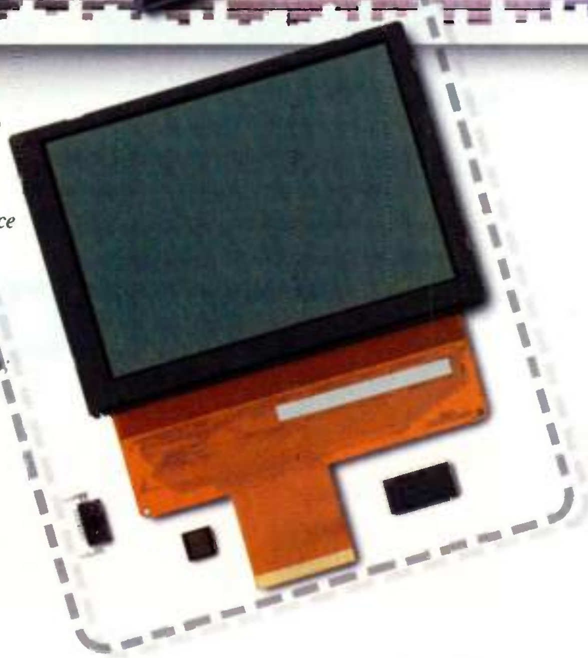
Room for everything but



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GREENLOOK

Until recently, designers concerned themselves only with how to build a product not its use or eventual disposal. Now, as more businesses are being forced to deal with the disposal and/or re-use of their products, a new discipline, known as *lifecycle engineering*, is gaining worldwide acceptance.

Leading the movement is an innovative research organization known as the Multi-Lifecycle Engineering Research Center (MERC), headquartered at the New Jersey Institute Of Technology (NJIT), Newark, N.J. "Current practice has created a linear flow from raw material extraction and processing into products and packaging that all too frequently are used once and discarded into a landfill," says Dr. Reggie Caudill, Executive Director of MERC. 'The Multi-Lifecycle Center will be a catalyst for the kind of revolutionary change in the engineering of products and processes that must occur in American industry."

Conceived in 1995 and in operation since February 1997, the MERC's mission is to turn environmental responsibility into a competitive advantage. Towards this end, the center is engaged in a number of projects, including developing new materials reengineered from waste streams, better products designed for remanufacture as well as manufacture, and agile production technologies that minimize waste and maximize production flexibility.

MERC employs a unique approach to design for environment (DFE) issues, using a cost-driven model to identify opportunities and approaches for solving environmental problems. By using a pragmatic, economic methodology to drive design, the program has attracted the support of many major companies, including AT&T, Fluor Daniels, IBM, Lucent Technologies, and Panasonic, who have already donated over $1.25 million.

According to Dr. Don Sebastian, a professor at NJIT and MERC staff member, part of the center's goal is to develop a common language between various engineering disciplines that will help them cooperate on larger issues such as recyclability, re-use, and overall environmental impact.

Current projects include development of software packages that will help engineers evaluate the manufacturability, health, quality, and environmental issues of a product while still in its design phase. Other programs look at design of universal disassembly tools and the analysis of current products for environmental impact and recyclability. Not all of MERC's programs are so theoretical. One of the more "hands-on" projects currently under way is one that looks at the best ways to recover materials from computers and CRTs, and finds potential uses for them.

For further information, contact the Multi-Lifecycle Engineering Research Center (MERC), New Jersey Institute of Technology, GITC Building, Suite 3400, 323 Martin Luther King Drive, Newark, NJ 07102; (973) 642-7198, fax (973) 642-7796.

Lee Goldberg

CH2M HILL is a company that helps public and private clients worldwide realize a greater return on their investments in environmental technology and sustainable infrastructure. The company, whose name is derived from the names of its founders (Cornell, Howland, Hayes, Merryfield, and Hill), specializes in project development, engineering and management of water, environmental and transportation infrastructure, and the design and construction of industrial facilities.

One of the company's subdivisions, IDC (Industrial Design Corporation), is a full-service firm that offers assistance in areas such as cost modeling for facility construction and operation, facilities services, and advance planning.

If you'd like more information on the company's services, contact CH2M HILL at 777-108th Ave. NE, Bellevue, WA 98004; (206) 453-5000; fax (206) 462-5957; Internet: http://www.ch2m.com.—**MS**

Africa's Smart Cards

Recently, Secretary of State Madeleine Albright traveled to Uganda to see the improvements made in the central African country as far as economic and overall living conditions were concerned. One of the major problems plaguing the Ugandans is the threat of robbery, injury, and even death, whenever they transport any amount of cash to and from banks and merchants. According to The World Bank, corruption and fraud are the biggest walls in the way of economic growth and stability in Africa. So, what are the solutions?

One solution to arrive in Africa from America was the Smart Card-based EMAX system from Productivity Enhancement Products (PEP). In January 1996, PEP installed the system at the International Credit Bank, Kampala, Uganda. Ever since, Smart Card payments have become the most widely accepted method of payment outside of Uganda shillings.

According to PEP, over 4000 Ugandans use PEP's Smart Cards to make purchases at over 500 merchants. Over $1.5 million are flowing through the Smart-Card EMAX system each month. Uganda's Revenue Authority (their version of the IRS) accepts the system for tax payments and license fees.

What's surprising about the change is that the Ugandan government agencies have made it *mandatory* to use Smart Cards. For example, the Ugandan Army and all government offices, must buy fuel with SmartFuel cards. And, now the Ugandan government is considering using the system for driver's licenses, military identification, and employee payment.

The EMAX point-of-sale merchant terminals work by using two cards. The customer's card makes the purchase and the system transfers the money to the merchant card. Consumer cards carry a Personal Identification Number (PIN) and a photograph of the consumer. Merchant cards carry a PIN and a photograph or company logo.

For more information, contact PEP, 26072 Merit Circle, #110, Laguna Hills, CA 92653; (714) 348-1011; fax (714) 348-1310.—**DS**

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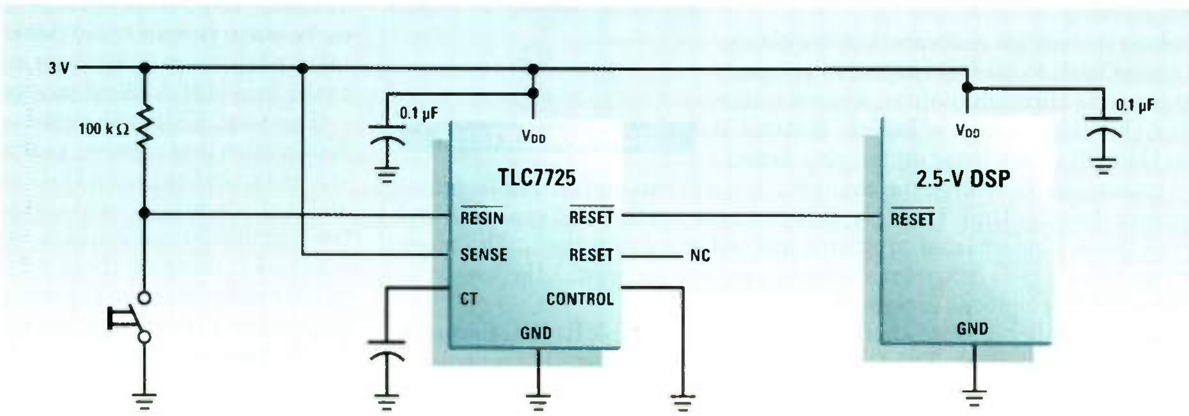

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MANAGING THE DESIGN FACTORY

The Champion Illusion

DON REINERTSEN

Inexperienced observers often note that a powerful executive champion increases the chance of project success. When MR. BIG becomes personally involved in a project, it happens faster and with less pain. The project also usually appears more successful, although this is harder to judge, because nobody wants to tell MR. BIG that his personal efforts were wasted. The conclusion: a powerful executive sponsor is key for a project's success.

The observations are accurate, but the conclusion is superficial. Powerful executive sponsors do help projects through their processes faster. However, this is not a sign of health. Instead, it screams that there are basic underlying defects in the organization. In reality, the champion is a workaround for fundamental management defects. Unfortunately, this common workaround obscures and preserves these fundamental problems instead of solving them. The more your organization needs champions to make projects successful, the less well-managed your development process is.

Let's think a little bit more about what happens when MR. BIG becomes interested in the program. The CEO is personally interested in a project. Every time this project encounters a bottleneck in the process the magical name of the CEO is invoked and the obstacles melt away. You can't get the capital authorization approved? Have MR. BIG's secretary call the finance department. You can't get a part through receiving inspection? Tell the inspectors that MR. BIG wants to know the badge number of anyone who delays the program.

The interventions of MR. BIG are not, in fact, making any basic improvements in the management process at all. Actually, they just allow his favorite project to jump to the head of the queue. Pushing his project to the head of the test queue doesn't mean that he has eliminated the queue in testing. Bypassing the mind-deadening bureaucracy that makes it take 40 signatures and four weeks to place a purchase order does not solve the bigger problem. This approach is cheating the system, not fixing it.

Ask yourself why development teams do not tell you that the key to getting paid is having a powerful champion to take care of your payroll. The answer is quite simple. Payroll works. The checks come out every month, printed correctly, and on time. You don't need an executive champion when a process does what it is supposed to do. If you have to use the influence of this type of individual to get things to work the way they are supposed to, you have a big problem. It means that your development process is broken and it needs to be fixed.

It is time to confront the real issue. The reason why champions work is because our development processes are usually massively overloaded. This situation creates large queues, which make head-of-the-line privileges valuable. Sadly, most supermarkets and gas stations have a better idea of how big their queues are than most development processes. And you don't need to personally know the store manager to buy groceries. Until we start measuring and managing queues the way we need to, we are unlikely to make any real progress. We will only accelerate individual projects, creating the illusion of progress, and ducking the true underlying problems.

Don Reinertsen is president of Reinertsen & Associates, a consulting firm specializing in product development management. Reinertsen is the author of "Managing The Design Factory: A Product Developer's Toolkit." He can be reached at (310) 373-5332 or e-mail: DonReinertsen@compuserve.com.

The Money's Out There For The Taking

It's great to have a good idea, an interesting technology, and ways of publicizing it, but if you don't have the funds to produce it on a large scale or research and test it, you're not going anywhere. One place to turn is the Department of Defense (DoD). DoD's Small Business Innovation Research (SBIR) and Small Business Technology Transfer (STTR) programs fund early-stage research and development projects at small companies to the tune of $0.5 billion each year.

This year, SBIR will award over $500 million to companies performing work that serves a DoD need and that potentially could end up in the commercial marketplace. Small companies, meaning those with up to 500 employees have the opportunity twice a year to secure these funds. The presolicitation period begins in April, and topic authors and topics are available online at: *www.acq.osd.mil/sadbu/sbir/*.

STTR directly funds small companies that work with researchers at universities and other research institutions. Small companies also can opt for the Fast Track policy, which allows a small business that wins a cash investment from an outside investor to gain a greater chance of a Phase II SBIR or STTR award. It also allows companies who win the funds to have expedited processing of their contracts.

Phase I is a six-month payment of up to $100,000 to determine the scientific, technical, and commercial feasibility of a company's new technology. Phase II encompasses up to two years and $750,000 to further develop the Phase I concept. By now the company should be at the prototype point. Finally, Phase III brings the technology to commercialization in either the private sector and/or military, using funds from sources other than SBIR.

For more information, contact SBIR, 8260 Willow Oaks Corporate Dr., Suite 800, Fairfax, VA 22031; (703) 205-1527; fax (703) 204-9447; e-mail: dod_sbir@brtrc.com.—DS

JUNE

Exhibition & Conference on System Integration in Microelectronics, June 16-18. Nuremberg Exhibition Centre. Call +49 711-61946-26/-74; fax +49 711-61946-93; www.mesago.de

JULY

IEEE International Geoscience & Remote Sensing Symposium (IGARSS '98), July 6-10. Sheraton Seattle, Washington. Contact Tammy I. Stein, IGARSS Business Office, 2610 Lakeway Drive, Seabrook, Texas 77586-1587, (281) 291-9222; fax (281) 291-9224; e-mail: tstein@phoenix.net.

IEEE Power Engineering Society Summer Meeting, July 12-16. Sheraton San Diego Hotel & Marina, San Diego, California. Contact Terry Snow, San Diego Gas & Electric, Post Office Box 1831, San Diego, California 92112; (619) 696-2780; fax (619) 699-5096; e-mail: t.snow@ieee.org.

SPIE's Annual Meeting & Optical Instrumentation Show, July 19-24. San Diego, California. Contact SPIE Exhibits Dept., P.O. Box 10, Bellingham, Washington 98227-0010; (360) 676-3290; fax (360) 647-1445; e-mail: exhibits@spie.org.

IEEE Nuclear & Space Radiation Effects Conference (NSREC '98), July 20-24. Newport Beach, California. Contact Jim Schwank, Sandia National Laboratories, Post Office Box 5800, MS-1083, Albuquerque, New Mexico 87185-1083; (505) 844-8376; fax (505) 844-2991; e-mail: schwanjr@sandia.gov.

AUGUST

AUTOTESTCON '98, Aug. 24-27. Salt Palace Convention Center, Salt Lake City, Utah. Contact Robert Myers, Myers/Smith Inc., 3685 Motor Avenue, Suite 240, Los Angeles, California 90034; (310) 287-1463; fax (310) 287-1851; e-mail: bob.myers@ieee.org.

SEPTEMBER

Sixth European Congress on Intelligent Techniques & Soft Computing (EUFIT '98), Sept. 7-10. Aachen, Germany. Contact Conference Secretariat: EUFIT '98, Promenade 9, D-52076 Aachen, Germany; +49 2408-6969; fax +49 2408-94582; e-mail: eufit elite/eufit.html.

ICSPAT & DSP World Expo, Sept. 13-16. Toronto Metro Convention Center, Toronto, Ontario, Canada. Contact Liz Austin, Miller Freeman Inc., (888) 239-5563, (415) 538-3848, e-mail: dspworld@mfi.com; www.dspworld.com.

WESCON '98, Sept. 15-17. Anaheim Convention Center, Anaheim, CA. Contact Electronic Conventions Management, (800) 877-2668; (310) 215-3976; fax (310)641-5117; e-mail: wescon.ieee.org; www.wescom.com.

Second International Conference on Evolvable Systems (ICES '98), Sept. 23-26. Swiss Federal Institute of Technology, Lausanne, Switzerland. Contact Andres Perez-Uribe, conference secretariat, +41 21- 6932652; fax +41 21-6933705; e-mail: Andres.Perez@di.epfl.ch; lslwww.

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Information Appliances: From Web Phones To Smart Refrigerators

Embedded Information Processors Are Spawning Many Unexpected Applications As They Use LAN And Internet Protocols To Communicate Across Almost Any Network.

Lee Goldberg

SPECIAL REPORT

The term "information appliance" (IA) is, at best, a slippery thing to define. That's probably the result of the enormous range of products emerging which perform embedded information access and processing. Unlike a regular PC or workstation, an IA hides its operating system and computational abilities behind a task-oriented interface. Using LANs, the Internet, and wireless technologies, these embedded communicators will provide connectivity to nearly every kind of electronic device manufactured in the coming years.

The broad spectrum of applications for IAs also makes a definition difficult to pin down, because it applies to a variety of devices, ranging from a set-top web browser to an Internet-enabled cardiac monitor. In fact, the obvious consumer applications, such as web phones, Internet-capable PDAs, and thin-client web browsers represent only the tip of a large digital iceberg.

Art Courtesy: Philips Electronics

Many of the applications for information appliances will be invisible, residing in web-savvy networking products, printers, environmental and industrial controls, and remote data-acquisition systems. With this in mind, let's try to get a working understanding of what the heck the electronics industry means when it talks so glibly about these new-fangled information appliances.

Until recently, communication products were designed to plug into one of several large, non-interoperable network infrastructures. This worked ell, unless one was attempting to connect across network boundaries. Beyond differences in their physical layers, the Internet, telephone systems, pager networks, and most local-area networks employed different protocols, requiring unwieldy bridging and conversion technologies to pass data between them. Even switches and routers from different vendors operating on the same local network often used different proprietary protocols to support remote management and control functions.

Common Protocols

This situation has changed over the past few years, as Internet protocols have gradually become almost universal as mediums of exchange between devices. Common data exchange standards such as Internet protocol (IP), file-transfer protocol (FTP), point-to-point protocol (PPP); and Internet-derived languages such as hypertext mark-up language (HTML), and Java are being used to form a smooth overlay that allows easy communication between wildly dissimilar systems.

Browser-based HTML pages now provide an

easily accessible front end, which can communicate with nearly any garden-variety PC using generic software. This lets a user employ the same browser-based program to retrieve e-mail, check the status of a printer in the next office, or send a text message to a pager. Network managers are also beginning to benefit from browser-based management software. A Web-aware program can let them quickly determine the status of network devices in the next room, city, or country.

Developers also benefit because they can bring their web-based software to market quickly, thanks to an abundance of development tools and libraries of prewritten code for nearly any application. In fact, many operating systems now come bundled with mail and file-transfer protocols, IP address handling, and connection-management functions. If your application requires additional functions or security features, there are several vendors who can supply them in either native or platform-independent code.

A Quick Market Overview

While IAs come in all shapes and sizes, they can be roughly classified into a variety of categories. The one many people think of first is the "thin-client" computer. These sub-$1000 (even as low as $500) units typically include a display and keyboard, plus some sort of pointing device. Applications and data will not be resident on these diskless wonders, but instead are loaded into their RAM off a server when needed.

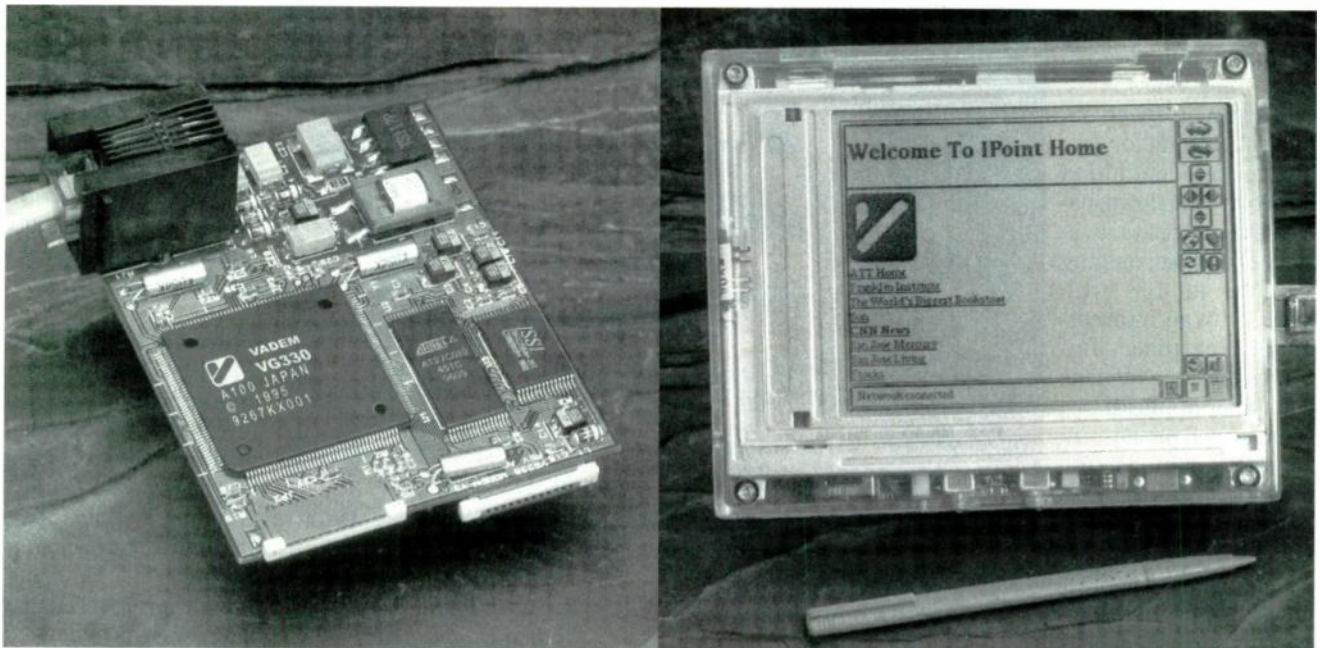
Several manufacturers expect that thin-client machines will find a home on many desks within the corporate and industrial sector, handling tasks that don't require the power of a full-blown workstation. These tasks could include things like word processing, order processing, data entry, and web access. Besides being less expensive to purchase, these high-end data appliances will cost significantly less to manage and support, according to thin-client advocates.

The other classic thin client is the set-top web browser. Intended to appeal to consumers with limited computer experience and less money to spend, set-top web browsers are marketed with varying degrees of success. Depending on options and features, these devices can retail for between $200 to $500.

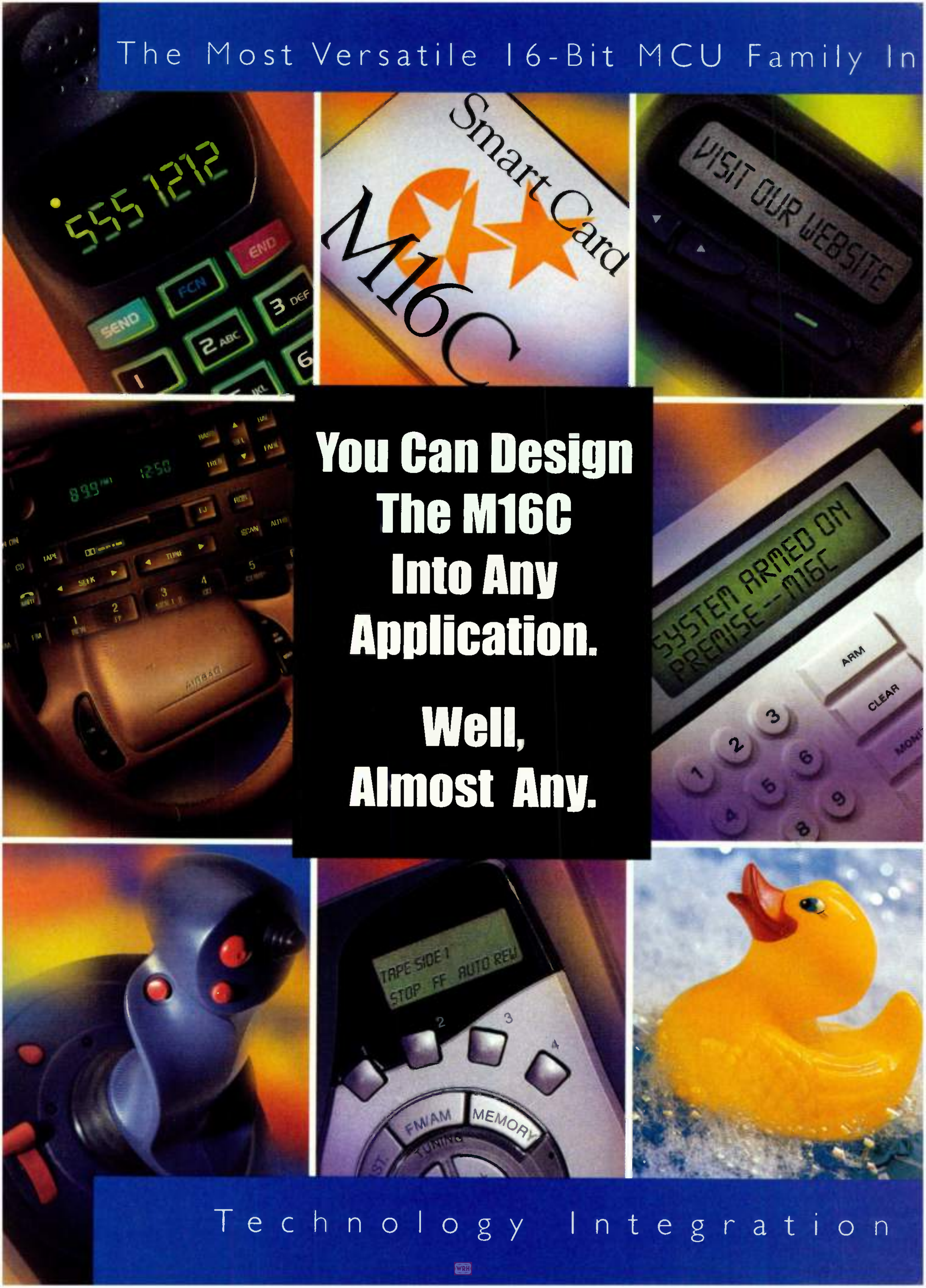
Another interesting variation is the web phone. These jazzed-up phones can directly access the Internet using a built-in modem, display, and embedded protocol processing functions *(see opening photo)*. Depending on screen resolution and available CPU power, some of these devices can view web pages, while others will simply send and receive e-mail. It is unclear at this time whether web phones will remain expensive novelties or become must-have fixtures in the average consumer's home.

While the web phone's fate is still in question, its wireless counterpart, the smart cellular phone is not. Cellular communication has become a way of life. Now, being able to make calls from anywhere is not enough, and there's a rapidly growing demand for wireless access to e-mail, faxes, and corporate file servers.

To fill this gap, manufacturers are adding larger displays, alphanumeric keypads, and significant amounts of processing power to their phones. They leverage the digital cellular/PCS infrastructure to send and receive data without the annoying bottleneck of having to convert it to modem tones first. The resulting products are hybrids which borrow functions from pagers, PDAs, and palmtop computers. It's too early to say which combination of features will be the most useful, but it's a good bet that you will have some sort of e-mail capability on your cell phone by 2001.



1. Embedded systems like the Vadem VG330, a 16-bit, 32-MHz, x86-based, information appliance reference design, can accelerate development of web-enabled applications (a). Integrated with developer's software, the design's IPoint firmware handles low-level protocols such as TCP/IP, PPP, and SLIP, plus tasks like modem or ISP setup, and FTP/SMTP transactions. The reference design can be embedded as a standalone Internet interface. With the addition of a display and input device, it can serve as web browser and user interface within a PDA or web-phone (b).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The pager industry is also undergoing a quiet revolution. Since there are many applications where a message of a few hundred characters or less is more than sufficient, designers are beginning to embed alphanumeric pagers into portable equipment. Thanks to a global infrastructure, mature technology, and low hardware cost, it now makes sense to place one- or two-way messaging capability into a palmtop, PDA, or other specialized handheld devices. Pager circuits have been designed to be exceptionally power-frugal, allowing them to easily piggy-back off a palmtop's tiny battery without severely impacting its operating time.

Throughout these categories runs the embedded system. Within nearly any kind of electronic device, it performs the low-level protocol processing and link control invisibly, enabling smart machines to talk to each other. For example, a delivery company might be able to query one of its trucks for its location and a list the parcels that had been delivered, using a web browser and a wireless link to the truck's onboard computer.

Protocols: Bricks And Mortar

Underlying this dazzling array of futuristic technology are the standards and protocols that enable communications between dissimilar devices across networks of undetermined pedigree. They act as "middleware," providing flow control, error correction, and data format conversion as needed.

Perhaps the most fundamental of all these standards is the transmission control protocol (TCP). Developed back in the 1960s, it enables setup of error-protected data connections between two end points across a network with an arbitrary topology. Alongside TCP is the internetworking protocol (IP), which handles hardware-layer issues such as addressing of packets, fragmentation and reassembly control, and encapsulation of data into other protocols. For connectionless transmissions, such as e-mail messages, the user datagram protocol (UDP) is most often employed. While UDP has no error control or guarantee of delivery, it is very efficient and allows these features to be invoked at a higher layer if desired.

The point-to-point protocol (PPP) is another very important connection tool. It provides the flow control, buffering, and other signaling necessary to set up Internet connections over dial-up and leased phone lines.

Further up the hierarchy, we find file-handling protocols, which break down files into IP packets, oversee their transmission, and reassemble them on the other end. Aptly named, the file-transfer protocol (FTP) is one

Resources For Information Appliance Design

Protocol Processors

Osicom Technologies Inc., *411 Oaks Rd., Bldg. 227, Waltham, MA 02154; (617) 647-1234; fax (617) 398-4867; www.digprod.com.*

Osicom manufactures the NET+ARM system-on-silicon, which combines an ARM RISC processor, a communications-oriented RTOS, a full suite of communication protocols, and on-chip interface circuitry for 10/100-Mbit Ethernet and other network applications. Ready to support HTTP and FTP clients and servers, the embedded software includes APIs for browser, server, and mail functions, plus a full TCP/IP stack. CIRCLE 486

Sun Microsystems, *901 San Antonio Rd., MS USJC02-302, Palo Alto, CA 94303, attn: Jenny Johnston; (408) 544-0176; fax (408) 544-0220; www.sun.com/sparc.*

Sun's low-cost, low-power chip directly executes either Java or Personal Java code quickly, without running an interpreter. A substantial library of I/O drivers, protocol stacks, and APIs is provided as a part of the device's development suite. Several flavors of the chip will soon be available to match various processing and I/O requirements. CIRCLE 487

Vadem Inc., *1960 Zanker Rd., San Jose, CA 95112; (408) 467-2100; fax (408) 467-2199; www. vadem.com.*

Vadem specializes in highly integrated solutions for embedded systems. Among their latest creations is the VG330, a 16-bit, 32-MHz, x86-based device. The VG330 is the heart of the IPump reference design, a low-cost platform which runs Vadem's IPoint Internet data transfer software. Its modular design can be adapted for a wide variety of applications. IPoint handles low-level protocols such as TCP/IP, PPP, and SLIP, plus tasks like modem or ISP setup, and FTP/SMTP transactions. CIRCLE 488

CPUs And Controllers

Advanced Micro Devices, *One AMD Pl., P.O. Box 3453, Sunnyvale, CA 94088-3543; (408) 732-2400; (800) 538-8450; www.amd.com.*

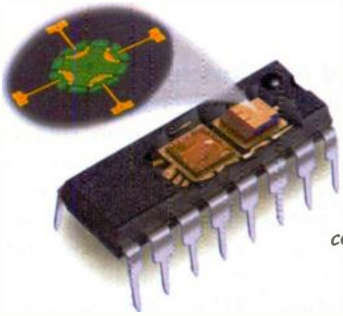
AMD's 16- and 32-bit system-on-a-chip products can include graphics controllers, communications interfaces, memory, and peripheral controller logic. Applications range from PDAs and set-top boxes, to wireless LAN controllers. Their new Elan series of controllers are aimed at power-sensitive applications like PDAs and palmtops, and can selectively clock only the portions of their logic currently being used. CIRCLE 489

Cirrus Logic Inc., *3100, W. Warren Ave., Fremont, CA 94538, attn: Ashis Kahn; (510) 226-2373; fax (510) 249-4540.*

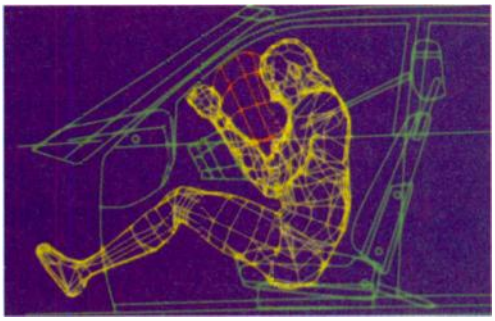
The CLPS7110, Cirrus Logic' version of the ARM RISC processor, delivers 15 MIPS while drawing 66 mW. It supports several operating systems, including Java OS, Wind River's Tornnado, and Microtec's VRTX. Versions of the ARM core are available which have been optimized for palmtop computing, network appliances, and wireless applications ranging from two-way paging to high-speed Internet access. CIRCLE 490

(continued on page 76)

Motorola's Sensors



Motorola's accelerometers feature the micromachined G-Cell that is available in a variety of packages ideal for automotive systems, computer and industrial products.



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of the most commonly invoked. Specialized file types often have their own protocols, such as HTTP and NNTP. HTTP is designed to efficiently handle the Hypertext used in web pages, and NNTP is used for moving network news files between Usenet news groups.

Mail services have their own protocols, such as the simple mail-transfer protocol (SMTP), the post-office protocol (POP), and the Internet message-access protocol (IMAP). For managing address books and adding addressing features (such as a web directory search), the lightweight directory-address protocol (LDAP) is most commonly used.

Originally, these protocols were run on the mainframe servers that shuttled mail and files between Internet sites. With the advent of the PC, they have migrated onto the desktop. Now, we are seeing handheld devices of all kinds implementing these functions in their ROM-based operating systems.

Because these standards-based protocol stacks are rather complex, many developers are choosing to license ready-made drivers to support the functions they need. Typically written in C, C++, or other platform-independent languages, they come with application programming interfaces (APIs) and drivers that minimize the effort required to integrate them with existing code *(see "Resources for Information Appliance Design," p. 74)*.

While many of today's protocols are excellent building blocks for most wired applications, they have difficulty coping with the display constraints and special challenges of maintaining a connection in a wireless environment. There is a new generation of protocols and standards emerging to support the unusual requirements of mobile data communication, however. We'll look at some of these in the April 20 issue, when we examine third-generation mobile-phone technologies.

Wired Appliances

Tethered IAs will get their network connections from one or more sources, including phone lines, cable-TV services, or fixed satellite connections. A web-capable thin-client usually communicates with its host by using standard Internet protocols such as TCP/IP and FTP, and languages such as HTML and Java. Using these established, well-supported standards will enable developers to quickly create browser-based applications including records access engines, group schedule managers, and transaction processing systems. At the low end of the spectrum, web phones provide an easy means of locating information and performing transactions such as shopping and banking.

(continued from page 74)

Digital Semiconductor Corp., *StrongARM Product Group, M.S. HL02-1/L12, 77 Reed Rd., Hudson, MA 01749; (800) 332-2717; (978) 628-4760; fax (978) 568-4866; www.digital.com/semiconductor/strongarm/strongar.html.*

The StrongARM processor, an extension of the ARM RISC engine, is a 32-bit, 100-Hz/150-MIPS machine aimed at compute-intensive applications where power is at a premium. A 233-MHz/268-MIPS version is also available, which consumes less than a watt of power. DEC also can supply extensive development software, as well as evaluation systems and prototyping boards. **CIRCLE 491**

LSI Logic Corp., *1551 McCarthy Blvd., Milpitas, CA 95035, attn: Denny Scharf; (408) 433-8000; fax (408) 433-8989; www.lsilogic.com*

LSI's "coreware" library of functional silicon blocks includes everything from MIPS, ARM RISC engines, and DSPs to interfaces for Ethernet, T1, ATM, and HDLC. Some drivers and protocol stacks are available also, as well as development tools. **CIRCLE 492**

Motorola Semiconductor Products, *P.O. Box 52073, Phoenix, AZ 85072-2073, attn: Mike Watson; (317) 571-7017; fax (317) 575-8278; e-mail: rvgb10@email.sps.mot.com; www.mot.com/ADC.*

Depending on the application, Mototola's product lines are built around their 68HCxx microcontrollers, their 6800x processor, or their 60x RISC architecture. There are single-chip systems for an assortment of applications from smart, two-way pagers and PDAs to SOHO routers. Development tools are available for most products. The MC92100 Scorpion graphics controller can turn a standard television into an interactive information appliance. Accepting MPEG2, DVD, and other digital video inputs, applications for Scorpion include Internet browsing, electronic program guides, and other set-top box functions. **CIRCLE 493**

Operating Systems And Software

CoSystems Inc., *1263 Oakmead Pkwy., Sunnyvale, CA 94086; (408) 522-0500; fax (408) 720-9114; www.cosystems.com.*

Their CoPPP/ML software provides an application with PPP and MultiLink PPP capability, enabling it to aggregate communication channels into a single high-bandwidth pipe. Coded in ANSI C language, it features bandwidth allocation control with call-back support, dynamic IP address allocation, header and data compression, authentication, filters for IP services, and many other functions required to support remote data links. **CIRCLE 494**

Cyber Vista, *1650 Borel Pl., Suite 121, San Mateo, CA 94402; (650) 372-0800; fax (650) 372-5605; www.cybervista.com.*

Cyber Vista's Data Grabber software solves one of the big problems encounterd with IAs - what to do with all that data. It can find, monitor, compare, analyze, retrieve, and distribute online information from the web, local databases, and other sources. Its smart agents can digest and reformat its findings to fit any display available. Software modules are available for servers, clients, and embedded applications. Security features can also be added as needed for secure transactions. **CIRCLE 495**

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KAWASAKI LSI

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The relatively low bit rates involved with POTS-based web phones lets them employ a single low-cost 16-bit microcontroller for communications control, protocol processing, applications processing, and juggling of the display and keyboard interfaces.

Set-top boxes perform similar functions, except that they use an ordinary television as an output device. Usually consisting of a modem, a medium-speed controller chip, and a video interface, the web phone can provide a means of accessing web pages without having to know a URL from an FTP. A pointing device of some kind (touch screen, joy stick, etc.) is the primary user interface, with a keyboard as an option.One of the primary tasks these boxes perform is reformatting the high-definition format HTML images used by web browsers, to be displayed on a low-resolution, consumer-grade, television CRT.

It is still uncertain whether the public will accept the concept of web pages on a television screen, or if people will be more comfortable surfing in a desktop environment. As the debate continues, we are seeing many novel variations on the set-top theme. Today's set-top units employ a variety of communication technologies. Among the most common are phone lines and cable data connections. While no firm plans have been announced, there is talk within the cable industry about incorporating a self-contained browser into the next generation of cable set-top boxes.

It is also interesting to note that set-top boxes are appearing which include satellite downlinks for fractional-Megabit access speeds.

Strategic Building Blocks

There is a wide variety of general-purpose processors available that are suitable for use in IAs. There are also several specialized communication controllers which offer cost, performance, and time-to-market advantages for some applications. These communication-oriented parts are equipped with on-chip I/Os that can handle anything from a single telephone connection to multichannel ISDN or SDLC services. Often, these specialized controllers are bundled with ready-made protocol stacks that speed product development and reduce interoperability problems.

In some cases, an even more integrated solution is desirable. For many IA applications, purchasing a complete reference design or board-level assembly for the communication engine can be a cost-effective choice *(Fig. 1)*. Often, these small boards can be purchased and configured for less than the cost of implementing a full-custom communication processor.

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General Software Inc., *12737 BelRed Rd., Suite 100, Bellvue, WA 98005-2636; (800) 850-5755; (425) 454-5755; www.gensw.com.*

General Software manufactures the embedded BIOS 4.0, used in the Vadem Internet appliance and other embedded systems. The modular BIOS contains its own embedded DOS-ROM. It is extensible and can be configured to support off-chip peripherals for most embedded tasks. A full suite of development and debug tools is also available. **CIRCLE 496**

Integrated Systems Inc., *201 Moffett Park Dive., Sunnyvale, CA 94089; (408) 542-1500; fax (408) 542-1950.*

In addition to their pSOS real-time operating system, and a real-time implementation of Java, their Epilogue division supplies a full suite of embedded Internet protocol stacks. Written for a variety of 8-, 16-, 32-, and 64-bit target processors (MIPS, Motorola, SPARC, x86, and others), software to develop web/HTTP and SNMP browser management functions, TCP/IP protocol stacks, and OSPF/RIP2/BGP4 routing applications is available. In addition, they implement both SNMP and RMON one-half network management functions, including master/sub-agent design, and MIB compilation. **CIRCLE 497**

Lucent Technologies Bell Labs, *600 Mountain Ave., Room 1C302, Murray Hill, NJ 07974; (888) 577-5650; (908) 582-4800; e-mail: infernosupport.com; www.lucent.com/inferno.*

Inferno 2.0 employs a virtual machine and OS for development of applications in Personal Java or Lucent's Limbo programming language. In distributed processing environments, Inferno allows its applications to check the target system and determine the interfaces and resources available to them at the time of execution. The kernel-based system runs in native mode on StrongARM, SPARC, Power PC, and X86 processors, or can be hosted as an application under most HP, SGI, Sun, and Windows operating systems. Inferno comes packaged with full suite of applications including a general-purpose GUI, an HTML browser, an e-mail protocol stack, and a variety of networking, PDA, and data exchange functions. **CIRCLE 498**

Passport Corp., *Mack Centre III, E. Ridgewood Ave., Paramus, NJ 07652; (201) 634-1100; fax (201) 634-4606.*

The Passport IntRprise development environment provides the tools and protocol stacks needed to develop Java-based thin-client applications for Windows or UNIX enterprise environments. Migration of applications written in C, C++, or COBOL also is possible. **CIRCLE 499**

Psion Software PLC, *19 Harcourt St., London, W1H 1DT, England, attn: Paul Cockerton; +44 171-208-1800; fax +44 171-724-4048; www.software.psion.com.*

Developed originally for the Psion series of PDAs, EPOC-32 is a real-time capable, modular operating system. Written in C++, the kernel-based architecture can be used in applications from an embedded meter reader to a smart phone or palmtop computer system. Unlike Windows CE, Psion's middleware allows developers to create their own GUIs for their particular platforms and tasks. Application-specific software modules can be added to enable products to do a variety of things from exchange HTML files to recognize handwriting. **CIRCLE 500**

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Telephone Line Interface Made Easy

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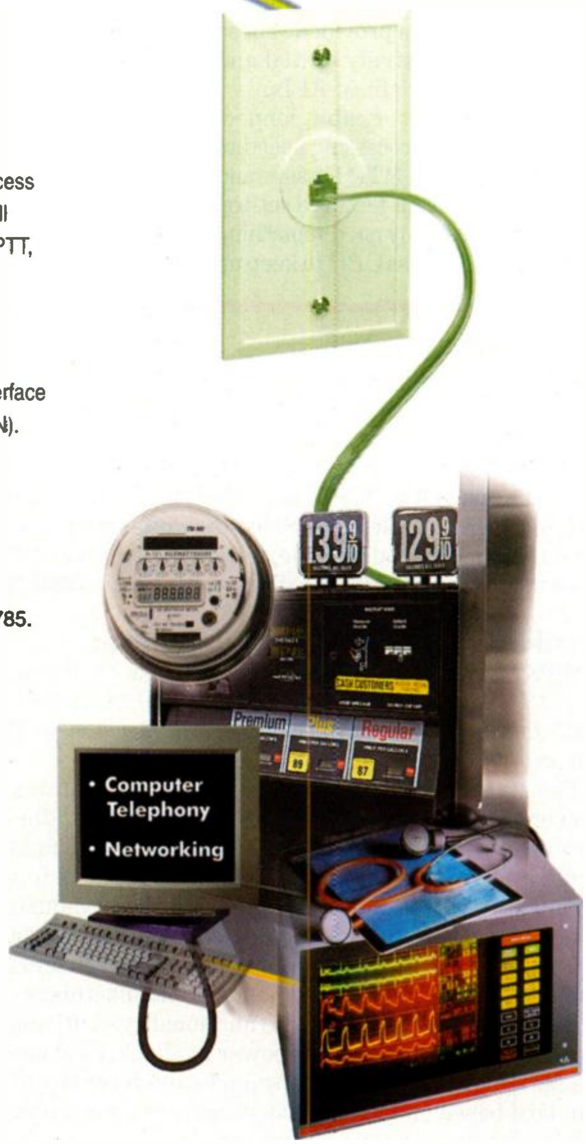

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In addition to providing all the necessary processing and network interface hardware, these tiny engines also contain embedded firmware with many of the most important protocol stacks (TCP, IP, PPP, UDP, etc.) already in place. The protocols are usually built directly on top of a ROM-based real-time operating system, making user calls from other applications easy and reliable *(Fig. 2)*. To further accelerate development, ROM-based network applications like FTP, HTTP, Telnet, POP3, and mail service, as well as the SNMP management functions, can also be provided. These routines are extensively tested and equipped with well-defined APIs.

Higher-rate DSL or cable connections require more processing speed to deliver graphics-rich HTML pages and full-motion video. Full-featured set-top browsers will probably need something close to a desktop-class CPU to keep up with the load. They also might need an off-chip graphics accelerator.

Some of the more interesting uses for these advanced services do not necessarily require the blinding speed they provide. Unlike a switched phone connection, both cable and DSL are constantly online. This opens up the potential for using web-based technology to remotely monitor and control all manner of automated functions. One intriguing application would be to support a secure home page that provided an authorized user to monitor or change the settings of a building's security or HVAC systems.

From here, it's not too big a stretch to imagine "smart appliances" linked to the Internet via your set-top box, using a low-cost network running through your home. Once networked, your dishwasher, refrigerator, or furnace could perform self-diagnosis and make automatic service calls over the Internet when needed. One could even imagine browsing the contents of one's refrigerator from work to make sure there is enough milk for dinner.

Another concept that is being explored at Motorola Semiconductor, Austin Tex., is the idea of a cordless web phone. Ken Edwards, marketing manager for Motorola's Embedded Computing Products Division, explains that the gadget would have a portable tablet with a keyboard and/or touch screen that would dock with a base station. Much like a conventional cordless phone, the screen and base would communicate over the 900-MHz or 2.4-GHz unlicensed bands. In theory, the base station would perform most of the processing. Transfer screen images at rates of up to 100 kbits/s could be achieved using commercially available digital spread-spectrum chip sets. If an efficient image-transfer protocol were developed,

(continued from page 78)

Trillium Digital Systems Inc., *12001 Wilshire Blvd., Suite 1800, Los Angeles, CA 90025-7118; (310) 442-9222; fax (310) 442-1162; www.trillium.com.*

Protocol stacks for TCP/IP, Frame Relay, and ATM networks, as well as V.5, X.25, ISDN, and SS7 telecom systems are available here. Since they offer fully annotated C-language source code, designers can customize these modules to their particular application. **CIRCLE 501**

Standards And Technology Information

MIPS Forum, *c/o John McQueen, P.O. Box 71, Massillon, OH 44648; (330) 833-8690; fax (330) 833-4002; e-mail: johnmcqueen@compuserve.com, www.mips-forum.org.*

The MIPS Forum works with industry to establish interoperability standards that will permit handheld wireless devices to access the Internet, exchange multimedia information, and perform other advanced functions. The MIPS Forum has begun building an industry model of wireless information devices in the years 2000 and 2002. The goal of this effort is to gain a consensus among service providers and handset manufacturers on projected availability of basic functionality. Anticipating the increased processing power available to phones, the MIPS group seeks to support development of a standard based on the Java language and the graphics-rich applications that it can support.

WAP Forum, *www.wapforum.org and www.xwap.com.*

The Wireless Application Protocol (WAP) Forum is an industry consortium which was established by Ericsson, Motorola, Nokia, and Unwired Planet. It aims to create a global wireless protocol specification. The WAP Forum's intent is to bring Internet content and advanced services to digital cellular phones and other wireless terminals. Their current approach is based on the GSM standard and a simplified version of HTML (HDML). Applications using WAP will be scaleable across a variety of transport options and device types.

Addison Wesley Longman Publishing, *One Jacob Way, Reading, MA 01867-3999; (781) 944-3700, www.awl.com/cseng/wirelessseries/*

Addison Wesley has recently introduced two books on wireless information systems:

Mobile IP - Design Principles and Practices, by Charles E. Perkins, introduces the IP-savvy reader to the design and implementation of wireless Internet protocols. He describes the technology behind mobile networking, focusing on the IETF's mobile IP protocol. Topics covered include mobile IP, route optimization, use of the dynamic host configuration protocol (DHCP), and encapsulation. **CIRCLE 502**

Wireless Multimedia Communications, by Ellen Kayata Wesel, is a comprehensive guide to understanding the design of wireless systems. Covering voice, video, and data communications, it provides an introduction to the problems and solutions of communicating multimedia traffic at high data rates over RF channels. **CIRCLE 503**

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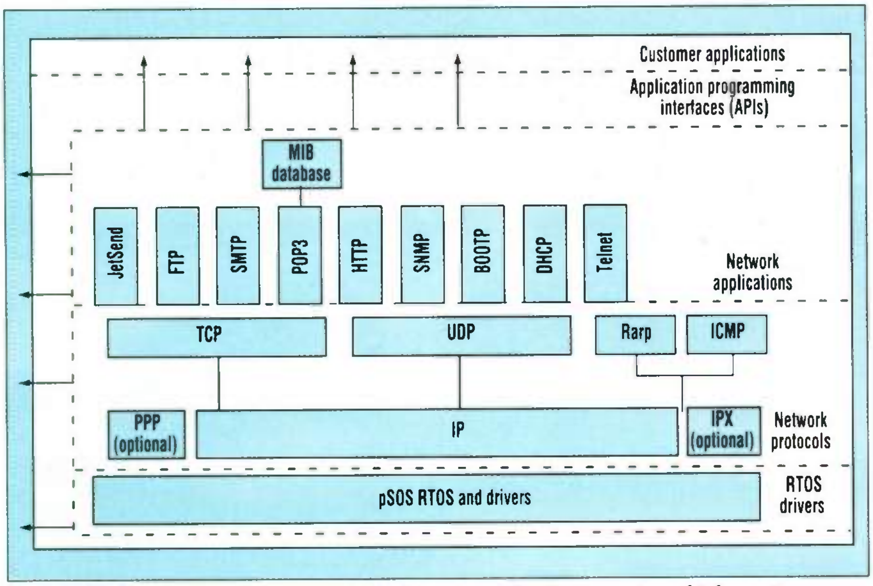


2. Embedded Internet engines can cut both the cost and development time of information appliances, thanks to their on-chip network interfaces, ROM-based protocol stacks, and network application software. Running under the control of a real-time operating system (RTOS), user applications can simplify mail, file transfer, management, and other well-defined network functions.

the pad could be equipped with a small camera to send pictures or video.

Going Wireless

These days, we need to get at information even when we're away from the wired infrastructure. That's where services like cellular, wireless local loop, and pager networks come in. In the past, options have been limited and slow, but that's changing rapidly with the introduction of digital cellular and PCs and proprietary services like the Ricochet Network. Even today's phones are beginning to offer direct data interfaces that can handle much faster bit rates than a modem-based connection. This is making it practical to send and receive e-mail, and exchange large files from a laptop, but it's only the beginning. John McQueen, a noted technology analyst, says that wireless phones are undergoing an evolution from relatively simple handsets to full-blown multimedia data appliances.

Brave New Phones

According to McQueen, the next generation of DSPs and controllers will be powerful enough to support PDA and web-browser functions, in addition to performing a myriad of tasks associated with establishing and maintaining a cellular connection. These new phones would most likely have a relatively large, high-resolution screen, that could be used to send and receive e-mail, as well as support an electronic scheduler, address book, and other PDA-type functions.

At this point, designers will have to include I/O (either electrical or IR) and software to facilitate file easy transfer and data synchronization between the phone and other devices.

With so many functions being crammed into a single package, there is the danger that the phone will become too bulky to be useful. For this reason, some manufacturers may choose to offer a two-piece solution, consisting of a PDA-like device and a compact phone which can be easily linked together to function as a wireless communicator. One of the first examples of this type of device is already available from Philips Electronics, Eindhoven, The Netherlands *(Fig.3)*.

Beyond transferring text and files, it is quite likely that these wireless phones will soon be capable of displaying web pages at speeds equal to or better than today's best analog ones. There is considerable interest in supporting some sort of abbreviated web-browsing capabilities over the small screens available in palmtop devices. Besides the web content, a properly equipped handset might have an embedded digital camera for transmission of images or even video.

Given the current cost of air time, cellular web browsing may or may not become a popular means of accessing information. If however, wireless providers offer discounted rates for data access, this could prove to be the "killer app" that would help them recover from the enormous expense of purchasing spectrum at PCS auctions.

3. This two-piece smart phone/PDA duo represents a different approach to mobile information appliances. The Trapeze PCS handset is a full-function phone with call control and voice-activated dialing. It can be connected to its companion unit, the Accent PDA, to form a wireless messaging unit. This unit can use its larger pen-based screen to send and receive faxes and e-mail, browse web sites, and download files from the Internet.

Standing between this vision of a multimedia phone and us are two nagging questions: How do you cram all that data onto a tiny screen, and what is the best format in which to transmit? Even as you read this, there are at least two groups which are hard at work on these very issues.

The simpler approach, known as the Wireless Access Protocol (WAP), is an attempt to put Internet access into today's phones with as little new technology as possible. Designed around the GSM cellular protocols, WAP will display web content using the Handheld Device Markup Language (HDML), a radically reduced subset of HTML which doesn't handle graphics well.

HDML is designed to work with today's LCDs, and not excessively tax the limited amount of processing power available in today's phones. Consequently, phones based on the WAP's proposed standards will be forced to read specially reduced versions of web pages which have all the color and most of the graphics stripped out. Despite its limitations, WAP is a quick interim solution, and it has already earned the support of at least four major cellular manufacturers and their strategic partners.

Taking a slightly longer-term view, the Mobile Internet Phone Services (MIPS) Forum is basing its vision of an Internet on technologies that should become available within the next 12 to 18 months. Their proposed technology would transmit web content, as well as downloadable applets using the Java language. This would allow MIPS to be deployed across many different wireless platforms including IS-95, IS-136, and GSM. John McQueen, founder and chairperson for the MIPS Forum, is confident that the next generation of low-power DSPs will have the 3-to-500 MIPS required to support execution of Java code in real-time.

New Homes For Pagers

Although cellular phones enjoy the bulk of the spotlight in the wireless arena, the pager and its associated technology will be finding its way into some of the most interesting applications. While pagers have relatively slow bit rates and cannot be used to transfer large files, they enjoy the advantages of being compact, inexpensive, and very power efficient. When you imagine a device which can receive short alphanumeric messages nearly anywhere in the world, with a bill-of-materials cost in the $10 range, the possibilities become quite intriguing.

According to Phil Hopkins, marketing and communications manager for Motorola's Wireless Products Group, pagers can deliver the services today that CDPD and PCS short messaging services are promising to do in the future—at a lower cost. The low price, compact volume, and nearly universal coverage means that it's no longer a risky proposition to embed a pager circuit on the mother board of a product. Since engineers can make use of mature pager products, and entrepreneurs can leverage a worldwide paging infrastructure, Hopkins expects that we will see pager technology turning up in many unusual places over the next year or two. For example, when pagers are embedded in PDAs and PC plug-in cards for laptops, users can receive near-instant paging and e-mail, even when their host devices are not turned on.

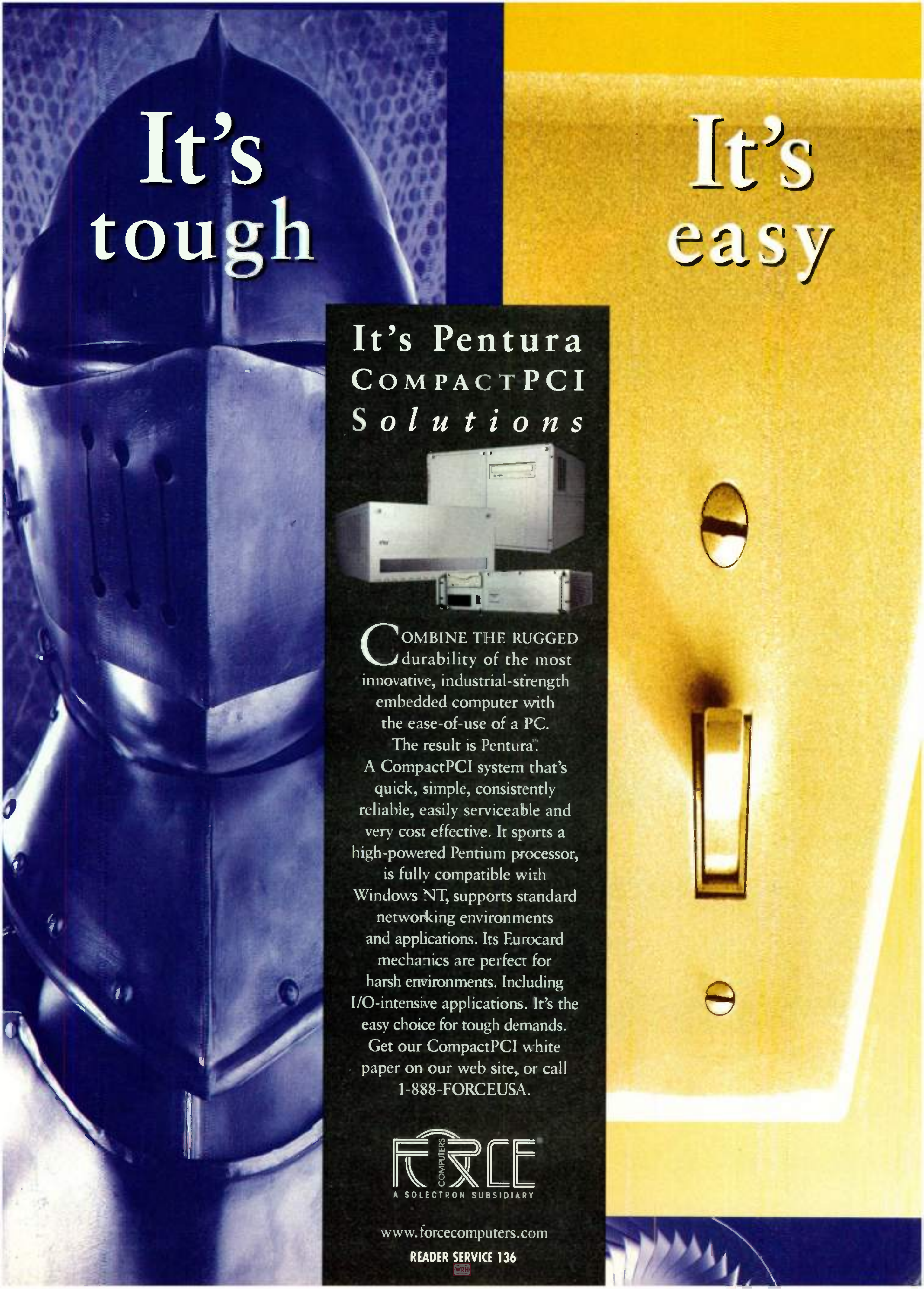
The ability to deliver relatively short messages to remote sites makes pager technology a reliable, low-cost means of updating outdoor electronic signs, either for advertising or highway messaging. With the addition of another layer of security, Edwards anticipates that a pager circuit embedded in a smart card will enable a bank to transmit credit from your account to your "electronic wallet," any time and any where you need it.

With the introduction of two-way messaging services, the possibilities become even more exciting. Currently, pager modules running the ReFLEX two-way protocol carry a $100 price tag, but chip sets should be available later this year for $20 to $30. Once this price barrier is crossed, we can expect to see them popping up in trucks and cars, providing enhanced security, navigation, and in-route information. In addition to providing an easy way to remotely read utility meters, two-way paging will enable vending machines and other unattended equipment to call for supplies or service.

Conclusions

It's anybody's guess where these trends will take us, but we can make a few educated prognostications about the near-term outlook. IA technologies are making it much easier not only to build intelligence into a product, but also to allow it to communicate with other devices across a variety of infrastructures. This powerful trend will most likely deliver the long-promised "universal information tool," either as a well-connected PDA or a very sophisticated mobile phone.

Perhaps the biggest impact however, will be in the invisible realm—meter reading, data capture, and industry automation—which benefits from a steady flow of information. One way or another, we're in for yet another big change in how we relate to information and how information comes to us.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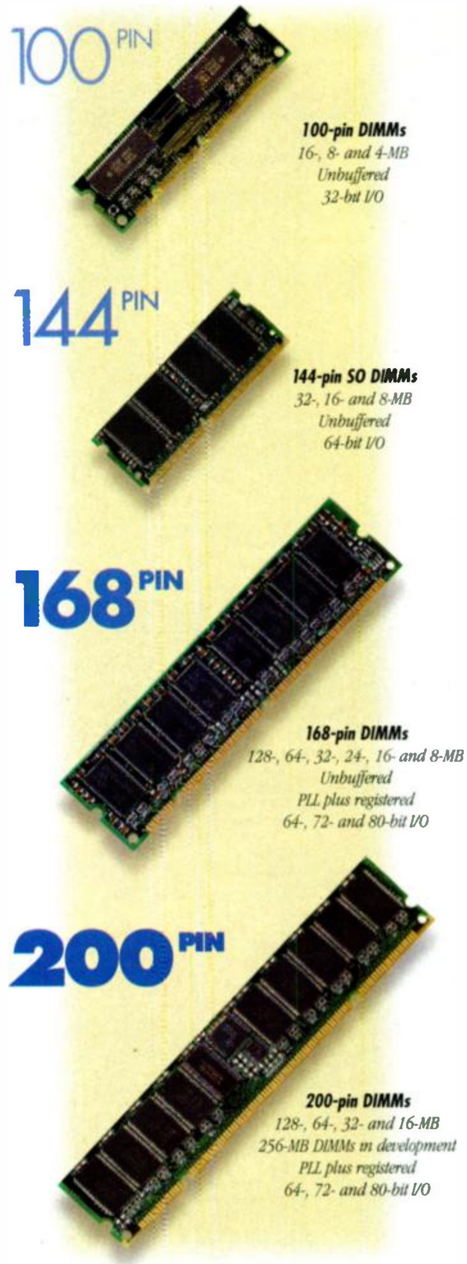

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Graphics-Optimized DRAMs Deliver Top-Notch Performance

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Dave Bursky

SPECIAL REPORT

In the world of graphics subsystems, there are three key specifications that are the cornerstones of system performance—speed, speed, and speed. Of course, other factors such as low cost, also play important roles in trying to deliver affordable graphics subsystems. These two, often contradictory, directions are actually merging as higher-performance demands are placed on the graphics subsystems and memory.

DRAM designers are developing new-architecture memories that can deliver the desired performance at economical prices. Such parts are now critical to system performance, as software applications increase in complexit, and the graphics controller is required to handle video files and animated 2D and 3D images for gaming and entertainment applications.

To achieve the higher levels of performance required, DRAM suppliers have crafted several generations of architectures that could be used for graphics. These memories range from standard, fast-page-mode DRAMs to the dual-ported video DRAMs to extended-data-out DRAMs, and to more radical new-generation architectures.

These new generation DRAMs include devices such as the Rambus RDRAM (which now includes the Direct RDRAM and concurrent RDRAM), the synchronous graphics RAM (SGRAM), and the soon-to-be-available double-data rate (DDR) SGRAM.

In terms of applications, it is estimated by Hyundai Electronics America that EDO DRAMs have about 10% of the graphics memory market, SGRAMs hold about 70%, RDRAMs about 10%, and other architectures take a total of about 10% (*Fig. 1*). Along the way, several other architectures that did not achieve mainstream acceptance were put into use in small-volume applications. These include a specialty triple-port DRAM developed by NEC, a multibank DRAM developed by Mosys (the MDRAM), the cache DRAM (two versions, one developed by Mitsubishi and the other by Ramtron which is now Enhanced Memory Systems), and the Window RAM developed by Samsung. Of these, the Window RAM has garnered some interest, but it is a sole-sourced device, and the MDRAM has been designed into a few graphics subsystems.

Art Courtesy: Micron Technololgy

Some high-performance graphics workstation vendors also have attempted to craft their own memories that were sized and designed to specifically match their graphics workstations. For example Sun Microsystems, in conjunction with Mitsubishi, designed a unique graphics DRAM for their high-end graphics workstations.

Besides the evolving memory architecture, graphics controllers have been widening their frame-buffer interfaces. Gone for the most part are the days of 32-bit-wide buses between the controller and graphics buffer memory. Most of today's graphics controllers employ a 64-bit-wide bus (and a few use even wider buses—128 to 192 bits) to move more data on every bus cycle, and those bus cycles are shrinking as well. Bus speeds of 50 MHz—typical of chips just a year or two ago—are now considered lethargic as new memories allow data transfers at 83 to 125 MHz.

The need for high performance also holds true in portable computing, but there's one additional constraint: The system also must operate at low power consumption levels. To accomplish these goals, many portable graphics chip suppliers have started to integrate the DRAM (embedded DRAM) and the graphics controller on the same chip. This approach greatly reduces power consumption and allows designers to achieve performance levels comparable to any desktop graphics controller, at costs approaching those of the multichip desktop solution (typically between $35 and $50/chip in volume) *(see "Embedding the DRAM", p. 94)*.

For the high end of the controller market, some chips with 128-bit-wide buses have started to appear, allowing twice as much data to move on every bus cycle. However, such wide buses really put the spotlight on one of the key memory issues in graphics: memory granularity.

Most graphics adapters and motherboard-based subsystems are shipped with a base-line amount of memory. They handle most PC resolution modes of 640 by 480, 800 by 600, 1024 by 768 pixels, and a few with 1280 by 1024 or 1600 by 1200-pixel capability. Many popular graphics cards and computers with graphics subsystems on the motherboard come with a 2-Mbyte frame buffer. This size is sufficient to handle the first three modes and permit the first two modes to display true color, while limiting the higher-resolution modes to 256 k or fewer colors. Often the boards can be upgraded with an additional 2 Mbytes, a size sufficient to provide true-color capability at most popular higher-resolution levels.

However, unlike main memory systems where memory capacity usually follows the thinking of "The larger the better," graphics systems will usually top out at 4 to 8 Mbytes. That upper limit often presents a problem if designers are using standard DRAMs, which usually aren't manufactured with word widths larger than 16 bits. Assuming in today's market that 4-Mbit memories are available with 8-bit data paths, eight devices would be required to implement a 4-Mbyte frame buffer. But, a 2-Mbyte frame buffer would not be possible because the granularity (512 kwords by 8 bits) will not allow shallower buffers.

As denser memories become available, they would have to be organized with wider word sizes for a better fit. With 16-Mbit DRAMs, that has started to happen. There are several by-16 DRAMs available, and they provide designers with a 1-Mword by 16-bit organization that allows an 8-Mbyte buffer to be built with four chips. However, for many applications, 8 Mbytes is overkill.

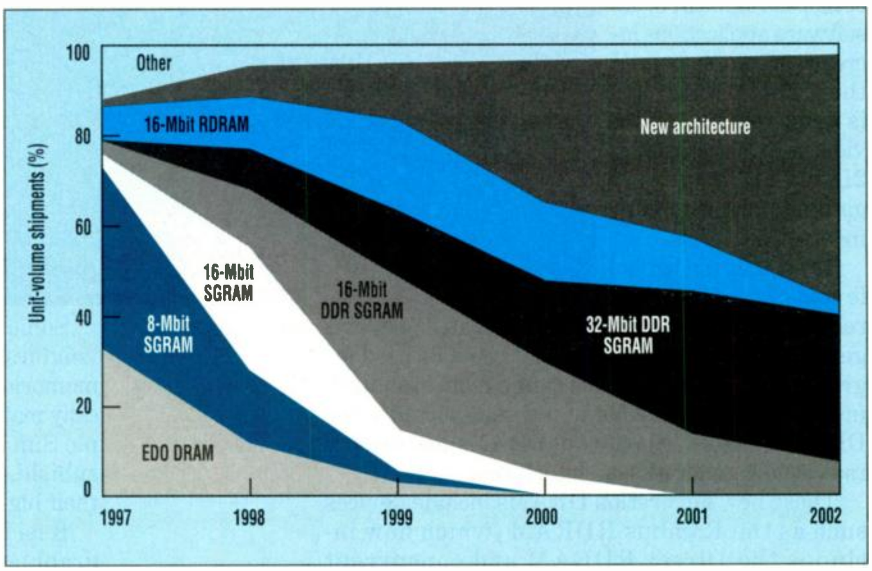
To solve that problem, memory designers have taken three approaches: Increase the memory's data bus width to 32 bits so just two chips are needed to form a 2- or 4-Mbyte buffer; reduce the memory capacity to an in-between level of 8 Mbits (512 kwords by 16 bits, or 256 kwords by 32 bits) so that a 4-Mbyte buffer can be implemented with four or two chips; or move to a totally different architecture such as the RDRAM.

Currently available RDRAMs employ a byte-serial interface, but later this year a 16-bit word-serial interface will become available (the Direct RDRAM). The RDRAM interface would allow systems to use just a single 16-Mbit RDRAM to form a 2-Mbyte buffer, or two chips to form a 4-Mbyte buffer. Unlike the wide-word DRAMs that require a 16-bit or 32-bit data bus and tie into a graphics controller that also has a wide data bus, the RDRAM interface requires fewer data lines. It only needs 8 or 16 lines to carry the data, and another half-dozen or so control signals. That would allow the RDRAM to be housed in a lower pin-count package than the 16- or 32-bit DRAMs. It also would considerably reduce the pin count on the graphics controller, lowering its cost. Or, to improve the controller's bandwidth, a second RDRAM interface could be integrated into the controller, providing a second high-speed data channel.

For several years, the workhorse graphics memory architecture was the video RAM—a dual-ported DRAM that allows independent writes and reads to the RAM from either port. The host port was a standard random-access port, while the graphics port was optimized for bursting data to the graphics subsystem through a pair of small parallel-to-byte-serial shift registers. However, the extra area on the chip required by the shift registers and control circuits increased VRAM manufacturing costs, leading to a 30% to 50% price premium over standard DRAMs.

Changing Of The Guard

The advent of higher-performance DRAMs with EDO capability and then the rapid rise of synchronous DRAM (SDRAM) architectures has basically



1. With the latest changes in graphics performance requirements, the need for different architecture memories has led to a fracturing of the memory market. This graph, developed by Hyundai, shows the percentage of unit-volume shipments for each popular type of memory used in graphics subsystems.

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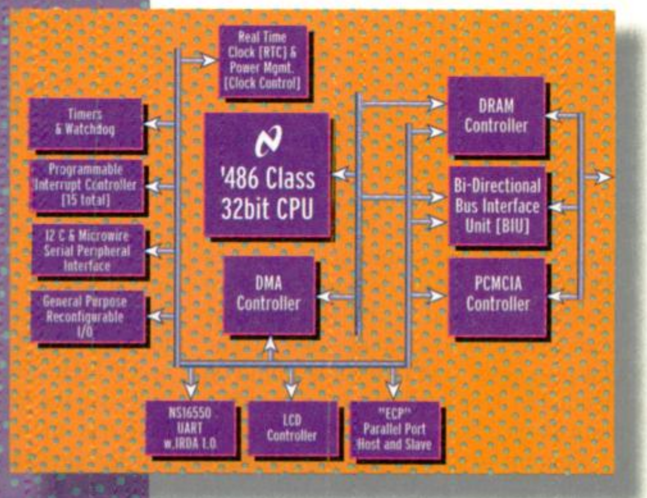

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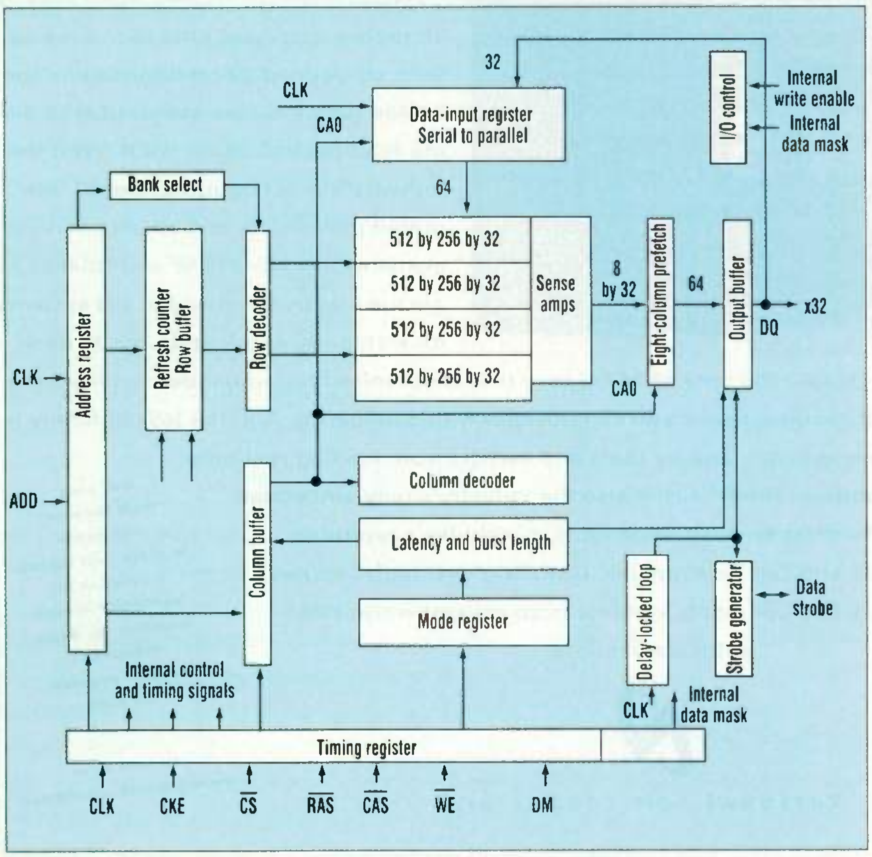
closed the door for new designs based on the VRAM architecture. At the same time, these new developments have cleared a path for synchronous graphics DRAMs (SGRAMs). And just about every supplier of synchronous DRAMs will be offering an SGRAM.

SGRAMs are very similar to the standard SDRAM, except that they have several additional functions that improve their effectiveness in graphics systems. Both Block-Write and Write-Per-Bit functions have been added to make the reading and writing of data faster and more efficient. These features are selected through the use of special mode registers and additional command pins that can be loaded with the appropriate information.

First-generation SGRAMs are 8-Mbit devices that come organized as 256-kword by 32-bit devices. They are typically housed in 100-lead thin or standard thickness, quad-sided, plastic flat packages. Just two chips would be needed to form a 2-Mbyte frame buffer for a 64-bit graphics controller.

Second-generation, 16-Mbit SGRAMs are now starting to appear from most SGRAM suppliers. These devices double the word depth, permitting a 4-Mbyte buffer to be built with just two chips. Coming later this year are higher-speed versions that will offer designers two approaches to get better throughput: higher clock speeds or DDR data transfers. Memory designers are even toying with a 64-bit-wide single-chip SGRAM, but thus far no company has committed to fabricating such a chip.

Most of today's 8-Mbit SGRAMs are available with data clock speeds of 83 or 100 MHz. By the second half of this year, most SGRAM suppliers will offer 125 MHz, and possibly 143 MHz versions of the memories. However, for the 16-Mbit generation, designers have started implementing the same approach used with SDRAMs. They use both edges of the clock to effectively double the data transfer rate. Therefore, a 100-MHz clock will transfer data at 200 MHz rates. These DDR versions will push the graphics bandwidth for an SGRAM up to 800 Mbytes/s (peak), allowing the graphics system to deliver top-notch performance.



2. Offering the highest data rate for a synchronous graphics DRAM, 300 Mbits/s on each I/O pin, this four-bank, 16-Mbit SGRAM developed by IBM Microelectronics delivers a peak data-transfer bandwidth of 1.2 Gbytes/s.

The high bus speeds of the SGRAMs could easily present some challenging system design problems due to noise and reflections. However, because the chips are often located in very close proximity to the controller, the high bus speeds, coupled with low-voltage TTL interfaces, should not cause any signal quality problems.

On the other hand, at bus speeds of 125 MHz and above, designers are seriously studying, and in some cases implementing, interfaces using series-stub-terminated logic, version 2 (SSTL-2). The SSTL-2 interface will be able to readily handle the 143-MHz and higher bus speeds (166 and 180 MHz) that designers at the DRAM suppliers expect to make available for future graphics subsystems.

One of the fastest parts to date, with a top clock speed of 150 MHz, is a 16-Mbit DDR SGRAM developed by IBM. Delivering the highest throughput of any available SGRAM, 300 Mbits/s for each data pin, it achieves a peak data rate over the 32-bit bus of 1.2 Gbytes/s. The 512-kword by 32-bit memory employs SSTL-2-compatible input and output buffers, and operates from a 3.3-V supply. The SSTL signal levels start with a center reference level of 1.25 V above ground, and have input high and input low (V_{IH} and V_{IL}) dc levels of V_{REF} ±0.18 V, and ac levels of V_{REF} ±0.35 V. Once an input signal passes those levels, it changes and maintains the new state.

Internally, the SGRAM is organized as a quad-bank device with four 128-kword by 32-bit blocks that share a synchronous interface (all signals are registered on the positive edge of the clock signal). Additionally, the DQ and DQ-Mask functions are registered at the 50% point between two successive clocks. Reads and writes have burst lengths of 2, 4, or 8 locations. A data-strobe signal is available to assist in reading data on each clock edge. The memory also has a 16-column Block-Write function and Write-Per-Bit capability, each of which can be combined with the individual byte-enable lines, DM0-DM3 *(Fig. 2)*.

Most other SGRAM designs have adopted a dual-bank approach to the internal architecture for 8- and 16-Mbit single-data-rate SGRAMs. Etron, Fujitsu, Hitachi, Hyundai, Micron, Mit-

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Embedding The DRAM

Although graphics controllers have achieved impressive gains in performance through the addition of 64-bit-wide interfaces to the off-chip frame buffer, the wide bus and high-speed signal switching cause the graphics subsystem to eat up power. For desktop systems, a few watts of power consumption for the entire subsystem might be tolerable, however for portable units it must be reduced. But, it must be done without any compromise in graphics performance. The solution: Get rid of the wide off-chip buses by embedding the frame buffer memory right onto the graphics controller chip.

Today there are more than six graphics chip suppliers that have done just that. NeoMagic Inc., Santa Clara, Calif., laid the foundation for the innovative use of the embedded memory by taking advantage of the merged architecture. Not only does the approach eliminate the wide external buses and the one or two off-chip DRAMs needed for the frame buffer, but it allows designers to innovate by actually using even wider buses on the chip to connect the memory to the controller. In fact, the latest-generation controllers from NeoMagic and the other suppliers use a 128-bit-wide memory bus for data transfers.

Such a wide bus allows the rapid transfer of graphics data from the memory to the controller, allowing the controller to deliver top-notch graphics performance. Because wide buses can be easily implemented on the chip, designers can dramatically reduce power consumption. Additionally, the size of the graphics memory can be optimized for the desired resolution modes that the controller will generate.

Although the integrated combination of the memory and controller is not always a cost reduction if the cost of individual components is added up (controller plus memory versus integrated controller), the architectural options offered by the merger allows designers to offer unique features or capabilities that the discrete solution doesn't. Additionally, because the wide external buses are eliminated, the package pin count is much lower, and the chip's power consumption is much lower than that of the multichip subsystem.

First- and second-generation merged controllers have employed basic DRAM architectures such as fast-page mode and EDO-style DRAM cores. However the latest generation controllers are employing synchronous DRAM cores for additional performance improvements. Further architectural enhancements between the graphics accelerator and the memory include the merging of logic functions into the memory cells to achieve better integration and high throughput.

One such development, detailed at this year's IEEE International Solid-State Circuits Conference, was jointly developed by Accelerix Inc., Ottawa, Ontario, Canada; Mosaid Technologies Inc., Kanata, Ontario, Canada; and Symbionics Ltd., Cambridge, U.K. The integrated graphics accelerator and frame buffer packs 13.4 Mbits of memory and has an internal transfer rate of 33 Gbytes/s. To achieve such a high rate, its designers integrated part of the graphics processor within the DRAM. The pixel processing unit and serial output registers are integrated into the DRAM architecture, pushing the bus width between the DRAM frame buffer and the processor to 4096 bits.

To merge the logic into the DRAM layout, the chip's designers had to pitch-match (size the logic functions so that they fit within, or match, the cell-to-cell spacing of the memory cells) the logic functions so that they don't disrupt the layout design of the memory array. That technique does restrict the complexity of the pixel processing logic to only the most basic pixel operations and raster processing functions. The pitch matching, however, allows the logic to be implemented with the aggressive design rules used by the memory array, keeping the area required by the logic to a minimum.

That design allows the frame buffer to accelerate some of the most basic graphics operations. For instance, a block move can require a source pixel read, a destination pixel read, a raster operation, and a destination pixel write. In a typical system with a 64-bit memory interface, this is done 64 bits at a time. With this new architecture, all reads and writes are done 4096 bits at a time.

The new Chips and Technologies subsidiary of Intel Corp., San Jose, Calif., has also started to sample a graphics controller with 16 Mbits of embedded DRAM. The HiQVideo 69000 chip contains 2 Mbytes of integrated synchronous DRAM for the graphics/video frame buffer that can support operations at data transfer rates of up to 83 MHz. The chip consumes just 650 mW when powered by a 3.3-V supply. The large on-chip memory allows the chip to support color displays of 1024 by 768 pixels with up to 16 bits per pixel, and 800 by 600 pixel displays with 24 bits per pixel for the color depth. Support for 16:9 aspect-ratio flat-panel displays is also included.

Also included on the controller are circuits that support multimedia applications—a digital YUV to RGB converter and scaling circuits that continuously scale the data with horizontal and vertical interpolation. The controller also includes the company's proprietary temporal modulated energy distribution (TMED) algorithm. TMED allows the display of 16.7 million true colors on low-cost STN liquid-crystal display panels without using frame-rate control or dithering techniques. The algorithm eliminates all of the flaws (such as shimmer, Mach banding, and other motion artifacts) normally associated with dithering and frame-rate control.

Additional suppliers of integrated DRAM/graphics controller chips include Silicon Motion Inc., San Jose, Calif.; Silicon Magic Corp., Santa Clara, Calif.; Trident Microsystems Inc., Mountain View, Calif.; and ATI Technologies Ltd., Thornhill, Ontario, Canada. Still more are in development. For instance, Micron Technology Inc., Boise, Idaho, is working with potential partners to leverage its DRAM manufacturing capability and jointly design a graphics controller that might appear in early 1999.

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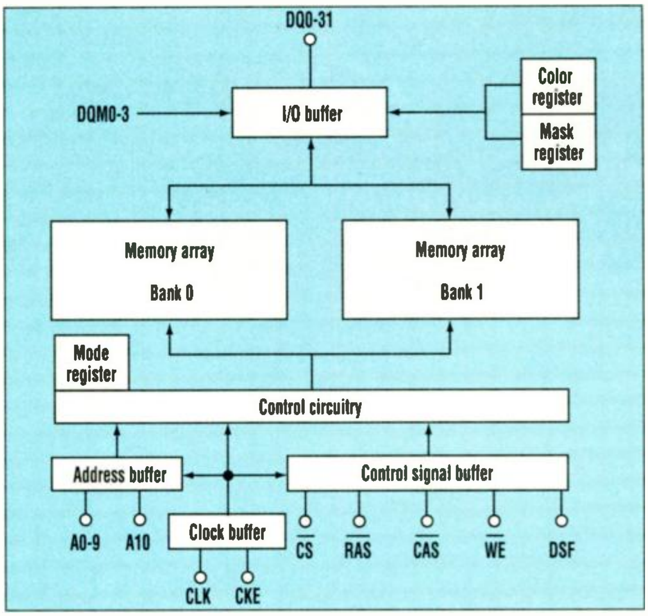
subishi, Mosys, NEC, Samsung, Siemens, and others, are all sampling or producing single-data-rate devices. Just about all of them are getting their DDR implementations ready for sampling. The dual-bank structure of Mitsubishi's 16-Mbit SGRAM is typical of all the dual-bank SGRAMs offerings from almost a dozen suppliers *(Fig. 3)*.



3. This simplified diagram of a dual-bank, 16-Mbit SGRAM from Mitsubishi has a structure very similar to that of a standard synchronous DRAM. However, included in the SGRAM are individual byte control signals, write-per-bit and burst-write capabilities, and extra internal registers to handle graphics operations.

In general, SGRAMs behave much like SDRAMs in that all input signals are registered on the positive edge of the clock, and data can be written or read in bursts of 1, 2, 4, or 8 bits, or a full page. Once a row is activated, only the starting column address for each burst is required. An internal counter increments the column address for all the locations after the first in a burst transfer. When the read or write parameters are configured, the memory continues through the entire burst until completion or interruption with new data being presented or accepted on each cycle of the burst. To switch to a new row, the current row must be precharged. Then, the new row may be activated.

SGRAMs have many programmable features that designers must have the system configure during both system initialization and graphics operations. Through a small command interpreter on the chip, the burst length, the column-address-strobe latency, the Write-Per-Bit modes, 8-column Block-Write, and the color register can be set to desired initial values and altered if system conditions change.

Although EDO DRAMs and a few VRAMs are still used in about 10% of all the graphics systems shipped, virtually no new designs are done with those chips today. The SGRAM is currently the most popular device, and is used in about 70% of all graphics systems. The remaining 20% of the graphics market is fragmented, with the RDRAM and Window RAM (WRAM) probably accounting for the majority of sockets. Otherwise, a few designs are still using MDRAMs or other memories.

With its popularity on the rise, the RDRAM in its latest incarnation, the Direct RDRAM, provides a low-overhead, high-speed memory that can be used very easily in graphics applications. Offering double the word width of the original RDRAMs, the Direct RDRAMs come in either a 16- or 18-bit (two extra bits for parity or data) wide organization. They are either 2 or 4 Mwords deep, for a total storage capacity of 32/36 or 64/72 Mbits on a chip.

This advanced version of the Direct RDRAM will be ready for sampling later this year. It will offer data-transfers of 1200 to 1600 Mbytes/s (600- and 800-MHz bus clock rates, respectively). To achieve that, the chips will employ low-lead-inductance, chip-scale packages, and will use Rambus signaling-level (RSL) technology to transfer data.

The internal multibank architecture of the RDRAMs allows the highest sustained bandwidth for multiple, randomly addressed memory transactions. Internally, the memory's 16 storage banks allow the chip to support up to four simultaneous transactions at rates of 1.25 ns for every two-byte transfer *(Fig. 4)*. The chips also have been designed to minimize access latencies. An on-chip write buffer allows data to be written, then lets the host move on to other tasks. Three precharge mechanisms give the memory controller a lot of operating flexibility. The ability to interleave transactions also helps improve data-transfer operations.

In addition to its high data-transfer rates, the Direct RDRAMs are also power smart. Advanced power-management modes allow them to tailor power consumption to minimize power drain during operation. Direct RDRAMs feature six modes ranging from basic power down with just the self-refresh operation active, to modes in which various portions of the chip are powered down and other portions are standing by for control signal inputs.

The Concurrent RDRAM alternative performs two bank operations simultaneously to allow high transfer rates using interleaved transactions. Such memories will operate with bus speeds of 600 MHz, achieving data-transfer speeds of up to 1.2 Gbytes/s.

Memory designers estimate that the Concurrent RDRAM will deliver about a 15% performance increase over the original RDRAM in graphics, video, and many other applications. Concurrent RDRAMs will be available in 16/18- and 64/72-Mbit densities with an 8- or 9-bit word width. Latencies can be kept low by operating the two or four 1-kbyte or 2-kbyte sense amplifiers as high-speed caches, and by using the random-access mode (page mode) to facilitate large block transfers.

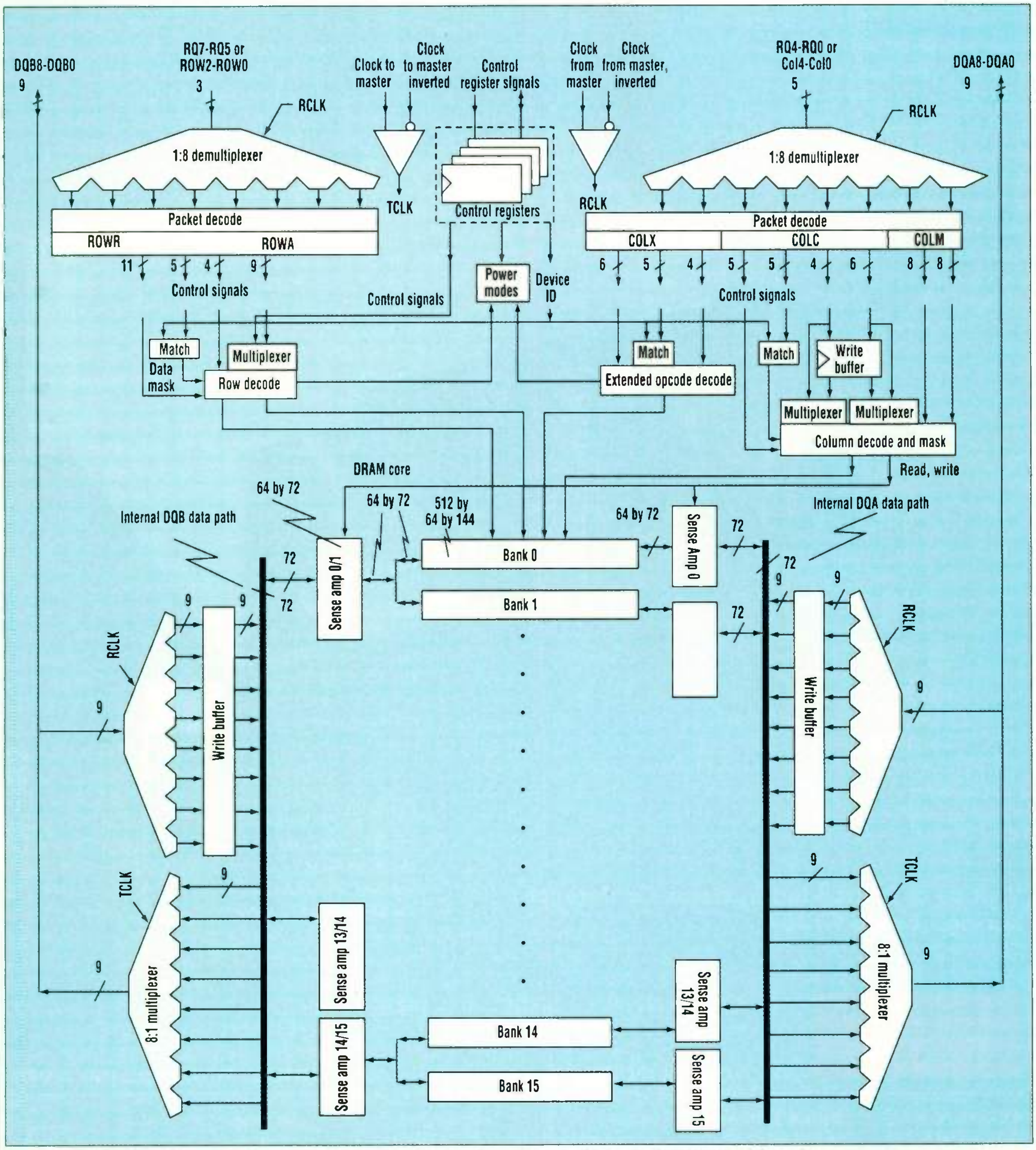
Other alternatives for graphics systems such as the WRAM, MDRAM, and cache DRAM provide designers with single-point solutions for specific graphics applications. Over the last year or two, the speed of most mid-range and high-end graphics subsystems has gone well beyond the speed achievable with systems based on the WRAM. WRAM delivers a peak data bandwidth of about 200 Mbytes/s, about half that achievable with the lowest-speed grade of SGRAM (83 MHz). Armed with the latest process developments, designers at Samsung expect to crank up the performance one more time to give designers a cost-effective solution for the entry-level systems.

The dual-ported WRAM has seen some moderate success as a single-chip frame buffer. Besides its 16-bit word-serial video port, the KM4232W259A

WRAM packs dual 128-byte split serial registers. These registers are fed by a 256-bit-wide internal bus from the main memory array, providing the chip with an internal data-transfer capability of 2.1 Gbytes/s when bursting data to the video output registers. The word-serial output, though, can be transferred at a maximum clock speed of 100 MHz (10-ns access time) to the display controller.

On the chip are scroll and aligned block-move graphic operations. Aligned bit-block transfers occur at up to 640 Mbytes/s, and feed the video port the data transfer bandwidth of 200 Mbytes/s when clocked at 100 MHz.

Also finding a home as a high-speed frame-buffer memory, the MDRAM developed by Mosys offers a multibank architecture capable of delivering a 666-Mbyte/s data transfer rate over its 32-bit-wide interface. The MD9xx series of MDRAMs are enhanced synchronous DRAMs that have short la-



4. The 16-bank architecture of the direct RDRAM developed by Rambus allows the high-speed memory to deliver data to a graphics system at rates of up to 1.6 Gbytes/s. The chip packs a 16-/18-bit data bus, and can handle four simultaneous transactions within the memory array.

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tencies, and support burst lengths ranging from 4 to 128 bytes.

An MDRAM can be viewed as an array of many independent 256-kbit (32-kbyte) DRAMs, each with a 32-bit interface, connected to a common internal bus. The external 32-bit bus is a buffered extension to the internal bus as seen through a bus repeater. The independence of the banks facilitates overlapping, or "hiding" the row-address-strobe access and precharge penalties, so that the average access times will approach the column-address-strobe access time.

Even cache DRAMs are finding homes in graphics systems—but not as frame buffers. Instead, they are being applied in 3D graphics systems for use as texture memory support. For example, the recently released 1-Mword by 16-bit enhanced SDRAM from Enhanced Memory Systems combines two banks (8 Mbits each) of fast 30-ns DRAM with two banks (4 kbits each) of 12-ns SRAM-based row register cache. The cache improves the initial memory latency when compared to standard SDRAMs, and can perform synchronous burst reads or data writes at speeds of up to 133 MHz. The memory can have two-row register pages. Up to two DRAM pages open simultaneously to maximize data transfer rates.

On a page miss, the DRAM bank is activated and data is read to the DRAM sense amplifiers. On the read command, the entire row of data is latched into the SRAM row register, and the specified starting address is output following the column-address-strobe (CAS) latency. The architecture allows a short initial latency to data in either of the two row registers on page hits. Since the row data is latched separately from the DRAM sense amplifiers, the ESDRAM can perform early auto or manual precharge once the row is latched to minimize page miss latency on the next random access.

The many memory types from which designers can select gives them a wide choice of trade-offs with which they can create cost- and performance-optimized systems. Additionally, design creativity won't stop here. Memory designers are working on next-generation architectures that will deliver data bandwidths greater than 2 Gbytes/s—a necessity for high-performance 3D graphics.

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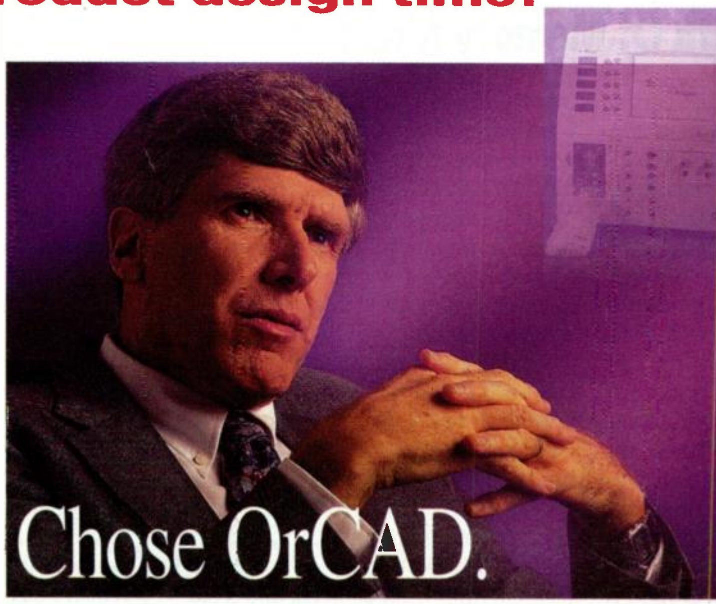

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Brian Murphy, Ph.D.
Associate Director of R&D,
Alcon Laboratories
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UPDATE ON MEMORY CARDS

MultiMediaCard: A New Direction In The Migration Path Of Memory Modules

PC cards (formerly PCMCIA cards) are famous for their roles in laptop and notebook computers. However, they suffer from a drawback that has limited their use on a wider scale. They're not suitable for plugging into mobile telephones because the connectors and cards would make a mobile telephone bigger and more expensive. On the other hand, another theoretical solution is the chip card. ICs in chip cards are very limited in size, minimizing the amount of memory they can hold. This smaller chip size, needed to prevent the chip from breaking, limits the maximum dimension of the die to 25 mm^2. Siemens Semiconductors, Munich, Germany, has now developed a new mass memory standard dubbed MultiMediaCard (MMC), which might alleviate both drawbacks. About the size of a postage stamp, this memory card, with a new form factor, is available in very inexpensive ROM and flash-EEPROM versions.

To ensure the MMC's media compatibility, Siemens has set up strategic partnerships with companies in the semiconductor, mobile communications, and PDA sectors. Siemens' goal is to establish a MultiMediaCard Association which actively supports the MMC standard and assures conformance to its specifications. LM Ericsson, Nokia, Motorola, Qualcomm, and Siemens PN (the Private Networks group which is active in the PBX, telephone handset, and GSM telephone business) have already announced that they will use the MMC in future generations of their products. In fact, it is quite likely that at the CeBIT show, the first GSM cellular telephones with an MMC interface will become available.

All these companies see the MMC as an attractive and inexpensive solution. While the costs for an MMC connector are less than $0.45, the potential to bring added value into the telephone is what excites them the most. Siemens, which knows that cellular telephones are very cost-sensitive, however, has a very aggressive cost roadmap in its product plans. "While the cost/Mbyte in a ROM MMC is today around $2.00, it will decrease to $0.80 cents/Mbyte within one year," says Christine Born, MMC marketing manager at Siemens.

MMC technology, which is optimized for mass-memory applications in serial systems, has a theoretically unlimited data-transfer rate. But, because it is controlled by software with a single bit, most likely, data transfers will not exceed 100 Mbits/s, and in more common applications 20 Mbits/s. According to Born, a Windows CE platform for MMC has been shipping as of early this year.

The MMC is specified for a supply voltage between 2 and 3.6 V, and a normal clock rate between dc and 20 MHz *(see the table)*. At 20 MHz and a 3.3-V supply, a ROM MMC consumes just 10 mW, which decreases to an average of 1 mW at 100 kHz.

Due to its serial structure, Siemens sees many applications for the MMC. A MMC ROM version, for example, is well-suited for dictionaries, software distribution, music players, toys, navigation tools, etc. MMCs have the potential to become the equivalent of the CD-ROM for the handheld computing market. For MMCs with flash memories, the majority of applications will be found in still images, music and speech recorders, and personal address books.

Siemens will manufacture the ROM version first, and a flash version in the future. SanDisk also plans to manufacture a flash model. Presently, the ROM-based Siemens MMC is available with storage capacities of 2 Mbytes; 8-Mbyte versions will be launched this quarter. A 32-Mbyte version is expected to be added within a year. In addition, Siemens is scheduled to launch a 128-Mbyte MMC in 2001. SanDisk will start shipping 2-, 4-, 8-, and 10-Mbyte MMCs this quarter as well *(Fig 1)*.

1. A MultiMediaCard (MMC) like these two from SanDisk, is about the size of a postage stamp. A concept developed by Siemens Semiconductor, it's supposed to fill the gap between PC cards and chip cards.

Because the MMC is software-addressable, many cards can be placed on a little pile and connected in parallel. The card required is then selected by software— a feature making multislot applications very easy. To allow software addressability, every MMC has a unique card number, the so-called CID.

The basis for Siemens' ROM MMCs is a 3D memory process that's said to double memory density compared to standard ROM processes. "Using the same process with the same minimum feature sizes, Siemens' 3D ROM memory cell architecture allows the integration of ROM on a chip half the size, at half the price," Born says *(Fig. 2)*.

With its power consumption of 1 mW at 100 kHz, and its variable supply voltage, the MMC is well-suited for battery-operated devices. To allow its use in many different applications, the MMC's read data rate is variable between 0 and a maximum of 20 Mbit/s.

The MMC has a serial synchronous interface that allows several cards to be operated simultaneously by connecting the card's connector pads via an MMC bus. The bus implementation allows the coverage of applications from low-cost to fast-data-transfer systems. The single-master bus includes a variable number of slaves.

An MMC bus master controls the entire bus, and each slave unit is physically a single MMC—perhaps with different memory technologies like ROM or flash. Each slave has its own controlling unit to perform data transfers. Furthermore, the MMC master also includes power connections for MMC slaves. The bus uses a dedicated protocol, the MMC bus protocol, which is applicable for both read-only and writable devices. As a result, the payload transfer between the host and the cards can be bidirectional.

The MMC bus architecture requires all cards to be connected to the same set of lines. No card may be individually connected to the host or other devices,

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SPECIFICATIONS FOR SIEMENS' MULTIMEDIACARD

Parameter	Value
Electrical	
Operating-voltage range	2.0 to 3.6 V
Power consumption, at 20 MHz/100kHz/standby	<20 mW/<1.0 mW/<0.1 mW
Serial data rate	Up to 20 Mbits/s
Access time	<3 µs
ESD protection	±4 kV
Logical	
Storage capacity	2, 4, 8, and 10 Mbytes currently (256 Mbytes to come)
Operating modes	Card ID mode to identify cards Data-transfer mode for high-speed data transport
Data rate for read, write	20 Mbits/s, 1.6 Mbits/s
Stackability	Suppprts up to 30 cards on a single bus via MMC bus
Mechanical	
Card size	24 by 32 by 1.4 mm
Number of connector pads	7
Insertion/removal endurance	10,000 cycles
Ambient operating temperature	-20 to 85°C
Ambient storage temperature	-40 to 85°C
Chip technology	ROM/flash-EEPROM

thereby reducing connection costs.

There are three power-supply busline groups: V_{SS1} and V_{SS2}, V_{DD}, V_{PP}. They supply the cards' data-transfer and clock signals. While V_{DD} is the power supply line for all cards, V_{SS1} and V_{SS2} are ground lines. V_{PP} provides a programming voltage.

After a power-on reset, the host initializes the cards by a special message-based MMC bus protocol. Each message is represented by one of three tokens: command, response, and data.

A command token starts an operation with a command sent from the host to either a single card (addressed command) or all connected cards (broadcast command). All commands are transferred serially via the command line.

A response is sent from an addressed card or (synchronously) from all connected cards to the host to answer a previously received command. All responses are also transferred serially via the command line. Data can be sent from the card to the host or vice versa. All data are transferred via the data line.

A single data transfer is called an MMC bus operation. All addressed operations always contain a command and a response token. Some operations also have a data token, but others transfer information directly within the command or response structure. In this case, no data token is present in an operation. Bits on the data and command lines are transferred synchronously to the host clock.

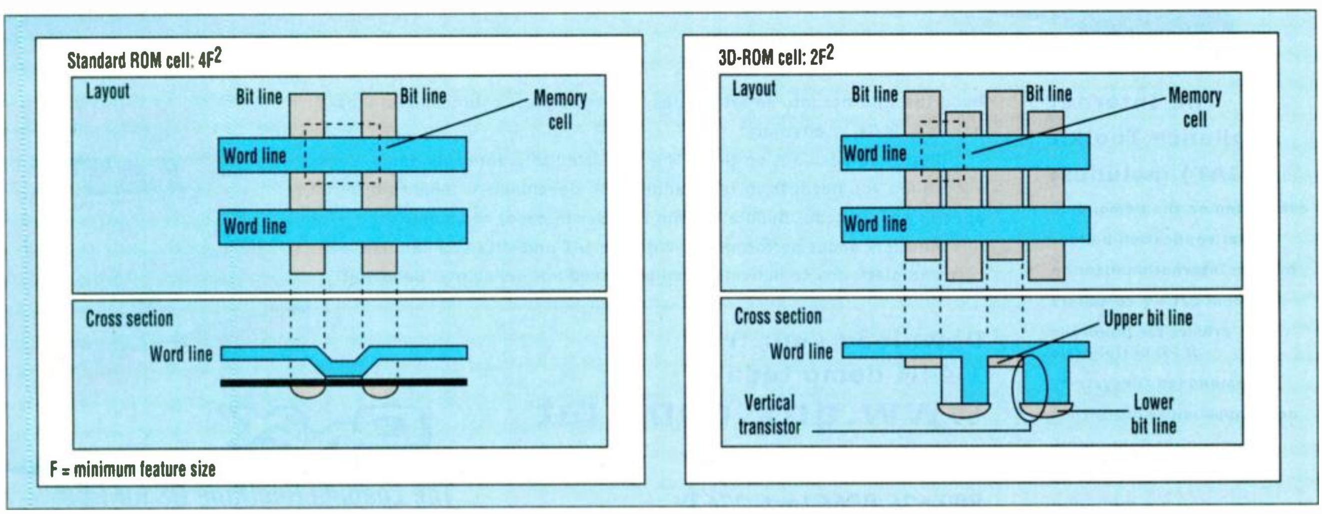
Siemens has defined two types of data-transfer commands: sequential and block-oriented commands. Sequential commands start a continuous data stream, which is only terminated by a new command following on the command line. This mode reduces the command overhead to an absolute minimum. Block-oriented commands send a data block followed by CRC bits. Both read and write operations allow the transmission of single or multiple blocks. A multiple block transmission is terminated when a new command follows on the command line. Each command token is protected by CRC bits to enable detection of transmission errors. Generally, hot insertions and removals are allowed. As data transfer operations are protected by CRC codes, bit changes resulting from insertion/removal can be detected by the MMC bus master.

Development Tool

To introduce potential designers to the MMC world and to allow testing, debugging, and development of MMC-based applications, Siemens offers MMC Explorer, which runs in Windows 96/NT. It can view the file system of the MMC and start applications. Cards can be initialized, read, erased, and written within it as well.

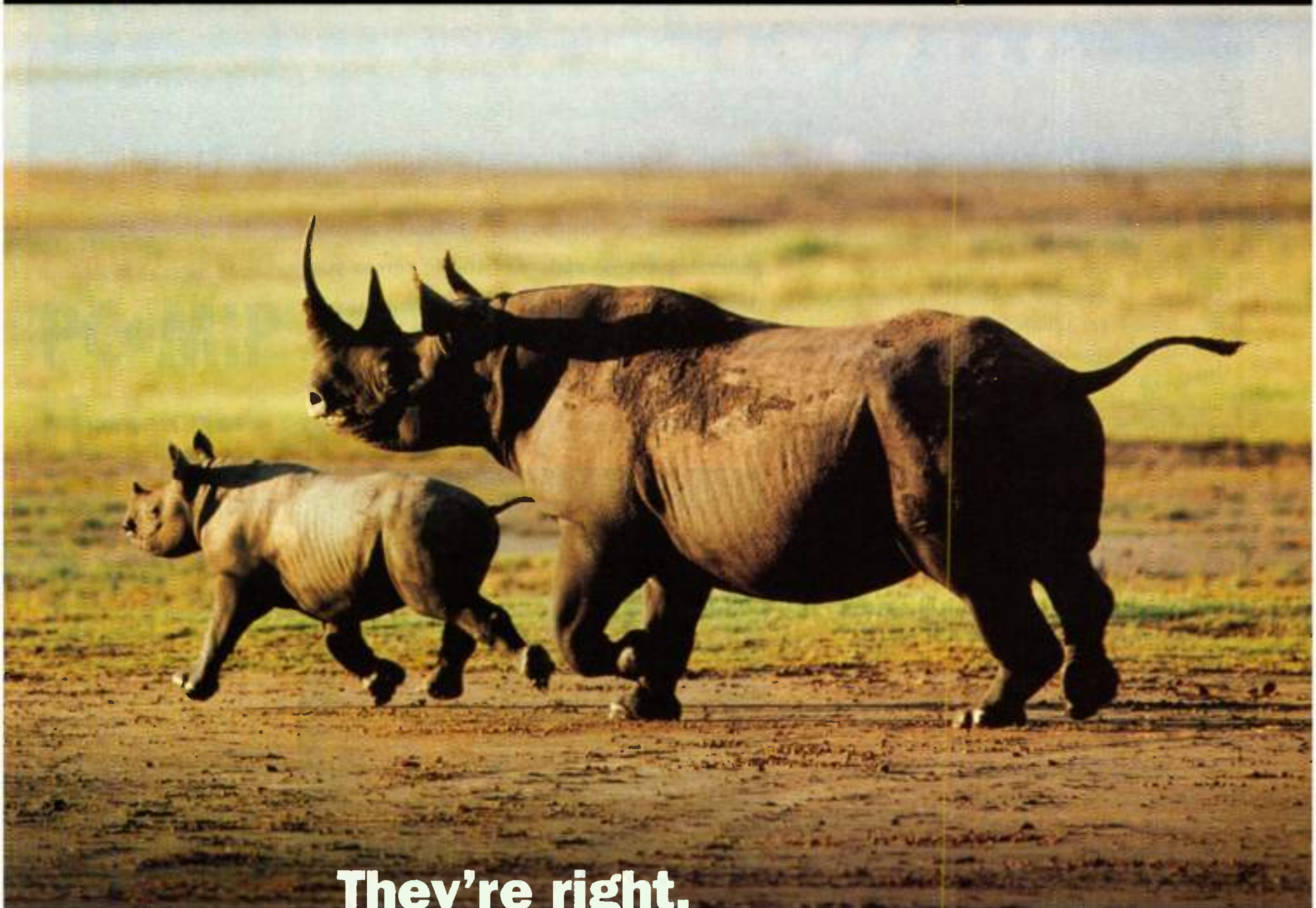
Contact Christine Born, Siemens AG, Semiconductor Group, P.O. Box 801709, 81617 Munich, Germany, +49 89 636 23211, fax: +49 89 636 27151, e-mail: Christine.Bron@HL.Siemens.DE. Or SanDisk Corp. at 140 Caspian Ct., Sunnyvale, CA 94089; (408) 542-0500.

Alfred Vollmer



2. Siemens' 3D-ROM architecture (right) allows the doubling of ROM density compared to a standard ROM process (left). While standard ROM cells occupy a chip area of four square-feature sizes, the 3D-ROM cell needs just two square-feature sizes when using the same process.

They say density runs in the family.



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Photonic Architectures

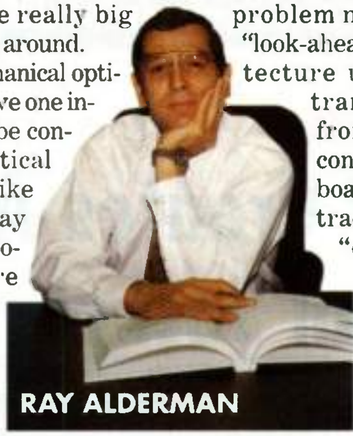
Computer architects of the world have spent the last 50 years designing and building buses with copper pc boards, shipping electrons from one point to another, and dealing with all the transmission-line effects of a backplane. We have explored rings, cubes, and switched architectures in this column, but at the end of the day, we're still moving electrons around.

First things first: "optical buses" is a misnomer. Photons are actually electrons on steroids, and they don't like to be routed, switched, or multidropped, requiring us to develop a new way of thinking. Optical links are typically bit-serial connections, so we have to endure the latencies to shift the bits from a parallel bus into a serial optical bit stream. Photonic architectures have a new set of "aberrant behaviors" that we must understand and manipulate to design an efficient and cost-effective optical architecture.

The primary aberrant behavior of all optical connections is serializing-deserializing latency. Each time a transaction is created for the optical interface, we must endure both delays (serialization at the source and deserialization at the receiver). But, once serialized and translated into photons, gigabit data rates can be achieved without all the problems of a transmission line.

There is one parallel optical bus connection however, called optobus. It transmits data eight bits wide (eight optical data lines) with a strobe and a latch optical control line, making it a 10-fiber point-to-point connection. The problem with optics is that they are much better for point-to-point connections than switched, routed, or multidropped configurations.

There are a number of optical splitters that can divide the beam of light and multidrop the connections like a bus. But each time you split the beam, you send one portion of the light to a board interface, and the remaining photons down the fiber. When you split the beam, there are fewer photons left over to send down the remaining pipeline, so the shared path must be short with few drop points. You can install optical repeaters to provide more photons as it travels down a longer pipe, but now you're spending some really big bucks just to move data around.



Then, there are mechanical optical multiplexers that have one input channel which can be connected to multiple optical output channels. It's like using a mechanical relay to connect data buses together. When you're moving data at gigabit rates, waiting 6 ms to connect the fibers is pretty inefficient. The mechanical connection cycle becomes the address cycle that regular buses use for transactions with electrons, except it is magnitudes longer in duration. Work is being done on very efficient solid-state multiplexers now, so we'll have to see if this will give any new options for photonic architectures.

If we assume a packet-switched architecture with optical connections, each node must translate the photons back to electrons, deserialize the data, and read the address. Then, it either takes the data off the optical network or sends it on by reserializing it and translating it back into photons. Now, we're adding more translation latency to the already-existing routing and switching latencies inherent in a packet-switched network.

So, how do we build an efficient optical architecture that can replace buses inside the computer? The answer lies in the fact that optics like point-to-point connections. The pristine method of solving the optical bus problem is to have unidirectional point-to-point connections FROM every board in the system TO every other board in the system. Mathematically, this requires n(n-1) connections, where n is the number of boards in the backplane. For a three-board system, it would require six optical paths. A four-board system would require 12 optical paths, a five-board system would require 20 optical paths, and so on. It isn't too bad now, but when you consider that a 20-board system would need 380 optical data paths, the methodology isn't very scaleable, or cost-effective.

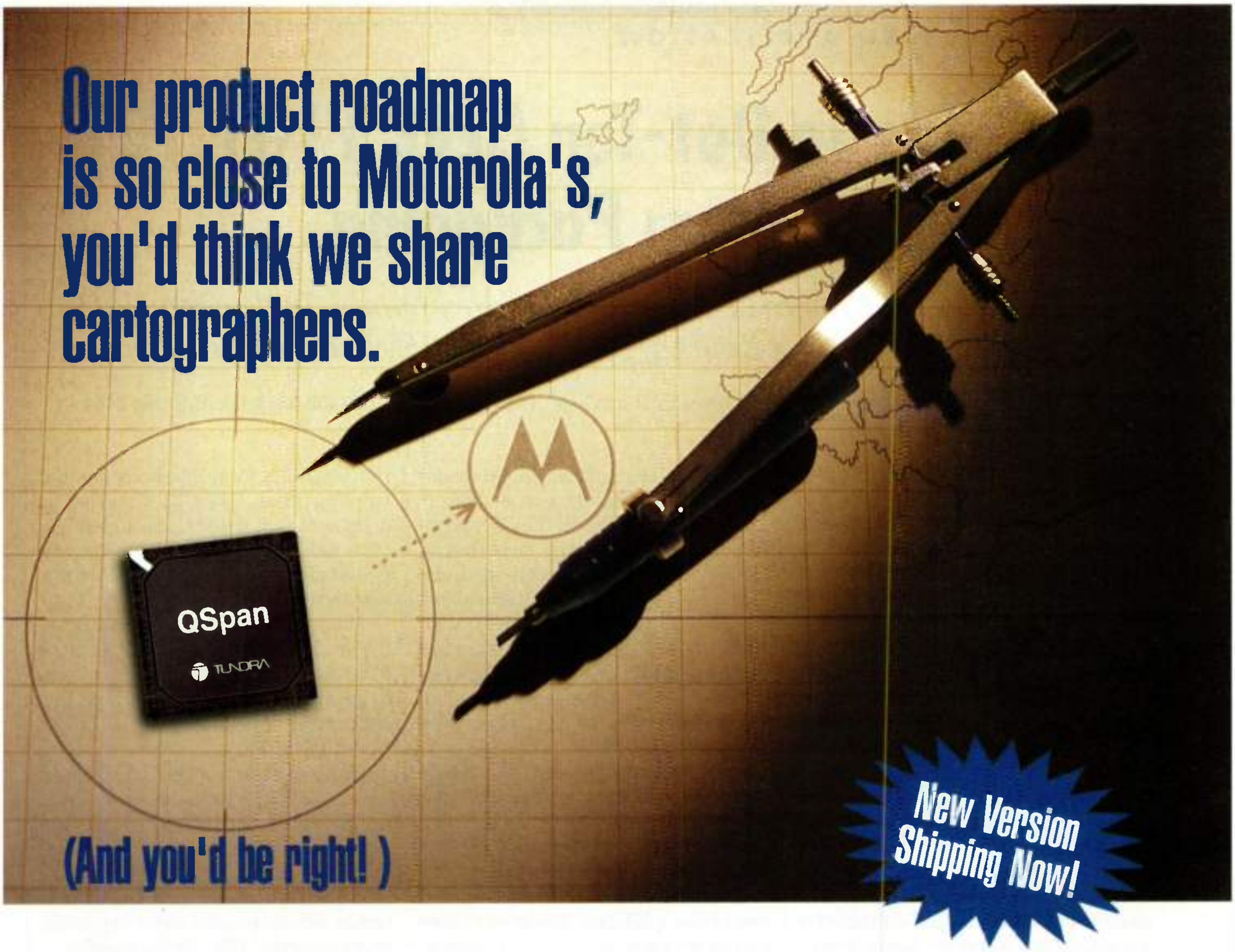
There's another way to solve the problem more efficiently—the "look-ahead pipeline." This architecture uses an optical data transmission bus made from single bidirectional connections between each board in the system, and a traditional multidropped "control bus." One processor in the system is responsible for taking "read" and "write" requests from the different nodes inside the box on the control bus. When we know where data comes from and where it's going to, we can synchronize the transactions on the shared bidirectional data path between the two nodes. The formula for the number of paths needed in this architecture is n(n-1)/2, or half the nodes needed in the perfect architecture. But, that's still 190 optical data paths in a 20-board system.

We could build an optical ring, which would only take n-1 paths, or 19 in a 20-board system. But now we're introducing a pile of translation latency on top of the routing and switching latencies inherent in a ring.

The best solution is an optical multiplexer, if we can overcome the connection latencies. If we use n-1 shared paths, we will always have one path available for nodes wanting to share data, virtually eliminating the possibility of blocking latency. And, we only need 19 optical data paths in a 20-board system, just like the ring, but without the routing and switching latencies.

If we can reduce the multiplexer connection latency to a value that is less than the switching and routing latencies of a ring, we would have an efficient optical bus. But, we still have to increase the data transfer rate tremendously, at the same cost of a traditional electron-based multidropped bus. Until we have cost-effective optical connections, an optical architecture will only be the subject of columns like this one in electronics magazines.

Ray Alderman is the executive director of VITA. He can be reached at exec@vita.com.



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DESIGN APPLICATION

A Guide To Dot-Ten (IEEE 1101.10) System Packaging

This Standard Covers Mechanical Improvements, Including EMI Shields, Connector Keying, And Injector/Extractor Handles.

FRANK COOPER, Electronic Solutions, 6790 Flanders Dr., San Diego, CA 92121-2902; (619) 452-9333; fax (619) 452-9464, www.zerocorp.com/elsol.

With the rapid growth of open-bus-architecture computers in the late '70s, there was a need to standardize the hardware for multivendor compatibility. Many of these computers were being installed into the popular 19-in. racks. The International Electrotechnical Commission (IEC) subcommittee 48D created a document which standardized the hardware based on the two-piece DIN (41612) connector also known as the IEC 603-2 connector.

In 1984, the IEC 48D committee approved the IEC 297-3 Dimensions of Mechanical Structures of the 482.6-mm (19-in.) Series—Part 3: Subracks and Associated Plug-in Units document. This standard covers the basic dimensions of a modular range of subracks for mounting in equipment according to IEC 297-1 (19-in. racks); and the connector-dependent dimensions used when two-part connector types, according to IEC 603-2 (two-part DIN 41612), are mounted on the subracks and plug-in units. It also specifies the standard positions of connectors such that plug-in units are mechanically interchangeable in subracks.

In 1987, the IEEE 1101 working group approved a standard that defined the dimensions and tolerances required to ensure mechanical function compatibility. This standard also offered integration guidelines with the intent of reducing design/development times and manufacturing costs. This mechanical format was known as the "Eurocard form factor."

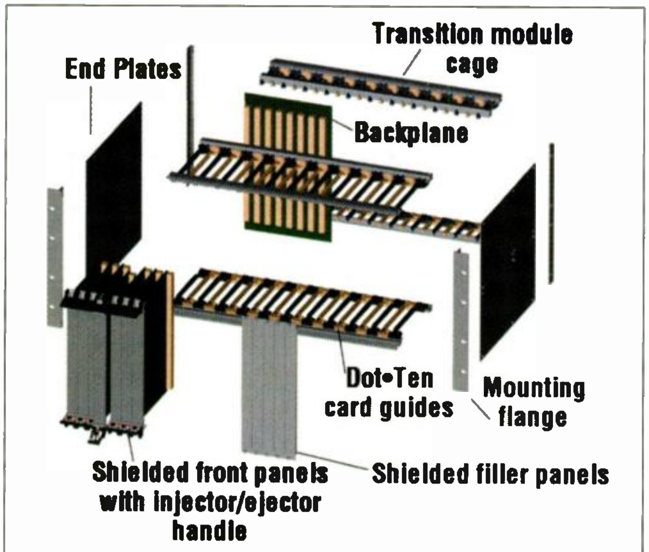
VMEbus: The Eurocard form factor became a popular mechanical standard offering multivendor availability, reduced costs, and interchangeability. VMEbus, the most popular industrial bus structure since the mid '80s, was one of the first open-bus architectures to utilize this mechanical format. Other buses like Multibus II, VXI, Nubus, as well as other proprietary bus designs, adopted the Eurocard form factor. Due to the development of many additional mechanical standards that were based on the IEEE 1101 standard, a new numbering system was created. IEEE 1101 became a family of standards distinguished by IEEE 1101.X. The original IEEE 1101 document became IEEE 1101.1, and was approved in 1991.

In the mid '90s, with the widespread use of the VMEbus, designers were looking for more features to enhance it. The result was a committee under the VITA Standards Organization called the VME64x (VME64 Extensions) working group. VITA 1.1 would be the document that defined the added features to VME64 (VITA 1-VME64 was a previous enhancement to VMEbus, adopted by the VSO in 1995).

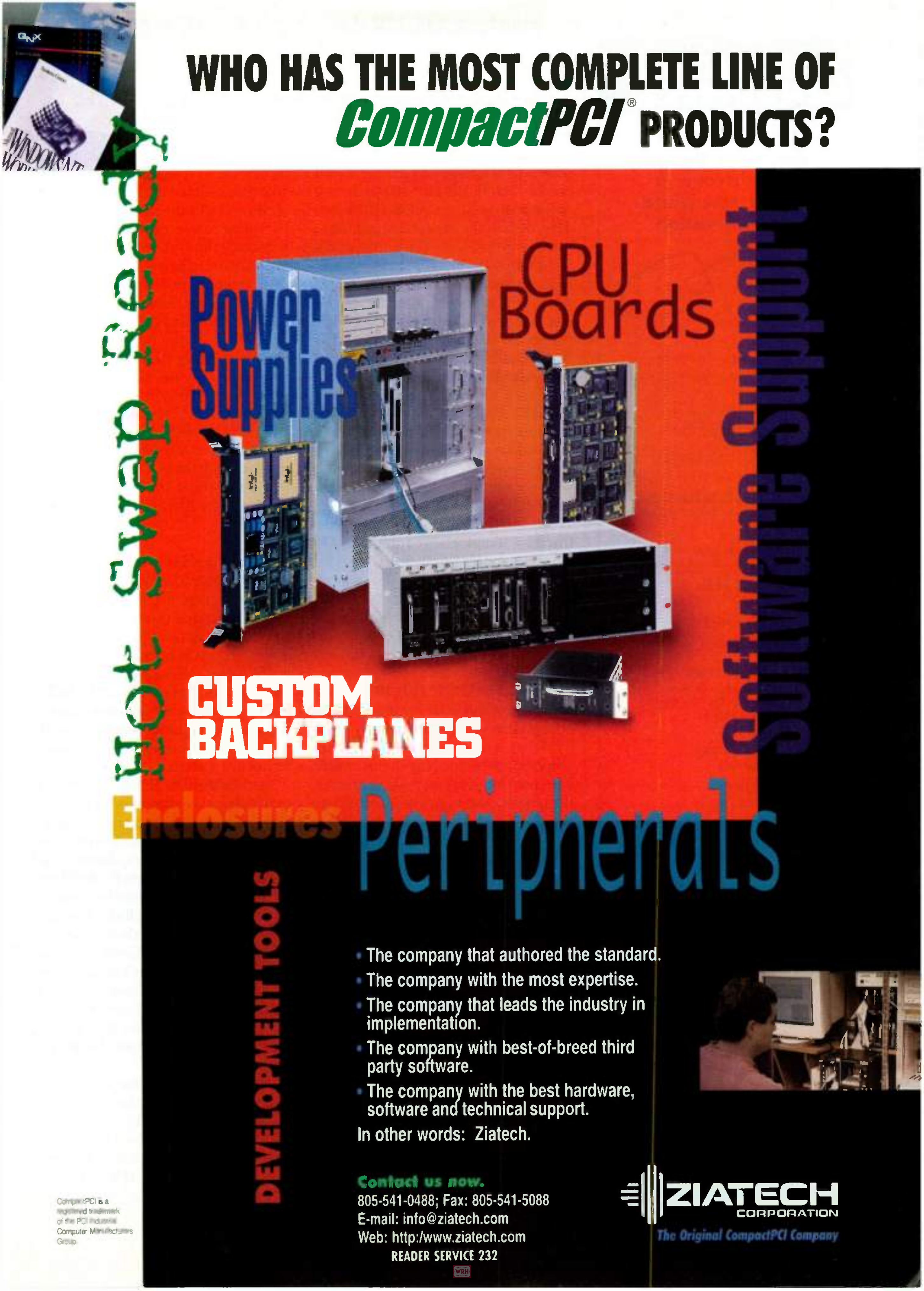
Many of these new features impacted the mechanical standard, prompting the formation of another IEEE committee to incorporate these new features. This committee was known as the IEEE 1101.10 working group. This working group, in conjunction with the VME64x working group, extended the mechanical features of IEEE 1101.1 *(see the figure)*. Some of the features include EMC shielding, an insertion/extractor handle, ESD protection, an alignment pin, protective side covers, and mounting details for an expanded IEC 603-2 connector.

CompactPCI: In the early '90s, a local-bus standard was created to provide a high-speed interconnect for peripheral devices. The PCI standard became the predominant local-bus standard in desktop PCs. A group of manufacturers decided to leverage the circuitry and low-cost components and software availability, and package this into the Eurocard form factor using a 2-mm hard-metric connector. This design became know as CompactPCI. The IEEE 1101.10 standard was approved by the working group in July 1996.

EMC Shielding: With the CE requirements in Europe, many system integrators are looking for ways to improve the EMI/RFI shielding of the subrack. One major area of concern is the subrack's front aperture. Many of the existing



This exploded view of the Dot-Ten (IEEE 1101.10) Eurocage highlights some of the extensions to the original IEEE 1101.1 specification. Included in the extensions are EMC shielding, ESD protection, protective side covers, and an injector/ejector handle.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designs require that the subrack be embedded into an enclosure to provide sufficient protection from EMI/RFI. Users are requesting easy access to plug-in boards for upgrades, repairs, or modifications. The IEEE 1101.10 standard, in conjunction with the IEEE 1101.1 standard, defines the mechanical and the interface dimensions for multivendor front panels to interoperate in a subrack. A gasket is provided on each front panel, which makes contact to an adjacent front panel. The front panels of the plug-in modules can now be exposed for user accessibility.

Injector/Extractor Handles: With the increased pin count in the expanded DIN/IEC connector and the additional J0 connector in VME64x, there came the need for a handle that would provide the leverage to overcome the insertion/extraction forces of the connector(s). Forces can be as high as 175 lbs. in the VME64x-P boards defined by the physics community. As mentioned, the CompactPCI bus selected the 2-mm connector. These insertion forces can be as high as 120 lbs in a fully configured 6U slot. The IEEE 1101.10 standard defines an injector/extractor handle and interfaces in the subrack to help in this area.

Keying: The IEEE 1101.10 standard defines provisions for keying for those applications that require slot exclusivity. When a plug-in board and slot are properly keyed, the plug-in card will fit into that slot. If the keys do not match, the plug-in board can't be inserted into the slot far enough for the two-piece DIN/IEC connectors to fully engage.

This feature is useful in applications where the user-defined pins of the bus structure may cause the system to be inoperable—or worse, cause damage to the plug-in board and/or backplane. The keying system defined in the standard will allow up to 4096 programming possibilities per slot.

Alignment Pin: The IEEE 1101.10 standard defines an alignment pin with the following features: assurance of parallel connector mating, an option for a front-panel ESD contact, and alignment for the shielded front panel. The alignment pin is located on the front panel assembly, and interfaces with the alignment pin receptacle in the card guide.

ESD Protection: The IEEE 1101.10 specifies two important features that help provide ESD (electrostatic discharge) protection:

- Card Guide ESD clip: A plug-in board may acquire static buildup while outside of the system. When the plug-in board is inserted into the system, the charge might discharge though the backplane connector, disrupting or even damaging the system. A feature in the card guide discharges any built up static from the plug-in board into the card-guide ESD clip, which is connected to the subrack frame ground. Depending on the design, the plug-in board may make continuous contact to the subrack frame, or may break contact to the frame prior to connector engagement.
- Alignment Pin ESD clip: Plug-in board front panels may conduct static through the system integrator or technician handling them. The IEEE 1101.10 standard defines an alignment pin that can provide a discharge path to the subrack frame.

Protective Side Covers: The standard defines a protective side cover for those applications requiring solder side protection to plug-in boards. These covers provide mechanical protection to the ESD gasket of an adjacent board as well as the solder tails or surface-mount devices on the solder side of the board. This cover also provides electrical protection from adjacent boards when the plug-in board is inserted or extracted from a live system.

Card Guides: The IEEE 1101.10 standard defines the dimensions of the card guide to allow intermateability with the plug-in boards. Other defined features are the keying chambers, alignment pin chamber, and provision for ESD contacts that can be built into the guide.

Card Guide Mounting Rails: The standard defines the feature in the mounting rail for injector/extractor surfaces. These surfaces allow the handle to inject or extract the plug-in board. The standard also defines the dimensions to allow multivendor handles to work with any IEEE 1101.10-compatible subrack.

Frank Cooper is vice president of sales and marketing for Electronic Solutions. He holds AAs in Management and in Electronics, from the College of the Canyons, Santa Clarita Valley, Calif., and a BA in History from Master's College, also in Santa Clarita Valley.

LINEAR TECHNOLOGY

DESIGN NOTES

LTC1387: 5V RS232/RS485 Multiprotocol Transceiver

Design Note 176

Y. K. Sim

Introduction

The LTC®1387 is a single 5V supply, single-port, logic-configurable RS232 or RS485 transceiver. The LTC1387 features Linear Technology's usual high data rates (120kBd for RS232 and 5MBd for RS485), a loopback mode for self test, a micropower shutdown mode and ±7kV ESD protection at the driver output and receiver inputs. This part is targeted at handheld computers, point-of-sale terminals and applications that require a minimum pin count and software-controlled multiprotocol operation.

RS232 and RS485 Interfaces

Most computers communicate with other computers, peripherals or modems through an RS232 interface, a single-ended interconnection standard. The simplest RS232 interface has three wires: a transmit data line, a receive data line and a ground return. EIA-562 is a single-ended electrical standard similar to RS232, with relaxed voltage levels.

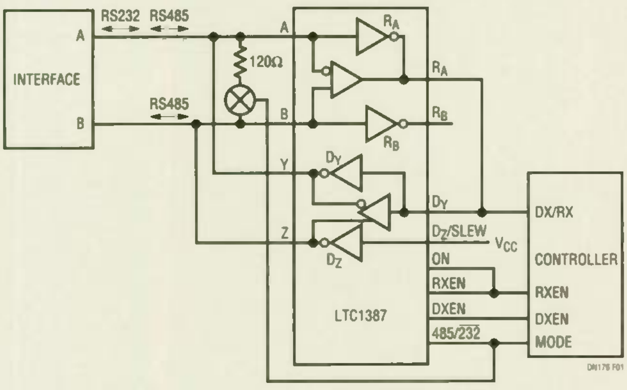
RS485, a differential signal interface, is popular because it offers increased noise immunity, longer transmission cable length than RS232 or EIA-562 and allows multiple transceivers on a twisted pair of wires.

Key Features

The LTC1387 offers a flexible combination of two RS232 drivers, two RS232 receivers, an RS485 driver, an RS485 receiver and an onboard charge pump to generate boosted voltages for true RS232 voltage levels from a 5V supply. Figures 1 through 4 show the LTC1387's versatility in software-controlled RS232/RS485 applications. The RS232 and RS485 transceivers are designed to share the same I/O pins for both single-ended and differential signal communication modes. Both half-duplex and full-duplex communication can be supported. Autodetection of RS232/RS485 interface is feasible via a controller software routine.

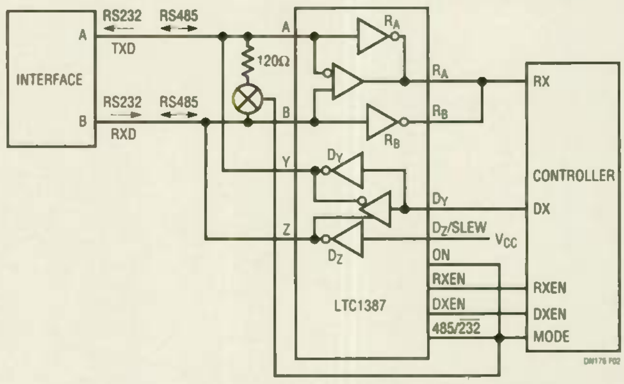
The RS232 transceiver supports both RS232 and EIA-562 standards, whereas the RS485 transceiver supports both RS485 and RS422 standards. The logic input (MODE) selects between RS232 and RS485 modes. With three additional control logic inputs (RXEN, DXEN and ON), the LTC1387 adapts easily, as shown in Table 1, to various communications needs, including a one-signal-line RS232 I/O mode.

A SLEW input pin available in RS485 mode changes the driver transition between normal and slow-slew-rate modes.



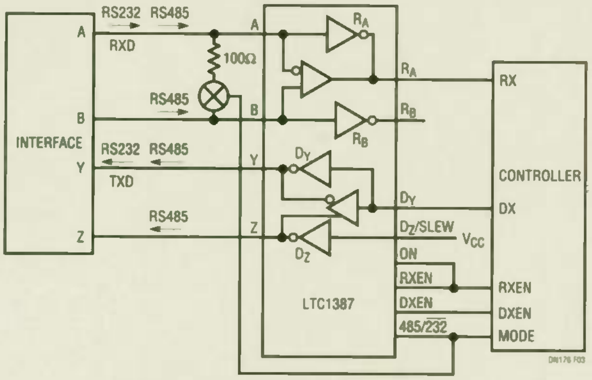
RS232 TRANSMIT MODE	RS232 RECEIVE MODE	RS485 TRANSMIT MODE	RS485 RECEIVE MODE	SHUTDOWN MODE
RXEN = 0	RXEN = 1	RXEN = 0	RXEN = 1	RXEN = 0
DXEN = 1	DXEN = 0	DXEN = 1	DXEN = 0	DXEN = 0
MODE = 0	MODE = 0	MODE = 1	MODE = 1	MODE = X

Figure 1. Half-Duplex RS232 (1-Channel), Half-Duplex RS485



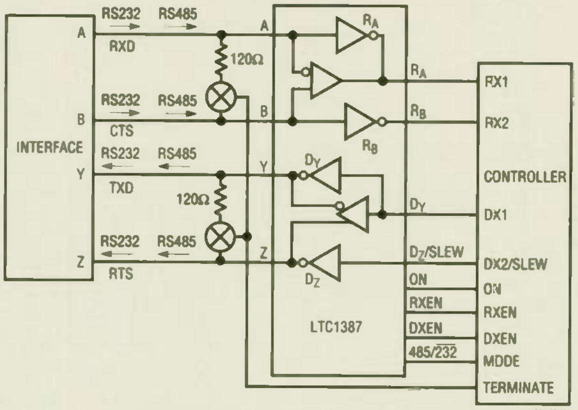
RS232 MODE	RS485 TRANSMIT MODE	RS485 RECEIVE MODE	SHUTDOWN MODE
RXEN = 1	RXEN = 0	RXEN = 1	RXEN = 0
DXEN = 0	DXEN = 1	DXEN = 0	DXEN = 0
MODE = 0	MODE = 1	MODE = 1	MODE = 0

Figure 2. Full-Duplex RS232 (1-Channel), Half-Duplex RS485



RS232 MODE	RS485 MODE	SHUTDOWN MODE
RXEN = 1	RXEN = 1	RXEN = 0
DXEN = 1	DXEN = 1	DXEN = 0
MODE = 0	MODE = 1	MODE = X

Figure 3. Full-Duplex RS232 (1 Channel), Full-Duplex RS485/RS422



RS232 MODE	RS485 MODE	SHUTDOWN MODE
ON = 1	ON = 1	ON = 0
RXEN = 1	RXEN = 1	RXEN = 0
DXEN = 1	DXEN = 1	DXEN = 0
MODE = 0	MODE = 1	MODE = X

Figure 4. Full-Duplex RS232 (2 Channel), Full-Duplex RS485/RS422 with SLEW and Termination Control

Table 1. This Function Table Indicates the Logic Inputs to Configure the LTC1387 for Various RS232/RS485 Modes

SELECT INPUTS				RECEIVER		DRIVER				
ON	RXEN	DXEN	485/$\overline{232}$	RXA	RXB	DXY	DXZ	CHARGE PUMP	LOOPBACK	COMMENTS
1	0	0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	ON	OFF	RS232 Mode, DX and RX Off
1	0	1	0	Hi-Z	Hi-Z	ON	ON	ON	OFF	RS232 Mode, DXY and DXZ On, RX Off
1	1	0	0	ON	ON	Hi-Z	Hi-Z	ON	OFF	RS232 Mode, DX Off, RXA and RXB On
1	1	1	0	ON	ON	ON	ON	ON	OFF	RS232 Mode, DXY and DXZ On, RXA and RXB On
0	0	1	0	Hi-Z	Hi-Z	ON	Hi-Z	ON	OFF	RS232 Mode, DXY On, DXZ Off, RX Off
0	1	0	0	Hi-Z	ON	ON	Hi-Z	ON	OFF	RS232 Mode, DXY On, DXZ Off, RXA Off, RXB On
0	1	1	0	ON	ON	ON	ON	ON	ON	RS232 Loopback Mode, DXY and DXZ On, RXA and RXB On
0	0	0	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	OFF	OFF	Shutdown, RS485 R_{IN}
1	0	0	1	Hi-Z	Hi-Z	Hi-Z	Hi-Z	ON	OFF	RS485 Mode, DX and RX Off
X	0	1	1	Hi-Z	Hi-Z	ON	ON	ON	OFF	RS485 Mode, DX On, RX Off
X	1	0	1	ON	Hi-Z	Hi-Z	Hi-Z	ON	OFF	RS485 Mode, DX Off, RX On
1	1	1	1	ON	Hi-Z	ON	ON	ON	OFF	RS485 Mode, DX On, RX On
0	1	1	1	ON	Hi-Z	ON	ON	ON	ON	RS485 Loopback Mode, DX On, RX On

In normal slew mode, the twisted-pair cable is terminated at both ends to minimize signal reflection. In slow slew mode, the maximum signal bandwidth is reduced; EMI and signal reflection problems are minimized. Slow slew rate systems can often use incorrectly terminated or unterminated cables with acceptable results. If cable termination is required, external termination resistors can be connected through switches or relays.

The RS485 receiver features an input threshold between 0V and −200mV. The receiver output has a known HIGH output state if both receiver inputs are open, if the cable is shorted or if no driver is active.

Conclusion

The LTC1387 is ideal for point-of-sale terminals, computers, multiplexers, networks or peripherals that must adapt on the fly to various I/O configuration requirements without hardware adjustments.

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WHAT'S ON BOARD

Development kits to support the creation of PCI interfaces for embedded processors such as the Intel i960 and the Motorola MPC860 are now available from Anchor Chips Inc., San Diego, Calif. The kits shorten the design time required to interface the company's AN3041Q CO-MEM PCI controller to either of the embedded processors. According to Anchor, the AN3041Q is the industry's first PCI controller to include integrated cache memory (16 kbytes). The cache replaces the traditional FIFO/DMA architecture, to provide a high-speed communication interface from a local microprocessor or DSP to the PCI bus. Furthermore, the PCI controller can completely replace or augment the local microprocessor or DSP chip's memory subsystem by caching its data and instruction memory needs across the PCI bus to host memory.

Each development kit includes a PCI-based add-in board that contains the AN3041Q device, which is interfaced without glue logic to either the i960 or MPC860. The designer can define the amount of host memory allocated to the embedded processor through software; up to 16 Mbytes of host memory can be allocated. The controller also has 512 bytes of shared memory.

Included with the kit is the company's CO-MEM Mapper software that can run on any PC with Windows 95, 98, or NT. The tool automatically configures and displays the AN3041Q's internal registers. Once the PCI chip is configured, the i960 or MPC860 can be released from reset to run the application. Debug tools also are included. Either kit sells for $495 each. Additional kits are available for the Motorola MC68020 and MC68360 microprocessors. Contact Pete Fowler at (619) 613-7900 or www.anchorchips.com.

A 42-in., diagonal, flat-panel, color plasma display, the ImageSite 42, provides a high-contrast 16:9 ratio screen that lets the panel deliver comparable picture quality to that of CRTs. Developed by Fujitsu Microelectronics Inc., San Jose, Calif., the display has a suggested list price of $10,999, which is 20% lower than the initial ImageSite display released last year. This display, however, provides twice the brightness and six times the contrast of the previous model.

Inputs to the display panel include component video and SVGA. Users can control the white balance to optimize the display for different applications. The 852-by-480-pixel panel can seamlessly display any type of graphical information and entertainment media, regardless of the source. For standalone operation, the display can be enhanced to include a PC-card slot, which can hold a single-board computer. This way, the display can be used for electronic posters, information displays, and presentation systems. The plasma display has a depth of less than 6 in. Because it is an emissive system, it can be viewed in almost any ambient-light conditions. The viewing angle of 160° on both the horizontal and vertical axes allows the panel to be positioned in any convenient location. Contact Joe Virginia at (408) 922-9000 or www.fujitsumicro.com.

A low-voltage octal buffer/line driver, and a 16-bit transparent latch have been added to the Crossvolt LCX and VCX families of logic interfaces. The 74LCX2244 buffer/line driver includes 26-Ω series resistors in the outputs to reduce ringing and eliminate external resistors. The chip contains eight noninverting buffers with three-state outputs. The chip also incorporates power-down high-impedance inputs and outputs and can operate from supplies ranging from 2.0 to 3.6 V. Compatible with the standard "244" series devices, the circuit can drive ±12 mA while introducing a propagation delay of as little as 1.5 ns (7.5 ns maximum). The 74VCX16373 16-bit transparent latch, can interface with 2.5, 3. 3, 1.8 V, or mixed voltage systems, and operate over a -40 to +85°C. Offering propagation delays of 3 ns maximum when operating with a 3.0- to 3.6-V supply, the latch can find a home in high-speed servers, desktop computers, mobile systems, and other high-performance systems. The 74VCX16373 also has a static drive capability of ±24 mA at 3 V, ±18 mA at 2.3 V, and ±6 mA at 1.8 V. Samples of the 74LCX2244 and VCX16373 are immediately available and sell for $0.53 and $2.10 apiece, respectively, in 1000-unit lots. Contact the company at (207) 775-8100 or www.fairchildsemi.com.

DSP Card Boasts PCMCIA Interface And Stereo Audio

A DSP-based interface card aimed at audio-signal processing offers 50 MFLOPS and stereo input and output. The BULLETdsp is a portable Type 3 PCMCIA interface card based on the TMS320C32 floating-point DSP. It features two stereo CD-quality audio I/O channels, up to 1 Mbyte of SRAM, 4 Mbytes of DRAM, and 512 kbytes of flash memory. Each audio channel is based on Crystal Semiconductor's 16-bit, stereo multimedia codec, which provides line-in, line-out, and phantom-powered mic-in channels. Both the host processor and the DSP may control the codec's programmable sample rate, input gain, and output attenuation. BULLETdsp is shipping now. The $895 base price includes 256 kbytes of SRAM.

Communication Automation & Control Inc., *1642 Union Blvd., Suite 200, Allentown, PA 18103; (800) 367-6735 or (610) 776-6669.* **CIRCLE 569**

VME64x Backplanes Include JO Connectors

Sporting a JO connector for each slot, the eight-layer VME64x-JO Series of backplanes is offered in 17 models that include from 5 to 21 slots. The units are claimed to meet the highest performance standards of the new VME64 Extensions specification. In addition, they use the company's DawnWrap metallization technology, which greatly reduces EMI/RFI emissions and system noise. The technology deactivates slot antennas that can result near the board edge when adjacent layers are operated at different potentials.

Other features of the backplanes include optimal power/ground distribution and signal-line impedance, balanced and matched-impedance transmission-line design, and provision for manual or optional electronic BusGrant functionality. There also are discrete circuits for V1 and V2 as well as a broad range of options. Prices range from $1100 to $2995, each depending on the number of slots.

Dawn VME Products, *47073 Warm Springs Blvd., Fremont, CA 94539; (510) 657-4444; www.dawnvme.com; e-mail: mail@dawnvme.com.*
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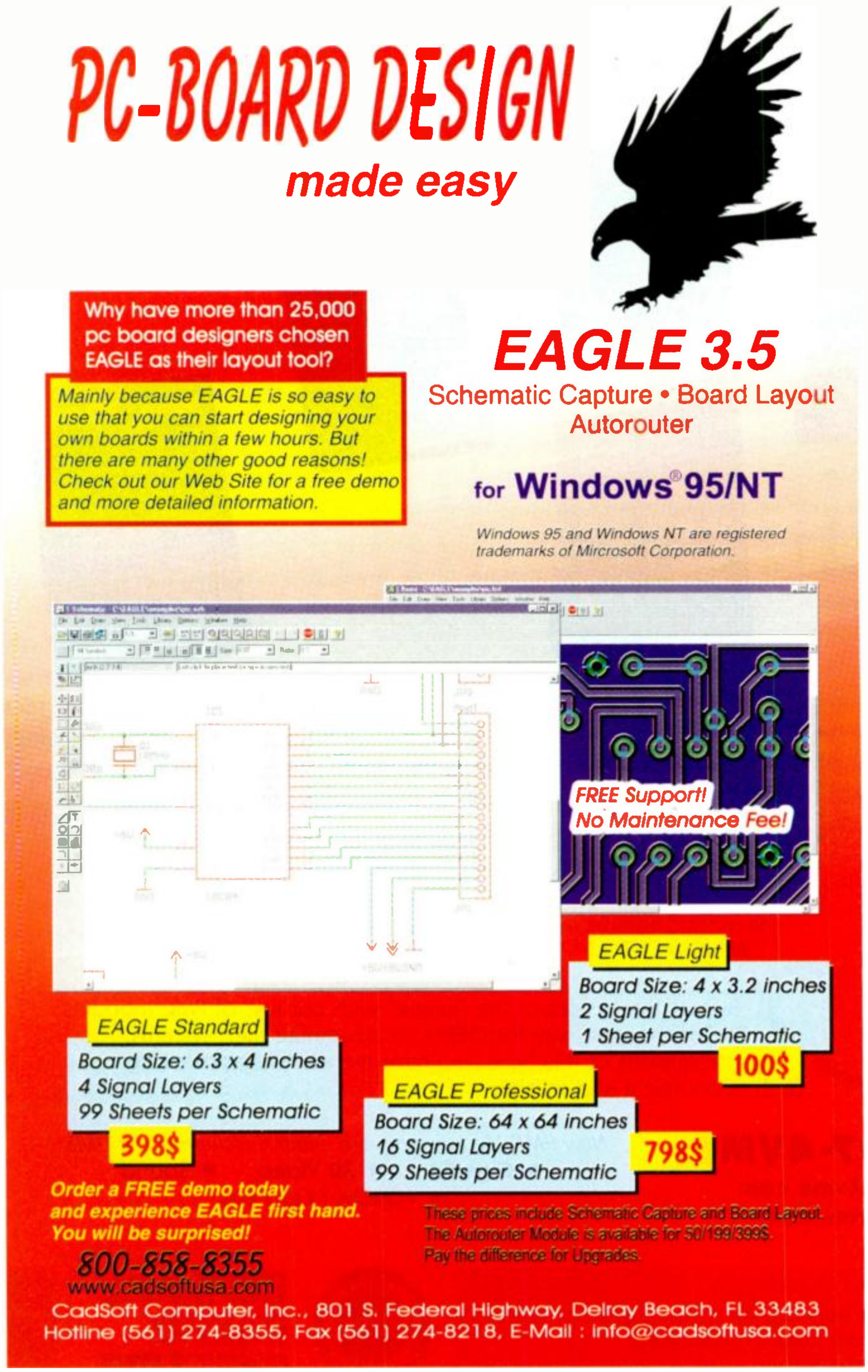
PCMCIA Communications Card Has RS-422 And -485 Ports

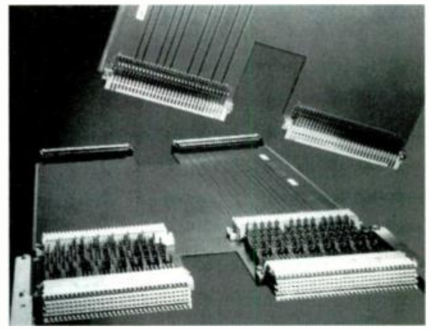
A new PCMCIA serial-communications card developed by Acces I/O Products is aimed at laptop computer designs. Key features of the PCM485 card include asynchronous RS-422 and RS-485 serial ports, 16-byte buffered type 16550 UARTs, and auto send-data control for Windows compatibility. The PCM485 can drive up to 60 mA on balanced lines with a quiescent current of 300 µA, and it can receive inputs as low as a 200-mV differential signal superimposed on common-mode noise up to 500 V. Its Maxim 485 output transceiver features thermal shutdown in case of communication conflict. The PCM485 communications card is available now for $149. That price includes the card, manual, software, and cable. Delivery is two weeks.

***Acces I/O Products**, 9400 Activity Rd., San Diego, CA 92126; (800) 326-1649; www.acces-usa.com; e-mail: sales@acces-usa.com.* **CIRCLE 548**



VME64 Extender Lets Users Test Boards Outside Subrack

A new 6U 10-layer stripline VME64 extender board enables users to test and configure their boards outside the subrack. All 160 pins on both the J1 and J2 connectors are extended, with

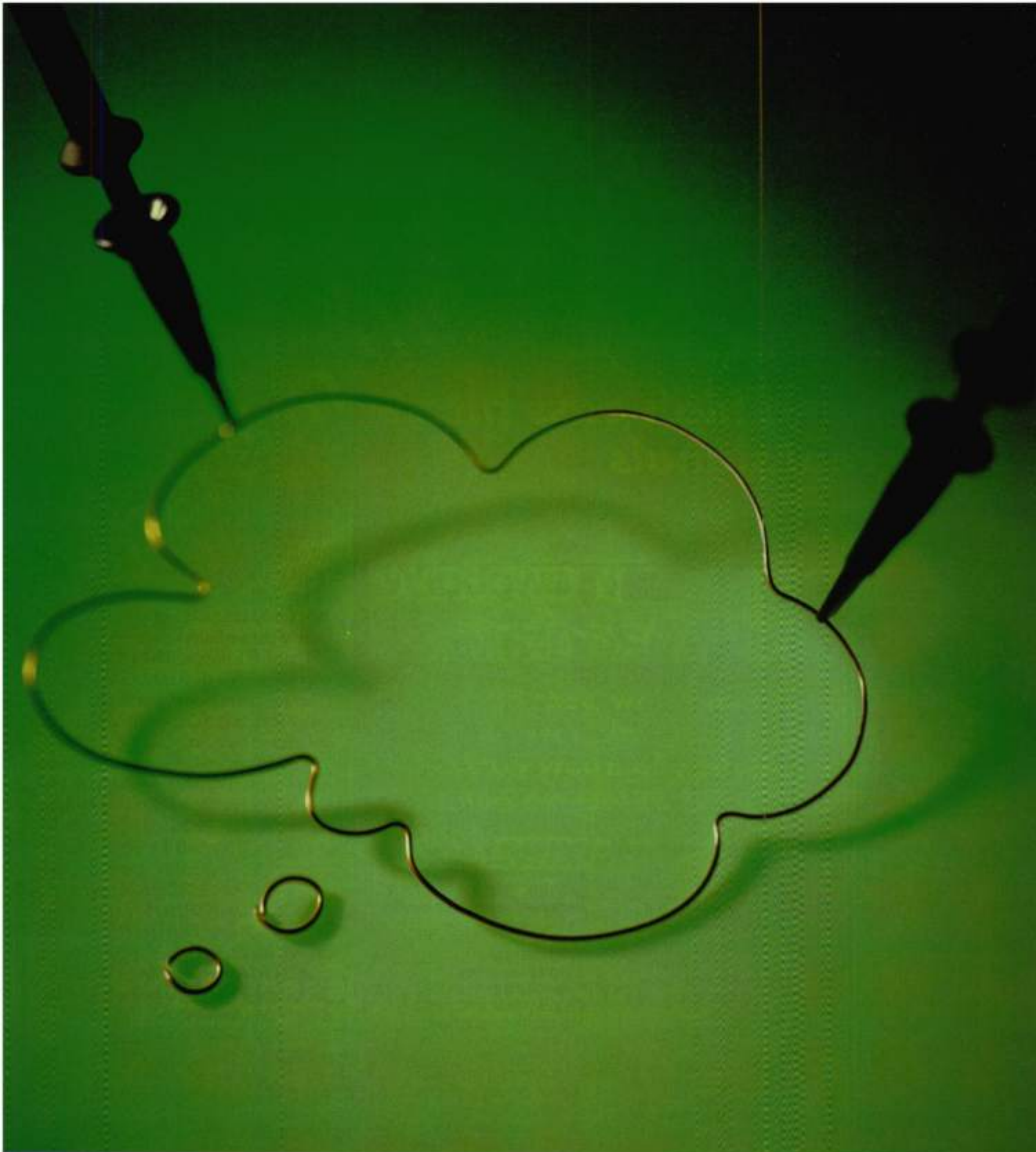


individual jumper links on each line to allow connectivity to be broken as required for analysis. Each signal line is individually screened to reduce crosstalk, and the extender board is supplied with connectors to accept a logic analyzer or termination module. A cutout in the J0 area lets the additional 95-pin J10 connector be extended by using a dedicated cable assembly. Contact the company for pricing and additional information.

***VERO Electronics Inc.**, 5 Sterling Dr., Wallingford, CT 06492; (203) 949-1100 or (800) 242-2863; Internet: http://www.vero-usa.com; e-mail: vero@vero-usa.com.* **CIRCLE 549**

Rugged Enclosure Holds Ten 6U And Eight 9U VME Slots

AP Labs announced its FS-8019 ruggedized enclosure that accommodates ten 6U VME slots and eight 9U (400 mm) VME slots. Other backplane configurations can be supplied by special order. The FS-8019 provides mounting for two half-high SCSI peripherals within the enclosure. Both are front-door accessible. The standard configuration is wired with a 1000-W ac power supply, and is constructed of solid-seam welded aluminum alloys *(continued on page 118)*



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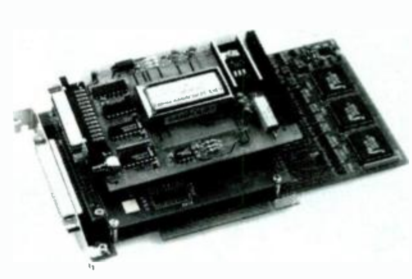
(continued from page 118)
ministic network-access times, scalable bandwidth, and high-speed ATM network connections (up to 155 Mbits/s). In addition, it complies with ATM's quality-of-service features, suiting the module for real-time applications.

The CPMC-ATM occupies a single slot and offers a good deal of I/O flexibility. Designers can select among the most common physical interfaces to ATM networks: 155-Mbit/s STS-3C on single- or multi-mode fiber optics, UTP5 155-Mbit/s STS-3C, and UTP3 at 25 Mbits/s. The CPMC-ATM module comes bundled with ATM software and complies with the PCI 2.0 interface. The device is available now for $790.

***CETIA Inc.**, 58 Charles St., Cambridge, MA 02141; (617) 494-0987; www.cetia.com.* **CIRCLE 553**

PC-Based Frame Grabbers Let Robots And Machines See

The PC_EYE product line offers a range of low-cost PC-based frame grabbers for machine and robot vision, image analysis, quality control, security, and medical imaging applications.



PC_EYE1 supports up to four monochrome matrix cameras and real-time acquisition of single images and sequences using PCI bus master DMA. PC_EYE2 is a PCI-based frame grabber for color matrix cameras that provides real-time acquisition of images and image sequences directly into the PC's main memory. PC_EYE3 provides a flexible PCI video input for line-scan camera, digital matrix camera, and general-purpose digital input. All of the frame grabbers are supported by PC_EYE Basic Tools, a C/C++ programming interface that can be used with Windows 95, Windows 3.1x, and Windows NT. Contact the company for pricing.

***American ELTEC**, 101 College Rd. East, Princeton, NJ 08540; (609) 452-1555; http://www.eltec.de; e-mail: websales_us@eltec.de.* **CIRCLE 554**

PCI Mezzanine Card Module Carries Four SHARC DSPs

The processing power of four ADSP-2106x SHARC DSPs is combined with the speed and flexibility of the PCI interface in the PMC/64, a single-width PCI Mezzanine Card (PMC) module. The board benefits from a reduced power demand and associated heat dissipation thanks to the SHARC digital signal processors' lower 3-V power-supply requirement.

The standard module can be plugged onto any suitable carrier that has a PMC site. These include PCI cards, CompactPCI cards, and
(continued on page 122)

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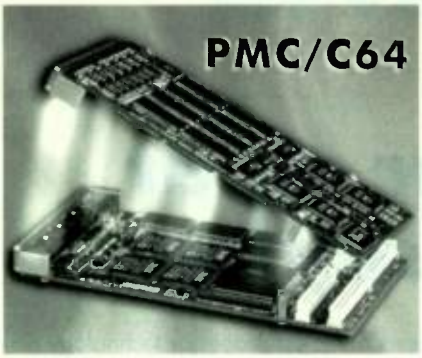

VME boards. It gives existing SHARC users the ability to add processing power to Loughborough boards on VME or PCI cards. Each of the four SHARC digital signal processors on the card can individually process 120 MFLOPS at 40 MHz for a total card performance of 480 MFLOPS. Software support is provided by the company's integrated development environment. On-module memory consists of up to 512k by 32 of SRAM, 16M by 32 of SDRAM and 1 Mbyte of flash memory. Pricing for the processors is $8000 each in OEM quantities.

Loughborough Sound Images Inc., *70 Westview St., Lexington, MA 02173; (781) 860-9020; www.lsi-dsp.com.*
CIRCLE 555

Flat-Panel CRT Replacements Display Full-Motion Video

A flat-panel CRT replacement called VAMP-SmartSize uses smooth image resizing to fit low-resolution images on high-resolution screens. In addition, the flat panel will display interlaced full-motion video as well as progressively scanned computer graphics.

The VAMP-SmartSize is available in a number of panel sizes (6.4 in. to 14.5 in.), and as a 15-in. color TFT LCD. The 15-in. panel features an enhanced viewing angle (–70° to 70°), good contrast ratio (300:1), and is available in a sunlight-readable configuration. All of the panels employ automatic calibration to correctly fo-

cus and position an image on the screen.

The VAMP-SmartSize 15-in. color TFT LCD costs $4699 in 10-unit quantities. That price includes a guided wave touchscreen and all interface electronics mounted in a rugged metal OEM frame. Contact the company for additional pricing and information.

Computer Dynamics, *7640 Pelham Rd., Greenville, SC 29615-5789; (864) 627-8800; www.cdynamics.com; e-mail: sales@cdynamics.com.*
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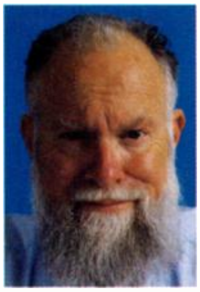
BOB PEASE

Bob's Mailbox



Dear Bob:

My old boss (John Myers) stopped by my cubicle a little while ago and dropped the Jan. 12 issue of *ELECTRONIC DESIGN*, open to your column, on my desk. He said, "Gerry, you are in good company with your copper-clad bread-boards," and then walked off.

Your column, as always, was good for a chuckle and a lot of whole-hearted agreement. Most of the YPEs (Young Punk Engineers) I have met recently have never had their hands dirty or changed the oil in their car, let alone prototyped.

The bread boards I used to make for John usually consisted of copper-clad stock with a twist. I use a Dremel tool with a mill ball and a straight edge to cut long, wide, bus bars into the copper-clad stock.

By the way, I have used your "What's All This..." title in several of the columns I have done for the Garland Amateur Radio Club. If you want to see them, they can be found at: *web2.airmail.net/gerryc/newham.html.*

Gerald Crenshaw
via e-mail

Gerry, you have some nice work on your site that can help new hams. Sections NHP-4, -3, and -9 seem quite thoughtful. You sure have your head screwed on right! Thanks.—RAP

Dear Bob:

I would like to take a moment to provide my insights (as an EE student) on the notion that there is a slight naivete about passive components. Sure, not every student is taught about differences, but common sense should prevail when looking at data sheets—the material is specified for a reason. Maybe that would give the EE a clue that, quite possibly, one could use other materials for the component.

Maybe not everyone uses data sheets, but that is why the experienced EE can be of great service to the new EE. With a little bit of assistance and encouragement, hopefully the new EE will become a great asset to the engineering community. So please remember to help the "new kid" and maybe you will feel a little bit better knowing that you are helping your future and someone else's.

MICHAEL ISAACSON
Electronics Design Technician
Nonin Medical Inc.
Plymouth, Minn.

Mike, I agree that we have to be nice and helpful to young engineers. But you'll agree, it's not always easy to get the message across.—RAP

Dear Bob:

Re: Your Jan. 12 column

Seems that these "wonderful" computers have virtually eliminated any lab courses. I remember a chemist friend of mine saying (20 years ago) that soon one would be able to get a degree in chemistry without ever touching a test tube.

At the time, he was programming simulations of titration at the University of Illinois. They were experimenting with computer teaching using plasma displays in combination with rear-screen projection of microfiche.

When I was a few years out of college (circa 1958), I was interviewing new graduates for positions in our company. I had been working on a little logic board, and during an interview, absent-mindedly asked one of the interviewees to pass me a 10-kΩ resistor from the pile laying on the table behind him. I got a blank look in return. "You don't know the resistor color code?" I asked. "No," was the reply. By then, in my early career, I recognized standard 5% resistors without "translating" colors.

Most of my career has been spent at the other end of the frequency spectrum from RF. Presently, I deal with subaudio signals from vibration transducers in balancing machines (5 to 20 Hz, most commonly). We deal with very-low-level signals from vibration transducers, and have learned how to keep our analog circuits quiet. We also have minimized crosstalk in two signal channels in the presence of high frequencies from the computer that processes the signal after the analog preprocessing.

It's too bad that engineering has gotten so filled with complex theory that there is NO time for anything practical. Back in my college days, we had lab courses in such areas as Welding (gas and arc) and Machine Shop (constructed a nice little bench vice using milling machines, a shaper, and a lathe).

The Mechanical Engineering side course had a lab studying internal combustion engines, dynamometer studies, speed-torque curves, etc.

The Electrical Machinery lab studied motors of various types. Surely most of what I learned in that course is now bordering on the obsolete, but the principles still work. I know the difference in characteristics between series and shunt wound motors, understand capacitor start and run, and single-phase ac motors.

A more recent graduate than I can do a DSP algorithm off the top of his head that sends me to read textbooks and look for cookbook solutions, but he lacks some of the basic understanding of the physics of the real world

RON ANDERSON
Chief Applications Engineer
Hines Industries
Ann Arbor, Mich.

Practical knowledge is so important, because without it, a young engineer can waste a lot of time and get discouraged. It's not easy being a mentor, when the young engineers don't even know what they don't know...The kind of resistor they might have, for example.—RAP

All for now. / Comments invited!
RAP / Robert A. Pease / Engineer
rap@web team.nsc.com—or:

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Note: The USA distributor of Wainwright Instruments Inc., whose prototyping system was mentioned in the Jan. 12 issue is : RDI Wainwright, 69 Madison Ave., Telford, PA 18969-1829; (215) 723-4333; fax: (215) 723-4620; e-mail: soldermount@rapdep.com.

Circle 520

Optically Isolated And Powered 1-kHz ADC

W. STEPHEN WOODWARD
Venable Hall, CB3290, University of North Carolina, Chapel Hill, NC 27599-3290; Internet: woodward@net.chem.unc.edu.

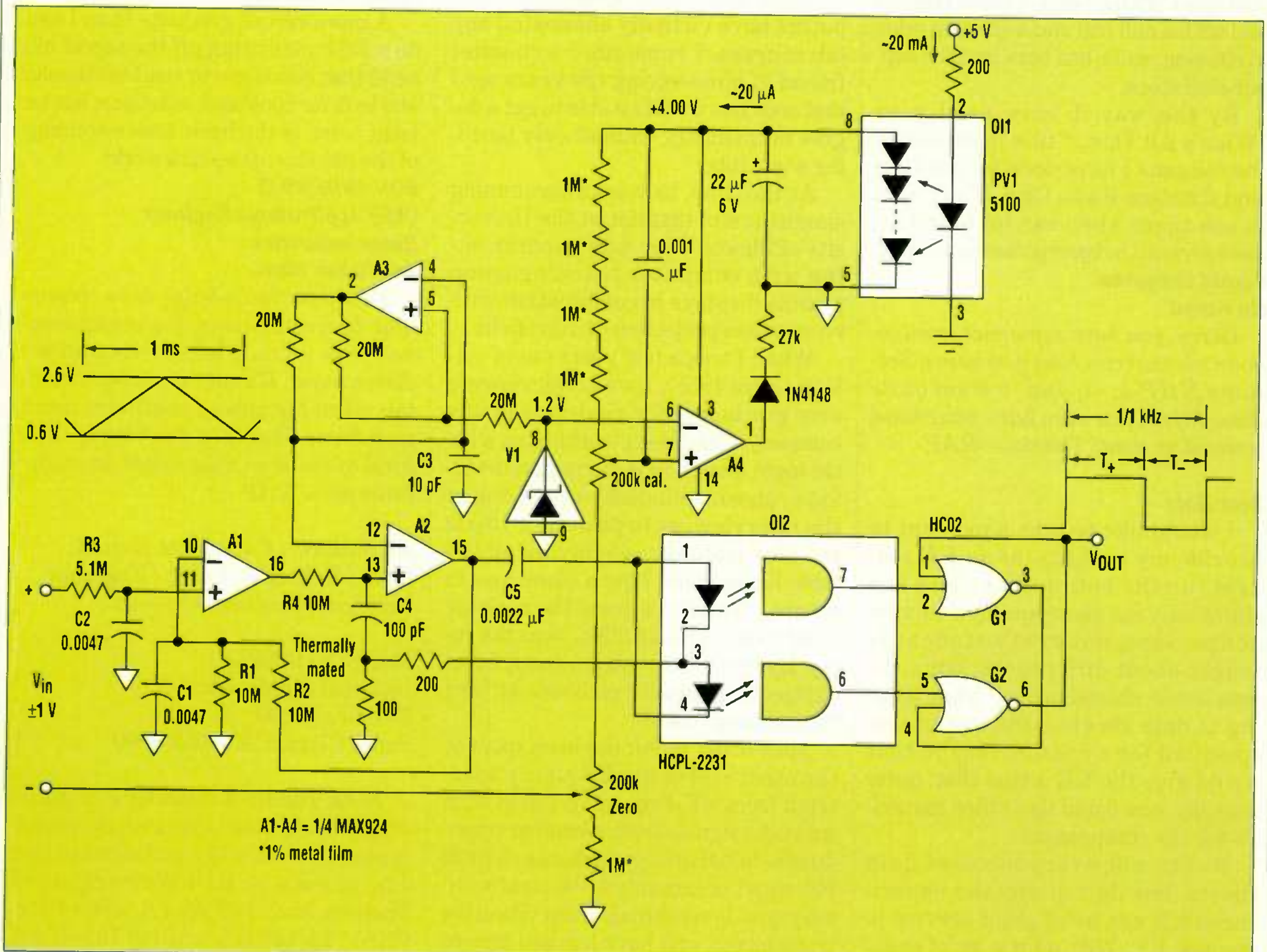
Some data-conversion applications require complete galvanic isolation of the signal source from system ground. Examples include industrial process monitoring using ion-selective and pH electrodes, and biological and medical diagnostics such as electrocardiography and electroencephalography (EKG, ECG) in which sensor electrode isolation is needed for both noise reduction and safety reasons. Optical coupling, of course, is the gold standard of signal isolation techniques, but it doesn't solve the sticky problem of providing a power source for converter circuitry on the transducer side of the isolation barrier.

The ADC introduced here is unique because it uses standard optoisolator devices to accomplish both tasks. Achieving this dual objective is an interesting exercise in sub-micropower signal-handling tricks.

The converter is based on pulse-width-modulation (PWM) techniques. A1 compares the filtered input signal (±1-V full scale) to the voltage on C1. A1's output is smoothed by the R4C4 time constant and compared by A2 to multivibrator A3's approximately 1-kHz "triangle" waveform. The resulting variable-duty-factor squarewave is scaled and averaged by R1, R2, and C1, and fed back to A1. This feedback loop continuously adjusts A2's duty factor to maintain V(C2) = V(C1). In doing so, A2's output squarewave is forced to track the unique $T_+/(T_+ + T_-)$ duty factor that maintains balance at A1's inputs.

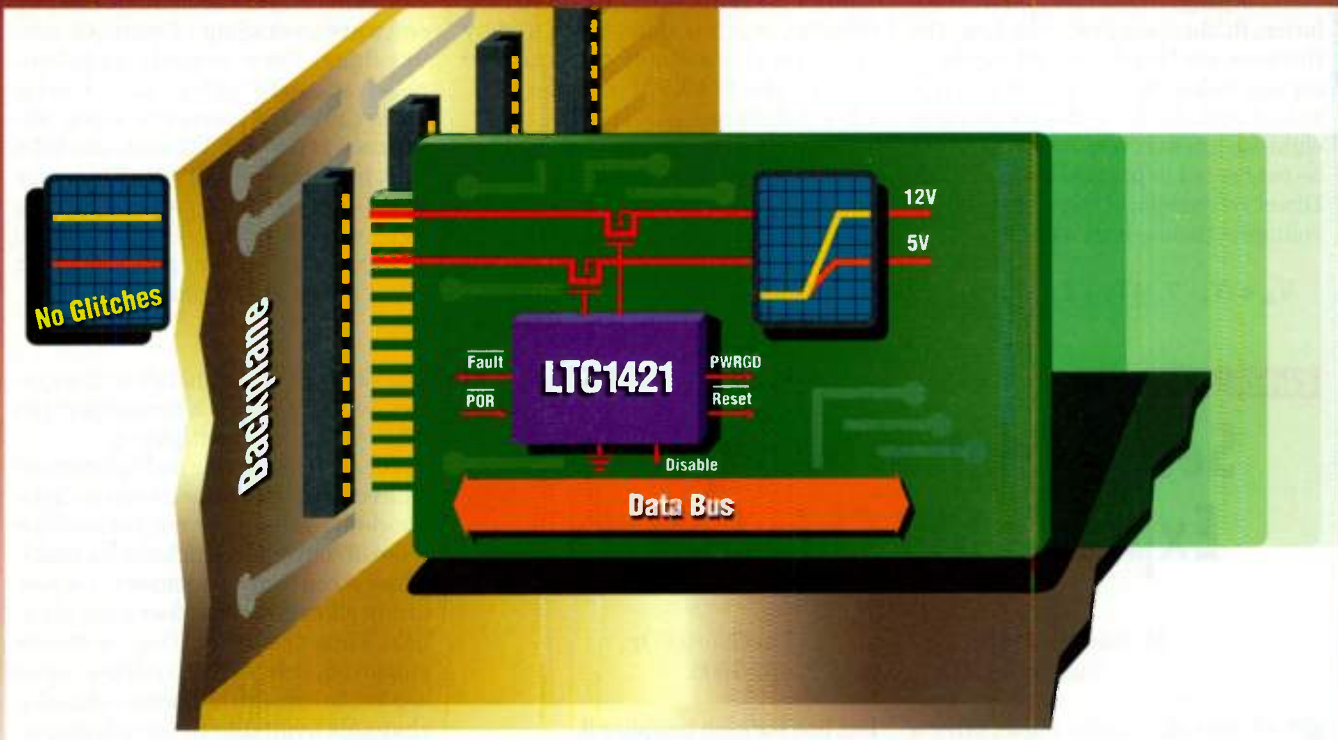
The A2 squarewave is differentiated by C5 to provide bipolar drive pulse to the anti-parallel LEDs of high-speed, low-current optoisolator OI2. In turn, OI2 produces ground-referred pulses that the HC02 NOR-gate flip-flop converts back to a squarewave with the same duty factor as A2's output.

Extracting a signed numeric conversion result from this signal can be



Using standard optoisolator devices and employing PWM techniques, this analog-to-digital converter is both optically isolated and powered.

Hot Swap Safely!



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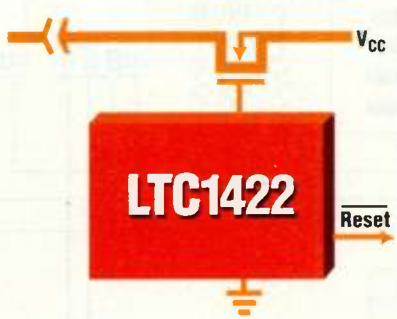

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done in a number of ways, the easiest (zero glue logic) of which is to use the "edge-capture" feature implemented in 68HC05, HC11, and HC12 microcontrollers. If, for example, one of the eight counter-timer channels of an HC12 is programmed for 8-MHz-resolution, dual-polarity edge capture, the timer-channel hardware will explicitly capture values for the T_+ and T_- intervals of each A2 cycle. Note that up to eight such converters could therefore be connected in parallel to one HC12. Direct conversion of these times to V_{in} voltage is then as easy as:

$$V_{in} = (T_+ - T_-)/(T_+ + T_-)$$

Isolated power for the converter comes from OI1—an International Rectifier PVI5100 photovoltaic optoisolator. This device is intended by the vendor to serve in isolated MOSFET gate drive applications. It can reliably source about 20 µA of current (80 µW), which is shunt-regulated by A4 to provide a stable 4.0 V ratioed against the MAX924 internal ±1%, 1.2-V reference.

Conversion resolution for this ADC is pretty good: 12 bits + sign in the HC12 example cited (8 MHz/1 kHz = 8000 counts/conversion cycle). Peak-to-peak conversion noise, on the other hand, isn't so wonderful: approximately 10 mV due to A1 and A2's rather large input-referred noise as is common in sub-micropower devices like the MAX924. But converter linearity and stability is better than 0.05%, so high-resolution applications can generally be accommodated by software averaging of multiple conversions. Thus, overall signal-to-noise ratio to the sub-millivolt level is achievable. Converter dc input impedance is about 1 TΩ with less than 1 pA bias. This permits good accuracy to be expected even when working with very high impedance signal sources. Converter span and input offset errors are trimmable to zero.

Circle 521

Serial-Control Multiplexer Expands SPI Chip Selects

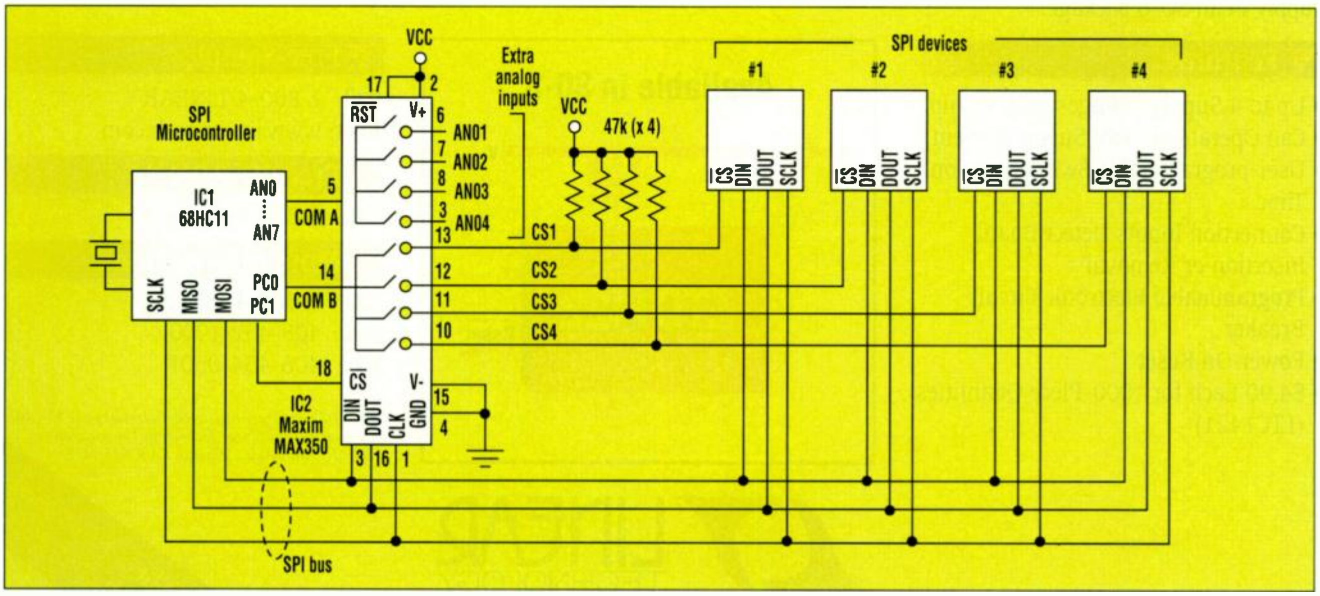
JOHN WETTROTH
Maxim Integrated Products, 120 San Gabriel Dr., Sunnyvale, CA 94086; (408) 737-7600.

SPI and Microwire buses offer a popular and convenient means for minimizing the number of interconnect wires required in connecting smart peripherals to a microcontroller. These standard synchronous buses comprise a serial-clock, data-in, and data-out line in addition to a chip-select line for each peripheral.

One chip select per device, however, can quickly use up the precious port pins in a microprocessor system. To ease this situation, the dual four-channel analog multiplexer (an SPI device itself) multiplexes a single port pin (PC0) to provide chip selects for four other SPI peripherals in the system *(see the figure)*. A second port pin (PC1) selects the multiplexer.

All switches in this multiplexer are bidirectional. Its two sections are independent, and either output (unlike those of conventional differential multiplexers) can be programmed to connect to any, all, or none of its four input channels. Thus, the second (top) section is employed, independently of the lower section, to expand the number of analog channels available to the microcontroller. The microcontroller's internal multiplexer supports eight channels, so this scheme (using one to get four more) yields a total of 11 input channels.

By operating "backwards," the lower 4:1 multiplexer routes the PC0 signal to a selected peripheral's $\overline{CS}$ in-



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put. Driving PC0 low selects that peripheral for receiving SPI data, and driving PC0 high de-selects all four peripherals. Read and write sequences are the same as in regular SPI systems, except that the chip selects must be set up beforehand. PC0 then goes low, the read/write operation is executed, and PC0 returns high to de-select the device.

This procedure isn't burdensome in practice. Typical SPI systems include a device that's serviced often (such as a display driver), and several others that require service only occasionally (such as EEPROMs or real-time clocks). Thus, the chip-select multiplexer can leave the heavily used device selected most of the time, and perform an update only when selecting a new device.

To accommodate other combinations of chip-select and analog expansion lines, you can replace the MAX350 with a similar device (the MAX395), whose eight serially-addressed SPST switches can be configured as required.

Circle 522

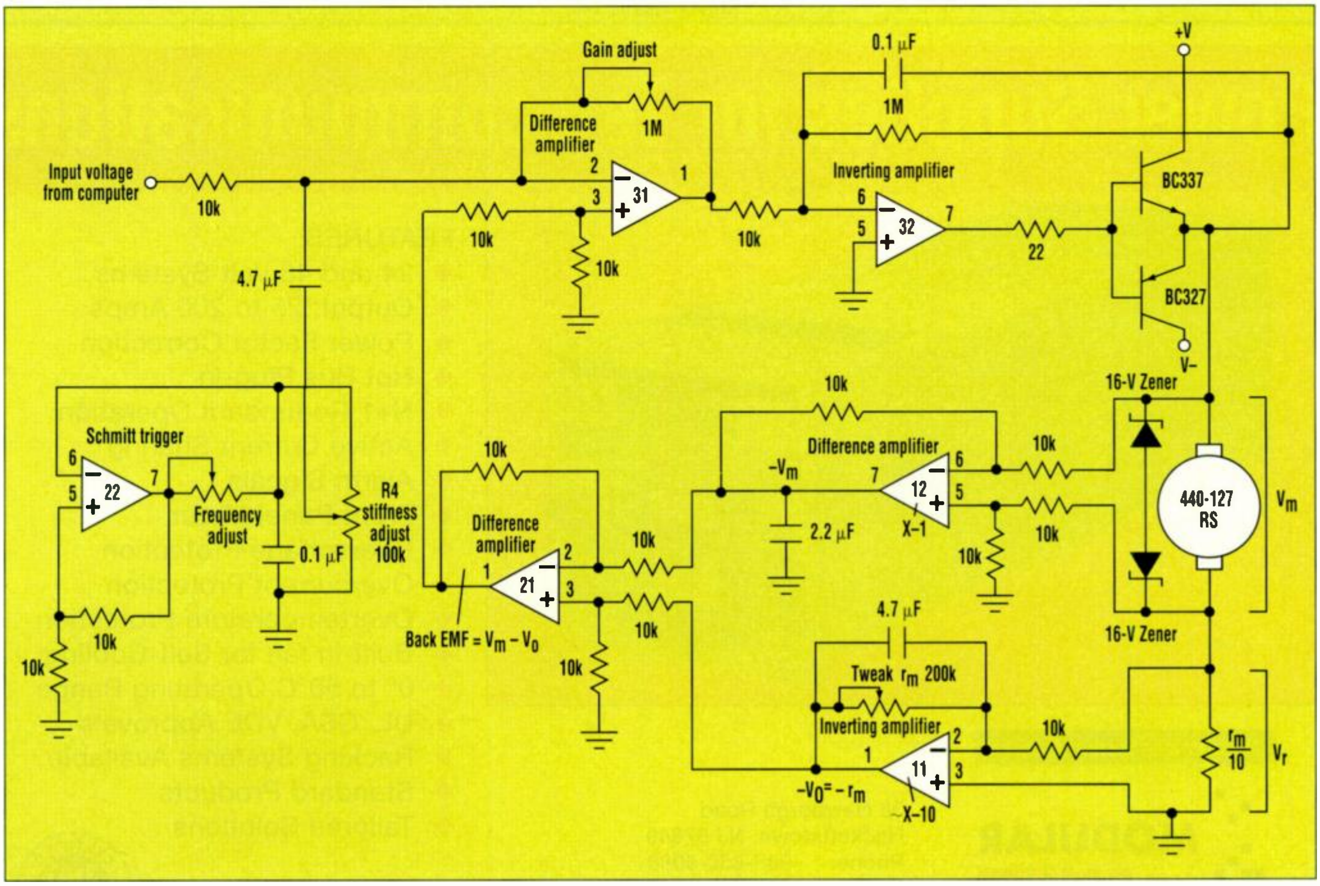
Control Circuit Keeps DC Motor Running At Constant Speed

A.M. WOOSTER
ITAL Structures, Via Monte Misone, 11/D, 38066
Riva Del Garda (TN), Italy.

The aim of the circuit presented here is to keep the permanent magnet dc motor running at a constant speed, set externally. To do this, the current through, and the voltage across, the brushes of the motor are monitored. The voltage consists of two components: First, a back-EMF generated by the windings of the armature moving through the magnetic field of the motor. Secondly, there's a voltage caused by the current passing through the real resistance of the windings and the brushes.

The current through the motor armature is caused to pass through a resistance ($r_m/10$) that is, for example, approximately 0.1 as large as the ohmic resistance of the motor. The voltage across this resistance is then amplified by a factor of approximately 10, and the resulting voltage is added to a second voltage in a differential amplifier. This second voltage is the voltage as measured across the two brushes of the motor.

The output of this amplifier is com-



To maintain a permanent magnet dc motor at a constant running speed, this circuit monitors both the current through the motor armature and the voltage across the commutator brushes of the motor (back-EMF) to regulate the motor output drive signal.

pared to the reference voltage (provided externally to the circuit, which determines the speed of rotation of the motor) in another differential amplifier. The output difference is used to control the output of a power output stage that drives the motor. In this way, the reference voltage is compared to the back-EMF and the motor is caused to run at a constant speed set by the reference voltage. To soften the switch from driving to not driving, a sawtooth waveform is superimposed on the reference voltage.

In the schematic, the voltage across the motor is measured (amp 12), multiplied by minus one and fed to one input of a difference amplifier (amp 21) At the same time, the voltage across resistor $r_m/10$ is measured and multiplied by approximately minus ten (amp 11). This output is fed to the other input of amp 21.

The exact factor by which the voltage across $r_m/10$ has to be multiplied can be set on the pot "TWEAK r_m". To accomplish this, the motor is disconnected from the output stage and fed through a suitable resistor, say 330 Ω, and then stalled. "TWEAK r_m" is adjusted until the output of amp 21 is zero (it may be necessary to use a compromise setting if the value of the resistance isn't the same at all positions of the rotor).

The output of amp 21 is then equal to the back-EMF of the motor (reconnect the motor to the output stage and adjust the gain and stiffness controls to suit your application). This output is fed into one input of a differential amplifier (amp 31) and compared to a reference voltage (provided externally). The output of this amplifier is the error signal and is used to drive the output stage (amp 32, BC337, and BC327) to keep the motor running at the speed at which the back-EMF equals the reference voltage.

The reference voltage includes a small sawtooth component to provide a softer transition from driving to not driving. The size of this component is controlled by the potentiometer labeled "Stiffness Adj." and comes from the oscillator (amp 22), whose frequency is controlled by the pot labeled "Frequency Adj."

The three op amps employed here were from a quad op amp CA0358E; the motor is 440-127. Both are from Radio Shack. But the circuit will work with almost any op amp and dc motor, although the output stage would need more powerful output transistors if a bigger motor is used.

Circle 523

Visible-Laser Driver Has Digitally Controlled Power And Modulation

ROGER KENYON
Maxim Integrated Products, 120 San Gabriel Dr., Sunnyvale, CA 94086; (408) 737-7600.

In the circuit presented here, a 10-bit digital-to-analog converter with a three-wire serial input operates and maintains a visible-light laser diode at constant average optical output power. A separate digital input line (MOD) enables a comparator with open-drain output (IC4) to implement digital communications by pulsing the laser diode via Q1. Circuit components were chosen to minimize the layout area and cost.

Many laser diodes include a photodiode that generates a current proportional to the intensity (optical power) of the laser beam. Most of these photodiodes, however, have relatively slow response times and can't track the peak optical power of a typical modulated laser diode. Instead, the driver circuits for these devices control the laser by monitoring a relative average optical power.

Resistor R6 converts the photodiode current to a usable voltage, which is applied to the inverting input of a "leaky" integrator based on the high-speed op amp IC3. The integrator smooths out variations in the modulation, and prevents the feedback loop from trying to regulate the laser pulses. The integrator is made leaky (by R10) to ensure compensation of downward as well as upward variations in the average power.

Thus, the integrator creates an error signal and base drive for Q1 by monitoring the voltage across R6 and comparing it to the DAC's preset voltage. The DAC's reference voltage (from IC1) is 2.5 V, but its output-voltage buffer has a gain of two, giving the DAC output an adjustment range of 0 to 5 V. With its nominal base voltage set by the DAC output, Q1 controls the optical power by regulating current through the laser diode.

R9 provides isolation and helps to stabilize IC3 when the base of Q1 is being shorted and released by a signal from the MOD input. By maintaining a small laser-diode current during the "off" periods of digital modulation, R1 preempts another problem—startup time for a laser diode increases tremendously if the forward current goes to zero. R1 ensures that the laser current is below the threshold for lasing, but high enough to allow an acceptable turn-on time for communication and modulation.

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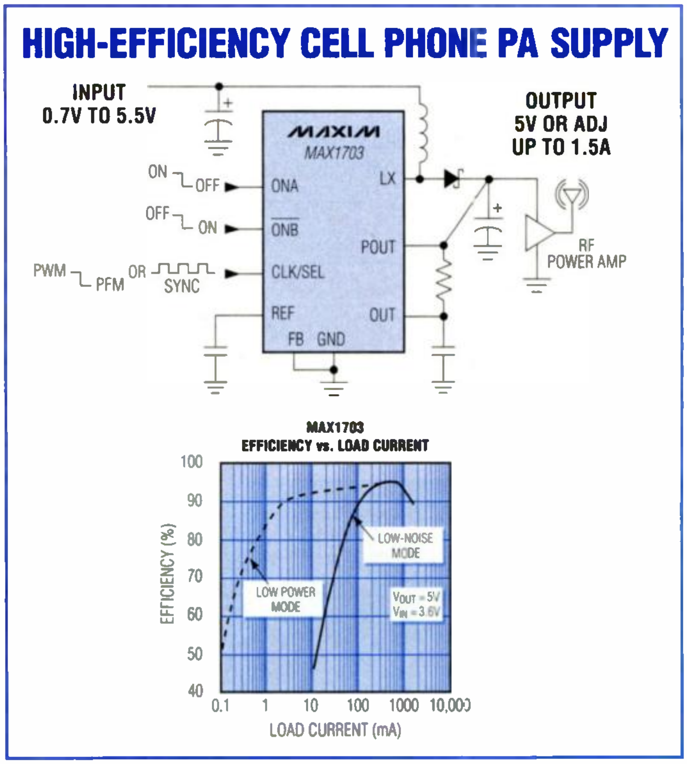

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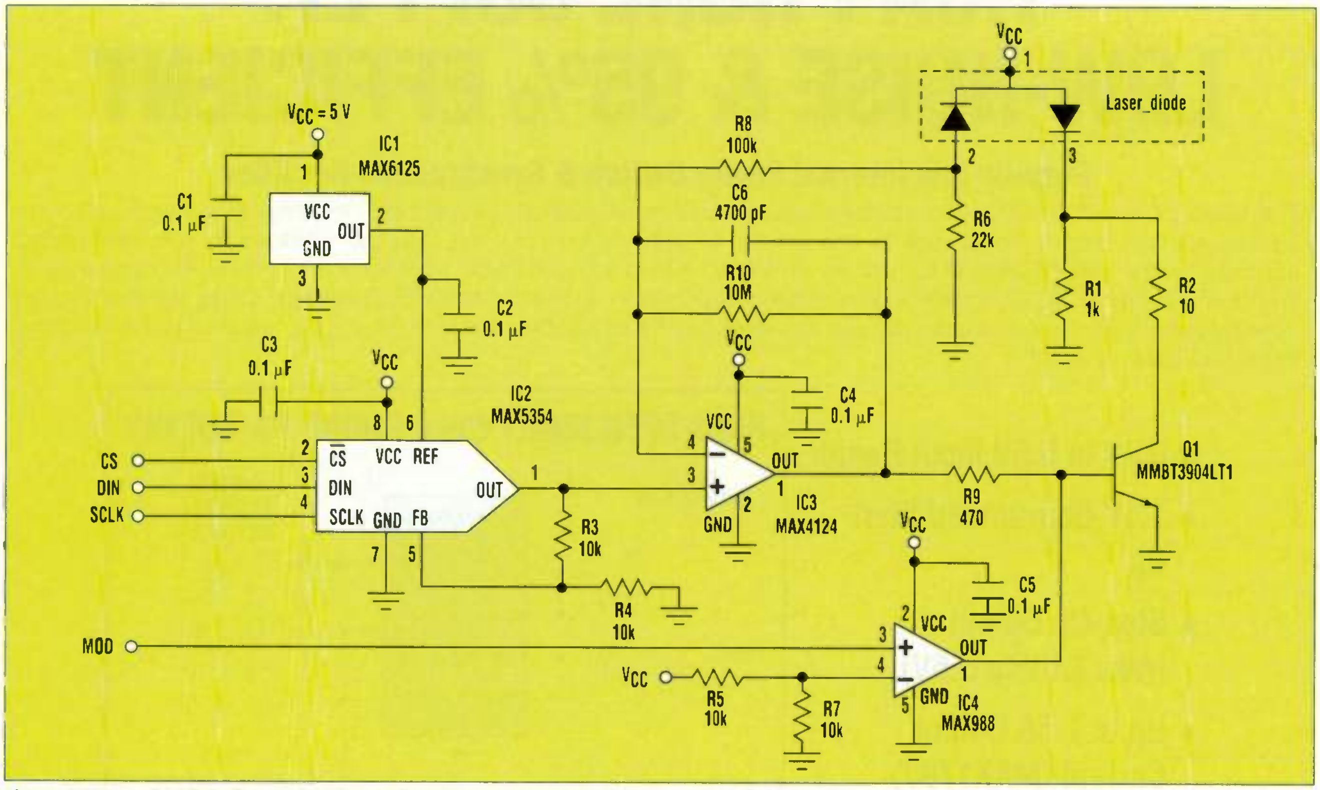

This circuit provides digital control of the modulation and the relative average optical power output of a visible-light laser diode.

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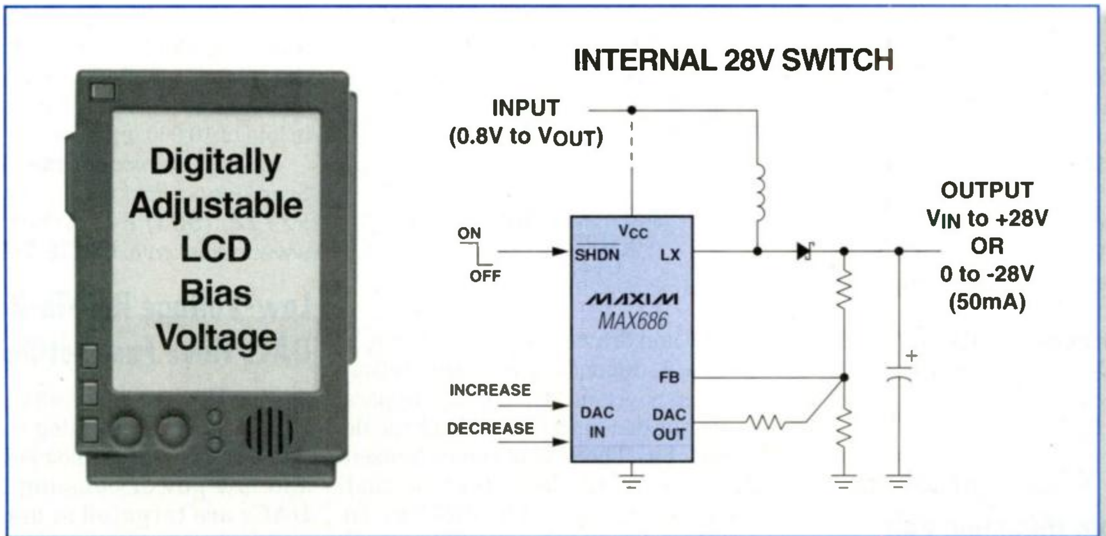

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Circle No. 161 - For International

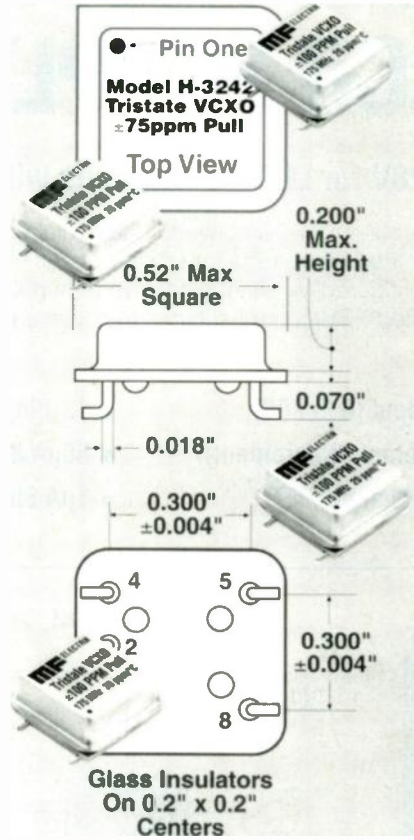
Op Amp's Input Extends Beyond The Rails

Designed for operation from a single +1.8- to +5.5-V supply or dual ±0.9- to ±2.5-V supplies, the MAX4240/4241 provides 90-kHz gain-bandwidth product while consuming only 10 µA of supply current per amplifier. In the shutdown mode, which is offered by the 4241, this reduces to less than 1 µA. In addition, these op amps enable rail-to-rail operation, with the output rated to swing within 9 mV of the rail with a 100-kΩ load. The input common-mode range is guaranteed to exceed either rail by 200 mV. Beyond the rails, input is made possible by the input stage comprising separate npn and pnp differential pairs operating in parallel. As a result, the input offset is as low as 250 µV.

These features make the device suitable for systems powered by two-AA alkaline cells. The MAX4240 comes in a 5-pin SOT23, and the MAX4241 is housed in an 8-pin µMAX/SO packages. The family also includes dual and quad versions, the MAX4242/4243 and MAX4244. In 10,000-piece quantities, the MAX4240 is priced at $0.79. AB

***Maxim Integrated Products,** 120 San Gabriel Dr., Sunnyvale, CA 94086; 1-800 998-8800; www.maxim-ic.com.* **CIRCLE 557**

Tristate VCXO Guarantees ±75-ppm Minimum Pull



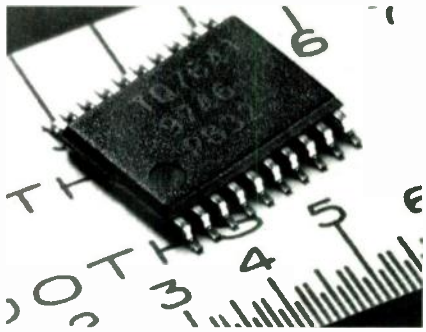
Covering center frequencies from 3 to 175 MHz, model H3242 is a surface-mountable voltage-controlled crystal oscillator (VCXO) that provides tristate operation and guarantees ±75-ppm (minimum) frequency pull range. The maximum frequency pull range for the oscillator is ±150 ppm, for a tolerance of 2:1.The control voltage range for the unit is 0.5 to 4.5 V. Consequently, the VCXO's actual frequency/voltage characteristics lies between the minimum and maximum pull extremes. Tight pull tolerance ensures high linearity, and minimizes frequency deviation.The oscillator's center frequency error is less than ±20 ppm over the temperature range of 0° to +70°C. Excellent linearity control suits the unit for advanced phase-locked-loop (PLL) circuits.

The VCXO operates from a 5-V supply and draws current from 30 mA to 45 mA, depending on the operating frequency. An internal 0.1-µF bypass capacitor decouples noise from the dc supply bus.The H3242 comes housed in a type-H stainless-steel can that measures 0.5 by 0.5 by 0.215 in. In OEM quantities, the H3242 is priced at $24.50. AB

***MF Electronics Corp.,** 10 Commerce Drive, New Rochelle, NY 10801; (800) 331-1236; www.mfelectronics.com* **CIRCLE 558**

3-V PAs Target DCS-1800 And PCS-1900 Handsets

While the TQ7541 is a high-efficiency power amplifier developed for DCS—1800 handsets operating in the 1710- to 1785-MHz frequency range, the TQ7641 is optimized for the PCS-1900 phones operating in the 1850- to 1910-MHz uplink band. Based on a low-voltage gallium-arsenide (GaAs) MESFET process, the new power amplifiers operate from a single 3-V supply. The units amplify GMSK (Gaussian minimum-shift keying) modulated signals, and provide a saturated output power of 32 dBm. Typical power-added efficiency for the TQ7541 is 45%, and 44% for the TQ7641. To achieve this performance, the RF amplifiers integrate a three-stage PA with on-chip negative voltage generator, bias control, supply



management logic, baseband interface, and 50-Ω matched input. Both the power amplifiers are housed in 20-lead plastic TSSOPs. Pricing is $5.59 in lots of 10,000 units. AB

***TriQuint Semiconductor,** 2300 N.E. Brookwood Parkway, Hillsboro, OR 97124; (503) 615-9000; Internet: www.triquint.com.* **CIRCLE 559**

Low-Voltage Rail-To-Rail DACs Have Fast Settling Time

Analog Devices offers three 8-bit rail-to-rail digital-to-analog converters (DACs) that feature fast settling time and low power consumption. The DACs are targeted at applications such as battery-powered instruments and programmable attenuators. All devices operate over a supply range of 2.7 to 5.5 V.

The dual AD7303 is a single-supply, general-purpose DAC featuring on-chip precision output buffers with true rail-to-rail output. It consumes 5 mW at 3 V, and has a 1.2-µs settling time (typical). The single AD7801 and the dual AD7302 offer the same features and settling time, but with respective typical power consumptions of 1.75 and 3 mA at 3.3 V. The AD 7303 comes in an 8-pin micro-SOIC, and is priced at $2.35 in 1000-piece quantities. The AD7302 and AD7801 are packaged in 20-pin TSSOPs and are priced at $2.00 and $1.80, respectively. LM

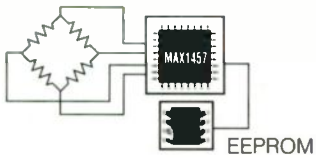
***Analog Devices Inc.,** Ray Stata Technology Center, 804 Woburn St., Wilmington, MA 01887; (617) 937-1428; www.analog.com.* **CIRCLE 560**

Evaluation Kit Includes Pressure Sensor

SIGNAL CONDITIONER DIGITALLY COMPENSATES SENSORS TO 0.1% ACCURACY

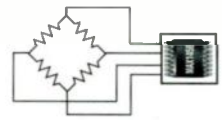
Eliminate Bulky Front-End Circuitry
Eliminate Manual Compensation Adjustments

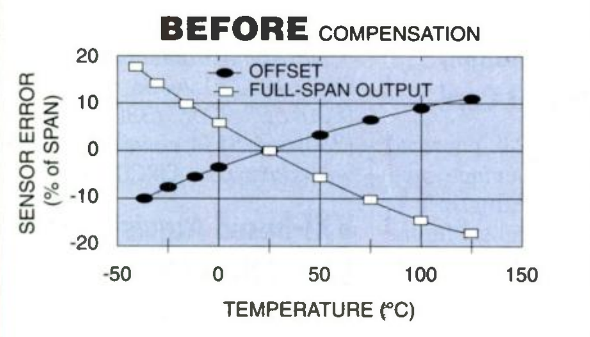
0.1% ACCURATE MAX1457

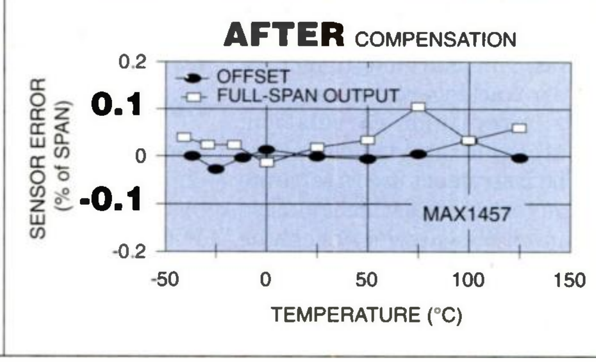


1% ACCURATE MAX1458

(INTERNAL EEPROM)







Simplify sensor manufacturing with Maxim's new signal-conditioning ICs. The highly-integrated MAX1457/MAX1458 provide digital compensation for linearizing piezoresistive sensor outputs. Alternatives to manual adjusting of trim pots, these devices greatly simplify and accelerate the process of manufacturing compensated sensors by digitally adjusting offset, offset TC, full-span output (FSO), FSO TC, and linearity. The MAX1450 is a low-cost sensor building block.

PART	ACCURACY* (%)	FEATURES
MAX1457	0.1	Current Source, PGA, 5 Adjustment DACs, Temperature ADC, Auxiliary Op Amp
MAX1458**	1.0	Current Source, PGA, 4 Adjustment DACs, Temperature Sensor, On-Chip EEPROM
MAX1450**	1.0	Current Source, PGA

*Accuracy is limited by inherent repeatability of the sensor error. **Future product—available after May, 1998.

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Circle No. 162 - For U.S. Response
Circle No. 163 - For International

Signal Analyzer Boasts 100-kHz Bandwidth On 2 Channels

The SR785 dynamic signal analyzer features a true, two-channel, 100-kHz real-time bandwidth, a noise floor of –160 dBVrms per root Hertz, a 90-dB dynamic range in FFT mode, and a 145-dB dynamic range in swept-sine

mode. Basic measurements include FFT, order tracking, real-time octave analysis, swept-sine correlation, time/histogram, and time capture mode. The instrument uses a separate 16-bit converter for each channel so two-channel measurements can be made to 102.4 kHz. Users can define math functions to perform just about any time-, frequency-, or amplitude-domain measurement.

The unit's low-distortion source (–80 dBc) generates sine, two-tone, white and pink noise, burst, chirp, and arbitrary waveform outputs. Standard data memory is 8 Mbytes, expandable to 32 Mbytes, and frequency resolution is up to 800 lines. Data-analysis capabilities include band, sideband, and harmonic analysis and pass/fail testing. The SR785 costs $10,950. JN

***Sanford Research Systems Inc.**, 1290-D Reamwood Ave., Sunnyvale, CA 94089; (408) 744-9040.* **CIRCLE 561**

Portable 5-Slot VXI Chassis Are Small And Lightweight

The CT-300 series five-slot, C-size VXIbus mainframes were designed for easy portability, with light weight and a very small footprint. The units feature a modular plug-in power supply and fan assembly and are available in both ac and dc versions. All supply lines are monitored, fused, and available to the user to drive the unit under test. With the company's VXIbus Modular Instrumentation Platform, the five-slot mainframes can hold up to 12 high-performance instruments. The CT-300 chassis costs $3400. Delivery is in four to six weeks. JN

***VXI Technology Inc.**, 17912 Mitchell, Irvine, CA 92614; (714) 955-1894; fax (714) 955-3041; www.vxitech.com.* **CIRCLE 562**

RS-232 Powers 8-Channel, Network-Capable I/O Card

The T8AH7BA is an RS-232-powered eight-channel analog interface card based on Dallas Semiconductor's 1-Wire technology. Users can configure each channel individually as a 0- to 5-V, 12-bit analog input. The board includes a multidrop controller that provides a unique 64-bit registration number that ensures error-free selection and absolute identity of the device. This technology virtually eliminates addressing confusion.

The card connects directly to 7B-series industrial standard analog isolation backpanels and modules. The built-in RS-232-to-1-Wire interface allows network expansion for driving up to 200 1-Wire devices over as much as 2000 ft. of CAT-5 twisted-pair cable. All data transfers are CRC 16 error checked. The included DDE driver offers interfacing to most Windows applications. Call for price and availability information. JN

***Point Six Inc.**, 138 E. Reynolds Rd., Suite 201, Lexington, KY 40517; (606) 271-1744; fax (606) 271-4695; www.pointsix.com.* **CIRCLE 563**

14-Bit Data-Acquisition Card Has Fast Sample Rate

The DI-410-PGH data-acquisition card offers 16 single-ended (eight differential) analog inputs with 14-bit conversion. It also has dual 14-bit digital-to-analog outputs and eight digital I/O channels. All calibration is done electronically. For high-speed data acquisition, the card has a 15,000-sample FIFO buffer. The ISA-based unit features an on-board 32-MIPS digital signal processor. Maximum acquisition speed is 125,000 samples/s using burst mode to minimize channel skew. Users can independently program each channel for sample rate; gains of 1, 2, 4, or 8; and single-ended or differential configuration. Also each channel can be in average, maximum, minimum, or last-point mode. The card comes with a software development kit for Windows and DOS; the WinDaq/Lite data-acquisition, playback, and analysis software; and WinDAQ Waveform Browser. LabVIEW, TestPoint, and HP VEE drivers are included. The DI-410-PGH card costs $1195. Delivery is from stock. JN

***DATAQ Instruments**, 150 Springside Dr., Suite B220, Akron, OH 44333-2473; (800) 553-9006; (330) 668-1444; fax (330) 666-5434; e-mail: info@dataq.com; www.dataq.com.* **CIRCLE 564**

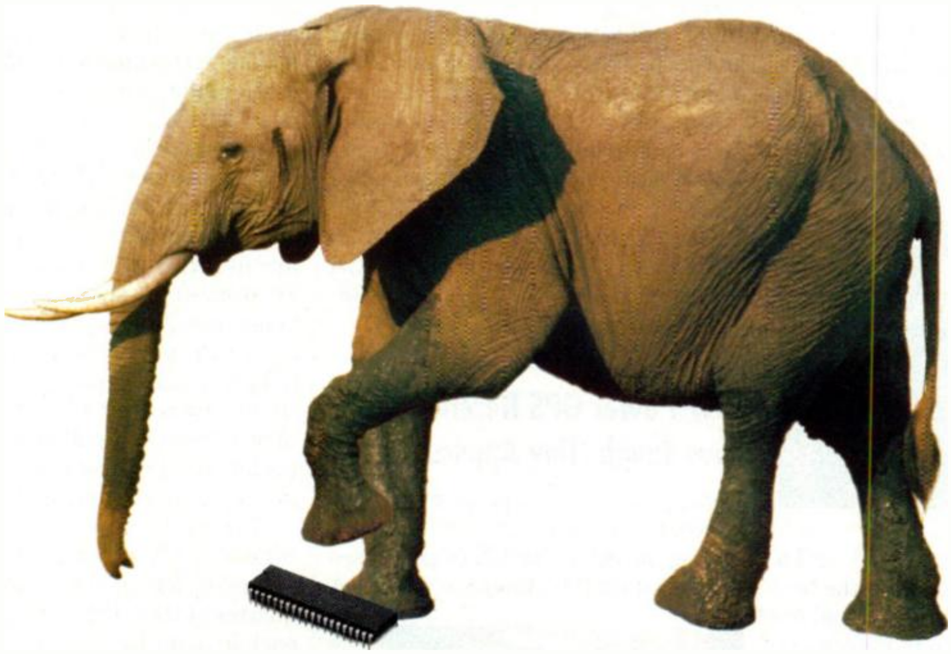
VXI-based Acquisition Line Sports High Channel Counts

The ProDAQ Series is a new VXIbus-module platform for data acquisition. Based on the 6700 Series motherboards with up to eight interface ports for function cards, one VXI slot can accommodate 384 digital I/O channels, 192 analog input channels, or 128 analog output channels. Those channel counts can be multiplied by 12 for a 13-slot mainframe with one slot 0 module. The first products in the series include the 6753 motherboard module and three function cards: the Type A with 48 digital I/O channels, the Type C with 24 16-bit analog inputs, and the Type D with 16 16-bit analog outputs.

The motherboard's comprehensive trigger matrix allows systems to handle nested trigger requirements. The function cards provide an autonomous data-acquisition mode, permitting a complete scan of data to be performed in hardware without software intervention. The ProDAQ modules come with full-function VXI*plug&play*-compatible drivers and operate with LabWindows/CVI and LabVIEW. Prices start at $1695 and delivery is in 8 to 12 weeks. JN

***Racal Instruments Inc.**, 4 Goodyear St., Irvine, CA 92618; (800) 722-2528; fax (714) 859-7139; Internet: www.racalinst.com.* **CIRCLE 565**

IS FLASH SMASHING EPROM?



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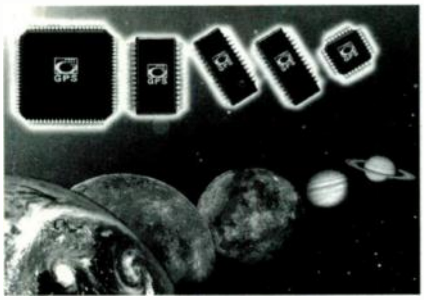
TOWER SEMICONDUCTOR USA INC.

READER SERVICE 203

First Dual-Band RF Chip Set For CDMA Cellular/PCS Phones

Code-named "Planets," the world's first dual-band integrated RF chip set enables designers to slash the cost and size of handsets that can operate both in the 900-MHz cellular band and the 1.9-GHz PCS band. Consisting of an RF front end, an IF demodulator, a fil-



ter ASIC, a transmit device, and a baseband and audio interface, the five ICs perform all of the transmit and receive functions required to implement the RF section of an IS-95 CDMA-based phone. The Planets chip set interfaces directly to Qualcomm MSM2-compliant and other CDMA baseband processors. This provides an antenna-to-microphone solution that can operate at supply voltages as low as 2.7 V.

Each of the five ICs in the chip set is named after one of the planets in the solar system. Venus is an RF receiver equipped with dual ports to accommodate both 900-MHz and 1900-MHz inputs, as well as two local oscillators and buffer amps. Saturn is an IF receiver equipped with selectable IF input buffers that can be used for both IF CDMA and FM SAW filter outputs. It incorporates AGC amps that provide –45 to +50 dB of gain. Jupiter is a CDMA and FM I/Q filter designed for low voltage operation. It employs a gyrator-based filter to provide low in-band and eliminate the problems associated with on-chip inductors or off-chip passives.

The Pluto chip interfaces the RF front end to the baseband processor section. It consists of a set of ADCs and DACs, plus two VHF synthesizers. The interface converts analog I/Q signals to equivalent digital bit streams in the receive direction, and reconstitutes outgoing digital signals back into analog form for processing by the RF section. Moon is a dual-band transmit circuit that includes an on-chip active upconversion mixer and active filter. AGC functions are split between the RF and IF sections to improve performance and reduce cost. An extensive set of application notes, development and debug software, evaluation boards, and reference designs also is available.

Due in early April, the Planets chip set is housed in SSOP and QSOP packages. Pricing is $67.16 in quantities of 10,000 units. LG

***GEC Plessey Semiconductors**, 1500 Green Hills Rd., Scotts Valley, CA 95067; attn: Andrew Burt (408) 438-2900; www.gpssemi.com.*
CIRCLE 566

Low-Power GPS Receiver Chips Love Tough, Tiny Applications

Designed for GPS applications where space, power, and signal quality are scarce, the SiRFstar/LX chip set uses advanced DSP techniques and strict

power management to maximize battery life. Drawing 10% or less of the power required by conventional receivers, the receiver brings position awareness to such unlikely places as cellular phones, PDAs, and other handheld devices.

The chip set consists of three components: the GRFX/LX, a front-end RF chip; the GSP1/LX, a GPS signal processor chip; and the GSW/LX software package. The GRF1 RF front end converts GPS signals from the 1.575-GHz carrier frequency into baseband signals. To save power, cost, and space, the GRF1 incorporates an on-chip VCO and an interface that connects directly to most passive and active antennas.

Its companion chip, the GSP1, employs a parallel-processing DSP architecture that's been optimized for GPS-related functions. The 12-channel receiver has an on-chip bus that connects it to a pair of integrated UARTs, a host CPU interface, a memory controller, and a baseband RF interface. When running with its modular software, it can produce up to 10 position fixes per second. Other modules include a customer-controllable receiver manager, tracking loops, data demodulation, navigation filtering, a standard API interface, and drivers for PC-oriented applications.

To cope with difficult urban environments, where buildings often obstruct much of the sky, the SiRFstar architecture can maintain position awareness for short periods using a single satellite, and reacquire others in as little as 100 ms. The device's signal-processing capability lets it effectively eliminate multipath signals in urban areas and pull in weak signals (as low as –180 dBw) that are attenuated by trees in rural areas.

Available now, samples of the SiRFstar/LX are available now, with full production slated for the first quarter of 1998. Pricing is set at $29.95 each in quantities of 10,000 pieces. A complete software/hardware development kit also is available for $995. LG

***SiRF Technology Inc.**, 3970 Freedom Circle, Santa Clara, CA 95954; (408) 980-4700; fax (4080 980-4705; www.sirf.com.* **CIRCLE 567**

Ultra-Low Power PLL Pumps 1.2 GHz At 1 V

Fabricated in Ultra-Thin Silicon (UTSI) technology, the PE3292, a 1.2-GHz/550-MHz dual fractional-N phase-locked loop (PLL), provides a precise, low-power frequency source for nearly any handheld wireless product. It can operate with variable prescalar supply voltages down to 1 V for low-power operation. Typical power consumption is only 3.9 mW when the RF PLL operates at 900 MHz and the IF PLL is at 300 MHz. The fractional architecture provides excellent phase noise and very small step sizes. Built-in spur compensation ensures that no external tuning is required. Housed in a 20-pin TSSOP, the PE3292 will begin sampling in the second quarter of this year. Pricing will be announced soon. LG

***Peregrine Semiconductor Corp.**, 6175 Nancy Ridge Dr., San Diego, CA 92121; (619) 455-0660, fax (619) 455-0770; www.peregrine-semi.com.*
CIRCLE 568

har-bus®64 New 160 Pin Connector For VME64

New series satisfies the new 64 bit computer architecture's requirement for higher speeds, more I/O and additional functionality. Offering a five row connector solution that is 100% backward compatible with the popular 96-pin Eurocard connectors, the new ***har-bus® 64*** has 160 pins with preleading contacts for live insertion. New contact rows can be used to improve signal speed of VME bus and as ground contacts. Current 96-pin Eurocard connectors mate to the 160 pin connectors, allowing all PCB's to be used in new or existing backplanes.

READER SERVICE 234

har-pak® 2.5MM High Density Connector System

Developed for backplane and daughter board applications in modern rack systems. The 5 row 2.5 mm connector design offers solderless PCB terminations, optimum utilization, of space three dimensional modularity, high contact density, EMI protection, and the ability to double-side surface mount components on daughter cards without loss of a 15mm card pitch. The *har-pak* connector system permits using a three dimensional 2.5mm grid. Only one connector style is required to solve your power, signal, ground, and high data rates, simplifying the design and manufacturing of future systems. The compliant pin technology utilizes the same 1mm plated through hole standard for many DIN 41612 compliant pin technologies. Consistency in design uses the many years of manufacturing and design experience already available. These attributes combined can lead to new advancements in board-level designs: 15mm card pitch with double-sided surface mounted daughter cards, butterfly or mid-plane techniques, modular design both horizontally and vertically, low number of system components combination with other standardized packaging systems, and lower applied costs.

READER SERVICE 237

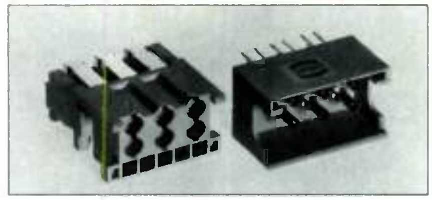
New SEK "Press'n Snap" Press in Header

Low profile press-in headers can be added to single or double-sided surface mount printed circuit boards any time after reflow. Press-in terminations of the two row .100" pitch headers permit easy installation into plated through holes without soldering. Removable temporary inserts allow any flat die to press the connectors. The straight header is shrouded by four plastic walls and available in versions from 6 to 64 contacts. The mating connectors are flat ribbon terminated socket connectors from HARTING's SEK range. These can be latched to the headers by using the locking levers installed onto the strain relief. The levers secure the socket connector to the end walls of the

header. Placing the locking levers on the socket instead of the PCB header saves valuable board real estate.

READER SERVICE 235

NEW HIGH DENSITY MICRO-COAXIAL CONTACTS



Designed for high speed data transfer rates. Can be used in the iec 1076-4-2 2.5mm High Density connector system, *har-pak®* Provides more space efficiency, high frequency capability, easy handling, low applied cost and application with current equipment and emerging metric equipment practices. Designed for PCB termination on both daughter card to backplane connection; allowing users to bring signal directly into the backplane without a cable transition.

READER SERVICE 236

READER SERVICE 238

Preamble, the Performance Leader in Differential Measurement.

Microvolts to Kilovolts!

Model 1822
DC-10 MHz
X1000 Gain
16 upper & lower
BW limits

NEW

Model 1855
DC-100 MHz
X10 Gain
Very fast
recovery
from overdrive

Preamble 1800 Series stand-alone differential amplifiers are designed to function as signal conditioning pre-amplifiers for your oscilloscope, spectrum or network analyzers.

Model 1855 combines Gain, High CMRR, Very Fast Overdrive Recovery and Wide Common Mode Range to simplify direct measurement of such difficult signals as a switching supply upper gate drive.

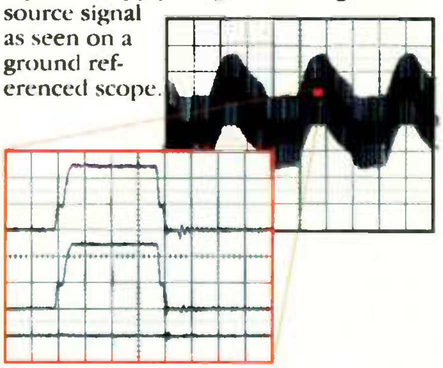
Model 1822's X1000 Gain can extend your scope's sensitivity to 1μV/div and includes a full complement of upper and lower bandwidth limits. Strain gauge, bio-medical and other physical parameters are well within the reach of the 1822.

Preamble XC Series Differential Probes give the user a choice of X1, X10, X100 and X1000 attenuation factors and circuit loading as low as 92 meg/4.5 pF. They facilitate differential measurements from microvolts to kilovolts.

The **1800 Series** sport the industry's widest common mode range; limited only by the probe's voltage rating.

Measurements in off-line switching power supply primaries become safe, accurate and easy-to-make.

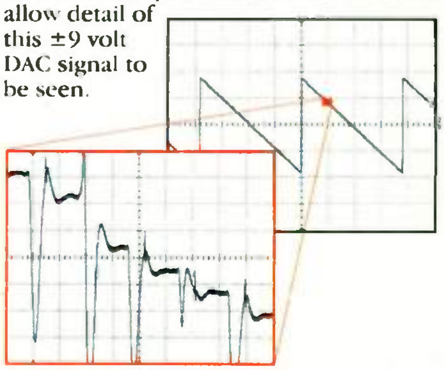
CONVENTIONAL
A power supply's highside FET gate to source signal as seen on a ground referenced scope.



DIFFERENTIAL
The 1855 rejects the line voltage and high dv/dt signal, cleanly displaying the upper and lower gate drive signals.

Preamble's 1800 Differential Amplifier Series low noise, wide common mode range and Precision Offset Generator allow minute portions of very large signals to be examined with 5½ digit resolution.
The generator acts as a precision position control and extends your scope position range to over ±150,000 divisions; the industry's tallest display!

CONVENTIONAL
A scope lacks sufficient position range and lacks the ability to recover from overdrive to allow detail of this ±9 volt DAC signal to be seen.



DIFFERENTIAL
The 1800 Series allow the individual DAC steps to be examined at any point on the wave-form and measured to 5½ digit resolution.

PREAMBLE INSTRUMENTS

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Distributors Boost Product Lines With Semiconductor Offerings

Strategic partnerships between several semiconductor companies and distributors have opened new avenues for designers. Hamilton Hallmark is now offering Hitachi Semiconductor (America) Inc.'s full line in North America. EBV Electronics Inc. became Scenix Semiconductor Inc.'s North American distribution partner. Peregrine Semiconductor Corp. signed on with Insight Electronics. And, All American Semiconductor Inc. is distributing products from SMART Modular Technologies Inc. and Clear Logic Inc.

"We are extremely excited about our new relationship with Hitachi," says Steve Church, president of Avnet OEM Marketing Group, which includes Hamilton Hallmark. "We anticipate that with Hitachi's leading technology products and Hamilton Hallmark's expertise in technical support and value-added services, we will be able to increase our combined value to our broad customer base."

At Scenix Semiconductor, Steve Leung, chief executive officer and cofounder, notes that "EBV is exactly the distribution partner we were looking for to help us grow our design base and open doors with new customers in North America. Not only will they stock and distribute our SX series of microcontrollers, but they'll be able to use their engineering-focused approach to help customers in the development phase of their designs." He says this would be particularly important for embedded applications of the 8-bit device.

Insight's exclusive agreement with Peregrine Semiconductor includes the latter's high-performance ICs designed for the wireless and satellite communication markets. "We're excited Peregrine now has the distribution sales power of a giant like Insight," says Milt Miller, Peregrine's director of sales. "Insight's demand-creation approach will be instrumental in helping us reach and serve customers who have our UTSi [Ultra-Thin Silicon] CMOS RF product line," Miller continues.

The agreement with SMART Modular Technologies "enables All American to effectively compete in a greater percentage of the complex memory applications, to include high-speed SDRAM and high-density flash memory module applications," according to George Parajohn, All American's vice president of marketing. "SMART's other product segments, modems and embedded computing, are synergistic with All American's flat-panel display solutions. SMART gives All American more options to help customers develop comprehensive, embedded display solution products," he says.

Clear Logic is a fabless manufacturer of ASICs, specializing in converting FPGA-based designs into lower-cost ASICs. The addition of the startup company "complements our offerings, which include FPGAs from Atmel as well as ASICs from Atmel, AMI, and Samsung," said Papajohn.

EDS Event Strives To Grab Smaller Firms

One of the goals of this year's Electronic Distribution Show (EDS) is to attract the participation of the emerging smaller, hybrid distributors while maintaining the event's value for larger manufacturers and distributors. The need for such emphasis comes out of an EDS Task Force comprising EDS directors, trade association executives, and staff, according to the National Electronic Distributors Association (NEDA).

The result is The Newcomers Pavilion, which accommodates startups, companies with small distributor rosters, and other manufacturers who want to try out the show without making a major financial commitment. Participants will get a mini-booth, with a furnished semiprivate table-top display for two of the three show days, for $750. Organizers hope the newcomer executives will use the third day to tour the rest of the show. In addition, leaders of the Electronic Industries Association (EIA) Components Group will mentor newcomers.

NEDA will hold its annual breakfast on May 12, the show's first day, featuring a talk by Tom Connellan, an expert on customer service. A breakfast meeting also will be sponsored by the Electronic Representatives Association (ERA) and the EDS on May 13 and, for the first time, the EIA and the EDS will jointly sponsor a breakfast meeting on May 14.

The EDS, cosponsored by the NEDA, EIA, and ERA, will be held at the Las Vegas Hilton. Registration is free to NEDA members until May 5. A $10 administrative fee will apply thereafter. For more information, call (312) 648-1140 or visit www.edsc.org.

Lambda Goes Distributor Route, Signs On With Time Electronics

For the past 50 years, Lambda Electronics has been the sole source for its line of power supplies. But that has changed now, with the recent signing of an agreement that makes Time Electronics the exclusive distributor for Lambda's power supplies in the U.S., complementing the manufacturer's direct sales efforts.

Ted Greene, Lambda's director of distribution, says Time Electronics has the market penetration, services, and information technology expertise to transition customers from a direct-supply relationship. "We feel that Time Electronics has the resources and market experience to help grow our customer base, and help our current customers adjust to a distribution supply model," Green asserts. "In addition, by offering a large number of value-added services, including materials management, power-supply modification, and a variety of online services, Time offers us exactly the kind of customer support we want in a distribution partner," he says.

Time Electronics president Burton Katz says his company, a member of Avnet's OEM Marketing Group, was "particularly delighted" about the agreement, and cited Lambda's broad capabilities in both off-the-shelf and custom power supplies. "This fits with Time's strategy of aligning itself with the industry's premier suppliers to provide our customers with a complete offering of interconnect, passive, and electromechanical products," according to Katz.

DISTRIBUTOR SHELF

Pioneer Sets Up New Services For Contract Manufacturers

Recognizing the growth of the contract-manufacturing industry, Pioneer-Standard Electronics has created a new sales segment, Electronic Manufacturing Services (EMS), within its Industrial Electronics Div. Through EMS, Pioneer will offer a wide range of products and services, including information management, enhanced market and product knowledge, and supply-chain solutions.

"Contract manufacturers' needs are changing because the market is increasingly outsourcing more business and services to them," says Tom Pitera, vice president of sales for the Industrial Electronics Div. He noted that contract manufacturing is predicted to be a $125 billion business by 2000.

EMS will serve as an additional channel for Pioneer's suppliers to reach this market segment. The service will provide a full complement of electronic components, including semiconductors and interconnect and computer products. It also will offer automated quote-and-order management response systems, develop a knowledge center for worldwide pricing, and provide inventory logistics support. The new business unit will be headed by Gary Miller, EMS segment vice president.

Specialty Distributor Brings Parts Catalog Online

Richardson Electronics, LaFox, Ill., has launched RELL Online, an electronic catalog containing a database with information on more than 100,000 parts used by a variety of niche markets. Through the company's web site (*www.rell.com*), users can perform searches by part number or parameters; find source-related part information; and view datasheets for electron tubes, RF and microwave components, power semiconductors, display products, and CCTV and security equipment. Later in the year users will be able to check inventory levels and place orders.

Compiled and edited by John Novellino, jnovellino@penton.com, (201) 393-6077.

HOME PAGE WEB SITE

ELECTRONIC DESIGN CATALOG/LITERATURE REVIEW

GIANT NEW SWITCH CATALOG

APEM's new 420 page full-line catalog is packed with their switch offerings. New products added: toggles, rockers, push-buttons, tacts, keys, industrial controls, DIPs, rotary DIPs, micro-limits, pushwheels, slides, keyboards, sealing boots. Many state-of-the-art switch models featuring process compatibility, surface mounting technology & electrostatic discharge withstanding. APEM Tel: 718-246-1007, Fax: 718-245-4531, URL: http://www.APEM.com E-Mail: info@APEM.com

CIRCLE 248

APEM

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TAL TECHNOLOGIES, INC.

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CIRCLE 250

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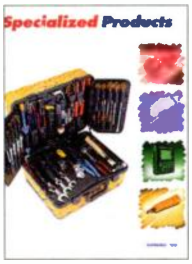
CASES, TOOLS AND TEST EQUIPMENT, SPC's FREE 384-page color catalog features 100+ installation, field service and repair tool kits. Modified and custom kits available. Electronic test equipment includes DMMs, datacom testers, oscilloscopes, power analysis equipment, benchtop test equipment and more. Phone: (800) 866-5353; FAX: (800) 234-5353.



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and Servo Products. Hansen offers DC and Stepper motors. DC motors are used in automotive, office machine, and computer peripheral industries. Stepper motors are designed for precision motion control applications like computer peripherals, office machines and HVAC. Hansen is ISO 9001-94 registered. Sales phone (812) 385-3415. Fax (812) 385-3013.

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COMPUTER DYNAMICS

DATA CONVERSION PRODUCTS

DDC's extensive line of data conversion products and components for MIL-STD-1553 Data Bus, Synchro/Resolver, Commercial Herospace, Power Hybrids and Solid State Power Controller applications is presented in this new, 544-page catalog.

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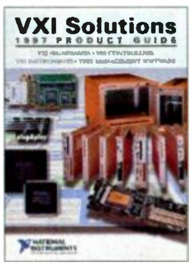
ILC DATA DEVICE CORP.

FREE VXI SOLUTIONS GUIDE

The 1997 VXI Solutions Product Guide is a catalog and technical reference featuring product information on controllers, software, and our new VXI-DAQ instruments. VXI Solutions also includes a directory of over twenty VXI system experts from our Alliance program. Phone: (512) 794-0100; (800) 433-3488 (U.S. and Canada); Fax: (512) 794-8411; e-mail: info@natinst.com; www.http://www.natinst.com



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NATIONAL INSTRUMENTS

NEW MICRO PITCH APPLICATION GUIDE

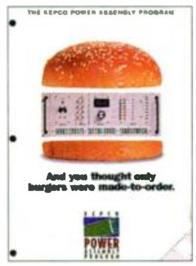
Samtec's Micro Pitch Application Guide. The booklet is divided into the following sections: Module-to-Board, Display Modules, Micro Storage Systems, Expansion Bays, micro and zero profile applications and one-piece connectors. For more information contact Samtec, Inc., P.O. Box 1147, New Albany, IN, 47151-1147. Phone: 800-SAMTEC9, or Fax 812-948-5047. Internet: www.samtec.com

CIRCLE 258

SAMTEC

KEPCO POWER ASSEMBLY PROGRAM

Selection of front & rear metering, connection, signaling and adjusting panels may be custom configured for your needs. Brochure 146-1863 describes Kepco's Power Assembly Program, how to select modules, options available for your assembly, how your system will be configured & documented. Kepco Inc., Tel: (718) 461-7000, email: hq@kepcopower.com, www.kepcopower.com.



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KEPCO

PRODUCT SELECTION GUIDE

CP Clare has published a new 32-page product selection guide to provide engineers with easy reference for their Advanced Magnetic Products, Circuits, Reed Relays, and Switches, and Surge Protection Products. Call 1 800 CPCLARE or visit www.cpclare.com

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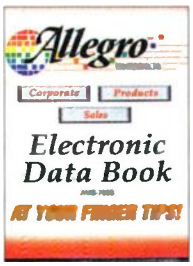

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ALLEGRO MICROSYSTEMS

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C&K COMPONENTS, INC.

ELECTRONIC DESIGN CATALOG/LITERATURE REVIEW

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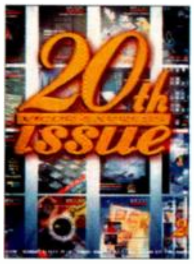

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VICOR CORPORATION

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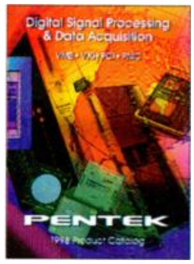

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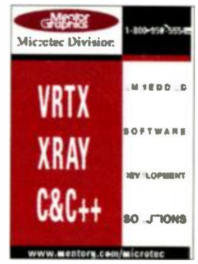

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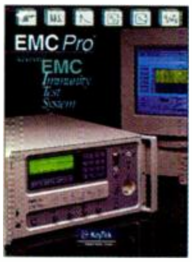

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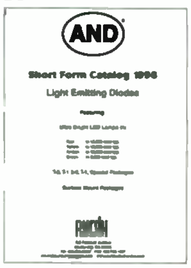

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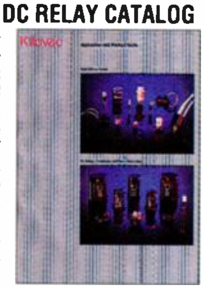

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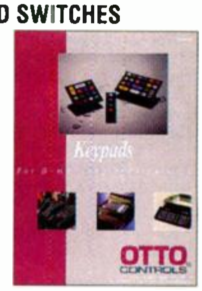

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OTTO CONTROLS

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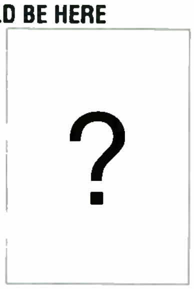

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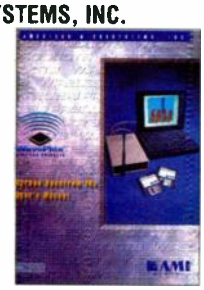

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AMI

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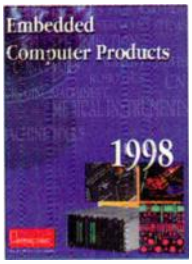

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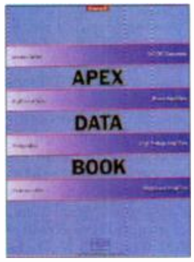

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APEX

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The Data I/O catalog is the direct-order source of affordable tools for users of programmable devices. From design software to device programming and automated handling systems, the Data I/O catalog offers unbeatable values on the high quality tools you need. Call 1-800-332-8246, ext. 806

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DATA I/O

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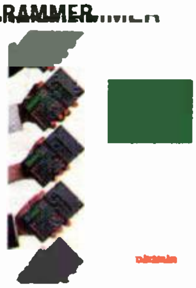

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DATAMAN

NEW OEM POWER SUPPLY CATALOG

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DELTRON

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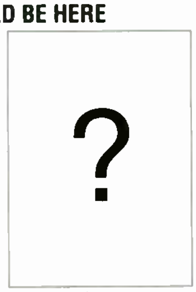

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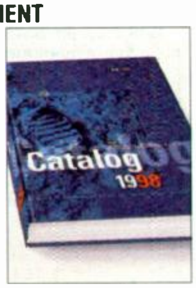

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OCTAGON SYSTEMS

ELECTRONIC DESIGN CATALOG/LITERATURE REVIEW

NEW SHORT FORM CATALOG

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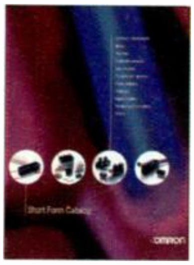

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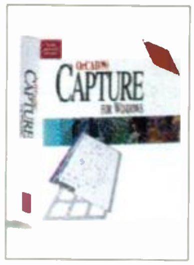

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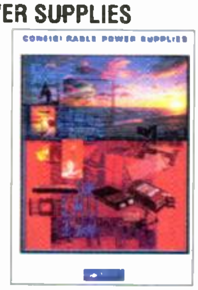

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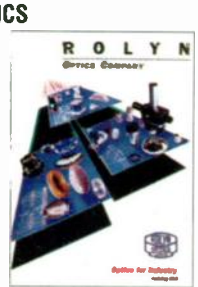

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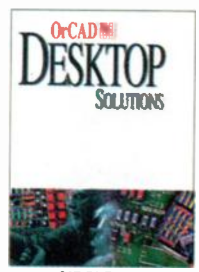

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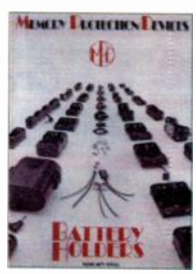

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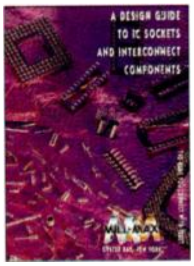

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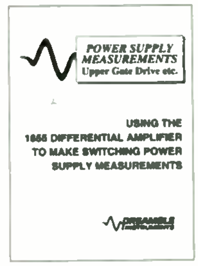

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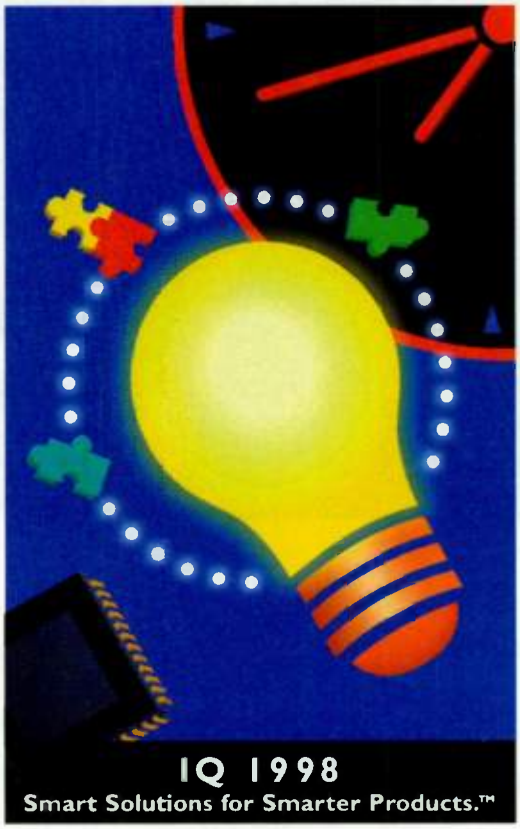

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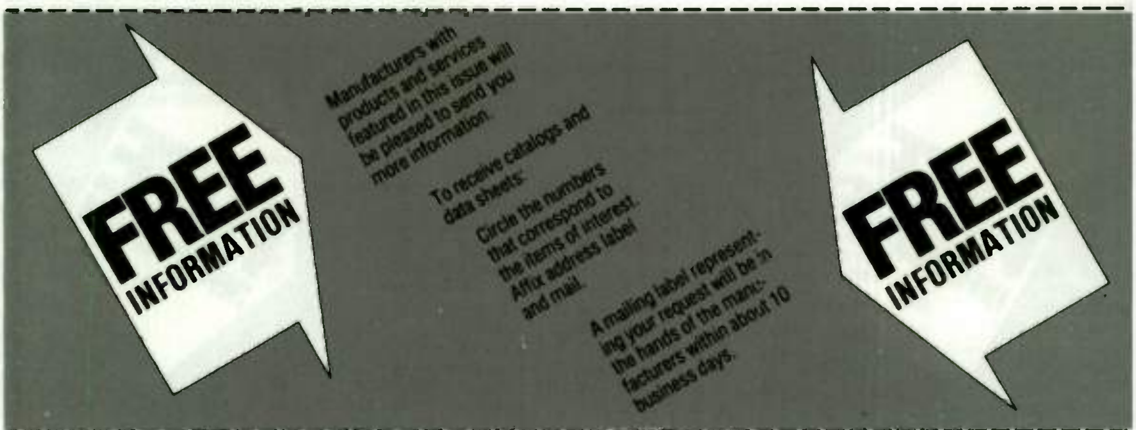

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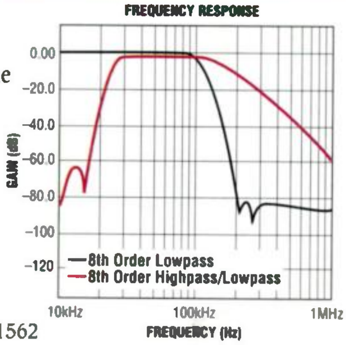

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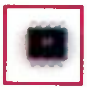

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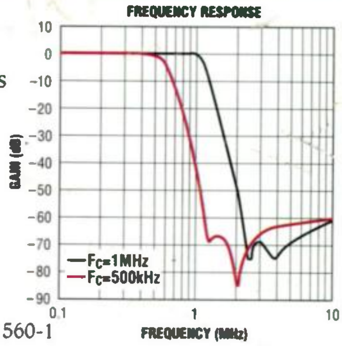

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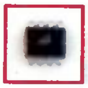

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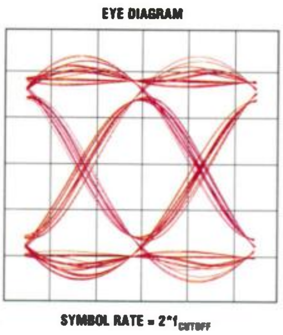

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