

ELECTRONIC DESIGN

TECHNOLOGY • APPLICATIONS • PRODUCTS • SOLUTIONS

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APRIL 6, 1998



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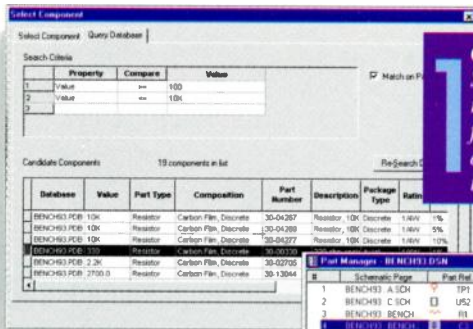
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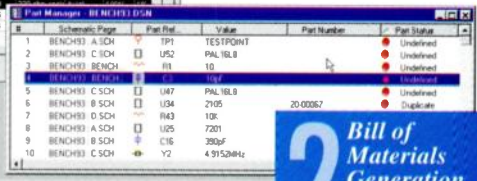
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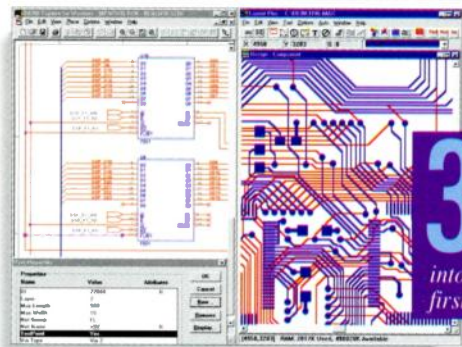
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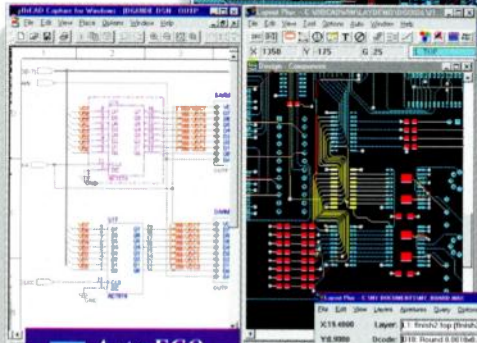
2 **Bill of Materials Generation**
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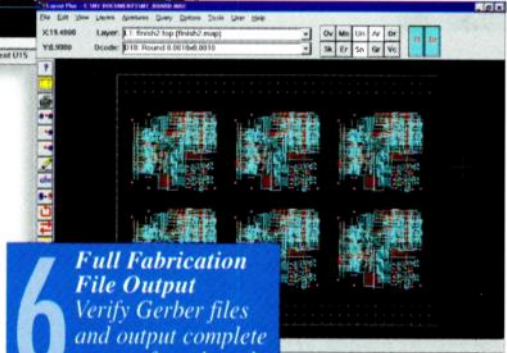
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4 **Shape-Based Autorouting**
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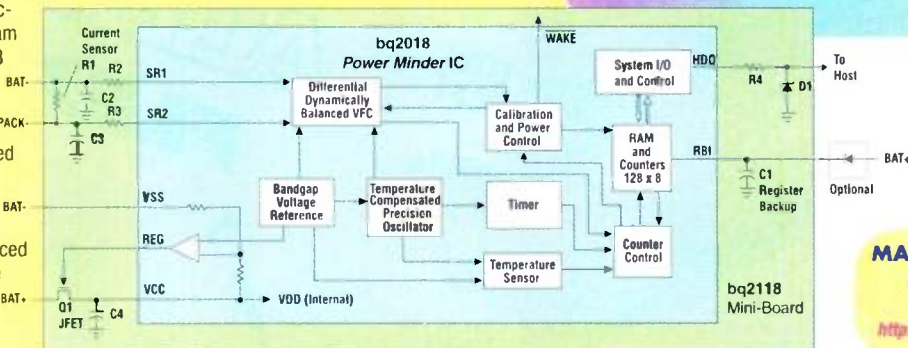
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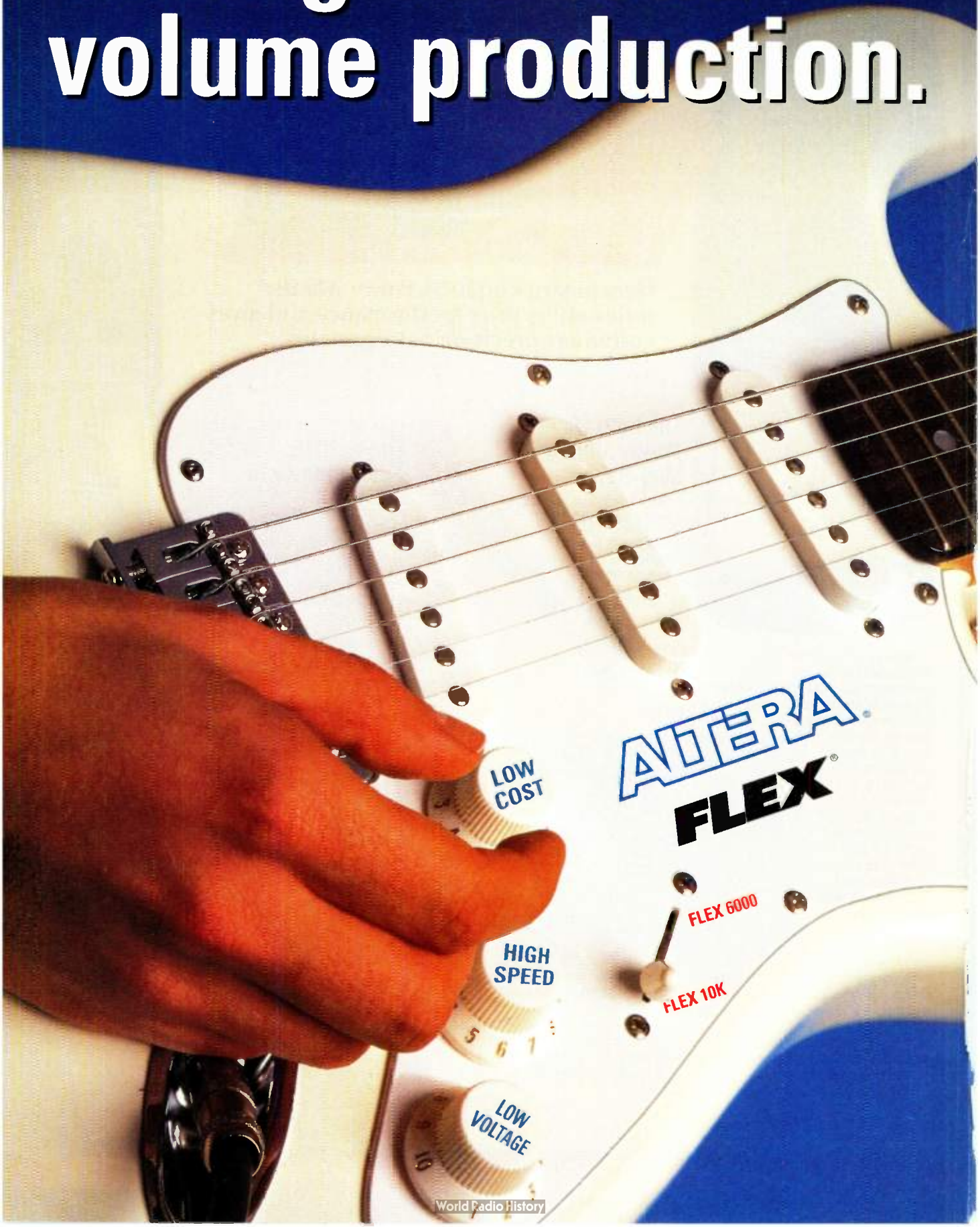


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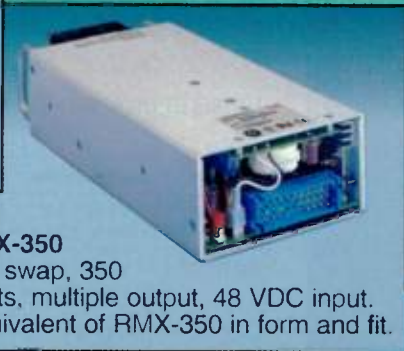
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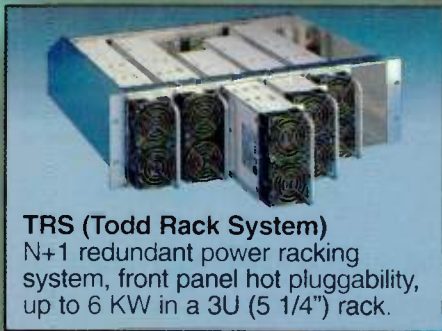
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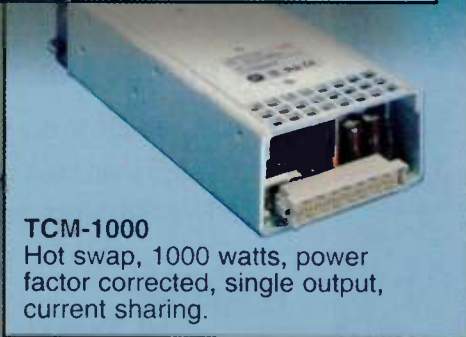
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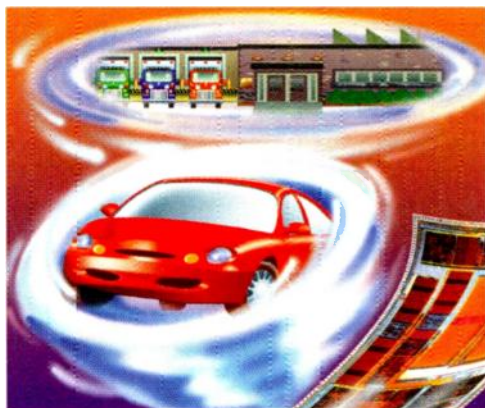


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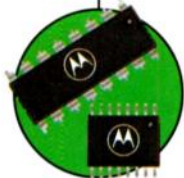
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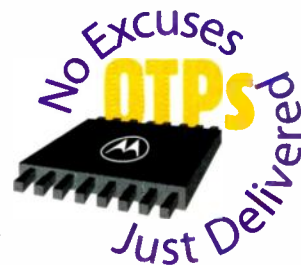
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68HC705C9A	16K	352	31	40-DIP, 44-PLCC, 44-QFP
68HC705J1A	1.2K	64	14	20-DIP, 20-SOIC
68HC705L16	16K	512	39	80-QFP
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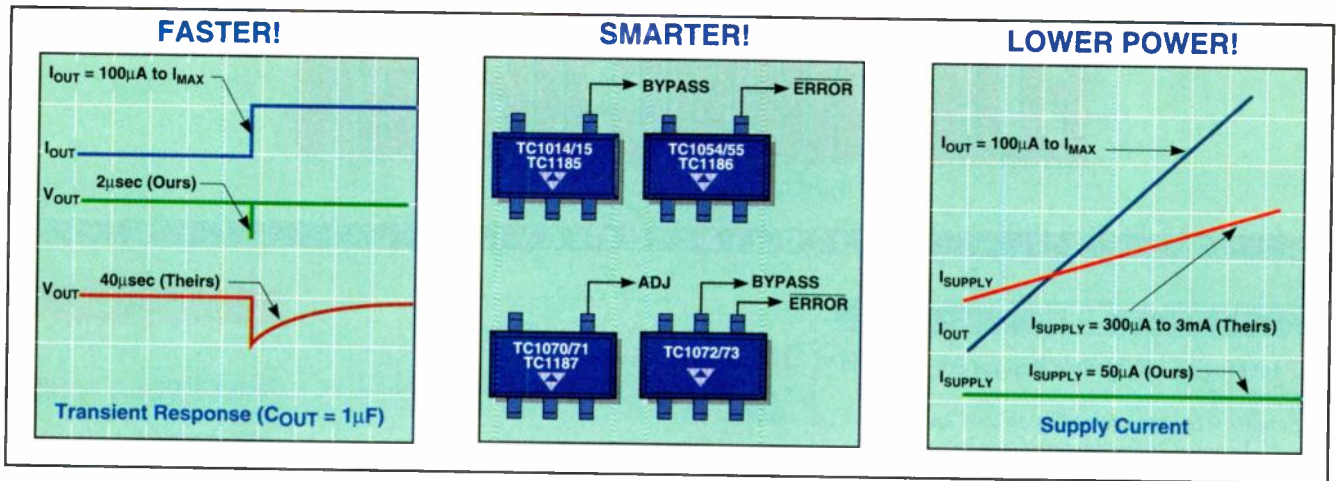
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TC1014	√	√	—	—	SOT-23A-5	2.5, 2.7, 2.85, 3.0, 3.3, 3.6, 4.0, 5.0	50	6.5	50	—	85	±0.5
TC1015	√	√	—	—	SOT-23A-5	2.5, 2.7, 2.85, 3.0, 3.3, 3.6, 4.0, 5.0	100	6.5	50	0.05	180	±0.5
TC1054	√	—	√	—	SOT-23A-5	2.5, 2.7, 2.85, 3.0, 3.3, 3.6, 4.0, 5.0	50	6.5	50	0.05	85	±0.5
TC1055	√	—	√	—	SOT-23A-5	2.5, 2.7, 2.85, 3.0, 3.3, 3.6, 4.0, 5.0	100	6.5	50	0.05	180	±0.5
TC1070	√	—	—	√	SOT-23A-5	2.2 → V _{IN}	50	6.5	50	0.05	85	—
TC1071	√	—	—	√	SOT-23A-5	2.2 → V _{IN}	100	6.5	50	0.05	180	—
TC1072	√	√	√	—	SOT-23A-6	2.5, 2.7, 2.85, 3.0, 3.3, 3.6, 4.0, 5.0	50	6.5	50	0.05	85	±0.5
TC1073	√	√	√	—	SOT-23A-6	2.5, 2.7, 2.85, 3.0, 3.3, 3.6, 4.0, 5.0	100	6.5	50	0.05	180	±0.5
TC1185	√	√	—	—	SOT-23A-5	2.5, 2.7, 3.0, 3.3, 5.0	150	6.5	50	0.05	270	±0.5
TC1186	√	—	√	—	SOT-23A-5	2.5, 2.7, 3.0, 3.3, 5.0	150	6.5	50	0.05	270	±0.5
TC1187	√	—	—	√	SOT-23A-5	2.2 → V _{IN}	150	6.5	50	0.05	270	—

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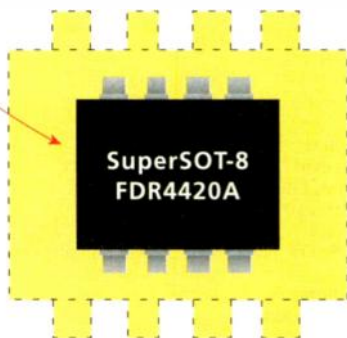
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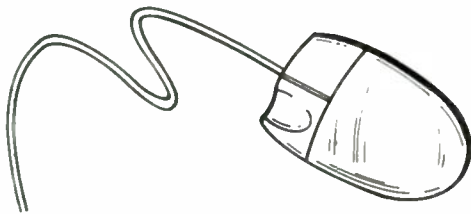
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Southeastcon '98, Apr. 24-26. Hyatt Regency, Orlando International Airport, Orlando, FL. Contact Parveen Ward, ECE Dept., University of Central Florida, Orlando, FL 32816; (407) 823-2610; fax (407) 823-5835; e-mail: pfw@ece.engr.ucf.edu.

16th IEEE VLSI Test Symposium, April 26-30. Hyatt Regency Monterey, Monterey, California. Contact Rob Roy, Intel Corporation MS:JFT-102, 5300 Elam Young Parkway, Hillsboro, Oregon 97124-6497; (503) 264-3738; fax (503) 264-9359; e-mail: robroy@ichips.intel.com.

IPC Printed Circuits Expo '98, Apr. 26-30. Long Beach Convention Center, Long Beach, CA. Contact Dan Green, The Institute for Interconnection & Packaging Electronic Circuits, 2215 Sanders Rd., Northbrook, IL 60062-6135; (847) 509-9700 ext. 371; fax (847) 509-9798.

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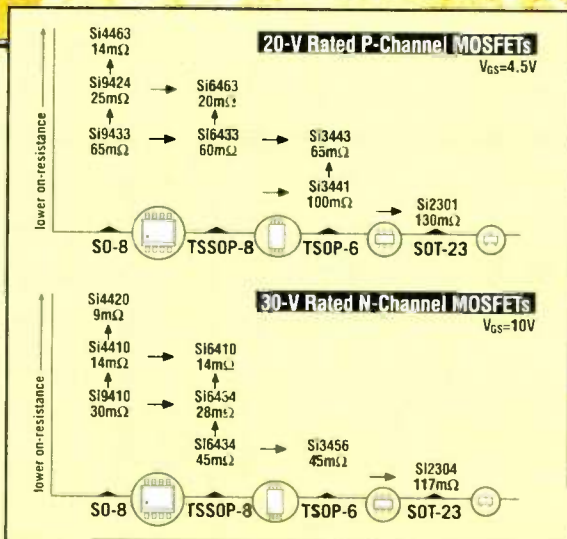
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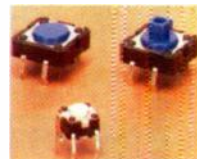
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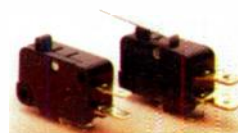
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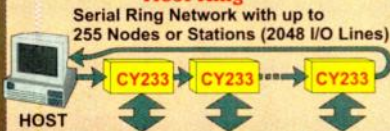
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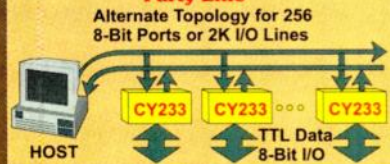
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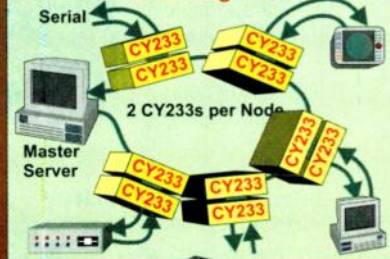
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See You At The Webcast

A few weeks ago, *Electronic Design's* EDA Editor Cheryl Ajluni moderated a "cybercast" on system verification that was co-sponsored by Hewlett-Packard Co. and Cadence Design Systems Inc. A cybercast, also known as a webcast, is basically a live seminar or panel discussion conducted on the World Wide Web, complete with an audience that registers, calls in, and participates. The term "webcasting" is used to describe the ability to use the web to deliver live or delayed versions of sound or video broadcasts.

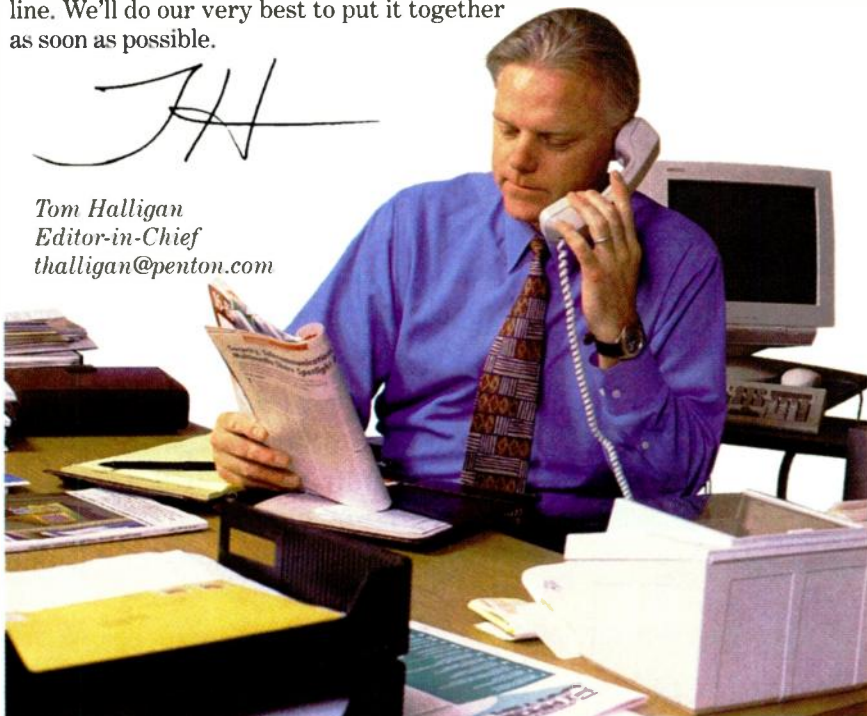
Considering that most companies really can't afford to send their staffs to every conference or seminar, a webcast offers an alternate means to obtain valuable information and also trade questions and comments with experts and speakers. Some 80 senior engineers and engineering managers participated in the audio webcast, and another 100 participants, who didn't have audio capabilities in their computers, linked into the webcast discussion via telephone. Presentations were given, corresponding slides popped up on participants' computer screen, and later on, questions were posed and answered.

Like me, I'm sure many of you folks out there have wasted countless days over the years attending half-day seminars on state-of-the-art widget development at some dank main airport hotel ballroom. Oh sure, you do get to have the complimentary coffee and danish. However, when you figure in all of the travel time, arrangements, and so on, you end up losing almost a full day's work to attend what amounts to nothing more than a 2.5-hour seminar. Participating in a webcast from the comfort of your office or home is incredibly easy, and I expect the webcast seminar/conference idea to quickly become a common component of our industry's workweek.

Following the webcast, feedback was immediate and thought-provoking. And after perusing the comments, the majority of the participants said that the webcast was a hit and they would like to see more. Many of those who participated, in fact, were intrigued with the technology used to conduct a webcast, seeing the potential in their own companies for training and exchanging information among peers.

We here at *Electronic Design* will be participating in and sponsoring more webcasts in the months ahead. If there are any particular topics or technologies that any of you would like to see addressed via a webcast, feel free to drop me a line. We'll do our very best to put it together as soon as possible.

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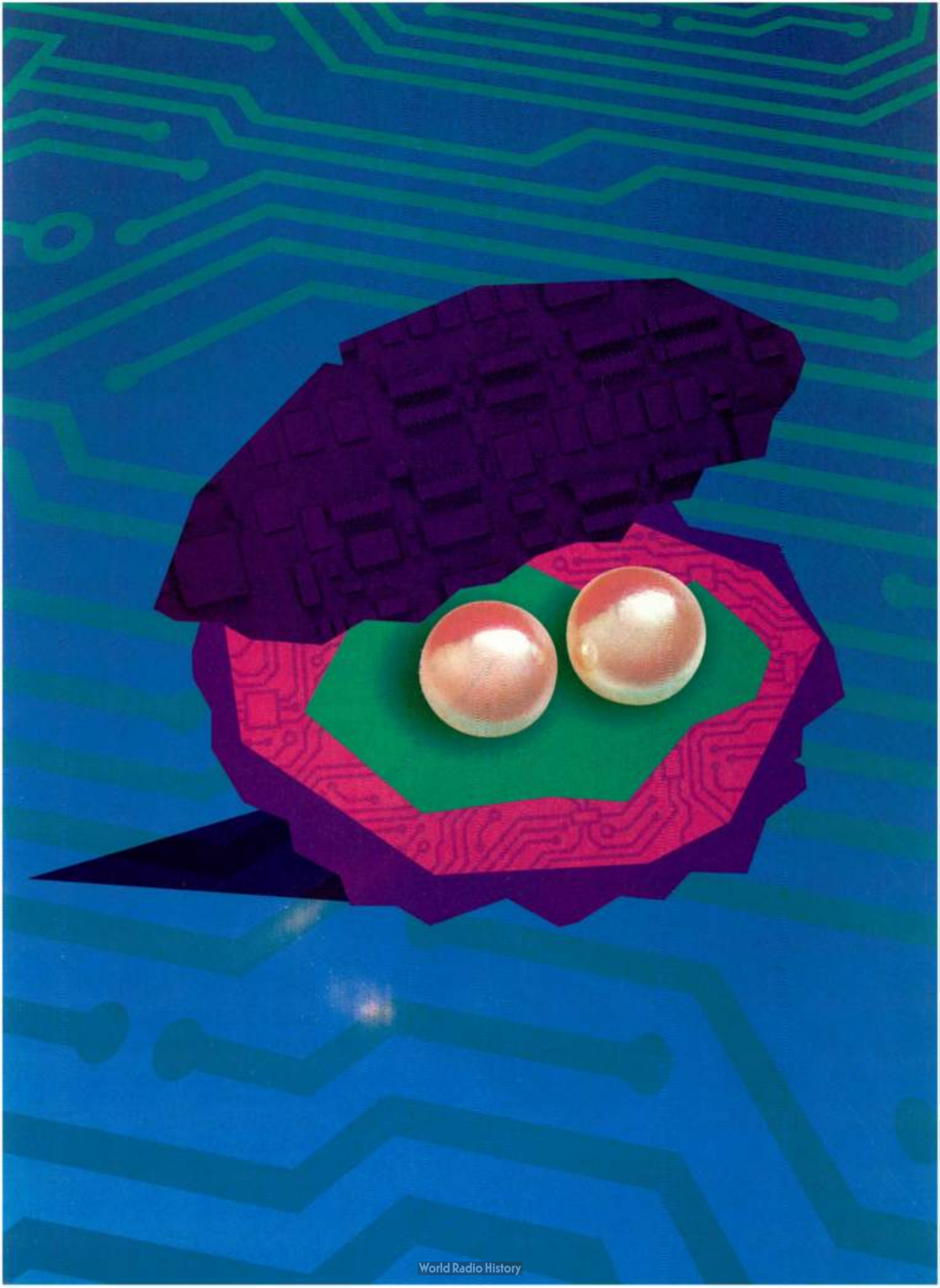


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Silicon Extends To RF Power Amps

Many users have been apprehensive of power silicon's capabilities at low voltages, and frequencies beyond 1 GHz. But, two recent developments in power amplification indicate that silicon is continuing its onward march, both in frequency and power. Its demise has been exaggerated. It is now ready to challenge gallium-arsenide (GaAs) devices in the low-voltage power sector, especially in the 1-GHz region. Designers at Hitachi and Texas Instruments have demonstrated that silicon-based power modules can provide "wattage" and efficiency at supply voltages below 5 V, to effectively compete with GaAs solutions in the wireless world at 900 MHz and above.

While silicon-based power devices continue to perform when operated at higher voltages, their luster begins to fade at RF, when the supply voltage is in the 3-V range. Consequently, some cellular telephone and other RF communications product designers have been doubling the voltage inside their systems to run silicon-based power amplifiers at higher voltages for desired efficiency and power. And, this doubling means more on-board components, which in turn, calls for more space and higher cost. But, that scenario has changed lately with the development of a 4-W RF power amplifier module, operating at a 3.6-V supply by Hitachi; and a 3-W RF MOS power amplifier running at 4.8 V by Texas Instruments.

The Hitachi module was introduced at the recent IEEE International Solid State Circuits Conference (ISSCC '98) in San Francisco, CA, while TI unveiled its accomplishment at the Wireless Symposium a week later in Santa Clara, CA. These achievements signal a new trend toward MOS-based power-amplifier solutions for digital cellular telephones and other wireless communications products that use lithium-ion or other high-density rechargeable technologies to power their portable products.

As a matter of fact, to push silicon into the RF power sector, Hitachi engineers have developed a 0.4- μm -gate MOSFET technology that is capable of handling 3 A of current at 900 MHz efficiently, with low on-state resistance. They've combined it with a new RF impedance-matching technique to obtain a module that is small enough to fit in a leadless 0.2-cm³ IC package. Hitachi claims an efficiency of 47% for its 4-W output power module for GSM handset telephones. The new RF impedance matching circuit, called divided-device and collectively impedance-matched amplifier (DD-CIMA), reduces line loss to enable the module to achieve 47% efficiency in the 880-915 MHz range. The technology has also allowed Hitachi to keep the size small, as well as prevent oscillations for better stability. Hitachi designers indicate that this technology can be extended to 1 GHz and above to meet the power amplification needs of global wireless communications.

Likewise, TI has developed a silicon-based, lateral power, RF MOSFET technology called RFMOS. Using RFMOS, the company's designers have built a three-stage power amplifier that provides 3 W under pulsed conditions at 900 MHz and a 4.8-V supply, with a power-added efficiency of 45%. With adequate heat sinking, the device is capable of sustained continuous-wave operation. Aimed at battery-powered digital cellular telephones and personal communications systems, TI says that its RFMOS-based module offers an alternative power-amplifier solution that is comparable in performance to GaAs, but with a lower system-level cost and smaller board size.

Meanwhile, proponents of GaAs-based power amplifiers continue to advance the technology and produce RF amplifiers that offer better efficiency at lower cost. It will be interesting to watch the two solutions, as they begin to look for sockets in the next generation of cellular telephones and other battery-operated wireless systems.

Send your comments and thoughts on this subject to me at abindra@penton.com.



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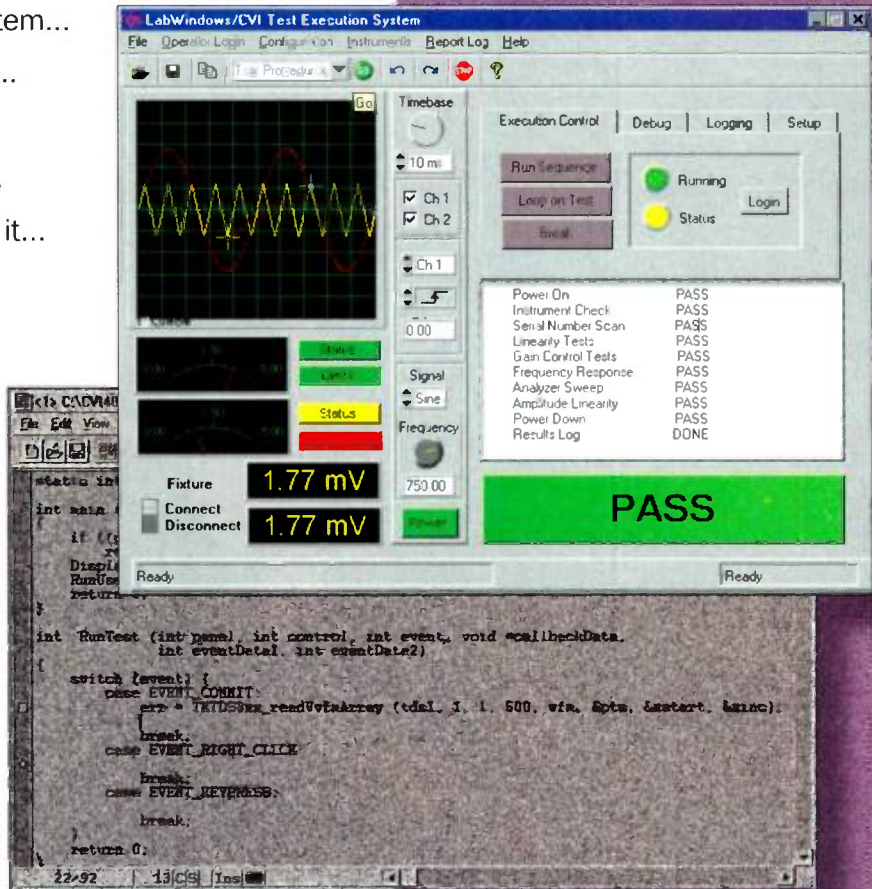
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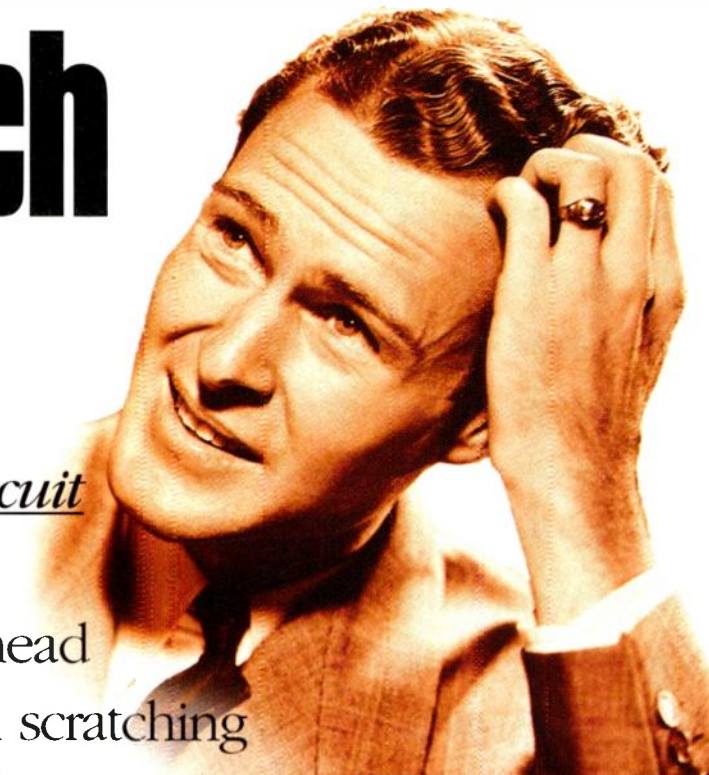
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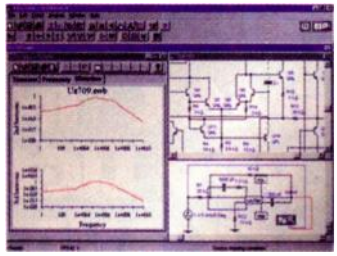
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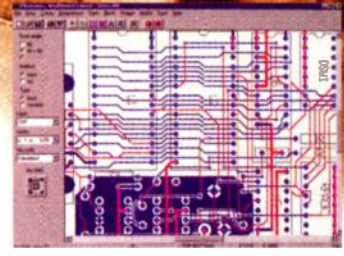
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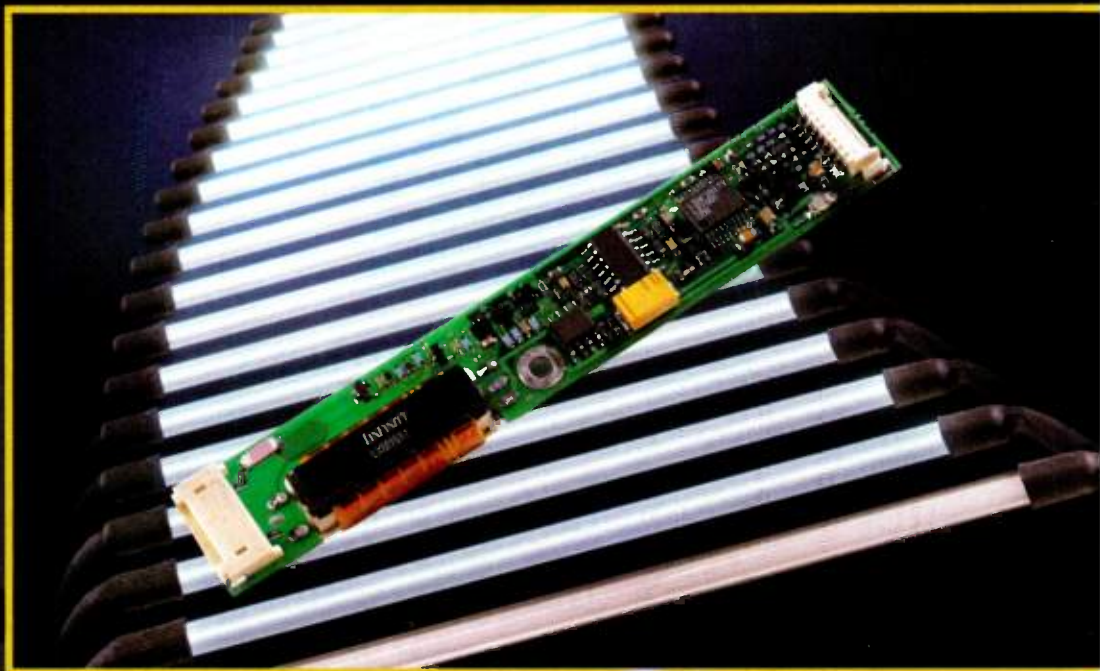
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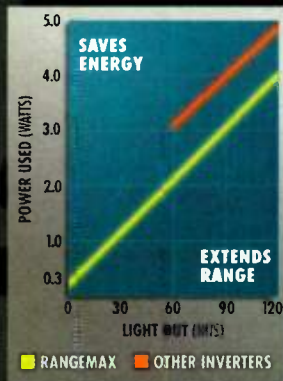


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READER SERVICE 113
World Radio History

Advanced Technologies To Combat Campus Violence

Prompted by the recent upswing in violent crimes committed on school campuses, congress has moved to draft legislation that names Sandia National Laboratories to head a national center of expertise for school security technologies known as the "School Security Technology Center." The center will be located in Albuquerque, and initially be operated by Sandia. Over time, responsibility for running the center will be transferred to a non-profit organization staffed by experienced school administrators and school security professionals; although it will continue to draw on Sandia's technological expertise.

Sandia was chosen to head the center because of its success in designing a New Mexico school security system two years ago. The system called for a closed campus and minor physical enhancements to the school grounds, along with video surveillance and sensor systems. Less than a year after these changes were implemented, the school witnessed a dramatic 90% decrease in vandalism and theft, 75% fewer fights on campus, and 95% fewer false fire alarms, among other improvements.

The School Security Technology Center will use this isolated success and, working hand in hand with the nation's schools, conduct vulnerability assessments, as well as provide advice on technologies and approaches to address various crime-related problems. To make school grounds safer for students by improving security, the center will leverage much of today's advanced technology, and draw on decades of Sandia's experience designing security systems to protect materials vital to U.S. national security. Of particular interest will be how to implement these security technologies in a cost-effective manner.

As part of its charter, the School Security Technology Center will advise schools on the limitations, maintenance requirements, costs, and public perceptions of technology, as well as civil rights and privacy issues that some technologies present. To push this effort along, Sandia is working on a set of "how-to" manuals to help administrators self-assess and solve some of the most common school security problems. In particular, the manuals will cover the topics of: violence, vandalism, and theft of school property; and drug and alcohol use on campuses. Funding for the manuals comes from The National Institute of Justice.

Overall funding for the center is mandated by the Safe Schools Security Act of 1998. It will provide Sandia with \$1.4 million per year for three years to help schools choose security technologies and measures that deter crime and protect school assets. An additional \$10 million per year will be made available to help selected schools purchase appropriate security technologies.

For more information on the School Security Technology Center, contact Sandia National Laboratories at (505) 844-8066; www.sandia.gov. CA

Initiative Focuses On Use Of CDMA Technologies

It's expected that future satellite communications, wireless local loop, and cordless and cellular phones will all rely substantially, if not exclusively, on wide-band CDMA (Code-Division Multiple Access) technologies. Recognizing this trend, Cadence Design Systems, San Jose, Calif., recently announced an initiative focused on the design of third-generation personal-communications systems. In support of this initiative, the company has now become a member of the Universal Mobile Telecommunications Systems (UMTS) Forum, a consortium chartered by the European electronics industry to develop new technologies and standards.

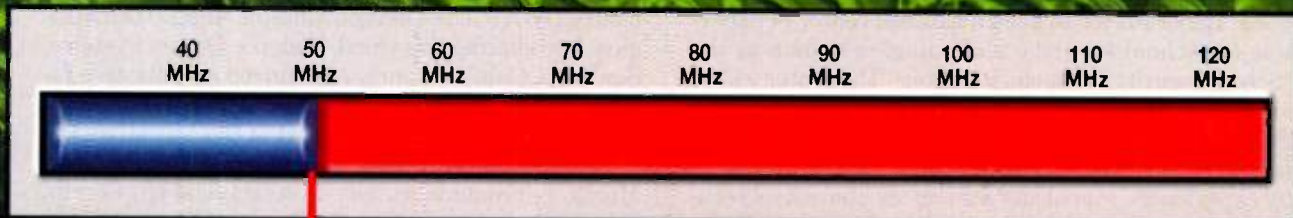
As part of the consortium, Cadence will provide a basis for independent assessment of UMTS proposals, incorporating and driving the adoption of accepted standards. Cadence also will help accelerate deployment of the UMTS service by offering member companies access to its communication-systems design software and design experience. In addition, the company will begin expansion of its ALTA technology portfolio to include an EnWave CDMA toolkit and an enhanced version of the Visual Architect behavioral synthesis product. For further information on the CDMA initiative, check out its web site at www.cadence.com. CA

Novel Hardware/Software Fusion Cuts The Cost Of ADSL

ADSL modems may soon be affordable by any computer owner, thanks to a new modem architecture that uses a combination of DSP hardware and host processing resources. Developed by Integrated Telecom Express, Santa Clara, Calif., the technology known as SAM (Scalable ADSL Modem) employs a low-cost DSP-based ASIC for some of the most compute-intensive tasks involved in converting a bit stream into a constellation of up to 128 QAM carrier tones. The remaining tasks still consume about 35% of a 200-MHz Pentium-class processor's MIPS to perform the complex transforms, channel control, and handshaking functions required to support an ADSL connection.

While it's not fully compliant with the ANSI T1.413 standard for ADSL modems, it's fully interoperable with any ANSI-compatible modem. To minimize the cost of the modem and keep the load on the host CPU to an acceptable level, the current SAM architecture doesn't implement the full set of 255 carrier tones, which can carry up to 2.5 Mbits/s. SAM assures interoperability by using the ANSI line probing and startup sequence to signal the ADSL modem on the other side of the line, telling it which carrier tones and data rates it can use. As developments make more processor power or DSP speed available, SAM's algorithms can be easily ad-

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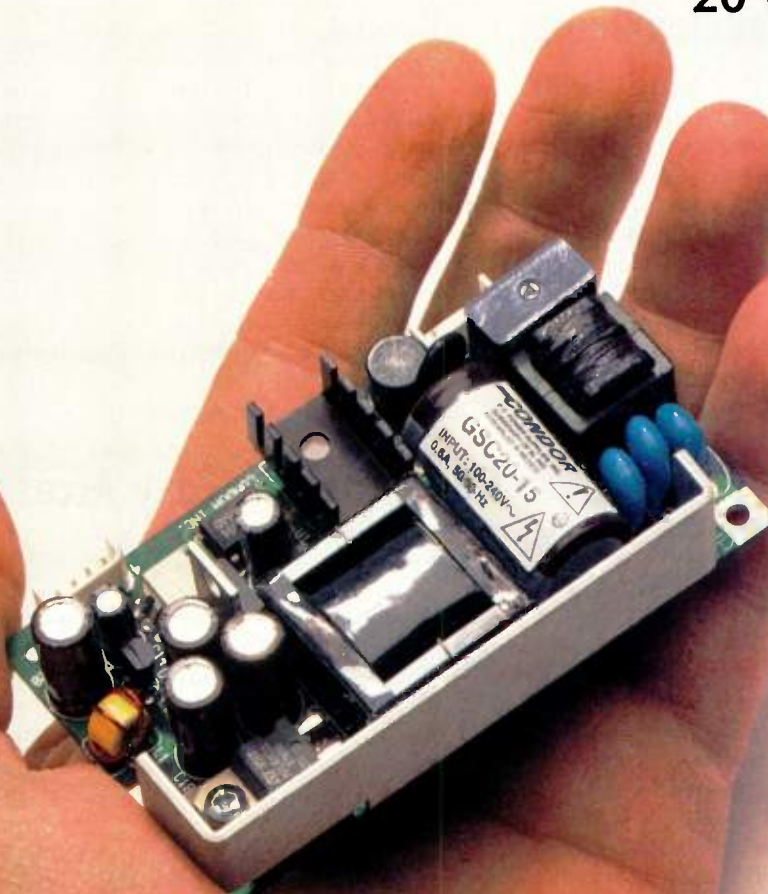


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justed to enable it to support higher data rates.

Information on licensing the software algorithms and ASIC design may be obtained by contacting Jow Peng, director of marketing at Integrated Telecom Express Inc., 2710 Walsh Ave., Santa Clara, CA 95051; 9408) 980-8168, ext.209; www.itexinc.com. LG

Joint Effort Targets Infrared Sensor Simulation Development

In an attempt to develop integrated infrared (IR) sensor simulation for use in real-time three-dimensional simulation environments, Coryphaeus Software Inc., Los Gatos, Calif., and Technology Service Corp. (TSC), Los Angeles, Calif., have entered into a joint development agreement. Terms of the agreement state that Coryphaeus' EasyScene and EasyTerrain development kits will be integrated with TSC's IRGen infrared database modeler.

This merger will allow developers to incorporate accurate representations of IP sensor output within real-time simulations, and for the first time enable them to realistically simulate IR displays within an application. This is particularly crucial for military applications, such as tank thermal viewers, which have stringent mission-critical requirements for the accurate display of IR band information. Integrating the Coryphaeus and TSC tools not only will make this advanced IR simulation capability possible, but provide users with an IR sensor display that's correlated with the visual out-the-window type scene simulated by the Coryphaeus products.

Because the integration is expected to provide an optimal solution for infrared real-time 3D simulation, it also will find use in civilian applications such as law-enforcement surveillance training. For more information on the ongoing integration, contact Coryphaeus at (408) 395-4537, or check out its web site at www.coryphaeus.com. TSC's web site can be accessed at www.tsc.com. CA

World's Fastest Supercomputer Under Construction

The safety and reliability of the United States' nuclear stockpile has become of paramount concern in the absence of nuclear testing. Hence, the Department of Energy has formed the Accelerated Strategic Computing Initiative (ASCI) program to build systems capable of terascale, trillion-calculations-per-second computing.

Such systems will be used to conduct the complex modeling and simulation needed to verify nuclear weapons without underground tests, and offers an eight-fold increase in simulation detail compared to what's available today. As part of this on-going program,

IBM, Somers, N.Y., has been awarded an \$85 million contract with the Department of Energy and Lawrence Livermore National Laboratory, Livermore, Calif., to build the world's fastest supercomputer.

IBM's supercomputer will be based on the RS/6000 SP technology. By the year 2000—when it's expected to be installed at the Livermore Laboratory, it will be able to handle 10 trillion calculations per second. When complete, the computer will be capable of calculating in a single second what would take 10 million years using a hand held calculator.

The results of IBM's work on the ASCI development will be used in future RS/6000 products for commercial and technical customers. For instance, automotive, aerospace, medical, and oil companies may use advances in high-speed computer simulation to replace traditional engineering and science methods of experimentation and prototyping.

IBM also is working on high-speed switching technology for supercomputers capable of 30 to 100 trillion calculations per second as part of the Department of Energy's PathForward initiative to build the infrastructure necessary for a 100-teraFLOPS computer. The system is expected to be ready for delivery in 1999. CA

CRADA Offers Easy Access To Sandia Technology

A cooperative research and development agreement (CRADA) has been signed between Sandia National Laboratories, Albuquerque, N.M., and SEMI/SEMATECH, an Austin, Texas-based consortium of U.S. suppliers to the global semiconductor industry. The goal is to make Sandia technology easily accessible to the 186 SEMI/SEMATECH member companies.

The CRADA hopes to establish an umbrella agreement that will allow work to begin on a project within one week of Sandia and the SEMI/SEMATECH member company negotiating cost, performance, and schedule. What results is a significant time savings and decrease in legal expenses. Under the terms of the agreement, SEMI/SEMATECH members will fund the work of Sandia technologists. In some projects, equipment and technology necessary for Sandia's radiation-hardened microelectronics and micromachining capability may be contributed to Sandia through the CRADA.

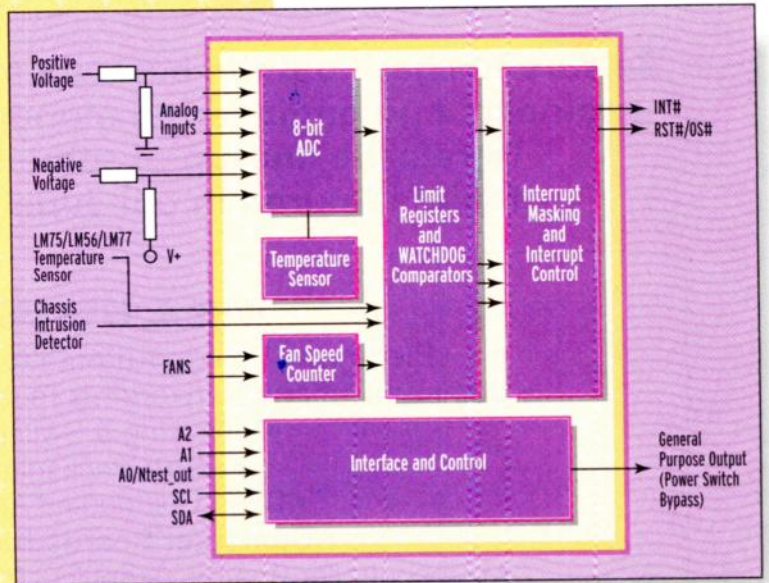
The agreement is expected to stoke the competitive fires of the U.S. semiconductor supplier industry, as well as support and nurture Sandia's technology base. Furthermore, it will simplify and expedite access to Sandia technology by SEMI/SEMATECH members.

For further details, contact Sandia National Laboratories Media Relations department at (505) 844-8066, or go to its web site at www.sandia.gov. CA

Edited by Roger Engelke

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JUNE 8, 1998 ISSUE

- **Electronic Design Automation:** DAC Preview
- **Communications/Networking Technology:** ATM/Gigabit Networking & Switching
 - **PIPS:** Packaging
 - **DSP:** Contributed Article .
- **Computer Boards & Buses:** Microcontroller Boards, Graphics, PCMCIA, Peripherals

JUNE 22, 1998 ISSUE

- **Analog Design:** Data-Aquisition Modules
- **Test & Measurements:** Update: Digital Storage Oscilloscopes
 - **Embedded Systems**
- **Digital Design:** Advanced Static Memories

JULY 6, 1998 ISSUE

- **Electronic Design Automation**
 - **PIPS:** Power Management
- **Analog Design:** Power Control
 - **Digital Design**

JULY 20, 1998 ISSUE

- **Communications/Networking Technology:** Advanced Paging/Messaging
 - **Computers Boards & Buses**
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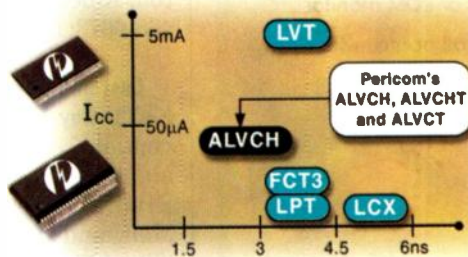
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MAY

IEEE International Conference on Neural Networks (ICNN '98), May 3-9. Anchorage, AK. Contact Patrick K. Simpson, Scientific Fishery Systems Inc., P.O. Box 242065, Anchorage, AK 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@alaska.net.

IEEE World Congress on Computational Intelligence, May 3-9. William A. Egan Civic and Convention Center; Anchorage, AK. Contact Patrick K. Simpson, Scientific Fishery Systems Inc. P.O. Box 242064, Anchorage, AK 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@alaska.net.

Seventh IEEE International Fuzzy Systems Conference, May 3-9. Anchorage, AK. Contact Patrick K. Simpson, Scientific Fishery Systems Inc., P.O. Box 242065, Anchorage, AK 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@alaska.net.

IEEE International Symposium on Electronics & the Environment, May 4-6. Oak Brook, IL. Contact ISEE Conference Registrar, 445 Hoes Lane, Piscataway, NJ 08855-1331; (732) 562-3875; fax (732) 981-1203; e-mail: j.slaven@ieee.org.

IEEE/IAS Industrial & Commercial Power Systems Technical Conference (I&CPS), May 4-7. Edmonton, Alberta, Canada. Contact Marty Bince, Modicon Canada Ltd., 5803 86th St., Edmonton, Alberta T6E 2X4, Canada; (403) 468-6673; fax (403) 468-2925.

Custom Integrated Circuits Conference (CICC), May 11-14. Westin Hotel Convention Center, Santa Clara, California. Contact CICC, 101 Lakeforest Blvd., Suite 270, Gaithersburg, Maryland 20877; (301) 527-0902; fax (301) 527-0994.

IEEE Radar Conference, May 12-14. Contact Scott Ramey, 2501 West University, MS 8056, McKinney, TX 75070; (972) 952-4409; fax (972) 952-3071; e-mail: sramey@ti.com.

IEEE International Conference on Acoustics, Speech & Signal Processing (ICASSP '98), May 12-15. Seattle Convention Center, Seattle, WA. Contact Les E. Atlas, Dept. EE (FT 10), University of

Washington, Seattle, WA 98195; (206) 685-1315; fax (206) 543-3842; e-mail: atlas@ee.washington.edu.

IEEE International Conference on Robotics and Automation, May 16-21. Katholieke Universiteit, Leuven, Belgium. Contact Georges Giralt, LAAS-CNRS, Toulouse, France, +33 61-33-63-48; fax +33 61-33-64-55; e-mail: giralt@laas.fr.

IEEE Power Electronics, Specialist Conference (PESC '98), May 17-22. Sea Hawk Hotel & Resort, Fukuoka, Japan. Contact Tsutomu Ogata, NTT Integrated Information & Energy Systems Labs., Midocho, Musashino, 180 Japan; +422-59-2350; fax +81 422-59-2347; mail: ogata@ilab.ntt.jp

IEEE Vehicular Technology Conference (VTC), May 18-21. Westin Hotel, Ottawa, Ontario, Canada. Contact Tara Hennessy, Industry Canada, 300 Slater St., Ottawa, Ontario, K1A 0C8, Canada; (613) 990-4711; fax (613) 952-5108; e-mail: hennessytara@ic.gc.ca.

Fourth PC Developers' Expo & Conference, May 18-22. San Jose Convention Center, San Jose, CA. Contact Anna Brooks (800) 690-3858 or (619) 673-0870; fax (619) 673-1591; www.annabooks.com., e-mail: expo@annabooks.com.

48th IEEE Electronic Components & Technology Conference (ECTC '98), May 25-28. Sheraton Hotel & Towers, Seattle, WA. Contact Components Group, EIA, 2500 Wilson Blvd., Arlington, VA 22201; (703) 907-7536; fax (703) 907-7501; mail: judya@eia.org.

IEEE International Symposium on Circuits Systems (ISCAS '98), May 31-June 03. Monterey Conference Center, Monterey, California. Contact Sherif Michael, Department of Electrical & Computer Engineering, Naval Postgraduate School, Monterey, California 93943; (408) 656-2252; fax (408) 656-2760; e-mail: michael@ece.nps.navy.mil.

JUNE

POF World '98 (Plastic Optical Fiber), June 1-4. Providence Convention Center, Providence, Rhode Island. Contact Information Gatekeepers Inc., 214 Harvard Ave., Boston, Massachusetts 02134; (617) 232-3111; fax (617) 734-8562; www.igigroup.com.



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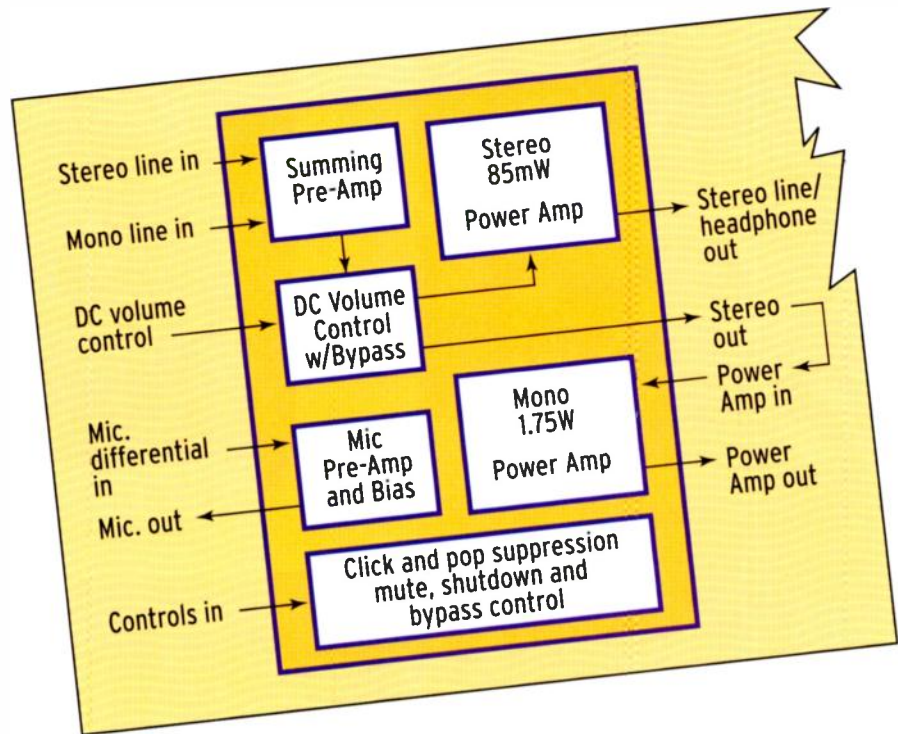
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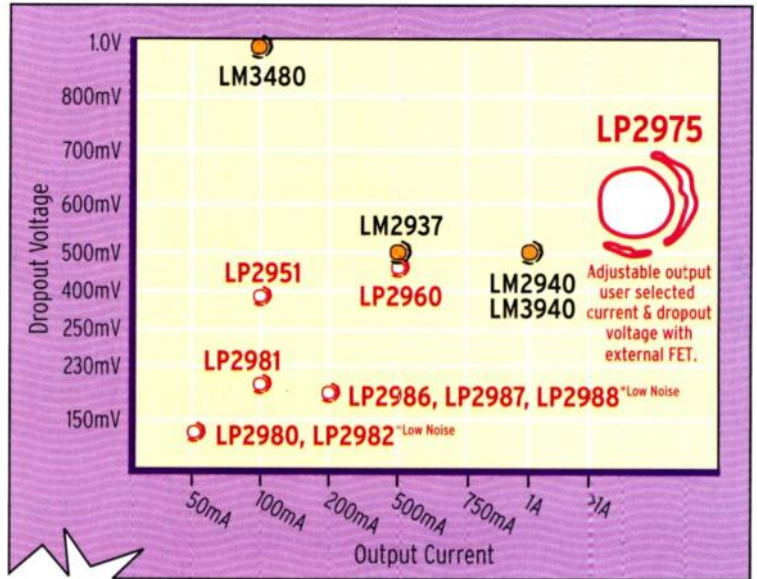
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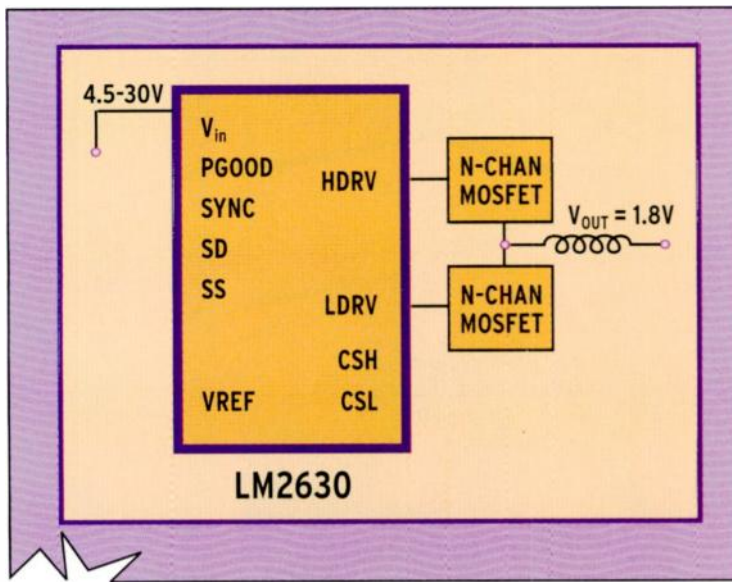
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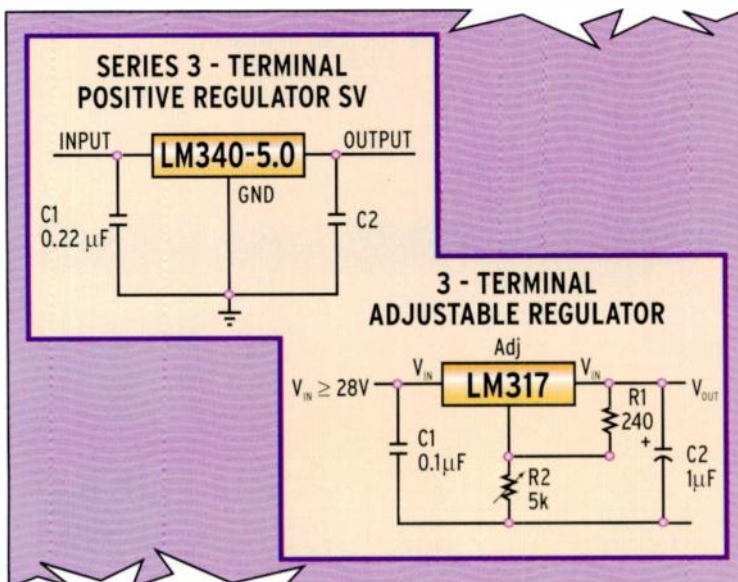


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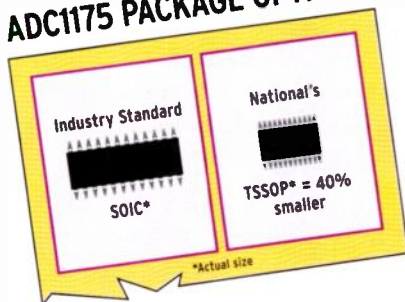
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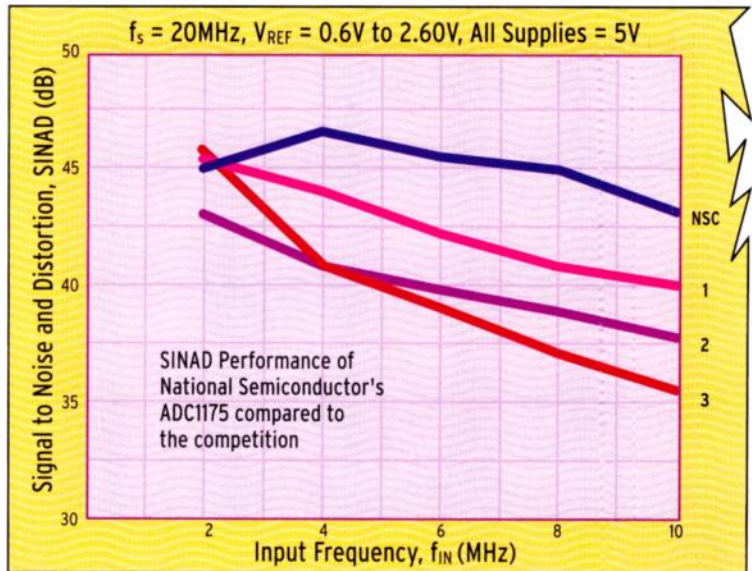
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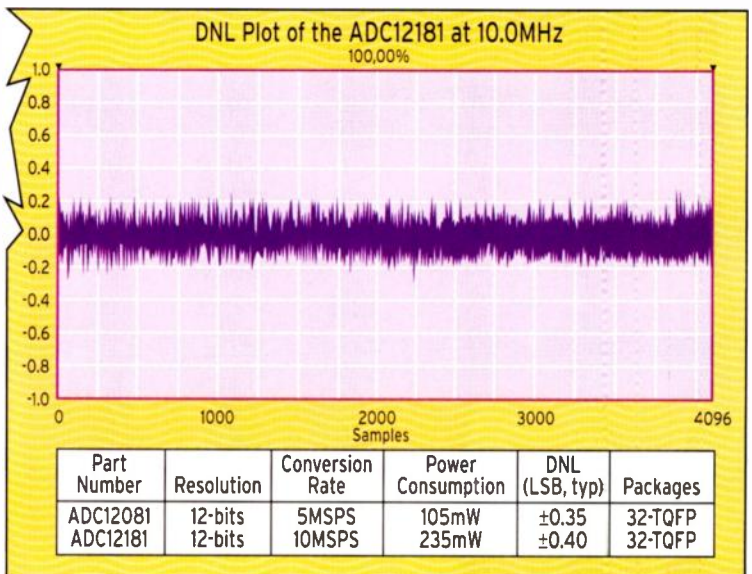
ADC1175 PACKAGE OPTIONS



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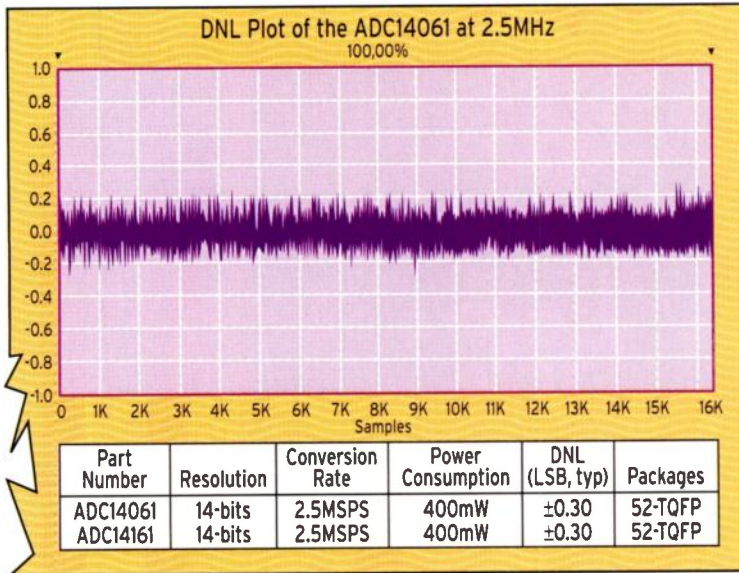


12-bit High-Resolution A/D Converters ADC12081/12181

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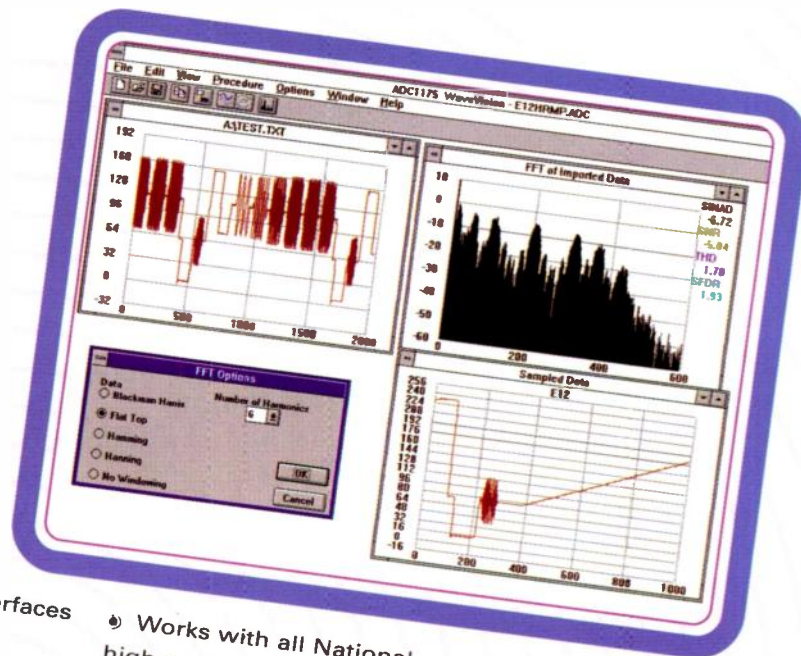
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14-bit High-Resolution A/D Converter ADC14061/14161

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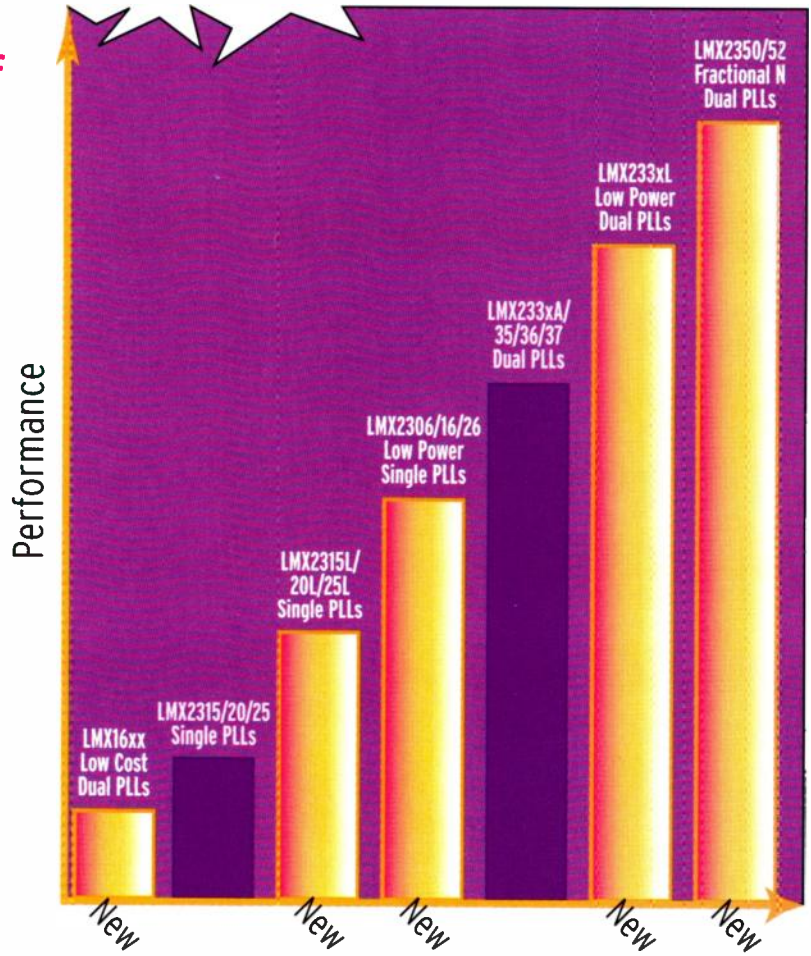
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NEW PLL SELECTION GUIDE

Part Number	RF Input (Main & Aux PLLs)	Active I _{cc} (typ @ 3V)	V _{cc} Range	Package*
Single PLLs				
LMX2306	550MHz	1.7mA	2.3 to 5.5V	TSSOP16
LMX2316	1.2GHz	2.5mA	2.3 to 5.5V	TSSOP16
LMX2326	3.0GHz	4.0mA	2.3 to 5.5V	TSSOP16
LMX2315L	1.2GHz	3.2mA	2.7 to 5.5V	TSSOP20
LMX2320L	2.0GHz	2.4mA	2.7 to 5.5V	TSSOP20
LMX2325L	2.5GHz	4.0mA	2.7 to 5.5V	TSSOP20
Dual PLLs				
LMX2330L	2.5GHz & 510MHz	5.0mA	2.7 to 5.5V	TSSOP20
LMX2331L	2.0GHz & 510MHz	4.0mA	2.7 to 5.5V	TSSOP20
LMX2332L	1.2GHz & 510MHz	3.0mA	2.7 to 5.5V	TSSOP20
LMX2335L	1.1GHz & 1.1GHz	4.0mA	2.7 to 5.5V	TSSOP16/SO16
LMX2336L	2.0GHz & 1.1GHz	5.0mA	2.7 to 5.5V	TSSOP20
LMX1600	2.0GHz & 500MHz	5.0mA	2.7 to 3.6V	TSSOP16
LMX1601	1.1GHz & 500MHz	4.0mA	2.7 to 3.6V	TSSOP16
LMX1602	1.1GHz & 1.1GHz	5.0mA	2.7 to 3.6V	TSSOP16
Dual Fractional N PLLs				
LMX2350	2.5GHz & 550MHz	7.0mA	2.7 to 5.5V	TSSOP24
LMX2352	1.2GHz & 550MHz	5.5mA	2.7 to 5.5V	TSSOP24

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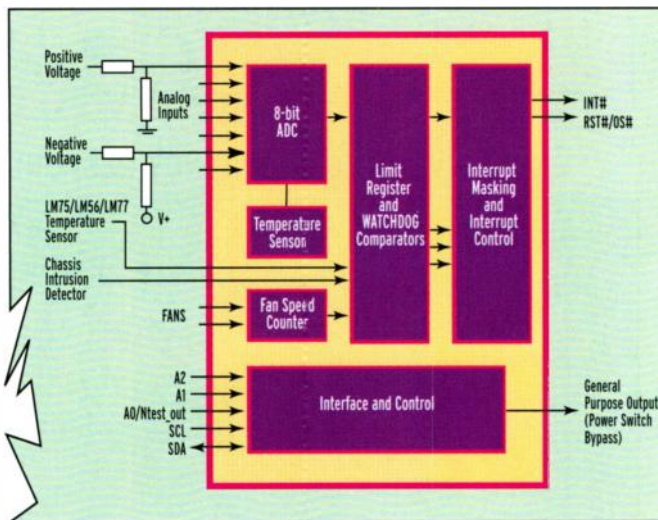
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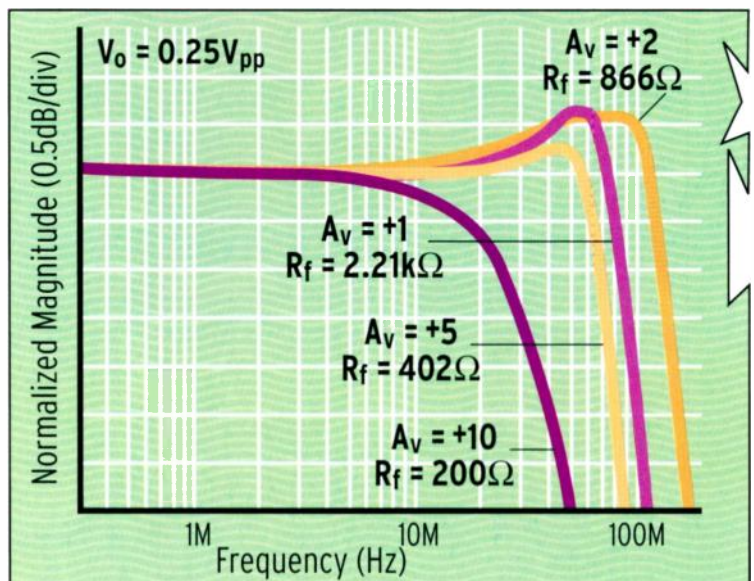
- 450MHz small signal bandwidth
- 2000V/ μ s slew rate
- -71dBc distortion
- 0.03%, 0.03 deg diff gain, phase
- 70mA output current
- 12 ns settling to 0.1%

NEW TINY OP AMPS/COMPARATORS

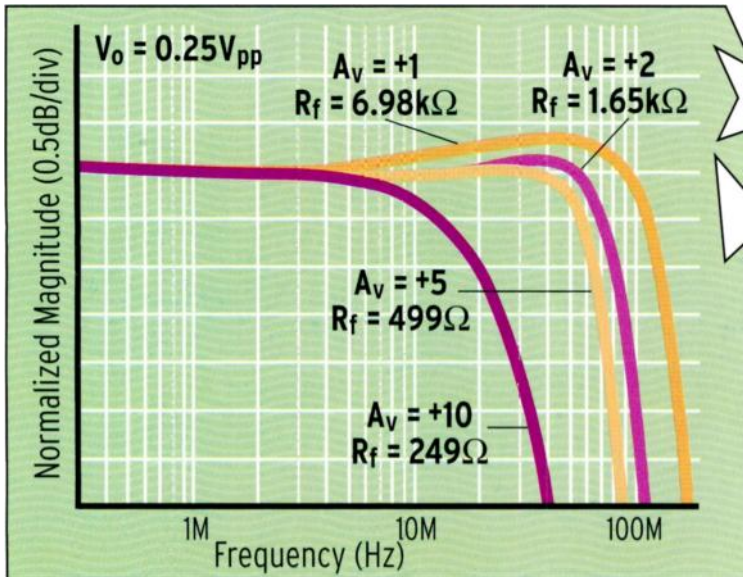
Part #	MHz	Supply Voltage	Package Sizes
LMV321* Single Op Amp	1MHz	2.7 - 5.5V	SOT23-5, SC70-5
LMV358* Dual Op Amp	1MHz	2.7 - 5.5V	SOIC-8, MSOP-8
LMV324* Quad Op Amp	1MHz	2.7 - 5.5V	SOIC-14, TSSOP
LMV331* Single Comparator	1MHz	2.7 - 5.5V	SC70-5, SOT23-5
LMV393* Dual Comparator	1MHz	2.7 - 5.5V	MSOP-8, SOIC-8
LMV339* Quad Comparator	1MHz	2.7 - 5.5V	TSSOP, SOIC-14

Package (Actual Size) *Industrial Temp Range (-40 to 85 C)

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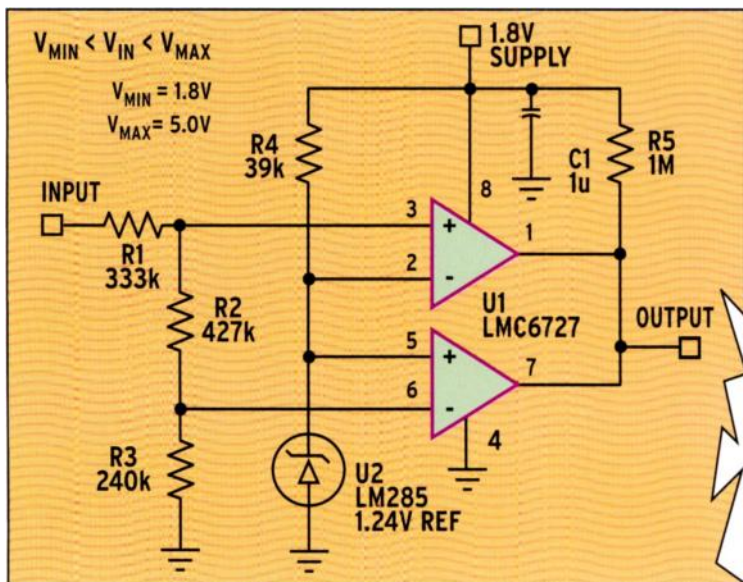
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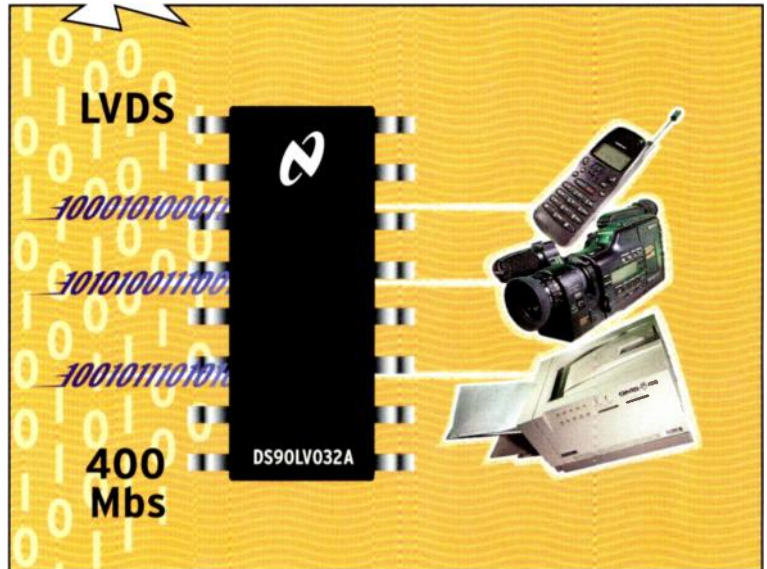
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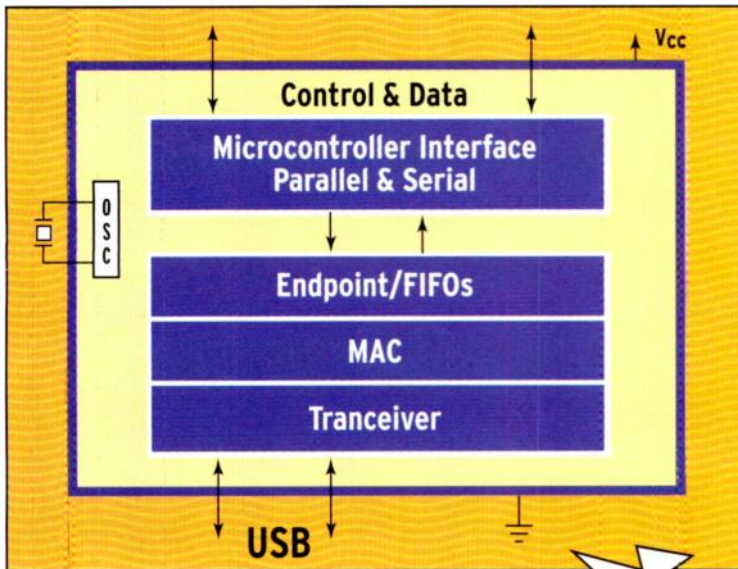


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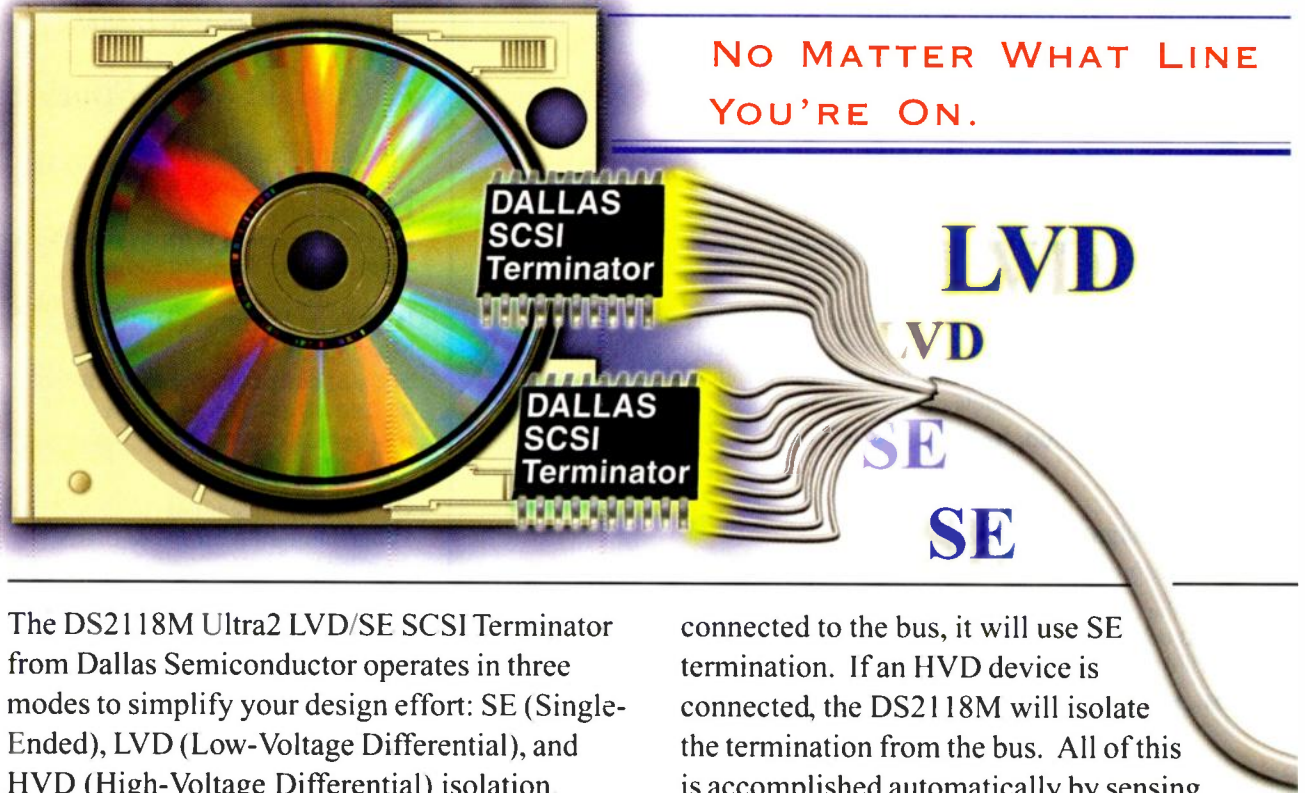
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Flat Polymer Display Promises TV-Quality Pictures Two Years Sooner Than Expected

Wafer-thin TV displays using light-emitting polymer (LEP) material may reach the marketplace two years earlier than previously thought. A pair of companies working on the technology have already built and demonstrated a small number of proof-of-concept models, with 180,000 pixels, configured to show a standard 4:3-aspect ratio, 525-line NTSC TV picture.

The first devices were monochrome displays with a diagonal screen size of 2.5 in., and a display area of 1 by 1.75 in. (see the figure). But 10-in.-diagonal prototypes with full-color capability will be ready before the end of the year, according to Mark Gostick, marketing director at Cambridge Display Technology Ltd. (CDT), Cambridge, England. The company is developing the LEP display with Seiko Epson Ltd., Suwa, Japan.

Originally, Gostick predicted that the first applications would be simple, low-information-content displays, like backlights for mobile phones, or single digits for instrument displays. He also said that those would be available "sometime in 1998" (*ELECTRONIC DESIGN*, January 8, 1996, p. 42). Full dynamic displays for TV and similar applications were "at least five years" in the future, Gostick said back then.

The breakthrough that pushed up that predicted schedule stemmed from CDT's alliance, forged a less than a year ago, with Seiko Epson. The Japanese company brought two technologies to the party: piezo ink jet printing and polysilicon thin-film transistor (TFT) deposition. Working together, the two companies developed the LEP material into what can only be described as light-emitting ink. It is the key to the whole manufacturing process, with display pixels literally being ink-jet printed onto a TFT matrix.

As a result, the manufacturing process (engineered by Seiko Epson) is very similar to the one currently used

for making TFT active-matrix LCDs. The essential difference is that the process uses fewer steps, because no cumbersome and light-absorbing polarizing filters, reflectors, or spacers are needed. In use, LEP displays also offer significant savings over LCDs, because no backlight components are needed to make the display visible.

Other immediately perceived benefits are the display's speed and its extreme viewing angle, which results from the active area being just microns deep. Gostick says speed is limited only by the RC time constants of the TFTs and connecting signal wires. Persistence then becomes an issue for the system designer, rather than a limit set by the material of the display.

But the biggest benefit, and the one that will ensure the commercial success of LEP, is that it protects intellectual and financial investments in system designs and manufacturing plants. For manufacturing, a standard LCD production line can be converted to LEP for minimal cost by disposing of redundant handling stages and installation of suitable ink-jet pixel printers (they don't have to print just pixels, of course). From the system designer's point of view, the LEP display will simply slip straight into any slot occupied by an equivalent LCD, with no more than basic tweaking of time constants.

Electrically, the prototype displays

work with around 4 V dc, and draw between 2 mA and 4 mA, depending on the luminance of the picture, says Gostick. Efficiency of the LEP material, in terms of converting electrons to photons, has been improved to between 5% to 10%, and is improving, Gostick claims. He says that there is little difference between green—the color chosen for the prototypes—and the red and blue emitting polymers that will be added to make a full-color display.

Physical construction is straight forward. The base is a polysilicon TFT active matrix adapted by Seiko Epson from a LCD. Each transistor in the matrix represents the anode for a pixel. The LEP material is then printed as pixels over the matrix. A second common layer of polymer is deposited over that to make a light-emitting junction for each pixel. The whole display is finished with a thin film of metal, which forms a common cathode. With a glass substrate for the TFT array, the prototypes measure just 2 mm thick.

The one remaining problem area is lifetime. Gostick says that development of the LEP material has reached a stage where 10,000 hours or more under full power has been achieved regularly with unencapsulated devices. He is confident that reliability will not be an issue when the time comes to market the devices.

Just when that will be is unclear. Gostick stresses that the relationship with Seiko Epson is purely a cross license agreement for development purposes. He won't say how or whether that will develop into something more commercial.

Equally secret are CDT's plans to market LEP material in a form suitable for ink-jet printing, or which companies will be licensed to make it in production volumes. Already CDT has licensed Hoechst a.g., Frankfurt, Germany, to manufacture the material. Philips Components B.V, Eindhoven, The Netherlands, and Uniax Corp. Santa Barbara, Calif., have also bought licenses to CDT's patents on LEP.

Readers can find more information on the physics of LEP on CDT's web site at www.cdttld.co.uk.

PETER FLETCHER



The proof-of-concept models of the displays based on light-emitting polymers are monochrome devices with a diagonal screen size of 2.5 in.

The Future Of The Pentium Processor Family Is Unveiled And Looks Promising: A Solid Plan For Extending System Performance

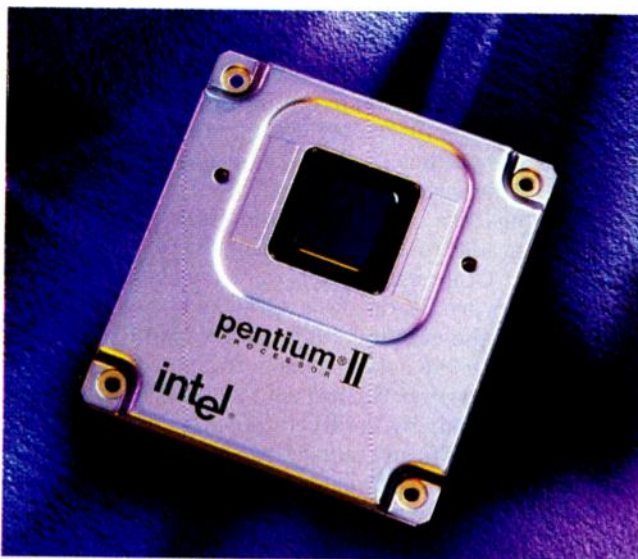
With CPUs able to clock at speeds of up to 450 MHz, and system bus interfaces clocking at 100-MHz rates, the future of the Pentium family looks promising. The first details of Intel Corp.'s game plan were unveiled last month at the Intel Developer's Forum held in San Jose, Calif.

In addition to revealing the IA-32 architecture in various presentations over three days, Intel provided details on its new Slot 2 interface. The company is targeting the new interface at workstation and server motherboards. Additional presentations covered its just-released i740 3D graphics controller, and system initiatives for DVD,

I/O buses, instant-on PCs, and other applications. The company said that efforts also are underway to improve processor performance in portable systems—the result, a new CPU minimodule format for the mobile computer market. The new module, slated to be released later this year for the Pentium II, also was disclosed at the forum (*see the figure*).

Key to the future, though, is the company's IA-32 CPU gameplan. It spans a wide range from 233-MHz Pentium CPUs on the "low" end to 450-MHz Slot 2 CPU modules at the high end by mid 1999. Currently, the Pentium family includes processors capable of operating at internal clock speeds of 333 MHz, and employing a 66-MHz, front-side system bus for main memory and I/O support. That will change shortly with the release of a 100-MHz, front-side bus interface that will allow for a 50% increase in memory bandwidth and data transfers to the peripheral subsystem.

The new minimodule format provides a form factor that is one-quarter the size and one-sixth the weight of the previous Pentium module that was available for portable platforms. The minimodule format squeezes the CPU, cache, and Northbridge logic



The new Pentium II minimodule format will offer a form factor one-quarter the size and one-sixth the weight of the previous Pentium module available for portable platforms.

chip into a volumetric area of just 22,000 mm³ (which is just under 2 in. on a side). Furthermore, the use of the company's advanced 0.25- μ m, five-layer, CMOS technology to produce the processor and cache chips, drops the processor's power consumption to less than 9 W when operating at a clock frequency of 233 MHz. That's a power level comparable to that of a 166-MHz Pentium processor with MMX technology.

Higher-Speed Versions

And even higher-speed versions of the minimodule will be available. Plans call for versions with clock speeds of 266 and 300 MHz to be released over the next 12 months. The module weight of just 35 g also reduces the weight of the CPU module considerably, allowing designers to redistribute or reduce the weight budget for future mobile systems.

For desktop platforms, cost reduction is the key to continued system volume growth. For that market, two new Pentium-class processors, code-named Covington and Mendocino, will be released later this year. First out will be the Covington, a 266-MHz device in a low-cost, card-edge, module format with a 66-MHz, front-side bus

interface. Later in the year, the more highly integrated Mendocino processor, which contains a level-two cache on the chip, will be released. The Mendocino chip will initially be able to operate at clock speeds of up to 300 MHz, with faster versions expected in 1999.

Midrange systems, currently served by the Pentium II modules, will continue to feature SECC vertical-mount modules. The current speed grades of 233 to 333 MHz will be supplemented by even higher-speed modules. Clock speeds will see 350, 400, and even 450 MHz over the next 12 months. These faster modules will include 100-MHz

front-side buses, and will be supported by new motherboard chip sets.

For the high-end of the product line—targeted at servers and workstations, the company plans to release a Pentium II processor module with 512 k, 1 M, or 2 Mbytes of cache; a 400- or 450-MHz internal CPU clock; and a 100-MHz front-side bus. The module will employ the company's yet unreleased Slot 2 expanded interface, which will permit N-way multiprocessor systems to be implemented.

Furthermore, if designers felt the desktop Pentium II Slot 1 module was difficult to deal with, look out! The Slot 2 modules are even larger—about twice the height of the original module, and even wider to accommodate the higher-pin-count bus. Also targeted at workstation-type systems, is a Pentium II Slot 2 module to be released in the first half of 1999. Code-named Katmai, the module's CPU will clock at 450 MHz, pack 512 kbytes of cache, and employ a 100-MHz front-side bus.

In addition to all the developments planned for the IA-32 32-bit architecture, design teams at Intel are releasing more details of their IA-64 64-bit design efforts. Although first described last year at the fall Micro-

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processor Forum, the IA-64 processors will be based on a technology the company calls explicitly parallel instruction computing (EPIC). This architectural approach takes advantage of the high levels of integration that will be possible with 0.18- μ m CMOS technology and the abundant CPU resources that it will permit designers to co-locate on a single chip.

Although details of the first hardware implementation will not be available until later this year, the company has indicated that the architecture permits multiple CPUs, multiple

floating-point units, and large register files (128 general-purpose registers for the integer processors, 128 floating-point processors, and 64 single-bit predication registers) to reside on a single chip.

Coupled with advanced compiler technology, the IA-64 architecture can leverage on-chip parallelism. It must first parallelize the code during compilation and then distribute the parallel operations among the multiple on-chip execution units. As a result, as many of the on-chip execution units as possible will be kept active during every in-

struction cycle. Additionally, the speculative execution allows the processor to execute both paths of the instruction branches so that both results will be ready to evaluate when the processor needs the answer. That process eliminates many of the overhead delays associated with operations such as branches (such as those found in if-then-else operations).

For an overview of these CPUs and the other developments announced at the Intel Developer's forum, set your browser to: developer.intel.com.

DAVE BURSUKY

3D Electromagnetic Modeling Techniques Expedite Accurate Design Of Septum Magnet

Physicists at the Brookhaven National Laboratory, Upton, New York, have used 3D electromagnetic-design analysis and simulation software to design a unique septum magnet to extremely accurate specifications. The magnet will be used to guide a metal ion beam of an alternating-gradient-synchrotron (AGS) accelerator into a circulating beam of the laboratory's relativistic heavy ion collider (RHIC).

Due to the magnet's critical location, at the intersection of the two beams, the field strengths generated by the magnet must be extremely precise. In fact, the two beams themselves are only 6 mm apart. That means the high magnetic field in the injected-beam region must be negligible in the circulating-beam region. And, the specs demand that the magnet bend the injected beam by 38 mrad, after which it continues on a straight path tangent to the circulating beam.

To ensure that the beam size at the entrance and exit of the magnet, for both injected and circulating beams, are not disturbed, the geometry of the magnet had to be right. This required the surface of the bottom pole of the magnet to make an angle of 2.57 mrad with the central ray of the circulating beam, and 2.24 mrad with the axis of

the pipe the beam circulates.

While 2D electromagnetic calculations enabled the scientists to design the cross-section of the magnet, the 2D software was unable to accurately model the conditions at the exit and entrance of the magnet. These conditions at the edges are three-dimensional due to the fringe fields around the entrance and exit holes, says physicist Nicholas Tsoupas. Consequently, finite-element-based 3D analysis software developed by Vector Fields, Aurora, Ill., was used to generate a very accurate model of the magnet and its field, Tsoupas says.

The 3D code also helped in precisely placing filed clamps at the entrance and the exit of the magnet to further reduce the fringe field (*see the figure*).

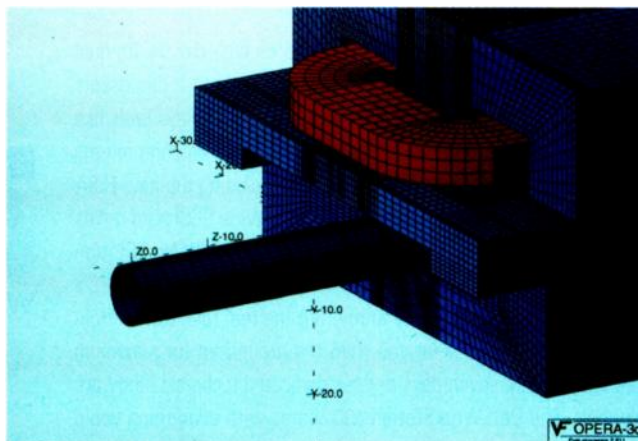
According to Tsoupas, scientists were able to change the model to reflect a new concept design within 30 minutes. And, after 14 iterations of changing the design and rerunning the analysis, they were able to accomplish their goal. The final results showed a maximum field of only 0.55 Gauss in the circulating-beam region.

Based on the 3D models, Brookhaven scientists have built an experimental magnet and verified the results. To their surprise, the actual field value in the circulating beam is substantially lower than predicted by the analysis. However, because the measurement of such small fields was not easy, the scientists concluded the analysis results are well within the range of the physical measurements.

The septum magnet is part of a \$500 million RHIC project that will explore matter and recreate the conditions of the "big bang" theory of how the universe was formed. The project will also test the current theory that protons, neutrons, electrons, and other basic components of matter were formed from the quark-gluon plasma as it cooled.

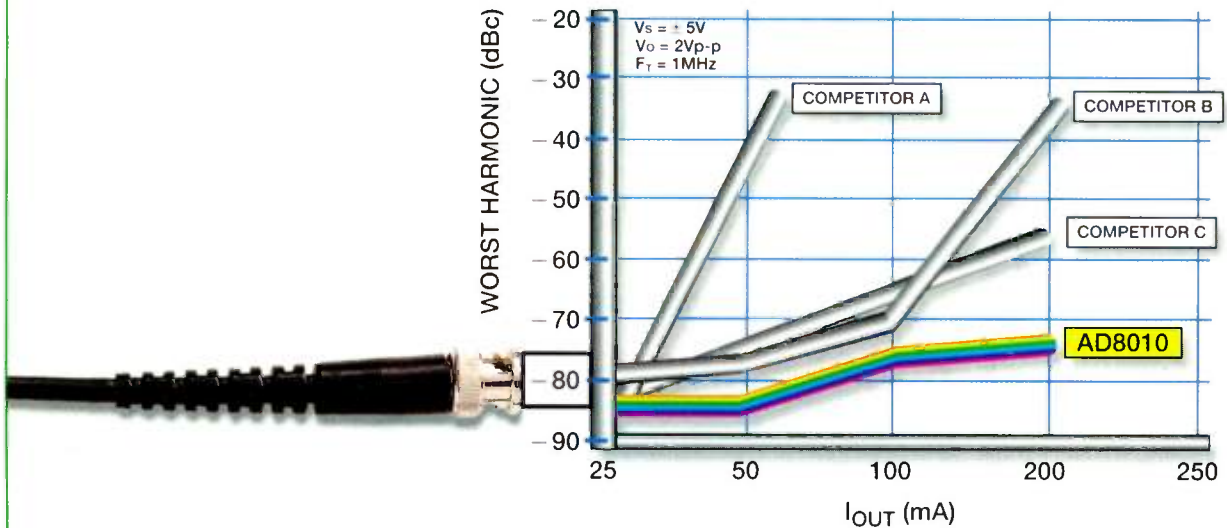
For further information, contact Nicholas Tsoupas at Brookhaven National Laboratory, P.O. Box 5000, Bldg. 911B, Upton, N.Y. 11973-5000. Telephone (516) 344-4979. www.bnl.gov. Or contact Jonathan Oakley at Vector Fields Inc., 1700 N. Farnsworth Ave., Aurora, Ill. 60505. Telephone (630) 851-1734. www.vectorfields.com.

ASHOK BINDRA



This 3D simulation of the Brookhaven National Laboratory septum magnet shows the coil, the field clamp, and the beam tube through which the beam of particles are directed.

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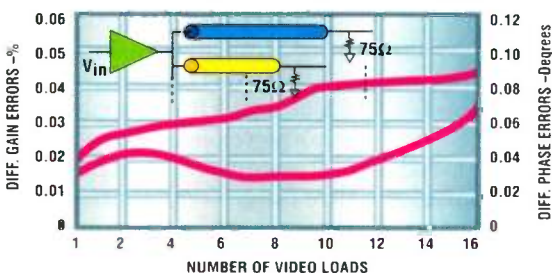
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TECH INSIGHTS

■ Exploring power-management design issues for advanced microprocessors

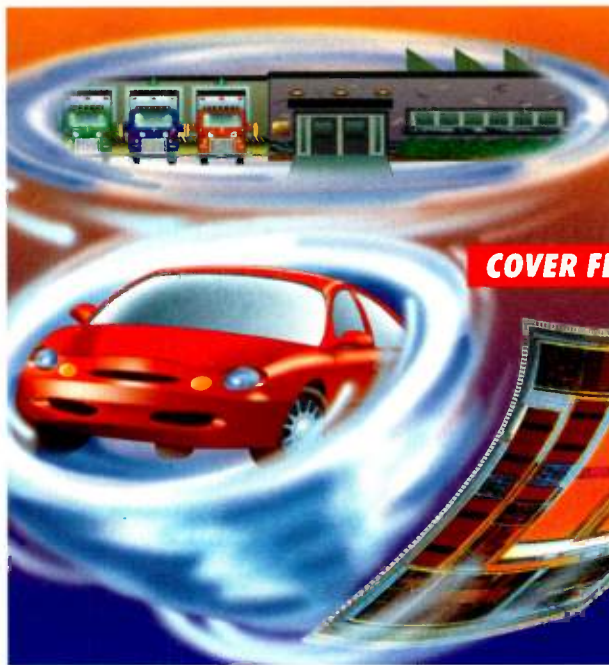
High-Integration Controller Tackles Automotive And Industrial Needs

Based On The PowerPC, This RISC CPU Packs 448 Kbytes Of Flash And Is A Complete Data Acquisition And Control System.

Dave Bursky

Automotive systems present a challenging design environment for embedded processors. Circuits must be rugged enough to handle harsh physical and electrical environments, and be highly integrated to keep costs as low as possible. Additionally, as new antipollution and safety regulations come on line, measurements and computations performed by the embedded controllers will get more complex, increasing the workload the processors must handle.

To approach the wide array of processing tasks in the automotive and industrial environments, designers at Motorola collaborated with engineers at automotive manufacturers to define a new high-end processor with a highly-integrated solution. The result is a 32-bit, PowerPC-based RISC processor internally referred to as Black Oak (the MPC555). The new processor can run at clock rates up to 40 MHz. In addition to the processor's PowerPC core with a floating-point unit, the computational portion of the processor packs 448 kbytes of flash memory (divided into two blocks of 256 and 192 kbytes) for program storage; 26 kbytes of fast static RAM (split into one 16-kbyte and one 10-kbyte block); a four-bank memory controller that works with SRAM, EPROM, flash EEPROM, and other peripherals; and a flexible memory-protection



COVER FEATURE

unit (Fig. 1).

Additional on-chip resources include two queued analog-to-digital converter (ADC) modules, each capable of handling up to 16 analog input channels; two CAN 2.0B controller modules for automotive/industrial networking; and 6 kbytes of RAM. The RAM is dedicated to the pair of time-processor unit (TPU3) blocks that each provide a dedicated macroengine that operates independently of the main CPU. Each TPU3 block provides up to 16 independently programmable channels and pins. There's also an 18-channel modular I/O subsystem that provides pulse-width modulated functions—counters and

other I/O port functions; a queued serial multichannel module with two high-speed UARTS and a queued serial port; and a system-bus-interface control block that includes some general-purpose I/O support.

In one sense, the chip can be thought of as a full data-acquisition, data processing, and control system all integrated onto a single piece of silicon that fits in a 272-lead plastic BGA package (256 active pins). As mentioned earlier, such a solution must also be cost effective. To that end, Motorola's designers have developed a very-dense flash memory cell structure that dramatically shrinks the area needed for the flash-based storage. A 3.3-V supply reduces the

chip's power consumption, allowing it to operate over a -40 to 125°C temperature range (see "Maximizing Chip Performance," p. 44).

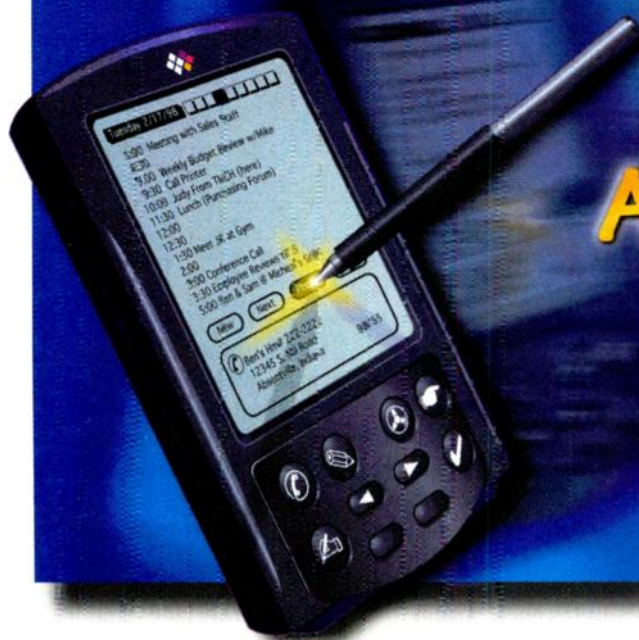
Four power modes—On, Doze, Nap, and Sleep—allow designers to optimize system power consumption by switching modes. At top speed the chip is relatively light on power, consuming about 1 W. But in the Doze, Nap, and Sleep modes, power will drop from tens of milliwatts to less than 1 mW in the deepest power-down state.

Intelligent Engines

The large on-chip memories allow the processor to pack all the memory

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Key Applications:

- PDA (Personal Data Assistant)
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- Touch Screen White Boards

Key Features:

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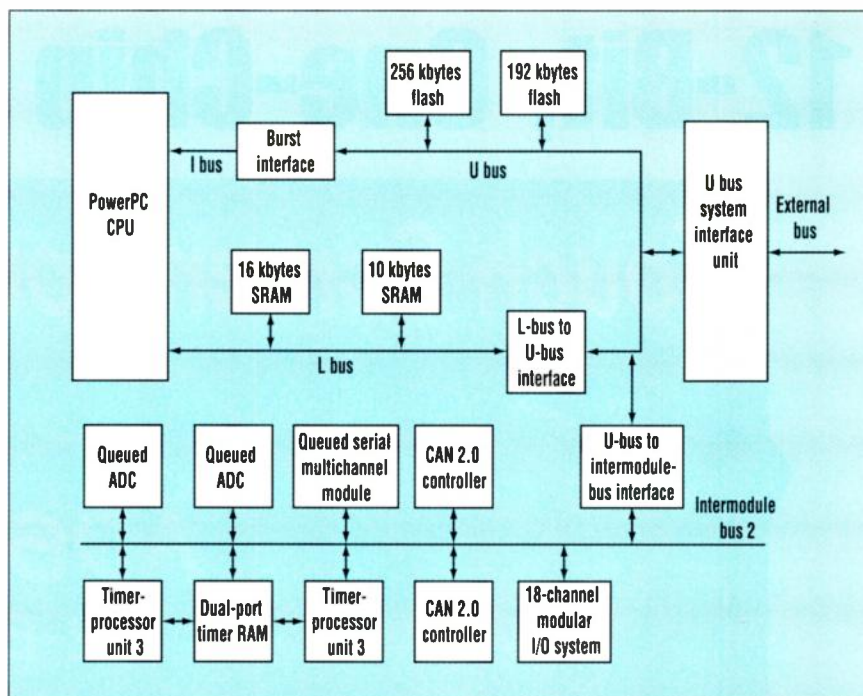
required for an engine control system. By eliminating off-chip memory, power consumption decreases, system communications improves, and system reliability increases.

By keeping the floating-point co-processor on the chip, system engineers can let the processor perform on-the-fly engine performance characterization without requiring large external or on-chip look-up tables. Instead, smaller tables can be used with just a few values. Intermediate values can then be calculated on-the-fly. An engine will soon be able to analyze itself and optimize internal operations to adjust things such as valve timing, firing points, etc.

In the long run, the control systems will allow the engine to compensate for even the slight mechanical differences from cylinder to cylinder, thus delivering optimal efficiency and minimal emissions. The all-in-one solution also allows car manufacturers to position the chip and controller box closer to the engine. This location reduces the amount of noise generated by the high-speed circuits that reaches the radio, simplifying the filtering that must be included in the radio. Additionally, the all-in-one solution keeps virtually all the high-frequency paths within the chip, reducing overall RF emissions.

When clocked at 33 MHz, the PowerPC 32-bit core delivers a throughput of 43.5 kMIPS (using the Dhrystone 2.1 benchmark). That clock rate can increase up to 40 MHz with an accompanying increase in throughput. Designed to be fully static, the core is compliant with the PowerPC architecture (Book 1) specification. It also implements a precise exception model and includes extensive system development support. Some of that support includes on-chip watchpoints and breakpoints, program flow tracking, an on-chip emulation development interface (the company's OnCE interface port), and an IEEE 1149.1 JTAG test access port.

To support the processor, its designers included a four-bank memory controller that allows the chip to work with SRAM, EPROM, flash EEPROM, and other memory-mapped peripherals. As part of the interface, they also included byte-write enable lines and 32-bit address decodes with bit masks. The memory protection unit provides four instruction regions and four data re-



1. A complete data-acquisition and control system on a chip, the MPC555 developed by Motorola for automotive applications, is based around a PowerPC 32-bit core. It packs 448 kbytes of flash non-volatile memory, 26 kbytes of SRAM, and an additional 6 kbytes of dual-port memory that either supports the timer-processor units or can be used as general-purpose SRAM. For data collection and control, the chip also packs dual 10-bit 16-channel ADCs, dual CAN 2.0 controllers, a total of 48 timing channels, general-purpose I/O lines, and several serial ports.

gions, with the ability to support region sizes of 4 to 16 Mbytes each. Additionally, the protection unit provides support for speculative accesses.

The processor's four power modes work in conjunction with the chip's

system interface unit that includes a clock synthesizer, time base, periodic interrupt timer, hardware bus monitor, and an interrupt controller that can service up to eight external and internal interrupt sources.

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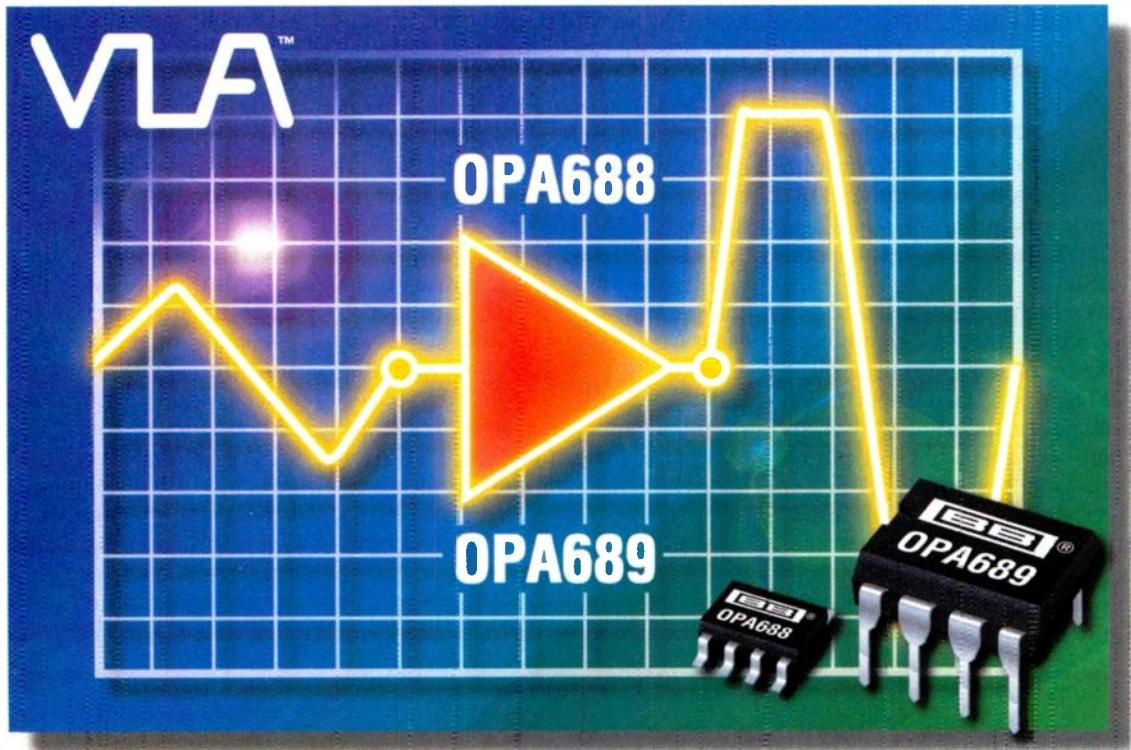
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Key Specifications:

- High Bandwidth..... 260MHz at $G=+2$
- High Slew Rate..... $1000\text{V}/\mu\text{s}$
- Input Voltage Noise..... $6.3\text{nV}/\sqrt{\text{Hz}}$
- Packaging.....8-pin plastic DIP, SO-8
- +5V Single or $\pm 5\text{V}$ Dual supply operation
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Key Specifications:

- High Bandwidth..... 280MHz at $G=+6$
- High Slew Rate..... $1600\text{V}/\mu\text{s}$
- Input Voltage Noise..... $4.6\text{nV}/\sqrt{\text{Hz}}$
- Packaging.....8-pin plastic DIP, SO-8
- +5V Single or $\pm 5\text{V}$ Dual supply operation
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The external interface provides 24 address lines, 32 data lines, and can support multiple master designs. The external bus interface can handle four-beat transfer bursts and two-clock minimum bus transactions. In the single-chip mode, the address and data lines can be used as general-purpose I/O lines. Additionally, the 18-channel modular I/O subsystem provides nine general-purpose I/O lines. The subsystem also can use many of the peripheral I/O pins as general-purpose I/Os when they're not being used for their primary functions.

The large flash memory is based on a new single-transistor cell that allows the 448 kbytes of storage to fit in space that previously could hold less than 25% to 50% of that amount. And, the flash array is fast—an on-page read can be done in just one system clock (25 ns), and an off-page read can be done in two system clocks (50 ns). In comparison, previous-generation flash memories had access times of approximately several hundred nanoseconds, which

caused a bottleneck with fast CPUs.

The flash array is divided into two sections, one that holds 256 kbytes and the other, the remaining 192 kbytes. Both sections are subdivided into 32-kbyte blocks, with the large section containing eight blocks and the smaller array packing six. The memory employs page-mode operation for reads, and can be block-erased in chunks of 32 kbytes. Data can be transferred to the flash array over the internal bus in word widths of 8, 16, or 32 bits.

The flash memory array was split into two sections so that software can "ping-pong" between them, allowing reads from one section while writes are done to the other. For programming and erasure, an external 4.75-to-5.25-V supply must be connected to the flash programming supply pin. Programming the array can be done quickly because up to 14 64-byte pages (each in a separate block) can be programmed simultaneously.

Complementing the flash memory array is a 26-kbyte SRAM array that

supports the CPU, and a second 6-kbyte block of SRAM that supports the timer subsystem. Accesses to the 26-kbyte SRAM blocks can be done in a single cycle, although a dual-cycle access mode is available for low-power operation. Additionally, byte, half-word, or word read or write accesses can be done in the SRAM. Protection control bits allow memory regions to be protected on 4-kbyte block boundaries. A low-power standby mode is available for data-retention when the chip is placed in its lowest-power mode.

Claiming the highest number of timers for any embedded processor, the 48-channel timer subsystem comprises dual time-processing units (TPU3 blocks) and the modular I/O system (MIOS). Similar to the TPU employed in other Motorola embedded processors, the TPU3 module can be viewed as a special-purpose microcomputer that performs a programmable series of matching and capturing operations. In the block is a scheduler and micro-engine controller that control the time

Maximizing Chip Performance

The harsh automotive environment requires a circuit design and process technology capable of wide operating temperatures, high performance, and handling the rough conditions under the hood. Fabricating the MPC555 consists of a dual-polysilicon, triple-well CMOS process based on 0.4- μ m minimum features. The technology incorporates low-voltage (3.3-V) surface-channel nMOS transistors, high-voltage (5- and 12-V) nMOS and pMOS transistors, a single-transistor flash EEPROM storage cell, and various resistors and capacitors for analog circuits. Three layers of metalization with full, global planarization between metal layers by chemical-mechanical polishing (CMP) help minimize chip area.

The "MoneT" (Motorola one transistor) flash EEPROM cell is the key to the high-speed, 448-kbyte storage array included on the chip. The memory cell consists of a standard, stacked wordline/floating-gate combination structure. It employs Fowler-Nordheim tunneling for both programming and erasure, which results in a low current flow during the program and erase operations. A narrow voltage spread in the distribution of programmed bits enables the read operation to be performed without a word-line boost over the full range of the supply voltage (2.7 to 3.6 V). The flash memory cells were designed to operate over an ambient temperature range of -40 to +125°C.

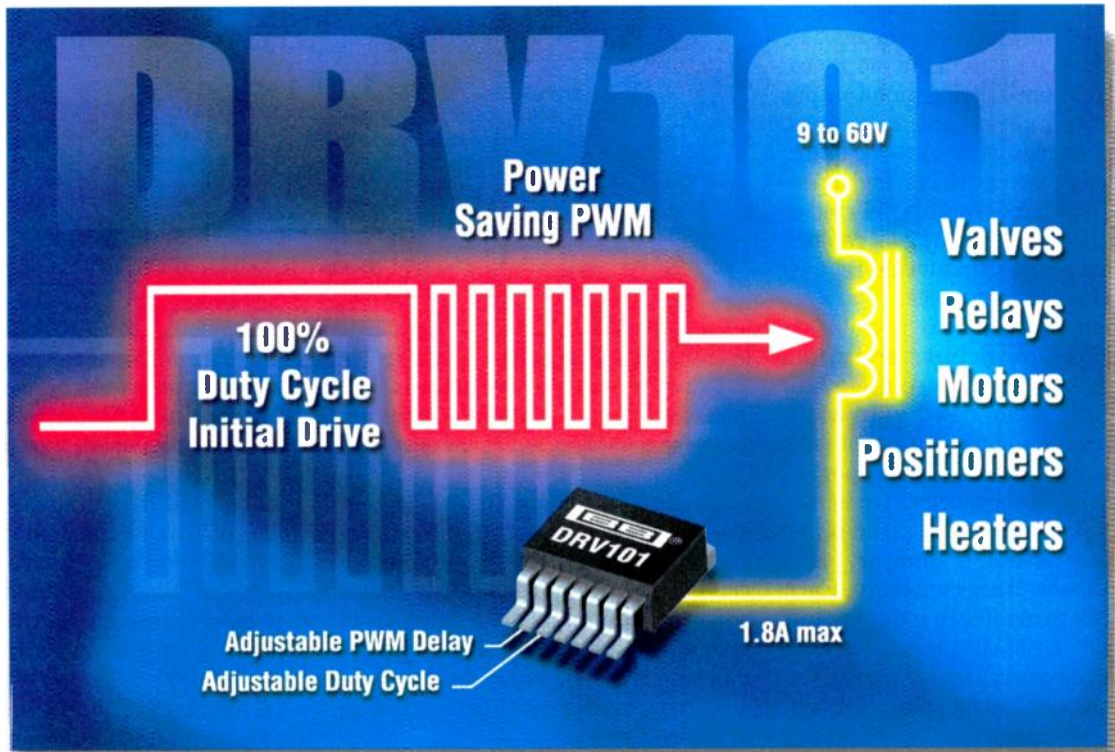
To achieve the chip's 40-MHz operating speed, the process it is made on was tuned to match the requirements of the flash memory with those of the CPU. The

flash memory array is optimized based on Motorola's MoneT bit-cell characteristics to achieve high-speed operation. The result is that the on-chip flash memory is fast enough to eliminate the need for an area-consuming and costly on-chip cache memory.

Included on the chip to improve CPU throughput are four non-overlapping 32-byte read page buffers for the embedded flash memory. An on-page read access returns data in a single system clock cycle, while an off-page read access returns data in two system clocks. Each read page buffer is associated with a different section of the flash memory address space to improve on-page access rates when branching or performing data fetches from the flash, while also fetching program code. Additionally, to compensate for the slower programming/erase capability of the Fowler-Nordheim tunneling mechanism, a page-mode programming scheme was selected. A 64-byte programming page buffer is tied to each erase block to allow for highly parallel program operation. For the MPC555, up to 14 64-byte pages, or a total of 896 bytes, may be programmed at once.

As a result, simulations show that code running from the internal flash memory executes much more quickly than code from external memory, with almost the same performance as if the code had been preloaded into a cache memory. For a true inline code, the average access time is slightly greater than one cycle (1.125). One additional cycle is required for each branch taken.

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Key Specifications

- Supply Voltage9V to 60V
- Load Current1.8A max
- On/Off InputCMOS/TTL
- Error Flag OutputOpen-Collector (TTL/CMOS)
- Packages7-lead TO-220, 7-lead surface-mount DPAK
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bases and timing channels (Fig. 2).

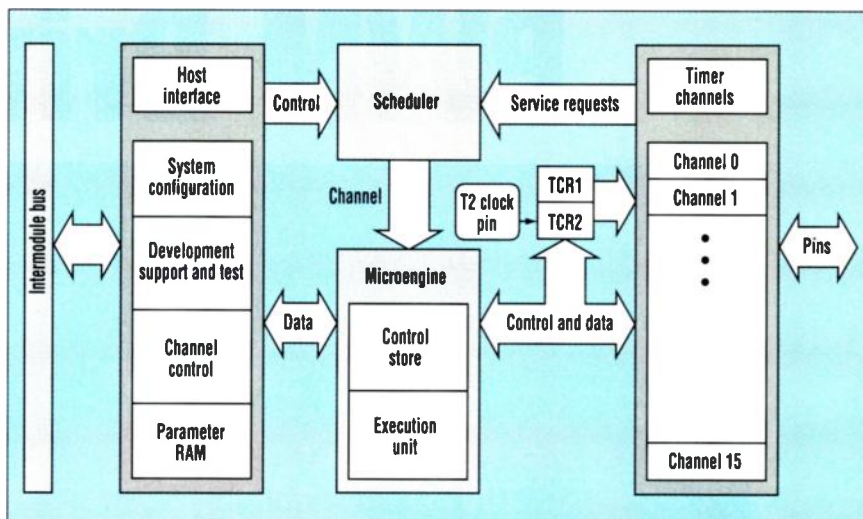
Slightly enhanced over the previous TPU modules, the TPU3 block doubles the amount of microcode used for programming (now up to 4 kbytes), and adds two more word-wide parameters per channel (now up to 8 words). The two 16-bit time bases in the block provide the reference timing for all output compare and input capture events. Each occurrence of a match or capture operation is called an event, and a programmed series of events is referred to as a function. TPU functions replace software functions that would require host CPU interrupt service.

Programmed functions available include input capture/input transition counter, output compare, pulse-width modulation, synchronized pulse-width modulation, period measurement with additional transition detect, period measurement with missing transition detect, position-synchronized pulse generator, stepper motor, and period/pulse-width accumulator. Each TPU block provides 16 independent and functionally identical channels, each connected to one of the I/O pins. Each channel has eight 16-bit parameter registers and an event register comprising a 16-bit capture register, a 16-bit compare register, and a 16-bit comparator.

As part of the TPU, the 6-kbyte SRAM serves to store the timer microcode. A control block that ties the memory into the TPU and the CPU, provides dual-port access to the memory array so that both TPU blocks can read from the memory. Typically, the SRAM would be loaded with microcode by configuring it as general-purpose memory and then after loading, reconfiguring the block as dedicated microcode memory for the TPUs. In the microcode mode, the host CPU cannot access the memory.

Real-World Interfaces

Providing all the analog inputs to the processor, the dual-queued ADC modules each provide 16 analog input channels, with a resolution of 10 bits per channel. Through the use of internal and external multiplexing, the number of channels can be expanded to a total of 41 for each module. Typical conversion time is 7 ms (142,000 samples/s), with the use of the on-chip sample-and-hold amplifier. Each converter module also includes two conversion command



2. Each of the two timer-processor units (TPUs) is based on a programmable microengine and scheduler that gets its control information from a dual-ported block of RAM shared by the two TPUs. The microengine sets up and controls 16 independently-programmable timer channels.

queues and automated queue conversion modes that can be initiated by either an external edge-triggered/level-triggered gate, internal timer, or a software command. The converters also allow subqueues using a pause mechanism. The output data is readable in right- or left-justified, signed, or unsigned formats.

The converter blocks were fabricated in the basic nonvolatile memory process. They do not require any unique process steps or trimming for resistors and/or precision matching of capacitors. They deliver 10 bits of resolution with two counts (LSB) of accuracy. The queues in the two converter blocks provide a total of 64 words of result storage. This minimizes frequent CPU interrupts and provides a flexible operating scheme.

Timed triggering of the analog-to-digital conversion provides better synchronization with the on-board timer channels. Furthermore, the use of the dual converter blocks provides system redundancy. It also allows the converters to be configured for differential sensing with synchronized queues. A gated mode, like an event counter, allows continuous sampling while the gate is held open by an external signal.

For communications in the automotive environment, the MPC555 processor includes a pair of CAN 2.0B controllers that provide the full implementation of the CAN protocol specification, versions 2.0 A and B. Each controller has 16 receive/transmit

message buffers that can hold messages of 0 to 8 bytes. Additional features include a 16-bit free-running timer for message time-stamping, a low-power sleep mode with programmable wake-up on bus activity, and programmable loop-back for self-testing.

A queued SPI port is also included on the chip; it provides synchronous full-duplex communications at maximum baud rates of one-quarter the system clock rate. The QSPI can handle up to 32 preprogrammed transfers, reducing processor overhead. It can also handle transfer lengths from 8 to 16 bits.

A wrap-around mode allows continuous sampling of a serial peripheral for efficient interfacing to serial ADCs. Also in this block are two serial communication interfaces (SCIs), that can operate in a UART mode with a non-return-to-zero format and half- or full-duplex mode. One of the SCI ports includes a 16-register receive buffer and a 16-register transmit buffer. Both SCI ports have advanced error detection and optional parity generation and detection.

Whether the application is a single- or a multichip implementation, the user can program the address, data, general-purpose I/O, peripheral, and control pins as desired. The MPC555 supports over 350 functional input/output signals in a 256-pin package. This flexibility is achieved by a high degree of multiplexing without affecting performance and reliability.

The MPC555's address and data pins are multiplexed with the general-

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OPA643 achieves low harmonic distortion over a wide frequency range by using a de-compensated voltage feedback architecture with two internal gain stages. Internally compensated for gains $\geq +3$ with 800MHz gain bandwidth product, OPA643 is particularly suited for wideband transimpedance amplifiers, moderate gain IF amplifier applications, and very low distortion ADC driving.

Key Specifications: OPA642 OPA643

Low Distortion	–95dBc at 5MHz	–90dBc at 5MHz
Low Noise	2.7nV/√Hz	2.3nV/√Hz
Gain Bandwidth Product	210MHz	800MHz
High Open-Loop Gain	95dB	95dB
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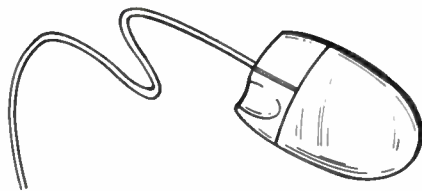
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purpose I/O pins (GPIOs), but the performance requirements of the address/data and GPIOs are very different. The address/data pins must operate at 40 MHz with 3-V levels, while the GPIOs are specified to produce 200-ns rise and fall times with 5-V levels. Each pin can be programmed to drive a slow slew-rate-controlled 5-V signal or a fast 3-V address/data signal. The 3-V logic is fully compatible with 5-V input levels.

The Black Oak processor is compatible with the instructions of the PowerPC and the MPC500 series of embedded PowerPC processors. However, tools enhanced specifically for the processor include compilers from Diab Data, Green Hills, Cygnus-GNU, and Microtec. Debugging tools will be available from Software Development Systems, Green Hills, and Lauterbach Inc. Several advanced tools specifically for automotive systems will be available this quarter from both Hewlett-Packard and ETAS.

Both a low-cost familiarization board and a full-function development system board will be available in the late second and third quarters, both with 40 MHz silicon. A cycle-accurate simulator will be ready in the third quarter from Software Development Systems, and real-time operating systems such as Motorola's own RTEK and ERCOS^{EK} from ETAS. In addition, Motorola can also provide services such as the development of low-level software drivers, high-level drivers, flash programming support, application routines, automotive electrical interfaces, and other services such as creating reference design or supplying known-good die.

However, with the built-in JTAG and OnCE test interfaces, a user can start testing and developing software with as little as a power supply and a DBM connection. The processor also has a self-clocking mode so that even the crystal can be eliminated for simple test execution.

PRICE AND AVAILABILITY

The MPC555 will sell for \$45 apiece, in lots of 10,000 units when it goes into production in late 1998. Samples will be available in the early third quarter of this year. Long-term projected pricing for the chip is estimated at about \$35 apiece in 10,000-unit lots in the year 2000.

Motorola Inc., 6501 William Cannon Drive West, Austin, TX 78735; Dick Spilo (512) 895-3260. **CIRCLE 50.**

FT • FS SERIES MODUFLEX® SWITCHERS

DESCRIPTION

The FT and FS Series are comprehensive lines of ultra compact power factor corrected models derived from our Moduflex® family of switching power supplies. This series utilizes advanced technology to produce a high quality input current wave form that is compliant to the harmonic requirements of EN61000-3-2. Based on modular construction, "off the shelf" modules permit high volume manufacturing with an outstanding quality level assuring timely delivery at a competitive cost.

Three classes of output modules are available. The **STANDARD** outputs allow short duration surge currents on all auxiliaries for hard starting loads. Optional **CURRENT LIMITED** outputs have square current limiting and feature wireless droop current sharing. Optional **ENHANCED** outputs have square current limiting, one wire star point current share, output good logic signal with LED, nominal 5V local bias, individual inhibit and margining. For requirements that cannot provide minimum load on the main output, the **ZERO PRELOAD** option is available for main outputs up to 500 watts.

DELIVERY

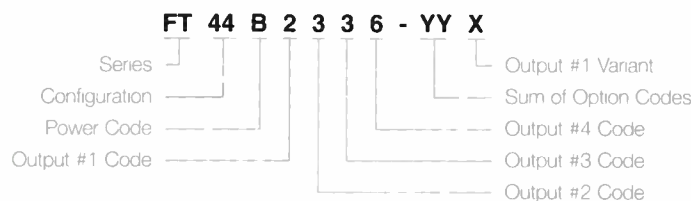
Choose stocked units or construct a model number using stocked modules for fast delivery. Otherwise, form a model from the adjacent page to meet your specific requirements. Contact factory for deliveries on models derived from non-stocked modules.

STOCKED MODELS - Available in 3 days.

Max Power	Output 1	Output 2	Output 3	Output 4	Model*
400W	5V @ 50A	12V @ 12A	12V @ 12A	5V @ 10A	FT46A2332-46P
400W	5V @ 50A	12V @ 12A	24V @ 6A	12V @ 6A	FT46A2363-45P
600W	5V @ 60A	12V @ 12A	12V @ 12A	5V @ 10A	FT46C2332-13P
600W	5V @ 60A	12V @ 12A	24V @ 6A	12V @ 6A	FT46C2363-13P

*400W models include power fail monitor, current limited modules, zero preload and end fan cover options.
600W models include the same options except fan cooling is built into the unit.

UNITS FROM STOCKED MODULES - Available in 2 weeks.



- Configuration:** Allowable quad output configurations are 42, 44, 46 and 48.
- Power Code:** Choose Power Code A through D for 400-750W models.
- Output Codes:** Select any outputs from the shaded area on the Output Types table consistent with the configuration chosen.
- Option Code:** Specify Option Code. Refer to the Option table. Codes 02 (redundancy) and 16 (enhanced) are excluded from models available in 2 weeks. Fan cooling is built into 600 and 750W units.

FEATURES

- 0.99 power factor.
- 5.5 watts per cubic inch.
- 1-7 outputs, 400-1000 watts.
- 120 kilohertz MOSFET design.
- Universal input.
- UL, CSA, TUV (IEC, EN), CE.
- FCC, EN Class A EMI.
- IEC, EN Immunity.
- All outputs:
 - Adjustable
 - Fully regulated
 - Floating
 - Overload and short circuit protected
 - Overtoltage protected
- Standard features include:
 - System inhibit
 - Fan output
- Options and accessories include:
 - Power fail monitor
 - Redundancy
 - Current Limited Outputs
 - Enhanced Outputs
 - Zero Preload
 - End fan cover
 - Top fan cover
 - Rack Assemblies

MODEL SELECTION

Models are available in power ratings of 400 to 1000 watts, with corresponding code letters A through E. See Power Code chart.

Output modules are available in six types: J, K, L, M, N and P in nominal power ratings from 75 - 500 watts. Type M, N and P modules are variable power rated depending upon the unit power rating. The M, N and P Module table directly below shows the corresponding multiplier applicable to the output current ratings of the M modules and allowable power ratings for the N and P modules. For example, a 750 watt multiple will have its M type module configured to produce 120A @ 5V or 12A @ 48V. The voltage and current rating of output modules are listed in the table of output types. This table assigns an alpha-numeric code designating the nominal voltage rating of the module.

Power Code	Unit Power Rating	M Module Current Multiplier		N/P Module* Allowable Power Rating
		Single Output	Multiple Output	
A	400W	0.8	0.5	250W
B	500W	1.0	0.6	300W
C	600W	1.2	0.8	400W
D	750W	1.5	1.2	500W
E	1000W	2.0	1.5	750W

*When an N or P module is used as the main output, the allowable power and the module current ratings must not be exceeded.

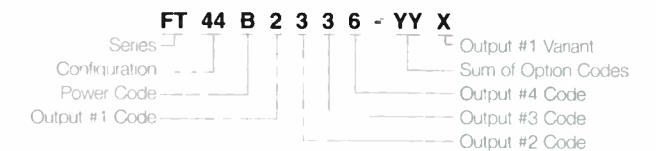
Code	Volts	Output Types* Module Type				
		J Amps	K Amps	L Amps	M Amps	N/P Amps
0	2	10	20	30	100	60
1	3.3	10	20	30	100	60
2	5	10	20	30	100	60
3	12	6	12	24	42	42
4	15	5	10	20	33	33
5	18	4	8	16	28	28
6	24	3	6	12	21	21
7	28	2.5	5	10	18	18
8	36	2	4	8	14	14
9	48	1.5	3	6	10	10
A	2.2	10	20	30	100	60
B	2.4	10	20	30	100	60
C	2.7	10	20	30	100	60
D	3	10	20	30	100	60
E	3.6	10	20	30	100	60
F	4	10	20	30	100	60
G	4.5	10	20	30	100	60
H	5.7	10	20	30	90	60
J	6.3	10	20	30	80	60
K	7	9	18	30	70	60
L	8	8	16	30	62	60
M	9	8	15	30	56	56
N	10	7	14	30	50	50
P	11	7	13	27	45	45
Q	13.5	6	11	22	37	37
R	17	5	9	18	30	30
S	19	4	8	16	26	26
T	21	4	7	14	24	24
U	23	4	7	13	22	22
V	26	3	6	12	19	19
W	29	3	5	10	17	17
X	32	2	5	9	16	16
Y	40	2	4	8	13	13
Z	44	2	4	7	12	12

Multiple output modules of a given type are arranged in ascending order by voltage magnitude in the same sense as the output number sequence in the configuration diagrams. *Shaded ratings are stock.

HOW TO ORDER

To form the proper model number defining a custom requirement, select the letters FS or FT to designate the series, then choose the desired configuration and list the configuration code. Insert the power code letter for the power level and follow with the output code numbers or letters for each specific output. Enter a dash and from the option table insert the sum of the option codes. Where lower power is desired for the main module, an N module can be substituted and is denoted by a letter N in the output variant position. In addition, when no preload is available for the main output, choose Option Code 08 and add a P in the output variant position. For an enhanced main and current limited auxiliaries, specify both 04 and 16 option codes.

HARMONIC CORRECTED 500W QUAD SWITCHER



OUTPUT CONFIGURATIONS

The boxes below are diagrammatic representations of the power supplies as viewed from the output end. The two-digit numbers above the boxes are the configuration codes.



Refer to the table below for allowable configurations by series.

Output Config	Unit Power Rating				
	400W	500W	600W	750W	1000W
12	•	•	• x	• x	x
24	•			• x	
26		•	• x	• x	x
30					x
32	•			• x	
34	•	•	• x	• x	
36	•	•	• x	• x	x
38					x
40					x
42	•	•	• x	• x	
44	•	•	• x	• x	x
46		•	• x	• x	x
48			x		x
50					x
52	•	•	• x	• x	x
54		•	• x	• x	x
56			x		x
62		•	• x	• x	x
64			x		x
72			x		x

• Represents allowable configurations for the FT Series.
x Represents allowable configurations for the FS Series.

SPECIFICATIONS

INPUT

90-264 VAC, 47-63 Hz.

POWER FACTOR

0.99 typical.

EMISSIONS

FCC 20780 Part 15/EN 55022, Class A Conducted. EN 61000-3-2, Harmonics. EN 61000-3-3, Voltage Fluctuations.

IMMUNITY

IEC 1000-4-2/EN 61000-4-2, Electrostatic Discharge. IEC 1000-4-3/EN 61000-4-3, Radiated Field. IEC 1000-4-4/EN 61000-4-4, Electrical Fast Transients. IEC 1000-4-5/EN 61000-4-5, Level 3 Surge. IEC 1000-4-6/EN 61000-4-6, Conducted Field.

INPUT SURGE

230 VAC - 38 amps max. 115 VAC - 19 amps max.

EFFICIENCY

75% typical.

HOLDUP TIME

20 milliseconds from loss of AC power.

OUTPUTS

See model selection table. Outputs are trim adjustable $\pm 5\%$.

OUTPUT POLARITY

All outputs are floating from chassis and each other and can be referenced to each other or ground as required.

LINE REGULATION

Less than $\pm 0.1\%$ or $\pm 5\text{mV}$ for input changes from nominal to min. or max. rated values.

LOAD REGULATION

$\pm 0.2\%$ or $\pm 10\text{mV}$ for load changes from 50% to 0% or 100% of max. rated values.

MINIMUM LOAD

Main output requires a 10% minimum load for full output from auxiliaries. Use Option 08 if no minimum load is available for mains up to 500 watts. Singles require no minimum load.

RIPPLE & NOISE

1% or 100 mV, pk.-pk., 20 MHz bandwidth.

OPERATING TEMPERATURE

0-70°C. Derate 2.5%/°C above 50°C.

COOLING

A min. of 10 LFS* for models without internal fans directed over the unit for full rating. Two test locations on chassis rated for max. temperature of 90°C. 600 watt, 750 watt and 1000 watt models have built-in ball bearing fans.
*Linear feet/second.

TEMPERATURE COEFFICIENT

$\pm 0.02\%/^{\circ}\text{C}$.

DYNAMIC RESPONSE

Peak transient less than $\pm 2\%$ or $\pm 200\text{ mV}$ for step load change from 75% to 50% or 100% max. ratings.

RECOVERY TIME

Recovery within 1%. Main output - 200 microseconds. Auxiliary outputs - 500 microseconds.

SAFETY

Units meet UL 1950, CSA 22.2 No. 950, EN 60 950, IEC 950.

ISOLATION

Conforms to safety agency standards.

INPUT UNDERVOLTAGE

Protects against damage for undervoltage operation.

SOFT START

Units have soft start feature to protect critical components.

OVERVOLTAGE PROTECTION

Standard on all outputs.

REVERSE VOLTAGE PROTECTION

All outputs are protected up to load ratings.

OVERLOAD & SHORT CIRCUIT

Outputs protected by duty cycle current foldback circuit with automatic recovery. Standard auxiliaries have additional back-up fuse protection. Options 04 and 16 have square current limiting with automatic recovery when overload is removed.

THERMAL SHUTDOWN

Circuit cuts off supply in case of local over temperature. Units reset automatically when temperature returns to normal.

FAN OUTPUT

Nominal 12 VDC @ 12 watts maximum.

INHIBIT

TTL compatible system inhibit provided. Option 16 has individual output inhibit.

REMOTE SENSING

On all outputs except standard and 04 Option outputs 75 watts or less.

SHOCK & VIBRATION

Shock per MIL-STD 810-E Method 516.4, Procedure I. Vibration per MIL-STD 810-E Method 514.4, Category 1, Procedure I.

MECHANICAL

CASE	SERIES	WATTS	H	x	W	x	L
1	FT	400W/500W	2.50"	x	4.93"	x	8.00"
3	FT	600W	2.56"	x	5.08"	x	10.03"
4	FS	600W	2.56"	x	5.08"	x	11.00"
5	FT	750W	2.63"	x	5.20"	x	10.03"
6	FS	750W	2.63"	x	5.20"	x	11.63"
7	FS	1000W	2.56"	x	7.13"	x	11.63"

OPTIONS

POWER FAIL MONITOR

Optional circuit provides isolated TTL and VME/VXI compatible ACFAIL signal providing 4 milliseconds warning before main output drops by 5% after an input failure. A SYSRESET signal following VME timing requirements is provided when an N module is used as a main output. Both logic signal outputs can sink current per the VME specification.

REDUNDANCY

Optional Or-ing diodes for hot pluggable N+1 redundant operation. For FT Series 500 watt & 750 watt models with 1-4 outputs. Main output current limited to 100 amps. Remaining outputs 16 amps max.

CURRENT LIMIT

Option provides on all outputs:

- Square current limit with auto recovery.
- Wireless droop current share for parallel or N+1 redundant operation.

ZERO PRELOAD

Optional circuit removes need for preload on main output up to 500 watts.

ENHANCED

Option provides on all outputs:

- Square current limit with auto recovery.
- Single wire active current share for parallel or N+1 redundant operation.
- DC output good logic signal with LED indicator.
- Logic inhibit.
- Nominal 5V bias.
- Margining.

END FAN COVER

Optional cover with brushless DC ball bearing end fan which provides the required air flow for full rating.

TOP FAN COVER

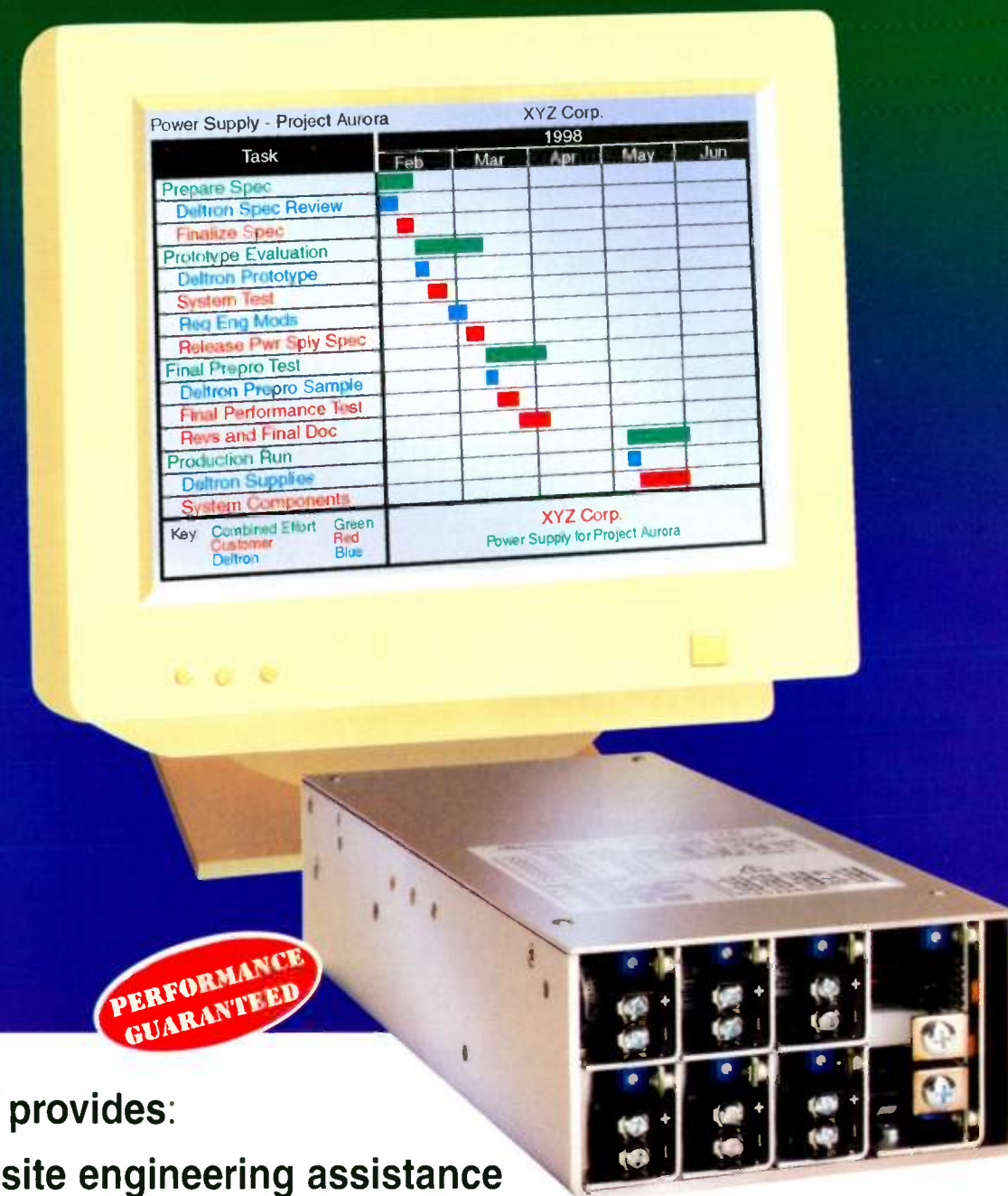
Same as above with fan cover mounted on top of the power supply.

ACCESSORIES

RA50 and RA75 Series 2U high rack assemblies provide hot pluggable interface and hold up to 3 FT Series 500 watt or 750 watt units respectively.

Specifications subject to change without notice.

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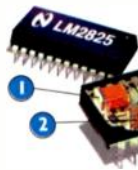
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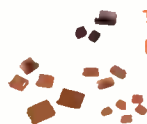


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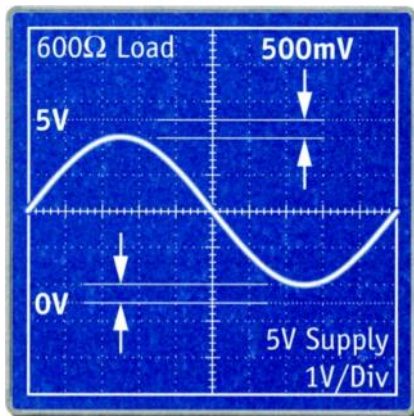


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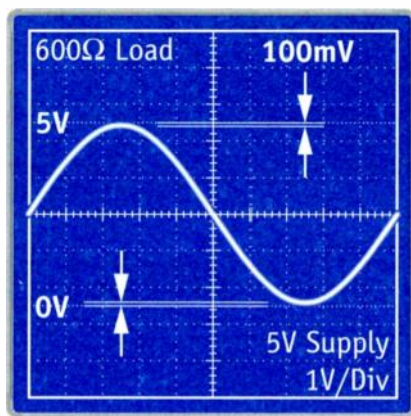
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The Specs

V_{SUPPLY}	$= 5.0V, -40^{\circ}C \leq T_A \leq 85^{\circ}C$
V_{OUT}	0.1V to 4.9V
$I_{OUT(SOURCING)}$	80mA
$I_{OUT(SINKING)}$	80mA
Input Offset	7mV
I_Q	1mA
I_B	64pA

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MAKING GLOBAL NETWORKS WORK

Get The Most Out Of ATM Networks With Multicasting

Careful Trade-Offs Must Be Made In ATM Multicasting Designs To Avoid Adding Excess Cost And Complexity.

JOSEPH C. LAU, formerly of TranSwitch Corp., 3 Enterprise Dr., Shelton, CT 06484; (203) 929-8810; fax (203) 926-9453.

Asynchronous Transfer Mode (ATM) has evolved from limited field trials to early volume deployment since the introduction of the first commercial product in 1993. There is a growing recognition in the industry that ATM connections to individual desktop computers will provide significant benefits to users including:

- A single network access point for all services
- Improved access to multimedia and video conferencing services
- Quality and simplified management of services

To increase the pace of ATM deployment, perceived barriers such as high cost and the lack of stable specifications for ATM services need to be overcome. The ATM Forum is moving rapidly to finalize key specifications that will make ATM the best option for multimedia applications. The specifications already finalized or soon-to-be finalized are:

- LAN Emulation
- Private Network Interfaces
- Multiprotocol Over ATM
- Traffic Management
- Switched Virtual Circuit
- Voice Over ATM

One common service that has become a business driver for the deployment of ATM networks today is the Internet. Recent dramatic increases in Internet access and usage have pushed up bandwidth demand and produced delays and congestion. ATM is an ideal solution for these applications, because it is inherently capable of providing the right quality of service (QoS) depending on the requirements.

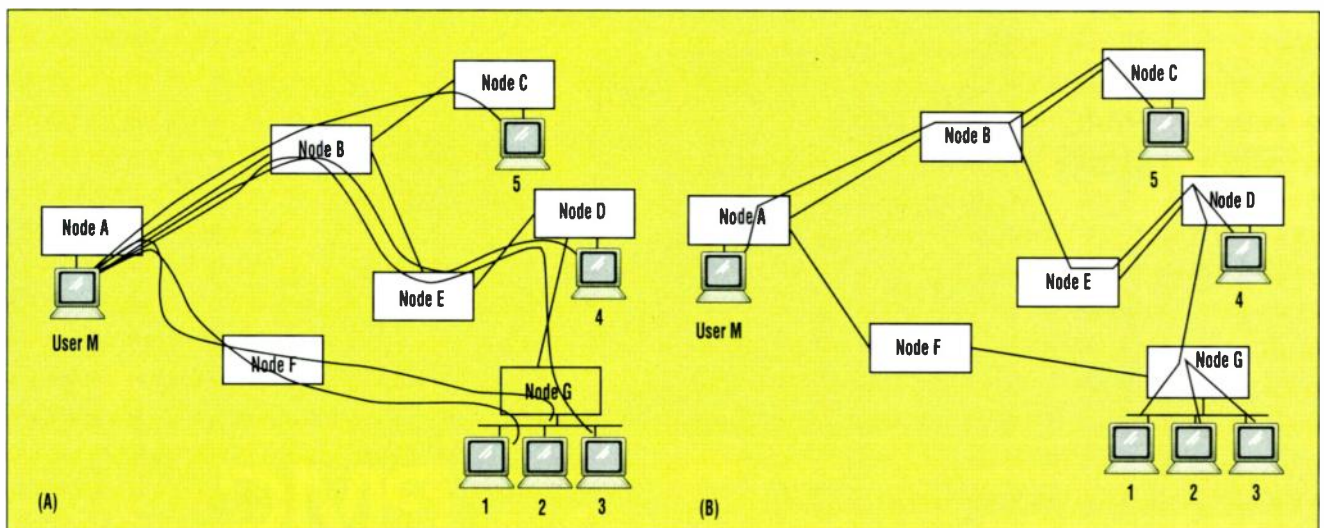
An approach that will enable ATM networks to be the most efficient and cost-effective solution is to use the switching capability of the network more efficiently. Such a scheme, multicasting, is discussed in this article.

The major advantage of an ATM network is its ability to transport different types of signals through a sin-

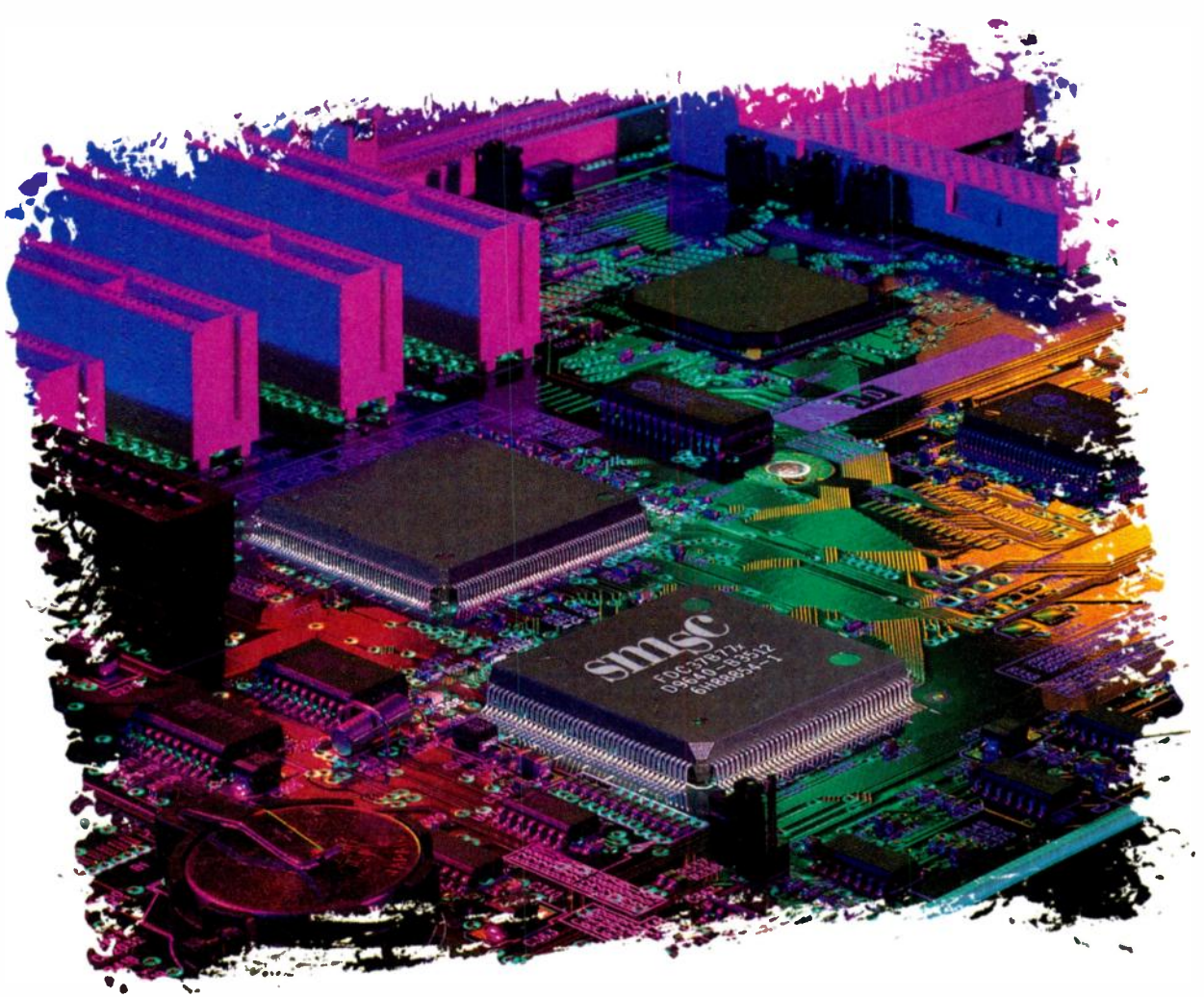
gle network using a standard cell format. Different classes of service imply various levels of cell priority, such as constant bit rate (CBR), for the transport of delay-sensitive traffic such as voice and interactive video; variable bit rate (VBR), for delay-insensitive traffic such as data; available bit rate (ABR), for non-time-critical traffic; and unknown bit rate (UBR) traffic.

Different modes of transmission demand support for unicast (point-to-point) and multicast (point-to-multipoint) transmission. Multicasting can be implemented as a series of multiple unicast links if the network is substantially under-used. But the recent dramatic increases in Internet usage will most likely overwhelm networks using the unicast approach. It is more economical to use true multicasting than to add more bandwidth and use unicasting. Therefore, the ATM switching nodes will need to provide both priority queuing and multicasting features.

Multicasting is an efficient way of



1. Transmission paths for broadcast messages in (a) a unicast environment and (b) a multicast environment.



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reducing the demand on the ATM network and switching bandwidth, thereby reducing the cost per connection. For example, if the ATM nodes do not have multicasting, a user sending an e-mail to coworkers 1, 2, 3, 4, and 5 must transmit five unicast copies of the same e-mail to five different destinations (Fig. 1a).

With multicast functionality, there are different ways the e-mails can be sent. One way is to send a copy to node B, from which it is multicasted to nodes C and E (Fig. 1b). Node C delivers the e-mail to coworker 5. Node E sends it to node D, where it is delivered to coworker 4, and passed down to node G, which delivers it to coworkers 1, 2, and 3.

Comparing Figures 1a and 1b, the unicast method uses 13 segments of the network while the multicast method uses only five (Table 1). Therefore, using multicasting in the above example results in a 62% savings on network bandwidth usage. Different amounts of network bandwidth would be saved if other paths are used. The trade-offs would be in the amount of delay and the probability of congestion.

Delay in a network is defined as the time it takes for the message to go from the sender to the receiver. The minimum delay is the sum of the time it takes for the message to travel across the links and the queueing time in the nodes. If any of the links in the path become congested, additional delay will be added until the link becomes available, assuming the message is not discarded due to congestion.

In normal operation, there should be no congestion, and the minimum delay is the absolute time it takes to traverse a path. In the e-mail example above, the use of multicasting sends the e-mail to coworker 1 through a four-node path versus a two-node path using unicast. As a result, the multicasting incurs more node and link delays. If L is the average delay through one node and one link, the average delay using multicast would be $4L$. This is the minimum possible delay assuming congestion-free transmission.

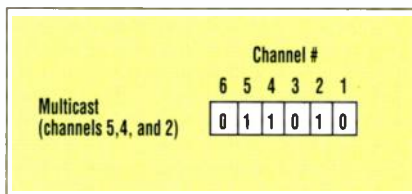
The total delay is dependent on how many times the

TABLE 1: NETWORK SEGMENT USAGE COMPARISON

Network Segment	Used in Unicast	Used in Multicast
AB	3	1
BC	1	1
BE	2	1
ED	2	1
DG	1	1
AF	2	0
FG	2	0
TOTAL	13	5

TABLE 2: COMPARISON OF P_{4F} AND P_{2F}

Probability of congestion P _{CU}	Probability of congestion-free transmission, P _{4F}	Probability of congestion-free transmission, P _{2F}
0.1	0.86	0.81
0.2	0.73	0.64
0.3	0.62	0.49
0.5	0.43	0.25
0.7	0.29	0.09
0.9	0.18	0.01



2. An in-band multiport indicator is a series of bits embedded within the existing cell which indicate the ports where the traffic will be directed.

e-mail stalls in a node, and the length of the congestion. Today, there is not enough experience with ATM traffic patterns, especially in the Internet service area, to give a definitive figure. However, a first-order estimate is given here to show the potential impact of multicasting.

If P_{CM} is the average probability of congestion for any node in multicast mode, and P_{CU} is the average probability of congestion for any node in unicast mode, the probability of conges-

tion-free transmission through the four-node path (P_{4F}) using multicast is:

$$P_{4F} = (1 - P_{CM})^4 \quad (1)$$

The probability of congestion-free transmission through the two-node path (P_{2F}) using unicast is:

$$P_{2F} = (1 - P_{CU})^2 \quad (2)$$

The probability of congestion in a network with multicast capability is smaller than with unicast only—in this example 62% lower. Therefore:

$$P_{CM} = 0.38 \times P_{CU} \quad (3)$$

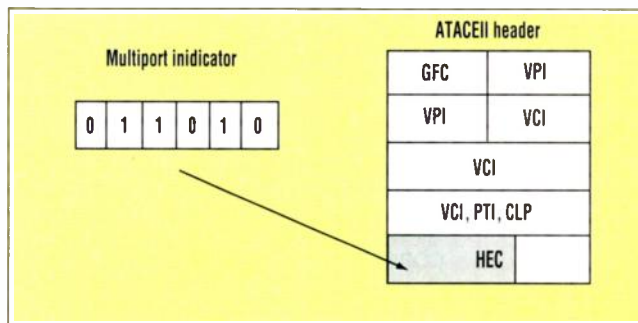
Combining equations 1 and 3 yields:

$$P_{4F} = (1 - 0.38P_{CU})^4 \quad (4)$$

A comparison of equations 2 and 4 is shown in Table 2.

For any given probability of congestion P_{CU} , the chance of having a congestion-free transmission is always higher using multicast than unicast, even though with multicast, the path is twice as long.

Therefore, using multicasting increases the probability of congestion-free transmission. Alternatively, the network can support more users for a given desired probability of congestion. The trade-



3. The ATM cell header's HEC byte is an easy location to implement an in-band multiport indicator.

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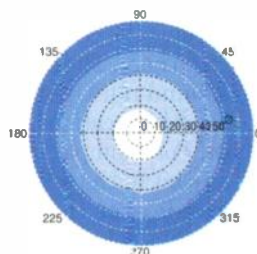
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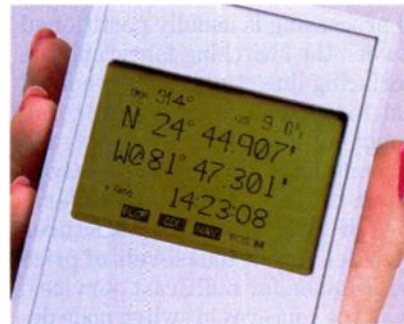
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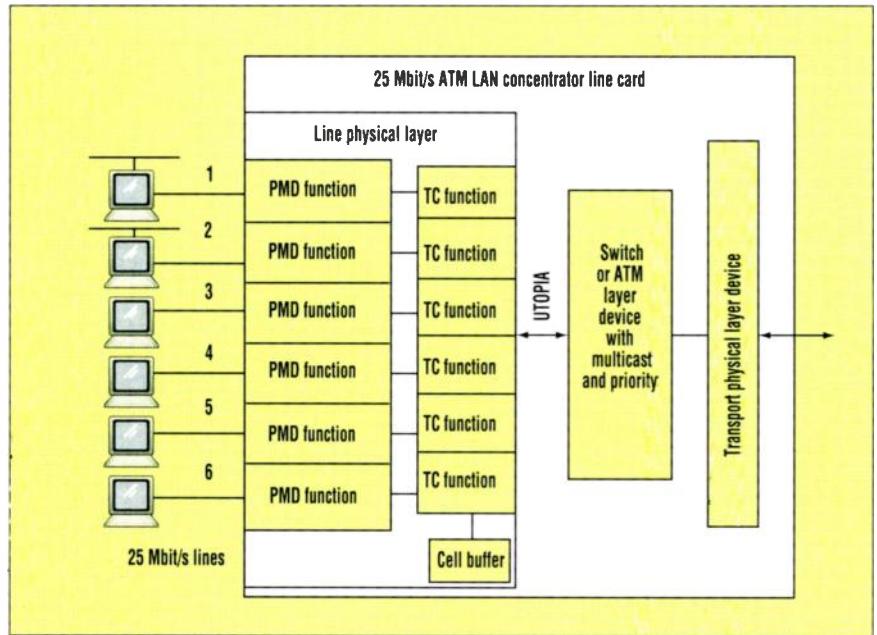
off is longer absolute minimum delay.

Within an ATM switching node, the cell processing is usually partitioned between the switching fabric and the interfacing line cards. Cells received on an incoming link are either stored in input buffers waiting to be routed to outbound links, or routed directly to output buffers. There are several types of ATM switch architectures which deliver various levels of price performance for multicast services. One of the concerns in switch node design is how effectively multicast and broadcast functions are supported.

Two options are: to queue up the cell in the input or output buffers within the switch fabric, or forward the cell to the queues in the interfacing line card. Although the first method results in very simple line cards, the disadvantages are an added memory requirement in the switch buffers, or an increase in blocking probability.

The advantages of the second method are lower memory requirement and less blocking probability in the switch fabric. On the other side, the disadvantage is the higher degree of complexity in an interface card design, such as the requirement for multiple virtual-circuit (VC) address translation before sending the cell to the multicasted terminals. The implementation of VC address translation requires a large amount of memory in the form of either a hashing function or content addressable memory (CAM).

Unfortunately, the current ATM physical layer standard (UTOPIA) favors a simple interface card design



5. The figure shows a block diagram of a six-channel, 25 Mbit/s ATM line card with simple physical interface devices.

that does not support either multicast-ing or priority queuing.

There are many ways to provide support for multicasting in both single- and multi-PHY UTOPIA. The key is to transmit the data with the multicast information, i.e. which channels will receive the cell. Two methods are presented here. The direct method uses an inband multiport indicator (Fig. 2). Each bit location is associated with a port. For example, the presence of a 1 in any bit of the 6-bit multiport indicator indicates that the corresponding port is selected. The inband multicast indicator can be carried any-

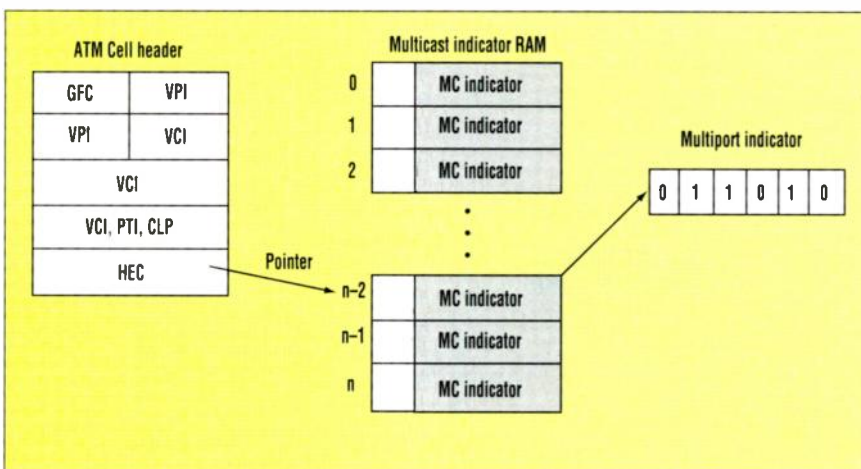
where in the ATM cell header. Figure 3 shows an example of using the HEC byte to carry the multicast indicator.

Another method of transmitting multicast information uses indirect addressing. The inband multiport code is used as an index to an internal RAM table that stores the actual multiport indicator (Fig. 4.) This method allows multiple communication sessions simultaneously.

To ensure that cells containing voice or video information are not delayed by less urgent messages, priority queuing is necessary. Usually four queues per port are enough to support CBR, VBR, ABR, and UBR traffic.

One way of providing priority in UTOPIA is to encode the priority in-band. Priority can be carried in any two bits within user-selectable locations in the ATM header. For these two priority bits, 00 might represent the highest priority, while 11 represents the lowest priority. Cells in the highest priority queue are sent as output first until the queue is empty, before a cell from the second priority queue is sent, and so on for all four queues.

A major challenge in communications system design is accommodating continuous changes in customer needs. One such need is the 25 Mbit/s ATM interface to the desktop. To add a 25 Mbit/s interface capability to an ATM switch node, the engineer must decide how many lines terminate in an



4. An alternative to in-band multicast signaling is to embed a tag byte within the cell to carry a multicast index. While more complex, it is more flexible, and facilitates a wider range of addresses.

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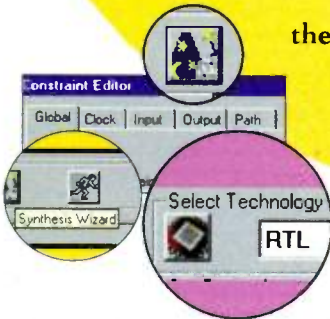
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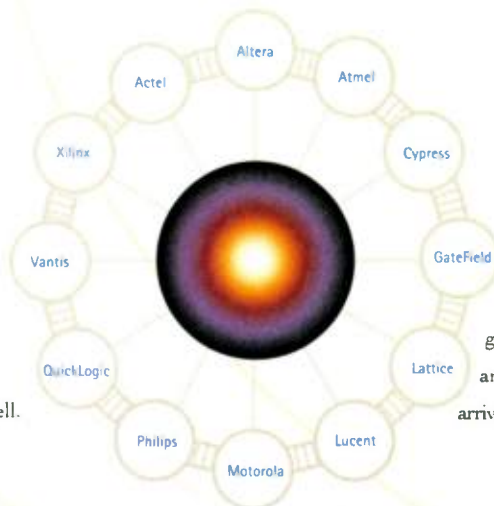
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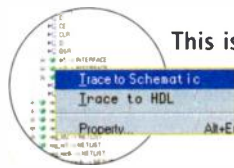
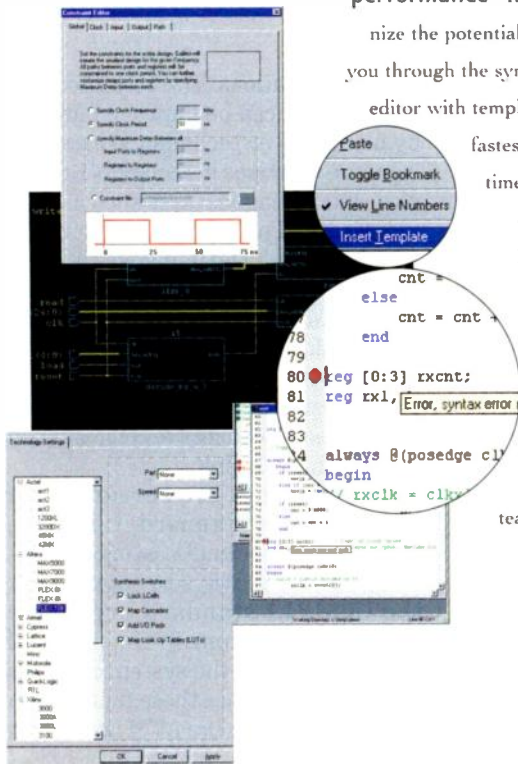
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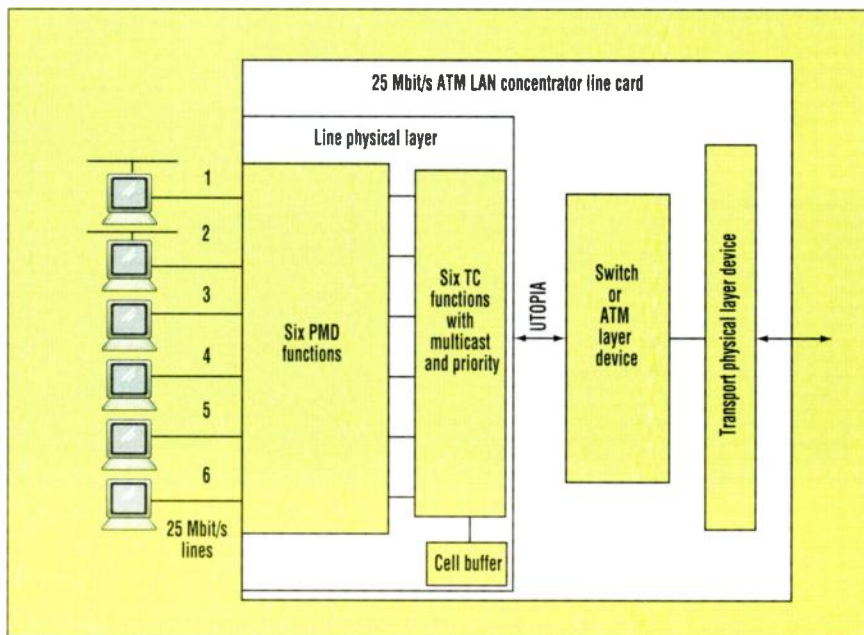
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6. Shown here is a block diagram of a six-channel, 25 Mbit/s ATM line card with multicasting and multipriority functions in the physical interface device.

interface card, which functions are necessary, and what level of loading is required for the switch fabric.

One of the most popular transport signals today is the OC-3 SONET/SDH signal. The OC-3 signal uses a 155.52 Mbit/s line rate that can carry a maximum ATM cell payload rate of 149.76 Mbit/s. The maximum ATM cell rate that can be carried in a 25 Mbit/s ATM signal is 25.126 Mbit/s. Six channels of 25 Mbit/s ATM signals would have a maximum cell rate of 150.75 Mbit/s, just 0.66% over the OC-3 maximum cell rate. Therefore, a six channel 25 Mbit/s ATM concentrator with some buffering is a logical and economical way to supply ATM to a community of users (Fig.5). This design uses simple line physical layer devices that provide the basic transmission-convergence (TC) sublayer and physical-media-dependent (PMD) sublayer functions.

Figure 6 shows another example of an ATM concentrator where the multicasting and priority capabilities are added to the physical-layer device. TranSwitch has successfully implemented a 208 pin PQFP VLSI device, SALI-25C, to provide the transmission convergence sublayer function, with up to 4000-cell buffering, multicasting, and multipriority for use in this type of concentrator.

Due to its built-in QoS capabilities, ATM is an ideal technology for multi-

media applications. The cost effectiveness of ATM can be improved further by using newer technology, integrating more functions in a single VLSI device, and adding features such as multicasting and priority queueing in the ATM network. The implementation of the multicasting and priority functions in an ATM switch node requires careful consideration of the switch node's internal architecture, the minimum transmission delay requirement, and the desired probability of congestion in the transmission link.

Even though the current ATM physical-layer standard, UTOPIA, lacks support for multicasting and priority, there are ways to supplement the UTOPIA standard to provide these two functions in the physical layer. This allows the system designer the freedom to place these functions in the physical layer, the ATM layer, or in the switch fabric.

Joseph Lau is vice president of Engineering at Loop Telecommunication International Inc., Hsinchu, Taiwan. Previously, Lau has been manager of Systems Engineering at TranSwitch Corp. Lau holds a BSEE from Case Western Reserve University, Cleveland, Ohio, and a Masters in Engineering (general degree) from the University of Florida, Gainesville. He can be reached at: +011-886-3-578-7696; fax +011-886-3-578-7695; e-mail: lau@loop.com.tw.

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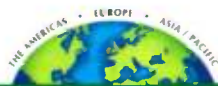
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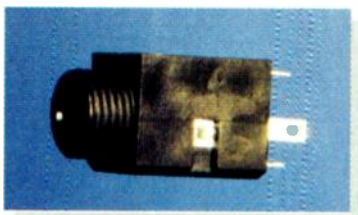
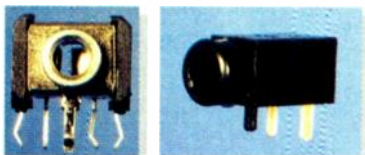
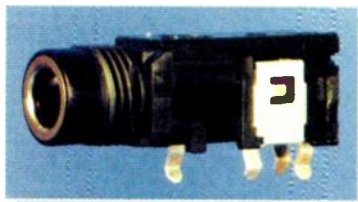
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MEETINGS

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International Conference on Consumer Electronics (ICCE), June 2-4. Los Angeles Airport Marriott, Los Angeles, California. Contact Diane Williams, Conference Coordinator, 67 Raspberry Patch Dr., Rochester, NY 14612-2868; (716) 392-3862; fax (716) 392-4397, e-mail: d.williams@ieee.org; www.icce.org.

IEEE International Conference on Communications (ICC '98), June 7-11. Atlanta, Georgia. Contact Debra Jordan, general secretary; fax (404) 881-6057; e-mail: icc98@comsoc.org; www.comsoc.org/conf/icc/98.

IEEE/MTT-S International Microwave Symposium (MTT 98), June 7-12. Baltimore Convention Center, Baltimore, MD. Contact Steven Stitzer, Westinghouse Electric Corp., P.O. Box 1521, MS 3T15, Baltimore, Maryland 21203; (410) 765-7348; fax (410) 993-7747.

USENIX 1998 Technical Conference, June 13-17. Marriott Hotel, New Orleans, LA. Contact USENIX Conference Office, 22672 Lambert St., Suite 613, Lake Forest, CA 92630; (714) 588-8649; (714) 588-9706; e-mail: conference@usenix.org; www.usenix.org.

35th Design Automation Conference, June 15-19. Moscone Center, San Francisco, CA. Contact MP Associates, 5305 Spine Rd., Suite A, Boulder, CO 80301; (303) 530-4333; e-mail: dacinfo@dac.com; www.dac.com.

Exhibition & Conference on System Integration in Microelectronics, June 16-18. Nuremberg Exhibition Centre. Call +49 711-61946-26/-74; fax +49 711-61946-93; www.mesago.de

JULY

IEEE International Geoscience & Remote Sensing Symposium (IGARSS '98), July 6-10. Sheraton Seattle, WA. Contact Tammy I. Stein, IGARSS Business Office, 2610 Lakeway Dr., Seabrook, TX 77586-1587, (281) 291-9222; fax (281) 291-9224; e-mail: tstein@phoenix.net.

IEEE Power Engineering Society Summer Meeting, July 12-16. Sheraton San Diego Hotel & Marina, San Diego, CA. Contact Terry Snow, San Diego Gas &

Electric, P.O. Box 1831, San Diego, CA 92112; (619) 696-2780; fax (619) 699-5096; e-mail: t.snow@ieee.org.

SPIE's Annual Meeting & Optical Instrumentation Show, July 19-24. San Diego, CA. Contact SPIE Exhibits Dept., P.O. Box 10, Bellingham, WA 98227-0010; (360) 676-3290; fax (360) 647-1445; e-mail: exhibits@spie.org.

IEEE Nuclear & Space Radiation Effects Conference (NSREC '98), July 20-24. Newport Beach, CA. Contact Jim Schwank, Sandia National Laboratories, P.O. Box 5800, MS-1083, Albuquerque, NM 87185-1083; (505) 844-8376; fax (505) 844-2991; e-mail: schwanjr@sandia.gov.

AUGUST

AUTOTESTCON '98, August 24-27. Salt Palace Convention Center, Salt Lake City, Utah. Contact Robert Myers, Myers/Smith Inc., 3685 Motor Ave., Suite 240, Los Angeles, California 90034; (310) 287-1463; fax (310) 287-1851; e-mail: bob.myers@ieee.org.

SEPTEMBER

Embedded Systems Conference Europe, September 7-9. Royal Ascot, England. Contact Michelle Troop, Miller Freeman Inc., (415) 278-5229; mtroop@mfi.com.

Sixth European Congress on Intelligent Techniques & Soft Computing (EUFIT '98), September 7-10. Aachen, Germany. Contact Conference Secretariat: EUFIT '98, Promenade 9, D-52076 Aachen, Germany; +49 2408-6969; fax +49 2408-94582; e-mail: eufit@mitgmbh.de; www.mitgmbh.de/elite/eufit.html.

ICSPAT & DSP World Expo, Sept. 13-16. Toronto Metro Convention Center, Toronto, Ontario, Canada. Contact Liz Austin, Miller Freeman Inc., (888) 239-5563, (415) 538-3848, e-mail: dspworld@mfi.com; www.dsp-world.com.

WESCON '98, Sept. 15-17. Anaheim Convention Center, Anaheim, CA. Contact Electronic Conventions Management, (800) 877-2668; (310) 215-3976; fax (310) 641-5117; e-mail: wescon.ieee.org; www.wescom.com.

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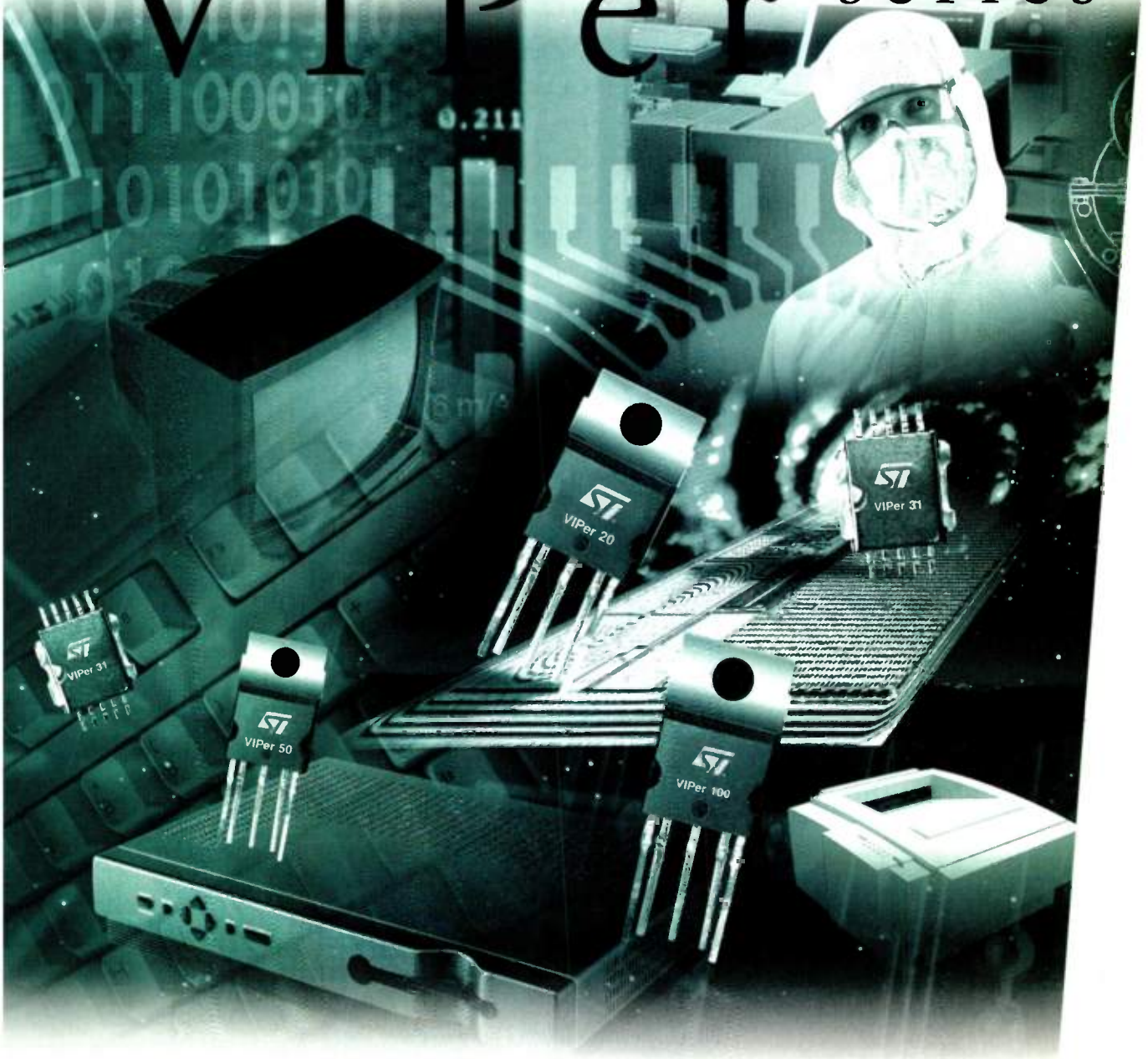
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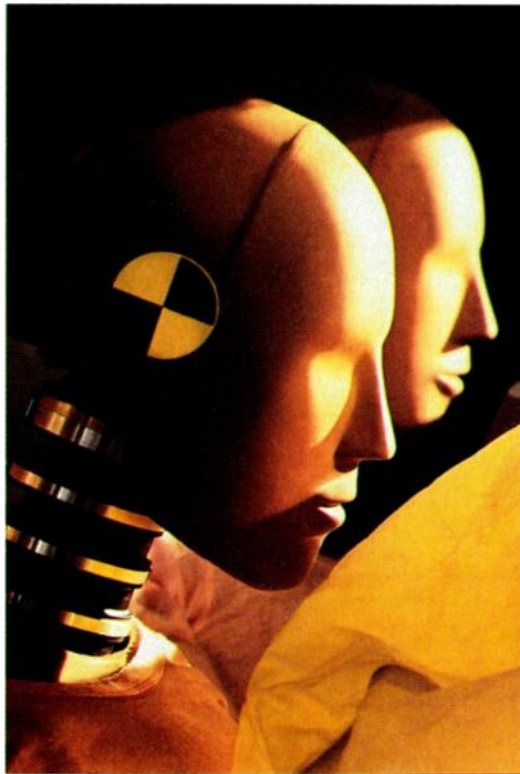
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ELECTRONIC DESIGN QUICK LOOK

■ Edited by Debra Schiff

MARKET FACTS

Putting Users On Buses

Every company promoting products that interface with "open" device/sensor buses such as ASI, DeviceNet, Interbus-S, LonWorks, Profibus-DP, SDS, and Seriplex should be thinking about how to put their end users on buses. Instead, though, they've chosen to spend their time shooting barbs at one another, attacking the real, or perceived, weaknesses of the competitive buses. The result

has been confusion among potential users, slowing industrial acceptance of control networks that use open-bus technology. To ensure the long-term success of bus technology in these applications, bus proponents need to refocus their efforts on growing the overall market, instead of on ineffective mudslinging tactics. A new study from Venture Development Corporation (VDC), "The U.S. Market for Industrial Automation Products Incorporating Device/Sensor Buses; ASI, CAN (DeviceNet, SDS), Interbus-S, LonWorks, Profibus-DP, and Seriplex, Second Edition," discovered that, although the usage level of open buses has increased dramatically since the 1995 study, the overall level of these device/sensor buses in the U.S. industrial control market is still low. In

its latest report, VDC estimated a potential market in the U.S. for connection of over 23 million devices (such as sensors, actuators, and controllers). However, VDC discovered that there are only an estimated 1.8 million devices so connected, representing a penetration level of under 8%. These 1.8 million devices are interfaced through an estimated 537,000 new device/sensor bus nodes, of which Lon-

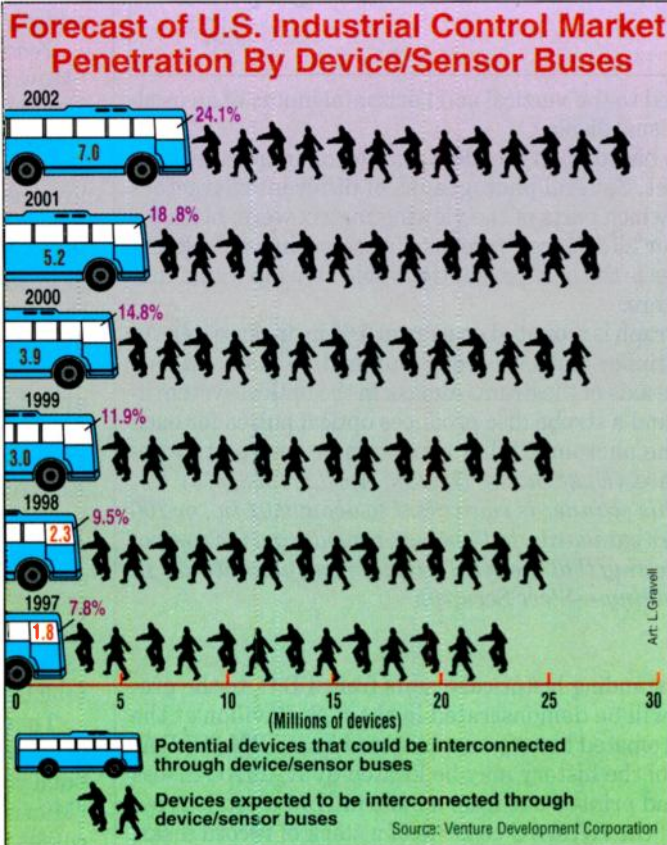
Works and DeviceNet accounted for 58%. The study forecasts that in the year 2002, despite an expected growth rate of about 38%, in new interfacing of devices to these buses, less than one-fourth of the potential market of 29 million devices will be tapped. These are expected to then be attached through 2.7 million nodes. While the various players fight it out, end users and machinery OEMs are waiting on the sidelines for the dust to settle before they choose to go the bus route. The real competition for these device/sensor

buses is the continuing use of conventional hard wiring, and to some extent other proprietary buses. Other open networks such as Ethernet and Fieldbus also pose some threat. Thus, device/sensor bus proponents should be focusing on increasing usage levels by such means as AIDA in the hopes of growing the overall pie. AIDA involves increasing user Awareness of device/sensor buses, generating greater Interest in device/sensor buses by users, generating greater Desire on the part of users to utilize these device/sensor buses, and getting users to take Action—to apply these buses in their applications.

In short, device/sensor bus proponents should be focusing more on increasing the overall levels of penetration for these buses. It is a lot more logical to fight over a piece of a much bigger pie

than it is to slash one's on throat for a mere crumb.

J. Timothy Shea is a project manager/industry analyst for VDC. He holds a BS in marketing from Bentley College, Waltham, MA and an MBA from the F. W. Olin Babson Graduate School of Business, Wellesley, MA. He can be reached at (508) 653-9000, ext. 132 or via e-mail: tshea@vdc-corp.com.



40 YEARS AGO IN ELECTRONIC DESIGN

Processing Pictorial Information On Digital Computers

Experiments involving general-purpose digital computers to help understand the nature of pictorial information are being conducted by the National Bureau of Standards. To feed pictorial information to the Bureau's Electronic Computer (SEAC), a simple mechanical drum scanning device digitizes the information as shown in the figure. Through associated scanner circuitry, a dark square on the picture is converted into a binary 1. A sufficiently white square produces a binary 0.

To display a picture, a program derives a pair of coordinate numbers for the position of each binary 1 in the picture stored in the memory. When decoded, the numbers produce a pair of

analog voltages that are applied to the vertical and horizontal inputs of an oscilloscope, thus generating the visual display.

A routine has been written based upon the identification of unique areas for each character of the alphabet. Several photographs of different characters were compared to determine which parts of the viewing matrix were: black for all letters concerned, white for all letters concerned, or sometimes black and sometimes white. This last area is the only part of the whole viewing frame that can be used to identify characters.

On the machine, the photograph is mounted on a drum 0.66 in. in diameter. As the drum rotates, a photomultiplier and a source of illumination mounted on a lead screw move parallel to the axis of the drum. A mask in the optical system illuminates a 0.25-mm square, and a strobe disc produces optical pulses for each 0.25 mm of drum rotation. The photomultiplier can examine the relative reflectance of each 0.25-mm square. (*ELECTRONIC DESIGN*, April 2, 1958, p. 5)

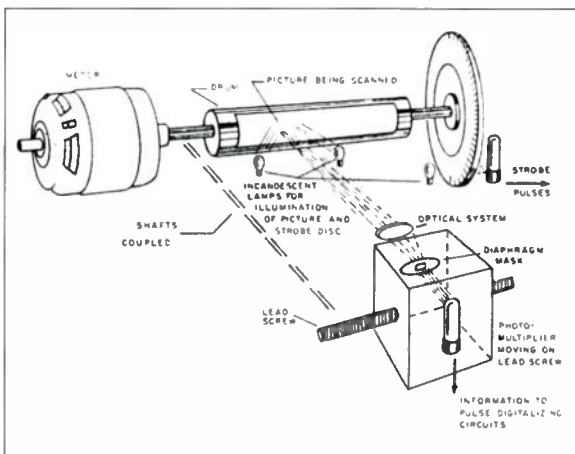
The 0.25-mm spot size in this scanner is equivalent to about 0.01 in., or 100 dots per inch—not up to today's standards, but not bad, considering the components it's using. It's also interesting that the NBS quickly recognized its use in OCR as well as in picture scanning.—Steve Scrupski

The Currents Of Time

An electronic review of outstanding historical events from 4 B.C. to the present in any of ten languages will be demonstrated in the U.S. Pavilion at the Brussels World's Fair. The automated history text is stored in an IBM 305 RAMAC computer. Any portion of the history may be located by RAMAC in less than two-thirds of a second and printed out from a built-in IBM electric typewriter. The memory section of the RAMAC consists of a stack of record disks, which revolve on a vertical shaft at 1200 rpm. An electronically controlled arm moves to any location of the records to recover the historical information, which is stored on the records as magnetized spots. The unit contains up to five million alpha-numeric characters. (*ELECTRONIC DESIGN*, April 16, 1958, p. 8)

The IBM 305 RAMAC, introduced in 1956, incorporated the industry's first hard-disk drive. It used 50 24-in. disks for its 5-Mbyte capacity.—Steve Scrupski

Steve Scrupski is a former Editor-in-Chief of ELECTRONIC DESIGN. Now semiretired, he can be reached at scrupski@worldnet.att.net.



Y2K UPDATE

Here we are, less than two years away from the turn of the century, and most companies have yet to address their Year 2000 (Y2K) compliance issues. Perhaps they're frozen by fear. Perhaps they've been hiding under a rock for the last year or so, while the mass media has been proclaiming the oncoming disaster. In any case, if they just read the *Year/2000 Journal*, they'll have a clue as to what to do.

This magazine, in its second year of publication, has become much thicker. It's not just the advertisements, though, it's the information within. For example, there's an article that talks about the conflicts facing the Euro currency conversion that takes place between Jan. 1, 1999 and Jan. 1, 2002. The issue is that there won't be enough resources to address both issues at the same time.

Year/2000 Journal also looks at "How Much Testing Is Enough?" The idea behind that article is that if a company does not understand the scale and complexities of the testing involved in compliance, there will be failures in testing. What I like about this publication is that it presents solutions. This article talks about what the current best practices are in testing, and how to prevent failures.

Also, information professionals and those on the Y2K compliance team should check out "A Minimal Risk Year/2000 Strategy for EDI." Electronic data interchange (EDI) is based upon the sharing of data between companies, and can pose quite a complication in terms of Y2K compliance efforts. Here, though, the author, Michael Gerner presents "Seven Steps to a Safe and Successful EDI Interface."

There are many other articles of great importance in the publication, but if you read nothing else, check out "Microsoft and Year/2000." It discusses the company's compliance (or lack thereof) and how to deal with it.

For subscription or other information, contact *Year/2000 Journal*, 9550 Skillman St., Suite 105, Dallas, TX 75243; (214) 340-2147; fax (214) 341-7081; e-mail: y2kjournal@connect.net, www.y2kjournal.com.—DS

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Waiting For Specialists

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Obviously, such dazzling skill should make it possible for us to develop our products faster. Less obviously, it often does not. Specialists in our development process can actually be a source of devastating delays. Let's examine why.

Sam is our only EMI expert, and every program uses him. He supports 20 projects at the same time. The critical project gets all the attention while the other 19 projects wait. A manufacturing engineer would say that this is a process with 95% queue time and 5% run time.

Such queue time has staggering consequences for our development cycle. It means, for example, that without special interventions to get two hours of work done, we will have to wait 38 hours in queue. The elapsed time is 20 times actual work time.

In projects with a high cost-of-delay, the cost of these queues can be devastating. Consider a project with a cost-of-delay of \$100,000 per month. Forty hours of delay are worth \$25,000 dollars. Two hours of work may cost \$200. The delay associated with the specialist costs 125 times its expense. Thus, the key measure of specialist performance is delay not expense.

Unfortunately, the delay time is



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not what most companies measure. They focus on specialist efficiency. They design their development processes to maximize the efficiency of their specialists, believing that this will optimize the overall efficiency of product development.

For example, consider what happens when we focus on the efficiency of our UL (Underwriter's

Laboratories) approval experts. We pressure them to be as efficient as possible, and they respond by trying to minimize the time they invest in each project. They look at projects late in the development process, when there is little chance that the design will change. The consequences are that they identify changes at a stage when the cost of change is 100 times higher than it would have been just a few months before. The specialist is now on the critical path where he or she needn't be. The bottom line is that changes this far down the line cost us *many times* any savings we could get by improving specialist efficiency.

At a deeper level, the specialists aren't the ones causing our problems. The real cause is that we combine fragmentation of work with high levels of utilization. Imagine that we had Sam drinking coffee half of the time. Half of the time, a new job would find him ready to go to work immediately. The rest of the time we would find him busy, but it would take him an hour to finish that work. This means that his processing time would always be less than four hours. The total cost of his activity would drop from \$25,200 to less than \$3,000, an eightfold improvement.

Specialists who are loaded to the right level of utilization will not cause queues. Essentially, we measure specialists the wrong way. We should be measuring their response time, not their efficiency. This will prevent us from waiting for specialists.

Don Reinertsen is president of Reinertsen & Associates, a consulting firm specializing in product development management. He can be reached at (310) 373-5332 or e-mail: DonReinertsen@compuserve.com.

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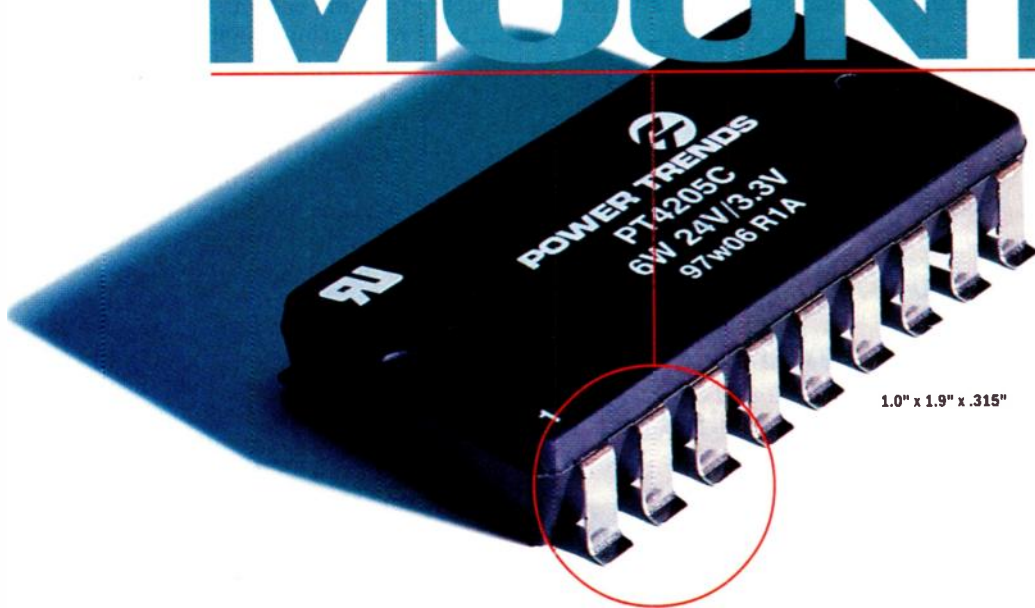
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6W	5V	1.2A	PT4206	PT4203
6W	12V	0.6A	—	PT4204
7W	+5V / -5V	1A ea	—	PT4301
7W	+5V / +3.3V	1A ea	—	PT4302
15W	3.3V	4.5A	—	PT4110
15W	5V	3A	PT4104	PT4101
15W	12V	1.2A	PT4105	PT4102
15W	15V	1A	PT4106	PT4103



POWER TRENDS

FLIPPING THROUGH THE INTERNET ROLODEX

www.bdti.com: When you drop by Berkeley Design Technology's site you'll find a newly available set of DSP processor overviews. They're reference guides for DSP engineers and designers who need to compare the basic architectural features of today's popular DSPs. Included in each overview are the data path, memory

architecture, peripheral, history, and predecessor information for each processor. New DSPs are covered, such as TI's TMS320C62xx, and Lucent Technology's DSP16xxx. The very popular Intel MMX Pentium and PowerPC 604e also can be found at the site. Links to other DSP resources, FAQs, and DSP benchmark

performance information (BDTI-mark) are featured at the site as well.

www.imaging.com: This new web site from Imaging Technology focuses on news in automated imaging and machine vision; tutorials on vision, robotics, and scientific imaging; and case histories in industrial inspection, machine guidance, and defense-related applications. The site splits off into 10 different sections: About ITI, Site Map, Product Tour, Online Store, Online Resources, Imaging News, Tutorials, Technical Support, Employment, and Partners Corner. Also at the site is "The Images Report," a quarterly publication dedicated to best practices in machine vision and automated imaging. Featured products at the site include the Prophecy 600 high-speed machine vision system; the IC-PCI family of high-speed, half-slot PCI-bus frame grabbers; and the MVC 150/40 family of high-performance VMEbus and PCI-bus pipeline processors.

www.cdw.com: Stop by Computer Discount Warehouse's site to check out the now almost 26,000 products available. Visitors to the site can search and order items here. There are over 6,500 items that have detailed specifications online. Anyone even thinking about purchasing a new PC or related product should stop by just to see the kind of information offered here. There are continually updated prices and availability, side-by-side comparisons, and order status features that make the site a handy addition to a bookmark file.

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AK4540	16	2 2	AC'97 Compliant Codec for PC applications
AK5392	24	2 -	116dB 24-bit ADC using only 500 mW
AK7712A	20	2 4	Integrated codec with fully programmable on-chip DSP

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INTERNET NEWS

If you're a web site builder (or play one on TV), your next stop on the World Wide Web should be Rhizome Internet L.L.C.'s StockObjects site. Clip art CD-ROMs are all well and good, but how new and how fresh are the images? How clean and legible are they? And, do they move? Those questions are important, especially since the pace of site visits is speeding up—and you don't want your client's site to be passed over on the way to somewhere else.

The best thing about the StockObjects site is that it's crammed full of fun things that you can use to make your site appetizing to anyone who visits. There are GIF animations, 3D models, images, Java applets, QTVR, and Shockwave animations. The company plans to have Flash animations in the near future.

StockObjects functions as a reseller of these computer-generated and film-transferred images. They pay a royalty to the new media developer based on the number of objects licensed for use by clients. Whenever anyone purchases an object, a perpetual license for digital use and related packaging is included with the purchase. The result is the elimination of the license negotiation process.

Just to see what all the hubbub was about, I visited the site. I looked for an animation with food as the subject that also involved a character. What came up were 16 relatively silly images. They all cost \$75 for nonsubscribers and \$37.50 for subscribers. My personal favorite was the "man stuffing his face with pie." Mind you, there are many serious images that convey a solid message, but I prefer the fun ones.

There's a gallery at the site for a quick showcasing of the types of graphics available at StockObjects. I checked them all out, but the Shockwave files, especially the "Mad Scientist," made me laugh out loud. Now, if you can get visitors to your site to keep coming back or even refer the site to someone else, based on even one silly graphic, that addresses your advertisers' questions about clicks.

The site does offer the option of becoming a supplier, which allows

the web developer to show his or her wares to a much larger, international audience than they would have otherwise. Additionally, the developer can submit work to the StockObject library without having to bargain with the reseller about the royalties. The audience is typically made up of multimedia developers, on-line com-

munities, content companies, advertising agencies, other web developers, and corporate site owners.

Even if you're not in the market for new digital objects, the site is definitely worth a look: <http://www.stockobjects.com>. Or call Jeff Phillips at (212) 406-8710, ext. 106 for more information.—DS

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READER SERVICE 126

I'm impressed. I guess I should get that out of the way at the beginning. *Today's Engineer*, published by IEEE-USA, is a brand-new, quarterly magazine that is intended to teach engineers to think about their careers in a different way. And, I read the thing cover to cover.

The focus here isn't on technical

competence. The publication assumes that if you've gotten to where you are in your career, you obviously have technical talent. Where it goes is the wider view: Do you have a business perspective? How can you advance your career effectively? Are you changing with the times? How do we change the public's view of the engineer? All of these ques-

tions encourage the engineer to, as editor-in-chief Gus Gaynor puts it, "think strategically, and develop a global business perspective."

Today's Engineer starts off with a few smaller pieces in the section called Short Circuit. Topics in this section include team dynamics, practical education, society's effect on technology, how not to treat a buyer, and fostering innovation.


Additionally, there is a News Makers column that turns its eyes to Donna Shirley. Shirley manages the Mars Exploration Program at the Jet Propulsion Laboratory, Pasadena, Calif. What's interesting about the piece is that although it does go into her experience as one of the few women in the field in the 1960s, it doesn't focus only on her gender. What Shirley did to achieve her position, the lengths that she went to in order to rise to be a leader of such an historic project, and the different directions she took are what kept me reading the story.

Other columns include Engineering Trends, Technology Policy, and Management Briefs. I made a copy of the "Get on Your Feet and More," piece by Mike Aucoin for our Editor-in-Chief, Tom Halligan. Aucoin examines different ways of holding meetings, including standing up. According to Aucoin, one of the generals held stand-up meetings during the Gulf War to keep his staff focused and the meetings fast paced.

The remainder of the magazine comprises the longer articles, "The Dawning of a New Age—Crossroads of the Engineering Profession," "Our Changing Work Environment—From the Bullpen to the Cubicle to the Virtual Office," "Project Scope Creep: Making Widgets Without Wedgies," "Great Expectations—Gen-X Engineers Speak Out," "Communication in the Profession: It's Not Eighth-Grade English," "Who Are We? How Different Are Men and Women Engineers?" and "Building on a Product Platform—Out with the Old, In with the New."

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3.3	1.5	-	-	20 IMX 7-03-7	40 IMX 7-03-7	70 IMX 7-03-7
5.1	1.2	-	-	20 IMX 7-05-7	40 IMX 7-05-7	70 IMX 7-05-7
5	0.6	5	0.6	20 IMX 7-05-05-7	40 IMX 7-05-05-7	70 IMX 7-05-05-7
12	0.25	12	0.25	20 IMX 7-12-12-7	40 IMX 7-12-12-7	70 IMX 7-12-12-7
15	0.2	15	0.2	20 IMX 7-15-15-7	40 IMX 7-15-15-7	70 IMX 7-15-15-7
24	0.13	24	0.13	20 IMX 7-24-24-7	40 IMX 7-24-24-7	70 IMX 7-24-24-7

Output 1		Output 2 Input		4 Watts		
V _o nom (V DC)	I _o nom (mA)	V _o nom (V DC)	I _o nom (mA)	V _i min...V _i max 8.4...36 V DC	Voltage Range V _i min...V _i max 16.8...75 V DC	
3.3	900	-	-	20 IMX 4-03-7	40 IMX 4-03-7	
5.0	700	-	-	20 IMX 4-05-7	40 IMX 4-05-7	
12	340	-	-	20 IMX 4-12-7	40 IMX 4-12-7	
15	280	-	-	20 IMX 4-15-7	40 IMX 4-15-7	
+5	+350	-5	-350	20 IMX 4-10505-7	40 IMX 4-0505-7	
+12	+170	-12	-170	20 IMX 4-1212-7	40 IMX 4-1212-7	
+15	+140	-15	-140	20 IMX 4-1515-7	40 IMX 4-1515-7	
+24	+90	-24	-90	20 IMX 4-2424-7	40 IMX 4-2424-7	

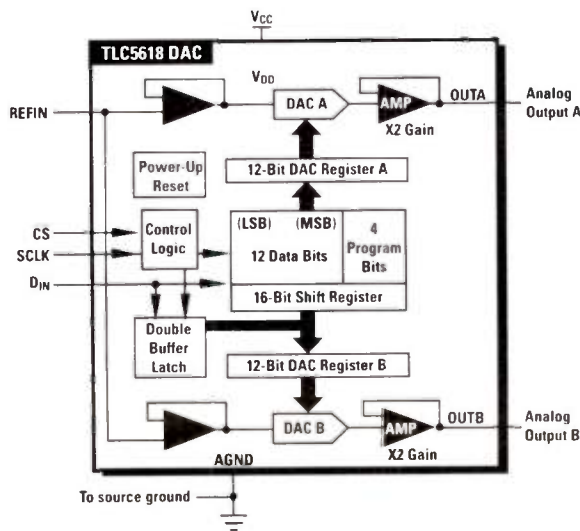
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ANALOG OUTLOOK

■ Exploring the world of analog, mixed-signal and power developments

Commodity DACs Wring More Performance From Smaller Packages

As Designers Seek Better Accuracy From Tinier Dies, Suppliers Tap Segmented Current Sources Or Resistor-String Architectures.

Ashok Bindra

The increasing trend toward digital trimming, control, and signal processing, is forcing engineers to adopt optimized, low-cost, high-resolution, digital-to-analog converters (DACs). These DACs are undergoing rapid changes as designers seek single-supply operation, lower power consumption, better resolution, greater dynamic range, and, above all, smaller packages without any price premium. These demands have resulted in DAC price erosions, driving converters beyond 12-bit resolution to the commodity status. It's encouraged DAC implementers to migrate to designs that employ 14- and 16-bit devices. In some instances, even affordable and reliable 24-bit DAC ICs are emerging.

Commodity DACs are mimicking low-cost, analog-to-digital converters (ADCs) on the front end, attempting to deliver more functionality on-chip with better resolution and drive for an affordable price tag. To that end, mixed-signal IC suppliers are combining advances in process technologies with architectural enhancements and new algorithms to

SPECIAL REPORT

meet this increasing price-performance bar.

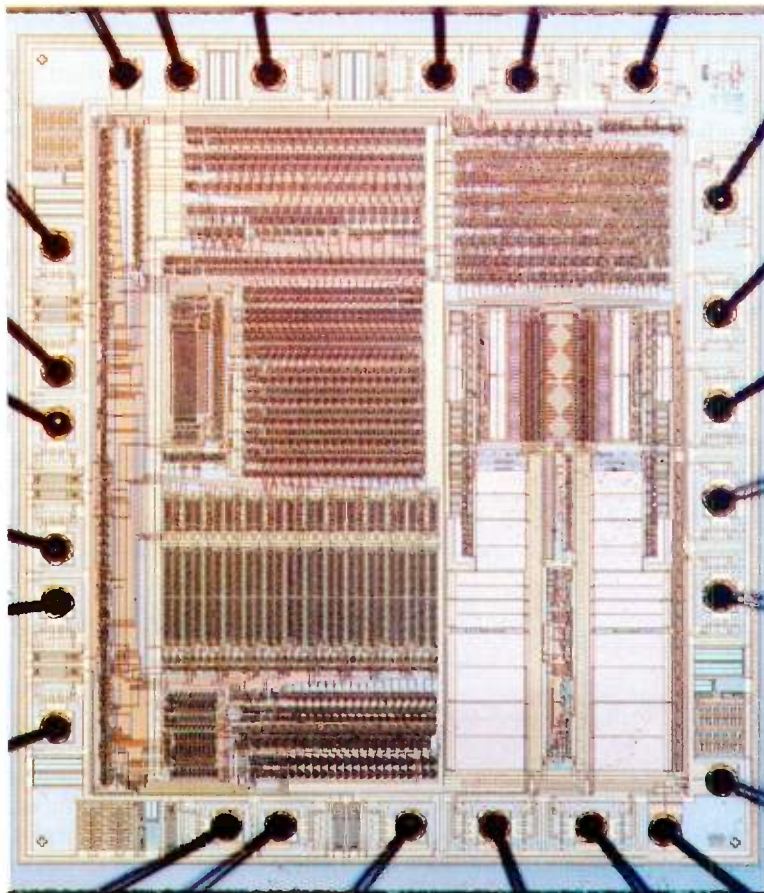
Many DAC IC manufacturers are combining advancements in CMOS with clever circuit techniques to tailor DACs with the right mix of speed, resolution, functions, peripherals, and package size for the target applications, while keeping cost

under control. For some others, though, using a biCMOS process is the answer.

Key proponents of using CMOS to make low-cost DACs are Harris Semiconductor, Analog Devices, Exar, Texas Instruments, and Maxim Integrated Products. These DAC makers are combining digital and linear attributes of CMOS to create a cost-effective, mixed-signal, data-conversion solution that addresses the user's system requirements. For audio applications, the Crystal Semiconductor Division of Cirrus Logic and AKM Semiconductor, the marketing arm of Japan's Asahi Kasei Microsystems, are combining CMOS' high-density capabilities with the performance of the D-S architecture

to create low-cost, high-resolution DACs.

The transition from bipolar to smaller CMOS



Art Courtesy: AKM Semiconductor Inc.

elements brings with it distortion and mismatched FET transistors. However, linearization of CMOS, coupled with innovative architectures, is helping DAC IC designers address this problem and create devices with improved levels of ac and dc characteristics, without hiking the cost.

Harris Semiconductor, for instance, has addressed this problem by employing segmented current-source arrays and current-steering pMOS FET switches instead of conventional R-2R resistance ladders. Besides improving differential and integral nonlinearities, the segmented current-source architecture also keeps glitch energy low, according to Harris Semiconductor's high-speed converter design engineer Bruce Tesch. For instance, notes Tesch, in a 10-bit design, five MSBs are segmented, and five LSBs are binary weighted to achieve a differential nonlinearity of less than one-half LSB. And, integral linearity error is within ± 1 LSB.

Migrating to a finer CMOS process has allowed Harris' designers to substantially increase the converter's speed. For example, the 10-bit HI5760 can perform 125 Msamples/s, consuming only 190 mW at 5 V and 45 mW at 3 V (Fig. 1). The HI5760 also offers excellent spurious free dynamic range

(SFDR) of 75 dB. Yet, despite this kind of performance, the HI5760 is priced at under \$10 each in 1000-piece lots. The 0.6- μ m CMOS process on which it is made also has enabled the manufacturer to pack dual high-speed 10-bit DACs in a 44-lead MQFP package. A dual-channel version, the HI5728, includes a common reference and clock, and is suited for digital modulation/demodulation in communication systems. Harris Semiconductor also is crafting a high speed 12-bit version, the HI5831 for release later in the year.

Segmented Current Sources

While Harris Semiconductor is betting on segmented current sources, Texas Instruments (TI) is going for a resistor string network in place of an R-2R resistance ladder to attain acceptable levels of differential and integral linearity. The resistor string is buffered with an op amp to convert digital data into analog voltages. Combining this approach with a high-speed, analog 0.8- μ m CMOS process lets TI pack multiple channels with high resolution and low power in miniaturized packages.

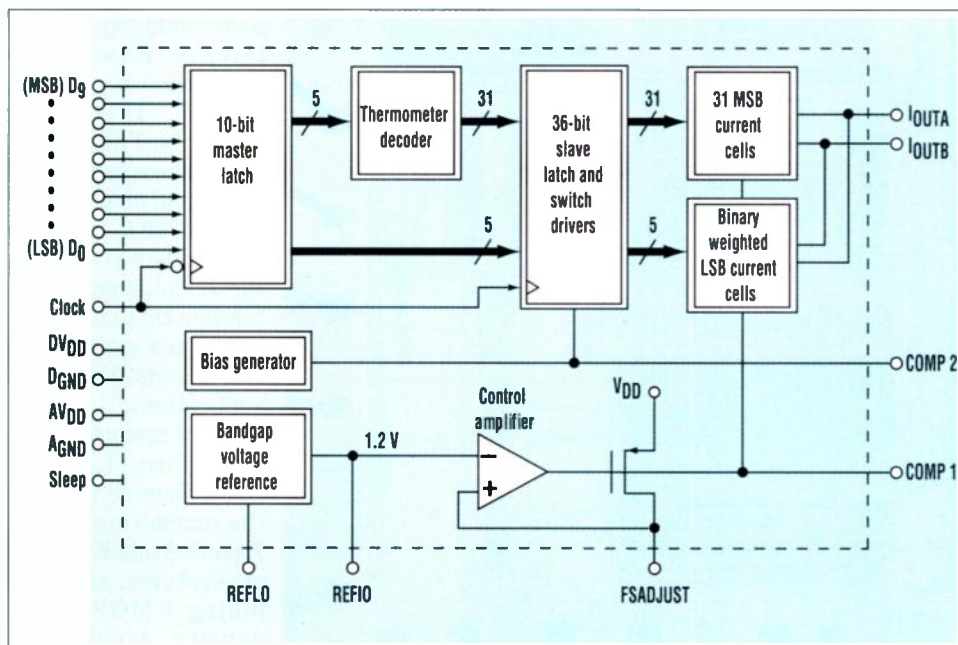
TI also has developed a programmable, dual, 12-bit voltage-output DAC that attains high speed and low

power from the same die, the TLC5618. For power-sensitive applications, TI's TLC5618 features programmable settling time versus power dissipation. In the fast mode, the TLC5618 has a settling time of 2.5 μ s, and dissipates 8 mW. In the slow mode, it dissipates 3 mW and settles in 12.5 μ s. A software-programmable power-down mode further reduces supply current to 1mA.

This flexibility is made possible by implementing a programmable-bias-current technique for the output amplifier. As a result, "the designer can trade off speed for power," explains Tom Lahutsky, new product development manager for TI's data converters. For instance, he adds, the user can optimize system performance versus power consumed as needed by the application. Plus, Lahutsky notes, the DAC uses resistor-string architecture to achieve well-matched resistors for a high degree of linearity. Maximum differential non-linearity for the TLC5618 is ± 1 LSB, and integral non-linearity is ± 4 LSB.

The TLC5618 employs a single supply pin that interfaces to both analog and digital circuits. This technique permits the engineer to utilize a cleaner analog supply for both circuits. "However, to get maximum performance from this device, the designer must implement a proper layout to ensure that the digital currents do not get back into the analog portion of the circuitry," asserts Lahutsky. Furthermore, he continues, the reference voltage input is buffered, thereby making the DAC input resistance code-independent. This feature makes it easier to design the reference generator circuitry, because the source impedance of the reference can be relatively high with low drive requirements, states Lahutsky.

TI continues to add more features to this part by integrating serial and parallel interfaces, thereby simplifying its link to DSPs and microcontrollers. One such model in the works is the TLC5618A with burst-mode serial ports for C2XX DSP family ICs. Other



1. Harris Semiconductor's HI5760 implements segmented current-source arrays instead of a conventional R-2R resistance ladder, to achieve a differential nonlinearity of ± 0.5 LSB, with an excellent spurious-free dynamic range (SFDR) of 75 dB. This 10-bit, 125-Msample/s DAC is fabricated in 0.6- μ m CMOS. It consumes 190 mW at 5 V supply, and 45 mW at 3 V.

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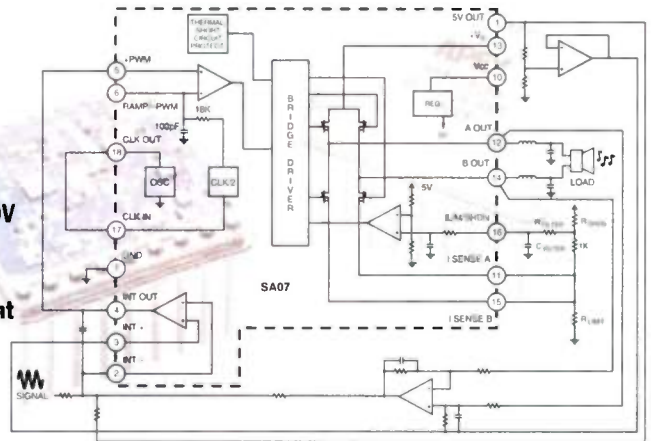
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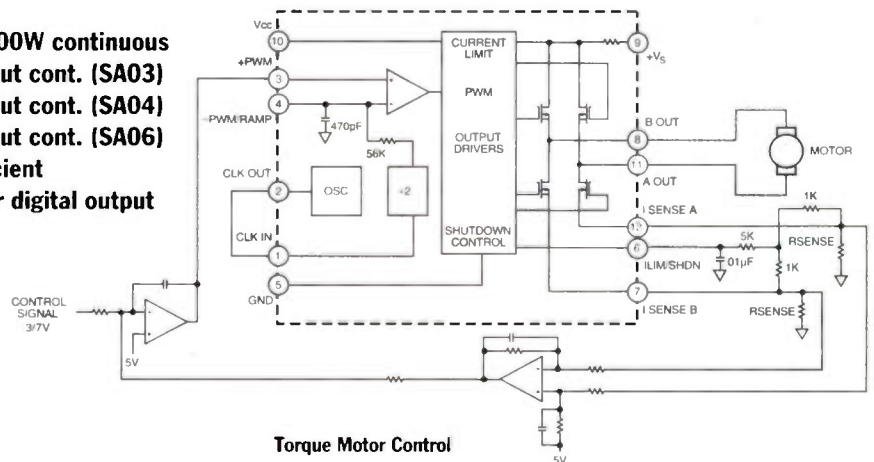


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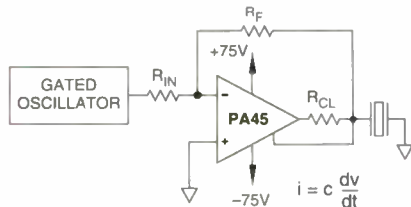
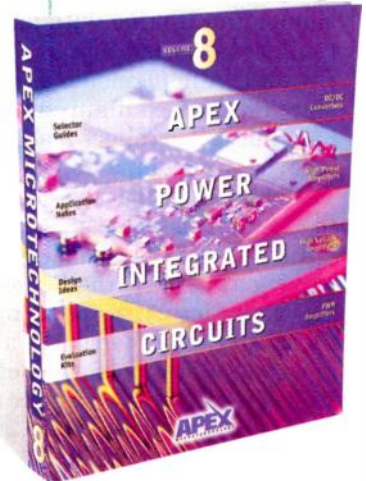
PWM Amplifiers Product Selector Guide

Model	Efficiency	I _{OUT} Cont.	Supply	Switching Frequency	Thermal Protection	Power Delivery	Full or Half Bridge
SA01	97%	20A	16V-100V	42kHz	Yes	2000W	Full
SA02	94%	10A	16V-80V	250kHz	Yes	800W	Full
SA03	97%	30A	16V-100V	22kHz	Yes	3000W	Full
SA04	97%	20A	16V-200V	22kHz	Yes	4000W	Full
SA06	97%	10A	16V-500V	22kHz	Yes	5000W	Full
SA07	94%	5A	5V-40V	500kHz	Yes	200W	Full
SA13	97%	30A	16V-100V	22kHz	Yes	3000W	Half
SA14	97%	20A	16V-200V	22kHz	Yes	4000W	Half
SA16	97%	10A	16V-500V	22kHz	Yes	5000W	Half
SA50	97%	5A	up to 80V	45kHz	No	400W	Full
SA51	97%	5A	up to 80V	external set	No	400W	Full

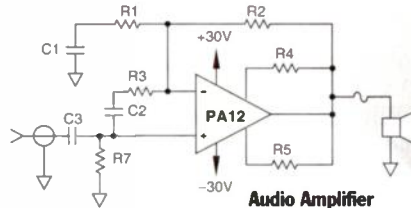
Applications 101: Power Amplifiers

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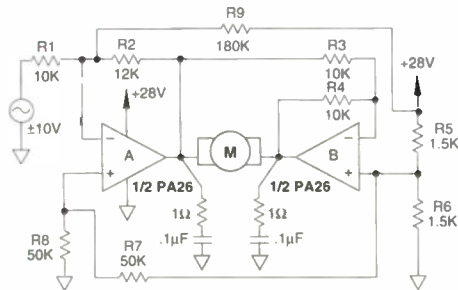
New Data Book Same Apex Quality



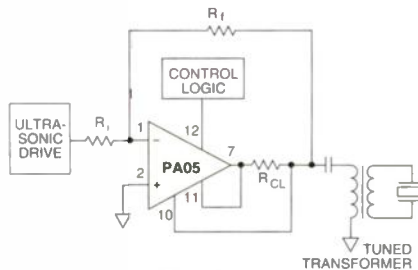
Simple Piezoelectric Transducer Drive



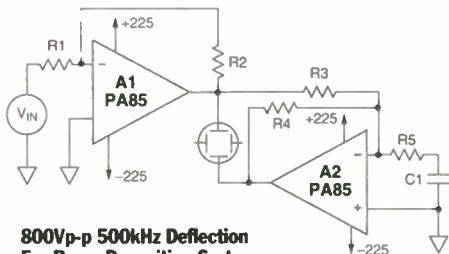
Audio Amplifier



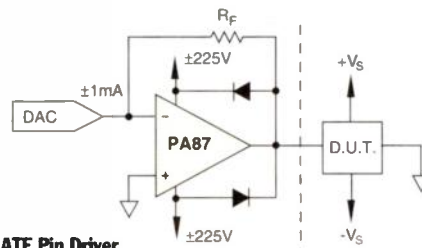
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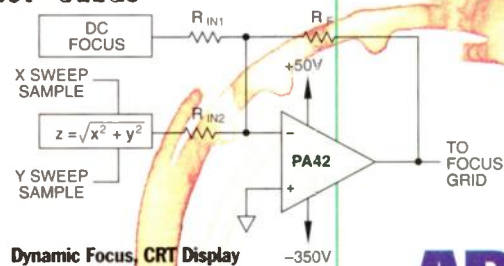
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High Voltage Amplifiers Product Selector Guide

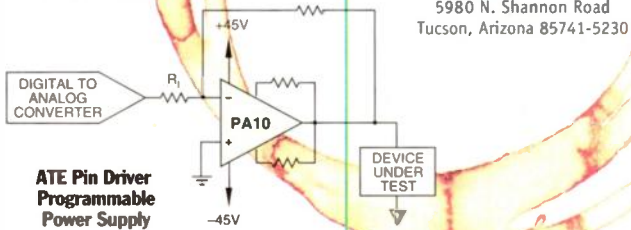
Model	Supply	I _{OUT} Peak	I _{STANDBY}	Slew Rate	Package
PA08	30V-300V	200mA	8.5mA	30V/ms	T0-3
PA41	100V-350V	120mA	2mA	40V/ms	T0-3
PA42	100V-350V	120mA	2mA	40V/ms	SIP
PA85	30V-450V	350mA	25mA	1000V/ms	T0-3
PA87	100V-450V	300mA	3.8mA	35V/μs	SIP
PA88	30V-450V	200mA	2mA	30V/μs	PowerDip
PA89	150V-1200V	100mA	6mA	16V/μs	PowerDip



Dynamic Focus, CRT Display

High Current Amplifiers Product Selector Guide

Model	Supply	I _{OUT} Peak	Slew Rate	Power Dissipation	Package
PA03	30V-150V	30A	8V/μs	500W	PowerDip
PA05	30V-100V	30A	100V/μs	250W	PowerDip
PA04	30V-200V	20A	50V/μs	200W	PowerDip
PA10	20V-90V	5A	3V/μs	67W	T0-3
PA12	20V-90V	10A	4/μs	125W	T0-3
PA26	5V-40V	2.5A x 2	1.2V/μs	25W	SIP
PA45	30V-150V	5A	27V/μs	85W	T0-3



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features include Serial Peripheral Interface (SPI) and queued SPI (QSPI) support for linking with microcontrollers. According to TI, the TLC5618A implements an internal state machine configured to handle both microcontrollers and DSPs. It also is pin compatible with the TLC5618. Available in an 8-pin SOIC, the TLC5618 is priced at \$4.20.

Like TI, Exar's engineers are also moving away from the R-2R ladder, and employing a resistor-string architecture for improvement in a DAC's linearity and dc performance. With the R-2R, the input resistance and capacitance varies with code, and this variation is greater than 20%. The resistor-string technique makes the input resistance independent of code, and dramatically reduces variation in capacitance with code, according to Hugh Wright, marketing manager for standard ADCs and DACs at Exar.

Using this approach, Exar has released a family of 8-, 10-, and 12-bit voltage-output DACs. The XRD5408/10/12 family is designed for digital calibration in applications such as instruments, battery-powered equipment, remote industrial devices,

cellular phones, and motion-control sensors.

Combining this architecture with a 0.6- μ m CMOS process allows Exar's engineers have cut power consumption to as low as 0.315 mW maximum at 5 V, while providing an output that can swing rail-to-rail. In fact, Exar engineers are planning to further improve this drive capability, as they see a rising demand for voltage-output, ultra-low-power DACs. The settling time for the XRD family is typically 13 ms to 12 bits. The smaller die size has enabled Exar to place this converter in 8-pin SOIC and plastic DIP packages. In 1000-piece quantities, the XRD5410 and XRD5412 are each priced at \$1.60 and \$1.92, respectively.

Miniature Packages

To deliver low-power DACs in miniaturized packages that are as small as those used in discrete-component designs, Analog Devices created a novel circuit on a 0.6- μ m CMOS process. It houses 8-bit (AD5300), 10-bit (AD5310), and 12-bit (AD5320) voltage-output DACs in ultra-small 6-pin SOT-23 packages. Consuming typically only 0.7 mW at 5 V, and 0.4 mW

at 3 V, they're designed to operate from a single 2.7- to 5.5-V supply.

An on-chip output amplifier allows the output of the AD5300 family DACs to swing rail-to-rail with less than 10 μ s of maximum settling time to 12 bits. In addition, maximum linearity performance for these converters is ± 0.25 LSB for the AD5300, ± 0.5 LSB for the AD5310, and ± 1 LSB for the AD5320. Analog Devices' product manager Leo McHugh says that the AD5300 series converters signal a new trend of providing performance and ultra-low power in ultra-small packages, at commodity prices. In 1000-piece quantities, for example, the AD5300, AD5310, and AD5320 are each priced at \$1.25, \$1.70, and \$2.50, respectively.

To achieve accuracy in a small area, the family employs a multiplying string architecture with buffered voltage output (*Fig. 2*). In this scheme, the main DAC comprises 64 resistors representing six MSBs, and a sub-DAC consisting of only 63 resistors for six LSBs. With a main DAC resistance of 40 k Ω , sub-DAC resistance of approximately 80 k Ω , and correctly sized coupling switches, the loading error is about 1 LSB.

To ensure that the devices power up to 0 V, and remain there until a valid write takes place, the AD 5300 family implements a power-on reset circuit. In fact, this feature is also being made available from other suppliers, as designers have realized that such devices tend to become unstable as soon the power is applied. However, each manufacturer is incorporating its own solution to alleviate this problem. Furthermore, to give the user a wide dynamic output range, the DAC's on-chip reference is derived from the power supply input. Because these converters have to interface with microcontrollers and DSPs, the AD5300 series incorporates a versatile, three-wire serial interface that is compatible with SPI, QSPI, and Microwire interface standards.

Multichannel Designs

Many designers are looking for multichannel solutions from a single package. To accomplish that, Analog Devices is readying a dual version of the AD5300 series with several additional features integrated on-chip.

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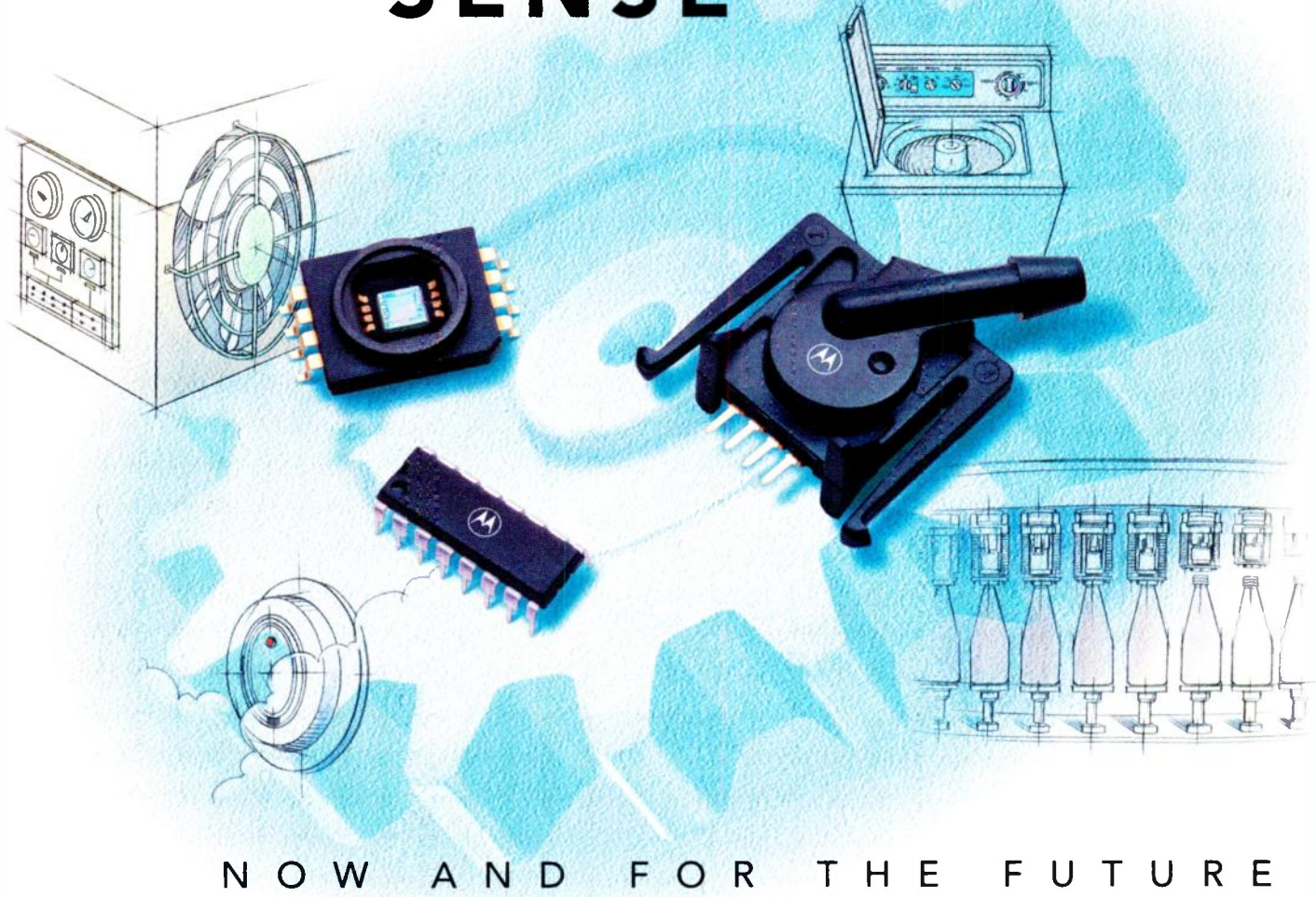
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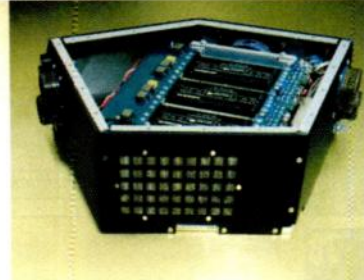
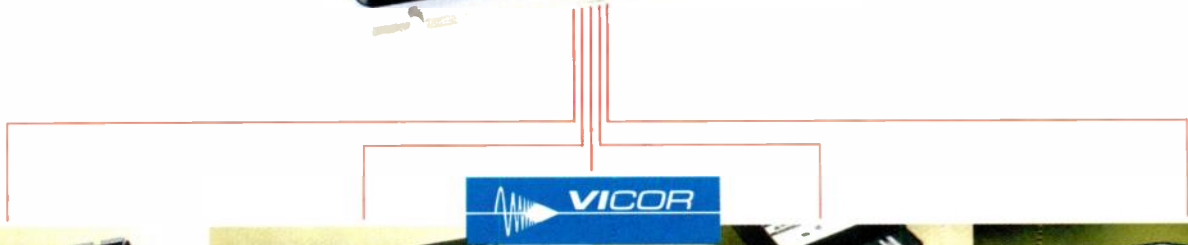
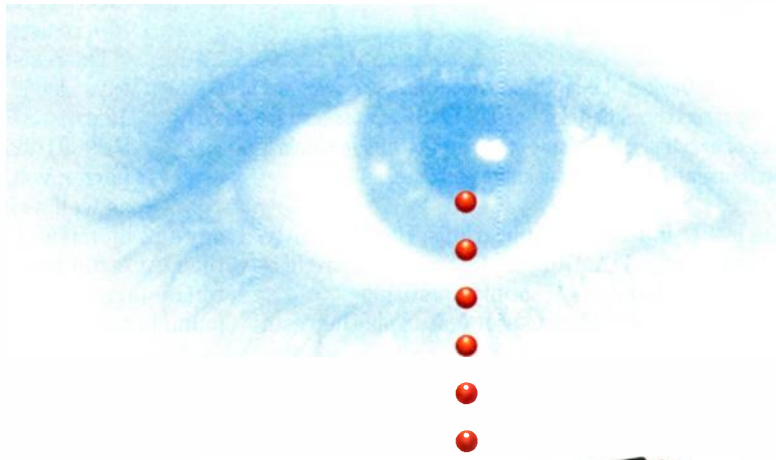
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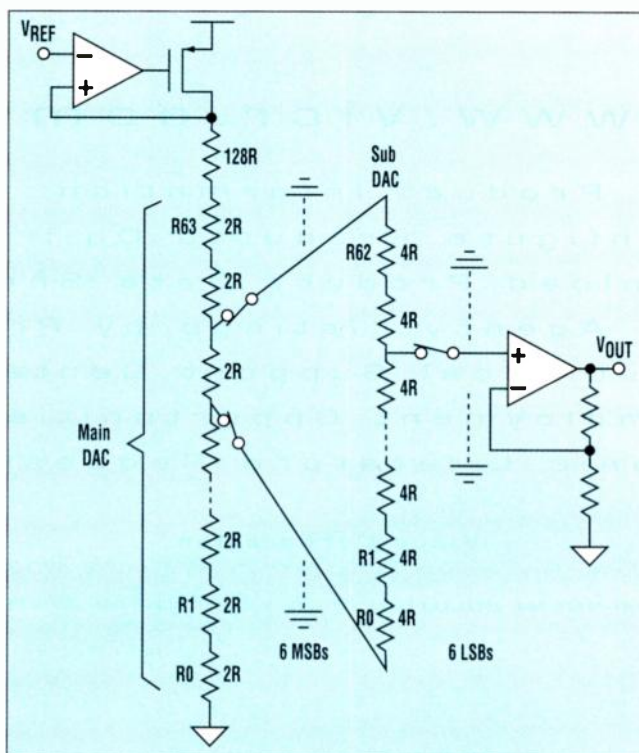
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Multichannel DAC solutions are ideal for activating valves, fans, and motors in industrial applications, where several DACs are required. To address such needs, Burr-Brown has packed four 12-bit voltage-output DACs on a single substrate. Previously, users employed separate DACs for each signal being processed, which in turn, required separate tweaking.

Now, quad solutions, such as Burr-Brown's DAC7624/25, that provide well-matched DACs from a single package, overcome this problem, says Bonnie Baker, Burr-Brown's applications engineer. These quads also offer two reference inputs; a high and a low. Because the voltage reference is not referenced to ground, the noise via ground is eliminated, notes Baker. Though many DAC makers prefer CMOS for low power and cost, Burr-Brown has opted for 2- μ m biCMOS for its quad models.

The biCMOS process exploits the low cost advantages of CMOS, while incorporating bipolar structures to support the wide operating voltage needed in



2. Analog Devices' 12-bit DACs exploit the low-power and high-integration capabilities of a fine-line CMOS process, and the smaller size of a multiplying resistor-string architecture to obtain high performance from micro-miniature packages.

industrial applications. Consequently, the DAC7624/25 feature both single 5-V and ± 5 -V supply operation.

Another useful feature is the reset

pin. An asynchronous reset clears all registers to a mid-scale on the DAC7624 or a zero-scale on the DAC7625. The DAC7624/25 are designed for 12-bit parallel data input; the serial input versions are the DAC7614/15. The quad DAC7624/25 come in 28-pin plastic DIP and SOIC packages, and cost \$9.15 each in 1000-piece quantities.

Burr-Brown uses the conventional R-2R architecture in its current IC DAC solutions. The manufacturer is in the process of employing silicon chromium (SiCr) thin-film resistors in versions to come, to obtain better dc characteristics from a smaller size. The company now uses nickel-chromium (NiCr) thin-film resistors.

The resistor string architecture also is evident in Sipex's, 12-bit SP9501/02/04 and SP9601/02/04 low-cost, low-power, voltage-output DACs, as well as in Linear Technology's 12-bit model LTC1659. To reduce the DAC's full-scale output sensitivity to the large weighting of the MSB found in conventional R-2R resistance

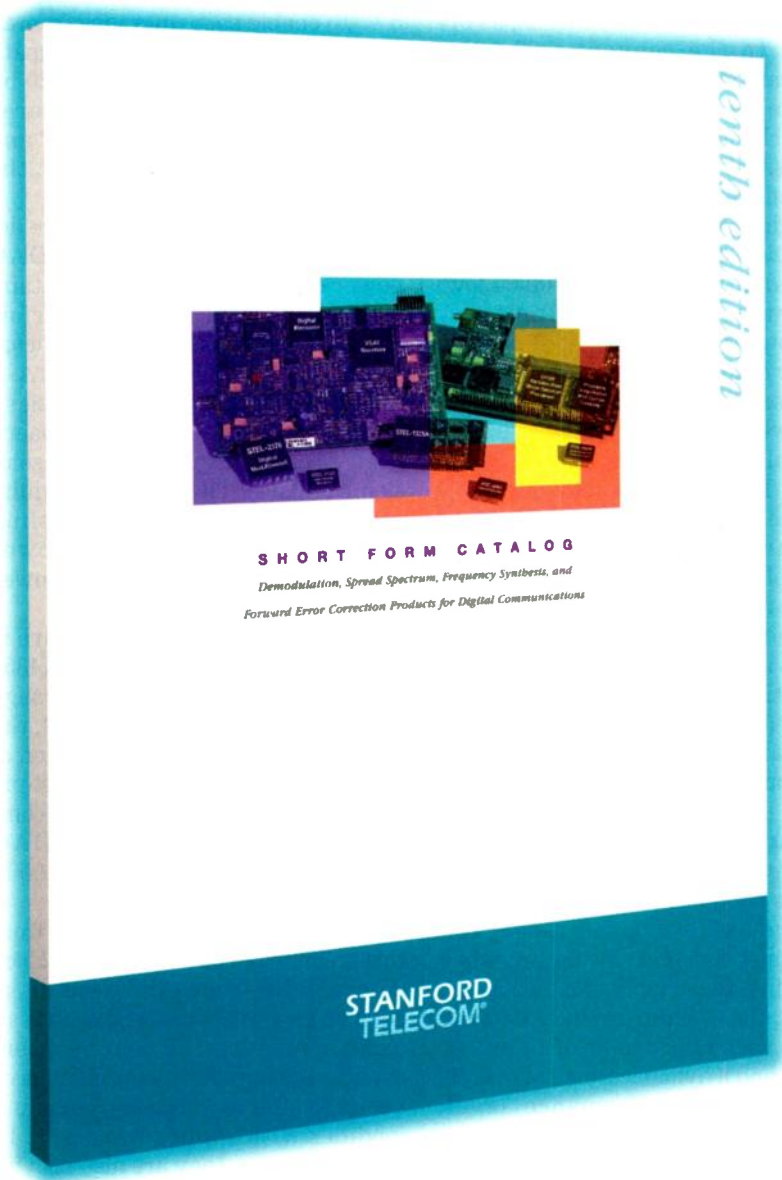
A REPRESENTATIVE COMPARISON OF LOW-COST COMMODITY 12-BIT VOLTAGE-OUTPUT DACs

Company	Model	Architecture	Process	Power Consumption (mW)	Setting time (μ s)	Maximum differential nonlinearity	Maximum integral nonlinearity	Package
Analog Devices	AD5320	Multiplying resistor string	0.6- μ m CMOS	0.7 (typical)	8 (typical) 10 (maximum)	± 1 LSB	± 4 LSB	6-pin and 8-pin μ SOIC
Burr-Brown Corp.*	DAC7624/25 (quad)	R-2R	2.0- μ m biCMOS	4.0/DAC (typical)	10	± 1 LSB	± 1 LSB	28-pin SOIC
Exar Corp.	XRD5412	Segmented resistor string	0.6- μ m CMOS	0.24 (typical)	13 (typical)	± 1 LSB	± 4 LSB	8-pin SOIC and 8-pin DIP
Linear Technology Corp.	LTC1659	Segmented resistor string	3.0- μ m biCMOS	1.25 (typical)	14 (typical)	± 0.5 LSB	± 5 LSB	8-pin MSOP and 8-pin SOIC
Maxim Integrated Products	MAX5352/5353	R-2R	1.2- μ m CMOS	1.5/0.9 (typical)	14 (typical)	± 1 LSB	± 1 LSB/ ± 2 LSB (low grade) ± 0.5 LSB/ ± 1 LSB (high grade)	8-pin μ MAX
Sipex Corp.	SP9501/9601	R-2R with three segmented MSBs	3.0- μ m biCMOS	16/2 (typical)	4/30	± 0.75 LSB (high grade) ± 1 LSB (low grade)	± 0.5 LSB (high grade) ± 1 LSB (low grade)	8-pin SOIC and 8-pin DIP
Texas Instruments*	TLC5618(dual)	Resistor string	0.8- μ m CMOS	8 (fast mode) & 3 (slow mode) (typical)	2.5 (fast mode) and 12.5 (slow mode)	± 1 LSB	± 4 LSB	8-pin SOIC

* Burr-Brown and Texas Instruments do not offer low-cost, single-channel 12-bit DACs, therefore, their representative quad and dual models are used here.

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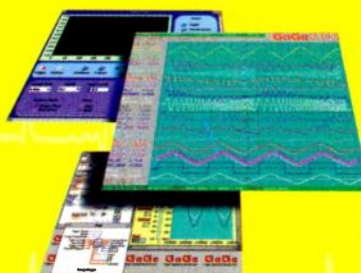
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ladders, Sipex uses a three-MSB segmented design. In this scheme, the three MSBs are decoded into eight, equally weighted levels.

According to Sipex's director of design engineering Alex Gusinov, this design reduces the contribution of each bit by a factor of four, thereby reducing the output sensitivity to the same number of mismatches in resistors and switches. This also improves linearity errors and stability, says Gusinov. Other benefits of a segmented design include a smaller untrimmed linearity error, less trim time, and lower cost. To further reduce the die area and cost of the DAC, Sipex uses a proprietary 1800-W/square, thin-film process, as opposed to the conventional 1000-W/square process, Gusinov says.

Like Burr-Brown, Sipex and Linear Technology also prefer a biCMOS process for DACs. Sipex has developed an inexpensive biCMOS process to produce low-cost, single- and multi-channel 12-bit DACs based on the segmented design—the 9501/02/04 low-power units, and the 9601/02/04 very low-power versions.

For example, the single-channel 9601 consumes only 2 mW (typical) at ± 5 V, while the 9501 is rated at 16 mW (typical) under similar voltage conditions. The 9502 and 9602 are dual-channel versions, and the 9504 and 9604 are quad models. The single-channel DACs come in 8-pin (0.15-in.) SOICs and plastic DIPs, and the duals and the quads are offered in 28-pin SOICs and plastic DIPs. In 1000-piece quantities, the 9501 and 9601 are each priced at \$2.20. In similar quantities, the dual versions cost \$4.70, while the quads are priced at \$9.40.

Δ - Σ Architecture

Many consumer digital audio applications need DACs with high resolution and a wide dynamic range. Yet, they must consume low power, while living in a reasonably small package. In fact, these audio products demand DACs with resolutions of 18 bits or better, and a dynamic range of over 90 dB. At this performance level, trimmed resistive DAC architectures run out of steam. To address these requirements without penalizing the user, manufacturers like Crystal Semiconductor and AKM Semicon-

ductor have adopted the Δ - Σ architecture with fine-line CMOS processes.

Using a single-bit, Δ - Σ modulation technique, Crystal Semiconductor's 24-bit stereo DAC CS4390 has raised the performance bar to a 106-dB dynamic range. It also has a 115-dB signal-to-noise ratio and -97 dB of total harmonic distortion (THD), plus noise. Also, the Δ - Σ technology alleviates the drift problems encountered in resistive-based DAC solutions. In addition, a fine-line CMOS process allows higher integration at lower cost.

Furthermore, the technology permits adjustable system sampling rates, including 32 kHz, 44.1 kHz, and 48 kHz. The chip consumes 185 mW at 5 V. To enable easy upgrades from 20 to 24 bits, the CS4390 is pin-compatible with the company's flagship 20-bit CS4329 DAC. The 24-bit stereo CS4390 comes in 20-pin SSOP and DIP packages. In lots of 1000, the CS4390 is priced at \$5.30 each.

Portable audio applications are demanding even further cuts in DAC power consumption, while maintaining higher resolution and ac performance. Engineers at AKM Semiconductor have developed a multibit Δ - Σ architecture that promises to slash the power by one-fifth without sacrificing the audio quality of high-resolution DAC ICs. The multibit modulator also reduces the oversampling rate, which translates into slower clocks. And, that means lower power in CMOS.

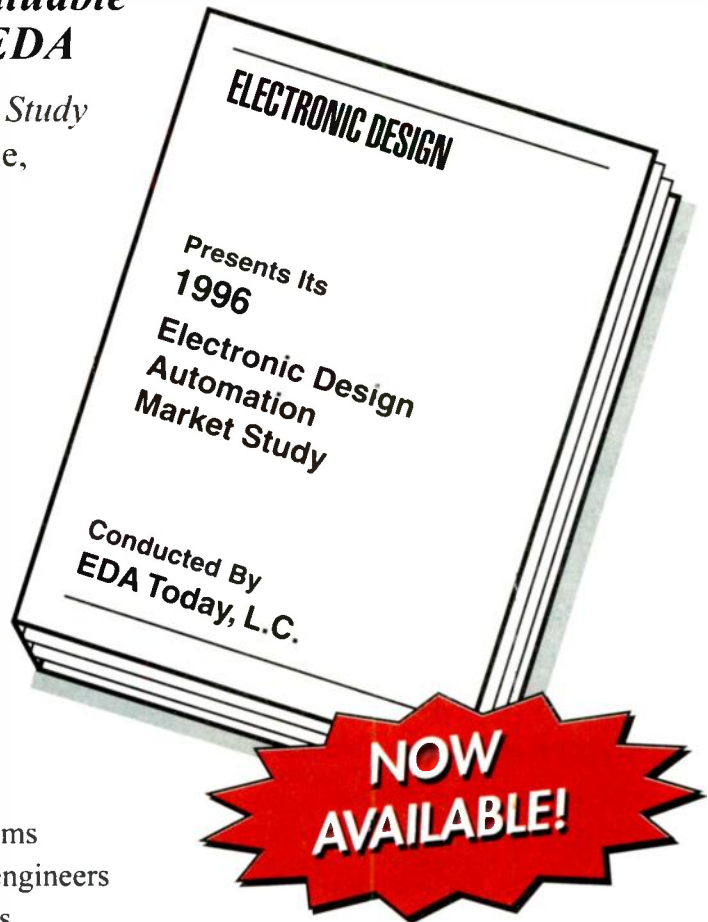
The multibit Δ - Σ architecture is implemented in AKM's 18-bit AK4350 stereo DAC. Offering a dynamic range of 92 dB with a SINAD of 85 dB, the AK4350 boasts power consumption of only 7.4 mW at 2 V. It comes in a 24-pin VSOP, and requires no external components. The 18-bit stereo DAC AK4350 carries a price tag of \$2.95 in 5000-piece quantities.

Selecting the right DAC chip from this ocean may not be as simple. Each device is different. And what looks good on paper may not be true in real-world applications. To help engineers evaluate the part fully, suppliers have begun to offer evaluation boards and modules with application notes. In some instances, they are also providing complete reference designs that go beyond the evaluation level to implementation in specific products.

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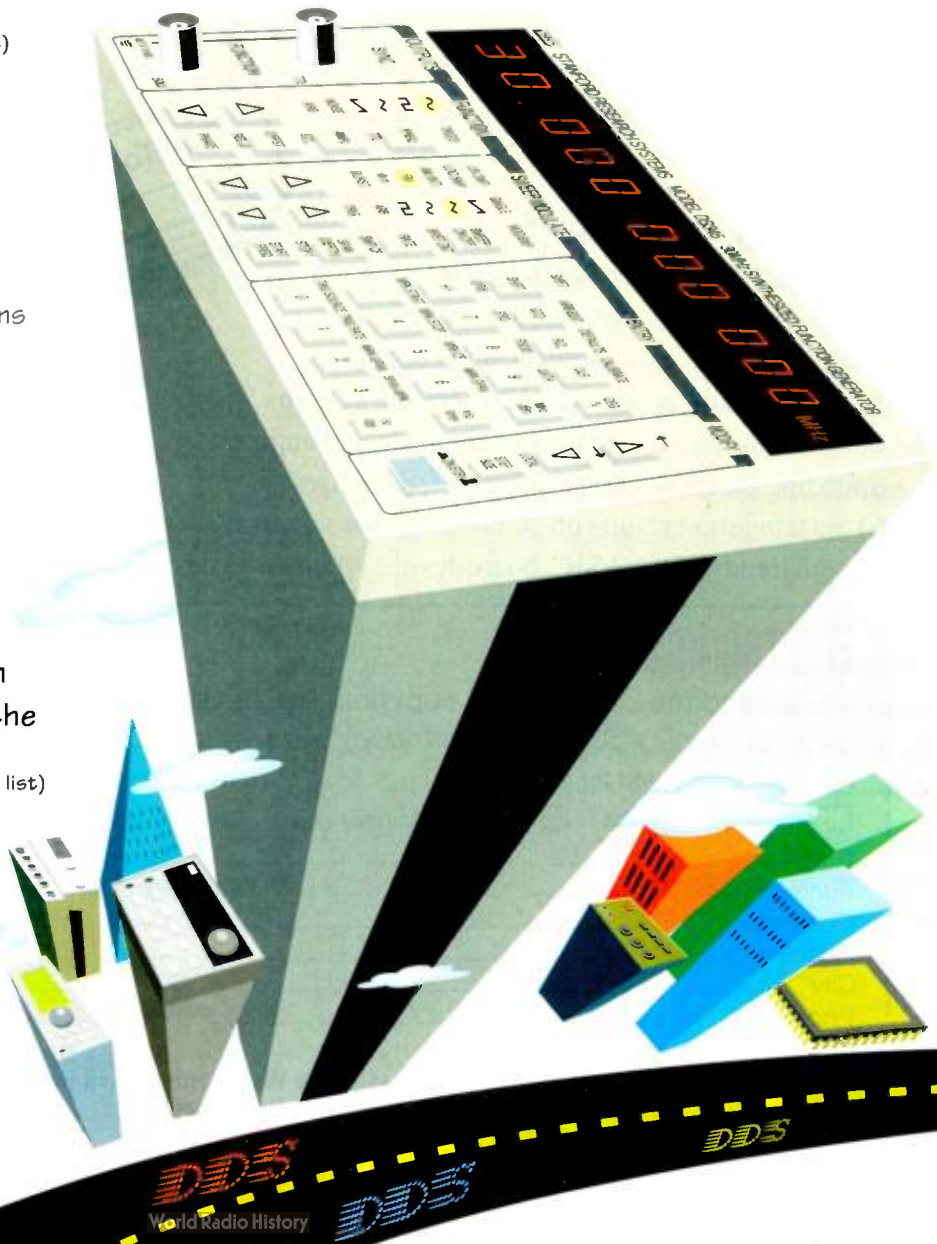
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Printed-Circuit Board Changes Enable New Design Possibilities

Designers Must Cope With An Evolving Market, And Understand Complex Advances In Pc-Board Technology.

Cheryl Ajluni

Printed-circuit board (pc-board) design is much different now than it was five years ago. A changing market and emergence of social issues have worked to shape a new environment for designers (see "New pc-board challenges," p. 84). Technical advances have placed extreme pressure on existing pc-board tools to continue to provide the desired performance and quality results in a shorter time.

Today, as designs become more complex, existing tools are being pushed to their performance limits. While issues such as packaging, advances in materials, and the desire to raise the level of design to the true "system" level are certainly representative of the types of changes coming down the road for pc-board design, it is the issues of migration to NT, high-speed design, and pc-board virtual prototyping that promise to have a more immediate impact on pc-board design.

One widely discussed issue is the movement away from Unix toward Windows NT. The move has been prompted by the evolution of PC performance to the point where there's no longer a difference between the power of tools on an Intel workstation versus those on a Unix workstation. And, for all practical purposes, Intel workstations are cheaper.

Having NT as a viable solution means that today's PCs can run many EDA applications just as fast as Unix workstations. It also means that high-end EDA tools (as opposed to low-end pc-board layout or

basic schematic-capture tools) can now run on PCs. And, these high-end tools, which include high-speed interconnect design tools, pc-board autorouters, and Verilog simulation tools, are now available in the same form on NT as they were on Unix.

This is advantageous for designers because, as Rick Almeida, vice president of marketing, PADS Software, Marlborough, Mass., explains, "Since

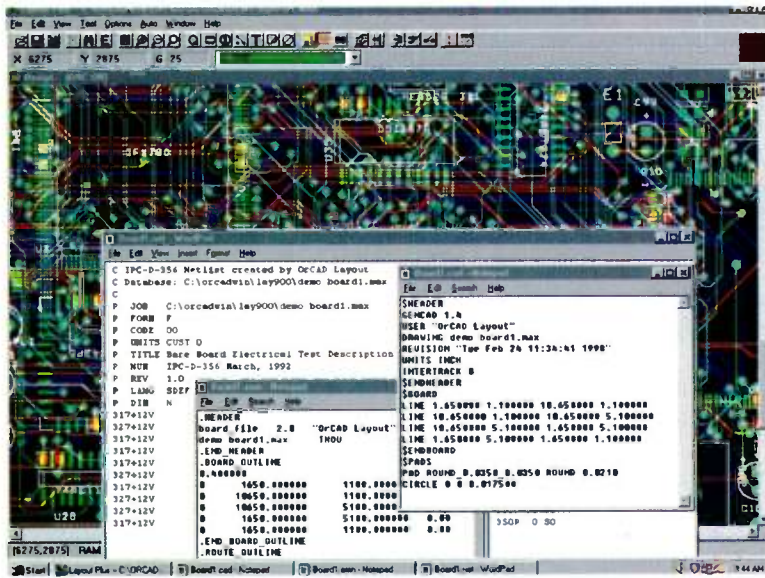
Unix no longer offers the performance or functionality advantages that it used to, the platform is really now a choice for customers based on their own computing strategies."

While there has been much speculation on how quickly the migration from Unix to NT will take place, the reality is that it is not going to happen overnight. Some Unix diehards have even been heard to utter the words, "I will die before I switch to NT." The reason they

feel so strongly is that until recently, the performance they got from Unix was unmatched by Windows-based applications.

Mark Noneman, Interconnectix Business Unit Director, Mentor Graphics, Wilsonville, Oregon, explains it this way: "These users design complex systems; resolving high-speed issues is just adding to their daily tasks and requires high-performance computers. On this Unix base, the migration seems slow, due in particular to the investment in Unix scripts to manage databases and design processes. However, the perceived lower cost of ownership of

SPECIAL REPORT



Art Courtesy: OrCAD

NT seems to play more in its favor. The challenge for these users is to provide them a solution that ensures Unix-NT cross-platform compatibility—because the migration won't be done at once—as well as provide similar performance on both platforms, especially for CPU-intensive tasks.”

Although the migration from Unix to NT is widely publicized, there is another migration path from Windows 95 to NT that plays a more defining role in pushing NT machines to support pc-board design. Until recently, pc-board designers designing lower-end consumer products have been able to get the performance they needed from cur-

rently available EDA tools running on a Windows 95 platform. But, what's happening now is that many of these designers are being driven by market pressures and higher system performance demands toward more complex high-speed designs.

For this new breed of pc-board designer, migration to NT offers them the ability to access performance capabilities in a similar environment to the one they are using today. The initial major shift to NT appears to be from these pc-board designers, and is attributed primarily to the fact that the high-end tools they require are now available on PCs running NT.

The migration to NT offers significant benefits to both the company and the pc-board designer. For example, many companies can drastically reduce costs and improve efficiency by eliminating the need to put both a workstation for EDA tools and a PC for such business applications as e-mail or word processing on a designer's desk. With an NT solution, the designer can consolidate all applications onto one PC and still get the same functionality.

As Dave DeMaria, vice president and general manager of pc-board products, Cadence Design System, San Jose, Calif., explains, “This is great news for designers. Now, they can have

New Printed-Circuit-Board Challenges

A key issue facing pc-board designers and the pc-board design industry is the relentless consolidation of pc-board vendors. This is due to several factors, including the recent upsurge in mergers and acquisitions. Industry analyst Gary Smith, Dataquest, San Jose, Calif., predicted a few years back that 75% of pc-board vendors would not exist in the coming years, and so far, his analysis is correct.

This presents a key risk and concern for pc-board designers, as it is extremely painful when vendors disappear. Oftentimes, this means that tools designers have grown accustomed to using die—requiring them to seek out new tool options. Examples of major mergers that have had profound impact on the industry include the acquisition of Racal-Redac by Zuken, Cadence's acquisition of Cooper & Chyan Technology—which subsequently acquired UniCAD—Synopsys' acquisition of Viewlogic, and the acquisition of MicroSim by OrCAD.

One issue dramatically changing the pc-board designer's entire purchasing decision process is the fact that the “traditional” tools that comprise the pc-board design flow, such as schematic-capture and pc-board layout, are not very different from one EDA vendor to another. The effect of this fact is threefold.

First, it means that pc-board designers need a compelling reason to switch from their current toolset. Windows NT, the need for high-speed tools, unhappiness with or the disappearance of their current supplier, all tend to be the major reasons for designers to switch. Second, pc-board designers need to find a vendor that is going to be a “partner” with them and, more importantly, be around to support them. As a result, the criteria for selection has changed from the ‘capabilities’ of schematic capture and pc-board editing to a combination of:

- Does the vendor have a solution that is going to solve my problems today and run on the platform, like NT, that I need? Do they have a viable solution for high-speed design?

- Does the vendor have a forward-looking vision and the ability to deliver on that vision? For example, do they have

the resources and technology to make that vision a reality?

- *Is the vendor going to be around? Do they have the financial resources? Are they growing? Do they have support near you?*

The third and final point is since most pc-board designers already have a pc-board system, a key factor affecting the designer's purchasing decision is the ease of transition from the old system to a new one. This often involves design and library translations, as well as retraining on the new tools. Pc-board vendors that offer services to help with this transition can be of great benefit to the designer.

Traditionally, pc-board design solutions have been segmented into three main toolsets: CAE (schematic capture, digital and analog simulation), FPGA design, and pc-board layout. Another major change occurring is the need to more tightly integrate these three pieces of the design process to better deal with both the technology demands and the continued pressure to shorten design cycles. Consequently, if you consider CAE and FPGA design as the engineering enterprise tool, then we begin to see the pc-board decision being lumped into the engineering tool enterprise decision.

The impact of this need is that pc-board designers are now looking for a more tightly integrated complete solution, while still demanding that each piece of the solution be “best-in-class.” However, more value is based on integration. The impact on vendors is the realization that they must provide a more complete solution that includes real front-end CAE, FPGA design and pc-board layout in a single unified solution. As a result, pc-board vendors will become “full solution vendors” providing the infrastructure for pc-board design, including such technologies as design capture, Verilog simulation, and pc-board layout. And, they will integrate best-in-class point tools, such as FPGA synthesis, and various analysis point tools, such as RF tools, into their design flow.

Contributed by Dave DeMaria, vice president and general manager of pc-board products, Cadence Design Systems, San Jose, Calif. For more information on this topic, see the company's web page at www.cadence.com.

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Seminar Locations		Introductory	Purchasing	KEELOQ	Advanced
Arizona	Phoenix	June 22	June 23		
California	San Jose	May 11	May 12		
	Irvine	June 8	June 9		
	Westlake	June 10	June 11		
	San Diego	June 24	June 25		
Colorado	Denver	June 8	June 9		
Connecticut	New Haven	May 13	May 14		
Florida	Orlando	June 15	June 16		
	Tampa	June 17	June 18		
Georgia	Atlanta	June 1	June 2		
Illinois	Chicago	May 4	May 5		
Indiana	Indianapolis	May 6	May 7		
Kansas	Kansas City	May 20	May 21		
Massachusetts	Boston	May 11	May 12		
Michigan	Livonia (Detroit)	May 18	May 19		
Minnesota	Minneapolis	June 1	June 2		
Missouri	St. Louis	May 18	May 19		
North Carolina	Raleigh	June 3	June 4		
New Jersey	Saddle Brook	May 13	May 14		
New York	Islandia, L.I.	May 11	May 12		
	Rochester	June 17	June 18		
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	Cleveland	May 20	May 21		
Oregon	Portland	May 13	May 14		
Pennsylvania	Philadelphia	June 15	June 16		
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	Austin	June 8	June 9		
	El Paso	June 10	June 11		
Utah	Salt Lake City	June 10	June 11		
Virginia	Falls Church	June 17	June 18		
Washington	Seattle	June 22	June 23		
Wisconsin	Milwaukee	May 6	May 7		
Canada	Eastern	Montreal, QUE	June 1	June 2	
		Ottawa, ONT	June 3	June 4	
		Toronto, ONT	June 15	June 16	
	Western	Calgary, AB	June 3	June 4	
	Vancouver, MB	June 24	June 25		
Mexico	Guadalajara	June 22	June 23		
	Mexico City	June 24	June 25		
South America	Argentina	Buenos Aires	May 18	May 19	
	Brazil	Sao Paulo	May 21	May 22	

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all the tools they need on a single platform. In addition, with the flexibility of portable PCs coupled with the advantages that the web provides, they have new freedom to work remotely, including from home, using hot design tools, while still being plugged in to their corporate network." Tom Hanson, marketing communications manager, Accel Technologies Inc., San Diego, Calif., adds "the NT solution can fit into businesses of any size in any environment, worldwide. Today's engineering design group size ranges from one person to networked global entities—the NT environment adapts easily to all of these."

The lower cost of hardware ownership and administration also is a prime benefit for those who adopt NT. But, application availability, ease of use, and integration with the rest of the company

have left doubts as to whether or not the migration is a good idea. For pc-board designers, these fears are calmed by the fact that a broad range of EDA tools running on NT are already available. And, although there may be a learning curve associated with using a new operating system and potentially new EDA tools, this too is made easier by the fact that many EDA companies, anticipating this period of transition, now offer mixed-environment solutions (*see the table*). Such solutions allow EDA tools to operate identically in both environments and maintain full cross-platform compatibility for all design files.

Going High Speed?

While a larger number of high-speed devices are being designed as ICs, they must ultimately be managed at the

board level. Managing such high speeds turns out to be a very difficult task because it leads to problems with timing, signal-integrity, and EMI.

Shrinking silicon feature size, lower voltages, and increases in system capacity and performance have strained existing tools to their limits. The side effects of these changes is increased edge rates which in turn create ringing, reflections, excess radiation and timing issues, and reduced system immunity to signal distortion.

Dave Kohlmeier, president HyperLynx, Redmond, Wash., explains: "Just as in deep submicron IC technology, interconnect delays have become a major issue in the design of the IC. The system designer is finding out that net delays on the pc-board have become an issue to deal with as well. However, delay

What You Need To Know

High-speed interconnect issues promise to dramatically impact the pc-board design process as well as the role designers play in that process. The pc-board designer's role, for example, must change to encompass a better understanding of the engineer's requirements and how to implement them in the physical domain. Pc-board virtual prototyping tools will help in this respect, but, as Gary Smith, EDA Analyst, Dataquest, San Jose, Calif., points out, "Roughly 80% of today's board designers are not degreed engineers." So, the question then becomes: How much engineering will the pc-board designer really need to know in the future, and where will the training come from?"

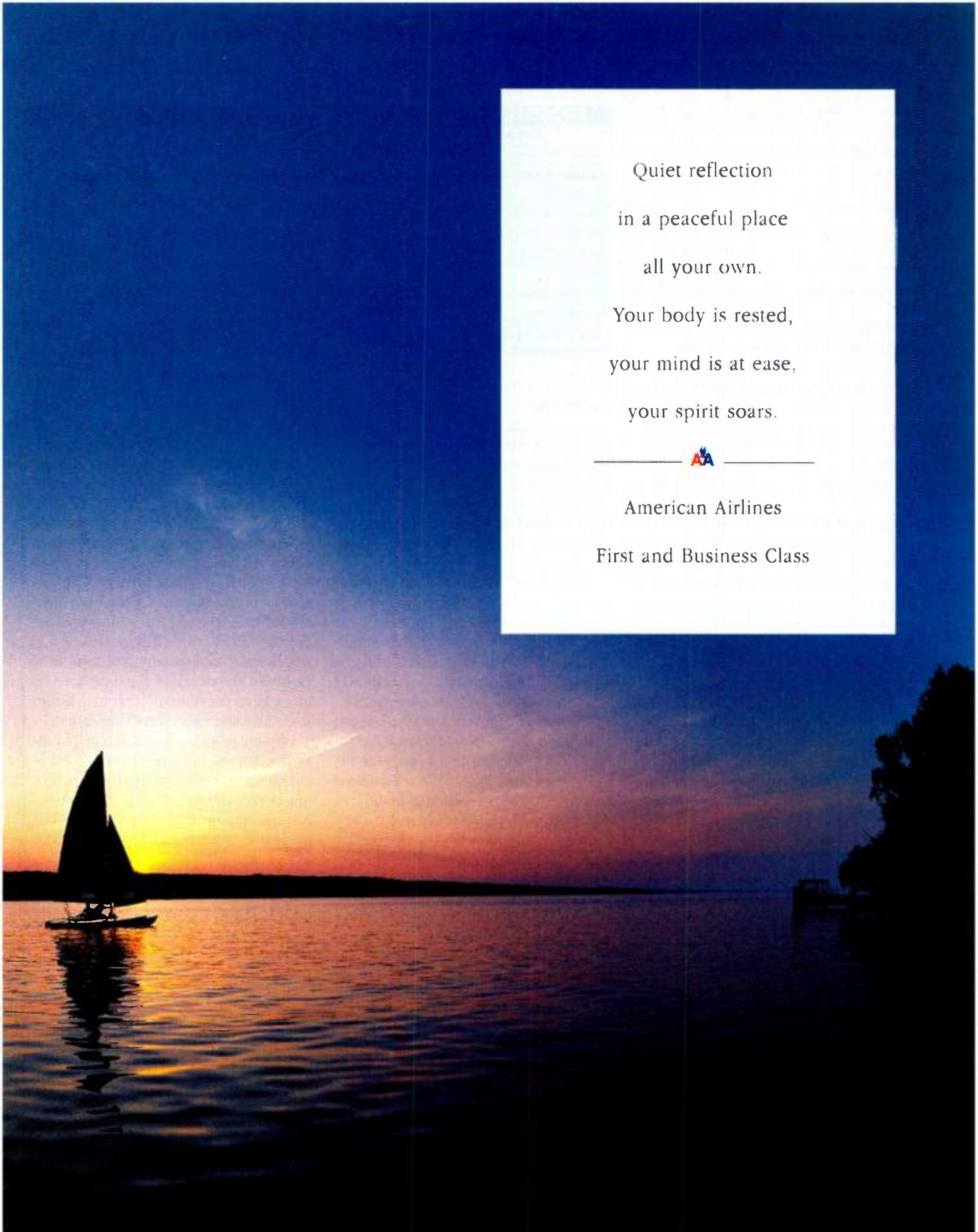
The easiest answer is that pc-board designers will need to become "engineering-aware." This does not mean, however, that they will need to become engineering experts. On the contrary, pc-board virtual prototyping tools capture much of the design engineer's knowledge, in the form of constraints or pre-routed sections of the design, and pass it on to the pc-board designer in the physical form that he or she can understand. Mark Noneman, Interconnectix business unit director, Mentor Graphics, Wilsonville, Ore., agrees with this assessment, adding that "board designers will need to know something about electrical engineering, but they shouldn't have to learn how to solve differential equations." On the other hand, while the engineering expertise might not be a requirement, for the pc-board designer committed to learning more about engineering, it offers not only a way for them to contribute more intelligently to the design process, but a means to potentially open up new career doors.

And where will this training come from? Fortunately there are a number of ways design engineers and pc-board designers can gain practical information on signal integrity and high-speed interconnect design. For example, many universities, such as the University of California at Berke-

ley, offer two- or three-day short courses. A number of EDA companies and other third-party organizations, such as Mentor Graphics or the Copper Connection, San Jose, Calif., also offer similar high-speed pc-board technology classes. Of course, for many pc-board designers, most of this knowledge is picked up through on-the-job training, or by attending industry trade shows, such as the Printed-Circuit Board Design Conference.

For the pc-board designer who either doesn't have the time, interest, or access to the resources to acquire such knowledge, don't worry. Intelligent "expert system" tools are emerging that may virtually eliminate the need for extensive training in the future. As Keith Felton, director of marketing for high-speed design, Viewlogic Systems Group, Marlboro, Mass., explains, "Pc-board designers will be presented information in their own language." For example, instead of being presented with: the signal needs to be 2 ns shorter, the pc-board designer will be presented with: take one-half inch of the trace length." And, if any training is required, it will most likely come from the EDA vendors, and relate to how to use a particular tool, as opposed to the pc-board designer needing to learn more about the specifics of engineering.

But to remain competitive in the industry, pc-board designers will not only need to know about engineering, but be able to understand both the physical and electrical implications of design decisions they are making. They also must understand the impact of their decision to the downstream process in fabrication, assembly, and test. As Rick Almeida, vice president of marketing, PADS Software Inc. Marlborough, Mass., summarizes, "Board designers will be pulled in both directions, and the successful ones will be those skilled enough to manage all of the demands placed on tomorrow's designs."



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times on the pc board are not just trace delays; it includes signal integrity issues sometimes referred to as 'flight times.' As a result, pc-board tools are being forced to become 'signal-integrity' aware."

In the past, signal integrity and EMI were dealt with by using manual placement and routing tools and on-line analysis packages. By ensuring that all high-speed constraints were met, these techniques effectively kept signal-integrity and EMI problems at bay.

According to Christopher Clee, technical marketing manager, Zuken-Redac, Inc., Santa Clara, Calif., "The real problem is not that signal integrity issues exist within a pc-board design environment; it is that, in many of today's designs, a large percentage of nets have these problems and, therefore, manual techniques are no longer adequate." Pc-boards are particularly critical as the electrical length of traces compared to the rise times of today's devices makes a large percentage of the nets on a board behave like a transmission line.

Unfortunately, the issue of high-speed cannot be ignored. By not dealing with it, or not addressing it properly, design teams run the risk of developing quality-related issues in their final products. Such issues might include products that operate intermittently or have low yields in manufacturing; both of which can mean death to a company trying to get a product to market before the competition.

The only way to combat this is to design high-speed problems out of the design. This means that pc-board tools must become more focused on solving signal integrity, emissions, and crosstalk issues. And, as PADS' Rick Almeida adds, this also means that "they will have to route the traces based on smart rules to assure the system meets speed specifications."

But it goes much farther than this. Using signal integrity analysis tools for analysis of a pc-board design at the end of layout no longer works for many of today's leading edge pc-board designers. One way to resolve this issue is by considering the physical 'constraints' up front in the early phases of the design process. This means a shift from a back-end post-layout analysis of the completed pc-board layout to up front tools that will allow early exploration of the design and the development of the

CROSS-PLATFORM OPTIONS OFFERED FOR PC-BOARD EDA TOOLS

Company	Windows NT	Unix
Accel Technology	✓	
Cadence Design Systems	✓	✓
HyperLynx	✓	
Mentor Graphics	✓	✓
OrCAD	✓	
PADS Software	✓	
Veribest	✓	
Viewlogic Systems Group	✓	✓
Zuken-Redac	✓	✓

This table is representative of only those companies mentioned in this article. No distinction is made between platform options available now and those that will be available prior to the end of 1998.

constraints that will drive placement and routing.

Such a shift will require new physical tools for the design engineer as well as a change in design methodology. Analysis technology, such as signal integrity, timing, and EMI, also will need to be coupled with constraint management tools and with placement and routing tools.

The issue of models also must be addressed. Although IBIS provides a standard for signal integrity models, it lags behind the leading-edge technology. What's needed is the flexibility to model these complex devices while still staying ahead of the technology curve.

For the pc-board designer, all these changes boil down to the need for increased knowledge of the issues relating to high speed (*see "What you need to know," p. 86*). Pc-board designers must be able to identify edge-rate problems and their effect on the performance of a design, as well as understand how to make changes to minimize these effects. They must get up to speed on tools used to predict and identify signal problems in the layout before prototyping. And, they will need tools with a much higher level of automation. Design engineers, on the other hand, will need to get more involved in the physical interconnect design and will require a wider set of constraints that they can use to control downstream processes.

Virtual Prototyping

Pc-board virtual prototyping tools have been identified as one way to bridge the gap between the design engineer and the pc-board designer. They are used in the area of the design flow where the engineer and designer functions merge. They are specifically designed to increase the cooperation and

communication between the design engineer and the pc-board designer. Accel Technology's Tom Hanson, extends this definition by including "cohesive project management teams that rely on analysis, project management, communication and floor-planning tools up front. These teams often include nonengineers, such as purchasing managers. All have a unique way to define a 'successful product release,' yet all share the goal of growing their business through timely and profitable product release. To beat this design time clock, teams must take all physical aspects of pc-board layout and design into account as early as possible to minimize design iterations and maximum compliance."

Virtual prototyping tools work by allowing the design engineer to do early concurrent exploration of the design and derive the constraints. Such explorations might include floorplanning the design to meet timing requirements, signal integrity optimization, or synthesis of critical nets to meet electrical requirements. If the prototyping tool is a robust solution, then all constraints derived during exploration can be automatically passed to the place-and-route tools used by the pc-board designer.

According to Mentor's Mark Neman, "The design process must leverage concurrent analysis to allow the design to be verified electrically as it is implemented. Thus, as designers make changes in the 'virtual' design, they are given feedback about any of these changes. The ultimate goal of the virtual prototyping environment is to allow the design team to realize an electrically correct design that maximizes performance and will operate with first pass success."

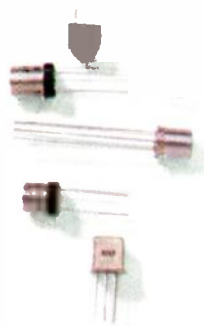
While the promise of virtual prototyping tools is that communication and enhancement of the design process will be made easier between the engineer

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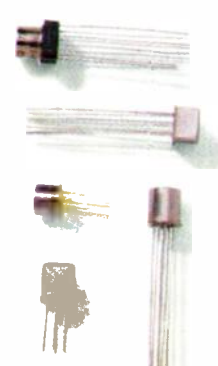
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and the designer, there is one downside. According to PADS' Rick Almeida, "Conceptually, with any engineering task, the more planning you can do up front, the more likely your success with delivery to market. Virtual prototyping allows you to do just that. The problem with pc-board virtual prototyping is that we have to ask customers to add another step in the process in an industry that attempts to minimize steps wherever possible."

A common misconception with the emergence of pc-board virtual prototyping tools is that they will replace the pc-board designer. The fact is that the design engineer can no longer expect to annotate a schematic with high-speed constraints and throw it over the wall to a pc-board designer. With increasingly complex designs and shortened design cycles, this is simply not a viable option. Instead, they must experiment in the physical domain, using pc-board virtual prototyping tools, to understand what can be achieved during the design process. Consequently, rather than eliminate the pc-board designer, they act as a platform for engineers to evaluate design trade-offs and to place intelligent constraints on the design process.

Cadence's Dave DeMaria notes that "some pc-board designers may feel threatened by the high-speed revolu-

tion and feel that design engineers will take over their jobs and have push-button tools that are good enough to replace designers. But, design engineers don't want to do the place and route of the pc board; they're being pulled into it. In addition, there will always be a need to optimize the design for manufacturing, a role typically played by the pc-board designer."

The bottom line is that the pc-board designer and the system engineer can accomplish more together. A high-speed designer, for example, understands high-speed digital design and will be the one to utilize "virtual prototypes." But, as HyperLynx's Dave Kohlmeier points out, "Layout experts will continue to finish the design and will be the experts on the manufacturability of the pc-board—something the digital system designer will not have the time to address."

This is because when it comes to the challenge of designing smaller, cheaper, more reliable, more easily manufacturable products—something outside the realm of engineering—the pc-board designer is the expert. This is not something that will change despite the emergence of virtual prototyping tools. The engineer's challenge will remain; to determine the predictability, viability and sensitivity of the design and the op-

erating margins required to stay within those parameters.

New Tools

New pc-board tools are indeed surfacing. One soon-to-be-released tool comes from Accel Technologies and focuses on signal integrity and crosstalk analysis. It works by providing a very rapid and accurate simulation of reflection and crosstalk effects on pc-boards. It also offers an interactive environment with an oscilloscope-type results display, result measurement, spreadsheet-like post processing, and "what-if" analysis of termination and routing strategies. A related tool, also soon to be released, will target design constraint management during pc-board layout, and works by enforcing comprehensive pc-board design constraints based on net properties. Both tools will be available in the second quarter of this year.

A number of companies also are developing new techniques and methodologies to help designers better deal with the growing complexity of pc-boards. Mentor Graphics, for example, is working on new algorithms to handle the new pc-board technologies that will be needed for the most advanced designs. They also are investigating new software technologies for implementation of tools and processes to help designers solve difficult interconnect problems.

Zuken-Redac is working on a program that it refers to as "Layout Synthesis," which manages the increase in design complexity by enhancing the automation of rules-driven placement and routing. This is accomplished by increasing cooperation between automatic placement and routing tools and by giving access to a wider set of constraints through constraint management tools. The Layout Synthesis toolset will feature increased automation, as well as full user override into semi-automatic and interactive design modes.

For its part, Cadence Design Systems has ongoing projects in the high-speed area. These focus on integrating the IC, or silicon design environment, with advanced package design; all ultimately integrated with board-level designs. These efforts will target both the deep technology issues in modeling and analyzing the interconnect across all three domains, as well as integrating the flow of design tools necessary.

One significant trend coming down

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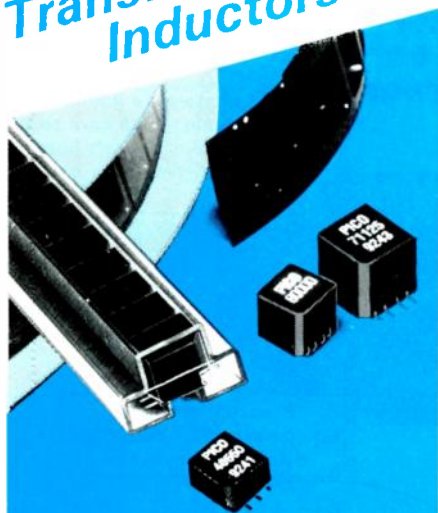
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the pipeline is the impact of packaging on high-speed design. This is becoming a critical path issue, particularly as you consider such effects as signal integrity from the die/chip to the package to the board. One reason why packaging has become an issue is that there is a concerted migration toward complex packaging going on in the pc-board industry.

This has left many designers struggling with BGA packages exceeding 800 contacts. Traditional pc-board routing tools just can't handle these very dense packages; they're constantly getting bigger as more designers place bare die on pc-board substrates to achieve higher densities, or improve signal performance. This has led to the development of such techniques as laminate BGAs, MCMs, and chip-scale packages.

But, to continue meeting the needs of the most advanced pc-board designs, advances in packaging technology will need to not only continue, but accelerate, and design tools, particularly on Windows platforms, will need to be able to support the different types of packaging technology for pc boards.

According to HyperLynx's Dave Kohlmeier, one issue expected to have an impact on pc boards is the "communication between layout and simulation tools. If we just try to constrain layout tools with a bunch of signal integrity issues, layout tools will choke on the constraints. They must work together on a net-by-net basis to get the job done." Toward that end, HyperLynx is developing an API for its simulator so that its layout tools can talk interactively with the signal integrity tool. The company is actively working with several pc-board vendors to get this defined.

According to the Viewlogic Systems Group, Marlboro, Mass., another area of interest is the trend toward powerplane analysis as a prerequisite to signal integrity analysis. This is necessary because in low-power (defined as 3.3 V and lower), high-performance designs, simultaneous switching of devices drags down the power rail. Higher speeds (>100 MHz) and wider buses (64 bits and up) only serve to aggravate this problem, and is not properly accounted for in current signal integrity tools. In fact, these tools often assume stability of the power plane in their analysis.

In an attempt to better represent these effects, Viewlogic is working on redeveloping AC/Grade, a tool for the

design and trade-off analysis of power switching effects in pc-board and MCM structures, as a power plane analysis and verification tool, as well as a co-simulation tool with signal integrity for real-world predictability.

Veribest, Boulder, Colo., identifies the movement of multiple design technologies on a single board as a trend that promises to create much change in pc-board design. This is being driven by requirements for reduced design cost and form factor. A prime example of this is a mobile phone. At one time, these devices were composed of separate RF, analog, and digital designs. Now, they are all sandwiched onto one board. In fact, it's safe to say that where at least two toolsets (RF and pc-board layout) were used in the past, now one is desired. This combination of toolsets will need to be addressed.

John Shotsky, product marketing manager pc-board design tools, OrCAD, Beaverton, Ore., says that another issue for the pc-board industry to address is that "just as the engineer is becoming more involved with pc-board design, the pc-board designer is becoming more involved in the fabrication, assembly and test (CAM) phase of product development. As a result, pc-board designers are required to know much more about the downstream processes."

To help deal with this situation, a number of initiatives have been brought forward proposing standards for passing pc-board (CAD) data to the CAM end of the business, where such data is further processed for operation with specific machines, such as bare-board testers, pick-and-place machines, and functional testers. These machines drive a need for more complete information, starting at the design-entry phase (CAE), and passing throughout the CAD process into the CAM process.

Such information is not traditionally passed in Gerber data, the current standard data format provided by most pc-board tools. OrCAD, recognizing this need, has worked to enable engineers to choose components through its Component Information System (CIS) which can then be put directly into OrCAD Capture (CAE). That data passes through to OrCAD Layout (CAD), and through OrCAD's GenCAD format passes the information to downstream software (CAM), such as Mitron's CimBridge, and FabMaster's tools.

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BOP 50-2M	$\pm 50V$	$\pm 2A$
BOP 100-1M	$\pm 100V$	$\pm 1A$
200 WATT		
BOP 20-10M	$\pm 20V$	$\pm 10A$
BOP 36-6M	$\pm 36V$	$\pm 6A$
BOP 50-4M	$\pm 50V$	$\pm 4A$
BOP 72-3M	$\pm 72V$	$\pm 3A$
BOP 100-2M	$\pm 100V$	$\pm 2A$
BOP 200-1M	$\pm 200V$	$\pm 1A$
400 WATT		
BOP 20-20M	$\pm 20V$	$\pm 20A$
BOP 36-12M	$\pm 36V$	$\pm 12A$
BOP 50-8M	$\pm 50V$	$\pm 8A$
BOP 72-6M	$\pm 72V$	$\pm 6A$
BOP 100-4M	$\pm 100V$	$\pm 4A$

BOP-HV MODEL TABLE

MODEL	d-c OUTPUT RANGE	
	E_0 max.	I_0 max.
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BOP 1000M	± 1000	$\pm 40mA$



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Leveraging LCD Module Designs For Handheld Applications

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MICHAEL G. PETERA, Three-Five Systems Inc., 1600 North Desert Dr., Tempe, AZ 85281; (602) 496-0035; fax (602) 389-8701.

Designing and implementing a liquid-crystal display (LCD) module for small, handheld applications requires particular attention to issues such as size, viewability, weight, cost, ruggedness, and tolerance of temperature extremes. While available technologies have greatly advanced the LCD's performance in each of these areas, the advances themselves create problems. To avoid these "gotchas" and ensure a smoother design flow, it is helpful to break down the module design stages and examine them in the context of these recently introduced advances. The stages can be loosely defined as the glass design and layout, the driver and interconnection technology, and the backlight as both an optical and mechanical component.

Glass Design

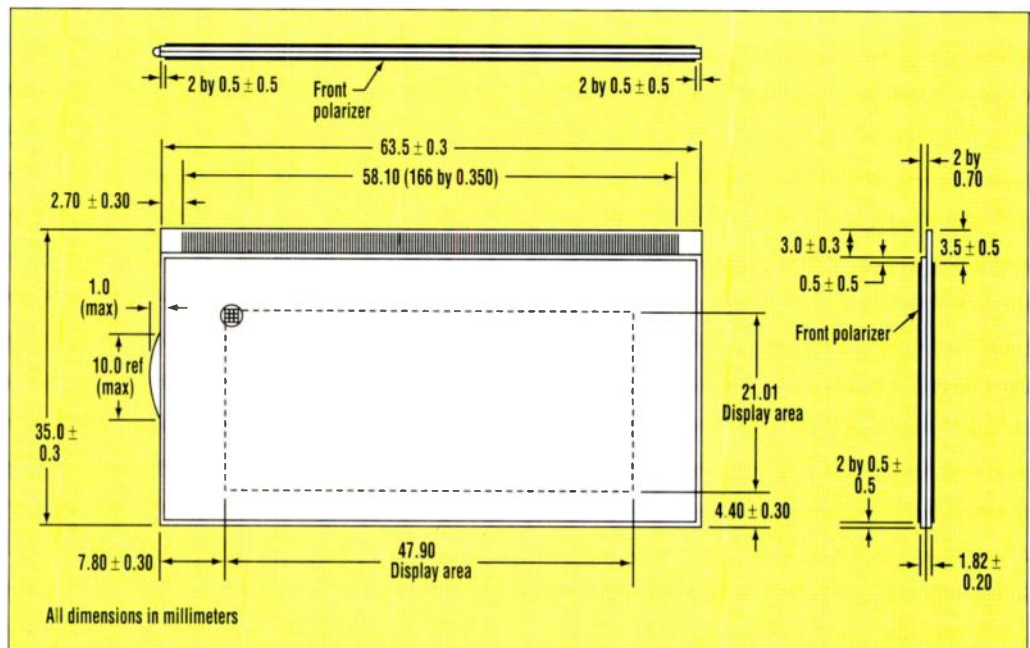
To create a cost-effective module design, the issue foremost in the designer's mind should be how to create a glass layout that will use the least amount of glass area to implement the desired display format (Fig. 1). In addition to the active viewing area of the glass, the other physical constraints of intercon-

tion ledge width, seal width, and the inactive area between the active viewing area and the environmental seal need to be minimized. This must be done without compromising the mechanical/environmental integrity of the display.

Pixel Size: At the heart of the design are the size of each pixel and the number of pixels that are required to present a suitable display to the user. Today's glass manufacturer can fabricate displays with pixel sizes that are

smaller than can be suitably viewed by a human. When pixel size is below a threshold of approximately 0.25 mm, the usefulness of the display in the handheld environment begins to degrade. At issue is character size, especially in a single-pixel format. Below this 0.25-mm threshold, multiple pixels must be used to create alphanumeric characters, leading to an increase in hardware and software complexity.

Generally, the larger the pixel, the



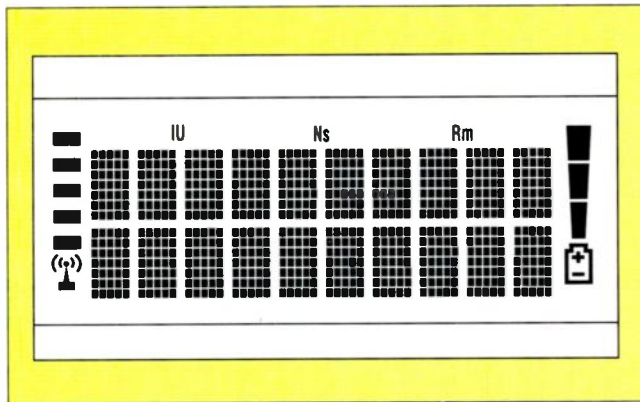
1. Proper glass layout is crucial to a cost-effective LCD-module design. While the size of the viewing area must be maximized, other factors such as interconnection ledge width, seal width, and the dimensions of the inactive area between the active viewing area and the environmental seal, need to be minimized. All must be done without compromising the mechanical/environmental integrity of the display.

more readable the information on the display. As a result, in the small, handheld environment, pixel sizes are usually greater than 0.30 mm. This pixel size allows enhanced character readability, and leads to quicker recognition of characters by the user. Thus, the user experiences less fatigue, especially under conditions of high usage.

To provide some aspect of differentiation, some manufacturers have adopted an asymmetric pixel shape for their characters' dot-matrix display formats. They have opted for a pixel that is taller in the vertical dimension than the square pixel. This pixel format is due to the aspect ratio required by the display. Again, a larger display makes it easier for the user. Therefore, if any dimension can be increased, without compromising the quality of the display, it will further aid the user in recognizing the presented information. In these instances, it makes sense to increase only the vertical size of the pixel. Note, however, that the format will make it unsuitable for use as a graphics display, due to the asymmetry of the pixel.

Active Viewing Area: The next step in the design process is to determine the number of pixels necessary for proper display of the desired information. In small, handheld environments, the trend is to put as much information on the display as possible, while keeping it from appearing crowded. In most cases, the display size is limited to no less than two lines of 10 characters, and no more than eight lines of 20 characters, within the graphics area. Icons can either be included in the display, or generated in the graphics mode, the character formats are user programmable, thus individual character format is a function of the application.

For the application of eight lines of approximately 14 characters, the total number of pixels in the graphics display will be at least 100 pixels horizon-

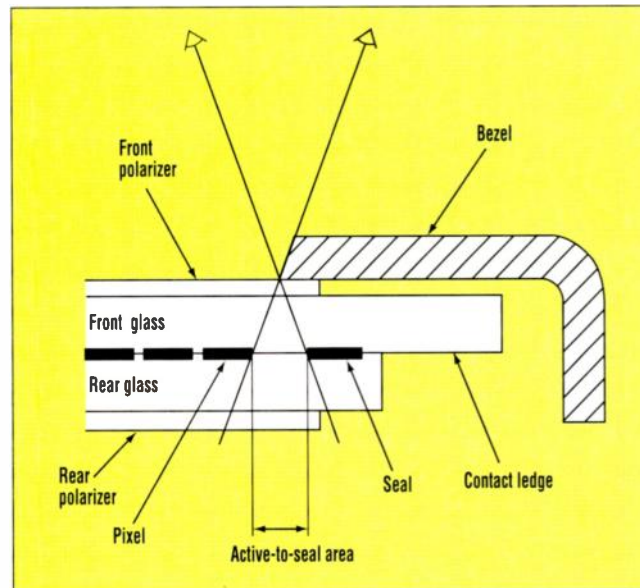


2. After deciding the pixel format, the entire display should be modeled. This effort will save a lot of headaches in the future. When modeling the display format, it is important that the display be scaled to actual size to assess the readability of the information presented. Mylar film should be created to evaluate the display formats.

tally by 64 pixels vertically. Standard LCD drivers are available which will drive formats of 102 by 65 pixels.

A viewable graphics area of 47.9 by 30.5 mm results when using the square-pixel format and a pixel size, trace, and space of 0.47 mm. The active area of the display is shown in Figure 1.

Note that the active area is much smaller than the actual glass area. This is to accommodate the area needed on the ends of the glass to route the row



3. The distance between the active pixel area and the inside edge of the LCD seal is determined by the bezel. This distance greatly affects the display's aesthetics. The seal width provides a mechanical link between the upper and lower glass plates, protects the liquid-crystal material from the environment, and provides precise spacing between the two plates. The contact ledge connects the LCD glass to the external driver circuitry, and its width determines the mechanical integrity of the interconnection medium into the glass.

traces. In small, handheld display applications, only one ledge can be used to interconnect the row and column lines. In our example, 32 row lines must be routed on each edge of the glass. As the number of rows increases, the number of crossover connections between the glass plates must increase, leading to lower reliability and higher cost.

Display Modeling

Once the pixel format is chosen, the entire display format should be modeled. When modeling a display format, it is imperative for it to be scaled to actual size, to assess the readability of the information presented. Mylar film, the same material used in the pc-board industry, should be used to evaluate the display formats. CAD packages, such as AutoCAD, are more than adequate for producing a mylar model (Fig. 2).

Display format modeling will save headaches in the future, especially from the marketing and sales, as well as the human aspect of the product. Many projects have failed after the prototypes have been delivered because the utility of the display was compromised due to inadequate pixel and/or display size, or unacceptable information content. It is obvious that, at this end point, time and money have been expended for no useful purpose.

Viewing Area-To-Seal Distance: The next area of consideration is the distance between the active pixel area and the inside edge of the LCD seal (Fig. 3). This distance is usually defined to be approximately 1 mm minimum. However, the actual distance is determined by the bezel opening in the user's housing.

The edge of the bezel opening should be within this area. To properly hide the seal area, the bezel should be placed as closely to the glass surface as possible, while retaining mechanical integrity.

The factor that defines the active area-to-seal distance is the

In most hand-held display applications, high-quality, environmentally stable polarizers are used. When designing the display module, the operational/storage environment of the display will dictate the polarizer to be used. Cost must become secondary to performance. For example, a polarizer used in an office product will not see the same temperature extremes as those encountered in a cellular-phone environment. The polarization efficiency can be increased in the office environment, reducing the cost.

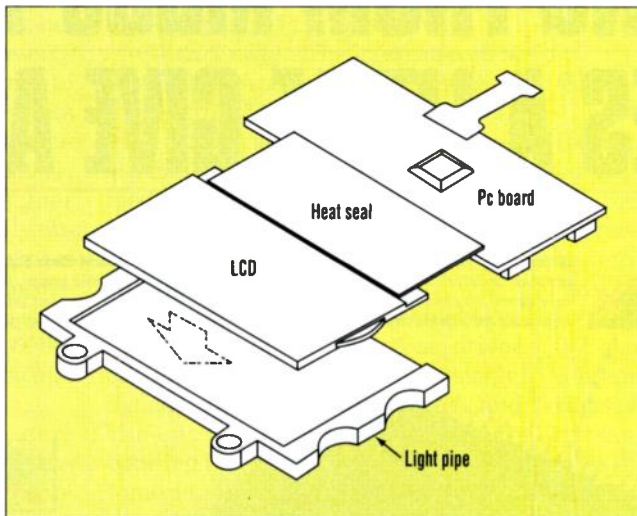
With this trade-off in mind, the system designer must be aware that improper polarizer selection can unnecessarily increase the cost or degrade the optical performance of the display.

Wiring And Interconnections

A number of technologies are available to provide electrical drive signals to the display. They include pc boards, heat-seal connectors, flexible circuit-board material, and TAB technology. The first of these, the pc board, is the most cost-effective method of providing signals to the display (Fig. 4). Whenever possible, a pc board, preferably using a thin material to reduce weight, is used as the base material for the interconnection of all electronic components. The pc board can be designed to accommodate a number of driver types and interconnection styles, and can be used as the structural support and mechanical fixturing for the display module.

Pc-Board Trace Resolution: To produce the most cost-effective module, the circuitry required to properly drive the display must be placed entirely on the pc-board substrate. Thus, the smallest components are used, as well as the most efficient interconnection methods between the driver and the output pins.

To this end, the trace resolution of the pc board should be kept to the minimum possible widths. In most high-volume applications, trace and space widths are kept to approximately 0.125 mm. Although further reduction in trace and space widths can be realized by some suppliers, the highest degree of manufacturability comes from pc boards that do not violate this basic size



6. The typical small, handheld backlight consists of a light pipe, diffuser material, and an LED illumination source. The light pipe serves both as an efficient LED light disperser to illuminate the display, as well as a mechanical structure for the display glass and pc board.

constraint. In most applications, this trace and space width will be adequate to attach most of the common LCD drivers to the pc board. Higher pin densities require more-advanced and expensive interconnection techniques.

The Chip-On-Board Process

The enabling technology for low-cost electronic modules is chip on board (COB). This technology, used in various forms since the mid 1970s, attaches the bare silicon die directly to the pc board. The die is then wire bonded to the board to create the interconnections between the driver and the display. After wire bonding, the die and wire bonds are protected with an epoxy encapsulation. As a rule, standard pitch die consisting of between 100 to 150 outputs can be easily wire bonded to the pc-board substrate.

The COB packaging method eliminates the requirement for a physical package around the die. The elimination of the package translates directly into cost savings to the module. Additionally, the use of COB allows a smaller interface circuit board to be used—again translating directly into cost savings on the module, and size reduction of the end item.

Heat-Seal Interconnection

When using a heat-seal interconnection from the pc board to the LCD glass assembly, a critical design factor is that the pitch of the glass must equal the pitch of the pc board. Slight variations in pitch can be accommodated on either

the glass or the pc board. However, neither the pc board nor the glass can be too wide because the overall module width must be maintained between components.

Both the glass and the pc board must have enough interconnection length to attach an interface connector. In most cases, the interface connector consists of graphite traces on a polyester carrier, which is bonded to both the glass and pc board with an anisotropic conductive adhesive.

Various manufacturers of this material are available. They have generated the data necessary to ensure that the assembly parameters of bonding time, pressure, and temperature produce an environmentally sound bond that will last for the service life of the product.

The heat-seal conductors can be fabricated in pitches that are slightly smaller than the pitches realizable on a pc board. Both the pc board and the glass must have sufficient interconnection trace length to allow the heat-seal connector to be bonded properly to both substrates.

Tape Automated Bonding

TAB technology is capable of the finest interconnection pitches. This method eliminates the need for wire bonding as a method of attaching the driver die to the Kapton/copper substrate material.

A process called inner-lead bonding is used to directly connect the pads on the driver dice to the copper traces of the TAB package. After inner-lead bonding has been completed, the driver dice is encapsulated in an epoxy material to maintain the environmental stability of the package. Inner-lead bonding pitches of 0.07 mm are routinely used for this application.

In general, the pitch used to accomplish the inner-lead bonding can also be used in other locations of the TAB circuit. The output portion of the TAB package usually consists of an arrangement of fingers that will make contact with the matching pattern on the interconnection ledge of the glass. Current technology allows this pitch to be as low as 70 μm . In practice, making the attach-

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ment pitch larger can enhance the yield of the TAB-to-glass interconnection.

Usually, high-density pitches are necessary to create one-third of a color pixel—either the red, green, or blue portion. The pitch required for color display applications is approximately three times smaller than the pitch that necessary to make the monochrome counterpart.

Chip-On-Glass Technology

Chip-on-glass (COG) interconnection technology is quickly becoming a recognized industry alternative to attaching the driver die to the liquid-crystal display (*Fig. 5*). For a COG implementation, each pad on the driver die is patterned with a gold interconnection "bump" to create a path of conduction from the glass substrate. These bumps are deposited onto the die, and allow a coplanar, conductive offset interconnection path from the driver dice to the glass surface.

Currently, the methods of attaching the dice to the glass involve an anisotropic adhesive, comprising a matrix of conductive gold spheres. The spheres are spaced apart from one another in such a manner that they are only conductive in the vertical axis. However, from a manufacturing standpoint, this attachment process is in its adolescence. High-volume assembly equipment is now becoming available to allow efficient, high-yielding processes to be realized.

COG is an appropriate interconnect technology for many LCDs, as the pitch of the interconnect pads on the dice translates directly to the input pitch of the glass. Current glass-fabrication technology makes it relatively easy to align the dice with the glass traces.

The benefits of COG are many, and include fewer interconnection process steps to produce the assembly. Rather than three steps, as is the case for a pc-board implementation, there is only one step required for COG. Thus, yield is significantly enhanced. However, there are negatives as well. For instance, the glass package size must be increased slightly to accommodate the chip and the fan in of the row and column leads.

LCD Driver Architecture

Having discussed the interconnection aspects of the driver die to the glass, it is time to discuss the electrical

functionality of the LCD driver itself. In most handheld display modules, the entire electrical functionality of the chip is contained on a single silicon substrate, including the row drivers, column drivers, controller, and voltage generator.

One of the most important criteria of the LCD driver is its ability to support the required LCD voltage. The quest for lower battery voltage is very much alive in the portable display industry, and has been responsible for the considerable reductions in battery weight and/or the increase in battery life.

Even though the trend toward decreasing battery voltage continues rapidly, the rate of voltage reduction occurring in the available liquid-crystal-fluid materials is not keeping pace. Although the physics of today's fluids changes such that we can create new displays with lower voltage, there is a physical limit that cannot be surmounted once the battery voltage goes too low. This means that higher voltages must be created and supplied by the driver chip, especially with a display module that has wide temperature-range requirements and/or high multiplex rates. As a result, voltage multiplication must be contained within the chip. In some cases—especially in higher-multiplexed display formats—voltage quadrupling or quintupling is necessary for proper operation of the display.

For instance, let's take the example of a 1/32 multiplex display operating from a battery with 1.8 V. The operational temperature of the module must range from -20° to 70°C. This range, with a commonly available fluid, can be realized with approximately 8.5 V. A voltage quintupler is necessary to generate the required LCD driver voltage. With a 2.7-V-minimum voltage supply, a voltage quadrupler is necessary to properly drive the LCD fluid.

Driver Functionality

As the state of the art in submicron photolithography continues to generate ever smaller structures, more functionality can be placed onto an LCD driver chip. Gone are the days when a separate controller and separate row- and column-driver chips were necessary to realize a display module. In fact, the chip is becoming pad limited before 100% of the silicon functionality is used.

Only the number of outputs that are

put into the driver chip limits the functionality of the chip. In many cases, this number is now over 300 outputs per die for a TAB or COG implementation

Backlighting

The typical small, handheld backlight consists of a light pipe, diffuser material, and an LED light source. Generally made of polycarbonate material, the light pipe serves two functions in the display. First, it efficiently disperses the light from the LED sources to illuminate the display. Secondly, it provides mechanical structure for the display glass and pc board (*Fig. 6*).

The light from the LED sources must be efficiently dispersed throughout the light pipe to provide uniform illumination at the surface of the light pipe. Several techniques are employed to diffuse the light sources so that hot spots and non-uniform area illumination is kept to a minimum. Microstructures are usually molded into the light pipe to diffuse the light into a uniform pattern. Additionally, materials can be placed into the light pipe to diffuse the light as it encounters these particles in the light pipe itself.

In some applications, a diffusing material is placed on the rear surface of the light pipe. The diffusing material acts to redirect the light upward to the surface of the light pipe, where a non-uniform surface treatment further diffuses the incoming light rays.

When the diffusing material is placed on the surface of the light pipe, between the pipe and the display, the incoming light rays are reduced in intensity and scattered at the surface of the diffuser material. In practice, both methods of diffusing the LED light are employed, and application specific as to their relative performance.

Light Pipes Doing Triple Duty: In hand-held display modules, weight is a key consideration. Thus, any dual or triple functionality that can be realized from existing mechanical components is mandated. With this in mind, the light pipe serves to take on a few more functions than just light distribution.

First, the light pipe serves to anchor the glass (*Fig. 6, again*). Features can be molded into the light pipe, which will capture the glass and hold it in place. This is especially useful in the vibration environment. The mass of the display glass is usually insufficient to deform or

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break the features clamping the glass to the light pipe. The light pipe provides the necessary support to keep the glass in place during vibration and shock.

The light pipe also is used to anchor the pc board. Using a heat-seal connector type of electronic module, the pc board can be wrapped around to the other side of light pipe. Features are molded into the light pipe, which hold the pc board in place. As with the glass, the pc board is held in place during shock and vibration.

Finally, the light pipe is used to hold the entire display module in place within the housing. Tabs, rings, holes, or other features can be molded into the light pipe to allow alignment of the module into the housing. These features can also serve as positive connection points between the housing and the display module. Special consideration must be given, however, to these points as mounting features.

While the mounting features on the light pipe may be strong enough to hold the display module in place during vibration or shock, they may not be strong enough to prohibit deflection of the display module when impacted by other mechanical components within, or external to, the housing.

Experience shows that the housing must be designed to prevent deformation of, and deflection into, the display module. The most common occurrence is glass breakage due to direct impact of a housing feature on the display module. The display module/housing interface must be adequately designed and modeled to prevent high-mass components from coming into contact with the display module. As an additional precaution, the mounting features of the display module, most notably ring or pin structures, must be modeled to prevent stress fractures from occurring over time. This stress leads to premature fatigue of the display module.

Michael G. Petera is the director of Advanced Design Concepts at Three-Five Systems Inc. Since 1988 he has been involved in the design and development of small- to medium-complexity LCD modules for high-volume applications. He graduated with a BSEE from the University of Wyoming, Laramie, Wyo. in 1978, and holds a patent in LCD technology. He is also a member of the Society for Information Display.

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Manufacturer	Device	Description	Price and delivery	CIRCLE
RESISTORS				
IRC, Advanced Film Div. Corpus Christi, TX 78411 Steve Wade (512) 985-3140 Fax (512) 992-3377	LRF Series current-sensing devices	Implemented in a flip-flop format, these precision, current-sensing devices have a resistance range of 1.0 Ω down to 0.01 Ω , and tolerances to $\pm 1\%$. Screen-printed and terminated only on one side, the devices are designed to be mounted face down on the pc board. They are rated at 1W at 70°C, have a TCR of ± 100 ppm/°C, and have an operating temperature of -55° to 150°C.	\$0.20 each per 10,000; stock to four weeks	525
	WCA and WCC chip arrays	These thick-film, resistor chip arrays feature four isolated resistors in a square-cornered, 3.2- by 1.6-mm termination array. The convex style WCA comes in a 0804 package, while the concave WCC uses a 0804 package. The devices have resistance values of 10 Ω to 1 M Ω , with 5% tolerance and TCRs of 200 ppm/°C.	\$0.03 each per 5000; stock to six weeks	526
ISOTEK Inc. Swansea, MA Bill Poisson (508) 673-2900 Fax (508) 676-0885 tekinfo@isotekcorp.com www.isotekcorp.com	PMC four-terminal sense resistor	Designed for precision current sensing in power modules, motor controllers, and power supplies, these devices come with resistance values of 1 to 3 m Ω $\pm 1\%$, at a continuous power rating of 3 W. The PMC operates over the temperature range of -55° to 125° C with a TCR of 30 ppm/°C from 20° to 60° C.	\$1.20 each per 10,000	527
Noble U.S.A. Inc. Rolling Meadows, IL Sales Dept. (847) 364-6038 Fax (847) 364-6045 www.nobleusa.com	XVB93 Series rotary potentiometer	This series of 9-mm, panel-mount, rotary potentiometers have a right-angle profile height of 6.5 mm. Available with a resistance range of 10 to 100 kW, with audio, linear, and reverse audio tapers, the devices are rated at 0.05 W, with a maximum rated voltage of 50 V ac or 10 V dc. Options include single, dual, or multiple sections, and single or	\$0.70 each per 1000	528
AVX Corp. Myrtle Beach, SC Sales Dept. (803) 946-0414 Fax (803) 448-1943 www.avxcorp.com	Accu-P Series 0402-size microwave capacitor	Offered as the first RF/microwave capacitors in an 0402 package, these devices come with a capacitance range from 12.0 pF down to 0.1 pF. Tolerances vary from ± 0.05 pF up to 5.6 pF, to ± 0.1 pF from 5.6 to 10 pF, up to $\pm 1\%$ above 10 pF. Rated voltages range from 10 to 50 V dc, with a temperature coefficient of ± 30 ppm/°C. The ESR, SRF, and Q values are	\$0.15 each; stock to 16 weeks	529
	IDC Series interdigitated, low-inductance capacitors	Offering inductance values as low as 175 pH, these FR4, pc-board-mounted capacitors are designed for operating frequencies above 300 MHz. Available in 0612 sizes, the devices come in values of up to 2.2 μ F at 10 V and 0.22 μ F at 16 V, with tolerances of $\pm 20\%$ in X7R dielectric.	\$0.30 each per 10,000; stock to 14 weeks	530
Seacor, Inc., Westwood, NJ Sales (800) 662-7322 Fax (201) 664-8544	PUK series motor-run capacitor	UL 812 recognized to 10,000 A fault current, these motor-run capacitors come with values ranging from 1.0 to 25.0 μ F, and are rated at 250 to 500 V ac. Designed for one- or three-phase induction motors, these devices replace any dry, metallized-polypropylene, ac motor-run capacitors.	\$0.40 each in quantity; six to eight weeks ARO	531
Tecate Industries, Inc. Poway, Ca Sales Dept. (619) 513-2300 Fax (619) 513-2345	Type MPX metallized polypropylene film	Class X2 interference suppression, metallized polypropylene film capacitors come with eight international approvals, including UL, CSA, and VDE. Include an operating temperature range of -40° to 85°C, a capacitance range of 0.0047 to 1.0 μ F with tolerances of $\pm 5, 10, \text{ or } 20\%$, and a voltage rating of 275 V ac. Sizes range from 13.0 by 11.0 mm to 37.0 by 24.0 mm.	\$0.15 each per 1000; stock to eight weeks	532
	Type 701 aluminum electrolytics	Axial, aluminum electrolytic capacitors have a load life of 1000 hours at 85°C, and are antisolvent. The devices come in case sizes ranging from 5 by 13 mm to 25 by 50 mm, with values ranging from 0.47 to 15,000 μ F. The operating temperature ranges from -40° to 85°C or -25° to 85°C, depending on the voltage rating, which ranges from 6.3 to 450V. The capacitance tolerance is	\$0.06 each per 5000; stock to 10 weeks	533
INDUCTORS				
Cal-Chip Electronics Inc. Warminster, PA Sales Dept. (215) 672-5500 Fax (215) 672-5501	WB Series, high-frequency SMD inductors	Available in EIA case sizes of 0805 and 1008, these high-frequency, surface-mount devices come in a range of inductance values from 2.20 nH to 10.0 μ H. The devices use ceramic construction and a nonmagnetic coil, and have an operating temperature range of -55° to 125°C. Tolerances are 5, 10, or 20%.	\$0.14 to \$0.21 each in quantity; from stock to eight weeks	534
Prem Magnetics Inc. McHenry, IL Derek Brooke (815) 385-2700 Fax (815) 385-8578 www.premmag.com	SPW-1000 series pc-board transformers	Rated at 2.5 VA, these pc-board-mounted power transformers have a range of agency approvals, including VDE 0305, UL 1950, 1446, 1585 Class II and III, and CSA 22.2 #66-1988. The device uses a three-flange-bobbin construction, have distinct, separately isolated windings, and are hi-pot tested to 4500 Vrms.	\$3.03 each in quantity	535
Toko America Inc. Mt. Prospect, IL Sales Dept. (847) 297-0070 Fax (847) 699-7864 www.tokoam.com	PTL Series chip inductors	Targeting VCO, GaAs amplifier-matching, and notch-filter applications, these photolithographically etched chip inductors have a temperature stability of 150 ppm/°C. Part of that series, the PTL2012 has an 0805 footprint with an inductance range of 1.0-39 nH, and is packaged in tape-and-reel format.	\$0.17 each per 50,000	5362

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READER SERVICE 137

See Duracell at
Hall 26 Stand A12

Miniature Color CCD Camera Has DSP And RS-232 Control

The KP-D8 color CCD camera, which measures 22 by 22 by 86 mm, uses the company's own DSP technology. One of its main features is an optional remote control via an RS-232 port. Housed in an all-metal case, the camera has a total of 410,000 pixels and a minimum sensitivity of 4 lux at f1.2. The DSP provides automatic 2H enhancement, automatic aperture correction, backlight correction, and three white-balance modes. Pricing is \$1150 each.

Hitachi Denshi America Ltd., 150 Crossways Park Dr., Woodbury, NY 11797; (516) 921-7200; fax (516) 496-3718. **CIRCLE 537**

Modulated Reflective Sensor Is Highly Sensitive

The OTM930 is a modulated reflective sensor that can sense black paper at distances as short as 0.10 in. or reflective surfaces up to 20 in. or further

away. Designed for ambient light conditions up to 4000 lux, the sensor employs an 880-nm infrared LED and a modulated photo integrated detector combined into an industry-standard package. Only a single external resis-



tor is required for operation. The device operates off a 4.5- to 12-V supply and has a radiant intensity of 20 mW/sr and a spectral bandwidth of 80 nm. Installation is helped by a 16-in. wire cable that's terminated with a seven-pin Molex connector. The operating temperature range is -25° to 60°C. Pricing is \$13.87 each per 100.

Opto Technology Inc., 562 Chaddick Dr., Wheeling, IL 60090; Tom Hegberg (847) 537-4277; fax (847) 537-4785.

CIRCLE 538

10.4-in. TFT Color Display Offers High Brightness

Targeting medical, office, and factory instrumentation, the AND10C209A-HB is a 10.4-in., color, TFT display with a brightness of 250 nits (cd/m²). Driven by a six-bit digital bus, the display generates 256,000 colors on its 640- by 480-resolution screen. The dot pitch is 0.33 mm arranged in a stripe pattern. The display runs off 5 V and consumes 125 mA, while the optional CCFL backlight requires 12 V at 600 mA (typical). Other features include a response time of 50 ms each for on and off, a weight of 590 g, and an active area of 211.2 by 158.4 mm. Pricing is \$770 each per 500.

Purdy Electronics Corp., 720 Palomar Ave., Sunnyvale, CA 94086; Brian Platt (408) 523-8200; fax (408) 733-1287. **CIRCLE 539**

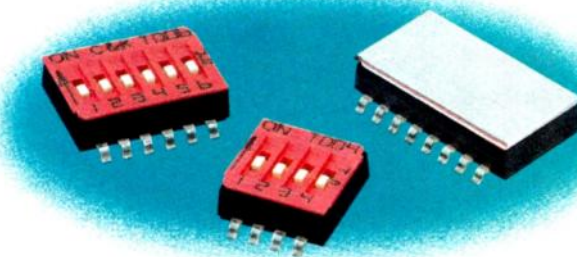
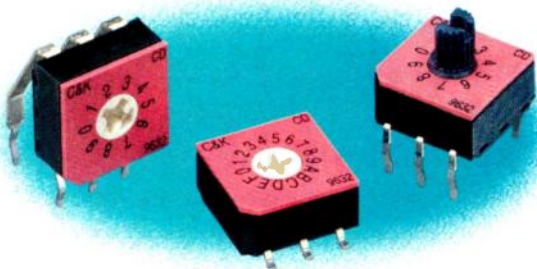
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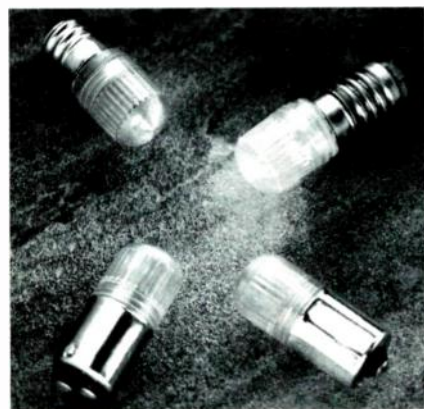
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High-Intensity LEDs Have A Wide Viewing Angle

Available in any voltage from 5 to 120 V ac, dc, or bipolar, the DDP 502 series of LED lamps use a 0.59-in.-diameter clear Fresnel lens to maximize viewing angle and light dispersion. The devices come in red,



orange, amber, green, and blue, with luminous intensities (in millicandela) and viewing angles of 900/30°, 1300/30°, 1300/30°, 1200/45°, and 325/45°, respectively. Designed to replace T 4-1/2 candelabra-style bulbs, the lamps take up to 100,000 hours to degrade to half brightness. Base styles are screw, bayonet, and double-contact bayonet. Pricing for the red, orange, and amber versions is \$8.39, while the green and blue versions are \$10.76 each per 1000. Delivery is from six to eight weeks.

Data Display Products, 445 South Douglas St., El Segundo, CA 90245-4630; Sales Dept. (800) 421-6815; fax (310) 640-7639. CIRCLE 540

Infrared Emitter Exhibits High Output Power

The CLE330E is a double-double-heterostructure junction infrared emitter that emits in the 850-nm range with a power of 20.0 mW at $I_F = 100$ mA dc. The typical total power output at $I_F = 1.5$ A is 300 mW, with a 100- μ s pulse at a 0.1% duty cycle. Mounted in a TO-46 header and encased in a water-clear epoxy dome, the device has an operating temperature range of -55° to 100°C. The modulation frequency is in excess of 10 MHz. Pricing is \$1.92 each per 1000; delivery is two to three (continued on page 110)

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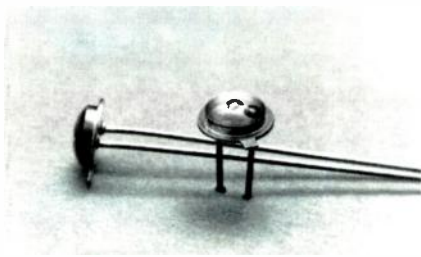
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OPTOELECTRONICS

(continued from page 109)

weeks. Samples are available from stock.

Clairex Technologies Inc., 1845 Summit Ave., #403, Plano TX 75074; (972) 422-4676; fax (972) 423-8628; www.clairex.com.

CIRCLE 541

Silicon Photodiodes Deliver Over Wide Temperature Range

The S6626 and S6838 silicon photodiodes have an operating temperature range of -40°C to 110°C . With a spectral response range of 320 to 840 nm and a peak sensitivity at 540 nm, the devices have a photosensitivity of 0.27 A/W.

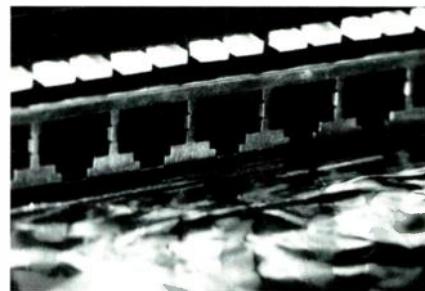
The dark currents and rise times for the S6626 and S6838 are 25 pA and 10 μs , and 10 pA and 2 μs , respectively. Pricing for the S6626 and S6838 is \$10.87, and \$10.68, respectively. Delivery is one week.

Hamamatsu Corp., 360 Foothill Rd., Box 6910, Bridgewater, NJ 08807; (800) 524-0504; fax (908) 231-1218.

CIRCLE 542

LEDs Give RJ-45 Jacks Direct-View Indication

The PCB-1185 series of LEDs come in a profile and format suitable for mounting over RJ-45 jacks to give indication without the need for light pipes. Configured in units of two LEDs per housing, the devices are mounted at right angles and come in colors of orange, high-output red, or blue, or high-efficiency red, green, or yellow. The devices feature co-planar alignment and UL94-V2 flame-retardant nylon 66 housing. Pricing with two LEDs per housing is \$0.88 each per 1000; delivery is 30 to 45 days.

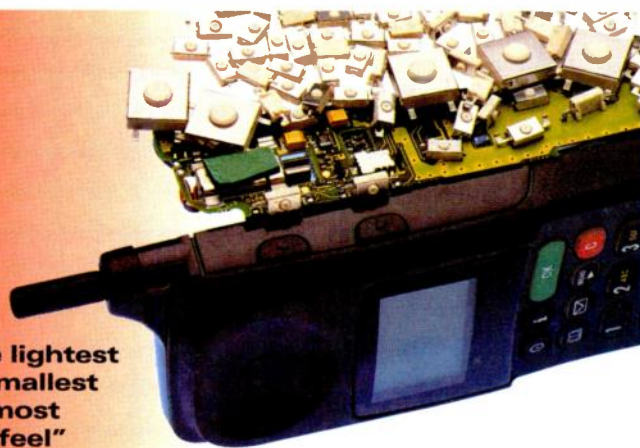


Samples are available in one to two weeks.

Ledtronics, 4009 Pacific Coast Hwy., Torrance, CA 90505; (310) 534-1505; fax (310) 534-1424; Internet: www.ledtronics.com. **CIRCLE 543**

High-Speed Sensor Offers Reliability And Low Cost

Designed for material handling, package distribution, and conveyor-monitoring applications, the SVP Series photoelectric sensor features micro-processor-based circuitry and an operating temperature range of -20° to 125°C . (*continued on page 112*)



Grayhill's Series 95 offers the lightest weight, smallest size and most positive "feel" of any tact switch.

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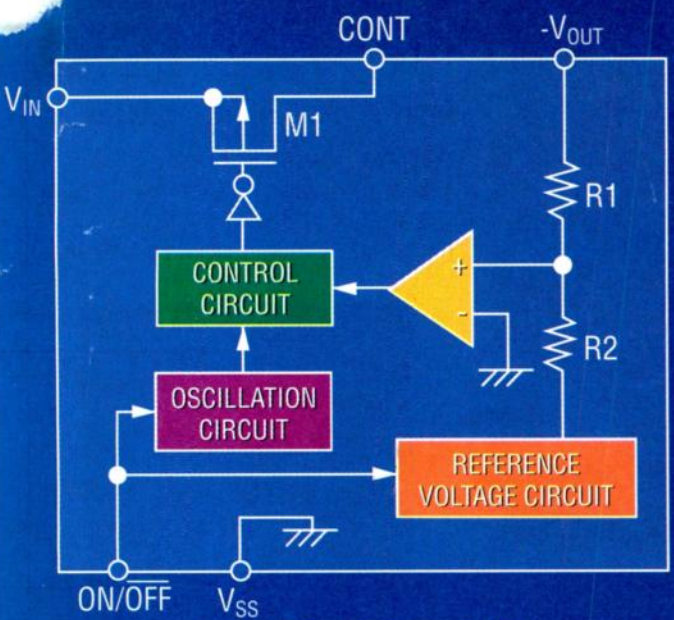
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INC.

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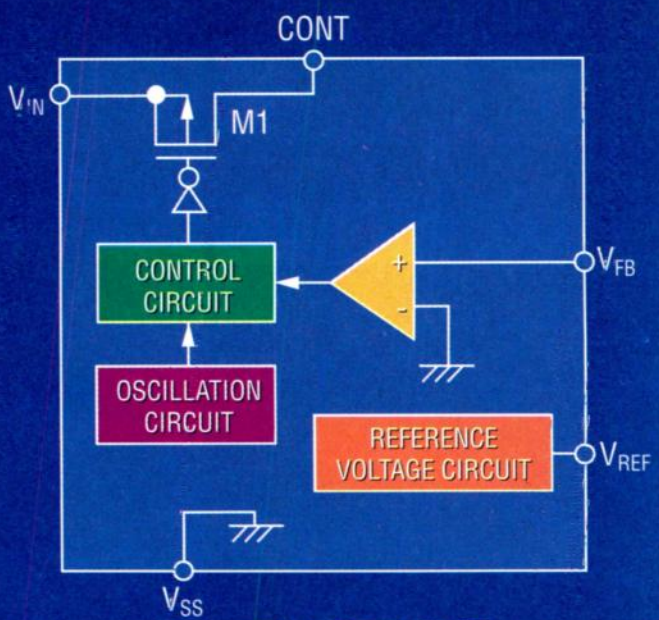
561 Hillgrove Avenue

P.O. Box 10373

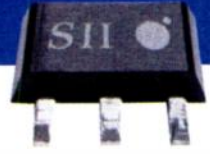
LaGrange, Illinois 60525-0373 USA



S-8437AF

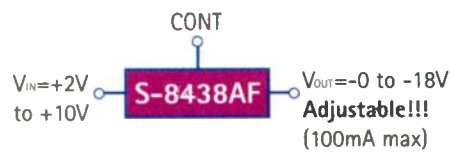
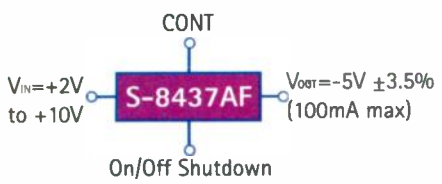


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- Wide input voltage range: +2V to +10V
- Output current to 100mA
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- Built-in power MOSFET
- Temp = $-40C$ to $+85C$
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- Only \$1.05 @ 1K!!!

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World's lowest current consumption:

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- Wide input voltage range: +2V to +10V
- Output current to 100mA
- Built-in RC oscillator (50kHz)
- Built-in power MOSFET
- Temp = $-40C$ to $+85C$
- Tiny SOT -89 (5 pin) package: 4.5 x 2.5 x 1.5mm
- Only \$1.05 @ 1K!!!

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- Calculators
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- Hand held terminals

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READER SERVICE 108

(continued from page 110)

55°C. The sensor accommodates light and dark operating modes, can sink or source current, and features green power- and red output-indicator



LEDs. Both connector and preleaded termination styles are available. Approvals include IEC, UL, CSA, CE, and C-Tick. Pricing is \$46 to \$58, and delivery is from stock.

Honeywell, Micro Switch Div., 11 W. Spring St., Freeport, IL 61032; (800) 537-6945; fax (815) 235-6545; www.honeywell.com/sensing.

CIRCLE 544

6.4-in. Active-Matrix Display Has High Resolution

The V-LCD6.4 is a 6.4-in. black-and-white TFT LCD monitor with a display format of 960 by 234 pixels. Measuring 61.5 by 4.72 by 0.56 in., the

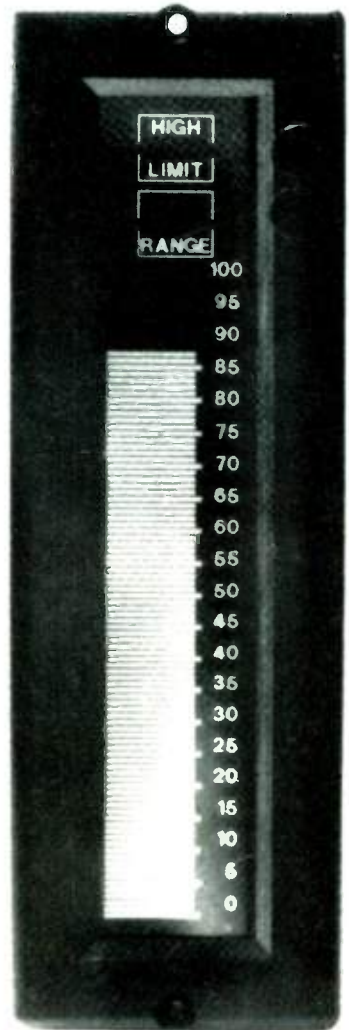


display runs off 12 V dc, requires 500 mA, and is available in NTSC or PAL versions. Options include cabinet mounting and/or speakers. Pricing is \$379 each per 100.

Marshall, Optical Systems Div., 5649 Mesmer Ave., Culver City, CA 90230; Nathan Mordukhay (310) 390-6608; fax (310) 391-8926; www.mars-cam.com. **CIRCLE 545**

Internal Bar Graph Replaces Analog Power Meters

The Model 578 uses an internal true RMS-to-dc multiplier to display the V-by-I product. Requiring no power sup-



ply, the device has high and low alarms, a 101-segment LCD bar graph, and an optional backlight. Over- and under-range limits are standard and adjustable. The device has a 90- to 500-V ac range option, an accuracy and linearity of $\pm 1\%$ full scale, and a maximum power consumption of 1 W. The bar graph can be vertically or horizontally mounted and comes in a NEMA 3 or NEMA 4X enclosure. Pricing is \$300 and delivery is stock to four weeks.

OTEK Corp., 4016 E. Tennessee St., Tucson, AZ 85714-2130; Otto Fest Jr. (520) 748-7900; fax (520) 790-2808. **CIRCLE 546**

LinearSolutions



Power

December 1997

Single Cell Li-Ion Step-Down DC/DC Converter

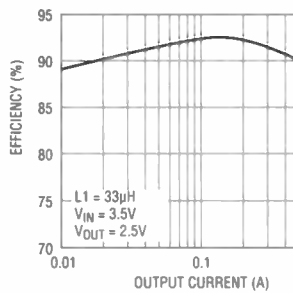
NEW!



The **LTC1626** is the industry's first step-down DC/DC converter that operates over the entire voltage range of a single Lithium Ion cell. Its 2.5V to 7V supply range allows the LTC1626 to maximize battery life while maintaining excellent output regulation. An internal P-channel MOSFET allows load currents up to 600mA with up to 95%

efficiency and 100% duty cycle operation allows extremely low dropout voltage. The LTC1626 incorporates Burst Mode™

operation to optimize efficiency at light loads, consuming just 160µA in standby and less than 1µA in shutdown.



Features:

- 2.5V to 7V supply range
- Low Q current: 160µA in standby, 5µA max in shutdown
- 100% duty cycle for low dropout operation

Circle No. 212

LTC1626: \$3.50 ea. for 1K-piece Qty.

Dual Input UPS Low Dropout Regulator

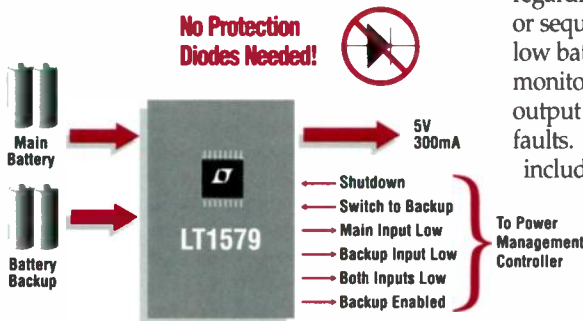
Seamless Switchover From Multiple Inputs

Operating from two independent power inputs up to 20V, the **LT1579** produces an uninterruptible output voltage for loads up to 300mA

with only 0.5V dropout. Automatic or logic-controlled input switching insures that the LT1579 maintains output regulation regardless of input voltages or sequencing. Integrated low battery comparators monitor both inputs and output flags warn of system faults. Other features include reverse battery protection, current limiting and reverse current protection.

Features:

- 0.5V dropout at 300mA load
- 3.5V to 20V supply range
- Control inputs and status flags interface to external logic or microcontroller
- 50µA quiescent current, 7µA in shutdown
- Adjustable and fixed 3V, 3.3V and 5V outputs



Circle No. 214

LTC1579: \$4.15 ea. for 1K-piece Qty.

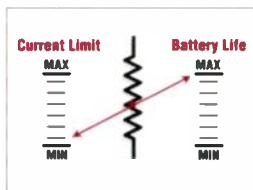
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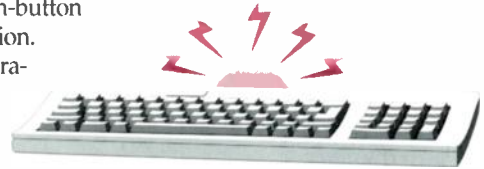
10 μ A I_Q Step-Down DC/DC Converter

The **LTC1474** and **LTC1475** are high efficiency step-down DC/DC converters with only 10 μ A of standby current, and precision programmable peak switch current limit (up to 400mA). The switch current limit peak can be reduced to match the needs of a low output current application. This improves system operating time from a battery supply, particularly Alkaline cells. The internal low-battery comparator is functional during shutdown.

Programmable Peak Switch Current For Extended Battery Life



The LTC1475 version easily implements push-button ON/OFF operation. Industrial temperature range versions are available.



4-cell to 3.3V Wireless Keyboard

Features:

- Very low standby current: 10 μ A typ
- 6 μ A shutdown current
- Adjustable and fixed 3.3V or 5V versions
- Programmable peak switch current limit
- Wide V_{IN} range: 3V to 18V
- High Efficiency: Over 92% possible
- Low battery detector active in shutdown
- Low dropout operation: 100% duty cycle
- Short-circuit protected
- 8-lead MSOP and SO packages
- \$3.40 ea. for 1K-piece Qty.

Circle No. 215

33 μ A I_Q Micropower Boost Regulator

The **LT1316** micropower boost switching regulator has a very low 33 μ A quiescent current and sports a programmable peak switch current limit adjustable from 25mA to 500mA. The shutdown current is just 3 μ A and the internal low battery detector is active in shutdown. The peak current limit is programmable using a low-cost external resistor. The benefit is that the peak current drawn from the battery can be set to match the needs of the load, saving precious battery energy. The LT1316 has a 30V switch

voltage rating permitting high output voltages. These features make the LT1316 an excellent solution for portable battery-powered devices needing boost or SEPIC configurations and the longest battery lifetime.

Features

- 33 μ A quiescent current
- 3 μ A shutdown current
- Programmable peak switch current limit
- V_{IN} as low as 1.5V
- Low Battery Detector is active in shutdown
- 8-lead MSOP or SO packages
- 30V Switch voltage
- Adjustable output voltage



Circle No. 216

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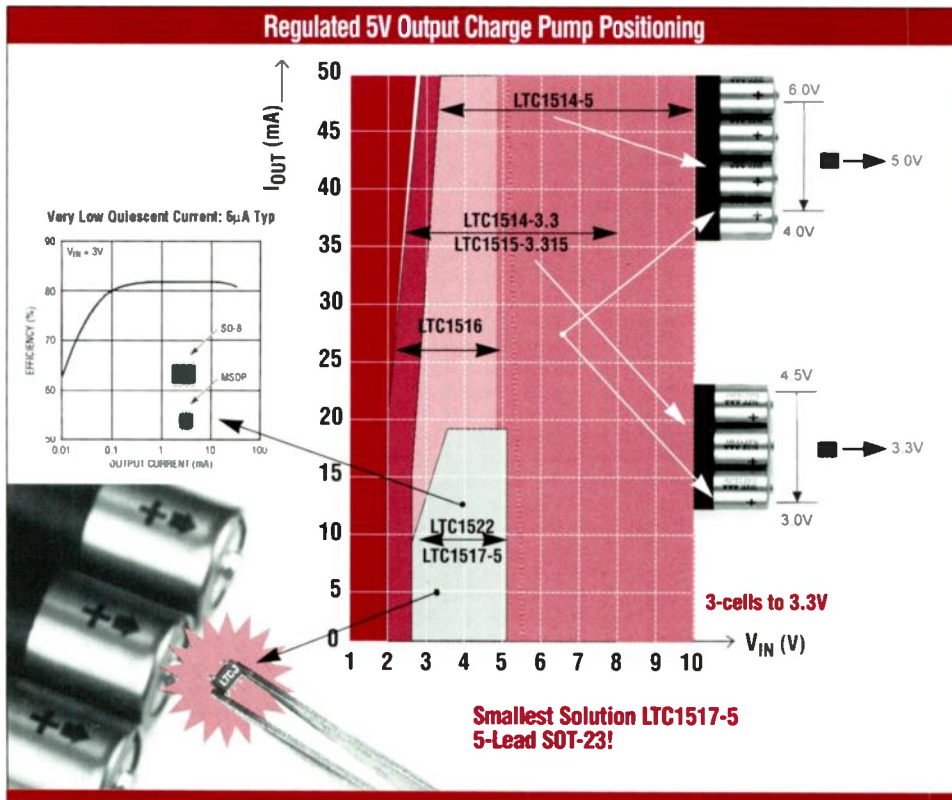
LTC introduces a new family of switched capacitor DC/DC converters with regulated positive output voltage. These new devices allow small PCB footprint solutions with no inductors required! All these devices can boost the input voltage

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Circle No. 217

V _{IN} Range	Step Down	Step Up	V _{OUT}	Output Current	Quiescent I _Q /Shutdown I _Q	Package	Significant Features	Device
2V to 8V 2.7V to 10V	✓	✓	3.3V, 5V	≤ 50mA	60μA / 10μA	SO-8	Low Battery Detector	LTC1514-3.3 LTC1514-5
2V to 8V 2V to 8V 2.7V to 10V	✓	✓	3V/5V, 3.3V/5V, ADJ	≤ 50mA	60μA / 1μA	SO-8	Power On Reset	LTC1515-3.15 LTC1515-3.315 LTC1515
2V to 5V		✓	5V	≤ 50mA	12μA / 1μA	SO-8	Short Circuit Protection	LTC1516
2.7V to 5V		✓	5V	≤ 20mA	6μA / NA	SOT-23	Smallest Size	LTC1517-5
2.7V to 5V		✓	5V	≤ 20mA	6μA / 1μA	MSOP, SO-8	Small MSOP	LTC1522



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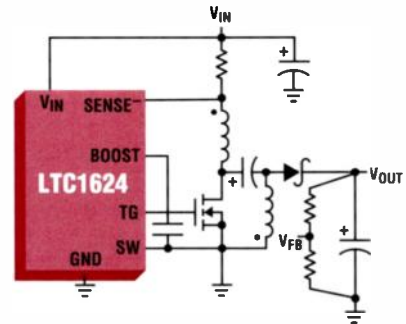


**The LTC1624
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Universal N-Channel Switching Regulator

The **LTC1624** is a current mode switching regulator that drives an external N-channel power MOSFET in all standard switching configurations including boost, step-down, buck-boost (SEPIC), inverting and

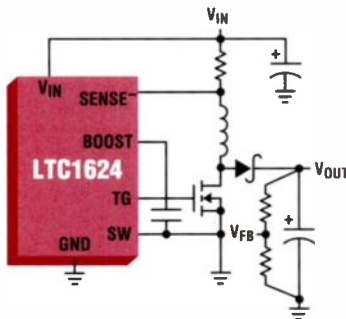
flyback. Its fixed 200kHz operating frequency and 8-lead SO package minimize the total solution size for space limited applications. Operation from 3.5V to 36V allows the LTC1624 to be used in a variety of applications. Burst Mode™ operation provides high efficiency at low load currents and 95% duty cycle provides low dropout voltage for increased operating life in battery powered systems.



SEPIC Converter

Features:

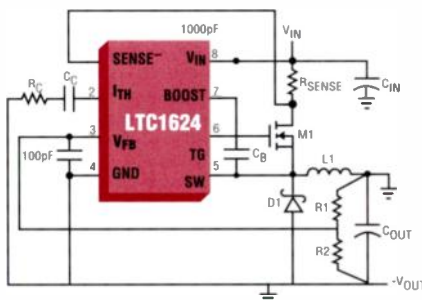
- Wide V_{IN} range: 3.5V to 36V
- Wide V_{OUT} range: 1.2V to 30V in step-down mode
- Low dropout operation: 95% duty cycle
- $\pm 1\%$ 1.19V reference
- Small SO-8 package



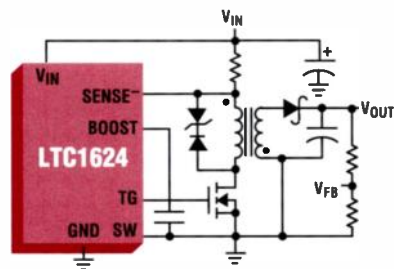
Boost Converter

Circle No. 218

3 Amp Step-Down DC/DC Converter



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Flyback Converter

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Single Cell to 3.3V at 75mA in MSOP Package

The **LT1307** is a micropower 600kHz current-mode PWM boost converter that allows the use of all ceramic capacitors and a small 10 μ H inductor for a very small footprint solution. Its 1V minimum input voltage and low operating quiescent current make the LT1307 an excellent choice for battery-powered applications. The LT1307 is great for hand-held devices using 1, 2, or 3 cells to generate

supplies for 3.3V or 5V logic, 12V flash memory or 28V LCD bias.

Features:

- V_{IN} as low as 1V
- 50 μ A quiescent current
- 3 μ A shutdown current
- 600mA internal switch
- 600kHz PWM with Burst Mode™
- Low Battery comparator
- Uses all ceramic capacitors
- 8-lead MSOP, SO and PDIP packages
- LT1307B is constant frequency at light load



Receive Pager

Cost-effective Solution for 1-, 2-, and 3-cell Applications

Circle No. 219

LT1307: \$2.05 ea. for 1K-piece Qty.

Single Cell to 3.3V at 300mA in SO-8 Package

The **LT1308** micropower, fixed frequency boost DC/DC converter has a 2A switch in an SO-8 package and can generate 3.3V at 300mA from a single NiCd battery. Its adjustable boost output voltage can also be set up to 28V. The LT1308 features a power saving Burst Mode™ to maintain high efficiency over a broad 100 μ A to 300mA load range. The LT1308 is well suited for pulsed high current applications such as two-way pagers, PC Card modems, and digital cameras, as well as GPS receivers and battery backup supplies.

Features:

- Pin-compatible with LT1307 for simple power upgrades
- V_{IN} as low as 1V
- 100 μ A Quiescent current
- 3 μ A Shutdown current
- 600kHz current-mode PWM
- Low Battery Comparator
- 2A switch in an SO-8 package



2-Way Pager

Smallest Footprint High Power Boost Solution Available

Circle No. 220



PC Card Modem

LT1308: \$3.45 ea. for 1K-piece Qty.

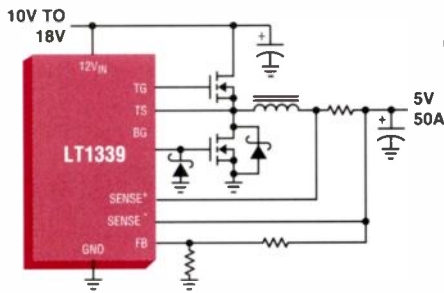
Synchronous Buck Controller Delivers Module Power Without the Cost



The **LT1339** is an easy to use current mode switching regulator controller that can deliver the power of a DC/DC converter “brick” without the high cost. Its robust N-channel synchronous MOSFET drivers can handle up to 10,000pF gate capacitance, making this

device perfect for main-frame computer and network server applications requiring load currents up to 50A. Programmable average current limiting allows accurate control of the DC output current independent of inductor ripple, and the operating frequency can be synchronized up to 150kHz for precise control of switching harmonics.

Other features include user-adjustable slope compensation, soft start and undervoltage lockout.



Also Available:
LT1680: Boost Controller
for high voltage, high current step-up applications

Features:

- High voltage: Operation up to 60V
- High current: N-channel synchronous drive handles up to 10,000pF
- Fixed frequency 150kHz operation, synchronizable
- Programmable average load current limiting
- 20-lead DIP and SO packages

Circle No. 221

LT1339: \$4.85 ea. for 1K-piece Qty.

Flyback Regulator Eliminates Optoisolators

The **LT1425** is a monolithic flyback switching regulator that provides isolated output

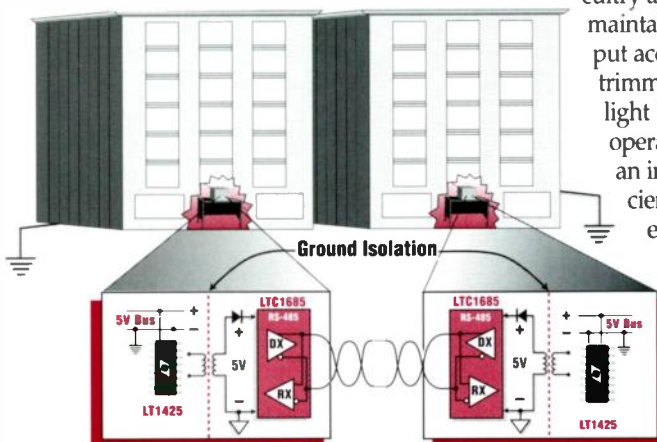
voltages without requiring a third winding or optoisolator. Advanced control circuitry allows the LT1425 to maintain $\pm 2\%$ typical output accuracy without user trimming, even at very light loads. A 275kHz operating frequency and an integrated high efficiency 1.25A switch

enables the LT1425 to deliver output loads up to 6W without any external power devices.

Features:

- No transformer third winding or optoisolator required
- $\pm 2\%$ output accuracy without user trimming
- Resistor programmable output voltage
- Maintains output regulation at very light loads

Circle No. 222



LT1425: \$2.90 for 1K-piece Qty.



For literature only: call 1-800-4-LINEAR

www.linear-tech.com

Ultra Low Noise Switching Regulator



The **LT1533** DC/DC converter produces less than 100µV output noise over a 100MHz bandwidth. The voltage and current slew rates of the internal power switches are user-adjustable,

resulting in dramatically reduced conducted and radiated EMI – up to 40dB lower than most switchers. Finally, a switching regulator that can coexist with noise-sensitive applications such as precision instrumentation and wireless communications.

Features:

- Controlled voltage and current slew rates
- 20kHz to 250kHz fixed frequency operation, synchronizable
- Regulates positive and negative output voltages

Up to 40dB Lower Conducted & Radiated EMI Than Most Switchers

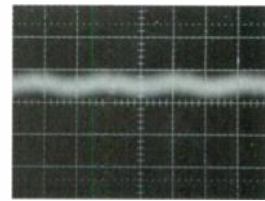
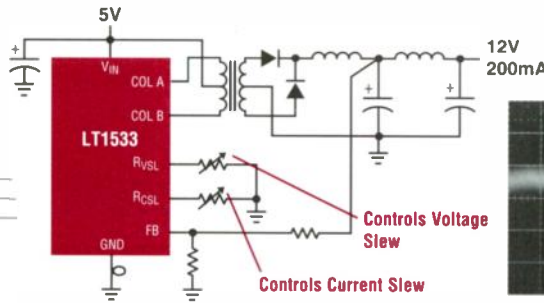
Precision Data Acquisition



Wireless Communication



Medical Instrumentation



Circle No. 223

LT1533: \$4.95 ea. for 1K-piece Qty.

6A, 500kHz Switching Regulator Saves Space

The **LT1370** is a high power current mode switching regulator that is ideal for space-limited applications. Its 500kHz operating frequency and low loss 6A/100mΩ internal switch allow the LT1370 to realize up to 90% efficiency using tiny external components. A 2.7V to 30V supply range

permits it to be used in a variety of applications and it can be synchronized to an external clock source for improved management of switching harmonics. The LT1370 is available in 7-lead DD and TO-220 packages.

Features:

- Fixed Frequency 500kHz Operation
- Small inductor size: As low as 4.7µH
- Uses all surface mount components
- Wide input supply range: 2.7V to 30V
- Easy synchronization to external clock

500kHz Switching Regulator Reduces Size of DC/DC Conversion Circuits

BOOST SWITCHING REGULATORS							
Switching Frequency (kHz)	Maximum Switch Current (A)						
	1.25 to 1.5	2.5 to 3	4	5	6	7.5 to 8	10
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60	LT1082		LT1271			LT1270	LT1270A
100	LT1172	LT1171	LT1269	LT1170			
150						LT1268	
250	LT1373						
500	LT1372	LT1371			LT1370		
1MHz	LT1377						

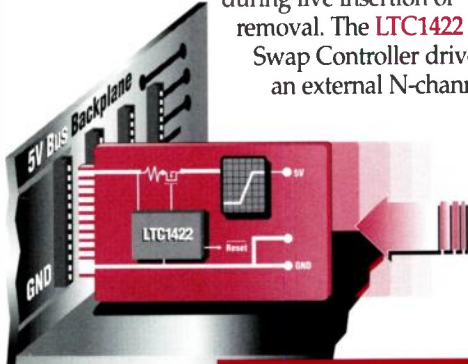


Circle No. 224

LT1370: \$6.15 ea. for 1K-piece Qty

Hot Swap Controller Allows Live Board Insertion

**Simple Control
for Hot Swapping
Circuit Boards**



Protect your board against system errors caused by power supply transients during live insertion or removal. The **LTC1422** Hot Swap Controller drives an external N-channel

MOSFET for a single supply from 2.7V to 12V and is flexible enough to handle -48V applications. Connection sense insures the board is properly seated before the supply ramps up and a supply monitor can be used to generate a system reset when the supply falls below a preset voltage. Ramp rates, reset threshold and current limit levels are all programmable, allowing maximum user control.

Features:

- Controls a single supply from 2.7V to 12V
- External N-channel MOSFET allows design flexibility
- Programmable ramp rates, reset threshold and current limit
- Small SO-8 package, requires few external components

Circle No. 225

LTC1422: \$2.75 ea. for 1K-piece Qty.

Smart Power Management for Dual Input Systems

**Power Path
Management for
Systems with
Multiple DC
Sources**

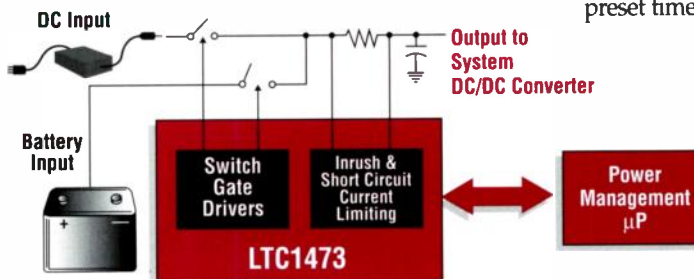
The **LTC1473 PowerPath™** Controller provides a simple power management solution for systems that operate from multiple DC sources. It drives two sets of back-to-back N-channel MOSFET switches to route power from either source to the main system switching regulator without causing system resets. A unique 2-diode

logic mode ensures correct system start-up regardless of the sequencing of the input sources and inrush current limiting ensures seamless operation during switch-over transitions. The LTC1473 also protects against system short circuits using a programmable timer to latch off the switches when the fault exceeds the preset time limit.



Features:

- All N-channel switching to reduce power losses and system cost
- Switches and isolates sources up to 30V
- Capacitor inrush and short circuit current limiting
- Small footprint: 16-lead narrow SSOP package



Circle No. 226

LTC1473: \$3.55 ea. for 1K-piece Qty.

For more details, contact Linear Technology Corporation, 1630 McCarthy Blvd., Milpitas, CA 95035-7417, Web Site: www.linear-tech.com. (408) 432-1900. Fax: (408) 434-0507. For literature only: 1-800-4-LINEAR.



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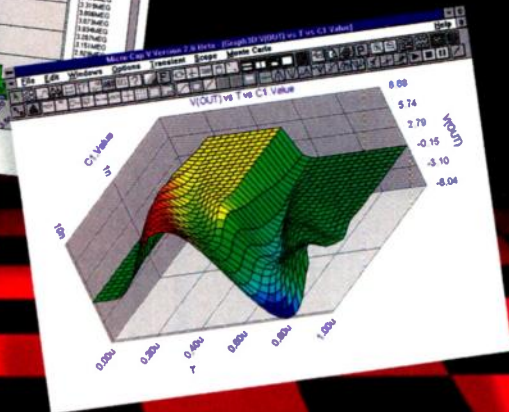
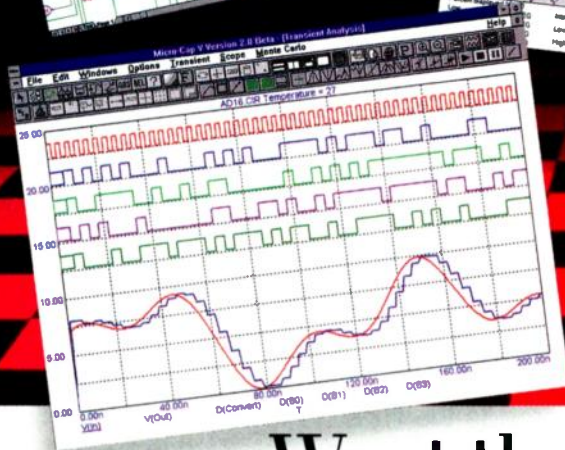
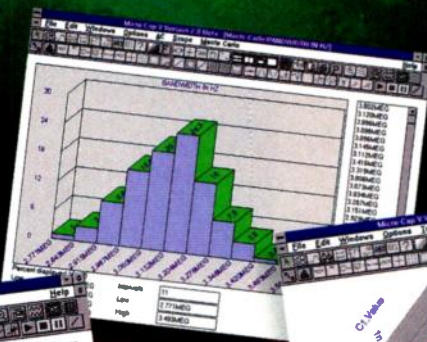
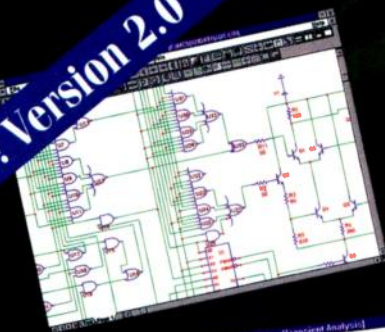
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STANDARDS WATCH

Who Needs All Those Display Standards Anyway?

Bob Myers, Senior Engineer, Displays, Hewlett-Packard Co.

Last year, I read a paper which proposed—among other things—that we no longer have the need for display standards. In fact, it said, we ought to be embracing efforts to move away from such standards as quickly as possible. The notion seemed to be that we should expect displays, and presumably their controllers, to be flexible enough to deal with just about anything, letting the user configure the display system to handle any format desired.

This sounds like a nice idea, although it may have been a bit of hyperbole on the part of that author. But, I'm afraid that there are many people who think that taking this position to its extreme is something we want to be doing. After all, any references to format and rate standards were removed from the recent ATSC proposal for the U.S. HDTV standard. There also appears to be no end to the proliferation of formats and rates our PCs provide. Have we finally reached a point where display standards, specifically format and timing standards, can be abandoned?

Certainly there have been a number of developments in recent years which reduce the need for strict adherence to specific timing standards. The widespread acceptance of the VESA Display Data Channel (DDC) standard and its accompanying ID format standard (EDID) are good examples. They allow plug and play of the display, letting the host configure itself to best drive whatever display device is in use. VESA has also established a method for generating "standard" timings for any arbitrary format and rate on the fly, in the Generalized Timing Formula (GTF) standard. Surely with these

standards being accepted by the industry, there is no need for further work in setting norms for image formats or display timing. Right?

This is most definitely not the case, and to declare that there is no longer a need for such standards ignores some major trends in the industry.

First, we no longer live in a "CRT-only" world. The CRT display is an extremely flexible device, one which easily adapts to a practically unlimited range of possible timings. But the non-CRT displays, which are poised to take over significant portions of the computer display market, are almost all fixed-format devices. We should not expect an extremely large number of different formats for these devices, simply due to the economies of scale. And no matter how well image format conversion can be done, it is still always best to drive these sorts of displays at their native format. For that matter, there's little justification for even trying to do otherwise. Can anyone really come up with a good reason for creating an image at, say, 1056 by 792 pixels, rather than the standard format of 1024 by 768 pixels? How much flexibility is really needed?

Standard timings also involve the standardization of refresh or update rates, in addition to dealing with standard formats. And in the past, there has certainly been a lot more flexibility in this area, again owing to the capabilities of the CRT display and the fact that the rate didn't matter all that much, as long as it was fast enough not to cause problems such as flicker. (The recent trend of promoting higher rates, far beyond those needed to achieve flicker-free images, is another

question entirely.)

Here again, though, the needs of the market are changing. The sources of display images are varied, and go far beyond the PC itself. One example is computer graphics, which represents the merger of TV with PCs. So, we need to use timings which are at least compatible with various image sources.

Just as in the case of format conversion, it doesn't really matter how good rate conversion gets; why do it if there's no good reason to? And again, there is little justification for a huge amount of flexibility. Is there really an advantage to supporting 75-Hz, 76-Hz, and 77-Hz refresh rates?

The key to future standards development is to provide a rich enough set of related standards to address all of these needs, while increasing the likelihood of any given controller or display being able to support them exactly. We must also make sure that the standards for non-CRT displays can be supported by the same hardware that up to now has been designed around the needs of CRT monitors. This includes making sure that both types can be properly driven by compatible standards.

Work is now underway within VESA's Display Committee to develop just such standards, and to bring them to the industry as quickly as possible. This effort will include not only a more complete set of standard CRT timings for the traditional 4:3 formats, but also will address the needs of the new 16:9 and 16:10 displays, those of non-CRT display technologies, and standards aimed at providing the best integration of computer and television imagery.

Bob Myers tracks display technology and standards for Hewlett-Packard's Personal Systems Group, and is the work group leader for the Timing Standards Work Group under VESA's Display Committee. He can be reached at (970) 898-2636. E-mail: myers@fc.hp.com.

It's The Pipelines, Stupid

In February, Sun Microelectronics announced the availability of their Sparc processor cards in the fledgling CompactPCI market, and targeted the telecommunications industry. Then, they waltzed into Ericsson Telecom and snatched a big piece of board business away from the traditional embedded board suppliers. Does this mean that Sun is changing to an embedded strategy?

Quite the contrary. Sun wants to play in the "convergence" and "enterprise computing" markets, both of which are merging through the telecom companies. Sun came and went in the VME board business back in the 1980s. But, they only used VME in their servers and some military commercial-off-the-shelf (COTS) applications. So, why get back into the board business again?

General George Patton made the observation that to conquer Italy, you have to take Sicily first. The Visigoths proved it, the Romans found this to be true, and Italy fell in World War II from invasions launched from Sicily. Sicily is the most conquered nation in history because it's the key to Italy. For Sun, the telecoms are Sicily, CompactPCI is a weapon, and the great convergence market is Italy.

Andy Grove recently disclosed Intel's low-end embedded strategy: "We are using the P6 microarchitecture (Pentium Pro/Pentium II) top to bottom in our product line, but the products are designed specifically for a given segment of computing." The merced 64-bit processor is going high in the enterprise computing space, and a skinny P6 is going low in the convergence market. Intel is selling their application binary interface (ABI) to the telecoms through hundreds of value-added resellers pitching commodity boards and boxes.

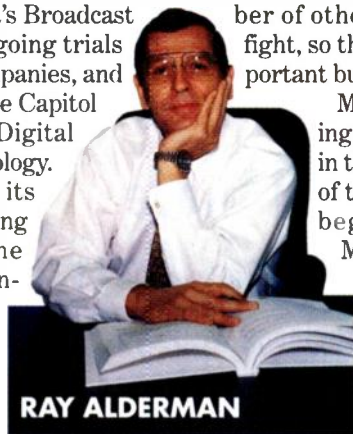
Bill Gates, on the other hand, is trying to establish the CE embedded operating system at the low-end convergence market, while NT is aimed at the high-end enterprise computing market. NT is doing just fine at the high-end. So, he just inked a deal with TCI that insures his place in the set-top-box standards with CE, an-

nounced that Microsoft's Broadcast TV initiative is undergoing trials by 12 major media companies, and has been lobbying at the Capitol for a faster rollout of Digital Subscriber Loop technology.

Microsoft is selling its application programming interface (API) to the telecoms through hundreds of value-added resellers pitching commodity boards and boxes. If Microsoft gets control of the software (the API) in the "pipes" at the telecoms with CE, and Intel gets control of the hardware (the ABI) in the pipes at the telecoms with P6 processors on the processor card, then Sun is dead in the water with Java, Sparc, and Solaris.

When Wintel expands their monopoly from the desktop to the communications channels, they can dictate the characteristics of all the gear that hooks onto the telecoms' pipes, just like they now dictate what hooks onto the PC. World domination would then be complete, and everyone in the convergence market from top to bottom, including the Japanese TV manufacturers and all the enterprise computing companies, would have to add value to Intel hardware and Microsoft software. IBM, HP, and Compaq Computer have all agreed to this deal, but not Sun. The possibility of this scenario happening keeps the lights burning in the Sun buildings in California late into the evening.

Will the PC win the battle against the TV in the convergence market? Yes, because it's prolific and it's already digital. Analog TV has to go digital, and there are at least four processor ABI's competing for digital TV. There's only one API in sight: CE. CE has been ported to the Intel P6 processors, Hitachi SH-series, StrongARM CPUs, and PowerPCs at the low-end of the market. And, Intel has the hardware advantage with their processor ABI monopoly at the high-end of the market. Pentium unit shipments are more than 70 times greater than Sparc unit shipments, and there are a num-



RAY ALDERMAN

ber of other CPU players in the fight, so the hardware issue is important but secondary.

Microsoft has the operating system API advantage in the PC, but CE, a subset of the NT API, is just now beginning to stabilize.

Meanwhile, Java is undergoing a transformation from a language into an operating system API. Sun bought Chorus Systems' real-time

kernel business last year to get into the telecom space, not the traditional bus-board market. If Sun doesn't get into the telecoms' pipes somehow with their Sparc ABI and a new OS-API (Chorus-Java), then Microsoft will control the pipes with CE and NT, Java defaults to a language, and the battle for Italy is lost.

When Microsoft has control of the telecoms' pipes, they can set the pace for new features and services from the wellhead, all the way down to the enterprise computing segment and the digital TV.

Sun's strategy is SparJaTel: the Sparc ABI, the Java API, and the telecom market. Sun is not moving into the traditional bus-board arena with their CompactPCI offerings. They are using CompactPCI boards to move their ABI and API into the telecom markets to keep Wintel from controlling how data goes through the pipes.

It certainly gives a new meaning to Sun's mantra, "The Network Is The Computer." But, their actions have nothing to do with the traditional bus-board markets like the industrial and military segments. Their CompactPCI boards are a tent pitched for protection against an impending hurricane. And, they will pitch a few more technology tents before this storm is over. The Java API is the key to Sicily, and Sicily is the key to Italy. So, it's the pipelines, stupid!

Ray Alderman is the executive director of VITA. He can be reached at (602) 951-8866 or via e-mail at exec@vita.com.

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READER SERVICE 206

World Radio History

Storage Controller Exploits File Array Technology

Array Controller Processes I/O Requests At The File-System Level To Deliver High Throughput And No-Down-Time Storage.

Lisa Maliniak

There's no question that Windows NT is taking the server world by storm. Over 732,000 units were installed in 1996, making it the best-selling server operating system that year. It has not yet, however, achieved a significant presence in the high end of the server market due to several key issues: I/O performance and scalability, information availability, and online storage management.

Adaptec's new FileArray product was designed to address the key issues concerning designers who need to deploy mission-critical applications on Windows NT. The AFA-333 FileArray Accelerator is based on technology introduced last November that offers benefits beyond those found in traditional RAID solutions. FileArray integrates the file system, I/O subsystem, RAID technology, and management software on a fast hardware-accelerator platform.

The product reduces the I/O performance bottleneck presented by traditional storage solutions, and offers a scalable means to boost total system speed. In addition, it offers the critical online facilities that are needed to manage storage resources without interrupting access to data. This capability is essential in commercial computing environments where even seconds of down time are costly.

Enterprise Storage

The FileArray Accelerator is aimed at OEMs designing RAID and enterprise

storage management capabilities into mid-range and high-end servers running Windows NT. The accelerator is also targeted at resellers, integrators, and others who develop storage solutions for mission-critical enterprise computing on Windows NT.

Three components comprise the FileArray Accelerator. First is the PCI-to-SCSI FileArray Accelerator card (see the photo). There's also FileArray software, which includes the file system, RAID software, and drivers for Windows NT servers. Finally, the package includes Adaptec's FileArray Storage Tool (FAST) soft-

ware for online storage configuration and management.

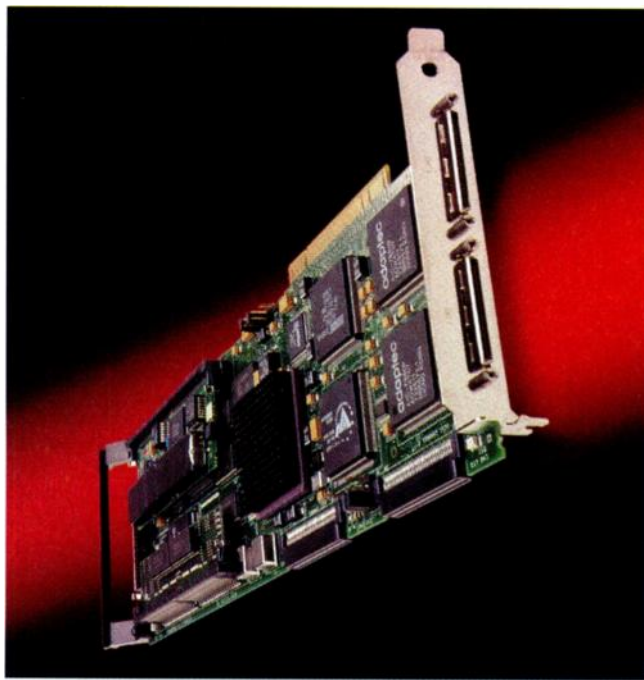
Conventional RAID controllers operate at the block level, and rely on the host server to process file I/O requests. Adaptec's FileArray accelerator takes a fundamentally different approach. It interacts with storage at the file-system level, the same level at which users and applications routinely interact with data. By using this approach, the product enables a more intuitive and efficient approach to storage I/O that increases speed and offloads the host CPU.

Storage Scalability

The FileArray system offers scalability. In the same fashion that compute-bound applications benefit from adding more processors, I/O-bound applications will benefit from adding more FileArrays. This is not true of conventional block-level controllers, in which adding one more controller may only deliver as little as a 10%-to-20% increase in performance.

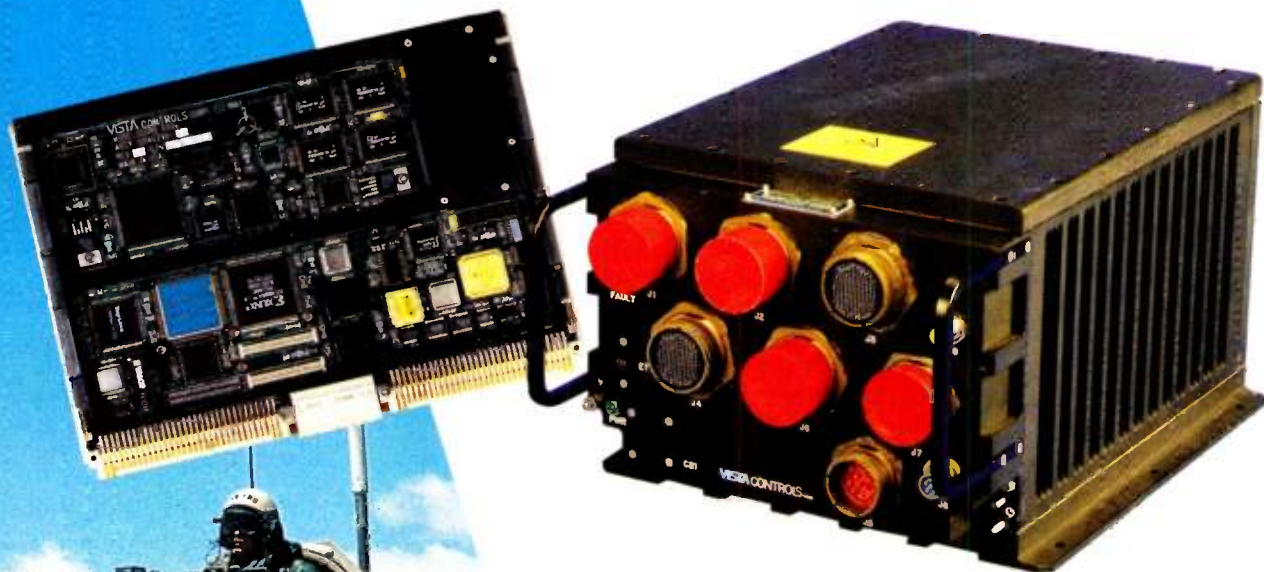
FileArray also relieves the host CPU of the burden of translating file-system requests into block-level requests. The result is increased host-server capacity that can be used to support more users, run more applications, and process more transactions.

Because FileArray integrates the file system and RAID software with the I/O subsystem, it enables system managers to perform storage management operations without ever taking the system down. Users can create, reconfigure, and backup storage resources while systems remain online. This feature is important to IS departments that need to manipulate their storage arrays during normal business



Adaptec's AFA-333 storage controller is based on the company's new file array technology. The product includes the 32-bit PCI-to-SCSI FileArray Accelerator card pictured here. Also included are FileArray and RAID software, Windows NT drivers, and online storage configuration and management software.

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BDS & BUSES CONTROLLER

hours, saving time and maintaining storage availability to users.

The PCI-to-SCSI accelerator card is a 32-bit PCI bus master DMA adapter built with an i960HD-66 microprocessor. The card includes 4-Mbyte, ECC-protected, nonvolatile DRAM; and support for a 16-Mbyte, parity-protected data cache. Its SCSI synchronous data rate goes up to 80 Mbytes/sec, via two independent channels, each of which can support up to 15 disk drives.

The Ultra, Fast, and Wide (both 8- and 16-bit) SCSI protocols are all supported. RAID support is provided for levels 0, 1, 0/1, and 5. In addition, RAID and software drivers are included with the card to provide functionality under Windows NT server applications.

GUI And Wizards

FAST provides a graphical user interface (GUI) and wizards that simplify the creation and management of storage resources. For example, users can create logical disks (containers) and RAID sets very quickly. They can initialize the disks, set up the structure, and lay down the file system in one step. Other features include dynamic online capacity expansion and RAID configuration without reboot, and management for SAF-TE storage enclosures.

The FileSnapshot feature supports online snapshot backup of the containers. There are three modes of operation: FileSnapshot, FileSnapshot with compaction, and FileSnapshot for mirrors. Users can backup during normal business hours because there's no system or information down time.

FAST also includes disk hot swap and failover. The hot-swap feature suspends I/O actions temporarily to allow for disk swap or storage maintenance, such as power-supply replacement. Users can swap any disk at any time, and the new disk is available for immediate use without a reboot of the system. The disk failover feature assigns hot-standby disks, and supports automatic failover for fault-tolerant containers.

PRICE AND AVAILABILITY

The AFA-333 FileArray Accelerator is shipping now through normal distribution channels. Pricing is set at \$2995.

Adaptec Inc., 691 S. Milpitas Blvd., Milpitas, CA 95035; (408) 945-8600 or (800) 442-7274; www.adaptec.com.

CIRCLE 486

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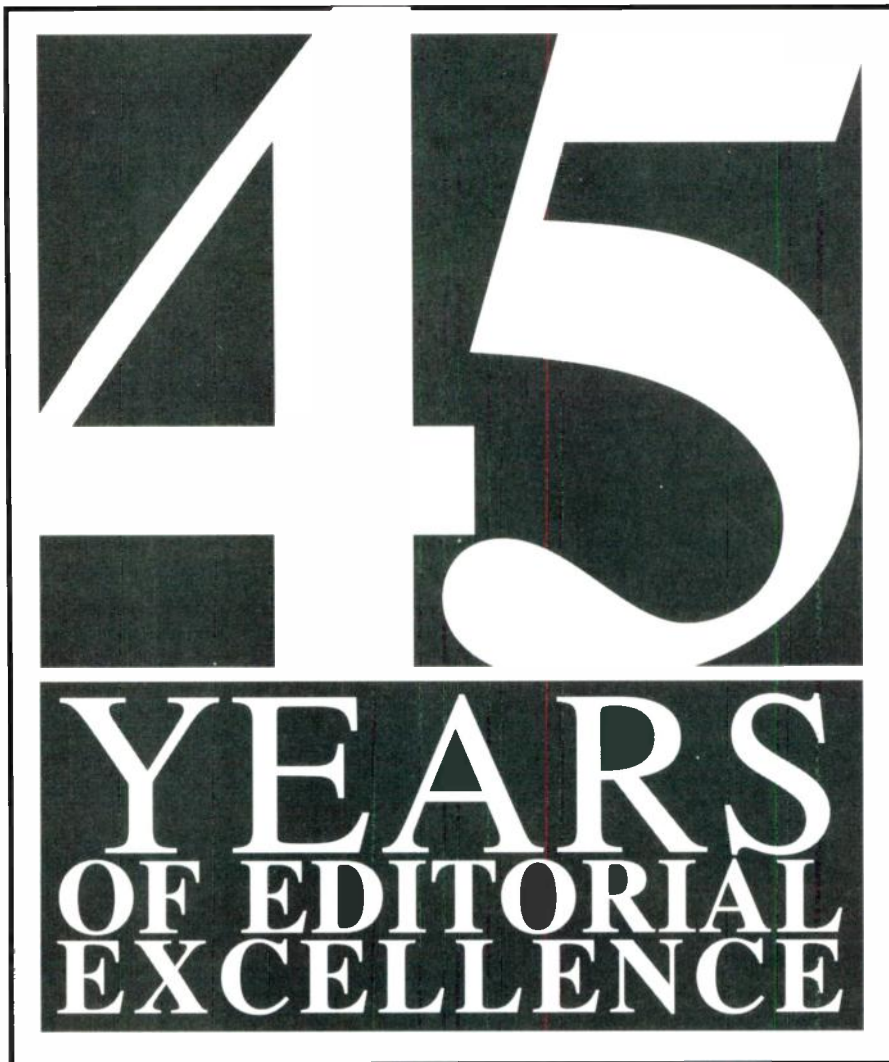
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DVD Drive Functionality Packs Into A Single Chip

High Integration Helps Single-Chip Drive Manager Increase Performance While Reducing Cost And Design Complexity.

Lisa Maliniak

The latest advance in the highly competitive digital-video-disk (DVD) market is a single-chip drive manager that offers a very high level of integration. Cirrus Logic has combined its hard-disk and optical-storage components with mixed-signal and CMOS design experience to create the CR3700 DVD drive manager. It's the first member of the company's emerging family of DVD drive products. The CR3700 integrates most of the necessary components for a DVD-ROM drive, and can also be used in a DVD player.

Cirrus Logic claims it is the first supplier of a single-chip DVD drive solution. The CR3700 combines an RF amplifier, data channel (read channel), servo controller, content scramble sys-

tem (CSS), DVD error correction code (ECC), and a decoder with an ATAPI interface (see the figure). This high level of integration lets the drive manager deliver the functionality currently performed by several chips.

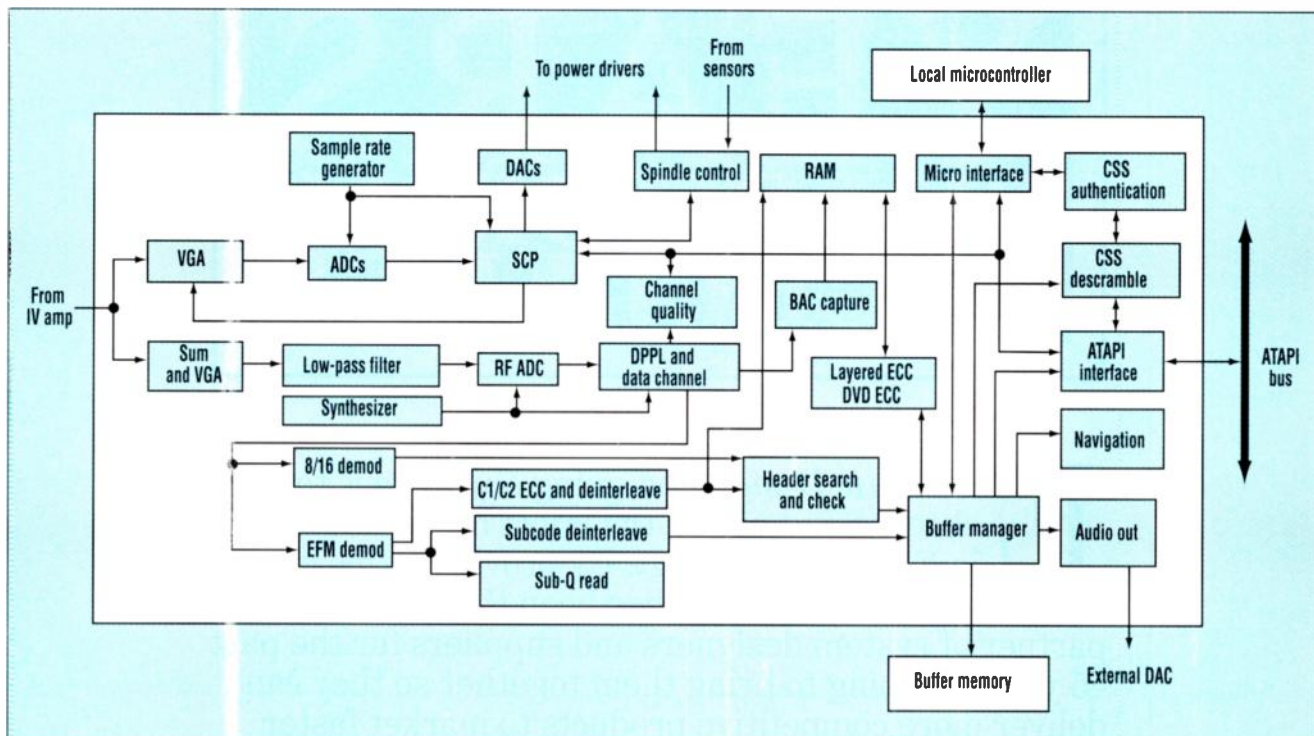
The drive manager can be combined with an audio digital-to-analog converter (DAC), external buffer memory, a local microcontroller, and power drivers to create a complete DVD-ROM solution. In addition, the CR3700 provides a direct interface to MPEG-2 audio and video decoders for DVD-player applications.

Built with 0.35- μ m CMOS technology, the digitally intensive, mixed-signal IC converts analog input signals to the digital domain as quickly as possible.

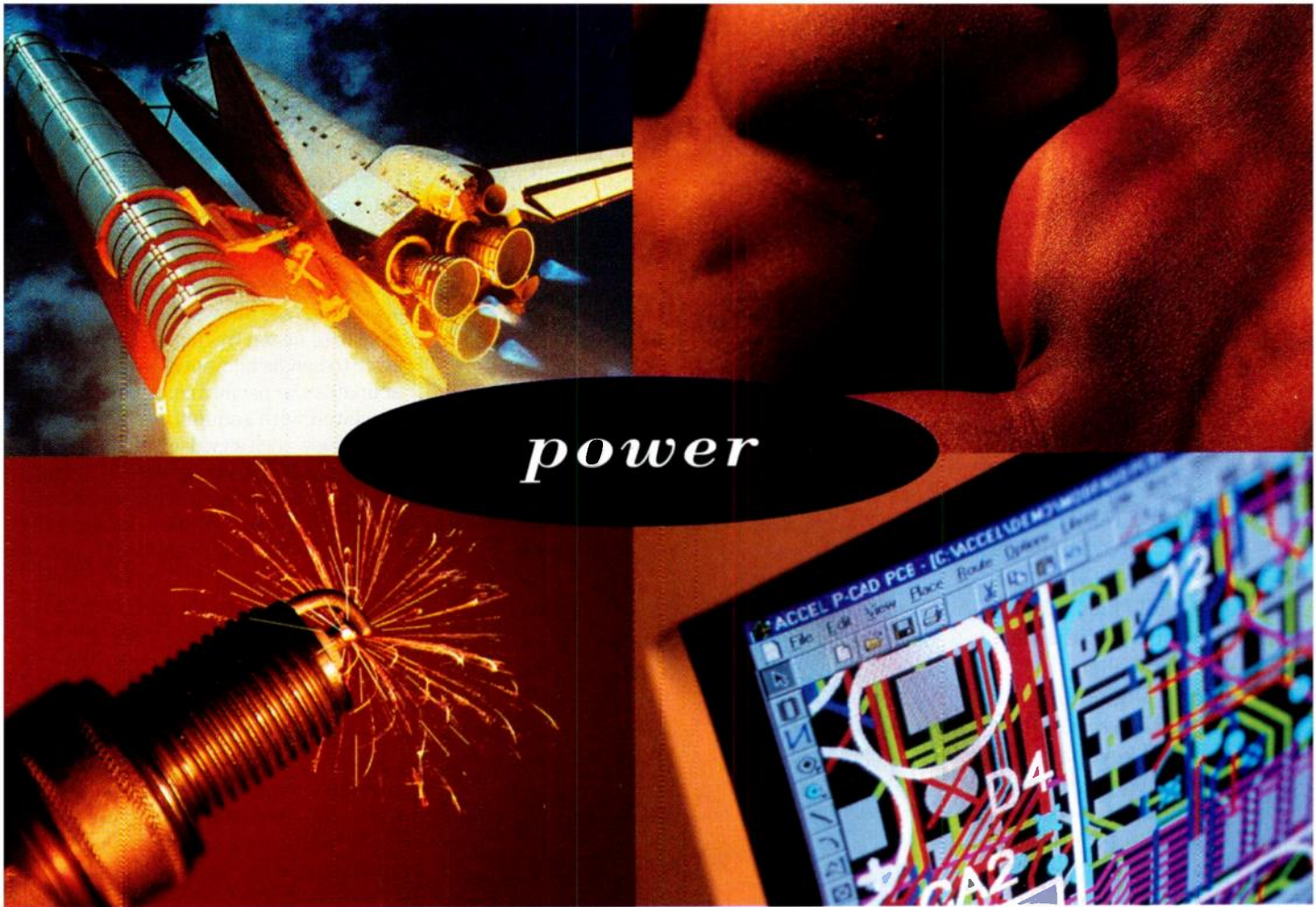
The RF signal is oversampled by a high-speed analog-to-digital converter (ADC). The timing loop is closed in the digital domain, with variable decimation and interpolation used to provide the output samples to the data recovery logic. A channel-quality logic circuit provides for parametric calibration.

In addition to its high integration, the CR3700 also offers designers graphics performance. By supporting 4.5X DVD and 27X CD-ROM data-transfer rates, the drive manager can eliminate problems such as the jagged images resulting from dropped frames. These emerge with high-quality video playback and graphically-intensive multimedia games.

The CR3700 supports the Ultra ATA



This functional block diagram illustrates the high level of integration that's packed into Cirrus Logic's CR3700 DVD drive manager IC. The device contains most of the logic needed for a DVD-ROM drive. It also can be used in a DVD player.



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interface, a requirement of Microsoft's PC '98 design initiative. Ultra-ATA support enables data to be burst from the CR3700 chip to the host at 33.3 Mbytes/s, which is twice as fast as the current non-Ultra solutions. The high-speed interface allows the CPU to retrieve data faster, freeing up processing power to handle additional tasks. It also eliminates the performance bottleneck associated with sequential streaming applications, such as video playback.

The CR3700 integrates Cirrus Logic's read-channel architecture with partial-response, maximum likelihood (PRML) technology. With PRML, analog pulses are quickly converted to digital signals so that the inherent noise generated by the analog signal can be digitally filtered. This technique allows data to be read even with worst-case signal-to-noise-ratio (SNR), significantly improving a drive's overall performance.

A DVD's increased storage capacity—nearly seven times more than a CD—makes it much more susceptible to common disk errors such as scratches, dust, or corrosion. Also, the lower reflectivity of the second layer in dual-layer disks produces more errors. That's why DVD drive manufacturers use ECC technology.

The CR3700 drive manager incorporates a unique asynchronous ECC algorithm that's capable of correcting faulty sectors while it continues to read other sectors. Even at the new chip's maximum 4.5X DVD disk speed, the CR3700's integrated ECC technology is utilized without stopping disk transfers when an error occurs. In addition, the algorithm is powerful enough to support dual-layer DVDs.

The CR3700 is firmware compatible with all Cirrus Logic CD-ROM and CD-Recordable/Rewritable devices. In addition, it will be compatible with future DVD family members, allowing OEMs to preserve Cirrus Logic's firmware code base, reducing firmware development and speeding time-to-market.

PRICE AND AVAILABILITY

The CL-CR3700 DVD drive manager comes packaged in a 208-pin, very-thin quad flat pack (VQFP). Samples are available now, and production volumes will ship in the third quarter. The new DVD drive manager is priced at \$22 each in 10,000-unit quantities.

Cirrus Logic Inc., 3100 W. Warren Ave., Fremont, CA 94538-6423; (510) 623-8300; (800) 359-6414; www.cirrus.com.

CIRCLE 485

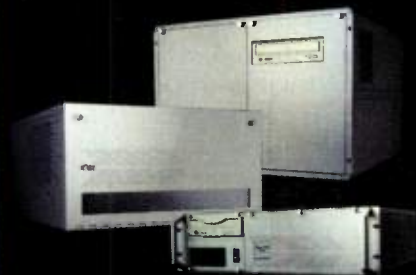


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WHAT'S ON BOARD

Seven CPU board manufacturers are joining with Annasoft Systems, San Diego, Calif., to create an embedded initiative that provides an out-of-the-box Windows CE solution. The initiative will be based on Annasoft's Jump Start kit, a package that provides all driver library software needed to boot and run Windows CE. The initiative's goal is to simplify the development and integration of Win32 applications on embedded platforms running Microsoft operating systems on processor boards based on Pentium or 486 CPUs. Pursuing this are the seven CPU board suppliers—Adastra Systems, Hayward, Calif.; Advantech, Sunnyvale, Calif.; Ampro Computers, San Jose, Calif.; Octagon Systems, Westminster, Col.; Or Industrial Computers, Fairfax, Va.; VersaLogic, Eugene, Ore.; and WinSystems, Arlington, Texas—who hope to leverage the tools to reduce the porting effort to a minimum. The jump-start kit will provide off-the-shelf board customers with an inexpensive, ready-to-run, Windows CE solution that requires little or no OEM abstraction layer adaptation. Each board manufacturer gets a Jump Start Driver Library Kit (DLK). The centerpiece of the kit is Annasoft System's CE Launcher, a utility for certifying Embedded Initiative/Win CE compliance. Residing on the boot media and occupying 11 kbytes, the CE Launcher software enables 486- and Pentium-based embedded PCs to load Windows CE from a rotating or flash disk and execute it out of RAM without MS-DOS assistance. The Jump Start DLK sells for \$1995; run times for CE Launcher cost \$4 to \$6 per copy in OEM quantities. Contact Richard Eppel at Annasoft Systems, (619) 674-6155, or check out the company's web site at www.annasoft.com.

Although Intel Corp., Santa Clara, Calif., had agreed to acquire the StrongArm RISC processor division from Digital Equipment Corp., Hudson, Mass., the license for the ARM architecture was apparently not part of the deal. Intel has secured an agreement with Advanced RISC Machines Ltd., Cambridge, U.K., to produce, sell, and enhance the StrongARM microprocessor family under license. The deal calls for a technology cross-license between the two companies, but is contingent upon the U.S. Federal Trade Commission's approval of the purchase of several semiconductor manufacturing assets in DEC's semiconductor division. Processors included in the agreement are the SA-110, SA-1100, and SA-1500, which DEC has already put into volume production, and forthcoming devices such as the SA-1101 and SA-1501. The availability of high-performance and low-power StrongArm processors opens yet another product door for Intel—Internet appliances, web TVs, web-connected dishwashers, toasters, etc. will also be prime targets for StrongArm CPUs. Contact Intel at www.developer.intel.com.

An enhanced DSP core that delivers a throughput of up to 260 DSP MIPS is the TeakDSPCore, developed by The DSP Group, Santa Clara, Calif. It employs a deeper pipeline so that it can operate at 130 MHz when fabricated on a 0.25- μ m process. The core is a software-compatible follow up to the company's previous two DSP cores, the Pine and Oak. A slight variation of the TeakDSPCore, the TeakLite, was designed for low-power applications, and includes several features that will considerably lower power consumption. Additionally, both cores are designed for use with synthesis tools and can be converted or "ported" into different technologies or moved very quickly to a different foundry using fully-automatic conversion schemes. The core packs several features that allow it to achieve its 260-MIPS peak performance—dual MAC units, new instructions to enhance the performance of major DSP algorithms, double-word memory read/write instructions, fast response for context-switching interrupts, an extended program-addressing space, and enhanced support for operating systems. Both versions of the Teak are backward-code-compatible with the OakDSPCore which eliminates the need to recompile or rewrite existing applications in the first level migration to the new core. For licensing information, contact Yizhar Ganor at (408) 986-4300, or contact the company on the web at www.dspg.com.

CD-ROM Jukebox
Holds 65 Gbytes

On local-area networks, storage is a top priority these days. Designed specifically for LAN use, the BC-MC-1110-AI is a 100-disk CD-ROM jukebox library with a total capacity of 65 Gbytes. The product features two 50-disk removable magazines, one CD-ROM drive, and a SCSI-2 interface. The unit's disk-handling mechanism provides an average disk load time of 3 seconds and an average disk exchange time of 6 seconds. Compatible with all standard CD formats, the BC-MC-1110-AI offers a data-transfer rate of 1.2 Mbytes/s and average access time of 150 ms. Speed is enhanced via a 256-kbyte buffer memory. The product comes complete with jukebox management software that supports hundreds of network users across an enterprise. Available now, the jukebox is priced at \$8995.

JVC Professional, Computer Products Div., 5665 Corporate Ave., Cypress, CA 90630; (714) 816-6500; www.jvc.net. CIRCLE 551

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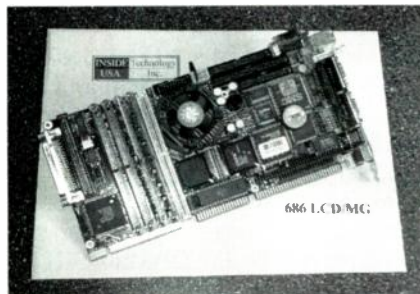
Today's single board computers are squeezing more and more functions onto a single card. Now a new PCI/ISA single-board computer lets designers decide whether to add sound or video. The board comes in two versions. One integrates sound support that's compatible with Creative Labs Soundblaster 16 and Roland MPU401UART mode. The second version integrates an ATI264VT 64-bit PCI graphics accelerator with 2 Mbytes of display DRAM. Both boards support a Pentium II processor of speeds up to 333 MHz and memory up to 256 Mbytes fast page mode or burst EDO DRAM.

Each version uses the Intel 440 series chip sets with a dual bus-master PCI-enhanced IDE interface. The Award flash BIOS has Plug and Play support and is autoconfigurable. Custom setup selection includes control for watchdog timer, master/slave interface, and page mode. The boards are available now for \$600.

Interlogic Industries, 85 Marcus Dr., Melville, NY 11747; (516) 420-8111; www.infoview.com. CIRCLE 552

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The 686LCD/MG is a highly integrated CPU board for embedded control, networking, and multimedia applications. It features an on-board 40-Mbyte/s ultra-wide SCSI interface,



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The board includes a PC/104 connector, up to 512 Mbytes of on-board DRAM, two IDE/EIDE hard-drive interfaces, floppy-disk and keyboard controllers, a PS/2 mouse interface, a flat-panel/CRT video controller with 2 Mbytes of video RAM, one parallel and two serial (RS232/IrDa and 485) ports, a two-channel USB interface, and an optional PanelLink interface (for mounting flat-panel displays up to 30 ft. away). Supporting Pentium MMX technology (optional) with 100- to 233-MHz speeds, it can be ordered with up to 8 Mbytes of on-board flash and up to 72 Mbytes of IDE flash disk. Single-unit price is \$971.86 and availability is now.

INSIDE Technology USA Inc., 8 Prestige Circle, Suite 116, Allen TX 75002; (972) 390-8593; www.inside-usa.com.

CIRCLE 571

**Motion Control Board
Rides Compact PCI**

You know a bus technology is gaining acceptance when special function

boards start to emerge. Following along these lines, the DMC-1600 series of compact PCI motion controller boards uses a rugged Eurocard mechanical configuration. Each card provides up to four axes of motion control and can be used with step motors, servo motors, and hydraulics on a combination of axes.

Among the DMC-1600's features are 80 user-configurable inputs and outputs, and nonvolatile program memory with multitasking of eight programs. The board sports dual high-speed FIFOs for sending and receiving commands, and a secondary FIFO for instant access to status and parameters. Servo rates sample at speed intervals as short as 62.5 μ s per axis. The board does encoder control at up to 12 million counts per second and step motor control of up to 3 million steps per second.

Modes of motion include point-to-point positioning, linear and circular interpolation, contouring, gearing, and ecam. Acceleration and deceleration is *(continued on page 128)*

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(continued from page 127)

programmable and profile smoothing eliminates "jerk." The controller provides continuous vector feed of an infinite number of linear and arc segments to ensure smooth following of complex contours. Enhanced precision is provided with a 16-bit motor-control command output DAC and a sophisticated PID filter. A 2-Mbit flash EEPROM on the board provides storage space of application programs, parameters, arrays, and firmware.

Available now, pricing for DMC-1600 controllers starts at \$995 for single axis, with 4-axis cards priced at \$1245. A starter kit is available for \$100.

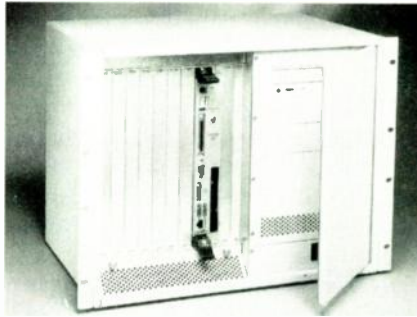
Galil Motion Control Inc., 203 Ravensdale Dr., Mountain View, CA 94043; (800) 377-6329; Internet: www.galilmc.com. **CIRCLE 572**

Compact PCI Chassis Offers Low Cost System Solution

Complete low-cost system integration is what Compact PCI is all about. Ex-

emplifying this trend, the CPX2000 series chassis incorporates a hot-swap enabled backplane, allowing the system to be upgraded to support board-level hot-swap as that technology becomes available.

The CPX2108 version is a rack-mounted Compact PCI chassis. The



6U backplane has a system slot that accommodates CPU boards up to 3 slots wide, plus seven I/O slots with front panel access. Three 5.25-in. drive bays support SCSI or IDE peripheral devices. The CPX2208 version has a similar basic configuration but accepts

IEEE 1101.11-compatible rear transition modules and supports the back-panel I/O scheme required for telecom applications.

Both chassis incorporate Compact PCI connectors with staged pins on the J1 connector. These pins provide power and signal sequencing. That, combined with backplane support for distributed signaling, comprise the hardware needed for a Compact PCI chassis to support minimal and dynamic hot-swap configurations compatible with the latest draft of the PICMG Hot-Swap spec.

Motorola provides a selection of pre-configured starter kits using the CPX2108 chassis. The CPX2108SK1 kit integrates a CPV5000 processor board and Windows NT workstation into the CPX2108 chassis. The CPV5000 sports a 200-MHz Pentium processor, 32 Mbytes of EDO DRAM, on-board IDE hard drive, plus a 3.5-in. floppy drive. The CPX2108K2 version uses a 233-MHz Pentium and adds a 32X CD-ROM drive. Pricing for the chassis starts at (continued on page 129)




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DESIGN NOTES

16-Bit, 333ksps ADC Achieves 90dB SINAD, -100dB THD and No Missing Codes – Design Note 177

Marco Pan and Kevin R. Hoskins

Fastest 16-Bit Sampling ADC

Linear Technology's recently introduced LTC[®]1604 is the fastest, highest performance 16-bit sampling ADC on the market. This device samples at 333ksps and delivers excellent DC and AC performance. The LTC1604 operates on $\pm 5V$ supplies and typically dissipates just 220mW. It has a fully differential input sample-and-hold and an onboard reference. Two power shutdown modes, NAP and SLEEP, reduce power consumption to 7mW and 10 μ W, respectively. At 333ksps, this 16-bit device not only offers performance superior to that of the best hybrids, but does so with low power, the smallest size, an easy-to-use parallel interface and the lower cost of a monolithic part. It is available in a tiny 36-pin SSOP package. Some of the key features of this new device include:

- 333ksps throughput
- 16 bits with no missing codes and ± 2 LSB INL
- Low power dissipation and power shutdown (10 μ W in SLEEP mode)
- Excellent AC performance: 90dB SINAD and -100dB THD
- Small 36-pin SSOP package

These features of the LTC1604 can simplify, improve and lower the cost of current data acquisition systems and open up new applications that were not previously possible because no similar parts were available.

Outstanding DC and AC performance

As shown in Figure 1, the LTC1604 combines a high performance differential sample-and-hold circuit with an extremely fast successive-approximation ADC and an on-chip reference. Together, they deliver an excellent combination of DC and AC performance.

The DC specifications include 16-bit with no missing codes and ± 2 LSB integral nonlinearity error, all guaranteed over temperature. The ADC includes an on-chip, curvature corrected bandgap reference. Figures 2a and 2b show the LTC1604's exceptional INL and DNL error.

In addition to its outstanding linearity, the LTC1604 provides exceptional spectral purity at 333ksps; better than 90dB SINAD and -100dB THD for a 20kHz input and 89dB SINAD and -96dB THD for a 100kHz input (Figure 3).

▲ LTC and LT are registered trademarks of Linear Technology Corporation.

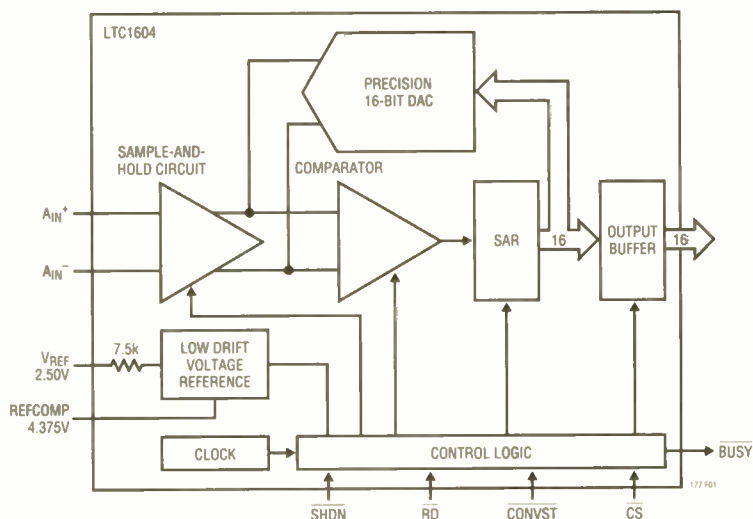


Figure 1. The 333ksps, 16-Bit ADC Features a True Differential S/H with Excellent Bandwidth and CMRR

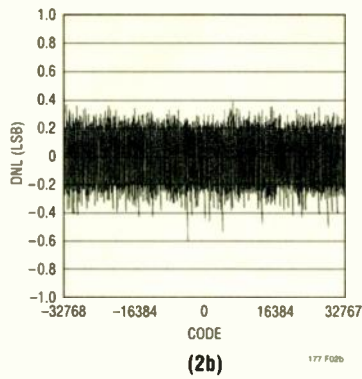
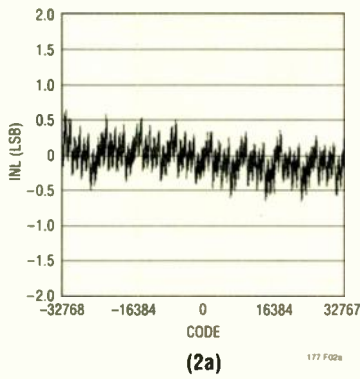


Figure 2. The LTC1604 Achieves Excellent INL (2a) and DNL (2b) Without Cumbersome Autocalibration

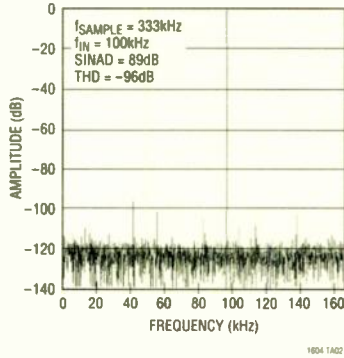


Figure 3. SINAD is Over 90dB and THD is -100dB at Low Input Frequencies. Even with 100kHz Inputs, SINAD Remains 89dB and THD is -96dB as Shown

Figure 4 shows how well the converter's signal-to-noise plus distortion ratio (SINAD) holds up as the input frequency is increased.

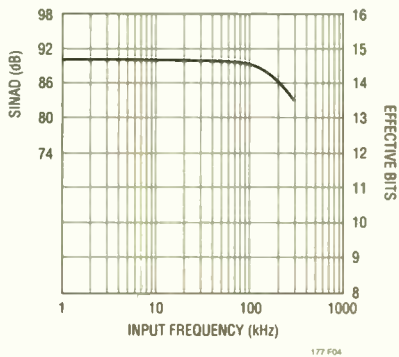


Figure 4. The Wideband S/H Captures Signals Well Beyond Nyquist

Differential Inputs Reject Common Mode Noise

Getting a clean signal to the input of an ADC, especially a 16-bit ADC, is not an easy task in many systems. In a single-ended sampling system accuracy and dynamic range can be limited by ground noise. When a single-ended signal is applied to an ADC's input, the ground noise adds directly to

the applied signal. Although a filter can reduce this noise, this does not work for in-band noise or common mode noise at the same frequency as the input signal. Figure 5 shows how the LTC1604 provides relief. Because of its excellent CMRR, the LTC1604's differential inputs reject ground noise, even at the frequency of the desired input signal. Further, the LTC1604's wideband CMRR can eliminate high frequency noise up to 1MHz and beyond.

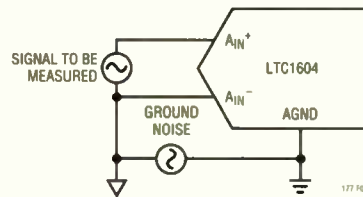


Figure 5. The LTC1604's Differential Inputs Reject Common Mode Noise by Measuring Differentially

Applications

The performance of the LTC1604 makes it very attractive for a wide variety of applications, such as digital signal processing, PC data acquisition cards, medical instrumentation and high resolution or multiplexed data acquisition.

With its excellent dynamic performance and linearity, and high sample rate the LTC1604 is the ideal ADC for high speed, 16-bit DSP and PC data acquisition card applications.

Applications such as single-channel or multiplexed high speed data acquisition systems benefit from the LTC1604's high sample rate and high impedance inputs. The high sample rate allows designers to multiplex more channels of a given bandwidth than slower 16-bit ADCs while meeting the demands of a low power budget.

For literature on our A/D Converters, call **1-800-4-LINEAR**. For applications help, call (408) 432-1900, Ext. 2453

(continued from page 128)

\$1695, with systems starting at \$3995. The chassis are available now and is supported under the company's product life-cycle support program.

Motorola Computer Group, 2900 South Diablo Way, Tempe, AZ 85282; (800) 759-1107; Internet: www.mot.com/computer. CIRCLE 573

233-MHz Pentium VME Board Supports MMX

The MMX technology in Intel's microprocessors help solve problems associated with high-end vision, image processing embedded server applications. The latest VME product to take advantage of MMX is the XVME-656. Available with 166- and 233-MHz MMX-enhanced Pentium processors, the XVME-656 takes full advantage of the architectural design enhancements that MMX technology offers.

The board processor provides a PCI-bus, UltraSCSI host adapter and a high-performance, 100-Mbit Intel PRO/100B-compatible PCI-bus Eth-

ernet controller. To support the high demands placed on an embedded server, the XVME-656 also supports 256 Mbytes of EDO Fast Page DRAM with 512 kbytes of synchronous pipeline L2 cache.

The PCI bus also plays host to the high-performance SVGA and a VME-bus to PCI bridge device. The SGVA controller integrates 2 Mbytes of high-speed SDRAM into the device, this combination supports resolutions up to 1280 by 1024 with 256 colors. The PCI-to-VME bridge device supports multiple VME master and slave images with BLT and DMA capability to provide high-performance block data operations. This gives users a flexible mapping architecture to allow configurations that will support various user applications.

Expansion for the XVME-656 is provided via a 32-bit PCI Mezzanine Card (PMC) site that allows users to add a wide variety of special interfaces, such as ATM, FDDI, SERCOS and so on. In addition to PCI expansion, the XVME-656 also can be con-

figured with a 16-bit PC/104 interface to support functional expansion of the on-board ISA bus. The XVME-656 is available now, and is priced at \$3200.

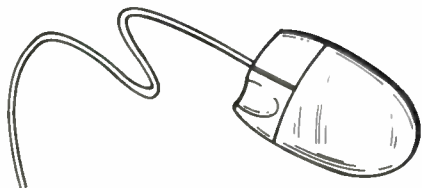
Xycom, Inc. 750 Maple Rd., Saline, MI 48176-1292; (800) 289-9266; www.xycom.com. CIRCLE 574

PCI-ISA Industrial Bridge Backplane Has 12 Slots

System designers continually require more PCI slots, yet they still rely on the large installed base of ISA I/O cards. PCI-ISA technology was developed to allow customers to take advantage of PCI's higher throughput while still maintaining 100% compatibility with "legacy" ISA peripherals.

Accommodating the best of both worlds is the PCI-972, a 12-slot passive backplane for PCI/ISA. The PCI-972 features six 32-bit PCI slots, one dedicated 32-bit PCI-ISA CPU slot, and six ISA slots. PCI bus loading limits are overcome by using PCI-to-PCI bridging. This permits a higher PCI bus slot *(continued on page 131)*

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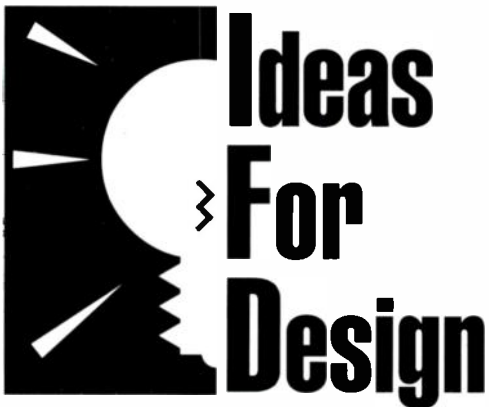
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(continued from page 129)

count—essential in many industrial and telecommunications applications—and allows concurrent bus operations on each PCI bus. In addition, each PCI slot provides Bus Mastering capability with the added benefit of a user-configurable Bus Mastering scheme on the primary PCI bus.

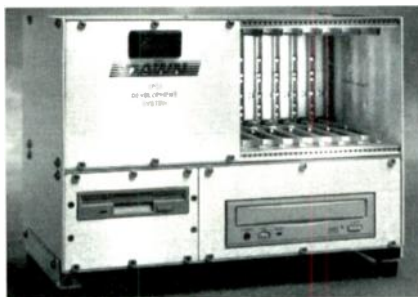
The unit conforms to IEEE P996 and PICMG rev. 2.0 specifications. All required connectors for LEDs, keyboard, speaker, and a reset switch are included. The PCI-972 has overall dimensions of 12.3 by 10.1 in., with mounting holes that are compatible with a multitude of commercially available enclosures from various vendors.

To minimize the possibility of mechanical interference with drive bays and power supplies, the unit has breakaway sections strategically located on the backplane. Available now, the PCI-972 is priced at \$400.

Teknor Industrial Computers, Inc., 616 Cure-Bolvin, Boisbriand, Quebec, Canada J7G 3A7; (800) 387-4222; www.teknor.com. **CIRCLE 575**

Development Chassis Helps Create cPCI Applications

The Model cPCIDEV-1 development chassis helps designers create applications and products using the Compact-PCI (cPCI) bus architecture. The chassis can be used for testing and



debugging, or software development. It's constructed of high-quality aluminum alloy, and is both lightweight and rugged. The backbone of the chassis is a high-performance backplane. A power supply designed specifically for the PC market provides all of the necessary voltages, and fans below the card

slots effectively cool all boards. The 8-pound chassis measures 9.85 in. high, 13 in. wide, and 7.91 in. deep. Model cPCIDEV-1 is available now for \$1195.

Dawn VME Products, 47073 Warm Springs Blvd., Fremont, CA 94539; (510) 657-4444 or (800) 258-3296; www.dawnvme.com. **CIRCLE 576**

ATX Motherboards Tackle Visual-Computing Applications

Samsung released two ATX form factor motherboards that support the company's Alpha 21164 microprocessor. The AlphaPC 164UX and 164BX boards run Windows NT and enable OEMs to create workstations and servers for high-end applications such as 3D rendering and animation. Both motherboards are based on Digital's 21174 single-chip core logic, which includes a DRAM controller and a 33-MHz, 64-bit PCI-bus controller. Call for pricing and additional information.

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Circle 520

PC-Based Time-Domain Display Of Digital Data

R. TOVAR, M. PENA, and R. OSORIO

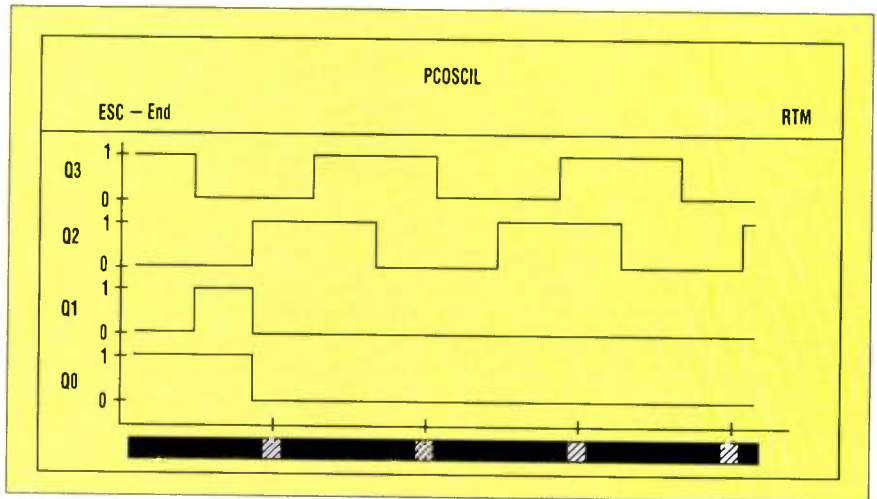
Institute of Applied Mathematics, University of Mexico, Apdo. Postal 20-726, Admon. No. 20, Delg. Alvaro Obregon, 01000 Mexico D.F.; e-mail: rtovar@uxdeal.iimas.unam.mx.

true (Q0 high level), every time the system gets and displays 40 input samples of Q0-Q3 on a screen window, and every time a trigger is detected (see the listing). In Figure 1, Q0 is the trigger signal and Q0-Q3 will be held until a new trigger signal appears. The code listing can be used to generate a TSR (Terminate and Stay Resident) program.

All signals are acquired by way of four voltage comparators U1

atching and display of time-domain digital signals with instruments like memory oscilloscopes, PC-based or any other available equipment in the market for this purpose, may result in a costly setup. This article presents a custom circuit and software support program to perform a qualitative time-domain display of four digital signals via an easy-to-read screen display window, using practical commands carried out on a PC.

To achieve this task in a low-cost manner, the parallel port of the PC is used. The software, written in C language, is designed to continuously sample data while a trigger signal is



1. This screen display window depicts the time-domain display of four digital signals.

```

.....
/* PC Oscilloscope program
 * for time domain display of digital signals using a parallel port
.....

#include <dos.h>
#include <ctype.h>
#include <stdlib.h>
#include <bios.h>

/* ++ Color constants ++ */
#define T_A 1 /* blue text */
#define T_V 2 /* green text */
#define T_R 4 /* red text */
#define FA_TA 30 /* blue bkgnd/yellow text */
#define FA_TB 31 /* blue bkgnd/white text */
#define FV_TB 47 /* green bkgnd/white text */
#define FR_TB 79 /* red bkgnd/white text */
#define FA-TV 18 /* blue bkgnd/green text */

/* function prototypes */
void salvar_video(), restaura_video();
void escribe_car(), escribe_cadena();
void dibuja_borde(), fondo();
void selec(), mostrar();

char wp[4000];
char far *mem_video;

/* main function */
main()
{
    pon_mem_video();
    mostrar();
}

/* VIDEO FUNCTIONS */
pon_mem_video() /* video mode setting */
{
    int modov;
    modov = modo_video();

    if ((modov != 2) && (modov != 3) && (modov != 7))
    {
        printf ("video can be text mode");
        exit(1);
    }
    /* video RAM addressing selection */
    if (modov == 7) mem_video = (char far*) 0XB0000000;
    else mem_video = (char far*) 0XB8000000;
}

modo_video() /* actual video mode updating */
{
    union REGS r;
    r.h.ah = 15;
    return int86(0x10, &r, &r) & 255;
}

void salvar_video (x1,y1,x2,y2) /* restores a specific screen area */
int x1,y1,x2,y2;
{
    register int i, j;
    char *buf_ptr;
    char far *v, far *w;
    buf_ptr = wp;
    v = mem_video;
    for (i=x1; i < x2+1; i++)
        for (j=y1, j < y2+1; j++)
        {
            w = (v + (j*160) + i*2);
            *buf_ptr++ = *w++;
            *buf_ptr++ = *w;
            *(w-1) = ""; /* clears the window */
        }
}

void restaura_video (x1,y1,x2,y2)
int x1,y1,x2,y2;
{
    register int i, j;
    char far *v, far *w;
    char *buf_ptr;

```

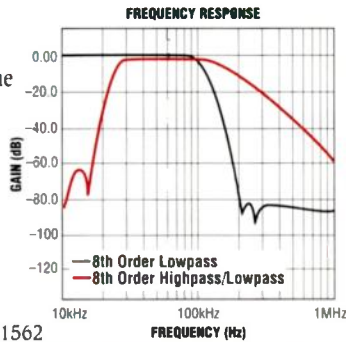

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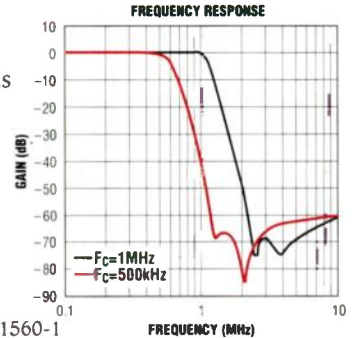
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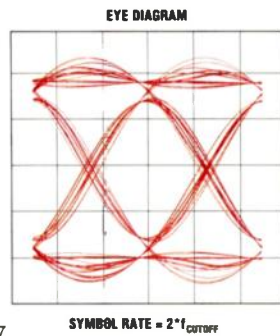
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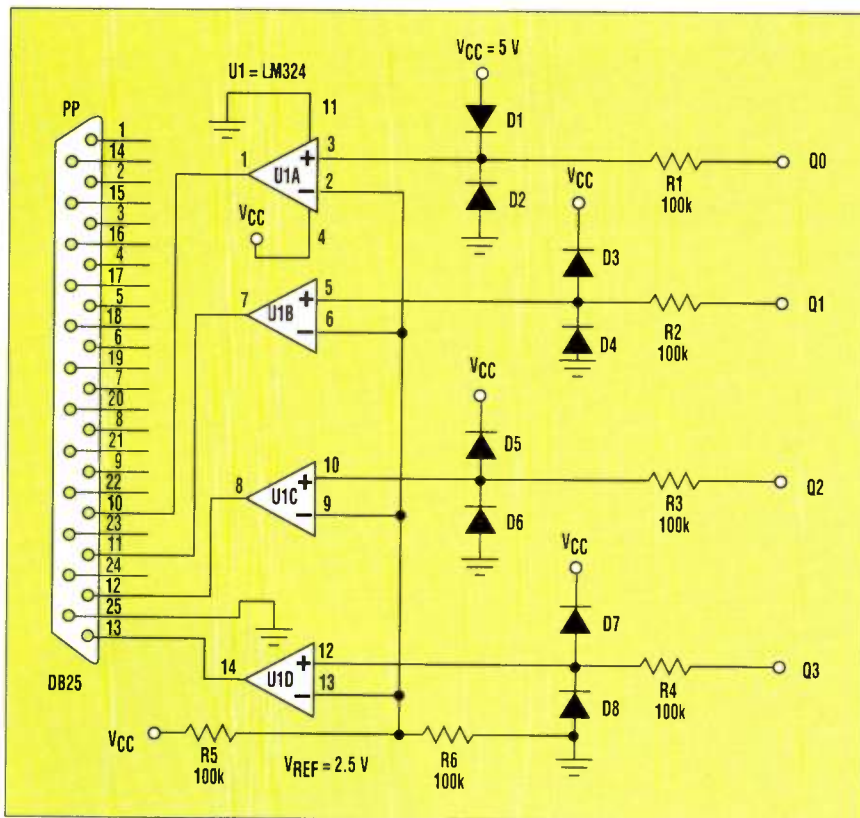
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2. All of the digital signals are acquired through the PC parallel port via four voltage comparators (U1) and a few associated discrete elements (D1-D8 and R1-R6).

(LM324) and associated elements D1-D8 and R1-R6, which protect the parallel port from overvoltages and set the port input lines to a low-level state if Q0-Q3 are disconnected (Fig. 2). If the inputs at Q0-Q3 are TTL signals, the components U1, D1-D8, and R1-R6 aren't necessary. For an optimal display of data, one of 10 different sample speeds can be selected using the 0-9 keys on the PC keyboard. The sample speed is shown on the bottom of the screen for an interactive selection by the user, and depends on the PC clock used.

Easy changes can be made to the program code to enhance the performance of the system. Some possible modifications include: allowing a larger number of input samples that are limited by the available memory on the PC; incrementing the capacity sampling to support up to eight input signals; selecting a specific digital word (combination of bit input signals instead of just one) for triggering acquisition display purpose; making the sample speed a direct function of real time; and creating a moving cursor in the screen window.

```

buf_ptr = wp;
v = mem_video;
w = v;
for(i = x1; i < x2+1; i++)
for(j = y1; j < y2+1; j++)
{
    v = w;
    v += (j*160) + i*2;
    *v++ = *buf_ptr++; /* character is written */
    *v = *buf_ptr++; /* attribute is written */
}
}

/* READ/WRITE FUNCTIONS */

void escribe_car (x,y,ch,atrib) /* char display with specific attribute */
int x, y;
char ch;
int atrib;
{
    register int i;
    char far *v;
    v = mem_video;
    v += (y* 160) + x*2;
    *v++ = ch; /* character is written */
    *v = atrib; /* attribute is written */
}

void escribe_cadena (x,y,p, atrib) /* chain display with specific attribute */
int x, y;
char *p;
int atrib;
{
    register int i;
    char far *v;
    v = mem_video;
    v += (y* 160) + x*2; /* addressing calculation */
    for (i=x; *p; i++)
    {
        *v++ = *p++; /* character is written */
        *v++ = atrib; /* attribute is written */
    }
}

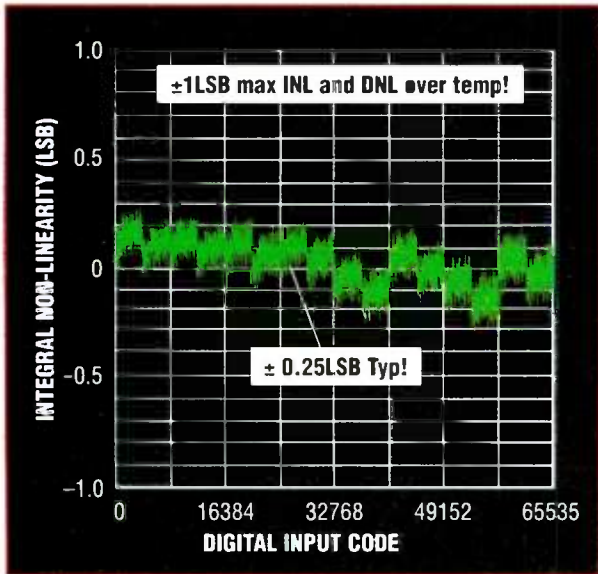
lee_car (x,y,color) /* reads and prints a character */
int x,y,color;
{
    union inkey
    {
        char ch[1];
        int i;
    } c;
    c.i = bioskey(0); /* reads a character from keyboard */
    escribe_car (x,y, c.ch[0], color);
    return c.i;
}

/* WINDOWS FUNCTION */

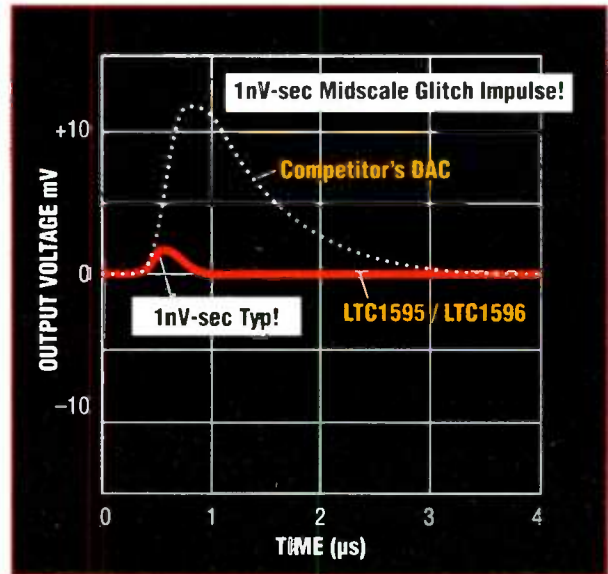
void mostrar() /* graphical signals window */
{
    salvar_video (14,3,66,21);
    fondo (15,4,65,20,T_A); /* window size */
    dibuja_borde(14,3,66,6,0,FA_TA);
    escribe_cadena(37,4,"PCOSCIL",FA_TA);
    escri_cadena(16,5,"ESC -Exit",FA_TA);
    escribe_cadena(62,5,"RTM",FA_TA);
    dibuja_borde(14,6,66,21,0,FA_TA);
    escribe_car(14,6,204,FA_TA);
    escribe_car(66,6,185,FA_TA);
    /* ===== axis display ===== */
    dibuja_borde (19,7,19,19,1,FA_TB);
    dibuja_borde (19,19,63,19,1,FA_TB);
    escribe_car (19,18,197,FA_TB); /* for Q0 */
    escribe_car (19,16,197,FA_TB);
    escribe_cadena (15,17,"Q0",FA_TB);
    escribe_cadena (18,7,"1",FR_TB);
    escribe_cadena(18,9,"0",FR_TB);
    escribe_car (19,15,197,FA_TB); /* for Q1 */
    escribe_car (19,13,197,FA_TB);
    escribe_cadena (15,14,"Q1",FA_TB);
    escribe_cadena (18,10,"1",FR_TB);
    escribe_cadena (18,12,"0",FR_TB);
}
    
```


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1nV-sec. Glitch

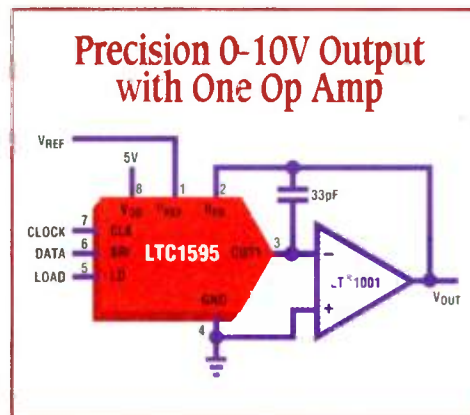


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```

escribe_car (19,12,197, FA_TB);          /* for Q2 */
escribe_car (19,10,197, FA_TB);
escribe_cadena (15,11, " Q2 ", FA_TB);
escribe_cadena (18,13,"1", FR_TB);
escribe_cadena (18,15,"0", FR_TB);
escribe_car (19,9,197, FA_TB);          /* for Q3 */
escribe_car (19,7,197, FA_TB);
escribe_cadena (15,8," Q3", FA_TB);
escribe_cadena (18,16,"1", FR_TB);
escribe_cadena (18,18,"0", FR_TB);
escribe_cadena (20,20,"_____",FA_TB);
select();
restaura_video (14,3,66,21);
}

void select()                          /* get and display input signals */
{
register int i, j, k, xr, yr, kr, val, inst, sal, color;
char nume,nume1;
inst=1; kr=0;
while (inst == 1)
{
sal = 1;
do                                     /* wait for triggering */
{
nume = inportb(0x379);
if( bioskey(1) != 0 )
{
nume1 = lee_car(17,20,FA_TB);
if( nume1 == 27 ) inst=0;
sal = 0;
}
}
while( (nume & 0x40) == 0 && sal == 1 ) ;
for( i = 0; i<=39; i++)                /* screen display */
{
xr = i+20;
escribe_car(xr,20,177,FA_TA);
if(nume & 0x80)                          /* for Q1 */
{ yr = 15; escribe_car(xr,yr, 196,FA_TA);
escribe_car(xr,yr-2,219,T_A); }
else
{ yr = 13; escribe_car(xr,yr,196,FA_TA);
escribe_car(xr,yr+2,250,FA_TA); }
if(nume & 0x40)                          /* for Q0 */
{ yr = 16; escribe_car(xr,yr,196,FA_TA);
escribe_car(xr,yr+2,250,FA_TA); }
else
{ yr = 18; escribe_car(xr,yr,196,FA_TA);
escribe_car(xr,yr-2,219,T_A); }
if(nume & 0x20)                          /* for Q2 */
{ yr = 10; escribe_car(xr,yr,196,FA_TA);
escribe_car(xr,yr+2,250,FA_TA); }
else
{ yr = 12; escribe_car(xr,yr,196,FA_TA);
escribe_car(xr,yr-2,219,T_A); }
if(nume & 0x10)                          /* for Q3 */
{ yr = 7; escribe_car(xr,yr,196,FA_TA);
escribe_car(xr,yr+2,250,FA_TA); }
else
{ yr = 9; escribe_car(xr,yr,196,FA_TA);
escribe_car(xr,yr-2,219,T_A); }
for( j = 0; j < kr+1; j++)
for( k = 0; k <= 1000; k++)

```

```

nume1 = bioskey(1);                      /* test for ESC to exit */
if (nume1 != 0)
{
nume1 = lee_car (17,20,FA_TB);
if (nume1 == 27) inst=0;
val=atoi(&nume1);
if( val >= 0 && val <= 9) kr=val;
}
nume = inportb(0x379);
escribe_car(xr,20,177,FA_TB);
}
for( j = 0; j < kr+1; j++)              /* delay */
{ for( k = 0; k <= 1000; k++) ; }
}

/* edges drawing for window */
void dibuja_borde (x1,y1, x2, y2, tipo, color)
int x1,y1,x2,y2,tipo,color;
{
register int i, j[6];
char far "v, far *t;
if (tipo == 0)
{ j[0]=186; j[1]=205; j[2]=201; j[3]=200; j[4]=187; j[5]=188; }
else
{ j[0]=179; j[1]=196; j[2]=218; j[3]=192; j[4]=191; j[5]=217; }
v = mem_video;
t = v;
for( i=y1+1; i < y2; i++)
{
v += (i*160) + x1 *2;
*v++ = j[0];
*v = color;
v = t;
v += (i* 160) + x2*2;
*v++ = j[0];
*v = color;
v = t;
}
for ( i=x1 + 1; i < x2; i++)
{
v += (y1 * 160) + i*2;
*v++ = j[1];
*v = color;
v = t;
v += (y2*160) + i*2;
*v++ = j[1];
*v = color;
v = t;
}
escribe_car (x1, y1, j[2], color);
escribe_car (x1, y2, j[3], color);
escribe_car (x2, y1, j[4], color);
escribe_car (x2, y2, j[5], color);
}

void fondo (x1, y1, x2, y2, atrib) /* set the window background color */
int x1,y1,x2,y2,atrib;
{
register xx,yy;
for (xx=x1, xx<=x2, xx++)
for (yy=y1; yy<=y2; yy++) escribe_car (xx,yy,219,atrib);
}

```

Circle 521

Tiny Light Sensor With Logic Output Draws Less Than 10 μ A

JOHN WETTROTH

Maxim Integrated Products, 120 San Gabriel Dr., Sunnyvale, CA 94086; (408) 737-7600.

A light-sensing circuit that consumes very little power can serve as an automatic backlight sensor in portable instruments (Fig. 1). This function is easily implemented with a logic gate or Schmitt-

trigger inverter, but those approaches draw considerably more supply current.

A logarithmic graph of supply current versus supply voltage illustrates a comparison (Fig. 2). As one expects for CMOS circuits, the 74HC inverter and 74HC14 Schmitt-trigger inverter draw very little current (less than 1 μ A) when their inputs are near the supply rails. Near mid-scale, however, the 74HC04 at 5 V draws more than 10 mA! The 74HC14 is better, but still draws more than 0.5 mA at mid-scale. These currents are a prob-

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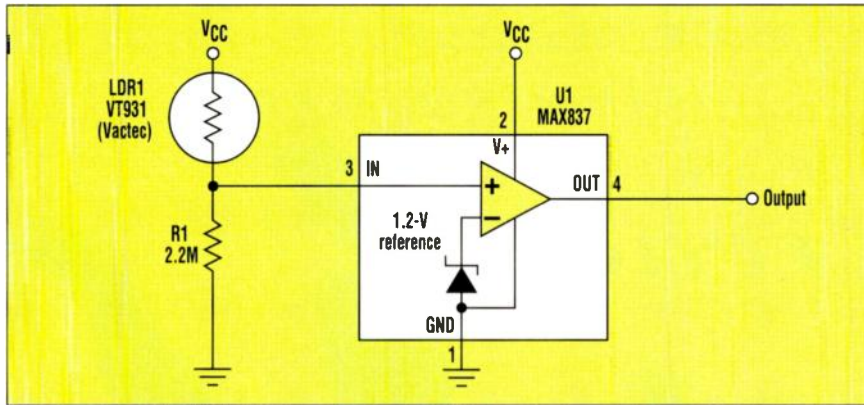
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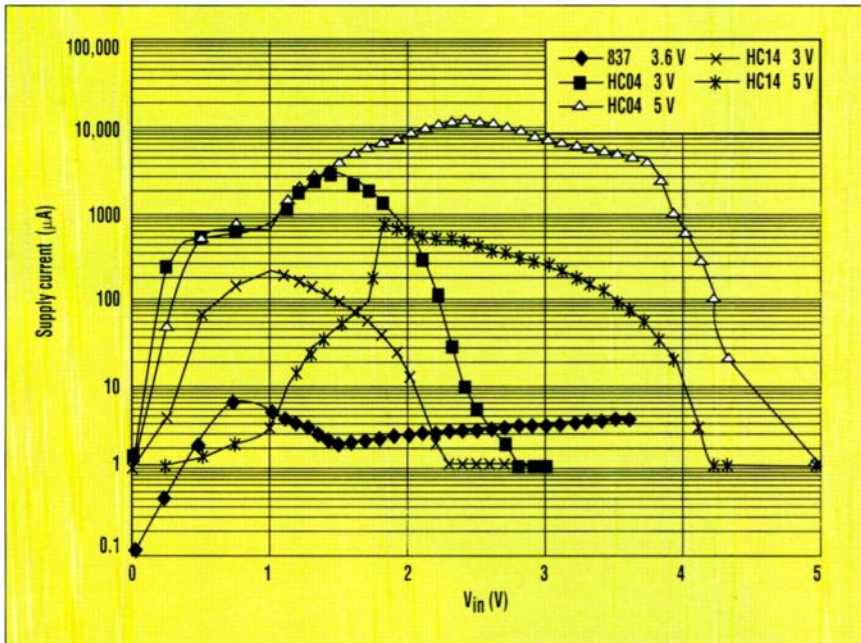
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1. This light sensor provides a low-to-high output transition at a light level determined by the voltage appearing across resistor R1, rather than a loosely specified logic-switching threshold.



2. These curves compare the supply current drawn by IC1 of Figure 1 (the lowest curve) with that of alternative devices. The total supply current for the entire circuit never exceeds 10 µA.

lem because the mid-scale condition in a light-sensing circuit can persist for a long time.

Even though 3-V power supplies lower the supply current by an approximate factor of three, the current is still significant. Adding hysteresis also helps somewhat, but there will remain a point just above or below the switching threshold at which these CMOS devices draw excessive class-A supply currents.

The lowest curve, representing the supply current for IC1 of Figure 1, varies only slightly over the signal range and never exceeds 7 µA. The external light sensor and bias resistor draw a maximum supply current of 3 µA with a 5-v supply. Therefore, the circuit's total supply current, independent of light level, is less than 10 µA. Unlike the other approaches, this circuit compares the light level (represented by a voltage on resistor R1) with a fixed reference voltage rather than a loosely specified logic-switching threshold.

Supply voltage can range from 2.5 to 11 V, with supply current measuring several microamperes at 11 V. IC1 comes in an open-drain version (MAX836) whose output (tied to a pull-up resistor) can exceed the supply voltage in a mixed-voltage system. If minimum power consumption is more important than size, choose the MAX931 comparator/reference IC. It comes in a shrink SO-8 package called µMAX (versus the MAX837 SOT package), but its maximum supply current is only 3 µA.

Circle 522

Software Linearization Of An RTD Sensor

REX KLOFENSTEIN JR.

King Industries Inc., 500 Lehman Ave., Bowling Green, OH 43402; (419) 353-5311 or (419) 353-2774; fax (419) 352-1583.

Interfacing a resistance-temperature detector (RTD) to a computerized data-acquisition system requires a resistance-to-voltage (or current) converter (bridge, voltage divider, etc.). Also, it will be neces-

sary to incorporate software routines to convert the ADC units of the data-acquisition system back into resistance values. Once the readings from the RTD are converted back into resistance values, the following algo-

gorithms can be used to generate temperature readings.

The relationship between the temperature and the electrical resistance is described by an equation developed by Callendar and later refined by Van Dusen:

$$t = \left[\frac{R_t - R_0}{R_{100} - R_0} \right] \cdot 100 + \delta \cdot \left[\frac{t}{100} - 1 \right] \cdot \left[\frac{t}{100} \right] + \beta \cdot \left[\frac{t}{100} - 1 \right]^3$$

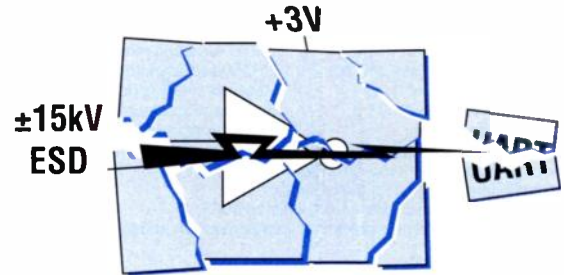
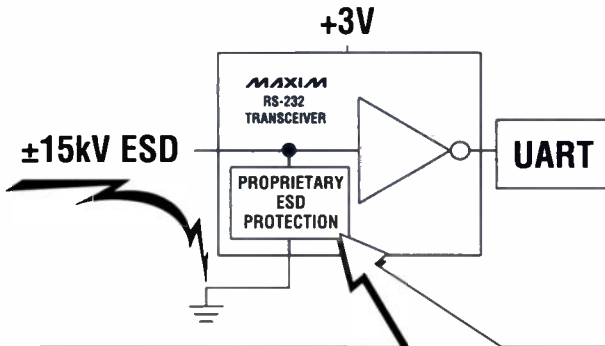
where t is temperature (°C), R_t is resistance at 0°C (Ω), δ is the linearity constant, and β is a constant determined by the boiling point of oxygen.

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						HUMAN BODY MODEL (kV)	IEC 1000-4-2 CONTACT DISCHARGE (kV)	IEC 1000-4-2 AIR-GAP DISCHARGE (kV)	IEC 1000-4-4 EFT* (kV)		
MAX3241E	+3.0 to +5.5	3/5	300	—	—	± 15	± 8	± 15	± 4	4 x 0.1	250k
MAX3243E	+3.0 to +5.5	3/5	1	—	Yes	± 15	± 8	± 15	± 4	4 x 0.1	250k
MAX3244E	+3.0 to +5.5	3/5	1	Yes	—	± 15	± 8	± 15	± 4	4 x 0.1	250k
MAX3245E	+3.0 to +5.5	3/5	1	Yes	—	± 15	± 8	± 15	± 4	4 x 0.1	1M

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```
//RTD Linearization Routine - Simplified

// -resistance- is the RTD resistance to be converted into temperature.
double LinearizeRTDSimple(double resistance)
{
    const double alpha=0.00392; //temperature coefficient (US)
    const double res0=100.000; //RTD resistance (ohms) at 0 deg C
    return(1.0/(alpha*(resistance/res0-1.0)));
}

//RTD Linearization Routine - Callendar-Van Dusen
// -resistance- is the RTD resistance to be converted into temperature
double LinearizeRTD_Callendar(double resistance)
{
    const double res0=100.000; //RTD resistance (ohms) at 0 deg C
    const double res100=138.500; //RTD resistance (ohms) at 100 deg C
    const double beta=0.0; //constant-boiling point of oxygen
    const double delta=1.508; //constant-departure from linearity
    double wtemp, work; //local work area
    // first, calculate rough estimate of temperature
    wtemp=((resistance-res0)/(res100-res0))*100.0;
    // apply delta to adjust for nonlinearity
    wtemp=beta*(wtemp/100.0-1.0)*(wtemp/100.0);
    // apply beta constant, if present, to compensate for subzero readings
    if(beta == 0.0)
        return wtemp;
    work=delta*(wtemp/100.0-1.0); //do now to speed calculation
    wtemp=wtemp+work*work*work;
    return wtemp;
}
```

If the RTD operates at or above 0°C, the third term drops out ($\beta = 0$). The actual value of δ can be determined by measuring sensor resistance at the triple point of water (0.01°C), the boiling point of water (100°C at sea level), and a third point (R_T) that can be generated with calibration equipment. Using the measured resistance and temperature values, the equation is solved for δ .

If the RTD is to operate at temperatures less than 0°C, the accuracy of the equation is improved by incorporating a third term. To calculate the value of the β coefficient for the third term, it's necessary to measure sensor resistance at the boiling point of oxy-

gen (-182.962°C). Using the resistance values measured at the boiling point of oxygen as R_T , the triple point of water, and the boiling point of water, two equations are written and solved for the values of δ and β .

To design an algorithm to solve the Callendar-Van Dusen equation, it's necessary to generate an intermediate result (t) from the first term. The intermediate value then is used to calculate correction values from the δ and β (if present) terms. The correction values are then algebraically added to the original intermediate value to generate a temperature magnitude.

A simpler, and less accurate, conversion equation can be used to con-

vert the RTD resistance value to a temperature magnitude. This algorithm is based on an approximation of the resistance-to-temperature relationship between 0°C and 100°C for platinum sensors:

$$t = \frac{1}{\alpha \left[\frac{R_t}{R_0} - 1 \right]}$$

where t is temperature (°C), R_t is resistance at t (Ω), R_0 is resistance at 0°C, and α is the temperature coefficient of resistance ($\Omega/\Omega/^\circ\text{C}$). Two standards exist for the temperature coefficient of resistance—in the U.S. $\alpha = 0.00392$ and in Europe $\alpha = 0.00385$.

The listing illustrates C++ functions that implement the linearization algorithms given in this article.

IFD WINNER

Walter Sangalli, Maxim Integrated Products, 120 San Gabriel Dr., Sunnyvale, CA 94086; (408) 737-7600. The idea: "Lead-Acid Battery Charger Also Monitors Terminal Voltage". July 7, 1997 Issue.

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Circle 523

Reduce Hum In Video Digitizer Circuits

NICHOLAS C. GRAY and TERRANCE SMITH

National Semiconductor Corp., MSD2130, 2900 Semiconductor Dr., Santa Clara, CA 95052-8090; (408) 721-6962 or (408) 721-8621; e-mail: ngray@redwood.nsc.com.

Low-frequency noise, especially hum, often is a problem in video systems. Fortunately, most hum experienced in such systems is common-mode. Hum and other low-fre-

quency signals can be rejected by using the common-mode rejection capability of a video-rate op amp.

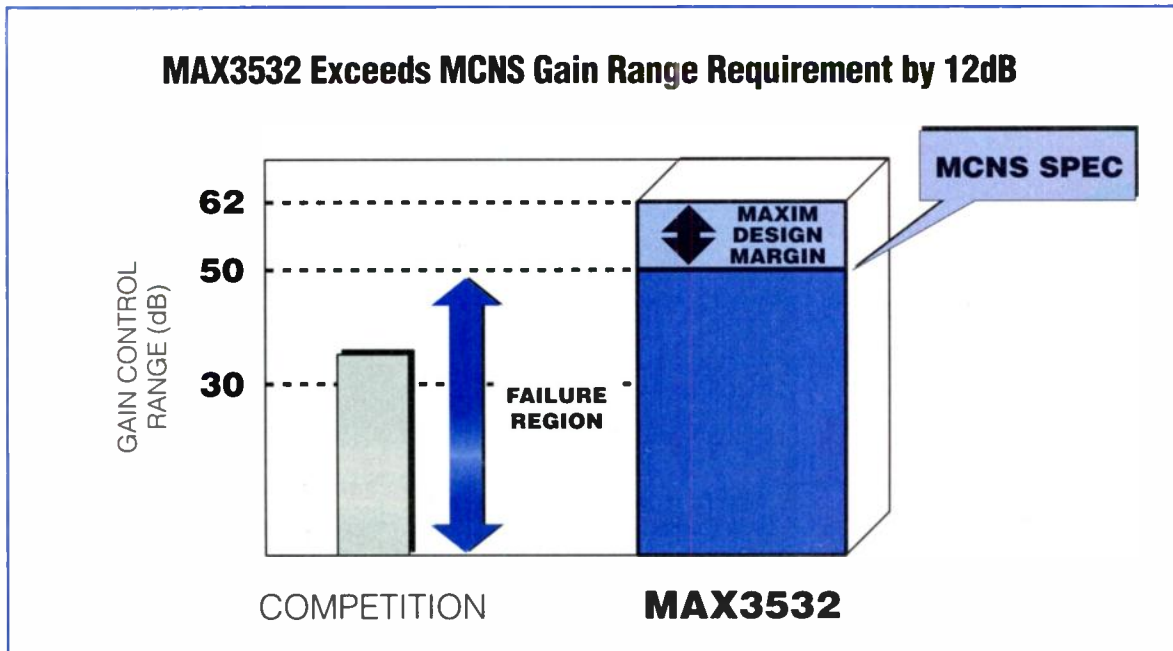
The simple circuit described here reduces low-frequency common-mode

noise that may be present on the cable (Fig. 1). As shown, the circuit provides a nominal gain of -1.

Capacitor C1 raises the cable from ground at low frequencies. C1 is a high-impedance capacitor at low frequencies when compared with the impedance of the 75- Ω cable. Any low-frequency common-mode signal, such as hum, is presented as a common-mode signal to the difference amplifier, which will then attenuate it. This circuit will attenuate hum at about 20 dB, so that 100 mV of hum will be reduced 10 mV. The attenuation is limited primarily by the ratio accuracy of resistors $R7/R6$ and $R4/R3$. The 20 dB obtained, however, is generally

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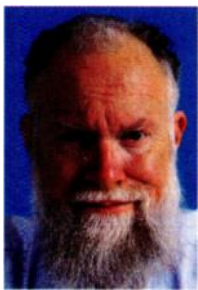
BOB PEASE

What's All This April Fools' Stuff, Anyhow?

It's that time of year again. So I've gathered some more nasty questions to make another April Fools' Column. But first I have to get serious about something for a moment.

Death in the Family: I knew Frank Goodenough for over 30 years, and worked with him for over 12 years. I've sent him many notes in the last eight years—a big envelope every week, as long we have been doing this column. Such a pleasant, enthusiastic guy. I was sure Frank would be around forever. But cancer got him on Friday the 13th of February.

We all need to take good care of ourselves. The next time you men take your annual physical exam, ask your doctor to run the PSA (Prostate Specific Antigen test), to make sure prostate cancer does not sneak up on you. Frank will be remembered



BOB PEASE

OBTAINED A BSEE FROM MIT IN 1961 AND IS STAFF SCIENTIST AT NATIONAL SEMICONDUCTOR CORP., SANTA CLARA, CALIF.

fondly by everyone who had the good fortune of meeting him.

Puzzler 1: Four guys named Ari, Ben, Cal, and Don have to cross a bridge. But the bridge is only strong enough to hold two men at a time. It's dark outside, and they have only one flashlight. If two guys cross using the flashlight, one guy will have to come back carrying the flashlight. (They cannot throw the flashlight across the bridge.) Ari takes one minute to cross; Ben is slower at two minutes; Cal is slower at five minutes; and Don is very slow at 10 minutes. They all have to make it across in 17 minutes.

This problem is given to Earl and Fran. Earl soon figures out that the best answer is 19 minutes. Fran says she knows the way to get everybody across in 17 minutes. How is that possible? The answer will be published here in two weeks.

Puzzler 2: A couple of my readers pointed out a new "invention" that is supposed to get much higher efficiency from an incandescent light bulb. This invention was published in one of the popular electronics magazines in April of 1997, and the inventor, Steven Rosenberg, has gotten a U.S. patent (5,463,307).

You can visit his web site at members.aol.com/Apsinfo/Apsinfo.html, where you can read the patent, and order a little evaluation kit, to see how great the efficiency really is. Sure, if you use an SCR circuit to chop the 115-V ac power going into a little 30-W 50-W light bulb, you can set a very narrow-pulse duty cycle. You also can establish an average voltage of perhaps 12.3 V (as measured by a dc voltmeter) across the bulb, and an average current of 0.6 A (as measured by a dc ammeter). And the light is as bright as an ordinary 100-W bulb!

Because $12.3\text{ V} \times 0.6\text{ A}$ is only 7.4 W, this guy claims that his circuit provides a factor of 10 or 12 more efficiency than ordinary dumb incandescent light bulbs. Why isn't everybody doing this? What's the problem? Check the end of this column for the answer.

Puzzler 3: You folks who have Internet accounts may have read about the "new" ice-water-and-pizza diet. Simply, if one drinks a lot of very cold water, the amount of calories to warm that water up to body temperatures (at the rate of 1 calorie per gram \times $^{\circ}\text{C}$) is almost as great as the calories in the pizza. Did you know that? See my comments at the end of the column for the details on this diet.

Puzzler 4: A couple readers pointed out that a spokesman for Sandia National Labs said that they had designed a long gear train which increased the POWER output from a nano motor, by a factor of over a million (*ELECTRONIC DESIGN*, Jan 26, p. 35). How did they do that?

Puzzler 5: As long as we are tweaking government laboratories, let's not forget the NASA engineer who claims he can get more bandwidth from an amplifier. Leonard Kleinberg has applied for a patent for the invention of connecting a small capacitor across the summing point of an op amp—from the negative input to the positive input. How does this work?

Puzzler 6: The data from my GPS receiver was really not useful in Nepal. It did provide one fun fact, which I figured out when I got home. I had three maps of the Annapurna area. One was grey, drab, and crude, by Mandala. One was very colorful (publisher not identified). And one was German, very crisp and meticulous. When I got back from Nepal, I compared the GPS readings I took at each campsite. When I got to the village of Jagat, the GPS said I was 1.2 mi. east, and 1.3 mi. south of the town—per the map. Did that mean that we were camped outside of town? Or that the GPS readings were WRONG? After all, the grey map did agree with the crisp map.

Puzzler 7: Everybody knows why man-hole covers are round. (You DO know that, don't you?) But where can you find man-hole covers that are NOT round?

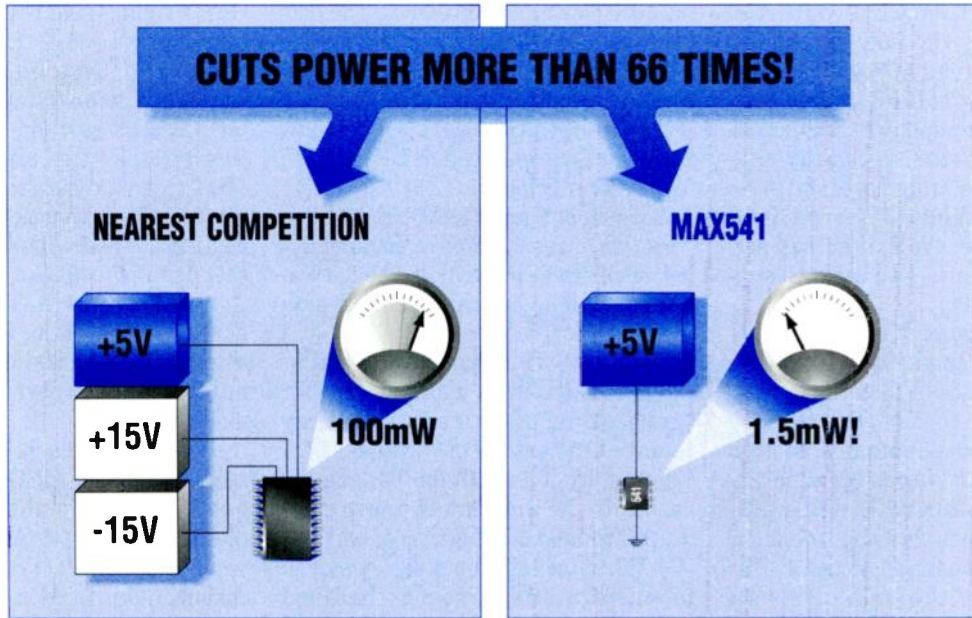
Solution to Puzzler 1: Wait 'til the next issue.

Solution to Puzzler 2: How about that 50-W bulb that puts out as much light as a 100-W bulb, with hardly 8 W of input power? Well, the average voltage across the bulb may be 12.3 V, and the average current may be 0.6 A, but the average power is NOT 7.4 W. In fact, the average power must be determined by the time integral (over one cycle) of the instantaneous $V \times I$, not by just multiplying (average volts) \times (average amperes).

When the duty cycle of a pulsed waveform is very small, the error is huge, if you were to just multiply the dc readings together. This measurement error has been so well docu-

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World Radio History

BOB PEASE

mented and debunked that you can look it up on Don Lancaster's web site: www.tinaja.com/muse112.pdf.

This is not a *new* mistake, but a very *old* mistake. I tried explaining this to the "Inventor," but he refused to believe me. He still multiplies the average dc voltage by the average dc current, and insists he has measured the average power. And, he's still selling those evaluation kits.

When I asked him why commercial wattmeters say the bulb is actually using 70 W instead of 7.4 W, he said they are just prejudiced against him, and the power company's wattmeters are in error. He says he can say anything he wants on his web site, no matter what I think—it's a freedom-of-speech issue. Well, if he can say anything he wants—so can I. Especially if I am right...

That little light bulb is actually running not at 8 W, but around 70 W. The efficiency of the bulb IS actually a little higher than that of the ordinary store-bought 100-W bulb that runs on 115 V ac. You can *always* get an incandescent bulb to run with higher efficiency (lumens per watt) by running it too hot, with too much V and I. But then the life of the bulb drops off rapidly, typically with the inverse of the seventh power of the voltage. So, if you need a bulb with high efficiency, go ahead and run it hot. But be prepared to replace it often.

That reminds me: These days, many flashlights do run their bulbs very "hot." This gives you higher efficiency, and more light, for a specified amount of battery drain. But the bulb life is LOUSY. These flashlights have a designed bulb life of only five hours, which is not mentioned at all. So be sure to take one or two spare bulbs on a long trip. I have no objection to the trade-off (improved efficiency vs. poor bulb life). But I consider it unconscionable, that the flashlight makers never warn you about the need to bring spare bulbs.

If you really want to get me on a rant, I'll explain about the Taguchi expert (Phillip Ross) who tells us, in his book *Taguchi Techniques for Quality Engineering*, to beware of flashlights where the bulb burns out too fast—because the manufacturers of batteries make them with such poor quality and tolerance, that the high battery volt-

age burns out the bulb too fast. Don't look now, but flashlight batteries are all made with the same chemistry—zinc and carbon.

Even alkaline batteries have the same voltage, 1.5 to 1.59 V, when new. There is no such problem as "bad quality causing too high voltage on flashlight batteries." But the Taguchi expert wanted us to believe that HE cares more about quality than we do, because he wants to browbeat the battery manufacturers into using higher quality. He didn't even understand that the flashlight bulbs burn out early because they are rated to operate at 2.2 V, but are operated at 2.7 or 2.8 V, for higher efficiency!

Solution of Puzzler 3: About that ice-water diet: Yes, it takes a certain number of calories to warm up the ice water you drink. But this diet relies on the confusion between a "calorie" and a "Calorie," which is actually a kilocalorie. (The calorie, which is short for "gramcalorie," is the amount of energy required to heat 1 g of water 1 °C.) A Calorie, by which all food energy is rated, is the amount of energy required to heat 1 Kilogram of water 1 °C. When we talk about the energy in food, we are likely to use the term calorie, even though we always mean kilocalorie or Calorie. The amount of energy required to warm up a glass of ice water is correctly computed in calories—and thus is 1000 times too small to make much difference in your Calorie intake. If you see this hoax in print, debunk it.

Solution for Puzzler 4: Of course, even though the Sandia guy said that a gear train could increase the output POWER, the editors at *ELECTRONIC DESIGN* shouldn't have printed that statement. Maybe the useful TORQUE or FORCE could have been increased by a factor of 100 or 1000, but surely not the power. And it will be interesting to see what actual output force or torque multiplication can be achieved, allowing for friction, and allowing for the finite strength of a tiny nano-etched silicon gear, before it breaks or binds up.

Solution for Puzzler 5: The NASA engineer, Mr. Kleinberg claims to be able to get more bandwidth, by connecting a small capacitor across the inputs of an op amp. How does this work? Poorly. He applied for a patent on this because nobody else had tried to do

that before. In MOST cases, people avoid adding in such capacitance, because it causes peaking, ringing, and extra output noise. It is not literally untrue that one can cause the 3-dB bandwidth to increase a little—it is just not useful in most cases. If you are going to install a capacitor, you can get increased *useful* bandwidth by installing it across an input resistor.

Solution for Puzzler 6: At Jagat, the GPS readings said that I was 1.2 miles east of town, and 1.3 miles south of the town. Did that mean that I was camped outside of town? Or that the GPS readings were WRONG? No, just because two maps agree, does NOT mean they are right. In this case, the colorful map was (nominally) correct. It agreed with the GPS. It said that Jagat was 40% of the way up from Sange to Chamje. The other maps agreed on 65% of the way. So in Nepal, as elsewhere in the world, maps are not necessarily correct, even if two maps agree!

In a couple years, Nepal will have maps as good as USGS maps, but the good maps have not yet been completed as far west as Annapurna. If you want to see all 22 of our campsites' locations (allowing for ±100 or 200 meters of uncertainty) you can look them up on my web site. NOTE: Even if there is some disagreement with the map, two hikers with GPS receivers should be able to find the same place with better accuracy! If you want to know how to buy the right map, even if it does not have any publisher listed, look in the Trip Report.

Solution for Puzzler 7: Of course, if a manhole cover is round, it cannot fall into the hole. However, in Nashua, N.H. there are still manhole covers that are triangular.

All for now. / Comments invited!
RAP / Robert A. Pease / Engineer
rap@webteam.nsc.com—or:

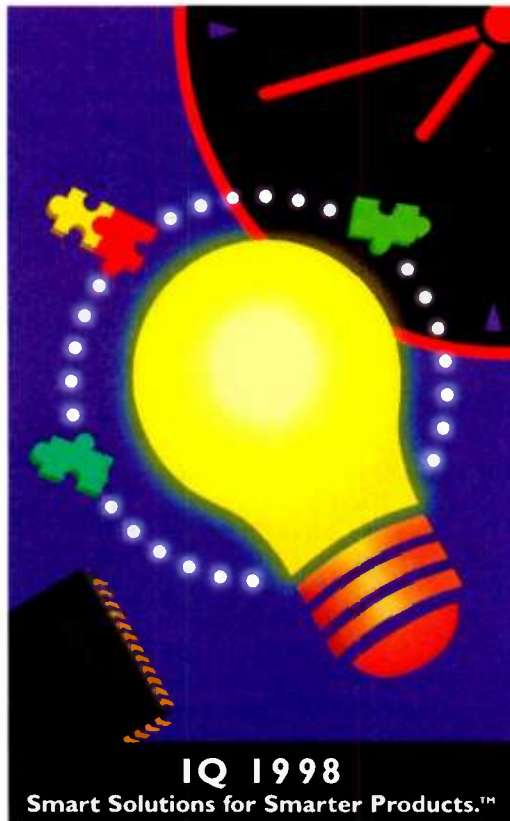
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Computer Tech Support

The Same Old Story Revisited

This month's column is on a favorite topic of "Tools and Tips" readers: computer tech support. This is a hot-button issue, with received mail peaking on it. Here's the best of that mail, plus the continuing saga of my computer experiences. On the latter, you'll read how I retired the trouble-prone old Pentium, and bought a new Pentium II office machine.

Computer Tech Support: This was first a column topic in the Aug. 4, 1997 "Tools and Tips," and was later revisited in the Nov. 3, 1997 column. And, the mail still comes in!

We start off with a thoughtful letter from Gordon Carter, chief engineer of Chicago's WFMT radio station, and associated radio networks.

I just read your Nov. 3, 1997 piece on computer tech support. I missed the first, so I may not have all the details, but I wanted to comment on your video problem story.

You didn't mention who was the PC vendor, so all of this may not be applicable. Many "manufacturers" of PC's are simply assembly houses. They buy the case, power supply, motherboard (MB), etc. from various vendors and put it all together into a computer. They slap their logo sticker on the case, and it then becomes an "XYZ" computer.

The problem with this business is that, in many cases, no one there has any idea about the complexities of drivers, chips, etc. If it doesn't work, they have no idea why, and assume it is the fault of the software or peripheral. Rarely do they expect the problem you had, because they have no idea what is happening on that board anyway.

If the problem was with the board, they should have referred you to the MB manufacturer, who could have directed you properly.

The best way to deal with a computer is to know who makes every component in it, and contact them. The "fix list" is endless for various combinations of parts—you need a computer just to keep track of the options.

For those who are serious about PC service, there is a priceless CD-ROM publication, the "Micro House Techni-

cal Library," also known as "MTL" (www.supportsource.com/ssready/mtl.htm, or call (800) 926-8299). Most Certified Network Engineers (CNE) know about it.

Novell incidentally, has a quite thorough certification program. A CNE probably knows a lot about the inner workings of PC's as well as networking, since that's all part of the testing. There are courses you can take (usually in the \$5000 range), or you can self-study. There also are some excellent books available for \$100 or less.

The "MTL" CD-ROM is rather pricey, but you do get quarterly updates. It includes data and pictures of virtually every PC part made, including MBs. I have a demo, and have found just that to be useful. You can browse through the pictures until you find a match. Yes, I know this isn't audio, but it is a matter of our professional survival.

Hi Gordon, good to hear from you. Yes, I've used an "XYZ" computer from the local computer store, and have seen the sort of process you describe. This scenario is most certainly a buyer-beware conditional deal.

Nevertheless, it can work, if you have a PC shop nearby with an individual who is technically very knowledgeable, and willing to work hard in supporting customers. I bought an "XYZ" computer under those circumstances, one which had incubation-stage MB problems. The shop owner hung in with it, and replaced things until it finally worked satisfactorily.

On keeping your own PC records, you are dead right on this one. This is basically what I've done on all the computers I've used. You do need to stay in touch with various USENET and other support groups, keep good files, and so on.

TIP: I checked further into your two recommended tools, the *MTL* and the CNE training, and found some useful information. In addition to the *MTL*, Micro House also has more gen-

eral support available for hard disks and other computer items, at: www.supportsource.com/s2main.htm. I also found a listing for CNE training related books, one example being a series by Michael Moncur, available for \$30 and up. You'll find these at: www.starlingtech.com/books/store.htm. (Note: I haven't seen these books in the flesh, this is simply availability information.)

A Problem PC Dies, and a New One Is Born: Readers following this column know that the genesis of the tech support topic came from problems with my 100-MHz Pentium machine, bought in the fall of 1995.

Almost two years to the day, this machine delivered its final "straw" of misbehavior, when it mysteriously shut down abruptly (in the middle of doing nothing). When a reboot was attempted, the ominous blue screen of a unique "Windows Death" reported "missing files." The machine would only boot to DOS. Closer examination showed a Windows directory just about completely blown away. Running Scandisk produced a cheerful creation of over 200 file fragments, and dozens of "DIRxx" recovered directories. *What to do now?*

Under such circumstances, the computer techies tell you to: 1. "Reinstall Windows 95, plus any additional applications necessary," and if that doesn't work; 2. "Repartition and reformat your hard disk, then do step 1." Nothing like a day or so of lost time doing 1 and 2, then weeks of reconfiguring those application settings.

Reinstalling Windows 95 got the machine up and running again, but in a crippled mode. The only good news in all this folly was that my data files, containing various working documents, hadn't been damaged.

At this point, I had had it. I wrote a letter to the company president documenting all of the machine's pathetic history (including copies of the two past columns describing it), and then began to research a new machine.

My complaint was acknowledged a month later by a form letter, informing me they would be in contact. Another month later, I got the final kiss-off from this PC company, whose analysis



WALT JUNG

WALT JUNG

(without any contact whatsoever) showed that my machine problems "stemmed from software." As the letter went, this made the problems unsupported, "since we do not support software after the first 30 days." Disk controller chips are software related?

To relate back to Gordon's comments, in this case, the MB manufacturer is the PC vendor. They wouldn't service my requests on the hard disk controller chip bugs, that is, the flaky chip that they had selected for use on their MB! The computer's crash-and-burn saga was a third and final strike. Time to move on.

TIP: Is there a lesson in all this? I think so. The message is that complaints to the top don't always receive a just resolution. So be prepared to trim your losses and move elsewhere.

Given all that, I then worked hard on identifying a suitable new machine. At the time, early December 1997, the PC market was populated at the high end by a number of 266- to 300-MHz Pentium II PCs. I studied reviews and web sites, trying to pin down the best combination of features, performance, vendor support, and integrity of the MB and its associated feature set, plus price.

I considered custom mail-delivery PC vendors such as Gateway 2000 and Micron, as well as more traditional vendors like Compaq, HP, and IBM. I leaned toward a final choice of a completely assembled, integrated name-vendor system, one which also had an Intel MB with the related "LX" chipset.

The final choice was a preconfigured Micron Millennia SKU 300, a 300-MHz Pentium II system with 64 Mbytes of RAM, an AGP video system, and a large hard drive (www.micronpc.com/products/computersnow/). The machine came in three days, and worked right out of the box in almost all regards. I did call the 24-hour tech support about a small configuration item, but that was readily resolved.

Things seemed OK, until I noticed after a day or so, that when in DOS, the three drives (C, D, and E) available under Windows were reduced to just C! And, F disk also reported that I had didn't have three drives either. To make a long story short, this problem was found to be related to a nonstandard hard-disk partitioning, as part of the original set up. This condition produced some ominous sounding error

messages from my favorite hard disk utility, Partition Magic from Powerquest (www.powerquest.com/). Among these were: "Partition didn't end on cylinder boundary," and "Starting sector of partition is inconsistent."

I wanted to be able to access all of the three drives, from either DOS or Windows, and ultimately, also be able to boot from another partition. To address the problem, I had to remove all the original data from the hard disk, then repartition and reformat it in a standard fashion. If this sounds a bit scary, it is! But it also happens to be much easier with the use of Partition Magic and a spare hard disk I happened to have on hand. So, after the repartitioning, I ended up with the same three drives, but all accessible from either DOS or Windows 95. Plus, I now had the ability to set up a second partition as bootable for a future OS such as NT or Linux.

In fairness to Micron, I ran this entire article by them for comment, and they had this to say:

"Micron Electronics currently sets all hard-drive partitions to use the maximum amount (2 Gbytes) permitted by the DOS FAT16 architecture. We don't use 'non-standard hard-drive partitioning' in any case. Even in the best of circumstances, after a machine has been used for any length of time by the customer, it is extraordinarily difficult to diagnose partition problems and determine an exact cause of failure.

Use of FDISK commands, software, any number of viruses, and many other factors can all cause the symptoms Mr. Jung describes. In the case of partition corruption, regardless of the cause, the correction is to FDISK and reformat the hard drive to ensure the proper partition creation. Perhaps distasteful, it does ensure that the hard drive is functioning properly.

During Mr. Jung's experience with the Micron Millennia XKU, he notes that he had 'a small configuration item, which was readily resolved by Micron tech support.' In his effort to resolve the partition configuration issue, he did not indicate (and our records do not show) he contacted our Technical Support team.

Regardless of where the problem occurred, Micron Electronics stands behind its products with the best war-

ranty and service in the industry. Contacting our Technical Support about this problem would have quickly confirmed the existence of the problem on the phone, and they could have offered one of two courses of action: 1. Help Mr. Jung reformat and reload his system to correct the problem (a few hours to complete), or 2. if still under 30 days from shipment, offered to replace the system at no charge (a few days to complete).

Micron Electronics wants our customers to be pleased with their purchase and performance of their Micron computers. Should Mr. Jung, or any Micron customer, encounter problems with their Micron product, we strongly encourage them to contact our Technical Support team at 888-FIX-MYPC anytime, 24 hours a day, seven days a week."

With regard to disk partitioning on the as-received machine, I have furnished Micron with a Partition Magic created data file of the machine's partition analysis in parallel with this article (originally made within a few days of receipt). Since I started using the new Pentium II machine on a day-day basis, it has been generally reliable (but not without some typical Windows 95 quirks). Only time will tell how reliable the new machine will be longer term, and more importantly, how support problems will be resolved.

Computer Tech Support in future columns: My feeling is that there is only so much that we as individuals can really do to change it. And, we have already discussed some very important basic points. In truth, the really worthwhile improvements in support need to come from the PC hardware and software vendors.

We simply need better answers to these problems. These difficulties lie not with us, but with the software (and hardware) that runs our PCs. See, for example, the USENET newsgroups alt.windows95, microsoft.public.win95.setup or "Bugging Out," by John C. Dvorak, *PC Computing*, Feb. 1998. I can only hope that the future holds better experiences for all of us.

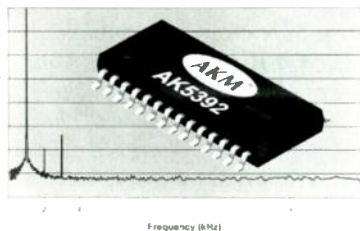
Walt Jung is a corporate staff applications engineer for Analog Devices, Norwood, Mass. A longtime contributor to ELECTRONIC DESIGN, he can be reached via e-mail at: Walt_Jung@CSI.com.

ANALOG

Audio ADC Achieves 116-dB Dynamic Range

The 24-bit stereo analog-to-digital converter (ADC) AK5392 exploits proprietary dual-bit delta-sigma architecture to achieve 116-dB dynamic range and signal-to-noise plus distortion ratio of 105 dB. In addition to offering profes-

AK5392: 116dB Dynamic Range and 105dB S/(N + D)



sional audio ADC performance, the AK5392 also cuts power consumption by half over previous solutions. Offering a sampling rate of 48 kHz, the part is designed for 5.0-V operation. However, the digital portion of this mixed-signal device can run at voltages as low as 3.0 V. With dissipation under 500 mW, the AK5392 simplifies power-supply designs and alleviates thermal problems. The monolithic ADC comes in a surface-mountable 28-lead SO package. It costs \$19.95 in 5000-piece lots. AB

AKM Semiconductor Inc., 2001 Gateway Place, Suite 650 West, San Jose, CA 95110; (408) 436-8580; www.akm.com CIRCLE 553

Dual Video Filter Improves Image Quality

By integrating dual 4th-order Butterworth low-pass filters, three video amplifiers, and a summing circuit on a single biCMOS chip, the ML6428 is able to produce clean S-video signals. It also generates a composite of the Y (luminance) and C (chrominance) video signals to improve image quality in products such as DVD players, set-top boxes, digital cameras, VCRs, and other similar applications. In fact, according to Micro Linear, the ML6428 is a single-chip solution that replaces three video amplifiers, 16 discrete components, and a DAC normally used to produce the composite of Y and C video signals. The result is a low-cost solution with significantly reduced noise and improved images. Prior to this chip, engineers had to em-

ploy several active and passive devices to meet the stringent filtering requirements to clean up digital video after it's converted to analog for playback.

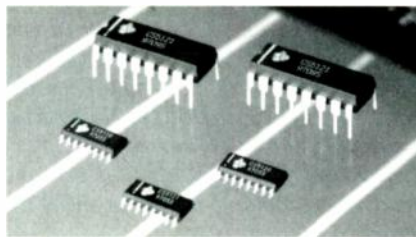
The on-chip 4th-order filters smooth out the quantization effects of DACs and reconstruct the Y and C signals. All three amplifiers directly drive standard 75- and 150- Ω cables to monitors and TVs. While the Y or C outputs can drive 2 V p-p into a 150- Ω load, the composite CV output can drive 2 V p-p into 75- Ω load. The amplifiers offer a gain of 6 dB with 1-V p-p input.

Available in an 8-pin SOIC, the 5-V M6428 is priced at \$1.50 in quantities of 1000. AB

Micro Linear Corp., 2092 Concourse Dr., San Jose, CA 95131; (408) 433-5200; www.microlinear.com CIRCLE 554

Buck Controllers Yield Compact DC-DC Converters

A set of two NFET buck controller ICs from Cherry Semiconductor are suited for configuring compact dc-dc converters with greater than 90% efficiency. Based on the company's propri-



etary V^2 control architecture, the CS-5120 and CS-5121 offer up to 100-ns transient response under severe load steps. Simple feedback-loop compensation and on-chip features minimize external components, which reduces cost and space requirements. Both the synchronous CS-5120 and nonsynchronous CS-5121 provide regulated outputs of 1.5 to 15 V from input voltages of 5 to 20 V, with 1% accuracy. Maximum output current for both versions is 1.5 A peak.

The CS-5120/21 controllers are available in 16-lead plastic DIP and plastic surface-mount narrow-body packages. In 1000-piece quantities, the respective pricing for the 5120 and 5121 is \$1.75 and \$1.67 each. LM

Cherry Semiconductor Corp., 2000 S. County Trail, East Greenwich, RI 02818-

1530; (401) 885-3600 or (800) 272-3601; www.cherry-semi.com; e-mail: info@cherry-semi.com CIRCLE 555

Potentiometer Combines High Resistance, Low Power

The AD7376 is a single-channel, 128-position digitally controlled potentiometer. It operates from +5 to +28 V in single-supply operation, and from ± 5 to ± 15 V in dual-supply operation. It's a high-voltage resistance digital-to-analog converter (RDAC), and comes with terminal resistance values of 10, 50, and 100 k Ω and 1 M Ω , suiting it for applications that require low power. The device provides a three-wire SPI-compatible serial data input register and a serial data output pin at the opposite end of the register. Additional features include a mid-scale resistance preset and a power shutdown of less than 1 mA. The AD7376 costs \$2.57 in 1000-unit quantities. It comes in a SO-14 surface-mount package, a 14-lead DIP, or a thin 14-pin TSSOP. LM

Analog Devices Inc., Ray Stata Technology Center, 804 Woburn St., Wilmington, MA 01887; (617) 937-1428; www.analog.com CIRCLE 556

24-Bit Stereo DAC Built With Delta-Sigma Technology

Crystal Semiconductor's new 24-bit stereo digital-to-analog converter (DAC) is built using the company's proprietary delta-sigma technology. Delta-sigma modulation techniques avoid the limitations of laser-trimmed resistive DAC architectures by using an inherently linear one-bit DAC. The CS4390 delivers high-quality audio for applications such as CD players, effects processors, digital mixing consoles, and DAT players. Features include a 106-dB dynamic range, 115-dB signal-to-noise ratio (EIAJ), and -97-dB THD+N. The CS4390 is pin-compatible with the company's CS4329 20-bit DAC so that users can upgrade without changing circuit design or layout. It's available in a 20-pin SSOP or a 20-pin DIP, and costs \$5.30 each in 1000-unit quantities. LM

Cirrus Logic, Crystal Semiconductor Products Div., 4210 S. Industrial Dr., Austin, TX 78744; (512) 442-7555 or (800) 888-5016; www.crystal.com CIRCLE 557

SENSORS

Wash-Process Sensor Is Cost-Effective And Easy To Use

The newest version of Honeywell's APMS-10G Series wash-process sensor has a cylindrical shape and uses an 8-to-30-V power supply for ease of application. The sensor incorporates a



microprocessor and three sensing functions: turbidity, conductivity, and temperature. Each of the sensing functions is conditioned by the internal processor, which transmits all data to the host system via a bidirectional serial-communications link.

The sensor can monitor and control an application to minimize consump-

tion of energy, water, materials, and time. Typical applications include aqueous pc-board washers and plating rinse baths. List price for the APMS-10G Series is set at \$90-\$100, and availability is one week. A wash-process-sensor application kit, which includes the sensor, a PC interface, and software, costs \$200. LM

Honeywell Micro Switch Div., 11 W. Spring St., Freeport, IL 61032; (800) 537-6945; on the Internet: www.sensing.honeywell.com; e-mail: info@micro.honeywell.com. **CIRCLE 558**

Closed-Loop Current Sensors Designed For Panel Mounting

Two new closed-loop current sensors from F.W. Bell are designed for panel mounting. Models CLN-300 and CLN-500 provide electrical isolation, and measure dc and ac currents up to 600 and 1200 A peak, respectively. Closed-loop technology allows for fast response, a wide frequency range, and linearity of more than 0.1%. The sensors are aimed at operation in high-speed

transistor and IGBT circuits. Applications include motor drives, switching power supplies, UPS systems, and battery chargers. Pricing for the CLN-300 and CLN-500 is \$125 and \$150. Delivery is from stock to four weeks. LM

Bell Technologies Inc., F.W. Bell Div., 6120 Hanging Moss Rd., Orlando, FL 32807; (407) 678-6900 or (800) 775-2550; www.belltechinc.com. **CIRCLE 559**

Glass-Probe Thermistors Offer Stability And Flexibility

A new line of glass-probe thermistors from Sensor Scientific offer excellent stability in a hermetically sealed, shock-resistant package. A wide choice of nominal resistance values and sizes allow for design flexibility. For example, the SP43A thermistor with a 0.043-in. diameter provides the small size advantage of the industry-standard large-bead thermistor without the associated handling problems. Prices start as low as \$1.00 per unit, and depend on tolerance and pur-
(continued on page 152)

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SENSORS

(continued from page 151)
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Sensor Scientific Inc., 6 Kings Bridge Rd., Fairfield, NJ 07004; (973) 227-7790; www.sensorsci.com; e-mail: sales@sensorsci.com. **CIRCLE 560**

Humidity Sensors Withstand Hostile Environments

The HS12 Series polymer humidity sensors combine high reliability and fast self-cleaning, suiting them for environments in which the air is contaminated with particulates or is extremely humid. Voltronics Sensors is the North American distributor for the sensors, which are manufactured by Scimarec Co.

Applications for the HS12 Series include humidifiers and dehumidifiers, humidity monitors, and air conditioners. They're available with lead pins or flexible leads, with a standardized or wide sensing window, and with temperature compensation. The sensors have a measurement range of 20-90% relative humidity, an operating temperature range of 0-50°C, and

measurement accuracy of ±5% relative humidity. Rated working voltage is 1 V ac, and rated power is 0.3 mW. Call for pricing and availability. LM

Voltronics Sensors Corp., 100-10 Ford Rd., Denville, NJ 07834; (973) 586-8585. **CIRCLE 561**

Piezoelectric and EM Transducers Have Clear Sound

An extremely clear and penetrating sound is one feature of the piezoelectric and electromagnetic transducers from North American Capacitor Co. (NACC). Introduced as part of the company's Mallory product line, the transducers are small, lightweight, and consume low amounts of current. Various mounting configurations are available.

The piezo transducers come in a number of styles: external drive with no feedback, self drive with feedback, surface mount, and miniature speaker (piezo and cone type). Sound output ranges from 75 to 105 dB. The Mallory EM transducers feature compact, low-profile housings, and offer sound out-

puts of 80 or 85 dB. Contact NACC for mor information. LM

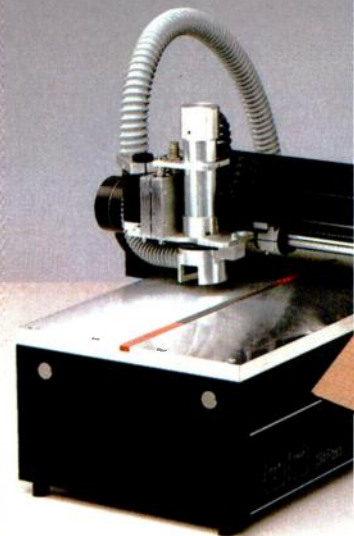
North American Capacitor Co., 7545 Rockville Rd., Indianapolis, IN 46214; (317) 273-0090. **CIRCLE 562**

Pliable Single-Button Force Sensor Is Paper Thin

A new thin-film force sensor developed by FlexiForce is flexible, pliable, and paper thin (0.003 in.). The single-button sensor conforms to almost any contour and can withstand most environments. The force buttons are small enough to allow for precise placement and large enough to ensure consistent actuation. FlexiForce offers full-scale ranges from one pound and up. The sensor can be combined with plastic or metal films to increase stiffness or for added protection from abrasion. Pricing ranges from \$30 to \$99, depending on application needs and packaging. LM

FlexiForce Inc., 307 W. First St., South Boston, MA 02127; (617) 269-8373; or e-mail flexiforce@ix.netcom.com. **CIRCLE 563**

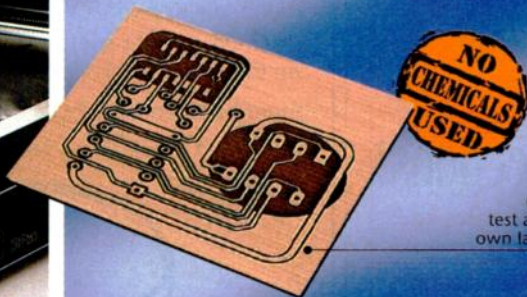
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SOFTWARE

Programming Tools Simplify Fiber-Optic Test Development

EXFO introduced the IQ Software Development Kit (IQ-SDK), a set of programming tools designed to let even novice programmers create fiber-optic test applications using the IQ-200 optical test system. The SDK is built around custom ActiveX controls for each fiber-optic instrument. Users can efficiently program in Visual Basic, Delphi, and Visual C++ environments without requiring an external data bus. With ActiveX controls, instruments are controlled and queried via Windows OLE automation over an internal PC bus. IQ-SDK also includes a step wizard and application wizard to guide programmers, an instrument simulator to develop and test applications without hardware, and command test utilities to help troubleshoot a system. Call for pricing. LM

EXFO, 465 Godin Ave., Vanier, Quebec, Canada G1M 3G7; (800) 663-3936 or (418) 683-0211; Internet: www.exfo.com. CIRCLE 564

Application Software Offers Investment Protection Plan

The Investment Protection Plan is a product strategy used by Account-Mate Software to provide long-term investment protection for end users. The company offers advanced financial-management solutions. Users get OOP source code and consistent graphical user interfaces, features, and functionality across the industry's most popular platforms. Platform support includes Windows 95/NT, IBM's AS/400, and Digital's Alpha server. The migration path between Account-Mate's multi-platform products is seamless. For example, the OOP source code enables users to carry forward any modification done to the software applications. Contact Account-Mate Software the company for further information on pricing and availability. LM

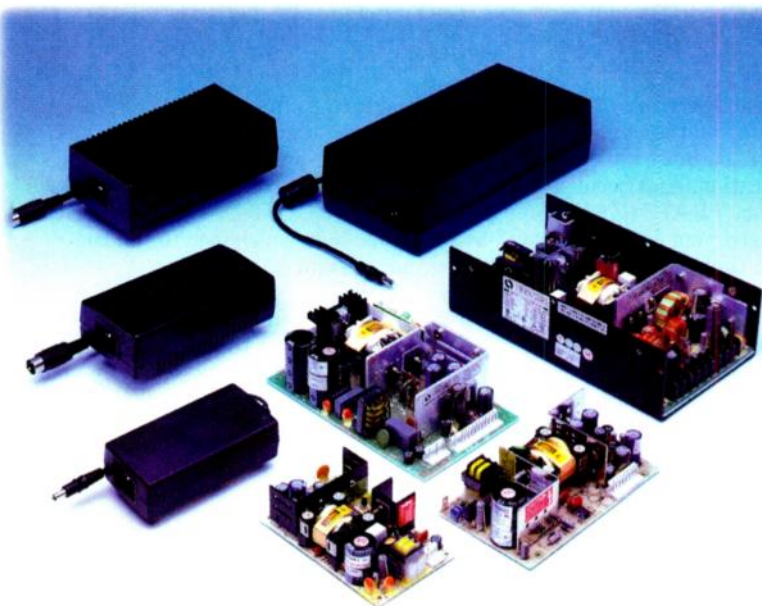
AccountMate Software Corp., 20 Sunnyside Ave., Mill Valley, CA 94941; (415) 381-1011 or (800) 877-8896; www.accountmate.com. CIRCLE 565

Automotive Customers Drive Software Tool Enhancements

A consortium of automotive companies helped define the requirements for the latest version of Integrated System Inc.'s MATRIX_x embedded-software development environment. Companies such as General Motors and BMW worked closely with the company to create Version 6.0 of the visual design and automatic code- and document-generation software. In addition to incorporating their customers' many suggestions, ISI also has revised and enhanced the product-development and quality-assurance processes associated with the product. MATRIX_x Version 6.0 is shipping now on PC, Sun, and HP platforms. Support for SGI, Digital Unix, and IBM-AIX platforms is planned. Call Integrated Systems for pricing information.

Integrated Systems Inc., 201 Moffett Park Dr., Sunnyvale, CA 94089; (408) 542-1500; Internet: www.isi.com. CIRCLE 566

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SOFTWARE

Development Package Builds TMS320C4x Applications

Software developers can use the DSP Toolchest+ to create applications for the TMS320C4x digital signal processor. The package is based on Spectron Microsystem's real-time operating system, and provides developers with a complete hardware and software environment for the 320C4x parallel processor.

Included are a 240-MFLOPS TMS320C44 quad-processor board, the PCI/C44, Spectron's operating system, Texas Instruments' optimizing C compiler, and GO DSP's debugger. Loughborough's Windows 95 and Windows NT access libraries and NVRAM programming tools also are included. Pricing for the DSP Toolchest+ is set at \$14,995. Call for further information. LM

Loughborough Sound Images Inc.,
70 Westview Street, Lexington, MA
02173; (781) 860-9020; Internet:
<http://www.lsi-dsp.com>.

CIRCLE 567

DSP Software Development Tools Support C62xx Board

Two leading DSP software tools now support the Texas Instruments C62xx processor used on Loughborough's PCI/C6200 board. The software pair includes the SPOX DSP real-time kernel from Spectron Microsystems and the Code Composer C-language debugger from GO DSP Corp. The version of Code Composer is a native bus port of the tool, running without the need for external emulation software. Contact Loughborough for additional information. LM

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CIRCLE 568

Transition Legacy Software To Thin Client Applications

Programmers needn't junk their existing software code if they take advantage of the Passport IntRprise de-

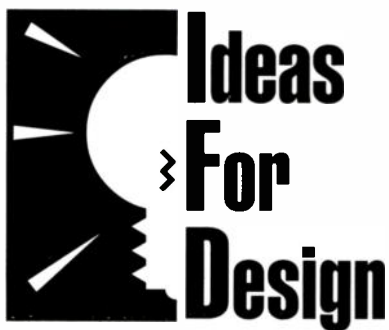
velopment environment. Passport IntRprise is an object-oriented 4GL software-development system for building thin client applications in Internet and enterprise environments. It combines a heterogeneous architecture with open middleware and database access, application fault tolerance, and scalability.

By encapsulating the business functionality, Passport IntRprise lets developers reuse the code in their existing applications. They can quickly create applications to run on Unix, Windows, and Java by re-linking the code to the target environment. Passport IntRprise is available now for Windows 3.1/NT/95, Open/VMS, and Unix. Pricing for the development environment starts at \$8995. Call the company for further details on availability. LM

Passport Corp., Mack Centre III, 140
East Ridgewood Avenue, Paramus, NJ
07652; (800) 926-6736 or (201) 634-
1100; or surf into the Internet at:
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IFD Guidelines:

- 1 to 1-1/2 pages of single-spaced typewritten text;
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- Your name, company affiliation, address, phone/fax/e-mail

Send your Ideas For Design to:

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or:
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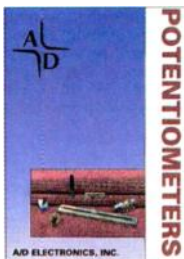


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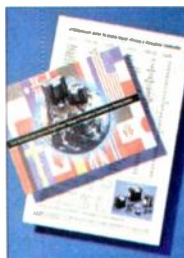


CIRCLE 253

A/D ELECTRONICS

INTERNATIONAL GUIDE

For 50/60 Hz Transformer Specifiers. Signal Transformer has issued the International Guide to Single Phase Voltage and Frequency Standards for design engineers who specify 50/60 Hz transformers used in equipment earmarked for export. Contact Signal Transformer Co., Insilo Technologies Group, 500 Bayview Ave., Inwood, NY 11096-1792. Phone: (516) 239-5777; fax: (516) 239-7208.



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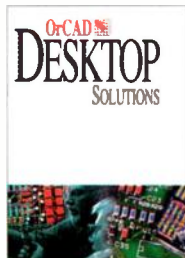


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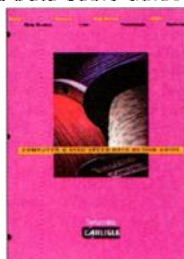


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SIGNAL TRANSFORMER CO.

Computer, High Speed Data Cable Guide

Tensolite has published a design guide to provide engineers with a guide to the new performance standards, as well as characterizations of specific cables in the Tensolite product line that meet and exceed the following standards: Fibre Channel, Gigabit Ethernet, SC1 1394-1995.a,b,2, Vesa, and Hippi. This design guide can assist in selecting cable for applications in the computer field.



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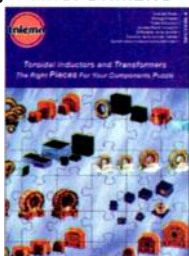


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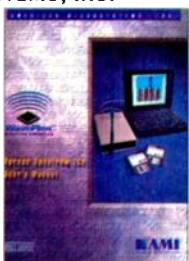


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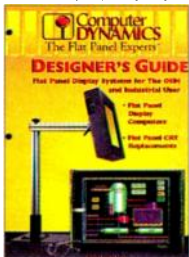


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AMI

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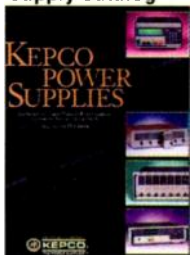


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COMPUTER DYNAMICS

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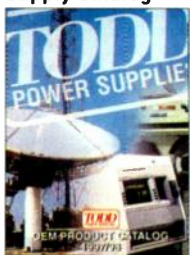


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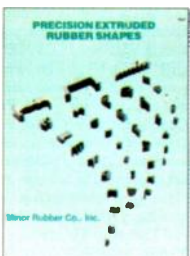


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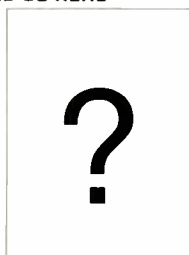


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BETA TRANSFORMER TECHNOLOGY CORP.

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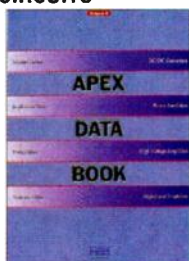


CIRCLE 270

ACCUTRACE INC.

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The 7th edition Apex Power Integrated Circuits data book contains complete product data sheets and applications notes for Apex Microtechnology's power Amplifier PWM Amplifier and DC/DC Converter product lines. Call: 1-800-862-1021; Fax: 1-520-888-3329 Email: ProLit@TeamApex.com

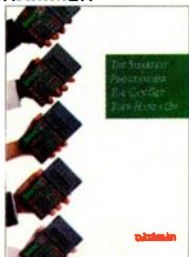


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APEX

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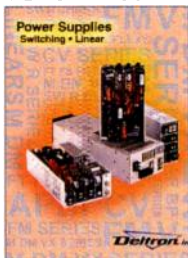
CIRCLE 276

DATA MAN

ELECTRONIC DESIGN CATALOG/LITERATURE REVIEW

NEW OEM POWER SUPPLY CATALOG

Deltron's full line catalog presents many new products including 1kW to 7.5kW T Series power factor corrected front ends for telecommunications systems, DeviceNet power modules, new generation modular F Series 0.99 power factor corrected switchers and Moduflex® M Series switchers. The catalog also details a full complement of time tested high-grade industrial and commercial power supplies. For free copy call 800-523-2332 or fax 215-699-2310.



CIRCLE 277

DELTRON

INTERCONNECT SOLUTIONS

This catalog enables design engineers to easily locate the correct adapters, clips and test accessories. The catalog includes a Ball Grid Array Reference Guide along with information on over 4000 ET products, including emulator tools, logic analyzer/scope adapters, programming adapters, production/test adapters, debugging accessories, prototyping adapters, field-configurable adapters and custom adapters. 1-800-ADAPTER www.emulation.com



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EMULATION TECHNOLOGY INC.

REVISED SWITCH CATALOG

Familiar E-Switch catalog has been revised for 1998, including new lines of sealed, illuminated push-button; illuminated rocker; slide; and SMT pushbutton switches. Catalog gives complete specifications, technical schematics, and ordering information for pushbutton, toggle, rocker, power, lever, slide, and rotary. Phone: 612-504-3525, Fax: 612-531-8235, http://www.e-switch.com, info@e-switch.com

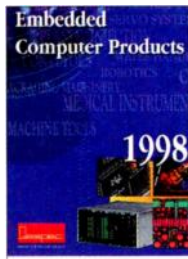


CIRCLE 279

E-SWITCH

EMBEDDED COMPUTER PRODUCTS

Gespac's 1998 catalog features a full line of 3U embedded PCs, 68XXO SBCs, motion control and over 200 I/O functions. The G-windows GUI for real-time systems running OS-9 is also offered. www.gespac.com or Phone 800-443-7722

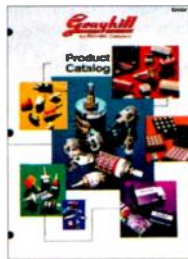


CIRCLE 280

GESPAC INC.

A WEALTH OF SWITCH INFORMATION

Grayhill's 320 page catalog provides you with electromechanical switch data, reference material, dimensional drawings and photos. Catalog No. 1 includes information on DIP Switches, Rotary Switches, Keyboards and Keyboard Modules. The detailed information allows the catalog user to select the proper product for their application right down to the part number. Phone: (708) 482-2131, Fax: (708) 354-2820.



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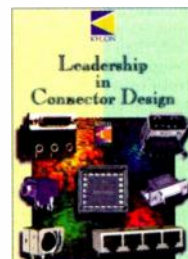


CIRCLE 286

KENT DISPLAYS

CONNECTOR CATALOG ON CD ROM

This 100 page catalog is available in both the standard full-line catalog and on CD ROM and includes many new products with complete specifications. Among the product highlights in Kycon's Catalog #11 are: •D-Sub-miniature connectors •Modular jacks •Mini-DINs •Stereo jacks •Power connectors •USB connectors •High temperature connectors •Ferrite and shielded connectors.

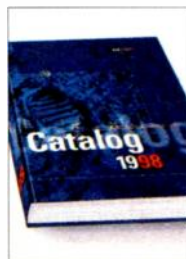


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APEM

ELECTRONIC DESIGN CATALOG/LITERATURE REVIEW

MINI COAX CONNECTOR SYSTEM

New 4-color brochure graphically illustrates the new Har-Pak Mini Coax connector system. Color photographs, detailed technical data, drawings and part numbers provide comprehensive information.



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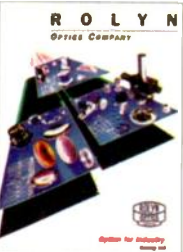


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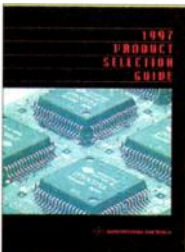


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SMI IMAGE PROCESSING LSIs GUIDE

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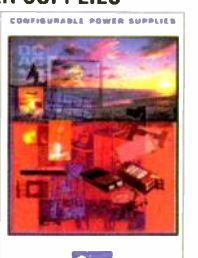


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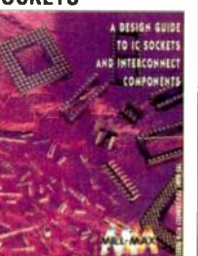


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Here's What's Coming In The Next Two Months

Be sure to check out the best cutting-edge information for engineers and engineering managers, every two weeks. Here's the line-up of some of the important topics featured in our June and July issues.

JUNE 8, 1998 ISSUE

- **Electronic Design Automation: DAC Preview**
- **Communications/Networking Technology: ATM/Gigabit Networking & Switching**
 - **PIPS: Packaging**
 - **DSP: Contributed Article .**
- **Computer Boards & Buses:**
Microcontroller Boards, Graphics, PCMCIA, Peripherals

JUNE 22, 1998 ISSUE

- **Analog Design: Data-Aquisition Modules**
- **Test & Measurements: Update: Digital Storage Oscilloscopes**
 - **Embedded Systems**
- **Digital Design: Advanced Static Memories**

JULY 6, 1998 ISSUE

- **Electronic Design Automation**
 - **PIPS: Power Management**
- **Analog Design: Power Control**
 - **Digital Design**

JULY 20, 1998 ISSUE

- **Communications/Networking Technology:**
Advanced Paging/Messaging
 - **Computers Boards & Buses**
- **Software: Development Tools For Java**
 - **Multimedia**

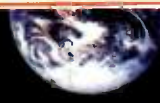
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ELECTRONIC DESIGN

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Issue Date	Closing
January 12	12/2/97
January 26	12/16/97
February 9	12/30/97
February 23	1/3/98
March 9	1/27/98
March 23	2/10/98
April 6	2/24/98
April 20	3/10/98
May 1	3/21/98
May 13	4/2/98
May 25	4/14/98
June 8	4/28/98
June 22	5/12/98
July 6	5/26/98
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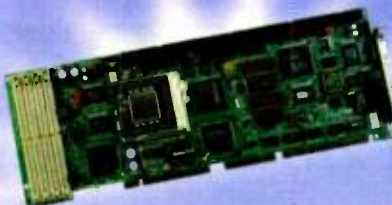
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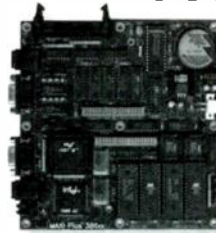
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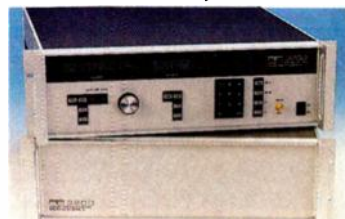
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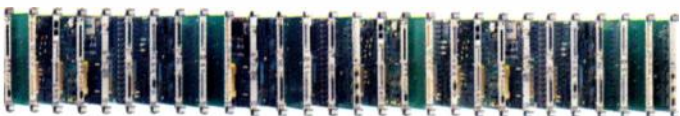
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multiplier, SIE, and transceiver. All supported by an array of design tools — including a \$99 Starter Kit (evaluation board shown). Cypress USB: Making USB Universal™. Call 800 858 1810 for your free #T040 USB literature kit or to order the #T041 CY3640 Starter Kit. Or see us at www.cypress.com/usb.

Part No.	Hub Ports	I/Os (max)	Packages	Applications
CY7C630/1/2xx	0	16	PDIP/SOIC	Low-Speed Periph.
CY7C634 5xx	0	40	PDIP/SSOP	Low-Speed Periph.
CY7C640/1xx	0	36	SOIC/SSOP	High-Speed Periph.
CY7C650/1xx	4/7	22	PDIP/SOIC/SSOP	Generic Hubs
CY7C660/1xx	4	39	PDIP/SOIC/SSOP	High-Speed Periph.+ Hubs



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