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ELECTRONIC DESIGN

TECHNOLOGY · APPLICATIONS · PRODUCTS · SOLUTIONS

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Electromagnetic Simulation Moves From Analysis To Design p. 39

Applications 101: DC/DC Converters

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High-Rel, Hybrid DC/DC Converters With Apex's Lifetime Warranty

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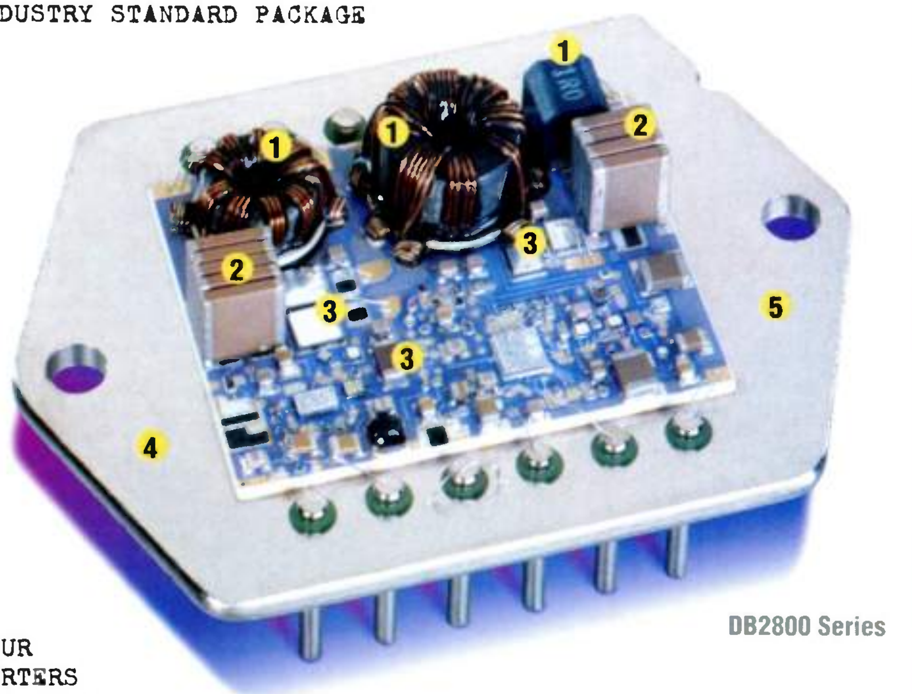

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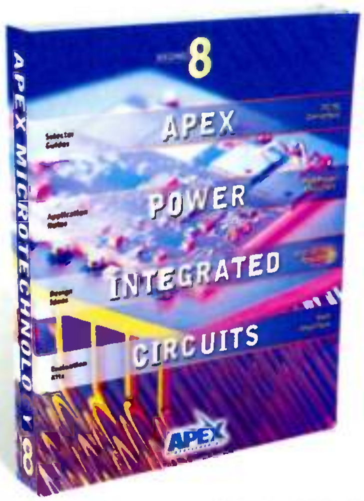

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Highlights

- Commercial grade parts designed for military ruggedness
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- –55°C to +125°C full power operation
- Fault tolerant
- Full short circuit protection
- Fully isolated
- Output voltage adjustment standard
- Remote shutdown provides on/off capabilities

DHC2800 Series

- DHC2803S—Industry's first 3V at 2A model
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- Up to 6W output, 17W/in^3 power density
- Input meets MIL-STD-704A/D requirements (80V transient)
- 11V to 50V input, exceeds industry standard
- 1" x 1" footprint, pin compatible, industry standard package

DB2800 Series

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- DB2805S—5V Single Output
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- Input meets MIL-STD-704D requirements (80V transient survival)

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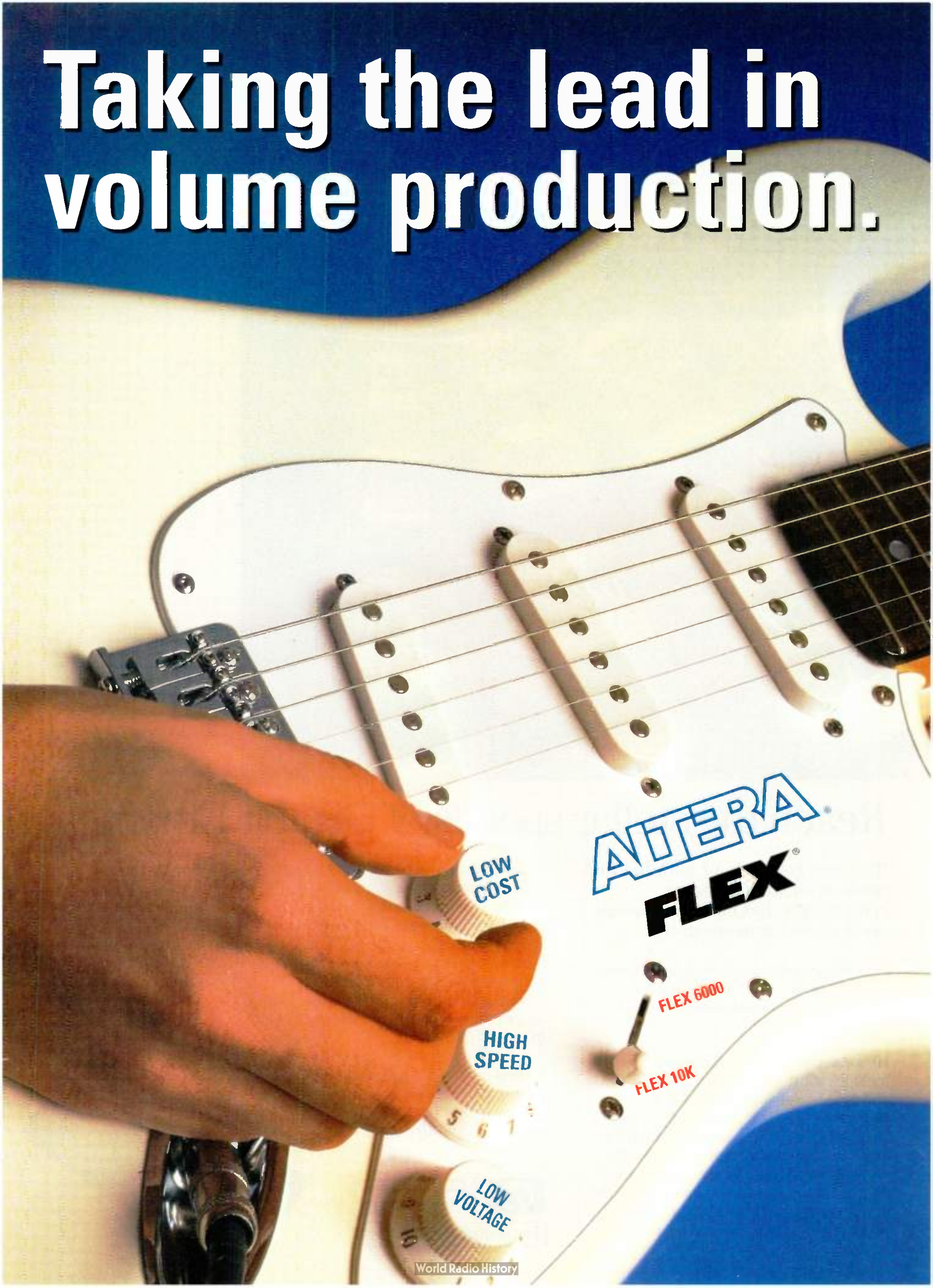
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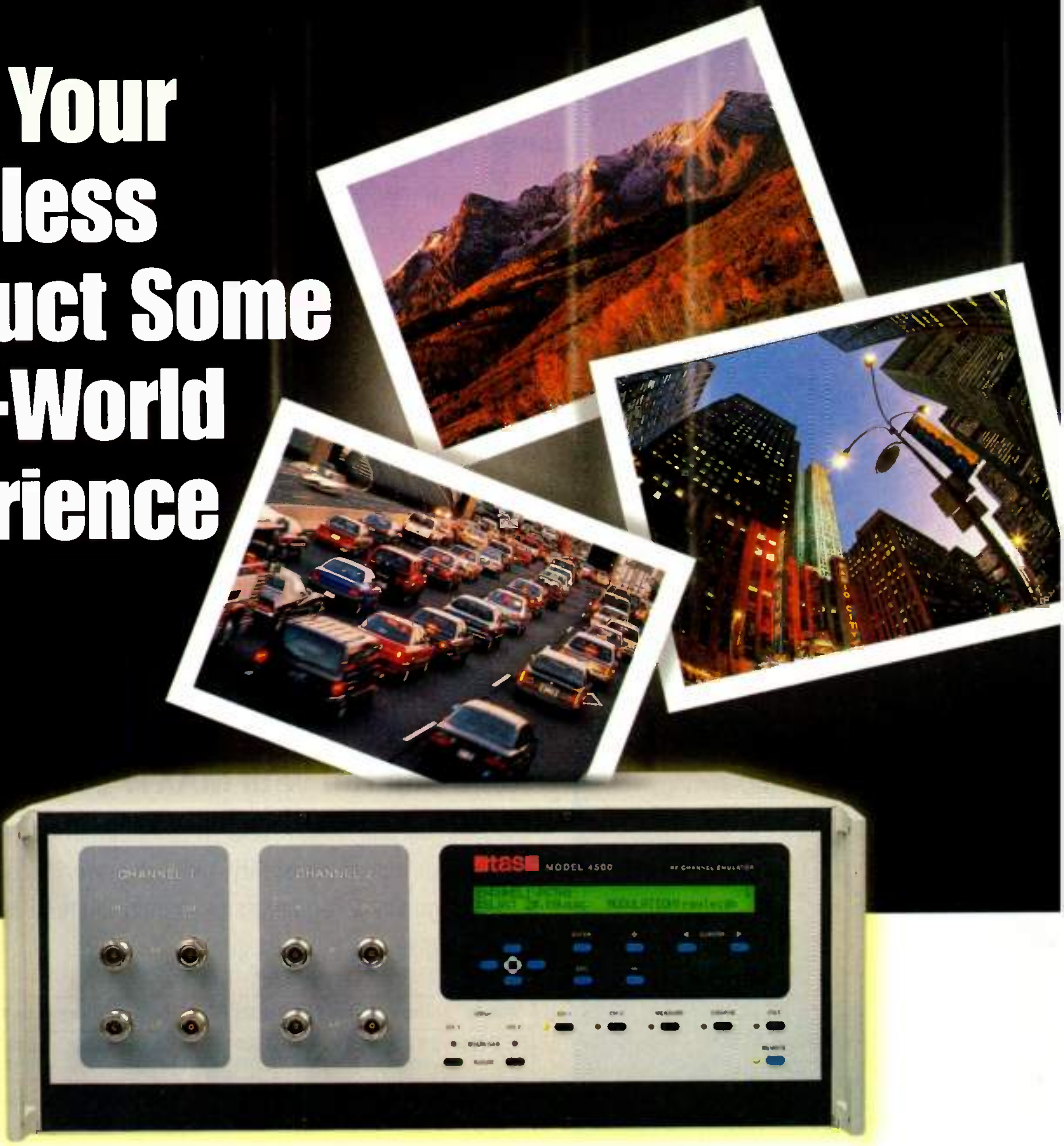

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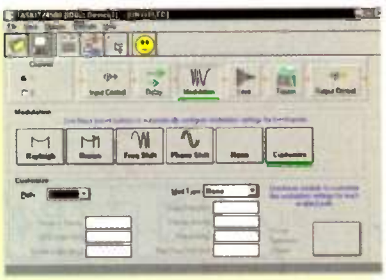

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ELECTRONIC DESIGN

April 20, 1998 Volume 46, Number 9

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April 20, 1998 Volume 46, Number 9

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Jesse H. Neal Editorial Achievement

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1968 First Place Award	1980 Certificate of Merit
1972 Certificate of Merit	1986 First Place Award
1975 Two Certificates of Merit	1989 Certificate of Merit
1976 Certificate of Merit	1992 Certificate of Merit

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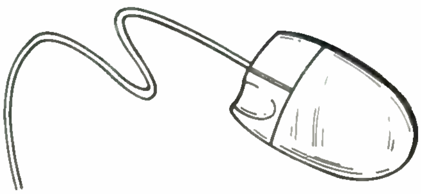

MAY 1998

100th ACerS Annual Meeting & Exposition, May 3-6. Dr. Albert B. Sabin Convention Center, Cincinnati, OH. Contact The American Ceramic Society Customer Service Dept.; (614) 794-5890; fax (614) 899-6109; e-mail: customer-srvc@acers.org; www.acers.org.

Conference on Lasers & Electro-Optics & The International Electronics Conference (CLEO/IEC), May 3-8. The Moscone Center, San Francisco, CA. Contact Amy Hutto, OSA Conference Services, 2010 Massachusetts Ave. N.W., Washington, DC 20036-1023; (202) 416-1980; fax (202) 416-6100; e-mail: cleo.info@osa.org.

IEEE International Conference on Evolutionary Computation, May 3-9. Ankorage, AK. Contact Patrick K. Simpson, Scientific Fishery Systems Inc., P.O. Box 242065, Anchorage, AK 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@alaska.net.

IEEE International Conference on Neural Networks (ICNN '98), May 3-9. Anchorage, Alaska. Contact Patrick K. Simpson, Scientific Fishery Systems Inc., Post Office Box 242065, Anchorage, Alaska 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@alaska.net.

IEEE World Congress on Computational Intelligence, May 3-9. William A. Egan Civic and Convention Center, Anchorage, AK. Contact Patrick K. Simpson, Scientific Fishery Systems Inc. P.O. Box 242064, Anchorage, AK 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@alaska.net.

Seventh IEEE International Fuzzy Systems Conference, May 3-9. Anchorage, AK. Contact Patrick K. Simpson, Scientific Fishery Systems Inc., P.O. Box 242065, Anchorage, AK 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@alaska.net.

IEEE International Symposium on Electronics & the Environment, May 4-6. Oak Brook, IL. Contact ISEE Conference Registrar, 445 Hoes Lane, Piscataway, NJ 08855-1331; (732) 562-3875; fax (732) 981-1203; e-mail: j.slaven@ieee.org.

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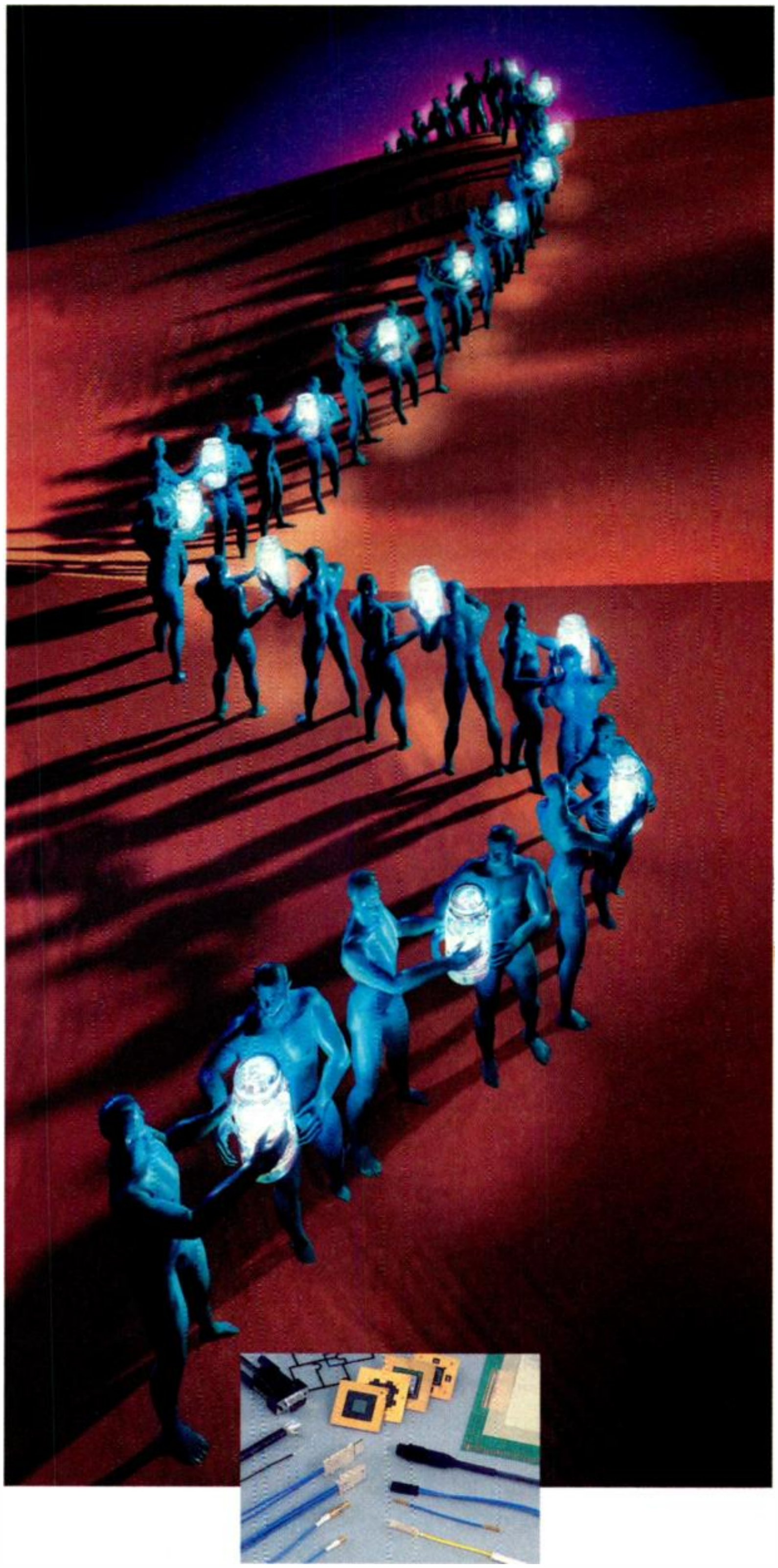

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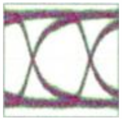

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IEEE/IAS Industrial & Commercial Power Systems Technical Conference (I&CPS), May 4-7. Edmonton, Alberta, Canada. Contact Marty Bince, Modicon Canada Ltd., 5803 86th St., Edmonton, Alberta T6E 2X4, Canada; (403) 468-6673; fax (403) 468-2925.

Custom Integrated Circuits Conference (CICC), May 11-14. Westin Hotel Convention Center, Santa Clara, California. Contact CICC, 101 Lakeforest Blvd., Suite 270, Gaithersburg, Maryland 20877; (301) 527-0902; fax (301) 527-0994.

IEEE Radar Conference, May 12-14. Contact Scott Ramey, 2501 West University, MS 8056, McKinney, TX 75070; (972) 952-4409; fax (972) 952-3071; e-mail: sramey@ti.com.

IEEE International Conference on Acoustics, Speech & Signal Processing (ICASSP '98), May 12-15. Seattle Convention Center, Seattle, WA. Contact Les E. Atlas, Dept. EE (FT 10), University of Washington, Seattle, WA 98195; (206) 685-1315; fax (206) 543-3842; e-mail: atlas@ee.washington.edu.

IEEE International Conference on Robotics and Automation, May 16-21. Katholieki Universiteit, Leuven, Belgium. Contact Georges Giralt, LAAS-CNRS, Toulouse, France, +33 61-33-63-48; fax +33 61-33-64-55; e-mail: giralt@laas.fr.

IEEE Power Electronics, Specialist Conference (PESC '98), May 17-22. Sea Hawk Hotel & Resort, Fukuoka, Japan. Contact Tsutomu Ogata, NTT Integrated Information & Energy Systems Labs., Midori-cho, Musashino, 180 Japan; +81 422-59-2350; fax +81 422-59-2347; e-mail: ogata@ilab.ntt.jp

IEEE Vehicular Technology Conference (VTC), May 18-21. Westin Hotel, Ottawa, Ontario, Canada. Contact Tara Hennessy, Industry Canada, 300 Slater St., Ottawa, Ontario, K1A OC8, Canada; (613) 990-4711; fax (613) 952-5108; e-mail: hennessytara@ic.gc.ca.

Fourth PC Developers' Expo & Conference, May 18-22. San Jose Convention Center, San Jose, CA. Contact Anna Brooks (800) 690-3858 or (619) 673-0870; fax (619) 673-1591; www.annabooks.com., e-mail: expo@annabooks.com.

48th IEEE Electronic Components & Technology Conference (ECTC '98), May 25-28. Sheraton Hotel & Towers, Seattle, WA. Contact Components Group, EIA, 2500 Wilson Blvd., Arlington, VA 22201; (703) 907-7536; fax (703) 907-7501; e-mail: judya@eia.org.

IEEE International Symposium on Circuits & Systems (ISCAS '98), May 31-June 03. Monterey Conference Center,Monterey, CA. Contact Sherif Michael, Department of Electrical & Computer Engineering, Naval Postgraduate School, Monterey, CA 93943; (408) 656-2252; fax (408) 656-2760; e-mail: michael@ece.nps.navy.mil.

JUNE

IEEE 25th International Conference on Plasma Sciences (ICOPS), Jun. 1-3. Raleigh Plaza Hotel, Raleigh, NC. Contact Sharon D. Moore, Continuing Education Specialist, North Carolina State University, Box 7401, 147 McKimmon Center, Raleigh, NC 27695-7401; (919) 515-8165; fax (919) 515-7614; e-mail: s_moore@ncsu.edu.

Eighth Biennial IEEE Conference on Electromagnetic Field Computation (CEFC), Jun. 1-4. Westin La Paloma, Tucson, AZ. Contact Paul A. Baltes, Engineering Professional Development, Box 9, Harvill Bldg., P.O. Box 210076, University of Arizona, Tucson, AZ 85721; (520) 621-3054; fax (520) 621-1443; e-mail: baltes@engr.arizona.edu.

POF World '98 (Plastic Optical Fiber), June 1-4. Providence Convention Center, Providence, RI. Contact Information Gatekeepers Inc., 214 Harvard Ave., Boston, Massachusetts 02134; (617) 232-3111; fax (617) 734-8562; www.igigroup.com.

International Conference on Consumer Electronics (ICCE), June 2-4. Los Angeles Airport Marriott, Los Angeles, CA. Contact Diane Williams, Conference Coordinator, 67 Raspberry Patch Dr., Rochester, NY 14612-2868; (716) 392-3862; fax (716) 392-4397, e-mail: d.williams@ieee. org; www.icce.org.

Fifth IEEE International Conference on Software Reuse, June 2-5. Victoria Conference Center, Victoria, BC, Canada. Contact Ted Biggerstaff, Microsoft Research, One Microsoft Way, Mail Stop 9S/1032, Redmond, WA 98052-6399; (206) 936-5867; fax (206) 936-0502; e-mail: tedb@microsoft.com.

Enterprise Networking and Computing (ENCOM '98), June 11. Georgia World Congress Center, Atlanta, GA. Contact Bhumip Khasnabish, GTE Labs Inc., (617) 466-2080; fax (617) 466-2130.

IEEE International Conference on Communications (ICC '98), June 7-11. Atlanta, GA. Contact Judy Keller, IEEE Communications Society, 345 E. 47th St., New York, NY 10017; fax (212) 705-7865; e-mail: j.keller@ieee.org.

IEEE International Symposium on Electrical Insulation, June 7-11. Key Bridge Marriott Hotel, Arlington, VA. Contact David R. James, Oak Ridge National Laboratory, P.O. Box 2008, Bldg. 4500S, MS-6123, Oak Ridge, TN 37831-6123; (423) 574-6213; fax (423) 574-6210; e-mail: dyj@ornl.gov.

IEEE/MTT-S International Microwave Symposium (MTT 98), June 7-12. Baltimore Convention Center, Baltimore, Maryland. Contact Steven Stitzer, Westinghouse Electric Corp., P.O. Box 1521, MS 3T15, Baltimore, Maryland 21203; (410) 765-7348; fax (410) 993-7747.

IEEE Symposium on VLSI Technology, June 9-11. Honolulu, HI. Contact Melissa Widerkehr, Widerkehr & Associates, 101 Lakeforest Blvd., Suite 270, Gaithersburg, MD 20877; (301) 527-0900; fax (301) 527-0994; e-mail: widerkehr@aol.com.

IEEE Symposium on VLSI Circuits, June 11-13. Honolulu, HI. Contact Phyllis Mahoney, Widerkehr & Associates, 101 Lakeforest Blvd., Suite 270, Gaithersburg, MD 20877; (301) 527-0900; fax (301) 527-0994; e-mail: pwmahoney@aol.com.

USENIX 1998 Technical Conference, June 13-17. Marriott Hotel, New Orleans, LA. Contact USENIX Conference Office, 22672 Lambert St., Suite 613, Lake Forest, CA 92630; (714) 588-8649; (714) 588-9706; e-mail: conference@usenix.org; www.usenix.org.

35th Design Automation Conference, June 15-19. Moscone Center, San Francisco, CA. Contact MP Associates, *(continued on page 65)*

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and then measure part of the digital signal

and then measure the analog signal

and then measure part of the digital signal

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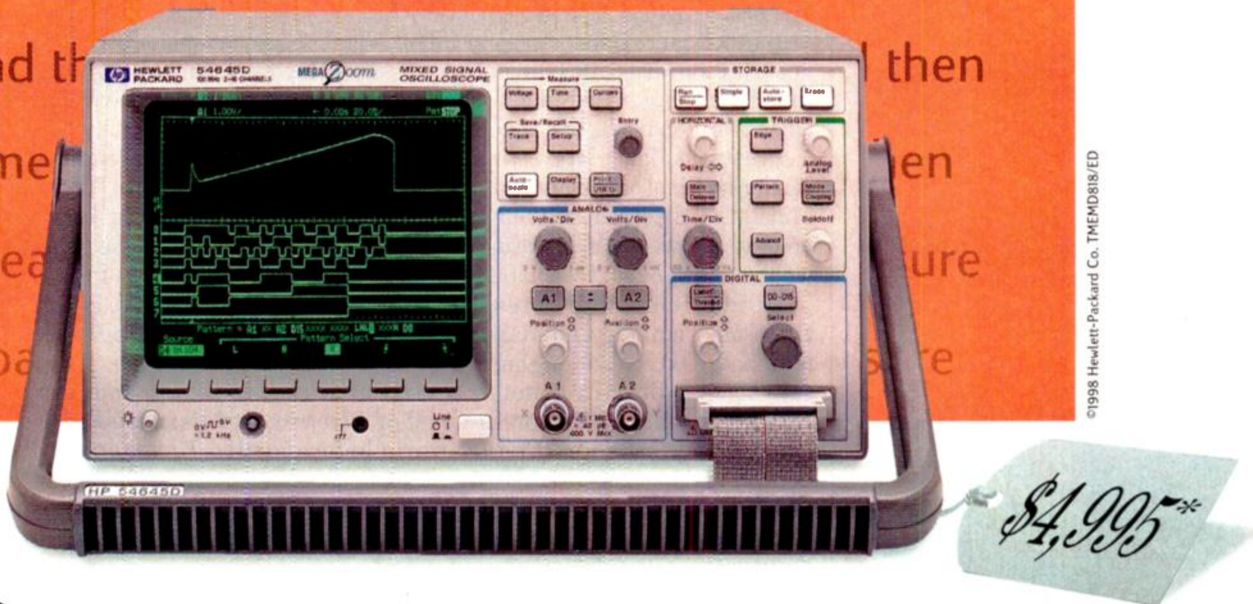

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HEWLETT PACKARD
Expanding Possibilities

EDITORIAL

From Isolation To World Player

The premier issue of *Electronic Design China* is just about ready to ship to a select group of design engineers and engineering managers who live in the most populated country on the planet—a country of 1.2 billion people that was basically closed to foreign visitors and outside influence less than 30 years ago.

To call China an emerging country would be an understatement. The country is swiftly moving from a centrally planned economy to a market economy; and from a sedentary, rural, agricultural nation to a mobile, urban, industrial society. China's economic policy has evolved from one of isolation into one that uses foreign capital and reaches out to global markets. And, along with all the other important changes, China's leadership has grown from rule by personal edict to a single-party government that makes use of technocrats and fast-growing legislative framework.

But not everything is rosy in China. The U.S. government has continued to voice its concern over human rights issues. However, our colleagues in China tell us that under President Jiang Zemin, a great deal of positive change has already taken place, and much more is expected.

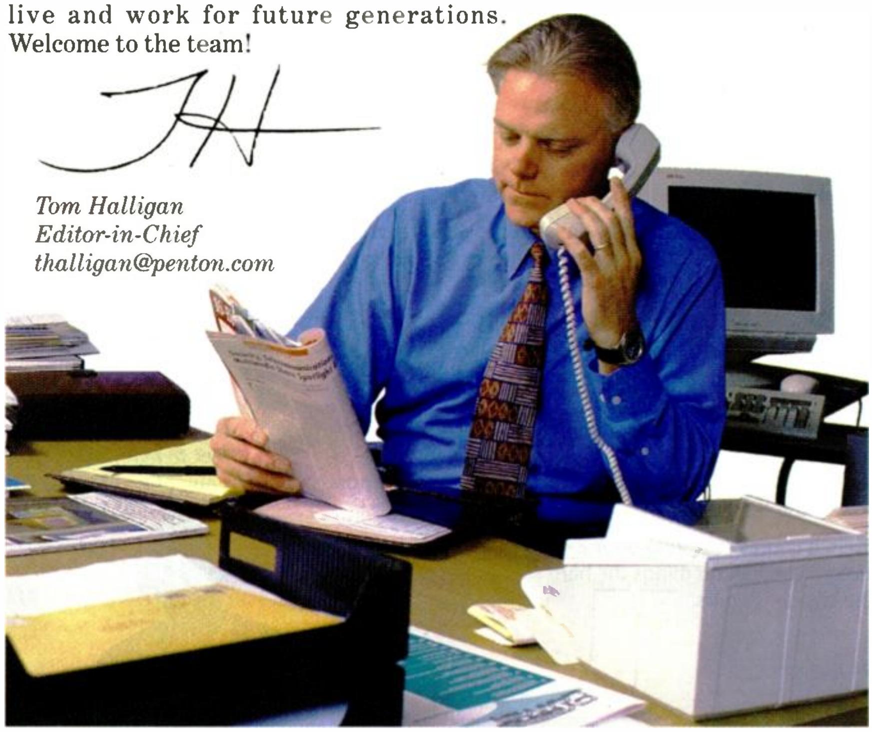
President Jiang, interestingly enough, majored in electrical engineering at Shanghai Jiaotong University, and previously served as Vice Minister and Minster of Electronics Industry. Additionally, he is well read in science, technology, and western literature. And, because President Jiang is an engineer, we'll make sure that we add him to our subscription list.

Heading our editorial team at *Electronic Design China*, is Editor-In-Chief Ma Tianfang and Managing Editor Liu Hong. Based in Beijing, both men have extensive engineering and publishing experience. Ma recently served as Editor-In-Chief of *Electronic Product World*, and previously served 10 years as Editor-In-Chief of *Electronics International*. Liu also worked at *Electronic Product World* before joining *Electronic Design China*, and has authored 10 high-tech books. His extensive experience also includes editing several technical magazines.

We look forward to working with our new editors at *Electronic Design China*. The entire *Electronic Design* group anticipates serving a new community of engineers who will no doubt make their country a better place to live and work for future generations.

Welcome to the team!

Tom Halligan
Editor-in-Chief
thalligan@penton.com



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Ditching The Myth—And The Box...

It's one of life's more interesting learning experiences when something you've held to be immutable fact is suddenly proven to be slightly inaccurate, somewhat of an untruth, or, in a worst-case scenario, an outright lie. Few areas of endeavor suffer as much from such gradations of truth than historical research, especially prior to, and during, the chaos of wartime. While heroes are being made and lost on the battlefield, issues such as patent rights and who invented what tend to pale in comparison. Such was the case with the invention of the first computer.

In my column "Ditching The Cardboard Box" (ELECTRONIC DESIGN, *Sept. 15, 1997, p. 22)*, I helped, quite accidentally, to perpetuate a myth. In that column, I related how U.S. Govt. Contract W-670-ORD-4926, signed on June 5, 1943, gave the go-ahead for the University of Pennsylvania to develop the Electronic Numerical Integrator and Computer, or ENIAC. The myth I helped perpetuate was that ENIAC was the first digital computer. It took Dave Perkins, manager of R&Q at Compressor Controls, to set me straight. In a well-written e-mail, this self-ascribed "old poop" was quick to show me the error of my beliefs. Read on!

"Patrick—I couldn't let your September 15 column go without pointing out that you have helped perpetuate the old belief that ENIAC was the first electronic digital computer. It was researched and proven in court recently that Dr. John V. Atanasoff, and graduate student Clifford Berry, of the physics department of what is now Iowa State University in Ames, Iowa, designed and built the first such machine for solving systems of simultaneous equations in 1939-1940. In fact, at least one of the people from the University of Pennsylvania who developed the ENIAC visited Dr. Atanasoff and was familiar with the principles he developed in the "ABC" (Atanasoff Berry Computer). Credit for this would have been clearly established through a number of patents, but World War II caused a staffing change at ISU and the applications were never properly filed. In fact, the original machine was ignored during and after the war and disassembled so that only parts of it still exist today.

PATRICK MANNION
POWER, PACKAGING, COMPONENTS

Let me explain that I have no ties to ISU or anyone else associated with this story, save one. Since Dr. Atanasoff's work was recognized, ISU has tried to call attention to it. Eventually money was raised to commission Ames Laboratory to construct a replica of the ABC, and I happen to know an older engineer and technician who were lucky enough to work on this project. With the few notes and original parts remaining, reconstructing it was a daunting task. The ABC really was a remarkable piece of work. Hanging above my PC is the schematic for the seven-tube add/subtract module used in it. An array of these were the electronic heart of the machine. Other features included punched-card I/O that, obviously, predated IBM's adaptation of the old loom programming method, but even did it one better in that the ABC used high voltages to punch through the cards as a means of output (the first example of burning a program into a form of ROM!). The memory drum I mentioned before consisted of a large array of capacitors that was physically rotated to synchronize the computation process, thereby defining the clock cycle of the processor. It was read and refreshed in a continuous cycle—this was literally a Dynamic Sequential Access Memory (DSAM).

The concept for all of this, if not the details, came to Dr. Atanasoff as he drove through a pounding rainstorm, at night, from central Iowa to Illinois where he stopped for a drink and sketched his ideas out on an available piece of paper—yes the first digital computer was actually first sketched on a cocktail napkin! Currently the replica has been constructed and has now passed testing. It will be circulated around the country for a variety of shows over the next year or so. If you'd like more information on this, call Glenda McIntire at ISU public relations at (515) 294-6136." And there you have it. Dave, please follow up again with a phone number or new e-mail address so I can forward to you any replies this column may receive. Thanks again for setting me straight. *pmannion@penton.com.*

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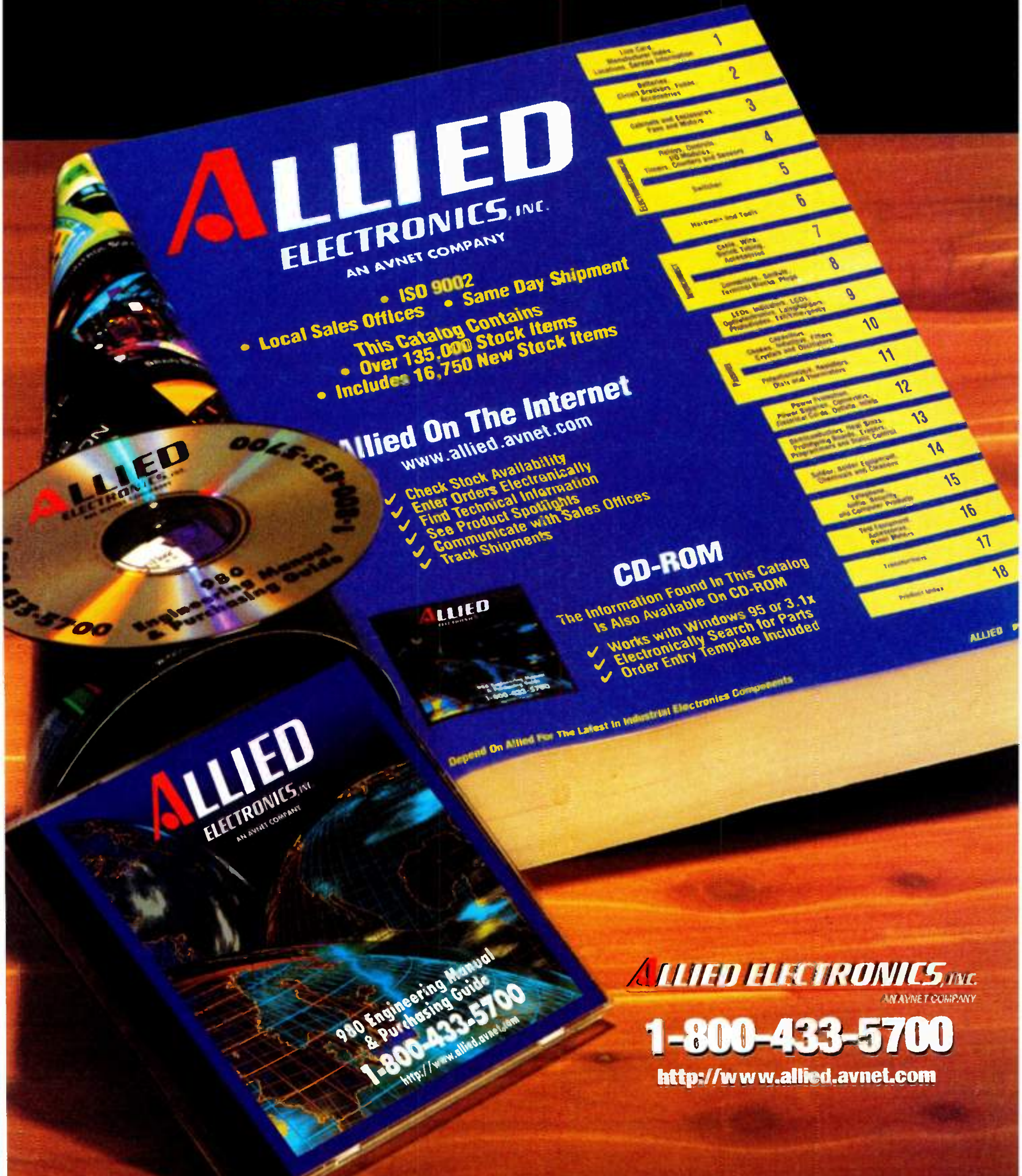

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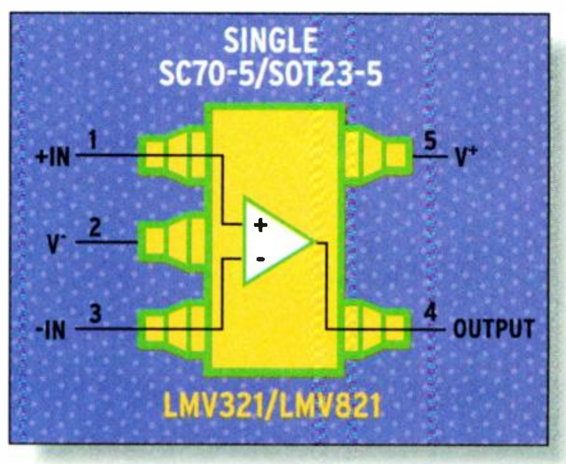

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LMV358	Op Amp	Dual	MSOP-8, SOIC-8
LMV324	Op Amp	Quad	TSSOP-14, SOIC-14
LMV331	Comparator	Single	SC70-5, SOT23-5
LMV393	Comparator	Dual	MSOP-8, SOIC-8
LMV339	Comparator	Quad	TSSOP, SOIC-14
LMV821	Op Amp	Single	SC70-5, SOT23-5
LMV822	Op Amp	Dual	MSOP-8, SOIC-8
LMV824	Op Amp	Quad	TSSOP-14, SOIC-14

	LMV300 Series	LMV800 Series
GBW	1MHz	5MHz
Slew Rate	1V/µs	2V/µs
Input Offset Voltage	7mV	3mV
CMRR/PSRR	50dB, 50dB	70dB, 70dB
Flat Band Noise	40nV/√Hz	25nV/√Hz
Supply Range	2.7 - 5.5V	2.5 - 5.5V
Supply Current	150µA/Channel	450µA/Channel
Current Limit Protection	No	Yes

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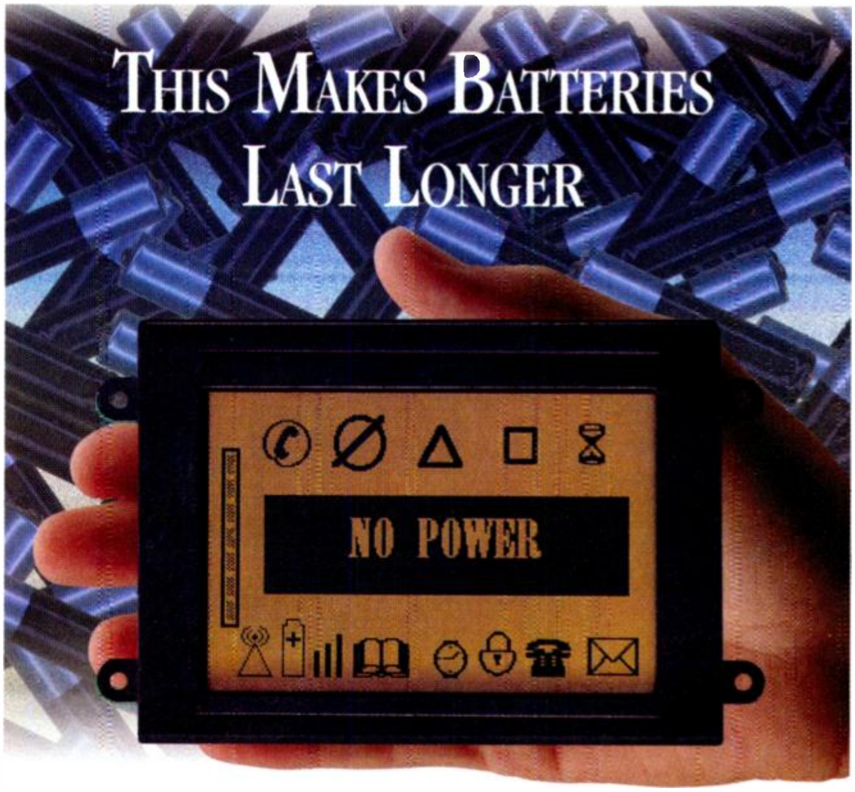

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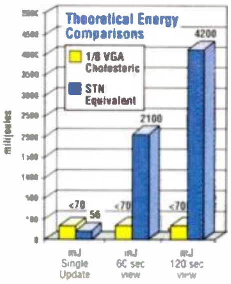

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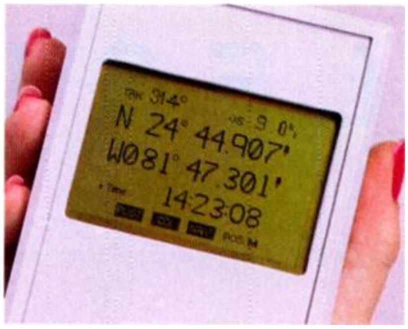
1/8 VGA "No Power" Display Modules



KENT 1/8 VGA display modules feature ChLCD technology for no power consumption except for image generation, high contrast and a wide viewing angle. They are available with a standard resolution of 100 dpi and an active viewing area of 40.6 mm X 61.0 mm (1.60 in. X 2.40 in). They're ideal for applications such as portable communications, data collection, global positioning systems and more to maximize battery life.

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MIT Humanoid Robot Project Takes Exciting Steps Forward

At a press event held in conjunction with the Council on Competitiveness National Innovation Summit, Professor Rodney Brooks, director of the Massachusetts Institute of Technology Artificial Intelligence Lab, demonstrated Cog—a humanoid robot. A project now four years old, Cog physically approximates the upper torso of a large man. Says Brooks, Cog has already "learned" some basic skills. For example, it can reach its hand to a visual target and shake its head back and forth or nod up and down in imitation of a researcher.

In getting this far, researchers have solved some serious engineering problems. For example, Cog's arms are safe to interact with, unlike those of most conventional robots. As a result, some of the robot's components are patented and available for licensing through the MIT Licensing Office.

Cog's creators base its design on "embodiment," the theory that people—and robots—need the form of the human body to shape human thoughts.

Key to the robot's operation is Cog's brain, which is comprised of many sets of computers, such as microprocessors, microcontrollers, and off-board desktop computers. Each set of computers represents a different part of Cog's nervous system. On-board chips include Motorola 68HC11's and 68300 series microcontrollers. A QNX real-time kernel along with other software components are used to form the operating system. Also key to the system is a physical spring system and an associated "virtual spring" software developed by MIT graduate students and professors.

Brooks said the ultimate goal of the project is to build a robot as human-like as "Commander Data" on the *Star Trek: The Next Generation* television series, but admitted that it probably wouldn't happen in his lifetime. For more information, contact Elizabeth A. Thomson at (617) 258-5402; e-mail: *thomson@mit.edu*. JC

Silicon-Carbide-Based Microwave MESFET Demonstrated

Cree Research Inc., Durham, N.C., has developed a silicon carbide (SiC) based n-channel metal-semiconductor field-effect transistor (MESFET) capable of producing 53 W of output power at a frequency of 3.0 GHz. According to Cree co-founder and director of advanced devices John Palmour, the 53 W was recently demonstrated under continuous wave operation from a single die with an area of only 3.0 mm^2. "This is the first demonstration of SiC MESFET with significant amount of power at microwave frequencies", says Palmour. These power transistors are being aimed at cellular base stations, solid-state television, and radio broadcast systems, as well as radar and electronic counter-measure systems in military applications.

Cree Research has been developing SiC MESFETs for the last few years under contract from Naval Research Labs, Offices of Naval Research, and DARPA. While the earlier work showed that MESFETs fabricated on a SiC substrate can operate efficiently at microwave frequencies, present efforts are focused on power-handling capabilities of such devices. Toward that end, scientists at Cree are developing larger die size MESFETs. Consequently, to achieve a 53-W output at 3 GHz, the die size of the SiC MESFET was increased by about 40 times over earlier devices.

While the current power density of the n-channel MESFET is about 1.25 W/mm, efforts are underway to improve that capability within a year. The device was operated at 40 V supply, with an operating current of 10 A and bias current of 2 A. Under class AB conditions, the MESFET offered a power-added efficiency of 37 percent. Other features include 100-V voltage breakdown, f_T of 10 GHz, and f_{MAX} of 20 Hz.

Although, the power measurements were made at room temperature, SiC devices can handle baseplate temperature of up to 200°C and junction temperature as high as 350°C, says Palmour. The semi-insulating substrate employed in this fabrication is 4H SiC substrate material. Meanwhile, reliability and accelerated life tests for 1000 hours at elevated temperatures are being conducted at Space and Naval Warfare (SPAWAR) Systems Center in San Diego, Calif. Simultaneously, Cree is exploring yield and production aspects of fabricating SiC-based microwave MESFETs.

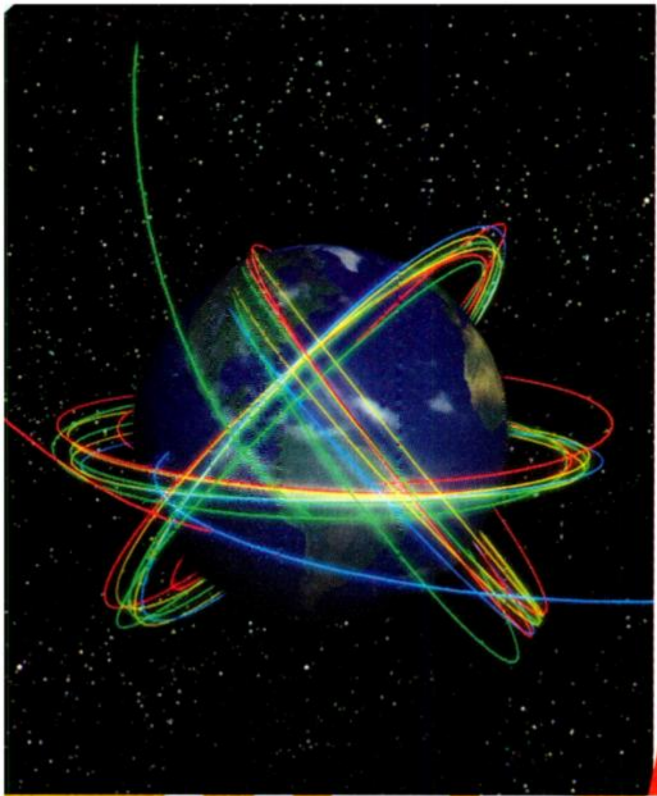
For additional details, call F. Neal Hunter at (919) 239-5119; or surf into *www.cree.com*. AB

Carbon Composite Material Found To Be Semiconducting

The first observation of semiconducting behavior in a carbon composite material was made by a student at the University of Buffalo, N.Y. Such a finding could revolutionize the fields of "smart" structures and electronics. This discovery lays the foundation for structural electronics—a new technology with the potential to provide structural materials with electronic capabilities without computer chips or electrical leads. Among the possibilities afforded by structural electronics include aircraft components that are huge energy-storage devices, solar cars with body panels that can store energy, and, eventually, computers without chips.

The new semiconducting material, made from carbon fibers embedded in a polymer matrix, would be easier and less expensive to fabricate than traditional silicon-based electronics. Because it would spread electronic capabilities over a much larger surface area, heat dissipation would no longer be a problem.

Carbon composites are known for their durability and light weight. They're used primarily in the manu-



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facture of aircraft parts, but are more frequently finding their way into automotive components, bridges, machinery, and sporting equipment. Currently, optical or electronic sensors that detect strain and deformation are embedded in carbon composites used to fabricate aircraft parts, a process that in itself can weaken the structural component rather significantly.

"In addition, these sensors can only be embedded in certain locations, not throughout the whole component," says Deborah Chung, PhD and professor of mechanical and aerospace engineering at the University of Buffalo, and principal investigator. "With this [new semiconducting] material, the whole piece is 'smart' and no electrical interconnection is needed."

For more information, contact the University of Buffalo's News Services at (716) 645-2626; fax (716) 645-3765. RE

Technical Standards Cater To Comm Needs For The Disabled

The International Telecommunication Union, Geneva, Switzerland, has finalized three recommendations aimed at enhancing the capability of the deaf or speech-impaired to use telecommunications.

The first recommendation, V.18, describes a multifunction text telephone that bridges the gap existing between several incompatible text telephones in use today. The second, T.140, adds new facilities to enable the use of different alphabets and character sets in text communications, such as Arabic, Cyrillic, Kanjii, and so on, as well as Latin-based characters. The third, T.134, describes how these facilities can be integrated in the multimedia systems defined by the ITU-T.

With these recommendations in place, disabled people will now be able to choose any combination of text, voice, graphics, and video for their communications. They'll be able to make their calls over the normal telephone network, using mobile phones, or over the Internet. V.18 and T.140 can be used immediately to improve text communication. The multimedia facilities will become increasingly useful as more multimedia devices come into use. For more information, call +41 22 730 51 11; e-mail: *itumail@itu.ch*; *www.itu.int/newsroom*. RE

Software NURBS Key To Speeding Electronic 3D Models

Designers of complex structures, whether they be toasters or nuclear reactors, often use computers to construct three-dimensional models electronically. Though effective, they suffer from a lack of speed—the more detailed these models become, the longer it takes to put these models in motion on screen.

Subodh Kumar, assistant professor of computer science at Johns Hopkins University, Baltimore, Md., has developed software that addresses this problem by significantly speeding up the way a computer re-displays a 3D model as it changes position. The program also gives designers greater control over the level of detail that appears on screen.

The secret to the software, says Kumar, is in how it handles Non-Uniform Rational B-Spline representations (NURBS). These are the mathematical shapes that computers can use to depict curved surfaces. A computer can put NURBS together to form a 3D representation of the complete object. The new software speeds up this process when an electronic designer is creating or refining a NURBS model.

Says Kumar, "This NURBS surface representation is in the computer's memory. It's data, just a sequence of bits and bytes that you can keep in a file and send to anybody. But how do you bring it back on screen and manipulate it in three dimensions."

One common technique is to convert the original model into numerous tiny triangles that, when assembled on the computer screen, look very much like the original shape. Each time the designer clicks a mouse to look at the model from a different point of view, the triangles must be re-displayed in a new way. The new software streamlines this task by generating far fewer triangles and taking several other technological short cuts. For further details, contact Johns Hopkins University at (410) 516-7160; *www.cs.jhu.edu/*. RE

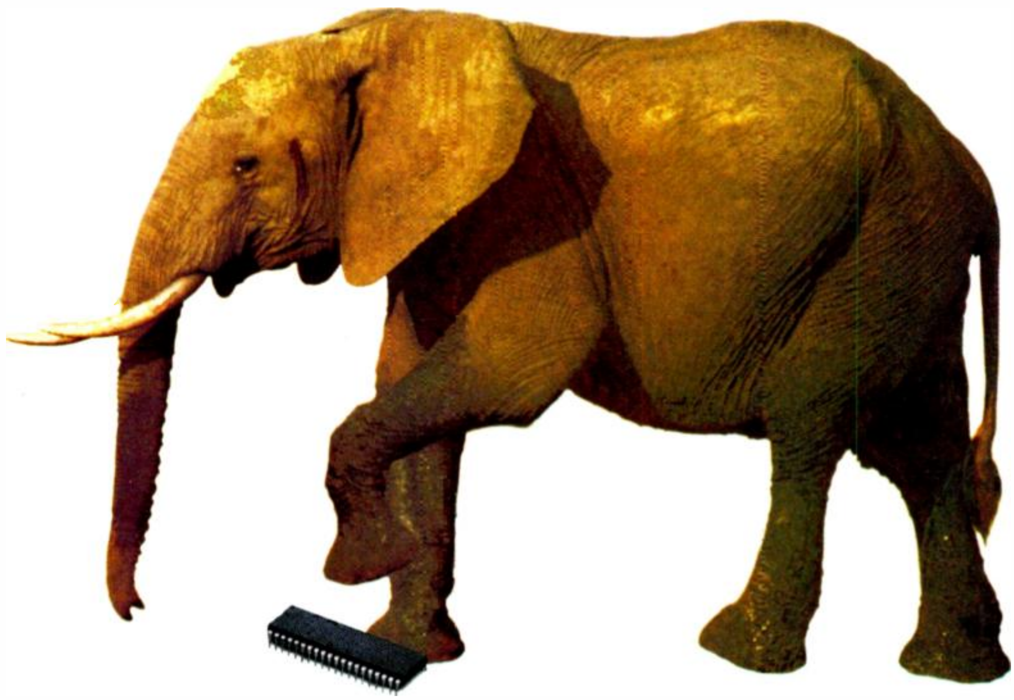
Low-K Dielectric Materials Target Sub-0.18-μm IC Manufacturing

In response to system performance requirements that are driving line widths ever smaller, AlliedSignal Inc., Los Gatos, Calif., has developed a low-k dielectric material for next-generation, sub-0.18-μm semiconductor manufacturing applications. Designated the Flare 2.0, the material, which provides gap fill and insulation functions between metal layers, features high thermal stability, low moisture absorption, and a high glass transition temperature.

To date, available technologies have provided materials with dielectric constants above 3.0, a figure deemed ineffective in meeting the manufacturing demands of future generations of semiconductor devices. The Flare 2.0, the result of research undertaken into spin-on dielectrics by the company's Advanced Microelectronic Materials (AMM) unit, has a constant of 2.8. The material exhibits no change in dielectric constant over the temperature range of 385° to 450°C, it has a glass-transition temperature of over 400°C for a larger procession window, and is temperature-stable up to between 425° to 450°C. For more information, call Karen Hopkins at (408) 341-3055; fax (408) 341-3001; e-mail: *karen.hopkins@alliedsignal.com*. PM

Edited by Roger Engelke

IS FLASH SMASHING EPROM?



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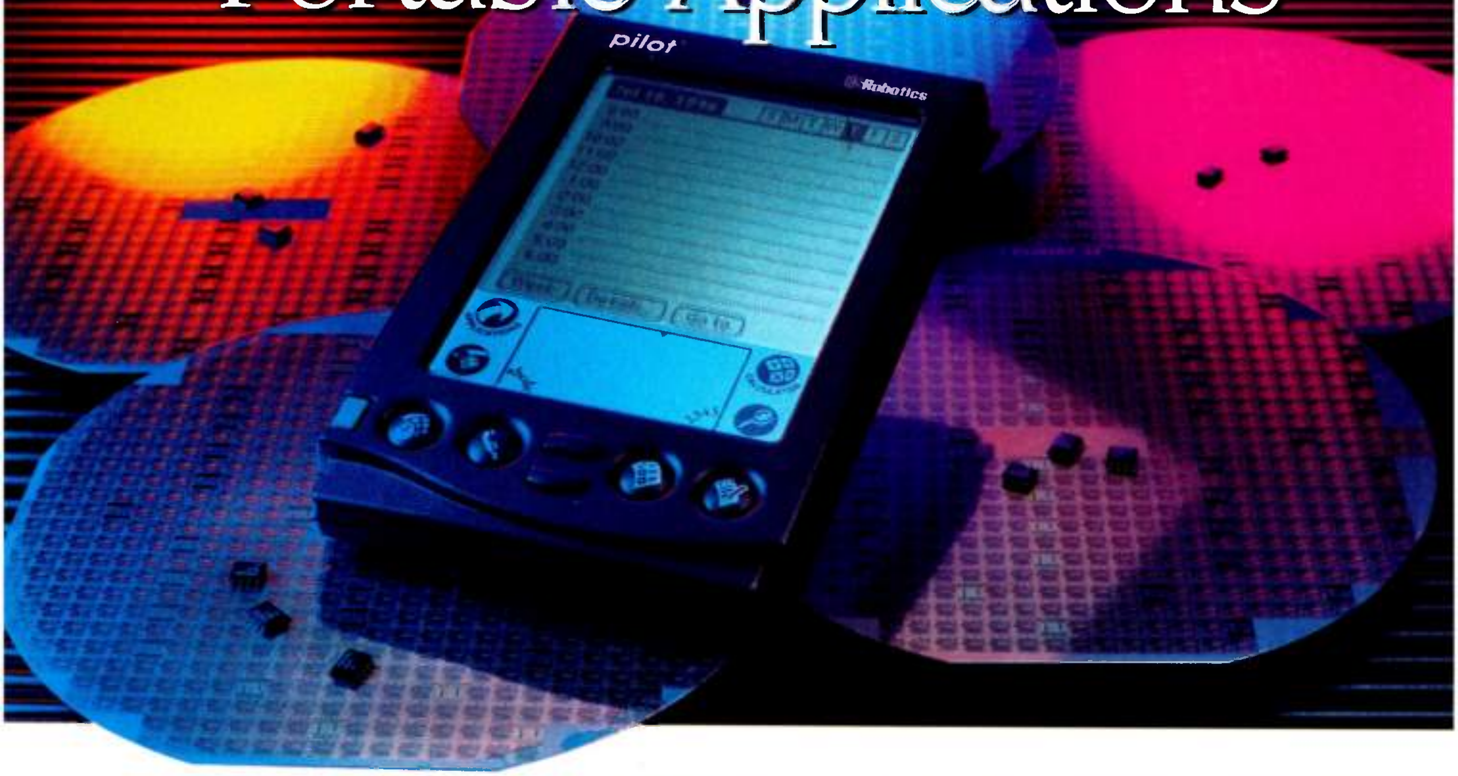

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SP4415	2.2V to 3.6V	5mA[1]		4 selectable light levels	Watches, Games, Apparel, Small LCD Displays
SP4422A	2.2V to 6V	8mA[1]	•	Requires minimal board space	Remote Control Units, Portable Instruments, POS Terminals, LCD Displays
SP4423	2.2V to 6V	5mA[1]	•	Low Power	PDA's, Calculators, LCD Displays
SP4424	1V to 6V	6mA[2]	•	Dual oscillator for coil and lamp control	Pagers, Digital Watches, LCD Displays
SP4425	1V to 6V	37mA[2]	•	Max light output @ low voltages	Pagers, Cell Phones, LCD Displays
SP4430	1V to 3V	75mA[3]	•	DC/DC converter	Cell Phones, PDA's, Pagers

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Ultra-wideband Optical Amps Allow Terabit Data Transmissions Over Long Distances

Scientists from Bell Labs, the research and development arm of Lucent Technologies, have demonstrated the world's first long-distance transmission of a terabit (trillion bits) of data per second over a single strand of optical fiber.

Using a new optical-fiber amplifier, the signals were transmitted at a rate of 10 Gbits/s over each of 100 wavelengths, or colors, of light for distances of nearly 250 miles (400 km), more than twice that achieved in previous experiments. The experiment is expected to lead to the design of faster optical amplifiers for use in wave-division multiplexer (WDM) systems. Driven primarily by Internet use, explosive growth in the telecommunications industry has increased demand for high-capacity optical systems that employ WDM technology.

WDM involves transmitting digitized voice, video, and data in the form of light pulses over multiple wavelengths. The ultra-wideband optical amplifiers used in the Bell Labs experiment span almost seven times the bandwidth of optical amplifiers used in today's commercial WDM systems.

For the experiment, researchers used ultra-wideband erbium-doped silica-fiber amplifiers (EDFA). The high-powered, gain-flattened amplifiers had a large dynamic range.

The outputs of 100 lasers were combined using four 100-GHz waveguide grating routers. Of the total 60 channels in the C-band, the odd-numbered ones were multiplexed using one router and even-numbered channels using another *(see the figure)*.

The two sets of channels were interleaved and combined, with 50-GHz spacing. In the L-band, 40 channels with 100-GHz spacing were multiplexed using two routers, one with 32 and the other with eight channels.

The researchers combined the output of all four routers using a 4-by-1 coupler. The signals were modulated at 10 Gbits/s and amplified. At the end the of the system, the signals were amplified by an EDFA as the optical preamplifier and demultiplexed with a tunable optical bandpass filter. They were detected and split for clock extraction and data.

The company's new ultra-wideband EDFAs overcome the limits of conventional silica EDFAs on long-haul, commercial Dense WDM systems. They are expected to make feasible the transmission of 100 WDM channels with 50-GHz channel spacing, which is suitable for transmission links that cross the oceans. The gain spectrum of the two-band amplifier was flattened using long-period fiber grating fibers. A patent covering this technology has been filed.

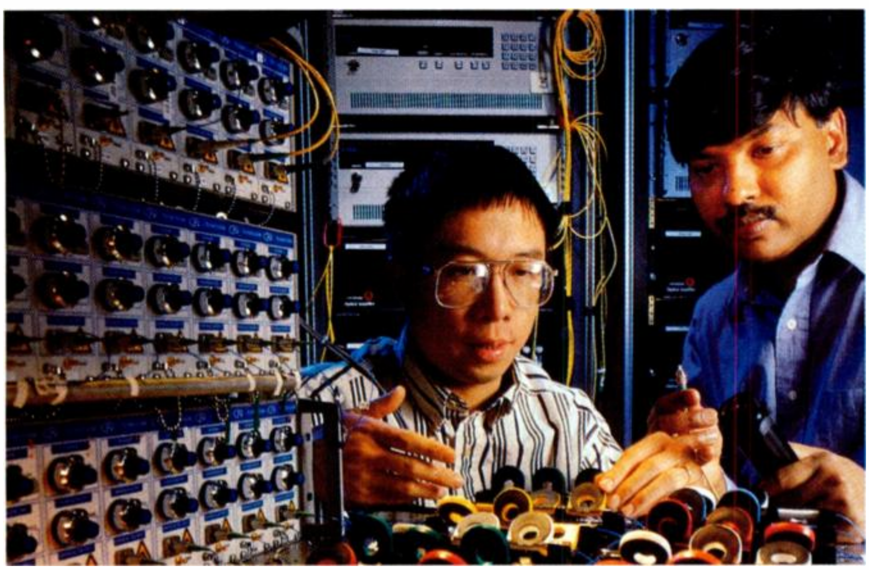
A research team led by Yan Sun and Atul Srivistava, both of Bell Labs' Photonic Networks Research department, presented the technical paper describing the long-distance, terabit transmission experiment at the Optical Fiber Communications conference.

In the past two years, researchers at Bell Labs and several other organizations have demonstrated terabit-capacity transmission over relatively short distances.

Kinchiro Ogawa, head of Bell Labs' Photonic Systems Technology Research department, presented a technical paper describing another high-capacity breakthrough: 1/2 terabit transmission, with 4 Gbits/s second carried over each of 30 wavelengths through 85 km of fiber.

More information is available on Lucent Technologies' web site at www.lucent.com.

Jeff Child



Bell Labs researchers adjust 400-km, 1-trillion-bit/s laser transmission experiment.

Low-K Dielectrics Being Characterized For Key Role In Copper Interconnects

Although copper interconnects have gained momentum recently, the full impact of the new technology cannot be realized without the use of appropriate material with low dielectric constants (K). Several candidates are vying for this application, including a variety of polymers, aerogels, and xerogels. Recent research indicates that these low-K interlevel dielectric (ILD) materials must be characterized in terms of their optical, thermal, electrical, and mechanical properties.

The material must be able to survive the processing conditions and also be compatible with the interconnect metal, according to a joint paper by researchers at the Center for Advanced Interconnect Science and

THIN-FILM PROPERTIES OF PMDA-TFMOB-6FDA COPOLYMERS AS A FUNCTION OF PMDA/6FDA DIANHYDRIDE RATIO

	Molar ratio of dianhydrides					
Number	PMDA	6FDA	Δn	Lateral CTE and temperature range	Thermal stress at 25°C	Tg
1	95	5	0.145	-3 ppm/°C (50-125°C) 29 ppm/°C (50-125°C) (175-300°C)	-12 MPa	>400°C
2	85	15	0.120	13 ppm/°C (100-200°C)	7 MPa	315°C
3	75	25	0.087	14 ppm/°C (100-200°C)	19 MPa	325°C
4	60	40	0.039	16 ppm/°C (100-200°C)	32 MPa	325°C

Technology, Rensselaer Polytechnic Institute (RPI), Troy, N.Y., and the Laboratory for Interconnect and Packaging, University of Texas (UT), Austin.

The researchers also note that these material property requirements will change with time, as supply voltages drop from the current 3.3 V down to nearly 1 V in the next couple of years, and to 0.55 V by 2012. According to the National Technology Roadmap for Semiconductors (NTRS), the dielectric constant requirements will drop from about 3.0 in 1997 to 1.5 to 2.0 in 2006, and 1.5 by the year 2009.

In general, scientists are investigating two types of materials. In the polymer group, both fluorinated and nonfluorinated dielectrics are being examined, while the second group comprises aerogels and xerogels.

The researchers at RPI and UT are exploring fluorinated polyimide films for the application. They have already summarized some of the results obtained concerning electrical and thermal properties, moisture uptake, and bonding behavior as a result of processing, as well as the changes in the film structure. In fact, tests on four varieties of PMDA with different concentrations of flexible 6FDA indicate the dependence of thermal stress on chemical structure, with stresses increasing as the coefficient of thermal expansion (CTE) of the copolymer increases *(see the table)*.

The RPI/UT paper also identifies test methods used to characterize these films. This characterization was conducted using film thickness as close as possible to that required for the ILD application.

These results were presented as part of an invited paper entitled "Characterization of Low-K Materials for Interlevel Dielectric Applications" at the recent Dielectrics for ULSI Multilevel Interconnection Conference in Santa Clara, Calif.

For further details, call Shyam Murarka at (518) 276-2978, or e-mail smurarka@unix.cie.rpi.edu

Ashok Bindra

Tests Prove Feasibility Of 11-Mbits/s Wireless Network Technology

Harris Semiconductor has tested the operation of a new wireless 11-Mbit/s radio technology that operates in the 2.4-GHz industrial, scientific, and medical (ISM) band. During the test, two radio transceivers—each equipped with a new 11-Mbit/s baseband processor Harris makes—successfully linked and communicated continuous packets of data at an effective data rate of 8.5 Mbits/s. In addition, part of the test included operation in close proximity to a high-power microwave oven to test the effects of interference.

The 11-Mbit/s WLAN promises a performance level comparable to a 10-Mbit/s Ethernet system. The operational test was aimed at addressing two major issues:

•The achievement of wireless networking that's as fast as current wired networks, and

•The concern that interference will either disrupt communication or seriously impede performance.

The Harris tests show that high data rates can be achieved in the 2.4-GHz band and that acceptable data rates can be maintained, even in the face of microwave interference.

Test engineers at Harris' radio test laboratory in Palm Bay, Fla., evaluated performance of the WLAN system while subjecting it to industrial microwave oven interference. A microwave oven cooks food by emitting microwave radio signals; some of these microwaves escape the enclosure and can interfere with any radio transmissions in the 2.4-GHz ISM band.

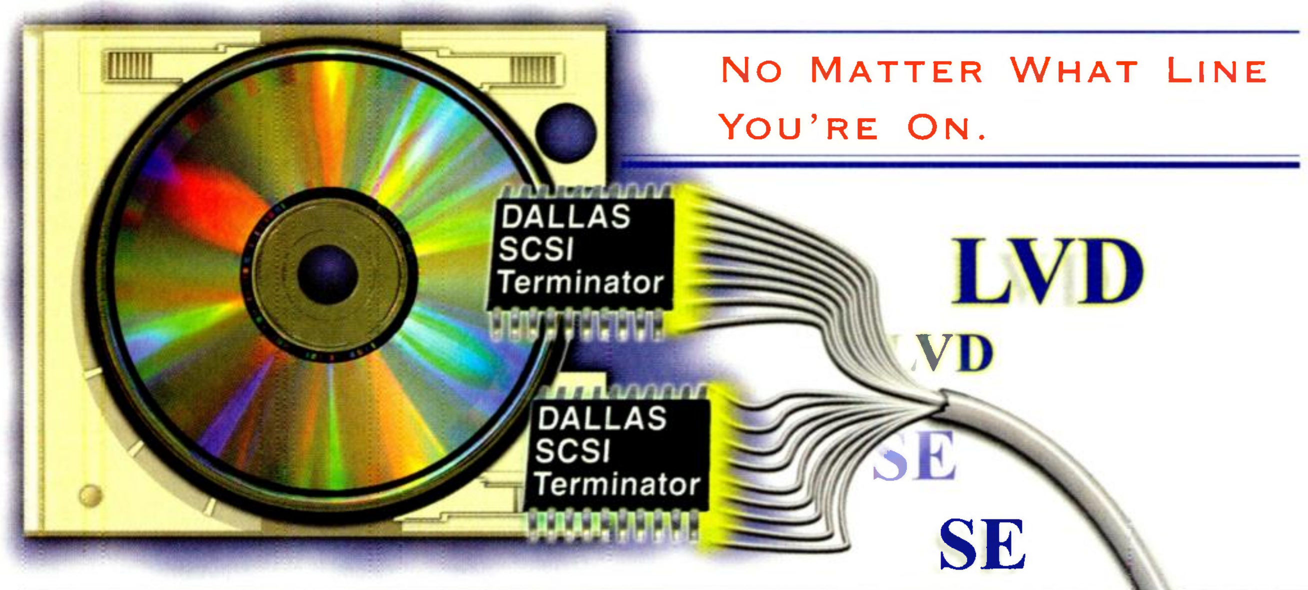
The demonstration unit uses a new Harris 11-Mbit/s baseband processor chip that dramatically improves wireless data rates. Called the HFA3860, the processor provides all the baseband transmit-and-receive functions required for the 2.4-GHz ISM unlicensed band on a single chip; it requires no external components. It also can achieve fallback rates to 5.5 Mbits/s to extend range—or to 1 and 2 Mbits/s, making it compatible with IEEE-802.11-compliant systems.

During the test, two radio transceivers and controlling computers were located in the Harris radio testing lab. One transceiver was placed at varying distances from six inches to six feet from an operating microwave oven. The other was located at a fixed five meters from the oven. The test was conducted over all 11 channels in the ISM band as defined by the IEEE-802.11 standard. Results showed an effective data rate of 8.5 Mbits/s with the oven off. With the oven operating, a strong data link was maintained over all 11 channels with packet throughput rate being typically reduced by less than 10%.

For more information, contact Harris Semiconductor at (407) 729-4928 or on the World Wide Web at www.semi.harris.com.

Jeff Child

THE BUS STOPS HERE.



The DS2118M Ultra2 LVD/SE SCSI Terminator from Dallas Semiconductor operates in three modes to simplify your design effort: SE (Single-Ended), LVD (Low-Voltage Differential), and HVD (High-Voltage Differential) isolation.

SCSI Standards Changing a Little Too Fast for You?

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The DS2118M provides 5% tolerance over the full temperature range on both LVD and SE termination resistance—the lowest in the industry. It also has a mere 3pF of power-down capacitance. Available in a 36-pin SSOP package, the DS2118M provides active termination of 9 signal line pairs.

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Electromagnetic Simulation Moves From Analysis To Design

Dramatic Speed Improvements And The Use Of Optimization Technology In Software Automates The Simulation Process.

Cheryl Ajluni

Electromagnetic (EM) simulators have traditionally been used as back-end analysis tools to verify the results of circuit simulators. They work by accurately modeling the physical effects in a variety of structures ranging from transmission lines to planar circuits and to general 3D structures. If the design looks good after EM simulation, it then proceeds to manufacturing. If, on the other hand, the tool picks up physical effects that changes the design's performance adversely, then the engineer must go back and tweak the design to compensate for the performance degradation. The design is then resimulated and the results are verified yet again.

COVER FEATURE

This iterative loop continues until the engineer has successfully achieved the performance goal. Despite the fact that it can be quite labor-intensive and can steal precious time from the engineer's already short design cycle, this method requires that the engineer understand the circuit being designed in order to tweak it in the right direction. Otherwise, the engineer can do little more than hope that the change being made corrects the design's performance and the resulting designs are quite often sub optimal.

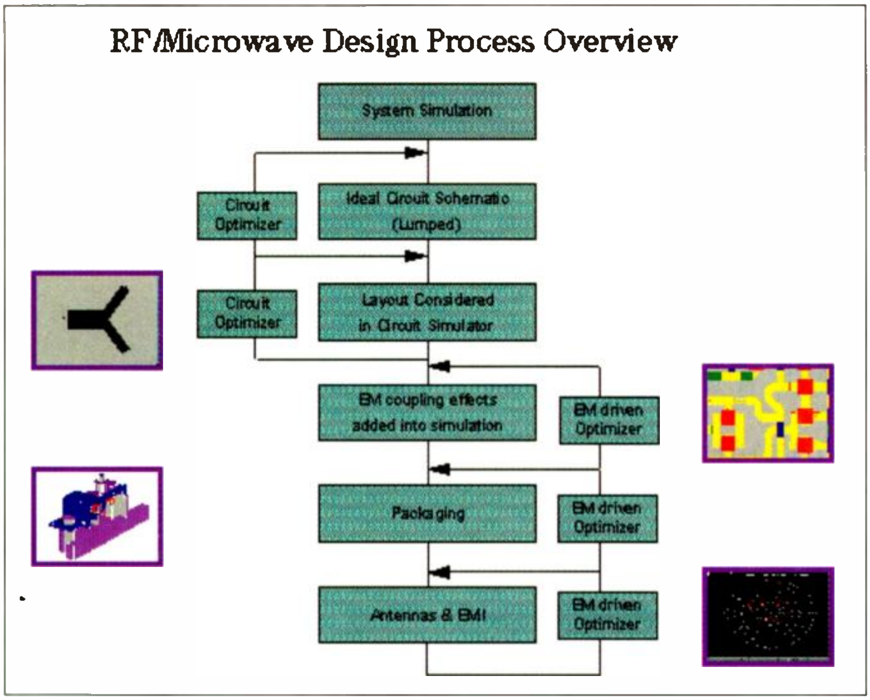
As microwave engineers begin to push the limits of currently available EM simulators, these difficulties become more pronounced. Overcoming these obstacles is not an easy process, requiring that EM simulator tools migrate further upstream in the design cycle and forcing tool vendors to reassess their using EM simulation tools altogether.

One EDA tool vendor, HP EEsof, Westlake Village, Calif., has come up with a solution that transparently thrusts EM simulation directly into the circuit design process *(Fig. 1)*. Known as HP HFSS Designer, this general-purpose solution for modeling arbitrarily shaped, passive 3D structures is not just a circuit design analysis tool. Rather, it allows the designer to specify a circuit's performance objective upfront, along with the design parameters and ranges. The EM engine then, in an intelligent manner, tries out possible solutions, making changes as each option is explored by the designer to check out performance. When this automated process is complete, the engineer has an optimal design with design parameters optimized with respect to the performance objective; all the while leaving him or her free to work on other aspects of the design. By successfully enabling EM simulation to move from analysis into design, the HP HFSS Designer tool is likely to create a paradigm shift in how circuits are designed.

The HP HFSS Designer tool is specifically targeted for use in the design of high-frequency circuits. Applications include the design and analysis of antennas, machined components such as waveguides, RF and microwave circuits, packages, and high-speed digital circuits.

The HP HFSS Designer tool is based on the company's HP HFSS 5.1 tool released last month. The original version of the tool, HP HFSS 5.0, was developed by HP EEsoft as a next generation product to the HFSS 4.0 tool developed by Ansoft, Pittsburgh, Pa., and marketed and sold by HP EEsoft.

HP HFSS Designer's uniqueness stems from its high performance and utilization of novel optimization tech-



1. This flow chart provides an overview of the RF/microwave design process, clearly showing how the HP HFSS Desginer tool can be inserted into this process.

nologies that enable it to be used as an integral part of the design process. HP HFSS Designer also offers improved usability through better performance of the post-processor and enhanced database updating. The result is a tool that effectively automates the process of manually changing the physical model of the design and enables the engineer to optimize the design for performance before the prototype phase of the design cycle—both of which give way to significant reductions in design time, as well as time-to-market.

HP HFSS Designer's high performance is attributed to significant speed and accuracy improvements made by the company in its new releases of HP HFSS 5.0 and HP HFSS 5.1. Speed is an especially crucial factor in allowing EM simulation tools to migrate from analysis to design, because EM simulation typically takes such a long time; in some cases, only allowing two to three runs per day. At these speeds, the exploration of different design options becomes an impossibility.

To deal with this issue, HP EEsof made significant changes to the HFSS 4.0 master code, resulting in a 20× speed improvement found in the HP HFSS Designer tool. Other speed improvement factors include a combination of code profiling, algorithmic improvements, and the use of better compilers. In addition, a new mesher was developed that requires fewer unknowns to solve a given problem and can handle more extreme solid-model aspect ratios. A new solver also was added to the mix.

While the speed capability of the EM simulator is itself a significant feature, it is the utilization of optimization technology that ultimately breaks EM simulation out of its role as a back-end analysis tool. This is because it effectively allows the designer to now simulate multiple structures, as opposed to simply a single structure.

The optimization technology utilized in the HP HFSS Designer tool hails from Optimization Systems Associates, Inc. (OSA), Ontario, Canada, a company acquired by Hewlett-Packard last November. It works by allowing the designer to specify geometry parameters and associated ranges, thereby optimizing the performance of the circuit according to predetermined specifications or certain goals related to circuit performance *(Fig. 2)*.

During a typical design scenario, a designer begins with a nominal project and a set of projects describing the directions of change. Each design parameter has an associated extra project that describes the change resulting from a variation in that particular design parameter. This means, for example, that if the length of a transmission line stub is varied, then there are two projects—the nominal one, and a project describing the circuit with a transmission line stub. Given the nominal project and the directions of change, the user can then specify the variables and their respective ranges (lower and upper bounds).

Next, performance objectives are specified and the optimizer has all the input required to optimize the circuit. It does that by taking different samples in the parameter space. To minimize the number of EM simulations, the optimizer uses interpolation techniques to build a multidimensional response surface. The optimization module then adjusts the variables automatically utilizing gradient information to meet performance specifications.

As Niels Fache´, HP EEsof's product marketing manager, explains, "A designer of a filter can specify design parameters such as stub lengths and spacings which vary between certain lower and upper values. Then the designer defines a desirable response of the filter (bandpass and stop bands). The optimizer will search for the optimal value(s) of the parameter(s) such that the goal(s) can be reached in a minimal number of iterations or EM simulations."

This capability, also known as automatic design refinement, effectively allows the designer using HP HFSS Designer to optimize for performance, in a matter of minutes to hours, depending on the complexity of the structure.

While there are other EM simulation tools currently on the market, no single tool had offered high-speed and high-performance EM simulation and optimization capability all in one. Although optimization techniques have been available for decades, they have often been relegated for use in circuit simulation. Applying optimization technology to EM simulation is an entirely new problem and is what makes EM-based automatic design refinement plausible.

What It Means

As the speed of EM-based simulators increases, designers can now solve real life problems much faster than previously possible. With the optimization capabilities, HP EEsof's EM-based tool becomes a true design tool and an integral part of the design process. As

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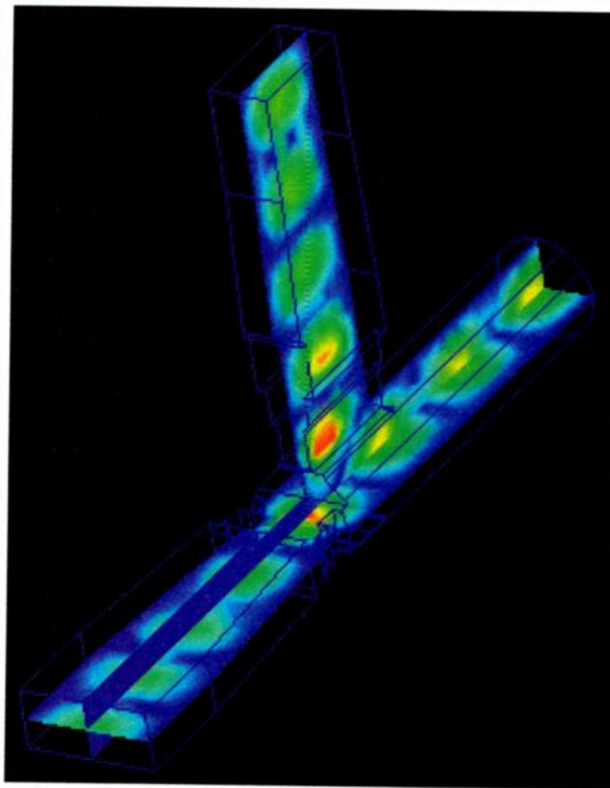

2. This graphic illustrates an example ofa typical 3D structure being optimized to achieve a designer's specific performance objectives, using one ore more design parameters.

Fache´ points out, "Designers may still use their traditional design methodologies including circuit analysis. However accurate and optimal results can only be obtained by using the HP HFSS Designer tool."

The ability to access EM simulation in the design phase offers a number of benefits to the designer, not the least of which is shortened design cycles. This is partially due to the fact that since the EM simulator runs faster, more iterative EM simulations can be run in the same amount of time. At the same time, designers can expect that the EM simulation runs will produce predicted performance results that better match the measured performance.

Another benefit of moving EM simulation into the design cycle is a decrease in the amount of engineering time spent refining the structure until a desired performance is reached. This results in an immediate productivity gain, since it reduces the need for the designer in the process. As Fache explains, "In many cases, refinement of a structure takes literally dozen of reruns. But, in the real world, people don't have the time to set up and run that many examples. Quite often, designers will make a few changes and work with a suboptimal structure. With the new optimizer capability, a designer can set up the problem and doesn't have to look at it until the process is completed."

As a result, whereas designers currently have to wait for the simulation to be complete and then start a new simulation, with HP HFSS Designer, this process is fully automated leaving the designer free to focus more on the design rather than on a series of EM-based simulations. HP EEsof estimates that design time might drop by an order of magnitude.

Another interesting benefit is the ability to allow designers to try out new, more complex designs that were too challenging for existing EM-based tools due to time and memory considerations. This is significant because designers were once limited by how well they knew and understood the various electromagnetic effects in their circuit. For example, designers of integrated circuits are often conservative in using real estate space to not deteriorate the performance of their designs. With HP HFSS Designer, designers are no longer forced to work this way. And, because there now exists an automated way to optimize parameters with respect to performance goals, designs will get better and the overall circuit and system performance will improve.

PRICE AND AVAILABILITY

HP HFSS Designer is now available and sells for $43,000. The optimization module, which sells as an external controller, also is available for $20,000. A fully integrated HP HFSS Designer and optimization solution is expected to be ready around October. The software runs on both Unix platforms, and PCs running Windows95 and Windows NT 4.0.

Hewlett-Packard Co., HP EEsof Div., 5601 Lindero Canyon Rd., Westlake Village, CA 91362; (818) 879-6200; Internet: www.hp.com/go/hpeesof. **CIRCLE 525**

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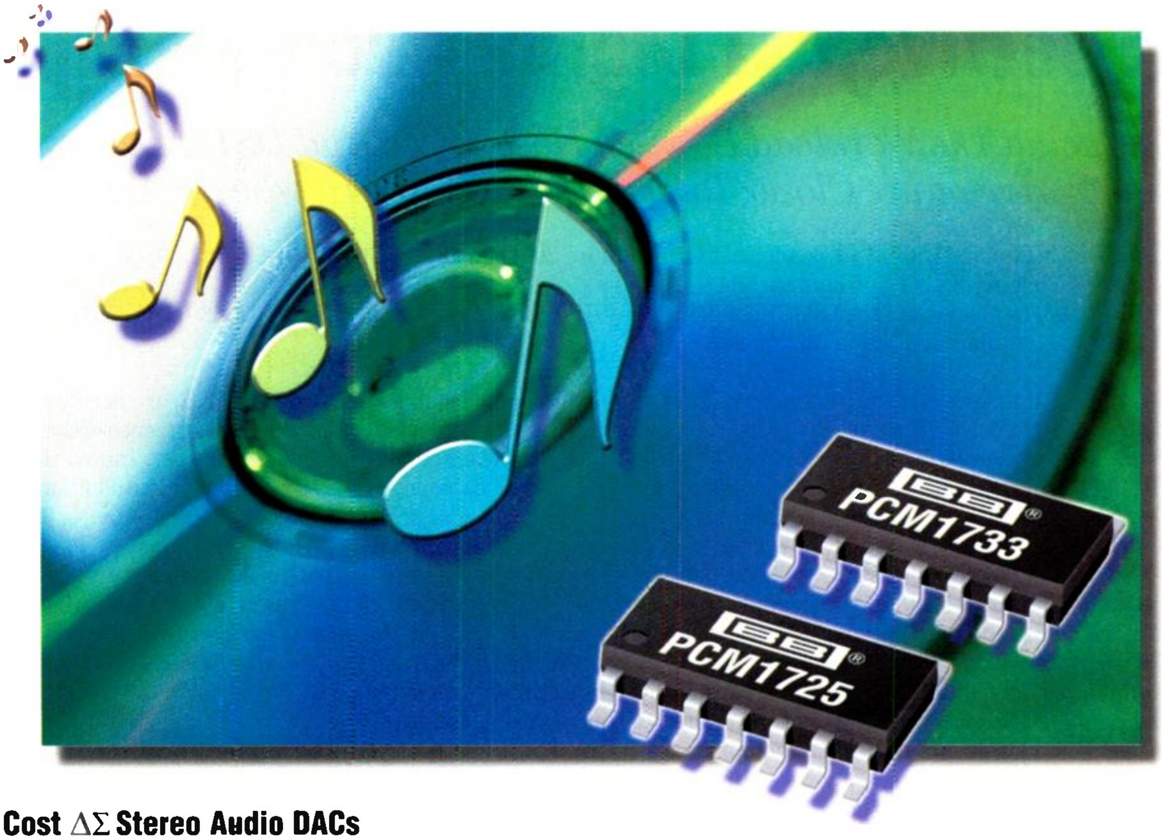

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PCM1725	DAC	16	95dB	97dB	–84dB	96kHz	+5V	14-Pin SOIC	11373	85
PCM1733	DAC	18	95dB	97dB	–84dB	96kHz	+5V	14-Pin SOIC	11435	86
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DESIGN APPLICATION

Use Programmable DSPs For Cost-Effective PCI Digital Audio Design

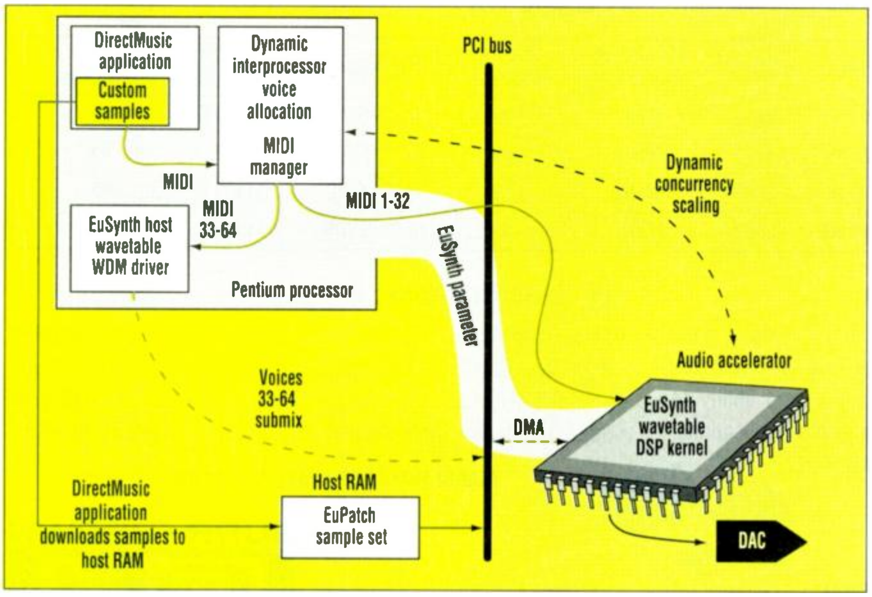
Balancing The Workload Between Host CPUs And DSP Accelerators Brings Performance Closer To That Of Dedicated Hardware Accelerators.

JEFFREY BARISH, EuPhonics Inc., 4840 Pearl East Circle, Suite 201E, Boulder, CO 80301-6115; (303) 938-8448; fax (303) 938-8885; e-mail: jb@EuPhonics.com.
JOHN CROTEAU, Analog Devices Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106; (781) 461-4010; fax (781) 329-1241; e-mail: john.croteau@analog.com.

Designing computer systems involves difficult cost-performance trade-offs. It's a given that systems offering the highest performance levels—high concurrency, sophisticated new features, and the highest quality levels—will always require hardware acceleration. At the other end of the spectrum, the increasing performance of host processors will never outpace the growing demands of applications for additional computation. But shrewd designers can find a successful middle ground between the two extremes. By way of illustration, consider what's happening with PC audio.

PC audio is undergoing a profound metamorphosis. Driven by new 3D games, published DVD movie content, and live audio downloaded from the Internet, future PCs will be offering more audio-related features and higher levels of performance. Music synthesizers will sound more realistic and be capable of creating a wider variety of sounds. It will be possible to position sound effects 360° around the listener without the expense and hassle of wiring additional rear channel speakers. Users will be listening to 5.1-channel sound tracks from DVD as well as musical accompaniment to Internet web sites. These applications are only the tip of the iceberg.

However, these new capabilities can only reach mass market prices through architectural innovation. Audio signal processing consumes significant computational resources. Running all the audio functions on the host processor attenuates system performance on other applications. Hardware accelerators preserve the performance of the host CPU, but they add cost. Innovative system design minimizes the additional cost and saves system performance.



The SoundMax 64 reference design splits up signal processing chores between the host CPU and a PCI-based programmable DSP. For example, the first 32 MIDI voices are handled by the DSP, and up to 32 additional voices are handled by the host CPU when needed.

Audio Accelerators Needed

System architects have a spectrum of options available for implementing audio subsystems that trade hardware cost for performance. The ends of the spectrum are well-defined. At one end are the basic, sub-$1000 systems. They run most signal-processing tasks on the host CPU, an architectural philosophy known as Host Signal Processing (HSP). This is done using an audio codec to provide baseline recording and playback functionality. At the other end are the performance systems. They rely on hardware ASICs or DSPs to implement signal-processing tasks.

To understand the rationale for adding hardware acceleration, hypothesize a set of signal-processing functions at a particular performance level, running entirely on the host CPU. Recognize that each real-time audio task steals cycles from other graphics, data, or numeric processing tasks. So, above 10% to 20% loading, the signal-processing burden detracts noticeably from the execution speed of the applications.

For example, a game's graphics will be noticeably slower; the game might respond to user control more sluggishly. Consumers who purchase a computer with a 300-MHz Pentium processor, half of which is consumed by signal-processing tasks, will find that applications will run as if the computer had a 150-MHz Pentium processor. Also, cramming too many real-time algorithms on the host CPU can lead to

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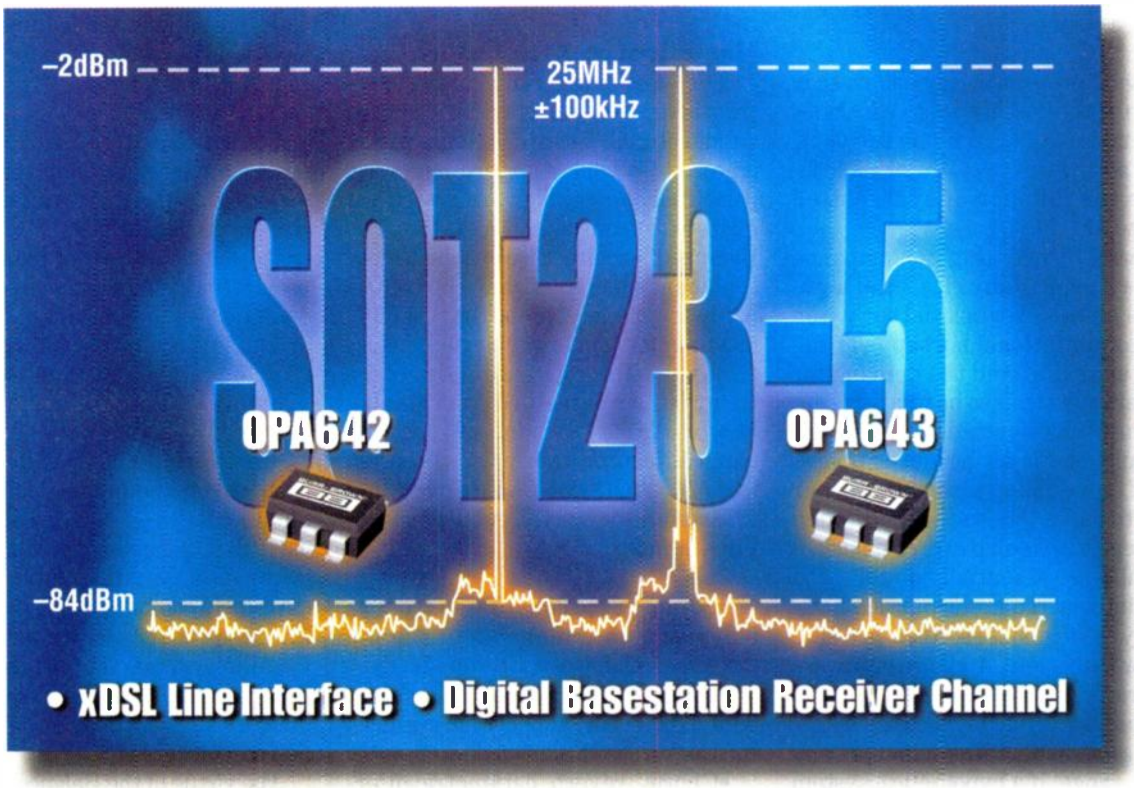

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After defining a set of signal-processing functions that do not impose an excessive burden, consider the following three points:

• Signal-processing capabilities span a range. If the baseline system includes a wavetable synthesizer with 24 voices, adding a hardware accelerator could increase the number of synthesized voices to 64.

• Signal-processing performance spans a range. Many classes of algorithms sound or work better when more computational horsepower becomes available, and the demand for MIPS always seems to be insatiable.

A wavetable synthesizer, for example, could use "layering" (the application of more than one oscillator per voice) to make the synthesized sound more realistic. Adding even a single additional layer essentially doubles the computational requirements, and high-quality synthesizers often provide three or four layers. Adding a hardware accelerator improves sound quality in the case of wavetable synthesis.

• Signal-processing concurrency spans a range. If a hypothetical system offers wavetable, adding a hardware accelerator could make it possible to offer 3D positioning and a hands-free speakerphone as well. There is no limit to the cleverness of algorithm designers, so there will always be other useful algorithms cropping up. To run them concurrently would require PCs equipped with hardware accelerators.

More sophisticated capabilities, higher levels of performance, and concurrency all require more computation. This additional capability can be provided at any given time by a hardware accelerator, or perhaps in the future by faster CPUs. Thus, performance systems are bellwethers. As CPUs get faster, PCs using them may acquire additional capabilities that previously required hardware accelerators to implement. However, the other applications also will increase their computational requirements, limiting the CPU performance available for signal processing. Consequently, it's very difficult to predict when host processors will be sufficiently powerful to run not only today's signal processing tasks, but also tomorrow's applications. These two architectural philosophies, host signal processing and hardware acceleration, define the endpoints of the spectrum of implementation options.

The Balanced Architecture

The vast middle range of the spectrum is served by an elegant "Balanced Architecture." This architecture makes it possible to achieve approximately the performance of the high-end systems at mainstream consumer price points. The Balanced Architecture reconciles the conflicting objectives above by using a hardware accelerator and the host CPU in a uniquely synergistic manner *(see the figure)*. This reference design of the Balanced Architecture from Analog Devices is called SoundMax 64 with dynamic interprocessor voice allocation *(see "The AD1818A-Based SoundMax 64 Accelerator," p. 48)*. Additional features include:

•Sample rate conversion from as many as eight independent sample rates, and mixing of the results.

•DirectInput-compatible analog/digital game port support for joysticks such as Microsoft Sidewinder.

•Chorus, reverb, parametric filtering, and dynamic LPF audio effects.

•ACPI- and On Now-compliant PCI power management.

To understand the Balanced Architecture concept, consider first the characteristics of the hardware accelerator. The ideal hardware accelerator (for either dedicated or balanced architectures) incorporates both a programmable core and some fixed-function circuitry. The programmable core preserves the advantages of programmable systems. These advantages are:

• Software solutions afford the possibility for the same hardware to be reconfigured to serve multiple functions—for example, a Dolby Digital decoder in a DVD playback scenario or a wavetable synthesizer in another.

• Software solutions allow field driver upgrades to support evolving standards—for example, alternative multichannel audio decoders such as MPEG-2, DTS, or Sony's new DSD standard.

• Software solutions accelerate development. Bugs in fixed-function hardware require redesign and modifications to masks; bugs in software can be fixed by changing the code.

• Software solutions make it easy to accommodate OEM customization in audio algorithms and feature sets such as dynamic equalization for a specific set of OEM speakers.

To reduce cost, the hardware accelerator implements common immutable operations in fixed-function form, thereby saving DSP MIPS for the functions that benefit most from them. A prominent example of a common audio operation is the sample-rate conversion and mixing required by Microsoft's DirectSound API. Mixing is required whenever there are more than two sources of audio.

The PC98 specification co-developed by Microsoft and Intel specifies support for at least seven sample rates, so it is likely that the mixing operation also will require sample-rate conversion—an extremely compute-intensive function. The requirements for sample-rate conversion and mixing are unlikely to change dramatically, so it is sensible to build these operations into fixed-function hardware.

The virtue of the Balanced Architecture becomes apparent when considering the requirements for the wavetable synthesizer. Historically, the polyphony requirements for wavetable synthesizers were determined by the General MIDI standard, which calls for 24 voices. However, the polyphony requirements will be driven to 64 voices this year by a component of the DirectMusic Core that supports downloadable sounds through the MIDI Manufacturers Association's DLS 1.0 specification. DLS lets developers use the wavetable synthesizer to support sound effects as well as the musical accompaniment.

For example, the game could download the sound of a laser blast once, and then trigger it numerous times using MIDI commands. Or better yet, it could download the engine drone of a race car and then pitch-shift it in the synthesizer as the car accelerates or decelerates. The 64-voice polyphony empowers wavetable synthesizers to support not only the requirements for musical accompaniment, but the requirements for sound effects as well.

Although synthesizers must be capa-

The AD1818A-Based SoundMax 64 Accelerator

The reference design includes the AD1818A accelerator, one or more audio codecs, and all required software to implement the balanced architecture. The design combines full-featured DirectX audio and telephony acceleration, supports PCI bus master/targeting, and complies with the Rev. 2.1 PCI bus interface. The 64-channel scatter-gather DMA support enables efficient use of host memory. The bus redirection mechanism supports USB and 1394 audio peripherals. The PCI and DC 97 controllers support advanced configuration peripheral interface (ACPI) and On Now compliant PCI-PM advanced power management.

The AD1818A uses a programmable DSP core to implement certain functions driven by two application scenarios:

Gaming
- DirectSound3D: eight streams
- DirectMusic: 32-voice DLS-1 wavetable synthesis
- Spatial enhancement (broadening of the stereo sound stage)

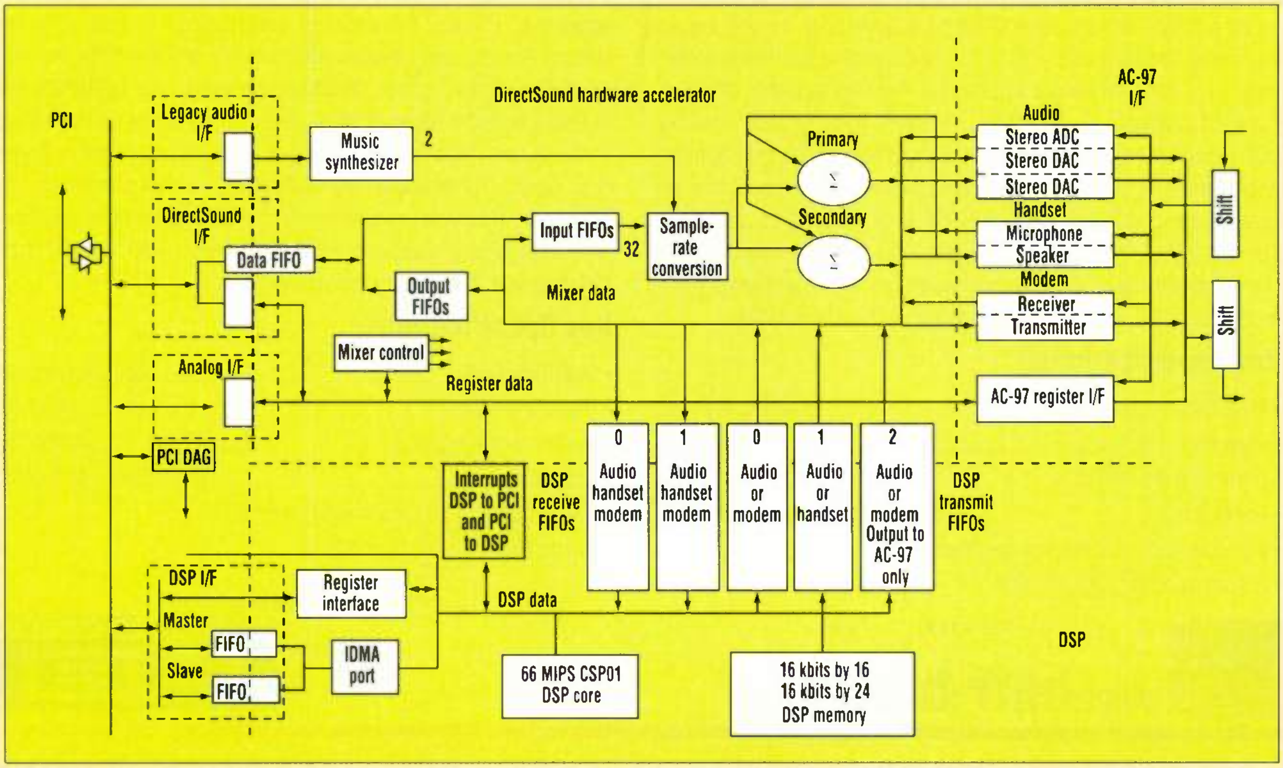
DVD playback
- Dolby Digital or MPEG-2 audio decoding
- 3D positioning (for virtual surround)

The SoundMax 64 includes a 66-MIPS, 733-MOPS DSP core from Analog Devices. It has integrated 16 kbits by 16 and 16 kbits by 24 SRAMs (80 kbytes)—sufficient for the computational needs of polyphonic wavetable synthesizers, 3D positioning algorithms or Dolby Digital (AC3) decoders.

The 64-channel DirectSound mixer is equipped with variable-sample-rate conversion to relieve the host CPU of a significant computational load. Sampled data streams must all be precisely the same sample rate before they're mixed, to avoid clicks, pops, and distortion due to rate mismatch. Variable rate conversion answers this requirement transparently—the AD1818A supports eight sample rates simultaneously, including eight independent time bases. The on-chip OPL3-compatible music synthesizer, and MPU-401-compatible MIDI UART provide legacy music synthesis.

The AC 97-compliant AC-link interface uniquely supports four analog-to-digital converters and six digital-to-analog converters, totaling ten simultaneous streams of analog input and output *(see the figure)*. By combining an AD1818A with multiple AD1819A codecs, the following architectures are supported:

- Single codec designs: DLS Level 1 wavetable synthesis with spatial enhancement, DirectSound3D audio localization, Dolby Digital decode with virtual surround sound output
- Dual codec designs: Same as above plus concurrent V.34/56 kbytes/s data/fax/voice modem
- Triple codec designs: Same as above plus Dolby Digital decode with 5.1-channel surround sound output.



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ble of synthesizing 64 voices, they will rarely be called upon to deliver that many. Music scores generally require only 12 to 16 voices, so a synthesizer capable of only 32-voice polyphony will often suffice, even with the additional requirements imposed by sound effects. A hardware accelerator configured for 64-voice polyphony devotes expensive, power-consuming silicon real estate to functionality that will rarely be utilized.

The balanced solution takes advantage of these statistics. A MIDI dispatcher running on the host receives the commands that specify the desired sounds. It forwards these commands to the hardware accelerator as long as the accelerator has not reached its limit of 32 voices. After the hardware accelerator reaches this limit, the MIDI dispatcher routes any requests for additional voices to a synthesis engine running on the host. Both synthesis engines implement the same algorithm and use the same data set (which resides in host memory), so the sound that emerges is the same regardless of the platform on which the voice originated.

Because 32-voice polyphony covers most situations, the average load on the host CPU is negligible. Furthermore, the cost of a 32-voice hardware accelerator is half the cost of a 64-voice one. Also note that this balanced solution uses abundant, inexpensive, host DRAM to store the sample set, thereby avoiding the cost of additional memory. The hardware accelerator accesses the sample set over the PCI bus, which offers bandwidth to spare for this application.

Another advantage of this balanced solution is that it supports Dynamic Concurrency Scaling. To achieve the highest level of performance possible, DSP tasks always consume as much of the DSP as is available. If something happens that requires execution of an additional task, the running tasks receive a message requesting that they free up resources.

For example, in a pure gaming scenario, the wavetable synthesizer can run in a high-performance mode. If the PC switches to a scenario that also requires a modem (for telegaming, perhaps), the DSP frees resources either by shifting some voices over to the host engine, or dropping some refinements of the wavetable synthesis algorithm. Dynamic concurrency scaling assures that DSP resources are always utilized to the fullest extent possible, given the concurrency requirements at the moment.

The hardware accelerator connects between the PCI bus and the AC 97 audio codec. The bandwidth of the PCI bus supports audio streaming, and scatter-gather DMA provides access to host memory for storing the wavetable sample set. Saving the cost of the local memory chips required in ISA systems in itself provides a compelling rationale for the shift to PCI.

Another use for the PCI bus-mastering interface is for so-called "digital-ready" PCs. Digital-ready means that all digital audio created in the PC can be mixed in the PC and sent to USB speakers or IEEE 1394-enabled consumer A/V appliances. Deferring the inevitable conversion from digital to analog may preserve audio fidelity. In fact, someday it will be commonplace to render the digital audio to analog outside of the PC. Until then, Digital Ready configurations make it possible to use digital links optionally. The primary digital audio output of the hardware accelerator is through an AC-link to a companion AC 97 Audio Codec.

In the foreseeable future, systems offering the lowest cost will always be based on HSP. During the time a particular feature set migrates from pure hardware acceleration to pure HSP, the balanced architecture will make it possible for moderately priced systems to support the capabilities of the performance systems with only a trivial cost-performance penalty.

Dr. Jeffrey Barish is founder and president of EuPhonics, a software firm specializing in digital audio and digital music synthesis products for the worldwide semiconductor industry. He is also a professor of electrical engineering at the University of Colorado at Boulder. Barish has a PhD and MSEE from Stanford University, Stanford, Calif., and a BSEE from the Massachusetts Institute of Technology, Cambridge, Mass.

John Croteau is director of strategic marketing for the PC segment at Analog Devices. He is responsible for digital audio, video, 56 kbytes/s and broadband modems, as well as motherboard power and thermal management programs. Croteau holds a BSEE from Penn State University, University Park, Pa.

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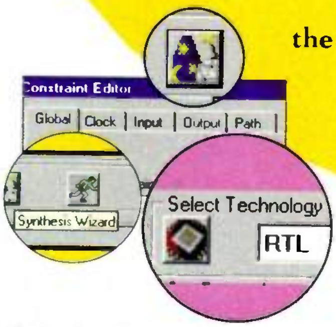

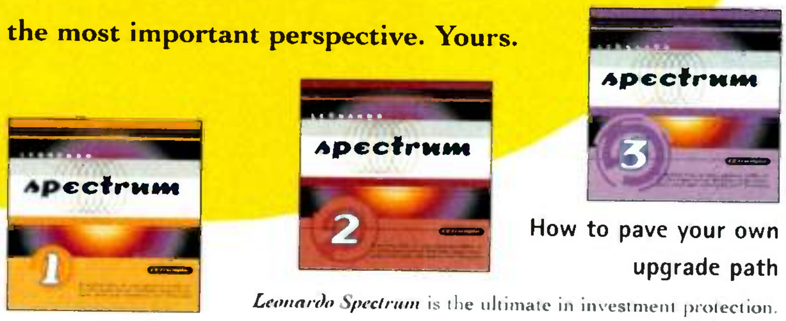

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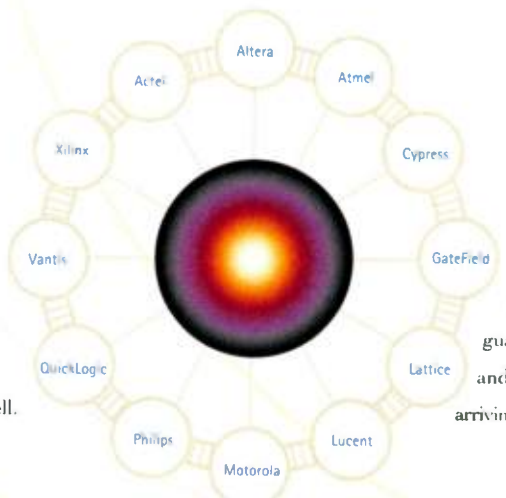

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EDA WATCH

A New Engineering Resource: Web-Based Design

Engineers have probably been using the Internet longer than any other group of users, having identified it as an ideal means of communication and distribution of information. The amount of pertinent information, data sheets, part numbers, and application notes on the Internet increases daily. But, until recently, limitations, such as lack of data, difficulty in finding data that *is* there, and variations in formats have hampered its ease of use as a true engineering resource.

In the real world, design engineers are being called on to deliver prototypes in shorter time spans. Such compressed product cycles don't allow for extensive ongoing product redesign or refinement. As a result, the component selection process often determines the delivery date and the prototype's ultimate production viability. The appeal of the web lies in its ability to provide rapid access to the information engineers need to complete designs in a timely manner.

Most manufacturers' web sites have good product information. However, with more than 200 IC manufacturers, and over 1000 electronic parts suppliers each having a web site, even the most skilled web searcher may not be able to track down part numbers and data sheets. In most cases, the engineer is left to sort through manufacturers' web sites, weeding through thousands of pages of information and data. This undermines the promise of the Internet as a succinct and time-saving tool, often turning it into an exercise in futility.

Until recently, the responsibility for literature fulfillment within the industry was shared primarily by manufacturers and their authorized distribution channels. Printed databooks and the trade press remain the primary media for delivery of product information—although CD-ROM and web-based documentation have seen significant growth in the last two years. Literature fulfillment, outsourced by many larger companies, is also used. It is usually found with "800" telephone numbers to qualify potential purchasers, and is provided by independent third parties.

During the design process, the engineer is generally presented with a system specification that describes end-product features and capabilities in great detail. Besides the product's features, this detail includes the form factor, power, and manufacturing cost targets.

A typical design process follows these steps:

- The designer first defines the product requirements in basic blocks, i.e., processor, input/output, memory, etc.
- The designer then selects ICs that solve individual design problems.
- Most designers insist upon reviewing many potential circuits because no individual product offers a perfect solution.
- Individual circuit characteristics are compared and negotiated in relation to all other circuits.
- Once circuit selection is complete, design simulation begins. Simulation is a multistep process and dictates ongoing design refinements.
- After final simulations are complete, a system breadboard is built with ICs, and tested in a live environment.
- After additional adjustments and enhancements, the breadboard evolves into a preproduction prototype.

Within the typical design cycle, places appear where the utilization of a web-based resource tool could provide a significant time savings. With today's shortened time-to-market requirements, this savings becomes especially crucial. How quickly components can be identified determines delivery date, and ultimately production viability of a design prototype.

Choosing A Web-Based Tool

Instead of searching each manufacturer's site for part numbers, data sheets, and application notes, engineers now have some excellent resources which encompass most of the available information. These online services contain most of the same data, however, they are presented in different ways. Here are some points to consider in choosing your online resource:

- ICs: The best way to organize IC information is by function, with the ability to search the database for part numbers and descriptions. It also is necessary to link other pertinent information with the data sheets, such as application notes and demo boards, that further explain the operation of the parts in question. IC information is quite mature and the data sheets have very similar formats, i.e. part number, description, features, and detailed information such as pinout and operating voltage.
- Board products: Many companies do not use part numbers, instead opting for names or cryptic descriptions. Features and descriptions are usually written by marketing, causing great confusion among engineers as to the method of comparing and contrasting these different products. This confusion is greatest between different companies, but even exists between different products in the same company.
- EDA tools: Many EDA tools on the market are for engineers designing ICs at the lowest level. These engineers are concerned with getting design projects that don't contain FPGAs or deep-submicron designs, to production. EDA companies should have their product offerings split up into industry usage segments such as pc board, FPGA, gate array, and full-custom products. With these segments they should have the part numbers and technical data to judge price versus performance.

Engineers are rapidly accepting web-based EDA resources which include technical reference information, design tools, software, and product samples. These online resources are now poised to save nearly 5% of the designer's time which equates to a nearly $1 billion design cycle.

The Internet offers great promise to reduce design and prototype purchase time. But companies and engineers must be cautious when seeking web resources that cover a broad range of their needs. They can't spend too much design time hoping to find the "promised land."

Contributed by Bobby R. Walker, technology product manager, QuestLink Technology Inc., Austin, Texas. Walker has more than 25 years of experience in the semiconductor and computer industry, and holds numerous electronic patents. For more information, or to check out QuestLink Technology's EE Design Center web-based tool, access www.questlink.com.

UPDATE ON AIRLINE SEAT POWER

In-Flight Power Plummets Under Pressure

This is an update to the article on commercial airline In-Seat Power Supply Systems (ISPSS) that appeared in the Feb. 9 issue of ELECTRONIC DESIGN. That article, entitled "Standards and Specs For In-Seat Power on Aircraft Still In The Clouds," addressed potential changes in the output voltage at passengers' seats, as well as possible modifications to the pending ARINC Specification 628, Part 2 on power-interface connectors.

The Airlines Electronic Engineering Committee's (AEEC) Cabin Equipment Interfaces (CEI) Subcommittee met just days after the article was published to consider changes to the existing proposed specification. The proposal called for 15 V dc at the seat's power port. The port itself had been defined as a Hypertronics Series-D connector.

American Airlines had already opted to install an alternate connector, namely a standard automotive car cigarette lighter receptacle—a proposal which had already been voted down by the AEEC CEI Subcommittee, as well as the Connector Working Group. A paper was presented to the subcommittee, the result of over three months of research and testing. Again, none of the findings were in favor of the car cigarette lighter.

The word was out, prior to the Feb. 12 meeting, that American Airlines was going to not only reopen the matter of the car connector, but that the airline already had arranged to have the car connector included in the ARINC specification—end of discussion.

What was going to be a straightforward meeting about revising the output voltage became what appeared to be a vote-in-principle-only affair. Once the car connector was "approved," it made no sense to set the output voltage higher than 15 V dc, even though that would deliver better power conversion efficiencies. If the in-seat power port looks like a car adapter port, then passengers would reasonably expect there to be a car-compatible voltage at that port.

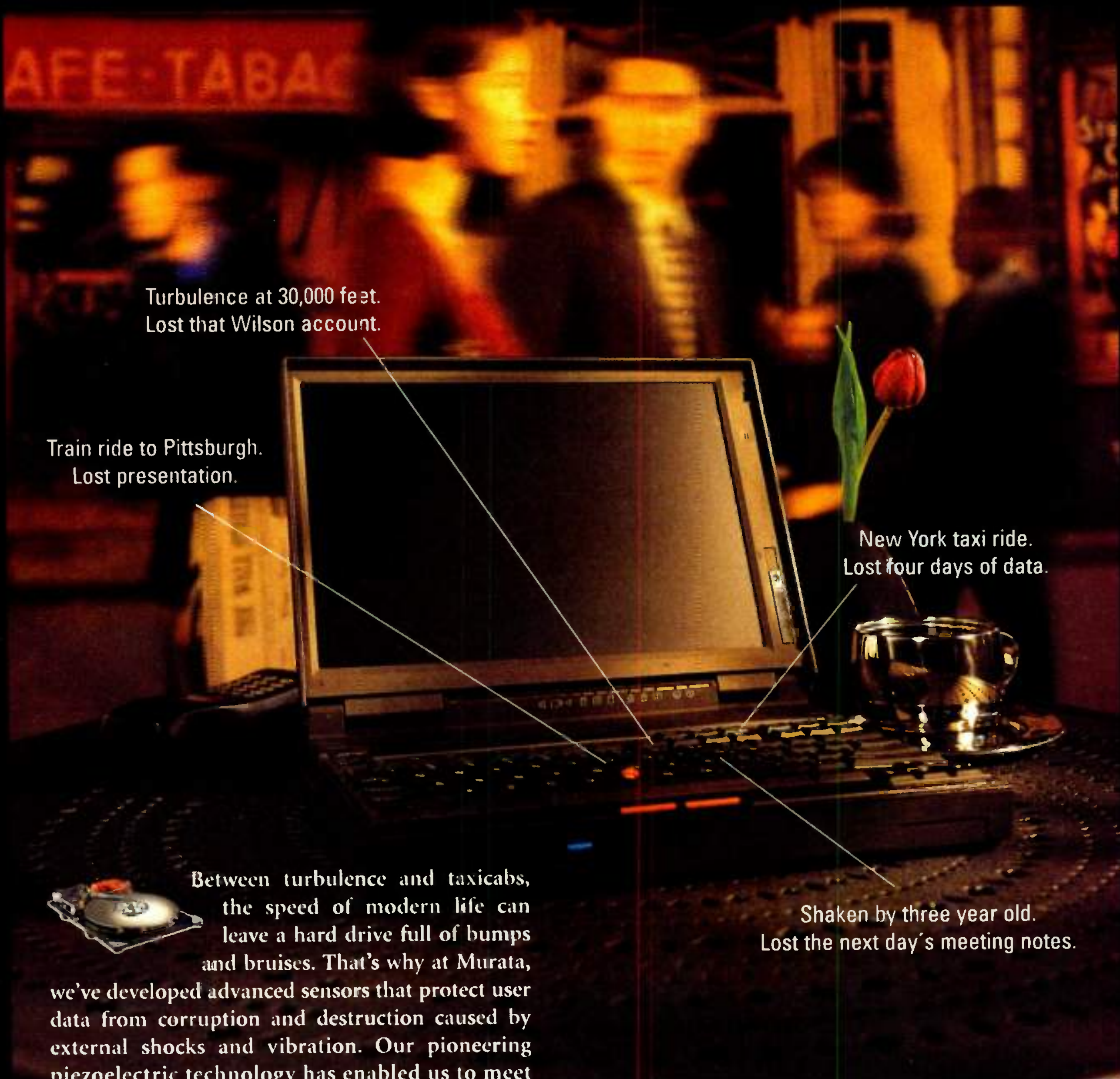
The potential consequences of this "approved" use of the automotive connector may pressure other airlines to opt for the less-expensive car receptacle. If the Hypertronics connector disappears, commercial aviation will lose one of the highly visible differentiators that indicates to passengers that they are on an airplane, and not in a car. Will passengers who can now easily use their car adapter to charge their cellular phones erroneously think that the airlines are somehow condoning the use of that cellphone? Will someone see a cigarette lighter port and reasonably believe that it's okay to light up and smoke?

Perhaps the biggest concern should be that dc-ac inverters are now legitimized. The Federal Aviation Administration (FAA) only has one prohibition about the design of the power interface at the passenger seat—it must not have the appearance of a 110-V ac wall outlet.

As it now stands, ac power will become prevalent on aircraft, through the use of car and RV inverters. ZD-Net, the web site for *PC Magazine*, recently had a travelers' hint: plug an inexpensive dc-ac inverter into the aircraft's automotive receptacle. Then, simply use the laptop-manufacturer-supplied ac-dc converter to power a laptop. Perhaps the airlines should just install ac wall outlets after all, and save passengers the cost and inconvenience of having to purchase and carry around an inverter. The risk of electrocution or fire is just as great with an 800-W inverter as it is from a wall outlet.

The inverter also opens up new risks from battery chargers Any cheap charger plugged into an inverter will charge Ni-Cds, NiMH, L-Ion, and even rechargeable alkalines in shavers, camcorders, toys, and so on. How the airlines weather this inevitable onslaught of "anything goes" battery charging may show that they have already crossed that fine line that separates passenger convenience from safety.

Patrick Potega is the acting director of PEDA (the Passenger Electronic Device Association). The organization's purpose is to represent the interests and needs of the mobile computing community to the commercial aviation industry. He can be contacted at 6320 Canoga Ave., Ste. 1500, Woodland Hills, CA 91367; (818) 887-3123; fax (818) 883-5706; e-mail: peda@mcimail.com.



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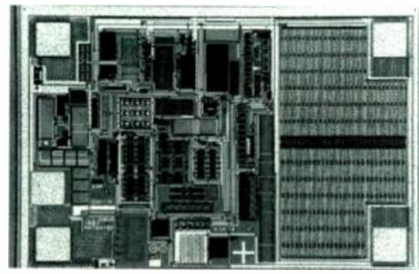
CMOS Low Dropout Voltage Regulator Breaks RF Performance Barrier

Combining innovative circuit design with a tweaked CMOS process, fabless analog/mixed signal design house Impala Linear Corp. has released a novel low-dropout (LDO) voltage regulator with improved RF performance. The ILC7081 is a RF LDO regulator that provides ultra-low quiescent current and low dropout voltage of CMOS with higher ripple rejection and transient response of bipolar and biCMOS LDOs. It comes in a tinier SOT-23 package that requires a small low-cost 0.47-µF ceramic output capacitor, according to Zahid Rahim, director of Impala Linear's power-management product group.

The ILC7081 raises the performance bar for CMOS low-dropout voltage regulators and improves the talk time per gram for battery-operated cellular phones, says Rahim. In a typical cellular phone, wherein several low-dropout voltage regulators are required, the ILC7081 provides an approximately 40% savings in bill of materials over previous solutions, adds Rahim. Thereby, it substantially lowers the weight of the cellular phone to achieve a higher talk time per gram, which is a new metric that measures the performance of the unit.



Typically, the linear ILC7081 is rated to dropout 100 mV at 100 mA with output voltage accuracy of 1%. Also, the ground-pin current is only 100 µA at 100-mA load, while its ripple rejection is 60 dB at 1 MHz and 85 dB at 1 kHz. In addition, the output noise voltage is only 80 µV rms.

The unit's RF performance eliminates the need for post-LDO filtering. Other features include 1-µA shutdown current, excellent line and load transient response, as well as protection against overcurrent and overtemperature conditions.

To achieve this performance, the CMOS RF LDO employs a combination of an error amplifier and transconductance amplifier. In this scheme, the internal circuits, such as the bandgap reference, error amplifier, and transconductance amplifier, are powered from the bootstrapped, regulated output voltage of the regulator. This allows extremely high ripple rejection and line-transient response. Also, the input-to-output isolation is high.

(continued from page 62)

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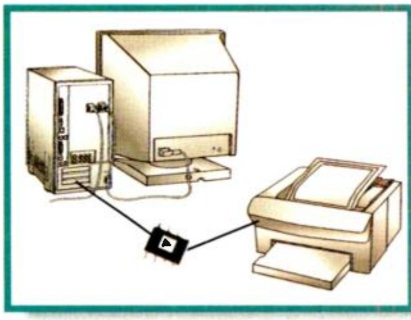

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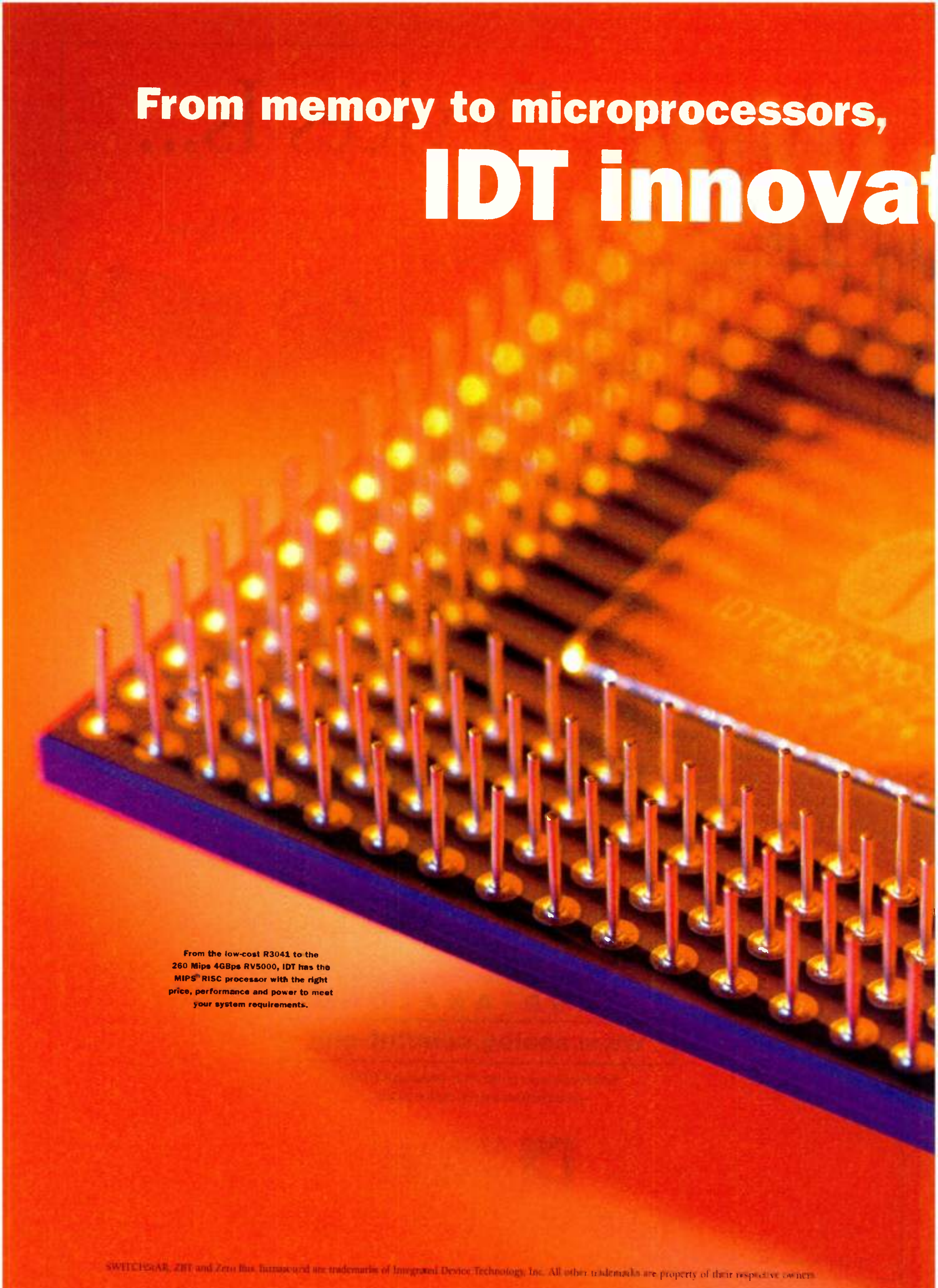

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powering what's next.

There's a digital revolution going on and IDT is powering the products that are changing the way the world communicates. From base stations to set-top boxes to networking systems that enable today's superfast LANs and WANs – you'll find IDT technology in the world's most sophisticated computing, communications and networking products.

That's not surprising with IDT's on-going record of innovations like ZBT™ SRAM optimized for high bandwidth communications. Powerful MIPS® RISC processors that move at speeds never before possible. Communications memories such as FIFOs and Dual Port RAMs. And ALVC Logic with delays less than 3ns. In short, the technology you need for today's most advanced products.

Put these together with IDT's performance-tuned manufacturing capability and our commitment to technical and design support and you'll be able to quickly convert your ideas into market-leading products. To find out more about how IDT can help you power what's next, visit our website or call us today at *1-888-438-3332 ext. 100.*

With delays less than 3ns and an ultra-low power level (0.4mW typical), IDT's ALVC high-performance logic devices are ideal for today's 3.3V system designs.

ZBT SRAM (Zero Bus Turnaround™) is the new standard for high bandwidth communications, offering 100% bus utilization.

SWITCHStAR™ is a highly integrated, 1.24 Gbps switching solution that dramatically reduces the cost of network switching.

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IDT™

READER SERVICE 117

PRODUCT FEATURE

(continued from page 58)

Available in a 5-pin SOT-23, the ILC7081 is pin-compatible with National Semiconductor's LP2981 and Micrel's MIC5205. This pin compatibility with existing standard parts is intended in order to gain easy upgradability.

Maximum input voltage for the low-dropout regulator is 12 V. The fixed output voltage can be either 3.0, 3.3, 3.6, or 5.0 V. Adjustable output voltage is optional. In 1000-piece quantities, the linear ILC7081 is priced at $0.92.

Impala Linear Corp.
628 East Evelyn Ave.
Sunnyvale, CA 94086
Susan Taguinod, (408) 730-3778
www.impalalinear.com
CIRCLE 560
ASHOK BINDRA

Mini AC-DC Power Supply Erases Cross-Regulation Effects Down To No Load

Many switching power supplies depend on proportional system loading to deliver their specified regulation. This is fine so long as you know that your loads will behave. In telecommunications applications, however, loads vary constantly, and that pulls the supply's regulation out of spec.

To alleviate this problem, the NLP65 Telco 65-W, open-frame, switching power supply provides individual regulation on each of its outputs to eliminate cross-regulation effects down to no load situations. The supply is the first product introduction from the recently announced merger of Computer Products Inc., Boca Raton, Fla., and Zytec Corp., Minneapolis, Minn., under the new name of Artesyn Technologies, Eden Prairie, Minn.

Measuring 5 by 3 by 1.25 in., the supply complies with existing emission and immunity standards of the EMC directive, including EN55022/11 and FCC part 15 level B standards for conduction noise. The supply also comes with UL and CSA approvals and is CE marked for the Low Voltage Directive.

Available in dual- or triple-output versions, the supply has a regulation of ±2.0% on the main output, and ±5% on the auxiliaries. Other features include a rise time of 1.0 second (maximum), and a temperature coefficient of ±0.02%/°C, as well as overvoltage and short-circuit protection.

The transient response at the main output, with a 25% step at 0.1 A/µs, is specified as 5.0%, or 250-mV maximum deviation for 1 ms (max), with a recovery up to 1%. The supply operates over the temperature range of 0° to 70°C and has an efficiency of 70% at 50 W. Pricing is $39 each per 1000.

Artesyn Technologies
7575 Market Place Dr.
Eden Prairie, MN 55344
(612) 941-1100
fax (612) 829-1837
www.artesyn.com
CIRCLE 561
PATRICK MANNION

PRODUCT FEATURE

Monochrome CMOS Imaging Sensor Simplifies Design Of Imaging Solutions

Well aware of the futility and risk of reinventing the wheel, designers of imaging solutions are quick to take advantage of ready-to-go devices that remove the need for experience in imaging technology. To them, the recent advances in CMOS imaging technology has been a boon. Devices incorporating this technology have made possible high-performance, cost-effective cameras with enhanced image quality. The most recent introduction comes in the form of the VV5404 developed by VLSI Vision, Edinburgh, Scotland.

The VV5404 is a 356- by 292-pixel monochrome CMOS image sensor that's offered as a single-chip solution for imaging applications. Operating off a 5-V supply, the sensor comes with on-board analog-to-digital conversion, and features 8-bit output and fully automatic setup with built-in automatic black-level calibration. The exposure and gain settings are programmable and operation is controlled via a serial interface. The frame rate is up to 30 frames/s over a 4-wire digital video bus.

Other features include a pixel size of 12.0 µm by 11.0 µm, a sensitivity of 0.5 lux at 30 frames/s, a signal-to-noise ratio of 52 dB, and an operating temperature range of –20° to 70°C. Pricing for a complete development system, including PC software, a capture and control card, a lens, and support circuitry, is $450.

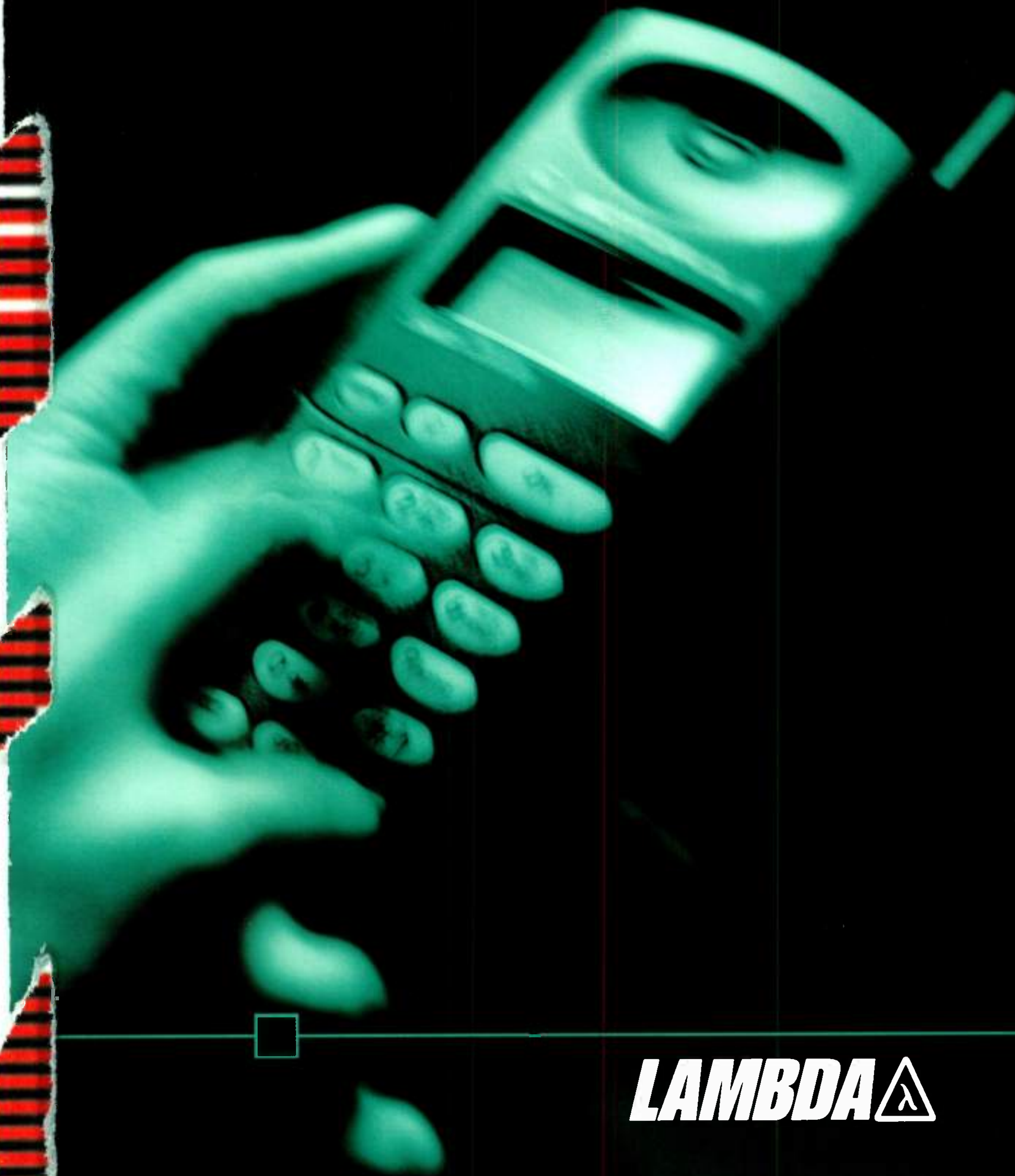
VLSI Vision Ltd.
Aviation House
31 Pinkhill
Edinburgh
Scotland EH12 7BF
44-(0) 131 539 7111
44-(0) 131 539 7141
www.vvl.co.uk
CIRCLE 562
PATRICK MANNION

242-Pin Connector Is Slot-1 Compatible

The Metrec 1.0-mm pitch connecto accommodates up to 242 pins and featrues Slot 1 compatibility. The Slot 1 compatibility allows the use of standard pc-board manufacturing tolerances—despite the tighter pitch—thereby keeping production costs low.

The connector uses beryllium-copper contacts, a thermoplastic housing, and has molded-in keys to preven mismating. Metal retention forkloc help retain the connector to the mot erboard during soldering. The conne tor also supports Intel's S.E.C. ca tridge technology for the Pentium processor, which incorporates a du independent bus architecture. Prici for 0.100-in. tail-length version $3059 per 1000 in quantities of 10,0 delivery is four to six weeks. PM

Molex Inc., 2222 Wellington Court, Lisle, IL 60532; Jim McGrath, (800) 78-MOLEX; fax (630) 969-1352. CIRCLE 56



Lambda has complete telecom power solutions that maximize system density and minimize downtime.

Wireless Cellular

Pole mounted pico and micro cell basestations covering 10 square miles and 1-2 square mile area, respectively, demand scaleable low power DC-DC converters to power internal circuitry. Front end power of 500 to 2000 watts provides either a 24 or a 48 volt bus voltage used to power amplifier circuitry, or is stepped down at the card level using DC-DC converters. Most systems use scaleable architectures to properly size the power capability with the application and allow the user to quickly increase power as the system demand increases.

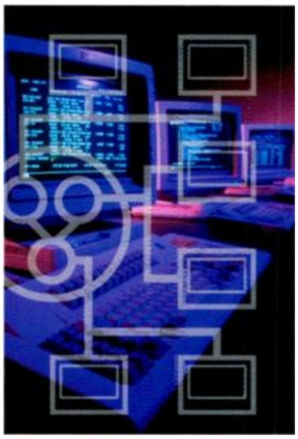
Paging

As the paging market extends its technology, offering high speed messaging and narrow band (PCS/2 way messaging), the paging industry will require high speed networks. Powering these networks are front end AC power systems up to 6000 watts at either 24 or 28 volt outputs. Specific features include current sharing at the card level, level B EMI performance (conducted and radiated) and AC and DC good signals.

	Wireless Cellular	Paging
PM Series	■	■
SM Series	■	■
FE Series	■	■
PA Series	■	
RM Series	■	
PP Series	■	■
WLR2800 Series	■	
SWT/ZWS/VSB Series	■	
PFD Series	■	
Value Added Solutions	■	■

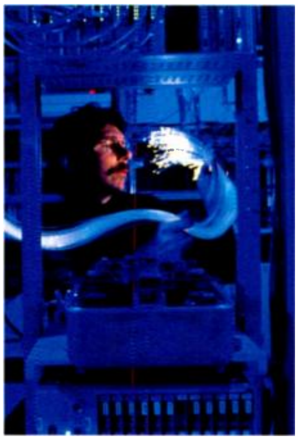
PBX Systems

Applications are moving more and more towards distributed power architectures where both in-shelf and point-of-load power is common. Large business PBX installations use central power plants consisting of AC-DC rectifiers and batteries feeding power to a DC-operated PBX system. Average system power is typically 500 watts using DC-DC converters at power levels from 30-100 watts.



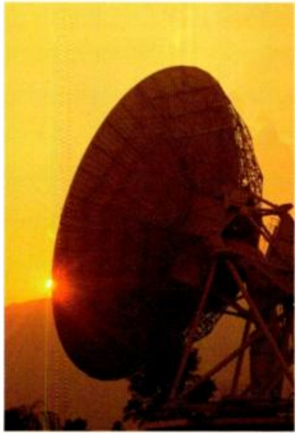
LAN/WAN

Most systems utilize low cost, low power AC-DC platforms from 30 to 250 watts with multiple outputs at 3.3 to 24 volts. The future trend is moving towards distributed power architecture to support the flexibility of scaleable systems for platforms higher than 300 watts. Most applications are extremely cost sensitive and are typically not as feature rich as other telecom applications. Open frame switchers and custom power supplies may be used as low cost solutions in volume applications.



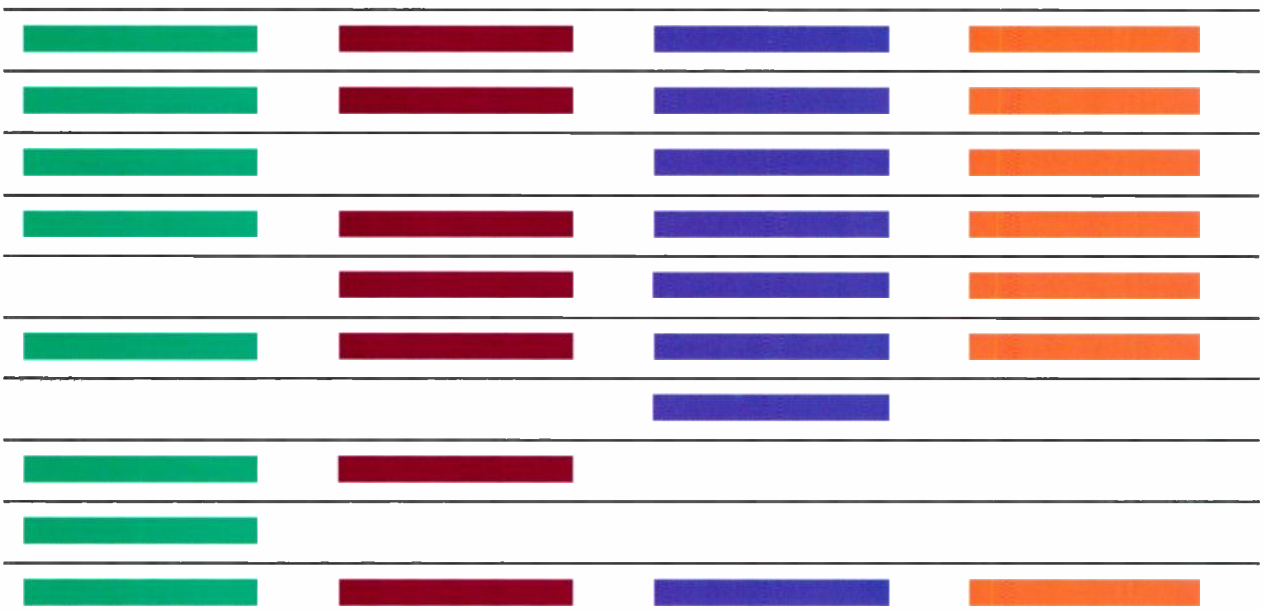
Broadband Distribution

Central office switching equipment is powered by traditional front end battery plants converting AC to a 48 volt bus for distribution in the system. Secondary step down conversion is typically accomplished using both distributed power architectures with redundancy, and current sharing designed in at the card level. Typical systems are required to meet stringent ETSI and Bellcore specifications such as those for seismic shock levels. Surface mount converters are becoming more desirable at the card level.



Remote Electronics

This fast-moving sector incorporates many new technologies such as “fiber in the loop”. The requirements of these applications mimic those of central offices using AC-DC rectification with battery backup. Typical power requirements include DC-DC conversion up to 40 watts and higher, operating off either a 24 or 48 volt bus. This market requires feature rich power systems including over temperature warning, DC output good, AC good, hot pluggability and low profile.



PM Series

The PM Series DC-DC Converters are available in single, dual and triple outputs with 12V, 24V, and 48V inputs and are ideal for distributed power applications. All modules conform to industry standard pin-outs allowing for direct replacement in existing systems. This series is designed specifically for telecommunication applications meeting all of the safety agency requirements including Bellcore and ETSI.

Broad product range (96 models in 5W, 10W, 15W, 20W, and 30W packages)

Industry standard footprints/ pinouts

Wide input range 2:1

Telecom compliant (Bellcore and ETSI)

Worldwide safety agency approvals (UL, CSA, VDE, CE mark)

SM Series

The new SM Series is the first family of surface mount DC-DC converters that are designed specifically for card level distributed power applications targeted at telecom and computer markets.

Using 100% SMT technology in combination with our patented thermal management strategy, the SM Series offers a non-encapsulated solution reducing the weight restrictions required for pick and place operation with existing vacuum end effectors.

First complete line of surface mountable DC-DC converters with low profile (0.4")

Hot plugable with a 10m sec start-up time

Broad product offering from 5W-30W in 56 different models

Short lead time (< 4 weeks)

Worldwide safety agency approvals, (UL, CSA, CE mark)

FE Series

The FE Series power modules and racking systems are the ideal foundation for fault tolerant distributed power architectures. Designed specifically for telecommunications, the FE Series is available in 24 or 48 VDC output modules, providing from 500W to 6000W of scaleable power. Lambda's FE Series power modules and racking systems are hot plugable, N+1 redundant, and make designing, building and qualifying your system easier, quicker and much less expensive.

Wide range input and power factor correction

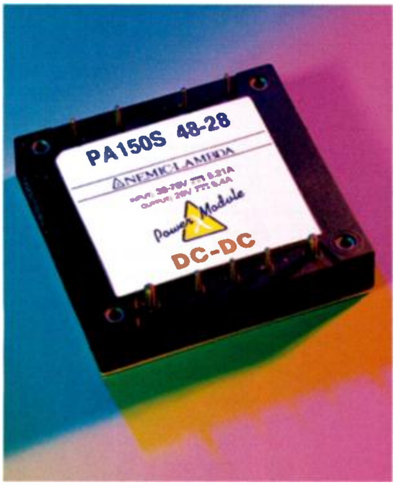
Modular and scaleable

Hot plug and N+1 redundancy

Active current sharing

Worldwide telecom and safety approvals (UL, CSA, TUV, CE mark and Bellcore NEBS and ETSI compliant)

PA Series



The "Half Brick" PA Series single output DC-DC converters are available with 48V inputs, and are ideal for distributed power applications. All modules conform to industry standard pin-outs allowing for ease of intergration in existing systems. This series is particiularly well suited for 48V input central office applications, and meets all of the safety agency approvals and telecom standards requirements.

Industry standard footprints (2.28" x 2.4" x .5") and pinouts

Wide input range 2:1

Remote sense

Remote on/off

High efficiency

Worldwide safety agency approvals (UL, CSA, VDE, CE mark)

PFD Series

The PFD Series is a DC-DC power supply designed to provide 750W or 1000W in multiple output configurations. They provide the industry's widest operating input range (36-75 VDC) ensuring worldwide operation through worst case input power sags and surges.

The PFD Series is designed with standard features such as current sharing, fan fail detection and input/output signals.

Wide range DC input: 36-75 VDC

Complete ETSI and Bellcore compliance

Meets worldwide telecom EMI requirements

High powered 3.3V and 5V outputs in 750 or 1000W packages

Available with system interface signals and current sharing

Worldwide safety agency approvals, (UL, CSA, VDE, CE mark)

RM Series

The RM Series low profile converters offer the highest efficiencies available on the market and do not require a heatsink. This makes the RM ideal for telecommunications applications such as broad band distribution, ATM exchanges, LANs, multimedia systems and other applications where high efficiency and low profiles are critical. The features included in the RM Series allow for hot plug, EMI filtering, diagnostics and control, making the RM Series ideally suited for the highest performance systems.

Wide range DC input: 36–75 VDC

90% efficiency at 5V

Low profile (8mm in height)

Internal EMI filtering

-40°C to +85°C operating temperature range

Worldwide safety agency approvals (UL, CSA, VDE, CE mark)

PP Series

The PP Series is a low cost DC-DC converter designed for low power (1.5W to 6W) and low profile applications. They have industry standard pinouts a height of only 8mm and are available in single and dual outputs with 5,12, 15, 24 and 48 volt inputs.

Low profile (8mm in height)

Wide input range

Industry standard footprints

Available in single and dual outputs

WLR2800 Series

The WLR2800 rectifier provides a high-density, cost-effective power factor corrected front end solution for distributed power and bulk power applications. The WLR2800 features comprehensive protection, alarm facilities, and is available with a range of different options, including hot swap and N+1 redundancy. It operates from a single-phase supply and is available with 24V or 48V nominal outputs.

Power factor correction

Hot swap and N+1 redundant capability

Integral diagnostics and front panel monitoring

Worldwide safety approvals (UL, CSA, TUV, CE mark and BABT)

SWT, ZWS, VSB Series

Lambda's SWT, ZWS and VSB Series are ideally suited for use in telecommunication applications, computers, peripherals, factory, office automation and other high volume applications requiring low cost single and multiple output power supplies.

All models meet radiated and conducted EMI to Curve B, for unparalleled global performance in a cost effective package with OEM-type input and output connectors.

Universal AC input (85–265 VAC)

Broadest product line with over 100 models in single and multiple outputs

Designed for low cost, high volume production needs

Worldwide safety agency approvals, (UL, CSA, VDE, CE mark), power factor correction and global EMI compliance

Value Added solutions

If your needs aren't met by one of our standard products, Lambda's Value Added & Custom Products Group can design your solution. With our broad line of low profile DC-DC converters, Lambda can quickly create a power card to your exact specification. These plug and play cards are designed with AC and/or DC input and are available with the industry's lowest card pitch. To speak with an Engineer about your application, call us at 1-800-851-5121.

Responsive tech support

In-house safety agency certification

Testing for low voltage and EMC directives for CE marking

Prototypes in less than two weeks

Complete custom designs in 12 weeks or less

Telecom power solutions selector guide

DC-DC Converters

Input	Power (W)	# of Outputs	Output, VDC	Dimensions (in)	Remote On/Off	10ms Start Up Time	Industry Standard Footprint	Output Adjustment	OVP	OCP	Short Circuit Protection
SM Series											
24 VDC	5	S, D	3.3, 5, ±12, ±15	.395 x 1.4 x 1.43	●	●		●	●	●	●
24 VDC	10	S, D	3.3, 5, ±12, ±15	.395 x 1.4 x 1.43	●	●		●	●	●	●
24 VDC	20	S, D	3.3, 5, ±12, ±15	.395 x 1.8 x 1.8	●	●		●	●	●	●
24 VDC	30	S, D, T	3.3, 5, ±12, ±15	.395 x 2.5 x 2.5	●	●		●	●	●	●
48 VDC	5	S, D	3.3, 5, ±12, ±15	.395 x 1.4 x 1.43	●	●		●	●	●	●
48 VDC	10	S, D	3.3, 5, ±12, ±15	.395 x 1.4 x 1.43	●	●		●	●	●	●
48 VDC	20	S, D	3.3, 5, ±12, ±15	.395 x 1.8 x 1.8	●	●		●	●	●	●
48 VDC	30	S, D, T	3.3, 5, ±12, ±15	.395 x 2.5 x 2.5	●	●		●	●	●	●
PM Series											
12 VDC	5	S, D	3.3, 5, ±12, ±15	1.0 x 2.0 x 0.335			●		●	●	●
12 VDC	10	S, D	3.3, 5, ±12, ±15	1.0 x 2.0 x 0.335			●		●	●	●
12 VDC	15	S, D	3.3, 5, ±12, ±15	1.6 x 2.0 x 0.335	●		●	●	●	●	●
12 VDC	20	S, D	3.3, 5, ±12, ±15	1.6 x 2.0 x 0.335	●		●	●	●	●	●
12 VDC	30	S, D, T	3.3, 5, ±12, ±15	2.5 x 3.0 x 0.335	●		●	●	●	●	●
24 VDC	5	S, D	3.3, 5, ±12, ±15	1.0 x 2.0 x 0.335			●		●	●	●
24 VDC	10	S, D	3.3, 5, ±12, ±15	1.0 x 2.0 x 0.335			●		●	●	●
24 VDC	15	S, D	3.3, 5, ±12, ±15	1.6 x 2.0 x 0.335	●		●	●	●	●	●
24 VDC	20	S, D	3.3, 5, ±12, ±15	1.6 x 2.0 x 0.335	●		●	●	●	●	●
24 VDC	30	S, D, T	3.3, 5, ±12, ±15	2.5 x 3.0 x 0.335	●		●	●	●	●	●
48 VDC	5	S, D	3.3, 5, ±12, ±15	1.0 x 2.0 x 0.335			●		●	●	●
48 VDC	10	S, D	3.3, 5, ±12, ±15	1.0 x 2.0 x 0.335			●		●	●	●
48 VDC	15	S, D	3.3, 5, ±12, ±15	1.6 x 2.0 x 0.335	●		●	●	●	●	●
48 VDC	20	S, D	3.3, 5, ±12, ±15	1.6 x 2.0 x 0.335	●		●	●	●	●	●
48 VDC	30	S, D, T	3.3, 5, ±12, ±15	2.5 x 3.0 x 0.335	●		●	●	●	●	●
RM Series											
48 VDC	30	S	2, 3.3, 5	2.36 x 0.315 x 2.56	●			●	●	●	●
48 VDC	50	S	2, 3.3, 5	2.36 x 0.315 x 3.86	●			●	●	●	●
48 VDC	100	S	2, 3.3, 5	2.36 x 0.315 x 4.57	●			●	●	●	●
PP Series											
5 VDC	1.5	S, D	5, ±12, ±15	1.29 x 0.31 x 0.81			●			●	
5 VDC	3	S, D	5, ±12, ±15	1.84 x 0.31 x 1.09			●			●	
5 VDC	6	S, D	5, ±12, ±15	1.84 x 0.31 x 1.65			●			●	
5 VDC	10	S, D	5, ±12, ±15	1.84 x 0.31 x 1.65			●			●	
12 VDC	1.5	S, D	5, ±12, ±15	1.29 x 0.31 x 0.81			●			●	
12 VDC	3	S, D	5, ±12, ±15	1.84 x 0.31 x 1.09			●			●	
12 VDC	6	S, D	5, ±12, ±15	1.84 x 0.31 x 1.65			●			●	
24 VDC	1.5	S, D	5, ±12, ±15	1.29 x 0.31 x 0.81			●			●	
24 VDC	3	S, D	5, ±12, ±15	1.84 x 0.31 x 1.09			●			●	
24 VDC	6	S, D	5, ±12, ±15	1.84 x 0.31 x 1.65			●			●	
48 VDC	1.5	S, D	5, ±12, ±15	1.29 x 0.31 x 0.81			●			●	
48 VDC	3	S, D	5, ±12, ±15	1.84 x 0.31 x 1.09			●			●	
48 VDC	6	S, D	5, ±12, ±15	1.84 x 0.31 x 1.65			●			●	
PFD Series											
36-75 VDC	750	Q,P	3.3, 5, 12, 24, 48	2.65 x 8 x 12	●				●	●	●
36-75 VDC	1000	Q,P	3.3, 5, 12, 24, 48	2.65 x 8 x 12	●				●	●	●

Rectifier/Front End

Amps	Output, VDC	No of Outputs	Input	Dimensions	Remote On/Off	Remote Sense	AC/DC Good	Current Share	PFC	Overtemperature	Output Adjustment	OCP	OVP	LED Status Indicators	Alarm Status	Hot Plug Capability	N+1 Capability	Cond EMI, Level B	Auxiliary Bias Supply	Racking System Available	Low Voltage Disconnect
FE Series																					
11	48	S	85 - 265 VAC	11.97 x 4.87 x 2.00	●	●	●	●	●	●	●	●	●	●	●	●	●	✚	●	●	●
21	48	S	85 - 265 VAC	11.97 x 4.87 x 3.30	●	●	●	●	●	●	●	●	●	●	●	●	●	✚	●	●	●
32	48	S	85 - 265 VAC	11.97 x 4.87 x 5.55	●	●	●	●	●	●	●	●	●	●	●	●	●	✚	●	●	●
42	48	S	170 - 265 VAC	11.97 x 4.87 x 5.55	●	●	●	●	●	●	●	●	●	●	●	●	●	✚	●	●	●
21	24	S	85 - 265 VAC	11.97 x 4.87 x 2.00	●	●	●	●	●	●	●	●	●	●	●	●	●	✚	●	●	●
42	24	S	85 - 265 VAC	11.97 x 4.87 x 3.30	●	●	●	●	●	●	●	●	●	●	●	●	●	✚	●	●	●
63	24	S	85 - 265 VAC	11.97 x 4.87 x 5.55	●	●	●	●	●	●	●	●	●	●	●	●	●	✚	●	●	●
84	24	S	170 - 265 VAC	11.97 x 4.87 x 5.55	●	●	●	●	●	●	●	●	●	●	●	●	●	✚	●	●	●
WLR2800 Series																					
58	48	S	176 - 264 VAC	5.00 x 8.00 x 13.00	✱	●	●	✱	●	●	✱	●	●	●	●	●	●	●			
116	24	S	176 - 264 VAC	5.00 x 8.00 x 13.00	✱	●	●	✱	●	●	✱	●	●	●	●	●	●	●			
PD800 Series																					
10	48	S	100 - 240 VAC	8.66 x 3.74 x 1.08	●		DC		●		●	●	●	●	●	●	●	●	●		
16	48	S	200 - 240 VAC	8.66 x 3.74 x 1.08	●		DC		●		●	●	●	●	●	●	●	●	●		

Rack Total Amps	Output VDC	Max No Modules	Input	Dimensions	Hot Plug Capability	N+1 Capability	Conducted EMI Level B	Low Voltage Disconnect	Input Circuit Breakers
FE Series Racking System									
11 - 88	24	8	85 - 265 VAC	16.0 x 5.25 x 17.75	●	●	✚	✱	✚
21 - 105	24	5	85 - 265 VAC	16.0 x 5.25 x 17.75	●	●	✚	✱	✚
32 - 96	24	3	85 - 265 VAC	16.0 x 5.25 x 17.75	●	●	✚	✱	✚
42 - 126	24	3	170 - 265 VAC	16.0 x 5.25 x 17.75	●	●	✚	✱	✚
21 - 168	48	8	85 - 265 VAC	16.0 x 5.25 x 17.75	●	●	✚	✱	✚
42 - 210	48	5	85 - 265 VAC	16.0 x 5.25 x 17.75	●	●	✚	✱	✚
63 - 189	48	3	85 - 265 VAC	16.0 x 5.25 x 17.75	●	●	✚	✱	✚
84 - 252	48	3	170 - 265 VAC	16.0 x 5.25 x 17.75	●	●	✚	✱	✚

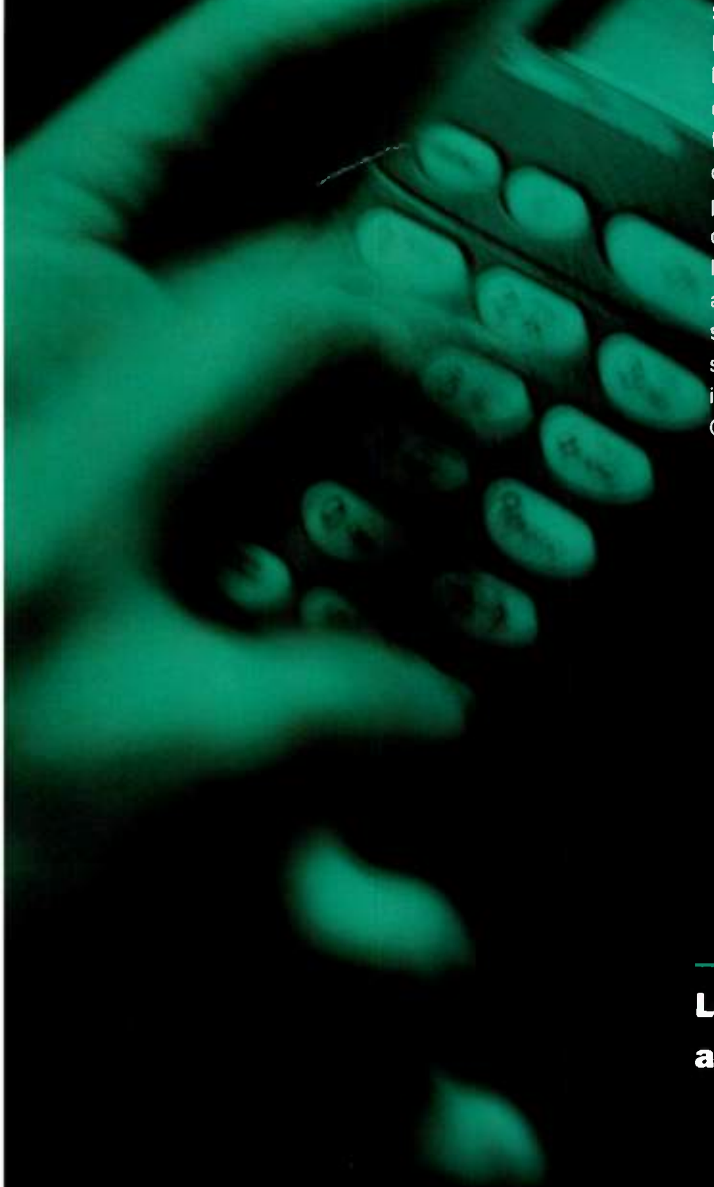
✱ Optional ✚ Available with "N" and "L" version racking systems.

AC-DC Power Supplies

Power (W)	No of Outputs	Input	Output, VDC	Dimensions	PFC	EMI, Curve B
SWT Series						
30	T	86-265 VAC	±5, ±12, ±15	1.2 x 5 x 3		●
40	T	86-265 VAC	±5, ±12, ±15	1.4 x 5 x 3		●
65	T	86-265 VAC, Auto	±5, ±12, ±15	1.77 x 6 x 3.5		●
100	T	86-265 VAC	±5, ±12, ±15	1.77 x 7.75 x 4.25		●
VSB Series						
10	S	85-132 VAC	3.3, 5, 12, 15, 24, 36, 48	.67 x 3.86 x 1.77		●
15	S	85-132 VAC	3.3, 5, 12, 15, 24, 36, 48	.67 x 4.53 x 1.97		●
30	S	85-132 VAC	3.3, 5, 12, 15, 24, 36, 48	.98 x 5.22 x 1.97		●
50	S	85-132 VAC	3.3, 5, 12, 15, 24, 36, 48	.98 x 7.68 x 1.97		●
75	S	85-132 VAC	3.3, 5, 12, 15, 24, 36, 48	1.26 x 8.76 x 1.97		●
100	S	85-132 VAC	3.3, 5, 12, 15, 24, 36, 48	1.26 x 8.76 x 2.44		●
150	S	85-132 VAC	3.3, 5, 12, 15, 24, 36, 48	1.42 x 8.76 x 2.95		●
ZWS Series						
5	S	86-265 VAC	3.3, 5, 12, 15, 24, 36, 48	.83 x 3.86 x 1.77		●
10	S	86-265 VAC	3.3, 5, 12, 15, 24, 36, 48	.83 x 4.13 x 1.97		●
15	S	86-265 VAC	3.3, 5, 12, 15, 24, 36, 48	.83 x 4.92 x 1.97		●
30	S	86-265 VAC	3.3, 5, 12, 15, 24, 36, 48	1.02 x 5.24 x 2.17		●
50	S	86-265 VAC	3.3, 5, 12, 15, 24, 36, 48	1.02 x 7.68 x 2.17		●
75	S	85-265 VAC, Auto	3.3, 5, 12, 15, 24, 36, 48	1.38 x 8.74 x 2.17	●	●
100	S	85-265 VAC, Auto	3.3, 5, 12, 15, 24, 36, 48	1.38 x 8.74 x 2.44	●	●
150	S	85-265 VAC, Auto	3.3, 5, 12, 15, 24, 36, 48	1.58 x 8.74 x 2.95	●	●

Reliability: A Lambda hallmark.

Throughout the industry, Lambda has built a reputation for products that perform where conditions are harsh and failure is unthinkable. This unsurpassed reliability is built into every product we make, and all the processes under which we make them.



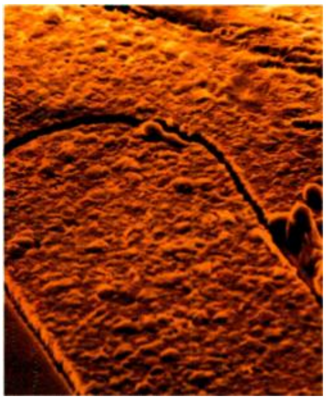
Shock & Vibration
Rough roads and poor handling during transport could cause potential damage to a product even before it is out of the box. Lambda prevents potential failures by designing to IEC-68 guidelines. In addition, our power supplies are designed to meet the stringent criteria for seismic shock and vibration as outlined in Bellcore specifications CORE GR0063.

Temperature Cycles
Today's applications dictate extreme temperature variations. Duplicating these conditions within Lambda's environmental chambers allows our engineers to prevent failures during continuous operation in harsh environmental conditions.

Lambda meets every agency approval associated with the telecom industry.

Design Process

Lambda designs high reliability into every product by involving all disciplines in our multi-level design review process in conjunction with our rigid design guidelines. Anticipation of potential failures is determined by Failure Mode Engineering Analysis stressing all components beyond their standard manufactures ratings. In addition, formal process verifications are conducted in both our engineering and manufacturing environments, ensuring compatibility between new designs and manufacturing processes.



Component Approval Process

The quality of our products starts from the very beginning. Careful consideration is given before Lambda selects its vendors as they must pass our rigorous qualification process. When selecting components, our engineers are mandated to design well within the manufactures guidelines. In addition, manufacturing shortages are prevented since we multi source components with 2 or more vendors.

Line Input Disturbances

In the event of a lightning strike, Lambda's power supplies have been designed to meet IEC requirements protecting the end user's equipment from damage. Additional design constraints will ensure continuous operation even during line surges and sags from capacitive & inductive loads.

For more information on Lambda's power supplies for telecommunications, call 1-800-LAMBDA-4 ext. 8734
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ELECTRONIC DESIGN QUICK LOOK

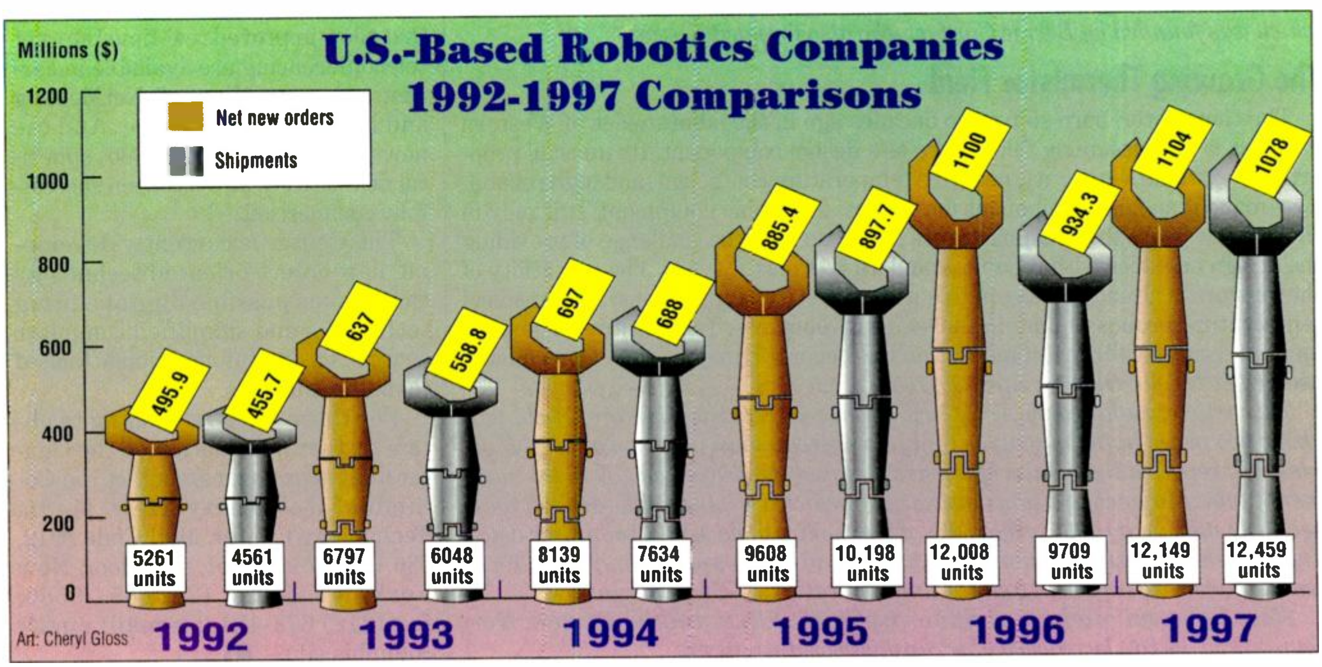
Edited by Mike Sciannamea and Debra Schiff

MARKET FACTS

A Career Year For The Robotics Industry

The North American robotics industry had its best year ever in 1997, according to new statistics recently released by the Robotic Industries Association (RIA). A total of 12,459 robots were shipped last year, leading the market to experience an increase of 28% over 1996. With a value of nearly $1.1 billion, shipment revenue topped the billion-dollar mark for the first time ever. Robot shipments have been on a dramatic upswing for the past five years, rising 172% in units and 136% in dollars since 1992. New orders also topped the billion-dollar mark, as a total of 12,149 robots valued at $1.104 billion were ordered last year. Though new orders rose just 1% in 1997, they are up 131% in units and 122% in dollars in the past five years. Donald A. Vincent, executive vice president of RIA, says, "1997 ended up stronger than we anticipated." He continues, "Shipments continued to soar, and the industry set another record for new orders despite some expectations of a downturn after five straight years of double-digit growth. Material handling applications, such as parts transfer, machine tending, packaging, and palletizing cut across many industries," Vincent explains. "Manufacturers of consumer goods, electronics, food and beverages, and other nonautomotive products are now taking advantage of robots to become stronger global competitors. Small, medium, and large companies in just about every industry are taking a fresh look at robots to see how the powerful technology can help them solve manufacturing challenges," he says. To help companies who are investigating robotics, Vincent says the RIA has produced two new resources. A videotape entitled "A Guide to Robot Solutions" has just been released, along with the "1998 Robotics Industry Directory" that provides detailed information on over 125 leading suppliers of robots and related automation products. The RIA is a trade group organized to specifically serve the field of robotics. Its membership includes over 160 manufacturers, distributors, system integrators, accessory equipment suppliers, major users, research groups, and consulting firms.

For further information, contact the RIA, P.O. Box 3724, Ann Arbor, MI 48106; (734) 994-6088; fax (734) 994-3338; e-mail: ria@robotics.org.—**MS**

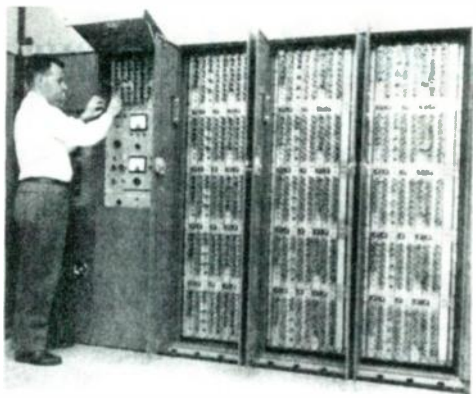


40 YEARS AGO IN ELECTRONIC DESIGN

Computer Link Facilitates Missile Flight Simulation

The effectiveness of digital and analog computers in simulating missile flights has been increased by the development of a multichannel computer link. The Addaverter is essentially a translating device to link the two types of computers and make their languages compatible.

Built for the Space Technology Laboratories, a division of The Ramo-Woodridge Corp., by Epsco Inc., of Boston, Mass., the Addaverter is being used with an Electronic Associates PACE analog computer and a Remington-Rand Univac Scientific Model 1103A digital computer. The Laboratories are responsible for the technical direction and systems engineering for the Air Force's ballistic missile program.



Both computers can now work on the same missile problem, with each one concerning itself with a different phase of the flight. While the digital computer plots the flight around the earth, tracing the trajectory to the eventual point of impact, the analog computer determines the flight oscillations. The Addaverter equipment responds to four distinct commands: write data from the digital computer, present data to the analog computer, sample data from the analog computer, and read data into the digital computer. In converting digital to analog and analog to digital, the Addaverter uses 30 channels. It has more than 2000 vacuum tubes and 1500 semiconductor diodes mounted on eight relay racks. *(ELECTRONIC DESIGN, April 16, 1958, p. 17)*

Epsco was one of the pioneering companies in data converters. In fact, the Boston area was—and still is, for that matter—a hotbed of analog circuitry and data converter designs. Luminaries of the area include such past and present companies as George A. Philbrick Researchers; Analog Devices; and Analogic, which was founded by Bernie Gordon, who also founded Epsco.

The Growing Thermistor Field

The thermistor, born some two decades ago in the laboratories of Western Electric, is now assuming full stature as a design component. Its unusual properties—extreme sensitivity, negative temperature coefficient, and high reliability—make it an ideal component for modern electronic equipment. It is only in the last few years that manufacturers have taken up the challenge of providing the design engineer with reliable, standard thermistor types. The versatility of thermistors is already reflected in a wide variety of applications, from medical temperature probes to missile-fuel sensing elements. Temperature measurement and control for instrumentation has become a major area of thermistor use. *(ELECTRONIC DESIGN, April 30, 1958, p. 12)*

This article, authored by A. J. Gizzi of General Electric, Edmore, Mich., ran about two pages in the magazine (only the introduction is shown above). It essentially reported the results of a market survey conducted by GE in the summer of 1957. Major conclusions included a predicted tripling of the annual market, to $9 million by 1965; when 50% of the applications would be in time delay and inrush surge suppression, 30% in temperature compensation, and 20% in temperature measurement and control applications.—Steve Scrupski

Steve Scrupski is a former Editor-in-Chief of ELECTRONIC DESIGN. Now semiretired, he can be reached at scrupski@worldnet.att.net.

BACK TO SCHOOL

Columbia University's New Media Technology Center is developing innovative multimedia technologies designed to change the nature of communication. Located in New York City, the "Silicon Alley" of the growing new media industry, the Center was founded to create new tools for digital storytelling. These tools can acquire, search, edit, and distribute multimedia information, and develop ease of access to the technology of image, sound, and text.

Columbia University has brought together engineers, journalists, business authorities, and educators from its faculties to accomplish these objectives. In addition, it has reached out to the worlds of education, commerce, and communications for perspective on priorities and needs. Currently, the University is launching pilot projects in public schools, and has established an office at the New York Information Technology Center at 55 Broad Street to offer technical and educational support to new media firms. It also has built partnership links with the city and state.

The Center already has tallied several notable accomplishments, including the development of the MPEG-2 digital video compression standard that allows the transmission of high-quality video and audio over limited bandwidth. Internet protocols developed by Columbia University faculty that allow improved real-time Internet teleconferencing are available in current versions of Microsoft NetMeeting and Netscape Conference. And the new Omnicamera, with a 360° spherical field of view, also has been successfully commercialized.

The Center is currently developing new object-oriented technology that makes possible digital editing techniques and simplified computer searches using information attached to multimedia files.

For those readers wishing to obtain further information on the Center and its programs, contact the Columbia University New Media Technology Center, Mail Code 8912, 530 W. 120th Street, 8th Floor, New York, NY 10027; (212) 854-6580; fax (212) 678-4817; e-mail: rjn2@columbia.edu.—**MS**

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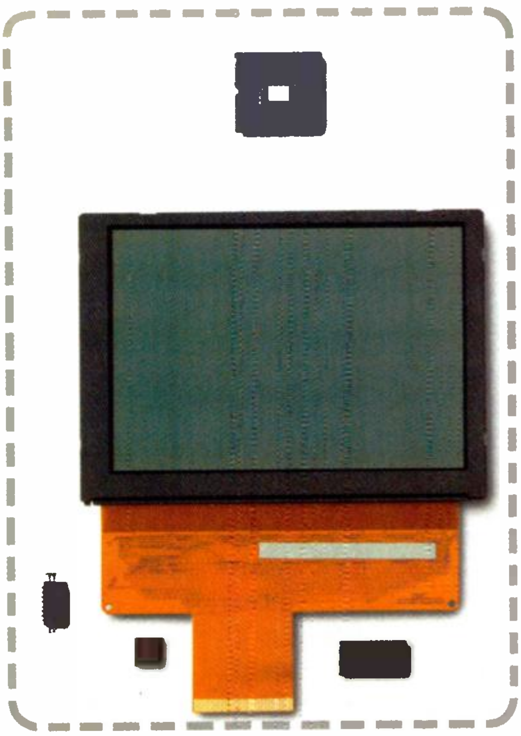

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Flash memory *options include Stacked-Chip Flash, combining two different memory die in one space-saving package, and NextGen™ Boot Block Flash in Sharp's unique Chip-Size Package.*

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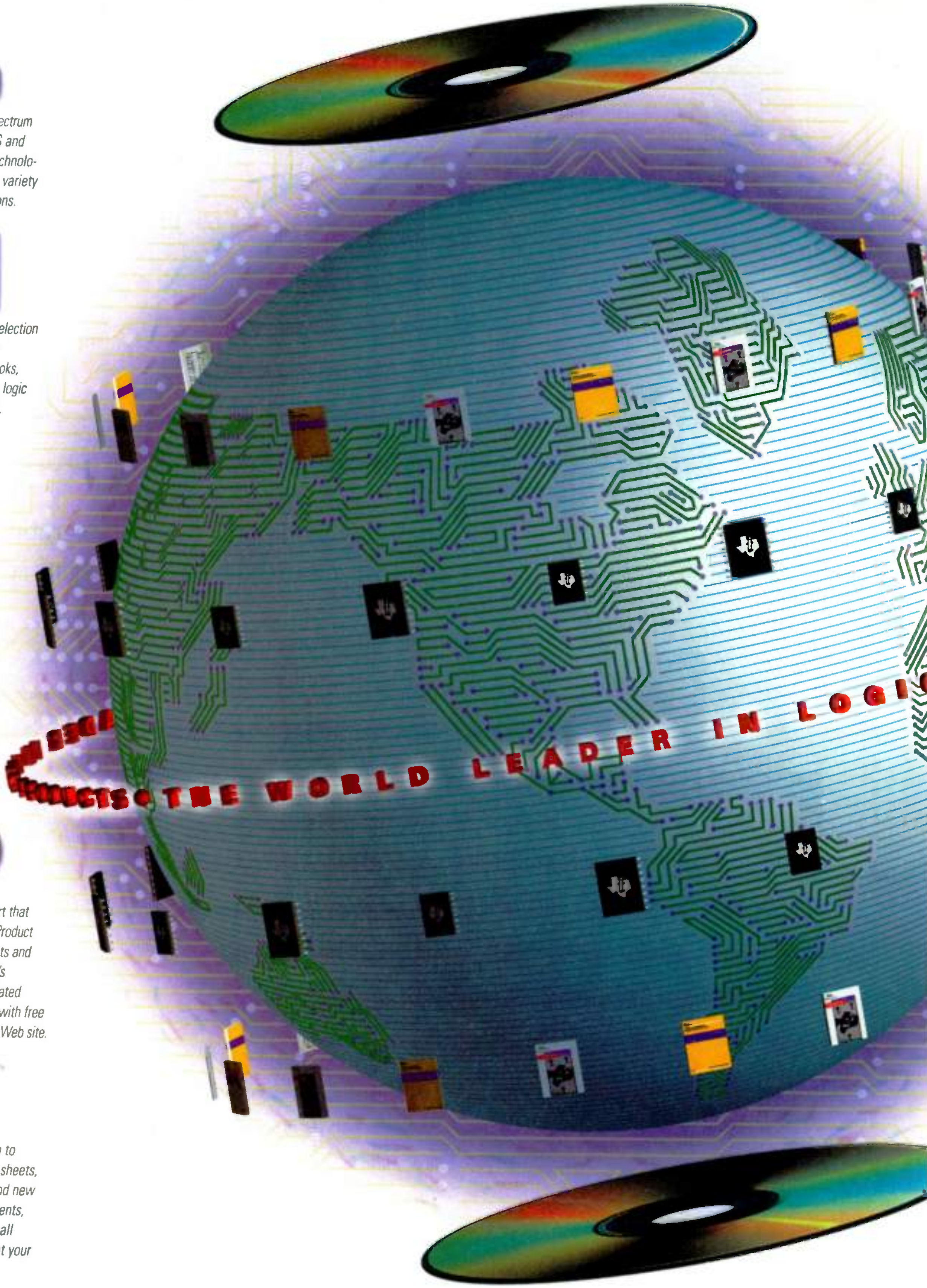

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THE WORLD LEADER IN

MANAGING THE DESIGN FACTORY

Give Me Control

You can probably identify with these comments: "My project is always waiting on parts," "We never have adequate priority," and "We could be successful if we had control of the prototype shop." They're common complaints. Project managers everywhere insist that their destiny is outside of their control because they are held hostage by support groups.

DON REINERTSEN

The psychological consequences of this are damaging. Psychologists say that the less people perceive themselves to be in control of a situation, the less control they will take. Lack of control feeds on itself, and consequently creates a victim mentality—which is the *last* thing that we want on development teams.

We want these teams to take charge of their own destinies. However, let's take some caution with this thinking. Does their perceived lack of control really require giving the team the run of the prototype shop? Surely, a centralized shop would have more resources and be able to be more flexible at supporting project teams. Is decentralizing the prototype resource the only solution?

To crack this problem, we must ask why the team wants to control the prototype shop. If the reason behind it is that their project never has adequate priority, they must control the resource to control its priorities. But why do projects need a high priority anyway? Because without priority you must wait for resources. But why do low priority jobs wait for resources? Quite simply, because we have allowed queues to develop in our process.

The request for control is always a symptom of something larger. The desire to run support groups is almost never based on a true need for control. Usually, it arises because support groups are not being responsive to project teams. For example, why don't teams ever ask to manage their own payroll? Is it because payroll is not important? No, teams don't want to get into dealing with payroll because payroll does what it is supposed to do. If the prototype shop functioned the way it was supposed to function, teams would not be requesting to control it.

Now, at a deeper level, we must ask why the prototype shop is letting the teams down. Does the shop manager have a perverse desire to undermine the company? Not very likely. It is much more probable that the shop is being measured with the wrong metrics. Prototype shops are often assigned to manufacturing and measured on efficiency.

Manufacturing knows how to be efficient. They build a solid backlog, run similar parts at the same time, and minimize expensive overtime. All such approaches lead to efficiency—and poor response time.

A better approach is to find out what users mean by good support. If response time is more important than efficiency, you must align the metrics to encourage response time. Start measuring the prototype shop on how long it spends on the critical path of the project. Then, the prototype shop will start trying to stay off the critical path.

By using that technique, you won't have to hear them boasting about how they've cut the cost of making prototype parts while Engineering moans about how long it takes to get them. Remember, a request for control is usually a sign that someone is not doing their job the way you want them to. It is usually smarter to change the way a support group is measured than it is to take on the responsibility to manage it on a daily basis.

Don Reinertsen is president of Reinertsen & Associates, a consulting firm specializing in product development management. He can be reached at (310) 373-5332 or e-mail: DonReinertsen@compuserve.com.

IT'S ALL IN THE WRIST

Who says that being grounded isn't any fun? Even if part of your job entails handling sensitive components and protecting them from harsh environmental conditions, you still have to smile once in a while, don't you?

The new 4600 series of wrist straps from 3M come in five colors—green, purple, maroon, blue, and lime—to help brighten your day at the shop, as well as protect those sensitive components from particles in the air.

The wrist strap material is a molded insulative thermoplastic. The low-profile plastic is lightweight, and 3M's exclusive "comfort bumps" design on the interior allows for air flow between the band and skin. These features enable workers to wear the bands for long periods with no discomfort. A zipper-type latching mechanism adjusts to any wrist size.

The band also offers exceptional electrical properties. The conductive interior provides effective grounding, dissipating static before it can harm sensitive electronics.The 4600 series ground cords are available with 4-mm, 7-mm, and 10-mm snap fasteners so they can be used worldwide. The cords come in 5- and 10-ft. lengths.

According to 3M, the new colors of the wrist bands are designed to emphasize the importance of the need for proper grounding. And, they also can be used to code different work groups in any given company.

3M's 2200 series wrist bands come in four types: adjustable fabric bands; expandable Speidel metal bands; fixed size (small, medium, large) fabric bands; and disposable bands. Another series, the 2300 dual-conductor fabric band, is designed for use with workstation and wrist-strap monitors.

Contact 3M's Electronic Handling and Protection Division, A130-3N-52, 6801 River Place Rd., Austin, TX 78726-9000; (800) 814-8709; Internet: www.3M.com.—**MS**

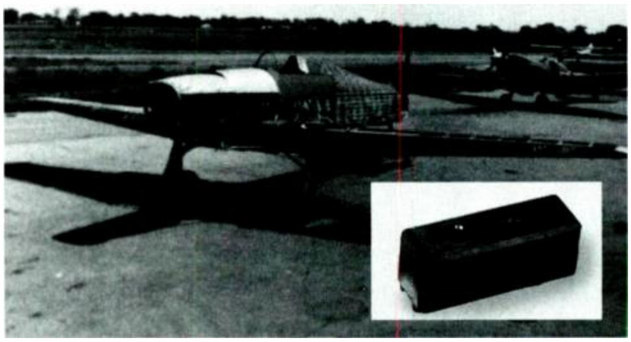
It Takes A Licking And Keeps On Switching

After resting in a swamp for almost 30 years, an old 1940's switch from Honeywell's Micro Switch Division is still functional. The switch was one of the electrical components of a 1942 World War II Hurricane. This particular fighter plane crashed while on coastal patrol in Gander, Newfoundland in December, 1943. Left to rot in the swamp, the Canadian-built plane was not recovered until 1972.

Q.G. Aviation of America Inc. of Fort Collins, Colo. has recently begun restoring and testing the Hurricane for the Lone Star Flight Museum, of Galveston, Texas. The Museum's aircraft are primarily World War II vintage planes, accurately restored to flying condition and flown at air shows throughout the country.

The large switch, positioned on the up-and-down lock indicators of the landing gear, was clearly labeled "MICRO SWITCH BZ-YR3 FREEPORT, ILLINOIS." Scott Stephens of Q.G.contacted Micro Switch and sent them the component, now more than 50 years old.

Not surprisingly the BZ-YR3 is no longer listed in the Micro Switch catalog. The original manufacturing specification, dated September 20, 1940, was still around though—on an old microfiche film.



Micro Switch engineer Steve Severson carefully studied the old switch, documenting visual, X-ray, operational and internal observations. He concluded, "The switch is operational, but does exhibit intermittent dead-break, probably caused by particle contamination." He recommended the BY-3YT as a viable alternative to the obsolete BZ-YR3.

Ralph Royce, Lone Star Flight Museum director, said the Hurricane is a rare breed today—only three left in the world are flying. Royce also noted that during the war, the Hurricane was the "workhorse of the Battle of Britain," despite the press given to the Spitfire.

If all goes well with the restoration process, a fourth Hurricane—with the new Micro Switch BZ switches on board—will soar again in the summer of 1999 at the annual air show in Oshkosh, Wis.

Joseph Desposito

New Sugar-Based Detergents Are Sweet On The Ecosystem

Columbia University, New York, N.Y., via generous grants from the National Science Foundation and 15 corporate partners, is now working on multiple uses for a new class of industrial detergents based on sugar. These new detergents, carrying the moniker of surfactants, were originally developed by chemists in Europe and America, but they're being adapted at Columbia for all kinds of novel uses. The five-year budget for the Industry/University Center for Surfactants at Columbia is $2.3 million.

Surfactants are surface-active compounds such as soaps, that have at least one hydrophobic region and one hydrophilic region. The hydrophobic region binds to insoluble grease or dirt and the hydrophilic region interacts with water. Surfactants work, on a chemical level, by coating the surface of a grease or dirt particle, leaving it to be broken down and washed away.

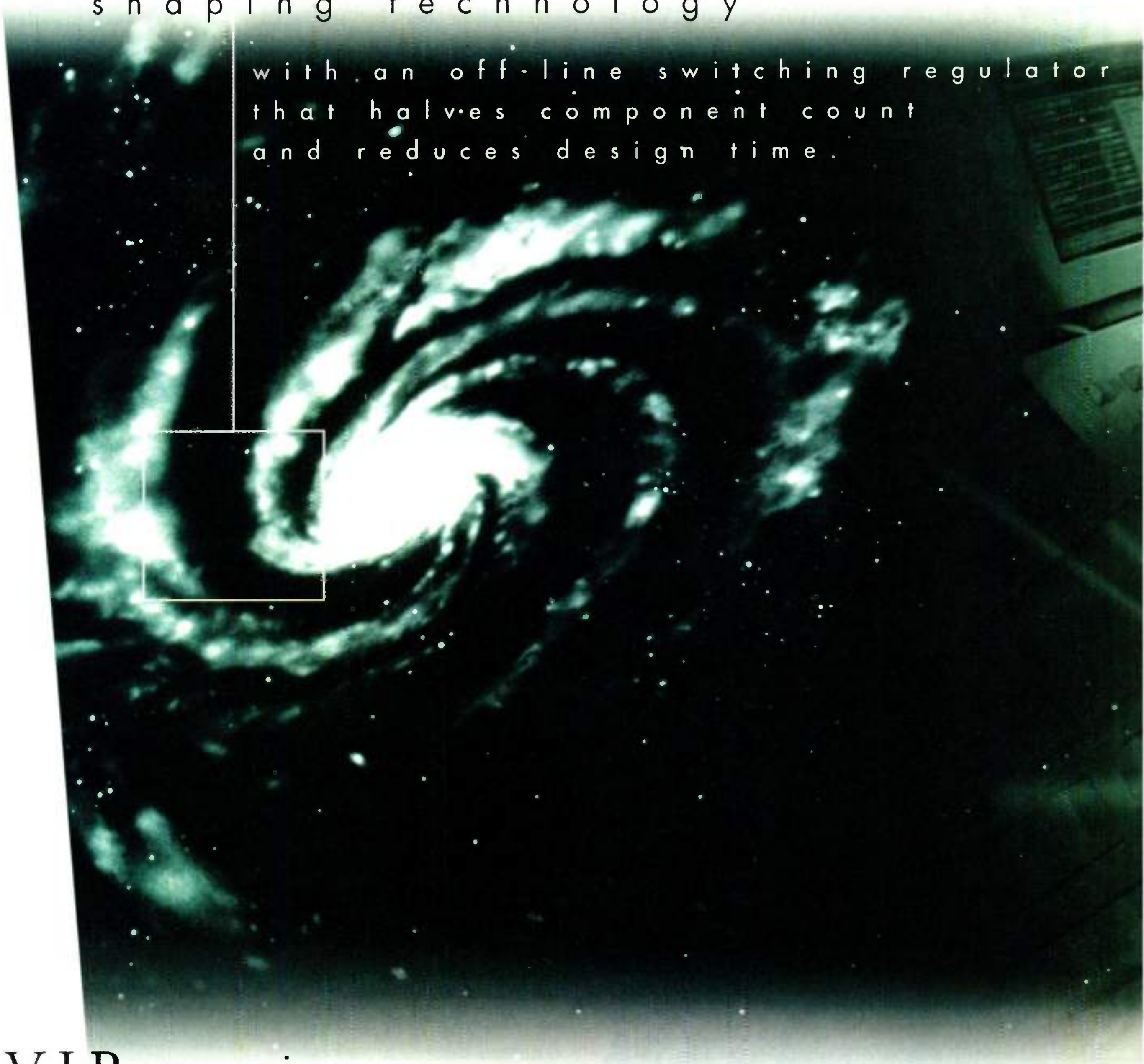
The surfactants also can bind to artificial polymers, holding them in suspension. In this way, they can be used in paints, advanced lubricants, and anticorrosive coating. There's a laundry list of uses for these compounds: advanced ceramics, biotechnology, cosmetics, food processing, fuels, liquid crystals, microelectronics, pharmaceuticals, and photographic films.

The research at Columbia is focused on unique ways of using the sugar-based cleanser from clothes detergents to lubricating titanium implants. The impetus for the research was the search by companies to find detergents that can replace the synthetics that don't degrade or require extra ingredients to soften the water.

In redesigning the way molecules attach, Columbia researchers have created surface-acting polyglucosides. These are short chains of two glucose molecules with attached hydrocarbon side groups. With this architecture, they are very effective grease dissolvers and can clean up soil that's been contaminated by gasoline. Unlike the synthetics, the sugar-based surfactants are mild, can be used in personal-care products, can be easily digested by microbes, are hard-water tolerant, and are completely biodegradable.

Molecular-level studies on the surfactants have been conducted using fluorescence spectroscopy and electron-spin resonance spectroscopy. Other research is in the works to develop polyglucoside-based antimicrobial agents that would eat the protective coating around bacteria. One use for these agents would be as a sterile lubricants for implanted titanium prostheses.

For more information, contact Columbia University, 304 Low Library, Mail Code 4321, 535 W. 116th St., New York, NY 10027; (212) 854-5573; e-mail: rjn2@columbia.edu.—**DS**



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JUST 4 THE KIDS

All Barney bashers beware—he's back stronger than ever as an interactive toy that utilizes the latest advances in RF, and sensor technology. Known as Interactive Barney, the talking and moving plush toy was first introduced at the 1997 Toy Fair as a high-tech learning tool for children ages two to five.

The new toy's developer, Microsoft, Redmond, Wash., has now introduced two new characters, Arthur and D. W., aimed at children ages four and up. All three characters, much adored by younger school-age children, are representative of the latest trend in toys, "edutainment." In other words, these toys are no longer just cuddly stuffed animals, they're interactive toys that entertain as well as educate.

All three toys are based on a new technology called Microsoft Actimates, which was developed in conjunction with early learning specialists, experts in software technology, and electronic learning.

One of the key components of the Actimate technology is Microsoft's Realmation animation technology which makes it possible for the Actimate characters to move their heads and arms as they interact with your child. An eye sensor allows the toys to respond to changes in light so that they can play peek-a-boo. And, with just a squeeze of a hand or foot, the Actimate characters virtually come to life singing songs, playing dozens of games, and speaking literally thousands of words.

The Actimate characters can be used as standalone toys or can be activated for play using individualized accessories. The first accessory, a TV Pack, consists of an RF transmitter that plugs into a VCR, and operates via encoded VHS videotapes. Using a wireless transceiver attached to a VCR's video output jack, signals are sent to the toy to cause it to make comments appropriate to the action on a television screen. A newly developed broadcast system uses the same transceiver to make the Actimate respond to an actual TV show.

What this means is that the Actimate can actually move and interact, in a logical way, with a TV show or video. This concept has become so popular that most PBS stations now broadcast Actimates-compatible Barney & Friends and Arthur television shows.

MARIFRANCES WILLIAMS

The second accessory is a PC Pack with a CD-ROM game and an RF transmitter that plugs into the game port on the PC. The PC Pack allows the Actimate characters to interact with Actimate software. It works by utilizing a transmitter configured to work with the computer's sound card.

By plugging the Actimates PC Pack transmitter into the PC's game port, and inserting the accompanying software such as the "Fun on Imagination Island" CD-ROM, a world of fun and educational activities are opened up for the child. The Actimate character is simply placed alongside the PC while the child plays games and participates in activities on the screen.

With its 14,000 word vocabulary, the character is able to offer support and encouragement to the child with visual directives, cognitive prompts, or friendship phrases. The Actimate-compatible software may be used with or without the Actimates character, PC Pack, and TV Pack.

What's significant about the Actimates early learning toys is that they represent a dramatic advance in self-directed learning opportunities for young children. While playing with an Actimate, the child is encouraged to explore and discover the curriculum that's built into the software programs, videotapes, and games. The child learns such skills as cooperation, word recognition, reading and memory-building techniques, and is introduced to the concepts of music, rhythm, letters, and numbers.

To help parents better participate in this interactive learning process, the Actimates toys come equipped with a library of information from learning experts on children's growth and development, and suggested activities parents can initiate to enhance the child's mastery of important skills.

Even though Barney might not be your favorite character, he certainly has come a long way from his early days as just a big purple dinosaur that could sing, dance, and offer a moral lesson here and there. Used properly, Interactive Barney offers a new way to use today's technology to help start children on the early path to successful learning. So, while you might be nauseated at the thought of another chorus of "I love you, you love me, we're a happy family..." you might be interested in what he can do to help give your children an educational headstart.

Actimates interactive characters are now available at local retailers, and sell for an estimated price of $109.95. The Actimates TV Pack and Actimates PC Pack cost approximately $64.95 each, while the PC software titles and videotapes cost $34.95 and $14.95, respectively.

For more information contact Microsoft Corporation, One Microsoft Way, Redmond, WA 98052; (425) 882-8080, www.microsoft.com.

Marifrances D. Williams holds a degree in Liberal Studies from San Diego State University, Calif. She is currently a 5th-grade teacher at Los Ranchos Elementary, San Luis Obispo, Calif. Williams specializes in the identification of advanced technology for the use of child-focused applications. She may be reached at williamsofsm@lightspeed.net

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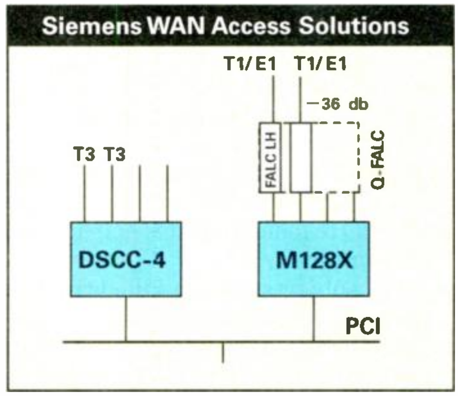

DSCC-4

- Large programmable FIFOs, 512 bytes each Tx and Rx
- DMA controller with 8 channels (4 Tx and 4 Rx)
- Lowest per port cost and the highest throughput port

MUNICH 128X

- The most cost competitive communications controller device for 128 channels.
- Easy to migrate from existing MUNICH 32 designs to the MUNICH 128X.
- A four port extension of the industry leading T1/E1 controller
- Compatible with H .100 bus

FALC LH

- Crystalless Jitter Attenuation/small footprint, high integration
- Bellcore and ETSI approved
- Software configurable T1/E1 and Long/Short Haul
- Also available as 4-port integrated chip

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FALC LH for the long — and short haul. The first integrated T1/E1 long haul and short haul framer and line interface device, the FALC LH operates at up to -36db, with an operation mode that's software selectable for easy configuration to worldwide standards.

MUNICH 128X — for seamless migration. A communications controller for 128 channels, the MUNICH 128X offers an easy migration path from existing designs and works seamlessly with the FALC LH. It's the smart solution for true design efficiency.

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TRUDEL TO FORM

JOHN D. TRUDELL

If a good future depends on innovation and freedom to create new realities, do conspiracy and control block progress? Of course. The Megastate is obsolete. We need more justice, less law, and a lot less bureaucratic interference.

Still, when all is said and done, the biggest problems are ignorance and outmoded thinking, and they're getting worse. It is interesting that all over the world, governments and large organizations consistently do such dumb things, often leading to truly catastrophic results.

My new book, *Engines of Prosperity*, discusses why standard Machine Age practice, "Old Think," often fails when applied in today's business environments. One fellow who has done much research on this subject is Dietrich Dorner. His work won Germany's highest science award, the Leibnitz Prize. His book, *The Logic of Failure*, should be on your reading list.

Dorner created computer worlds, wherein he let officials have dictatorial power and infinite resources to help societal problems. One scenario helped mythical "Moros," poor tribes who led a marginal existence in a desert. He found that this help usually left the natives worse off than they were originally.

His subjects usually killed the Moros with well-intentioned blunders. Their bad decisions caused massive die-offs due to a variety of unanticipated, but obvious in retrospect, disasters. Intervention would ease health problems, so the natives would breed geometrically, and then die from famine.

Attempts to help that problem by drilling wells would lead to further expansion, and a greater catastrophe when the water table was depleted. Amusingly, after the disasters, the subjects typically blamed everything, but their own actions.

If that seems too abstract, think of the welfare system, education, the war on drugs, your local road system, or the Chernobyl disaster, to which Dorner devotes a chapter. As with the Moros, the application of Old Think—one thing at a time, cause and effect, and linear thinking—often makes matters worse.

Today, everything is interrelated. We can't do one thing at a time, because everything has multiple outcomes. We can't think of isolated cause and effect, because all situations have side effects and long-term repercussions.

It is similar in the world of global business. George Grieder's new book, *One World Ready or Not*, says that 1994 may have demarcated the end of America's economic dominance. That was the first time since 1917, a war-year spike, that the annual outflow of financial returns to foreign investors exceeded all of the dividends, interest, and profits paid to U.S. investors.

Albert Einstein once said that "compound interest" was the most powerful force in nature. As Greider notes, our economy has drifted into the classic debtor's trap. The rest is mathematics. Like a household that tries to live on its credit cards, we go deeper in debt each month to pay for last month's spending.

What has this got to do with engineering and innovation? That's where it all comes together. A golden age of prosperity is possible.

By making the right choices, odds are we'll see a return to innovation and to creating unique new products. We can roll up our sleeves, work smart, and add value. The new focus can include good jobs and national prosperity, not just clones and paper profits. Things could get very interesting.

John D. Trudel, CMC, provides business innovation consulting to selected clients. Lectures, keynotes, and workshops are available. He is the author of "High Tech with Low Risk" and "Engines of Prosperity." The Trudel Group, 33470 Chinook Pl., Scappoose, OR 97056; (503) 638-8644; fax (503) 543-6361; e-mail: jtrudel@gstis.net; www.trudelgroup.com.

The Results Are In

To answer such people as Peter Nuskey, who wrote asking about the results of the First Annual QuickLook Paper Airplane Contest, we have a winner. Congratulations to Bill Riley of Davis & Associates, Richardson, Texas, who won the grand prize with his talking airplane. Actually, it didn't talk, it sang.

When I pushed the button, the plane sang, "Up in the air, junior birdmen." Then, when I flipped the toggle switch, the electric motor was triggered, causing the propeller to spin. I followed Riley's instructions, "...hand launch LEVEL for proper flight." Mind you, Communications and Networking Editor, Lee Goldberg and I were performing the test launch in the main hall by the elevators. The plane did fly, but crashed, knocking its own motor loose. Even without the motor, the plane did very well, met our guidelines, and made me laugh with the little song.

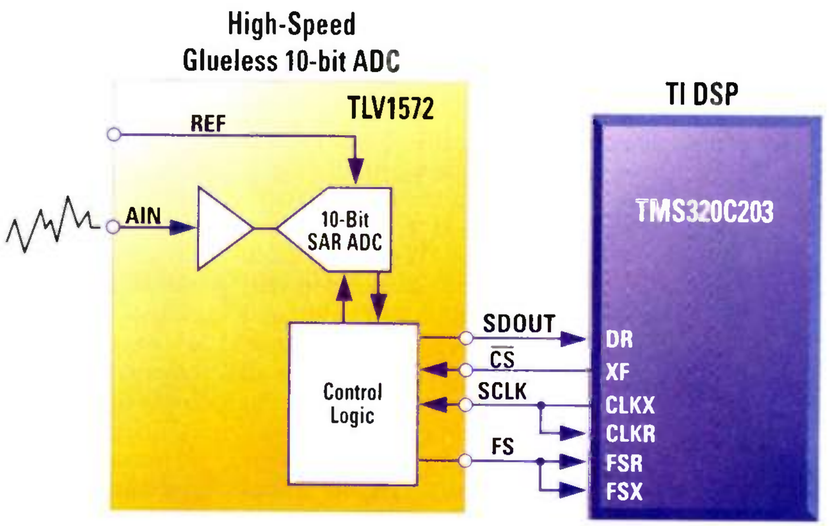
The singing plane garnered a $200 check from 1-800-BATTERIES, the contest's sponsor. Riley can use that money to purchase such items as a portable power pack, traveling software, and various other laptop gear, including batteries from the company's catalog.

About the contest itself, it did sadden me that not very many people sent in qualifying entries. I spoke about the problem with an engineer friend of mine. He said that it is indeed sad that engineers don't even have enough time to work on a contest such as this one because the time-to-market constraints of their jobs prohibit such efforts. Even the professional model maker, Nuskey, who wanted to know how the contest panned out failed to send in a plane. So, what does that tell you?

In any case, I enjoy talking with readers and e-mailing answers to questions. You tell me a lot about what you like in QuickLook and in the rest of the magazine. The constructive criticism is helpful as well. It's good to hear. Keep it up.

Contact us at QuickLook, 611 Route 46 West, Hasbrouck Heights, NJ 07604; (201) 393-6060; fax (201) 393-6242. I can be reached by e-mail at debras@csnet.net.—**DS**

FASTEST LOW-POWER, 10-BIT, 1.25-MSPS SERIAL ADC.



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- *3-V or 5-V operation*
- *Low power – 8 mW at 3 V, 25 mW at 5 V*
- *Auto-powerdown: 10 μA (max)*
- *Small footprint 8-pin SOIC*

** Price is per device in quantities of 1,000*

The TLV1572 is the industry's first high-speed, 10-bit ADC to interface gluelessly with TMS320 DSPs or (Q)SPI digital microcontrollers, while packaged in a tiny 8-pin SOIC. This device accepts analog input range from 0 V to V_{CC} and digitizes the input at a maximum 1.25-MSPS throughput rate. Implemented with a successive approximation architecture, the TLV1572 has a typical DNL of ±0.3 LSB and a typical INL of ±0.5 LSB. The Signal-to-Noise Ratio + Distortion is 59 dB (typ). The small 8-pin SOIC package, combined with an extremely high sample rate-to-power ratio, makes this ADC ideal for compact, low-power or remote high-speed systems. TLV1572 applications include mass storage, various automotive uses, wireless modem and digital motor control.

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TEXAS INSTRUMENTS

HEADS UP

Virtual Displays Come To Portable Electronics

S.W. Cheung, Motorola's vice president and general manager for their Displays Division, Tempe, Ariz., makes a key point when he talks about virtual displays. Cheung says that with conventional portable products, everything is getting smaller except the display. But virtual displays will eliminate this barrier, enabling portable product designers to volume-reduce the display, and provide more information.

Virtual displays are essentially electronic viewfinders. Users place them close to their eyes, seeing an image that can be as clear and crisp as a desktop monitor, which appears to be a foot or two away. This illusion will probably be driven by a display that is less than an inch in diagonal. Add some magnification optics, and the package is considerably smaller than a direct-view display with equivalent resolution.


CHRIS CHINNOCK

Virtual displays are now poised to explode into a host of new consumer products. This year could certainly see the first crop emerge in products ranging from digital still cameras and cell phones, to PDAs, smart card readers, camcorders, and head-mounted computer monitors.

The technology to create virtual displays is not necessarily new. For example, virtual-reality headsets and some camcorders already create virtual displays based upon a high-temperature polysilicon LCD fabrication process. These virtual display applications have not fared well, however, but projection products have. Japanese manufacturers dominate production of these polysilicon devices, but start-up Sarif, Vancouver, Wash., should enter the fray this summer.

The recent trend has been the emergence of new technical approaches to virtual displays that will enable new products and features at a variety of price points. These concepts are now maturing and being designed into products.

Not only virtual displays, but projection products to display data or video images for use in business, education and home entertainment, will benefit from these new devices.

Almost all of the new approaches are pushing to achieve high-fidelity color in a variety of resolutions. Resolutions from quarter-VGA (320 by 240) up to SXGA (1280 by 1024) are now possible.

Progress is showing up on a number of fronts. Consider an LED-based scanning technology from Reflection Technologies, Waltham, Mass. What was once monochrome red will soon be full color and VGA resolution. Planar, Beaverton, Ore., has an active-matrix electroluminescent technology that will soon allow color VGA or monochrome SXGA devices. Texas Instruments, Dallas, Texas, the developer of the digital micromirror device, recently worked with projection vendors to enable very-high-brightness projection products up to XGA resolution. But the loudest buzz is coming from the developers of a class of mini displays called liquid crystal on silicon (LCOS). Here, vendors fabricate the on- and off-screen electronics in single crystal silicon, and then build liquid-crystal layers on top. Both reflective and transmissive devices can be realized. It is a hybrid approach that leverages mature semiconductor and LCD fabrication techniques.

Players such as Displaytech, Longmont, Colo.; IBM, Yasu, Japan; and Microdisplay, Richmond, Calif; are all in the hunt. Most, however, acknowledge that Kopin, Taunton, Mass., now has taken the early lead in this technology area.

Since Kopin introduced their quarter-VGA CyberDisplay in April 1997, they have lined up Taiwan's United Microelectronics Corp. and Unipac Optoelectronics as high-volume silicon foundries. They've also acquired some high-profile strategic partners like Motorola and FujiFilm Microdevices Co. Ltd., Sendai Industrial Park, Japan. FujiFilm is currently developing chip sets for digital cameras. January marked the introduction of Kopin's color QVGA mini display.

Why has Kopin been so success[illegible] and so high profile? A recent I[illegible] may answer that question, but su[illegible] cess is based upon good fundame[illegible] tals. Motorola for example, cited t[illegible] manufacturability, availability [illegible] color, a rapid time-to-market, and l[illegible] cost of the Kopin display as key re[illegible] sons for forming a partnership.

By the third quarter of this year, Motorola plans to offer OEM customers display engines, including the Kopin display; magnification optics; RGB LEDs for illumination; and an IC for databus interfacing. Volume customers can expect to pay about $30 for this—less than half the price of a comparable direct-view LCD.

Other LCOS vendors are quieter about the products they're develo[illegible] ing for their customers, but digi[illegible] cameras and PDAs are high on t[illegible] list. At higher price points, bo[illegible] front- and rear- screen projecti[illegible] systems are using these devices. E[illegible] pect to see CRT-based, rear-scre[illegible] TVs replaced with engines from t[illegible] category.

Such devices also play well in t[illegible] convergence of computers, digital T[illegible] and the Internet. As IBM's Paul A[illegible] explained, "We will see lots of creative products in categories we haven't even thought of yet." Stay tuned.

Chris Chinnock holds a BSEE from the University of Colorado and reports on flat-panel displays an[illegible] other emerging technologies. H[illegible] company, Technical Marketing Se[illegible] vice, provides writing, marketi[illegible] and public relations services to te[illegible] nology companies. Chinnock can [illegible] reached at (203) 849-8059; fax (20[illegible] 849-8069; e-mail: chrischinnock[illegible] compuserve.com.

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- 120 - 700 Watts
- 1 - 4 Outputs
- Low Cost

Deltron inc.
POWER PRODUCTS

VR SERIES HI-REL SWITCHERS

Single Output • 300-700 Watts

DESCRIPTION

VR Series World Class switching power supplies are a family of single output models designed for applications requiring ***Ultra Reliability*** and ***Low Cost!*** These supplies have actual demonstrated MTBF ratings up to 1 million hours. The time tested design has been continually updated to take advantage of the latest technological improvements in circuits and components resulting in the fine performance of these supplies.

MODELS & RATINGS

Max Power	Output	Model
300W	5V @ 50A	VR300AXX
	12V @ 25A	VR300BXX
	15V @ 20A	VR300CXX
	24V @ 12A	VR300DXX
	48V @ 6A	VR300EXX
500W	5V @ 80A	VR500AXX
	12V @ 40A	VR500BXX
	15V @ 30A	VR500CXX
	24V @ 20A	VR500DXX
	48V @ 10A	VR500EXX
700W	5V @120A	VR700AXX
	12V @ 58A	VR700BXX
	15V @ 46A	VR700CXX
	24V @ 29A	VR700DXX
	48V @ 15A	VR700EXX

FEATURES

- *UL, CSA, TÜV (IEC, EN), CE.*
- *5.5 watts per cubic inch.*
- *80% typical efficiency.*
- *1,000,000 hrs. demonstrated MTBF.*
- *Stock delivery.*
- *Full complement of options.*

VR OPTIONS

Option Code	Function
00	None
01	Power Fail Monitor
02	Auto Ranger
04	Pilot Bias
08	Screen Cover
16	End Fan Cover
32	Top Fan Cover

To order, replace "XX" in model number with sum of Option Codes desired.

CV SERIES ENCLOSED SWITCHERS

Single Output • 360-600 Watts

DESCRIPTION

The CV Series is a line of low profile, fan cooled power supplies which utilize Deltron's field proven V Series components. CV units are single output models in a rugged enclosed package nominally 3 inches in height and 5 inches in width. With power ratings of 360 to 600 watts, these units are a space saving alternative to 5 x 8 inch shoe box modules.

MODELS & RATINGS

Max Power	Output	Model
360W	5V @ 72A	CV360AXX
	12V @ 30A	CV360BXX
	15V @ 24A	CV360CXX
	24V @ 15A	CV360DXX
	28V @ 13A	CV360JXX
	48V @ 7.5A	CV360EXX
500W	5V @ 100A	CV501AXX
	12V @ 42A	CV501BXX
	15V @ 33A	CV501CXX
	24V @ 21A	CV501DXX
	28V @ 18A	CV501JXX
	48V @10.5A	CV501EXX
600W	5V @ 120A	CV601AXX
	12V @ 50A	CV601BXX
	15V @ 40A	CV601CXX
	24V @ 25A	CV601DXX
	28V @21.5A	CV601JXX
	48V @12.5A	CV601EXX

FEATURES

- *UL, CSA, TÜV (IEC, EN), CE.*
- *4 watts per cubic inch.*
- *80% typical efficiency.*
- *200,000 hrs. demonstrated MTBF.*
- *Heavy duty enclosed chassis.*
- *Full complement of options.*

CV OPTIONS

Option Code	Function
00	None
02	Power Fail Monitor
04	Thermal Shutdown
08	Logic Inhibit
16	Auto Ranger

To order, replace "XX" in model number with sum of Option Codes desired.

V SERIES OPEN FRAME SWITCHERS

Single & Quad Outputs • 120-600 Watts

DESCRIPTION

V Series World Class switching power supplies are a family of single and quad output models designed for a wide variety of commercial and industrial applications. These industrial workhorses have demonstrated MTBF ratings greater than 500,000 hours. A proprietary proportional drive circuit prevents excess switch saturation and permits higher switching frequency operation. This makes possible increased reliability and a compact size.

One of the unique features of the V Series is a dual loop regulation system. This system provides a tightly regulated main output and eliminates cross regulation in the auxiliaries.

FEATURES

- *UL, CSA, TÜV (IEC, EN), CE.*
- *4.8 watts per cubic inch.*
- *80% typical efficiency.*
- *500,000 hrs. demonstrated MTBF.*
- *High power auxiliaries.*
- *High peak current capability.*
- *Full complement of options.*

SINGLE OUTPUT

Max Power	Output	Model
120W	5V @ 25A	V120AXX
	12V @ 10A	V120BXX
	15V @ 8A	V120CXX
	24V @ 5A	V120DXX
180W	5V @ 36A	V180AXX
	12V @ 15A	V180BXX
	15V @ 12A	V180CXX
	24V @ 7.5A	V180DXX
250W	5V @ 50A	V250AXX
	12V @ 21A	V250BXX
	15V @ 17A	V250CXX
	24V @ 11A	V250DXX

Max Power	Output	Model
270W	5V @ 54A	V270AXX
	12V @ 22A	V270BXX
	15V @ 18A	V270CXX
	24V @ 12A	V270DXX
360W	5V @ 72A	V360AXX
	12V @ 30A	V360BXX
	15V @ 24A	V360CXX
	24V @ 15A	V360DXX

Other voltages, e.g. 2V, 3.3V, 28V, and 48V available on special order.

Max Power	Output	Model
500W	5V @ 100A	V501AXX
	12V @ 42A	V501BXX
	15V @ 33A	V501CXX
	24V @ 21A	V501DXX
600W	5V @ 120A	V601AXX
	12V @ 50A	V601BXX
	15V @ 40A	V601CXX
	24V @ 25A	V601DXX

QUAD OUTPUT

Max Power	Output 1	Output 2	Output 3	Output 4	Model
225W	5V @ 30A	+12V @ 6(12)A	-12V @ 4A	-5V @ 4A	V225AXX
	5V @ 30A	+12V @ 6A	-12V @ 4A	+24V @ 4(8)A	V225BXX
	5V @ 30A	+15V @ 6(12)A	-15V @ 4A	-5V @ 4A	V225CXX
	5V @ 30A	+15V @ 6A	-15V @ 4A	+24V @ 4(8)A	V225DXX
	5V @ 30A	+12V @ 6(12)A	-12V @ 4A	+12V @ 4A	V225EXX
300W	5V @ 40A	+12V @ 4A	-12V @ 4A	-5V @ 3A	V300AXX
	5V @ 40A	+12V @ 4A	-12V @ 4A	+24V @ 3(5)A	V300BXX
	5V @ 40A	+15V @ 4A	-15V @ 4A	-5V @ 3A	V300CXX
	5V @ 40A	+15V @ 4A	-15V @ 4A	+24V @ 3(5)A	V300DXX
	5V @ 40A	+12V @ 4A	-12V @ 4A	+12V @ 3(5)A	V300EXX
325W	5V @ 45A	+12V @ 8(16)A	-12V @ 6A	-5V @ 4A	V325AXX
	5V @ 45A	+12V @ 8A	-12V @ 6A	+24V @ 4(8)A	V325BXX
	5V @ 45A	+15V @ 8(16)A	-15V @ 6A	-5V @ 4A	V325CXX
	5V @ 45A	+15V @ 8A	-15V @ 6A	+24V @ 4(8)A	V325DXX
	5V @ 45A	+12V @ 8(16)A	-12V @ 6A	+12V @ 4A	V325EXX
400W	5V @ 50A	+12V @ 8A	-12V @ 8A	-5V @ 4A	V400AXX
	5V @ 50A	+12V @ 8A	-12V @ 8A	+24V @ 4(6)A	V400BXX
	5V @ 50A	+15V @ 8A	-15V @ 8A	-5V @ 4A	V400CXX
	5V @ 50A	+15V @ 8A	-15V @ 8A	+24V @ 4(6)A	V400DXX
	5V @ 50A	+12V @ 8A	-12V @ 8A	+12V @ 4(6)A	V400EXX
500W	5V @ 60A	+12V @ 10A	-12V @ 10A	-5V @ 5A	V500AXX
	5V @ 60A	+12V @ 10A	-12V @ 10A	+24V @ 5(8)A	V500BXX
	5V @ 60A	+15V @ 10A	-15V @ 10A	-5V @ 5A	V500CXX
	5V @ 60A	+15V @ 10A	-15V @ 10A	+24V @ 5(8)A	V500DXX
	5V @ 60A	+12V @ 10A	-12V @ 10A	+12V @ 5(8)A	V500EXX
600W	5V @ 80A	+12V @ 10(20)A	-12V @ 10A	-5V @ 5A	V600AXX
	5V @ 80A	+12V @ 10A	-12V @ 10A	+24V @ 5(10)A	V600BXX
	5V @ 80A	+15V @ 10(20)A	-15V @ 10A	-5V @ 5A	V600CXX
	5V @ 80A	+15V @ 10A	-15V @ 10A	+24V @ 5(10)A	V600DXX
	5V @ 80A	+12V @ 10(20)A	-12V @ 10A	+12V @ 5A	V600EXX

V OPTIONS

Option Code	Function
00	None
01	OVP protects all auxiliaries
02	Power Fail Monitor
04	Thermal Shutdown
08	Cover
16	Logic Inhibit
32	Post Regulator for output 4

To order, replace "XX" in model number with sum of Option Codes desired.

NOTES:

1. *Numbers in parentheses ( ) are peak ratings for short duration service such as motor starting.*
2. *Output 1 is floating and can be either polarity.*
3. *Quads require 10% of maximum power distributed among auxiliary outputs for optimum performance.*
4. *Outputs can operate to no load with slight increase in specifications.*

SPECIFICATIONS

INPUT
90-132 VAC or 180-264 VAC, 47-440 Hz.
Consult factory for 400 Hz. operation.

EMISSIONS
FCC 20780 Part 15/EN 55022, Class A Conducted.
EN 61000-3-3, Voltage Fluctuations.

IMMUNITY
IEC 1000-4-2/EN 61000-4-2, Electrostatic Discharge.
IEC 1000-4-3/EN 61000-4-3, Radiated Field.
IEC 1000-4-4/EN 61000-4-4, Electrical Fast Transients.
IEC 1000-4-5/EN 61000-4-5, Level 3 Surge.
IEC 1000-4-6/EN 61000-4-6, Conducted Field.

INPUT SURGE
17 amps peak from cold start for models up to 250 watts and VR300, 68 amps for other models, from nominal 110 or 220 VAC.

EFFICIENCY
80% typical.

HOLDUP TIME
20 milliseconds after loss of nominal AC power.

OUTPUTS
See table of models.

LINE REGULATION
±0.1% for line change from nominal to min. or max. rating with 20% min. load on the measured output.
±0.05% with post regulator and no min. load.
Singles to no load.

LOAD REGULATION

5V main/singles	±0.2%
-5V aux.	±3%
±12V aux.	±2%
±15V aux.	±2%
+24V aux.	±1.5%

Post Regulated Outputs

Option 32	±0.05%

for load change from 60% to 20% or 100% max. rating.
With post regulator to no load. Singles to no load.

CROSS REGULATION
±0.2% for load change on the main 5V output from 75% to 50% or 100% max. rating with 20% min. load on the measured output.
±0.05% with post regulator and no min. load.
Not applicable to singles.

CENTERING

5V main/singles		±5% trim adj.
Aux. 1 and 2		±5% trim adj. tracking
Aux. 3:	-5V	±3%
	+12V	±2%
	+24V	±1%

with all outputs loaded to 50% max. ratings and output #2 set precisely at its rated value. With post regulator ±3% trim adj.

RIPPLE & NOISE
1% or 100 mV, pk.-pk., 20 MHz bandwidth.

OPERATING TEMPERATURE
0-70°C. Derate 2.5%/°C above 50°C.

COOLING

Models	Forced Air
V120, V180, V225, V250, V270, V300, VR300, V360	30 CFM
V325, V400, V500, VR500, V501, V600, V601, VR700	60 CFM

TEMPERATURE COEFFICIENT

5V main/singles	±0.02%/°C
Auxiliaries	±0.05%/°C
With post regulator	±0.02%/°C

DYNAMIC RESPONSE
Peak transient less than ±2% or ±200 mV for step load change from 75% to 50% or 100% max. ratings.

RECOVERY TIME
Less than 400 microseconds on main/singles output.
Less than 50 microseconds on post regulated auxiliaries.

SAFETY
Units meet UL 1950, CSA 22.2 No. 950, EN 60 950, IEC 950.

DIELECTRIC WITHSTAND
3750 VRMS input to ground.
3750 VRMS input to output.
700 VDC output to ground.

SPACING
8 mm primary to secondary.
4 mm primary to grounded circuits.

LEAKAGE CURRENT
0.75 mA at 115 VAC, 60 Hz. input.

INPUT UNDERVOLTAGE
Proprietary proportional drive and low voltage lockout protects against damage for undervoltage operation.

SOFT START
Units have soft start feature to protect critical components.

OVERVOLTAGE PROTECTION
Standard on main output/singles. Optional on auxiliaries.

REVERSE VOLTAGE PROTECTION
All outputs are protected up to load ratings.

OVERLOAD
Outputs short circuit protected by current foldback with automatic recovery. Post regulators have individual current foldback protection.

REMOTE SENSING
On singles/5V mains which are fully isolated from all auxiliaries.

SHOCK & VIBRATION
Shock per MIL-STD 810-E Method 516.4, Procedure I.
Vibration per MIL-STD 810-E Method 514.4, Category 1, Procedure I.

MECHANICAL

MODELS	H	x	W	x	L
VR300	2.50"	x	4.85"	x	8.50"
VR500, VR700	2.75"	x	4.85"	x	10.50"
CV360, CV501, CV601	3.15"	x	4.85"	x	12.63"
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V270, V360, V501, V601	2.50"	x	4.75"	x	10.50"
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Exhibition & Conference on System Integration in Microelectronics, June 16-18. Nuremberg Exhibition Centre. Call +49 711-61946-26/-74; fax +49 711-61946-93; www.mesago.de

IEEE Antennas and Propagation Society International Symposium and URSI National Radio Science Meeting, June 21-26. Stouffer Renaissance Waverly Hotel, Atlanta, GA. Contact Andrew Peterson, Georgia Institute of Technology, School of Electrical & Computer Engineering, ECE 0250/Van Leer, Atlanta, GA 30332; (404) 894-4697; fax (404) 894-4641; e-mail: peterson@ee.gatech.edu.

American Control Conference (ACC '98), June 24-26. Adams Mark Hotel, Philadelphia, PA. Contact Joe Chow, ECSE Department Rensselaer Polytechnic Institute, Troy, NY 12180-3590; (518) 276-6374; fax (518) 276-6261; e-mail: chowj@rpi.edu.

JULY

Conference on Precision Electromagnetic Measurements (CPEM '98), July 6-10. Renaissance Washington Hotel, Washington, D.C. Contact Katherine H. Magruder, NIST, Bldg. 220, Room B162, Gaithersburg, MD 20899; (301) 975-2402; fax (301) 926-3972; e-mail: katherine.magruder@nist.gov.

Second IEEE World Conference on Photovoltaic Energy Conversion (WCPEC), July 6-10. Vienna, Austria. Contact Heinz Ehmann, WIP, Sylvensteinstrasse 2, D-81369 Munchen, Germany.

IEEE International Geoscience & Remote Sensing Symposium (IGARSS '98), July 6-10. Sheraton Seattle, WA. Contact Tammy I. Stein, IGARSS Business Office, 2610 Lakeway Dr., Seabrook, TX 77586-1587, (281) 291-9222; fax (281) 291-9224; e-mail: tstein@phoenix.net.

IEEE Power Engineering Society Summer Meeting, July 12-16. Sheraton San Diego Hotel & Marina, San Diego, CA. Contact Terry Snow, San Diego Gas & Electric, P.O. Box 1831, San Diego, CA 92112; (619) 696-2780; fax (619) 699-5096; e-mail: t.snow@ieee.org.

SPIE's Annual Meeting & Optical Instrumentation Show, July 19-24. San Diego, California. Contact SPIE Exhibits Dept., Post Office Box 10, Bellingham, Washington 98227-0010; (360) 676-3290; fax (360) 647-1445; e-mail: exhibits@spie.org.

IEEE Nuclear & Space Radiation Effects Conference (NSREC '98), July 20-24. Newport Beach, California. Contact Jim Schwank, Sandia National Laboratories, Post Office Box 5800, MS-1083, Albuquerque, New Mexico 87185-1083; (505) 844-8376; fax (505) 844-2991; e-mail: schwanjr@sandia.gov.

AUGUST

IEEE International Symposium on Information Theory, Aug. 16-21. Massachusetts Institue of Technology, Cambridge, MA. Contact G. David Forney, Motorola Inc., MS M4-15, 20 Cabot Blvd., Mansfield, MA 02048-1193; (508) 261-5347; fax (508) 337-7173; e-mail: LUSE27@email.mot.com.

IEEE International Symposium on Electromagnetic Compatibility (EMC '98), Aug. 23-28. Adam's Mark Hotel, Denver, CO. Contact R. Barry Wallen, P.O. Box 387, 1350 County Rd., #16, Rollinsville, CO 80474; (303) 682-6600; fax (303) 682-6672; e-mail: bwallen@intellistor.com.

AUTOTESTCON '98, Aug. 24-27. Salt Palace Convention Center, Salt Lake City, UT. Contact Robert Myers, Myers/Smith Inc., 3685 Motor Ave., Suite 240, Los Angeles, CA 90034; (310) 287-1463; fax (310) 287-1851; e-mail: bob.myers@ieee.org.

SEPTEMBER

Embedded Systems Conference Europe, September 7-9. Royal Ascot, England. Contact Michelle Troop, Miller Freeman Inc., (415) 278-5229; mtroop@mfi.com.

Sixth European Congress on Intelligent Techniques & Soft Computing (EUFIT '98), Sept. 7-10. Aachen, Germany. Contact Conference Secretariat: EUFIT '98, Promenade 9, D-52076 Aachen, Germany; +49 2408-6969; fax +49 2408-94582; e-mail: eufit@mitgmbh.de; www.mitgmbh.de/elite/eufit.html.

ICSPAT & DSP World Expo, September 13-16. Toronto Metro Convention Center, Toronto, Ontario, Canada. Contact Liz Austin, Miller Freeman Inc., (888) 239-5563, (415) 538-3848, e-mail: dspworld@mfi.com;www.dspworld.com.

WESCON '98, Sept. 15-17. Anaheim Convention Center, Anaheim, CA. Contact Electronic Conventions Management, (800) 877-2668; (310) 215-3976; fax (310)641-5117; e-mail: wescon.ieee.org; www.wescom.com.

Fourth International Symposium on Ultra-Clean Processing of Silicon Surfaces (UCPSS '98), Sept. 21-23. Oostende, Belgium. Contact Barbara Kalkis, Maestro PR, (408) 996-9975; fax (408) 996-8534, kalkis@compuserve.com.

Second International Conference on Evolvable Systems (ICES '98), Sept. 23-26. Swiss Federal Institute of Technology, Lausanne, Switzerland. Contact Andres Perez-Uribe, conference secretariat, +41 21- 6932652; fax +41 21-6933705; e-mail: Andres.Perez@di.epfl.ch; lslwww.epfl.ch/ices98/.

IEEE Petroleum and Chemical Industry Technical Conference (PCIC '98), Sep. 28-30. The Westin Hotel, Indianapolis, IN. Contact David L. Johnson, Eli Lilly & Co., Lilly Corporate Center, DC 4121, Indianapolis, IN 46285; (317) 276-1717; fax (317) 276-9394; e-mail: david_lee_johnson@lilly.com.

OCTOBER

Fifth IEEE International Conference on Image Processing (ICIP '98), Oct. 4-7. The Westin Hotel Chicago, Chicago, IL. Contact Billene Mercer, CMS, 3109 Westchester Ave., College Station, TX 77845-7919; (409) 693-6000; fax (409) 493-6600; e-mail: mercer@conf.mgmt.com.

IEEE International Telecommunications Energy Conference, Oct. 4-8. Hyatt Regency Hotel, San Francisco, CA. Contact Lou Scerbo, Bellcore, Room 1J206G, 445 South St., Morristown, NJ 07960; (201) 829-5962; fax (201) 829-5962; e-mail: lscerbo@notes.cc.bellcore.com.

PCI Plus Europe '98 Developers' Conference and Expo, Oct. 5-8. Le Palais des Congres (Porte Maillot), Paris, France. Contact Active Exhibitions
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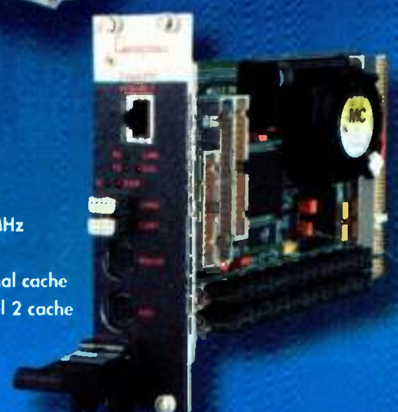

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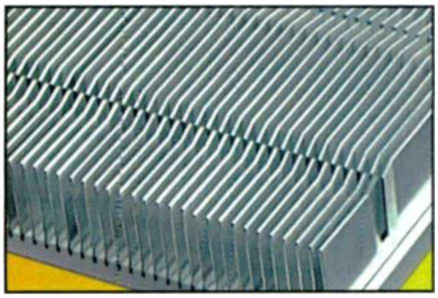

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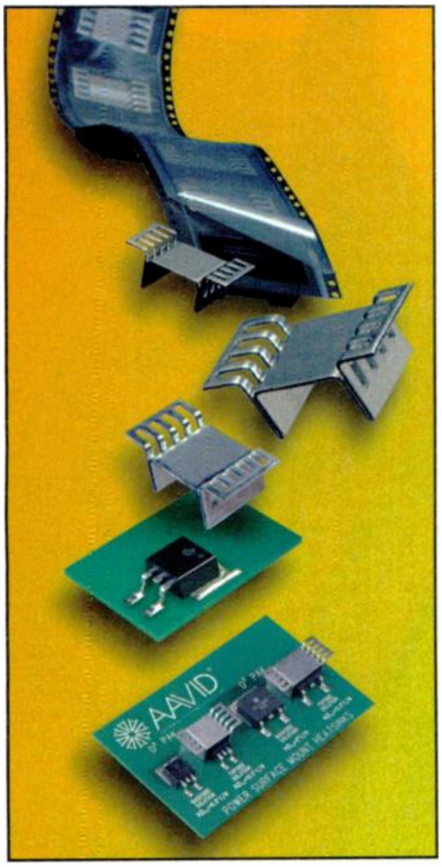

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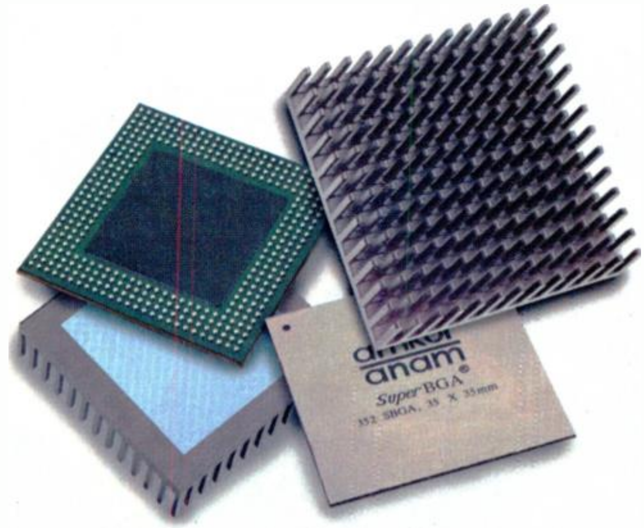

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Next-Generation Cellular Technologies: Convergence Or Chaos?

Competing Standards And Uncertain Technologies Characterize Efforts To Deliver Third-Generation Wireless Services With The Promise Of An Advanced Global Network On The Horizon.

Lee Goldberg

SPECIAL REPORT

It's no secret that wireless services, in the form of cellular and PCS phones, are among the biggest growth markets on the planet. In many urban areas, second-generation digital technologies are rapidly displacing first-generation analog services, bringing paging, messaging, and e-mail access into the same handset that used to only deliver voice. Even before the second-generation networks have been fully deployed, a third generation (3G) of wireless networks is already being defined. With multimegabit data rates and sophisticated call control functions, they promise to bring high-speed Internet, video, and a host of other advanced services into the palm of your hand.

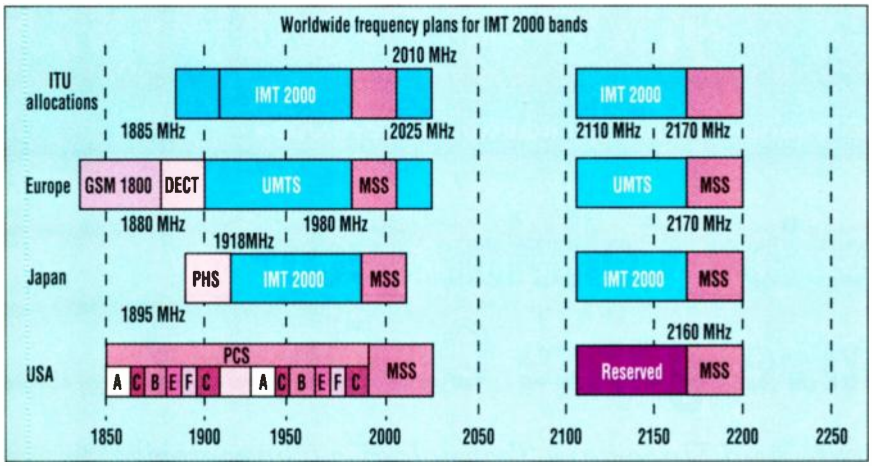
Of equal importance, 3G technologies hold the potential to unify a fragmented wireless infrastructure, allowing access to all of these services nationally, or even globally, with a single handset. However, many questions remain as to whether infighting between competing factions within the wireless industry will prevent the realization of this utopian vision. While it will take some heavy silicon to deliver these palmtop wonders to the public, technology is only part of the equation. Annoying as it is to us technical types, economics and market politics will play equal roles in defining the types of services available in 3G networks, as well as the technologies used to deliver them.

During the next year, the standards that will form the "genetic code" for building 3G systems are finalized. These standards, have been under development in Europe and Japan for the past five or more years, with the U.S. entering the fray just recently. The results of these efforts will leave a lasting mark since they will determine not only the technologies used in 3G systems, but also whether they will be able to interoperate. Because these nontechnical factors will play such a dominant role in determining the shape of 3G, it would be helpful to get an overview of the standards efforts before getting down to nuts-and-bolts issues.

Art Courtesy: Sony Wireless

Deja Vu Again

Until recently, it looked as though 3G wireless networks would repeat the pattern of global fragmentation that has characterized the market to date, with North America,



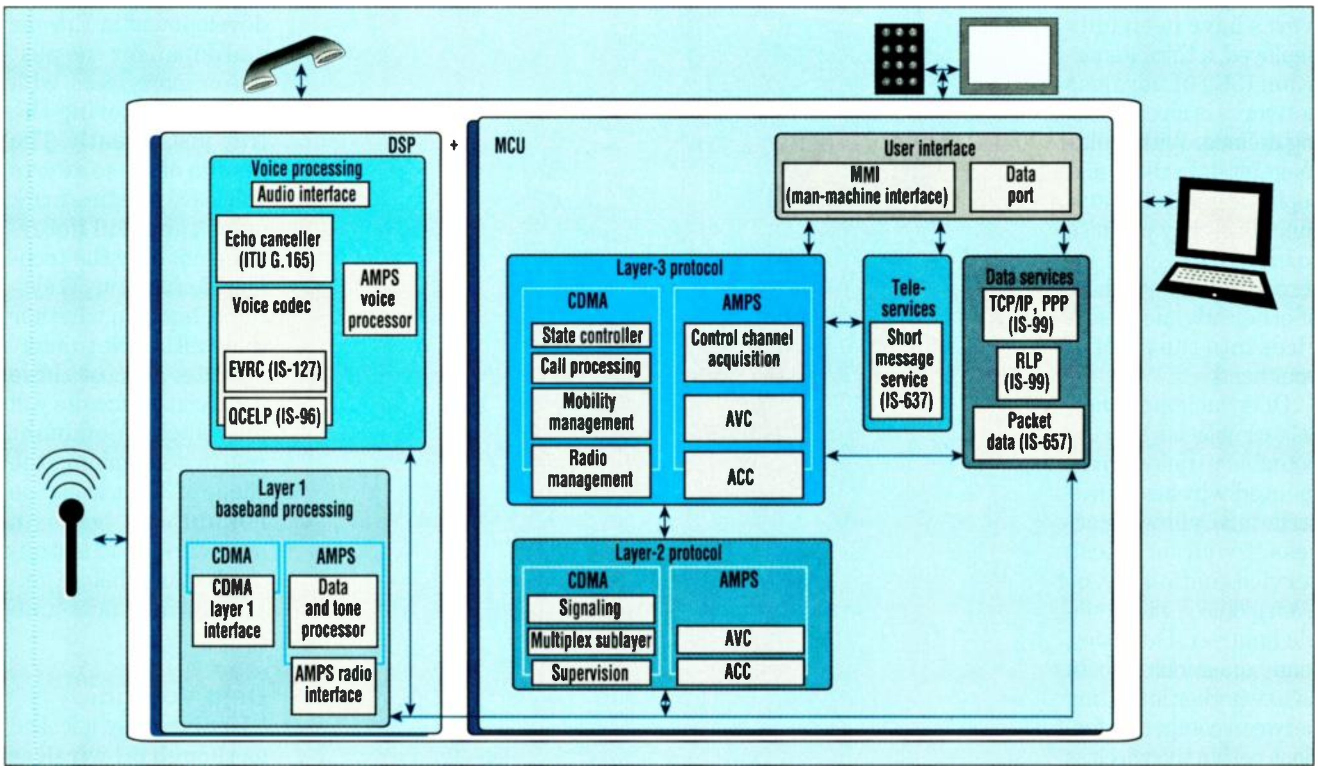
1. Europe and Japan have harmonized their spectrum allocation with the ITU's frequency plan for a global 3G network. The U.S. has "paved over" most of the terrestrial 3G spectrum, making interoperability a challenge.

Japan, and Europe retreating into separate camps. Japan retreated into its own Personal Handyphone System, (PHS) technology and has only recently begun to implement regular digital cellular service. The worst offender, however, may have been the United States. In a frenzy of free-market mania, the U.S. Federal Communications Commission (FCC) practically turned over the standards-making process for digital U.S. 2G cellular service to the industry it was assigned to regulate. Rather than accelerating the roll-out of digital cellular, this policy had the opposite effect as competing carriers turned North America into an isolated, balkanized landscape of non-interoperable technologies.

Determined to avoid a future quagmire, the International Telecommunication Union's (ITU's) World Radio Administration Congress (WARC) allocated a worldwide spectrum and issued its guidelines for an advanced wireless standard in 1992. In addition to assigning the 1885 MHz to 2200 MHz band, the Congress set some basic goals for advanced systems, leaving the details to be worked out by the telecommunications industry *(Fig. 1)*. Most notably, WARC set very aggressive goals for delivering wireless data to handsets.

When communicating with pico-cells in fixed locations, a 3G handset was expected to transmit and receive multimedia streams at up to 2 Mbits/s. In low-speed mobile situations (walking, bicycling, etc.), a local area link was expected to support transmissions at speeds of up to 384 kbits/s, and 144 kbits/s for high-speed environments, such as cars or trains. The ITU's initial guidance and subsequent issuance of the International Mobile Telecommunications 2000 (IMT-2000) standard has provided guidelines for worldwide development of 3G systems.

Initially, a massive menagerie of competing technologies jumped into the fray, but by 1996, three major contenders from North America, Europe, and Japan emerged, each seemingly more interested in dominating its own



2. "Soft" 2G cellular phone designs have faster, easier, and more likely to meet stringent standards, thanks to highly evolved, fully certified third-party software. This embedded IS-95 embedded communications suite from Telogy Networks can be easily ported to a number of baseband DSPs and controller chips. It is likely that this trend will accelerate for 3G handset designs.

market, rather than providing a globally compatible standard. The U.S. continued to show little or no interest in any sort of interoperability with the rest of the world by selling off most of the internationally reserved 3G spectrum for use by 2-G PCS systems *(Fig. 1, again)*. Until recently, it looked like America and Japan wouldremain isolated pockets of proprietary technologies within the global wireless community.

Meanwhile, back across the Atlantic, a surprising evolution was taking place. Before GSM had really completed its rollout, its developers were hard at work developing its successor. Under the guidance of ETSI, the Future Public Land/Mobile Telecommunication System (FPLMTS) development effort was established. Much like GSM that preceded it, FPLMTS was a pan-European project, involving government agencies from nearly all countries and most major electronics manufacturers.

As the project matured, its name changed, as did its goals. What emerged was a much more flexible system built on the strengths of the GSM architecture while greatly expanding on its capabilities. Under a less awkward name, Universal Mobile Telecommunication System (UMTS), the project moved away from its original charter that detailed every application and device the network was to provide.

To avoid creating a rigidly defined network that would rapidly become obsolete, UMTS was restructured to be more open-ended. ETSI's SMG1 committee chairperson, Derek Richards explains it this way: "UMTS aims to standardize service capabilities and not the services themselves. (This) will provide mechanisms to enable service providers and operators to create their own supplementary services, teleservices, and end-user applications." Toward this end, UMTS was designed as "a system of capabilities, functionalities, and relationships which are independent of their physical implementation or their location within the network hierarchy."

This permitted the UMTS architects to provision it with resources and signaling protocols that could be used in an object-oriented manner that would permit operators to mix-and-match functions, applications, and services at will. If fully implemented, UMTS will let a particular application select its preferred security functions, data transmission protocols, and even select speech codecs with bit rates from two to 64 kbits/s.

By decoupling services from the infrastructure, it is hoped that subscribers will be able to have something known as a "Virtual Home Environment (VHE)," with a specific "look and feel." The VHE will include a user-defined feature set and a list of network resources that the subscriber has signed up for. When embedded into a smart card, a VHE will allow you to configure a UMTS handset for things like your voice-activated dialing directory, the speed at which you wish to retrieve data off the World Wide Web, the level of quality of audio or video connection you wish to pay for, and so on.

A European Perspective On 3rd-Generation Wireless Technology And Politics

The decision to adopt both W-CDMA and TD-CDMA as the standard for UTRA—UMTS Terrestrial Radio Access—was mostly political, although there is some technical rationale. The politics revolve around the desire of the Japanese Ministry of Post and Telecommunications (MPT) to ensure that whatever standard is adopted in Japan for "next generation" cellular services is as international as possible. At the same time, the European Union is equally keen to ensure that the standards for UMTS will allow the perceived success of GSM to be sustained.

But the Japanese mobile network operators, in particular the all-powerful NTT DoCoMo, had already made their decision to use wideband CDMA (W-CDMA). DoCoMo also is a very influential voice in RIBA, the Japanese equivalent of TIA. In addition, DoCoMo owns some of the essential patents in the variant of W-CDMA they developed in collaboration with Ericsson and Nokia.

The techno-politicians tended to favor the W-CDMA solution. For example, the British government representative cast all its weighted votes in favor of W-CDMA. However, the main stumbling block was patents. ETSI Special Mobile Group calculated that there are around 1500 "essential patents" relating to W-CDMA. Of these, only 150 or so are owned by European companies, with 750 owned in Japan, and the rest in North America. On the other hand, time-division CDMA (TD-CDMA), was promoted by the UMTS Alliance comprising Alcatel, Bosch, Italtel, Motorola, Nortel, Siemens, and Sony. It involves 150 essential patents, spread roughly 50, 50, 50 between Europe, Japan, and North America.

Eventually the Japanese—really NTT—agreed to the formation of a "patent pool," and to sign up to the ETSI rule that has worked so well for GSM that all essential patents should be made available to all involved in UMTS "on a fair and nondiscriminatory basis." That done, the consensus was unanimous for a compromise using both technologies.

The technical rationale for adopting both WCDMA and TD-CDMA relates to the way in which the spectrum has been allocated for UMTS by the ITU (and recently by Japan). It is divided into seven segments, allowing both WCDMA and TD/CDMA services to operate *(see the table)*. Note that the FDD-based WCDMA service was assigned a spectrum in paired segments—one each for transmit and receive, while the TDD-based service is unpaired because time slots can be assigned for uplink and downlink channels.

While W-CDMA is suitable for the paired segments (3 and 6), it is not considered efficient for the nonpaired TDD segments. These TDD bands are seen as beign used for applications such as Internet/intranet access and transaction-based applications, where dynamic "on-demand" bandwidth allocation and asymmetric working is required. Theoretically, TD-CDMA can assign any number of times slots to a

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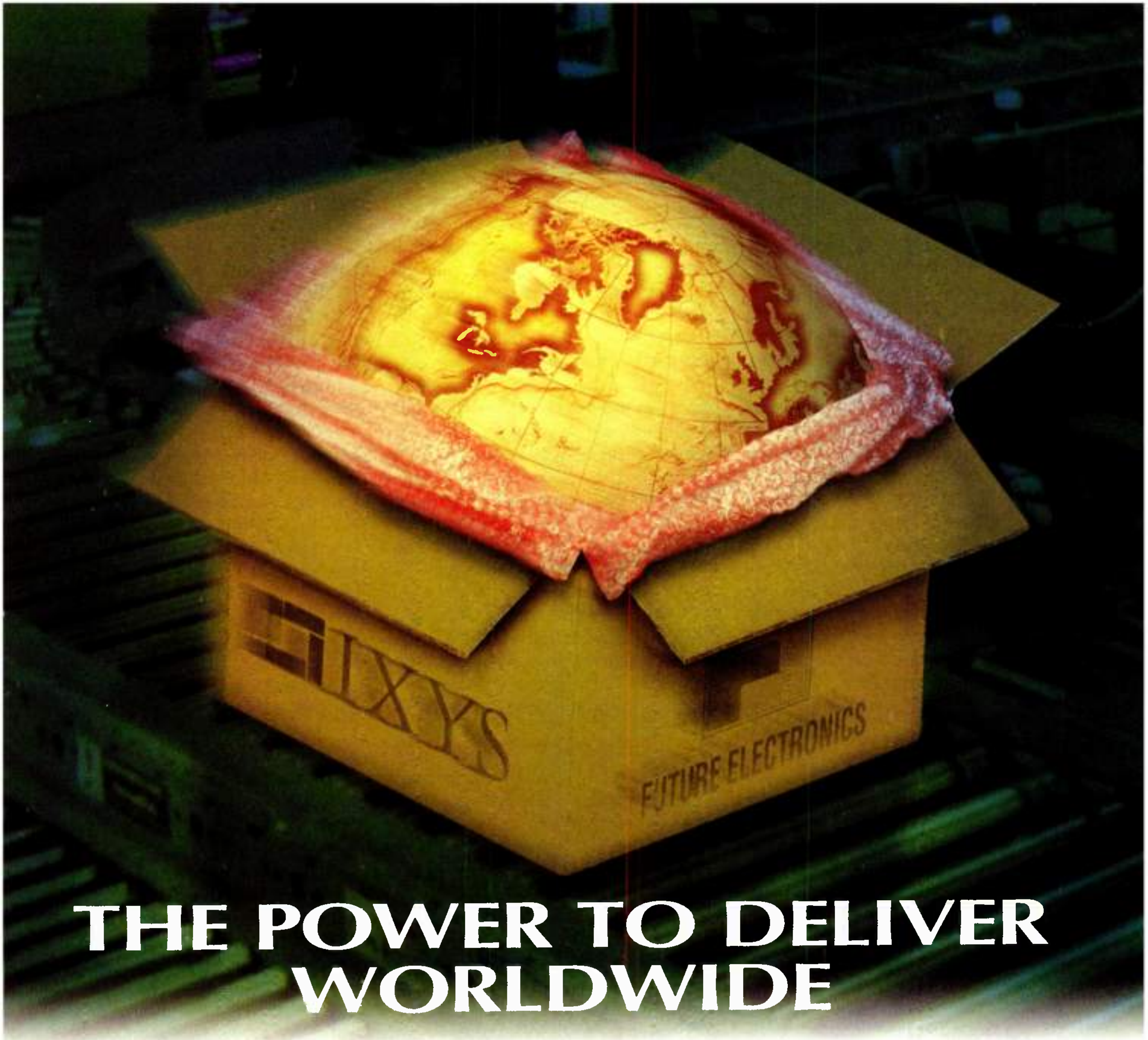

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Despite the potential for political roadblocks and marketing wars in an effort with so many factions, UMTS has made surprising progress, thanks in part to a carefully crafted patent-pooling agreement between all participants.

Over on the Pacific rim, there also has been much activity. Oki Semiconductor pioneered many wide-band CDMA (W-CDMA) concepts with its IS-665 standard. Developed in 1993/94, it never really caught on except for wireless local loop (WLL) applications. Nevertheless, the concepts it championed formed the basis for much of the W-CDMA technology that went into Nippon Telephone & Telegraph's (NTT's) current 3G standard.

Employing a hybrid FDD/TDD air interface, a Gold code-spreading sequence, and a variable-length spreading sequence (to speed initial synchronization), the NTT proposal represented an ambitious bit to assume technical leadership in the wireless market.

U.S. 3G activities also have been underway for several years, under the aegis of ANSI's T1/E1 committee. While there has been active participation by many groups, the effort appears to have been dominated by Qualcomm and the IS-95 standard that it helped to develop. In the end, it appears that the ANSI's CDMA1 3G plan will be built as a direct extension of current IS-95 CDMA technology. Qualcomm seems to have used its influence to structure the ANSI CDMA1 standard to help maintain its market majority position and near-monopoly on CDMA patents on North American digital cellular.

The CDMA1 standard is based on the IS-95B protocol, scheduled for roll-out before the turn of the century. It retains a chipping code and modulation scheme similar to those used in the current IS-95A standard, but gives it wider bandwidth and an expanded feature set. While not as ambitious as the UMTS plan, it supports things like direct data connections (no modem required), messaging, and support for IP-based services. While each CDMA1 channel only supports 14.4 kbits/s worth of data, the IS-95B protocol allows a user to aggregate up to eight channels into a single link of 115.2 kbits/s.

Deja Vu Averted

What seemed like an inevitable collision between giants has been, at least in part, averted. This past January, Europe's ETSI and Japan's NTT/DoCoMo alliance reached an agreement to harmonize their two standards efforts. As of this writing, only a few details remain to be cleared up before a true interoperable specification is achieved.

At this time, the agreement splits the 1885- to 2200-MHz 3G band into seven segments. Spectrum is assigned for both basic CDMA services, and a hybrid time-division CDMA (T/CDMA) service. T/CDMA was developed to optimize bandwidth usage and promote easy implementation of asymmetric connections for applications like web browsing (*see "A European perspective*

(continued from page 72)

single user for traffic in either direction. This bandwidth-on-demand feature could allow a TD-CDMA base station to provide high-bandwidth, asymmetric service for web surfing and other downlink-intensive applications. This remains to be seen, since there are doubts that CDMA can be efficiently adapted to a TDD environment.

As a result, TD-CDMA is to be used for TDD applications in "closed" environments. At the announcement, this was described as "unlicensed applications" such as business and domestic cordless PBX, phones and local area networks, although there may be other opportunities for public commercial applications at a future date.

The other technical rationalization relates to power control and the need for spectrum management. It is said that TD-CDMA will not require spectrum management so there will be no restriction on fixed base-station siting. TD-CDMA's advocates claim that it can operate with "open loop" power control, whereas W-CDMA needs a closed loop. This also is significant in base-station siting. The upshot of these developments is that there also is now a requirement for the development of low-cost multistandard mobile terminals—including the ability to work with all GSM standards—at 900, 1800 and 1900 MHz, as well as with TD-CDMA and W-CDMA. The terminal manufacturers say they don't see this as being difficult to achieve by 2002.

Indeed, Alistair Urie, Director of Product Strategy for Alcatel says that more time and effort is required by the marketing people to decide which combinations to include that it does for the engineers to make them. This does, however, place more emphasis on the "software" radio concept. The rationale for this approach is that it will allow a variety of mobile terminals to be sold with varying capabilities. Much like a wide range of cameras that all use standard film cartridges, consumers will be able to purchase anything from a simple voice-only handset, to a full-blown wireless multimedia workstation, and they will all be able to utilize the same network infrastructure.

Underlying all this is the fundamental requirement to protect investments in GSM. As a result, both Japanese and Europeans will adopt an "evolved" GSM architecture for the core network. No formal decisions on this have yet been made, although NTT DoCoMo have stated emphatically that this is what they want to do. Most of the Europeans also want this.

Finally, the need for GSM compatibility raises two other issues. First, they are all now working to specify that data structures and protocols of the new UTRA technologies are backwards compatible with GSM. For example, the TDMA frame in TD-CDMA has been carefully chosen to have the same timing as GSM, while CDMA chip code lengths for W-CDMA will be multiples of those for the CDMA element of TD-CDMA, and so on.

Although this looks like a European-Japanese "club," some care has been taken to ensure that North America isn't excluded. For example, they are very keen that Qualcomm (a member of ETSI) is on board—basically, they are interested in some CDMA power control technology that makes Qualcomm sought after as a partner in the whole thing. Next, there is a clearly stated requirement that the new air interface standards are formulated so that they can be used where spectrum is limited to 2 X 5 MHz. This was included at the specific request of the U.S.-based participants.

Contributed by Peter Fletcher, Electronic Design's European correspondent based in London, England.

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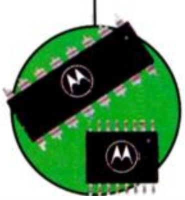

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on 3rd-generation wireless technology and politics," p 72).

Despite its fairly entrenched position, the U.S. may even be moving toward some type of compromise that would allow North American 3G equipment communicate with the rest of the world. In a recent interview with Qualcomm's vice president of Global Standards, Anil Kripalani emphatically stated that Qualcomm was working toward some level of interoperability between the UMTS and CDMA1 standards. Among other efforts, Kripalani says that there are efforts to find a resolution to the timing problems caused by the different frame lengths (20 ms in the U.S., 10 ms in Europe) used by the two systems. He also cites recent tests being conducted in England to develop a way to pass voice traffic between MSCs (mobile service carriers) using the U.S. ANSI 41 and European MAP air interface protocols.

It's Not Just About Roaming

While some of these activities might be political maneuvering, there are still hopeful signs of progress toward a global interoperability agreement. Although far fewer than 5% of wireless subscribers are expected to need intercontinental roaming capability, global interoperability is a critical element in the success of a 3G system. Taking a lesson from the computer industry, the wireless world must embrace open standards and liberal technology cross-licensing policies to insure a broad user base and to drive the cost of their equipment down. Should the U.S. cling to proprietary technologies while the rest of the world embraces the ETSI/DoCoMo standard, America may find itself saddled with handsets and an infrastructure that will be priced out of line with other 3G products being used and produced on a global basis.

Still, another ray of hope for U.S. interests might lie in evolving the IS-136 TDMA standard toward interoperability with a future generation of the TDMA-based GSM cellular network. The Universal Wireless Communications Consortium, Bellevue, Wash., has just released its UWC-136 proposal. Supported by Ericsson, AT&T Wireless Services,, and others, UWC will not be interoperable with CDMA-based technologies in the near future, but may at least provide something other than a "forklift upgrade" solution for carriers with TDMA-based 2G infrastructures who desire some level of international compatibility.

UWC-136 claims to be a 100% pure TDMA digital solution that provides an evolutionary path to the next generation from IS-136 to IS-136+ to IS-136HS (the high-speed component of UWC-136). IS-136+ will provide extremely high-fidelity voice services and higher-rate packet-data services, up to 43.2 kbits/s in the existing 30-kHz bandwidth. IS-136HS provides user-data rates up to 384 kbits/s for wide area coverage in all environments and faster than 2 Mbits/s for in-building coverage. Boasting high spectral efficiency, UWC-136 enables carriers to implement 3G services in stages. This could have great appeal to many incumbent carriers with large bases of installed infrastructure.

Advanced Services

Putting protocols, politics, and posturing aside, what might a 3G service look like? How would it differ from today's digital cellular/PCS services? Much of this is still up for grabs, but we

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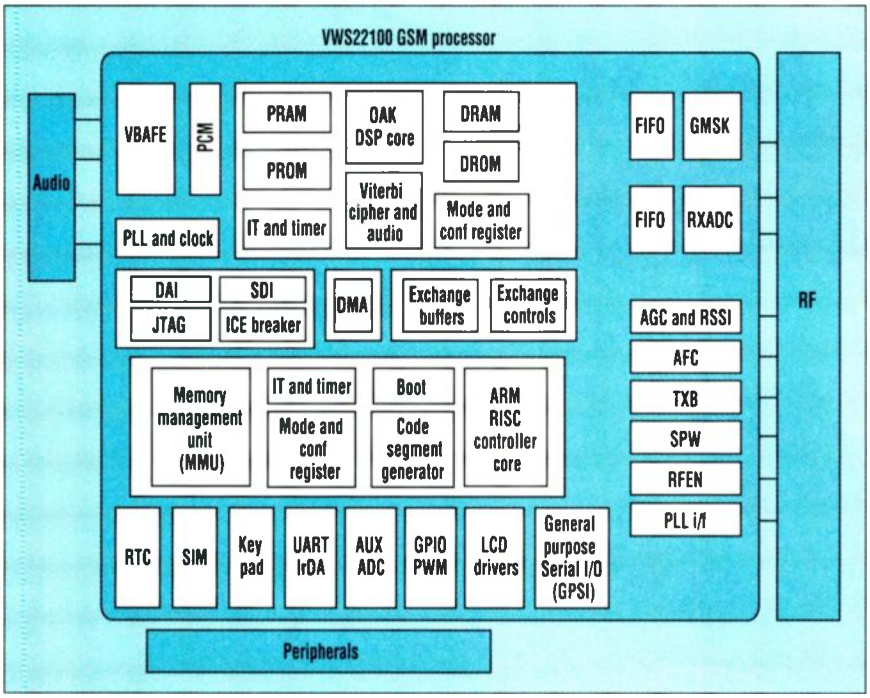


3. Communication-oriented ASICs will probably play a large role in 3G handset design, much like this 2G GSM processor from VLSI Logic. To support next-generation increased bandwidths and sophisticated protocols, ASIC manufacturers will have to develop faster, smarter processor cores for their cell libraries.

can make some educated prognostications. Besides the obvious high-speed data capabilities, the most striking differences between 2G and 3G systems will be in their flexibility. If the ETSI/NTT concept of decoupling the network from its services works out, we can expect to see a much more entrepreneurial environment where both cellular networks and third-party providers can quickly develop a wide variety of custom functions tailored to individual needs.

During his keynote address at the Wireless Symposium and Exposition, Christian Dupont, Texas Instrument's (TI's) wireless communications business group director, expressed his enthusiasm for the possibilities a 3G wireless network created.

At a minimum, Dupont said a 3G handset could behave like a cordless phone at home, a wireless PBX handset at work, and a cellular unit when on the road. He foresees the day when flexible hardware and software platforms will enable us to download new applications onto phones. These might include medical imaging programs, database search engines, specialized messaging services, or even AI-based Web agents that autonomously prospect, mine, and refine data from the Internet and deliver summaries to your phone's screen. Travelers could access navigation and information services from their phone either for a small fee or from sites that rely on advertising revenues.

The incredible diversity of services described by Dupont would be made possible by the "soft phone" concept. In this scenario, the heart of a 3G handset would be a powerful DSP, possibly working in conjunction with an embedded RISC engine. The surplus processing power available in these chips would make it possible to run downloadable applications on a "virtual Java engine." TI has already licensed Java and is well along in developing a practical architecture that would support 3G services.

Soft phones are an attractive idea being pursued by many parties, including software development companies. There are already several multiplatform 2G handset software packages, such the ones from Telogy Networks, Germantown, Md., capable of supporting IS-95, IS-136, or GSM functionality *(Fig. 2)*. They enable designers to implement a nearly turnkey solution for a variety of DSP and controller combinations. The next generation of software packages may enable multiprotocol phones, providing the phone's transceiver is capable of handling the RF.

Nuts And Volts

Since the standards are still in the process of being finalized, there are many uncertainties about what will be required of a 3G phone chip set. This places semiconductor makers in the unenviable position of having to begin designs ahead of a firm standard. For this reason, we can expect to see highly programmable solutions and lower levels of integration for the next couple of years. Despite the uncertainty, there are several areas in which designers can safely make assumptions to help them begin the difficult task of delivering working 3G silicon on a timely basis.

Third-generation handsets will de-

EUROPEAN/JAPANESE UMTS SPECTRUM ALLOCATIONS (IN MHz)

Segment 1	1885-1900	TDD nonpaired. Unusable in Europe (used for DECT).	(15 MHz)
Segment 2	1900-1920	TDD nonpaired. Used for TD-CDMA service.	(20 MHz)
Segment 3	1920-2080	FDD Used for WCDMA service, paired with Segment 6 for wide area mobile services.	(60 MHz x 2)
Segment 4	1980-2010	FDD paired with Segment 7 for mobile satellite service.	(30 MHz x 2)
Segment 5	2010-2025	TDD nonpaired. Used for TD-CDMA service.	(20 MHz)
Segment 6	2110-2170	FDD - paired with Segment 3.	
Segment 7	2170-2200	FDD - paired with Segment 4.	

TDD = Time division duplex.
FDD = Frequency division duplex.

mand new levels of performance from their RF sections, according to Hans Dropmann, marketing manager for Maxim Corp., Sunnyvale, Calif. To meet the wider bandwidth, increased linearity, and lower power requirements, he expects that companies like Maxim will need to focus on delivering parts using high-speed-low-noise bipolar processes, such as GaAs and SiGe. One of the main challenges will be in the mixed-signal area, such as analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) that will have to operate at 10+ Msamples/s. Another critical area Maxim will concentrate on for its 3G products will be to reduce the number and size of the external passive devices used for filtering and coupling functions.

External passives also are on the mind of Brent Dietz , wireless product manager for Harris Semiconductor, Melbourne, Fla. In his view, nontraditional RF architectures will find a home in 3G handsets. While Dietz feels that some sort of sub-sampled zero-IF receiver would be an optimum solution, he says that one of the great challenges will be accommodating the variable carrier bandwidths employed by most bandwidth aggregation schemes.

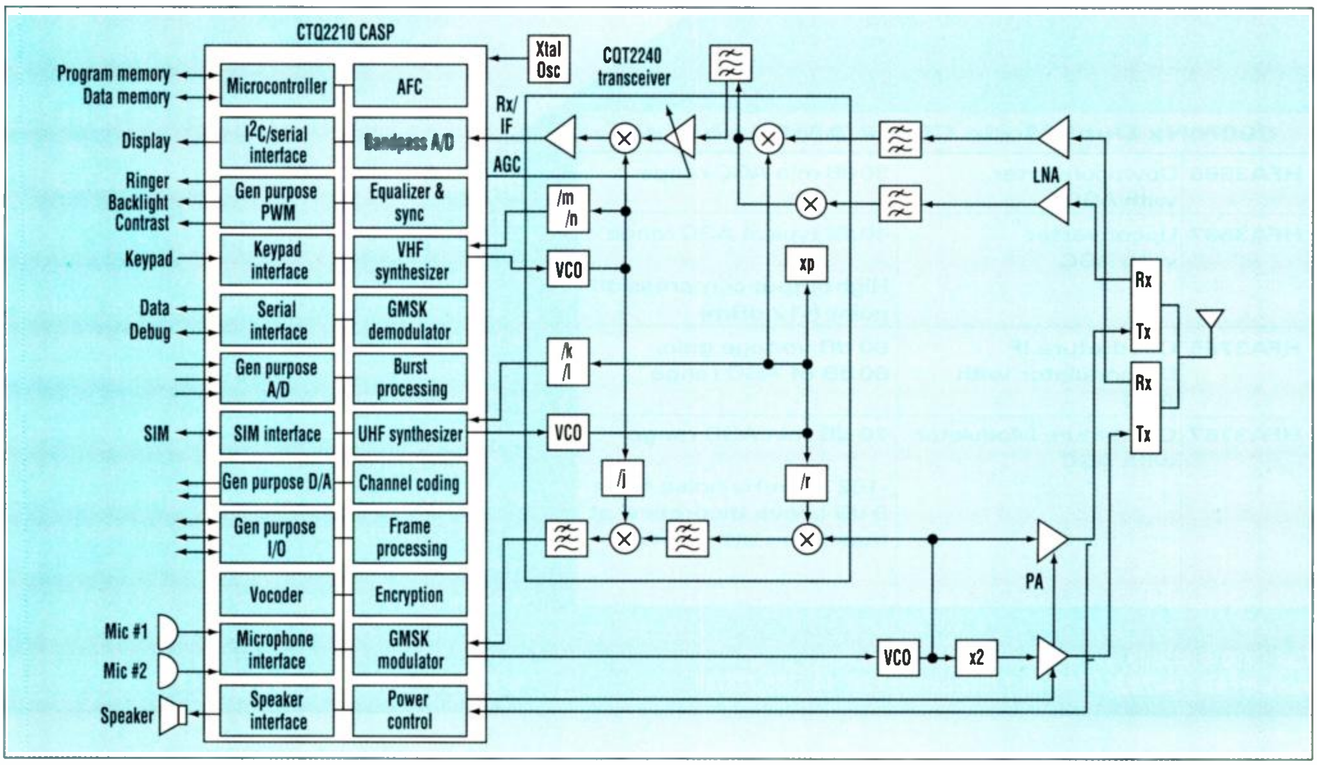
Placing the ADC stage at the IF will not work well for variable bandwidth since the SAW filters traditionally employed for filtering have fixed frequencies and bandwidths. This wouldnecessitate moving the ADC right to the antenna. While impractical today, authorities at Harris feel that such a radio will be made possible using submicron line widths and their newly acquired high-speed SiGe technology.

Andrew Burt, marketing manager of Mitel's cellular product division (formerly GEC Plessey), Scotts Valley, Calif., concurs with Harris that this will force designers to explore unconventional radio architectures, such as digital oversampling direct-conversion receivers. These radios would move digitization of signals much closer to the antenna, enabling designers to use programmable DSPs or other configurable logic to perform demodulation and decoding tasks

Burt also thinks that one of the ironclad requirements for 3G handsets is that they will have to be backwards-compatible with existing technologies, allowing them to use 2G GSM or IS-95 cellular networks when they can't connect with a 3G service. Since air interface schemes will be in flux for some time, splitting the transmit and receive RF functions across two chips will also ease development of the first chip sets.

Given a 15-MHz carrier signal, Burt's thumbnail calculations place the sampling speed of such a radio at around 80 MHz. Assuming it takes around 60 MIPS worth of DSP to support a typical GSM phone, and around 80 MIPS for an IS-95 handset, he estimates that a 3G WCDMA phone will require a 300-MIPS processor to perform its channel coding/decoding tasks. For this reason, Mitel and many other wireless players are concentrating on developing baseband processors that will be able to handle this quantum leap in throughput. Burt suggests that the next generation of low-power DSPs will be able to supply around 150 of the needed MIPS, leaving the most repetitive and compute-intensive tasks (Viterbi processing and voice codecs among others) to dedicated ASIC logic.

Many ASIC manufacturers, like VLSI Technologies, San Jose, Calif. and LSI Logic, Milpitas, Calif., are already gearing up for the 3G wave. They are acquiring new, more powerful processors and creating libraries of functional cells



4. A distributed array architecture may be an extremely efficient way to meet the need for the quantum leap in signal processing and control functionality required to function in broadband 3G networks. A current example is CommQuest's flexible distributed processor used to build this 2-chip, dual-mode, cellular phone, capable of communicating on the 900-, 1800-, and 1900-MHz bands.

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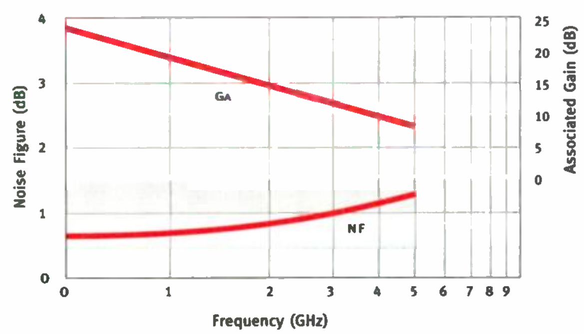

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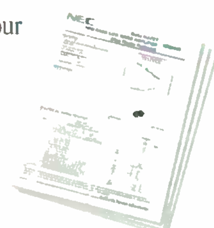

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that will form the basis for both custom and merchant 3G phone chip sets. Much like their 2G chips *(Fig. 3)*, they will have an embedded DSP and RISC controller, surrounded by a sea of specialized logic that reduces glue logic and other external components *(Fig. 1, again)*. The quick turnaround afforded by the vast libraries of cells and software will help manufacturers develop products quickly, and to adjust them to evolving standards and market demands.

While most semiconductor makers are placing their faith in a single massive DSP to perform 3G tasks, at least one contrarian viewpoint is making a very compelling argument for a distributed processing architecture. CommQuest Technologies, Encinitas, Calif., has enjoyed considerable success with its CASP architecture which places an array of specialized controllers and signal-processing logic blocks on a single chip *(Fig. 4)*. The functional blocks communicate with each other over a high-speed intra-chip data bus, passing data and intermediate results back and forth until they become audio waves bound for the handset speaker or analog IF to the single-chip RF section.

CommQuest feels that it takes fewer gates and less power to implement many key wireless functions in dedicated logic. Along with their recently acquired SiGe technology, this may enable them to deliver very cost and power-effective 3G chip sets. Since there are both fixed and programmable processors available in the CASP library, it is quite conceivable that they also will support downloadable functions.

Gen 2.5?

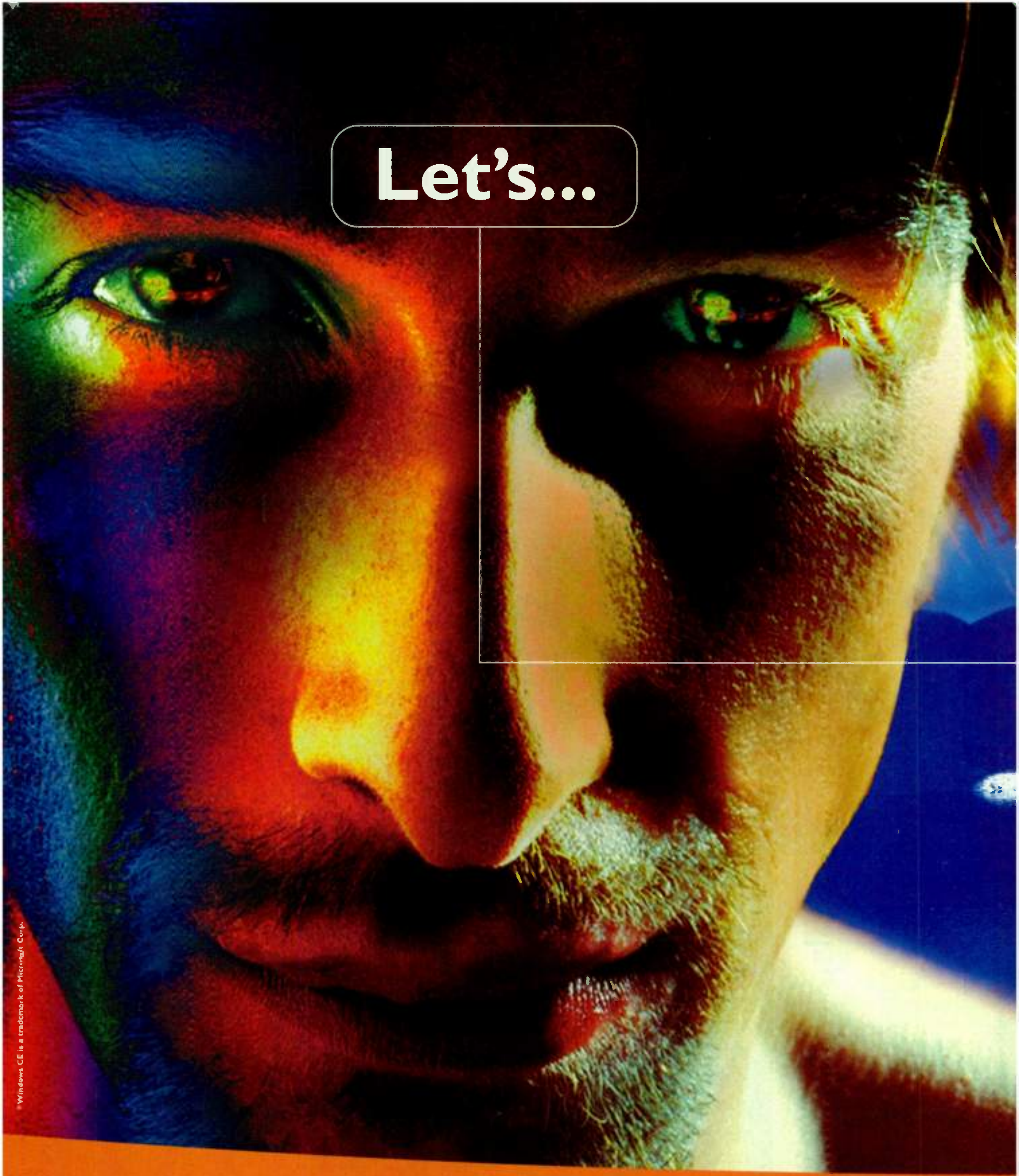
Given the fact that 2G digital wireless systems are not yet fully deployed, let alone paid for, many people are justifiably dubious about whether there is sufficient demand for 3G systems. Despite their many advantages and opportunities, it will be hard to get entrepreneurs to risk rolling out a wideband wireless network in the near future. One strategy finding increasing favor within the wireless community is to implement a limited subset of advanced features over existing infrastructures and air interfaces. It is hoped that they will stimulate the expectations of a bandwidth-hungry public and create a bottoms-up demand for the services that only a 3G system can offer.

For example, Mr. Dupont places this "pull" strategy at the core of TI's plans for delivering 3G. Embracing the 3G philosophy of open-ended network capabilities, Dupont avoids defining a "killer app" for 2.5G phones. Instead, he envisions many specialized applications being developed for Java phones which don't require the enormous gobs of bandwidth that their 3G successors will consume. Simple, handy applications, such as map services, financial data delivery systems, weather information, and stock market tracking could all be implemented by content providers using the bandwidth available in today's networks. Dupont speculates, however, that we won't really know what the most important applications will be until we stumble over them.

Clay Karmel, product development manager for Sony Wireless, San Diego, Calif., feels that things like web browsing and e-mail will increase demand for bandwidth, but will not offer manufacturers a way to differentiate a product or a compelling reason to move to a 3G phone. Karmel predicts that when phones can provide local-area navigation and help people find resources within a particular neighborhood, they will begin to realize their potential.

He also notes that Sony expects that transmission of images, and eventually video also will be the sorts of things that will drive people to use their phones in radically different ways. Fortunately, we won't have to wait for a 3G system to experience phone-top photography. A 64-kbyte JPEG image of your kids or favorite pet can be uploaded to your web page across a standard 14.4-kbit/s line in less than a minute. As the IS-707 specification is incorporated into the next upgrade of the IS-95 CDMA standard over the next year or so, subscribers will be able to transmit images and data over either circuit switched or packet switched data sub-channels, making these services faster and less expensive. Ultimately, however, Karmel expects that subscriber demand for higher bandwidth should drive network operators to transition to 3G systems.

Although the next few years will witness turmoil as competing factions vie for dominance, we can still have hope for the shining promise of a truly global wireless network. Like many things, its realization or failure will depend as much on politics and business as technology. Stay tuned for the latest developments.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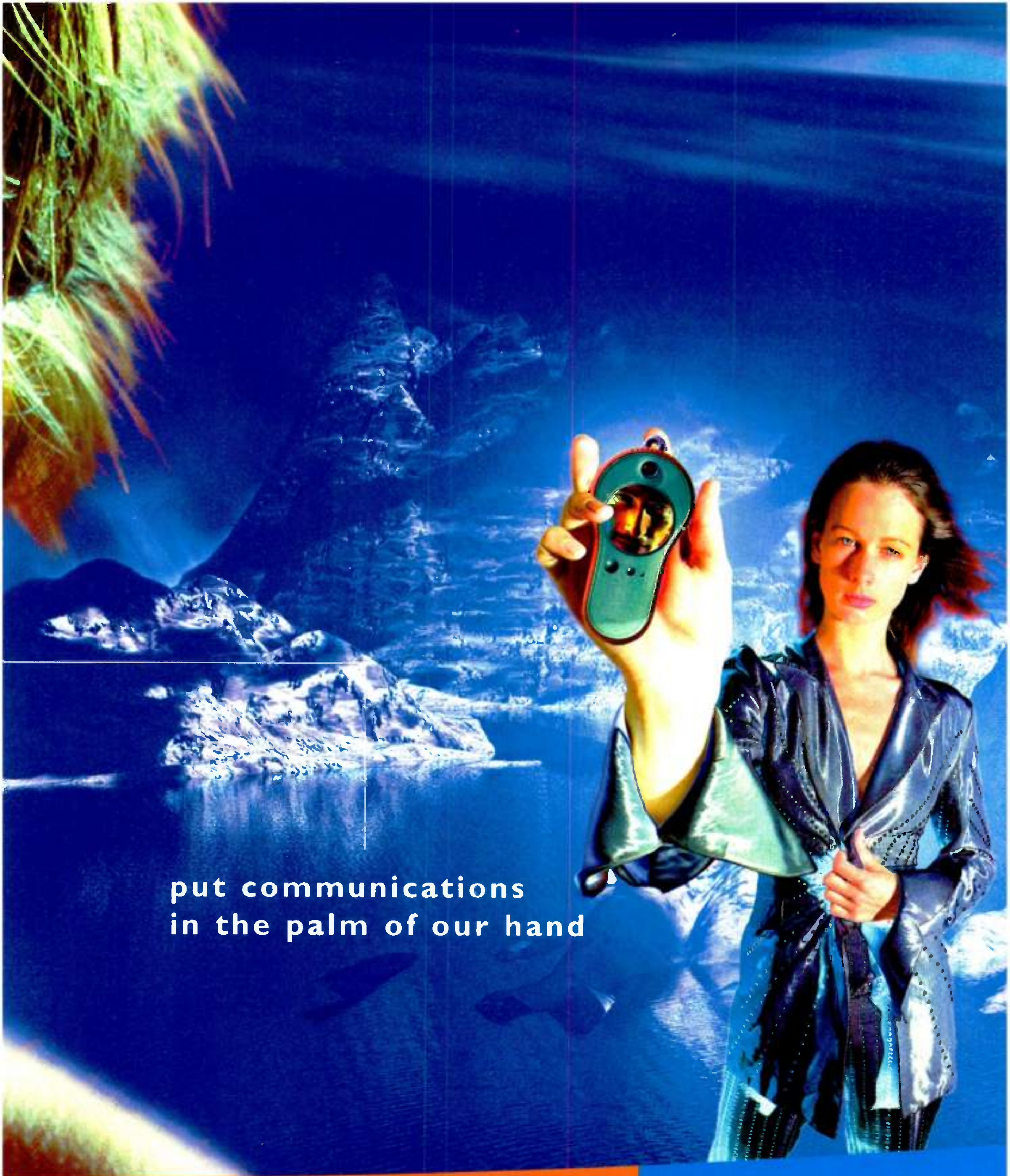
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A highly integrated chip set and its associated set of development tools will soon enable manufacturers to quickly design and produce full-featured SDH access equipment at prices similar to current T1/E1 PDH-type products. By putting 150-Mbit/s devices into the market at close to the cost of 1.5-Mbit products could help telcos overcome their chronic shortage of bandwidth close to the local loop. Supplying increased bandwidth will also be a key factor in driving backbone-level bandwidth into lower-tier services, such as Internet service providers and CLECs.

The two-chip set can be used to implement E1 multiplexers at STM-0 (51 Mbit/s) and STM-1 (155 Mbit/s) rates in SDH terminal and add/drop multiplexers. This would be well-suited for radio and fiber applications such as Digital Cross-Connect Sys-

tems (DCCS), Next Generation Digital Loop Carriers (NGDLC), and STM-0/STM-1 point-to-point radios. With a single mapper processing 21 E1 signals and its 3.3-V core, the chip set offers the highest level of integration and the lowest power consumption of any solution available on the market today.

Consisting of the SXT 6051, an overhead terminator, and the SXT 6251 (an asynchronous 21 channel E1 mapper), the chip set was designed for fiber and radio applications. All alarms and overhead bytes are processed internally to counteract the effects of errors occurring in wireless transmission systems. All overhead is processed on the chip, eliminating the need for a digital signal processor on the board. The industry-standard Telecom Bus interface allows for easy and flexible interconnections.

The SXT 6051 overhead terminator provides regenerator and multiplexer section termination and high-order path termination in STM-0 and STM-1 multiplexers. It implements highly configurable architecture with extensive on-chip alarm detection and performance monitoring capabilities. When it is combined with the SXT 6251 (21 E1 mapper), the overhead terminator creates a complete solution for a 21 E1 or a 63 E1 multi-

(continued on page 90)

PRODUCT FEATURE

(continued from page 88)

plexer. The SXT 6251 complies with the ITU's 1+1 protection switching and is versatile enough to be configured as either a repeater, a terminal multiplexer (main or slave) or an add/drop multiplexer (main or slave).

The SXT 6251 E1 mapper asynchronously maps and demaps 21 E1 PDH signals into the SDH format. The PDH side interfaces with E1 LIU or standard E1 framers via NRZ clock and data, while the SDH side uses a standard Telecom Bus interface. The companion SXT 6051 overhead terminator chip completes the signal processing, creating the final STM-0 or STM-1 signal. One mapper can process 21 E1s into STM-0, while three mappers can process 63 E1s into an STM-1 stream.

The SDH chip set is backed by software support, reference designs, and technical and architecture expertise. The CANDO software provides a PC-graphical user interface (GUI) to access the functions of the chip set. The CANDO software easily interfaces with the customers' development system and speeds up design verification by allowing the designer to set up the chip set's different configurations (STM-0/STM-1, repeater/terminal/add-drop, main/slave, etc.). It also can be used to help the designer understand the implementation of the latest ITU-T specifications in the SDH chip set.

The SXT 6051 and SXT 6251 meet the latest specifications of ITU G703, G707, G782, and G783. The SXT 6051 complies with Bellcore TR, NWT. 000253, ANSI T1.105 SONET specifications, and Bellcore TRTSY 00842.

Both chips, in 208 PQFP packaging, operate within the extended temperature range of -40 to +85°C. In quantities of 1000, the SXT 6051 is priced at \$83 and the SXT 6251 is priced at \$131. They're available in volume quantities.

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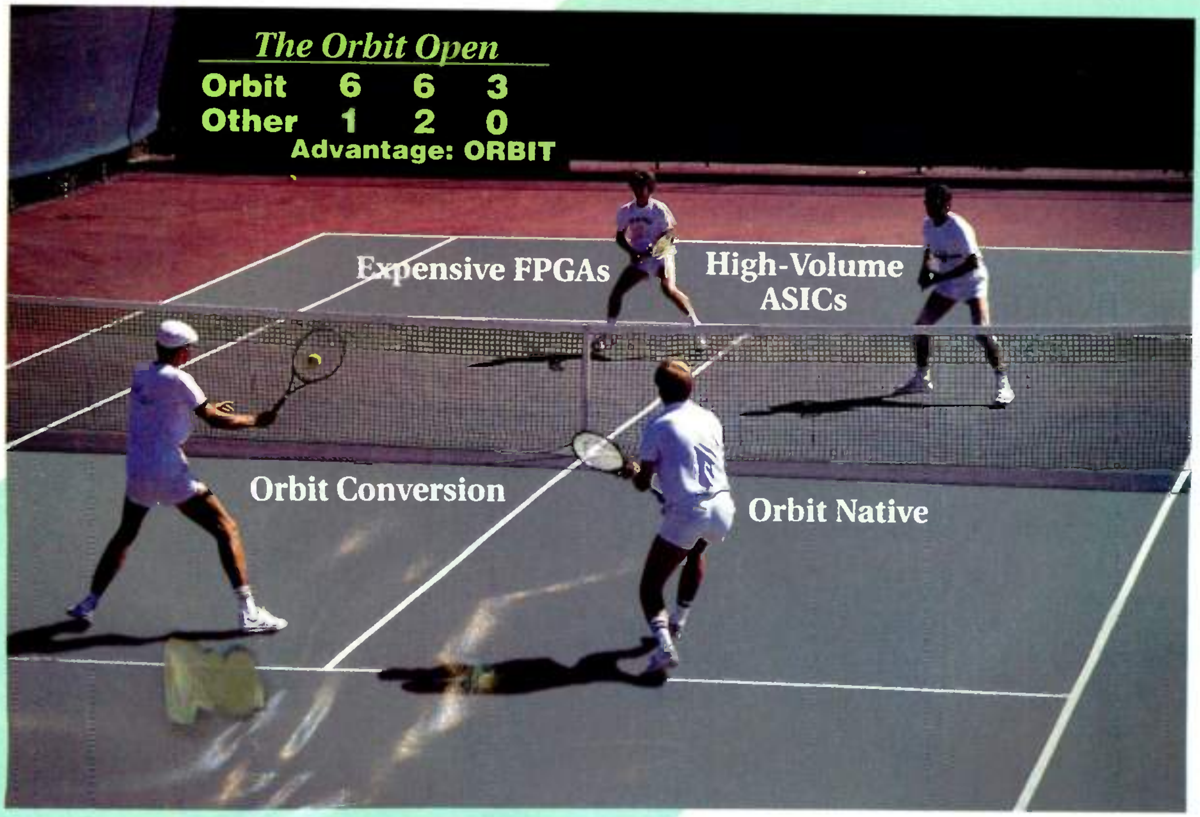

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READER SERVICE 163

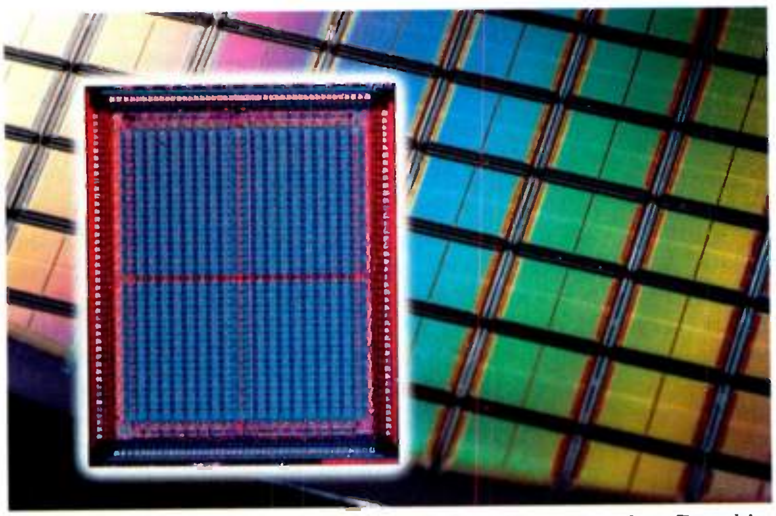
High-Density FPGAs Go Toe-To-Toe With Gate Arrays

Featuring Capacities Of 250 kgates And More, The Latest Round Of FPGAs Deliver Performance And Density Levels Rivaling Mainstream Gate Arrays.

Dave Bursky

SPECIAL REPORT

The age-old battle of "mine is better than yours" continues to rage in the ASIC market when it comes to deciding whether to use gate arrays or field-programmable logic devices to implement a design. Many factors are fueling the fire—FPGAs and CPLDs are becoming denser, faster, and less expensive as process fabrication dimensions shrink from 0.5 to 0.35 to 0.25 and eventually to 0.18 µm. Programmable-logic design tools and libraries are improving, permitting more efficient use of the logic and improved placement and routing for higher operating speeds. At the same time, advances in gate-array technology for chips with less than 500 kgates have slowed down. Most new efforts are concentrating on developing megagate-density products for system-on-a-chip designs.



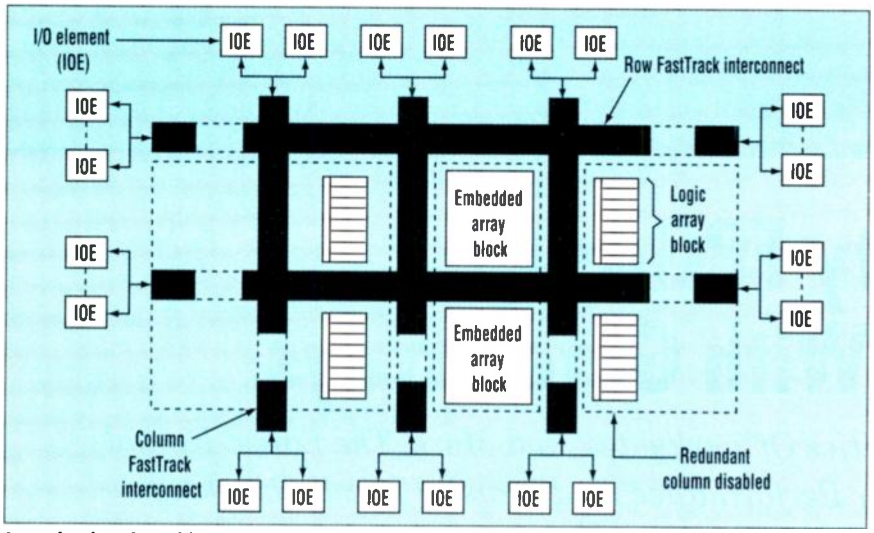
Art Courtesy: Actel

Even while gate arrays and programmable products compete at one level, they complement each other at another. Most designers acknowledge that CPLDs and FPGAs are great solutions for prototyping and low-volume production, but they often consider switching to some type of mask-programmed solution to lower costs for high-volume production. Many FPGA suppliers offer hardwired versions of the programmable chips (such as the XH3 series from Xilinx for its SC4000 and SC5000 FPGAs), yet non-FPGA suppliers also can partake in the action. For instance, gate-array vendors have played right into that area by offering conversion services and tools that ease the conversion from programmable device to gate array *(see "ASIC Alternatives," p. 97).*

The higher densities of today's FPGAs—top capacities of 250 kgates are being sampled while one-million-gate devices are on the drawing boards—basically require that the same tools and design approaches used for gate arrays be applied for FPGAs. No longer are designs done at the schematic level by connecting gate after gate to form basic functions. Rather, designers who use FPGAs and large CPLDs can now leverage basic logic-function design libraries, compilers, large blocks of intellectual property (IP), logic synthesis software, and other tools that are comparable to the tools used by designers of gate-array-based logic.

The growing popularity of these tools is driven by one key factor: time to market. By taking advantage of libraries of basic functions (counters, multiplexers, etc.) as well as compilers to generate multibit versions of the circuits, designers can get a jump start. Using larger blocks of IP—microprocessor and DSP cores, PCI interfaces, and many other functions developed by programmable-logic suppliers and third-party suppliers—greatly boosts productivity. Such IP blocks are typically either licensed by their respective developing companies to the logic chip suppliers, or are offered for independent licensing to the company designing the ASIC.

As a result, the typical design flow for systems



1. Redundant logic blocks were included in the architecture of Altera's FLEX 10KE family. Just as with memory chips that employ redundancy to improve chip yield, the redundant logic columns can be enabled when a column of logic cells is put out of commission by a manufacturing defect and then disabled.

based on gate arrays or on large programmable logic devices should be very similar. That will facilitate the designer's job. And, with the range of high-density FPGAs and CPLDs broader than ever, designers have a wide range of densities and architectures to select from.

At the high end are Altera, DynaChip, GateField, Lucent, and Xilinx. They offer families based on 0.25- or 0.35-µm design rules that can deliver top capacities of between 105 to 250 kgates. Of course, each family has a range of chips, with the smallest devices providing capacities of as little as a few thousand gates. Such lower-density devices (5 to 100 kgates) will compete not only with each other, but with programmable-logic families from Actel, Atmel, Lattice, Motorola, QuickLogic, and Vantis, which offer devices with capacities of up to about 50 kgates.

Turning The Strikes Into Hits

Large programmable devices have typically had three strikes against them: They've been expensive (often 10 times or more the cost of gate arrays), relatively slow (one-third to one-fourth the speed of gate arrays), and much harder to place and route than gate arrays to meet desired performance goals. However, the latest-generation programmable devices have done away with the last two strikes: The chips internally operate at 250 MHz and can be placed and routed using timing-driven tools to maximize performance. Because companies are working hard to reduce costs by shrinking the chip area, they can drop chip prices to levels competitive with gate arrays (typically two to three times the cost, since programmable devices don't have overheads associated with gate arrays).

How these tools are being enhanced can be seen through an alliance struck between Altera and Exemplar in the APEX program (Altera Partnership with EXemplar). It will focus on developing and marketing advanced design software and methodologies for next-generation Altera PLDs. By working together, the companies hope to create new ways to enhance the integration of Exemplar's synthesis and place-and-route tools with Altera's MAX+PLUS II development software.

In another partnership, this time with Synplicity, Altera hopes to create superior synthesis and high-level design methodologies to both speed development and minimize the time spent optimizing the design. The effort will focus on the optimization between Synplicity's synthesis engine, Synplify, and Altera's MAX+PLUS II software. Improvements will focus on floorplanning, timing constraints and analysis, integration of megafunctions, and libraries of parametrized modules, as well as the quality of results for design implementation.

Silicon improvements also will be crucial for tackling designs that previously were only the domain of gate arrays. For instance, the latest FLEX 10KE family devices designed by Altera provide gate capacities from 30,000 to 250,000 gates, can operate in systems with bus speeds of 66 to 70 MHz, and internally can run at speeds of up to 250 MHz. With such performance, the programmable chips can be used in systems including 100-Mbit and 1-Gbit Ethernet subsystems, advanced graphics port (AGP) or peripheral component interconnect (PCI) interfaces, and others.

To achieve the speed and density, designers at Altera started with their latest 0.25-µm, five-level metal process and were able to craft chips that have abundant routing resources that don't occup valuable silicon area but rather are po tioned in the space above the silico That allows the spacing between tra sistors to be kept to a minimum, redu ing chip area by as much as 40% versu the company's FLEX 10KA family.

Because the logic core operates from 2.5 V, internal power consumption is low, enabling higher packing density as well. To support any external system interface, the arrays also include the company's MultiVolt I/O structure, which allows I/O pins to be configured for 2.5-, 3.3-, or 5-V systems.

Included with the logic gates are dedicated blocks of dual-port RAM—24 kbits on the 30-kgate chip, increasing to 80 kbits on the 250-kgate device, which is about double the amount included in the previous FLEX 10K series. The combination of high-densi logic and dedicated memory, along wi from 246 to 470 user I/O pads, mak the FLEX 10KE family competiti versus gate arrays.

Since the programmable devic have many features akin to memory ar rays, designers at Altera have included redundant columns of logic on the chips. Therefore, if a defect causes one column to not respond, the defective column can be disabled and a spare column switched in. This is very similar to how RAMs are repaired to improve device yield, thus further lowering chip cost *(Fig. 1)*.

Projected pricing for the 10KE d vices will be very competitive wit gate arrays as well. By the end of 199 the 30,000-gate chips will sell for abo $8 apiece, while the 100,000-gate devi cost about $30/unit in lots of 50,00

OP AMPS VIDEO & COMPARATORS **ANALOG DESIGN SOLUTIONS**

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NEW World's Lowest Power, 2-Cell, Rail-to-Rail I/O Op Amps

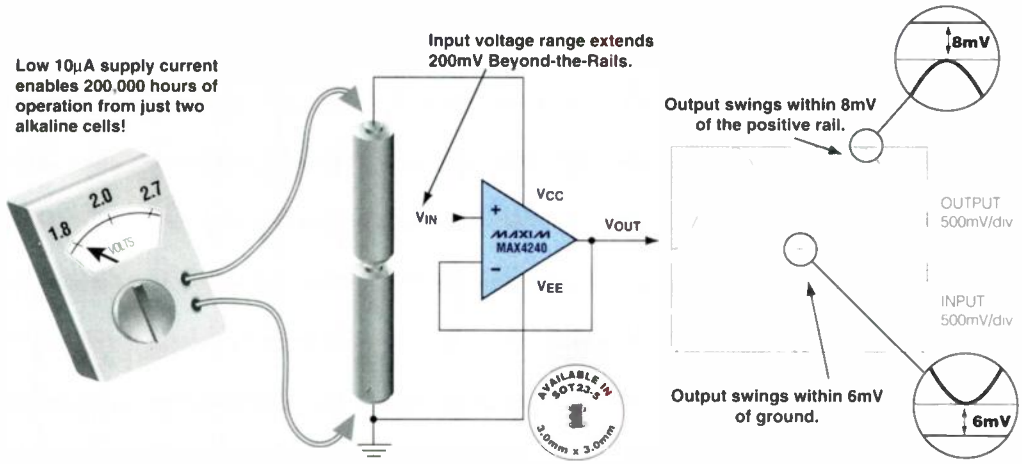
10µA Supply Current with Operation Down to 1.8V

SOT23-5 3.0mm x 3.0mm

Devices in Maxim's new MAX4240–MAX4244 family of Rail-to-Rail® I/O op amps are the first to guarantee single-supply operation down to 1.8V for only 10µA (12µA max) supply current. This combination of features makes these devices ideal for any 2-cell portable/battery-powered application. They have a 90kHz gain bandwidth and operate from a single +1.8V to +5.5V supply.

The MAX4240–MAX4244 outputs swing rail-to-rail and their input common-mode voltage range extends 200mV Beyond-the-Rails™. The MAX4241 and MAX4243 feature a shutdown mode that places the outputs in a high-impedance state and lowers the supply current to just 1µA per amplifier.

Low input offset voltage (250µV typical), low input bias current, and high open-loop gain suit these amplifiers for many low-power, low-voltage, precision applications. For space-critical applications the single MAX4240 comes in a tiny 5-pin SOT23 package.



ANALOG DESIGN SOLUTIONS

Choose Maxim for the Best Low-Voltage, Micropower Op Amps

Part	No. of Amps	Gain-Bandwidth Product (kHz)	Supply Voltage Range (V)	Max Supply Current per Amp (µA)	Low-Power Shutdown Mode	Beyond-the-Rails Inputs	Rail-to-Rail Outputs	Pin-Package
MAX4240	1	90	+1.8 to +5.5	12	—	Yes	Yes	5-pin SOT23
MAX4241	1	90	+1.8 to +5.5	12	Yes	Yes	Yes	8-pin SO/µMAX
MAX4242	2	90	+1.8 to +5.5	12	—	Yes	Yes	8-pin SO/µMAX
MAX4243	2	90	+1.8 to +5.5	12	Yes	Yes	Yes	14-pin SO, 10-pin µMAX
MAX4244	4	90	+1.8 to +5.5	12	—	Yes	Yes	14-pin SO

Beyond-the-Rails is a trademark of Maxim Integrated Products
Rail-to-Rail is a registered trademark of Nippon Motorola Ltd

MAXIM

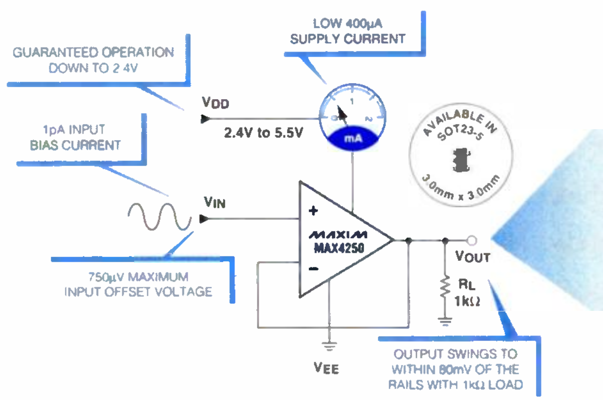
Spice Models Available

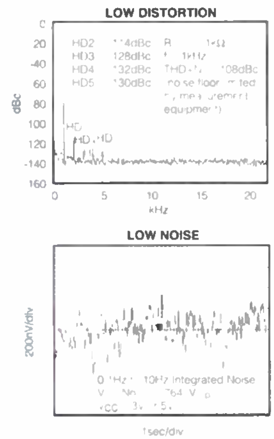
NEW

Lowest Distortion/Noise Op Amps Achieve -108dBc with Only 400µA

Operate Down to +2.4V, Available in SOT23-5

The MAX4249–MAX4257 single/dual/quad, low-power, single-supply op amps are ideal for any portable/battery-operated application that requires low noise and/or distortion. They achieve -108dBc total harmonic distortion plus noise (THD+N) while drawing only 400µA of quiescent supply current per amplifier. Furthermore, a low-power shutdown mode allows the MAX4249/MAX4251/MAX4253/MAX4256 to operate from only 0.5µA. The MAX4250–MAX4254 are unity-gain stable and deliver a 3MHz gain bandwidth, while the MAX4249 and MAX4255/MAX4256/MAX4257 are stable for gains of +10V/V or greater and have a 22MHz bandwidth. These devices are fully specified to operate from a single supply as low as +2.4V. Outputs swing rail-to-rail for this op amp family, and the input common-mode voltage range extends beyond ground. For space-sensitive applications, the single MAX4250/MAX4255 are available in a miniature 5-pin SOT23 package.

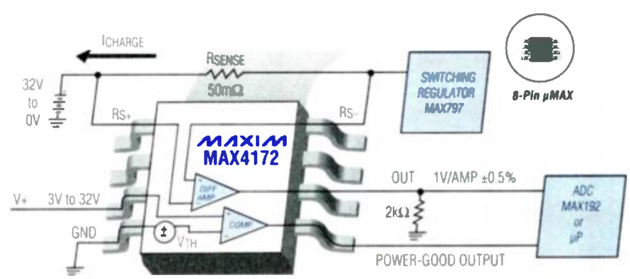




High-Side Current-Sense Amp Offers ±0.5% Accuracy Over Temp

Build a Low-Cost Battery Charger Using the MAX4172

High-side current measurement simplifies designs and offers higher precision than low-side sensing. The MAX4172 is the first low-cost, high-side current-sense amplifier for battery-powered equipment such as portable PCs and cellular phones. Unlike some battery chargers and "smart" batteries, the MAX4172 monitors current without disrupting the ground-return paths. Its wide bandwidth and ground-level-sensing capability make it ideal for use in closed-loop battery chargers.



The input common-mode voltage range is 0V to 32V regardless of the supply voltage, which ensures that the current-sense feedback remains viable even when connected to a battery in deep discharge. Measurement accuracy (full scale, over temperature) is typically ±0.5%.

The chip's open-collector power-good (PG) output indicates when the supply voltage has reached a level sufficient to guarantee proper internal operation. This new current-sense IC accepts supply voltages in the range 3V to 32V and is available in a space-saving µMAX package.

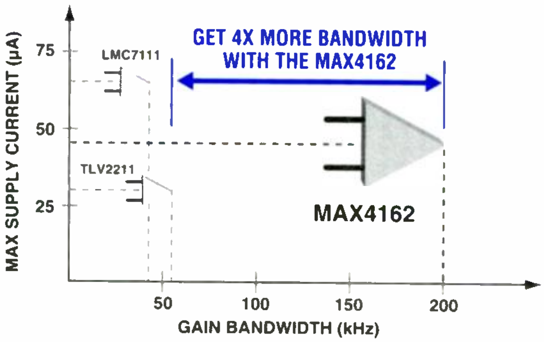
MAXIM

Spice Models Available

SOT23 Rail-to-Rail I/O Op Amps Provide 200kHz GBW with Only 25µA Supply Current

Single-Supply Operation Down to 2.7V

200kHz gain bandwidth, low power consumption, and a small footprint make the single/dual/quad MAX4162/MAX4163/MAX4164 an excellent choice for use in portable equipment and other low-power, single-supply applications. Maxim's new micropower, rail-to-rail I/O op amps achieve an exceptionally high bandwidth for their power consumption. The gain-bandwidth product is 200kHz and the quiescent supply current is only 25µA (40µA max) per amplifier.



These amplifiers are unity-gain stable for any capacitive load. The outputs swing to within 3mV of the rails (R_L = 100kΩ) and their input common-mode range extends 250mV Beyond-the-Rails. A proprietary internal architecture ensures a very high input common-mode rejection ratio without producing the mid-swing nonlinearities found in other rail-to-rail op amps.

For space-critical applications, the single MAX4162 is available in a SOT23-5 package.

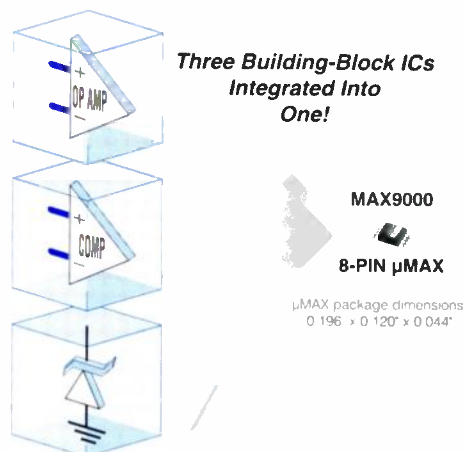
Spice Models Available

NEW

Op Amp + Comparator + Reference Offers 8MHz BW+185ns Prop. Delay + 8ppm/°C Tempco in 8-Pin Package

Single-Supply Operation Down to 2.5V, Use Only 340µA Supply Current

The MAX9000 family of building-block ICs exceeds the speed limit set by existing solutions. In a single 8- or 10-pin µMAX package, these devices integrate a low-power, high-speed op amp with a high-speed comparator, as well as a precision 1.230V reference. The unity-gain-stable devices in this family (MAX9000/MAX9001/MAX9002) deliver a fast 1.25MHz amplifier, while amplifiers in the MAX9003/MAX9004/MAX9005 have a gain-bandwidth product of 8MHz and are stable for gains of +10V/V or greater. Add to that a comparator with a fast 185ns propagation delay, and you've got a family of building-block ICs that's over 15-times faster than previous integrated solutions.



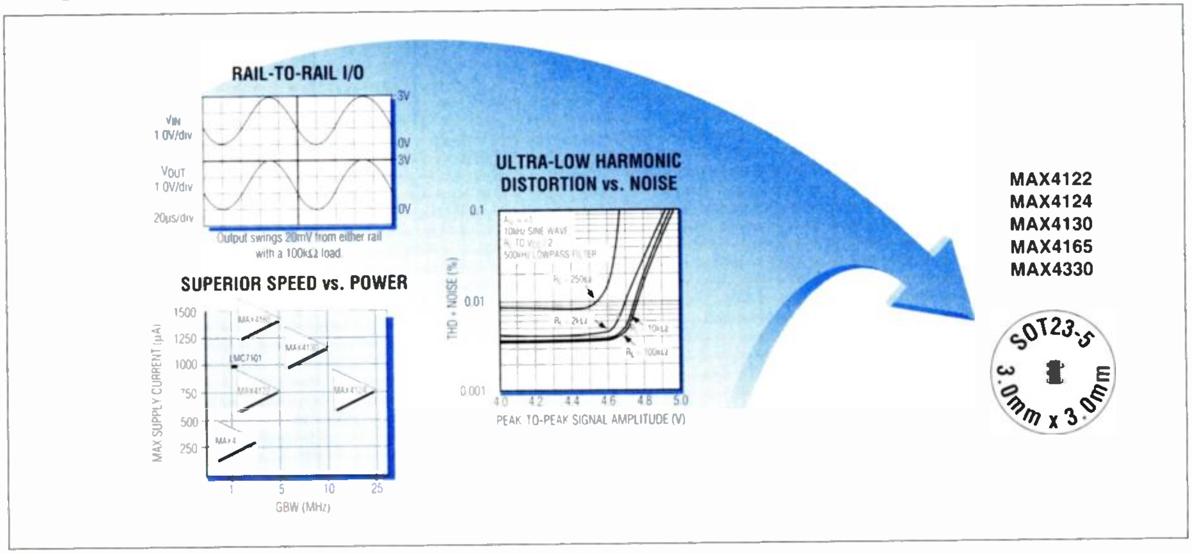
These devices operate from a +2.5V to +5.5V single supply and typically draw just 340µA (425µA max) of quiescent current. The MAX9000/MAX9004 offer a low-power shutdown mode that reduces supply current to 2µA. Additionally, the MAX9000/MAX9001/MAX9003/MAX9004 feature an internal ±1%, 1.230V reference with an 8ppm/°C tempco. Outputs swing rail-to-rail and the input common-mode range includes ground.

MAXIM

Spice Models Available

Best Rail-to-Rail I/O Op Amps in a SOT23-5 Package

Single-Supply Operation Down to 2.4V, GBWs from 3MHz to 25MHz



Choose from the Most Rail-to-Rail Options in the Industry!

Device	Amplifiers per Package	Shutdown	Supply Voltage (V)	Minimum Stable Gain (V/V)	Gain Bandwidth (MHz)	Supply Current per Op Amp (µA, max)	Vos (µV, max)
MAX4122/4123	Single	Yes	+2.7 to +6.5	1	5	750	600
MAX4124/4125	Single	Yes	+2.7 to +6.5	10	25	750	600
MAX4126/4127	Dual	Yes	+2.7 to +6.5	1	5	750	750
MAX4128	Dual	No	+2.7 to +6.5	10	25	750	750
MAX4129	Quad	No	+2.7 to +6.5	1	5	750	1500
MAX4130/4131	Single	Yes	+2.7 to +6.5	1	10	1050	600
MAX4132/4133	Dual	Yes	+2.7 to +6.5	1	10	1050	750
MAX4134	Quad	No	+2.7 to +6.5	1	10	1050	1500
MAX4165/MAX4166	Single	Yes	+2.7 to +6.5	1	5	1400	1500
MAX4167/MAX4168	Dual	Yes	+2.7 to +6.5	1	5	1400	850
MAX4169	Quad	No	+2.7 to +6.5	1	5	1400	850
MAX4330/MAX4331	Single	Yes	+2.4 to +6.5	1	3	290	600
MAX4332/MAX4333	Dual	Yes	+2.4 to +6.5	1	3	290	900
MAX4334	Quad	No	+2.4 to +6.5	1	3	290	1000

The MAX4122–MAX4134, MAX4330–MAX4334, and MAX4165–MAX4169 rail-to-rail input/output op amps simplify low-voltage designs. Designed on Maxim's new proprietary high-speed bipolar process, these amplifiers combine wide bandwidths with excellent DC precision and superior speed-to-power ratios. The three families feature gain-bandwidth products of 3MHz, 5MHz, 10MHz, and 25MHz ($A_V \geq 10V/V$) and are guaranteed to operate down to a +2.4V single supply. Beyond-the-Rails capability allows the inputs to extend 200mV **beyond** the supply rails and the output to swing within 20mV from either rail (R_L = 100kΩ)! The MAX4122–MAX4129 require only 650µA (750µA max) per amplifier and are capable of driving 250Ω loads. The MAX4130–MAX4134 are single, dual, and quad 10MHz amplifiers that consume less than 1.05mA per amplifier. This superior speed vs. power makes the MAX4122–MAX4134 ideal for high-speed portable applications. In addition, the single-amplifier MAX4122/MAX4124/MAX4130/ MAX4165/MAX4330 are available in the space-saving SOT23-5 package. For applications where power consumption is critical, a shutdown mode is also provided to cut supply current to just 25µA per amplifier.

Spice Models and EV Kit Available

First Single-Supply, 300MHz Rail-to-Rail Op Amps Offered in a SOT23-5

0.1dB Gain Flatness to 50MHz; Drive 150Ω Loads

The MAX4212–MAX4222 family of rail-to-rail op amps incorporates low power consumption, single-supply operation, and wide bandwidth—all in a tiny 5-pin SOT23 package. These features make the MAX4212 op-amp family ideal for a variety of battery-powered instruments, high-speed ADC preamps, and video applications. These devices employ a voltage-feedback architecture, but their specifications are typical of current-feedback amplifiers.

Devices in this family operate from a single supply of +3.3V to +11V or dual supplies of ±1.65V to ±5.5V. They require only 5.5mA quiescent supply current per amplifier while achieving a 300MHz -3dB bandwidth, slew-rates of 600V/µs, and an output current drive of ±100mA. In addition, they offer 0.1dB gain flatness to 50MHz, low differential gain/phase errors of only 0.02%/0.02°, and a spurious-free dynamic range (SFDR) of -78dBc at 5MHz.

Their input common-mode range includes ground and their outputs swing rail-to-rail, making these devices ideal for low-voltage single-supply applications. In addition, an optional disable mode lowers the supply current to 550µA (max) and places the outputs in a high-impedance state—a useful feature for multiplexing applications.

Choose the Ideal Single-Supply Op Amp for Your High-Speed Application

Part	No. of Amps	Min. Stable Gain (V/V)	-3dB Bandwidth (MHz)	0.1dB Gain Flatness (MHz)	Slew Rate (V/µs)	Diff. Gain/Phase Error (%/°)	Output Swing (V)** (R_L = 10kΩ)	Shutdown	Pin-Package
MAX4212/4213	1	1	300	50	600	0.02/0.02	0.05 to 4.95	Yes	5-pin SOT23, 8-pin SO/µMAX
MAX4214/4215	1	2	300	50	600	0.02/0.02	0.05 to 4.95	Yes	5-pin SOT23, 8-pin SO/µMAX
MAX4216	2	1	200	35	600	0.02/0.02	0.05 to 4.95	No	8-pin SO/µMAX
MAX4217	2	2	200	35	600	0.02/0.02	0.05 to 4.95	No	8-pin SO/µMAX
MAX4218/4220	3/4	1	200	35	600	0.02/0.02	0.05 to 4.95	Yes	14-pin SO, 16-pin QSOP
MAX4219/4222	3/4	2	200	35	600	0.02/0.02	0.05 to 4.95	Yes	14-pin SO, 16-pin QSOP

**V_{CC} = +5V, V_{EE} = 0V

Applications:

- Professional Video
- Ultrasound Equipment
- LAN Cable Testers
- A/D Drivers

MAXIM

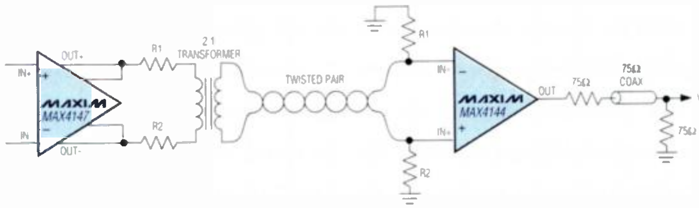
Spice Models and EV Kit Available

300MHz Diff. Line Driver Delivers 160mA with Only -87dBc Distortion

NEW

High-Speed ±5V Line Drivers and Receivers

The MAX4144/MAX4145/MAX4146 triple op-amp instrumentation amplifiers and MAX4147 differential line-driver IC are ideal for video and telecom digital subscriber line (DSL) driver and receiver applications. This family replaces existing circuits that require multiple high-speed, high-power op amps.



The MAX4147 is optimized for differential, high-output-current, low-distortion applications. The output drives ±5.6V (differential) or ±2.8V (single-ended) into a 50Ω load. The amplifier is set for a fixed closed-loop gain of +2V/V. Operating from only 10mA supply current, the MAX4147 features a 300MHz -3dB bandwidth, 70MHz 0.1dB bandwidth, and ultra-low 0.008%/0.03° differential gain/phase. Superior low-distortion performance of -87dBc (3kHz, R_L = 33Ω) makes the MAX4147 ideal choice for DSL applications.

The MAX4144/MAX4145/MAX4146 instrumentation amplifiers have fully symmetrical differential inputs and a single-ended output. These amplifiers use laser-trimmed, matched thin-film resistors to achieve 60dB CMR at 10MHz. The output is capable of driving ±2.6V into a 150Ω load. The MAX4144 is internally set for a gain of +2V/V and features a 130MHz bandwidth, 110MHz full-power bandwidth, and 1000V/µs slew rate. The MAX4145 is unity-gain stable and features a 250MHz bandwidth and a 1400V/µs slew rate. The MAX4146 is optimized for high-gain applications (≥ +10V/V), and its gain can be set with a single resistor.

Spice Models and EV Kit Available

1mA, 270MHz Amplifier Available in a SOT23 Package

Low 73dB SFDR, 70MHz 0.1dB Gain Flatness

The MAX4180 family of ultra-low-power amplifiers features very wide bandwidths, 450V/µs slew rates, low distortion, and excellent video specifications in space-saving packages—including the ultra-small 6-pin SOT23! These devices operate from either a +5V single supply or dual ±2.25V to ±5.5V supplies and draw only 1mA (1.2mA max) supply current, making them ideal for power-critical video applications such as ultrasound, professional cameras, or any high-speed portable equipment. In addition, the MAX4180/MAX4182/MAX4183/MAX4185 have a low-power shutdown mode that reduces supply current to only 135µA and places the outputs in a high-impedance state, which is useful in multiplexing applications.

The MAX4180/MAX4182/MAX4183/MAX4186 are compensated for closed-loop gains of +2V/V (6dB) or greater, while the MAX4181/MAX4184/MAX4185/MAX187 are optimized for unity gain.

Part	No. of Amps	Minimum Stable Gain (V/V)	-3dB Bandwidth (MHz)	-0.1dB Gain Flatness (MHz)	Diff. Gain/Phase Error (%/°)	Settling Time to 0.1% (ns)	Slew Rate (V/µs)	Shutdown	Pin-Package
MAX4180/4181	1	2/1	245/270	70/60	0.08/0.03	20	450	Yes	6-pin SOT23, 8-pin SO
MAX4182/4184	2	2/1	245/270	70/60	0.08/0.03	20	450	No	8-pin SO
MAX4183/4185	2	2/1	245/270	70/60	0.08/0.03	20	450	Yes	14-pin SO, 10-pin µMAX
MAX4186/4187	4	2/1	245/270	70/60	0.08/0.03	20	450	No	14-pin SO, 16-pin QSOP

Spice Models and EV Kit Available

2/4/8-Channel Video Mux/Amps Offer 0.1dB Gain Flatness to 130MHz

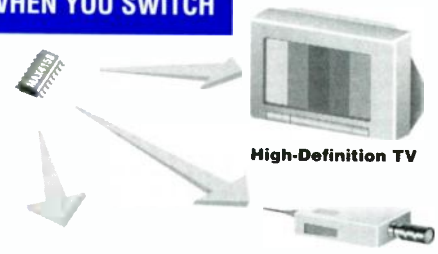
Pixel Switch in 20ns, Drive 50Ω Coaxial Cable

The combination of fast input-signal multiplexing, excellent 0.1dB gain flatness, and low differential gain and phase error makes the MAX4158/MAX4159/MAX4258/MAX4259 and MAX4160*/MAX4161*/MAX4260*/MAX4261* 2-, 4- and 8-channel multiplexer/amplifiers ideal for any broadcast-quality video application. These new, noninverting video mux/amps feature a 0.1dB bandwidth of 130MHz, differential gain/phase errors of 0.01%/0.01°, and the ability to drive ±2.5V into back-terminated 50Ω or 75Ω cables. They operate from ±5V supply rails and consume only 100mW.

The MAX4158/MAX4159 and MAX4160/MAX4260 are optimized for unity-gain stability. They feature -3dB bandwidths of 350MHz and slew rates (at Av = 0dB) of 700V/µs. The MAX4258/MAX4259 and MAX4161/MAX4261 are optimized for Av = +6dB. They have -3dB bandwidths of 250MHz and slew rates (at Av = 6dB) of 1000V/µs. All exhibit fast channel-to-channel switching (20ns) and small switching transients (less than 70mV), making them an excellent choice for video multiplexing and pixel-switching applications.

*Future product—contact factory for availability

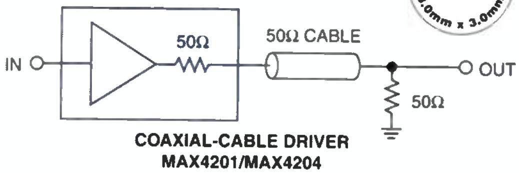
NO GLITCH WHEN YOU SWITCH



- **Broadcast Video**
- **High-Speed Signal Processing**
- **Video-Signal Multiplexing**
- **Workstations**
- **Multimedia Products**

NEW

World's First Open-Loop Buffers in SOT23-5



FEATURES

- **780MHz -3dB Bandwidth**
- **4200V/µs Slew Rate**
- **Low 2.2mA Supply Current**
- **High ±90mA Output Drive**
- **Low 2.1nV/√Hz Voltage-Noise Density**

APPLICATIONS

- **High-Speed ADC Input Buffers**
- **Wireless LANs**
- **High-Speed DAC Buffers**
- **IF/Communications Systems**
- **Digital-Transmission Line Drivers**

Part	No. of Amps	On-Chip Output Termination (Ω)	-3dB Bandwidth (MHz)	0.1dB Gain Flatness (MHz)	Supply Current (mA)	Slew-Rate (V/µs)	Input Voltage Noise Density (nV/√Hz)	Pin-Package
MAX4200	1	—	660	220	2.2	4200	2.1	5-pin SOT23, 8-pin SO
MAX4201	1	50	780	280	2.2	4200	2.1	5-pin SOT23, 8-pin SO
MAX4202	1	75	780	280	2.2	4200	2.1	5-pin SOT23, 8-pin SO
MAX4203	2	—	530	130	2.2	4200	2.1	8-pin µMAX/SO
MAX4204	2	50	720	230	2.2	4200	2.1	8-pin µMAX/SO
MAX4205	2	75	720	230	2.2	4200	2.1	8-pin µMAX/SO

MAXIM

Spice Models and EV Kit Available

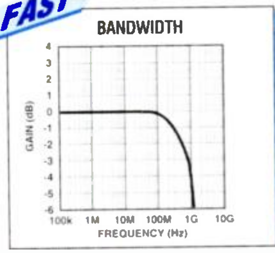
Stealth Op Amps: Fast and Silent

880MHz -3dB Bandwidth with Only 2.1nV/√Hz Noise

NEW

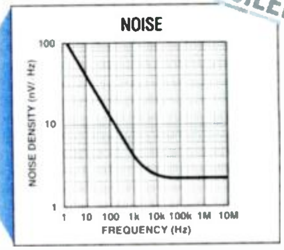
The MAX4104/MAX4105/MAX4304/MAX4305 are ultra-high-speed, low-noise (2.1nV/√Hz), and low-distortion (-88dBc SFDR) op amps in tiny SOT23-5 packages. This combination of features makes these amplifiers ideal for low-noise/low-distortion video and telecommunications applications. These devices also feature a wide output voltage swing of ±3.7V, and ±70mA output current drive capability.

FAST



AVAILABLE IN SOT23-5 3.0mm x 3.0mm

SILENT



	Part	Min Stable Gain (V/V)	Supply Voltage (V)	-3dB Bandwidth (MHz)	Slew Rate (V/µs)	0.01% Settling Time (ns)	Distortion (SFDR, dBc) (R_L = 100Ω)	Voltage Noise (nV/√Hz)	Diff. Gain/Phase Error (°/%)	Pin-Package
NEW	MAX4104	1	±5	880	400	25	-88	2.1	0.01/0.01	8-pin SO, 5-pin SOT23
NEW	MAX4105	5	±5	430	1400	25	-74	2.1	0.02/0.02	8-pin SO, 5-pin SOT23
LOWEST NOISE	MAX4106/ MAX4107	5/10	±5	350/300	275/500	18	-63/-60	0.75	0.02/0.04	8-pin SO
NEW	MAX4304	2	±5	730	1000	25	-88	2.1	0.01/0.01	8-pin SO, 5-pin SOT23
NEW	MAX4305	10	±5	350	1400	25	-74	2.1	0.02/0.02	8-pin SO, 5-pin SOT23

Spice Models and EV Kit Available

SOT23 Op Amps Deliver 1GHz -3dB Bandwidth while Drawing Only 6.0mA

80mA Output Current Drive, 300MHz 0.1dB Gain Flatness

SOT23-6 3.0mm x 3.0mm

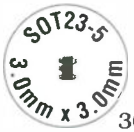
The new MAX4223–MAX4228 family of ultra-high-speed, low-power amplifiers features low distortion, 80mA output current, and excellent video specifications in a space-saving 6-pin SOT23 package. These devices operate from dual ±2.85V to ±5.5V supplies and draw only 6.0mA (9.0mA max) of supply current per amplifier.

The MAX4223–MAX4228 are ideal for professional video applications, with differential gain and phase errors of 0.01% and 0.02°, 0.1dB gain flatness of 300MHz, and a 1700V/µs slew rate. Total harmonic distortion (THD) of -60dBc (10MHz) and an 8ns settling time suit these devices for driving high-speed ADC inputs in data-communications applications. The MAX4223/MAX4224/MAX4226/MAX4228 have a shutdown mode that reduces supply current to only 350µA, making them suitable for portable/battery-powered applications. Their high output impedance in shutdown mode is also useful for multiplexing applications.

Part	No. of Amps	Minimum Stable Gain (V/V)	-3dB Bandwidth (MHz)	-0.1dB Gain Flatness (MHz)	Diff. Gain/Phase Error (%/°)	Settling Time to 0.1% (ns)	Slew Rate (V/µs)	Low-Power Shutdown	Pin-Package
MAX4223/4224	1	1/2	1000/600	300/200	0.01/0.02	8/5	1700/1400	Yes	6-pin SOT23, 8-pin SO
MAX4225/4227	2	1/2	1000/600	300/200	0.01/0.02	8/5	1700/1400	No	8-pin SO
MAX4226/4228	2	1/2	1000/600	300/200	0.01/0.02	8/5	1700/1400	Yes	10-pin µMAX, 14-pin SO

Low-Cost, Micropower, Microsize Rail-to-Rail I/O Comparators

Available in a SOT23 Package, Operate Down to 2.5V



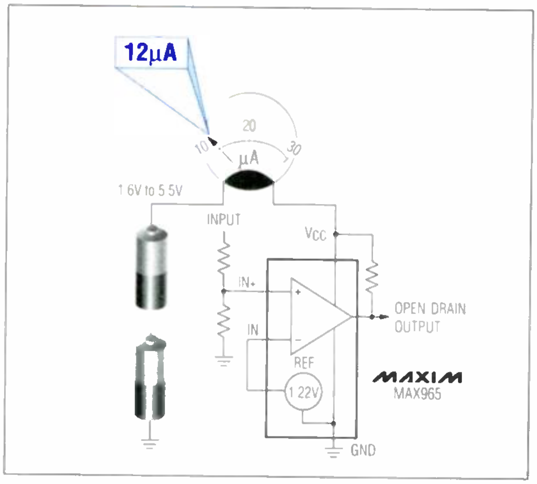
The MAX985–MAX996 comparators combine ultra-low power consumption, single-supply operation, Beyond-the-Rails inputs, and rail-to-rail outputs in a space-saving 5-pin SOT23 package. They operate from a single +2.5V to +5.5V supply, making them ideal for single 3V or 5V systems in portable/battery-powered applications. The MAX985/86/89/90/93/94 have a 300ns propagation delay while drawing only 13µA (20µA max) of supply current per comparator. The MAX987/88/91/92/95/96 typically draw only 48µA (80µA max) while achieving a 120ns propagation delay.

These comparators have outputs that swing rail-to-rail and an input common-mode voltage range that extends 200mV beyond both rails. The MAX985/87/89/91/93/95 have a push/pull output stage that allows them to both source and sink current, while the MAX986/88/90/92/94/96 have open-drain outputs, useful for wire-ORing. For space-critical applications, the single MAX985–MAX988 are available in a SOT23-5 package, the dual MAX989–MAX992 come in an 8-pin µMAX or SO, and the quad MAX993–MAX996 are available in a 14-pin SO or 16-pin QSOP.

Micropower, Beyond-the-Rails Comparator Guaranteed to Operate Down to 1.6V

5µA Supply Current, Internal 1.22V Reference

Maxim's new MAX965–MAX970 micropower, ultra-low-voltage comparators deliver true 2-cell operation with inputs that extend 250mV Beyond-the-Rails and rail-to-rail outputs. In addition, the MAX965 and MAX967/MAX968/MAX969 have an internal 1.22V ±1.5% bandgap reference. These ICs are guaranteed to operate from a single supply down to 1.6V, and draw less than 5.5µA of supply current, maximizing battery life in 2-cell portable systems. The MAX966 and MAX970 are dual and quad comparators, respectively, that typically operate from supply voltages as low as 1.0V and draw less than 5µA of supply current.



Choose from the Lowest Voltage, Micropower, Rail-to-Rail Comparators Available

Part	No. of Comparators	1.22V Internal Reference	Supply Voltage Range (V)	Max Supply Current per Comparator (µA)	Rail-to-Rail Inputs and Outputs	Programmable Hysteresis	Pin-Package
MAX965	1	Yes	+1.6 to +5.5	12	Yes	Yes	8-pin µMAX/SO
MAX966	2	No	+1.6 to +5.5	5	Yes	No	8-pin µMAX/SO
MAX967	2	Yes	+1.6 to +5.5	8	Yes	Yes	8-pin µMAX/SO
MAX968	2	Yes	+1.6 to +5.5	8	Yes	Yes	8-pin µMAX/SO
MAX969	4	Yes	+1.6 to +5.5	5.5	Yes	Yes	16-pin SO/QSOP
MAX970	4	No	+1.6 to +5.5	4.5	Yes	No	14-pin SO, 16-pin QSOP

MAXIM

Spice Models Available

Only µPower Op Amp + Comparator + Reference in a Single 8-Pin Package!

Consumes Less than 7µA, Single-Supply Operation Down to 2.7V

Devices in the MAX951 family are the first building-block ICs to integrate an ultra-low-power op amp, comparator, and reference (MAX951/MAX952) in an 8-pin SO or µMAX package! These unique, versatile ICs consume 10-times **LESS** power than the existing discrete solution, and require 1/6 the board space (when using the µMAX package).

The MAX951 family is optimized for single-supply, ultra-low-power applications. The op amp and comparator's input voltage range includes ground, and the outputs swing rail-to-rail. And, unlike industry-standard micropower CMOS op amps, the MAX951 family's op amp is capable of driving capacitive loads in excess of 1000pF.

Part	Op Amp: 20kHz Unity-Gain Stable	Op Amp: 125kHz Decomp'd (Av ≥ 10V/V)	Comparator	Reference	Min Supply Voltage (V)	Supply Current (µA)
MAX951	✓		✓	✓	2.7	7
MAX952		✓	✓	✓	2.7	7
MAX953	✓		✓		2.4	5
MAX954		✓	✓		2.4	5

Spice Models Available

NEW

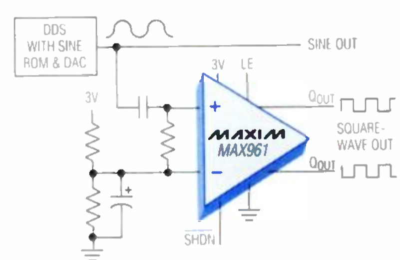
4.5ns, Beyond-the-Rails Comparators Guarantee Operation Down to 2.7V

5µA Supply Current in a 5-Pin SOT23 Package

The MAX961–MAX964/MAX997/MAX999 high-speed comparators are the first to guarantee less than 7ns (4.5ns typical) propagation delay while operating from a single supply as low as +2.7V. And, propagation delay skew is only 300ps—an important feature for digital communications applications.

Optimized for high-speed 3V systems, these devices feature an input voltage range that extends 100mV Beyond-the-Rails to maximize the comparator's dynamic range. Supply current for the MAX997 and MAX999 is 5mA (6.5mA max). For power-sensitive applications, a shutdown feature reduces the supply current to 500µA and puts the output into a high-impedance state. Internal hysteresis is added to ensure that the parts remain stable through the linear region. Other features include complementary outputs (MAX961/MAX963) and an output latch function (MAX961/MAX963). For space-sensitive applications, the MAX999 is available in a tiny SOT23-5 package.

SINE TO SQUARE-WAVE CONVERTER



Select the Ideal Comparator for Your Low-Voltage, High-Speed Design

Part	Comparators per Package	Input Offset Voltage (mV)	Logic	Complementary Outputs	Supply Voltage (V)	Supply Current per Comparator (mA, max)	tPD (ns, max)	Pin-Package
MAX961	1	0.5	CMOS	Yes	+2.7 to +5.5	11	7	8-pin SO/µMAX
MAX962	2	0.5	CMOS	No	+2.7 to +5.5	8	7	8-pin SO/µMAX
MAX963	2	0.5	CMOS	Yes	+2.7 to +5.5	11	7	14-pin SO
MAX964	4	0.5	CMOS	No	+2.7 to +5.5	8	7	16-pin SO/QSOP
MAX997	1	0.5	CMOS	No	+2.7 to +5.5	6.5	7	8-pin SO/µMAX
MAX999	1	0.5	CMOS	No	+2.7 to +5.5	6.5	7	5-pin SOT23

MAXIM

Spice Models Available

NEW

World's Fastest Comparators Under 650μA

20ns Propagation Delay, Available in SOT23 Package

The new single MAX998, dual MAX976, and quad MAX978 comparators have the best speed/power ratio of any high-speed comparator in the industry. While drawing a mere 225μA (650μA max) supply current, they achieve a propagation delay of 20ns (40ns max). These rail-to-rail comparators are optimized for use in single 3V or 5V systems, making them ideal for portable/battery-powered applications.

The MAX998/MAX976/MAX978's inputs have a common-mode voltage range of -0.2V to (V_{CC} - 1.2V). The outputs are capable of rail-to-rail operation without external pull-up circuitry. In addition, both the inputs and outputs can tolerate a continuous short to either rail.

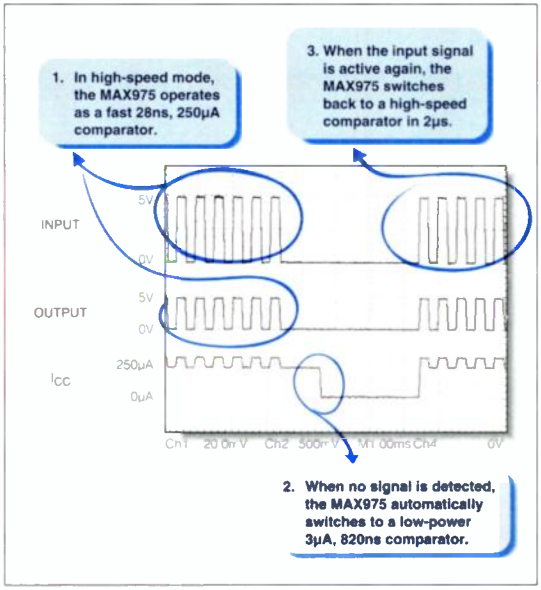
Part	No. of Comparators	Propagation Delay (ns)	Supply Voltage Range (V)	Supply Current per Comparator (μA, max)	Rail-to-Rail Outputs	Pin-Package
MAX998	1	20	+2.7 to +5.5	650	Yes	5-pin SOT23, 8-pin SO
MAX976	2	20	+2.7 to +5.5	650	Yes	8-pin μMAX/SO
MAX978	4	20	+2.7 to +5.5	650	Yes	14-pin SO, 16-pin QSOP

Spice Models Available

World's First AutoShutdown Comparators

Switch from a Fast 28ns Comparator to a Power-Saving 3μA Comparator

Unlike typical high-speed comparators that waste valuable supply current, the dual-speed MAX975/MAX977 offer the benefit of speed only when required. Power consumption is automatically reduced and the comparator is placed in a low-speed mode when no signal is detected. These new comparators operate with a single supply down to +2.7V and their outputs swing rail-to-rail. Their dual-speed feature makes them ideal for IR, Toll Tag™, and data-acquisition applications where high-speed signals are not continuously present.



In high-speed mode they draw only 300μA (500μA max) supply current and achieve a propagation delay of 28ns (50ns max). In the low-power/low-speed mode they consume a mere 3μA while maintaining an 820ns propagation delay. The auto-standby feature automatically disables the comparator when it exceeds a programmed interval without an output transition and places it in a low-power/standby condition (5μA max supply current). When it next detects a signal, it goes back into its high-speed mode.

The inputs have a common-mode voltage range of -0.2V to (V_{CC} - 1.2V). The outputs are capable of rail-to-rail operation without external pull-up circuitry, simplifying the interface with CMOS/TTL logic.

Toll Tag is a registered trademark of Amtech Corp

Part Number	V_{OS} (mV max)	I_{BIAS} (nA max)	Unity GBW (MHz)	V_{IN} Range (V_{CC-}_V) to (V_{EE+}_V)	V_{OUT} Swing/Load (V_{CC-}_V) to (V_{EE+}_V)/(Ω)	Supply Voltage (V)	Supply Current/ Op Amp (mA max)	Features	Price† 1000-up ($)
LOW-OFFSET-VOLTAGE BIPOLAR ICs									
MAX400	10 to 15μV	2	0.4	1 to 1	3 to 3/1k	±3 to ±18	4	Ultra-low V_{OS} & drift, non-chopper stabilized	5.16
MAX427/437	15μV	35	8/60	2 5 to 2.5	1.2 to 1.2/2k	±15	4	High speed, low 3.8nV/√Hz noise, precision	1 83
MAX478/479	70 to 250μV	6	60kHz	1 1 to -0.3	1.2 to 0.2/2k	+2 2 to +36, ±1.1 to ±18	17μA	Micropower, precision dual 8-pin SO and quad 14-pin narrow SO, 3V, 5V, and ±15V specs	2.58/3.35
MAX480	70μV	3	20kHz	1 to 0	0.8 to 0/2k	+1.6 to +36, ±0.8 to ±18	15μA	Low V_{OS} & drift, micropower, single supply, input/output extend to negative rail	2.59
MAX492/494/495	500μV	60	500kHz	0 to 0	0.15 to 0.15/1k	+2.7 to +6	150μA	Dual/quad/single, precision, rail-to-rail I/O	2.25/3.60/1.45
MXL1001	15 to 60μV	2 to 4	0.8	1 to 1	1.5 to 1.5/1k	±3 to ±18	2	Precision LT1001 second source	1.73
MXL1007	25 to 60μV	35 to 55	8	2 5 to 2.5	2.5 to 2 5/600	±15	4 to 4.7	Low noise, precision LT1007 second source	1.85
MXL1013/1014	150 to 800μV	20 to 30	0.6	1.2 to -0.3	1 to 5mV/600	+4 to +36, ±2 to ±18	0.50 to 0 55	Dual/quad, precision LT1013/1014 second source	1.57/3 06
MXL1178/1179	70 to 600μV	5 to 6	60kHz	1.1 to -0.3	1.2 to 0.2mV/2k	+2.2 to +36, ±1.1 to ±18	17 to 21μA	Dual/quad, precision, micropower LT1178/1179 second source	2 50/3.35
OP07	25 to 150μV	2 to 12	0.6	1 to 1	3 to 3/1k	±3 to ±18	4	Industry standard, precision	1 58
OP27	25 to 100μV	40 to 80	8	2 7 to 2.7	3.5 to 3.5/600	±3 to ±18	4.6 to 5.6	Industry standard, low noise	2.06
OP37	25 to 100μV	40 to 80	63 (Av ≥ 5)	2 7 to 2.7	3 5 to 3 5/600	±3 to ±18	4 6 to 5 6	Industry standard, low noise	2 06
OP90	150 to 450μV	15 to 25	0.020	1 to 0	0.8 to 0.1mV/10k	±0.8 to ±18, +1.6 to +36	15 to 20μA	Industry standard, micropower	1.60
LOW-OFFSET-VOLTAGE CHOPPERS									
MAX420/422	5 to 10μV	0 03 to 0 10	0 125 to 0 5	3 5 to -0.1	0 5 to 0.5/10k 0.4 to 0.4/100k	±2.5 to ±16 5	0 5 to 2	±15V chopper stabilized	3 77/4.21
MAX421/423	5 to 10μV	0.03 to 0 10	0.125 to 0.5	3 5 to -0 1	0.5 to 0.5/10k 0 4 to 0.4/100k	±2.5 to ±16 5	0.5 to 2	±15V chopper stabilized with clamped output and INT/EXT clock option	4 21/5.57
MAX430/432	5μV	0.1	0.125 to 0.5	2.5 to -0.1	0.5 to 0.5/10k	±2 5 to ±16 5	0.5 to 2	±15V chopper stabilized with internal caps	4.80/5.29
ICL7650	5 to 10μV	0.01 to 0.02	2	3 to -0.2	0 05 to 0.05/100k	±5	2	Industry standard, chopper stabilized	2.16
ICL7652	5 to 10μV	0 03	0 45	1 to 0 2	0 05 to 0 05/100k	±5	2	Low noise, industry standard, chopper stabilized	3 24
LOW BIAS CURRENT									
MAX406/407/418	10	10pA	8 to 40kHz	1.1 to 0	0 01 to 0.01/1M	+2.5 to +10	1 2μA	Single/dual/quad, lowest power, single supply, rail-to-rail outputs, unity-gain stable	1 38/1.95/3.40
MAX409/417/419	10	10pA	150kHz (Av ≥ 10V/V)	1.1 to 0	0.01 to 0.01/1M	+2.5 to +10	1.2μA	Single/dual/quad, lowest power, decompensated (Av ≥ 10V/V)	1.38/1.95/3.40
MAX420/422	5 to 10μV	0 03 to 0 10	0 125 to 0 5	2.5 to -0.1	0.5 to 0.5/10k 0.4 to 0.4/100k	±2.5 to ±16.5	0 5 to 2	±15V chopper stabilized	3 77/4 21
MAX421/423	5 to 10μV	0 03 to 0 10	0 125 to 0 5	2 5 to -0.1	0 5 to 0.5/10k 0.4 to 0.4/100k	±2.5 to ±16.5	0.5 to 2	±15V chopper stabilized with clamped output and INT/EXT clock option	4.21/5 57
MAX430/432	5μV	0.1	0.125 to -0.1	2.5 to -0.1	0.5 to 0.5/10k	±2.5 to ±16.5	0.5 to 2	±15V chopper stabilized with internal caps	4.80/5.29
MAX4162	4	100pA	200kHz	-0.25 to -0 25	0 04 to 0.025/10k	+2.7 to +10	40μA	Single, rail-to-rail I/O, ultra-low power, available in SOT23-5	0.75
MAX4163/4164	4	100pA	200kHz	-0.25 to -0.25	0.04 to 0.025/10k	+2.7 to +10	40μA	Dual/quad, rail-to-rail I/O, ultra-low power	1.20/2.10
LOW NOISE									
MAX400	10 to 15μV	2	0 4	1 to 1	3 to 3/1k	±3 to ±18	4	Ultra-low V_{OS} & drift, non-chopper stabilized	5.16
MAX410/412/414	1 typ (320μV MAX414)	150	28	1.3 to 1.2	1.3 to 1.2/2k	±2 4 to ±5 25	2.7	Single/dual/quad, high speed, low noise, <2.4nV/√Hz at 1kHz guaranteed, unity-gain stable	1 50/2.45/4.50
MAX427/437	15μV	35	8/60	2.5 to 2.5	1.2 to 1.2/2k	±15	4	High speed, low 3.8nV/√Hz noise, precision	1 83
MAX4249/4257	0 7	100pA	22 (Av ≥ 10V/V)	-0.2 to 1.1	0.08 to 0.07/10k	+2 4 to +5 5	575μA	Dual, 2 4V, low noise, low distortion, rail-to-rail outputs, MAX4249 with shutdown (Av ≥ 10V/V)	1.45/1.30
MAX4250	0.7	100pA	3	-0.2 to 1.1	0.08 to 0.07/10k	+2.4 to +5.5	575μA	Single, 2.4V, low noise, low distortion, rail-to-rail outputs in SOT23	0 83
MAX4251	0.7	100pA	3	-0.2 to 1.1	0.08 to 0.07/10k	+2.4 to +5.5	575μA	Single, 2.4V, low noise, low distortion, rail-to-rail outputs in 8-pin μMAX with shutdown	0.95

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Part Number	V_{OS} (mV max)	I_{BIAS} (nA max)	Unity GBW (MHz)	V_{IN} Range (V_{CC}-_V) to (V_{EE}+_V)	V_{OUT} Swing/Load (V_{CC}-_V) to (V_{EE}+_V)/(Ω)	Supply Voltage (V)	Supply Current/ Op Amp (mA max)	Features	Price† 1000-up ($)
LOW NOISE (continued)									
MAX4252/4253	0.7	100pA	3	-0.2 to 1.1	0.08 to 0.07/10k	+2.4 to +5.5	575µA	Dual, 2.4V, low noise, low distortion, rail-to-rail outputs	††
MAX4254	0.7	100pA	3	-0.2 to 1.1	0.08 to 0.07/10k	+2.4 to +5.5	575µA	Quad, 2.4V, low-noise, low distortion, rail-to-rail outputs	††
MAX4255	0.7	100pA	22 ($A_V \geq$ 10V/V)	-0.2 to 1.1	0.08 to 0.07/10k	+2.4 to +5.5	575µA	Single, 2.4V, low noise, low distortion, rail-to-rail outputs in SOT23 ($A_V \geq$ 10V/V)	0.83
MAX4256	0.7	100pA	22 ($A_V \geq$ 10V/V)	-0.2 to 1.1	0.08 to 0.07/10k	+2.4 to +5.5	575µA	Single, 2.4V, low noise, low distortion, rail-to-rail outputs in 8-pin µMAX with shutdown ($A_V \geq$ 10V/V)	0.95

Single-Supply, Low-Power Op Amps

Part Number	Op Amp Compensation	Op Amp GBW (kHz)	Comparator Propagation Delay (µs)	Reference (1.2V ±1%)	Supply Voltage (V min)	Supply Current (µA max)	Features	Price† 1000-up ($)
OP AMP + COMPARATOR + REFERENCE ICs								
MAX951	Unity-gain stable	20	4	Yes	2.7	10	Single-supply, rail-to-rail outputs, 8-pin package, low-cost op amp drives capacitive loads	1.60
MAX952	Decompensated ($A_V \geq$ 10V/V)	125	4	Yes	2.7	10	MAX951 with decompensated op amp for $A_V \geq$ 10V/V	1.60
MAX953	Unity-gain stable	20	4		2.4	8	MAX951 without the reference	1.30
MAX954	Decompensated ($A_V \geq$ 10V/V)	125	4	–	2.4	8	MAX953 with decompensated op amp for $A_V \geq$ 10V/V	1.30
MAX9000/9001	Unity-gain stable	1.25MHz	0.185	Yes	2.5	500	Low power, single supply, rail-to-rail outputs, shutdown (MAX9001)	1.80/1.89
MAX9002	Unity-gain stable	1.25MHz	0.185	Yes	2.5	500	MAX9000 without the reference	1.20
MAX9003/9004	Decompensated	8MHz	0.185	Yes	2.5	425	MAX9000 with decompensated op amp for $A_V \geq$ 10V/V	1.80/1.89
MAX9005	Decompensated	8MHz	0.185	Yes	2.5	425	MAX9003 without the reference	1.20

Part Number	V_{OS} (mV max)	I_{BIAS} (nA max)	Unity GBW (MHz)	V_{IN} Range (V_{CC}-_V) to (V_{EE}+_V)	V_{OUT} Swing/Load (V_{CC}-_V) to (V_{EE}+_V)/(Ω)	Supply Voltage (V)	Supply Current/ Op Amp (mA max)	Features	Price† 1000-up ($)
MICROPOWER									
MAX406/407/418	10	10pA	8 to 40kHz	1.1 to 0	0.01 to 0.01/1M	+2.5 to +10	1.2µA	Single/dual/quad, lowest power, single supply, rail-to-rail outputs unity-gain stable	1.38/1.95/3.40
MAX409/417/419	10	10pA	150kHz ($A_V \geq$ 10V/V)	1.1 to 0	0.01 to 0.01/1M	+2.5 to +10	1.2µA	Single/dual/quad, lowest power, decompensated ($A_V \geq$ 10V/V)	1.38/1.95/3.40
MAX478/479	70 to 250µV	6	60kHz	1.1 to -0.3	1.2 to 0.2/2k	+2.2 to +36, ±1.1 to ±18	17µA	Micropower, precision dual 8-pin SO and quad 14-pin narrow SO, 3V, 5V, and ±15V specs	2.58/3.35
MAX480	70µV	3	20kHz	1 to 0	0.8 to 0/2k	+1.6 to +36, ±0.3 to ±18	15µA	Low V_{OS} & drift, micropower, single supply, input/output extend to negative rail	2.59
MAX492/494/495	500µV	60	500kHz	0 to 0	0.15 to 0.15/1k	+2.7 to +6	150µA	Dual/quad/single, precision, rail-to-rail I/O	2.25/3.60/1.45
MAX4162	4	100pA	200kHz	-0.25 to -0.25	0.04 to 0.025/10k	+2.7 to +10	40µA	Single, rail-to-rail I/O, ultra-low power, available in SOT23-5	0.75
MAX4163/4164	4	100pA	200kHz	-0.25 to -0.25	0.04 to 0.025/10k	+2.7 to +10	40µA	Dual/quad, rail-to-rail I/O, ultra-low power	1.20/2.10
MAX4230/4233	1.3	0.75	40kHz	-0.1 to -0.1	0.2 to 0.2/5k	+2.7 to +5.5	5µA	Single, ultra-low power, rail-to-rail I/O, available in SOT23	††
MAX4231/4234	1.3	0.75	40kHz	-0.1 to -0.1	0.2 to 0.2/5k	+2.7 to +5.5	5µA	Dual, ultra-low power, rail-to-rail I/O, available in 8-pin µMAX	††
MAX4232/4235	1.3	0.75	40kHz	-0.1 to -0.1	0.2 to 0.2/5k	+2.7 to +5.5	5µA	Quad, ultra-low power, rail-to-rail I/O, available in 16-pin QSOP	††
MAX4240/4241	0.75	5.0	90kHz	-0.2 to -0.2	0.009 to 0.009/100k	+1.8 to +5.5	15µA	Single, 1.8V, micropower, rail-to-rail I/O, MAX4240 in SOT23-5, shutdown (MAX4241)	0.83/0.95
MAX4242/4243	0.75	5.0	90kHz	-0.2 to -0.2	0.009 to 0.009/100k	+1.8 to +5.5	15µA	Dual, 1.8V, micropower, rail-to-rail I/O, MAX4242 in 8-pin µMAX, shutdown (MAX4243)	1.30/1.45
MAX4244	0.75	5.0	90kHz	-0.2 to -0.2	0.009 to 0.009/100k	+1.8 to +5.5	15µA	Dual, 1.8V, micropower, rail-to-rail I/O	2.20

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†† Future product—contact factory for pricing and availability. Specifications are preliminary.

Part Number	V_{OS} (mV max)	I_{BIAS} (nA max)	Unity GBW (MHz)	V_{IN} Range (V_{CC}-_V) to (V_{EE}+_V)	V_{OUT} Swing/Load (V_{CC}-_V) to (V_{EE}+_V)/(Ω)	Supply Voltage (V)	Supply Current/ Op Amp (mA max)	Features	Price† 1000-up ($)
MICROPOWER (continued)									
ICL7611	2 to 15	0.05	0 044 to 1 4	0.8 to 1	0.1 to 0.1/100k	±1 to ±8	0.02 to 2 5	Programmable quiescent current	1.35
ICL7612	5 to 15	0 05	0 044 to 1 4	-0 3 to -0 1	0.1 to 0 1/100k	±1 to ±8	0.02 to 2 5	Programmable quiescent current, rail-to-rail I/O	1 29
ICL7614	2 to 15	0 05	0 48*	0 8 to 1	0.1 to 0 1/100k	±1 to ±8	0.25	External compensation	0 95
ICL7616	2 to 15	0.05	0 044 to 1 4	2 to -0 1	0.1 to 0.1/100k	±1 to ±8	0.02 to 2 5	Programmable quiescent current, extended CMVR	1.62
ICL7621/7622	5 to 15	0 05	0 48	0 8 to 1	0.1 to 0 1/100k	±1 to ±8	0.25	Dual, low I_{BIAS} and I_{OS}	1 06/1 48
ICL7631/7632	5 to 20	0.05	0.044 to 1.4	0 8 to 1	0.1 to 0.1/100k	±1 to ±8	0 022 to 2.5	Triple op amp, programmable quiescent current, ICL7632 is externally compensated	2.27/2 12
ICL7641/7642	5 to 25	0 05	0.044 to 1.4	1 3 to 1.3, 0.6 to 1	0.5 to 0 5/10k, 0 1 to 0.1/1M	±1 to ±8	0.015 to 2.5	Quad, low power, CMOS	1 41/1 56
MXL1178/1179	70 to 600µV	5 to 6	60kHz	1 1 to -0 3	1 2 to 0 2mV/2k	+2.2 to +36, ±1.1 to ±18	17 to 21µA	Dual/quad, precision, micropower LT1178/1179 second source	2 50/3 35
OP90	150 to 450µV	15 to 25	0.020	1 to 0	0 8 to 0.1mV/10k	±0 8 to ±18, +1 6 to +36	15 to 20µA	Industry standard, micropower	1 60
HIGH SPEED									
MAX473/474/475	1 to 1 5	150	10	1 7 to -0 1	0 05 to 0.05/no load	+2 7 to +6	3	Single/dual/quad single or dual supply, wide output swing, 15V/µs min slew rate	1 45/2 25/3 60
MAX4122/4123	0 6 to 1 0	150	5	-0 25 to -0 25	0 24 to 0 125/250	+2.7 to +6 5	0 75	Single, rail-to-rail I/O, MAX4122 in SOT23-5, shutdown (MAX4123)	0 85/0 98
MAX4124/4125	0 6 to 1 0	150	25 (A_V ≥ 10V/V)	-0.25 to -0 25	0.24 to 0 125/250	+2.7 to +6 5	0.75	Single, rail-to-rail I/O, decompensated, shutdown (MAX4125)	0.85/0.98
MAX4126/4127	0 75 to 1 5	150	5	-0 25 to -0 25	0 28 to 0 18/250	+2 7 to +6 5	0 75	Dual, rail-to-rail I/O, unity-gain stable, shutdown (MAX4127)	1 40/1 67
MAX4128	0 75 to 1 5	150	25 (A_V ≥ 10V/V)	-0 25 to -0 25	0 28 to 0 18/250	+2 7 to +6 5	0 75	Dual, rail-to-rail I/O, decompensated	1 40
MAX4129	1 5	150	5	-0 25 to -0 25	0.28 to 0 18/250	+2.7 to +6.5	0.75	Quad, rail-to-rail I/O, unity-gain stable	2 40
MAX4130/4131	0 6 to 1 0	150	10	-0 25 to -0 25	0 24 to 0 125/250	+2 7 to +6 5	1 05	Single, rail-to-rail I/O, MAX4330 in SOT23-5, shutdown (MAX4131)	0 85/0 98
MAX4132/4133	0 6	150	10	-0 25 to -0 25	0.28 to 0 18/250	+2.7 to +6 5	1.05	Dual, rail-to-rail I/O, unity-gain stable, shutdown (MAX4133)	1 40/1 67
MAX4134	0.6	150	10	-0 25 to -0.25	0 28 to 0 18/250	+2 7 to +6 5	1 05	Quad, rail-to-rail I/O, unity-gain stable	2 40
MAX4165/4166	1 5	150	5	-0.25 to -0 25	0.34 to 0 16/25	+2.7 to +6 5	1.4	Single, 80mA output current drive, rail-to-rail I/O, MAX4165 in SOT23-5, shutdown (MAX4166)	0 80
MAX4167/4168	0.85	150	5	-0 25 to -0.25	0.34 to 0 16/25	+2 7 to +6 5	1 4	Dual, 80mA output current drive, rail-to-rail I/O, shutdown (MAX4168)	1.10/1 25
MAX4169	0 85	150	5	-0 25 to -0 25	0 34 to 0 16/25	+2 7 to +6.5	1.4	Quad, 80mA output current drive, rail-to-rail I/O	1 65
MAX4249–4257	(See Low-Noise Op Amp section tables)								
MAX4330/4331	0 60	65	3	-0 25 to -0 25	0 175 to 0 15/2k	+2 3 to +6 5	290µA	Single, rail-to-rail I/O, MAX4330 in SOT23-5, shutdown (MAX4331)	0 78/0 85
MAX4332/4333	0 90	65	3	-0 25 to -0 25	0 175 to 0 15/2k	+2.3 to +6 5	290µA	Dual, rail-to-rail I/O, MAX4332 in 8-pin µMAX, shutdown (MAX4333)	1 25/1 40
MAX4334	0 10	65	3	-0 25 to -0 25	0 175 to 0 15/2k	+2 3 to +6 5	290µA	Quad, rail-to-rail I/O	2 15
HIGH-SIDE CURRENT-SENSE AMPS									
MAX471		–	–	0 to 3 amps**	1.5 to 0/no load	+3 to +36	100µA (5µA SHDN)	Precision, high-side current-sense amplifier with internal sense resistor, measures charge and discharge	2 50
MAX472	60µV	–	–	–	1.5 to 0/no load	+3 to +36	100µA (5µA SHDN)	Precision, high-side current-sense amplifier	2 05
MAX4172	0 75	–	–	–	1.2 to 0/I_{OUT} ≤ 1.5mA	+3 to +32	1.6	Low-cost, precision, high-side current-sense amplifier	1 45

* External 39pF compensation capacitor added

** Sense resistor current range.

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Dual-Supply, Low-Power Op Amps

Part Number	V_{OS} (mV max)	I_{BIAS} (nA max)	Unity GBW (MHz)	V_{IN} Range (V_{CC-}_V) to (V_{EE+}_V)	V_{OUT} Swing/Load (V_{CC-}_V) to (V_{EE+}_V)/(Ω)	Supply Voltage (V)	Supply Current/ Op Amp (mA max)	Features	Price† 1000-up ($)
HIGH SPEED									
MAX400	10 to 15µV	2	0 4	1 to 1	3 to 3/1k	±3 to ±18	4	Ultra-low V_{OS} & drift, non-chopper stabilized	5.16
MAX402	2	5	2	1.2 to 1 2	1 1 to 1 1/20k	±3 to ±5	75µA	High speed, micropower	1 98
MAX403	2	25	10	1 2 to 1 2	1 4 to 1 4/4k	±3 to ±5	375µA	High speed, micropower	2 75
MAX410/412/414	1 typ (320µV MAX414)	150	28	1 3 to 1 2	1 3 to 1 2/2k	±2 4 to ±5.25	2.7	Single/dual/quad, high speed, low noise <2 4nV/√Hz at 1kHz guaranteed, unity-gain stable	1 50/2 45/4.50

Video/High-Speed Amplifiers

Part Number	-3dB BW (MHz)	Stable Gain (V/V)	0.1dB BW (MHz)	Slew Rate (V/µs)	V_{OUT} Swing/ Load (V/Ω)	DP/DG (deg./%)	Output Current (mA min)	Supply Voltage (V)	Supply Current per Ch. (mA)	Features	Price† 1000-up ($)
SINGLE-SUPPLY VIDEO/RF AMPLIFIERS											
MAX4012	200	+1	30	600	0 5 to 4 5/150	0.02/0 02	100	+3 3/+5 or ±5	5 5	Low-cost, SOT23, high-speed, single-supply amplifier	0 88
MAX4016	150	+1	30	600	0 5 to 4 5/150	0 02/0 02	100	+3 3/+5 or ±5	5 5	Low-cost, dual high-speed, single-supply amplifier	1 10
MAX4018	150	+1	30	600	0.5 to 4 5/150	0.02/0 02	100	+3 3/+5 or ±5	5 5	Low-cost, triple, high-speed, single-supply amplifier	1.80
MAX4020	150	+1	30	600	0 5 to 4 5/150	0 02/0 02	100	+3 3/+5 or ±5	5 5	Low-cost, quad, high-speed single-supply amplifier	2 05
MAX4212/4213	300	+1	50	600	0 5 to 4 5/150	0.02/0 02	100	+3 3/+5 or ±5	5 5	SOT23, high-speed, single-supply amplifiers, shutdown (MAX4213)	1 55
MAX4216	200	+1	35	600	0 5 to 4 5/150	0 02/0 02	100	+3 3/+5 or ±5	5 5	Dual, high-speed, single-supply amplifier	2 25
MAX4218	200	+1	35	600	0 5 to 4 5/150	0.02/0 02	100	+3.3/+5 or ±5	5 5	Triple, high-speed, single-supply amplifier with enable	2 98
MAX4220	200	+1	35	600	0 5 to 4 5/150	0 02/0 02	100	+3 3/+5 or ±5	5 5	Quad high-speed, single-supply amplifier	3 95
DUAL-SUPPLY VIDEO/RF AMPLIFIERS											
MAX404	40	+2	–	500	±8/50	0.01/0 05	50	±5	30	Broadcast-quality, low DP/DG symmetrical inputs, 70dB CMRR, 66dB A_{VOL}	2 68
MAX408/428/448	33	+3	–	90	±2 7/51		50/ op amp	±5	7/7 5/7 5	Single/dual/quad, high output drive	3 02/4 06/6 74
MAX435/436	275/200	+1	–	800	±3 5/500	–	10	±5	35	Ultra-fast differential input/output transconductance amp, no feedback required	2 75
MAX452	50	+1	–	300	±3/150	0 2/0 5	14	±5	25	Unity-gain stable drives 75Ω coaxial cable	2 40
MAX457	70	+1	–	300	±2 5/150	0 2/0 5	15	±5	17 5	Dual, unity-gain stable, drives 75Ω coaxial cable	4 45
MAX477	300	+1	130	1100	±3/100	0 01/0 01	70	±5	8	Voltage feedback, 130MHz 0 1dB gain flatness, drives 100pF C_{LOADS}	2 40
MAX4100/4101	500/200	+1/+2	65/50	250	±3 5/100	0 04/0 06, 0 04/0 07	65	±5	5	Low power, low cost, voltage feedback	1 95
MAX4102/4103	250/180	+1/+2	130/80	350	±3 4/100	0.002/0 002, 0 003/0 008	65	±5	4 6	Ultra-low differential phase/gain, broadcast quality	1 95
MAX4104/4105	880/430	+1/+5	95/100	400/1400	±3.5/100	0.02/0.02	70	±5	20	SOT23, ultra-high speed, low noise	1 70
MAX4106/4107	350/300	+5/+10	75/45	275/500	±3 5/100	0 02/0 04, 0 03/0 03	65	±5	15	0 75nV/√Hz ultra-low noise low distortion	3 88
MAX4108/4109	400/225	+1/+2	100/25	1200	+2 7 to -3.7/100	0.008/0 004	90	±5	20	Ultra-low distortion -93/-90dBc at 20MHz (SFDR)	3 88
MAX4112/4113	400/270	+2/+8	100/115	1200/ 1800	±3 5/100	0 03/0 02 0 04/0.02	80	±5	5	Low power low cost, current feedback	1 95
MAX4117/4118	400/300	+2/+8	100/115	1200/ 1800	±3 5/100	0 03/0 02 0.04/0.02	80	±5	5	Dual low power low cost current feedback 280/240MHz full-power bandwidth	2 65
MAX4119/4120	270/300	+2/+8	100/115	1200/ 1800	±3 5/100	0 03/0 02 0 04/0.02	80	±5	5	Quad low-power low-cost current feedback	3 95
MAX4180/4181	240/270	+2/+1	90/60	400	±3 2/150	0 03/0 08	50	+5 or ±5	1	Single, 1mA, high-speed SOT23 amplifier with shutdown	1 80
MAX4182/4183	340	+2	80	400	±3 2/150	0 03/0 08	50	+5 or ±5	1	Dual, 1mA high-speed amplifiers, shutdown (MAX4183)	2 80/2 90
MAX4184/4185	400	+1	60	400	±3 2/150	0.03/0.08	50	+5 or ±5	1	Dual, 1mA, high-speed amplifiers, shutdown (MAX4185)	2 80/2.90
MAX4186/4187	340/400	+2/+1	80/60	400	±3 2/150	0 03/0 08	50	+5 or ±5	1	Quad, 1mA high-speed amplifiers	3 65
MAX4188/4189	200	+1/+2	60	400	±3 2/150	0 03/0 08	90	+5 or ±5	1	Triple, 1mA, high-speed, low-glitch amplifiers	††

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†† Future product—contact factory for pricing and availability Specifications are preliminary.

Part Number	-3dB BW (MHz)	Min. Stable Gain (V/V)	0.1dB BW (MHz)	Slew Rate (V/µs)	VOUT Swing/ Load (V/Ω)	DP/DG (deg./%)	Output Current (mA min)	Supply Voltage (V)	Supply Current per Ch. (mA)	Features	Price† 1000-up ($)
DUAL-SUPPLY VIDEO/RF AMPLIFIERS (continued)											
MAX4190/4191	200	+1/+2	60	400	±3.2/150	0 03/0.08	90	+5 or ±5	1	Single, 1mA, high-speed, low-glitch amplifiers	††
MAX4223/4224	1000/600	+1/+2	300/200	1100/ 1700	+2 5	0 02/0 02	80	±5	6	SOT23, ultra-high-speed, low-power amplifiers with shutdown	2 15
MAX4225/4226	1000/600	+1	300	1100	+2 5	0 02/0 02	80	±5	6	Dual, ultra-high-speed, low-power amplifiers, shutdown (MAX4226)	3 45
MAX4227/4228	600	+2	200	1700	±2 5	0 02/0 02	80	±5	6	Dual, ultra-high-speed low-power amplifiers, shutdown (MAX4228)	3.45
MAX4304/4305	730/350	+2/+10	70/75	1000/ 1400	±3 5/100	0.02/0 02	70	±5	20	SOT23, ultra-high speed, low noise	1.70
MAX4308/4309	200/200	+5/+10	100/30	1200	+2 7 to -3.7/100	0.008/0 004	90	±5	20	Ultra-low distortion: -83dBc at 20MHz (SFDR)	3.88

Part Number	-3dB BW (MHz)	Gain (V/V)	0.1dB BW (MHz)	Slew Rate (V/µs)	VOUT Swing/ Load (V/Ω)	DP/DG (deg./%)	Output Current (mA min)	Supply Voltage (V)	Supply Current per Ch. (mA)	Features	Price† 1000-up ($)
SINGLE-SUPPLY VIDEO/RF BUFFERS											
MAX4014	200	+2	30	600	0 7 to 4 3/50	0 02/0 02	100	+3 3/+5 or ±5	5 5	Low-cost SOT23, high-speed, single-supply buffer	0 98
MAX4017	150	+2	30	600	0.7 to 4.3/50	0.02/0 02	100	+3.3/+5 or ±5	5.5	Low-cost, dual, high-speed, single-supply buffer	1.25
MAX4019	150	+2	30	600	0 7 to 4 3/50	0 02/0 02	100	+3 3/+5 or ±5	5 5	Low-cost, triple, high-speed, single-supply buffer with enable	1.95
MAX4022	150	+2	30	600	0.7 to 4.3/50	0 02/0 02	100	+3.3/+5 or ±5	5 5	Low-cost, quad, high-speed, single-supply buffer	2.25
MAX4214/4215	300	+2	50	600	0 7 to 4.3/50	0 02/0 02	100	+3 3/+5 or ±5	5.5	SOT23, high-speed, single-supply buffers, enable (MAX4215)	1.40/1 50
MAX4217	200	+2	50	600	0 7 to 4 3/50	0 02/0 02	100	+3 3/+5 or ±5	5 5	Dual, high-speed, single-supply buffer	2.05
MAX4219	200	+2	50	600	0.7 to 4.3/50	0.02/0.02	100	+3.3/+5 or ±5	5.5	Triple, high-speed, single-supply buffer with enable	2.80
MAX4222	200	+2	50	600	0 7 to 4.3/50	0 02/0 02	100	+3 3/+5 or ±5	5 5	Quad, high-speed, single-supply buffer	3.40

Part Number	-3dB BW (MHz)	Gain (V/V)	0.1dB BW (MHz)	Slew Rate (V/µs)	VOUT Swing/ Load (V/Ω)	DP/DG (deg./%)	Output Current (mA min)	Supply Voltage (V)	Supply Current per Ch. (mA)	Features	Price† 1000-up ($)
DUAL-SUPPLY VIDEO/RF BUFFERS											
MAX405	180	+0.99	–	650	±3 4/50	0.01/0.03	60	±5	35	Closed loop, 0 99V gain guaranteed over temp	4 25
MAX460	140	+0.99	–	1500	±9.8/100	–	90	±15	19	FET input, EL2005/LH0033 upgrade	19 78
MAX467	100	+1	–	200	±2.4/75	0.03/0 01	20	±5	17	Triple (RGB) video buffer, low DP/DG	3.70
MAX468	100	+1	–	200	±2.4/75	0.03/0.01	20	±5	16	Quad, unity-gain video buffer, low DP/DG	4.20
MAX469	90	+2	–	300	±2 4/75	0.14/0.12	20	±5	17	Triple (RGB), gain of +2 video buffer, low DP/DG	3.70
MAX470	90	+2	–	300	±2 4/75	0.14/0 12	20	±5	16	Quad, gain of +2 (6dB) video buffer, low DP/DG	4.20
MAX496	375	+1	80	1600	±3.3/50	0.01/0.01	66	±5	8	Quad, gain of +1 (0dB) closed-loop buffer, low DP/DG	4.95
MAX497	275	+2	120	1500	±3.3/50	0.01/0.01	66	±5	8	Quad, gain of +2 (6dB) closed-loop buffer, low DP/DG	4.95
MAX4005	950	+1	60	1000	+0 8 to -0 65/75	0.03/0.11	75Ω output	±5	24	FET input buffer with 75Ω output to minimize reflections, low DP/DG, 60MHz 0.1dB gain flatness, 28dBm IP3 (100MHz)	2.75
MAX4178	330	+1	150	1300	+2.5/50	0.01/0.04	70	+5	8	Closed loop, gain of +1 buffer, 150MHz 0.1dB gain flatness, low DP/DG	2.40
MAX4200/1/2	780	+1	280	4200	±3.7/100	0.15/1.3	80	±5	4	Single, SOT23, low power, 780MHz, open-loop buffers	1.70
MAX4203/4/5	720	+1	230	4200	±3.7/100	0.15/1.3	80	±5	4	Dual, low power, 720MHz, open-loop buffers	2.50
MAX4278	310	+2	150	1600	±2.5/50	0.01/0.04	70	±5	8	Closed loop, gain of +2 buffer, 150MHz 0.1dB gain flatness, low DP/DG	2.40
SINGLE-SUPPLY VIDEO MULTIPLEXERS/AMPLIFIERS											
MAX4310/4313	400/450	+1/+2	50	700/900	0 05 to 4.5/150	0.04/0.02	100	4 to 10, ±2 to ±5	6 5	2-channel, single-supply video mux amps with shutdown	††
MAX4311/4314	400/450	+1/+2	50	700/900	0.05 to 4.5/150	0.04/0.02	100	4 to 10, ±2 to ±5	6.5	4-channel, single-supply video mux amps with shutdown	††
MAX4312/4315	400/450	+1/+2	50	700/900	0.05 to 4.5/150	0.04/0.02	100	4 to 10, ±2 to ±5	6.5	8-channel, single-supply video mux amps with shutdown	††

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†† Future product—contact factory for pricing and availability. Specifications are preliminary.

Video/High-Speed Amplifiers (continued)

Part Number	-3dB BW (MHz)	Gain (V/V)	0.1dB BW (MHz)	Slew Rate (V/µs)	V_{OUT} Swing/ Load (V/Ω)	DP/DG (deg./%)	Output Current (mA min)	Supply Voltage (V)	Supply Current per Ch. (mA)	Features	Price† 1000-up ($)
DUAL-SUPPLY VIDEO MULTIPLEXERS/AMPLIFIERS											
MAX440	160	+1	–	370	±3/150	0.03/0.04	20	±5	40	Video amp with 8-channel mux, low DP/DG, 15ns switch time, high-Z output state	8.95
MAX441	160	+1	–	370	±3/150	0.03/0.04	20	±5	40	Video amp with 4-channel mux, low DP/DG, 15ns switch time	5.90
MAX442	140	+1	–	250	±3/75	0.09/0.07	33	±5	40	Video amp with 2-channel mux, 15ns switch time, 8-pin DIP/SO	4.45
MAX453	50	+1	–	300	±3/150	1.2/0.5	14	±5	25	Video amp with 2-channel video mux	3.94
MAX454	50	+1	–	300	±3/150	1.2/0.5	14	±5	25	Video amp with 4-channel video mux	5.25
MAX455	50	+1	–	300	±3/150	1.2/0.5	14	±5	25	Video amp with 8-channel video mux	8.75
MAX4111	330	+0.99	150	700	±2.5/5k	0.01/0.01	500µA	±5	4	1x1 video crosspoint building block, 150MHz 0.1dB gain flatness, low DP/DG	1.70
MAX4121	330	+0.99	150	700	±2.5/5k	0.01/0.01	500µA	±5	4	2x1 video crosspoint building block, 150MHz 0.1dB gain flatness, low DP/DG	2.10
MAX4141	330	+0.99	150	700	±2.5/5k	0.01/0.01	500µA	±5	4	4x1 video crosspoint building block, 150MHz 0.1dB gain flatness, low DP/DG	2.95
MAX4158	350	+1	100	700	±3.5/50	0.01/0.01	70	±5	11	2 inputs/1 output, current feedback, A_{VCL} ≥ 1V/V	2.30
MAX4159	350	+1	100	700	±3.5/50	0.01/0.01	70	±5	11	2 inputs/1 output, current feedback, A_{VCL} ≥ 1V/V, output enable	2.60
MAX4160/4260	350/250	+1/+2	100/130	700/1000	±3.5/50	0.01/0.01	100	±5	11	4-channel video mux amps	††
MAX4161/4261	350/250	+1/+2	100/130	700/1000	±3.5/50	0.01/0.01	100	±5	11	8-channel video mux amps	††
MAX4221	330	+0.99	150	700	±2.5/5k	0.01/0.01	500µA	±5	5	Dual 2x1 video crosspoint building block, 150MHz 0.1dB gain flatness, low DP/DG	4.50
MAX4258	250	+2	130	1000	±3.5/50	0.01/0.02	70	±5	11	2 inputs/1 output, current feedback, A_{VCL} ≥ 2V/V	2.30
MAX4259	250	+2	130	1000	±3.5/50	0.01/0.02	70	±5	11	2 inputs/1 output, current feedback, A_{VCL} ≥ 2V/V, output enable	2.60

Part Number	-3dB BW (MHz)	Buffer Amp Gain (V/V)	0.1dB BW (MHz)	Slew Rate (V/µs)	V_{OUT} Swing/ Load (V/Ω)	Switching Time (ns)	Number of Inputs	Number of Outputs	Output Current (mA)	EV Kit	Features	Price† 1000-up ($)
RGB VIDEO SWITCHES												
MAX463/465	100/90	+1/+2	–	300	±2.4/75	20	6 (RGB_A, RGB_B)	3 (RGB)	20		RGB switch with 75Ω cable drivers	6.97
MAX464/466	100/90	+1/+2	–	300	±2.4/75	20	8 (RGB_A + Sync, RGB_B + Sync)	4 (RGB + Sync)	20	Yes	RGB + sync switch with 75Ω cable drivers	7.97
MAX498	250	+2	70	1250	±3/100	3	8 (RGB_A + Sync, RGB_B + Sync)	4 (RGB + Sync)	40		Drives back-terminated 75Ω cables	4.40
MAX499	250	+2	70	1250	±3/100	3	6 (RGB_A, RGB_B)	3 (RGB)	40		Drives back-terminated 75Ω cables	3.50

Part Number	-3dB BW (MHz)	Min. Gain Stable (V/V)	0.1dB BW (MHz)	Slew Rate (V/µs)	V_{OUT} Swing/Load (V/Ω)	DP/DG (deg./%)	Output Current (mA)	Supply Voltage (V)	Supply Current per Ch. (mA)	Features	Price† 1000-up ($)
DISTRIBUTION AMPLIFIERS											
MAX4135	185	+2	40	1000	+2.6 to -2.4/150	0.02/0.09	70	±5	45	1 input/6 outputs, fixed gain of 2V/V, high-impedance outputs in shutdown, outputs can be individually enabled/disabled	5.90
MAX4136	140	+2	40	1000	+2.6 to -2.4/150	0.03/0.12	70	±5	45	1 input/6 outputs, external gain set, high-impedance outputs in shutdown, outputs can be individually enabled/disabled	5.90
MAX4137	185	+2	40	1000	+2.6 to -2.4/150	0.02/0.10	70	±5	30	1 input/4 outputs, fixed gain of 2V/V, high-impedance outputs in shutdown, outputs can be individually enabled/disabled	4.50
MAX4138	140	+2	40	1000	+2.6 to -2.4/150	0.02/0.10	70	±5	30	1 input/4 outputs, external gain set, high-impedance outputs in shutdown, outputs can be individually enabled/disabled	4.50

Part Number	-3dB BW (MHz)	Gain (V/V)	0.1dB BW (MHz)	Slew Rate (V/µs)	V_{OUT} Swing/Load (V/Ω)	DP/DG (deg./%)	Output Current (mA)	Supply Voltage (V)	Supply Current per Ch. (mA)	Features	Price† 1000-up ($)
DIFFERENTIAL LINE DRIVERS											
MAX4142	300	+2	70	2000	±6/100	0.03/0.008	80	±5	12	Fixed gain of +2V/V, high output drive	††
MAX4147	300	+2	70	2000	±5.6/53	0.01/0.008	160	±5	10	Fixed gain of +2V/V, high output drive	2.50
HIGH-SPEED LINE RECEIVERS											
MAX4144	130	+2	30	1000	±2.6/150	0.03/0.03	50	±5	13	Fixed gain of +2V/V, differential input/single-ended output	3.35
MAX4145	70	+100	10	800	±2.6/150	0.07/0.12	50	±5	13	External gain set +10V/V to +100V/V, low 3.5nV/√Hz noise, differential input/single-ended output	2.40
MAX4146	70	+10	10	800	±2.6/150	0.07/0.12	50	±5	13	External gain set +1V/V to +10V/V, low 3.5nV/√Hz noise, differential input/single-ended output	2.40

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Video/High-Speed Amplifiers (continued)

Part Number	-3dB BW (MHz)	Min. Stable Gain (V/V)	0.1dB BW (MHz)	Slew Rate (V/µs)	V_{OUT} Swing/ Load (V/Ω)	DP/DG (deg./%)	Off Isolation (dB)	Crosstalk (dB)	EV Kit	Features	Price† 1000-up ($)
VIDEO CROSSPOINT SWITCHES											
MAX456	35	+1	–	250	±1.3/0	1/0.5	80 (5MHz)	-70 (5MHz)		8x8 crosspoint switch array with eight output buffers, high-Z output	19 98
MAX458/459	100/90	+1/+2	–	200/300	±3/150	0.05/0.01	60 (10MHz)	-55 (10MHz)	Yes	8x4 crosspoint switch array with four 75Ω cable drivers, high-Z output	21.85
MAX4111	330	+0 99	150	700	±2.5/5k	0 01/0.01	86 (30MHz)	–	Yes	1x1 video crosspoint building block, 0 1dB gain flatness of 150MHz	1.70
MAX4121	330	+0.99	150	700	±2.5/5k	0.01/0.01	78 (30MHz)	-92 (30MHz)	Yes	2x1 video crosspoint building block, 0 1dB gain flatness of 150MHz	2.10
MAX4141	330	+0 99	150	700	±2 5/5k	0 01/0.01	74 (30MHz)	-66 (30MHz)	Yes	4x1 video crosspoint building block, 0.1dB gain flatness of 150MHz	2.95
MAX4221	330	+0 99	150	700	±2 5/5k	0.01/0.01	84 (30MHz)	-70 (30MHz)	Yes	Dual 2x1 video crosspoint building block, 0 1dB gain flatness of 150MHz	2.95

Comparators

Part Number	Comps. per Pkg.	Input Offset Voltage (mV)	V_{IN} Range (V_{CC}-_V) to (V_{EE}+_V)	Logic	Latched Outputs	Complementary Outputs	Supply Voltage (V)	Supply Current per Comp. (mA max)	t_{PD} (ns)	Features	Price† 1000-up ($)
HIGH SPEED											
MAX900	4	0.5	2.25 to -0 1	TTL	Yes	No	+5 to +10, ±5	4 (I_{CC})	8	Single +5V capability, low power, CMVR extends to neg. rail, separate analog & digital supplies, internal pull-up resistors	7.01
MAX901	4	0.5	2.25 to -0.1	TTL	No	No	+5 to +10, ±5	4 (I_{CC})	8	MAX900 without output latch	5 23
MAX902	2	1	2.25 to -0 1	TTL	Yes	No	+5 to +10, ±5	4 (I_{CC})	8	Dual MAX900	4.01
MAX903	1	1	2 25 to -0 1	TTL	Yes	No	+5 to +10, ±5	4 (I_{CC})	8	Single MAX900	3 15
MAX905	1	0 5	2 2 to -0.1	ECL	Yes	Yes	-5 or ±5	24 (I_{EE})	1 8	Edge-triggered master/slave architecture eliminates oscillations and resolves 3mV input voltages, also operates with -5.2V or +5V, -5 2V ECL supplies	3.54
MAX906	2	0 5	2 2 to -0.1	ECL	Yes	Yes	-5 or ±5	24 (I_{EE})	1.8	Dual MAX905, also operates with -5 2V or +5V, -5 2V ECL supplies	5.23
MAX907	2	0 5	1 5 to -0 2	TTL	No	No	+4 5 to +5 5	1	30	High speed, ultra-low power, single +5V, 8-pin DIP/SO, built-in hysteresis	1 70
MAX908	4	0 5	1.5 to -0.2	TTL	No	No	+4 5 to +5.5	1	30	High speed, ultra-low power, single +5V, 14-pin DIP/SO, built-in hysteresis	2.95
MAX909	1	0 5	1 5 to -0.2	TTL	Yes	Yes	+4 5 to +5 5, ±5	1 8	30	High speed, low power, single or dual supply, input range includes ground, complementary outputs	1 50
MAX910	1	1	2 to 2	TTL	Yes	No	±5 or +5, -5 2	30 (I_{CC})	8	TTL-compatible, 8-bit digitally programmable input voltage threshold, on-board reference	5.20
MAX912	2	0 8	1.5 to -0.2	TTL	Yes	Yes	+5 or ±5	10	10	Dual MAX913	3.90
MAX913	1	0.8	1 5 to -0.2	TTL	Yes	Yes	+5 or ±5	10	10	Lowest power 10ns comparator with complementary outputs single/dual supply, CMVR extends below ground to V+ - 1.5V	2.55
MAX915	1	0 5	2.2 to -0.1	TTL	Yes	Yes	+5 or ±5	18 (I_{CC})	6	No oscillations, master/slave, clocked	2.55
MAX941	1	1	-0.2 to -0.2	TTL/CMOS	Yes	No	+2 7 to +6	600µA	75	Low power, 3V or 5V single supply, rail-to-rail inputs (5µA SHDN)	1.40
MAX942	2	1	-0 2 to -0.2	TTL/CMOS	No	No	+2 7 to +6	600µA	75	Dual MAX941, 8-pin DIP/SO	1.50
MAX944	4	1	-0.2 to -0.2	TTL/CMOS	No	No	+2 7 to +6	600µA	75	Quad MAX941	2.50
MAX961	1	0.5	-0.1 to -0 1	TTL/CMOS	Yes	Yes	+2 7 to +5.5	11	4.5	High speed, internal hysteresis, rail-to-rail inputs, shutdown mode	2.50
MAX962	2	0 5	-0 1 to -0.1	TTL/CMOS	No	No	+2 7 to +5.5	8	4 5	Dual, internal hysteresis, rail-to-rail inputs	3.35
MAX963	2	0 5	-0.1 to -0 1	TTL/CMOS	Yes	Yes	+2 7 to +5.5	11	4.5	Dual, internal hysteresis, rail-to-rail inputs, shutdown mode	3.35
MAX964	4	0 5	-0 1 to -0 1	TTL/CMOS	No	No	+2 7 to +5.5	8	4 5	Quad, internal hysteresis, rail-to-rail inputs, shutdown mode	5.50
MAX976	2	0.2	1.2 to -0.2	TTL/CMOS	No	No	+2.7 to +5.5	600µA	20	Dual, high speed, 3V/5V	2.05
MAX978	4	0 2	1 2 to -0.2	TTL/CMOS	No	No	+2 7 to +5.5	600µA	20	Quad, high speed, 3V/5V	3 10
MAX997	1	0.5	-0.1 to -0.1	TTL/CMOS	No	No	+2.7 to +5.5	6.5	5	SOT23, high speed, internal hysteresis, rail-to-rail inputs	2.15
MAX998	1	0 2	1.2 to -0 2	TTL/CMOS	No	No	+2.7 to +5.5	600µA	20	Single, high speed, 3V/5V, available in SOT23-6 with shutdown	1.70
MAX999	1	0.5	-0.1 to -0 1	TTL/CMOS	No	No	+2 7 to +5.5	6 5	5	Single, high speed, 3V/5V, available in SOT23-5	1.97
MXL1016	1	0.8	1.5 to 1.25	TTL	Yes	Yes	+5 or ±5	35 (I_{CC})	10	High speed, complementary outputs, LT1016 second source	1.92
MXL1116	1	1	2.5 to 0	TTL	Yes	Yes	+5 or ±5	38 (I_{CC})	12	High speed, single supply, complementary outputs, LT1116 second source	1.92

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Part Number	Comps. per Pkg.	Input Offset Voltage (mV max)	V_{IN} Range (V_{CC}-_V) to (V_{EE}+_V)	Logic	Latched Outputs	Comple-mentary Outputs	Supply Voltage (V)	Supply Current per Comp. (mA max)	t_{PD} (ns)	Features	Price† 1000-up ($)
MICROPOWER											
MAX921/971	1 + ref	10	1.3 to 0	TTL/CMOS/ open drain	No	No	+2.5 to +11, ±1.25 to ±5	3.2μA (total pkg.)	12μs	Micropower comparator + 1% reference & hysteresis, single-supply capability, CMVR extends to GND	1.50/1.50
MAX922/972	2	10	1.3 to 0	TTL/CMOS/ open drain	No	No	+2.5 to +11, ±1.25 to ±5	3.2μA (total pkg.)	12μs	Dual, single-supply micropower comparator in 8-pin DIP/SO	0.98/0.98
MAX923/973	2 + ref	10	1.3 to 0	TTL/CMOS/ open drain	No	No	+2.5 to +11, ±1.25 to ±5	4.5μA (total pkg.)	12μs	Dual, single-supply comparator with 1% voltage reference in 8-pin DIP/SO	1.95/1.95
MAX924/974	4 + ref	10	1.3 to 0	TTL/CMOS/ open drain	No	No	+2.5 to +11, ±1.25 to ±5	6.5μA (total pkg.)	12μs	Quad, micropower comparator with 1% voltage reference	2.25/2.25
MAX931/981	1 + ref	10	1.3 to 0	TTL/CMOS/ open drain	No	No	+2.5 to +11, ±1.25 to ±5	3.2μA (total pkg.)	12μs	Low-cost comparator + 2% reference & hysteresis, single-supply, CMVR extends to GND	0.98/0.98
MAX932/982	2 + ref	10	1.3 to 0	TTL/CMOS/ open drain	No	No	+2.5 to +11, ±1.25 to ±5	4.5μA (total pkg.)	12μs	Dual, low-cost, single-supply comparator + 2% reference & hysteresis in 8-pin DIP/SO	1.26/1.26
MAX933/983	2 + ref	10	1.3 to 0	TTL/CMOS/ open drain	No	No	+2.5 to +11, ±1.25 to ±5	4.5μA (total pkg.)	12μs	Dual, low-cost, single-supply comparator + 2% reference & hysteresis in 8-pin DIP/SO (window comparator input configuration)	1.26/1.26
MAX934/984	4 + ref	10	1.3 to 0	TTL/CMOS/ open drain	No	No	+2.5 to +11, ±1.25 to ±5	6.5μA (total pkg.)	12μs	Quad, low-cost comparator + 2%-accurate reference, single/dual supply	1.31/1.31
MAX965	1 + ref	3	-0.25 to -0.25	Open drain	No	No	+1.6 to +5.5	12μA	10μs	Single, rail-to-rail I/O, operates down to 1.6V, has 1.22V internal ref.	1.05
MAX966	2	3	-0.25 to -0.25	Open drain	No	No	+1.6 to +5.5	5μA	10μs	Dual, rail-to-rail I/O, operates down to 1.6V	1.05
MAX967/968	2 + ref	3	-0.25 to -0.25	Open drain	No	No	+1.6 to +5.5	8μA	10μs	Dual, rail-to-rail I/O, operates down to 1.6V, has 1.22V internal ref.	1.30
MAX969	4 + ref	3	-0.25 to -0.25	Open drain	No	No	+1.6 to +5.5	5.5μA	10μs	Quad, rail-to-rail I/O, operates down to 1.6V, has 1.22V internal ref.	1.95
MAX970	4	3	-0.25 to -0.25	Open drain	No	No	+1.6 to +5.5	4.5μA	10μs	Quad, rail-to-rail I/O, operates down to 1.6V	1.60
MAX985–998	1	5	-0.25 to -0.25	TTL/CMOS/ open drain	No	No	+2.5 to +5.5	20μA/80μA	300/120	Single, rail-to-rail I/O, single-supply operation, available in SOT23-5	0.66
MAX989–992	2	5	-0.25 to -0.25	TTL/CMOS/ open drain	No	No	+2.5 to +5.5	20μA/80μA	300/120	Dual, rail-to-rail I/O, single-supply operation	1.05
MAX993–996	4	5	-0.25 to -0.25	TTL/CMOS/ open drain	No	No	+2.5 to +5.5	20μA/80μA	300/120	Quad, rail-to-rail I/O, single-supply operation	1.58
OP AMP + COMPARATOR + REFERENCE ICs											
MAX516	4	4.9*	0 to 0	TTL/CMOS	No	No	+4.75 to +16.5	10.01 (total pkg.)	800	Quad comparator + quad 8-bit DAC for independent threshold setting, single-supply capability, rail-to-rail input voltage ranges	3.00
MAX910	1	1	2 to 2	TTL	Yes	No	±5 or +5, -5.2	30 (I_{CC})	8	TTL-compatible, 8-bit digitally programmable input voltage-threshold, on-board reference	5.20
MAX951–954	(See Single-Supply, Low-Power Op Amp section for tables)										–
MAX975	1	0.2	1.2 to -0.2	TTL/CMOS	No	No	+2.7 to +5.25	0.300 (high speed), 0.003 (low power)	28 (high speed), 480 (low power)	Dual speed, automatically switches from high-speed comparator to low-power comparator	1.95
MAX977	2	0.2	1.2 to -0.2	TTL/CMOS	No	No	+2.7 to +5.25	0.300 (high speed), 0.003 (low power)	28 (high speed), 480 (low power)	Dual speed, automatically switches from high-speed comparator to low-power comparator	3.50
MAX9000–9005	(See Single-Supply, Low-Power Op Amp section for tables)										–

* Total unadjusted error equals ±1LSB (max).

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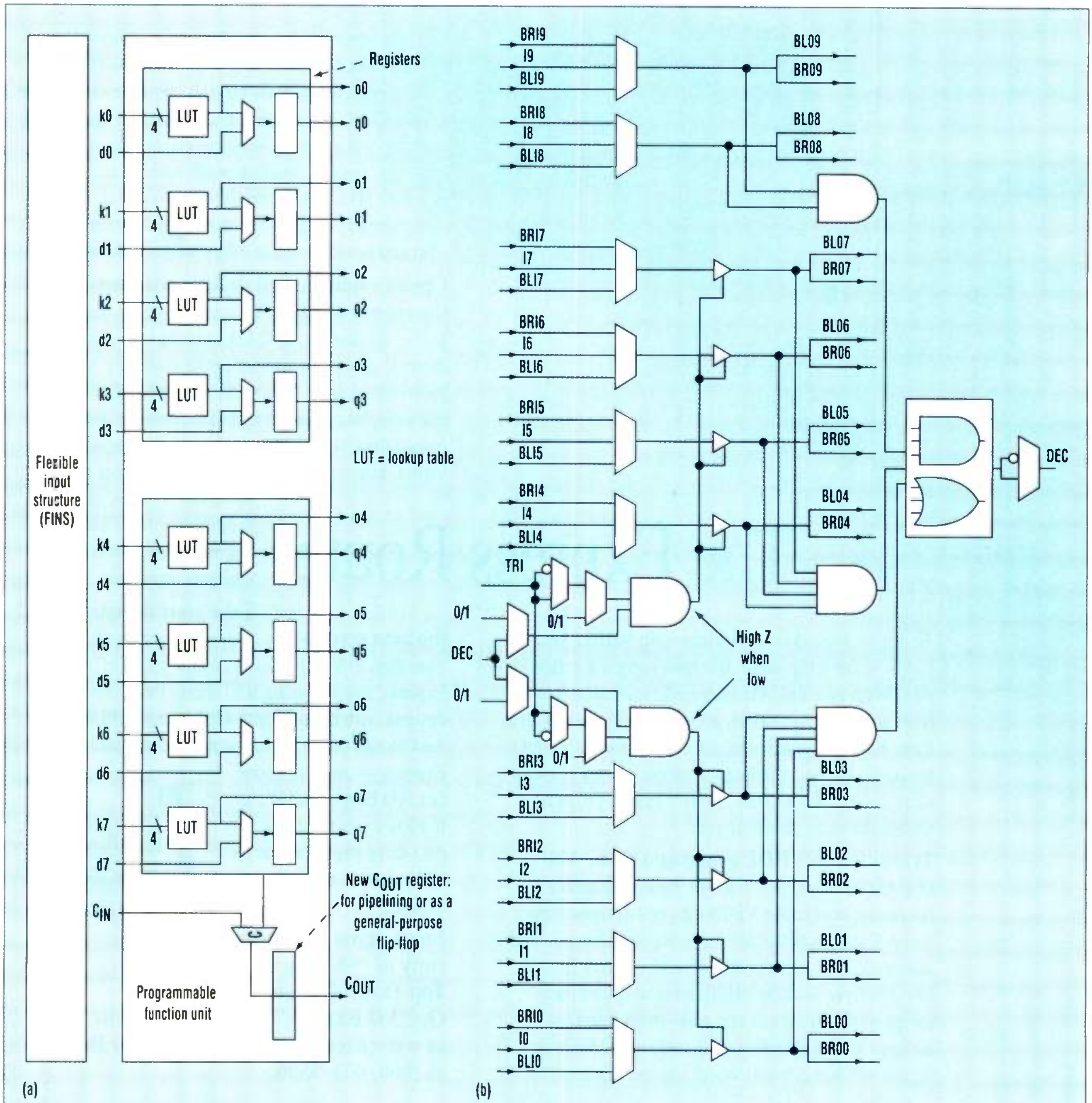
(PFU), routing resources, and a supplemental logic and interconnect cell (SLIC) that includes a new decoder and PAL-like logic. This creates a family that blurs the distinction between FPGAs and complex PLDs *(Fig. 2)*.

Such a combination should give designers more flexibility to implement complex logic functions. Within the programmable function unit is a pair of quadruple four-input lookup-table (LUT) blocks that can be configured for nibble- or byte-wide datapaths. Enhanced routing capabilities such as diagonal routing and Express Clock routing for global signals provide additional design flexibility and improved performance.

Each quadruple block contains four, four-input (16-bit) LUTs and four latches/flip-flops. Two blocks plus an additional flip-flop and a 32-word-by-4-bit RAM (or a ROM for production) to hold the configuration data or serve as static RAM, are included in the full PFU. Local routing resources between LUT functions allow fast, programma-



2. The main logic element of the ORCA Series 3 FPGAs from Lucent Technologies is the Twin-Quad programmable function unit. It contains two groups of four-input lookup table logic blocks (a). The PFU also includes a new C_{OUT} register that can be used for pipelining, or as a general-purpose flip-flop. Adding some PAL- like functionality and wide-decode capability to the FPGAs, the supplemental logic and interconnect cell (SLIC) performs both logic and interconnect functions (b). Ten bidirectional buffers are divided into two groups of four (all three-state capable) and a third group of two buffers for control. The SLIC also can implement a PAL-like decoder with up to 10 inputs using AND-OR functions, a wide logical OR, or a decoder of up to 10 bits.

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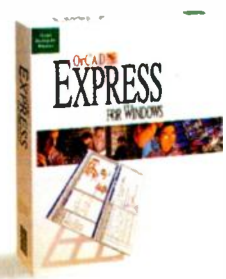

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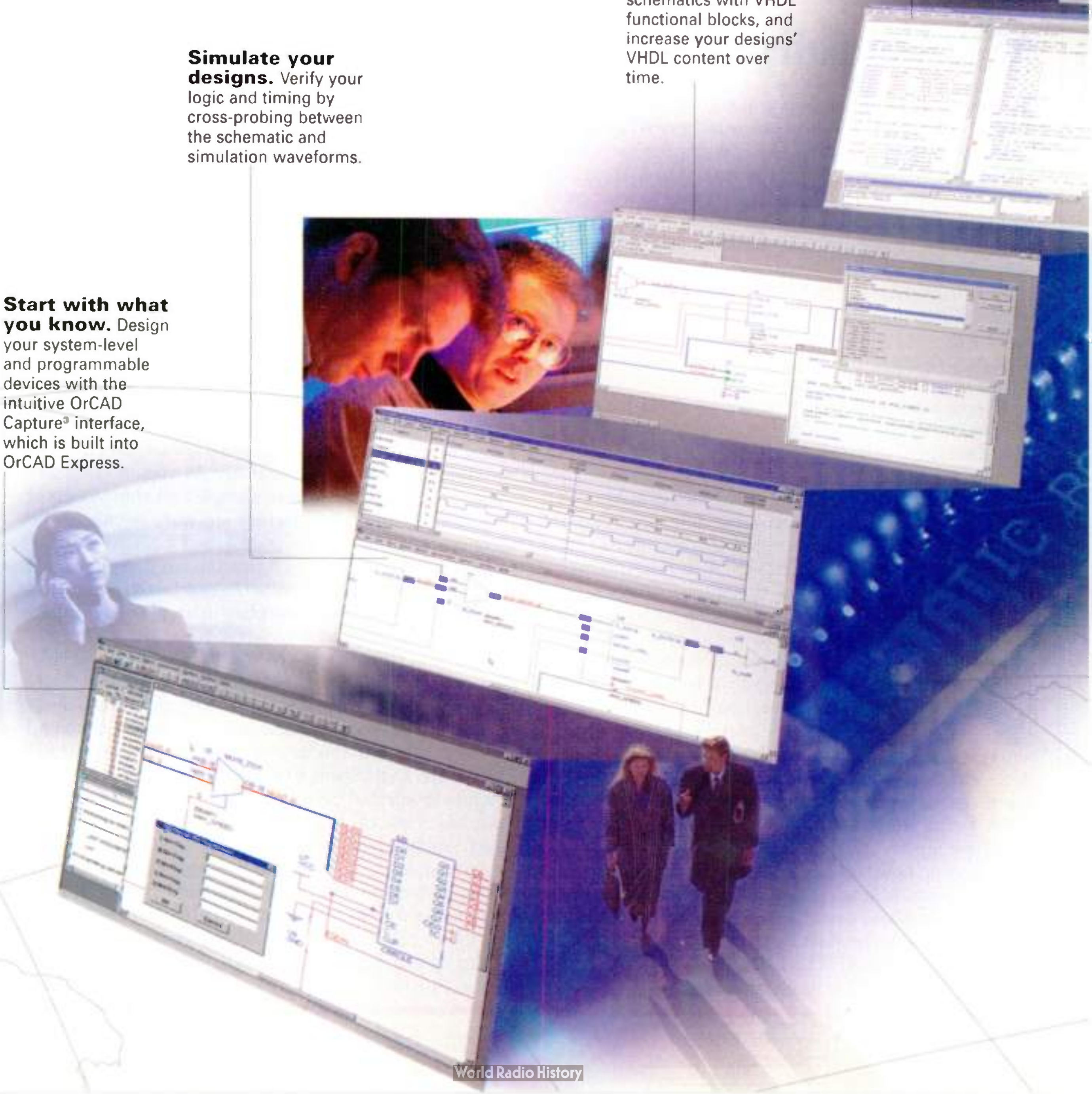

pieces. Although the prices are higher than the gate-array per-unit prices, there are no nonrecurring engineering charges, no chips to scrap if the configuration changes, and so on.

The next-generation of programmable logic now on the drawing boards at Altera—the Raphael family—will include devices that pack up to 2 Mgates, and will combine both product term and FPGA architectures on one chip. Initially, chips in the family will be fabricated in the company's 0.25-µm process, but that will transition quickly to a 0.18-µm technology. Such chips will allow system operation at speeds of over 100 MHz and internal clock speeds of about 400 MHz.

Initially available with gate capacities of up to 125 kgates, the ORCA Series 3 FPGAs from Lucent are the next step in the evolution of the ORCA family. There will actually be two versions of the Series 3 family. First, there's the 3Cxx, which will offer 5-V interfaces and complexities of up to 80 kgates while operating at system clock speeds of over 90 MHz. The other is the 3Txxx series of 3.3-V devices, which can pack up to 225 kgates and operate at system speeds of over 120 MHz.

The 3C series will be fabricated on a 0.35-µm process with four levels of metal interconnect, while the 3T series will be made on a 0.25-µm process containing five levels of metal to achieve the higher performance and density. All chips will include IEEE-1149.1 boundary-scan logic and special system-level features, such as a microprocessor interface that supports both Intel i960- and Motorola/IBM PowerPC-style bus interfaces, and a pair of programmable clock managers.

Merging Features

Each logic block in the array consists of a programmable function unit

ASIC Alternatives

It's virtually a unanimous concession that FPGAs, CPLDs and PLDs are ideal products for developing prototype system hardware and employing for low-volume production. What few companies can agree on, though, is when the design should be converted over to what most companies feel is a lower-cost alternative—a gate array or some other more-integrated solution such as a standard-cell or full-custom chip. The volume numbers most companies are bandying back and forth seem to be in the 10,000- to 20,000-unit quantities. When production volumes reach that range, it's time to consider lowering manufacturing cost, particularly if the system volume is expected to increase, or the design is extremely stable.

Although individual chip prices will usually be lower over the lifetime of the ASIC solution, there are several negatives associated with gate-array or cell-based solutions. For starters, most ASIC manufacturers have a nonrecurring engineering (NRE) fee associated with the initial startup cost, a fee that must be amortized across the entire product run of chips (however that fee can be negotiated down if production volumes are high enough). And with ASIC manufacturing being a rather lengthy process—typically 6 to 10 weeks—if a problem is found after the manufacturing begins, all of the chips in the pipeline will have to be scrapped. The cost of those chips will be distributed across all viable chips.

Perhaps one of the larger negatives is that most FPGA to ASIC conversions aren't "pushbutton" processes. Designers often are faced with lots of redesign, resimulation, and resynthesis of their circuits. A few companies, such as American Microsystems, Orbit Semiconductor, Chip Express, as well as all mainstream gate-array suppliers, have software utilities to help in the conversion. But engineers may typically have to spend months redoing their designs and creating new test vectors to obtain that lower-cost ASIC implementation. Furthermore, the short product lifecycle also places designers on the hot seat. That's because any delay in product ramp up due to lengthy ASIC conversion times could cause a miss on the market window. That, of course, would damage product sales.

FPGA suppliers, in many cases, do offer a metal-mask programmed version of their FPGAs, which for really firm designs can provide a first-level solution to obtaining lower-cost production volume components. One alternative to the conversion headache is emerging from the ASIC world through a company called ClearLogic. It developed an architecture-specific gate array—a laser-programmable gate array whose architecture mimics the architecture of the FLEX 8000 programmable logic chips from Altera. In lots of 100 units, ClearLogic expects to sell a configured CL8452A, 160-pin device, for $14.50—about 20 to 50% lower than the price of the 4000-gate FLEX 8000 device it replaces.

The software that controls the proprietary laser-configuration system allows FLEX 8000 designs to be transferred directly with no redesign or resynthesis. Furthermore, the company can configure as few as just one chip, and charges no NRE on the transfer. As a result, designers can order any quantity, from a single test chip to tens of thousands of units. Proprietary software developed by ClearLogic will automatically take the FLEX 8000 configuration bit stream, convert it into the laser-configuration file, and automatically generate the new test-vector file, allowing the conversion to take place in hours to days rather than weeks and months.

If several FPGAs must be consolidated in to one chip, designers at LightSpeed Semiconductor, another fairly new company, have come up with a fast turnaround alternative for a gate-array-like solution. It provides several masterslices, with the largest initial offering about 375 kgates. The LightSpeed COSMIC (cycle-optimized sea of modules integrated circuit) array family has two unusual features. First there's the single-mask-programming, which will keep the turnaround time from approved net list to samples to just one week or less. Second, the AutoTest embedded test circuits offer 100% stuck-at fault coverage, which eases the task of creating the test vectors, thus shortening the time to complete the design. For the 275-kgate member, volume pricing will be about $50/unit in lots of 10,000.

ble connections to be made between the eight LUTs and SLICs, improving speed by as much as 40% versus the previous Series 2 devices.

SLICs also can act as RAM bank drivers to allow large blocks of RAM to be created without sacrificing performance—single- and dual-ported memories can operate at speeds greater than 175 MHz. Flexible I/O cells contain a fast capture latch on the input. They provide two output flip-flops and a buffer similar to that used in the previous 2C/2T family, but with a fast, open-drain option for dealing with system buses. A chip like the 3T55, which packs about 80 kgates and comes in a 208-lead power shrink quad-sided flat package, will sell for $71.90 each in lots of 25,000 units by the end of 1998.

The ORCA Foundry release 9.2, which supports gate-array design methodologies, includes true RC skew analysis and multicycle timing capability, timing-driven placement and routing, an interactive layout editor, and static timing analysis, among other features. The Foundry software is compatible with industry standards such as EDIF, VHDL, Verilog, and SDF, and can integrate easily with tools from other suppliers.

Xilinx attempts to tackle both the high- and medium density levels with its two latest families of SRAM-based FPGAs. The Virtex high-density family, unveiled last fall, is made on a 0.25-µm, five-level metal process that delivers capacities up to 500,000 "system gates" (20,000 logic cells) per chip, and allows operation from 2.5 V and 3.3 V for the I/O (ELECTRONIC DESIGN, *Nov. 17, 1997, p. 67*). The other, moderate-density series—the Spartan family—was introduced earlier this year and provides up to about 40,000 system gates (ELECTRONIC DESIGN, *Feb. 23, p. 98*).

The first implementation of the Spartan series will employ a hybrid set of design rules—0.5-µm./0.35-µm features—with a three-level metal process so that it can operate from 5 V. This coming fall, a second version of the family, fabricated with a tighter set of hybrid design rules—0.35/0.25 µm—will allow 3.3-V I/Os while operating internally from 2.5 V.

The initial Virtex series, the XC4000XV, will top out at 500 kgates with operating speeds of over 100 MHz.

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*Many gate-array/ASIC suppliers not listed in this table also supply conversion services and/or tools

By late 1998, however, Xilinx expects to sample devices with capacities of one million gates and be able to clock at speeds of over 150 MHz. In addition to the logic cells that each contain the equivalent of one four-input LUT building block and one register, the FPGAs include dedicated blocks of embedded SRAM—from 8 to 30 blocks of 4 kbits each. The blocks can be configured in various word width/depth combinations to form larger memory arrays.

The Spartan XCSxxx family is based on the company's popular XC4000 architecture. Thanks to process improvements, design layout, and a reduction in power consumption, the new devices will operate with system speeds of up to 80 MHz (internal performance to exceed 150 MHz).

The smaller chip sizes will allow the lower-complexity devices such as the 5000-gate XCS05 to sell for less than $4 in large volume by late 1998 . To reduce the size and cost of the chip, designers at Xilinx removed some the XC4000-series features that most customers didn't use. But to make the chips less expensive to test, they added some new circuits for built-in self test functions. Unlike the Virtex series, the Spartan devices don't have dedicated blocks of SRAM. Instead, they use the small SRAMs in each LUT to form from 3200 to 25,088 bits of memory, which can be used in almost any combination.

New Players Welcome

DynaChip, a newcomer to the CMOS FPGA market, has just released what it claims is the highest-speed family of SRAM-based FPGAs. The DL6000 family can support clock rates up to 250 MHz and operates in systems with bus speeds exceeding 100 MHz. Based on a proprietary active repeater embedded in the interconnect channels, the arrays deliver gate-array-like performance and are available in versions with densities that range from 9000 to 105,000 gates.

Like the high-speed gate arrays it's intended to replace, the DL6000 architecture allows the creation of high-speed memory blocks with sub-8-ns access times and supports a variety of fast interface options. Each I/O pin can be configured for LV-TTL or GTL interfaces. The chips also have several PLLs that can be used to remove clock-buffer latency and divide or multiply incoming clocks by factors of two, three, four, six, or eight.

Prior tot he DL6000 family, DynaChip unveiled a high-speed family of FPGAs—the DL5000 series. These are the only biCMOS FPGAs in the industry and can support clock and data rates of up to 270 MHz. Chip densities in the family are much lower than in the DL6000 series—the first devices pack just 1250, 5000, and 10,000 gates. However, the circuits also use the active repeater technology and can achieve internal operating speeds of 140 MHz for a 32-bit fully synchronous counter or 200 MHz for a 24-bit adder/accumulator (ELECTRONIC DESIGN, *Nov. 3, 1997, p.72)*.

Although not newcomers to programmable logic, both Atmel and Vantis (an Advanced Micro Devices subsidiary) have debuted into the realm of high-density SRAM-based FPGAs. Introduced last fall, Atmel's AT40K family offers several novel features, including diagonal connections between logic cells to achieve improved routing (ELECTRONIC DESIGN, *November 3, 1997, p. 46)*. The arrays are dynamically reconfigurable so that logic configuration updates can be made even during system operation.

Discrete blocks of SRAM, organized as 32-word-by-4-bit arrays, are located at the corners of each eight-ported logic cell. Because those blocks don't take away any capability from the logic function, they give the designer abundant resources for memory-rich applications. The distributed memory ranges from 2048 bits for the 5-kgate AT40K05, to over 18,000 bits for the 40-kgate AT40K40.

The VF1 series developed by Vantis also focuses on the high-performance end of the FPGA realm, putting the family into direct competition with some gate-array families. Based on a 0.18-µm, four-layer-metal process, the arrays will permit memory blocks to operate at pipeline speeds of 250 MHz.

The family will initially include devices with capacities from 12 up to 36 kgates (functionally equivalent to 50 kgates if on-chip memory is included) and 3584 to 6144 bits of SRAM. The architecture can be extended to future chips that pack up to 250 kgates and 64 kbits of memory using the same process rules.

By the end of the century, Vantis expects its next process with even smaller gate lengths. Also, a fifth level of metal interconnections will make possible FPGAs with capacities of over half-a-million gates, 128 kbits of RAM, and over 800 I/O lines.

Unveiled earlier this year, the VF1 series employs a variable-grain architecture. The arrays can deliver speeds that are 50 to 100% faster than most other RAM-based FPGAs (ELECTRONIC DESIGN, *Feb. 23, p. 102)*. Some of that performance increase can be attributed to the use of a shallow-trench isolation scheme. It isolates the adjacent n- and p-type wells, permitting high packing densities and minimal parasitics.

The variable-grain architecture consists of three levels. At the lowest level is the configurable building block, which consists of dual three-input LUTs, multiplexers, a register, and the configuration/interface logic. The next higher level consists of the variable-grain blocks. These each contain four configurable building blocks and special wide gating that allows users to combine two or more configurable building blocks into more complex functions. At the top level are the super-variable grain blocks, each containing four variable grain blocks. Those blocks can be combined to form even more-complex functions. The VF1 series also includes a large pool of signal routing resources that provide for many local interconnection options as well as global-routing resources.

Although not at the 100-kgate level yet, Motorola's MPA1000 series of FPGAs provides devices with capacities ranging from 3500 to 22,000 gates. Even more interesting is the movement by Motorola to combine the FPGA architecture and a microcontroller core on the same chip to provide a highly flexible system solution.

Last year, both Actel and Lucent Technologies also announced they would start designing selected FPGA chips that include dedicated function blocks, such as a PCI core, prediffused in the silicon. The need for such a solution is two-fold. First, it allows the silicon vendor to guarantee the core's performance since it's "prefabricated." Second, it reduces the area occupied by the core, making the chip smaller or allowing FPGA suppliers to put new functions on the chip.

Touting its fine-grain architecture as a very close match to gate-array design

approaches, GateField's ProASIC GF260F family delivers programmable silicon with maximum capacities of 310,000 equivalent gate-array gates. The GF260F family, introduced last fall, complements the company's previously released GF250F "gate only" products. It provides designers with up to 46,000 bits of programmable memory optimized for use in single- and dual-port configurations , as well as for FIFO buffers (ELECTRONIC DESIGN, *Dec. 1, 1997, p. 68)*. Based on nonvolatile flash-memory cells rather than SRAMs cells, the chips do away with the external configuration memory or boot cycles required by SRAM-based FPGAs. Thus the GF250/260 series products can offer "instant on" capabilities once the configuration pattern is stored on the chip.

The fine-grained architecture of the GF260 allows design tools to deal with the family as if the chips were based on gate-array cells. Thus, anyone familiar with the gate-array design flow can leverage that experience to quickly get up to speed and start implementing their design on the ProASIC arrays. Designers can employ the same robust VHDL or Verilog HDL descriptions targeted for gate arrays and standard-cell-based chips. Circuits are synthesized using GateField's libraries and can then be simulated, have their timing analyzed, and then be placed and routed using the company's ASICmaster software.

Small but fast probably best define the ispLSI31xx family of in-system programmable, flash-memory-based, programmable-logic devices from Lattice Semiconductor. The largest family member is the ispLSI3448, which packs up to 20,000 gates and 224 universal I/O pins. The chip is available in 70- and 90-MHz speeds. Other family members include the just-released 14-kgate ispLSI3220 devices that come in a 208-lead metal QFP, and several other lower-density devices.

Dense Antifuse Arrays

Actel has always felt its antifuse-based, fine-grain ACT products were very much like gate arrays, because the chips employ a relatively small programmable cell. The latest products, unveiled last fall, include the MX family with members packing 2000 to 52,000 gates, and the just-released SX family, which includes arrays that hold 8000 to 64,000 gates (ELECTRONIC DESIGN, *Dec. 1, 1997, p. 64)*.

The MX series is optimized for use in 5-V or mixed 5-V/3.3-V systems and delivers a clock-to-output time of just 5.6 ns. Targeted at systems that operate at 33 MHz or slower, the devices can tie right into PCI buses and operate at full PCI speed. Moreover, the multiplex I/O structure in the I/O cells allows users to select the drive level and provides selectable input switching for 3.3 V, optimizing I/O performance in 3.3-V systems. One unusual feature is a selectable low-power mode that can drop standby current to just 100 µA—a value that's 5 times less than any competing device.

The just-released SX family goes beyond the MX series and offers clock-to-output delays of just 4 ns—a 33% speed improvement over the MX family. That short delay also enables internal logic to be clocked at up to 320 MHz. Other performance-enhancing features include a 2-ns, 25-bit internal decode, and fast datapath ability that lets the family members tackle applications that require architectural features of both FPGAs and CPLDs.Fabricated on a 0.35-µm process, SX devices employ triple-level metal that helps ensure a small die size and plenty of routing resources.

Also banking on a nonvolatile antifuse technology, designers at QuickLogic developed a high-performance FPGA solution that delivers up to 100,000 usable PLD gates and up to 15,000 bits of embedded RAM—the pASIC 3 family. Based on 0.35-µm design rules, pASIC devices allow functions such as 16-bit counters to operate at clock speeds of 225 MHz and faster (ELECTRONIC DESIGN, *Nov. 3, 1997, p. 69)*.

Frequently, FPGAs chip sizes are pad limited—they can't be made any smaller than the size of the pad ring surrounding the logic core. To help shrink the packaging, designers at QuickLogic moved to a staggered bonding-pad arrangement. This shrunk the perimeter of the chip, and in turn reduced the chip area. Consequently, the devices have become more competitive with gate-array solutions, some of which also use the staggered bond-pad scheme. Therefore, a chip like the the QL3060, which packs the equivalent of about 60 kgates, can sell for just $84 apiece in 100-unit quantities.

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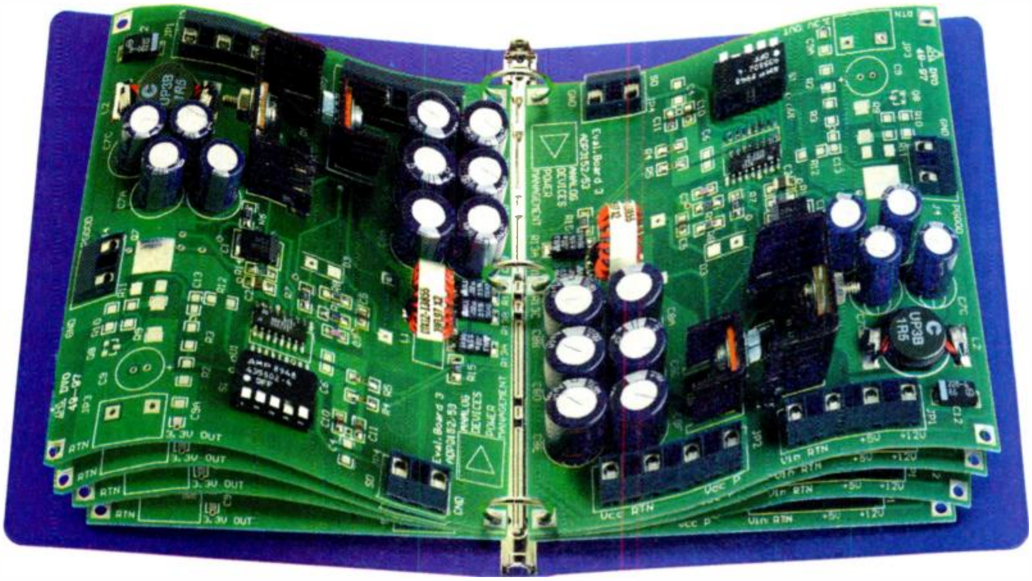

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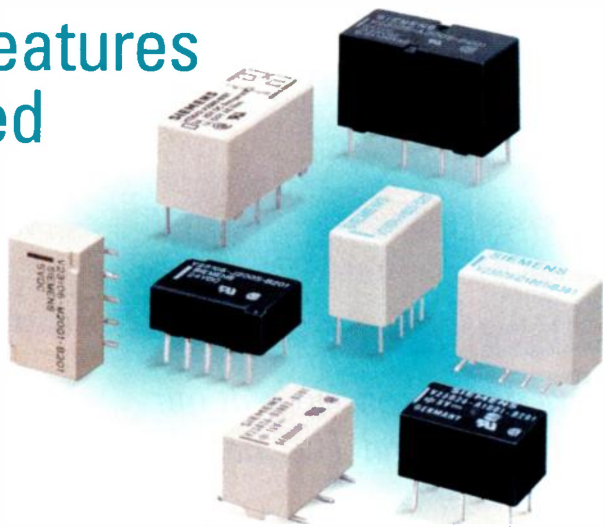

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READER SERVICE 173

PRODUCT FEATURE

Laser-Configured ASICs Lower Cost Yet Speed Up FLEX-Based Systems

The higher cost of FPGAs or CPLDs versus mask-programmed devices often is offset by the convenience of near-instant turnaround and the ability to change designs without concern about unused stock. Clear Logic has come up with a compromise to that situation by using its laser-configured ASIC technology. Armed with this, designers can use the Altera FLEX 8000 arrays to transfer their designs with no redesign or resynthesis, no nonrecurring engineering charges, no minimum orders, and no need to generate new test vectors.

Prototypes of the converted circuit are available within a week of receiving the bit stream, and volume production is available in three to four weeks. Clear Logic generates test vectors with 100% fault coverage at the factory and fully tests devices prior to shipment. The cost of the CL8000 equivalents can be as much as 50% less than the FLEX counterparts.

The lower cost is due partly to a single laser fuse which replaces the six-transistor memory cell used in the FLEX arrays for each configuration element. Thus, the CL8000 arrays are considerably smaller than the RAM-based FLEX devices. The lower number of transistors on the chip also helps reduce the power consumption of the CL8000 arrays compared to the RAM-based chips.

Although the CL8000 masterslices are based on a prefabricated array-like architecture, they're not general-purpose gate arrays and are optimized for direct conversion of the FLEX 8000 family. Consequently, no redesign or backstepping is required to convert FLEX configurations to the LASICs.

In contrast, if a generic gate array were used, the FLEX-based design would have to be reverted to its original HDL or schematic description. Then it would need to be resynthesized, resimulated, and go through all of the steps required for placement on a gate array. However, such a restructuring isn't always possible since some characteristics of a design (timing requirements, for example) aren't always extractable from a design. Therefore, designers may have to restart the conversion process from scratch.

By emulating the physical design of the FLEX structure, the CL8000 solves these problems and lets designers directly convert their logic . That's because the basic logic element of the CL8000 arrays consists of a four-input lookup table with a register.

To minimize the time required to convert the configuration file, Clear Logic developed a suite of EDA tools that perform the bit-stream extraction (ClearShot) and laser configuration (ClearFire) to achieve short turnaround times. ClearShot extracts the FLEX 8000 bit stream and converts it to laser-configuration instructions that result in functionality, internal timing, and electrical characteristics identical to those of the FLEX 8000 chips.

The company's NoFault embedded test capability allows Clear Logic to automatically generate all of the necessary test vectors based on the bit stream, and provide 100% fault coverage. Consequently, all CL8000 chips can be fully factory tested at the wafer level and after packaging.

The first replacement device to be sampled, the CL8452A, provides the equivalent to a 4000-gate FLEX device. The CL8452AQC160-4 comes in a 160-lead PQFP and sells for $14.50 each in lots of 100 units. A version housed in an 84-lead PLCC (the CL8452ALC84-4) sells for $10.40 each in similar quantities. Additional family members will include devices with gate counts of 6000, 8000, 12,000, and 16,000 gates, and direct replacements for the Altera EPF8636A, 8820A, 81188A, 8282A (and AV), and 81500A.

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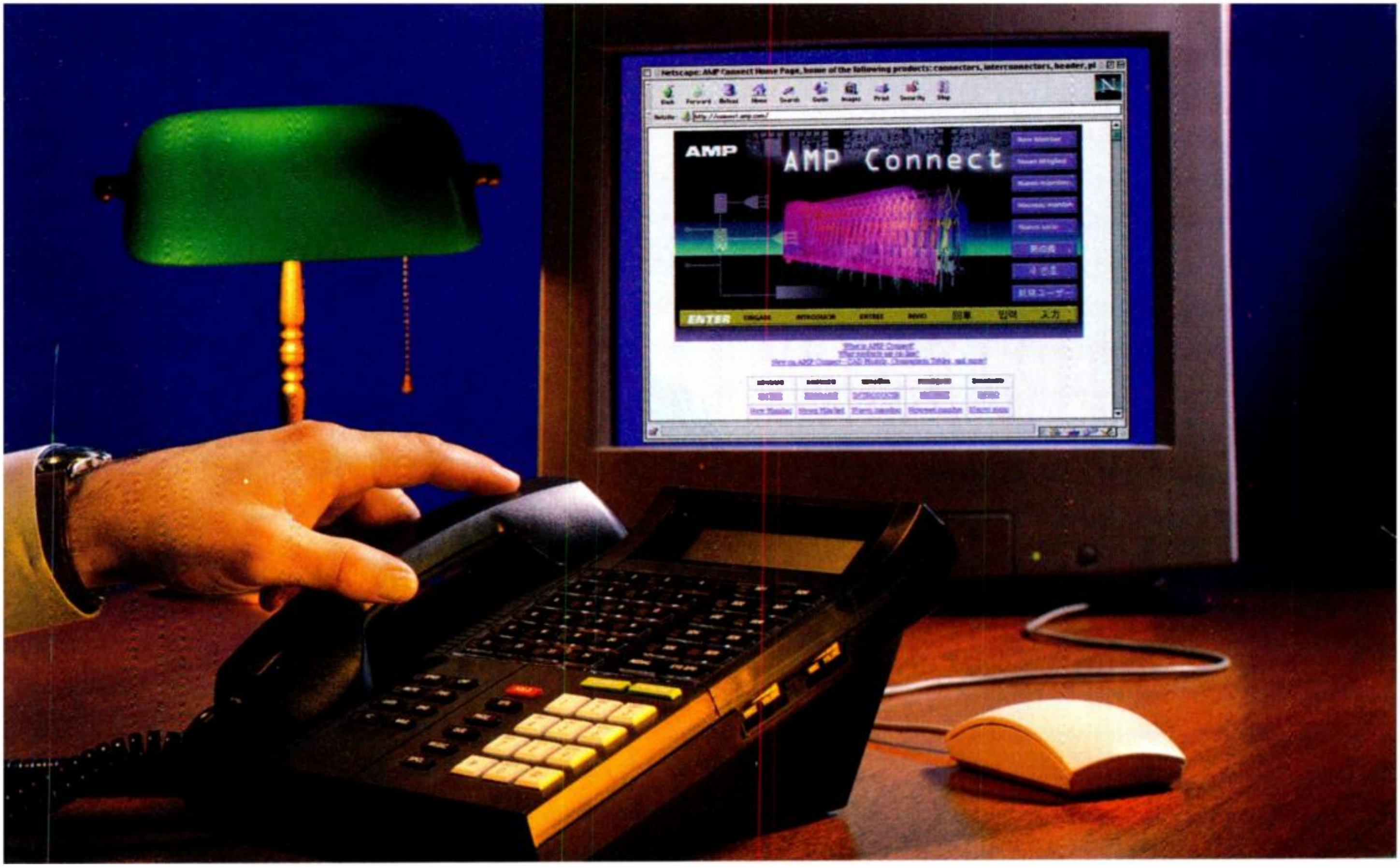
Lightweight MMX-Capable CPU Module Makes Pentium II Mobile

A new reduced-size module format and a move to a finer-line IC manufacturing process allowed Intel's designers to trim the power, size, and weight of its Pentium II processor module. As a result, portable computer systems won't have to pay any power or space penalty to use the Pentium II. Consuming just 7 to 8 W, the 35-gram, 57-by-60-by-6.5-mm minicartridge module contains the CPU with its on-chip L1 cache, a level-2 pipelined burst cache of 512 kbytes and associated tag RAM, and a thermal sensor.

Able to operate at clock rates of 233 or 266 MHz, the module's power consumption is less than one-third that of the original Pentium II edge-connector module, and is about the same power as the original 166-MHz Pentium processor. Also available is a slightly larger printed-circuit card module that also includes the 443BX "North-bridge" motherboard logic circuit and a voltage regulator.

The Pentium II MMX-capable CPU in the module employs 7.5 million transistors, and by itself consumes about 6.8 W thanks to the use of 0.25-µm design rules and a low, 1.75-V, internal operating-voltage level. To better suit mobile applications, the CPU includes two new low-power states—Quick Start and Deep Sleep—and a larger L1 cache (32 kbytes). The processor employs low-power GTL+ I/O levels for its 66-MHz bus interface, and a 2.5-V supply to power the I/O interface. The off-chip cache and tag RAMs operate from 3.3- and 1.8-V supplies.

The 6.5-mm thickness of the minicartridge allows the creation of very thin form-factor notebook systems. Furthermore, rather than pins on the bottom of the minicartridge, there's a 240-contact BGA area that helps keep the profile low when the module is *(continued on page 112)*



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(continued from page 110)
mounted on a motherboard. The larger mobile module format employs a 280-contact edge connector.

Supporting the mobile Pentium II products is the just-released 440BX chip set. The set includes the company's quad-port architecture, which

provides high-performance buffering to allow for maximum concurrency on all buses. Also part of the chip set are ACPI support and enhanced power-management features. The two chips in the set comprise the 82433BX, the North-bridge chip (which comes in a 492-contact ball-grid array package), and the 82371AB South-bridge chip, which comes in a 324-contact ball-grid array.

In 1000-unit lots, the 233- and 266-MHz minicartridge processors sell for $466 and $696 apiece, respectively, while the same-speed mobile pc-card modules with the North-bridge chip and regulator sell for $542 and $772, respectively. Samples are available from stock.

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DESIGN NOTES

LT1534 Ultralow Noise Switching Regulator Controls EMI

Design Note 178

Jeff Witt

Today's circuit designer is often challenged to assemble a high performance system by combining sensitive analog electronics with potentially noisy DC/DC converters. Requirements for a small, efficient, cost effective solution are in conflict with acceptable noise performance—noisy switching regulators call for filtering, shielding and layout revisions that add bulk and expense. Most electromagnetic interference (EMI) problems associated with DC/DC converters are due to high speed switching of large currents and voltages. To maintain high efficiency, these switch transitions are designed to occur as quickly as possible. The result is input and output ripple that contains very high harmonics of the switching frequency. These fast edges also couple through stray magnetic and electric fields to nearby signal lines, making efforts to filter the supply lines ineffective.

The LT®1534 ultralow noise switching regulator provides an effective and flexible solution to this problem. Using two external resistors, the user can program the slew rates of the current through the internal 2A power switch and the voltage on it. Noise performance can be evaluated and improved with the circuit operating in the final system. The system designer need sacrifice only as much efficiency as is necessary to meet the required noise performance. With the controlled slew rates, system performance is less sensitive to layout, and shielding requirements can be greatly reduced; expensive layout and mechanical revisions can be avoided.

The LT1534's internal oscillator can be programmed over a broad frequency range (20kHz to 250kHz) with good initial accuracy. It can also be synchronized to an external signal placing the switching frequency and its harmonics away from sensitive system frequencies.

Low Noise Boost Regulator

In Figure 1, the LT1534 boosts 3.3V to supply 650mA at 5V with its oscillator synchronized to an external 50kHz clock. The circuit relies on the low ESR of capacitor C2 to keep the output ripple low at the fundamental frequency; slew rate control reduces the high frequency ripple. Figure 2 shows waveforms of the circuit as it delivers 500mA. The top trace shows the voltage on the collector of the internal bipolar power switch (the COL pins), and the middle trace shows the switch current. The lowest trace is the output ripple. The slew rates are programmed to their fastest here, resulting in good efficiency (83%), but also generating excessive high frequency ripple. Figure 3 shows the same waveforms with the slew rates reduced. The large high frequency transients have been eliminated.

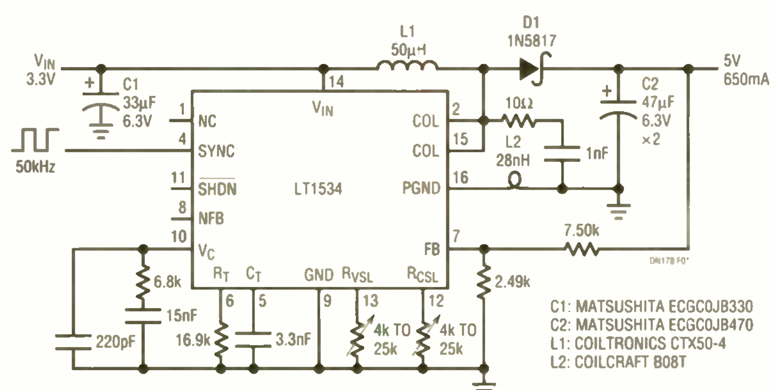

Figure 1. The LT1534 Boosts 3.3V to 5V. The Resistors on the R_{VSL} and R_{CSL} Pins Program the Slew Rates of the Voltage On the Power Switch (COL Pins) and the Current Through It

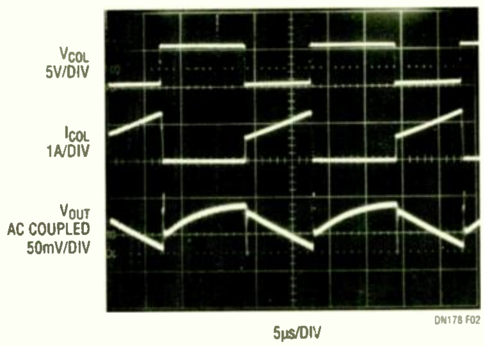

Figure 2. High Slew Rates (R_{CSL} = R_{VSL} = 4k) Result in Good Efficiency But Excess High Frequency Ripple

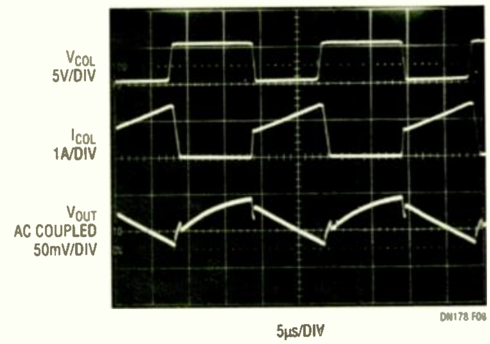

Figure 3. Low Slew Rates (R_{CSL} = R_{VSL} = 24k) Result in an Output Without Troublesome High Frequency Transients

Low Noise Bipolar Supply

Many high performance analog systems require quiet bipolar supplies. This circuit (Figure 4) will generate ±5V from a wide input range of 3V to 12V, with a total output power of 1.5W. By using a 1:1:1 transformer, the primary and secondary windings can be coupled using capacitors C2 and C3, allowing the LT1534 to control the switch transitions at the output rectifiers as well as at the switch collector. Secondary damping networks are not required.

Additional LT1534 Features

The LT1534 is a complete, low noise switching regulator with an internal 2A power switch, packaged in a 16-lead narrow plastic SO. The current mode architecture provides fast transient response and cycle-by-cycle current limit. Undervoltage lockout and thermal shutdown provide further protection. The large input range (2.7V to 23V) and high switch voltage (25V), combined with a 12µA shutdown mode, result in a very flexible part suitable for battery-powered operation. The LT1534 can directly regulate either positive or negative output voltages.

The LT1533, closely related to the LT1534, provides two slew rate-controlled 1A power switches. Optimized for push-pull topologies, the LT1533 provides even greater opportunity for reducing DC/DC converter noise. For further applications, consult the LT1533 and LT1534 data sheets and Linear Technology's Application Note 70.

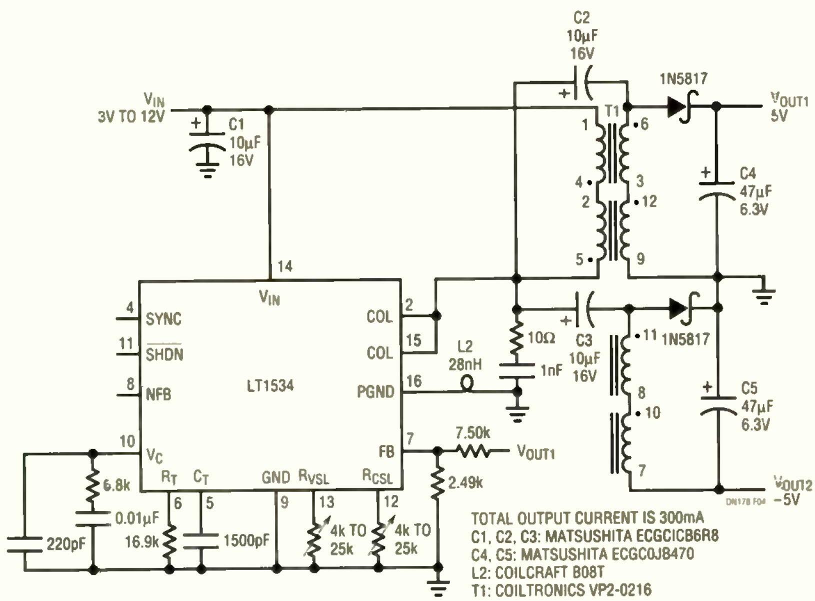

Figure 4. A Low Noise, Wide Input Range ±5V Supply

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PRODUCT FEATURE

8-Bit Microcontrollers Deliver Flash, SRAM, And Analog-To-Digital Converters

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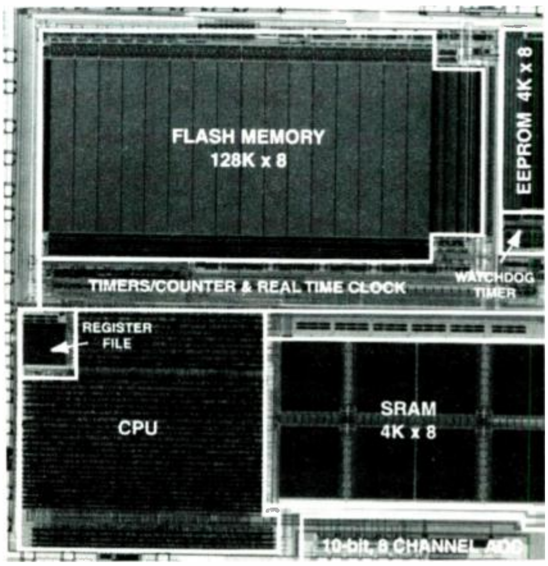

All of these features will be on one chip—the ATmega103. The ATmega603 packs half the flash and half the EEPROM, but otherwise has all the other resources of the ATmega103. Additional family members with less memory and other features are planned for release later this year and in 1999.

Claiming the highest throughput for feature-rich 8-bit microcontrollers, the AVR series employs a Harvard architecture with single-cycle instructions that allow the chips to deliver up to 8 MIPS when clocked at 8 MHz. The high throughput of the MCUs allows the circuits to replace 16-bit MCUs or multiple, slower 8-bit MCUs. The 4-kbyte block of SRAM and 32 general-purpose registers in the CPU provide programmers with a large stack space and a local variable storage area that supports C-code programming. Also, the EEPROM provides a secure storage area for sensitive data such as credit-card PIN codes.

The 128 kbytes (64 kbytes for the '603) of on-chip flash memory can be programmed in system, and programming voltages as low as 2.7 V can be used. The in-system programming feature allows code updates, bug fixes, and new features to easily be uploaded to the processor through the chip's serial port. The remaining features—48 programmable I/O lines, the real-time clock, 10-bit ADC, UART, and serial peripheral interface (SPI) port—provide all of the system resources required by most designers.

The MegaAVR MCUs include a set of 120 instructions that are optimized for very efficient assembly and C-language code density. To support the MCUs, the company has a comprehensive set of development tools; high-level language support is available from third-party vendors. The MegaICE tool, which sells for $4995, is a full-featured in-circuit emulator. It has a large trace buffer, support for unlimited breakpoints, external trigger capability, and built-in logic analyzer support.

Both the ATmega103 and 603 will operate from 2.7- to 5-V supplies and will come in 64-lead thin quad flat packages. In lots of 10,000 units, the '103 sells for $15 apiece, while the '603 goes for $11 each in similar quantities.

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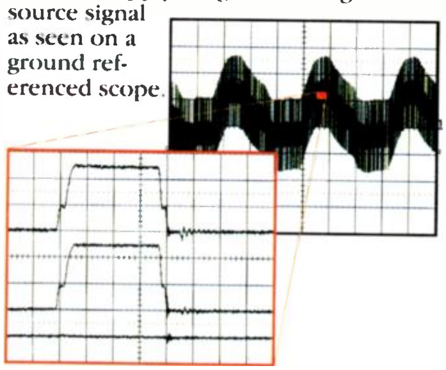

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The 1855 rejects the line voltage and high dv/dt signal, cleanly displaying the upper and lower gate drive signals.

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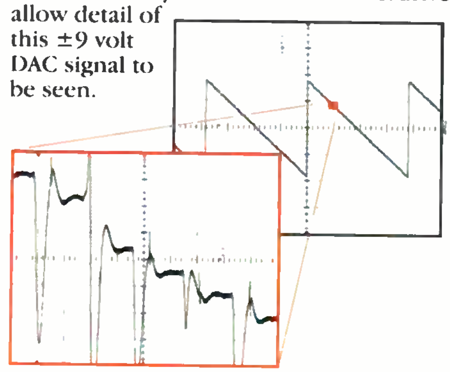
CONVENTIONAL
A scope lacks sufficient position range and lacks the ability to recover from overdrive to allow detail of this ±9 volt DAC signal to be seen.



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DVD Encoding Complexity Drives Embedded CPU Core Choice

Programmability And CPU Flexibility Are Key When Handling The Wide Array Of Algorithms Required In DVD.

REYNALDO ARCHIDE, ALAIN BISMUTH, and GREGG DIERKE, LSI Logic Corp., 1551 McCarthy Blvd., Milpitas, CA 95035, (408) 433-8000; fax: (408) 954-4855.

Requirements vary when choosing embedded CPU cores for system-on-a-chip designs. For DVD encoding, system engineers should emphasize an embedded CPU's level of flexibility and programmability. It's important to select an embedded CPU that gives engineers top-level control of the entire coding process in a high-level language (HLL) such as C or C++.

Being equipped with a basic understanding of how the encoding engines operate makes it relatively easy to modify an encoding algorithm through basic reprogramming. Programmers then can get immediate feedback on the video quality. This kind of CPU programmability via C/C++ is critical for supporting an assortment of different algorithms, including adaptive ones, to provide designers with an ample range of product differentiation.

A completely hardware-based architecture, on the other hand, locks systems designers into a single algorithm. Implementing a newer algorithm or performing alterations to an existing one requires a complete hardware change, thus incurring major design-engineering costs. Even architectures that are programmable may impose similar restraints if the microcoding isn't user-friendly.

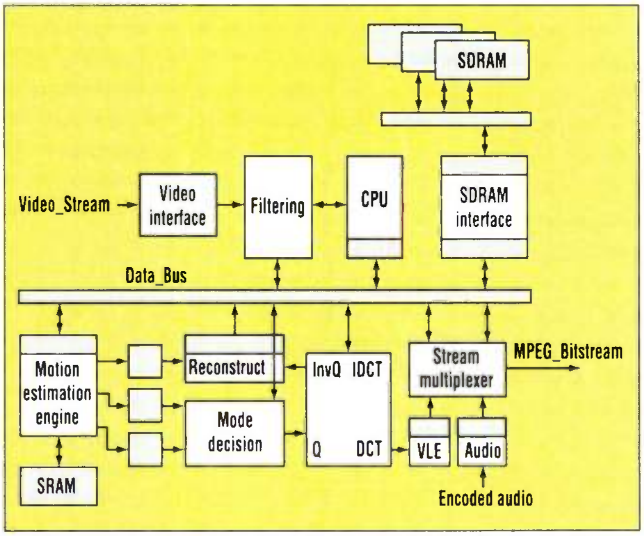
It also is best not to get bogged down by low-level, mundane, fixed tasks like discrete-cosine-transform (DCT) and variance calculations. Designers should choose an embedded CPU that lets them operate at a higher level, focusing on issues that affect video quality and/or bit rate, such as quantization selection or mode decision.

Quantization and Quality

Quantization (Quant) selection, in particular, plays a crucial role in DVD video quality. It's important to have the necessary CPU flexibility and programmability to target the proper levels of Quant selection, not only for video quality, but also for system differentiation. Today, there may be no single best viable algorithmic equation that can produce an "optimum" quantization value. But through the programmability features of an embedded CPU, system engineers have the ability to easily incorporate tomorrow's algorithms, allowing the product to improve as compression technology evolves.

To understand why Quant selection is so crucial to video quality, you must understand that real-world video compression is a lossy process. A certain amount of image detail must be sacrificed to achieve DVD bit rates. You simply can't have high compression without significant loss of data. But once this data is lost, it's gone forever. Ideally, this loss is introduced where it's least noticeable. That' what quantization is all about—it allows you to decide how much loss you can introduce into part of the image or picture.

In MPEG, quantization takes place in the frequency domain. An 8-by-8 block of pixels is first converted to an 8-by-8 block of frequency coefficients by the Discrete Cosine Transform (DCT). The DCT itself is a completely reversible process, meaning that the original coefficients can be converted back to the original



In the encoder circuitry shown, the embedded CPU controls the bit-stream generation and monitors the results of the encoder's various sub-engines. These include blocks such as motion estimation, mode decision calculations, quantization/inverse quantization, and the variable length encoder (VLE).

Two Paths For MPEG Syntax Generation

The MPEG syntax layers correspond to a hierarchical structure. A sequence constitutes the top layer of the video-coding hierarchy, consisting of a header and a number of group of pictures (GOPs). A GOP is a random-access point, meaning it's the smallest coding unit that can be independently encoded within a sequence. It contains a header and a number of pictures. The GOP header features time and editing information.

The TinyRISC embedded TR4101 embedded microprocessor core *(see the figure in "Embedded CPU Core Is Programmer-Friendly," p. 120)* supports syntax generation for all six MPEG layers, each of which supports either a signal-processing or a system function. The layers are: system, sequence, GOP, picture, slice, and macroblock *(see the figure.)*

The three types of pictures are intracoded (I), predictive-coded (P), and bidirectionally predictive-coded (B). "I" pictures are coded without reference to any other pictures; "P" pictures are coded using motion-compensated prediction from the previous I or P reference pictures; and "B" pictures are coded using motion compensation from a previous and a future I or P picture. Pictures consist of a header and one or more slices. The picture header includes time, picture type, and coding information.

A slice provides immunity to data errors. If the encoded bit stream is unreadable within a picture, the decoder can recover by waiting for the next slice, without having to drop an entire picture. Slices consist of a header and one or more macroblocks. The slice header contains position and quantizer scale information.

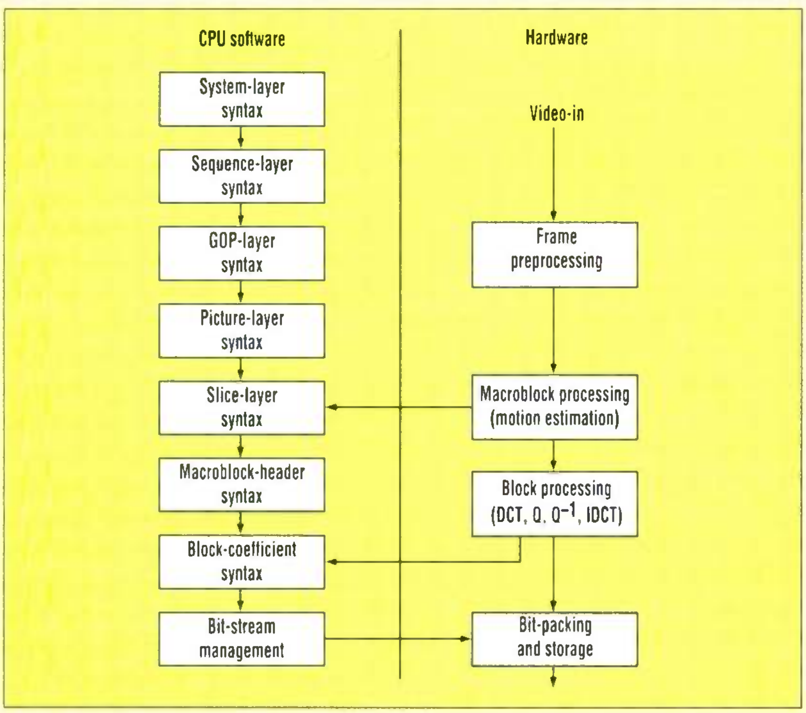
A macroblock is the basic unit for motion compensation and quantizer scale changes. In MPEG 2, the block can be either field or frame coded. Each macroblock consists of a header and six component 8-by-8 blocks; four blocks of luminance, one block of Cb chrominance, and one block of Cr chrominance. The macroblock header contains quantizer scale and motion compensation information. A macroblock has a 16-pixel by 16-line section of luminance component and the spatially corresponding 8-pixel by 8-line section of each chrominance component.

Blocks are the basic coding unit, and the DCT is applied at this block level. Each block contains 64 component pixels arranged in an 8-by-8 order. After the DCT, the resulting 8-by-8 block of coefficients are quantized, zig-zagged, grouped in run-level pairs (the number of zero coefficients preceding each non-zero coefficient is the "run"; the nonzero coefficient, itself, is the "level") and finally, Huffman encoded. Because these operations are very math intensive, only the Huffman coding is performed by the CPU.

The embedded microprocessor also handles the rate-control function of the encoder. Rate-control algorithms are feedback mechanisms that regulate the number of bits generated during the transform coding process over a given elapsed time. They're typically divided into two groups—fixed or variable.

For a fixed data rate, the output bit stream must be constant to ensure the encoder operates properly with a fixed-rate communications channel, such as satellite. Equally important, it must also ensure that decoder receiving the fixed-rate bit stream operates properly. Over a period of time determined by the size of the encoder's output or channel buffer, the average number of bits per macroblock must be held below a fixed threshold to prevent the decoder's video output from underflowing or overflowing. As a result, the quality of the video varies inversely with the image complexity.

When in a variable data-rate mode, the instantaneous bit rate is allowed to vary continuously in proportion to the level of complexity of the image. This is also known as "constant quality" bit-rate encoding. Variable rate control can be useful when there are multiple channels being multiplexed onto a single transport stream, or in a closed-loop system such as DVD. By knowing the type of the source material in advance (using so-called forward-analysis techniques), the encoder can optimize the image compression, based on statistics and image complexity, and set priorities.



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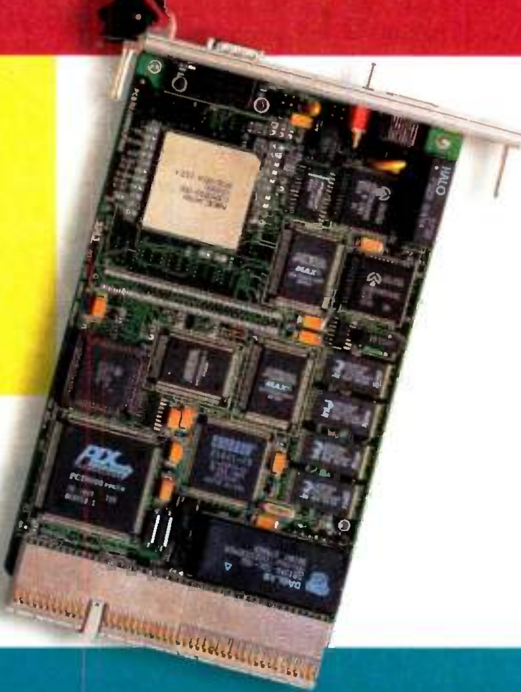

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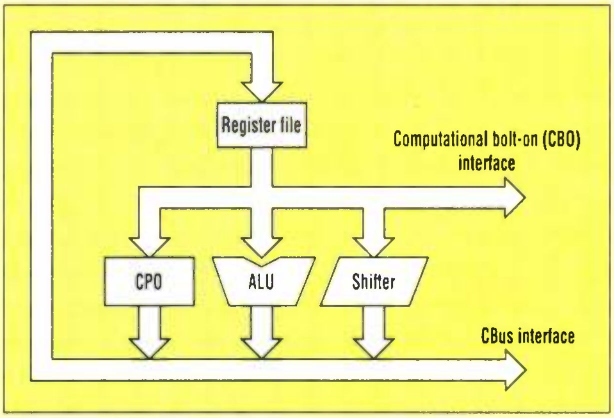
READER SERVICE 174

Embedded CPU Core Is Programmer-Friendly

The 81-MHz, 71-MIPS 16-/32-bit TinyRISC TR4101 embedded microprocessor core consists of a register file, system control coprocessor (CPO), arithmetic logical unit (ALU), shifter, CBus interface, and a computational bolt-on (CBO) interface *(see the figure)*. The register file contains general-purpose registers, supplies source operands to the execution units of the encoding function and handles the storage of results to the target registers.

The CPO processes exceptions, which includes interrupts; the ALU performs the necessary arithmetic and logical operations in support of the encoding functions and does address calculations; and the shifter performs shift operations. The CBO interface gives the systems engineer a way to insert specialized arithmetic instructions to the microprocessor. For example, an embedded CPU can attach a multiply-divide unit (MDU) via the CBO interface to perform such encoding-support functions as complex rate-control calculations.



The CBus interface passes data to and from the core. Thus, systems engineers can attach up to three tightly coupled special-purpose coprocessors that enhance the embedded microprocessor's general-purpose computational power. By taking this approach, high-performance, application-specific hardware is made directly accessible to a programmer at the instruction-set level.

The embedded CPU's code is written in C/C++, then compiled into instructions and stored in memory. Besides handling syntax generation for all MPEG layers, the code also handles frame control and type, rate control, audio and system-stream multiplexing, and parts of the mode decision process.

8-by-8 block of pixels using an Inverse DCT (or IDCT), without any loss.

The quantization process essentially involves dividing these coefficients by a Quant value during encoding, and then multiplying by the same Quant value during decoding. This does two things to the original frequency coefficients: First, it reduces the accuracy of the larger values. In general, this type of "loss" is very minor, and typically unnoticeable, after conversion back to the spatial domain. The second effect is the complete elimination of the smaller coefficients. This is much more serious, because it can introduce very noticeable losses in the spatial domain, especially if it involves a lower frequency.

Although the most noticeable distortion results from eliminating coefficients, this also contributes most to higher compression ratios. And there's the rub. To achieve high compression ratios, you have to start throwing away coefficients—a lot of them. At a bit rate of 4 Mbits/s, an average I-block uses only about six coefficients. Some blocks need more and some need fewer. But which ones? The trick to successful quantization is finding a way to eliminate all coefficients that are the least

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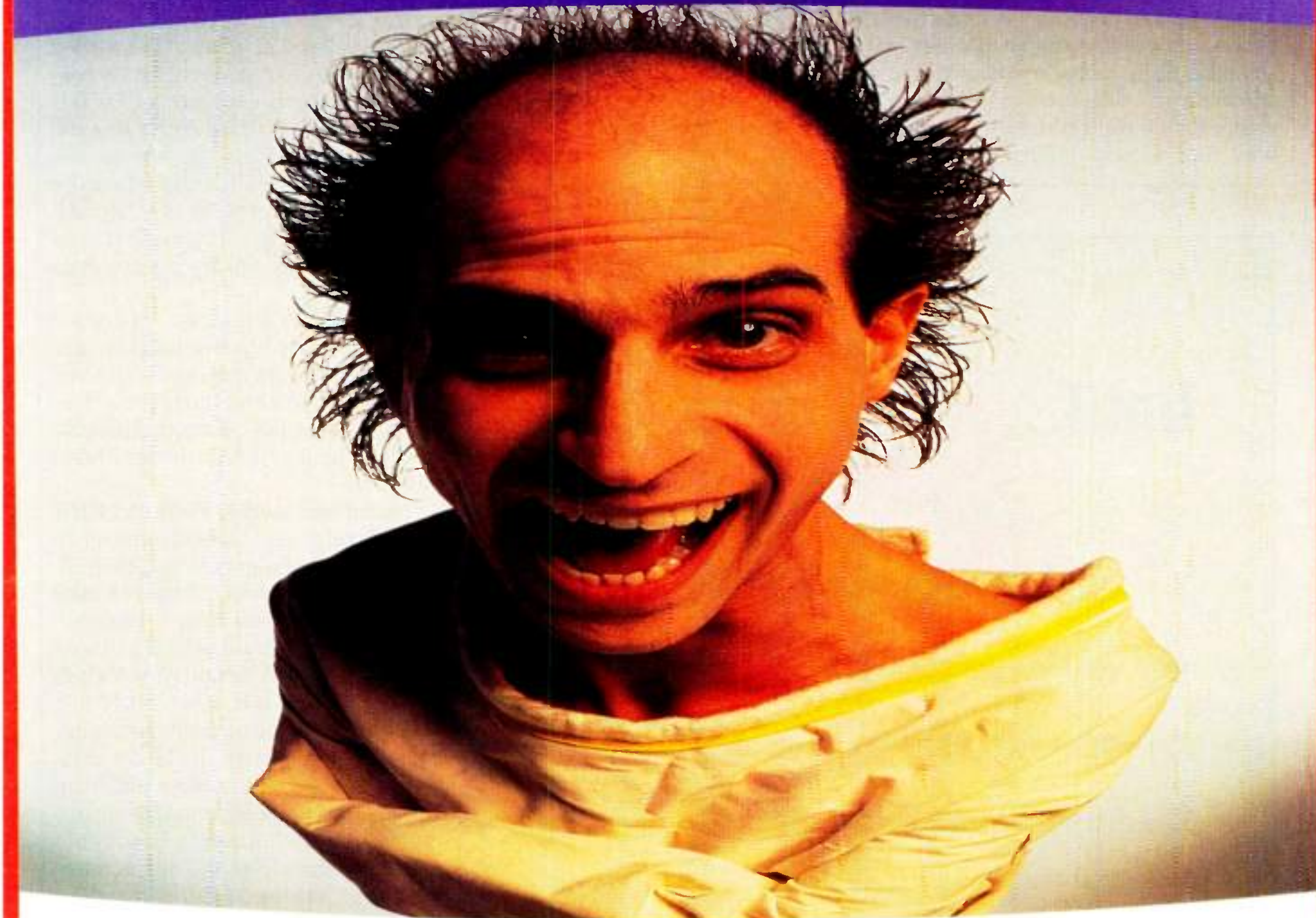

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noticeable to the human eye.

Ultimately, the entire quantization algorithm boils down to a sophisticated modeling of the human visual system. Some kinds of data loss are more tolerable than others. While this process may sound simple, it's highly complex. Still, the basic principle is to throw away enough data to meet the compression required, but do it in a way that's least noticeable. It's a tricky proposition; there are many different ways to perform Quant selection, and engineers are always finding better algorithms. That's the reason this particular encoding function should be performed in software and not in hardware.

Variable Bit Rate

Embedded CPU flexibility and programmability also play a part in attaining video quality goals in a DVD system design. Consider that most DVD systems are based on variable bit rate (VBR). The instantaneous bit rate of a DVD system varies continuously with the complexity of the image being created. This allows the encoded video quality to remain relatively constant. The average bit rate for DVD is 4.7 Mbits/s. But actual data rates can slip below 2 Mbits/s and accelerate to a maximum of over 10 Mbits/s. Because a DVD player/recorder is a "closed-loop" system, this is the method used to generate high-quality images from the DVD disk.

In contrast, a broadcast application is an open-loop system with severe constraints on channel bandwidth and buffers. In this case, the bit rate control of choice is Constant Bit Rate (CBR). Think of this as the antithesis of VBR.

In the real world, VBR and CBR actually represent the endpoints of an entire range of algorithmic possibilities. The specific algorithm selected depends on various system parameters, and, as in Quant selection, these algorithms are constantly evolving. With that in mind, it's simply not smart engineering to hardwire the encoding function with the latest algorithm. A single hardware platform that can easily accommodate future algorithmic refinements is not only more economical, but will also accelerate the evolution of video-encoding technology.

Each To Their Own Duties

In the encoder circuitry shown in Figure 1, the embedded CPU *(see "Embedded CPU Core Is Programmer Friendly," p. 120)* controls the bitstream generation and monitors the results of the encoder's various subengines. These include such blocks as motion estimation, mode decision calculations, quantization/inverse quantization, and the variable length encoder (VLE). The CPU tracks and reads the motion vectors in a register after motion estimation is performed. Likewise, the same is done with mode decision. This module makes the necessary calculations, and afterward, it stores the results in several registers. The CPU monitors the calculations, and then via software arrives at a mode decision and a quantization value.

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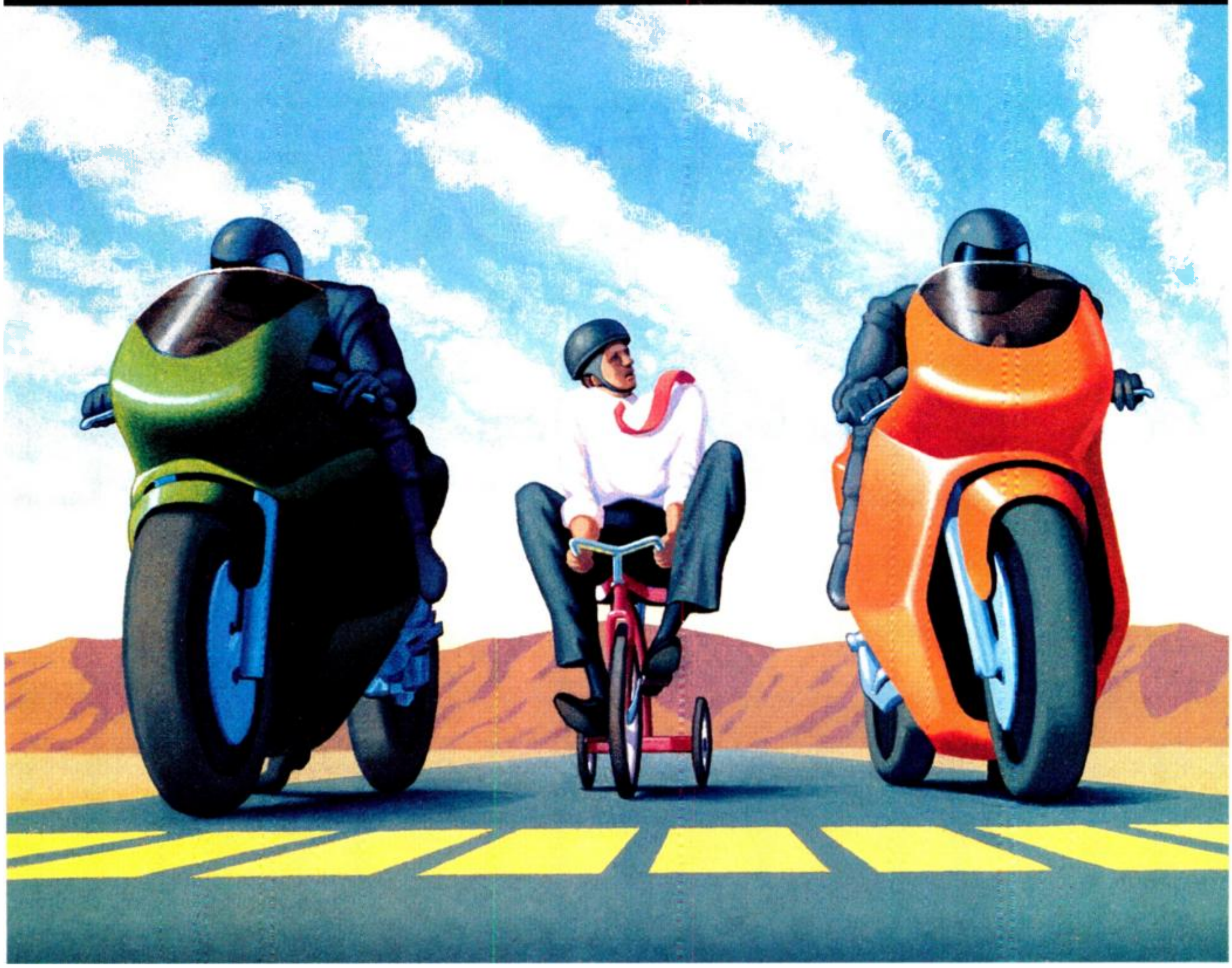

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READER SERVICE #18

In this encoding application, a custom coprocessor performs variable length encoding (VLE). This encoding operation is a reversible and lossless procedure for coding. It assigns shorter code words to frequent events and longer code words to less-frequent events, thereby achieving further compression. Huffman coding is the most often utilized form of VLE, due to its simplicity and efficiency in reducing the number of bits necessary to encode without losing information.

Several key attributes contributing to design flexibility differentiate one encoder from another. They include quantization value selection, rate control, how many frames are being stored, the number of bidirectional or interpolated pictures (B frames) between anchors, or whether or not original and/or reconstructed data is being used for encoding.

The embedded CPU in this encosing application also supports syntax generation for all six MPEG layers. Each layer supports either a signal-processing or a system function *(see "Two Paths For MPEG Syntax Generation," p. 118)*.

To sum things up, the ideal encoder combines programmable and hard-wired functions to achieve the best possible cost/performance trade-off. It performs math-intensive, well-defined functions in hardware using hard-wired "subengines," while it will make programmable those functions and decisions that allow engineers to differentiate the end product.

Reynaldo Archide is Microprocessor Core product manager at LSI Logic. He received his BSEE from the University of British Columbia and his MSEE from Santa Clara University, Santa Clara, Calif.

Alain Bismuth is director of Consumer DVD Marketing at LSI Logic. He holds an MSEE is from the Ecole Centrale in France.

Gregg Dierke is design manager for DVD Products, Consumer Products Division. Dierke is currently manager and technical lead for LSI Logic's consumer MPEG-2 Encoder project. He received his B.S. in Electrical Engineering from Stanford University, Stanford, Calif.

Java Software Co-Processor Will Serve Embedded Market

NSI Com has signed a license agreement with Sun Microsystems for providing a Java software co-processor to the embedded market. Under terms of the agreement, NSI Com will sell its family of binary products called JSCP to both Sun licensees and non-licensees. In addition, Sun and NSI Com will jointly market the product in certain areas

The JSCP products help users implement and port EmbeddedJavaOS to embedded devices. It uses the company's encapsulation technique to effectively isolate the Java and non-Java threads. This isolation is important for providing a high degree of robustness. JSCP provides most of the OS services for Java on the designated CPU rather than acting as an interface between the native OS and Java programs. It behaves as an additional operating system on the CPU of the embedded system. As a result, it appears as just one additional task to the native OS. In that single task, JSCP provides multithreading, program scheduling, and communications management. LM

NSI Com US, *1999 S. Bascom Ave., Suite 700, Campbell, CA 95008; (408) 879-6245; www.nsicom.com; e-mail: info@nsicom.com.* **CIRCLE 568**

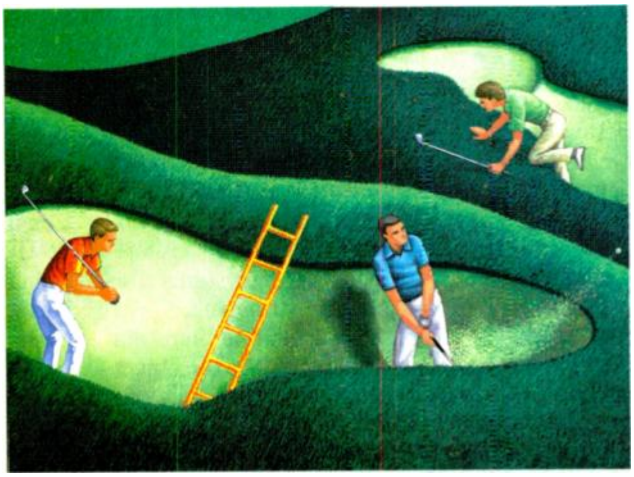
Hardware/Software Bundle Supports DSP Workshop

DSPEngine is a hardware and software bundle that's used with The MathWorks' DSP Workshop for system development. DSP Workshop is a block-diagram development environment. The DSPEngine provides a target platform for DSP Workshop, smoothing the development path from block diagram to a real-world system.

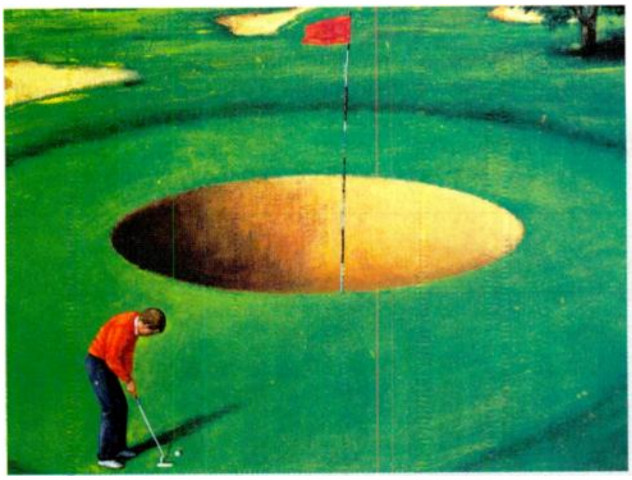
DSPEngine's hardware consists of a PC/C32 PC plug-in card that has a 60-MHz TMS320C32 floating-point DSP, 1 Mbyte of SRAM, and two daughter-module sites to add real-world I/O. The software portion of the product, Link-RT, establishes a real-time link between the DSP hardware and DSP Workshop. DSPEngine costs under $1000, and is sold with DSP Workshop. LM

Loughborough Sound Images Inc., *70 Westview St., Lexington, MA 02173; (781) 860-9020; www.lsi-dsp.com.* **CIRCLE 569**

Designing With Ordinary PCI Interface Chips.



Designing With The New S5920 PCI Interface Chip.



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The S5920 delivers increased reliability and performance for designers moving from ISA to the PCI interface, as well as superior economics to an off-the-shelf ASIC. It also features unique control port programmability through the system or add-on side, as well as support for synchronous and asynchronous local bus connections, advanced mailbox functionality, and integrated external devices. And it's compliant with both the existing 2.1 and proposed 2.2 PCI standards.

Because the S5920 is software compatible with our proven S5933, it eliminates debugging time and gives designers the flexibility to create smarter designs with reduced design-in costs and time to market.

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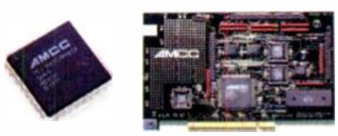

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Programming System Combines Top-Down, Bottom-Up Approaches

While most development tool systems use either a top-down or a bottom-up approach, Control Shell lets users combine both. With the software, users can start with a global unified concept, then decompose it into more specialized subsystems.

The Control Shell-Release 6.0 is a component-based real-time programming system that lets users create object oriented designs from existing software components. It combines event-driven logic and sampled data feedback control in an automated visual programming system.

EM system designs can be created from the "top down" by visually decomposing problems into interacting objects. Alternatively, it lets designers build systems from the "bottom up" by graphically combining components from a repository of reusable, tested and maintainable software.

ControlShell is supported on Sun, Silicon Graphics, and Windows NT hosts. Real-time target applications will run on Wind River Systems' VxWorks and SGI's React. Control Shell also is integrated with Wind River Systems' Tornado development environment.

Both behavioral and functional diagrams can be built thanks to an object-modeling feature. Objects can be connected through well-defined interfaces and organized through a hierarchical design configuration.

The software includes library of matrix and mathematical utilities that let you craft complex algorithms for real-time execution. Automatic code generation also is possible. Users can generate C++ code classes for all interfaces and primitive components. Changes can be merged to interface and component definitions with custom user code.

For team development, the software allows users to store all work in reusable repositories. Team members can browse and access internal, external, and RTI-supplied shared repositories during design and development.

Control Shell features live analysis, debugging, and monitoring. Users can watch state-machine diagrams transition as their application runs. RTI's Stethoscope tool monitors and debugs running applications. Users can analyze noise, tune performance, and measure responses on-the-fly.

With a run-time interpretive Shell, users are able to interact directly with the running application. It's possible to change parameters, monitor sta s, write test scripts, and change cor nents while the system is running.

Available now, licenses for Con Shell start at $13,250.

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CIRCLE 570

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April 1998

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RS232 (V.28)	V.35	V.36
EIA-530	RS449	X.21
EIA-530-A	RS423 (V.10)	RS422 (V.11)

Configurable transceivers simplify designs on both DTE and DCE sides of the interface. But depending on the modes that are implemented, the transceiver may need to provide different configurations.

Full-Featured, All Protocols – LTC1343

- Remote Loopback (RL)
- Local Loopback (LL)
- Test Mode (TM)
- Ring Indicator (RI)
- Internal Echo Clock Mode
- DTE/DCE Switching

Smallest Footprint, All Protocols – LTC1543/LTC1544

- Local Loopback (LL)
- DTE/DCE Switching

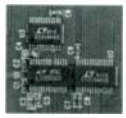
Protocol Selection

M0	M1	M2	Mode
0	0	0	V.10
0	0	1	EIA530-A
0	1	0	EIA530
0	1	1	X.21
1	0	0	V.35
1	0	1	449, 530, V.36
1	1	0	V.28, RS232
1	1	1	No Cable

The modes are completely software controlled – no DIP switches or relays! In fact, with clever use of connector pins, the modes can be enabled with pull-up resistors for a cable-selectable serial port.

Key Features

- Single 5V Supply Operation
- Uses 1.0µF Capacitors
- No Cable Mode uses just 3mW
- Flow-Through Architecture



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Meets NET1, NET2 and New TBR2 Requirements!

The LTC1343 is packaged in the 44-lead SSOP while the LTC1543 and LTC1544 are available in the 28-lead SSOP package. Combined with the LTC1344 in the 24-lead SSOP, the chipset can be implemented in less board space than a single chip.

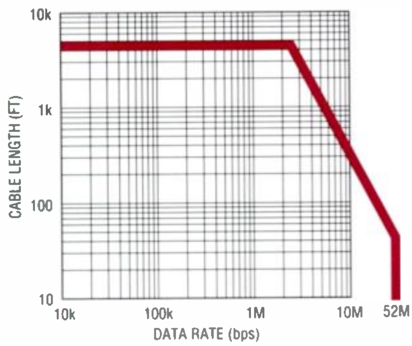
Choose the right combination for your application:

CLK/Data	Control	Term.	Protocols	Features	Benefits
LTC1343	LTC1343	LTC1344	• V.35 • V.36 • V.28 (RS232) • V.10 (RS423)	Supports optional control signals such as remote loopback, local loopback, test moce, ring indicator and internal echo clock mode. DTE/DCE switchable. Transparent LATCH allows control signals to be shared.	Full functionality
LTC1343	LTC1544	LTC1344	• EIA-530 • EIA-530-A	Supports optional control signals such as remote loopback, local loopback, test mode and internal echo clock mode. DTE/DCE switchable.	Best trade-off between size and functionality
LTC1543	LTC1544	LTC1344A	• RS449 • X.21	Supports most common control signals including local loopback. DTE/DCE switchable.	Smallest Implementation
LTC1543	LT1134A	LTC1344A	V.35 and V.28 (RS232)	Supports optional control signals such as remote locpback, local loopback, test mode, ring indicator. DTE/DCE switchable.	Lowest Cost

In This Issue...

Break the Rules in High Speed RS485 – 52Mbps!

Playing by the "rules" in RS485 limits your network to 10Mbps and a distance of 100 feet. Innovations from Linear Technology break through



the barriers and give you transceivers capable of 52Mbps! This opens up the possibilities while still providing the ruggedness of traditional RS485 networks.

The new transceivers have precision propagation delay providing a ±3.5ns window that is guaranteed over temperature. The chip-to-chip skew is typically only 500ps – that's half a nanosecond! This makes the timing easy for parallel applications.

What can you do with 52Mbps?

- Drive OC-1/STS-1 line rates of 51.84Mbps
- Push LVDS speeds with V_{CM} of -7V to 12V
- Amazing 104Mbps full-duplex bandwidth!
- Upgrade RS485 bus speeds FIVE times!
- Drive differential Fast SCSI

RS485 Ruggedness

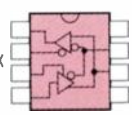
Linear Technology and RS485 have been synonymous with high performance, ruggedness and low power. These transceivers are capable of unprecedented speed as well as the wide common mode range and high three-state impedance required for industrial networks.

- Wide Common Mode:-7V to 12V
- Guaranteed Fail-Safe
- Short-Circuit Protected
- Thermal Shutdown
- High Impedance in Three-State or Power Off (Won't load down the bus)

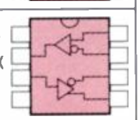
Guaranteed Fail-Safe Protection

Most RS485 "fail-safe" transceivers only detect an open condition on the bus. Linear Technology's new receiver inputs include special circuitry to detect the difference between a dead short and an idle, terminated bus. Before, the termination required a bias to pull the bus high during idle conditions, wasting power and space. With Fail-Safe, the transceiver detects the idle state and provides a high output.

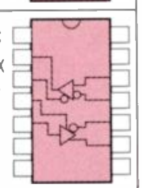
LTC1685 52Mbit/sec Half-Duplex Transceiver



LTC1686 52Mbit/sec Full-Duplex Transceiver



LTC1687 52Mbit/sec Full-Duplex Transceiver



These high speed transceivers come in full- and half-duplex in the most popular industry standard RS485 pin configurations.

Low Power Short-Circuit Protection

The RS485 "rules" allow the short-circuit current limit to be up to 250mA. That'll burn your finger! RS485 loads can draw over 50mA in normal operation, but these new high speed transceivers detect shorts and limit them to a cool 10mA.

Breaking the rules by sensing the output level and throttling back the current saves power and protects your fingers! It also protects the bus from ringing or oscillating that may occur when the bus is shorted and it no longer acts like a transmission line.

RS485 just got a new set of rules. Break through the barriers with Linear Technology.

Configurable Transceivers for RS232/RS485

Connect your portable instrument or Point-of-Sale terminal to either an RS232 port or an RS485 port using the same connector - without throwing switches, swapping chips or unplugging modules! The LTC1387 can be switched between RS232 and RS485 on the same I/O port.

Benefits

- Replace RS232 and RS485 transceivers
- One Layout, One Chip – Two Protocols
- Software Switching between Modes
- No DIP Switches, No Sockets, No Relays
- Single 5V Supply
- ±10kV ESD Protection

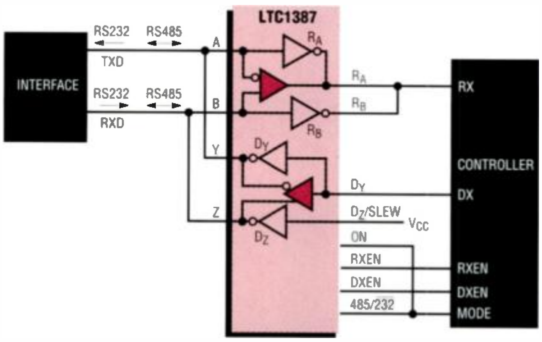
Several enabling options are possible with this flexible transceiver for full- and half-duplex operation. The RS485 driver also has a low slew rate mode for minimum EMI. Loopback mode allows the port to test itself for diagnostics.

LTC1387 is available in 20-lead wide surface mount and shrink small outline packages (SSOP). Commercial and Industrial temperature grades are available.

Circle No. 220

Single RS232/RS485 Serial Port

No DIP Switches! No Sockets! No Relays!



Enabled as Full-Duplex RS232 and Half-Duplex RS485

LTC1387: $4.50 ea. for 1K-piece Qty.

Dual Transceiver As RS232/RS485 Translator

The LTC1334 is a dual port, configurable RS232/RS485 transceiver. Each port can be configured as two RS232 drivers and receivers or one RS485 transceiver. The entire device operates on a single 5V supply with only four 0.1µF capacitors. And true to Linear Technology tradition, the I/O pins are protected against ±10kV ESD as well as high DC voltage levels.

Benefits

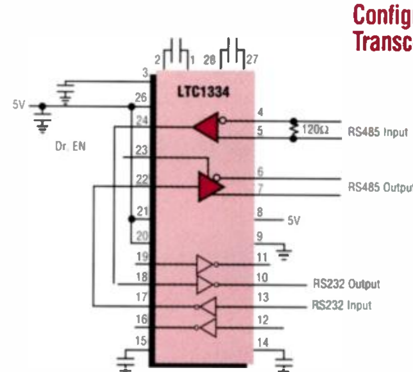
- Replace TWO RS232 and RS485 transceivers
- One Layout, One Chip, One 5V Supply
- Two Full Ports, Two Configurable Protocols
- Software Switching between Modes
- No DIP Switches, No Sockets, No Relays
- ±10kV ESD Protection

Each port has separate enable control for the most flexibility. Loopback mode allows the port to test itself for diagnostics. And in shutdown, the device consumes only 10µA!

LTC1334 is available in 28-lead wide surface mount and plastic dual-inline packages (PDIP). Commercial and Industrial temperature grades are available.

Circle No. 222

Single Supply Dual RS232/RS485 Configurable Transceiver



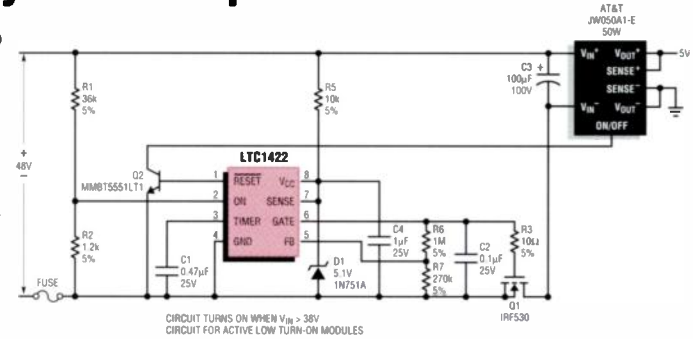
LTC1334 Configured as an RS232 to RS485 Translator

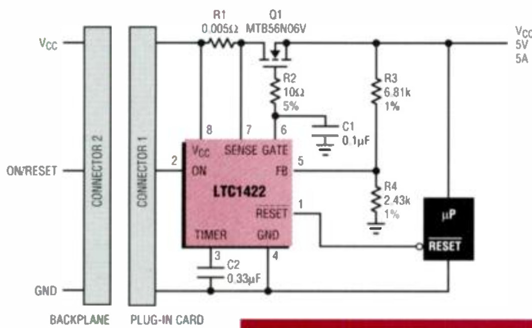
LTC1334: $6.50 ea. for 1K-piece Qty.

Single Supply Hot Swap: Small & Flexible

SO-8 Package

The LTC1422 is designed to turn a single supply board's supply voltage on and off in a controlled manner, allowing the board to be safely inserted or removed from a live backplane. Also provided is a system reset signal to indicate when board supply voltage drops below a programmable voltage.





With a few external circuits you can hot swap -48V.

The LTC1422 is available in an SO-8 package which makes a very small and efficient hot swap control circuit. Commercial and Industrial temperature grades are available.

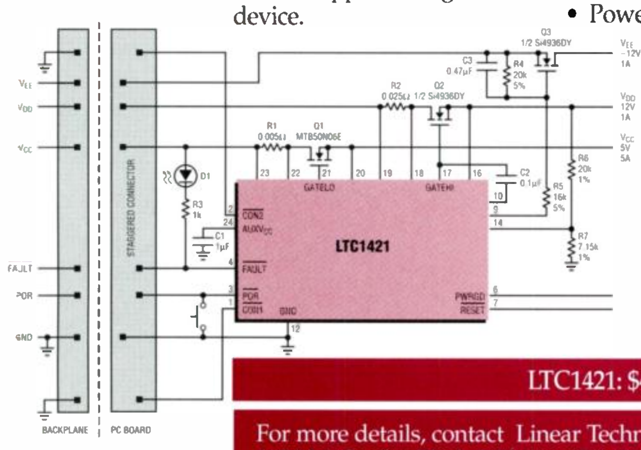
LTC1422 Programmable Features:
- Reset threshold
- Circuit breaker current limit
- FET turn-on rate and delay

Circle No. 224

LTC1422: $2.75 ea. for 1K-piece Qty.

Hot Swap Four Supplies with Full Reset Control

With the LTC1421 Hot Swap Controller two supplies can be sensed directly but you can hot swap up to four supplies using this device.



Power Management Features:
- Connection Sense Inputs Indicate Board is Completely Connected to the Backplane
- Power-On-Reset
  - FAULT Output when Over-Current Fault is Detected
  - RESET Output when Power Failure Occurs
  - PWRGD Output once Voltages reach a Preset Threshold
- DISABLE Output can be used to disable the Data Bus

The LTC1421 is available in the 24-pin SSOP and wide SO packages.

Circle No. 226

LTC1421: $4.90 ea. for 1K-piece Qty.

For more details, contact Linear Technology Corporation, 1630 McCarthy Blvd., Milpitas, CA 95035-7417, Web Site: www.linear-tech.com. (408) 432-1900. Fax: (408) 434-0507. For literature only: 1-800-4-LINEAR.

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(continued from page 65)
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Seventh IEEE International Conference on Universal Personal Communications, Oct. 5-9. Palazzo Congressi & Centro Affari, Florence, Italy. Contact Federico Tosco, CSELT, Via Reiss Romoli 274, 10148 Torrino, Italy; +39 11-228-5321; fax +39 11 228-5295; e-mail: Federico.Tosco@CSELT.STET.IT.

IEEE/LEOS Semiconductor Laser Conference, Oct. 5-10. Nara Public Hall, Nara, Japan. Contact Elsie L. Vega, IEEE/LEOS, 445 Hoes Ln., P.O. Box 1331, Piscataway, NJ 08855-1331; (732) 562-3897; fax (732) 562-8434; e-mail: e.vega@ieee.org.

The Vision Show, Oct. 6-8. San Jose Convention Center, San Jose, CA. Contact Automated Imaging Association (AIA), 900 Victors Way, P.O. Box 3724, Ann Arbor, MI 48106; (313) 994-6088; fax (313) 994-3338; e-mail: kerickson@automated-imaging.org; www.automated-imaging.org.

IEEE Ultrasonics Symposium, Oct. 6-9. Hotel Metropolitan Sendai, Sendai, Japan. Contact Noriyoshi Chubachi, Tohoku Gakain University, Faculty of Engineering, Tagaio, Miyagi 985, Japan; +81 22-217-7077; fax +81 22-263-9230; e-mail: chubachi@chubachi.ecie.tohoku.ac.jp.

IEEE-SP International Symposium on Time-Frequency and Time-Scale Analysis, Oct. 7-9. Pittsburgh Sheraton, Pittsburgh, PA. Contact Patrick J. Loughlin, 348 Benedum Hall, Department of Electrical Engineering, University of Pittsburgh, Pittsburgh, PA 15261; (412) 624-9685; fax (412) 624-8003; e-mail: pat@ee.pitt.edu.

IEEE International Conference on Systems, Man, & Cybernetics, Oct. 12-14. Hyatt Regency La Jolla, La Jolla, CA. Contact M.A. Jafari, Dept. of Industrial Engineering, Rutgers University, P.O. Box 909, Piscataway, NJ 08855; (908) 445-3627; fax (908) 445-5467; e-mail: jafari@gandalf.rutgers.edu.

International Test Conference (ITC), Oct. 20-22. Sheraton Washington Hotel, Washington, D.C. Contact ITC, 2000 L St. N.W., Washington, D.C. 20036; (202) 973-8665; fax (202) 331-0111; e-mail: itc@courtesyassoc.com.

NOVEMBER

Embedded Systems Conference, Nov. 1-5. San Jose Convention Center, San Jose, CA. Contact Liz Austin, Miller Freeman Inc.; (888) 239-5563; (415) 538-3848; e-mail: esc@mfi.com; www.embedded.com.

Photonics East & Electronic Imaging International Exhibition, November 1-6. Boston, Massachusetts. Contact SPIE Exhibits Dept., P.O. Box 10, Bellingham, Washington 98227-0010; (360) 676-3290; fax (360) 647-1445; e-mail: exhibits@spie.org.

Voice, Video & Data Communications Conference & Exhibition, Nov. 1-6. Boston, MA. Contact SPIE Exhibits Dept., P.O. Box 10, Bellingham, WA 98227-0010; (360) 676-3290; fax (360) 647-1445; e-mail: exhibits@spie.org.

Technology 2008, November 3-5. Hynes Convention Center, Boston, Massachusetts. Contact Melissa Hinnen, Show Coordinator; (212) 490-3999; fax (212) 986-7864.

IEEE Global Telecommunications Conference (Globecom '98), Nov. 9-13. Sydney, Australia. Contact Sam Reisenfeld, School of Electrical Engineering, University of Technology, Sydney, Post Office Box 123; Broadway, NSW 2007, Australia; +61 2-330-2435; e-mail: samr@transmit.ee.uts.edu.au.

Third Broadband/The Last 100 Meters Conference and Exhibition, Nov. 12-14. Hynes Convention Center, Boston, MA. Contact Information Gatekeepers Inc., 214 Harvard Ave., Boston, MA 02134; (800) 323-1088; (617) 232-3111; fax (617) 734-8562; e-mail: igiboston@aol.com; www.igigroup.com.

DECEMBER

IEEE International Electron Devices Meeting (IEDM), Dec. 6-9. San Francisco, CA. Contact Phyllis Mahoney, Widerkehr & Associates, 101 Lakeforest Blvd., Suite 270, Gaithersburg, MD 20877; (301) 527-0900; fax (301) 527-0994; e-mail: pwmahoney@aol.com.

12th Systems Administration Conference (LISA '98), Dec. 6-11. Marriott Hotel, Boston, MA. Contact USENIX Conference Office, 22672 Lambert St., Suite 613, Lake Forest, CA 92630; (714) 588-8649; (714) 588-9706; e-mail: conference@usenix.org; www.usenix.org.

37th IEEE Conference on Decision and Control, Dec. 16-18. Hyatt Regency Westshore, Tampa, FL. Contact John D. Birdwell, Department of Electrical Engineering, University of Tennessee, Knoxville, TN 37996-2100; (423) 974-9187; fax (423) 974-9257; e-mail: birdwell@hickory_engr.utk.edu.

IEEE Region 10 Conference on Energy, Communication, Computers, and Controls (TENCON '98), Dec. 17-19. Asmoka Hotel, New Delhi, India. Contact Tripta Narang, A-10, Lajpat Nagar-III, New Delhi, 110024, India; +91 11-643-5441; fax +91 11-646-5645; e-mail: purkay.sagrik@axcess.net.in.

JANUARY 1999

Annual Reliability & Maintainability Symposium (RAMS), Jan. 19-21. Washington Hilton, Washington, DC. Contact V.R. Monshaw, Consulting Services, 1768 Lark Lane, Cherry Hill, NJ 08003; (609) 428-2342.

IEEE Power Engineering Society Winter Meeting, Jan. 31-Feb. 4. New York, NY. Contact Frank Schink, 14 Middlebury Lane, Cranford, NJ 07016; (908) 276-8847; fax (908) 276-8847.

FEBRUARY

Photonics West, February 6-12. San Jose, CA. Contact SPIE Exhibits Dept., P.O. Box 10, Bellingham, Washington 98227-0010; (360) 676-3290; fax (360) 647-1445; e-mail: exhibits@spie.org.

IEEE International Solid-State Circuits Conference (ISSCC '99), February 15-17. San Francisco Marriott, San Francisco, California. Contact Diane Suiters, Courtesy Associates, 655 15th St., N.W., Washington, DC 20005; (202) 639-4522; fax (202) 347-6109; e-mail: isscc@coutesyassoc.com.

Portable by Design, February 21-25. Santa Clara Convention Center, Santa Clara, California. Contact Rich Nass, Electronic Design, 611 Rte. 46 West,
(continued on page 140)

Circle 520

Optically Isolated Precision Bipolar Current Source

W. STEPHEN WOODWARD
Venable Hall, CB3290, University of North Carolina,
Chapel Hill, NC 27599-3290; e-mail: woodward@net.chem.unc.edu.

One of the most frequently requested instruments in the field of in-vivo and in-vitro neurophysiology research is the galvanically isolated neural stimulator. Applications in this field require an accurate, voltage-programmable, bipolar current source capable of driving microamp to milliamp currents into isolated electrodes with a voltage compliance in the range of volts to tens of volts. Commercial products of this type exist, but none of them are precise enough for quantitative studies without resorting to time-consuming unit-specific calibration.

This stimulator described here combines a dual op amp with two multichannel optoisolators (one dual and one quad) to control a floating, battery-powered H-bridge output stage *(see the figure)*. The bridge topology has the advantages of generating both output current polarities from a single battery (B1), and using a single output-current-monitoring optoisolator (E1/Q1) for both output polarities with an associated improvement in output symmetry.

To understand circuit operation, consider first a positive-polarity input: $V_{IN} > 0$. To sink the resulting input current and thus maintain input balance, A1-pin1 will slew negative until $I_{E2} = V_{IN}/R1$. The E2/Q2 coupled gain will drive $I_{Q2} > 0$ and a consequent negative excursion appears at A2-pin6. A2-pin7 will therefore slew positive, taking the common node of LEDs E3 and E5 with it.

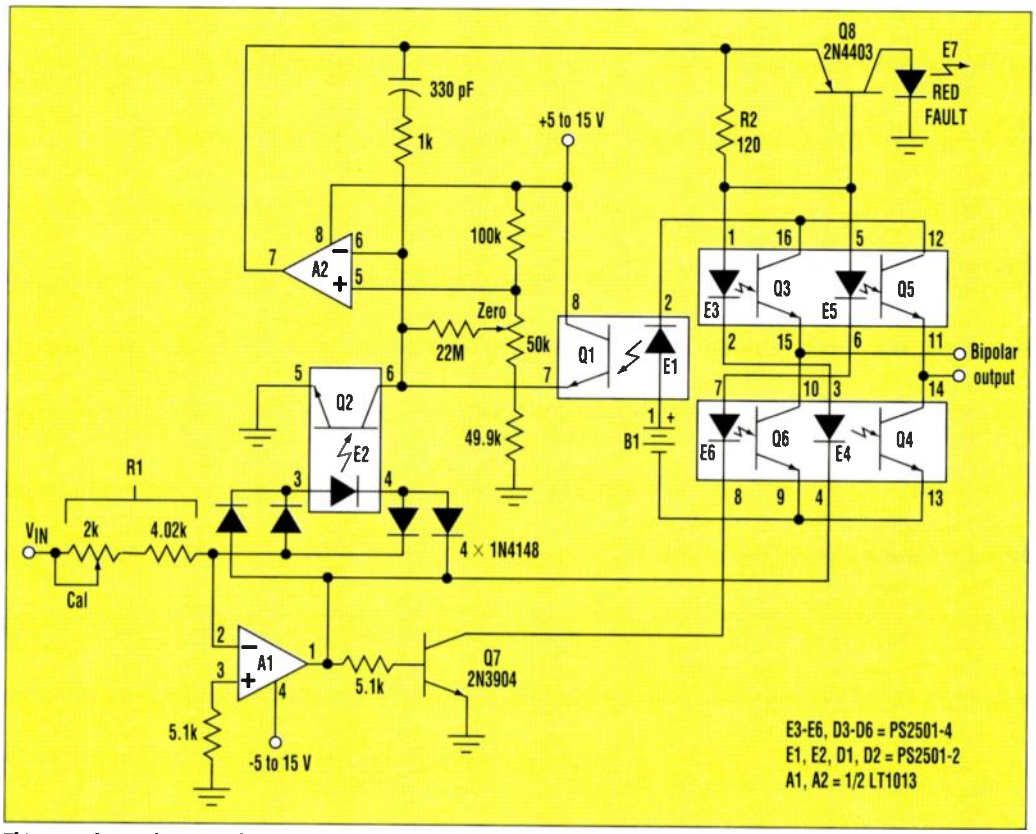
The negative voltage present at A1-pin1 will force Q7 off and thus steer current into E3 and E4, turning on H-bridge phototransistors Q3 and Q4. The resulting electrode current is sourced from B1 and must therefore pass through E1, closing a current-regulating feedback loop around A2 via the E1/Q1 coupled gain. A2 will then adjust the E3-E4 drive current until $I_{Q1} = I_{Q2}$. In doing so, because of the good tracking that exists over wide ranges of photocurrent between channels in a multichannel optoisolator like the PS2501 series, A2 accurately forces $I_{E1} = I_{E2}$ (the adjustment of R1 taking care of any a-priori mismatch between the coupled gains of the two channels) and thus:

$$I_{E1} = V_{IN}/5000$$

Operation for negative ($V_{IN} < 0$) control inputs is similar, except A1-pin1 will, of course, slew positive until $I_{E2} = -V_{IN}/R1$. This will turn Q7 on and steer the A2 output current to E5-E6 instead of E3-E4. Consequently, bridge output polarity will reverse. However, the output current magnitude is still sensed by E1/Q1, and thus the same R1 adjustment will serve to establish:

$$I_{E1} = -V_{IN}/5000$$

What results is precise correspondence between V_{IN} and output current over several orders of magnitude. To improve the reliability of the overall operation, Q8 and visible LED E7 watch for excess current drive from A2 to the H-bridge. E7 will thus give a warning when the voltage compliance of the H-bridge is exceeded. This will occur when the electrodes develop excessive impedance or when B1 needs to be replaced. When the drop across



This neural stimulator employs an optoisolated H-bridge output stage to generate both output-current polarities from a single battery (B1). Sensing the bridge current also allows improvements in output symmetry.

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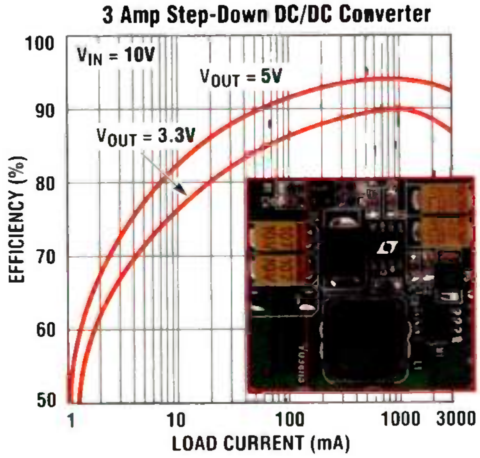

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R2 is > 0.7 V, indicating that the bridge is nearing or in output saturation, Q8 will turn on and light E7.

Defective electrodes are a more common cause of voltage compliance faults than battery failure due to the fact that B1's service life will typically approximate the shelf life of a 9-V, 500-mAhr battery. For applications requiring more output-voltage compliance than a single 9-V battery can provide, advantage can be taken of the 80-V_{CEO} rating of the PS2501 phototransistors by simply adding additional batteries in series with B1.

Circle 521

Current-Sensing LDO Voltage Regulator

JOHN STOUGHTON
UMM Electronics, 6911 Hillsdale Ct., Indianapolis, IN 46250-2062.

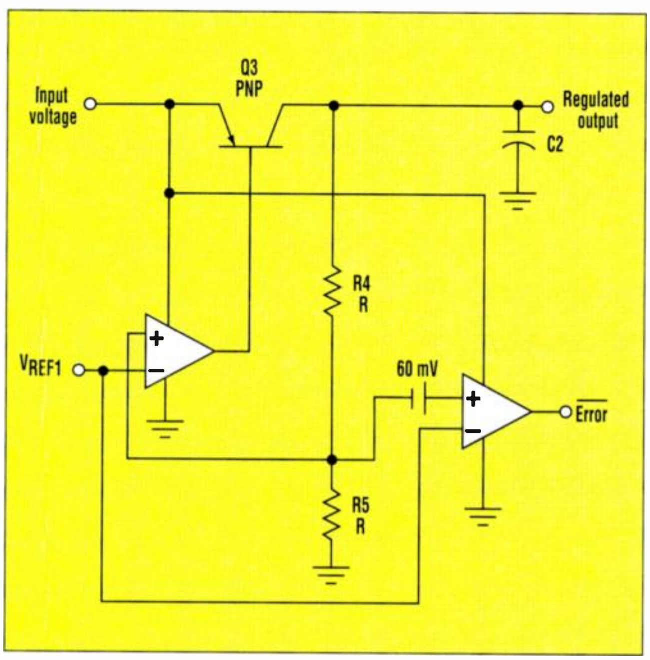
When designing battery-operated devices, battery contact chatter can be prove to be a difficult problem to overcome. When the chatter occurs at a critical time, the results can often be devastating. For instance, if a memory write takes place during a power interruption, memory corruption can occur, and checksums may be incorrectly computed or not be written at all.

A great tool in the arsenal of battery-powered device designers has been the low-dropout (LDO) regulator. These regulators use PNP devices for their output devices. As a result, they have dropout voltages that equal the V_{CESAT} of the PNP rather than a couple of V_{BE} drops. For example, the LP2951 has a dropout voltage (at I_{OUT} = 100 mA) of 600 mV while the dropout voltage of the LM317L is almost 2 V under the same conditions. This feature of LDO regulators allows designers to gain an additional volt or more of precious end-of-life battery potential.

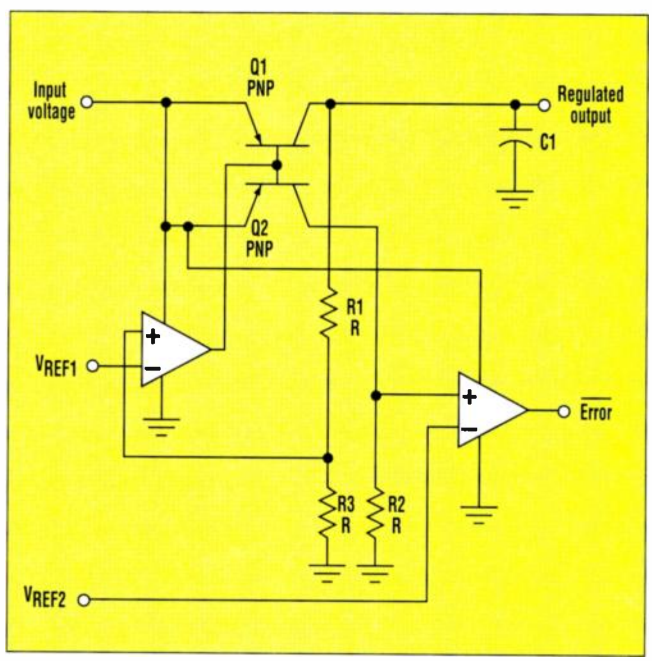
Several manufacturers of regulators provide output signals that indicate a power error condition. These circuits generally monitor the output voltage of the IC and activate a signal if the output voltage falls out of bounds *(Fig. 1)*. This is an after-the-fact error detection. By the time that the microprocessor sees the warning, the output is already out of specification. In the ubiquitous LP2951, the error pin goes low only after the output is already 7.5% below its nominal output voltage. Many logic devices call for regulation within ±5% of nominal. The problem with this type of error sensing is obvious.

The circuit configuration shown senses any interruptions in the regulator input current instead of the output voltage *(Fig. 2)*. This is a more proactive error-detection scheme than sensing output voltage. The input current interruption can be sensed while the output voltage is still within regulation limits, saving valuable milliseconds of operating time. The time gained can be used to do those emergency "clean up" tasks that are required for a safe shutdown while the regulator's output voltage is still within specification.

To accomplish this current sensing, a second PNP transistor (Q2) has been added (in a current-mirror configuration) to the pass PNP of the classical LDO topology. The transistor would be scaled so that Q2 conducts a frac-



1. "Standard" error detection, as implemented on many popular low-dropout regulators, monitors the output voltage only.



2. An improved LDO error detection topology senses the input current interruptions, providing a valuable early warning signal.

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tion of the current that flows through Q1 to limit power consumption. It also is possible that R2 could be sized so that the transistor is normally in saturation (minimizing the power dissipation of this transistor and load). The voltage across this load resistor is compared to a known voltage (V_{REF2}). If this sense voltage is lower than V_{REF2}, then the $\overline{\text{ERROR}}$ pin goes low, signifying an error event.

What distinguishes this approach from the standard ERROR signal of other LDO regulators is that the output hasn't begun to fall at the point the error signal is generated. If one knows how long it takes to finish the longest critical event that the microprocessor performs, it's easy to size the post regulator filter capacitor to keep the voltage drop over this time to an acceptable level. The battery-powered device then can do whatever is required to put the instrument to "sleep" while minimizing the potential for serious instrument malfunctions. This could include the computation and writing of a checksum to EEPROM memory.

In practice, designers would probably want to retain the output-voltage sensing of the conventional LDO circuit. Otherwise the voltage could drop out of regulation with no error detection. Optimally the outputs of the two error-detection circuits (current sensing and output-voltage sensing) could be combined. The LP2951 output is an open collector output. If the proposed current-sensing circuitry was added to this IC, the collectors of the two comparators could be connected. Other enhancements could include a pulse-stretching circuit or a latch on the error output.

Programmable Speed Control Targets Stepper Motors Using 8254

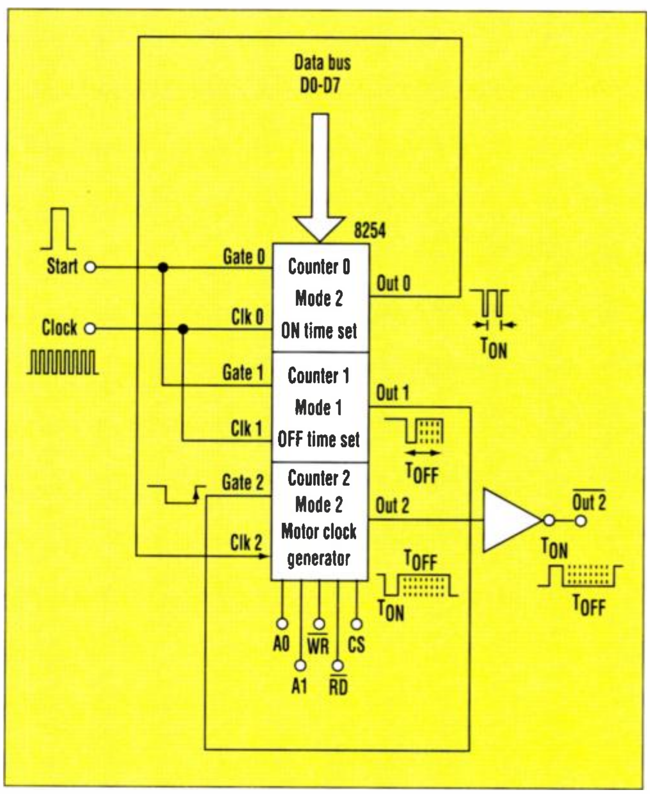
J. JAYAPANDIAN
Materials Science Division, Indira Gandhi Centre for Atomic Research, Kalpakkam, Tamil Nadu, India.

This design idea describes a basic speed controller for stepper motors implemented by programming a common 8254 programmable counter timer IC. The speed control of the stepper motor is achieved by varying the OFF time in its clock's duty cycle. All three counters available in 8254 are used for this purpose.

Counter 0 is programmed in mode 2, which divides the system clock (supplied by a PC, microcontroller, or microprocessor system) connected to its clock input CLK1. The division factor can be calculated from the ON time requirement for the duty cycle of the selected stepper motor and then loaded into the counter register.

The time period T_{ON} of the OUT0 pulse only sets the ON time of the final output *(see the figure)*. Counter 1 is programmed in mode 1 to function as a one-shot whose time period T_{OFF} is set by loading the appropriate word pattern to the counter register. Counter 2 is programmed in mode 2 to generate the final clock output for the stepper motor by receiving the clock with a fixed period T_{ON} and triggering by the one-shot pulse with time period T_{OFF}. The digital word written to Counter 0 will set the ON time, and the word written to Counter 1 will set the OFF time of the stepper clock.

This design provides a motor control output signal with user-programmable OFF times and ON times through simple programming of the 8254 IC. The duty cycle ON time T_{ON} is fixed for the stepper motor but will vary from type to type. The varying OFF time T_{OFF} provides the motor speed control. The "Start" pulse will enable the Counter 0 and Counter 1.



This simple and inexpensive programmable stepper-motor speed controller utilizes the common 8254 programmable timer IC.

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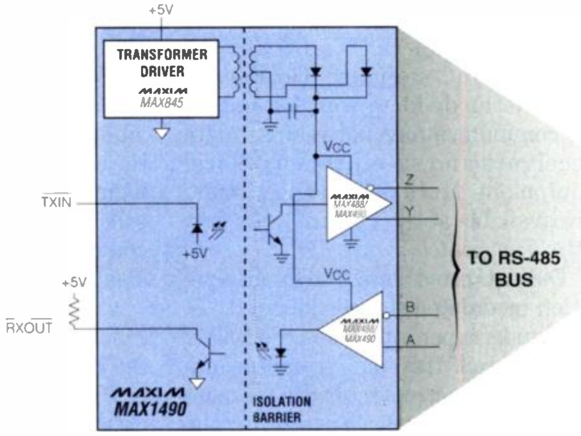

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Circle No. 150 - For U.S. Response
Circle No. 151 - For International

Circle 523

Adjustable LNB Power Supply Is DiSEqC-Compatible

JOHN M. WETTROTH
Maxim Integrated Products, 120 San Gabriel Dr., Sunnyvale, CA 94086; (408) 737-7600.

The circuit shown provides a digitally switchable 13 V or 17 V for the low-noise block (LNB) typically found in satellite receivers at the antenna feedhorn. This variation of supply voltage "tells" the remotely located LNB electronics whether it should set the antenna polarization clockwise or counterclockwise, thereby eliminating the need for an interface and cable connection to the antenna.

The circuit also supports an emerging and more sophisticated communications bus called the DiSEqC standard (for Digital Satellite Equipment Control). Though developed by the European Telecommunications Satellite organization (EUTELSAT), the open DiSEqC standard promises to become the de facto world standard for communications between satellite receivers and satellite peripheral equipment. More details and circuits are available at the DiSEqC web site: *http://www.eutelsat.org.*

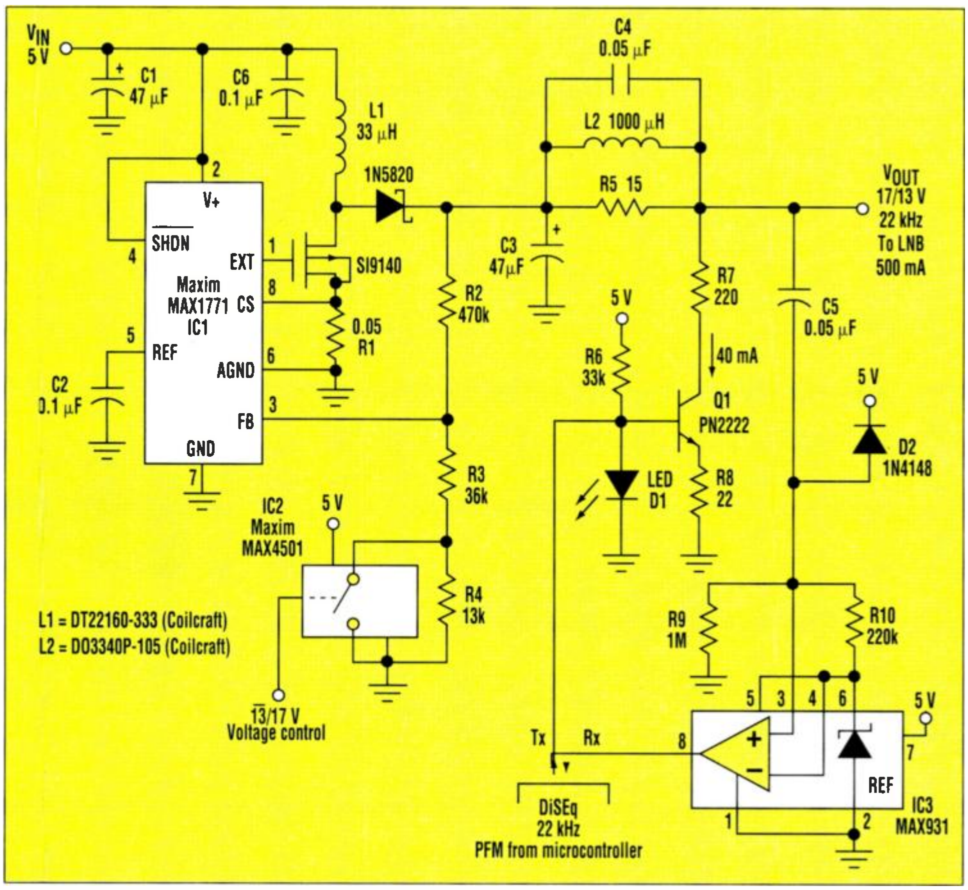
DiSEqC provides a 22-kHz pulse-position-modulated signal of about 0.6-V amplitude, superimposed on the LNB's dc power rail. Its coding scheme allows the remote electronics to perform more complex functions, such as varying the downconversion frequency or physically rotating the antenna assembly.

IC1 is a PFM boost-converter controller that controls an external FET to provide the step-up conversion from 5 V to either 13 V or 17 V. The digital input Voltage Control sets the position of an analog switch that determines the amount of feedback to IC1 and hence the output voltage level. Thus, an input logic low selects 13 V and a logic high selects 17 V. IC2, a single switch that comes in a tiny SOT23-5 package, is ideal for this simple switching task.

Components on the right side of the schematic provide compatibility with the DiSEqC standard. The comparator in IC3 forms a receiver that detects data transmitted from a slave LNB assembly (the DiSEqC standard specifies bidirectional data flow). This output connects to the IRQ or port pin of a microcontroller (not shown) for decoding.

The DiSEqC transmitter consists of transistor Q1 and an LED (D1) that acts as a transmit indicator and as a constant-voltage source that forces a relatively constant current of about 40 mA through Q1. During encoded 22-kHz bursts from the microcontroller, the low portions turn off the LED by sinking its drive current, which forces Q1 off as well. The 40-mA switched current flows through R5, providing 600-mV output swings as required by the specification.

C4, L2, and R5 form a resonant circuit whose impedance at 22 kHz is 15 Ω as required by the specification. The inductor's dc resistance must be 0.50 or lower to accommodate the 0.5-A maximum load currents. The circuit also operates on 12 V, and does so with greater efficiency. When operating at 12 V, consult the MAX1771 data sheet for suitable values of L1 and R1.



1. Designed for the low-noise block (LNB) in a satellite receiver, this DiSEqC-compatible power supply communicates data by toggling its supply voltage between 13V and 17V.

VOTE!

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Circle 524

Transformerless EL Display Driver Uses Low-Voltage 555 IC

DAVE BROTTON
Zetex Inc., 47 Mall Dr., Unit 4, Commack, NY 11725; (516) 543-7100; fax (516) 864-7630; e-mail: dbrotton@zetex.com.

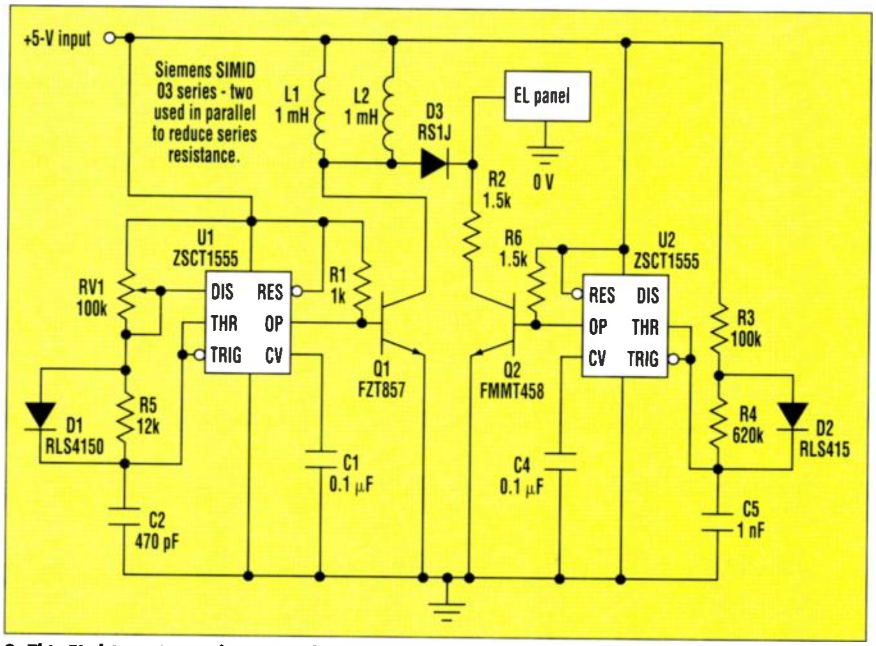
The 555 timer has been manufactured in greater volumes than any other linear IC. Regarded by many as one of the most successful devices of all time, the 555 timer is perhaps only equaled in popularity by the 741 op amp. The success of the part can be attributed to its flexibility, performance, and ability to satisfy the timing requirements of a wide range number of applications. Design demands have changed, though, and the performance of the standard 555 is rapidly becoming inadequate.

The original bipolar parts are used in many applications employing 5-V supplies or higher; while today's requirements often use 3.3- and 3.0-V supplies or lower. The move to low-power circuits and the increased use of battery power also mean that the original 555 quiescent current rating of 5 to 10 mA now proves to be a limiting factor. By producing the 555 in CMOS, manufacturers have already managed to reduce power consumption and operating voltage, with parts developed requiring 250-µA quiescent current and operating at 2 V.

Zetex's ZSCT1555 uses bipolar technology capable of operation from a single-cell battery. The new part can operate down to 0.9 V. Assuming a 5-V supply, a typical CMOS solution draws 170 µA, while the new timer consumes only 140 µA; at 1.5 V, this becomes 75 µA. Shown is the ZSCT1555 quiescent current versus supply voltage *(Fig. 1)*.

Electroluminescent (EL) panels are becoming increasingly popular for backlighting portables due to the advantages they offer over CCFL, LED, and incandescent displays. EL panels are more robust, feature a longer life expectancy (approximately 10,000 hours), have uniform light dispersion, and consume less power. They're usually employed for very low light level viewing, suitable for any equipment featuring an LCD display, including mobile phones, pagers, meters, portable PCs, and automotive instrumentation.

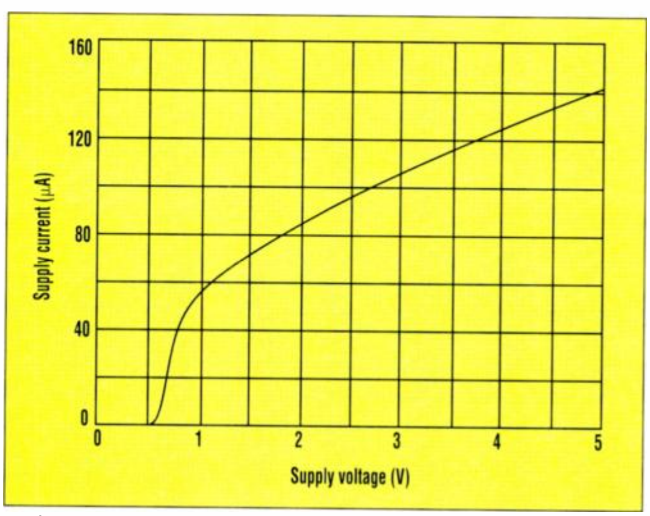
Traditional EL driver circuits feature a flyback transformer design to generate the high ac voltage required to energize the panel. This approach is expensive when the cost of the transformer is considered along with the larger pc-board area it requires. The circuit shown in Figure 2 eliminates the need for a transformer, takes advantage of the ZSCT1555's low power and the efficiencies of the discrete switching transistors.



2. This EL driver circuit eliminates the transformer and takes advantage of the the high-frequency switching capability and low saturation voltage of the bipolar transistors.

The design uses two combined switching circuits. The first generates a high voltage, approximately 200 V using a boost converter. The voltage is chosen according to EL panel size and desired brightness by varying the frequency; the EL panel presents a capacitive load. The second circuit converts the high voltage to an 800-Hz ac signal to drive the EL panel.

The two ZSCT1555 timers are utilized as clocks for the switching transistors. High efficiency is ensured by the high-speed switching characteristics of the bipolar transistors. Advanced transistor design gives the lowest saturation voltage, minimizing power dissipation.



1. The ZSCT1555 quiescent current characteristic has been optimized for single-cell applications, consuming only 0.12 mW at 1.5 V.

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(continued from page 129)
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FEBRUARY 1999

The Wireless Symposium and Exhibition, Feb. 21-25. San Jose Convention Center, Santa Jose, CA. Contact Bill Rutledge, Penton Publishing, 611 Rte. 46 West, Hasbrouck Heights, NJ 07604; (201) 393-6259; fax (201) 393-6297; instant faxback (800) 561-7469; www.penton.com/wireless.

MARCH

Southeastcon '99, Mar. 25-29. Marriott Resort Hotel, Lexington, KY. Contact Don Hill, 1676 Donelwal Dr., Lexington, KY 40511-9021; (606) 257-8487; fax (606) 323-1034; e-mail: d.w.hill@ieee.org.

APRIL

IEEE/PES Transmission & Distribution Conference & Exposition, Apr. 10-17. Ernest N. Morial Convention Center, New Orleans, LA. Contact Grace Juneau, c/o Entergy, P.O. Box 61000, New Orleans, LA 70161-1000; (504) 576-2400; fax (504) 576-5989; e-mail: gjuneau@entergy.com.

41st IEEE Cement Industry Technical Conference, Apr. 11-15. Roanoke, VA. Contact Margaret Peterson, Roanoke Cement Co., P.O. Box 27, Cloverdale, VA 24077; (540) 992-1501; fax 966-1542.

IEEE Radar Conference, Apr. 20-22. Boston, MA. Contact Robert Alongi. 255 Bear Hill Rd., Waltham, MA 02154; (617) 890-5290; fax (617) 890-5294.

MAY

IEEE/IAS Industrial & Commercial Power Systems Technical Conference (I&CPS), May 3-6. Nuggett Hotel, Sparks, NV. Contact Kerry Flannigan, Sierra-Nevada Power Co., P.O. Box 10100, Reno, NV 89520; (702) 689-4848; fax (702) 689-4139.

Sixth IFIP/IEEE International Symposium on Integrated Network Management (IM '99), May 9-14. Boston Park Plaza Hotel, Boston, MA. Contact Judy Keller, IEEE/COMSOC, 345 E. 47th St., New York, NY 10017; (212) 705-8248; fax (212) 705-7865; e-mail: j.keller@ieee.org.

JUNE

IEEE/MTT-S International Microwave Symposium (MTT '99), June 13-18. Anaheim, CA. Contact Robert Eisenhart, 5982 Ellenview Ave., Woodland Hills, CA 91367; (818) 716-1995; fax (818) 713-1161.

JULY

IEEE Power Engineering Society Summer Meeting, July 18-22. Edmonton, Alberta, Canada. Contact Dave Fraser, Edmonton Power Capital Square, Edmonton, Alberta, T5J 3B1, Canada; (403) 448-3554; fax (403) 448-3192.

OCTOBER

IEEE Industry Applications Society Annual Meeting, Oct. 4-8. Civic Center, Phoenix, AZ. Contact Michael Andrews, Andrews Associates, 12438 80th Pl., Scottsdale, AZ 85260.

FEBRUARY 2000

IEEE International Solid-State Circuits Conference (ISSCC '00), Feb. 7-9. San Francisco Marriott, San Francisco, CA. Contact Diane Suiters, Courtesy Associates, 655 15th St., N.W., Washington, DC 20005; (202) 639-4255; (202) 347-6109; e-mail: isscc@courtesyassoc.com.

May

IEEE International Conference on Acoustics, Speech & Signal Processing (ICASSP 2000), May 23-26. Istanbul Hilton & Lutfu Kirdar Conference Center, Istanbul, Turkey. Contact Huseyin Abut, Electrical and Computer Engineering Dept., San Diego State University, San Diego, California 92182-1309; (619) 594-3702; fax (619) 594-3703; e-mail: abut@anadolu.sdsu.edu.

FEBRUARY 2001

IEEE International Solid-State Circuits Conference (ISSCC '01), Feb. 5-7. San Francisco Marriott, San Francisco, CA. Contact Diane Suiters, Courtesy Associates, 655 15th St., N.W., Washington, DC 20005, (202) 639-4255; fax (202) 347-6109; e-mail: isscc@courtesyassoc.com.

AUGUST

IEEE 100th Anniversary Power Electronics Conference, Aug. 25-31. Maui, HI. Contact Robert A. Begun, 23609 Skyview Ter., Los Gatos, CA 95030; (408) 353-1560; fax (408) 354-1403; e-mail: r.begun@ieee.org.

FEBRUARY 2002

IEEE International Solid-State Circuits Conference (ISSCC '02), Feb. 4-6. San Francisco Marriott, San Francisco, CA. Contact Diane Suiters, Courtesy Associates, 655 15th St., N.W., Washington, DC 20005; (202) 639-4255; fax (202) 347-6109; e-mail: isscc@courtesyassoc.com.

FEBRUARY 2003

IEEE International Solid-State Circuits Conference (ISSCC '03), Feb. 10-12. San Francisco Marriott, San Francisco, CA. Contact Diane Suiters, Courtesy Associates, 655 15th St., N.W., Washington, DC 20005; (202) 639-4255; fax (202) 347-6109; e-mail: isscc@courtesyassoc.com.

JUNE

IEEE/MTT-S International Microwave Symposium (MTT '03), June 6-15. Philadelphia, PA. Contact Richard V. Snyder, c/o RS Microwave, 22 Park Place, Butler, NJ 07405; (201) 492-1207; fax (201) 492-2471; e-mail: r.snyder@ieee.org.

AUGUST

IEEE International Symposium on Electromagnetic Compatibility (EMC '03), Aug. 3-4. Boston, MA. Contact John Clarke, CNE EMCS, 24 Althea Dr., Yarmouthport, MA 02675; (508) 362-7195.

FEBRUARY 2004

IEEE International Solid-State Circuits Conference (ISSCC '04), Feb. 9-11. San Francisco Marriott, San Francisco, CA. Contact Diane Suiters, Courtesy Associates, 655 15th St., N.W., Washington, DC 20005; (202) 639-4255; fax (202) 347-6109; e-mail: isscc@courtesyassoc.com.

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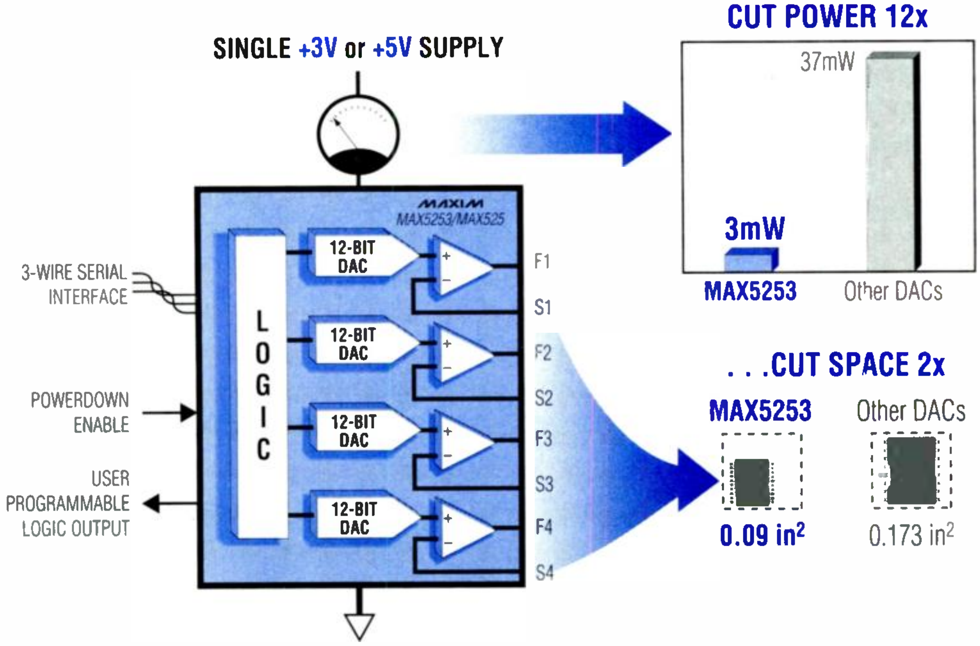

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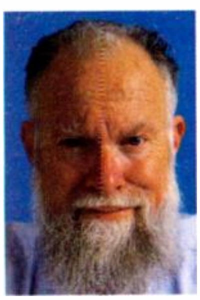
BOB PEASE

What's All This Floobydust Stuff, Anyhow? (Part 6)

Well, it's time for another assortment of miscellaneous, or what I like to call "Floobydust" topics. But first, let's start with the solution for Puzzler 1 that ran in the last issue.

I'll restate it: Four guys named Ari, Ben, Cal, and Don must cross a bridge, but the bridge can only hold two men at a time. It's dark, and they have only one flashlight, which they must use to cross the bridge. If two guys cross using the flashlight, one guy will have to come back carrying the flashlight. (They cannot *throw* the flashlight across.) Ari takes one minute to cross; Ben is slower at two minutes; Cal is slower at five minutes; and Don is very slow at 10 minutes. Everybody must cross within 17 minutes.

If the fastest walker, Ari, crosses with each of the other three guys, and returns as needed, that will take 19 minutes. How can we beat that? Obviously, if the two slower guys each go across separately, there's 15 minutes shot right there. In order to gain any advantage, we have to get the two slow guys to cross *together*. Now do you see the solution?



BOB PEASE
OBTAINED A BSEE FROM MIT IN 1961 AND IS STAFF SCIENTIST AT NATIONAL SEMICONDUCTOR CORP., SANTA CLARA, CALIF.

First trip: Ari and Ben cross. At the end, Ari and Ben cross again. In the middle, the two slow guys cross together, thus incurring a minimum penalty. They can cross together because Ari carried the flashlight back (trip two) and left Ben. After the two slow guys have crossed, Ben carries the flashlight back (trip four) to get Ari. BUT, it does not make any difference if Ari does trip two and Ben does trip four, or vice versa. The total is still 17 minutes. Those are the two solutions. (Jim Ball suggests that Ari can carry each other guy across, taking five minutes total, an elegant rule bender.)

At first, I took about two minutes to work on the puzzle, and I saw the 19-minute solution. I knew I did not have my finger on any 17-minute solution. I then had to get back to work. A few days later I had a few minutes, so I took up the puzzle again, and solved it in three or four minutes. A neat trick. I saw this on the Internet. I'm passing it around not because it is a very hard puzzler, but because it is fun.

My Beetle Dies: I was going to run my 1968 Volkswagen Beetle forever, but it was cruelly murdered by a single steel cable, 3 ft. off the ground, with no flag or warning on it. It wrecked the poor little car's front pillars, bashed in the windshield, and sprung the body—not worth repairing. Fortunately I was only going 4 mph, and only got scratches on four fingers. Not even a bump or scratch on my head. The engine was salvageable, though. The car went to the junkyard at 365,200 mi. It didn't owe me a thing.

So what did I buy to replace it? I was thinking about a good 1968 or '69 Beetle, but I bought a newer car—a clean 1970 Beetle with only 112,000 mi. on it.

GPS Receivers: If you thought that $400, $300, $200, or even $100 is too much to pay for a GPS receiver, how about $99.99? Magellan's new Pioneer has some pretty good features at that price. (Call Cabela's at (800) 237-4444, or your favorite retailer.) I'm sure competitors will be right behind.

I got a good Garmin GPS38 model a year ago for about $170, and it works fine. It even worked fine in Nepal. And, I do not begrudge the $70.01 that I "overpaid."

Altimeters: Okay, a GPS machine is not very useful on a trek in Nepal (where the sherpas know exactly where we are camping, and you can hardly get lost, because there isn't a lot of choice as far as trails go). How about a recording altimeter? My wife wanted one for our trek. I thought that bringing an altimeter was a bit silly. But when my wife gives me a solution to the question, "What should I get her for her birthday," I don't argue. We checked out the Avocet Vertech, a combination watch-altimeter, which costs about $140. It seemed to have the right features.

Nancy wore it on the trip. Was it a silly thing to bring? Nope. The third day on the trail, I pulled into camp at Dharapani, good and tired. Why? Nancy pointed out that even though we had only ascended from 4300 ft. to 6440 ft.—and climbing 2140 ft. did not sound like a lot of work—actually we had ascended a total of 4300 ft., and descended 2160 ft. No wonder I was a little worn out! So, the recording altimeter can provide a sanity check!

The trek involved starting at 2650 ft. at BesiSahar, ascending to 17,771 ft. at Thorong La, descending to Tatopaani at 4200 ft., back up to 9700 ft. at Ghorepani, and down to the road at New Bridge at 3000 ft. That sounds like about 20,600 ft. of rise, and 20,300 ft. of fall. But by the end of the trip, Nancy was able to show that we had actually ascended and descended about 38,000 ft. I was impressed! So I am going to stop being so skeptical about what my wife wants to bring on a trek!

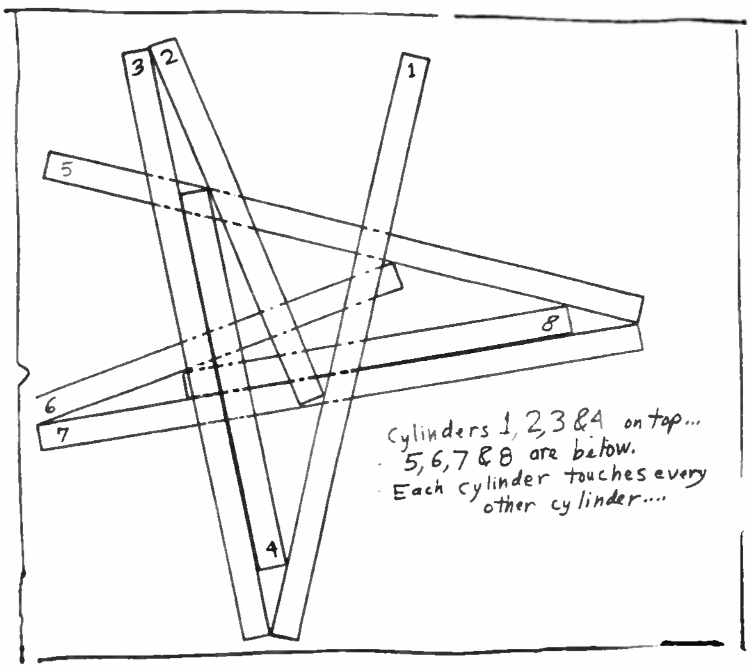
Thermistors: Back in November, I talked about using thermistors over a wide temperature range, such as in your home oven. But who makes thermistors that will cover that wide range? I finally found a data sheet by Keystone Thermometrics located in St. Marys, Penn.; (814) 834-9140. They have one model OVHT(A-1288) that is rated from room temperature up to 500 °C, which is 932 °F, a good safe margin above the 700 °F of a self-cleaning oven.

That's the good news. But are these thermistors inexpensive? The bad news is that this thermistor is packaged in stainless steel for good reliability, and thus is NOT cheap. About $30 in 100's. Also, the gain (logarithmic characteristic) of the thermistor varies by about a factor of 1.8:1, between 50 °C and 250 °C. This is not a serious problem. It would still be fairly easy to make a good oven thermostat using such a device, but it just reminds us that thermistors are not always simple and easy to use, over wide temperature ranges. The thermocouple looks better and better.

Thermocouples: That reminds me—one guy pointed out that in my November circuit for thermocouples, I showed the thermocouple connected incorrectly, backwards. The *red* lead is NOT positive at hot temperatures. The *yellow* lead is. You would have figured this out, if you had built it. I have labeled this kind of thermocouple correctly in the past.

Other Thermistors: Keystone does make another thermistor, type AUHT(A-1291), that is characterized between 250 °C (R = 6.01 MΩ) and 1000 °C (R = 590 Ω). That's pretty impressive! Again, the packaging in stainless steel is NOT cheap—about $40—and it may well be worth it! Do other manufacturers make thermistors rated above 300 °C? I called around and couldn't find a one.

Puzzler Answer: A year ago, I said that you could arrange seven long cylinders so that each one touches the other six. A very small number of readers had the right solution, the same as I did. But one reader came up with a solution of eight cylinders, all the same diameter *(see the figure)*. The long cylinders have to be at least as long as about 22 times the diameter, and the shorter ones have to be about 13 times the diameter—they have to be down near 60% of the long ones. And they all do touch! Each of the eight touches the other seven. I like it!



Servo Circuit: A guy named Jerry wished for a circuit to drive a Screw Motor with a Feedback Resistor Servo. The circuit in my Ball-on-Beam Balancer was pretty good *(ELECTRONIC DESIGN ANALOG SUPPLEMENT, Nov. 20, 1995, p. 50)*. It never gave me any trouble. Since Jerry did not give me a return address, that's the best advice I can give him.

IC Logos: I got a nice book from Karen Mittelstadt at Sams Publisher: *Component Identifier and Source Book*, by Victor Meeldijk, Prompt Publications (a subsidiary of Sams), ISBN 0-7906-1088-4, about $25. It lists all the logos of all IC's made. A useful resource for the library of any big, serious, electronics company. But as several readers pointed out, if you have *IC Master*, you might have a lot of that logo info in there, already.

Epaminandas: After reading my story of Epaminandas , one reader pointed out that you can buy a little book—he searched it out at Amazon Books: *Epaminondas and His Auntie*, by Sara Cone Bryant *(ELECTRONIC DESIGN, Oct. 23, 1997, p. 151)*. At about $12 including tax and shipping, I bought the book. In its 16 pages, it had several drawings of little boys, and about the same story as I told. I think I told it better. Hardly a good investment, unless you are a nut about such stories. But it was amusing to see that it was not out of print.

Books as small as this, with just five pages of text, do not usually get an ISBN number (0-89966-556-x), but this one did. Stories as old as that one do not usually get a 1976 copyright date. But this one did.

One reader upbraided me, because my mother's "abuse" of me (she gave me a whack, which I well deserved, for spilling my milk) caused me to be brutal and abusive to others when I grew up. He claimed I was thus brutal to my children, causing a continuing pattern of brutality. This foolish (and anonymous) writer did not recognize that I plainly stated that when my son tried to pull his glass away, I was careful to not let him spill a drop. I didn't have to whack him. So, Mr. Anonymous, I don't think that a parental swat or spank necessarily constitutes "brutality." I wouldn't buy your theory, even if you had signed your name.

More Speaker Cables: If you want to see some OUTRAGEOUS, preposterous claims about high-end speaker cables, check out these web sites: *www.nordost.com* and *www.cardas.com*.

Taguchi: It seems that most Taguchi experts are not worth wasting your time on. But when Professor T. N. Goh from Singapore University comes to town, I want to see his proposals. He claims he can make Taguchi methods work well. I tend to believe him. (I'm not sure if I should say anything good about Prof. Goh, because I want his success to depend upon what he says, not what I say about him. Still, I want people to attend his lectures. A quandary....)

All for now. / Comments invited!
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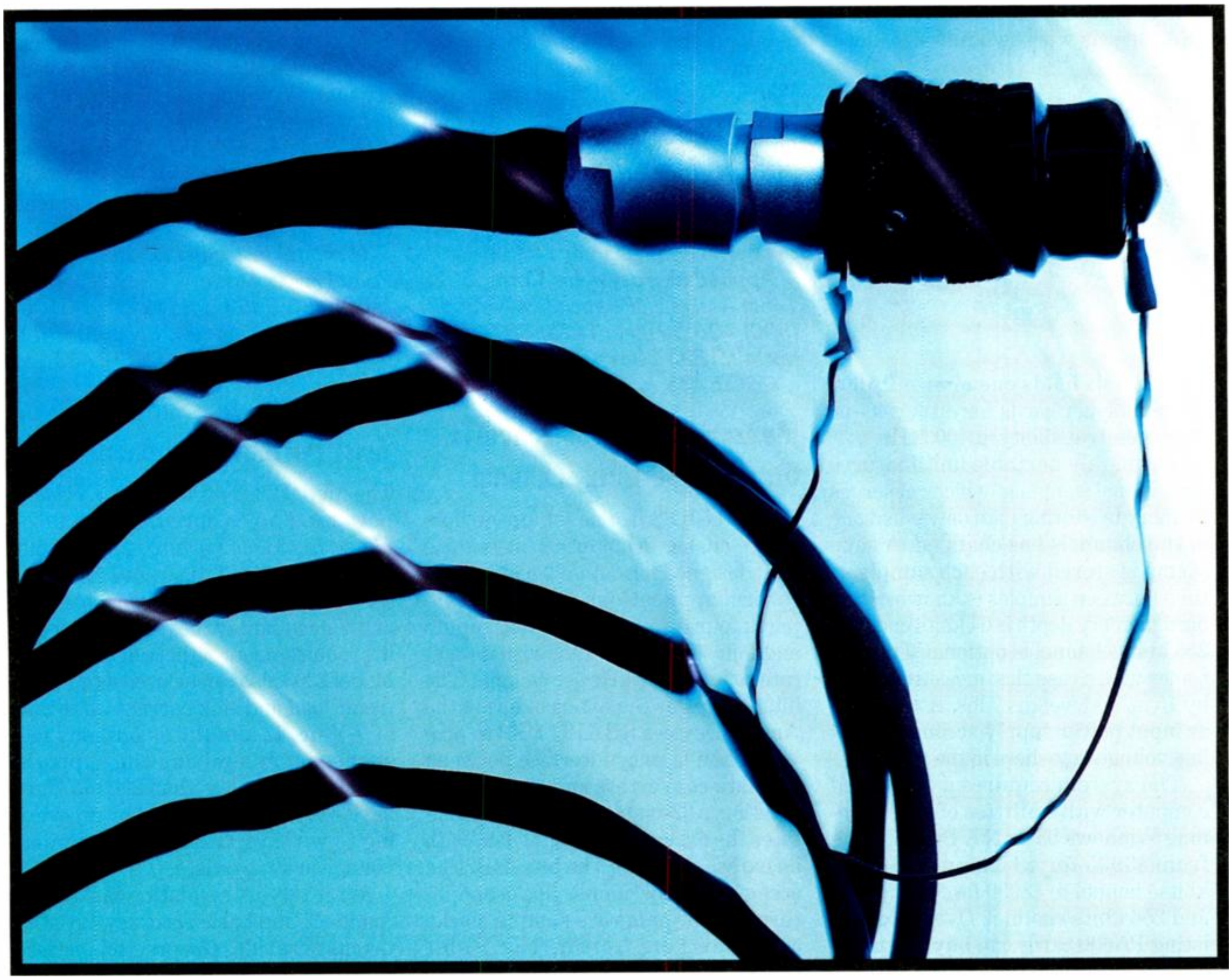

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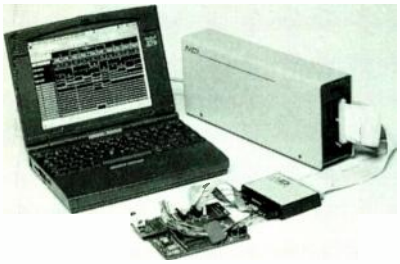


The chassis holds one or two PA600 logic-analyzer cards for either 48- or 96-channel capability at 400 MHz.

The highly portable unit features transitional sampling, which conserves memory by storing data only when one of the channels has changed. A time stamp is stored with each sample so time between samples is known. Standard memory depth is 64 kbits/channel; 256 kbits/channel is optional. The unit comes with a case that measures 3 by 6 by 15 in. and weighs 7 lbs. A universal ac input power supply accommodates line voltage anywhere in the world.

The system requires a 486-based computer with 8 Mbytes of RAM running Windows 95 or NT. Prices range from $3995 for 48 channels and 64 kbits/channel to $8990 for 96 channels and 256 kbits/channel. Owners of existing PA600 cards can buy an empty Mobilogic chassis for $1000. Delivery is from stock. JN

NCI, 6438 University Dr., Huntsville, AL 35806; (205) 837-6667; fax (205) 837-5221; e-mail: nci-usa@ro.com; www.nci-usa.com. **CIRCLE 485**

Integrated Tools Provide Rich Support For PowerPCs

A complete set of tools to create, compile, link, debug, and assemble fast, optimized embedded code is available for the PowerPC. Hosted on Windows NT and 95, Metroworks' CodeWarrior for Power PC embedded systems will be combined with Applied Microsystems' development and testing products—the CodeTAP, PowerTAP, and SuperTAP emulators and CodeTEST software verification tools. The CodeWarrior debugger will directly control the CodeTAP and PowerTAP emulators. This suite offers an integrated project manager, text editor, optimized C/C++ compiler, linker, source/assembly-level debugger, high-performance run control, and high-speed download. CodeWarrior for PowerPC Embedded Systems Developer Release 3 is available for $899. A system package including the CodeTAP emulator for the Motorola PowerPC 8xx family of processors or the PowerTAP emulator for the PowerPC 60x family is $6495. JD

Applied Microsystems Corp., 5020 148th Ave. N.E., Redmond, WA 98052; (800) 426-3925 or (425) 882-2000; fax (425) 883-3049; www.amc.com. **CIRCLE 486**

Mezzanine Adapter Converts Data At 200 MHz/Channel

The bitsi-BB2 is a new high-performance analog I/O interface mezzanine card designed for data-acquisition and control applications. The card supports four differential analog inputs and four analog outputs, with data at rates of up to 200 kHz per channel. The bitsi-BB2 uses the external bus of the Analog Devices SHARC DSP to provide a low-latency interface between the data converters and the DSP. In addition, a 32-bit digital I/O port facilitates the exchange of digital data with an external device. The bitsi-BB2 can accept external sample clocks and interrupts, or generate sample clocks and interrupts from its two 16-bit timers. The bitsi-BB2 is available immediately starting at $1750. JD

Bittware Research Systems, 33 N. Main St., Concord, NH 03301; (603) 226-0404; fax (603) 226-6667; www.bittware.com. **CIRCLE 487**

PCI Board Combines GPIB Controller and Analyzer

The PCI-GPIB+ combines the functionality of both an IEEE-488.2 talker/listener/controller and a complete GPIB analyzer. It's a high-performance interface that can sustain data-transfer rates up to 2.5 Mbytes/s using the IEEE-488.1 three-wire handshake or up to 8 Mbytes/s with the high-speed GPIB protocol. The PCI-GPIB+ can control GPIB instruments as well as troubleshoot a variety of IEEE-488 hardware and software problems. It also reveals GPIB communication problems, such as addressing inconsistencies, protocol violations, simple bus time-out conditions, and more. The PCI-GPIB is completely jumperless and features plug-and-play functionality for any Windows-based analyzer software, and is compatible with LabVIEW and LabWindows/CVI application software. The PCI-GPIB+ is available immediately with prices starting at $795. JD

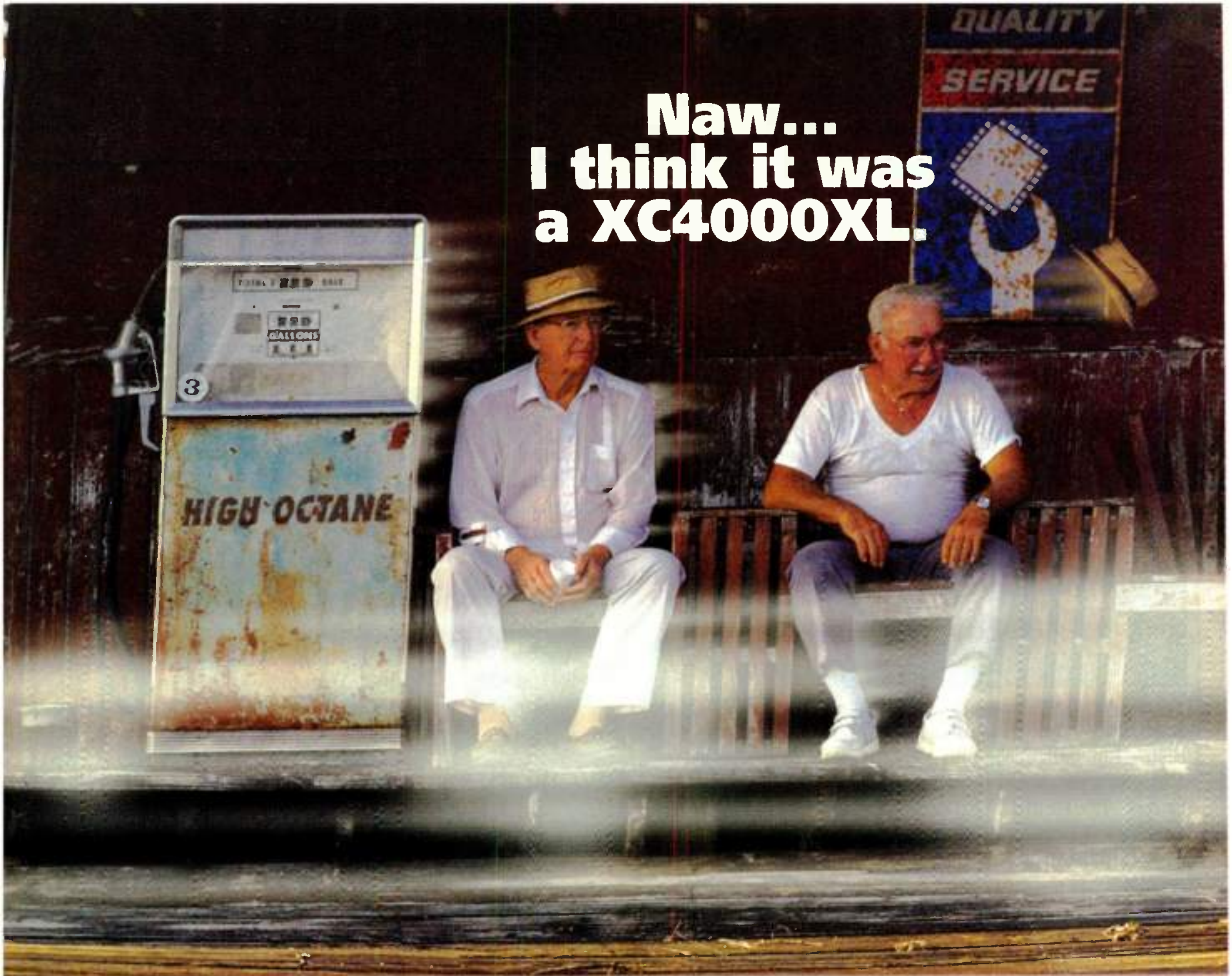
National Instruments, 6504 Bridge Point Pkwy., Austin, TX 78730-5039; (800) 433-3488 or (512) 794-0100; fax (512) 794-8411; Internet: www.natinst.com/gpib. **CIRCLE 488**

Precision Power Supply Tests Portable Equipment

The Model 2303 high-speed precision power supply is optimized for automated testing of portable telecommunications devices. It's rated for 45-W service and can deliver as much as 5 A at 9 V dc to satisfy the peak pulse loading requirements of these devices. The Model 2303 also can be used as an electronic load and sink current up to 2 A at 7 V dc. It simulates battery response by minimizing the supply's voltage drop to less than 200 mV during large load changes and by recovering to within 100 mV of the original voltage in 40 µs or less.

With 100-nA resolution in current readback and basic accuracy of 0.2%, the unit provides the precision necessary to monitor minute sleep mode currents. The Model 2303 can measure both peak and average currents. Furthermore, it's able to make peak current measurements on pulses as narrow as 60 µs, while its long integration mode can average measurements on pulse trains for periods up to 15 seconds. The Model 2303 also provides two digital outputs for control of external devices. Price of the Model 2303 is $1895, with delivery in six to eight weeks. JD

Keithley Instruments, Inc., 28775 Aurora Rd., Cleveland, OH 44139-1891; (800) 552-1115 or (440) 248-0400; fax (440) 248-6168; e-mail: product_info@keithley.com; Internet: www.keithley.com. **CIRCLE 489**



All across America the XC4000XL family is turning heads. Why? Performance. The kind of lightning fast speed you've come to expect only from a gate array. But now you can get that same performance in a high density programmable logic device. Plus all the inherent flexibility that's made Xilinx FPGAs the "time-to-market" choice of thousands of leading system designers.

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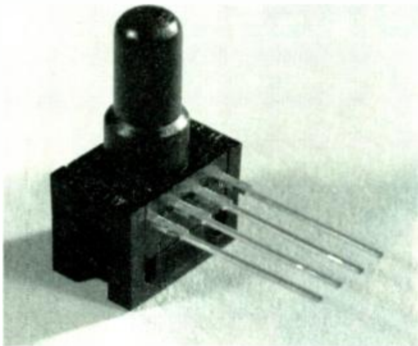
READER SERVICE 185

Mini Absolute Pressure Sensor Sports A Low Price Tag

Honeywell's 24PC Series miniature absolute pressure sensor is aimed at applications requiring highly accurate hysteresis, stability, and repeatability. The low-cost, unamplified sensor offers three pressure-port configura-



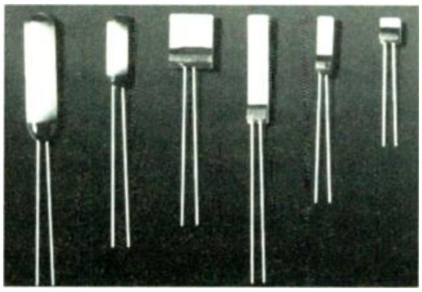
tions. Its package incorporates a patented modular construction that withstands pressures up to 60 psi. The low-power, unamplified, noncompensated Wheatstone bridge circuit design provides stable millivolt outputs over the 2-to-15 or 2-to-30 psi sensing ranges. You can choose from two termination styles: a four-pin inline or a two-by-two arrangement. List price for the 24PC Series sensor is \$15.65, and availability is four to six weeks. LM

Honeywell Micro Switch Div., *11 W. Spring St., Freeport, IL 61032; (800) 537-6945; www.sensing.honeywell.com; e-mail: info@micro.honeywell.com.* **CIRCLE 495**

Platinum Temperature Sensors Offer Rapid Response Times

IRC offers a comprehensive line of precision platinum film and wirewound resistive temperature detectors (RTDs) for industrial, automotive, and HVAC applications. The parts are available in various radial, axial, and space-saving surface-mount packages. All of the RTDs feature high accuracy, long-term stability, and rapid response over a wide temperature range. And they all meet the Class B IEC 751 standards for temperature detection from –200° to +850°C.

The product line includes the ISMD Series miniature surface-mount film sensors; the IGR, IGW, and IGWP Series of radial-lead film sensors; the IA



and IL Series of film sensors with perpendicular leads; the IW60 and IW86 Series wirewound sensors; and the IWS81 Series wirewound compact sensors with highly accurate temperature sensing. Typical pricing for the parts ranges from \$3.00 to \$4.00 in 1000-unit quantities. Delivery is from stock to two weeks. LM

IRC Inc., *A TT Group Company, P.O. Box 1860, Boone, NC 28607; (704) 264-8861 or (512) 992-7900.* **CIRCLE 496**

Pancake-Style Transducer Provides Maximum Life Span

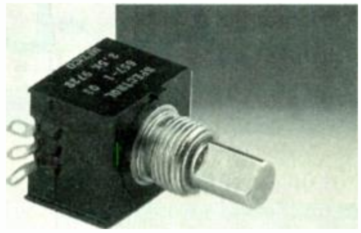
The FN3042S load cell is a pancake-style transducer designed to provide maximum life in high-cycle environments. Life expectancies routinely exceed 10E9. The transducer, which is

available in ranges from 1000 to 100,000 lb., provides ±0.5% FSO performance. A grounding option allows for termination of cable shields to the sensor or to the instrumentation. The part's 17-4 precipitation hardened stainless-steel structure and high-stability metallic strain gages configured in a Wheatstone bridge ensure operation of the instrument with all classic signal-conditioner inputs. Dual-bridge versions also are available. Contact the company for pricing and availability. LM

Sentech Systems Inc., *21814 Harrisburg Ave., Mount Joy, PA 17552 (717) 653-2306; e-mail: ssi@redrose.net.* **CIRCLE 497**

Position Sensor Is Virtually Immune To Physical Damage

Spectrol's Model 657 Super Cube is a position sensor that's virtually immune to damage and therefore able to operate reliably in severe environments. The 5/8-in.^{3} sensor is available with



standard resistance values ranging from 50 Ω to 25 kΩ, power ratings to 0.5 W at 40°C, excellent stability over a temperature range of –40° to +125°C, and up to one million shaft revolutions. The sensors come with or without mechanical stops, and feature electrical travel to 320°. Options include special shafts and bushings, custom wire harnesses in lieu of wire terminals, special ink systems, and high-temperature versions. Pricing for the Model 657 Super Cube is less than \$6.00 each in production quantities, and shipment is four to six weeks. LM

Spectrol Electronics Corp., *4051 Greystone Dr., Ontario, CA 91761; (800) 624-8902 or (909) 923-3313; Internet: www.spectrol.com; e-mail: spectrol@spectrol.com.* **CIRCLE 498**

NTC Chip Thermistors Are Sensitive And Accurate

Arco Electronics offers its CT08 series of NTC chip thermistors that pack high sensitivity and accuracy into a tiny package. The thermistors, which are manufactured by Soshin Electric Co., are aimed at temperature-sensing and temperature-compensation applications in which small size is required. The CT08 chip thermistors come in the full range of industry-standard resistance values. Custom designs are also available. The CT08 series is available in tape reels or in bulk. Pricing ranges from \$0.12 to \$0.40, depending on tolerance and quantities. LM

Arco Electronics, *5310-J Der.y Ave., Agoura Hills, CA 91301; (818) 707-6465 or (800) 441-2726.* **CIRCLE 499**

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READER SERVICE 197

USB Chip Eliminates ISA-Bus On Motherboards

Not all USB solutions fully exploit all available bandwidth. When you do, virtually all of the classic PC legacy ports, such as serial, parallel, keyboard, and mouse, can be located on a single USB connection along with the floppy drive.

With the USB97C100 chip, engineers can design full-featured USB PC monitors, and even make practical the total elimination of the ISA bus on PC motherboards. The USB97C100, which connects ISA-type peripherals to the Universal Serial Bus, is aimed at fully utilizing the USB bandwidth in PC peripheral applications. With two addresses and up to 16 transmit and 16 receive endpoints per address, the USB97C100 can simultaneously attach several peripherals to a single USB connection.

Unlike other USB peripheral controllers, the USB97C100 dynamically allocates data buffers from a 4-kbyte internal memory. The chip's hardware determines the specific requirements of each endpoint and assigns it a buffer of up to 1280 bytes. To further achieve high throughput, the USB97C100 transfers data without intervention by the MCU. Instead, the IC's MMU (memory management unit) combined with its internal DMA automatically transfers USB data packets at the full bandwidth of the USB connection.

The USB97C100 contains the USB transceivers, USB SIE (Serial Interface Engine), SIE DMA controller, MMU with 4-kbyte buffer, 8051 MCU, external 1-Mbyte memory interface, an 8237 ISA DMA controller, and a quasi-ISA peripheral interface with 64 kbyte I/O and separate 1-Mbyte memory space in a 128-pin QFP package. Engineering samples are available now; production quantities are due in the second quarter of 1998. JC

***Standard Microsystems Corp.**, 80 Arkay Dr, Hauppauge, NY 11788; (516)-435-6000; www.smsc.com.*
CIRCLE 500

Eurocard Subrack Boasts Enhanced EMC Shielding

Meeting electromagnetic shielding standards can be a tough hurdle for many applications. Along these lines, the KM6-RF subrack is designed to provide electromagnetic-compatibility (EMC) shielding to 3U and 6U Eurocard bus/board systems operating in the high end of the frequency spectrum. Both VME and Compact PCI boards follow the Eurocard mechanical format. The shielded card frame meets IEEE 1101.10 industry standards. It minimizes intrusion into the board area by using extruded EMC front panels and contact fingers. Users can enhance the screening level of the front panels with an optional finger strip.

The KM6-RF subrack comes in two versions. One has ventilated overall EMC covers and the other has PCV depth covers and Type 2 backplane extrusions. Both are manufactured in 240-, 300-, and 360-mm-deep models to accept a variety of Eurocards. Upgrades are available to customize the subrack in order to meet special shock and vibration requirements. JC

***VERO Electronics, Inc.**, 5 Sterling Ave., Wallingford, CT 06492, (800) 242-2863; www.vero-usa.com.*
CIRCLE 501

Dual-Stage VME Boards Perform Speedy FFTs

Achieving high-performance fast Fourier transform (FFT) capability typically requires an entire multiboard system. GEMINI is the first dual-stage vector processing (fast Fourier transform) board that fits into a single-slot 6U VME form factor, offering the highest DSP performance available. CRI selected Sharp Microelectronics' BDSP9124 processor for its high-performance frequency-domain processing and its optimization for FFT algorithms.

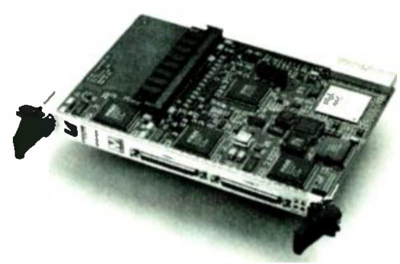
The BDSP9124-enabled GEMINI board is designed to do FFTs, convolutions, correlations, and related DSP functions in a wide variety of government, high-reliability, and industrial applications, including radar, sonar, digital filtering, communications, image processing, spectrum analysis, and electronic warfare. GEMINI also includes the company's simple, plug-and-play software API and System Development Framework.

The GEMINI board uses two parallel Butterfly DSP BDSP9124s to sustain a 1K complex FFT at 27.3 µs—at a continuous 37.5-Msample/s complex data rate. This speed makes the GEMINI board suitable for real-time processing of radar, video, RF, and medical imaging signals. The GEMINI processing board is available now. JC

***Catalina Research, Inc.**, 1321 Aeroplaza Dr., Colorado Springs, CO, 80916; 719-637-0880; Internet: www.cri-dsp.com.* **CIRCLE 502**

RAID Invades CompactPCI As Controller Ups Throughput

Designed for a wide range of storage systems where RAID reliability is required, the CPCI-944 UltraSCSI RAID controller gives OEMs the ability to use RAID technology on the CompactPCI bus. Applications include file servers, on-line transaction processing systems, mission-critical systems, graphic/CAD workstations



and video/imaging systems. An on-board Intel i960RD66 intelligent I/O processor offloads the host CPU by driving disk-array controller functions such as parity generation, RAID algorithms, striping algorithms, and cache management. UltraSCSI data-transfer rates are as high as 40 Mbits/s per channel.

The controller supports three UltraSCSI channels with up to 15 SCSI devices each. Performance and fault tolerance are optimized with support for multiple RAID levels that allows system designers to select the desired combination of storage capacity, data availability (redundancy), and I/O transfer performance for any data application. Support for the controller is available for all major PC server operating systems, including Windows NT, Novell NetWare, OS/2, Banyan Vines, SCO Unix, Solaris, and UnixWare. Pricing is $1057 each in lots of 1000. JC

***Cyclone Microsystems Inc.**, 25 Science Park, New Haven, CT C6511; (203) 786-5536; www.cyclone.com; e-mail: info@cyclone.com.* **CIRCLE 503**

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Expansion Of Design Centers Brings PLD Expertise Closer To Home

Engineers looking for help with their PLD-based designs now have several new sites they can go to for local expertise. The design centers, a total of 10 in the U.S. and other countries, were opened recently by Memec Design Services (MDS), a subsidiary of Insight Electronics.

Memec had already been "teleconsulting," doing design work at all levels, from conception to product end-of-life, notes Tim Smith, director of MDS. In February, the company expanded its capabilities by opening design centers in Boston, Mass., and Ottawa, Canada. In another round of expansion last month, MDS opened design centers in London, England; Munich, Germany; Nesbru, Norway; Van Taa, Finland; Stockholm, Sweden; Zurich, Switzerland; and Guadalajara and Mexico City, Mexico.

"Customers benefit from local access to specialized engineering expertise," say Smith. "We offer established, third-party FPGA and CPLD engineering support." The teleconsulting approach will still be available to customers outside the local areas.

MDS focuses on Xilinx-specific FPGA design work. Application areas include datacom, telecom, digital video, embedded systems, satellites, and others. Services include custom FPGAs, FPGA cores, integration, and board cost reduction. Customers facing obsolescent products can hire MDS to convert end-of-life ASICs to Xilinx devices.

MDS offers free evaluations for projects, as well as low-cost initial consultations and feasibility studies. Insight Electronics is a semiconductor distributor that provides engineering expertise and value-added services to OEMs and contract manufacturers. Memec Design Services and Insight Electronics are both members of the Memec International Components Group. For more information, contact MDS at (602) 491-4311 or go to www.memecdesign.com.

Connector Manufacturer Picks National Distributor

Erni Components Inc. has selected Sager Electronics as its first national distributor. Sager has also been franchised to handle Erni products in the Canadian market.

Sager, which is based in Hingham, Mass., said it will help the connector manufacturer serve the telecommunications, networking, computer, instrumentation, process control, and contract manufacturer markets. The distributor will maintain a deep inventory of Erni's products, in an effort to speed response time and allow just-in-time delivery. "In Sager, we feel we have a strong partner that shares our vision of providing timely delivery of top quality connectors with top quality service at competitive prices," said Willy Rau, president and CEO of Erni Components.

Erni is part of the Erni Group, based near Zurich, Switzerland. The company's U.S. headquarters and manufacturing operations are based near Richmond, Va.

SCSI Cards Distributed By Bell Microproducts

Symbios Inc., which creates solutions for moving and storage of information, has signed a distribution agreement with Bell Microproducts Inc. for Symbios' SCSI host adapter cards. The agreement allows Bell Microproducts to provide product sourcing for its customers, and to integrate a wider variety of PCs, workstations, servers, and application-specific systems into its own value-added operations.

"This partnership represents a unique opportunity for Symbios to leverage Bell Microproducts' position as the primary distributor of Sun Microelectronics' Ultra AX motherboard," said Michael Shapiro, director of distribution for Symbios.

Symbios, which is based in Fort Collins, Colo., focuses on developing partnerships with its customers, including OEMs and resellers in the storage, server, peripherals, and communications markets. Bell Microproducts distributes high-technology products, including semiconductor devices such as memory, logic, microprocessors, and specialty components, to the industrial and commercial markets. The San Jose company's line card also includes computer products like hard-disk, optical, and tape drives; PCMCIA devices; subsystems; and complete computer systems.

CPI Klystrons Now Stocked By Richardson Electronics

Richardson Electronics Ltd. is now handling the line of multistage, depressed-collector (MSDC) klystrons made by Communications and Power Industries (formerly Varian Corp.). Earlier this year Richardson picked up CPI Canada's standard, wide-band, external-cavity klystrons. It is also CPI's worldwide distributor of power transmitting tubes.

The new agreement includes the VKP7990, a popular klystron used in Harris and TVT transmitters. Richardson provides the VKP7990 from stock. It also will be offering MSDC retrofit options for increasing the efficiency of transmitters.

Richardson, based in LaFox, Ill., distributes specialized electron tubes, RF and microwave components, power semiconductors, display products, CCTV, and security equipment. For emergency deliveries call the 24-hour hotline: (800) 348-5580. For more information go to www.rell.com/tubes-r-us/bcstline.html.

Hamilton Hallmark Wins Rights To SBC Controllers

ZF MicroSystems, Palo Alto, Calif., has signed a North American distribution agreement with Hamilton Hallmark for ZF's single-board computer (SBC) solutions. Signing on with the distributor will allow ZF MicroSystems to focus on its core business, noted president David Feldman, who invented the concept of PC/104 and 5-1/4-in SBCs.

For the embedded SBC market, ZF's OEM module technology packs an x86-compatible PC controller with full-motherboard capability and embedded BIOS and DOS into a 2.2- by 3-in. surface-mount component.

Hamilton Hallmark distributes semiconductors, connectors, passive components, computer peripherals, and materials logistics services to OEMs throughout North America.

For more information go to www.hh.avnet.com.

Applications Engineers Boost Customer Support Capability

To boost technical support to their customer base on behalf of their suppliers, Sager Electronics has created an Applications Engineering Department. Besides the company's technically degreed, field-application engineers, the new department will be staffed by product specialist engineers who concentrate on early design intervention, design assistance and analysis, and product recommendations.

In addition, the department will identify technical solutions providing consistent customer service on behalf of the company's suppliers, and develop marketing information to improve direct and indirect services to customers and suppliers. "By creating more effective communications and resource management, Sager's new department will increase productivity and reduce inefficiencies," according to Ed D'Entremont, senior vice president.

To head the department, Sager appointed Gerald Connolly as its new director of Application Engineering.

Catalog Features RF And MW Components For T&M

A 32-page catalog of RF and microwave components for test and measurement applications is available from Richardson Electronics. The publication supplies key specifications, drawings, and prices for components from Amphenol, KDI/Triangle, M/A-COM, QMI, RF Gain, RF Power Components, Stellex (formerly Watkins-Johnson), and Wakefield engineering. Among the products included are coaxial test cables, cable assemblies, coaxial connectors, amplifiers, and other active and passive interconnect devices.

For a copy, contact Richardson at (800) 737-6937 in the U.S. and Canada, at +44 01753-733010 in Europe, or at (603) 208-2200 for other international locations. Or e-mail the company at marcom@rell.com.

Compiled and edited by John Novellino, jnovellino@penton.com, (201) 393-6077.

Linking Between Chips

Many thanks to Ray Alderman for the mention of IEEE 1355 HIC (Heterogeneous InterConnect) in the *ELECTRONIC DESIGN* column of Dec. 1, 1997.

Networks with three or more dimensions certainly are more difficult to build, physically, than two-dimensional networks. The problem is that most networks are still buses and rings—essentially one-dimensional. Off-chip buses, even with the huge amount of development going into making them faster, are improving at snail's pace compared with chip performance.

A two-dimensional crossbar is a great network that ought to be used far more often. It scales much better than buses and rings, but its cost also goes up as the square of the number of ports. One place where it is being used more is within silicon chips. Even with the on-chip bus capacitance of less than 1pF, the poor scalability of the bus limits chip performance.

1355 uses simple point-to-point links between chips, which can be processor, peripheral, or switch chips, or any combination. The switch chips are used on-chip 2D crossbars to give several Gbits/s throughput, even for 100 Mbaud links. These chips can then be assembled into 2D grid networks to extend the use of the two dimensions.

The telephone people found long ago that the crossbar was fine to a point, but that beyond that, the Clos and Fat tree networks gave better total throughput for a given cost. I'm glad you're dealing with these super-scalable architectures in a future column.

You comment that performance prediction for these networks is difficult. It certainly can be. But you might be interested in "The Network Designer's Handbook," by A. M. Jones, et al., IOS Press, ISBN 90 5199 380 3.

This recently published book includes a wealth of simulation results of 1355 networks for a variety of nodes, dimensions, and topologies. The simulations have been calibrated with an actual system built with up to 1024 nodes, which achieves, in some circumstances, a useful throughput of 64 Gbits/s with 100 MBaud 1355 links.

The book also includes a chapter I wrote on physical design, which says, that 2D networks are easier to build than higher dimensions. It also shows how to unfold some of the higher dimensions onto two dimensions, and how to build the Clos and Fat tree networks with conventional, nonexotic, PCB technology.

I'd be very interested to see a similarly thorough piece of simulation and test work giving performance figures of throughput, utilization, and latency for other technologies. One reason these are never published is, as you say, that they are difficult. Perhaps another reason, particularly the buses and rings, is that the results are too embarrassing to publish?

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Ray Alderman responds: IEEE 1355 (HIC or Heterogeneous Interconnect) is an excellent 3D architecture. But, the performance characteristics of 3D architectures are counter-intuitive in many cases. A Fat tree can have paths blocked. A Clos Switch can be blocked at the recipient, where the message will be dropped, and a nondelivery message sent back to the sender. Many times, zealots of a certain topology will simply add-up the bandwidth of each path and tell you that this number is the aggregate bandwidth of the architecture. Not so. Aggregate bandwidth and scaleability are inversely proportional in many 3D architectures. HIC has overcome some of those limitations.

Another architecture that has solved some of these latency problems is Myrinet, a packet-switched mesh that has FIFO's in each node.

But that's a different kettle of fish.

A Graceful Exit

I read the first one or two sentences of your "goodbye" in the Dec. 15 issue of *ELECTRONIC DESIGN*, got upset, and powered on this system.

While waiting for an IPL (boot in today's language) I reread what you wrote. There WILL be a "40 Years Ago" column in *ED*. I really enjoy the column. I don't know why, but I guess it reminds me of some of the water that went under my bridge.

My dad started radio repair in the teen's, I picked it up in the early fifties, was a Fire Control Tech on a submarine, joined IBM as a Customer Engineer in Jan. 1960, and retired in 1991. I still repair tube amplifiers (I can still see the parts, and if I goof, a tube glows a bit red, or a resistor smokes), so I guess that's the reason your column is so interesting and important.

In fact, if the powers that be would allow you to expand the column to a page, and also print a supplement such as you do with Bob Pease' column, I'd REALLY appreciate it.

Bob Walters
Portland, Oregon

Steve Scrupski responds: Thanks for your very interesting comments about yourself and "40 Years Ago."

I didn't do as much repairing as you did, but I did manage to keep things running around my house with the help of an RCA Tube Manual and a Heathkit multimeter.

It was really interesting hearing about your father—in the teens! I started my career with IBM, too, in 1954, right out of college. I worked in Poughkeepsie, N.Y., in a magnetic-core memory group working on the SAGE computers. The computer was based on MIT's Whirlwind; maybe that's why I seem to comment so often on the prominence of magnetic technology back then.

I was just starting to get the hang of things when I was called into the U.S. Air Force for two years. When I got out, I went back to school, taught a while, worked as an engineer, and then moved into the magazine business in 1962, with ELECTRONIC DESIGN. I moved around a little, spent 10 years with McGraw-Hill on ELECTRONICS in the late 60s and 70s, and returned to ELECTRONIC DESIGN in 1978.

We will continue "40 Years Ago." What I would really like is to continue doing the column into the year 2002, so I could comment on some of my own articles which I wrote back in 1962. That would be a kick.

Letters to the Editor, including the writer's name, address, and daytime phone number, should be sent to: Letters Editor, ELECTRONIC DESIGN, 611 Route 46 West, Hasbrouck Heights, NJ 07604; fax (201) 393-0204; e-mail: debras@csnet.net. Letters may be edited for space and clarity. Names will be withheld upon request.

How To Advance In Your Engineering Track And Guarantee Your Survival In The Workforce

Debra Schiff

OK, we can all agree that there are absolutely no guarantees in life, but there are some pretty solid ways to protect your career. There also are a variety of proven ways to garner promotions, raises, and the respect of peers and superiors. Sometimes the most common-sense types of approaches make the most impact, no matter how silly they may sound. "These are the '90s," you say, "I don't need to play games with my employer." Guess what? You do. Play along and we'll see where you are 10 years from now.

One of the smarter approaches engineers can take is to start reading some books by experts on career management. For this article, we're going to take a look at John Hoschette's *Career Advancement and Survival for Engineers*, published by John Wiley & Sons. Hoschette is a senior staff engineer with Lockheed Martin, Sunnyvale, Calif., whose background includes developing infrared sensors for night vision and laser sensors for weapons and helmet-mounted displays. But, Hoschette moonlights as a professional speaker, consultant, and seminar instructor on topics relating to engineering and career development. He's also a member of the Institute of Electrical and Electronics Engineers' (IEEE's) Career Maintenance Committee. If you need to know more about his credentials, e-mail him at *ctsgroup1@aol.com*.

Career Advancement and Survival for Engineers examines all of the elements of the career process from the bottom rung of the rope to leaving the company. The take-home message throughout the book is that no matter how technically proficient an engineer is, that individual simply won't succeed unless he or she knows the process of conducting business. Younger engineering professionals especially need to gain this education because believing that if you simply do a great job you'll get a promotion just doesn't hold anymore.

Finding The Path

Hoschette says that the first question engineers need to ask themselves is: "Are you in control of your career?" You may think that you are, but when was the last time you had a promotion? In order to truly control your career, you must be ready to accept that you're going to be very busy. You're going to be busy planning, working very hard, and managing your circumstances in such a way that you are the primary beneficiary. What you're really doing is putting yourself in a position of power that you may never have experienced before.

In the process of gaining personal career growth power, in order to play the game, the players must know the rules. In engineering, the rules are pretty much the same as most careers, but the engineering path's structure takes a few more twists and turns *(see the figure)*.

Even before engineers rise to the staff level, they have to pay their dues in the lower level positions. These are often called associate engineer, engineer, senior engineer, principal engineer, and senior principal engineer. In the lower levels, engineers are expected to work on assignments that will generally take them about one or two days. As engineers rise to the senior engineer or principal engineer status, the assignments expand to weeks or months, with an emphasis on technical work. Senior principal engineers are primarily responsible for directing large teams of engineers with a variety of backgrounds.

At the staff level, the engineer must make the decision that will truly determine his or her career. Do you want to follow a more technical path or a more business-oriented one? In the most technically focused arena are the fellows. The folks in this part of engineering are the PhDs in the company who typically stay away from management as much as possible, says Hoschette. Fellows tend to be the experts and can be very helpful when it comes to finding shortcuts. The progression usually goes from fellow to senior fellow to principal fellow to chief fellow.

The other technical path is staff engineering. These engineers will hold MSEEs and will concern themselves with system-level problems, as opposed to fellows who will deal with specific characteristics of a product. They are usually the people to whom management turns for scheduling and cost figures. These engineers are looking at the big picture and usually have walls full of flow charts and year-long wall calendars. Their career ladder is short: staff engineer to senior staff engineer to principal staff engineer.

For those who may have a knack for running projects and estimating cost, the program manager might be the right ladder for you. They schedule performance, organize teams, and control funding for programs. These individuals are bottom-line people, primarily because they receive a bonus for all projects brought in on time. The ladder program managers have to climb starts at program manager, steps up to senior program manager, then to principal program manager, to director of programs.

The career ladder in engineering with the highest number of rungs is the management ladder. Managers also are focused on the bottom line. They're also the people who control the raises and promotions. The ladder goes from supervisor to manager to chief engineer to director of engineering to vice president, to divisional vice president to group executive vice president to president to chief executive officer.

Education

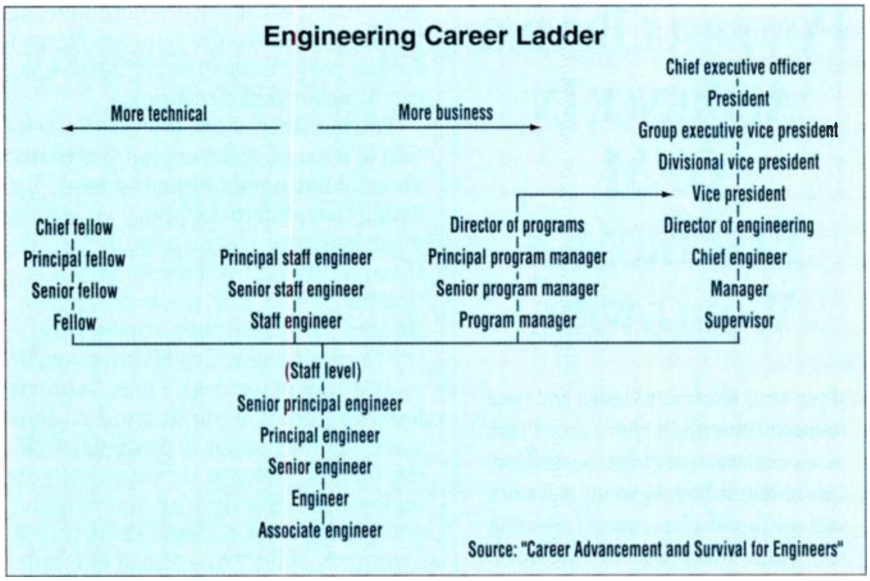
Get familiar with this fact: no matter what you do, if you want to move up in the career ladder, you'll have to go back to school. According to Hoschette, below the first supervisory level, 80% of the engineers have bachelor degrees, 15% hold masters and 5% earned their PhDs. At the director level, the numbers even out a bit. PhDs make up 50% of the directors, 40% have masters degrees, and only 10% just hold bachelors degrees. CEOs are typically (60%) PhDs, but there are some who have multiple degrees or masters (40%).

Employees who wish to pursue further education are encouraged, for the most part, because they will bring new and improved methods back to the company. These new techniques might just save the company money, therefore more than paying for the education. Education costs also are tax deductible, so the company stands to win either way.

Other points made for education in *Career Advancement and Survival for Engineers* include shared knowledge and contacts. Shared knowledge works on the principle that if one employee attends a class, the information that employee brings back to the company will be shared among other employees. This type of communication results in even larger cost savings for the company because many employees have benefitted from the education of only one.

Contacts made by employees who attend classes at technical symposiums can teach the engineers many things. One, for example, is what the competition might be doing. Another might be what the customers would like to see in new products. These contacts, whether they're potential customers or competitors, are an easy way for a company to keep a finger on the pulse of the industry.

Another contact that companies need to keep is one in academia. More often than not, large engineering firms keep university professors on their staff to advise them in high-level technological methods. When an employee attends a class of a new professor, the company now has another way of scouting out technical expertise. Usually these universities benefit by receiving research grants.



This ladder tracks the various paths an engineer's career can take. The big decision is whether to choose a more technical- or business-oriented path.

There are some tricky points with regard to furthering your education through your employer, though. When asking about tuition reimbursement, watch your supervisor's face carefully. If he or she approves, proceed on with whatever your company's policy is with tuition reimbursement. If, on the other hand, your supervisor hesitates or objects, ask why. It could be that the budget simply cannot carry that weight. If that's the case, try asking your supervisor to plan for your education in the next budget cycle. Your supervisor might be objecting because you're needed at work. Assure him or her that you've shown up for your job before and you will continue to do so while you're pursuing your education.

Then, there's the issue of insecurity. Not yours, but your supervisor's. He or she may feel threatened by your going back to school, offering boatloads of excuses why you can't register. While exercising caution, it might be wise to let your supervisor know that he or she would be performing beyond the call of duty by supporting your professional development. The most important thing that Hoschette stresses is that you "do not take 'no' for an answer. It's your career."

Performance Evaluations

Whether you like it or not, you're constantly under the eyes of your supervisor and his or her superiors. They're evaluating your performance every day. The questions you need to ask yourself are: "How are they judging me? What are they looking for?" Basically, there are two types of criteria for evaluation: formal and informal.

Formal criteria come in three flavors: job performance review, job performance guidelines, and promotion review. Although he or she may hate the paperwork, your supervisor must document how you perform in your position. Most of the time this job performance review takes place annually. If you haven't had a performance review, ask for a copy of the form your supervisor has to fill out.

Usually the form asks for the name, education, years in current position, and the like. Then, the form will ask about the employee's performance. Is the employee growing in his or her grade or level? How quickly is progress happening? Does the employee keep up with his or her job requirements? The answers given in this section will determine if you receive a raise or promotion.

There often is a section referring to career development as well. This portion of the review will look at the employee's desire to discuss career development with his or her supervisor. Unless you're taking home more money than you think you should (yeah, right) or you plan on retiring next year, you should definitely be discussing career development with your supervisor. One tip from Hoschette:

don't discuss career development at the same time you're being reviewed for job performance. Schedule a separate time for that discussion.

During the review, pay close attention to what your supervisor has to say about what needs improvement. By listing these points for you, your supervisor is giving you an assignment; do these things and you'll get the promotion next time. But, under no circumstances take these points personally or try to rebut them. It will hurt you. If your supervisor really comes down hard on you, you might want to consider whether or not to continue working for that person. Be sure that you understand exactly why you're being critiqued in certain areas. Then, turn it around to ask: "Are these the only points I need to address to grab that promotion next time?"

Informal criteria are tough to pin down. The most important thing to do to identify them is to listen carefully. Subtle hints dropped by supervisors can run the gamut. These hints are often based on personal tastes or opinions drawn from experience or family background. Unfortunately, some of them can be based upon things as shallow as your appearance, but as we all know, not every job allows you to come to work in shorts and sneakers.

Pay attention to how your supervisor dresses and wears his or her hair. If he or she tends toward the formal, for example, suits, you may want to rethink your wardrobe choices if you're not dressing in the same vein. How you wear your hair can have equal importance. If your supervisor's hair is finely coiffed and yours is long in need of a trim, it may be time to see a stylist.

Look at your supervisor's office. Is it in the same shape as yours? Is it tidy and organized? Is yours? According to Hoschette, "It is a good idea to mimic your supervisor in dress and office appearance unless your supervisor is clearly a maverick in the company."

Methods of information presentation also are an invisible key to informal criteria. They're also a good way to gauge the way your communication techniques are being understood. Typically, there are two types of people, verbal and graphic. The verbal people use words to express their thoughts and the graphic people map out their ideas through pictures. If your supervisor is a word person and you tend to draw out your thoughts, you'll probably have a challenging working relationship. Try to meet your supervisor on his or her own ground. It will help you in the long run, in any interpersonal communication.

Then, there are the results-oriented supervisors and the people-oriented supervisors. In order to deal with results-oriented supervisors, save the home-life details for people who are really interested. They're not. They only want to hear about how you are doing in your work and how soon you'll be done with your current project. The people-oriented supervisors, on the other hand, need to hear about your family life, what you may have done on the weekend, or how your new car is holding up. Remember to also ask them how their spouses are doing (if they have them) or what books they've read recently.

The Take-Home Message

Taken independently these tips and hints may seem like trivial things to focus upon, but they add up. Keeping your job and advancing in the direction that will bring you to the comfort level you're seeking are dependent on the way that your supervisors see you. Whether you want to or not, it's in your best interests to play the game. Getting the raises and promotions that you deserve simply is not based on hard work any more. It's about listening to superiors and paying attention to their attitudes and behaviors.

The best part about changing the way you do things in your career is that you can use all of the techniques and skills in your life outside of the workplace as well. *Career Advancement and Survival for Engineers* features many more time-proven ideas and practical assignments for employees who are truly serious about climbing that career ladder. By using this tool to become an observant, career-savvy engineer, you'll see improvements in your communication skills across the board, leading you to become the source of information for your peers, superiors, and people outside the work environment.

For more information, contact John Hoschette, CTS Group, 3650 Buckley Ave., Suite 403, Santa Clara, CA 95051; telephone (408) 985-1499; e-mail: ctsgroup1@aol.com.

Debra Schiff is chief copy editor at Electronic Design.

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