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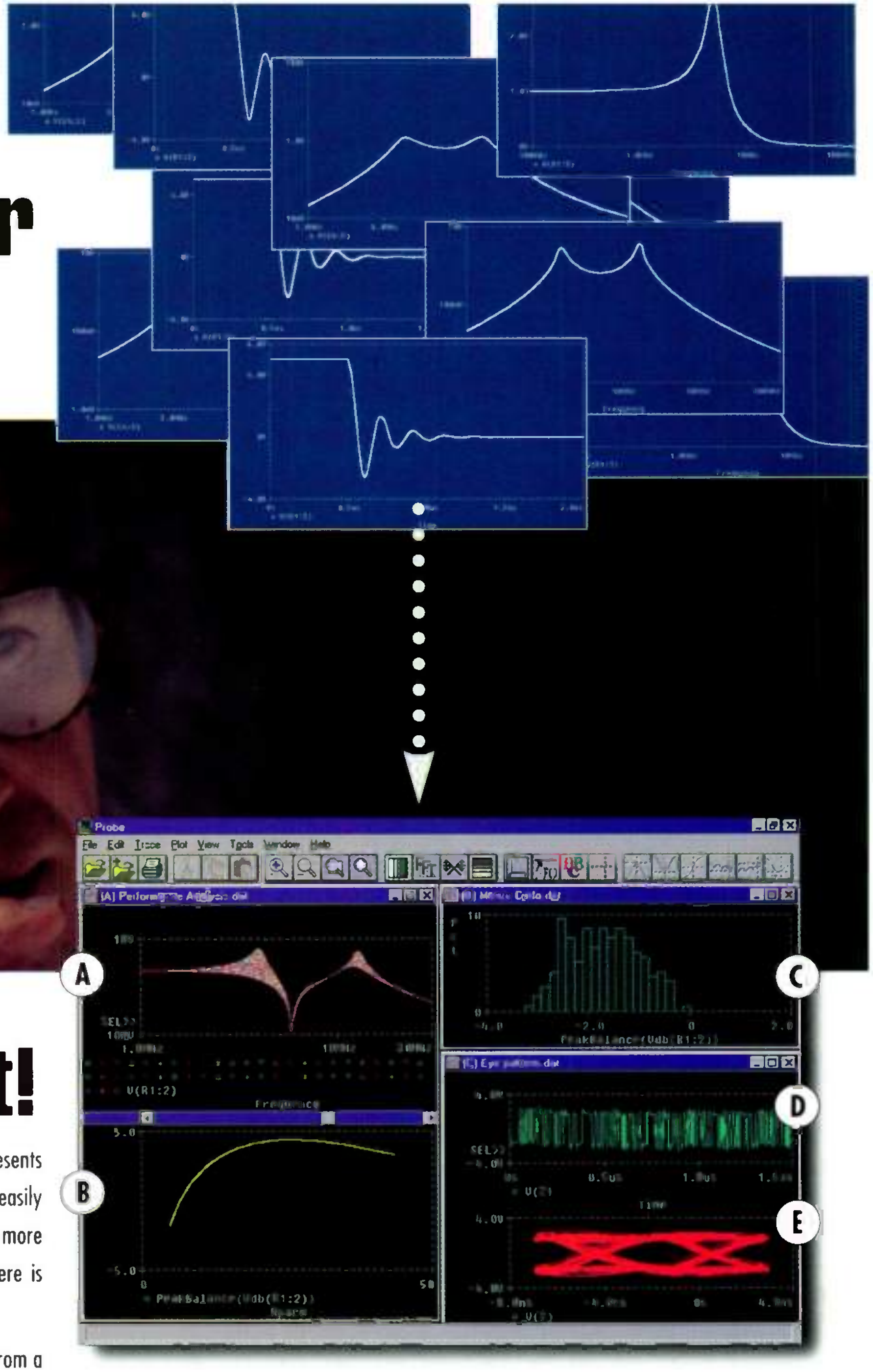

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1967 First Place Award	1978 Certificate of Merit
1968 First Place Award	1980 Certificate of Merit
1972 Certificate of Merit	1986 First Place Award
1975 Two Certificates of Merit	1989 Certificate of Merit
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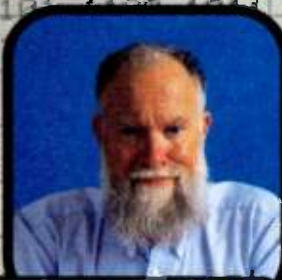

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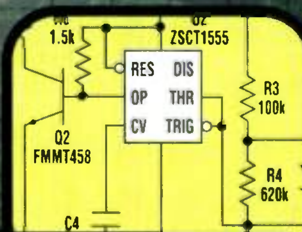
If you're searching for market-related information, recommended reading, or need a laugh, the Community pages have what you're looking for. Click into the Book Shelf, ED University, or Comedy Club, and see what else is out there beyond the workbench!



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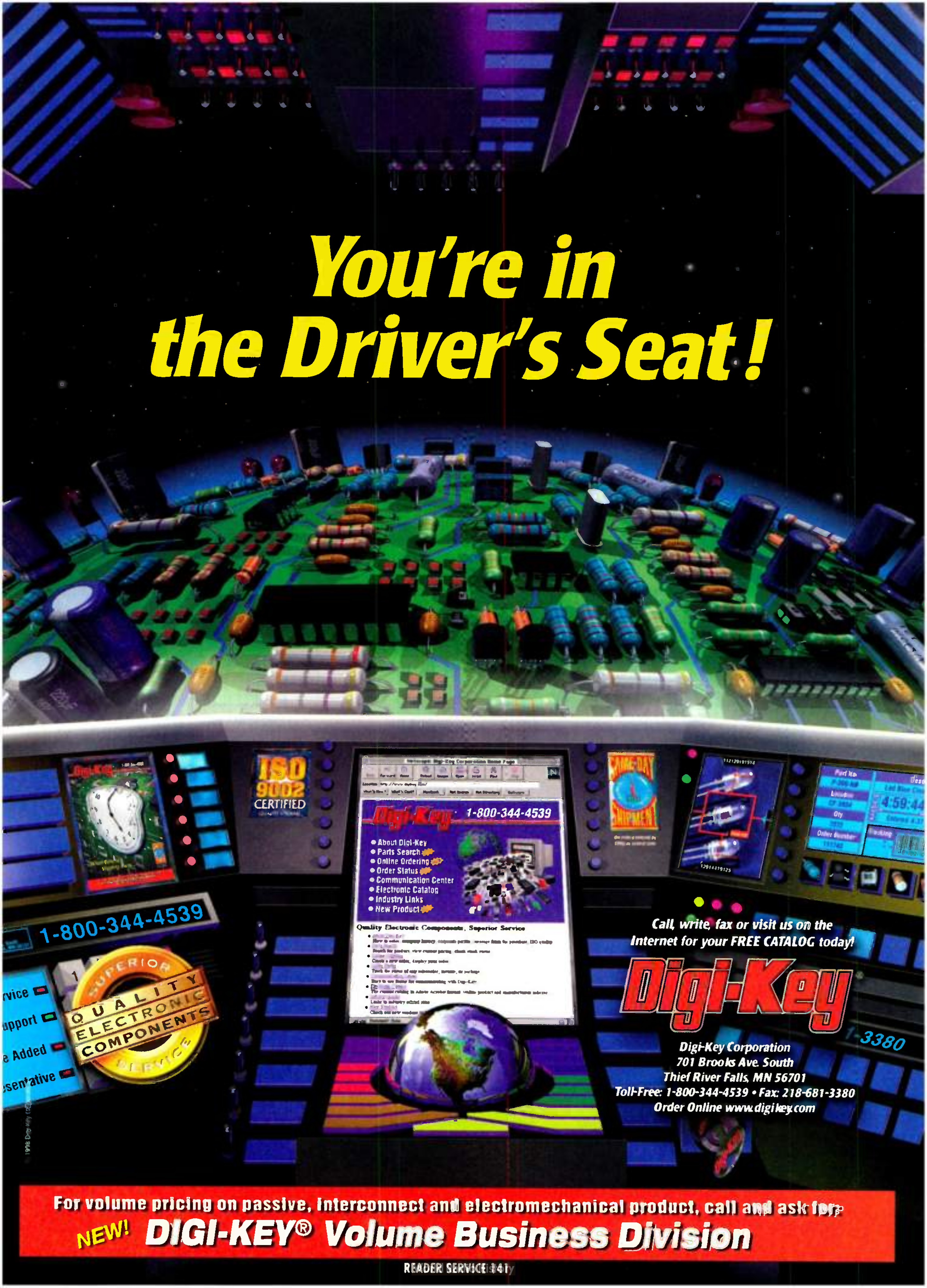

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IEEE Power Electronics, Specialist Conference (PESC '98), May 17-22. Sea Hawk Hotel & Resort, Fukuoka, Japan. Contact Tsutomu Ogata, NTT Integrated Information & Energy Systems Labs., Midori-cho, Musashino, 180 Japan; +81 422-59-2350; fax +81 422-59-2347; e-mail: ogata@ilab.ntt.jp

IEEE Vehicular Technology Conference (VTC), May 18-21. Westin Hotel, Ottawa, Ontario, Canada. Contact Tara Hennessy, Industry Canada, 300 Slater St., Ottawa, Ontario, K1A OC8, Canada; (613) 990-4711; fax (613) 952-5108; e-mail: hennessytara@ic.gc.ca.

Fourth PC Developers' Expo & Conference, May 18-22. San Jose Convention Center, San Jose, CA. Contact Anna Brooks (800) 690-3858 or (619) 673-0870; fax (619) 673-1591; www.annabooks.com., e-mail: expo@annabooks.com.

48th IEEE Electronic Components & Technology Conference (ECTC '98), May 25-28. Sheraton Hotel & Towers, Seattle, WA. Contact Components Group, EIA, 2500 Wilson Blvd., Arlington, VA 22201; (703) 907-7536; fax (703) 907-7501; e-mail: judya@eia.org.

IEEE International Symposium on Circuits & Systems (ISCAS '98), May 31-June 03. Monterey Conference Center,Monterey, California. Contact Sherif Michael, Department of Electrical & Computer Engineering, Naval Postgraduate School, Monterey, California 93943; (408) 656-2252; fax (408) 656-2760; e-mail: michael@ece.nps.navy.mil.

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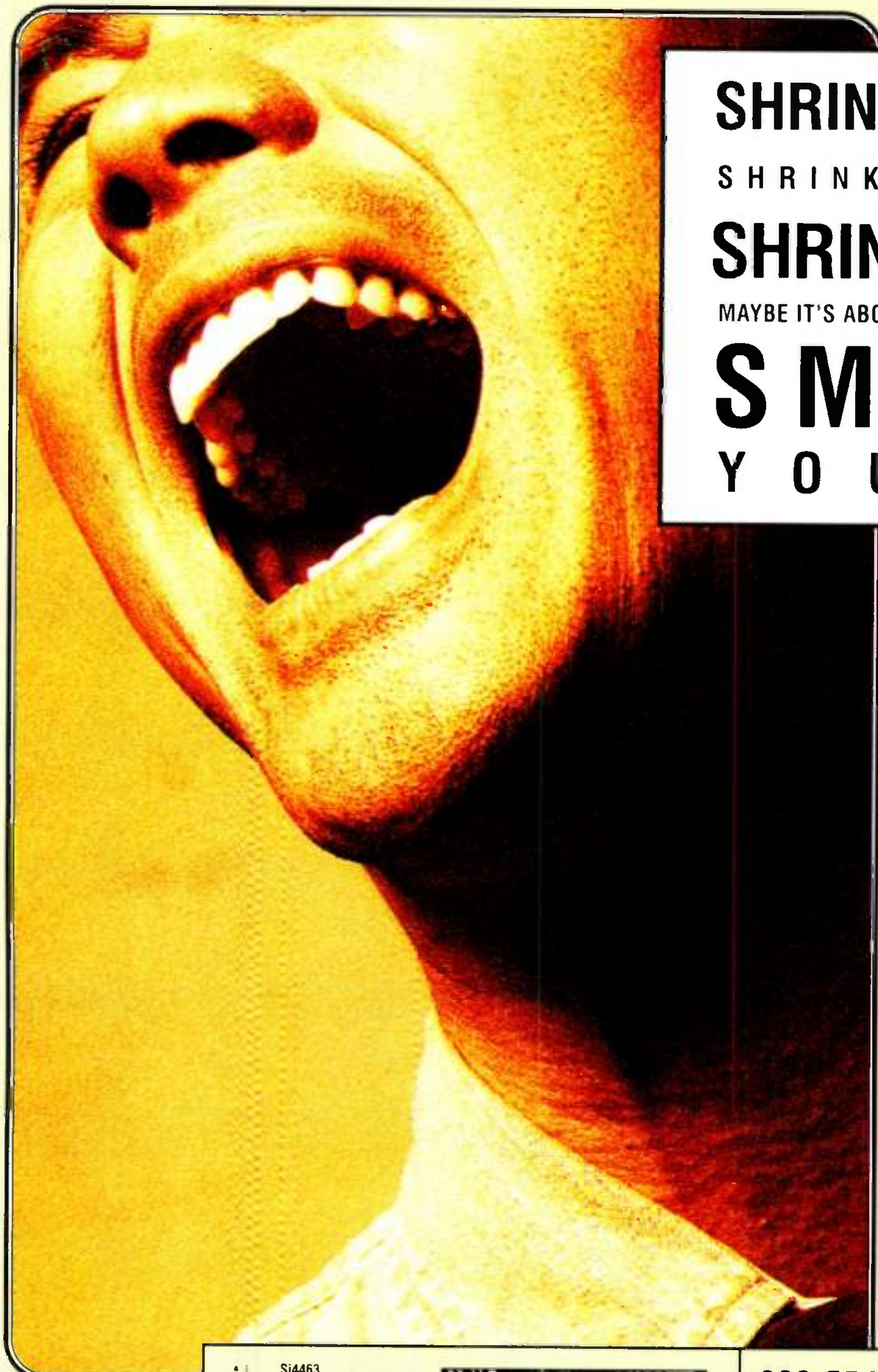
IEEE 25th International Conference on Plasma Sciences (ICOPS), Jun. 1-3. Raleigh Plaza Hotel, Raleigh, North Carolina. Contact Sharon D. Moore, Continuing Education Specialist, North Carolina State University, Box 7401, 147 McKimmon Center, Raleigh, North Carolina 27695-7401; (919) 515-8165; fax (919) 515-7614; e-mail: s_moore@ncsu.edu.



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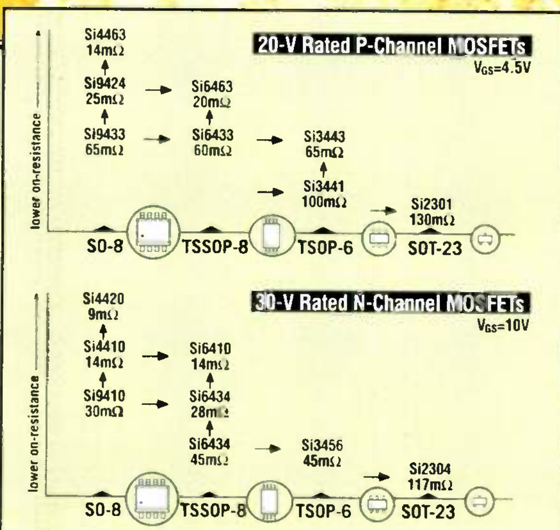

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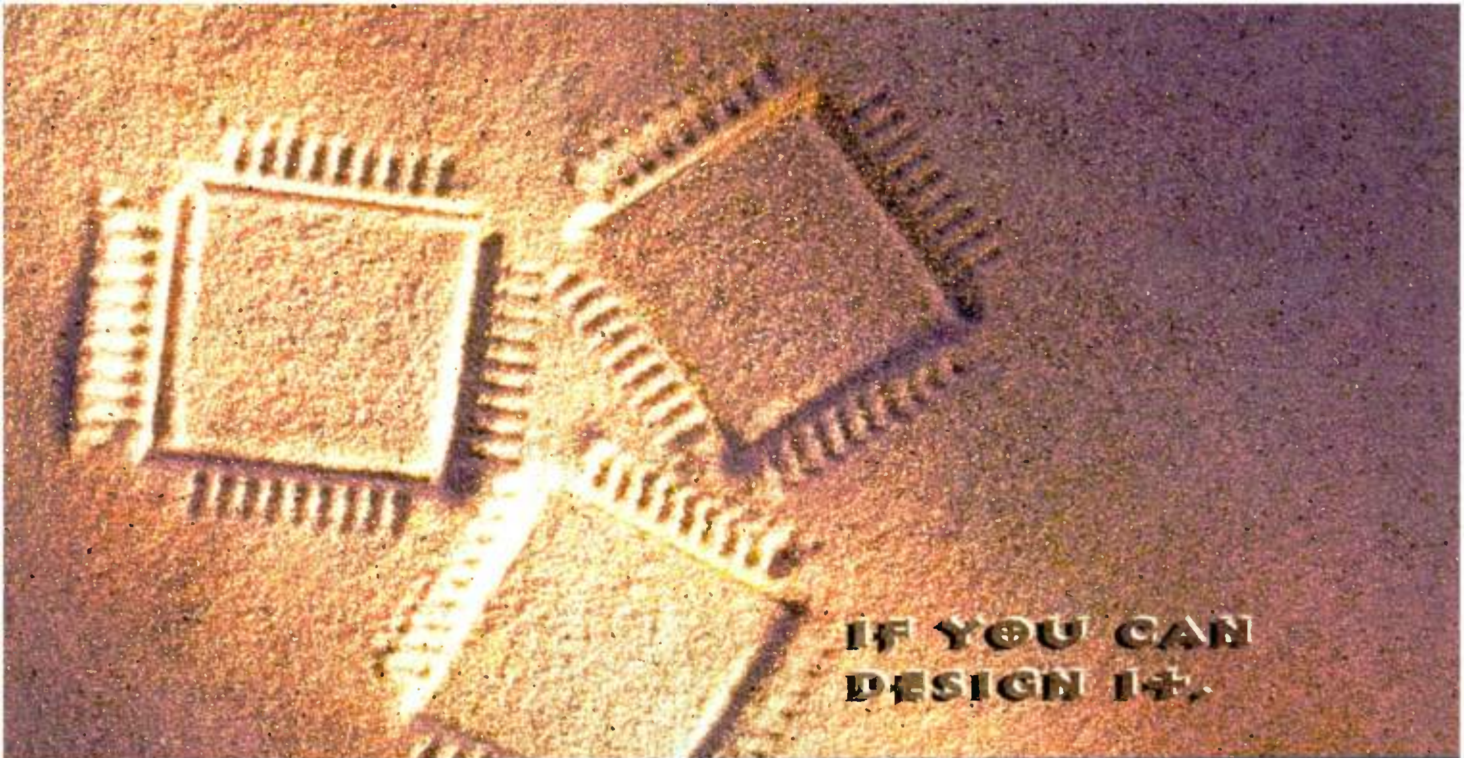

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We're In The Information Age

Brian Halla, chairman of the board, president, and CEO of National Semiconductor, Sunnyvale, Calif., recently asked, "How many people use a PC to compute?" No one in the audience of semiconductor executives at the Semico Research Corp., Phoenix, Ariz., conference raised a hand. Halla used the question to back up his point that we have moved beyond the time when computers were employed to do actual computing.

According to Halla, we have migrated away from the Computer Age, and are now knee-deep in the Information Age. From here on, the computer (in a variety of forms) is the primary vehicle for gaining access to a world of real-time information.

Can't argue the point. When I want to crunch numbers, play with forecasts or statistics, I whip out my nine-year-old HP business calculator. It has all the horsepower and intelligence I need. It boots up instantaneously, is extremely portable, doesn't mandate the latest version of Windows, and requires absolutely no maintenance or support contract.

What Halla and other ship and computer executives are talking about nowadays is the belief that the public's thirst for access to information will be quenched by an array of low-coast (sub-$1000) information appliances. And, from the statistics I've seen, they're right on target.

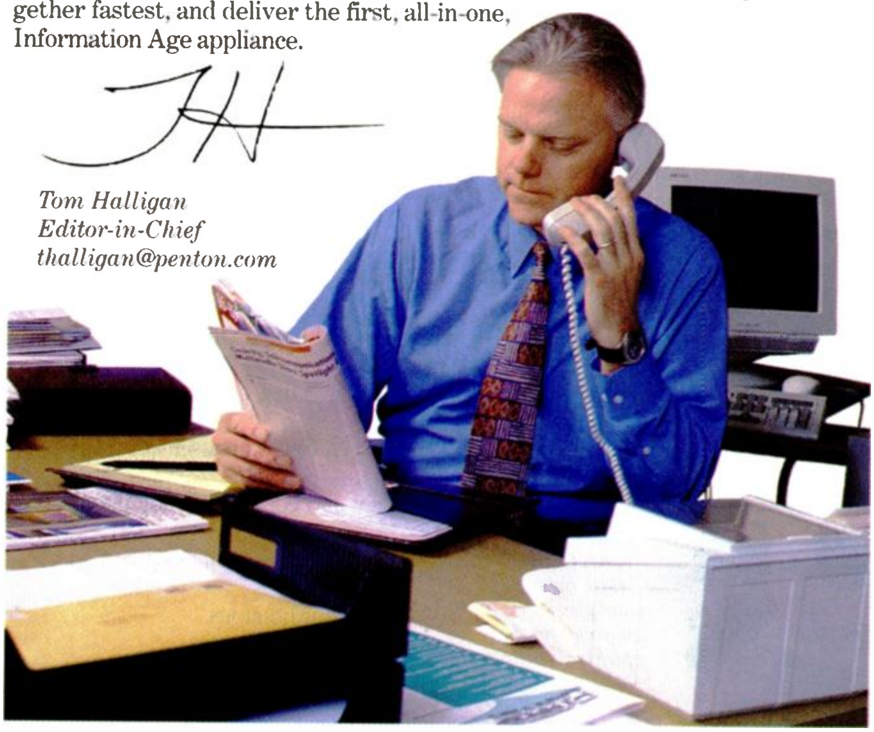
Of course, he has a lot riding on the information age. When Halla took over the reins at National a couple of years ago, he reshaped the company to focus on a system-on-a-chip strategy. In fact, National just publicly announced a new system-on-a-chip that is set to ship June 1999. The 266-MHz chip features graphics, audio, network, and communications capabilities.

National isn't the only company working toward the goal of delivering an all-in-one information technology to the masses. The mission is to deliver an appliance that sits in your family room where you can have access, via a wireless keyboard, to a high-definition monitor where video, audio, multimedia, communications, Internet, and arcade functions are at your fingertips.

I purposely left out "work," because I just don't see any productive work being done in a family or living room. Hmmm, should I finish the article or click over to that neat, new interactive Internet game? You get the point.

The success of such a box will come down to price and marketing. The technology is there to make it happen. It will be interesting to see who can pull it all together fastest, and deliver the first, all-in-one, Information Age appliance.

Tom Halligan
Editor-in-Chief
thalligan@penton.com



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I'm A Believer

After sitting through two multiday conferences focusing on the topic of intellectual property (IP) for the semiconductor industry, I feel very optimistic about the future of the IC industry. However, unlike the religious fervor associated with cult indoctrinations, I came away with a strong belief that the semiconductor industry has taken the proper steps in nurturing IP from its early, faltering steps to its current preadolescent stage. Additionally, the industry has set in motion various standards organizations and activities that will help guide the maturation of IP into a strong and solid technology. This technology will lend its muscle to the Herculean task of implementing chips that contain tens of megagates.

Today, most design-tool suppliers estimate that a good designer can craft new circuits at the rate of about 100 gates per day. Such productivity is woefully inadequate to achieve the six-to-12-month turnaround times demanded by system developers who must have megagate-complexity chips for advanced systems. Thus, reuseable circuit blocks can end up increasing productivity by 10-to-100 fold. Circuit designers can pull multiple, large-circuit functions (CPU cores, bus interfaces, multimedia engines, communications blocks, etc.) from a library, add some application-unique circuitry, and then rapidly assemble all the blocks into a single, highly-integrated chip.

DAVE BURSKY
DIGITAL ICs

But, as was pointed out at both the Silicon Strategies and IP'98 conferences by speaker after speaker, most IP blocks are not really ready for prime time. They are either missing some of the support elements such as test vector files, or timing information, or they have not been made general enough to merge with most design systems. Most blocks of IP must be massaged or significantly modified before they can be used in most design flows. Additionally, there are many other issues, some business related, that are still in their embryonic stages and must be addressed—licensing fees and/or royalty payments, and data security to prevent unauthorized reuse. More importantly, for the system designer, failure responsibility must be determined.

Many of the presentations at both conferences focused on approaches that intend to standardize the interfaces to the IP blocks, or define a standard set of support information that should be included along with the block's HDL description or the physical block description (in the case of a "hard" block). Once the block interfaces are a bit more uniform, the majority of a design can be done at a higher level of abstraction. Rather than focus on small-circuit blocks such as multipliers, data paths, and the like, designers can "assemble" most of their desired chips from cores: a CPU here, a DSP block there, an MPEG decoder, etc. Such a high-level design considerably reduces the design turnaround time, when everything comes together perfectly.

The software industry is also in same state. At the recent JavaOne conference, many companies were demonstrating Java Beans, small Java programs (applets) that are "encapsulated" with a standard interface that allows them to be plugged into an overall software framework. These Java Beans are, in my mind, the equivalent to the megacell building blocks in the IC industry. Perhaps the IC vendors might observe how well the Java industry seems to be cooperating to allow the mixing and matching of the Java Beans to create the desired blend.

The ASIC industry as a whole, though, is not quite plug-and-play yet. It is getting better, and in another few years, I think designers will see tremendous gains in system-chip design productivity. In the meantime, it will take the effort of many semiconductor companies and EDA tool suppliers working in lockstep to create the standards and tools that will be needed. These firms also need to work in tandem to update existing IP and design new IP blocks to follow the new standards. This cooperation will make designing a chip as easy as building miniature houses with an Erector Set or Lego blocks.

Dave Bursky can be reached at dbursky@class.org.

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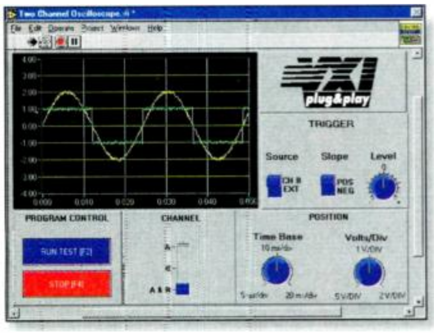

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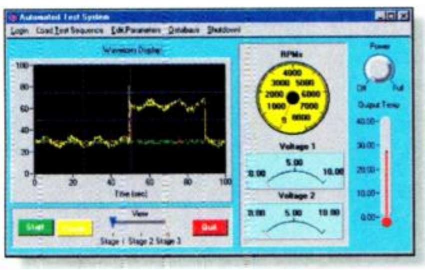

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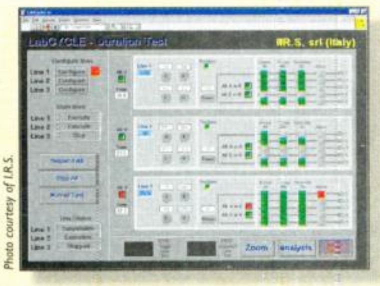

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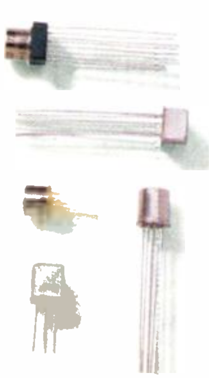

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READER SERVICE 98

ICCE Unveils Algorithms, Circuits That Offer More For Less...

Digital technology's splash into what was once the unquestioned domain of analog entertainment electronics has forever altered the landscape of stereo systems, television receivers, home theaters, cellular communications, and other consumer products. At this year's IEEE International Conference on Consumer Electronics, May 31-June 4, at the Los Angeles Airport Marriott Hotel, Calif., presentations will cover a broad range of topics, from advanced VCR circuits to set-top box architectures to personal communication solutions.

Tutorials on Sunday and Monday, May 31 and June 1 provide designers with updates on the latest technologies—a pair of 3-1/2 hour presentations on Sunday evening let designers either get an update on the latest details of the IEEE1394 serial bus, or an overview of the ATSC digital television standard. On Monday are six similar length tutorials that cover "Video Format Conversion," "Digital TV: Transmission System & Receiver Design," "European Digital Television Broadcasting Systems," "Video Coding Tools in MPEG-4," "Security Systems for Digital Television," and "Digital Cordless Telephony."

The rest of the conference will consist of 28 technical paper presentation sessions that cover a myriad of topics, plus a special poster paper session and an evening panel that discusses the "Advanced Digital TV Roll-Out Scenarios" in transporting or storing digital video images. Image size is a key concern to minimize transmission time or maximize storage. In trying to solve some of those issues, Session 3 focuses on new approaches to coding images by using Fractals, visual block pattern truncation, DCT-based Wavelet transform coding and other techniques, while Sessions 4, 7, 9, 10, 15, 21, and 22 all detail developments in many aspects of digital video.

...Such As In Digital Television And Cable Systems...

For example, Sessions 4 and 10 focus on digital TV video decoders and system architecture and testing. Session 7 explores digital camera designs, while Session 9 examines improvements in motion-estimation and compensation algorithms for better image coding. Sessions 21 and 26 focus a bit more on improvements to redisplay images on the receiver, with presentations highlighting picture-in-picture processing, better image filtering and stability, digital video encoding and decoding schemes for NTSC/PAL, and PC-based video phones. Session 27 discusses the merging of the PC and television when it comes to video and graphics. Topics include 3D graphics, scan conversion techniques, a Java-based video editing system, a distributed and collaborative graphics rendering system, and multimedia synchronization techniques.

Communication systems, both satellite and base-station based, also receive lots of attention at this year's ICCE. For instance, Sessions 23 and 28 are devoted to OFDM (orthogonal frequency division multiplexing) and related topics to show off the latest techniques in designing digital-video-broadcast receivers and improving front-end performance. Session 22 examines the latest developments in cable networks, while Session 18 takes a look at the latest architectural approaches in the design of cable and satellite set-top boxes.

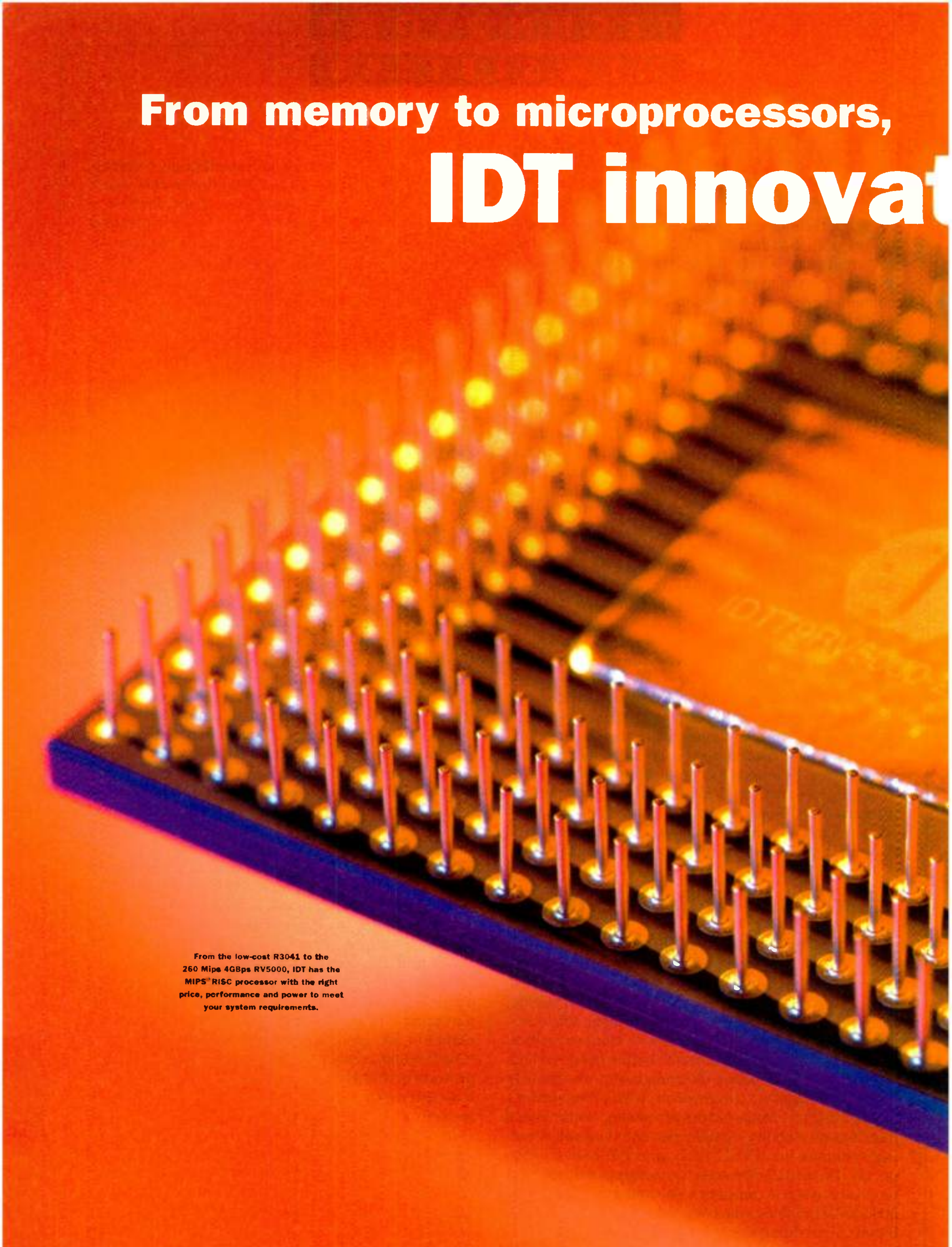
...While Sinking Its Teeth Into Issues Involving The Set-Top Box

The set-top box, discussed in presentations in Session 18, provides the gateway for many types of audio, video and Internet capabilities on the home receiver. Among the presentations, which span a wide range of issues, are performance benchmarking, a 1394 digital interface to link the box and the PC, a receiver decoder card for the PC, Internet support for digitally-encoded music, streaming video, and desktop video conferencing.

Other communications-related papers can be found in Session 2, which covers digital connectivity for wireless, ATM, and Ethernet network issues. Session 5 deals with Satellite and Terrestrial delivery, including an overview of the local multipoint communication system (LMCS) being set up in Canada, and a look at both transmission systems and receiver design for satellite digital broadcasting.

Speech recognition and speech-based control are the focus of Sessions 6 and 12. Session 6 examines speech and other intelligent user interfaces to handle functions like browsing the web, performing web queries, performing call management, and creating voice memos. Session 12 delves into portable user interfaces for home systems and digital cameras, as well as graphical user interfaces for automotive navigation and digital media computer systems.

Containing a montage of topics, the special poster session will have 17 parallel presentations, some with actual demonstrations. Topics include the design of a new push-type content delivery system, the development of a PC card receiver for FM subcarrier data broadcasting, a long cable PHY for IEEE 1394, a new protocol architecture to move ATM data over 1394, a low-power chip that transmits audio and video data using infrared, a new low-bit-rate speech-coding algorithm that will be used in the new MPEG-4 standard, and a 3D computer graphics system for digital TV applications. For information on attending the conference, contact the IEEE International Conference on Consumer Electronics, 67 Raspberry Patch Dr., Rochester, N.Y. 14612-2868; Diane Williams, (716) 392-3862; fax (716) 392-4397; *www.icce.org.* DB



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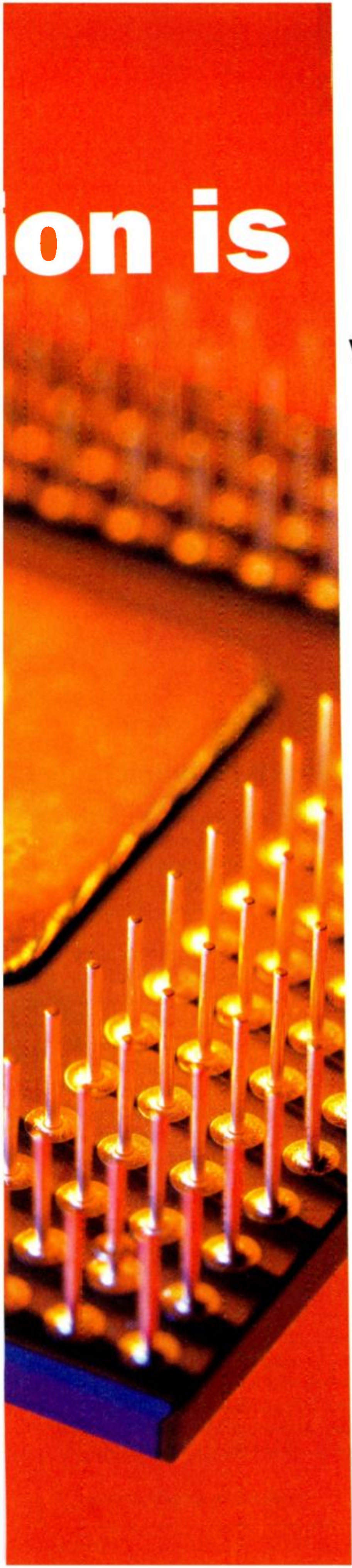

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Universal ADSL Working Group Activity Expanding

The Universal Asynchronous Digital Subscriber Line (ADSL) Working Group, a consortium of industry leaders working to accelerate the adoption and availability of high-speed communications, has accelerated its technical efforts and expanded its membership. The goal of the Universal ADSL Working Group (UAWG) is to propose a simplified version of ADSL based on open, interoperable standards that will provide consumers with high-speed communications over existing copper phone lines at up to 25 times the speed of current analog modems.

The new Universal ADSL standard being proposed by the UAWG is a slower-speed, consumer-oriented adaptation of traditional ADSL devices. It doesn't require the use of a"splitter" to segregate voice and data traffic at the customer's location. This will allow rapid acceptance by eliminating the costs associated with installing additional equipment by carriers.

The Universal ADSL Working Group consists of Compaq, Intel, Microsoft, and leaders in the networking and telecommunications industries, including 3Com, Alcatel, Cisco, Ameritech, Bell Atlantic, BellSouth, GTE, Ericsson Telecom AB, Lucent Technologies, MCI, Nortel, PairGain, Paradyne, Rockwell Semiconductor Systems, Siemens, Sprint, Texas Instruments, Tut Systems Inc., US West, and Westell Technologies, among others. The goal of the Universal ADSL specification work is to contribute an interoperable extension of the ANSI standard T1.413 ADSL. The proposal will be submitted through the ITU standardization process to gain global acceptance and leverage current deployment of T1.413-based equipment by telecommunications carriers around the world. More information on the UAWG may be obtained at *www.uawg.com*. LG

Intelligent Room Responds To Verbal Commands

Scientists at M.I.T. are bringing the idea of an intelligent room toward reality. At a press event in conjunction with the Council on Competitiveness National Innovation Summit, graduate student Michael Coen demonstrated an intelligent room capable of responding to verbal commands.

Coen presented a paper on this technology for the Spring Symposium on Intelligent Environments of the American Association of Artificial Intelligence. Coen is developing the room for his doctorate.

One intelligent demo room, which simulates a command center for disaster relief, is able to respond to a user's verbal request for a layout of the Virgin Islands by projecting a map on the wall. The intelligent room incorporates a variety of artificial-intelligence technologies such as speech-recognition programs and machine vision. These programs, in turn, receive raw data to determine, for example, the location of the user through a variety of cameras and other embedded devices in the ceiling and walls.

The Intelligent Room is controlled by a modular system of software agents. These 30 distinct, interlinked software agents runs on ten networked workstations. The agents primary task is to link the room's tracking speech recognition and video systems with information retrieval systems.

The researchers are developing an advanced version of the software that coordinates the room. One of the more developed components of the room is the speech-recognition technology. It expands the kind of capabilities available in commercially available speech-recognition software packages. The new software will be used in an Advanced Research Agency (ARPA) project called the Command Post of the Future.

For more information, contact Elizabeth A. Thomson, at the MIT News Office (617) 258-5402; *thomson@mit.edu*. JC

Protonic Nonvolatile Memory Irons Out Stubborn Problems

Nonvolatile memory, although a mature and rather robust technology, does have its drawbacks. Present nonvolatile memory technologies, for example, often require a high programming voltage and long write times, and are plagued by the obstacle of limited write cycles.

Attempting to come up with a nonvolatile memory technology that isn't so problematic, Sandia National Laboratory, Albuquerque, N.M., is involved in an extensive research and development project focused on devising an entirely new class of technology. The approach the laboratory came up with—protonic nonvolatile memory—is able to save computer data in the event of a power failure by making protons in the primary storage mechanism of information. This memory technology is low power, operates at high speed, and has a demonstrated reliability of just over 1 million cycles.

Researchers have applied this technology to what's being termed a nonvolatile field-effect transistor. During the device's operation, protons sandwiched between silicon layers in the memory-retentive protonic chip maintain the memory state when power is removed. The device is inexpensive, easy to build, and compatible with a majority of existing manufacturing processes. Researchers, therefore, expect that it will significantly impact the entire multi-billion dollar nonvolatile memory industry. For further information, contact the Media Relations department at Sandia National Laboratory at (505) 844-8066, or check out the Lab's web site at *www.sandia.gov*. CA

Edited by Roger Engelke

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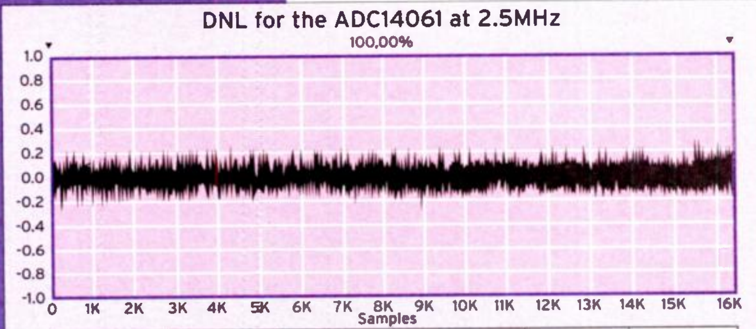

Part Number	Resolution	Conversion Rate	Power Consumption	DNL (LSB, typ)	Packages
ADC14061	14-bits	2.5MSPS	390mW	±0.30	52-TQFP
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ADC12081	12-bits	5.0MSPS	105mW	±0.35	32-TQFP
ADC12181	12-bits	10.0MSPS	235mW	±0.40	32-TQFP

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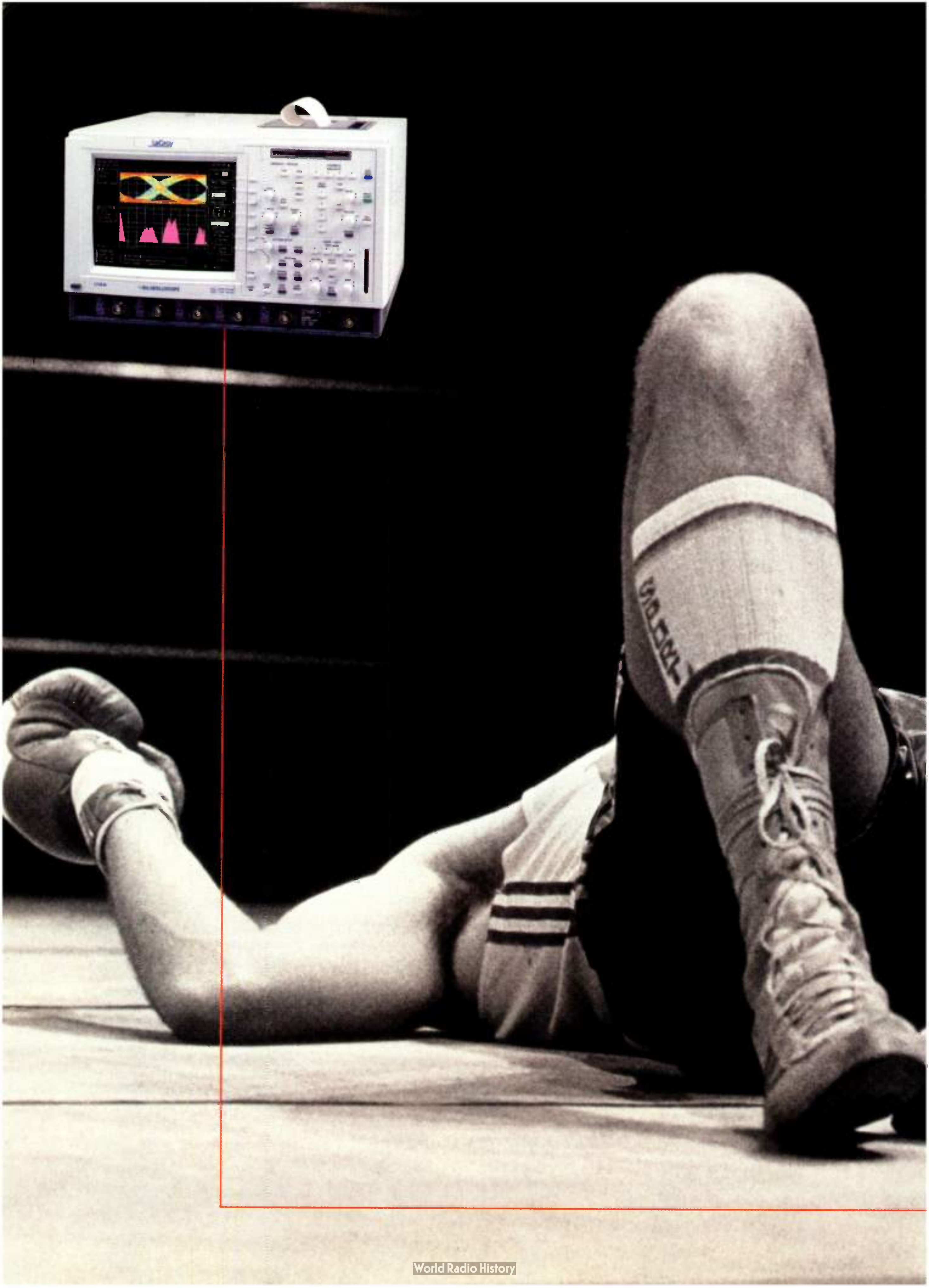

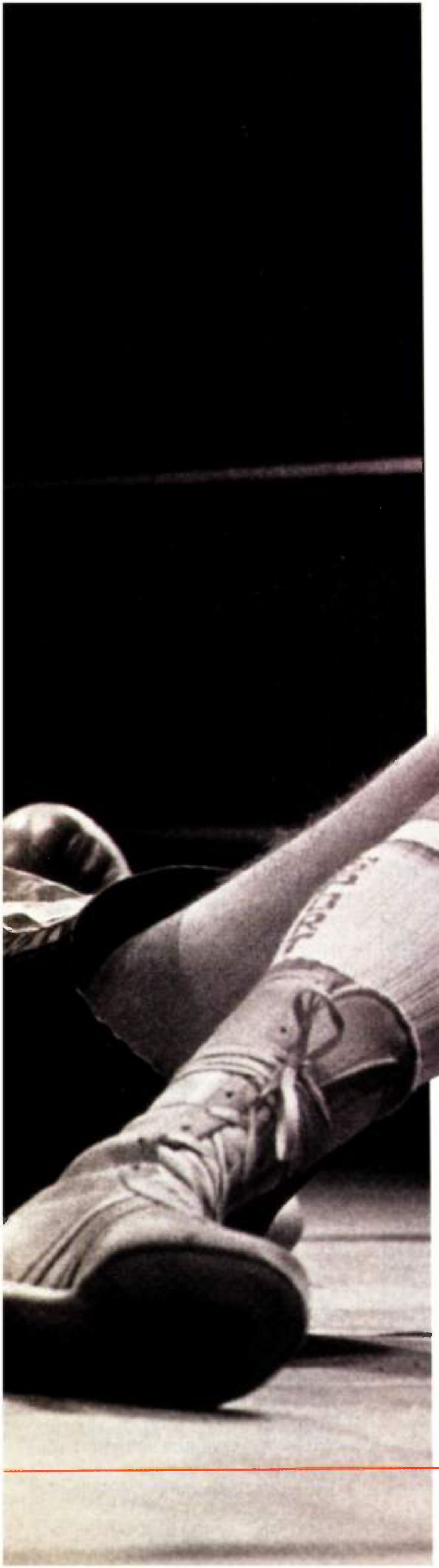

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READER SERVICE 148

Combined Laser And Magnetic Techniques Promise Storage Densities Of 40 Gbits/in.²

Storage densities in pure magnetic-based disk storage systems are starting to hit an upper limit of about 10 Gbits/in.² However, by combining an advanced laser light delivery system with a novel head design and a micromachined electromechanical system for fine servo control, researchers at Quinta Corp., San Jose, Calif., a division of Seagate Inc., expect to achieve storage densities of 40 Gbits/in.² and beyond. Dubbed the Optically Assisted Winchester (OAW) technology, the scheme delivers a laser light beam to the read/write head. That beam controls the fine servo, which positions the head very accurately.

Most researchers believe the super-paramagnetic limit—the point at which traditional hard-disk media can no longer hold a stable domain—to be between 20 and 40 Gbits/in.² However, Quinta researchers expect the OAW technology to exceed that limit by early in the next decade. Not only can the technology be applied to a single platter, it also can be used in multiplatter drives and with removable-media drives.

The four key systems in the OAW approach include the advanced light delivery system, a unique head design, a novel servo system, and a nonmetallic recording media substrate (plastic). The light delivery system is based on an optical switch module that generates light pulses and switches their destination between the actuator arms in as little as 1 ms. A network of fiber-optic cables no thicker than human hairs spans the drive's actuator arms and carries light pulses to the read/write heads.

The design of the read/write head itself combines an advanced magnetic head technology for vertical recording with micro-optic lenses that focus the fiber-optic's light pulses onto the media surface. Less then 350 µm in diameter, the lenses are several times smaller than anything yet created, and can focus the laser's light sharply on the media surface, while also providing a large margin of error to account for potential flying-height variations *(see the figure)*.

The laser light exiting from the end of the hair-like fibers strikes micromachined mirrors no larger than the head of a pin. The reflected light goes through the objective lens and is focused on the magnetic surface of the platter.

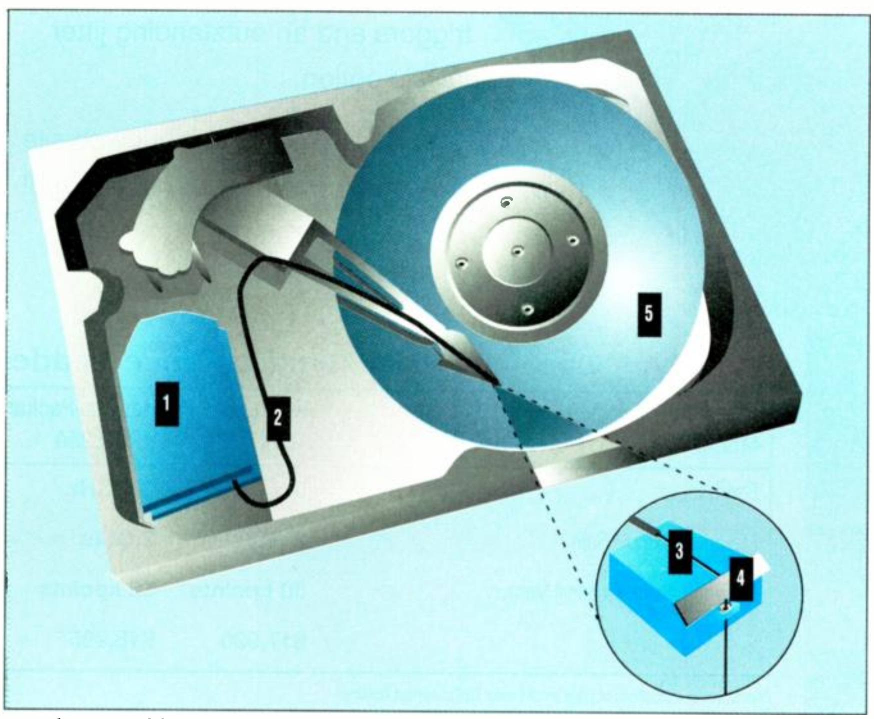
After the read/write heads are positioned using standard servo positioning, small electrical currents are routed along the actuator arm in order to cause a slight change in the reflection angle of the mirror. This causes the beam position on the surface to change. Consequently, this permits very fine adjustments to be made in the head position, allowing the system to employ much tighter track spacings while achieving higher densities. Researchers estimate that the system can achieve over 100,000 tracks per inch.

Although the media used in OAW systems is constructed in a manner similar to that of traditional Winchester platters, the substrate can be made from plastic, which is lighter and less expensive than aluminum. Plastic also permits some preformatting of the media so that the servo track could be included as well.

The magnetic layer on the OAW discs consists of amorphous, rare-earth transition metals that can support theoretical area densities much higher than those possible with conventional Winchester storage media. The amorphous nature of the magnetic layers also avoids the super-paramagnetic limit of conventional Winchester media and allows the use of vertical recording techniques rather than conventional longitudinal recording.

The vertical recording technology helps reduce the size of the data regions on the platter, thus further improving storage capacity. To write the data, the optical pulse from the laser is sent through the fiber and positioned by the mirror onto the platter's surface. The beam heats the material, and then the planar coil on the read/write head is pulsed to set the polarity of the magnetic domain in the platter. To read data, the laser is switched to a lower power intensity and passes polarized light through the magnetized spot. The Kerr rotation of the magnetic domain is then detected by analyzing the reflected beam, very much like how magnetic optical disks are read.

The cost of embedding the technol-



A combination of five technology enhancements will help future disk drives to pack data at densities of up to 40 Gbits/in.². An optical switching module (1) routes the laser light, while hair-thin optical fibers (2) route the light to the new read/write heads (3), which include both a microlens and a unique electrically controlled mirror (4). The laser beam is then focused through the lens so that it will hit the platter (5) in a very precise location.

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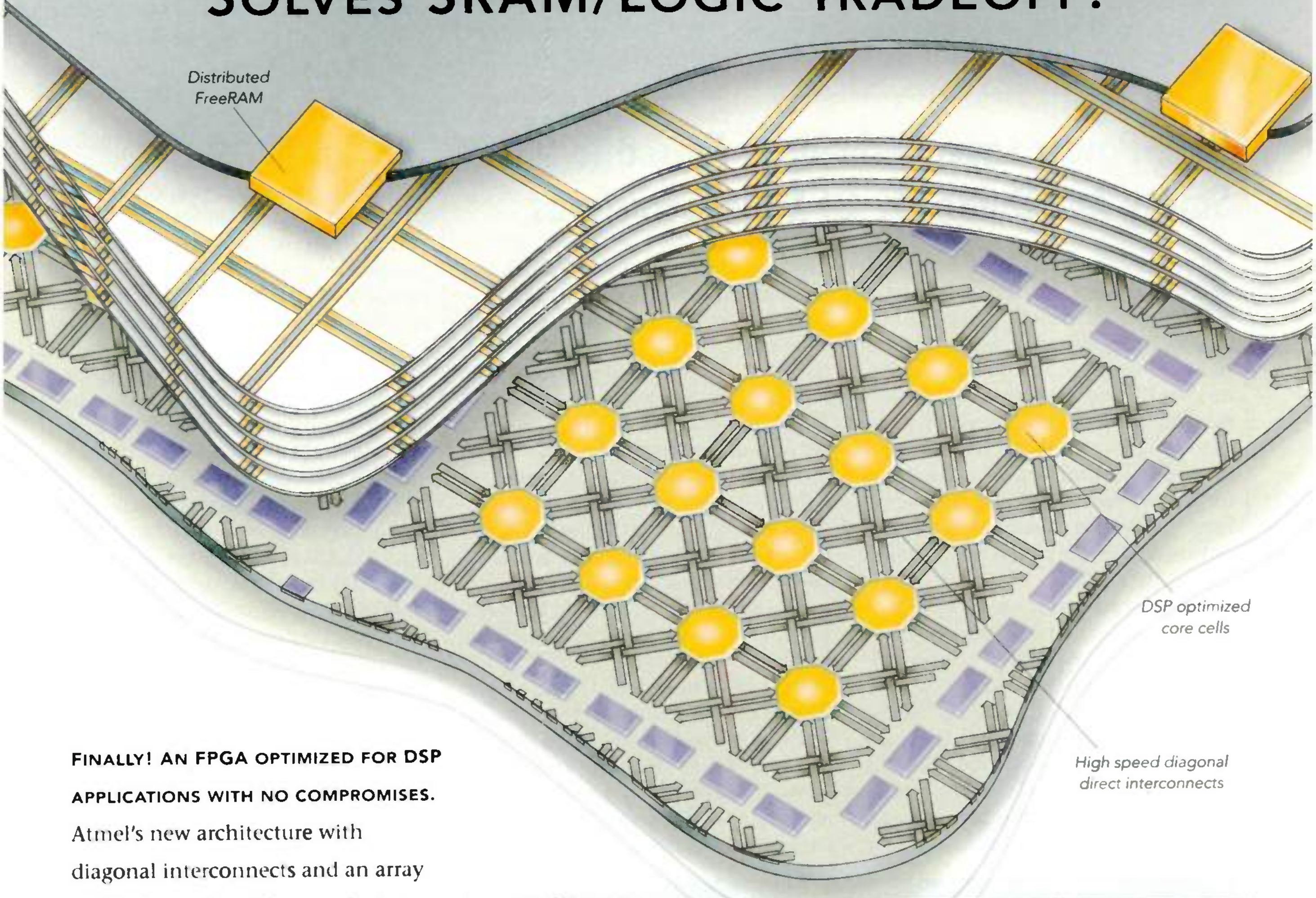

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AT40K10	10K–20K	576	4096	192	84 PLCC, 100 VQFP, 144 TQFP, 160 PQFP, 208 PQFP, 225 BGA, 240 PQFP
AT40K20	20K–30K	1024	8192	256	84 PLCC, 144 TQFP, 160 PQFP, 208 PQFP, 225 BGA, 240 PQFP, 304 PQFP, 352 BGA
AT40K30	30K–40K	1600	12,800	320	84 PLCC, 144 TQFP, 160 PQFP, 208 PQFP, 225 BGA, 240 PQFP, 304 PQFP, 352 BGA, 432 BGA
AT40K40	40K–50K	2304	18,432	384	84 PLCC, 144 TQFP, 208 PQFP, 225 BGA, 240 PQFP, 304 PQFP, 352 BGA, 432 BGA, 475 PGA

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ogy in the disk drive is estimated to be about the same as for the much higher-precision electromechanical positioning systems, so drive prices shouldn't be forced to unaffordable levels. Furthermore, since the heads have a flying height several times that of standard media—15 µin.—and have a good depth of focus (about 30 µm), there are fewer causes of data errors and drive malfunctions and the forthcoming drives should offer at least as good MTBF ratings.

Expectations are that drives based on the technology may come out of R&D by late this year with production some time next year. Contact Quinta at (408) 952-5000, Internet: www.quinta.com.

Dave Bursky

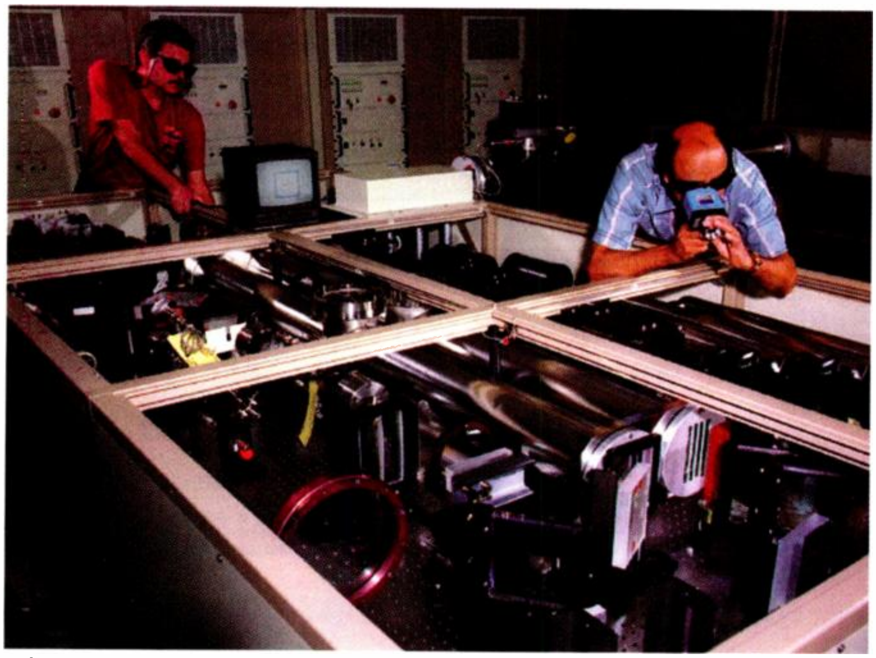
High-Power Laser Technology Poised To Boost Safety And Durability Of Metal Structures

A new type of laser, with a peak pulse power roughly equivalent to that of a nuclear power plant, promises a significant impact on a number of industries, including aviation, medical, and the military. The neodymium-doped glass laser, originally developed by researchers at the Lawrence Livermore National Laboratory, Livermore, Calif., for national defense applications, features an average power of 600 W and a peak power of 3,000,000,000 W.

The new laser also boasts a fire rate of 10 pulses per second. By comparison, the best commercial laser available today only fires one pulse every two seconds *(see the figure)*. Because of this extraordinary performance, researchers believe the laser and adaptations of its original design will lead to new manufacturing techniques. These, in turn, could have effects such as improving the safety of aircraft and the durability of hip-joint implants.

One of the initial areas targeted by this technology is peening, or surface treatment, of metals. To assist in this effort, Livermore researchers linked with Metal Improvement Co., Paramus, N.J. As part of the Cooperative Research and Development Agreement (CRADA) between the two organizations, work to adapt the laser technology will begin immediately and is expected to last two years.

The conventional method for peening, known as shot peening, works by bombarding a material with miniature metal balls, the size of a grain of salt. This induces compressive stress that effectively prevents metal fatigue and reduces corrosion. While the idea of laser peening was originally introduced as an alternative to this conventional method back in the mid-1980's, the high cost and slow response of available lasers prevented their adoption in this application.



Technicians align the new 600-W (average power) neodymium-doped glass laser at Lawrence Livermore National Laboratory. The device outputs a peak pulse power of 3,000,000,000 W.

Laser peening is not expected to replace conventional shot peening completely. Instead, the technology will be be used in areas where more intense compressive stress is needed. Testing has shown that while conventional shot peening can only reach a depth of about 1/100 of an inch to instill compressive strength, the laser-peening method extends roughly four times deeper. The result is that metal structures can be made stronger and the end product safer.

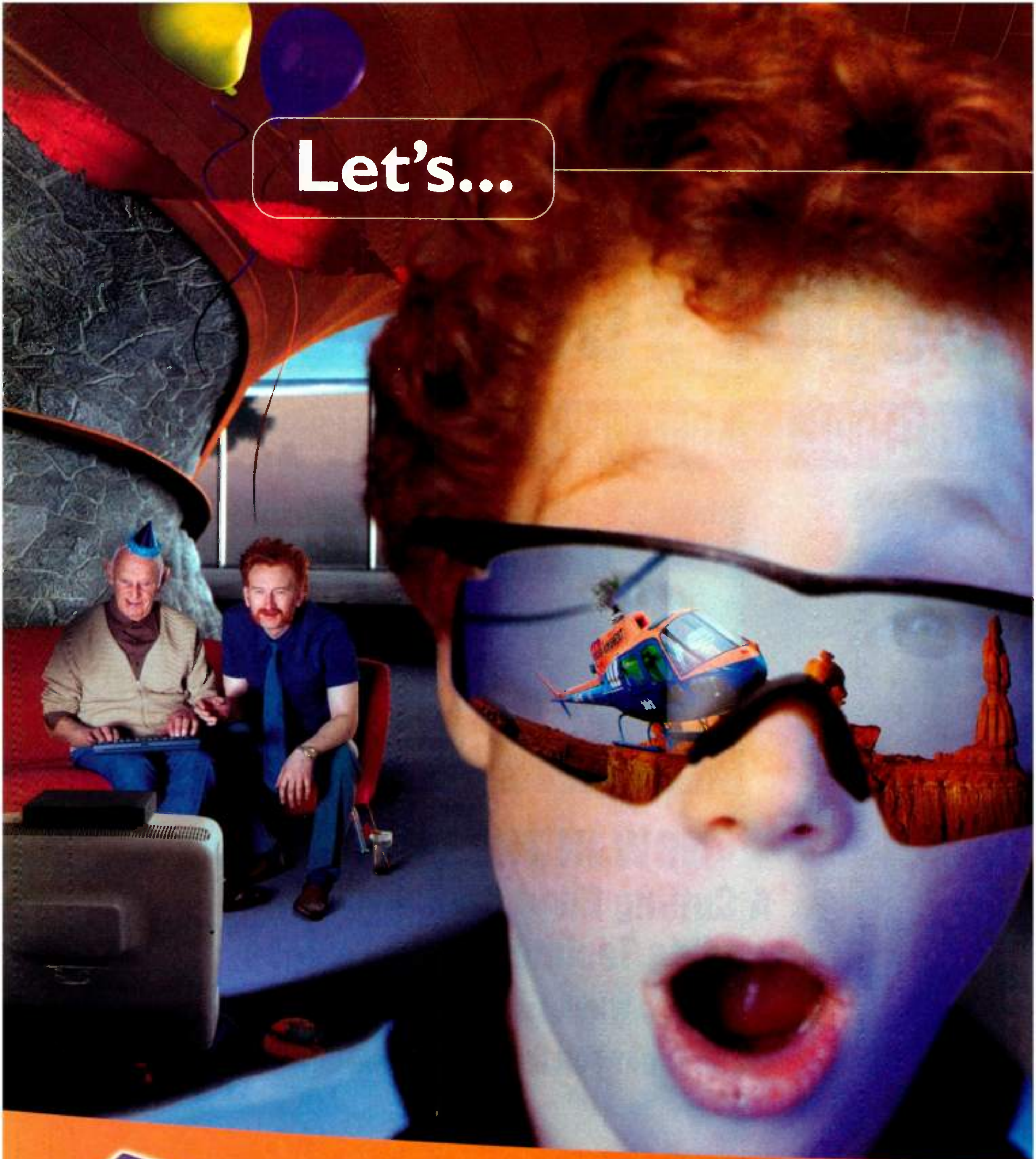
The neodymium laser also has significant implications for life-cycle costs, reliability, and damage tolerance. In the aviation industry, for example, laser peening of jet engine components like turbine blades, disks, rotors, and shafts could eliminate stress cracking. In particular, it could increase the resistance of turbine blades to strikes from foreign objects, such as birds, ice, or stones. Damage from these strikes can easily propagate through the entire blade, leading to failure, and even destruction of the aircraft's engine.

Researchers are also investigating the use of this technology for the elimination of high-cycle blade fatigue⇓a major propulsion concern for the U.S. Air Force. Recent testing shows that laser peening increases metal fatigue strength 10% to 40%, allowing engines to operate at higher stress loads without metal fatigue. Additionally, laser-peened engine blades have an average lifespan three-to-five times longer than blades peened using conventional techniques. At a cost of roughly $40,000 a blade, the savings are obvious.

Other areas where the technology might prove useful include oil-drilling tools, marine engines and shafts, rocket engine parts, and in the chemical and power-generation industries. Commercial products manufactured using laser peening are expected to be roughly two-to-four years away from introduction.

Contact Lawrence Livermore's Public Affairs Office at (925) 422-1100.

Cheryl Ajluni



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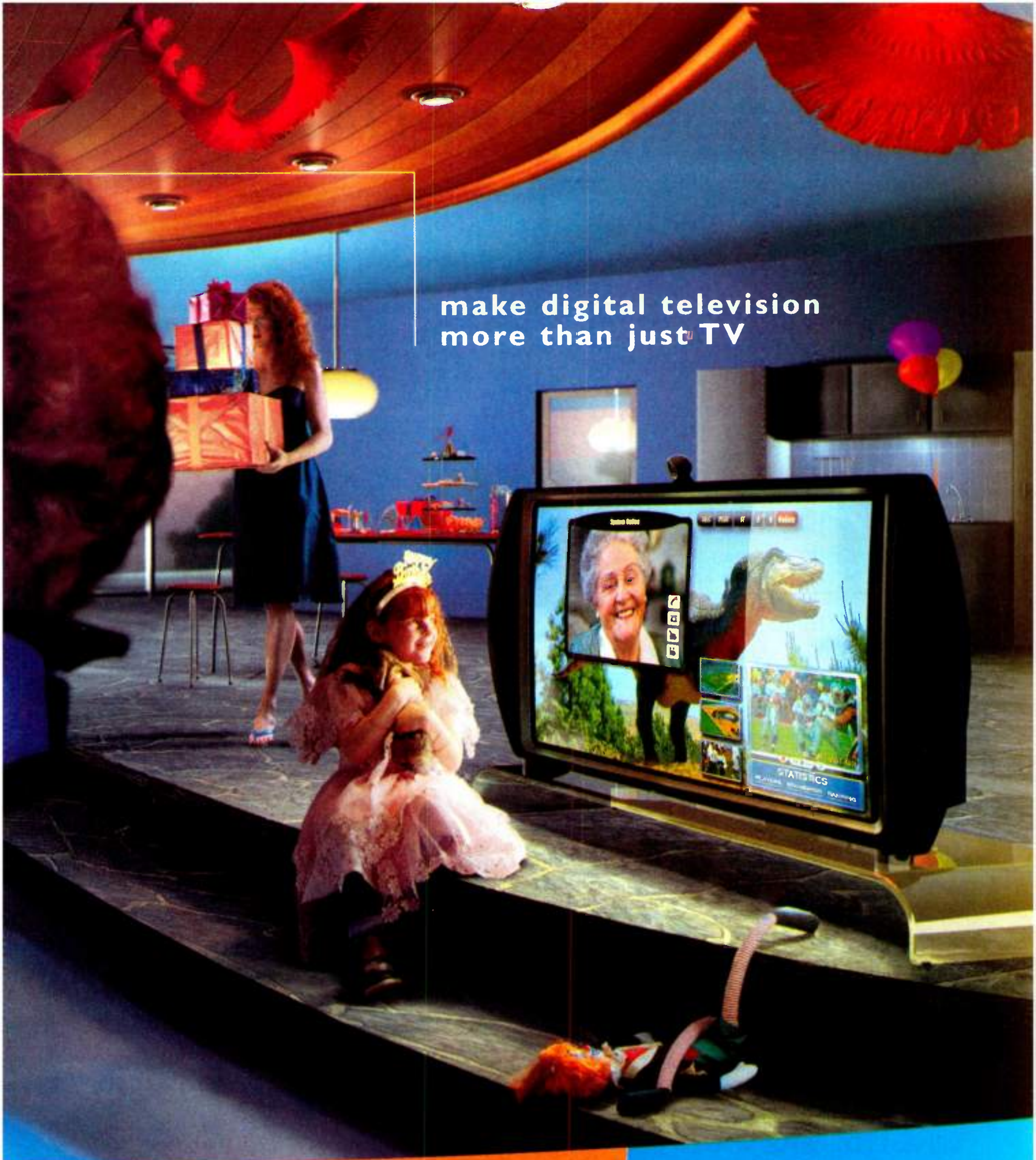
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■ **Previewing the latest developments at the 1998 Custom Integrated Circuits Conference**

Systems-On-A-Chip And Advanced IC Processes Take Center Stage At The 1998 CICC

The 20th annual Custom Integrated Circuits Conference (CICC), to be held May 11-14 at the Santa Clara Westin Hotel and the Santa Clara Convention Center, Calif., provides a multifaceted demonstration of the latest design techniques, circuit architectures, advanced processing, design tools, and test techniques for custom ICs. As the leading forum for IC development, this year's CICC features a rich program that includes 24 technical sessions, four educational sessions, and three evening panel sessions covering a wide variety of topics *(see the table)*. Several exhibitor marketing sessions, in addition to a general exhibition that runs concurrently with the technical paper sessions, round out the CICC's program.

Our conference preview focuses on four main technology areas: digital, analog, communications, and EDA technologies. Digital advances are highlighted by developments in system chips, programmable-logic devices, and deep-submicron processes. Analog innovations include developments in data converters, op amps, and CMOS characterization for better analog circuits. Communications growth is seen by a renewed emphasis on device theory, oscillator design, and monolithic RF-circuit analysis. And, EDA developments in simulation techniques and innovative modeling methods wrap up our conference projection.

The Keynote address, "To the Rescue of Moore's Law," will be delivered on Tuesday morning by Aart J. de Geus, president and CEO of Synopsys Inc. It examines "how design teams will traverse the increasingly complex path from concept to finished chip," in the modern design environment.

The General Chairman for this year's CICC is Robert Cordell, the Conference Chairman is Rakesh Kumar, and the Technical Program Chairman is Brian Fitzgerald.

For conference registration, contact CICC, 101 Lakeforest Blvd., Ste. 270, Gaithersburg, MD 20877; (301) 527-0902 (ph); (301) 527-0994 (fax); *E-mail: cicc@his.com.*

1998 CUSTOM INTEGRATED CIRCUITS CONFERENCE (CICC)

Monday May 11 8:00 a.m. to 5:00 p.m. (Educational sessions)	Session 1 Current issues in IC Design	Session 2 High-level design techniques	Session 3 Advanced integration issues	Session 4 Wireless IC Design
Tuesday May 12 8:00 to 9:30 a.m.	**Session 1: Welcome/opening remarks and keynote address** "To the rescue of Moore's Law," by Aart J. de Geus, president and CEO, Synopsys			
10:00a.m. to 12:00p.m. (Technical sessions)	**Session 2** Digital circuits for communications	**Session 3** Analog techniques	**Session 4** Design and analysis of oscillators	
1:00 to 2:00p.m. (Exhibitors' preview sessions)	**Session 1** Cascade Design Automation, EPIC, Mentor Graphics, Tanner EDA	**Session 2** Frequency Technology, Simplex Solutions	**Session 2—continued** Ultima Interconnect Technology, BTA Technology	**Session 3** Accurel Systems International, CADABRA, NWL Ltd., Silicon Access
2:00 to 5:00p.m. (Technical sessions)	**Session 5** Wireless circuit design techniques/ technology	**Session 6** System-on-a-chip integration	**Session 7** Low-power approaches to digital signal processing	**Session 8** IC technologies trends and future
Wednesday May 13 8:30a.m. to 12:00p.m. (Technical sessions)	**Session 9** Audio and video signal processing	**Session 10** Modeling for high-frequency design	**Session 11** Data converters	**Session 12** Innovations in programmable-logic architectures
2:00 to 5:00p.m. (Technical sessions)	**Session 13** IP creation and management	**Session 14** Deep-submicron library design	**Session 15** Wireline communications	**Session 16** Amplifiers and sample/hold circuits
8:00 to 11:00p.m. (Evening panel sessions)	**Session 17** Analog design challenges in deep-submicron process technology	**Session 18** IP—intellectual property or intense pain?	**Session 19** Electrical engineering education: Is it up to today's job challenge?	
Thursday May 14 8:30a.m. to 12:00p.m. (Technical sessions)	**Session 20** Wireless transceivers and systems	**Session 21** Custom circuits and non-volatile memories	**Session 22** Advanced simulation techniques	**Session 23** Analog modeling and CAD
1:30 to 5:00p.m. (Technical sessions)	**Session 24** Low-power/high-performance circuits and techniques	**Session 25** Reliability and test in deep-submicron design	**Session 26** Phase-locked-loop design and applications	**Session 27** DSM issues, tools, and methodologies

Circuit Density And Smaller Geometries Drive CICC's Digital Sessions

System Chips, Programmable Logic Advances, And Deep-Submicron Processes Continue To Challenge Design Engineers. **DAVE BURSKY**

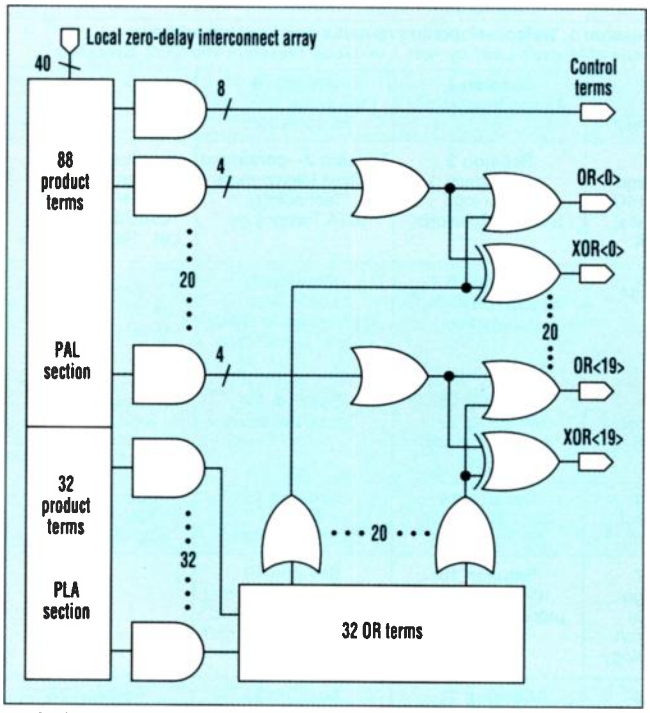
With the phrase "system-on-a-chip" rolling off the lips of almost every ASIC supplier, designers trying to implement these chips struggle with many issues, from defining and integrating the blocks of intellectual property (IP) to working with deep-submicron processes. The digital technology papers at this year's Custom IC Conference provide designers with a montage of new technology approaches, examples of system-chip design, and early looks at evolving technologies for megagate system integration.

Examining the advances in system-on-a-chip design, Sessions 6, 13, and 27 focus on function integration, creation of IP (reusable building blocks), and deep-submicron design and methodology issues, respectively. Presentations in Session 8 highlight various trends in advanced processing technologies for high-density ASICs. Session 12 and 21 cover developments in programmable logic architectures and custom circuit design, and several ferro-electric memory implementations, respectively.

Many approaches for system-on-chip integration try to leverage the use of an on-chip bus to interconnect the various major blocks assembled on the chip. In an invited presentation in Session 6, Sonics Inc., Los Altos, Calif., details a new on-chip interconnect that employs an active bus interface between the functional blocks to form an on-chip communications subsystem (the silicon backplane). By using a consistent interface to the blocks of IP, the Sonic module interface (MI), all the functional blocks can remain independent of the silicon, allowing easier mix-and-match approach to silicon design.

The backplane implements a fully-distributed protocol that unifies all of the communication traffic between the various IP blocks on the chip. The protocol is used as part of the interface modules that tie each IP block to the bus. There are four basic module types: snooping, target, initiator, and backplane bridge. In the interface module, clock signals are decoupled, data widths are adjusted, out-of-band signals are routed, addresses are matched, and IP core-device-control and status registers are implemented.

In another session paper, jointly developed by CSELT, Torino, Italy, and SGS Thomson, Agrate Brianza, Italy, designers examine the implementation of a virtual chip set—the creation of a parametric IP library for system-on-a-chip design. Basically, the designers have created a parametric VHDL IP library based on synthesizable system-level modules, where any element can be customized, connected, and merged with the others. The library consists of modules, each written in RT-level VHDL, and each implementing a popular function in different application areas such as data communications or telecom. The modules can then be mapped during device simulation into any technology.



1. The logic array block in the CR960, developed by Philips, is subdivided into two sections: The first is a PAL block containing 88 40-input product terms, eight of which are used to form control p-terms. The second section contains a PLA that provides 32 p-terms used to drive an array of 20 32-input OR terms.

The remaining papers in Session 6 include a methodology for synthesizing interface controllers directly from timing diagram specifications, by researchers at Labratoire LASSO, University of Montreal, Quebec, Canada, and an analysis of pin versus gate proportions in heterogeneous systems, jointly done by the Microelectronics Research Center at the Georgia Institute of Technology, Atlanta, and LSI Logic Corp., Milpitas, Calif. Another paper looks at the building blocks needed for a single-chip, GSM baseband processor by LSI Logic, Milpitas, Calif., and Oasis Design, Austin, Texas. Finally, there's a CPLD implementation of a motion-detection algorithm for video surveillance by the University of Bradford, West Yorkshire, United Kingdom.

Several related papers in Session 13 deal with the creation and management of IP.

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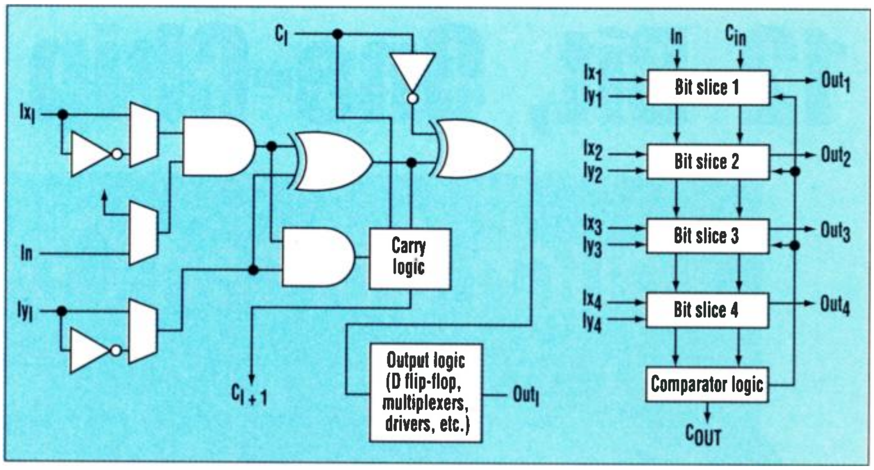
In the first paper, designers from MOSAID Technologies Inc., Ontario, Canada, examine ways to reinvent the DRAM to more-efficiently use it as a building block in embedded applications. The second presentation by Toshiba Corp., delves into the design of a DRAM module generator that allows designers to get custom DRAM organizations with minimal effort.



2. At the heart of the computationally optimized, programmable logic circuit developed at the University of Toronto, is this simple bit-slice containing a full adder composed of two XOR gates and the carry logic. Four bit slices and additional logic form a partial add, subtract, and multiply block used in implementing the data path operations.

CMOS Advances

Investigating some of the deep-submicron design trends, the first invited paper in Session 8 provides an overview by researchers from Toshiba Corp., Kawasaki, Japan, of expected CMOS advances up through the year 2010. The other invited presentation from Sematech and Motorola Inc., both in Austin, Texas, looks at the impact the high resolution required by lithography systems will have on IC mask design.

In its view of the future of CMOS, Toshiba digs into the technical and economic challenges posed with circuits based on 0.1- and sub 0.1-µm design rules. The speaker notes that there are many concerns and even some pessimistic observations regarding the realization of 16- and 64-Gbit DRAMs with 0.1-µm and smaller design rules.

Some of the concerns include the skyrocketing production costs incurred with additional process steps and increased price of the equipment, and a saturation of the operating speed due to signal and clock propagation delays in the long and dense interconnects. Other issues are the degradation of yield and reliability due to the large number of transistors and other elements on a chip, and the increase in power consumption and heat generation, also due to the large number of devices on the chip.

Additionally, as gate dimensions shrink, the gate leakage current due to short-channel effects becomes an ever-increasing issue. Then again, there's the channel resistance and the drain and source resistances, which tend to increase to suppress the short-channel effects. Therefore, ways must be found to reduce resistances while suppressing the short-channel effects, or the downsizing of the MOSFETs will be almost meaningless.

When experimenting with transistors that have gate lengths of 0.04 µm, gate-oxide issues also limit performance because many researchers see a 3-nm "limit" on thickness due to direct-tunneling leakage. However, Toshiba researchers have halved the thickness to just 1.5 nm, and still achieve good transistor characteristics, thus further downsizing the transistor structures. In practice, they estimate that the limit for gate lengths will be down at about 0.025 µm, while propagation delays for a transistor may drop by two orders of magnitude to about 0.1 ps. Practical designs might only see a propagation delay of about 1 ps/gate.

The second invited presentation deals with the mask-creation issues that crop up in producing the extremely fine-featured devices in the next century. More complex pattern-handling algorithms must be put in place to handle the several-orders-of-magnitude increase needed to create the masks. Additionally, for 100-nm and smaller features, new post-optical lithography techniques will be needed, and the presently undeveloped technologies will require radical changes in data handling.

Putting some of the research to work, designers at the Device Development Center of Hitachi Ltd., Tokyo, Japan, have developed a 0.2-µm, seven-layer, metal CMOS process. It includes some new interconnect scaling rules that take advantage of optional wide lines and line repeaters. The resulting circuits deliver a 1.5-times speed improvement and a fourfold increase in integration without any RC delay increase over its 0.3-µm process.

Researchers from Lucent Technologies' Bell Laboratories, Orlando, Fla., detail a merged 2.5- and 3.3.-V, 0.25-µm CMOS process that employs four or five levels of metal. Targeted at ASIC design, the process integrates both 2.5- and 3.3-V transistor structures on the same chip, with the addition of just one extra ion-implant mask level. Such an approach allows the cointegration of functional blocks that operate at either supply level, rather than two separate chips that each operate at either 2.5 or 3.3 V.

Connections With Lasers

Laser technology has long been used in memory and other logic circuits to open metal links, disconnect blocks of circuits, and enable other blocks to repair bad rows and columns in storage devices, or configure some gate arrays. However lasers can also be used to make connections, as pointed out by researchers from the Materials and Nuclear Engineering Department of the University of Maryland at College Park. They describe an additive technique using IR lasers that allows them to form solid metallic connections between two standard levels of metalization, with resistances of less than 0.8 Ω per connection.

The laser-connection technique banks on two intrinsic factors: When heated, metal expands and becomes

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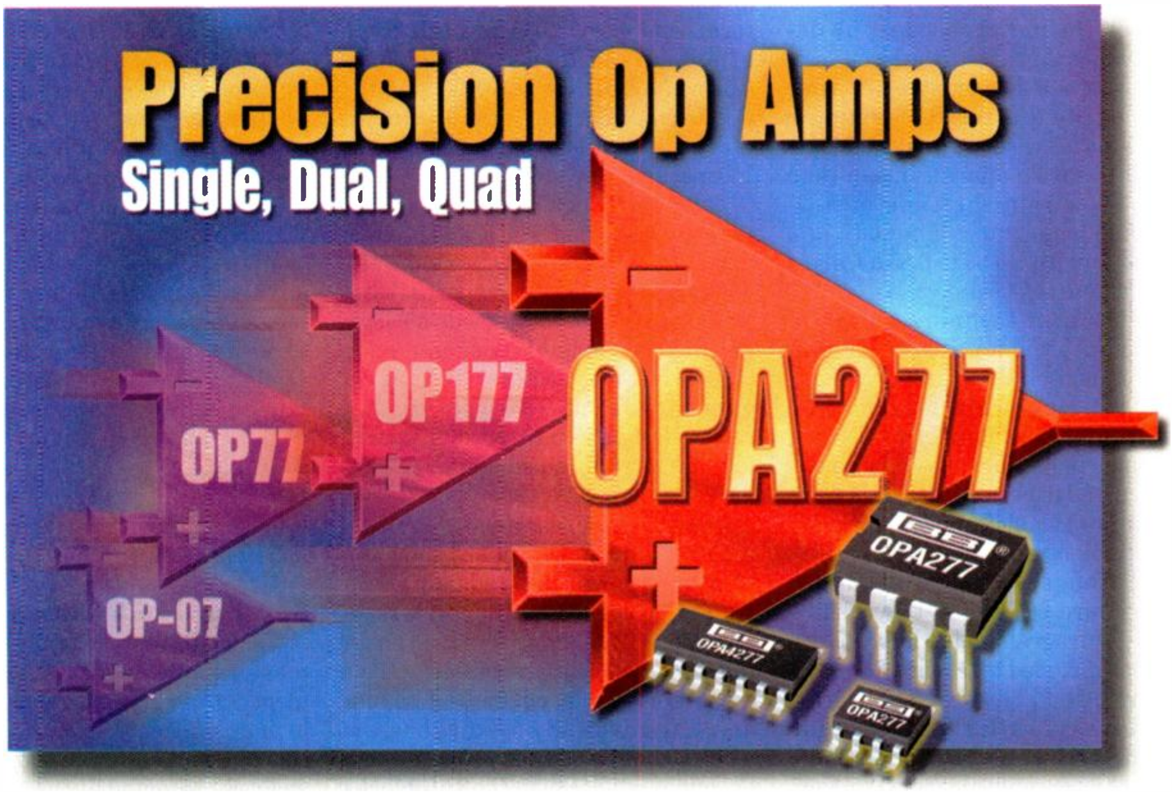

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Such a laser technique could be used for last-minute circuit modifications on full ASIC designs, or on programmable logic circuits, giving designers more options for modifying the connections. More options also will be discussed in Session 12, which deals with innovations in programmable logic architectures.

For example, a new SRAM-based architecture will be put to work in a complex, programmable logic device that was unveiled by Philips Semiconductors, Albuquerque, N.M. The architecture of the CR960 is based on 12 identical logic cores (called FastModules), that communicate with each other using an interconnect matrix, the global zero-delay interconnect array (ZIA). A single-poly, five-layer metal CMOS process using 0.35-μm drawn channel lengths is used to fabricate the circuit.

In each FastModule are four logic array blocks (LABs). Each LAB contains 20 macrocells, 12 of which are "buried" (have no external I/O). Communication between the four LABs is accomplished with a local ZIA routing pool. Additional circuitry, such as shift registers, scan registers, memory elements, and associated controllers are also on the chip and used for test and configuration. Therefore, one FastModule can feature considerable functionality, and offer a combinatorial delay of less than 5.8 ns and a clock to output delay of 4.8 ns, both under worst-case conditions.

Each LAB has two sections: a programmable array logic (PAL) block that contains 88 40-input product terms, and another programmable logic array (PLA) block that contains 32 p-terms that drive an array of 20 32-input OR-terms *(Fig. 1)*. Eight of the 40-input product terms are used to form control p-terms. Outputs from both the PAL and PLA blocks are arranged into 20 identical, ordered groups of signals, each carrying four p-terms and one OR-term. Each group of signals produces two outputs (formed by OR-ing and XOR-ing the OR term with the sum of four p-terms). These two outputs serve as I/O macrocell inputs.

Over 8.5 million transistors are integrated to form the CR960. Most of those transistors are buried deep within the various logic paths. That makes the standard methods for logic testing unwieldy because innumerable sets of test vectors would be required to evaluate every device. As a result, designers incorporated special test circuitry that provides 100% device coverage.

First the chip was divided into two major sections, controllers and core. Controllers were tested using full-scan technology, while the core was divided into 12 sub-blocks that all share the same test controls, but have their own internal scan chains and boundary-scan chains. By subdividing the blocks, some test-time reduction can be achieved, because the sub-blocks can be exercised in parallel.

Optimized For Computing

Appropriate for computational applications, a novel, field-programmable architecture will be detailed by the Department of Electrical and Computer Engineering at the University of Toronto, Canada. Researchers created a configurable, compute-intensive block containing a flexible data path and control circuitry.

Set up in a nibble-wide configuration, each block can perform a ripple-carry addition, subtraction, and partial multiplication *(Fig. 2)* These blocks can be connected through the on-chip interconnect to form complete adders, subtractors, and multipliers of any word width. The design developed at the university is only five-to-seven times less area efficient than a custom chip. General-purpose FPGAs are estimated to require about 22 times more area than a custom circuit to perform similar computations. However, some of the FPGA inefficiency may be due to non-optimal synthesis tools for the FPGAs.

Another application-optimized programmable circuit, this time a field-programmable, analog array will be detailed by researchers from the Department of Electrical Engineering from Texas A&M University, College Station. The array is targeted at signal processing applications. Based on simple, current-mode primitive amplifiers that allow operation at high frequencies and low voltages, the circuit was implemented in a digital CMOS process. It can be programmed to operate over two decades, from several tens of kilohertz to a few megahertz. A modular array of cells forms the chip, with each array containing three subcells: a configurable analog cell (CAC), a programming register, and programming logic. The CAC block is based on an active cascode integrator, and can be configured to form an integrator, an amplifier, or an attenuator.

Boosting FPGA Efficiency

Taking advantage of the embedded memory arrays in FPGAs to implement certain logic functions can result in more efficient use of the FPGA resources. This assertion comes from an analysis presented by the Department of Electrical and Computer Engineering at the University of British Columbia, Vancouver, Canada. When not used for storage, embedded memory arrays can extend the logic functionality by using the RAM as ROM-like look-up tables. The paper explores the effects of memory-array depth, width, and flexibility on the array's efficiency when implementing logic. The results indicated that the best efficiency occurs when the array blocks contain between 512 and 2048 bits, and have word widths that are configurable as 1, 2, 4, or 8 bits wide.

The remaining papers in the session, both by Altera Corp., San Jose, Calif., detail the architectures of the company's third generation EEPROM-based MAX9000 CPLD and the SRAM-based FLEX6000 programmable logic circuits. The 560 macrocell EPM9560A is the first member of the MAX9000 family, and is fabricated with a 0.5-μm, triple-layer metal process. The process, combined with architectural enhancements, keeps the cross-chip propagation delay to

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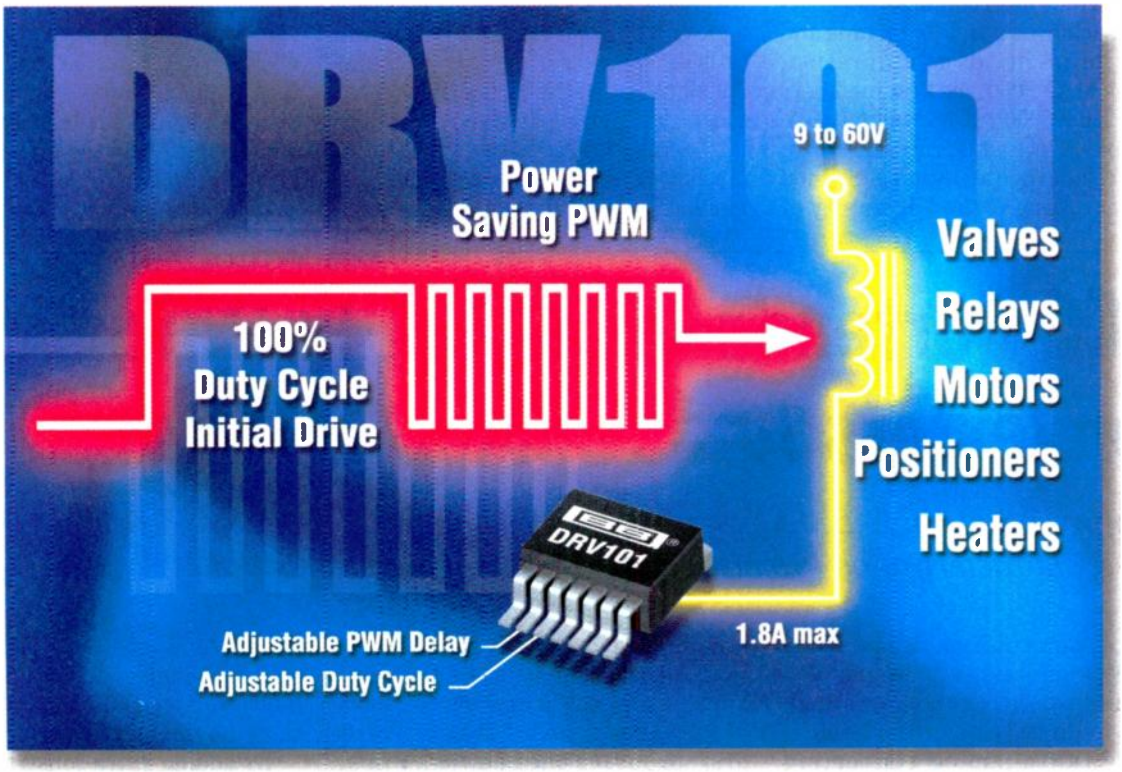

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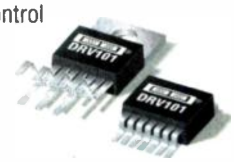

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The FLEX 6000 architecture, on the other hand, employs a register-rich, look-up-table approach, with very efficient interconnect and routing that achieves a small chip area and allows for in-circuit configuration. Like the MAX9000, the first members of the FLEX6000 will be built on a 0.5-µm, triple-level metal process.

In a related presentation in Session 13, researchers at the University of California at Los Angeles have developed an approach that "fingerprints" circuit blocks used in FPGAs. This process can provide some degree of copyright protection and allows them to quickly be identified if used in other logic circuit implementations. The approach places a secure, but transparent signature in the FPGA block. That block can then be further integrated into a full FPGA design, which actually buries the watermark still further, making it harder to find.

Many other digitally oriented papers covering nonvolatile memory technology, low-power processing, and a multitude of process and design-related issues will provide additional insight into the future of custom circuit design. In its entirety, of course, CICC covers a much broader range of technologies—mixed signal, communications, and sensor technologies to name a few—and the presentations in all those areas provide solid insights regarding the future of the industry.

CICC Portends Evolution In Data Converters And Analog Circuits

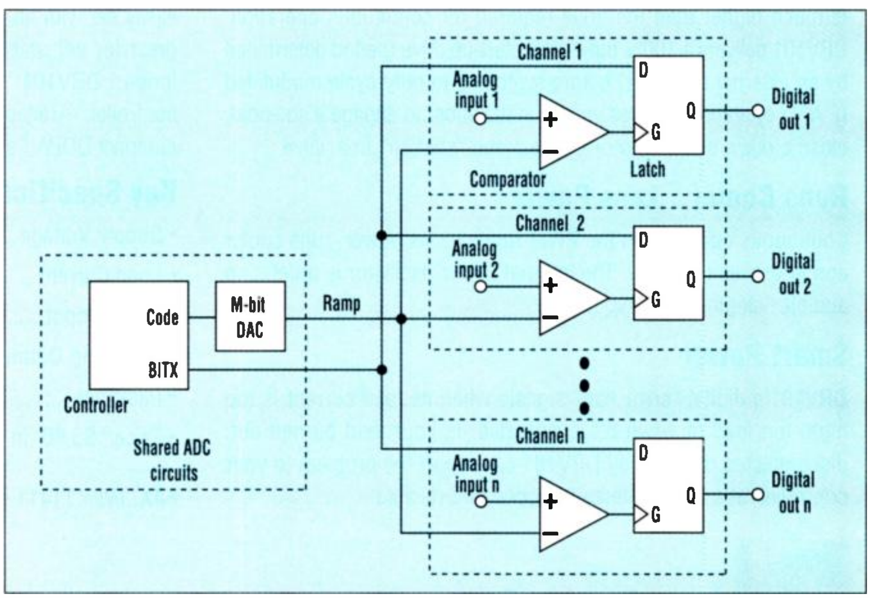
As Improvements In Δ-Σ Modulators Drive Performance In ADCs And DACs, CMOS Characterization Promises Better Analog ICs. **ASHOK BINDRA**

Delta-sigma (Δ-Σ) modulators and CMOS process technologies continue to push performance in both analog-to-digital converters (ADCs) and digital-to-analog converters (DACs). This evolution is being exploited by a wide range of applications, including imaging, video, and RF transceivers used in communications. So it comes as no surprise that this year's CICC focuses on developments in this area, as it also sheds light on special characterizations of CMOS for analog and RF circuits. An important CICC session, "Amplifiers and sample/hold circuits," tracks advancements in high-speed op amps and track-and-hold circuits.

Because one-bit, Δ-Σ modulators lend themselves to CMOS, they have been widely used in high-linearity, moderate-bandwidth data converters. But now, designers are exploring multibit techniques. Key reasons include better signal-to-noise ratio (SNR), and desired output with much less out-of-band noise, thereby easing post-filtering requirements. An added benefit is that the output signal is less sensitive to edge jitter.

But multibit modulators pose problems such as component mismatch and unshaped noise due to DAC errors. Several mismatch-shaping schemes are under development for both discrete- and continuous-time implementations of multibit Δ-Σ modulators. Session 11, "Data converters," proposes one solution. Paper 11.1, "Modified mismatch-shaping for continuous-time Δ-Σ modulators," a joint effort of Oregon State University at Corvallis; Analog Devices, Wilmington, Mass.; and Portland, Ore.-based Veris Industries, suggests a modified mismatch-shaping principle to reduce the spectral artifacts caused by element switching.

By adding extra constraints to the vector quantizer in a general mismatch-shaping system, dynamic errors caused by element switching in a continuous-time, Δ-Σ modulator are reduced in the band of interest. The



1. Aimed at CMOS image sensors, this Nyquist-rate, multichannel, bit-serial ADC uses successive comparisons to output one bit at a time simultaneously from all pixels. In this scheme, several pixels share one detector circuit, while a DAC/controller is shared by all pixels.

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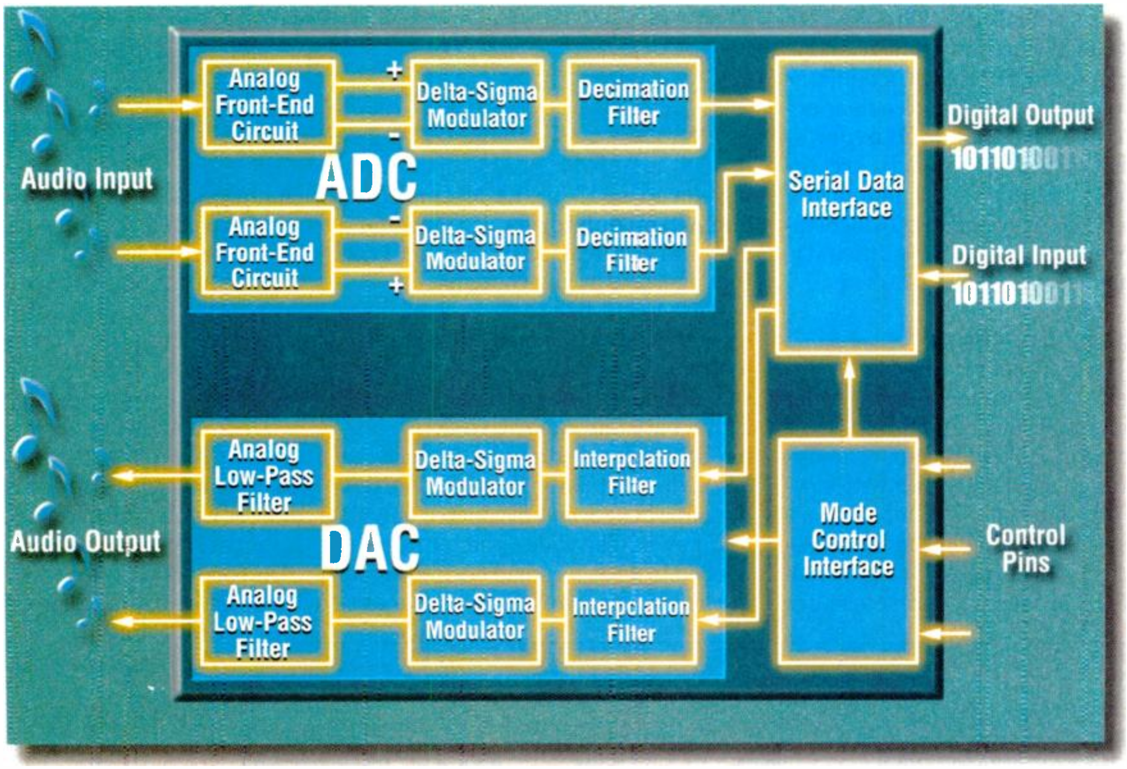

Low Cost, ΔΣ Stereo Audio CODECs

The **PCM3000/1/2/3** are single chip stereo audio CODECs (A/D and D/A) with single-ended analog inputs and outputs. The ADC core employs Delta-Sigma modulation with 64x oversampling, and includes a digital decimation filter and high pass filter. The DAC core employs Burr-Brown's proprietary Multi-Level Delta-Sigma architecture which includes an 8x oversampling digital interpolation filter. PCM3000/1/2/3 accepts all industry-standard data formats. The PCM3000 and PCM3001 operate on a +5V power supply, while the PCM3002 and PCM3003 operate on a +3V power supply.

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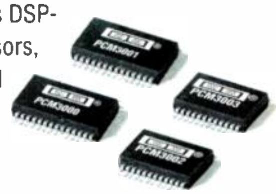

Products	Description	Supply Voltage	Bits	Dynamic Range	THD+N	Package	FAXLINE# (800) 548-6133	Reader Service #
PCM3000	CODEC	+5V	16/18	96dB	–88dB	28-Pin SSOP	11342	83
PCM3001	CODEC	+5V	16/18	96dB	–88dB	28-Pin SSOP	11342	84
PCM3002	CODEC	+3V	16/20	94dB	–86dB	24-Pin SSOP	11414	85
PCM3003	CODEC	+3V	16/20	94dB	–86dB	24-Pin SSOP	11414	86

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Burr-Brown Corporation • P.O. Box 11400 • Tucson, AZ • 85734-1400 • Call **(800) 548-6132** or use **FAX*LINE* (800) 548-6133** • **http://www.burr-brown.com/**

Distributors: Arrow: (800) 777-2776 • Digi-Key Corp: (800) 338-4105 • Insight Electronics: (888) 488-4133 • J.J.T. Supply: (800) 246-9000 • Sager Electronics: (800) 724-3780 • SEMAD (Canada): (800) 567-3623 researchers claim to have confirmed the results via Matlab simulations and an FPGA implementation. In both cases, they used a third-order, low-pass modulator with nine-level quantization and associated modified mismatch-shaping logic. The results indicate that the spurious-free dynamic range (SFDR) of the modulator improves by 15 dB, and noise floor decreases by more than 5 dB over designs that do not use shaping. According to the researchers, the method proposed here can lead to the development of high-speed, high-linearity, continuous-time Δ-Σ modulators.

EXPERIMENTAL RESULTS OF A THREE-STAGE OP AMP

Parameter	Single-ended, three-stage	Fully differential three-stage
dc gain	82 dB	122 dB
Gain bandwidth	230 MHz	138 MHz
Slew rate	150 V/µs	360 V/µs
Phase margin	49°	70.6°
Gain margin	11.5 dB	8.5 dB
Power 3.0V/2.5V	4.2 mW	11 mW

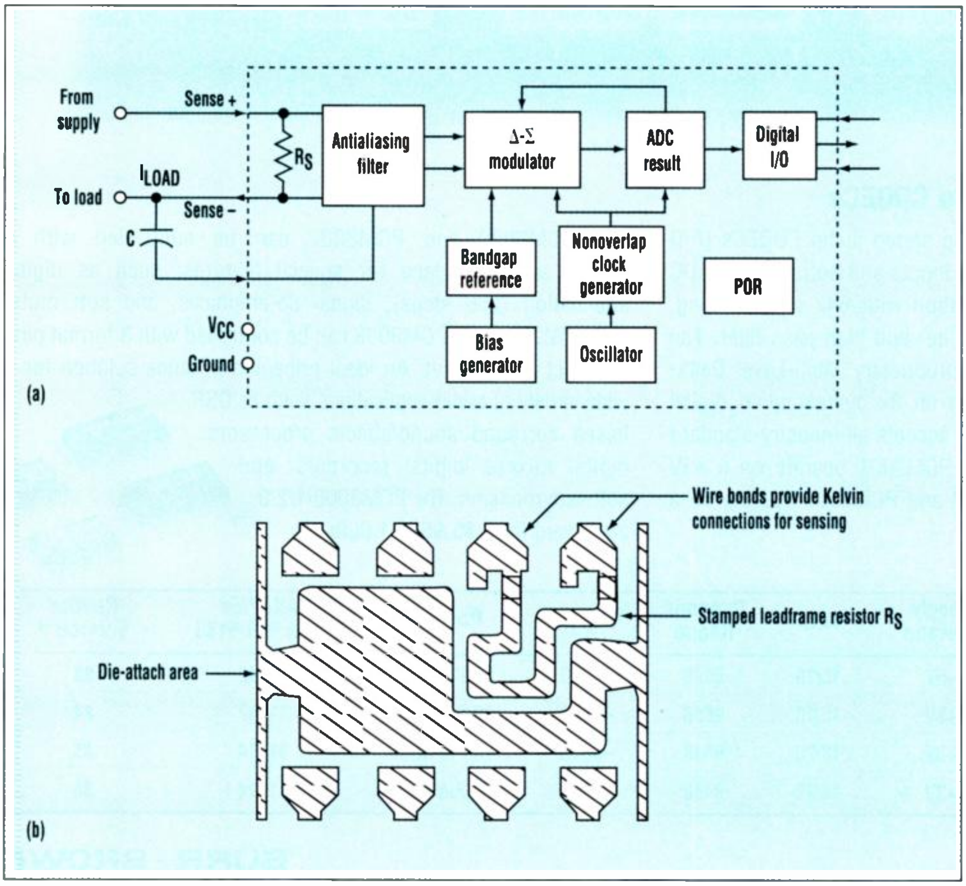
Δ-Σ For RF Baseband

Similarly, researchers at the Department of Electrical Engineering and Computer Sciences, University of California at Berkeley, push the dynamic range and bandwidth with low-power dissipation of Δ-Σ modulators for direct conversion in the RF baseband path of receivers. Using a 0.72-µm CMOS process, the researchers developed "A 13-bit, 1.4-Msample/second Δ-Σ modulator for RF baseband channel applications," (Paper 11.2) that operates at low voltages.

This circuit uses a cascade of three second-order loops operating at a 16× oversampling ratio. It also utilizes a two-stage op amp with an all-nMOS signal path and capacitive-level shifting between the stages. Operating at 3.3 V, the modulator achieves 77 dB of dynamic range, and dissipates only 81 mW power. The wide dynamic range is needed to detect a small desired signal in the presence of strong adjacent-channel interference. While earlier wideband and dynamic range issues have been addressed for direct conversion at 5 V and higher, the Berkeley paper attempts to significantly cut power consumption for these devices by combining architectural enhancements with low-voltage design.

The remaining papers in Session 11 present Nyquist-rate converters for imaging and video applications. A paper from the Information Systems Laboratory of Stanford University, Stanford, Calif., describes a "A Nyquist-rate, pixel-level ADC for CMOS image sensors" (*Fig. 1*). The paper shows that a pixel-level ADC achieves a good SNR and low power consumption at very low speeds. This technique uses successive comparisons to output one bit at a time simultaneously from all pixels. Using this scheme, the researchers fabricated a 320-×-240-pixel image sensor with an ADC in a 0.35-µm process. The chip consists of a 160 × 120 array of 2-×-2-pixel blocks, each sharing the one detector circuit, a row decoder, column-sense amplifiers, and multiplexers. The one detector circuit is implemented using a 1-bit comparator and a 1-bit latch. In this design, the ADC demonstrated integral and differential nonlinearities of 2.3 and 1.2 LSBs at 8 bits, respectively.

The last three papers Session 11 describe developments in low-power, high-speed DACs operating at 3.3 V and below. While Philips Research Labs' Digital VLSI Group in Eindhoven, The Netherlands, will discuss an 8-bit "Video-rate DAC using reduced-rate, Δ-Σ modulation," (Paper 11.4), the



2. The current sensor chip (a) stamps a 0.005-Ω metal loop into its lead frame as a sense resistor (b), which provides a 5-mV, full-scale signal at 1 A. This complete solution can detect a positive or negative current with 9-bit accuracy.

paper by Cicada Semiconductor, Austin, Tex., describes "A 325-MHz, 3.3-V, 10-bit CMOS DAC core with a novel latching circuit" (Paper 11.6). The second, very compact device combines the digital decoding latch and switch driver functions into a single circuit to keep the die area of the DAC core to about 0.135 mm^2. According to its designers, this is a substantial reduction in size compared to previous designs. The core architecture employs a double cascoded p-channel current-source array with a 5-bit segmented MSB and a binary 5-bit LSB, to achieve less than 1 LSB of differential and integral nonlinearities.

Many video and wireless communications applications are demanding high-resolution, high-speed DACs with very-low-glitch energy. A paper from the Dept. of Electrical Engineering, ESAT-MICAS, Belgium, proposes "A 12-bit, 200-MHz low-glitch CMOS DAC" (Paper 11.7). Its designers claim to have measured glitches of only 0.8 pVs. To obtain this very-low-glitch energy specification, the circuit uses a new driver based on a dynamic latch. Measured integral nonlinearity is better than ±0.5 LSB, and power consumption is 140 mW at the maximum conversion rate. Fabricated using 0.5-µm CMOS, the DAC operates at 2.7 V.

Characterizing CMOS

Digital CMOS processes have often proved inadequate for precise analog and RF circuits. But, for reasons of cost and time-to-market, many mixed-signal and analog ICs must be derived from a common mainstream digital CMOS process. Although, several efforts are underway to generate accurate models to tailor the process for analog design, the work is still not complete. An invited paper in Session 3, "Analog techniques," proposes to address this issue.

Paper 3.1, "CMOS technology characterization for analog and RF design," from the Electrical Engineering Dept. of the University of California at Los Angeles, describes various tests and techniques to quantify device behavior for analog applications. According to the author, the design of analog and RF circuits in digital CMOS, entails many difficulties because the devices are characterized and modeled to simple benchmarks such as current drive and gate delay. And, this gets worse with scaling, as semiconductor manufacturers migrate from sub- to deep-submicron CMOS processes.

By contrast, analog circuits must be optimized with respect to a number of parameters such as speed, noise, linearity, matching, and dc characteristics. Consequently, the need is dire for specialized analog characterization of the process. Toward that goal, the paper describes a set of properties and test vehicles to characterize both active and passive devices in CMOS. These include dc and ac behavior, linearity, matching, noise, and temperature dependence. The paper indicates that similar techniques must be adopted for RF design, but cautions that RF circuits are more specialized, having substantial variability of device and circuit parameters with process and temperature.

Digital CMOS processes have often proved inadequate for precise analog and RF circuits.

Paper 3.3 from National Semiconductor, Grass Valley, Calif., "Current sensor IC provides 9-bit + sign result without external sense resistor," details a solution to accurately represent currents as high as 1 A and above using sense resistors. The current sensor IC incorporates a metal loop within the leadframe (*Fig. 2*). The loop acts as a sense resistor and provides a 5-mV, full-scale output at 1-A sense current. The IC measures the sense voltage, and corrects for the temperature coefficients in the loop. It then provides a 9-bit PWM output. Fabricated on a 1-µm CMOS process, this circuit consumes less than 125 µA in the operating mode, and below 3 µA in the sleep mode. It employs a chopped Δ-Σ ADC to generate a PWM signal proportional to the current, and minimizes offset voltage.

An EEPROM-based, gain-trim circuit allows nulling of the error resulting from the stamped 0.005-Ω resistor's +2800 ppm/°C temperature coefficient. To compensate for the sense-resistor's temperature drift, the on-chip voltage reference was also incorporated with a similar temperature coefficient.

Amplifiers

Session 16, "Amplifiers and sample/hold circuits," covers the latest developments in op amps. The quest for a multistage op amp that provides the best combination of high gain, wide bandwidth, fast slewing, and excellent power efficiency in CMOS continues. Joint work by National Semiconductor's LAN Products Group, Santa Clara, Calif., and the Dept. of Electrical Engineering at Arizona State University at Tempe, yielded "A multistage amplifier topology with embedded tracking compensation" (Paper 16.1).

The amplifier requires only n-2 embedded RC compensation networks for n gain stages. In addition, the researchers developed a low-power, tracking RC compensation technique that ensures stability and fast settling over process, voltage, and temperature variations. Implementing this scheme in 0.6 µm n-well CMOS, the team developed a single-ended, three-stage amplifier with one tracking RC compensation network, as well a three-stage fully differential version *(see the table)*. The work is supported by grants from the NSF Center for the Design of Analog/Digital ICs (CDADIC), and Hewlett-Packard Co.

Paper 16.2 "A 120-MHz, 12-mW CMOS current-feedback op amp," discusses a device derived from a novel compound transistor with a higher transconductance than a single MOS transistor. It comes from the Imperial College of Science, Technology and Medicine, London, U.K.

Session 16 will also report on "A CMOS instrumentation amplifier with 600-nV offset, 8.5 nV/$\sqrt{Hz}$ of noise, and 150-dB CMRR" (Paper 16.3). Developed by scientists at the Swiss Federal Institute of Technology's Integrated Systems Laboratory, Zurich, the device has a gain of 77 dB ±0.3 dB, and a bandwidth of 600 Hz. Key to its performance is a chopper technique that's used in conjunction with a bandpass filter matched to an on-chip oscillator. Because no external components or trimming are needed, the amplifier can serve as a building block in many microvolt-signal sensor applications.

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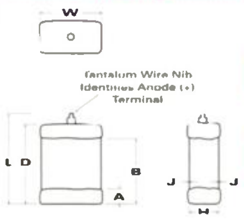
VISHAY 1000µF COATED TANTALUM CAPACITORS		 

CASE CODE	L[MAX)	WIDTH	HEIGHT	A	B	D(REF)
R	.283 [7.2]	.235 ± .010 [6.0 ± 0.3]	.136 ± .012 [3.5 ± 0.3]	.050 ± .015 [1.3 ± 0.4]	.190 ± .025 [4.8 ± 0.6]	.253 [6.4]

J[MAX)	V. RATING	CAPACITANCE	MAX DCL @ 25°C (µA)	MAX DF @ 25°C 120Hz
.004 [0.1]	6.3 volts	1000µF	63	12

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Foundations For Communication's Future Laid At CICC '98

CICC Provides A Rare Opportunity For Comm Circuit Engineers To Compare Notes On The Perils And Promises Of Submicron Design. **LEE GOLDBERG**

The 1998 CICC promises to be a gold mine for communications designers. One of the distinguishing features of this gathering is that it is not simply a place to trot out one's latest widget. It also is a very active forum for taking a close look at the design methodologies and processes that will be used to design tomorrow's integrated circuits.

The insights provided at CICC come none too soon. While marketing types glibly prattle on about the dawn of the age of the "system on a chip," engineers and scientists throughout the world are busily trying to make the technology meet the hype.

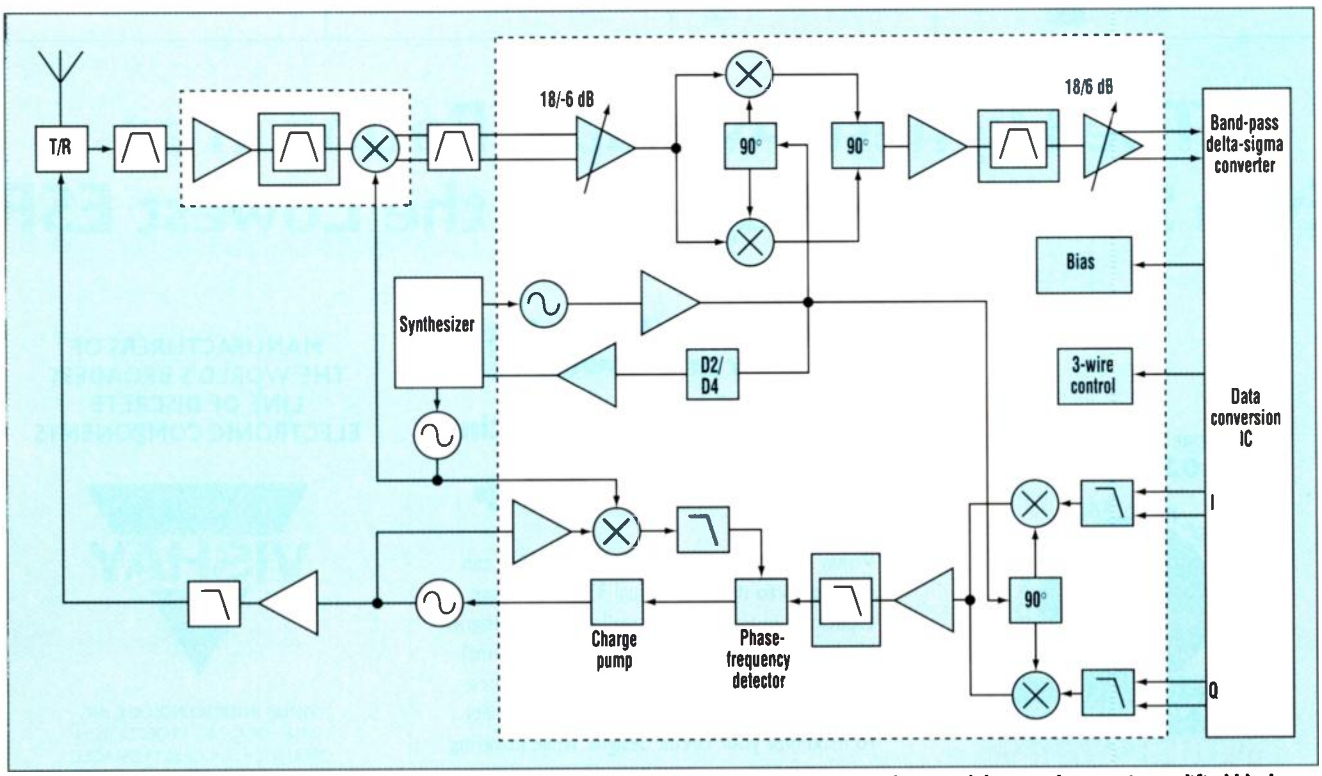
In addition to a formidable array of novel, single-chip solutions for wired and wireless communication, this year's sessions are chock-full of solutions to the new classes of problems emerging as designs migrate towards deep submicron processes.

Back To Basics

Some of the most interesting work at CICC is on the basics. A re-emphasis on device theory, oscillator design, and monolithic RF circuit analysis is happening because designers must contend with running their chips at higher frequencies even as feature size, operating voltages, and power budgets shrink. These opposing demands are causing them to re-examine the assumptions that have characterized both CMOS and bipolar circuit design for the past half-decade or more.

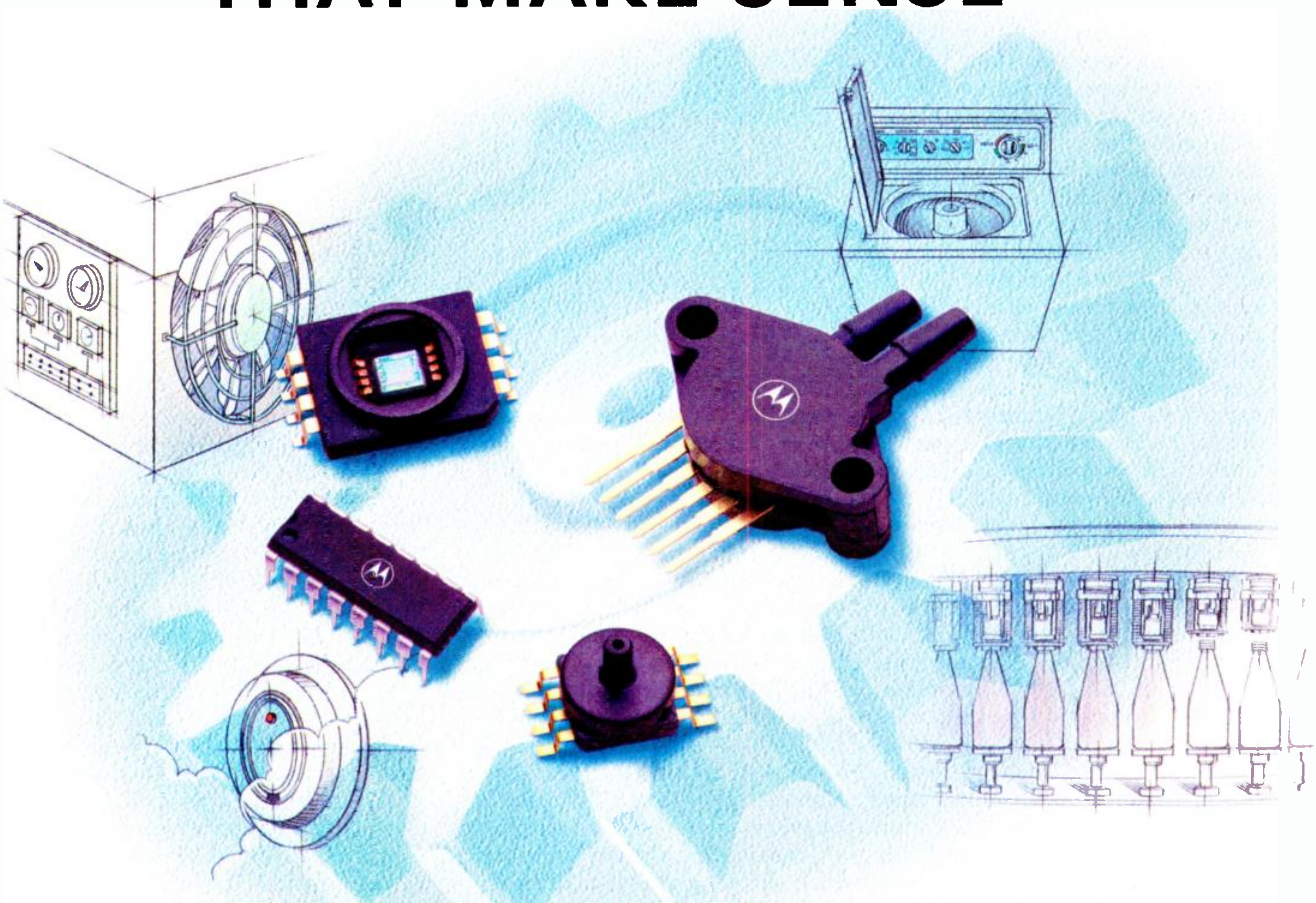
Session 4, entitled "Design and Analysis of Oscillators," typifies this "back to basics" movement. While on-chip oscillators using monolithic passives have been in production for some time now, the higher operating frequencies and sophisticated, multiphase modulation schemes used in the next generation of products are demanding much higher levels of performance than ever before. Developments from this and other sessions will be essential to integrating precise high-frequency sources onto communication ICs.

In his paper, "On the Exact Design of RF Oscillators," Q. Huang of the Swiss Federal Institute of Technology, Zurich, presents a rigorous analysis of the phase noise exhibited in Colpitts-type oscillators. From this he derives



1. This single-chip, dual-band transceiver is intended for cellular/PCS operation using constant-envelope modulation schemes. A simplified block diagram of a single-band system is shown.

SENSING SOLUTIONS THAT MAKE SENSE



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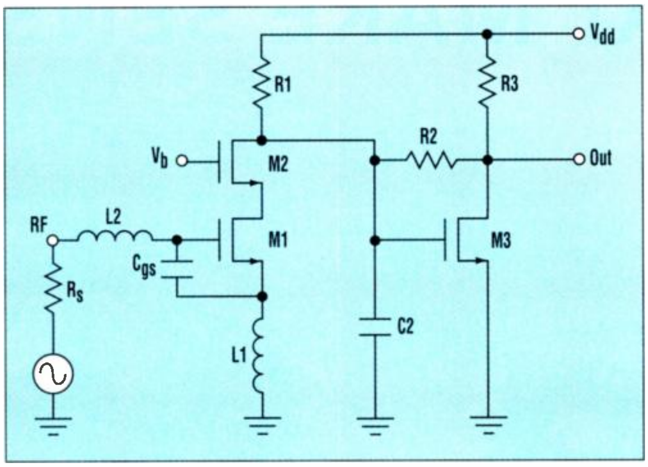
an exact formula for the phase noise-to-carrier ratio for a given design.

Given the use of standard CMOS processes, the author arrives at three possible methodologies to improve sideband noise and carrier ratio. While raising bias current is not desirable in most applications, Huang describes methodologies for cutting inductor losses and calculating the minimum size of the circuit's capacitive elements permitted by process variations. The extremely detailed explanation of the trade-off methodologies that follows should prove valuable to the many designers tackling GHz+ designs.



2. A common-source LNA avoids noise due to parasitic effects commonly found in common-gate realizations. Early samples of this unit have demonstrated noise levels as low as 1.7 dB.

Similar topics also were addressed in "Phase Noise And Timing Jitter In Oscillators," presented by a team of researchers from Bell Laboratories, Murray Hill, N.J. The team describes its efforts to apply "a rigorous nonlinear analysis for phase noise in oscillators," and reaches some interesting conclusions. Rather than becoming undefined at the carrier frequency, the power spectrum of an oscillator assumes a Lorentzian profile about each harmonic.

They also uncover a phenomenon whereby "the average spread of the timing jitter grows exactly linearly with time," allowing the use of a single scalar constant to characterize both jitter and spectral broadening due to phase noise. Based on these observations, the researchers show how they have developed efficient computational methods for predicting phase noise in circuits.

Other important topics in Session 4 include "Phase Noise in Multi-Gigahertz CMOS Ring Oscillators," from the Center for Integrated Systems, Stanford, Calif., and a paper entitled "Nonlinear Behavioral Modeling And Phase Noise Evaluation In Phase Locked Loops," presented by the Electrical Engineering Department of Catholic University (ESAT-MICAS), Heverlee, Belgium.

Phase Locks To Go!

Phase-locked loops and other frequency sources also enjoy a significant degree of attention in Session 28. Typical of these papers was "A 2-V, 1.6-GHz BJT Phase-Locked Loop," presented by the Department of Electronics Engineering, at the National Chiao-Tung University, Hsin-Chu, Taiwan. Anticipating applications in the cellular, pager, and PCS markets, the team designed a low-voltage PLL using BJT transistors fabricated in 0.8 µm biCMOS. An LC-tuned negative resistance oscillator shares the chip with its companion PLL, drawing a total of 225 mW of power consumption.

The Georgia Institute of Technology, Atlanta, in conjunction with Rockwell Semiconductor Systems, Newport Beach, Calif., produced a paper entitled "A 1 GHz, Low-Phase Noise CMOS Frequency Synthesizer With Integrated LC VCO For Wireless Communications." In the paper, tshey describe how they built a synthesizer with 64 programmable frequency channels. They enjoy a frequency resolution of f_{ref} / 64 and a phase noise figure of –110 dB/√Hz at a 200-kHz offset frequency. The fractional-N architecture achieves this extremely low noise figure by employing a noise-shaping method that suppresses fractional spurs using high-order sigma-delta loops.

Also in the session is "RF-CMOS Oscillators With Switched Tuning," presented by the Electrical Engineering Department of the University of California, Los Angeles. The paper's authors tackle the tough topic of supplying a highly stable, tunable oscillator fabricated using standard CMOS processes.

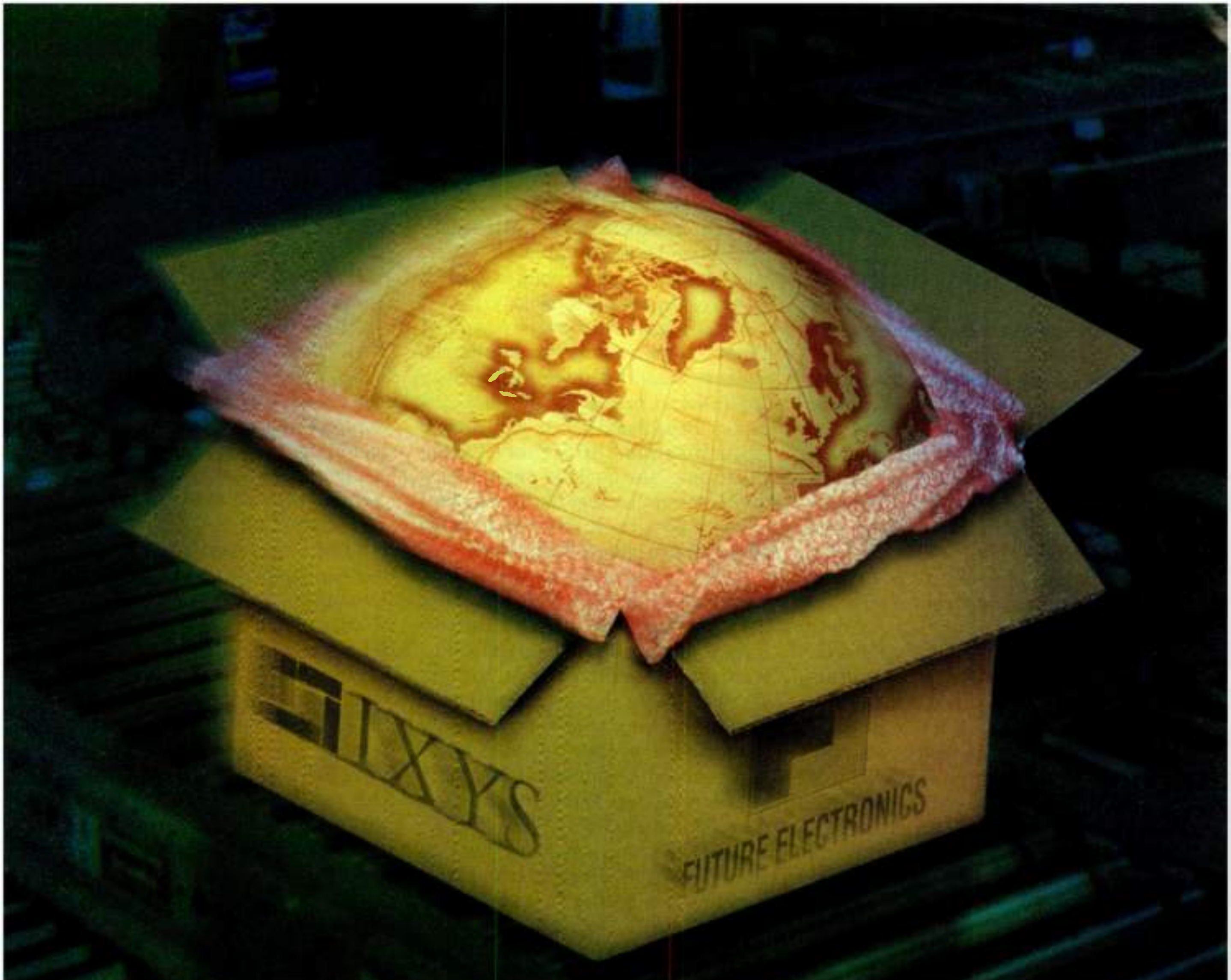
They address the practical problems involved with designing low-power, phase-stable, CMOS RF oscillators that have a wide enough tuning range to compensate for the relatively large variations in the values of passive components normally encountered in bulk CMOS fab lines. The result is a circuit that employs multilayer inductors and switched capacitors connected by MOS analog switches designed to have low on-resistance and parasitics.

Wired communications also was represented in Session 28 with "2.488 Gbit/s Bipolar Clock and Data Recovery IC For SONET (OC-48)," presented by AMCC Corp., San Diego, Calif. The paper described a bipolar silicon IC that performs both clock recovery and data retiming functions for OC-48 data streams. This development is notable for several reasons, including its single-chip implementation, low power consumption (800 mW), and low external component count. Employing a first-order active filter in its loop, the chip achieves a jitter generation of 2.8 ps rms, and an impressive jitter transfer figure of less than 0.005 dB.

The importance of truly flexible frequency sources was driven home by "A 2.7V 900 MHz/1.9GHz Dual-band Transceiver IC for Digital Wireless Communication." The paper was a joint effort between Broadcom, Irvine Calif., and Rockwell International, Newport Beach, Calif. The chip that forms the heart of the system incorporates a receive, transmit section, plus a local oscillator that boasts a phase noise level of –106 dB/√Hz *(Fig. 1)*.

CMOS Does Microwaves!

With the increasing price and performance pressures in the wireless arena, we are seeing the humble CMOS device being pressed into service in areas never conceived of even five years ago. It is no surprise then, that CICC's Session 5, "Wireless Circuit Design Techniques/Technology," was devoted almost exclusively to applying CMOS circuits in the microwave spectrum.



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One of the most valuable papers of the conference was given by the RF Technology Group at the Wireless Communications Center of the University of Waterloo, Ontario, Canada. In "Microwave CMOS—Devices and Circuits," the authors address the technical challenges and of designing front-end CMOS RF circuits, and how to apply microwave design methodologies to meet them. One of the more important points made is that although commercial CMOS processes exist with F_t's of 20 GHz and beyond, the transistor structures designers traditionally use are not optimized for high-frequency applications.

The paper uncovers three primary reasons for this apparent disconnect. The first is that the models currently available for MOSFET devices (such as HSPICE) don't do a good job in predicting power gains and noise figures. Secondly, most MOS RF ICs employ design topologies that are simply copied from BJT and MESFET designs, and don't take advantage of the fact that complementary devices can be used. Finally, the authors indicate that "many (MOSFET) concepts and design methodologies have to be reformulated to include some microwave concepts."

The paper then goes on to present a series of new models for MOS transistors, and design methodologies which make use of the information contained in the models. Emphasis is placed on understanding how gate resistance affects performance and accurate noise modeling at microwave frequencies.

Toward the end, design methodologies for classical applications, such as LNAs and downconversion mixers, are explored in depth. The information contained in this and other papers at CICC will help designers deliver much more efficient and effective MOS-based RF components, without having to wait for advances in process technology.

CMOS LNAs also were a topic of discussion for a team representing the Swiss Federal Institute of Technology and Toshiba Corp., Kobe, Japan. In the paper, "Broadband 0.25 micron CMOS LNAs with Sub-2 dB NF for GSM applications," the authors explain how they cracked the magic 2-dB noise barrier—no easy trick, even when using more suitable bipolar technologies.

Achieving an inexpensive low noise is of great significance, since it is one of the key components affecting the performance of cellular handsets. The team employ a common-source input architecture for the first stage (rather than a conventional common-gate arrangement) to achieve devices which had good impedance, and linearity characteristics, and demonstrated noise figures as low as 1.74 dB *(Fig. 2)*.

Another novel development in Session 5 was "A 1 GHz Programmable Analog Phase Shifter for adaptive Antennas." Written by researchers from the University of Toronto, Canada, the paper describes a programmable analog phase shifter which can be used in adaptive antenna systems to steer the direction of an antenna array. The bipolar device was small enough to permit up to 16 phase shifters to be put onto a single chip. This technology may have significant applications in advanced cellular systems which employ adaptive picocells to enhance coverage and bandwidth density.

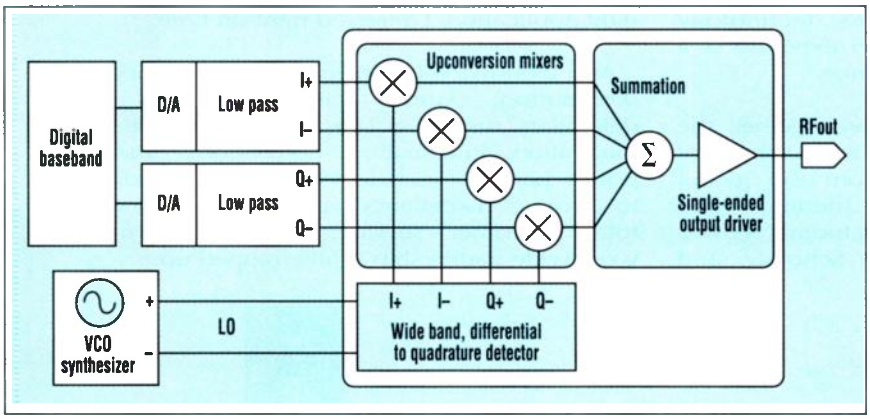
In addition, ESAT-MICAS made a pair of interesting contributions to Session 5. The first, "A 10 mW Inductorless Broadband CMOS Low Noise Amplifier for 900 MHz Wireless Communications" described a part which offered a noise figure better than 3.3 dB while drawing only 3.4 mA from its 3.0-V supply. Rather than use a classical heterodyne receiver architecture, it makes use of a novel current-reuse technique in an all-nMOS open-loop configuration.

In the second paper, "A 1.5V, 3 GHz, Wide Band CMOS Quadrature Direct Up-Converter for Multi-Mode Wireless Communications," the team from Heverlee presents a novel device which includes a wide-band polyphase filter, a set of linear quadrature up-converters, and a single-ended output stage *(Fig.3)*. It demonstrates over 35 dB of mirror suppression within its operating range of 700 MHz to 3 GHz. Devices like this could be integrated into the transmit path of an RF IC, eliminating the need for much of the IF and RF filtering used in conventional architectures today.

RF Systems

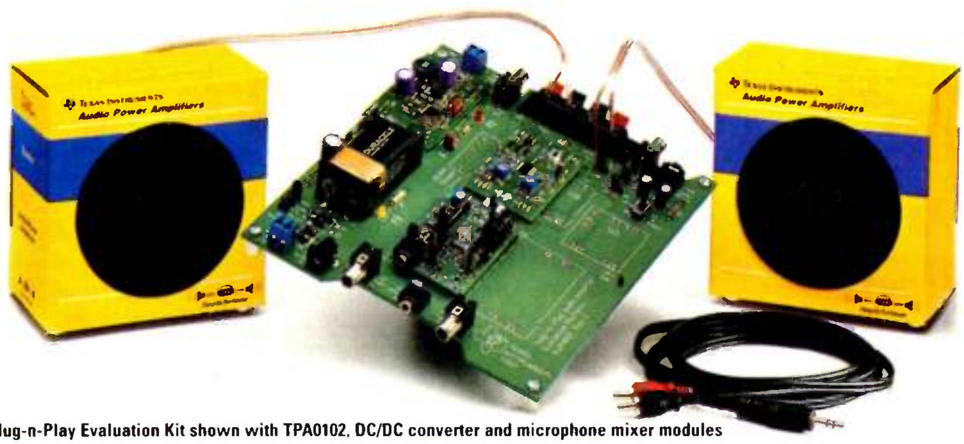
Session 20, "Wireless Transceivers and Systems," also provides a wealth of information on this emerging generation of integrated RF chips. For perspective on this burgeoning field, it may be useful to read the paper written by B. Razavi from the University of California, Los Angeles' Electrical Engineering Department. Entitled "Architectures and Circuits for RF CMOS Transceivers," it covers receiver topologies such as heterodyne, direct-conversion, and image-reject, and contrasts their relative strengths and weaknesses. The author then examines the design of other building blocks such as LNAs, mixers, baseband interfaces, and oscillators.

Also of note in Session 20 was "A High-Q 200-MHz Low-Power Fully Integrated Bandpass IF Filter," presented by SGS-Thompson, Crollen, France, and France Telecom, Meylan, France. A combined effort by researchers from Alcatel Bell, Antwerp, Belgium, SSL, Swindon, England, TEMIC, Heilbronn, Germany, and Alcatel SdM, Charleroi, Belgium, produced an interesting report entitled



3. This CMOS quadrature direct up-converter employs a unique wide-band polyphase filter, a series of linear quadrature up-conversion mixers, and a single-ended output stage. Boasting more than 35 dBc of mirror suppression, it has an operating range of 700 MHz to 3 GHz.

PLUG-N-PLAY AUDIO EVALUATION KIT.



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TEXAS INSTRUMENTS

"Silicon Germanium and Silicon Bipolar RF Circuits for 2.7 V Single-Chip Radio Transceiver Integration." The paper describes the basics of the low-voltage design and preliminary measurement results for this very promising single-chip transceiver.

The receiver section employs a balanced-quadrature-demodulator architecture, realized by means of an input differential pair with emitter degeneration. The single-ended LNA signal is converted to a balanced radio signal to drive the mixers using capacitive coupling. On the transmit side, a zero-IF single side-band mixer is followed by a pre-power amplifier (PPA) Current-mode operation was employed to ensure that the balanced baseband I and Q inputs to help the amplifier use its small (2.7-V) supply voltage swing efficiently. The PPA then delivers its 0-dB output signal to a 1:2 transformer before delivering it to the input of an external PA.

Catch A Glimpse Of The Future Of EDA Tools And Methodologies

Advanced Simulation Techniques, DSM Issues, And Innovative Modeling Methods Highlighted At CICC. **CHERYL AJLUNI**

As in past years, issues related to Electronic Design Automation (EDA) play a central role at the Custom Integrated Circuits Conference, (CICC). In part this is because of the ongoing migration to system-on-a-chip design, as well as the availability of smaller design geometries. These factors have stressed the limits of available EDA tools and methodologies, and forced vendors to seek new techniques to supplement traditional design practices. In particular, the EDA issues highlighted at this year's CICC include advanced simulation techniques, designing in a deep submicron (DSM) environment, development of DSM libraries, and new modeling techniques for analog and high-frequency designs.

Simulation Techniques

Despite the onslaught of research and development in new EDA tools and design methodologies, simulation still remains a staple of the designer's EDA diet. But, with the rising complexity of IC's in recent years, traditional simulators are being strained to the limits of their capabilities. As a result, attention has focused on improving simulation techniques to address a variety of application-specific issues. Session 22, "Advanced simulation techniques," offers a look at some of the tools and methodologies that are now being introduced for implementing advanced simulation techniques.

"Modeling and simulation for low power in mixed-signal integrated systems," from the Katholieke Universiteit Leuven, Heverlee, Belgium, shows how to make modeling and optimization of the power consumption in mixed-signal integrated systems a reality. Targeted at telecommunications, portable electronics, and wireless communications, these techniques focus on minimizing the system's power consumption at the architectural level, and maintaining this state throughout all lower levels of the design hierarchy.

Several technological advances and the development of a tool for architectural-level exploration and optimization of analog RF-receiver front-ends, known as ORCA, make this concept feasible. The tool allows the different blocks in the design to be modeled at a behavioral level, with simulations performed in the spectral domain for realistic input power spectra. This means that the designer can interactively explore a variety of RF-receiver topologies, and examine all associated design trade-offs. Building on this development, researchers formulated an optimization algorithm for determining the optimal analog-digital partitioning for a mixed-signal system, as well as a method for modeling the power of analog blocks. Additionally, a system for custom synthesizing analog blocks with minimum power consumption is presented.

A technique for analyzing circuits with widely separated frequencies comes from Bell Laboratories, Murray Hill, N.J., and is summarized in "MPDE methods for efficient analysis of wireless systems." The numerical method is based on the multirate partial-differential equation (MPDE) formula. It makes simulation of a number different types of circuits such as dc-dc power converters, switched-capacitor filters, and RF mixers, now possible.

The technique works by representing multirate signals as functions of more than one time variable. In this manner, it is possible to analyze strong nonlinearities together with widely separated time scales. This technique has achieved simulation speed increases of more than two orders of magnitude, as compared to more traditional simulation methods. It can also be used to abstract compact, high-level models from detailed circuit descriptions of wireless system components.

As gate counts rise and component speed increases, the ability to perform accurate timing verification at the system level becomes crucial. Just such a technique is the focus of a joint effort on the part of researchers at Stanford University, Stanford, Calif., and the University of California at San Diego. As summarized in "Practical timing analysis of asynchronous circuits using time separation of events," the technique works by modeling interacting asynchronous controllers and datapath elements using special timing constraint graphics. Performance metrics and circuit timing constraints that need to be checked are then for-

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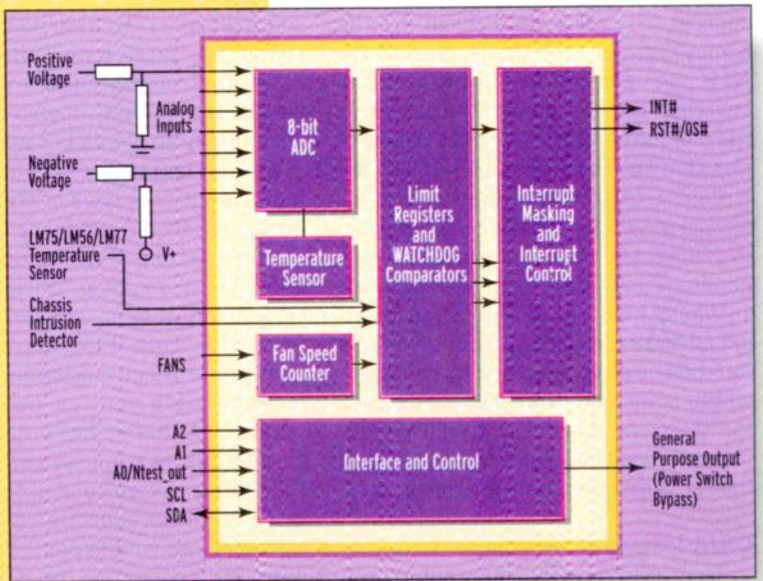

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mulated as time separations between appropriate events. The time separations between all pairs are computed in a single pass.

Another interesting development, a transistor-level simulator for switched-current (SI) integrated circuits, hails from Columbia University, New York, N.Y. As detailed in "Simulator for switched-current integrated circuits," the simulator operates on the assumption that the circuit completely settles within each switching interval. This effectively reduces the transient analysis to a simple problem of solving for a set of nonlinear algebraic equations for each switching interval. Assuming small-signal operation, the frequency response can then be easily obtained by running a single transient simulation to extract the bias point. A standard frequency-domain analysis for switched networks is then performed to complete the process.

DSM Issues

Issues surrounding deep submicron (DSM) design are not new. In fact, much of the attention given to the EDA industry today either deals with what DSM means, or how it impacts the traditional design environment. What's really needed though, are ways to improve current tools, techniques, and methodologies for dealing with these DSM issues. Two sessions at this year's CICC, Session 14, "Deep-submicron library design," and Session 27, "DSM Issues, Tools, and Methodologies," focus specifically on this point. They offer practical, real-world advice intended to help the designer steer through the quagmire of obstacles encountered in a DSM environment.

The topics in Session 14 range from the timing qualification of a 0.25-µm CMOS ASIC library, and an automatic layout generation system for CMOS uniform height cells, to a standard cell methodology for the development of a complex, mixed-signal, analog and digital Power IC.

Cadence Design Systems, San Jose, Calif., presents a newly developed algorithm that can compute the effective capacitance in DSM circuits. Compared to more conventional algorithms, this technique exhibits significant improvements in both accuracy and speed. As explained in "A new algorithm for computing the effective capacitance in deep-submicron circuits," the technique relies on a table of circuit simulation results. Here, designers obtain the effective capacitance of any circuit. Derived from a series of Spice simulations in which the driver circuit closely represents a typical MOS driver, the algorithm interfaces with industry-standard empirical timing libraries. As a result, the algorithm also interfaces with timing-driven EDA applications.

Of particular interest are "Manufacturability analysis of standard cell libraries," from Level One Communication Systems, Sacramento, Calif., and "An overview of library characterization in semi-custom design," from Motorola, Phoenix, Ariz. The first paper discusses a methodology for comparing multiple cell libraries, whether in-house or commercial. It also details an application illustrating the prime advantages of building an internal library for high-volume designs. The second paper assesses current characterization flows, and delves into such topics as data management, the effects of resistive interconnect, and high-frequency design, as well as rapid retargeting of existing libraries to new processes.

While Session 14 focuses more on DSM library design issues, Session 27 targets the tool- and methodology-specific end. In particular, some of the topics include a look at what a fabless design company will encounter as it moves into the DSM design environment. Special emphasis is on the types of design flows and libraries required for 0.35-µm and smaller feature size. Additionally, there's a technique for saving power dissipation in large datapaths that reduces unnecessary switching activity on wide buses.

A new router is also presented that effectively reduces antenna effect damage. Developed by Mitsubishi Electric Corporation, Hyogo, Japan, it works by combining a traditional router and a modification of wires using a rip-up and reroute method. The technique has been successfully demonstrated and results in minimal die size and performance penalty.

A new method for inserting buffers into a circuit, in conjunction with gate-sizing techniques, offers better power-delay and area-delay trade-offs. The technique, developed by Cadence Design Systems, San Jose, Calif., is based on a delay model which incorporates placement-based information, and the effect of input slew rates on gate delays.

Of particular interest is a VLSI design technique developed to deal with standard cell placement. The procedure, which hails from the University of Waterloo, Ontario, Canada, works by combining a method for iterative construction with a nonlinear programming local improvement method.

As described in "A nonlinear programming and local improvement method for standard cell placement," the technique is specifically intended to work for row-based, standard cell layout with instance sizes of up to tens of thousands of cells. During operation, the iterative construction method provides an initial placement. This construction technique spreads cells evenly through the placement area, and as a result, generates a good legal placement that can then be utilized as input for a local improvement method. The local improvement method takes this initial placement and searches to see if it can find a better one.

Another interesting development, for growing and inserting clock trees on low-power chips, comes from IBM Microelectronics Division, Endicott, N.Y., and is detailed in "A new direction in ASIC high-performance clock methodology." When utilized with an automated balanced router and a special clock buffer circuit, it is suitable for a large variety of chip sizes, package types, latch counts, and operating frequencies.

Key features of the method are that it refrains from adding wires unnecessarily, it avoids the noise and power-supply drop associated with localized high-current-density clock circuits, and it accounts for high-frequency effects such as inductance. It has been proven to work, and can serve a large number of macrocells and cores. The method also handles greater than 40,000 master/slave latch pairs in either a flat or hierarchical environment.

Advances In Modeling

While simulation remains a staple of any EDA design flow or methodology, the key to making simulation runs accurate and worthwhile is good models. Accurate, detailed models become even more important in a complex DSM design environment. They are

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required for optimal completion of any design. This year, in recognition of the increased focus on developing accurate models, CICC features two sessions dedicated to analog modeling and modeling for high-frequency designs.

Session 10, "Modeling for high-frequency designs," features such topics as a fast, integral-equation-based method for full-wave extraction in layered media; a methodology for simultaneous calibration of critical ac MOSFET model parameters; and an evaluation of MOS compact models that focuses on BSIM3v3.

An algorithm for generating upper and lower bounds on inductance, including frequency dependencies, comes from Carnegie Mellon University, Pittsburg, Pa. These bounds are useful for fast calculation of worst-case inductance, and can be utilized as a quick screening process to evaluate the impact of inductance over a specified frequency range.

In "Nonlinear macromodels of large, coupled interconnect networks," researchers provide a look at a new macromodel for the crosstalk effects between adjacent interconnects. The macromodel brings together a reduced-order representation of the equivalent impedance and coupling seen at each driver output, and a network order-reduction-based macromodel of the overall linear interconnect network. The macromodel, which takes into account the driver nonlinear behavior, has been proven successful in application to 0.25 µm, high-density CMOS technology.

Another interesting development hails from Bell Laboratories, Lucent Technologies, Murray Hill, N.J., "How to make theoretically passive, reduced-order models passive in practice." Researchers developed a new variation on the symmetric multiport Pade via Lanczos algorithm (SyMPVL). Based on a new band Lanczos process with coupled recurrences, the algorithm produces stable and passive models for all circuits characterized by pairs of symmetric positive semi-definite matrices. This development is significant because, until now, it has been virtually impossible to produce unstable and nonpassive models using traditional circuit-reduction methods.

Session 23, "Analog modeling and CAD," offers a look at such topics as a behavioral model of a digital-to-analog

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converter (DAC), a switched-current circuit technique for the fabrication of mixed-signal ICs in a conventional CMOS process, and a look at the timing jitter of oscillations in digital system applications. A process for transforming small-signal modeling into control system modeling comes from the Katholieke Universiteit. This modeling technique results in a behavioral signal-path model that shows the different poles and zeros along the signal path. This feature provides valuable insight into a circuit's operation, and makes it possible to perform pole-zero placement of specific design parameters.

In "Schematic-driven module generation for analog circuits with performance optimization and matching considerations," from Washington State University, Pullman, Wash., a technology-independent, correct-by-construction, module-generation technique for analog circuits is described. The layout is generated as an optimal stack of transistors with complete inter-module connectivity. Design constraints are taken into consideration, and the port structures for each module are created. A fully parameterized, design-rule-independent module is then generated to match the selected circuit partition.

Another innovative development comes from the Katholieke Universiteit, and is detailed in "Mondriaan: a tool for automated layout synthesis of array-type analog blocks." The paper discusses the development of a new tool set that is specifically targeted at the physical design automation of array-type analog blocks. This flexible tool solves the layout synthesis problem using a three-step procedure: floorplan generation, symbolic place and route, and technology mapping. The process is technology independent and takes into consideration the typical analog constraints.

The breadth of information provided at this year's Custom Integrated Circuits Conference offers not only a look at the future of EDA, but real-world solutions that designers can utilize today to improve their designs. As a result, for any designer faced with issues of DSM design, or who requires the speed and accuracy that comes from the use of either advanced simulation techniques or new, more comprehensive models, CICC is one resource that can't be overlooked.

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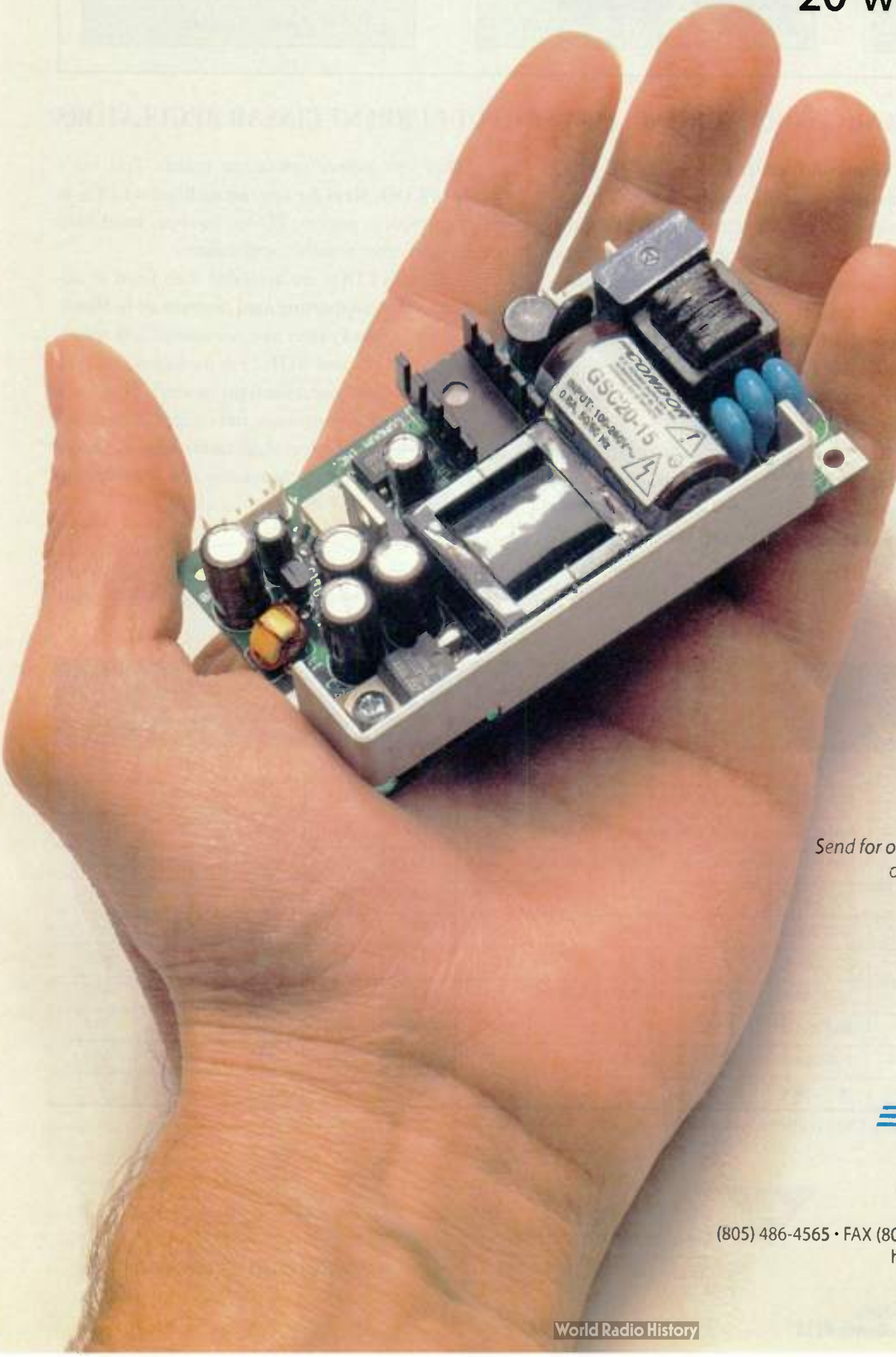

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A Family Of High-Speed ADCs Taps Δ-Σ Modulation And Digital Filtering To Obtain True 16-bit Performance At 2.7 V.

Ashok Bindra

Accuracy and precision bars continue to rise in many industrial process control applications, battery operated medical instruments, as well as portable weighing scales. These applications are demanding higher performance, higher speed, and lower power consumption, all while keeping costs low. Designers have resorted to digital techniques to satisfy an insatiable appetite for such demands. And, this progression in data acquisition is putting enormous pressure on the suppliers of analog-to-digital converter (ADC) ICs, the core of the front-end data-conversion block for these systems.

Combining architectural improvements with refinements in finer CMOS and biCMOS processes, makers of ADC chips are pushing the performance envelope of high-resolution data converters, while piling more functions and interfaces around the chip for a more integrated solution. In fact, these integrated ADCs are providing complete front-end systems that can be linked directly to the transducer without any additional conditioning of the input signal. At the same time, finer process geometries are enabling designers of these chips to keep the operating voltage and power low, which means smaller packages at lower prices.

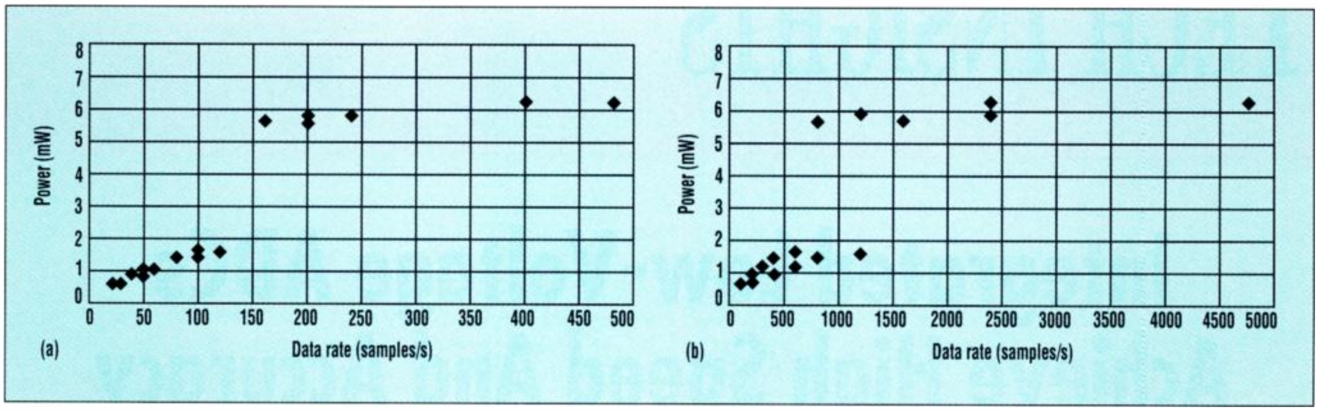
To meet such stringent end-application demands, Maxim Integrated Products has crafted a novel ADC family that taps the advantages of the delta-sigma (Δ-Σ) modulation technique and digital filtering to accomplish true 16-bit accuracy from a single die. The MAX1400/01/02/03 high-speed ADC family of chips are made on a 1.0-µm biCMOS process and are available in miniature plastic 28-pin SSOPs, with guaranteed ac and dc performance down to a 2.7-V supply.

While the bulk of the family's circuitry is in CMOS, very high precision current sources are implemented in bipolar to obtain the desired accuracy and noise performance for the MAX1400 series. Although the Maxim parts look similar to competitive devices, they outperform competitors' parts in a number of ways.

The new ADC ICs promise to deliver a complete analog front-end for multichannel low-frequency measurements at unparalleled speeds, and do so with "unsurpassed" noise and linearity performance particularly at low voltages. The MAX1400 series of ADCs are guaranteed to provide integral non-linearity of 0.0015% all the way down to 2.7 V. Also, according to Maxim, the MAX1400 ADCs are designed to generate 18 bits of data, even though the converters are specified as true 16-bit devices. Typical power consumption is 1 mW.

In order to serve varying needs of different users, the MAX1400 converters offer flexibility in terms of resolution and power *(Fig. 1)*. This feature permits the user to optimize the resolution versus output data rate, thereby allowing higher data rates for lower resolution. For example, to attain true 16-bit conversion, the sampling rate is up to 480 samples/s. However, that rate can go as high as 4800 samples/s for 10 to 12 bits of accuracy.

"At 4800 samples/s, the MAX1400-03 ADCs are four to eight times faster than existing devices from key players



1. The MAX1400 series of ADCs from Maxim Integrated Products offers flexibility in the choice of resolution, power, and data rate. The user can trade off output data rate versus power for a given resolution. Depending on the application, the MAX1400 ADCs can be optimized for either the lowest power dissipation at 16-bit accuracy(a) or the highest output data rate at 12 bits (b).

like Analog Devices (Norwood,Mass.), Burr-Brown (Tucson, Ariz.), and Harris Semiconductor (Melbourne, Fla.)," claims Maxim's director of product development and definition Ali Foughi. "And, this data rate is independent of the programmable-gain amplifier (PGA) setting."

In addition, the MAX1400 ADCs enable the designer to trade off speed versus power. This feature allows the user to select the sampling frequency in accordance with power dissipation. As a result, the converters can be optimized for either the lowest power dissipation or the highest output data rate without losing resolution and linearity, according to Foughi.

Flexible Data Rate

"This flexibility in the data rate versus resolution and power is made possible by the modulator design which allows it's sampled rate to be varied over an 8 to 1 range," says Mark Pinchback, lead designer of the MAX1400 ADC family. The sample rate of the digital filter tracks that of the modulator and provides a variable decimation factor, adds Pinchback. The digital filter implements both a Sinc (Sinx/x) and $Sinc^3$ or $(Sinx/x)^3$ low-pass filter functions.

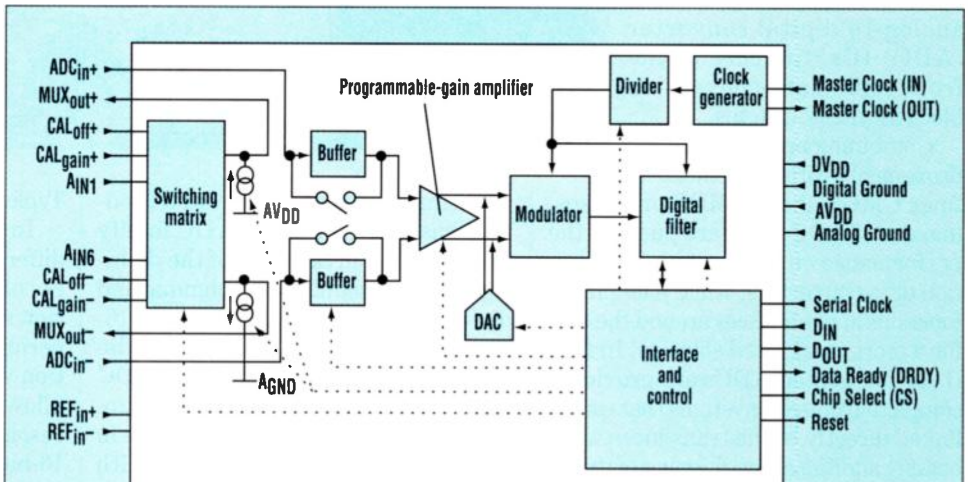
"While the Sinc response enables fast settling time, the $Sinc^3$ response is tailored for accuracy," notes Pinchback. "The Sinc mode provides a fast settling response while retaining the same frequency response notches of the $Sinc^3$." By comparison, the Sinc filter settles in one word, as against three output samples needed for the $Sinc^3$ filter to settle.

For instance, with 60-Hz notches, the settling time for the Sinc mode is 1/60 or 16.7 ms, whereas the $Sinc^3$ mode would settle in three times as much or 50 ms. Consequently, by simply setting the "fast" bit in the global set-up register, the user can toggle between Sinc and $Sinc^3$ modes, as required by the application, notes Pinchback.

In essence, the data conversion from analog to digital is performed by the second-order switched-capacitor Δ-Σ modulator, which samples at a much higher rate than the bandwidth of the input signal. The fast serial data stream generated by the Δ-Σ modulator is fed to the digital filter for decimation of the digital output *(Fig. 2)*.

In fact, there are seven 8-bit control registers on-chip, out of which six others are intended for configuring the PGA gain, signal polarity, channel selection, and data rate. Although the MAX1400 members are tailored for three fully differential signal input channels, they can be configured with five pseudo-differential input channels.

In either mode, the ADCs offer two additional fully differential channels for system calibration. While these channels are intended for correcting system gain and offset error, they can be used as additional fully differential signal channels. Depending on the input resolution required, each channel could be independently programmed with a gain between 1 and 128.



2. Combining second-order delta-sigma modulation with a Sinx/x (or Sinc) digital filtering function, the MAX1400/01 ADCs achieve true 16-bit accuracy for significantly high output data rate at supply voltages as low as 2.7 V. They also provide access to the multiplexed output for connection to a high-performance amplifier in the signal path.

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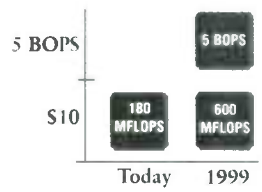

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"This approach permits a user to design a very sensitive converter," notes Pinchback. "In addition, it permits the user to link the ADC directly to the transducer, eliminating the need for signal conditioning before feeding it to the MAX1400 ADCs." However, Pinchback cautions that very high gain results in thermal noise, becoming the limiting factor. The on-chip 8-bit registers can be accessed via the serial port.

Bells And Whistles

Speaking of the serial port, the MAX1400 is compatible with three wire interfaces like the standard peripheral interface (SPI) and the queued SPI (QSPI). Also, according to Pinchback, input signals from the transducer or other sources are often corrupted with dc offset and noise. To alleviate this problem, the MAX1400 converter incorporates a 3-bit +sign digital-to-converter (DAC) at the modulator input, that enables each channel independently to compensate a dc offset of up to 116.7% of the selected full-scale range.

There are three registers that control the DAC, with each register unique to a signal channel. "Implementing this compensation scheme helps improve the signal-to-noise ratio (SNR) in certain applications by 6 to 12 dB," Pinchback says. "As a result, the user does not loose the available input range because of undesired signals."

The chip is packed with more bells and whistles. The embedded logic of the MAX1400 enables the ADC to scan all signal inputs, and make the results available via the serial interface with a minimum of communications overhead. To indicate the source of each conversion, an identification tag is attached to the output word.

Many designs are migrating to higher frequencies to reduce the size of the passive components, which in turn lowers the cost of the system. Maxim has taken a similar approach. It has increased the frequency of the external crystal employed in such circuits. Unlike some utilizing 2.5 to 3.686 MHz, the MAX1400-03 can use crystals operating at 4.9152 MHz. Also, the MAX1400 provides access to the multiplexed output, thereby allowing the user to add a high-performance amplifier that can be shared by all the channels.

To isolate the channel inputs from the sampling capacitors, the MAX1400 series provides an option of using the data converter in the buffered mode. In this mode, the two matched buffers are switched in to buffer the channel inputs. Using the buffers eliminates the possibility of sampling related gain error at the expense of a small, 1 nA, input leakage current.

The primary difference between the MAX1400/01 and MAX1402/03 is the multiplexed outputs. The MAX1400/01 ADCs are architected to provide access to the multiplexed outputs. The series is available in 5 V and 3 V grades

PRICE AND AVAILABILITY

Initially, MAX1400 parts will be sampled this month with production planned for early third quarter. This will be followed by MAX1401/02/03 sequentially every six weeks. In 1000-piece quantities, the MAX1400 in 28-pin SSOP is priced at $9.50 each.

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The Latest Advances In Sensor-Based Systems And Applications, Are Highlighted At This Year's Sensors Expo.

Cheryl Ajluni

Each year, engineers from around the world come to the Sensors Expo Conference and Exposition to gain valuable, up-to-date information on the latest advances in sensor technology, sensor-based systems, and a myriad of innovative applications. This year will be no different. Scheduled for May 19-21, at the San Jose Convention Center, Calif., the show will feature over 250 exhibitors, 70 of which will be launching new products or services. There's also a stellar conference line-up, organized and moderated by some of the most experienced professionals in the sensor industry *(see the table)*.

With over 30 different product categories, including acoustic emissions, computer hardware, peripherals, and software; data acquisition systems; electrical/electronic components; fiber optics; infrared detectors; sensors networking; and signal conditioning, there's little doubt that this year's Sensors Expo offers something for everyone.

The show's conference portion features 26 information-packed sessions on a variety of topics ranging from all you need to know about sensor/control networking to packaging issues. Of particular interest is a session entitled "MEMS/MSTs/micromachines: A global perspective on applications and commercialization issues." It provides an overview of the MEMS/MST/micromachines market and examines current and future applications. The session will also cover technology trends and the development of the MEMS infrastructure. Other topics addressed include microfluidics, micropositioners, magnetic sensors, biosensors, chemical sensors, design automation, testing, manufacturing equipment, and infrared detectors.

For those engineers new to sensors or just looking to brush up on their skills, four conference sessions focus on the

SENSORS EXPO TECHNICAL PROGRAM

Date and time	Tutorials (ADT and HDT) and seminars (S)
Monday May 18 9:00 a.m. to 5:30 p.m.	**ADT1:** Modem communications systems for sensor, Parts I and II **ADT2:** Digital data acquisition and anaylsis **ADT3:** Capacitive and electric-field sensors: design and applications
Tuesday May 19 9:00 a.m. to 5:30 p.m.	**ADT4:** Transducer interfacingand signal conditioning **ADT5:** Smart sensors and smart sensor communication
9:00 to 11:30 a.m.	**HDT1:** Fiber-optic sensors; techniques and applications **HDT2:** Fundamentals of sensor technology: temperature
9:00 to 10:30 a.m.	**S1:** Understanding laser triangulation sensors **S2:** Innovations in hall-effect sensors
10:45 a.m. to 12:15 p.m.	**S3:** Chemical gas sensors for aeronautic and space applications **S4:** Microtechnology and instrumentation for biomedical analysis
3:00 to 5:30 p.m.	**HDT3:** Biochemical sensing: the science of miniaturization microfluidics **HDT4:** A new perspective on magnetic-field sensing **HDT5:** The Anderson loop: successor to the Wheatstone bridge
Wednesday May 20 9:00 a.m. to 5:30 p.m.	**ADT6:** MEMS/MST micromachines: A global perspective on applications and commercialization issues.
9:00 to 11:30 a.m.	**HDT6:** What you need to know about networking **HDT7:** Fundamentals of sensor technology: pressure **HDT8:** Sensors and sensor networks for safety and damage control
9:00 to 10:30 a.m.	**S5:** Advances in thermistor technology **S6:** High-precision, non-contact position measurement (with emphasis on Eddy current technology)
10:45 a.m. to 12:15 p.m.	**S7:** Gas detection systems for the semiconductor fab **S8:** The six-degree-of-freedom sensor: enabling manufacturing flexibility
3:00 to 4:15 p.m.	**S9:** Life work: reduction and career planning for engineers and scientists
3:00 to 4:30 p.m.	**S10:** Packaging of integrated circuits **S11:** NTC thermistors in biomedical applications
3:00 to 5:30 p.m.	**HDT9:** Fundamentals of sensor technology I: proximity and photoelectric sensors **HDT10:** Measurement and direction of humidity: methods and instructions
Thursday May 21 10:00 to 11:30 a.m.	**FR1:** Sensors magazine "wish list"—free to all attendees

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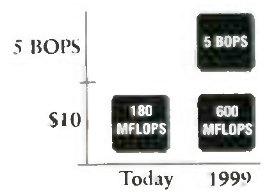

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fundamentals of pressure, presence sensing, transducers, and temperature. In, "Fundamentals of sensor technology: Pressure," engineers will learn about the basic physics of pressure, operating principles of pressure sensors, and selection criteria for the most common pressure-sensing applications. They will also gain information as to the types of pressure sensors available and any related advantages and disadvantages. Discussions in the session include definitions, terminology, and units specific to pressure measurement.

In "Fundamentals of sensor technology: Temperature," the session provides a broad understanding of the various issues surrounding temperature measurement and sensing, including basic operational information and applications.

"Fundamentals of sensor technology: Proximity and photoelectric sensors" offers insight into the basic operating principles and selection criteria for an assortment of presence-sensing technologies including inductive, capacitive, photoelectric, and magnetically actuated types. Of particular interest will be a discussion of the current trends in solid-state presence sensing, and information on software tools.

Similarly, "Transducer-interfacing and signal-conditioning fundamentals," explores the basics of different types of transducers including thermocouples, RTDs, strain gauges, photodiodes, and piezoelectrics. Also featured will be practical information on circuit techniques, application examples, and a look at recent developments in monolithic ICs.

There's no disputing the fact that sensor technology is quite dynamic. This is evidenced, at least in part, by the multitude of advances that have taken place in Hall-Effect and magnetic sensors, just since last year's Sensors Expo. All of the latest developments related to these sensors are highlighted in this year's conference program. Additionally, advances in thermistor technology, focusing on devices with negative- and positive-temperature coefficients, and high-precision, non-contact-position measurement technology are explored. In the latter, special emphasis is placed on eddy current technology. Focus here is on understanding the issues of measurement precision versus accuracy, a comparative review of various non-contacting measurement devices, considerations for applying analog technology and DSP error correction, and advantages and considerations for applying eddy current position-measurement devices.

Other sessions include "Understanding laser triangulation sensors" and "Digital data acquisition (DA) and analysis." The first session explains the fundamentals of laser sensors, with emphasis on the various terms used to specify accuracy, repeatability, resolution, and traceability. As the demand for laser-triangulation sensors—often used for dimensional inspection and process control—rises, the variety of lasers increases. This session will also clear up the confusion between the plurality of laser sensors now available, as well as give practical advice on how to choose the right laser sensor for a particular application.

A full-day session on "Smart sensors and smart sensor communication," is especially useful for the engineer looking to gain more information on trends and cutting-edge developments in smart sensor technology. The session covers networking for smart sensors, the IEEE 1451.2 smart sensor communication standard, the IEEE P1451 standard extensions under development, and first implementations of IEEE 1451. Additionally, it looks at a broad range of sensor technologies including sensors with built-in intelligence, single-chip silicon sensors with built-in electronics, and microelectronics for sensors. Of particular interest is the world's first commercial integrated pressure sensor with on-chip compatibility for fluids.

A session sure to draw a crowd is "Biochemical sensing: The science of miniaturization microfluidics." This session will examine the abundance of engineering tools available as applied to a microfluidic device test case. The tools included in this comparison are ultra-precision diamond machining, a variety of electrochemical machining techniques, electrodischarge machining (EDM), ion-beam milling, laser and e-beam machining, ultrasonic machining, bulk and surface silicon micromachining, and LIGA. The results of this comparison will better equip engineers to choose the right micromachining tools applicable to specific microengineering tasks.

Two other sessions will focus on a new type of sensor and circuit topology. The first, "The SixDOF sensor: Enabling manufacturing flexibility," offers a glimpse at Lawrence Livermore Na-

Sensor Offers Low-Differential-Pressure Measurement

The 267LCD pressure sensor and optional 3-1/2 digit LCD—designed to measure low differential pressure and flow—dramatically increases overall building operating efficiency. Because it's optimized for non-conducting gas and air compatibility, the sensor is ideal for maintaining proper building pressurization and air-flow control, environmental pollution control, and static duct and clean-room pressures, as well as for oven pressurization and medical instrumentation.

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The LCD, housed in a compact NEMA4/IP65 enclosure, features a high level 10-V dc analog output or 4-20 mA output that's compatible with all energy management systems. The 267LCD pressure sensor is NEMA 4/IP65 rated and complies with the European requirements of Council Directive 89/336/EEC.

Now available, the device comes with a 3/16-in. O.D. pressure fitting for 1/4-in. push-on tubing. Electrical connection is through a screw terminal strip with PG-9 or PG-13 cable strain relief. Price depends on the quantity of purchase. CA

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High-Speed Solid-State Vertical Gyro Now Available

A recently introduced high-speed solid-state vertical gyro offers both the speed and accuracy necessary to accurately measure roll and pitch in dynamic environments such as camera and antenna stabilization, artificial horizon applications, and automotive testing. Called DMU Turbo, it's based on a combination of silicon micromachined microelectromechanical systems (MEMS) technology and high-speed digital processing. As a result, the gyro offers a much more cost-effective and higher-reliability solution than its mechanical counterparts. In fact, the DMU Turbo has a reliability estimated at over 100,000 hours of mean time between failures (MTBF), while the MTBF of comparable mechanical sensors can be as low as 500 hours.

The DMU Turbo works by providing stabilized roll and pitch (artificial horizon) output with an instantaneous initial erection rate. Sophisticated software calculates instantaneous angle from the rate sensors, while accelerometers are used to correct for drift and provide a gravity reference. This results in functionality equivalent to the traditional mechanical gyro.

Specific features of this 10-Hz dc bandwidth device include a roll and pitch range of ±180° and 90° respectively, and operation over a temperature range of –40°to 85°C. It can withstand shock up to 1000 G. The DMU Turbo comes in either a custom package or standard 3 in. by 3.375 in. by 3.25 in. aluminum housing that weighs 475 grams. Available now, it sells for a single unit price of $4000. CA

Crossbow Technology Inc., *41 E. Daggett Dr., San Jose, CA 95134; (408) 324-4830; www.xbow.com.*
CIRCLE 526

tional Laboratory's six-degrees-of-freedom (DOF) sensor with special emphasis on the device's construction and potential for application. The second session, "The Anderson loop: Successor to the Wheatstone bridge," examines the development of the Anderson loop measurement circuit topology, a circuit that has been proven to outperform the Wheatstone bridge in many sensor applications. The session focuses on providing the engineer with hands-on experience with this new technology and explore some of its possible uses.

The more exciting portions of this year's conference program include the sessions related to specific applications. This is in part because developing a new sensor technology is one thing, but actually making it applicable to the real world is something else altogether. For example, fiber-optic sensors have gained much attention of late for having the potential to offer significant advantages over sensors based on conventional electrical and/or electromechanical technologies. But, because the fiber-optic sensor is being targeted at applications already occupied by the more conventional sensors, many engineers are faced with the question "why change?" Understanding the benefits and advantages of using fiber-optic sensors in such applications is crucial to making them real-world applicable. This information, as well the ways in which such sensors can be utilized in a variety of different applications is the subject of a session entitled, "Fiber-optic sensors: Techniques and applications."

In the area of biomedical applications, two sessions take center stage: "Microtechnology and instrumentation for biomedical analysis," and "NTC thermistors in biomedical applications." In the first session, the emphasis is on work in the area of microtechnology done at Lawrence Livermore National Laboratory, which focuses on photonics devices and bulk micromachining, including MEMS and associated areas. In particular, the session will highlight examples of microtechnology devices including portable polymerase chain reaction

LCD Compass Targeted For Automotive Use

A liquid-crystal-display (LCD) electronic compass module, called the Navifinder-200, is specifically designed for automotive use. Based on magneto-inductive (MI) magnetic sensor technology, the device offers a number of advantages over other comparable compass technologies, including having a high sensitivity, a large dynamic range, low power consumption and a low price.

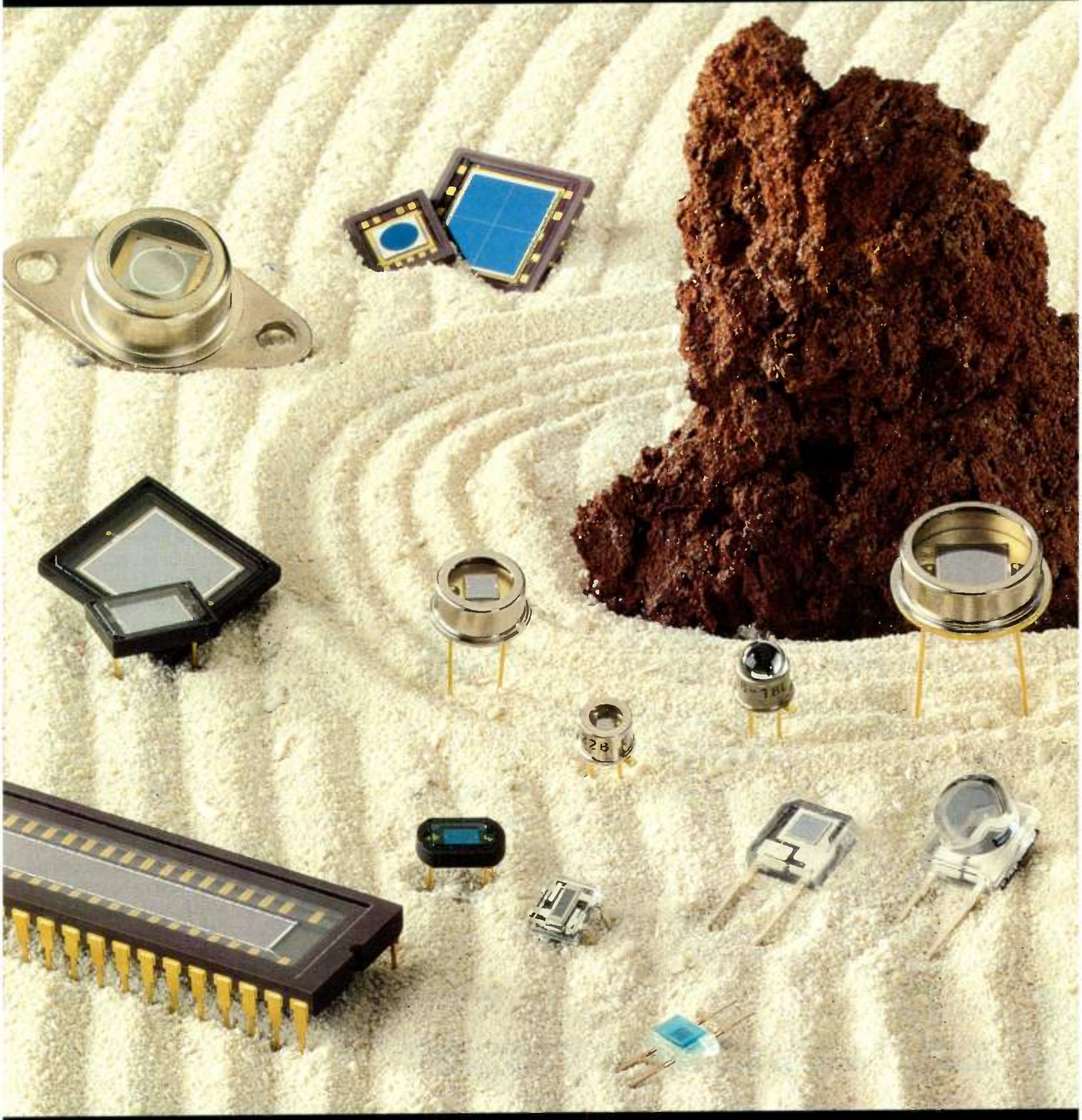
During operation it relies on advanced calibration algorithms to discriminate between the Earth's magnetic field and those generated externally, such as from the metal and electronics in a vehicle. By electronically compensating for these external factors, the Navifinder-200 can provide highly accurate compass readings in all vehicle environments.

Compared to the more conventional floating ball compass, the device is much easier to set up, taking less than two minutes to calibrate. It's also simpler to use, because it offers a continuous display of the exact heading.

The device, which has been optimized to offer high reliability and ruggedized features, can be powered by any 12-V battery supply and ignition system or externally mounted on/off switch and battery. It operates over a temperature range of ±10°C to 60°C. It outputs the compass heading on a LCD in 5° numeric digits and 8 cardinal points (N, NE, E, SE, etc.), with an accuracy of 2°. Different viewing angles can be achieved without any loss in accuracy by mounting the device with up to ±30° of tilt.

Designers now are working to add more features, such as an electroluminescent backlight, a variety of different LCDs, a vacuum fluorescent display (VFD), and sensors that register inside and outside temperatures. The Navifinder-200 compass, which can either be mounted on a dashboard or enclosed in a housing, is now available and sells as a single unit for $75. For OEMs, the 1000-unit price is $32. CA

Precision Navigation Inc., *1235 Pear Ave., Suite 111, Mountain View, CA 94043; (650) 962-8777; fax: (650) 962-8776; www.precisionnav.com.* **CIRCLE 527**



(PCR) thermal cyclers for DNA analysis, hand-held gas chromatographs, flow-stream-waveguide-based cytometers, and etched-microchannel electrophoresis systems. The second session examines some of the different types of commercially available NTC thermistors and their associated biomedical applications. Specific applications include thermodilution catheters, cardiac pacemakers, skin-surface sensors, oral/rectal fever thermometers, esophageal sensors, urinary catheters, and other patient-care sensors. Engineers will also be able to gain valuable insight into the future of biomedical thermometry and such future applications as disposable and reusable sensors.

Of particular interest, especially in light of all the recent earthquakes and El Nino-related storm damage, is a session entitled, "Sensors and sensor networks for safety and damage control." This session discusses details of an ongoing project sponsored by the U.S. Navy to provide emergency response personnel with pertinent information to guide them in their rescue efforts. Additionally, the state of the industry as it pertains to sensors and systems for emergencies involving earthquakes, gas, fire and smoke, and carbon monoxide, and where it needs to go in the future are on the agenda for that session.

Special emphasis will be placed on the development of safety valves which involve smart remote control systems and alarms that interface with other systems. Other topics to be discussed include technology needs, smart sensors and signature analysis, remote status and control telecommunications, coordination of disaster relief and utility repair efforts, and safety agencies' regulations and mandates.

Another session not to be overlooked is "Modern communications systems for sensor applications, Parts I and II." As the use of the Internet grows in acceptance and feasibility, it is inevitable that it will be utilized as a means for transporting sensor data. The question is how, and what do you need to know to make this an efficient and viable solution?

In Part I, "Delivery of sensor data: Wireless, optical, and network systems," the focus will be on understanding the concepts behind communication, such as bit error rates, coding, and signaling, and exploring the variety of high-speed services available today including ISDN, cable-modem systems, and low-speed embedded messaging using traditional over-the-air television signals. Part II, "How to establish an Internet-based sensing/control station," will take this discussion one step further by defining the method for setting up an automated web site. Special attention will be paid to the variety of components that must work together to accomplish this goal. These include a camera, video acquisition board, micro-computer, and software for image acquisition. Other topics will include setting your web server to accept Internet-issued commands and translating those commands to physical action.

If you're in a sensor-related industry, looking for the latest developements in sensor technology and products, or just trying to gain a greater appreciation of where the world of sensors if headed, the Sensors Expo is the place to be.

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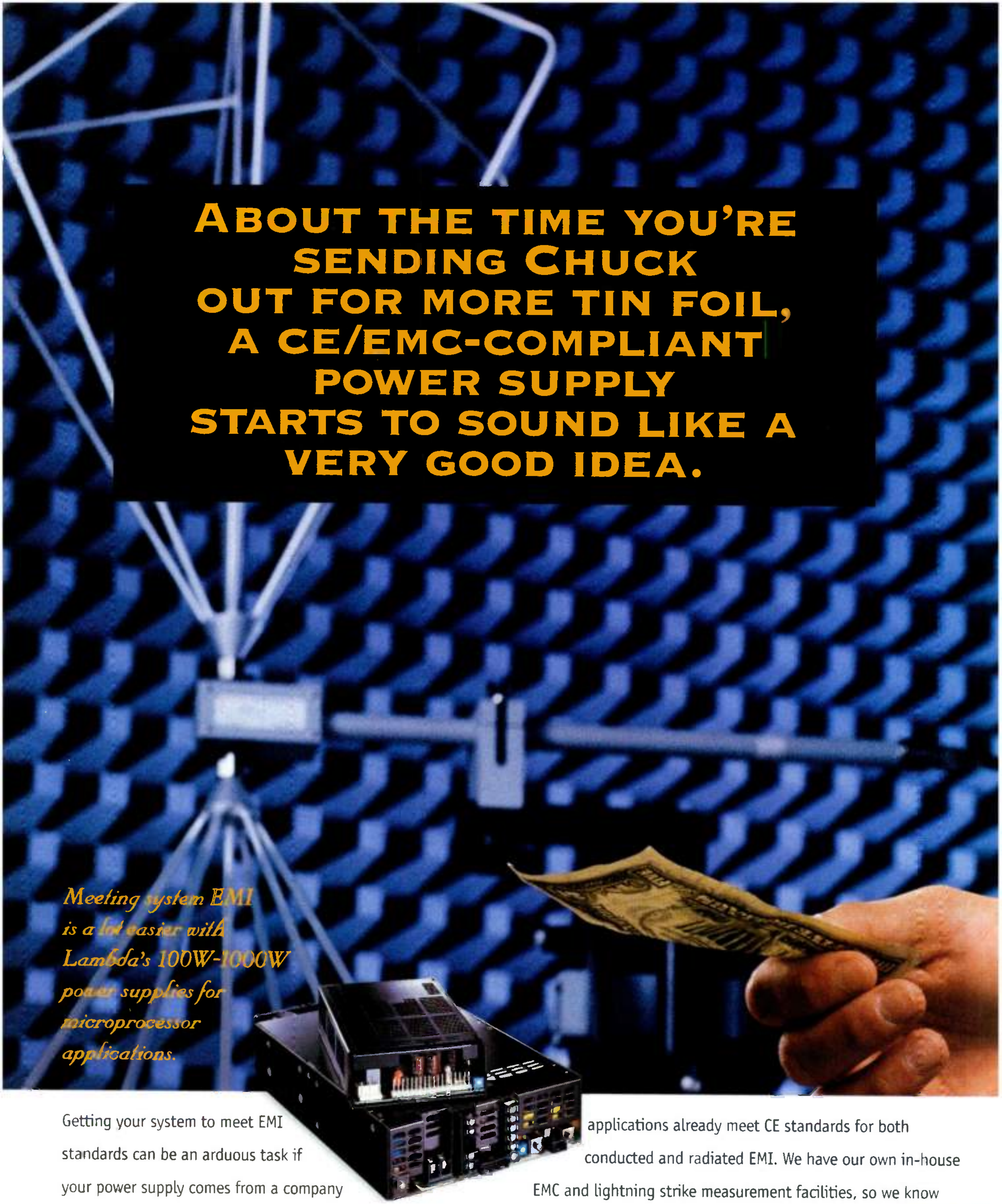

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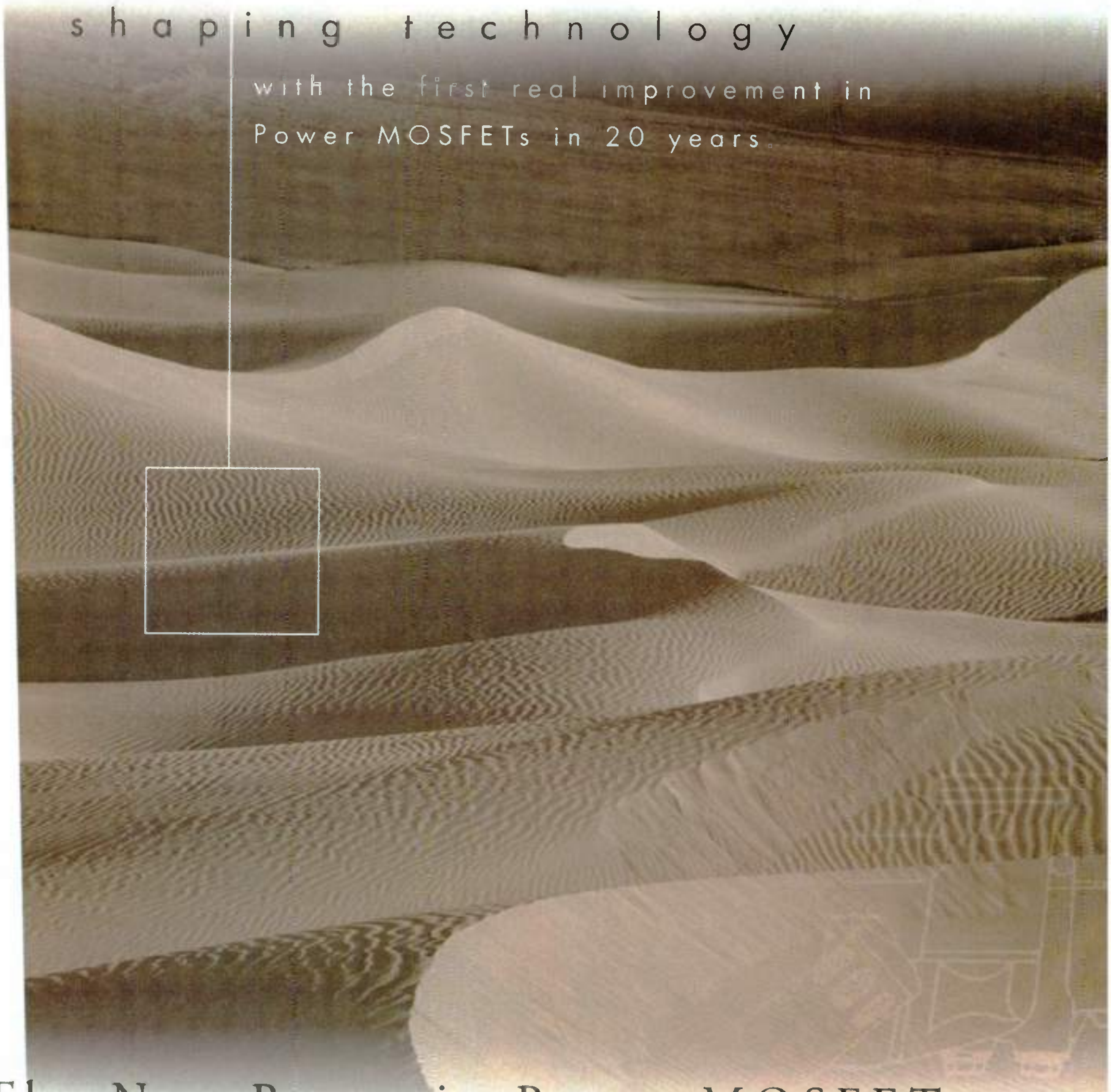

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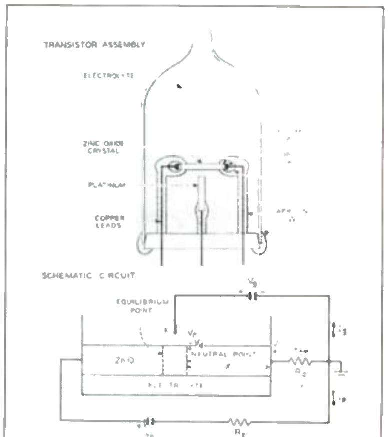
Transistor Uses Field Effect

A transistor amplifier using a semiconductor electrolyte interface modulated by an electrical field is being developed at Bell Telephone Labs. Experiments have demonstrated amplifier operation at 1000 cps, with gain in excess of 15 db. The experimental device uses a hexagonal, rod-like crystal of very pure zinc oxide as the semiconductor, immersed in a highly conducting electrolyte. A platinum electrode placed nearby serves as the grid element. Because zinc oxide is a large-energy-gap semiconductor, it can be operated in a high-enrichment condition, with one end of the crystal negatively biased with respect to the solution, and the other end positively biased. In between is a neutral point where the energy bands are flat right up to the surface of the crystal. As this neutral point shifts back and forth under the influence of varying biasing grid voltages, the resistance of the crystal changes, passing a current which follows the driving frequency closely. A fairly extended range of linear response is obtained, the Labs report.



Cross-section view of field effect transistor amplifier, with schematic circuit diagram showing principle of operation

To make electrical contact to the zinc-oxide crystal, the two ends are first indium plated to assure good ohmic contact. They are then copper plated to allow soldering of copper wire leads. The platinum grid completes the assembly. After insulating all wires and connections except the grid, the assembly is immersed in the electrolyte (5% sodium tetraborate and boric acid solution), and hermetically sealed in a small glass tube to avoid electrolyte evaporation.

Small size is required to give high-frequency operation. The smallest units constructed so far use crystals about 0.3 mm long, and 0.15 mm in diameter. It is expected that by going to a flat-plate crystal instead of the rod geometry, the present low output power levels could be raised appreciably, without any overall increase in size, or any change in other operating characteristics. *(ELECTRONIC DESIGN, May 14, 1958, p. 5)*

It's difficult to believe that this device, with its liquid electrolyte, was anything more than an experimental vehicle for the study of semiconductors. In the late '50s, there was still much to learn about transistors, and Bell Labs, with its commitment to pursue a broad range of investigations, was arguably the leading developer of basic semiconductor technology.—Steve Scrupski

From The E-Mail Bag (Back To The Present For A Moment)

My comments on J. Presper Eckert and John W. Mauchly as having "developed the first electronic digital computer" in the January 26 issue's "40 Years Ago" column brought some strong responses from readers. Rodney Steffen, Boca Research Inc., Don Everhart, Wells Mfg. Corp., and Erik Henderson all pointed out that the honor belongs to John Vincent Atanaosoff and Clifford Berry, who constructed the first electronic digital computer at Iowa State College, in the 1939-1942 time period.

In the February 23 issue, we reproduced an article on a transistorized TV set, which used a 20,000-V supply derived by stepping up 12 V ac to 2500 V, and then quadrupling it. Noting the 10,000-V discrepancy, Cliff Bruhn wondered "Have they changed to a new modern mathematics again?" This is one I can't answer—the original article was quoted correctly. Does anyone out there have any ideas on how to resolve the discrepancy—which part of the statement is more likely to be wrong or incomplete?—Steve Scrupski

Steve Scrupski is a former Editor-in-Chief of ELECTRONIC DESIGN. Now semi-retired, he can be reached at scrupski@worldnet.att.net.

Hot Jobs

It's time once again for the results of the Christian & Timbers' "1998 Report on Hot Jobs and Not-So-Hot Jobs." One of the fastest-growing retained executive search firms in the U.S., Christian & Timbers has access to a large number of professionals in a variety of fields. According to president Jeffrey Christian, Hot Jobs are those that show the greatest growth in demand and compensation. The converse goes for Not-So-Hot Jobs.

Christian & Timbers derived their results from a year's worth of personal and telephone interviews, client surveys, and statistics from a variety of sources.

The good news first—the top 13 Hot Jobs are (including predicted growth):

1. Brand-name Chief Executive Officer (300%)
2. Chief Financial Officer (227%)
3. Vice President of Electronic Commerce (210%)
4. Principals and Senior Managers within Consulting/System Integration (205%)
5. Chief Information Officer (179%)
6. Vice President of Development (Internet Company) (163%)
7. Vice President of Supply Chain Management (154%)
8. Vice President of Outsourcing (133%)
9. U.S. Financial Institutions Portfolio Manager (127%)
10. Chief Executive Officer (traditional IT company) (104%)
11. Vice President of Healthcare Information Protection (93%)
12. Vice President of Firewall and Security (87%)
13. Focus Factory Manager (71%)

On the Not-So-Hot side, it looks pretty bad for bank presidents, stock brokers, vice presidents of corporate environmental affairs, and all flavors of middle managers.

For more information or a copy of the complete report, contact Christian & Timbers, One Corporate Exchange, 25825 Science Park Dr., Suite 400, Cleveland, OH 44122; (216) 464-8710; fax (216) 464-6160; www.ctnet.com.—**DS**

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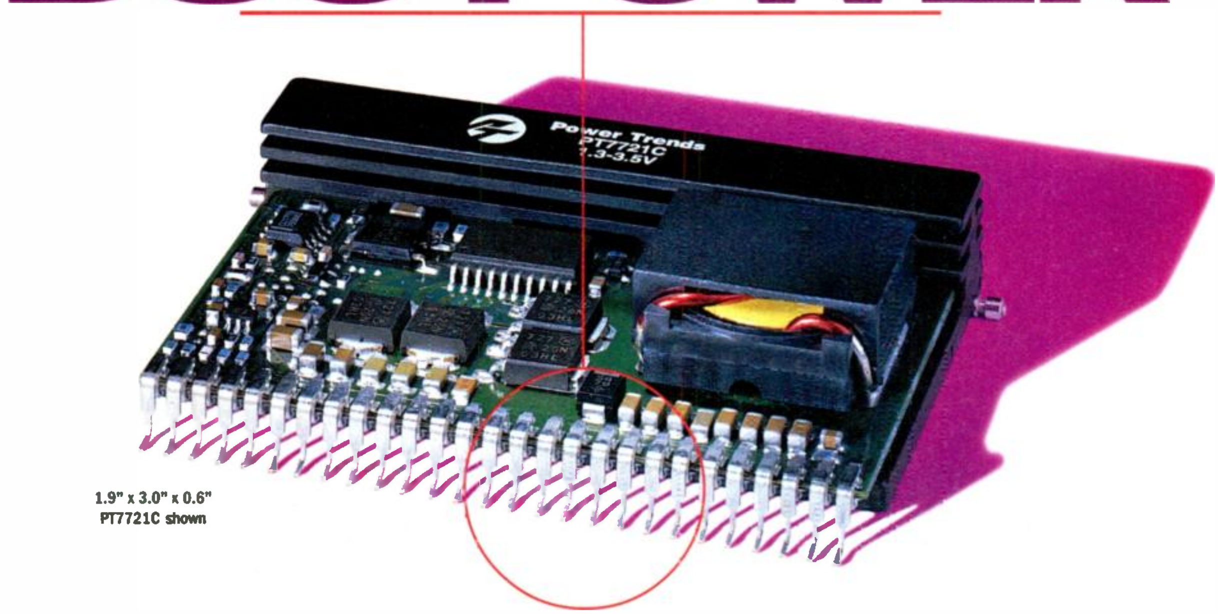

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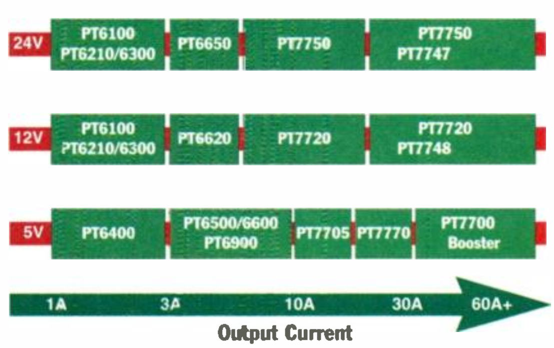

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LOGIC PRODUCTS

TEXAS INSTRUMENTS

New Program Helps OEMs Get SMART

Ever wonder why most stores have seemingly incredible sales promising big percentages off of every item in the store? While you may think that retailers are being kind to their customers by charging less for their goods, it's really because they have excess inventory that they must move, and they want to recoup some of their financial investment instead of taking a big loss on unsold goods.

The same theory applies to the purchasing and materials management teams of most high-tech manufacturers. To combat this problem, GC Management's Surplus Materials Asset Recovery Team (SMART) provides a reliable method for OEMs seeking to reduce surplus inventory levels while maximizing the financial recovery of their materials investments.

This is accomplished in a confidential and secure environment whereby GC Management and the OEM enter into a Bonded Consignment program. GC Management acts as the sole sales agent for the OEM's surplus materials inventory.

The SMART team analyzes the inventory and provides a fair market value for all resalable materials. The materials are classified as either High Demand, Marketable, or Non-Marketable Materials based on current market value assessment. High Demand and Marketable materials are delivered to GC Management's warehousing facilities. If materials are deemed as Non-Marketable, they are then recommended for scrapping by either GC Management or the OEM.

The materials are then marketed and sold by GC Management, who receives a previously agreed upon percentage for all goods sold. Of course, GC Management will make every attempt to achieve the highest possible return on each transaction.

The OEM's public exposure from the transaction is always minimized due to GC Management's strict policy of confidentiality in remarketing the surplus materials.

The OEM benefits by receiving a substantially higher rate of return on the inventory than if it had been disposed via their traditional liquidation processes.

"We created the SMART program because surplus inventories are the bane of even the most efficient purchasing and materials management teams. No amount of foresight can predict materials needs to a degree that eliminates the eventual occurrence of excess inventory materials," explained Gary B. Munoz, president and CEO of GC Management. "In fact, the rapid pace of technology turnover and the resulting shortened product life cycles inevitably produce both shortage and excess conditions, which can be rectified with GC Management's SMART program."

For more information, contact GC Management, 991 Calle Amanacer, San Clemente, CA 92673; (714) 361-8800; www.gcman.com.—**MS**

FLIPPING THROUGH THE INTERNET ROLODEX

www.motorola.com/semi/otp: This portion of Motorola's web site is now an interactive area focused on the company's one-time-programmable (OTP) 68HC05 8-bit microcontrollers. Seven devices, including the very-low-cost 68HC705KJ1, are at the site, with reduced prices. Here, engineers can find technical documentation, downloadable software, and OTPs and development tools to order (from authorized distributors). The family of OTP parts offer a wide range of pin counts and complement Motorola's line of MCUs.

www.rfglobalnet.com/hp-rfsemi: Point your browser here for Hewlett-Packard's newest version of its electronic product-selection guide and information database. This portion of the RF Globalnet site includes HP's entire line of RF and microwave semiconductor products. Navigating through the guide, users can delve into particular markets such as IS-95 CDMA or 802.11 wireless data. The site features links to user groups and standards bodies. PDFs of individual data sheets, application notes, or reliability information are ready for downloading here. Spice models, s-parameter data, an MDS model library, a reference glossary, and an acronym library hold much design information at the site. RF Globalnet is a site developed and owned by Mircrowave Online Services. RF Globalnet itself hosts expert discussions, technical publications, industry activities, online educational and career opportunities, and engineering texts.

www.arcglobal.com: ARC Global Technologies, the Polymac keypad manufacturer, now showcases its product literature and design guides, FAQs for design engineers, and links at its new corporate web site. Products found at the site include PermaGraph, an in-mold graphics system; and the IMD Lens, a molded, optic cover.

www.pentek.com: Engineering system designers can click here for Pentek's Knowledgebase site. The newest expansion at the Pentek site features a technical support database, with up-to-date product information for the company's entire line. FAQs, product bulletins, tips and techniques, product compatibility, and the gamut of technical documents are at the site. Tutorials and applications at Pentek's site are available for use. Tutorials highlight such new technologies as digital receivers, while applications focus on successful implementation ideas for a wide range of systems. Pentek manufacturers and markets DSP systems to OEMs, distributors, and value-added resellers.

Raising The Bar For BIST Technology

The new book, "Arithmetic Built-In Self Test For Embedded Systems," by Janusz Rajski and Jerzy Tyszer, lays the foundation for a new way to develop the built-in self tests used in today's most complex ICs. The book is based on the results of research in arithmetic built-in self test (ABIST). Some of these results have have been presented in IEEE publications.

Tyszer and Rajski first bring us up to date on the current state of design-for-test (DFT) and built-in-self-test (BIST) techniques, and explain why these are inadequate. The authors then present what they call "an approach fundamentally different than from the (test) solutions introduced so far."

The jist of ABIST is its use of the computational potential of modern DSP cores and embedded processors. The 268-page book points out the fact that "although the vastness of data-path architectures consist of powerful building blocks such as adders, multipliers, or arithmetic and logic units (ALUs) offering a very high computational potential, existing data-path BIST schemes are unfortunate examples of having sophisticated modules on the chip, but remaining unable to translate this advantage into efficient nonintrusive testing schemes."

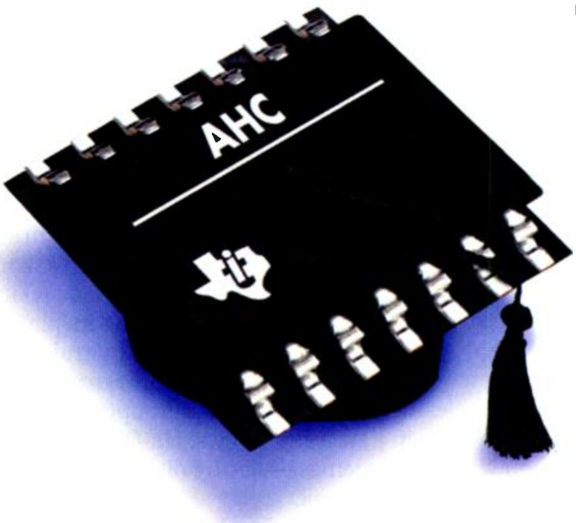
Once the authors lay the groundwork for the existence of ABIST, they proceed to explain how one might bring this new methodology to fruition. Tyszer, a chief scientist and DFT Research manager at Mentor Graphics, Wilsonville, Ore., and Rajki, a professor at the University of Technology in Poland, Poznan, make use of assembly language programs, 2-dimensional and 3-dimensional graphs, charts, schematics, Markov chains, and mathematical formulas to make their point.

After presenting the methodology, "Arithmetic Built-In Self Test For Embedded Systems" spends a chapter detailing several case studies that highlight the ABIST approach. A rich, 14-page bibliography of books and articles on BIST technology rounds out the book, which retails for $70.

The authors do a fine job of presenting the current state of research on ABIST, and showing how it can be applied in real-world situations. The book is not for casual readers, though; it demands a solid background in low-level programming, mathematics, and digital logic design principles. But if you want to stay on the cutting edge of BIST testing technology, this book should provide you with that knowledge.

For more information on "Arithmetic Built-In Self Test For Embedded Systems," ISBN 0-13-756438-4, contact Prentice Hall at their web site: www.prenhall.com/divisions/ptr. The book also is available at Amazon.com.

Joseph Desposito



MANAGING THE DESIGN FACTORY

Give Me Control

You can probably identify with these comments: "My project is always waiting on parts," "We never have adequate priority," and "We could be successful if we had control of the prototype shop." They're common complaints. Project managers everywhere insist that their destiny is outside of their control because they are held hostage by support groups.

The psychological consequences of this are damaging. Psychologists say that the less people perceive themselves to be in control of a situation, the less control they will take. Lack of control feeds on itself, and consequently creates a victim mentality—which is the *last* thing that we want on development teams.

DON REINERTSEN

We want these teams to take charge of their own destinies. However, let's take some caution with this thinking. Does their perceived lack of control really require giving the team the run of the prototype shop? Surely, a centralized shop would have more resources and be able to be more flexible at supporting project teams. Is decentralizing the prototype resource the only solution?

To crack this problem, we must ask why the team wants to control the prototype shop. If the reason behind it is that their project never has adequate priority, they must control the resource to control its priorities. But why do projects need a high priority anyway? Because without priority you must wait for resources. But why do low priority jobs wait for resources? Quite simply, because we have allowed queues to develop in our process.

The request for control is always a symptom of something larger. The desire to run support groups is almost never based on a true need for control. Usually, it arises because support groups are not being responsive to project teams. For example, why don't teams ever ask to manage their own payroll? Is it because payroll is not important? No, teams don't want to get into dealing with payroll because payroll does what it is supposed to do. If the prototype shop functioned the way it was supposed to function, teams would not be requesting to control it.

Now, at a deeper level, we must ask why the prototype shop is letting the teams down. Does the shop manager have a perverse desire to undermine the company? Not very likely. It is much more probable that the shop is being measured with the wrong metrics. Prototype shops are often assigned to manufacturing and measured on efficiency.

Manufacturing knows how to be efficient. They build a solid backlog, run similar parts at the same time, and minimize expensive overtime. All such approaches lead to efficiency—and poor response time.

A better approach is to find out what users mean by good support. If response time is more important than efficiency, you must align the metrics to encourage response time. Start measuring the prototype shop on how long it spends on the critical path of the project. Then, the prototype shop will start trying to stay off the critical path.

By using that technique, you won't have to hear them boasting about how they've cut the cost of making prototype parts while Engineering moans about how long it takes to get them. Remember, a request for control is usually a sign that someone is not doing their job the way you want them to. It is usually smarter to change the way a support group is measured than it is to take on the responsibility to manage it on a daily basis.

Don Reinertsen is president of Reinertsen & Associates, a consulting firm specializing in product development management. He can be reached at (310) 373-5332 or e-mail: DonReinertsen@compuserve.com.

Y2K UPDATE

About a year ago, we saw some of the merchandising associated with the Year 2000 Date Change (Y2K) dilemma. Well, this year it's a "text adventure game." The game is called "Uh-Oh!" and it brings the computer problem right to your own monitor.

The game begins in 1998. Your character works in an office where the Awareness phase is just beginning (a bit late for a successful compliance program, but since it's a game, we'll give it license). The object here is to convince your superiors that the Y2K problem is a reality Within the game are quotes from well-known corporate leaders, bankers, politicians, and programmers who talk about how awful it could get if compliance doesn't happen.

Next comes the Preparation phase of the game which takes place in (gasp!) a shopping mall. Here, in 1999, you have to load up on all the supplies you'll need when everything goes black. The game gives you a debit card, so it's really an exercise in budgeting, creativity, and practicality. Think gearing up for Armageddon.

Finally, the game takes you to the Survival phase, which consists of making it through the crisis while roughing it in a rural environment.

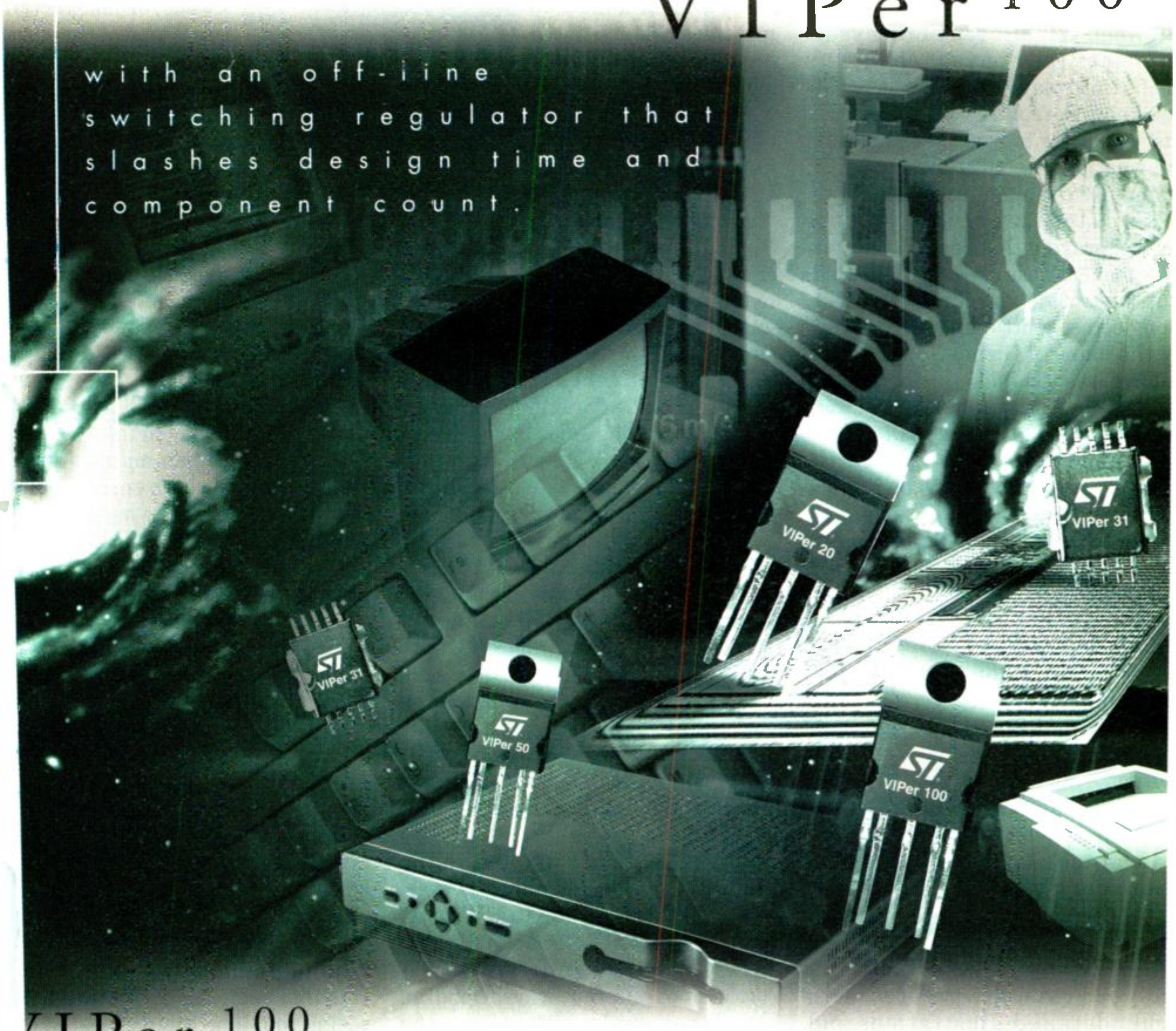
Scott Covert, the game's creator, had a problem with a lot of the computer games that were available during the 1980s, because they couldn't be solved. These games often carried price tags of $30 or more, plus the $10 you could dish out if you wanted the hint books (a cop out, if you ask me).

This game has a solution and uses a "Hints" system to bring its players to the answers. The full version of the game includes a Y2K Survival Guide, game maps, instant upgrades, and future game news. Uh-Oh! costs $10, and comes either by diskette or via secure e-mail.

Additionally, a trial version may be downloaded from Covert's web site: www.successinformation.com/game.htm. The game works on Mac, PC, and other systems.

To order by mail or phone, contact Scott Covert, R.R. #8, 1956 O'Brien Rd., Peterborough, Ontario, Canada K9J 6X9; (705) 742-9458.—**DS** shaping technology

VIPer 100™



VIPer 100

Thanks to ST VIPer100 (Vertical Integrated Power energy regulator) technology, SMPS designs are really shaping up. By combining an optimized, high voltage, avalanche rugged Vertical Power MOSFET with state-of-the-art PWM circuitry, VIPer100 family devices simplify and streamline AC to DC conversion — and actually cut component count in half. Printers, digital satellite receivers, auxiliary power supplies and more can now get to market faster and more economically. So why not let ST VIPer100 devices help you shape technology? For comprehensive literature plus information on interactive application design software and low-cost development kits, fax 781-259-9442 and visit us on the web at www.st.com.

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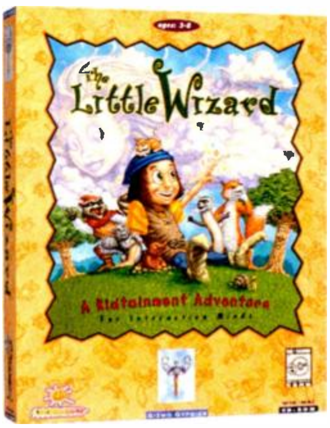
READER SERVICE 159

JUST 4 THE KIDS

Be honest. Aren't there times when you just can't bring yourself to read to your child? It's been a long day, you're tired, etc.—you know the routine. Or, maybe you just can't bear to hear how "Jack and Jill went up the hill to fetch a pail of water" for the billionth time.

Let's face it, we've all been there before, praying that Jack would take a permanent nose dive down that hill. But, just when you think all is lost, along comes a little-known company by the name of Gizmo Gypsies Inc., Santa Clara, Calif.

Gizmo Gypsies is offering an interactive-adventure-story-filled CD-ROM and DVD called "The Little Wizard." It's ideal for anyone looking for an educational, yet entertaining option to reading a book. And, it's a fun way to introduce your child to the computer.



Developed by an expert team of conceptual artists, musicians, animators, 3D modeling and interactive game developers, and programmers, "The Little Wizard," is targeted at children ages three to eight. Upon entering into the world of the Little Wizard, you and your child are greeted with richly detailed illustrations and brightly colored graphics. You join along as he and his forest friends journey to strange and mystical lands such as wild-and-crazy Bugville, Slo-Mo Junction, and nutty Normal Town, in search of someone who may have special powers like his own.

A number of games interspersed throughout the series of adventure stories allow your child to build skills such as pattern recognition, basic math, construction, and color mixing. In the Cave Game, for example, the child is asked to match colors and solve basic math problems. The Eartail Forest game calls on your child to use the mouse and keyboard to help the Little Wizard create music or add sounds. In Slo-Mo Junction, the child follows a blueprint to build different things with blocks. Other games found in the Little Wizard adventure stories include The Snoring Game and The Snoozing Juice Bar.

"The Little Wizard" uses advanced technologies like random embedded animation, and lip-synched character voices to totally immerse the child in the adventure stories. Interactive music and 3D characters add to this experience. And, with the ability to depict simultaneous multiple events, "The Little Wizard's" cast of characters are able to react not only to the child, but to the surroundings as well.

"The Little Wizard" CD-ROM/DVD can be utilized in an assortment of different ways. Children can, for example, either have the story read to them, read it on their own, or have it read to them scene by scene. In these ways, they can interact with each scene. They also have the ability to review any one of 22 scenes, or fast-forwa.. to any one of the scenes by using a special Pick-A-Scene option.

MARIFRANCES WILLIAMS

A special start/stop narration feature allows the child to interrupt the story or click on text so that sequences of words can be read back. In addition, children have access to special tools to create and listen to music as they interact wi' the CD-ROM.

While this is certainly not t first interactive animated story the market for children, it is uniq in that it offers a true hands-on mı tidimensional learning capability that evolves with the child. This is possible thanks to a built-in update feature that uses the World Wide Web to access and load the latest story updates.

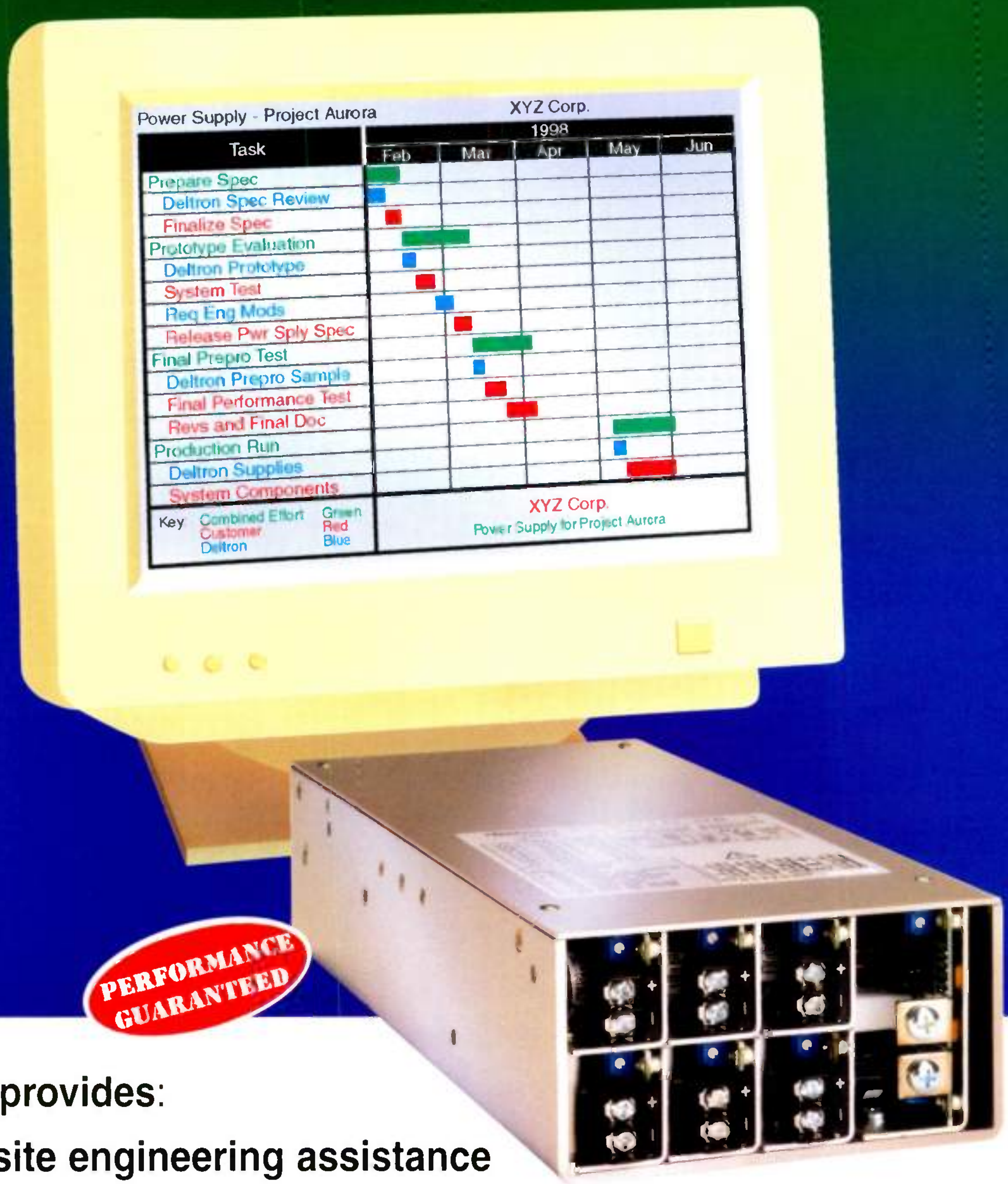
Such updated information might include the introduction of new characters, more music, and the addition of greater complexities to the games. As a result, once the child masters certain skills, he or she can be immediately introduced to new situatio and more difficult game levels tl will again challenge them to lea something new. And, for the pare reading along with their childr this means no more getting bor seeing the same thing repeated o and over again.

"The Little Wizard" CD-ROM . priced at $29.95, and is now available at a variety of retail stores. It also can be purchased via the company's web site listed below.

For more information, contact Gizmo Gypsies Inc., 990 Linden Dr., Suite 201 Santa Clara, CA 95050; (408) 248-9151; www.gizmogypsies.com.

Marifrances D. Williams holds a degree in Liberal Studies from San Diego State University, Calif. She is currently a 5th-grade teacher at Los Ranchos Elementary, San Luis Obispo, Calif. Williams specializes in the identification of advanced tech nology for the use of child-focused c plications. She may be reached . williamsofsm@lightspeed.net

We partner with you to get the job done right and on-time.



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- Prototypes in two weeks
- J.I.T. delivery

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Deltron inc.
POWER PRODUCTS

F Series Power Supplies
0.99 Power Factor

- 1,000,000 + Models
- 400-1000W
- 1 - 7 Outputs
- Ultra Compact Size

FT • FS SERIES MODUFLEX ® SWITCHERS

DESCRIPTION

The FT and FS Series are comprehensive lines of ultra compact power factor corrected models derived from our Moduflex® family of switching power supplies. This series utilizes advanced technology to produce a high quality input current wave form that is compliant to the harmonic requirements of EN61000-3-2. Based on modular construction, "off the shelf" modules permit high volume manufacturing with an outstanding quality level assuring timely delivery at a competitive cost.

Three classes of output modules are available. The **STANDARD** outputs allow short duration surge currents on all auxiliaries for hard starting loads. Optional **CURRENT LIMITED** outputs have square current limiting and feature wireless droop current sharing. Optional **ENHANCED** outputs have square current limiting, one wire star point current share, output good logic signal with LED, nominal 5V local bias, individual inhibit and margining. For requirements that cannot provide minimum load on the main output, the **ZERO PRELOAD** option is available for main outputs up to 500 watts.

DELIVERY

Choose stocked units or construct a model number using stocked modules for fast delivery. Otherwise, form a model from the adjacent page to meet your specific requirements. Contact factory for deliveries on models derived from non-stocked modules.

FEATURES

- 0.99 power factor.
- 5.5 watts per cubic inch.
- 1-7 outputs, 400-1000 watts.
- 120 kilohertz MOSFET design.
- Universal input.
- UL, CSA, TÜV (IEC, EN), CE.
- FCC, EN Class A EMI.
- IEC, EN Immunity.
- All outputs:
  - *Adjustable*
  - *Fully regulated*
  - *Floating*
  - *Overload and short circuit protected*
  - *Overvoltage protected*
- Standard features include:
  - *System inhibit*
  - *Fan output*
- Options and accessories include:
  - *Power fail monitor*
  - *Redundancy*
  - *Current Limited Outputs*
  - *Enhanced Outputs*
  - *Zero Preload*
  - *End fan cover*
  - *Top fan cover*
  - *Rack Assemblies*

STOCKED MODELS - Available in 3 days.

Max Power	Output 1	Output 2	Output 3	Output 4	Model*
400W	5V @ 50A	12V @ 12A	12V @ 12A	5V @ 10A	FT46A2332-45P
400W	5V @ 50A	12V @ 12A	24V @ 6A	12V @ 6A	FT46A2363-45P
600W	5V @ 60A	12V @ 12A	12V @ 12A	5V @ 10A	FT46C2332-13P
600W	5V @ 60A	12V @ 12A	24V @ 6A	12V @ 6A	FT46C2363-13P

**400W models include power fail monitor, current limited modules, zero preload and end fan cover options. 600W models include the same options except fan cooling is built into the unit.*

UNITS FROM STOCKED MODULES - Available in 2 weeks.

FT 44 B 2 3 3 6 - YY X

- FT — Series
- 44 — Configuration
- B — Power Code
- 2 — Output #1 Code
- 3 — Output #2 Code
- 3 — Output #3 Code
- 6 — Output #4 Code
- YY — Sum of Option Codes
- X — Output #1 Variant

Configuration: Allowable quad output configurations are 42, 44, 46 and 48.

Power Code: Choose Power Code A through D for 400-750W models.

Output Codes: Select any outputs from the shaded area on the Output Types table consistent with the configuration chosen.

Option Code: Specify Option Code. Refer to the Option table. Codes 02 (redundancy) and 16 (enhanced) are excluded from models available in 2 weeks. Fan cooling is built into 600 and 750W units.

OPTIONS

Option Code	Function
00	None
01	Power Fail Monitor
02	Redundancy
04	Current Limited
08	Zero Preload
16	Enhanced
32	End Fan Cover
64	Top Fan Cover

Replace the YY with the sum of the Option Codes.

MODEL SELECTION

Models are available in power ratings of 400 to 1000 watts, with corresponding code letters A through E. See Power Code chart.

Output modules are available in six types: J, K, L, M, N and P in nominal power ratings from 75 - 500 watts. Type M, N and P modules are variable power rated depending upon the unit power rating. The M, N and P Module table directly below shows the corresponding multiplier applicable to the output current ratings of the M modules and allowable power ratings for the N and P modules. For example, a 750 watt multiple will have its M type module configured to produce 120A @ 5V or 12A @ 48V. The voltage and current rating of output modules are listed in the table of output types. This table assigns an alpha-numeric code designating the nominal voltage rating of the module.

Power Code	Unit Power Rating	M Module Current Multiplier		N/P Module*
		Single Output	Multiple Output	Allowable Power Rating
A	400W	0.8	0.5	250W
B	500W	1.0	0.6	300W
C	600W	1.2	0.8	400W
D	750W	1.5	1.2	500W
E	1000W	2.0	1.5	750W

**When an N or P module is used as the main output, the allowable power and the module current ratings must not be exceeded.*

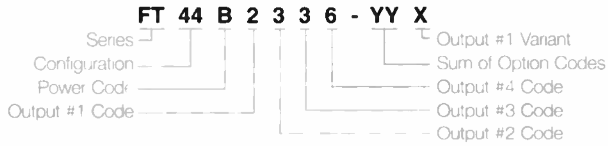
Output Types*						
Output		Module Type				
Code	Volts	J Amps	K Amps	L Amps	M Amps	N/P Amps
0	2	10	20	30	100	60
1	3.3	10	20	30	100	60
2	5	10	20	30	100	60
3	12	6	12	24	42	42
4	15	5	10	20	33	33
5	18	4	8	16	28	28
6	24	3	6	12	21	21
7	28	2.5	5	10	18	18
8	36	2	4	8	14	14
9	48	1.5	3	6	10	10
A	2.2	10	20	30	100	60
B	2.4	10	20	30	100	60
C	2.7	10	20	30	100	60
D	3	10	20	30	100	60
E	3.6	10	20	30	100	60
F	4	10	20	30	100	60
G	4.5	10	20	30	100	60
H	5.7	10	20	30	90	60
J	6.3	10	20	30	80	60
K	7	9	18	30	70	60
L	8	8	16	30	62	60
M	9	8	15	30	56	56
N	10	7	14	30	50	50
P	11	7	13	27	45	45
Q	13.5	6	11	22	37	37
R	17	5	9	18	30	30
S	19	4	8	16	26	26
T	21	4	7	14	24	24
U	23	4	7	13	22	22
V	26	3	6	12	19	19
W	29	3	5	10	17	17
X	32	2	5	9	16	16
Y	40	2	4	8	13	13
Z	44	2	4	7	12	12

Multiple output modules of a given type are arranged in ascending order by voltage magnitude in the same sense as the output number sequence in the configuration diagrams.
**Shaded ratings are stock.*

HOW TO ORDER

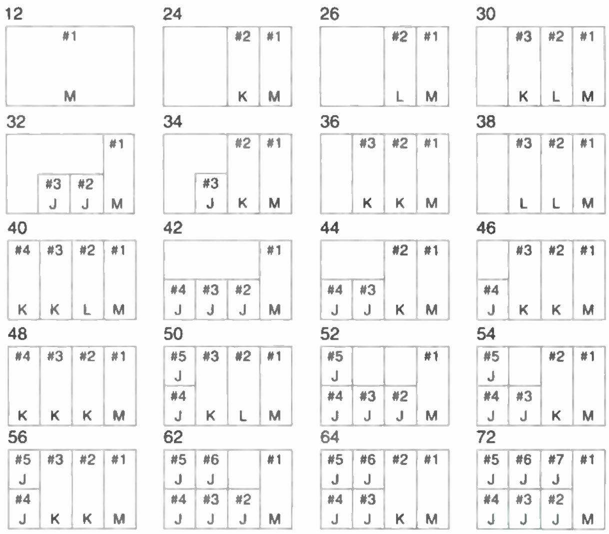
To form the proper model number defining a custom requirement, select the letters FS or FT to designate the series, then choose the desired configuration and list the configuration code. Insert the power code letter for the power level and follow with the output code numbers or letters for each specific output. Enter a dash and from the option table insert the sum of the option codes. Where lower power is desired for the main module, an N module can be substituted and is denoted by a letter N in the output variant position. In addition, when no preload is available for the main output, choose Option Code 08 and add a P in the output variant position. For an enhanced **main** and **current** limited auxiliaries, specify both 04 and 16 option codes.

HARMONIC CORRECTED 500W QUAD SWITCHER



OUTPUT CONFIGURATIONS

The boxes below are diagrammatic representations of the power supplies as viewed from the output end. The two-digit numbers above the boxes are the configuration codes.



Refer to the table below for allowable configurations by series.

Output Config	Unit Power Rating				
	400W	500W	600W	750W	1000W
12	•	•	• x	• x	x
24	•			• x	
26		•	• x	• x	x
30					x
32	•			• x	
34	•	•	• x	• x	
36	•	•	• x	• x	x
38					x
40					x
42	•	•	• x	• x	
44	•	•	• x	• x	x
46		•	• x	• x	x
48			x		x
50					x
52	•	•	• x	• x	x
54		•	• x	• x	x
56			x		x
62		•	• x	• x	x
64			x		x
72			x		x

• Represents allowable configurations for the FT Series.
x Represents allowable configurations for the FS Series.

SPECIFICATIONS

INPUT
90-264 VAC, 47-63 Hz.

POWER FACTOR
0.99 typical.

EMISSIONS
FCC 20780 Part 15/EN 55022, Class A Conducted. EN 61000-3-2, Harmonics. EN 61000-3-3, Voltage Fluctuations.

IMMUNITY
IEC 1000-4-2/EN 61000-4-2, Electrostatic Discharge. IEC 1000-4-3/EN 61000-4-3, Radiated Field. IEC 1000-4-4/EN 61000-4-4, Electrical Fast Transients. IEC 1000-4-5/EN 61000-4-5, Level 3 Surge. IEC 1000-4-6/EN 61000-4-6, Conducted Field.

INPUT SURGE
230 VAC - 38 amps max. 115 VAC - 19 amps max.

EFFICIENCY
75% typical.

HOLDUP TIME
20 milliseconds from loss of AC power.

OUTPUTS
See model selection table. Outputs are trim adjustable ±5%.

OUTPUT POLARITY
All outputs are floating from chassis and each other and can be referenced to each other or ground as required.

LINE REGULATION
Less than ±0.1% or ±5mV for input changes from nominal to min. or max. rated values.

LOAD REGULATION
±0.2% or ±10mV for load changes from 50% to 0% or 100% of max. rated values.

MINIMUM LOAD
Main output requires a 10% minimum load for full output from auxiliaries. Use Option 08 if no minimum load is available for mains up to 500 watts. Singles require no minimum load.

RIPPLE & NOISE
1% or 100 mV, pk.-pk., 20 MHz bandwidth.

OPERATING TEMPERATURE
0-70°C. Derate 2.5%/°C above 50°C.

COOLING
A min. of 10 LFS* for models without internal fans directed over the unit for full rating. Two test locations on chassis rated for max. temperature of 90°C. 600 watt, 750 watt and 1000 watt models have built-in ball bearing fans.
*Linear feet/second.

TEMPERATURE COEFFICIENT
±0.02%/°C.

DYNAMIC RESPONSE
Peak transient less than ±2% or ±200 mV for step load change from 75% to 50% or 100% max. ratings.

RECOVERY TIME
Recovery within 1%. Main output - 200 microseconds. Auxiliary outputs - 500 microseconds.

SAFETY
Units meet UL 1950, CSA 22.2 No. 950, EN 60 950, IEC 950.

ISOLATION
Conforms to safety agency standards.

INPUT UNDERVOLTAGE
Protects against damage for undervoltage operation.

SOFT START
Units have soft start feature to protect critical components.

OVERVOLTAGE PROTECTION
Standard on all outputs.

REVERSE VOLTAGE PROTECTION
All outputs are protected up to load ratings.

OVERLOAD & SHORT CIRCUIT
Outputs protected by duty cycle current foldback circuit with automatic recovery. Standard auxiliaries have additional back-up fuse protection. Options 04 and 16 have square current limiting with automatic recovery when overload is removed.

THERMAL SHUTDOWN
Circuit cuts off supply in case of local over temperature. Units reset automatically when temperature returns to normal.

FAN OUTPUT
Nominal 12 VDC @ 12 watts maximum.

INHIBIT
TTL compatible system inhibit provided. Option 16 has individual output inhibit.

REMOTE SENSING
On all outputs except standard and 04 Option outputs 75 watts or less.

SHOCK & VIBRATION
Shock per MIL-STD 810-E Method 516.4, Procedure I.
Vibration per MIL-STD 810-E Method 514.4, Category 1, Procedure I.

MECHANICAL

CASE	SERIES	WATTS	H	x	W	x	L
1	FT	400W/500W	2.50"	x	4.93"	x	8.00"
3	FT	600W	2.56"	x	5.08"	x	10.03"
4	FS	600W	2.56"	x	5.08"	x	11.00"
5	FT	750W	2.63"	x	5.20"	x	10.03"
6	FS	750W	2.63"	x	5.20"	x	11.63"
7	FS	1000W	2.56"	x	7.13"	x	11.63"

OPTIONS

POWER FAIL MONITOR
Optional circuit provides isolated TTL and VME/VXI compatible ACFAIL signal providing 4 milliseconds warning before main output drops by 5% after an input failure. A SYSRESET signal following VME timing requirements is provided when an N module is used as a main output. Both logic signal outputs can sink current per the VME specification.

REDUNDANCY
Optional Or-ing diodes for hot pluggable N+1 redundant operation. For FT Series 500 watt & 750 watt models with 1-4 outputs. Main output current limited to 100 amps. Remaining outputs 16 amps max.

CURRENT LIMIT
Option provides on all outputs:
- Square current limit with auto recovery.
- Wireless droop current share for parallel or N+1 redundant operation.

ZERO PRELOAD
Optional circuit removes need for preload on main output up to 500 watts.

ENHANCED
Option provides on all outputs:
- Square current limit with auto recovery.
- Single wire active current share for parallel or N+1 redundant operation.
- DC output good logic signal with LED indicator.
- Logic inhibit.
- Nominal 5V bias.
- Margining.

END FAN COVER
Optional cover with brushless DC ball bearing end fan which provides the required air flow for full rating.

TOP FAN COVER
Same as above with fan cover mounted on top of the power supply.

ACCESSORIES
RA50 and RA75 Series 2U high rack assemblies provide hot pluggable interface and hold up to 3 FT Series 500 watt or 750 watt units respectively.

Specifications subject to change without notice.

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JUNE

Eighth Biennial IEEE Conference on Electromagnetic Field Computation (CEFC), Jun. 1-4. Westin La Paloma, Tucson, AZ. Contact Paul A. Baltes, Engineering Professional Development, Box 9, Harvill Bldg., P.O. Box 210076, University of Arizona, Tucson, AZ 85721; (520) 621-3054; fax (520) 621-1443; e-mail: baltes@engr.arizona.edu.

POF World '98 (Plastic Optical Fiber), June 1-4. Providence Convention Center, Providence, RI. Contact Information Gatekeepers Inc., 214 Harvard Ave., Boston, Massachusetts 02134; (617) 232-3111; fax (617) 734-8562; www.igigroup.com.

International Conference on Consumer Electronics (ICCE), June 2-4. Los Angeles Airport Marriott, Los Angeles, CA. Contact Diane Williams, Conference Coordinator, 67 Raspberry Patch Dr., Rochester, NY 14612-2868; (716) 392-3862; fax (716) 392-4397, e-mail: d.williams@ieee. org; www.icce.org.

Fifth IEEE International Conference on Software Reuse, June 2-5. Victoria Conference Center, Victoria, BC, Canada. Contact Ted Biggerstaff, Microsoft Research, One Microsoft Way, Mail Stop 9S/1032, Redmond, WA 98052-6399; (206) 936-5867; fax (206) 936-0502; e-mail: tedb@microsoft.com.

Enterprise Networking and Computing (ENCOM '98), June 11. Georgia World Congress Center, Atlanta, GA. Contact Bhumip Khasnabish, GTE Labs Inc., (617) 466-2080; fax (617) 466-2130.

IEEE International Conference on Communications (ICC '98), June 7-11. Atlanta, GA. Contact Judy Keller, IEEE Communications Society, 345 E. 47th St., New York, NY 10017; fax (212) 705-7865; e-mail: j.keller@ieee.org.

IEEE International Symposium on Electrical Insulation, June 7-11. Key Bridge Marriott Hotel, Arlington, VA. Contact David R. James, Oak Ridge National Laboratory, P.O. Box 2008, Bldg. 4500S, MS-6123, Oak Ridge, TN 37831-6123; (423) 574-6213; fax (423) 574-6210; e-mail: dyj@ornl.gov.

IEEE/MTT-S International Microwave Symposium (MTT 98), June 7-12. Baltimore Convention Center, Baltimore, Maryland. Contact Steven Stitzer, Westinghouse Electric Corp., P.O. Box 1521, MS 3T15, Baltimore, Maryland 21203; (410) 765-7348; fax (410) 993-7747.

IEEE Symposium on VLSI Technology, June 9-11. Honolulu, HI. Contact Melissa Widerkehr, Widerkehr & Associates, 101 Lakeforest Blvd., Suite 270, Gaithersburg, MD 20877; (301) 527-0900; fax (301) 527-0994; e-mail: widerkehr@aol.com.

IEEE Symposium on VLSI Circuits, June 11-13. Honolulu, HI. Contact Phyllis Mahoney, Widerkehr & Associates, 101 Lakeforest Blvd., Suite 270, Gaithersburg, Maryland 20877; (301) 527-0900; fax (301) 527-0994; e-mail: pwmahoney@aol.com.

USENIX 1998 Technical Conference, June 13-17. Marriott Hotel, New Orleans, Louisiana. Contact USENIX Conference Office, 22672 Lambert St., Suite 613, Lake Forest, California 92630; (714) 588-8649; (714) 588-9706; e-mail: conference@usenix.org; www.usenix.org.

35th Design Automation Conference, June 15-19. Moscone Center, San Francisco, CA. Contact MP Associates, 5305 Spine Rd., Suite A, Boulder, CO 80301; (303) 530-4333; e-mail: dacinfo@dac.com; www.dac.com.

Exhibition & Conference on System Integration in Microelectronics, June 16-18. Nuremberg Exhibition Centre. Call +49 711-61946-26/-74; fax +49 711-61946-93; www.mesago.de

IEEE Antennas and Propagation Society International Symposium and URSI National Radio Science Meeting, June 21-26. Stouffer Renaissance Waverly Hotel, Atlanta, Georgia. Contact Andrew Peterson, Georgia Institute of Technology, School of Electrical & Computer Engineering, ECE 0250/Van Leer, Atlanta, Georgia 30332; (404) 894-4697; fax (404) 894-4641; e-mail: peterson@ee.gatech.edu.

American Control Conference (ACC '98), June 24-26. Adams Mark Hotel, Philadelphia, PA. Contact Joe Chow, ECSE Department Rensselaer Polytechnic Institute, Troy, NY 12180-3590; (518) 276-6374; fax (518) 276-6261; e-mail: chowj@rpi.edu.

JULY

Conference on Precision Electromagnetic Measurements (CPEM '98), July 6-10. Renaissance Washington Hotel, Washington, D.C. Contact Katherine H. Magruder, NIST, Bldg. 220, Room B162, Gaithersburg, MD 20899; (301) 975-2402; fax (301) 926-3972; e-mail: katherine.magruder@nist.gov.

Second IEEE World Conference on Photovoltaic Energy Conversion (WCPEC), July 6-10. Vienna, Austria. Contact Heinz Ehmann, WIP, Sylvensteinstrasse 2, D-81369 Munchen, Germany.

IEEE International Geoscience & Remote Sensing Symposium (IGARSS '98), July 6-10. Sheraton Seattle, WA. Contact Tammy I. Stein, IGARSS Business Office, 2610 Lakeway Dr., Seabrook, TX 77586-1587, (281) 291-9222; fax (281) 291-9224; e-mail: tstein@phoenix.net.

IEEE Power Engineering Society Summer Meeting, July 12-16. Sheraton San Diego Hotel & Marina, San Diego, California. Contact Terry Snow, San Diego Gas & Electric, Post Office Box 1831, San Diego, California 92112; (619) 696-2780; fax (619) 699-5096; e-mail: t.snow@ieee.org.

SPIE's Annual Meeting & Optical Instrumentation Show, July 19-24. San Diego, California. Contact SPIE Exhibits Dept., Post Office Box 10, Bellingham, Washington 98227-0010; (360) 676-3290; fax (360) 647-1445; e-mail: exhibits@spie.org.

IEEE Nuclear & Space Radiation Effects Conference (NSREC '98), July 20-24. Newport Beach, California. Contact Jim Schwank, Sandia National Laboratories, Post Office Box 5800, MS-1083, Albuquerque, New Mexico 87185-1083; (505) 844-8376; fax (505) 844-2991; e-mail: schwanjr@sandia.gov.

AUGUST

IEEE International Symposium on Information Theory, August 16-21. Massachusetts Institute of Technology, Cambridge, Massachusetts. Contact G. David Forney, Motorola Inc., MS M4-15, 20 Cabot Blvd., Mansfield, Massachusetts 02048-1193; (508) 261-5347; fax (508) 337-7173; e-mail: LUSE27@email.mot.com.


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READER SERVICE 93

Generate Advanced PWM Signals Using DSPs

On-chip Timers And Registers Enable DSP Controllers To Generate Symmetric Space-Vector PWM Signals For Three-Phase Motors.

ISSA PANAHI, ZHENYU YU, and MOHAMMED AREFEEN, Texas Instruments, Digital Control Applications Group, 12203 S.W. Freeway, M/S 723, Stafford, TX 77477; (281) 274-3247; fax: (281) 274-4809.

Today's programmable digital signal processors (DSPs) provide capabilities that make generating advanced pulse-width-modulation (PWM) signals easier than previous techniques. Using a DSP makes it easy to change carrier frequency and PWM scheme simply through reprogramming. In addition, they allow generation of three pairs of complementary PWM waveforms with programmable dead bands for three-phase voltage-source inverters. The combination of these features helps reduce the number of chips needed to implement the entire circuit, increasing reliability and lowering the overall cost of the system.

TABLE 1: SWITCHING PATTERNS AND OUTPUT VOLTAGES OF A 3-PHASE POWER INVERTER

a	b	c	V_a	V_b	V_c	V_{ab}	V_{bc}	V_{ca}
0	0	0	0	0	0	0	0	0
1	0	0	2/3	-1/3	-1/3	1	0	-1
1	1	0	1/3	1/3	-2/3	0	1	-1
0	1	0	-1/3	2/3	-1/3	-1	1	0
0	1	1	-2/3	1/3	1/3	-1	0	1
0	0	1	-1/3	-1/3	2/3	0	-1	1
1	0	1	1/3	-2/3	1/3	1	-1	0
1	1	1	0	0	0	0	0	0

As a result, advances in solid-state power devices and high-performance processors have substantially increased the use of switching power converters in more modern motor drives to convert and deliver the required energy to each motor. There also are many advantages of PWM-based switching power converters over linear power amplifiers. Some key benefits include easy implementation and control, no temperature variation and aging-caused drifting or degradation in linearity, compatibility with today's digital microprocessors, and lower power dissipation. These advances, in turn, are helping manufacturers to shorten the time-to-market.

Popular PWM Techniques

Three commonly used PWM techniques include sinusoidal, hysteresis (bang-bang), and space-vector (symmetrical or asymmetrical) implementations. Widely used in industrial applications, sinusoidal PWM (SPWM) is the generation of PWM outputs with sine waves as the modulating signals (*Fig. 1a*). The on and off instances of the PWM signal can be determined by comparing a sine wave (the modulating wave) with a high-frequency triangular wave (the carrier wave). In SPWM, the frequency of the modulating wave determines the frequency of the output voltage. The peak amplitude of the modulating wave determines the modulation index, and in turn controls the rms value of output voltage. Changing the modulation index can vary the rms value of the output voltage and significantly improves the distortion factors, as compared to other multiphase modulation techniques.

To implement SPWM using analog circuits, the following building blocks must be used:

- a high-frequency triangular wave generator;
- a sine wave generator;
- a comparator; and
- an inverter circuit with dead-band generators to produce complimentary driving signals with required dead bands.

All of these building blocks can be implemented using single or multiple chips, however, analog implementation of these circuits does present challenges commonly associated with analog circuits.

Hysteresis PWM refers to the technique where the output is allowed to oscillate within a predefined error band called a "hysteresis band." The switching instants are generated from the vertices of the triangular wave (*Fig.1b*). Hysteresis PWM techniques do not require any information about the inverter load characteristics. As long as the reference signal is known and the inverter output voltage is not saturated, the inverter output will always follow the reference.

Hysteresis PWM can be implemented with both analog circuits and digital circuits, however, digital implementation utilizing DSPs is becoming more popular due to the processor's programmable flexibility and overall reliability. Any available DSP controller can be utilized to implement this PWM technique.

The Space-Vector PWM technique refers to a special switching sequence of the three-phase voltage source inverters using basic space-vectors to generate the output voltages to the motor. The space-vector PWM technique has been shown to generate less harmonic distortion in output voltages and/or currents applied to the phases of an ac motor. In addition, it provides a more efficient use of the supply voltage in comparison with direct sinusoidal modulation technique.

The objective of space-vector PWM is to approximate the output voltage vector U_{out} by a combination of the eight switching patterns. With today's DSPs, space-vector PWM can easily be implemented. The on-chip timer and compare unit features available in DSP processors like the TMS320C24x play a key role in the implementation of PWM signal generation.

The event manager module in such processors also has built-in hardware to simplify the generation of symmetric space-vector PWM waveforms (*Fig.1c*). This on-chip hardware eliminates the need to determine the channel toggle frequency, as it also simplifies the compare register loading requirements so that the user does not have to worry about matching the values with the compare registers.

Symmetric PWM

The energy that a switching power converter delivers to a motor is controlled by PWM signals that are applied to the gates or the bases of the power transistors. PWM signals are described as pulse trains with variable pulse width, fixed frequency and magnitude—with one pulse of fixed magnitude in every PWM period. However, the width of the pulses changes from pulse to pulse according to a modulating signal.

When a PWM signal is applied to the gate/base of a power transistor, it causes the turn-on and turn-off intervals of the transistor to change from one PWM period to another PWM period according to the same modulating signal. The frequency of a PWM signal must be much higher than the modulating signal, the fundamental frequency, such that the energy delivered to the motor and its load depends mostly on the modulating signal.

The pulses of a symmetric PWM signal are always symmetric with respect to the center of each PWM period. The pulses of an asymmetric PWM signal always have the same side aligned with one end of each PWM period. Asymmetric PWM can be used for stepper motors and other variable-reluctance motors.

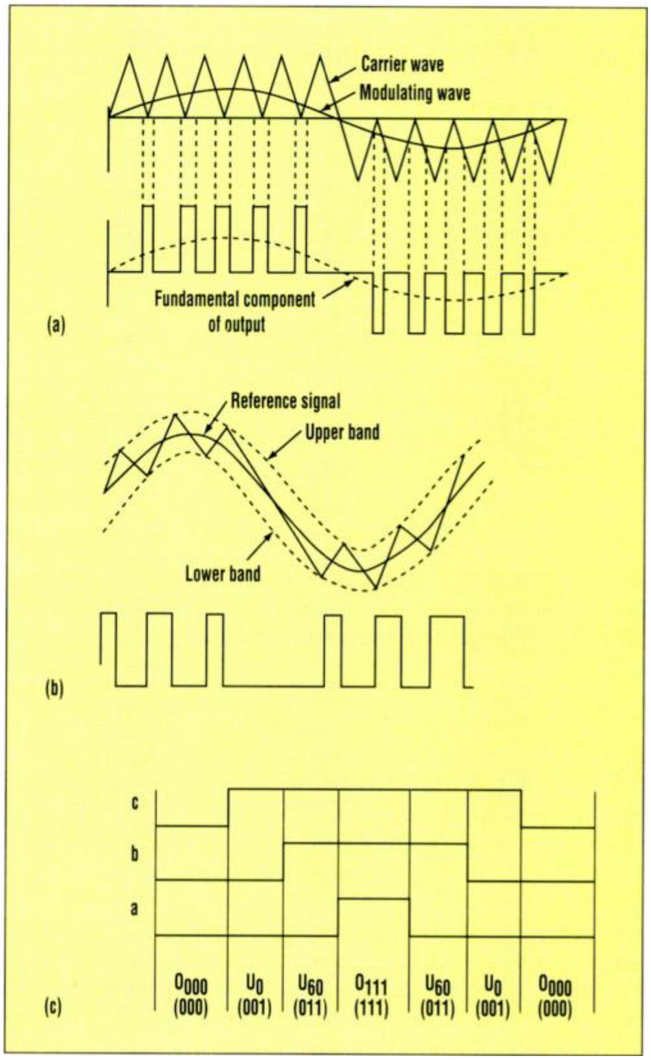
Symmetric PWM methods are often used for three-phase ac induction and brushless dc motors, due to the lower harmonic distortion that is generated on phase currents in comparison to asymmetric PWM methods.

Generating Waveforms

To generate the proper signals, engineers require a high-frequency PWM, the flexibility to change frequency in real-time and dead band to secure safe operation of the power converter. DSP controllers have made it more practical for designers to apply space-vector PWM waveform generation. This has allowed high-speed processing to meet high-frequency requirements and programmable frequency changes either from application to application, or in real-time in a given application. High-frequency PWM signals are desirable for better control of the motor phase currents and smoother performance of the motor and load. An additional benefit is optimizing the

TABLE 2: HARMONICS IN OUTPUT CURRENTS WITH SPACE VECTOR AND SINUSOIDAL PWM TECHNIQUES (dB)

	Magnitude of fundamental	Magnitude of 2nd harmonic	Magnitude of 3rd harmonic
Space vector PWM	78	0.602	1.348
Sinusoidal PWM	85	0.715	2.369
Sinusoidal PWM / space vector PWM	Ratio = 1.09	Ratio = 1.19	Ratio = 1.760



1. In the sinusoidal pulse-width modulaion (PWM) technique, the modulating sinewave determines the frequency of the output voltage (a). The hysteresis PWM's output oscillates within a predefined error band called the hysteresis band (b). The symmetric space-vector PWM waveform generates a switching sequence of the three-phase voltage using basic space vectors (c).

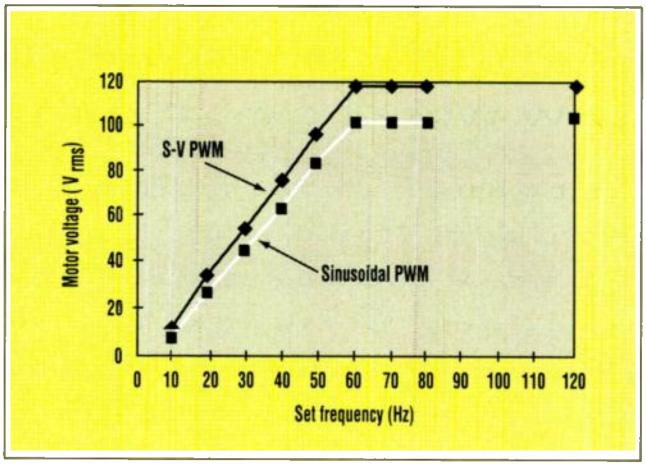
dead band and eliminating its undesired impacts on the motor phase currents.

Symmetric space-vector PWM has been widely used in three-phase switching power converters, including those used for three-phase ac induction motors. Using DSPs, specifically the TMS320C24x with built-in, on-chip hardware, for such applications, facilitates the implementation of a symmetric space-vector PWM waveform. In addition, the speed of DSPs allows implementation of this kind of PWM at high frequencies. This leaves ample time for the CPU to do other motor control functions. Also, dedicated features on these controllers eliminate the need for external off-chip components.

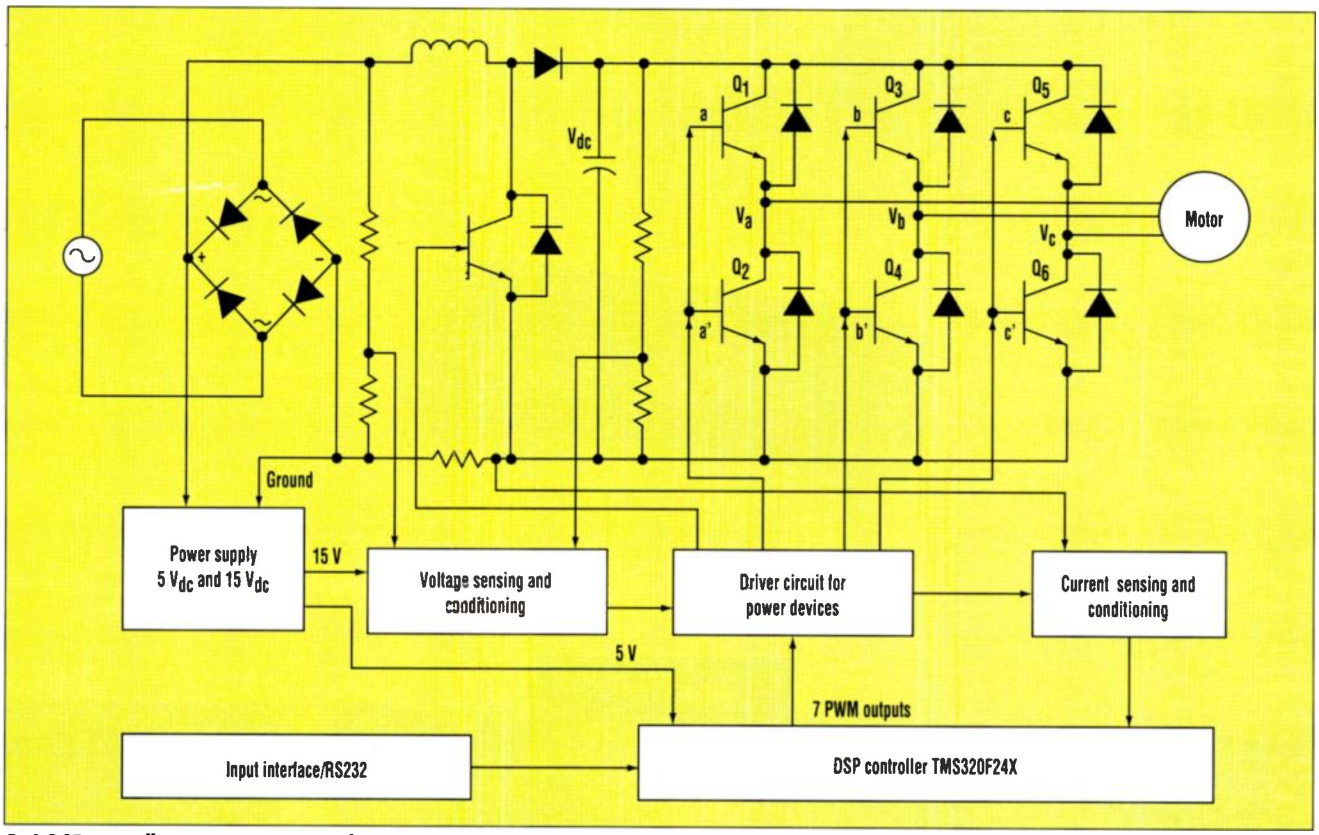
For instance, the TMS320C24x has 3 general-purpose timers, 3 full Compare Units, and 3 simple compare units, Programmable dead-band units and a dedicated space-vector PWM module that can be used for generating PWM outputs. It can generate up to 12 PWM outputs, of which half are complementary with programmable dead-band time.

The general-purpose (GP) timers can be configured to run in up and up/down count modes for generating asymmetrical and symmetrical PWM outputs. The period registers of the GP timers are shadowed to allow on-line change of PWM frequency, which in turn allows wabbling of PWM frequency, which can help spread out the spectrum of the PWM outputs.

The pulse widths of the PWM outputs are determined by values in the compare registers. The compare registers are shadowed, allowing the CPU to write to these registers at any time during the current PWM period. The new compare values can be programmed to become active immediately on underflow or on period match. The polarities of the PWM outputs can be independently controlled by the action control register and the simple action control register. The polarity of a PWM output can be active high, active low, forced high, and forced low, allowing control of different types of power devices, such as IGBTs, power Mosfets, and bipolars.. The action control registers are also shadowed so users can write to these registers to change the polarities of PWM outputs at any time during a PWM period.



3. By comparison to the sinusoidal technque, the space-vector PWM generates approximately 14 to 25% more output voltage, and produces less harmonics in the output current.



2. A DSP controller eases generaton of symmetric space-vector PWM signals for controlling a three-phase motor. The pulse widths of the PWM outputs are determined by values in the timer and compare registers of the programmable DSP.

The space-vector PWM module automatically generates space-vector PWM patterns once a starting basic vector and a direction is given in the action control register.

The generation of such PWM outputs is entirely register-based. All the registers are data memory mapped so the CPU can access them as data memory locations. To generate a certain kind of PWM output, the CPU:

- Writes to the pin configuration registers to configure the pins as PWM outputs
- Writes to the GP timer control, compare control registers, the action control registers, and the dead-band control registers to configure PWM frequency, type of PWM waveform to be generated, polarities of the PWM outputs and the dead band
- Continuously updates the compare registers based on newly determined pulse widths.

Any of the mentioned PWM techniques can be used to determine the pulse widths.

One significant advantage of using symmetric space-vector PWM is that the technique applies about 14% more voltage on motor windings in comparison to sinusoidal PWM with the same dc bus voltage. This translates into a more efficient utilization of bus voltage, as well as a motor that can be rated at a higher voltage and lower current to achieve the same horsepower rating.

Using symmetric space-vector PWM results in 10% less phase current, with a reduced power dissipation and heat generation in the power converter and motor. Finally, symmetric space-vector PWM technique generates less harmonics in phase current for less power dissipation and less noise. It has been observed that symmetric space-vector PWM technique generates less audible noise, especially when the dc bus voltage goes above 100 V.

Depicted is the structure of a typical three-phase voltage-source power inverter—V_a, V_b, and V_c are the output voltages applied to the windings of a motor *(Fig. 2)*. Q1 through Q6 are the six power transistors that shape the output, which are controlled by a, a', b, b', c, and c'. When an upper transistor is switched on (a, b, or c is 1), the corresponding lower transistor is switched off (a', b', or c' is 0). The on and off states of the upper transistors Q_1, Q_3, and Q_5, or equivalenty the state of a, b, and c, are sufficient to evaluate the output voltage.

The relationship between the switching variable vector $[a, b, c]^t$ and the line-to-line voltage vector $[V_{ab}\ V_{bc}\ V_{ca}]^t$ is given by Equation 1, from which one can easily arrive at Equation 2 that determines the phase voltage vector $[V_{ab}\ V_{bc}\ V_{ca}]^t$.

As shown in Figure 2, there are eight possible combinations of on and off patterns for the three power transistors that feed the three-phase power inverter. Notice that the on and off states of the lower power transistors are opposite to the upper ones, so they are completely determined once the states of the upper power transis-

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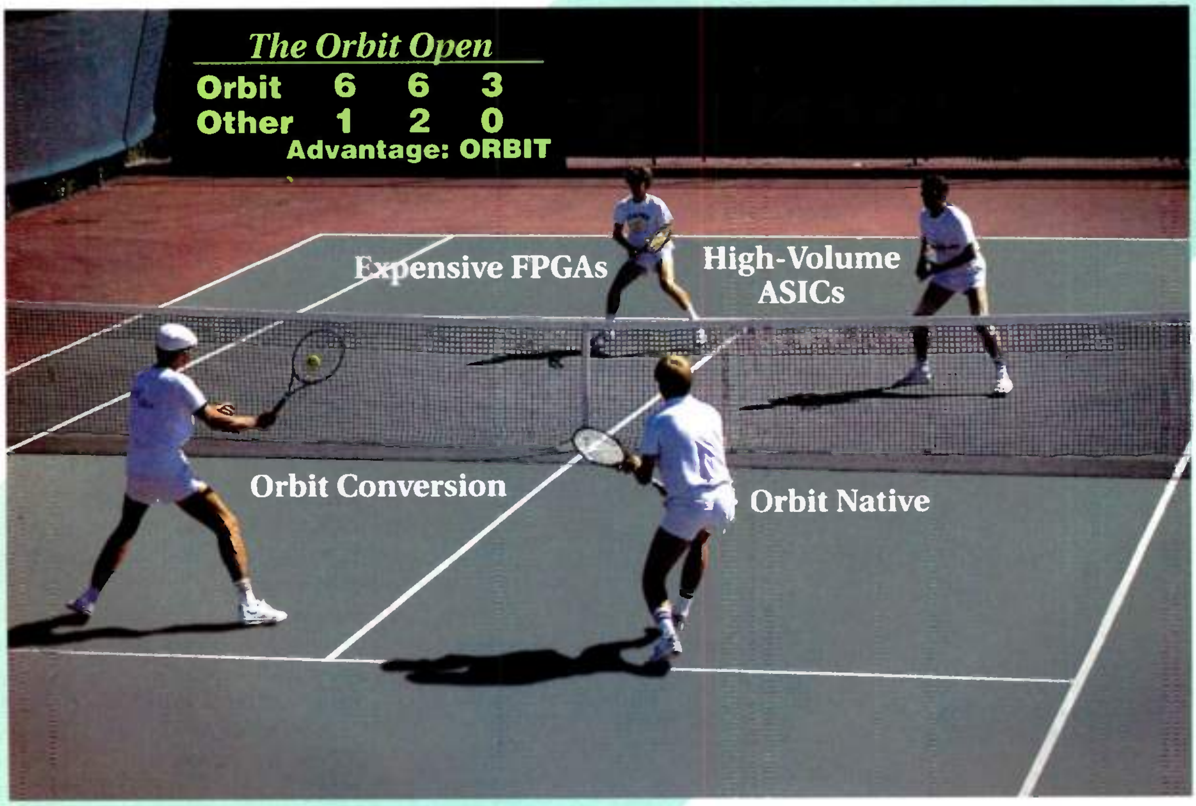

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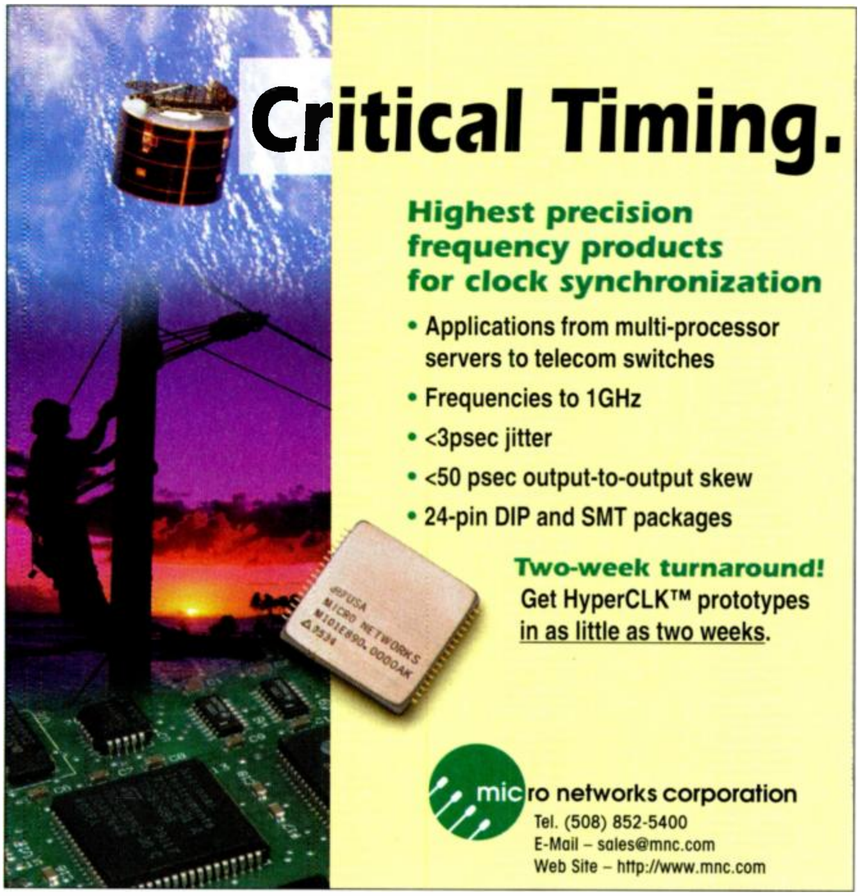

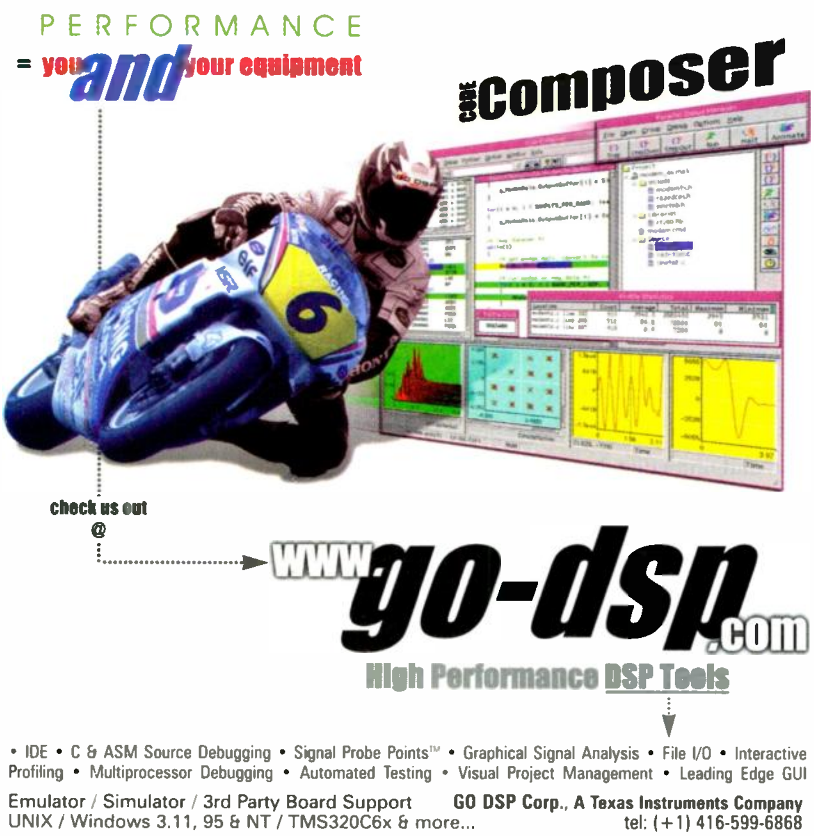

tors are known. The eight combinations and the derived output line-to-line and phase voltages in terms of dc supply voltage V_{dc}, according to Equation 1 and 2, are shown in Table 1.

$$\begin{bmatrix} V_{ab} \\ V_{bc} \\ V_{ca} \end{bmatrix} = V_{dc} \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \quad (1)$$

$$\begin{bmatrix} V_{a} \\ V_{b} \\ V_{c} \end{bmatrix} = \frac{1}{3} V_{dc} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \quad (2)$$

Experimental Results

Experimental data results of using the TMS320 DSP, as well as the sinusoidal and space-vector PWM techniques are shown *(Fig. 3 and Table 2)*. A three-phase ac induction motor, rated at 147V, 60 Hz and 1/2 hp is controlled, in this case, based on constant V/Hz principle with a PWM frequency of 25 kHz, sampling frequency of 12.5 kHz, and dc bus voltage of 180V. It can be seen that the space-vector PWM technique generates 14 to 25% more output voltage and an obvious reduction in harmonics in output currents.

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Mohammed Arefeenis a DSP applications engineer for power electronics and motor control. He holds an MS and a Ph.D from Texas A&M University, College Station. Dr. Arefeen can be contacted via e-mail at at aref@micro.ti.com.


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ADCs Lend Flexibility To Vector Motor-Control Applications

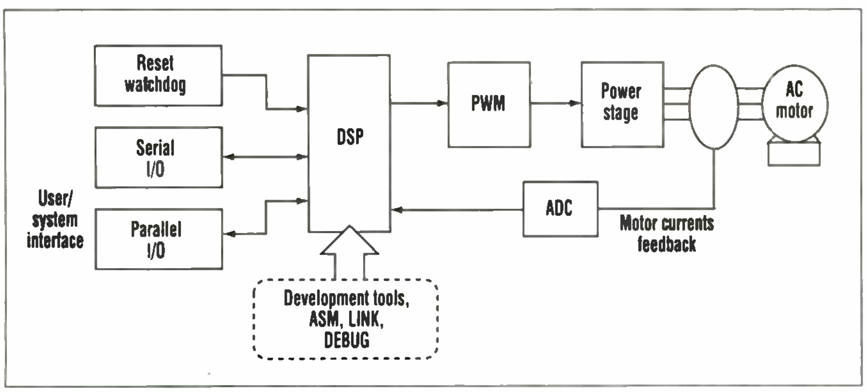
Available Either As Discrete Devices Or, More Recently, Packaged With A DSP Core, ADCs Are Stepping Up To User Requirements.

NIALL LYNE, Analog Devices Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106 (781)329-4700

The performance of high-end servo drives is quickly approaching its limits due to the physical constraints imposed by high-resolution position acquisition. These limits are set by the need to use analog position-feedback signals to obtain the higher resolution needed. Furthermore, the motor-control industry in general is demanding higher levels of system integration from their silicon providers.

Responding to the challenge, these providers are pushing the limit of mixed-signal integration of high performance analog-to-digital converters (ADCs) on the same substrate as a high-performance digital signal processor (DSP). This push has led to the introduction of single-chip motor-control solutions that integrate successive approximation (SAR) or sigma-delta (Σ-Δ) converters, which in turn are only part of a range of single-chip DSP microcontrollers for ac motor-control applications.

However, before any comparative discussion of discrete simultaneous-sampling, SAR ADC solutions and an integrated Σ-Δ solution can begin, it is important to review what is required of a typical ac motor-control system. The discrete SAR and integrated Σ-Δ solutions, both of which demonstrate the versatility of ADCs, can then be discussed in the context of applications issues that arise when choosing one solution over the other in high-performance, variable-speed, motor-drive systems.



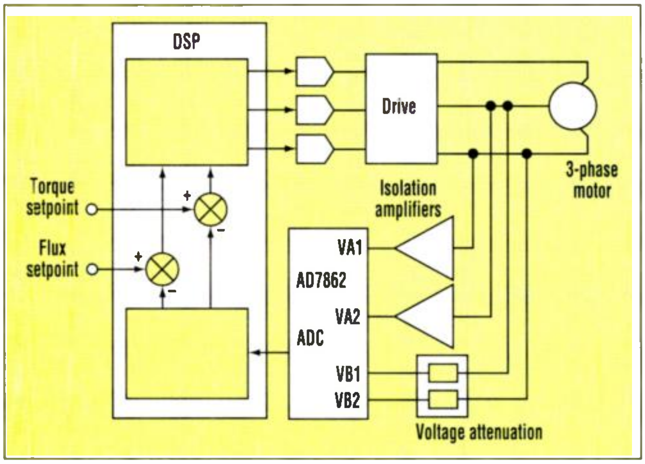
1. The typical motor-control signal chain requires a processor core and a generic set of peripheral function blocks to interface between the digital processor and the "real-world" signals. The control system has two loops; the motion loop handles the mechanical load and maintains rotary position and velocity, while the current loop handles the dynamics of the motor electrical system and controls torque production. Eight- or 16-bit microcontrollers are usually sufficient.

Types Of ADCs Used

A servo-control application will typically demand synchronous sampling of at least two motor currents. At the system level, this usually requires the use of sample-and-hold amplifiers, the outputs of which feed a multiplexer, which in turn is sampled with a single SAR ADC. In a discrete realization of such a system, the analog and digital portions can be isolated by using separate ground planes and separate supplies. With mixed-signal integration, the analog and digital portion must coexist on the same substrate. As a result, the high-frequency clocks, which emanate from the processor portion of the die, will couple into the analog portion of the device. There they will corrupt the information content of the measurement signal. The sample-and-hold amplifier, which is in essence a large capacitor (in die area, not value), is particularly susceptible to this substrate noise.

One solution to this mixed-signal integration problem is to remove the sample-and-hold amplifier and still satisfy the system requirement for simultaneous sampling by providing two SAR ADCs converting in parallel. A second alternative would be to reduce the conversion time of the ADC, say to less than 1 µs. By doing so, the hold time, and hence the capacitor size, can be reduced. This, in turn, will reduce the susceptibility of the analog portion to substrate noise.

A third approach is to use a fast ADC with a conversion time of less than 1 µs. Then, sample the current information serially, without using a sample-and-hold amplifier. Although this doesn't satisfy the system-level requirements for simultaneous sampling, many applications could tolerate the error associated with a delay of 1 µs between samples. The limitation here is the provision of greater than 11 bits of accuracy in less that 1 µs—for a reasonable cost. Today, this is no longer as big an issue due to the availability of cost-effective, 12-bit devices that operate at upwards of 60 Msamples/s.



2. A typical dual-channel ADC for vector-controller applications includes simultaneous-sampling capability. The high-speed, low-power, dual-channel, simultaneous-sampling, 12-bit ADC contains two 4-µs, successive-approximation ADCs and two track/hold amplifiers. By sampling each channel simultaneously (each channel has two inputs: VA1 and VA2, and VB1 and VB2), the relative phase information of the signals on both analog inputs is preserved. A DSP microprocessor is then used to perform the mathematical transformations and control-loop calculations on the information fed back by the ADC.

A fourth approach is to use two ΣΔ converters in parallel. A successive-approximation ADC, by design, has a sample-and-hold amplifier on the input channel. As in the case of the system-level sample-and-hold amplifier, it too is susceptible to substrate noise. In this case, however, the hold time, and hence the size, of the capacitor is smaller. Nevertheless, this sample-and-hold amplifier is susceptible to substrate noise.

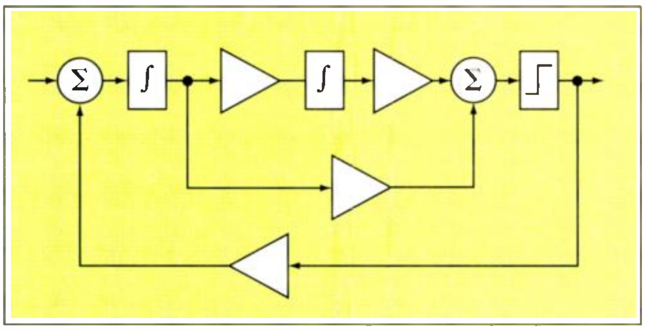
With a Σ-Δ converter, the sample-and-hold amplifier is an order of magnitude smaller again. Indeed, the size of the analog logic portion of the converter is an order of magnitude smaller than that of its successive-approximation counterpart. Thus, the overall susceptibility of a Σ-Δ converter to substrate noise is significantly lower than that of a successive-approximation converter. This article will focus on the two most common ADC architectures mentioned, SAR ADCs, and the Σ-Δ-ADC approach.

The Ac Motor-Control System

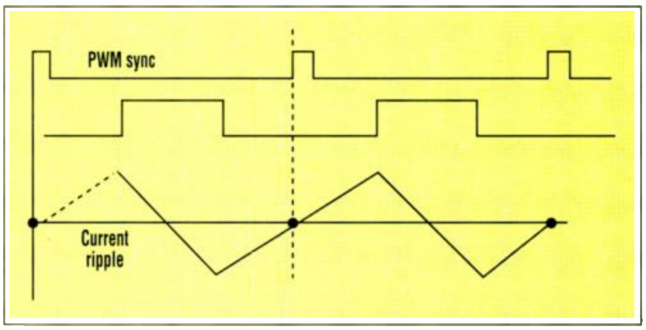
The typical motor-control signal chain requires a processor core and a generic set of peripheral function blocks to interface between the digital processor and the "real world" signals *(Fig. 1)*. The basic blocks to interface to an ac motor power converter are a PWM generator and an analog-to-digital conversion system. There also are other peripherals required for real-time embedded control systems, such as a parallel digital I/O block, a serial communication interface, a watchdog timer, and event timers. The DSP microcontroller combines the powerful DSP core with the set of peripherals to complete the signal chain.

The control system has two loops—the motion loop handles the mechanical load and maintains rotary position and velocity, while the current loop handles the dynamics of the motor electrical system and controls torque production. Motion-control loops in variable-speed and servo-drive systems typically have bandwidths of the order of 20 or 30 Hz, with sample rates of 500 Hz to 3 kHz. This bandwidth can be handled by 8- or 16-bit microcontrollers. Typically in these systems, the current loops are implemented in the analog domain and the input signals to this domain are generated using digital-to-analog converters (DACs).

Recently introduced to the world of motion control, DSPs are high-speed microcomputers developed originally for such applications as telecommunica-



3. Σ-Δ converter technology is based on an oversampling technique. The input signal is typically sampled with a 1-bit converter (a modulator) at high frequencies—typically 1 to 2 MHz. The resulting high-frequency bit stream is digitally filtered and decimated (downsampled) to the effective sample rate. Attention to the sampling frequency and its relation to the PWM waveform can eliminate any harmonics. This converter technology is well suited to a bulk CMOS process, and also is very conducive to mixed-signal integration.

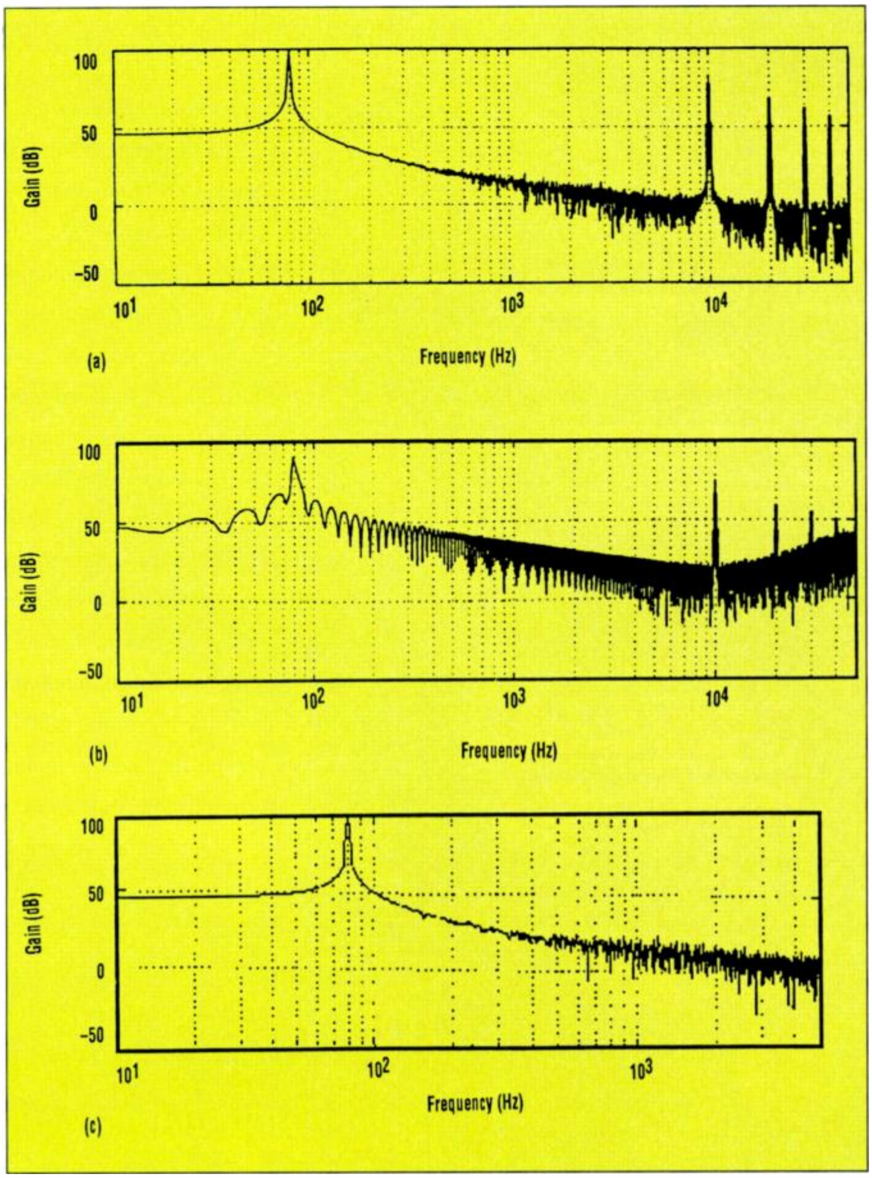


4. Typically, the sampling of a current waveform is synchronized with the pulse-wave-modulated (PWM) waveform to reduce the effect of PWM ripple on the sampled data. In doing so, each of the sideband harmonics are symmetric about the PWM switching-frequency harmonic. By sampling at the PWM switching frequency, all the sideband harmonics sum to dc. By sampling at the zero mean point of the current ripple, the sideband harmonics sum to zero. This point aligns with the synchronization pulse of a center-based PWM system.

tions and speech processing. The high-speed signal-processing capability of these devices makes them well-suited for ac motor-control applications.

There are many reasons for moving toward a completely digital control system with DSPs at the core. The primary reason is that a digital system offers the most flexible control-system architecture. The switching signals for the three-phase power converter are digital rather than analog in nature. Though they may be produced by using analog comparators, they are just as easily generated using digital timing functions, which eliminates the requirement for a DAC for each current phase. The realization of completely digital control also reduces the susceptibility of the system to the noise sources associated with the power converter.

Typically, current-loop bandwidths are of the order of 1 to 2 kHz, requiring sample rates up to 20 kHz. This must be matched to the power-converter frequency, so high processing speeds are required. Although DSPs have the computing power to control high-bandwidth current loops, they require additional peripheral hardware to implement some of the motor-control peripheral functions—unlike some conventional microcontrollers. Often these functions have been implemented using standard components such as ADCs, and by using gate arrays or application-specific ICs (ASICs). However, depending on the application and the feedback resolution required, this may not be a cost-effective solution.



5. The Σ–Δ converter architecture that is part of the ADMC300 one-chip motor control solution was analyzed to generate the spectrum of the current waveform as well as the spectrum of the remodulated current waveform, (a) and (b), respectively. From (b) it is apparent that the PWM harmonics are indeed sampled. However, by choosing a modulation frequency equal to the decimation factor times the PWM frequency, the sampled PWM harmonics are aliased to dc (c).

Simultaneous-Sampling ADCs

The current drawn by a motor can be split into two components—one produces torque, and the other produces magnetic flux. For optimal performance of the motor, these two components should be controlled independently.

In conventional methods of controlling a three-phase motor, the current (or voltage) supplied to the motor, and the frequency of the drive, are the basic control variables. However, both the torque and flux are functions of current (or voltage) and frequency. This coupling effect can reduce the performance of the motor. For example, if the torque is increased by increasing the frequency, the flux tends to decrease.

Vector control of an ac motor involves controlling phase in addition to drive and current frequency. Controlling the phase of the motor requires feedback information on the position of the rotor relative to the rotating magnetic field in the motor. Using this information, a vector controller mathematically transforms the three-phase drive currents into separate torque and flux components.

A typical dual-channel, simultaneous-sampling ADC (AD7862) for vector-controller applications is shown in circuit *(Fig. 2)*. Along with simultaneous-sampling capability, the high-speed, low-power, 12-bit ADC has two 4-μs successive-approximation ADCs and two track/hold amplifiers.

There are four analog inputs that are grouped into two channels (A and B). Each channel has two inputs (VA1 and VA2, and VB1 and VB2) that can be sampled simultaneously, thus preserving the relative phase information of the signals on both analog inputs. The critical track/hold specifications for preserving the relative phase informa-

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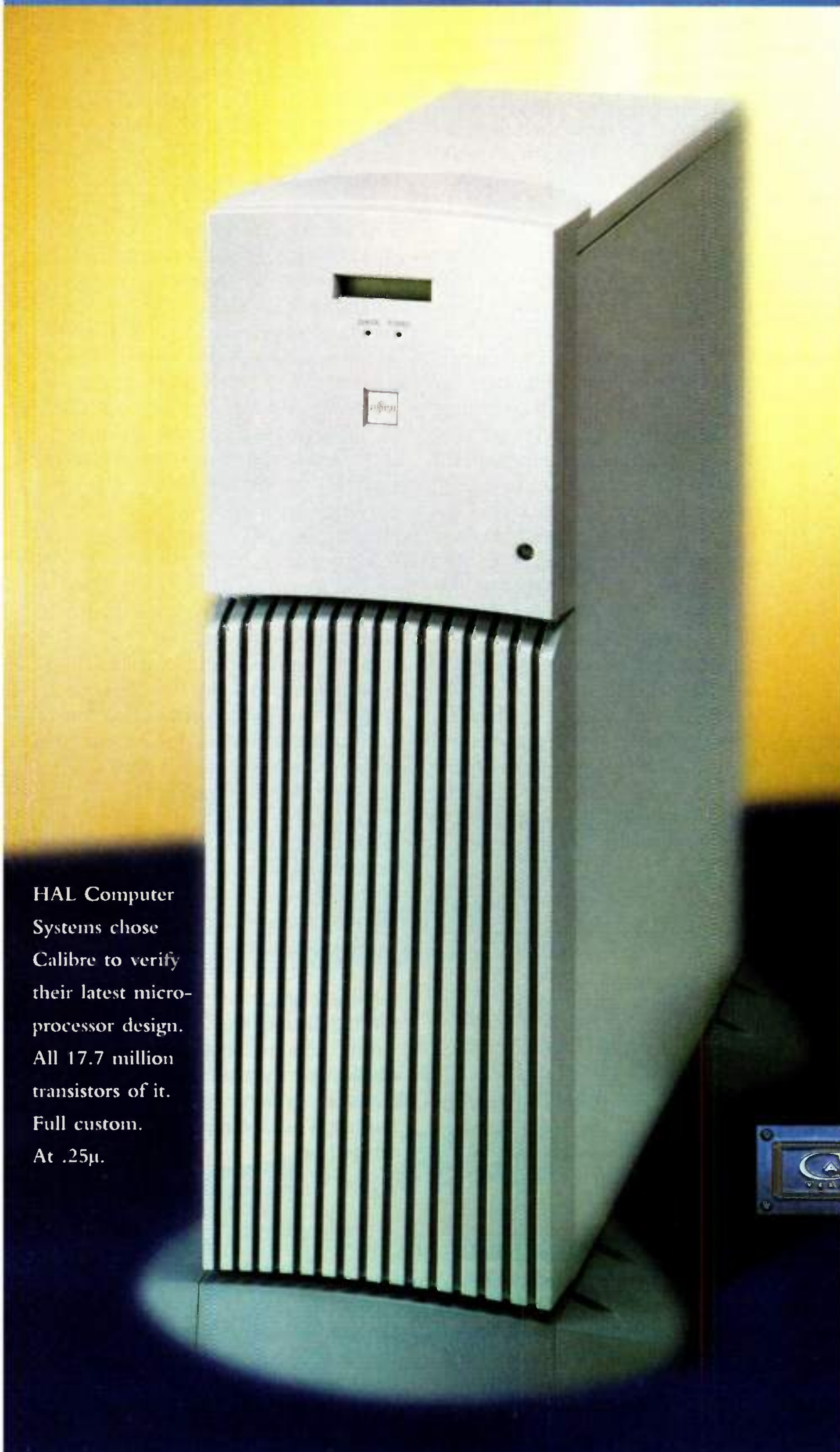

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ples x(0) ...x(n) ...where x(x) is the most recent sample, then z × x(n) = x(n-1).

In the case of the ADMC300, the decimation factor is 64 and the modulation frequency is 64 × PWM frequency. The phase response of the decimation filter for a 10-kHz PWM switching frequency is shown *(Fig. 6)*. Typically, the PWM switching frequency is a decade above the closed-loop bandwidth; therefore, the large-signal harmonic will be typically less than 1 kHz.

For example, a 600-Hz-fundamental current waveform would have a phase delay in the order of 30°. In some applications, this phase delay may be unacceptable, in which case the Σ-Δ can be configured to sample the current waveform at a multiple of the PWM frequency, and the phase delay can be reduced by the oversampling factor. However, oversampling the current waveform at a multiple of the PWM switching frequency will introduce additional PWM harmonics into the passband. These harmonics can be removed by a DSP with a notch filter.

Indeed, the integration of multiple Σ-Δ converters, a center-based PWM scheme, a 25-MIP DSP core, and other peripherals such as encoder interfaces and event timers, provides the motor-controller designer with a very powerful platform to implement sophisticated control schemes which traditionally would not have been at their disposal because of cost and design constraints.

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2. *AD7862 Datasheet*, 10/96, Analog Devices Inc., Norwood, Mass., pp 14 to 15.

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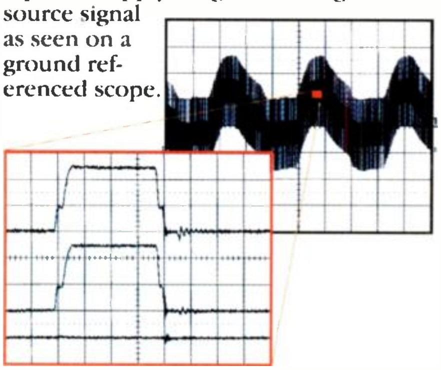

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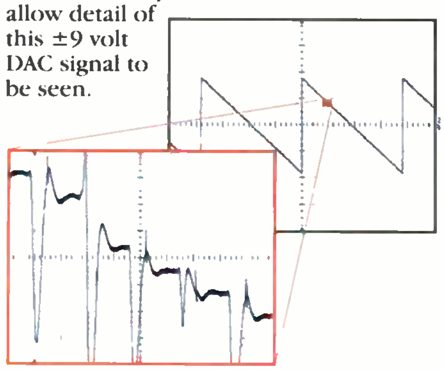

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Power Supply Considerations For Servo Amplifiers

Specifying To Real-World, Power-Supply Requirements Can Greatly Reduce Initial System Costs, While Ensuring A Successful Design.

JIM WOODWARD, Copley Controls Corp., 410 University Ave., Westwood, MA 02090; (781) 329-8200; fax (781) 329-4055; e-mail: jwoodward@copleycontrols.com; www.copleycontrols.com.

The "linear" power supply is simple: just a transformer, rectifier, and capacitor. But, selecting one to power a servo amplifier and motor can be anything but simple. What follows is a short tutorial outlining some of the problems motion-control engineers encounter and the solutions available for them.

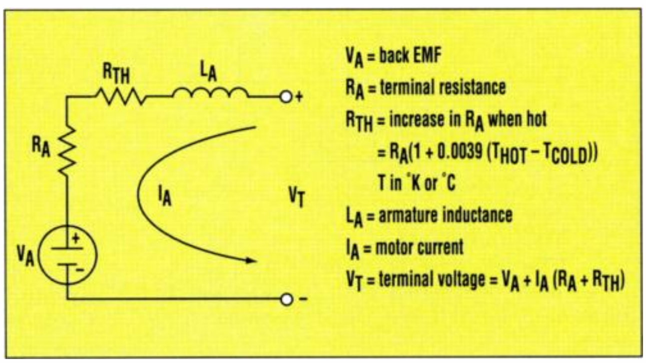
While a control-system engineer thinks in terms of control/amplifier/motor/load, it's common for the motor to be chosen by a mechanical engineer (ME) who is more in touch with the actual pieces of an automatic machine. The ME makes choices based on mechanical units such as torque needed for acceleration, maximum rpm, and continuous power needed at a shaft, and so forth. These considerations yield a motor, rating, case size, and rotor inertia.

What's missing from this picture is the copper. Magnetic fields produce torque in the motor, and these are produced by ampere-turns of copper in the motor. It is this magnetic-field strength in the motor that gives it the power rating at the shaft.

The field strength is a function of the number of turns of wire multiplied by the current in the wire. This produces the motor constant (Km), which can be expressed in units of torque per ampere of winding current (Kt), or as volts per rotational velocity units (Ke). In the English system, one sees Kt as lb-in./A, or oz-in./A, and in the SI system, these become Nm/A. The rotational units (Ke) are V/krpm (volts per thousand rpm) in English, or V/rad/second in SI.

Now, ampere-turns as a product, is governed by two factors: the current in the wire, and the number of turns. Look in a motor catalog, and you'll see the real-world embodiment of this fact as a choice of windings for a particular case size and power rating. You won't see the number of turns listed, it's hidden in the motor constant. Ordinarily, there will be from two to four windings for a given motor, with different motor constants for each. Since torque = torque constant × current (Kt × I), for a constant shaft torque rating, it will take more or less current to do the job. Or, high current multiplied by few turns produces the same strength field in the motor as low current in a lot of turns. So which winding is the right one?

Enter the electrical engineer (EE), who is informed by the ME which motor must be used for the latest and greatest machine, and who must produce a control and drive system for it. How do you choose between the different windings available?



1. Mechanical considerations should give you maximum accelerating torque, T_X, and the top speed, U_X. From these, calculate the maximum motor terminal voltage (V_{TX}) that must be delivered by the power supply and amplifier combination. For the power-supply selection, ignore the armature inductance as the voltage across this will depend on the modulation type. It can be assumed to have an average value of zero under steady-state conditions.

Choosing The Windings

Begin with the maximum expected speed of the motor, then add a fudge factor for possible variations, to produce your design-maximum revolutions per minute. Divide this number by 1000 to get "krpm," run your finger across the columns in the motor chart where you find Ke (back-EMF constant in V/krpm), and do some quick multiplications. The result is a range of voltages that are the motor back EMF (BEMF) at your design-maximum rpm.

Next, have your ME give you the maximum torque expected during acceleration to the maximum rpm. Divide this (don't lose track of units) by the torque constant, and the result should be the peak current in amperes. Multiply this by the motor resistance to get the IR drop across the motor windings.

If you're going to be thorough, don't forget that the motor will heat up if you're driving it hard. Without extending this tutorial into all of the calculations needed to compute the motor rms (root-mean-square) current, let's just assume that you heat it up to the motor's design T_{MAX}, frequently 150°C. If you start at room temperature, 25°C, this is a change of 125°C, with the result that the armature resistance can increase by as much as 49%! So now you have the "worst-case" terminal voltage for the system, which is the voltage required to accelerate the

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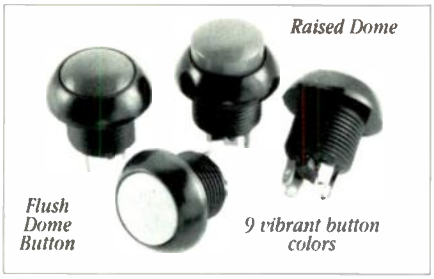

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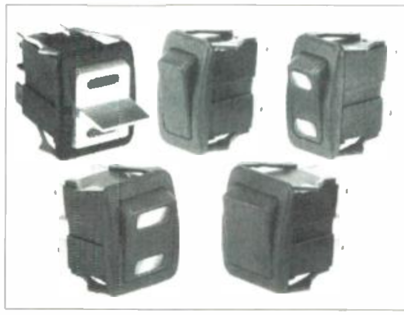

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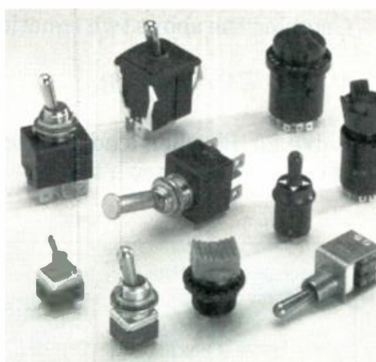

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motor at the maximum rate up to the maximum velocity expected.

Mechanical considerations should give you maximum accelerating torque, T_X, and the top speed, U_X. From these, calculate the maximum motor terminal voltage that must be delivered by the power supply and amplifier combination (V_{TX}) *(Fig. 1)*:

$$V_{TX} =$$

$$V_{AX} + I_X(R_A + R_{TH}) + L_A(dI_X/dt)$$

where V_{AX} = maximum BEMF, or $U_X \times Ke$, and $I_X = T_X/Kt$.

For the power-supply selection, ignore the armature inductance, because the voltage across this will depend on the modulation type. It can be assumed to have an average value of zero under steady-state conditions.

Choosing a power supply is like most other decisions made in pursuit of a goal. All of this motor talk is about defining that goal. Congratulations, you just did that. Now you know the terminal voltage that must be delivered to the motor by the amplifier/power-supply combination if your machine is going to work. Next stop—the servo amplifier.

The Servo Amplifier

Commonly a pulse-width-modulated (PWM) type servo amplifier controls the voltage across the motor to produce a current in the winding. This current, produces torque, which divided by inertia, produces acceleration. When the acceleration is integrated with respect to time, it produces velocity, and then position, and so on.

Suppose that we calculated our design-maximum motor terminal voltage to be 90 V dc. Do you choose an amplifier with a 24- to 90-V dc operating voltage range? You could, but it would be cutting it close to use an amplifier that is about to go into overvoltage shutdown just as it outputs the voltage that the motor needs. The problem is, the amplifier is not just a piece of wire connecting the power supply and the motor.

In a PWM amplifier, MOSFET or IGBT devices are switching away, but rarely get to turn on all of the time (achieve a 100% duty cycle). So, our maximum design voltage might occur at, say, 97% duty cycle, therefore add 3% to the input voltage to the amplifier.

Those amplifiers aren't perfect conductors either. They actually have something called "on-resistance" or "output resistance," R_O *(Fig. 2)*. This is actually a sum of resistances in the transistors and the internal resistors used for current sensing. This output resistance might be in the range of 0.2 to 0.5 Ω. So, take the design-maximum motor current, multiply it by the amplifier output resistance to get the "IR drop." Add that figure to the equation to get the voltage required at the input of the amplifier such that the output produces the design maximum

Linear Power-Supply Regulation And Internal Resistance

The full load current, in terms of the voltage across the load resistance, is found through the equation:

$$I_L = V_{FL}/R_L$$

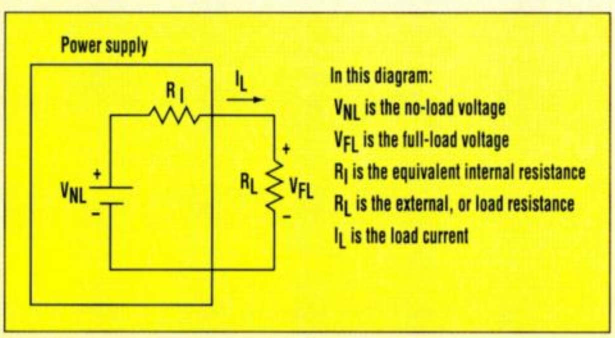
The load current, in terms of the load current and internal, or no-load voltage is given as:

$$I_L = V_{NL}/(R_I + R_L)$$

Combine the above two equations to get:

$$V_{FL}/R_L = V_{NL}/(R_I + R_L)$$

Solve for R_I when load resistance, no-load, and full-load voltages are known to get:



$$R_I = R_L \times [(V_{NL} - V_{FL})/V_{FL}]$$

However, these data are not usually shown on a datasheet. It's more likely you'll find the output (full-load) voltage, current, and percent regulation. So, look again at the diagram above and see that V_{FL} is actually the internal no-load voltage minus the drop across the internal resistance:

$$V_{FL} = V_{NL} - (I_L \times R_I)$$

Rearrange to solve for R_I:

$$R_I = (V_{NL} - V_{FL})/I_L$$

Now, remember that percent regulation was defined as:

$$\text{Percent regulation} = ((V_{NL} - V_{FL})/V_{FL}) \times 100$$

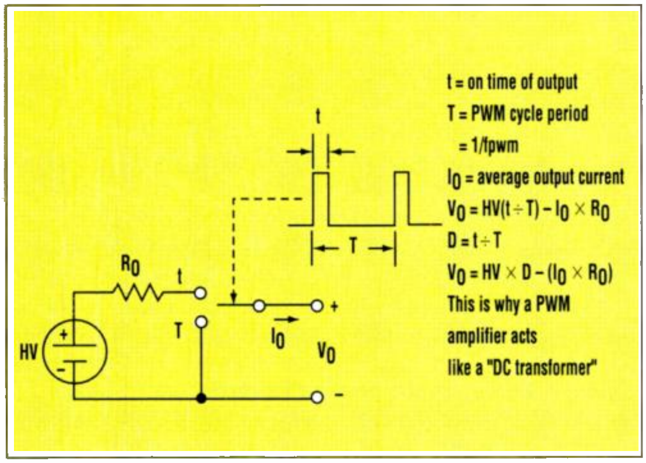
Insert the above term into the equation for R_I and reduce it to give:

$$R_I = (\text{percent regulation}/100) \times (V_{FL}/I_L)$$

The result is a handy equation to model the effective internal resistance of a power supply based on specification-sheet data—namely, full-load voltage and current, and percent regulation.

terminal voltage to do the job at the motor shaft.

Working backward from the motor terminal voltage, through the amplifier to its input terminals, what you get is the minimum voltage required from the power supply. This is the voltage needed at the amplifier's input power terminals to run the motor in the way the ME intended.



2. PWM amplifiers are not perfect conductors. They actually have something called "on-resistance" or "output resistance," which is actually a sum of resistances in the transistors and the internal resistors used for current sensing. This output resistance might be in the range of 0.2 to 0.5 Ω, and must be factored in to get the voltage required at the input of the amplifier such that the output of the amplifier produces the design maximum terminal voltage to do the job at the motor shaft.

If we allow that our 90-V motor might need 20 A for its peak acceleration, we can quickly see why a 90-V amplifier won't work—90 V/0.97 = 92.8 V (remember the maximum duty cycle?). And, 20 A × 0.3 Ω = 6 V. So, the input voltage to the amplifier has to be at least 92.8 V + 6 V= 98.8 V. Let's call that 99. From this you can see that your "90-V" motor will need something more than a 90-V power supply and a 90-V amplifier.

But, before you pick up the phone to order that 99-V power supply, check the datasheet for something called "regulation." This is the no-load voltage minus the full-load voltage, divided by the full-load voltage. Multiply this by 100 and you can express it in a percentage. Obviously, if the voltage didn't change as the load changed, the answer would be 0%.

You will not find this number on a linear power-supply datasheet. What you will find is a number more likely to be from 5 to 15%. This is caused by the internal resistance of the power supply. As long as you select your power supply based on the full-load output voltage, your system will have enough voltage to drive the motor. The effects of non-zero regulation will, however, affect the choice of servo amplifier (*see "Linear Power-Supply Regulation and Internal Resistance," p. 104*).

What about your local electric power company? Read the fine print and you'll find that the 120 V (or 115 V, 100 V, 200 V, 230 V, or 240 V, depending on your country and locale) that is the nameplate voltage on your power delivery system isn't always accurate. It might vary as much as ±10%. Result: all of that stuff about minimum voltage needed at the amplifier terminals, and at the output of the power supply at full load had better be happening at low-line mains voltage, or your control system will be offline when the power dips. In fact, if you examine closely the operating range of equipment made for the U.S., you will commonly see a range of 105 to 132 V ac. This means that for a nominal 120-V supply, the output might dip (120 – 105)/120, or 12.5% from nominal during those brown-outs, and rise 10%, too.

In order to guarantee the minimum power-supply output voltage under the load calculated previously, you must now raise the voltage rating by 12.5% to be prepared for a low-line situation. This will handle the motor needs nicely.

All that's left now is to consider is the amplifier. From 120 V, the voltage can rise 10% to 132 V. We must be sure that the amplifier will be OK with this high-line, no-load voltage before we wrap and bag this design.

This is a key point of linear power-supply selection: when the power line sags, and the load is at a maximum, there must be enough voltage to drive the motor and amplifier. And, when the motor is idle, amplifier disabled, and the power line at its maximum possible voltage, the output will rise to a maximum that cannot damage or disable the amplifier. From a design point of view, pick the power-supply voltage based on expected line excursions and your minimum amplifier input voltage. Then, check the maximum voltage to see if it's OK for your amplifier's operating voltage range (*see "Worst-Case Power-Supply Output Voltage," p. 106*).

Back at the amplifier terminals, two things are happening. Most of the power entering those terminals is converted to watts at the motor terminals, but some of it just makes the amplifier hot. There we go again, those darn amplifiers just aren't perfect. But, they are pretty good, typically 90% or better. That is, 90% of the power going into the amplifier zips right out the other end, into the motor. Furthermore, the PWM action at the amplifier outputs acts like a dc transformer. The constant bus voltage is modulated to appear as a variable voltage from 0 to ±HV. So, the real wattage needed at the amplifier input becomes motor power plus amplifier losses. Divide this actual power by the needed bus voltage, and you'll get the dc current needed from the power supply.

Power-Supply Definition

Elbow room is great. A good design doesn't need to be more tightly defined than necessary, because tight tolerances cost money and narrow the range of operation. If motors had no internal resistance, amplifiers no losses, and power supplies perfectly regulated, none of this would be necessary. We choose not to wait for this to happen, but offer instead the step-by-step procedure for doing by the numbers what we have described above (*see "Power-Supply Definition Procedure," p. 107*). We will not delve into the origins of the maximum revolutions per minute and accelerating torque at this time, but will assume that the mechanical types have dutifully left these data on your desk, along with a datasheet of the motor model of choice.

Current Rating

Now that you know the key voltages for your motion system, it's time to find the current-rating of the power supply. The easy way is to make this the same as the amplifier's peak current. But, in incremental motion systems, this will typically occur only a portion of the overall time, so using this figure will usually result in an oversized (and overpriced) power supply.

Linear supplies are designed to tolerate short-term overloads of 200% to 300% of their continuous ratings. You can use this figure to find a rating closer to your actual needs. The real mechanical watts in your system are determined by the average motor speed, motor current (i.e.: torque), and duty cycle. Try to find a value for the average motor speed and current, multiply these, and get an average power. Take this number and divide it by the power-supply voltage, and you will have an estimate of the supply-current rating. This will generally be somewhat less than the peak amplifier's current value.

Now you have completed the first pass through the process. There were three windings for this motor, weren't there? Did this iteration result in a power-supply voltage range that fits with any servo amplifier you have seen lately? Yes? Jot down the model number, and proceed. If not, do it again! Fact: You are a techno-juggler with at least three pieces to keep in the air at a time. You must pick your parts so that the motor, amplifier, and power supply not only work, but work together simultaneously. But, if it was that easy, everyone would be doing it.

Suppose that you have done a fine job, and now have a motor winding, amplifier, and power-supply choice in hand. Are we there yet? For one motor, sure, but most real systems have multiple axes. Do we repeat this process for each axis, and then add up the watts and buy a power supply to handle all of these at once? Unless your loads are all pumps that run continuously at the design maximum load, the answer is "no." It's time for a major engineering fudge-factor.

Duty-Cycle Fudge Factor

It's called duty cycle (not the PWM type this time). In incremental-motion systems, those factory-automation engineers most frequently encounter, not all axes run all of the time. If your process is very deterministic, you might succeed in calculating the watts per axis, and adding these successfully. But, it's more likely that your machine runs different motion programs depending on a process that changes over time. The best way to sort this out is not on paper, but on the floor (of the R&D lab, in this case).

Begin with a power supply sized for, say, one axis of a three-axis machine. Run your machine as it was intended. Come back in one hour, and place your hand on the power transformer. The copper in its windings is an excellent rms detector of current. We gave it an hour to run because of the long thermal time-constant of the transformer itself. If the transformer is hot, increase the power rating of the supply and try again. If it is cold, you oversized. Downsize the power rating of the supply and try again.

If the transformer doesn't get noticeably warm, you're probably not getting your money's worth. So, you can buy the confidence of over-spec-ing, or play roulette with the winding temperature rating of the transformer. It's up to you. But, the final decision based on multi-axis, duty-cycle demands is tough to make on paper, so allow some lab or floor time to sort this out in the design cycle. The reward will be a power supply that saves you money, and reliably delivers the power you need.

Making Everything Work

Are we done yet? If you know all about grounding, cabling, fusing, and handling regenerative energy, the answer is "yes." If not, continue.

First, cabling. How do we connect all these parts together? Size the wire first. Use the charts in the wire catalogs, and any local electrical codes and wiring practices, if needed. Teflon-insulated wire is best for power wiring due to its very high-temperature and voltage ratings. Next best is cross-linked or irradiated PVC (polyvinyl chloride). Less common, and much cheaper than Teflon, it will withstand solder-iron temperatures without melting. And it's more flexible and easier to strip than the Teflon. The last choice is regular PVC. It's OK for

Worst-Case, Power-Supply Output Voltage

Lowest Output Voltage ($V_{LO(DC)}$) = ($V_{LOWLINE}/V_{NOM}$) × V_{FULL_LOAD}

Highest Output Voltage ($V_{HI(DC)}$) = (V_{HILINE}/V_{NOM}) × V_{FULL_LOAD} × (1 + %R/100)

where:

$V_{LOWLINE}$ = low-line mains voltage
V_{NOM} = nominal mains voltage
V_{HILINE} = high-line mains voltage
V_{FULL_LOAD} = full-load supply output voltage
%R = power-supply regulation in percent

Example:

A power supply has these specs: 65 V dc, 8 A, and 5% regulation.

$V_{LOWLINE}$ = 105 V ac
V_{NOM} = 120 V ac
V_{HILINE} = 132 V ac

Lowest Output Voltage = 56.9 V dc
Highest Output Voltage = 75.1 V dc

Compare the minimum required voltage at the amplifier input terminals with the Lowest Output Voltage to check adequacy.

Compare the Highest Output Voltage with the amplifier's operating voltage range to ensure that the amplifier will not shut down due to an overvoltage condition.

lower voltage, in cooler-running or lower-powered equipment, but not a good choice for anything connected to the mains, or above, say 75 V dc, or so.

Next, PWM amplifiers put fast ripple currents into power supplies, in addition to the average currents they draw (the ones we have been discussing). To keep these currents from "talking" to adjacent cables, twist power-supply leads (one-to-three turns per inch) together. For newer CE-compliant applications, consider using shielded cables to reduce EMI emissions from these wires. Typically, these are going to be bigger wires (AWG 18 to 12), so it's best not to try soldering them, but use crimp-on connectors to mate with screw-lugs, or Euro-style compression connectors instead.

Fusing

Most people think that the fuse is meant to protect their equipment. In fact, the prime function of the fuse is to protect the world from your equipment when it fails. The survival of your machine is secondary. At the minimum, you will want a fuse between the mains and your final choice of power supply. Given the inrush currents associated with capacitor-input supplies, this will be a time-delay fuse.

Choose the current rating based on the power-supply nameplate rating, and add 25%. Remember, a fuse should only carry 80% of its rated current continuously. If you have a 500-W power supply operating from 120-V ac mains, the rated line current would be 500/120 or 4.17 A. Divide this by 0.8 to get 5.21 A. Make the choice between a 5- or 6-A fuse based on how much of that power-supply rating you're likely to use in practice.

The choice of a second tier of fuses to protect each individual amplifier is up to you. Depending on the cost or value you assign to an individual amplifier, you can let the pc-board etch be the fuse of final resort. And, you only need to put a single fuse in the mains wiring to the power supply, or fuse each amplifier individually. Given that

Power-Supply Definition Procedure

1. Find the maximum motor armature voltage:

$$V_{AM} = V_{DM} \times Ke$$

where:

V_{AM} = maximum armature voltage
V_{DM} = design-maximum rpm (in krpm)
Ke = V/krpm (volts per rpm/1000)

Add at least 10% to compensate for manufacturing tolerances, and to include a little operating headroom for the control system.

2. Find maximum IR drop (V_{RM}) in motor resistance:

$$I_{DM} = T_{DM}/Kt$$

where:

I_{DM} = design-maximum current
T_{DM} = design-maximum torque
Kt = torque constant
T_{DM} and Kt should use same units for torque

$$V_{RM} \approx 1.5 \times I_{DM} \times R_A$$

where:

V_{RM} = maximum IR drop
R_A = armature resistance
1.5 = addition of 50% to V_{RM} to cover hot-motor scenario.

3. Find design-maximum motor terminal voltage:

$$V_{TM} = V_{AM} + V_{RM}$$

where:

V_{TM} = design-maximum motor terminal voltage

Multiply this by maximum current to get armature wattage. Now you know the maximum power input to the motor terminals in watts.

4. Find minimum power-supply voltage at amplifier input terminals:

$$HV_{MIN} = (V_{TM}/D_M) + (I_{DM} \times R_O)$$

where:

HV_{MIN} = minimum power-supply voltage at amplifier input terminals
D_M = maximum duty cycle (e.g. 0.97 for 97%)
R_O = amplifier "on" resistance

5. Find full-load, power-supply output voltage:

$$V_{FL} = HV_{MIN} \times (V_{NOM}/V_{LOWLINE})$$

where:

V_{FL} = full-load power-supply output voltage
V_{NOM} = nominal mains voltage
$V_{LOWLINE}$ = low-limit mains voltage

In the power-supply catalog find a device with a full-load output voltage near to this. Take this number, and calculate the high-line, no-load voltage($V_{HI(DC)}$) according to the procedure already outlined *(see "Worst-Case Power-Supply Output Voltage," p. 106)*. This is the high-line voltage that the amplifier must tolerate without going into shutdown.

the amplifiers usually shut down with internal (or external) short circuits, and that total, catastrophic failure is rare, most users decline the individual fuse per amplifier. It's your call.

Wiring And Grounding

Don't daisy-chain wires from power supply, to amplifier 1, and then onto amplifier 2, etc. Instead, use a star system, with one twisted pair from each amplifier connecting to the terminals of the power-supply filter capacitor.

Also, ground your system properly. Remember, there are two currents in those wires between the amplifiers and the power supply: slow currents, or the average currents that drive the motor, and fast currents, the ones you can't see, but exist due to the switching of the transistors in the amplifiers. The slow currents make measurable IR drops between the ends of the cables. The fast currents produce even bigger voltage spikes in the inductance of the wires.

Enter relativity. The voltage between the ends of the power wires are relative to those ends. Ground the negative terminal of the power-supply capacitor, and these voltages will appear between the amplifier ground terminals, and chassis (general electrical system) ground.

From the viewpoint of the amplifier circuits (remember relativity), the world just got very noisy. From where the control system sits, the amplifier looks really noisy. You can eliminate this noise by disconnecting the power-supply capacitor from ground, instead grounding each amplifier with its own short grounding conductor to a local star ground terminal. This way, the wiring noise will be seen between the capacitor negative terminal and ground, but there it won't matter to the amplifiers, or to the control system.

Regeneration

Finally, because this is a motion-control system with stored mechanical energy, there's regeneration to consider. Your servo amplifier is a two-way street when it comes to power. Most of the time you deliver power to the load. But, once you accelerate a load to a given speed, or elevate it to some height against the pull of gravity, you have stored mechanical energy that must now dissipate to bring the load to rest. This energy flows from the load back into your system.

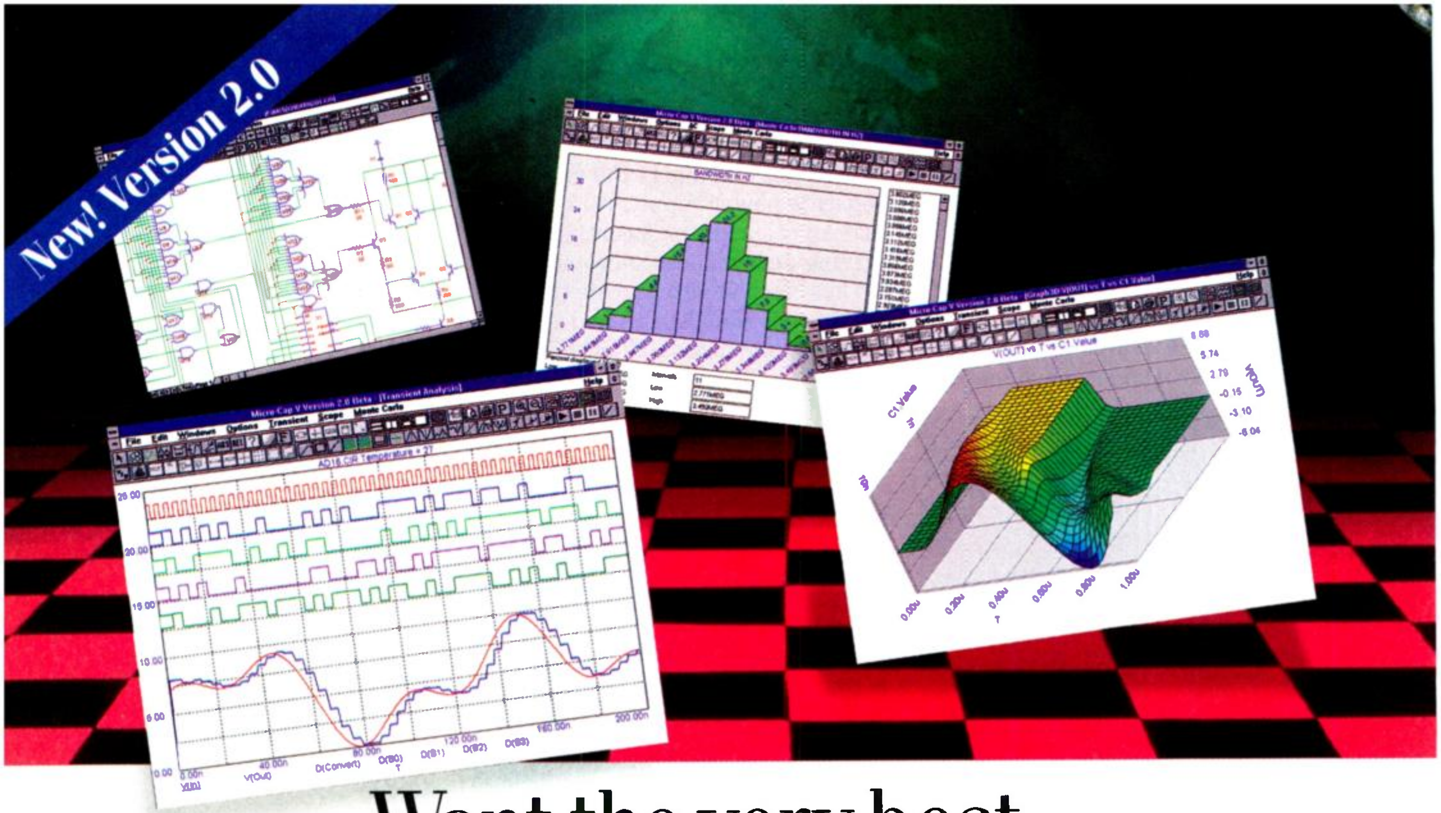
The motor handles this two-way power delivery easily, as does your four-quadrant PWM servo amplifier. But, when you get to the power supply, you're looking into the business end of a rectifier that only passes power in one direction—from the power line into the filter capacitor. In the case of regeneration energy, it's a brick wall. The solution is a "dumper," or regenerative energy dissipater.

These devices connect across the filter capacitor terminals, and rapidly switch a high-power resistor across the terminals to dissipate the energy as heat. As more energy comes back from the load, the dumper switches with an ever-increasing duty cycle to mimic a resistor with a lower and lower resistance. The effect is to have a rheostat across the cap that is electrically variable to satisfy the Ohm's law solution $R = E/I$; where E is the bus voltage during regeneration, and I is the current coming from the motor during deceleration. As soon as the load is brought to rest, the "pump-up" of the power supply stops, the voltage drops, and the dumper turns off.

These devices are common accessories from amplifier makers, and found as part of the amplifier, or as external accessories. They are usually adjusted to a voltage that is below the amplifier's shut-down voltage, but above any steady-state, high-line, and no-load voltages. The peak power dissipated by these devices is very high, and they are intended to operate only during deceleration intervals when mechanical energy is to be dissipated.

By now, you should know enough to pick your motor winding, select and size a power supply, roughly spec a servo amplifier, and wire the whole thing together. You're now ready for your next assignment—making it all work! But that's another story.

Jim Woodward is applications manager for motion-control products at Copley Controls Corp., Westwood, Mass. He manages the applications lab where Copley servo amplifiers are set to custom requirements. Actively involved in the field of motion control since 1979, he received a BSEE from Northeastern University, Boston, Mass., in 1982.



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The BAI Intellidrive series of indexers, which measure 7.25 by 5 by 2.88 in., operate in velocity, torque, indexing, and teach modes to drive both brush and brushless servo motors.

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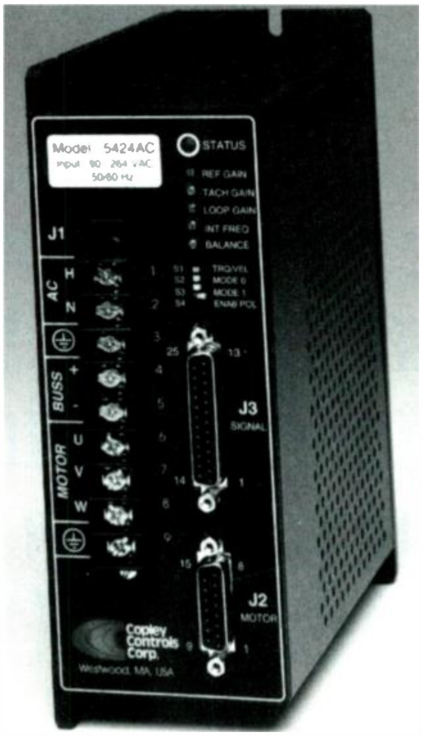
Aerotech Inc., 101 Zeta Dr., Pittsburgh, PA 15238-2897; Rob Sobek (412) 963-7470; fax (412) 963-7459; e-mail: aerotech@aerotechinc.com; www.aerotechinc.com.

CIRCLE 528

Servoamp Features Remote Speed/Torque Mode Switching

The Model 5424AC servoamplifier takes any ac input over the 90- to 264-V range, and features remote switching between speed to torque modes for fastener-tightening applications. The device eliminates the need for a separate power supply, yet develops ±20 A peak and ±10 A continuous for driving dc brushless servomotors to 2.5 hp. The unit also provides isolated outputs of 5 V at 200 mA and ±10 V at 5 mA for encoder or Hall-effect-sensor excitation. The amplifier's PWM frequency is 12.5 kHz, current-ripple frequency is 25 kHz, and the bandwidth is 3 kHz. Measuring 7.50 by 2.72 by 7.00



in., the unit can drive motors with inductances over the 0.4- to 40-mH range. An internal frequency-to-voltage converter eliminates the need for a tachometer. Pricing is $595 each per 100; delivery is from stock to four weeks.

Copley Controls Corp., 410 University Ave., Westwood, MA 02090; Dean Crumlish (781) 329-8200; fax (781) 329-4055; e-mail: sales@copleycontrols.com; www.copleycontrols.com.

CIRCLE 529

PWM ICs Speed Development Time And Lower Costs

The SA868 and SA869 are three- and single-phase motor controllers, respectively. They use an architecture that includes two new waveform options, eliminating the need for a micro-

(continued on page 112)

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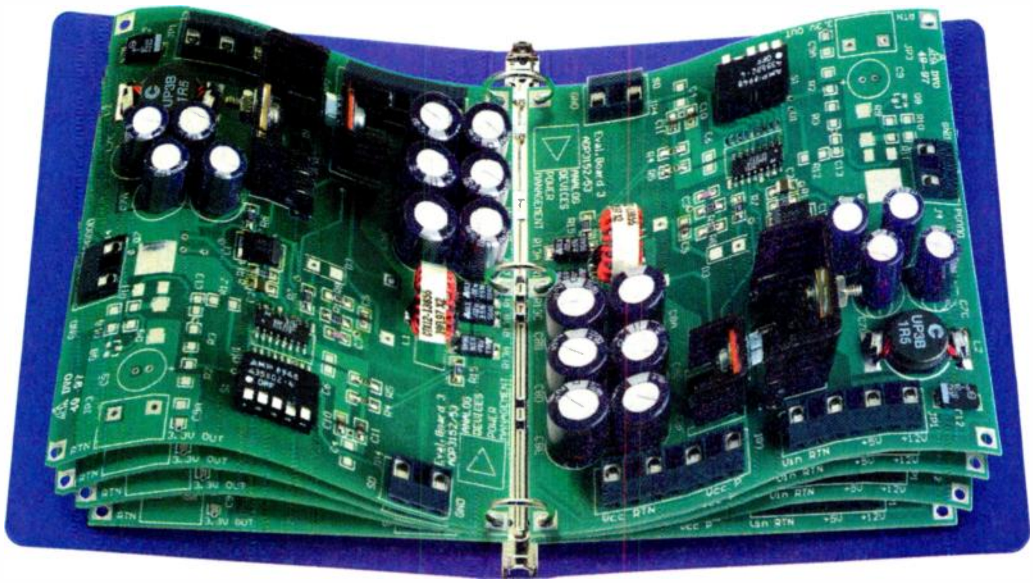

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(continued from page 110)

processor. Targeting control applications in washing machines, fan drives, and conditioning systems, the devices also can be integrated into non-motor applications such as uninterruptible power supplies and static inverters.

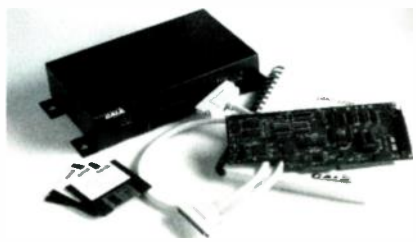
The four available waveforms are: the triplen power option, the dead-banded triplen option, pure sine wave, or custom. A patented acceleration and deceleration algorithm ensures motor-speed changes are executed at a safe, user-specified and resistor-programmable rate. The PWM carrier frequencies of up to 24 kHz allow ultrasonic operation and a power frequency of up to 4 kHz for motor speeds in excess of 200,000 rpm. The output resolution is 16 bits and using a 4-bit input the user can select from 15 custom speeds mask programmed on the chip. An evaluation board, the PWM86X, also is available.

Pricing for the SA868 in a 24-pin, SOIC plastic package is $3.63 each per 1000; the SA869 in a 20-pin, SOIC plastic package costs $2.45 each per 1000; and the evaluation board costs $200.

GEC Plessey Semiconductors, *1500 Green Hills Rd., Scotts Valley, CA 95067; Kim Norton (408) 438-2900; www.gpsemi.com.* **CIRCLE 530**

Controllers Get Upgraded To 80 I/Os With Multitasking

Now available with up to 80 I/Os containing firmware that doubles the number of multitasking threads, the DMC-1700 series is able to control from one to eight axis. The units come standard with eight uncommitted dig-



ital inputs, eight digital outputs, and eight analog inputs. The buffered I/O is accessible via two 50-pin ribbon cables that plug directly into OPTO 22 PO Series or Grayhill 70 or HL Series I/O expansion racks. Programs can be stored in nonvolatile memory—up to eight can be executed concurrently. Features include trigonometric functions and IF/ELSE statements for nested statements up to 255 levels deep. Pricing ranges from $1195 for the single-axis version up to $3295 for the eight-axis version.

Galil Motion Control, *203 Ravendale Dr., Mountain View, CA 94043; (800) 377-6329; fax (650) 967-1751; www.galil.com.* **CIRCLE 531**

Integrated Development Suite Speeds Control-System Design

The latest version of dSPACE Real-Time Interface (RTI) 3.0 enables generated code from control-system block diagrams (modeled in MathWorks Simulink/Stateflow/Real-Time Workshop) to run on dSPACE's control-system prototyping hardware for real-

(continued on page 113)

DESIGN NOTES

Micropower 600kHz Step-Up DC/DC Converter Delivers 5V at 1A from a Li-Ion Cell – Design Note 179

Steve Pietkiewicz

Linear Technology introduces a new micropower DC/DC converter designed to provide high output power from a single cell or higher input voltage. The LT®1308 features an onboard switch capable of handling 2A with a voltage drop of 300mV and operates from an input voltage as low as 1V. The LT1308 features Burst Mode™ operation at light load; efficiency is 75% or better for load currents of 1mA. The device switches at 600kHz; this high frequency keeps associated power components small and flat; additionally, troublesome interference problems in the sensitive 455kHz IF band are avoided. The LT1308 is intended for generating power on the order of 2W to 5W. This is sufficient for RF power amplifiers in GSM terminals or for digital-camera power supplies. The LT1308 is available in the 8-lead SO package.

Single Li-Ion Cell to 5V/1A DC/DC Converter for GSM

GSM terminals have emerged as a worldwide standard. A common requirement for these products is an efficient, compact, step-up converter that develops 5V from a single Li-Ion cell to power the RF amplifier. The LT1308 performs this function with a minimum of external components. The circuit is detailed in Figure 1. Many designs use a large aluminum electrolytic capacitor (1000µF to 3300µF) at the DC/DC converter output to sustain the output voltage during the transmit time slice, since the amplifier can require more than 1A. The output capacitor, along with the LT1308 compensation network, serves to smooth out the input current demanded from the Li-Ion cell. Efficiency, which reaches 90%, is shown in Figure 2. Transient response of a 0A to 1A load step with typical GSM profiling

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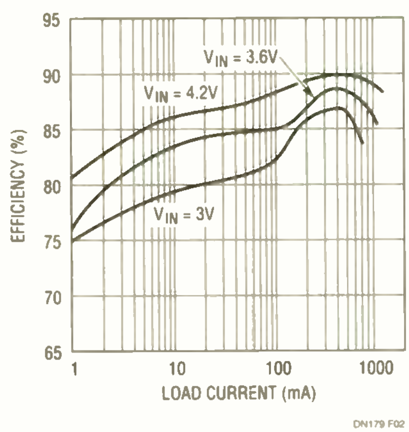
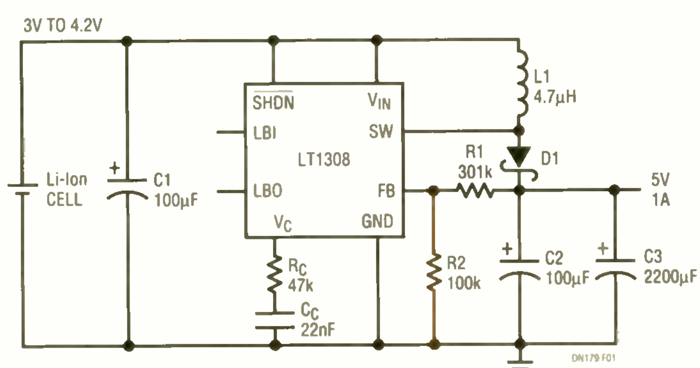


Figure 2. Efficiency of Figure 1's Circuit Reaches 90%



C1,C2: AVX TPSD107M010R0100
D1: INTERNATIONAL RECTIFIER 10BQ015
L1: COILTRONICS CTX5-1
COILCRAFT DO3316-472

Figure 1. Single Li-Ion Cell to 5V/1A DC/DC Converter

Circle No. 190

(1:8 duty cycle, 577μs pulse duration) is depicted in Figure 3. Voltage droop (top trace) is 200mV. Inductor current (bottom trace) increases to 1.7A peak; the input capacitor supplies some of this current, with the remainder drawn from the Li-Ion cell.

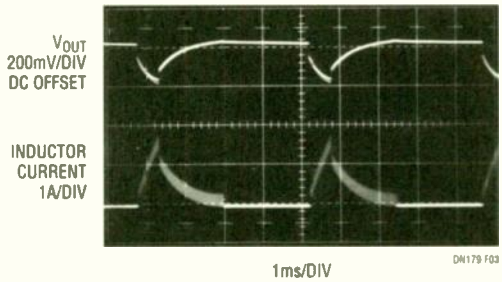


Figure 3. Transient Response of DC/DC Converter: V_{IN} = 3V, 0A to 1A Load Step

2-Cell Digital-Camera Supply Produces 3.3V, 5V, 18V and –10V

Power supplies for digital cameras must be small and efficient while generating several voltages. The DSP and logic need 3.3V, the ADC and LCD display need 5V and biasing for the CCD element requires 18V and –10V. The power supplies must also be free of low frequency noise, so that post filtering can be done easily. The obvious approach, to use a separate DC/DC converter IC for each output voltage, is not cost effective. A single LT1308, along with an inexpensive transformer, generates 3.3V/200mA, 5V/200mA, 18V/10mA and –10V/10mA from a pair of AA or AAA cells. Figure 4 shows the circuit. A coupled-flyback scheme is used, actually an extension of the SEPIC (single ended primary inductance converter) topology. The addition of capacitor C6 clamps the SW pin, eliminating a snubber network. Both the 3.3V and 5V outputs are fed back to the LT1308 FB pin, a technique known as split feedback. This compromise results in better overall line and load regulation. The 5V output has more influence than the 3.3V output, as can be seen from the relative values of R2 and R3. Transformer T1 is available from Coiltronics, Inc. (561-241-7876). Efficiency vs input voltage for several load currents on both 3.3V and 5V outputs is pictured in Figure 5. The CCD bias voltages are loaded with 10mA in all cases.

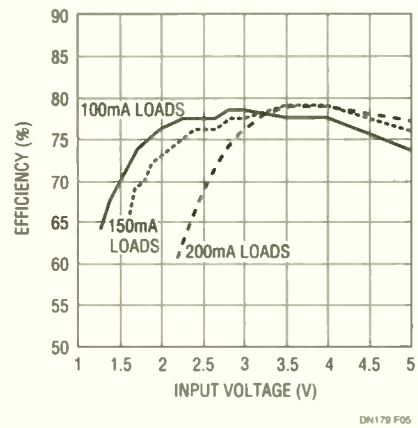


Figure 5. Efficiency vs Input Voltage for 100mA, 150mA and 200mA Loads on 3.3V and 5V Outputs

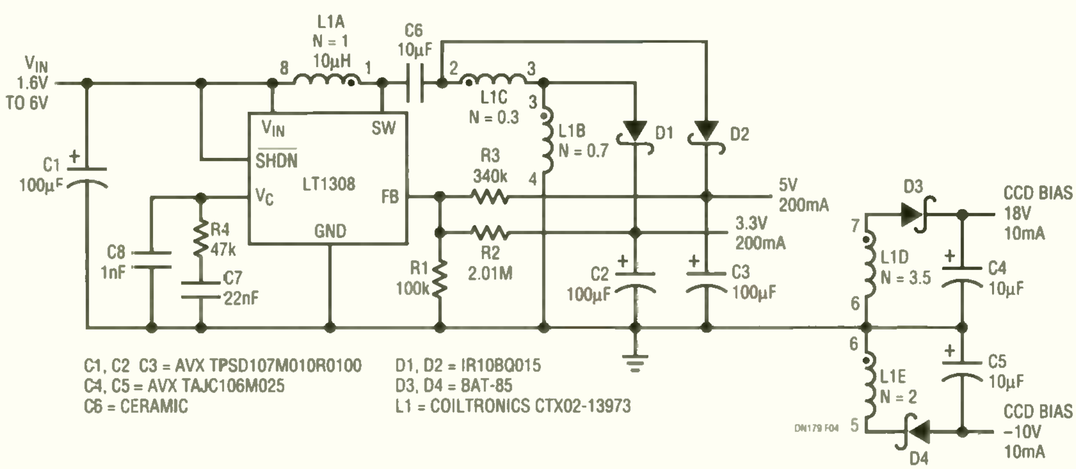


Figure 4. This Digital-Camera Power Supply Delivers 5V/200mA, 3.3V/200mA, 18V/10mA and –10V/10mA from Two AA Cells

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MOTION CONTROL

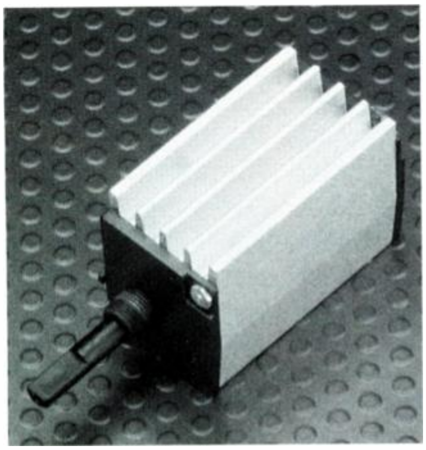
(continued from page 112)

time execution. Using the cross-linked development suite accelerates the design, debugging, and integration process for complex systems to produce more robust designs in less time. Among dSPACE's features are support of triggered and enabled subsystems through external hardware interrupts, intuitive dialogs, and automatic code generation for I/O drivers. Pricing for Simulink and Stateflow starts at $1995; Real-Time Workshop starts at $9995 with a single-seat processor license; dSPACE starts at $1700 on Windows 95 and NT.

The MathWorks Inc., *24 Prime Park Way, Natick, MA 01760-1500; (508) 647-7000; fax (508) 647-7001; e-mail: info@mathworks.com.*
CIRCLE 532

Motor-Speed Controller Presents Low-Cost Alternative

The MSC Series of motor-speed controllers is offered as a low-cost method of varying the speed of a fan or other motor load. Control is provided by an



on-board potentiometer on/off switch that's threaded to allow panel mounting. An extruded-aluminum housing allows the controller to be used in ambient temperatures of up to 85°C, while outputting over the ranges of 1 to 3 A or 2 to 4.5 A. The unit operates off 120 to 230 V ac. Electrical connections are made via 0.25-in. male quick-connect terminals. Pricing is $14.28 each per 100.

SSAC Inc., *P.O. Box 1000, Baldwinsville, NY 13027; Dave Eastwood (800) 377-7722; fax (315) 638-0333; www.ssac.com.* **CIRCLE 533**

MOTION CONTROL

Low-Loss IGBTs Save On Power Consumption

The ITS range of IGBTs have a switching loss of 2.85 mJ at 35 A and target ac motor-control applications. Able to drive motors rated from 0.5 to 10 hp, the devices feature a short-circuit-withstand time of 10 µs, a typical saturation voltage of 2 V at 35 A, and operating voltage and current options of 600 V and 1200 V at 8 to 60 A. Package options include TO-220, TO-247, and TO-264. Pricing ranges from $0.81 each per 5000 to $0.65 each per 10,000.

***Mitel Semiconductor**, 1500 Green Hills Rd., Scotts Valley, CA 95067; (408) 438-2900; www.semicon.mitel.com.* **CIRCLE 534**

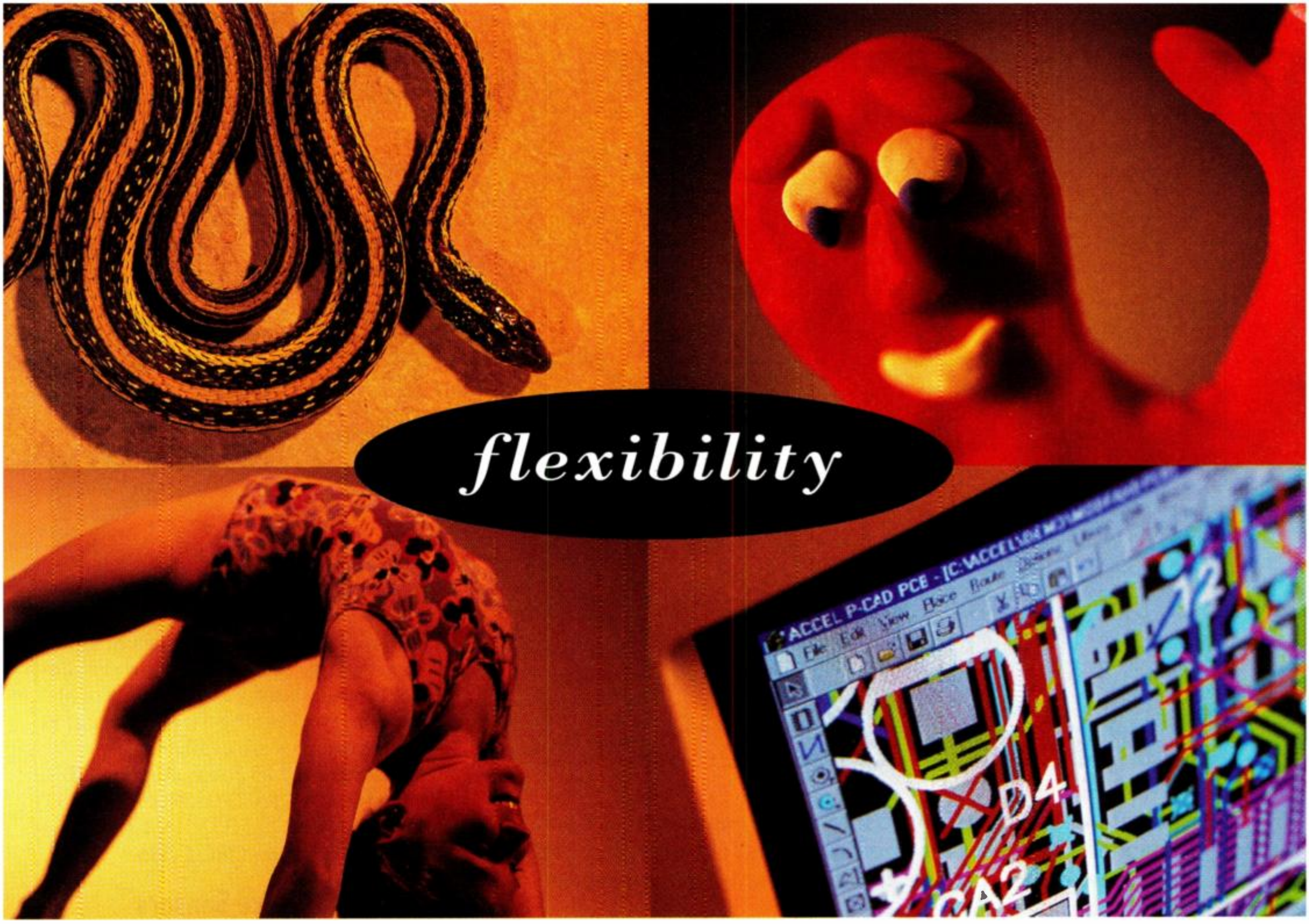
Rectifier Package Lowers Cost Of High-Power Designs

Targeting motor-drive and welder applications, the SMD-10 rectifier package handles from 5 to 50 kW. The first offering, the IRG4ZC70UD CoPack IGBT, is rated at 100 A at $T_C = 25°C$, with a $V_{CE(ON)}$ of less than 1.9 V. The device switches off in 130 ns at 150°C, with a total on/off loss of 0.68 mJ/A off a 360-V bus, or 0.9 mJ/A off a 480-V bus. IGBT/HEXFRED CoPaks also are available. Designed for flexibility, the package puts the power and control connections on opposite sides for ease of paralleling. Other features include 11-kW inverter stages with 30-nH inductance and a package inductance of 2 nH. Pricing is $12.90 each per 1000.

***International Rectifier**, 100 N. Sepulveda Blvd., 8th. Floor, El Segundo, CA 90245; ProCenter (310) 252-7105; Fax on Demand (310) 252-7100; www.irf.com.* **CIRCLE 535**

Hall-Effect Sensor Is Fully Programmable

The MLX 90215VA is a linear, fully-programmable Hall-effect sensor in a single-chip CMOS IC with no need for discrete components. Programmable functions include offset calibration, gain adjustment, temperature compensation, and clamping output voltage. Active error-correction circuitry eliminates offset errors, while internal digital-to-analog converters allow the device to be programmed in its own *(continued on page 116)*



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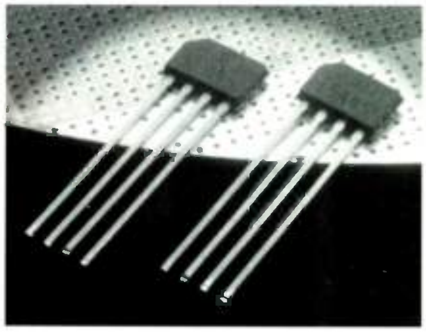
(continued from page 114)
operating environment. The system can be trimmed to an initial error of ±0.01% and ±0.4% over the standard automotive temperature range of –40°

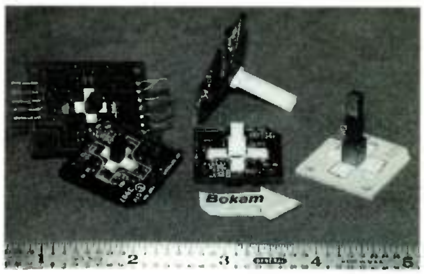


to 150°C. In addition, programmable temperature compensation brings the system temperature coefficient to almost zero. Pricing is $3 each per 10,000; samples are available now.

Melexis Inc., 15 Sutton Rd., Box 837, Webster, MA 01570-0837; (508) 943-9430; fax (508) 943-0487; www.melexis.com. ***CIRCLE 536***

Thick-Film Force Sensors Target Control Applications

The Aurora line of solid, ceramic, two- or three-axis force sensors are based on thick-film technology and provide a distinct linear output on all axes for

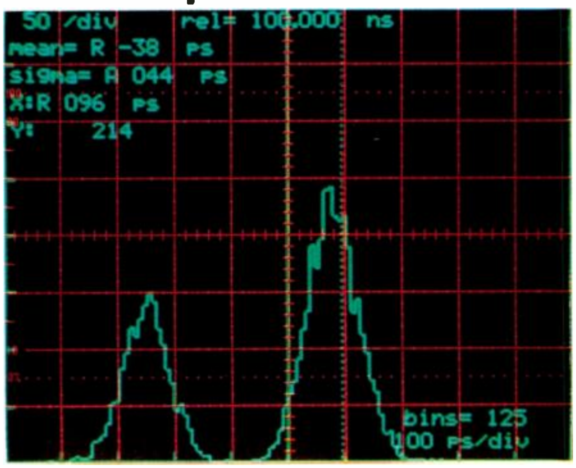


precise, smooth motion control. Tested to 10 million cycles on all axes, the device comes with temperature compensation for operation at temperatures up to 450°F. Packaging options range from sensor alone to a complete motion-control package. Pricing is from $20 to $100, depending on level of integration and quantity. Delivery is from six to eight weeks.

Bokam Engineering, 3633 West MacArthur Blvd., Suite 412, Santa Ana, CA 92704; (714) 513-2200; fax (714) 513-2204; e-mail: bokam5@aol.com; www.bokam.com. ***CIRCLE 537***

A picture is worth a thousand points in a time interval measurement.

SR620 Output



HP5370B Output

100.038 ns

The SR620 brings graphic statistical analysis to time interval and frequency measurements. The SR620 shows you more than just the mean and standard deviation - multimode frequency distributions or systematic drift for example. Histograms or time variation plots are displayed on any X-Y oscilloscope, complete with Autoscale, Zoom, and Cursor functions. Hardcopy to plotters or printers is as easy as pushing a button.

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Circle 520

Improvements On The Circuit-Break Locator

DAVID C. SALERNO
Unitrode Corp., 7 Continental Blvd.,
Merrimack, NH 03054; e-mail: salerno@unitrode.com

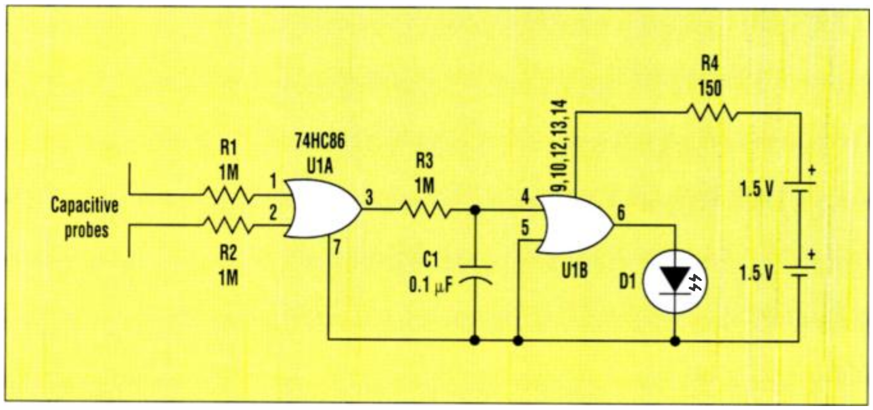
With a little tweaking of the test hook and gimmick capacitor, I was able to get W. Stephen Woodward's unique open-bulb detector circuit working properly (*"Circuit Locator For The Holidays,"* ELECTRONIC DESIGN, *Nov. 17, 1997, p. 99*). However, in practice, I found it can be difficult to interpret the LED readings. The problem is that, due to the weak and distorted sinusoidal input signals, the XOR gate's output is always switching. This causes the LEDs to be duty-cycle-modulated at 120 Hz. The variation in duty cycle causes one LED to be brighter than the other. (neither LED is ever fully on or off). A change in the relative intensity of the two LEDs indicates a bad bulb (i.e., an open circuit).

By adding a simple RC low-pass filter to the output of the first XOR gate and feeding the filtered signal to one of the inputs of a spare XOR gate (leaving the other input tied High or Low), the circuit performance can be greatly improved. In the improved circuit, the low-pass filter (R5 and C2) converts the duty-cycle-modulated signal to an equivalent DC voltage *(Fig. 1)*. The second XOR gate serves as a comparator to turn on one LED or the other, depending on whether the input is High or Low. This eliminates any 120-Hz switching or duty-cycle modulation, resulting in easy-to-interpret LED readings. One LED is fully on and the other is fully off, depending on what phase of the ac line you're probing with the test hook.

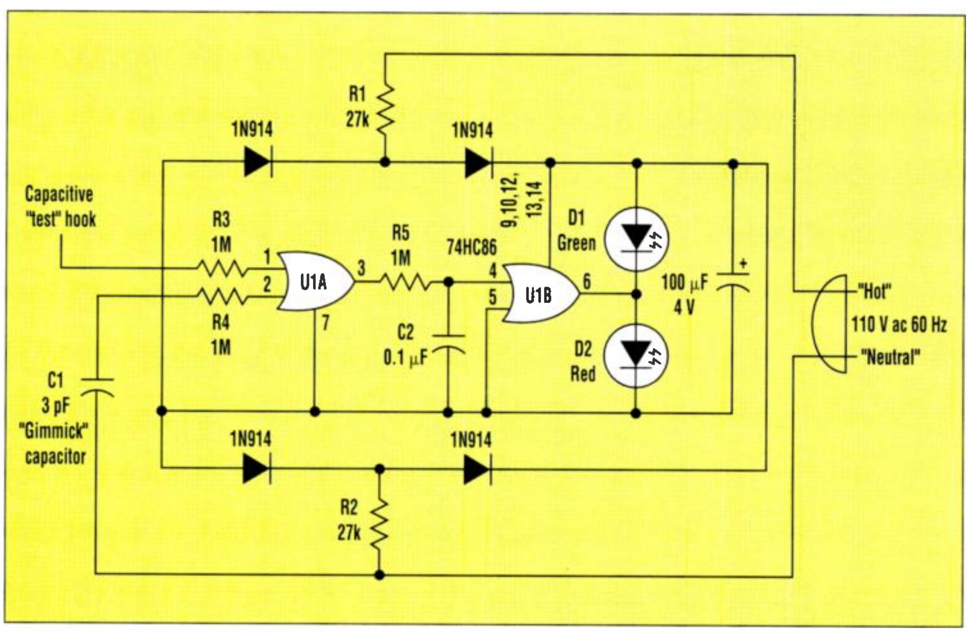
As an applications engineer for portable products, I felt obliged to design a similar circuit that would operate from batteries, eliminating the need for an ac cord *(Fig. 2)*. It operates on the same basic principle as the ac-powered version, except it uses two small 1.5-V batteries and requires fewer parts. Rather than relying on one side of the ac line as a reference, it has two capacitive "probes" to sniff out a differential voltage in the circuit under test. Therefore, only one LED is required, which only lights when there's a differential voltage present, indicating an open circuit. This lengthens battery life. The leakage currents on the two floating XOR inputs seem to be matched well enough whereby the gate's output remains in the low state when there's no differential voltage impressed across the probes.

The low-pass filter (R3 and C1) and the second XOR gate operate in the same manner as the previous design. Only one LED is required in this design, because the LEDs aren't needed to clamp the voltage across U1, as they are in the ac-powered version. (A second LED can be added from U1 pin 14 to pin 6 if desired, to retain the traditional red and green Christmas colors. In this case, the second LED will be lit until an open circuit is detected.)

Resistor R4 is located such that it limits the current to



2. In this simpler, battery-powered detector circuit, a single LED indicates an open bulb.



1. Adding a low pass filter (R5, C2) to produce a dc voltage and utilizing a spare XOR gate (U1B) as a comparator produce easier-to-interpret LED readings in this improved circuit-break locator.

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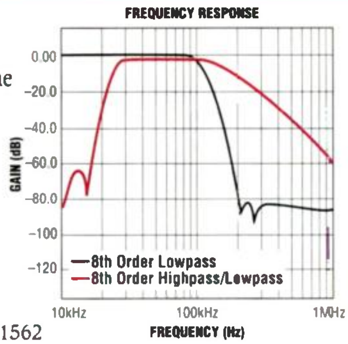

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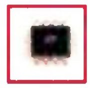
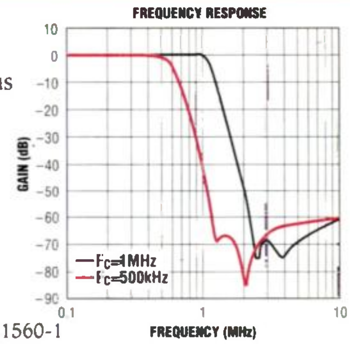


Actual Size



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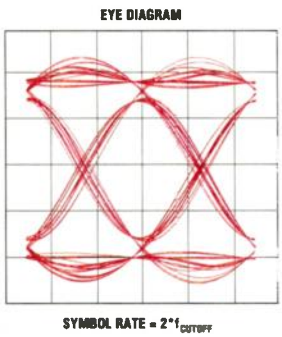

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the LED as well as into U1. This eliminates the possibility of high cross-conduction currents in U1, resulting from the floating CMOS inputs. Another benefit of putting R4 in this circuit location is that when D1 turns on, the resulting current causes U1's supply voltage to drop. This lowers the logic-High threshold voltage, providing hysteresis to help U1B switch cleanly.

To detect an open bulb in a string of lights, simply place the probes next to the two wires feeding the bulb under test. The 1-MΩ resistors (R1 and R2) protect U1's inputs from ESD damage. I used the leads of the 1-MΩ resistors, bent apart at 90°, as the probes. It works best when the probes are close to and parallel with the wires under test.

Circle 521

Improve Group Delay Response In The Anti-Aliasing Filter

NICHOLAS C. GRAY AND TERRANCE SMITH
National Semiconductor Corp., 2900 Semiconductor Dr., Santa Clara, CA 95052-8090; (408) 721-6962 / (408) 721-8621; e-mail: ngray@redwood.nsc.com.

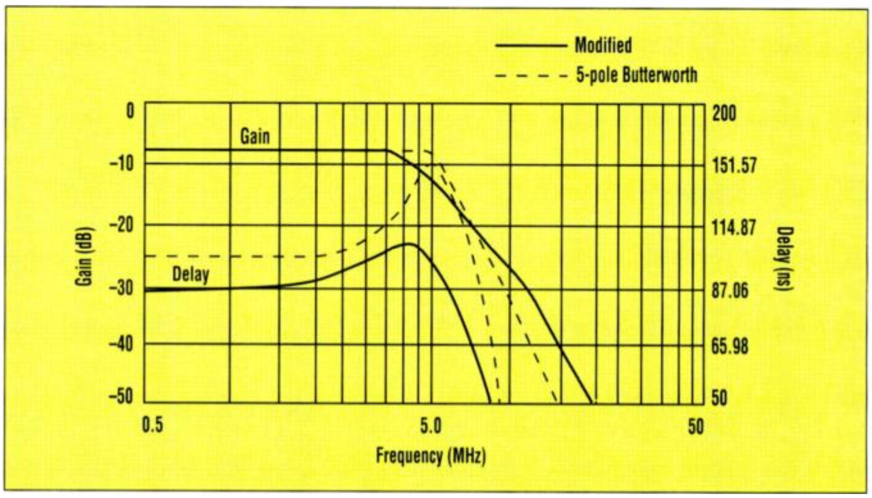
You can dramatically improve the group delay performance of a video digitizer by using the anti-aliasing filter shown *(Fig. 1)* instead of a Butterworth anti-aliasing filter. Anti-aliasing filters are necessary in most video-acquisition circuits to prevent signals at frequencies greater than 1/2 the sampling rate from contaminating desired signals during the sampling process. However, anti-aliasing filters introduce phase errors that may add undesired transients to the reproduced picture.

To accurately sample a signal and eliminate aliasing, you must reduce undesired signals at the quantizer input to acceptable levels. To reduce energy at frequencies greater than those desired at the ADC input, it's common to employ an anti-aliasing filter in the analog signal path prior to quantization. For NTSC (National Television Standards Committee—used in the United States and Japan) and PAL (Phase Alternate Line—used in much of Europe) video systems, the filter cutoff frequencies are about 4 to 6.5 MHz, depending upon the video system.

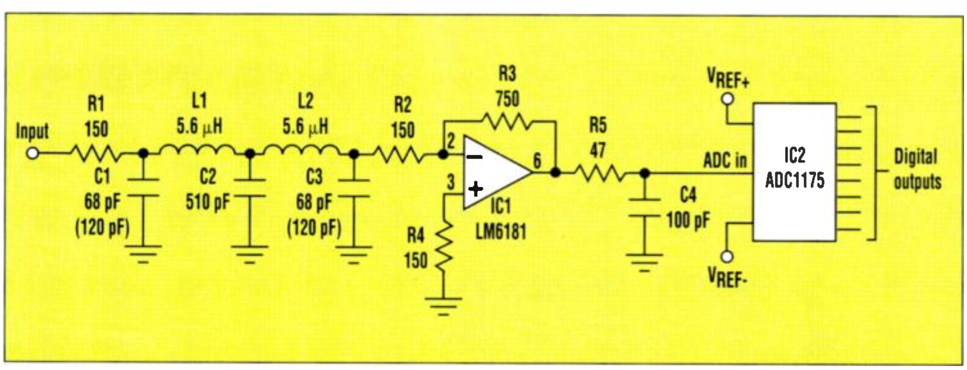
Practical filter design requires a compromise between gain flatness in the passband and stopband slope. To overcome these limitations, the sampling rate is often four or more times the highest frequency of interest. For example, in NTSC systems with a color subcarrier of 3.58 MHz, it's conventional to use a sampling rate of 14.318 Msamples/s.

The choice of filter to be used depends upon which characteristics must be maintained and those that can be somewhat compromised. Chebyshev and elliptic filters feature very steep stopband slopes, but also have a very nonlinear phase response. For video systems, this nonlinear phase response is catastrophic because phase and frequency, as well as amplitude, provide critical information.

The Butterworth filter has been widely used as the anti-aliasing filter in video systems because of its flat passband response and relative insensitivity to component tolerance. The Butterworth design, however, exhibits more group delay near cutoff than most video systems can accept.

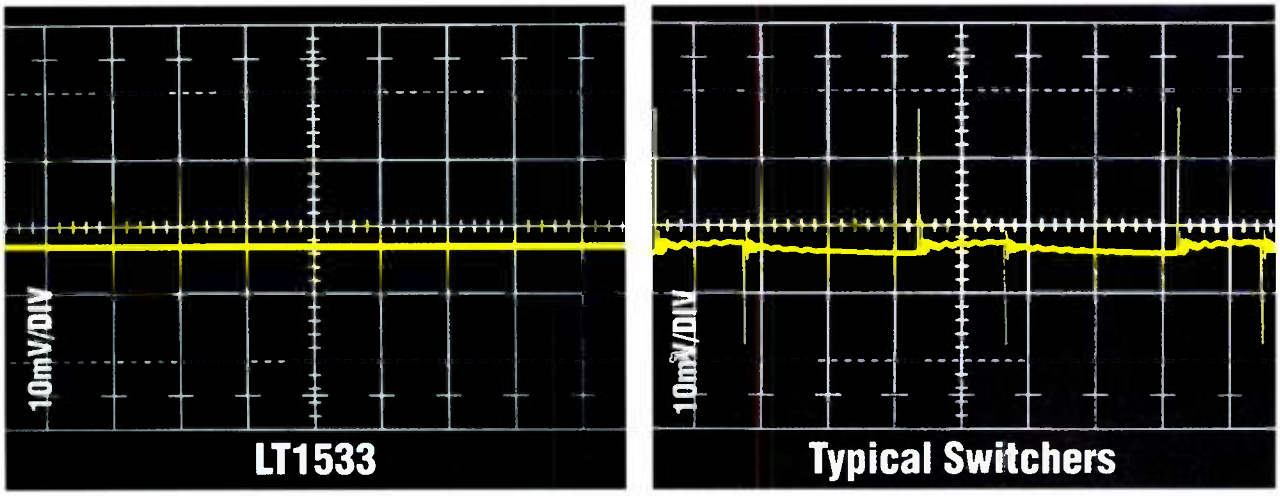


2. Comparing the modified filter response with that of a normal Butterworth filter shows significantly improved group delay response with little sacrifice in gain roll-off.



1. The group delay of this 5-pole anti-aliasing filter were improved by modifying the values of the input and output capacitors. Output filter R4C4 helps to isolate the filter amp while improving phase margins.

100µV Output Noise Switching Regulator



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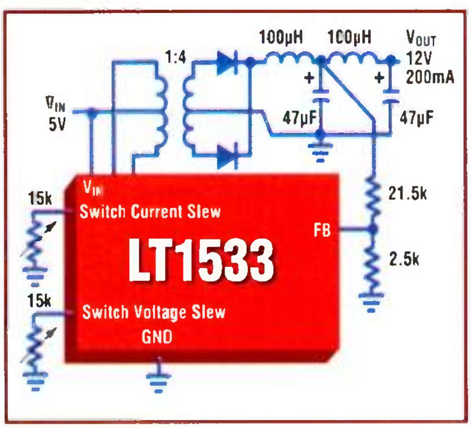

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A 5-pole filter with a Butterworth-like amplitude response and reduced phase lag near the 4-MHz cutoff is shown in Figure 1. If you modify the Butterworth filter so that capacitors C1 and C3 are about half of the "ideal" value, you can get a modified phase response that improves group delay and transient response. R1 and R2 are termination resistors for the filter. The sum of the driving source impedance and R1 should be 150 Ω. The Butterworth capacitor values for C1 and C3 are shown in parentheses for comparison.

The plots of Figure 2 demonstrate the resulting gain and phase response of this 5-pole filter, compared with that of a 5-pole Butterworth filter. Note that the stopband slope of the modified filter is not as steep as that of the Butterworth filter, but the phase delay near cutoff is significantly reduced. Some of the stopband slope steepness in the amplitude response is sacrificed to achieve less group delay. The reduced steepness of this slope is not a problem since the sampling rate is four times the maximum frequency of interest, allowing enough attenuation of energy at half the clock rate to avoid aliasing problems. The reduced group delay reduces ringing in the step response of the system.

This circuit was developed for use in an ADC1175 signal conditioning circuit. The ADC1175 is an inexpensive, low-power 20-Msamples/s analog-to-digital converter with superior dynamic performance characteristics.

Video ADCs tend to have input current transients that can upset the driving amplifier, causing it to distort the driving signal as it attempts to counteract the transient load current. R5 and C4 isolate the amplifier's output from the current transients at the input to the ADC, maintaining signal fidelity. This RC also adds a small phase lag that improves the phase margin of the video driver.

Circle 522

ADC Clock Gating Circuit Maximizes Data Throughput

MARK MADDOX
Analog Devices Inc., 804 Woburn St., Wilmington, MA 01887; (781) 937-2955; fax: (781) 937-1069; e-mail: mark.maddox@analog.com.

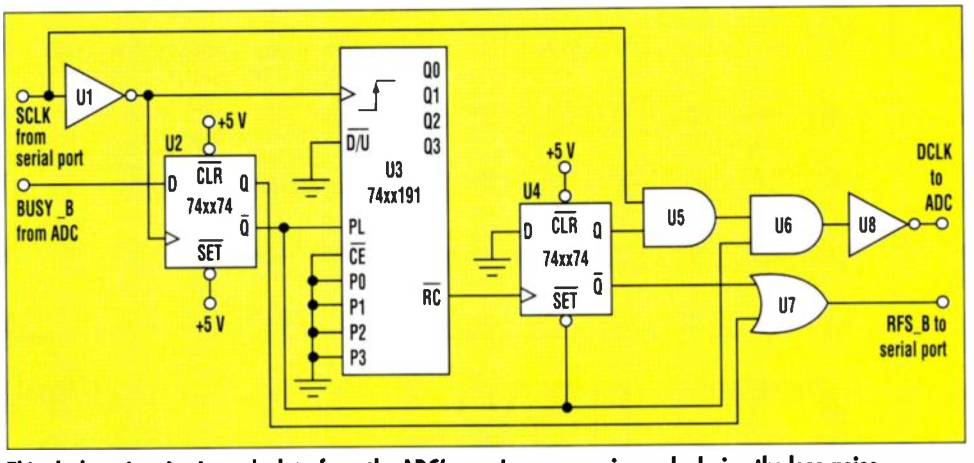
When reading the data from a serial analog-to-digital converter (ADC), it may be desirable to use a serial port available on a microprocessor or a digital signal processor. If the ADC offers high resolution (i.e., 16 bits or greater), it may actually degrade the converter's performance by having the microprocessor's serial data clock running at the same time the ADC performs a conversion. Or, more specifically, during the last half of the conversion when the least significant bits are being determined.

The ADC's specifications that could be degraded are integral nonlinearity, differential nonlinearity, or transition noise. Unfortunately, some serial ports found on commercial processors will generate a data clock that continually runs even when data isn't being read from the ADC. Therefore, the clock can't readily be shut down during the analog-to-digital conversion cycle.

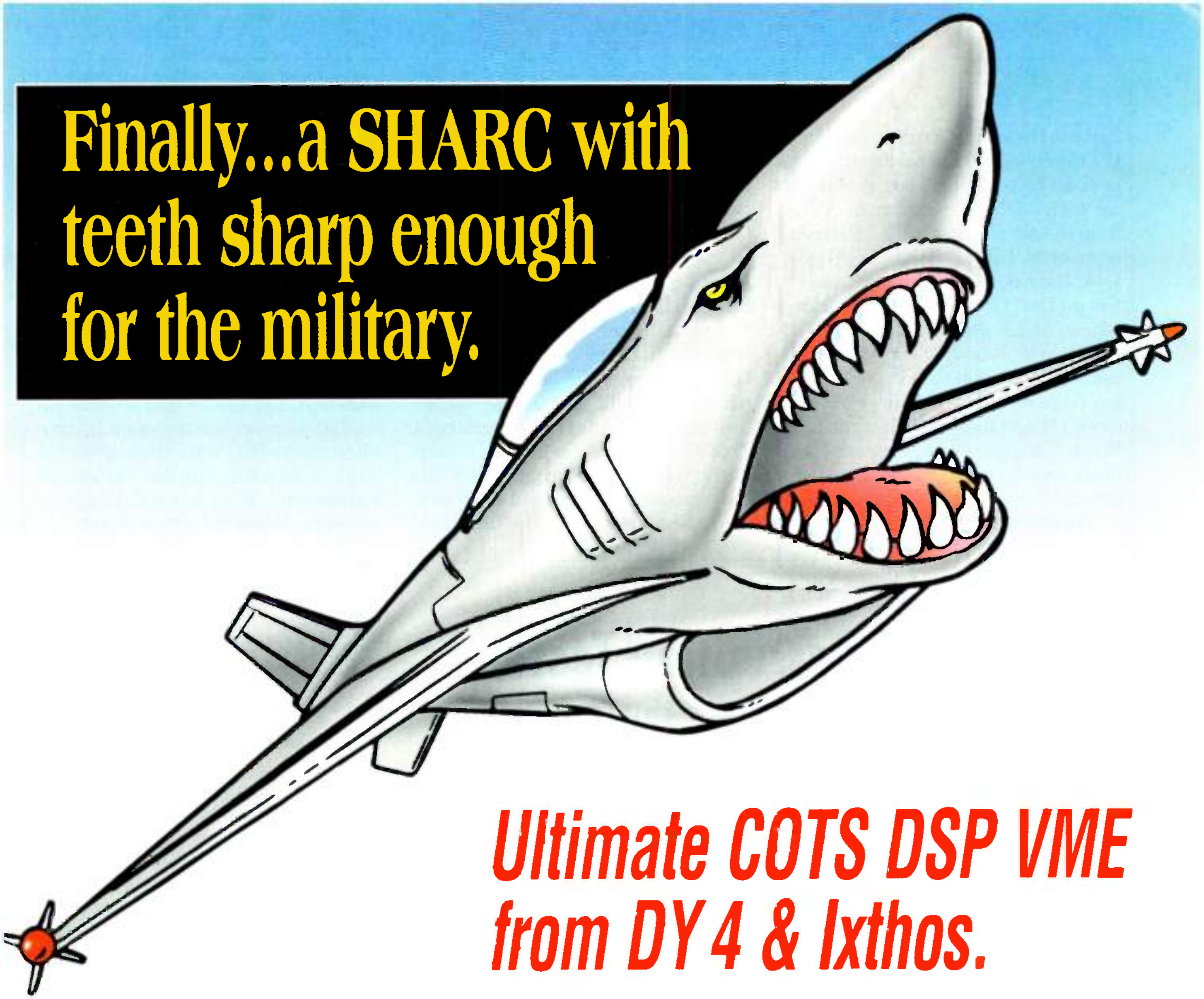
This circuit will take a continuous clock provided by the serial port, pass the minimum amount of clock pulses required by the ADC on through to the converter and block all of the other clock pulses. This will minimize the effect of digital feedthrough of the clock during the sensitive portions of the ADC's conversion period. The circuit shown in the figure is designed to read the data from the ADC's previous conversion cycle during the first half of the current conversion cycle. This method of reading the data is ideal for maximizing data throughput, assuming the ADC isn't sensitive to having its serial data and clock pins changing state during this first half of the conversion.

A signal from the ADC that indicates when the converter is performing a conversion is required by the circuit. In this illustration, the ADC is providing the signal BUSY_B, which is Low during the period of time the conversion is occurring. This circuit assumes the ADC presents data on the rising edge of SCLK, and the serial port will latch the data on the subsequent falling edges of SCLK. The circuit is held in a reset state while BUSY_B is High by forcing the binary counter to preload all zeros. This will also force its ripple carry output to High. With BUSY_B High, the receive frame sync signal to the serial port, RFS_B, is forced High and the clock signals are blocked at U6 and unable to pass through to the ADC.

When BUSY_B goes Low to



This clock gating circuit reads data from the ADC's previous conversion cycle during the less-noise-sensitive first half of the current conversion cycle, helping to maximize data throughput.



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indicate the start of a conversion cycle, the binary counter is taken out of the preload state and will begin counting up with each falling edge of SCLK from the serial port. On the 16th rising edge of SCLK, after BUSY_B goes Low, the ripple carry output from U3 will go Low. On the subsequent falling edge of SCLK, the 16th falling edge after BUSY_B went Low, the ripple carry output will return High. This rising edge of the ripple carry out will clock U4 and force its Q output Low. When U4-Q goes Low, it forces U5 to block any further clock pulses from passing through to the ADC.

The clocking of U4 also removes the receive frame sync to the serial port. The clock pulses to the ADC will remain blocked for the remainder of the time that BUSY_B is Low. When the analog-to-digital conversion is complete, BUSY_B will return High and the next falling edge of SCLK will force the counter into the preload state again.

Assuming the ADC is more sensitive to digital feedthrough when the least significant bits are being determined, all 16 data bits must be read before this point of sensitivity occurs. This will place a lower limit on the frequency of SCLK. If a converter with a conversion time of 5 µs is used, for example, the frequency of SCLK should be set to 8 MHz to ensure that all 16 bits of data can be read in a time less than the first half of the conversion cycle. An 8 MHz clock has a period of 62.5 ns from rising edge to falling edge and, therefore, the worst-case propagation delay through this circuit would have to be less than this value.

By reversing the connections at the outputs of flip-flop U2, the circuit operation can be modified so that the data from the ADC would be read immediately after a conversion is complete rather than after the conversion begins. Reading the data after the conversion is complete will, however, result in a lower data throughput.

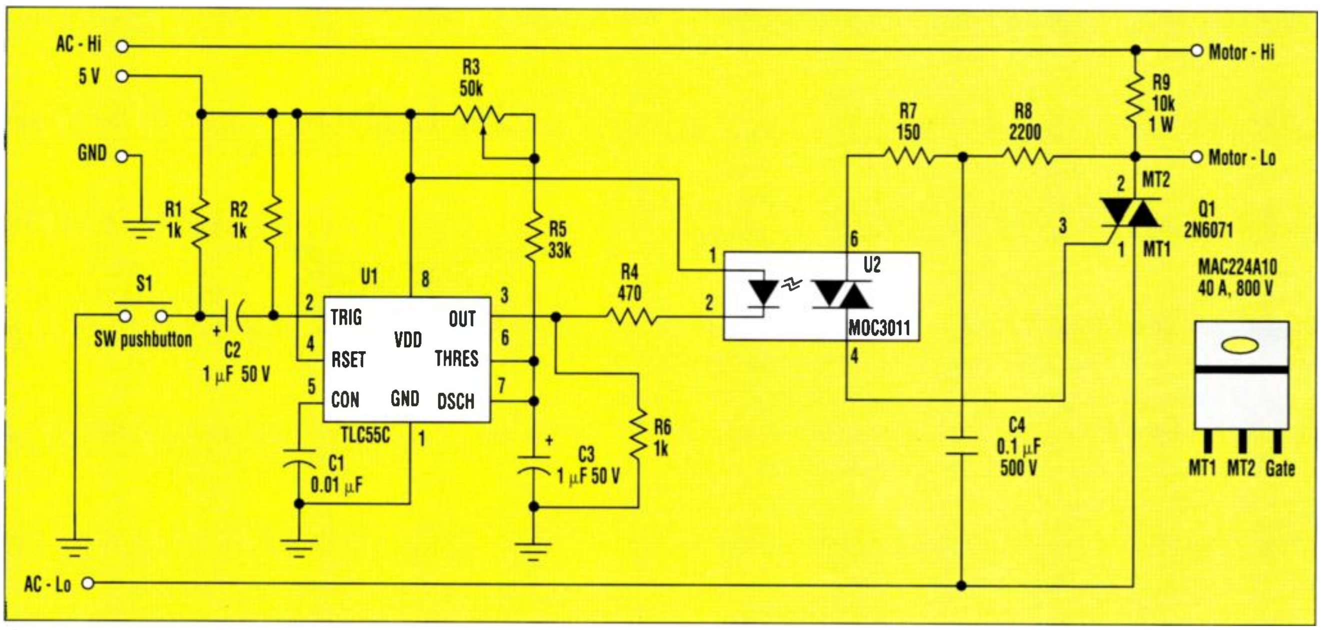
Circle 523

Power Interruption Tester For Restart Circuit

KEITH KENYON
GAST Manufacturing Corp., Remark Facility, P. O. Box 97, Benton Harbor, MI 49023-0097; (616) 927-5742; fax: (616) 927-5725;
e-mail: Keith_Kenyon@gastmfg.com

Compressors are susceptible to brief power interruptions as short as 30 ms or 2 cycles of ac power. Even these short "glitches" may cause a pump to stall when it's under load. To alleviate this potential hazard, a restart circuit was designed. It controls a valve that opens momentarily to relieve the load after the power interruption. The power-interruption tester presented here was designed to test the operation of the "restart circuit." It also has been used to characterize pumps and determine which ones require a restart circuit.

The power interruption circuit uses a 555 timer to create the variable width pulse that momentarily turns off a triac. The triac functions as an electronic switch supplying ac power to the pump under test. The circuit is activated by pressing a momentary contact switch. This supplies a ground to the positive end of C2, which has been charged to +5 V. By setting the value of C2 to 1 µF, the contacts of the switch are debounced and won't retrigger the 555 one shot. The leading edge of the pulse is transferred to the trigger in-



This Power Interruption Tester conveniently simulates the effect of momentary power line glitches that can be produced during storms or maintenance operations. The circuit can produce simulated power interruptions which vary from 20 to 50 ms in duration

put of the one shot.

The 555 timer circuit is configured as the standard one-shot design. C3 is the timing capacitor and chosen to be 1 µF, while R3 is a variable 50k potentiometer. Having it in series with R5, a 33k resistor, allows the pulse duration to vary from 20 to 50 ms. Changing these values can easily provide alternative pulse widths and adjustment ranges.

The pulse is coupled to the optoisolator through R4. Resistor R6 assists in wave-shaping the pulse. The output of the one shot is low until it fires. This condition maintains the isolator and the triac in the conducting state. When the one shot fires, the output switches to 5 V, which causes the isolator to remove the drive signal to the output triac. The triac remains open or off for the duration of the pulse.

The triac chosen for this application is a 2N6071. This part provides plenty of current capability for the largest motors that were tested. The 800-V breakdown voltage offers plenty of margin if the tester is to be used on 230-V motors. It was mounted on a heat sink to assure that the load of larger motors didn't cause the triac to overheat. Using the power interruption tester makes it convenient to simulate the effect of power-line glitches that can occur with momentary failures due to storms or maintenance operations.

Circle 524

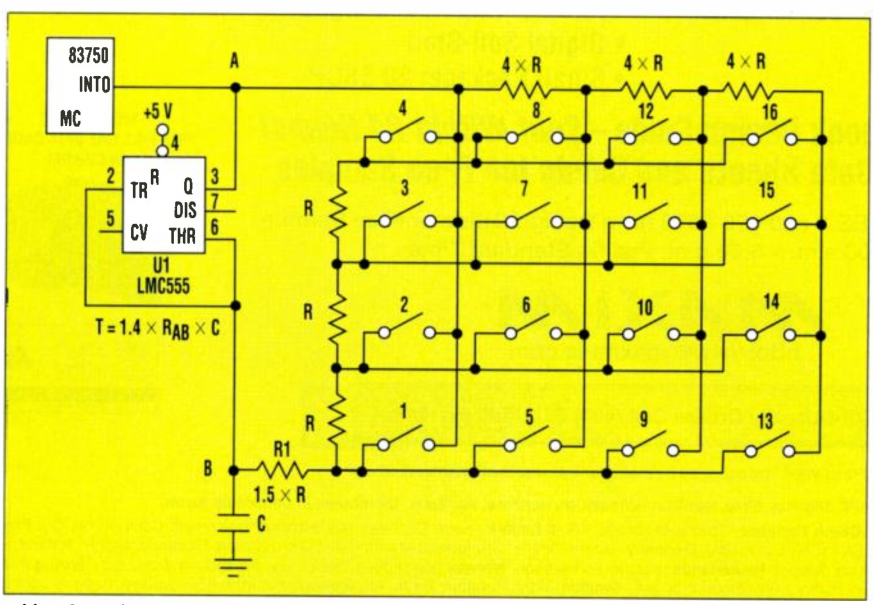
Connect Any Keypad With Any Microcontroller Using Only One Pin

SAMUEL KEREM

Patton Electronics Co., 7622 Rickenbacker Dr., Gaithersburg, MD 20879;
(301) 975-1000; fax: (301) 869-9293; e-mail: samuelkerem@juno.com

After "Use A Tiny Microcontroller With A Large Keypad" was published (ELECTRONIC DESIGN, *Sept. 2, 1997, p. 166)*, I got a number of responses that prompted me to develop a corollary design. Presented here is a design applicable to microcontrollers not equipped with a built-in ADC.

Looking at the figure, you'll notice a familiar 4x4 keypad with a single difference—each row and column are separated by a resistor. If key #1 is pressed, the resistance between nodes A and B (R_{1AB}) is equal to 1.5*R; for key #2—R_{2AB} = 1.5*R+R = 2.5*R; and so on ... key #N—R_{NAB} = N.5*R. This variable resistor network is connected to a 555 timer (CMOS version), configured as an oscillator with the period of oscillation equal to T = 1.4*R_{AB}*C, directly proportional to R_{AB}.



Adding large keypad matrices to microcontrollers without built-in ADCs is practical using this modified keypad arrangement. Up to 500 keys can be scanned at rates up to 8 characters/sec.

The oscillator runs only when a key is pressed, causing an interrupt request for the microcontroller. The INT0 pin is set up as edge-sensitive. The general algorithm can be described as: 1) after detecting the edge on the INT0 pin, wait 20 ms to eliminate ringing; 2) detect the next edge and start the internal timer; 3) the following edge stops the internal timer. The measured period (the time between two consecutive positive edges) will define the key number. Any microcontroller with a built-in timer (the vast majority of microcontrollers) can implement this idea.

For a specific example, I will use the 8051-family microcontroller with a 12-MHz clock. In this situation, the single count of the timer will be 1 µs. If we choose 47 nF for the capacitor and 3.9 kΩ as the resistor value, we will have T = 1.4*R*C = 256.6 ≈ 256 µs. That is the period difference between oscillations produced by two serial keys. After calculating the period interval produced by any key pressed, we need only to make integer division by 0xFF (256_{10}) to get the key number of the depressed key. The value for R1 =1.5*R is chosen to provide the highest error margin for the elements by moving the period value in the middle of two consecutive numbers.

Some possible sources of errors in this application are: 1) component tolerances; 2) 256.6 µs instead of 256 for 1% resistors; 3) the closest value to 4*R, if R = 3.9k, will be 15.4K or 15.8K instead of the calculated 15.6k., an additional 1% error for each following column; 4) the 555 oscillator inaccuracy—temperature drift of 75 ppm/C° and variation 0.03% for a power-supply variation of ±0.1 V.

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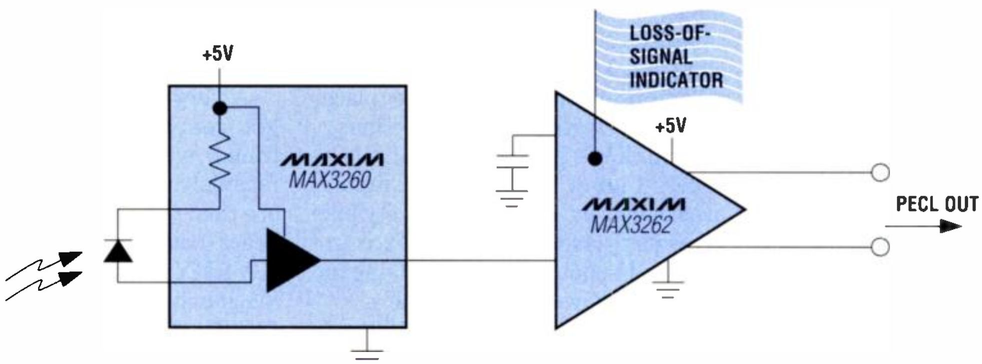

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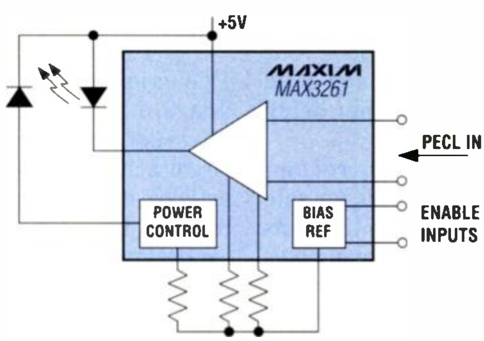

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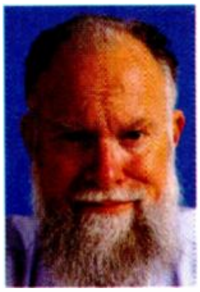
BOB PEASE

Bob's Mailbox



Hi Bob:

I've been an EE for some 20 years or so, and a keen biker for slightly longer than that, so your column in the Feb. 9 issue was doubly interesting.

The one thing that puzzles me is the fact that you have sampled the joys of motorcycling, yet aren't going to take it up in what is probably one of the best places on Earth, weather-wise: California.

I think it's true to say that all the bikers I know over here in England are hooked; even a small-capacity bike gives you performance far in excess of any car. I'm not necessarily talking top speed, but how fast you get there.

I've got a 1978 Triumph 750 cc (a pushrod engine based on a bored and stroked 500-cc design of 1938). Although it's pushed to top 100 MPH, it can (or could) get from 0 to 60 in. about five seconds. A line of cars is no obstacle—even in England where we probably have some of the narrowest, most-crowded roads in the world. Just squirt the throttle, and away we go.

I think you should reconsider your decision. I would hate to think of all that beautiful biking weather being wasted.

I'm sure the book you recommended is an excellent basis for safe riding, but the one maxim that has kept me out of trouble (both on bikes and in cars) is to treat the other guy as a jerk. Ninety-nine times out of 100 you'll be proved wrong, but that one time could save your life.

PHIL GEARY
via e-mail

I like to take all sorts of suitable, reasonable risks. The one risk I do not like to take is on a motorcycle. It's too easy for people to ignore you, not see you, or just not care. I'll tell you exactly what it will take to make me buy and ride a motorcycle: it would have to be outfitted with this "accessory"—a laser hologram that looks like a Mack Truck or like a big, rusty Land-Rover. That way, nobody could ignore me. Until then, thanks, but I'll pass.—RAP

Hi Bob:

Good article. Motorcycling can be a lot of fun if it is done safely. Another way to learn is to get a dirt bike, and learn to ride off-road first. You can learn a lot about handling, weight-transfer, and the rest, that way. And it's not so fatal if you fall. That is how I learned.

A very good piece of advice, that I got from a LA CHP motor officer (a friend), was to drive (on the street) defensively, as if no one else knows you are there. It has worked for me for 31 years. I also agree that riding in traffic is VERY dangerous, especially in a metropolis like the Bay area.

CHRIS LITTLE
via e-mail

Yeah, I always rode bicycles assuming nobody could see me. I only got run down once by a guy making an illegal U-turn in the middle of a bridge. Maybe I should buy a dump truck with a laser hologram of a motorcycle?—RAP

Hi Bob:

I just wanted to tell you how much I've enjoyed your articles over the years. I am an analog impostor, a physicist who enjoyed playing with circuits in the lab, reading books and articles, etc. Fifteen years and many products later, I'm considered an "analog designer" (whatever the heck that means), but I still feel like an impostor. Will I ever get over this?

BARRY McGINLEY
via e-mail

Barry—are you trying to say that you might have a guilty conscience because you are getting PAID for having FUN? Well, don't feel too bad about it. I get paid for having fun, too.—RAP.

All for now. / Comments invited!
RAP / Robert A. Pease / Engineer
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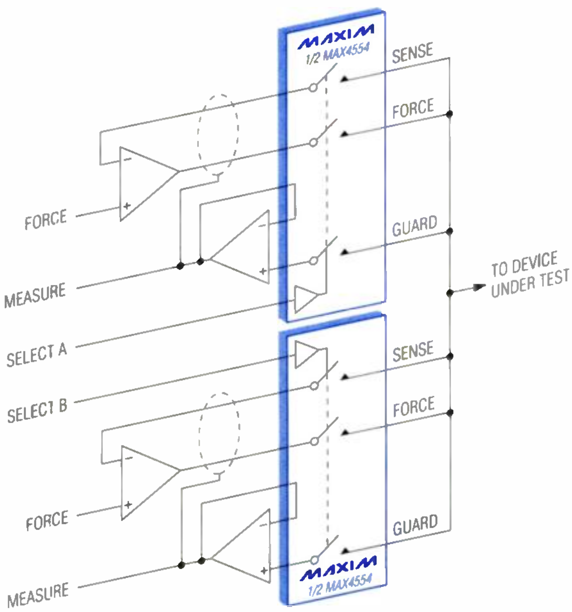

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Spice Programs:

Computerized Circuit Analysis For Analog EEs

This month we follow up on the Feb. 9th column's general topic of Spice. We're also going to look at some of the programs available, and learning aids convenient to the analog-oriented EE. In the earlier column, the main focus was a couple of Spice-oriented book reviews. Now I'd like to share with you some of the comments I received.

Spice Training Programs: In addition to the previously mentioned RCG Research Inc. training programs, there are other sources suitable for those interested in learning Spice. Charles Hymowitz of Intusoft wrote making this point.

I am attaching flyers on our Spice class that we have been teaching for over 10 years now, with over 1000 students during that time. We are the only Spice vendor that does their own classes, and have had a lot of experience with the "Spice learning curve." One flyer describes some great-selling, Spice-related books, especially the "SMPS Simulation with Spice 3."

*You might also want to check out our web site (*www.intusoft.com*) for more information and lots of Spice goodies. Unlike other EDA sites that are primarily advertising, we have posted a wealth of technical literature, articles on Spice, and related modeling topics, application notes, and free models.*

Thanks for the useful information, Charles. I noted from a visit to your web site that the Spice book list which you forwarded is available under the "Spice Reference Books" button. Numerous working Spice program files are under the "Demos" button, and the class descriptions are at *www.intusoft.com/classes.htm*. I was also impressed with the number of technical articles you have online, and the issues of your newsletters. You have a very useful and information-rich site.

Spice Vendors: Several months ago, before the great PC crash of Fall 1997 (see the April 6th column), I had been working on accumulating and evaluating a number of demo Spice packages. Well, frankly, the PC crash wiped out much of that work. So, for this article I simply decided to list a number of commercial and public domain Spice program sources. All are available for web download. Most commercial packages mentioned are "suites," meaning integrated schematic capture and simulation, and in some cases, PCB design capability.

The MicroSim web site is at *www.microsim.com*, and it offers demo programs via the "Download" button. These are not only the latest releases of the main program PSpice, plus the related schematic capture and PCB design files, but also the associated user guides, in PDF format. Numerous tech support files, newsletters, Spice bibliographies, and book lists can also be found, under the "Tech Info" button.


WALT JUNG

MicroSim has recently merged with OrCad, and there is a news item addressing this point. The main MicroSim site is loaded with lots of tech info, but other (older) PSpice versions can be found at various EE web sites (see below).

Another Spice simulator which has long been popular with the design community is Micro-Cap, from Spectrum Software (*www.spectrum-soft.com*). The web site features a demo version of the current release, Micro-Cap 5, version 2, which runs under Windows 3.1, 95, and NT. It appears that the authors of Micro-Cap have made great efforts toward interfacing compatibility with other simulators. For example, they state that Micro-Cap reads, writes, creates, and analyzes standard Spice and PSpice text files, as well as its own schematic files. This feature is not a minor point, if you have older ASCII circuit files.

Interactive Image Technologies Ltd., Toronto, Canada, has a popular, under-$1000, integrated Spice program called Electronics Workbench. It is available in full-featured professional, and more- limited versions (*www.interactiv.com*). These simulators include a schematic capture program and an interactive simulator, but PCB layout is separate. A distinguishing feature of the program is the "workbench" look and feel, using a virtual oscilloscope and signal generators. A demo version of the software is available.

Ron Tipton of TDL Technology reported his experiences with another Spice vendor, Penzar.

*Penzar Development (*www.penzar.com*) offers an inexpensive Spice (compared to PSpice and Intusoft). They call their version TopSPICE, with both DOS and Windows versions available. I've been using it six-to-seven years, and it is very satisfactory, as it includes both mixed-mode and analog behavioral modeling.*

The Intusoft Newsletter is a good model info source, as are EDN and ELECTRONIC DESIGN. *I've been clipping and saving models, and have a thick notebook full of them. Enjoyed your Spice comments.*

Thanks for your comments, Ron. I checked out the Penzar web site, and as you say, their programs are relatively inexpensive. The full Windows 95 version, TopSPICE/Win32 5.4, sells for under $500. There are demo versions available for Windows 3.1 and 95, and DOS platforms. I also noted that the packages include schematic capture and simulation.

A literal cornucopia of free Spice simulators is available on the web. Just point your browser to *www.paranoia.com/~filipg/HTML/FAQ/BODY/F_Free_Spice1.html#FREESPICE_001*. Here you will find Spice simulators for numerous operating systems, DOS, Windows, OS2, and even several PSpice versions back. You'll also find Berkeley Spice in several flavors.

Reader Reactions To Spice Issues: February's column ended with queries on these Spice issues: the general appeal of simulation as a design tool, the adequacy of current simulators and models, and the move toward integrated suites.

Wilfried Adam, a German consulting engineer, answered thusly:

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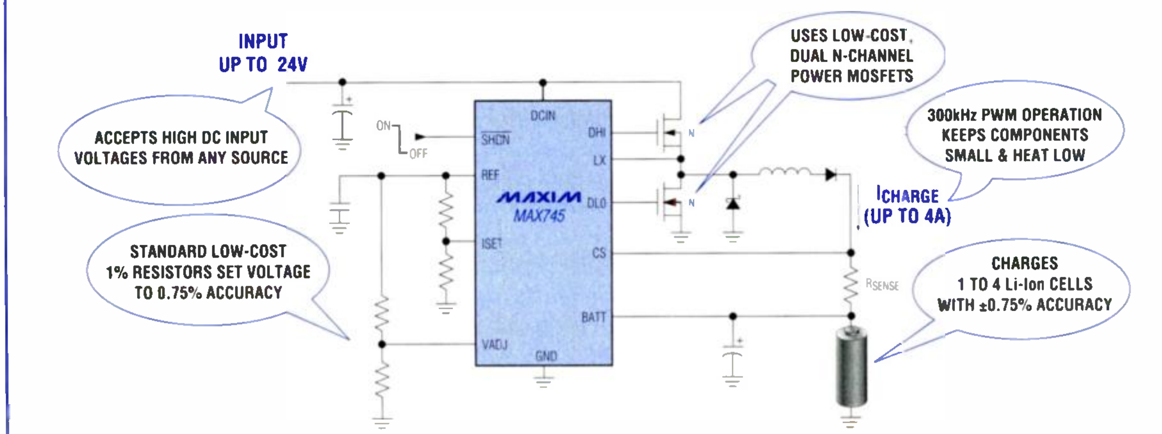

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MAX1647/1648	✔	✔	✔	✔	Switch-Mode w/ SMBus™ Interface
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WALT JUNG

audio electronics, and I use simulators only occasionally, i.e., once a week to once a month.

I find simulation indispensable, especially because the next electronic components shop is 55 km away, and ordering special one-off parts by mail order isn't particularly cost effective. As for the adequacy of simulators, yes, they offer much more than I need.

Regarding suites, for the professional engineer, the answer is probably "Yes," whereas in my case, suites are too difficult to handle. It is difficult enough for me already to learn how to use a simulator because the learning curve is usually very steep—the MicroSim design center in particular—and even more so if used only on an occasional basis. The more educationally oriented simulators do not cover my needs, although they are much easier to handle. The best compromise for my needs was, and still is, Micro-Cap, where I could even master the DOS version (when used only occasionally).

Simulators have surely come a long way from command-line and net-list DOS programs to the more user-friendly GUI versions of today. The user interface still needs attention, and the introduction of (optional) wizards as seen in modern word processors, might be a very good idea for simulators too.

Thanks for the comments Wilfried. I find your reactions to GUI-oriented simulators interesting, as I don't always find them an ideal working environment, either.

The comments below by Dave Graff of Electronic Consultants, Inc. touch in this area as well.

In response to your request for Spice opinions, I offer my experiences and comments. As a design consultant, I do a lot of circuit analysis, and find Spice transient analysis a very valuable tool for many analog circuits. The two areas that you touched on in your article, however, are the major problems with Spice.

First, and foremost, is the model problem. At best, models supplied by device manufacturers are barely adequate for evaluating nominal circuit performance. No vendor provides best- and worst-case model parameters. It is up to the analyst to determine the appropriate model parameters to vary (and by how much), and to match data sheet tolerances. This is no easy task.

Even worse, the nominal models don't always work. I've seen cases where adding a small resistor in series with the power-supply pin causes an op amp output voltage to rise tens of volts above the supply voltage. After looking into the model, I found that the problem was caused by a current source in a behavioral model for the output stage. There was nothing to limit the output voltage to realistic values. The bottom line is that all models need testing, to verify that they produce realistic results.

The other major problem is convergence. Adjusting tolerances and time steps sometimes solves the problem, but not always. I'm interested in Ron Kielkowski's comments on this.

Regarding integrated packages, my only experience has been with the MicroSim Windows version 7 product. I found the schematic capture unfriendly and difficult to use. I couldn't even find simple switch models on their parts menu. I decided not to use that product, using the older 6.1 DOS version instead, finding it much easier editing a net list. I'm against integrated packages, because they force you to use a single vendor's product, when that vendor may only be superior in one phase of the problem (e.g., simulation). I prefer using the best products for each task. Of course, it would be nice if all packages from different vendors could communicate with each other.

Thanks, Dave. I'd like to add some perspective on models. My company (Analog Devices Inc., Norwood, Mass.) offers IC models, as do most other semiconductor suppliers. While not directly involved with these models, I have had past modeling experience.

To best understand a basic model limitation, let it be said that virtually all available vendor-supplied models are *macromodels*, for reasons of simplicity, speed, and proprietary interests. As such, they mimic a real part with controlled sources, passive parts, and a minimal number of junctions. Sometimes, controlled sources don't offer the same dynamics of real transistors, for example in an output stage (an inherent weakness of this type of model). But still, the example you cited should not have happened, and it simply sounds like you ran into a defective model.

But, models *can indeed* be made to mimic real parts with regard to worst-case offsets, gains, etc. Taking the ADI library as one example, there is an "A" suffixed OP177A, etc., documented as: "This version of the OP-177 model simulates the worst-case parameters of the A grade. The worst-case parameters used correspond to those in the data book." A user of this op amp can employ the proper suffix model to simulate appropriately.

That said, it is also true that more complex models with many bells and whistles for various device operating modes will in turn, run slower and be more difficult with convergence. So, model fidelity is not a simple issue!

As for the comments on convergence, I forwarded your letter to Ron Kielkowski, who offered this:

Regarding Dave Graff's comments: Most designers today fail to realize that Berkeley Spice and all of the derivatives based on it have been compromised. The original authors decided that fast simulation was one of the primary program design goals. As a result, the time-step control and numeric integration algorithms, plus the device model equations are in many ways less than optimum for accurate, convergent simulation. While better, more-accurate algorithms exist, they weren't ever implemented, because they all slow down simulations. Therefore, our simulations are often plagued with time-step control errors, numeric integration instabilities, and of course, nonconvergence.

But, before throwing up our hands, let's remember two points: The original authors of Spice (and Cancer) pulled off a minor programming miracle when they produced the code which is now the mainstay for circuit simulation, and when a user takes the time to understand the inner working of Spice, many of the problems are easily overcome.

Dave Graff mentioned that setting tolerances and adjusting time steps sometimes helps nonconvergence. But he failed to mention any of the other nonconvergence aids available in Spice. Nonconvergence can be caused by no fewer than six different mechanisms. It is unfortunate that more en-

gineers don't understand what causes nonconvergence, because understanding of those causes allows us to prevent 80% to 90% of the typical nonconvergence cases we see.

Our "Successfully Simulating Circuits with Spice" course has been on hold since 1995 because of a flood of requests received for our two MicroSim PSpice Workshops. But we may be able to start offering this course again soon. Until then, it is my hope that the information in my "Inside SPICE" book will be benefit all Spice users. The second edition just came out, and it has new Windows-based programs to replace the first edition's DOS versions.

Thanks for the clarifying comments, Ron. Readers should note the new book constitutes another Spice source, in addition to those above.

Gary Huntress of the Newport Naval Undersea Warfare Center wrote in with some interesting ideas fpr running Spice (and other things) on a PC, but under Linux (a UNIX-for-PCs OS), in contrast to Windows 95.

Walt, I enjoyed your recent Spice tutorial and book article. I hadn't used it for some time, and now you've prompted me to pick it up again.

Although not mentioned in your article, I suppose that you know Spice is available for the Linux operating system? For about $30, you can have a world-class operating system with wonderful simulation tools. The fact that Linux runs great on a 486 motherboard that you can rescue from the trash is a plus too! I haven't found anything that can't be done better, faster, and cheaper under Linux. The biggest obstacle is the learning curve.

Thanks for some insight into an alternate way, Gary. Obviously, a hands-on Linux piece isn't something to do quickly, so I'll defer signing up for now.

TIP: On the seminar trail, I hope to personally meet some of you *Electronic Design* readers during April and May, while travelling around the U.S. and Canada to selected sites. I'll be presenting material, along with the rest with the 1998 Analog Devices seminar team.

Walt Jung is a corporate staff applications engineer for Analog Devices, Norwood, Mass. A longtime contributor to ELECTRONIC DESIGN, *he can be reached via e-mail at: Walt_Jung@CSI.com.*

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Protocol Processor Chip Puts Network Smarts In Anything

Capable of handling most network protocols, the NET+ARM embedded processor is intended to let nearly any kind of equipment communicate over LANs or the Internet. The single-chip communication controller can cut in half the cost and development time of net-enabled products, such as industrial controls, medical equipment, printers, point-of-sale terminals, building controls, and security systems.

It combines a powerful 32-bit ARM RISC processor with on-chip network interface logic, a real-time operating system, and a complete set of communication protocol stack software. The software includes 10/100Base-T Ethernet and Internet protocols, HTTP and FTP client and server functions, plus support for web browser, mail servers, and most other commonly used communication drivers and interfaces. Its flash download feature permits updates or addition of code to support new protocols.

The NET+ARM boasts an on-chip 10/100 Ethernet MAC, a memory controller (with refresh logic), a 10-channel DMA controller, and two serial ports. It also sports four IEEE 1284 parallel ports, a bus controller, several timers and a clock generator, and a general-purpose I/O port. The following network protocols are currently supported: TCP, UDP, RARP, and ICMP. NET+ARM's embedded software has drivers and APIs for many network applications, including: HTTP for web servers, POP3 and SMTP for Internet mail, FTP for data transfers, SNMP and HTTP management protocols, plus Bootp and DCHP for installation. Optional communications software can be included to support PPP and JetSend functions.

Housed in a 208-pin plastic pack, the NET+ARM operates on a 3.3-V supply. A development kit that includes documentation, hardware, and a set of GUI-based development tools also is available. The NET+ARM costs $30 - $40 each, depending on configuration, in quantities of 20,000. LG

Oscicom Technologies Inc., 2800 28th St., Suite 100, Santa Monica, CA 90405; (310) 581-4030; fax (310) 581-4032; www.osicom.com.

CIRCLE 548

Low-Power Design

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Mezzanine Card Has Four 200-kHz Analog I/O Channels

Designed for data acquisition and control applications, the bitsi-BB2 supports four differential analog inputs and four analog outputs, with data at rates of up to 200 kHz per channel. The card meets the BITSI I/O mezzanine standard, which is optimized to match the SHARC DSP's sophisticated I/O capabilities. It uses the SHARC's external parallel bus to provide a low latency interface between the data converters and the SHARC. In addition, a 32-bit digital I/O port facilitates the exchange of digital data with an external device. The bitsi-BB2 can accept external sample clocks and interrupts, or it can generate sample clocks and interrupts from its two 16-bit timers.

Dozens of off-the-shelf BITSI I/O mezzanines are available from BittWare, including audio, control, video, and telephony interfaces. The interface consists of 32 data bits, 20 address bits, 10 control signals, 2 DMA channels, 6 SHARC link ports, and 3 serial ports. The bitsi-BB2 is available immediately starting at $1750. JC

BittWare Research Systems, 33 N Main St., Concord, NH 03301; (603) 226-0404, ext.534; www.bittware.com. **CIRCLE 538**

Removable Modular Flash For The PC/104 Standard

The PC/104 embedded bus standard continues to leverage advances from the PC world. The latest such technology feeding into PC/104 is Compact Flash. The PCM-CFlash is a PC/104 compatible adapter that supports Compact Flash (CF) cards.

Compact Flash is a worldwide standard for removable storage cards the size of a matchbook—1.7 by 1.4 in. (43 mm by 36 mm) and weighing half an ounce. The PC/104 board measures 3.6 by 3.8 in. (90 mm by 96 mm) and mounts in a PC/104 stack. The module can act as the boot disk if no other disk is in the system. PCM-CFlash also is offered without PC/104 mounting; it's called the ADP-CFlash.

The PCM-CFlash module links to the CF card via its ATA/IDE interface. To software, the CF cards appear to be a standard IDE disk drive. Compact Flash cards with capacities up to 24 Mbytes are available today. PCM-CFlash is available today at a price of $59 (without CF cards). JC

Winsystems, Inc., 715 Stadium Dr., Arlington, TX 76011; (817) 274-7553; www.winsystems.com. **CIRCLE 539**

VME Board Performs 1.92 GFLOPS Per Slot

The IXZ16 is the first COTS VME board incorporating 16 SHARC DSP devices on a single 6U board. The 1.92-GFLOPS/slot performance is achieved using four clusters of four SHARC processors. Each of the 16 SHARC devices on the new board runs at up to 120 MFLOPS. It includes a large on-chip SRAM (up to 4 Mbits), which is dual-ported to support internal DMA engines that concurrently drive the six

(continued on page 139)

(continued from page 138)
40-Mbyte/s Link-Ports and a 160-Mbyte/s parallel bus. On-chip multiprocessor arbitration allows the SHARCs to be grouped together in clusters of tightly coupled DSPs.

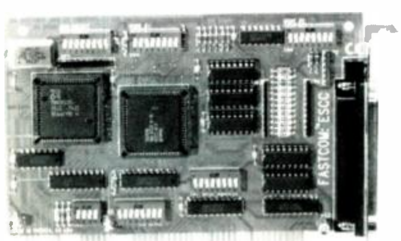
On the IXZ16, four SHARCs in each cluster fit into a single multichip module (MCM). Each MCM uses advanced ball-grid-array (BGA) technology to minimize size and reduce ground bounce and inductive loops between signal pins. The small size of each MCM makes it possible to attach all four SHARC MCMs directly to the baseboard, which in turn reduces susceptibility to vibration and electromagnetic interference (EMI).

The board holds two IXI mezzanine cards within a single 6U slot. IXIs interface to signals via the front panel and can provide continuous throughputs of 160 Mbytes/s to the board's SHARCs. A wide variety of IXI mezzanines is available, with analog-to-digital conversion to 50 MHz, digital-to-analog conversion to 25 MHz and parallel digital interfaces capable of 100 Mbytes/s. JC

DY 4 Systems Inc., 333 Palladium Drive, M/S 212, Kanata, Ontario, K2V 1A6, Canada; (613) 599-9191; www.dy4.com. **CIRCLE 540**

Communications Adapter Is Available For PCI Or ISA Bus

A new series of high-speed communications adapter boards is available in both PCI and ISA bus versions. Both cards in the FASTCOM/ESCC Series



support RS-422/485 communications using synchronous and/or asynchronous HDLC, SDLC, ISDN Lap D, and X.25 Lap B protocols. Each card provides dual, individually configurable channels using the Siemens 82532 communications controller. In the PCI version, the Siemens chip allows for full-duplex data-transfer rates up to 10 Mbits/s on both channels. The ISA version is limited to 4 Mbits/s on each channel, although rates up to 10 Mbits/s may be obtained in the half-duplex or forced-idle-time modes.

Each board occupies a single half-length AT expansion slot and provides operational specifications of 0-70°C and 0 to 90% relative humidity. Hook-up to the card's dual-channel serial port is made through one DB-9 male connector conforming to the RS-530 standard configuration. Pricing for the PCI and ISA versions of the FASTCOM/ESCC card is set at $525 and $425, respectively. Dial (800) 677-7329 for an index of fax-on-demand datasheets. JC

Industrial Computer Source, 6260 Sequence Dr., San Diego, CA 92121-4371; (800) 523-2320; Internet: www.indcompsrc.com; e-mail: sales@indcompsrc.com. **CIRCLE 541**

Parametric Test System Supports Windows NT

The Model S900NT is a pc-based parametric test system for process monitoring and device characterization in semiconductor testing environments under Windows NT. The S900NT links high-speed instruments, a low-noise switching matrix, and a PC with the Keithley Test Environment (KTE) software. The design of the new parametric test system includes high-accuracy instruments, such as one or more source-measure units and the Model 9631 integrating system voltmeter unit (ISVU). The source-measure units can be programmed to apply up to 100 V and 1.5 A.The ISVU digitizes the source-measure output for processing by the KTE.

A modular system with an open architecture, the S900NT can serve a wide array of test needs as well as adapt to emerging requirements. It's compatible with Keithley's wafer level reliability system. The s900NT is priced at $120,000 and is available 12 weeks ARO. JD

***Keithley Instruments Inc.**, 28775 Aurora Rd., Cleveland, OH 44139-1891; (800) 552-1115; (440) 248-0400; fax (440) 248-6168; www.keithley.com; e-mail: product_info@keithley.com.* **CIRCLE 542**

Thermal Power Sensors Improve Measurement Speed

The MA2420A series thermal sensors offer improved measurement speed over previous sensors. The series includes 18-, 32- , 40-, and 50-GHz models. In addition, better connector technology reduces measurement mismatch uncertainty through 50 GHz. This compares to previously attained levels of only 20 GHz. The sensors come with internal EEPROMs for storage of calibration factor data versus frequency. This allows a power meter to interpolate and correct readings automatically, useful in ATE and benchtop applications. Pricing is from $1200 to $3700. JD

***Anritsu Co.**, 1155 E. Collins Blvd., Richardson, TX 75081; (800) ANRITSU; (972) 644-1777; fax (972) 644-3416*
CIRCLE 543

3.2-GHz Workstation Calibrates High-End Scopes

The Model 9500/3200 scope calibration workstation calibrates high-performance oscilloscopes through the use of the company's Active Head Technology. The Model 9500/3200 workstation can drive as many as five active heads, and each head is able to deliver all of the required calibration waveforms as well as switch in a 50-Ω termination when necessary. As a result, the calibration of even multichannel oscilloscopes can be fully automated.

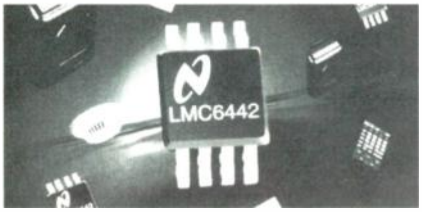
The workstation also comes equipped with Portocal-II/9010 calibration and inventory management software, plus a comprehensive library of scope calibration procedures for popular oscilloscopes. Pricing of the 9500/3200 is $24,995 with immediate availability. JD

***Wavetek Corp., Instruments Div.**, 9045 Balboa Ave., San Diego, CA 92123; (619) 279-2200; fax (619) 565-9558; www.wavetek.com.*
CIRCLE 544

ANALOG

Tiny Dual Op Amp Draws Very Little Supply Current

The LMC6442 dual op amp features a typical power current consumption of less than 0.95 µA per amplifier, and a guaranteed supply current of 1.2 µA per amplifier. The rail-to-rail-output, single-supply device is characterized for 2.2- to 10-V operation, and is fully guaranteed at 2.2, 5, and 10 V.



On the low side of the supply range, the LMC6442 is well suited for single-(Li-Ion) or two-cell (NiCd or alkaline) battery-powered systems that need low standby current for long service life. As battery life approaches end-of-charge state, its performance degradation is minimized by the LMC6442's low input bias current (5 fA typical), plus minimal variations in supply current over supply voltage. The LMC6442 dual op amp is available in an MSOP-8 or 8-pin SOIC package. Pricing for the part in these packages is set at $1.80 and $1.75 in 1000-unit quantities. LM

***National Semiconductor Corp.**, 2900 Semiconductor Dr., Santa Clara, CA 95052-8090; (408) 721-5000; http://www.national.com/pf/LM/LMC 6442.html.* **CIRCLE 545**

Op Amp, Comparator, And Reference Come In One SO-8

To provide more functionality from a single package and save board space, Linear Technology Corp. has released the LTC1541. It combines a micropower op amp with rail-to-rail outputs, a comparator, and a 1.2-V reference in a single SO-8 package.

While the op amp is internally compensated to be unity-gain stable, with a typical bandwidth of 12 kHz and a slew rate of 8 V/ms, the comparator has ±3 mV of hysteresis to ensure clean output switching. Also, the inverting input of the comparator is internally connected to the reference output. The LTC1541 operates from a single 2.5 to 12.6 V or dual ±1.25 to ±6.3 V, with a typical quiescent current of 5 µA. The common-mode input range for both the op amp and the comparator is from V_{SS} to within 1.3 V of the positive supply.

Capable of sourcing output up to 2 mA and sinking up to 20 µA, the reference output can drive a bypass capacitor of up to 0.01 µF without any oscillations. The LTC1541 is available in both 8-lead MSOP and SO packages. In 1000-piece quantities, the pricing starts at $2.15. AB

***Linear Technology Corp.**, 1630 McCarthy Blvd., Milpitas, CA 95035-7417; (408) 432-1900; www.linear-tech.com* **CIRCLE 546**

Synchronous Power Controller Is Efficient And Small

The LM2630 is a high-efficiency synchronous step-down switching converter packed in an ultra-thin TSSOP package. Designed to provide core CPU power in battery-operated systems, the LM2630 can achieve efficiency of 92% in applications requiring high output current. The high efficiency is made possible by a current- mode control scheme that quickly achieves output voltage with fast loop response and a very good line regulation of 0.002%. Other features include 0.3% load regulation; a power-saving sleep mode; protection against overcurrent, overvoltage, and undervoltage; and adjustable soft-start. While the input supply voltage range for the unit is 4.5 to 30 V, the output is adjustable from 1.8 V to 6.0 V. Also, the step-down converter's operating frequency can be adjusted from 200 to 400 kHz. Available in a 20-pin TSSOP, the LM2630 is priced at $3.00 in 1000-unit quantities. AB

***National Semiconductor Corp.**, 2900 Semiconductor Dr., Santa Clara, CA 95052-8090; (408) 721-5000; www.national.com.* **CIRCLE 547**

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CIRCLE 249

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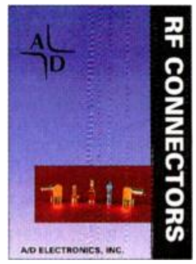
A/D Electronics' free RF Connector catalog offers 40 pages of F, TNC, UHF and Twinax connectors as well as SMA, SMB and SMC coaxial connectors in different configurations. The design engineer can obtain complete specs, dimensional drawings and evaluation samples upon request. Technical Support is available by contacting: A/D Electronics. Phone: (253) 851-8005; Fax: (253) 851-0990; www.adelectronics. com



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A/D ELECTRONICS

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CIRCLE 251

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CIRCLE 252

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CIRCLE 253

DYNAMIC SOFT ANALYSIS

BATTERY MANAGEMENT CATALOG

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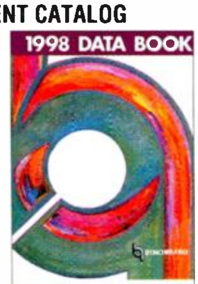

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BENCHMARQ MICROELECTRONICS, INC.

RACKMOUNT COMPUTER SYSTEMS

Interlogic's designs and manufacturers a complete line of rack computer systems and workstations. The new catalog features a selection guide to over 100 backplanes, ISA/PCI/PCISA - CPU cards, 486, Pentium, Pro and Pentium II. Custom solutions to meet your application needs. 516/420-8111, fax: 516/420-8007, www.infoview.com

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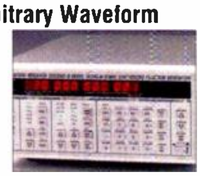

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A quarterly publication containing application notes, technical articles and modeling techniques on spice circuit simulations and test design. Available in hardcopy or online (www.intusoft.com.). Modeling disks accompany annual subscriptions ($45.00).

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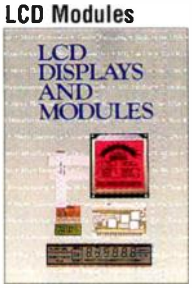

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DCI INCORPORATED

IC DESIGN SOFTWARE

Tanner EDA offers innovative, feature rich yet easy to use software solutions for custom and semi-custom IC design entry, simulation, layout and verification on Windows platforms, all at cost-effective prices. Ten years of experience producing EDA software for the PC providing these tools at a fraction of the cost of our competition. www.tanner.com/eda; (626) 792-3000; fax: (626) 792-0300; info@tanner.com.

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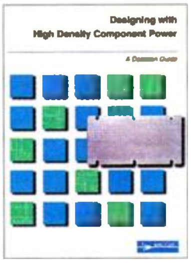
This free brochure, Designing with High Density Component Power, covers a wide range of issues that will expand your thinking beyond the limitations of traditional power system design, providing enough information to begin a discussion about the most effective power solution for your applications. 23 Frontage Road, Andover, MA 01810, (800)-735-6200; Contact: Vicor Express



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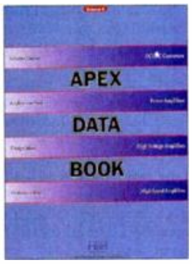

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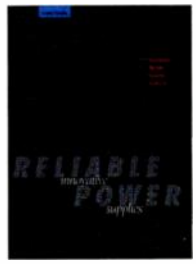

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Informative, illustrated Product Guide from Communications Instruments, a division of CII Technologies, features a broad line of high performance relays; low level to 10A; TO-5; 1/2-size, and others. Select from solid state relays and QPL to MIL-R-39016, 28776, and 5757 application assistance and council available. Contact: Raymond McClinton, Phone: 704-628-1711. Communications Instruments, Inc., div. of

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CII TECHNOLOGIES

C&K's EXPANDED BROADLINE CATALOG

C&K's expanded Newton Division Catalog #9801 is the most extensive switch catalog in the industry with 360 pages of models and options and process compatible switches. C&K Components, Inc., 57 Stanley Avenue, Watertown, MA 02172; Tel: (800) 635-5936 or (617) 926-6400; Fax (617) 926-6846.

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C&K COMPONENTS, INC.

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The Data I/O catalog is the direct-order source of affordable tools for users of programmable devices. From design software to device programming and automated handling systems, the Data I/O catalog offers unbeatable values on the high quality tools you need. Call 1-800-332-8246, ext. 806

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DATA I/O

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The catalog covers our entire product line and includes comprehensive supported device listings, all available options and features, and a complete price list. For information, call Yvon J. Blais Phone: (407) 649-3335, FAX: (407) 649-3310

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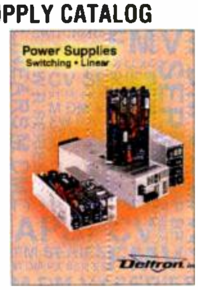
DATAMAN

NEW OEM POWER SUPPLY CATALOG

Deltron's full line catalog presents many new products including 1kW to 7.5kW T Series power factor corrected front ends for telecommunications systems, DeviceNet power modules, new generation modular F Series 0.99 power factor corrected switchers and Moduflex® M Series switchers. The catalog also details a full complement of time tested hi-grade industrial and commercial power supplies. For free copy call 800-523-2332 or fax 215-699-2310.



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DELTRON

INTERCONNECT SOLUTIONS

This catalog enables design engineers to easily locate the correct adapters, clips and test accessories. The catalog includes a Ball Grid Array Reference Guide along with information on over 4000 ET products, including emulator tools, logic analyzer/scope adapters, programming adapters, production/test adapters, debugging accessories, prototyping adapters, field-configurable adapters and custom adapters.
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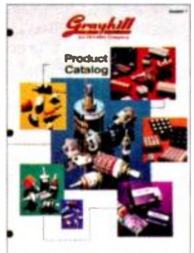
Gespac's 1998 catalog features a full line of 3U embedded PCs, 68XXO SBCs, motion control and over 200 I/O functions. The G-windows GUI for real-time systems running. OS-9 is also offered. www.gespac.com or Phone 800-443-7722

CIRCLE 275

GESPAC INC.

A WEALTH OF SWITCH INFORMATION

Grayhill's 320 page catalog provides you with electromechanical switch data, reference material, dimensional drawings and photos. Catalog No. 1 includes information on DIP Switches, Rotary Switches, Keyboards and Keyboard Modules. The detailed information allows the catalog uses to select the proper product for their apliction right down to the part number. Phone: (708) 482-2131, Fax: (708) 354-2820.



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This new catalog features three new product lines and many additions to existing lines. Contains complete information on the company's axial and radial lead aluminum electrolytic, film, ceramic and power capacitors. It's all you need to make a knowledgeable capacitor selection. Contains full specifications, useful formulas and data, authorized distributor listings. 144-pages. 847-675-1760; fax 847-673-2850

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IRONWOOD ELECTRONICS

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Kent Displays' brochure details the benefits of No-Power™ Reflective Cholesteric Liquid Crystal Displays. This technology requires no energy to maintain an image. Displays have wide viewing angles and are flicker free. Call (330) 673-8784.

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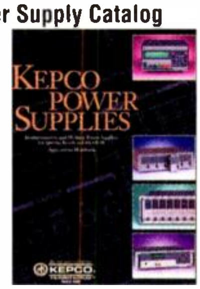
KENT DISPLAYS

Full-Color 1998 Power Supply Catalog

Kepco's new power supply catalog provides 178 full-color pages covering ac-dc and dc-dc modular power supplies and instrumentation power supplies, both analog-programmable and digitally-programmable. Digital models support GPIB/VISA/LabView/VXI and Kepco's single address multiple instrument protocol. Visit us at www.kepcopower.com for information. Tel: 718-461-7000, Fax: 718-767-1102.



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GIANT NEW SWITCH CATALOG

APEM's new 420 page full-line catalog is packed with their switch offerings. New products added: toggles, rockers, push-buttons, tacts, keys, industrial controls, DIPs, rotary DIPs, micro-limits, pushwheels, slides, keyboards, sealing boots. Many state-of-the-art switch models featuring process compatibility, surface mounting technology & electrostatic discharge withstanding. APEM Tel: 781-246-1007, Fax: 781-245-4531, URL: http://www.APEM.com E-Mail: info@APEM.com

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APEM

6050 I/O With I/Q

Octagon Systems has introduced a new family of single card industrial computers called the PC Microcontroller Series. The card family combines the industry standard PC architecture with industrial-class I/O and an extensive suite of embedded software in a small 4.5 X 4.9 package rated from - 40° to 85° C.

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OCTAGON SYSTEMS

NEW SHORT FORM CATALOG

Omron's Control Components Short Form Catalog contains 200-plus pages of relays, switches, photomicrosensors, card readers, photoelectric sensors, power supplies, totalizers, digital displays, temperature controllers and timers. Call 1-800-55-OMRON. E-mail: SFC2_EDLit@omron.com

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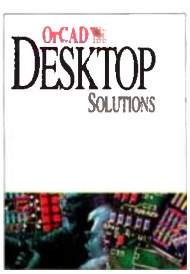

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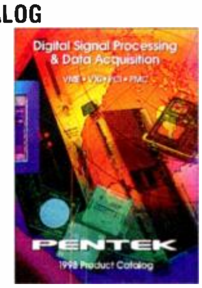
ORCAD

1998 PRODUCT CATALOG

Catalog provides full specifications on our VME, PCI, PMC and VXI product lines. You'll also find helpful tutorials, case studies and real-life applications stories. Get the latest information on the broadest line of DSP processors, including our new C6x, C80 and SHARC boards, advanced I/O peripherals and world-class software tools. (201) 818-5900, ext. 855, http://www.pentek.com, e-mail: info@pentek.com



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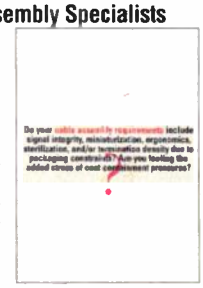
Precision Interconnect, a division of AMP Inc. has released a new brochure explaining their design and manufacturing approach for cable assemblies needing to perform in challenging electrical, mechanical or environmental applications. Solutions include miniaturization, dense packaging, precise electricals, sealed systems, etc. Phone (503) 620-9400: Fax (503) 620-7131.



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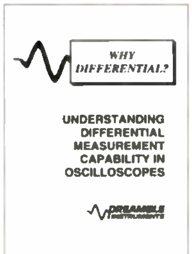
PRECISION INTERCONNECT

ELECTRONIC DESIGN CATALOG/LITERATURE REVIEW

DIFFERENTIAL MEASUREMENTS

A discussion of sing;e-ended and differential scope measurements on ground referenced and floating signals. differential amplifier characteristics such as common mode rejection ratio and commen mode range are covered. 1-800-376-7007



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PREAMBLE INSTRUMENTS

LIQUID CRYSTAL DISPLAYS

A division of Purdy Electronics has released its 1998 LCD short form catalog. The catalog features a full line of TFT and STN color panels and monitors plus intelligent graphic and character monochrome displays.

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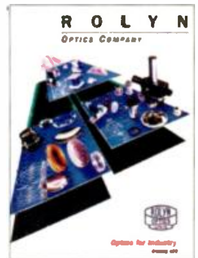

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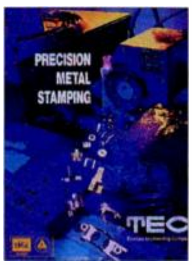

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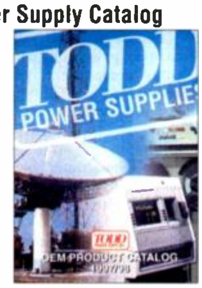
SPH-1200 (38 cents per watt in OEM quantities) and TCM-1000, TMX-350 (multiple output, 48 Vdc clone of RMX-350); TRS Todd Rack System for N+1 redundancy and front-panel hot plug. 180 standard swtiching power supplies 150 to 1500 watts, unlimited custom power solutions. 800-223-8633, 516-231-3366; FAX 516-231-3473; e-mail: info@toddpower.com; www.toddpower.com



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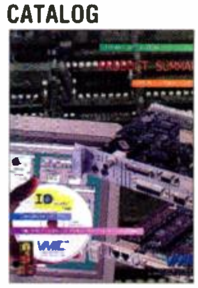
FREE VMIC PRODUCT CATALOG

VMIC's Product Summary Catalog features a wide selection of VMEbus I/O, VMEbus CPU's, Real-Time Networks using VMIC's reflective memory products for VME, PCI, CompactPCI, PMC, Multibus, IOWorks component software, and a host of other products designed to provide complete, open solutions from one vendor. 12090 South Memorial Parkway, Huntsville, AL 35803-3308; 800-322-3616; http://www.vmic.com



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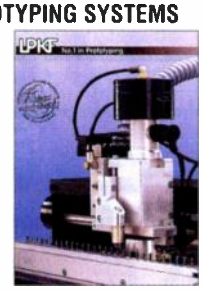

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Z-World's new 1998 product catalog with new additions to our product line and some exciting new applications. We provide C-programmable controllers, software, core modules, LCD and keypad interfaces, graphic displays, and other control related devices programmed with Dynamic C[*]. Save time, money on controllers for embedded systems, machine control OEM industrial applications. 1-500-757-3737; fax: 1-530-753-5141; web:www.zworld.com

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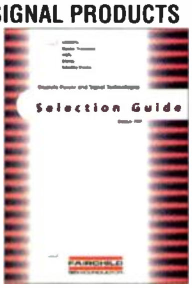
CIRCLE 300

ICP ACQUIRE, INC.

DISCRETE POWER & SIGNAL PRODUCTS

A new Discrete Power and Signal Technologies Selection Guide provides engineers with selection criteria for Fairchild Semiconductor's comprehensive lines of MOSFETs, Bipolar Transistors, JFETs, Diodes, and Schottky Diodes. Electronic version available on the web at www.fairchildsemi.com/products/discrete/dsg.html. Fairchild Semiconductor, Sunnyvale, California.

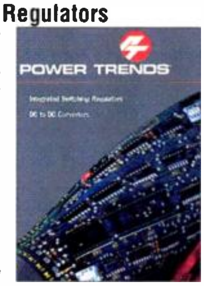


CIRCLE 301

FAIRCHILD SEMICONDUCTOR

Integrated Switching Regulators

DC to DC converters Power Trends' new 120 page full-line catalog details their complete line of Integrated Switching Regulators (ISRs) and DC to DC Converters. Catalog introduces significant new 5V, 12V, and 24V bus products along with extensions to existing product lines. Catalog is also available on CD-ROM. (800) 531-5782; fax: (630) 393-6902; e-mail:sales@powertrends.com.; www: http://www.powertrends.com



CIRCLE 302

POWER TRENDS, INC.

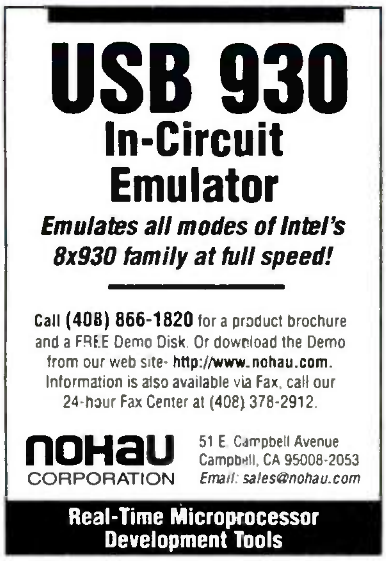
ENCLOSURES & ACCESSORIES

Bud Industries' new Standard Products Catalog provides technical data and ordering information on over 3,000 products ranging from large relay racks and cabinets to desktop and portable instrument cases including a full line of NEMA and other plastic enclosures. Also included is information on computer workstations, custom fabrication and a wide range of enclosure accessories.

CIRCLE 303

BUD INDUSTRIES, INC.

PROTO EXPRESS CIRCLE 416



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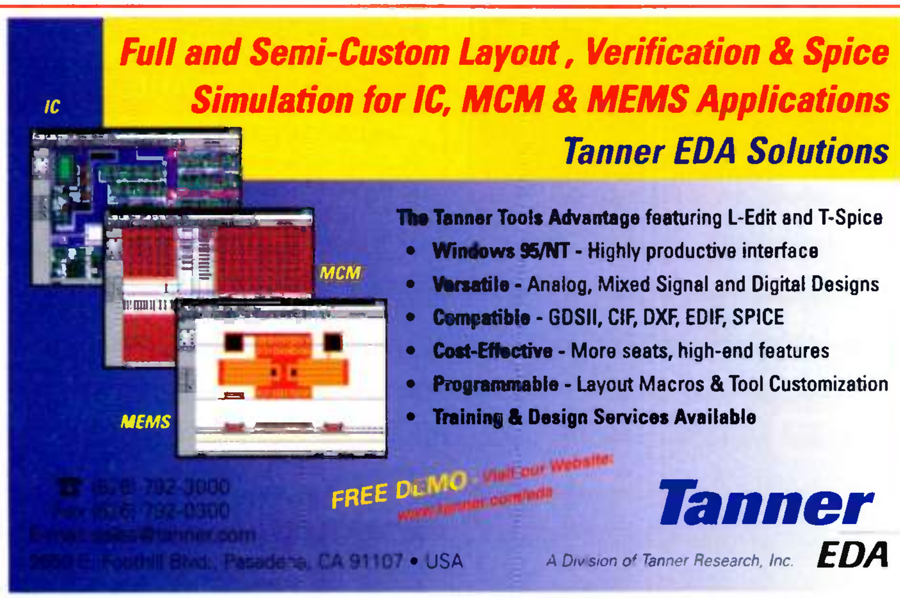

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in^2	SS	DS	4L	6L	8L	10L
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33 to 72	$290	$320	$520	$620	$850	$1200
73 to 108	$325	$340	$580	$690	$960	$1450
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73 to 108	$360	$420	$700	$820	$1450	$2200
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