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TECHNOLOGY · APPLICATIONS · PRODUCTS · SOLUTIONS

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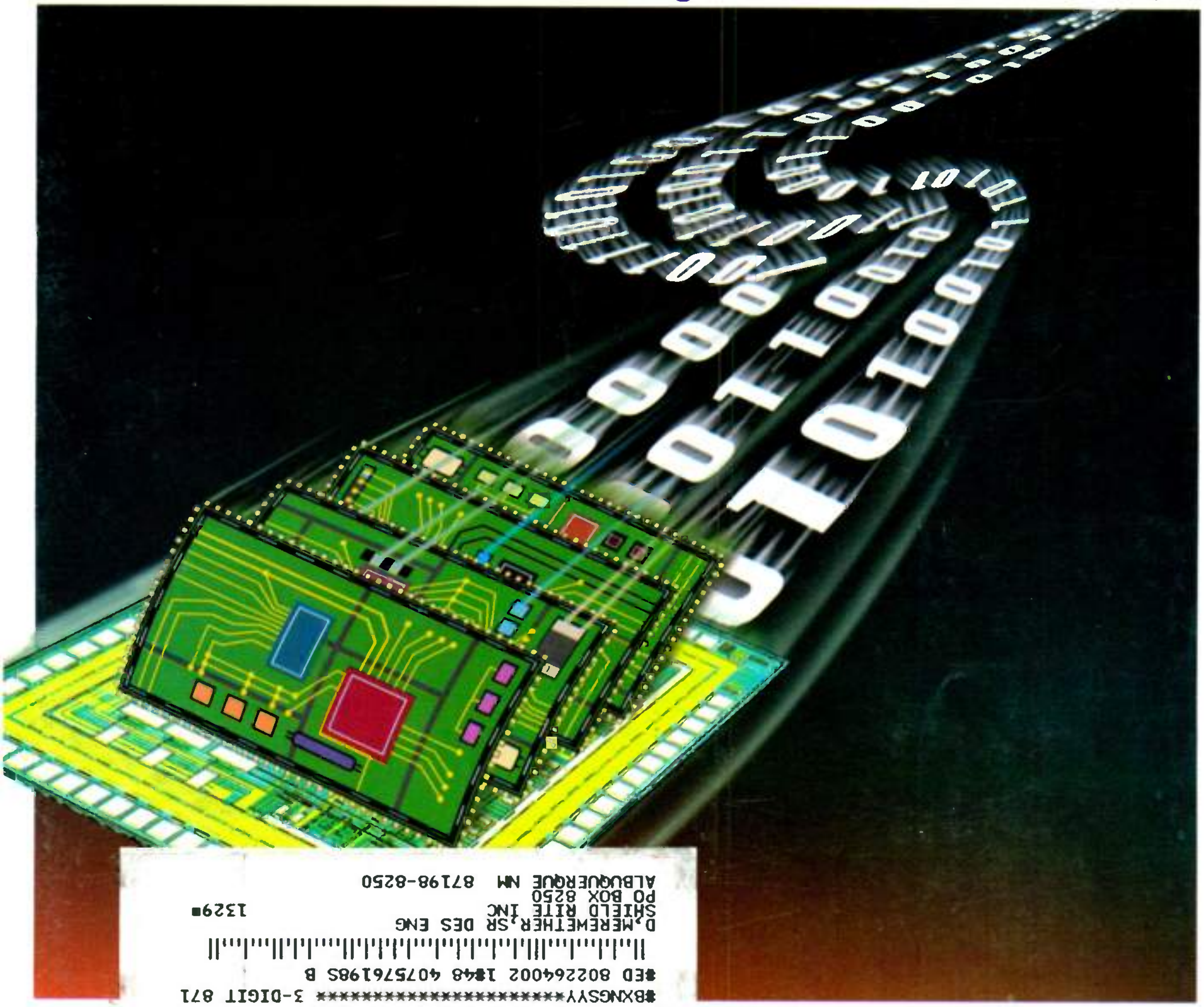

Low-Voltage Differential Signaling Reports For Bus Duty p. 39

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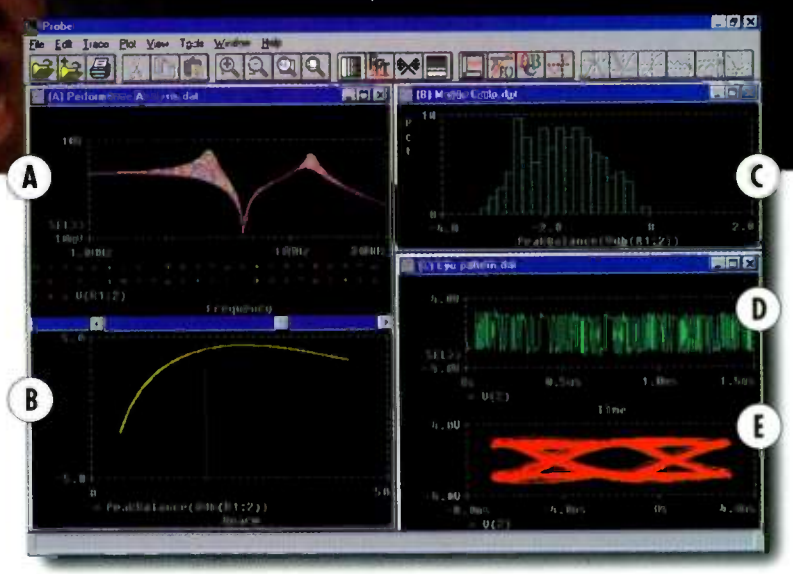

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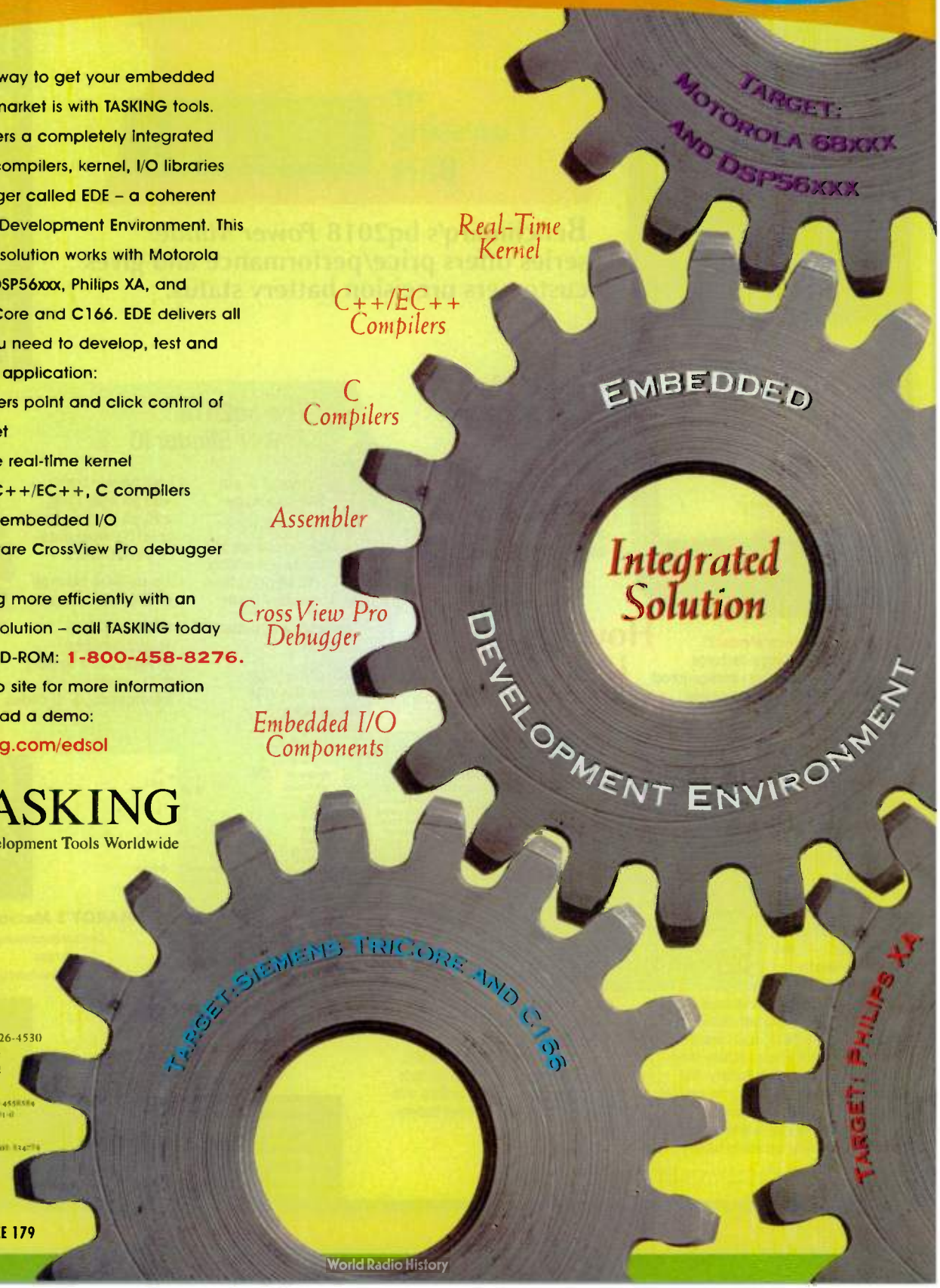

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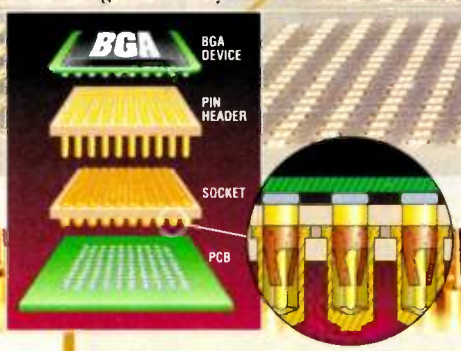

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May 25, 1998 Volume 46, Number 12

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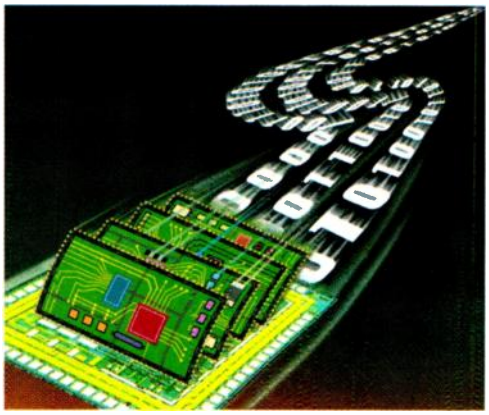

TECH INSIGHTS

DSP

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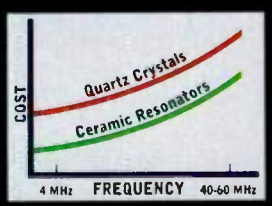

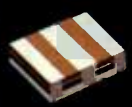

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May 25, 1998 Volume 46, Number 12

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QUICKLOOK

LOOKING AHEAD: June 8, 1998

- **PIPS/Packaging:.....** A special expanded version of Patrick Mannion's PIPS section includes the latest technology trends and design tips on the critical issue of IC packaging.
- **Communications Technology:....** Communications Technology Editor Lee Goldberg examines what LAN and WAN technologies are doing to meet growing bandwidth requirements using gigabit transmission technologies.
- **Computer Boards & Buses:.....** Learn what our Computer Systems Editor Jeff Child found out at a recent roundtable discussion with leading bus-board industry experts on the newest mezzanine standard, PC•MIP.

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Jesse H. Neal Editorial Achievement

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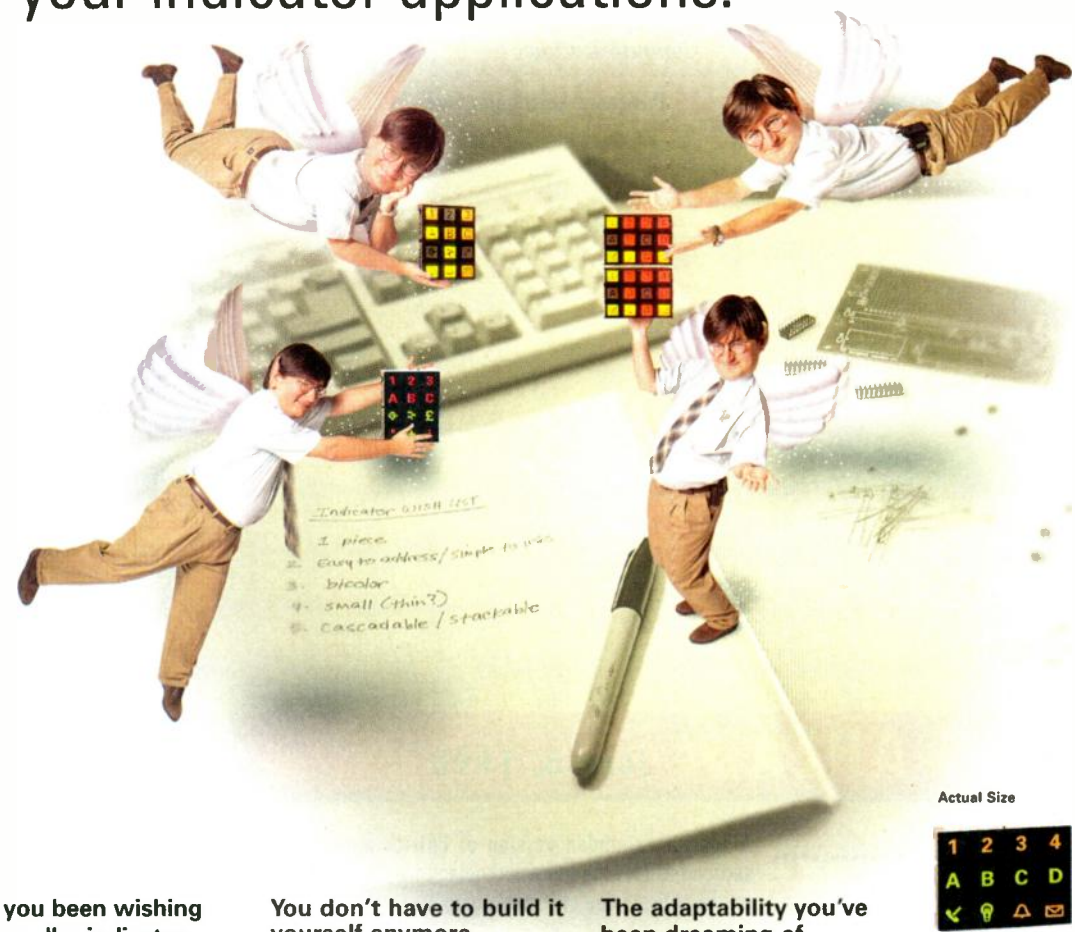

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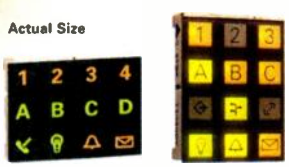

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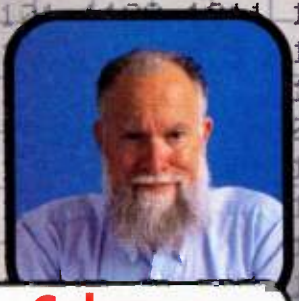
Technology Lab

Divided into eight design-specific sections–Analog Design, Communications/Networking, Components/Packaging (PIPS), Computer Boards & Buses, Digital Design, Electronic Design Automation (EDA), Embedded Systems & Solutions, and Test & Measurement–you can find the technical information you need right away.



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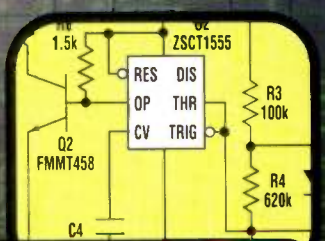
Get the latest on what's happening in the industry in the News Page. You'll read items such as what the government is doing to help solve the Y2K problem, or whether or not you can recharge your laptop computer on an airplane. Stay tuned to the News Page!



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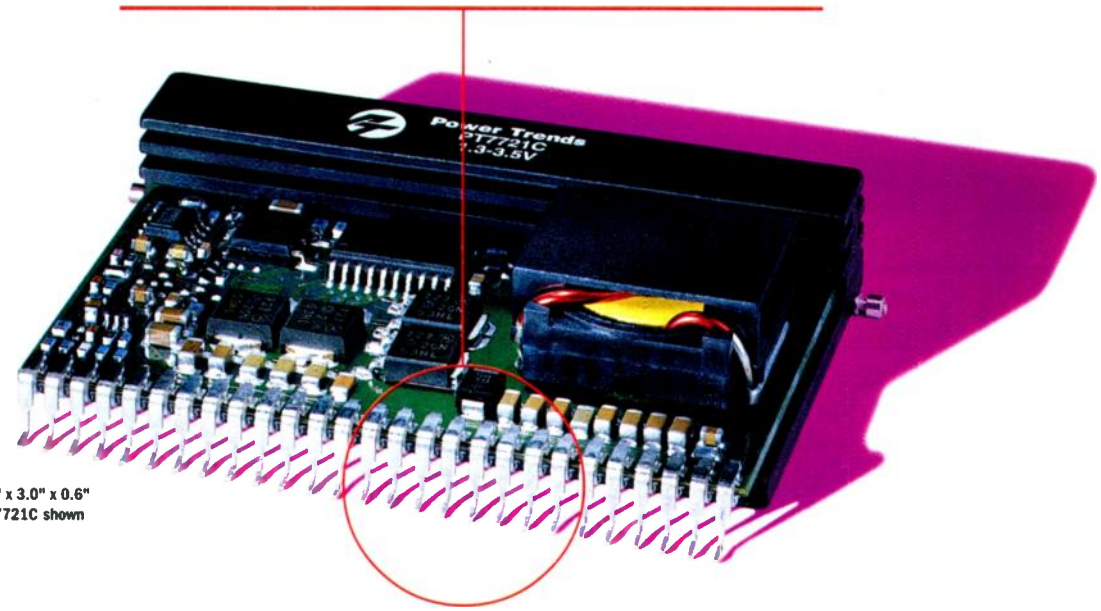

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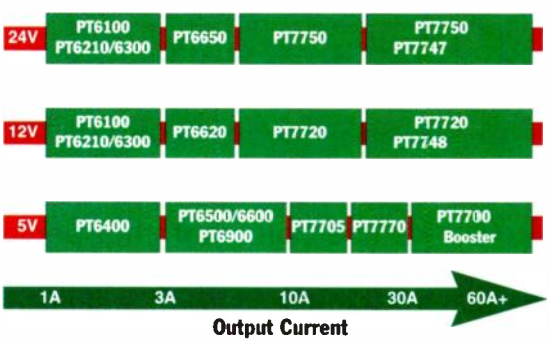

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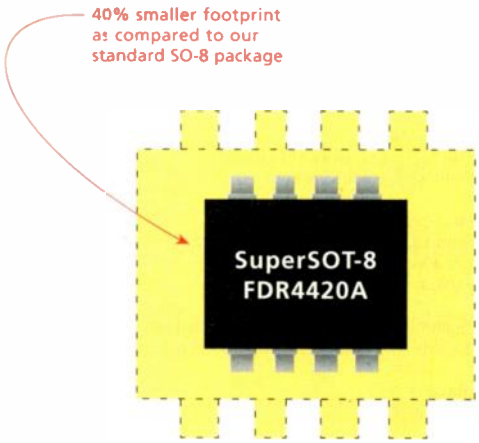

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IEEE International Conference on Communications (ICC '98), June 7-11. Atlanta, GA. Contact Judy Keller, IEEE Communications Society, 345 E. 47th St., New York, NY 10017; fax (212) 705-7865; e-mail: j.keller@ieee.org.

IEEE International Symposium on Electrical Insulation, June 7-11. Key Bridge Marriott Hotel, Arlington, VA. Contact David R. James, Oak Ridge National Laboratory, P.O. Box 2008, Bldg. 4500S, MS-6123, Oak Ridge, TN 37831-6123; (423) 574-6213; fax (423) 574-6210; e-mail: dyj@ornl.gov.

IEEE/MTT-S International Microwave Symposium (MTT '98), June 7-12. Baltimore Convention Center, Baltimore, Maryland. Contact Steven Stitzer, Westinghouse Electric Corp., P.O. Box 1521, MS 3T15, Baltimore, Maryland 21203; (410) 765-7348; fax (410) 993-7747.

Electro '98/Nepcon East, June 9-11. Bayside Exposition Center, Boston, MA. Contact Electro '98, P.O. Box 552, Brookfield, IL 60513-0552; (800) 467-5656; (203) 840-5656; fax (708) 344-4444; http://electro.reedexpo.com.

IEEE Symposium on VLSI Technology, June 9-11. Honolulu, HI. Contact Melissa Widerkehr, Widerkehr & Associates, 101 Lakeforest Blvd., Suite 270, Gaithersburg, MD 20877; (301) 527-0900; fax (301) 527-0994; e-mail: widerkehr@aol.com.

IEEE Symposium on VLSI Circuits, June 11-13. Honolulu, HI. Contact Phyllis Mahoney, Widerkehr & Associates, 101 Lakeforest Blvd., Suite 270, Gaithersburg, Maryland 20877; (301) 527-0900; fax (301) 527-0994; e-mail: pwmahoney@aol.com.

USENIX 1998 Technical Conference, June 13-17. Marriott Hotel, New Orleans, LA. Contact USENIX Conference Office, 22672 Lambert St., Suite 613, Lake Forest, CA 92630; (714) 588-8649; (714) 588-9706; e-mail: conference@usenix.org; www.usenix.org.

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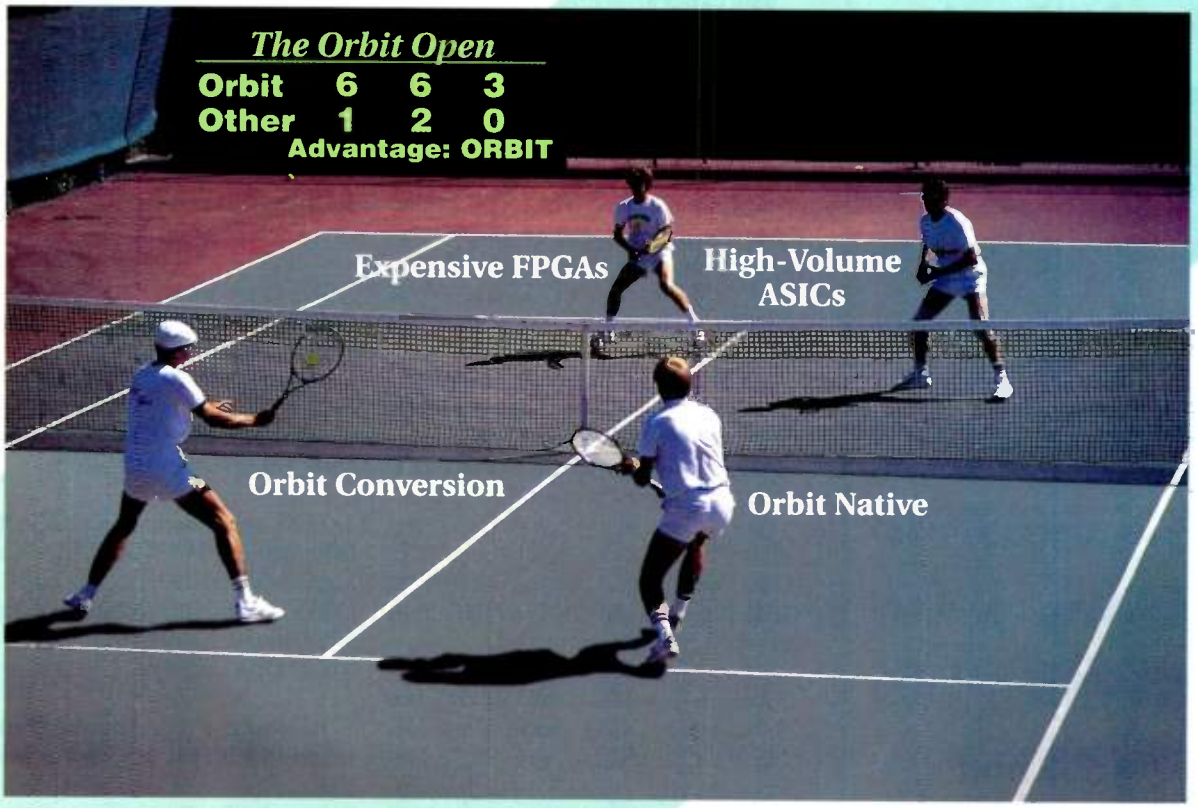

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Exhibition & Conference on System Integration in Microelectronics, June 16-18. Nuremberg Exhibition Centre. Call +49 711-61946-26/-74; fax +49 711-61946-93; www.mesago.de

IEEE Antennas and Propagation Society International Symposium and URSI National Radio Science Meeting, June 21-26. Stouffer Renaissance Waverly Hotel, Atlanta, GA. Contact Andrew Peterson, Georgia Institute of Technology, School of Electrical & Computer Engineering, ECE 0250/Van Leer, Atlanta, GA 30332; (404) 894-4697; fax (404) 894-4641; e-mail: peterson@ee.gatech.edu.

American Control Conference (ACC '98), June 24-26. Adams Mark Hotel, Philadelphia, PA. Contact Joe Chow, ECSE Department Rensselaer Polytechnic Institute, Troy, NY 12180-3590; (518) 276-6374; fax (518) 276-6261; e-mail: chowj@rpi.edu.

JULY

Conference on Precision Electromagnetic Measurements (CPEM '98), July 6-10. Renaissance Washington Hotel, Washington, D.C. Contact Katherine H. Magruder, NIST, Bldg. 220, Room B162, Gaithersburg, MD 20899; (301) 975-2402; fax (301) 926-3972; e-mail: katherine.magruder@nist.gov.

Second IEEE World Conference on Photovoltaic Energy Conversion (WCPEC), July 6-10. Vienna, Austria. Contact Heinz Ehmann, WIP, Sylvensteinstrasse 2, D-81369 Munchen, Germany.

IEEE International Geoscience & Remote Sensing Symposium (IGARSS '98), July 6-10. Sheraton Seattle, WA. Contact Tammy I. Stein, IGARSS Business Office, 2610 Lakeway Dr., Seabrook, TX 77586-1587, (281) 291-9222; fax (281) 291-9224; e-mail: tstein@phoenix.net.

ASIC Design Bridge Camp II (Digital Design), July 6-17. Professional Development Centre, Faculty of Applied Science and Engineering, University of Toronto, Ontario. Contact Ianita Ivanova, (888) 233-8638; (416) 978-3907; fax (416) 971-2141; e-mail: ivanova@ecf.utoronto.ca; www.ecf.utoronto.ca/apsc/cee.

Gignet, July 7-10. World Trade Center, Boston, MA. Contact Technology Transfer Institute, (310) 394-8305; (800) 200-4884; fax (310) 451-2104; e-mail: custserv@tticom.com; www.tticom.com/gignet.

IEEE Power Engineering Society Summer Meeting, July 12-16. Sheraton San Diego Hotel & Marina, San Diego, CA. Contact Terry Snow, San Diego Gas & Electric, P.O. Box 1831, San Diego, CA 92112; (619) 696-2780; fax (619) 699-5096; e-mail: t.snow@ieee.org.

SPIE's Annual Meeting & Optical Instrumentation Show, July 19-24. San Diego, California. Contact SPIE Exhibits Dept., Post Office Box 10, Bellingham, Washington 98227-0010; (360) 676-3290; fax (360) 647-1445; e-mail: exhibits@spie.org.

IEEE Nuclear & Space Radiation Effects Conference (NSREC '98), July 20-24. Newport Beach, California. Contact Jim Schwank, Sandia National Laboratories, Post Office Box 5800, MS-1083, Albuquerque, New Mexico 87185-1083; (505) 844-8376; fax (505) 844-2991; e-mail: schwanjr@sandia.gov.

ASIC Design Bridge Camp II (Analog, Layout, and Fabs), July 20-31. Professional Development Centre, Faculty of Applied Science and Engineering, University of Toronto, Ontario. Contact Ianita Ivanova, (888) 233-8638; (416) 978-3907; fax (416) 971-2141; e-mail: ivanova@ecf.utoronto.ca; www.ecf.utoronto.ca/apsc/cee.

AUGUST

IEEE International Symposium on Information Theory, Aug. 16-21. Massachusetts Institute of Technology, Cambridge, MA. Contact G. David Forney, Motorola Inc., MS M4-15, 20 Cabot Blvd., Mansfield, MA 02048-1193; (508) 261-5347; fax (508) 337-7173; e-mail: LUSE27@email.mot.com.

IEEE International Symposium on Electromagnetic Compatibility (EMC '98), Aug. 23-28. Adam's Mark Hotel, Denver, CO. Contact R. Barry Wallen, P.O. Box 387, 1350 County Rd., #16, Rollinsville, CO 80474; (303) 682-6600; fax (303) 682-6672; e-mail: bwallen@intellistor.com.

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EDITORIAL

We Need Your Opinion

A few weeks from today, our worldwide staff of editors, writers and correspondents will gather in New York City for our annual three-day editorial planning meeting. This year's meeting will be held at the historic Algonquin Hotel, located on West 44th Street in the heart of Midtown Manhattan.

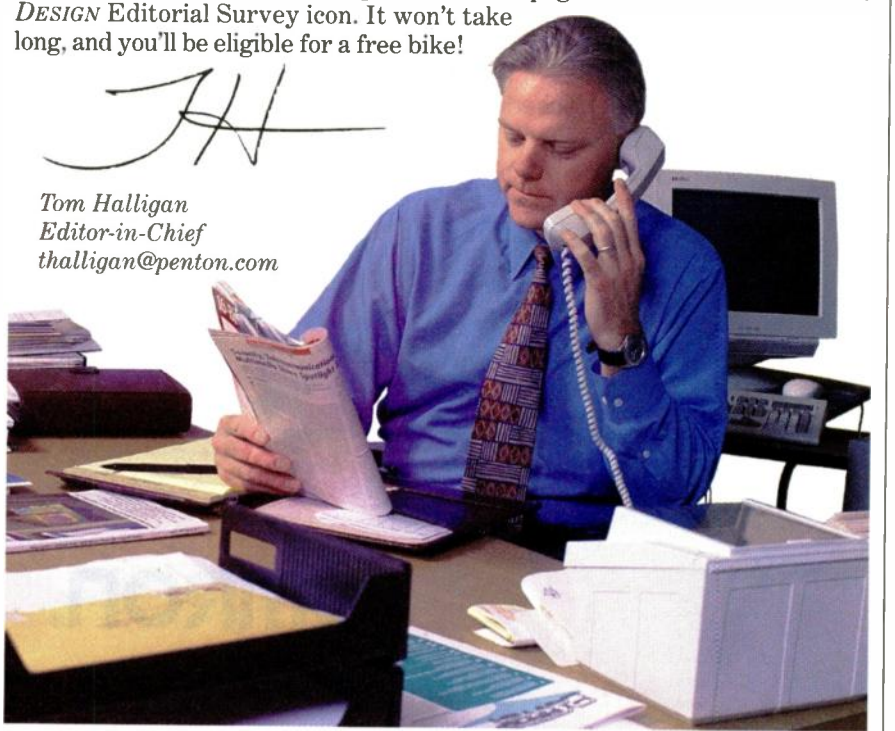
I chose the Algonquin for our meeting because of its legendary status as the gathering place of some of the most renowned figures in literary and publishing history. Such notable figures as H. L. Mencken, Gertrude Stein, Sinclair Lewis, Simone de Beauvoir, and William Faulkner regularly stayed at the hotel. In fact, the hotel's most enduring literary legacy derives from an unlikely, but brilliant group of up-and-coming writers who, for 10 years during the 1920s, lunched daily at what eventually became the famous Round Table. Some of the members included Dorothy Parker, Robert Benchley, and Robert E. Sherwood.

With its long tradition as a Mecca for writers, the Algonquin will provide the atmosphere for spirited discussion and debate during our annual editorial meeting. The main purpose of the meeting is to plan our editorial coverage for 1999. But, we also plan to spend many hours discussing everything and anything that could improve our editorial coverage of the industry, the quality of the magazine, and our ancillary publications.

Now here's where you come in. We need your input to make sure we're delivering the kind of magazine that helps you excel at your job. We'll be conducting an online editorial survey on our web page (*www.elecdesign.com*) during June, and I invite you to participate. And, to entice you further, we're going to hold a drawing to give away a top-notch bicycle to one respondent (subscribers only) after the editorial survey is completed at the end of the month.

So, not only do you have the chance to win a bike, more importantly, you have the opportunity to help us shape our editorial coverage. The readership survey results will be presented at our editorial meeting, and I'm sure we'll have lively debates over your opinions.

Our goal is simple. We intend to continue to be the leading technical magazine for design engineers and engineering managers. We value you as readers, and we respect your opinions. All of our editors and writers look forward to hearing from you. All you have to do is go to our home page and click the *ELECTRONIC DESIGN* Editorial Survey icon. It won't take long, and you'll be eligible for a free bike!



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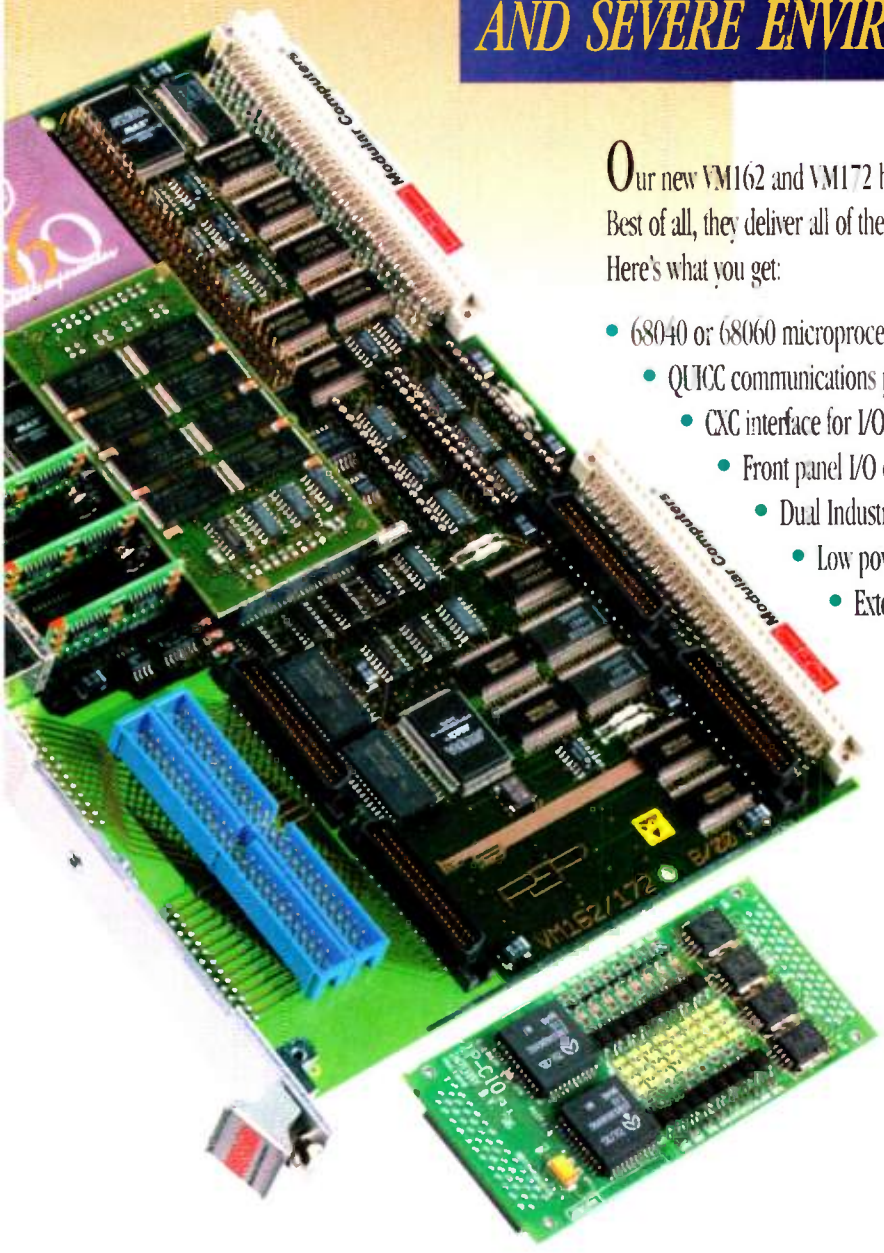

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READER SERVICE 117

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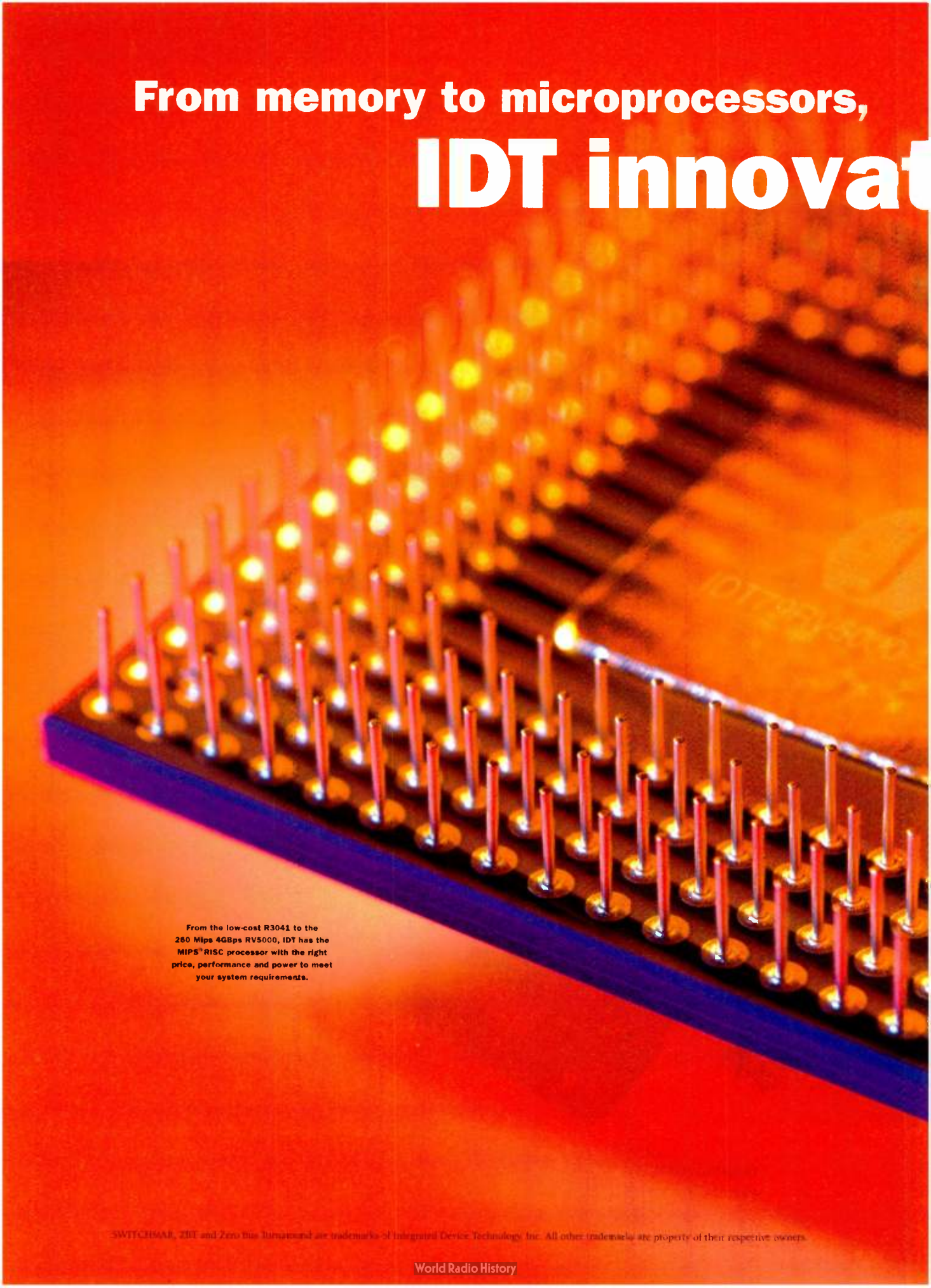

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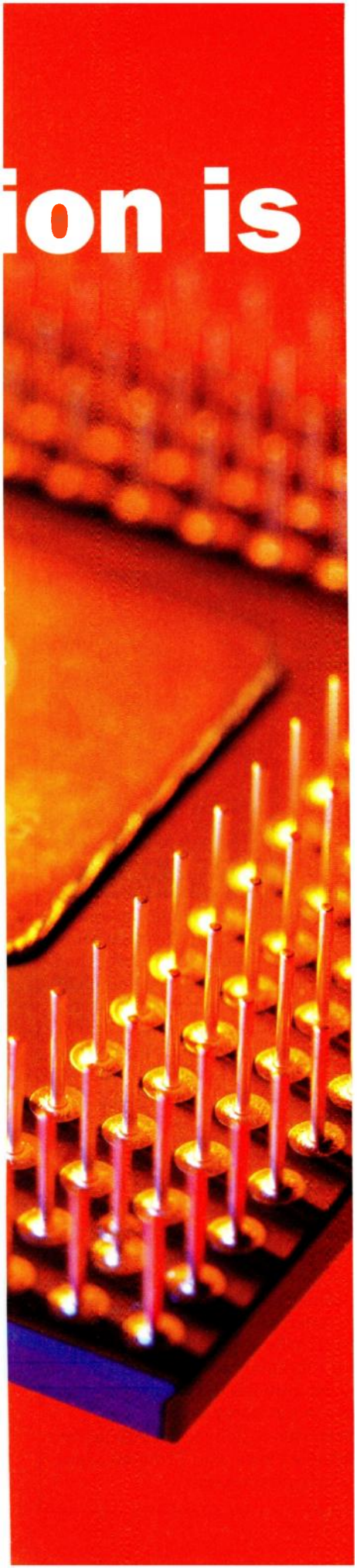

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READER SERVICE 187

It's DAC Time Again

It seems like only yesterday that I recovered from all the hoopla of the 1997 Design Automation Conference (DAC), and now I find that it's less than one month until DAC 1998. This year, the event is scheduled to take place in San Francisco's Moscone Center, June 15-19. Right about now, nearly everyone in the EDA industry is preparing to live through all the excitement yet again.

If you're an EDA vendor, you go to DAC because if you don't, everyone in the industry will wonder *why* you didn't. After all, DAC is a sort of right of passage. It's how you know when you've made it as a legitimate EDA company—if you're large enough or profitable enough, you get a booth at DAC. If you're an EDA tool user you go because it's the one place where you can survey new tool offerings, and find solutions to some of the design problems you just can't seem to fix. It's also a place to see the new problems that you can expect to affect your designs in coming months.

And let's be honest, we all go for the toys. Last year alone I came home with two bags full of everything from assorted clothing to a window squeegee and oversized beach umbrella. My husband quickly confiscated the clothing and my daughter latched on to the stuffed animals. I was left with barely a handful of candy. If I'm smart this time around I'll hide the goodies before I get home.

CHERYL AJLUNI
ELECTRONIC DESIGN AUTOMATION

In any event, this year's DAC, goodies or not, promises to be quite an exciting and worthwhile event. With a focus on the critical design issues plaguing today's designer, the conference will highlight how to deal with faster clock speeds, and growing complexity and capacity, while still developing advanced electronic products. In particular, some of the major trends that will be discussed include deep-submicron design, hardware/software co-verification and co-design, verification in general, intellectual property (IP), and systems design.

One of the new events added to the line-up is the Silicon Village; an area on the exhibit floor dedicated to silicon vendors that will feature over 20 semiconductor and IP vendors and their products. Silicon Village was established as a way to address the growing interdependence between silicon and EDA vendors, and is a prime example of how ASIC and EDA companies are working together to meet the challenges facing the industry today.

This year's DAC will also feature a special workshop titled, "Forget the Ceiling—Breaking the Glass." The workshop, scheduled for Sunday June 14, 9:00 a.m. to 4:00 p.m., proposes to help women identify the behaviors and attitudes in themselves that may be holding them back in their careers, to help them learn how highly successful women made it to the top of their chosen fields, and to teach women to develop a personal plan for career advancement. The intention is to help women begin to break the barriers that have traditionally kept them from advancing in technical fields.

This event is significant because although in recent years a small, but steadily growing stream of women have entered the electronics field, traditionally this segment of the industry has been dominated by men. Workshops such as this one will help by showing how women can succeed in this career track. But, it will take much more than a workshop to change the male-dominated landscape of the electronics industry. It will require the industry to come together as a whole to devise ways of encouraging women to pursue careers in the electronics industry, and for each individual, man and woman alike, to change the way they perceive women in the workplace.

Whatever your interest in EDA, DAC promises to deliver something for everyone. Just don't forget to wear comfortable shoes, and bring an extra piece of luggage for all the toys you collect. *cjajluni@class.org.*

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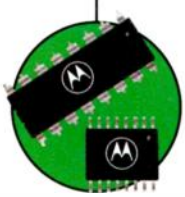

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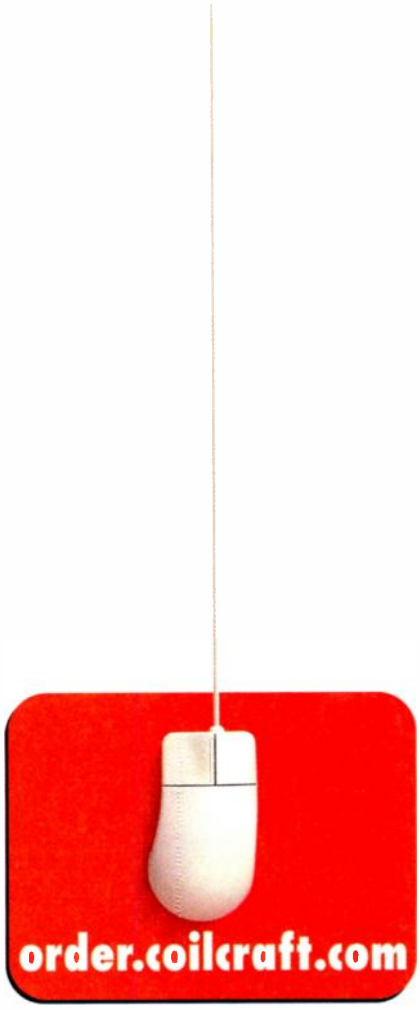

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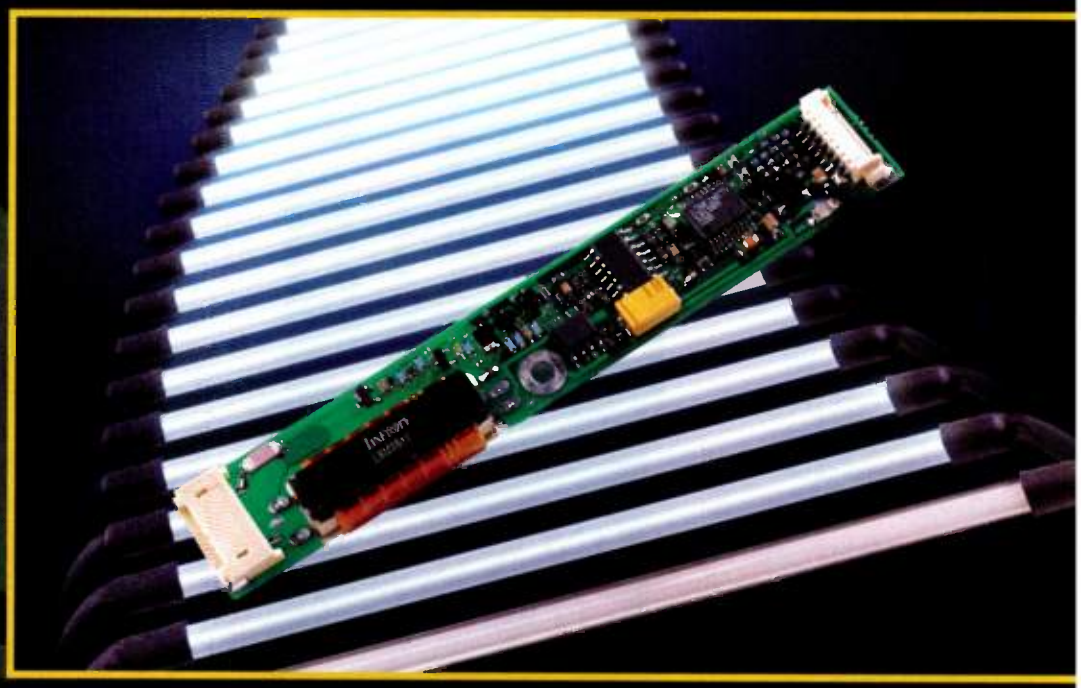

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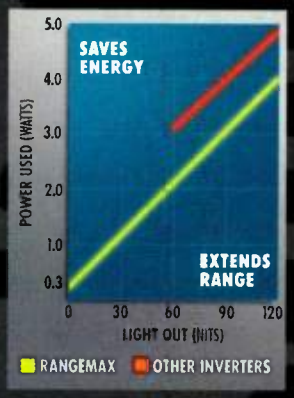

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READER SERVICE 113

Java-Based Specification Emerges For Smart Cards

At last month's CardTech/SecurTech conference in Washington D.C., the OpenCard Consortium revealed the OCF (OpenCard Framework) 1.0. OCF 1.0 is a Java-based smart-card specification that enables interoperability between smart cards and network devices or readers, including PC readers, ATM machines, set-top boxes, and merchant-site readers.

While advances in security, single-sign-on, and commerce applications have increased awareness of smart-card technology, a general lack of standards has prevailed. The OFC spec is expected to change that, though. OFC specifies two interfaces: One is a high-level application programming interface that hides the characteristics of a particular provider's components (either a specific type of smart card and/or smart-card terminal) from the application and service developers. The second is a common provider interface that enables the seamless integration of smart-card building blocks from different vendors.

The goals of the framework are to spur application development, with the ultimate goal of making the smart-card infrastructure as ubiquitous as the credit-card infrastructure. At the show, IBM, Armonk, N.Y., showcased multifunction cards with embedded public keys based on OCF 1.0. Microsoft Corp., Redmond, Wash., introduced a Microsoft- branded smart card for use with Windows NT and Windows 98.

For more information about the Open Card Framework, browse through their web site at *www.opencard.org*, or e-mail the Consortium at *opencard-info@opencard.org*. JC

8-VSB Measurements Will Ensure Digital-Signal Quality

Tektronix Inc. recently demonstrated a new 8-VSB (eight-level vestigial sideband) broadcast measurement capability. While digital transmission will enhance TV broadcasting with features like HDTV and data services, more care is required to ensure that the highest-quality signal is being made available to the consumer.

The capability to perform 8-VSB measurements will be required by all broadcasters in the U.S. as they implement the new ATSC (Advanced Television Systems Committee) DTV standard. The Tektronix 8-VSB technology assists broadcasters in making the transition from analog to digital television.

Zenith developed the 8-VSB digital transmission system adopted by the FCC as part of the ATSC standard for terrestrial DTV broadcasts. Tektronix collaborated with Zenith on the 8-VSB test suite to create a system that's expected to be a reference for compliance with the ATSC standard.

For more information on 8-VSB testing, contact Tektronix Measurement Business Div., Box 3960, Portland, OR 97208-3960; (800) 426-2200 (press 3, code 1071); fax (503) 222-1542; *www.tek.com/Measurement*. JD

ETSI, ITU-T Conformance Tests Targeted For Digital Interfaces

Network operators are constantly challenged by the growing volume of data traffic from commercial and private users. To ensure the basic conditions necessary for trouble-free data communications are met, these operators must comply with certain standards defined by national and international bodies.

Wandel & Goltermann has produced an application note that describes a set of standardized tests on digital interfaces. These tests can be used to comply with the European Telecommunications Standardization Institute (ETSI) and International Telecommunication Union (ITU-T) norms.

Included in the application note is a listing of eight standards, which cover the interfaces used in ISDN, business telecommunications, and the open network provision (ONP). Another listing shows the measurements needed to test each standard, such as input and output return loss, longitudinal conversion loss, output signal balance, impedance toward ground, and tolerable longitudinal voltage.

The application note was drafted for engineers and technicians who work for network operators and manufacturers of terminal equipment, as well as those who deal with the electrical properties of digital interfaces. The application note is available for free on the Wandel & Goltermann web site (search keyword: AN 57).

For more information, contact Wandel & Goltermann GmbH & Co., Marketing International, Postfach 1262, D-72795 Eningen, Germany; +49 7121 86-1616; fax: +49 7121 86-1333; e-mail: *info@wago.de*; *www.wg.com*. JD

Archival Storage Scheme Packs 95,000 Images On A 2-in. Disk

An archival data-storage system that permits up to 95,000 images to be stored on a new 2-in. disk format promises the densest storage technology to date. Detailed by Norsam Technologies Inc., Los Alamos, N.M., at the May AIIM Conference in Anaheim, Calif., the HD-Rosetta technology uses an ion beam process to create microscopic reproductions —as small as 20 by 30 µm—of human eye-readable images from microfilm,original documents, or other media. The images are first captured using digital technology and then converted back to analog form

and drawn on a durable metal master disk, referred to by the company as a Pancake Disc. That master disk then can be used to create low-cost distribution copies.

Unlike magnetic or CD-based data-storage systems (which require a computer and bit-stream interpreter to view information), the contents of the HD-Rosetta disk can be viewed with a high-powered microscope. This ensures that the information stored on the disk will never be unreadable due to hardware obsolescence. As a result, it can be readable as long as the disk surface remains intact—potentially for thousands of years into the future—without the aid of any special software or computer hardware. Because of this feature, several federal agencies, including the Library of Congress, and the National Library of Medicine, have shown interest in the HD-Rosetta concept and are currently testing the process.

The metal disks are formed from corrosion-proof material, can survive most fires, and are free of the rigid environmental storage criteria that most common storage media (paper, magnetic tape, and microfilm) require. An ion-beam writer is set up at the company's service bureau facility in Los Alamos, near the Los Alamos National Laboratory where the system was first developed. Contact Steve Sukman at (505) 983-0473. DB

VisualDSP Development Garners Third-Party Support

To aid developers in cutting tool integration time, as well as ensuring interoperability among third-party software suppliers, some 15 DSP hardware and software tools providers have announced support for Analog Devices Inc.'s integrated VisualDSP environment. Designed to provide a single graphical framework, the VisualDSP comprises an integrated development environment (IDE) and debugger that enables designers to define a DSP system, edit source files, and debug a project. However, the current release of VisualDSP supports ADI's 32-bit ADSP-2106x SHARC DSP processors, while support for 16-bit fixed-point DSPs is planned for later in the year.

A wide variety of application programming interfaces (APIs) within the VisualDSP toolset facilitate integration with development tools from other vendors. This allows designers to seamlessly migrate from one DSP to another with the same set of tools within that environment. The aim is to eliminate the need for learning new tools as the designer moves from one DSP system to another.

In short, the environment is focused on speeding up the time-to-market systems based on the ADI DSPs. But, the extensive set of APIs within VisualDSP don't preclude DSP processors from other major vendors, according to Lori Berenson, marketing manager for Analog Devices' DSP development tools. In fact, Analog Devices is expecting the support list to grow rapidly, propelling VisualDSP toward becoming an open DSP development environment. VisualDSP runs on both Windows 95 and Windows NT.

For additional information, call Lori Berenson at (781)-461-3735 or check out the Analog Devices' web site at *www.analog.com*. AB

Voice-Intelligibility Processor Technology Rolls Out

SRS Labs Inc., a developer and licenser of audio- and voice-enhancement technologies, announced the introduction of VIP (voice-intelligibility processor) technology at the NSCA Convention in Las Vegas, Nev. The NSCA (National Systems Contractors Association) provides the ideal setting for the VIP's introduction to the community responsible for manufacturing and installing public address and sound re-enforcement equipment.

VIP is a patented voice technology that offers major improvements in audio intelligibility, particularly in environments with high levels of ambient noise. The VIP technology has been issued one United States patent, with additional foreign patents pending.

VIP is based on psychoacoustic principles of the human hearing system. Specifically, its approach to increased recognition is based on the speech patterns and frequency distribution of the human voice. VIP selectively enhances, in real time, the voice portions of an audio signal. Then it individually amplifies and selectively weighs them. Finally, the processed voice sound and unprocessed baseband voice components are combined to provide an output signal of greatly improved intelligibility with minimum increase in the amplitude of the speech. Aside from increasing speech intelligibility, the VIP process enhances music quality in noisy reverberant spaces. It's also compatible with other voice technologies, including voice recognition, voice cancellation, and voice filtering.

SRS Labs will offer a stand-alone unit that can be added to the audio path of most any PA system or audio installation using common connectors. Next will be the availability of DSP Code for porting to most platforms where DSP is used to facilitate instruction; C-Code where the technology is used in voice-processing and voice-recognition software; and Custom Core digital signal processors from any number of SRS Labs chip partners.

VIP was developed originally at the Hughes Aircraft Co. by award-winning inventor Arnold Klayman, who is now a principal audio scientist at SRS Labs.

For more information, contact SRS Labs at 2909 Daimler St., Santa Ana, CA 92705; (714) 442-1070; fax (714) 852-1099; *www.srslabs.com*. JC

Edited by Roger Engelke

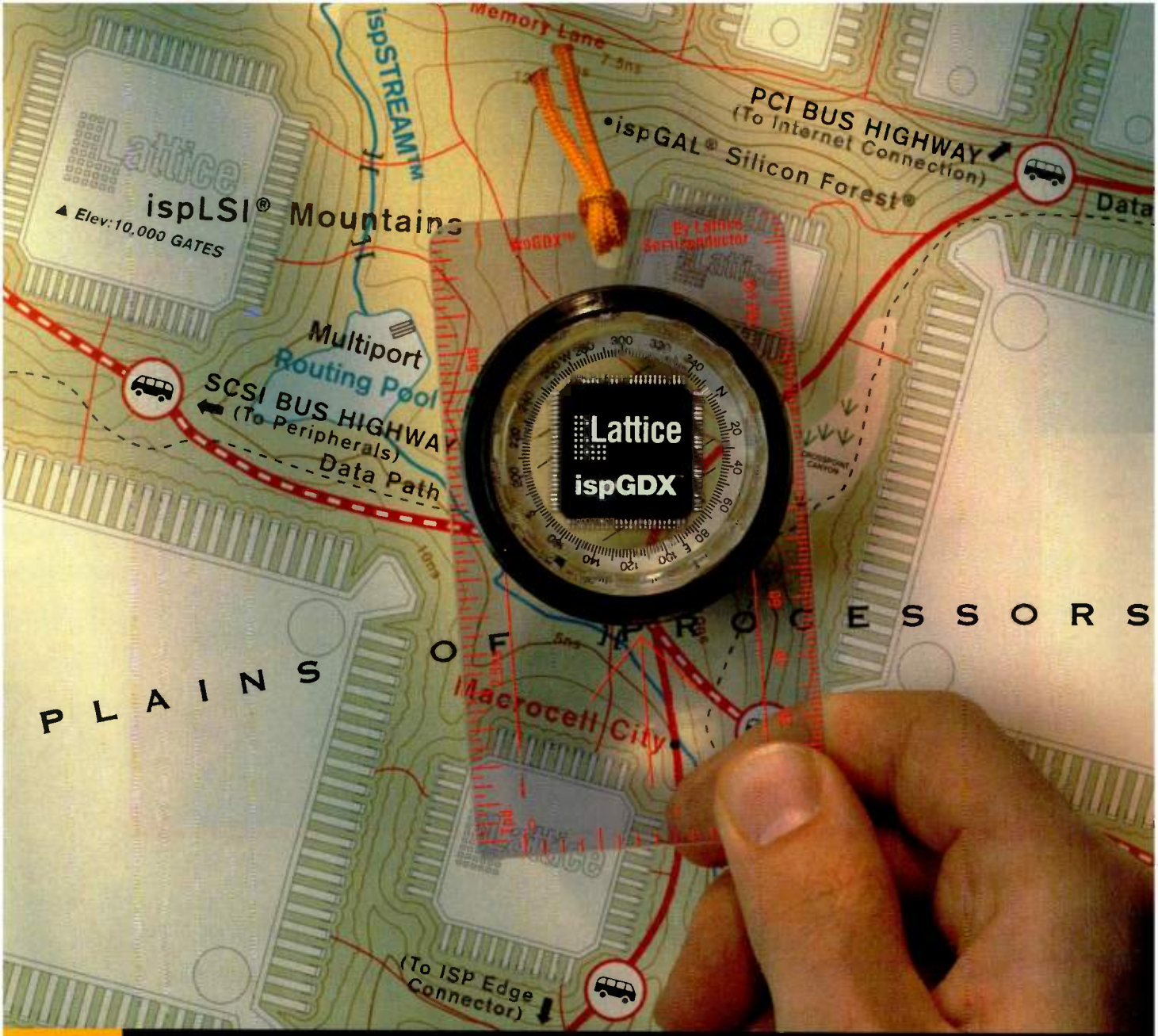
AT 166 MHZ, YOU CAN FEEL THE POWER OF OUR 4-MEG SRAMS.

Partial Selection	Access Time (ns)	Max. Freq.
256K x 18 pipelined	3.5 to 4.0	166 MHz
128K x 36 pipelined	3.5 to 4.0	166 MHz
256K x 18 flow-through	7.5, 8, 8.5, 10	117 MHz
128K x 36 flow-through	7.5, 8, 8.5, 10	117 MHz

Designers building the next generation of hot products for applications such as networking, communications and servers have high speed on their minds. ■ Galvantech is shipping high speed, high performance SRAMs today. Our 4-Meg synchronous burst SRAMs operate from a 3.3V power supply and deliver mind-blowing access times. The chips feature low standby power, sleep mode and support for the popular processors powering today's ultra-high performance devices. ■ Our high speed synchronous and asynchronous product line includes 1-Meg, 2-Meg and 4-Meg devices in a variety of organizations. The pipelined version of our 4-Meg achieves frequencies up to 166 MHz--with faster versions on the way! ■ If you want fast access to fast SRAMs, visit **www. galvantech.com today. Or call 408.566.0688 x 888.**

Galvantech

READER SERVICE 126



GO ANYWHERE. FROM ANYWHERE: LATTICE CHARTS A NEW COURSE IN DIGITAL SIGNAL ROUTING.

When you're blazing new trails, you need the flexibility to change directions whenever and wherever you want. Introducing Lattice's new ispGDX™ family of high pin count, in-system programmable (ISP™) digital crosspoint devices, the first programmable components optimized for digital signal interface and routing applications. The unique ispGDX architecture can route signals from "any pin to any pin" with only a 5 ns delay and multiplex signal paths in real time so multi-port interfaces are a breeze. Best of all, each high drive I/O pin can be independently configured to emulate any interface logic function, so a single ispGDX part can replace a dozen or more octal devices.

Download Free ispGDX Design Software From Our WebSite!

Lattice's ispGDX family offers I/O counts from 80 to 160 I/O pins, in space-saving QFP and BGA packages. Industry standard boundary scan test and in-system programming allow you to reconfigure and test signal paths and interfaces in seconds without removing components from your PCB.

Visit the Lattice web site (**www.latticesemi.com**) and learn more about the ispGDX family. Or give us a call at 1-888-ISP-PLDS and ask for information packet 335.

Lattice® Semiconductor Corporation
The Leader in ISP™ PLDs

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NEW WORKS.

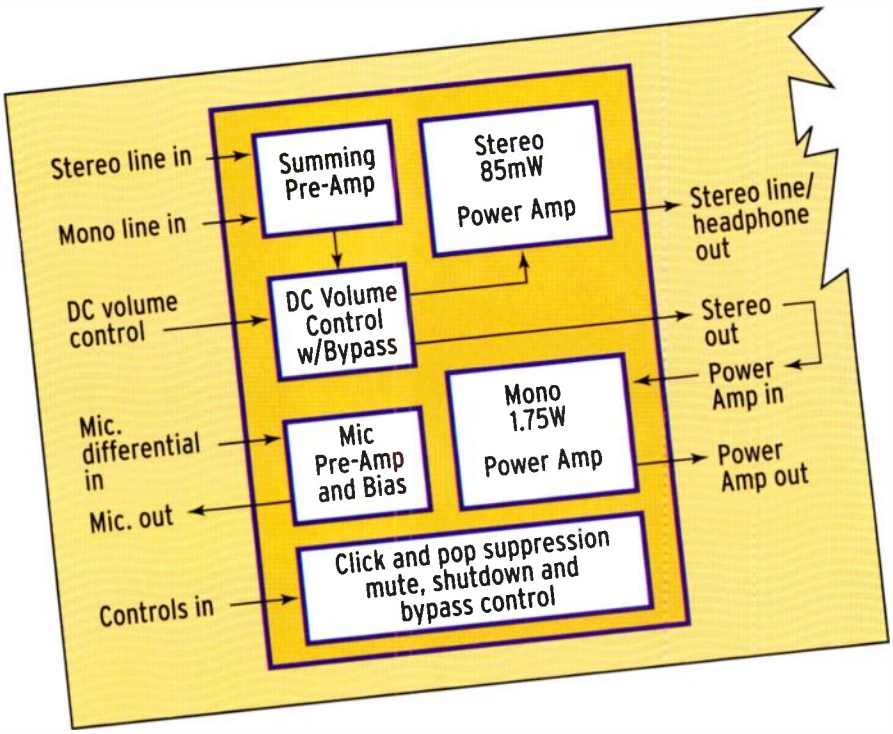
THE ART OF DESIGNING THE FUTURE.

Here are the new products you need to make your next design a work of art. Interface devices that throw the data pipeline wide open. Power switching controllers for the next generation of portables. Advanced A/D converters and PLL frequency synthesizers that keep resetting the industry standard. Sophisticated sensors and monitors for system designs. Op amps, comparators, and audio solutions. All of them designed to give you design options you need to turn your talents loose and create a masterpiece.

Use this special URL — www.national.com/see/newworks — to order eval boards, data sheets, spice models, application notes, and samples for all the products in this catalog.

National Semiconductor

Newest member of the BOOMER Family for desktop PCs.



BOOMER Integrated Audio Solutions for PCs
LM4834

Highly integrated BOOMER solutions simplify your design, minimize components and maximize reliability.

- 1.75 watt mono power amp
- Stereo headphone amp
- DC volume control w/bypass
- Low shutdown current
- Microphone pre-amp and bias supply
- Mono input for system beep
- PC 98 compliant

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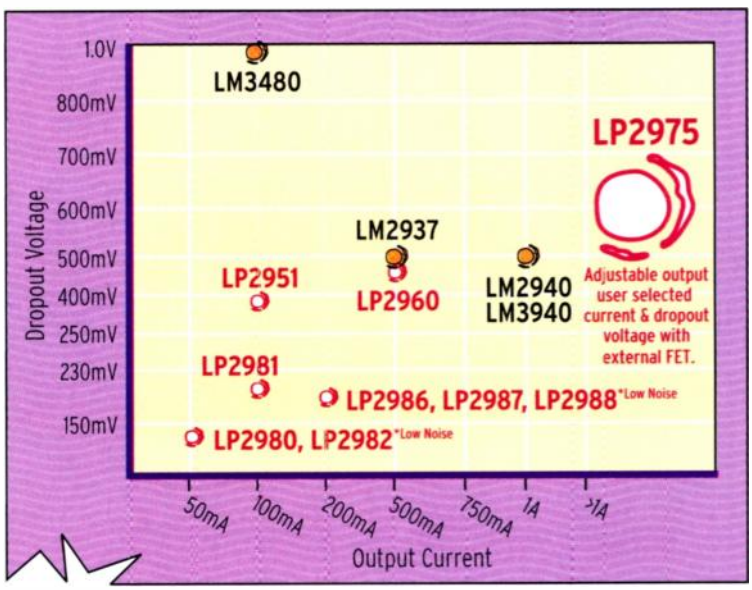
POWER

The power of possibilities: National enhances its growing family of controllers and regulators for desktops and portables.

LOW DROPOUT REGULATORS



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Low Dropout Regulator LM3940

Optimized for 5V to 3.3V conversion.

- Excellent load regulation; 3.3V V_{OUT} regulation with V_{IN} as low as 4.5V
- Guaranteed 1A output current
- Requires only one external component
- Built-in thermal protection
- Short circuit protection

Low Cost 100 mA Low Dropout Regulator LM3480/LM3490

Now available in miniature 3 & 5-lead SOT 23 TinyPak

- Dropout voltage 1.2V (max) at full load over entire temp range
- 5% guaranteed output voltage tolerance over full load and entire temp range
- Input voltage as high as 30V
- 3.3, 5, 12, and 15V solutions

400mA Low Dropout Regulator LM2937

Advanced SOT223 Power package offers industry's smallest footprint.

- Output current exceeds 400mA
- 3% V_{OUT} accuracy
- Wide output capacitor ESR range 0.01Ω to 5Ω
- Internal short circuit and thermal overload protection
- Reverse battery protection
- 60V input transient protection
- Mirror image insertion protection

1A Low Dropout Regulator LM2940

SOT223 Power package breaks the size barrier.

- Dropout voltage 0.5V @ I_{OUT} = 1A (typ), maximum of 1.0V over entire temp range
- ± 5% output tolerance over all conditions
- Reverse battery protection
- Internal short circuit current limit
- Mirror image insertion protection
- P+ product enhancement tested

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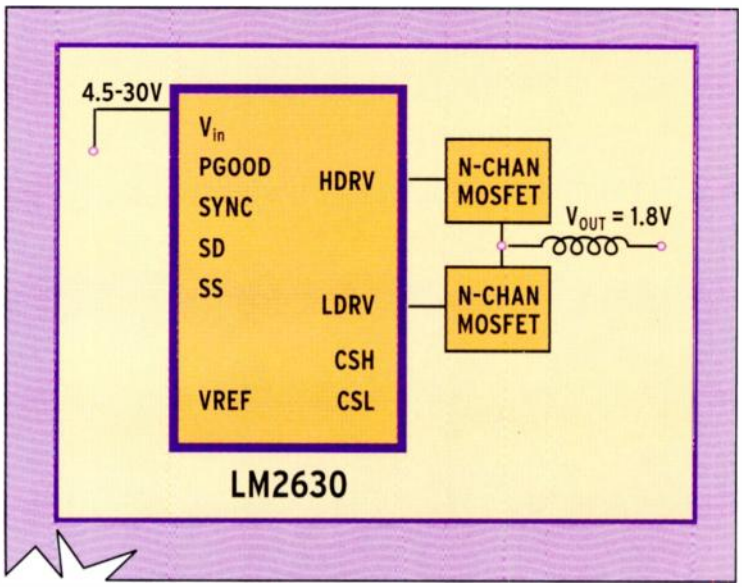
STEP-DOWN SYNCHRONOUS CONTROLLER FOR PORTABLES

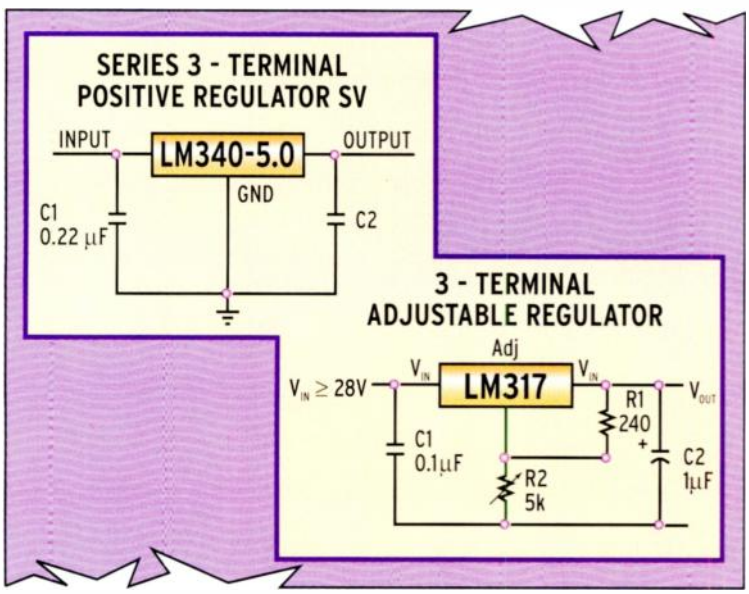


Synchronous Step-Down Switching Controller LM2630

Ideal for generating the required CPU core voltage in notebook power supplies.

- Fast loop response; line regulation of 0.002%/V and load regulation of 0.3%
- Low shutdown current (0.1µA); 92% efficiency at 3A and 80% efficiency at 50µA
- Ultra-thin 20-ld TSSOP package
- Under/over voltage protection, current limiting, thermal shutdown, adjustable frequency

SOT223 HIGH-POWER REGULATORS



Regulator Family LM317, LM337, LM340-5

The world's smallest high-power regulators.

- SOT223 footprint 30% smaller than TO-252 D-Pak
- LM317: adjustable positive 1A regulator
- LM337: adjustable negative 1A regulator
- LM340-5: 5V positive 1A regulator

Reference LM385

The first low-current reference in a SOT-23, it uses half as much board space as an SO package.

- First SOT low-current reference
- 10 µ A min. operating current
- 2% precision
- 1.2V and 2.5V options

A/D CONVERTERS

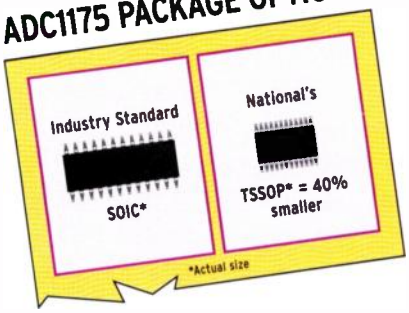
High-performance A/D converters provide high speed high resolution in imaging & communications applications.

8-bit Low Power Video A/D Converter ADC1175

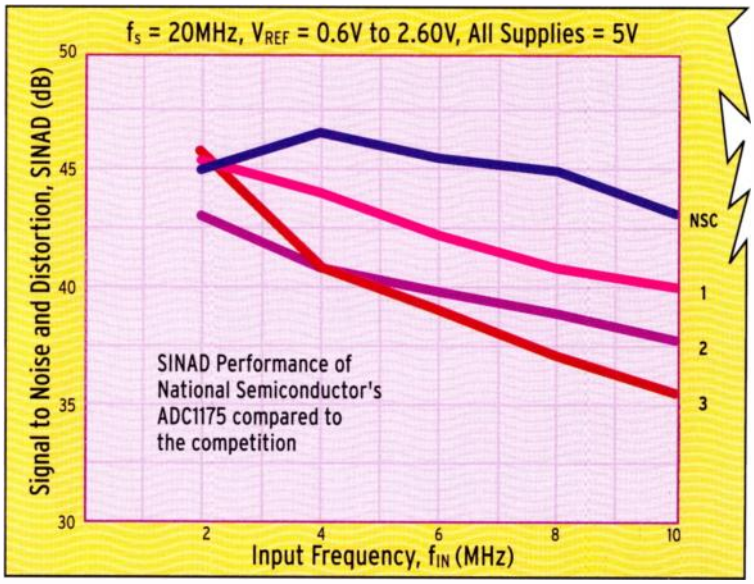
8-bit A/D conversion for low-power video and imaging applications.

- Clock frequency: 20MSPS
- Superior DNL of 0.5LSB
- Low Noise: 42dB SNR @ Nyquist rate
- Low Power: 55mW

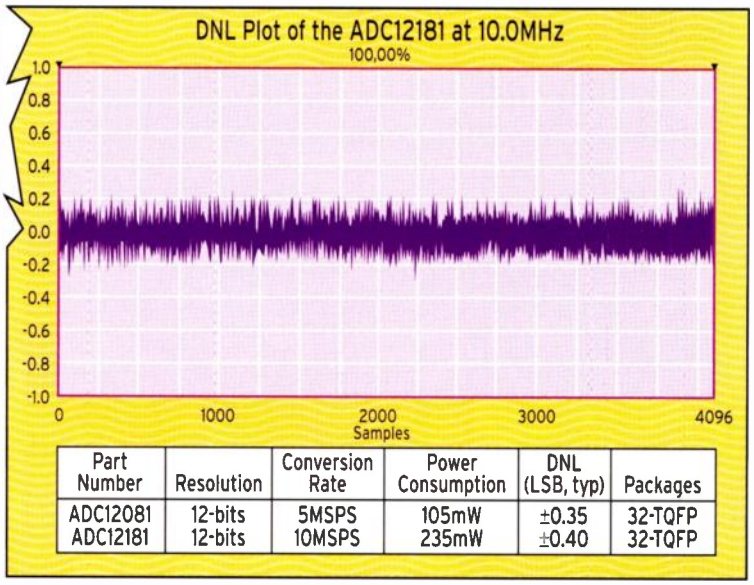
ADC1175 PACKAGE OPTIONS



NATIONAL'S SINAD OUTPERFORMS THE COMPETITION



HIGH-RESOLUTION HIGH-SPEED 12-BIT A/D CONVERTER



Part Number	Resolution	Conversion Rate	Power Consumption	DNL (LSB, typ)	Packages
ADC12081	12-bits	5MSPS	105mW	±0.35	32-TQFP
ADC12181	12-bits	10MSPS	235mW	±0.40	32-TQFP

12-bit High-Resolution A/D Converters ADC12081/12181

- Clock frequency: 5MSPS/ 10MSPS
- Superior DNL of 0.35LSB
- Low Noise: 68dB SNR (f_{IN} = 500kHz)
- Low Power: 105mW (Max, ADC12081)

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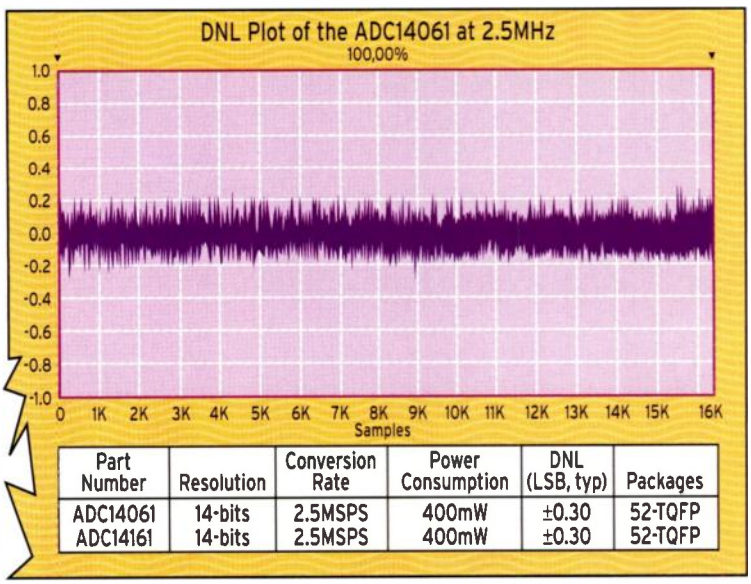
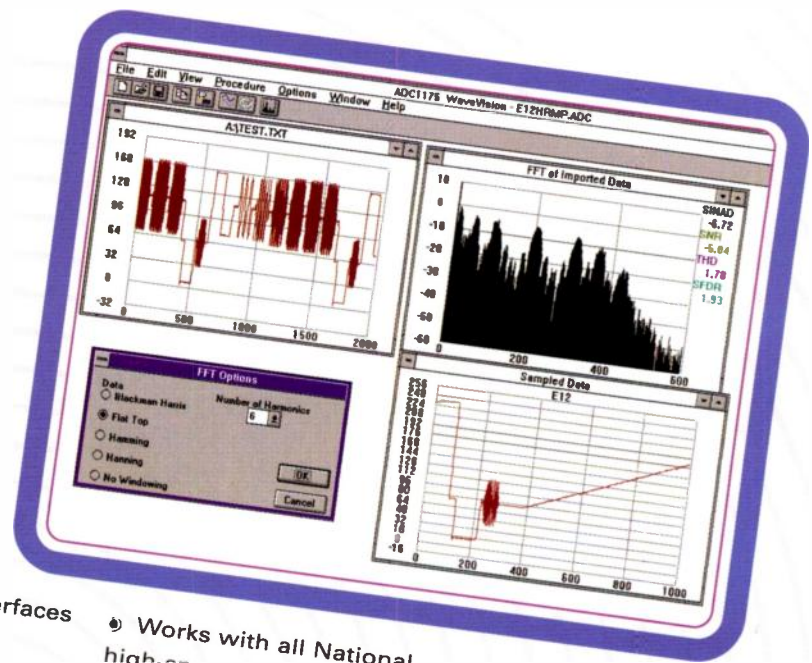
HIGH-RESOLUTION HIGH-SPEED 14-BIT A/D CONVERTER



Part Number	Resolution	Conversion Rate	Power Consumption	DNL (LSB, typ)	Packages
ADC14061	14-bits	2.5MSPS	400mW	±0.30	52-TQFP
ADC14161	14-bits	2.5MSPS	400mW	±0.30	52-TQFP

14-bit High-Resolution A/D Converter ADC14061/14161

- Clock frequency: 2.5MSPS
- Superior DNL of 0.3 LSB (ADC14061)
- Self-calibrating architecture
- Low Noise: 80dB SNR (f_{IN} = 500kHz) (ADC14161)
- Low Power: 390mW



WaveVision™ Design Evaluation System Kit

- Data capture card interfaces to your PC
- Easy-to-use Windows®-based software
- Simplifies system design and performance evaluation
- Works with all National high-speed ADC products
- Available on the web (http://www.nsc.com)

WIRELESS

Pushing the limits of PLL frequency synthesizers: Wireless solutions set new standards for low power and high performance.

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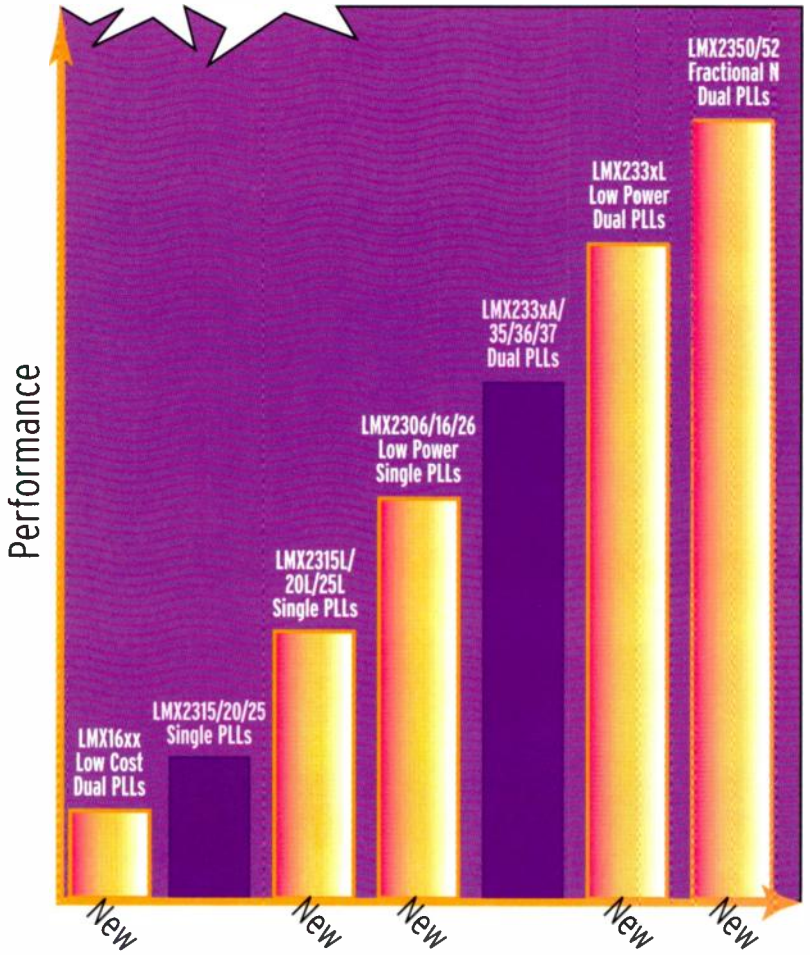
COMPLETE PLL PORTFOLIO



Low Cost Dual PLLs
LMX1600/01/02

Optimized for cost-sensitive applications.

- V_{CC} range of 2.7V to 3.6V
- Low power consumption: I_{CC} = 5.0mA for 1.1GHz/1.1GHz dual
- TSSOP16: smallest package available
- Digital lock detect

Low Power Single PLLs
LMX2315L/20L/25L

Drop-in upgrade for industry-standard LMX2315/20/25.

- 60% less power consumption
- Same low phase noise
- Same high-performance charge pump

Low Power Dual PLLs
LMX2306/16/21/26

Performance up to **3.0GHz.**

- I_{CC} = 2.3mA @ 1GHz
- V_{CC} range of 2.3V to 5.5V
- Ultra-low phase noise floor (-167dBc/Hz)
- TSSOP16: smallest package available
- Selectable Fastlock™ Mode

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NEW PLL SELECTION GUIDE

Part Number	RF Input (Main & Aux PLLs)	Active I_{CC} (typ @ 3V)	V_{CC} Range	Package*
Single PLLs				
LMX2306	550MHz	1.7mA	2.3 to 5.5V	TSSOP16
LMX2316	1.2GHz	2.5mA	2.3 to 5.5V	TSSOP16
LMX2326	3.0GHz	4.0mA	2.3 to 5.5V	TSSOP16
LMX2315L	1.2GHz	3.2mA	2.7 to 5.5V	TSSOP20
LMX2320L	2.0GHz	2.4mA	2.7 to 5.5V	TSSOP20
LMX2325L	2.5GHz	4.0mA	2.7 to 5.5V	TSSOP20
Dual PLLs				
LMX2330L	2.5GHz & 510MHz	5.0mA	2.7 to 5.5V	TSSOP20
LMX2331L	2.0GHz & 510MHz	4.0mA	2.7 to 5.5V	TSSOP20
LMX2332L	1.2GHz & 510MHz	3.0mA	2.7 to 5.5V	TSSOP20
LMX2335L	1.1GHz & 1.1GHz	4.0mA	2.7 to 5.5V	TSSOP16/SO16
LMX2336L	2.0GHz & 1.1GHz	5.0mA	2.7 to 5.5V	TSSOP20
LMX1600	2.0GHz & 500MHz	5.0mA	2.7 to 3.6V	TSSOP16
LMX1601	1.1GHz & 500MHz	4.0mA	2.7 to 3.6V	TSSOP16
LMX1602	1.1GHz & 1.1GHz	5.0mA	2.7 to 3.6V	TSSOP16
Dual Fractional N PLLs				
LMX2350	2.5GHz & 550MHz	7.0mA	2.7 to 5.5V	TSSOP24
LMX2352	1.2GHz & 550MHz	5.5mA	2.7 to 5.5V	TSSOP24

*Chip Scale Packaging (CSP) available soon.

Low Power Dual PLLs LMX2330L/31L/ 32L/35L/36L

National's newest PLL — an upgrade to our industry standard with 60% lower power consumption than before.

- Drop in upgrade for industry standard LMX2330A/31A/32A/35/36
- Power consumption reduced by 60%
- Same ultra-low phase noise floor (-169dBc/Hz)
- Same high performance charge pump
- Selectable Fastlock™ Mode

Fractional Dual PLLs LMX2350/52

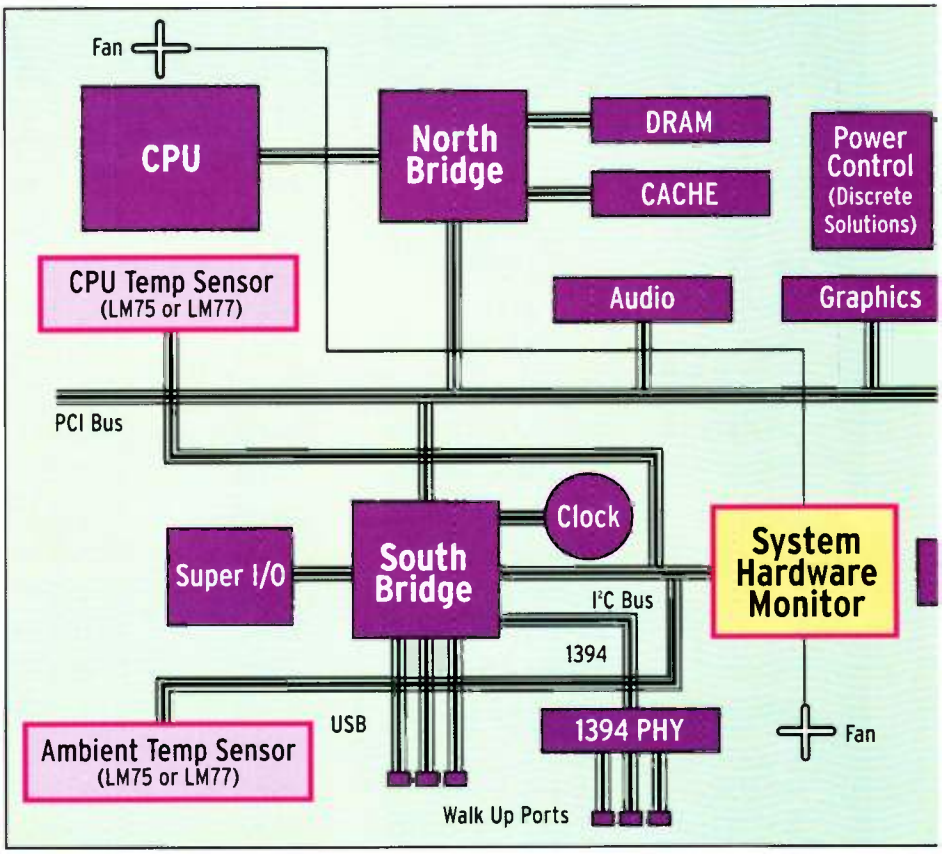
Up to modulo 16 fractional N divider with no fractional current compensation.

- Up to 2.5GHz performance
- Output voltage doubler
- V_{CC} range of 2.7V to 5.5V
- Low current consumption: I_{CC} = 7.0mA and 5.5mA
- Selectable Fastlock™ Mode

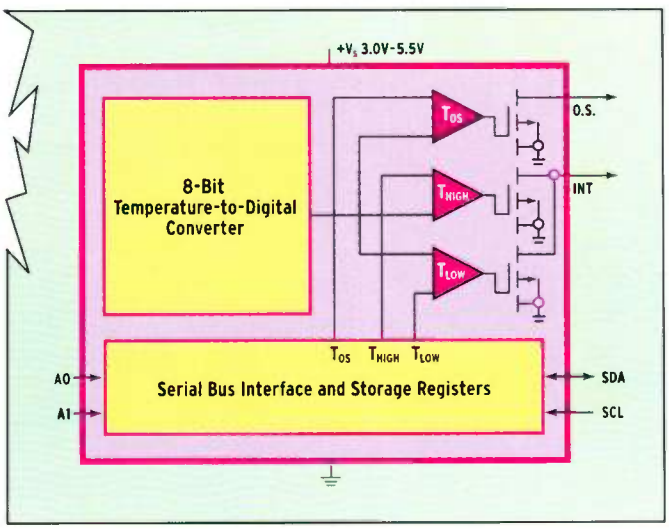
SENSORS/MONITORS

Hardware monitoring and temperature sensor solutions enhance system reliability and performance.

SYSTEM MANAGEMENT SOLUTION



DIGITAL TEMPERATURE SENSOR



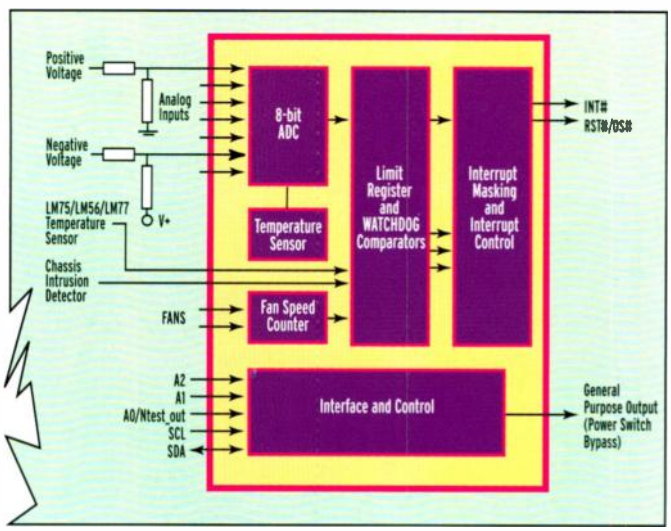
Digital Temperature Sensor LM77

The next generation of the industry standard LM75.

- ACPI enabled thermal response
  - Thermal window comparator with interrupt
  - System 911 alert over-temp shutdown
- User programmable temp thresholds and hysterisis
- 2-Wire serial interface (I^2C)

LAN

SYSTEM HARDWARE MONITOR



System Hardware Monitor LM80

Records key system parameters to enable timely preventive maintenance and system management.

- Temperature sensor accuracy to ±3.0°C
- 7 Voltage monitors/analog inputs
- 2 fan speed monitors (±10%)
- 8-Bit ΔΣ A/D converter
- WATCHDOG™ comparison of system hardware monitor inputs
- 2-Wire serial bus (I^2C) interface

OP AMPS/COMPARATO

Power to the portables: Op Amps and Comparators meet your needs for price, packaging and performance.

Op Amp Family LMV321/324/358 and LMV331/339/393

The LMV321 is the world's smallest op amp.

- Single, dual & quad op amps and comparators
- 2.7V-5V single supply
- Rail-to-rail output
- SC70, SOT-23, MSOP, TSSOP & SOIC packages

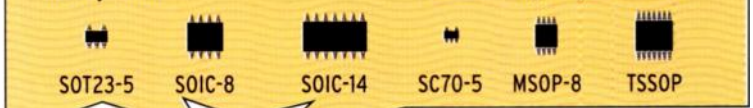
Very High Speed, Low Cost Quad Op Amp CLC5654

- 450MHz small signal bandwidth
- 2000V/μ s slew rate
- -71dBc distortion
- 0.03%, 0.03 deg diff gain, phase
- 70mA output current
- 12 ns settling to 0.1%

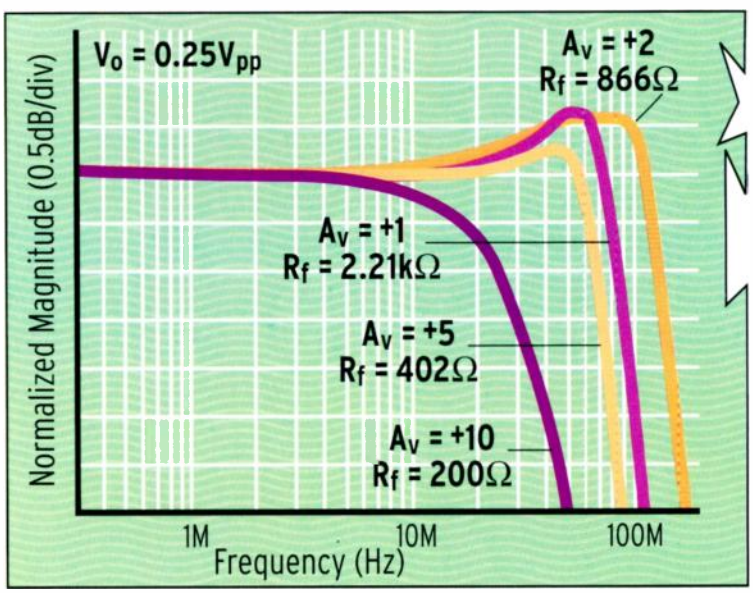
NEW TINY OP AMPS/COMPARATORS

Part #	MHz	Supply Voltage	Package Sizes
LMV321* Single Op Amp	1MHz	2.7 - 5.5V	SOT23-5, SC70-5
LMV358* Dual Op Amp	1MHz	2.7 - 5.5V	SOIC-8, MSOP-8
LMV324* Quad Op Amp	1MHz	2.7 - 5.5V	SOIC-14, TSSOP
LMV331* Single Comparator	1MHz	2.7 - 5.5V	SC70-5, SOT23-5
LMV393* Dual Comparator	1MHz	2.7 - 5.5V	MSOP-8, SOIC-8
LMV339* Quad Comparator	1MHz	2.7 - 5.5V	TSSOP, SOIC-14

Package (Actual Size) *Industrial Temp Range (-40 to 85 C)



NON-INVERTING FREQUENCY RESPONSE



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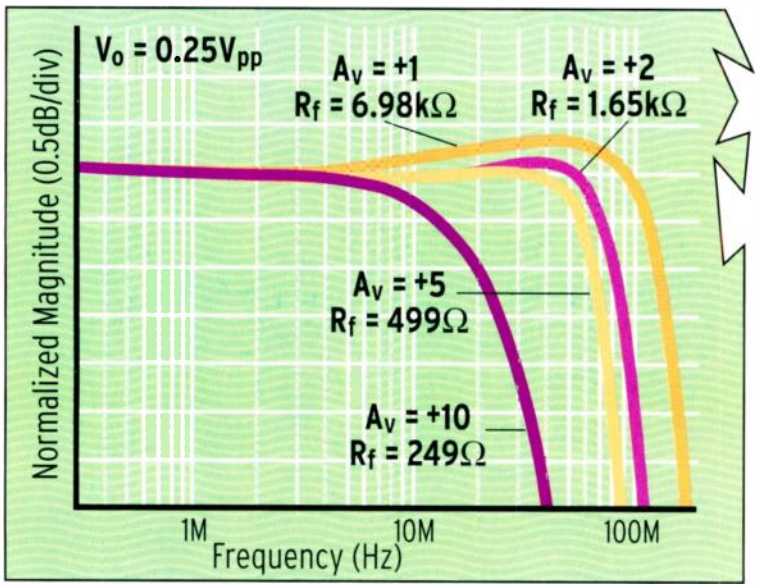
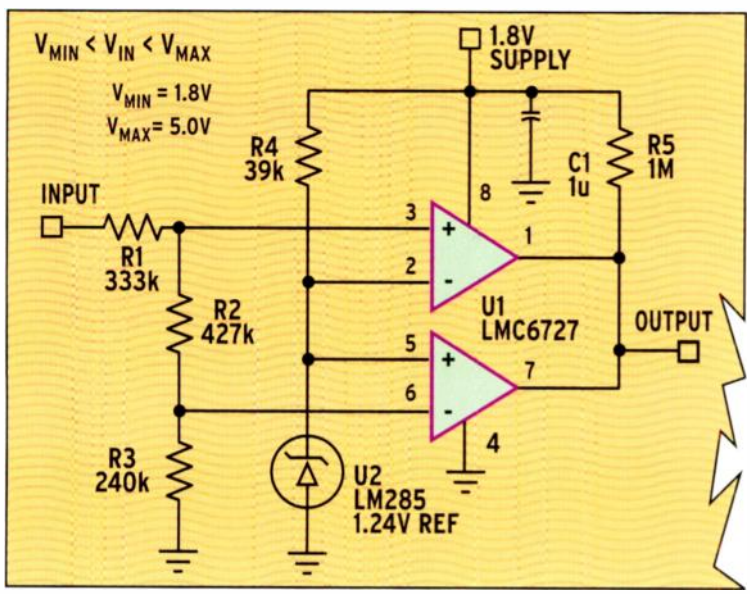
NON-INVERTING FREQUENCY RESPONSE



Low Power, Low Cost Quad Op Amp CLC5644

- 170MHz small signal bandwidth
- 2.5mA/channel supply current
- 1000V/μ s slew rate
- -72dBc distortion
- 0.04%, 0.07 deg diff gain, phase
- 70mA output current
- 16 ns settling to 0.1%

WINDOW COMPARATOR EXAMPLE



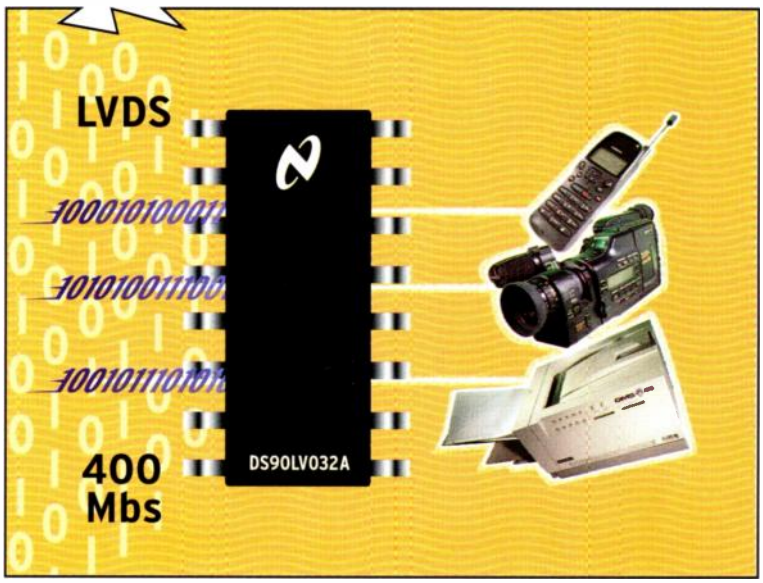
Comparators LMC6717/27

- Ultra low power: 1 μ A/comparator
- Guaranteed 1.8V and 5V performance
- Rail-to-rail input common mode range
- Push-Pull (LMC6717) or open drain (LMC6727) outputs
- High output current drive: (@Vs = 5V): 45mA
- SO-8 and MSOP-8 packaging

INTERFACE

More megabits for your milliwatts: Low-power LVDS solutions move at the speed of data.

FAST LVDS DRIVERS AND RECEIVERS



LVDS 3V Quad Driver/ Receiver
DS90LV031A/32A

LVDS technology makes this the world's fastest quad driver/receiver, without any trade-offs in power consumption.

- 400 Mbs operation
- 2.0 ns typ prop delay (driver)/3.3 ns (receiver)
- 400 ps typ channel-to-channel skew/1200 ps typ chip-to-chip skew
- Consumes 13mW @ 3.3V (driver)/40mW @ 3.3V (receiver)

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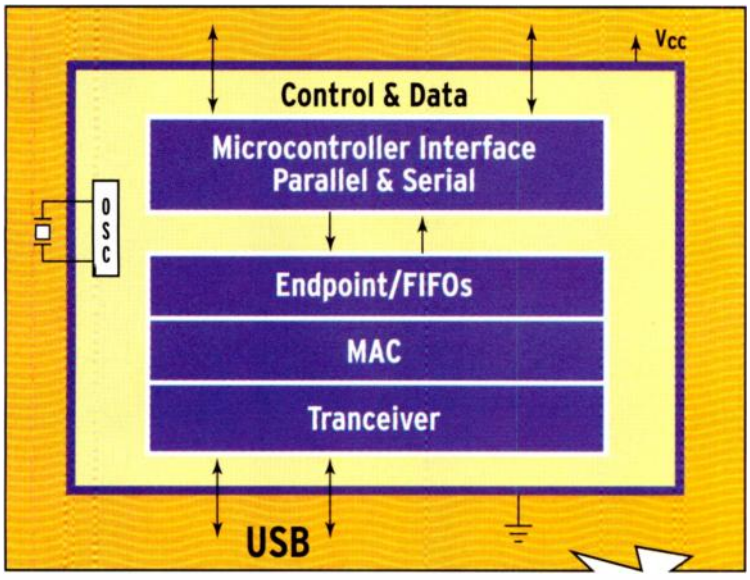
USB NODE CONTROLLER



Microcontroller Independent USB Node USBN9602

Contains all the functions required to create USB Specification 1.0-compliant node products like 56K modems, high-end joy sticks, bar code scanners and digital cameras.

- Microcontroller independent
- Seven FIFO endpoints support all four USB modes — one bi-directional for mandatory control EP0; six for uni-directional support of USB interrupts, and bulk and isochronous data transfers
- 8-bit parallel interface supports addresses/databases in multiplexed and non-multiplexed systems
- Programmable interrupt scheme allows device configuration for different interrupt signal requirements

National Semiconductor

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570676-001

New Self-Extinguishing Electrolyte Should Lead Non-Flammable Lithium-Ion Battery

vantages like greater energy orage and lighter weight are driving lithium-ion batteries into laptops, cellular phones, and other portable electronics. Despite their benefits, however, safety is a major concern for both primary and rechargeable lithium-metal and lithium-ion batteries. Researchers at SRI International's Electrochemical nd Polymer Technology Center, Menlo Park, Calif., claim to have cked this safety problem by coming with a non-flammable, self-extinishing electrolyte for both types of nium cells.

The alarm sounded in 1995, when Sony's rechargeable lithium-ion manufacturing plant in Japan caught fire. Concern heightened last year when several fires were reported by consumers, and a major fire occurred at a Matsushita plant in Japan.

The problem is the use of a flammable electrolyte in the lithium-ion cells. Designers have incorporated safety measures into lithium-ion packs by mploying techniques such as voltage ntrol of the charge and discharge ndition. These include self-discharge, shut-down separators, and fety vents. Yet these precautions ere designed to prevent thermal naway, and therefore do not treat e inherent problem of flammability.

nosphorous Base

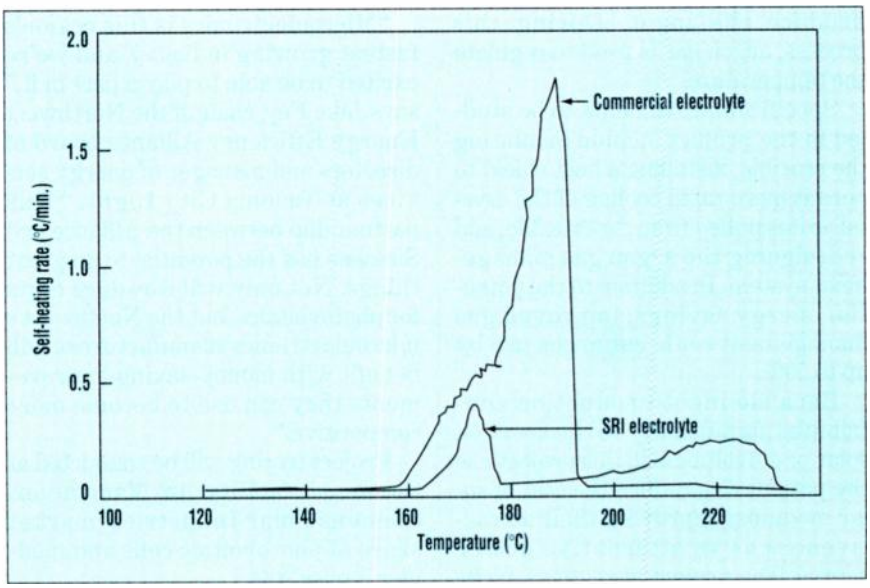
According to SRI, the researchers ve developed a five-component electolyte comprising phosphorous, pyrourbonate, and lithium salt. "It is the hosphorous base that provides nonflammability," says Subash Narang, director of SRI's Energy Technology Laboratory. "SRI's new non-flammable electrolyte eliminates the safety concerns by replacing the hazardous, flammable electrolyte, without sacrificing power or energy performance," ates Narang.

Other properties of SRI's non-flammable electrolyte include high dielectic constant (greater than 13), low scosity, good ionic conductivity, and od chemical stability. As a result, electrolyte can dissolve a range of lithium salts in acceptable concentration to give a usable electrolyte conductivity. Furthermore, it requires no special handling procedures, and is environmentally-friendly, with no known toxic hazards. Also, its operating temperature range is –20 to 60°C, while its boiling point temperature is greater than 200°C.

According to SRI, the new non-flammable electrolyte has been tested with a wide range of lithium battery chemistries. In addition, the material has been subjected to accelerated-rate calorimeter testing to test the flammability and thermal hazards of the material *(see figure)*. To demonstrate the viability of the new electrolyte, SRI has constructed a 1.3-Ahr lithium-ion cell measuring 18 by 65 cm, the standard size found in laptops. SRI claims it is functionally equivalent to the commercially available, lithium-ion cells.

For more information, call Subhash Narang at (650) 326-6200, or e-mail him at subash_narang@qm.sri.com.

Ashok Bindra



The accelerated-rate calorimetric test indicates that the new electrolyte material, developed by SRI International, exhibits a maximum self-heating rate of only 0.38°C/min. at 178°C. In contrast, the commercial electrolyte tested as part of the program has a much larger exotherm, with a maximum self-heating rate of 1.76°C/min. at 191°C.

Joint Conservation Project To Demonstrate More Efficient Silicon Production Techniques

A cooperative project underway in the state of Washington is intended to cut both energy usage and production time in the manufacture of silicon crystals for ICs and photovoltaic cells. The $2-million program is being funded by Siemens Solar Industries, Vancouver, Wash., and the Northwest Energy Efficiency Alliance, Tacoma, Wash.

The joint effort will investigate technical improvements that will reduce the amount of electricity used in the energy-intensive process of growing single-crystal silicon ingots, These are cylindrical bars of silicon sliced into round wafers. Siemens estimates that the improvements could eventually yield energy savings of 40% to 50%, and cut the time necessary to produce the ingots by 15%.

To make the ingots, raw polysilicon

is placed in a crucible and melted in a super-heated furnace. A small piece of pure silicon lowered into the spinning crucible touches the liquid silicon, and then slowly draws out the material to produce the ingot. During this process, argon gas is used to regulate the temperature.

Specific improvements to be studied in the project include insulating the crucible, installing a heat shield to permit more rapid cooling of the crystal as it is pulled from the crucible, and redesigning the argon gas management system. In addition to the potential energy savings, improved gas management could cut argon use by up to 50%.

Because ingot production contributes significantly to the cost of a solar photovoltaic cell, this project has the potential to reduce the cost of solar modules, improving their attractiveness as an alternative power source. The project also offers exciting promise for semiconductor manufacturing because the same equipment is used to produce ingots for that industry as well. If these improvements are successfully transferred to the semiconductor industry, the energy saved could serve a community of 50,000 people.

"Microelectronics is this region's fastest growing industry, and we're excited to be able to play a part in it," says Jake Fey, chair of the Northwest Energy Efficiency Alliance board of directors and manager of energy services at Tacoma City Light. "This partnership between the Alliance and Siemens has the potential to do great things. Not only will it reduce costs for photovoltaics, but the Northwest's microelectronics manufacturers will benefit with money-saving improvements they can use to become more competitive."

Project testing will be conducted at Siemens' facility in Vancouver. Siemens Solar Industries' market share of photovoltaic cells and modules is over 20%.

Officially formed in October 1996, the Northwest Energy Efficiency Alliance is a consortium of Northwest electric utilities, state and local governments, public interest groups, and private concerns dedicated to increasing the efficiency of energy use in the region. The alliance seeks to bring about significant and lasting changes in markets for energy-efficient technologies and practices, to improve the region's efficient use of energy, and reduce costs to consumers and the electric system.

The Alliance also hopes to leverage and provide for non-energy benefits. Collaboration both inside and outside the region is a vital element of the Alliance,whose members look to market incentives and transformation ventures as a means to save considerable energy at potentially low long-term costs.

For further information, contact the Northwest Energy Efficiency Alliance at 522 S.W. Fifth Ave., Suite 410, Portland, OR 97204; (800) 411-0834, (503) 827-8416, fax (503) 827-8437, e-mail: *nweea@nwalliance.org*; *www.nwalliance.org*.

Lee Goldberg

Proposed Internet Standards May Improve Virtual Private Networking Capabilities

The submission of two draft documents to the Internet Engineering Task Force (IETF) may signal progress in the development of standards for quality-of-service control, security, and other virtual network services over IP-based networks. According to the authors at Northern Telecom's (Nortel's) Enterprise Data Networks group, the proposals are an attempt to improve the reliability and security of virtual-private-network (VPN) traffic over public networks.

In the past, some customers may have been deterred from using the Internet (or an Internet service provider) for private networking due to a lack of security and/or inadequate traffic management. Both features are becoming increasingly important as businesses become more dependent on the Internet for operational communication and electronic commerce. As the size and sophistication of Internet-based applications grows, providers, administrators, and users are faced with several important problems.

First, the scalability of networks is growing almost daily, thanks to the rapid growth in bandwidth demand, and the distances between users. Nortel has found that as the size of a WAN network grows, traditional point-to-point and non-broadcast multiple-access (NBMA) network topologies or network models lose their performance.

Second, administrators and users increasingly need to segregate traffic according to class of service (CoS). While quite adequate for simple file transfers, a single "best-effort" service cannot perform well when handling audio or video feeds. Also, providers are beginning to demand ways to differentiate the quality of the service offered to their clients based on multiple policies.

Third, enterprise networks are now often using WANs to carry mission-critical traffic that cannot tolerate loss of service. There also is a growing need for simplified network administration to handle the permanent virtual circuit (PVC) provisioning of large NBMA topologies until switch virtual circuit (SVC) deployment becomes more commonly used. Finally, proper segregation of traffic is now a must-have function.

The first draft document from Nortel reports on how the company's layer-three switching technology can provide a full suite of VPN capabilities and performance enhancements. The second document outlines recommended guidelines to increase control and management of IP networks that rely on tunneling capabilities.

Comprehensive View of VNS

The document, delivered to the Multiprotocol Label Switching (MPLS) Committee, presents a comprehensive view of Virtual Network Switching (VNS), Nortel's label-switching technology. The introduction to the IETF proposal explains, "VNS is a multiprotocol switching architecture that provides CoS-sensitive packet switching; reduces the complexity of operating protocols like PPP and frame relay; provides logical networks and traffic segregation for VPNs, security, and traffic engineering; enables efficient WAN broadcast

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ing and multicasting; and reduces address space requirements. VNS reduces the number of routing hops over the WAN by switching packets based on labels."

The introduction continues, "VNS makes a network of point-to-point links (trunks) appear to be a single LAN (broadcast, multiple access) media. The network used by a particular instance of VNS is called a Logical Network (LN). A LAN packet is encapsulated in a VNS header as it enters the LN, and the label in the header is used to switch the packet across the LN. The encapsulation header contains the identifier of the last node (or egress node) that processes the packet as it traverses the LN. It is the first node (or ingress node) that decides to which egress node the packet is sent. All nodes between the ingress and egress nodes (known as tandem nodes) decide independently the best packet forwarding route to the egress node identified in the packet."

According to Nortel, it improves performance by reducing latency, while providing a way for service providers or enterprises to offer or deploy economic IP transport solutions across WAN backbones.

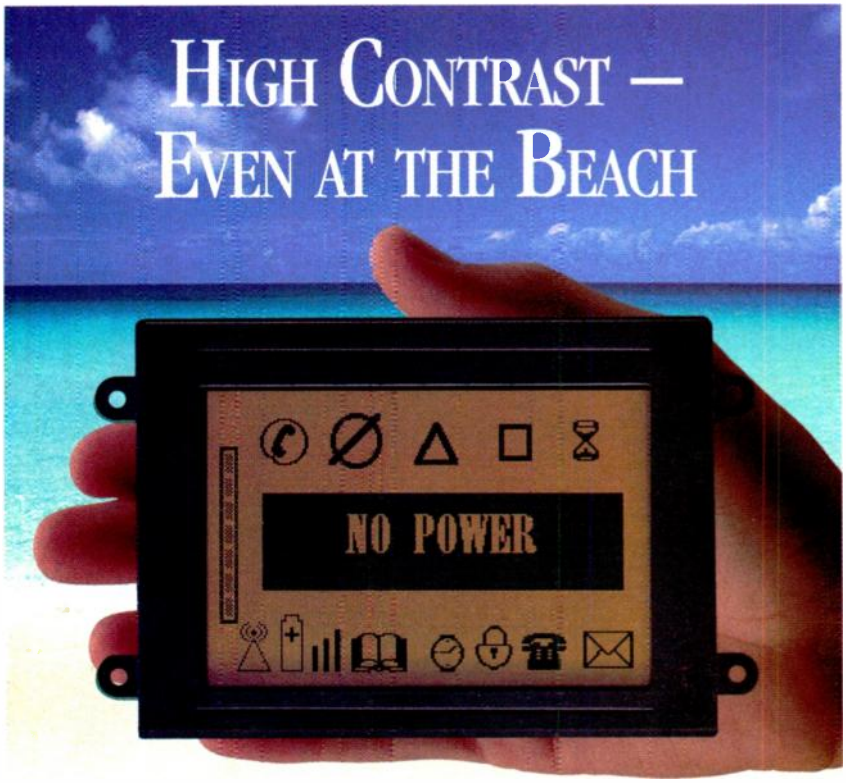
The second draft document describes a method for the distribution of VPN address information across a public network. It provides a blueprint for the automatic configuration of VPNs between switches and routers to streamline IP tunneling technology. It is meant to simplify and standardize the implementation and configuration of VPN services, using current IP tunneling technology, to avoid the problems experienced by carriers today. The proposed VMMT is a protocol that supports the dynamic distribution of VPN information throughout a shared network, and the automatic formation of multipoint-to-multipoint tunnels between VPN routers.

The introduction of the proposal explains that "each VPN peer (router) belonging to a VPN is identified by a 32-bit VPN identifier (VPNID) that is unique in the shared network, but common to all routers belonging to the VPN." To manage and distribute the address information within the VPN, Nortel's scheme lets each VPN peer have "one shared IP address assigned to it and multiple private IP addresses," says the proposal.

It continues, "The shared IP address is used as the source address in all tunnel IP headers. There is also, optionally, a shared IP multicast group address that is used to send VPN multicast or broadcast packets to VPN peers. It also has one private address for each interface into the private network, and one for the interface into the shared network. The private IP address for the interface into the shared network will have the same IP subnet value as all VPN peers." A full text of the draft document on virtual private networking submitted to the IETF can be viewed at: *www.ietf.org/*.

For more information, contact Nortel at 1-800-4-NORTEL, or visit their web site at www.nortel.com.

Lee Goldberg



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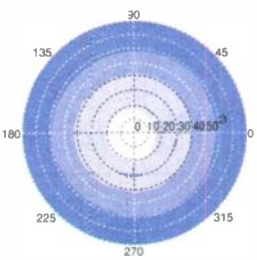

This contrast ratio polar representation illustrates KENT's 360 degree viewing cone.

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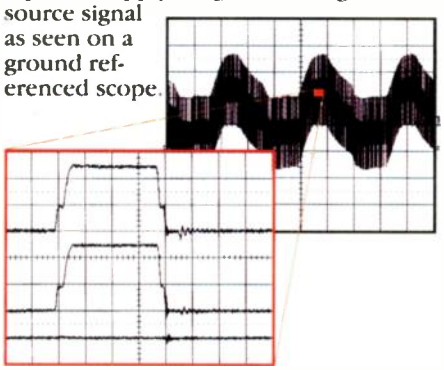
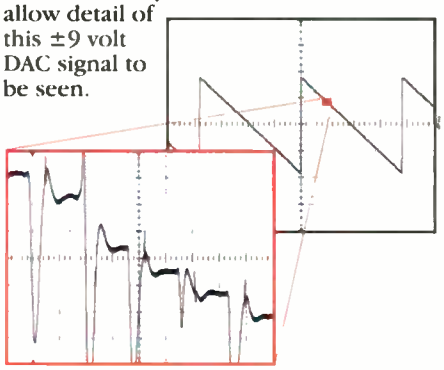
CONVENTIONAL
A power supply's highside FET gate to source signal as seen on a ground referenced scope.



DIFFERENTIAL
The 1855 rejects the line voltage and high dv/dt signal, cleanly displaying the upper and lower gate drive signals.

Preamble's 1800 Differential Amplifier Series low noise, wide common mode range and Precision Offset Generator allow minute portions of very large signals to be examined with 5½ digit resolution.
The generator acts as a precision position control and extends your scope position range to over ±150,000 divisions; the industry's tallest display!

CONVENTIONAL
A scope lacks sufficient position range and lacks the ability to recover from overdrive to allow detail of this ±9 volt DAC signal to be seen.



DIFFERENTIAL
The 1800 Series allow the individual DAC steps to be examined at any point on the wave-form and measured to 5½ digit resolution.

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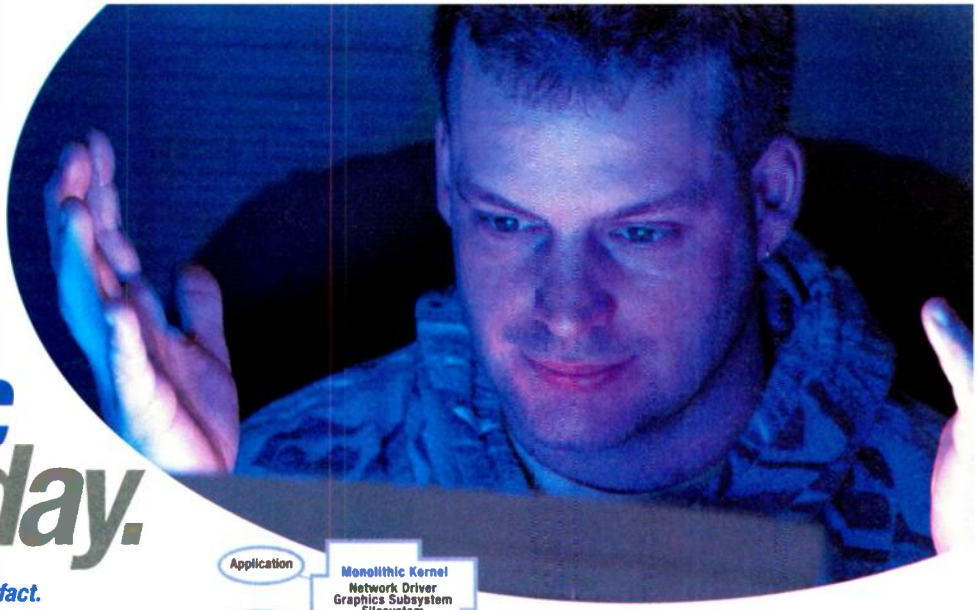
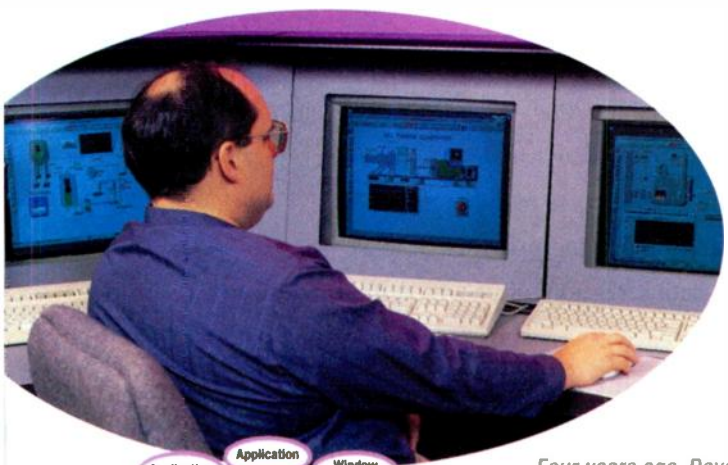
READER SERVICE 169

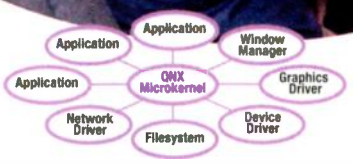
Joe reboots his PC every day.

That's a fact.



Conventional OS Architecture
The monolithic OS on Joe's machine clumps all OS components into a single address space. One subtle programming error in just one driver, and ***whoomp!****, Joe has to reboot – again.*





QNX® Microkernel Architecture
The QNX OS on Dave's machine runs ***every*** *OS component in its own MMU-protected address space. So if a driver – or virtually anything else – fails, the rest of the system stays up.*

Dave hasn't since 1994.

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For a handy 12-point checklist on OS reliability, download Dave's paper, Which OS for PC-based Control?, *at www.omnx.com/productinfo/technical_papers.htm.*

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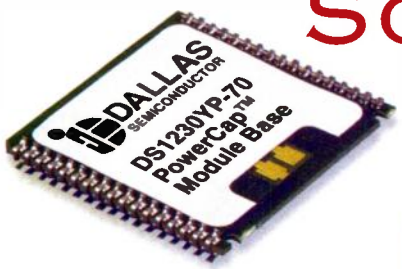
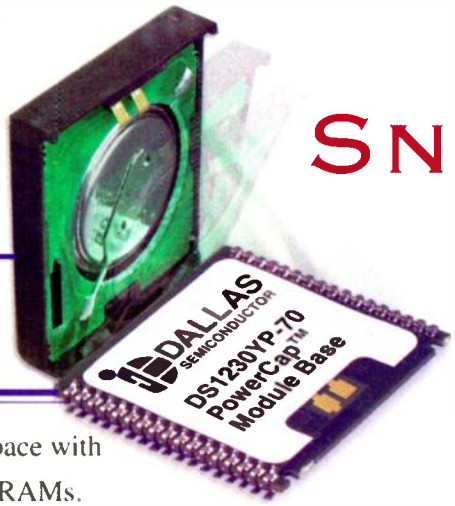
SOLDER.



SNAP.



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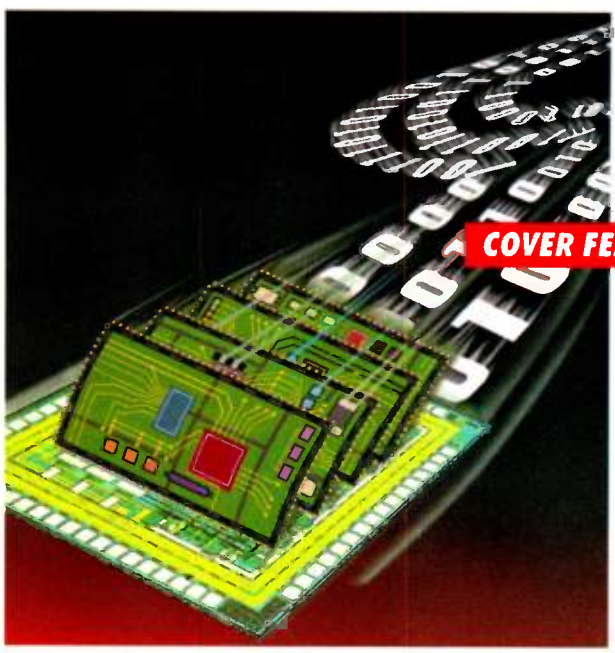


COVER FEATURE

Whether you're linking boards via a backplane or subsystems via cables, your design will need some sort of bus scheme. Intrasystem buses offer advantages over point-to-point solutions by allowing multiple transmitters and receivers on the same interconnect. This reduces the amount of interconnect required, along with the cost of associated hardware. For example, a four-port switch requires five point-to-point connections (including the switch node), but only a single bus. The higher the number of devices, the more attractive a bus becomes.

When the bus links your own internal hardware, you can avoid the protocol overhead of open standard interconnects like VME, PCI, or Fibre Channel. Today's typical bus solutions range from TTL, with bus speeds of just 30 MHz (on a heavily loaded bus), to ECL, which achieves 150- to 300-MHz in a typical multipoint application. For its part, ECL has been the only viable technology for higher bandwidths. However, it's expensive, consumes large amounts of power, and allows only low levels of integration.

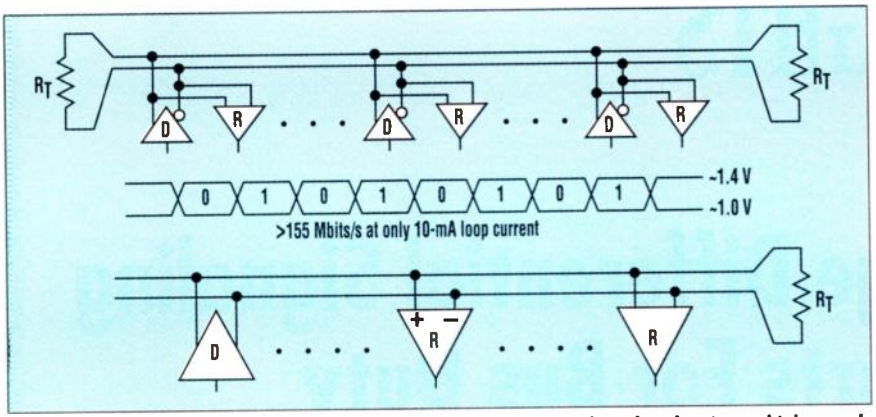
Alternatives such as Low-Voltage Differential Signaling (LVDS) offer an attractive speed/power/cost mix. But LVDS technology has been available only as a point-to-point solution. LVDS is an electrical standard for communicating high-speed digital data over distances of less than 10 m, characterized by a very-low (350 mV) differential swing, low power consumption, and low cost. As an established standard in the ANSI/TIA/EIA 644 specification, the technology is typically used for point-to-point applications such as linking flat-panel displays to computers.

To address bus applications, National Semiconductor has taken the core LVDS technology and expanded it for bus applications. Bus LVDS, the resulting technology, solves the major problems associated with alternative single-ended solutions based on TTL and GTL. It consumes less power, enables hot-insertable boards, operates on a passive backplane that requires only two termination resistors, and is far less susceptible to signal reflections.

Because Bus LVDS is a CMOS technology, it lends itself to inexpensive, high-integration solutions. In fact, complex chips can use Bus LVDS for high-speed interchip communications. Additional Bus LVDS advantages include low EMI, low susceptibility to common-node noise, and a reduction in bus width for some applications.

Two Architecture Choices

While conventional LVDS is a point-to-point technology, Bus LVDS extends to enable full bus interactions. It supports both multipoint and multidrop architectures *(Fig. 1)*. Multipoint buses allow multiple drivers on the same bus, and are typically used in chassis backplanes, LAN applications, central-office switches, and stackable hubs. Multidrop buses have one driver and multiple receivers. And there's typically only one termination. Good examples of multidrop buses are ADSL systems or video-on demand systems, where you're receiving large bandwidth data into a rack, and then distributing it across the rack to multi-



1. The S92LV1021 serializer transforms a 10-bit, parallel CMOS/TTL data bus into a high-speed, LVDS serial data stream. The complementary DS92LV1210 deserializer transforms the LVDS serial stream back into 10-bit data and recovers the embedded clock.

ple network terminator cards.

For multipoint buses, the first-generation Bus LVDS product, is National's DS92LV090 chip *(Fig. 2)*. The device implements a 9-bit bus that provides signaling rates greater than 200 Mbit/s. The device operates from a 3.3-V supply, and includes a delay-locked loop that keeps part-to-part skew below ±200 ps. Bus load is light, typically only 5 pF per LVDS load.

Other members of National's Bus LVDS family include an LVDS serializer for equipment such as network switches that need fast point-to-point and multidrop connections. The S92LV1021 transforms a 10-bit parallel CMOS/TTL data bus (1 data byte plus 2 control bits) into a high-speed LVDS serial data stream *(Fig. 3)*. The complementary DS92LV1210 deserializer transforms the LVDS serial stream back into 10-bit data and recovers the embedded clock *(Fig. 3, again)*. When operating with a 40-MHz input clock, the devices provide a serial LVDS bandwidth of 400 Mbits/s over a single twisted pair or differential pc-board traces.

By handling bandwidth requirements up to about 500 Mbits/s in a backplane, the first-generation Bus LVDS products address the key performance area that is inaccessible to single-ended technologies. In addition, Bus LVDS interface devices can be used in parallel to increase overall throughput. In a six-node stack of 100Base-T units, for example, several 100-Mbit/s Bus LVDS channels can be combined over low-cost SCSI-type interface cables to deliver throughputs as high as 2.4 Gbits/s.

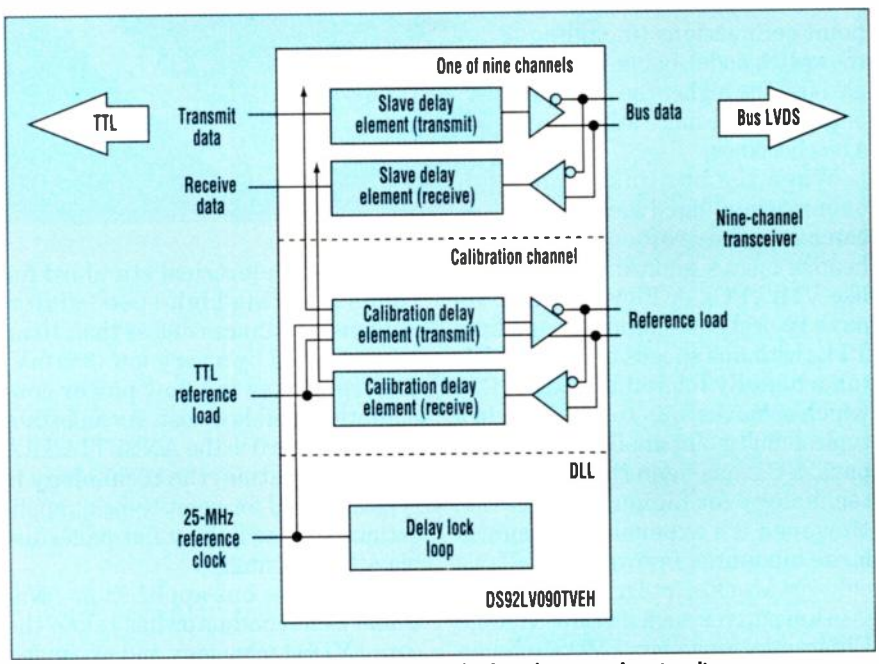
Most of the advantages of Bus LVDS are inherent in industry-standard LVDS technology, which relies on a differential data-transmission scheme with a small voltage swing. Differential transmission uses two wires with opposite voltage swings instead of the one wire used in single-ended technologies such as BTL and TTL. The differential signals minimize susceptibility to external noise because the noise couples onto both wires and is thus rejected by the receivers. The receivers respond only to differential voltages, which represent data signals. The same characteristics make Bus LVDS receivers virtually immune from the effects of common-mode signal reflections.

Because LVDS reduces concerns about noise, the technology can use lower signal-voltage swings. This advantage is crucial, because it's impossible to raise data rates and lower power consumption without using low-voltage swings. Specifically, LVDS uses a differential voltage swing of only 300 mV (typical), which is less than one-half the voltage swing of PECL and 10 times lower than traditional TTL/CMOS levels. Furthermore, the CMOS current-mode driver design used in LVDS greatly reduces the generation of noise.

Multipoint Bus LVDS

Dealing with propagation delays between the chips on a bus can be difficult, especially when driving hundreds of Mbits/s across it. The delays can vary by process technology or temperature. Uncertainties can add up quickly. Propagation delays of the bus transceivers and the backplane itself could result in as much as 10 ns of uncertainty about where the signal is going to be at any point in time. To account for that, systems designers have to degrade the systems' timing budget.

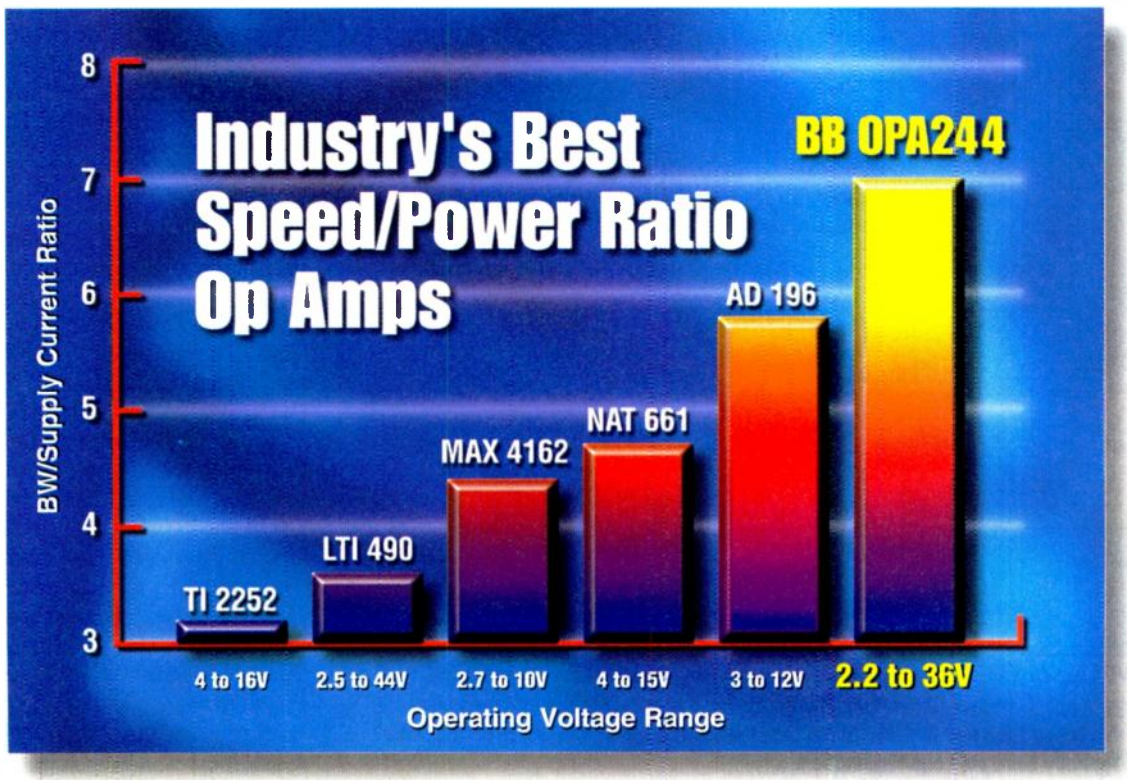
The DS92LV090 bus transceiver overcomes that problem with some innovative calibration circuitry. The



2. The DS92LV090 tranceiver chip implements a 9-bit bus that provides signaling rates greater than 200 Mbit/s. The device operates from a 3.3-V supply, and includes a delay-locked loop that keeps part-to-part skew below ±200 ps. Bus load is light, typically only 5 pF per LVDS load.

microPower PLUS™

More For Le$$!



Speed vs. Power

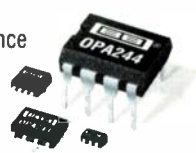
It's a fundamental tradeoff...speed versus power. But now Burr-Brown offers you a new industry best! The **OPA244** family, single and dual versions consume a mere 40µA/channel, yet have a 350kHz bandwidth.

OPA244 operates from a wide power supply range—too, 2.2V to 36V single supply (or ±1.1V to ±18V). Excellent common-mode range to the negative supply, so it's great for battery powered applications.

*micro*Packages!

Great for portable and other compact applications, the OPA244 is available in the tiny SOT-23-5 and the dual version comes in the MSOP-8, half the size of an SO-8.

Burr-Brown offers a wide range of high performance micropower, micropackage op amps, including CMOS and bipolar types. Check our great selection below.



Product	Single Dual,Quad	Offset (mV) max	Drift (µV/°C) typ	BW (MHz)	V_S (V)	I_Q/Chan (µA) max	*micro* Packages	Price/Chan* (1kpcs)	FAX*LINE*# (800) 548-6133	Reader Service #
OPA244	S,D	1	2	0.35	2.2 to 36	50	SOT-23, MSOP**	$0.41	11266	197
OPA234	S,D,Q	0.25	0.5	0.35	2.7 to 36	300	MSOP-8**	$0.88	11269	198
OPA237	S,D,Q	0.75	2	1.4	2.7 to 36	350	SOT-23, MSOP, SSOP**	$0.76	11327	199
OPA241	S,D,Q	0.25	0.4	0.035	2.7 to 36	28	**	$0.90	11406	200
OPA2337	D	3.0	2	3	2.5 to 5.5	750	SOT-23-8**	$0.26	11410	201
OPA336	S,D,Q	0.5	1.5	0.1	2.1 to 5.5	32	SOT-23, MSOP, SSOP**	$0.50	11380	202

*Dual version, recommended resale in US dollars/channel; FOB USA. **Other packages available.

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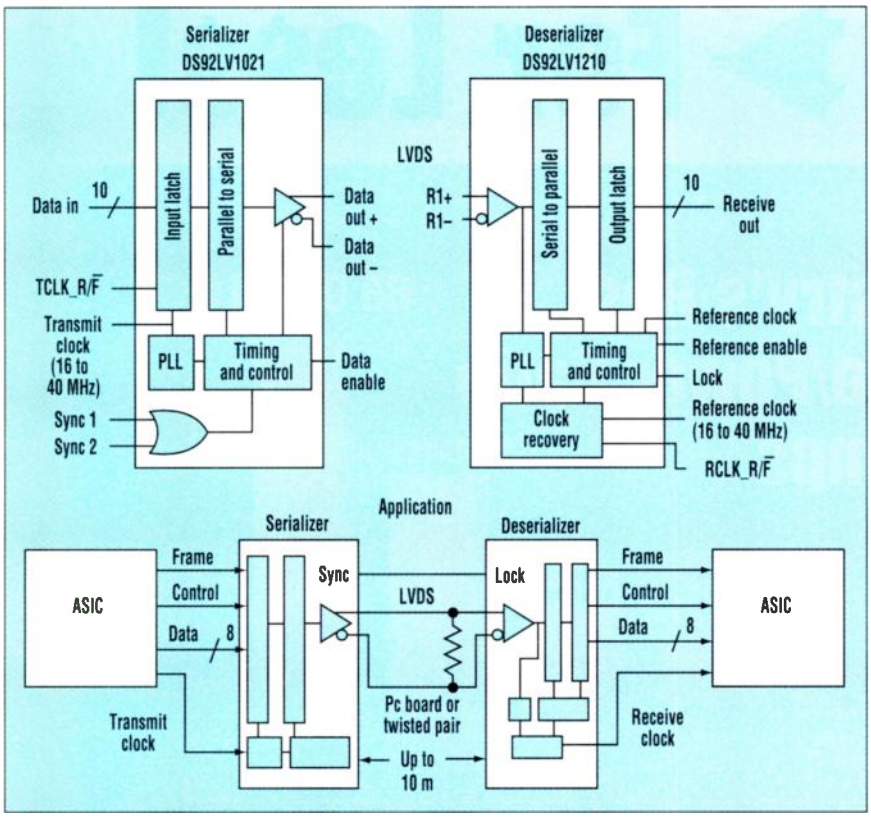

3. Bus LVDS can do 155-Mbit/s data transfers using only 10-mA of loop current. The technology supports both mutlipoint and multidrop architectures. Multipoint buses allow multiple drivers on the same bus. Multidrop buses allow the use of one driver on the same bus, and typically have only one termination.

chip has 10 channels, nine of which are usable for data transmission. The tenth is a calibration channel. The user supplies it with a reference clock of 25 MHz to give this calibration channel an absolute value of time. You can connect the reference clock as a common clock into the other chips, but designers don't need to worry about phase angle. The phase angle of the clock signals into each chip doesn't matter, only the frequency does. That reference clock is used to create a 10-ns pulse that then runs through the calibration channel.

The calibration channel has a series of digital-to-analog converters in it which then drive de-skew circuitry. They're able to adjust the propagation delay, both in the transmit and receive paths, to be 10 ns. These calibration delay elements then drive slaves on the other nine channels to calibrate them, as well. The result is that whether the bus comprises one chip, two chips, or any number of chips, ±200-ps skew is guaranteed from chip to chip. That means that the timing budget on the backplane can be very tight.

For multidrop buses, National Semiconductor offers the S92LV1021 serializer and the complementary DS92LV1210 deserializer. In a multidrop systems, there is one transmitter and multiple receivers. The serializer chip takes in a 10-bit stream, serializes it so that it is then "busable," and then drives it out across the bus. The device also embeds the clock with the data.

The deserializer then takes the serialized stream, deserializes it, and recovers the clock. With the two-chip set you can send, for example, 11 signals across a backplane using just one pair of wires. In this way, you reduce the skew, and the amount of interconnect. The 10 to 40-MHz input clock provides up to a 400-Mbit/s payload over one pair of wires. The 3.3-V chip set consumes only 150 mA of power. Both chips are available in 28-pin SSOP packages.

Users of equipment containing Bus LVDS devices can swap cards for maintenance and upgrades without powering down

Fault Tolerance

Fault tolerance is essential in any backplane application. Bus LVDS provides fault tolerance by going to a high-impedance state when powered-down. Thus, if a card loses power for any reason, signals on the bus do not damage the transceiver or pull the bus down.

Bus LVDS also provides inherent fault-tolerance in extreme bus-contention situations. If all the drivers on a 20-device TTL bus transmit simultaneously, for example, they can dump 2 A on the bus and destroy all the transceivers. This failure is impossible with Bus LVDS for two reasons. First, LVDS is a low-current technology. Second, as Bus LVDS drivers increase the differential voltage on the bus, they reach a point at which they cannot push this differential any wider. They automatically back off to a safe compliance level.

Bus LVDSs differential signals also make it safe to hot swap cards on the bus. So long as the pins of an inserted card connect the bus together (a straightforward requirement), the resulting insertion glitches will been seen as common mode, and will not cause erroneous switching on the bus. Users of equipment containing Bus LVDS devices can, therefore, swap cards for maintenance and upgrades without powering-down the equipment. With Bus LVDS, users get high fault tolerance for continuous up-time and quick mean time to repair.

Price And Availability

Both the DS92LV090 transceiver and the serializer/deserializer chip set are available June 1. In 1000-unit quantities, the 400 Mbit/s DS92LV090 in a 64-pin TQFP is priced at $8.50 each. In 28-pin SSOPs, the DS92LV1021TMA serializer and DS92LV1210TMA deserilaizer are each priced at $9.50 in the same quantities.

National Semiconductor Corp., 2900 Semiconductor Dr., Santa Clara, CA 95052; contact Guy Nicholson, product marketing manager, (408) 721-2431; www.national.com.

CIRCLE 485

SoundPLUS™

Low Cost Audio DACs!

Low Cost ΔΣ Stereo Audio DACs

The *SoundPlus™* **PCM1725** and **PCM1733** are 16-bit and 18-bit pin-for-pin compatible stereo audio D/A converters complete with 3rd-order ΔΣ modulators, 8X oversampling digital interpolation filters (with de-emphasis available at 44.1kHz), and analog output amplifiers. The PCM1725 and PCM1733 are the best low cost solution for CD-quality consumer audio applications. Key features include: 95dB Dynamic Range, 96kHz operation, 256fs/384fs system clock, TTL Logic interface, +5V power supply, and 14-Pin SOIC package. The PCM1725 and PCM1733 are priced from $1.95 in 10,000s.

Products	Description	Bits	Dynamic Range	SNR	THD+N	Maximum Sample Rate	Supply Voltage	Package	FAX*LINE*# (800) 548-6133	Reader Service #
PCM1717/18	DAC	16/18	96dB	100dB	–90dB	48kHz	+2.7 to +5V	20-Pin SSOP	11289, 11325	81
PCM1725	DAC	16	95dB	97dB	–84dB	96kHz	+5V	14-Pin SOIC	11373	82
PCM1733	DAC	18	95dB	97dB	–84dB	96kHz	+5V	14-Pin SOIC	11435	83
PCM1720	DAC	16/20/24	96dB	100dB	–90dB	96kHz	+5V	20-Pin SSOP	11333	84

Low Voltage CMOS Audio Op Amp

The **OPA340** series of rail-to-rail CMOS op amps (single, dual, quad) are optimized for low voltage, single supply operation. Its performance, space saving miniature package, and ability to drive a 600Ω load, make it ideal for low cost audio applications. The OPA340 (single) is priced from $0.59 in 10,000s.

Recommended resale in USD; FOB USA

Key Specifications:

- Wide Bandwidth.....5.5MHz
- High Slew Rate.....6V/µs
- Low THD+N.....0.0007%
- Supply Voltage (single supply).....+2.5V to +5.5V

Reader No. **85** • **FAX***LINE* # 11404

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Get A Firsthand Look At The Display Technologies Of The Future

New Display Technologies, Display-Based Applications, And Advancements In Fabrication Techniques Highlighted At SID '98.

Cheryl Ajluni

Where does one go for the latest information on anything and everything to do with displays? The answer is simple: the 1998 Society for Information Display (SID) international symposium, seminar, and exhibition, scheduled for May 17-22 at the Anaheim Convention Center in Anaheim, Calif. With a line-up of over 350 papers, nearly 400 exhibitors, and a slew of day and evening short courses, seminars, and panel sessions, there is something to appeal to every attendee's level of interest *(see the table)*. As Russel Martin, Principal Scientist at Silicon Image, Inc., San Jose, Calif., and General Chair for SID '98 explains, "The conference has become the leading international forum for advances in electronic-display products, technology, systems, applications, manufacturing, testing, and human factors."

As a result, it seems only fitting that new information on displays—information that will help to change how we live, work, and play—will be delivered near the home of "the most magical place on earth"—Disneyland. And, in keeping with this theme, attendees will be treated to keynote addresses from Hisashi Yamada, Toshiba Corporation, Kawasaki, Japan, who will describe Digital Video Disk (DVD) technology and explore its many applications, and Eric Haseltine, Vice President and Chief Scientist of Walt Disney Imagineering, Anaheim, Calif., who will speak on the continually increasing possibilities for using computers in entertainment.

One of the new items at the show is a Display Technology Showcase. The object of the showcase is to feature side-by-side comparisons of different display technologies intended for similar applications, and operating from the same signal sources.

Some of the technologies that will be featured at the Display Technology Showcase include large video and graphics displays using plasma, liquid-crystal dispaly, cathode-ray tube, and front- and rear-projection technologies; medium to medium-large monitors using a variety of technologies; LCD monitors using TFT, standard STN, and enhanced STN technologies; medical displays; and small datagraphic displays using LCD, FED, LED, and EL technologies.

Display Technology Advances

In recent years, the maturation of the display industry has been dominated by three factors: the demand for more display-based consumer products; the drive toward lower-power, higher-performance portable display technologies; and the call for large-area, low-weight display technologies driven by HDTV and wall-hanging television applications. Not surprisingly, the trends at this year's show are no different.

On the consumer side, an interesting technological development known as the reverse emulsion electrophoretic display (REED) comes from researchers at Zikon Corporation, Campbell, Calif. Basically, it's a flat-panel display (FPD) technology (which utilizes the electrophoretic properties of reverse emulsions) that's being eyed as a viable alternative to LCDs (Liquid Crystal Displays). In its continuous or non-polar phase, this emulsion is a clear liquid. Its polar phase is a liquid that can be colored with virtually any dye as long as it is soluble in a polar solvent and insoluble in the non-polar phase. To form a stable suspension of colored droplets inside the non-polar phase, detergent is used to form micelles containing the polar phase. These colored micelles can then be electrically charged, or otherwise responsive to electric fields, depending on the specific components chosen.

To form the display, this reverse emulsion is injected into a sealed cell. The cell is comprised of two glass plates with etched ITO (Indium Tin Oxide) electrodes. By applying voltages across the emulsion through the ITO electrodes, the color of the display can be changed.

As compared to LCDs, the REED offers higher performance in transmissivity—in excess of 70%, a wider viewing angle, and increased color brightness. The technology also offers lower power consumption, low material cost, is inexpensive to produce, easier to fabricate, and has the potential to display full colors. Further details of this development are highlighted in paper 47, "Reverse emulsion electrophoretic display (REED)."

One of the major factors driving the development of low-power, high-performance portable display technologies is the growing popularity of portable laptop computers and cell phones. To answer this need, a joint team of researchers from Sarnoff Corporation, Princeton, N.J., and Thomson-LCD, Moirans, France, have developed an 8.4-in. a-Si AMLCD (amorphous silicon active matrix liquid crystal display). With a pixel size of 204 μm by 202 μm and an aperture ratio of 45%, it is the first a-Si display designed for direct-view applications, and the largest built to date with integrated row and column drivers.

As summarized in paper 148, "Subnotebook a-Si color SVGA display with integrated drivers," the large-area a-Si AMLCD, with on-board scanners, uses a sample-and-hold column driver with a threshold autozero function. This allows for uniform column charging and an increased data-

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The DACs Are Back!

Burr-Brown's new quad, 12-bit DACs are the first in a new series of BiCMOS D/A converters featuring a voltage output specifically designed for single-supply or low voltage dual-supply applications.

Low Cost

At less than $2.50 per converter, these quad DACs are an ideal solution for multiple output applications such as process control, motor control, ATE, analytical and portable instrumentation.

A DAC Guarantee

DAC7614, **DAC7615**. **DAC7624** and **DAC7625** have guaranteed channel-to-channel matching of linearity to ±1LSB, unipolar zero to ±2LSBs, and bipolar zero to ±1LSB. Plus, they offer 10µs max settling time at only 2.5mW/DAC power dissipation in single supply operation.

Precision Solutions

Burr-Brown has a wide selection of 12- to 18-bit D/A converters featuring competitive pricing! See our web site for a complete listing.

Product	Resolution (Bits)	INL (LSBs)	DNL (LSBs)	Guaranteed Monotonicity	Interface	DAC Interface Features	FAX*LINE*# (800) 548-6133	Reader Service #
DAC7614	12	±1	±1	–40°C to +85°C	Serial	Individual DAC Update	11445	86
DAC7615	12	±1	±1	–40°C to +85°C	Serial	Simultaneous DAC Update	11443	87
DAC7624	12	±1	±1	–40°C to +85°C	Parallel	Output Reset to Mid-Scale	11419	88
DAC7625	12	±1	±1	–40°C to +85°C	Parallel	Output Reset to Zero-Scale	11419	89

*Priced from $9.66 in 1000s. Recommended resale in USD. FOB USA.

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sampling interval. The row drivers incorporate previous line storage with circuitry to reduce horizontal crosstalk. Transistor threshold drift cancellation circuits also are used to extend lifetime. Special bussing techniques are used to help reduce power dissipation.

By now, almost everyone has heard about the coming of HDTV (high-definition television). What we haven't heard is when it will arrive. Part of the problem is standards related and the other part stems from lack of mature technology. One of the most promising candidates for HDTV is PDP (plasma display panel). But until now, they have lacked the higher resolution, larger display area, and higher picture-quality characteristics required by the consumer TV and HDTV markets.

Researchers from NEC Corporation, Kanagawa, Japan, think they have changed all this with the development of a high-contrast 50-in. color AC plasma display. As detailed in paper 165, "High contrast 50-in color AC plasma display with 1365 x 768 pixels," the display features 17 million colors

SID '98 Symposium at a Glance — Anaheim Convention Center

MONDAY MAY 18	TIMES	Room C1	Room C2	Room C3	Room C4	Room B7	Room B8	Times	MONDAY MAY 18
TUESDAY, MAY 19	7:00 a.m. – 9:00 p.m.							5:00 – 9:00 p.m.	
	7:00 – 8:00 a.m.					APPLICATIONS SEMINAR A-1 How to Assess Display Markets and Technologies (7:30–9:00)	APPLICATIONS SEMINAR A-2 LCD Optical Performance Modeling (7:30–9:00)	7:00 – 8:00 a.m.	TUESDAY, MAY 19
	8:00 – 8:45 a.m.		SESSION 1 Annual SID Business Meeting					8:00 – 8:45 a.m.	
	8:45 – 9:00 a.m.		SESSION 2 Formal Opening					8:45 – 9:00 a.m.	
	9:00 – 10:20 a.m.		SESSION 3 Keynote Addresses					9:00 – 10:20 a.m.	
	10:20 – 10:40 a.m.	Coffee Break (Exhibit Hall B)		Coffee Break (Exhibit Hall B)		Coffee Break (Exhibit Hall B)		10:20 – 10:40 a.m.	
	10:40 – 12:00 p.m.	SESSION 4 Organic Displays	SESSION 5 Reflective Light Valves	SESSION 6 Polymer Laminates for LCDs	SESSION 7 Applications Avionics Displays	SESSION 8 Color CRTs		10:40 – 12:00 p.m.	
	12:00 – 2:00 p.m.	Lunch Break		Lunch Break		Lunch Break		12:00 – 2:00 p.m.	
	2:00 – 3:20 p.m.	SESSION 9 FEDs I	SESSION 10 Projection Systems	SESSION 11 LC Alignment	SESSION 12 Applications Backlight Technology	SESSION 13 Visual Performance Issues in CRTs		2:00 – 3:20 p.m.	
	3:20 – 3:40 p.m.	Coffee Break (Exhibit Hall B)		Coffee Break (Exhibit Hall B)		Coffee Break (Exhibit Hall B)		3:20 – 3:40 p.m.	
	3:40 – 5:00 p.m.	SESSION 14 FEDs II	SESSION 15 Large-Area Displays	SESSION 16 Reflective LCDs	SESSION 17 Backlighting Systems	SESSION 18 CRT Technology I		3:40 – 5:00 p.m.	
	5:30 – 6:30 p.m.	Author Interviews (Exhibit Hall B)		Author Interviews (Exhibit Hall B)		Author Interviews (Exhibit Hall B)		5:30 – 6:30 p.m.	
	6:00 – 7:30 p.m.	Exhibitor Reception (Exhibit Hall B)		Exhibitor Reception (Exhibit Hall B)		Exhibitor Reception (Exhibit Hall B)		6:00 – 7:30 p.m.	
	8:00 – 10:00 p.m.	EVENING PANEL DISCUSSIONS E-1 Display Viewability	E-2 Reflective LC Devices on CMOS Backplanes					8:00 – 10:00 p.m.	
WEDNESDAY, MAY 20	7:00 – 9:00 a.m.					APPLICATIONS SEMINAR A-3 Optics for Light-Valve Projection Systems (7:30–9:00)	APPLICATIONS SEMINAR A-4 FPD Measurement and Standards (7:30–9:00)	7:00 – 9:00 a.m.	WEDNESDAY, MAY 20
	9:00 – 10:20 a.m.	SESSION 19 Color Plasma Displays I	SESSION 20 Novel AMLCDs	SESSION 21 Reflective and Wide-Viewing-Angle Displays	SESSION 22 Navigation and Vehicle Display Systems	SESSION 23 CRT Technology II		9:00 – 10:20 a.m.	
	10:20 – 10:40 a.m.	Coffee Break (Exhibit Hall B)		Coffee Break (Exhibit Hall B)		Coffee Break (Exhibit Hall B)		10:20 – 10:40 a.m.	
	10:40 – 12:00 p.m.	SESSION 24 Color Plasma Displays II	SESSION 25 a-Si AMLCD Devices and Processes	SESSION 26 Materials for LCDs	SESSION 27 Image Resolution	SESSION 28 CRT Electron Guns		10:40 – 12:00 p.m.	
	12:00 – 2:00 p.m.	SID Luncheon (Anaheim Marriott -- Grand Ballroom)		SID Luncheon (Anaheim Marriott -- Grand Ballroom)		SID Luncheon (Anaheim Marriott -- Grand Ballroom)		12:00 – 2:00 p.m.	
	2:00 – 3:00 p.m.	Executive Poster Sessions (Anaheim Marriott -- Orange County Ballroom)		Executive Poster Sessions (Anaheim Marriott -- Orange County Ballroom)		Executive Poster Sessions (Anaheim Marriott -- Orange County Ballroom)		2:00 – 3:00 p.m.	
	2:00 – 5:00 p.m.	Poster Session (Anaheim Marriott -- Marquis Ballroom)		Poster Session (Anaheim Marriott -- Marquis Ballroom)		Poster Session (Anaheim Marriott -- Marquis Ballroom)		2:00 – 5:00 p.m.	
	4:30 – 5:30 p.m.	Author Interviews (Exhibit Hall B)		Author Interviews (Exhibit Hall B)		Author Interviews (Exhibit Hall B)		4:30 – 5:30 p.m.	
	6:00 – 10:00 p.m.	Special Event (Lakeside Pavilion)		Special Event (Lakeside Pavilion)		Special Event (Lakeside Pavilion)		6:00 – 10:00 p.m.	
THURSDAY, MAY 21	7:00 – 9:00 a.m.					APPLICATIONS SEMINAR A-5 Display Module Electronics (7:30–9:00)	APPLICATIONS SEMINAR A-6 Going Digital (7:30–9:00)	7:00 – 9:00 a.m.	THURSDAY, MAY 21
	9:00 – 10:20 a.m.	SESSION 29 Manufacturing Emissive Displays	SESSION 30 Poly-Si AMLCD Devices and Processes	SESSION 31 Cholesteric LCDs	SESSION 32 3-D Display Systems	SESSION 33 Display Measurement		9:00 – 10:20 a.m.	
	10:20 – 10:40 a.m.	Coffee Break (Exhibit Hall B)		Coffee Break (Exhibit Hall B)		Coffee Break (Exhibit Hall B)		10:20 – 10:40 a.m.	
	10:40 – 12:00 p.m.	SESSION 34 Electroluminescent Displays	SESSION 35 Direct-View a-Si AMLCDs	SESSION 36 LC Modeling	SESSION 37 Novel Displays	SESSION 38 Spatio-Temporal Visual Interactions		10:40 – 12:00 p.m.	
	12:00– 2:00 p.m.	Lunch Break		Lunch Break		Lunch Break		12:00– 2:00 p.m.	
	2:00 – 3:20 p.m.	SESSION 39 FEDs III	SESSION 40 AMLCD Projection Light Valves	SESSION 41 Wide-Viewing-Angle LCDs	SESSION 42 Display Manufacturing Thin-Film Coating & Processes	SESSION 43 Image Quality		2:00 – 3:20 p.m.	
	3:20 – 3:40 p.m.	Coffee Break (Room C Lobby)		Coffee Break (Room C Lobby)		Coffee Break (Room C Lobby)		3:20 – 3:40 p.m.	
	3:40 – 5:00 p.m.	SESSION 44 Late-News Papers	SESSION 45 Display Interfaces and Drivers	SESSION 46 Ferroelectric LC Devices	SESSION 47 Display Manufacturing AMLCDs	SESSION 48 Visual Factors and Display Performance		3:40 – 5:00 p.m.	
	5:30 – 6:30 p.m.	Author Interviews (Exhibit Hall B)		Author Interviews (Exhibit Hall B)		Author Interviews (Exhibit Hall B)		5:30 – 6:30 p.m.	

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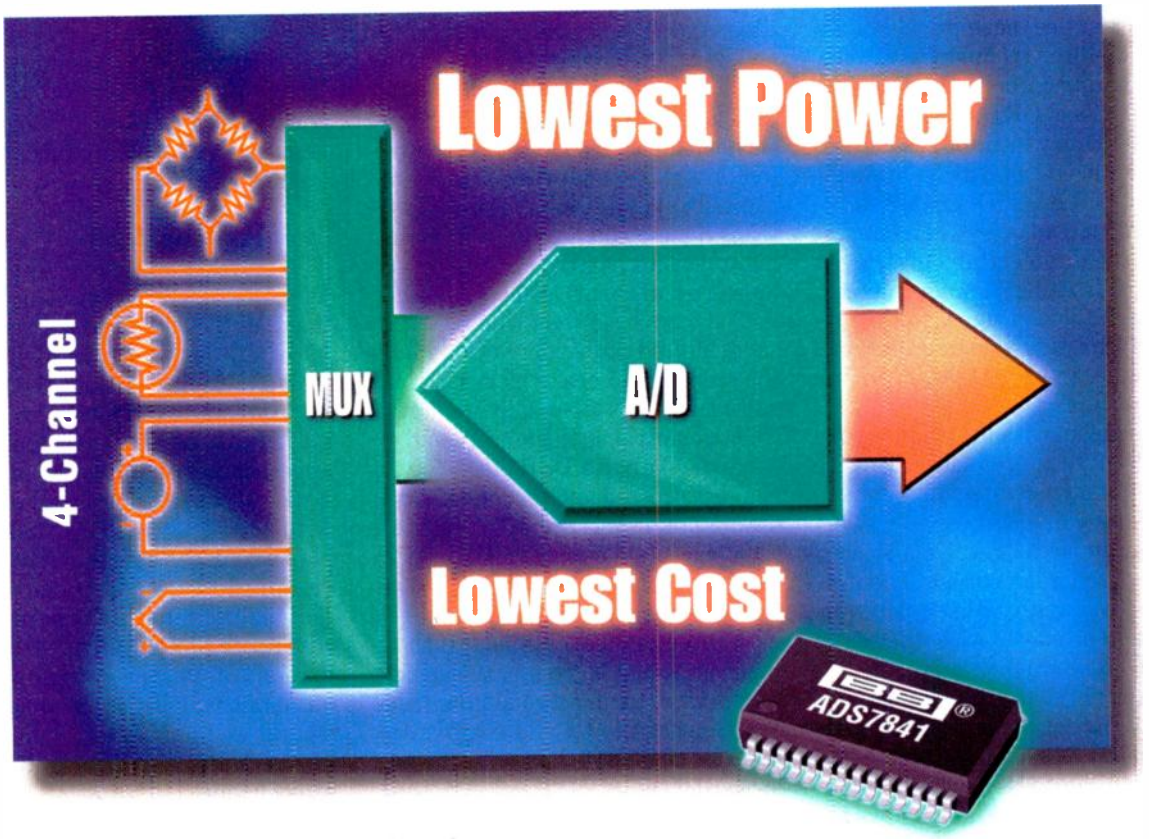
Smallest 4-Ch, 12-Bit A/D



Simplify Your Data Collection Applications

Burr-Brown's family of 12- and 16-bit, 4-channel, A/D converters continues to grow and provide you with the best price/performance options available on the market. These converters feature an on-board multiplexer, and are complete with internal clock, S/H amplifier, and internal voltage reference. All offer low power, parallel and serial outputs, and a continuous conversion mode that allows you to sample sequentially through all four channels. Plus, the serial interface also provides a low-cost isolation solution for remote data acquisition. With conversion rates up to 200kHz and power dissipation under 15µW in shutdown mode, these products are ideal for battery operated systems such as personal digital assistants, portable data loggers, and measurement equipment.

ADS7841 Key Specifications:

- Single Supply: 2.7V to 5V
- 4-Channel Single-Ended or 2-Channel Differential Input
- Up to 200kHz Conversion Rate
- Serial Interface
- Alternate Source for MAX1247
- 16-Lead SSOP Package

Product	Resolution (Bits)	Channels	INL (LSB)	NMC*	Sample Rate (kHz)	Power (mW)	SINAD (dB)	Price (1kpcs)	FAX*LINE*# 1-800-548-6133	Reader Service #
ADS7824	12	4	±0.5	12	40	50	73	$12.30	11303	203
ADS7825	16	4	2	16	40	50	86	$28.46	11304	204
ADS7832	12	4	±0.75	12	117	14	71	$16.00	11332	205
ADS7841	12	4	±1	12	200	3	72	$4.59	11420	206

*No Missing Codes

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and can display both HDTV (Hi-Vision) and XGA (PC) images with a 350:1 dark-room contrast ratio. This latter feature is made possible by the use of a single priming drive sequence. The PDP also uses an improved capsulated color-filter technology and features a wider color array than the more traditional CRT.

NEC's display monitor is a mere 97 mm in depth—despite its 50-in. diagonal area, and has an aspect ratio of 16:9. Using a dual-scan technique, the panel can be driven in 8-bit gray levels without miswriting. A scaling IC converts the Hi-Vision signal to 768 progressive scan data allowing the panel to reproduce vivid high-definition moving pictures.

One problem with the conventional CRT is that its curved face can cause distorted images when viewed from the side, as well as unwanted reflections from ambient light. Thanks to researchers from Mitsubishi Electric Co., Kyoto, Japan, these problems have now been solved with a perfectly flat face color-display tube. As detailed in paper 236, "Development of perfectly flat face color display tube DIAMONDTRON NF," this tube features high brightness and high resolution, is distortion free, and allows for natural-looking flat images. Because the tube is flat, the reflection and glare caused by ambient light is significantly reduced.

The DIAMONDTRON NF tube was developed using an accurately calculated polynomial curve based on typical usage environments and human vision characteristics. It incorporates a host of new technologies including a tempered glass bulb, flatter aperture grille, and a new electron gun. Its surface is treated with an antireflection coating.

Emerging Applications

One exciting feature of the SID show is that it affords attendees the opportunity to get a first glimpse at some of the more innovative uses of display technology; especially as it pertains to consumer products. An interesting development in this area comes from a joint effort by Jaguar Cars Ltd., Coventry, England; Texas Instruments (TI), Dallas; and Pilkington Optronics, Glasgow, Scotland, to develop an automotive Heads Up Display (HUD). The system, which uses a HUD to project an enhanced image into the drivers line of view, incorporates a variety of technologies including Pilkington's optical modules, and TI's digital near-infrared (NIR) CCD camera.

The project, summarized in paper 97, "Evaluation of flat panel display technologies for an automotive night vision enhancement HUD system," came about as a result of human factor trials done by Jaguar indicating that night vision systems can dramatically improve automotive safety.

The way the system works is that a set of filtered car headlights illuminate the scene ahead of a vehicle with NIR radiation. A NIR-sensitive digital CCD camera images the scene and exports the data to a DSP. Here, the image is processed and presented to the display. The HUD display module then projects the image off a partially reflective combining element. The image becomes superimposed on the real view through the windshield and is focused at a point in front of the vehicle. To a driver looking through the windshield, what they would see is an enhanced image overlaid onto the real forward view.

Work on this system is now focused on the use FPDs, as opposed to CRTs. This could lead to substantial improvements in performance while reducing volume, complexity, and unit cost. A production-intent prototype of the system is expected to be developed next year.

Medical Imaging

In the medical arena, researchers from the X-ray Imaging Research Laboratory, Henry Ford Health System, Detroit, Mich., have developed a computational method for examining the effect of rough surfaces and antireflective thin-film coatings on luminance spread functions. This is an especially critical capability for medical imaging applications where images with wide luminance range and low contrast detail are displayed.

To achieve the required display quality for medical applications, careful control of the light transport processes in the faceplate of CRTs is needed. But, the luminance range of CRT systems is limited by the glare associated with light diffusion in the thick glass faceplate.

One way to deal with this problem is through the use of an optical Monte Carlo simulation code (DETECT-II). This code, written in FORTRAN 90, can effectively model the luminance spread in emissive structures. Specific details of the code are presented in paper 260, "X-ray Monte Carlo modeling of glare in cathode-ray tubes for medical imaging."

Eyeglass Displays

A new approach to the design of an eyeglass-based display is highlighted in paper 250, "Optical approaches to incorporation of displays within eyeglasses," from The MicroOptical Corporation and Northeastern University, both of Boston, Mass. The approach incorporates the optical relay between the display and the eye within the eyeglass lens, and the display within the eyeglass temple. This design offers an eyeglass appearance that is acceptable to the user. Such an advance is significant since the development of wearable computers requires a portable display that is lightweight and low power, and that can be operated without requiring the use of hands.

The system uses a 0.25-in. diagonal, 320 X 240 pixel format AMLCD, and an optical relay built into the frames. The display and backlight are mounted within the temple of the glasses. The image is provided to the eye by the optical relay mounted within the eyeglass lens. When the display is turned off, the system reverts back to ordinary glasses. A cable runs through the temple that connects the analog AMLCD to drive electronics. The electronics receive standard VGA signals and convert the data to the format required to drive the 320 X 240 display. A monochrome version of this eyeglass system has already been developed, with a color version currently being developed.

Anyone looking for more information on display technologies or a glance at some the latest display-based products should look no farther than SID. For more information on the conference or to register, contact Mark Goldfarb, Palisades Institute for Research Services, 201 Varick St., Suite 1006, New York, NY 10014; (212) 620- 3380; fax (212) 620-3379.

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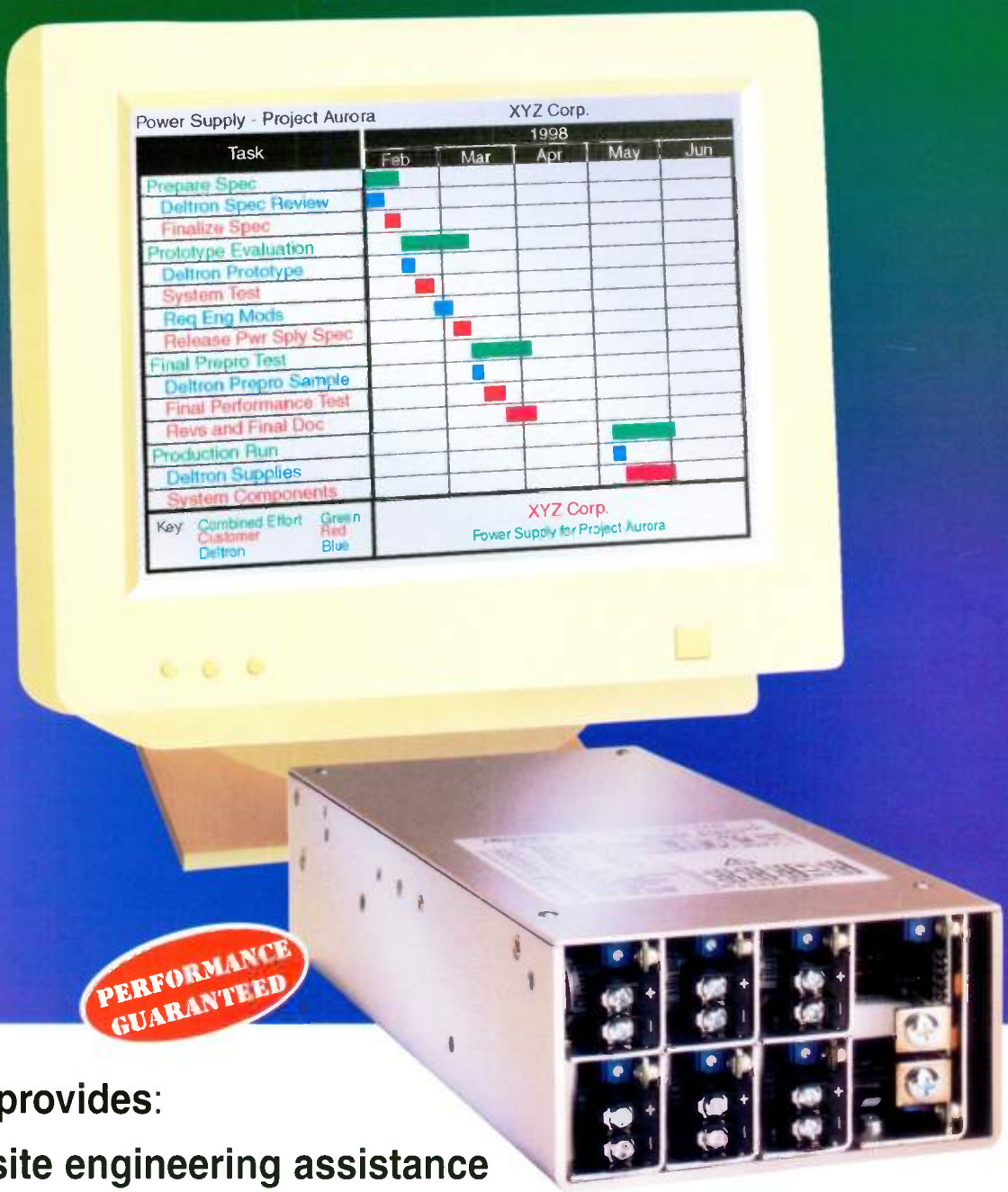

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- 1 - 7 Outputs
- Ultra Compact Size

FT • FS SERIES MODUFLEX ® SWITCHERS

DESCRIPTION

The FT and FS Series are comprehensive lines of ultra compact power factor corrected models derived from our Moduflex® family of switching power supplies. This series utilizes advanced technology to produce a high quality input current wave form that is compliant to the harmonic requirements of EN61000-3-2. Based on modular construction, "off the shelf" modules permit high volume manufacturing with an outstanding quality level assuring timely delivery at a competitive cost.

Three classes of output modules are available. The **STANDARD** outputs allow short duration surge currents on all auxiliaries for hard starting loads. Optional **CURRENT LIMITED** outputs have square current limiting and feature wireless droop current sharing. Optional **ENHANCED** outputs have square current limiting, one wire star point current share, output good logic signal with LED, nominal 5V local bias, individual inhibit and margining. For requirements that cannot provide minimum load on the main output, the **ZERO PRELOAD** option is available for main outputs up to 500 watts.

DELIVERY

Choose stocked units or construct a model number using stocked modules for fast delivery. Otherwise, form a model from the adjacent page to meet your specific requirements. Contact factory for deliveries on models derived from non-stocked modules.

FEATURES

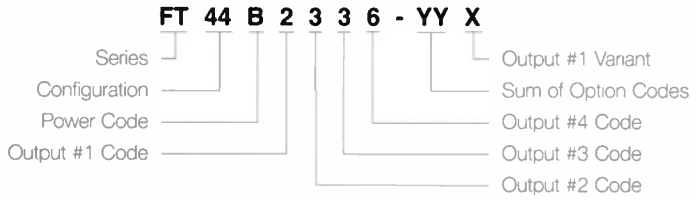
- 0.99 power factor.
- 5.5 watts per cubic inch.
- 1-7 outputs, 400-1000 watts.
- 120 kilohertz MOSFET design.
- Universal input.
- UL, CSA, TÜV (IEC, EN), CE.
- FCC, EN Class A EMI.
- IEC, EN Immunity.
- All outputs:
  - *Adjustable*
  - *Fully regulated*
  - *Floating*
  - *Overload and short circuit protected*
  - *Overvoltage protected*
- Standard features include:
  - *System inhibit*
  - *Fan output*
- Options and accessories include:
  - *Power fail monitor*
  - *Redundancy*
  - *Current Limited Outputs*
  - *Enhanced Outputs*
  - *Zero Preload*
  - *End fan cover*
  - *Top fan cover*
  - *Rack Assemblies*

STOCKED MODELS - Available in 3 days.

Max Power	Output 1	Output 2	Output 3	Output 4	Model*
400W	5V @ 50A	12V @ 12A	12V @ 12A	5V @ 10A	FT46A2332-45P
400W	5V @ 50A	12V @ 12A	24V @ 6A	12V @ 6A	FT46A2363-45P
600W	5V @ 60A	12V @ 12A	12V @ 12A	5V @ 10A	FT46C2332-13P
600W	5V @ 60A	12V @ 12A	24V @ 6A	12V @ 6A	FT46C2363-13P

**400W models include power fail monitor, current limited modules, zero preload and end fan cover options.*
600W models include the same options except fan cooling is built into the unit.

UNITS FROM STOCKED MODULES - Available in 2 weeks.



Configuration: Allowable quad output configurations are 42, 44, 46 and 48.
Power Code: Choose Power Code A through D for 400-750W models.
Output Codes: Select any outputs from the shaded area on the Output Types table consistent with the configuration chosen.
Option Code: Specify Option Code. Refer to the Option table. Codes 02 (redundancy) and 16 (enhanced) are excluded from models available in 2 weeks. Fan cooling is built into 600 and 750W units.

OPTIONS

Option Code	Function
00	None
01	Power Fail Monitor
02	Redundancy
04	Current Limited
08	Zero Preload
16	Enhanced
32	End Fan Cover
64	Top Fan Cover

Replace the YY with the sum of the Option Codes.

MODEL SELECTION

Models are available in power ratings of 400 to 1000 watts, with corresponding code letters A through E. See Power Code chart.

Output modules are available in six types: J, K, L, M, N and P in nominal power ratings from 75 - 500 watts. Type M, N and P modules are variable power rated depending upon the unit power rating. The M, N and P Module table directly below shows the corresponding multiplier applicable to the output current ratings of the M modules and allowable power ratings for the N and P modules. For example, a 750 watt multiple will have its M type module configured to produce 120A @ 5V or 12A @ 48V. The voltage and current rating of output modules are listed in the table of output types. This table assigns an alpha-numeric code designating the nominal voltage rating of the module.

Power Code	Unit Power Rating	M Module Current Multiplier		N/P Module*
		Single Output	Multiple Output	Allowable Power Rating
A	400W	0.8	0.5	250W
B	500W	1.0	0.6	300W
C	600W	1.2	0.8	400W
D	750W	1.5	1.2	500W
E	1000W	2.0	1.5	750W

**When an N or P module is used as the main output, the allowable power and the module current ratings must not be exceeded.*

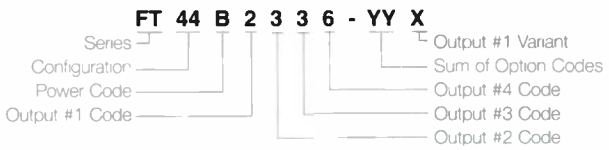
Output Types*						
Output		Module Type				
Code	Volts	J Amps	K Amps	L Amps	M Amps	N/P Amps
0	2	10	20	30	100	60
1	3.3	10	20	30	100	60
2	5	10	20	30	100	60
3	12	6	12	24	42	42
4	15	5	10	20	33	33
5	18	4	8	16	28	28
6	24	3	6	12	21	21
7	28	2.5	5	10	18	18
8	36	2	4	8	14	14
9	48	1.5	3	6	10	10
A	2.2	10	20	30	100	60
B	2.4	10	20	30	100	60
C	2.7	10	20	30	100	60
D	3	10	20	30	100	60
E	3.6	10	20	30	100	60
F	4	10	20	30	100	60
G	4.5	10	20	30	100	60
H	5.7	10	20	30	90	60
J	6.3	10	20	30	80	60
K	7	9	18	30	70	60
L	8	8	16	30	62	60
M	9	8	15	30	56	56
N	10	7	14	30	50	50
P	11	7	13	27	45	45
Q	13.5	6	11	22	37	37
R	17	5	9	18	30	30
S	19	4	8	16	26	26
T	21	4	7	14	24	24
U	23	4	7	13	22	22
V	26	3	6	12	19	19
W	29	3	5	10	17	17
X	32	2	5	9	16	16
Y	40	2	4	8	13	13
Z	44	2	4	7	12	12

Multiple output modules of a given type are arranged in ascending order by voltage magnitude in the same sense as the output number sequence in the configuration diagrams.
**Shaded ratings are stock.*

HOW TO ORDER

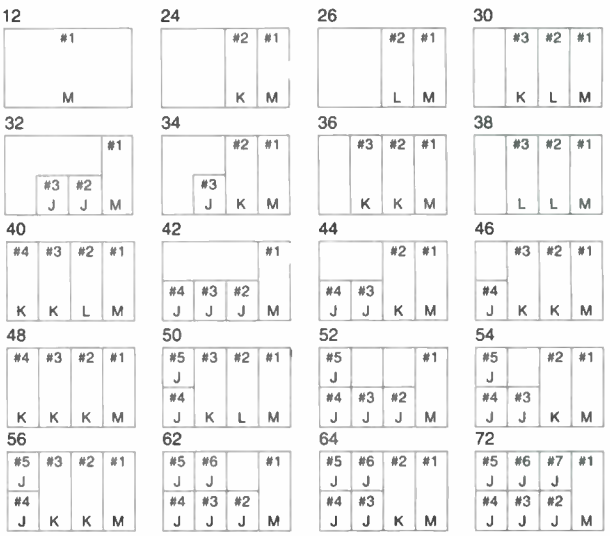
To form the proper model number defining a custom requirement, select the letters FS or FT to designate the series, then choose the desired configuration and list the configuration code. Insert the power code letter for the power level and follow with the output code numbers or letters for each specific output. Enter a dash and from the option table insert the sum of the option codes. Where lower power is desired for the main module, an N module can be substituted and is denoted by a letter N in the output variant position. In addition, when no preload is available for the main output, choose Option Code 08 and add a P in the output variant position. For an enhanced **main** and **current** limited auxiliaries, specify both 04 and 16 option codes.

HARMONIC CORRECTED 500W QUAD SWITCHER



OUTPUT CONFIGURATIONS

The boxes below are diagrammatic representations of the power supplies as viewed from the output end. The two-digit numbers above the boxes are the configuration codes.



Refer to the table below for allowable configurations by series.

Output Config	Unit Power Rating				
	400W	500W	600W	750W	1000W
12	•	•	• x	• x	x
24	•			• x	
26		•	• x	• x	x
30					x
32	•			• x	
34	•	•	• x	• x	
36	•	•	• x	• x	x
38					x
40					x
42	•	•	• x	• x	
44	•	•	• x	• x	x
46		•	• x	• x	x
48			x		x
50					x
52	•	•	• x	• x	x
54		•	• x	• x	x
56			x		x
62		•	• x	• x	x
64			x		x
72			x		x

• *Represents allowable configurations for the FT Series.*
x *Represents allowable configurations for the FS Series.*

SPECIFICATIONS

INPUT
90-264 VAC, 47-63 Hz.

POWER FACTOR
0.99 typical.

EMISSIONS
FCC 20780 Part 15/EN 55022, Class A Conducted. EN 61000-3-2, Harmonics. EN 61000-3-3, Voltage Fluctuations.

IMMUNITY
IEC 1000-4-2/EN 61000-4-2, Electrostatic Discharge. IEC 1000-4-3/EN 61000-4-3, Radiated Field. IEC 1000-4-4/EN 61000-4-4, Electrical Fast Transients. IEC 1000-4-5/EN 61000-4-5, Level 3 Surge. IEC 1000-4-6/EN 61000-4-6, Conducted Field.

INPUT SURGE
230 VAC - 38 amps max. 115 VAC - 19 amps max.

EFFICIENCY
75% typical.

HOLDUP TIME
20 milliseconds from loss of AC power.

OUTPUTS
See model selection table. Outputs are trim adjustable ±5%.

OUTPUT POLARITY
All outputs are floating from chassis and each other and can be referenced to each other or ground as required.

LINE REGULATION
Less than ±0.1% or ±5mV for input changes from nominal to min. or max. rated values.

LOAD REGULATION
±0.2% or ±10mV for load changes from 50% to 0% or 100% of max. rated values.

MINIMUM LOAD
Main output requires a 10% minimum load for full output from auxiliaries. Use Option 08 if no minimum load is available for mains up to 500 watts. Singles require no minimum load.

RIPPLE & NOISE
1% or 100 mV, pk.-pk., 20 MHz bandwidth.

OPERATING TEMPERATURE
0-70°C. Derate 2.5%/°C above 50°C.

COOLING
A min. of 10 LFS* for models without internal fans directed over the unit for full rating. Two test locations on chassis rated for max. temperature of 90°C. 600 watt, 750 watt and 1000 watt models have built-in ball bearing fans.
*Linear feet/second.

TEMPERATURE COEFFICIENT
±0.02%/°C.

DYNAMIC RESPONSE
Peak transient less than ±2% or ±200 mV for step load change from 75% to 50% or 100% max. ratings.

RECOVERY TIME
Recovery within 1%. Main output - 200 microseconds. Auxiliary outputs - 500 microseconds.

SAFETY
Units meet UL 1950, CSA 22.2 No. 950, EN 60 950, IEC 950.

ISOLATION
Conforms to safety agency standards.

INPUT UNDERVOLTAGE
Protects against damage for undervoltage operation.

SOFT START
Units have soft start feature to protect critical components.

OVERVOLTAGE PROTECTION
Standard on all outputs.

REVERSE VOLTAGE PROTECTION
All outputs are protected up to load ratings.

OVERLOAD & SHORT CIRCUIT
Outputs protected by duty cycle current foldback circuit with automatic recovery. Standard auxiliaries have additional back-up fuse protection. Options 04 and 16 have square current limiting with automatic recovery when overload is removed.

THERMAL SHUTDOWN
Circuit cuts off supply in case of local over temperature. Units reset automatically when temperature returns to normal.

FAN OUTPUT
Nominal 12 VDC @ 12 watts maximum.

INHIBIT
TTL compatible system inhibit provided. Option 16 has individual output inhibit.

REMOTE SENSING
On all outputs except standard and 04 Option outputs 75 watts or less.

SHOCK & VIBRATION
Shock per MIL-STD 810-E Method 516.4, Procedure I. Vibration per MIL-STD 810-E Method 514.4, Category 1, Procedure I.

MECHANICAL

CASE	SERIES	WATTS	H	x	W	x	L
1	FT	400W/500W	2.50"	x	4.93"	x	8.00"
3	FT	600W	2.56"	x	5.08"	x	10.03"
4	FS	600W	2.56"	x	5.08"	x	11.00"
5	FT	750W	2.63"	x	5.20"	x	10.03"
6	FS	750W	2.63"	x	5.20"	x	11.63"
7	FS	1000W	2.56"	x	7.13"	x	11.63"

OPTIONS

POWER FAIL MONITOR
Optional circuit provides isolated TTL and VME/VXI compatible ACFAIL signal providing 4 milliseconds warning before main output drops by 5% after an input failure. A SYSRESET signal following VME timing requirements is provided when an N module is used as a main output. Both logic signal outputs can sink current per the VME specification.

REDUNDANCY
Optional Or-ing diodes for hot pluggable N+1 redundant operation. For FT Series 500 watt & 750 watt models with 1-4 outputs. Main output current limited to 100 amps. Remaining outputs 16 amps max.

CURRENT LIMIT
Option provides on all outputs:
- Square current limit with auto recovery.
- Wireless droop current share for parallel or N+1 redundant operation.

ZERO PRELOAD
Optional circuit removes need for preload on main output up to 500 watts.

ENHANCED
Option provides on all outputs:
- Square current limit with auto recovery.
- Single wire active current share for parallel or N+1 redundant operation.
- DC output good logic signal with LED indicator.
- Logic inhibit.
- Nominal 5V bias.
- Margining.

END FAN COVER
Optional cover with brushless DC ball bearing end fan which provides the required air flow for full rating.

TOP FAN COVER
Same as above with fan cover mounted on top of the power supply.

ACCESSORIES
RA50 and RA75 Series 2U high rack assemblies provide hot pluggable interface and hold up to 3 FT Series 500 watt or 750 watt units respectively.

Specifications subject to change without notice.

Deltron inc. POWER PRODUCTS

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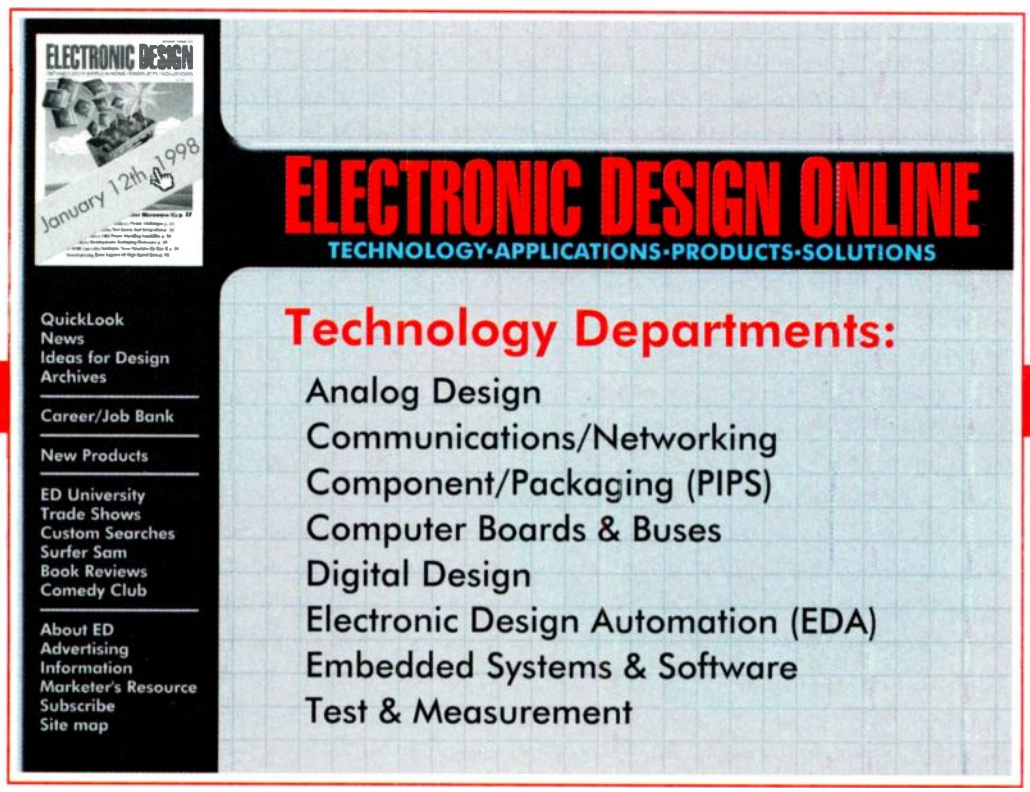

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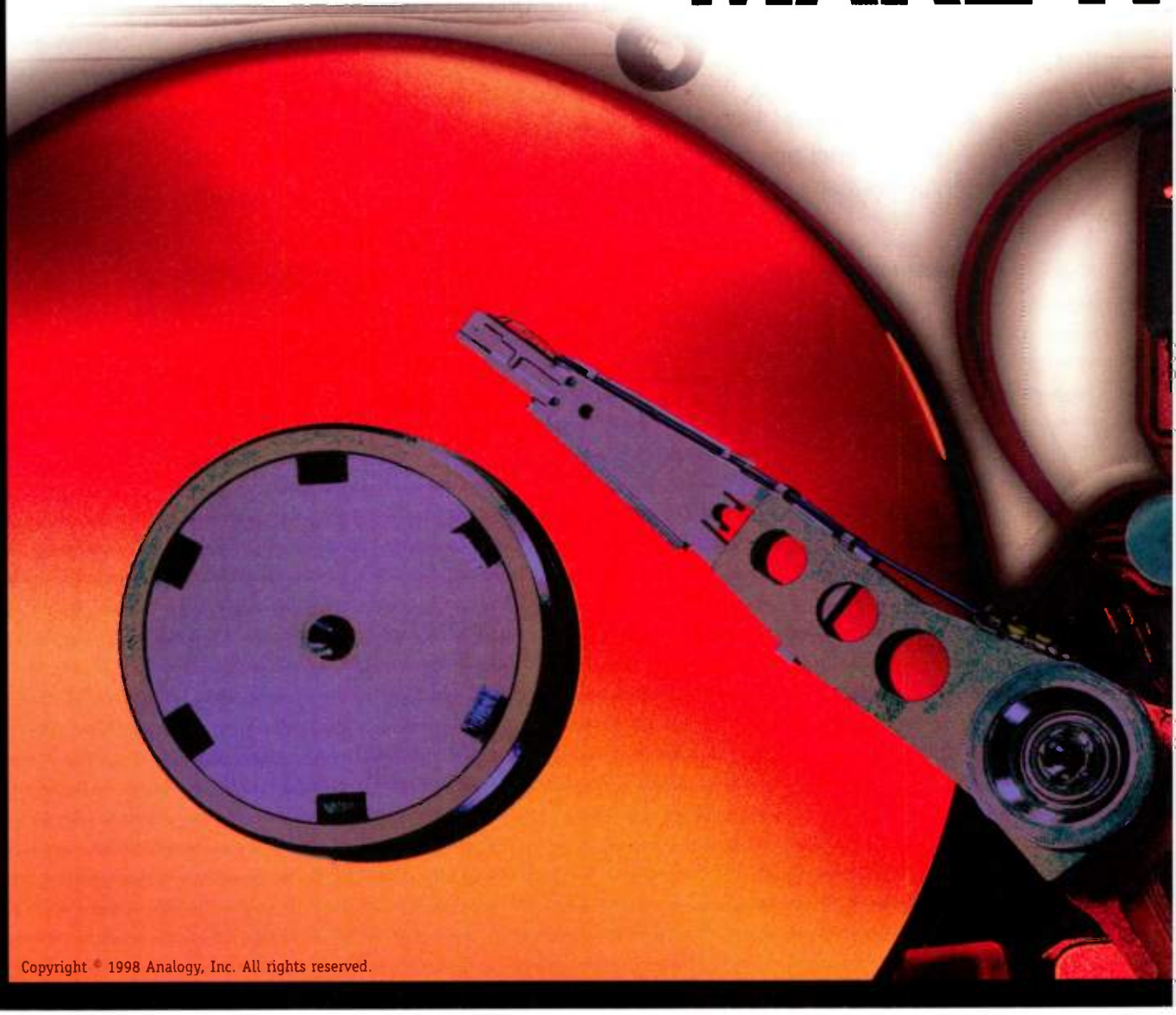
How can IC designers CUT THE at the fab stage? Texas Instruments used Analogy to GET IT RIGHT in the able to take a spec and MAKE IT



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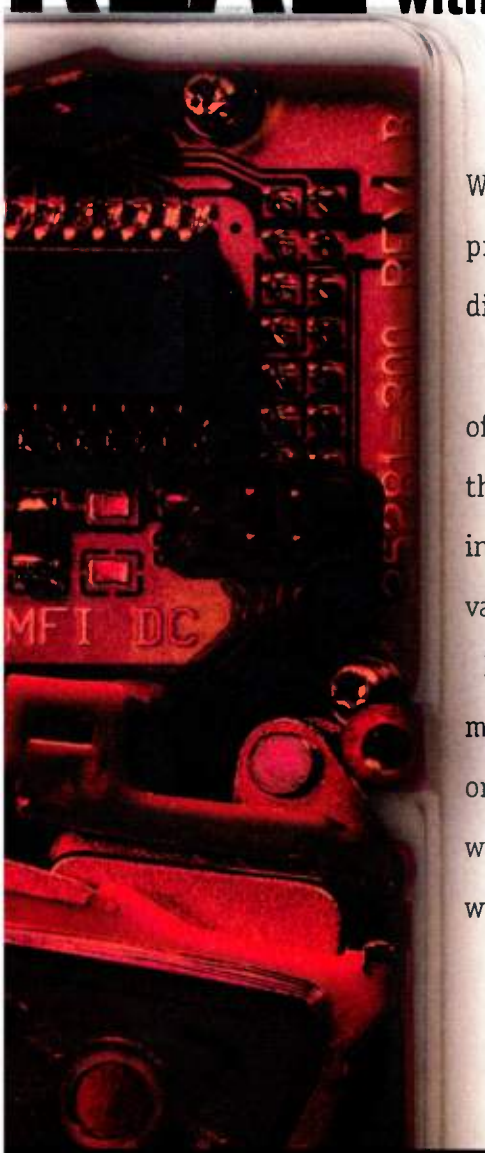
first pass. They were REAL within 24 hours after first silicon.



Within a day after the first silicon came in, Texas Instruments' prototype control chip was up and turning their client's disk drive.

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SOFTWARE DEVELOPMENT TOOL INTEGRATION

Software Development Tools Take On Integration Challenges

From Cruise Missiles To Luxury Cars, Software Tools Progress To Meet The Needs Of A Plethora Of Embedded Designs.

Teri Sprackland

Software development tool makers are busy trying the meet the reliability and ease-of-use needs of software developers. Answering these demands is becoming more critical as more and more embedded systems emerge to control everything from small toasters in the home to large industrial plants.

The best way to ensure software reliability is to develop the software using a process that is well defined, known, transparent, repeatable, and modifiable. That means making use of a suite of software-development tools that are not only compatible with one another, but are also totally integrated within one system.

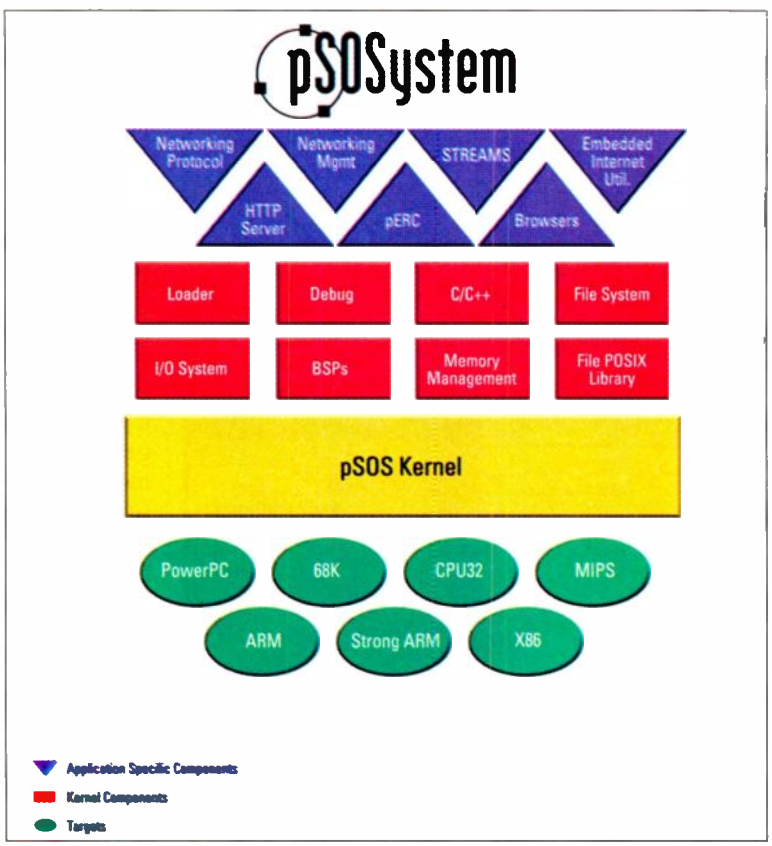
SPECIAL REPORT

The early suites of software development tools included source text editors and compilers, data-flow diagramming tools, requirements trackers, and critical-path calendar creators. Newer development-tool suites now offer a broader range of tools that are integrated to work together, and are open to allow the use of proprietary as well as third-party tools developed to meet a specific application need.

The challenge to software programmers is still essentially to develop reliable software code, and to deal with its complexity as quickly as possible. Further accentuating these challenges are the different end markets that are being addressed. The automobile industry, for example, works on much slimmer profit margins than the defense industry, and the task must be accomplished with time-to-market and cost considerations being met as well.

"There are 10 to 15 microprocessors in today's cars," notes Steve Houtchens, director of new technology at Integrated Systems Inc. "The customer must be able to depend on total reliability for something like the antilock brakes," he continues. Tool integration allows software to take over part of the coordination functions that middle managers once performed in less-complex development environments.

Recompiling an entire system may be impractical, due to time or resource constraints. Software development tool suites can keep track of where the interfaces between modules are, and can help the user manage the various versions and configurations.



Art Courtesy: Integrated Systems Inc.

Many Solutions

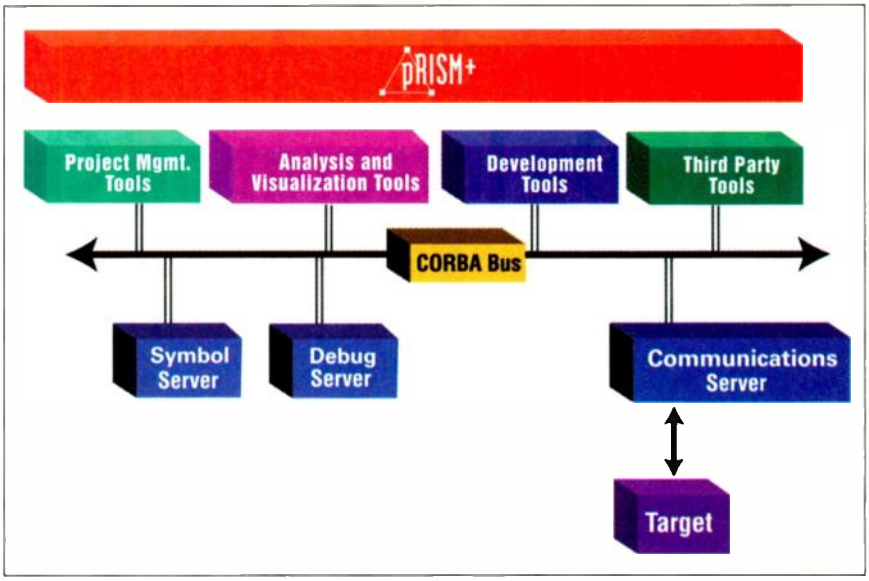
To meet these needs, software companies offer a plethora of solutions. Some are focused on a particular demand, while some work to pull everything together. Some companies provide only development tools, while others will organize individual embedded application developments from start to finish.

The emergence of low-cost, 32-bit embedded microprocessors and intellectual property (IP) cores has further moved software developers to add features to their products, further blurring the line between hardware and software develop-

ment. This is particularly the case in automotive, printer, and telecommunications applications. To address these applications, WindRiver Systems developed its Tornado environment, aimed at embedded systems. Its graphically oriented tools are taking the place of the many more primitive text-based approaches *(Fig 1)*.

Tornado comprises three major integrated components. They include a set of Tornado plug-in tools, a set of cross-development tools and utilities, and the VxWorks run-time system. VxWorks includes a range of host/target communications such as Ethernet, a serial port, and an in-circuit emulator (ICE). In addition to the Tornado tools, third-party tools can be brought into an integrated development environment (IDE). Tornado and all its components run within a graphical user interface (GUI) that functions on operating systems like WindowsNT, Windows 95 and several flavors of Unix.

Communication between the host-based development environment and the target takes place via a scaleable agent on the target. This agent provides the access for all tools through the host-based target server. The target server can serve on a host other than that containing the actual development tools.



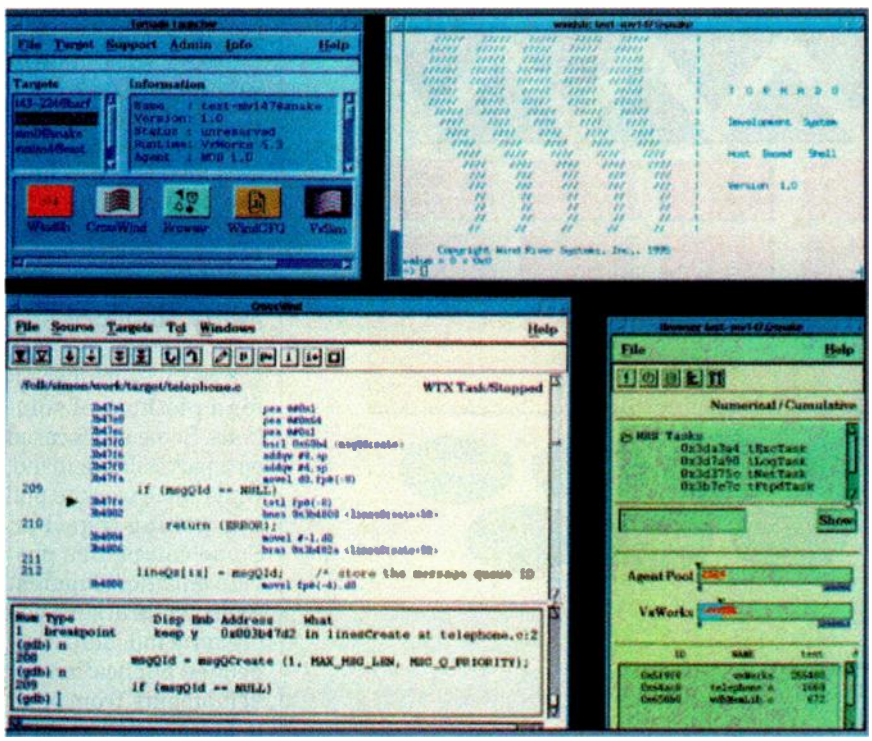
2. pRISM+, from Integrated Systems Inc., provides a complete graphical environment for embedded development. It includes a complete tool suite built for specific target microprocessors, and is built around the industry-standard CORBA bus to accommodate expansion to third-party tools.

The user communicates to the tools, which talk to the target server, and the server then establishes communication with the target via connection plug-ins, which are implemented as dynamic link libraries (DLLs). Connection plug-ins support specific types of target interfaces such as an ICE, a ROM monitor, or connection to the host-based simulator, VxSim.

Plug-In Interfaces

On the tools side, the WindRiver and third-party tools interface to the system via plug-ins that mediate between the specific tool interfaces and a published Tornado application programming interface (API). This means that any tool that's interfaced to Tornado can talk to any target for which there is a proper connection plug-in. In addition to the connection plug-ins, there are object-module-format plug-ins available that let tools interact with object formats for which they might not have been originally designed.

Among the tools available with Tornado are the GNU toolkit, that includes C and C++ compilers and a collection of supporting tools; WindRivers' CrossWind source-level debugger; a graphical source-code browser; and Windconfig, a target system configuration tool. Other tools available include the WindView run-



1. Tornado, from WindRiver Systems, is an integrated, cross-development environment for embedded systems. It consists of three major integrated components: a set of Tornado plug-in tools; a set of cross-development tools and utilities; and the VxWorks run-time system that includes the VxWorks real-time operating system, and a range of host/target communications such as Ethernet, a serial port, and an in-circuit emulator (ICE).

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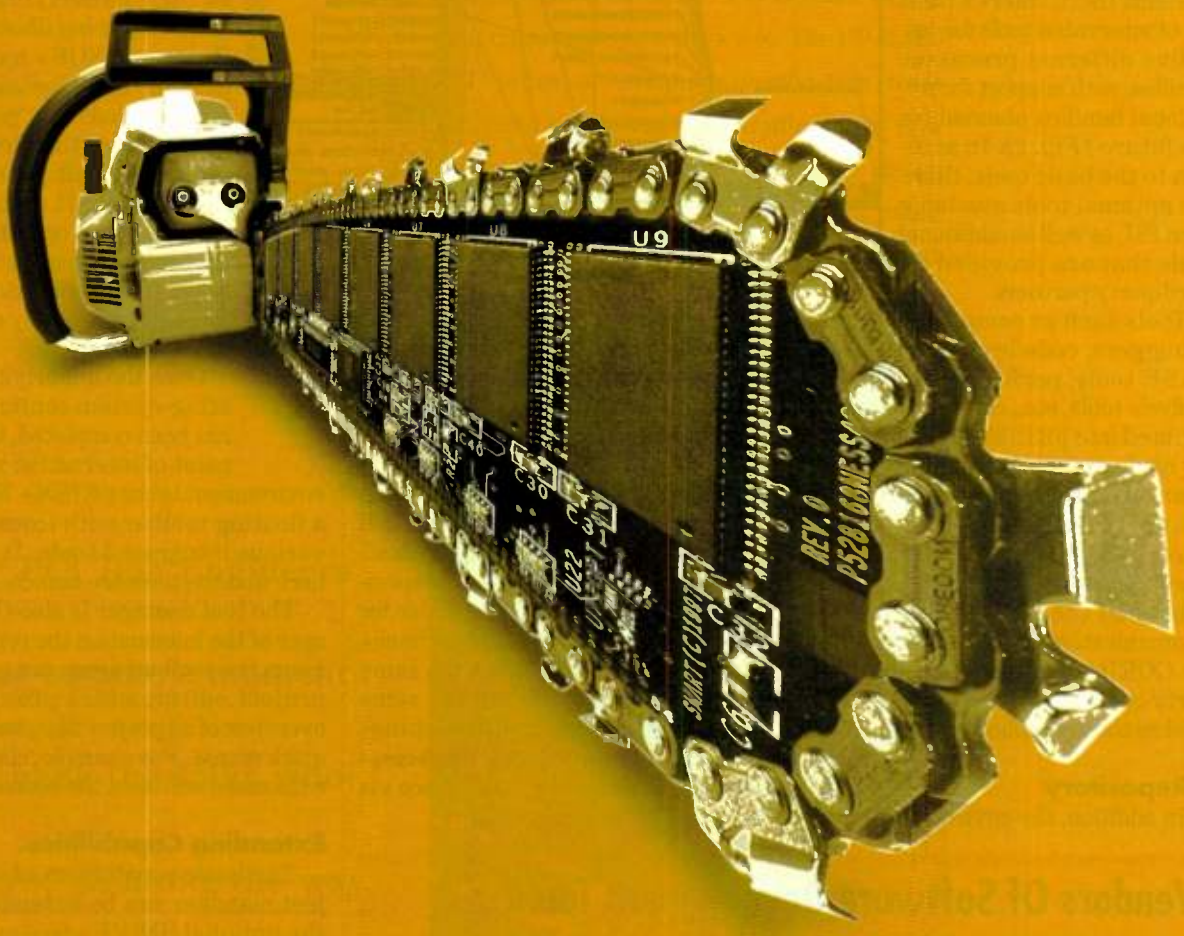

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ment tools provided can be replaced with other available tools such as ClearCase from Pure Atria, or PVCS from Intersolv.

The basic package of pRISM+ is delivered with the Wizard, the pRISM+ Manager/toolbar, a compiler, and a debugger for the target processor. The debuggers are kernel-aware, and ISI is attempting to supply its own products for the basic package wherever possible. For example, ISI's Searchlight debugger is supplied for the MIPS platform package, while the SingleStep debugger from Software Development Systems, Oak Brook, Ill., is supplied for the 68000-processor platform. This does not preclude the use of third-party debuggers that are pRISM+ compliant. An ARM compiler and debugger are supplied for the ARM package.

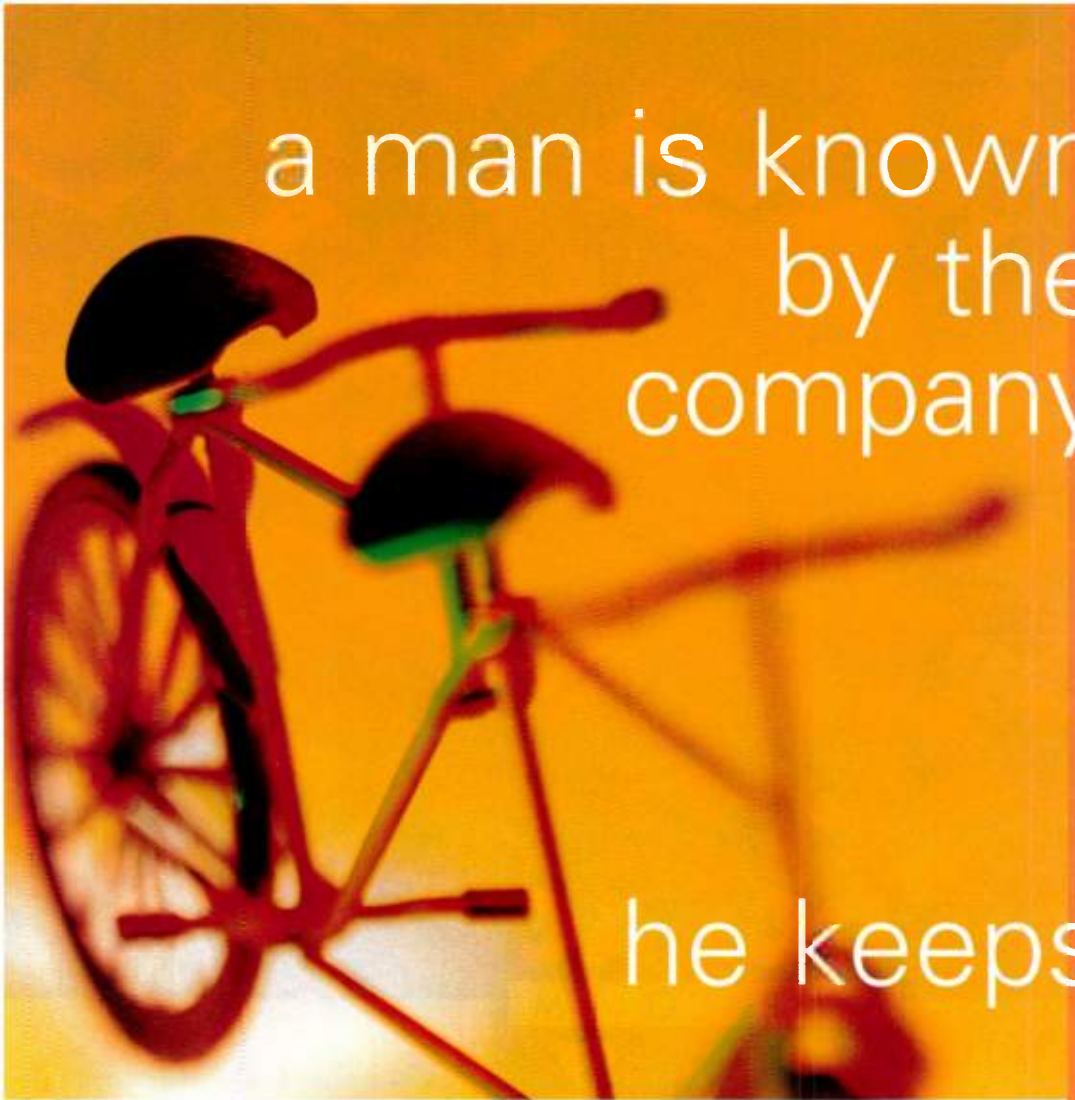
One noteworthy integrated environment of development tools is CodeWarrior Professional from Metrowerks Inc. designed for what t he company claims "serious, industrial-strength programming." CodeWarrior Professional allows one to edit, compile and debug C, C++, Java and Pascal programs for multiple target processors and operating systems.

Microsoft Developer Studio is an example of an IDE originally targeted for desktop application development, but increasingly used for embedded development as well. Many software development activities, such as writing and compiling code, take place initially in a desktop environment, therefore, the activities are generic to programming in general.

Developer Studio has the ability to easily integrate other Windows-based tools so that they appear to be natural menu items selected the same way as the features supplied by Microsoft. In addition to the Nucleus POWERplant, Phar Lap Software has integrated its Embedded ToolSuite into the Developer Studio. In fact, the Developer Studio look and feel is serving as an example to companies developing their own proprietary tools because it has become such a familiar environment for so many programmers.

The Web

Another area of concern for software integration is the porting of the



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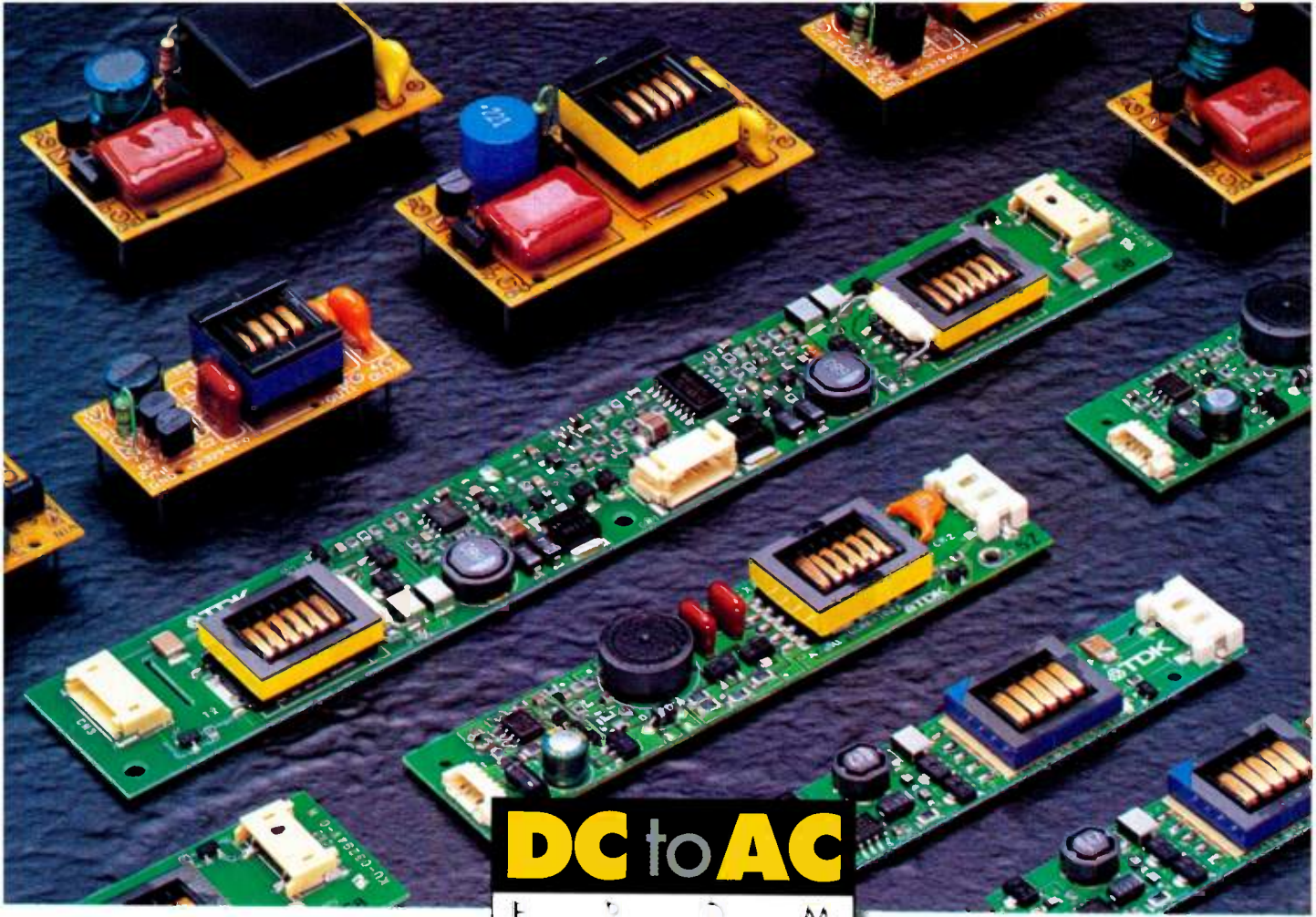

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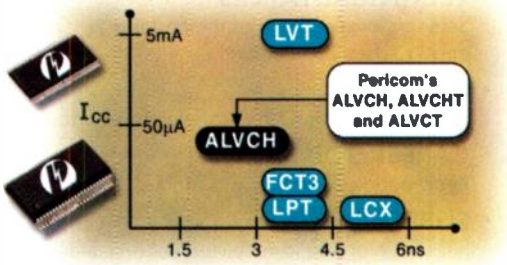

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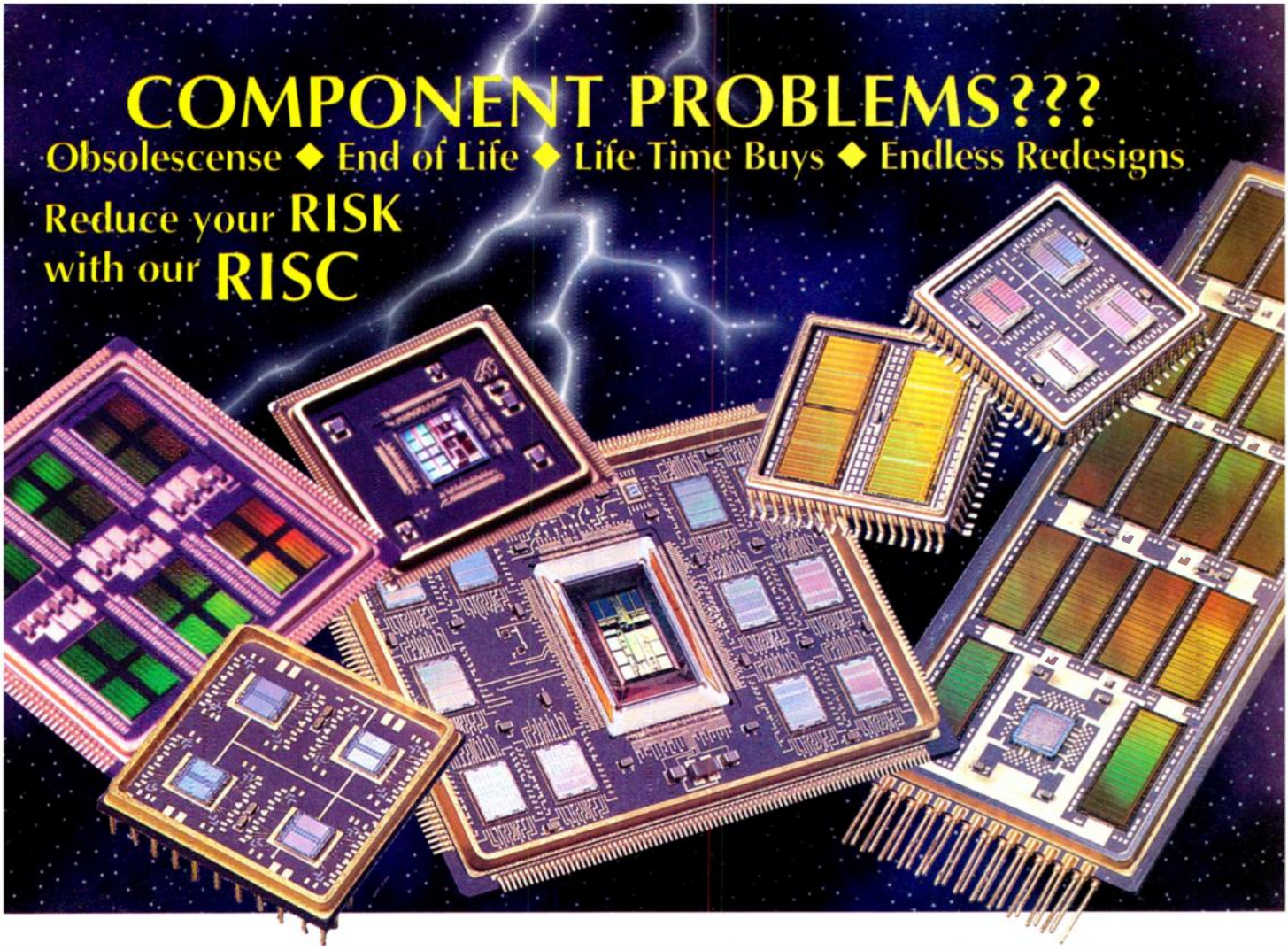
process through the growing web environment. This new area of software-change management must enable distributed and diverse web developers to function as cohesive teams. The web can be viewed as the largest and most complex embedded system in the world—and one that is growing phenomenally fast, without any review process, that now contains the core of many businesses' mission-critical applications. It may prove to be the greatest challenge in large-scale integration of development tools.

With that in mind, Continuus Software Corp. has introduced Continuus/WebSynergy, which supports the collaborative development, management, approval, and deployment of all types of web content and software. "Frequent changes by large, diverse teams are making it very difficult, if not nearly impossible, to ensure high quality while changes are being made at web speed," explains Dick Heiman, the research manager for application development tools at Continuus. "In large organizations, web teams can include software and content developers, webmasters, graphic designers, testers, as well as approvers," adds Heiman. The Continuus/WebSynergy product includes a content-client, task-based management suite for web teams with task-based web workflow, team coordination, and deployment.

Continuus claims that one of the Big Three automobile makers has an intranet application with some 20,000 web objects that are critical to the distributed development of vehicle controller software. Currently, about 100 engineers and designers use a variety of PC applications to create and submit content. The number of content developers is expected to grow to 10,000 or more in the next few years. By maintaining these standards of development integration, the flow of information in the design of automobiles can work without bottlenecks to slow down development, or collisions that could have serious or catastrophic consequences. This would be an excellent goal for all of today's embedded-system software developers.

Teri Sprackland is a contributing editor. She can be reached at (650) 728-2038; e-mail: 102175.1650@comuserve.com.



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SEPTEMBER

Embedded Systems Conference Europe, September 7-9. Royal Ascot, England. Contact Michelle Troop, Miller Freeman Inc., (415) 278-5229; mtroop@mfi.com.

Sixth European Congress on Intelligent Techniques & Soft Computing (EUFIT '98), Sept. 7-10. Aachen, Germany. Contact Conference Secretariat: EUFIT '98, Promenade 9, D-52076 Aachen, Germany; +49 2408-6969; fax +49 2408-94582; e-mail: eufit@mitgmbh.de; www.mitgmbh.de/elite/eufit.html.

ICSPAT & DSP World Expo, September 13-16. Toronto Metro Convention Center, Toronto, Ontario, Canada. Contact Liz Austin, Miller Freeman Inc., (888) 239-5563, (415) 538-3848, e-mail: dspworld@mfi.com;www.dspworld.com.

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Fourth International Symposium on Ultra-Clean Processing of Silicon Surfaces (UCPSS '98), Sept. 21-23. Oostende, Belgium. Contact Barbara Kalkis, Maestro PR, (408) 996-9975; fax (408) 996-8534, kalkis@compuserve.com.

Second International Conference on Evolvable Systems (ICES '98), Sept. 23-26. Swiss Federal Institute of Technology, Lausanne, Switzerland. Contact Andres Perez-Uribe, conference secretariat, +41 21-6932652; fax +41 21-6933705; e-mail: Andres.Perez@di.epfl.ch; lslwww.epfl.ch/ices98/.

IEEE Petroleum and Chemical Industry Technical Conference (PCIC '98), Sep. 28-30. The Westin Hotel, Indianapolis, IN. Contact David L. Johnson, Eli Lilly & Co., Lilly Corporate Center, DC 4121, Indianapolis, IN 46285; (317) 276-1717; fax (317) 276-9394; e-mail: david_lee_johnson@lilly.com.

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AT17LV256	256K x 1	3.3 V	No	In Stock
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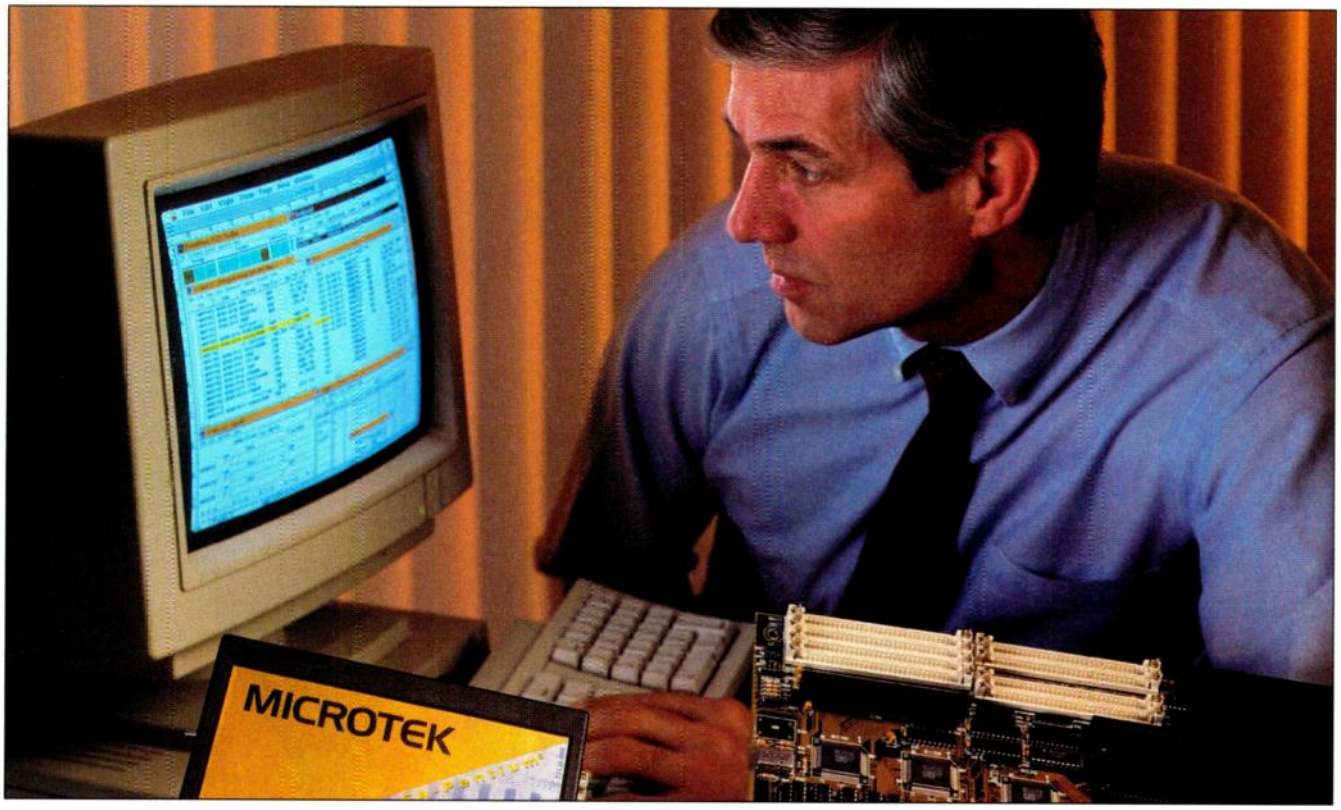
Dhrystone MIPS	347	415, 519
On-chip Debugging	JTAG boundry scan port, N-wire and N-trace functions	
Power Consumption	2.5W	3.5W, 4.4W
Multimedia Extensions	Yes	Yes



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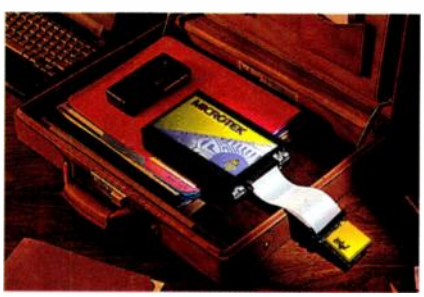

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ELECTRONIC DESIGN QUICK LOOK

Edited by Debra Schiff and Nancy Konish

MARKET FACTS

Help Desk Growth To Surge Through 2001

Growth is coming to the industry in what some would call an unexpected area—the help desk. While the help desk used to be a convenience for the company, or a selling point for customers, it's currently evolving into a necessity. The internal help desk generally serves to make computer processes run smoothly for employees, so that their time can be spent performing the tasks at hand, rather than on problems with the computer or its programs. If the help desk is proactive in its approach, it boosts internal productivity, while simultaneously allowing the company to reap the benefits of the information technology in which it invested. An external help desk, on the other hand, can be everything from a product information line to customer support. Due to its large volume of customer communication, it can actually become one aspect of the sales and marketing department. Companies have begun to see the advantages of help desks in revenue studies, which reflect substantial growth. From $7.9 billion in 1997, revenues have been forecasted to rise to $24.5 billion in the year 2004, with a compound annual growth rate of 17.6%. These numbers have pushed many companies into setting up a help desk system. Most start by using "software suites," which consist of problem solving software, such as spreadsheets, word-processing programs, and operating systems. The internal suite is generally aimed toward management issues, while the external should be directed at customers and consumer information. Another help desk possibility is outsourcing. Outsourcing allows companies to gain the technical support they lack via a third party. Whether the help desk is inside or outside the company, however, will not affect the expected rush to add help desks, as the rate of growth in the market is expected to peak in the year 2000. Growth is also forecast to steadily continue at a slightly lower rate (*see the chart*). Aside from this financial aspect, the focus is also on the shifts that will cause help desks to become necessities, such as cost reduction, and improvement in the quality of service. The help desks may also be restrained, though, by things such as cost. Companies may not invest in building their own help desks, and be unwilling to outsource them. There will be a certain amount of pressure on the help desks to stay ahead of consumers in terms of functionality. This will mean constant communication with customers, in addition to keeping up with the technology. Debate is also growing around the role that the help desk will play. Because everything is becoming centered around technology, it's very possible that the help desk will become the hub of the company, responsible for all information, and thereby erasing the need for any human resources. If empowered by its position as the center of the company, it will most likely rely on its strength—information technology. Usage would then go up, causing new tools to be created. Companies that offer help desk tools and software will most likely be lost in the shuffle as competition grows exponentially. Consumers may be confused, as so many choices leave them no opportunity to forge loyalty to one company. Limited growth may lead to eventual consolidation, most likely as smaller companies are enveloped by the top competitors. Until then, the help desks are still developing, and discovering ways to better serve the customer and employee. The help desk may help the industry at large as much as it helps individual companies. As more user-friendly information is made available, the average user may, for the first time, grow with the industry.

U.S. Forecasts for Help Desk Software Tools and Services

Year	Revenues ($ billion)	Revenue Growth (%)
1994	4.87	–
1995	5.66	16
1996	6.65	17
1997	7.86	18
1998	9.32	18
1999	11.11	19
2000	13.35	20
2001	15.81	18
2002	18.43	17
2003	21.27	15
2004	24.51	15

Compound Annual Growth Rate (1997 to 2004): 17.6%

Source: Frost & Sullivan

For more information, contact Rachel Putter at Silicon Valley, 2525 Charleston Rd., Mountain View, CA 94043; (650) 237-4947; fax (650) 903-0915; rputter@frost.com.—**NK**

JUST 4 THE KIDS

When I was a child, computers were those mysterious, monstrous machines that took up entire rooms and worked all day to answer a single question.

They were an amazing, yet unknown entity. I never would have even thought to touch such a marvel. As I've gotten older though, times have changed, along with computer technology. Today, children have the opportunity to work with computers on virtually a daily basis.

Most parents are thrilled with this, wanting to expose their child, early in the education process, to the wonders of the computer. But, at the same time, many are concerned about the potential for their child to damage such a high-priced piece of equipment. And, then there's the unsuitable information they might gain access to while surfing the web.

Offering parents a better option, Tiger Electronics, Vernon Hills, Ill.—best known as the maker of the Giga Pet—has developed two new electronic learning aids. These devices, the Headstart Computer and the Ultra Pack PC, are for children ages five to eight, and ages nine and up, respectively. Specifically designed as early learning tools to help introduce your child to the world of computers, they offer an inexpensive alternative to today's PC. For the child who has graduated to the PC or MAC, Tiger Electronics also offers an interactive CD-ROM called Lights Out 3D.

The Headstart Computer is based on a laptop design with a two-line, 12-character LCD screen. It has a raised QWERTY keyboard with movable keys and a built-in mouse, plus a retractable cord. The raised keyboard feature makes it more easily accessible to a child's small fingers.

Another feature of the computer is that it's memory can be expanded by simply adding an additional cartridge. And, for those of you concerned with safety, no cords are necessary; instead it uses four AA batteries.

MARIFRANCES WILLIAMS

The Headstart Computer is an interactive learning aid that can actually talk to the child. It has a spoken vocabulary of roughly 450 words that are used to encourage and direct the child as he or she plays different educational games.

The Headstart Computer features 30 activities in all that teach spelling, vocabulary, homonyms, memory building, math, definitions, counting, and rhymes.

The Ultra Pack PC also uses the laptop design, making it easy to take anywhere. It has a full-stroke qwerty keyboard, computer-like mouse, touch-sensitive activity selector pad, calculator, four-line LCD screen, and spell checker. Like the Headstart Computer, the Ultra Pack PC's memory can be expanded simply by adding cartridges. It requires six AA batteries or a nine-volt adapter for operation.

The Ultra Pack PC is also an interactive talking precomputer. It features 35 multilevel learning activities that increase in difficulty to match the child's growing skill level. With three levels of difficulty, children can actually pace their own learning progress, and transfer back and forth between levels at any time. With the Ultra Pack PC, the child learns such skills as spelling, vocabulary, verb tenses, grammar, and math in an entertaining and easy-to-understand way.

Both the Headstart and Ultra Pack PC precomputers are child-friendly, standalone learning toys that expose the child to the world of computers in a fun and educational manner. They teach keyboard smarts and give the child a heads-up in the classroom in a variety of different subject matters and computer technology.

If your child has already made it to the PC or MAC levels, Tiger Electronics suggests the CD-ROM called Lights Out 3D. This interactive CD-ROM features mind-bending puzzles with enhanced environments, animation, and state-of-the-art graphics. It runs on both Windows and MAC.

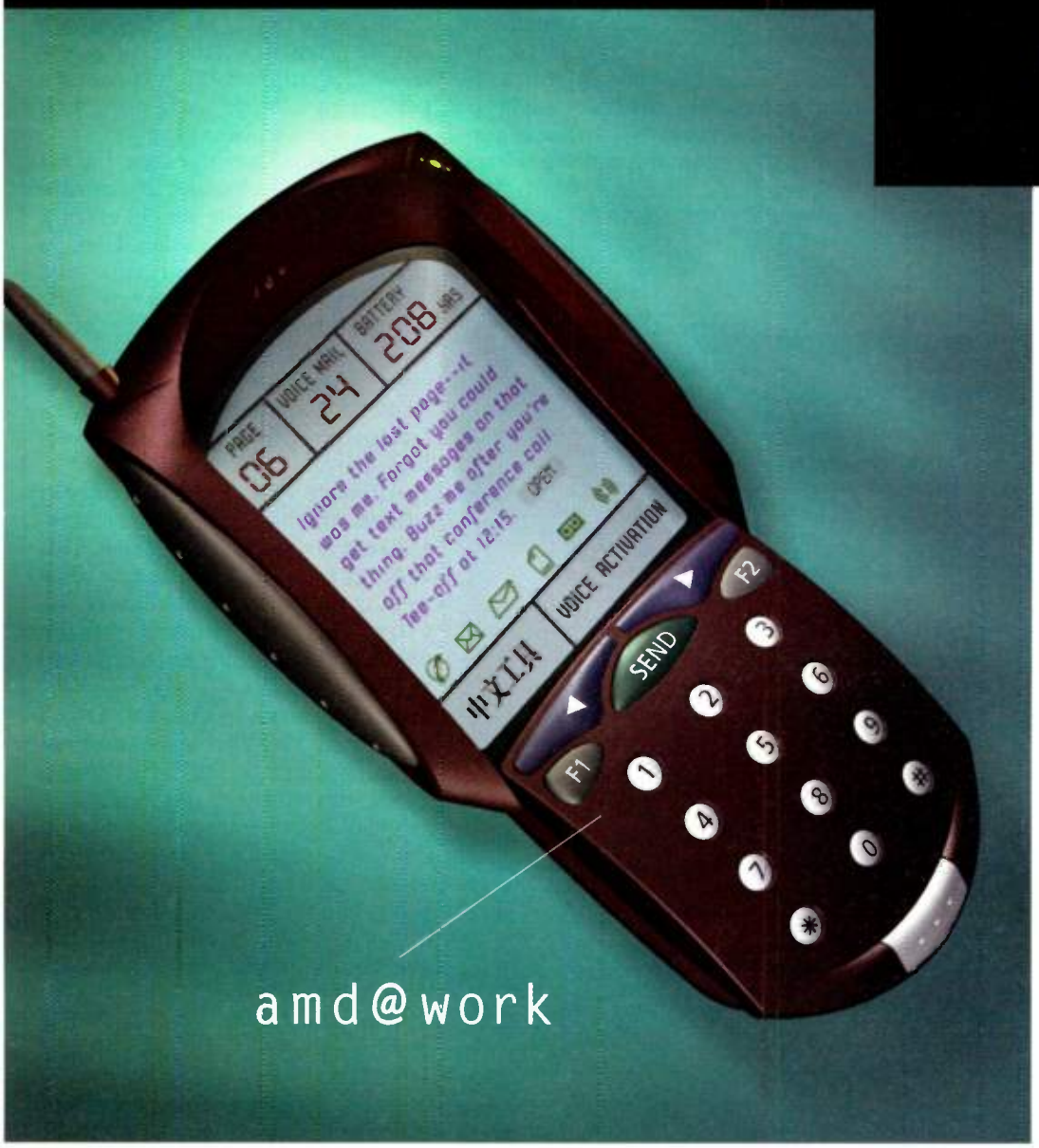
While the child plays a variety of games—Classic, Lit Only, Lights In, Toggle, Looping, Three Color, and Flipit—they are actually strengthening their higher-level cognitive thinking skills. These skills include the ability to infer, by developing strategies and using logic. Every educator works to help children develop such skills daily as they are taught science, math, and language arts. With the Lights Out 3D CD-ROM, the child learns these skills by having fun. In fact, often times they become so engulfed in the games that they don't even realize they are learning.

The Headstart Computer, Ultra Pack PC, and Lights Out 3D may be purchased at a variety of retailers and via the web at *www.tigertoys.com.*

The Headstart Computer costs $50.00, Ultra Pack PC is priced $89.99, and the Lights Out 3D CD-ROM wears a price tag of $34.99. For more information, contact Tiger Electronics, 980 Woodland Parkway, Vernon Hills, IL 60061; 847-913-8100.

Marifrances D. Williams holds a degree in Liberal Studies from San Diego State University, Calif. She is currently a fifth-grade teacher at Los Ranchos Elementary, San Luis Obispo, Calif. Williams specializes in the identification of advanced technology for the use of child-focused applications. She may be reached at williamsofsm@lightspeed.net.

Time to make a little low-power magic.



amd@work

The Am29SL800, the first 1.8V-only, read, program and erase flash device. Our flash family offers a number of product and packaging options—including chip scale packaging—from which to choose.

Full Function 1.8V Flash

While you're reshaping things with 1.8V, we'll be busy developing the first 0.9 volt flash device for a generation of products yet to come.

This remarkable Perpetua cell phone from Studio Red is not yet available. But the flash technology that's making it possible is here today. From AMD.

For a data sheet, packaging information and links to other Flash memory products, visit

www.amd.com/magic/

If you doubt the existence of magic these days, wait 'til you see what's possible with an advanced piece of silicon like the Am29SL800. This remarkable 8 megabit, 1.8-volt-only flash memory chip is your opportunity to develop exceptionally low-power designs with extended operating life and a myriad of features. (Thanks in no small part to our advanced power management system with zero-power operation.) Next-generation cell phones can now offer increased levels of talk and standby time long enough to exhaust the most conversationally-addicted. So what's the easiest way to begin making it happen? That's no trick at all. Simply call 1-800-222-9323 or visit our Web site.

AMD

www.amd.com

Talking Navigation System Hits The Road

By now we've all heard about global positioning satellite (GPS) based navigation systems. As many of you may remember, they grew in popularity after a rash of car jackings took place throughout the U.S. Without having to try to read a map while driving, these systems help travelers get where they need to go quickly, and prevent them from making a wrong turn into an unfavorable area.

It's hard to dispute the benefits of such a system, but they have one drawback; they require you to take your eyes off the road to read directions on a screen. While this is certainly better than fumbling with a map, it still presents a hazardous driving condition. A new device from IVS Inc., Monrovia, Calif., promises to eliminate this hazard through its Avstar product; a hands-free, eyes-free, transportable, interactive voice-navigation device, for use with both cars and trucks.

Avstar gets its power from the vehicle's cigarette lighter. To operate the system, the user simply gives it an origin and a destination. Using a CD-ROM map of your particular city, it determines the fastest route. Origins and destinations may be given as an address, intersection, or landmark. The information is then related back to the user, on demand, through a series of turn-by-turn verbal commands.

Although Avstar can be enhanced with an optional GPS antenna and receiver, it does not require them. This added functionality will simply allow Avstar to automatically determine your point of origin, and provide warning signals for next-turns and the destination.

Avstar can understand what you say by digitizing your voice and identifying word patterns. The loudness, speed, and pitch of your voice are irrelevant because they don't change the words' meanings. Once the word patterns are found, Avstar compares them to patterns for other words that make sense in response to the question, and picks the one most like what you asked.

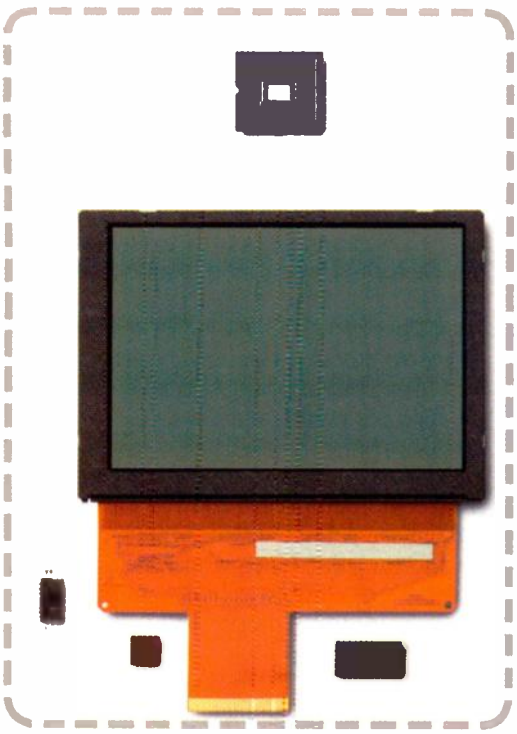
The main advantage of Avstar is that because it does not use a display screen, the user's eyes never leave the road. It does have one drawback though; it requires you to spell out street names. But don't despair, even if you *can't* spell, Avstar has a special spelling corrector to fix any errors you might make.

Avstar is now available and sells for approximately $1000; $1500 with the GPS option included. Each purchase comes with one CD-ROM map. Additional maps sell for roughly $29 to $39. It can be purchased at auto dealerships or through the company's web site at www.ivs.com.

For more information contact IVS at (626) 359-1318.

Cheryl Ajluni

Sharp's skills in performance integration can connect you to the best in packaging solutions.



Tomorrow's idea of a phone booth will be a lot less confining, that's for sure. Even today, Sharp's latest wave of components and integration know-how can open up a new, direct line to your next-generation devices. You can couple our seasoned integration capabilities with components like these:

***New 1/5" CCD sensors** require just a single 5V power supply, allowing digital cameras to be made smaller and lighter—with up to 30% fewer components.*

***Super Mobile, Highly Reflective TFT-LCDs** in 2.5", 4", 6.5" and 8.4" sizes are half the weight, one-third thinner and use just one-seventh the power of conventional LCDs.*

***Bi-directional IR data links** offer data transfer rates of up to 75Kbps, supporting the use of multiple input devices—up to eight at a time.*

***Flash memory** options include Stacked-Chip Flash, combining two different memory die in one space-saving package, and NextGen™ Boot Block Flash in Sharp's unique Chip-Size Package.*

*For technical information about these and other Sharp components, visit our web site at **www.sharpmeg.com** or call **1-800-642-0261**, Ext 920.*

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READER SERVICE 156

Taking Stock

If you're keeping an eye out for new services in the industry, check out Associated PartStock, a program of Associated Distribution Logistics (ADL). This program consists of a large network of parts depots in the U.S., North America, Europe, and the Far East.

Clients use these storage locations to create their own network of parts distribution facilities. The convenience of Associated PartStock is that it is customized.

To create a network, you choose your depot locations. There are no stipulations for the number of depots that customers use, or the locations of the depots. You then define your shipping needs. Options include surface and air transportation, as well as use of air-ride vans and lift-gate trucks for heavier equipment.

If you're steadily swamped, you might want to try ADL's inventory program. The fully computerized depots log transactions and organize account reports. This system, which is accessible via computer, also ensures that your parts are in stock, and ready to be delivered.

The latest ADL innovation is the "swap-out service," which allows you to completely swap out components and products at any U.S. or overseas location. One of the companies that uses this service is Panasonic.

For more information, contact Associated Distribution Logistics, 3333 New Hyde Park Rd., New Hyde Park, NY 11042, (800) 443-3443, fax (516) 627-8915, or contact their web site at www.agsystems.com/partstock.—**NK**

TIPS ON INVESTING

The following is a lesson on the Education IRA—a new government giveaway to help educate our children.

Education costs: Education costs have typically risen two-to-three times the rate of inflation.

Decrease in financial aid: More students are seeking financial aid—76% in 1996, compared to 66% a decade ago. While the top students will no doubt be able to get into a desirable school regardless of their ability to pay, many of the "average" students will be expected to pay a higher percentage of their college bill if accepted into those same schools.

Unparalleled salaries: A college education is one of the greatest investments you could make. The U.S. Department of Labor notes that in September 1997, the average annual income of a college graduate was 50% greater than that of someone with a high-school diploma.

HENRY WIESEL

College aid: More than $55 billion was available to college students in 1996-97 from federal, state, and institutional sources. After inflation, this is 70% higher than a decade ago. However, two-thirds of this increase in financial aid was in the form of loans rather than grants. Furthermore, most of the increased borrowing is unsubsidized; e.g., the government no longer pay the in-school interest.

Accelerated growth: Unlike a regular savings account where you pay taxes on your earnings every year, in an Education IRA, your earnings grow free of taxes, allowing your funds to benefit from compounding of interest and dividends over time.

Tax-free earnings: All distributions are excluded from gross income if funds are used to cover qualified higher education expenses of the beneficiary.

Incentive: There is a strong incentive to use the money saved in an Education IRA for education purposes because a 10% penalty will be assessed, as well as ordinary income taxes, on the earnings portion of the distribution if used for noneducational purposes.

Other family members: If funds in an Education IRA are not used by the original beneficiary before age 30, the account can be transferred tax-free to an Education IRA benefitting another family member.

No minimum, $500 maximum: Your savings schedule is flexible with an Education IRA. You can contribute up to $500 annually for each child, or nothing at all, the choice is yours.

Investment decisions: The account holder of the Education IRA is in control of the funds contributed for a child.

Relative or friend, anyone can contribute: Full contributions are allowed for single filers whose Adjusted Gross Income (AGI) is under $95,000 and for joint filers whose AGI is under $150,000. If you are not eligible to make contributions, someone else can contribute on the child's behalf, i.e. grandparents, birthday presents, etc.

Annual contributions add up fast: Annual contributions must be made by December 31 of the contribution year.

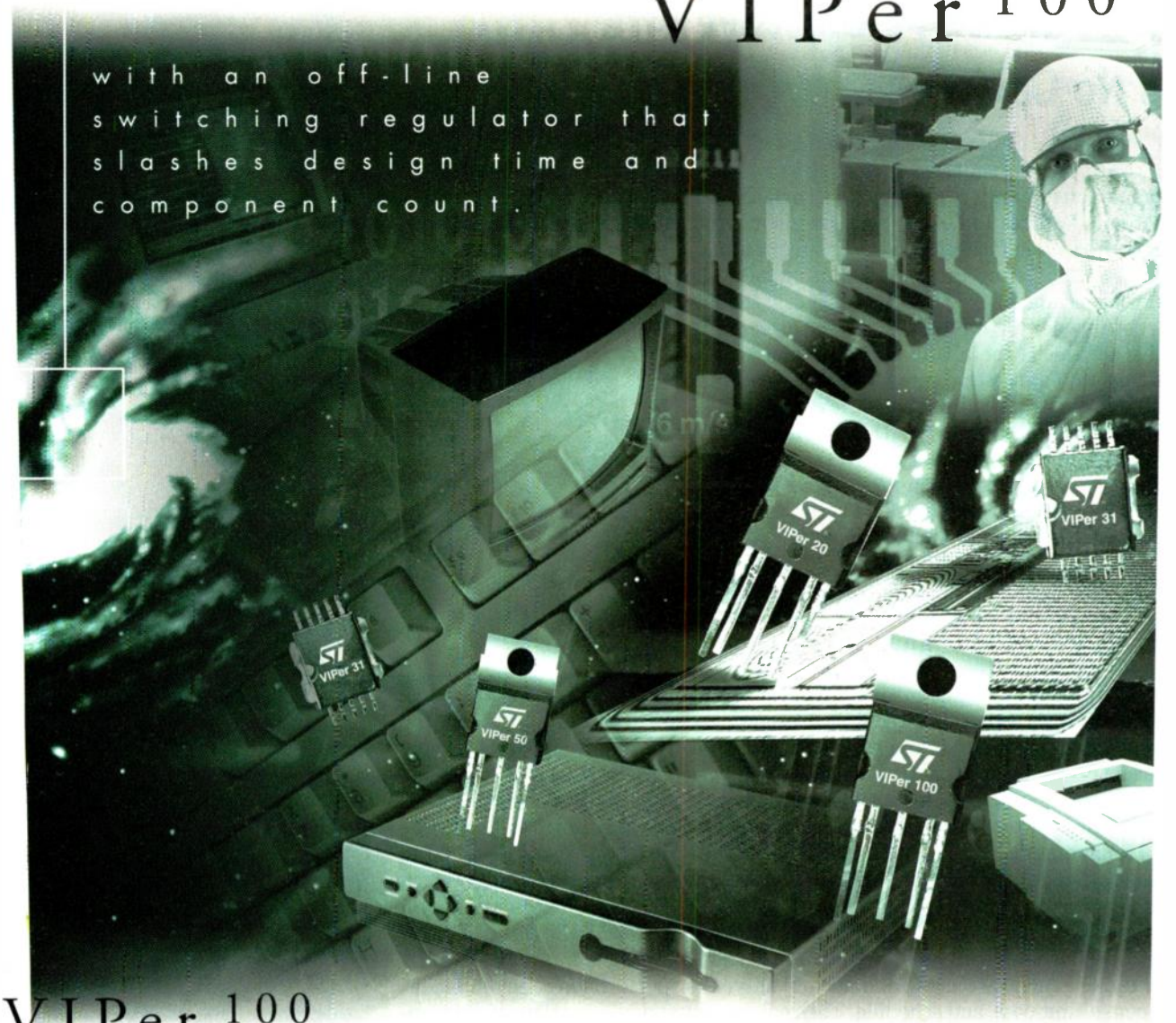
For free information, brochure, and help setting up an Education IRA for children, grandchildren, or a child you care about, contact Henry Wiesel at the address or phone number listed below.

Henry Wiesel is a vice president of investments, financial consultant, and qualified pension coordinator with Smith Barney. He may be contacted at 1040 Broad St., 2nd Floor, Shrewsbury, NJ 07702; (800) 631-2221, ext. 8653.

shaping technology

VIPer 100™

with an off-line switching regulator that slashes design time and component count.



VIPer 100

Thanks to ST VIPer100 (Vertical Integrated Power energy regulator) technology, SMPS designs are really shaping up. By combining an optimized, high voltage, avalanche rugged Vertical Power MOSFET with state-of-the-art PWM circuitry, VIPer100 family devices simplify and streamline AC to DC conversion — and actually cut component count in half. Printers, digital satellite receivers, auxiliary power supplies and more can now get to market faster and more economically. So why not let ST VIPer100 devices help you shape technology? For comprehensive literature plus information on interactive application design software and low-cost development kits, fax 781-259-9442 and visit us on the web at www.st.com.

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SHAPING TECHNOLOGY

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READER SERVICE 142

MANAGING THE DESIGN FACTORY

More Than One Objective Is No Objective

Long ago, in an age when an engineer still knew what a slide rule was, I went to Harvard Business School to get my MBA. I was fresh out of the Navy, and awed by my brilliant professors. In one course, a professor quoted a statement attributed to Texas Instruments, which asserted that, "More than one objective is no objective." It sure seemed pretty wise, at the time. As years went by, I saw companies diluting their efforts with too many objectives, and often remembered this quote...it still seemed pretty wise.

Only recently have I begun to think somewhat more carefully about whether this is useful advice. For example, most of us would agree that our businesses are interested in making profits. That's the easy part. Unfortunately, more than one thing affects profits. Our wise quote suggests that we should seek out the factor that has the biggest single impact on profits, and focus only on that factor. Any other objectives would only dilute our attention.

DON REINERTSEN

Beam me down to the real world! Since when could we focus a development program on a single objective? Consider a project targeted to achieve a gross margin of 60%, with an introduction date of July 1st. Which of these should be our "one" objective? "Say Boss, I've got good news and bad news. The good news is that the product will be done on time. The bad news is that the profit margin is zero." In reality, profit is an objective that is affected by many variables. If only one factor influenced profit, we could optimize that single factor. When more than one factor affects profits, we will ultimately confront trade-offs between these factors. To make trade-offs, we need trade-off rules.

Management isn't about choosing objectives at all. It's about developing trade-off rules. All complex tasks, like development programs, require such trade-off rules. It is fine to have more than one objective, as long as you have a rational way to make trade-offs between these objectives. To do this, you must be able to measure all objectives with the same yardstick: impact on profits. All development projects will have objectives for performance, development expense, unit cost, and schedule. The real art of managing consists of developing trade-off rules to balance these objectives.

For example, assume a low-cost vendor became available for your project, but using this vendor would delay the project. Should you utilize the vendor or not? You can make this decision rationally, but only if you quantify the financial effect of a unit cost reduction versus a schedule delay. The good news is, with a couple of hours of analysis, you can develop a set of trade-off rules which enables you to make such decisions quickly, and reliably.

You may have been lucky enough to get by without such trade-off rules in the past, but this is unlikely in the future. You will increasingly confront competent competitors who understand their economics. If you don't know how to manage multiple objectives, you will be forced to pursue the objective of the month. Your people will be puzzled, because you are constantly shifting your focus. Ironically, your supposed single-mindedness will cause you to hop from one objective to another. It's better to learn how to make systematic trade-offs between multiple important objectives. Being focused really doesn't mean that you must have only one objective. If you know how to make trade-offs, you will be ready to live in the real world, where we have to do more than one thing well.

Don Reinertsen is president of Reinertsen & Associates, a consulting firm specializing in product development management. He can be reached at (310) 373-5332 or e-mail: DonReinertsen@compuserve.com.

Y2K In Court

The Year 2000 Legal Coalition is working to protect you. From what? Think lawsuit...then imagine the implications of the Y2K lawsuits that have already been filed. The estimated price for settling these suits is climbing toward the $600-billion mark.

The Coalition's founding members are manufacturing, business, and technical individuals. They are the chief preponderants for Assembly Bill 1710, California, which was created to protect companies from frivolous date-change lawsuits.

Companies are covered by this bill as long as they aggressively inform their customers of updates and methods which make programs and systems Y2K-compliant. They also must offer free updates of off-the-shelf, Y2K-compatible software. By complying, companies earn "reasonable protection." They should be exempted from exploitive lawsuits claiming fraud, negligence, or unfair competition and business practices.

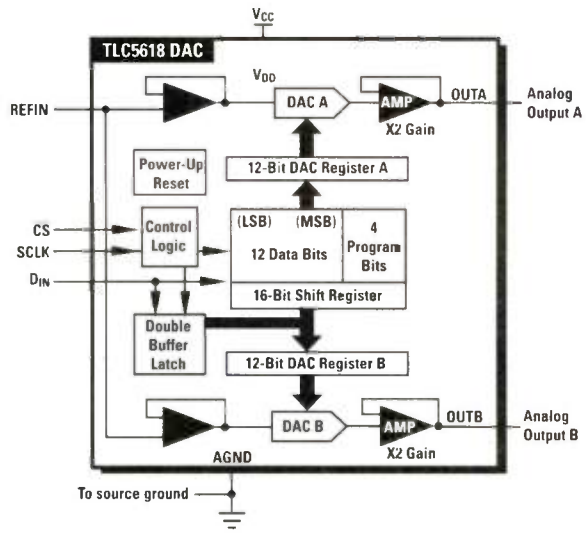
In contrast, if a company makes no effort to deal with this issue, Assembly Bill 1710 offers no protection. The bill does not shield any company from claims of bodily injury due to a computer date failure. It also will not affect agreements establishing responsibility for software performance problems.

The bill will go into effect January 1, 1999. The Coalition hopes that this earlier date will give companies more time to provide comprehensive software updates and information. Its greatest benefit is that it motivates companies to produce user-friendly, date-change material.

By utilizing this material, individual users and smaller businesses can also make an easier transition into the year 2000. The point of the bill is to protect and help industry users universally, not to support only the larger, more technical companies.

For more information contact The Year 2000 Legal Coalition, 1201 K St., Suite 1150, Sacramento, CA 95814, (916) 443-4900; fax (916) 443-4306; or visit their web site to see an on line copy of Assembly Bill 1710 at www.actr.com/actr/y2k.—**NK**

FIRST PROGRAMMABLE, DUAL 12-BIT SERIAL DAC IN AN 8-PIN PACKAGE.



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The TLC5618 starting at only $6.22*

- *Programmable settling times of 2.5 µs (fast mode) and 12.5 µs (slow mode) to 0.5 LSB*
- *1.21-MHz update rate (@ 20 MHz SCLK)*
- *Low power consumption of 3 mW (slow mode) and 8 mW (fast mode) with separate programmable power-down mode to 1 µA*
- *3-wire serial interface*
- *5-V single-supply operation*
- *8-pin SOIC package*

**Price is per device in quantities of 1,000.*

The TLC5618, TI's programmable, dual, serial input voltage-output 12-bit DAC, lets you select and specify the right performance level for your multiple DAC applications. Plus it clocks to 20 MHz, resulting in a 1.21-MHz update rate over a 3-wire serial interface for easy connection to DSPs. So whether you need high-speed or low-power performance, TI's 12-bit DAC lets you optimize your design.

For free data sheets, samples and product information, contact us at:
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1830-97R

MIXED SIGNAL & ANALOG

TEXAS INSTRUMENTS

READER SERVICE 178

Do-It-Yourself Compact Disks

Do you ever find your children or friends fighting over a music CD to determine who has the right to listen to it on their own CD player? Or have you ever wished you could take your favorite tracks from several CDs and combine them in just the order you wanted on a single CD? Thanks to Philips Consumer Electronics, Atlanta, Ga., you can.

Recently, Philips released the first home music-CD recorder that can use either write-once or rewriteable CD disks. It allows you to add your own audio from tapes, broadcasts, records, or other media; or copy full CDs or selected tracks to the blank CD, while maintaining the CD audio quality.

The CDR 870 recorder system connects to your existing audio sources—both analog or digital—and lets you record a CD by pressing a few buttons. The resulting CDs can be played on any CD player.

Inside the CDR870, the company incorporates its 1-bit SAA 7366 analog-to-digital converter (ADC), the TDA1315 optical input, and TDA 1305 continuous-calibration digital-to-analog converter (DAC). Housed in 435- by 310- by 75-mm cabinet that weighs 4 kg, the CDR 870 consumes just 15 W.

The entire system comprises three main circuit groupings: a playback path that is essentially similar to a conventional CD player's, an additional recording path, and the CD-R/CD-RW mechanism. The playback path transfers the digital signal data from the readout unit (laser, optics, and mechanism) to the decoder, where the decoding, and if required, error correction are performed. Information is supplied to the display by the coordinating host microprocessor that controls all internal operations.

The recording path is then followed by an encoder. Digital inputs bypass the converter, but do go through a sample-rate converter so that recordings made with different sampling rates (15 to 56 kHz) can be converted to the sampling rate used by the CD. The CD-R/CD-RW mechanism has a higher-power laser than conventional CD players to provide the write and erase capabilities. The mechanism can perform very precise tracking, particularly during recording.

Included in the CDR 870 are both the serial-copy management system (SCMS), and the recorder-unique identifier (RID) features that prevent the unit from making multiple generation copies from copyright-protected originals. The systems, however, do allow users to make single copies for personal use. Disks used for audio recording must bear the appropriate audio logo to ensure that levies are collected and payed to the relevant copyright protection associations.

The SCMS status of the original is indicated by a copy bit present on an original CD, and is placed on a recording at a frequency of 75 frames/s. For originals that are subject to copyright protection, the copy bit is continuously on; conversely, recordings that have no copyright restrictions have the bit continuously off. A copy of the original disk has the copy bit toggled between the ON and OFF states every five frames. The SCMS scheme can thus distinguish between three scenarios: copyright free originals that have no copying restrictions, normal copyrighted material, and SCMS "originals" (copies of copyright-protected originals).

The RID feature is a 97-bit code that is recorded every 100 frames on all disks made with the CDR 870. Included in the code is a brand-name identifier, a type number, and the drive number that uniquely identifies the equipment on which the disk was recorded.

In addition to the main system unit, the $649 suggested list price includes a remote control, audio cables, and a digital coaxial cable. Check with your local audio stores for availability or contact Philips at (770) 821-2400.

Dave Bursky

Say Cheese...

Want to show off those embarrassing photographs at family functions? It just got easier. With Toshiba's Smart Media card, which will be featured in the new digital still cameras from Fujifilm and Olympus, you can hook your camera up directly to your television.

SmartMedia, or the Solid State Floppy Disk Card (SSFDC), is the thinnest small-form, factor-storage in the industry at 45 by 37 by .76 mm. It consists of a NAND flash, electrically erasable, programmable read-only memory chip. It provides fast write, erase, and high-speed read functions.

For applications requiring small form-factor storage, flexibility, and cost-efficiency, you may want to try SmartMedia for nonvolatile memory. Its density ranges from 2 to 16 Mbytes. With a 3.5-in. floppy disk adapter, or a PCMCIA card adapter, you can work on portable PCs or consumer electronics. The user-friendly adapters also facilitate the quick data transfers.

Fujifilm's MX-700 is the smallest digital camera in the world. By utilizing the SmartMedia Floppy Disk Adapter (FD-A1), you can make your MX-700 PC-compatible. The adapter package includes Adobe PhotoDeluxe 2.0 image-editing software, and serial cables and data transfer software for Windows and Macintosh.

Olympus' 36-mm D-340L also lets you record images on the VCR. By using the Olympus P300 dye-sublimation printer, you can even process your prints. The D-340L comes with a 3.3-V, 4-MByte SmartMedia card, Adobe Photoshop Deluxe 2.0, InMedia Slides, Sound Plus 2.0, and image panorama software.

Toshiba plans to double the card's density each year, so plan on 1 Gbit in 2001. To find out more, contact Toshiba America Electronic Components, Inc., 9775 Toledo Way, Irivine, CA 92718, (714) 455-2000; or visit their web site at www.toshiba.com/taec.—**NK**

REFERENCE

ANALOG DESIGN SOLUTIONS

Data Sheets • Applications Notes • Free Samples

NEW

Low-Noise References Guarantee 1ppm/°C Tempco

2.5V, 4.096V, and 5.0V References Limit Noise to Only 2.8μVRMS*

Maxim's MAX6325/MAX6341/MAX6350 precision references use a low-power temperature-compensation scheme to achieve the excellent temperature stability normally found in costly, power-hungry heated references.

- **1ppm/°C Maximum Tempco**
- **0.02% Initial Accuracy**
- **Low, 1.8mA Quiescent Supply Current**
- **1.5μVp-p Noise (0.1Hz to 10Hz)**
- **±15mA Source/ Sink Current**
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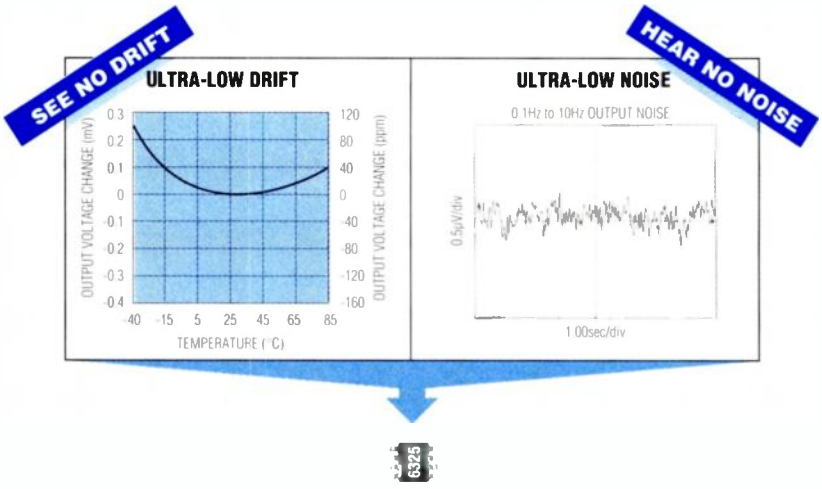

PART	TYPICAL OUTPUT VOLTAGE (V)	MAXIMUM TEMPCO (ppm/°C)	INITIAL ACCURACY (%)	MAX NOISE* (μVRMS)	OPTIONAL NOISE REDUCTION & VOLTAGE TRIM	PRICE** ($)
MAX6325	2.5	1.0	±0.04	2.8	Yes	6.70
MAX6341	4.096	1.0	±0.025	4.0	Yes	6.70
MAX6350	5.0	1.0	±0.02	5.0	Yes	6.70

* 10Hz ≤ f ≤ 1kHz **1000 pc price, FOB USA

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ANALOG DESIGN SOLUTIONS

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9	D/A Converters
10	Display Drivers
11	Voltage References
12	3V Analog

MAXIM

Low-Cost Micropo

Low-Dropout 3-Terminal References Guarantee 50ppm/°C

2.5V, 4.096V, 4.5V, 5.0V, and Adjustable (1.23V to 12.4V) Outputs

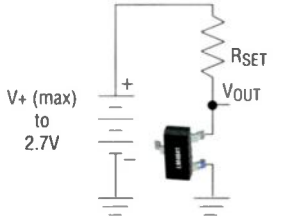
Maxim's family of low-cost, micropower, microsize, three-terminal voltage references features temperature coefficients of less than 50ppm/°C (15ppm/°C typical) and ultra-low dropout. Output voltages are 2.5V (MAX6125), 4.096V (MAX6141), 4.5V (MAX6145), 5.0V (MAX6150), and adjustable in the range of 1.23V to 12.4V (MAX6160) with initial accuracies of ±1%.

LOW DROPOUT

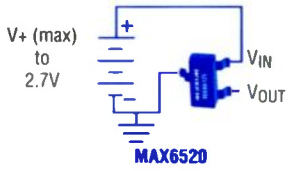
An ultra-low, 200mV minimum dropout voltage and very low quiescent supply current of only 75µA make these references ideal for 3V or 5V systems in portable and battery-powered equipment. In addition, unlike two-terminal (shunt/zener) references that waste battery current and require an external resistor, the MAX61xx family's supply current is virtually independent of input voltage variations, thus extending battery life.

The MAX6160 is available in a space-saving 4-pin SOT143 package, as well as an 8-pin SO. All other products in this family are available in 3-pin SOT23 and 8-pin SO packages.

TYPICAL SHUNT REFERENCE WITH EXTERNAL RESISTOR



OR . . . NO EXTERNAL RESISTOR!



SOT23-3
2.5mm x 3.05mm

SOT143
2.5mm x 3.05mm

Choose the Ideal SOT23 Re

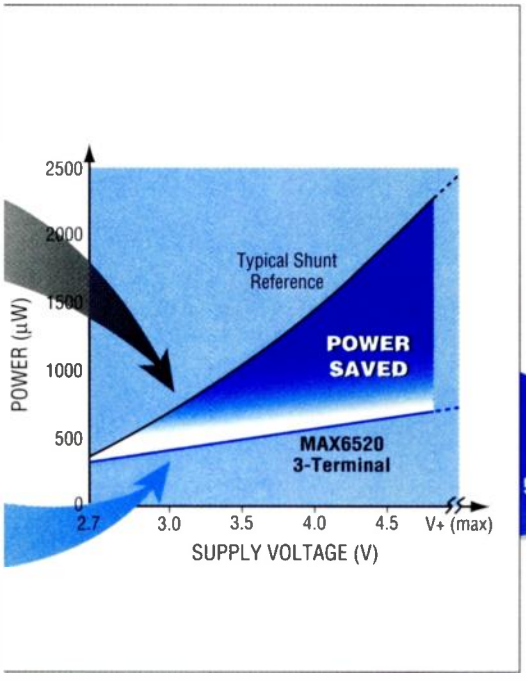
1.2V • 2.5V • 4.096V

PART	OUTPUT VOLTAGE (V)	SUPPLY CURRENT (µA, typ)
MAX6120	1.2	50
MAX6125	2.5	75
MAX6141	4.096	78
MAX6145	4.5	79
MAX6150	5.0	80
MAX6160	Adj. (1.23 to 12.4)	75
MAX6520	1.2	50

wer SOT23 Family

1.2V 3-Terminal References Guarantee 50ppm/°C and 100ppm/°C Tempcos

Less than 70µA Supply Current, Regardless of Input Voltage



Maxim's family of low-cost, micropower, SOT23, 1.2V three-terminal references features temperature coefficients of less than 50ppm/°C (25ppm/°C typical) for the MAX6520 and 100ppm/°C (30ppm/°C typical) for the MAX6120. These devices are the lowest power references available in space-saving SOT23-3 packages, making them ideal for battery-powered equipment in which space and power conservation are critical.

Existing two-terminal shunt/zener references require a series resistor to set the minimum current that flows through the load and the reference. As a result, two-terminal references waste valuable battery current. Because of the MAX6520/MAX6120's three-terminal architecture, the external set resistor is eliminated and the supply current is virtually independent of input voltage variations, maximizing efficiency at all battery voltages.

LOW COST
50ppm/°C and 100ppm/°C

ference for Your Application

• 4.5V • 5.0V • Adj.

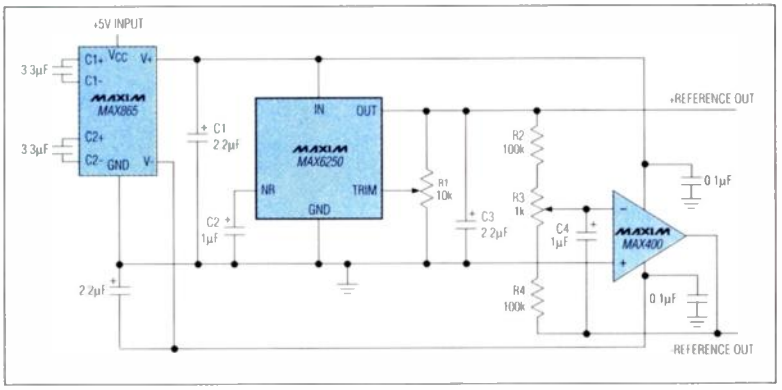
SOT23-3
2.5mm x 3.05mm

VOLTAGE DRIFT (ppm/°C, max)	SUPPLY VOLTAGE (V, min)	PACKAGE
100	2.4	3-pin SOT23
50	2.7	3-pin SOT23
50	4.3	3-pin SOT23
50	4.7	3-pin SOT23
50	5.2	3-pin SOT23
100	2.7	4-pin SOT143
50	2.4	3-pin SOT23

MAXIM

Ultra-Low-Noise, Low-Cost, Precision Voltage References *Guarantee* 2ppm/°C

. . . and ±0.02% Initial Accuracy, Only 1.5µVp-p Output Noise



Both a +5V and -5V precision reference can be obtained from a single, unregulated +5V supply. A MAX681 generates approximately ±9V to operate the MAX6350 reference and MAX400 inverting amplifier. The +5V is inverted by the ultra-low-offset MAX400 op amp.

For applications that require ultra-low noise and extremely low temperature coefficients, Maxim offers the MAX62xx family of precision voltage references. Excellent line/load regulation and low output impedance at high frequencies make them ideal for high-resolution data conversion systems up to 16 bits, such as instrumentation and medical equipment. These references use a buried-zener technology that enables a very low output noise level of only 1.5µVp-p (0.1Hz to 10Hz).

Maxim's MAX62xx reference family exhibits the ultra-low tempcos (1ppm/°C typical, A grade) normally associated with more costly and power-hungry heated voltage references, while consuming only 18mW of power.

Output voltages are fixed at 2.500V (MAX6225), 4.096V (MAX6241), and 5.000V (MAX6250), with initial accuracies of ±0.02% (A grade). Each reference guarantees 5ppm/mA load regulation while sinking or sourcing up to ±15mA. All devices have optional external voltage trim and noise reduction pins, and are available in 8-pin SO packages.

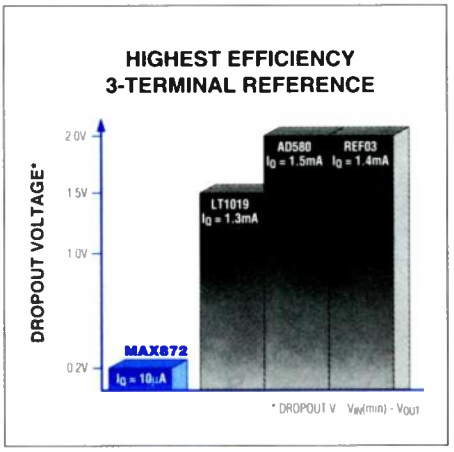
Micropower 2.5V Reference Operates from 2.7V Supply

Consumes <10µA, Regardless of Input Voltage

The MAX872 is the *only* three-terminal precision voltage reference guaranteed to regulate from a supply voltage as low as 2.7V. The precision 2.5V ±0.2% output voltage makes it ideal for 3V battery-powered systems. It is the lowest power three-terminal voltage reference available, consuming less than 10µA supply current independent of input voltage.

The MAX874, with a 4.096V output voltage guaranteed from an input as low as 4.3V, is designed for 5V micropower applications. The MAX874 consumes only 10µA, regardless of input voltage.

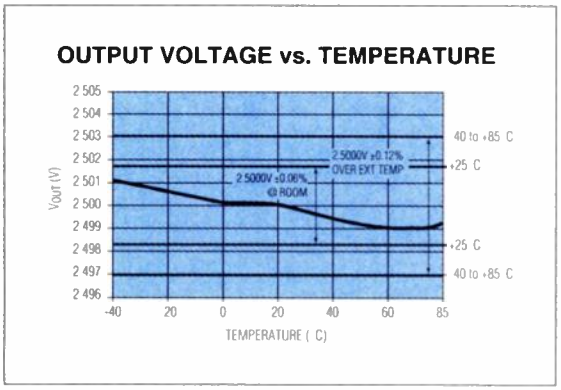
Load regulation for both devices is 500µV/mA when sourcing and 400µV/mA when sinking, so stability is guaranteed regardless of load—unlike two-terminal "zener diode" references.



Unlike other three-terminal references, the MAX872's unique architecture enables it to regulate to within 200mV of its output.

Superior Performance Over REF43 and 40% Less Power

2.5V, 7ppm/°C Voltage Reference is Available in 8-Pin SO Package

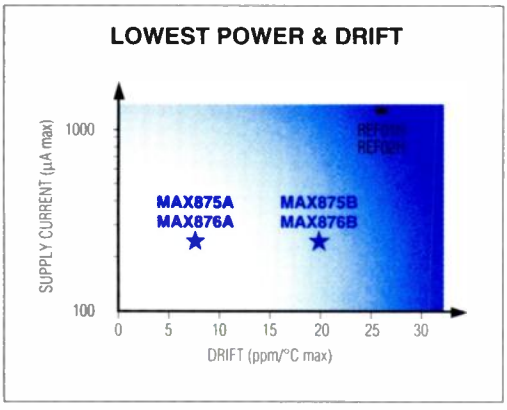


The MAX873 precision 2.5V reference provides unadjusted accuracy of ±0.06% at room temperature and 0.12% over the extended temperature range.

The MAX873 redefines the standard for all future low-power, precision 2.5V references by surpassing the REF43 in accuracy and power consumption. The 7ppm/°C (A-grade) and 20ppm/°C (B-grade) drift characteristics of the MAX873 improve on the 25ppm/°C drift of the highest grade 8-pin SO REF43. Plus, the MAX873 consumes a maximum of 280µA quiescent current, compared to 450µA for the REF43—a 40% savings in power. Initial accuracy is also improved over the REF43: ±1.5mV for the MAX873A and ±2.5mV for the MAX873B, versus 5mV for the REF43.

5V and 10V References Consume Less than 280µA and Guarantee Less than 7ppm/°C Drift

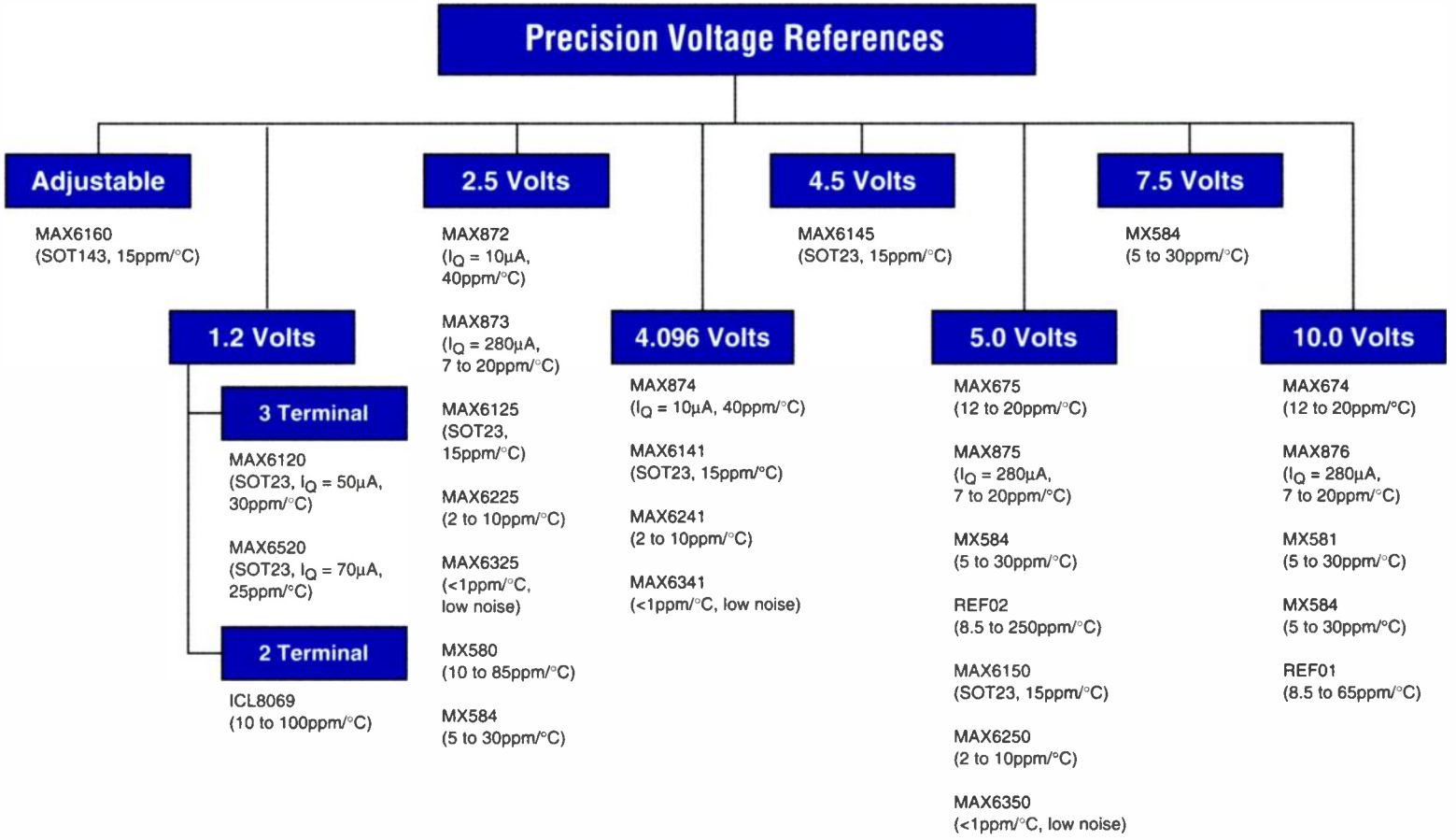
MAX875 and MAX876 are Available in 8-Pin DIP and SO Packages



The MAX875 and MAX876 draw 80% less power than the REF01 or REF02.

The MAX875 and MAX876 are the only 5V and 10V references to guarantee 0.06% initial accuracy and 7ppm/°C drift while operating from less than 280µA supply current. Both parts offer an 80% reduction in power and an 80% improvement in accuracy compared to the industry-standard REF01 and REF02.

MAX875/MAX876 output characteristics include a maximum line regulation of 4ppm/V and a load regulation of less than 15ppm/mA. And, unlike the REF01 and REF02, the MAX875/MAX876 sink as much as 2mA and source 10mA. A TEMP pin is available for applications that require temperature compensation. An output voltage trim pin is also available, to provide a ±95mV trim range for applications that require output voltage adjustment.



Voltage References

Part Number	Voltage (V)	Temp. Drift (ppm/°C max)	Initial Accuracy T_A = +25°C (%F.S. max)	Quiescent Current (mA max)	Noise 0.1Hz to 10Hz (µVp-p), max(typ)	Package Options	Temp. Ranges*	Features	Price† 1000-up ($)
MAX6160	Adj.	100 (15 typ)	1	100µA	(15)	SOT143, SO	E	Low-cost, low-dropout 3-terminal adjustable voltage reference	1.50
MAX6120	1.2	100 (30 typ)	1	70µA	(10)	SOT23, SO	E	Low-cost, micropower 3-terminal reference	0.80
MAX6520	1.2	50 (25 typ)	1	70µA	(10)	SOT23, SO	E	Low-cost, micropower 3-terminal reference	1.25
ICL8069	1.2	10 to 100	2	0.05	5 (10Hz to 10kHz)	TO-52, TO-92, SO[1]	C,E,M	Micropower 2-terminal reference	0.65
MAX872	2.5	40	0.2	10µA	(60)	DIP, SO	C,E	Lowest power, lowest dropout precision reference. V_{CC} = V_{OUT} + 200mV	2.12
MAX873	2.5	7 to 20	0.06 to 0.1	0.28	(16)	DIP, SO	C,E	Low power/drift, REF43 upgrade	2.25
MAX6125	2.5	50 (15 typ)	1	100µA	(15)	SOT23, SO	E	Low-cost, low-dropout 3-terminal reference	1.25
MAX6225	2.5	2 to 5	0.04 to 0.1	2.7	(1.5)	DIP, SO, CERDIP	C,E,M	Low drift, less than 1.5µVp-p output noise	2.25
MAX6325	2.5	1 to 2.5	0.04	2.7	(1.5)	DIP, SO, CERDIP	C,E,M	Ultra-low drift, 1.5µVp-p output noise	6.70
MX580	2.5	10 to 85	0.4 to 3	1.5	(60)	TO-52, SO[2]	C,M	Low-drift bandgap reference	2.03
MX584	2.5	5 to 30	0.05 to 0.3	1	(50)	TO-99, DIP, SO, CERDIP	C,M	Low-drift programmable reference	3.09
MAX874	4.096	40	0.2	10µA	(60)	DIP, SO	C,E	Lowest power, lowest dropout precision reference. V_{CC} = V_{OUT} + 200mV	2.12
MAX6141	4.096	50 (15 typ)	1	105µA	(25)	SOT23, SO	E	Low-cost, low-dropout 3-terminal reference	1.25
MAX6241	4.096	2 to 5	0.02 to 0.1	2.9	(2.4)	DIP, SO, CERDIP	C,E,M	Low drift, less than 2.4µVp-p output noise	2.25
MAX6341	4.096	1 to 2.5	0.02	2.9	(1.5)	DIP, SO, CERDIP	C,E,M	Ultra-low drift, 2.4µVp-p output noise	6.70
MAX6145	4.5	50	1	105µA	(30)	SOT23, SO	E	Low-cost, low-dropout 3-terminal reference	1.25
MAX675	5.0	12 to 20	0.15	1.4	15	TO-99, DIP, SO, CERDIP	C,E,M	Low-drift, low-noise bandgap reference	3.08
MAX875	5.0	7 to 20	0.06 to 0.1	0.28	(32)	DIP, SO	C,E	Low power/drift, REF02 upgrade	2.10
MAX6150	5.0	50 (15 typ)	1	110µA	(35)	SOT23, SO	E	Low-cost, low-dropout 3-terminal reference	1.25
MAX6250	5.0	2 to 5	0.02 to 0.1	3	(3)	DIP, SO, CERDIP	C,E,M	Low drift, less than 3.0µVp-p output noise	2.25
MAX6350	5.0	1 to 2.5	0.02	3	(1.5)	DIP, SO, CERDIP	C,E,M	Ultra-low drift, 3.0µVp-p output noise	6.70
MX584	5.0	5 to 30	0.05 to 0.3	1	(50)	TO-99, DIP, SO, CERDIP	C,M	Low-drift programmable reference	3.09
REF02	5.0	8.5 to 250	0.3 to 2	1.4	15	TO-99, DIP, SO, CERDIP	C,M	Low-drift bandgap reference	1.28
MX584	7.5	5 to 30	0.05 to 0.3	1	(50)	TO-99, DIP, SO, CERDIP	C,M	Low-drift programmable reference	3.09
MAX674	10.0	12 to 20	0.15	1.4	30	TO-99, DIP, SO, CERDIP	C,E,M	Low-drift, low-noise bandgap reference	3.08
MAX876	10.0	7 to 20	0.06 to 0.1	0.28	(64)	DIP, SO	C,E	Low power/drift, REF01 upgrade	2.10
MX581	10.0	5 to 30	0.05 to 0.3	1	(50)	TO-39, SO[3]	C,M	Low-drift bandgap reference	2.30
MX584	10.0	5 to 30	0.05 to 0.3	1	(50)	TO-99, DIP, SO, CERDIP	C,M	Low-drift programmable reference	3.09
REF01	10.0	8.5 to 65	0.3 to 1	1.4	30	TO-99, DIP, SO, CERDIP	C,M	Low-drift bandgap reference	1.28

1 The ICL8069 is available in 2-pin TO-52, 2-pin TO-92, and 8-pin SO packages.
2 The MX580 is available in 3-pin TO-52 and 8-pin SO packages.
3 The MX581 is available in 3-pin TO-39 and 8-pin SO packages.
* Temperature Ranges: C = 0°C to +70°C, I = -25°C to +85°C, E = -40°C to +85°C, M = -55°C to +125°C
† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates. Lowest grade pricing.

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MAXIM

Here's What's Coming In The Next Two Months

Be sure to check out the best cutting-edge information for engineers and engineering managers, every two weeks. Here's the line-up of some of the important topics featured in our June and July issues.

JUNE 8, 1998 ISSUE

- **Electronic Design Automation:** DAC Preview
- **Communications/Networking Technology:** ATM/Gigabit Networking & Switching
- **PIPS:** Packaging
- **DSP:** Contributed Article .
- **Computer Boards & Buses:** Microcontroller Boards, Graphics, PCMCIA, Peripherals

JUNE 22, 1998 ISSUE

- **Analog Design:** Data-Aquisition Modules
- **Test & Measurements:** Update: Digital Storage Oscilloscopes
- **Embedded Systems**
- **Digital Design:** Advanced Static Memories

JULY 6, 1998 ISSUE

- **Electronic Design Automation**
- **PIPS:** Power Management
- **Analog Design:** Power Control
- **Digital Design**

JULY 20, 1998 ISSUE

- **Communications/Networking Technology:** Advanced Paging/Messaging
- **Computers Boards & Buses**
- **Software:** Development Tools For Java
- **Multimedia**

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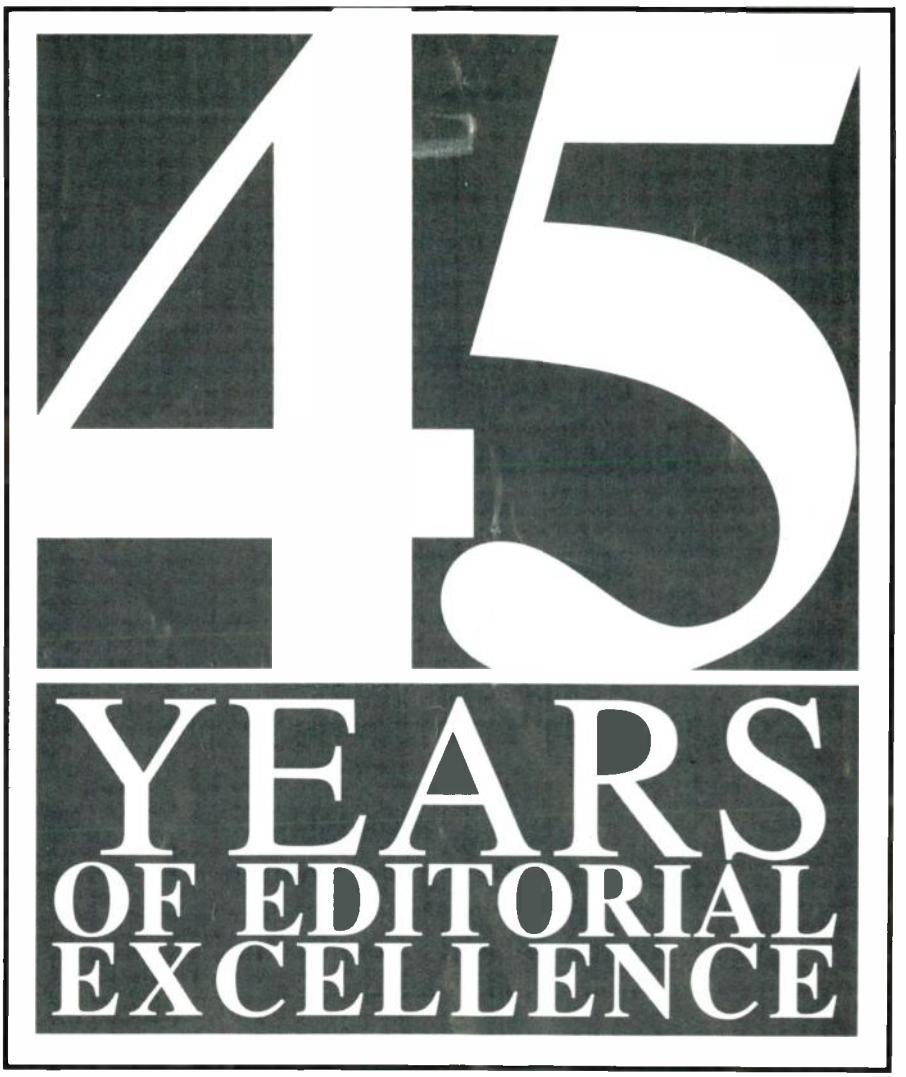

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A PENTON PUBLICATION

Suppliers Tailor DSPs For Digital Motor Control

Suppliers Ready DSP Solutions For Consumer And Industrial Use By Integrating Peripherals, Memory, And Control Functions Around A Core.

Ashok Bindra

Programmable digital signal processors (DSPs) have evolved substantially to bring on board the appropriate mix of processing power, peripherals, and memory necessary to pervade the emerging world of digital motor control. DSP suppliers are creating devices with the speed and computational power to execute control algorithms required in servo control; industrial control; brushless dc; single-phase ac induction motors; and advanced three-phase, variable-drive systems. In short, they are crafting chips that are ready to challenge microcontrollers on their own turf.

To do this, suppliers are revamping DSP architectures. But they also have significantly cut manufacturing costs to make the price-per-MIPS attractive for high-volume, cost-sensitive appliance and industrial applications, in addition to applications in disk drives and many other emerging high-volume consumer products. In fact, today, the DSP chip is armed with a combination of high-speed, number-crunching capabilities for real-time signal processing, as well as the ability to perform fast-context switching and data manipulation for control tasks.

On the other hand, microcontroller manufacturers are adding math capabilities to their processors to make them attractive for DSP operations in similar applications. MCU's like Motorola's 68HC16 and Intel's 80196 are two popular examples. Recently, Motorola combined its 32-bit M-core RISC controller with its 16-bit, 60 MIPS DSP56600 to create a single low-voltage, baseband processor (DSP56652) for cellular applications. A sophisticated MCU-DSP interface (MDI) module allows the two cores to communicate while handling their specific core and peripheral functions.

Meanwhile, Hitachi has combined a 32-bit RISC engine with a 16-bit fixed-point DSP to produce the SH-DSP core. This core blends signal processing and microcontroller operations on the same die. The current wave of RISC/DSP combinations is being targeted at digital communication designs, but it won't be long before their capabilities are exploited in consumer and control applications. In fact, Zilog has added a powerful set of peripherals to its 20 MIPS, 16-bit DSP core to address the embedded controller market.

Ready For Production

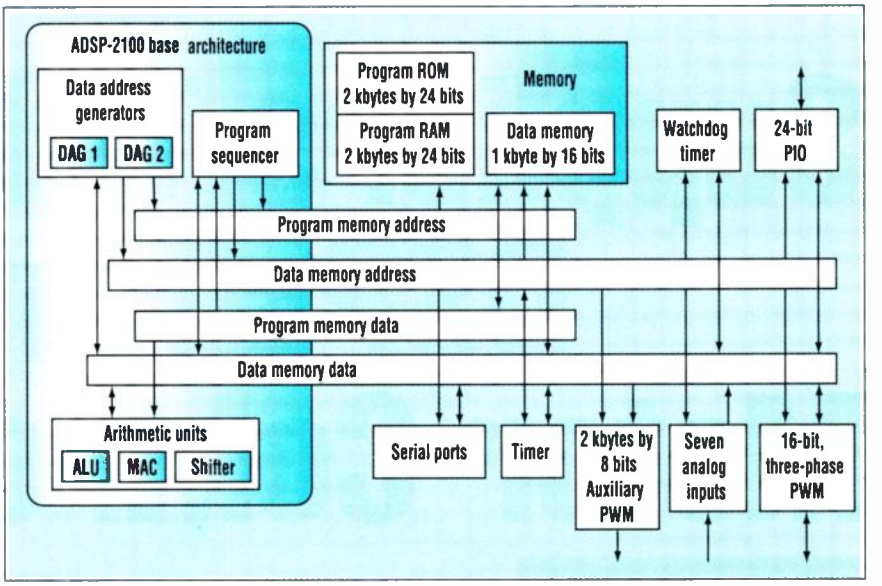
After years of design and development, DSP-based motor-control systems are ready for production, according to the market research firm Forward Concepts Inc., Tempe, Ariz. From an insignificant market share in 1996, motor control is estimated to consume over 21 million DSP units this year, predicts Forward Concept's preliminary study. The company projects the consumption of programmable DSPs in the motor-control market to expand to over 400 million units by the end of the decade.

These numbers are based on the use of DSP chips in motor-control systems employed in "white goods" of all types,

automotive steering servos, robotic control motors, and other similar applications. However, it does not include disk-drive control units like hard drives, CD-ROMs, and DVD drives. Texas Instruments' internal marketing experts predict that by 2001 some 1.5 billion motors will be using digital control instead of the traditional analog motors.

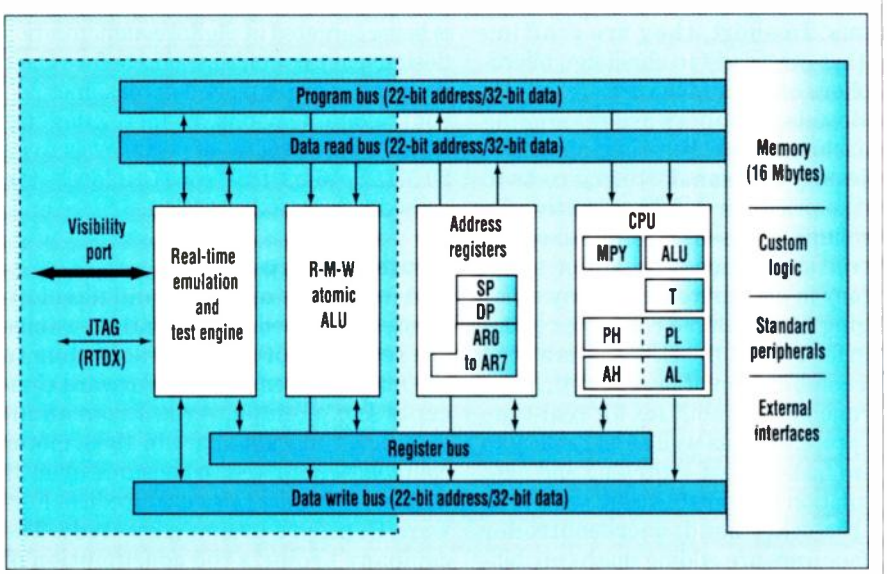
But DSP motor-control development cannot take place in a vacuum, notes Forward Concepts' president Will Strauss. According to Strauss, the development of motors that are more amenable to DSP control is gaining momentum. His research indicates that the switched reluctance (SR) motor (a brushless dc motor with no rotor windings or permanent magnets) controlled by a DSP chip could eventually be the most cost-effective solution for many applications.

The SR motor's high energy efficiency and low-speed torque have generated tremendous interest in this technology. However, prior to the DSP approach, the cost of electronics associated with the SR motor was prohibitively high for volume applications. The availability of inexpensive DSP chips promises a bright future for SR motors, predicts Forward Concepts' latest report.



2. Analog Devices' DSP motor controller, the ADMC331, integrates a 26-MIPS, 16-bit, fixed-point DSP core with a 10-bit ADC and the right set of control peripherals and memory to drive motors in appliances, fans, pumps, and other industrial systems.

Two key players optimizing their wares for this vast marketplace are Texas Instruments and Analog Devices. Both of these manufacturers have been working closely with systems houses for the last several years to generate solutions that are optimized for the end products. Meanwhile, other companies have been adding multiply-and-accumulate (MAC) instructions to the MCU, or combining DSP and MCU functions on-chip for motor control.



1. The real-time data exchange (RTDX) and Read-Mod-Write (R-M-W) are unique to Texas Instruments' new TMS320C2700 DSP architecture. The RTDX and visibility port permit developers to monitor, analyze, and modify code at 100 MHz without halting applications. This 100-MIPS, 16-bit fixed-point DSP engine combines control and signal processing functions to address a wide variety of embedded control applications.

Uniprocessor Architecture

To deliver an optimized DSP processor for the motor-control market, TI developed a brand new architecture that fully integrates the best of control and signal-processing tasks. The TMS320C2700 combines the high-speed MAC operations of DSP with the intensive I/O operational characteristics of the microcontroller (*Fig.1*). The result is a unified 100 MIPS processor for real-time embedded control applications. Plus, it offers MCU-like code density for control operations, says TI's product manager Andrew Soukup.

For example, a single instruction directs the processor to read data from memory, modify it, and write it back. Traditional DSPs, and even RISC-based MCUs require two or more steps to perform I/O operations. And, the C2700 core is compiler friendly, says TI.

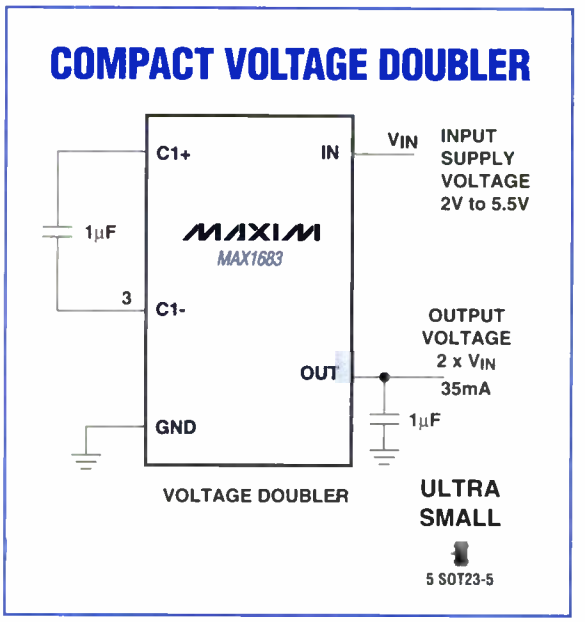
In fact, to simplify programming and development, TI has also developed an efficient C compiler for the C2700 architecture. The C compiler is designed to make the most of the C2700 assembly instructions. By comparison, the C2700 compiler code has

SOT23 VOLTAGE DOUBLERS DELIVER UP TO 35mA

Use Only Two 1µF Capacitors

The MAX1682 and MAX1683 are tiny charge-pump DC-DC converters that **double** an input voltage (2V to 5.5V), creating output voltages of 4V to 11V. They come in an ultra-small 5-pin SOT23 package that uses only 1/4 the board space of a standard 8-pin SO. Only two small ceramic capacitors are needed to complete the circuit, which fits in 0.03in² (19mm²). For **inverting** charge pumps with the same package and specifications, consider the MAX828 and MAX829 or MAX870 and MAX871.

- Double the Input Voltage
- 5-Pin SOT23 Package
- 2.0V to 5.5V Input Voltage Range
- Low Supply Current: 110µA (MAX1682)
- Uses Only Two 1µF Capacitors (MAX1683)



Use the MAX1682 where low power consumption is critical. Use the MAX1683 where small size is critical. It switches at 35kHz, which is also above the audio range.

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been demonstrated to be up to 45% more dense than compiled code for widely used MCUs like the MC68HC16, 80196, and ARM7TDM1.

In order to speed system debugging and time-to-market, the C2700 DSP architecture incorporates a JTAG-based visibility port and TI's new real-time data exchange (RTDX). In conjunction with the JTAG port, the RTDX allows C2700 developers to monitor, analyze, and modify code at speeds of 100 MHz, without impacting results or halting applications, according to chief architect Alex Tessarolo. Traditional in-circuit emulation breaks down as signal speeds ramp up above 100 MHz, adds Tessarolo.

The RTDX communicates between the host computer and the target DSP device using an emulator and a very small procedural library. This internal data-exchange library makes use of a scan-based emulator to move data via the IEEE-1149.1 (JTAG) serial test bus. Initial RTDX implementations will result in data exchange rates of at least 8 kbytes/s, sufficient for running control, servo and audio applications at full speed, claims TI. The company intends to improve the RTDX bandwidth in future DSP introductions by a factor of 10.

Additionally, the Read-Mod-Write atomic ALU is unique to this architecture, notes Tessarolo. This provides about 15% improvement in code density, while protecting the code from interrupts. In essence, C2700 is a flexible architecture that permits intermixing of DSP and control instructions, asserts Tessarolo.

"Capable of addressing large program memories, the C27XX DSP will take us into new areas where multiple motors have to be controlled in synchronization, such as in industrial automation, robotics, and the textile industry, as well as control applications that need precision," says Raj Chirayil, worldwide business manager for TI's digital control systems. A single 100 MIPS processor now brings the precision needed in disk drives and other mass storage products where tracks-per-inch keep rising, adds Chirayil. Because the CPU of the C2700 is identical to the 16-bit fixed-point C2XX processor, it provides an upgrade path to the users of the optimized TMS32024X family. However, initially the C2700 based DSP solutions are targeted at mass storage systems such as hard disk drives and digital video disks (DVDs).

DSP Solutions

While the C2700 core-based, application-specific devices will not be on the market before the first quarter of 1999, TI continues to expand the 24X family for a variety of electric motor-control applications. Scheduled for sampling in this quarter are two flash-based DSP controller devices, the TMS320F241/243 with 8K of reprogrammable flash memory and control area networking (CAN). Complex machines that use multiple electric motors can be interconnected using a CAN bus to link DSP controllers within each motor for smoother, precise control of the machine.

Other applications targeted for these devices include uninterruptible power supplies, computer numerically controlled (CNC) machines, and automotive systems. ROM versions, the C241/242, are planned for the third quarter. Tailored for cost-sensitive consumer and home appliances, the C242 with 4 kwords of ROM is priced under $5 in quantities of 100,000. The F241 and C241/242 come in pin-to-pin-compatible, 68-lead PLCC and 64-lead PQFP packages. The F243 will be offered in 144-pin TQFP packages.

Similarly, TI also has planned aggressive pricing for C2700 core-based DSPs. Currently, the DSP supplier is readying custom solutions using the 2700 core and 0.25-µm CMOS process. Standard 100 MIPS devices using the new-generation core and 0.18-µm TImeline technology are slated for release early next year. TI's roadmap indicates that the C2700 core will deliver 150 MIPS next year using 0.18-µm technology, with the goal to achieve 200 MIPS capability by the end of this decade.

Equally aggressive about the digital motor-control market is Analog Devices, which is rapidly building its ADSP-2171 core-based ADMC3XX family for a myriad of motor-control requirements. The latest member to join this growing family is the ADMC331, a 26-MIPS part integrated with a 10-bit ADC and various motor-control peripherals for ac-induction, permanent-magnet synchronous motors, brushless dc, and SR motors (*Fig. 2*).

Key peripherals include a three-phase, 16-bit PWM generation unit; a 16-bit watchdog timer; 24-bit I/O ports; and two flexible, bidirectional synchronous serial ports. Plus, the device offers a 2 k-by-24-bit program ROM and a 2 k-by-24-bit data RAM. The program memory ROM contains a number of useful mathematical and motor-control utilities that can be called up as subroutines from the user code. The routines include various trigonometric routines, logarithmic functions, and vector transformations and rotations needed for ac-induction and permanent-magnet synchronous motors.

To compete from a price-performance standpoint, the ADMC331 is priced below $5 in quantities of 250,000 in an 80-pin TQFP package. To challenge microcontrollers in this market, Analog Devices shaved off a few functions to come up with a version housed in a 28-pin package and priced at $3 in OEM quantities. In brief, the suppliers are watching the price line as they struggle to bring prices under $5, kicking these devices into high gear.

Aggressive Plans

"Our commitment to the motor-control industry is evident in our plan to develop 20 new DSP-based motor-control chips over the next two years," states Phil Davies, director of Analog Device's dedicated Motor Control Group. The ADMC331 is the third member of the family. The last two were the ADMC300 and ADMC330. In fact, the ADMC300 was developed under a DARPA contract for the Electric/Hybrid Vehicle powertrain program. A new line of motor-control DSPs is also in the works.

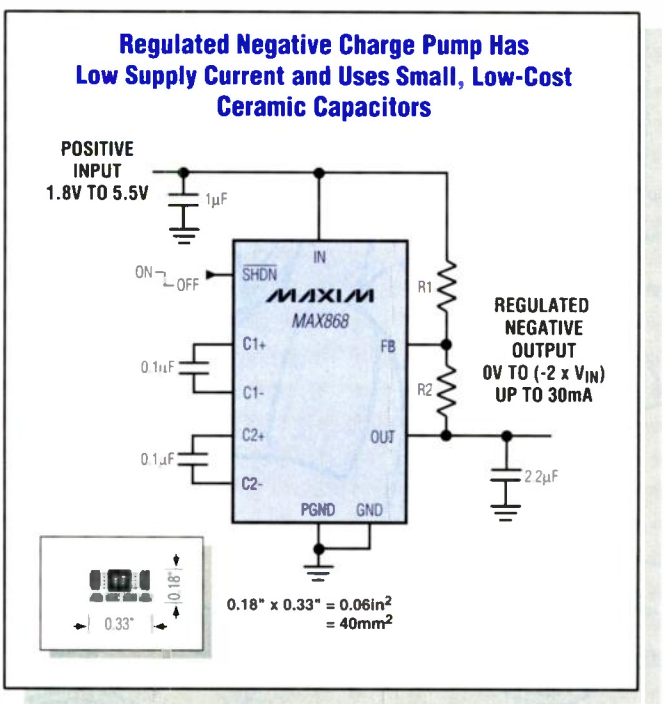
Exploiting the 33-MIPS capability of the ADSP-2171 DSP core, the company is in the process of readying a brand new family, the ADMC400. This new line of motor-control DSPs will leverage Analog Devices' strength in fast, high-resolution data converters, and provide a major leap

SMALLEST REGULATED +3V_{IN} TO -5V_{OUT} SUPPLY

Regulated Charge Pump Fits in 0.06in² with Only 1.11mm Height

The MAX868 generates a regulated negative supply of up to -2 x V_{IN} for LCDs, CCD arrays, and other analog circuitry. A unique 450kHz on-demand switching scheme regulates up to 30mA loads using very small ceramic capacitors and holds quiescent current at just 35µA for maximum light-load efficiency. The MAX868 comes in a 10-pin µMAX package that's only 1.11mm high and occupies half the board area of a standard 8-pin SO.

- **Regulated Negative Output Voltage Up to -2 x V_{IN}**
- **Up to 30mA Output Current**
- **Unique 450kHz On-Demand Switching Offers Best Combination of:**
  - **Small Capacitors (0.1µF)**
  - **Low Quiescent Current (30µA)**
- **1µA Shutdown Current**
- **1.8V to 5.5V Input Range**
- **No Inductor Needed**



Generate a regulated negative supply with up to 30mA output current using an ultra-compact design that fits in 0.06in² (40mm²) and is only 1.11mm high.

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in performance. The ADMC400 is being targeted at sensorless and fluxless control-type applications. The first member of the ADMC400 family will be based on a 0.5-µm process, and incorporate a 12-bit or better ADC with a 2-MHz sampling rate, programmable encoder interface, and other common control peripherals. Samples will be available in the third quarter, with production slated for early next year.

Furthermore, derivatives of the 32-bit, floating-point SHARC core are also under development for high-end multiaxis motor control, according to Analog Devices. Optimized motor-control DSPs designed around the SHARC core are expected to be unveiled later in this year.

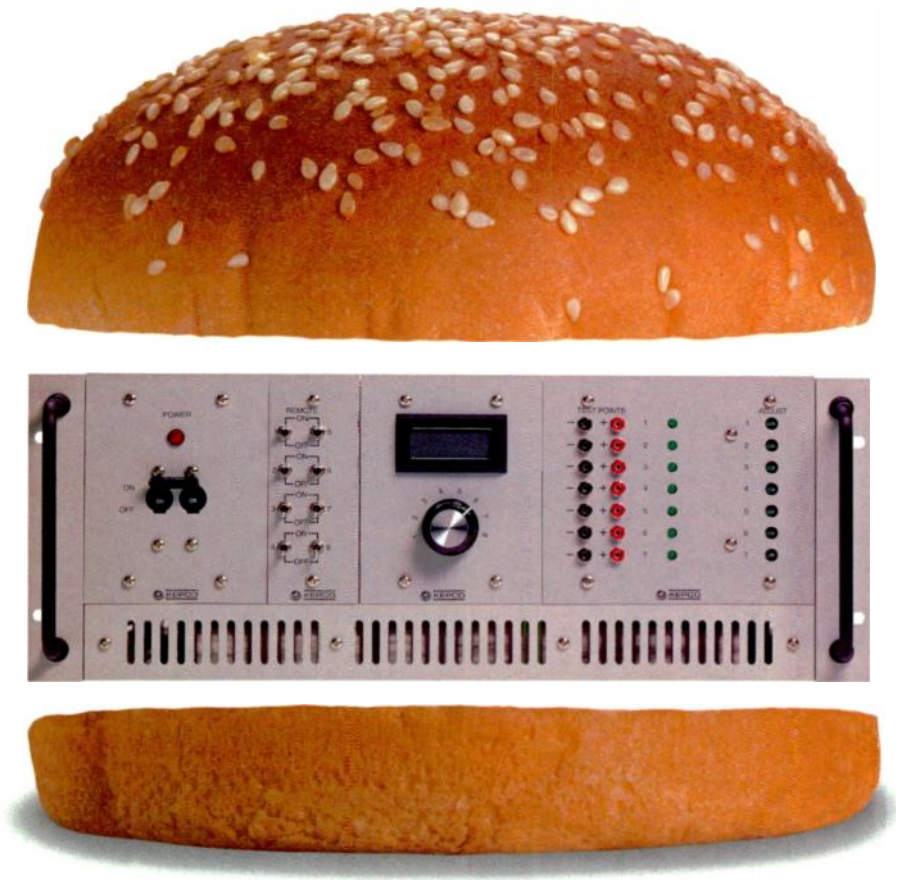
To promote and expedite application development around the ADMC3XX DSPs, Analog Devices, in partnership with International Rectifier Corp., a supplier of power mosfets and IGBTs, has crafted a motion-control development kit. Called Advanced PowIRtrain, the kit furnishes all the hardware, software, and tools needed to build an ADMC3XX-based motor control system.It costs $750.

Similar strategy has also been adopted by TI. In co-operation with third parties, the manufacturer is making available a motion-control kit (MCK240) for designs based on the F240, the first member of the DSP controller family. The kit provides the designer a complete set of tools to develop, implement, and test digital motor control algorithms.

Adding peripherals like PWM functions, watchdog timers, serial peripheral interface, ADCs, I/Os, PLL, and memory around a 20 MIPS, 16-bit fixed-point core, licensed from Clarkspur Design, Zilog has produced a family of optimized DSPs. Zilog's Z893X3 series is aimed at motor-controls, in addition to other markets served by the microcontrollers.

To support a variety of development needs, this family features the Z89323, with 8 kwords of ROM, and a one-time programmable version for prototypes and early production runs. To generate and debug code, the company offers an interactive in-circuit emulator under Windows.

THE KEPCO POWER ASSEMBLY PROGRAM

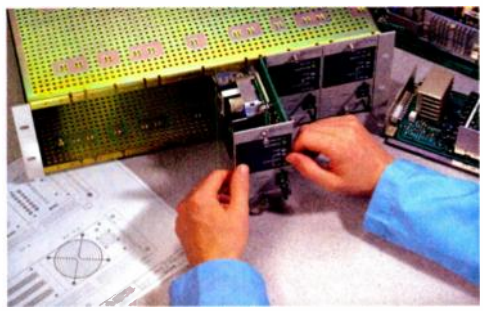


And you thought only burgers were made-to-order.

KEPCO
POWER
ASSEMBLY
PROGRAM

The Program

Kepco's power assembly program allows you to specify custom-configured arrays of volt-ampere combinations in rack mount housings of various sizes from 1U to 5U height (1 3/4" ~ 8 3/4"). Kepco's variety of single and multi-output power modules offers you a selection of output voltages from a nominal 3.3 volts to a nominal 48 volts. Power levels range from 15 watts to 1500 watts. For higher voltage we can easily connect modules in series and can parallel them for you to increase current capability or provide redundancy. You can select from switch-mode modules for fixed or trimmable outputs, or linear series-pass modules for analog-programmable applications. Digitally programmable (IEEE 488.2) plug-in power supplies are available for test applications.



Kepco power modules have either selectable 115-230 volt inputs or wide range (85-264 volt) inputs. Many sizes are available with Power Factor Correction (PFC). Models with d-c inputs (12V-150V d-c) are also available.

KEPCO POWER ASSEMBLY PROGRAM

You can specify the combinations you need, up to 8 outputs per assembly or more in bolt-down style. Select front panel components: meters, LEDs, test points, trimmers, etc. Select rear panel components: a-c or d-c input connections and barrier strips for the d-c output. We can mark the terminals as you require and custom screen and paint the panels if you wish.

Kepco's power assemblies are a good solution to the need for multiple output power supplies in industrial test applications.

Easy

We do all the work and deliver a fully tested, warranted product under a single part number, ready to slip into your system...hassle free. We're fast, too. Try us.

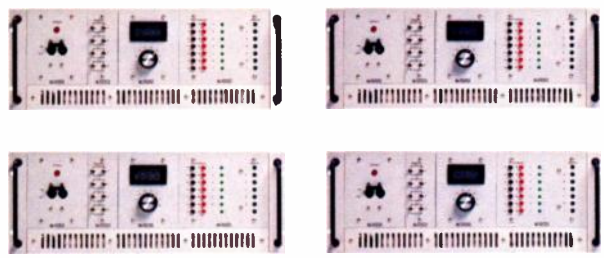
Send us as much detail as you can about your requirements. If there are special restrictions on size, environmental conditions, connectors, displays or sequencing...let us know. Our professional engineering staff will recommend a suitable combination of power modules, accessories, front and rear panel options, and will prepare for your consideration a CAD outline drawing showing how we plan to mount the power modules and how your front and rear panels will appear.

If there are equally effective alternate solutions, we will call to discuss these options. To help you decide, we can draft up separate proposal drawings for you to choose between. It is an interactive process until you are satisfied that you have your optimum solution.

Our plug-in modules offer a do-it-yourself option for many requirements. If we think this approach suitable, we will propose an appropriate selection which you can plug in on-site. This has the advantage of being easily modified as your requirements change.

Repeatable

No matter how many, or how few you order, all Kepco Power Assemblies are documented in full so we can easily reproduce your assembly at any time. Order one to use as a prototype. Order your production quantities now or later, whenever you are ready. Our CAD drawings can easily be recalled and printed allowing Kepco to reproduce your Power Assembly exactly, in any quantity.

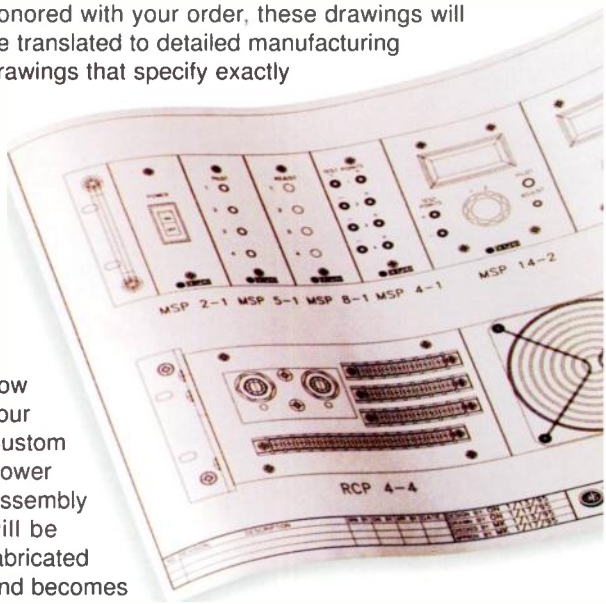


Your documentation includes a systems manual with all of the CAD drawings showing the arrangement of the front and rear panels and a top view drawing showing the position of all the individual power modules. The individual instruction manuals for each power module are also included.

KEPCO POWER ASSEMBLY PROGRAM

Professional
CAD Drawings

This is a sample of the documentation you'll get with our quotation. Computer-generated CAD drawings detail exactly how we propose to make your Power Assembly. When we have been honored with your order, these drawings will be translated to detailed manufacturing drawings that specify exactly how your Custom Power Assembly will be fabricated and becomes part of the instruction manual you receive when we ship. We will be using previously finished power modules that have already been tested and have been in boxes on our warehouse shelves. The finished Power Assembly will be tested as a whole and is shipped with a five year warranty regardless of the individual power module's warranty.



Flexible

Because Kepco stocks nearly all of the individual power modules in depth, we can easily respond to urgent needs. We have created and stock a variety of front and rear panels in multiples of 1/8th of a standard 19˝ x 3U rack. Eight of these panels or combinations of larger panels adding up to 8/8 may be combined to provide you with a nice selection of input switching, metering, pilots, trimmers and test points. The standard 3U high panels can be mounted in a 4U or 5U rack with a vent opening completing the balance of the space. Other panel sizes can be fabricated on a custom basis.

A typical 100 watt single voltage bolt-down power module, Series FAW

Do you need a special connector? Supply it to us, or tell us where to get it and we'll install it as you wish. Do you want to install your own equipment in the rack? Provide us with drawings of how the holes are to be punched and we will do your sheet metal, install the power modules, test them and deliver the assembly to you for finishing. Alternatively, you may supply Kepco with your own housing for us to do the power module installations. We're flexible, Talk to us. See how we can work with you to deliver professional, documented, warranted Custom-made Power Assemblies.

Our service includes installation of the power units you've selected (or we recommend) into one of our rack housings; professionally harnessing them to the front panel meter and control panels, and to the rear input/output panels and testing the completed assembly.

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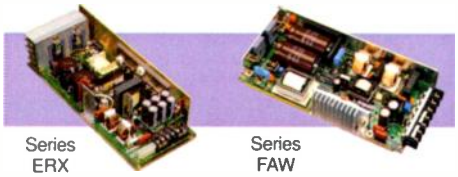
KEPCO POWER ASSEMBLY PROGRAM

The Products

Kepco will select suitable modules from the whole of our standard catalog line. Catalog 146-1862 details the specs on all of the available modules. Generally we select power supplies from among our ERX, FAW, HSM, RAX or RCW products, for bolt-down assemblies, and our PAT and PTR modules for analog-programmable requirements. If your requirements demand, we'll recommend other appropriate modules.



Series ERX 30~240W

Series FAW 15~150W

STANDARD OFF-THE-SHELF BOLT-DOWN POWER MODULES

Series RAX 50~1500W 300W shown

Series HSM 1000W/1500W

Series RCW 100~1500W 750W shown

Table of Voltage and Power Available from Standard Kepco Bolt-Down Power Modules

Nominal Voltage	15W	25W	30W	50W	60W	100W	150W	175W	240W	300W	350W	750W	1000W	1500W
3.3V				x		x		x			x	x	x	x
5V	x	x	x	x	x	x	x	x	x	x	x	x	x	x
12V	x	x	x	x	x	x	x	x	x	x	x	x	x	x
15V	x	x	x	x	x	x	x	x	x	x	x	x	x	x
24V	x	x	x	x	x	x	x	x	x	x	x	x	x	x
28V				x		x	x	x		x	x	x	x	x
48V				x		x	x	x		x	x	x	x	x

Kepco's plug-in 200 watt, IEEE 488.2 controllable modules. Series MST

IEEE-488.2 Programmable Plug-in Power Modules SERIES MST

Voltage	Current
0-6V	0-20A
0-15V	0-12A
0-25V	0-8A
0-36V	0-5A
0-55V	0-3.5A
0-75V	0-2.5A
0-100V	0-2A
0-150V	0-1.2A

USER-CONFIGURABLE PROGRAMMABLE POWER ASSEMBLIES

Does your requirement involve programmable power? Kepco's MST group are plug-in 200 watt power modules that mount in a 4U (7" high) housing called RA 55. This accommodates up to nine power modules. MST have a wide range a-c input: (85-264V a-c) with power factor correction (PFC). They are available with outputs from 0-6V to 0-150V, programmable.

MST are fitted with circuits for current sharing so that they can be used for N+1 redundancy combinations.

The table to the left shows the available models.

Control signals to the MST are distributed via a serial bus based on IEEE-1118. There are a number of instruments available from Kepco which will interface to an IEEE 488.2 bus, a VXI controller or directly to your PC or Mac. Resolution is 12 bits and either voltage or current may be controlled.

One such interface is MST 488-27, a plug-in interface to the GPIB (IEEE 488.2) that can be mounted into one slot of the RA 55 housing to provide you with a single GPIB connector through which you can address all eight remaining slots and two more full racks as well. A total of 27 MSTs can be addressed from a single GPIB connector.

KEPCO POWER ASSEMBLY PROGRAM

USER-CONFIGURABLE MULTIPLE-OUTPUT POWER ASSEMBLIES

3~8 Units, 50 Watts/Module to 1000 Watts/Module

Series HSP 1000W and 1500W plug-in modules for multi-output or N+1 redundancy

Does your requirement include a hot-swap N+1 fault tolerant assembly? We have configured two special groups of plug-in modules called HSF and HSP especially for this kind of application.

High power N+1 redundancy is available from Kepco's HSP group. These modules plug in for hot swap applications. A selection of their housings are described below. Up to three (3) 1500 watt modules are accommodated in a 3U panel height, either wired for independent operation, or in parallel for redundancy. These kilowatt plug-ins have a built in current-share circuit, OR-ing diodes, a voltage set trimmer and operate from any a-c voltage from 90-277 volts. Additionally, they meet the harmonic current limits of EN 61000-3-2 by having a PFC (Power Factor Correction) circuit built in. The 1500W modules operate from 230V a-c nominal.

HSP modules plug into a rack housing called RA 60 for hot swap, N+1 redundancy. Use RA 62 for two slots wired in parallel and one independent slot. Use RA 63 for three independent plug-in slots. If you wish to mount them without the plug-in feature, hard wired to your load, choose RA 58.

HSF are available in 50, 100 and 150 watt power levels. They're mounted on a slide that glides into keyed slots in a special set of housings: RA 19-(X)B. The RA 19-8B will accommodate up to eight (8) 50 watt or 100 watt plug-ins. The RA 19-6B will accommodate up to six (6) 150 watt plug-in HSFs. A combination of four of the narrow 50/100 watt HSF and three of the wider 150 watt HSF can be accommodated in an RA 19-7B.

Series HSF 50-150W plug-in modules for multi-output or N+1 redundancy

The table below shows the models available in Kepco's HSP and HSF groups.

Hot Swap N+1 Plug-in Power Modules

Nominal Voltage	50W	100W	150W	1000W	1500W
3.3V				HSP	
5V	HSF	HSF	HSF	HSP	
12V	HSF	HSF	HSF	HSP	
15V	HSF	HSF	HSF	HSP	
24V	HSF	HSF	HSF	HSP	HSP
28V		HSF	HSF	HSP	HSP
48V	HSF	HSF	HSF	HSP	HSP

RA 19-(X)B Accessories

Accessory	Part Number	Use
Filler Panel 1/24 Rack	RFP 19-24	Cover unused 1/24 rack slots
Filler Panel 1/12 Rack	RFP 19-12	Cover unused 1/12 rack slots
Filler Panel 1/8 Rack	RFP 19-18	Cover unused 1/8 rack slots
Filler Panel 1/6 Rack	RFP 19-16	Cover unused 1/6 rack slots
Filler Panel 2/8 Rack	RFP 19-28	Cover unused 2/8 rack slots
Filler Panel 2/6 Rack	RFP 19-26	Cover unused 2/6 rack slots
Filler Panel 3/8 Rack	RFP 19-38	Cover unused 3/8 rack slots
Filler Panel 1/2 Rack	RFP 19-48	Cover unused 1/2 rack slots

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KEPCO POWER ASSEMBLY PROGRAM

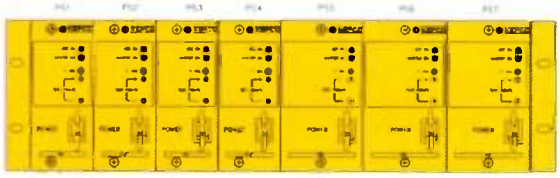
The Products

The rear of these 3U rack housings are designed for both flexibility and maximum redundancy. Euro-style terminal blocks accept a-c input wiring and d-c output wiring. Two a-c input blocks are provided so that power can be redundantly provided from separate branch circuits. The d-c outputs can combine like units for N+1 redundancy (the "OR-ing" diodes are built into each individual HSF power module). Connectors are provided for error sensing, current sharing and form C status contacts. The HSF power modules have forced current sharing for parallel operation.

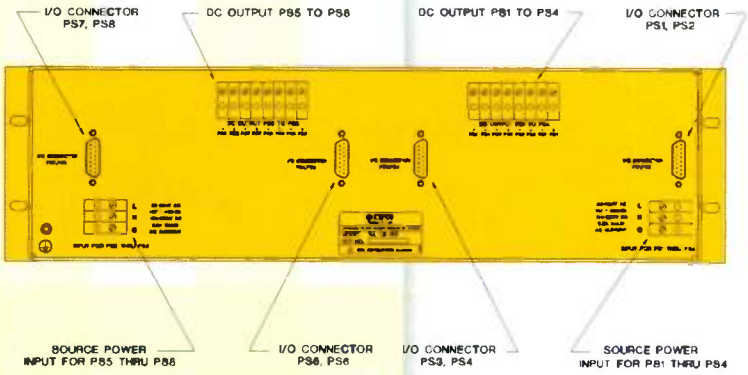
Alternatively, the individual plug-in HSF can be used separately to custom make a multi-output assembly with the added feature of being easily field configurable. Filler panels are available to cover unused slots.

RA 19-6B Rack Adapter with (6) 150W HSF Installed

RA 19-7B Rack Adapter with (4) 100W and (3) 150W HSF Installed



RA 19-8B Rack Adapter with (8) 100W HSF Installed



RA 19-8B Rack Adapter Rear Panel
This is the standard rear panel configuration. Other connector options are available. Please consult the factory.

The I/O Connector functions are brought out as follows:

1- Error sense (+S, -S) for each position.

2- Output voltage (+V, -V) for each position to permit wiring for local sense.

3- Current share bus (1) connection brought out for each pair of modules. (Each pair internally connected using DIP switches on the back plane).

4- Output status alarm contacts (Form C) for each position.

The front panel of each HSF contains an on-off switch, a "V d-c on" light, and a "master light". A recessed trimmer allows precise voltage settings and a pair of test points allow you to connect an external meter to calibrate the setting.

HSF have a wide range a-c input accepting any voltage from 95-264 volts a-c, 50-60 Hz. The input EMI filter is to FCC and VDE 0871 class B.

The RA 19-(X)B series of housings can be provided with other input and output connectors on a custom basis. Please give us a call to discuss your requirements.

KEPCO POWER ASSEMBLY PROGRAM

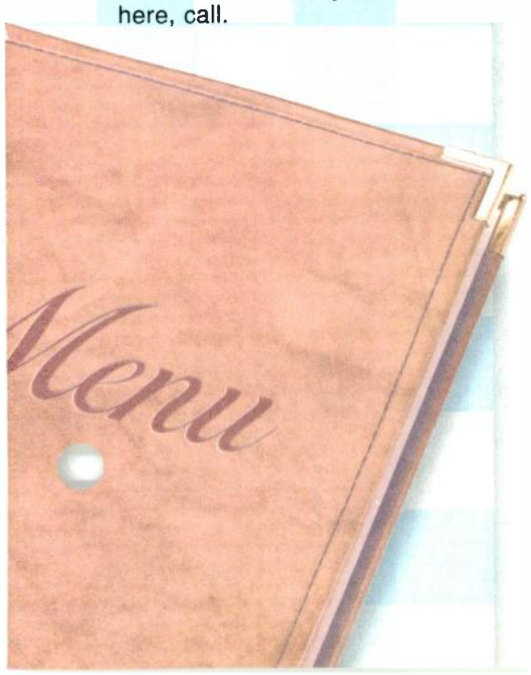
The Parts

Kepco offers a selection of front panel options for the bolt-down power assemblies. They are configured in multiples of 1/8-widths in a 3U (5.25") height. A total of 8/8 such panels fully populate a Power Assembly's front panel. The illustrations show our selection of on-off switches and circuit breakers, meters, LEDs, trimmer controls, test points for monitoring, etc. Filler panels are available in all widths to complete your assembly.

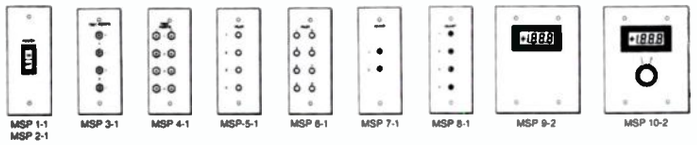
The rear panel parts include a-c and d-c input connectors, a variety of d-c output terminal blocks, vent panels and fans. These, too, are arranged in multiples of 1/8th panel width and should total 8/8. Blank fillers are available in all sizes.

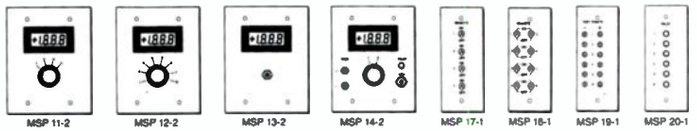
We have an array of precision current sensing resistors that we will wire as you request to provide current monitoring functions for the bolt-down assemblies. These are 50W and 100W low drift resistors in small ohmic ratings.

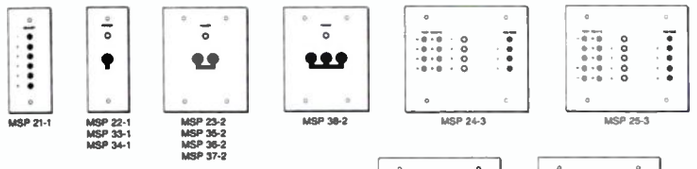
We can provide relays, diodes, chassis mounting slides and other special-purpose components as you require. If you don't see what you need here, call.

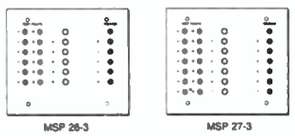


Front Panel Components

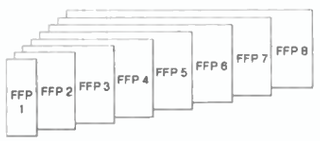




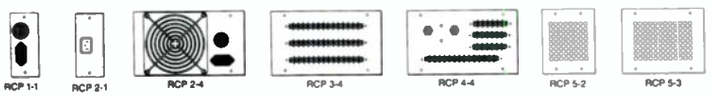


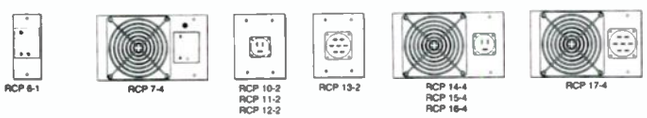


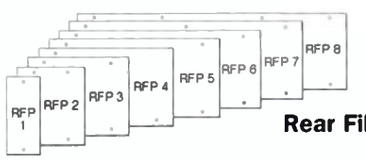
Front Filler Panels



Rear Panel Components







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8	

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The Proof

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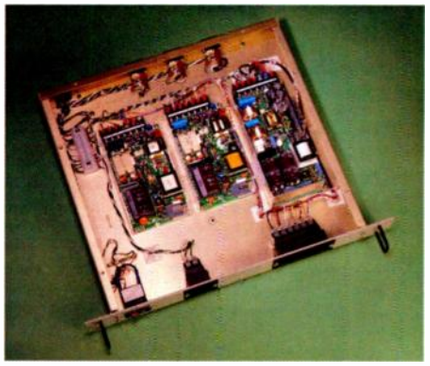
Visit our web site (http://www.kepcopower.com) for updated images of our work.

Kepco also does custom rack and stack assemblies using our large variety of instrument-grade power supplies 50W ~1000W.



A 1U housing containing three power modules. Customer specified connectors are mounted on the panel.

This is one of two assemblies we made for a major aerospace manufacturer. It is comprised of two linear power modules (PAT and PTR) and two 100W switch-mode modules (RAX). A third-party high voltage unit is also installed together with splitters to derive multiple HV outputs. A remote control circuit sequences the outputs on and off.

We made a custom panel and chassis for this customer in which we installed the power modules and delivered it for completion by the customer.

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Higher-Throughput DSP Chips Take On Complex Applications

Consumer, Telecommunications, And Instrumentation Gain From DSP Chips With Reduced Cost, And Lower Power Consumption.

Dave Bursky

Not long ago, the first-generation TMS320 16-bit DSP chips, developed by Texas Instruments, delivered an impressive 5 to 10 MIPS of compute throughput. Designers today, however, probably wouldn't raise an eyebrow at a processor with such meager computational power. The current-generation 16- and 24-bit DSP chips deliver from 40 to over 100 MIPS at prices well below that of the original TMS320C10. And, over the next year or so, new generations of DSP chips will deliver performance levels two-to-five times better than today's chips.

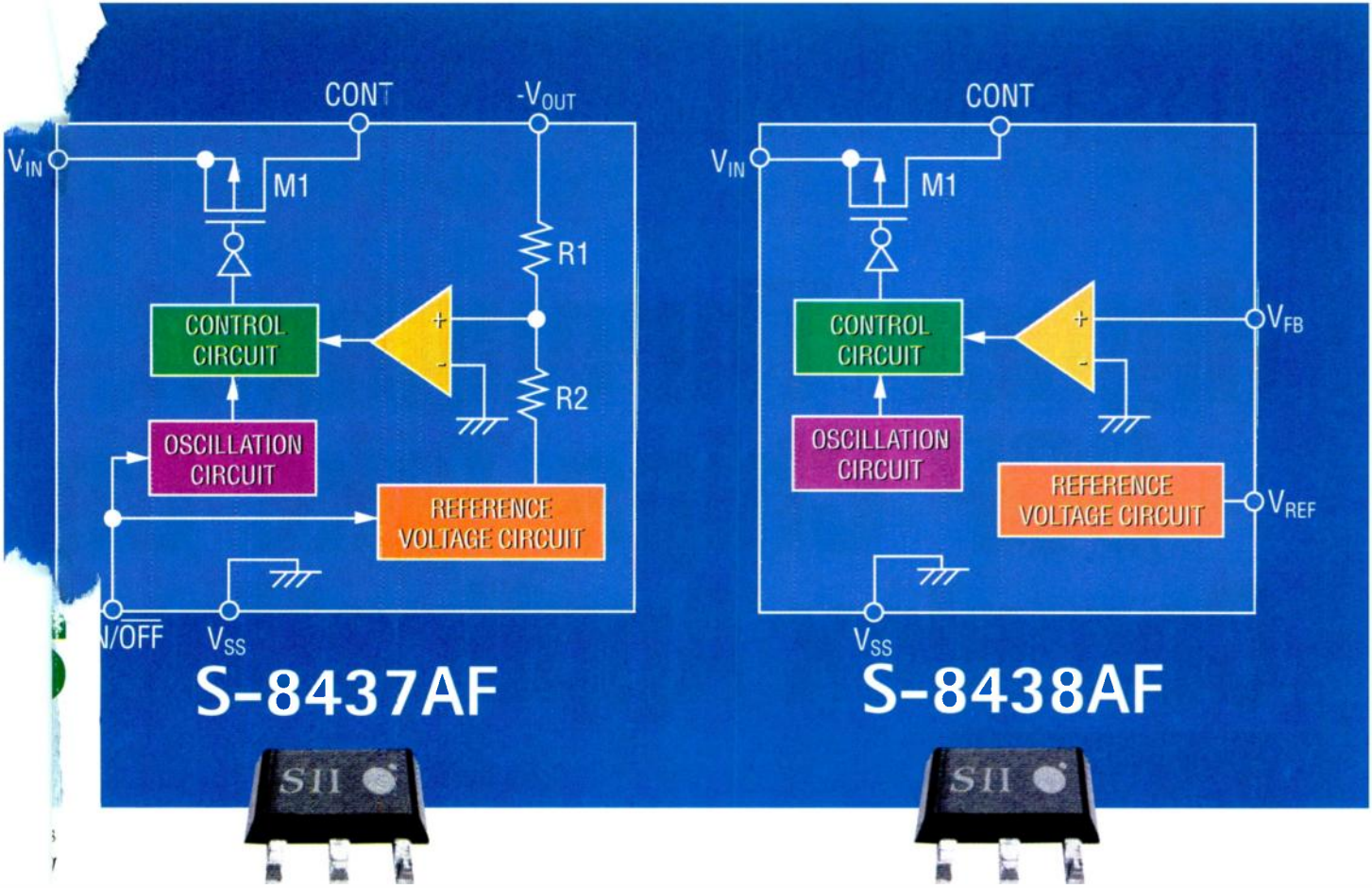
Today's consumer, telecommunications, and instrumentation markets are leveraging those millions of low-cost MIPS to create high-performance, low-cost products that use less power. And performance levels are on the rise as fabrication features shrink, circuit complexities and operating speeds increase, and new architectures evolve that take advantage of all these improvements.

DSP devices and compute blocks are not just standalone chips. Many have been turned into building-block cores, or have been initially created as a core rather than as a chip. Such cores allow designers to very easily craft a silicon-specific solution for their signal-processing needs. Additionally, programmable logic, as it gets denser and faster, can play a significant role in DSP. Recently released multihundred-thousand-gate chips by Altera, Xilinx, and others provide the capacity and performance to create application-specific algorithm accelerators that can surpass most off-the-shelf DSP chips *(see "Rolling Your Own DSP With FPGAs," p. 84).*

In recent months, many of the major suppliers of commodity DSP chips—Analog Devices, DSP Group, Lucent Technologies, Motorola, Siemens, and Texas Instruments—have introduced a new crop of low-cost, yet high-performance DSP chips. Additionally, several other companies including Advanced RISC Machines, Hitachi, Motorola, National Semiconductor, and Zilog, offer microprocessors or microcontrollers with on-chip DSP cores. Then, there are companies like GEC Plessey, LSI Logic, and VLSI Technology (as well as many of the DSP chip suppliers), that allow designers to custom craft a DSP chip by "gluing" together the appropriate cores and custom logic.

To reduce cost and improve performance, most companies have aggressively moved their chip design rules to 0.35 µm or smaller. One big benefit resulting from the smaller chips is reduced power consumption, which is a result of several factors—lower operating voltage, reduced parasitic losses, and of course, better circuit design.

In communications systems like cellular and cordless phones, the power reduction's immediate perks come in the form of longer battery life or reduced battery weight. Standby power in the microamp range is now possible for DSP chips. Operating voltages of less than 2-V at performance levels of 30+ MIPS also are now practical, and even lower operating volt-



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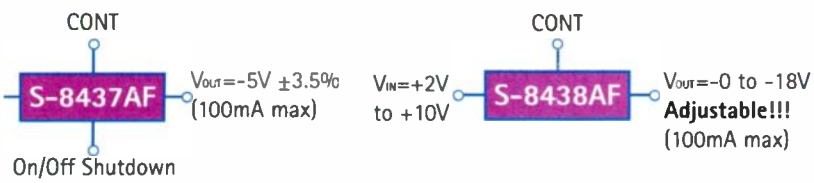

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- Remote controllers
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- Calculators
- LCD bias voltage
- Cordless phones
- Cell phones, pagers
- Hand held terminals

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After much thought and discussion, our editors have developed a new tag line that is about as direct and to the point as one can possibly get. It describes who we are and what we do. These four words tell our readers and advertisers what *Electronic Design* is all about:

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This new tag line reflects how *Electronic Design* reports on both emerging and new *technology* garnered from the movers and the shakers of this global industry. We report on and analyze how new technology will work in various *applications*. We then report on and analyze new *product* introductions. Finally, we offer you, our readers, *solution* articles and design ideas that help you and your peer engineers to build better products in this very competitive arena. These four words also represent the stages in which you, the design engineer, work.

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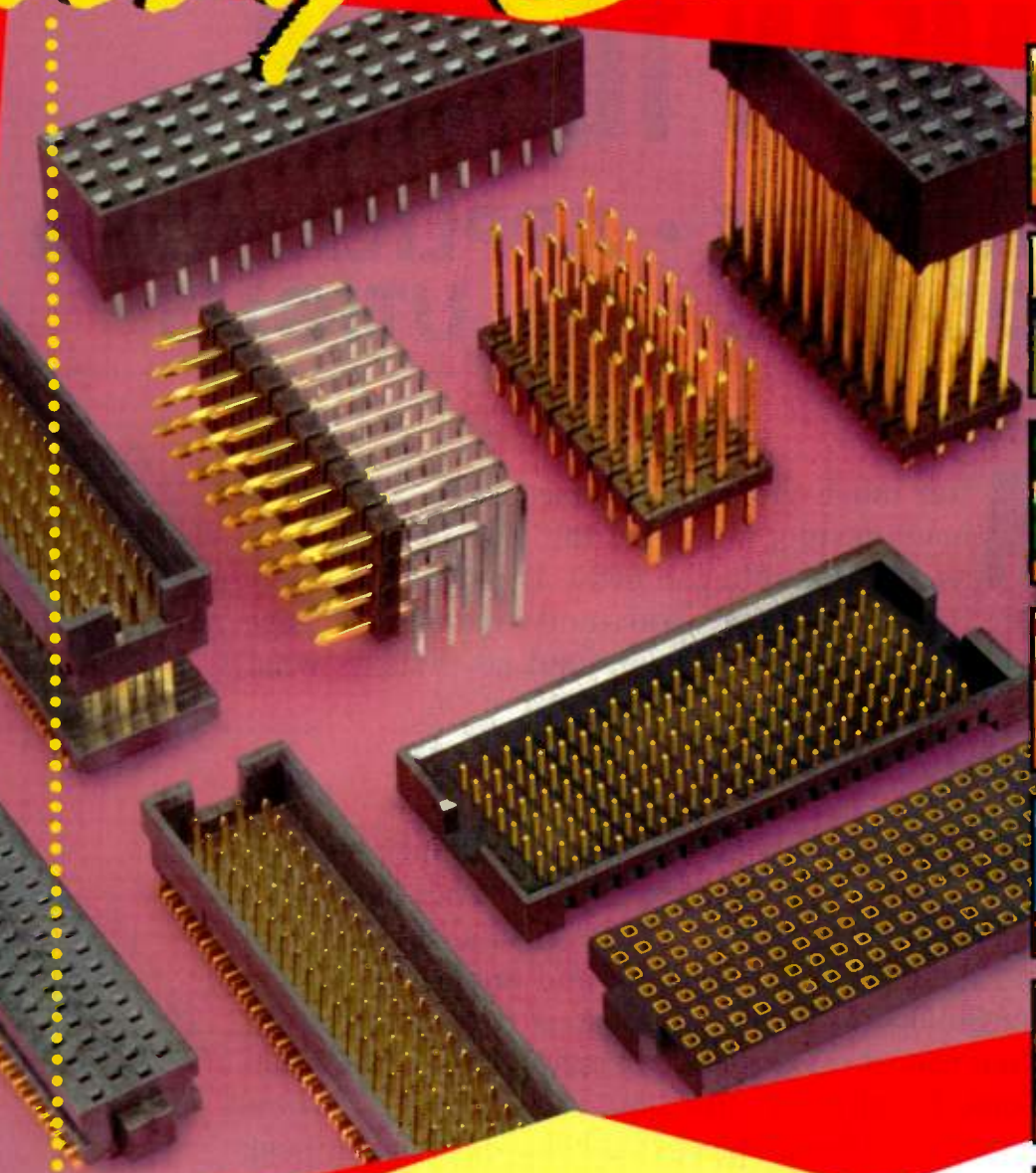

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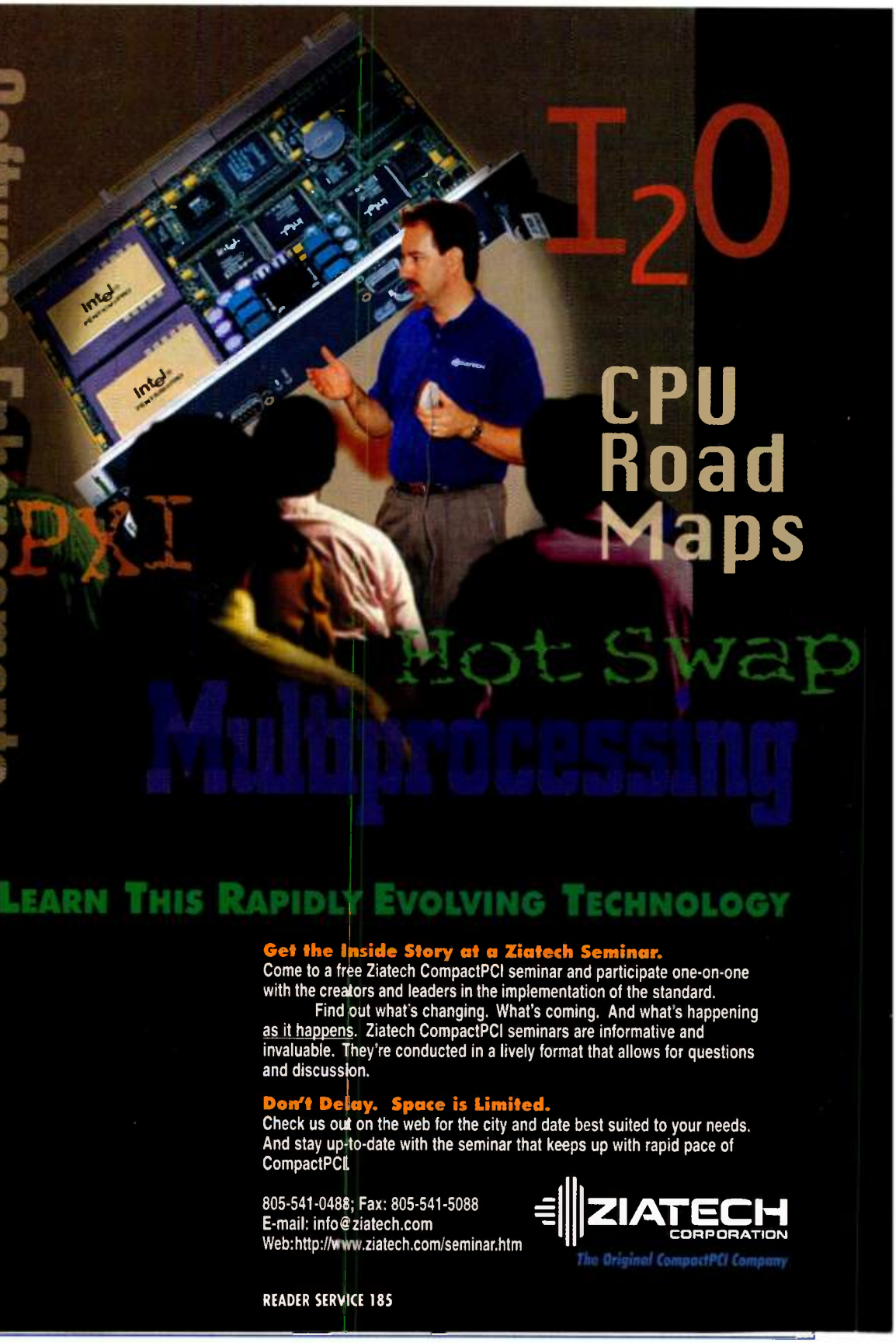

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Optimize Memory Subsystem For Top Performance

A Better Understanding Of Memory Accesses Allows DSP Memory Subsystems To Be Better Matched To The DSP Chips.

Richard Jaenicke and Paul Taddonio,
SKY Computers Inc., 27 Industrial, Chelmsford, MA 01824;
(978) 250-1920; Internet: www.sky.com.

Designers are increasingly using multiple DSP chips in applications that contain huge data sets—tens to hundreds of megabytes. Such applications can no longer be economically implemented with static RAMs, most of which typically have maximum capacities of 512 kbytes. Consequently, many system designers must consider the use of dynamic RAMs (DRAMs) to provide the larger memory space. Most DRAMs, however, are designed for PC workstations. To optimize DRAM use in DSP applications, designers must select the correct DRAM technology based on a different set of goals.

In addition, most DSP chips are optimized for I/O handing, and that typically means an interface optimized for use with SRAMs. As a result, overall memory subsystem performance in a DSP application depends on both the memory technology and the DSP chip's external interface.

Designers can pick from several DRAM architectures, each of which brings a number of pros and cons for various DSP system implementations. Thus, a better understanding of DRAM architectures and the DSP memory interface will allow designers to better optimize the memory subsystem for multiprocessor DSP applications.

On PCs, short read bursts for instruction cache-line fills have dominated accesses to main memory. But the increasing use of object-oriented languages and multitasking operating systems on PCs has lead to a significant number of accesses that are dispersed throughout main memory. This, in turn, has lead to an increasing emphasis on random-access latency instead of solely on burst-access time for subsequent reads to an open DRAM page.

Due to the emphasis on random-access latency, many PC manufacturers were slow to replace EDO (extended data out) DRAMs with synchronous DRAM (SDRAM) technology, which emphasizes burst accesses. In a typical 66-MHz memory implementation, SDRAM adds a cycle of latency on the initial access in exchange for one less cycle on each of the subsequent accesses. For a four-clock burst the net result is a two-cycle savings, but that is only relevant if more than just the first fetch was needed.

Differing Emphasis

In a DSP system, the speed of instruction loads is generally not the main concern. Signals are typically processed as vectors, which are many times the length of the data cache line. The code for the tight inner loops of signal processing is typically loaded once for a long vector of data. The emphasis, therefore, is on the speed of both the subsequent reads to the same cache line

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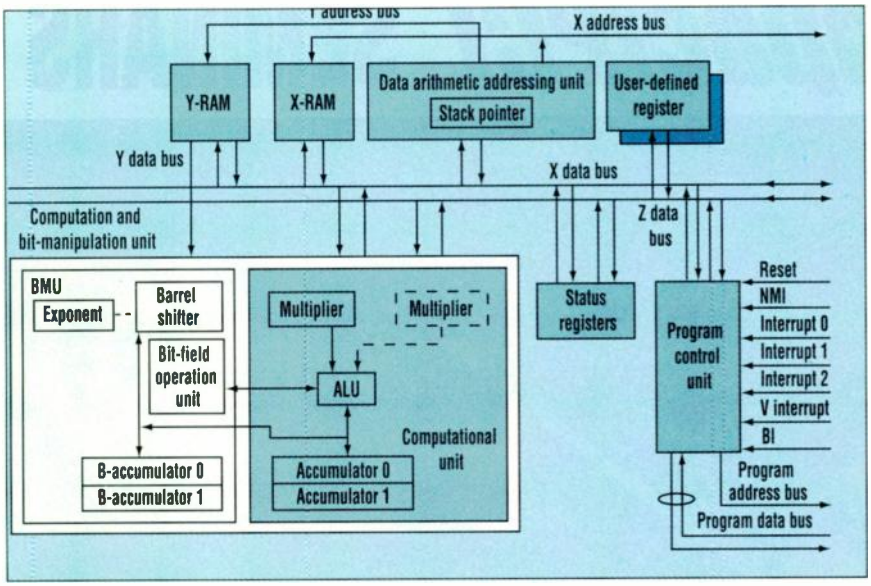

1. The Teak and TeakLite cores from the DSP Group deliver increased functionality compared to the company's previously-released Oak core, including a deeper pipeline and power management mechanisms. The full Teak core adds a second integer multiplier (dotted lines).

ages are possible.

Both Texas Instruments and Motorola have laboratory prototypes of 1-V DSP engines that may be in commercial products over the next 12 to 24 months. The problem, however, is that there aren't enough support circuits available that also operate at that low voltage. And 2.5- or 3.3-V logic interfaces will consume more power than the chips, thus canceling the benefit of the low operating voltage.

There also are many architectural improvements that designers can make to boost DSP engine performance. For instance, the DSP Group recently released an enhanced core, the Teak DSP, that employs a secondary multiplier in the data path to accelerate multiplication-intensive DSP algorithms *(Fig. 1)*. Similarly, Lucent Technologies released a dual multiplier DSP core and chip late last year—the DSP 16000 core and the 16100 processor. The Teak core can operate at clock speeds of up to about 130 MHz when powered by a 3.3-V supply. That yields a peak throughput of about 260 MIPS. Targeted at a similar performance requirement, the 16000-series core can operate at speeds of up to 100 MHz (at 2.7 V), but with the dual multiplier-accumulators, delivers a top throughput of about 200 MIPS.

Designed for use with synthesis tools, the Teak core actually comes in two versions, the Teak and the TeakLite. Both are backward-binary compatible with the company's previously released Oak DSP core. The TeakLite has a deeper pipeline than the Oak, allowing the new core to operate at speeds of 130 MHz when implemented in a 0.25-µm process. Also included are several power-management mechanisms to reduce power consumption.

The full Teak core, slated for release in the second half of this year, will feature the dual multiplier-accumulator units to deliver a peak throughput of 260 MIPS. It also supports multi-DSP core systems and CPU cores such as CompactRISC, recently licensed from National Semiconductor. The core will also handle double-word memory read and write instructions and perform high-speed interrupts and fast context

Roll your own DSP with FPGAs

The high logic complexity now available on field-programmable gate arrays (FPGAs) allows designers to implement custom DSP functions that can deliver algorithm acceleration levels well beyond what standard-architecture DSP chips can deliver. For instance, the 100-kgate-plus FPGAs from Altera, Xilinx, and other suppliers can be used to craft dedicated FIR or other filter algorithms in hardware, or to implement an array of multipliers to accelerate the computations for large matrix multiplications. The FPGAs can serve as a standalone solution or a co-processor to the DSP chip or host microprocessor.

As part of its design library, Altera provides the Flex DSP collection of macros that implement functions such as parameterized FIR filters; optimized high-level, fast-Fourier transform engines; and adaptive FIR megafunctions. Building blocks like an 8-by-8-bit pipelined multiplier can operate at 172 MHz while consuming 145 logic cells. A 16-bit multiplier can operate at 109 MHz, and consumes 561 logic cells. A more-complex function, such as a 512-point FFT engine with 8-bit data and 8-bit twiddle factors, employing on-chip dual memory blocks consumes 1075 logic cells and requires 40.3 µs to execute the function.

Taking a more software-oriented approach, Xilinx uses its core generation software in combination with DSP-system-level design tools that Elanix Inc., Westlake Village, Calif., created and ported to the Xilinx FPGA architecture. Thus, with the Elanix SystemView tools, designers can create and verify the algorithms, optimize the bit widths of the various functional blocks, and then pass the design file to the Xilinx Core Generator. The core generator creates parameterized cores using the company's Smart-IP technology. Those cores can then be combined with other logic functions when the total circuit is placed and routed on the FPGA. Performance of the multiplier and other functions is comparable to the performance of the Altera FPGAs.

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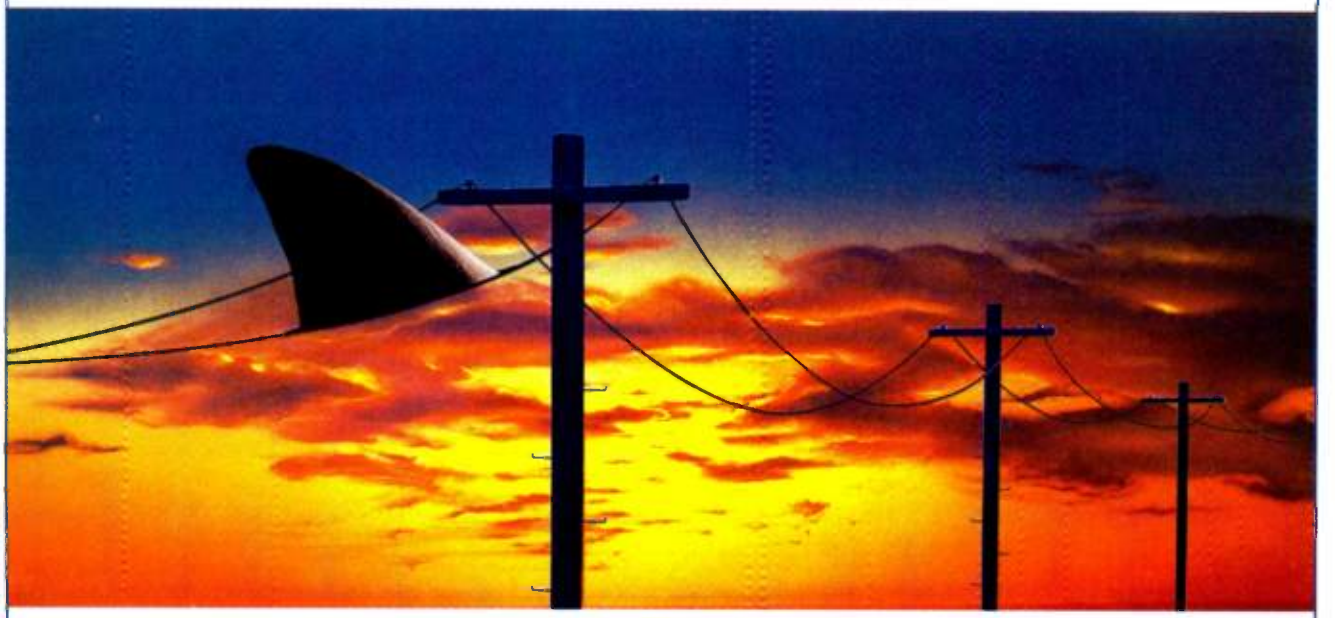

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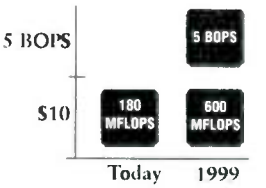

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switching. Designers also gave the Teak core an extended program addressing space, new instructions to accelerate the performance of various DSP algorithms, and enhanced support for operating systems. The various enhancements to the cores make them well-suited for telecommunications applications.

Lucent's DSP16000 was actually released before the Teak, and perhaps laid the ground work for the dual-MAC computation unit developed by the DSP Group. The instruction set of the DSP16000 core is backward source-code compatibility with the company's DSP1600 family. To take on more complex applications, however, the DSP16000 core also includes a mixed 16/32-bit instruction-set architecture, a 20-bit unified linear address space, and an on-chip cache. The cache reduces system power by minimizing external bus accesses. Unlike the DSP Group, which only licenses the core, Lucent has the core in its ASIC library. It also offers a standalone chip, the DSP16210, which is based on 0.35-µm design rules, and has 10-ns instruction cycle time when operating from a 3-V supply *(Fig. 2)*. The chip designers included 60 kwords of dual-port RAM to support downloadable system software (a key capability to support field upgrades), and 8 kwords of ROM to hold the boot code and development support code.

The external memory interface supports asynchronous or synchronous static RAMs, and 16- or 32-bit memory interfaces. In addition to the dual MACs, the DSP core includes a bit-manipulation unit and a three-input, 40-bit ALU. It also has add/compare/select logic that enhances signal coding efficiency and Viterbi acceleration. Additionally, a 31-instruction by 32-bit interruptable Do-Loop cache supports zero-overhead looping.

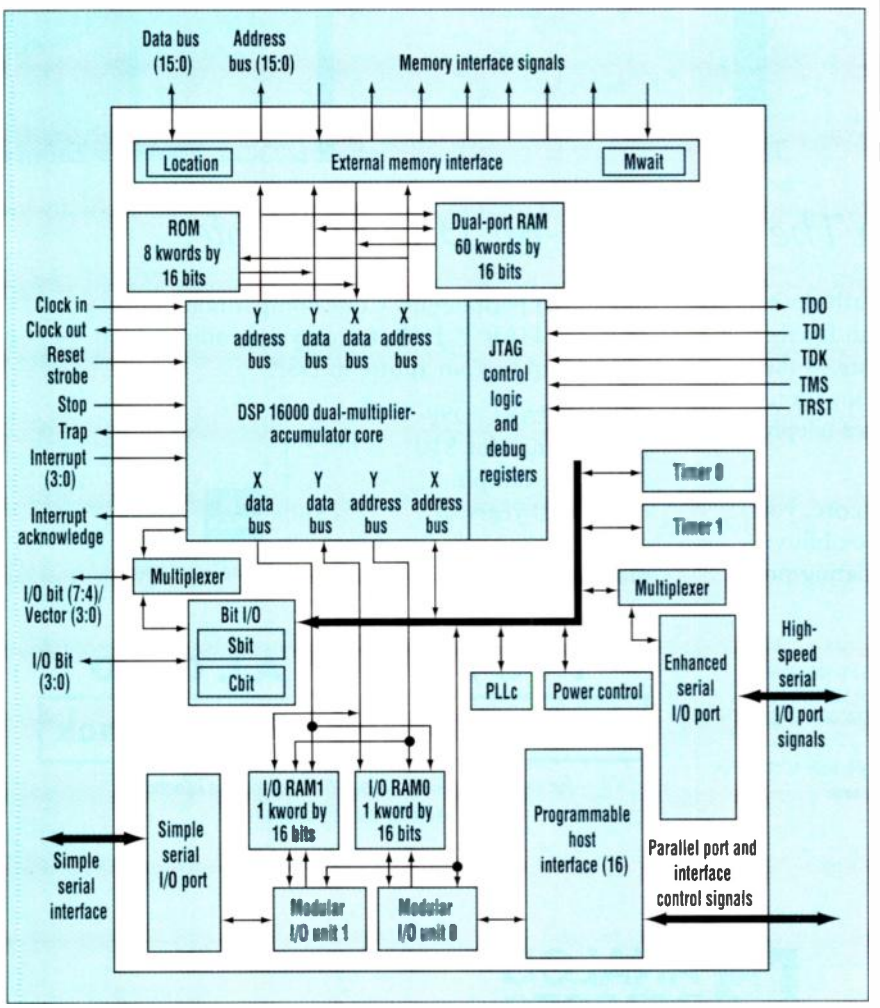
Also on the chip are a high-speed serial port that handles transfers at rates of up to 25 Mbits/s, and a pair of dedicated DMA controllers that off-load I/O processing from the DSP core. Both JTAG and a full-speed emulation system are incorporated to ease system testing and software debugging.

The just-released Carmel architecture from Siemens provides designers with the option of mixing both a standard instruction set and a user-definable instruction set. Available as a core, the Carmel architecture combines an enhanced, customizable, long-instruction-word capability along with a modular, superscalar architecture that allows designers to allocate DSP power where needed. The 16-bit integer, fixed-point core can execute 120 M MIPS (multiple millions of instructions per second) when clocked at 120 MHz and powered by a 2.5-V supply

The long instruction word allows the chip to perform up to 15 operations in parallel because it packs dual ALUs, a dual multiplier-accumulator, and a multiple-bus architecture. The architecture allows multiple simultaneous transfers for high data bandwidth. Peak throughput of the core is 15 times 120 MHz, or approximately 1800 MIPS.

Adding multiple arithmetic units to perform parallel processing isn't a new concept for DSP, but until recently it has not been an option for low-cost chips. One company that is developing a scalable DSP capability for integer DSP operations, ZSP Inc, recently unveiled a parallel processing architecture and a series of one-, two-, or four-engine processor chips that will deliver 400 MIPS per chip. That's two to 10 times the MIPS available from most commodity DSP chips *(Electronic Design, Feb. 9, 1998, p. 37)*.

The 10X DSP architecture consists of a scalar processing engine with a five-stage pipeline and dual multiplier-accumulator units. One, two, or four of these engines are then combined on a



2. The DSP16000 core used in the DSP16210 DSP chip from Lucent Technologies also employs dual multiplier-accumulator units. A large, dual-port RAM and an 8-kword by 16-bit ROM provide plenty of local storage. The chip includes a high-speed serial interface; several timers; a 16-bit parallel I/O port; and full-speed, in-circuit emulation capability to speed debugging.

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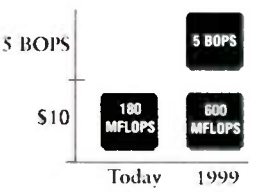

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single chip. The dual MAC can perform either two 16-bit multiply-accumulates, or one double-precision, multiply-accumulate operation in a single cycle. All functional units share a common register file that consists of 16 16-bit registers. That file serves as a source and destination for MAC operands, and keeps the compiler structure simple for efficient coding.

The first chip out, the ZSP16401, has four functional units and the register file, as well as 48 kwords (96 kbytes) of high-speed SRAM. A rich set of on-chip peripherals, including a non-cycle-stealing DMA controller, provides a flexible interface and fast I/O. First versions will employ a 0.35-µm process, but future devices will use 0.25-µm design rules and operate at speeds of up to 200 MHz.

More targeted solutions like a digital-filter processor from ITT Intermetall, take on audio and speech applications by offering two variants—the ASCO2300 for audio applications and the SPC2350/2360 for voice processing.

And, taking aim at cost-sensitive applications, designers at Analog Devices have trimmed back the 32-bit SHARC DSP architecture to cut the DSP chip cost to less than $10 in quantities of 100,000 units. The ADSP-21065L performs both integer or floating-point operations. It delivers a peak throughput of 180 MFLOPS (120 MFLOPS, sustained) or 60 MIPS, which designers estimate is about three times the throughput of comparably priced DSP chips from other suppliers. In addition to the high-performance arithmetic units, the DSP chip packs 544 kbits of SRAM, eight serial-port DMA channels, 12 programmable I/O pins, and an SDRAM controller to connect the chip to a large, but low-cost external memory.

Both Motorola and Texas Instruments have recently introduced low-cost DSP/controller chips. In the case of TI, the chip is a unified controller-DSP engine that will form the basis for a family of chips known as the TMS320C27x series. Motorola, on the other hand, crafted a standalone DSP chip targeted at high-end audio applications, the DSP56362. The chip delivers a throughput of about 100 MIPS. It includes algorithms to handle all popular audio decoding standards in a single device, as well as other audio processing requirements such as subwoofer management, soundfield effects, 3D virtual surrounds, equalization, Lucasfilm THX Cinema processing, and Pacific Microsonics HDCD. And, it will cost less than $20 in lots of 10,000 units.

Motorola has also that designed a dual-core DSP/controller chip that will be sampled this quarter. The chip combines an M-Core controller and a 56100-class DSP engine on a single chip with a unique memory interface block that allows each engine to run its optimum speed.

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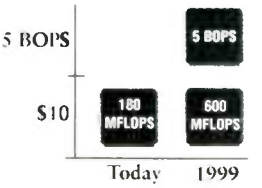

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A Better Understanding Of Memory Accesses Allows DSP Memory Subsystems To Be Better Matched To The DSP Chips.

Richard Jaenicke and Paul Taddonio,
SKY Computers Inc., 27 Industrial, Chelmsford, MA 01824;
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Designers are increasingly using multiple DSP chips in applications that contain huge data sets—tens to hundreds of megabytes. Such applications can no longer be economically implemented with static RAMs, most of which typically have maximum capacities of 512 kbytes. Consequently, many system designers must consider the use of dynamic RAMs (DRAMs) to provide the larger memory space. Most DRAMs, however, are designed for PC workstations. To optimize DRAM use in DSP applications, designers must select the correct DRAM technology based on a different set of goals.

In addition, most DSP chips are optimized for I/O handing, and that typically means an interface optimized for use with SRAMs. As a result, overall memory subsystem performance in a DSP application depends on both the memory technology and the DSP chip's external interface.

Designers can pick from several DRAM architectures, each of which brings a number of pros and cons for various DSP system implementations. Thus, a better understanding of DRAM architectures and the DSP memory interface will allow designers to better optimize the memory subsystem for multiprocessor DSP applications.

On PCs, short read bursts for instruction cache-line fills have dominated accesses to main memory. But the increasing use of object-oriented languages and multitasking operating systems on PCs has lead to a significant number of accesses that are dispersed throughout main memory. This, in turn, has lead to an increasing emphasis on random-access latency instead of solely on burst-access time for subsequent reads to an open DRAM page.

Due to the emphasis on random-access latency, many PC manufacturers were slow to replace EDO (extended data out) DRAMs with synchronous DRAM (SDRAM) technology, which emphasizes burst accesses. In a typical 66-MHz memory implementation, SDRAM adds a cycle of latency on the initial access in exchange for one less cycle on each of the subsequent accesses. For a four-clock burst the net result is a two-cycle savings, but that is only relevant if more than just the first fetch was needed.

Differing Emphasis

In a DSP system, the speed of instruction loads is generally not the main concern. Signals are typically processed as vectors, which are many times the length of the data cache line. The code for the tight inner loops of signal processing is typically loaded once for a long vector of data. The emphasis, therefore, is on the speed of both the subsequent reads to the same cache line

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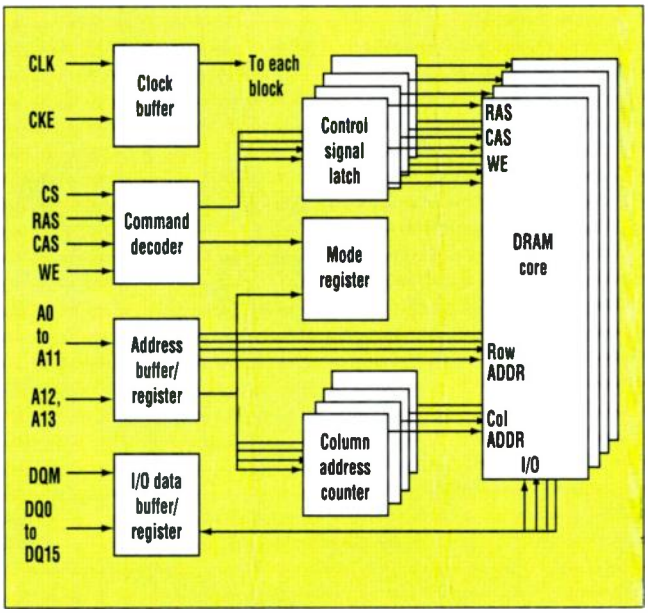
and for immediate access to sequential memory locations.

The workhorse dynamic memories like standard fast-page mode (FPM) DRAMs, EDO DRAMs, and burst-EDO DRAMs are basically the same, save for some differences in the interface for reading data out at the time of the column access strobe (CAS) signal. With FPM DRAMs, the CAS signal causes data to be read directly from the sense amplifiers. EDO DRAMs add a latch to the output of those sense amplifiers, which allows the data-output buffers to stay on even after the rising edge of CAS. The result is a faster cycle time from column address to column address—up to a third faster than standard FPM DRAMs.



1. The multibank DRAM core in a typical synchronous DRAM allows the memory to access one bank while precharging the others so that data can be quickly accessed.

Burst-EDO DRAMs replace the output latch on the EDO DRAM with a register. That adds an internal pipeline stage, which allows data within a burst to come out quicker after the CAS signal for the second and subsequent accesses in the burst. The trade-off is an extra pipeline stage for the CAS signal on the first access, but this does not lower performance because the first data access is limited by the row access strobe (RAS) time, not the CAS time.

SDRAMs present more of an architectural change from FPM DRAMs than do the EDO DRAM variations. From the DSP system designer's standpoint, the important differences are that SDRAMs are synchronous and use a clock input. An internal SDRAM divides the memory into multiple banks, each with its own row decoder and sense amps. Current high-performance SDRAMs use four internal memory banks, although earlier versions typically used two banks *(Fig. 1)*.

The multibank architecture eliminates gaps between data accesses because data can be accessed from one bank while the others are precharging. The SDRAMs buffer both inputs and outputs, and that does affect the latency for the first access in a burst. The increased pipelining, though, enables both quicker access to a full burst and operation at higher frequencies, compared to EDO DRAMs.

As a result, one of the key performance issues becomes how the system can deal with pipelined memory operations. The highest memory-to-processor throughput is achieved by using the multiple accesses inherent in the bursts of a cache line load. If that approach isn't used, the access rate is limited by the speed of the address bus, which usually has a duty cycle of only a percentage of the data bus. To reach the full potential of pipelined memory systems, the pipeline should be full as long as possible. Like a pump that needs priming, the data through a pipelined memory system will incur startup latency after any time the pipeline stalls. Accessing long vectors typically used in signal processing data arrays helps keep the pipeline full.

Match Latency To Pipeline

When evaluating the various memory technologies for use in DSP systems, the designer should match each technology to the processor's capabilities. That is, the latency of the memory subsystem should be matched to the pipeline capabilities of the processor. The more pipelining in the processor, the higher the latency it can tolerate in the memory and the memory controller without affecting throughput.

However, many DSP chips do not support pipelined memory accesses, while other architectures support pipelining by using a separate DMA engine. In some applications, RISC processors can be used to execute DSP algorithms. Some RISC CPUs support pipelining, but even those are optimized to deal with alternating instruction and data accesses. Such a simplified design can work well on general-purpose applications that have an unstructured mix of instruction and data transfers, but it is not of much benefit for DSP applications. Unrestricted data pipelining delivers the most benefit in DSP applications, and this capability is available in some high-end RISC chips.

Additional considerations affect memory-access latency in RISC processors. For example, some high-end processors support a feature called "late cancellation," which allows a memory access to be canceled the cycle after the acknowledgment is sent by the memory controller. Late cancellation can be useful to support either an error-correcting (ECC) memory implementation or a cache coherency protocol. To implement this feature, however, the processor must have an additional one-cycle internal latency. If ECC and cache coherency are not needed, overall latency can be reduced by turning this feature off.

In addition to the processor's external memory interface and the DRAM itself, the memory controller is the third component that greatly affects the latency and throughput in the memory subsystem. The latency through a memory controller is mostly affected by the technology of the components. For absolute speed, an ASIC is the best choice; however, FPGAs are good alternatives to meet demands of flexibility and shortened time to market. FPGAs also are amenable to a pipelined implementation due to the abundance of flip-flops

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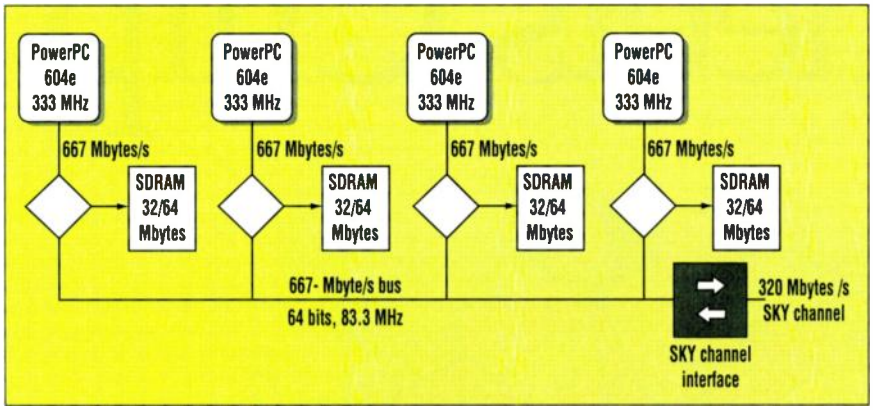


2. A quad-processor module, based on the PowerPC RISC processor, can be constructed with each processor having its own local SDRAM memory and communicating via a high-speed on-board bus that can transfer data at 667 Mbytes/s. The board ties into the rest of the system via the ANSI standard SKYchannel interface, which transfers data at 320 Mbytes/s.

in their architecture.

FPGAs provide the flexibility to design the exact controller features and behavior desired, such as the page handling algorithm, and they are relatively fast, with the latest crop claiming to support 90-MHz and faster pipelines. Such pipeline speeds should be sufficient to keep pace with most of the highest-speed RISC processors, which operate with bus interface speeds of 83.3 MHz. Once the design has been debugged, it is relatively easy to turn an FPGA into an ASIC. And, although converting the FPGA to an ASIC will not remove any of the stages of the latency without a redesign, it will permit the circuits to operate at higher clock frequencies while reducing system cost.

When they use SDRAMs, designers must decide how the memory controller will handle the open pages of the multiple internal banks. One technique is to treat data from each of the memory banks as four independent open pages. This architecture can present four separate memory buffers to the application. The results from operating on two vectors in two different buffers could be placed in a third vector in the third buffer.

One disadvantage to this approach is that it places a greater burden on the software. Each vector must be placed in a different buffer to get maximum throughput. The manipulation required to do this for a long chain of vector operations is not an easy task and, in fact, may be impossible.

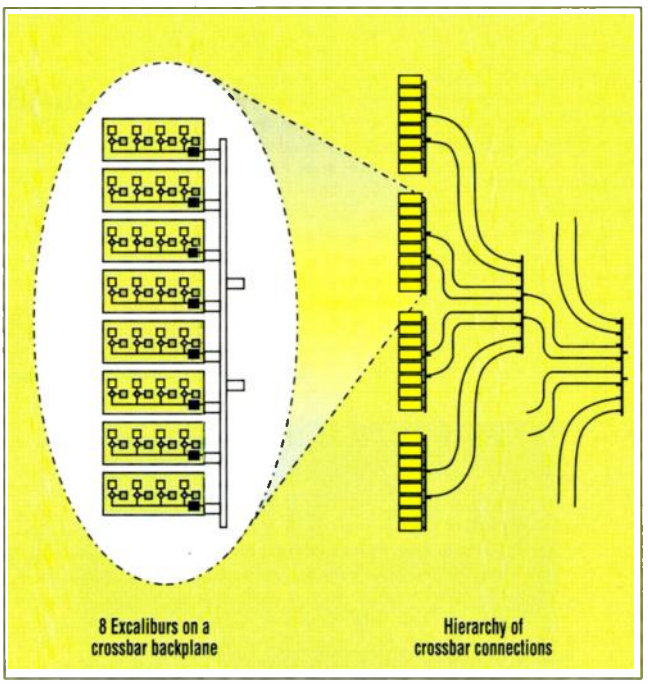
An alternative option is to present one big open page that covers all the internal banks. Accesses, though, will still be interleaved at the cache-line level. Not only will this arrangement be simpler to program, it also will provide better performance for strided accesses. Strided accesses would stay within a larger page for a larger number of accesses. The final benefit is a simplified design for the memory controller compared to managing four open pages, and that would have a direct impact on improving the time to market.

Finally, most DSP designs are size limited. In addition to reserving space for the processor, DRAMs, and memory controller, designers must allow for line terminations as well. For example, a multiprocessor board with four processors, each with a 64-bit external interface, has 256 data lines that would need to be terminated on each end. For many implementations, the space required to place 256 resistors on a board is prohibitive.

The best option could be to choose bus interface devices that include output resistors. If such parts are not available, transceivers are another option. In many memory bus implementations, however, the physical placement constraint would cause the drivers to be spread too far apart, and ringing on the signal lines would result. Ringing, though, can be controlled without termination by minimizing line lengths and choosing drivers that match the particular line characteristics. Such a design is possible, even at speeds over 80 MHz, but only after performing a thorough signal-integrity analysis.

Engineers can create multiprocessor DSP systems using optimized building blocks containing the processor, memory, and memory controller. Designing such a system becomes an exercise in optimizing data transfers between processors and memory, and between two memories. Ideally, the interface to remote memory should have the same features and performance as for local memory.

Available interconnect technology is typically a factor of two to four times slower than current memory buses, so the design must be optimized for



3. The SKYchannel communication architecture allows up to 4096 chassis in a single system. In this example, eight Excalibur multiprocessor boards are connected to a crossbar backplane, which is itself connected to multiple backplanes by a hierarchy of crossbars.

LINEAR TECHNOLOGY

DESIGN NOTES

A High Efficiency 500kHz, 4.5A Step-Down Converter in an SO-8 Package – Design Note 181

Karl Edwards

Reducing board space and improving efficiency are key requirements in many systems, especially at higher currents, where component size and power losses generally increase. Linear Technology has addressed these issues with the new LT®1374, a 500kHz, 4.5A monolithic buck converter designed to meet the needs of higher current applications. The LT1374 contains the power switch, logic, oscillator and all the control circuitry necessary to make a compact, high efficiency buck converter. The topology is current mode for fast transient response and good loop stability, with the added benefit of full cycle-by-cycle current limit.

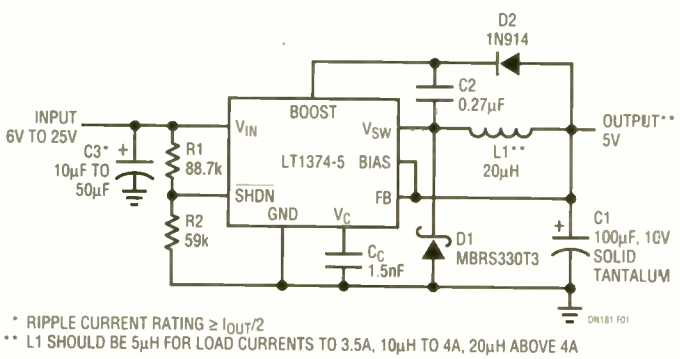
The device is available in three package options: SO-8, DD and TO-220. For the most space-sensitive applications, the SO-8 retains the full 4.5A switch rating and is ideal for medium power applications with high peak loads. The DD package is intended for surface mount applications with continuous high current; the TO-220 is for high power, high ambient temperature systems.

A switching frequency of 500kHz allows the use of small, low value surface mount components to reduce board area. To further reduce power consumption, the LT1374 has two shutdown modes. A precise 2.38V threshold on the shutdown ($\overline{SHDN}$) pin keeps the internal reference alive but disables switching. This mode can be used as an accurate input undervoltage lockout, as shown in Figure 1. Grounding the $\overline{SHDN}$ pin takes the part into complete shutdown, reducing supply current to only 20µA.

For noise-sensitive applications, the $\overline{SHDN}$ pin can be replaced by SYNC (LT1374-SYNC), enabling the internal oscillator to be synchronized to an external system clock in the range of 580kHz to 1MHz. Both adjustable and fixed 5V output voltage parts are available. The LT1374, together with a minimum of small surface mount components, produces a 4.5A step-down regulator that is efficient in both power and board space.

High Efficiency, 25V, 0.07Ω Switch

High efficiency is the result of a fast bipolar process and a unique transistor layout that produces a high voltage switch with only 0.07Ω typical on-resistance. This permits the LT1374 to operate over an input voltage range of 5.5V to 25V with switch currents up to 4.5A. Figure 1 shows an example of the LT1374-5 in a typical 5V output step-down application. Efficiency for a 10V input is shown in Figure 2. Note that efficiency remains at over 88% from 0.5A up to the circuit's maximum 4A load current.



* RIPPLE CURRENT RATING ≥ $I_{OUT}/2$

** L1 SHOULD BE 5µH FOR LOAD CURRENTS TO 3.5A, 10µH TO 4A, 20µH ABOVE 4A

Figure 1. 5V Buck Converter

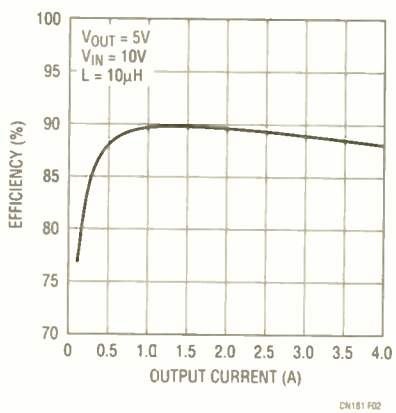


Figure 2. 5V Efficiency vs Output Current

4.5A in an SO-8

The output switch of the LT1374 is designed to minimize power dissipation from both switch resistance and switch drive current. This allows the use of the SO-8 packaged LT1374 in applications that would have previously required a power package, especially when selection is defined by high dynamic load currents. Typical static and dynamic thermal characteristics for various load currents are shown in Figures 3 and 4. These measurements were made in still air with the LT1374 SO-8 placed on a 4in^2 double-sided circuit board. Multiple vias conduct heat from the board's topside to a continuous copper plane on the bottom side. A typical application for the SO-8 package is supplying a motor driver. The motor may require 4A at start-up but only 2.5A when running. With a 60°C ambient temperature, the SO-8 package can provide 4A of load current for up to seven seconds, followed by 2.5A of continuous current. If 4A of continuous current were required, the surface mount DD package (θ_{JA} = 30°C/W) could be used; for even higher power, use the TO-220 (θ_{JC} = 4°C/W).

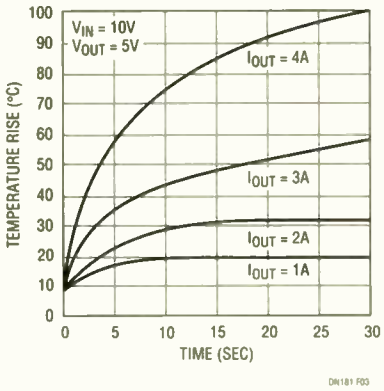


Figure 3. Temperature Rise vs Time

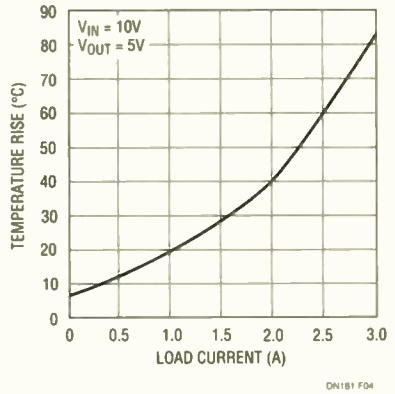
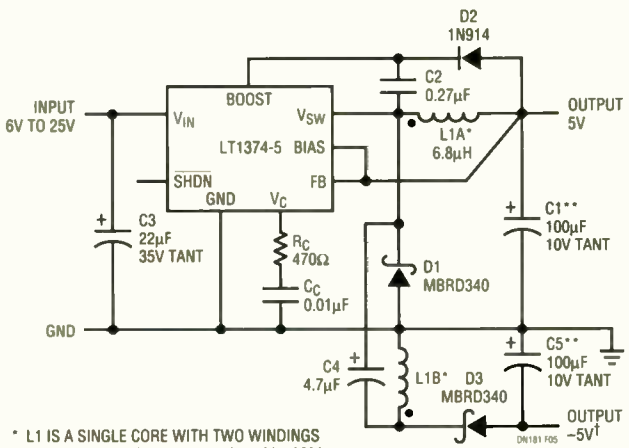


Figure 4. Temperature Rise vs Load Current

Dual Output SEPIC Converter

The circuit in Figure 5 generates both positive and negative 5V outputs from two windings on a single core. The converter for the 5V output is a standard buck converter. The –5V topology would be a simple flyback winding coupled to the buck converter if C4 were not present. C4 creates a SEPIC (single-ended primary inductance converter) topology, which improves regulation and reduces ripple current in L1. Without C4, the voltage swing on L1B compared to L1A would vary due to relative loading and coupling losses. C4 provides a low impedance path to maintain an equal voltage swing in L1B, improving regulation. In a flyback converter, during switch on-time, all the converter's energy is stored in L1A only, since no current flows in L1B. At switch off, energy is transferred by magnetic coupling into L1B, powering the –5V rail. C4 pulls L1B positive during switch on-time, causing current to flow and energy to build in L1B and C4. At switch off, the energy stored in both L1B and C4 supplies the –5V rail. This reduces the current in L1A and changes L1B's current waveform from square to triangular.



* L1 IS A SINGLE CORE WITH TWO WINDINGS
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† IF LOAD CAN GO TO ZERO, AN OPTIONAL PRELOAD OF 1k TO 5k MAY BE USED TO IMPROVE LOAD REGULATION

Figure 5. Dual Output SEPIC Converter

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the difference in performance. One popular approach is to use multiple levels of interconnection that vary by distance. This approach provides very high bandwidth where possible for nearby processors and memory, while using standard interconnects for more distant connections.

For neighboring processors and memories on the same printed-circuit board, the full local memory bandwidth should be achievable. For example, a 64-bit, 83.3-MHz connection can be used to connect a set of four processors and memories *(Fig. 2)*. At those frequencies, using a bus to make the connection can be problematic. A better approach would be to make point-to-point connections using a multiported switch. One port on the switch should be connected to the interconnect used between boards.

The interconnect should minimize the funneling effect of going from the neighborhood connections to the interboard connections. This implies choosing a high bandwidth per connection, and using very high-speed FIFOs to decouple the two bus speeds. A DMA engine at the interface to the interconnect will prevent a fast processor from waiting for the interconnect transfer to complete.

Real-World Example

How does all this come together in the real world? Let's examine the high-performance memory architecture for DSP applications employed in the Excalibur PowerPC daughtercard from SKY Computers. On the daughtercard, each of four PowerPC processors is connected to its own local SDRAM by an 83.3-MHz interconnect *(Fig. 2, again)*. The memory controllers also are connected to each other at the same 83.3-MHz rate, so any processor can access any memory on the daughtercard at the same raw bandwidth.

PowerPC processors were chosen primarily for the sustained throughput of their external interface, including the raw bandwidth and the pipelining capabilities. Different PowerPC processors have different pipelining capabilities, as well as being available with different maximum CPU core frequencies. The Excalibur card can be implemented with different processors to take advantage of those various combinations as they change over time.

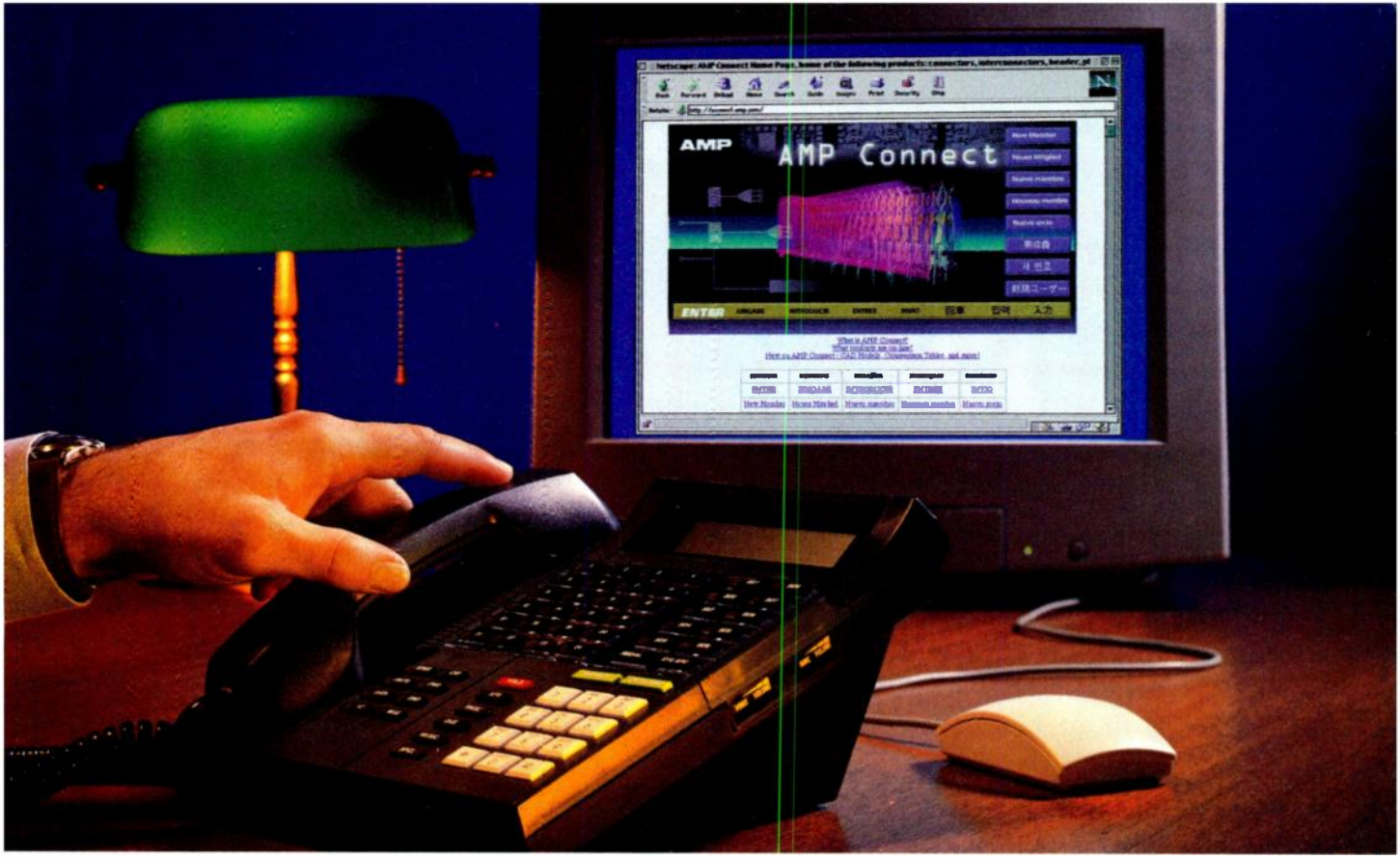
The current top performer is the 333-MHz PowerPC 604e. It allows three memory accesses to be pipelined, enabling single-cycle throughput for subsequent loads from the same cache line. The 604e also has a feature called "streaming," which allows subsequent cache line loads to occur without a gap. The result: a sustained memory access pattern for data reads of "... 1111 1111 1111 ..." Therefore, the sustained performance in this case is the same as the theoretical peak performance.

The memory controllers on Excalibur also can access the interface to the SKYchannel interconnect. The ANSI-standard SKYchannel Packet Bus (ANSI/VITA 10-1995) provides a 320-Mbyte/s connection to all the other daughtercards in the system. Multichassis systems as large as 4096 units are possible using SKYchannel *(Fig. 3)*. Achieving the highest performance for multiprocessor DSP applications thus requires a global optimization of processors, memory technology, controller design, and multiprocessor interconnect.

When SDRAMs are combined with processors that support pipelining, they can provide sustained memory accesses at 667 Mbytes/s, while providing hundreds of megabytes of storage capacity. This combination of speed and capacity is critical for DSP applications with large data sets.

Richard Jaenicke is director of marketing at SKY Computers Inc., Chelmsford, Mass. He received his BA in Computer Science from Dartmouth College, Hanover, N.H. and his MS in Computer Engineering from Rensselaer Polytechnic Institute, Troy N.Y..

Paul Taddonio is a senior hardware engineer at SKY Computers. He received a BSEE from Rensselaer Polytechnic Institute.



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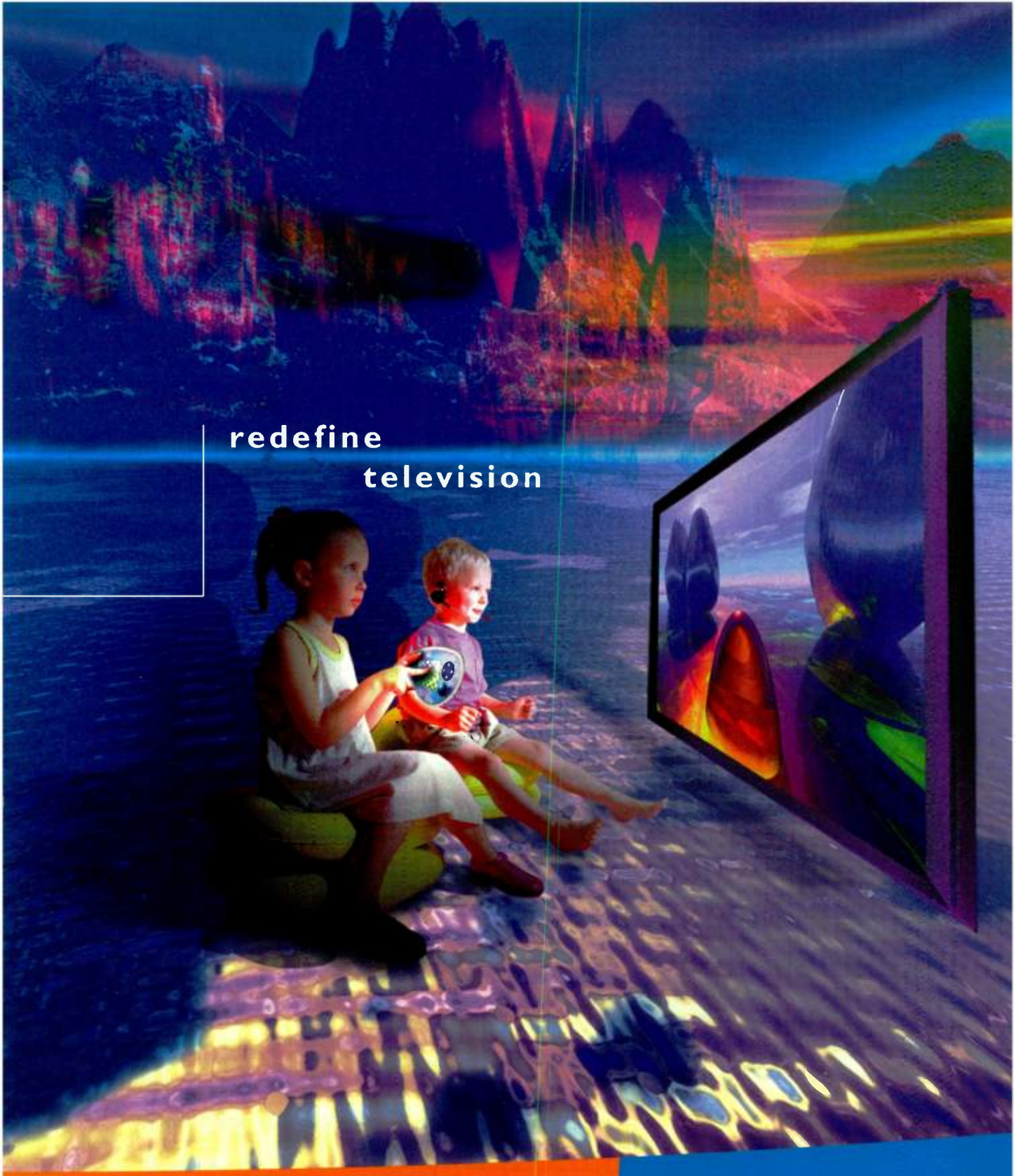

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Major home appliance manufacturers are always adding new features and simplifying the use of their products in order to maintain a competitive edge. New designs also are influenced by current and pending government regulations on energy efficiency and water usage. In many major appliances, advanced three-phase variable speed drive systems provide the performance improvements needed to meet these demands.

Designing fractional horsepower drives for home appliances such as refrigerators and washing machines presents some interesting technical challenges. As a result, manufacturers are turning to a digital-signal processing (DSP) control platform. The following applications show how DSP motor control designs are implemented in two different home appliances.

Home Refrigerator Control

A home refrigerator runs continuously and, therefore, consumes a significant amount of electricity. Since the main power consuming element is the compressor, appliance manufacturers are always looking to improve its cooling efficiency.

Designers can boost efficiency by reducing the speed of the compressor to match the cooling required for normal refrigeration operation. High-speed operation is reserved only for rapid cooling whenever the refrigerator is filled with food. The more simple control methods for single-phase induction motors result in a significant loss in efficiency of the motor. For fractional horsepower applications, the motor with the highest efficiency is an electronically controlled three-phase permanent magnet motor.

In domestic refrigeration systems, the compressor and motor are hermetically sealed within the same metal enclosure. The environment within the chamber is quite harsh, so Hall sensors can't be used. These sensors are typically used in other low-cost permanent magnet drives. As a result, a sensorless mode of operation where the motor acts as its own commutation sensor is essential.

Consequently, the target for a refrigeration application is to provide a drive for a 200-W compressor motor, without sensors, at minimum size and cost, and meeting all the regulatory requirements for electromagnetic compatibility (EMC) and safety.

Motor Control Strategy

A permanent-magnet motor is the most efficient ac motor type. It doesn't require rotor magnetizing current as does an induction motor. However, to run an ac motor efficiently, it is important to synchronize the frequency of the applied voltage with the position of the permanent-magnet rotor. An effective control scheme is to run the motor in a six-step commutation mode with only two windings active at any one time. In this case, the back emf on the unconnected winding is a direct indica-

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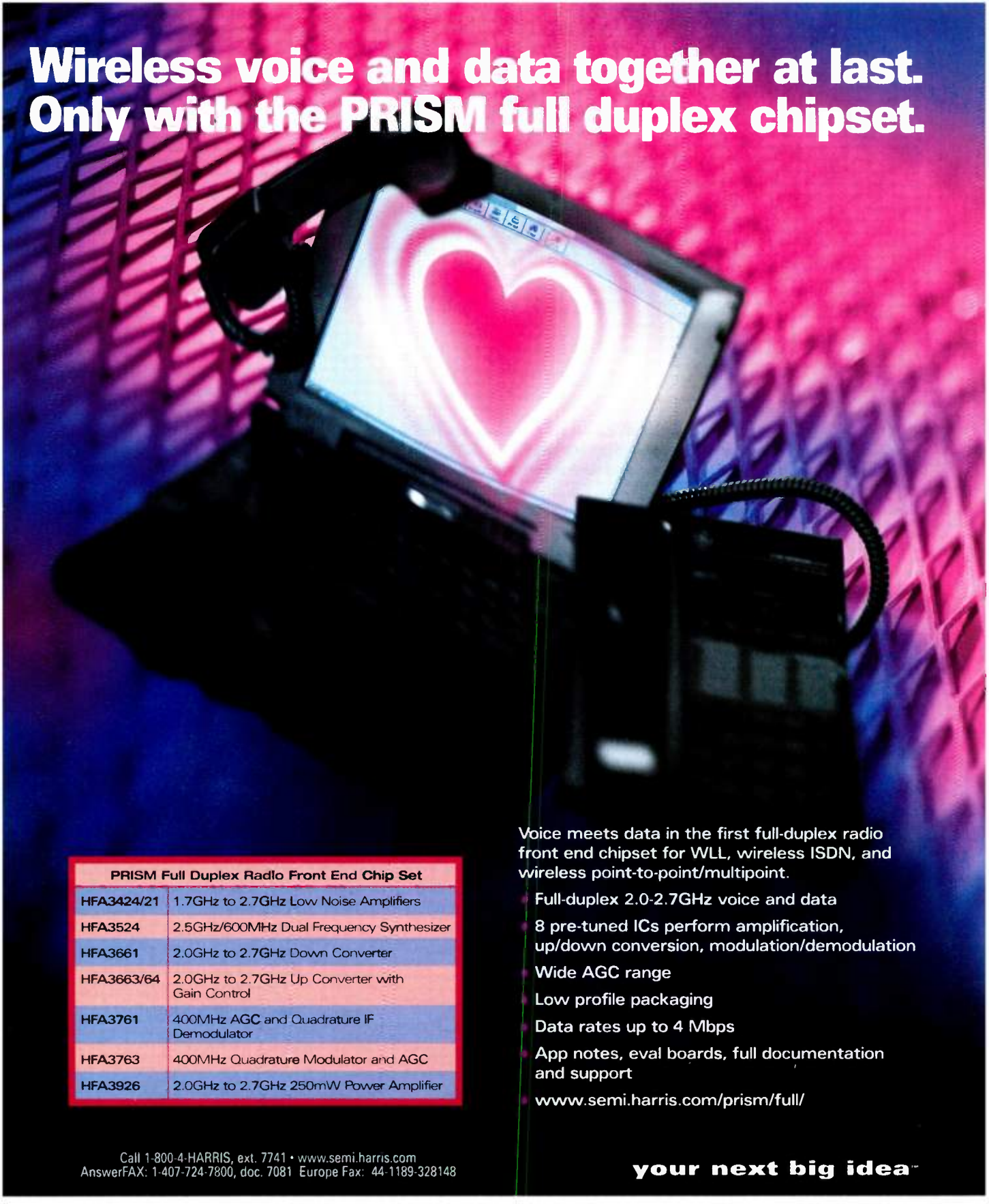

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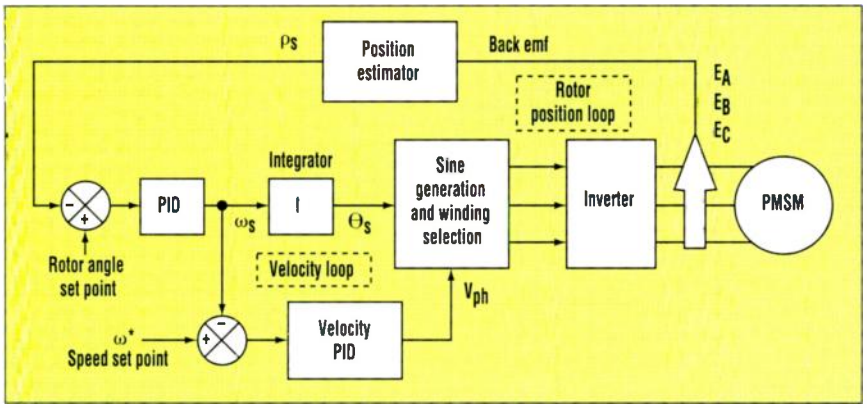


1. This sensorless control system for a permanent-magnet synchronous motor (PMSM) in a refridgerator can bring the compressor up to speed in a few seconds and maintain the target speed within 1%. In addition, the smooth running of the compressor reduces audible noise.

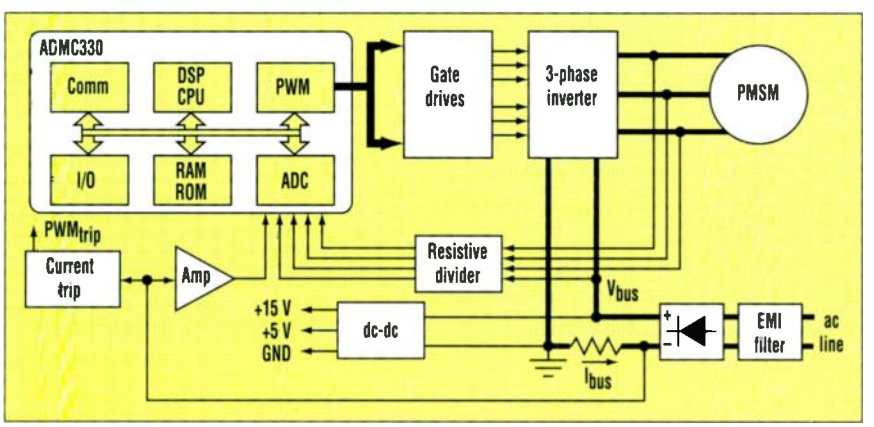
tion of the rotor position. This position is estimated by matching a set of back emf waveform samples to the correct segment of the stored waveform profile. This technique averages the data from a large number of samples giving a high degree of noise immunity.

The control system has an inner position control loop (Fig. 1). This adjusts the angle (qs) of the applied stator field to keep the rotor synchronized. The integrator input tracks the motor velocity when the rotor position error is forced to zero. The outer velocity loop adjusts the applied stator voltage magnitude to maintain the required velocity. The controller can accelerate the compressor to its target speed within a few seconds and can regulate speed to within 1% of its target. The smooth running of the compressor reduces audible noise. The lower operating speed helps minimize the temperature cycles in the refrigeration compartment, and improves the quality of food refrigeration.

The complete drive system includes the EMI filter, the input rectifier, the control power supply, the DSP motor control circuit, the signal conditioning circuits, the power inverter, and gate drives (Fig. 2).

ADC Checks Currents, Voltages

Upon power-up, the internal program RAM inside the controller IC is loaded from an 8-pin external boot ROM via one of the serial ports. The control program performs initialization and diagnostics and then starts the motor in an open-loop mode. When the back emf reaches a minimum level, the motor is switched to normal running mode. During every PWM cycle the analog-to-digital converter (ADC) samples the motor back emf, the motor current, and the bus voltage.



2. The complete PMSM control drive system includes an EMI filter in order to meet regulations for eliminating electromagnetic interference. The system's power stage employs a full three-phase MOSFET power inverter bridge and three integrated gate drive amplifiers.

An internal multiplexer selects the appropriate back emf signal to be converted. The DSP CPU calculates a new rotor position estimate and calculates the PWM duty cycle needed to apply the required voltage to the motor. At particular values of estimated rotor position angle, the CPU selects a new set of active motor windings by writing to the PWM segment selection register. The CPU also performs diagnostic functions and monitors dc bus voltage, motor current, and speed. In the case of overload conditions, the drive is shut down and a restart is attempted after a short time delay.

The drive power stage consists of a full three-phase MOSFET power inverter bridge and three integrated gate drive amplifiers. The rectifier common is connected to the control IC ground; so the PWM outputs are connected directly to the gate drive inputs. The back emf signal conditioning consists of three matched high-voltage resistive dividers and a passive RC filter. The current amplifier circuit is synchronized to the PWM sampling frequency in a way that it can determine the motor winding current from the dc bus current.

To reach the cost targets demanded by this application, the complete control hardware, including the processor core, memory, PWM, and ADC, was integrated into a single motor control IC. The ADMC330 DSP motor controller is an example of a single-chip DSP device for this application (Fig. 2, again). It has three independent computational units within the CPU section: an arithmetic logic unit (ALU), a multiply and accumulate unit (MAC), and a shifter unit.

The memory-mapped PWM controller requires only three register writes per PWM cycle to control the motor winding voltages. This minimizes the processor overhead in generating PWM signals. The ADC is synchronized to the PWM frequency, producing four updated samples every PWM cycle.

The other elements of the drive solution include the control power supply and the EMC components to meet all the regulatory requirements. The compact power supply design derives the +15 V and +5 V supplies from the 300-V supply using a two-stage buck converter, thus avoiding the use of a bulky

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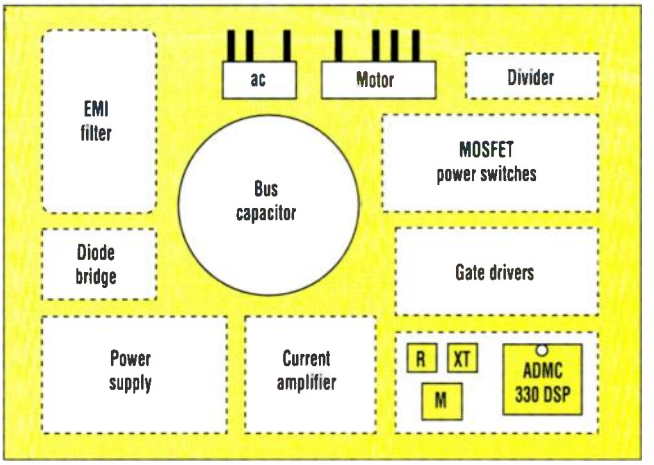
The complete motor drive system is integrated onto a single control card (Fig. 3). The major challenges were in minimization of the control board size and manufacturing costs. The minimum size constraint on the board meant that the DSP motor control IC was placed within 2 inches of a MOSFET power inverter switching currents greater than 1A from a 300-V bus. For this reason, special attention was placed on the power circuit layout, routing, and grounding in order to prevent any inverter switching noise from coupling into the control circuits. All the high-current-carrying components and tracks are close to the ac power and motor connectors.



3. The major challenges in building the refrigerator motor controller onto a single board were to minimize the board size and manufacturing cost.

Also included are the external components needed to run the IC. These are the power-on reset IC (R), the clock crystal (XT), the boot ROM (M), and an ADC capacitor. The final drive product met the customer cost targets and delivered in a 30% reduction in energy consumption by the compressor compared to a fixed-speed, single-phase motor.

Washing Machine Control

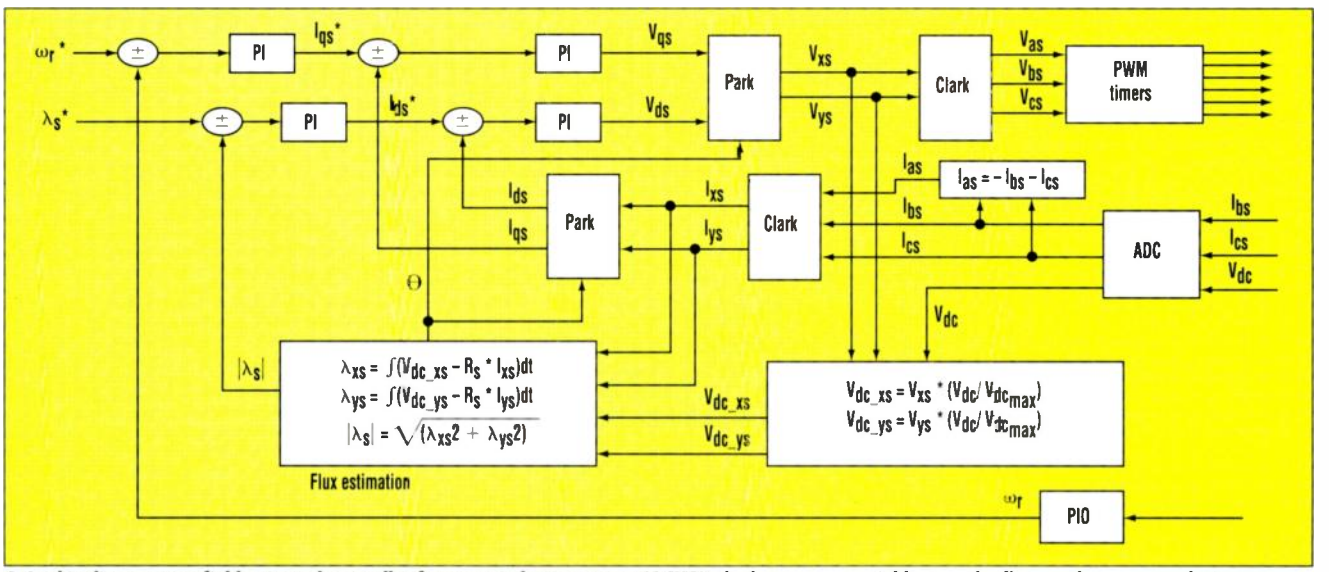
European and Japanese washers are typically horizontal axis machines with a drum driven by a universal brush type motor. Drum speed control can be implemented using a phase controlled rectifier and an 8- or 16-bit microcontroller. However, universal motors have well-known problems of brush wear and limitations on their high-speed range. In contrast, ac induction motors don't use brushes and have a wider speed range.

In this application, the speed ripple and load torque of the washing machine motor provide valuable information on the washing load. The load torque variation with the drum rotation can provide information about the predominant fabric in the wash load. Thus, the machine controller can automatically select the wash program and simplify the use of the machine. The speed ripple can be used to estimate the load unbalance before starting the spin cycle, thereby improving the mechanical reliability of the machine.

Motor Control Strategy

The control of an ac induction motor (ACIM) is potentially much simpler than that required for a permanent-magnet ac motor. Driven in open-loop configuration by a three-phase inverter, the ACIM offers adequate speed-control for many simple pump and fan applications.

However, when a wide speed range and high dynamic performance is required, a field-oriented control scheme is necessary. In this case, the flux- and torque currents are independently controlled to provide a performance similar to that obtainable from a permanent magnet synchronous motor. In the low-speed range of operation the flux is kept constant and torque is directly proportional to the torque current. In the high-speed range, when the motor voltages are limited by the dc bus voltage, the flux is reduced to allow operation at higher speeds.



4. In this direct stator field-oriented controller for an ac induction motor (ACIM), the key motor variables are the flux- and torque-producing components of the motor currents. In this circuit, the Park and Clark reference frame transformation functions calculate the effect of the stator currents and voltages in a reference frame that is synchronized to the rotating stator field.

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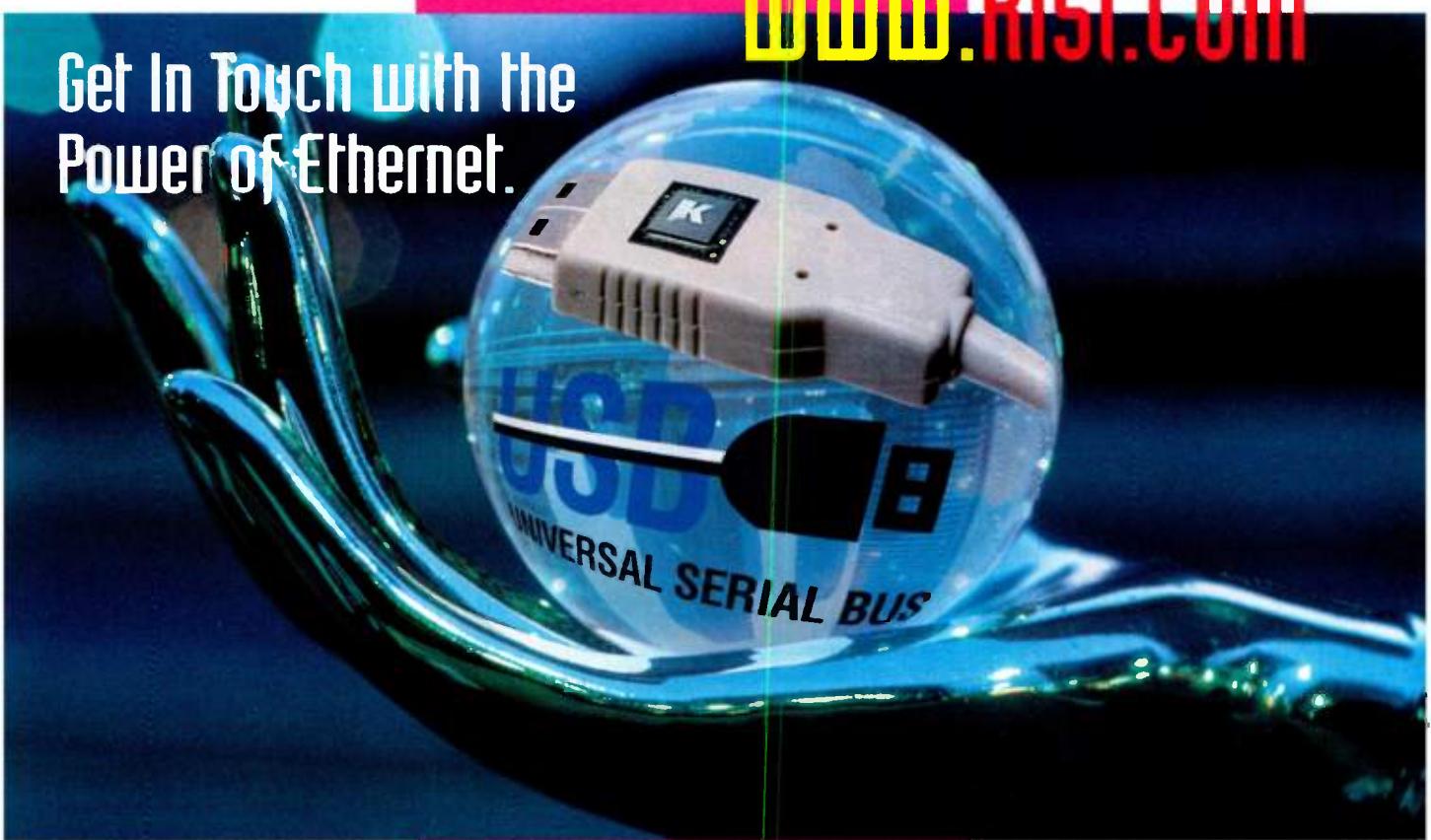

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Shown is a direct stator field-oriented control scheme (Fig. 4). The key motor variables are the flux and torque-producing components of the motor currents. The choice of reference frame is the key element that distinguishes the various vector control approaches from one another. In this scheme, a reference frame synchronized to the rotating stator flux is selected because of the availability of stator current and dc bus voltage information. A number of other field-oriented schemes require position information or stator flux measurements. These are not suitable for this application where controlled operation at close to zero speed is not required.

The Park and Clark reference-frame transformation functions calculate the effect of the stator currents and voltages in a reference frame synchronized to the rotating stator field. This transforms the stator winding currents into two quasi dc currents representing the torque producing (Iqs) and flux producing (Ids) components of the stator current.

The stator flux angle is an essential input for the reference-frame transformations. The stator flux is calculated in the fixed reference frame by integrating the stator winding voltages. In this system, the stator voltage demands to the inverter are known. Therefore, the applied stator voltages can be calculated from the voltage demands and the dc bus voltage measurement. The flux estimation block uses stator current to compensate for the winding resistance drop. The outputs of this block are the stator flux magnitude and the stator flux angle.

There are four closed control loops in this application. Two inner current loops calculate the direct and quadrature stator voltages required to force the desired torque and flux currents. The Park and Clark functions transform these voltages to three ac stator voltage demands in the fixed reference frame. The outer loops are the speed and flux control loops. The flux demand is set to rated flux for below base-speed operation. It is reduced inversely with speed for above base-speed operation in the "field weakening mode." Finally, the torque loop is the same as in any classical motion control system.

Induction Motor Control

The hardware portion of the ac induction motor system is implemented using the same generic variable speed ac drive configuration as the permanent-magnet drive described earlier (Fig. 5). In this case, the motor is rated at over 400 W, so IGBT's are the power devices most suited to the application. The feedback signals include the motor currents, the bus voltage and a pulse train from a digital tachometer. The motor winding current is derived from the power inverter currents. The DSP motor controller calculates velocity by timing the pulse-train frequency from the digital tachometer.

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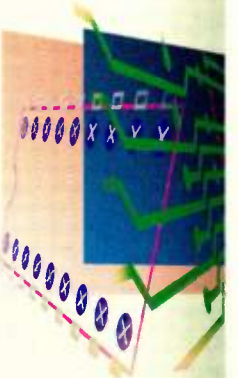

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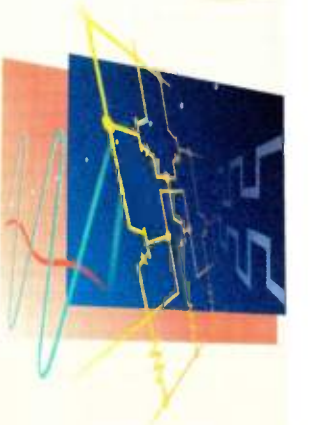

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DSP Control

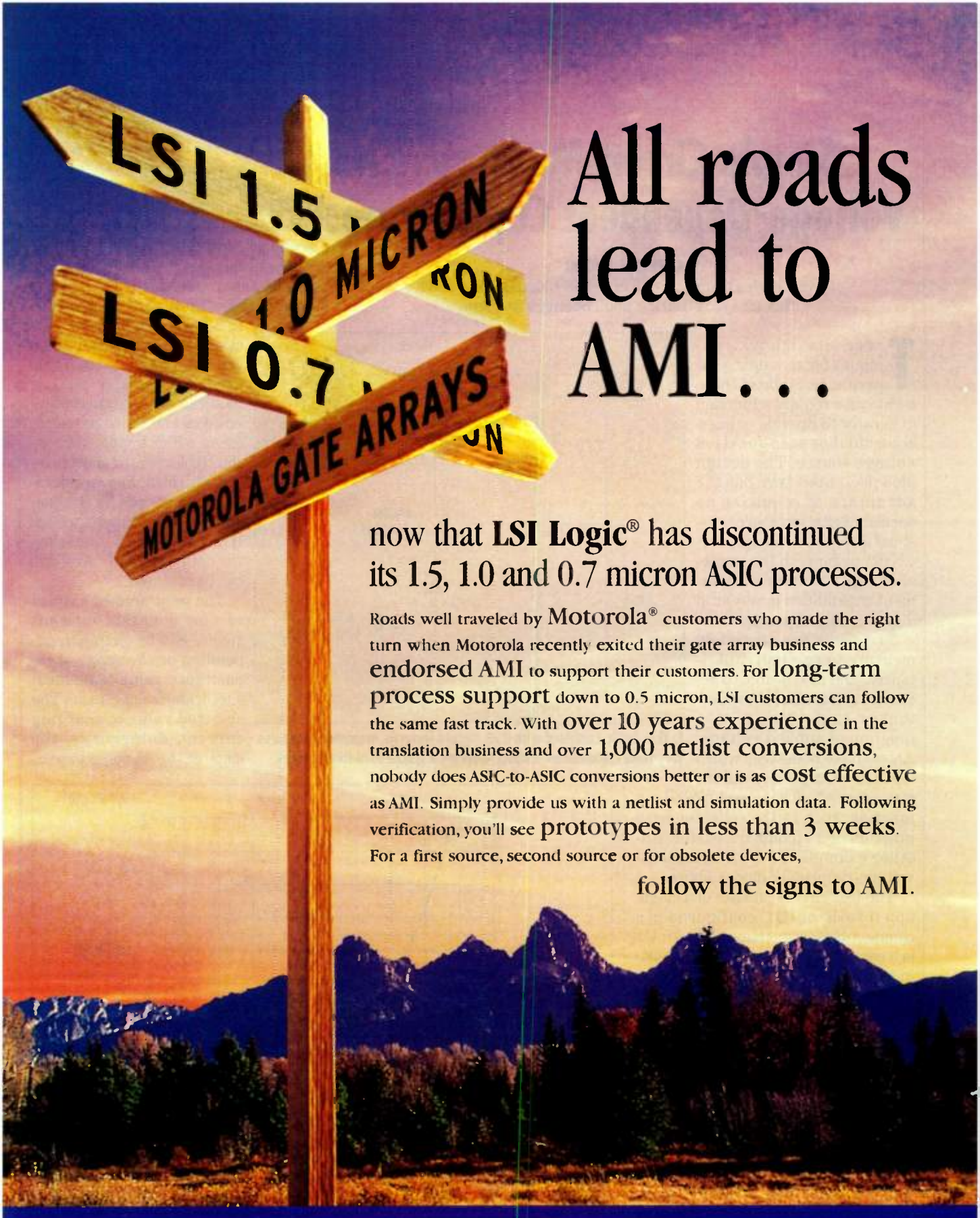
The DSP motor control IC communicates with the front-panel washing machine control over an isolated serial link. This allows speed profile information to be downloaded to the controller, and motor speed and torque information to be uploaded to the washing machine controller

The control software for the washing machine application was developed for an ADMC331 motor control IC. The challenge for this controller was to run four simultaneous control loops where the variables have a very wide dynamic range. A solution, which very much improved performance, was to use floating point variables for all the PI control loops. This extended the processing time somewhat but was not found to be a significant burden when using a 25 MIPS DSP core.

The processor must handle multiple interrupt sources from the ADC, the digital I/O block, the communication ports, and the timer. A number of useful device features such as an auto-buffered serial port and a single context switch made the task possible without significant overhead in pushing or popping a stack. Finally, the code development was somewhat simplified by the availability of library functions on the ADMC331 ROM for mathematical functions and the Park and Clark transformations.

The availability of DSP microcontrollers presents a new set of challenges for motor-control design engineers. The vast increase in processing power over standard microcontrollers offers an opportunity to increase drive performance or reduce cost. The two examples given here show that to fully employ this power requires new control approaches and philosophy. The challenge will be to fully exploit the opportunities possible with this new technology. The world of domestic appliances is changing in a similar fashion as the automotive industry changed a few years ago. The future is a world of "intelligent" home appliances.

Aengus Murray leads the systems engineering team within the Analog Devices Motion Control Group. He graduated with BE and PhD degrees from University College, Dublin, Ireland, in 1980 and 1985.



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Circle 520

Simple Circuit Measures Voltage-Dependent Capacitance

ROBERT N. BUONO
2049 Charles Court, Mahwah, NJ 07430; (201) 512-8534;
fax (201) 512-1494; e-mail: bbengg@aol.com.

There are many techniques for measuring capacitance. Some of these techniques require a function generator to provide either a sinusoidal or step-function voltage source. The design idea presented here has the advantage of requiring no special excitation source. Instead it relies on a simple test circuit, along with the single-shot capture and measurement capabilities inherent in digital oscilloscopes (DSOs).

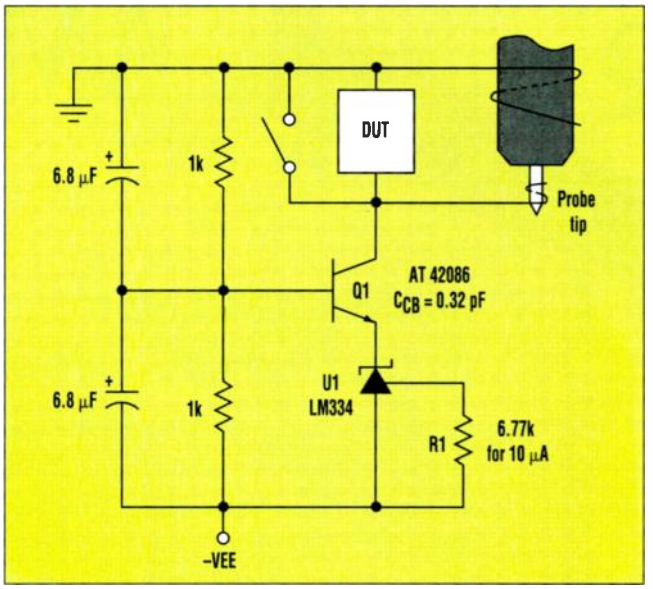
The circuit can accurately measure very small capacitances, and also is able to accurately measure capacitances that change as a function of applied voltage. An example of devices which feature voltage-dependent capacitance is a reversed-biased p-n junction, such as the collector-base junction of a bipolar transistor. Another example is a TVS (transient-voltage-suppressor diode) device.

The test circuit consists of a single npn transistor (Q1) configured in a common-base connection *(Fig. 1)*. U1 is a constant-current source (LM334) in the emitter leg of the transistor. The transistor exhibits very low collector-base capacitance (C_{CB} = 0.32 pF typical). This specification is critical to the design, as the actual voltage swing across the DUT will occur between the collector of the transistor and ground. The base of the transistor is biased with a constant dc voltage equal to 1/2 of the supply voltage ($-V_{EE}$). Maximum V_{CE} for the transistor used in this circuit is 12 V, therefore $-V_{EE}$ should be limited to about –22 V maximum.

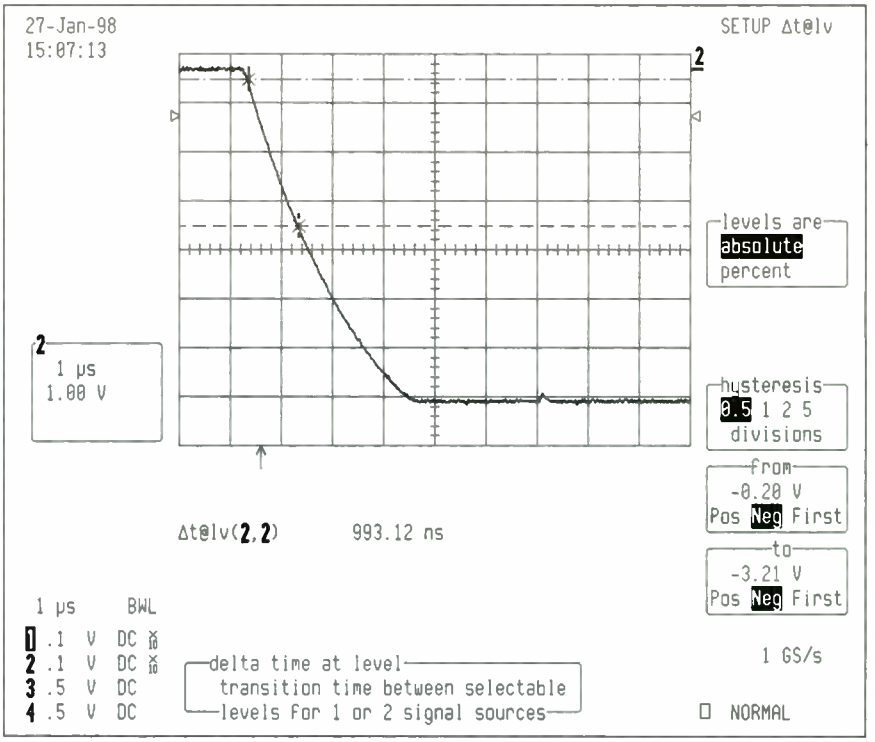
The circuit works as follows. The LM334 constant-current source (U1) is programmed for a cathode current of 10 µA by the selection of R1 (67 mV/R1 = $I_{CATHODE}$). The capacitance to be measured is connected between circuit ground and the collector of Q1. A low capacitance switch is used to short the collector of Q1 to ground. Please note—I used the sharp edge of a simple clip-lead to manually contact the ground node, making a very low capacitance connection.

A very low capacitance scope probe (FET type) is attached to the circuit as illustrated in Figure 1. A digital oscilloscope is used in single-shot capture mode to capture the falling edge of the voltage waveform, which appears across the DUT after the short is released. The unknown capacitance is charged by the constant current source through Q1. With proper triggering, the entire voltage waveform can be captured.

The programmed current of the constant-current source can be changed, depending on the range of capacitance value to be measured, and is not critical. The selected value of charging current determines the slope of the displayed wave-



1. This circuit, combined with DSO capture features, accurately measures very small capacitances without requiring a special excitation sources.



2. The waveform shown is a measurement of test circuit capacitance without a device under test.

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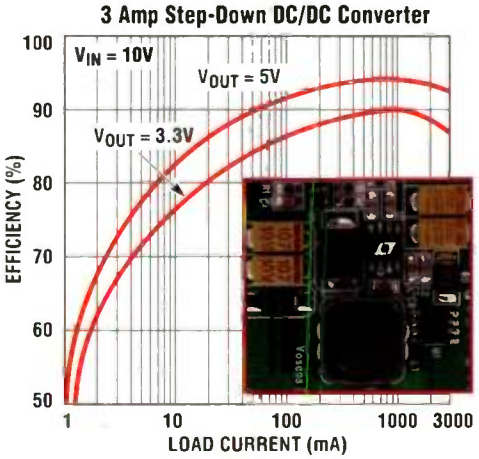

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form. The voltage response (slope) can be made arbitrarily slow so that inductances inherent in the circuit won't affect the measurement.

The displayed results can be analyzed as follows. Because the DUT has been charged with a constant-current, the capacitance of the device is simply:

$$C = I/(dV/dT)$$

Both the time and voltage parameters (slope of the captured voltage waveform) can be measured directly from the displayed waveform. Devices with a fixed capacitance will display a linear slope characteristic (up to the saturation voltage of Q1). Devices with capacitance that is voltage-dependent will show a varying-slope characteristic. Capacitance can be directly measured at any bias voltage for devices with a voltage-dependent capacitance.

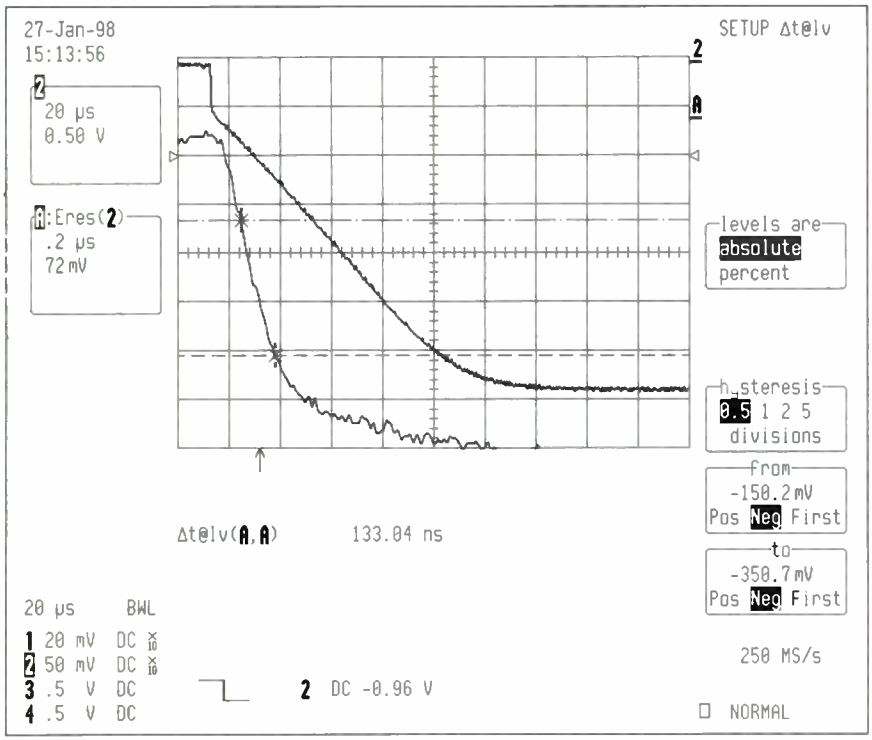
Certain features of typical modern DSOs make these type of measurements particularly convenient. LeCroy oscilloscopes have a measurement feature called "delta-time-between-levels," which allows a direct measurement and readout of the delta-time between two cursor-selected voltages on any displayed waveform (Figs. 2, 3, and 4).

The waveform displayed in Figure 2 is captured with the measurement circuit alone, without any DUT. Therefore, this is a baseline measurement of the capacitance of the test circuit. This consists of the capacitance (C_{CB}) of Q1, the scope probe, and the parasitic capacitances of the physical test circuit. The measured value (3.3 pF) will be subtracted from subsequent measurements.

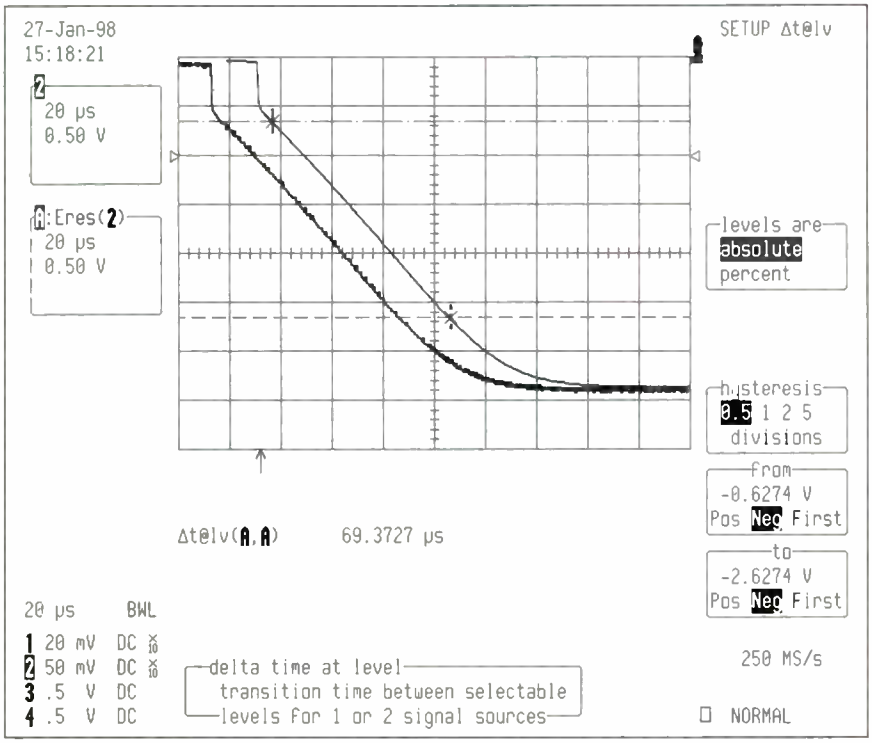
Figure 3 displays a waveform obtained when the DUT is a TVS device. Such a device is termed a "low-capacitance-type" TVS. The manufacturer achieves a low capacitance by inserting a high-speed rectifier (with low-capacitance) in series with the TVS diode. It can be seen in the displayed result that the capacitance of the device is indeed very low (3.4 pF) when the device is biased with up to 0.5 Volts. However, above this bias voltage, the internal rectifier diode is conducting, and the capacitance of the TVS device now dominates.

Figure 4 displays two waveforms. Trace 2 is the entire captured waveform showing TVS characteristics from 0 V on up to its breakdown voltage with a bias current of 10 µA (this is a 3-V TVS device). The expanded trace (A) is an expansion of the region from 0 V to approximately –0.5 V (the region of low capacitance). Measurement on this expanded trace yields the capacitance value of 3.4 pF.

This is a convenient technique which uses a simple, small, and



3. Here, the region of low capacitance (i.e. below 0.5V bias) is determined using a "low-capacitance" transient-voltage-suppressor (TVS) device as the DUT.



4. Capacitance of the TVS device is measured at bias voltages greater than 0.5 V.

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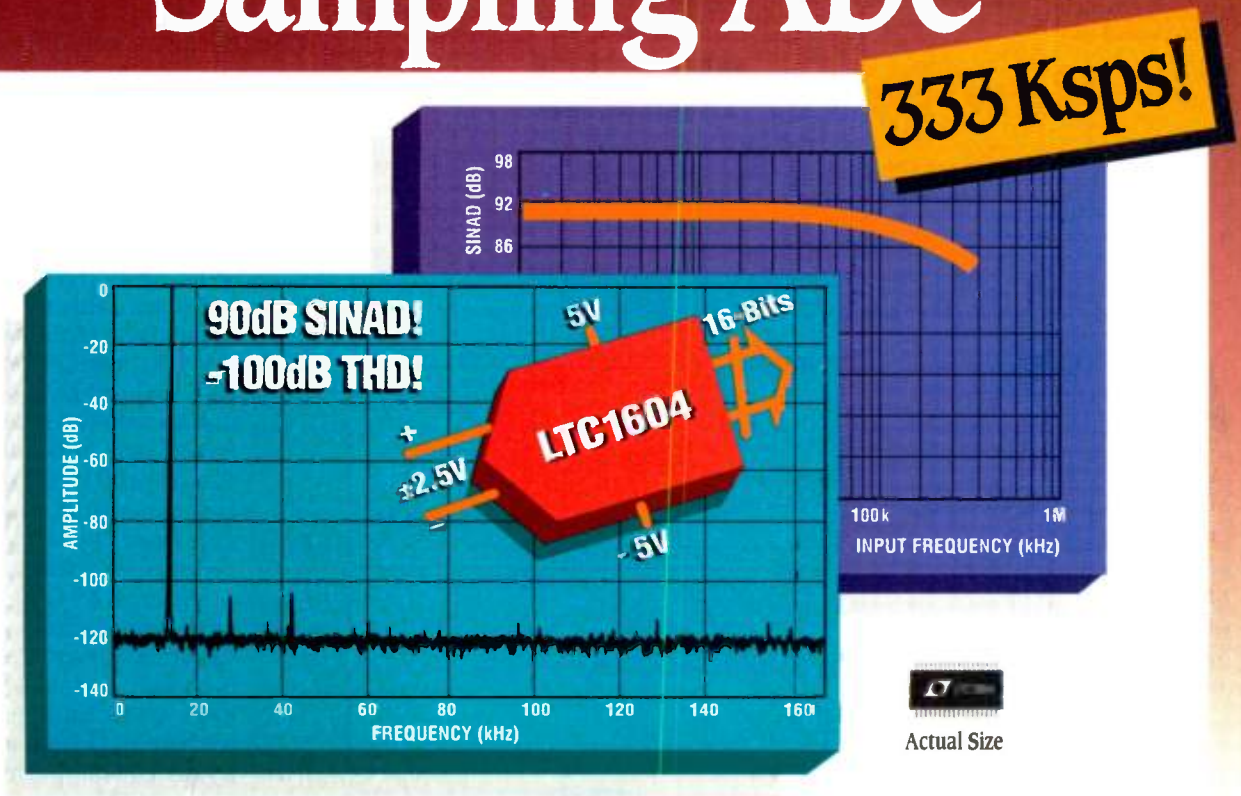

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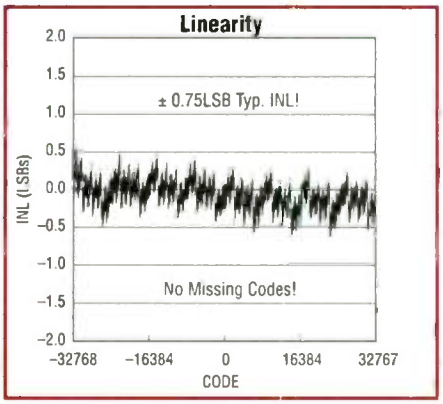

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portable circuit to measure voltage-dependent capacitance characteristics. This circuit also has been used to measure the parasitic capacitances at input connectors and other areas of pc boards, which could not easily be driven by sinusoidal voltage sources or connected to test instruments for direct measurement.

Circle 521

Low-Power Thermal Airspeed Sensor

W. STEPHEN WOODWARD
Venable Hall, CB3290, University of North Carolina,
Chapel Hill, NC 27599-3290; e-mail: woodward@net.chem.unc.edu.

Among the techniques available to measure airspeed, thermal anemometry has the virtues of simplicity and easy miniaturization. Such anemometers use the relationship between airspeed and power dissipated by a heated sensor known as King's Law. One good approximation to King's Law is:

$$S = A * [(P - D)/(T_S - T_A)]^2$$

where:

S = air speed

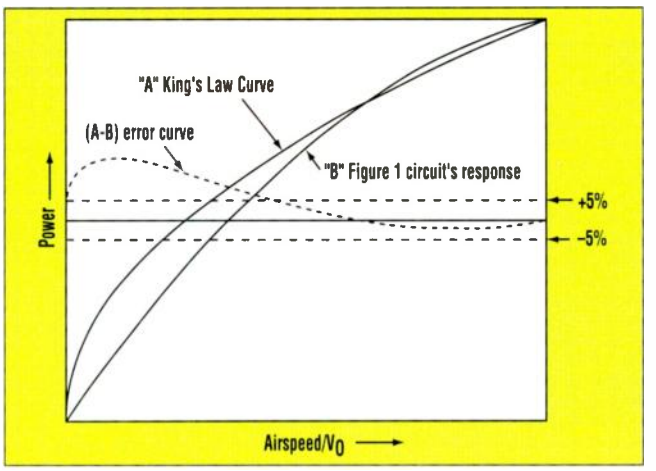
A = full-scale calibration constant

P = power dissipated by the airspeed sensor

D = "still-air" (S = 0) power dissipation

T_S = temperature of the airspeed sensor

T_A = ambient temperature



2. The quadratic relationship between P and V2 helps cancel the King's Law nonlinearity, resulting in less than a 5% error over more than half of the zero to full-scale range of airspeed.

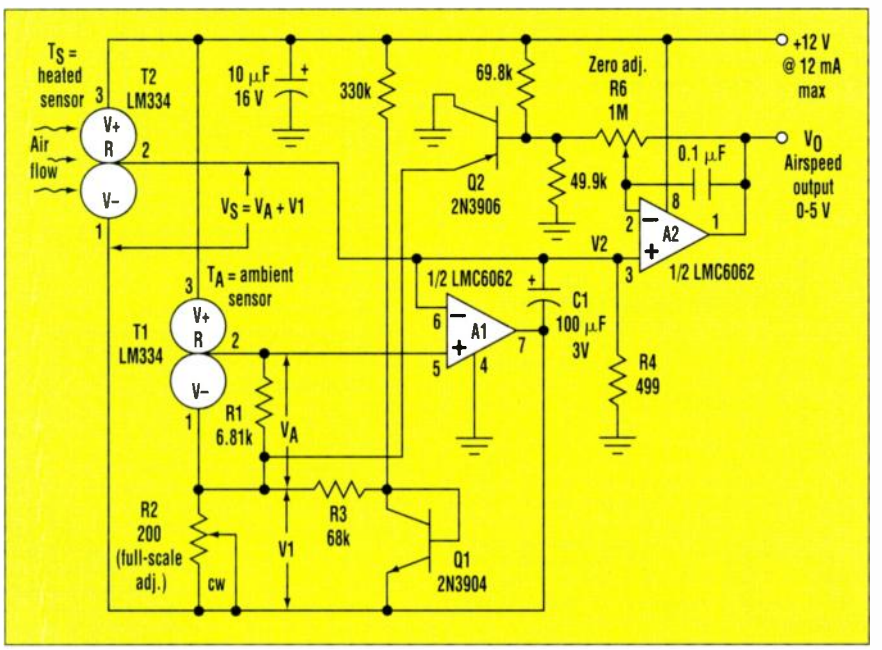
Two practical problems of thermal airspeed sensors are apparent from this equation. First, the accuracy of the airspeed measurement obviously depends on stability of the $(T_S - T_A)$ term. This means that either the T_S and T_A measurements must track very closely, or the $(T_S - T_A)$ differential must be made large enough to swamp the drift caused by ambient temperature excursions.

Accurate temperature measurement isn't easy, so the brute-force route usually is chosen, and the sensor is kept good and hot. The penalty of this strategy is power consumption on the order of 1 W, making portable operation problematic.

Also, the second-order exponent makes the raw sensor output nonlinear with airspeed. Therefore, thermal anemometers typically need some provision for measurement linearization.

Figure 1's circuit utilizes the venerable LM334 temperature sensor to minimize both headaches. LM334s generate a proportional-to-absolute-temperature (PTAT) voltage of ≈214μV/°Kelvin. Therefore, if a constant $(V_S - V_A)$ voltage differential is maintained, a constant $(T_S - T_A)$ temperature differential will result. Figure 1's arrangement of R2, R3, and Q1 provide a stable voltage difference (V1) in the range of 0 to 4 mV to be added to V_A.

Op-amp A1 adjusts V2 to maintain $V_S = V_A + V1$ and, thereby, $T_S = T_A + V1/214\ \mu V$. This works because the power dissipation of ambient-sensor T1 is about 100 μW and is, therefore, too little to significantly heat the sensor (LM334s in TO-92 packages have a still-air dissipation constant of



1. Two LM334 temperature sensors are used in this thermal airspeed sensor to minimize power consumption and provide for linearization.

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5.6mW/°C). Airflow-sensor T2's dissipation, however, is much larger: P = 1.06 * (12 – V2) * V2/R4, making T2 heat up when A2's output slews positive, taking V2 with it. As V2 swings from 0 to 5 V, P goes from 0 to 74 mW. Depending on air speed, this power range is sufficient to maintain a (T_S – T_A) differential (as set by R2) of 4 to 13°Kelvin. V2 is buffered and zero-corrected by A2 and becomes the 0-to-5-V airspeed output signal.

But what about measurement linearization? As illustrated in Figure 2, the inherent quadratic relationship between P and V2 does a reasonable job of canceling King's Law nonlinearity and results in less than 5% error over more than half of the zero/full-scale range of airspeeds. Anemometer zero/full-scale calibration is straightforward and interaction-free if done in the right sequence. T2 should first be exposed to air flow corresponding to the desired full-scale airspeed and R2 adjusted for V_O = 5 V. T2 then is placed in calm air and R6 adjusted for V_O = 0.

C1 and Q2 provide protection against feedback-loop oscillation and latchup. The 12-V supply should be well-regulated for good circuit stability. Total power consumption depends on airspeed, but never exceeds 144 mW (12 V @ 12 mA). This figure is easily six times less than the requirements of comparable performance sensors, especially anemometers that use sturdy plastic sensors instead of fragile metallic filaments. Response is fairly quick (less than 2 seconds) due to the constant-temperature operation of T2.

Circle 522

Simple Sine-Wave Generator Has No Low- Or High-Pass Filters

FRANTISEK MICHELE
Barvicova 17A, CZ 60200 Brno, Czech Republic.

Generating sine waves with controlled frequencies over a wide range is difficult when using RC or LC sinusoidal oscillators. However, this performance can be simply created using a wideband digital squarewave oscillator, a counter, and a weighted summing network.

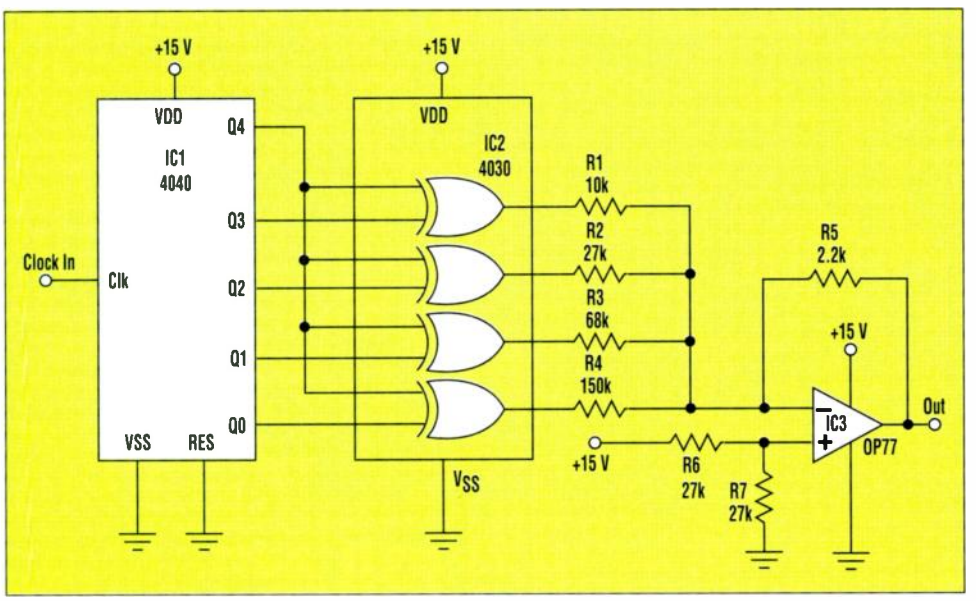
Using the circuit shown, a sinusoidal output signal with a 100,000,000+:1 frequency range from about 1 MHz to under 0.01 Hz can be obtained without need for any low-pass or high-pass filters. The circuit consists of two parts. The first part is a counter IC with a controlled inverter (IC2) that sequences the switching of input resistors of the second part—a summing amplifier (IC3). The EXOR gates are used to invert signals from four of IC1 counter's outputs (Q0-Q3), depending on logical value at the fifth counter output (Q4). This operation creates the positive and negative halves of the sine waveform. Each of these halves consists of 2^4 = 16 parts.

The logical values at IC1's Q0-Q4 outputs produce weighted-symmetrical currents at the summing junction of IC3. The amplifier adds all four weighted currents and generates an output signal with the desired sinusoidal waveform.

Every period of the output signal needs 16 * 2 = 32 periods of input signal, i.e. the frequency of input clock signal must be 32 times higher than the desired frequency of output analog signal:

$f_{OUT\text{-}ANALOG} = f_{IN\text{-}DIGITAL} / 32$

By changing the values of resistors R1-R4, other waveforms can be produced.



Only a wideband digital squarewave oscillator, a counter, and a weighted summing network are required to create this wide-range sine-wave generator. Other waveforms are possible using different resistor values

IFD Winners

W. Stephen Woodward, Venable Hall, CB3290, University of North Carolina, Chapel Hill, NC 27599; e-mail: woodward@net.chem.unc.edu. The idea: "Linear Pitot-Tube Air-Speed Indicator", June 9, 1997 Issue.

M. Periera and F. Perez-Fontan, University of Vigo (Spain), Dept. of Communication Technologies, Campus Universitario, E-36200, Vigo, Spain; tel: +34 86 812137; fax: +34 86 812137. The idea: "Generate A 9.997925-MHz Signal Using A 10-MHz Reference", June 23, 1997 Issue.

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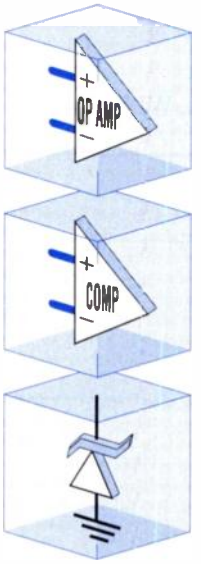

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NEW	MAX9000/9001	1.25	—	185	✔	2.5 to 5.5	410	1.80	8-pin µMAX/SO
NEW	MAX9002	1.25	—	185		2.5 to 5.5	340	1.20	8-pin µMAX/SO
NEW	MAX9003/9004	—	8.0	185	✔	2.5 to 5.5	410	1.80	8-pin µMAX/SO
NEW	MAX9005	—	8.0	185		2.5 to 5.5	340	1.20	8-pin µMAX/SO
	MAX951	0.02	—	4000	✔	2.7 to 7.0	7	1.47	8-pin µMAX/SO
	MAX952	—	0.125	4000	✔	2.7 to 7.0	7	1.47	8-pin µMAX/SO
	MAX953	0.02	—	4000		2.4 to 7.0	5	1.19	8-pin µMAX/SO
	MAX954	—	0.125	4000		2.4 to 7.0	5	1.19	8-pin µMAX/SO

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Circle 523

Special Low-Pass Filter Limits Slope

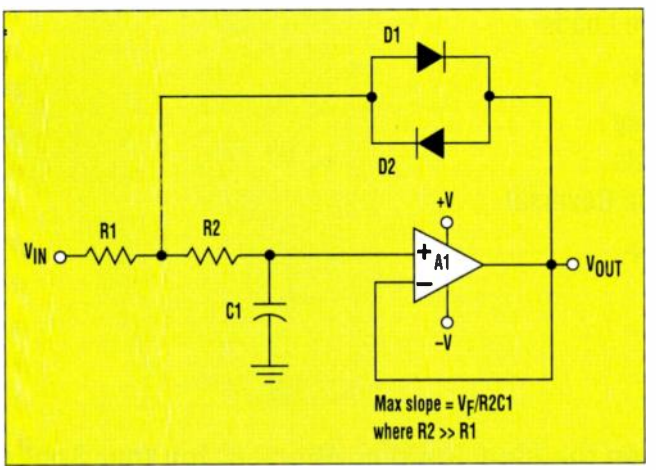
ANDREW R. WILLIAMS
5939 W. Wells St., Wauwatosa, WI 53213

Adding several components to a simple first-order, low-pass filter, helps to create a different yet handy filter. The circuit shown in Figure 1 combines a low-pass filter (R2, C1, A1) with a bidirectional diode clipping network (R1, D1, D2). The result is a filter that will limit the maximum slope (not frequency) it passes.

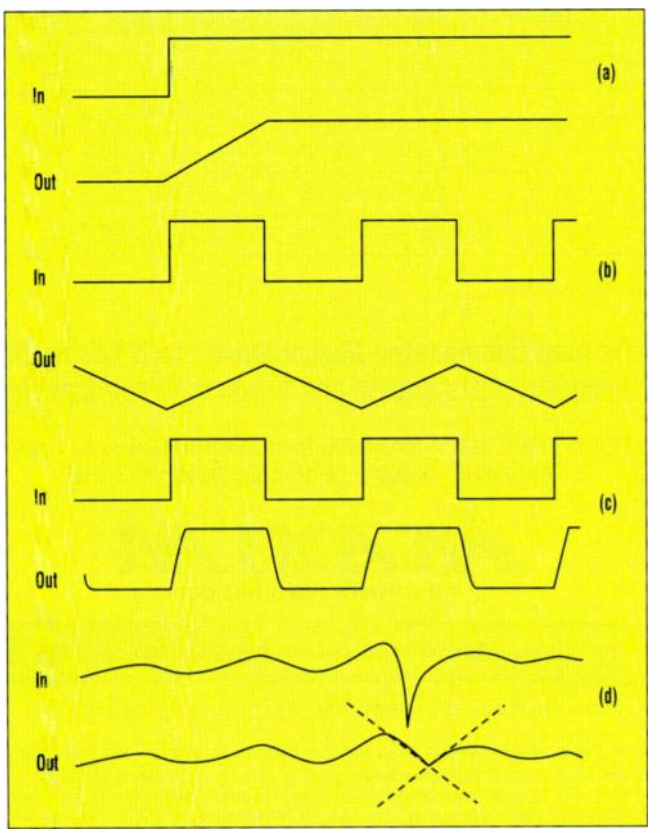
Typical uses for this circuit are shown in Figures 2a-2d. In general, it's used to create ramps from step voltages, generate triangle/trapezoid waveforms from square waves, remove unwanted fast components (noise/transients) from any signal, or limit the maximum rate of change of any signal.

Here's how it works. Whenever the input voltage V_{IN} differs from the output voltage V_{OUT} by one forward diode drop or more, one of the diodes will turn on (D1 when $V_{IN} > V_{OUT}$ and D2 when $V_{IN} < V_{OUT}$). When this happens, the voltage across R2 is held fairly constant (because the voltage at the "+" input and the output of A1 are equal) at one forward diode drop.

With a fixed voltage across R2 and, therefore, a constant current through it, the capacitor C1 charges linearly instead of exponentially. The maximum slope (V/T) that the circuit will pass is equal to the V_F of the diodes used divided by R2C1 (maximum slope (V/T) = V_F / R2C1). This assumes R2 >> R1. No matter how quickly the input voltage changes, the output will never change any faster than the limit set by R2C1. Any signal or part of a signal with a slope less than this limit simply passes through the circuit unaffected.



1. Combining a low-pass filter with a bidirectional clipping network, this filter can limit the maximum slope (not frequency) that it will pass.



2. Typical uses for the filter include: (a) creating ramps from step voltages; (b) generating triangle waveforms or (c) trapezoid waveforms from square waves; and (d) limiting the maximum rate of change of any signal.

V_{IN} should be driven by a low impedance source. Resistor R1 limits the current through D1 or D2 when they conduct. Typically R1 is 1k-10k. Its value should be kept as small as practical and depends on the drive capabilities of A1 and the op-amp or other device driving V_{IN}. R2's resistance should be much greater than that of R1 to swamp out its contribution to the circuit's R2C1 time constant. R2 and C1 form a low-pass filter and A1 buffers it and provides a low impedance path for Dl or D2 when in conduction. For the best performance, D1 and D2 should be low V_F (Schottky) types, although other diode types (1N914, 1N4148, etc.) will work satisfactorily.

When a square wave or step voltage is slope-limited by this circuit, a slight rounding will be seen at the top and bottom of the output waveform. This is due to the loss of overhead voltage (needed for diode conduction) that occurs when the capacitor has charged within one diode drop of the input's peak voltage. This rounding is minimized by using low V_F diodes, keeping R1 as small as possible, and by using the largest amplitude input waveform your supply voltage will allow.

I originally came up with this circuit while designing a servo control loop. I needed a simple way to limit the rate of change of the servo's output signal. It also can be used to soft start lights, create smooth motor speed transitions, filter a signal by its slope instead of its frequency, tame ill-behaved servo circuits, slow square wave transitions (without excessive rounding), and so on. Unlike integrator-based circuits this circuit works with single-ended or bidirectional supplies.

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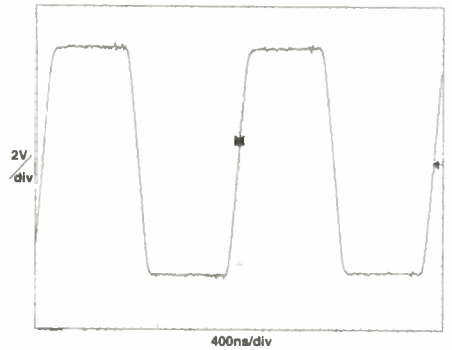

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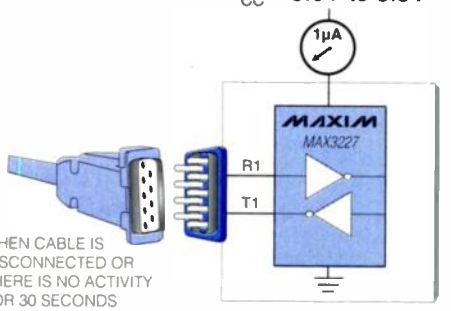

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MAX3224	+3.0 to +5.5	2/2	1	250k	Yes	—	4 x 0.1
MAX3224E	+3.0 to +5.5	2/2	1	250k	Yes	✔	4 x 0.1
MAX3225	**+3.0 to +5.5**	2/2	**1**	**1M**	**Yes**	—	**4 x 0.1**
MAX3225E	**+3.0 to +5.5**	**2/2**	**1**	**1M**	**Yes**	✔	**4 x 0.1**
MAX3226	+3.0 to +5.5	1/1	1	250k	Yes	—	4 x 0.1
MAX3226E	+3.0 to +5.5	1/1	1	250k	Yes	✔	4 x 0.1
MAX3227	**+3.0 to +5.5**	**1/1**	**1**	**1M**	**Yes**	—	**4 x 0.1**
MAX3227E	**+3.0 to +5.5**	**1/1**	**1**	**1M**	**Yes**	✔	**4 x 0.1**
MAX3244	+3.0 to +5.5	3/5	1	250k	Yes	—	4 x 0.1
MAX3244E	+3.0 to +5.5	3/5	1	250k	Yes	✔	4 x 0.1
MAX3245	**+3.0 to +5.5**	**3/5**	**1**	**1M**	**Yes**	—	**4 x 0.1**
MAX3245E	**+3.0 to +5.5**	**3/5**	**1**	**1M**	**Yes**	✔	**4 x 0.1**

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OCTOBER

Fifth IEEE International Conference on Image Processing (ICIP '98), Oct. 4-7. The Westin Hotel Chicago, Chicago, IL. Contact Billene Mercer, CMS, 3109 Westchester Ave., College Station, TX 77845-7919; (409) 693-6000; fax (409) 493-6600; e-mail: mercer@conf.mgmt.com.

IEEE International Telecommunications Energy Conference, Oct. 4-8. Hyatt Regency Hotel, San Francisco, CA. Contact Lou Scerbo, Bellcore, Room 1J206G, 445 South St., Morristown, NJ 07960; (201) 829-5962; fax (201) 829-5962; e-mail: lscerbo@notes.cc.bellcore.com.

PCI Plus Europe '98 Developers' Conference and Expo, Oct. 5-8. Le Palais des Congres (Porte Maillot), Paris, France. Contact Active Exhibitions Europe, P.O. Box 2114, 5300 CC Zaltbommel, Netherlands; +31 418 51299; fax +31 418 540599.

Seventh IEEE International Conference on Universal Personal Communications, Oct. 5-9. Palazzo Congressi & Centro Affari, Florence, Italy. Contact Federico Tosco, CSELT, Via Reiss Romoli 274, 10148 Torrino, Italy; +39 11-228-5321; fax +39 11 228-5295; e-mail: Federico.Tosco@CSELT.STET.IT.

IEEE/LEOS Semiconductor Laser Conference, Oct. 5-10. Nara Public Hall, Nara, Japan. Contact Elsie L. Vega, IEEE/LEOS, 445 Hoes Ln., P.O. Box 1331, Piscataway, NJ 08855-1331; (732) 562-3897; fax (732) 562-8434; e-mail: e.vega@ieee.org.

The Vision Show, Oct. 6-8. San Jose Convention Center, San Jose, CA. Contact Automated Imaging Association (AIA), 900 Victors Way, P.O. Box 3724, Ann Arbor, MI 48106; (313) 994-6088; fax (313) 994-3338; e-mail: kerickson@automated-imaging.org; www.automated-imaging.org.

IEEE Ultrasonics Symposium, Oct. 6-9. Hotel Metropolitan Sendai, Sendai, Japan. Contact Noriyoshi Chubachi, Tohoku Gakain Univ., Faculty of Engineering, Tagaio, Miyagi 985, Japan; +81 22-217-7077; fax +81 22-263-9230; e-mail: chubachi@chubachi.ecie.tohoku.ac.jp.

IEEE-SP International Symposium on Time-Frequency and Time-Scale Analysis, Oct. 7-9. Pittsburgh Sheraton, Pittsburgh, PA. Contact Patrick J. Loughlin, 348 Benedum Hall, Department of Electrical Engineering, University of Pittsburgh, Pittsburgh, PA 15261; (412) 624-9685; fax (412) 624-8003; e-mail: pat@ee.pitt.edu.

IEEE International Conference on Systems, Man, & Cybernetics, Oct. 12-14. Hyatt Regency La Jolla, La Jolla, CA. Contact M.A. Jafari, Dept. of Industrial Engineering, Rutgers University, P.O. Box 909, Piscataway, NJ 08855; (908) 445-3627; fax (908) 445-5467; e-mail: jafari@gandalf.rutgers.edu.

International Test Conference (ITC), Oct. 20-22. Sheraton Washington Hotel, Washington, D.C. Contact ITC, 2000 L St. N.W., Washington, D.C. 20036; (202) 973-8665; fax (202) 331-0111; e-mail: itc@courtesyassoc.com.

NOVEMBER

Embedded Systems Conference, Nov. 1-5. San Jose Convention Center, San Jose, CA. Contact Liz Austin, Miller Freeman Inc.; (888) 239-5563; (415) 538-3848; e-mail: esc@mfi.com; www.embedded.com.

Photonics East & Electronic Imaging International Exhibition, November 1-6. Boston, Massachusetts. Contact SPIE Exhibits Dept., P.O. Box 10, Bellingham, Washington 98227-0010; (360) 676-3290; fax (360) 647-1445; e-mail: exhibits@spie.org.

Voice, Video & Data Communications Conference & Exhibition, Nov. 1-6. Boston, MA. Contact SPIE Exhibits Dept., P.O. Box 10, Bellingham, WA 98227-0010; (360) 676-3290; fax (360) 647-1445; e-mail: exhibits@spie.org.

Technology 2008, November 3-5. Hynes Convention Center, Boston, Massachusetts. Contact Melissa Hinnen, Show Coordinator; (212) 490-3999; fax (212) 986-7864.

IEEE Global Telecommunications Conference (Globecom '98), Nov. 9-13. Sydney, Australia. Contact Sam Reisenfeld, School of Electrical Engineering, University of Technology, Sydney, Post Office Box 123; Broadway, NSW 2007, Australia; +61 2-330-2435; e-mail: samr@transmit.ee.uts.edu.au.

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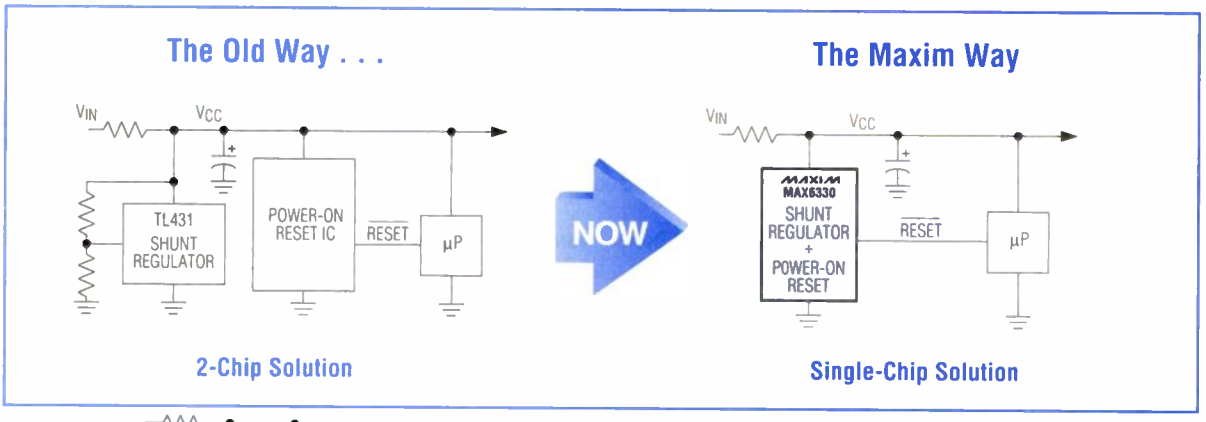

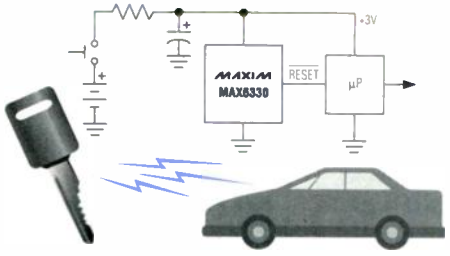

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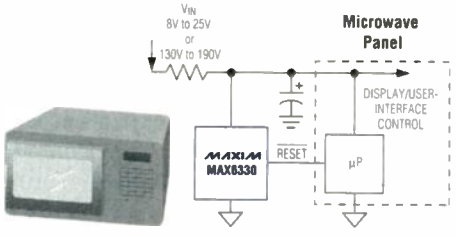

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DECEMBER

IEEE International Electron Devices Meeting (IEDM), Dec. 6-9. San Francisco, CA. Contact Phyllis Mahoney, Widerkehr & Associates, 101 Lakeforest Blvd., Suite 270, Gaithersburg, MD 20877; (301) 527-0900; fax (301) 527-0994; e-mail: pwmahoney@aol.com.

12th Systems Administration Conference (LISA '98), Dec. 6-11. Marriott Hotel, Boston, MA. Contact USENIX Conference Office, 22672 Lambert St., Suite 613, Lake Forest, CA 92630; (714) 588-8649; (714) 588-9706; e-mail: conference@usenix.org; www.usenix.org.

37th IEEE Conference on Decision and Control, Dec. 16-18. Hyatt Regency Westshore, Tampa, FL. Contact John D. Birdwell, Department of Electrical Engineering, University of Tennessee, Knoxville, TN 37996-2100; (423) 974-9187; fax (423) 974-9257; e-mail: birdwell@hickory_engr.utk.edu.

IEEE Region 10 Conference on Energy, Communication, Computers, and Controls (TENCON '98), Dec. 17-19. Asmoka Hotel, New Delhi, India. Contact Tripta Narang, A-10, Lajpat Nagar-III, New Delhi, 110024, India; +91 11-643-5441; fax +91 11-646-5645; e-mail: purkay.sagrik@axcess.net.in.

JANUARY 1999

Annual Reliability & Maintainability Symposium (RAMS), Jan. 19-21. Washington Hilton. Washington, DC. Contact V.R. Monshaw, Consulting Services, 1768 Lark Lane, Cherry Hill, NJ 08003; (609) 428-2342.

IEEE Power Engineering Society Winter Meeting, Jan. 31-Feb. 4. New York, NY. Contact Frank Schink, 14 Middlebury Lane, Cranford, NJ 07016; (908) 276-8847: fax (908) 276-8847.

FEBRUARY

Photonics West, February 6-12. San Jose, CA. Contact SPIE Exhibits Dept., P.O. Box 10, Bellingham, Washington 98227-0010; (360) 676-3290; fax (360) 647-1445; e-mail: exhibits@spie.org.

IEEE International Solid-State Circuits Conference (ISSCC '99), February 15-17. San Francisco Marriott, San Francisco, California. Contact Diane Suiters, Courtesy Associates, 655 15th St., N.W., Washington, DC 20005; (202) 639-4522; fax (202) 347-6109; e-mail: isscc@coutesyassoc.com.

Portable by Design, February 21-25. Santa Clara Convention Center, Santa Clara, California. Contact Rich Nass, Electronic Design, 611 Rte. 46 West, Hasbrouck Heights, New Jersey 07604; (201) 393-6090; fax (201) 393-0204; e-mail: portable@class.org.

FEBRUARY 1999

The Wireless Symposium and Exhibition, Feb. 21-25. San Jose Convention Center, Santa Jose, CA. Contact Bill Rutledge, Penton Publishing, 611 Rte. 46 West, Hasbrouck Heights, NJ 07604; (201) 393-6259; fax (201) 393-6297; instant faxback (800) 561-7469; www.penton.com/wireless.

MARCH 1999

Southeastcon '99, Mar. 25-29. Marriott Resort Hotel, Lexington, KY. Contact Don Hill, 1676 Donelwal Dr., Lexington, KY 40511-9021; (606) 257-8487; fax (606) 323-1034; e-mail: d.w.hill@ieee.org.

APRIL 1999

IEEE/PES Transmission & Distribution Conference & Exposition, Apr. 10-17. Ernest N. Morial Convention Center, New Orleans, LA. Contact Grace Juneau, c/o Entergy, P.O. Box 61000, New Orleans, LA 70161-1000; (504) 576-2400; fax (504) 576-5989; e-mail: gjuneau@entergy.com.

41st IEEE Cement Industry Technical Conference, Apr. 11-15. Roanoke, VA. Contact Margaret Peterson, Roanoke Cement Co., P.O. Box 27, Cloverdale, VA 24077; (540) 992-1501; fax 966-1542.

IEEE Radar Conference, Apr. 20-22. Boston, MA. Contact Robert Alongi. 255 Bear Hill Rd., Waltham, MA 02154; (617) 890-5290; fax (617) 890-5294.

MAY 1999

IEEE/IAS Industrial & Commercial Power Systems Technical Conference (I&CPS), May 3-6. Nuggett Hotel, Sparks, NV. Contact Kerry Flannigan. Sierra-Nevada Power Co., P.O. Box 10100, Reno, NV 89520; (702) 689-4848; fax (702) 689-4139.

Sixth IFIP/IEEE International Symposium on Integrated Network Management (IM '99), May 9-14. Boston Park Plaza Hotel, Boston, MA. Contact Judy Keller, IEEE/COMSOC, 345 East 47th St., New York, New York 10017; (212) 705-8248; fax (212) 705-7865; e-mail: j.keller@ieee.org.

JUNE 1999

IEEE/MTT-S International Microwave Symposium (MTT '99), June 13-18. Anaheim, CA. Contact Robert Eisenhart, 5982 Ellenview Ave., Woodland Hills, CA 91367; (818) 716-1995; fax (818) 713-1161.

JULY 1999

IEEE Power Engineering Society Summer Meeting, July 18-22. Edmonton, Alberta, Canada. Contact Dave Fraser, Edmonton Power Capital Square, Edmonton, Alberta, T5J 3B1, Canada; (403) 448-3554; fax (403) 448-3192.

OCTOBER 1999

IEEE Industry Applications Society Annual Meeting, Oct. 4-8. Civic Center, Phoenix, AZ. Contact Michael Andrews, Andrews Associates, 12438 80th Pl., Scottsdale, AZ 85260.

FEBRUARY 2000

IEEE International Solid-State Circuits Conference (ISSCC '00), Feb. 7-9. San Francisco Marriott, San Francisco, CA. Contact Diane Suiters, Courtesy Associates, 655 15th St., N.W., Washington, DC 20005; (202) 639-4255; (202) 347-6109; e-mail: isscc@courtesyassoc.com.

May 2000

IEEE International Conference on Acoustics, Speech & Signal Processing (ICASSP 2000), May 23-26. Istanbul Hilton & Lutfu Kirdar Conference Center, Istanbul, Turkey. Contact Huseyin Abut, Electrical and Computer Engineering Dept., San Diego State University, San Diego, California 92182-1309; (619) 594-3702; fax (619) 594-3703; e-mail: abut@anadolu.sdsu.edu.

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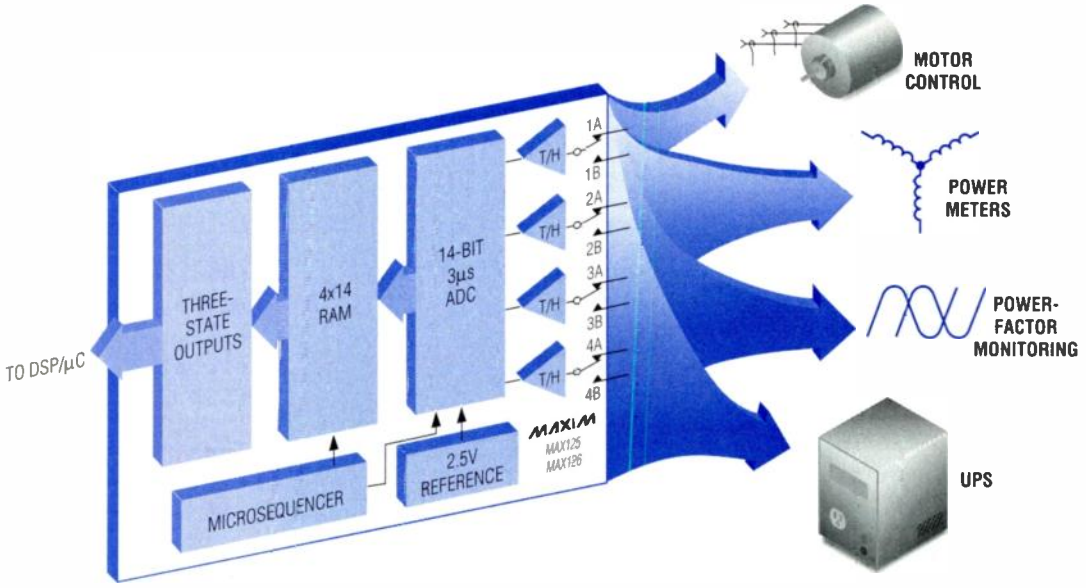

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READER SERVICE 176

BOB PEASE

Bob's Mailbox

Dear Bob:

I've been following the technique of breadboarding with copper clad. I have used the Moto-tool approach to cut between the traces, but I think I have an easier way. I noticed that merely scoring the copper with a knife and a straight edge is enough to allow it to be pulled away from the board. So, I soldered two utility knife blades together so that they would both cut at the same time. Now, when installed in the utility handle, they make two neat, parallel cuts 20 mils apart that can be pulled away easily with an X-ACTO knife. Thinking that 20 mils might be small for my purposes, I tried grinding off the cutting edge of another blade to use as a spacer. Now the three-blade sandwich makes a 40-mil line.

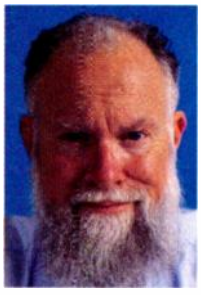
JIM PHILLIPS
via e-mail

Hey, Jim, I'll have to try that. I am not sure it's much faster than just using a hacksaw to cut a line. But it sure will make L-shaped cuts better than a hacksaw can!—RAP

Dear Bob:

I, too, have seen the ice-water and pizza diet floating around the net, and tried to debunk it. Interestingly, I came on the same thing a long time ago (mid-1950s) when I was a kid. You see, I like soft drinks with "lots" of ice, and my mother complained about the number of calories they contained. I calculated about how much energy it took to raise the water to body temperature (including the latent heat of melting). And, yes, I did understand the difference between calories and kilocalories, even then, at about 10. It really did make a difference of about one-third in the number of calories—if you fix drinks the way I do. I don't know if my mother ever bought the calculation, though.

By the way, there is another reason why manhole covers are round besides keeping them from falling into the hole. You can move them by rolling, which is harder, though not impossible, with triangular covers.



BRUCE WALKER
via e-mail

In many places, rolling a manhole cover may not be a big deal, but in other cases, it's a distinctly neat feature. Thanks for pointing this out.—RAP

Dear Bob:

This is in regard to your International Travel column in the March 9, issue. I recently returned from four months in Turkey. I didn't trust the tap water, but realized bottled water would be very expensive. I took along iodine tablets for emergencies, but for regular drinking water I used a camper's micropore filter, and filtered the tap water in my apartment. It was a lot cheaper than bottled water.

I was going as a visiting professor, and knew I'd also be giving some seminars. Taking along all my overhead slides would have been a horrible burden. Instead, I saved my slides as PowerPoint files on a ZIP drive. Once there, I was able to print them out on transparencies. On one occasion, I had to give a briefing to the Turkish Department of Defense. One of my colleagues translated my slides into Turkish, and in effect, we gave two briefings in parallel. We showed both sets of slides at the same time. I would say a few words in English, and my colleague would then repeat what I said in Turkish. It worked out fairly well, but not as well as speaking directly to the audience.

JOE MARTINO
via e-mail

You are correct that the water filter is a wise third option. I should have mentioned that. AHA! You've run the double-foil presentation and it seemed to work! I'm glad to hear that.—RAP

All for now. / Comments invited!
RAP / Robert A. Pease / Engineer
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So, this year, don't get left behind, register early! In all, only a few thousand very elite engineers will be able to be a part of this high-level conference. And the subjects they talk about this June will have a huge effect on the next wave of products that hit the shelves, so reserve your space now.

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32-Bit Floating-Point Digital Signal Processor Targets Mainstream Applications

The ADSP-21065L is the latest member of Analog Devices Inc.'s 32-bit general-purpose programmable floating-point SHARC (Super Harvard Architecture Computer) family. To bring 32-bit performance into mainstream applications, Analog Devices has lowered the price of ADSP-21065L device to $10 in OEM quantities.

With 60 MIPS or 180 MFLOPS at $10 apiece, the ADSP-21065L is expected to bring 32-bit DSP performance to many new audio, automotive, biometrics, communications, and industrial applications, says Gerald McGuire, product line manager at Analog Devices. Plus, the ease of programming a floating-point device with high-level language will attract fixed-point DSP and microprocessor users to the low cost ADSP-21065L-based 32-bit solution, adds McGuire. In fact, he continues, it can process both floating-point and fixed-point math.

The ADSP-21065L also processes 180 million fixed-point operations per second. As a result, the new SHARC processor will facilitate the development of real-time applications such as smart cruise control/collision avoidance systems in automobiles, digital audio in consumer, and speech recognition in computers.

Several factors have contributed to cutting the price of the latest SHARC member. First, the on-chip link ports have been removed. Earlier, these ports enabled multiple SHARC devices to be gluelessly linked with each other for multiprocessing applications. The ADSL-21065L is aimed at low-cost applications in which a single powerful device will suffice, according to the manufacturer.

Secondly, the on-chip memory has been reduced to 544 kbits of SRAM. Memory is a major cost contributor, and it occupies a major segment of the DSP chip. Lastly, the 0.35-µm geometry slashes the die size and power consumption to permit low-cost packaging, further cutting the cost of the DSP chip.

Based on 0.35-µm three metal layer CMOS process, the ADSP-21065L integrates a high-performance 32-bit floating-point DSP core with features like 544 kbits of dual-ported SRAM, host processor interface, direct-memory-access controller, synchronous DRAM (SDRAM) controller, and enhanced serial ports.

The SDRAM controller permits glueless interface to low-cost external memory up to 64 Mbytes. Consequently, it can be linked to various commercially available memory types. In addition, it features an I/O throughput of 240 Mbytes/s. Other key features include two external ports for communicating with external devices, an I_2C interface that supports eight data channels for consumer audio and video systems, and 10 direct-memory-access channels.

According to Analog Devices, the ADSP-21065L is code-compatible with earlier family members ADSP-21060/61/62. Meanwhile, the company has plans to increase the processing power of the 32-bit floating-point digital signal processor to 600 MFLOPS without hiking the price. The 600-MFLOPS version is planned for release sometime next year. The 3.3-V ADSP-21065L comes in a 208-pin PQFP. Sampling now, the chip is slated to go into volume production later this year.

Because the chip is backward-code-compatible, it's supported by all of the existing software-development tools available for the SHARC family. In addition, it will be supported by the visual DSP tool suite, which the company plans to launch later in this quarter. Furthermore, a development board is being readied for the ADSP-21065L.

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Penton Publishing, in joint agreement with CCI Asia-Pacific Ltd., is co-publishing the "new" *Electronic Design China.* In keeping with Penton's strong tradition of editorial excellence, the company has announced that two experienced editors, Mr. Ma Tianfang and Mr. Liu Hong, both former members of the editorial team of the previous version of *Electronic Design China* (formerly known in China as *Electronic Product World),* have been appointed as Editor-in-Chief and Managing Editor respectfully.

Penton has also mandated that 80% of *Electronic Design China's* editorial will be contributed from the pages of Penton's industry-leading technology magazine, *Electronic Design.* Our editors based in Beijing will produce the remaining editorial and over-see the entire editorial presentation, ensuring that all the editorial content is on target for China's growing electronics industry.

Mr. Ma Tianfang
Editor-in-Chief
Electronic Design China

Mr. Ma was formerly the Editor-in-Chief of *Electronic Design China* (formerly known in China as *Electronic Product World).* In addition, Mr. Ma was also Editor-in-Chief of *Electronics International* for ten years. A graduate of Beijing University, he was a senior researcher for the Ministry of Electronics Industries' Institute of Science and Technology Information for 23 years. Mr. Ma is a senior engineer and a member of China's prestigious Electronic Institute.

Mr. Liu Hong
Managing Editor
Electronic Design China

Mr. Liu was formerly the Managing Editor of *Electronic Design China* (formerly known in China as *Electronic Product World).* With 8 years of editing experience, 6 in the electronics arena, Mr. Liu brings authoritative knowledge to his new position. As a graduate of Beijing University, he has authored ten books on various technological subjects. He has also been responsible for research and report writing for China's State Council in the office of the Premier.

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Fast CD-ROM Drive Boasts 80-ms Average Access Time

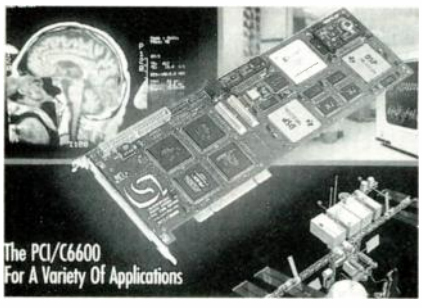
Hitachi America announced what it claims is the industry's fastest CD-ROM drive for personal computers. The CDR-8430 boasts an 80-ms average access time and a 14X-32X maximum data rate. It reads data recorded on all types of CD media, including CD-R and CD-RW discs. The drive uses Hitachi's constant-angular-velocity (CAV) technology, which improves the data-transfer performance and reliability of CD drives by spinning disks at a constant rate. With CAV technology, data-transfer rates increase as the optical reader head moves from the inner to outer tracks of the CD. In addition, the constant motor speed eliminates the need for settling of the optical pickup after seeking data, resulting in an improved access rate compared to drives using older constant linear velocity technology.

The CDR-8430 can transfer data at rates between 2100 to 4800 kbytes/s. The drive uses the E-IDE bus interface and supports DMA Mode 2 to minimize the effect of drive operations on CPU performance. Contact the company for pricing and additional information. JC

Hitachi America Ltd., *Computer Div., Hitachi Plaza, 2000 Sierra Point Pkwy., Brisbane, CA 94005-1835; (415) 589-8300 or (800) 448-2244; Internet: www.hitachi.com.* **CIRCLE 526**

Multiprocessor DSP Board Supports TI's C6x Chip

Suited for use in a variety of embedded DSP environments, the PCI/C6600 DSP board delivers 3200



MIPS of peak processing power. The board, which is designed to support Texas Instruments' C6x DSP chip, is equipped with two 200-MHz TMS320C6201 processors, each with 16 Mbytes of SDRAM and 512 kbytes of SBSRAM. The dual architecture enables the first processor to act as both a data processor and an off-board data router with access to a PCI interface, a DSPLINK2 interface, and TMS320C4x communication ports. The second of the two DSPs is used solely for data processing.

The board is supported by extensive development software from Loughborough and from many third-party vendors. It's priced at $4000 each in OEM quantities. JC

Loughborough Sound Images Inc., *70 Westview St., Lexington, MA 02173; (781) 860-9020; www.lsi-dsp.com.* **CIRCLE 527**

100-MHz 486 Single Component Computer

For embedded applications that require low power consumption, easy integration, high reliability, broad thermal adaptability, and small size, ZF MicroSystems offers a 100 MHz computer in a single in a 240-pin gull-wing footprint smaller than a credit card.

Called the OEMmodule486, the product provides full motherboard system functionality, including serial and parallel I/O, floppy- and hard-disk controllers, AT keyboard and speaker interface, and a Fail Safe Boot ROM. Pre-loaded in 512 kbytes of its 2-Mbyte resident flash disk are a PC-compatible BIOS and DOS. The remaining 1.5 Mbytes are available for the user.

With the OEMmodule 486, there are no cables to cause reliability problems and no mounting hardware that will vibrate loose. It also eliminates the assorted connectors and mounting hardware usually required by single-board computers. The OEMmodule 486 is fully compatible with PC/AT ISA bus.

Operating within a temperature range of –40 to +85°C at software selectable speeds up to 100 MHz, the maximum power consumption is under 2.5 W. Sample quantities are available now, with full production in June. It costs under $200 each in volume. JC

ZF MicroSystems, Inc., *1052 Elwell Court, Palo Alto, CA 94303; (650) 965-3800; www.zfmicro.com.* **CIRCLE 528**

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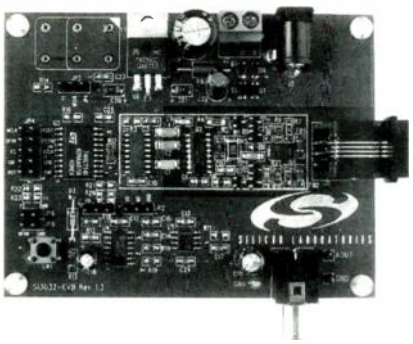
All-Silicon DAA Cuts Cost And Size Of Modem Products

The Si3032 is a silicon-based direct-access-arrangement (DAA) chip set that provides electrical isolation between a telephone device, such as a modem, and the telephone line as required by



FCC Part 68. The two-chip set greatly reduces the cost (up to 50%) and required board space (by a factor of 5) of implementing a telephone interface for modems, fax machines, and telephone line interface systems. At the same time, it improves performance over traditional solutions.

Using the newly developed "ISOLink" technology, the DAA sends digital signals, both data and control, across a transformer-less isolation barrier, eliminating the need for the relays, optoisolators, hybrid circuit, and transformer found in today's modems. The codec also is eliminated because the Si3032 has a direct digital interface to the modem's digital signal processor (DSP). In addition, the Si3032 supports advanced modem features such as caller ID.

The Si3032A and Si3032B each come in a compact 16-pin SOIC package. The Si3032 chip set is priced at $4.80 in quantities of 100,000. Samples are available now and production will begin in the second quarter of 1998. An evaluation board, the Si3032-EVB, also is available for $150. LG

***Silicon Laboratories Inc.**, 2024 E. St. Elmo, Austin, TX 78744; (512) 416-8500; Fax (512) 416-9669, Internet: www.silabs.com.* **CIRCLE 529**

DSS Chip Set Cuts Cost, Boosts Performance And Talk Time

The Hummingbird Digital Spread Spectrum (DSS) cordless-phone chip set lets designers create phones with improved audio quality, customization, flexibility, advanced security features, and intelligent channel-hopping capabilities. Not only can they build phones with these features, but it can be done with fewer parts and lower manufacturing cost. It boasts new power-management features that boost talk time by 30% to five and a half hours, and a 21-day standby time on a 3.6-V battery. The new design also reduces the number of packages required for either the handset or base from five to three.

The chip set is self-configurable for use in either the handset or base. Various telephone configurations can be implemented, including a basic phone, basic two-line phone, and dual keypad phone with half duplex (HDX) speakerphone, with optional caller ID functions. The baseband portion consists of two devices—a linear audio codec and an ASIC. The ASIC integrates a 900-MHz DSS baseband modem, an audio modem, and an embedded microcontroller core. These two devices are packaged together in a single 100-pin PQFP Monopack to minimize system cost. The ASIC and audio codec also are available as separate devices to support more customized OEM designs. Interfaces are provided for all peripheral functions required for a complete DSS telephone, such as keypad, LED, LCD, and EEPROM.

The Hummingbird solution includes all necessary reference-design materials and software-development tools for creating a full-featured phone that can operate from the base station, the handset, or via remote access over telephone lines. To reduce time to market, a royalty-free license is available for fully functional spread-spectrum telephone software, which can be customized by OEMs to add a variety of unique phone features.. Pricing for the Hummingbird starts at $15 in quantities of 50,000. LG

***Rockwell Semiconductor Systems**, 4311 Jamboree Rd., Newport Beach, CA 92658-8902; (800) 854-8099; (714) 221-6996; ww.rss.rockwell.com; e-mail: rockwell@salessupport.com.*
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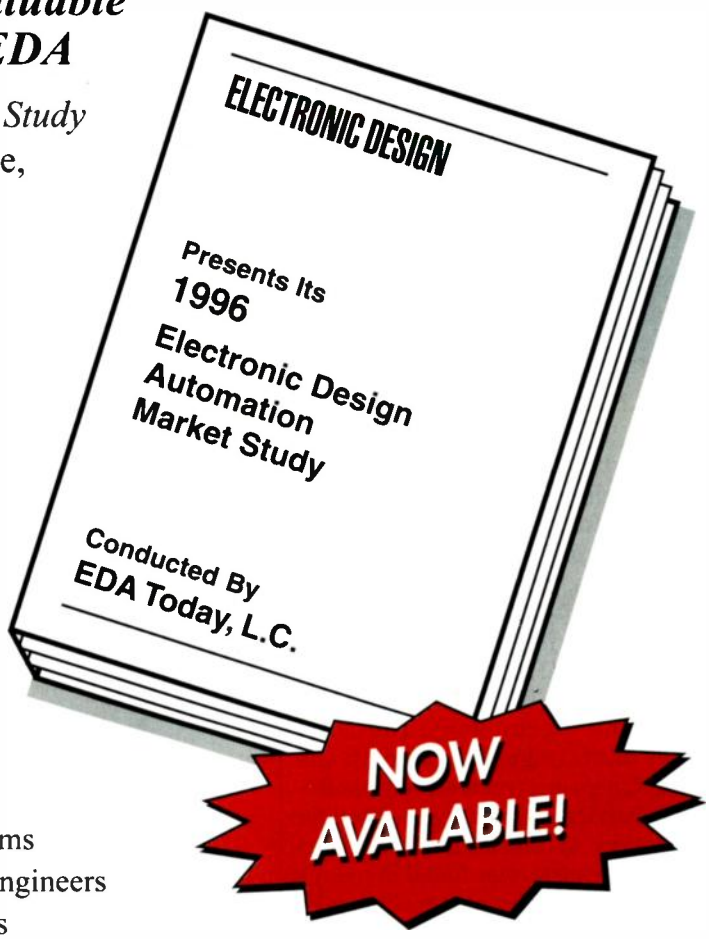

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Distributors Spending More On IT, But Still Wary Of Internet Trade

Distributors are expanding their budgets for information technology at a mean level of $150,000 for last year, according to a survey by the National Electronic Distributors Association (NEDA). The 1998 NEDA Technology Survey was designed to measure the distribution industry's application of technology, including the Internet and Electronic Data Interchange (EDI).

The survey shows that the industry still has concerns about doing business on the Internet. Some 42.5% of respondents said they are somewhat uncomfortable with the prospect of conducting business (for example, electronic commerce) on the Internet. Reasons given include security (82.1%), cost, and inappropriate usage (both cited by 30.8%).

Yet 45.2% of respondents believe the Internet will be an important business tool in the next year. The real value of the Internet, in business, is for communications, according to 52.9% of the respondents. In fact, 80.5% of the companies surveyed had a home page on the Internet.

The survey shows that the industry is also slow to adopt EDI. When asked what percentage of purchase order transactions are conducted via EDI, the average answer (among all respondents) was 11.5%. Manufacturer members led distributor members, however, 21.5% to 12.3%.

Full survey results cost $59 for NEDA members, and $79 for nonmembers. Order from the association at (312) 558-9114.

Semiconductors Firms Ink Distributor Pacts

Several recent agreements have opened up new, or expanded, distribution channels for a range of semiconductor products. Included are mixed-signal ICs, gallium arsenide ICs, and discrete devices.

Insight Electronics, San Diego, Calif., is now handling the entire product line for Cirrus Logic, San Diego, Calif. Insight has been distributing Cirrus' Crystal line of high-performance, mixed-signal ICs for consumer electronics, industrial automation, and instrumentation since 1989. The new agreement includes devices for WAN, LAN, intelligent "net-aware" communications applications, and advanced multimedia chip solutions, both for PC and home entertainment applications.

Contact Insight at (800) 688-7718 or visit *www.insight-electronics.com*.

TriQuint Semiconductor signed a representation and distribution agreement with MEMEC, Hong Kong, for the Hillsboro, Ore., manufacturer's RF, millimeter-wave, analog, and mixed-signal gallium arsenide ICs. The devices will be sold by MEMEC's Unique Divisions in South Korea, Taiwan, China, and Hong Kong, while MEMEC Asia Pacific Ltd. will cover Singapore, Malaysia, Thailand, Indonesia, and the Philippines. TriQuint said it chose MEMEC because of its extensive infrastructure in Asia and its central warehouse in Hong Kong.

Contact TriQuint at (503) 615-8900 or visit *www.triquint.com*.

Finally, Sager Electronics, Hingham, Mass., has received North American sales authorization for discrete semiconductor products from General Semiconductor Inc., Melville, N.Y. With its recent acquisition of ITT Industry Inc.'s Discrete Semiconductor Division, General Semiconductor has more than doubled its product market. The company is now revamping its distribution program to service this increased customer base.

Contact Sager at (781) 740-2300 or visit *www.sager.com*.

Ada Development Systems Distributed By DDC-I

DDC-I Inc., Phoenix, Ariz., is now the exclusive distributor for three Ada development systems, formerly known as Tartan Ada Development Systems (TADS), from Texas Instruments, Dallas, Texas. The agreement with TI gives DDC-I the right to use, distribute, support, maintain, and modify the products, which target the Intel 80960, MIL-STD-1750A, and Motorola M68xxx microprocessors.

DDC-I announced that the new offerings strategically position the company in the real-time, embedded marketplace. The 80960 system completes the company's suite of Ada development tools for the Intel architecture. The MIL-STD-1750A and M68xxx compilers provide mature, highly optimized solutions for these chips, the company said.

For more information, visit DDC-I's web site at *www.ddci.com*.

Crystal, Oscillator Maker Adds North American Reps

Ecliptek Corp., Costa Mesa, Calif., has added The Schoomaker Co., and Beta Technology Sales Inc., to its list of manufacturer's representatives for its quartz crystals and clock oscillators. Headquartered in Richardson, Tex., Schoomaker serves Arkansas, Oklahoma, and Louisiana. Beta Technology Sales is based in Itaska, Ill., and has two sales offices in Wisconsin.

"Schoomaker and Beta Technology are ideal strategic partners for Ecliptek," stated Steve Peak, national sales manager. "It is clear that their established relationships, innovative business tactics, and professionalism will reinforce our business efforts in these regions," says Peak.

For more information, contact Ecliptek at (800) 325-4783, *sales@ecliptek.com*, or visit its web site at *www.ecliptek.com*.

NEDA Publishes Software Guide For Distributors

Distributors needing to buy new business software can finally find some help. The recently released 1998 edition of the *NEDA Software Guide*, published by the National Electronic Distributors Association, offers details on 23 suppliers. These suppliers provide software for distributors, including packages for customer service, inventory control and management, financial reporting and management, and office automation. Each company's systems, services, and software package features are cross-referenced in a convenient reference chart. The guide was compiled by BSW Consulting Inc.

To order the NEDA Software

Guide, call the association at (312) 558-9114. The guide costs $39 for members, and $59 for non-members.

Download Data, Place Orders At Web Site

A new web-based tool, QuickSource, aims to dramatically cut the time it takes design engineers to source products. The site, found on Hamilton Hallmark's home page (*www.hh.avnet.com*), contains more than 100,000 downloadable data sheets. It also features application notes on products available from the company's franchised suppliers. Designers can use their credit cards to order prototype quantities of the products.

"For many engineers, gathering product specifications, and determining the right solution for their design, can be a time-consuming and painstaking process," said Bill Roeder, director of interactive marketing for Hamilton Hallmark, Inglewood, Calif. "QuickSource not only offers all this information in a single place, but then gives our customers the opportunity to order prototype volumes of product. It can significantly reduce the amount of time engineers spend sourcing and procuring products, and ultimately help them get their products to market faster," stated Roeder.

Pioneer Strengthens Its Position In IBM Market

Upon completing its acquisition of Dickens Data Systems, Pioneer-Standard Electronics, Cleveland, Ohio, has become a leading distributor of IBM computer systems, peripherals, and service in North America. Dickens, based in Roswell, Ga., is one of the largest North American distributors of IBM's mid-range products, with revenues of about $347 million last year.

"Dickens Data Systems is an excellent operational fit for our computer systems business, and further underscores Pioneer's strategic commitment to accelerate growth in selected markets worldwide," announced chairman and CEO James L. Bayman.

Compiled and edited by John Novellino, jnovellino@penton.com, (201) 393-6077.

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Digital Design Engineer

The chosen candidate will be responsible for designing integrated circuits using the latest CMOS technology - 0.25 um and below, which will require block architecture, design simulation, synthesis, P & R, and post layout timing verification. The qualified candidate will possess a BSEE (MSEE preferred) coupled with 3 years of relevant experience in the digital design of semiconductors for wireless applications. Working experience with high level languages such as VHDL/Verilog, synthesis, and Place and Route tools is essential. **Job Code: ED-DDE.**

Marketing Development Engineer

The chosen candidate will be responsible for developing new semiconductor activities in the field of wireless communication in North America. Qualified candidates will possess a BSEE (MSEE preferred) coupled with 5 years of relevant experience in marketing semiconductor for wireless applications or systems architecture or applications for cellular phones/pagers. Some traveling in the US and Europe will be required. **Job Code: ED-MDE**

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Will work with BiCMOS and CMOS processes. Must be familiar with Spice/Verilog, behavioral modeling and one or more software methods. Knowledge of precision analog layout preferred. A strong Data Converter background is essential.

Mixed-Signal IC Design Engineers

Will design CMOS and BiPolar circuits such as ADCs, DACs filters and charge pumps for wireless applications. Knowledge of BiPolar, CMOS, Cadence and Verilog is required.

Data Converter/Mixed Signal Design Managers

Will develop product roadmaps for data converters and communication circuits. Involves BiCMOS and CMOS processes. Should have experience leading a team of analog and digital design engineers. BS/MSEE required. Must be familiar with Spice/Verilog. Should be familiar with precision analog layout techniques. A strong Data Converter background is essential.

Product/Test Engineers

Responsible for test program development including test time optimization on LTX and DTS testers. Will work with customer analog products. Requires a BSEE with 2+ years engineering experience. Knowledge of LXT and/or DTS test systems desired.

Test Engineers

Working in the Probe and Test development groups, you will be responsible for test program transfers form Product/Test groups to Probe Test Floor area. Activities will include device, and test hardware/software correlation, probe hardware debug, development of the test program/process and establishing a viable manufacturing test process. Requires a BSEE or related degree, and 3-5 years experience in test engineering and software development with emphasis on product test.

Analog Applications Engineers

Will apply knowledge of analog design (2Mhz and below) in support of our Field Programmable Analog Array. Tasks may include library/macro development, device benchmarking, customer support and interaction with next generation product and software development teams. Requires solid experience in low frequency analog system design.

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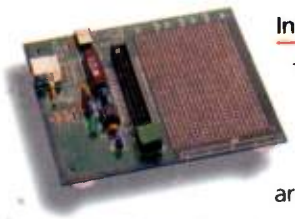

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