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ELECTRONIC DESIGN

TECHNOLOGY • APPLICATIONS • PRODUCTS • SOLUTIONS

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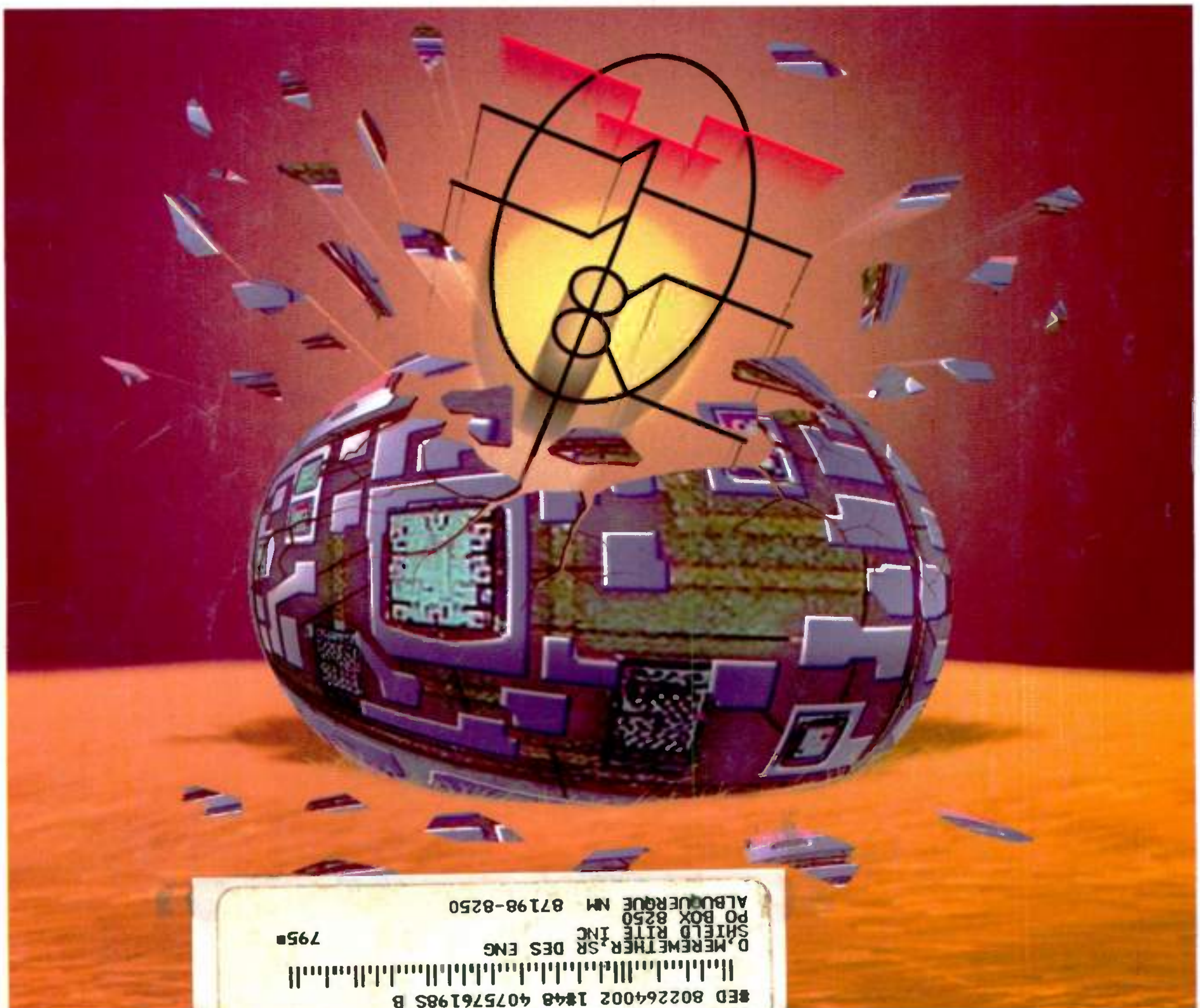

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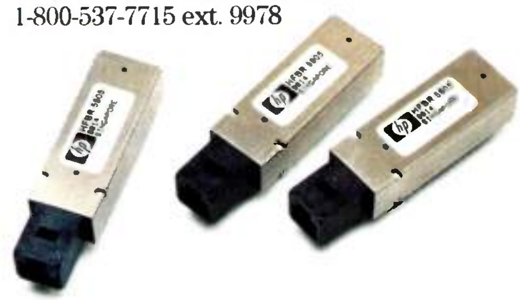

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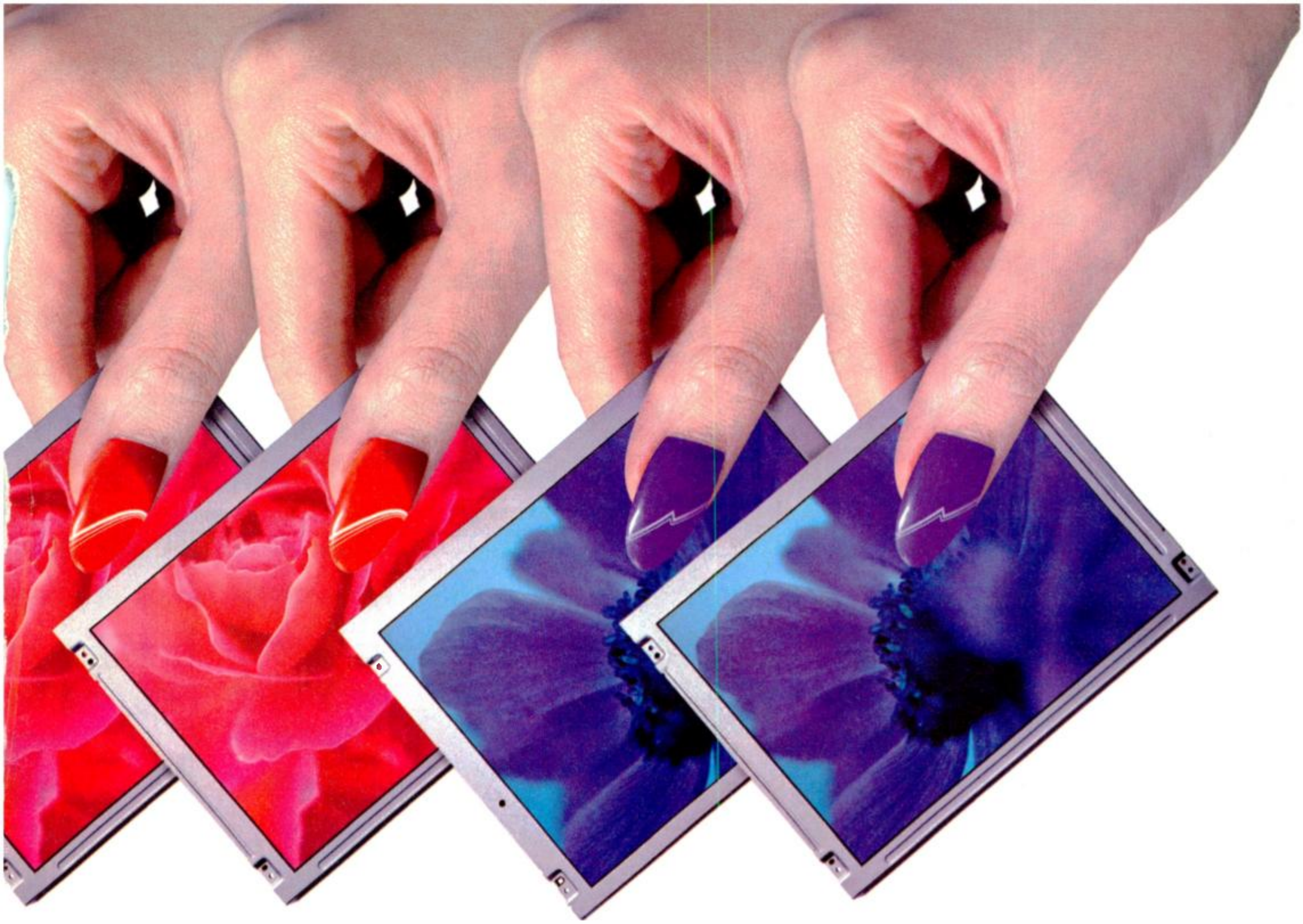

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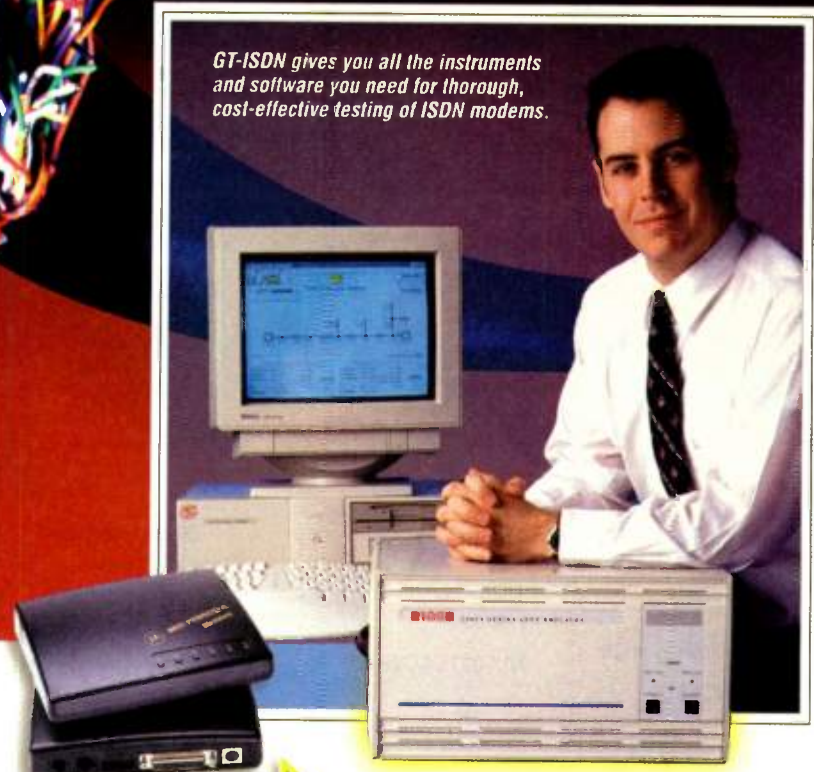

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July 6, 1998 Volume 46, Number 16

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ELECTRONIC DESIGN
TECHNOLOGY•APPLICATIONS•PRODUCTS•SOLUTIONS
July 6, 1998 Volume 46, Number 16

EDITORIAL OVERVIEW

LOOKING AHEAD: July 20, 1998

● **Communications:**........................ Two-way wrist radios? Maybe someday. Until then, Communications Editor Lee Goldberg reports that wireless paging and messaging technology is finding its way into many nontraditional, "off-the-belt" applications within other products.

● **Boards &Buses:**.......................... A Special Report by Computer Systems Editor Jeff Childs notes that because image-processing applications vary so much, it's still a board-level technology. The bus choice depends on the size of the task.

● **Software:**................................ A Special Report by Contributing Editor Ralph Spindell takes a look at the broad range of development tools intended for Java program developers. Many third-generation and high-level tools available for mature languages like C++ are now reaching the Java industry.

COVER ILLUSTRATION BY:
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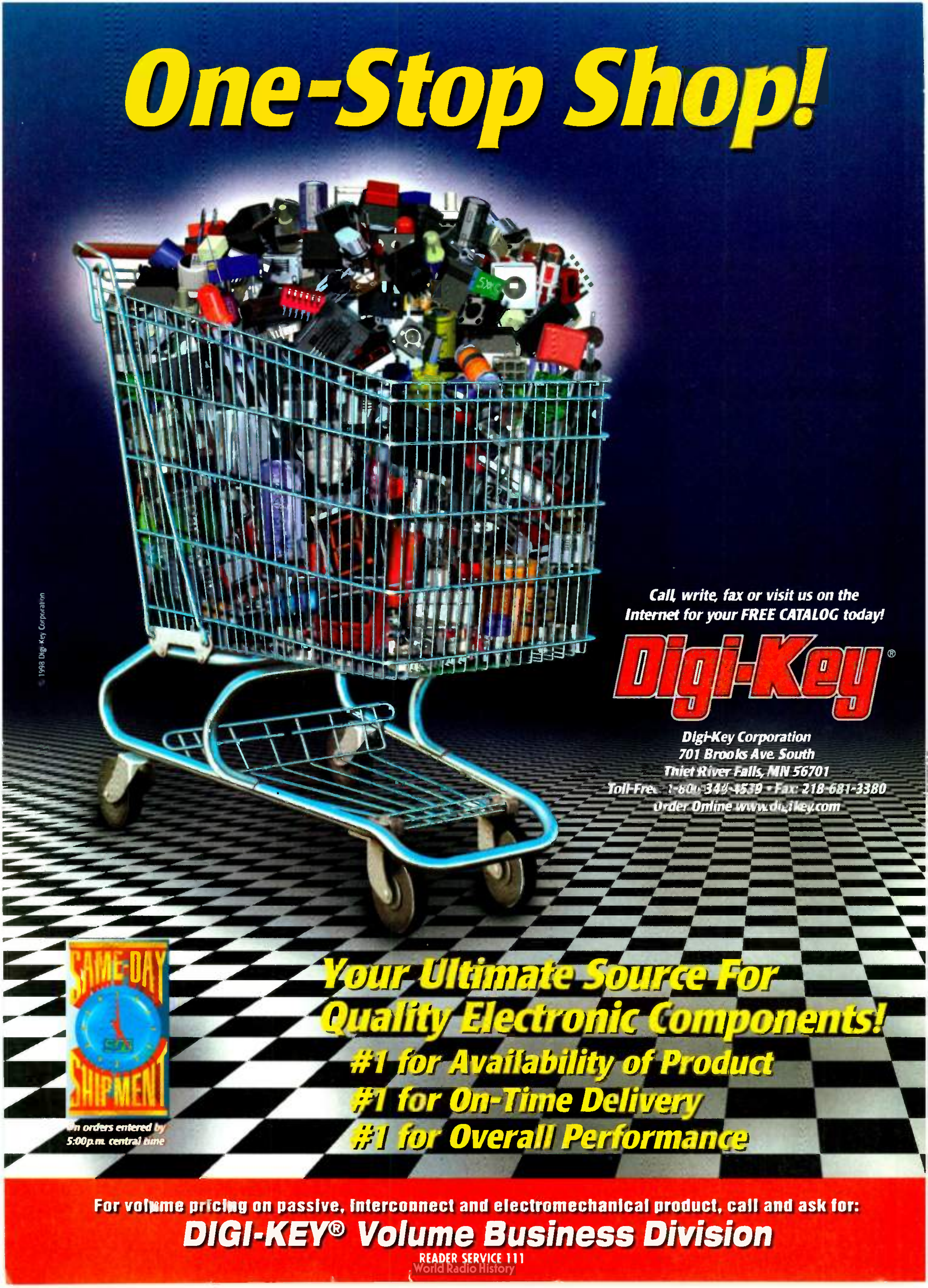
Jesse H. Neal Editorial Achievement

1967 First Place Award	1978 Certificate of Merit
1968 First Place Award	1980 Certificate of Merit
1972 Certificate of Merit	1986 First Place Award
1975 Two Certificates of Merit	1989 Certificate of Merit
1976 Certificate of Merit	1992 Certificate of Merit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ONLINE OVERVIEW

July 6, 1998 Volume 46, Number 16

See Electronic Design Online's Table of Contents to preview what's in store for you on the web!

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Comprehensive listings of what **Electronic Design's** technology editors are working on, including:

- **Editorial Call**--Upcoming features editors are working on, and how readers can contribute material.
- **Face to Face**--Conferences/seminars editors will be attending.
- **What's Going On?**--Short takes on developing stories in the industry.
- **Cool Web Sites**--The editors recommend sites for readers.

For more information, see Press Room in About Electronic Design at www.elecdesign.com.

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Detailed descriptions of distributors/vendors of OEM products, including featured products, special offers, ordering information, and links to company web sites.

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Is hardware/software coverification a mature technology?

NEWS

U.S. Government's Year 2000 Problem resolution plans get failing grades

BOOK SHELF

New releases on LINUX device drivers and parallel port programming

COLUMNS

London Correspondent Peter Fletcher on the gentle art of "Wisteria Weaving"

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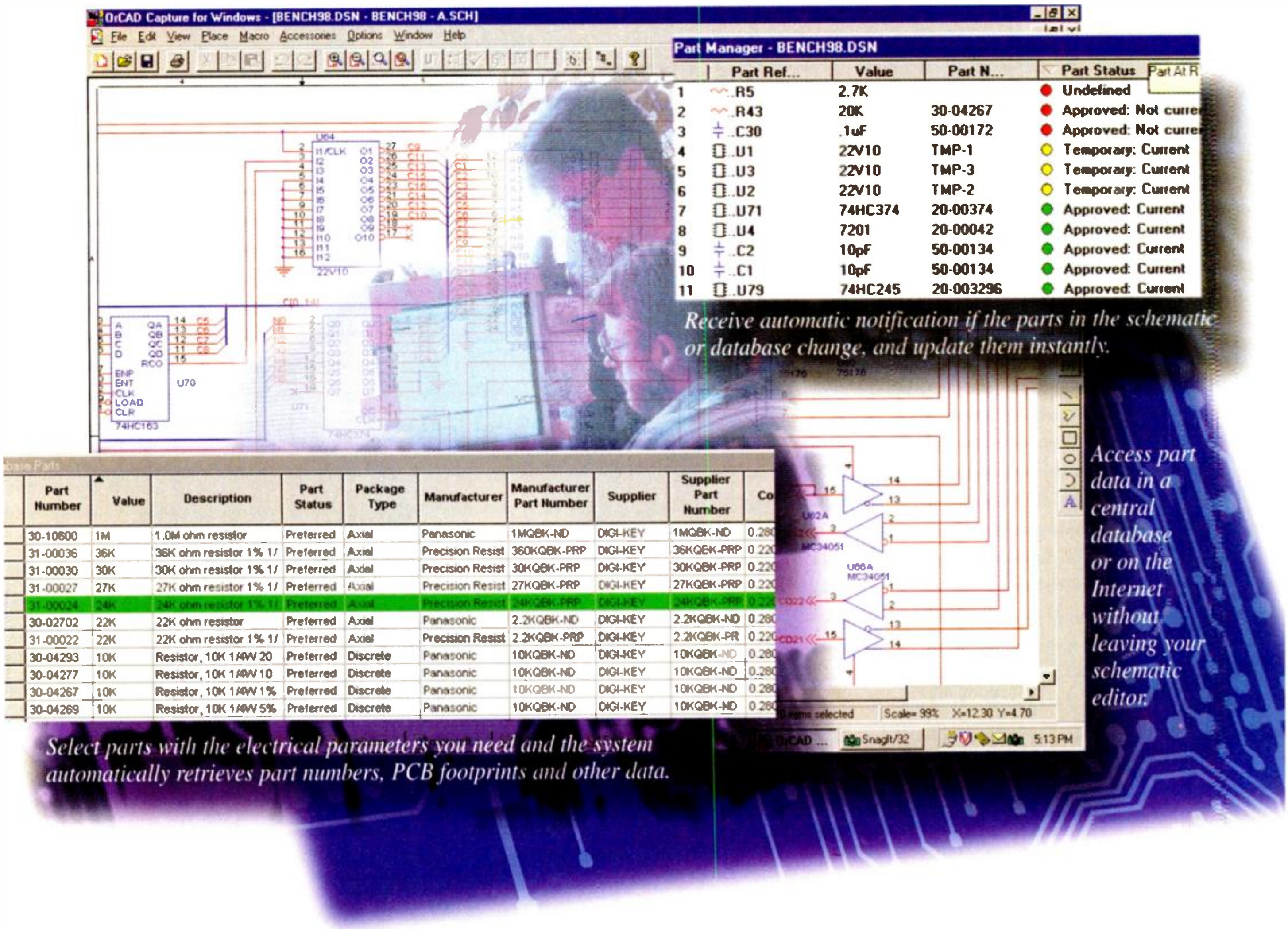
Engineers Spend 30% Of Their Time Researching And Entering Part Data.



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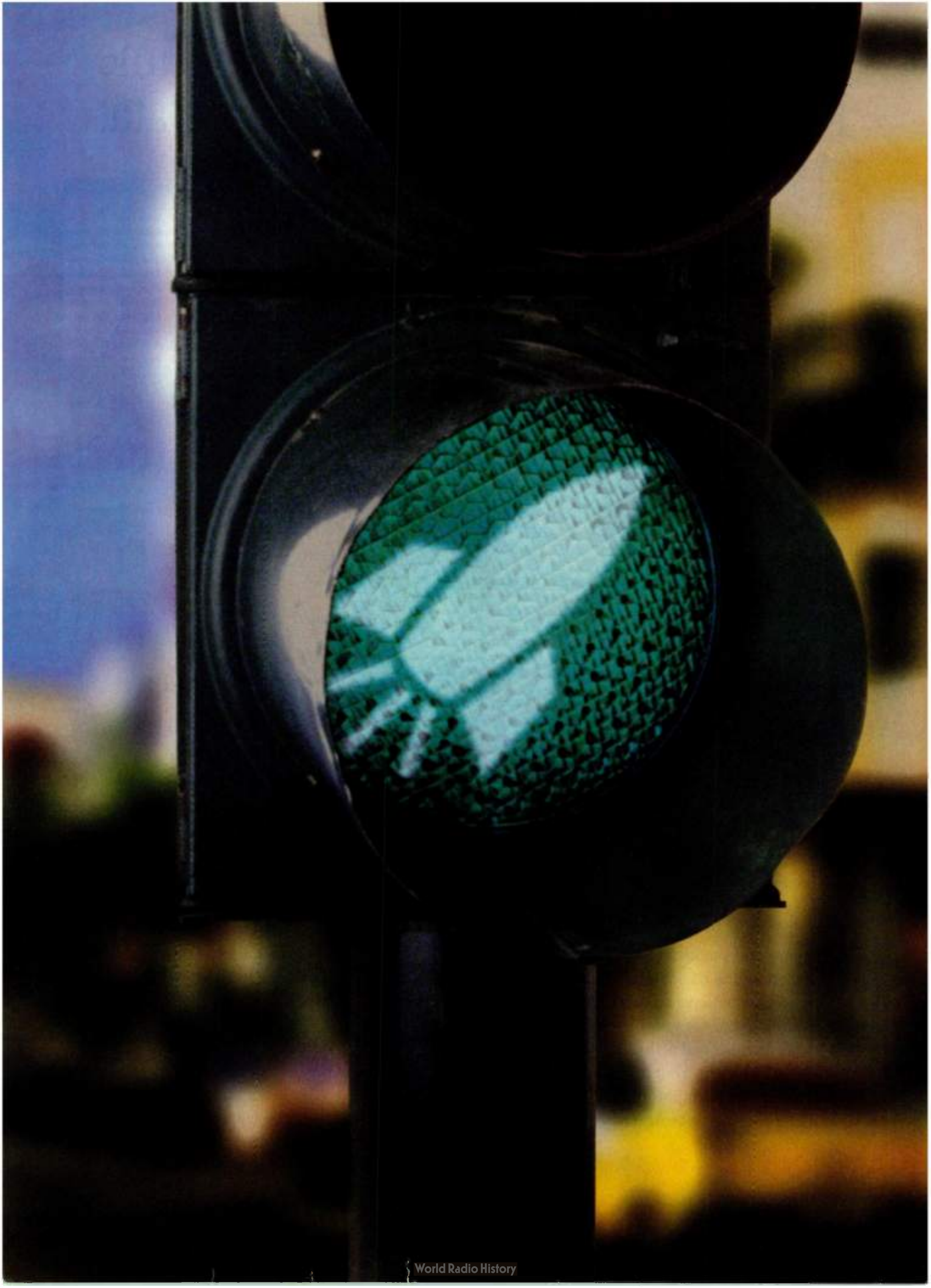
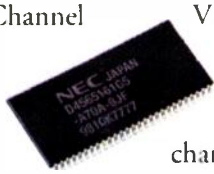


Go faster. Start now.

New memory core technology boosts PC graphics performance up to 100%. Without changes in motherboard design.

Microprocessors keep getting faster while memories struggle to keep pace. Most new memory devices provide faster data transfer rates by improving I/O interface. NEC takes a more radical approach. We've redesigned the memory core and introduced a powerful new architecture called Virtual Channel Memory (VC Memory).



The new architecture features flexible, multiple channels with cache SRAM between memory cells and the I/O interface. The channels store prefetched data while the cells perform read and write operations. These innovations result in higher throughput, faster random access and lower latency.

Introducing 64Mb Virtual Channel Synchronous DRAMs

The first silicon incorporating the new technology is our 64Mb Virtual Channel Synchronous DRAM (VC SDRAM). It features 16 virtual channels, each with 1,024 bits of SRAM. Our VC SDRAMs can raise the graphics performance of PCs up to 100%, and boost overall system performance by approximately 20%. These new 64Mb memories are organized in two banks configured as x4, x8 and x16 bits. They offer three speeds: 100, 125 and 143MHz.

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NEC is offering VC Memory technology at no cost to all memory manufacturers. We're convinced this architecture will become the de facto industry standard. Virtual Channel SDRAMs offer an immediate low-cost solution for designers working on post-SDRAM main memory. For more information, contact your nearest NEC representative.

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And The Verdict Is...

My interest in sports has waned over the years. I don't possess a law degree to help me decipher the daily newspaper's sports section or the legalese spewing out of the talking heads on ESPN. Sports is not about games or competition anymore. It's about arbitration, strikes, contracts, free agency, mediators, lawyers, and judges. Now, I might need to brush up on the law just so I can follow what's currently making news in our industry. Is there an "Antitrust Law for Dummies" book out there?

As the whole world knows by now, both Microsoft and Intel have ticked off the Justice Department and the Federal Trade Commission, respectively. The two superpowers may have violated antitrust laws. From my high school days, I recall that it was around 1890 when the Sherman antitrust laws were established. From then on, big oil and railroad barons could not use their girth to squash all competitors. In Microsoft's case, the antitrust charges are at least clear. The software behemoth is charged with using predatory pricing strategies and other questionable and illegal tactics to wax the competition. Microsoft denies the charges...see you in court.

But, the Intel suit doesn't seem to violate the traditional antitrust rulebook. It is three of their customers, not their competitors, whom Intel is accused of threatening and damaging. The suit alleges that they bullied Compaq, Intergraph, and Digital Equipment. The companies were given a choice of licensing their technologies to Intel or face being shut out from the supply chain of advanced chip information. All three companies need to build products based on Intel's microprocessors. No information, no products. No products, no companies.

Is this a true antitrust case? Compaq and Intergraph aren't in the chip manufacturing business. And it would be a long stretch to imagine Digital and its Alpha chip as competitors. No, what we have here is a major league intellectual property (IP) issue. It was bound to happen. I don't think any other issue is debated as hotly within our industry as IP. The FTC's antitrust action against Intel is a move to stretch the antitrust laws. Or, it's a way to set new laws for the nature in which high-tech companies do (or don't do) business in today's world.

I don't believe either of these two suits will ever get to the "...and the verdict is..." stage. The platoons of clever lawyers on all sides will get together for lunches and bang out settlements. What will be interesting to observe from the Intel suit is where the IP issue goes from here.

Tom Halligan
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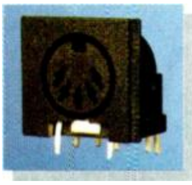

Customer Research Spurs Innovation

Has your company done any customer research lately? If not, you may be missing out on a great way to foster product innovation. Take, for example, a recent product announcement by Hewlett-Packard—the HP 16600A and 16700A series of logic analysis system mainframes. These products, which combine logic analysis and emulation, were a result of the input of thousands of designers worldwide.

Digital-systems design-team members told HP that it is common to start a new design without a clear picture of how they will debug the product along the way. (HP says digital design teams typically consist of five to seven software/firmware designers for every hardware designer.)

According to HP, there are numerous challenges brought on by market expectations and technical possibilities. They can be categorized as those created by new-generation microprocessors and microcontrollers, product designs and business pressures, and traditional debugging tools.

About the challenges presented by traditional debug tools, designers told HP they were getting less support from their debug tools. The emergence of fast processors and complex designs exposes the major weaknesses of traditional in-circuit emulators (ICE). Specifically, HP's global customer research uncovered five problem areas. These were: intrusiveness can change the behavior of the system under test; ICEs have little or no ability to show system activity beyond the processor; debugger quality is sacrificed because customers are forced to use tools from ICE vendors, rather than choose from the best debuggers on the market; real-time trace depth is often insufficient for today's complex systems; and designers have no way to correlate software behavior with hardware activity.

JOSEPH DESPOSITO
TEST & MEASUREMENT

HP also discovered a lack of coordination between hardware and software designers in the selection and use of debug tools, which frustrates and delays the design process. For example, the discrepancies in results when using a logic analyzer, as opposed to an emulator, causes conflict between hardware and software teams, because the teams lack a common set of data to analyze.

Further, processor support is often late, or even nonexistent, with ICE. HP believes this is a financial issue. Motivation to develop emulators lessens as new processors proliferate, because each new processor has a short life span. It is a struggle for tool vendors to create emulators for complex, high-speed processors.

But, logic analyzers also have their shortcomings. When considering traditional logic analyzers as an alternative to in-circuit emulators, software designers had several complaints. Most logic analyzers lack some key debug tools, such as code download, target control, and good debugger connections. Also, software designers find connecting logic analyzer probes difficult.

ICE and logic analyzers alike have been perceived as expensive. Designers complained about the need to buy new emulation hardware for each new processor and to learn new tools each time a new processor is used. Customer research concluded that the frustration of using old tools to solve new problems posed by complex digital systems is so acute that designers in a wide range of industries are looking for alternatives.

Responding to this customer feedback, HP blended both technologies—logic analysis and emulation—into its new products. HP is hoping to provide design teams with more control of, and visibility into, system behavior than is possible with a logic analyzer or emulator alone.

If your company is struggling to come up with new product ideas, invest in customer research. It pays off.

Joseph Desposito can be reached at jdespo@ix.netcom.com.

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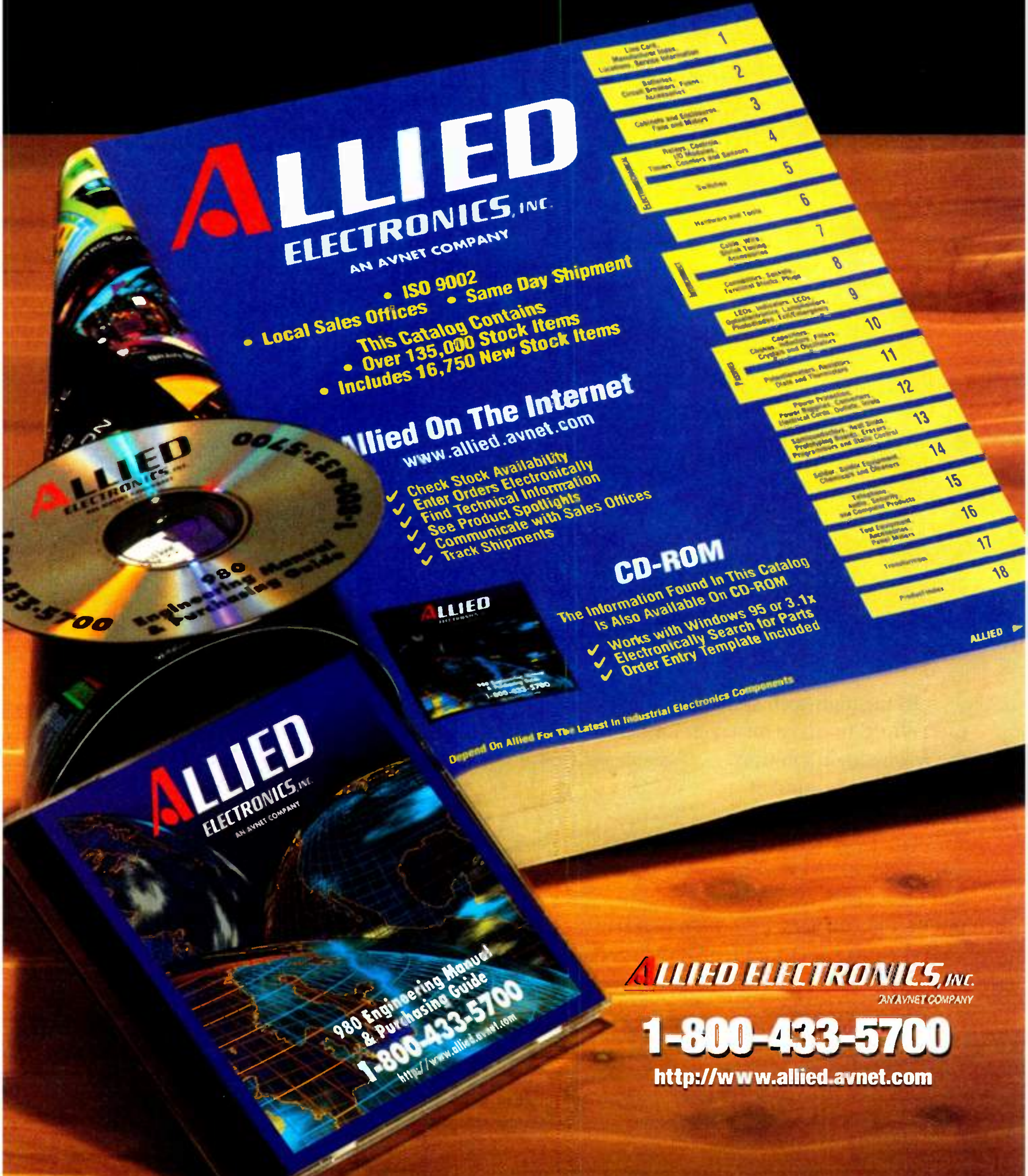

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Slanted Package Mounting Technology Boosts Card Density

Hitachi Semiconductor (Brisbane, Calif.) Inc. and Hitachi ULSI Systems Co. Ltd. announced the development and patenting of a new Flash component mounting technology. It will result in the industry's largest capacity PCMCIA flash cards to date—300 Mbytes.

The new technology, called slanted package mounting, provides a way to increase the storage capacity of flash cards four-fold. Hitachi's slanted-package-mounting technology uses ultra-thin TCP (Tape Carrier Package) flash components arranged in an angled configuration, as opposed to traditional TSOP stacking methods that employ a flat orientation. This makes it possible for the company to quadruple the memory densities of its flash cards by fitting four times the memory within the same space on the card. For example, it can fit 40 TCP-packaged 64-Mbit components on one PCMCIA card. Consequently, densities of 300 Mbytes per card are acheivable.

For more information concerning the flash-card technology, contact Hitachi Semiconductor (America) Inc., 2000 Sierra Point Parkway, MS-080, Brisbane, CA 94005-1897; fax: 303-297-0447; Internet: *www.hitachi.com/semiconductor.* JC

PCI SIG Releases PCI v2.2 Specification For Review

The Peripheral Component Interconnect Special Interest Group (PCI SIG) has made the v2.2 of the PCI Local Bus standard specification available for member review. The latest version of the PCI standard includes the new functionality of PCI Hot-Plug and PCI Power Management, in addition to a roll-up of Engineering Change Notices (ECNs) and errata since version 2.1 was completed in August 1995. Version 2.2 is essentially a "clarification release" of the specification.

The major elements of v2.2 PCI Hot-Plug and PCI Power Management have been in the works since last fall, and contains no major surprises. PCI Hot-Plug provides the ability to insert and remove PCI adapter cards without shutting the system down. PCI Power Management addresses the issues of power management and energy conservation on the PCI bus. Working with the operating system, it allows expansion cards to be powered down when not in use and powered up when in demand.

After incorporation of any post review changes, v2.2 is expected to be formally released this month. For more information, contact PCI SIG via phone at (800) 433-5177 (within the U.S.) or fax at (503) 693-8344, or visit the PCI SIG web site at *www.pcisig.com.* JC

Edited by Roger Engelke

Superconducting Imaging Surface Slashes Cost Of Measuring Brain Activity

The U.S. Department of Energy's Los Alamos National Laboratory has unveiled a new medical instrument which measures brain activity. This instrument is expected to aid physicians in assessing patients with brain injuries and diseases. It also may help solve the mystery of how the brain works.

The whole-head magnetoencephalography (MEG) sensor system is a method of measuring the tiny magnetic fields that are produced when groups of the brain's 100 billion or so cells (neurons) are active. The fields are generated by electrical currents resulting from thought, sound, muscle movement impulses, and other types of brain activity.

The helmet-like system contains 155 ultra-sensitive sensors, known as superconducting quantum interference devices (SQUIDS). Atop the device is a unique shield that screens out electrical and magnetic interference, and an instrument column, immersed in liquid helium, that maintains the SQUIDS at –450°F.

The SQUIDS record the magnetic fields produced by active neurons, and display the fields as topographic maps. Computer models calculate the locations and durations of brain activity. They then project maps of those active neurons on three-dimensional magnetic resonance imaging (MRI) displays of the brain.

Previous MEG systems required costly, specially constructed rooms to shield SQUID sensors from external magnetic fields, such as those generated by building wiring and lighting systems. The Los Alamos breakthrough is a patented, superconducting imaging surface. This unique superconducting shield repels interfering magnetic fields and simultaneously, it focuses the magnetic fields generated by brain activity, greatly reducing the time needed to measure brain activity. Use of such innovations should reduce the cost of MEG from about $3 million to less than $500,000.

The shield incorporates a cryogenic material similar to Corian, which is used for some kitchen countertops. Los Alamos holds a joint patent for the material with DuPont Corp., Wilmington, Del.

Photolithography techniques, similar to those used to make electronic circuits, will allow the lab to etch the conducting loops into the helmet's interior. The conducting loops register the brain's magnetic signals. Manufacturers can then mass-produce the sensor surfaces, and install more sensors into the helmet. More sensors will reduce the time needed to make measurements, as well as increase the amount of available information.

Los Alamos has completed preliminary tests of the new, full-head MEG system, and is ready to begin initial measurements of human subjects. The system will then be installed at the Albuquerque Veterans Administration Center for clinical trials.

For more information, contact Jim Danneskiold, Los Alamos National Laboratory, Los Alamos, N.M. 87545; (505) 667-1640; e-mail: slinger@lanl.gov; www.lanl.gov.

Joseph Desposito

Bluetooth Initiative Bites Into RF Wireless Network, Linking Laptops To PDAs, Phones, And More

How would you like an RF wireless, local-area network (LAN) to link your laptop computer to communication devices up to 10 meters away? You'd love it, and so would most other people. That's why five major players in the industry came together in an initiative code-named "Bluetooth." Members hope to create firm specifications for just such a network by early next year, with limited product availability by mid-1999.

In the free-use 2.45-GHz portion of the spectrum, the transmitter's RF output would be less than 100 mW (an external power amplifier could boost the range up to 100 meters). With such a limited distance, symbol rates of up to 1 Mbit/s are possible. One-on-one connections allow for a maximum data transfer rate of 721 kbits/s (three voice channels). For most system requirements, this should provide sufficient connectivity. But, for users who need higher data rates, a 2 Mbit/s version of Bluetooth is also in development.

The radio technology will employ a packet-switching protocol, based on a fast frequency-hopping scheme (1600 hops/s), which can operate even in high-noise environments. The approach is similar to that used in the IEEE-802.11 wireless LAN specification. Additionally, the transmitter uses an adaptive power output to minimize interference with other nearby units. The communication protocol utilizes short data packets to maximize capacity during interference. A fast acknowledge capability allows low coding overhead for the links.

For voice transmission over the link, the Bluetooth standard will use continuous-variable-slope delta modulation (CVSD), despite high bit-error rates. The air interface is tailored to minimize current consumption and keep battery power drain to a minimum—just 0.3 mA on standby, and 30 mA when transmitting. Like Ethernet nodes, a unique 48-bit address is allocated to each transmitter/receiver. Thus, any device which contains a Bluetooth transceiver is uniquely identifiable.

Individuals with Bluetooth-enabled devices could, if within range of a Bluetooth system, automatically synchronize data bases, transfer data, or perform some other task—without touching their systems. The protocol used for system handshaking is coupled with the "wake-on-LAN" capa-

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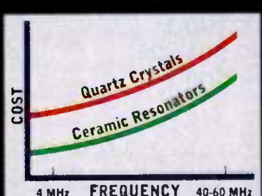

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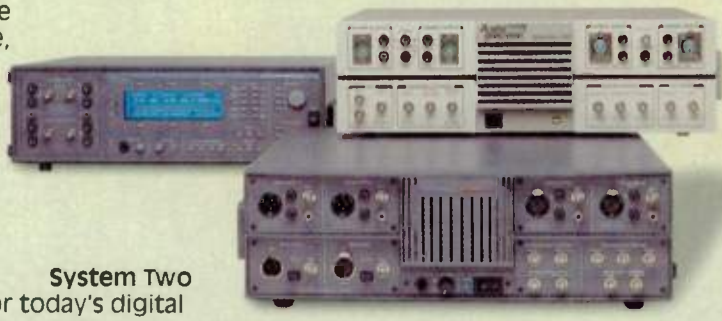

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DESCRIPTION

The FT and FS Series are comprehensive lines of ultra compact power factor corrected models derived from our Moduflex® family of switching power supplies. This series utilizes advanced technology to produce a high quality input current wave form that is compliant to the harmonic requirements of EN61000-3-2. Based on modular construction, "off the shelf" modules permit high volume manufacturing with an outstanding quality level assuring timely delivery at a competitive cost.

Three classes of output modules are available. The **STANDARD** outputs allow short duration surge currents on all auxiliaries for hard starting loads. Optional **CURRENT LIMITED** outputs have square current limiting and feature wireless droop current sharing. Optional **ENHANCED** outputs have square current limiting, one wire star point current share, output good logic signal with LED, nominal 5V local bias, individual inhibit and margining. For requirements that cannot provide minimum load on the main output, the **ZERO PRELOAD** option is available for main outputs up to 500 watts.

DELIVERY

Choose stocked units or construct a model number using stocked modules for fast delivery. Otherwise, form a model from the adjacent page to meet your specific requirements. Contact factory for deliveries on models derived from non-stocked modules.

FEATURES

- 0.99 power factor.
- 5.5 watts per cubic inch.
- 1-7 outputs, 400-1000 watts.
- 120 kilohertz MOSFET design.
- Universal input.
- UL, CSA, TÜV (IEC, EN), CE.
- FCC, EN Class A EMI.
- IEC, EN Immunity.
- All outputs:
  - *Adjustable*
  - *Fully regulated*
  - *Floating*
  - *Overload and short circuit protected*
  - *Overvoltage protected*
- Standard features include:
  - *System inhibit*
  - *Fan output*
- Options and accessories include:
  - *Power fail monitor*
  - *Redundancy*
  - *Current Limited Outputs*
  - *Enhanced Outputs*
  - *Zero Preload*
  - *End fan cover*
  - *Top fan cover*
  - *Rack Assemblies*

STOCKED MODELS - Available in 3 days.

Max Power	Output 1	Output 2	Output 3	Output 4	Model*
400W	5V @ 50A	12V @ 12A	12V @ 12A	5V @ 10A	FT46A2332-45P
400W	5V @ 50A	12V @ 12A	24V @ 6A	12V @ 6A	FT46A2363-45P
600W	5V @ 60A	12V @ 12A	12V @ 12A	5V @ 10A	FT46C2332-13P
600W	5V @ 60A	12V @ 12A	24V @ 6A	12V @ 6A	FT46C2363-13P

**400W models include power fail monitor, current limited modules, zero preload and end fan cover options. 600W models include the same options except fan cooling is built into the unit.*

UNITS FROM STOCKED MODULES - Available in 2 weeks.

FT 44 B 2 3 3 6 - YY X

Series — FT
Configuration — 44
Power Code — B
Output #1 Code — 2
Output #2 Code — 3
Output #3 Code — 3
Output #4 Code — 6
Sum of Option Codes — YY
Output #1 Variant — X

Configuration: Allowable quad output configurations are 42, 44, 46 and 48.
Power Code: Choose Power Code A through D for 400-750W models.
Output Codes: Select any outputs from the shaded area on the Output Types table consistent with the configuration chosen.
Option Code: Specify Option Code. Refer to the Option table. Codes 02 (redundancy) and 16 (enhanced) are excluded from models available in 2 weeks. Fan cooling is built into 600 and 750W units.

OPTIONS

Option Code	Function
00	None
01	Power Fail Monitor
02	Redundancy
04	Current Limited
08	Zero Preload
16	Enhanced
32	End Fan Cover
64	Top Fan Cover

Replace the YY with the sum of the Option Codes.

MODEL SELECTION

Models are available in power ratings of 400 to 1000 watts, with corresponding code letters A through E. See Power Code chart.

Output modules are available in six types: J, K, L, M, N and P in nominal power ratings from 75 - 500 watts. Type M, N and P modules are variable power rated depending upon the unit power rating. The M, N and P Module table directly below shows the corresponding multiplier applicable to the output current ratings of the M modules and allowable power ratings for the N and P modules. For example, a 750 watt multiple will have its M type module configured to produce 120A @ 5V or 12A @ 48V. The voltage and current rating of output modules are listed in the table of output types. This table assigns an alpha-numeric code designating the nominal voltage rating of the module.

Power Code	Unit Power Rating	M Module Current Multiplier		N/P Module*
		Single Output	Multiple Output	Allowable Power Rating
A	400W	0.8	0.5	250W
B	500W	1.0	0.6	300W
C	600W	1.2	0.8	400W
D	750W	1.5	1.2	500W
E	1000W	2.0	1.5	750W

**When an N or P module is used as the main output, the allowable power and the module current ratings must not be exceeded.*

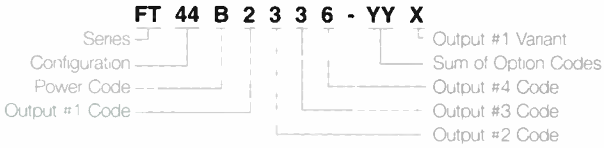
Output Types*						
Output		Module Type				
Code	Volts	J Amps	K Amps	L Amps	M Amps	N/P Amps
0	2	10	20	30	100	60
1	3.3	10	20	30	100	60
2	5	10	20	30	100	60
3	12	6	12	24	42	42
4	15	5	10	20	33	33
5	18	4	8	16	28	28
6	24	3	6	12	21	21
7	28	2.5	5	10	18	18
8	36	2	4	8	14	14
9	48	1.5	3	6	10	10
A	2.2	10	20	30	100	60
B	2.4	10	20	30	100	60
C	2.7	10	20	30	100	60
D	3	10	20	30	100	60
E	3.6	10	20	30	100	60
F	4	10	20	30	100	60
G	4.5	10	20	30	100	60
H	5.7	10	20	30	90	60
J	6.3	10	20	30	80	60
K	7	9	18	30	70	60
L	8	8	16	30	62	60
M	9	8	15	30	56	56
N	10	7	14	30	50	50
P	11	7	13	27	45	45
Q	13.5	6	11	22	37	37
R	17	5	9	18	30	30
S	19	4	8	16	26	26
T	21	4	7	14	24	24
U	23	4	7	13	22	22
V	26	3	6	12	19	19
W	29	3	5	10	17	17
X	32	2	5	9	16	16
Y	40	2	4	8	13	13
Z	44	2	4	7	12	12

Multiple output modules of a given type are arranged in ascending order by voltage magnitude in the same sense as the output number sequence in the configuration diagrams.
**Shaded ratings are stock.*

HOW TO ORDER

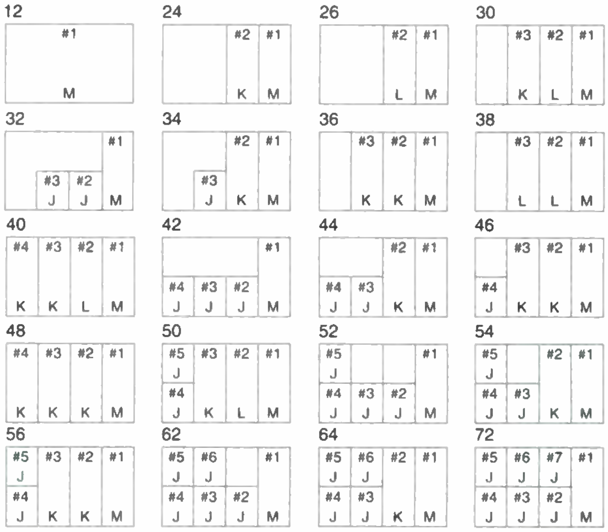
To form the proper model number defining a custom requirement, select the letters FS or FT to designate the series, then choose the desired configuration and list the configuration code. Insert the power code letter for the power level and follow with the output code numbers or letters for each specific output. Enter a dash and from the option table insert the sum of the option codes. Where lower power is desired for the main module, an N module can be substituted and is denoted by a letter N in the output variant position. In addition, when no preload is available for the main output, choose Option Code 08 and add a P in the output variant position. For an enhanced **main** and **current** limited auxiliaries, specify both 04 and 16 option codes.

HARMONIC CORRECTED 500W QUAD SWITCHER



OUTPUT CONFIGURATIONS

The boxes below are diagrammatic representations of the power supplies as viewed from the output end. The two-digit numbers above the boxes are the configuration codes.



Refer to the table below for allowable configurations by series.

Output Config	Unit Power Rating				
	400W	500W	600W	750W	1000W
12	•	•	• x	• x	x
24	•			• x	
26		•	• x	• x	x
30					x
32	•			• x	
34	•	•	• x	• x	
36	•	•	• x	• x	x
38					x
40					x
42	•	•	• x	• x	
44	•	•	• x	• x	x
46		•	• x	• x	x
48			x		x
50					x
52	•	•	• x	• X	x
54		•	• x	• X	x
56			x		x
62		•	• x	• X	x
64			x		x
72			x		x

• Represents allowable configurations for the FT Series.
x Represents allowable configurations for the FS Series.

SPECIFICATIONS

INPUT
90-264 VAC, 47-63 Hz.

POWER FACTOR
0.99 typical.

EMISSIONS
FCC 20780 Part 15/EN 55022, Class A Conducted. EN 61000-3-2, Harmonics. EN 61000-3-3, Voltage Fluctuations.

IMMUNITY
IEC 1000-4-2/EN 61000-4-2, Electrostatic Discharge. IEC 1000-4-3/EN 61000-4-3, Radiated Field. IEC 1000-4-4/EN 61000-4-4, Electrical Fast Transients. IEC 1000-4-5/EN 61000-4-5, Level 3 Surge. IEC 1000-4-6/EN 61000-4-6, Conducted Field.

INPUT SURGE
230 VAC - 38 amps max. 115 VAC - 19 amps max.

EFFICIENCY
75% typical.

HOLDUP TIME
20 milliseconds from loss of AC power.

OUTPUTS
See model selection table. Outputs are trim adjustable ±5%.

OUTPUT POLARITY
All outputs are floating from chassis and each other and can be referenced to each other or ground as required.

LINE REGULATION
Less than ±0.1% or ±5mV for input changes from nominal to min. or max. rated values.

LOAD REGULATION
±0.2% or ±10mV for load changes from 50% to 0% or 100% of max. rated values.

MINIMUM LOAD
Main output requires a 10% minimum load for full output from auxiliaries. Use Option 08 if no minimum load is available for mains up to 500 watts. Singles require no minimum load.

RIPPLE & NOISE
1% or 100 mV, pk.-pk., 20 MHz bandwidth.

OPERATING TEMPERATURE
0-70°C. Derate 2.5%/°C above 50°C.

COOLING
A min. of 10 LFS* for models without internal fans directed over the unit for full rating. Two test locations on chassis rated for max. temperature of 90°C. 600 watt, 750 watt and 1000 watt models have built-in ball bearing fans.
*Linear feet/second.

TEMPERATURE COEFFICIENT
±0.02%/°C.

DYNAMIC RESPONSE
Peak transient less than ±2% or ±200 mV for step load change from 75% to 50% or 100% max. ratings.

RECOVERY TIME
Recovery within 1%. Main output - 200 microseconds. Auxiliary outputs - 500 microseconds.

SAFETY
Units meet UL 1950, CSA 22.2 No. 950, EN 60 950, IEC 950.

ISOLATION
Conforms to safety agency standards.

INPUT UNDERVOLTAGE
Protects against damage for undervoltage operation.

SOFT START
Units have soft start feature to protect critical components.

OVERVOLTAGE PROTECTION
Standard on all outputs.

REVERSE VOLTAGE PROTECTION
All outputs are protected up to load ratings.

OVERLOAD & SHORT CIRCUIT
Outputs protected by duty cycle current foldback circuit with automatic recovery. Standard auxiliaries have additional back-up fuse protection. Options 04 and 16 have square current limiting with automatic recovery when overload is removed.

THERMAL SHUTDOWN
Circuit cuts off supply in case of local over temperature. Units reset automatically when temperature returns to normal.

FAN OUTPUT
Nominal 12 VDC @ 12 watts maximum.

INHIBIT
TTL compatible system inhibit provided. Option 16 has individual output inhibit.

REMOTE SENSING
On all outputs except standard and 04 Option outputs 75 watts or less.

SHOCK & VIBRATION
Shock per MIL-STD 810-E Method 516.4, Procedure I.
Vibration per MIL-STD 810-E Method 514.4, Category 1, Procedure I.

MECHANICAL

CASE	SERIES	WATTS	H	x	W	x	L
1	FT	400W/500W	2.50"	x	4.93"	x	8.00"
3	FT	600W	2.56"	x	5.08"	x	10.03"
4	FS	600W	2.56"	x	5.08"	x	11.00"
5	FT	750W	2.63"	x	5.20"	x	10.03"
6	FS	750W	2.63"	x	5.20"	x	11.63"
7	FS	1000W	2.56"	x	7.13"	x	11.63"

OPTIONS

POWER FAIL MONITOR
Optional circuit provides isolated TTL and VME/VXI compatible ACFAIL signal providing 4 milliseconds warning before main output drops by 5% after an input failure. A SYSRESET signal following VME timing requirements is provided when an N module is used as a main output. Both logic signal outputs can sink current per the VME specification.

REDUNDANCY
Optional Or-ing diodes for hot pluggable N+1 redundant operation. For FT Series 500 watt & 750 watt models with 1-4 outputs. Main output current limited to 100 amps. Remaining outputs 16 amps max.

CURRENT LIMIT
Option provides on all outputs:
- Square current limit with auto recovery.
- Wireless droop current share for parallel or N+1 redundant operation.

ZERO PRELOAD
Optional circuit removes need for preload on main output up to 500 watts.

ENHANCED
Option provides on all outputs:
- Square current limit with auto recovery.
- Single wire active current share for parallel or N+1 redundant operation.
- DC output good logic signal with LED indicator.
- Logic inhibit.
- Nominal 5V bias.
- Margining.

END FAN COVER
Optional cover with brushless DC ball bearing end fan which provides the required air flow for full rating.

TOP FAN COVER
Same as above with fan cover mounted on top of the power supply.

ACCESSORIES
RA50 and RA75 Series 2U high rack assemblies provide hot pluggable interface and hold up to 3 FT Series 500 watt or 750 watt units respectively.

Specifications subject to change without notice.

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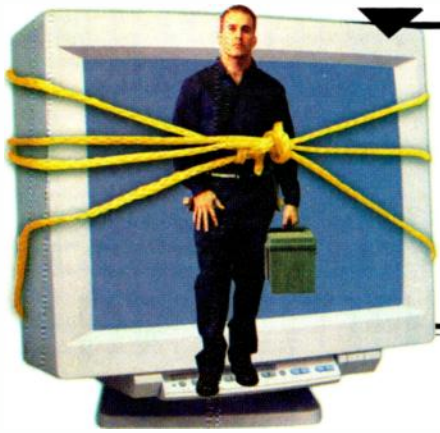

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- **Power Supply Voltages**: monitors up to six
- **System Security**: reports when case is opened, even if power is off
- **Programming Simplicity**: popular 2-wire interface with 2-bit addressability
- **Wide Operating Range**: from 2.8V to 5.75V

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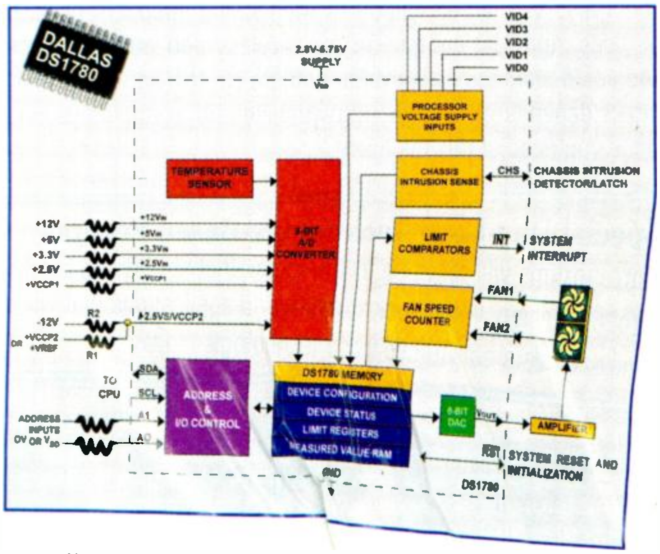

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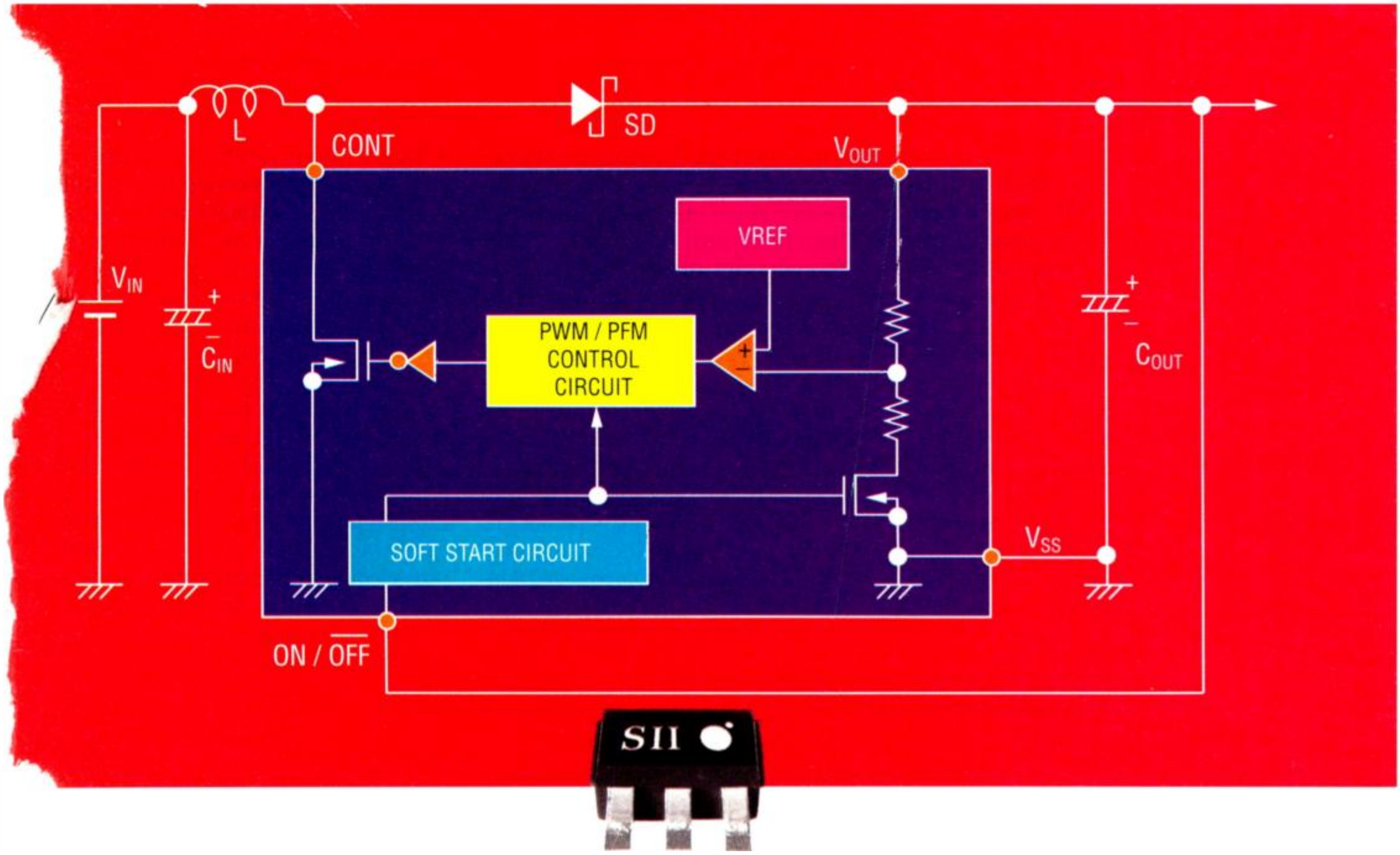

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Model	VOUT
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bility. When a receiver, which is in low-power listen mode, detects an incoming message, it can wake up the host system (a laptop, for instance). Both systems will then perform the desired operation. Afterwards, the host system is put back to sleep.

The five founding members of the Bluetooth initiative include Ericsson Mobile Phones and Terminals, Lund, Sweden; IBM Corp., White Plains, N.Y.; Intel Corp., Santa Clara, Calif.; Nokia, Espoo, Finland; and Toshiba Corp., Tokyo, Japan. Many other companies support the initiative, and hope to have products in either prototype or production form for the second half of 1999. These companies include 3Com, Axis, Cetecom, Compaq Computer, CTIA, Hewlett-Packard, Lucent Technologies, Motorola, Puma Technology, Qualcomm, Symbionics, TDK, VLSI Technology, and Xircom.

Designers estimate that the full transmit/receive module for the Bluetooth interface will occupy less than half a square inch of board real estate. At this size, it could easily be embedded in a system. Prototype transceiver modules already fabricated require only about one square inch, even without being area-optimized.

To make this technology a reality, Ericsson is contributing the basic radio technology expertise. Toshiba and IBM are developing the common specification for integrating Bluetooth into mobile devices. Knowledge of advanced chips and software is coming from Intel, while Nokia is contributing expertise in radio technology and mobile handset software. Other companies are invited to use the core technology on a royalty-free basis to ensure that Bluetooth technology is implemented.

Because the transceiver will operate on the globally available, 2.45-GHz ISM free band, international travellers will be able to use Bluetooth-enabled systems worldwide. Unlike the infrared port on today's laptops, the RF interface does not require a line-of-sight setup. It can function when computers or other devices are tucked away in briefcases, desk drawers, etc.

Bluetooth promises to do away with all the connectivity cables, o cradles, typically needed by a mobil system user. Flexibility will increas as users travel or move about mor freely, even in their own facilities. For example, users will be alerted to incoming e-mail, and may use their mobile phone to respond to it.

In such a scenario, the PC or PDA wakes up when an e-mail message arrives. It alerts the mobile phone, via which the user instructs the PC. The e-mail can be sent to the intelligent mobile phone. The user can either read the message, or have the computer convert the message to voice, and play it back over the phone.

Another possible scenario for users is to send instant "postcards"—voice or text messages that include an image file. That image file could be captured by either a corded or cordless camera, which is linked to the mobile phone.

For more information on Bluetooth check out the special interest group web site at www.bluetooth.com.

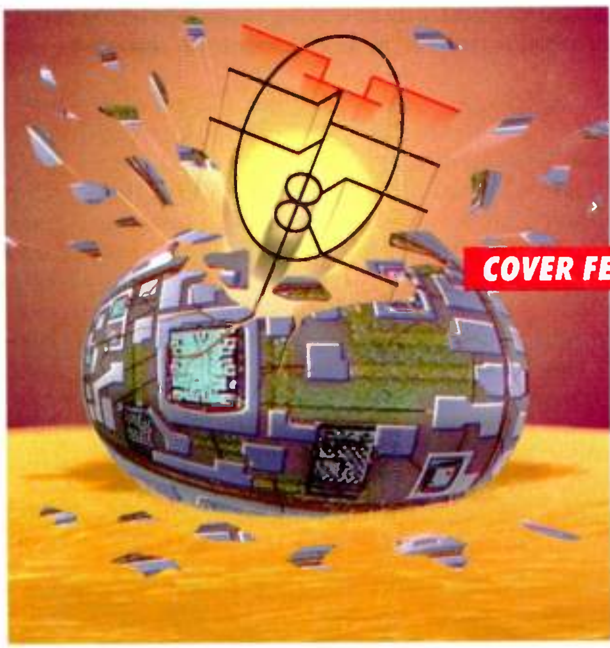
Dave Bursky

Unique Valve Independently Controls Power Parameters

Novel Circuit Topology Simultaneously Or Separately Controls The Amount Of Current, Maximum Voltage, And Effective Voltage.

Ashok Bindra

COVER FEATURE



The vacuum tube was the first electron valve to control power to a load. Its successor, the transistor, was smaller, generated less heat, and ran on lower voltages. The thyristor, or silicon-controlled rectifier, followed, addressing current-control requirements at higher power ranges, where conventional transistors bump into heat dissipation limits. But transistors and thyristors have significant limitations, especially in the areas of operating voltage range, efficiency, noise, power dissipation, and maintenance of maximum voltage while controlling the effective voltage of a power pulse wave. Above all, they can either control the output current or the voltage, but not both at the same time.

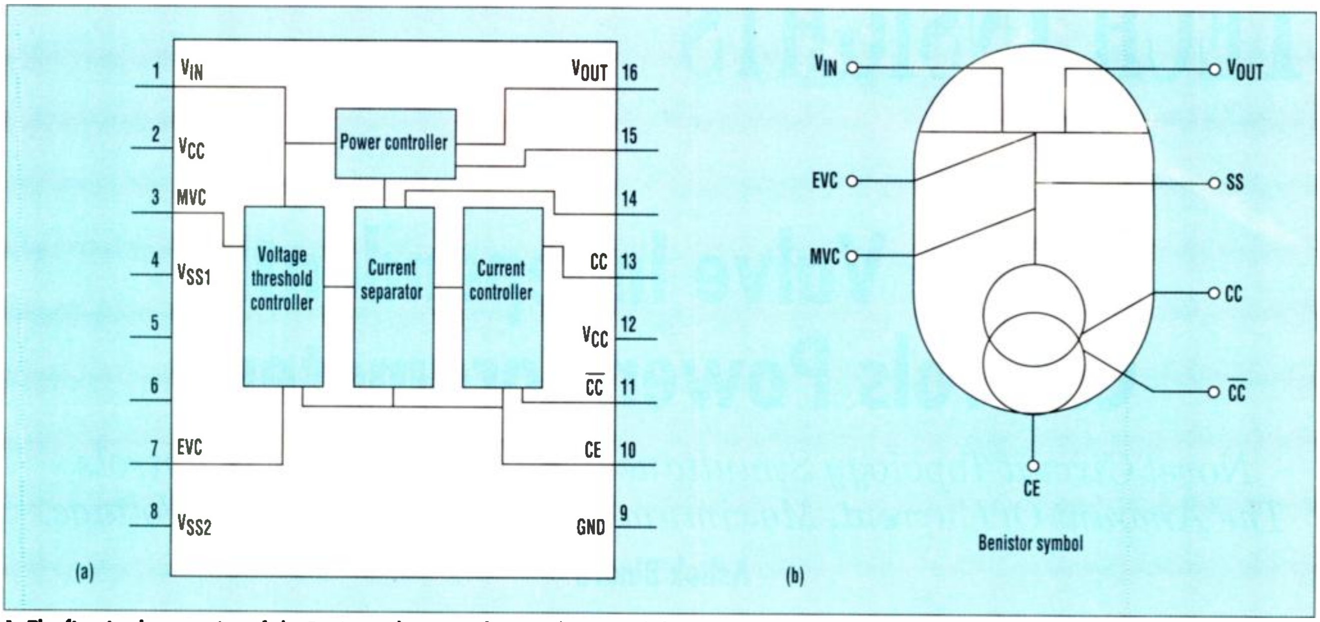
A novel, controllable electron valve overcomes all these shortcomings. The circuit, dubbed a Benistor, can control separately or simultaneously, the amount of current, the maximum voltage, and/or the effective voltage value coming in from a power source and sent out to a load. And, it does so in a linear, switching, or self-switching mode of operation. In fact, unlike the transistor or thyristor, the Benistor exercises complete control over an output waveform regardless of the input waveform.

The name Benistor is a combination of *b*lockade of *e*lectric *n*etwork and trans*istor*. According to its inventor, Benjamin Acatrinei, the Benistor is the fourth element in power control, after vacuum tubes, transistors, and thyristors. Acatrinei's company, Bensys Corp., Santa Clara, Calif., has contracted with foundry service provider Calogic Corp., Fremont, Calif., to produce the Benistor, which comprises four bipolar chips housed in a 16-pin DIP (*Fig. 1*).

The first result of this commercialization effort is the Ben 35100. This component features a maximum input voltage of 36 V, maximum supply current of 3 mA, maximum bias current of 500 nA, and a typical threshold voltage of 0.54 V. Typical turn-on time for the Benistor is 650 ns, with a typical fall time of 5.6 μs. The saturation voltage for the unit is only 65 mV. Rated for 0 to 70°C, the Ben 35100 is internally protected against reverse voltage or current. The output response of the device to voltage conditions at various electrodes is shown in Figure 2.

"The independent control afforded by the Ben 35100 will let designers create a wide variety of novel power-control circuits that are simpler and lower in cost than conventional power-control circuits," says Acatrinei. Potential applications include switching power supplies, light or heat controllers, battery chargers, and a multitude of other circuits now served by transistors and thyristors. In fact, adds Acatrinei, with its unique method of controlling the electric energy delivered to the load, the Benistor's potential is limited only by the imagination of the designer.

Although, the device's first implementation is in bipolar technology, Bensys also is exploring other process technologies to meet the specific needs of target markets and applications. Meanwhile, the company is in the process of converting the hybrid design into an IC. Benistors with a variety of supply and input voltage ratings are also in the works, with plans



1. The first implementation of the Benistor electron valve is a device with four bipolar chips (a). The device controls load current and voltage simultaneously or separately within a pre-established range set by the control electrodes shown in the device's schematic symbol (b).

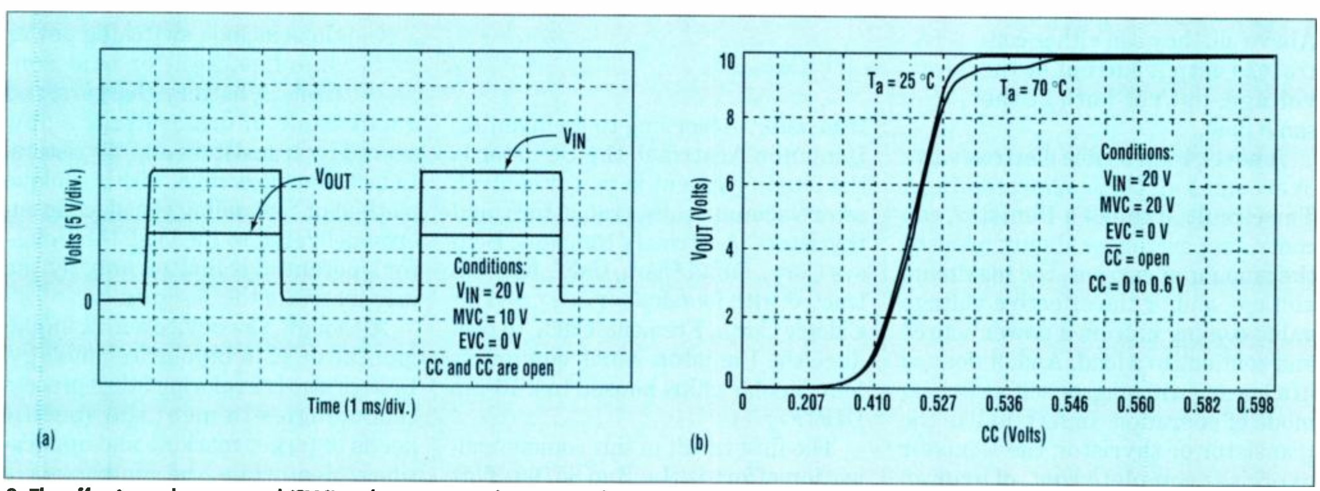
to extend the input voltage capability of the device to 400 V.

The four building blocks that make up the Benistor include a power controller, current separator (CS), current controller (CC), and voltage-threshold controller (VTC) *(see Fig. 1 again)*. The power controller is a simple pnp transistor that acts as a switch or a variable resistor between the power source and the load. The CS block incorporates three npn transistors to enable the voltage controller and current controller to work simultaneously or separately.

Comprising two open-collector op amps and two resistors, the current controller acts as a voltage/current converter for the power controller. There are two control inputs to this block: non-inverting input CC and the inverting input $\overline{CC}$. The amount of voltage input at the non-inverting current control is directly proportional to the current output to the load, and the amount of voltage at the inverting electrode is inversely proportional to the output current.

Functioning as a window comparator, the VTC controls the buffer's base current, in either switching or self-switching mode. The two controls of the VTC are effective voltage control (EVC) and maximum voltage control (MVC), which determine the threshold voltages of the output. While the voltage at EVC establishes the threshold for switching from off to on state, the voltage at MVC pin determines the on/off states. In effect, the voltage settings on these two pins pre-establishes the output voltage window.

In summary, the Benistor is a multi-electrode device consisting of impedance command pins for precise control of output current and voltage. Consequently, there are eight electrodes that completely define the



2. The effective voltage control (EVC) and maximum voltage control (MVC) pins determine the threshold voltages of the output, with the maximum output voltage set by the voltage at the MVC pin (a). Current controller pins CC and $\overline{CC}$ establish the output current, a small change in voltage at pin CC provides a linear control of the output current. V_{OUT} is the measured voltage drop across a 10 kΩ load resistance (b). Note that there is negligible change in the output response of the Benistor with changes in the operating temperature.

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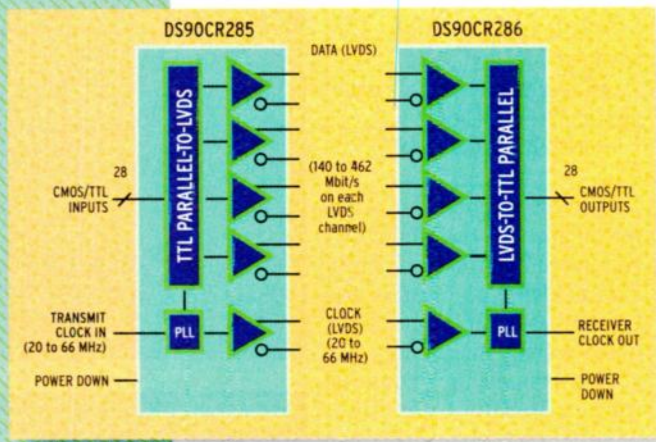

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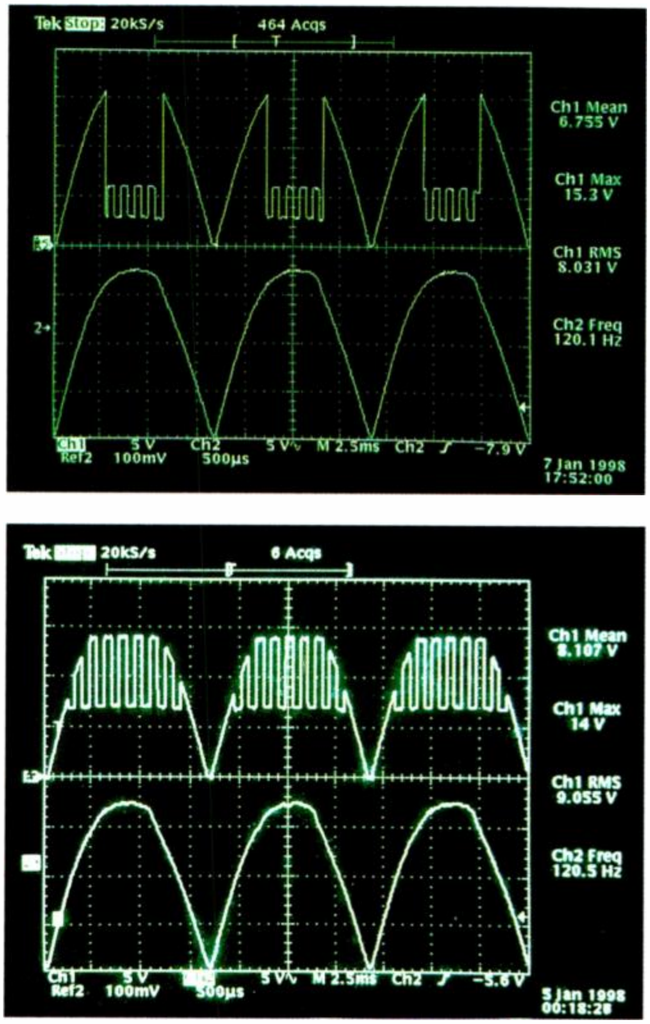
Benistor. These are:

- Voltage-in (V_{IN})
- Voltage out (V_{OUT})
- Common electrode (CE)
- Voltage control electrodes EVC and MVC
- Current-control electrodes CC and $\overline{CC}$
- Switching select (SS)

The SS electrode sets the initial state of the Benistor's self-switching mode of operation as either on or off at the beginning of an input power pulse wave. Having only two states, it is either grounded (on) or floating (off). Likewise, the CE provides the reference voltage for the device, while the CC determines the window of output current, and the VTC pre-establishes the window of output voltage. Based on these settings, the power controller will deliver to the load only that part of the input power signal, with respect to the amount of current and voltage, that is within the two pre-established ranges. In effect, together, the voltage and current-control electrodes can provide the system designer with virtually any output possibilities.



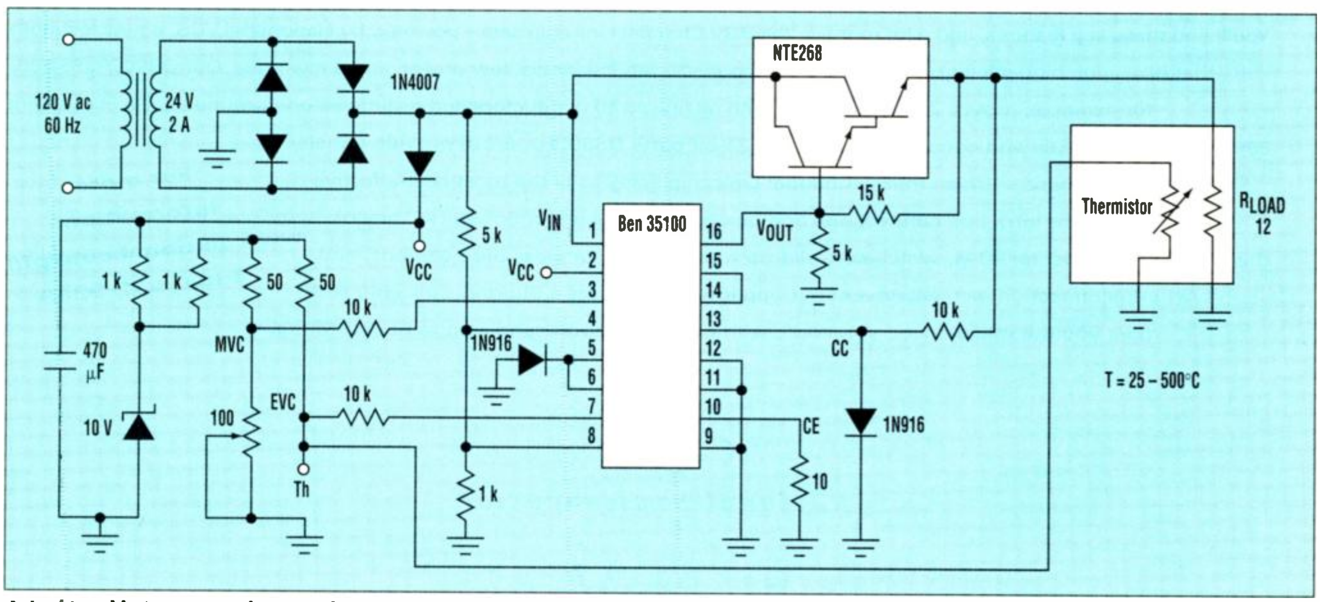
3. The Benistor provides complete control of the output waveform regardless of the input. For the same inputs (bottom traces in each photo), many types of clean complex outputs can be created (top traces).

Because the device can accept ac, dc, and pulse inputs, and provide outputs in any of these modes or combination thereof (based on conditions at the control electrodes), the Benistor inspires a new way of thinking in power control and power conversion. Combining the capabilities of all three previous valves, it provides designers a unique method of controlling power parameters(*Fig. 3*).

Unlimited Applications

Although, at its introduction, the Benistor is targeted at some specific markets like switching power supplies, battery chargers, and fluorescent light ballasts, the novel device is being positioned as a fundamentally new power controller with unlimited applications.

To enable engineers to understand the capabilities of the unusual Benistor, the company has developed application notes for switching-power-supply designs and battery chargers. According to Bensys, the Benistor's unique operating ac and dc-characteristics can contribute to improving the classic design of a battery charger in



4. In this soldering iron application, the Benistor replaces the traditional thyristor to enable a 10 W transistor to precisely control a 50 W load. The system cost is cut by half and energy savings are significant. Plus, it precisely controls load current to achieve 0.5 °C temperature control.

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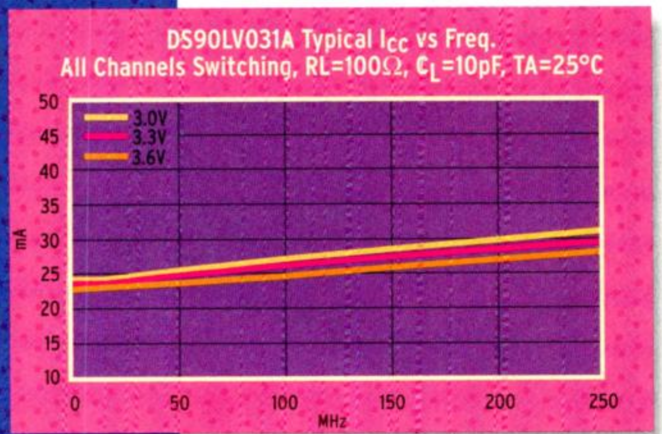

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terms of system cost, reliability, size, and efficiency.

Its feedback mechanism prevents voltage and current overload, thereby allowing a safer charging process. And, its ability to change the frequency of the charging pulses as required further optimizes the charging speed. In addition, it allows the same design to be adapted to any battery chemistry with regard to voltage and current. Likewise, the valve's onboard amplifiers and comparators, coupled with its ability to alter V_{OUT}, eliminates the need for such components in traditional switching power supplies, while simplifying the design and enhancing the efficiency of the power supply design.

Bensys also has demonstrated the capabilities of the new controller by comparing traditional approaches against those using the Benistor. For example, in a voltage regulator circuit, with a 5.0-V regulated output at 100 mA and a 24-V ac input from a transformer, the Benistor implementation achieves a significant improvement in the overall efficiency of the circuit, according to Bensys. The lower dissipation in the Benistor eliminates the need for the heat sink, making it easier for the voltage regulator to maintain output accuracy, states Bensys.

And, when deployed in a 50-W soldering iron to control the temperature at the tip of the iron, the Benistor design accomplished substantial savings in power, while lowering the cost of the system by half, claims Bensys. Unlike traditional thyristor control circuits used in soldering irons, the Benistor design uses only a 10-W transistor to control a 50-W load (*Fig. 4*). Because the Benistor scheme synchronizes the output pulse with respect to the input, it reduces waste, and improves efficiency of the control circuit. Plus, it simplifies the system design by minimizing external components, and provides 0.5 °C control of the temperature at the tip.

PRICE AND AVAILABILITY

Samples of the Ben 35100 in 16-pin DIP packages are available now, with production scheduled for the fourth quarter. In 10,000 piece lots, the Benistor costs $2.75 each. An evaluation board is available for $97.

Bensys Corp., 3140 De La Cruz Blvd., Suite 200, Santa Clara, CA 95054-2046; (888) 423-6797; fax: (408) 919-4628; www.bensyscorp.com. **CIRCLE 497**

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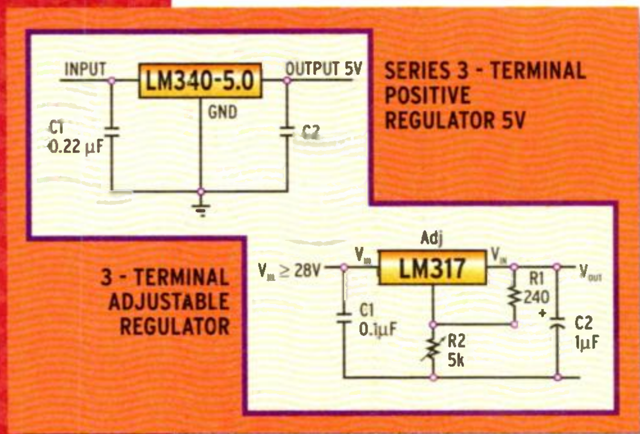

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DESIGN APPLICATION

Tuned Decoupling Tames Noise In Switching Circuits

Suppress Specific Frequencies By Resonating The Inductance In Circuit-Board Traces And Component Leads.

JOHN-CYRIL HANISKO, Eaton Corp., Innovation Center, 26201 Northwestern Highway, P.O. Box 766, Southfield, MI 48037; (248) 354-2910; fax (248) 208-2018.

As printed-circuit boards become more densely populated, the opportunities for "intra-module" interference grows. Similarly, the probability of "inter-module" interference increases. The move to higher switching rates, higher spectral content, and higher power exacerbates these trends. At the same time, engineers struggle with more stringent emissions regulations. Together, these considerations elevate the need to effectively decouple switching circuits.

To achieve effective decoupling, the decoupling source—invariably a good-quality capacitor located close to the switching circuit—must provide the ac content of the switched current. Meanwhile, the main power source—usually located away from the target—must provide the average current and, hence, all of the energy. This confines the high-frequency currents to a small loop in the vicinity of the target, thus minimizing board emissions. In addition, high-frequency currents are kept off the power and ground buses, which minimizes inductively coupled interference. Furthermore, because the ripple voltage across the decoupler (i_1Z_1) appears on the power bus, minimizing this voltage will reduce capacitively coupled interference *(Fig. 1)*.

A number of recent papers have considered the effect of both the pc board's bus structure[1,2] and the characteristics of the decoupling capacitors themselves[3] on suppressing emissions. Here, we mainly investigate the benefits and caveats of using decoupling networks, which suppress specific frequencies. Engineers are often challenged to suppress one or more clock frequencies and, perhaps, related harmonics or subharmonics. In most cases, general decoupler choices do not efficiently address the highly defined suppression targets.

Consider the lumped-parameter model shown in Figure 1. Here, the target (switching) circuit is modeled as an ac current source. V_y (f, t) is the ac voltage developed at point y on the power bus, due to the interaction of switching currents and system impedances; i_0 (f, t) is the ac current drawn by the target circuit; i_1 (f, t) is that part of i_0 supplied by the decoupler, and i_S (f, t) is the part of i_0 that flows on the power bus. Z is the total impedance of the power bus; Z(y) is the power bus impedance between the decoupler and point y; Z_1 is the impedance of the decoupler; and Z_0 is the impedance between the decoupler and the target. For convenience, we have incorporated the internal impedance of the main power source into Z. The equations are:

$$i_S = \frac{Z_1}{Z_1 + Z} \times i_0 \quad (1)$$

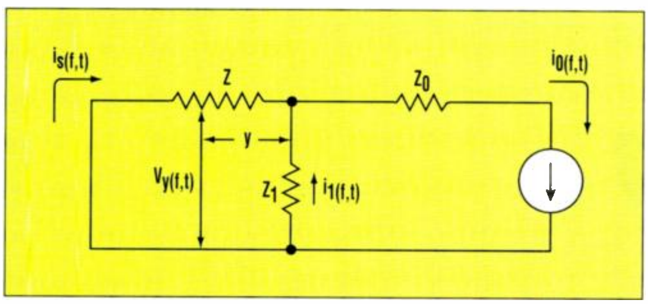
$$V_y = i_S Z(y) - i_1 Z_1 \quad (2)$$

Notice that both i_S and V_y have zeroes at $Z_1 = 0$ and have poles at $Z_1 + Z = 0$.

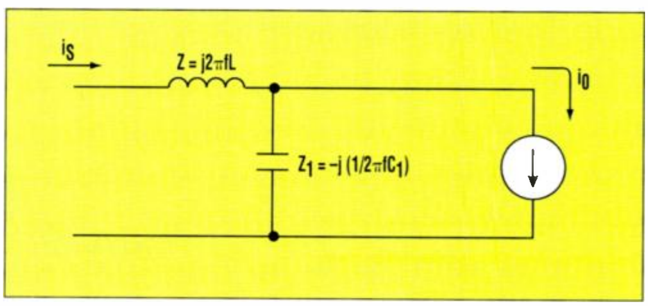
Now, let's consider some familiar decoupler configurations: 1) single-branch, pure (ideal) capacitance; 2) single-branch, capacitance plus inductance; and 3) dual-branch, capacitance plus inductance.

Pure Capacitance

In the good old days, before the advent of modern switching frequencies, it was reasonable to assume pure capacitance for a decoupler. Switching rates were low enough that trace, lead, and connection inductances could usually be ignored. In this case, the model of Figure 2 guides the analysis. From now on, we shall ignore the effect of Z_0, since doing so does not affect the generality of



1. The lumped-parameter model shows the target (switching) circuit as an ac-current source. For convenience, the internal impedance of the main power source is incorporated into Z.



2. A single-branch, pure capacitance circuit model was useful before the advent of modern switching frequencies. Switching rates were low enough for trace, lead, and connection inductances to be ignored.

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our analyses. The equations for this configuration are:

$$\frac{i_S}{i_0} = \frac{1}{1 - \frac{f^2}{f_\infty^2}} \qquad (3)$$

where

$$f_\infty = \frac{1}{2\pi\sqrt{LC_1}} \qquad (4)$$

The frequency response of the relative amplitude, i_S/i_0, has a pole at $f = f_\infty$.

The main consideration in such a situation is the selection of C^1. This value should be such that the amplitude, $|i_S/i_0|$, is well rolled-off in the frequency range of interest, and f_∞ is far from this region.

Inductance and Capacitance

Most switching rates are now high enough that pure capacitance has become an untenable assumption for the decoupler. The analysis is better guided by the model of Figure 3. The equations for this configuration are:

$$\frac{i_S}{i_0} = \frac{1 - \frac{f_1^2}{f^2}}{1 + \frac{L}{L_1} - \frac{f_1^2}{f^2}} \qquad (5)$$

where

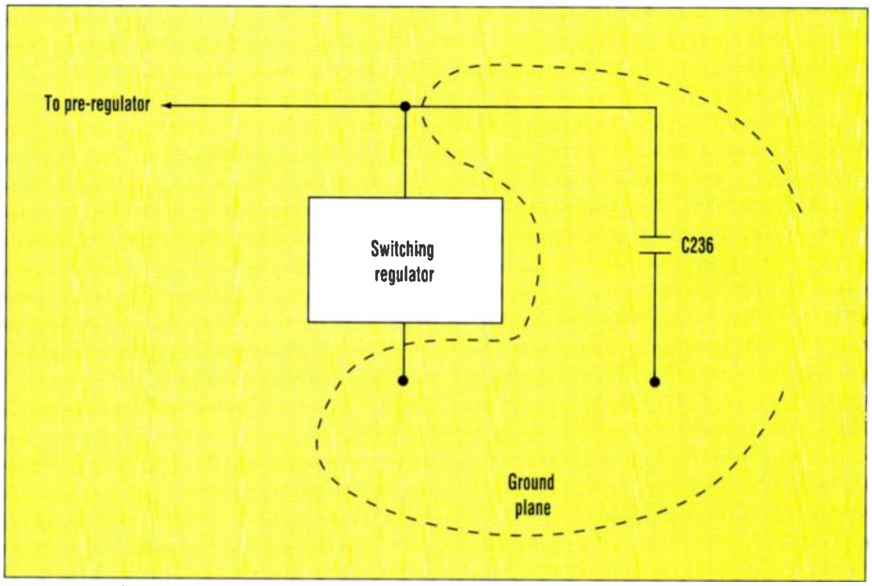
$$f_1 = \frac{1}{2\pi\sqrt{L_1C_1}} \qquad (6)$$

is a zero of the response, and

$$f_\infty = \frac{f_1}{\sqrt{1 + \frac{L}{L_1}}} < f_1 \qquad (7)$$

is a pole.

The existence of a zero at $f = f_1$ immediately suggests a method of optimally decoupling a specific frequency. That is, choose a decoupling capacitor that just happens to have its impedance anti-resonant at the target frequency. Then, connect this component into a negligible-inductance decoupler branch. At the target frequency, all of the current is provided by the decoupler. None of this current flows in the power bus (or ground bus).



5. In an initial attempt at decoupling, the sample board already had a high-quality dielectric, 1-µF ceramic surface-mount capacitor "downstream" of the switching regulator, at a site designated as C236. This capacitor was connected to the power-input pin of the regulator by a two-section, series-connected trace.

Between the target frequency and the anti-resonant frequencies of the available decoupling capacitors, a sufficiently close match cannot always be found. In this situation, a tuned decoupling can still be achieved by choosing a capacitor with an anti-resonant frequency, f_{ar}, such that $f_{ar} > f_1$, where f_1 now designates the target frequency. Let C_1 be, once again, the capacitance of the decoupling component. Then

$$l_1 = \frac{1}{f_{ar}^2 4\pi^2 C_1} \qquad (8)$$

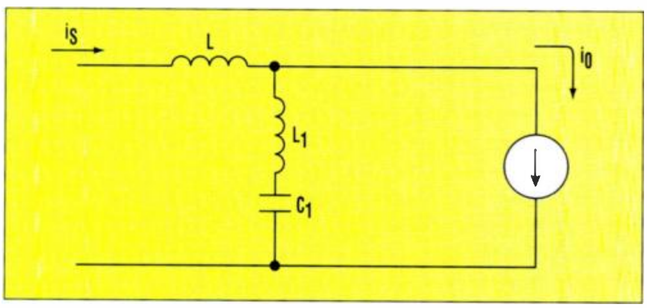
where l_1 is the intrinsic inductance of the component. Consequently, if external inductance is added to the decoupling circuit, as in

$$\Delta l_1 = \frac{1}{4\pi^2 C_1}\left(\frac{1}{f_1^2} - \frac{1}{f_{ar}^2}\right) \qquad (9)$$

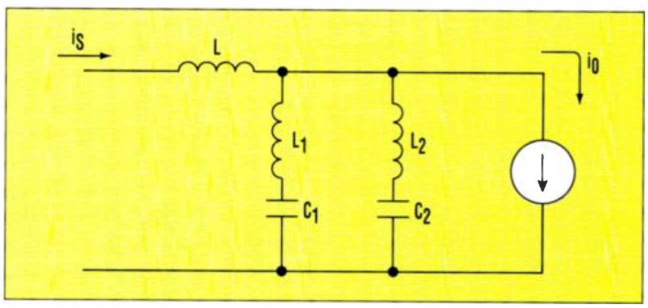
a branch is constructed that maximally decouples the target frequency.

The additional inductance may be inserted in the form of a discrete component. Or, it may be obtained in the form of a pc-board trace of appropriate geometry. For an example of the calculation of trace inductances, see the Rostek article.[4]

In some situations, it may be worth considering multiple decoupling



3. Most switching rates are now high enough that pure capacitance has become an untenable assumption for the decoupler. A single-branch, inductive, and capacitance circuit is a more suitable model.



4. In some situations, a dual-branch decoupler is worth considering. One situation is to achieve a lower response at the anti-resonant frequency, while another is a need to simultaneously suppress several frequencies.

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AD7417	4	I^2C	±1	0.2 mW @ 1 kSPS	2.95	SOIC, TSSOP	16
AD7817	4	SPI	±1	3.0 μW @ 10 SPS	2.95	SOIC, TSSOP	16
AD7418	1	I^2C	±2	0.2 mW @ 1 kSPS	2.25	SOIC, μSOIC	8
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branches. For example, tuned circuits have residual, if minor, resistance at the anti-resonant frequency. In order to achieve an even lower response at this frequency, identically tuned decoupling branches are sometimes placed in parallel in the circuit.

A second example of an application for multiple decoupling branches is provided by the need to suppress several frequencies simultaneously. In this case, several decoupling branches, each one tuned to a different target frequency, might be used. Though the following analysis is for dual decoupling branches *(Fig. 4)*, the extension to more than two branches can be made relatively easily.

Consider a dual branch decoupler in which the each of the branches is tuned to different frequencies, f_1 and f_2. The equation is:

$$\frac{i_S}{i_0} = \frac{\frac{L_1L_2}{L(L_1+L_2)}\left(1-\frac{f_1^2}{f^2}\right)\left(1-\frac{f_2^2}{f^2}\right)}{1-\frac{f_S^2}{f^2}+\frac{L_1L_2}{L(L_1+L_2)}\left(1-\frac{f_1^2}{f^2}\right)\left(1-\frac{f_2^2}{f^2}\right)} \quad (10)$$

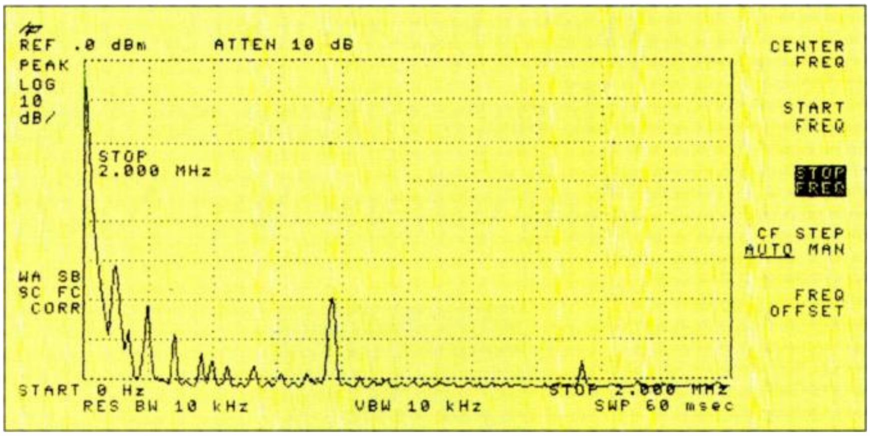
where

$$f_S = \frac{1}{2\pi}\left[\frac{(L_1+L_2)C_1C_2}{C_1+C_2}\right]^{-\frac{1}{2}} \quad (11)$$

and

$$f_1 < f_S < f_2 \quad (12)$$

for $f_2 > f_1$.



7. For this case, a surface-mount capacitor was used at the C236 site, and a radial capacitor was connected directly to the power input and ground pins of the regulator. This resulted in zeros at 698 kHz and 1.17 MHz, unity at 847 kHz, and poles at 531 kHz and 916 kHz.

For the real-life application of these techniques, consider the reduction of radiated emissions from the I/O harness of a pre-production electronic module. Shielding the harness was not an option. Furthermore, since the design was all but "frozen," extensive rework of the pc board was out of the question. Appreciable reduction of radiated emissions, with minimal intervention, was required.

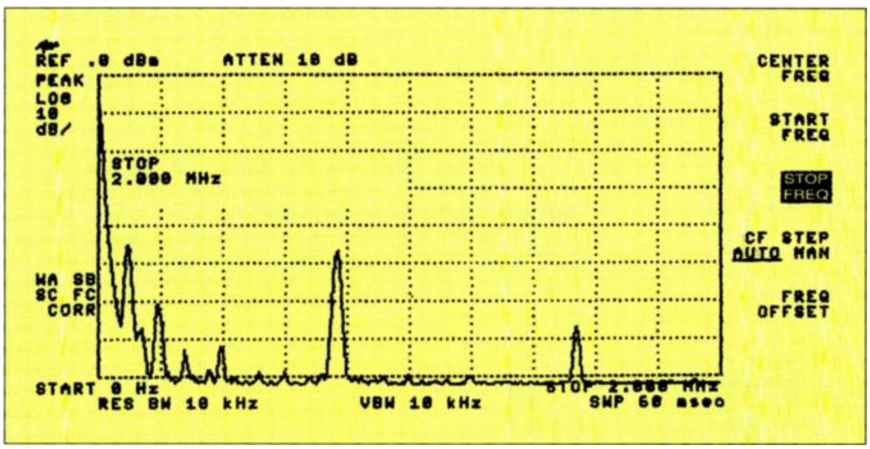
Regulator Noise

The offending frequencies were the 750-kHz fundamental and 1.5-MHz second harmonic, produced by a commercially available switching regulator. The power-input pin of the regulator was connected to the filtered output of a preregulator by 1.5 in. of a 100-mil wide, 2-mil thick isolated trace. Using Rostek's formula[4], the inductance of this trace calculates to be 29.4 nH. The regulator was returned directly to a very low-impedance ground plane.

In an initial attempt at decoupling, the board already had a high-quality dielectric, 1-µF ceramic surface-mount capacitor "downstream" of the regulator at a site designated C236 *(Fig. 5)*. The capacitor at this site was connected to the power-input pin of the regulator by a two-section, series-connected trace. One section of the trace measured 0.94 in. long, 100 mils wide, and 2 mils thick. The other section measured 0.150 in. by 100 mils by 2 mils. The capacitor was returned to the ground plane by a 0.32-in. by 50-mil by 2-mil trace. All of these traces were located at a height of 20 mils over the ground plane. The inductance of the complete trace calculates to be 17.6 nH.

A 1-µF capacitor of this type has a minimum impedance. which is a zero, at about 5 MHz. This yields an intrinsic inductance (equation 6) of about 1 nH. Thus, the zero of the decoupling loop, for a 1-µF capacitor at C236, calculates to 1.17 MHz, with a pole (equation 7) at 728 kHz.

Preliminary benchtop tests were conducted using an H-field "wand" and a spectrum analyzer. The tests measured the relative strengths of the frequencies radiating from the harness. Baseline measurements were made with no decoupling *(Fig. 6)*. For the second case, measurements were made with the 1-µF surface-mount capacitor at the C236 site. The decoupling significantly reduced the second harmonic, as expected, but had little effect on the fundamental. This latter result is due in part to the pole at 728 kHz being lo-



6. Preliminary benchtop tests were conducted, using an H-field "wand" and a spectrum analyzer, to measure the relative strengths of the frequencies radiating from the I/O harness of a pre-production electronic module. Baseline measurements were made with no decoupling.

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The surface- mount capacitor was replaced by a 1- µF radial capacitor for the third case. This was tuned to have a zero at 700 kHz, obtained by providing about 52 nH of lead inductance. With this capacitor, the decoupling loop has a zero at 600 kHz and a pole at 500 kHz, yielding significant reduction at the fundamental frequency, and some reduction at the second harmonic.

Capacitor Returned

For the fourth case *(Fig. 7)*, the surface mount capacitor was returned to the C236 site, and the radial capacitor was connected directly on the power input and ground pins of the regulator. This resulted in zeros at 698 kHz and 1.17 MHz, unity at 847 kHz (equation 11), and poles at 531 kHz and 916 kHz. The reduction at the fundamental is not as great as in the third case, probably because of the proximity of the unity to the higher-frequency pole. However, the reduction at the second harmonic is as substantial as that obtained in the third case, in spite of the 916-kHz pole.

Subsequent radiated emissions measurements—in an anechoic chamber—supported the "wand" results. A variation of the fourth case was used for the production module.

The use of tuned decouplers can be very helpful, particularly in those situations in which the main contributors to interference are sharply defined, well-separated frequencies. As shown, however, the technique introduces poles as well as zeros, and should be applied with these considerations in mind. For maximum effectiveness, the poles should be located in the frequency-range regions in which there is no interference structure. They should also be located at a sufficient distance from the zeros, so that the presence of the poles does not degrade the decoupling effect.

John-Cyril Hanisko works in analog circuit design and sensor development at the Eaton Corp.'s Innovation Center in Southfield, Mich. He holds a MSEE from the University of Detroit, Detroit, Mich., and a PhD in physics from Wayne State University, Detroit.

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4. Rostek, P. M., "Avoid Wiring-Inductance Problems," *Electronic Design*, Dec. 6, 1974, pp. 62-65.

PRODUCT INNOVATION

Complete GPS Receiver Fits On Two Chips

A Pair Of Complementary ICs, An RF Front End And A Microcontroller, Allow Total GPS Receiver Implementation.

Alfred Vollmer

Until now, global-positioning-satellite (GPS) systems always had a little glamour about them, tending toward something that's extraordinary, expensive, and unusual. However, this scenario might change quite soon because STMicroelectronics NV (ST) (formerly SGS-Thomson Microelectronics), Saint Genis, France, is introducing a pair of complementary ICs—the STB5600 RF front end and the ST20GP6 microcontroller—that allows a complete GPS system to be implemented *(Fig. 1)*. "These two chips provide the industry's most compact solution for the rapidly emerging GPS market," claims Dr. Philip Mattos, consultant engineer at ST.

In addition to integrating all the analog and digital functions required, the chip set also provides enough spare processing power to allow user application functions to be implemented without the need for an external CPU. ST plans to offer the chip set for the U.S. market at a low enough price to allow its entry into new markets such as entertainment electronics and mobile communications.

In the U.S., cellular mobile telephones, for example, will soon be required to send information about their current position to the base station. In terms of licensing, the two-chip set will make it a lot easier to securely identify the physical point of operation. This is due to the fact that licenses to use a specific product in a specific country or even state can be exactly obeyed by using a GPS receiver and an electronic map. The map contains information about the borders between countries (or states), along with an electronic circuit blocking the entire system if it is used outside a licensed area.

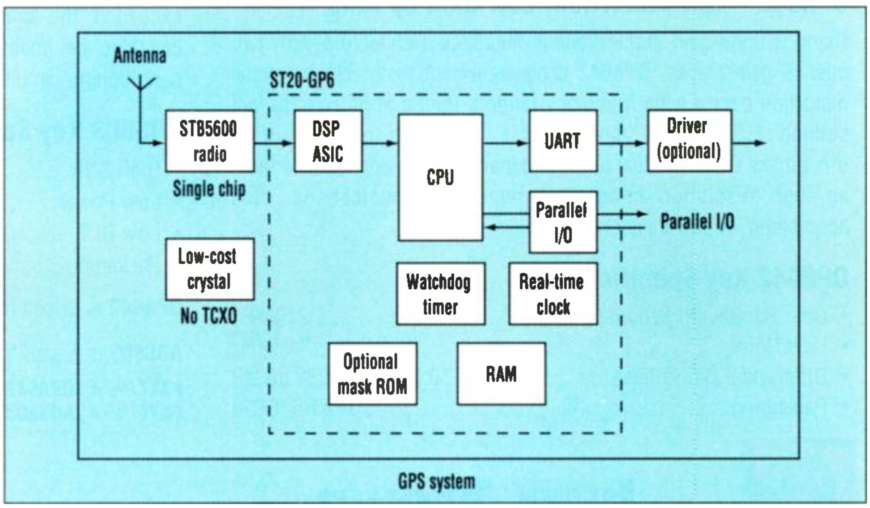
The ST20GP6 contains all the ROM and RAM required to build a complete GPS system on one side of a 50- by 40-mm board, even if an RS232 driver is required *(Fig. 2)*. For lower-volume applications, where a masked ROM is not suitable, a single external flash ROM chip is added. As Mattos points out, the entire chip set requires less than 20 external components, most of which are power-decoupling devices. "There is no need for a temperature-controlled crystal oscillator (TCXO) because a simple crystal is sufficient to work with this solution," he says.

Down Conversion

The RF front-end STB5600 provides down conversion from the GPS (L1) signal at 1575 MHz via a 20-MHz IF of 20 MHz to an output frequency of 4 MHz suitable for the ST20GP6 GPS controller. It uses an external single-transistor reference oscillator to generate both the RF local-oscillator signal and the processor reference clock. The second mixer, second local oscillator, and second-stage filtering are performed digitally, the first two in the STB5600 and the last in the DSP hardware of the ST20GP6.

The signal from the active antenna is passed through a ceramic RF filter to reject image noise, and then through a matching network into the STB5600 *(Fig. 3)*. The matching network, which consists of just two capacitors and a printed-track inductance, both converts from 50 to 300 Ω impedance, as well as from single-ended to differential drive.

The reference oscillator runs at 82 MHz. This signal is available at the emitter, and high-order harmonics (18, 19, and 20×) can be obtained at the collector. An identical ceramic RF filter selects the 19th harmonic and feeds it to the STB5600's first local-oscillator port. A capacitive tap on the emitter tank circuit takes a very low-amplitude feed at 82 MHz to the STB5600 divider input, where it is divided by five to create the 16-MHz second local oscillator and the output clock for the



1. This total GPS receiver system can now be implemented using just two chips from ST: the STB5600 RF front end, and the ST20-GP6 microcontroller. No temperature-controlled crystal oscillator (TCXO) is required.

ST20GP6. Both the 1554.96- and the 81.84-MHz signals are on the pc-board tracks at very-low levels of less than -40 dBm, to minimize RF leakage and EMC problems.

The first STB5600 mixer outputs a 20-MHz differential signal to an external LC filter for the IF, allowing the user to select the required bandwidth for the application. Then, the filtered signal is fed back into the high-gain limiting amplifier, and latched using the 16-MHz divider output.

Clocking the 20-MHz signal at 16 MHz creates a sub-sampled alias at 4 MHz—the frequency required by the ST20GP6, resulting in the 20-MHz IF filter aliasing as a 4-MHz filter. The skirts drop away at a rate consistent with the required 20-MHz bandwidth. As a result, neither a complex filter nor an analog 4-MHz filter are required. Clock and data outputs are then fed to the ST20GP6 at CMOS/TTL levels, via on-chip output buffers.

The DSP section of the ST20GP6 is drawn directly from that used on the ST20GPI, which is already found in automotive applications in Japan. The 4.092-MHz CMOS/TTL input signal coming from the STB5600 RF IC is latched by the 16.368-MHz clock from the same source. All operations beyond this point are performed digitally. The 16-MHz clock is divided to generate phase and quadrature versions (I and Q) of the 4.092-MHz clock. It also provides the master timebase for the system. These I and Q signals (4 MHz) are multiplied with the incoming data to generate signals with frequencies which are nominally zero. Nevertheless they still have the original bandwidth (about 2 MHz) of the spread-spectrum GPS signal. Due to its three components of reference oscillator error, satellite Doppler shift, and user Doppler shift, this signal is not centered.

Stop The Spreading

The next step is the distribution of the I/Q data to each of the twelve parallel-processing channels where the first task is to de-spread the signal. This is performed by multiplying it with a copy of the same spreading code used in the satellite. It is important that this multiplication takes place synchronously with the code on the signal.

Accumulating this signal for about 4 ms results in low-pass filtering, yielding to a low-bandwidth signal of around 50 Hz, which is created by the communications data from the satellite. A narrower filter is not feasible at this stage due to the potential frequency errors that are not yet compensated.

A second conversion removes the frequency errors by multiplying the I/Q data channels by the i/q signals generated by a numerically controlled oscillator. This down-conversion is performed in an image-rejecting mixer.

Mathematically, the operation is as follows:

$$I(out) = I \times I - (Q \times q)$$
$$Q(out) = I \times q + (Q \times I)$$

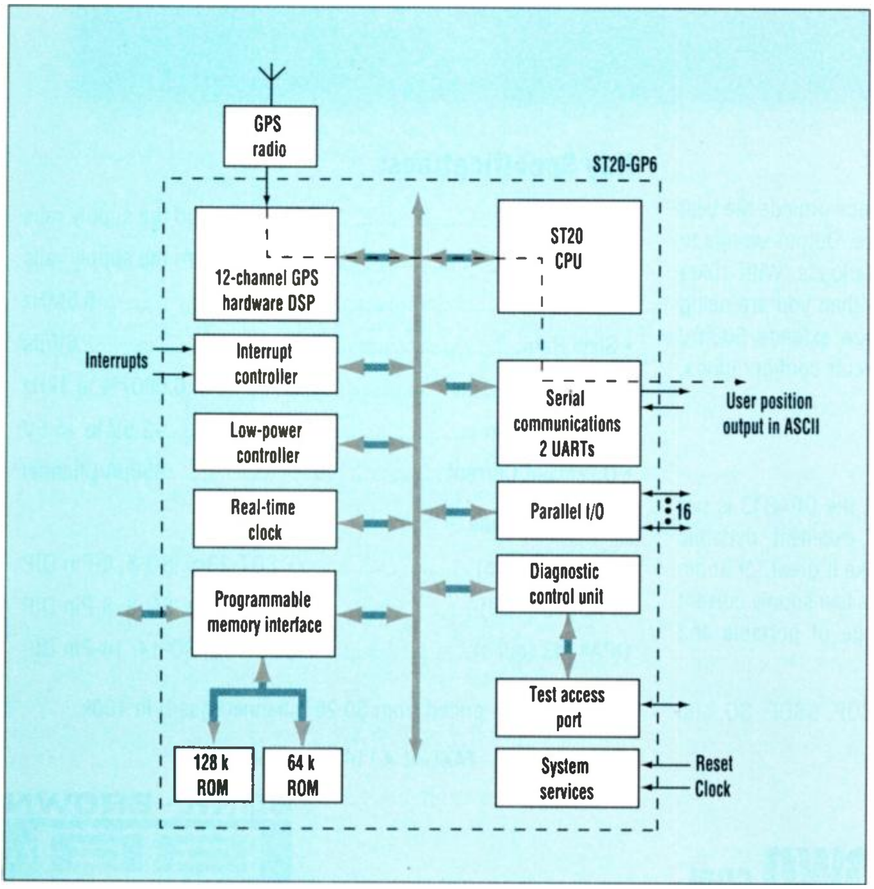
Controlled by software, the numerically controlled oscillator is set in a way that the i/q signals are at exactly the same frequency and phase as the I/Q satellite signals. As a result, the final frequency output is zero with a constant phase.

The remaining phase shifts contain the modulation information of the satellite-carrying communication data. This output signal is then passed through a low-pass filter to generate the final output to be used by the software.

Delivery to the software is performed in two steps: First, each of the 12 channels is retimed to the common 1-ms clock of the DSP hardware. Then, it is double-buffered to allow a DMA transfer to the CPU memory. In doing so, it uses idle bus cycles, and therefore, does not influence CPU throughput.

It is important to note that the measurables of the system which are used to calculate the user position are not output signals of the DSP; they're input signals. The only output is the signal amplitude and its phase error. Using this output data, the software calculates whether or not its internal high-resolution estimates of the measurables are correct. After suitable adjustment, the software closes the control loop by feeding back new, truncated, low-resolution versions of the settings to the hardware.

According to Mattos, this approach allows for much higher precision in terms of calculations (64 bits), while the



2. All the RAM and ROM needed to build a complete GPS system is included in ST's ST20-GP6 microcontroller chip.

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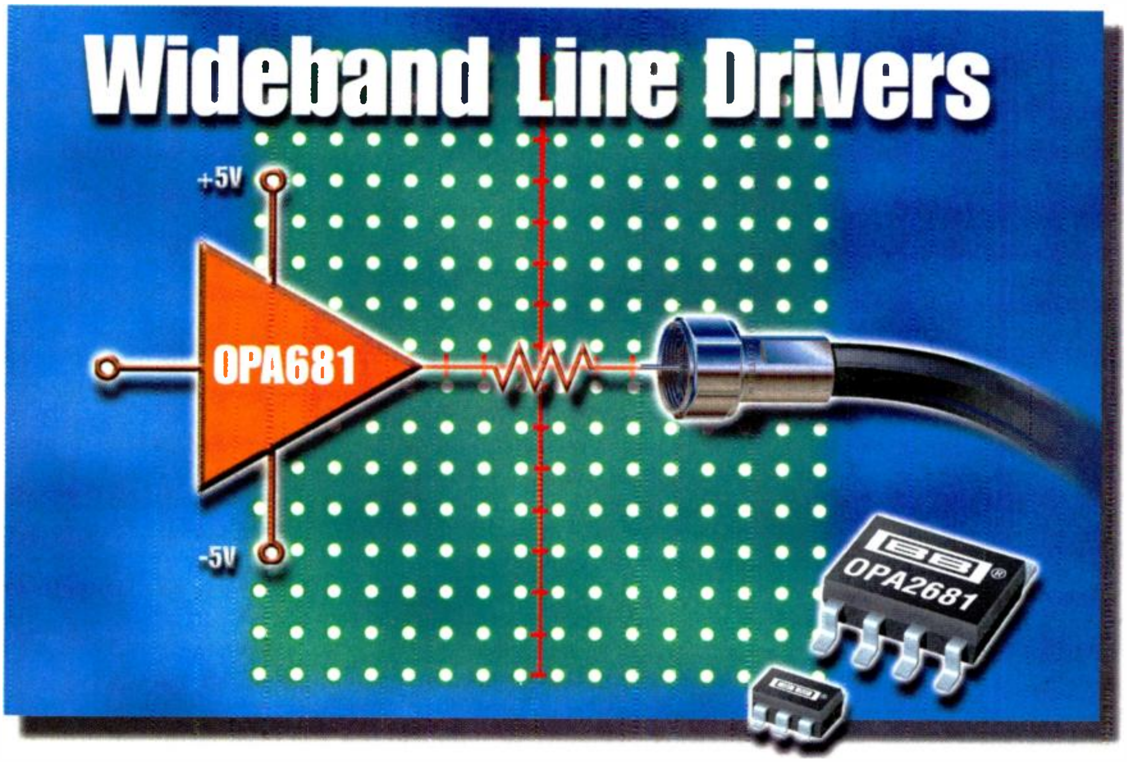

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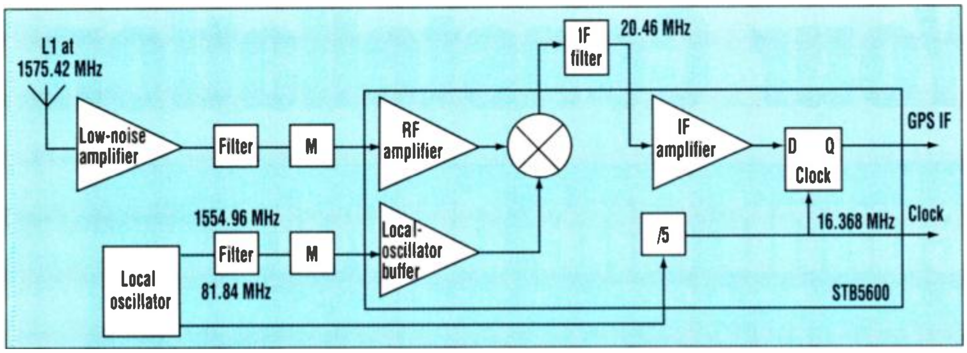

3. The first mixer of the STB5600 uses an external LC filter to set the desired IF bandwidth.

hardware is designed economically by supporting only the number of bits required at each stage. For example, the hardware measures the signal delay from the satellite in intervals of 122 ns, which is one-eighth of a code-chip coded in a 13-bit field, while the software uses an interval of about 200 ps. While the hardware is adjusted after a minimum frequency change of 1 Hz, the software deals not in frequency changes, but much more precisely in phase changes in steps of around 3°. The signal path starts at one bit (GPS IF pin), and grows to 6 bits after first accumulation to 16 bits, before it's delivered to the software.

The ST20GP6 uses a CPU of the ST20 type, which is manufactured on a 0.35-µm process. In most cases, the CPU runs with a clock speed of 33 MHz. However, in power-critical implementations, it also can operate at 16 MHz, due to the on-chip memory (RAM and ROM). On the other hand, it is possible to run the CPU faster (e. g. at 50 MHz), if other applications are also loaded to operate in parallel with the GPS software. At 33 MHz, the CPU achieves performance of about 25 MIPS.

SRAM

On the chip, there are 64 kbytes of SRAM which can be accessed every instruction cycle (e. g. every 20 ns at 50 MHz), at its full 32-bit width. The lower 16 kbytes can also be powered by using a second power pin to allow battery backup of data. There are an additional 128 kbytes of mask ROM integrated on the ST20GP6 chip, which allow on-chip integration of the GPS application programs, as well as additional customer applications. While the mask ROM is used for cost-critical applications (e. g. automotive), lower-volume applications or development versions can use an external flash memory because the ST20GP1 offers a full external memory interface.

To avoid bus-bandwidth bottlenecks which might occur due to longer access times of the mask ROM, ST implemented an instruction pipeline. The RISC instruction set offers variable coding length. Each instruction requires an average of one 32-bit data access. However, a single access to fetch code automatically loads about three instructions because the average instruction length is 10 bits.

ST estimates that production runs of more than 50,000 units with the same software are more economical if a monolithically integrated mask ROM is used. Smaller volumes should use external program memory devices.

Peripheral Functions

The ST20GP6 integrates all the functions required to set up a GPS module: a watchdog timer, RS232 serial ports (DUARTs), a real-time clock, a wake-up alarm, parallel I/O, an interrupt controller, and a diagnostic controller. A GPS used in an automotive application may require an analog-to-digital converter (ADC) and a vehicle bus interface. In this case, an external ADC is used, and serially interfaced via the parallel I/O pins.

The watchdog offers a single time-out period of 2 s, and the software is reduced to just turning it on initially, and then resetting it periodically within the 2-s time frame. If the watchdog initiates a system reset, a register indicates that the reset was initiated. The register's content may be used for statistical purposes in order to report the need for maintenance.

The real-time clock is compatible with the GPS satellite time-encoding format, which means that it works with weeks and seconds instead of simple ticks. The hardware is managed via a library so that the clock provides date and time information in the conventional format: hours, minutes, and seconds, and the day, month, and year.

An interesting peripheral function is the wake-up alarm, which is a function of the low-power controller on the chip. It allows the software to choose the parts of the chip to be powered down or forced to stay in either a sleep or a hibernation mode. An external pin indicates the sleep mode, to allow switching off of external chips. In the GPS application, this feature is used for solar-powered systems like those for container tracking or marine buoys. Other applications include those where power consumption is important, such as radio transmitters in weather balloons, vehicle security systems, or mobile telephones. This pin is connected to the RF portion to power it down as well.

Even the external clock may be disabled this way because the wake-up alarm is controlled by a 32-kHz watch crystal. After the programmed time has elapsed, the status pin is transferred to the low state, the radio powers up, and the clock starts working. Once the on-chip PLL has locked, the execution of instructions starts again. A wake up may also occur prior to the programmed time if an external event such as an interrupt happens—an interesting feature for vehicle security applications, where a position check may be made every 15 minutes, but if a door is opened, an immediate power-up may occur.

Parallel I/O is provided by two general-purpose, 8-bit ports, where any pin may be programmed to be either input or output. Furthermore, any pin can be programmed to interrupt the CPU if it changes its state, so that no polling of the input pins is required. It is possible to drive LEDs directly from the parallel pins, and to implement an entire keyboard as well as an LCD module interface by using the 16 pins.

The interrupt controller evaluates the priority of incoming events, and forwards the most important one to the CPU. For in-circuit emulation (ICE) during the design phase, the diagnostic controller is used. It allows for on-chip

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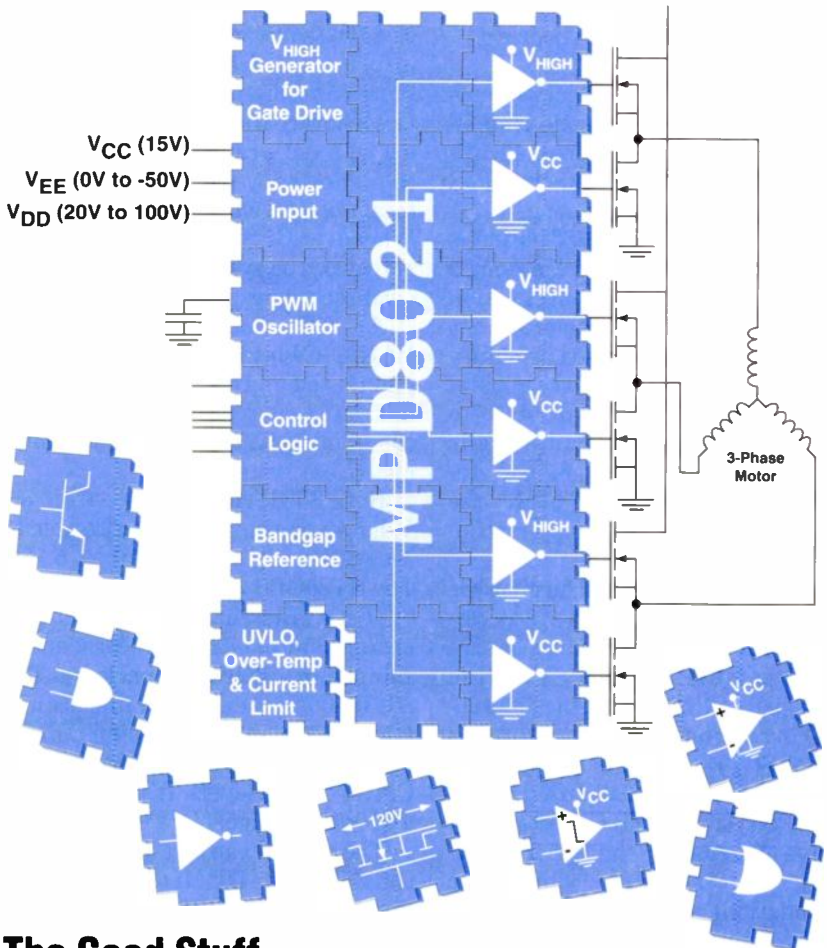

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emulation (ONCE) at full speed with hardware trace, hardware breakpoints, and watchpoints. In conjunction with the development system, which is attached via a serial JTAG port, the diagnostic controller allows debugging constructs such as "stop if this function is called for the eighth time by a specific part of the program."

Software Support

Within its software library, ST provides the following for a one-time license fee: the GPS function itself, differential correction, WAAS/EGNOS corrections, and dead reckoning.

If a standard NMEA 0183 output is required, the GPS function can remain unchanged. If, however, integration with other applications is required, GPS data will have to be accessed by library calls. At the simplest level, the application calls "gps_load" and "gps_start" to initiate the system. Then, it calls "gps_fix_store," "gps_fix_get_pos_status," and "gps_fix_get_pos" to read the resulting output every second, or whenever it's required.

While the GPS standard function has already been available for the predecessor, ST20GP1, two major extensions are now available for the ST20GP6. Through the RS232 ports, the differential-corrections library supports RTCM-SC104 differential corrections, which are conventionally used in marine GPS systems. This corrects for selective availability (the U.S. Department of Defense deliberate degradation), and for ionospheric errors, resulting in a position determination with an accuracy of within more than 10 m (usually 3 to 5 m).

This correction service requires additional information through other radio channels either from marine radio beacons or from long-wave transmitters (like those in Germany), or from FRM RDS signals. In the future, similar data will be available via INMARSAT satellites. This data service is called WAAS in the U.S. and EGNOS in Europe. Using this service does not require any additional hardware because it's a GPS-compatible signal on the same frequency.

The ST20GP6 can receive these INMARSAT satellites, which means that when the signals will be available in about two years, an external receiver will no longer be required. If buildings are blocking the signals from the GPS satellites, corrections will not be enough.

Automotive GPS systems need a backup system for city centers and tunnels. In most cases, this is a piezo-electric gyroscope for guidance and routing, in combination with a wheel-turn counter to determine the distance traveled. The software creating positioning information from these two data sources is called dead-reckoning. ST offers a library to combine dead-reckoning with GPS, calibrating the low-cost (i. e., not very precise) sensors by means of GPS when both are available. Whenever GPS signal reception does not work, the system switches back to dead-reckoning.

As ST's Mattos points out, a VAN/CAN interface may also be implemented on the chip if higher volumes are required. This would allow an easier integration into complex automotive bus systems.

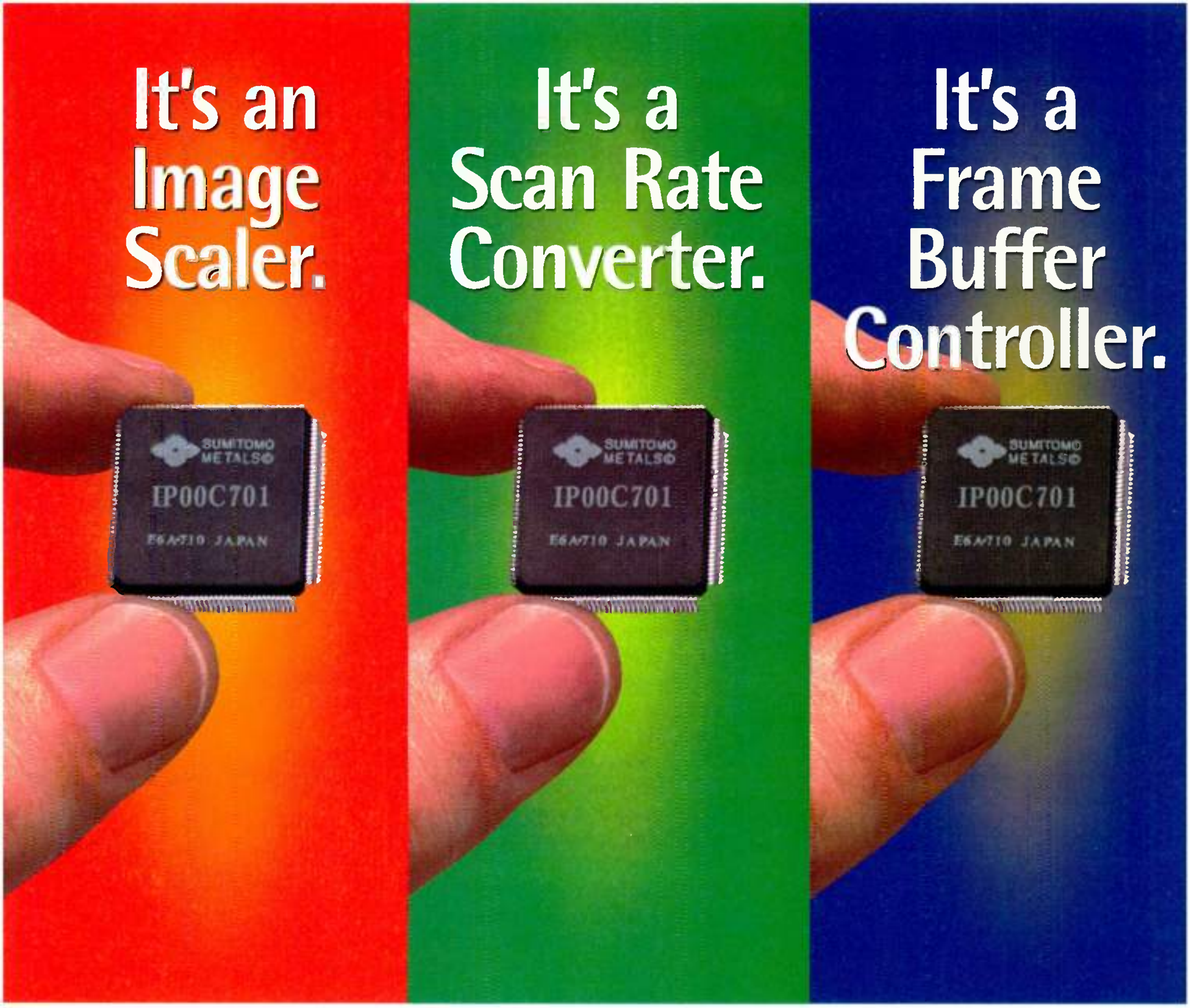
Both ST devices operate from 3.3 V, however, the ST5600 is also able to accept supply voltages up to 5.9 V. The ST20GP6 was designed in Bristol, Great Britain. It's manufactured on an 0.35-µm CMOS process, and is shipped in a PQFP100 package. The STB5600 was designed in Catania, Italy. It's manufactured on a high-speed bipolar process and offers CMOS output levels. It's shipped in a TQFP32 package.

The chip set can be evaluated using the ST20GP6-DEMO GPS Evaluation Kit. The kit is a hardware reference design intended to accelerate the evaluation, design, and development cycles of GPS applications based on the ST20GP6 microcontroller and the STB5600 RF front end. Together with the ST20GP6-SW1 reference software, the ST20GP6-DEMO reference hardware provides a starting point for GPS hardware evaluation and application development. Software running on the CPU performs control and positioning functions, and communicates off-chip via messages in NMEA 0183 format.

Price And Availability

The two-chip GPS set is immediately available at a price of $25 per set, in 100,000-unit quantities.

Contact STMicroelectronics, 55 Old Bedford Rd., Lincoln, MA 01773; (781) 259-0300; www.st.com; Philip Mattos e-mail: philip.mattos@st.com. CIRCLE 525



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PRODUCT INNOVATION

Digital Phosphor Oscilloscope Breaks New Measurement Ground

Fast Acquisition And Parallel Processing Bring A Wealth Of Information To The Display.

Joseph Desposito

Step aside ART and DSO, there's a new kid on the block. Its name is DPO—digital phosphor oscilloscope. Developed by Tektronix, the DPO is heralded as a technology that surpasses both analog real-time (ART) and digital storage oscilloscopes (DSO). It is targeted at engineers working with complex electronic signals during the debugging and verification stages of electronic design.

Tektronix has announced seven new DPO models, including four TDS 700D-series oscilloscopes (color display), and three TDS 500D-series oscilloscopes (monochrome display). The DPOs feature up to a 2-GHz bandwidth; four channels; a 4-Gsample/s, single-channel sample rate; and 8 Mbytes of single-channel record length. The top model in the line is the TDS 794D *(Fig. 1)*.

What Is A DPO?

By definition, a digital phosphor oscilloscope displays, stores, and analyzes complex signals in real time using three dimensions of signal information: amplitude, time, and distribution of amplitude over time. The DPO creates a 3D array that retains information for hundreds of millions of samples. Using this information, the DPO can replicate the range of intensities of an ART display by digitally controlling the replacement of data in the 3D array.

As a signal is acquired over time, this array is continuously updated with image after image of the signal. Unlike DSOs, which decimate, or throw away an enormous number of samples, the signals coming into a DPO are acquired at rates comparable to an ART, and are all used to create the image. This protects against aliasing due to the abundant number of samples collected and used.

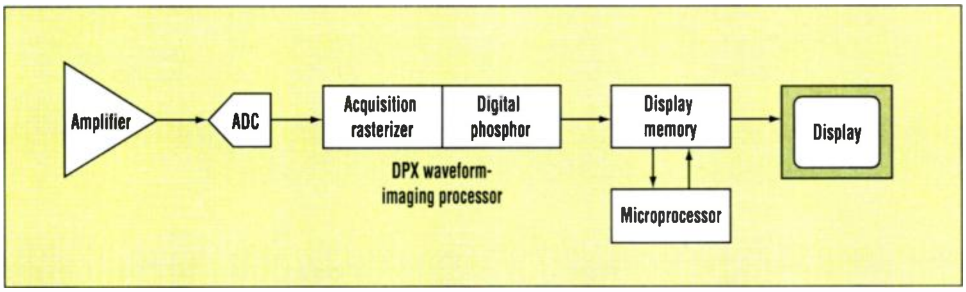
A hardware-based, parallel processing approach is used to achieve high performance (*Fig. 2*). Creating a detailed image of a waveform's activity in hardware makes it possible to achieve a real-time response similar to an ART. The acquisition engine of the DPO continuously samples at the maximum rate, triggering and building images with minimal dead time between acquisitions. A new snapshot is sent to the display every one-thirtieth of a second, creating an image that corresponds to waveform activity in real time. Even when the display is updated, the DPO continues to gather new samples. The DPO can capture all the details and anomalies that occur in today's complex, dynamic signals, and display them as fast as the human eye can assimilate them.

According to the company, real-time processing is what sets a DPO apart from DSOs using post-processing modes, such as persistence. Post processing in a DSO is executed in software, on the normally acquired waveforms. This requires acquisition over a long period of time to build up the display, thus prohibiting instantaneous feedback. The time needed to create this display is further lengthened as multiple channels are turned on, because they all use the same processor. Additionally, during this processing time, the DSO is no longer acquiring new information. It can miss salient details on dynamic waveforms and important aperiodic events. This is often the very behavior an engineer is hoping to uncover and examine.

The DPX Processor

At the heart of each Tektronix DPO is a patented DPX waveform-imaging processor. The DPX processor was designed by Tektronix specifically for acquiring and managing three dimensions of waveform information. A 0.65-µm CMOS, highly pipelined processor with 1.3-million transistors,

1. The Tektronix TDS 794D digital phosphor oscilloscope (DPO) shows the distribution of a metastable logic signal in real time, using color variations.



2. The figure shows a simplified block diagram of a DPO. A hardware-based, parallel-processing approach is used to achieve high performance.

the DPX is tailored for high-speed image acquisition and memory management. To ensure maximum throughput, it has distributed internal control, and works independently of the other processors in the oscilloscope.

The DPX waveform-imaging processor is completely dedicated to the acquisition and database management process. It includes an acquisition rasterizer and digital phosphor 3D database array *(Fig. 3)*. This enables the DPX processor to emulate the behavior of chemical phosphorescence to provide a real-time, intensity-graded display. The basic operation of the DPX waveform-imaging processor involves drawing repeated images in the digital phosphor, controlling the rate of image decay, and periodically sending snapshots of that information to the oscilloscope's display system.

The gigabyte-per-second acquisition memory of the TDS oscilloscope is harnessed by the DPX processor to create an image composed of multiple waveforms. The top-of-the-line TDS DPO can acquiring up to 200,000 records/s, and up to 500,000 samples in a single acquisition.

The DPX waveform-image processor accomplishes this feat by incorporating a full 21-bits of gradation information in the digital phosphor's 500-by-200-pixel array. This array represents each pixel on the display. The information is compressed to 4 bits on the display, shown as 16 levels of intensity grading. This depth is what enables DPX to retain so much waveform information, and show the distribution of the signal over time. Each time the oscilloscope triggers, and draws a new waveform into the array, the data is used to update the 21 bits for every point that describes the waveform.

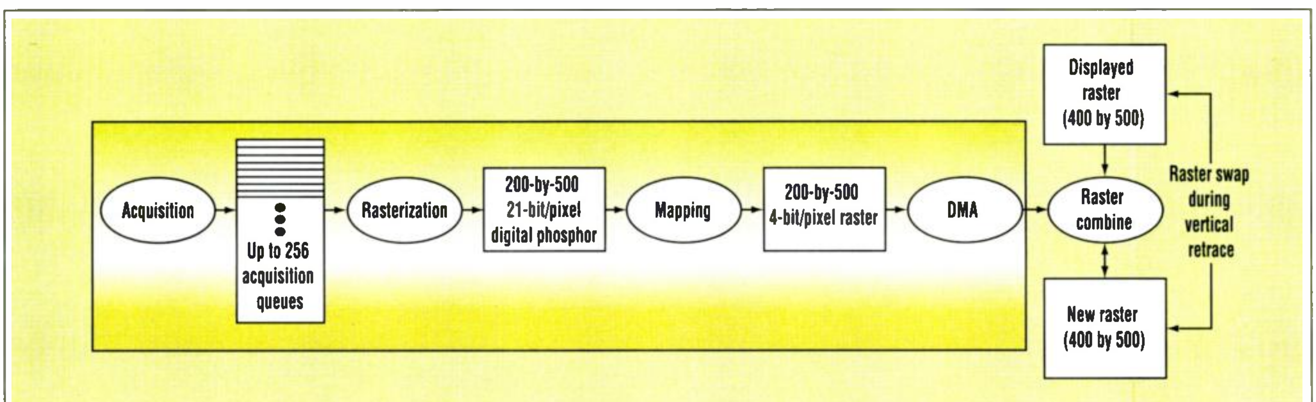
In the histogram mode, the DPX engine extends each point in the digital phosphor to be 32- or 64-bits deep. This enables the oscilloscope to build a statistically significant database in just a few seconds. It also makes it possible, for example, to characterize long-term drift in communications applications, and high-speed jitter in microprocessor-based development. The deeper bit level ensures that the digital phosphor does not saturate or overflow, even if the designer examines signal behavior over a period of days. In addition, any portion of the histogram, whether live or stored, can be examined to determine the distribution of the waveform data.

The digital phosphor contents can also be exported from the DPO to a PC for 3D plots using common application software such as Excel or Mathcad. The result is a unique 3D representation of the waveform that provides further insight into the behavior of the signal over time.

In the XY or XYZ modes, Tektronix's DPO display works much like a scan converter. It continuously draws samples at a rate of 10.4 Msamples/s into the digital phosphor and scans the information out serially to the display at 1 Mpixels/s. The effect is a display analogous to a 10.4-million-point electron ART, with no rearming dead time. This continuous acquisition enables a dynamic and accurate XY display. Compare this to the XY display of a DSO, which does not provide sufficient sample density or continuous acquisition.

Depending on the time/div. setting, the DPX waveform imaging processor automatically selects a long record length and sample rate to maximize the data density. As a result, the DPX acquisition capabilities can compress lengths of up to a half-million-million samples or as few as 500a, enabling it to present an accurate, detailed representation of the signal at any sweep speed.

The DPX waveform imaging processor simultaneously uses three different methods to create the digital phosphor and resulting real-time intensity-graded display: repeated drawing,



3. Shown here is a simplified block diagram of the DPX waveform-imaging processor used in Tektronix's digital phosphor oscilloscope (DPO). The acquisition engine and the digital phosphor 3D database array are key components of the proprietary chip.

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compression, and slew-rate weighting.

The repeated drawing approach is used at all but the slowest-sweep speeds. Because the DPO can trigger at a much faster rate, the DPX processor repeatedly draws the acquisitions into the digital phosphor, accumulating brightest intensities where the signal overlaps most frequently. By relying on multiple acquisitions, the processor can build intensity and statistical information about the waveform.

The compression approach is used at all but the fastest sweep speeds, because the DPX engine has time to gather up to 500,000 samples on a single acquisition. To show the viewer all this information in one display, it compresses the data into the 500 columns that make up the digital phosphor array. As a result, multiple points in time are compressed in the display, and the resulting intensity reveals areas where the signal spends most of its time.

This ability to show a large amount of signal activity in a single display is ideal for complex waveforms such as packetized data in telecommunication, disk-drive, and video signals. Instead of painstakingly scrolling through enormous waveform records, engineers can view a complete sector of a disk-drive sequence in one display, and immediately see any anomalies. They can even gather all the information on a composite TV signal in one display.

Slew-rate weighting is used when drawing vectors. The DPO display emulates an analog oscilloscope's display, showing dimmer fast edges and brighter signal peaks. This varying intensity indicates that the signal is spending more time at the top and the base of the waveform, and less time at the transitions. This is especially useful when examining envelope-type waveforms. The viewer can immediately tell the difference between a sine, square, or triangle wave by merely looking at the intensity of the edge and peaks.

PRICE AND AVAILABILITY

The TDS550D and 700D series of digital phosphor oscilloscopes are available with eight-week delivery times from receipt of order. Prices are as follows: TDS580D, $18,490; TDS540D, $15,750; TDS520D, $9760; TDS794D; $34,995; TDS784D, $22,495; TDS754D, $17,990; TDS724D, $12,695.

Tektronix Measurement Business Division, P. O. Box 3960, Portland, OR 97208-3960; (800) 426-2200 (press 3, code 1080; fax (503) 222-1542; www.tek.com/Measurement.

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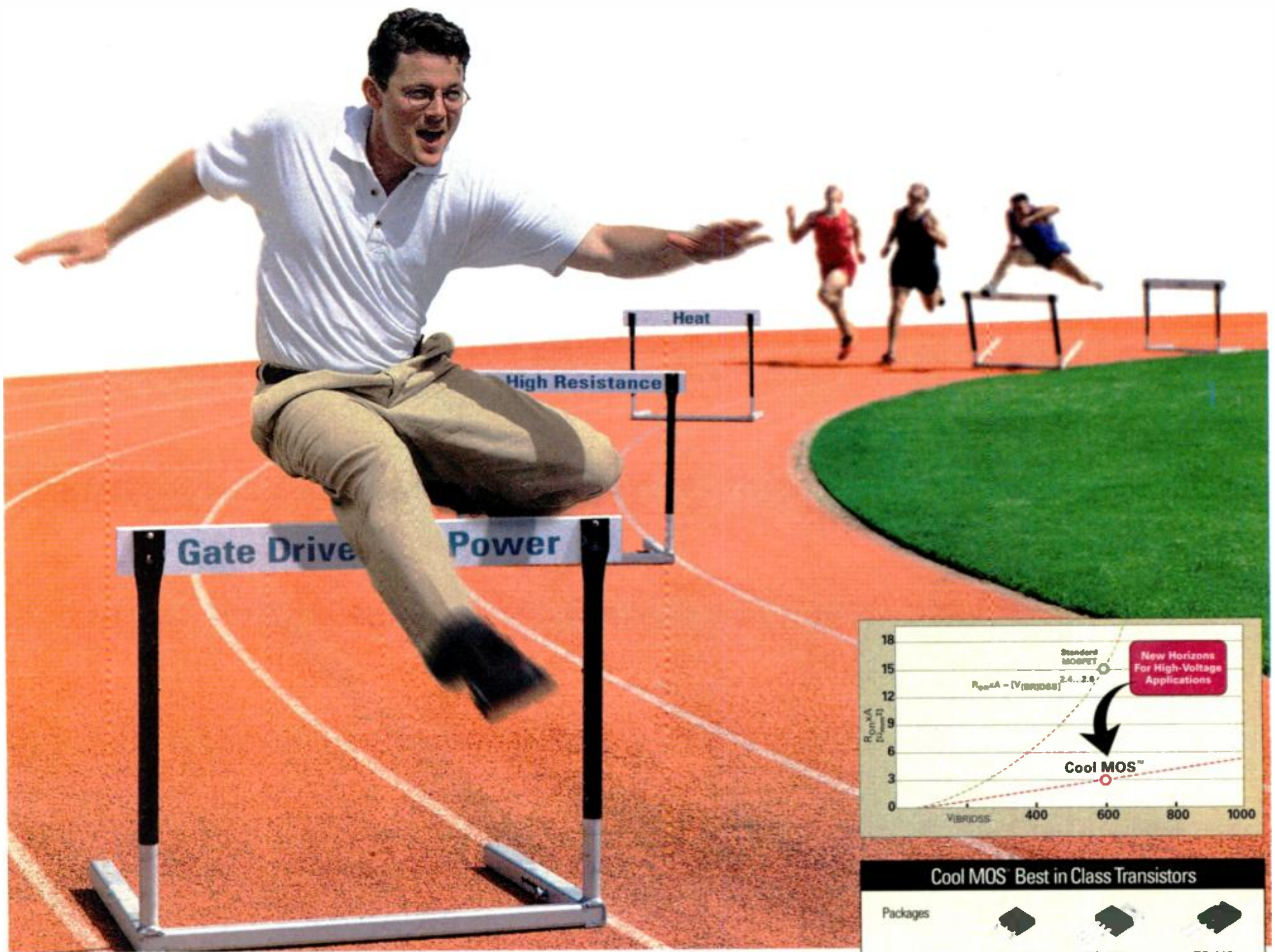

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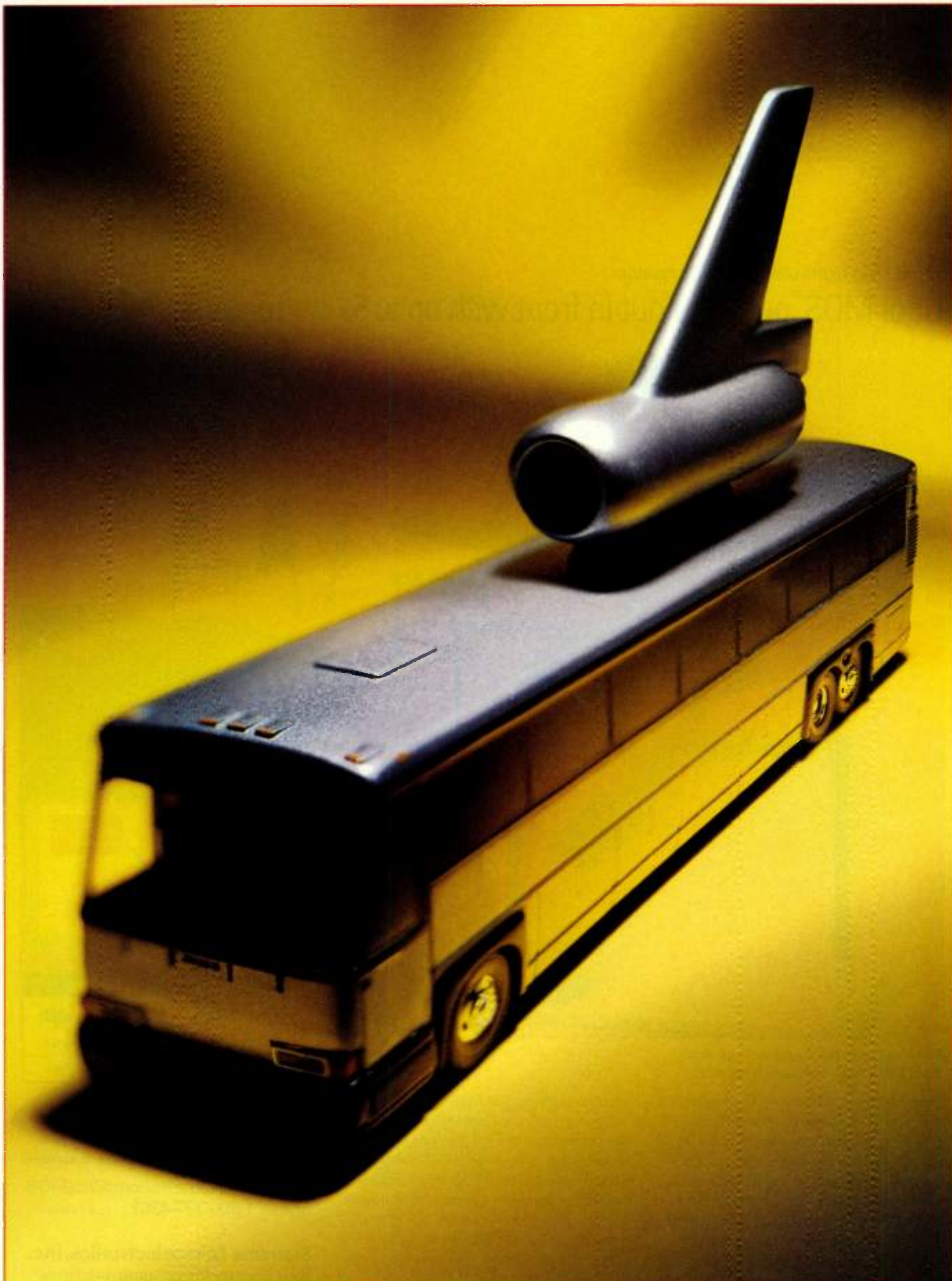


(WHEN A PIECE OF TECHNOLOGY LIKE THIS COMES ALONG, WE'RE GOING TO SUPPORT IT.)

ELECTRONIC DESIGN QUICK LOOK

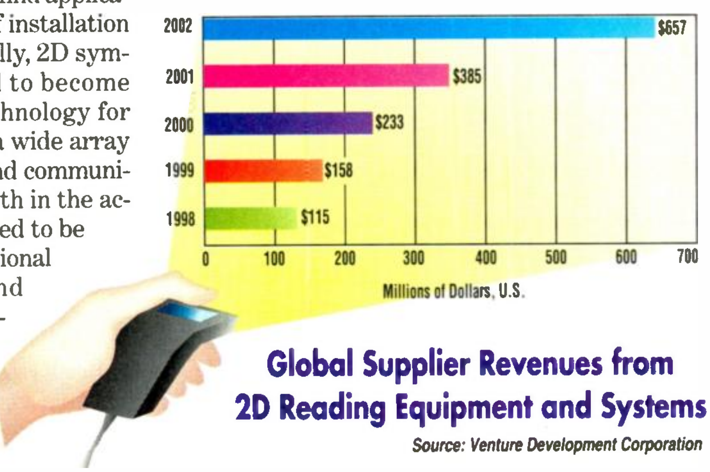
■ Edited by Debra Schiff and Nancy Konish

MARKET FACTS

2D Symbology Plunges Reading Code Into Profit

Anxiously, they've been waiting...and waiting. For nearly a decade, AIDC industry participants and observers have been predicting the market for two-dimensional (2D) reading equipment and systems. Finally, in 1997, global market consumption of these scanning systems reached nearly $90 million. The 1997 market represents the tip of the iceberg for 2D symbology applications. These symbologies are expected to find applicability in a broad range of installation environments. Specifically, 2D symbologies are predicted to become both a key enabling technology for AIDC subsystems and a wide array of computing, control, and communications platforms. Growth in the acceptance of 2D is expected to be complementary to traditional (linear bar codes) and emerging (RFID tagging) AIDC technologies. Some displacement of these technologies is expected. A coherent map of the most appropriate, application-specific technology solutions, however, has not yet been developed. The challenge will lie in realizing profitable revenues from the sale and support of 2D symbology reading equipment and systems. End-users and resellers generally know little about the values of, or requirements for, adopting this technology. Moreover, education and training skills have proven to be difficult to develop. Regional and vertical market opportunities are developing with vastly different rates. The effective delivery of application-specific solutions (a perceived requirement for profitable participation) will therefore vary across nearly all market segments. The overall markets for 2D reading equipment and systems are expected to grow as rapidly as 50% per year during the next five years. Yet, hopeful suppliers of 2D reading equipment and systems must address a number of specific issues, including the following questions:

- Of the symbologies, which are commercially viable? In which markets? For what applications?
- What hardware, software and service components constitute a 2D-symbology solution?
- Who currently uses and evaluates 2D symbologies? What are their service requirements? Do they have preferences for marking and reading equipment?
- During the next two to three years, which markets for 2D symbology reading equipment and systems will be the most lucrative?
- What do I need to participate in this business?



Global Supplier Revenues from 2D Reading Equipment and Systems

Source: Venture Development Corporation

The single most important factor that will enable or restrain growth in this market is end-user community education. Technology suppliers, system integrators, and end-users agree that a lot of work is required to prepare this market for broader acceptance and further penetration. As part of Venture Development Corp.'s recent study, "Global Markets and Applications for Two-Dimensional Symbology Reading Equipment and Systems," suppliers and integrators were surveyed on their perceptions of market knowledge of 2D symbologies. Some potentially alarming statistics were revealed. On a scale of 1 (no knowledge of 2D) to 10 (comprehensive knowledge of 2D), suppliers and integrators rated the current market at 3.5. Their estimated knowledge level requirement was 7.0. The end-user survey revealed that fewer than 35% of current 2D users and evaluators consider 2D suppliers and integrators their prime source of valuable information on 2D technologies. Clearly, 2D suppliers and integrators must strive to realize their share of this emerging market.

Christopher John Rezendes is director, AIDC Industry Research and Consulting Group at Venture Development Corporation. He and his team provide research and consulting services many of the leading suppliers and integrators of AIDC equipment and systems. Rezendes is a graduate of Harvard University, Cambridge, Mass. He can be reached at cjr@vdc-corp.com.

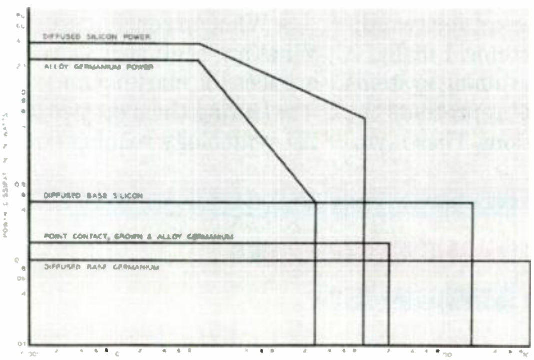
40 YEARS AGO IN ELECTRONIC DESIGN

Decade Of Transistor Progress

Progress over the past 10 years in the transistor field has been feverish and exciting. The transistor chart in this issue, which lists 619 units, indicates this growth. Our first transistor chart in 1953 listed 43 available types. From 1948, the year of the transistor's invention, to 1958, when transistors provided the radio voice in our satellites, some of the realized potentials of the transistor were:

- Diffused-base transistors operate in the 1000 mc range;
- Rise, storage, and fall times of switching transistors in the order of 10 millimicrosec;
- Operating junction temperature over 100°C with silicon transistors;
- Germanium power transistors available with power gains of 35 db, and collector currents of 13 amp.

Operation frequency is plotted in Fig. 1 as a function of power dissipation for various types of transistors. Values of alpha cutoff frequencies are used. For oscillator applications, higher values of frequency are possible. Lower values would apply for broadband applications. Areas beneath the curves show that the trend of transistor device development continues toward the latest types of structures, with wider ranges of operating characteristics.



As the power rating of a transistor is increased by enlarging the active areas of the emitter and collector, a corresponding increase in the value of C_{be} is inevitable, reducing the operating frequency range. The use of diffusion techniques to produce a graded base, or drift transistor, extends the frequency range for any given power device. *(ELECTRONIC DESIGN, July 9, 1958, p. 5)*

The first issue of July traditionally contained ELECTRONIC DESIGN's Annual Report on Transistors. In the early years, the report listed every commercially available transistor. Eventually, such lists became impractical.—Steve Scrupski

New Literature: Computer Design Techniques

This well-illustrated booklet explains the application of advanced computer-aided design methods. It begins with the checking of logical equations for systems definition, and continues with the preparation of component lists and wiring tabulations. Control Data Corp., 501 Park Ave., Minneapolis, Minn. *(ELECTRONIC DESIGN, July 9, 1958, p. 100)*

The roots of computer-aided logic design run deep.—Steve Scrupski

New Literature: Egghead Manual

An invaluable guide to aspiring eggheads is now in its second printing. "On Being An Egghead, or Engineermanship for the Shell of It," contains a complete set of rules for egghead behavior. The booklet is fully illustrated. Benson-Lehner Corp., 11930 W. Olympic Blvd., Los Angeles 64, Calif. *(ELECTRONIC DESIGN, July 9, 1958, p. 99)*

As we've mentioned before, engineering humor seemed to be more prevalent in the '50s than it is today (Scott Adams and Dilbert notwithstanding). This booklet looks intriguing; does anyone out there have a copy?—Steve Scrupski

Steve Scrupski is a former Editor-in-Chief of ELECTRONIC DESIGN. Now semi-retired, he can be reached at scrupski@worldnet.att.net.

OFF THE SHELF

RFMD Silicon Innovations Designer's Handbook features new data and the latest in RFMD silicon-based RFICs. It includes more than 50 wireless components, technical information, performance test data, product specifications, schematics, application notes, and articles on the components. Also available is the latest *RFMD Designer's Handbook* and the current designer supplement. Both handbooks can assist engineers to choose wireless components by something other than price and availability. The catalogs are free, and are available in both print and CD-ROM format. Contact RF Micro Devices, 7625 Thorndike Rd., Greensboro, NC 27409-9421; (910) 664-1233; Internet: www.rfmd.com.

Datacom/Networking Cookbook Number 11 is the latest from Telebyte Technology Inc. Its aim is to help datacom professionals, electronic design engineers, and system architects deal with process control, power utilities, and manufacturing. The catalog includes an expanded section on application notes, as well as solutions and ideas for networking data communications. Highlights include the new fiber optic networking products. The 136-page catalog is available from Telebyte Technology Inc., 270 Pulaski Rd., Greenlawn, NY 11740; (800) 835-3298; Internet: www.telebyteusa.com.

Digital Transmission Lines concentrates on the use of mathematical algorithms to simulate the increasing of circuit board signals. The algorithms demonstrate the design of digital transmission lines that are compact, but have low crosstalk. The book covers "Transmission Line Fundamentals," "Circuit Solutions at Line Terminations," "Propagation in Layered Media," "Transmission Line Parameter Determination," and "Simulation of Skin Effect." The 333-page book is priced at $53.00. Contact Oxford University Press, 198 Madison Ave., New York, NY 10016.

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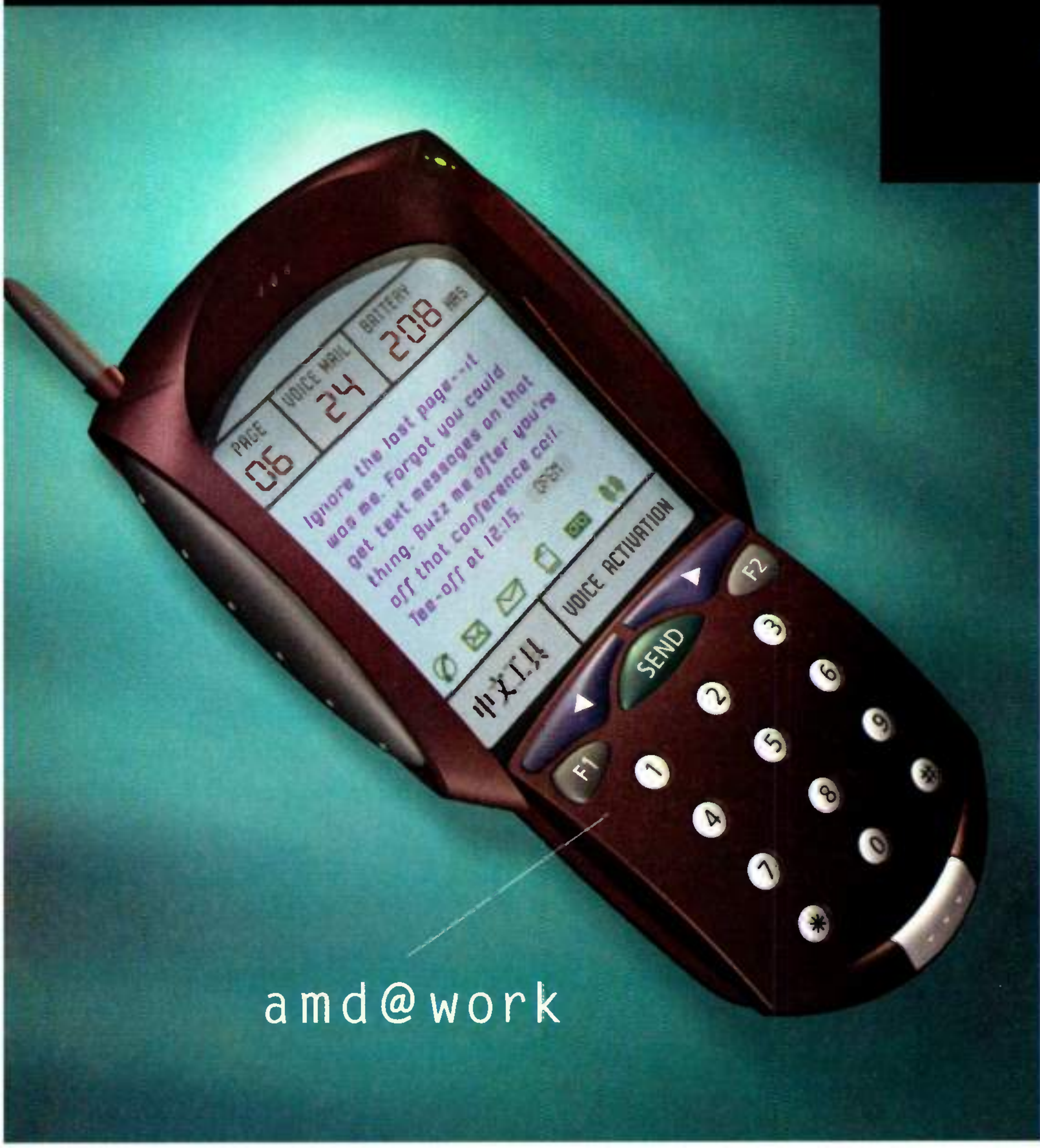

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I/O Bus	32	64
I Cache Size	32KB	32KB
D Cache Size	32KB	32KB
Pin Count/Package	208 PQFP	272 ABGA
Dhrystone MIPS	347	415, 519
On-chip Debugging	JTAG boundry scan port, N-wire and N-trace functions	
Power Consumption	2.5W	3.5W, 4.4W
Multimedia Extensions	Yes	Yes

NASA's Neurolab Is SHARC Infested

Space Shuttle Columbia's recent STS-90 flight carried hundreds of critters—mice, rats, snails, crickets, and fish—into orbit. The purpose? To perform life-science experiments in NASA's Neurolab. Through a series of 26 human and non-human sensory and motor skill tests, NASA explored how the nervous system develops and functions, both in space and on earth.

The Neurolab Sensory Motor Experiment 136 tested voice compression in space. The experiment's hardware consisted of a SHARC-based digital signal processing (DSP) board, Snaggletooth, from BittWare Research Systems, Concord, N.H. Snaggletooth, a 40-MHz ISA DSP board, was the main voice recording mechanism for NASA's Virtual Environment Generator (VEG).

The VEG system includes a 3D graphics processor, helmet-mounted display with a wide-field view, head tracker, headset, and joystick. It is designed to provide a controlled, interactive, virtual environment. Developed by Lockheed Martin, Marietta, Georgia, the VEG's headset microphone tracks the astronaut's comments, and simultaneously archives and downlinks voice data to earth in real time.

BittWare's Snaggletooth board, with an AMBE-1000 vocoder from Digital Voice Systems Inc. (DVSI), Burlington, Mass., provides the main voice compression engine for the VEG. It compresses at a constant bit rate of 4 kbytes/s. Voice is compressed on board. It is then downlinked to Johnson Space Center's Mission Control, where it is decompressed by another Snaggletooth board in real time.

The VEG platform for Neurolab is a generic system designed for multiple flight use, including upgrades for the forthcoming International Space Station. Based on a 200-MHz Pentium Pro processor, with 256 Mbytes of RAM, it includes a 13-board passive backplane in a custom ruggedized drawer. The Snaggletooth SHARC board is configured with an eight-channel analog audio I/O mezzanine with DVSI voice compression and 16 channels of digital I/O.

The system includes five cards for virtual reality graphics generation (an accelerator card, two cards for left-eye generation and two for right-eye), and a special telemetry downlink data interface. The software used is Windows NT and WorldToolKit from Sense8 Corp., Mill Valley, Calif. The SHARC chip, from Analog Devices, Cambridge, Mass., has a 32-bit floating point core, and offers up to 40-MIPS performance, with a peak of 120 MFLOPS.

More information about NASA's Neurolab can be found on the Web. Just point your browser to www.neurolab.nasa.gov.

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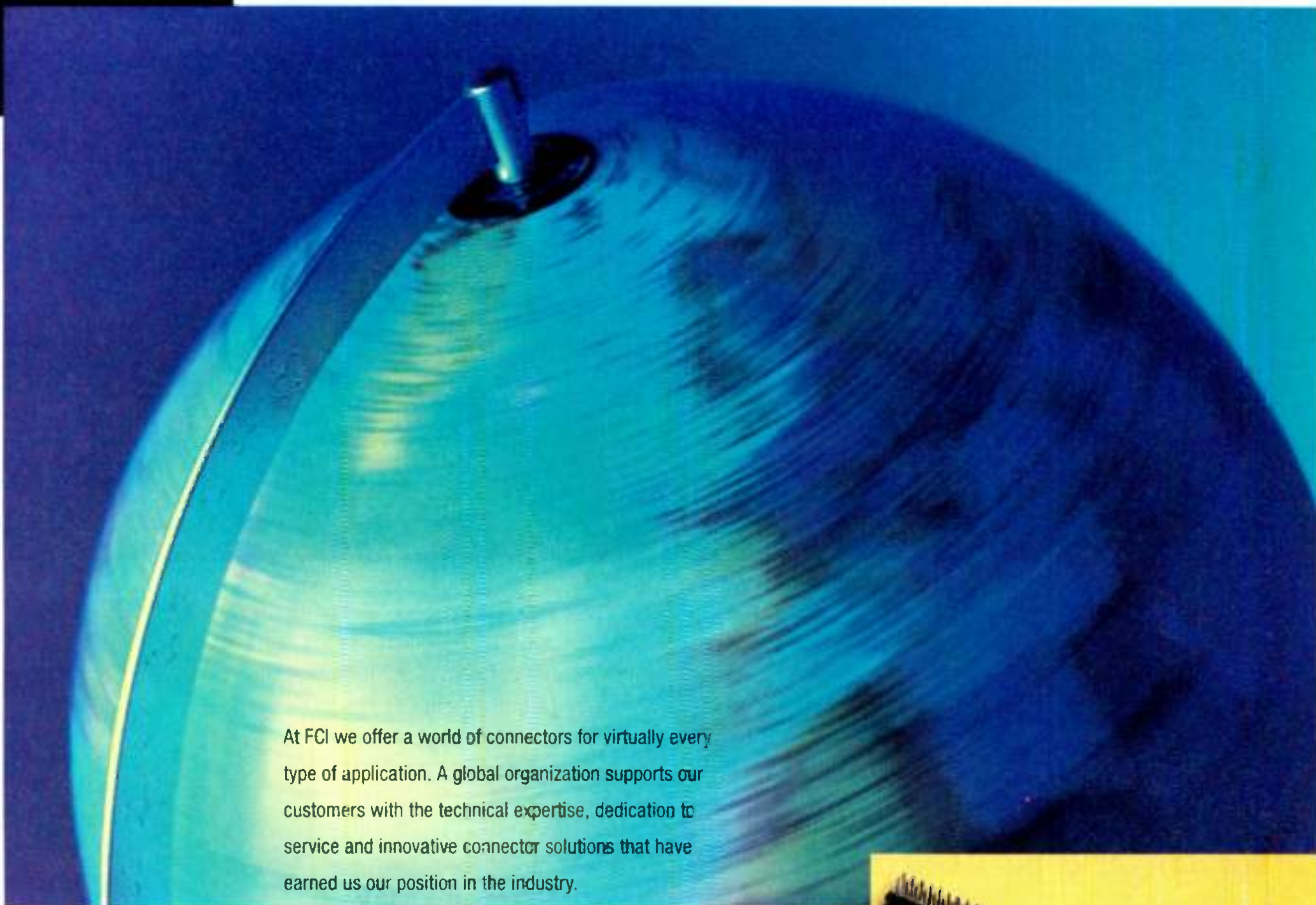

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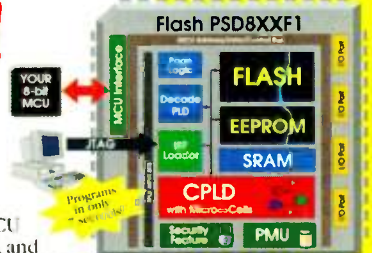

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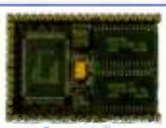

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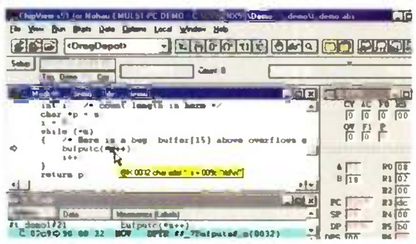

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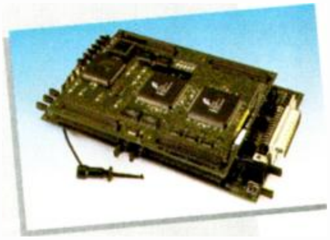

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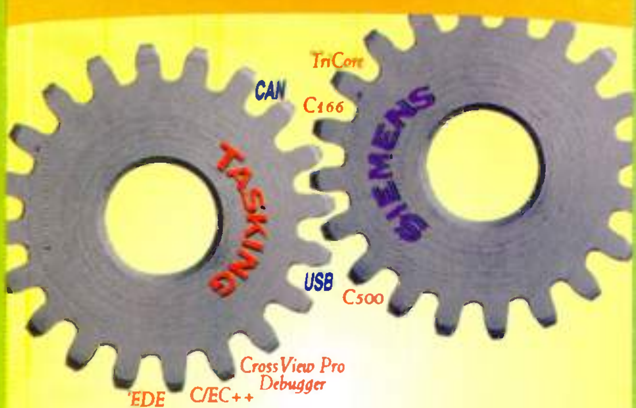

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MANAGING THE DESIGN FACTORY

The Gap In Subsystem Testing

Many companies have effective component testing processes. And, many companies have good system testing processes. However, most companies have great weaknesses in the way they do subsystem testing. They simply do not understand the economics of testing at intermediate levels in the system. They view subsystem testing as expensive and adding extra delays to the project. As a result they, do too little testing at a subsystem level.

The reality of subsystem testing is actually quite different. Such testing offers more benefits than system testing. Finding problems in a well-designed subsystem test can be both cheaper and faster than finding the same problems in a system test. Why? System tests usually rely on naturally occurring faults to break the system. Such naturally occurring faults occur at random. For example, when testing a copier, you might have to wait for a open circuit on the fuser roller before you know whether your software can respond to this error. It can take a long time for this condition to occur during natural testing processes because fuser rollers don't open circuit too frequently.

DON REINERTSEN

In contrast, we could test the control electronics of the copier as a subsystem by feeding it simulated signals from the mechanical engine. With such a configuration we can generate the set of all possible fault signals in a matter of minutes. It is not unusual to compress testing times by 100 to 1 or more with good subsystem testing. With this speed improvement comes a dramatic reduction in the cost of testing.

If there is a huge opportunity in subsystem testing, why don't more companies take advantage of it? There are two reasons. First, it is the rare company that properly analyzes system testing data. Every time you find a defect in system testing you should ask, "How could I have found this defect at an earlier stage of testing?" I have found cases where 80% of defects found in system testing could have been found more cheaply and faster in a well-designed subsystem test.

The second reason for poor subsystem testing is our unwillingness to allocate resources to the problem. This comes from a fundamental misconception about development testing. Most companies view an investment in the testing environment as a waste of money. "After all," they think, "the only reason we spend money on testing is because our engineers don't know how to do the design right the first time! We want to invest in preventing defects not in finding them."

Nothing will do more to guarantee a stone-age testing department. A good test department is one of the most precious treasures a product developer has. You will never improve testing if you do not invest time and money in this problem. In one case, I saw a manufacturer of radio equipment improve their testing productivity by a factor of 50. Unfortunately, it had to be done by hiding money in dark corners of the budget and stealing engineers to work on the project. After 10 years of working on a shoestring, they had completely overhauled their testing process. It would have been much nicer if it had been done with high-level management support, instead of as an underground project.

Where can you start? Carefully analyze the defects that are showing up in your system tests. Ask if some of these defects could be found in a well-designed subsystem test. Calculate the impact on development speed and expense by doing so. You will probably be astounded at how much you can save with good subsystem testing.

Don Reinertsen is president of Reinertsen & Associates, a consulting firm specializing in product development management. He can be reached at (310) 373-5332 or e-mail: DonReinertsen@compuserve.com.

Y2K UPDATE

You are now pronounced...partners in dealing with the Y2K issue. Such a union did take place recently between Oracle Corp., Redwood Shores, Calif., and Ravel Software Inc., San Jose, Calif.

Ravel Software's UNRAVEL 2000 offers a variety of languages, platform independence, the parser-based engine, and the convenience of online integrated project management and integrated code repository. Perhaps most important, it's also user-friendly.

Oracle has already begun its Y2K compliance with recent developments in database and information management tools. Oracle's customers have adapted these new products for inputting forms, processing, and reports. Yet, it is probable that these entries are non-compliant, which is where UNRAVEL 2000 steps in.

UNRAVEL 2000 reads and evaluates everything. It then identifies any date variables that may cause problems in Oracle applications and development tools. The software also guides and tracks the repairs. UNRAVEL 2000 possesses tools which will enable Oracle to assess their individual customers' systems, as well as offer them detailed plans to deal with Y2K.

Dave Ghosh, CEO of Ravel Software, stated, "Since its inception, Ravel has been involved with Oracle as a leading member of the Oracle Tools Initiative program. This close working relationship has allowed us to design our tools specifically to meet the needs of the Oracle user community."

The UNRAVEL 2000 Product Suite has a tool for SQL*Forms 2.3, 3.0, Forms 4.5/5.0, SQL*Reports/ReportWriter 1.1, and Reports 2.5/3.0. Also included are tools for C/C++, PowerBuilder, Unix Shell Scripts, Visual Basic, Perl, Jam, FoxPro, SQR, T-SQL and Cobol.

For more information, contact Ravel Software Inc. at (408) 955-1990, or visit their web site at www.unravel.com.

Lisa Calabrese

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JUST 4 THE KIDS

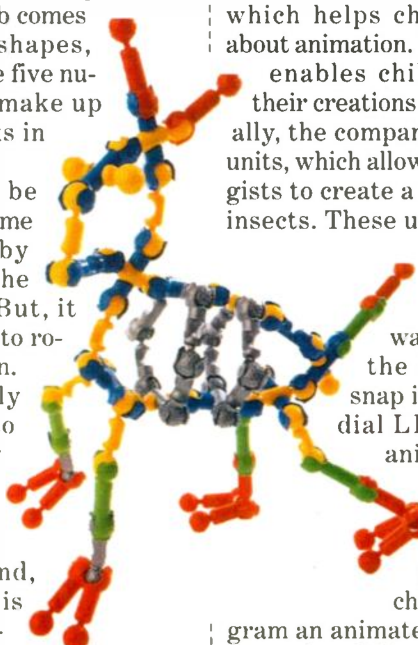
How many of you have ever played with mud? I know I did, and I don't think I'm alone when I say I wish there was a way to recapture that feeling of squishing my hands through mud—without having to get my hands dirty. Thanks to a San Francisco-based company known as Primordial LLC, we may now have our wish.

What they've come up with is a hi-tech creation, known as a Zoob, that can be played with by children ages five and up. This toy—a brightly colored, plastic, linking toy that resembles genetic strands of DNA—is so unique in construction that it can even be utilized for a number of different engineering and bioengineering applications.

Granted, the name of the toy, "Zoob," may sound relatively simplistic. But, don't be fooled—there is nothing simple or trivial about this toy. The word "Zoob" stands for zoology, ontology, ontogeny, and botany.

Resembling a two-and-a-half inch bone, the toy consists of a shaft with a socket on one end and a dimpled sphere, called a "citroid," on the other. This ball-and-socket (citroid) system was specifically devised as a means of replicating the connecting elements in nature. In keeping with this intent, the Zoob comes in five different shapes, each inspired by the five nucleic acids which make up the building blocks in every living thing.

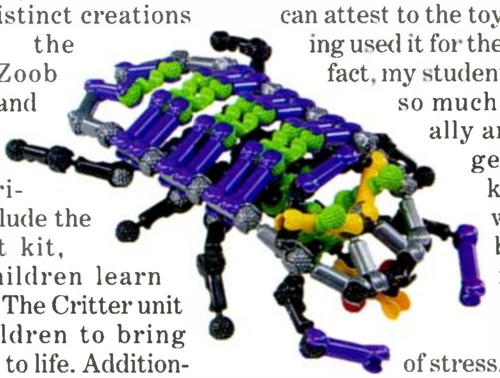
The Zoob can be used in much the same way as a lego—by simply snapping the pieces together. But, it also has the ability to rotate in any direction. The Zoob truly brings the lego into the 21st Century by creating a potentially endless number of swirling, life-like forms. And, because the Zoob is genderless, it dispenses with the dated male/female stereotypes typically associated with many toys.



The Zoob toy successfully combines art, geometry and anatomy. It is ideal for children who enjoy creating anything their minds can imagine. The toy can also help the child develop important skills. While a child plays with the Zoob, he or she is also improving dexterity, hand-and-eye coordination, and higher-level thinking skills.

MARIFRANCES WILLIAMS

A number of structures can be developed using the Zoob play system. For example, with the right combination of pieces, a Zoob can closely resemble the double helix of a DNA strand. Using the Zoob Rex kit, the child can create a Tyrannosaurus Rex. And, it does not stop there. They can even build toys that can morph or change into four movable, distinct creations that include the Zoobamator, Zoob craft, Zoob bot, and Zoob hawk.



Other offerings from Primordial LLC include the Zoobtoons unit kit, which helps children learn about animation. The Critter unit enables children to bring their creations to life. Additionally, the company offers two other units, which allow budding entomologists to create a variety of movable insects. These units are called Hot Citropod and Cool Citropod.

For the child who wants to do more with the Zoob than simply snap it together, Primordial LLC has created an animated video to coincide with the Zoobtoons unit. With some computer knowledge, children can even program an animated Zoob creature to dance, by visiting the company's web site at *www.zoob.com*.

The versatility of the Zoob makes it a natural toy for children of all ages. At the same time, it is equally well-suited for more advanced uses, such as anatomical, architectural, and mechanical modeling. In fact, recognizing this capability, Primordial LLC is planning to develop a bioengineering curriculum to help teach DNA sequencing.

The Zoob toy is now available in units, or quantities, of 35, 70, 120, and 280. The toys can be purchased at a number of book, museum, and toy stores nationwide. Prices range from $6.99 for a Zoobdude, to $79.99 for a 280-unit kit.

The Zoob toy can be used in schools to help with both math and science curriculums. As a teacher, I can attest to the toy's success, having used it for these purposes. In fact, my students enjoy the toy so much they continually argue over who gets to use the kits first, and what they will build. Take it from me, if you want to save yourself a lot of stress, buy a separate kit for each of your children. Ultimately, whether you buy the toy for your child or for yourself, it's guaranteed to offer you a fresh and creative look at the world around you. Happy creating!

For more information, contact Primordial LLC, 450 Geary St., Suite 400, San Francisco, CA 94102; (415) 923-1895; www.zoob.com.

Marifrances D. Williams holds a degree in Liberal Studies from San Diego State University, Calif. She is currently a fifth-grade teacher at Los Ranchos Elementary, San Luis Obispo, Calif. Williams specializes in the identification of advanced technology for the use of child-focused applications. She may be reached at williamsofsm@lightspeed.net.

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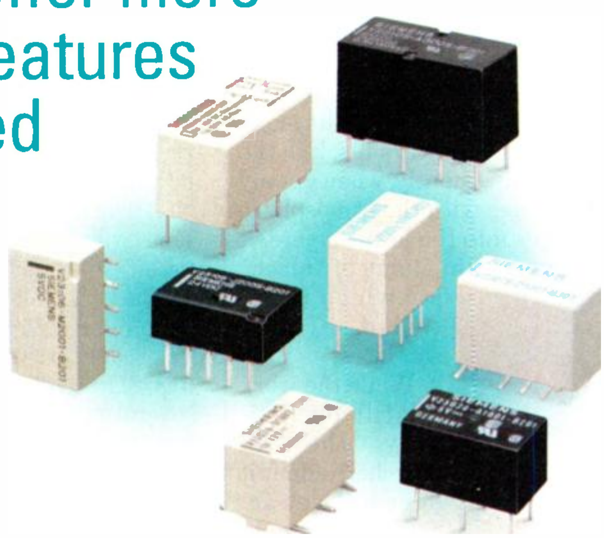

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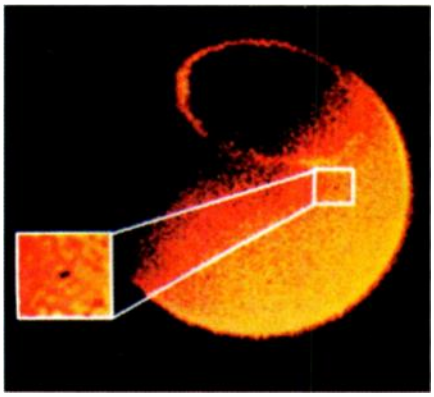
Dark Spot Theories Garner Much Skepticism

I have always tried to live by the credo that anything is possible unless proven otherwise. After all, it wasn't *that* long ago that people actually believed the world was flat. Yet, Galileo dared to think otherwise, claiming that the world was round. And, despite his excommunication from the church, and dismissal by his scientific colleagues as a nut, in the end, the world proved to be round.

Why is this significant? Because, despite skepticism, space scientists Louis Frank and John Sigwarth, from the University of Iowa at Iowa City, have put forth a hypothesis on the origin of transient dark spots that suggests they are caused by water vapor from 30,000 house-sized comets that strike the Earth's atmosphere each day. This theory runs counter to conventional wisdom. It is based upon the Dynamics Explorer-1 satellite's observations of transient dark spots in the upper atmosphere's far-ultraviolet dayglow emission.



As critics of their hypothesis point out, the tremendous daily influx of small comets that would need to occur for the theory to be true has yet to be observed. And, if true, the water-bearing comets would add massive quantities of water to the Earth. If it were shown to happen, much of what is known about comet creation and the origins of oceans, terrestrial life, and perhaps even of the solar system, might need revision. Nevertheless, Frank and Sigwarth are holding firm to their hypothesis. In fact, they claim recent evidence from observations made by the NASA satellite Polar validates their theory by providing support for the existence of the dark spots.

While the comet theory offers one explanation for the existence of dark spots, physicist Mark Boslough, Sandia National Laboratory, Albuquerque, New Mexico, and researcher Randy Gladstone, Southwest Research Institute, San Antonio, Texas, believe they know the real cause of the dark spots: meteor plumes.

Using complex computational simulations, they determined that ordinary meteoroids can form dark spots similar to those observed by satellite instrumentation. The computations were based on Sandia's CTH shock code, as well as earlier computations which led to the prediction of visible plumes from Comet Shoemaker-Levy 9's impact into Jupiter in 1994.

According to the results of these computations, atomic oxygen is momentarily displaced by the passage of meteoroids. Normal air from lower altitudes contains oxygen in its molecular form, and appears black to the satellite. Consequently, when a stony object collides with the atmosphere and plunges into the lower layers, it ejects a very thin plume of "black" air which is detected by the satellites.

While the work is still preliminary, the researchers admit it does not yet account for the observed high rate of dark-spot formation. Boslough and Gladstone are convinced that it's simply a matter of time before the U.S. Department of Defense satellites detect an infrared flash from a large meteor that corresponds exactly to the time and location of one of the spots. This would serve as the proof which they will need to validate their claim.

As more researchers now find themselves joining in this dispute, it is evident that the mystery surrounding the origin of dark spots is not likely to go away any time soon. Advances in computer technology, algorithmic models, and electronic observation equipment promise to help provide the missing clues. But, it will still fall on forward-thinking scientists like Galileo, to put the missing pieces of the puzzle together and solve the mystery.

For more information, check out Sandia's web site at www.sandia.gov.

Cheryl Ajluni

Lend E.T.s An Ear

If E.T.s are calling, how can you answer? First, you need a great big, powerful antenna. That's why the Search for Extra-Terrestrial Intelligence (SETI) League just acquired a 60-ft. radio telescope. Now they can listen to the whole universe.

Noel C. Welstead, SETI coordinator for eastern Australia, made an agreement with the Australian Commonwealth Scientific & Industrial Research Org. (CSIRO) to obtain the telescope. Though the telescope currently stands at the Parkes Radio Observatory, New South Wales, Australia, it will eventually reside in Boonah, a rural town abut 80 km south of Brisbane. This 2-acre site, which is surrounded by mountains, will protect the telescope from urban radio interference.

The radio telescope was a prototype designed for the Australia Telescope Array, which is also run by CSIRO. It has not been used for several years, and will have to be refurbished before it can be utilized by SETI. This instrument is predicted to become an essential tool for Project Argus, a SETI operation which searches for intelligent life signals in space. The project plans to eventually employ 5000 smaller, amateur radio telescopes worldwide.

Project Argus' current instruments can detect radio signals as far away as 200 light years. Yet, the point of the project is also to receive communication. The larger telescope will verify any signals that the stations receive. Prior to attaining this telescope, the group did not have equipment powerful enough to provide this verification.

The applications for electronic technology are virtually without boundaries. In addition to the acquisition and interpretation of the signals being investigated in this process, SETI scientists utilize microwave measurements to search for other life forms.

For more information, contact The SETI League, Inc., 433 Liberty St., P.O. Box 555, Little Ferry, NJ 07643, (201) 641-1770; fax (201) 641-1771; e-mail: www.setileague.com.—**NK**

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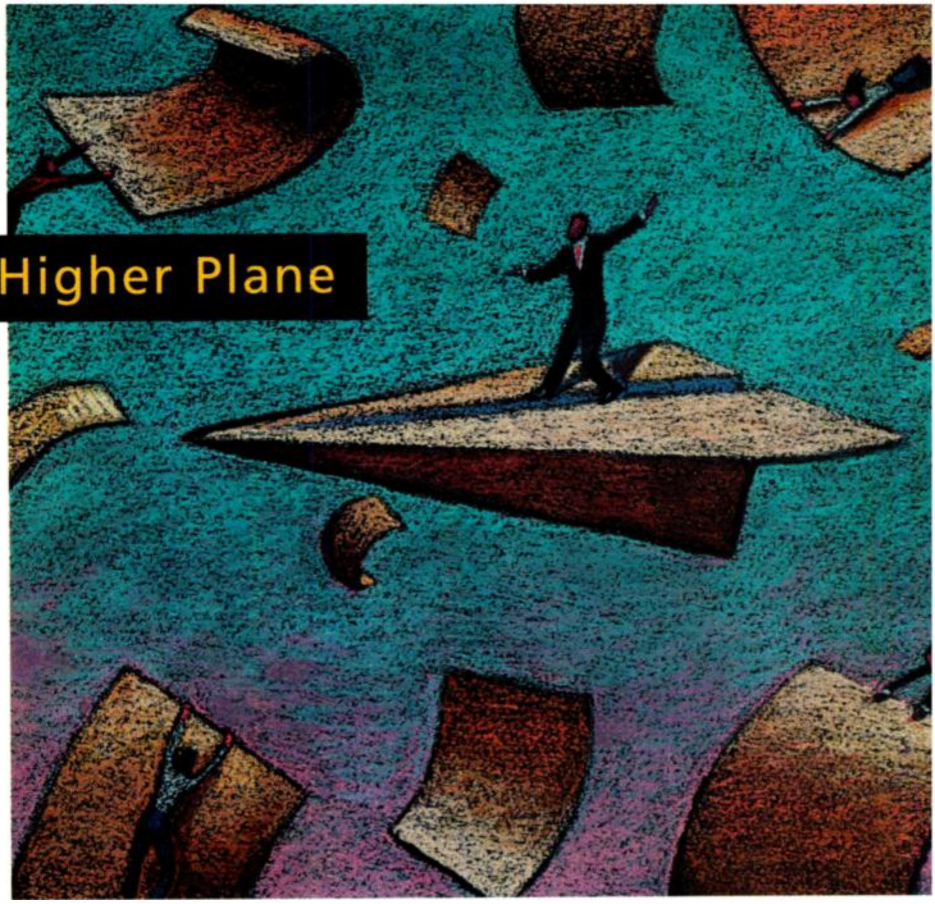

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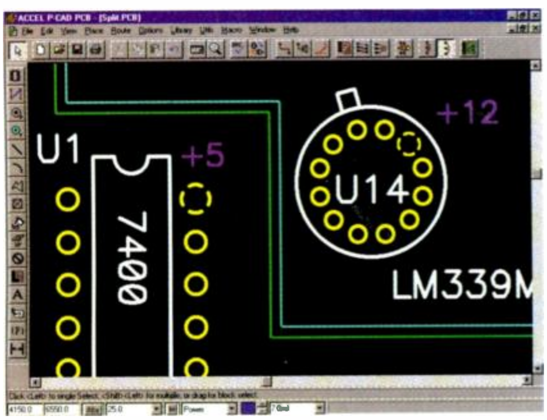

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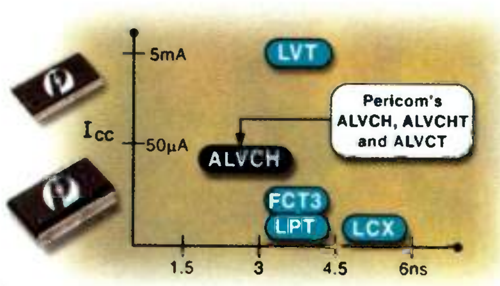

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Electronic Design Automation Mainstreams MEMS Design

A New Generation Of Tools For MEMS Structures Opens Endless Possibilities For Future Designs.

JEAN-MICHEL KARAM, MEMSCAP, 155-157 Cours Berriat, Grenoble, Cedex, France 38028; +33 4 76 70 93 70; fax +33 4 76 48 93 38; e-mail: Jean-Michel.Karam@imag.fr.

The use of microelectromechanical systems (MEMS) has stirred up a great deal of interest in many markets. Just how important is MEMS technology? According to Gordon Moore, chairman emeritus of Intel Inc., Santa Clara, Calif., "MEMS is a really intriguing technology, and I believe it will have a significant impact in the next century." In fact, many engineers believe that MEMS devices will have as profound an effect on our everyday lives in the next decade as the microchip had in the previous one. Design teams at Xerox, Webster, New York; Texas Instruments, Dallas, Tex.; and many small start-ups are already researching potential applications that range from rudderless aircraft to buildings that self-adjust during an earthquake.

MEMS are tiny mechanical systems—sensors, motors, nozzles, valves, and others—that fit onto the surface of computer chips. They're created using the same semiconductor technology as ICs. For example, to create a MEMS pressure transducer, most of the surface material in a defined area of a silicon wafer is etched away. The result is a transparent diaphragm that can be as thin as a single micron. Resistors are then embedded into the surface of this diaphragm and used to translate the slightest movement of the membrane into a voltage.

Although this all sounds pretty futuristic, don't dismiss MEMS as a "blue-sky" technology. Engineering teams see the technology becoming more mainstream and highly applicable for enhancing today's consumer electronics equipment *(see "MEMS Hits The Big Time," p. 70)*. In fact, any device that requires motion sensitivity is a candidate for MEMS, including computer mice, camcorders, and virtual-reality headsets.

Challenges Of MEMS

The increasing attention paid to applications, coupled with the technology's cost effectiveness has brought about rapid progress in MEMS. But for all the benefits it offers, there are still formidable hurdles that need to be addressed before it can become truly mainstreamed.

One major obstacle is the lack of a smooth communications link between the mechanical and electronic worlds. Engineering teams charged with the design of integrated microelectromechanical systems are particularly conscious of this gap, and, in many cases, are still constrained by an "over-the-wall" approach to integration. Typically, each group within the team handles only the tools traditionally associated with its single discipline, throwing the project over the wall to the next group when its portion of the design is completed. With no common interface, such a separatist approach can result in catastrophe when prototype testing reveals a design flaw requiring additional iterations. One group may fix the error, but what will the repercussions be on the rest of the design, and who will fix them?

For example, none of the information derived from using 3D field solvers on MEMS structures information can be automatically transferred to an IC design tool. Microsystems engineers painstakingly identify material properties and boundary conditions to build a mesh so that the field solver can run a 3D finite-element analysis. The tool then predicts the amount of stress and strain in the structures, structural movement, or any other possible effects. But the information is useless without a means to incorporate the data into an electronic design format that other tools can exploit.

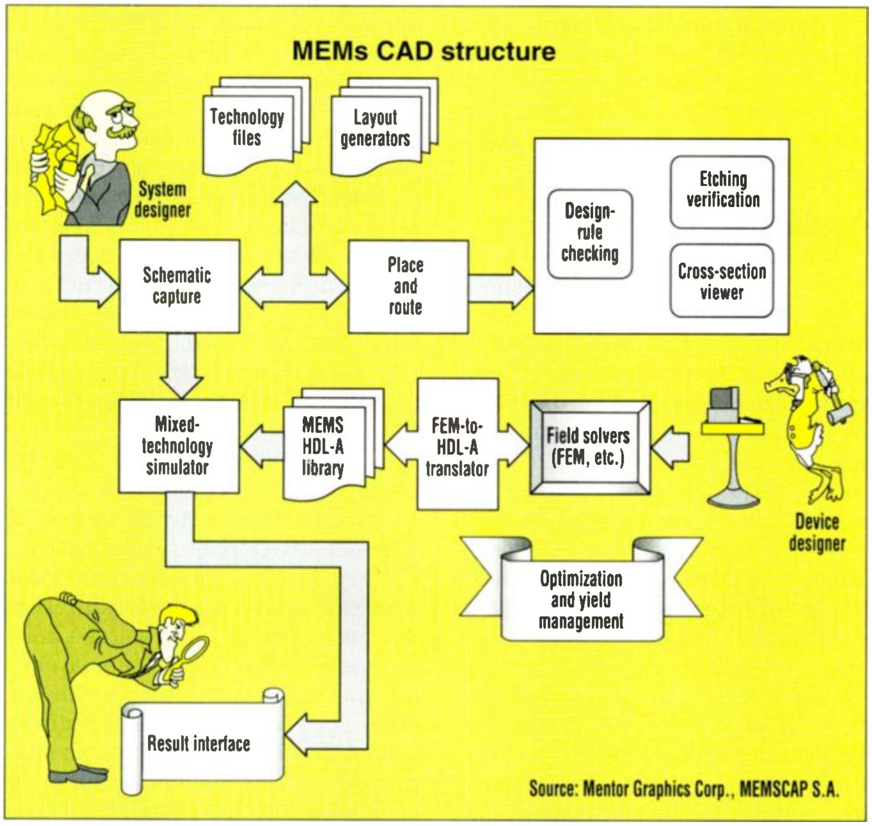
The urgency of developing a completely integrated solution for MEMS design can be demonstrated by looking at automotive airbag system designs. Clearly the airbag design team must consist of engineers across different disciplines. One group requires a finite element method (FEM) simulator to design the MEMS device, while another needs an electrical simulator to design the circuitry. Without an integrated approach, each group must spend precious days just translating data from the other group, a task that adds no value to the design, and that almost inevitably introduces errors into the process.

A secondary hurdle is enabling engineering teams to make full use of pre-existing intellectual property (IP) in MEMS design. The ability to smoothly integrate cores into a system-on-silicon architecture provides designers with both the latest functionality and a major productivity gain that can catapult the product to market months ahead of the competition. Until now, designers had to create MEMS by pushing polygons, and understanding the fine details about the target fabrication process. Obviously, this approach demanded exceptional engineering skills, and expanded design schedules and budgets.

To bring MEMS into the mainstream, it is absolutely essential that the difficulties surrounding MEMS design be minimized. One thing is certain: If electronics engineers can use MEMS devices in their system design, without excessive complexity, then market growth will be significantly intensified. And, the potential of that market growth is enormous. According to research from Ernst & Young Entrepreneurs Conseil, Paris, France, in 1996, the MEMS market was $12 billion for devices and $34 billion for systems. The same firm estimates that by the year 2002, the market will have grown to $34 billion for devices and $96 billion for systems.

Next-Generation MEMS CAD

A market with this kind of growth potential justifies the development of new approaches and tools for MEMS design. A new generation of design tools that combine aspects of electronic design automation (EDA) with the mechanical, thermal, and fluidic computer-aided design (CAD), is needed. The development of an integrated EDA/CAD solution for MEMS structures, offering a continuous top-to-bottom design flow, would bring the benefits of MEMS to the entire design industry. Specialists and non-specialists across different disciplines will then be able to leverage a common design language, as well as design reuse, as they work toward the realization of sophisticated miniature systems, at costs much lower than previously thought possible.



1. The key to successful implementation of EDA for MEMS design is the integration of the system engineer's flow and the component engineer's flow. The system designer is responsible for schematic capture, simulation, layout, and post-layout (including design-rule checking, etching verification, and cross-section viewing). The component engineer provides finite elements modeling (FEM), which may be translated to an analog HDL model to enable validation of full system functionality, and libraries at different levels that are coupled to the schematic driven layout feature. Enabling these multidisciplinary teams to work together—instead of using the "over-the-wall approach"—will help bring MEMS design to the mainstream.

Dr. Dirk Beernaert, principal scientific officer of the Brussels-based European Commission responsible for microsystems in the ESPRIT research and development program, sums up the challenges facing the industry today. "What's needed is not only the combination of the different disciplines required to create a microsystem, but also a full-system-oriented approach, so that MEMS design can be a true subsystem within the overall design. The use of the right design methodology will greatly enhance reusability and efficiency while reducing cost and risk—still considered the main barriers to wider introduction of these technologies in many applications."

In developing the best computer-aided design environment for MEMS, engineering teams will require a number of capabilities. High on the list is the ability to create both monolithic (single-chip) and hybrid (multichip, multitechnology) MEMS designs. Hybrid design has been around for some time, and such environments are readily available. The monolithic approach, however, aims for nothing short of complete cofabrication of electronic and non-electronic functions. To this end, existing microelectronics lines are being extended and adapted to allow MEMS production.

This monolithic environment must allow a continuous design flow that provides benefits for both the non-specialized system-level designer, as well as the device designer. The system level designer needs an architectural-level view to create a new MEMS system from at least two different technology areas; micromechanical and electronic. The device designer, on the other hand, possessing expertise in his technology area, needs a vehicle to pass on his or her knowledge.

The environment must enable the device designer to design modules; simulate them; and pass on the knowledge in the form of characterized, standard-cell libraries. The system-level designer can then take advantage of the multilevel information contained in those libraries, such as layout information, behavioral models, and FEM

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models. By assembling the desired cells, the designer can create and simulate a system-level design. The resulting system is then handed over to the back-end team for chip-level design work. Once final layout is produced, both the system- and device-level engineers can review the features of the MEMS design.

The proliferation of MEMS products and potential applications has inspired the EDA industry to smooth the bumps posed by the integration of the electronic and mechanical worlds. Coupling mechanical and other solutions, such as electrostatic and thermal simulation, has been a particular problem. Some companies have achieved a measure of success in addressing this problem by using point tools on an ad hoc basis, such as those from Ansys, Canonsburg, Pa.

In an effort to bring MEMS out of the research arena and into mainstream design, the U.S. Pentagon's Defense Advanced Research Projects Agency (DARPA) has been actively

MEMS Hits The Big Time

It's a fact that microelectromechanical systems are now becoming a part of mainstream design practices. The technique has already opened up new vistas for automotive designers. Now, car makers can provide consumers with "smarter," improved safety features including airbag systems, intelligent highway equipment, self-adjusting comfort mechanisms, and better fuel and aerodynamics monitors.

And, the industry is now at work applying MEMS to solve a problem recently brought into the public spotlight: how to reduce the risk of airbag injury, especially for children. Design teams at Delphi Delco Electronics Systems, Kokomo, Ind., are working on combinations of MEMS-based sensors that can tailor the response of the restraint system by modifying the airbag inflation rate. Factors that affect the inflation rate are a passenger's weight and position, and crash severity.

David Rich, sensor designer at Delphi Delco Electronics Systems, says that while the core of his MEMS design organization has been pressure sensors and accelerometers for airbag deployment, the company is developing MEMS products for new applications that will enhance vehicle control and reduce emissions.

For example, the company designs chassis control systems based on a combination of accelerometers and angular rate sensors. Achieving improved chassis control requires the development of 1- to 2-G accelerometers and angular rate sensors that can pick up angular rates of less than 1°/s. When the angular rate and steering are out of control, the system applies differential braking before the vehicle begins to spin. While low-G technology and angular rate sensors are already in production at several companies, the products come at a premium. Delphi Delco Electronic Systems believes that development of micromachined sensors will drastically reduce costs, paying off on a large scale.

The company also expects MEMS to help new mass airflow devices improve control over the fuel mixture, helping auto manufacturers to comply with stricter emissions standards. Currently manufacturers use manifold air pressure sensors or hot-wired animometers, but these solutions are only unidirectional. Small, four-cylinder engines in European vehicles require bidirectional mass-airflow devices that function when all four valves are closed, creating a reverse flow. MEMS offer that bidirectionality in a cost-effective form factor.

It is this lower cost, along with delivering enhanced functionality and performance, that makes MEMS so alluring. The electronics industry is now at the point where easier and cost-effective design of MEMS-based products makes mass production an attractive proposition. The critical motion detector in the airbag circuitry, for example, is a MEMS sensor in silicon. It is inexpensive, yet delivers superior performance to the mechanical sensor it replaces that costs twice as much.

All this interest in MEMS is not limited to just the automotive market. MEMS is also emerging as a viable technology in other areas that include medical applications such as blood-pressure kits and chemical analysis equipment. A MEMS-based system is also at the heart of a new projection television system by Texas Instruments, Dallas, Texas, that delivers a far superior picture compared to the competition. And, sophisticated projection systems from companies like In Focus Systems, San Jose, Calif., incorporate MEMS devices to create a sharp, clear display.

"MEMS technology is starting to branch out into disparate applications," says Karen W. Markus, director of the MEMS Technology Applications Center at MCNC, Research Triangle Park, N.C., a non-profit technology resource center for business and government. "The early application areas of accelerometers have expanded to include many aspects of inertial systems, from stabilization systems for missile and aircraft navigation and head-mounted displays, to mice for your 10-year-old's computer game."

Markus believes that after inertial systems, the two hottest markets are optical systems and RF devices. As she explains, "MEMS has the potential to significantly affect the ability of RF systems to provide higher capability in a smaller package, and will include everything from actively tunable systems to low-noise switches. The field of MEMS is extremely exciting right now. We seem to be limited only by our imaginations and our ability to ramp-up manufacturing."

Already a respectable size, the MEMS market will undoubtedly grow as it spills over into other arenas in the very near future. Look for MEMS devices to first replace expensive, bulky electromechanical technologies. Entirely new areas previously restricted to electromechanical sensors are then expected to develop due to MEMS' size and low cost.

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promoting the development of a composite CAD program for MEMS. To help jump-start the EDA development in this area, this program funds on-chip MEMS design.

This focus by DARPA has already helped stimulate progress in the EDA sector. Several companies now offer MEMS design-tool support. For example, Mentor Graphics, Wilsonville, Ore., in partnership with MEMSCAP, Grenoble, France—a spin-off of Grenoble-based Circuits Multi-Projects (CMP), and an affiliate of the French TIMA research institute—has recently announced a set of MEMS Engineering Kits *(Fig. 1)*. In addition, Mentor Graphics and MEMSCAP, together with MCNC, Research Triangle Park, N.C., were recently awarded a grant from DARPA for the development of an MCNC foundry-specific engineering kit.

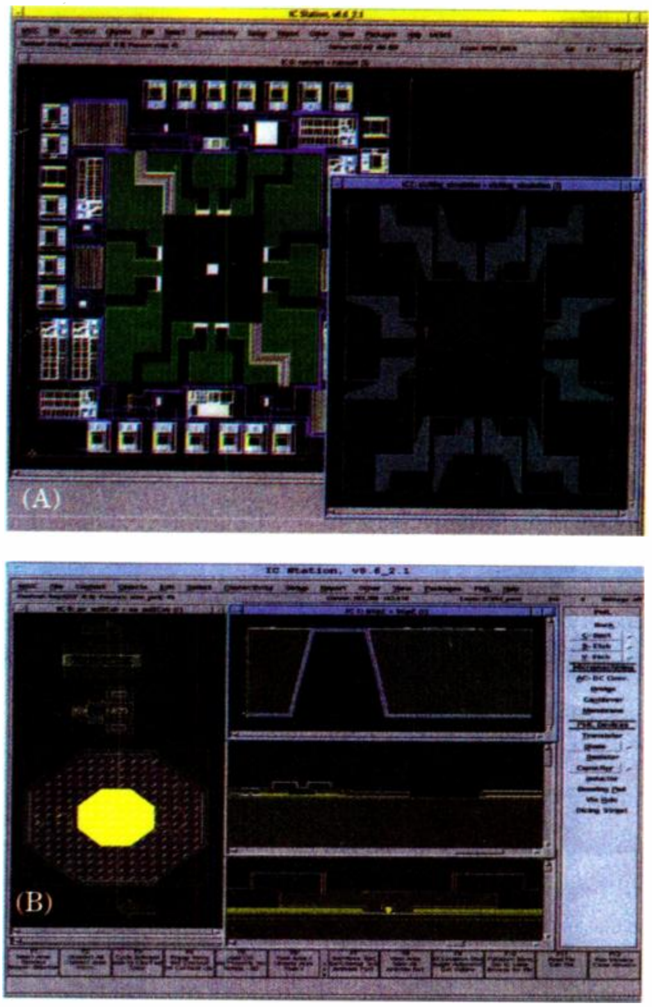
There are several key features a designer should look for when choosing a design kit. First, it must include the basics. Parameterization from behavioral models all the way down to layout generation is an absolute must. The kit should support bulk micromachined structures such as infrared sensors, piezoresistive mechanical devices, and accelerometers, as well as surface-micromachined elements such as capacitive sensors and electrostatic actuators. Both monolithic MEMS design and hybrid design on-chip with analog and digital circuitry should be supported. Furthermore, schematic entry must be complemented with access to analog behavioral modeling and layout generation for structures ranging from bridges and cantilevers, to infrared sensors and accelerometers, etching simulation, cross-sectional viewing, and extended design rules for MEMS layout *(Fig. 2)*. Interfaces to finite-element solvers are necessary to evaluate the 3D models created in the design process.

Another essential requirement is a continuous design flow from front- to back-end. By seamlessly combining the electromechanical and IC design environments, the kit will eliminate the confusion and inefficiency of going back and forth between the two. As a result, a MEMS design can flow seamlessly from structural model to layout, with multidisciplinary teams including mechanical, electrical, component, and system teams, working together in the same environment and directly sharing results. And, if there are interfaces to specific foundries, a fast track from design to market is almost a sure bet. The Mentor-MEMSCAP kits, for example, will support several foundries including MCNC; Bosch, Reutlingen, Germany; Austria Mikro Systems, Graz, Austria; and SensoNor, Horton, Norway.

"One of the biggest limitations to continued growth of the MEMS user base is the fact that with existing design systems you have to be a rectangle-pusher." At least that's how Karen W. Markus, director of the MEMS technology Applications Center at MCNC sees it. She continues, "The limited tools that are available to help a MEMS designer require that person to have at least a basic idea of CAD layout and the process being used."

Markus contends that a vast, untapped market exists in systems designers, people who think in terms of black boxes that capture all the behavioral and intrinsic information. "The engineering design kits currently under development by MCNC and its partners will provide these black boxes and the supporting design framework to the systems design community, opening the door for their participation in MEMS foundry activities. This has the potential to spark an additional level of interest and product introduction beyond the current frenzy," says Markus.

To move MEMS up the design chain, support for design IP is necessary. This is especially important for designers new to MEMS. Intellectual property provides more general-purpose ready-made pieces to help jump-start the design. As a result, instead of laboriously creating a device by pushing polygons, the designer can use MEMS IP to significantly streamline the design effort. This makes it easier for those new to this type of design to efficiently produce a viable MEMS application.



2. Using a design kit within Mentor Graphics' IC Station, etching verification is integrated within the EDA environment (a). The user can select a specific region from the layout or the whole layout for the etching simulation. In this case, the simulator is applied on a complete MEMS device that includes electronics next to the multibeam membrane. The result is displayed in a new window. The green region in the new window is the etched area. This design kit cross-section viewer has generic functionality (b). It can provide views of integrated electronics, bulk micromachined devices, and surface micromachined devices. It also provides views for any technology, including silicon and gallium-arsenide. In the cross-section viewer pictured here, the user can select a cut line from any angle, whether vertical, horizontal, 45°, 30°, etc.

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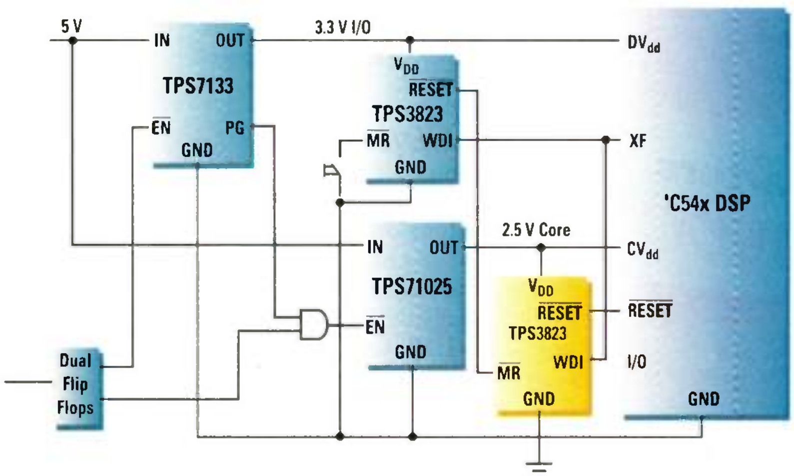

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The designer can still zero in on crucial areas at the device level, and work with field solvers. However, once the designer is satisfied, lower-level information can be automatically translated into an analog HDL, and integrated with other IP at the system level.

Dr. Beernaert of the European Commission emphasizes the pressing need for reusability, "Currently, every new MEMS application is a new process, a new device design that starts from scratch. This is very inefficient, very expensive, and is asking for mistakes to be made. Having interfaces in the form of IP to specific foundries, and qualified, debugged MEMS building blocks will be critical for faster development times, and for increasing the chances of immediate success."

MEMS: On The Verge

With the ability to support any combination of electrical and micromechanical devices on a single chip, MEMS opens an endless horizon of tantalizing possibilities for future designs. But to fully mine the staggering potential of MEMS tomorrow, design tools and methodologies must be devised today that support that vision. With the combined effort of DARPA and the EDA industry focusing on MEMS, significant effort has already made in that direction. Such progress ensures that the tremendous promise that MEMS holds for next-generation IC-based applications will, in fact, become a reality.

Jean-Michel Karam is president and CEO of MEMCAP. From 1994 through 1997, he led the Microsystems Group of TIMA Laboratory and the Microsystems and Multi-Chip-Module Manufacturing Programs of CMP (Circuits Multi-Projets) Service. He received PhD in microelectronics from the Institut National Polytechnique de Grenoble in 1996, an Advanced Studies degree (DEA) in microelectronics from the University of Paris VII, and his engineering degree from the Ecole Supérieure d'Ingénieurs en Electrotechnique et Electronique (Paris, France) in 1993. He received a degree in Mathématiques Supérieures et Spéciales from the Ecole Supérieure d'Ingénieurs of Beirut, Lebanon, in 1989.

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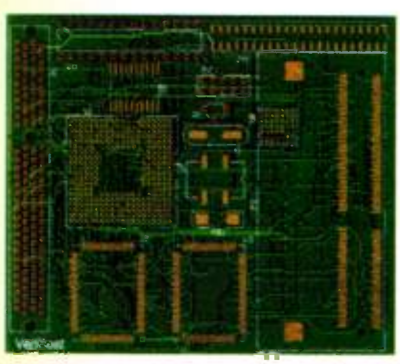

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EDA WATCH

Emerging Design Tools Promise To Move MEMS Into Mainstream Applications

The EDA industry has experienced great changes in the last few years: shrinking design geometries, faster components, and improved tool performance and interoperability, to name just a few. EDA has gone from the unsung hero of the electronics industry—always behind the scenes doing the grunt work but getting little credit—to an enabling technology that will enhance the growth of many new technologies. The microelectromechanical systems (MEMS) industry is already feeling the effects of design automation, and may turn out to be the EDA industry's most revolutionary market.

MEMS devices have been around for many years—in cars, toll booths, and medical devices, as well as security and environmental detection systems. According to a recent study, the market for MEMS devices amounted to $12 billion in 1996. By all accounts, the market is expected to grow at an astounding rate, to $34 billion in 2001. The primary driving force, which is the widespread use of MEMS components in systems design, will need an enabling technology in order to meet this growth rate. EDA will be that technology, helping to eliminate problems caused by increasing design complexity and the desire to move MEMS into mainstream systems.

MEMS devices are becoming increasingly complex. They are pushing the limits of available design tools, and quickly growing beyond what designers can analyze or design without MEMS-specific software design tools (MDTs). Compounding the problem is the fact that very complex devices typically have unacceptably long design cycles. Examples are the multi-axis accelerometers and gyro devices now under development. It can take more than a year to move such a device from a functioning prototype into production. In an industry driven by time-to-market pressures, that's unacceptable.

Complexity is not the only problem, however. Lack of available foundries and resources for MEMS development make it difficult to use the technology in systems design. In fact, until now, including a MEMS device in a system meant hiring and training a staff of engineers, establishing in-house manufacturing capabilities, and coming up with usable design tools—either by developing them in-house or building interfaces to existing point tools. Most companies don't have the time or resources to invest in such a commitment.

But, as foundries become available and MDTs emerge, engineers will be able to use MEMS in a much wider array of applications. Ultimately, this will create the ability to plug and play MEMS into a variety of systems, and dramatically boost the proliferation of MEMS devices into more mainstream applications.

New Tools Needed

Developing design tools targeted at MEMS is much more difficult than it sounds. For one thing, designing MEMS requires the modeling and simulation of a broad set of physics and coupled-physics domains. As Michael Jamiolkowski, president of Microcosm Technologies Inc., Raleigh, N.C., explains, "There is such a variety of different device technologies involved, such as electro-mechanical, thermal, piezoresistive, piezoelectric, magnetic, and fluid flow. Common devices being designed today include accelerometers, micro-gyroscopes, pressure sensors, valves, pumps, micromirrors, micropositioning systems, micro-data-storage devices, and microchemical analyzers." Tools, therefore, may have unique device, packaging, and system design requirements.

MDTs must even take the process into account. IC designers can be reasonably sure of getting good results if their chips both follow a foundry's design rules for layout and function correctly when simulated with the foundry's Spice parameters. The same is not yet true for MEMS designs.

Darrell Teegarden, principal engineer at Analogy Inc., Beaverton, Ore., notes, "Design tools must incorporate information that reaches all the way down into the process. Even crucial material properties are process-dependent. The functional equivalent of foundry-model parameters does not yet exist."

The effective use of standard cells or synthesis for MEMS is even farther into the future, according to Teegarden. "The notion of MEMS IP (intellectual property or reusable fragments of MEMS structures) will not be practical for several years, because the processes are not sufficiently interchangeable to make useful design fragments 'portable' across processes.."

Ultimately, frequent changes to the process, customizing the process to produce real products, and the lack of process standardization force MDTs to transcend a wide range of functionality. Yet, the MDTs must also provide a close integration of both EDA and MDA (mechanical design automation) tools.

Make no mistake, however. Despite the magnitude of these and other hurdles to the adoption of MEMS as a mainstream technology, CAE/CAD for MEMS is an inevitability. MEMS technology offers too many unique benefits not to be included in future system designs. The only questions remaining are what the new MDTs will look like, and what designers should look for when contemplating a tool purchase.

In general, MDTs will have to handle device- and system-level design and modeling, manufacturing design, and package design. But, these tools will also need to provide specialized solutions for a variety of applications.

MDTs must interface with the appropriate MDA tools, since the MEMS design process involves both mechanical and electrical components. As Jamiolkowski explains, "Layout, process descriptions, and tools from EDA will be inputs for building 3D MEMS device models using solid-modeling and mesh-generation tools from MDA. Partial-differential-equation solvers from both EDA and MDA will help extract reduced-order system and package models. System and package models will then go into EDA-based tools like Spice to simulate the behavior of large systems containing MEMS."

Another requirement for MEMS design tools will be the integration of physical design tools and system-level modeling tools. The physical design tools will incorporate pertinent process information and multiple energy domains, providing simultaneous 3D simulation of things like mechanical structures, electrostatic and electromagnetic fields, fluid dynamics, and heat transfer.

Jean Michel Karam, president and CEO of MEMSCAP, Grenoble, France, adds that for the emerging MDTs to be successful, "the user will must be able to use them to perform full system functionality verification. This means the ability to pass from layout to solid model, which necessitates a characterized component library (IP), both at system level and layout level, that has been targeted to a given technology or foundry where the material parameters are known."

Helping to move the process of MDT development along will be the advent of standard modeling languages, like IEEE 1076.1 VHDL-AMS, the analog/mixed-signal version of VHDL. This will provide model interchangeability, while allowing designers already familiar with VHDL an easier entry into MEMS design. Calibrated foundries will speed the acceptance of these tools by creating stable processes that will provide designers with predictable results.

Once developed, widespread adoption of MEMS design tools will be driven, in part, by the competitive advantage they provide. Existing MEMS design solutions often involve licensing, support, and prototype costs. Furthermore, using and integrating these tools is not easy, and typically requires many hours of development and training, on top of design efforts. But, the newly emerging tools will allow designers to work more quickly, as well as afford an opportunity to explore and optimize design ideas. In the long run, this means lower costs. The end result will be a win-win situation for the designer and the end user.

For more information on MEMS-based EDA tools, visit ELECTRONIC DESIGN's web site at www.elecdesign.com. Refer to the Table of Contents.

Sources For MEMS Research And Design Tools

Analogy Inc.
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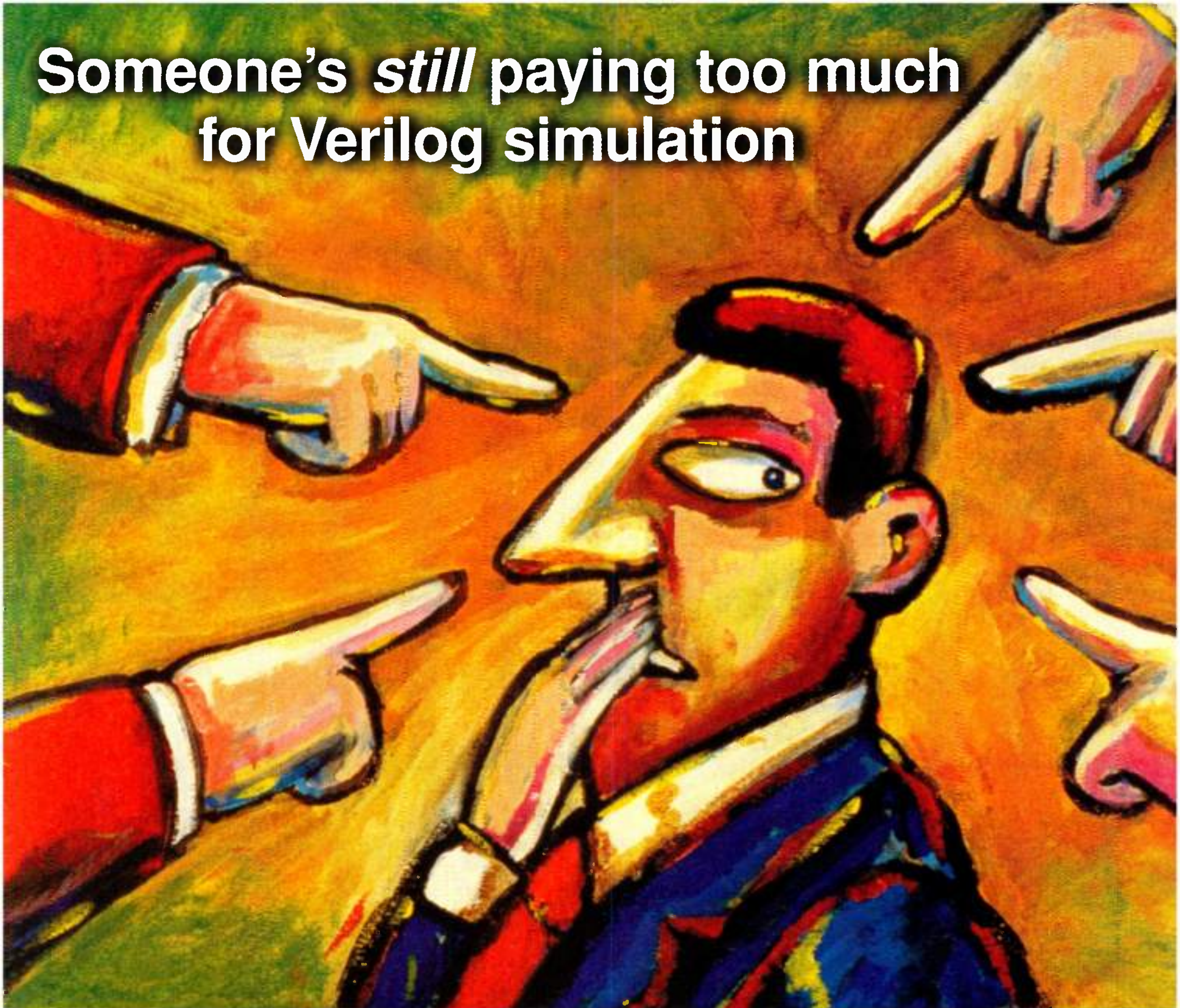

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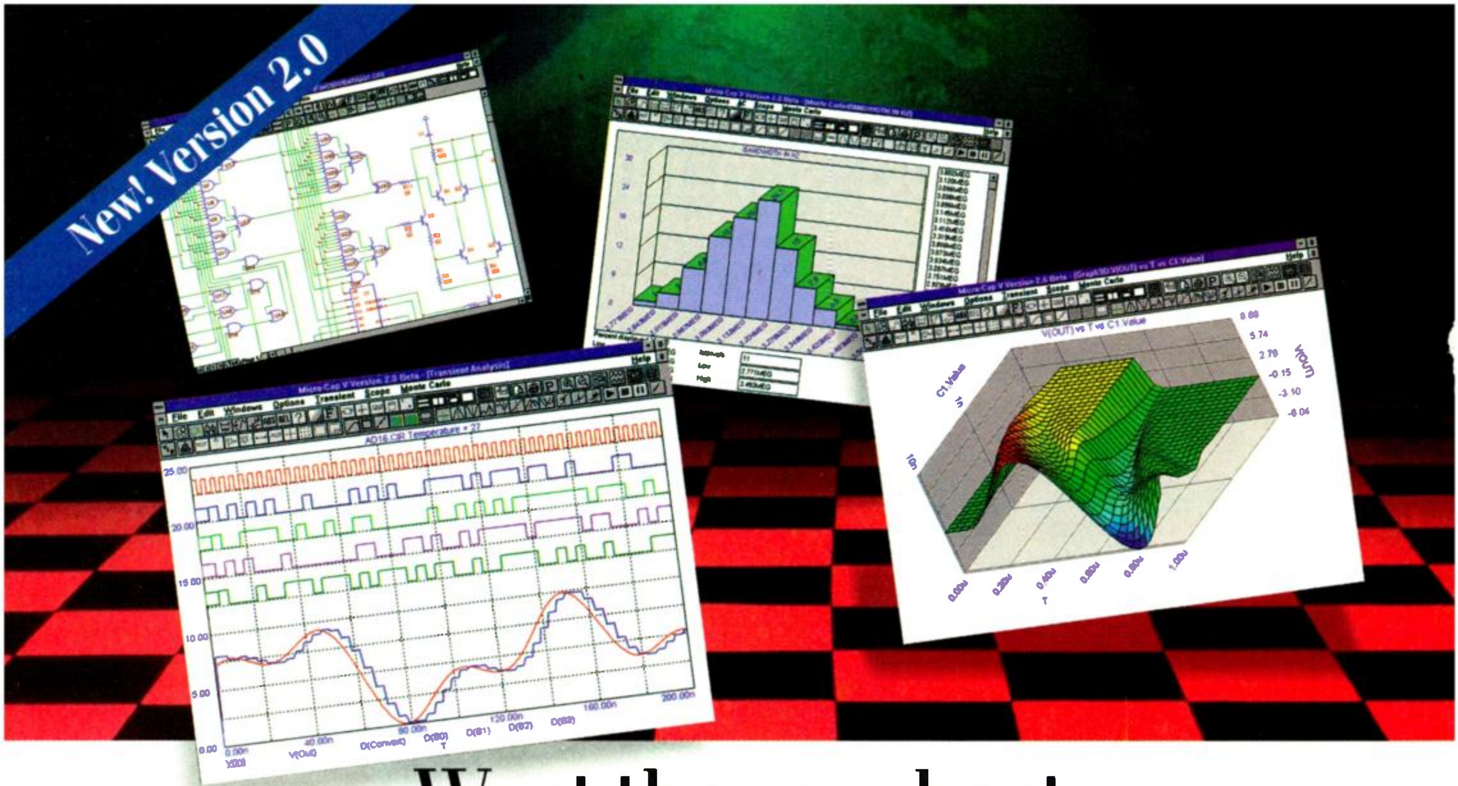

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Convert Asynchronous Designs To Synchronous Equivalents

Practice Good Digital Design Techniques To Reap The Benefits Offered By Synchronous Logic.

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The advent of programmable logic has given designers nearly infinite flexibility in implementing digital logic designs. However, with the flexibility afforded by these devices, some common design practices may get overlooked. Often, the speed in which today's tools can take a design from specification to implementation leads to numerous trial-and-error attempts to get the design to work. In haste, engineers might end up with a design that contains asynchronous circuits in places where synchronous circuits could be used. Because flexible parts are used to implement the logic, the designs easily fit to the parts with the asynchronous logic intact.

This article will discuss the advantages of synchronous circuits over asynchronous circuits, and will also present common rules for designing good synchronous circuits. Lastly, we'll look at some circuits that contain asynchronous behavior and provide better synchronous alternatives.

If there were but one rule to follow in digital design it would be to make the design completely synchronous. Using registers that are clocked by a single common clock leads to the best overall system designs for a variety of reasons.

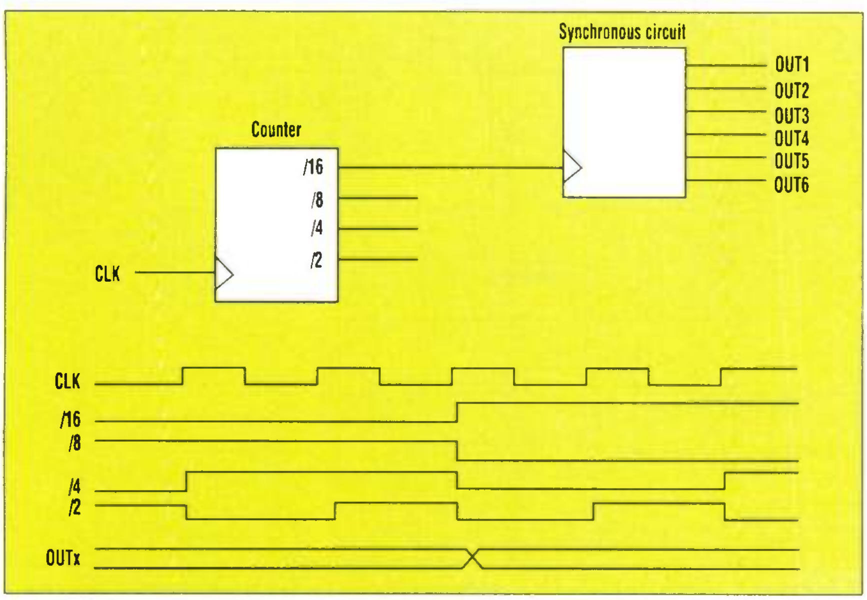
First of all, synchronous designs are more reliable. They are deterministic in their behavior, due to the fact that all signals are sampled at a well-defined time interval. Synchronous designs rely on very few timing parameters to guarantee operation, namely, the maximum frequency of operation of a device (f_{max}), the register setup and hold times (t_{SU} and t_H), and the register clock-to-output time (t_{CO}). Meeting these parameters ensures designs will work under temperature, voltage, and process variations.

Synchronous designs are also portable. In all PLDs and ASICs, the master clock, or clocks, are routed via a low-skew clock network. These networks ensure that a design done in one PLD architecture will be compatible with a different architecture, with good results. Synchronous designs take advantage of this trait.

In addition, synchronous designs can be tested more easily and run statically, with the clock input driven by a test signal. They can be made virtually immune to noise. Therefore, finding errors in a design will not be a cross between identifying logic errors and tracking down noise-induced errors.

Synchronous designs attain performance levels easily. The maximum operational frequency of a synchronous design can be determined from the data sheet for many PLDs. Determining maximum performance of circuits that include asynchronous clocking events is much more complicated.

Finally, synchronous designs are easier to code in a hardware description language (HDL), and are also easier to



1. Typical of a design practice commonly used, this asynchronous circuit uses the output of a counter as a clock input to a synchronous logic circuit.

read. Designs built around a common clock yield compact, efficient code. On the other hand, designs with numerous clocks and asynchronous behavior are more difficult to understand. Their code descriptions can also get cumbersome.

Synchronous Rules To Live By

All inputs to a synchronous circuit need to be synchronous. If an asynchronous input to a synchronous circuit violates the t_{SU} or t_H of the registers, some of the registers may resolve the input as a logic 1, while others resolve it to logic 0. The classic way to synchronize asynchronous signals is to drive the signal through two cascaded D flip-flops.

Most PLD architectures guarantee a very high mean time between failure (MTBF) with this type of circuit, up to the f_{max} specification on the device data sheet. The MTBF, in this sense, is a statistical value that measures how often, on average, the second register in the synchronizer will receive an input that is not yet resolved by the first register. For example, the Cypress Flash370i and Ultra37000 families of CPLDs guarantee a 10-year MTBF for this type of circuit. This circuit is designed into the input macrocells of the device. Thus, the output of the second register will provide a signal that is synchronous to the rest of the logic.

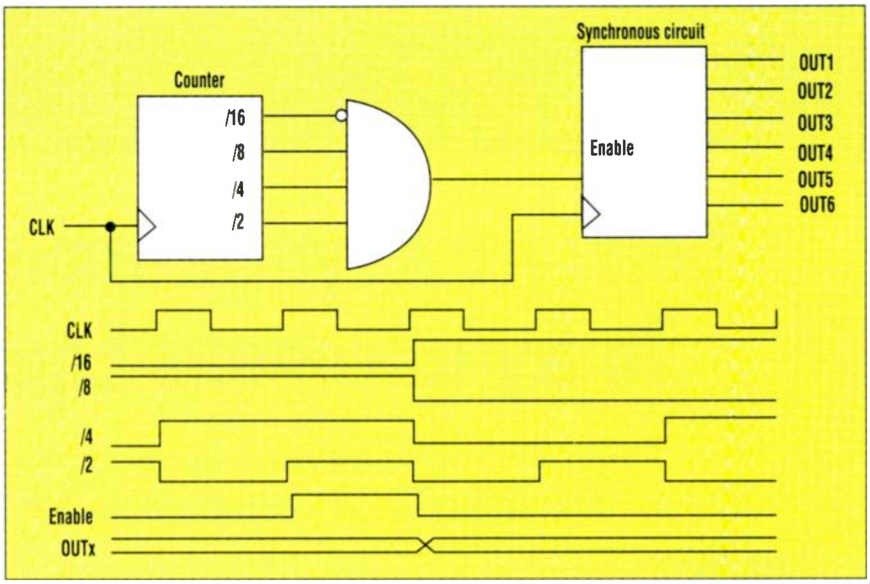
When a design relies on more than a single clock, and information needs to be transferred from one clock domain into the other, the interaction must be treated as an asynchronous event—unless there's a known phase and frequency relationship between the clock domains. If many signals need to be transferred, a single synchronized handshake signal from the source-clock domain to the receiving domain should be used. When the handshake signal is received, the remaining signals can be captured from the source side. Those remaining signals should be sent across without synchronization. This guarantees that they have enough settling time to meet the t_{SU} for the clock in the other domain.

Every asynchronous external signal input to a finite state machine (FSM) must be synchronized (with the two flip-flop synchronizer) to the FSM's clock to ensure appropriate behavior. Imagine the chaos that would result if a signal were to be left asynchronous and, while the input was in transition, some of the FSM's state registers detected a logic low while others detected a logic high.

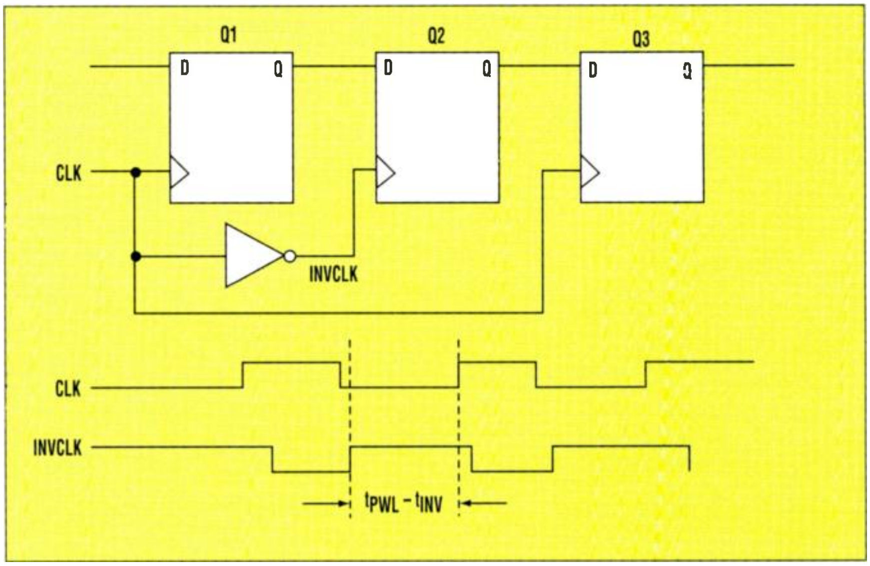
It's just as important to keep outputs from an FSM synchronized. FSM outputs can be used for such functions as counter enables, register enables, and output enables. In any of these cases, the signal integrity is best when kept synchronous with the FSM's clock. This prevents unwanted propagation delays and possible glitches when the FSM transitions between states.

In many cases, engineers insert buffers and inverters in their designs to create an artificial delay. Too often, these delays are used to fix bad design techniques, such as using a register output to drive the clock input of another register. The delay might be put in the clock path to ensure that data arrives at the register before the clock does. The problem with adding delays is that the delay time is always unpredictable. What works today might not work if the design is ported to another device. The temperature differs, the process used for the device changes, the version of the logic synthesizer changes, and so on.

Unfortunately, we often violate the



2. Functionally equivalent to the Figure 1 circuit, this design achieves completely synchronous clocking by using an enable signal in conjunction with a common synchronous clock.



3. To make use of both clock edges in a synchronous circuit, the design engineer must know the circuit's implementation. The propagation delay between the CLK and INVCLK must be accounted for in timing analysis.

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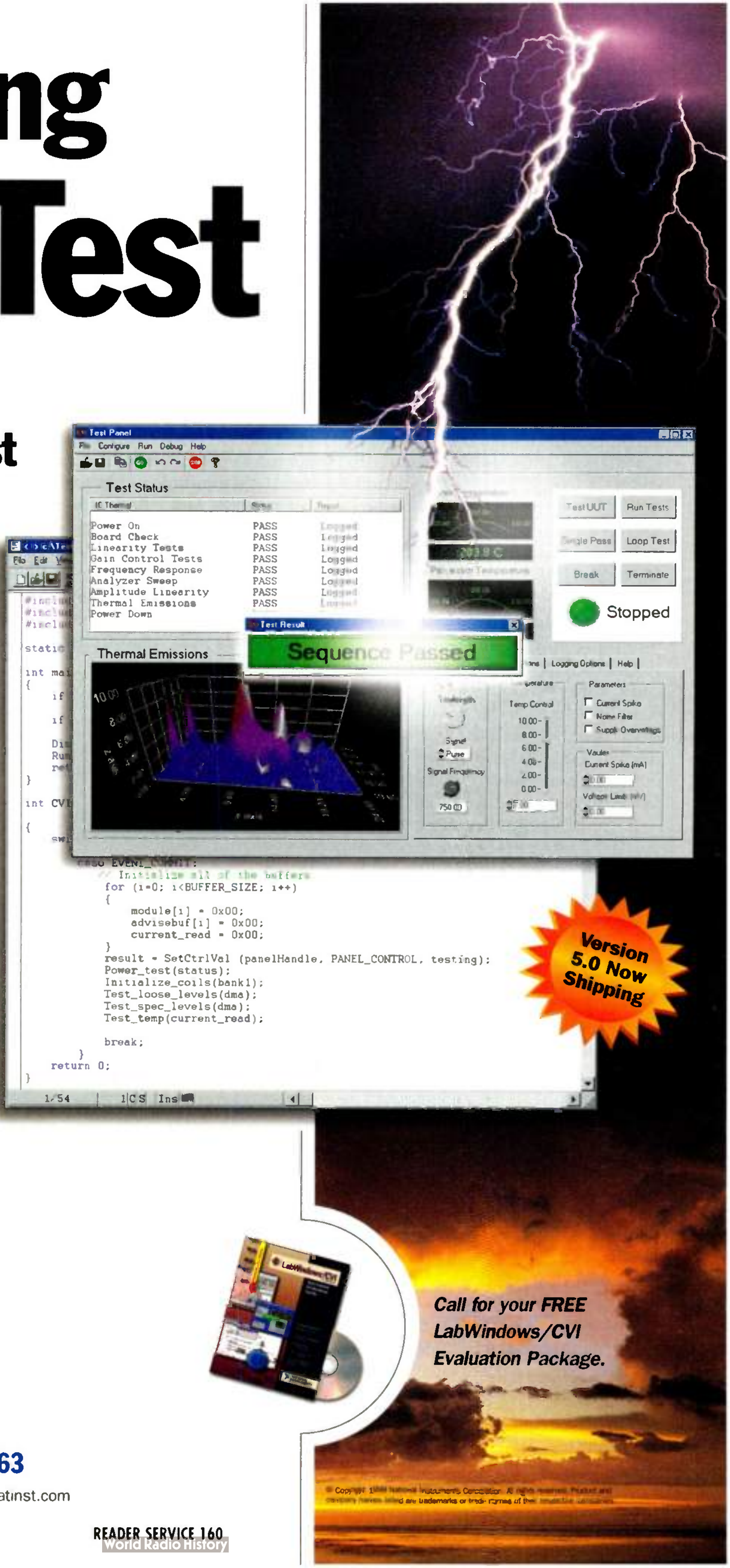

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aforementioned rules when time constraints and old habits overcome us. But, by combining knowledge of the these rules with the following tools for eliminating asynchronous circuits from designs, designers can achieve a high-performance, successful result that will be reliable, portable, and easy to test.

Lower frequency operation is often required in today's designs. Many designers simply take an output of a counter and use it as the clock to another synchronous circuit *(Fig. 1)*. Using the counter output forces internal clocking within a PLD—an external global clock is not the clock source for some registers. Because the counter output is registered, it can be used reliably as a clock to another circuit without the possibility of glitches. However, there are three main problems associated with this type of circuit:

1. The timing of the circuit is more difficult to analyze and the circuit will not run at the device's f_{max}. This is because there's a clock-to-output delay (t_{CO}) from CLK to /16, and another t_{CO} from /16 to OUTx. If the OUTx signals are distributed to logic clocked by CLK, both t_{CO} delays must be accounted for in the calculation of the circuit's f_{max}.

2. The timing problem is exacerbated if a ripple counter is used. For each output of the counter, an additional t_{CO} needs to be added to the timing. In addition, the timing of the internal clocking (often called asynchronous clocks, or product-term clocks) and external global clocking will most likely be different, and require careful analysis.

3. The design may not fit within the target device architecture if internal clocking isn't supported. However, all devices have at least one global clock input that can be driven from a device pin.

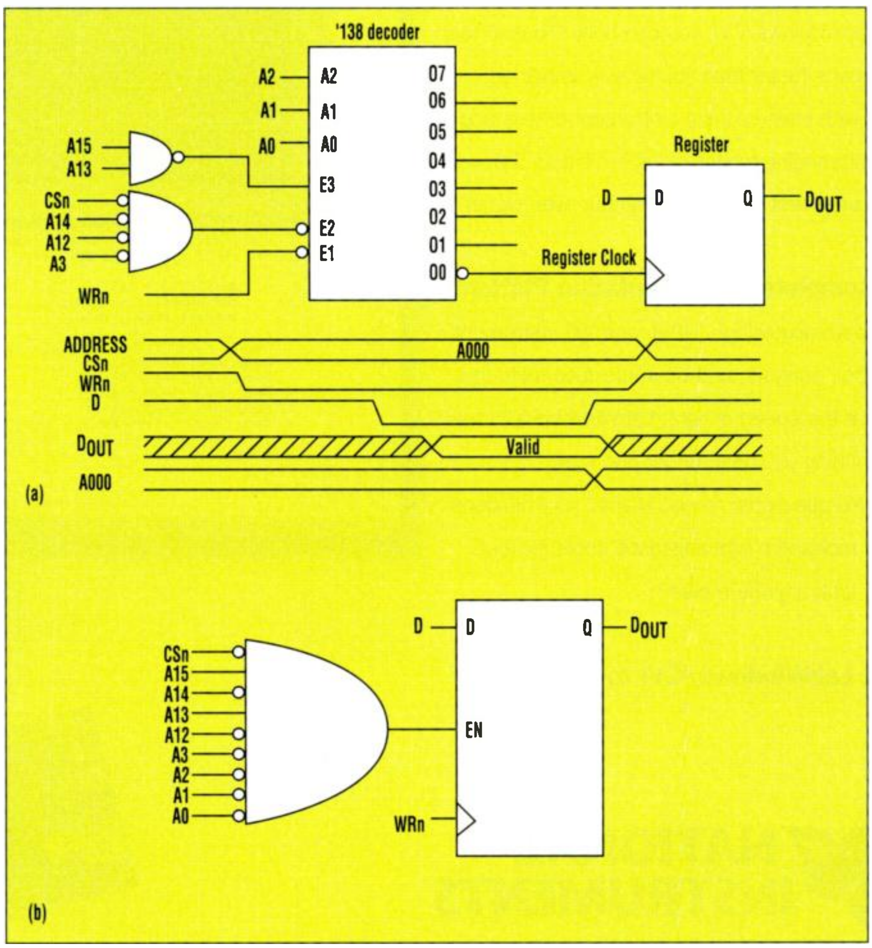
This type of design can be converted to an equivalent circuit that is only dependent on a single clock. Notice that the CLK clock edge, where the counter changes from a value of 7 (0111) to 8 (1000), is ultimately when the OUTx signals are changed as well. Converting from using the /16 counter output as a clock to using the CLK signal as the clock requires that an enable signal be created. This lets the synchronous circuit operate only when the counter is transitioning from 7 to 8 *(Fig. 2)*.

The timing of this circuit is only tied to the transition of CLK. It will easily fit into any device because it uses only one clock, with no internal clocking. In a CPLD with a simple timing model (such as the Cypress Flash370i or Ultra37000 families), the circuit will run at the maximum frequency allowed by the device. In an FPGA or ASIC, the timing is easy to analyze. The enable signal is the only critical path, external to the synchronous circuit, for determining the maximum frequency.

The only issue that designers need to be concerned with is the additional logic required by the enable signal. The implementation of the enable is done with the logic of a 2:1 multiplexer on the D input to a register. The enable is the select line to the multiplexer, which chooses between the two inputs. One input to the multiplexer is the register's output, while the other is the logic to be implemented when the register is enabled. Thus, the register will either retain its prior value on a clock edge, or possibly change to a new value, depending on the logic input.

In a CPLD, the circuitry shown in Figure 2 will require three more inputs to a logic block for the additional counter outputs, an additional input to the logic block for each OUTx, and five product terms for each OUTx (this assumes that a single product term was originally required for a given OUTx's input equation). In a CPLD architecture, where the register can be configured to be a toggle flip-flop rather than a D flip-flop, the product term usage drops to two. However, FPGAs and ASICs have different logic architectures, and the enable logic may put more demands on the design. With appropriate logic synthesis, these demands are minimal.

This example illustrates a general technique of finding an equivalent, synchronous circuit to reproduce the operation of the asynchronous circuit. The easiest way to do this is to analyze the timing diagram of the asynchronous circuit, and determine when outputs tran-



4. Decoding a microprocessor access cycle creates a complex logic function for the register clock (a). Instead, the WRn signal can be used as the clock to the register, while the remaining logic can be used as an enable to the register (b).

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sition. Then, create an enable signal that, when used in conjunction with a master clock, will cause the outputs to transition at the same time.

There's nothing inherently wrong with using the rising and falling edges of a clock in the same circuit. The problem lies in how the inverted clocks are created. Often, the use of both edges of a clock could speed up the operation of a circuit *(Fig. 3)*. Q1 and Q2 form a two flip-flip synchronizer, with the first register clocked off the rising edge of CLK and the second clocked off an inverted version of CLK. A few assumptions must be made about the characteristics of the CLK signal and registers. If the registers have a certain maximum frequency of operation (f_{max}), CLK must be run at f_{max} /2 if both edges are to be used (and possibly slower, as will be shown). We'll assume that the duty cycle of the CLK is 50%/50% to simplify the timing analysis.

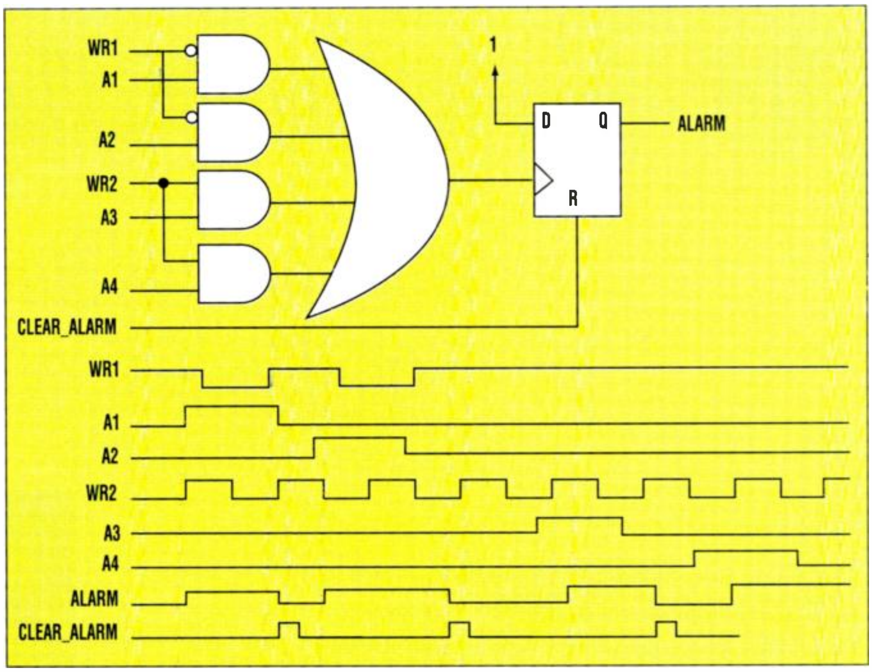
If the logic shown is created with discrete TTL components, the propagation delay of the inverter (t_{INV}) must be accounted for. To ensure that the t_{SU} of Q3 isn't violated, the low time of the clock (t_{PWL}) minus t_{INV} must be greater than or equal to t_{SU}. Thus t_{INV} must be accounted for in determining the maximum rate at which CLK can be run.

If the logic is implemented in a CPLD or FPGA, the architecture of the device determines the timing requirements. In some architectures, CLK is driven directly to all of the device registers across a low-skew clock distribution network. However, to get an inverted version of CLK, the CLK signal might have to pass through a macrocell (in the case of a CPLD), or through a logic cell and routing (in the case of an FPGA).

The timing on t_{INV} will vary, depending on how the clock inversion is created. In a CPLD, t_{INV} is likely a single fixed value, regardless of how many registers need to be clocked with the inverted signal. But, in an FPGA, t_{INV} will probably vary on a register-by-register basis due to placement of the registers and routing of the inverted clock.

Ultimately, the best-case scenario for timing analysis and device operation is for INVCLK to be created, with no skew in relationship to CLK (in other words, t_{INV} = 0 ns). This can easily be done with an appropriate clock-buffering device. However, some FPGA and CPLD architectures, such as the Flash370i and Ultra37000 families, can create inverted versions of incoming clock signals. The device's registers can select either the inverted version of the clock or the original clock, and the clocks are generated with zero skew between them. Any delay from the clock pin to the registers is accounted for in the t_{SU} and t_H values for a register, and are equivalent for inverted and noninverted versions of the original clock.

Using both edges of a clock is a design practice than can speed up the operation of a circuit. Make sure you understand the implementation trade-offs when choosing to use this kind of circuit.



5. Complex logic on a clock's input requires a good deal of analysis. The timing diagram of this circuit indicates that WR1 and WR2 act as clocks.

Asynchronous Bus Interface

In each of the previous examples, there has been a periodic synchronous clock available. Some designs, however, have the clock inputs to registers and flip-flops clocked with internal signals, when no periodic clock is available as a reference. It's often possible to find an alternative circuit that would take advantage of global clocking of a device. By finding an alternative implementation of a circuit that uses a global clock, you can guarantee portability across many architectures and simplify timing analysis.

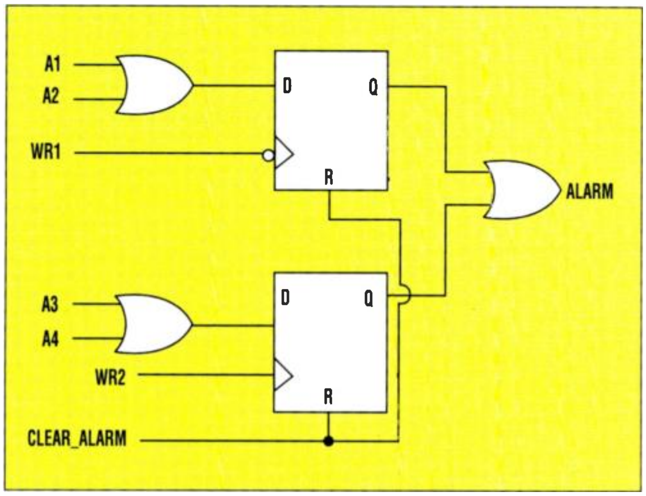
One common use of a programmable logic device is as a peripheral to a microcontroller or microprocessor with an asynchronous bus interface. Let's examine a register that is written to when a processor is accessing the address Axx0 *(Fig. 4a)*. When the logic is reduced for fitting into a CPLD, the result is a fairly complex equation on the clock input to the register:

$$REGCLK = CSn + WRn + \overline{A15} + A14 + \overline{A13} + A12 + A3 + A2 + A1 + A0$$

The timing diagram for this circuit indicates that the register actually changes value on the rising edge of the WRn signal. Also, the processor's data sheet shows that there is a guaranteed t_{SU} and t_H on the data bus around the WRn signal coming from the processor. With this in mind, it's possible to come up with an alternate circuit with WRn as the clock.

This is accomplished by extracting WRn out of the equation above, using it alone as a clock, and using the remaining term as an enable to the register *(Fig. 4b)*. Note that the polarity of the logic is inverted to account for an active high enable on the register. The operation is preserved, but the engineer now has a circuit that can be ported to any device with global clocking, rather than having to rely on a device with product-term clocks.

The previous example was a fairly simple example of extracting a clock



6. A better solution has WR1 and WR2 extracted as clocks to drive independent registers. Although an additional register is needed with this approach, clock logic is simplified.

out of an equation and using the remaining logic as an input to a register (in that case, an enable to a register). Consider an example where logic on six signals makes up the clock to a D flip-flop *(Fig. 5)*. A few simple steps will determine if the circuit in question can be implemented in an equivalent synchronous circuit that doesn't use product-term clocks.

First, look for signals that act like clocks. Typically, these are the signals with the shortest pulse periods (as WRn was in the previous example) or with periodic operation. They effect a change in an output around one edge. In Figure 5, WR1 and WR2 are examples of such signals. WR1 has a short pulse period, and its falling edge causes ALARM to go to 1. WR2 is a periodic signal that can cause a change on ALARM on its rising edge.

Next, look for signals that work in conjunction with the clocks to affect changes in the output. Obviously, A1 and A2 work in conjunction with WR1 to set ALARM, and A3 and A4 work with WR2 to set ALARM. These signals should then be extracted to independent registers *(Fig. 6)*.

For the register clocked by the falling edge of WR1, the logical OR of A1 and A2 can be used on the register's D input to produce its contribution to the final ALARM signal. Likewise, the logical OR of A3 and A4 can be used on the register's D input, clocked by the rising edge of WR2.

Independently, these registers produce a signal that can be used to determine the state of ALARM. In some cases, the logic might be created as a register enable combined with logic on the register's input. However, in this case, logic on the register's D input creates the proper signal. Both registers can use a common clear signal as an asynchronous reset. This will clear the intermediate states, and permit the registers to be ready for another clock edge.

In this example, the OR of the two registers produces the final output as shown in Figure 6. We have eliminated complexity from the clock input to a register, and created a circuit that can be implemented in any programmable logic device or ASIC—without requiring product-term clocking.

Following good design techniques is imperative when designing with the latest PLDs and ASICs. Creating a design is synchronous, and converting those that are not, will make it much easier to get a design to work properly the first time. By following these few simple conversion rules, an engineer can ensure the reliability, readability, portability, and testability of designs:

- Analyze the timing diagram and create an equivalent circuit with a single synchronous clock with clock enables.
- Understand how clocks are created, and the skews and delays that can be expected.
- Find a signal that looks like a clock. Extract it, and use the remaining logic as an enable to the register.
- Extract those same signals again. This time, use the remaining logic as input logic or enables for registers that are clocked by that particular clock. Combine the registers logically to achieve a final result.

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For Optimal Cooling, Rely On Closed-Loop, Fan-Speed Control

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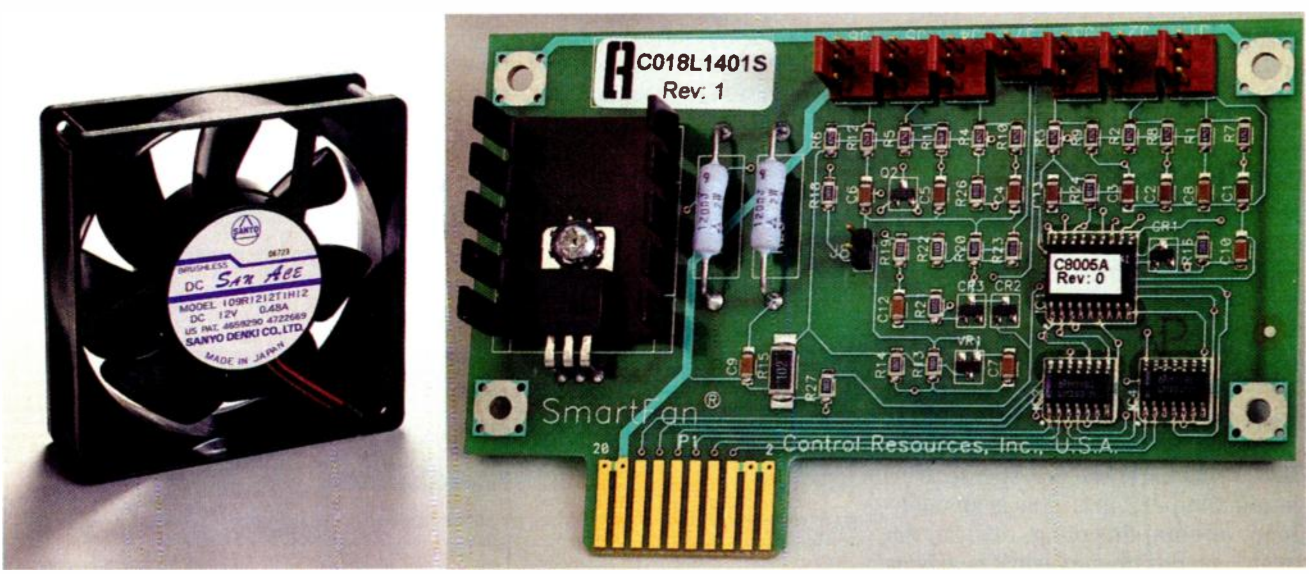
The benefits to designing a cooling system with closed-loop, fan-speed control abound. If done properly, this control method can result in fan-noise reduction under normal thermal conditions, significant savings in energy costs, and increased system reliability. Also, because a closed-loop, speed-control system senses the equipment exhaust air temperature, a temperature-sensing alarm output can be a very economical safety byproduct. With the ready availability of off-the-shelf ac and dc controller boards, as well as dc fans with built-in, closed-loop control, this technology is becoming even more attractive *(see Fig. 1)*.

The principle of closed-loop speed control is really quite simple; the thermostat in your home operates on a closed-loop principle. The thermostat senses air temperature and keeps it nearly constant by turning the heating system on and off. In an electronic-system cooling application, fans run at whatever speed is necessary to hold equipment air temperature near constant. This converts a fan from a "flow-regulating device" to a "temperature-regulating device." Isn't that what you chose a cooling fan for?

With your fans now regulating temperature, you can add or remove a circuit card, or you can take your system to Denver or Death Valley. You don't have to worry about customers changing air filters on time, or the air conditioning breaking down. Even in these cases, your fans will hold equipment temperature near constant by running at the required speed.

Closed-Loop System Design

When it comes to designing a closed-loop system, a number of key parameters or variables must be taken into consideration. The first of



1. The availability of off-the-shelf ac and dc controller boards, as well as dc fans with closed-loop control built right in, makes it relatively easy for a designer to take advantage of the numerous benefits of a closed-loop, fan-speed control system.

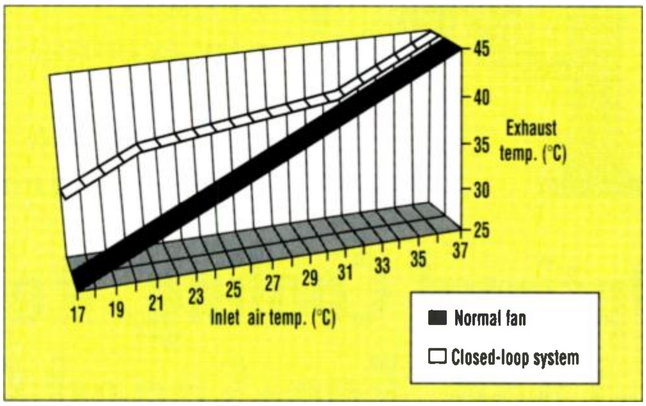
these is the equipment temperature rise, ΔT (the temperature rise of the equipment with fans running at full speed). This can be defined as:

$$\Delta T = T_E - T_A$$

where:

T_E = Exhaust temperature of equipment at full-fan speed.

T_A = Ambient room temperature.



2. With no speed control (fans running permanently at full speed), the system temperature rise is 8°C. As the equipment inlet air temperature varies from 21° to 32°C, the exhaust temperature varies from 29° to 40°C. However, with closed-loop control at a 40°C control temperature, fans idle at half speed below a room ambient of 21°C. They run at full speed above a room ambient of 32°C. As the equipment inlet air temperature varies from 21° to 32°C, the exhaust temperature only varies from 37° to 40°C.

A designer can vary ΔT by choosing air movers with different flow rates, measured in cubic feet per minute.

Another variable to consider when designing closed-loop control is the control temperature. This is defined as the equipment-exhaust temperature, above which fans run at full speed. The recommended control temperatures are shown *(see Table 1)*.

Example

A cooling system has no speed control. Thus, fans constantly run at full speed. The system temperature rise is 8°C. In this example, as the equipment inlet air temperature varies from, say, 21° to 32°C, the exhaust temperature varies from 29° to 40°C *(Fig. 2)*.

Using the same system with a closed-loop control at a 40°C control temperature, with the fans idle at half-speed, below a room ambient temperature of 21°C. The fans run at full-speed above a room ambient temeprature of 32°C. In this example, as the equipment inlet air temperature varies from 21° to 32°C, the exhaust temperature varies from 37° to 40°C *(Fig. 2, again)*.

Other Options

At this time, one might ask, "Why not sense the inlet air temperature (open-loop control)?"

A cooling system could be designed by varying fan speed in response to inlet air temperature. This is an open-loop, or compensating, design. An open-loop design may work nearly as well as a closed-loop design—but not all the time. Going back to the thermostat in your home, an open-loop design is equivalent to placing the thermostat outdoors. This could work—until you light the wood stove or open a window. The internal thermostat (closed loop) can sense these changes, while the external thermostat (open loop) cannot.

The electronic equivalents to the wood stove and window example are: adding or removing cards from a card cage, blocking an air inlet, or having a fan failure (in a system with multiple fans). A closed-loop design (sensing exhaust air temperature) senses these changes, and adjusts fan speed to hold equipment temperature near constant. The open-loop design (sensing inlet air temperature) does not.

A closed-loop design also increases or decreases fan speed according to altitude; an open-loop design does not. A fan in San Francisco can run at a lower speed than the same fan in Denver, for the same thermal load. As stated, the fans in a closed-loop system run at the speed which holds exhaust temperatures near constant. In Denver, where the air is thin, higher velocity is required to achieve the same amount of cooling *(see Table 2)*.

Noise Reduction

A significant advantage of sensing temperature to control fan speed is the potential for considerable reduction in fan noise (under normal thermal conditions). Most equipment designers select fans for the worst-case thermal conditions anticipated, such as a 90°F day in a Denver office, with a broken air conditioner. This creates excessive, unnecessary fan noise under normal thermal conditions, such as a 70°F office building in New York.

Because there is a fifth-power relationship between noise level and fan speed, a small change in fan speed will cause a large change in fan noise. The equation for determining the noise level of a fan, at less than full speed, is given as:

$$L_S = L_1 + 50 \log S$$

where:

S = Fan speed as a fraction of full fan speed.

L_S = A-weighted noise level at fan speed S.

L_1 = A-weighted noise level at full speed.

Example: A 300-ft^3/min. fan has a

TABLE 1: RECOMMENDED CONTROL TEMPERATURES

Equipment Temp. Rise (ΔT) (°C)	Control Temperature (°C)		
	35	40	45
3	■		
4	■		
5	■	■	
6	■	■	
7	■	■	
8		■	■
9		■	■
10			■
11			■
12			■

full-speed noise rating of 59 dBA. What would the noise rating be at half speed?

$L_{fi} = 59 + 50 \log (fi)$
$L_{fi} = 59 - 15$
$L_{fi} = 44$ dBA

Energy Savings

Controlling fan speed according to temperature saves energy. There is an approximate square-law relationship between fan speed and power consumption:

$P_S = P_1(S)^2$

where:

S = Fan speed as a fraction of full-fan speed.
P_S = Power consumption at a fan speed of S.
P_1 = Power consumption at full speed.

If a fan is running at a reduced speed under normal thermal conditions, the potential for saving power is very high.

Example: A 1200-ft^3/min. blower uses 200 W at full speed. How much power would be required to run the blower at 600 ft^3/min. (half speed)?

$P_{fi} = 200(fi)^2$
$P_{fi} = 50$ W

Increased Reliability

Bearing failure, caused by heat and wear, is the most common cause of fan and blower failure. By allowing air movers to run at reduced speeds much of the time, speed control increases fan life. Typical speed-control circuitry can be expected to have a mean time between failure (MTBF) in the 10^6 hours range—far greater than a typical fan running at full speed. The negative impact of the added control circuitry is significantly outweighed by the increased fan MTBF at reduced speeds.

Adding speed control to a cooling system prevents fluctuations in line-frequency and supply-voltage from adversely affecting fan speed. This ensures that fan speed varies only in relation to temperature.

One of the most intriguing aspects of fan-speed control is the positive effect on system reliability. One might think that adding another feature to any system could only decrease its reliability. This is not the case with speed-control circuitry.

With fluctuating semiconductor junction temperatures being a major source of component failure, maintaining a constant temperature inside the enclosure can greatly improve overall system reliability. A closed-loop, speed-controlled system, with the proper slope (3°C in Figure 2) will tend to hold semiconductor junction temperatures constant, even when:

- Circuit boards are added or removed
- Air inlets are partially blocked
- Equipment changes altitude
- One fan fails in a multiple-fan system

No matter how thermal conditions inside the equipment enclosure change, fans run at whatever speed is necessary to hold junction temperatures constant.

Alarms: Temperature Vs. Tach

The use of fans with a tach output, which senses the speed of the fan, has become very popular during the last several years. This tach output is often used to sense and report fan failure using an LED, audible, or electrical alarm signal. A closed-loop speed control may be used in conjunction with the circuitry designed to accept the fan-tach pulses. This arrangement will trigger an alarm faster than a temperature alarm, and has a diagnostic advantage whereby the system can tell a service technician that a fan has failed. By using a tach alarm, one can also avoid the problem of locating an air- or surface-temperature sensor in the critical spot.

One disadvantage of a tach alarm, versus a temperature alarm, is the problem of cost. If you have a closed-loop, speed-controlled system with six fans, adding tach alarms means using six tach fans (three-wire fans), alarm circuitry for the six fans, and additional wiring for each fan. The costs for adding tach detection continue to increase with each additional fan in the system. Adding a temperature alarm, which senses exhaust air or surface temperatures, requires one simple circuit and one output device, but not a special fan.

Another disadvantage to using tach alarms over temperature alarms is the potential for false positives. For example, if the system described above is alarmed to the hilt, and a user unwittingly blocks the equipment exhaust, the fans rise to full speed because of the closed-loop speed control. However, with nowhere for the hot air to go, the temperature continues to rise inside the cabinet. Unfortunately for the piece of equipment, no alarms are triggered, because all the fans are running.

As the equipment operator, I do not care if all the fans are running. My biggest concern is whether my equipment is overheating. Only the service technician that I call after my machine overheats needs to know if all the fans are running.

To model your own closed-loop cooling system, check out the interactive demo at www.controlres.com, or call (978) 486-4160 and request a 3.5-in. demo diskette.

James Kundert is the cofounder and president of Control Resources Inc., Littleton, Mass., a manufacturer of off-the-shelf and custom fan controls and alarms. He has a BS degree in Business Administration from the University of Vermont at Burlington.

TABLE 2: COMPARISON OF LOOP-CONTROL SCHEMES

Closed-loop control	Open-loop control
Noise reduction	Noise reduction
Energy savings	Energy savings
Increased cooling-system reliability	Increased cooling-system reliability
Increased equipment reliability	
Compensates for changes in equipment configuration	
Compensatesfor changes in altitude	
Temperature alarm byproduct	

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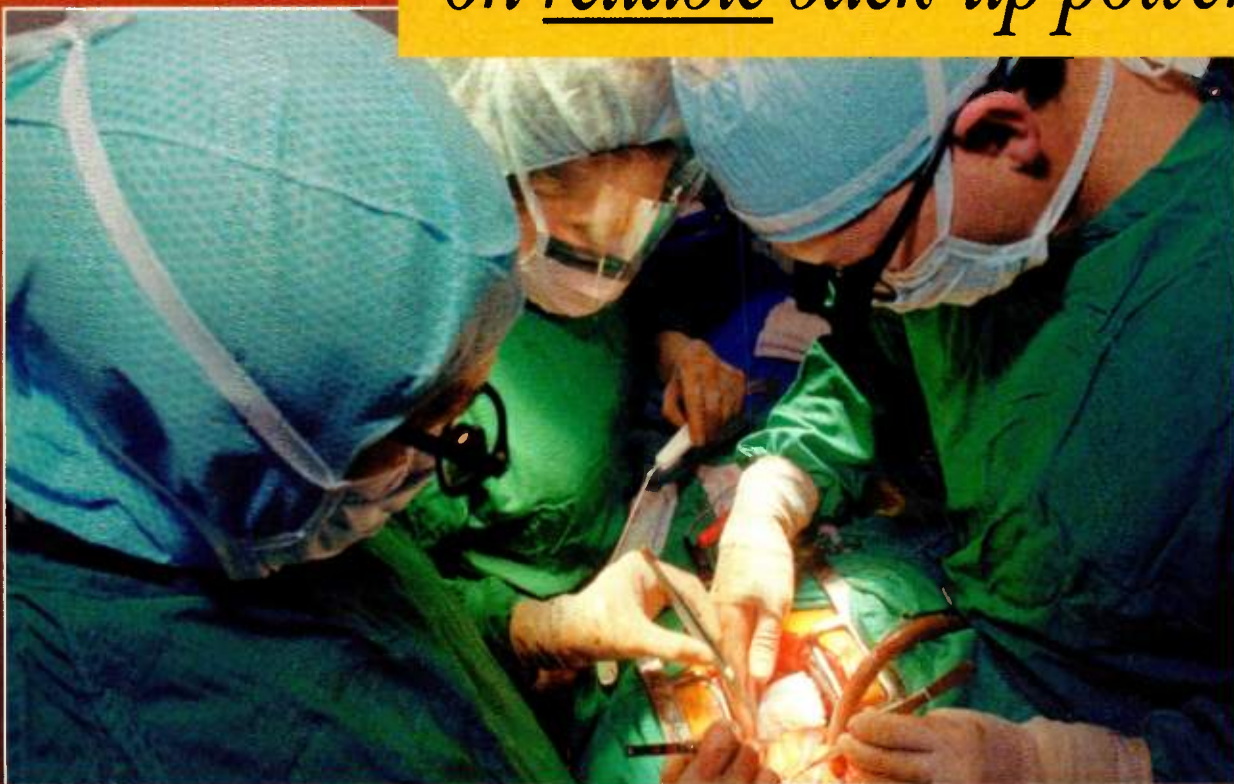

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CPLDs Come In Chip-Scale Package

With its XC9536 complex programmable logic device (CPLD), Xilinx Inc. is the first non-memory, programmable-logic supplier to market with a chip-scale package (CSP). Targeted at PC Card, pc-board, and many portable applications, the CPLD has 48 pins and a footprint that's a third the size of the 44-pin TQ44 package.

Roughly 20% larger than the die they contain, CSPs are currently available in up to 40 different formats from a slew of packaging houses. With their rising popularity, the cost of these devices, which has traditionally been high, is slowly decreasing. In addition, improved reliability, combined with a growing infrastructure to support their manufacture, are combining to make CSPs a more attractive and cost-effective option.

The XC9536 CPLD is but one of many CSP-based devices that will begin to appear in the near future. The device sues a 7- by 7-mm ball-array configuration with a 0.8-mm solder-ball pitch. According to Evert Wolsheimer, vice president and general manager of Xilinx's CPLD division, "Our very popular XC9536 device, in this new 48-pin chip-scale package, contains the same amount of logic as a 44-pin PLCC, but in a package that is roughly the same size as the head of a pencil." The device will be available in 7- and 10-speed grades. Pricing for the XC9536-10CS48 is $3.35 each per 100. Samples are available now, with production volumes ready by June.

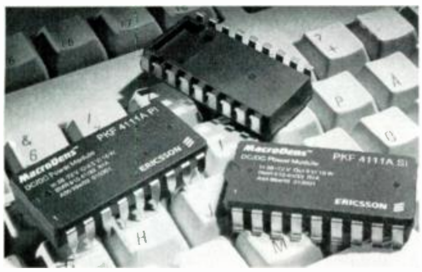
Xilinx Inc.
2100 Logic Dr.
San Jose, CA 95124
Sales Dept. (408) 559-7778
Fax (408) 559-7114
www.xilinx.com.
CIRCLE 452

PATRICK MANNION

PRODUCT FEATURE

Miniature Converter Outputs Up To 2 A

As more and more converters get shoehorned into a single board or subsystem, any measure taken to decrease size to simplify handling and save space can dramatically affect overall system cost. With this in mind, Ericsson shrunk its MacroDens product line with the introduction of the PKF 4000A I series for 48-V and 60-V dc power systems. The first in the series, the PKF 4111A, provides a fully isolated 5-V/2-A output and comes with a 48- by 25-mm footprint.



The PKF 4000A series is available in both surface-mount and through-hole versions, both with an MTBF of over 4.9 million hours. Full output is achieved without heatsinks or forced-air cooling. Key attributes are its low profile, which allows board spacing down to 15 mm; VDE, FCC, and CISPR EMI conformance; and a full 10-W output over the temperature range of –45° to 100°C. Other features include an output that is adjustable from 4.3 to 5.8 V, remote control, and load sharing within 10%. Protection features that include undervoltage (adjustable), short-circuit, and overcurrent. The output-voltage accuracy also is guaranteed at 5.05 V, ±30 mV. The voltage regulation and efficiency are 80 mV and 83%, respectively.

Pick-and-place compatible, the series' overmolded package is fully compatible with aqueous and semi-aqueous cleaning processes. Pricing is $25.50 per 1000; samples are available from stock.

Ericsson Components AB
Energy Systems Div.
Pyramidbacken 1. Kungens Kurva
S-16481, Kista-Stockholm
Sweden
Lars Thorsell, +46 8 721 7045
e-mail: lars.thorsell@ericsson.com
CIRCLE 453
PATRICK MANNION

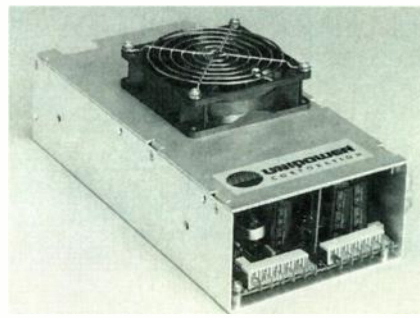
40-W DC-DC Converter Has Low-Voltage Outputs

The BXA40 is a 40-W dc-dc converter that measures 2.2 by 2.2 by 0.5 in. Able to take inputs of 18 to 36 V or 36 to 75 V, the converter outputs 3.3, 5, 12, or 15 V, or 2.9, 3.3, 5, 12, or 15 V, respectively. Triple-output versions output 5 and ±12 V or 5 and ±15 V. The converter uses fixed-frequency switching at 400 kHz to minimize noise, and has IEC950 safety approval. Other features include aluminum baseplate technology, 1500-V dc isolation between input and output and between input and case, and remote on/off capability. Specifications include a line and load regulation of ± 0.3% and ±1.0%, respectively. Pricing is $62 each per 1000.

***Artesyn Technologies,** 7575 Market Place Dr., Eden Prairie, MN 55344; 612-941-1100; fax (612) 829-1837; Internet: www.artesyn.com.* **CIRCLE 454**

375-W Switchers Include Power-Factor Correction

Available with two to four outputs in a compact case, the LM Medical Series of 375-W switching supplies also comes with power-factor correction to 0.99. The supplies take a universal input of 90 to 264 V ac, are certified to IEC601 and UL2601, and have an earth leakage current specification of 0.3 mA (max) for a 250-V ac input. The supplies come in three versions: open frame, covered with top fan, or covered with end fan. Measurements are 2.5 by 5 by 10 in. and the power density is 3 W/in.^{3}. Other features include outputs of 5, 12, or 24 V, overvoltage protection, remote sensing, current sharing, and main output voltage adjustment of ±5%. Pricing starts at $418; delivery is five days.



***Unipower Corp.,** 3900 Coral Ridge Dr., Coral Springs, FL 33065; (954) 346-2442; fax (954) 340-7901; e-mail: sales@unipower-corp.com; Internet: www.unipower-corp.com.* **CIRCLE 455**

Linear Power Supplies Reduce System Costs

The H Series of low-cost linear power supplies operate in ambients of up to 70°C and come with CE, UL, CSA, and TUV approvals. Noise levels below FCC Class B and VDE level B for EMI reduce the need for system filtering. The series comes in 20 models with single, dual, or triple outputs, and with voltages ranging from 5 to 28 V. Power outputs range from 15 to 115 W. Pricing ranges from $34.50 to $88.75.

***Lambda Electronics,** 515 Broadhollow Rd., Melville, NY 11747; David Norton (619) 575-4400, ext. 508; fax (619) 575-7185.* **CIRCLE 456**

LINEAR TECHNOLOGY DESIGN NOTES

Micropower MSOP 10-Bit ADC Samples at 500ksps

Design Note 184

Guy Hoover, Marco Pan and Kevin R. Hoskins

INTRODUCTION

The LTC®1197/LTC1199 10-bit serial ADCs offer small size, low power operation and fast sample rates with good AC and DC performance. These parts are ideal for low power, high speed and/or compact designs. This Design Note discusses the features and performance that make the LTC1197/LTC1199 excellent choices for such new designs.

FEATURES

Smallest Size (MSOP)

The LTC1197/LTC1199 are among the smallest ADCs available. The LTC1197/LTC1199's serial interface allows the use of 8-pin MSOP and SO packages. Although the SO package consumes little area, the MSOP package reduces the small footprint even further. These are some of the first ADCs available in the MSOP package, which is about half the size of the SO-8.

3V or 5V Supplies

The LTC1197/LTC1199 are 5V parts (V_{CC} = 4V to 9V for the LTC1197 and 4V to 6V for the LTC1199). Also available for use in 3V systems are the LTC1197L and the LTC1199L (V_{CC} = 2.7V to 4V). Designed for use in mixed-supply systems, these devices operate flawlessly even when the the digital input is greater than the V_{CC} voltage. This is useful in systems where the ADC is running at a lower supply voltage than the processor. If the ADC is running at a higher supply voltage than the processor, the ADC serial data output voltage can easily be decreased to a level appropriate for the processor.

PERFORMANCE

Micropower Performance with Auto Shutdown at Full Speed

Running continuously, the LTC1197L consumes only 2.2mW at the maximum sampling rate (25mW for the LTC1197). The power consumption drops dramatically, as shown in Figure 1, at lower sampling rates. The formula for calculating power consumption is:

$$P_D = V_{CC} \bullet I_{CC} \bullet t_{CONV} \bullet f_S$$

where P_D is the power consumption, V_{CC} is the supply voltage, I_{CC} is the supply current while the conversion is occurring, t_{CONV} is the conversion time and f_S is the sample rate. As you can see from the formula, lowering f_S reduces the power consumption linearly. It is also important to minimize t_{CONV} by clocking the ADC at its maximum rate during the conversion. In this way, the total power is less because the device is on for a shorter period of time.

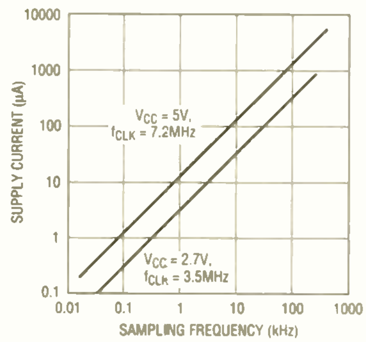


Figure 1. The LTC1197/LTC1199 Reduce Their Supply Current Consumption and Save Power When Operating at Lower Sample Rates

High Speed Capability

Even though the LTC1197/LTC1199 are capable of micropower operation, they are able to sample at rates of up to 500kHz. These parts can also digitize fast input signals up to the Nyquist frequency (250kHz for the LTC1197) with over nine effective number of bits (ENOBs).

Good DC and AC Specs

The DC specifications of these parts are very good. Linearity (both INL and DNL) is typically 0.3LSB with a maximum spec of 1LSB. Offset is specified at 2LSBs (max) and gain error is specified at 4LSBs (max). These specifications are guaranteed over the full temperature range of the part. Both commercial and industrial temperature range versions are available.

AC performance is equally impressive. S/(N + D) is typically 60dB (58dB for the L version). THD is typically −64dB (−60dB for the L version) and the peak harmonic or spurious noise is typically −68dB (−63dB for the L version). An FFT of the LTC1197's conversion performance is shown in Figure 2.

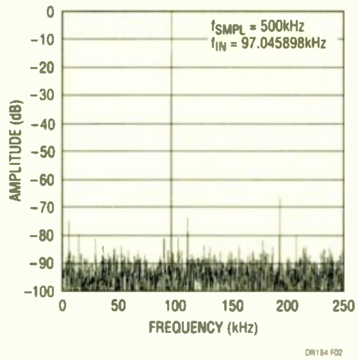


Figure 2. The LTC1197's Typical 60dB SINAD Shown in the FFT Curve is Among the Best and Translates into 9.7 Effective Bits

Flexible Inputs

The LTC1197 has a single differential input and a wide range reference input. The reference input allows the full scale to be reduced to as low as 200mV. This translates to an LSB size of only 200µV. Combined with the high impedance of the analog input, this allows direct digitization of low level transducer outputs, which can save board space and the cost of a gain stage.

With its software-selectable 2-channel MUX, the LTC1199 is capable of measuring either one differential or two single-ended input signals. Both parts have a built-in sample-and-hold.

Serial I/O

The LTC1197/LTC1199 are hardware and software compatible with SPI and MICROWIRE™ protocols using either 3- or 4-wire serial interfaces. This compatibility is achieved with no additional circuitry, allowing easy interface to many popular processors.

Battery Current Monitor

Figure 3 shows a 2.7V to 4V battery current monitor that draws only 45µA from the battery it monitors. Supply current is conserved by sampling at 1Hz and using the LTC1152's shutdown pin to keep the op amp off between conversions. The LTC1197 automatically shuts down after a conversion. The circuit can be located near the battery, serially transmitting data to the microprocessor.

CONCLUSION

Conserving space and power, the LTC1197/LTC1199 have a small footprint and are capable of micropower operation. They have a versatile, SPI/MICROWIRE compatible serial interface. The adjustable reference input, 2-channel, software-selectable MUX and 5V or 3V operation increase this ADC family's versatility. When this versatility is combined with the high conversion rate and good DC and AC performance, you can see why these ADCs are good choices for low power, high speed and/or compact designs.

MICROWIRE is a trademark of National Semiconductor Corporation.

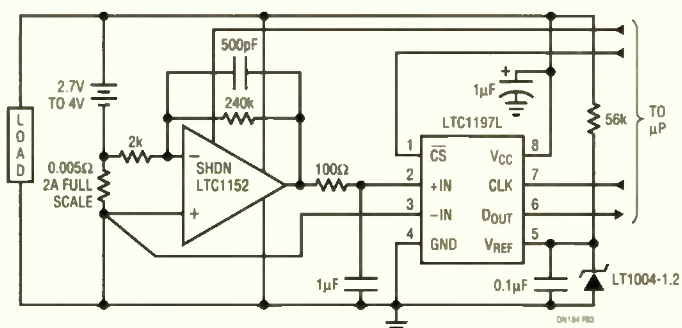


Figure 3. This 0A to 2A Battery Current Monitor Draws Only 45µA from a 3V Battery

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PRODUCT UPDATE: COMPONENTS

Manufacturer	Device	Description	Price and delivery	CIRCLE
		RESISTORS		
AVX Corp. Myrtle Beach, SC Sales Dept. (803) 946-0414 Fax (803) 448-1943 www.avxcorp.com	LR50 series current-sense chip resistor	This thick-film, current-sense chip resistor comes in a 1020-size package, and can handle up to 1 W. The devices range in value from 50 to 20 mΩ, with standard tolerances of ±1%, and a TCR of ±100 ppm/°C. The operating temperature range is from -55 to 125°C.	$0.14 to $0.25 each per 100.000	485
Isotek Corp. Swansea, MA Bill Poisson (508) 673-2900 Fax (508) 676-0885 E-mail: tekinfo@isotekcorp.com www.isotekcorp.com	IR-H high-power resistor	This high-power, metal-clad, wirewound resistor is available in nine power ratings, from 0.1 W to 6.8 kW. Available in 1500-, 3500-, 4500-, and 5400-V ac dielectric strength options, the resistor comes in an extruded-aluminum housing with standard or non-inductive windings. Connections are via metal-tab terminals or high-temperature-resistant lead wires. Stacking is optional.	$27.20 each per 500	486
Ohmite Skokie, IL Sales Dept. (847) 675-2600 Fax (675) 675-1505 E-mail: ohmite@wwa.com www.ohmite.com	OX/OY series ceramic resistors	These axial-leaded, ceramic-composition resistors are available in values from 3.3 W to 1 MW, with a standard tolerance of ±10%. Derating is linear from 100% at 70°C, to 0% at 200°C.	$0.42 to $0.63 each per 1,000; stock to eight weeks	487
State of the Art, Inc. State College, PA Sales Dept. (800) 458-3401 Fax (814) 355-2714 E-mail: sales@register.com www.resistor.com	Thin-film chip attenuators	Measuring 0.075 by 0.060 by 0.010 in., these lightweight, thin-film chip attenuators are available with attentuation factors of 1 to 20 dB in 0.5-dB increments. the devices are rated at 50 V (max) and 0.125 W (min). With an operating frequency range of dc to 18 GHz, the devices have a VSWR as low as 1.2, depending on size, style, and frequency. Available tolerances are ±0.5 dB and ±1 dB.	$1 each in quantity; eight to 10 weeks ARO	488
Unique Concepts Springfield, PA Sales Dept. (716) 283-4025 Fax-back (800) 7-VISHAY	NOMC series precision network	This dual-in-line, precision resistor network comes in a power range of 100 W to 500 KW, with a tolerance range of 1.0% to 0.10%. The absolute TCR is ±50 ppm/°C to ±10 ppm/°C (0° to 70°C). Rated at 50 mW, the device measures 0.150 in. wide and has four, 14, or 16 pins.	$1.77 each per 1000; eight weeks	489
		CAPACITORS		
Sprague-Goodman Electronics Inc. Westbury, NY Bernice Feller (516) 334-8700 Fax (516) 334-8771 E-mail: Info@spraguegoodman.com www.spraguegoodman.com	GKG 15/16 series ceramic-dielectric trimmers	These top-tuning (15 series) or bottom-tuning (16 series), low-cost, ceramic-dielectric trimmer capacitors are available in nine capacitance ranges from 1.0 to 3.0 pF, and from 15.0 to 70.0 pF. The 6-mm devices are color coded, and their operating temperature range is from -25° to 85°C. The voltage rating is 100 V dc.	15 series, $0.13 each per 25,000; stock to 12 weeks	490
Tecate Industries Inc. Poway, CA Sales Dept. (619) 513-8700 Fax (619) 513-2345	Type 715E axial aluminum capacitors	With an operating temperature range of -40° to 105°C and measurements of 5 by 13 mm, these axial, aluminum, electrolytic capacitors target a variety of commercial and industrial applications. The capacitance and voltage ranges are 0.47 to 15,000 µF, and 6.3 to 100 V, respectively. The capacitance tolerance is ±20% (120 Hz, 20°C). Custom sizes are available.	$0.08 each per 5000; stock to eight weeks	491
United Chemi-Con Rosemont, IL Sales Dept. (847) 696-2000 Fax (847) 696-0857 E-mail: Info@chemi-con.com www.chemi-con.com	LXY and LXZ series axial aluminum electrolytic capacitors	Measuring 4 by 5 to 16 by 40 mm (LXY) and 4 by 7 to 18 by 40 mm (LXZ), these aluminum electrolytic capacitors can withstand HCFC cleaning agents for five minutes. The devices have capacitance and voltage ranges of 3.3 to 8200 µF and 4.7 to 18,000 µF, and 10 to 63 V dc and 6.3 to 50 V dc, respectively. Their operating temperature range is -55° to 105°C.	$25 each per 1000; stock to 10 weeks	492
		INDUCTORS		
Associated Components Technology, Inc. Garden Grove, CA Erik Dieckhoff (800) 234-2645 Fax (714) 265-4810 E-mail: actsales@ix.netcom.com	SHR series surface-mount transformers	Able to handle up to 10 A, these surface-mount inductors can replace through-hole, radial-, and axial-leaded devices. The devices have a footprint of 0.44 in.^{2}, with profile heights of 0.20, 0.32, 0.42, and 0.52 in. Inductances range from 1.0 to 10.0 µH, and four different wire gauges are available. The chips are both flow and reflow solderable, and the operating temperature range is -45° to 125°C.	$0.95 each per 10,000; stock to six weeks ARO	493
Toko America Inc. Mt. Prospect, IL Sales Dept. (847) 297-0070 Fax (847) 699-7864 E-mail: Info@tokoam.com www.tokoam.com	PTL series etched chip inductor	Targeting VCO, GaAs amplifier matching, and notch-filler applications, these single-layer, photo-etched inductors have a stability of 150 ppm/°C, and come with an 0805 footprint. The devices have an inductance range of 1.0 to 39 nH, and come on tape and reel in quantities of 4000.	$0.17 each per 50,000	494
		SEMICONDUCTORS		
CP Clare Corp. Beverly, MA Sales Dept. (800) CPCLARE Fax (978) 524-4900 www.cpclare.com	LCA100/ LCA100L optically coupled MOSFET	This single-pole, normally open, optically coupled MOSFET switch has an on resistance of 25 Ω, handles up to 125 mA at 350 V, and has a 2-mW drive capability. Other features include an expected life of over 15 billion operations, an input/output isolation of 3750 VRMS, and compatibility with wave soldering.	$1.58 to $1.65 each per 10,000	495
SGS-Thomson Microelectronics Inc. Lincoln, MA Sales Dept. (781) 259-0300 www.st.com	STY34NB50 power MOSFET	Based on the company's PowerMESH technology, this 500-V power device has an on resistance of 100 mW, a total gate charge of 150 nC, and a maximum body diode dV/dt rating of 4 V/ns. The device is 100% avalanche tested at both 25° and 100°C.	$5 each per 10,000	496

Circle 520

Sensor Identifies Insulated "Hot"-Line Conductors

ANDRE S. KISLOVSKI
Ascom Energy Systems, Berne, Switzerland.

Certain situations call for a simple way to find out if a line conductor is "hot" or not. If the conductor isn't insulated, a popular method is to use a screwdriver with a built-in high-value resistor and a neon tube. The sensitivity of such a device is too low to work with an insulated conductor. The circuit shown in the figure can identify a "hot" conductor even if it's insulated.

A clip put around the conductor under test acts as a small capacitor between the conductor and the circuit, and the path to the ground conductor is closed, exactly as in the case of the popular screwdriver test, through the operator. If the conductor is "hot" and the switch is open, a diode charge pump raises the voltage across the gate-to-source capacitance (not shown) of a MOSFET, so that eventually the MOSFET starts conducting.

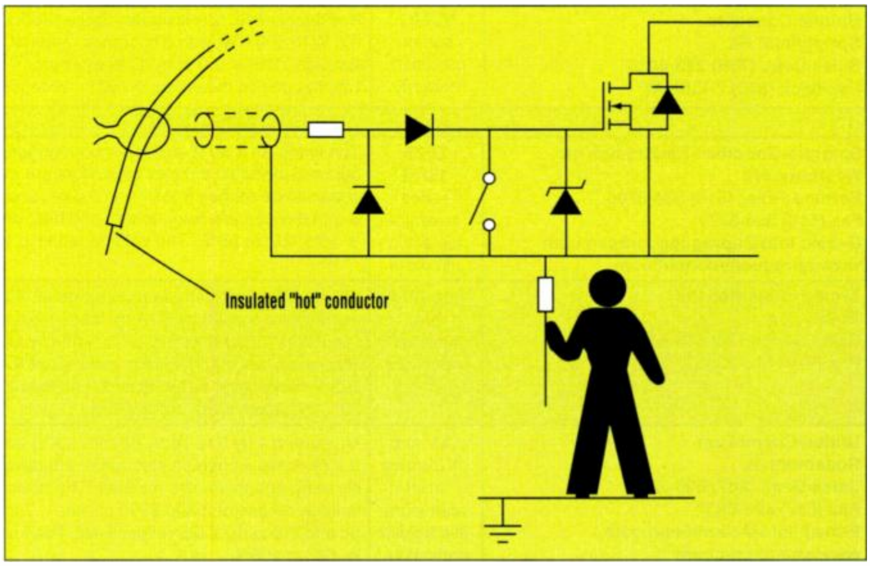
The MOSFET's conduction can be monitored either by a built-in ohm-meter, or a buzzer of an inexpensive handheld multimeter. Another possibility is to make the MOSFET turn on a LED indicator powered by a separate battery. In that case, the capacitive "hot"-line-conductor sensor is independent of the multimeter.

A switch is included to quickly discharge the gate-to-source capacitance in case of repeated tests. A resistor is added to protect the operator and the circuit in the event the test clip is brought in direct contact with a non-insulated "hot" line conductor. The shield is insulated and can't touch the line conductor. Note that the sensor works equally well with insulated and non-insulated line conductors. Finally, a Zener diode prevents the gate-to-source voltage from exceeding the MOSFET's ratings.

The entire circuit requires so little space that it could be incorporated into handheld multimeters. The author upgraded his multimeter by inserting a small PCB with the entire sensor circuit between the case of the multimeter and its flexible protective sheath. The test clip is a slightly modified mounting clip from one side of a 20-by-5-mm pc-board fuse. The length of the cable between the clip and the first protection resistor of 1.5 M is approximately 50 cm. Both diodes are 1N4007s, the Zener diode is a BZX55C15, and the second protection resistor also is 1.5 M. The MOSFET isn't critical, but its case should be flat if the circuit is to be mounted between a multimeter and its sheath.

Note that if a digital multimeter (DMM) with an extremely high input impedance were used with a similar clip, it could, in principle, also detect a "hot" conductor. However, because of the omnipresent line-power fields, it would display some reading also with the clip being anywhere in the space—not only when it's placed on the insulation of a "hot" conductor. Depending on local environment, a DMM would even display a reading with the clip around a "cold" conductor.

The merit of the circuit shown is that it substantially increases the signal-to-noise ratio and thus decreases a probability of false readings. In addition, any of the described versions of this sensor could be used to locate an ac line circuit break.



A capacitive sensor can be used to detect "hot" ac-line conductors, even when insulated.

Circle 521

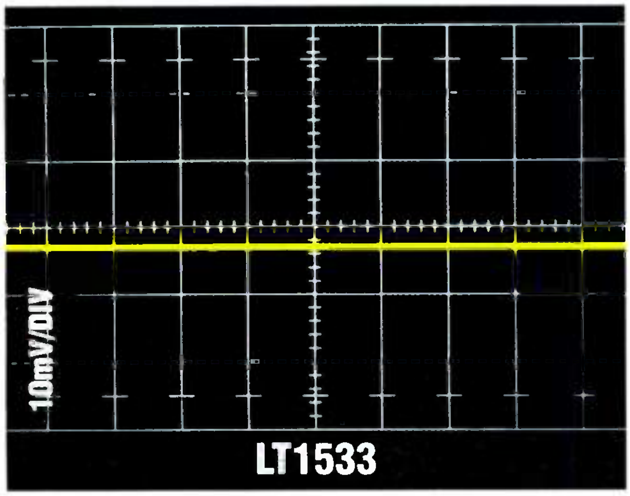
Automatically Switch Between Two Serial Input Devices

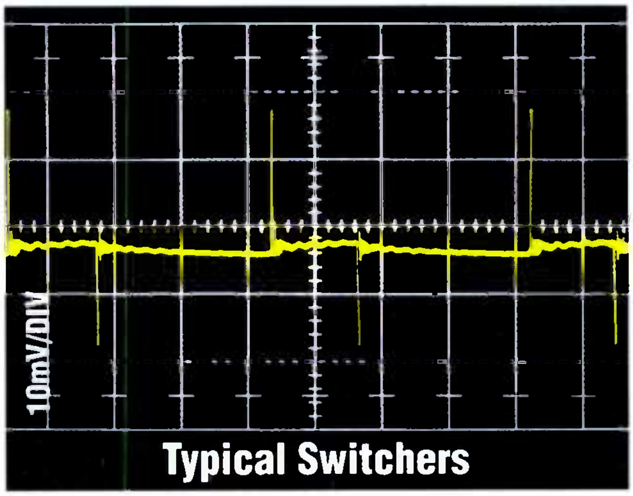
LUCIANO PAUTASSO
Via Verdi 11, 10042 Nichelino, Italy; e-mail: l.pautasso@Rocketmail.com

Typically I prefer to use the standard serial mouse when working with most programs in Windows, such as Office95, but when drafting with programs like Autocad, I prefer using a trackball. The automatic switchover circuit presented here accomplishes this without requiring the user to shut down, change connectors, and reboot the PC.

It can be constructed in a small box with two sub-D connectors to accept the

100µV Output Noise Switching Regulator





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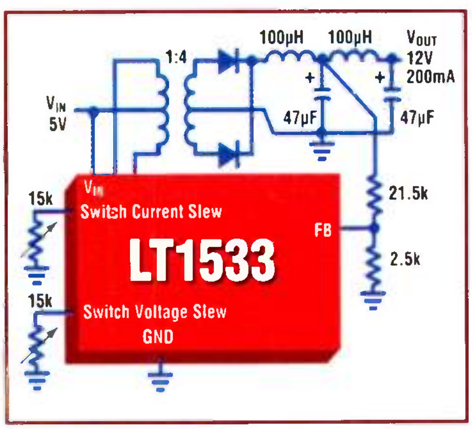

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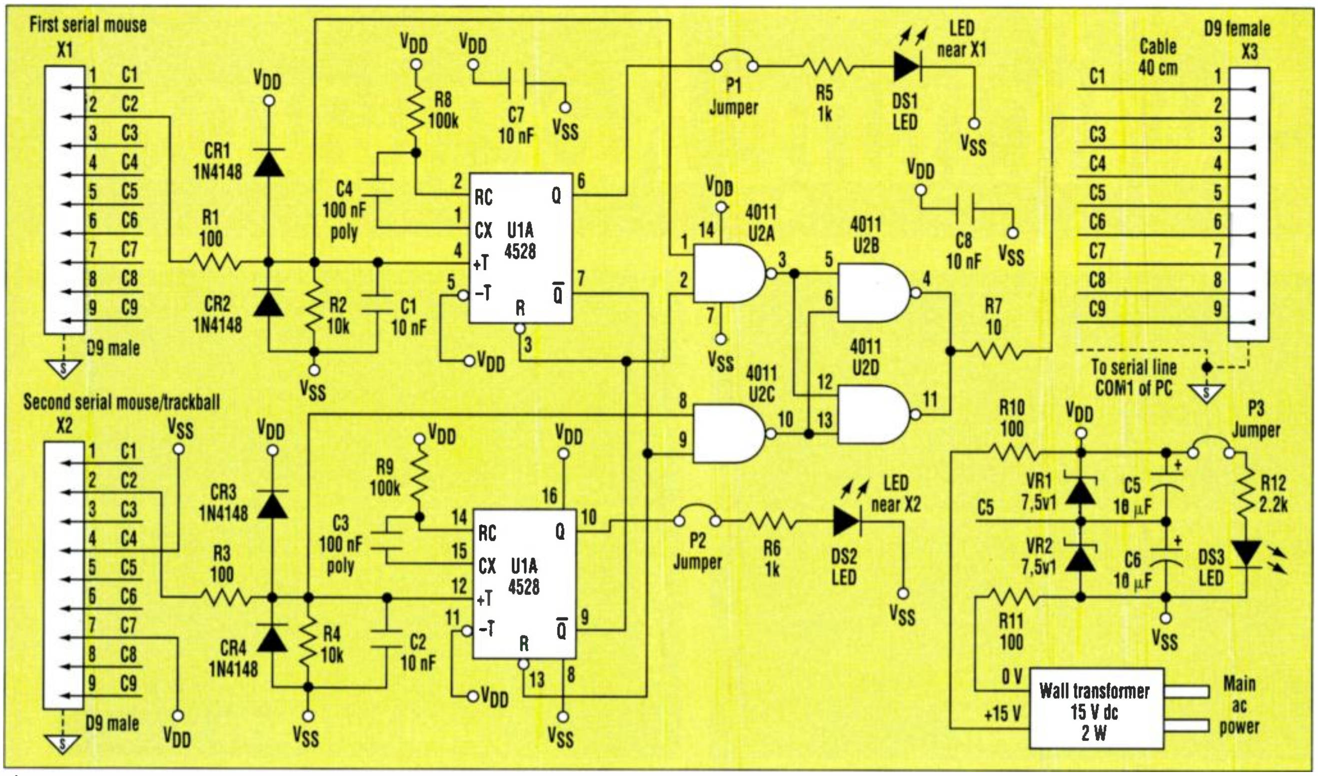

This circuit provides the user with the convenience of automatic switchover between a serial mouse and a trackball.

two mice. A third cable with a sub-D connector is connected to the PC serial port (COM1 or COM2).

The circuit is an automatic switch controlled by two signal detectors. When the first mouse is moved, U1A (a retriggerable flip-flop) disables the second mouse and vice versa. If both the mice are moved simultaneously, only one will gain access to the PC's serial input. LEDs DS1 and DS2 indicate which mouse is currently connected.

The power supply is external from a wall transformer to avoid overloading the serial lines of the PC. To experiment with self-powered configurations, you must:

- remove P1,P2,P3, to reduce the current used
- remove VR1,VR2,C5,C6
- remove the wall transformer
- jumper V_{DD} to C4
- jumper V_{SS} to C7.

Circle 522

Low-Cost Fan Manager For Power-Supply Applications

DON ALFANO
Telcom Semiconductor Inc., 1300 Terra Bella Ave.,
P.O. Box 7267, Mountain View, CA 94039-7267.

Modern system ergonomics require an increasing amount of electronics to be crammed into ever tighter quarters. Consequently, space allocations for the ubiquitous power supply shrinks. These smaller power-supply form factors, in addition to greater power demands, are boosting the popularity of brushless dc (BDC) cooling fans. But while BDC fans adequately evacuate heat from the system enclosure, they add other more significant problems.

First, there's the annoying acoustic roar of turbulent air flow from the fan's normal full-speed operation. Then there's the issue of the large current consumed by the fan itself—a significant problem in today's microamp-stingy systems. In addition, fan reliability and service life are concerns. Because the fan is a complex electromechanical device, it probably will require replacement before the lifetime of its host system expires. Finally, even if all is well with the fan, trauma brought on by an obstruction of the fan air intake or an object lodged in its rotor, can completely incapacitate it. These issues are bringing ever increasing scrutiny to the fan and its well-being.

These concerns can be addressed with common system techniques. For example, it's been known for some time that acoustic noise is greatly reduced when the fan is operated at lower speeds. Temperature-proportional fan-speed control, for example, runs the fan only as fast as required to keep the system cool. This not only greatly reduces acoustic noise, but extends fan service life because the fan isn't subjected to the stress imposed by continuous full-speed operation.

While speed control is a cure for sev-

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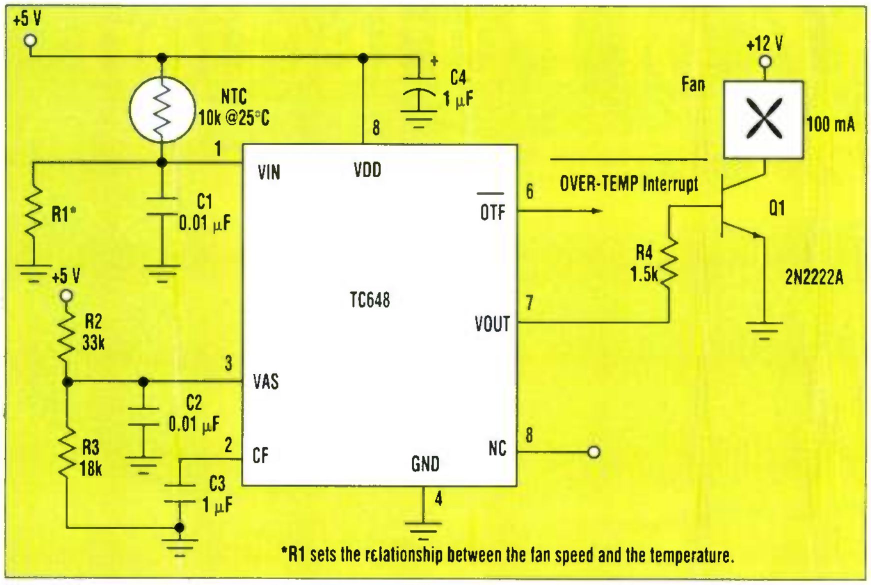

Shown is a temperature-proportional fan-speed control that operates the fan only as fast as required to keep the system cool. This, consequently, minimizes acoustic noise and extends fan service life.

eral fan ills, monitoring the fan's health can be a complex task. One very simple approach is to detect when system temperature is excessively high, indicating the fan has either lost capacity (possible air-intake obstruction or bearing failure), or has stopped running altogether.

The circuit shown in the figure is a complete solution to the problem of fan management as previously outlined. TelCom's TC648 is a stand-alone, low-cost fan manager that integrates a pulse-width modulation (PWM) fan speed controller (with integrated startup timer) and an over-temperature detector. It drives any standard two-wire fan through a low-cost transistor (Q1). The input voltage range (V_{IN}) is 1.5 V to 2.6 V (corresponding to 0% to 100% fan speed). The figure shows the temperature signal generated with a low-cost NTC thermistor and R1. The output duty cycle (and, therefore, fan speed) increases with increasing voltage on V_{IN}. The over-temperature fault output ($\overline{OTF}$) is asserted when the voltage on V_{IN} exceeds 2.6 V, indicating insufficient cooling due to a fan fault or system thermal runaway.

The circuit provides temperature-proportional fan-speed control and over-temperature detection. It also suspends fan operation (for even greater system efficiency) when temperature falls to a point (set by R2 and R3) where forced-air cooling is no longer required. This elegant little circuit is a fitting mate to any two-wire BDC fan, and rewards the end user with quieter system operation, improved system reliability, and more efficient system operation.

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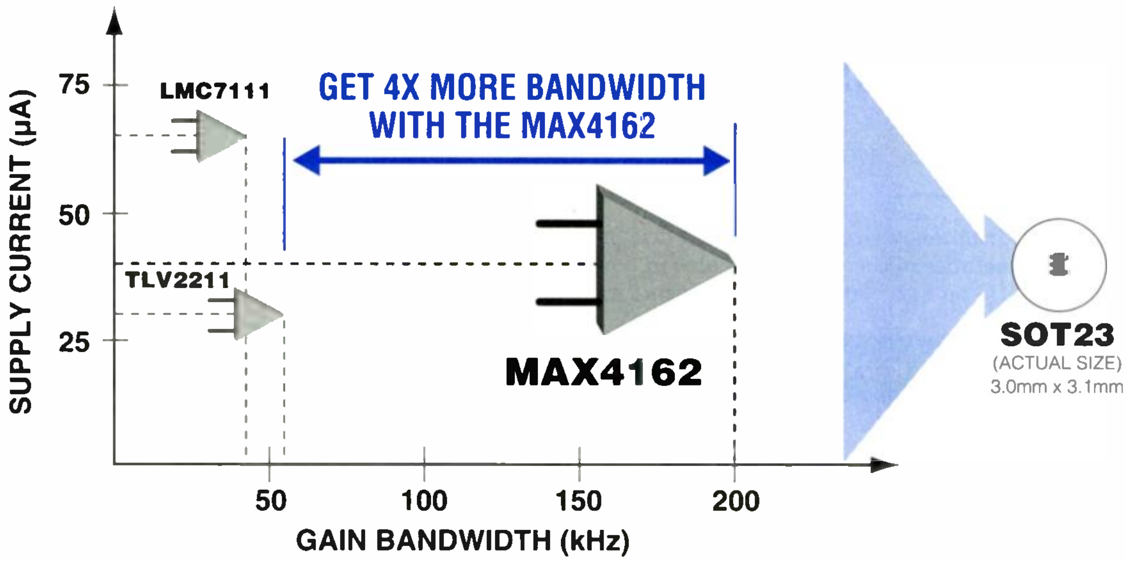

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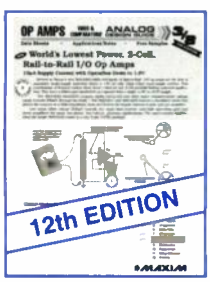
MAX4162	1	40	200	2.7 to 10.0	-0.25 to 3.25	0.005 to 2.995	10	5-pin SOT23, 8-pin SO
MAX4163	2	40	200	2.7 to 10.0	-0.25 to 3.25	0.005 to 2.995	10	8-pin SO/μMAX
MAX4164	4	40	200	2.7 to 10.0	-0.25 to 3.25	0.005 to 2.995	10	14-pin SO, 16-pin QSOP

† V_{SS} = 0V, V_{DD} = 3.0V   Rail-to-Rail is a registered trademark of Nippon Motorola Ltd.



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Circle No. 152 - For International

Circle 523

Specifying Frequencies For Leakage Inductance Measurements

JIM ALLEN
J. A. Associates, P.O. Box 5705, Diamond Bar, CA 91765; (909) 860-7408.

In modern high-frequency circuits, the leakage inductance of the magnetic components can be a very important design consideration. However, it's also important not to hamper the transformer manufacturer with unrealistic testing requirements. A little time spent considering the test frequency can save time and frustration later.

The typical transformer shown has a primary inductance (L_P) of 16.5 mH; a primary dc resistance (R_P) of 14 Ω; a secondary dc resistance (R_S) of 52 mΩ; a primary-to-secondary ratio (a) of 15 (210/14); and a leakage inductance (L_L) of approximately 150 mH *(Fig. 1)*. To measure the leakage inductance, first short the secondary winding, (i.e., load the secondary with its dc resistance, or R_S), then measure the inductance on the primary. The equivalent circuit is shown in Figure 2.

To calculate the inductance of the equivalent circuit, less the leakage inductance, rationalize the impedance equation and solve for the new inductance, L_E, where $R_E = a^2R_S$ and L_P is the primary inductance:

$$L_E = \frac{X_O}{\omega}$$

where:

$$X_O = \frac{R_E^{\,2} * XL_P}{R_E^{\,2} + XL_P^{\,2}}$$

LEAKAGE INDUCTANCE MEASUREMENTS

L_P	a^2R*	f_1	L_{e1}	L_{m1}	f_2	L_{e2}	L_L
16.5 mH	11.7 Ω	1 kHz	207 µH	357 µH	15.75 kHz	0.85 µH	155 µH
0.77 H	8 Ω	100 Hz	210 µH	290 µH	1 kHz	2.1 µH	85 µH
1.5 mH	8 Ω	10 kHz	10.7 µH	11.5 µH	150 kHz	0.05 µH	0.8 µH
11.8 µH	0.42 Ω	10 kHz	2.9 µH	5.9 µH	100 kHz	0.04 µH	3.4 µH
14.5 µH	0.21 Ω	10 kHz	0.73 µH	1.08 µH	100 kHz	0.008 µH	0.45 µH

*a^2R is the parallel combination of the a^2Rs of each secondary winding.

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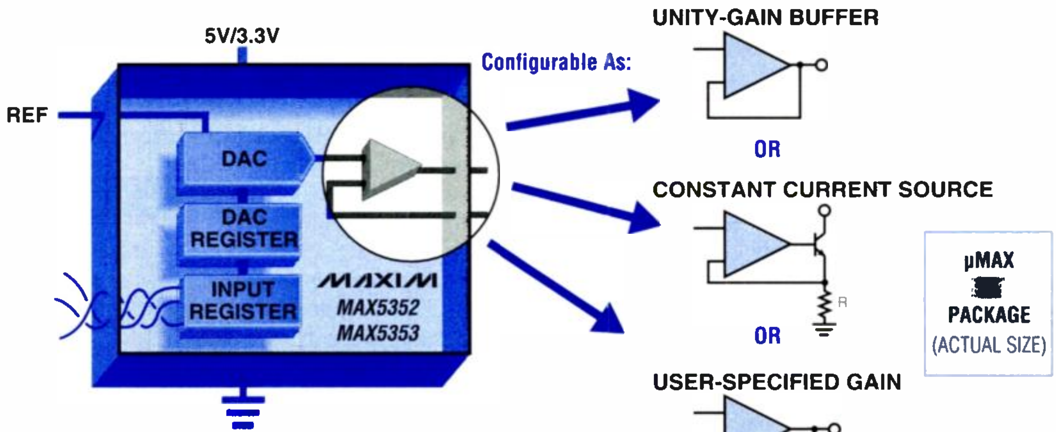

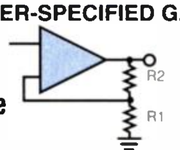

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MAX5353	12	3.3	8-pin μMAX/DIP	Yes
MAX5354	10	5	8-pin μMAX/DIP	Yes
MAX5355	10	3.3	8-pin μMAX/DIP	Yes

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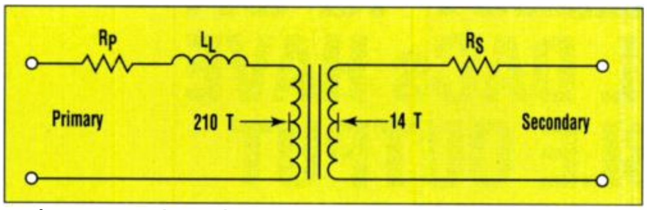
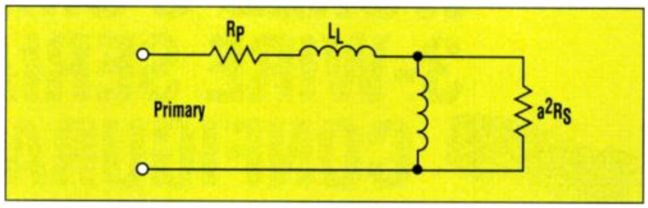


1. This is a typical transformer featuring a primary inductance of 16.5 mH; primary and secondary dc resistances of 14 Ω and 52 mΩ, respectively; a primary-to-secondary ratio of 15 (210/14); and a leakage inductance of about 150 μH.



2. An equivalent circuit to that in Figure 1 is used to calculate leakage inductance. Using such a model, the leakage inductance at a specific test frequency can be reliably predicted, allowing the generation of more realistic transformer testing requirements.

To calculate the equivalent (leakage) inductance at 1000 Hz:

$\omega = 2\pi f = 6.28 * 10^3$

$XL_P = \omega L_P = 104$

$R_P = a^2 R_S = 11.7$

Substituting in the given equations gives: $X_O = 1.3$; and $L_E = 207\ \mu H$.

This (L_E) plus the actual leakage inductance is the measured leakage inductance. For this example, the leakage inductance measures 360 μH (207 μH + 150 μH).

Now, calculating the equivalent inductance at 15,750 Hz:

$\omega = 2\pi f = 9.89 * 10^4$

$XL_P = \omega L_P = 1.63 * 10^3$

$R_P = a^2 R_S = 11.7$

Substituting in the given equations results in: $X_O = 0.084$, and $L_E = 0.85\ \mu H$. For all practical purposes, this (L_E) plus the actual leakage inductance is the *measured* leakage inductance!

The table provides a listing of various transformers with their equivalent leakage inductance calculations at different frequencies and the leakage inductance measurements at f_2. The measured inductance at f_1 (L_{M1}) for all tabulated transformers is within 20% of the calculation (L_{E1}) when L_L is subtracted.

A good rule of thumb when selecting the frequency for measuring leakage inductance is to be sure that the primary reactance (XL_P) is at least 100 times the reflected secondary dc resistance (a^2R).

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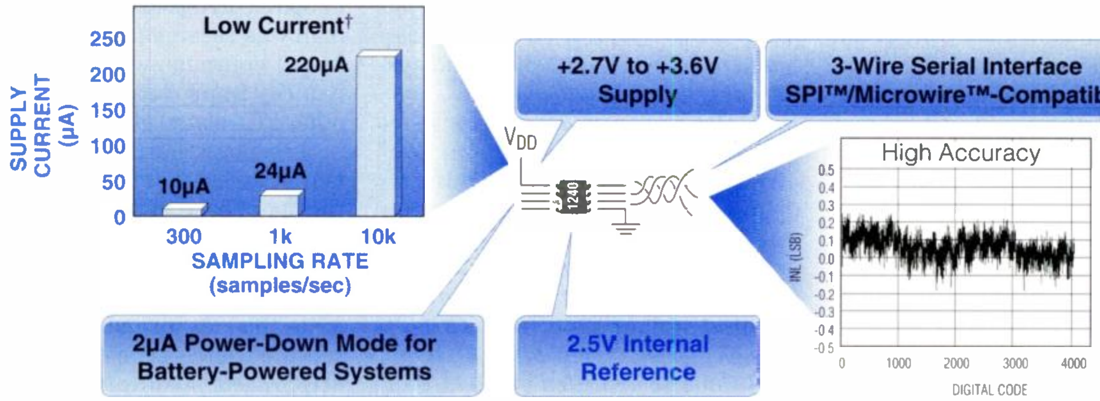

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MAX1241	12	External	73	2.7 to 5.25	2
NEW MAX1242	10	Internal	73	2.7 to 3.6	2
MAX1243	10	External	73	2.7 to 5.25	2

† $V_{REF} = V_{DD}$. Using the internal reference, the supply current at 1ksps is 139µA.
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Readers Respond:

Another Mailbag

This month we take a look at some recent mail sent to this column. While a variety has come in, much of it has been concerned with computer-related issues. "Ouch!" you say? If you're worried that that means another round of computer hardware and tech support horror stories, that's not quite true. This time, we'll touch on some considerations about the computer *operating system* (OS), as opposed to the underlying hardware. But, we'll also focus at greater length on a range of Spice issues.

Windows 95-Related Items: A letter on Windows 95 weaknesses came from an old friend and fellow audiophile, Dave White, of Baraka-Intracom.

Hi Walt.

I found it amusing to read your April 6 Computer Tech Support comments. I wanted to forward a few of my own related experiences.

My office system crashed last week after installing Norton Utilities 3.0, and then would only fire up in safe mode. First, I went through the device manager trying to correct the problem, with no success. Then, I tried reinstalling Windows, but no luck—I kept getting a password error. I was forced to reformat the hard drive and reinstall everything, after trying to backup data files to a floppy in DOS. To say I was unhappy was an understatement.

I don't consider Windows 95 a robust OS. While testing software at my present company (as well as a previous one), we do fresh Windows installs before every software test, as the only way to ensure a consistent environment. To safely run Windows 95 on a system which must keep running, I now follow these rules:

1. Never install software you don't absolutely have to have forever.

2. During install, shut down every single background program (those little lower right-hand corner icons).

3. Never install trial version (time-out) SW. The released version from many SW vendors cannot be installed over the trial version. Plus, you also can end up with constant error messages.

4. Be cautious installing software without an accompanying uninstall program. If you have problems,you may be stuck with it. Always backup your registry files (user.dat and system.dat) before installing.

5. Don't use disk cleanup or move programs, and don't let your "C:" drive get down to less than 100 Mbytes of free space. These cleanup programs are like playing "Russian Roulette" with a fully loaded gun. Any program you install will have a substantial amount of data installed to C:, even though you tell it to install to D:, and it will show as installed on D: in Windows Explorer.

6. Don't install software with automated online upgrade features. I get sick of the windows popping up telling me to upgrade at a $5 per month fee. Why wasn't the software properly done in the first place?

WALT JUNG

As you are aware, Windows 95 uses the registry as the "brains" of the system, and it doesn't take much for it to get corrupted. If you have a lot of software installed and are dependent on your machine, you should take the time to get a book explaining the registry and how to maintain and/or modify it.

Hi Dave! Many thanks for the list of Windows 95 cautions. I can relate to some of your experiences, as several months back I had installed Norton Utilities 3.0, expressly for the touted crash-management recovery features. I didn't have problems at first, but the constant update reminders drove me crazy. It did catch program crashes and prevented lock-ups. Then, more recently, I experienced a hard lock-up from which the Norton Utilities couldn't recover, and I lost some data. I then decided that such limited and costly protection wasn't necessary after all. Bye-bye, Norton Utilities!

Crash management and/or prevention utilities, such as those by Norton, are really symptomatic of basic limitations in the underlying OS. It makes much more sense to me for that system *itself* to be rock-solid—which Windows 95 simply isn't. No user of an OS should ever need to buy books about how the OS stores basic program data, just to be able to recover more quickly from crashes!

Spice Correspondence: Lots of Spice mail was received on the Feb. 9 and May 1 columns, which I consider a healthy improvement over OS and other PC-related glitches!

A reader wrote in regarding a problem accessing the "free Spice" URL in the May 1 column. He may have made a typo. Or, a subtle change of *case* within a typed-in URL can cause things to fail (UNIX systems don't tolerate this). A full and correct URL is repeated here—type it in exactly: *http://www.paranoia.com/~filipg/HTML/FAQ/BODY/F_Free_Spice1.html#FREESPICE_001*

Vacuum Tube Spice Models: Earles L. McCaul of Raytheon Missile Systems wrote about his experiences with vacuum tube and transistor guitar amplifiers, and the desirability for more tube Spice models. It's likely he had no idea what an info avalanche this might unleash...

I read with interest your May 1 commentary on "Spice Programs," and would like to speak up for the "Antiquity-Boys," those of us who <u>still</u> design, work with, and use vacuum-tube equipment, e.g. <u>musicians</u>! There are literally millions of Fender, Mesa-Boogie, Kendricks, etc. guitar amplifiers still in use. So long as the musicians using them perceive these amplifiers as a "part of the musical instrument" process, there will be vacuum tubes around. And, somebody will be needed to design the amps!

As a musician and EE, I've studied and used both tube and transistor amplifiers. At first, tubes were something to be "replaced" by the smaller, lighter, more efficient transistors. Then reality set in, as side-by-side playing showed tubes to be more "warm" sounding and easier to "play into distortion" than were transistor amps. Sure, transistors had more power and less weight, but they didn't sound "familiar." So, they were immediately

Circle No. 202 - For U.S. Response
Circle No. 203 - For International

WALT JUNG

branded "bad" by any and every musician worth his guitar strings. Except for bass amplification, guitarists considered tubes "IN" and transistors definitely "OUT."

What I would like to see is a Spice library suite for the most common vacuum tubes, such as triodes: 12AT7, 12AU7, and 12AX7/7025/ECC83; power pentodes: 6V6GT, 6L6GC, 6CA7/EL34, 6550, and 7027; and rectifiers 5AR4, 5U4, and GZ34. Vacuum tubes aren't dead, they're just DAMN expensive!

In my first response to Earles, I referred him to Marshall Leach's work, among the better known papers on Spice models for vacuum tubes.[1] See Leach's web site at *www.ee.gatech.edu/users/207/* for more information, as well as references to using Spice for other tasks.

I also alluded to several other available sources, which I have now tracked down. Bear with me here, as there is *lots* of Spice info on tubes. Others published are the models by Intusoft,[2,3] and those of Broydé and Clavelier,[4] and Rydel.[5] There also have been some letters on tube Spice modeling, which provide an overview of several approaches.[6,7]

The publication *Glass Audio* has had numerous articles on Spice-based preamp design and related modeling techniques.[8,9] A recent AES paper also discusses an improved model for triodes,[10] and more *Glass Audio* articles and letters address modeling improvements and preamp circuits.[11-13]

Some time after my first correspondence with Earles McCaul, Tom Bruhns of Hewlett-Packard wrote in after reading the second Spice column, and offered some timely modeling advice.

Hi Walt,

Just read your May 1 column in ELECTRONIC DESIGN, and I didn't notice a pointer to: duncanamps.simplenet.com/spice.html.

Duncan has models there that can be hard to find; for example, some vacuum-tube models. He also has lots of pointers to simulators and sources of other models.

I didn't catch your earlier articles, but thought you'd enjoy a really simple circuit example that can cause convergence problems:

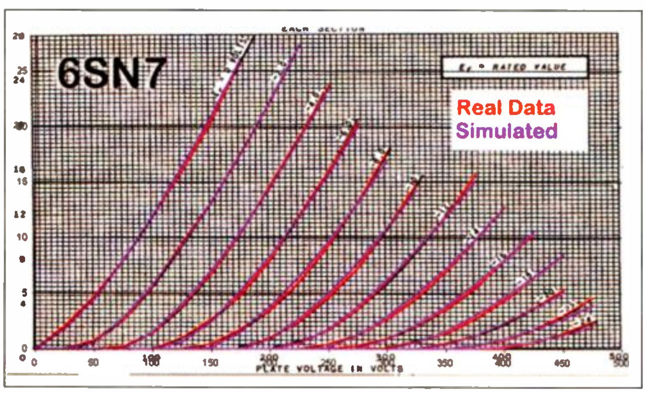
It consists of a series circuit of a step generator (say, 0 V before t = 1 ms and 20 V after), a diode (e.g., 1N4001), an inductor, and a capacitor.

For convenient time scaling, make the LC resonate around 1 kHz. Run a default .tran simulation, then try again with integration=gear. It is just a resonant-charging circuit, but it is also the simplest circuit I've found, which causes Spice to remind me that I still have a head, and it's worthwhile using it!

In standard Berkeley Spice3f5, and in other Spices I've tried, default integration results in oscillation of the voltage between the diode and inductor. Adding resistance in various places doesn't seem to help it converge, at least if the resistance is high enough (or low enough, if in series) to not ding the Q too much. Gear integration makes it behave.

I find Spice to be a very good tool to ensure that I put appropriate thought into my circuits. Sometimes running a simulation points out shortcomings of Spice, sometimes shortcomings of the macromodels (when used), and sometimes shortcomings of the circuit itself. But all that's OK, as my head can sort it out just fine. I value all inputs early in the design. And, sometimes it's been valuable late in the design, too. I've used Spice with very abstracted models of my circuit to analyze performance of nonlinear feedback systems, and it has saved me huge amounts of bench time.

Thanks for the input, Tom. I found Duncan Munro's web site to be quite a treat, as not only does he have online many of the models that Earles McCaul requested, but lots of other info as well. See the Figure for Duncan Munro's 6SN7 plots. As you most likely know, you can sign up for e-mail notification on model updates as they appear. Also, thanks for your insights using Spice as one element of an overall design.



I noted that some of Duncan Munro's models exist in PSpice, as well as 3f4 formats. For those wondering about what seems like duplication, this arises from the existence of some very useful functions within PSpice, which aren't available in more generic Spice versions. Duncan explained it thusly:

These (functions) are ones that I specifically use with my models, and are not available in either 2g6 or 3f4; they are purely proprietary to PSpice:

".PARAM"—allows parameters to be passed, "LIMIT(x,min,max)"—to constrain a value.

There is no way round the lack of .PARAM in 2g6 or 3f4. If you refer to the PSpice file, you will see that two models have been written, and all of the tube types come from parameters being passed. Nice and neat.

In the 3f4 version, you will see that each model is described individually. In actual fact, they are all exactly the same model; it's just that some of the parameter values in them are different.

TIP: The list of various vacuum tube Spice model references below is by no means a complete list. While reasonably extensive, it also can be expanded considerably from citations within. You also can supplement your info on Spice via the web, by doing an AltaVista search: *www.altavista.digital.com/*. Use a search entry of +"vacuum tube" +spice, and you'll get enough hits to keep you busy for some time.

I Meet *ELECTRONIC DESIGN* Readers: In the May 1 column, I had a brief note about hoping to meet some of the column readership at upcoming seminars. Now that the tour is over, I'm happy to say that more than a few folks did stop by to say hello, identifying themselves as column readers. My thanks, first for reading the column, and second, for stopping by and saying hello. It was a real treat to meet some of the readership firsthand.

As always, reader comments are invited on Spice (or other) topics. Enjoy not just the reading, but also

WALT JUNG

those warm tube sounds !

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5. C. Rydel, Simulation of Electron Tubes With Spice," Preprint No. 3965, Presented at 98th AES Convention, May 1995.
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11. John Harper; Norman Koren, "Spice It Up; author's reply," *Glass Audio (Letters)*, Vol. 10, No. 1, 1998.
12. Stefano Perugini, "A PSpiced Preamp With THD Cancellation," *Glass Audio*, Vol. 10, No. 2, 1998.
13. Jean-Charles Maillett, "Algebraic Technique for Modeling Triodes," *Glass Audio*, Vol. 10, No. 2, 1998. (see web site with triode and rectifier models at *www.lynx.bc.ca/~jc/tubes.html*)

Walt Jung is a corporate staff applications engineer for Analog Devices, Norwood, Mass. A long-time contributor to ELECTRONIC DESIGN, *he can be reached via e-mail at: Walt_Jung@CSI.com.*

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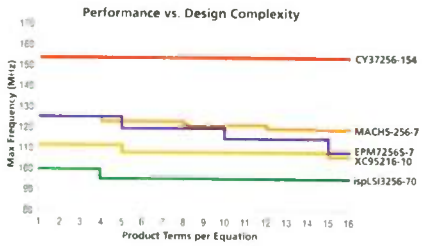

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CY37128	128	6.5	167	133	TQFP, PLCC
CY37192	192	7.5	154	125	TQFP, PLCC
CY37256	256	7.5	154	197	TQFP, PQFP BGA
CY37384	384	7.5	154	197	PQFP, BGA
CY37512	512	7.5	154	269	PQFP, BGA

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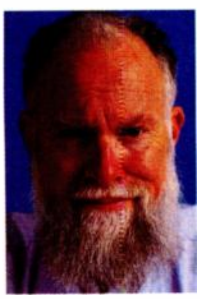
BOB PEASE

What's All This Circuits-In-Your-Car Stuff, Anyhow?

Hip, hip, hooray. Pease is *finally* going to talk about electronic circuits. So many of these recent columns have been about things that have nothing to do with electronics. True...Sorry about that. Well, I have been designing lots of circuits, but a lot of them I can't talk about. I can't talk about a circuit we are developing and planning to sell. I can't talk about circuits that we are patenting. There's lots of things that I can't very well talk about. But these circuits here are NOT confidential. You might call them chicken-manure circuits, but they do work OK. They are useful, and not completely obvious. I have never seen them in print. Even though these circuits are not very sophisticated, if applied in a useful way, they can be very valuable.



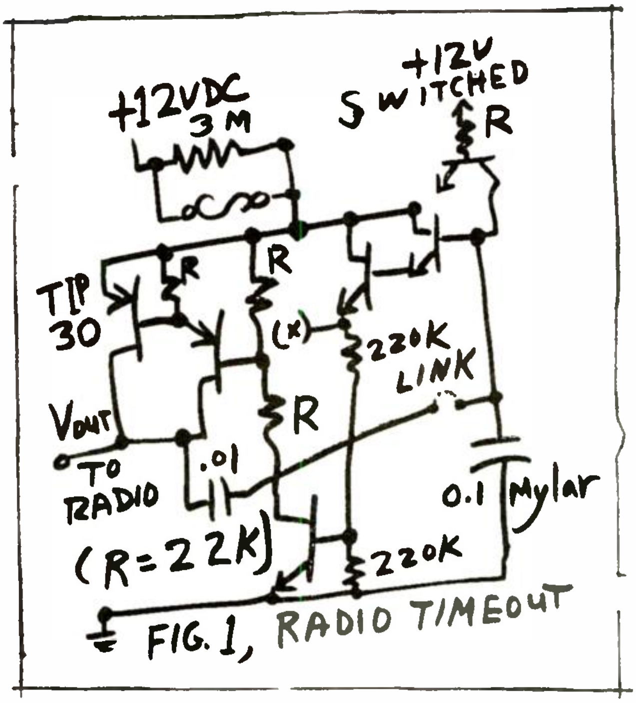
BOB PEASE
OBTAINED A BSEE FROM MIT IN 1961 AND IS STAFF SCIENTIST AT NATIONAL SEMICONDUCTOR CORP., SANTA CLARA, CALIF.

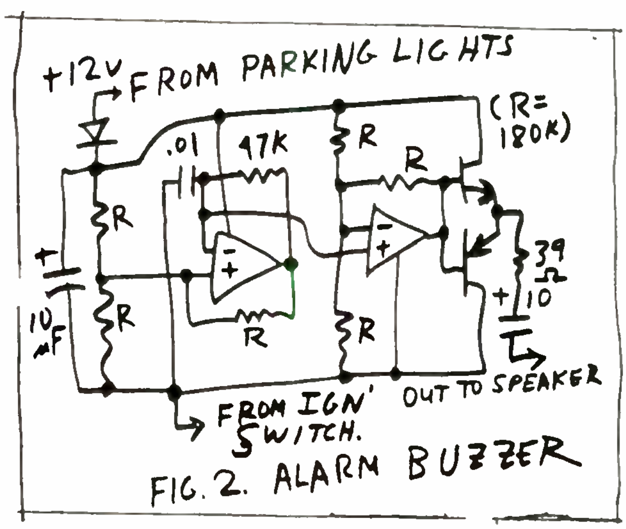
Would you like me to write about all the U.S. patents I have? I could do that. Many of them are circuits. **Circle 550** on the Reader Response Card if you think I should do that. I was *really sure* I had 15 U.S. patents, but the last time I checked, I had 16. I have no idea how that extra one crept up on me. I'm working on two others that might be out in a year or so.

Just one caution: if you are trying to search at the U.S. Patent Office to find out the patents of an inventor, and type in: IN/"Jones Jr.; John."—you can't find anything, even if "John Jones Jr." has a patent. Their search engine can drive you wild. You have to type in a *comma* after Jones, and *then* they will lead you to the patent.

But, today I will talk about the circuits I am putting in my "new" car. These days, there are microprocessors and circuits everywhere, in most new cars. That is probably half the reason I prefer to buy a not-so-new car. Some guys have asked me, "How can I protect my car so it will not be disabled by an ElectroMagnetic Pulse?" I tell them it's easy—just buy an old car.

Chimes: I am always amused when I rent a car with chimes. I don't want to BUY one, or to OWN one, but it's fun to drive one, for a change. Some cars have chimes to warn if you are leaving your keys in the car when you open the door. Or if you leave your directional signals blinking absent-mindedly for too long. I am always reminded of the story of the man who gave out an awful belch. A very proper lady nearby was horrified, and she said so. He responded, "Exactly what were you expecting? Chimes?" Modern cars have circuits to turn chimes and lights on and off, circuits to run your ignition and your fuel injection, and 999 other things. Some high-end cars have dozens and dozens of 'processors'... but not the one I just bought (a relatively new, 1970 VW Beetle).





I got a radio. I think it has eight transistors. It doesn't run very well. Flakey. I'm gonna rip it out and put in one that has 10 transistors. I got ignition points that open every time I need to fire a spark plug. I got a coil. I got a horn. I got lights. I got electricity.

BOB PEASE

So, what *electronic* circuits am I going to add to my latest car? Look for a horn-rattler, alarms, reminders, timers, radio turn-off, etc.

Radio turn-off: Sometimes I like to sit in my car and listen to the radio, with the ignition off. But I don't like to just leave the +12-V dc power on permanently for the radio because it could easily run the battery down, if I forget to turn it off. So, I put in a timer that turns the radio off a couple minutes after the key is turned off.

Refer to the circuit in Figure 1. I have built about four versions of this circuit, for various cars. It works OK for me. So, I just built another one for my new red Beetle. Hey, I never had a red Beetle before.

How does it work? When the ignition is ON, the transistor at the upper right acts as a diode and keeps the 0.1-µF cap charged up. All the transistors are turned ON. When the ignition is turned OFF, that capacitor is discharged down in a couple minutes, by the base current of the transistors—perhaps 5 or 10 nA. When the voltage on the cap gets low enough, all the transistors turn off, and the radio turns off. The positive-feedback capacitor (0.01 µF) is optional.

Maybe this time I'll build it without that, to minimize the *click*. No, I will solder in the capacitor on one end, but I won't connect it—so I can easily change my mind.

When I built this circuit in June, the shut-down time was more than 10 minutes, so I had to put a 27-kΩ resistor from the emitter of the Darlington, at "x," to ground, to get the delay near three minutes. The NPN betas were too high.

I've built this basic circuit with a PNP Darlington output driver, and a PNP-NPN, and a big Germanium PNP that came out of a Minuteman I nose-cone. Most of these schemes have an ON voltage of about 0.9 V at 1 A, and that's OK with me. If I needed a better switch, with lower ON voltage, I could drive the gate of an N-channel MOSFET to +23 V. But, since that is not a big deal, I've never done it.

The "3-MΩ resistor" is just a place where I solder up a single strand from a stranded wire, to act as a fuse. If the fuse blows, I'd swap in another 3-MΩ resistor—with a new strand.

Of course, in all these circuits, *unless otherwise noted*, NPNs are 2N3904 or similar; PNPs are 2N3906 or similar; resistors are ±10%, and diodes are 1N914/1N4148.

Headlight reminder buzzer: See Figure 2. It is so easy to turn on your headlights or parking lights and forget to turn them off, that I really need this buzzer. On a rainy day, it is a VERY good idea to turn your headlights ON. But it is also a good idea to turn them OFF. I just connect this circuit between a parking-light fuse and the ignition switch. So, if the lights are left on when the ignition is turned off, I will be reminded.

I like to make this a 1.5-kHz triangle wave, so if I have to leave my lights on, the buzzer will not annoy me to death. I typically feed this signal into one of my car's speakers, through 39Ω in series with 10 µF.

Burglar alarm, Mode I: Type this up and print it out, and tape it to each rear window: "IF ALARM SOUNDS, call 911, or call (Your home phone number), or call (your work phone number)." That's what I do. If a car thief or robber wants a reason to pass over your car, this should give him a good reason to look elsewhere.

Burglar Alarm, Mode II: I connect a detector to my indoor light switch, so when a door is opened, a sequence begins: there is a wait of four seconds. Then a LOUD beeper starts. After four more seconds, it starts blowing the horn. This is enough to chase most car thieves away. Schematic not shown, but you could easily figure it out yourself.

Burglar Alarm, Mode III: I built up a timer that is very useful. When I leave the car, I just set it to run. It blinks for a while and then turns itself OFF. I don't know very many people who are stupid enough to break into a car where all sorts of winken-stinken-blinken is going on. In my next column, I'll write about some more circuits.

All for now. / Comments invited!
RAP / Robert A. Pease / Engineer
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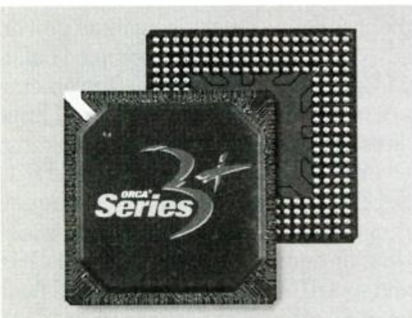
Field-Programmable Gate Array Combines Dedicated PCI Core And Programmable Logic

Although FPGAs provide designers with plenty of flexibility, they're sometimes hard-pressed to deliver high-speed operation for complex functions. To rectify that problem, Lucent Technologies has combined a high-performance dedicated function (i.e., a 66-MHz PCI core) on the same chip with its latest-generation programmable logic technology. Called the ORCA 3TP12, its the first in a family of merged dedicated core and FPGA logic circuits.



The PCI core is designed from the ground up, and is fabricated in the silicon—it's not just a pre-wired collection of FPGA gates.

By creating a ground-up implementation, designers were able to integrate many features in the PCI core, including large buffer memories, that would be impractical if implemented with FPGA gates and embedded SRAM blocks. The company also plans to introduce additional merged core and FPGA chips. At this point, though, it hasn't committed to the specific function that will be integrated with the FPGA logic.

The full-featured PCI core and buffers occupies about one quarter of the original 18-by-18 logic cell array contained on the OR3T55 FPGA chip. Four rows (4 by 18) are replaced by the PCI core (about 7800 FPGA gates), which actually contains about 75 kgates—almost a 10-fold denser block due to the use of standard cell and standard ASIC design approaches. The remaining FPGA section contains about 30 to 60 kgates of logic. The PCI core complies with version 2.1 of the PCI specification and can automatically detect whether it's in a 5-V or 3.3-V PCI bus system. It also automatically provides the appropriate I/O signal levels.

In addition to providing a full bus master or target PCI core function, the core can be configured for either a 64- or 32-bit PCI interface. Included in the block are two 32-word by 64-bit master FIFO blocks, and two 16-word by-64-bit target FIFO blocks (in the 64-bit mode), which allow designers to select the desired amount of I/O buffering for the system under design. When configured as a 32-bit PIC interface, the buffers are configured as 64 words by 32 bits for the master read and write functions, and 32 words by 32 bits for the target read and write functions.

The PCI block can deliver no-wait-state full-burst PCI transfers in either direction. Between the chip's PCI core and the FPGA logic is an interface area that makes the core signals look like Series 3 family I/O lines, which makes it easy to configure the interface. The FPGA logic portion of the chip can be programmed through the PCI interface. Therefore, when a system starts up, it appears as a simple PCI interface. The chip's programmable logic contains the same logic blocks as on the company's previously released Series 3 family chips. It includes features that allow designers to create wide logic functions (decoders and PAL-like functions) typically implemented with CPLDs. In addition, the FPGA architecture includes a predesigned interface that can directly tie into either the Intel i960 or Motorola PowerPC style CPU buses.

Depending on the desired PCI-bus interface, the ORCA 3TP12 can be ordered in 240-lead shrink QFPs, or 256- or 352-contact BGA packages. Samples of the chip are immediately available and come in three speed grades, all of which will meet the 66-MHz PCI speed requirements. For the 240-lead version, expected volume pricing in the fourth quarter is $79.80 each in lots of 25,000 units.

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CIRCLE 553
DAVE BURSKY

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The CATC FireInspector IEEE 1394 Bus & Protocol Analyzers are designed for 1394-based product development and testing. At the heart of CATC's FireInspector 1394 analyzers is the FireEngine core. This core uses PLD technology to incorporate both a high-speed recording engine and configurable building blocks. The new analyzers feature full IEEE Std. 1394-1995 and P1394a compliance, support of transfer rates to 400 Mbits/s, 128 Mbytes of recording memory, real-time event triggering and capture filtering, accurate time-stamping and search and analysis capabilities. Graphical displays illustrate bus transactions and connection topologies.The basic FireInspector analyzer is available immediately for $15,950; the FireInspector Plus version (including bus traffic generation) goes for $19,950. JD

***Computer Access Technology Corp.**, 2403 Walsh Ave., Santa Clara, CA 95051-1302; (408) 727-6600; fax (408) 727-6622; www.catc.com* **CIRCLE 554**

READER SERVICE 137

Spectrum Analyzer Operates At Up To 30 GHz

The MS2667C spectrum analyzer covers a frequency range of 9 kHz to 30 GHz. The unit is designed for analyzing signals used in point-to-point and point-to-multipoint microwave radio networks at the R&D, manufacturing, and maintenance stages. Built-in measurement functions include channel power, adjacent channel power, occupied bandwidth, and noise power. Measurements are conducted automatically and limit lines are available for pass/fail testing. Overall level accuracy of the MS2667C is ±2.3 dB over the entire frequency range. Phase noise performance is less than or equal to –95 dBc/Hz at 1 GHz and –83 dBc/Hz at 30 GHz. Noise floor performance is less than or equal to –115 dBm at 1 GHz and –91 dBm and 30 GHz. JD

***Anritsu Co.**, 1155 East Collins Blvd., Richardson, TX 75081; (972) 644-1777; fax (972) 644-3416.* **CIRCLE 555**

Benchtop Supplies Are GPIB-Programmable

The Model 1770/1775/1780 power supplies can be regulated via the GPIB programming interface or the front-panel keypad. The three new models feature a selection of voltages from 0 to 35 V and current from 0 to 6 A. Internal software enables the power supplies to be calibrated in the case, eliminating the need for third-party adjustments. System software sends calibrated constants for output voltage and current to the supply via the front-panel keys. The supplies then can be calibrated using a shunt resistor and accurate voltage meter. Output of the 1780 ranges from 0 to 18 V dc and 0 to 4 A; the 1775 goes from 0 to 35 V dc and 0 to 2 A. The supplies are priced from $950 (Model 1770) to $1350 (Model 1780). JD

***B&K Precision**, 1031 Segovia Circle, Placentia, CA 92870; (714) 237-9220; fax (714) 237-9214; Internet: www.bkprecision.com.* **CIRCLE 556**

Vertical Gyro Exploits MEMS And DSP Technologies

Combining a silicon micromachined accelerometer with 32-bit floating-point digital signal processing (DSP) and proprietary algorithms, Crossbow Technology has developed a true solid-state vertical gyro. It quickly and accurately measures roll and pitch in dynamic environments.

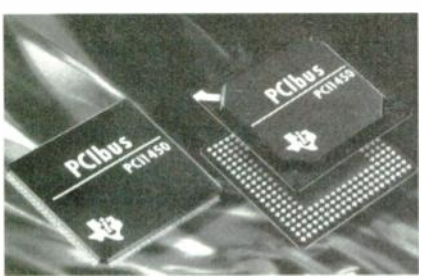
According to Crossbow Technology, the latest vertical gyro DMU-VGX delivers a more cost-effective solution than its mechanical predecessors. For example, it offers accurate acceleration and angle measurement in applications like camera and antenna stabilization, automotive testing, marine motion monitoring, and unmanned vehicle orientation sensing and stabilization. In essence, the DMU-VGX is an intelligent 6-axis inertial measurement system that outputs X,Y, Z, roll, pitch, and yaw information with instantaneous power-up and high sampling rate.

While many mechanical sensors have a mean-time between failure (MTBF) of only 500 hours, the DMU-VGX offers an MTBF of over 50,000 hours, claims Crossbow Technology. Packaged in an aluminum housing that measures 3.00 by 3.375 by 3.25 in., the DMU-VGX uses a single 8-30 V dc supply and consumes 250 mA maximum current. A single unit price is $4000. AB

***Crossbow Technology Inc.**, 41 East Daggett Dr., San Jose, CA 95134; (408) 324-4830; www.xbow.com.* **CIRCLE 557**

CardBus Controller Supports Power Management Specs

Texas Instruments' PCI1450 is a new two-slot controller chip for PCI bus-to-CardBus interface. It conforms to



the PCMCIA's CardBus power-management specifications. Featuring a parallel pipelined architecture, it can transfer data across the PCI bus at approximately 132 Mbytes/s. The chip supports hot insertion and removal of CardBus or PC card modules. In addition, it provides an internal zoom video capability that transfers graphic data directly to the system's graphics processor without using the PCI bus, thereby easing the load on the PC's PCI bus. According to Texas Instruments, the PCI1450 will be fully supported by all versions of the Windows operating system. Sampling begins in the third quarter, with production slated for the fourth quarter. The PCI1450 comes in a 256-pin ball-grid-array (BGA) package. It's priced at $14.50 in quantities of 10,000. AB

***Texas Instruments Inc.**, Semiconductor Group, SC-98023A, Literature Response Center, P.O. Box 17228, Denver, CO 80217; (800) 477-8924, ext.4500; www.ti.com.* **CIRCLE 558**

Layer-3 Switch Engine And MAC Chips for Desktops, Workgroups

Cost-effective layer-3 Fast Ethernet switches can be easily implemented using the XpressFlow 2020 line of 10/100-Mbit Ethernet switch chips, the SC220 XpressFlow Engine and their companion EA234 4 Port Fast Ethernet Access Controller. The XpressFlow 2020 product line allows switch manufacturers to offer more feature-rich products. Both chips operate using a 2.1-Gbit/s bus with a distributed memory architecture that supports up to 24 10/100-Mbit/s ports or 48 10-Mbit ports. The products support a system bill of materials (including enclosure and power supply) cost of less than $29 per port for managed Layer 3 10/100 switches in high volumes.

The SC220, which is the switch engine chip of the XpressFlow 2020 chip set, is designed to handle IP packet address resolution, packet forwarding, and communication with the management processor. Improved performance from the embedded RISC processor, combined with the ability to support up to four SC220s in a design, results in the ability to route packets at 200k to 800k packets/s, and switch Layer 2 packets at up to 1.8M packets/s.

The EA234 4 Port Fast Ethernet Access Controller provides four 10/100-Mbit/s Ethernet access ports, and is responsible for buffering data and handling Ethernet MAC protocols. Internal hardware provides buffer management for an external SBRAM, enabling the EA234 to support full wirespeed 100-Mbit/s transfers.

Samples of the XpressFlow SC220 XpressFlow Engine and the EA234 4 Port Fast Ethernet Access Controller will be available June 12. Pricing in quantities of 10,000 is $42 for the SC220 and $59 for the EA234. LG

***Vertex Networks Inc.**, 16842 Von Karmen Ave., Suite 250, Irvine, CA 92606; (949) 252-8880; Internet: www.vertex-networks.com.*
CIRCLE 559

ATM Signaling Software Handles 7200 Calls Per Second

An enhanced ATM signaling software package is now available that can make over 7200 calls per second while also maintaining the interoperability and flexibility that computer and communications equipment manufacturers require. The software was designed to accommodate the needs of switch and test equipment manufacturers who require high-performance call rates,but can't sacrifice the flexibility to handle multiple ports, change the characteristics of ports dynamically at run-time, or selectively process message elements.

The new ATM signaling software, meets the requirements and includes the Q.93B and Q.SAAL protocol layers. The software's dynamic architecture enables service providers to configure or reconfigure links dynamically at run-time. The software package price starts at $60,000, depending on options. LG

***Trillium Digital Systems Inc.**, 12100 Wilshire Blvd., Suite 1800, Los Angeles, CA 90025; (310) 442-9222, fax (310) 442-1162, www.trillium.com; e-mail: sales@trillium.com.* **CIRCLE 560**

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FAX: (216) 696-8206

CAREER OPPORTUNITIES

SR. P.C.B. DESIGN ENGINEER. 45 HRS/WK. 8:30am-6:30pm; M-F, OT as nec., $48,254/yr. 2 positions avail. Design and engineer p.c.b.s and provide fabrication and assembly consultation using Encore PCB, Calay, Orcad, Mentor, CCT Autorouter, View Logic, Solaris, Windows 95, and Autocad, and requiring analog, U.L., digital, and high speed design. Requirements: MSc in Electrical Engineering or Electronics, and 2 yrs. exper. in job offered or 2 yrs. exper. as Electronics Engineering. 2 yrs. exper. must include design of p.c.b.s in analog, digital, and U.L. and use of Orcad, Calay, Scicards or Encore, and Windows. Must have proof of legal authority to work permanently in the U.S. Send resumes to: Illinois Department of Employment Security, 401 S. State St. - 7 North, Chicago, IL 60605, Attn: Len Boksa, Ref #V-IL 18575-B. An employer paid ad. No Calls -- send 2 copies of both resume and cover letter.

OI Analytical

A corporation that specializes in the research, development, manufacturing, and marketing of analytical instrumentation for chemical analysis is seeking individuals for the following positions:

Mechanical Design Engineer to analyze product requirements, develop design proposals, and produce detailed mechanical designs and drawings. Requires a BSME with 3 years experience including new product specification development, component design, assembly drawings, electro/mechanical design, and AutoCAD R13.

Electrical Engineers (2) to analyze system requirements, develop electro-mechanical system designs, design PCAs/PCBs, and implement and test designs in instruments. Requires a BSEE with experience including digital and analog design, electro-mechanical systems design, and software programming in an embedded systems environment. The senior position requires 5+ years experience, and the junior position requires 1+ years experience.

Windows/C++ Programmer to analyze applications requirements and generate Windows-based programs using development tools and C/C++ compiler. Requires a BS in a relevant field and 2 years experience in a Windows programming environment, C++ experience a must. Experience with analytical instrumentation a plus.

Must have excellent communication skills, strong self-motivation, and the ability to work in a team environment. Must be willing to relocate to Bryan/College Station, TX. For confidential consideration, please send resume to OI Analytical, Personnel Dept., P.O. Box 9010, College Station, TX 77842-9010 or fax resume to (409) 690-0440. EOE.

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3VDC/100MA	CX099	$0.75
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FREE CATALOG!

ELECTRONIC DESIGN CATALOG/LITERATURE REVIEW

FREE APPLICATIONS CD

This applications CD is designed to help system designers make the most of their available space using Vicor power components. It includes the Vicor Applications Manual, seven product configurator programs, and the complete selection of downloadable Vicor product data sheets. (800) 735-6200; Fax: (978) 475-6715; www.vicr.com

CIRCLE 248

VICOR CORPORTATION

IC DESIGN SOFTWARE

Tanner EDA offers innovative, feature rich yet easy to use software solutions for custom and semi-custom IC design entry, simulation, layout and verification on Windows platforms, all at cost-effective prices. With ten years of experience producing EDA software for the PC, we offer an outstanding price-performance combination. www.tanner.com/eda; (626) 792-3000; info@tanner.com.

CIRCLE 249

TANNER EDA

1998 Data Acquisition Boards Catalog

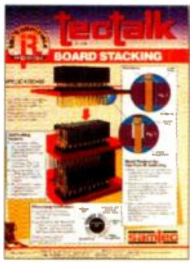
New 48 page, 1998 supplement catalog from DATEL SYSTEMS offers a wide range of high performance and general purpose Data Acquisition boards. Over 50 new products are offered including advanced performance boards for PCI, ISA and VME bus. For additional information or to request a catalog contact us at: 800-233-2765, URL: www.datel.com; e-mail: datellit@datel.com.

CIRCLE 250

DATEL SYSTEMS

IR Processing Through-Hole Connectors

A common problem with soldering mixed technology boards and self-nesting sockets is the inability to place sufficient solder paste necessary to wet the lead without hand-soldering or secondary reflow operations. This issue has been resolved by Samtec and is addressed in their new tectalk no. 9804: SMT Compatible Through-Hole Board Stacking. 800-SAMTEC9; Fax: 812-948-5047; www.samtec.com

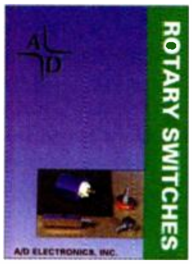


CIRCLE 251

SAMTEC USA

ROTARY SWITCHES

A/D Electronics' free Rotary Switches catalog features a variety of rotary switches in different configurations. The design engineer can obtain complete specs, dimensional drawings and evaluation samples upon request. A/D Electronics also supplies a variety of interconnects for the OEM. Support is available by contacting A/D Electronics. (253) 851-8005; fax: (253) 851-8090; www.adelectronics.com.

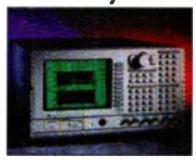


CIRCLE 252

A/D ELECTRONICS

Dual Channel FFT Spectrum Analyzer

The SR780 is a two channel FFT analyzer with a freuqency range of 102.4 kHz and a dynamic range of 90 dB. Features include ANSI standard octave analysis, swept sine measurements, transient capture, and computed order tracking (opt.). The SR780 comes with a low distortion source (-80 dBc), 8 MB of memory (up to 32 MB opt.), a 3.5 inch DOS disk drive and RS-232 and GPIB computer interfaces. (408) 744-9040.

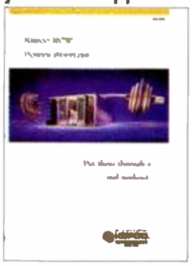


CIRCLE 253

STANFORD RESEARCH SYSTEMS

Kepco RCW Heavy-Duty Power Supplies

Six pages of detailed data on RCW Power Supplies. RCW are heavy-duty, single output, industrial grade d-c power supplies. Available in five sizes, 100, 175, 350, 750 and 1500 watts, they are enclosed modules. Excellent stabilization, low ripple. Voltage stabilization with current limiting.www.kepcopower.com/rcw.htm; (718)-461-7000; Fax: 718-767-1102; e-mail: hq@kepcopower.com.



CIRCLE 254

KEPCO, INC.

FREE PCB DESIGN DEMO CD!

ACCEL Technologies' ACCEL EDA electronic design automation software for designers of analog, digital, and mixed-signal printed circuit board designs. Schematic capture, simulation, PCB layout, high-performance autorouting, placement, signal integrity, CA, documentation. Call 800-488-0680 or 1 619 554-1000 for FREE multimedia demo CD. E-mail: sales@acceltech.com; www.acceltech.com/electronic.html.

CIRCLE 255

ACCEL TECHNOLOGIES

STANDARD-SETTING LEAD ACID BATTERY

Described in new color brochure from Yuasa-Exide. New brochure details Dynacel DDH modular valve-regulated lead acid (VLRA) battery, which comes in 24V and 48V versions, rated 120 Ah to 6000 Ah (three-parallel string configuration) and up to 2000 Ah battery (non-parallel string. Battery features include a Skate-Key™ compression system for faster installation. 800-538-3627; Fax: 610-372-8613; e-mail: andreaf@ptd.net; www.yuasa-exide.com.

CIRCLE 256

YUASA-EXIDE

FAST TURNAROUND PROTOTYPES

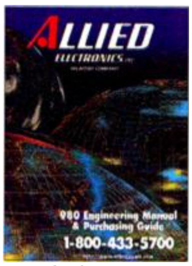
Accutrace offers the Best Quality along with Excellent Service and Best Turnaround Time. Our capabilities include SAME DAY Prototypes, Instant Quotes, SMOBC & LPI, Scored Panels, Electrical Testing, SMT & Thru Hole, Complete CAD/DFM, Gold/ Nickel Plating, Blind & Buried Vias, UL Approved and more. e-mail: info@accutrace.com
Tel: 408-748-9600,
Fax: 408-748-1982

CIRCLE 257

ACCUTRACE INC.

ELECTRONICS ENGINEERING MANUAL

Allied Electronics Engineering Manual & Purchasing Guide contains reference data plus electronics from over 275 manufacturers. The Allied Catalog is available on CD-ROM. Allied Electronics is an Avnet Company with access to hundreds of millions of dollars of inventory. This breadth and depth gives you service capabilities found only at Allied Electronics, Inc. http://www.allied.avent.com; 1-800-433-5700.



CIRCLE 258

ALLIED ELECTRONICS

FREE VHDL SIMULATOR

Aldec, Inc., announces the release of Active-VHDL version 3.1 a complete VHDL design environment. Active-VHDL is a complete IEEE 1076-93 VHDL design environment, including a VHDL editor, Behavioral Simulator, Automatic Test Bench Generator, interface to logic synthesis & FPGA/CPLD vendor P/R tools, VHDL design browser & Structural VHDL simulation. (800) 487-8743; (702) 456-1222; www.aldec.com

CIRCLE 259

ALDEC, INC.

SuperTAP™ Emulator for x86

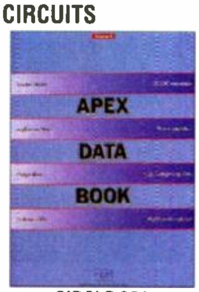
The new standard in high-end in-circuit emulators, SuperTAP solves tough hardware/software integration problems, debugs firmware and software, maximizes embedded system quality and performance. Palm-sized, full processor speed, easy set up, at half the price of chassis-based emulators 1-800-426-3925.

CIRCLE 260

APPLIED MICROSYSTEMS

POWER INTEGRATED CIRCUITS

The 7th edition Apex Power Integrated Circuits data book contains complete product data sheets and applications notes for Apex Microtechnology's power Amplifier PWM Amplifier and DC/DC Converter product lines.
Call: 1-800-862-1021; Fax: 1-520-888-3329 Email: Prolit@TeamApex.com



CIRCLE 261

APEX

ENCLOSURES & ACCESSORIES

Bud Industries' new Standard Products Catalog provides technical data and ordering information on over 3,000 products ranging from large relay racks and cabinets to desktop and portable instrument cases including a full line of NEMA and other plastic enclosures. Also included is information on computer workstations, custom fabrication and a wide range of enclosure accessories.

CIRCLE 262

BUD INDUSTRIES, INC.

ELECTRONIC DESIGN CATALOG/LITERATURE REVIEW

New & Expanded Crystal Oscillator Catalog

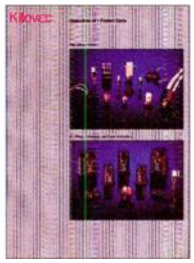
Champion Technologies' new crystal oscillator catalog and selection guide features technical information, electrical specifications and mechanicals for its newly expanded offering of frequency control products. Catalog provides detailed information on Champion's low cost clock oscillators and VCXOs, plastic SMT clocks, SMT VCXOs and TCXOs and high frequency TCXOs. 847-451-1000 or 800-888-1499, Fax: 847-451-7585. Website: www.champtech.com

CIRCLE 263

CHAMPION TECHNOLOGIES, INC.

HIGH VOLTAGE RF & DC RELAY CATALOG

Product Guide from Kilovac, a division of CII Technologies, features a broad line of high voltage RF & DC power relays and contactors. Feature ratings and specifications on relays up to 70 KV including QPL. Choose from 28 Vdc 270 Vdc aerospace power relays, contactors and power controllers. Industrial contactors to 750 Vdc. Contact: Pat McPherson, 805-684-4560; 550 Linden Ave., Carpinteria, CA 93013.

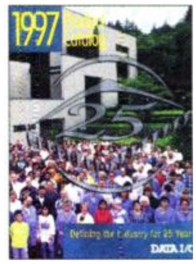


CIRCLE 264

KILOVAC Div. of CII TECHNOLOGIES

DEVICE PROGRAMMERS & HANDLERS

The Data I/O catalog is the direct-order source of affordable tools for users of programmable devices. From design software to device programming and automated handling systems, the Data I/O catalog offers unbeatable values on the high quality tools you need. Call 1-800-332-8246, ext. 806

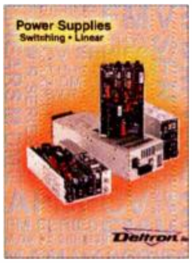


CIRCLE 265

DATA I/O

NEW OEM POWER SUPPLY CATALOG

Deltron's full line catalog presents many new products including 1kW to 7.5kW T Series power factor corrected front ends for telecommunications systems, DeviceNet power modules, new generation modular F Series 0.99 power factor corrected switchers and Moduflex® M Series switchers. The catalog also details a full complement of time tested hi-grade industrial and commercial power supplies. For free copy call 800-523-2332 or fax 215-699-2310.



CIRCLE 266

DELTRON

INTERCONNECT SOLUTIONS

This catalog enables design engineers to easily locate the correct adapters, clips and test accessories. The catalog includes a Ball Grid Array Reference Guide along with information on over 4000 ET products, including emulator tools, logic analyzer/scope adapters, programming adapters, production/test adapters, debugging accessories, prototyping adapters, field-configurable adapters and custom adapters. 1-800-ADAPTER www.emulation.com

CIRCLE 267

EMULATION TECHNOLOGY INC.

MINIATURIZED POWER SUPPLIES

EOS Corp. offers a complete line of miniaturized switching power supplies, from 24 Watts to 100 Watts, both internal and external. For example: 100 Watts in a very small 1" x 3" x 5" form factor, convection cooled! Call 805-484-9998. www.eoscorp.com

CIRCLE 268

EOS CORP.

FREE SRAM CATALOG

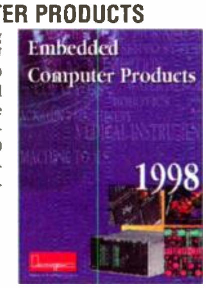
Galvantech, Inc. designs, manufactures and markets high speed, high performance static random access memories (SRAMs). A broad product line includes 1-meg, 2-meg and 4-meg densities available in both asynchronous and synchronous versions.

CIRCLE 269

GALVANTECH, INC.

EMBEDDED COMPUTER PRODUCTS

Gespac's 1998 catalog features a full line of 3U embedded PCs, 68XXO SBCs, motion control and over 200 I/O functions. The G-windows GUI for real-time systems running. OS-9 is also offered. www.gespac.com or Phone 800-443-7722



CIRCLE 270

GESPAC INC.

A WEALTH OF SWITCH INFORMATION

Grayhill's 320 page catalog provides you with electromechanical switch data, reference material, dimensional drawings and photos. Catalog No. 1 includes information on DIP Switches, Rotary Switches, Keyboards and Keyboard Modules. The detailed information allows the catalog uses to select the proper product for their appliction right down to the part number. Phone: (708) 482-2131, Fax: (708) 354-2820.

CIRCLE 271

GRAYHILL, INC.

INDUSTRIAL PC POWER SUPPLY

ICP Acquire Inc. is a manufacture of single Board computers, provide Backplane, rackmount chassis , and Industrial Power supplies. Including: 3-20Slot BP, 386/486/Pentium SBC, 3-20Slot chassis, DC-12V/24V-48V PS and 85-265V AC PS. Contact Allen, phone: 650-967-7168

CIRCLE 272

ICP ACQUIRE, INC.

ILLINOIS CAPACITOR CATALOG

This new catalog features three new product lines and many additions to existing lines. Contains complete information on the company's axial and radial lead aluminum electrolytic, film, ceramic and power capacitors. It's all you need to make a knowledgeable capacitor selection. Contains full specifications, useful formulas and data, authorized distributor listings. 144-pages. 847-675-1760; fax 847-673-2850

CIRCLE 273

ILLINOIS CAPACITOR, INC.

WE SHIP PROTOS SAME DAY

Imagineering specialized in FAST TURNAROUND, High Quality. Multi-layer, FR4 PC Boards. Other Services include SMOBC & LPI, Bare Board Electrical Testing. Gold/Nickel Plating, Scored Panels, Blind & Buried Vias. Complete CAD/DFM Service. UL approved and more. e-mail: info@imagineering_pcb.com Tel: 847-806-0003 FAX: 847-806-0004.

CIRCLE 274

IMAGINEERING

DSP AND DATA ACQUISITION

Innovated Integration manufacturers of high-performance DSP cards with extensive I/O capabilities for ISA, PCI, Compact PCI and stand alone applications. www. innovative-dsp.com

CIRCLE 275

INNOVATIVE INTEGRATION

VLSI INTERCONNECTION SPECIALISTS

Ironwood Electronics' produces a complete range of Interconnect Solutions including hundreds of adaptors: prototyping, test probe, programming, and other interconnect devices. For fully compliant surface mount interconnect test adaptors, we offer a wide selection of high quality solutions. We also have custom design services for unique solutions in packaging. 612-452-8100 Fax 612-452-8400 www.ironwoodelectronics.com

CIRCLE 276

IRONWOOD ELECTRONICS

"No-Power" Cholesteric Crystal Displays

Kent Displays' brochure details the benefits of No-Power™ Reflective Cholesteric Liquid Crystal Displays. This technology requires no energy to maintain an image. Displays have wide viewing angles and are flicker free. Call (330) 673-8784.

CIRCLE 277

KENT DISPLAYS

ELECTRONIC DESIGN CATALOG/LITERATURE REVIEW

MICROPAK® INSTRUMENT ENCLOSURES

Lansing Instrument Corp. offers enclosures for smaller, free standing electronic instruments used in hand-held or desktop applications. Three body stylesand a choice of end cap configurations are available, along with several finishes and colors. Literature includes information for stock and custom choices, and a no-risk offer at a special price. Contact Rich Kippola at Lansing Instrument Corp., (800) 847-3535.

CIRCLE 278

LANSING INSTRUMENT CORP.

THE LECROY 1998/99 CATALOG

288 page color and black-and-white pages packed with information on oscilloscopes, disk drive analyzers, power measurement tools, jitter tracking applications, and loads of technical application notes. It's also available on CD with a virtual encyclopedia of facts on signal measurements, including videos!

CIRCLE 279

LECROY CORP.

ADHESIVES AND SEALANTS

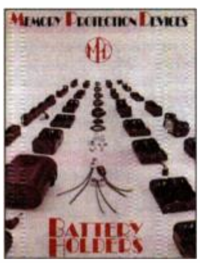
Master Bond Inc., Hackensack, NJ manufactures over 3000 grades of adhesives, sealants and coatings. Line cosists of epoxies, anaecobics, cyanoacrylates, silicones and acrylics. One and two part systems are available. Tel 201-343-8983.

CIRCLE 280

MASTER BOND INC.

BATTERY HOLDERS

Featured products: SMT button cell holders, battery snaps, case hardware, computer clock back-up holders, multi-cell holders with covers, auto cigarette lighter plugs. For computers, alarms, controls, instruments, toys, appliances, etc.



CIRCLE 281

MEMORY PROTECTION

1998 SRAM DATA BOOK

NEW! Includes detailed product data sheets on 1Mb, 2Mb, and 4Mb SyncBurst SRAM; 2 Mb and 4Mb ZBT® SRAM; and 4Mb Late Write and Claymore SRAM. You'll find technical notes, package drawings and sales and service info. Be sure to visit our web site: www.micron.com/mti.

CIRCLE 282

MICRON SEMICONDUCTOR

GIANT NEW SWITCH CATALOG

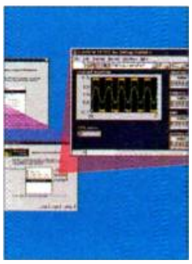
APEM's new 420 page full-line catalog is packed with their switch offerings. New products added: toggles, rockers, pushbuttons, tacts, keys, industrial controls, DIPs, rotary DIPs, micro-limits, pushwheels, slides, keyboards, sealing boots. Many state-of-the-art switch models featuring process compatibility, surface mounting technology & electrostatic discharge withstanding. APEM Tel: 781-246-1007, Fax: 781-245-4531, URL: http://www.APEM.com E-Mail: info@APEM.com

CIRCLE 283

APEM

Power to Make it Simple With LabVIEW!

With LabVIEW, you can build the solutions you need quickly and easily. LabVIEW features the simplicity of a graphical development environment AND the power of a complete programming language. With LabVIEW 5.0, you can get up and running immediately with complete solutions using wizard technology. Phone: (800) 433-3488 (U.S. and Canada) Fax: (512) 794-8411; info@natinst.com; www.natinst.com



CIRCLE 284

NATIONAL INSTRUMENTS

6050 I/O With I/Q

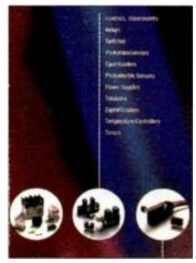
Octagon Systems has introduced a new family of single card industrial computers called the PC Microcontroller Series. The card family combines the industry standard PC architecture with industrial-class I/O and an extensive suite of embedded software in a small 4.5 X 4.9 package rated from - 40° to 85° C.

CIRCLE 285

OCTAGON SYSTEMS

NEW SHORT FORM CATALOG

Omron's Control Components Short Form Catalog contains 200-plus pages of relays, switches, photomicrosensors, card readers, photoelectric sensors, power supplies, totalizers, digital displays, temperature controllers and timers. Call 1-800-55-OMRON. E-mail: SFC2_EDLit@omron.com

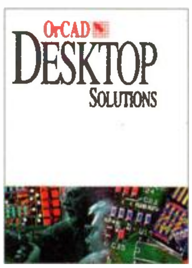


CIRCLE 286

OMRON ELECTRONICS, INC.

FREE EDA CD-ROM

OrCAD's new Desktop Solutions CD includes product overview, detailed data sheets and working demo versions of OrCAD's 32-bit Windows software- including new OrCAD Express and Capture CIS. Order today by calling 1-800-671-9505 or visit our website at www.orcad.com

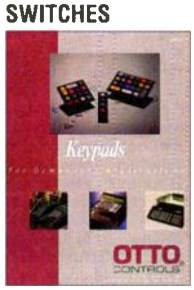


CIRCLE 287

ORCAD

RUGGEDIZED KEYPAD SWITCHES

for Demanding Applications. Z Series ruggedized sealed Keypad Switches are designed to withstand extreme environmental conditions. Custom appearance through keycap options, front panel sealing that will withstand direct water spray per IP67, protection to vandal-proof levels, and resistance to extreme shock and vibration. Call: 847-428-7171; Fax: 847-428-1956; www.ottoeng.com; info@ottoeng.com

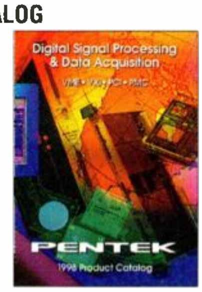


CIRCLE 288

OTTO CONTROLS

1998 PRODUCT CATALOG

Catalog provides full specifications on our VME, PCI, PMC and VXI product lines. You'll also find helpful tutorials, case studies and real-life applications stories. Get the latest information on the broadest line of DSP processors, including our new C6x, C80 and SHARC boards, advanced I/O peripherals and world-class software tools. (201) 818-5900, ext. 855, http://www.pentek.com, e-mail: info@pentek.com

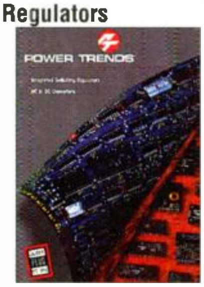


CIRCLE 289

PENTEK, INC.

Integrated Switching Regulators

Power Trends' new 120 page full-line catalog details their complete line of Integrated Switching Regulators (ISR)s and DC to DC Converters. The catalog introducts significant new 5V, 12V, and 24V bus products along with extensions to existing product lines. Photos and standard applications are provided for each product. (800) 531-5782, Fax: (630) 393-6902; E-mail: sales@powertrends.com www: http://www.powertrends.com

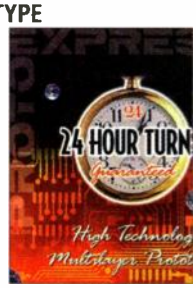


CIRCLE 290

POWER TRENDS, INC.

MULTILAYER PROTOTYPE

Award winning quick turn multilayer prototype manufacture specializing in 24 hour to 5 day turns, for commercial and milspec boards (Milp-55110E) on FR4 and polyimide materials. Our capabilities also include "blind and buried" vias, full body gold, carbon baste, metal core boards, small hole drilling, and net list testing.



CIRCLE 291

PROTO EXPRESS

Challenging Cable Assembly Specialists

Precision Interconnect, a division of AMP Inc. has released a new brochure explaining their design and manufacturing approach for cable assemblies needing to perform in challenging electrical, mechanical or environmental applications. Solutions include miniaturization, dense packaging, precise electricals, sealed systems, etc. Phone (503) 620-9400: Fax (503) 620-7131.

CIRCLE 292

PRECISION INTERCONNECT

ELECTRONIC DESIGN CATALOG/LITERATURE REVIEW

LIQUID CRYSTAL DISPLAYS

A division of Purdy Electronics has released its 1998 LCD short form catalog. The catalog features a full line of TFT and STN color panels and monitors plus intelligent graphic and character monochrome displays.

CIRCLE 293

PURDY ELECTRONICS CORP.

LITERATURE REVIEW

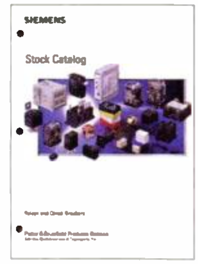
Complete selection of embedded single board computers featuring Intel's 386EX and 80188EB embedded microprocessors and I/O modules. All products fully software supported by C/C++ demo and drivers. Call 1-888-RLC-TECH, FAX (805) 466-9736 or visit our website at http://www.RLC.com

CIRCLE 294

RLC ENTERPRISES INC.

RELAYS & CIRCUIT BREAKERS

Stock catalog lists Potter & Brumfield and Siemens relays and circuit breakers. Electromechanical, solid state and time delay relays are detailed, as well as magnetic and thermal breakers. Many ratings and various coil, package and terminal options are offered.



CIRCLE 295

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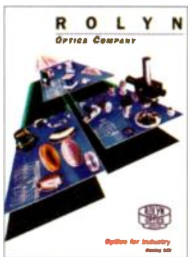

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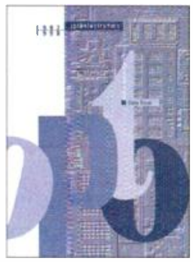

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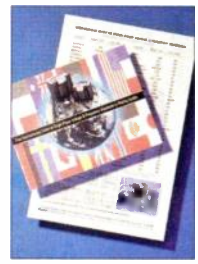

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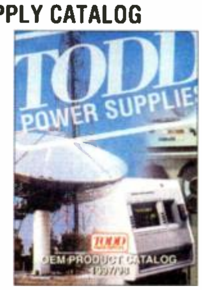

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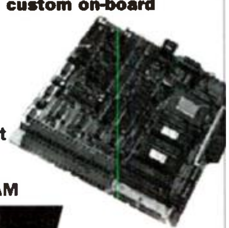

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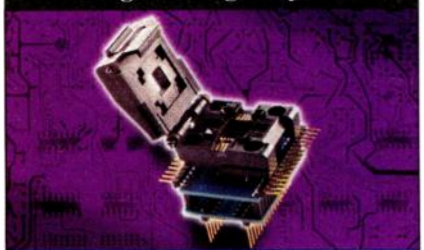

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