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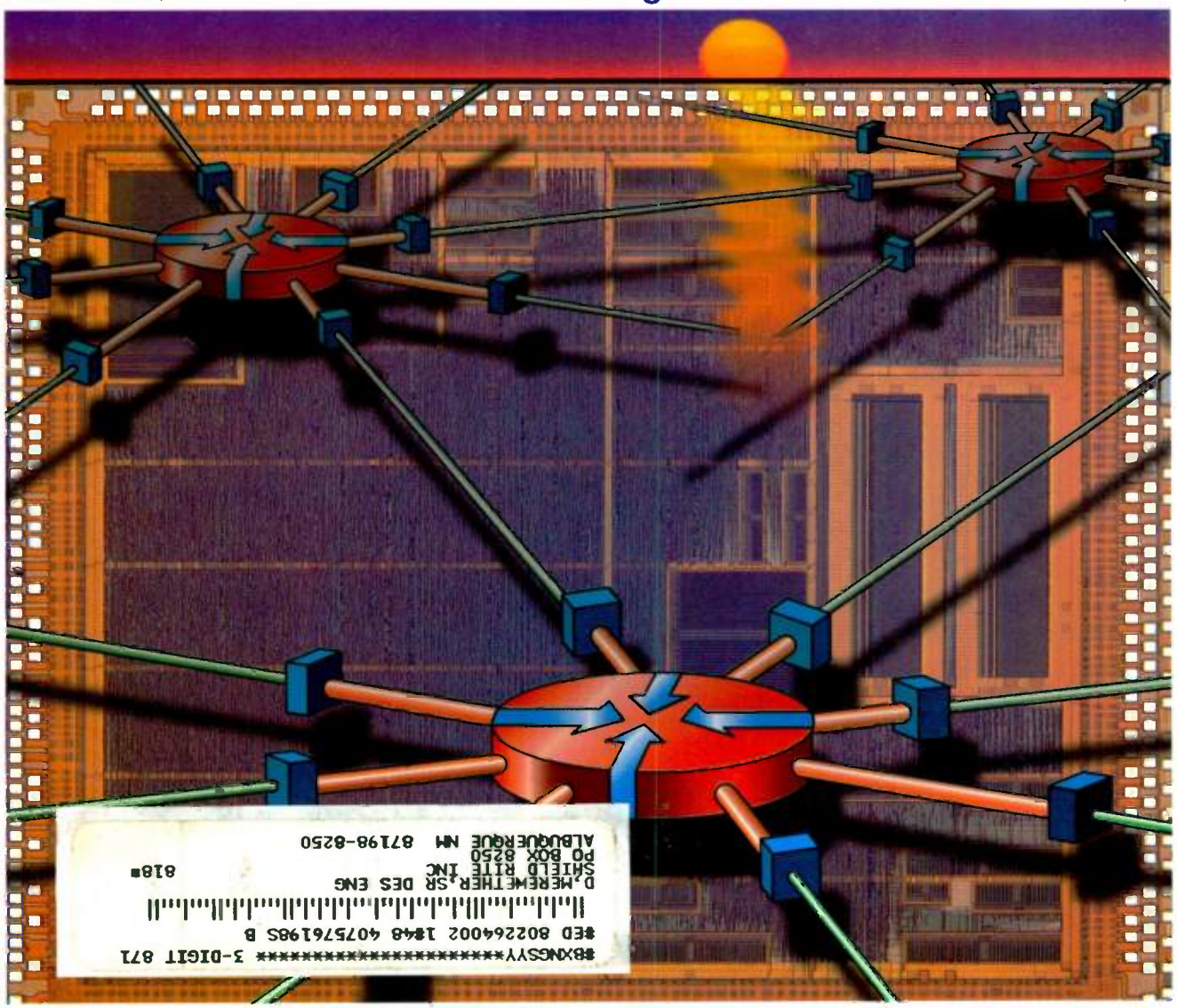

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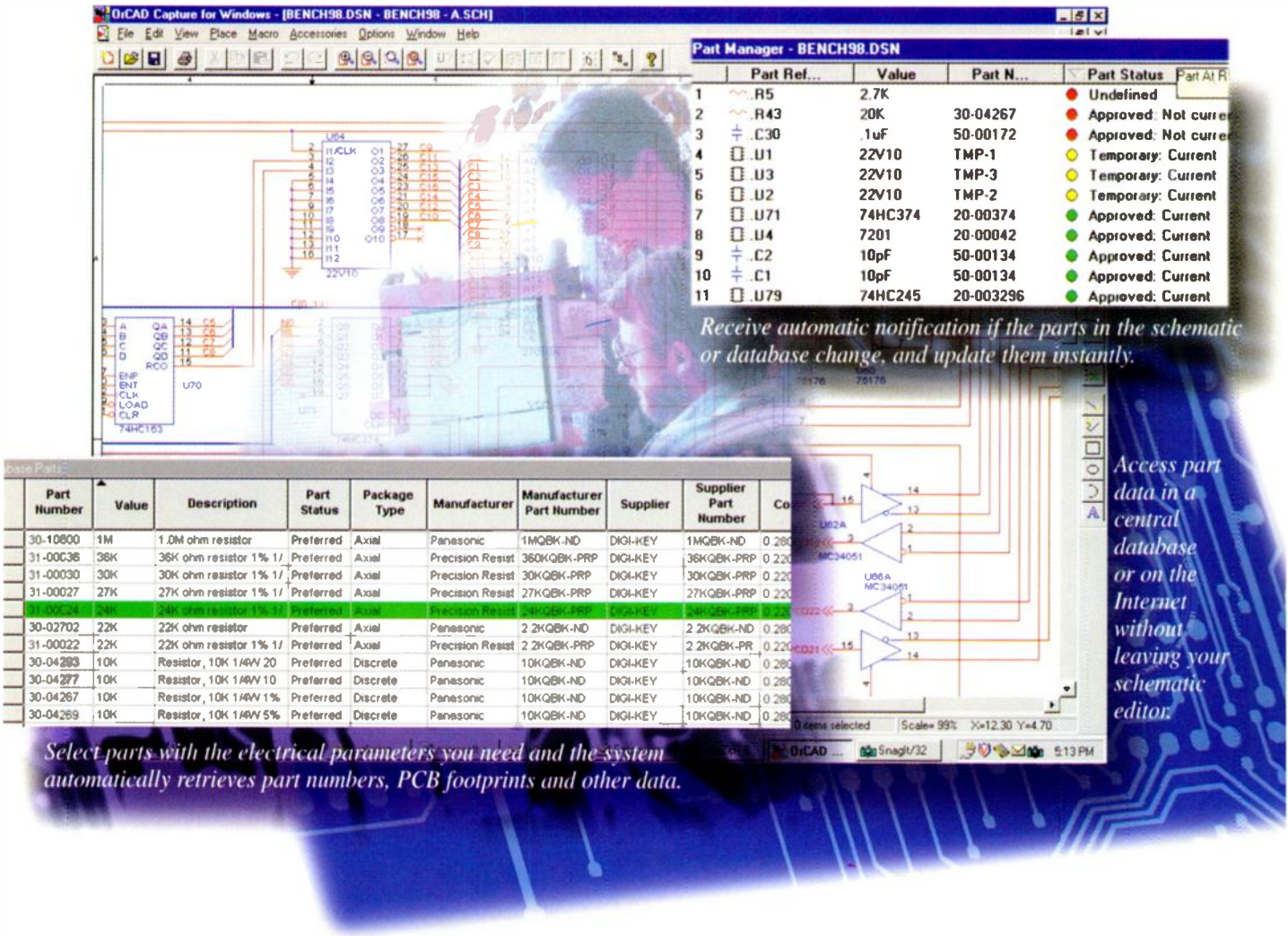
Engineers Spend 30% Of Their Time Researching And Entering Part Data.



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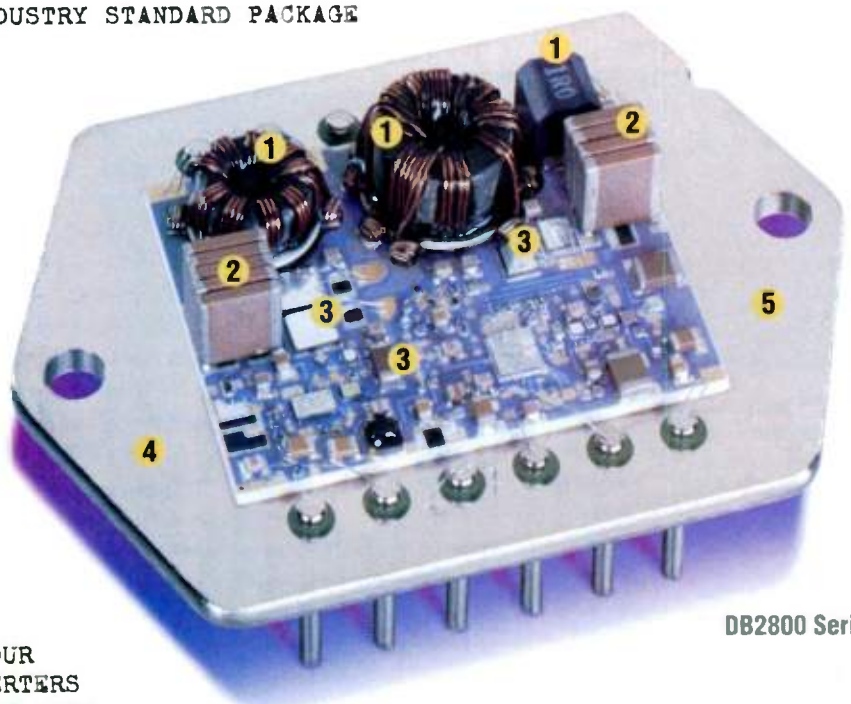

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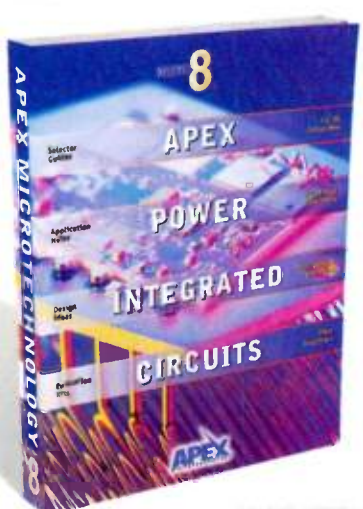

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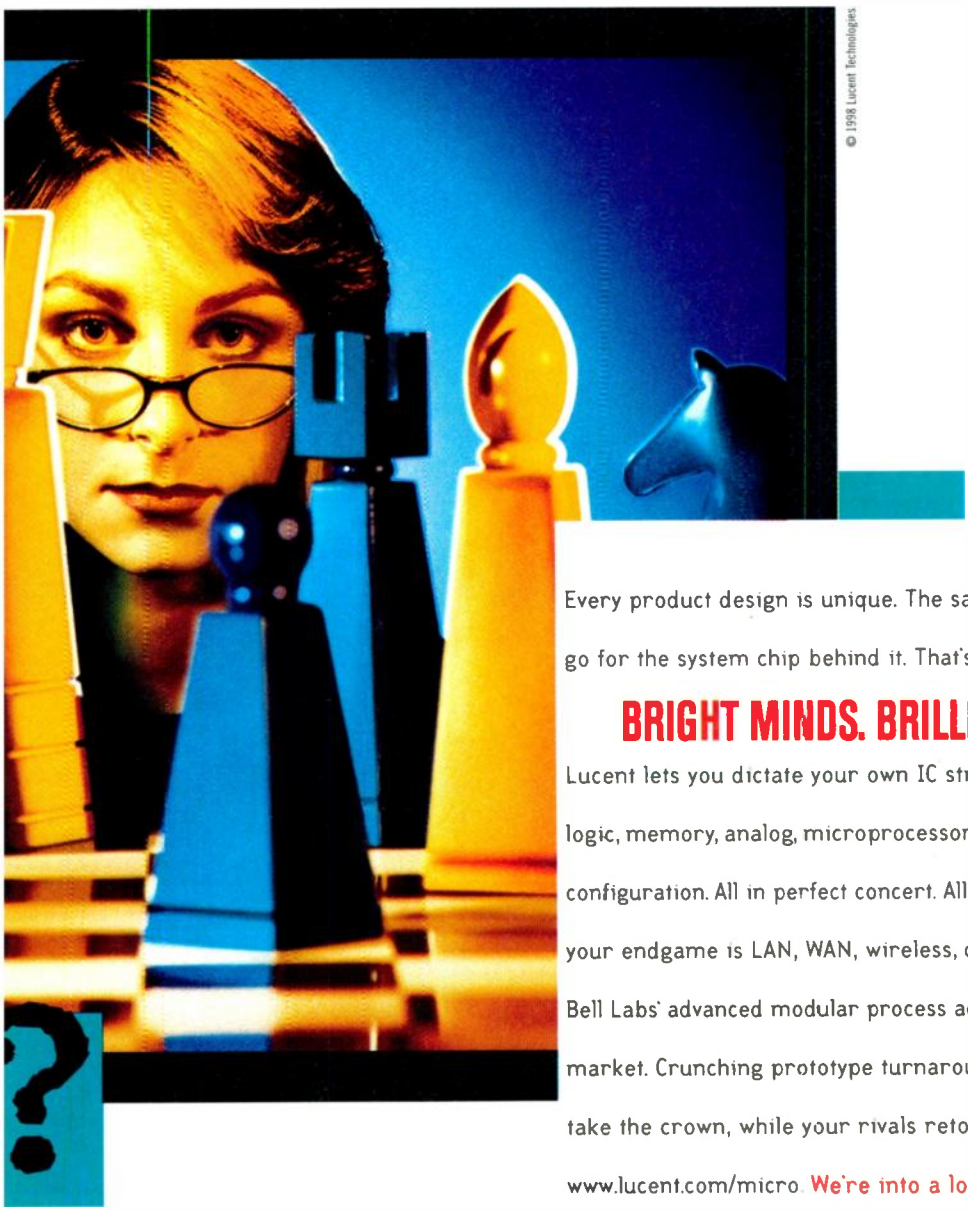

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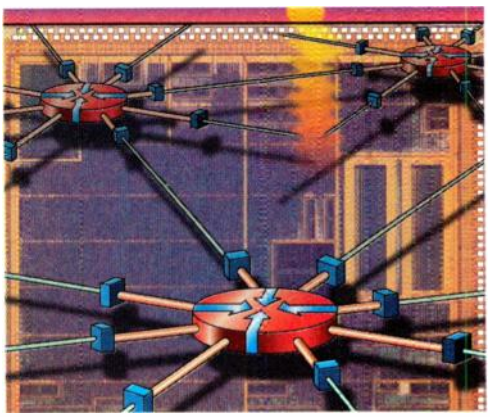

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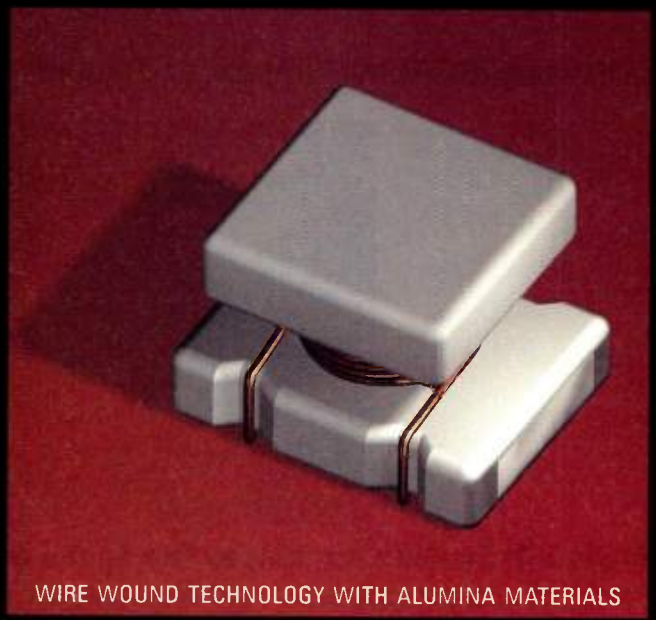

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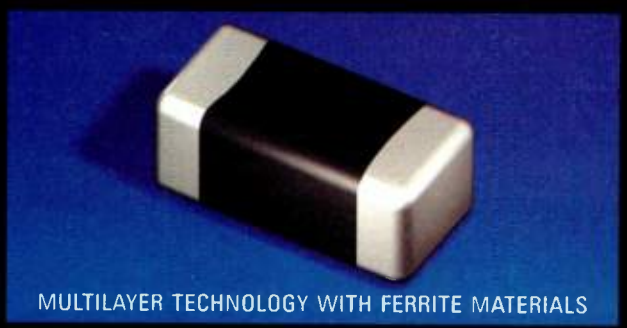

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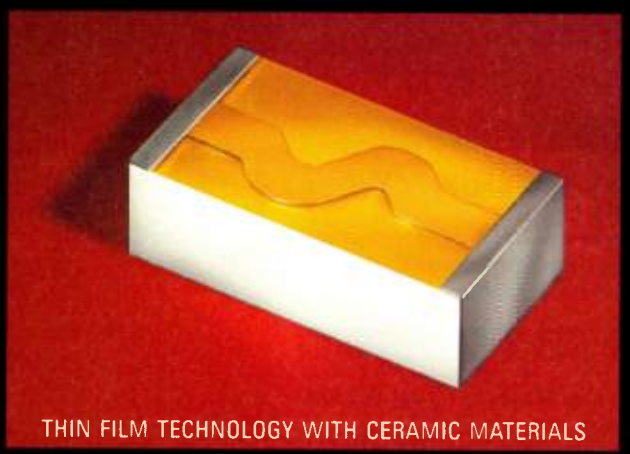

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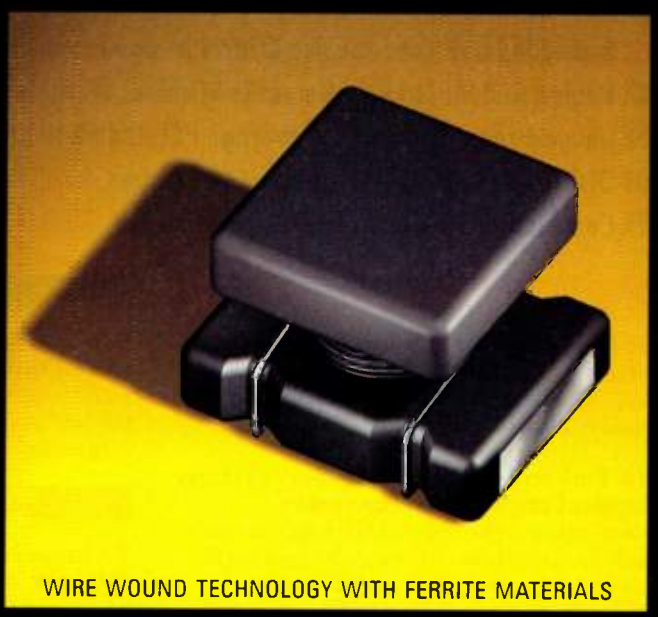

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●Analog Design:..... Check out the latest power technology in our two previews. First there's the International Symposium on Low-Power Electronics and Design (ISLPED'98), then the International Conference on Microelectronics and Packaging (ICMP'98).

●Test & Measurement:..... What challenges are posed by system-on-a-chip and deep-submicron geometries as applied to design for test? Read the Special Report by Test and Measurement Editor Joe Desposito.

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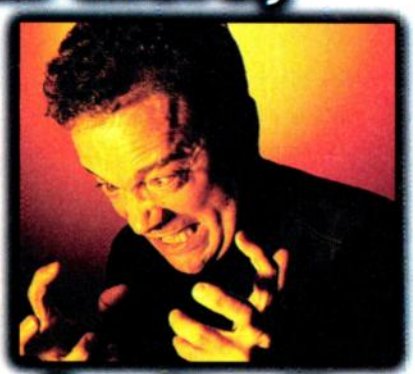

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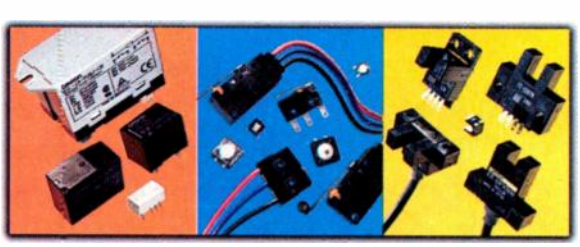

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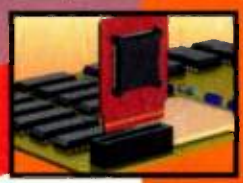
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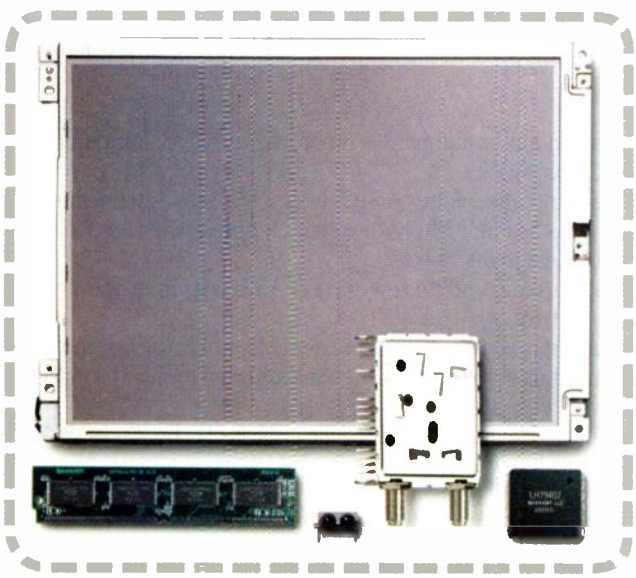

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Even now, designers are aiming to develop kitchens that integrate appliances and automate everything from stocking up to washing down. That parallels Sharp's goal of giving you easy access to a huge range of mouth-watering components . . . and to doing more at our end to mix, blend and adjust them into custom integrated subsystems. For appetizers, consider these recent innovations:

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LH79402 ARM-based 32-bit Universal Microcontroller. *This system-on-chip includes on-chip memory, a no-glue memory interface, serial and parallel comm ports and a host of other peripherals, making it ideal for high-performance, compact, low-power-consumption designs.*

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BSFZ Series satellite tuners *for reception of digital and video streams.*

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EDITORIAL

El Niño Blows Through DAC

Stormy, El Niño-related weather created chaos in Northern California all year. It finally broke just a few days before the opening of the Design Automation Conference (DAC), held last month in San Francisco. Those attending, however, may have thought El Niño settled inside the Moscone Convention Center.

Let's take a look at the current EDA radar map and spot the disturbances. There were some 18 acquisitions last year, 44 new start-ups, three closed shops, and enough hot air from some vendors about IP and system-on-a-chip (SOC) solutions to launch a weather balloon. But hey, this is the EDA industry. As one Dataquest analyst remarked, "Overall, EDA in 1997 was turmoil as usual."

With plenty of ideas, talent, and venture bucks around, there were some 20 new players on the show floor this year. They were launching (or talking about) technologies that may provide the key tools everyone is hoping for. (Keep an eye on EDA Editor Cheryl Ajluni's upcoming articles on emerging technologies.)

At *Electronic Design's* annual state of the EDA market briefing, Ron Collett, Collett International, said a number of "power forces" will reshape the electronics industry and, specifically, the EDA market. Some forces motivating semiconductor companies to choose an SOC design: the rising costs of fab plants, soaring IC design complexity, time-to-market pressures, and the shift to consumer products. Here are some conclusions:

- In order to survive, semiconductor companies must become SOC companies, with strong ASSP and ASIC businesses.
- The number of systems companies doing ASIC design has steadily declined over the last several years. This trend is likely to continue unless the cost, complexity, and difficulty of ASIC design decreases.
- Moreover, system-design teams will do fewer new ASIC designs and rely more on reused ASICs in the future.
- The semiconductor industry will adopt advanced IC technology more rapidly—i.e., adopting leading-edge process geometries and designing ICs with much higher gate counts.
- The semiconductor industry is embracing SOC aggressively; however, it is also in desperate need of system knowledge.

We'll keep you posted with adequate warnings on the fast-moving EDA front.

Tom Halligan
Editor-in-Chief
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Advanced 6U VME SBCs from PEP...

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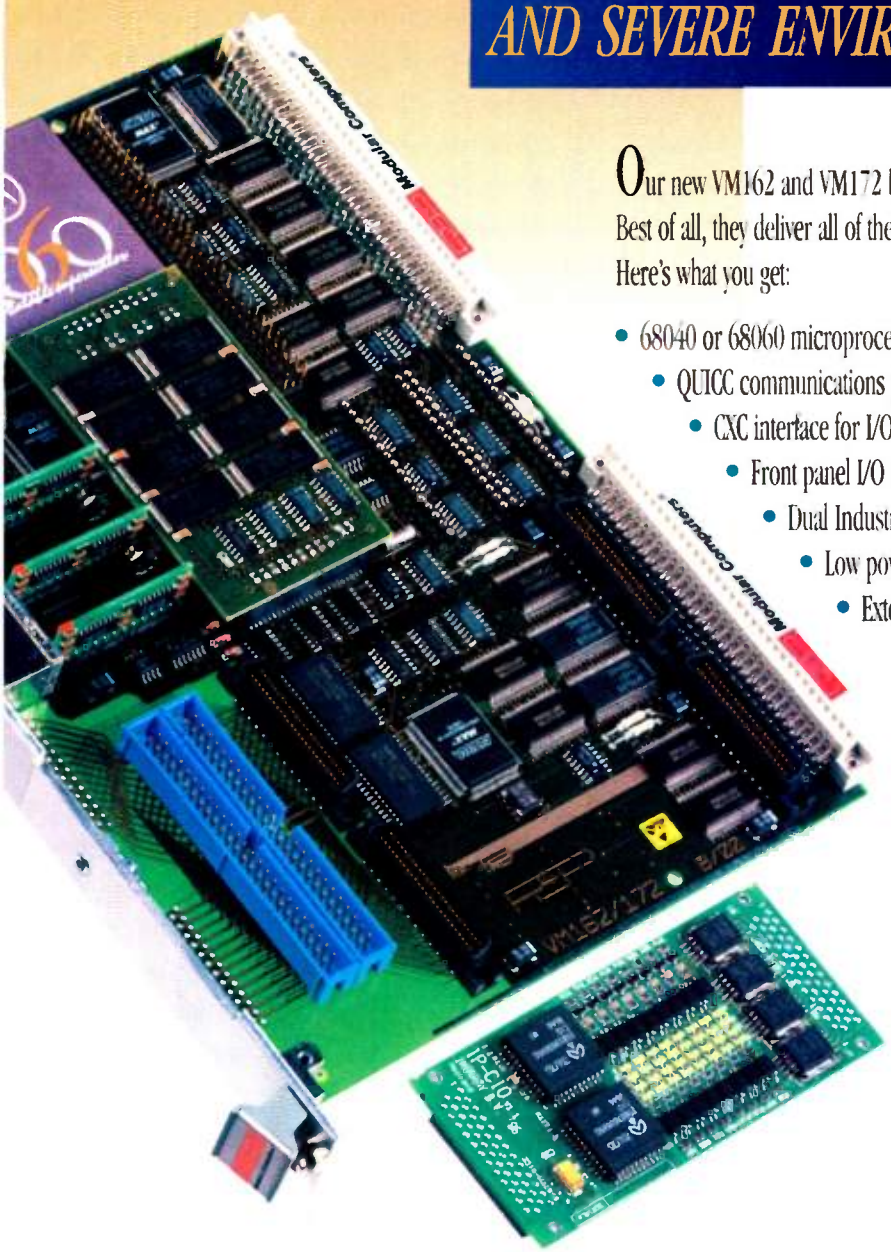

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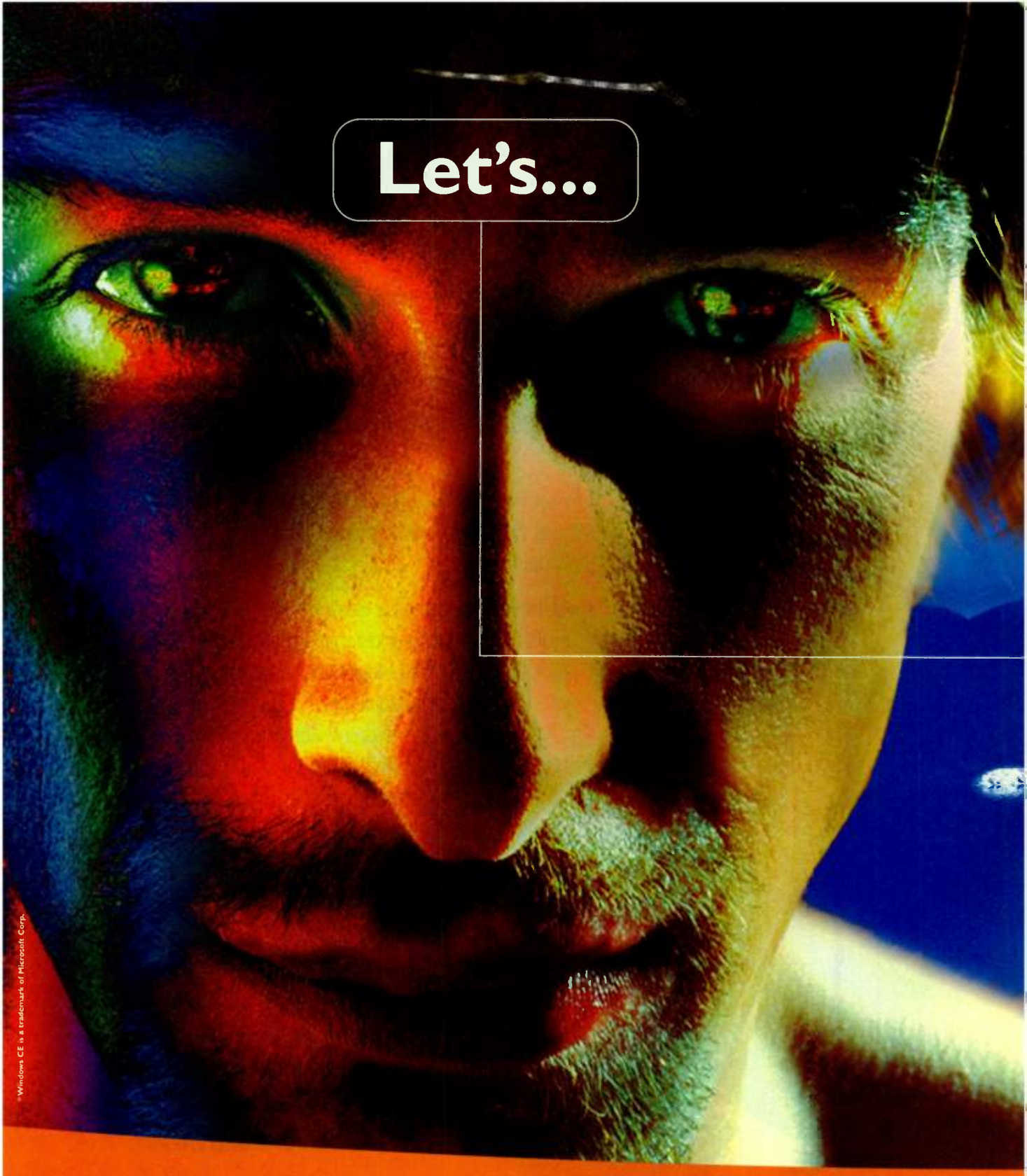

*Windows CE is a trademark of Microsoft Corp.

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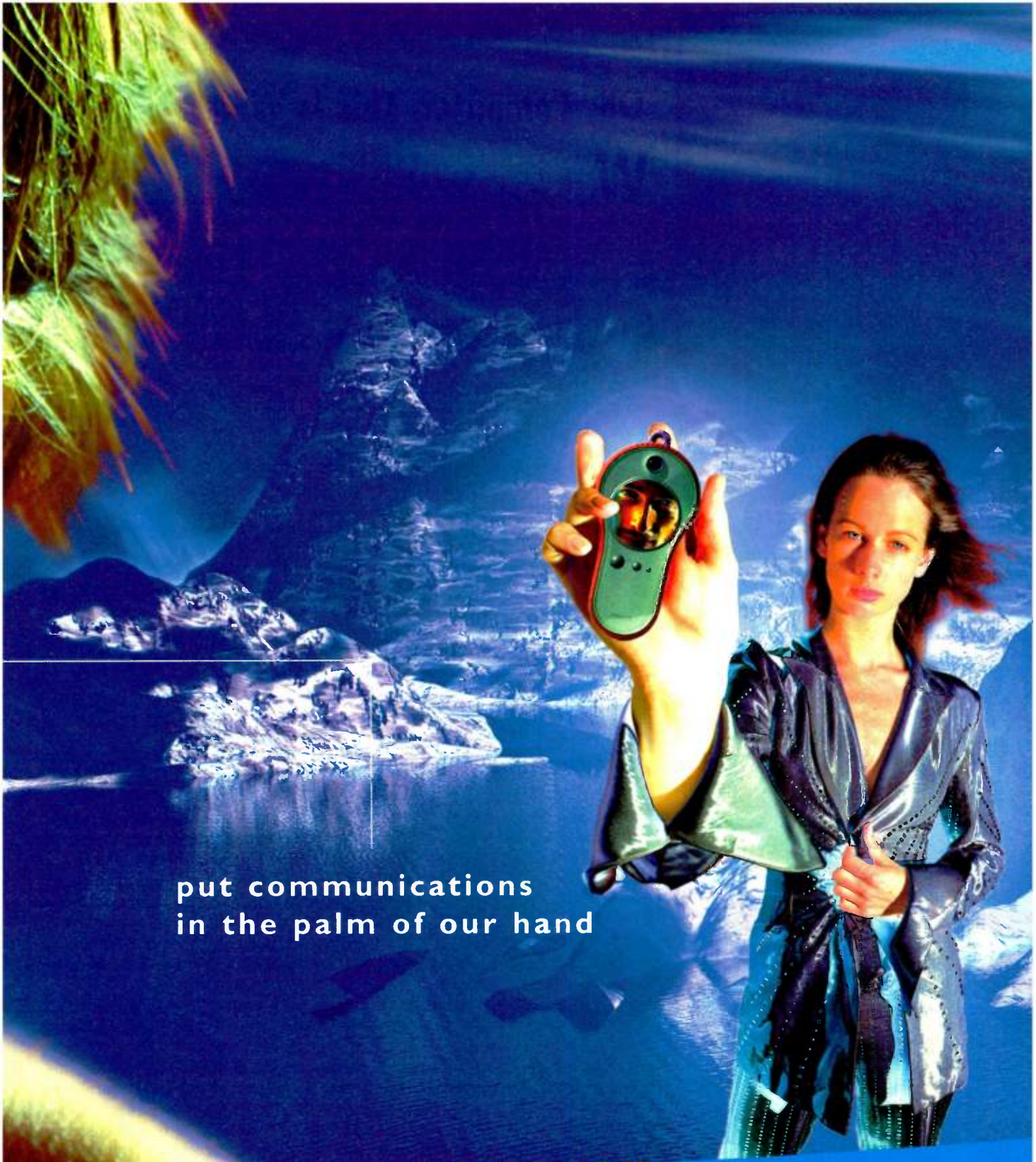

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PHILIPS

Let's make things better.

Patented Chuck Enables Low-Cost Wafer Cooling

Researchers from Sandia National Laboratory, Albuquerque, N.M., have developed a patented prototype device that offers a new method for cooling silicon wafers during the chip manufacturing process. The device, known as an electrostatic chuck, electrostatically clamps onto a silicon wafer and regulates its temperature with confined helium gas. The chuck's face is made of a combination of materials that include silicon, silicon dioxide, and silicon nitride, and is fabricated using conventional silicon chip technology.

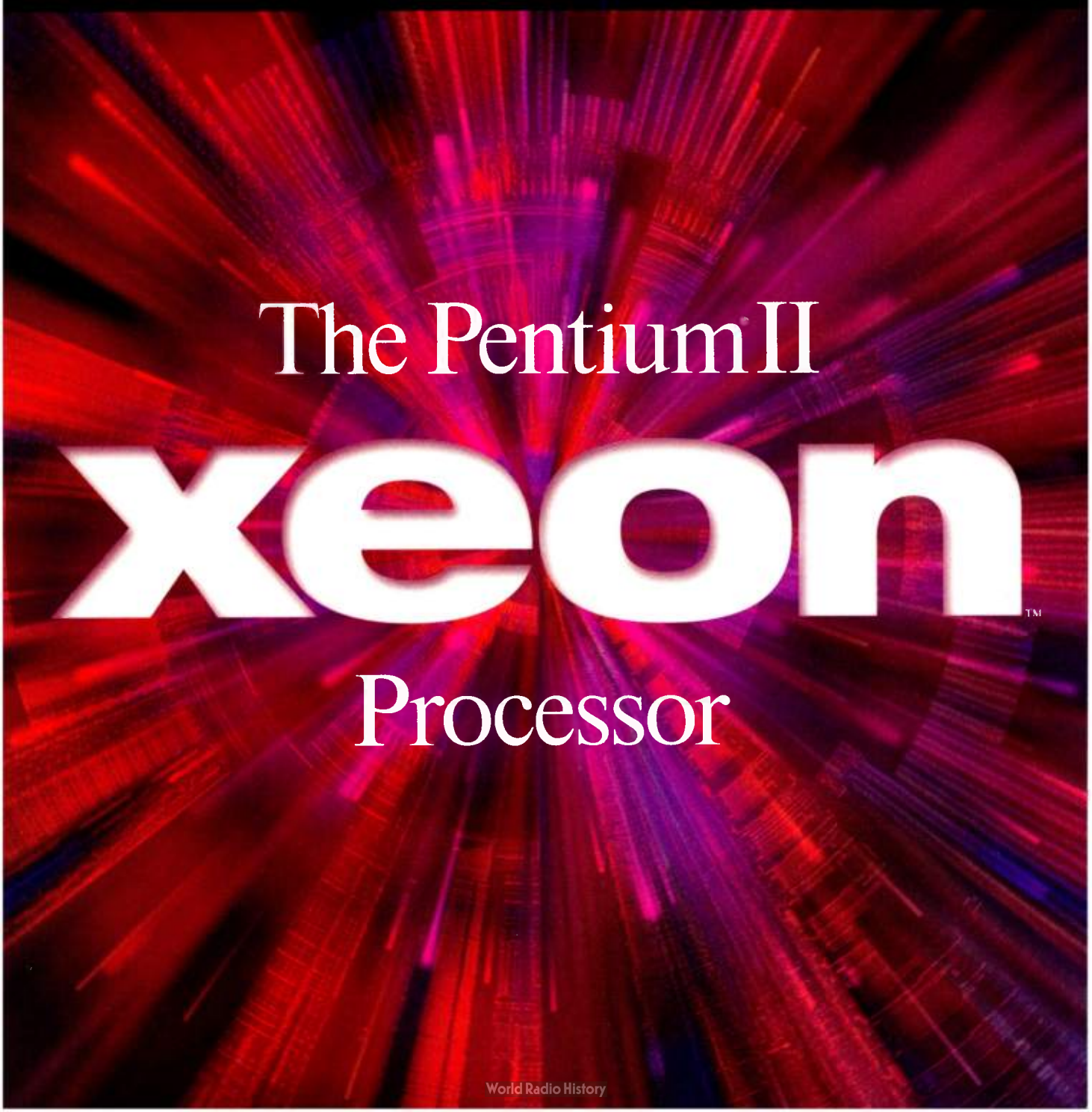
Its unusual construction allows it to operate at higher temperatures that are more suited to modern wafer processing. In fact, researchers believe that it may even be possible to develop a chuck that will operate at up to 600°C. And, because it clamps and releases wafers more quickly than other methods, overall processing time is decreased. Researchers believe this device will provide a more effective, and less expensive microchip production process

One of the advantages of this approach is its innovative chuck face design, which is made up of an easily produced, patterned silicon wafer. The wafer consists of tiny, non-conductive silicon-dioxide islands rising above the surface of the rest of the wafer. These islands physically support the wafer being etched. Because they provide insulation, a strong electric field can be applied between the chuck face and the clamped wafer without excessive currents being developed. This field can be turned on or off very quickly, allowing the chuck to grab or release just as rapidly.

The prototype chuck comes from a project funded by the Department of Energy and SEMATECH. Contact Sandia at (505) 844-8066, or check out its web site at *http://www.sandia.com.* CA

Edited By Roger Engelke

A new word for workstations.



Work [wond

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The Pentium® II Xeon™ Processor.

The new Intel® Pentium® II Xeon™ processor delivers the power for amazing workstation performance. It's hard-core processing. So it's no wonder demanding applications like Pro/ENGINEER and SOFTIMAGE|3D are designed for Intel®-based workstations, and new titles like CATIA, Maya and Design Compiler are being introduced for them.

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Thick-Film Gold Conductors Replace Thin-Film In High-Performance Applications

With sub-nanosecond signal rise times and operating frequencies extending to the higher-gigahertz region, the materials used to design high-speed circuits have become extremely critical. At these operating frequencies and rise times, a poor choice can cause noise, crosstalk, reflections, impedance mismatches, propagation delays, and signal-attenuation problems.

To reduce signal loss due to attenuation, the conductor-related conditions must be met. These include high conductivity, high backlit density, and ultra-fine-line resolution circuit lines. In addition, the lines must have constant width and height (cross-section) along the entire length of the critical signal line.

In response to these requirements, DuPont Photopolymer & Electronic Materials, Research Triangle Park, N.C., has introduced a high-density, thick-film, gold conductor composition. This composition provides low losses at frequencies above 20 GHz, and is capable of being etched to resolve features of less than 20 µm.

Designated QG150, the conductor is compatible with a wide range of ceramic substrates and thick-film, multilayer dielectrics. It's offered as a low-cost alternative to thin-film metallizations for both high-density interconnects and RF/microwave applications, such as cellular phones, satellite communications, and local multipoint distribution systems.

The use of gold metallizations in electronics is nothing new. The material is used extensively in high-performance, high-reliability, and high-frequency applications. Thick-film circuits can be used with little concern for migration under standard temperature, bias, and humidity conditions. However, for some high-frequency, microwave, and high-density multichip module (MCM) applications, thin-film deposition technologies are used. While thin-film gold circuits offer high conductivity, high density, and ultra-fine-line resolution capabilities, they can be costly—relative to thick-film techniques.

Technological Advances

To make the performance of the lower-cost, thick-film gold metallization competitive with that of the thin-film, advances were made in three key areas: the metal powder itself (gold, in this case), the inorganic binder, and the organic vehicle. With respect to the metal, high-density gold compositions were used. These comprise a new type of gold powder, which is different in shape, size, composition, and surface morphology. Powder sizes ranging from 0.3 to 4 µm were studied for fine-line printing, packing density, and etching characteristics, with the size finally selected being in the submicron range.

The inorganic binder system was optimized for high-sintering density, wirebond strength, and complete etching and post-etching capabilities. It was designed so that high-density gold thick film can be used as a top layer, as well as for internal metallization using various thick-film dielectric compositions. Finally, the organic vehicle system was optimized for stable viscosity, fine-line-width screen printing, and thin-printing capabilities for etching applications.

Test Results

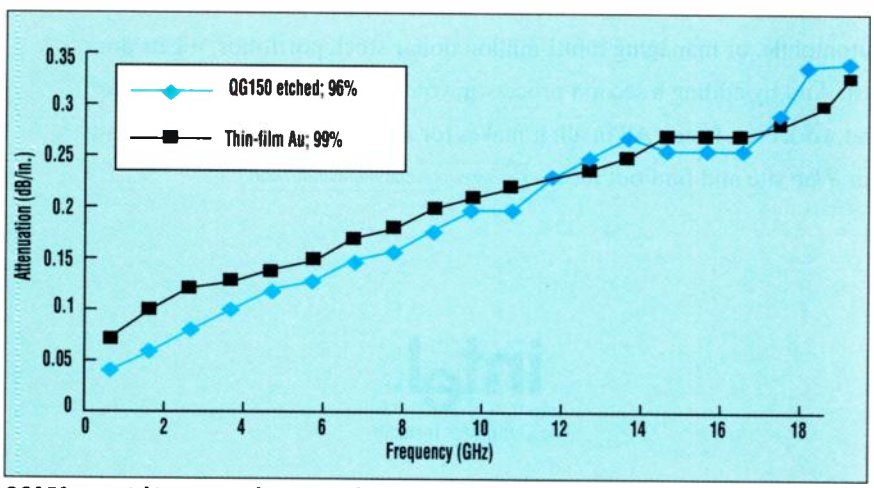
A T-pattern microstrip resonator was used to test the high-frequency performance of the circuit, which was manufactured using these newly optimized components. The test circuit has a nominal characteristic impedance of 50 Ω, and a stub length that results in a primary resonance at about 0.5 GHz. A typical circuit measures 2 by 6 in.

Properties for thick- and thin-film materials were evaluated using conductors patterned on 0.025-in. thick alumina substrates, with the T-pattern on one side and the return path on the other. Alumina substrates were chosen because they are well characterized in the industry. QG150 material, patterned on 96% alumina substrates, has a high-frequency performance equivalent to that of thin-film, which is patterned on more costly 99% alumina substrates *(see the figure)*. Other features of the material include an average peel adhesion strength of 25 to 28 N, which is equivalent to the standard peel strength for traditional gold thick-film compositions. The resistivity of the material was measured at 2.5 mΩ per 2-by-2-in. square. Normalized to 10 µm, it is almost equal to the bulk resistivity of pure gold.

The printed or etched high density gold thick-film compositions are compatible with thick-film resistors, thermistors, and thick-film dielectric compositions for internal or external metallizations, as well as high-density MCM circuits.

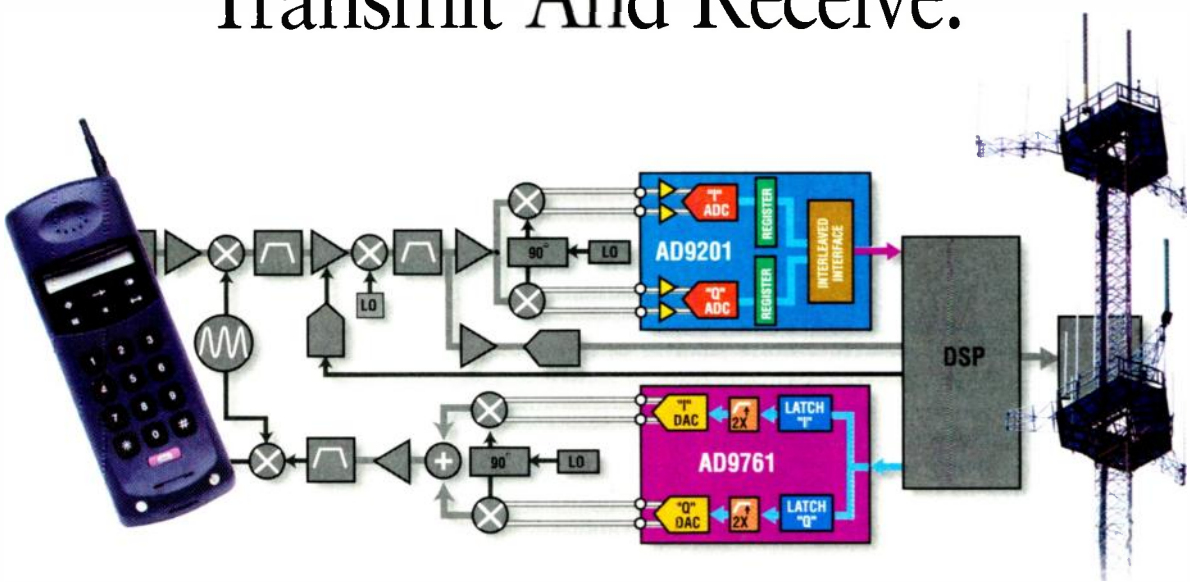
For more information, contact DuPont at (800) 284-3382, or visit www.dupont.com/mcm.

Patrick Mannion



QG150 material is patterned on 96% alumina substrates. Over a test range of 0.5 to 18 GHz, it was shown to have a high-frequency performance equivalent to that of thin-film, which is patterned on more costly 99% alumina substrates.

Convert I&Q Channels In Both Transmit And Receive.



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[1] @ 2 MHz/20 MSPS
[2] USD 10,000s, recommended resale, FOB U.S.A.

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Enhanced Memory Interface Speeds Systems With Foreground And Background Operation

Various suppliers of motherboard chip sets, graphics chips, and DRAM are pitching their support for the Virtual-Channel Memory (VCM) interface. The VCM promises to enhance system performance by providing multiple access channels to memory, without adding complexity to the system. It permits personal computer and workstation designers to reduce access latencies, while allowing multitasking operations to main memory or specific subsystems, like graphics. The scheme requires just a few thousand gates in the system controller, with minimal changes to the memory chips and BIOS.

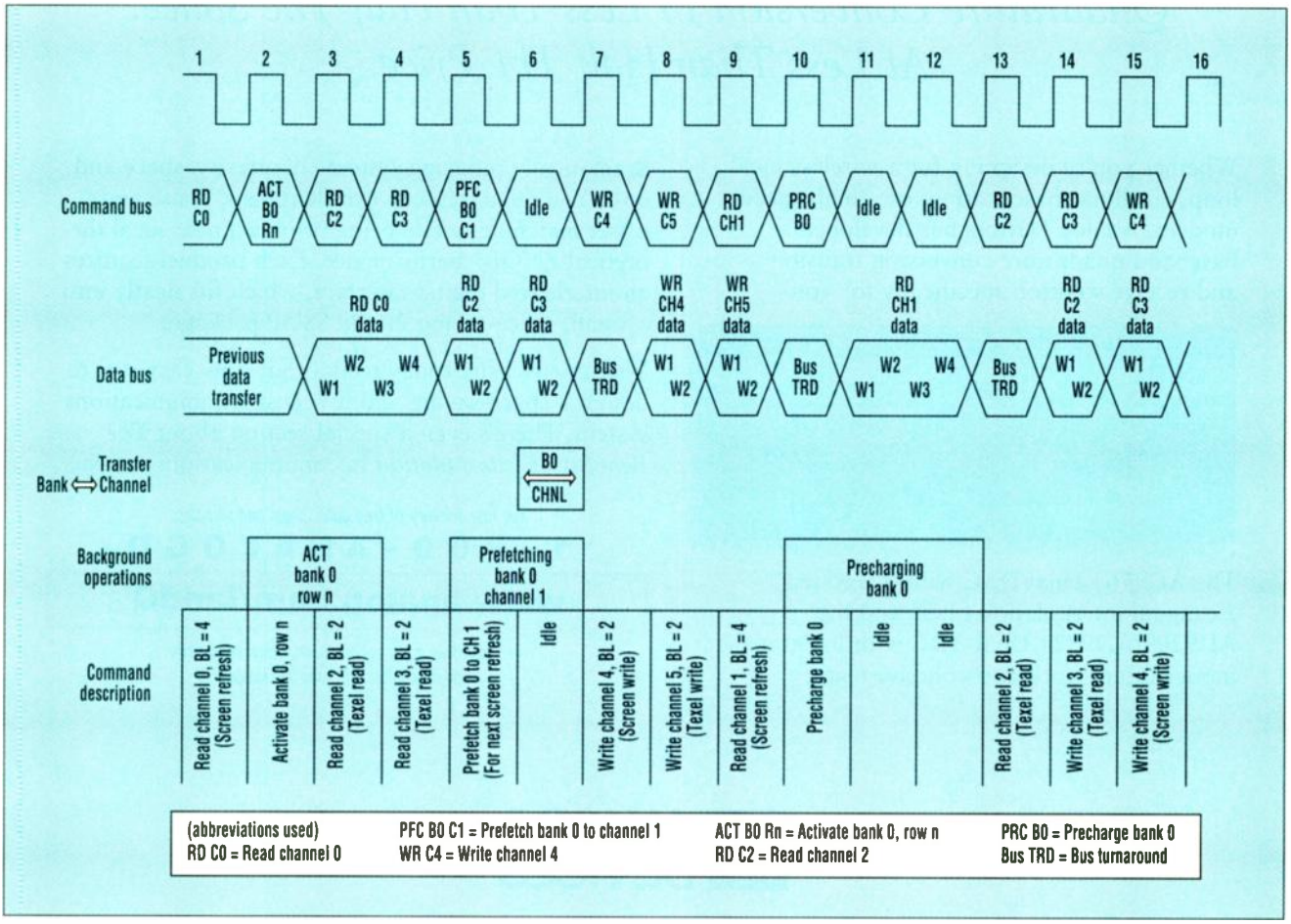
The VCM interface was developed last year by NEC Electronics Inc., Santa Clara, Calif. The company plans to offer VCM as an open standard, and will not charge any licensing fees for use of this technology.

The VCM interface embedded in the memory chips employs a wide internal interface (1024 bits), which is used to implement the multiple virtual channels. Multiple memory masters (the host CPU and various peripherals, such as graphics controllers and data-communications chips) appear to simultaneously access the memory. This results in improved system throughput (concurrent foreground and background operations). The scheme will work with most DRAM interfaces now in use—extended data out (EDO), double data rate (DDR), synchronous graphics (SG), synchronous, and others.

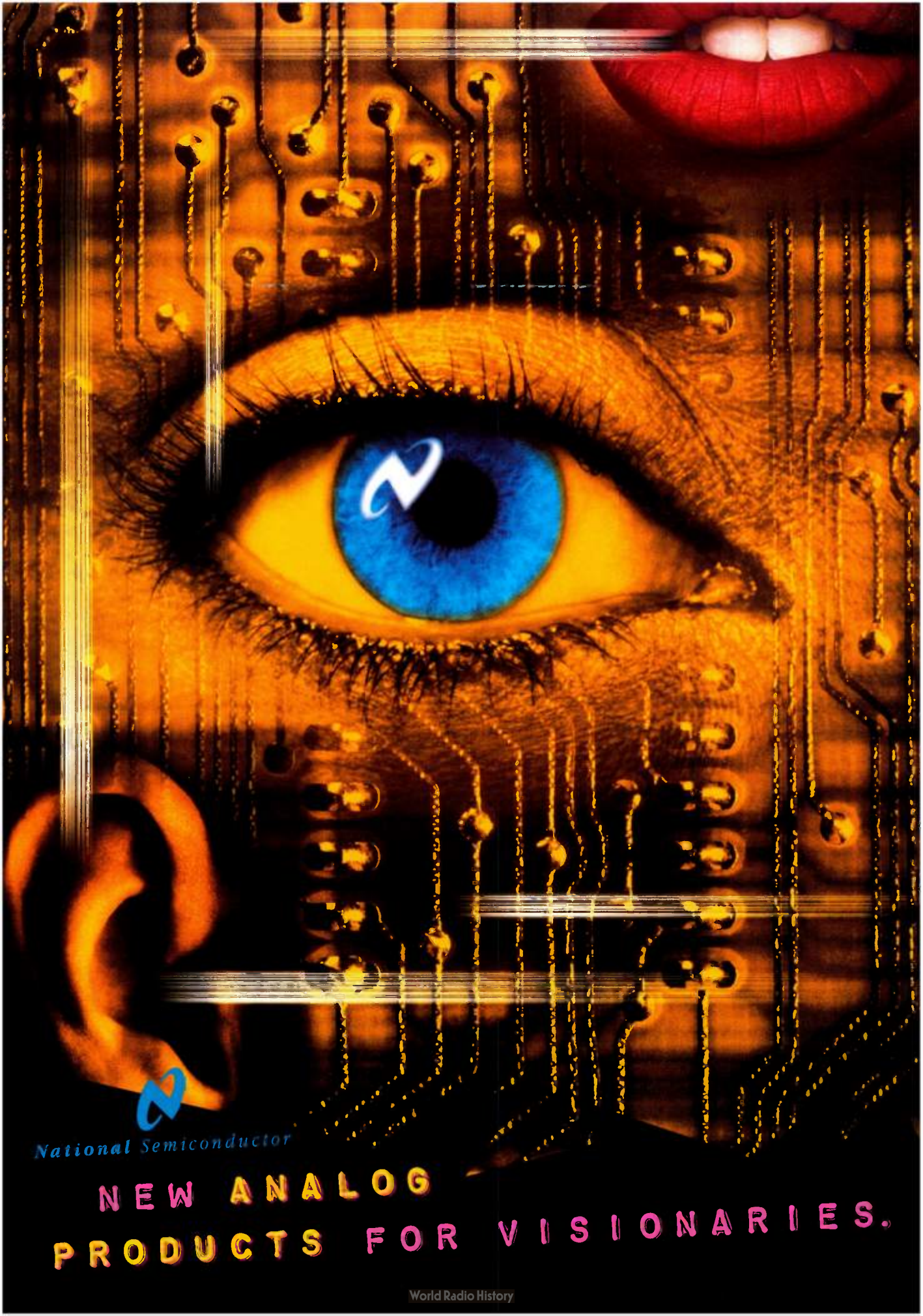
Each virtual channel accesses a region of memory, referred to as a locality. The locality, which is a range of address locations in the memory, can be anywhere in the memory array. The locations are assigned to a channel by the controller set-up software. Each system memory master can control multiple logical channels. Resources, such as row buffers, special operation modes, and burst transfer modes, are dedicated to each channel.

Designed as a core technology, the VCM interface can easily be integrated into existing I/O architectures. It requires minimal circuit modifications and no circuit-board changes. System designers can upgrade the components without needing a new motherboard.

Most of today's memory architecture developments have focused on improving the memory-bus interface. The VCM approach concentrates on changes to the memory core, which remove some of the idiosyncrasies inherent in DRAMs. Fully-associated row buffers give the system the flexibility



The command and timing sequence for a Virtual-Channel Memory interface shows how the different operations are interleaved. This provides improved throughput by using foreground and background operations.



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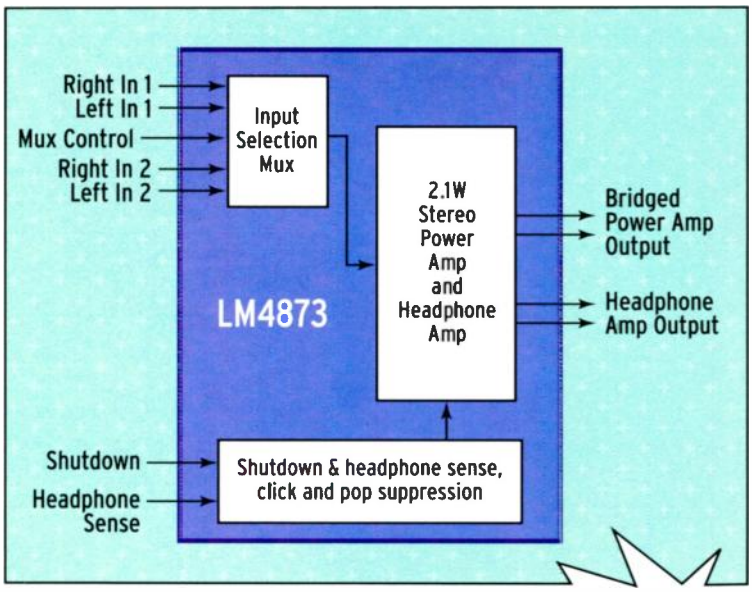
BIG POWER, LITTLE PACKAGE



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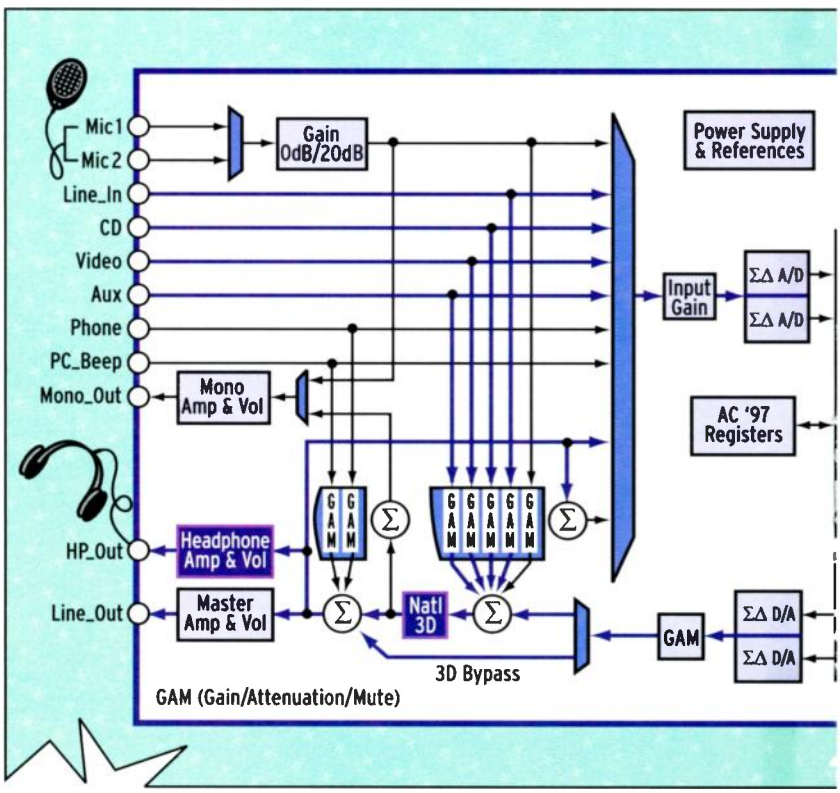

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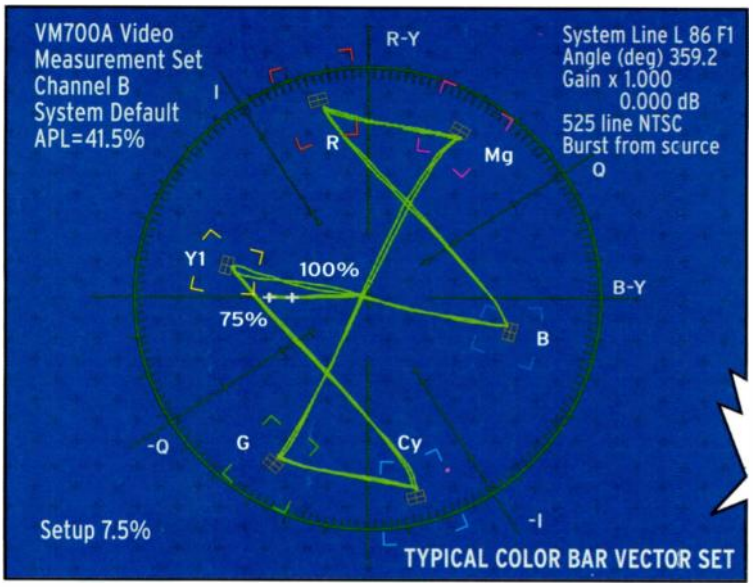
A/D CONVERTERS

3V 8-BIT VIDEO/IMAGING A/D CONVERTER



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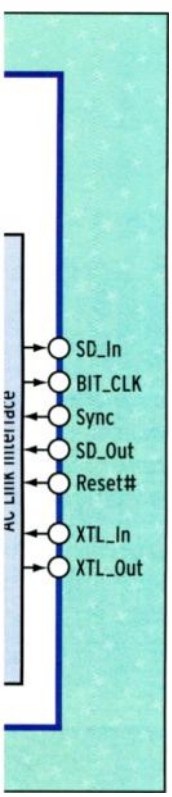

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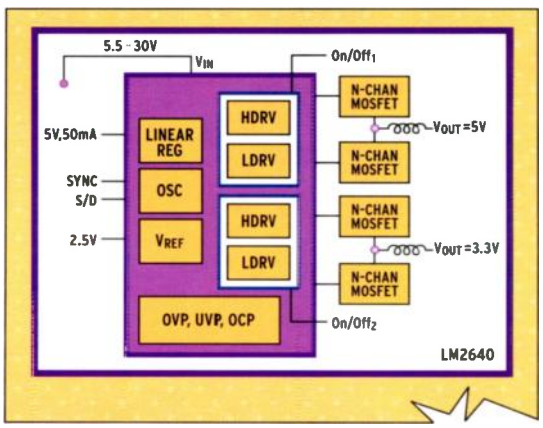
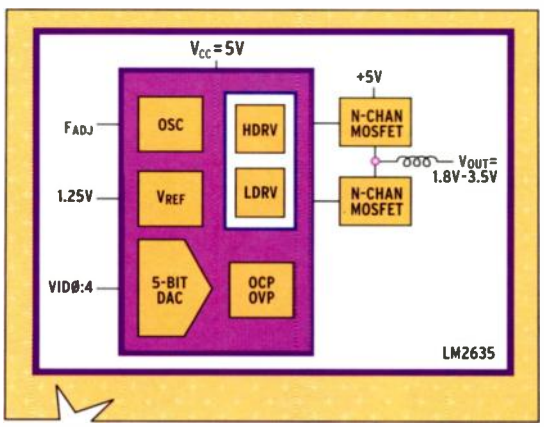
- 2% output accuracy over line, load, and temperature variations
- Built-in dual fast-action comparators for fast response to large load transients
- Dynamic output voltage positioning
- Current limit without external sense resistor
- Powergood flag and output enable; over-voltage protection
- Precision 1.25V reference output

DUAL STEP-DOWN SYNCHRONOUS CONTROLLER FOR PORTABLES



STEP-DOWN SYNCHRONOUS CONTROLLER FOR DESKTOPS



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- Numerous fault-detection flags for safe and reliable cell charges
- Five charge modes for 100% charge under all conditions
- LED drivers for visual indication of charge status

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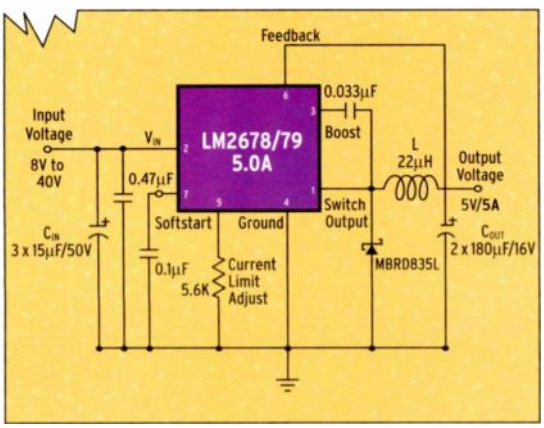
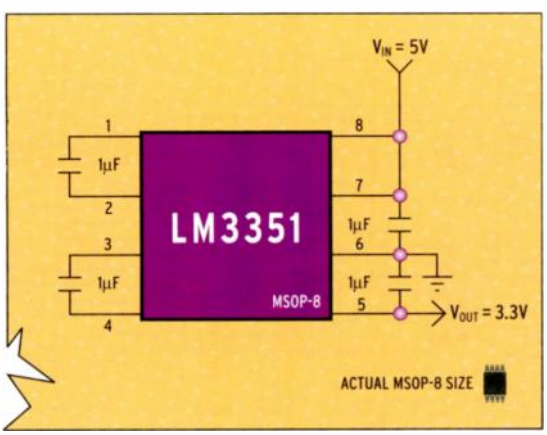
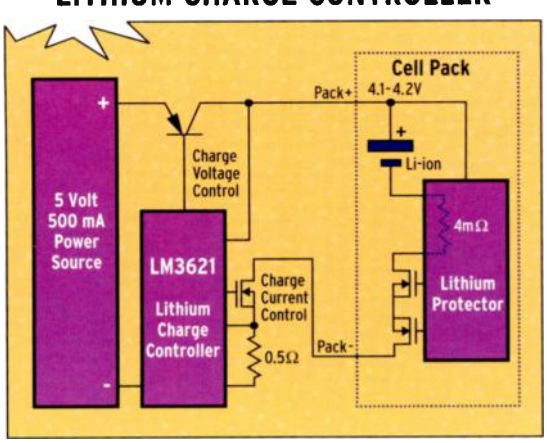
5.0A SIMPLE SWITCHER CONVERTERS



STEP-DOWN CONVERTER MSOP-8 PACKAGE



LITHIUM CHARGE CONTROLLER



5A SIMPLE SWITCHER Converter LM2678/79

These 5.0A versions of our SIMPLE SWITCHER step-down power converters feature efficiency ratings greater than 90%, making them ideal for high current applications.

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With highly efficient conversion (95%) at 200kHz, low quiescent current and a space-saving solution size, the LM3351 is a very cost-effective option – perfect for battery-operated applications.

- Efficient conversion of 3.3V to 5V or 5V to 3.3V
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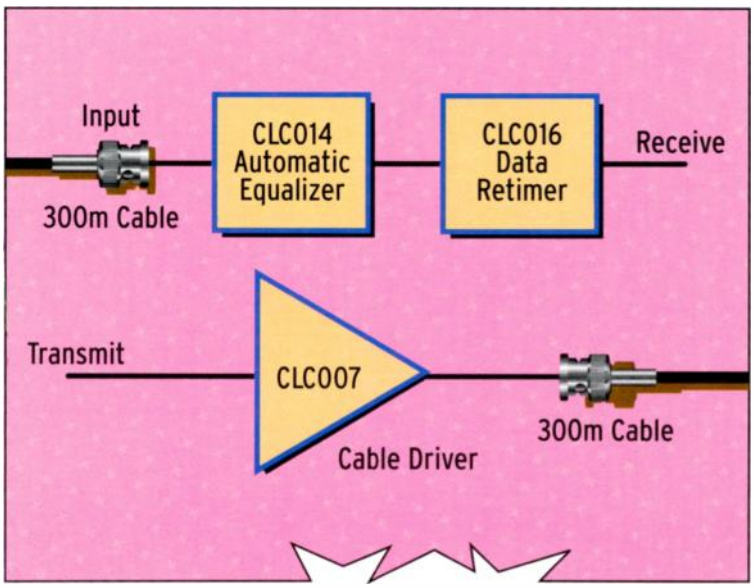
SERIAL DIGITAL INTERFACE CHIP SET

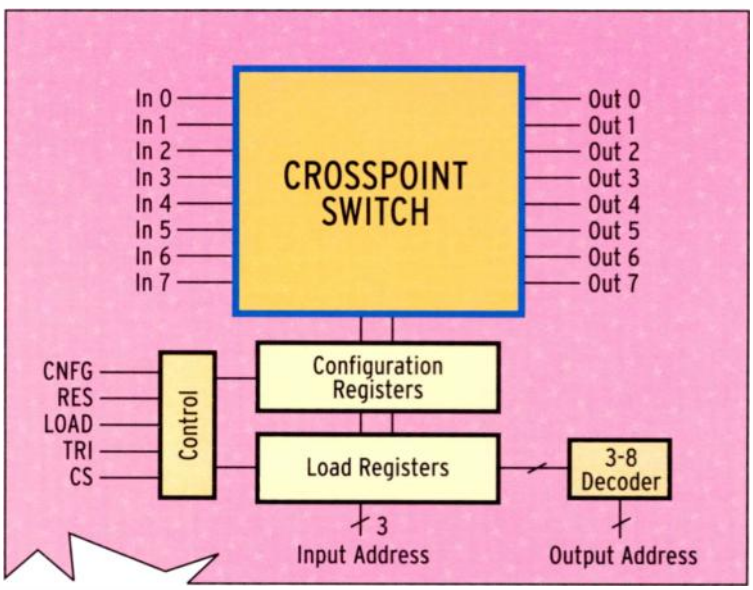


National's Comlinear Serial Digital Interface Chip Set CLC007/014/016

Together, these high-speed, high-performance devices provide links that assure clear, strong, consistent signals over hundreds of meters of cable.

- Automatic equalization for cable links of up to 300m with no user input required
- Throughput at speeds up to 400Mbps
- Automatic switching between four user-selected data rates, e.g. 52Mbps, 100Mbps, 155Mbps, and 400Mbps

DIGITAL CROSSPOINT SWITCH



Crosspoint Switch CLC018

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OP AMPS/PGBs

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NEW SILICON DUST OP AMPS

	Single LMV821	Dual LMV822	Quad LMV824
GBW (MHz)	5	5	5
Supply Voltage	2.5-5.0	2.5-5.0	2.5-5.0
I_S (mA)	0.5	0.8	1.12
Slew Rate (V/µs)	2.0	2.0	2.0
R-to-R Output	Yes	Yes	Yes
Packages (shown actual size)	SOT23-5, SC70-5	SOIC-8, MSOP-8	SOIC-14, TSSOP

SOT23-5 SOIC-8 SOIC-14 SC70-5 MSOP-8 TSSOP

FAMILY AVAILABLE IN SOT23-5 PACKAGES

	CLC450	CLC451	CLC452	CLC453
Product Type	Amp	PGB*	Amp	PGB*
Bandwidth	100MHz	85MHz	130MHz	110MHz
Supply Current	1.5mA	1.5mA	3mA	3mA
Output Current	100mA	100mA	100mA	100mA
Slew Rate	280V/µs	260V/µs	400V/µs	370V/µs
2nd/3rd Harmonic Distortion 2Vpp @ 1MHz	-79/-75	-66/-75	-78/-85	-65/-84

+5V Performance specifications

*Programmable Gain Buffer (PGB)

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National's economical replacement for CMOS op amps, bringing miniaturized packaging and high performance to low-voltage portable applications.

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- Rail-to-rail output
- SC70, SOT-23, MSOP, TSSOP, and SOIC packages

High-Speed Amplifier and Programmable Gain Buffer Family in SOT23-5 Packages CLC450/1/2/3

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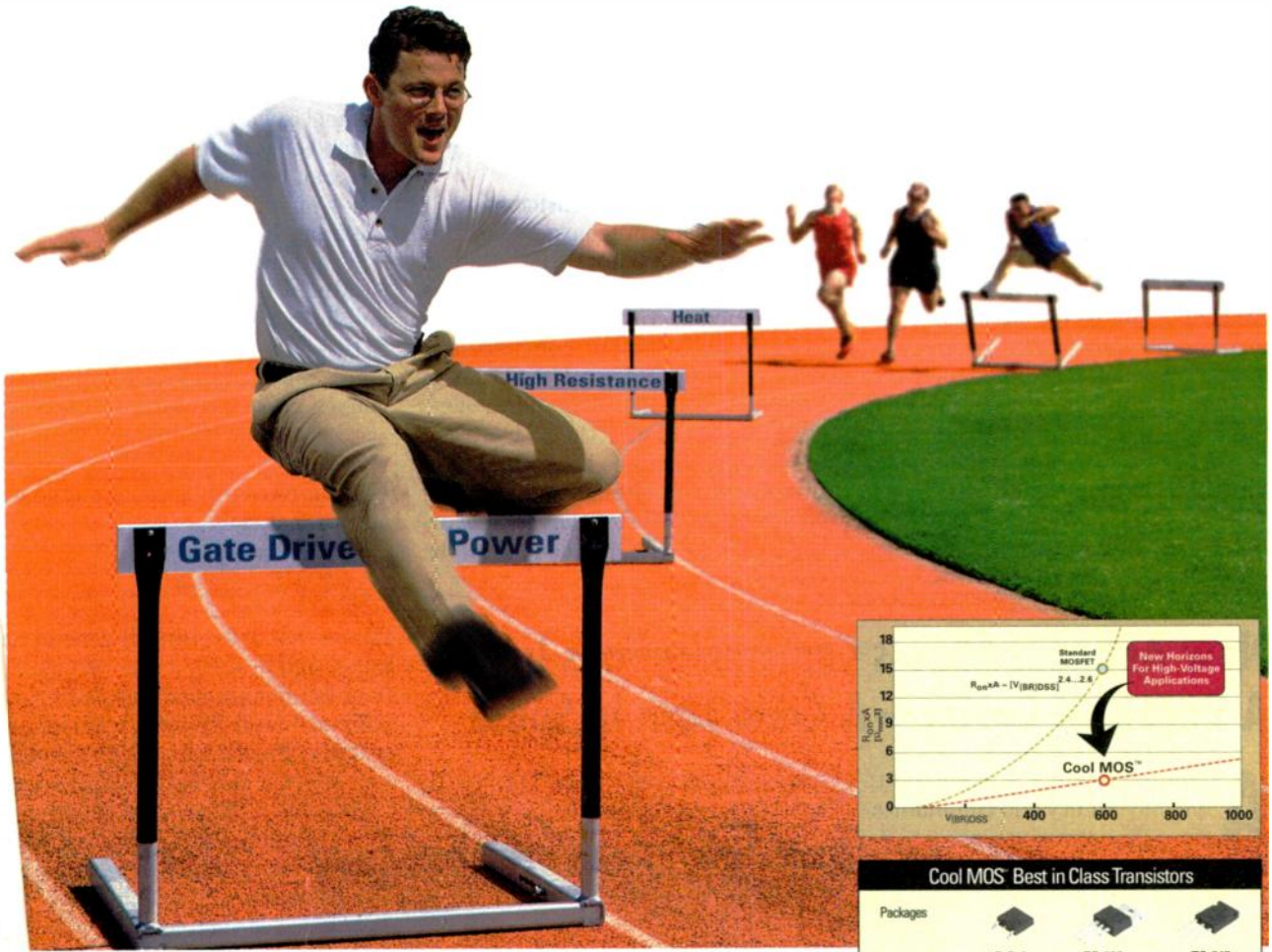

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Packages	D-Pak	TO-220	TO-247
600V	600mΩ	190mΩ	70mΩ

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READER SERVICE 151

and discretion to use the memory more efficiently. The system "directs" memory in managing requests.

Designers at NEC compared a VCM-enhanced Rambus DRAM (four channels, 1-kbyte row cache) to a low-latency standard RDRAM (two banks, 2-kbytes write-through internal cache). Although the peak bus bandwidth is the same, the VC RDRAM offers better throughput for both large- and small-block accesses. For large-block accesses, the VC RDRAM delivers 290 Mbytes/s, while the standard chip runs at 178 Mbytes/s. Similarly, for small-block accesses, the VC RDRAM runs at 196 Mbytes/s. For the standard RDRAM, the interface runs at 110 Mbytes/s.

In this comparison, the VC version works with four different memory masters, with one channel per memory master. Large-block burst lengths are defined as 16 bytes for screen refresh and 8 bytes for bit-block transfers and polygon draws. Small-block accesses use half the number of bytes.

In a 3D graphics system, the VCM interface can improve data transfers by permitting the frame buffer to handle several concurrent tasks. It also refreshes the server and updates the display. By interspersing the screen-refresh accesses with texel read-and-write and other screen-write accesses, the VCM interface can handle the transfers with a relatively simple foreground/background timing sequence *(see the figure)*. All the accesses are made to different rows of either the same bank or other banks.

In conventional memories, such as SDRAMs and DDR SDRAMs, the memories must have precharge and activate operations, which require up to six clock periods. The data for these accesses in VCM-based chips is already preloaded in the virtual-channel row buffer. The accesses on these channels are performed as read- and channel-write operations. They will consistently have the lowest latency.

Most Overhead Eliminated

Activate and precharge operation times are about one-tenth that of an SDRAM. These are done as part of the background operating mode, which allows them to be done concurrently with the channel read/write foreground operations. Most of the overhead associated with the activate and precharge functions is eliminated in this way. In an intense multitasking environment, the row switching overhead can take up more than half of the DRAM operating efficiency. By eliminating most of this overhead, this approach can achieve up to 2.5 times the performance of standard DRAMs.

In the system timing diagram, VCM channels 0 and 1 work in tandem, and are used for screen-refresh operations. When all the data in channel 0 is read out, the system switches to channel 1, allowing channel 0 to be reloaded with new data. Texel reads are done with channels 2 and 3, which are used for reading texture maps—either two different textures or two different "levels of details," as needed in trilinear interpolations. Texel writes to screen memory are done on channel 5, while screen writes are performed on channel 4. Additional channels can be assigned, or used, when other pipelined tasks need to access the frame buffer.

The company expects to sample a 64-Mbit VCM SDRAM this quarter, and both a VCM SGRAM and DDR SDRAM before the end of this year. Chip-set suppliers and alternate-source memory-chip suppliers will also be announced later this year.

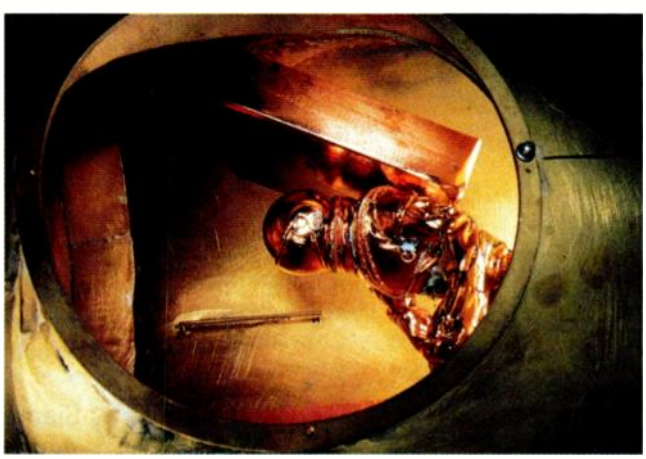
For more information, contact NEC at (408) 588-6000, or on the web at www.nec.com.

Dave Bursky

New Antenna Allows Communications Inside A Resonant Cavity—A Crew Lock In Space

A unique antenna is expected to enhance safety and communications for astronauts as they prepare for challenging space walks. Developed by the Georgia Tech Research Institute (GTRI) in Atlanta, the Orlan antenna was designed for the NASA-led International Space Station. This 2-ft. long "loop" design is intended for the crew lock, a cramped, cylindrical air lock that can hold two astronauts outfitted in spacesuits.

Lab researchers, together with the Boeing Co., Everett, Wash., have been working on this project since last year. The greatest technical hurdle involved the antenna's location within the crew lock. "Ordinarily, antennas go on an exterior surface; this one needs to go inside a metal container and provide a radio-frequency field for communications there," explained Victor Tripp, a principal research engineer with GTRI's Sensors and Electromagnetic Applications Laboratory. "Ordinary techniques don't apply, because a radiation pattern is meaningless inside a resonant cavity."



The crew-lock antenna for the International Space Station was developed with the aid of a one-sixth scale model. Test frequencies were raised by a factor of six to maintain the ratio of wavelengths to physical dimensions.

The antenna provides communication for International Space Station astronauts, who will use Russian-designed spacesuits. These spacesuits employ the same communication frequency used for many years aboard the Russian spacecraft, Mir. This frequency is four times lower than the frequency used by U.S. spacesuits, which have their own antenna within the crew loc The Russian wavelength barely short enough to re onate in the crew lock's 65-i

diameter. This require an antenna so large that it must also act as a handrail.

Dependable operation of the crew-lock antennas is essential. While astronauts wait within the crew lock in their spacesuits, these antennas transmit verbal communications to the crew as well as data for monitoring each astronuat's phusical condition.

To develop an optimal antenna design, Tripp and other GTRI researchers first performed calculations using High-Frequency Structure Simulator (HFSS) modeling and simulation software by Ansoft, Pittsburgh, Penn. They augmented those findings with their own 1:6 scale model of the crew lock. The researchers even developed a scale model of an astronaut, with a conductive spacesuit that simulated the Russian spacesuit design *(see the photo)*. A metallic layer in the Russian version lets the whole suit function as an antenna.

The researchers even scaled the frequencies. The "full-size" frequencies of around 120 MHz were adjusted upward to about 720 MHz so that wavelength and crew lock dimensions would maintain their proportions.

Such detailed effort seems to be paying off. At NASA's Johnson Space Center, Houston, Texas, the loop antenna in Boeing's full-scale crew-lock model was recently tested. According to Tripp, it produced data that closely resembled data from the scale model.

Dependable operation of the crew-lock antennas is essential. While astronauts wait within the crew lock, these antennas carry verbal communication between astronauts and the crew. They also transmit vital signs and other data needed to monitor each astronaut's physical condition. For instance, each spacesuit's umbilical cord provides coolant to keep astronauts from overheating inside the highly insulated spacesuit. Temperature data transmitted from the crew lock lets the space station's communication center make sure the cooling system is operating properly.

The test loop antenna was made of copper; the final, space version will be high-strength aluminum. It will perform almost identically to copper.

For more information, check the Georgia Tech Research Institute web site at www.gtri.gatech.edu/ rco.html.

Joseph Desposito

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MAX 7000E	32–256	6 ns	5.0 V	3.3 V, 5.0 V	X		
MAX 7000S	32–256	5 ns	5.0 V	3.3 V, 5.0 V	X	X	X
MAX 7000A	**32–1,024**	**5 ns**	**3.3 V**	**2.5 V, 3.3 V, 5.0 V**	**X**	**X**	**X**

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The ALTERA Advantage

New Development Tools Keep Java Percolating

Code Generation Is Getting Easier Thanks To A Plethora Of Discrete Tools And Integrated Development Environments.

Ralph Spindell

SPECIAL REPORT

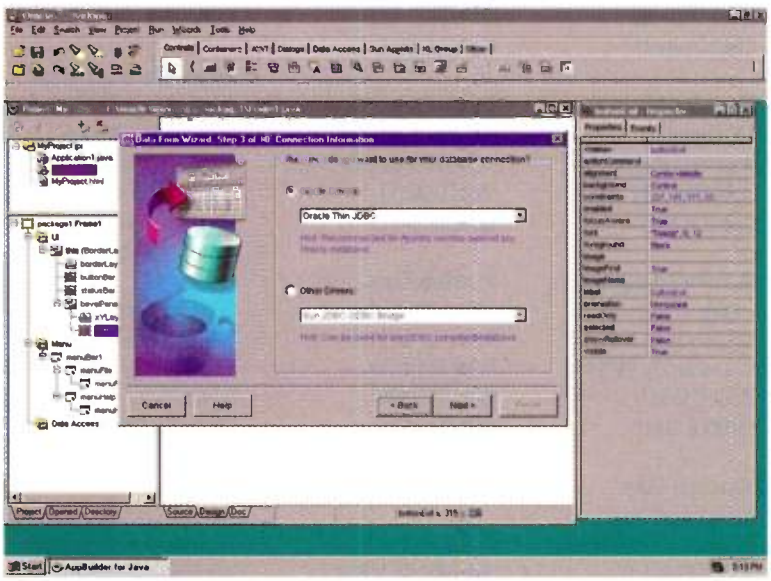
With the right tools, Java could replace C++ or Visual Basic as IT professionals' development language of choice. In a nutshell, Java development needs to become faster, better, easier, and cheaper. And tool vendors are trying to make that happen. There are over 360 tools available for serious, professional Java development. In addition, the language specification and core-application programming interfaces (APIs) are maturing. So, fire up the Integrated Development Environment of your choice, load up your toolkit, and give Java a spin.

To write professional-quality Java code, the serious developer relies on a burgeoning set of Java development tools. Even at this early stage in the Java language's life-cycle, a broad range of development tools and aids are currently available. Many third-generation and high-level development tools have been available for other, more mature languages, such as C++. Now, they are reaching into the Java sector. Java's unique approach to object-oriented programming, and its promise of a write-once, run-anywhere, virtual-machine architecture, has created a need for a new class of Java code-development tools.

While the default Java API offers a rich set of classes, Java development-tool suppliers are filling the gaps in performance, security and third-party libraries for electronic commerce, business objects, and other needs. Also, Java's small-size bytecode portability makes it ideal for the embedded and real-time systems markets. This is spawning a series of Java tools specifically for embedded-systems design. This article, however, focuses on tools for traditional Java applications.

Tool categories range from the discrete to the complete. Discrete tools focus on a specific area of Java development, such as debuggers, class browsers, testing and quality-assurance tools, profilers, and porting tools.

There's also installation and distribution, database connectivity, client/server, thin-client, and server-side development tools, as well as embedded-systems tools, class libraries, component "Bean" libraries, and graphical-user-interface (GUI) toolkits. Most discrete tools are available in the more comprehensive development suites.



Art Courtesy: Oracle Corp.

Complete suites of tools are also available: Integrated Development Environments (IDEs) and Workbenches, third-generation Rapid Application Development (RAD) visual design and authoring tools, and CASE tools that support or generate Java code. Other tools for developing Java code include preparsers, code and version management, documentation tools, and just-in-time compilers. With the advent of JavaBeans—a component-based architecture—comes tools for Rapid Application Development. RAD tools let you use pre-

made components, which can be connected or wired together using a visual programming method.

Definitions of various categories of development tools follow, as well as capsule descriptions of some products available within each category. Authoring tools and applet-generation tools, geared towards the non-developer, are not discussed in this article.

Integrated Development Environments: You'll probably write your first simple "Hello World" application using a text editor and the Java Development Kit's command line compiler and AppletViewer. After that, you will almost certainly want to use a comprehensive Integrated Development Environment or Workbench.

An IDE provides a comprehensive set of development tools for code editing, visual layout of components, compiling, interactive debugging, searching and browsing—all in one package. Some IDEs also provide internal project management or more comprehensive source-code and version control. IDEs also tend to fall into two main classes: file-based IDEs, which store your project in standard system files, and repository-based, where all code is stored in specialized databases. Repository-based IDEs tend to have an advantage in team programming environments, as the repository methodology assists in sharing and maintenance for both codes and objects.

There are dozens of IDEs. Many of those are available from major players, such as Sun's Java Studio and Java WorkShop products, Symantec's Visual Café Pro, Silicon Graphics'

Companies Mentioned In This Article

CosmoSoftware Inc.
2011 N. Shoreline Blvd.
Mountain View, CA 94043
(888) 912-6766
CIRCLE 553

Eastridge Technology
85 Winant Rd.
Princeton, NJ 08540
(609) 252-0825
CIRCLE 554

4th Pass Software Corp.
810 32nd Ave. South
Seattle, WA 98144
(206) 329-7460
CIRCLE 555

IBM North America
1133 Westchester Ave.
White Plains, NY 10604
(800) IBM 4 YOU
CIRCLE 556

Innovative Software GmbH
Kaiserstr. 65
60329 Frankfurt/M
Germany
49 69 236929
CIRCLE 557

INPRISE Corp.
100 Enterprise Way
Scotts Valley, CA 95066
(408) 431-1000
CIRCLE 558

Intuitive Systems Inc.
599 N. Mathilda Ave.,
Suite 19
Sunnyvale, CA 94086
CIRCLE 559

KL Group
260 King St. East
Toronto, Ontario
Canada M5A 1K3
(416) 594-1026
CIRCLE 560

Marimba, Inc.
440 Clyde Ave.
Mountain View, CA 94043
(650) 930-5282
CIRCLE 561

Mercury Interactive Corp.
1325 Borregas Ave.
Sunnyvale, CA. 94089
(800) TEST-911
CIRCLE 562

Microsoft Corp.
One Microsoft Way
Redmond, WA 98052-6399
(425) 882-8080/
(800) 621-7930
CIRCLE 563

NobleNet Inc.
337 Turnpike Rd.
Southboro, MA 01772-1709
(508) 460-8222
CIRCLE 564

NuMega Technologies Inc.
9 Townsend West
Nashua, NH 03063
(800) 4-NUMEGA
CIRCLE 565

ObjectShare Inc.
16811 Hale Ave. Suite A
Irvine, CA 92606
(949) 833 1122
CIRCLE 566

Oracle Corp.
500 Oracle Parkway
Redwood Shores, CA 94065
(800) ORACLE1
CIRCLE 567

ParaSoft Corp.
2031 S. Myrtle Ave.
Monrovia, CA 91016
(626) 305-0041/
(888) 305-0041
CIRCLE 568

PowerBBS Computing Inc.
35 Fox Ct.
Hicksville, NY 11801
(516) 938-0506
CIRCLE 569

Progress Software Corp.
14 Oak Park
Bedford, MA 01730
(781) 280-4000
CIRCLE 570

Rational Software Corp.
18880 Homestead Rd.
Cupertino, CA 95014
(408) 863-9900
CIRCLE 571

Reliable Software Technologies Corp.
21515 Ridgetop Circle,
Suite 250
Sterling, VA 20166
(703) 404-9293
CIRCLE 572

Rogue Wave Software, Inc.
5500 Flatiron Parkway
Boulder, CO 80301
(303) 473-9118/
(888) 442-9641
CIRCLE 573

Stingray Software Corp.
9001 Aerial Center,
Suite 110
Morrisville, NC 27560
(800) 924-4223/(919) 461-0672
CIRCLE 574

Sun Microsystems Inc.
901 San Antonio Rd.
Palo Alto, CA 94303
(650) 960-1300
CIRCLE 575

SuperCede Inc.
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Suite 390
Bellevue, WA 98004-5840
(425) 462-7242
CIRCLE 576

Sybase Inc.
6475 Christie Ave.
Emeryville, CA 94608
(800) 395-3525
CIRCLE 577

Symantec Corp.
175 W. Broadway
Eugene, OR 97401
(541) 334-6054/
(800) 441-7234
CIRCLE 578

TakeFive Software Inc.
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Suite 200
Cupertino, CA 95014
(408) 777-1440
CIRCLE 579

TV Objects Ltd.
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Princeton, NJ 08540
(609) 514-1444
CIRCLE 580

WingSoft Corp.
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Fremont, CA 94537
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68HC705C8A	8K	304	31	40-DIP, 44-PLCC, 44-QFP
68HC705C9A	16K	352	31	40-DIP, 44-PLCC, 44-QFP
68HC705J1A	1.2K	64	14	20-DIP, 20-SOIC
68HC705L16	16K	512	39	80-QFP
68HC705P6A	4.6K	176	21	28-DIP, 28-SOIC

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Cosmo Code 2.5, Asymetrix's SuperCede, and Microsoft Visual J++.

Sun's Java WorkShop includes support for the latest JDK 1.1 and JFC 1.1 "Swing" components, a fast compiler, and a just-in-time compiler built into the Java Virtual Machine. A new profiler is included for identifying bottlenecks. And, a powerful, flexible debugger with remote capability permits you to debug from anywhere on the network. There's also JavaBean support for creating, importing, and reusing components, as well as a visual Java GUI builder. In addition, there's ObjectStore, a Java object persistent-storage engine (PSE) for developing Java database applications which are portable over the network. You also get MindQ's interactive tutorial on JavaBeans and Java WorkShop.

www.sun.com/workshop/java

IBM VisualAge for Java is a repository-based IDE. Its unique design provides a highly dynamic development environment. VisualAge keeps everything compiled all the time, and maintains a list of unresolved inconsistencies. You can run any class, or execute arbitrary code fragments, in the scrapbook window. There is no distinction between running, debugging, and editing code while debugging. The repository-based storage system allows for robust version control/change management and team collaboration. Enterprise Access Builders eliminates programming database-dependent embedded SQL in the application. It also generates Bean components and middleware code that connect the Java client to existing transaction, data, and application servers.

www.software.ibm.com/ad/vajava

Asymetrix SuperCede is a high-performance IDE with complete support for JDK 1.1 and JavaBeans. SuperCede offers a high level of dynamic operation through its interactive Flash Compiler. This compiler lets you instantly see the effect of changing or adding new code to your application—while it runs. The RAD debugger includes innovative features, like the ability to interactively test new source-code fragments and expressions. By associating a series of legal Java statements with a tracepoint, ActionPoints permit you to easily debug complete problems. With the BackTrack feature, you can fix a problem in the current method, backtrack to before the method was called, and retry the modified method. The Data Browser allows you to connect to and browse legacy databases, as well as drag and drop tables and columns into the form editor. Java Data Objects provides a complete object-oriented interface to JDBC.

www.supercede.com

Created by Silicon Graphics, Cosmo Code 2.5 is a third-generation tool comprised of an integrated set of powerful and highly visual tools for creating Java applications, applets, and classes. Cosmo supports the entire development cycle: designing, debugging, and delivering. It comes with AWT 1.1-compliant class libraries from Rogue Wave, one of the leaders in object-oriented components, as well as JTools, JWidgets, JChart, and JDBTools. The product generates JDK 1.1-compliant code for applications, JDK code 1.0 when the target environment is a browser. It even generates 1.1 objects with the 1.0 event model. There's also a very-comprehensive static-analysis tool and class browser, graphical debugger, and project-management features.

www.cosmo.sgi.com

Symantec's Visual Café Professional is a very popular RAD IDE that supports JDK 1.1.5, JavaBeans and JFC (Java Foundation Classes, Sun's GUI toolkit). Along with a JavaBean Editor, it has an Interaction Editor, which minimizes the coding needed to develop JavaBeans and wire them together. Another feature is an open API. Visual Café sports the fastest just-in-time compiler for Java. The Database Development Edition adds support for over 30 databases through JDBC and ODBC, and includes dbANYWHERE, a 100% JDBC-compatible middleware server with native drivers for Oracle, Sybase, SQL Server, Access, and JDBC/ODBC.

www.symantec.com/

Visual J++ 6.0 from Microsoft provides productivity features such as a fast Java compiler, debugger, GIF/JPG editor, macro scripting, and a post-build process for packaging. Its very Windows-centric approach supports ActiveX, and allows Java developers to build and deploy high-performance, data-driven client/server solutions for the Windows operating system and the Web. It supports the Windows Foundation Classes (WFC), an object-oriented framework designed to provide easy access to the full power of the Windows platform. WFC lets developers build high-performance, native Windows-based applications using the Java programming language. Visual J++ provides complete access to the native Windows Win32 API through J/Direct API architecture. *www.microsoft.com/visualj*

JBuilder from Borland International features JavaBeans component creation, a scalable database architecture, visual "Two-Way" development tools. It also produces "100% Pure Java" platform-independent applications, applets, servlets, and JavaBeans. The product's open environment supports JDK 1.1.x, JDK 1.2, JFC/Swing components, JavaBeans, Enterprise JavaBeans, CORBA, RMI, JDBC, and all major corporate database servers. It also includes Mocha and Crema—a decompiler and its companion obfuscator. Their Client/server Suite comes with VisiBroker for Java, which is Borlands CORBA technology. Included are over 200 JavaBean components ,with source code and tools for creating and managing JavaBeans. Note: Borland has changed its name to InPrise.

www.inprise.com/jbuilder

Oracle's JDeveloper Suite 2.0 lets you use Java to build server-based solutions. JDeveloper Suite includes AppBuilder for Java, Oracle Application Server 4.0, OracleData Server, and Symantec's Visual Page HTML editor. With a broad range of database connectivity options, AppBuilder's IDE is well-suited for building sophisticated, enterprise-class database applications. Oracle plans to support Java on all three tiers of the network computing platform.

With AppBuilder's integrated SQLJ—a pre-compiler for embedding SQL directly in Java source code—developers can create reusable JCORBA cartridges. These components contain business logic written in Java. They are accessed through an embedded CORBA 2.0-compliant ORB for deployment on the Oracle Application Server. Future support for Enterprise JavaBeans is planned.

www.oracle.com/products/tools/jdeveloper

PowerJ, from Sybase, is an enterprise application-development envi-

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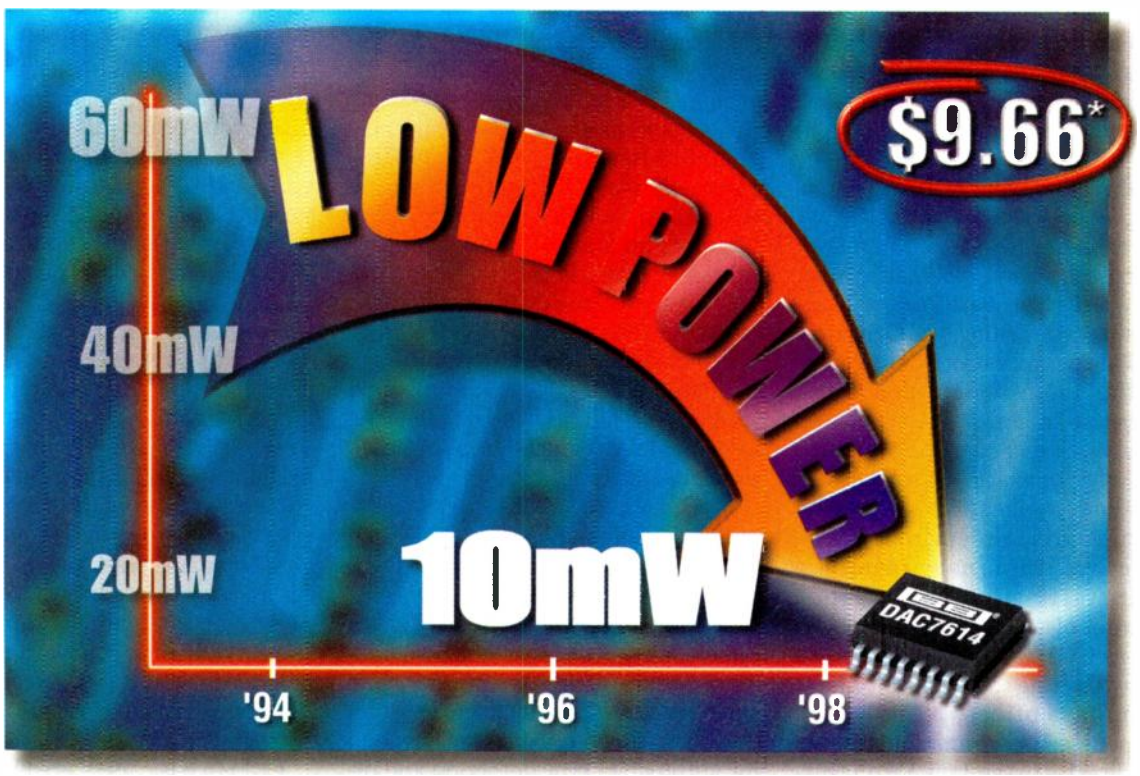

The DACs Are Back!

Burr-Brown's new quad, 12-bit DACs are the first in a new series of BiCMOS D/A converters featuring a voltage output specifically designed for single-supply or low voltage dual-supply applications.

Low Cost

At less than $2.50 per converter, these quad DACs are an ideal solution for multiple output applications such as process control, motor control, ATE, analytical and portable instrumentation.

A DAC Guarantee

DAC7614, **DAC7615**, **DAC7624** and **DAC7625** have guaranteed channel-to-channel matching of linearity to ±1LSB, unipolar zero to ±2LSBs, and bipolar zero to ±1LSB. Plus, they offer 10µs max settling time at only 2.5mW/DAC power dissipation in single supply operation.

Precision Solutions

Burr-Brown has a wide selection of 12- to 18-bit D/A converters featuring competitive pricing! See our web site for a complete listing.

Product	Resolution (Bits)	INL (LSBs)	DNL (LSBs)	Guaranteed Monotonicity	Interface	DAC Interface Features	FAX*LINE*# (800) 548-6133	Reader Service #
DAC7614	12	±1	±1	–40°C to +85°C	Serial	Individual DAC Update	11445	80
DAC7615	12	±1	±1	–40°C to +85°C	Serial	Simultaneous DAC Update	11443	81
DAC7624	12	±1	±1	–40°C to +85°C	Parallel	Output Reset to Mid-Scale	11419	82
DAC7625	12	±1	±1	–40°C to +85°C	Parallel	Output Reset to Zero-Scale	11419	83

*Priced from $9.66 in 1000s. Recommended resale in USD. FOB USA.

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ronment for business applications, in a multitier distributed-computing environment. If you're new to Java, features like the Reference Card and Parameter wizards assist your learning curve with drag-and-drop programming methods. There's complete support for JavaBeans, ActiveX, and CORBA. A set of data-aware components can be used with any JDBC source to create enterprise database applications. PowerJ includes Sybase SQL Anywhere, a middleware application server, and jConnect, Sybase's JDBC driver. PowerJ has a high level of integration with Powersoft Jaguar CTS, a component transaction server, and Sybase Dynamo, a dynamic data-driven web server. *www.sybase.com*

Optimization, Testing, and Debugging Tools: Thorough testing, debugging, and optimization of Java applications will increase reliability, performance, and quality. Standard testing requires writing a script which plays out on the GUI of your application—supplying program control and data from a user's perspective. This usually requires a separate testing tool and script on each target platform you are developing for, as GUIs would be different on each. Java testing tools, however, have a leg up. Java utilizes a single code base among all platforms and delivers events directly to the Java Virtual Machine. This bypasses the GUI, eliminating the difficulties to automated testing posed by different GUI controls on different platforms, and "stretchable" GUI components. Optimization tools look for performance problems and bottlenecks in your code by profiling your applications performance and resource utilization.

JavaStar, from Sun Microsystems, was the world's first tool to test at the language level. It automatically records user actions and generates test scripts in pure Java. The scripts can be edited in your standard IDE, and work across all platforms. JavaStar also provides comparison testing among platforms, and regression testing among versions of your software. *www.sun.com/suntest/JavaStar*

Reliable Software Technologies offers a set of practical, early-life-cycle testing tools for developers and testers to identify and remove bugs at the earliest stages of development. The set includes DeepCover, a test-coverage tool that reveals how well your code is tested. Another tool, called TotalMetric, captures and displays traditional complexity/effort and advanced object-oriented metrics. AssertMate, a code-assertion system for Java, supports data assertions, pre- and post-conditions, and invariants to validate code correctness. *www.rstcorp.com*

OptimizeIt 2.0, from Intuitive Systems, is a comprehensive Java profiling tool. It permits developers to track performance issues in Java programs. You can determine how your application uses memory and CPU resources, as well as detect excessive object allocations and time-consuming algorithms. *www.optimizeit.com*

Mercury Interactive Corp. provides WinRunner and Xrunner for functional testing of Java clients. LoadRunner load-tests Java-based systems, and TestDirector manages testing of Java-based applications. *www.merc-int.com*

Jtest, from ParaSoft Corp., is an excellent Java debugging tool which can even locate uncaught run-time exceptions. *www.parasoft.com/jtest*

Numega DevPartner, for Java's SmartDebugging tools, helps you deliver fast, reliable Java applications and components. Available from Compuware Numega, it includes Jcheck for automatic error detection and diagnosis, and TrueTime for automatic performance analysis and optimization. Jheck's unique EventDebugging technology captures system and runtime events for detailed analysis, and has advanced thread monitoring and debugging capabilities. *www.numega.com*

Installation and Distribution Tools: Installing your Java application onto target platforms can be pretty difficult. Problems arise because each target operating system has different methods for invoking application programs; a Java Virtual Machine may or may not already exist on the target platform; and, if it doesn't exist, it will need to be installed.

InstallAnywhere 2, from Zero G Software, is an authoring tool for distributing Java software and creating installation scripts. The tool creates a universal multiplatform installer that runs on any system. It also installs the Java Virtual Machine run-time environment, if needed, on the target system. Icons, shortcuts, or shell scripts are installed, if appropriate, on the target platform to launch your application. A unique Web Install feature allows installations directly from the Internet. *www.zerog.com*

Marimba's Castanet is an infrastructure that enables the automatic distribution and management of applications and content over the Internet. These items include Java applications, Java applets, JavaBeans, web pages, and other types of content. To use Castanet, your target platform must have the Castanet Tuner installed. And, you need to be running a Castanet server to deliver your applications or content. *www.marimba.com/products*

Porting and Code-Translation Tools: Porting tools generate Java bytecode from other languages. This allows a developer to leverage his existing codebase and experiences in another language, such as C++ or Visual Basic. Translating code can also act like a bridge to learning Java development. After conversion, you can read the generated source code and see how your algorithms and classes look in Java. This can assist your learning curve.

Applet Designer Enterprise 1.7, from TvObjects, is an add-in component for Visual Basic that converts entire Visual Basic projects to Java. www.tvobjects.com/products/enterprise.html

C2J is a basic freeware C++ to Java translator, available courtesy of Chris Laffra of the IBM T.J. Watson Research Center, Yorktown Heights, N.Y. *members.aol.com/laffra/c2j.html*

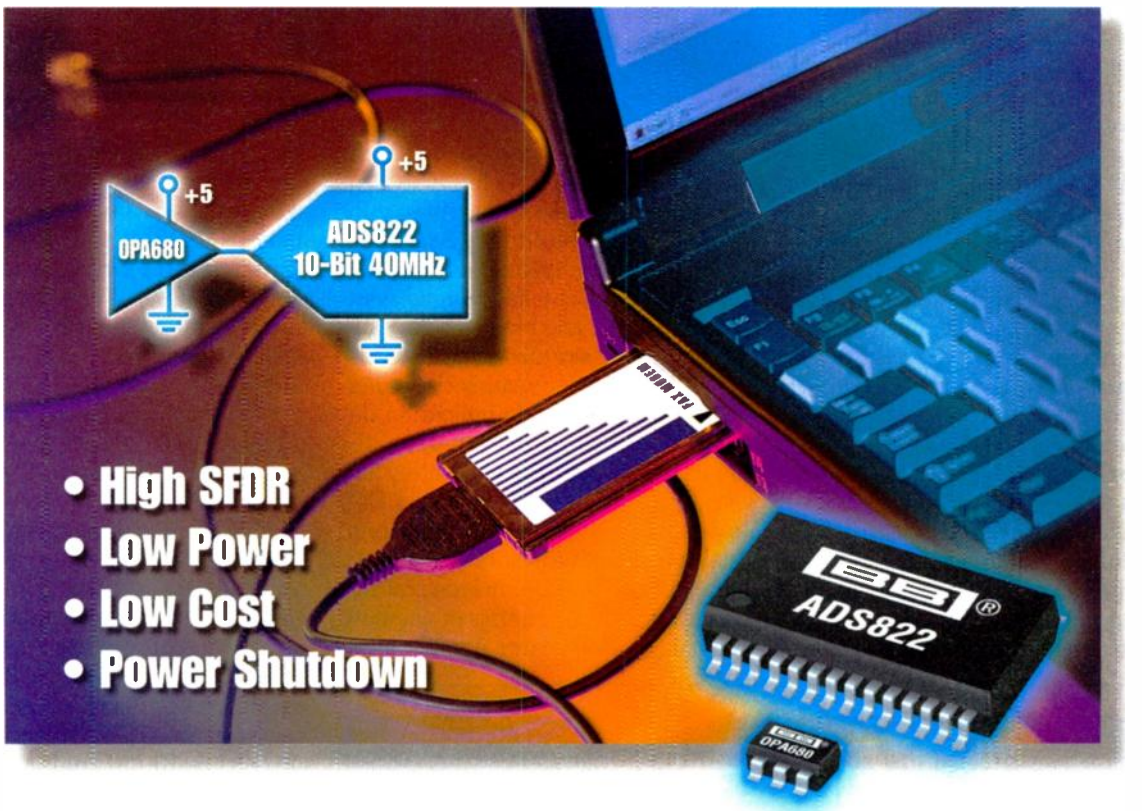
Delphi2Java Database Edition, from PowerBBS Computing, converts your Delphi code into Java applets or applications. *www.javadelphi.com/db.htm*

Decompilers and Obfuscators: Decompilers take a compiled .class file and try to reconstruct the original Java- compatible source-code file for the class (.java files). This comes in handy, for instance, when you've lost the source code for your own project, but have the binary compiled files. It can also be used, however, to reverse engineer another developer's class files to determine trade-secret algorithms, or to assist in software piracy. To protect your code from decompilation, another tool, called an obfuscator, can remove certain symbols from your class files and replace them with fake information intended to confuse decompilers.

Mocha, the first decompiler for

Speed PLUS™

Designed For Portability



A Dynamic Combination

Get the highest performance in a wideband 10-bit digitizer channel on a single +5V supply. OPA680 driving the ADS822 brings low power and price to your size constrained portable applications.

OPA680—+5V ADC Driver Solution

OPA680 is a unity gain stable voltage feedback op amp with optional power shutdown. OPA680's new internal architecture provides slew rate and full power bandwidth previously found only in wideband current feedback amplifiers. Using a single +5V supply, OPA680 can deliver a 1V to 4V output swing with over 100mA drive current and 150MHz bandwidth.

Key Specifications:

High Gain Bandwidth Product	300MHz
High Slew Rate	1800V/µs
Shutdown Power	1mW
Packages	SOT23-6, SO-8, DIP

OPA680 is priced from $1.79 in 1000s.*

ADS822—10-Bit, 40MHz Versatility

ADS822 is a new pipeline, CMOS A/D converter that operates from a single +5V supply. This high performance, low cost converter is complete with a 10-bit quantizer, high bandwidth track/hold, and high accuracy internal reference. ADS822 features low 200mW power dissipation, with an optional power shutdown, while providing a solid 60dB SNR through 20MHz signal inputs.

Key Specifications:

High SNR	60dB
High SFDR	72dBFS
Low Power	200mW
Package	28-lead SSOP

ADS822 is priced from $5.95 in 1000s.*

OPA680—FAX*LINE#* 11426 • Reader **84**

ADS822—FAX*LINE#* 11385 • Reader **85**

***Recommended resale in US dollars; FOB USA.**

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Java, is available at *www.brouhaha.com/~eric/computers/mocha.html*. Unfortunately, since the author recently passed away, it may not be updated anytime soon. Borland, however, has included Mocha and its companion obfuscator, Crema, in their Jbuilder product. Other decompilers include DeJaVu from Innovative Software GmbH *www.isg.de/OEW/Java/* and WingSoft Corp's WingDis *www.wingsoft.com/wingdis.html*.

Some available obfuscators are Eastridge Technology's Jshrink, *www.e-t.com/jshrink.html* and Hashjava (now called SourceGuard) from 4th Pass Software Corp., *www.sbktech.org/hashjava.html*. Crema, the companion of Mocha, was available at *java.cern.ch:80/CremaE1/DOC/index.html*. At the time this report was written, however, the URL was not operational.

Other Tools: TakeFive Software has a language-independent development environment that supports Java, SniFF+J. it's suitable for building large client/server applications utilizing both Java and C/C++. It allows working with multiple programming languages in one unified environment. The integrated object-oriented development environment offers code comprehension, configuration management, project management, and version control and documentation tools. It also provides the ability to manage teams of developers working on large projects in heterogeneous computing environments. *www.takefive.com/langjava.htm*

ObjectShare's Parts for Java Professional is a toolset designed to fully support teams building distributed applications. It offers integrated support for PVCS, tracks changes, compares versions, and manages development projects. *www.objectshare.com*

NobleNet's Nouveau is the industry's first distributed application-development environment. It is designed to automate the generating and integrating of diverse CORBA, COM, Java, and RPC-based applications. Previously, developers could only communicate through bridge translation layers. The benefits of the new technology are greater functionality, increased productivity, and improved performance. Nouveau takes a new and direct approach to middleware interoperability by implementing native interoperability directly in the applications. *www.noblenet.com/nouveau.htm*

Apptivity, from Progress Software Corp., is geared towards development of business-critical Java database applications. It provides tools to develop, test, and maintain Java business applications. Apptivity Server manages sessions, executes Java application logic, and handles database connectivity. *apptivity.progress.com/java/apptivity/apptivity.htm*

Rational Software Corp. makes a CASE tool with support for Java, called Rational Rose 98. This graphical component-modeling and development tool lets you model software applications. You can also perform graphical visualizations of your applications using the industry-standard Unified Modeling Language. Rational Rose 98 supports round-trip engineering. Visual Quantify lets you visually identify performance bottlenecks in your Java code. *www.rational.com*

JavaBean Component and Class Suppliers: Stingray offers JavaBean component libraries. Their Object Grid/J and Objective Blend tools package 30 Java/AWT extensions, which add professional GUI functionality to Java applications. *www.stingray.com*

The KL Group develops Jclass JavaBeans component libraries for professional GUI development. Available Beans include hierarchical grids, table, charting, data input and validation, as well as essential GUI components like tab managers, tree/outliners, and multi-column lists. *www.klg.com*

RogueWave Software offers StudioJ, a suite of integrated JavaBeans components, AWT and JFC GUI extensions, and grid, chart, and SQL database tools. *www.roguewave.com/ad/studioj*

Ralph Spindell is the founder and executive producer of WebSpin (www.spindell.net/webspin), a consulting company that specializes in e-commerce solutions for small and medium-sized businesses, and has provided consulting services to major corporations such as IBM. He can be reached at ralph@spindell.net or www.spindell.net for Internet consulting, e-commerce, and web site design.

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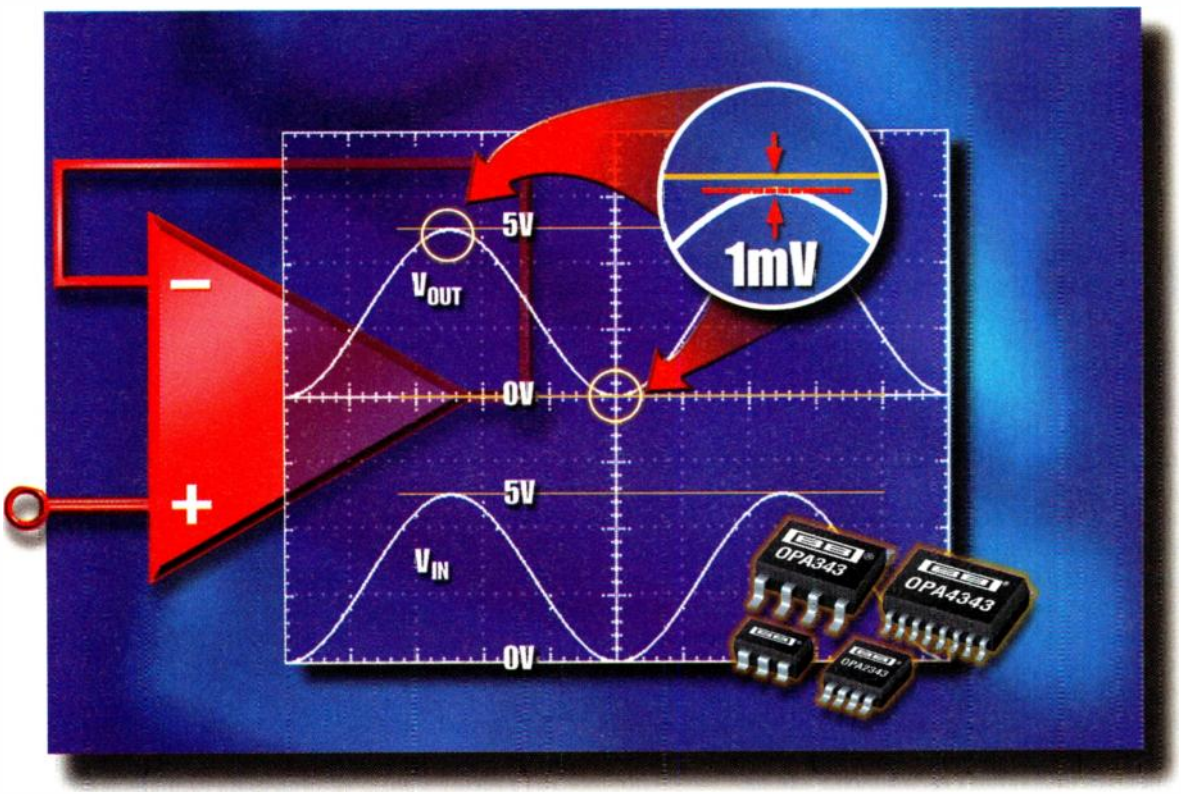
Low Cost Rail-to-Rail



Rail-to-Rail Input and Output

Burr-Brown's new **OPA343** series CMOS op amps provide the best rail-to-rail performance at an unbelievable price. Output swings to a mere 1mV from the supply rails with 100kΩ loads. With 10kΩ loads, output swings to within 10mV—better than you are using now. And, input common-mode voltage range extends 500mV beyond the supply rails, so it works in all circuit configurations, including G=1 buffer.

It's Fast, Too!

With 6V/µs slew rate and 5.5MHz bandwidth, the OPA343 is not just another *sloooow* CMOS amplifier. Its excellent dynamic performance and wide input/output swing make it great for audio applications or driving A/D converter inputs. Its low supply current (850µA) also makes it suited to a wide range of portable and battery operated equipment.

Single, dual, and quad versions—SOT-23, MSOP, SSOP, SO, and DIP—provide true design flexibility.

Key Specifications:

- Input Swing ..... 500mV beyond the supply rails
- Output Swing ..... 1mV from the supply rails
- Bandwidth 5.5MHz
- Slew Rate 6V/µs
- THD+N ..... 0.0007% at 1kHz
- Supply Range ..... +2.5V to +5.5V
- Quiescent Current 850µA/Channel

Package Options

OPA343 (single) ..... SOT-23-5, SO-8, 8-Pin DIP

OPA2343 (dual) ..... MSOP-8, SO-8, 8-Pin DIP

OPA4343 (quad) ..... SSOP-16, SO-14, 14-Pin DIP

OPA343 series priced from $0.26/channel (quad) in 100k.

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Embedded DSP Core Successfully Juggles Critical Design Parameters

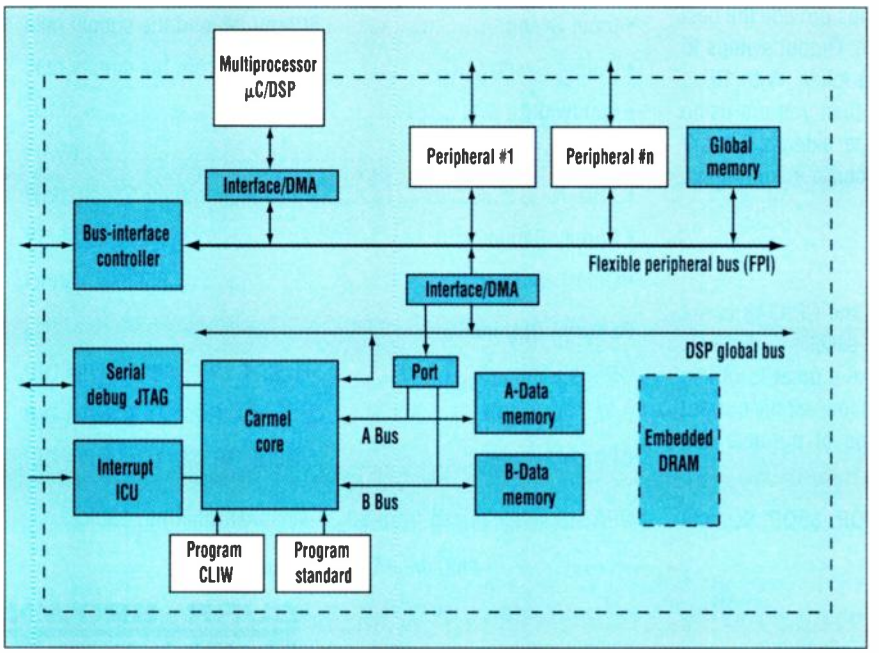
Satisfying High-Volume DSP Applications Calls For An Optimum Balance Between Performance, Price, and Power Consumption.

Alfred Vollmer

What about its performance? That's the question most designers ask whenever a new microprocessor or digital signal processor (DSP) architecture is introduced. If this performance does not outdo almost every comparable device, it will quite often not be considered a real breakthrough. In the real world, however, there are three basic "technical" criteria (nicknamed the three P factors) affecting a designer's opinion about whether a device is suited for a particular application: performance, power consumption, and of course, price. Finding a suitable balance between these three P factors is not an easy task at all.

But, that task has now become easier. Siemens Semiconductors, Munich, Germany, has announced a new DSP core architecture for systems on a chip. This architecture considers all three P factors simultaneously. Systems on-a-chip are typically employed in high-volume applications, such as consumer products like mobile phones, which leads to the price factor becoming a very sensitive issue. But, so are the other two P factors. For example, single-chip systems for GSM mobile phones require a significant amount of DSP performance and low power consumption. A long battery life has become one of their major themes in technical marketing.

Keeping these factors in mind, Siemens Semiconductors created Carmel, its new 16-bit integer-core architecture for embedded DSP applications. "We do not intend to receive the olympic gold medal for creating the DSP with the world's highest performance," states Dr. Reinhard Rueckriem, director of Siemens Semiconductor's DSP project group. "We concentrate on the commercially important parameters: performance, power, and price." Looking at Carmel's three P factors, Rueckriem first comments on the price, "We are looking for Carmel applications with really low power consumption, requiring chip prices in the $5-to-$10 range."



One of the architectural features of the Carmel DSP core is two independent data memories (Memory A and Memory B). These dual memories allow two memory operations to take place simultaneously. If the memories are dual-port types, four simultaneous accesses are possible.

M-MIPS

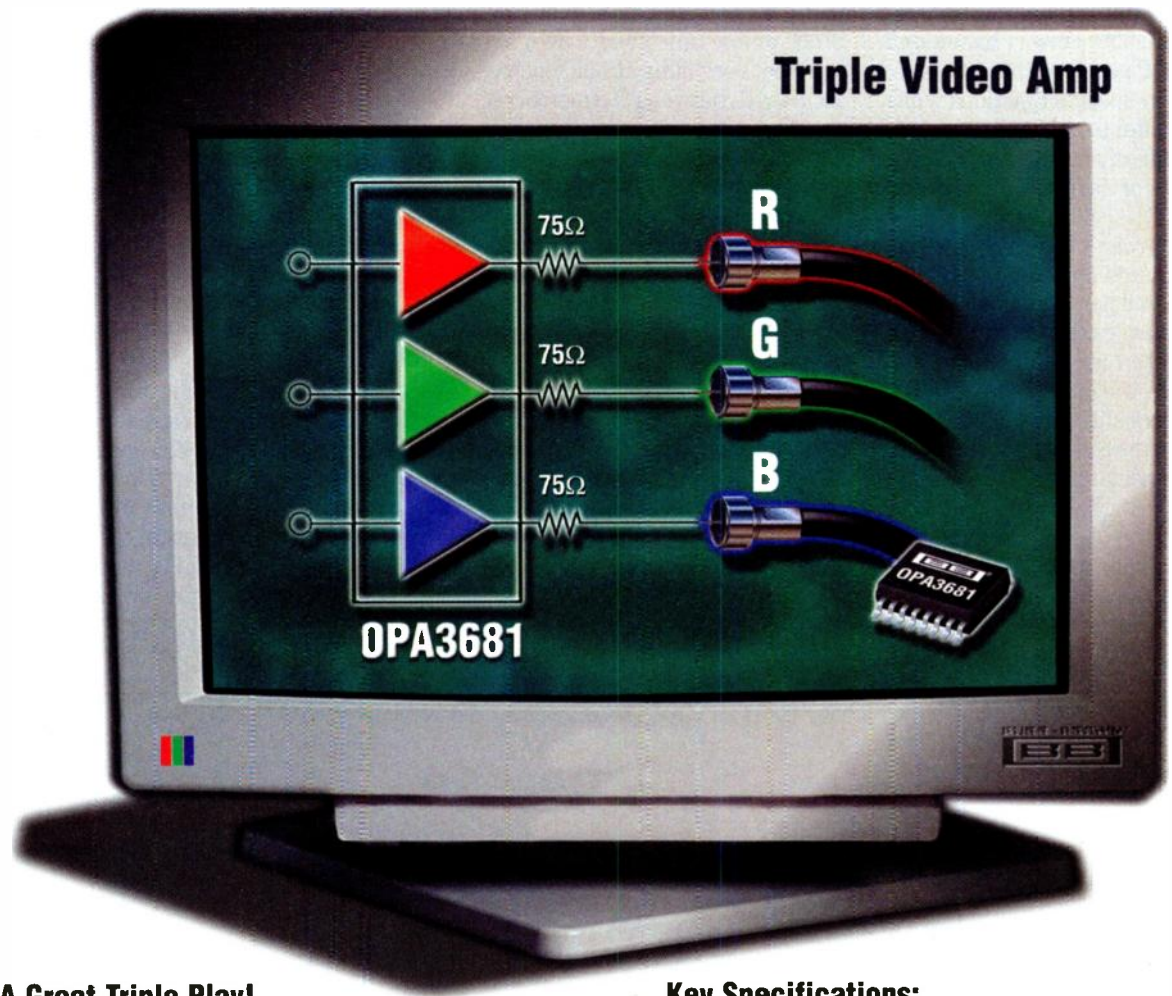
Until now, a device's overall performance was determined by multiplying the clock rate with the number of execution units. For example, 1600 MIPS (Million Instructions Per Second) would be the rating for a device with eight execution units running at 200 MHz.

To describe the performance of its new Carmel architecture, Siemens created a new physical dimension for measuring performance: M-MIPS (Multiple MIPS). Carmel offers a performance of 120 M-MIPS. As Carmel is able to perform up to 15 basic operations in parallel, its overall performance is higher than just 120 MIPS. Multiplying 15 parallel operations with 120 MIPS results in a performance of 1800 MIPS (in specific applications only).

Siemens did not use the conventional, speed-up-the-clock approach to achieve this high performance. Speeding up the clock increases power consumption and makes memory-access timing more critical. "We analyzed the main algorithms and tried to create an architecture that allows us to process the main algorithms within a lower number of clock cycles," explains Rueckriem. Of course, fewer clock cycles implies that the same performance may be achieved with a significantly lower clock frequency. Furthermore, Carmel allows the use of synchronous memories for data and program memo-

Speed PLUS™

High Res RGB Driver



A Great Triple Play!

The **OPA3681** is Burr-Brown's first triple op amp in the high-speed product family. Requiring a low 6mA/ch supply current, it features the high slew rate and low gain stability of a current feedback design with a high power output stage. OPA3681's optional disable is useful for power savings in portable devices, or implementing simple multiplexing circuits.

A +5V Single Supply Winner!

OPA3681's new output stage architecture delivers high output current with minimal voltage headroom and crossover distortion. Using a single +5V supply, the **OPA3681** can deliver a 1V to 4V output swing with over 100mA drive current and 150MHz bandwidth—an excellent RGB line driver or single supply ADC input driver. Priced from $3.79 in 1000s.

Key Specifications:

- Wideband +5V or ±5 Operation .....225MHz (G=+2)
- Output Voltage Swing.....±4.0
- High Output Current.....150mA
- High Slew Rate..... 2100V/µs
- Low Disabled Current..... 200µA/Ch
- Packaging SSOP-16

Key Applications:

- RGB Line Driver and/or 2x1 MUX
- Single Supply ADC Driver
- Wideband, High Gain Instrumentation Diff. Amps
- xDSL Line Interface

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ries. This results in power savings when compared to the use of asynchronous memories.

Carmel's core architecture can basically be called dual superscalar because it offers two multiply-and-accumulate (MAC) units. The core is based on a standard DSP architecture, extended by application-specific functions which operate parallel to the standard DSP part. The rule of thumb, "A program executes 90% of its instructions in 10% of its code" is closely related to Siemens' approach: operations which are only executed once are not as critical to the overall performance as operations which are executed in a permanently repeated way. Using the same program code, the inner loops are being run many times. As this code is only written once, the code itself may be bigger. But, the performance for every cycle needs to be high.

Placing several execution units in parallel is an appropriate means to increase the performance. This results in a very high code density, because short instructions are used and every instruction is calculated within another part of the program. This architecture, however, requires careful distribution of the individual processing loads. The programmer's challenge is to make sure that every single unit is busy anytime. Since every unit has its own private memory, communications mechanisms are needed between the memories.

CLIW

Carmel combines MIMD (Multiple Instruction Multiple Data) with VLIW (Very Long Instruction Word) into CLIW (Configurable Long Instruction Word). Like any DSP, Carmel is able to use short, as well as long, instructions: 24 bit, 2- by 24-bit superscalar, and 48-bit single extended format for complex address modes (e.g., for long immediate data, or when several address pointers need complex modification).

In addition, Carmel's CLIW architecture is able to work with supplemental, highly dedicated instructions, which are 96-bits long. This results in a maximum code length of 48 bits + 96 bits = 144 bits. CLIW instructions are executed in parallel to the "standard" DSP instructions. Furthermore, there is a 10-bit field specifying the direct address of the 96-bit extension within the CLIW memory. Inside the 48-bit instruction, 10 bits are reserved for this microcode address, resulting in a maximum of 2^{10} = 1024 CLIW memory positions. A CLIW extension may be used at any clock cycle.

Included within the 48 bits are the direct address pointers which are to be manipulated. If a microprogram will be used multiple times, but works with different addresses, these address modifiers are included in the 48-bit instruction, where an address space of eight Mwords is available. The CLIW memory may then be kept quite small, because all of this code may be reused. For example, in a designer's daily work, say a FFT (fast Fourier transform) program is called 10 times during a program run. The program only needs to be stored in the CLIW memory once. The total program size for the complete FFT program is in the range of 20 words. The CLIW memory space of

1000 words will probably even be sufficient for bigger applications. Nevertheless, code density may be kept quite high. Most instructions which need to be stored in a chip-space, consuming memory, are short instructions (24 or 48 bits, but no CLIW instructions with an overall length of 144 bits). This results in a compact code size.

An eight-stage pipeline is the basis for this architecture. Running through the pipeline, the bits that indicate a CLIW instruction are decoded at an early stage to allow the selection, assignment, and reading of the individual, 96-bit CLIW word. This ensures that the required 96-bit code is available when the rest of the instruction (the first 48 bits) is ready to be executed. Both the 48- and 96-bit instructions are then executed in parallel. Imagine a program consisting of just 24-bit instructions. At any position within the program, a 144-bit instruction suddenly appears. To process this CLIW instruction, no mode switching is required. The user is able to individually decide (for every single clock cycle) whether to use a short or long instruction.

This feature requires separate chip space, because all CLIW instructions are executed in a separate execution unit, and CLIW instructions are fetched from a special CLIW memory. "The area demand of the CLIW execution unit is very small," explains Rueckriem. Compared with the total memory size of today's common applications, the CLIW program memory is also quite small.

Whenever the CLIW functionality is not used, it is powered down by disabling the clock. Because it is a 100% static logic design, there will be a leakage current only when the block is switched off. The entire Carmel core is a static design, which means that the system clock may be decreased down to zero. Only D flip-flops (and no transmission gates) are used, allowing very flexible handling of the clock frequency. For example, to further decrease power consumption, the designer can clock the core with any frequency lower than 120 MHz (as long as the performance requirements can still be met). In applications where high, as well as low, computing power is needed, it's possible to dynamically switch Carmel between different clock speeds.

Carmel does not offer a set of registers, as done in classic processor designs. Source operands may be immediate data, four different words from the memory, a numerical value from the address unit or program control unit, or a result from one of the six accumulators. Added up, there is a maximum of four (not six) memory-access functions in a single clock cycle (e.g., four read functions, or two read and two write functions). These four memory-access functions do not have the same address. Thanks to four independent address generation units, it's possible to read or write at four independent positions within the memory. This allows memory-to-memory arithmetic where the operands are fetched from the memory, combined and/or calculated, and written back to the memory.

Carmel uses two independent data memories: Memory A and Memory B. These data memories allow two simul-

SPECIFICATIONS

INPUT
90-132 VAC or 180-264 VAC, 47-63 Hz. Strappable. 40-60 VDC for DM Series.

EMISSIONS
FCC 20780 Part 15/EN 55022, Class A Conducted.
EN 61000-3-3, Voltage Fluctuations.

IMMUNITY
IEC 1000-4-2/EN 61000-4-2, Electrostatic Disc
1000-4-3/EN 61000-4-3, Radiated Field
4-4, Electrical Fast Transients /E
Level 3 Surge. IEC 10

INPUT SUP
34 a

REVERSE VOLTAGE PROT
All outputs are prot

OVERL

LI
±0.
max

MINIM
Main o
auxiliar
mains up

RIPPLE &
1% or 100 r

OPERATING
0-70°C. Derat

COOLING
A min. of 6 LFS*
directed over the
rated for max. temp
factory.
*Linear feet/second.

TEMPERATURE COE
±0.02%/°C.

DYNAMIC RESPONSE
Peak transient less than ±
from 75% to 50% or 100%

RECOVERY TIME
Recovery within 1%. Main outp
outputs - 500 microseconds.

SAFETY
Units meet UL 1950, CSA 22.2 No

ISOLATION
Conforms to safety agency standard

INPUT UNDERVOLTAGE
Protects against damage for undervolta

SOFT START
Units have soft start feature to protect criti

OVERVOLTAGE PROTECTION
Standard on all outputs. VX Series - standard

Deltron inc. 2S
PHI
E-MA

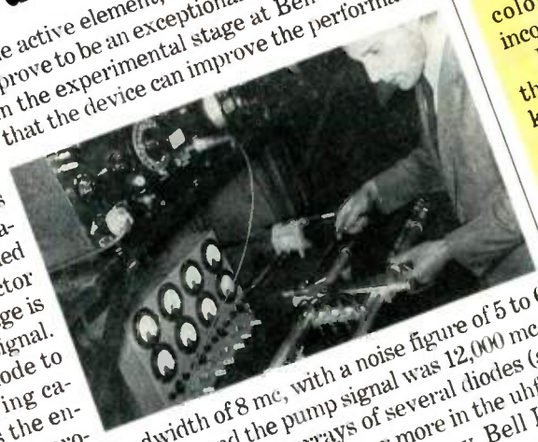
98703C

TECH INSIGHTS/QUICKLOOK

40 YEARS AGO IN ELECTRONIC DESIGN

Low-Noise Microwave Amplifier

Using a semiconductor diode as the active element, a variable reactance amplifier now under development may prove to be an exceptional low-noise uhf and microwave device. Although still in the experimental stage at Bell Telephone Labs, preliminary results indicate that the device can improve the performance of many types of microwave receivers. Variable reactance is provided by the diode, whose capacitance varies with the applied voltage. As with other varactor amplifiers, the applied voltage is derived from an hf pump signal. This signal causes the diode to function as a time-varying capacitance, and supplies the energy which is necessary to produce amplification. At 6000 mc, a bandwidth of 8 mc, with a noise figure of 5 to 6 db, has been obtained. The gain was 18 db, and the pump signal was 12,000 mc.



A traveling-wave amplifier configuration using arrays of several diodes (*see the photo*) shows promise of providing bandwidths of 25% or more in the uhf region. Using four stages with the special diodes in such an array, Bell Labs demonstrated a bandwidth of 100 mc at a 400 mc signal frequency, with a pump frequency of 900 mc and a pump power of 10 mw. This experimental amplifier has a gain of 10 db and a noise figure of only 3.5 db. (*ELECTRONIC DESIGN, July 23, 1958, p. 5*)

Variable-reactance, or parametric, amplifiers were interesting devices that offered low-noise figures, but they were somewhat unwieldy and did not make it into broad mainstream applications.—Steve Scrupski

Ultraminiature Device Integrates Entire Circuit in Single Unit

Development of an experimental shift register transistor, 1/2 in. long and 0.004 in. thick, may herald another significant breakthrough in ultraminiaturization of integrated electronic devices. This unit is expected to perform application functions of circuits which presently require twenty transistors, forty resistors, and twenty capacitors. Laboratory operation of the shift register transistor indicates the feasibility of integrating both active and passive elements. Ten transistor-like elements on a single strip of germanium function as separate two-way switches connected in a series. Each of these elements can receive and hold a single bit of information in the form of a strong or weak current corresponding to 0 or 1. Storage of 10-digit numbers is possible.

The bits of information are fed into the device one by one at high speed and at one end, and are shifted from one element to the next, in order, by shift pulses. When these pulses are stopped, each bit of information will remain in one of the transistor-like elements. When the pulses are restarted, each bit shifts from one element to the next, until the pulses are again stopped. When the bits reach the final element, they are read out in the same order in which they were fed in at the start. Development of the shift register transistor is being carried on at RCA Laboratories, Princeton, N.J. (*ELECTRONIC DESIGN, July 23, 1958, p. 12*)

This really is an interesting item—several "transistor-like elements" on a chip—and appears to be the first mention of an elementary monolithic IC in ELECTRONIC DESIGN (or at least the first that I've seen while poring through these old issues). It was around this time—July, 1958—that Texas Instruments' Jack Kilby began work on an IC that included resistive and capacitive components. The electronics industry was about to take a quantum leap forward.—Steve Scrupski

Steve Scrupski is a former Editor-in-Chief of ELECTRONIC DESIGN. Now semi-retired, he can be reached at scrupski@worldnet.att.net.

Barbie Snapshots

Now Barbie even takes pictures—as if she didn't do enough already. VISION Ltd., Edinburgh, Scotland, and Mattel Inc., El Segundo, Calif., have united to develop a new line of electronic toy cameras. The first product planned for release is a full-color toy camera that will be incorporated into Barbie products. Mattel is the current leader in the design, manufacture, and marketing of children's toys worldwide, and is producing the Barbie line. VISION is responsible for devis
and producing the optical an
electronic parts of the toy ca
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Lisa Calabres

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M Series
Moduflex® Power Supplies

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- 250 - 1500 Watts
- 1 - 7 Outputs
- AC and DC Inputs
- Competitive Prices

Deltron inc.
POWER PRODUCTS

M ■ DM ■ VX SERIES MODUFLEX® SWITCHERS

DESCRIPTION

Moduflex® Series form a comprehensive line of open frame power supplies assembled from standard "off the shelf" modules. The design features "State of the Art" topology, a meticulous thermal structure and the use of high efficiency circuits and components to attain the desired power density. The modular system concept reduces manufacturing to submodule assembly, capable of high volume production with a superior quality level at moderate costs.

M Series are available in output power ratings from 250-750 watts. **DM Series** are available with a 48VDC input and output power ratings of 400 and 600 watts. **VX Series** units consist of four specialty units with output power ratings of 500, 750, 1000 and 1500 watts having the VXI standard voltages and currents.

Three classes of output modules are available. The **STANDARD** outputs allow short duration surge currents on all auxiliaries for hard starting loads. Optional **CURRENT LIMITED** outputs have square current limiting and feature wireless droop current sharing. Optional **ENHANCED** outputs have square current limiting, one wire star point current share, output good logic signal with LED, nominal 5V local bias, individual inhibit and margining. For requirements that cannot provide minimum load on the main output, the **ZERO PRELOAD** option is available for main outputs up to 500 watts.

DELIVERY

Choose stocked units or construct a model number using stocked modules for fast delivery. Otherwise, form a model from the adjacent page to meet your specific requirements. Contact factory for deliveries on models derived from non-stocked modules.

FEATURES

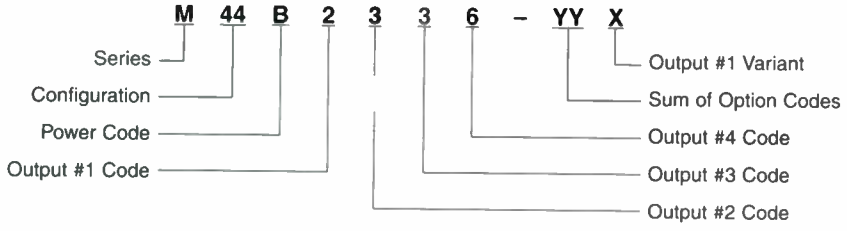
- UL, CSA, TÜV (IEC, EN), CE.
- 6 watts per cubic inch.
- 1-7 outputs, 250-1500 watts.
- AC & DC input models.
- VXI rated specialty models.
- 120 kilohertz MOSFET design.
- All outputs:
  - *Adjustable*
  - *Fully regulated*
  - *Floating*
  - *Overload and short circuit protected*
  - *Overvoltage protected*
- Standard features include:
  - *System inhibit*
  - *Load proportional DC fan output*
- Options include:
  - *Auto ranger*
  - *VME/VXI Monitor*
  - *End fan cover*
  - *Top fan cover*
  - *Current Limited Outputs*
  - *Enhanced Outputs*
  - *Zero Preload*
- Fast delivery.
- Replaces expensive high density systems using potted modules.

STOCKED MODELS - Available in 3 days.

Max Power	Output 1	Output 2	Output 3	Output 4	Model*
425W	5V @ 50A	12V @ 12A	5V @ 10A	12V @ 6A	M44R2323-47P
425W	5V @ 50A	24V @ 6A	12V @ 6A	12V @ 6A	M44R2633-47P
600W	5V @ 60A	12V @ 12A	12V @ 12A	5V @ 10A	M46C2332-47P
600W	5V @ 60A	12V @ 12A	24V @ 6A	12V @ 6A	M46C2363-47P

**Models shown in table include power fail monitor, auto ranger, current limited modules, zero preload and end fan cover options. 600W models Case #3.*

UNITS FROM STOCKED MODULES - Available in 2 weeks.



Configuration: Allowable quad output configurations are 42, 44, 46 and 48.
Power Code: Choose Power Code P, R, A through D for 250-750W models.
Output Codes: Select any outputs from the shaded area on the Output Types table consistent with the configuration chosen.
Option Code: Specify Option Code. Refer to the Option table. Codes 02 (redundancy) and 16 (enhanced) are excluded from models available in 2 weeks.

OPTIONS

Option Code	Function
00	None
01	Power Fail Monitor
02	Auto Ranger
04	Current Limited
08	Zero Preload
16	Enhanced
32	End Fan Cover*
64	Top Fan Cover

*Replace the YY with the sum of the option codes. *600 & 750 watt units require Case 5.*

MODEL SELECTION

Models are available in power ratings of 250 to 1500 watts, with corresponding code letters P, R and A through D. See Power Code chart. Contact factory for 1000 and 1500 watt models.

Output modules are available in six types—J, K, L, M, N and P in nominal power outputs from 75-500 watts. Type M, N and P modules are variable power rated depending upon the unit power rating. The M, N and P Module table directly below shows the corresponding multiplier applicable to the output current ratings of the M modules and allowable power ratings for the N and P modules. For example, a 750 watt multiple will have its M type module configured to produce 120A @ 5V or 12A @ 48V. The voltage and current rating of output modules are listed in the table of output types. This table assigns an alpha-numeric code designating the nominal voltage rating of the module.

Power Code	Unit Power Rating	M Module Current Multipliers: Single Output	M Module Current Multipliers: Multiple Output	N/P Module* Allowable Power Ratings
P	250W	0.5	0.3	175W
R	425W	0.85	0.5	250W
A	400W	0.8	0.6	250W
B	500W	1.0	0.8	300W
C	600W	1.2	1.0	400W
D	750W	1.5	1.2	500W

**When an N or P module is used as the main output, the allowable power and the module current ratings must not be exceeded.*

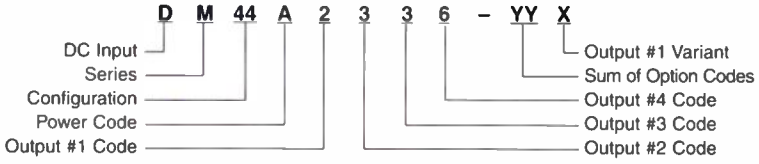
Output Types*						
Output		Module Type				
Code	Volts	J Amps	K Amps	L Amps	M Amps	N/P Amps
0	2	10	20	30	100	60
1	3.3	10	20	30	100	60
2	5	10	20	30	100	60
3	12	6	12	24	42	42
4	15	5	10	20	33	33
5	18	4	8	16	28	28
6	24	3	6	12	21	21
7	28	2.5	5	10	18	18
8	36	2	4	8	14	14
9	48	1.5	3	6	10	10
A	2.2	10	20	30	100	60
B	2.4	10	20	30	100	60
C	2.7	10	20	30	100	60
D	3	10	20	30	100	60
E	3.6	10	20	30	100	60
F	4	10	20	30	100	60
G	4.5	10	20	30	100	60
H	5.7	10	20	30	90	60
J	6.3	10	20	30	80	60
K	7	9	18	30	70	60
L	8	8	16	30	62	60
M	9	8	15	30	56	56
N	10	7	14	30	50	50
P	11	7	13	27	45	45
Q	13.5	6	11	22	37	37
R	17	5	9	18	30	30
S	19	4	8	16	26	26
T	21	4	7	14	24	24
U	23	4	7	13	22	22
V	26	3	6	12	19	19
W	29	3	5	10	17	17
X	32	2	5	9	16	16
Y	40	2	4	8	13	13
Z	44	2	4	7	12	12

*Multiple output modules of a given type are arranged in ascending order by voltage magnitude in the same sense as the output number sequence in the configuration diagrams. *Shaded ratings are stock.*

HOW TO ORDER

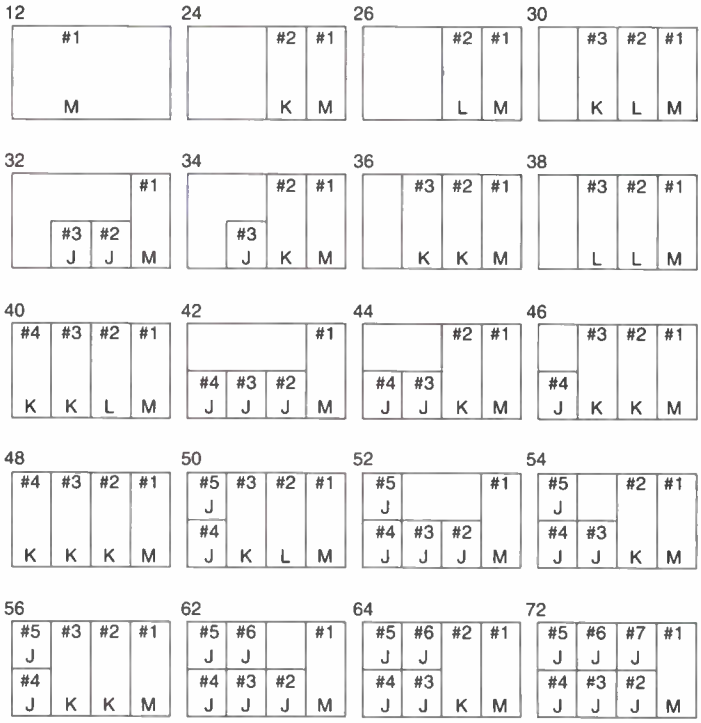
To form the proper model number defining a custom requirement, select the letters M or DM to designate the series, then choose the desired configuration of output modules and list the configuration code. Insert the power code letter for the power level and follow with the output code numbers or letters for each specific output. Enter a dash and from the option table insert the sum of the option codes. Where lower power is desired for the main module, an N module can be substituted and is denoted by a letter N in the output variant position. In addition, when no preload is available for the main output, choose Option Code 08 and add a P in the output variant position. For an **enhanced** main and **current limited** auxiliaries, specify both 04 and 16 option codes.

MODUFLEX 400W QUAD SWITCHER



OUTPUT CONFIGURATIONS

The boxes below are diagrammatic representations of the power supplies as viewed from the output end. The two-digit numbers above the boxes are the configuration codes.



Refer to the table below for allowable configurations by series.

Output Configuration	Unit Power Rating: 250W	400W	425W	500W	600W	750W
12	x	• x	x	x	• x	x
24	x	• x	x	x	• x	x
26					• x	x
30					• x	x
32	x	• x	x	x	• x	x
34	x	• x	x	x	• x	x
36		• x	x	x	• x	x
38					• x	x
40						x
42	x	• x	x	x	• x	x
44		• x	x	x	• x	x
46		• x		x	• x	x
48		• x			• x	x
50						x
52		• x	x	x	• x	x
54		• x		x	• x	x
56		• x			• x	x
62		• x		x	• x	x
64		• x			• x	x
72		• x			• x	x

• Represents allowable configurations for the DM Series.
x Represents allowable configurations for the M Series.

SPECIFICATIONS

INPUT
90-132 VAC or 180-264 VAC, 47-63 Hz. Strappable. 40-60 VDC for DM Series.

EMISSIONS
FCC 20780 Part 15/EN 55022, Class A Conducted.
EN 61000-3-3, Voltage Fluctuations.

IMMUNITY
IEC 1000-4-2/EN 61000-4-2, Electrostatic Discharge. IEC 1000-4-3/EN 61000-4-3, Radiated Field. IEC 1000-4-4/EN 61000-4-4, Electrical Fast Transients. IEC 1000-4-5/EN 61000-4-5, Level 3 Surge. IEC 1000-4-6/EN 61000-4-6, Conducted Field.

INPUT SURGE
34 amps peak from cold start for units under 400 watts, 68 amps for other models.

EFFICIENCY
75% typical.

HOLDUP TIME
20 milliseconds after loss of nominal AC power. 3 milliseconds for DM Series.

OUTPUTS
See model selection table. Outputs are trim adjustable ±5%.

OUTPUT POLARITY
All outputs are floating from chassis and each other and can be referenced to each other or ground as required.

LINE REGULATION
Less than ±0.1% or ±5mV for input changes from nominal to min. or max. rated values.

LOAD REGULATION
±0.2% or ±10mV for load changes from 50% to 0% or 100% of max. rated values.

MINIMUM LOAD
Main output requires a 10% minimum load for full output from auxiliaries. Use Option 08 if no minimum load is available for mains up to 500 watts. Singles require no minimum load.

RIPPLE & NOISE
1% or 100 mV, pk.-pk., 20 MHz bandwidth.

OPERATING TEMPERATURE
0-70°C. Derate 2.5%/°C above 50°C.

COOLING
A min. of 6 LFS* for models under 400 watts, 10 LFS for others, directed over the unit for full rating. Two test locations on chassis rated for max. temperature of 90°C. For convection ratings consult factory.
*Linear feet/second.

TEMPERATURE COEFFICIENT
±0.02%/°C.

DYNAMIC RESPONSE
Peak transient less than ±2% or ±200 mV for step load change from 75% to 50% or 100% max. ratings.

RECOVERY TIME
Recovery within 1%. Main output - 200 microseconds. Auxiliary outputs - 500 microseconds.

SAFETY
Units meet UL 1950, CSA 22.2 No. 950, EN 60 950, IEC 950.

ISOLATION
Conforms to safety agency standards.

INPUT UNDERVOLTAGE
Protects against damage for undervoltage operation.

SOFT START
Units have soft start feature to protect critical components.

OVERVOLTAGE PROTECTION
Standard on all outputs. VX Series - standard on main output.

REVERSE VOLTAGE PROTECTION
All outputs are protected up to load ratings.

OVERLOAD & SHORT CIRCUIT
Outputs protected by duty cycle current foldback circuit with automatic recovery. Standard auxiliaries have additional backup fuse protection. Options 04 and 16 have square current limiting with automatic recovery when overload is removed.

THERMAL SHUTDOWN
Circuit cuts off supply in case of local over temperature. Units reset automatically when temperature returns to normal.

FAN OUTPUT
Nominal 12 VDC @ 12 watts maximum.

INHIBIT
TTL compatible system inhibit provided. Option 16 has individual output inhibit.

REMOTE SENSING
On all outputs except standard and 04 Option outputs 75 watts or less.

SHOCK & VIBRATION
Shock per MIL-STD 810-E Method 516.4, Procedure I. Vibration per MIL-STD 810-E Method 514.4, Category 1, Procedure I.

MECHANICAL

CASE	WATTS	H	x	W	x	L	
1	250W/425W	2.50"	x	4.15"	x	8.00"	
2	400W/500W	2.50"	x	5.05"	x	9.00"	
3	600W/750W	2.50"	x	5.20"	x	9.63"	
4	600W/750W	2.50"	x	6.50"	x	9.63"	Config. 40 & 50 only.
5	600W/750W	2.50"	x	6.00"	x	9.63"	Option 32 only.
6	1000W	5.00"	x	5.05"	x	10.40"	
7	1500W	5.00"	x	5.20"	x	11.00"	

OPTIONS

POWER FAIL MONITOR
Optional circuit provides isolated TTL and VME/VXI compatible ACFAIL signal providing 4 milliseconds warning before main output drops by 5% after an input failure. A SYSRESET signal following VME timing requirements is provided when an N module is used as a main output. Both logic signal outputs can sink current per the VME specification.

AUTO RANGER
Optional circuit provides automatic operation at specified input ranges without strapping. Not applicable to DM Series.

CURRENT LIMIT
Option provides on all outputs:
- Square current limit with auto recovery.
- Wireless droop current share for parallel or N+1 redundant operation.

ZERO PRELOAD
Optional circuit removes need for preload on main output. Available for mains up to 500 watts.

ENHANCED
Option provides on all outputs:
- Square current limit with auto recovery.
- Single wire active current share for parallel or N+1 redundant operation.
- DC output good logic signal with LED indicator.
- Logic inhibit.
- Nominal 5V bias.
- Margining.

END FAN COVER
Optional cover with brushless DC ball bearing end fan which provides the required air flow for full rating.

TOP FAN COVER
Same as above with fan mounted on top of the power supply.

Specifications subject to change without notice.

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words will probably even be sufficient for bigger applications. Nevertheless, code density may be kept quite high. Most instructions which need to be stored in a chip-space, consuming memory, are short instructions (24 or 48 bits, but no CLIW instructions with an overall length of 144 bits). This results in a compact code size.

An eight-stage pipeline is the basis for this architecture. Running through the pipeline, the bits that indicate a CLIW instruction are decoded at an early stage to allow the selection, assignment, and reading of the individual, 96-bit CLIW word. This ensures that the required 96-bit code is available when the rest of the instruction (the first 48 bits) is ready to be executed. Both the 48- and 96-bit instructions are then executed in parallel. Imagine a program consisting of just 24-bit instructions. At any position within the program, a 144-bit instruction suddenly appears. To process this CLIW instruction, no mode switching is required. The user is able to individually decide (for every single clock cycle) whether to use a short or long instruction.

This feature requires separate chip space, because all CLIW instructions are executed in a separate execution unit, and CLIW instructions are fetched from a special CLIW memory. "The area demand of the CLIW execution unit is very small," explains Rueckriem. Compared with the total memory size of today's common applications, the CLIW program memory is also quite small.

Whenever the CLIW functionality is not used, it is powered down by disabling the clock. Because it is a 100% static logic design, there will be a leakage current only when the block is switched off. The entire Carmel core is a static design, which means that the system clock may be decreased down to zero. Only D flip-flops (and no transmission gates) are used, allowing very flexible handling of the clock frequency. For example, to further decrease power consumption, the designer can clock the core with any frequency lower than 120 MHz (as long as the performance requirements can still be met). In applications where high, as well as low, computing power is needed, it's possible to dynamically switch Carmel between different clock speeds.

Carmel does not offer a set of registers, as done in classic processor designs. Source operands may be immediate data, four different words from the memory, a numerical value from the address unit or program control unit, or a result from one of the six accumulators. Added up, there is a maximum of four (not six) memory-access functions in a single clock cycle (e.g., four read functions, or two read and two write functions). These four memory-access functions do not have the same address. Thanks to four independent address generation units, it's possible to read or write at four independent positions within the memory. This allows memory-to-memory arithmetic where the operands are fetched from the memory, combined and/or calculated, and written back to the memory.

Carmel uses two independent data memories: Memory A and Memory B. These data memories allow two simul-

taneous memory-access operations *(see the figure)*. If these memories are implemented as dual-port memories, four (2×2) memory-access operations can be handled simultaneously. This means that data bus A and data bus B are both existing twice. Furthermore, the memories need to be distributed onto separate banks, and the software needs to keep track of this.

CLIW and program memory can be implemented as RAM or ROM. The interface to the flexible peripheral interface (FPI) bus—a Siemens proprietary 32-bit bus—is used for communication with the outside world. This bus may also be available off-chip, as it runs at half the clock frequency (60 MHz when Carmel is clocked at 120 MHz). At 60 MHz, this 32-bit bus achieves a bandwidth of 240 MByte/s.

The DSP/Microcontroller interface can establish a connection to another, or several additional, masters without any glue logic, because the system is able to work with multiple masters. Embedded DRAM may also be implemented.

Benchmarks

Mathematically, a finite-impulse-response (FIR) filter is a sum of products. With its two MAC units, Carmel calculates two FIR filter taps within a single cycle, yielding a theoretical execution time of one-half clock cycle per tap.

With more-complex algorithms, Carmel shows its real strengths when functions need to be calculated in an inner loop. Quite often, complex memory-access functions with complex address modes and several add/multiply functions are executed within these inner loops. For example, an FFT is split into so-called butterflies (symmetric operations, where a complex multiplication with a twiddle factor is performed in combination with a complex command difference). Carmel is able to calculate such a butterfly function within two clock cycles. A Viterbi decoder requires 22 clock cycles, while a Viterbi equalizer requires 28 clock cycles. "These benchmarks show that our architecture is up to two times more efficient for complex inner loops than any other solution," says Rueckriem.

In terms of performance efficiency, Carmel needs about 7 M-MIPS to implement a GSM half-rate speech encoder. This means that in a base station for micro cells, 13 channels can be handled by a single Carmel core running at 2.0 V and 100 MHz.

In the mobile phone market (for example, with GSM cellular phones), the microcontroller code is stored in an external flash memory to enable updates, protocol extensions, etc. The signal-processing code, however, is stored on the DSP system chip. Therefore, not only is the core size itself of vital interest, but also the code density, because the code density determines the size of the signal-processing program memory. For example, in a currently available GSM mobile-phone IC, the ROM size is bigger than the entire DSP core. This combination of core size and code density was also a major focus during Carmel's design phase.

Power Consumption

Designed in 0.25-µm CMOS, Carmel will offer 120 M-MIPS at a supply voltage of 2.5 V. Operating with 2.0 V, it will still offer 100 M-MIPS.

At 2.0-V supply voltage, Carmel's power consumption is specified to be in the range of 1 mW/M-MIPS. At 2.5 V, the power consumption is about 1.5 mW/MHz. As a result, the Carmel core's maximum power consumption is 180 mW at the maximum frequency of 120 MHz. The entire power management for the core, memories and peripherals is designed to operate at supply voltages below 1.5 V, which is a feature of the process technology.

Of course, all this data only addresses the core. Power consumption of peripherals, memories, etc., still needs to be considered. But, compared to a board solution, a system-on-a-chip offers other advantages than just saving space. Due to capacitive loads of leads, vias, and connections, boards often consume a higher percentage of their total power consumption in the I/O area.

Roadmap

Siemens Semiconductors is considering creating a so-called "Tiny Carmel," with just a single MAC (instead of two) and two simultaneous memory accesses instead of four. According to Rueckriem, such a Tiny Carmel, with half the memory bandwidth, would require about half the chip area of a full-size Carmel. As mentioned previously, the CLIW functionality only accounts for a small area of board space. Furthermore, Siemens is thinking about implementing a 24-bit Carmel for high-end applications, mainly in the audio area.

"The DSP industry proved that the quality of tools will never be extremely good when tools are designed in-house only, and nobody will be able to afford additional tools from a second tool vendor," claims Rueckriem. To increase tool quality, Siemens decided to license its Carmel core to third parties. The reason for this is that the company intends to establish a DSP core standard and a widely supported user base. Siemens also wants to gain a major share in the embedded DSP market.

A licensee using the Carmel core implements a design within a normal semicustom design flow. If the licensee designs in the proper manner, the chip manufacturer cannot determine the functionality of the design, as reverse engineering is not possible anymore. A full-scan design allows automatic generation of test vectors, offering almost 100% test coverage of functionality. The silicon manufacturer only receives these test vectors. All functional test vectors remain within the design department. Thus, a system house, without close ties to a semiconductor manufacturer, can get an ASIC made at any foundry—without the risk of distributing company confidential know-how.

Assemblers/linkers, simulators, and C-compilers will be available from Siemens. For their next step (and level), they are planning to offer very fast C models for hardware-software co-simulation. A further step will be real hardware-software codesign, with automatic generation of code and structures.

Sorry, Californians—the name Carmel derives from a hill in Israel. The architecture was designed by a Siemens joint venture named IC.COM in Israel, in cooperation with Professor Fettweis, Technische Universitaet, Dresden, Germany. Siemens Semiconductors owns all the rights on Carmel and is open to licensing its core. The first license has already been given to LSI Logic, Milpitas, Calif.

Price And Availability

First silicon for the Carmel DSP core and dedicated design tools will be available in the third quarter of 1998. The company may be reached for pricing information.

Contact Dr. Reinhard Rueckriem, Munich, Germany at +49 89 636 837 01; fax: +49 89 636 817 82, e-mail: Reinhard.Rueckriem@hl.siemens.de. Or check Siemens' web page at www.siemens.de/semiconductor. **CIRCLE 519**

ELECTRONIC DESIGN
QUICK LOOK
Edited by Debra Schiff and Nancy Konish

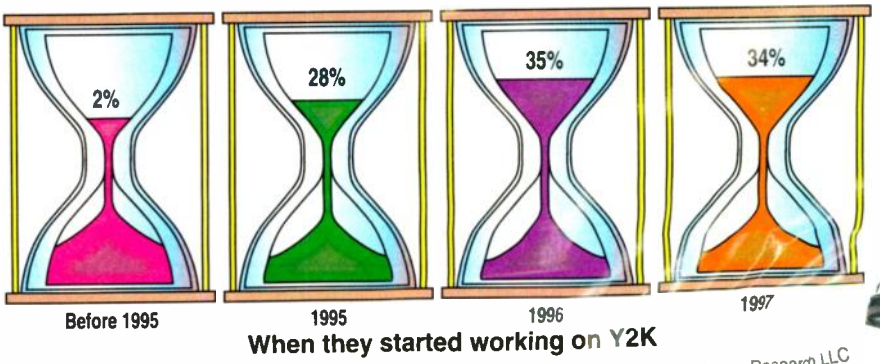
MARKET FACTS

The Big Names Just Aren't Moving On Y2K

As we've been saying in our "Y2K Update" column, come the turn of the century, many systems will fail unless they're repaired to accept date fields containing 00 as 2000, rather than 1900. Of course, that's a simplistic view of the situation that has already yielded more than a handful of liability lawsuits, but thanks to the mass media, Y2K has become a household word. But, what's really surprising is that, according to a recent study by Triaxsys Research LLC, in it's Research Reports, of the 250 largest companies in the U.S., 60% have yet to complete the first phase (assessment) of their Y2K compliance efforts. The companies were chosen by Triaxsys according to their revenue rankings in the U.S. Securities and Exchange Commission's EDGAR database. The study found that the majority of these companies headed into their Y2K compliance process late, and have made little progress in the direction of conversion. And, as predicted a few years ago by nearly every analyst with a calculator, Y2K expenditures are going to empty some deep pockets. These 250 companies will spend at least $33 billion total to get their year 2000 date change matters in order. Only 20% of that sum has been spent so far. When the firms told Triaxsys about their risk potential, 45% said that they *might* suffer adverse material impacts if their Y2K efforts are not completed by the time we're all flipping our calendars to January 2000. Those material impacts are the forces that will cause those heavily invested in Fortune 250 companies to pressure the corporate managers to get on the ball with their Y2K compliance efforts. What's stymied the IT analysts and investors is that their assumptions that the largest U.S. companies have had their Y2K projects well in hand, have been totally off the mark. As of December 1997, almost half of the companies surveyed didn't even disclose their Y2K program status. Those who did decide to furnish their Y2K information told a scary tale of what investors can expect in the coming years. Most (58%) are in the assessment phase of their Y2K compliance projects—internal systems only. About one-third (36%) s: that they are currently converting some of their syst and a paltry 6% are in the testing phase. By 1999 forts should be in the testing phase in order to enough time to deal with failures. As previ tioned, expenditures will be very high. The pany in the surveyed group will spend $131 dress Y2K issues. Triaxsys projects that at th companies were going at the end of last year, th range of only 7% to 45% toward completion. says that General Motors has made the least pr with estimated costs of $565 million, 7% of that figu ready spent in Y2K compliance efforts. First Chic NBD, on the other hand, has met 45% of its total es mated costs, and is projected to dish out only $100 millio more to support its work toward Y2K compliance. The crunch that the investors are really going to feel (and hear about) the most will come from the material losses expected with Y2K failures, incomplete compliance, and third-party failures. Essentially, according to Triaxsys, 80% of the work still needs to be done—meaning that companies are going to miss their conversion deadlines put untested code into production, and spawn fail and material costs—the nature of which are nightm at best.

The annual subscription rate for Triaxsys Re Reports is $995. For more information, c Research LLC at (888) 320-8882.—**DS**

SOBERING STATS



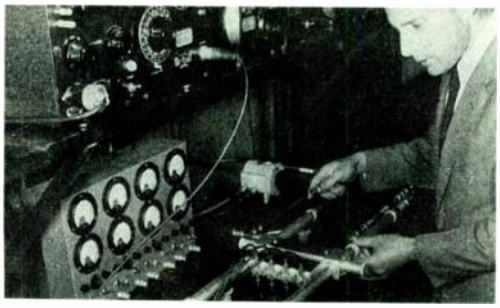
Art: L. Gravell

Source: Triaxsys Research LLC

40 YEARS AGO IN ELECTRONIC DESIGN

Low-Noise Microwave Amplifier

Using a semiconductor diode as the active element, a variable reactance amplifier now under development may prove to be an exceptional low-noise uhf and microwave device. Although still in the experimental stage at Bell Telephone Labs, preliminary results indicate that the device can improve the performance of many types of microwave receivers. Variable reactance is provided by the diode, whose capacitance varies with the applied voltage. As with other varactor amplifiers, the applied voltage is derived from an hf pump signal. This signal causes the diode to function as a time-varying capacitance, and supplies the energy which is necessary to produce amplification. At 6000 mc, a bandwidth of 8 mc, with a noise figure of 5 to 6 db, has been obtained. The gain was 18 db, and the pump signal was 12,000 mc.



A traveling-wave amplifier configuration using arrays of several diodes (*see the photo*) shows promise of providing bandwidths of 25% or more in the uhf region. Using four stages with the special diodes in such an array, Bell Labs demonstrated a bandwidth of 100 mc at a 400 mc signal frequency, with a pump frequency of 900 mc and a pump power of 10 mw. This experimental amplifier has a gain of 10 db and a noise figure of only 3.5 db. (*ELECTRONIC DESIGN, July 23, 1958, p. 5*)

Variable-reactance, or parametric, amplifiers were interesting devices that offered low-noise figures, but they were somewhat unwieldy and did not make it into broad mainstream applications.—Steve Scrupski

Miniature Device Integrates Entire Circuit in Single Unit

Development of an experimental shift register transistor, 1/2 in. long and thick, may herald another significant breakthrough in ultraminiaturized integrated electronic devices. This unit is expected to perform application functions of circuits which presently require twenty transistors, forty resistors, twenty capacitors. Laboratory operation of the shift register transistor indicates the feasibility of integrating both active and passive elements. Ten transistor-like elements on a single strip of germanium function as separate two-way stores connected in a series. Each of these elements can receive and hold a single bit of information in the form of a strong or weak current corresponding to 0 or 1. Storage of 10-digit numbers is possible.

Binary bits of information are fed into the device one by one at high speed and at the input end, and are shifted from one element to the next, in order, by shift pulses. When these pulses are stopped, each bit of information will remain in one of the transistor-like elements. When the pulses are restarted, each bit shifts from one element to the next, until the pulses are again stopped. When the bits reach the final element, they are read out in the same order in which they were fed in at the start. Development of the shift register transistor is being carried on at RCA Laboratories, Princeton, N. J. (*ELECTRONIC DESIGN, July 23, 1958, p. 12*)

This really is an interesting item—several "transistor-like elements" on a chip—and appears to be the first mention of an elementary monolithic IC in ELECTRONIC DESIGN (or at least the first that I've seen while poring through old issues). It was around this time—July, 1958—that Texas Instruments' Kilby began work on an IC that included resistive and capacitive compo- The electronics industry was about to take a quantum leap forward.—rupski

ki is a former Editor-in-Chief of ELECTRONIC DESIGN. Now n be reached at scrupski@worldnet.att.net.

Barbie Snapshots

Now Barbie even takes p tures—as if she didn't enough already. VISION L Edinburgh, Scotland, and Mat Inc., El Segundo, Calif., ha united to develop a new line of el tronic toy cameras. The first pro uct planned for release is a fu color toy camera that will b incorporated into Barbie products

Mattel is the current leader i the design, manufacture, and ma keting of children's toys worldwide and is producing the Barbie line VISION is responsible for devis and producing the optical an the electronic parts of the toy ca mera. Its most important compone nts are made using ColorMOS (CMOS), a recent image sensor techn ology.

VISION is the driving force behind the technology of CMOS-based imaging. CMOS Cameras consume a only small percentage of the power required for Charge Coupled Device (CCD) products. Since sensors used for CMOS are capable of higher levels of product integration, system costs for these cameras are also lower.

This is not the first time VISION has worked with a toy company. They worked with TYCO to produce the TYCO Kid's Videocam, a monochrome children's video camera. Mattel chose to work with VISION because of their ability to develop products, and enter volume production quickly.

Andy Rifkin, Senior VP at Mattel, said, "VISION stood out as a product developer with a clear competitive lead. Mattel has been delighted with the responsiveness and speed of VISION's product design, which is crucial to our ability to bring innovative and exciting toys to a growing market."

VISION develops and produces CMOS imaging chips and cameras for volume supply to Original Equipment Manufacturers (OEMs). Their largest market is in digital color cameras used with PCs for the videoconferencing market.

For more information, visit VISION's web site at www.vvl.co.uk.

Lisa Calabrese

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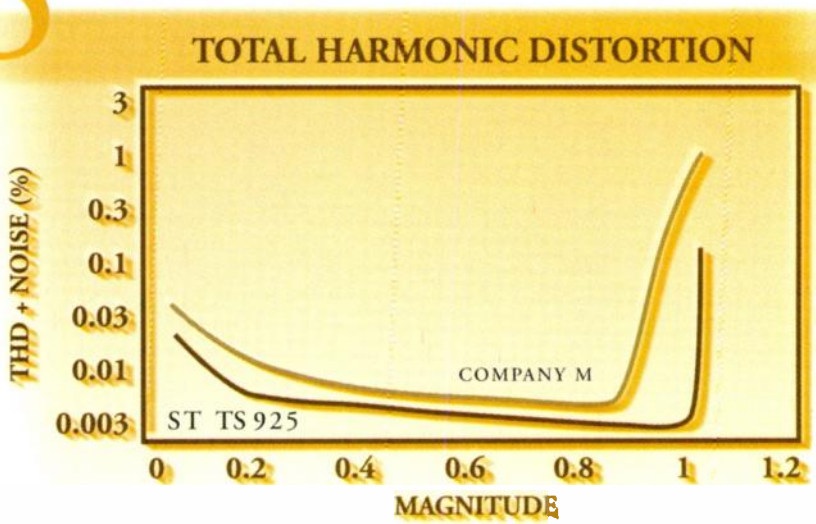

• *Curves compare THD of ST TS925 to leading competitive rail-to-rail op amp.*

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TRUDEL TO FORM

My last few columns discussed useful metrics and strategies. I suggest making innovation a competitive weapon, as business has done in the past for other competencies like quality and fast cycles. You can use innovation to gain a competitive advantage.

One of the tricky things about innovation is that it's always uncertain. Results are not assured. Machine-Age business was based on predictability. Traditional business tools are linear, deterministic, and financially-centric. They do not work well, if at all, for probabilistic phenomena.

Common financial tools like ROI (return-on-investment) analysis were designed to help guide investment in capital assets. They don't work well for today's important decisions like knowledge investments and creating the future. That's especially true for new product development (NPD). You only get to invent a new technology once; the next time it's different.

As quantum physics demanded new templates of science, so Information-Age business demands major changes in management's viewpoint and approach. My book, *Engines of Prosperity* discusses this, and cites cases and references. We predict that, when everything shakes out, finance will no longer be the center of the business solar system.

JOHN D. TRUDEL

All this raises two questions: How can engineers persuade management to shift from financially based project selection, and how can firms best decide which NPD project to pursue?

The first question is tougher to answer. We're asking for a major behavioral change on the part of those who are in power. Still, the two questions are linked. Presumably, if one can show management that they can get better business performance by a different method of NPD project selection, then some may change.

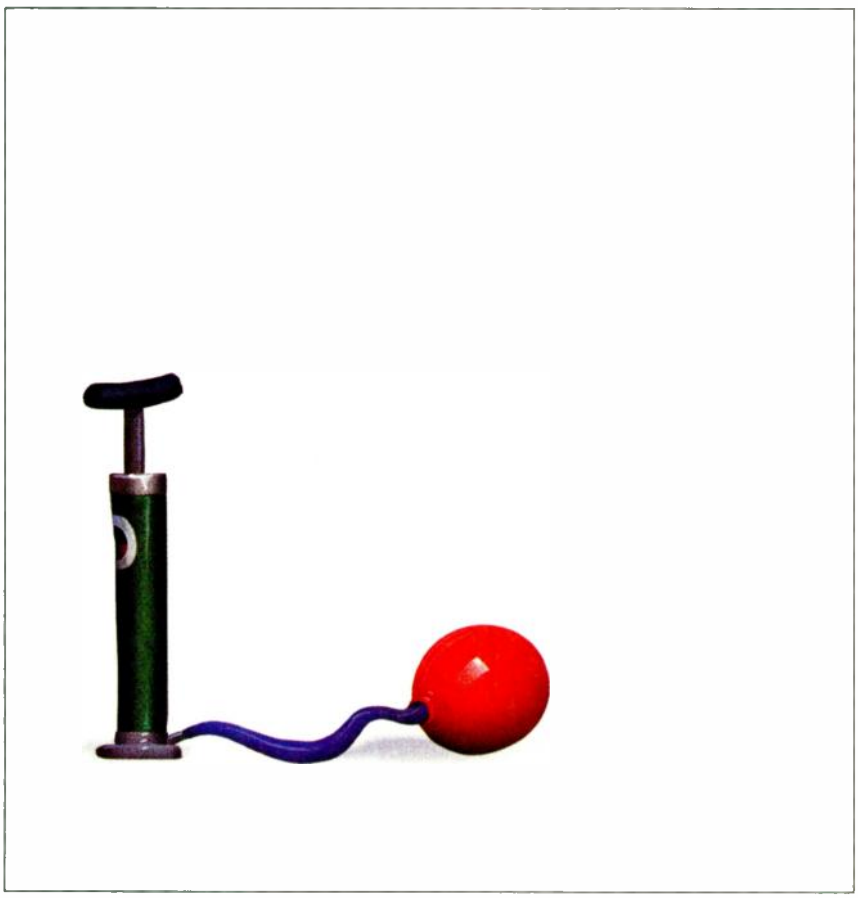
Bob Cooper, a researcher at Canada's McMaster University, is famous for making the stage-gate method of new product management popular. His book, *Portfolio Management in New Product Development* is available from Addison Wesley. Cooper's main conclusion was that "financial methods have little to commend them." He and his colleagues found that they "suffered a multitude of weaknesses, but, ironically, were the most popular."

He had three major criticisms of financial methods. First, they were "an ineffective decision tool, often leading to the wrong decisions." Second, their limitations "were not fully understood by management." Finally, they failed to deal with vital portfolio issues including balance, gridlock and timeliness, and matching the right number of projects to the resources available.

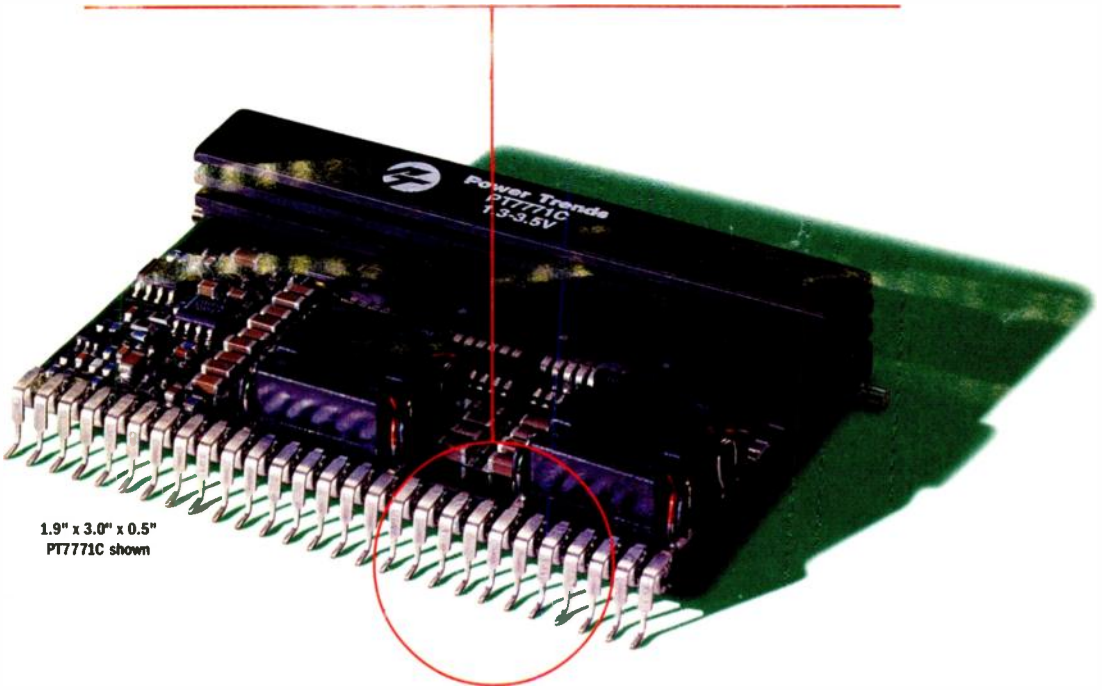
These points have been raised before, by others and myself, but Cooper's contribution is having sampled 238 firms and correlated portfolio decision methods to the high and low business performers. This is as close to proof as we'll get.

So which methods work better? It depends on what you want to accomplish. There are three main goals of portfolio management: maximizing value, balancing, linking to business strategy. A wide variety of scoring-model, bubble-chart, and strategic-planning approaches are available. The details vary, but all require top-level involvement and management buy-in.

John D. Trudel, CMC, provides business innovation consulting services to selected clients. Lectures, keynotes, and workshops also are available. He is the author of "High Tech with Low Risk" and "Engines of Prosperity." The Trudel Group, 33470 Chinook Pl., Scappoose, OR 97056; (503) 638-8644; fax (503) 543-6361; e-mail: jtrudel@gstis.net; www.trudel-group.com.



32 AMPS
SURFACE MOUNT



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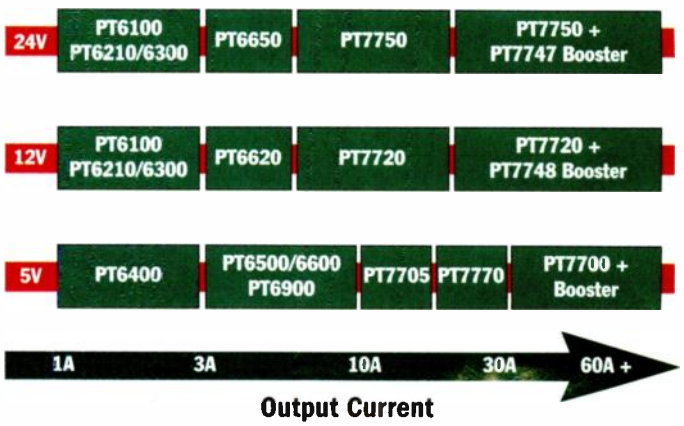


POWER TRENDS

READER SERVICE 146

MANAGING THE DESIGN FACTORY

Virtual Colocation Doesn't Exist

DON REINERTSEN

Ever since Ogg, the Cro Magnon designed the first stone wheel for Grnk, the Neanderthal, colocation has been invaluable for product development teams. Recently some observers have concluded that electronic man, as a more highly evolved species, has finally eliminated the need for colocation of team members. Who would have thought that you could give 100 teammates the pleasure of listening to 30 minutes of your insight by punching in a few simple numbers on your phone? Today, they say, we have entered the age of "virtual colocation", an age when physical proximity is no longer necessary.

Before you swallow this line, you might ask what colocation actually accomplishes for a team, and assess whether virtual colocation can do the same thing. Communications on colocated teams differs greatly from communications on other teams. Interestingly, it has to do with subtle differences in both the content of the data, and the way it is interpreted.

Colocated teams have a much higher incidence of accidental and informal communications. Here, the conversation is not 100% business-focused. Instead, conversations contain a large component of personal communications, therefore team members know each other as people, not just as gears in the development machine.

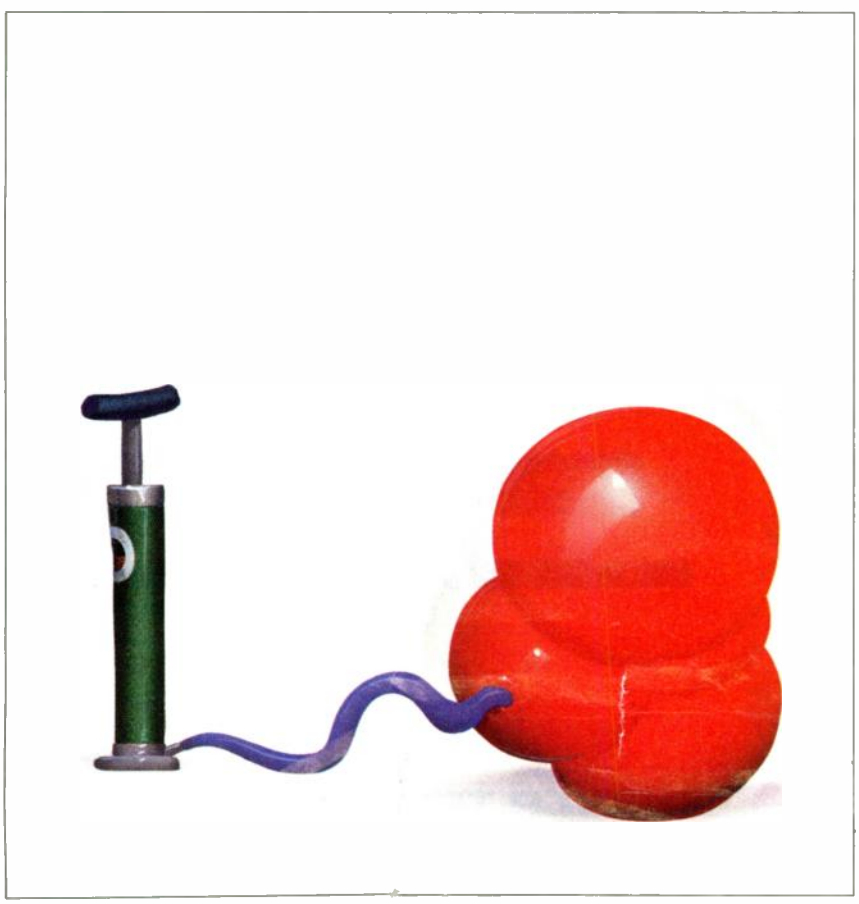
Psychologists have found that our knowledge of other people affects the way we process information that we get from them. We can more accurately interpret messages from people we know. The informal communications on colocated teams improves their ability to interpret the formal communications.

But it's not only a question interpreting information. Colocation has an important effect on how we emotionally perceive other team members. We perceive people in close proximity as members of the "in group," and those who are separated as members of the "out group". Members of the out group are viewed as simple, irrational, and monolithic. In contrast, the in group perceives itself as complex, rational, and diverse.

Importantly, the inherent distortion with which we see distant group members can cause us to misinterpret the meaning of their behavior, making inaccurate inferences about why they do things. If an engineer arrives late to a team meeting it must mean that there was a special situation with a good reason. If somebody from Finance arrives late to a team meeting it is because "they never arrives on time." Inaccurate inferences cause us to form inaccurate beliefs. The inaccurate beliefs then distort any new data.

If colocation was only about the exchange of data, it might be possible for us use technology to substitute for it. In reality, colocation is more about psychology than it is about exchanging messages. All our new-fangled communications tools are unlikely to ever substitute for colocation. The best teams will chose colocation whenever possible. They recognize that communications is one of the greatest challenges to any team, and use every tool that they can get their hands on. The tools really do improve communications; they are just not a substitute for true colocation.

Don Reinertsen is president of Reinertsen & Associates, a consulting firm specializing in product development management. He can be reached at (310) 373-5332 or e-mail: Don.Reinertsen@compuserve.com.



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Flipping Through The Internet Rolodex

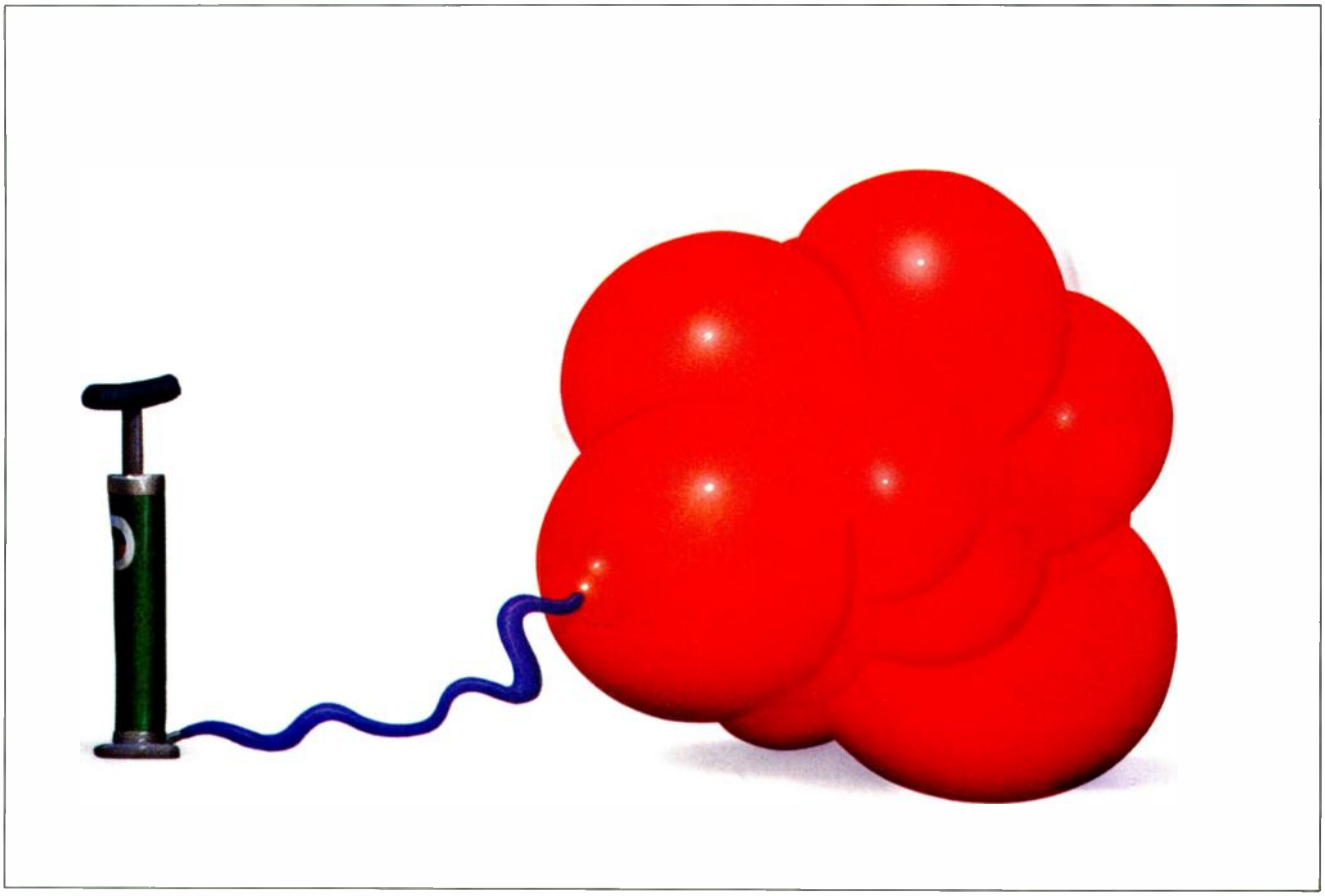
www.metricUSA: This site might just be THE metric source on the web. It certainly is the only place where engineers, consultants, and buyers can find facts and sources for metric products and services. Metric-related events are listed in the Calendar of Events, while the Metric News section features product, government, and industry news. Other resources are the Directory of Products and Services and a metric Conversion Calculator. To get into heated discussions about metric topics, visit Speak Out. The site also covers information on industrial standards, both worldwide and in the United States.

www.bofw.com: Ever gotten frustrated trying to get past the muck on the Internet, and get to some real information? Someone at Luckman Interactive Inc. obviously has, and it motivated them to create a free online directory. Best of the Web makes finding useful information on the web both quicker and easier. It contains only those sites that were rated, reviewed, and found to be four- and five-star web sites. Best of the Web lists 25,000 web sites in all, out of a total 150,000 reviewed. It includes 18 categories: Art, Business, Computers, Education, Entertainment, Family, Government, Interests, Health, Humanities, Internet, Music, News, Regions, Science, Shopping, Sports, and Travel.

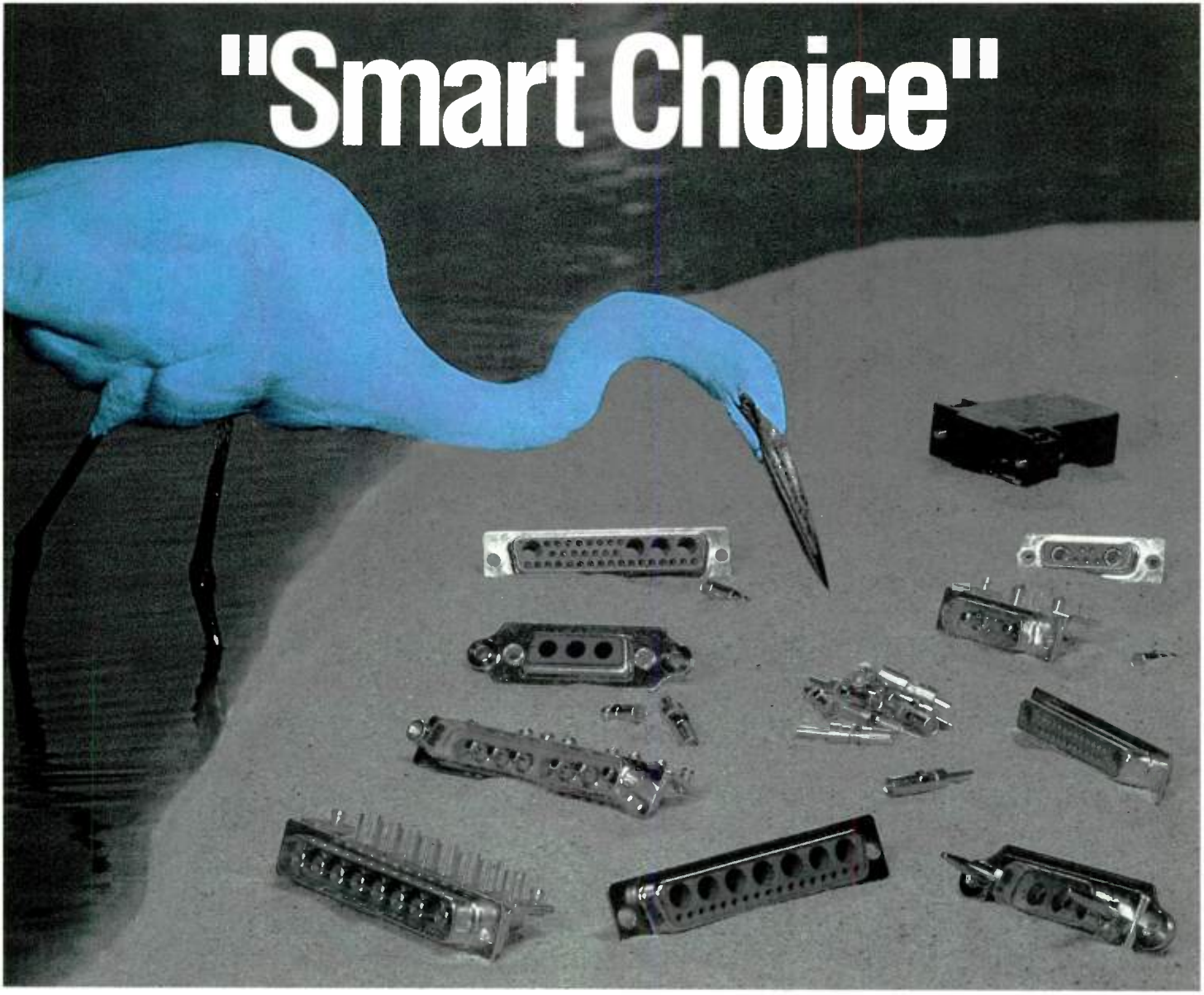
www.ericssonservice.com: If you want to see the first web site devoted to customer service, come here. Ericsson's new web site provides comprehensive product information and service solutions for those who sell and repair Ericsson mobile phones and accessories. The company hopes that the web site will improve customer service. The site also includes programming instructions and training for the mobile phones and accessories, as well as information on Ericsson's AMPS, D-AMPS, and GSM phones. Check out the bulletin boards for product and technology updates.

www.switchcraft.com: This site shows the highlights of a 336-page Engineering Design Guide. Other items of interest include a complete product cross-reference and product literature for Switchcraft's components, as well as new product, trade show, and sales information.

www.pios.com: Users of Pioneer-Standard products will be happy to discover their new, improved web site. It has a new feature which provides online pricing and information about product availability, 24 hours a day. Accessing this information is as easy as going to the web site and clicking on the Industrial Electronic Division icon. Searches can be done by part number or manufacturer. The site, established to make purchasing and forecasting easier, catalogs 110,000 industrial electronic parts.



"Smart Choice"



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JUST 4 THE KIDS

Looking for hi-tech, interactive activities that are fun and educational for your children, but aren't too expensive? You might want to try the CD-ROMs from Hasbro Interactive, Beverly, Mass., which offer family entertainment on a shoestring. Targeted at anyone three years or older, they aim to please the whole family.

For the younger child—ages three to eight—Hasbro offers three CD-ROM options: Tonka Construction, Tonka Search and Rescue, and Tonka Workshop Interactive Playset. With Tonka Construction, the child learns how to use a fleet of Tonka trucks to dig quarries, build roads, and design parks. The child also cultivates planning skills by taking control of realistic construction projects, such as City Development and Desert Road Building.

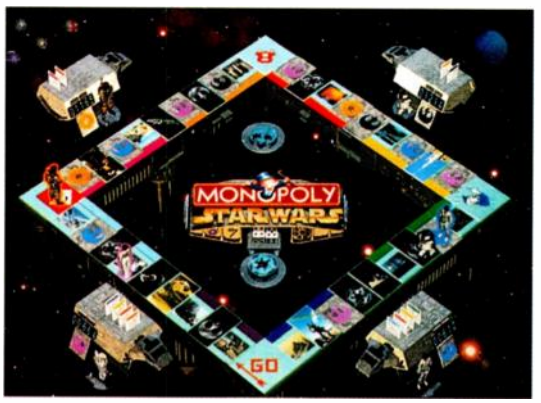
Tonka Search and Rescue lets the child play the hero. This sequel to Tonka Construction lets the child take charge of dozens of land, air, or sea rescue missions. Various CD-ROM activities teach the child about a fleet of 14 animated, 3D rescue vehicles. The Tonka Academy teaches rescue skills, such as putting out fires, maneuvering trucks, and flying helicopters. The child can also visit the Tonka Garage to learn how to maintain rescue vehicles and equipment. To make the activity really come to life, a fully integrated print center allows the child to create customized badges, certificates, and decals for the Tonka toys. Complete Tonka truck playsets can also be printed out.

The Tonka Workshop Interactive Playset merges the toy with the computer. Using the playset, the child can have hands-on fun with the PC. Guided by Tonka Joe, the child builds, explores, and constructs everything from robots, imaginative inventions, toy houses, and spaceships, using a variety of tools. Children sharpen their tool skills in the Tool Olympics activity by using tools to uncover mysteries at the Junk Shop. Once these skills are mastered, the child earns a Master Tool License, and can hop in the Tonka Workshop Van to go to real, on-site, fix-it missions.

This interactive playset fits easily over all standard Windows PC keyboards, so no additional desk space is required. The playset is also programmed to work directly with the letters and numbers on the computer keyboard. To use it, you simply snap it onto the computer keyboard.

For the older child—ages six and up—you might want to take a look at the Scrabble CD-ROM, Monopoly Star Wars Edition CD-ROM, and Star Wars Millennium Falcon Interactive Playset. The Scrabble CD-ROM allows the child to play the word game with state-of-the-art computer technology, music scores, sound effects, and high resolution, 3D graphics. It features 10 levels, ranging from beginner to expert, and a customizable dictionary. Up to four players can compete on the same game board, and family members from around the world can compete with each other by using the Internet at Microsoft's Internet Gaming Zone.

MARIFRANCES WILLIAMS



The Monopoly Star Wars Edition CD-ROM is the classic Monopoly game in the Star Wars universe. It is hosted by the original C-3PO, Anthony Daniels. The child chooses one of eight full-motion, 3D Star Wars heroes or villains. With each roll of the dice, favorite Star Wars properties are bought and sold. Movie scenes and music from the Star Wars trilogy, meanwhile, can be viewed and heard. Graphics and sound effects set the stage as players battle opponents at home or around the galaxy via the Internet. The child can play with up to six players simultaneously, in multiple languages such as French, German, Spanish, and Japanese. All transactions, including currency, happen in real time. Players buy and sell Star Wars property seamlessly.

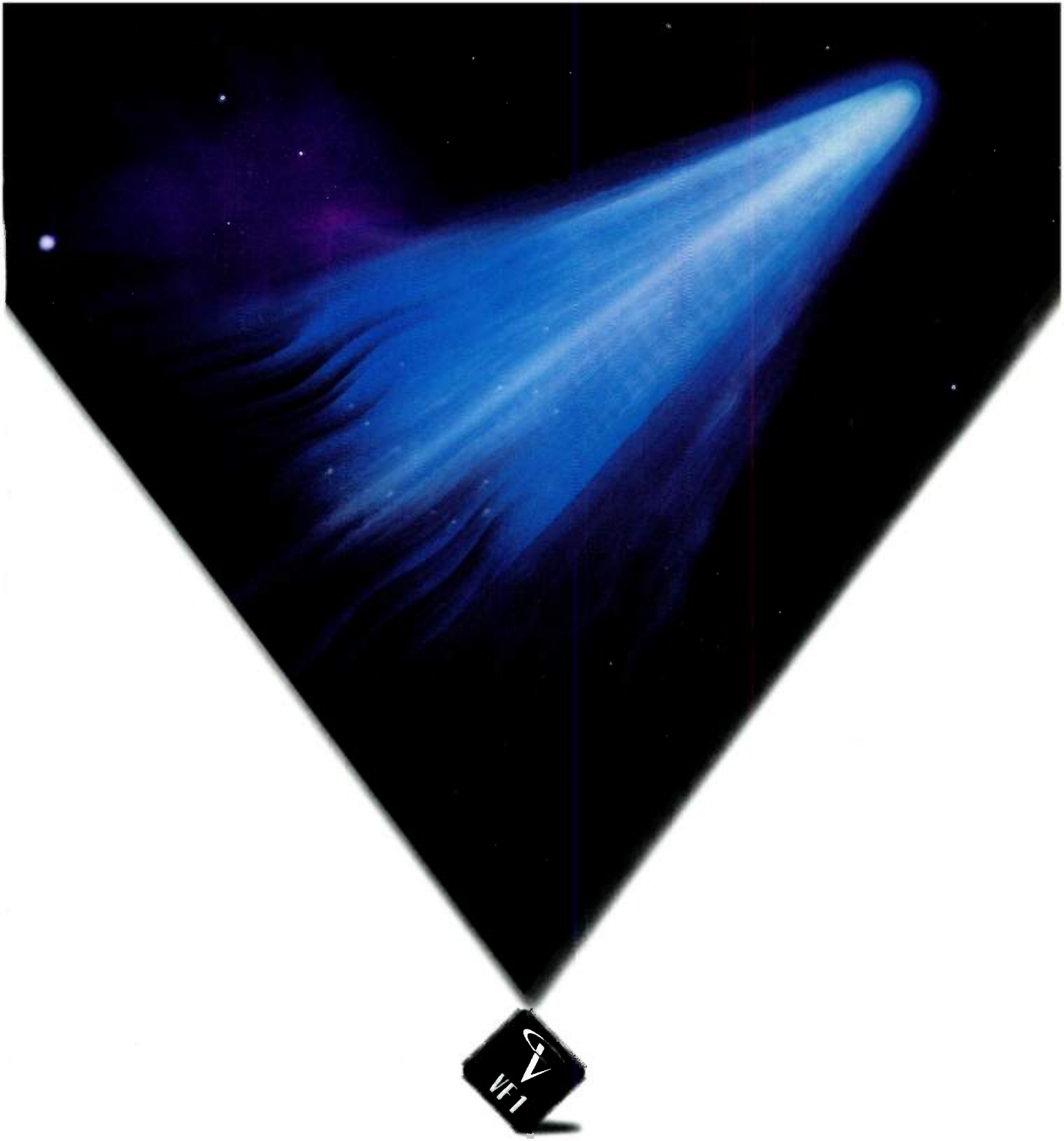
With the Star Wars Millennium Falcon Interactive Playset, the child pilots a detailed, Millennium Falcon cockpit as it explores the Star Wars universe. The child interacts with Star Wars action figures in search of the Death Star's thermal exhaust port, and receives guidance and wisdom from characters like Obi-Wan Kenobi and Yoda. The child can also relive scenes from the popular Star Wars movie trilogy, bringing Star Wars fantasy to life on the computer.

While playing with these CD-ROMs and Interactive playsets, the child develops problem-solving skills, cause-and-effect connections, sequential thinking, and construction and high-level thinking skills—all in a fun-filled atmosphere.

The Tonka Construction CD-ROM is available at retail stores and sells for $19.95. Also available are the Tonka Search and Rescue and Scrabble CD-ROMs, which sell for $29.95, and the Monopoly Star Wars Edition, which sells for $39.95. Both the Tonka Workshop Interactive Playset and Star Wars Millennium Falcon Interactive Playset will be available in the Fall and sell for $39.95.

For more information, contact Hasbro Interactive Inc., 50 Dunham Rd., Beverly, MA 01915-1844; (508) 921-3700; e-mail: www.hasbro.com.

Marifrances D. Williams holds a degree in Liberal Studies from San Diego State University, Calif. She is currently a fifth-grade teacher at Los Ranchos Elementary, San Luis Obispo, Calif. Williams specializes in the identification of advanced technology for the use of child-focused applications. She may be reached at williamsofsm@lightspeed.net.



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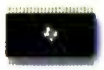

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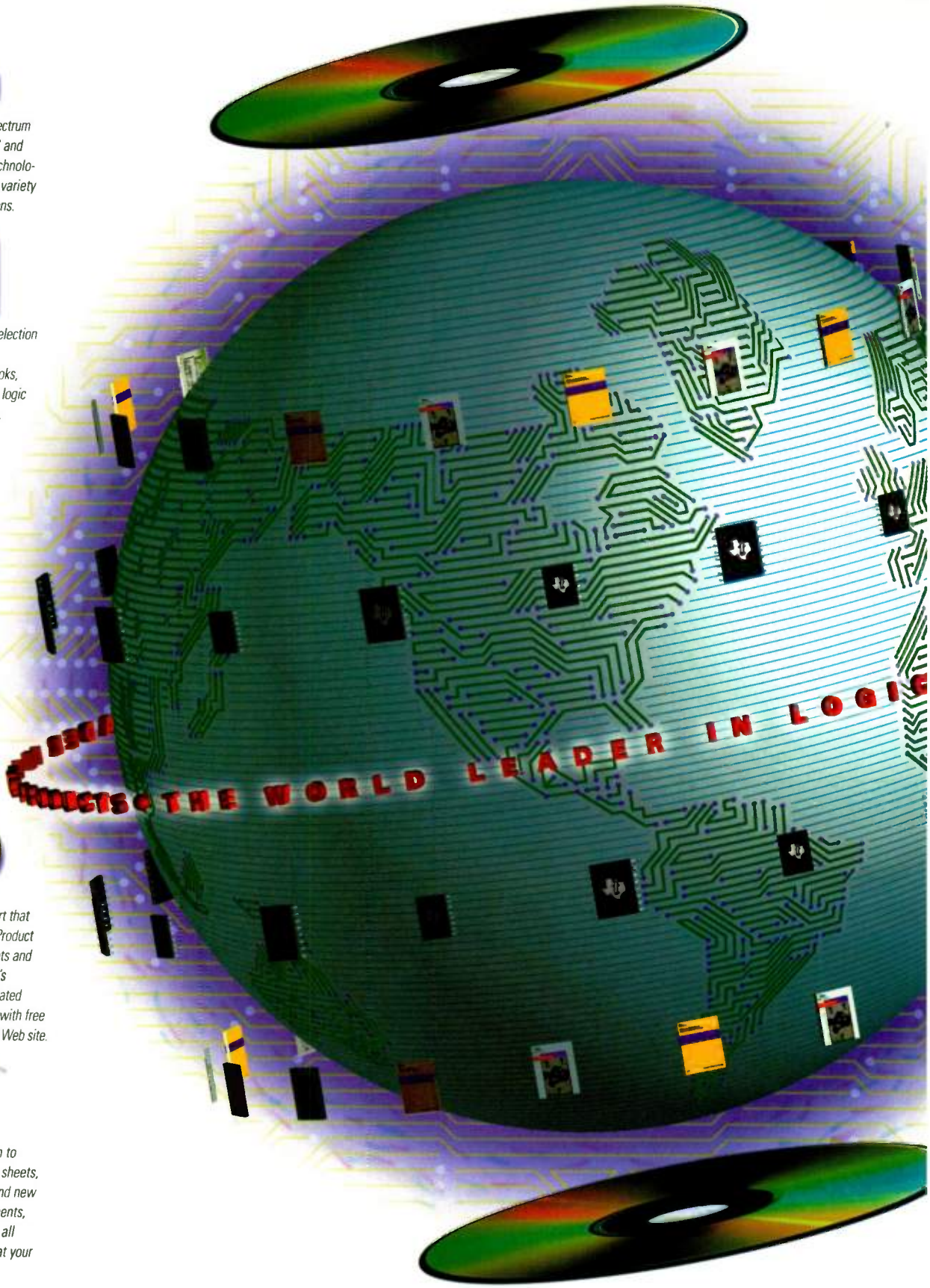

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TEXAS INSTRUMENTS

Wireless Payphones: A New Way To Communicate—Anywhere

Have you ever stopped to use a payphone and discovered that it didn't work properly? Perhaps you could hear the party on the receiving end, but they couldn't hear you, or vice versa. That could all change with the introduction of Code-Division-Multiple-Access (CDMA) digital wireless payphones from Qualcomm, San Diego, Calif.

The payphones promise to deliver crystal-clear voice quality, and private and secure conversations. They transmit 14.4 kbytes/s data transmission rates and G3 14.4 kbytes/s fax transmissions.

Based on the company's CDMA radio transceivers, these phones are fully self-contained, with built-in security features to protect the user as well as the phone itself. For example, a security protocol in the phone can be configured to confirm if the unit is securely connected to the payphone controller unit before initiating a call. This feature reduces the possibility of cloning, and theft of transferred credit- and debit-card payment data.

A unique code distinguishes the wireless payphones from the multitude of calls simultaneously transmitted over the same broadcast spectrum. The present analog system and other digital systems available today divide the available spectrum into narrow channels, and assign one or more conversations to each channel. CDMA, on the other hand, has a wideband, spread-spectrum technology, that works by distributing multiple conversations across a wide segment of the broadcast spectrum. This technology helps to ensure a high voice quality throughout the life of the phone call.

What really makes this development exciting is that wireless payphones offer rapid deployment, and can be easily redeployed to meet public access demands as the need arises. When these phones hit the streets, you will no longer have to wait in long lines to use a payphone while attending a trade show or conference.

Do you use public transportation? These phones may be used for high-traffic, public transportation areas as well as disaster-relief areas. This means that the next time El Niño strikes again, you won't have to worry about being isolated from the rest of the world by downed phone lines. Digital wireless phones are impervious to power outages.

An optional battery pack and solar charger are also available, with support service in remote areas.

For additional information, contact Qualcomm Inc., 6455 Lusk Blvd., San Diego, CA 92121; (619) 651-8768; fax (619) 651-8962.

Bradie Sue Grimaldo is the West Coast Editorial Assistant for ELECTRONIC DESIGN *and the Marketing Assistant for* MICROWAVES & RF. *Grimaldo is currently pursuing her Associate's degree in Journalism at San Jose City College, Calif.*

Testing The CardScan Business Card Reader

How many times have you come home from a trade show or conference with your pockets bulging with business cards? You may promise yourself that you'll key them into your contact manager. But more often than not, the cards end up moldering, forgotten in a desk drawer.

Although these contacts are a journalist's life blood, attempting to migrate my 700+ card collection into a database seemed impossible. Then, there was the issue of finding the time to update it with the 30+ new contacts I make each week. That's why I looked forward to test-flying the CardScan Plus 300 business card scanning system from Corex Technologies.

The consumer version of CardScan consists of a small desktop scanner, designed specifically to inhale a business-card-sized piece of paper and pass its digital image on to a computer for further processing. Corex's 32-bit, Windows-based text-recognition software extracts the name, address, phone number, URL, etc., and puts them into its filing system and contact manager. Just translating paper cards into an electronic Rolodex would be a tremendous leap forward, but the CardScan software also lets you use the data in everything from mailing labels and faxes to steering web browsers directly to a selected contact's site.

Because many of us work in groups, the need to share contact information is critical. Corex also offers additional software packages which allow users to share a single scanner to compile their own data bases. Equally important, CardScan lets users exchange contacts freely among themselves, as well as through a central database.

I was fairly pleased with the time savings and versatility it offers. Setting up CardScan was straightforward, requiring only a connection to my PC's parallel port, and a software installation. Once operational, it did a pretty good job of getting around on a card and entering the data into the correct field. Occasionally, it would stumble over the odd card with exceptionally peculiar fonts, but it was still orders of magnitude easier and faster than entering the data by hand. There also were instructions for using the software with almost any TWAIN-compliant flatbed, handheld, and sheetfed scanner.

Corex also offers an OEM version of CardScan for embedded applications. Intended for use in lead-capture systems for trade shows, automated kiosks, and other devices which record people's personal data. A complete software development kit is available to allow easy integration and customization of the unit and its software.

For more information, contact Corex Technologies Corp., 130 Prospect St., Cambridge, MA 02139; (800) 942-6739; www.cardscan.com. For OEM applications, contact Corex's wholesale support line at (888) 888-7226 ext. 252.

Lee Goldberg

KMET'S KORNER

What measures do you take to avoid marketing and sales assaults? If you're like me, you have a number of shields in place for protection. Here are a few techniques I use, and the system which shattered my defenses—the "blinking light."

I find physical mail the easiest advertising form to control. Unlike many of you, I do not have mail delivered to my home. Mail gets delivered to our local post office. A mile separates me from my mail. A few times each week, I empty my mailbox, place the contents on a table within the post office, and proceed to run my well-refined sort algorithm.

I place first class items in one pile, and all other pieces in the trash can for automatic recycling. The remaining first class stack gets one more screen, which results in over half of it tossed into the recycle can. I then read and process the remainder of my mail. I like this system. My physical mail remains out of sight and out of mind until I elect to deal with the stuff; sorting only takes a few minutes each week.

The phone presents its own unique challenges. Defensively, I've sent letters to many database firms requesting that they remove my name and number from their computer systems. This step keeps most of them from calling, but provides no protection against random solicitors. To fight them, we use an answering machine. We've informed the folks who call us routinely that we screen all calls. They know to leave at least a 10 second message, which, if we are home, gives us time to recognize their voice. This system is 100% effective. Telemarketers do not leave messages!

RON KMETOVICZ

Television presents smaller challenges. Not watching it presents the best defense. When engaged in the act of real-time observation, I gravitate toward PBS or subscriber-funded channels. Network programs are best watched after being recorded on a VCR. Effective use of the VCR makes it possible to fast forward past commercials in just a few seconds. This technique quickly wears out the VCR, though.

I find Internet methods quite easy to ignore. Banners rarely attract my attention, and those that do only take a few seconds to explore at the next deeper level. I might spend a few minutes each week digging down deep to get to the "no thanks" button. And, so far, I have not received any unsolicited e-mail hocking products or services.

The previous paragraphs might make you think I'm in control. Well, I was...until the "blinking light" came into my home. It's a feature of my Digital Satellite System (DSS), by which Direct TV or USSB send me a sales and marketing pitch over the microwaves. When they do, a green light-emitting diode (LED) on the receiver blinks. Opening the message, almost all the time, results in my reading its content. And, surprisingly, most of the messages have been informative. I actually want to read them.

I encourage marketing engineers reading this column to check out the "blinking light" DSS feature. It's not just the light, but the information content behind the blinks that gives this system its uniqueness. Effective adaptation of some of the structures could result in increased sales of your products. Is anyone against that?

Ron Kmetovicz, president of Time To Market Associates, is the author of "New Product Development, Design and Analysis." He helps new product development teams deliver profitable products to the market quickly. He can be reached at: P. O. Box 1070, 100 Prickly Pear Rd., Verdi, NV 89439; (702) 345-1455; fax (702) 345-0804; e-mail: kmetovicz@aol.com.

Extending The Design And Development Enterprise

How does an $18-billion company, known for office machine copiers, document handlers, and printers, compete in a rapidly growing, low-cost, digital "convenience" copier/printer market? How does such a company "reenter" such a market after abandoning it about a decade ago due to price competition? Xerox Corp., Rochester, N.Y., faced this challenge two years ago, when it decided to develop its 214 and 212 digital copier/printers.

Xerox immediately recognized two goals as the answer: Sizeable reductions in product development costs and cycle times would permit Xerox to compete effectively. The company formed their "extended enterprise" process to reach these goals. Xerox stuck to its core strengths, while forging an alliance with key partners, thereby gaining access to the partners' strongest product elements.

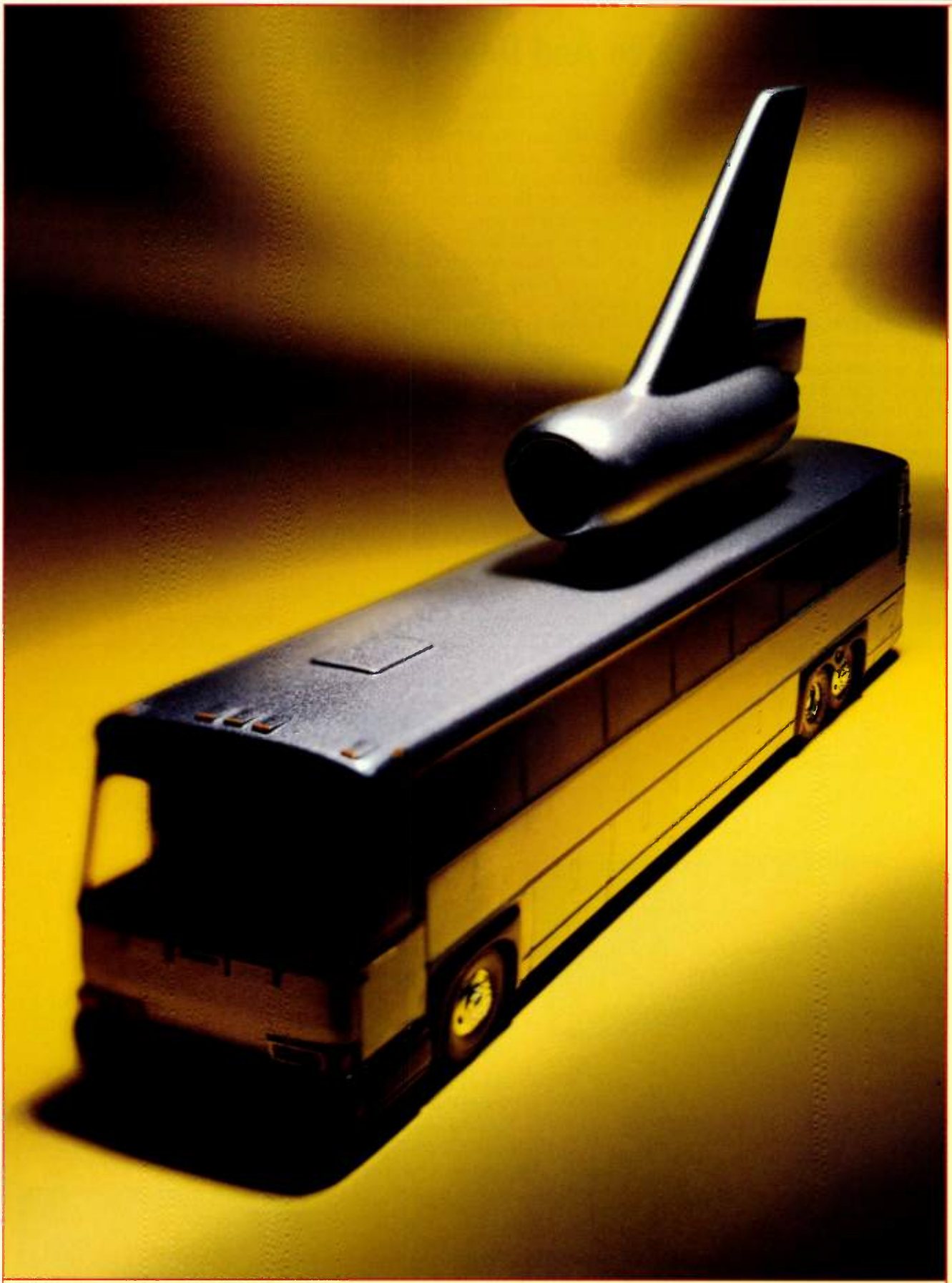
In this setup, a design is employed, each strategic partner produces one or more of the end product's subsystems to meet a specification (set by Xerox). Next, all the modules are assembled. Digital copier/printer models 214 and 212, with outputs of 14 and 12 prints/min., at a resolution of 600 dots/in., are the results of this. The suggested retail prices for these models are $2095/ $2550, respectively. Xerox states, this is almost 30% less than the cost of comparable analog copier products.

Several key strategic partners working together on a product is not new, and is used by many other companies. But Xerox went one step further: They mandated that engineering and marketing personnel from each strategic partner had to actually physically work together in the same location. In a building Xerox and its partners occupied, engineers and marketing personnel worked closely for over two years to produce the models 212 and 214 digital copiers/printers.

Key partners chosen were Mack Molding Co., E. Arlington, Vt., to produce the paper-tray module, plastic moldings and the products' covers; Ascent Power Tech., Ontario, Canada, who developed the electronic control and power subsystems; Fuji Photo Optical Ltd., Saitama, Japan, provided the scanner and laser imaging technology; and Shinano Kenshi Ltd., Nagano, Japan, produced the mechanical drives and shafts.

Early on, Xerox decided to stick to its core strength—"xerography." They used an advanced ASIC, developed by Xerox's Image Processing and Advanced Computer Tech. (IMPACT), a unit of the company's Corporate Research and Technology organization. This unit is a "virtual-copier-on-a-chip," and contains all the critical image-processing functions. It is integrated within the control subsystem produced by Ascent Power Tech. Xerox applied its traditional expertise to the imaging cartridge, fusing subsystems, and document-handling subsystem.

Roger Allan



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READER SERVICE 162

HEADS UP

A friend of mine likes to describe reflective displays as "black, white, and squint." But what designers want are handheld, smart electronic products, probably a high performance thin-film transistor (TFT) or a color super-twisted nematic (CSTN) display. Such a choice is likely to mean that it's not only the most costly and bulky component; it also consumes the most power.

To hit the power, size, and cost targets of many portable products, designers have turned to reflective or transflective displays. Reflective displays eliminate the thick and power-hungry backlight, altogether. Transflective displays can operate as both a transmissive or a reflective display. They must, however, retain the backlight for occasional use.

The problem with most of these displays is that their visual performance has not been very inspiring. Many are monochrome, with little or no gray scale, or offer a very small color palette. They also have a very slow response. While reflective displays can have good contrast in high ambient light conditions, they are useless in dim environments. Transflectives allow periodic illumination, but must often compromise visual performance. Therefore, they are worse than either transmissive or reflective displays.

Until recently, no one really figured out how to build a visually attractive, color-reflective display. Now, a spate of announcements and demonstrations indicates that color reflective displays—with much improved visual performance—are nearing commercial availability. They could start showing up in audio/visual, portable information tools, and smaller PC products by the end of the year. Consider these developments in color-reflective displays:

- Sharp, Camas, Wash., says that production has now started on 2.5-in. device, and will follow up with 3.9-in. and 8.4-in. models.
- Toshiba, Tokyo, Japan, is planning to start mass production of 8.4-in. panels in Q1 99.
- By the spring of 1999, Sony, Tokyo, Japan, is planning production of 8.4-in. products.
- Philips Flat Panel, San Jose, Calif., says they will begin sampling 8.4-in. and 12.1-in. devices by this fall.
- Hitachi, Norcross, Ga., is showing key customers prototypes from a quarter to half VGA, and is talking about production next year.
- Production of 5.7-in., 7.2-in., 10.4-in., or 12.1-in. displays may begin as early as Q3 by Kyocera, Kagoshima, Japan.
- Epson Electronics America, Redondo Beach, Calif., is showing two 312 × 230 displays with production possible by Q1 99.
- Papers on 4.4-in. to 7.8-in. prototypes were presented by Matsushita, Osaka, Japan, at last May's SID '98 conference.

CHRIS CHINNOCK

Sharp, Toshiba, Sony, and Philips are pursuing a TFT approach, while Hitachi and Kyocera are going for STNs. Epson is using a matrix of thin-film diodes, while Matsushita appears to still be evaluating both TFT and STN approaches.

The CSTN reflectives are currently in the "showing prototypes to customers" phase. Kyocera, for instance, says that they probably need to get better color saturation and more reflectance from their devices before they are able commit to production.

Perhaps a solid representative of the TFT camp's approach is Sharp's color-reflective line. They have dubbed it Super Mobile Highly Reflective (HR) TFTs. Technology that is capable of boosting the reflectance of the back electrode from today's 10%, to about 30% in Sharp's case, is key to this approach. When combined with their manufacturing method for improving the aperture ratio, the 8.4-in. model ends up being one-third thinner, one-half lighter, and using one-seventh the power of a comparable transmissive TFT. Also featured are 50 ms response, a 260K color palette, and a 100-degree viewing cone. They are very good-looking displays.

Philips says they are also evaluating customer reactions and working in three areas: color filters, optimization of the liquid crystal cell, and compensation films. Good color saturation can be achieved with thick filters. But, it reduces light transmission for light going in and being reflected back out of the display. The result is a grayish color on what should be a white screen. Cell optimization and film compensations are needed to help improve contrast, viewing angles, and speed of response.

An 8.4-in. color reflective could very well end up being a popular choice for a new generation of Windows CE computers. They will be power-miser baby brothers to desktop siblings. Also identified by most groups is the need for a front light.

So far, most agree that a good solution does not yet exist, but will be necessary to provide occasional illumination. Some applications are also likely to need a touch panel. Integrating a front light and touch panel seems a smart way to go.

Designers should begin to check these new color-reflective displays to see if they will meet the requirements of upcoming products. Why not put in your two cents for the features you would like to see? If you're a big enough customer, display manufacturers may even design a display or shift production to fit your needs. Sharp did. Perhaps my friend should change his tune on reflective displays.

Chris Chinnock holds a BSEE from the University of Colorado and reports on flat-panel displays and other emerging technologies. His company, Technical Marketing Service, provides writing, marketing, and public relations services to technology companies. Chinnock can be reached at (203) 849-8059; fax (203) 849-8069; e-mail: chrischinnock@compuserve.com.

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AT45D081	8M bit	5.0V	Serial	264 bytes
AT45D161	16M bit	5.0V	Serial	528 bytes
AT45DB011	1M bit	2.7V	Serial	264 bytes
AT45DB021	2M bit	2.7V	Serial	264 bytes
AT45DB041	4M bit	2.7V	Serial	264 bytes
AT45DB080	8M bit	2.7V	Parallel	264 bytes
AT45DB081	8M bit	2.7V	Serial	264 bytes
AT45DB161	16M bit	2.7V	Serial	528 bytes

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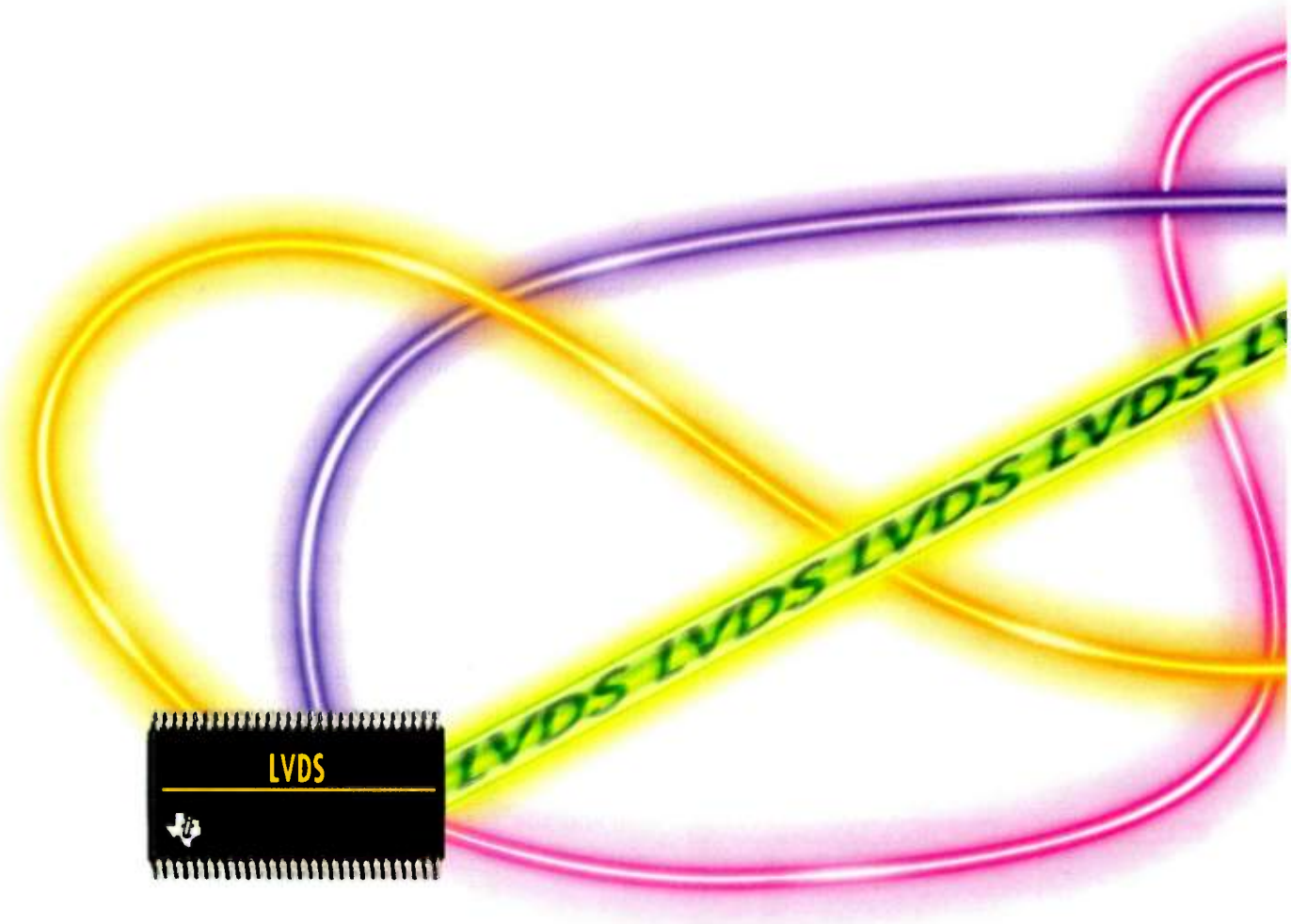

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& ANALOG

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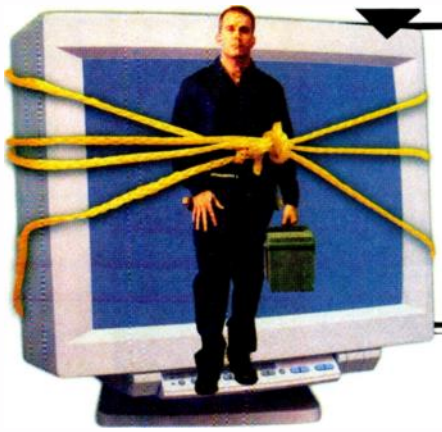

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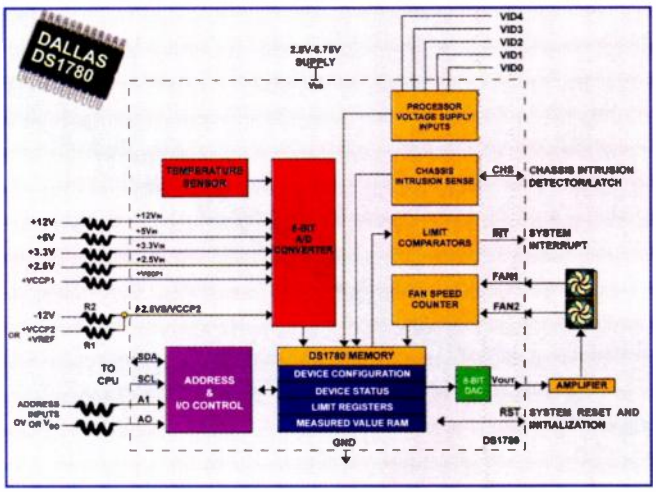

or calibration. It's easy to program—uses the popular 2-wire interface with 2-bit addressability. And it's easy to test—integrated NAND tree provides board-level testability. The DS1780 is also the ultimate security guard: it will signal when the case is opened, even if the power is off.

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READER SERVICE 121

Speed Does Matter: Gigabit Switch Chip Raises The Bar

New Switch Chip Family Cuts The Cost Of A Gigabit Switch Port Below $100. A Flexible Ring Architecture And Modular Design Support Many Applications.

Lee Goldberg

Godzilla may claim that size matters, but engineers know differently. In the realm of high-speed communications, at least, it's speed, price, and functionality that determine whether a product is a box-office smash. Perhaps it's no coincidence, then, that just a few weeks after our favorite radioactive reptile rampaged New York, Silicon Valley is being stalked by the Allayer AL100 and AL1000. This pair of powerful little monsters is ready to eat traditional networking semiconductors for breakfast.

COVER FEATURE

Designed by Allayer Technologies, a San Jose, Calif.-based fabless manufacturer of communications semiconductors, the AL1000 chip holds all the digital circuits needed to implement a two-port Gigabit Ethernet switch *(Fig. 1)*. Its companion, the AL100, has a similar internal architecture, but carries eight full/half-duplex, 10/100 Fast Ethernet media access controller (MAC) interfaces feeding its switching circuitry *(Fig. 2)*. Both of these chips can be assembled, like building blocks, into a multitude of switch configurations using an on-chip high-speed expansion bus.

According to marketing manager Dave Wong, Allayer hopes this chip set will help close a perceived market hole between Fast Ethernet and Gigabit-capable equipment. Wong foresees a time in the near future when almost every PC made for commercial service will come equipped for Fast Ethernet—something that will seriously tax the capabilities of most LANs. High-performance workgroups already generate Gigabit torrents which swamp the installed base of hubs, switches, and routers.

This situation will only worsen as diskless, "thin-client" network computers (NCs) grow in popularity. NCs will place even greater bandwidth demands on existing networks, as they are asked to ship operating systems, applications, data files, and multimedia streams from a centralized server. Without a Gigabit uplink in the local switch, these bandwidth-hungry devices could find themselves competing for access to one thin data pipe.

Wong notes that none of today's moderately priced, Fast Ethernet workgroup switches have a Gigabit uplink, an essential element for efficiently tying workgroups to a server without serious congestion. He envisions a solution in the form of a "hybrid switch," with both 100- and 1000-Mbit/s Ethernet connections in the same box. One of the primary applications for the Allayer chip set will be to provide just this kind of equipment, at a price that resource-starved network managers will appreciate.

Allayer's multispeed switching is made possible by an on-chip expansion bus interface, which allows the switch chips to exchange Ethernet packets at wire speed. Known as the RoX (ring of switches) bus, it uses a closed-ring architecture to circulate traffic through up to four switch chips *(Fig. 3)*. This scheme also facilitates the assembly of larger switch configurations.

The patent-pending, 66-MHz, 32-bit parallel data bus permits chips to circulate packets at 2 Gbits/s. A separate control channel within the RoX bus allows swift transmission of status, routing, and flow-control information between all network elements.

The RoX bus has an effective rate of 4 Gbits/s, because each chip is receiving and transmitting simultaneously. According to Allayer, this allows non-blocking, wire-speed transfers between ports in fully loaded, two-chip switches. Due to the efficiency of the RoX bus, a four-chip eight-port Gigabit switch, running at full capacity, will have only a 10% chance of experiencing blocking at any given moment.

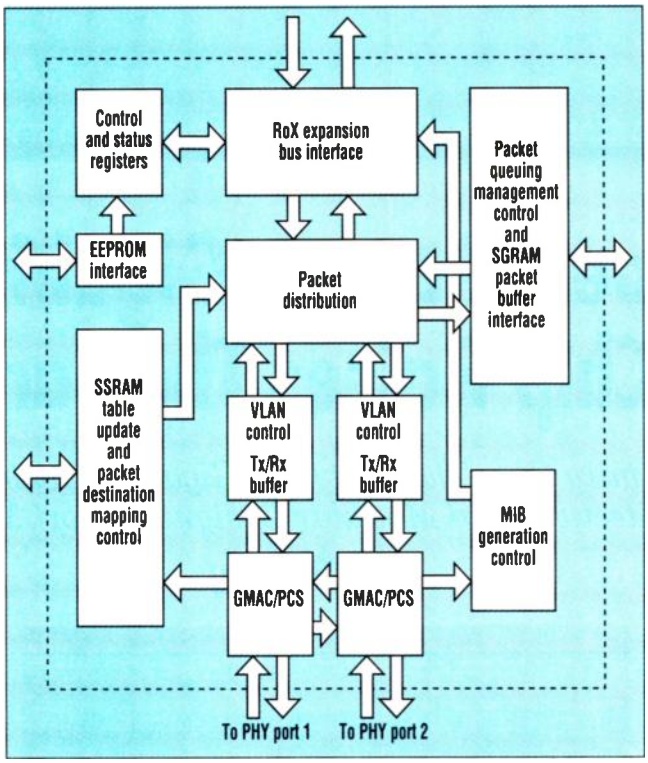
A third chip, the AL300 management engine, can be added to extract and log statistics and management information from the switch engines. Using the management ring in the RoX bus, the AL300 collects all the port information required to provide spanning tree support for the other RoX chips, as well as all the required management information base (MIB) statistics used in SNMP and RMON protocols.

The two switch chips, mixed and matched at the designer's discretion, offer the right mix of ports for almost any networking box. The price savings over today's implementations is also significant. Wong estimates that a fully functional Gigabit switch can now be assembled for a total semiconductor component cost of less than $100 per port. He predicts that this could signal a sea change in the networking industry, as the modular chip set allows manufacturers to produce extremely cost-effective hybrid switches. For example, a fully loaded system with 24 10/100 Ethernet ports, and a pair of Gigabit connections to LAN backbones or server farms, would retail for $2000 to $2500. A comparable configuration would cost $4000 today.

Other applications for the versatile trio include a standalone two-port Gigabit Ethernet switch (bridge), or a layer-2 Gigabit Ethernet switch that is cascadable up to eight ports. Future developments include a bridging module for a layer-3 routing/switch processing module, which will plug into the current layer-2 switch.

Several factors contribute to the AL1000's high functionality and low cost. First, the RoX bus provides a fast way to pass data between chips, while performing double duty as part of the switch fabric itself. Another cost-saving measure is the use of inexpensive synchronous graphic RAM (SGRAM) to perform the buffering between input and output ports. Finally, Allayer's designers took a close look at the tasks performed by each networking function. They came up with an innovative and efficient means of breaking them up into discrete blocks, which could be efficiently integrated onto one chip.

Despite their low cost, the Allayer switch chips offer many of the capabilities found in the most sophisticated networking equipment. The AL1000 packs a pair of full-featured IEEE-802.3z Gigabit Ethernet MAC engines that include an integrated Physical Coding Sublayer (PCS). The PCS performs the 8B/10B PHY-layer encode/decode function. Full auto-negotiation capabilities, as well as support for the IEEE-802.3x flow-control mechanism for packet-congestion control, are offered by the MAC logic in both the AL100 and AL1000. Both chips are also VLAN-capable, with on-chip IEEE 802.3ac VLAN Tag/Untag functions on each port for both incoming and outgoing directions. This permits an AL100/1000-based product to easily support both implicit and explicit port-based VLAN schemes.



1. The AL1000 incorporates two Gigabit Ethernet media-access controllers (GMACs) and a 2-Gbit/s (4-Gbit/s effective rate) expansion bus that allows the connection of up to four chips in a ring of switches (RoX). On-chip logic handles all bus arbitration, address translation, and tagging to support IEEE-standard VLAN protocols.

A Look Inside

The main interfaces on the AL1000 are the two gigabit media-access-controller (GMAC) ports. These ports connect the device to the serializer/deserializer (SERDES) devices, which form the first layer of the physical interface *(Fig. 1 again)*. The AL1000 also manages two SGRAM interfaces that each support up to 512k by 32 bits of external memory. Each SGRAM interface buffers the outgoing (and incoming) data for one of the GMAC ports. This dedicated wire-speed buffer completely eliminates any head-of-line (HOL) blocking that might occur as an Ethernet packet awaits its turn to pass through the switch.

Using a programmable processor to perform any sort of header processing on a per-cell basis is not only expensive. It's also impractical at Gigabit speeds. The AL1000 handles tasks like VLAN tagging with blocks of highly optimized, dedicated logic within the chip itself. For example, the chip's VLAN Tx/Rx buffer registers contain control logic that modifies the Tx/Rx packets with VLAN tag insertion and stripping, and performs CRC regeneration. Each port has an option to tag or untag outgoing packets with their corresponding VLAN ID. The chip's tagging mechanism can handle packets which arrive with explicit VLAN tags, or create them for untagged packets using their source-port ID.

The switch's table update and packet-control block uses either an on-chip memory or external SSRAM array (32k by 32 bits) to store the variables used for address learning, aging, and destination-address map-

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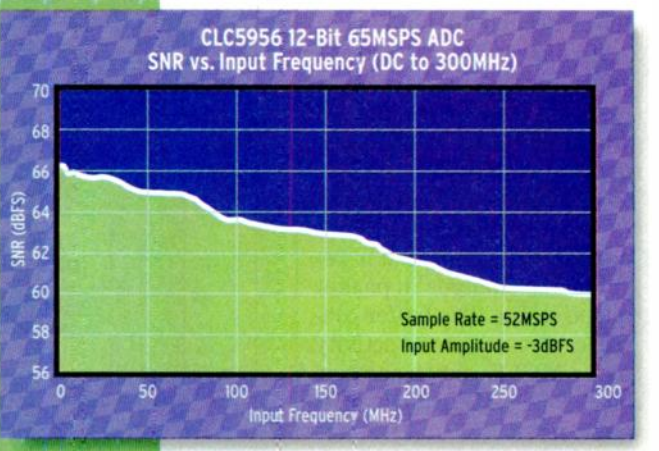

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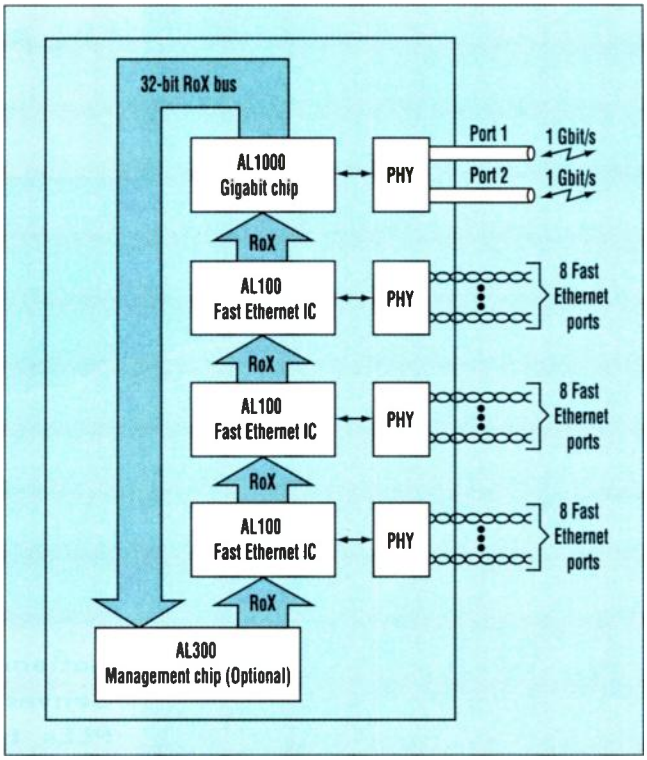
ping functions. Each Gigabit MAC/PCS block takes the packet data from the associated TX buffer for transmission, and delivers the received packet data from its port into the associated RX buffer.

To ease congestion in the switch and prevent packet loss, the buffer controller works in concert with the packet-queuing control block to generate IEEE-802.3x flow-control packets. These packets are generated in response to changes in packet queue status. The buffer controller also reports its activity to the MIB Event Generation block for SNMP/RMON MIB accumulations.

For the dynamic MAC address learning, the SSRAM packet destination-mapping control block creates a table. This table holds the source MAC addresses and its associated port ID from packets received from both ports, as well as incoming packets from the RoX bus. Meanwhile, the control block runs a process to age each dynamic MAC entry.

Destination mapping is performed by taking the MAC address from the received packet. The table is then searched to find a match that associates the related ID with the packet. If there is no match, the packet will be flooded or forwarded to a designated uplink. When a match is found, the packet is forwarded to the port associated with the Port ID, or passed to a group of ports associated with the Multicast Group ID. Packets are then filtered for errors or invalid addresses.



3. The Allayer architecture allows construction of an inexpensive "hybrid switch," which has up to 24 10/100 Fast Ethernet ports and a pair of Gigabit Ethernet uplinks. An optional management chip (the AL300) supports full MIBs for SNMP and RMON, and permits the host controller or communication processor to connect to the switch.

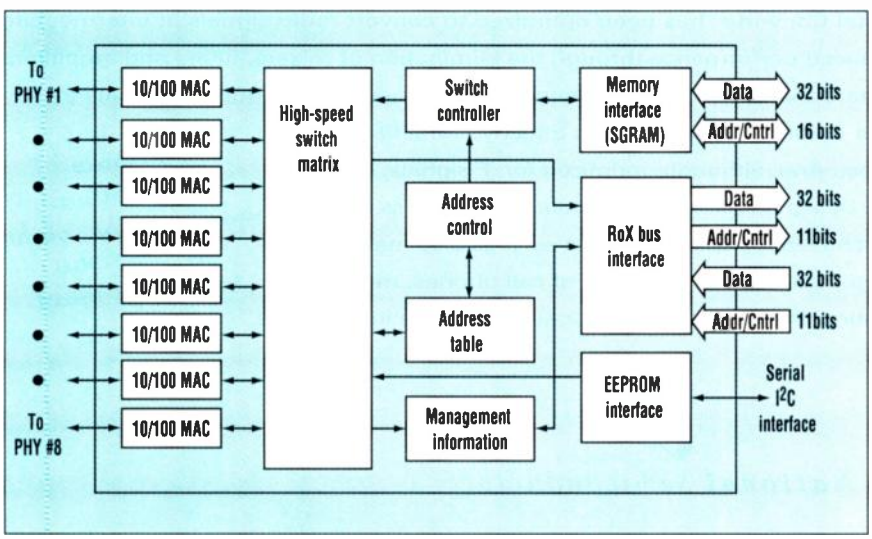
Efficient management of the buffer is an essential part of a high-performance switch. It ensures the best use of available capacity and minimizes latency. The packet-queuing control and SGRAM packet buffer-control block is responsible for the queuing and buffering of the incoming packets from both ports.

Although packets will be buffered on the input side when received from both ports, the queuing control structure is based on output ports for the whole system. Each output port will, optionally, have guaranteed minimum buffer space. In addition, the HOL blocking associated with input buffering is avoided. The queuing control will track the buffer utilization watermark. It notifies the related MAC to send flow-control packets once too many packets are queued in the buffer and the watermark is passed. Congestion in the switch is thus avoided.

The packet-distribution block is responsible for the packet forwarding among the ports, the SGRAM buffer, and the RoX Bus interface. Packets received from ports will be sent to the SGRAM buffer, along with header information from the destination mapping block. Once in the SGRAM, packets bound for a local (on-chip) port are forwarded to the corresponding MAC/PCS block through its TX buffer. If the destination is somewhere off-chip, the packet is forwarded to the RoX interface block. It is then transmitted to the next device for further processing.

Packets downloaded from the RoX bus are forwarded through the TX buffer block to the corresponding MAC/PCS block for transmission. This block maintains a multicast packet buffer for storing the downloaded packet. The buffer prevents interruptions in RoX bus operation, which often occur when one of the MAC/PCS blocks is transmitting another packet.

The RoX expansion-bus interface



2. The AL100 contains eight complete full-duplex 10/100-Mbit/s Fast Ethernet MACs and a non-blocking switch matrix. Should more ports be needed, the on-chip RoX bus can connect it to three other Fast Ethernet or Gigabit Ethernet switch chips.

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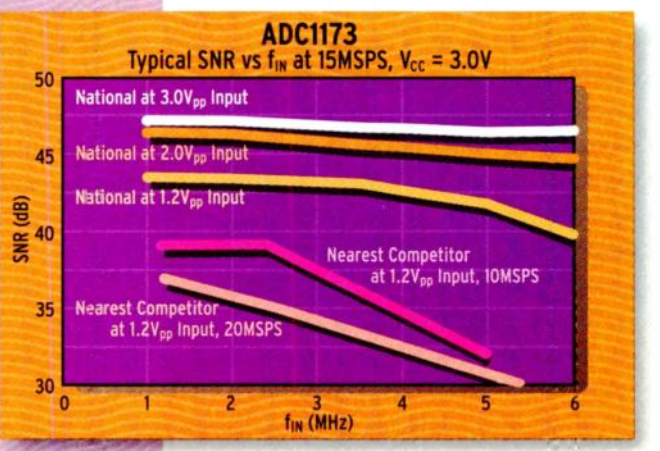

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block is responsible for the packet transfer between switching chips. It runs a protocol that manages the bandwidth allocation on the RoX ring. When receiving packets from the ring, the interface checks their destination. If appropriate, it then downloads them to the packet distribution block for distribution within the chip. If the interface does not see a familiar address, the packet will be passed back to the ring for the next downstream device. Meanwhile, the expansion bus interface block will insert the packet from the packet distribution block onto the ring, according to the bandwidth negotiated. It will also use the control channel in the RoX ring to manage the MIB event, system control, and status-report information transfer.

Manageability Is Key

In today's complex network environments, support for standardized management solutions is no longer an option.The AL100 and AL1000 have built-in statistics-collection logic. The RoX bus is structured to allow in-band transmission of statistical data to the AL300, or another central management device. Each switch segment features an MIB event-generation block, which is responsible for maintaining a set of MIB counters. These counters track, receive, and transmit activities on both ports.

The AL300 MIB is designed specifically to support SNMP/RMON network management. It maintains a small counter for each MIB, and generates a MIB event whenever a counter is wrapped around. Each MIB event is delivered through the RoX control ring to the AL300 for further accumulation and processing. A single AL300 can provide statistics collection and management functions for any combination of 100Base and 1000Base Ethernet ports. It also supports spanning tree information for the chip.

While the AL300 passes control and status packets between the switch chips and the control processor, it is not responsible for packet-by-packet enforcement of control or congestion-management policies. Instead, the AL300, or other control device, is simply responsible for programming parameters into the control logic on each switch chip. This distributed policy enforcement and address learning offloads the control processor, enabling much higher throughput than centralized control schemes found in other chip sets can offer.

The management chip also serves as a bridge between the switch itself and a host control processor. It provides a glueless interface to most 486-based microcontrollers and the MPC 801 series of PowerPC-based communication controllers. The controller serves as both a management interface and gateway, connecting between any one of several WAN transmission protocols, including HDLC and ATM.

By being compatible with two of the most popular controller architectures, these libraries offer access to a large base of commercial communication processing software. In the fast-moving, standard-dependent worlds of networking and telecommunications, they can reduce time and cost from a product's development cycle.

Other Applications

Thanks to its flexible architecture, these switch elements may find applications beyond a relatively simple workgroup switch. The AL100's ability to aggregate a number of Fast Ethernet ports into a single channel lets it inhale data from a disk farm or server at an enormous rate. In work groups that routinely process large amounts of high-speed multimedia, it could have important applications.The Allayer team has also begun to speculate about using their two-port Gigabit switches as bridges between RoX buses. By tying a pair, a dozen, or even more switching rings together, the AL1000's architects envision creating a very inexpensive fractional-terabit switch. For now, however, they're content to simply launch a revolution on the desktop.

Price And Availability

The AL1000 is sampling now, with production scheduled for October. It is housed in a 352-pin BGA package and costs $120. The AL100 is currently in production. Housed in a 352-pin BGA, the eight-port Fast Ethernet switch costs $100. The AL300 management chip also is in production. It comes in a 240-pin PQFP for $60. All prices are for quantities of 1000 chips.

For further information, contact Allayer Technologies Corp., 425 Koll Circle, Suite 109, San Jose, CA 95112; (408) 573-8880, fax (408) 573-8928, www.allayer.com.

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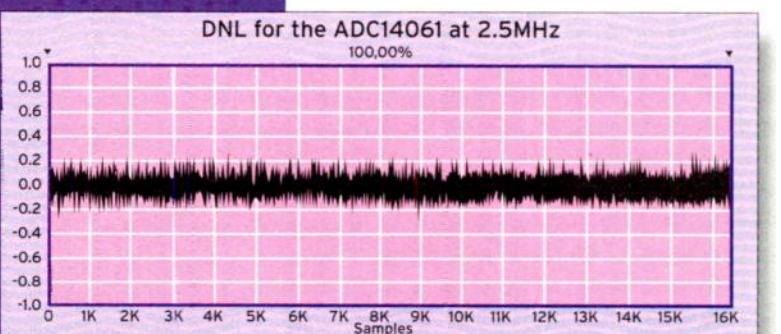

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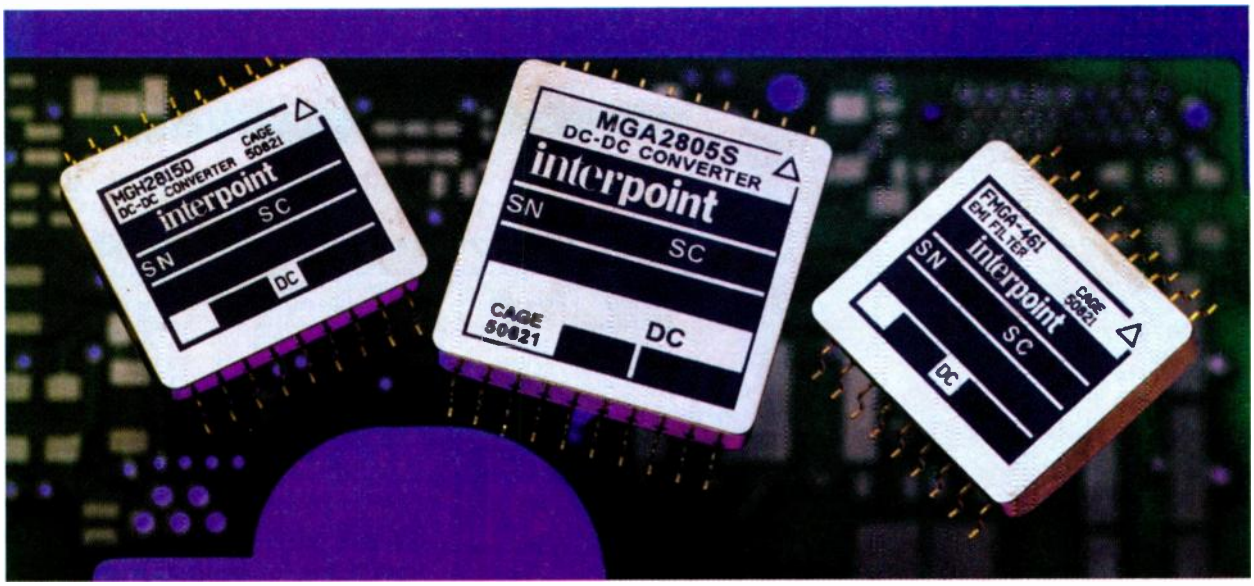

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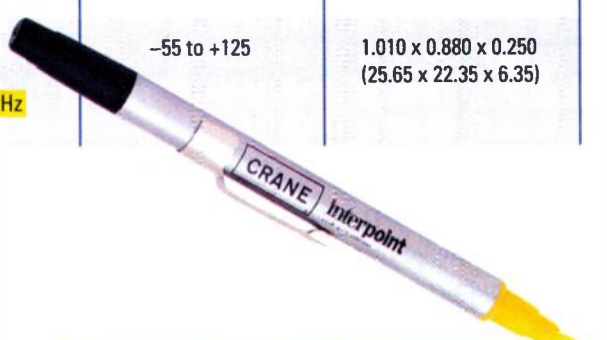
MGA Converter	Power 5 W	5, 12 or 15 single 12 or 15 dual	Continuous: 16–40 Transient: 50 V/50 msec	–55 to +125	1.110 x 1.110 x 0.250 (28.19 x 28.19 x 6.35)
FMGA Filter	Throughput Current 0.8 A	Noise Reduction 40 dB minimum at 200 kHz 60 dB minimum at 500 kHz and 50 MHz		–55 to +125	1.010 x 0.880 x 0.250 (25.65 x 22.35 x 6.35)



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Paging And Messaging Technologies: Versatile Wireless Workhorses

The Humble Pager Finds A Home In Many "Off-The-Belt" Embedded Applications, While Two-Way Messaging Services Pursue New Areas.

Lee Goldberg

SPECIAL REPORT

One day, we may all be wearing Dick Tracy-style wrist communicators, capable of sending and receiving e-mail, video conferences, or web pages. As the industry readies itself to roll out these multimedia, multi-megabit wireless technologies, it's easy to conclude that the relatively simple paging and mobile data networks of today will soon be obsolete. But, nothing could be further from the truth. Large numbers of these slower, dumber, less glamorous, and incredibly useful little critters are finding their way into both traditional and unexpected applications.

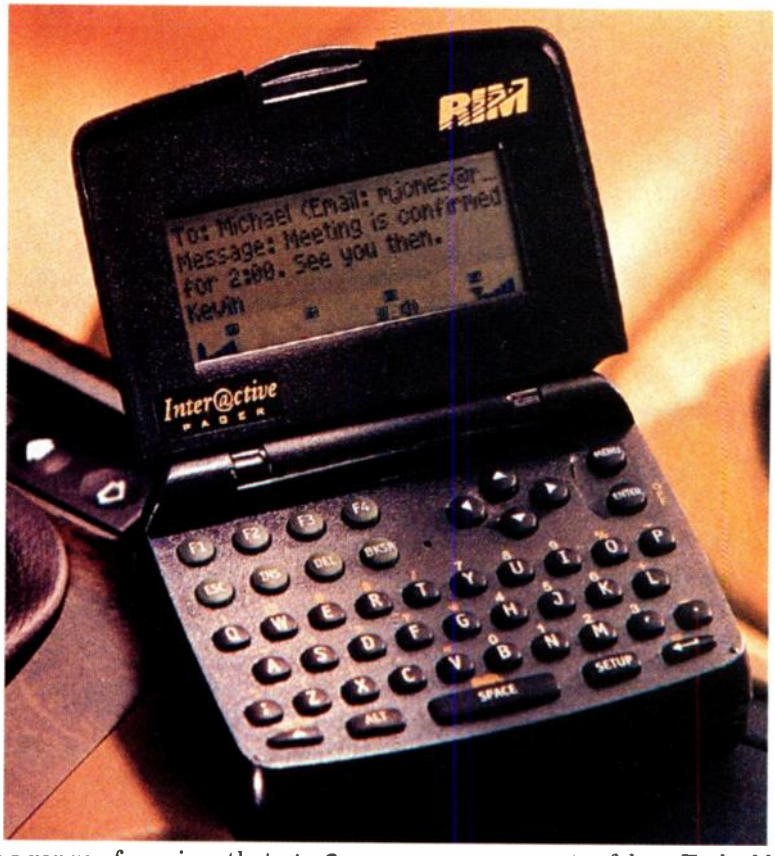
Stand-alone pagers have been enjoying tremendous popularity throughout the world (especially in developing nations). Yet, interest is also growing in embedding paging and messaging capabilities within other products. Many engineers find this a cost-effective way to add connectivity and intelligence to anything from traffic signals to medical equipment.

Other wireless messaging technologies, such as cellular digital packet data, mobile data services, and even satellite data, are finding growing markets in applications where paging systems cannot supply sufficient speed, capacity, or functionality. Indeed, there exists a range of services that can give you the right mix of coverage, speed, and file size for your project.

The first of these is the humble pager. Inexpensive, simple, and easy to design into most products, pager-type technologies are great stuff. Much like the POTS phone infrastructure, there may be more exotic high-performance wireless WAN technologies on the horizon. But, few will match their nearly universal coverage and low cost of deployment anytime in the near future.

Costing under $10 in parts and able to operate on minuscule amounts of power, three-chip, one-way pager circuits are easy to embed into a PC card, an industrial control system, or a palmtop computer. A local one-way paging service can run $5 or less per month. If needed, you can augment your local coverage with ties to the Internet and satellites to provide regional, national, and even international reach.

Network operators can support a large service area with a relatively inexpensive, thinly deployed infrastructure. Depending on terrain and other vagaries of propagation effects, base stations can be positioned 5 to 10 miles apart. This permits a handful of sites to cover both a large metropolitan area and its suburbs.



Art Courtesy: Research In Motion

Off The Belt!

Throughout the world, paging technology is also appearing in less traditional, "off-the-belt" applications. While the technology is slow (typically 9.6 kbits/s or less) and limited in capacity, a surprising number of vital tasks require relatively small amounts of data. Embedded paging is beginning to serve as an inexpensive, reliable way to do anything from updating prices in vending machines to posting messages on electronic highway signs.

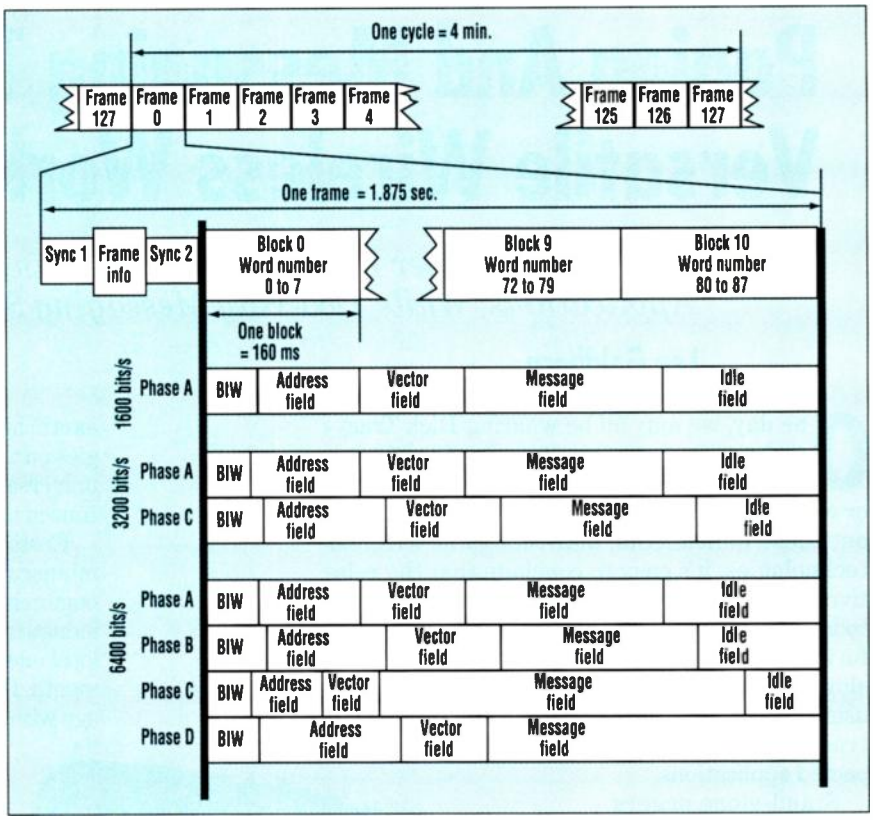
With the addition of two-way capability, it becomes easy to monitor the temperature of cargo in a refrigerated trailer, read a neighborhood's utility me-

ters, or receive an alarm from a fixed or mobile installation. The same technologies connect lightweight, handheld computers, organizers, and PDAs to e-mail, Internet, or other messaging services. Whether it's exchanging a quick e-mail about an appointment, collecting statistics on highway traffic flow, or sending a signal to activate the irrigation system on the south 40, pager technology can do it efficiently, and at a reasonable price.

Many applications can be easily piggybacked directly onto one or more pager networks. Thanks to simple modulation schemes and some modest error-correction coding built into their protocols, pager signals can be decoded at very low signal levels, –110 dB or lower. Combined with their relatively low operating frequencies (150 to 900 MHz), and depending on what part of the world you're in, pager networks can penetrate deep into buildings, even when transmission towers are several miles apart.

Protocols 101

Though operating frequencies vary from country to country, only a few major pager protocols are used around the world. This reduces potential interoperability problems, while increasing the availability of inexpensive merchant ICs. Until recently, the dominant protocol has been the Post Office Code Standard Advisory Group (POCSAG) system, which used a two-level PSK modulation scheme that could deliver data at up to 2.4 kbits/s over a 25-kHz channel.



1. The FLEX paging protocol packs messages for pagers into a four-minute-long series of 128 frames. Each frame contains the address of the pager that will receive the message and a word indicating message size.

Each pager has its own address, permitting it to receive and decode only the messages directed to it. POCSAG's symbol-oriented transmission format requires the pager to stay "awake" at all times. It listens for the start sequence, by which it synchronizes on , or reads, an incoming frame.

Standing on POCSAG's shoulders are the FLEX and ERMES protocols, which add new capabilities and power-

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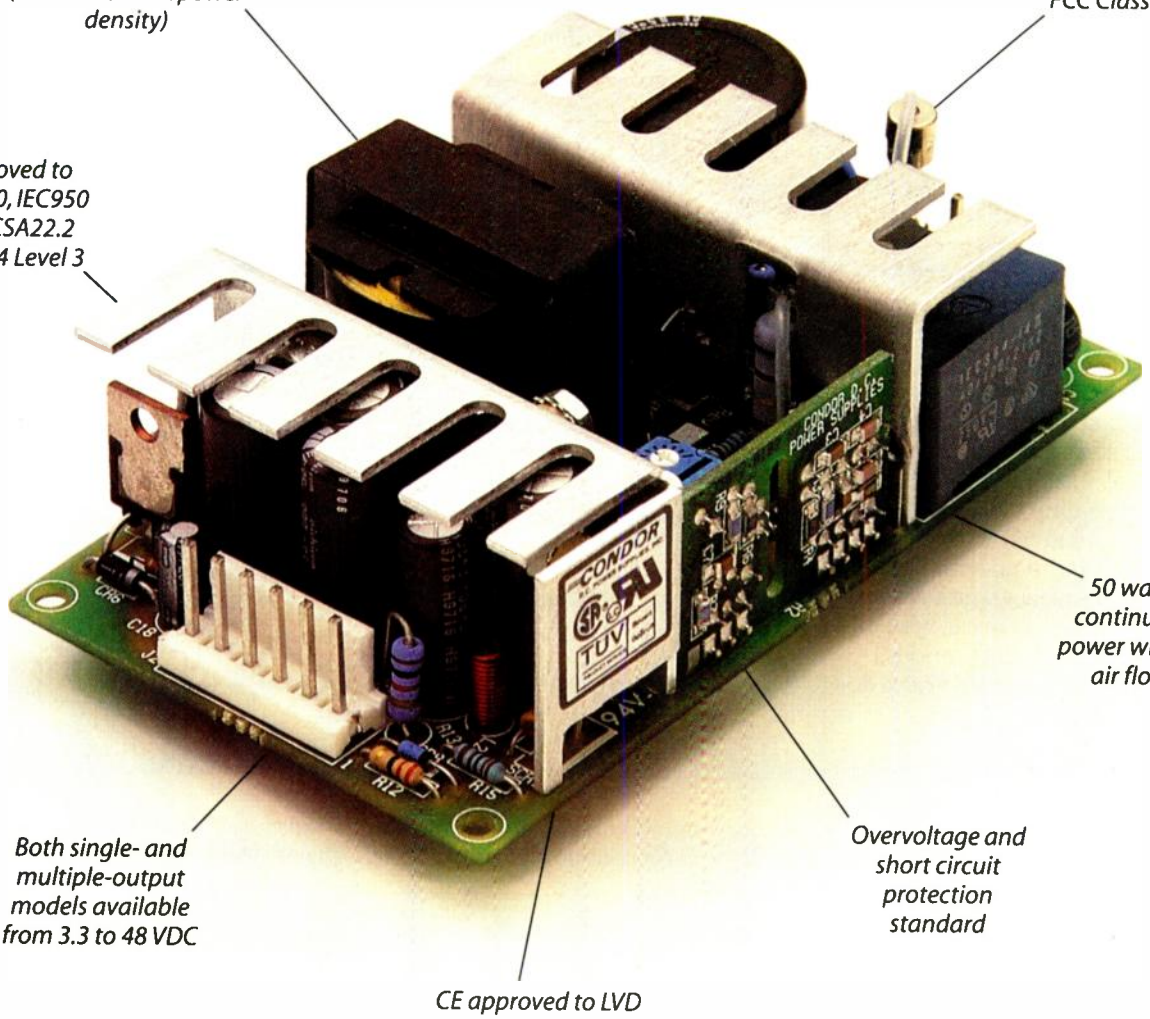

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saving features. These more advanced protocols support alphanumeric messages and higher data rates. Deeper modulation lets more subscribers share the same piece of spectrum. Equally important, the pager battery spends most of its time in a low-power standby mode, extending battery life.

FLEX was originally developed by Motorola, Schaumberg, Ill., but has been licensed by many other semiconductor and pager firms, including Analog Devices Inc., Norwood, Mass.; Lucent Technologies, Allentown, Penn.; Philips Semiconductors, Eindhoven, The Netherlands; and Texas Instruments, Dallas, Texas. It has become a sort of de facto advanced paging standard in many parts of the world.

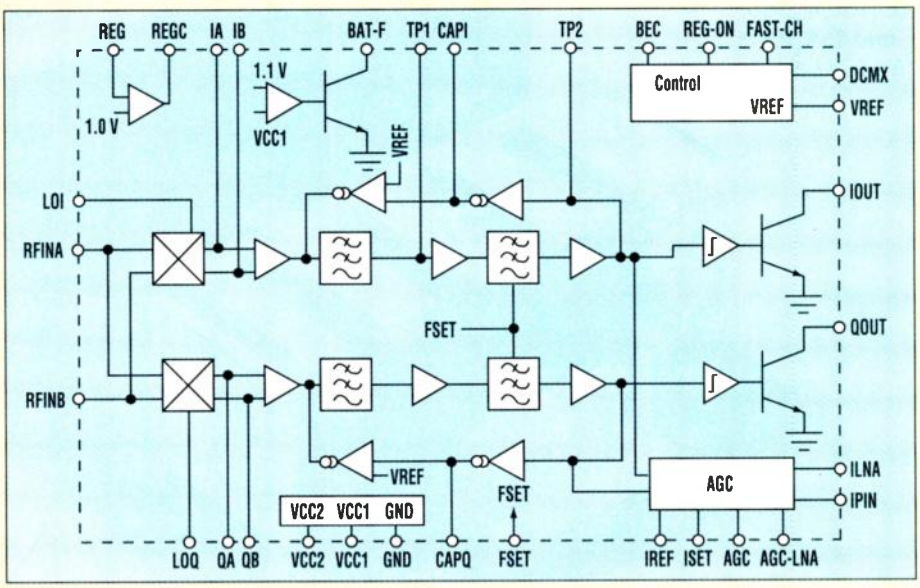
One key difference between POCSAG and FLEX is the synchronous time-slotted frame format, which places a message on the air at precise times. Each data-frame cycle consists of 128 data frames that are transmitted once during each four-minute period *(Fig. 1)*. Each frame lasts 1.875 seconds. A frame contains two synchronization sequences, a header that contains frame information, and 11 discrete data blocks.

FLEX assigns each pager a specific "home" frame within the frame cycle, and requires it to check that frame for waiting messages. During the four-minute cycle, the pager only has to wake up for a few seconds to determine if a message is waiting.

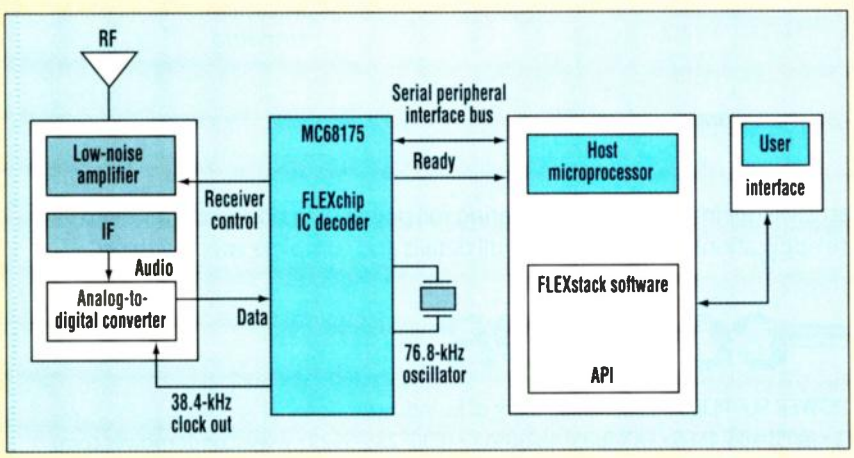
Upon awaking, the pager synchronizes on the frame header and adjusts itself to the transmitting network's bit rate. It then checks the frame-information header, looking for any waiting message with its address. If there is no message, it resumes its sleep mode, where virtually nothing but a small timer circuit remains active. Thanks to an aggressive power-management strategy, a FLEX pager can run on a pair of AA

Focus On Design For Embedded Paging

Compared with many wireless systems, pagers have a fairly straightforward system architecture. A typical FLEX-based unit will consist of an RF front end, a receiver/decoder that turns the baseband into a bitstream, and a host controller that handles the pager protocol stack *(Fig. A)*. The basic three-chip baseline design can be enhanced with off-chip RAM for more message capacity, or a frequency synthesizer to allow roaming in areas with different operating frequencies.



Earlier designs used analog decoders, but most modern pagers employ a DSP, states Vijay Dazar, technical manager for Motorola's two-way technology division, Austin, Texas. He explains that signal processors can employ Hilbert functions and other highly specialized filtering and correlation algorithms. Weak signals can then be extracted from high noise, multipath-filled environments.



Tunable antenna elements can also be controlled with DSP to overcome multipath and fading. A programmable solution allows field upgrades or new product-line features without needing to re-spin silicon. Using a basic 16-bit DSP, Dazar estimates that it takes about two-and-a-half MIPS to do basic FLEX demodulating and decoding. Adding ReFLEX functions raises the minimum to between six and 10 MIPS.

If cost is a driving factor, designers can sometimes eliminate the controller chip. This is done by by allowing the controller's functions to be

(continued on page 66)

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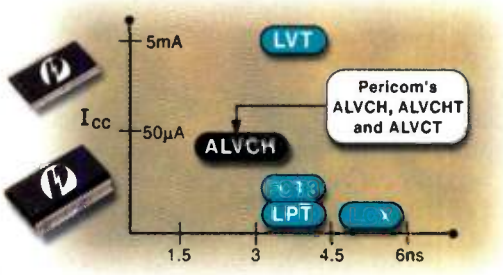

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batteries for several weeks or longer.

The FLEX air interface uses either a two- or four-level FSK modulation scheme to encode the outgoing bits on nearly any available frequency, from 150 to 900 MHz. To help protect against data loss due to multipath or fading, the bits within a message are interleaved. FLEX also uses CRC and FEC coding of the data stream to ensure that all bytes arrive in one piece.

As briefly mentioned earlier, the basic FLEX system has a dynamically adjustable bit rate that ranges from 1.6 to 6.4 kbits/s. Depending on the network, a FLEX data block actually contains between one and four 1600-bit/s subchannels, known as phases. Phases can be used separately or aggregated into faster channels. Further enhancements allow transmission rates of up to 9.6 kbits/s. Because a pager automatically adjusts itself to the available data rate, it can receive transmissions from any FLEX system, including older networks which run two-level FSK and support only a single phase.

Though designed primarily for short alphanumeric messages, FLEX has "hooks" that permit longer messages to be chopped up and transmitted in multiple blocks. In theory, this lets files of up to several megabytes be sent to a pager. In practice, it's usually best to keep file sizes to about 2 kbytes to avoid tying up the network for an uncomfortably long time. A 2-kbyte file can be surprisingly useful, allowing transmission of reasonably long text messages, small data files, and even short bursts of digtized, compressed speech.

The ERMES protocol was developed a bit earlier (in the late eighties) by a European consortium. It's similar to FLEX in that it uses a time-slot system, which permits the receiver to sleep most of the time. Unlike FLEX, it has a fixed transmit rate of 6.25 kbits/s, and operates only at a pre-assigned pan-European band at about 169-MHz. A fixed frequency may seem to be a disadvantage. But, it allows seamless coverage throughout the continent and contributes to the standard's widespread adoption in many countries.

Despite growing support for FLEX and ERMES, many POCSAG-based products will enjoy brisk sales during the next decade. Most will be used in areas with existing infrastructures, where lower traffic densities don't warrant an expensive "forklift" upgrade.

Two-Way Options

Senders can never be sure that their urgent messages have gotten through to a one-way pager. One solution is ReFLEX, an extension of the one-way protocol that offers two-way service at its simplest. A ReFLEX pager can talk back to the network, sending a brief "Ack-Back" message that acknowledges successful delivery or requests retransmission of any lost data blocks. Should short messaging be required, ReFLEX can easily be upgraded to provide it.

The Ack-Back signal also automatically locates a pager within the network. This solves another thorny problem for system operators who offer national coverage in regional segments. Knowing the location of a particular device saves network bandwidth. The message is delivered to a small group of base stations instead of the entire countryside being flooded in the hopes of reaching one particular subscriber.

Other more sophisticated versions of the ReFLEX protocol support long messaging and semi-real-time data transfers, making it possible to access e-

(continued from page 64)

performed using excess DSP power. The POMP-15 DSP/controller chip from Lucent Technologies, Murray Hill, N.J., for example, has enough power to support baseband processing, as well as the protocol tasks required for both one and two-way messaging. The POMP's 2.4-V logic draws just 0.7 mA per MIP. Rob DeRobertis, product line manager, Analog Devices, Norwood, Mass., anticipates 1.8-V devices, drawing 0.35 mA per MIP, being produced by the next generation of silicon processes.

Pager front ends are somewhat different from other RF applications. Designers must face difficult tradeoffs to achieve a balance between cost, sensitivity, noise immunity, and power consumption. This is made easier by the simple modulation schemes and relatively low frequencies used by pagers. These features allow the use of very novel receiver architectures and all-silicon MOS circuits.

For example, Mitel (formerly GEC Plessey), Scotts Valley, Calif., produces a series of direct-conversion, zero-IF (ZIF) receivers for both FLEX and POCSAG applications *(Fig. B)*. These receivers are widely used in Europe and Asia, where operating frequencies are often below 250 MHz. The direct-conversion architecture employs gyrator-based, on-chip filtering to reduce component count. Yet, great care should be taken when working with ZIF receivers. Compared to conventional receiver architectures, they are more susceptible to energy that can re-radiate from the local oscillator. It only takes a small amount of energy to desensitize a receiver stage or give its phase-lock circuitry fits. Wherever possible, it is advisable to provide shielding and decoupling components.

Even conventional receivers can easily be swamped by noise emanating from the pager unit, or the product it is housed in. Dazar notes that embedding paging systems within laptops or palmtops creates its own set of challenges. Laptops and PDAs are shielded against spewing the noise from their switching supplies and high-speed clocks into the outside world. Pagers residing inside their cases, however, must be properly shielded and decoupled from the power supply. Otherwise, pagers can see levels of Gaussian white noise that can slash sensitivity by 70 dB. If possible, Dazar suggests, place the pager circuitry outside the main enclosure.

Antenna design and placement is also critical to good performance. Unless you have the time for exhaustive analysis and testing, an external antenna is the way to go. This avoids the potential for accidental shielding, or interaction with the other active and passive components within the case. Finally, Dazar recommends that despite the extra cost ($0.50 to $1), antenna diversity is one of the best ways to ensure good reception under difficult conditions. In fixed applications, diversity becomes almost a necessity, as a piece of equipment can easily be installed within a permanent null zone.

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Adding Voice Technology To Next-Generation Pagers

Paging has been thought of as primarily a low-cost, reliable, one-way numeric notification system. Recent advances in both equipment and communications protocols, however, have made alphanumeric and two-way paging a common option for many users. By effectively integrating the use of voice-telephone access, paging will cross into a new frontier.

System designers face a basic challenge: to deliver these new, voice-paging services as "additive" improvements. The added features should work in concert with existing alphanumeric systems, without necessitating a major overhaul or replacement of existing paging infrastructures. Achieving this goal requires giving close attention to the following critical design factors:

- an in-depth understanding of existing paging protocols and bandwidth limitations
- highly efficient voice-compression algorithms deliver acceptable levels of voice quality and quantity, despite tight bandwidth constraints
- cost-effective pager designs incorporate high-performance DSP capabilities and new user interfaces that support multimedia
- voice-paging server architecture can merge and leverage with the existing paging infrastructure, rather than replace or radically change it

"A Few Words" On Voice Paging

Voice paging is not about delivering long, complex voice messages, nor is it about providing fully interactive, two-way conversations. Those types of services are best accomplished by the cellular and PCS telephony systems. Voice paging effectively and reliably delivers short (2-to-20-seconds), tightly focused voice messages that clarify, expand, and amplify the alphanumeric content of a page. Two seconds of voice is considered a minimum requirement for adding a simple voice tag, such as the caller's name. The maximum length, 20 seconds, allows for reasonable information content.

Alphanumeric paging is being increasingly deployed as an effective way of delivering expanded content to mobile users. It requires that the sending party have access to a QUERTY keyboard to enter the message. Routine voice input via publicly switched telephony continues to be the simplest and most universally available communications option on the planet. A well-designed voice-paging network should act as a seamless bridge between the two systems, permitting users to make the most of each.

The first widespread global standard for paging was POCSAG (Post Office Code Standardization Advisory Group), which was adopted in 1981. It can support up to two million addresses per carrier using single-tone numeric or alphanumeric pagers. Although POCSAG still is the most widely deployed paging protocol, the de facto standard for new paging systems has become the FLEX protocol developed by Motorola.

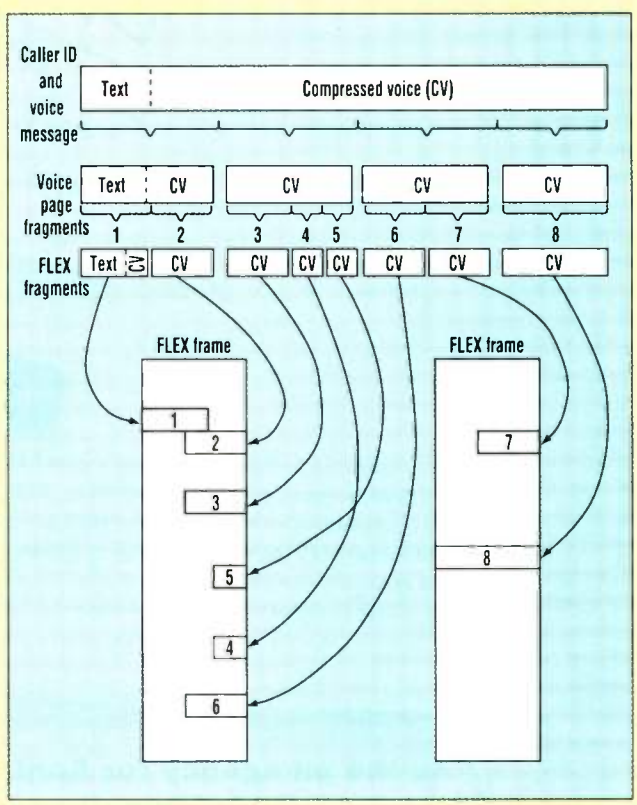
Developed in 1993, FLEX is a digital, synchronous-frame protocol. A FLEX system can effectively support up to five billion individual addresses and over 600,000 numeric pages per channel. All paging traffic is organized into fixed-frame data packets. The packets are transmitted in 128-frame cycles that last exactly four minutes per cycle. For each pager, FLEX schedules all message traffic into a predetermined time slot (or slots) in a specific data-frame buffer within the frame cycle.

By supplying a range of different service levels, FLEX gives greater deployment flexibility for pager-service providers. Service providers simply assign a pager more time slots on the 128-frame cycle, thereby reducing the overall system latency for that user.

The major difficulty in deploying voice content over a FLEX network is coherently segmenting the whole message. The message will then fit into a series of the FLEX protocol's very small frame buffers (consisting of 88 32-bit words per frame buffer). The longer the message content, the more fragmentation is required. This adds overhead and system latency in terms of additional frame headers, error correction steps, and processing time to both fragment and reassemble the message content.

During each transmit cycle, the fixed allocation, as well as the location of data slots for each pager, complicate the situation. Multiple messages may be concurrently queued for transmitting. Fragmented voice content will possibly have to be segmented over several discontinuous frame

(continued on page 70)



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ropolitan areas. Using Motorola's DataTAC protocol and multi-level FSK modulation, it provides comparable services and features, with data rates of up to 19.2 kbits/s. Mobile units uplink using the 806-to-825-MHz band, and receive over 851 to 870 MHz. The U.S. network of ARDIS/DataTAC services is currently operated by American Mobile Satellite Corp. (AMSC), with similar services provided in Canada by Bell Mobility. Both RAM and ARDIS services are available in other parts of the world (although sometimes on different frequencies) including Europe, Asia, and Australia.

Because of its higher data rates, larger file capacity, and real-time connectivity, mobile data is excellent for everything from handheld point-of-sale terminals to remote telemetry collection systems. Several players in the intelligent transportation system (ITS) movement have recently expressed great interest in using these mobile data technologies to provide connectivity for vehicular navigation, control, and security systems.

Several companies, like Research in Motion, Waterloo, Ontario, Canada, make a wide variety of mobile data devices for use in both DataTAC and Mobitex systems. Ranging from plug-in PCMCIA modules to credit card-sized transceivers and driver software, they can be easily embedded within your next handheld widget. Depending on the features and number of units, expect to pay $175 to $300 for an OEM transceiver. Development kits for both hardware, applications, and operating system software are designed to speed up the design cycle. Taking care of the basics allows engineers to concentrate on applications-related issues.

Looking to go wireless yourself? Consumers and mobile professionals can choose stand-alone, pocket-sized mobile message terminals or plug-and-play style PCMCIA cards that can transform any laptop into a fully connected mobile office. Price tags for these little wonders can run between $250 and $400, with pricing expected to slowly fall as demand increases.

Packet Data Over Cellular

While it hasn't caught on as quickly as predicted, cellular digital packet data (CDPD) is an excellent way to ship bits across the airwaves. CDPD is intended to leverage the unused bandwidth in much of the enormous installed base of analog cellular equipment available throughout North America. Packets are carried on a "space-available" basis, having been received over cellular channels that aren't carrying voice. They are then sandwiched into the wired backhaul between voice traffic.

Not all areas offer CDPD service yet, and roaming can be a bit tricky. Yet, things are improving quickly. If it's available in the region you need, CDPD's excellent range, coverage area, and high data rates (up to 19.2 kbits/s for an effective rate of 14.4 kbits/s after overhead) make it a smart choice for many tasks. If you're transferring a lot of large files, the flat-rate plans (typically around $55 per month for an unlimited number of packets) offered by most major carriers can help you realize tremendous savings.

2. The Novatel Minstrel CDPD modem adds wireless Internet access and messaging capabilities to a pocket organizer (a). Palmtop computers can also easily go wireless, using PCMCIA-based modems or embedded modules (b).

Much like their packet network counterparts, CDPD modems are available as general-purpose embeddable modules, or as specialized plug-and-play products that can add wireless capability to a laptop, palmtop, or PDA. Novatel Wireless, San Diego, Calif., for example, manufactures several such devices, including a 2-in.-by-4.75-in. CDPD card (costing $299) that behaves just like a standard-issue AT-bus modem. The card supports TCP/IP, PPP, UDP, and SLIP protocols, so many existing software applications can transition to a wireless environment without missing a beat.

A Glimpse At The Future

Novatel gets big points in the "geek toy" department for the Minstrel, a clever little product that can convert either a Palm Pilot organizer or IBM Workpad palmtop into a wireless communicator *(Fig. 2a)*. Both the Minstrel and the company's new CDPD-enabled, handheld PC *(Fig. 2b)*, called Contact, can exchange faxes and e-mail and browse the Internet almost exactly as though they were using a hard-wired POTS connection. External modems are also available to bring RAM, ARDIS, and CDPD services to nearly any laptop.

Take a close look at the neat little gadgets offered by RIM and Novatel. They may not be the whiz-bang communicator of the future, but they're a good first-order approximation of things to come. Besides, they're here today and they do many neat things that could make life easier, for busy engineers and civilians alike. Eventually, products will be designed for a world where wireless connectivity is as common as a laptop computer is today. Suddenly, catching up on your e-mail or shipping out a recently debugged piece of source code from the poolside doesn't seem so farfetched after all.

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Image Processing Boards Leverage PCI and Multimedia Technology

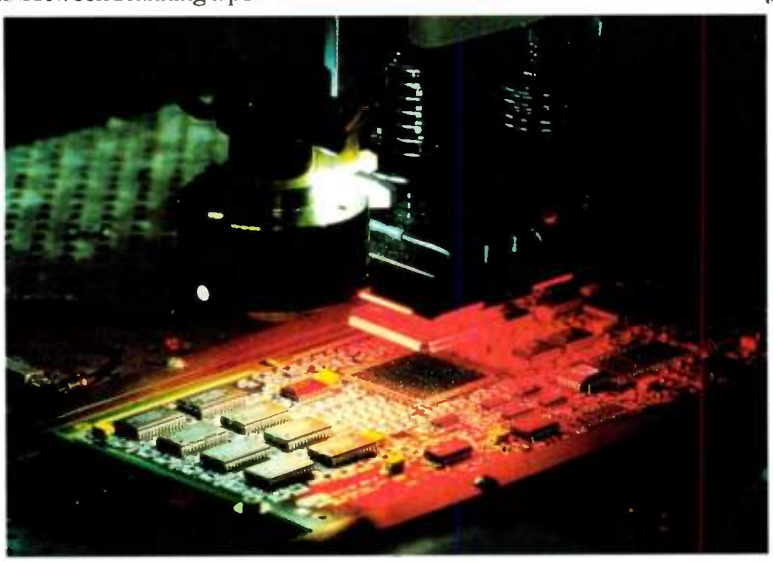
Cost And Performance Benefits Of PCI And MMX Are Pushing VME And Proprietary Designs Into Smaller Niches.

Jeff Child

SPECIAL REPORT

Image processing is still a board-level technology, and will continue to be for many years to come. That's because each individual application can be very different from the next. Applications span the gamut from bar-code readers, to automated printing inspection, to real-time medical imaging, to the imaging portion of military signal-processing systems. Even the differences between scanning a pencil and a pc board can be quite different *(see the opening illustration)*.

While large volume consumer markets can invest in chip-level imaging solutions for multimedia, the industrial and high-end imaging markets still thrive on board-level subsystems. This is changing slightly as the image-processing applications leverage technologies like Intel's Multimedia Instruction Set (MMX) on it's Pentium and latter processors *(see "MMX technology accelerates machine vision algorithms," p. 82)*.



Art Courtesy: Matrox

Because applications can vary so much, the bus architecture best suited to a particular application depends largely on the size of the problem. It's still a board-level game, and many high-end image-processing board makers are shifting to new processor and bus choices to improve their mix of computing muscle, bus bandwidth, and cost.

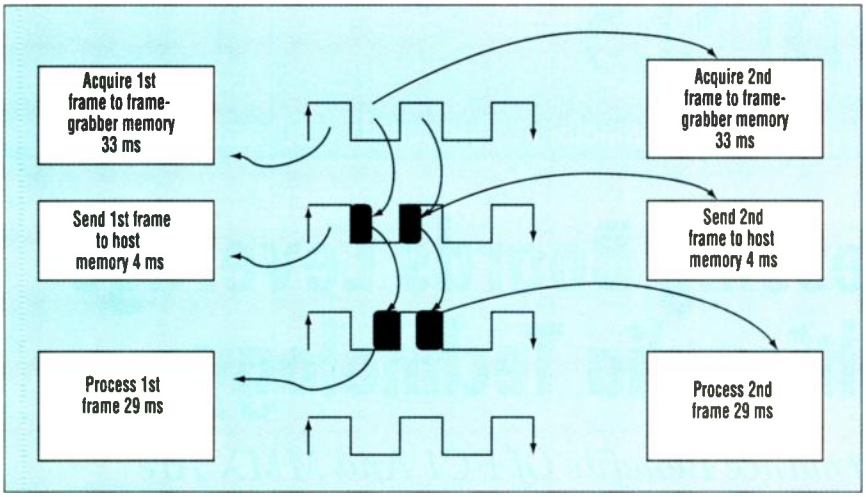
PCI Sweeps In

Perhaps the most sweeping technology shift in image processing is the move to the PCI bus. PCI offers a theoretical bandwidth up to 133 Mbytes/s. And, because PCI comes from the desktop PC world, the silicon for connecting to PCI is ubiquitous, inexpensive, and available in high volumes. As the performance and availability of PC-based image-processing products continue to increase, the gap between power and price will likewise shrink. This trend will lead many, if not most, image-processing applications to migrate away from the VME to the PCI bus. Image-capture and -data acquisition boards are among the newest class of specialty boards to embrace PCI.

The PCI bus is useful for imaging because it allows real-time transfer of an ample number of consecutive frames from the imaging board to the system memory. This has two benefits for system designers. First, on-board memory isn't required, since much less-expensive system RAM can be used. Second, with an imaging board acting as a PCI bus master, image data transfers to the CPU quickly, increasing overall processing time.

Along such lines, a number of imaging board makers, including Data Translation, Matrox, and Coreco, have moved into the PCI frame-grabber board business over the past few years. Thanks to the bandwidth of PCI, a system's host CPU can handle many of the image-processing functions. Some imaging applications, however, need more intelligence on the imaging board itself.

Even if PCI's full speed isn't exploited, it still has



1. The PCI bus offers considerable bandwidth between the frame grabber hardware and the host. According to Imaging Technology however, this doesn't mean you can eliminate the memory for the frame-grabber board. The diagram shows how on-board memory lets you send data in a single burst. The burst rate in this example is a mere 4 ms to send the entire frame to the host. That frees up 29 ms for processing.

benefits for imaging. You've got a bus that theoretically lets you transfer 132 Mbytes/s. When you implement something, you find that it's about 20 to 25 Mbytes/s. But that's still plenty for imaging. In monochrome imaging you're moving data in the neighborhood of 12 Mbytes/s. You get the information digitized and over to the host a lot faster than you could with the ISA bus.

Where's The Memory?

PCI also effects the cost of board-level imaging. Because the ISA bus had been too slow, board makers were forced to put memory and display controllers on their boards to acquire and display images in real time. With PCI, you have a bus that's fast enough so that you don't need to do that. You just send the information straight over the bus right to the memory of your PC or to your VGA display card.

Because you can do a real-time transfer over the PCI bus, you don't need any memory on the frame grabber. Yet, you still see frame grabbers with on-board memory that aren't really needed anymore. As the bus gets faster and the host gets smarter, a peripheral like a frame grabber doesn't have to have as much responsibility.

An important aspect for PCI image processing is bus mastering. PCI allows for burst mode transfers of all the data in a specific amount of time. To take advantage of this, it's important that the PCI imaging board has the capability to become a bus master. That way, it can control the bus and transfer the data when it needs to.

Without bus mastering, other peripherals on the PCI bus might tie the bus up. The burst mode tells the CPU to essentially sit back while the frame-grabber card takes over the bus to do the data transfer. If your imaging board isn't a bus master, the CPU has to oversee the transfer. That's an intensive task, so you're really wasting a lot of CPU time. Many vendors are moving to bus-matering PCI imaging boards.

While your PCI frame grabber is a bus master, the CPU can keep busy doing other tasks. As long as the frame grabber is a bus master, it can send the data over to a particular segment of memory, and the CPU can start working on that data, doing some image processing. Meanwhile, the frame-grabber can get the next set of data, and load it into yet another segment of memory while the CPU is actively doing work on the previous data *(Fig. 1)*.

Data Translation's latest PCI imaging product is the DT3152-LS line-scan frame grabber. As the newest member of the firm's MACH Series of PCI frame grabbers, it's an optimized version of the popular DT3152 variable-scan PCI frame grabber. The DT3152-LS interfaces to RS-170, NTSC, CCIR, PAL, variable-scan, and line-scan video, and accepts signals and RS-422 interfacing for DALSA, Loral/ Fairchild, and EG&G Reticon line-scan cameras.

The DT3152 variable-scan PCI frame grabber was designed for imaging applications requiring both accuracy and input flexibility. The board accepts four monochrome inputs. Its Fidelity front end delivers what the company claims is highly accurate image processing that's ideal for motion or time-lapse analysis.

The DT3152-LS provides users with access to the existing feature set of the DT3152 along with new line-scan functionality, making the board an ideal choice for applications where high-accuracy line-scan image capture is required. Specific applications that can take advantage of line-scan functionality include Web inspection, bar-code reading, topography, and a wide range of other moving/gauging type applications where line-scan cameras are commonly used.

Designers must be realistic about what can be done over the PCI bus. While many companies making PCI bus products quote numbers like 132 Mbytes/s for a burst-mode transfer, very few chip sets are available that actually support burst-mode transfers. To transfer information, you have to use a regular transfer mode, which consumes 100% of the bandwidth of the PCI bus.

System designers need close to that bandwidth to perform many of the operations required in many imaging applications. A simple operation like averaging can't be performed by the Pentium processor becuase it doesn't have enough throughput. That's one reason why you would want to put that kind of hardware onto the frame-grabber card itself. Other functions might be run-length encoded, which, with dedicated hardware, could be done in real time. Even something as simple as real-time image subtraction can't be done with the Pentium. In that case you'd need hardware on the frame-grabber or image-processing card.

A second reason for having more intelligence on the imaging board is to offload the host processor. In a process-control application, the host CPU is responsible for controlling other things in the external environment, like robot arms, solenoids, other measurement devices, data-acquisition devices and user interfaces. If the host is consumed with performing a convolution or edge-detection function on an image, it won't have time to be as responsive as it

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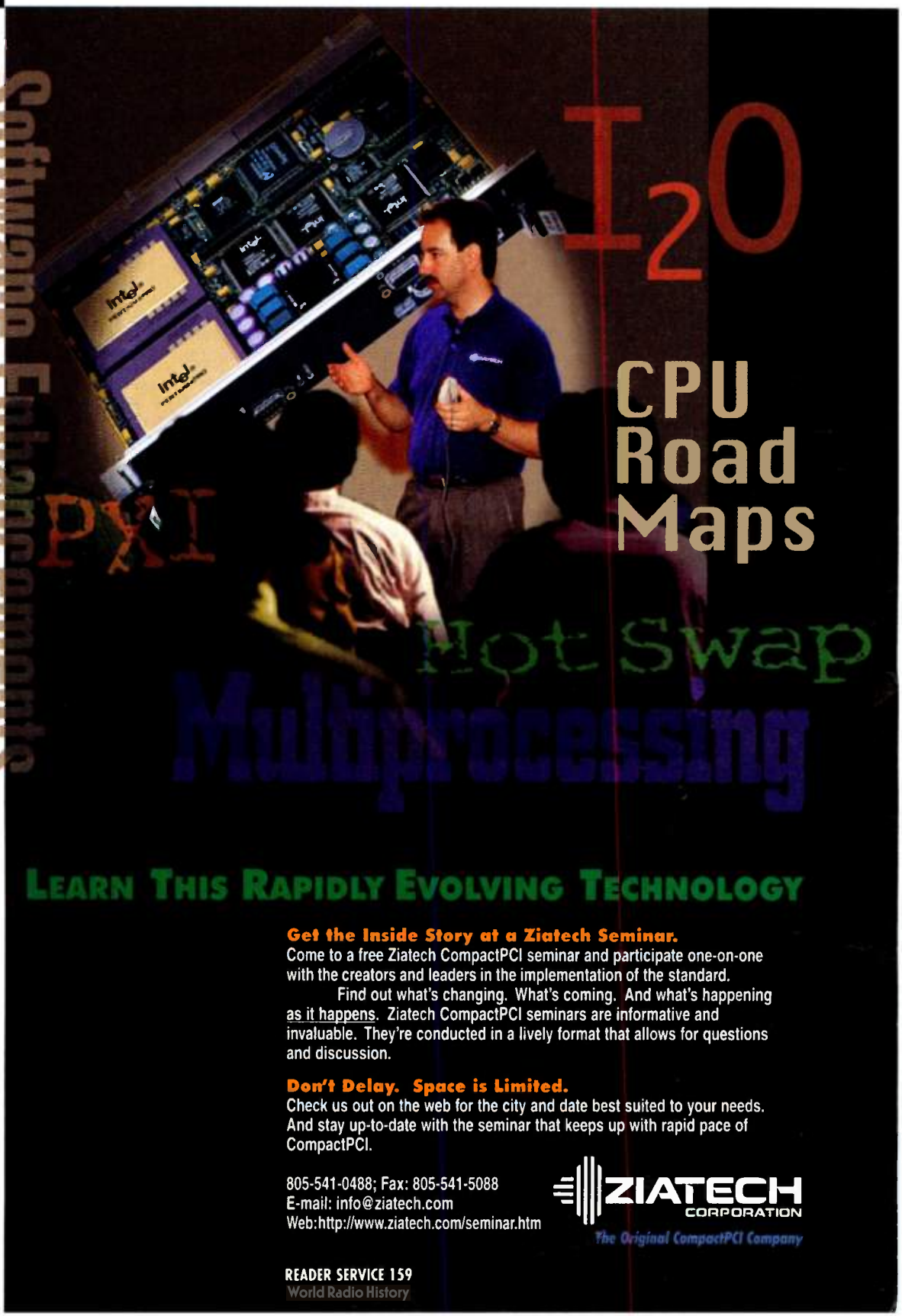

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should in those environments.

So far, Coreco is the only imaging-board vendor to embrace the TI C60 DSP chip. A color and monochrome image processor, the Cobra/C6, features the TI TMS320C620 IC. With six ALUs and two multiplier units, 64 kbytes of on-die cache memory and an integrated software language for parallel processing, the C60 can execute 1600 MIPS.

The heart of the Cobra/C6 architecture is the Image Gateway, an intelligent transfer controller custom-designed by Coreco to deliver high I/O throughput for multipass data transfers. Featuring seven I/O ports with a combined bandwidth of 1520 Mbytes/s, the Image Gateway can simultaneously interconnect any five ports for a maximum combined transfer rate of 720 Mbytes/s. It can move image data rapidly to other devices on the board, including the Pixel Processor (a proprietary processor used to accelerate point-to-point and neighborhood operations). The Cobra/C6 features a 200-Mbyte/s auxiliary bus known as the CAB to communicate image data to other processors, such as the Python/C6 multiDSP processor.

Matrox's Imaging Products Group is also expanding its offerings in PCI imaging. The Matrox Meteor-II provides standard acquisition capabilities from NTSC, PAL, RS-170 and CCIR sources. Targeted at cost-sensitive applications with no particular display requirements, this boardas well as others in the family can be used in conjunction with Matrox graphics accelerator cards for superior acquisition and display.

A second family member is called the Matrox Meteor-II Multi-Channel. It captures images from analog interlaced or progressive-frame-scanRGB cameras; two-channel (double-peed) analog progressive-frame-scan monochrome cameras; or multiple-standard (RS-170/CCIR) monochrome cameras. Hardware trigger support is available for asynchronous reset cameras used in inspection or other machine vision applications requiring synchronization to external events.

Matrox's Meteor-II Digital model lets users take advantage of the better image quality typically available when using digital cameras. Interfacing color/monochrome single- or multitap-output digital-frame or line- scan cameras to PCs is supported in an RS-422 format, and the newer EIA-644 LVDS standard being widely adopted by camera makers. An optional hardware module provides lossy or lossless motion JPEG compression/decompression for applications where storage space may be a concern, such as picture archiving and retrieving applications.

An integral component of the Matrox Meteor-II boards is the custom-designed Matrox Video Interface ASIC (VIA). This controller first appeared on the Matrox Genesis PCI image processor *(Fig. 2)*. It provides real-time image reconstruction and reformatting capabilities. For example, Matrox's VIA can take non-consecutive pixel data from time-multiplexed or multitap cameras and reconstruct the pixel data in memory in real-time.

Matrox's VIA PCI bus master interface lets any Matrox Meteor-II board achieve real-time transfers to display or system memory at up to 130 Mbytes/s for imaging. This controller also permits scatter-gather DMA op ation for more efficient use of syst memory. A VM Channel secondary interface, also under Matrox VIA c trol, provides an additional bidir tional data bus to off-board resour (other Matrox boards) without load down the PCI bus.

Additional design concerns, such PCI latency, are addressed with 2 t Mbytes of on-board memory. This eff tively eliminates the possible ima data loss in a system with many PCI vices competing for bus bandwid Other features include an RS-232 se interface and a power output.

Optimizing For Machine Vision

Frame grabbers made to display images usually have an on-board VGA adapter and mix the video and graphics together. They usually accept NTSC/PAL video in standard formats, without strobes and triggers. They have PCI bus interfaces, but the mer

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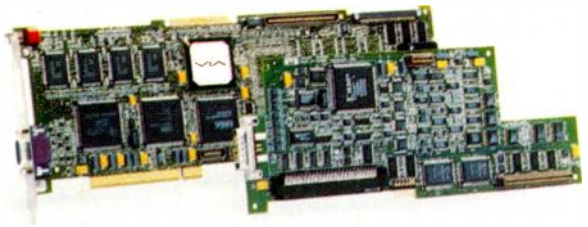
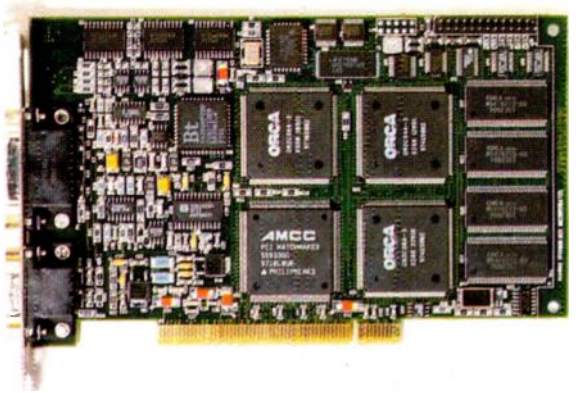


2. Matrox's Genesis-LC offers analog data acquisition at a rate of up to 140 MHz, up to 32 bits digital at up to 30 MHz, and frame or line scan input at up to 64k pixels per line and 64k lines. As many as 4 channels of data can be acquired at once. The board performs a sustained capture operation to the display and transfers data to system memory at a rate of over 100 Mbytes/s for simultaneous visualization and processing of data.



3. Designed specifically for machine vision applications, the PC Vision board from Imaging Technology sports 2 Mbytes of on-board VRAM for buffering image data between the camera and host PC system. This feature allows image transfers over the PCI bus 10 times faster than competitors' products, leading to simultaneous acquisition and processing of data. The on-board memory also assures that image information will not be lost during transfer to system memory.

ations, where the system is always waiting to get the next instruction or piece of data.

Pipelining has a further advantage in that it's deterministic. You know that a certain piece is doing a certain job at a certain time. As a result, it's a little easier to figure out how to build a pipeline that'll do a certain job within a certain time constraint.

Datacube's latest pilelined image-processing board is the mvPower-PCI. It combines a high-performance embedded CPU with Datacube's pipeline processing technology. The dedicated mvPower-PCI vision processor controls all machine-vision functions, including image acquisition, pyramiding, fast normalized correlation, metrology, morphology, blob analysis, projections, and pixel counting—all at the highest precision and speed levels available to the machine vision market today claims Datacube.

The full-length, single-slot PCI board combines specialized image-processing components and an embedded PowerPC 740 CPU. The mvPower-PCI has been designed to accommodate 300- and 166-MHz PowerPC 740 processors, and 500-MHz processors in the future. With an enhanced cache, these processors provide high-speed data access.

At a 40-MHz pipeline rate, image data can be pipelined directly to PowerPC memory and/or a VGA graphics card (across a VAFC interconnection). In addition, a 640-by-480-pixel image can be transferred directly from system memory across the PCI bus in less than 4 ms in the burst mode, with mvPower-PCI acting as a busmaster. The result is exceptionally-fast execution of all machine-vision algorithms and fast, direct image access.

In applications such as controlling a pick-and-place machine, the division of responsibility between the host CPU, motion-control cards, and mvPower-PCI enables greater system throughput. The host CPU can be dedicated to the operator's console and overall control, while the separate vision processor handles complex vision algorithms.

The mvPower-PCI is equipped with four of Datacube's custom image processing ASICs: an Arithmetic Unit (AU) and three Virtual Surface Image Memory (VSIM) modules. In addition to storing images in memory, VSIM memory is capable of carrying out certain important image-processing functions. The AU is a built-in arithmetic processor and crosspoint switch that's been fine-tuned specifically for image processing. The three image memories are 4 or 16 Mbytes each, for a total of up to 48 Mbytes. It has 16 Mbytes of DRAM for the CPU and utilizes the PC's VGA card's flash ROM (typically, 4 Mbytes).

For many advanced image-processing applications, you need more processing power than a single processor can provide. Even with the newer generation of DSPs and the multiple instruction-per-clock, and wide-word architecture, you're still limited in terms of what you can cram through. That's why many imaging applications need boards with multiple DSPs. This means you have to combine processing elements in a way that makes efficient use of communications and processor bandwidth. Still, the overall cost of DSP-based systems tends to be less because you're using commercially available chips.

Rather than make a tradeoff between the pipelined and the DSP-based approach, another option is a hybrid system. This architecture makes sense when, for example, you're dealing with an image that's 1k by 1k pixels, and within it, there's an object you want to analyze. For instance, you may want to decide if the object is square or round. In the hybrid system you can do preprocessing in a pipeline to identify the object. Then, only the pixel data that makes up that object is sent to the DSP side for analysis.

New DSP Choices

Among the makers of high-end DSP-based image-processing boards, there are many architectural twists. Many vendors are shifting to new processors, and new types of buses and interconnects. For years, Intel's i860 RISC processor was the engine of choice for processor-based advanced image processing. Companies like Alacron, Mercury Computers, CSPI, and Sky Computers, have long histories making i860-based accelerator VME cards, with 4, 8, and 16 processors per board.

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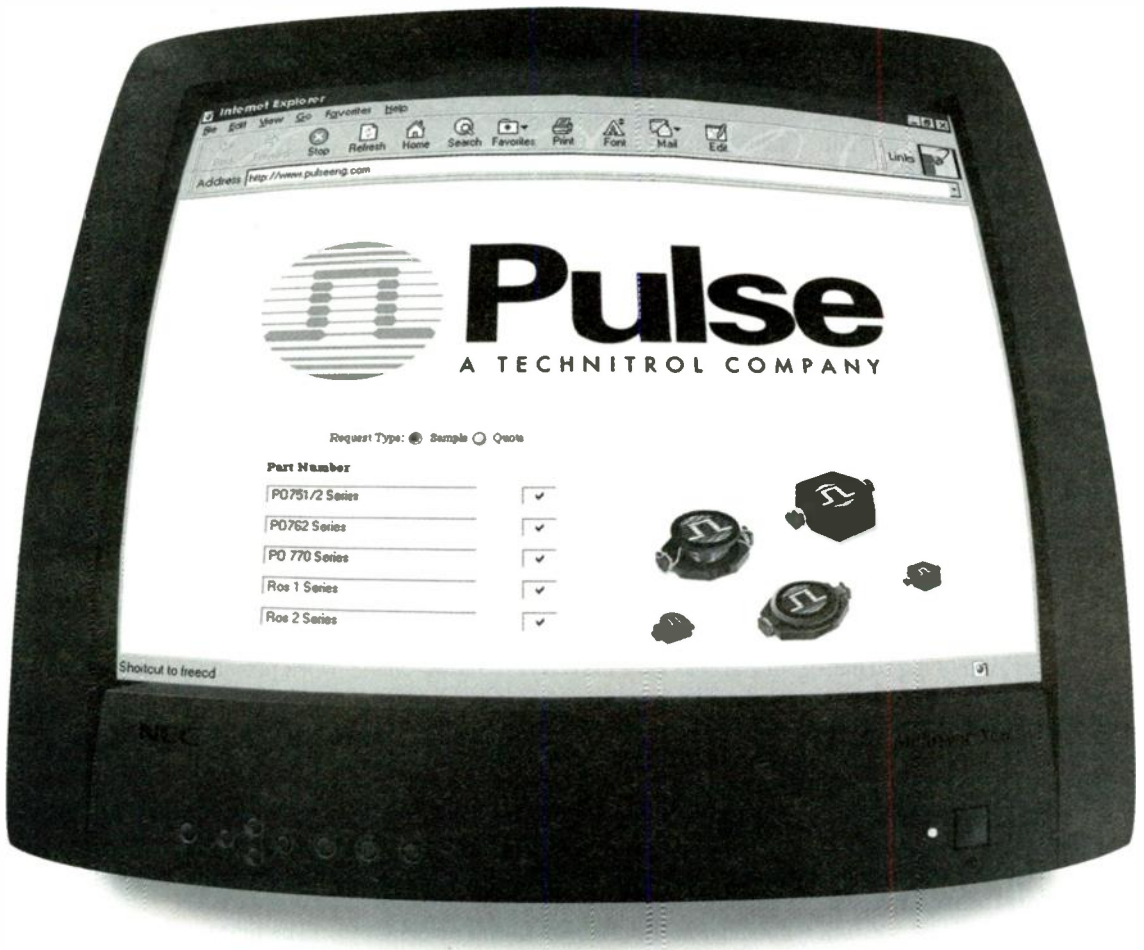

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Unfortunately, Intel has no plans to offer a follow-on to the nine-year-old i860 processor. The fact that there's not a long family of i860s planned will limit its design wins on new projects. That has pushed some i860-board makers toward newer DSP architectures like Analog Device's 21060 SHARC and Texas Instruments' TMS32C80. In some cases, the PowerPC 603 RISC chip is getting designed-in to work in concert with these newer DSPs. Even the TI C60 DSP, while designed for the telecom market, has been seeing some interest in the imaging world.

In general, the major DSP IC vendors have chip roadmaps heading in a direction different from what image-processing board makers require. DSP IC makers like Texas Instruments and Motorola are putting their efforts more into digital communications, hand-held assistants, and set-top boxes. Those aren't the types of processors needed to do medical imaging, radar or sonar.

Mercury Computers is among those embracing a SHARC/ PowerPC combo architecture: together, they fill the gap left by the i860. They're moving to handling the DSP-intensive parts of an application with a SHARC and the RISC-intensive parts with a PowerPC 603, 603e, and 604.

For its part, CSPI has also moved to the SHARC. The SHARC DSP has a set of link ports, which allow it to communicate with several other SHARCs. CSPI's MAP series boards let the link ports interconnect in a cluster. This allows you to write an algorithm where the SHARCs share data with one another, but everything comes in and out through the traditional I/O channels. Users can access these link ports in multiple boards. If the algorithm and data flow require more than eight processors, they can go up to 16 and share data that way.

The MAP-1310 and MAP-1311 multiprocessors deliver a robust, high-performance DSP/RISC platform to implement real-time, floating-point intensive processing solutions. These 6U VME products combine PMC-based SHARC TM 21060 processors with the 603 PowerPC. The 1310 offers four clustered SHARC processors and space for a third-party PMC I/O or graphics board.

The 1311 delivers the processing power with eight SHARCs. These combinations achieve synergy from the SHARC's high-MFLOPS/Power Density ratio and the versatile general-purpose PowerPC. While the SHARC chips provide the DSP speed, the PowerPC provides system-level and cluster-management services. The PMC format allows you to create flexible system solutions with available third-party PMC modules.

Continuing to exploit the PowerPC architecture, last fall Sky Computers announced its 2-GFLOPS Excalibur multiprocessor daughtercard. Excalibur's card is based on the new PowerPC 740 microprocessor, the third generation of PowerPC processors. Each Excalibur card includes four PowerPC 740 microprocessors and up to 256 Mbytes of DRAM.

A single Excalibur card on a 6U VME motherboard delivers 2 Gflops of performance. Four Excaliburs on a 9U VME motherboard deliver 8 GFLOPS, with total performance in a single VME chassis of a record-breaking 128 GFLOPS. The key to accessing this superior processing performance is the PowerPC 740 microprocessor's memory access rate of 83.3 MHz at 64-bits wide. The combination of 2 GFLOPS and 2.66 Gbytes/s makes The Excalibur daughter card ideal for very demanding image and signal-processing applications, such as radar, sonar, medical imaging, and image analysis.

A prime advantage of the Excalibur card is its fast access to large amounts of memory at three levels. Each PowerPC microprocessor is coupled to its own bank of 32-or 64-Mbytes of SDRAM that's accessed over the processor's memory bus at 667 Mbytes/s. Memory from other processors can be accessed over the daughtercard at the same 667-Mbyte/s bus. Global memory and memory on other compute daughtercards is accessible through the 320-Mbyte/s SKYchannel interface.

Sky Computer chose the PowerPC 740 microprocessor because of its 83.3-MHz external bus. This feature is more critical to overall application performance than the processor clock speed, says Richard Jaenicke, director of marketing. Ever-increasing clock speeds can cause high-performance applications to become memory-bandwidth limited. Older designs that connect a 66-MHz external bus to ordinary page-mode DRAM, or EDO DRAM, will have one or more wait-states bringing the effective access rate down to 33 MHz or less. Sky's SDRAM design at 83.3 MHz represents a significant advance in overall performance.

For it's part, Alacron has also embraced the SHARC with it's FT-Dominator FT-2106x Series. The FT-Dominators are commercial off-the-shelf systems intended for use in distributed, compute-intensive, high-data-rate applications in both the commercial and military domains.

The FT-Dominator series provides a very high degree of scalability. Internally, each FT-Dominator supports from 1 to 96 ADSP-2106x SHARC processors. A single FT-Dominator may be employed as a PCI or VME accelerator in a desktop workstation, while multiple 6U and 9U VME FT-Dominators may serve as compute nodes in a high-performance server or distributed system.

The first product in the FT-Dominator series provides both VME64 and PMC interfaces. Through the FT-Dominator's PMC interface, the SHARCs can DMA directly to Myrinet, a network providing full-duplex communication in excess of 1 Gbit/s, which is ten times the speed of fast Ethernet. Alacron's FT-Dominators can be employed in in-cabinet clusters connected by a Myrinet System-Area Network (SAN) or serve as compute nodes in large distributed systems connected by a Myrinet LAN.

The first product in the FT-Dominator series is a scalable array of up to 8 SHARC processors, interconnected using Alacron's Dual Ported Local Memory (DPLM) architecture. The DPLM design eliminates processor contention for off-chip memory, allowing the memory bandwidth of the SHARC array to scale linearly with the number of SHARC processors. A two-dimensional DMA engine isolates the SHARC array from the system bus, shielding it from the impact of system bus traffic, while doing data movement and scatter gather operations.

Still despite the fact that PCI-based boards have become entrenched in the off-the-shelf image-processing market, VME-based boards continue to hold sway in many applications. The tried and true VME bus continues to offer high-end designers the greatest flexibility in I/O options, processors, scalability, and performance.

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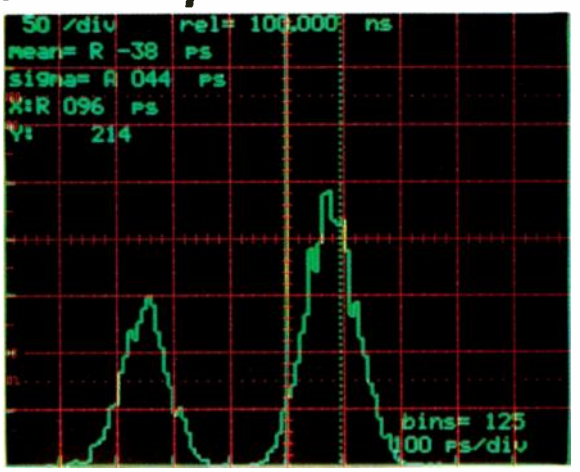

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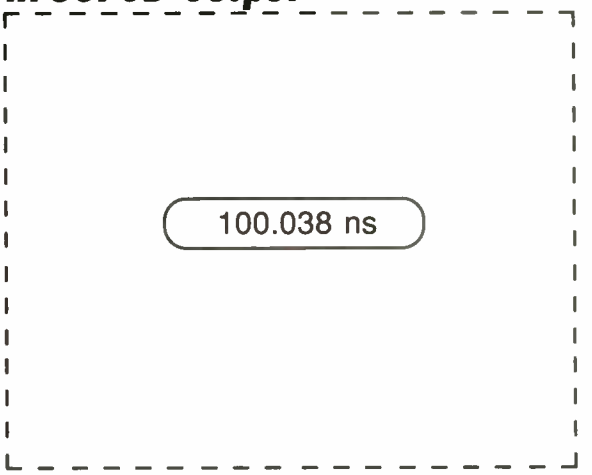

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Disk-Drive Chip Pushes Integration Barriers

HDD Chip Set Hits Milestone By Combining Read-Channel Logic, A Disk Controller, And An Open-Architecture Processor.

Jeff Child

Disk-drive electronics have always ridden the leading edge of mixed-signal semiconductor integration. The pressure to shrink costs and size, particularly in the sub-$1000 and mobile-PC markets, drives the demand for lower-chip-count solutions.

Along such lines, Cirrus Logic, Fremont, Calif., has announced a hard-disk-drive (HDD) chip set that boasts two firsts. Called the CL-SH8665, it's the first product to integrate a microcontroller, ATA disk controller, and read channel on one chip. And, it's the first to use an open architecture processor, the ARM, as the microcontroller. That milestone may have implications that go beyond the traditional PC market.

Cirrus Logic is currently the leading supplier of disk-drive chips, having shipped over 30-million HDD read channels in 1997. Dataquest forecasts the desktop HDD market to grow from 120-million units in 1998 to 190-million units by 2001.

Pieces Of The Puzzle

The CL-SH8665 combines a number of Cirrus Logic's building blocks. These include a partial-response-maximum-likelihood (PRML) read channel for reliable data acquisition, an Ultra DMA33 disk controller for high-speed data transfers, and an ARM 32-bit processor core to handle both system and servo control functions *(see the figure)*. Because the chip already integrates servo logic into its disk controller, and the ARM processor includes program memory, the only system functions needed to create a complete HDD design are the preamp, motor drivers, and buffer memory.

By using an open processor architecture from ARM Ltd., Cambridge, U.K., Cirrus Logic hopes to introduce an open programming environment and a new supplier choice in mass storage. The controller on disk drives has traditionally been a proprietary microcontroller or digital signal processor. An ARM-based chip solution allows drive makers to select from most major semiconductor suppliers, rather than a single source or closed technology.

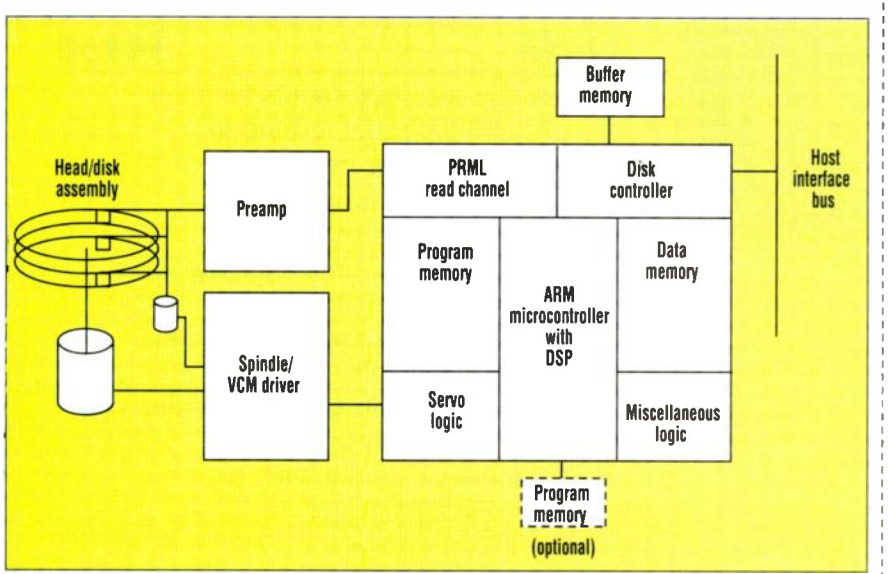
HDD firmware can entail a multimillion-dollar development effort—and ARM protects that investment, while offering unmatched opportunities for HDD OEMs to leverage their designs long term. The open ARM architecture has been embraced by 29 licensees worldwide, including most of the major semiconductor suppliers to the mass-storage market.

The ARM 32-bit RISC core processor offers sufficient performance to take on both the microcontroller and servo control functions in HDD designs. The core dissipates very little power, and fits within a small die size.

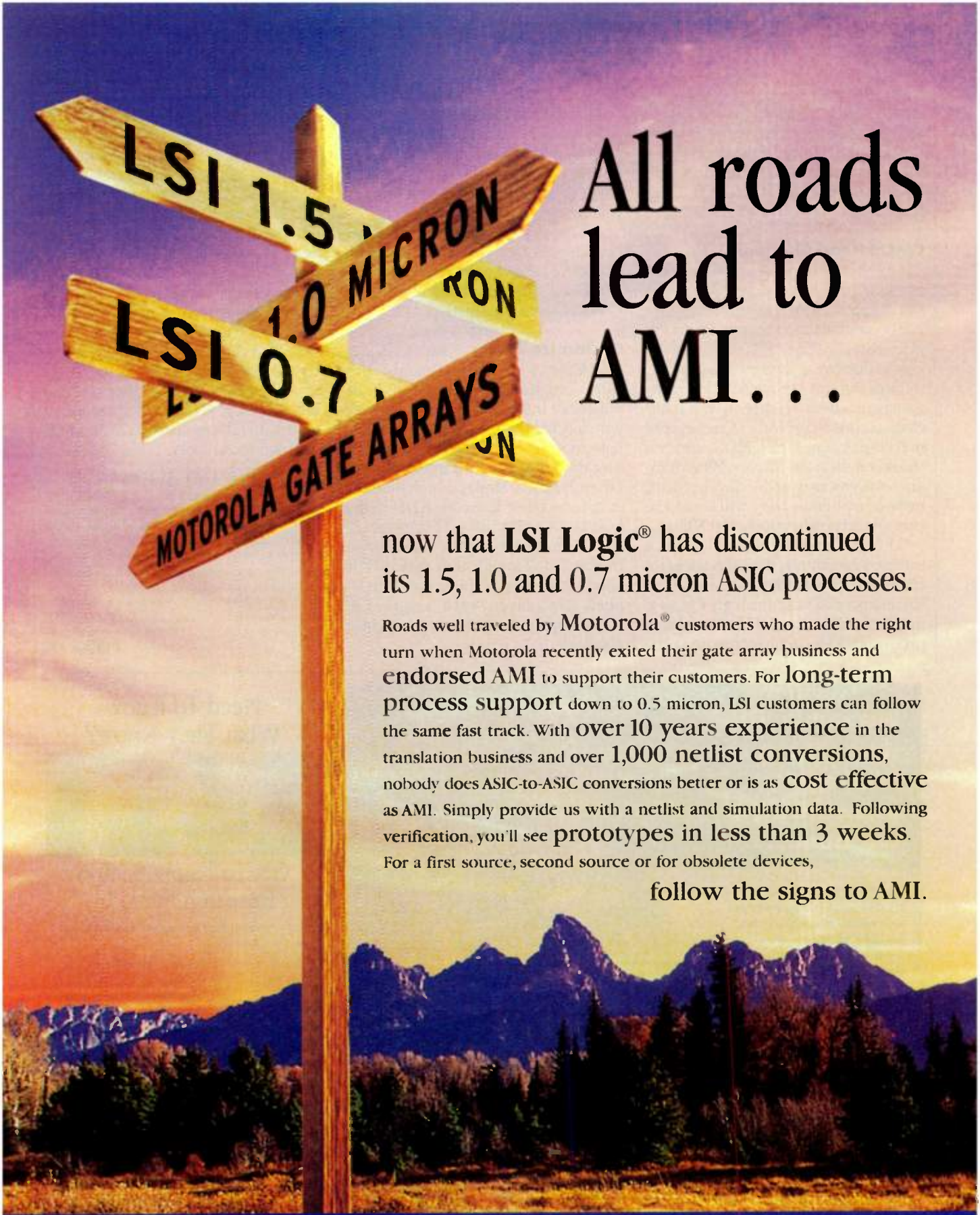
In addition to offering an optimized hardware solution, ARM provides very efficient software and code development. For example, to minimize memory size and overall system cost, ARM increases code density by automatically compressing frequently used system instructions from 32- to 16-bits. Meanwhile, ARM's C-Language compiler generates efficient code, reducing firmware code development time (compared to writing in assembly language).

Combining the ARM Thumb core with the micro-DSP assist logic provides enough bandwidth to manage servo and spindle control, as well as disk controller and other drive functions. The ARM Thumb architecture allows 16-bit instructions to execute within the 32-bit processor core, reducing the firmware code size with no penalty in performance. For critical functions, such as servo processing or interrupt handling, 32-bit instructions can be employed.

A high-speed, 16-bit external bus is



The CL-SH8665 integrates an ARM microcontroller, PRML read channel, and an ATA disk controller. The chip needs only flash memory, EDO DRAM buffer memory, a preamplifier, and a power driver to make up the complete drive electronics for an ATA disk drive.



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used to fetch instructions from flash memory. Data memory can be accessed through the internal SRAM, or by using a portion of the buffer memory with direct processor access via the disk controller.

CMOS Read Channel

CL-SH8665's read-channel core is manufactured in standard CMOS. Cirrus Logic's PRML technology lets HDD manufacturers increase a drive's platter storage capacity, thereby reducing the number of platters. This, in turn, reduces the cost per-megabyte of next-generation desktop drives. The read-channel core is currently manufactured in 0.35-µm standard CMOS, and can transfer data at 300 Mbits/s. When 0.25-µm solutions, now under development, become available, they will boost the core's data transfer rate to 500 Mbits/s.

The chip's read-channel logic is a sampled-amplitude, digital read/write channel that provides a flexible, synchronous read path for high-density, magnetic disk drives. This block has a programmable architecture and calibration feature that allows the channel parameters be tuned to characteristics of each drive, head, and zone. High disk-drive rates—up to 245 Mbits/s along the read channel—and erasure pointers are supported.

An on-chip frequency synthesizer provides all of the clock frequencies required for three system power modes. Automatic clock disabling of idle subsystems saves even more power.

Customize Away

A Cirrus Logic HDD controller core is integrated into the CL-SH8665 platform, but can be easily replaced with a drive OEM's custom controller, if desired. The Cirrus Logic HDD core contains an ATA-4 host interface with Ultra DMA33 Mode, which enables data to be burst from the HDD to the host at 33.3 Mbytes/s. This interface lets the host CPU retrieve data faster, freeing it to handle other tasks while eliminating the performance bottleneck associated with sequential streaming applications, such as video playback.

The hard-disk controller logic offers full hardware support of the ID-less architecture, including automatic sector-pulse generation, logical sector mapping, and on-track defect management. Buffer bandwidth using EDO DRAM of up to 64 Mbytes/s can sustain host data rates of 33.3 Mbytes/s in Ultra DMA mode 2, and disk data rates up to 260 Mbits/s.

Advanced error-correction-code (ECC) logic provides 5-byte error correction, and can correct a single-burst error of 113 bits, or a double-burst error of 49-bits on the fly. Designers can achieve more ECC capability using off-line firmware correction and erasure pointer support.

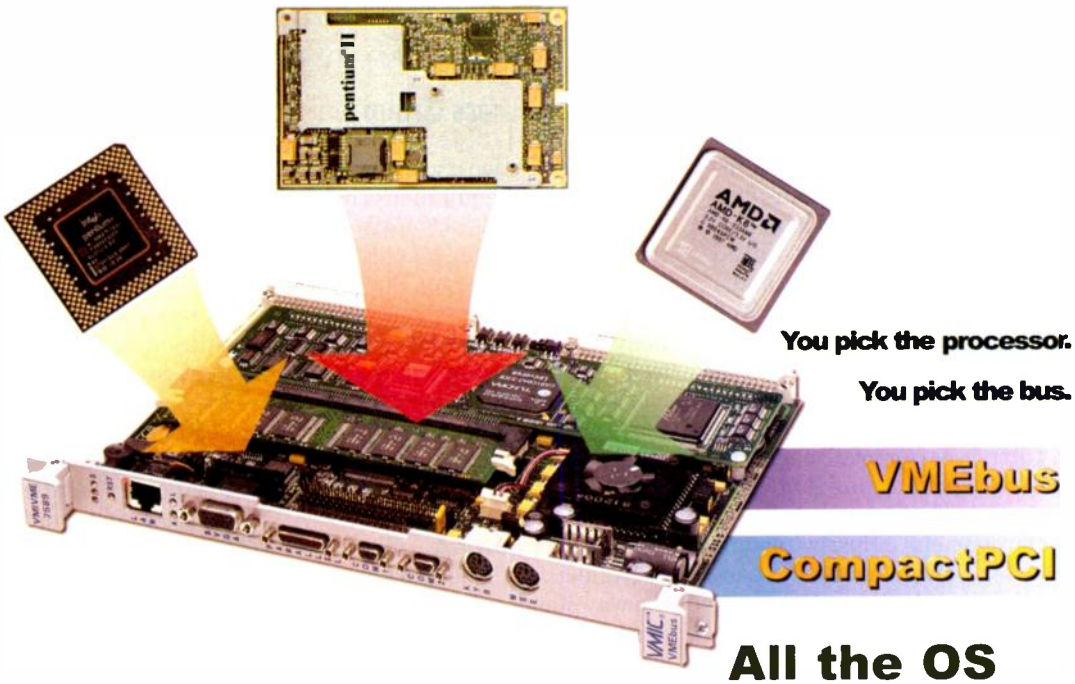
Pricing and Availability

The first product in the CL-SH8665 platform is implemented in a 0.35-mm, 3.3-V CMOS process. Scheduled to sample in the third quarter of 1998 in 208-pin LQFP packages, the device will be available in volume quantities by early in the fourth quarter at $15 each in quantities of 100,000.

Cirrus Logic Inc., 3100 West Warren Ave., Fremont, CA, 94538; (510) 226-2001; www.cirrus.com.

CIRCLE 495

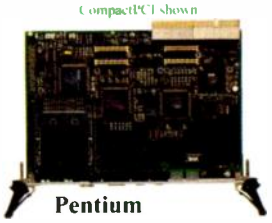
Get the Embedded Computer you want.



Select the Processor that is RIGHT for you.

200-333 MHz

CompactPCI shown



Pentium
Pentium Pro
Pentium MMX
Pentium II

Pentium® is Intel's cornerstone processor for high-speed, performance-based computing.

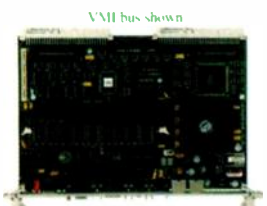
The **Pentium Pro** processors were designed to significantly exceed the performance of the 200 MHz Pentium processor using the same die geometry. Test results measure a 33 percent faster clock speed than a Pentium processor.

The **Pentium MMX™** class of processors offers 200 to 233 MHz of speed. A Pentium MMX-equipped processor (Megahertz-for-Megahertz) is up to 20 percent faster than a Pentium non-MMX processor.

Pentium II processor family speeds range from 233 to 333 MHz. The Pentium II processor family's significant performance improvement over previous Intel-architecture processors is based on the seamless combination of the P6 microarchitecture and Intel MMX media enhancement technology.

233-300 MHz

VME bus shown



AMD-K6

The new **AMD-K6** offers 233 to 300 MHz of speed. This is AMD's sixth generation of providing high performance at an affordable price.

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READER SERVICE 157

STANDARDS WATCH

CompactPCI Thrives In The Outsourcing Era

Joe Pavlat, PCI Industrial Computer Manufacturers Group

CompactPCI is becoming an increasingly popular system-platform choice. It combines modularity, ruggedness, low-radiated emissions, relatively low cost, and a wide range of available CPUs, as well as the operating systems that run on them. High I/O density greatly enhances the flexibility of applications. Emerging hot-swap abilities are particularly attractive for critical telecom and datacom applications that can't tolerate long down times.

The march in our industry toward faster, better, newer, and less-expensive solutions is relentless. However, three additional forces also affect CompactPCI's popularity: outsourcing, open standards, and the evolution of those standards.

Outsourcing

The effort to dramatically reduce product development, time-to-market, and cost is often driven by narrow market windows for new-product features. The PC market has thrived for years in that environment, but it's relatively new to the telecom world. Companies are thus concentrating on core competencies, buying what they can rather than building their own.

Today's fast PCI circuitry—the backbone of virtually all high-performance computing—is more difficult to design than older TTL technology. PCI's controlled impedance and transmission-line characteristics, coupled with the need to perform prelayout and post-layout simulations, lead many engineers and project managers to buy rather than build. And, 100-MHz, front-side, processor-to-memory buses are not for the faint of heart.

Open Standards

The urge to outsource moves equipment builders to insist on open architectures, like CompactPCI. They are not controlled by a single supplier. Use of standards improves interoperability and increases the number of available suppliers, which, in turn, promotes competition and lowers prices.

By building equipment that uses an open architecture, OEM's can concentrate on the features of the boards and systems they buy. Simply, they don't have to worry about the potentially negative consequences of being tied to a single supplier. Again, this has been a given in the PC market for a long time, but it's relatively new for much of the industrial and telecom markets.

Standards Setting

Reflecting these market trends, the way standards are developed and presented is also changing significantly. Historically, computer standards emerged from organizations like ANSI or the IEEE. They provided a stable, open process that generally ensured a balance between supplier and user interests. But the processes are slow. Typically, individual companies with vision developed open specifications, and then gave them up to the world—through a standards organization. That's how it worked with Hewlett-Packard and GPIB (HP-IB), Intel and Multibus, IBM and ISA, etc.

Today, dominant technologies usually come from industry consortia comprising industry experts in a particular area. Examples include the PCI Industrial Computer Manufacturers Group (PICMG); the PCI Special Interest Group (PCI SIG), which maintains the core PCI specification; the I2O SIG; the Enterprise Computer Telephony Forum (ECTF); and the protocol engineering and development arm of the Internet, the Internet Engineering Task Force (IETF). Such bodies generally stay focused on a technology, and tend to work quickly.

Industry consortia are proving to be better at advancing new technologies. Their specifications form critical mass during the process of development, or they aren't completed. They also tend to quickly stabilize a technology by proliferating it in the market. This has the added benefit of focusing the technology on real-world problems. In a broader sense, they reflect the "eat or be eaten" nature of today's computer marketplace.

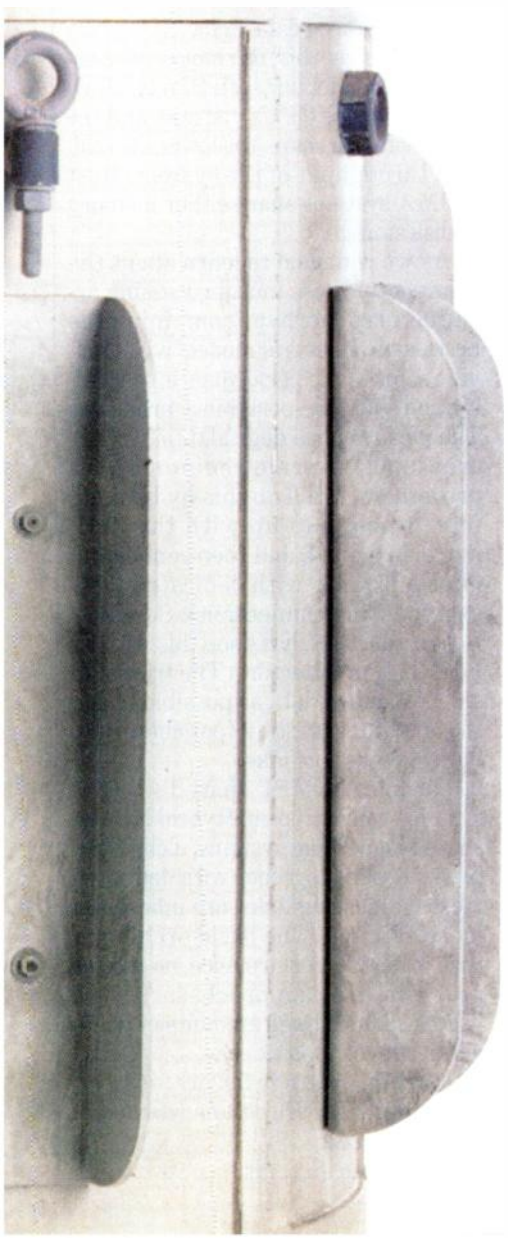
The continuing move toward shorter development times (which sparked the outsourcing trend) could easily double or triple the size of the embedded, non-desktop market for boards and systems within five years. As equipment builders buy more of their solutions on the open market, architectures like PCI and CompactPCI, developed by fast moving industry consortia will play a dominant role.

PICMG was formed in 1994 to develop open standards that apply PCI technology to non-desktop applications like telecommunications and industrial control. It developed the Passive Backplane PCI-ISA specification in 1994 and the CompactPCI specification in 1995. PICMG has more than 380 members and affiliates operating in Europe, Japan, and China. The group is now focusing on extensions such as the recently released CompactPCI Computer Telephony Specification, and the soon-to-be-released CompactPCI Hot Swap spec *(ELECTRONIC DESIGN, May 13, 1998, p. 109)*. Due for release later this year, revision 3.0 will make hot swapping a fundamental part of the core specification, and define a number of important I/O definitions and extensions.

PICMG has been working with the Enterprise Computer Telephony Forum (ECTF) to craft a version of the H.100 telephony bus specification for CompactPCI. Version H.110 will run across the upper connectors on a 6U CompactPCI card, and put the voice bus on the backplane. Under the leadership of Lucent Technologies' Steve Hall, the group has done extensive, detailed backplane simulations to define the specification. This standard is expected to cause the first real step function of volume shipments of CompactPCI cards, because it will let computer telephony board vendors start making compatible boards.

Joe Pavlat is director of strategic planning for the Motorola Computer Group and president of PICMG. He can be reached at (408) 646-3511; fax (408) 646-3520; e-mail: Joe_Pavlat@mcg.mot.com.

Crank up the Amps!



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READER SERVICE 120

No Free Lunch In Multiprocessing

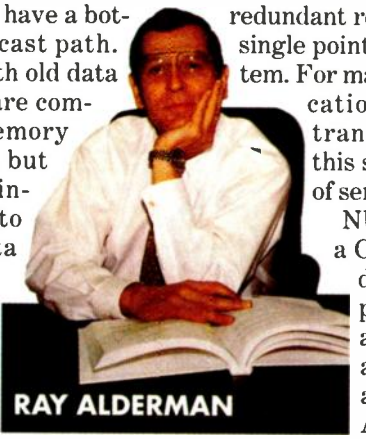
There are millions of applications for single-processor computers in both the embedded and commercial markets. Many sophisticated applications could benefit from a multiprocessor architecture. But, when we start hooking processors together, we open a large can of worms. New performance/scalability trade-offs, increased hardware/software complexities, and higher costs are only a few of the wriggly creatures that come crawling out.

Depending on the resources that the CPUs share, multiprocessing architectures fall into three basic classes: shared everything, shared nothing, and shared something. However, the way these resources are shared between processors further complicates matters.

In a purist example of shared-everything architectures, multiple processor cards on a bus share memory resources, communications channels, and I/O interfaces. In this symmetrical multiprocessing (SMP) model, each CPU arbitrates for the common shared path (the bus), and completes its transactions. Then, the next CPU controls the bus for a period. Increasing CPUs on the bus raises system performance to a point. But SMP systems don't scale well above four CPUs, due to the contention for bus mastership.

Processors in an SMP system typically share one copy of the operating system. The main drawbacks to SMP, besides limited scalability, are the many "single points of failure" that exist with so many shared resources. The benefit of SMP is that application code can run on any CPU in the system without software changes.

To eliminate the contention problem, you could install a broadcast mechanism or reflective memory. Here, all CPUs have their own pool of resources, but share a specific memory block. If any CPU changes the values of the shared memory, that data is sent to all the CPUs. That is, memory changes are reflected to the other CPUs. This scheme is very efficient because all transactions are writes. But when all the CPUs try to change the shared data, you'll have a bottleneck on the broadcast path. Every CPU works with old data until all the updates are completed. Reflective memory systems are scalable, but true performance is inversely proportional to the amount of data shared.


RAY ALDERMAN

Massively parallel processing (MPP) is a shining example of a shared-nothing architecture. Each CPU has its own resources (memory, OS code, I/O channels, etc), and communicates with other processors through dedicated connections. The Transputer architecture using DS-Links for interprocessor communications (IPC) is the model for shared-nothing systems.

MPP is highly scalable, but it introduces tremendous software complexity: parallelizing the application code. The message-passing interface between the many CPU's slows things down to a snail's pace compared to SMP. While the aggregate performance of an MPP system is huge, the realized performance is inversely proportional to the number of processors sharing data. This behavior simply proves The Great Multiprocessing Paradox: There are no free lunches in multiprocessor architectures.

The shared-something category includes three models: networked processors; clustered processors; and nonuniform memory-access architectures (NUMA). The networked-processor model looks a lot like SMP, except that the shared path is the network connection. Each node has its own hardware resources and copy of the operating system like the MPP shared-nothing systems.

Clustering, on the other hand, is quite similar to MPP. Each computer has its own resource pool, and communicates with the other CPUs through a dedicated channel. This architecture is used mostly in critical applications. If one CPU fails, another in the cluster takes over the applications that were lost. Clustering is expensive because it employs many redundant resources to avoid any single point of failure in the system. For many commercial applications, such as on-line transaction processing, this structure makes a lot of sense.

NUMA means that when a CPU wants a copy of data shared between processors at a specific address, the data could actually be at another address in the system. An elaborate set of memory directory chips and software scattered throughout the system translates all the addresses until the system finds the desired data. Some NUMA architectures use this "directory-cache-coherence" model very effectively. However, the more CPUs you add, and the more data you share, the lower the realized throughput of the system. Most NUMA systems share either memory or disk storage.

As we continue to learn about the behavior of these multiprocessing architectures, perhaps combining the best parts of several models will eliminate some of the performance, scalability, and software-portability problems. The performance degradation will decrease as we scale the number of processors. We'll do this by hooking four processors up with the SMP model in a quad, and then connecting multiple quads with dedicated message-passing connections. Sequent, Beaverton, Ore., has done this with its NUMA-Q architecture. The trick is to share as much data as possible inside the quad, and as little as possible on the message-passing links.

Ultimately, MPP shared-nothing systems will disappear. Hybrid NUMA shared-something systems, using SMP blocks hooked together with dedicated message-passing links, are inherently more efficient. The basic problem is that reads kill performance, no matter how you link the processors. And writes require huge amounts of bandwidth to avoid bottlenecks.

Ray Alderman is the executive director of VITA. He can be reached at exec@vita.com.

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WHAT'S ON BOARD

With cycle times as quick as 3.3 ns, the CXK77B series of 4-Mbit late-write synchronous SRAMs from Sony Semiconductor Company of America, San Jose, Calif., are among the fastest commercially available SRAMs. The memories can operate at system clock speeds of up to 300 MHz, which is about 27% faster than the 4-Mbit devices the company released last year. The new chips are well-suited for use in workstations, mainframes, and high-throughput buffer applications in network routers, hubs, and backbone switches. The late-write devices make data available one clock cycle after the address and control signals switch, thus eliminating the need for a bus-turn-around cycle when changing from a read to a write operation. Input registers, output registers/latches, and a one-deep write buffer are all included in the memories, as well as four programmable operating modes to optimize system performance. Several version are available—the CXK77B3640AGB and 77B1840AGB have HSTL input/output levels, while the 77B3641AGB and 77B1841AGB are LVTTL/LVCMOS compatible. The 77B3640AGB/3641AGB are configured as 128 kwords by 36 bits, while the 77B1840AGB/1841AGB are organized as 256 kwords by 18 bits. All versions come in 119-contact plastic BGA packages and operate from a 3.3-V supply. Samples are immediately available. The devices cost approximately $100 each in 1000-unit lots. Contact Sony at (408) 955-6572 or go to www.sony.com/semi.

Able to provide either 10- or 100-Mbit Ethernet connectivity at one quarter the power drain of its predecessor, the 82559 Ethernet controller from Intel Corp., Santa Clara, Calif., also reduces the board space required for the network interface by 75%. Housed in a 15-by-15-mm BGA package that is just 1.56-mm thick, the Ethernet controller chip consumes less than 125 mA when active. In sleep mode, it drops the current drain to just 5 mA. The device uses a 3.3-V supply. The low power drain and small size make the chip well-suited for mobile applications and adapter cards, as well as for use in servers and various desktop platforms. As an enhanced version of the company's previously released 82558, the chip takes advantage of available driver software, thus simplifying network support across multiple generations of controllers. Additional features include the Alert-on-LAN capability, which allows the 82559 to notify the host when there is a chassis intrusion, even if the main system is turned off. The ACPI and Wake-on-LAN provide power management support and the ability to wake-up the host system when pertinent LAN activity occurs. The Alert-on-LAN features, which previously required a separate chip, are compatible with the Wired-For-Management 1.1 specification for desktop systems. Samples of the 82559 are immediately available. In lots of 10,000 units, the controller will sell for less than $20 each. Contact Intel at (503) 264-6223, or go to www.intel.com.

Providing DVD playback support for the Intel i740 graphics processor, the EM8220 REALmagic DVD chip from Sigma Designs Inc., Fremont, Calif., also includes a VMI 1.4 interface. Part of the reference design for boards based on the i740 processor, the EM8220 supplies virtually all the functions of a DVD decoder on a single chip. It combines the bidirectional VMI 1.4 interface, an MPEG-2 decoder, and a video scaler with bilinear interpolation filtering in both X and Y directions. By using the VMI interface, DVD data and video can be passed to the graphics controller without loading the PCI bus in the host. The EM8220 performs all MPEG decompression in both PAL and NTSC modes. Video-frame-rate conversion is done with only 2 Mbytes of memory. A built-in S/PDIF encoder can turn a PC into a full-featured home-theater DVD player that fully exploits the digital video and surround capabilities of DVD. Samples of the EM8220 are immediately available, and sell for $35 each in small quantities. Contact Sigma at (510) 770-0100, or visit www.sigmadesigns.com.

Pentium Processor Module Isolates I/O From Circuitry

The mini-cartridge package has opened opportunities for the Pentium II in the board-level embedded computing realm. The EPM-2 is an embedded processor module, featuring a mini-cartridge, mobile Intel Pentium II processor that upgrades the processor function without changing the I/O structure. The module architecture separates the processor from the base I/O design, isolating the I/O from high-speed circuitry associated with high-speed processors.

The module integrates DRAM, BIOS, and expansion interfaces. Interface support includes PCI, USB, enhanced IDE, and a DRAM controller. Phoenix PICO BIOS resides in 512 kbytes of flash on the module. The EPM-2 interfaces to CompactPCI, VME, or any other baseboard via four connectors.

Radisys Corp., *5445 NE Dawson Creek Dr., Hillsboro, OR 97124; (503) 615-1100; fax (503) 615 1150; www.radisys.com.* **CIRCLE 451**

PCI-to-Serial Controller Has Eight Sync/Async Ports

When connecting large modem banks, bulletin-board servers ,and Internet connections, high-port count serial links are ideal. Aurora Technologies is pushing new levels of performance with the Saturn Multiport 8520P.

The unit is an 8-port synchronous/asynchronous PCI bus serial controller. It performs data transfers at rates up to 230.4 kbits/s asynchronous and 256 kbits/s synchronous, full duplex.

The Saturn Multiport is compatible with Sun Solstice communications protocols, Microsoft Routing and Remote Access Services for Windows NT Server, and Microsoft SNA Server for Windows NT. Optional communications protocols for Sun Solaris include Frame Relay, X.25, PPP, HDLC, and SDLC.

Available now, the unit is offered in 2-, 4-, and 8-port versions. Price is $1850, including a DB-25 breakout box.

Aurora Technologies, Inc., *176 Second Ave., Waltham, MA 02154; (781) 290-4800; fax (781) 290-4844; www.auroratech.com.* **CIRCLE 452**

LINEAR TECHNOLOGY

DESIGN NOTES

A Seven Nanosecond Comparator for Single-Supply Operation

Design Note 185

Jim Williams

The LT®1394—An Overview

A new ultrahigh speed, single-supply comparator, the LT1394, features TTL-compatible complementary outputs and 7ns response time. Other capabilities include a latch pin and good DC input characteristics (see Figure 1). The LT1394's outputs directly drive all 5V families, including the higher speed ASTTL, FAST and HC parts. Additionally, TTL outputs make the device easier to use in linear circuit applications where ECL output levels are often inconvenient.

A substantial amount of design effort has made the LT1394 relatively easy to use. It is much less prone to oscillation and other vagaries than some slower comparators, even with slow input signals. In particular, the LT1394 is stable in its linear region. Additionally, output-stage switching does not appreciably change power supply current, further enhancing stability. Finally, current consumption is far lower than that of previous devices. These features make the 200GHz gain bandwidth LT1394 considerably easier to apply than other fast comparators.

This device permits fast circuit functions that are difficult or impractical using other approaches. Two applications are presented here.

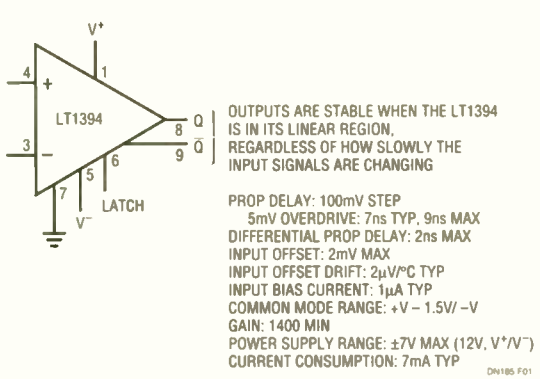

Figure 1. The LT1394 at a Glance

4× NTSC Subcarrier Tunable Crystal Oscillator

Figure 2, a variant of a basic crystal oscillator, permits voltage tuning the output frequency. Such voltage-controlled crystal oscillators (VCXO) are often employed where slight variation of a stable carrier is required. This example is specifically intended to provide a 4× NTSC subcarrier tunable oscillator suitable for phase locking.

The LT1394 is set up as a crystal oscillator. The varactor diode is biased from the tuning input. The tuning network is arranged so a 0V to 5V drive provides a reasonably symmetric, broad tuning range around the 14.31818MHz center frequency. The indicated selected capacitor sets tuning bandwidth. It should be picked to complement loop response in phase locking applications. Figure 3 is a plot of tuning input voltage frequency deviation. Tuning deviation from the 4×NTSC 14.31818MHz center frequency exceeds ±240ppm for a 0V to 5V input.

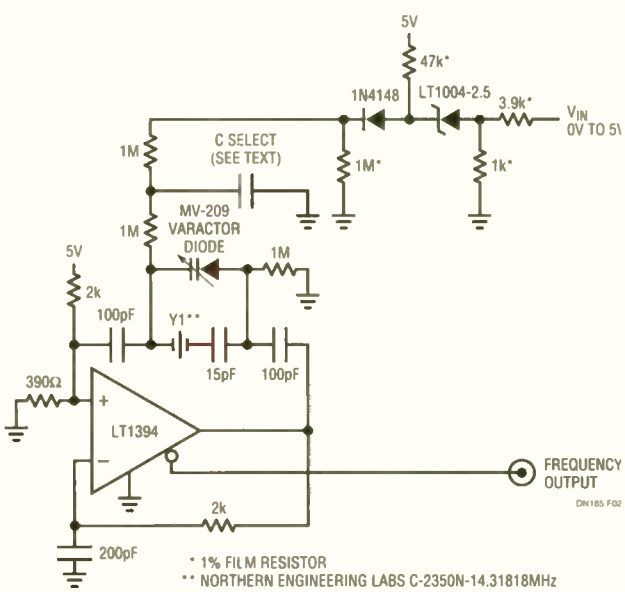

Figure 2. A 4× NTSC Subcarrier Voltage-Tunable Crystal Oscillator. Tuning Range and Bandwidth Accommodate a Variety of Phase Locked Loops

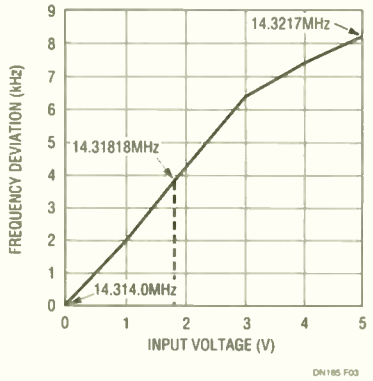

Figure 3. Control Voltage vs Output Frequency for Figure 2. Tuning Deviation from Center Frequency Exceeds ±240ppm

High Speed Adaptive Trigger Circuit

Line and fiber-optic receivers often require an adaptive trigger to compensate for variations in signal amplitude and DC offsets. The circuit in Figure 4 triggers on 2mV to 175mV signals from 100Hz to 45MHz while operating from a single 5V rail. A1, operating at a gain of 15, provides wideband AC gain. The output of this stage biases a 2-way peak detector (Q1 through Q4). The maximum peak is stored in Q2's emitter capacitor, while the minimum excursion is retained in Q4's emitter capacitor. The DC value of the midpoint of A1's output signal appears at the junction of the 500pF capacitor and the 3MΩ units. This point always sits midway between the signal's excursions, regardless of absolute amplitude. This signal-adaptive voltage is buffered by A2 to set the trigger voltage at the LT1394's positive input. The LT1394's negative input is biased directly from A1's output. The LT1394's output, the circuit's output, is unaffected by >85:1 signal amplitude variations. Bandwidth limiting in A1 does not affect triggering because the adaptive trigger threshold varies ratiometrically to maintain circuit output.

Figure 5 shows operating waveforms at 40MHz. Trace A's input produces Trace B's amplified output at A1. The comparator's output is Trace C.

Additional applications and a tutorial on high speed comparator circuitry can be found in Application Note 72, "A Seven Nanosecond Comparator for Single-Supply Operation."

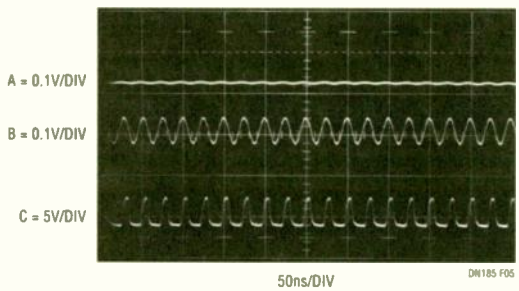

Figure 5. Adaptive Trigger Responding to a 40MHz, 5mV Input. Input Amplitude Variations from 2mV to 175mV are Accommodated

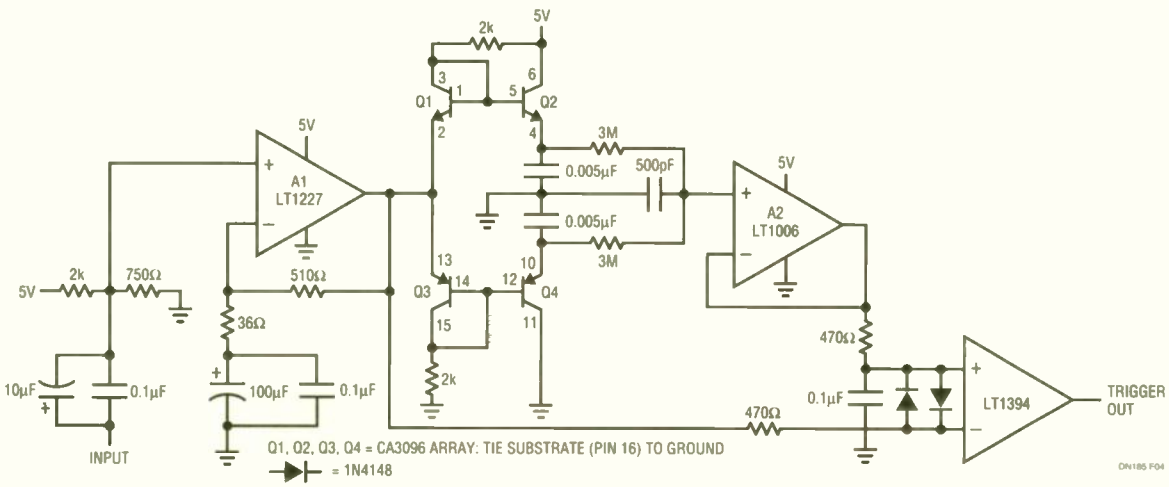

Figure 4. 45MHz Single-Supply Adaptive Trigger. Output Comparator's Threshold Varies Ratiometrically with Input Amplitude, Maintaining Data Integrity over >85:1 Input Amplitude Range

For literature on our High Speed Comparators, call **1-800-4-LINEAR**. For applications help, call (408) 432-1900, Ext. 2456

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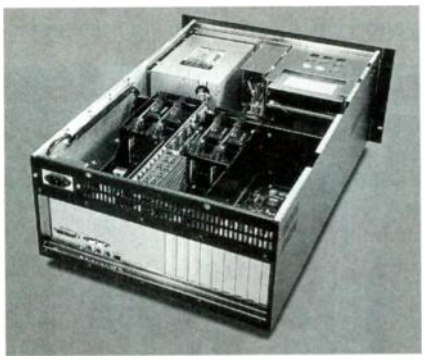
Four-Way Embedded Sparc Multiprocessor Board

To get multiprocessor performance in deeply embedded industrial applications, integrators often are forced to retrofit traditional office enterprise servers . The mismatch leads to excessive use of central-office rackmount



space, limiting integration flexibility.

As an alternative, Sun Microsystems has introduced the SPARCengine Ultra AXmp. It's a board-level solution that lets OEMs develop high-performance, four-way multiprocessing embedded systems based on the Sparc processor and Solaris.

The Ultra AXmp motherboard is designed to be deployed in an industrial, rackmount chassis in either a horizontal or vertical orientation. The board fits comfortably in a standard 5U high chassis or in a custom chassis as small as 4U. Up to ten Ultra AXmp boards can be placed in a single 19-in. rack cabinet. The Ultra AXmp motherboard has six 64-bit high-performance PCI slots, four at 33 MHz and two at 66 MHz.

Sampling now, the SPARCengine Ultra AXmp board, is sampling now, with general availability in the second half of 1998. Prices start at $7500 in volume quantities, depending on the speed and number of UltraSPARC-II S-series modules.

Sun Microelectronics, Inc. *901 San Antonio Rd, Palo Alto, CA; (512) 434-1503; www.sun.com/microelectronics.*

CIRCLE 453

PCI Mezzanine Card Hosts 3D Video Accelerator

High-performance 3D graphics can be hard to get outside the desktop world. Feeding that need is a new PCI Mezzanine Card (PMC) called the PMC/Video-3D. It easily plugs into any CompactPCI single-board computer with PMC connectors, or works as an add-on to a PMC carrier card. The card implements the PERMEDIA-2 graphics processor from 3Dlabs. The PMC/Video-3D, which contains 8 Mbytes of SGRAM, is OpenGL-compliant and Direct-3D-compatible.

The PERMEDIA-2 provides up to one million textured polygons per second; 83 million textured, bilinear filtered and perspective corrected pixels per second, and 42 million textured, filtered and perspective corrected pixels per second.

The PMC/Video-3D provides video streams, I/O capabilities, and is designed to work with a video-acquisi-

(continued on page 98)

(continued from page 97)
tion card. Its I/O functions include built-in 230-MHz RAMDAC for RGB video output and VESA VMI streams to user PMC connectors. The card works with Windows NT, Windows 95, OpenGL 1.1, Direct3D, and Heidi.

Alto Technology Corp., *9500 South 500 West, Suite 212, Sandy, UT, 84070; (801) 562-1010; fax (801) 254-2020; www.altatech.com.* **CIRCLE 454**

Thermal Printer Module Targets Kiosk Applications

The kiosk market, including everything from label, bar code, point-of-sale, gaming, and gas-tank level sensing kiosk applications, is expected to be a billion dollar market within a few years. Thermal printer subassemblies represent a key part of such systems.

The Speed Module is a compact (2.95 by 5.05 by 6- in.), lightweight (2.5 lbs.), thermal printer module that can be mounted either vertically or horizontally. The module offers a print resolution of 8 dots/mm, print speed of 75 mm/s or 6.75 cps, and a current consumption of 1.8 A to 4.3 A at 24 V dc). It's available in three models: 60-mm, 80-mm, and 112-mm paper widths. Featuring a 2-in. paper roll, paper advance, cutter activation, error and paper-out indicators, the Speed Module also offers a full range of options, including full- or partial-cutting capability, as well as automatic and manual paper loading.

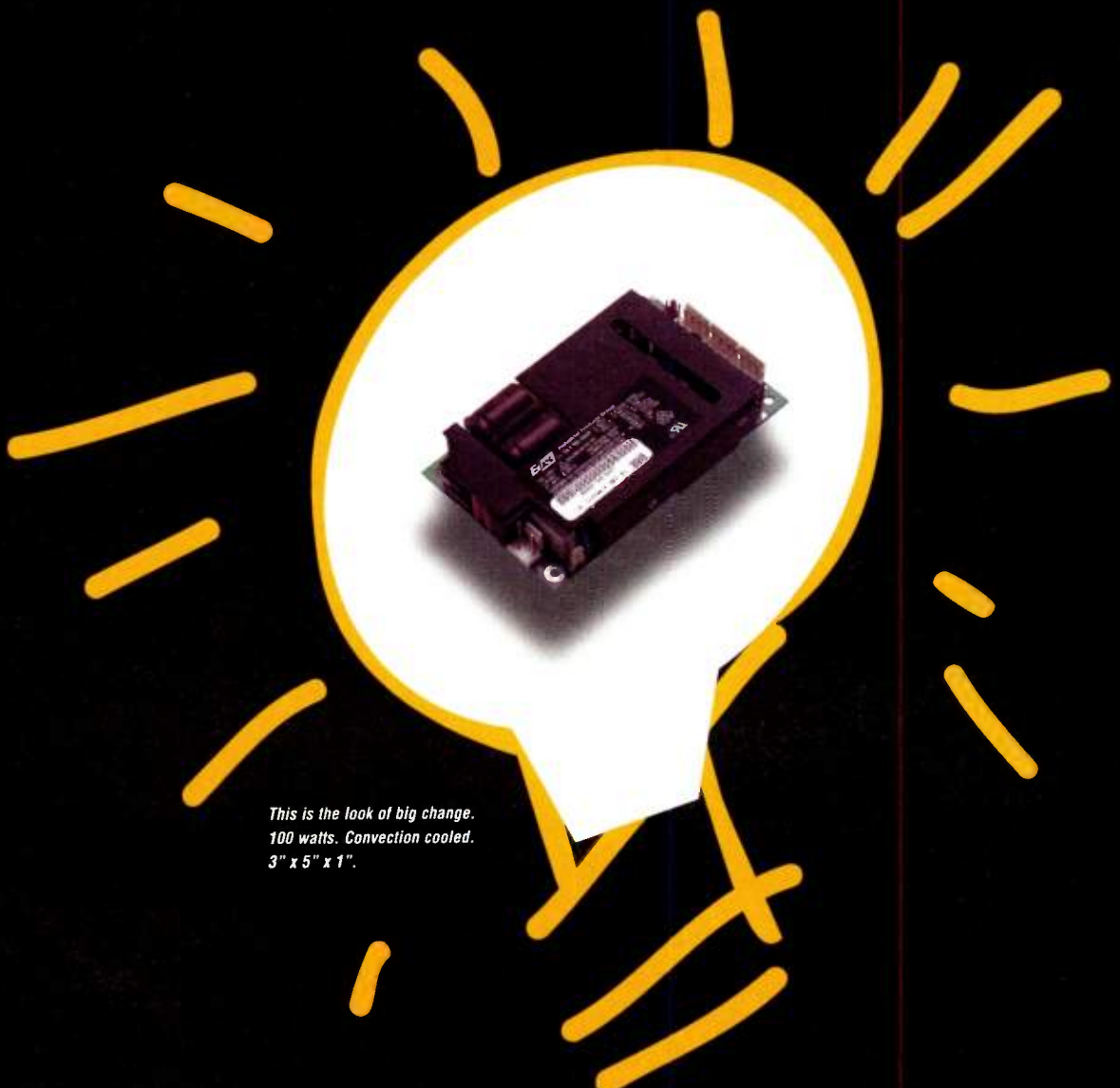
All of Seiko Instruments' kiosk subassemblies include the company's proprietary page mode firmware. Called Thermal Control Language (TCL), it enables design engineers and system integrators to design and store unique templates for any application. TCL is integrated into the subassemblies, and provides an easy-to-use design tool for quickly developing templates for receipt printing.

TCL operates under Windows and provides a rich command set that includes line and box drawing functions, text bar codes, and PCX graphics, as well as multiple copy capabilities. Templates are stored as data files in flash memory, allowing for easy upgrade through the communication interface.

Available immediately, the suggested retail price for the Speed Module series is $683 for the 60-mm, model number KSM-60; $730 for the 80-mm, model number KSM-80; and $751 for the 112-mm, model number KSM-112.

Seiko Instruments USA Inc., *2990 West Lomita Blvd, Torrance, CA 90505; (800) 553-6570; fax (310) 517-8154; www.siumpd.com.* **CIRCLE 455**

HEY! WHAT'S THE SMALL IDEA?



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READER SERVICE 124

Circle 520

Electronic Flicker Pulsing Suppresses EMI Problems

MARK A. JOHNSON AND PAUL J. COTE
Benet Labs, Watervliet, NY 12189-4050.

Pulsing circuits generate EMI that can affect sensitive circuitry and adversely contribute to the spectral signature of the equipment. "Flicker-noise" concepts, derived from chaos theory, have been employed to efficiently pulse circuitry while generating a virtually undetectable spectral signature. Pure flicker pulsing requires that the components be driven with a set of uncorrelated pulses, with random heights, started at random times. Jensen, et. al. *(Phys. Rev. B40, 7425, 1989)* demonstrated that the power spectral density for such a signal generates $(1/f)^n$-type noise given by:

$$S(f) = \frac{\upsilon}{(\pi f)^2}\int_0^\infty d\tau G(\tau)\sin^2(\pi f\tau) \qquad (1)$$

where v is the pulse rate and $G(\tau)$ is the weighted distribution of lifetimes, defined as:

$$G(W) = \int_0^\infty dS P(S,W)[S/W]^2 \qquad (2)$$

where P(S,W) is the joint probability for a pulse to have area S and width W. In most circuitry, S, W, and the pulse spacing, T, are normally fixed, with a duty cycle given by W/(W+T).

The power spectral density (PSD) for a periodic signal with W = 122 μs, S = nW = 122 μV-s, and T = 1.83 ms is given in Figure 1. When S, W, and T are allowed to vary, the results are dramatically different. Figure 2 shows the PSD for a signal with W, S, and T given by uniform probability density functions with mean values: $\overline{W}$= 122 μs, $\overline{S} = n\overline{W}$= 122 μV-s, and $\overline{T}$= 1.83 ms. The PSD was obtained using Welch's method of estimating the power spectrum from the time series data signal, using a Hanning window of length 256 and with a sampling frequency of F_S = 820 kHz.

The analytic solution can be determined from Equation 1, assuming fixed pulse amplitudes and a probability density function P(W) of the form:

$$P(W) = \int_0^\infty P(S,W)dS = \frac{1}{(W_{MAX} - W_{MIN})} = \frac{1}{\Delta W} \qquad (3)$$

Assuming the pulses are all fixed amplitude, S = nW, requires

$$P(S) = \int_0^\infty P(S,W)dW = \frac{1}{n\Delta W} \qquad (4)$$

therefore

$$P(S,W) = \frac{1}{n\Delta W}\delta(W - S/n) \qquad (5)$$

and

$$G(W) = n^2/\Delta W \qquad (6)$$

This results in a power spectral density given by:

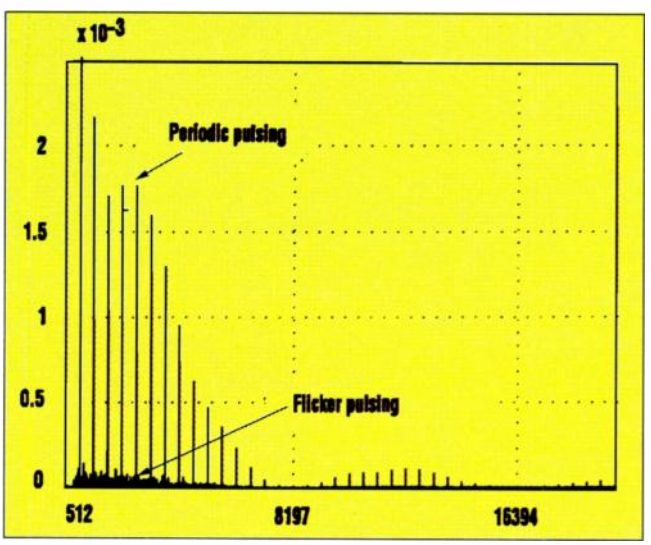
$$S(f) = \frac{\upsilon}{2}\left(\frac{n}{\pi f}\right)^2 \times \left(1 - \frac{\cos(\pi f(W_{MAX} + W_{MIN})\sin(\pi f\Delta W)}{\pi f\Delta W}\right) \qquad (7)$$

For W_{MIN} = 0, S(f) reduces to:

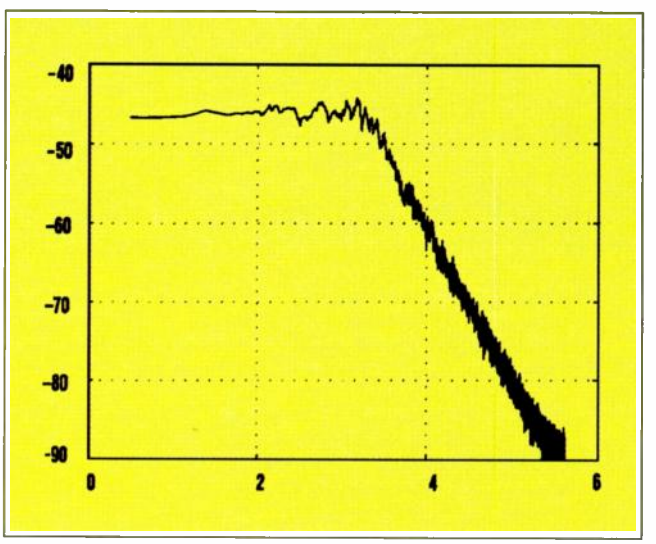
$$S(f) = \frac{\upsilon}{2}\left(\frac{n}{\pi f}\right)^2 (1 - \mathrm{sinc}(2fW_{MAX})) \qquad (8)$$

S(f) corresponding to this pulse distribution, with ν = 512 pulses/s and W_{MAX}=244 μs, is given in Figure 3. The analytic solution agrees with the PSD obtained from the time series data and also shows the origin of the $(1/f)^2$ dependence.

In our application, we were required to improve the efficiency of LED drivers, without affecting the spectral signature of the system. Pulsing an LED is an effective means of attaining maximum light intensity with minimum power drain. A rule of thumb for most LEDs is that driving the LED in the

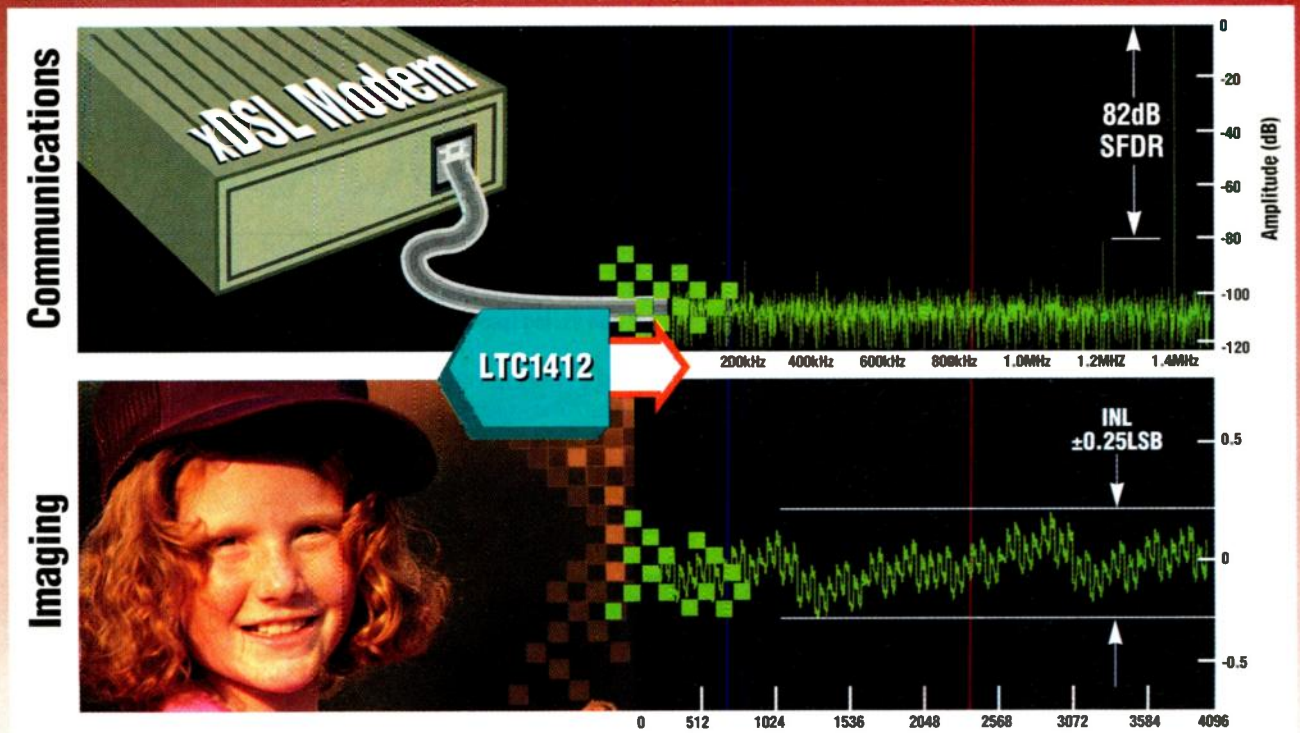


1. Power spectral density for periodic and flicker pulsing with W = 122 ms, S = nW = 122 mV-s, and T = 1.83 ms. (volts²-sec vs. sec⁻¹)



2. Power spectral density for $P(S,W) = \frac{1}{n\Delta W}\delta(W - S/n)$.(dB vs. log (sec⁻¹))

12-Bit 3Msps ADC Has Best AC and DC Performance

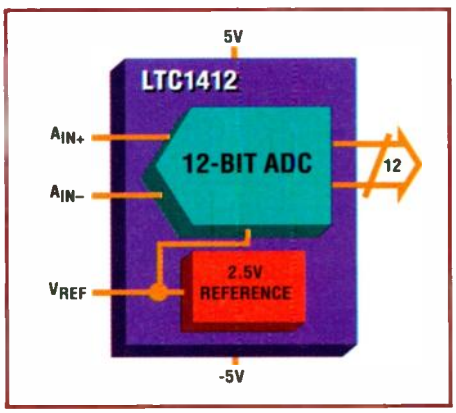


LTC1412: Best Spectral Performance for Communications Best DNL/INL Performance for Imaging

The LTC1412 excels in both AC and DC performance making it ideal for both Communications and Imaging applications. The 3Msps sampling rate is perfect for most demanding xDSL modem applications or for digitizing CCD outputs in imaging applications. Several added features make it easy to use: onboard 2.5V reference, high CMRR differential inputs, low 150mW power dissipation and the small SSOP-28 package.

Features

- 3Msps Sample Rate
- 72dB SINAD and 82dB SFDR for Communications
- ±0.1LSB Transition Noise and ±0.25LSB Typical DNL for Imaging
- 150mW Power Dissipation
- No Pipeline Delay
- Smallest Footprint: SSOP-28
- ±1LSB Max INL and DNL Over Temperature
- $9.95 Each in 1000-Piece Quantities



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IDEAS FOR DESIGN

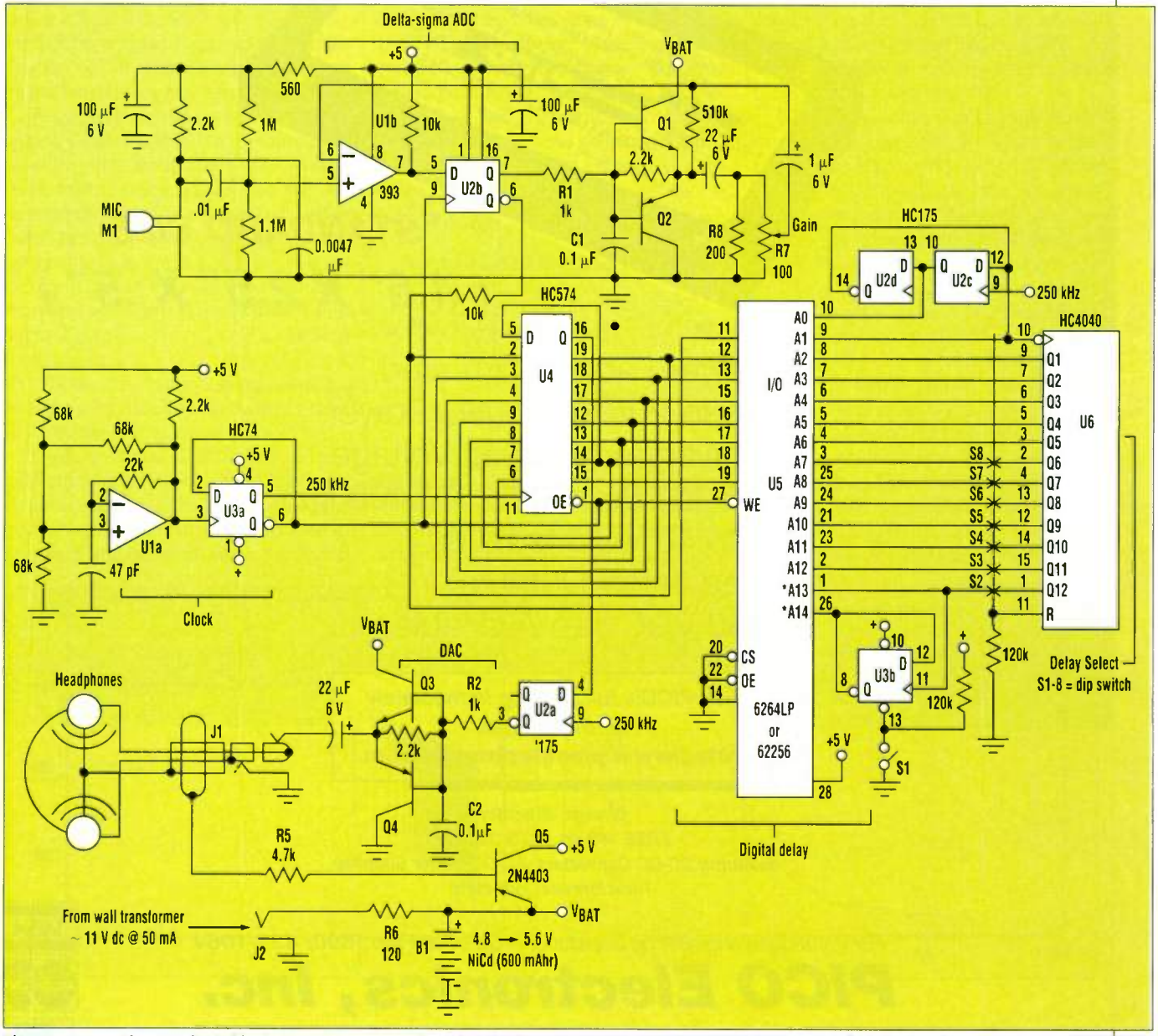
Circle 521

Vocal-Aural Feedback Digital Delay Device

W. STEPHEN WOODWARD
Venable Hall, CB3290, University of North Carolina,
Chapel Hill, NC 27599-3290; Internet: woodward@net.chem.unc.edu.

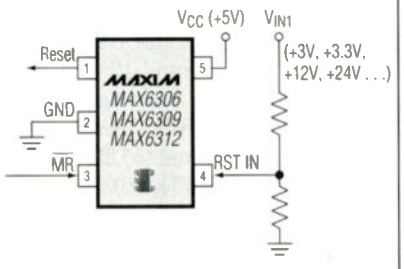
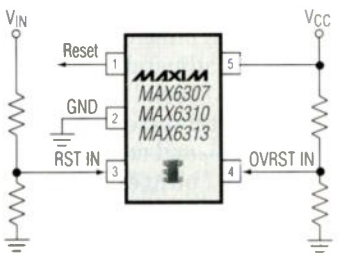
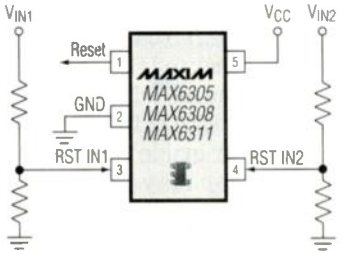
When humans speak, many complicated, interrelated, and not completely understood neural and muscular processes must all coordinate. Most of these processes aren't accessible to simple investigation, but one important speech-production mechanism is subject to easy and harmless experimentation. It's based on the obvious fact that we normally hear our own voice whenever we talk and instinctively rely on this real-time feedback to aid in the production of fluent speech.

If a time delay of the right duration (0.2 to 0.5 seconds) is inserted in this vocal-aural feedback pathway, normal speech becomes amazingly and fascinatingly difficult. Some interesting insights (not to mention amusement) can be gained by experimenting with this effect. Moreover, there's evidence that speech therapy involving sessions of talking under delayed aural feedback can help improve a common and sometimes severe speech handicap: stuttering.



This circuit provides an adjustable, battery-powered audio delay that's well suited for speech experimentation and stuttering therapy.

SINGLE SOT RESET IC MONITORS 3V/5V, 5V/12V, 5V/24V, . . . SYSTEMS

V_{CC} Undervoltage + Adjustable Undervoltage	V_{CC} Undervoltage + Adjustable Undervoltage + Adjustable Overvoltage	Dual Adjustable Undervoltage
		

- 8µA I_{SUPPLY}
- 4 Timeout Delays: 1/20/140/1120ms
- Factory-Trimmed V_{CC} Reset Thresholds; 2.5V to 5.0V in 100mV Increments
- Guaranteed Reset Valid to V_{CC} = 1V
- Guaranteed Over Temperature
- Immune to Short V_{CC} Transients
- 5-Pin SOT Package

PART	FACTORY-TRIMMED V_{CC} RESET	ADJUSTABLE UNDERVOLTAGE RESET	ADJUSTABLE OVERVOLTAGE RESET	MANUAL RESET INPUT	OUTPUT
MAX6305		✔			Open-Drain $\overline{\text{RESET}}$
MAX6306	✔	✔		✔	
MAX6307	✔	✔	✔		
MAX6308		✔			CMOS $\overline{\text{RESET}}$
MAX6309	✔	✔		✔	
MAX6310	✔	✔	✔		
MAX6311		✔			CMOS RESET
MAX6312	✔	✔		✔	
MAX6313	✔	✔	✔		

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Circle No. 128 - For U.S. Response
Circle No. 129 - For International

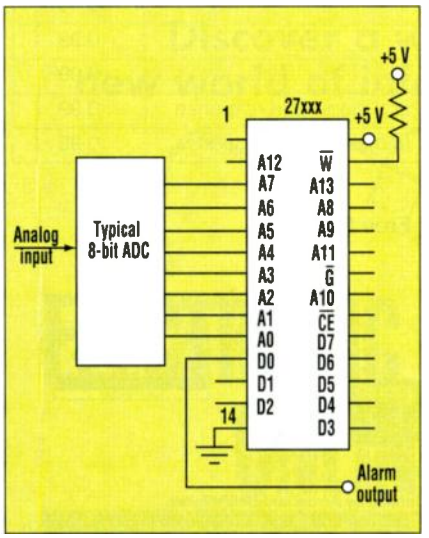
Circle 522

Novel Decoding/ Threshold-Sensing Technique

JUD HILDEBRANT
C.E.T., Hildebrant Engineering, Defiance, OH 43512; (419) 784-5923.

Here's an *Idea For Design* that's more *Idea* than it is *Design*. Using inexpensive memory devices, you can construct a voltage, current, or count sensing system that can be permanently programmed for one set of input conditions or programmable for custom sensing of input parameters.

In Figure 1, we have a parallel-output analog-to-digital converter wired to a typical EPROM. The EPROM has been programmed with zeroes for the first 128 bytes, the 129th byte contains the value 1, and the remaining bytes are zeroes. Let's assume the ADC has a 0- to 5-V input and a fairly linear output. As the input voltage swings from 0 to 5 V, the analog-to-digital output goes from binary 0 to binary 255. At approximately 2.5-V input, the output will be the binary number 129, and the EPROM, decoding address 129, will output its stored value (one). Data line 0, here labeled "alarm output," will go high, signaling that the input has reached the level we're monitoring. If an inverted output is needed, simply substitute ones for zeroes and zeroes for ones.



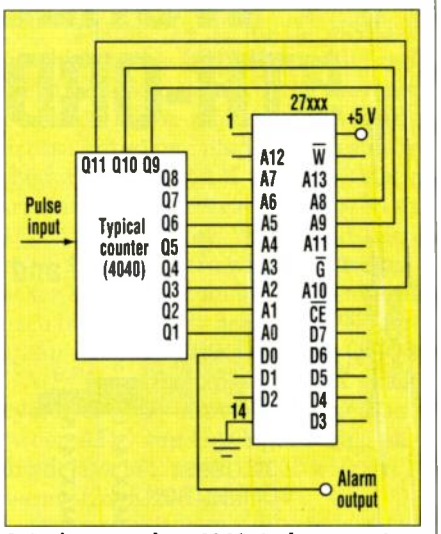
1. Here, an Analog-to-Digital Converter is wired to a typical EPROM, providing the basis for a different approach to creating a voltage, current, or count sensing system.

By programming all ones in memory addresses 129 and up, our alarm output becomes an overvoltage indicator. Alternately, by putting ones into addresses 0 to 129, and zeroes above, we have an undervoltage sensor. By putting single-bit numbers (4, 8, 16, etc.) into the EPROM, one could monitor up to eight different input levels, each with an individual output.

When a frequency-to-voltage converter is used as an input to the ADC, a dandy little frequency-drift monitor results. By programming the EPROM with different values, the direction and extent of the drift can be determined.

In Figure 2, a 4040 ripple counter is connected to our EPROM. This circuit will count from zero to 4096, then ripple out to zero, etc. Suppose we need to know when the input has received exactly 2345 pulses (or any arbitrary number). By programming the EPROM with all zeroes, except for memory location 2345 which contains a one, the circuit will output when the desired pulse count is reached. If you need to count a given number of pulses and then reset to start over, the D0 output can be brought back to the 4040's RESET input. As in the example above, by putting single-bit numbers into specific memory locations, up to 8 different pulse counts can be monitored. By cascading counter chips, one could monitor pulse counts into the millions.

Still referring to Figure 2, if the EPROM is programmed with the numbers 0 to 255 in memory locations 0 through 255, and the number pattern is repeated throughout the rest of the memory locations, the EPROM becomes a frequency divider with output D0 = input/2, D1 = input/4, etc. up to D7 = input/256. Each output maintains a 50% duty cycle, regardless of the input signal's duty cycle. By carefully selecting other bit patterns, division by any number from 2 through 128 is possible. For example, the byte pattern 0,0,1,0,0,1, etc., will provide a divide-by-3 function with a 33% duty cycle, and 0,1,1,0,1,1 yields a 67% duty cycle.



2. In this example, a 4040 ripple counter is connected to the EPROM. This circuit arrangement could, for instance, monitor an address bus for a given address value, or monitor a data bus for a given byte value.

By connecting the EPROM's address lines to a typical data bus, you can monitor the bus for a given byte-value. This may be useful as an inexpensive data-acquisition system.

By connecting the EPROM's address lines to a typical address bus, you can monitor the bus for a given address value. A non-valid address would indicate a "crashed" or "insane" processor. The alarm output then could be used to reset the processor.

Of course, this circuit configuration isn't limited to using an EPROM. Depending on the application, SRAM, NVSRAM, flash, etc. might be substituted. With a microprocessor or microcontroller monitoring the output of the memory chip, it becomes possible to reprogram the chip on-the-fly, thus enabling the circuit to monitor a vast multitude of varying input conditions. This could be useful for scaling an unknown or widely varying analog input.

The circuit diagrams presented here are intentionally lacking in detail, in the hope that this will stimulate the readers' imagination and encourage further experimentation with the techniques presented.

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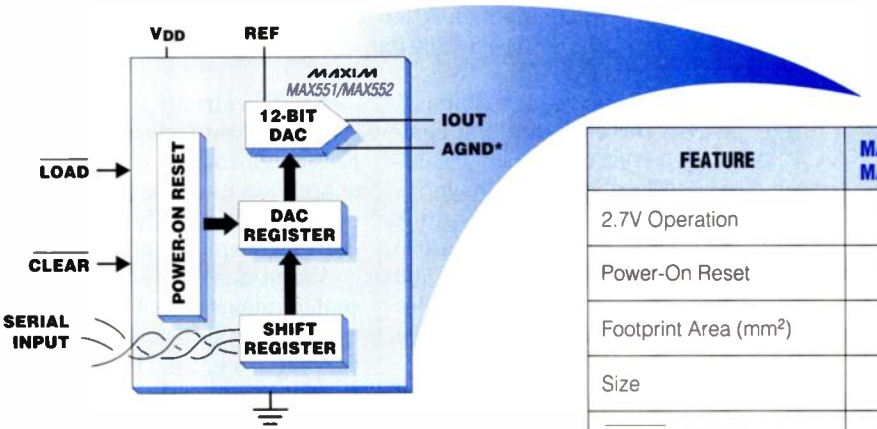

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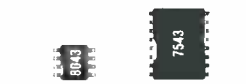

FEATURE	MAX551 MAX552	8043	7543
2.7V Operation	Yes	No	No
Power-On Reset	Yes	No	No
Footprint Area (mm^2)	16	31	114
Size	1x	2x	5x
$\overline{CLEAR}$ (RESET)	Yes	No	Yes
Bipolar Operation (Offset) with Single Supply	Yes	No	No

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Circle No. 132 - For U.S. Response
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Circle 523

Simple Current Sensor Features Galvanic Isolation

JOSE A. CARRASCO
Universidad de Valencia, Dpto. de Informatica y Electronica,
C/. Dr. Moliner, 50, 46100 Burjassot, Spain;
phone: 34-96-3160460; fax: 34-96-3160466.

Applications that require a simple, low-cost current sensor with galvanic isolation can employ the circuit described here. If used as drawn, it's possible to sense currents up to 10 A with high precision (usually within 2%) and wide bandwidth (more than 500 kHz). The use of optocouplers provides 3000 V of isolation between the primary and secondary and 50 dB of CMRR.

Transistors T1 and T2 form a coupled pair in current-mirror configuration that's unbalanced by the current (I) to be measured. Once this happens, transistor in OP1 balances the current-mirror biased by T3 that also biases OP2, making its transistor conduct the same current that balances the current-mirror. Because the balancing current is directly proportional to the current being measured, a direct measurement is achieved. It can be easily shown that the gain in current is given by the ratio of the sensing resistor (R_S) and R1, producing a proportional voltage drop at the Output terminals.

For the circuit to work properly, it's important that the coupled transistors which form the current mirror share the same substrate and that the optocoupler be a dual version, in order to have matching characteristics.

Variations on this idea may lead to configurations that can be used in a wide range of applications, such as sensing current in a ground line (inverting the operating idea of the current-mirror by using npn transistors) or offering different conditioning at the output (increasing voltage with increasing current). The power supplies needed can be implemented using Zener diodes since only a small amount of power is required—usually less than 50 mW.

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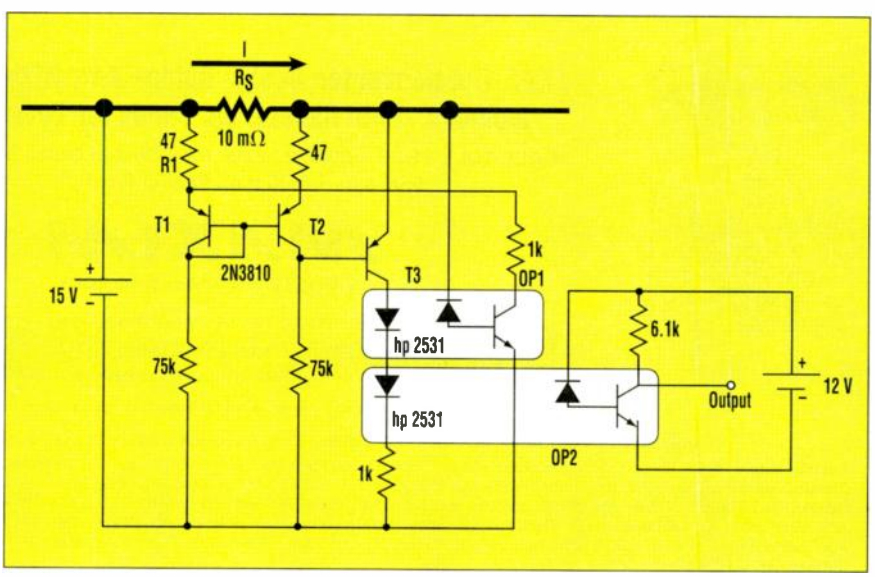

This simple, low-cost current sensor, which features galvanic isolation, uses a current-mirror configuration to sense currents up to 10 A with high precision and wide bandwidth.

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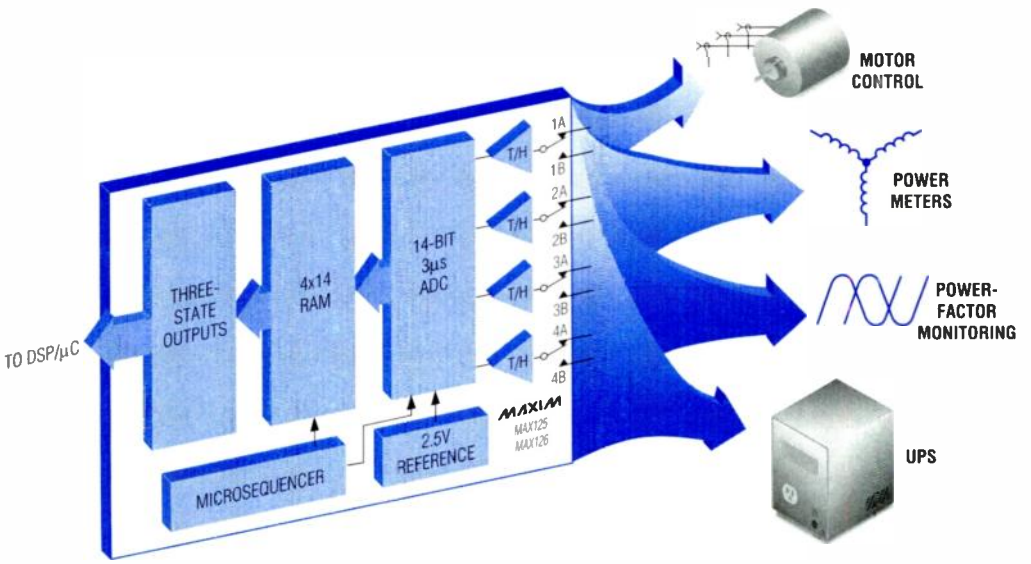

- 14-Bit, 3µs ADC
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  ±2.5V (MAX126)
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- 4 Simultaneous T/Hs with 2:1 Muxed Inputs
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- Internal 2.5V Voltage Reference
- High-Speed, 14-Bit Parallel Interface
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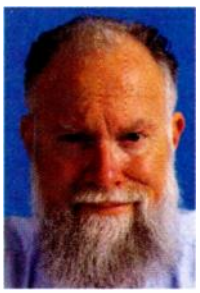
BOB PEASE

Bob's Mailbox



Dear Bob:

In your April 20 column, you mentioned that someone corrected your use of the red thermocouple wire as the positive lead. Actually, there is no "correct" answer.

It seems that the IEC standard for thermocouple color coding calls out red as the *plus* lead; this standard is used around the world, except in the U.S. The U.S. uses an ISA/ANSI standard for thermocouples that calls out red for the *minus* lead.

This standard has expired, and there is a big controversy going on (or at least there was a few months ago) over whether or not to adopt the IEC standard in the U.S. (This would cause quite the confusion, what with the huge installed base of *minus* red lead thermocouples already in place.) You can search for more info about this on the web.

DEAN ATHANIS
Another ex-Philbrickian,
via e-mail

P.S. I got five minutes for the bridge crossing puzzle, too—although I bet Ari would've slowed down a bit by the time he carried the third guy across!

Thanks for clarifying "which way is up!" Maybe they'd better pick some new colors—not red or yellow. And hey, that ARI is a tough guy! (One guy suggested they could get over in 12 minutes if they just waited 'til morning.)—RAP

Dear Bob:

Re: manhole covers (Puzzler #7, in the April 6 issue): I knew why they were round. In Minnesota we had rectangular storm drain covers, which *some kids* would often drop into the sewers below. But not having been in Nashua very often (I did live in Lynn, Mass.), I failed to notice the triangular manhole covers up there.

I immediately thought of a large pressure vessel, such as a boiler or locomotive inspection cover. This type of "Manhole" is big enough for some hapless boilerworker (boilerperson doesn't sound right) to crawl inside. The cover has a ledge on the inside to withstand the high pressure, and is merely held in place from the outside by a set of "dogs" or other clamping device. The manhole is oval, to permit it from being unbolted. And when the pressure is relieved, it may be lifted into the vessel, twisted 90 degrees twice, and withdrawn from the pressure vessel. Does this count as a non-round "manhole?"

ROBERT DAHLGREN
Fujikura Technology America Corp.
via e-mail

Hello, Robert D. On the FRONT of a steam locomotive, you will often see a large round Disc, the inspection hole for the Steam Box—fastened down by bolts or dogs. Those discs are round, usually. Perhaps three or five feet in diameter. But THEY do not have to hold any particular pressure, maybe three or seven pounds per square inch. They are just fastened on the outside of the engine, on the front.

The manholes YOU refer to DO have to stand off a whole lot of pressure. You are correct that oval is a very good shape for them, and that they get turned and turned and mounted inside.

In some cases, where there is not a lot of stress, a single bolt & (two-eared) clamp holds them in place. I can't guess how many years ago that was figured out, but maybe 200 or 300? Maybe more? I'll try to check into this. Your point is nicely taken.—RAP

Hi Bob:

I always enjoy your Pease Porridge. In regard to the April 20 column, you mentioned getting a "whack" for spilling your milk as a kid. Well, as recent parents, we give our son "swats" for being bad. We don't punish accidents, but deliberate misbehavior is another matter. *(I tend to agree with your policy. Of course, there is every kind of INTERPRETATION..../rap)*

We have an excellent example of what *not to follow* living across the street. On one occasion, we observed the younger boy taking a roundhouse swing of a hollow plastic bat and connecting (squarely, I might add) with the back of his older sister's head. Repercussions, you might ask? Their mother ordered the boy to apologize to his sister and give her a hug. *(One of these days, he may use a wooden baseball bat, not realizing what damage can thus be caused...not just repercussions, but CONcussions—or death. Sigh. /rap)*

This is but one of a forest of stories about these kids and their parents. By not controlling and punishing this behavior, the parents encourage them to use similar tactics on others (and it has happened).

So, the question to ask the reader who claimed you were "brutal" to your son is: Who is more "brutal?" The parents who allow their children to misbehave, so as to not damage their delicate psyches—yet the children grow up to be reckless and irresponsible adults? Or, the parents who risk hurting their children's feelings when they misbehave so that they grow up to be responsible and respectful adults? *(A very well-phrased question.../rap)* I happen to believe that you did the right thing.

Bob Becker
via e-mail

IF my son had pulled the glass away, I think I would have given him a very SMALL swat—just to get his attention, maybe a rough pat on the shoulder, so he would realize he had made a mistake.

*I know a gal who always threatened her kids, "If you don't start behaving right away, I'm going to beat your a** 'til your nose bleeds." But she never did. And I think one of her kids grew up OK. The other one I'm not so sure about, and the third is in the PEN, doing 5 to 10....*

Sigh...one out of three is not a great batting average....—RAP

All for now. / Comments invited!
RAP / Robert A. Pease / Engineer
rap@web team.nsc.com—or:

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New Drain Structure Cuts High-Voltage MOSFET's On-Resistance

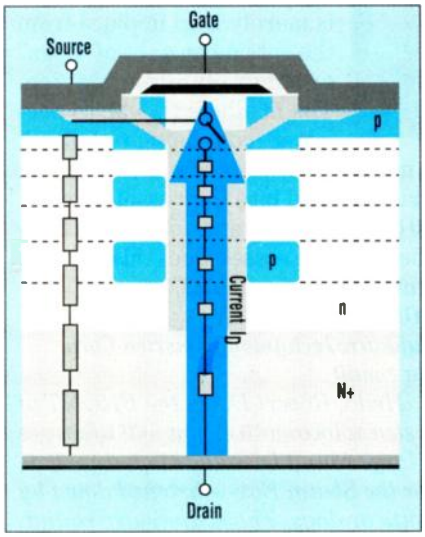
By incorporating vertical p-stripes in the drift region of the power MOSFET, as well as using thinner epitaxial layers, Siemens Semiconductor Group in Munich, Germany, was able to craft a new line of low $R_{DS}(on)$ high-voltage MOSFETs. Siemens claims that the novel drain structure, implemented in the new CoolMOS family, will result in over five times improvement in the on-resistance of 600- to 1000-V power MOSFETs. In fact, current plans call for extending this performance to 400 V first, and then later developing 1200-V CoolMOS power MOSFETs.

"It is a radical change in MOSFET design that drastically reduces practical on-state resistance for a given chip area in high voltage MOSFETs," says Claus Geisler, vice president of marketing for power semiconductors at Siemens AG.

According to Jon Hancock, senior applications engineer at Siemens Microelectronics, "This improvement has been obtained without impairment to the ruggedness and high avalanche strength of the MOSFET."

The new design changes the relationship of the on-resistance to the blocking voltage. In conventional MOSFETs, the on-resistance for a given chip area increases exponentially with breakdown voltage. The CoolMOS changes it to a linear relationship, according to Geisler. The internal measurements indicate that this linear relationship between Ω–mm^2 and breakdown voltage holds true from 400 to 1000 V. And, efforts are underway to extend it beyond 1000 V.

Plus, Geisler says, the gate charge requirement has been reduced by half with the new design. As a result, the



drive circuit for the CoolMOS transistor is simpler, thereby lowering the overall system cost. Also, the chip area has been shrunk significantly, permitting smaller packages for high-voltage MOSFETs. In essence, the redesign provides current capability for a given chip area of the MOSFET that approaches the performance of an IGBT.

Because epitaxial resistance is a major contributor to the $R_{DS}(on)$ of high-voltage MOSFETs, Siemens' designers came up with a fundamentally different epitaxial drain structure. In the new scheme, six layers of alternating n and p structures produce a neutral region with a high blocking capability in the off state. In the on state, the structure produces a low resistance path in parallel to another path that blocks high voltage. The result is a higher voltage-blocking capability with a thinner epitaxial layer, notes Hancock. Incorporating a small number of additional layers raises this blocking voltage.

The CoolMOS MOSFETs will target off-line switching power supplies, electronic ballasts for lighting, class D switching amplifiers for professional audio and medical equipment, and many other applications that are seeking high-voltage MOSFETs in smaller packages. According to Siemens, with lower loss from smaller packages, the new devices are expected to help bring about miniaturized systems with better efficiency and reduced component cost.

The first member of the CoolMOS family, the SPP21N60S5, is a 600-V, 21-A n-channel MOSFET in a TO-220 package with an $R_{DS}(on)$ of 190 mΩ. Other package options include TO-218, TO-247, and D^2PAK. Sampling now, this part is slated for production in the fourth quarter. Meanwhile, the manufacturer plans to add several more 600-V MOSFETs in various packages to the CoolMOS family, ranging from 6 Ω to 70 mΩ by year's end. This will be followed by 800- and 1000-V devices in the first quarter of 1999.

Siemens Microelectronics Inc.
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www.smi.siemens.com
CIRCLE 460
ASHOK BINDRA

UART Comes With On-Chip Tx/Rx FIFO Counters

To improve system throughput, Exar Corp. has released universal asynchronous receiver/transmitter (UART) ICs with on-chip transmit (Tx) and receive (Rx) FIFO (first-in, first-out) counters and 128-byte FIFO depth. A FIFO depth of 128 bytes allows the UART to receive longer data packets, thereby increasing the interval between required CPU accesses. The single model is XR16C850, while the quad version is XR16C854.

Both new UARTs provide a maximum data rate of 1.5 Mbits/s at 5.0 V. In addition, the UARTs include an automatic RS-485 half-duplex switch. According to the company, the XR16C850 and XR16C854 are pin-to-pin (drop-in) replacements for earlier generations.

Optional serial interfaces include an IrDA-compliant infrared encoder/decoder and a modem. The UARTs can operate from a single 5.0-V or 3.3-V supply. Typical operating current at 5.0 V is 1.5 mA. Both of the chips provide automatic wake-up and sleep modes.

While the XR16C850 comes in 44-pin PLCCs, 40-pin plastic DIPs, and 48-pin TQFPs, the quad XR16C854 is housed in 68-lead PLCCs, 64-lead TQFPs, and 100-lead quad flat packs. In 10,000 piece quantities, the XR16C850 costs $5.00, and the XR16C854 is priced at $12.00. AB

***Exar Corp.**, 48720 Kato Rd., Fremont, CA 94538; (510) 668-7000; www.exar.com.* **CIRCLE 461**

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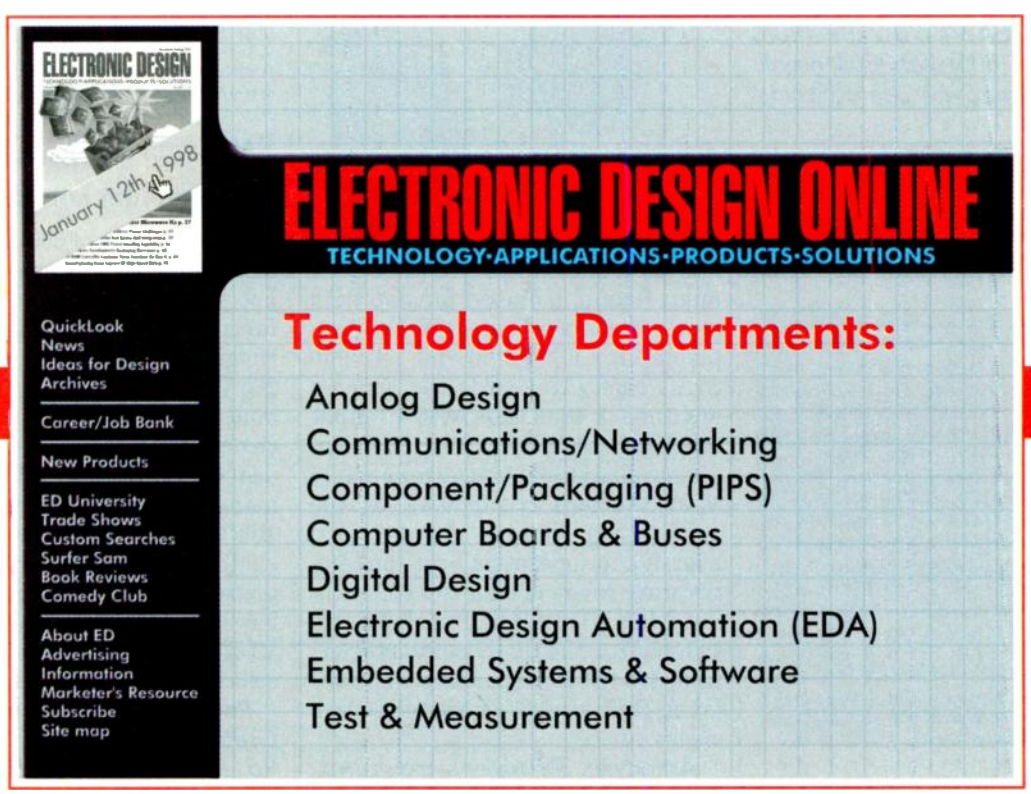
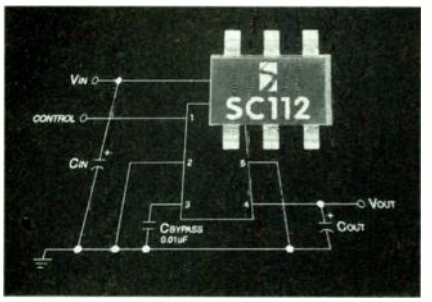


www.elecdesign.com

Ultra-Low-Dropout Regulator Has Small Footprint

Targeting a range of consumer and computer applications, the SC112 voltage regulator has a dropout of 180 mV at 60 mA and comes in a six-lead SOT-23 surface-mount package. A functional replacement for the 150-



mA TK112, the regulator has a fixed trimmed voltage tolerance of ±3%, a standby current of 0.1 µA, (OFF, V_{IN} of 8 V), and a current range to 150 mA. Other features include short-circuit protection, a noise voltage level of 30 µV with a bypass capacitor, and available voltages of 2.75, 3.0, 3.25, 3.3, 3.5, 4.0, 4.5, 4.75, and 5.0 V. Pricing is $0.29 each per 10,000. PM

***Semtech Corp.**, 652 Mitchell Rd., Newbury Pk., CA 91320-2289; (805) 498-2111; fax (805) 498-3804; e-mail: info@semtech.com; www.semtech.com.*

CIRCLE 462

Plug-In DC-DC Converter Needs No Extra Components

The UNR-3.3/3-D5 is a low-cost dc-dc

converter that requires no extra components. Measuring 1 by 1 by 0.45 in., the converter runs off 4.75 to 5.5 V and outputs 3.3 V at 3 A. The line and load regulations are ±0.4% (max) and ±5% (max), respectively. Other features include a noise level of 30 mV, a transient response of 40 ms, and full-power operation up to 70°C. Based on a switching buck-regulator design, the converter comes encapsulated in a thermally conductive potting compound in a plastic package. Snubber circuits and formed clock pulses allow it to pass all relevant FCC and EN testing for radiated emissions. Pricing is $23 each per 5000; delivery is from four to eight weeks. PM

***Datel Inc.**, 11 Cabot Blvd., Mansfield, MA 02048-1151; Bill Smith (508) 339-3000, ext. 397; fax (508) 339-6356; e-mail: sales@datel.com; www.datel.com.*

CIRCLE 463

Open-Frame DC-DC Converters Meet UL And TUV Specs

Designed for telecom and embedded applications, the ASDH Series of MicroBrick dc-dc converters come in an

open-frame, isolated format with power levels of 5, 7, or 10 W. Fully approved for EN60950 and UL1950 SELV safety standards, the converters come in 48 models with 4:1 input ranges of 9 to 36 V and 18 to 75 V. Single and dual outputs range from 3 to 15 V. Measuring 1 by 2 by 0.375 in., the converters include an integral heatsink for operation over the temperature range of –25° to 71°C without additional cooling or derating. Pricing for the dc-dc converters is from $15 to $29, depending on power level. Delivery is from stock to two weeks. PM

***Astrodyne**, 300 Myles Standish Blvd., Taunton, MA 02780; Paul Charrette, (508) 823-8080; fax (508) 823-8181.*

CIRCLE 464

Triple-Output Converters Produce Up To 50 W

The Model pV48-T3512 and Model pV48-T512 are triple-output dc-dc converters that output up to 50 W. Both measure 0.5 by 2.4 by 4.6 in. and take an input of 39 to 60 V dc. The 'T3512 outputs 3.3 at 4 A, 5 V at 6.5 A, and –12 V at

0.5 A, while the 'T512 outputs 5 V at 8 A, 12 V at 1 A, and –12 V at 0.2 A. Features include an input-to-output isolation of 2000 V dc (min), an efficiency of 82%, 3.3- and 5-V outputs trimmable to ±5%, short-circuit protection with automatic recovery, and power-OK signalling. Protection comprises non-shutdown overvoltage protection, thermal shutdown at 105°C, and logic on-off control. They sell for $115 each per 100. PM

***RO Associates Inc.**, 246 Caspian Dr., P. O. Box 61419, Sunnyvale, CA 94088; (408) 744-1450; fax (408) 744-1521; e-mail: sales@roassoc.com; www.roassoc.com.* **CIRCLE 465**

Hot-Swap AC-DC Supplies Offer Custom Configurations

The PFC Series of 600- to 2000-W ac-dc power supplies come in a 3U DIN hot-swap configuration with power-factor-corrected universal inputs ranging from 84 to 265 V ac or 174 to 265 V ac. The scalable supplies feature dual-bus outputs of 380 V dc, an efficiency of over 90%, a typical harmonic distortion of less than 5%, and an operating case temperature of –40° to 100°C. Other features include non-shutdown/auto-recovery overvoltage protection and a 14-V dc, 10-mA auxiliary supply. Measuring 5.06 by 2.00 by 12.53 in., the supply weighs 2.7 lb. It sells for $998. PM

***Power & Data Technology Inc.**, 81 Great Oaks Boulevard, San Jose, CA 95119; Stewart Novak (800) POWER-85; fax (520) 204-9799; e-mail: snowak@powerdatatech.com.*

CIRCLE 466

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Upgrades To IC Disty Site Include Links To DRAM Manufacturers

A redesigned web site aims to make it easier for users to get up-to-date information on the availability and pricing of ICs. In addition to a new look and access format, the RAMDEX site, operated by American IC Exchange (AICE), Aliso Viejo, Calif., now features the DRAM Manufacturers Center, which provides a direct link to the web sites of six DRAM manufacturers.

With some 5000 customers and industry analysts accessing the site every day, AICE reorganized it into sections for "Buyer Information" and "Analyst Information." The two key pages for buyers are "View Stock," which includes product listings, and the DRAM Manufacturers Center.

Visitors can expedite use of the site with its Portfolio feature. This allows you to specify the type of devices you are interested in, and then view a list of those devices on one page. The visitor can then click on the desired device and obtain detailed information, including charts and graphs. Selections can be saved for future use, at which time the page will present updated information on the selected devices.

Because of widespread international use of the site, AICE also added a "DRAM Currency" page, which lists the values of different currencies so international visitors can quickly convert U.S. dollar prices to their own currency. Other upgrades include new graphics and a more user-friendly home page.

The RAMDEX web site is at www.aice.com. Or call (800) 229-7690 for further information.

Enhanced IT Will Strengthen Components Distributor

Sager Electronics has added two information technology management positions as part of a multimillion dollar investment in enhanced IT infrastructure. Software improvements include PeopleSoft enterprise resource planning applications and supply-chain management software.

"The use of PeopleSoft will create business efficiencies, and give our personnel more time to work even closer with our customers and vendors," says Ron Lovell, Sager's director of information technology. Another new application, Optum's Move software, is a warehouse management system that should improve the efficiency and accuracy of Sager's distribution center operations.

To complement the new software, the company is enhancing its hardware and storage infrastructure, using Hewlett-Packard Unix servers, the disk-storage expertise of EMC^2, and the communications expertise of Cisco. The entire sales staff will be outfitted with PCs. "Our goal is to have the same access for everyone, no matter where they are geographically," says Lovell.

The new staff members are Shannon Freise, PeopleSoft implementation manager, and Guy Lochiatto, information technology operations manager.

Pioneer Adds FPGA And Power Supply Lines

Pioneer-Standard Electronics Inc. has added two diverse product groups to its family. The Cleveland, Ohio-based company has picked up Actel Corp.'s SX family of FPGAs, and Lambda Electronics Inc.'s ac-to-ac and dc-to-dc power products for North American distribution.

The Actel devices feature 4-ns clock-to-out speeds and 320-MHz maximum clock rates, allowing them to be used in applications from Gigabit Ethernet to 66-MHz, fully compliant, PCI designs. "We now will have the benefit of offering the SX device to a substantially broader customer base, with Pioneer-Standard distributing our new SX family," says Carl Burrow, Actel's vice president for marketing.

Lambda's products target OEMs, especially in the telecommunications, computer, office equipment, and industrial markets. "The addition of Lambda gives Pioneer-Standard one of the strongest supplier groups for power products in the distribution industry,"

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states Tom Pitera, president of the distributor's Electronics Div. Pioneer's Power Products Center, Fremont, Calif., offers engineering, design, integration, and assembly services.

PCMCIA Disk Drives Get National Distributor

Bell Microproducts has signed a national master distribution agreement to handle Calluna Technology Ltd.'s PCMCIA-based, 1.8-in. hard-disk drives. Calluna, which has its world headquarters and manufacturing facilities in Glenrothes, Scotland, redesigned its PC-card hard-disk drives to incorporate magneto-resistive technology and PRML coding.

"Calluna offers our customers a great opportunity to adopt high-capacity PCMCIA storage into innovative product designs for many mobile applications," says Phil Roussey, senior vice president of the San Jose, Calif.-based distributor. "Bell Microproducts is looking forward to the future products on Calluna's road map, and the exciting opportunities that will develop as customers implement Calluna technology in their product designs," adds Roussey.

Calluna, whose U.S. headquarters is in San Jose, currently makes 520-Mbyte, type III PCMCIA removable hard-disk drives in volume. Scheduled for release later this year are a 1.04-Gbyte type III drive and a 260-Mbyte drive that fits the type II form factor.

Components Distributor Opens Kansas City-Area Office

All American Semiconductor Inc. has opened a sales office in Overland Park, Kan. The office is headed by general manager Ron Lambert, who has 25 years of distribution experience in Kansas City and the surrounding marketplaces. "In order to increase our support to the valued customers of the Kansas City and surrounding tri-state area, and to further promote the products of our quality suppliers, we have opened this office with a group of talented industry veterans," announced Bruce M. Goldberg, president and CEO of the Miami-based firm. According to the company, they have moved up to become the seventh largest distributor of semiconductors, and the 14th largest electronic components distributor overall.

Commodity IC Distributor Adds Computer Peripherals

American IC Exchange (AICE) has expanded its charter from commodity ICs to include a Computer Products Div. that buys and sells peripherals for personal computers. Products offered include notebook computers, hard-disk drives, CD-ROMs, LCD projection panels, modems, and monitors.

AICE, based in Aliso Viejo, Calif., buys the excess supplies of these new, finished goods from OEMs. They then sell them to business buyers, such as value-added resellers, systems integrators, and corporate and government purchasing agents.

"Adding computer peripherals to our line-up provides a means for us to accelerate the growth of our company," says Jim Binford, head of the new division. "In addition, handling these type of products is a natural progression for AICE," Binford added.

Richardson Expands Its Power Tube Territory

Richardson Electronics Ltd., LaFox, Ill., has expanded its distribution agreement with Siemens Power Tube Div. to include territories outside of North America. Under the new pact, Richardson will sell Siemens power tubes in South and Central America, Singapore, Malaysia, Indonesia, the Philippines, and Thailand. Richardson is a highly specialized, value-added distributor of electron tubes, RF and microwave components, power semiconductors, display products, and CCTV and security equipment.

Avnet Moves Into U.K. Computer Business

Avnet Inc., Great Neck, N.Y., has acquired the business of U.K.-based Bytech Systems Ltd., which specializes in technical value-added distribution. Avnet chairman and CEO Leon Machiz says the acquisition strategically positions the company's Computer Marketing Group throughout the U.K., and provides the opportunity to expand Avnet's computer business to a new global market.

Compiled and edited by John Novellino, jnovellino@penton.com, (201) 393-6077.

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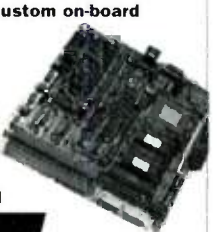

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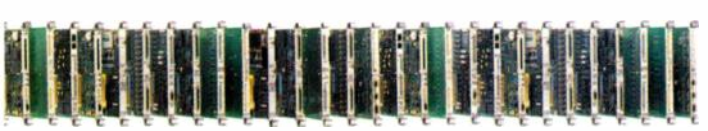

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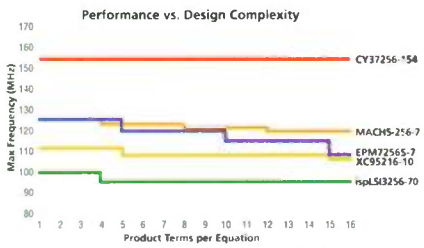

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