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ELECTRONIC DESIGN

TECHNOLOGY • APPLICATIONS • PRODUCTS • SOLUTIONS

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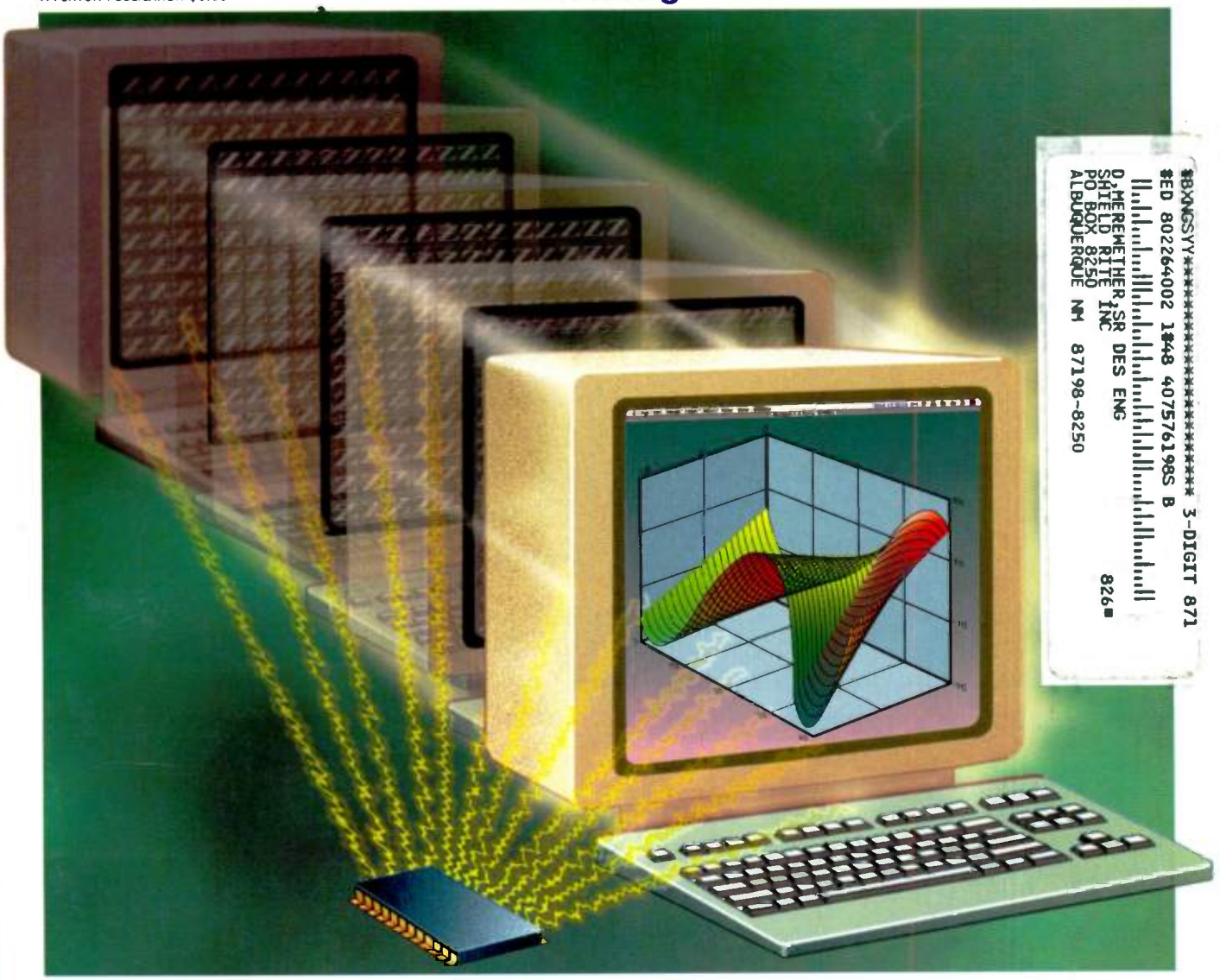

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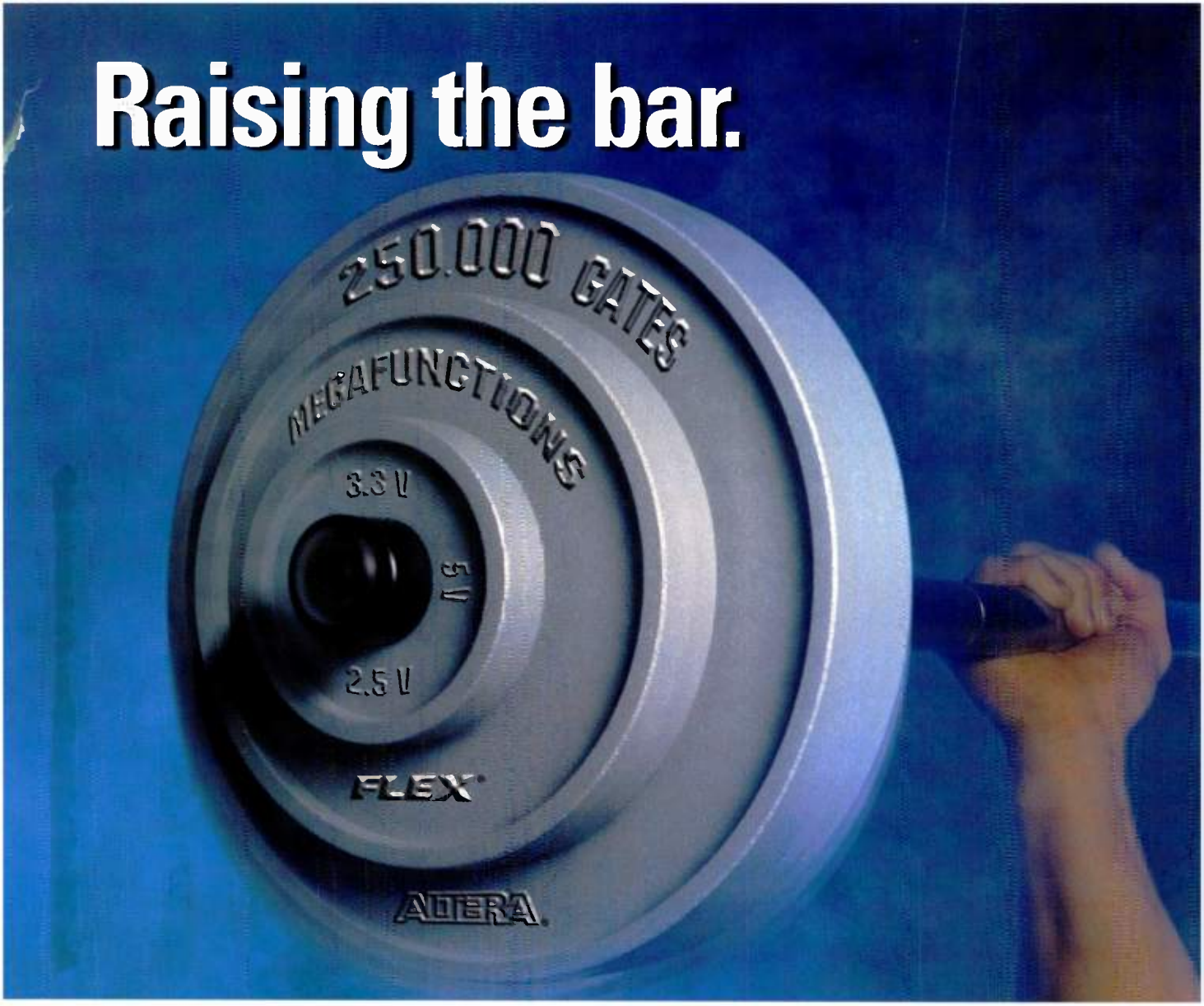
Raising the bar.



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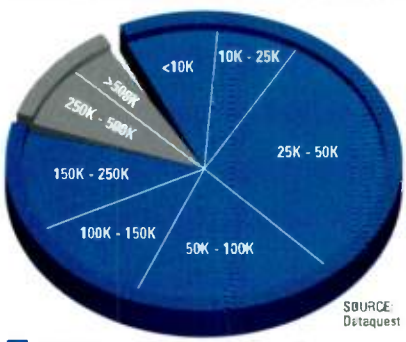

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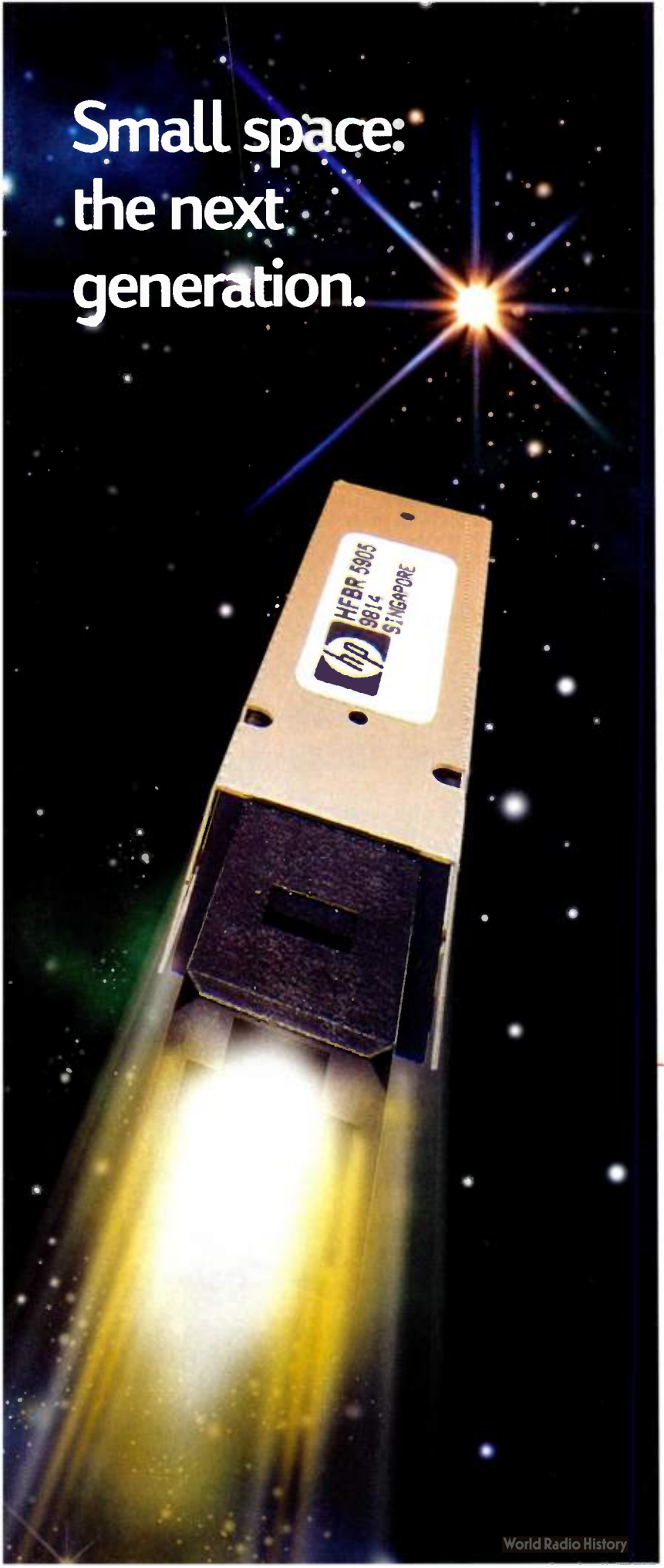

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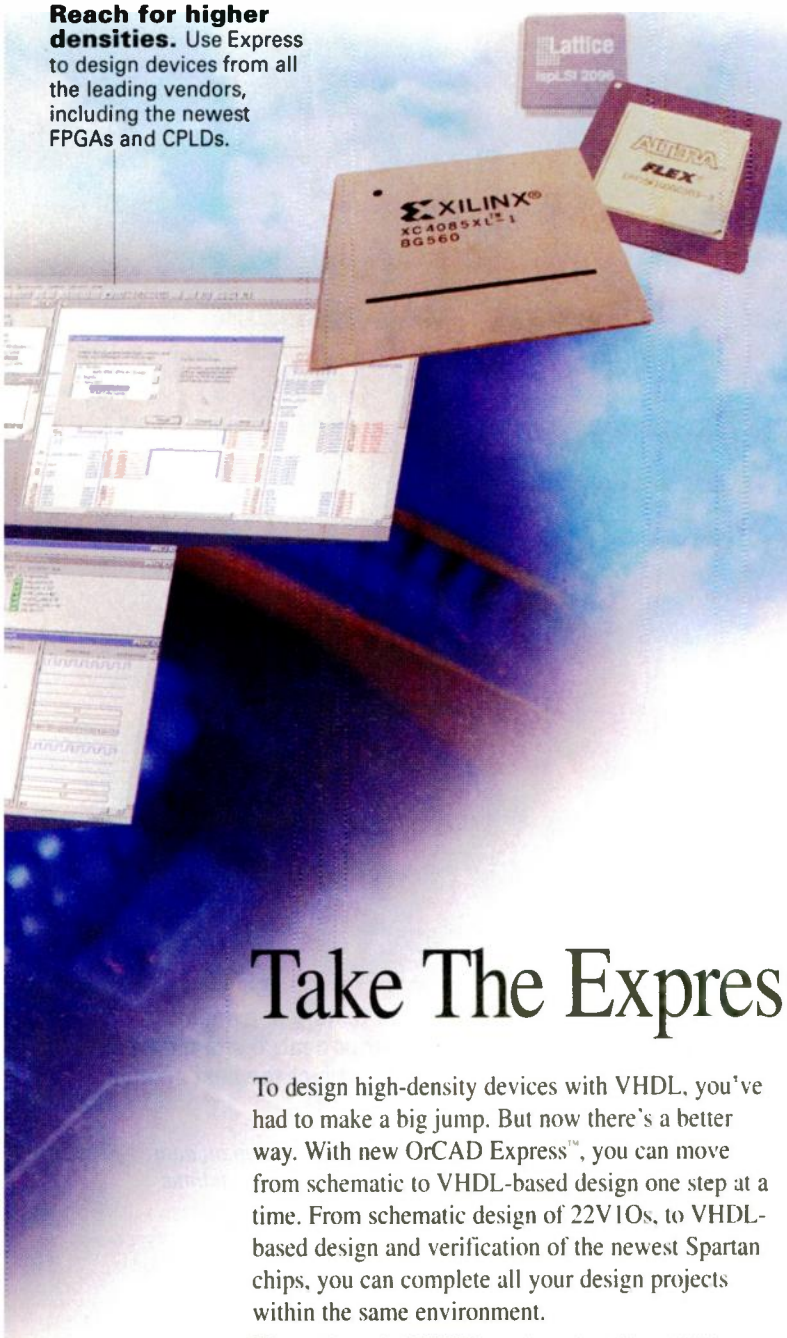

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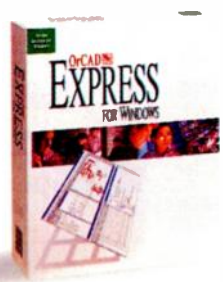

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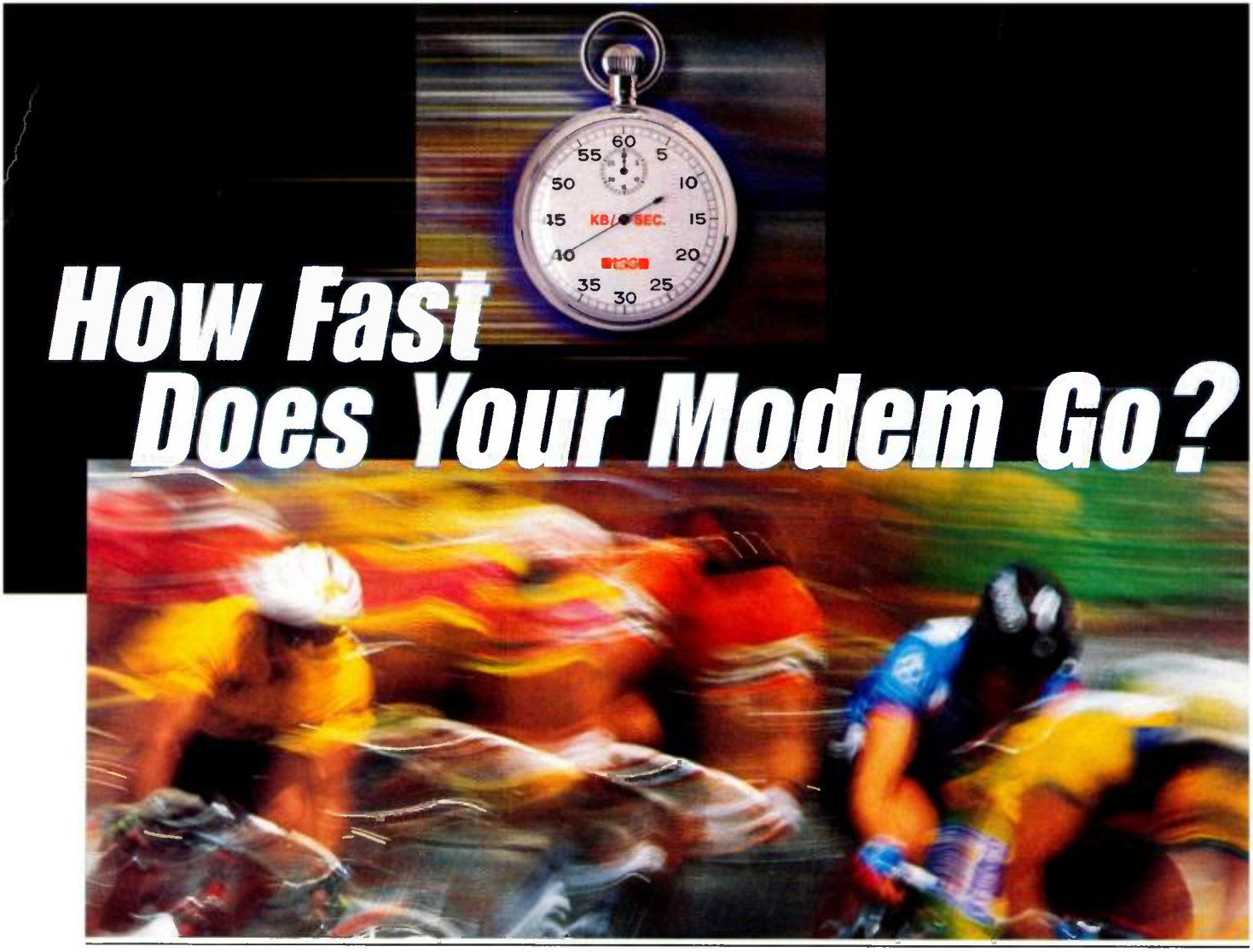

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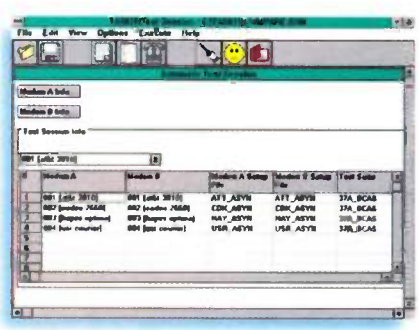

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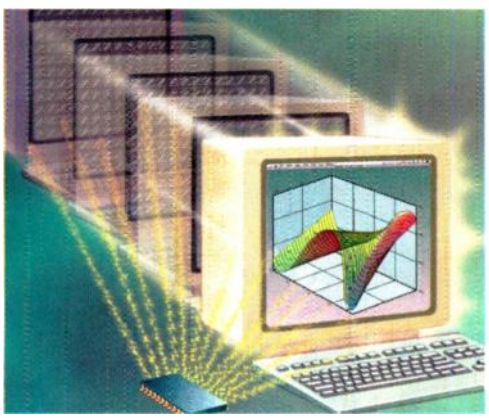

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- **Thin Displays Special Report:....** Contributing Editor Chris Chinnock previews what's ahead in small and medium-size flat-panel graphics displays. The special report will feature technology choices and major applications.

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Comprehensive listings of what **Electronic Design's** technology editors are working on, including:

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EDITORIAL

Here's Your Cubicle, Part II

I must always remember that when I ask for your opinion on a subject, I should expect to see a lot of e-mail. Wheew! My June 22 editorial sparked an explosion of passionate and very opinionated comments and life experiences. For those of you short on RAM, I asked for your thoughts on Congress' loosening of the restrictions placed on the number of immigrant high-tech workers because industry execs say that can't find enough homegrown talent.

Well, I heard numerous points of view. There were the former engineers who, like my uncle, were whacked during the "pension dump" of the '60s and '70s. Then, there were the foreign engineers who say that the problem is not immigrant engineers taking American jobs, but the dwindling number of American youths pursing engineering degrees, especially at the post-graduate level.

One Indian engineer said that all one has to do is look at the ethnic make up of engineering graduate schools. He also pointed out that the notion of the low-paid immigrant worker (engineer) is wrong, "I don't deny that there might be cases where someone might be misusing the H1 visa. But in my opinion, immigrant workers are paid the same money required by U.S. law."

Maybe if you're bagging fries at the mall you'll make the same money. But everyone knows that any CEO worth his suspenders plays the supply and demand game. If the supply of workers is high, you pay less. If the talent pool is low, you pay more. And, if you can attract top talent at a low or reasonable salary, you'll get a fat bonus and condo in Barbados as a reward if you meet earnings projections.

Shouted one engineer, "The immigration debate is TIRED! It's simple; companies are trying to avoid paying fair salaries for good engineers...and I'm not suggesting that every engineer make $100,000. But the reason for the so-called 'shortage' is because engineering is HARD, and it doesn't pay as well as competing disciplines."

The most heart-wrenching comments came from older engineers who were laid-off, or fired because in their opinions, their only fault was that they grew old and made a decent salary. One engineer blamed human resource departments whose first order of business is to look at the graduation date on a resume. On the other side, there were those who stressed that it's up the individual to continue to update their skills and tool kits so they because more "marketable."

We'll continue to explore the impacts of this issue. Keep those comments coming.

Tom Halligan
Editor-in-Chief
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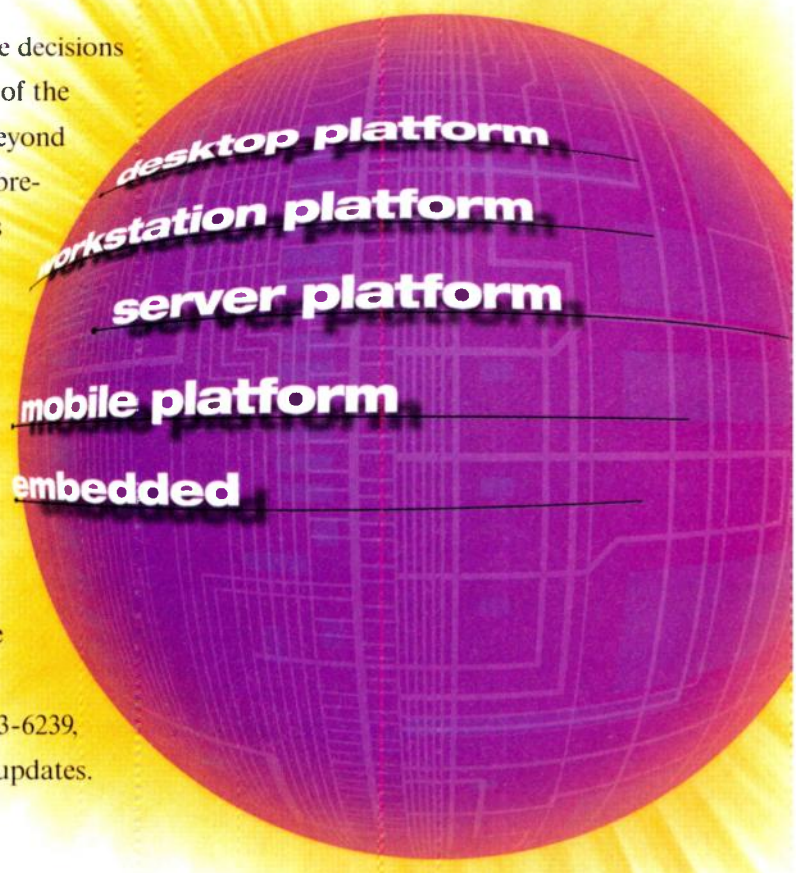

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Trade Off Density And Speed

The demand for ever-higher-density DRAMs has pushed memory manufacturers to migrate toward increasingly smaller feature sizes, moving DRAM densities from 16- to 64-Mbit chips and beyond. In previous generations' transitions—from 1- to 4-Mbit, and from 4- to 16-Mbit chips—significant gains in access time were achieved. These gains were due to reduced feature sizes and architectural enhancements that led to page, extended data out, and synchronous operating modes.

However, as DRAM densities extend to the 64-Mbit level, memory designers are not achieving the same performance gain on the access time as they achieved when they moved from generation to generation in past years. Improvements of 10% to 25% are not acceptable any more as processor clock speeds move ever upward. Part of the problem is the higher density itself. The long word and bit lines that criss-cross the memory chips at the 64-Mbit level and higher are loaded down by the large number of memory cells in the storage array. The capacitive loading and high resistance of the long lines combine to negate some of the performance gains from the finer-line processes.

Although most DRAM manufacturers are currently shifting production of 64-Mbit memories to 0.25-µm processes, which will be used for the next-generation 256-Mbit memories, many of the companies find that the 256-Mbit devices are not very cost-effective. In some cases, they operate slower than the 64-Mbit memories. Thus, one alternative to blindly following the 4× density growth is to take a half-step back, and create a 2× memory density option—a 128-Mbit memory chip. Such a chip, fabricated on the same 0.25- or 0.20-µm process can be cost-effective, and will not suffer as much from the loading effects. Several manufacturers, including Toshiba America Electronic Components Inc., Irvine, Calif., plan to release such chips later this year.

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DIGITAL ICs

Of course, finer-line processes in the 0.20- to 0.18-µm arena will allow full-256-Mbit chips to be fabricated, while even smaller-geometry processes will yield cost-effective 512-Mbit chips. As the chips grow denser, word width must also increase, otherwise memory increments at the system level could become a little unwieldy. Therefore, many manufacturers consider releasing a 32-bit-wide SDRAM option. If they choose that direction, the SDRAM could start to compete with synchronous-graphics memories for budget-priced graphics subsystems. Designers are also considering a 64-bit-wide SDRAM interface as an option, mostly at the 128-, 256-Mbit, and higher densities. Experimental chips with 64-bit buses have already started to appear in conference papers.

At this past June's IEEE Symposium on VLSI Circuits, designers detailed several new DRAM architectures that promise to dramatically reduce the access time, and provide high data bandwidth, all without the overhead associated with pipelined memories. One approach, described by Fujitsu Ltd., Tokyo, Japan, in a 1-Mword by 64-bit (or 2-Mword by 32-bit) experimental fast-cycle DRAM (FCDRAM) eliminates the multiplexed address inputs, allowing all address bits to be loaded simultaneously. Additionally, the internal circuits have an automatic reset capability that provides for continuously pipelined operation. This feature eliminates the memory array's having to set aside a specific time to reset the circuits. Thus, the reset cycle is hidden, and the memory can achieve a random cycle time of just 20 ns. This figure is more than twice as fast as standard DRAMs, and it's actually less than the access time, 26 ns.

Such fresh thinking is just what the memory industry needs to keep pace with advances in CPU throughput And, more innovations are yet to come as new products such as the synchronous-link DRAM, and still other architectures emerge from R&D. *dbursky@class.org.*

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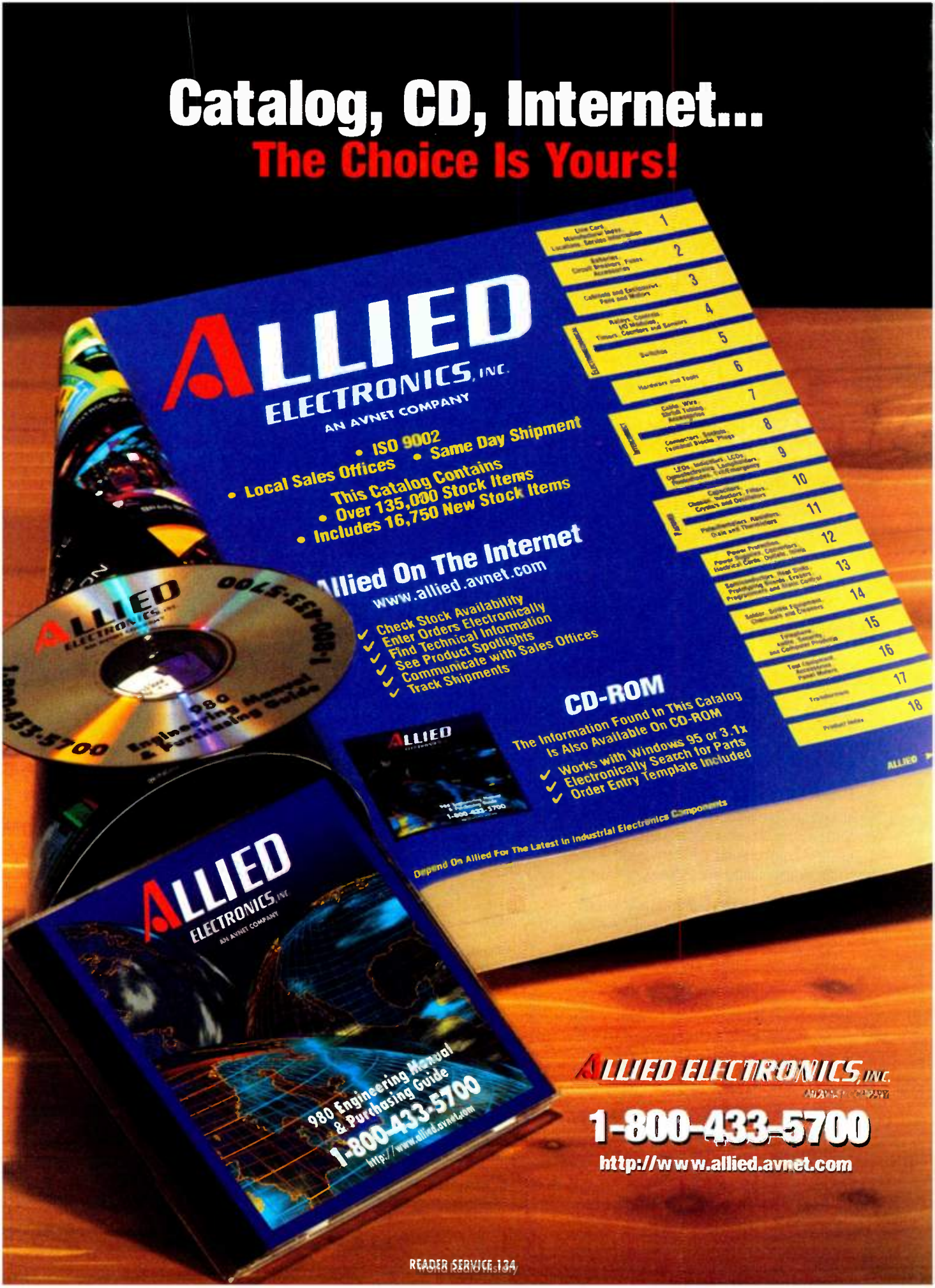

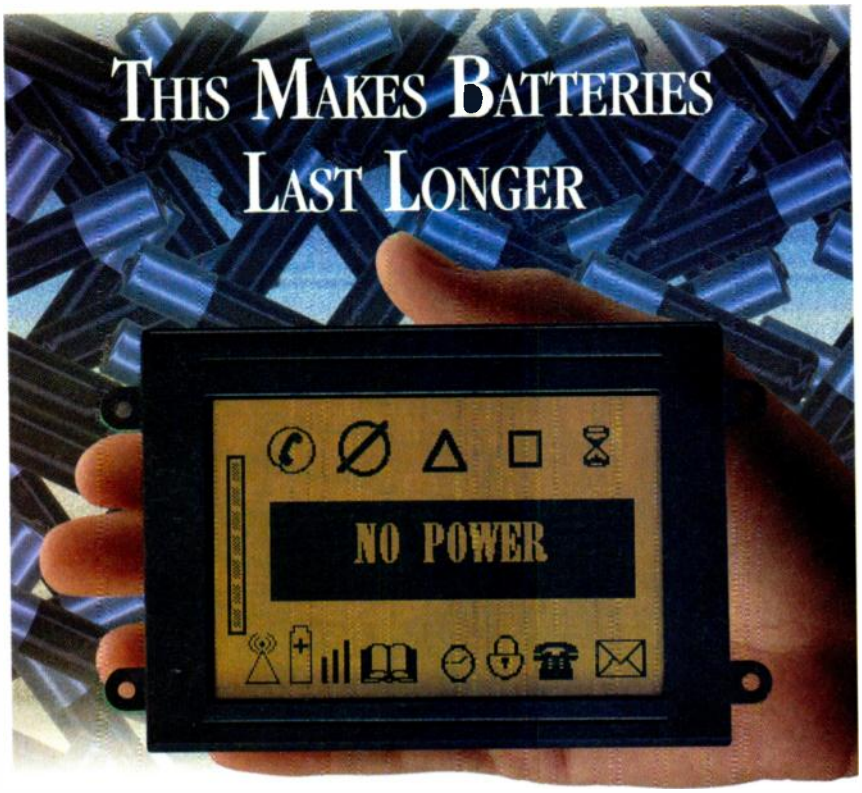

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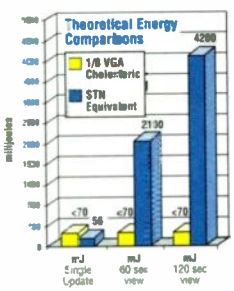

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Tektronix Voluntarily Recalls TDS210 And TDS220 Oscilloscopes

Tektronix has voluntarily recalled its model TDS210 and TDS 220 oscilloscopes. According to the company, certain incorrect use of the products could cause the ground connection to fail. The company is not aware of any injuries to users, although it has received reports of situations where the ground lead on an oscilloscope has opened when the product was used incorrectly. A failure of the ground connection could expose the user to risk of serious personal injury or death.

If a user incorrectly connects a probe ground lead to a voltage source or incorrectly touches the ground ring near the probe tip to a voltage source, a circuit board trace in the oscilloscope's electrical ground path may open. Once this occurs, the product may still appear to function normally. However, the oscilloscope is no longer properly grounded. Subsequent use of the scope could then result in a serious electrical shock to the user.

Tektronix is conducting a voluntary recall to prevent this possibility of injury to its customers, and is part of the company's overall commitment to providing reliable, safe, and high-quality products. This recall applies to approximately 60,000 TDS210 and TDS220 units with the following serial numbers: for the TDS210, serial numbers below BO49400 or CO10880; and for the TDS220, serial numbers below BO41060 or CO11175.

Tektronix is asking customers to stop using the scopes in question immediately and to contact the company to receive instructions on how to return the scope for modification. Customers should not assume the oscilloscope is properly grounded even if it appears to be functioning properly.

Customers can receive instructions for returning the product by contacting Tektronix at 800-835-9433, ext. 2400, in the U. S.; *www.tek.com/measurement*. International TDS200 recall information can also be found on the web. JD

Residue Removal Is Environmentally Friendly

A new ozone gas process for the removal of photoresist and organic post-etch residues from wafer surfaces has been announced by IMEC, Leuven, Belgum, one of Europe's leading centers for microelectronics research. The new environmentally friendly process provides an alternative to the use of harmful solvent strippers and eliminates the need for various sulphuric acid-based process steps in IC production.

In the new process, wafers are exposed to a moist ozone (O_3) environment and then spiked, if appropriate, with an additive. Oxidation efficiency is further enhanced by maximizing the ozone concentration at elevated temperatures, while controlling the wet boundary layer on the wafer surface. The moist atmosphere produces a thin condensation layer on the wafer, which maintains a continuous concentrated supply of O_3. This process results in complete resist layer removal in less than ten minutes.

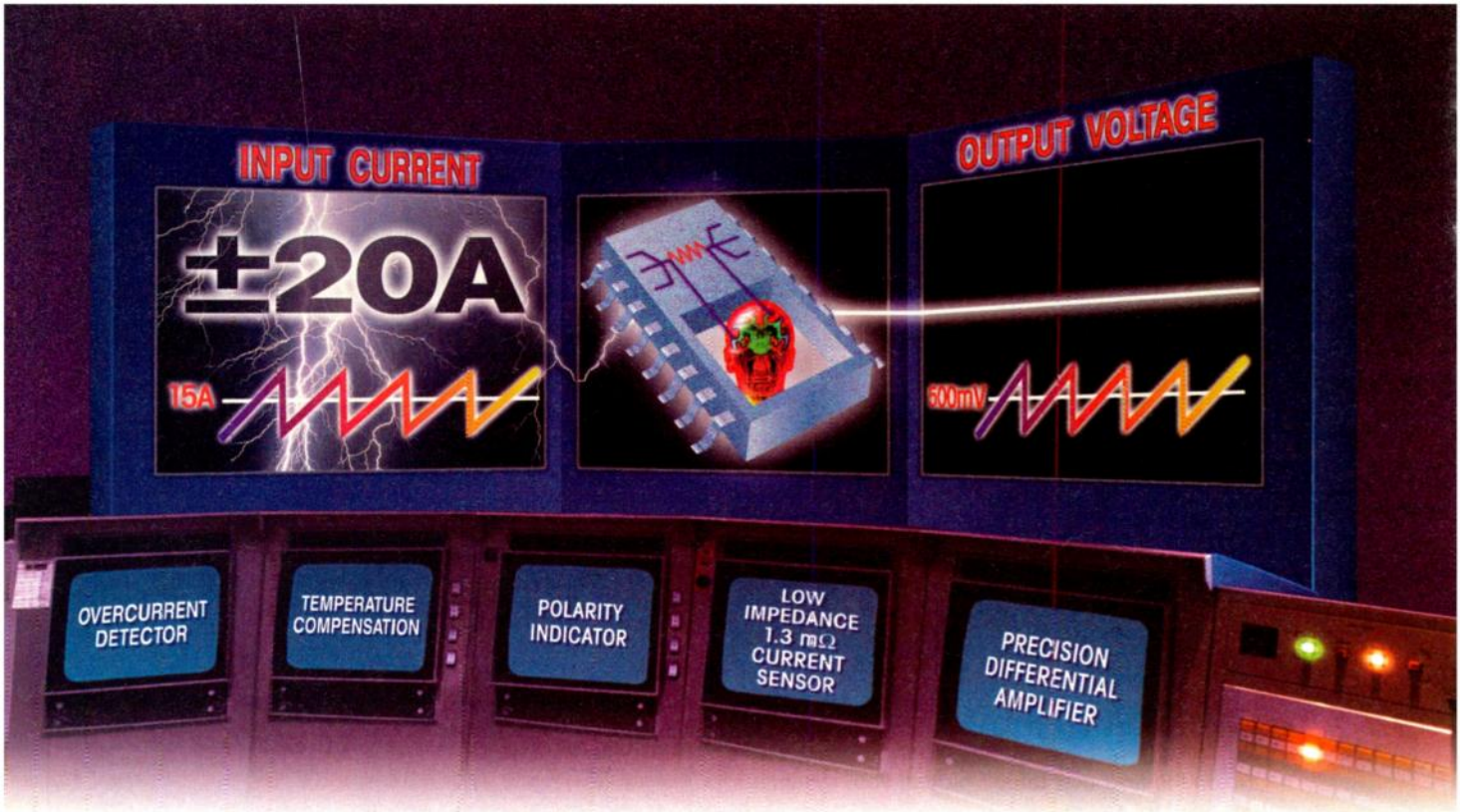
For further information, please contact either Barbara Kalkis in the U.S. at (408) 996-9975; e-mail: *kalkis@compuserve.com.* LG

UPS Manufacturer Implements Battery-Recycling Program

MGE UPS Systems, Costa Mesa, Calif., manufacturer of a broad range of uninterruptible power supplies, recently introduced Green Sweep, the company's innovative recycling program for UPS batteries. The first of its kind, MGE's Green Sweep will facilitate the secure disposal of any 3-kVA and up UPS batteries—regardless of manufacturer. Because UPS batteries contain lead and sulfuric acid, they're considered a biological hazard and are illegal to dispose of without the guidance of the Environmental Protection Agency.

Traditionally, when a UPS battery has reached the end of its life, users are required to spend time and money hunting for an authorized recycling or disposal solution. More often than not, batteries are thrown away with common refuse—a dangerous and potentially illegal activity. Through Green Sweep, MGE has an EPA-approved recycler that picks up UPS batteries free of charge at MGE's facility in Costa Mesa. The only fee incurred by the user is the battery's shipping charges to MGE.

Contact MGE UPS Systems, 1660 Scenic Ave., Costa Mesa, CA 92626; (800) 523-0142; fax (714) 557-3256; e-mail: *info@mgeups.com.* PM



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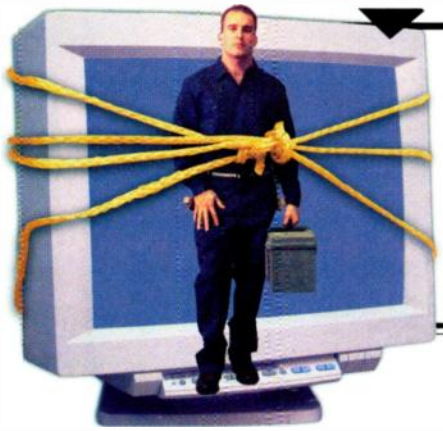

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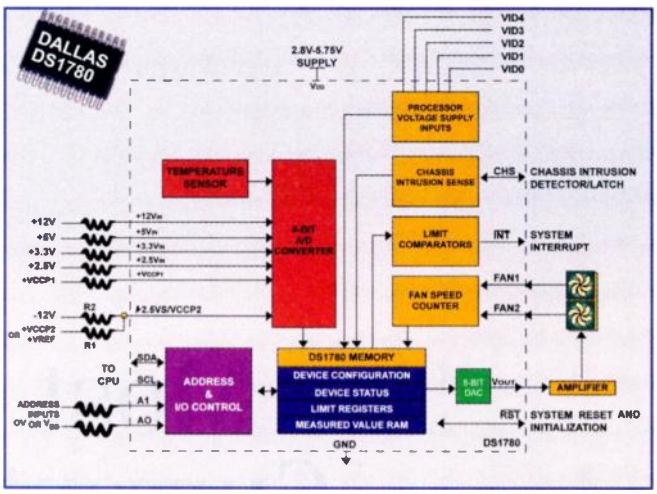

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Cheaper Electrical Power On The Way Via Silicon-On-Insulator Electronics

Recently developed silicon-on-insulator (SOI) devices may hold the key to making electricity produced from geothermal energy more cost-effective. Because SOI components and systems do not use conventional, semiconductive bulk silicon, leakage current is much lower, and the electronics can work in high-temperature environments. On-going experiments with SOI devices by researchers at Sandia National Laboratories, Albuquerque, N.M., may point the way to sharply reduced costs for geothermal electrical energy, and greatly increase its use in the U.S.

Current methods of geothermal electrical conversion involve the use of electronics and batteries that, along with any associated instrumentation, must be encased in dewar flasks to protect them from temperatures up to 350°C in geothermal wells. SOI-based electronics may offer a less-expensive solution by eliminating the need for the dewar flasks in the wells. Because geothermal wells account for approximately one-fourth to one-half the cost of a geothermal power plant, the total cost reduction could make geothermal generation more practical.

The Sandia researchers are experimenting with the Honeywell HT83C51 SOI processor, which includes 32 kbytes of RAM. But the harsh environment in which it must operate makes testing of the device a challenge, prompting researchers to develop new methods of assembly and support for hardware. Tests of the microprocessor circuit, for example, required that the ICs be hard-wired onto a ceramic board using laser-welded connections. This was necessary because standard printed-wiring boards do not exist for use at these temperatures, and common solders melt at between 180°C and 250°C.

Testing of electronic components for function and performance at various temperatures in an actual geothermal well is impractical. Instead, they must be tested in a high-temperature oven in one of the laboratories at Sandia's Geothermal Research Department. To accomplish this, instruments on the outside of the oven are connected by ceramic insulated wires to the electronic devices being tested. To date, the longest temperature run of Sandia's microprocessor circuit at 300°C, has been 72 hrs. The only interruption to the test came when the researchers needed to cool the oven to add new experiments. The same electronic devices have logged 2500 hrs at 250°C, over a period of months.

Sandia researchers are also evaluating and designing new electronic instrument systems that can operate at up to 315°C—more than 100° hotter than systems presently available to the geothermal industry. Systems that are in development include a high-temperature battery that can function without the need for thermal isolation, and a dewarless data logger.

The geothermal energy experiments at Sandia are part of an ongoing project funded by the Department of Energy's Office of Geothermal Technologies. If successful, the development and use of high-temperature electronic components may very well spill over into a number of different electronics-based applications such as monitoring and testing in high-temperature environments or in any application where electronic components are required to operate at temperatures above 300°C.

For more information on this project contact Sandia's media relations department at (505) 844-8066 or check its web site at www.sandia.gov.

Cheryl Ajluni

SLDRAM Prototype Complete, Door Now Open For 800 Mbytes/s Memory

A consortium of companies, including major computer manufacturers and many of the world's top computer memory producers, were eager for a new device. They commissioned it, and were rewarded with the Synchronous Link DRAM (SLDRAM), which features a high-speed interface of 400 Mbits/s per pin. The result is a single chip with a total data transfer rate of 800 Mbytes/s—eight times faster than current synchronous DRAM technology.

Because the memory, designed by MOSAID Technologies Inc., will be an an open standard, consortium members will be able to create their own SLDRAM products based on the technology. The consortium, known as SLDRAM Inc., includes IBM, NEC, Texas Instruments, and Toshiba among its members. Prototypes of the chip are expected to be available for testing by the end of summer.

To maximize performance, computer microprocessors must work in tandem with similarly fast memory technology. The challenge for DRAM chip makers is to achieve ever-higher performance without significant cost penalties—such as larger die sizes. Currently, computer manufacturers feel an intense market pressure to reduce retail prices.

A major feature of MOSAID's SLDRAM design is an "adaptive interface." By automatically adjusting the times at which data is sent, this interface meets the demands of systems that require levels of accuracy measured in fractions of a nanosecond. Without such a feature, the costs of building the chips—and the systems that use them—escalate considerably.

This key technique of making the chip adjust and calibrate its own timing had its genesis in MOSAID's other business line, engineering test systems for memory chips. Self-calibration is the standard way to set the timing accuracy for the company's chip testers. With the SLDRAM design, the technology is within the design of the chip itself.

For more information, contact Brenda Adams at Mosaid Technologies, (613) 599-9539 ext. 1205; www.mosaid.com. For more information about the SLDRAM consortium, check out www.sldram.com.

In other DRAM news, Ramtron International Corp., Colorado Springs,

Colo., announced the approval of its enhanced synchronous DRAM (ESDRAM) product definition. The JEDEC Memory Subcommittee has accepted the ESDRAM as a superset to the SDRAM memory standard. Developed and marketed by Ramtron's wholly owned subsidiary, Enhanced Memory Systems Inc., Colorado Springs, Colo., the ESDRAM is an ultra-fast version of the synchronous DRAM.

The new ESDRAM and double data rate (DDR) ESDRAM superset addresses system companies' demands for extended functions, such as lower DRAM latency. At the same time, the superset maintains compatibility with the JEDEC SDRAM and DDR SDRAM standards.

The JEDEC Memory Subcommittee ballot approval for the ESDRAM superset is the result of more than a year of work by the standards organization's DRAM committee and Enhanced Memory Systems. The DRAM committee membership includes all major industry DRAM suppliers and many leading computer systems companies. The approved ballots have been forwarded to the JEDEC council for final resolution and action.

For more information about JEDEC, and to access JEDEC standards online, visit www.eia.org/jedec. For additional information regarding Enhanced and the ESDRAM products, contact Enhanced Memory Systems, 1850 Ramtron Dr., Colorado Springs, CO 80921; (800) 545-3726; fax (719) 488-9095; www.ramtron.com.

Jeff Child

Enhanced PowerPC Architecture Delivers Vector Processing, Wider Internal Bus

In a major architectural upgrade to the PowerPC processor, designers at Motorola Inc., Austin, Tex., have revamped the CPU's internal bus structure to handle 128-bit-wide data transfers. They've also added a highly configurable and programmable vector-processor block to accelerate compute-intensive algorithms. The upgraded CPU, to be sampled later this year, intends to boost the performance of demanding applications such as graphics, video, digital-signal processing, and image processing. Dubbed the AltiVec, it's the first enhancement to the PowerPC architecture since its introduction in 1991. The device also will be the first produced by Motorola using its HiP 5, 1.8-V, high-performance copper-interconnect process.

The vector unit is a 128-bit-wide processing block that operates concurrently with the existing integer and floating-point units *(Fig. 1)*. But it is optimized for use with large arrays of data rather than sporadic, single-word com-

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68HC705C9A	16K	352	31	40-DIP, 44-PLCC, 44-QFP
68HC705J1A	1.2K	64	14	20-DIP, 20-SOIC
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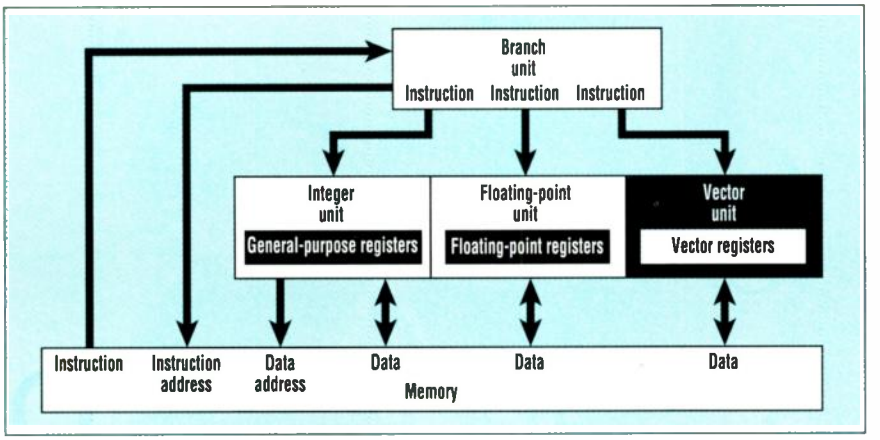


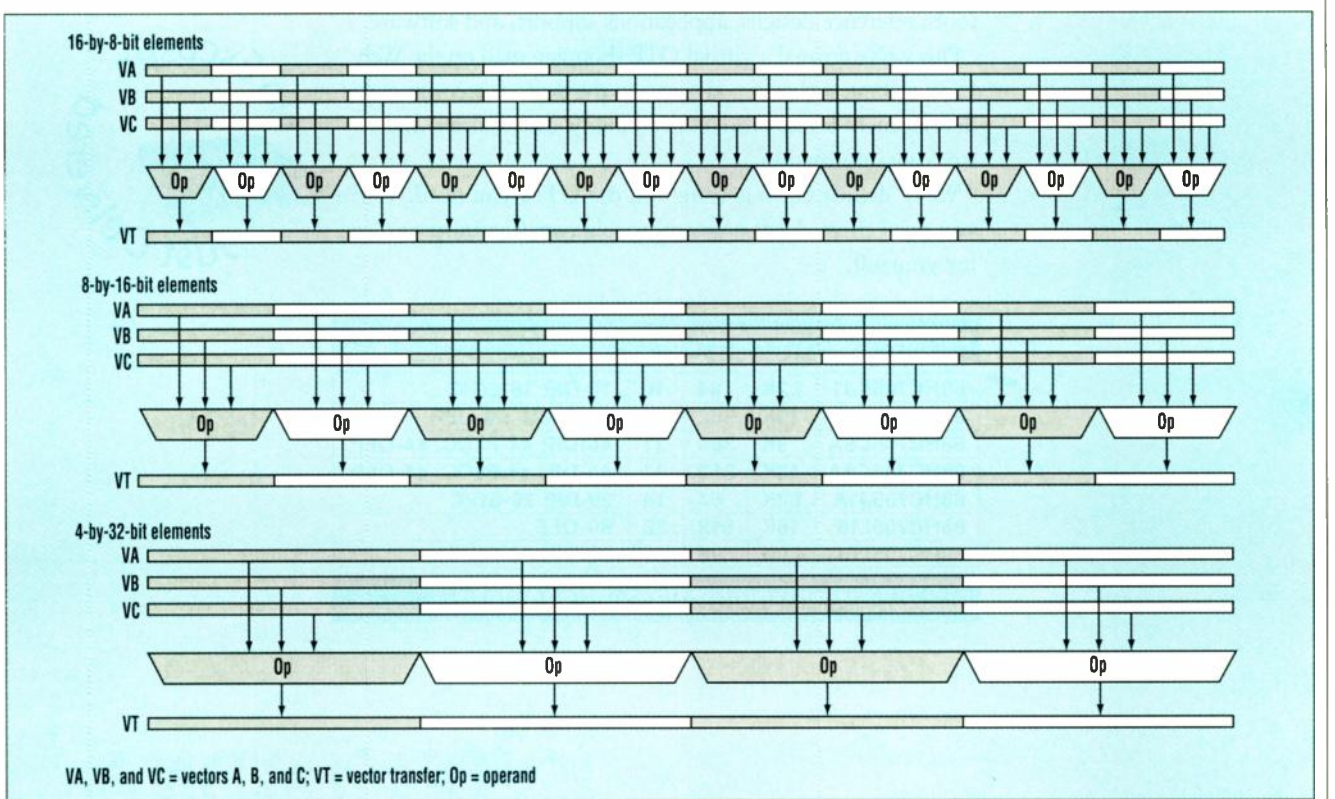
1. The vector-processor unit added to the PowerPC architecture in the AltiVec upgrade is optimized for use with large arrays of data, rather than for sporadic single-word computations. The unit operates concurrently with the existing integer and floating-point units.

putations. The unit has 32 dedicated registers, each 128 bits wide. These registers supplement the 32 32-bit registers in the PowerPC integer processor, and the 32 64-bit registers in the CPU's floating-point unit.

Although the vector unit has a 128-bit-wide arithmetic unit, computations are typically performed on either four 32-bit words (signed and unsigned integers or IEEE floating-point numbers), eight 16-bit words, or 16 8-bit words simultaneously. This design improves overall computational throughput by a factor of four to 16, depending on the data width, versus a single 32-bit arithmetic logic unit (ALU) *(Fig. 2)*. In addition to subdividing the ALU into a single-instruction, multiple-data (SIMD) processor, the vector unit offers many other powerful capabilities.

The 128-bit-wide register file, for instance, holds the data vectors for the execution units. What's more, the 162 new instructions offered by the vector unit can specify up to three source operands and one destination operand. Additionally, the new instructions provide programmers with powerful commands that will greatly reduce computation time for various algorithms. For example, a 1024-point complex fast-Fourier transformation can be completed in less than 30 µs. Also, the enhanced PowerPC can execute H.263 video-conferencing algorithms two to four times faster than the C6x DSP chip from Texas Instruments, and run GSM algorithms more than twice as fast as the DSP chip.

One group of the new instructions falls into a category Motorola calls intra-element arithmetic operations. These commands allow programmers to perform independent parallel computations on the elements contained in the source vector registers, and place the results in the corresponding fields of the destination vector registers. The ALUs can perform addition, subtraction, multiplication, and multiplication-addition tasks. Additional commands in this group include instructions to find minimum, maximum, and average values, as well as conversions between 32-bit floating-point and integer formats.



2. The arithmetic unit in the vector processor is highly configurable. Designers can set it to process four 32-bit words, eight 16-bit words, or 16 8-bit words in parallel, thus accelerating compute-intensive algorithms by four to 16 times compared with a standard PowerPC.

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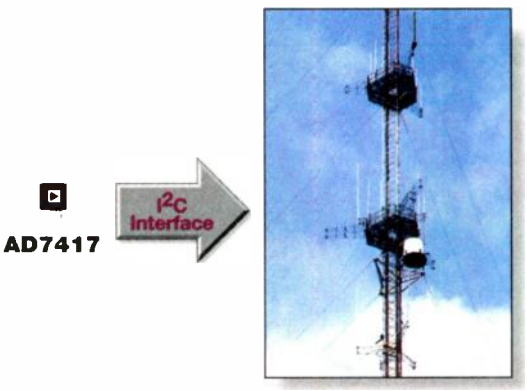

To Communications

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AD7816	N/A	SPI	±2	3.0 µW @ 10 SPS	1.30	SOIC, µSOIC	8
AD7417	4	I²C	±1	0.2 mW @ 1 kSPS	2.95	SOIC, TSSOP	16
AD7817	4	SPI	±1	3.0 µW @ 10 SPS	2.95	SOIC, TSSOP	16
AD7418	1	I²C	±2	0.2 mW @ 1 kSPS	2.25	SOIC, µSOIC	8
AD7818	1	SPI	±2	3.0 µW @ 10 SPS	2.25	SOIC, µSOIC	8

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Also available are intra-element, non-arithmetic operations that include various forms of compare, shift, and rotate instructions. Logical operations such as AND, OR, NOT, XOR, and AND-NOT are supported. There also is a Select instruction, which was designed to choose source data from one of two source registers and transfer that data to the results register. The combination of compare and select operations provides a powerful way to mask and replace data elements across the entire 16-byte field of vector registers using very few instructions.

Several specialized vector instructions were also created to speed up inter-element computations such as sum-of-products and sum-across commands. These instructions allow for elements within a single vector register to be summed in combination with a separate accumulation register. This is a very efficient approach for generating dot products (a common vector operation).

In addition to inter-element math operations, the vector unit includes several highly efficient, non-arithmetic operations that consist of wide-field-shift commands and pack and unpack operations (including a special instruction to handle the 1/5/5/5 pixel format common for 16-bit color pixels). One of the most powerful commands in this group is the Permute operation, which allows the vector unit to set up a byte-wide crossbar. This crossbar can arbitrarily select any 16 8-bit elements from 2-by-16 8-bit elements (two 16-byte source registers), and send the result to a single 16-byte destination register.

Such a capability reduces the overhead for operations where 8- and 16-bit data items must be reorganized in memory before or after computations. In many instances, a single Permute command can operate on 16 bytes of data, and replace four or five operations per byte using a traditional RISC or DSP engine. Merge operations are also available. They allow data to be interleaved at the byte, halfword, and word level.

The new commands available as part of the AltiVec architecture make the forthcoming PowerPC processors well suited for applications in Internet-protocol telephony gateways, multichannel modems, speech-processing systems, echo-cancellation systems, image- and video-processing systems, scientific-array processing, and network infrastructure hardware, like Internet routers and virtual-private-network servers. The enhancements also allow the PowerPC processor to accelerate many common time-consuming operations, like memory copies, string compares, and page clears.

To leverage the parallel computation capability available in the AltiVec enhancements, designers at Motorola have developed a standardized set of C and C++ language extensions. These extensions allow software developers to use their preferred C/C++ development environment and language syntax while explicitly taking advantage of the parallel functional units and other capabilities of the AltiVec additions.

For more information, check out the Motorola web site at motorola.com/altivec, or call (800) 845-6686.

Dave Bursky

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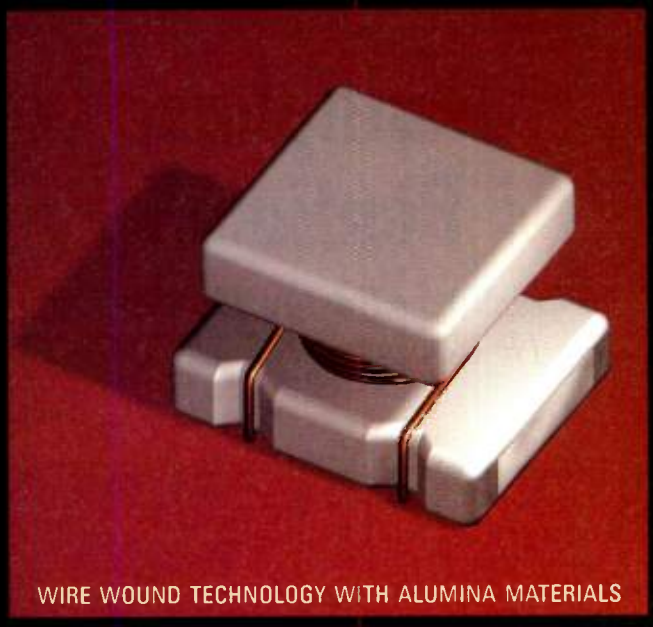
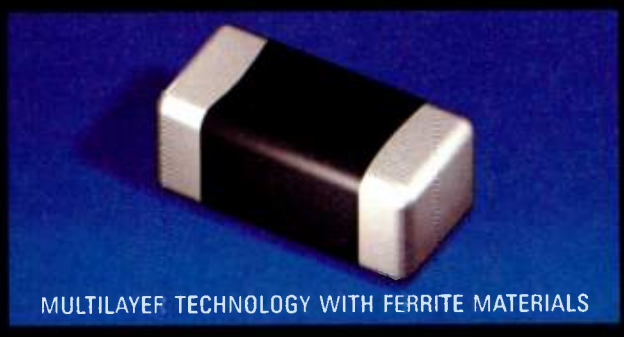
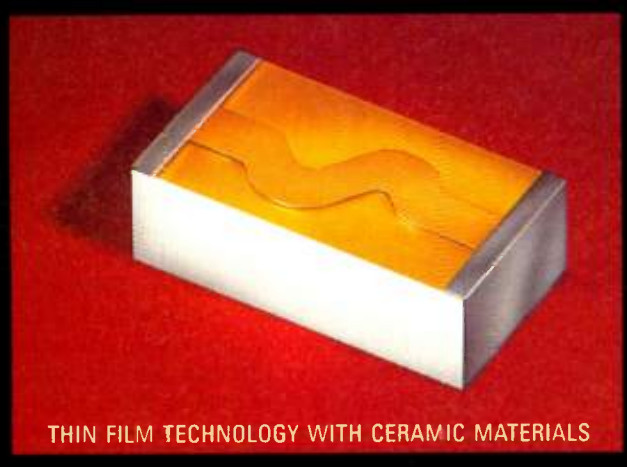
MULTILAYER TECHNOLOGY WITH CERAMIC MATERIALS



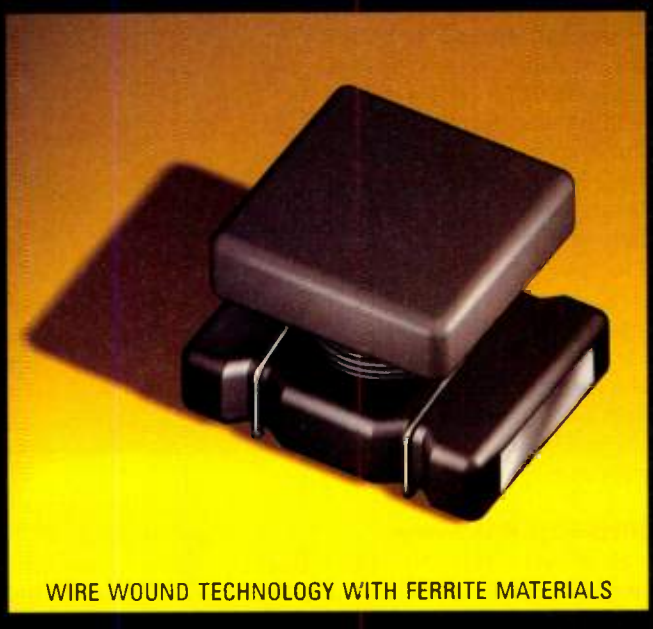
WIRE WOUND TECHNOLOGY WITH ALUMINA MATERIALS



MULTILAYEF TECHNOLOGY WITH FERRITE MATERIALS



THIN FILM TECHNOLOGY WITH CERAMIC MATERIALS



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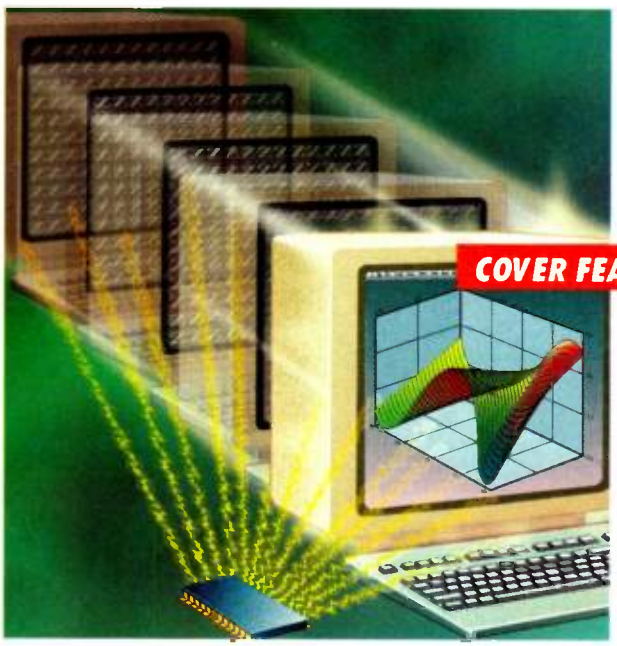
Multiphase Controller Meets Pentium's Power Demands

This Novel Design Enables Low-Cost, Compact, Programmable Dc/Dc Converters With Ultra-Fast, Transient-Current Response.

Ashok Bindra

As microprocessor architectures begin to tackle more tasks in a shorter time, voltage and current requirements grow more stringent. To power such advanced microprocessors in the latest computer desktops, servers, and workstations, the dc/dc converters must be swift enough to handle the load transient-current response required by the latest Pentium IIs and beyond. Besides responding in a flash, these voltage converters must also possess the ability to deliver high power from a smaller space. To comply with Intel's advanced specifications for new-generation Pentiums, they must also provide output voltage which is both accurate and programmable.



Ultra-Fast Recovery

Semtech Corp., Newbury Park, Calif., has crafted a multiphase pulse-width-modulated (PWM) controller, called the SC1144. This controller enables programmable dc/dc converters to have a fast response. The converters are also packaged smaller and remain compliant to Intel's specifications. The device satisfies advanced Pentium demands for step increases from 5 to 20 A in 500 ns at a slew rate of 30A/µs (*Fig. 1*). Able to provide the drive for selectable one- to four-phase operations, the SC1144 simplifies the construction of multiphase buck dc/dc converters to obtain desired speeds and precision. In addition, the SC1144's on-chip, 5-bit digital-to-analog converter (DAC) allows programmable output voltage that ranges from 1.3 to 2.05 V in 50-mV increments, and 2.0 to 3.5 V in 100-mV steps. "Aside from ultra-fast transient response, the multiphase scheme achieves the smallest possible circuitry," says Trevor Newlin, principal design engineer at Semtech.

The multiphase controller distributes equally large current between the four PWM generators and its corresponding inductors. Consequently, the multiphase technique generates four precise output voltages, which are 90° apart in phase (*Fig.2*). The four digitally phase-shifted outputs are then summed together to obtain the desired output voltage at the intended current rating.

By equally distributing the current, the heat is well spread amongst the components. This eliminates the need for large, bulky inductors and other passive components. Reducing the stress and heat on the output components eliminates the need for heat sinks, thereby solving thermal management problems. A conventional, single PWM controller, by comparison, will employ large components with appropriate heat sinking to handle currents as high as 20 A. Switching from the sleep to the dynamic mode in about 1 µs further aggravates this problem in conventional power solutions. Semtech attributes the precise current sharing among the four output phases to clever circuit techniques, as well as the trimming of critical elements.

The programmable multiphase PWM controller, according to Semtech, incorporates a high-speed, transconductance-based error amplifier to achieve faster transient recovery time. Newlin notes that, in this controller, the design of the error amplifier and the associated feedback mechanism contributed significantly toward improving the transient load response time. "The error amplifier's feedback tech-

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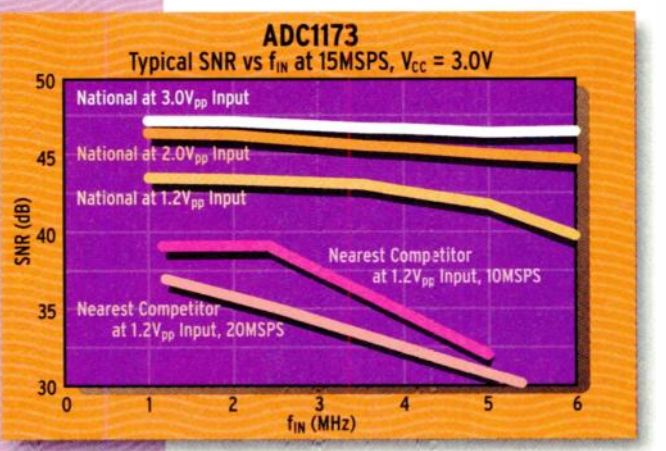

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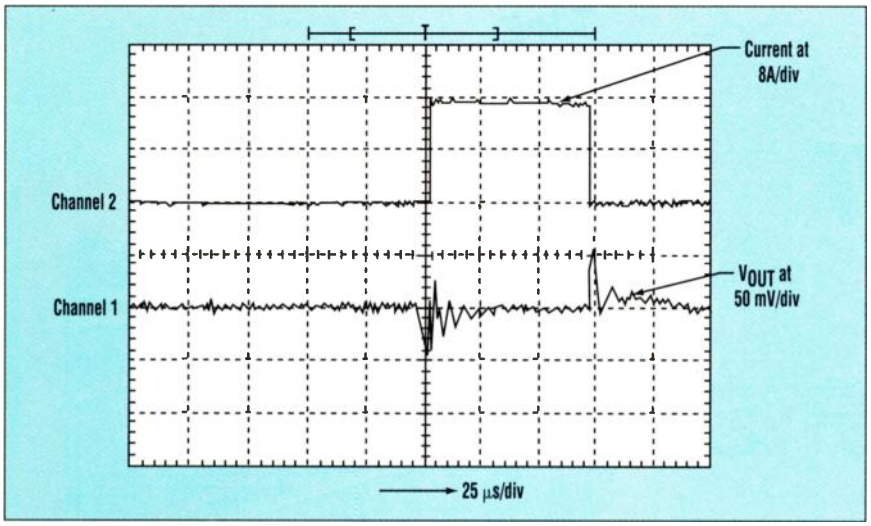


1. Semtech's SC1144 multiphase PWM controller offers ultra-fast transient recovery time. The top curve shows output transient current response when subjected to a slew rate of 30 A/μs. The bottom curve indicates that the transient voltage error is below 100 mV p-p.

nique is so good that the performance is far beyond the Intel specifications," adds Newlin. In fact, Semtech claims that the PWM controller's fast response time will easily support the transient needs of the upcoming 64-bit Merced processor. For precision, the amplifier features a high, open-loop gain of 10,000. However, its compensation RC network at the output attenuates the high-frequency gain for stability, according to Newlin.

The error amplifier also serves as a summing unit for the DAC section. The amplifier's output voltage is set by the bandgap reference, which provides a stable 2.05 V. When the bandgap goes out of regulation, the Enable signal shuts it down. To ensure that the multiphase controller wakes up without overshoot, the error amplifier is externally initialized using a soft-start capacitor. This feature protects the low-voltage microprocessor.

This technique provides dc/dc converters with excellent load regulation. As per Semtech's data sheets, the worst-case no-load-to-full-load regulation is under 10 mV. Also, the input ripple current is reduced by as much as 80%, the manufacturer claims.

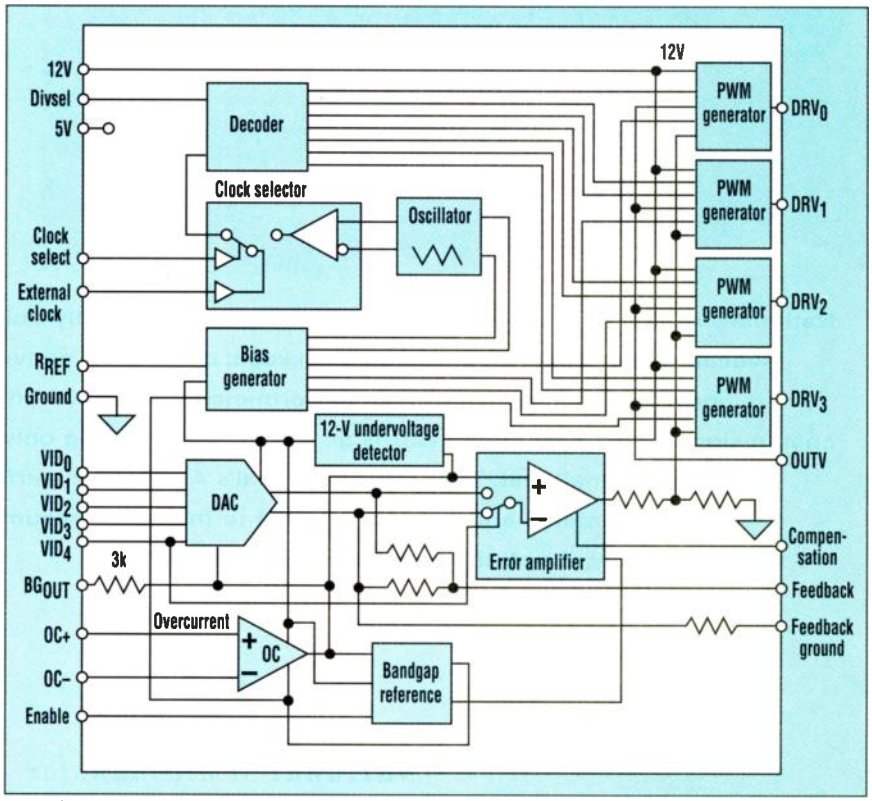
Multiphase Operation

To permit the use of smaller cheaper passive components, the controller's oscillating frequency is set at 8 MHz. This unusually high frequency allows the use of miniature, low-cost, multilayer ceramic chip capacitors with an ESR of only 3 mΩ. Conventional PWM techniques running at several hundred kHz, by comparison, meet the load transient response time by employing larger and more expensive electrolytic capacitors. Consequently, the resultant dc/dc converter offers high volumetric efficiency (*Fig.3*).

To keep its profile below a third of an inch, the converter utilizes a clever magnetic design that produces a compact surface-mount inductor. This new design replaces the large toroidal inductor, which can be as high as an inch. The resultant low-profile compact converter can be comfortably mounted on the backside of a dense CPU board. Many modern CPU boards, very crowded with components, have no room for bulky parts. Such boards require several of these converters on board.

"The transient response dictates that the dc/dc converter be placed close to the output connector, so that the parasitics due to the long interconnects are avoided," explains Newlin. "This design makes it possible to do so. Plus, it lends itself to automated assembly, reduces parts count, and offers an inherent reliability increase," Newlin comments.

Alan Moore, Semtech's marketing manager for power ICs, adds, "And, in addition, it lets the user build the dc/dc converter solution for under $10.00." To



2. By digitally phase-shifting the PWM outputs, the controller distributes the output load across four converter channels. The four channels are precisely matched to ensure that the four PWM outputs are accurately phase-shifted. The controller's on-chip transconductance-based error amplifier and its feedback mechanism enable the controller to provide ultra-fast transient-recovery time.

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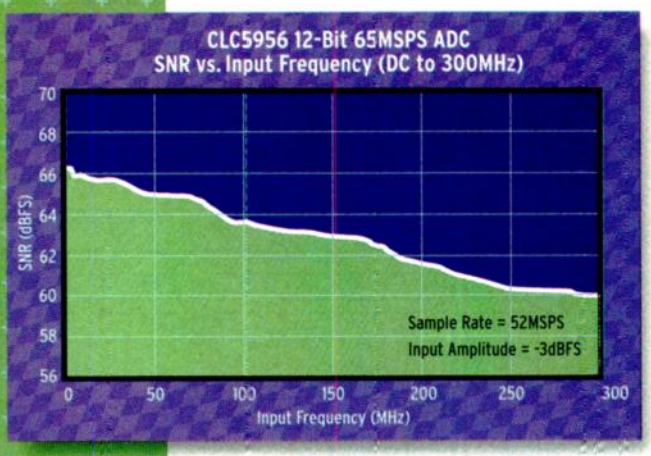
AT 250MHz



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- *Differential input*
- *Fully loaded and tested evaluation board*
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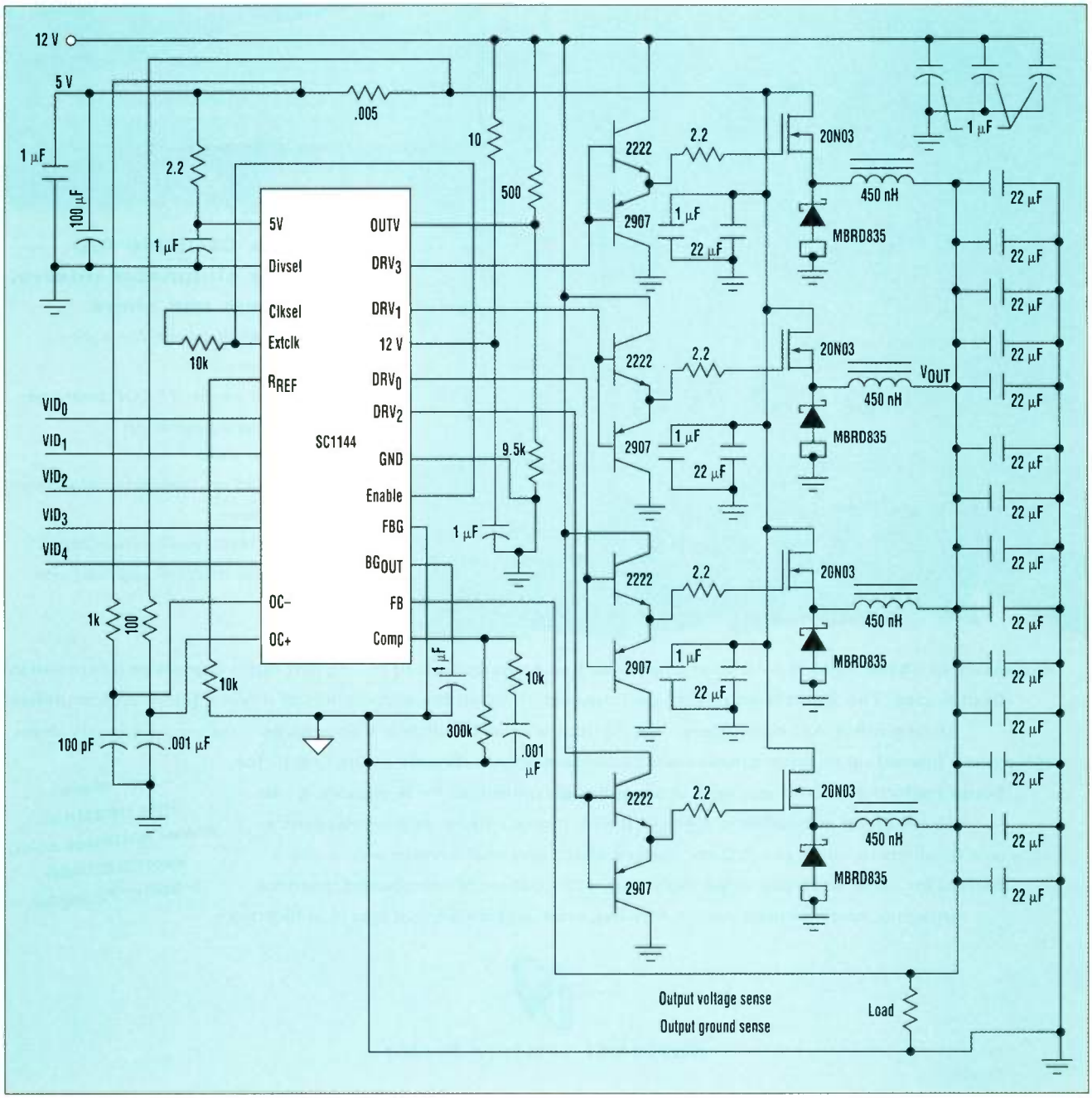
implement four-phase operation, the internal divide-by-four circuit scales the 8-MHz frequency down to 2 MHz. Each 2-MHz signal is then decoded to provide the trigger signals for the four PWM generators.

The PWM reference threshold voltage is set by the error amplifier, which is common to all four PWM generators. The on-time and off-time of the PWM comparator output, which drives the output power MOSFET, is determined by comparing the PWM reference threshold voltage to the ramp signal from the bias generator. To ensure that the four PWM outputs are accurately phase-shifted, the on-times of all four channels are precisely matched.

While a single resistor programs the internal master clock frequency (8 MHz), the on-chip Clock Select switch allows the use of an external source for applications requiring even better frequency control. In effect, the external clocking allows synchronous timing of multiple SC1144s. The external clock frequency is given by the clock input divided by the number of phases. The SC1144 can also operate as a three-phase controller by providing the logic high signal to the divide-by-four circuit. Dual- or single-phase operation is possible as well.

Other features of the multiphase PWM controller include undervoltage lockout with hysteresis and overcur-



3. In this programmable four-phase synchronous buck dc/dc converter, the digitally phase-shifted outputs are summed together to obtain the desired output voltage at the desired current rating. The output current is equally distributed among the four power MOSFETS and associated inductors, substantially reducing the size of the inductors and capacitors.

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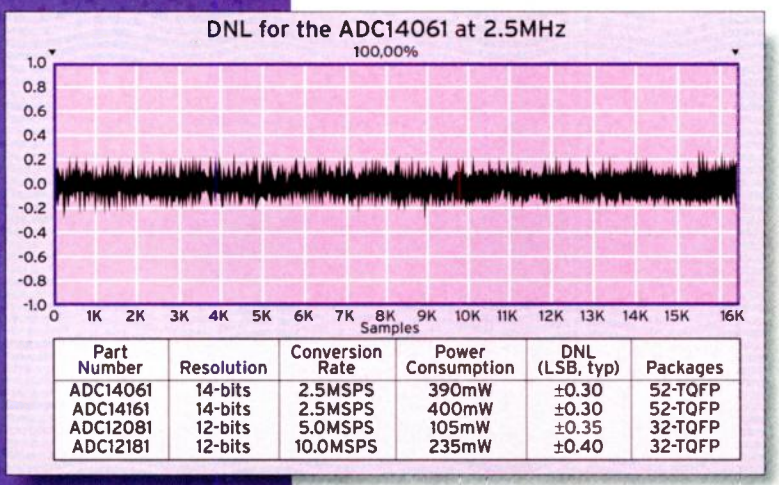

Part Number	Resolution	Conversion Rate	Power Consumption	DNL (LSB, typ)	Packages
ADC14061	14-bits	2.5MSPS	390mW	±0.30	52-TQFP
ADC14161	14-bits	2.5MSPS	400mW	±0.30	52-TQFP
ADC12081	12-bits	5.0MSPS	105mW	±0.35	32-TQFP
ADC12181	12-bits	10.0MSPS	235mW	±0.40	32-TQFP

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rent protection. While the undervoltage lockout protection is provided by the bandgap reference and associated circuitry, the overcurrent comparator assures that the device remains in the off state whenever the supply voltage drops below the set parameters. The SC1144 is made on a 4-µm single-metal bipolar process. Designed for a 12-V supply, it consumes less than 250 mW of power.

The multiphase PWM controller, and the resulting dc/dc converter solution, was a collaborative, synergistic effort between the power IC supplier Semtech and the computer maker Dell Inc., Round Rock, Texas. Prompted by the dire need for a compact power solution with ultra-fast transient recovery time, engineers from Dell's power development group developed a discrete multiphase buck dc/dc converter incorporating the novel PWM controller. They then approached Semtech to take the discrete solution and convert it into a single chip. Dell's power engineers have been working on this solution for about a year and a half. Semtech only reviewed the integration feasibility early this year. Yet, they successfully converted the discrete approach into a monolithic silicon chip—within six months.

Dell is the preferred customer for the SC1144. In June, they received samples which have been designed in Dell's new generation desktops. Dell next plans to implement the multiphase dc/dc solution in high-end servers and workstations.

The Semtech and Dell partnership is definitely not exclusive. Dell intends to create more sources for its multiphase PWM controller, and is planning to work with other major producers of power ICs. "The aim is to create an industry standard part with multiple sources," summarizes Alan E Brown, Dell's technical specialist for the power development group. He adds confidently, "This technique will be accepted fairly quickly."

Price And Availability

Samples of the four phase controller chips are available now, with production expected to start next month. In 10,000-piece quantities, the SC1144 in a 24-pin SOIC package is priced at $2.95 each. An evaluation board for the multiphase controller is also available for $49.00 each.

Semtech Corp., 652 Mitchell Rd, Newbury Park, CA 91320-2289; (408) 498-2111; Internet: www.semtech.com. **CIRCLE 485**

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CONFERENCE PREVIEW

ISLPED '98 Eyes Low-Power Components And Systems

Featuring The Latest Research On Low-Power Products, ISLPED Showcases Emerging Techniques, Methodologies, And Software.

Ashok Bindra

With today's thrust toward compact, cool, electronic products increasing, the pressure to design miniaturized circuits and associated systems with extremely low-power consumption is high. And, the pressure continues to rise as consumers demand more in performance and functionality from the tinier parts. To address issues related to the design and production of such low-power components and their end systems, this year's International Symposium on Low-Power Electronics and Design (ISLPED'98) sheds light on emerging design techniques, methodologies, and CAD tools and software that show great promise for commercial impact. The ISLPED symposium convenes next week (Aug. 10-12) at the Monterey Convention Center, Monterey, Calif.

While the contributed papers, running in two parallel tracks, focus on practical aspects of design, invited talks by industry and academia address key issues related to the design and fabrication of low power circuits. In addition, panel discussions will debate past and future blockbusters in low-power electronics *(see the program grid)*. Interestingly, this year's ISLPED also sponsors company exhibits demonstrating the state-of-the-art in design tools and products.

Keynote Addresses

The symposium kicks off with two keynote addresses. The first talk, "High-performance DSPs—what's hot and what's not?" by Bryan Ackland and Chris Nicol of Lucent Technologies, Holmdel, N.J., reviews techniques utilized in low-power DSPs, and probes other techniques which have fallen below their expectations. In fact, the talk investigates methodologies that provide answers to conflicting constraints such as getting high performance from low-power DSPs at a low cost. The second keynote address by Christer Svensson and Atila Alvandpour of Linkoping University, Linkoping, Sweden, explores low-voltage CMOS circuit techniques affecting power consumption in logic, latches, and flip-flops. This talk analyzes a variety of latches and flip-flops from the power-consumption standpoint. And, it uses the data obtained to build low-power and high-speed circuits. For example, the Swedish paper shows that simple static logic, in general, has the lowest power consumption, but pass-transistor logic is superior in some special cases such as the XOR function. Another key factor is the supply voltage. This talk discusses the effect of low supply voltage on the choice of circuit techniques.

Following the two keynote addresses, the technical program splits into two parallel sessions, M1 and M2. While M1 presents RF building blocks such as CMOS and bipolar components for micropower systems, M2 takes a peek at RT-Level power modeling and analysis.

Speaking of RF, researchers at the University of California at Los Angeles plan to unveil a complete RF CMOS front-end, operating at extremely low power. Their paper presents techniques for developing a micropower, voltage-controlled oscillator (VCO) and mixer circuits for emerging narrowband communications systems. In fact, the UCLA researchers intend to demonstrate methods for combining high-Q inductors and weak-inversion MOSFET operation to drastically reduce power consumption in RF front-end components. Other papers in this session include a 1.4-GHz, 3-mW CMOS LC, low-phase-noise VCO using tapped-bond-wire inductance, and a 3.8-mW, 2.5-GHz dual-modulus prescaler fabricated in a 0.8-μm bipolar process.

In the modeling and analysis arena, three papers highlight the trend toward simulation-based power estimation. In a paper by the Polytechnic Institute of Torino, Italy, scientists introduce a new stream-synthesis method for efficient power simulation, based on a discrete Fourier transform and its inverse. This method determines a reduced sequence of vectors that shortens the time for power simulation. The authors plan to demonstrate the effectiveness of the proposed synthesis by presenting experimental results.

Minimizing Power

After lunch, there are two more parallel technical sessions. While four papers in session M3 explore silicon-on-insulator (SOI) technology and low-voltage CMOS for low-power applications, M4 papers investigate architectural techniques for general-purpose systems.

In the SOI area, a joint effort by TIMA Labs, Grenoble, France, and the University of Bologna, Italy, with support from the European ESPRIT program, has resulted in the development of 3D CMOS SOI technology using symmetrical T-gate transistors. The T-gate transistors are produced lithographically using an independent, edge-defined MOS (EDMOS) technology. Unlike lithographically defined geometries, EDMOS uses the thickness of deposited films to determine gate lengths and widths.

A 16-by-16-bit multiplier based on SOI methodology is slated for presentation, and its performance will be compared to 2D designs. Comparative

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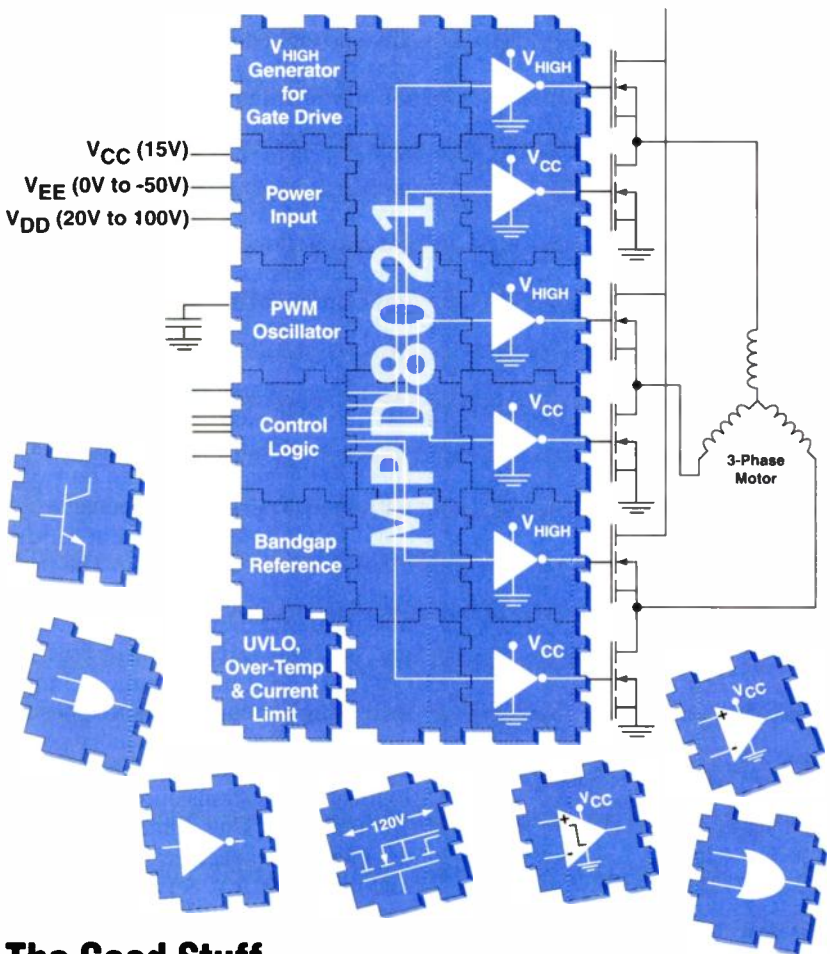

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results indicate that the 3D integration offers significant improvement in energy consumption, delay, and area.

Another paper entitled, "A high-speed and low-power SOI inverter using active body-bias," from researchers at Wonkwang University, Chonpuk, Korea, evaluates a novel inverter circuit that can operate with efficient body-bias control at a 1.5-V supply.

Recent efforts in architectural modifications to minimize power or energy have compromised processor performance. Consequently, such improvements have been targeted at low-end embedded markets. A collaborative work by scientists at the University of Illinois at Urbana, and experts at Intel Corp., Santa Clara, Calif., addresses this issue by implementing an extra, small cache between the I-cache and the CPU. This serves to reduce the effective energy dissipation per memory access. The development team has ensured that the compiler generates code that exploits the new memory hierarchy and reduces the likelihood of a miss in the extra cache. According to the paper, almost 55% of the energy dissipated in the I-cache subsystem can be saved with a small performance penalty.

Cutting power in embedded DRAMs also is challenging. The problem gets worse when the heat and noise generated by the logic portion of the merged DRAM/logic LSI degrades DRAM performance. Simply increasing memory refreshes does not work, because it leads to more power consumption. Yet, researchers at the Institute of Systems and Information Technologies, Fukuoka, Japan, have developed an architecture that optimizes the DRAM refresh count for merged DRAM/logic LSI ICs.

While most of the work related to architectures is hardware oriented, a team at the University of California at Berkeley has taken the software route. Here, the researchers have developed a dynamic-voltage-scaling (DVS) algorithm to cut energy consumption in microprocessors. Using software control, this approach varies the processor's voltages to meet changing performance requirements dynamically. The Berkeley paper evaluates the DVS algorithm, as well as presents simulation techniques.

Brief poster papers will attempt to uncover a variety of uses for low-power circuits, including a low-threshold CMOS (LTCMOS) with low standby current by Mircea R. Stan of the University of Virginia at Charlottesville, and minimum supply volt-

1998 INTERNATIONAL SYMPOSIUM ON LOW-POWER ELECTRONICS AND DESIGN

Monday August 10 8:30-10:00 a.m.	**Plenary session M0** **Keynote address** M0.1: High-performance DSPs—what's hot and what's not? **Keynote address** M0.2: Low-power and low-voltage CMOS digital circuit techniques	
10:30 a.m.-12:00 noon	**Parallel paper sessions M1 and M2**	
	M1: RF building blocks	M2: RT-level power modeling and analysis
1:00-3:00 p.m.	**Parallel paper sessions M3 and M4**	
	M3: Enabling device technology for low-power applications	M4: Low-power architectural techniques for general purpose systems
3:30-4:30 p.m.	**Parallel poster sessions P1 and P2**	
	P1: Circuits and technology	P2: Systems and CAD
4:30-5:30 p.m.	**Poster displays**	
5:30-6:30 p.m.	**Industry demos**	
7:00-9:00 p.m.	**Panel session**	
	Panel discussion Past and future blockbusters in low-power design	
Tuesday August 11 8:30-10:00 a.m.	**Plenary session T0** **Invited talk** T0.1: Industrial perspectives on emerging CAD tools for low-power processor **Invited talk** T0.2: Recent developments in high-integration multistandard CMOS transceivers for personal communications systems	
10:30 a.m.-12:00 noon	**Parallel paper sessions T1 and T2**	
	T1: Low-power logic circuits	T2: System-level power issues
1:00-2:30 p.m.	**Parallel paper sessions T3 and T4**	
	T3: Variable voltage and analog techniques	T4: Logic synthesis for low power
2:30-3:30 p.m.	**Poster displays**	
3:30-5:30 p.m.	**Parallel paper sessions T5 and T6**	
	T5: Circuit-level power analysis and estimation	T6: Low-power design for application-specific processors
Wednesday August 12 8:30-10:00 a.m.	**Plenary session W0** **Invited talk** W0.1: Power distribution in high-performance design **Invited talk** W0.2: Low-power miniaturized information display systems	
10:30 a.m.-12:00 noon	**Parallel paper sessions W1 and W2**	
	W1: Low-power memory	W2: High-level power analysis and optimization
1:00-4:30 p.m.	**Parallel tutorials 1 and 2**	
	Tutorial 1: Design methodologies for low-power signal processing	Tutorial 2: Low-power wireless communications

age for bulk silicon by James D. Meindl et al of Georgia Institute of Technology at Atlanta. One noteworthy paper hails from Germany's Institute for Microelectronics, Stuttgart. This paper describes 0.5-V CMOS logic delivering 200 million 8-by-8-bit multiplications/s based on a 50-nm T-gate SOI technology. A parallel poster session also sheds light on advancements in CAD tools for power estimation and modeling at the system level.

Low-Power Techniques

Tuesday's program starts with two plenary invited talks. Motorola Inc.'s David Blaauw will discuss "Industrial perspectives on emerging CAD tools for low-power processor design." Blaauw's presentation looks into existing and emerging methodologies that have contributed toward power management of designs at Motorola. The invited paper also focuses on a number of CAD software developments that are still in their infancy. Specifically, Blaauw will discuss initial applications of automated high-level synthesis for low power circuits, and the need for power distribution analysis and optimization tools. In addition, he will address the emerging need for leakage measurement and threshold-voltage optimization tools.

The second talk is entitled "Recent developments in high-integration multistandard CMOS transceivers for personal communication systems," by Jacque C. Rudell of the University of California at Berkeley. Rudell's talk discloses radio systems that incorporate integrated single-chip transceiver functions, and examines power-saving strategies similar to those adopted by digital designers. Additionally, the talk will also describes a single-chip receiver for DECT applications, based on 0.6-µm CMOS. The presentation also spends time on a prototype under development that meets dual DCS1800/DECT standards.

The plenary talks will be followed by parallel technical sessions, T1 and T2. Session T1 on "Low-power logic circuits" features three papers. One of the papers by authors from the University of California at Berkeley, examines power dissipation in FPGAs. It proposes structures that alleviate power problems due to interconnects, while permitting FPGAs to operate at

low voltages for lower power consumption. The authors claim an order of magnitude reduction in power consumption over existing implementations. Parallel session T2 on "System-level power issues" comprises three papers indulging in modeling, estimation, optimization, and management.

There are two more parallel sessions on Tuesday afternoon, T3 and T4. Session T3 focuses on "Variable voltage and analog techniques," and session T4 dwells on "Logic synthesis for low power." In session T3, a paper by MIT's department of Electrical Engineeering and Computer Science unveils a versatile, digital PWM power controller that features reconfigurability, dual outputs, and low power dissipation. In the same session, another paper from Kyushu University, Kasuga, Japan, addresses voltage-scheduling issues related to dynamically variable voltage processors. The Japanese researchers present a novel scheduling model that minimizes energy consumption.

The advent of portable electronics has made low-power logic synthesis increasingly important. However, until now, designers have concentrated on minimizing the total switching activity of a circuit using a zero-delay model. This simplification ignores the effects of glitch transition, which may contribute as much as 30% of a circuit's total power consumption. Consequently, low-power logic synthesis employing a zero-delay model cannot attain real power savings. To overcome this problem, researchers at Intel Corp. and the University of Illinois have cooperated to develop low-power logic synthesis under a general delay model. They will present their results in session T4.

This will be followed by two more parallel technical sessions, T5 and T6. Circuit-level power analysis and estimation is the theme of track T5, and low-power design for application-specific processors is the umbrella topic for session T6.

Leakage current becomes critical as supply voltages decrease, and correspondingly, device threshold voltages fall. A paper from the School of Electrical and Computer Engineering, Purdue University, W. Lafayette, Ind., describes a technique to accurately estimate leakage power by modeling the leakage current in tran-

sistor stacks, and thus minimize the problem during fabrication. This paper will be presented in session T5. Similarly, in parallel session T6, engineers at IBM Microelectronics, Essex Junction, Vt., will unfold an ASIC design methodology for low-power microprocessors aimed at battery power products. According to the IBM paper, the active power usage is slashed by a factor of 10 over a standard 3-V ASIC design methodology.

Optimizing Design

The final day of the symposium opens with a plenary talk by Michael Benoit of Simplex Solutions, Sunnyvale, Calif. Benoit's paper focuses on power distribution in high/-performance circuit design. In this presentation, Benoit discusses power-distribution design challenges to the reliable delivery of predictable voltage to all transistors under all operating conditions. He also reviews implementation and verification techniques.

Low-power miniaturized information display systems is the subject of the next invited talk by Philip Alvelda of The MicroDisplay Corp., San Pablo, Calif. He will emphasize power dissipation trends in miniaturized LCDs and associated systems. The paper explores a number of drive schemes, including time-multiplexed binary drive and digital steering of external analog voltages. It also evaluates power-distribution techniques.

The last two parallel technical sessions focus on low-power memory (W1) and high-level power analysis and optimization (W2). A paper by Japan's Mitsubishi Electric Corp. describes low-power SRAMs based on auto-backgate-controlled multithreshold CMOS circuits. This technique combines low-threshold voltages for improved performance, and selective back-gate biasing to reduce leakage current. It results in both lower power and faster access time.

In short, the ISLPED symposium attempts to highlight all aspects of designing low-power products. As the technology grows, low-power electronics consistently develop both issues and advances. The symposium covers both of these, and presents methodologies for implementing and fabricating end systems using emerging techniques and solutions.

CONFERENCE PREVIEW

Brazil Meeting Explores The Latest In Microelectronics And Packaging

ICMP '98 Reviews A Wide Variety Of IC Design, Process, Testing, Interconnect, And Packaging Issues.

Roger Allan

Next week's annual International Conference on Microelectronics and Packaging (ICMP '98) and its attendant exhibits put the spotlight on IC technological advancements and innovations, from circuit conception to final product. About two-thirds of the technical program speakers are from Brazil—a country rapidly becoming a major force in the electronics sector.

The conference is sponsored by the Brazilian Microelectronics Society (SBMicro) and the International Microelectronics and Packaging Society (IMAPS). It is organized by the Central Research and Development Laboratory (LAC) of the Federal University of Paraná (UFPR), in conjunction with the Power Utility Company of Paraná (COPEL). It will be held August 10-14 in Curitiba, Brazil, in the southeastern part of Brazil's Paraná State (*see "Brazil: A Growing Electronics Market," p. 46*). The General Chairman of ICMP '98 is Ivan Chueiri of COPEL.

The conference's preliminary technical program, chaired by Professor Carlos Reis, Unicamp University, São Paulo, Brazil, consists of 84 presentations spread out over 18 technical sessions *(Table 1)*. Technical presentations run daily in three consecutive tracks (A, B, and C), with a fourth parallel track (D) devoted to the subject of "Business in microelectronics." The program also includes 16 poster session presentations.

On Wednesday, August 12, at 9:00 a.m., Professor Pier A. Abetti, Lally School of Management and Technology, Rennselaer Polytechnic Institute, Troy, N.Y., will deliver the keynote address: "Technology, strategy and global competitive advantage: Winning in high-tech markets." He'll explain why some companies, like GE Medical Systems, Motorola Communications, Intel, Microsoft, Nokia, and Toshiba, have achieved worldwide leadership through technology. Abetti will also cover the reasons that others, like IBM, General Motors, and Digital Equipment, have not succeeded—despite having excellent R&D facilities.

All technical paper presentations, each 20 minutes in duration (except for invited papers, which last 40 minutes), will be presented Wednesday, Thursday, and Friday, August 12-14. Preceding the technical program on Monday and Tuesday, August 10 and 11, will be two days of tutorials. These

TABLE 1: PRELIMINARY 1998 INTERNATIONAL CONFERENCE ON MICROELECTRONICS AND PACKAGING (ICMP'98)

Wed. Aug. 12 9:00 a.m.	KEYNOTE ADDRESS			
11:00 a.m.	Opening Session			
12:00 NOON	Lunch			
August 12 2:00-4:00 p.m.	Session 1A Analog design I	Session 1B Miscellaneous	Session 1C Hardware-software codesign	Session 1D Business in microelectronics
4:20-5:20 p.m.	Session 2A Fuzzy logic and neural nets	Session 2B Interconnections	Session 2C Micro-electro-mechanical-systems	Session 2D Business in microelectronics
7:30 p.m.	Welcome Reception			
Thursday August 13 8:20-10:20 a.m.	Session 3A Thin films	Session 3B Digital design	Session 3C Analog design II	Session 3D Business in microelectronics
10:40 a.m.-12:00 noon	Session 4A Smart sensors	Session 4B Data communications and software	Session 4C Prototyping	Session 4D Business in microelectronics
12:00 noon	Lunch			
2:00-4:00 p.m.	Session 5A Fabrication processes	Session 5B Smart power	Session 5C Characterization and test I	Session 5D Business in microelectronics
4:20-5:20 p.m.	Poster session			Session 6D Business in microelectronics
7:30 p.m.	Dinner (Live music)			
Friday August 14 8:20-10:20 a.m.	Session 6A Characterization and test II	Session 6B -Δ analog-to-digital conversion and filters	Session 6C Device physics	Session 7D Business in microelectronics
10:40 a.m.	Discussion panel (with translation)			
12:20 p.m.	Lunch			
2:20 p.m.	SBMicro assembly meeting			

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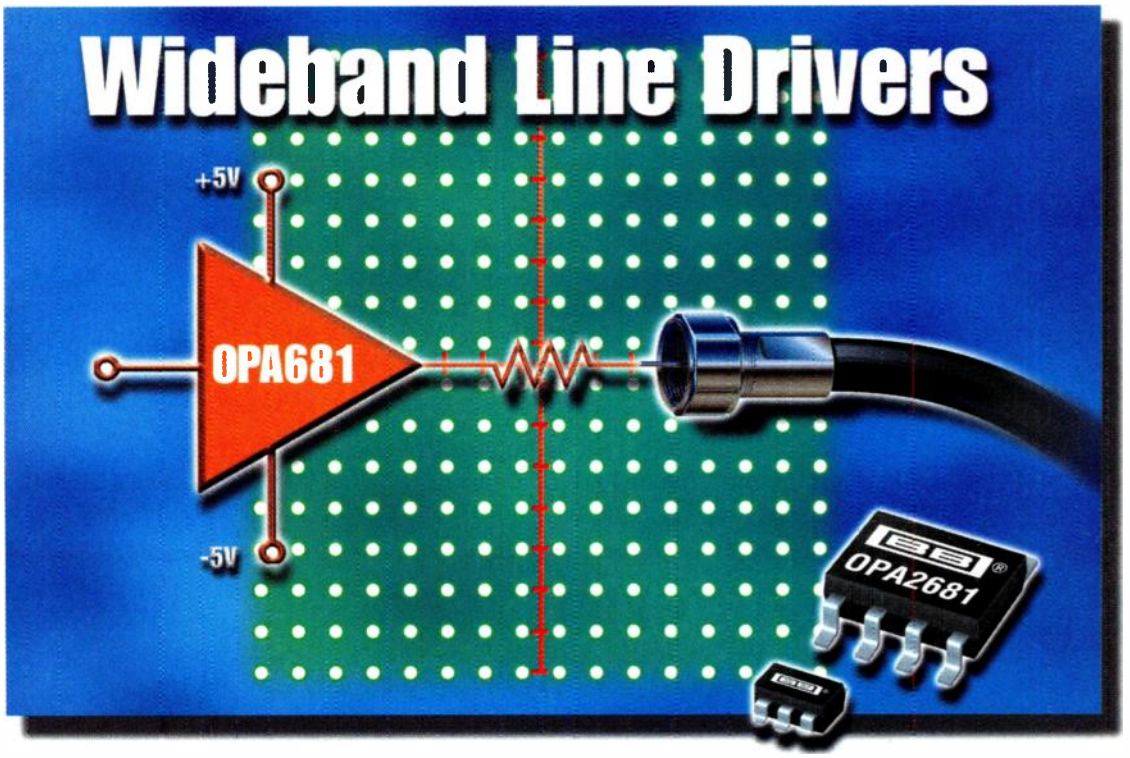

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- Output Current ..... +190mA/–150mA
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are given by experts in a number of state-of-the-art fields of electronics technology *(Table 2)*.

Despite the fact that the majority of the presentations have their roots in Brazil, this conference has a truly international flavor. Speakers are coming from Argentina, Austria, Belgium, Canada, Cuba, Denmark, France, Israel, Japan, Portugal, Switzerland, Turkey, the U.K., and the U.S.

The conference will also feature about 40 electronics exhibitors, many of which are major companies showing off their latest wares. These include Motorola Semiconductor, Texas Instruments, AEGIS Semiconductor, Dupont, Hewlett-Packard Co., Semikron, Altera, Xilinx, and Orbit Semiconductor, to name a few.

Running The Gamut

Technical program papers cover a wide range of subjects. Many focus on analog and power device developments, IC materials and processes, and EDA issues. A host of papers examine packaging and interconnect issues, digital device developments, communications ICs, fuzzy logic, neural networks, sensors, microelectrical mechanical systems (MEMS), and testing issues.

Sessions 1A, 1B, 3C, and 6B contain papers highlighting analog device developments. Several advances in sigma-delta analog-to-digital converters are described in session 6B. In this session, Jose Camargo de Costa, Brazilia Federal University, Distrito State, will talk in an invited paper about "Nanoelectronics—a promising option for gigascale to terascale integration."

Session 5B reviews smart power device advances, including an invited joint paper by F.H. Behrens, PUC-CAMP, Campinas, and S. Finco and M.I. Castro Simas, CTI, Campinas. "Power devices in standard CMOS technology" is the result of this shared effort.

Session 3B is entirely devoted to digital technology advances. Its invited paper by Paulo Batista Lopes, Texas Instruments, São Paulo, Brazil, talks about "The TMS320C6x: A VLIW architecture for DSP applications."

Materials And Processes

A fair number of presentations deal with advancements in all aspects of IC materials and processes. For example, Session 3A has several papers on thin films, including an invited paper by U.S. researchers Charles Bauer and Happy Holden, TechLead Corp., Evergreen, Colo. The two researchers will address whether ICs should be designed for manufacturability or for the lowest cost. They will also deliver two

TABLE 2: ICMP'98 TUTORIALS

MONDAY AUG. 10

8:00-9:30 a.m. Tutorial 5A
Companding filters for communications applications, Douglas Frey, Lehigh University, U.S.

8:00-9:30 a.m. Tutorial 6
Microelectronic packaging and interconnect, Philip Garrou, Dow Chemical Co., U.S.

9:30-10:00 a.m. Coffee Break

10:00-11:30 a.m. Tutorial 3
Retargetable block-driven analog-digital design, Jose Franca, Instituto, Superior Technico, Portugal

10:00-11:30 a.m. Tutorial 6 (see above)

11:30 a.m.-2:00 p.m. Lunch

2:00-3:30-p.m. Tutorial 3 (see above)

2:00-3:30-p.m. Tutorial 7
Microelectronic mechanical systems, Dan Horonia, Tel Aviv University, Israel

2:00-3:30-p.m. Tutorial 9
Making the most of existing and emerging packaging technology, Brian Waterfield, TWM Technology, U.K.

3:30-4:00 p.m. Coffee Break

4:00-5:30 p.m. Tutorial 3 (see above)

4:00-5:30 p.m. Tutorial 7 (see above)

4:00-5:30 p.m. Tutorial 11
COTS-EEE components and plastic encapsulated semiconductors for space application, John Wall, Defense and Evaluation Research Agency, U.K.

TUESDAY AUG. 11

8:00-9:30 a.m. Tutorial 2
Application-specific systems design and prototyping, Luigi Carro, UFRGS, Brazil

8:00-9:30 a.m. Tutorial 4
The present and future of the silicon revolution: technology, manufacturing and device design implications, Pierre Fazan, EMMarin/EPFL, Switzerland

8:00-9:30 a.m. Tutorial 5B (see 5A above)

8:00-9:30 a.m. Tutorial 13
DSP—digital signal processors, Lourival Lippmann Jr., LAC-UFPR/COPEL, Brazil

9:30-10:00 a.m. Coffee Break

10:00-11:30 a.m. Tutorial 2 (see above)

10:00-11:30 a.m. Tutorial 4 (see above)

10:00-11:30 a.m. Tutorial 8
RF design: From basic concepts to the state of the art, Bahzad Razavi, UCLA, U.S.

10:00-11:30 a.m.Tutorial 13 (see above)

11:30 a.m.-2:00 p.m. Lunch

2:00-3:30-p.m. Tutorial 1
High-tech entrepreneurship: An international perspective, Pier Abetti, Rensselaer Polytechnic Institute, U.S.

2:00-3:30-p.m. Tutorial 8 (see above)

2:00-3:30-p.m. Tutorial 10
Packaging evolution and future challenges, Rao Tummala, Georgia Institute of Technology, U.S.

2:00-3:30-p.m. Tutorial 12
Embedded core-based system-on-a-chip test strategies, Yervant Zorian, LogicVision, U.S.

3:30-4:00 p.m. Coffee Break

4:00-5:30 p.m. Tutorial 1 (see above)

4:00-5:30 p.m. Tutorial 8 (see above)

4:00-5:30 p.m. Tutorial 10 (see above)

4:00-5:30 p.m. Tutorial 12 (see above)

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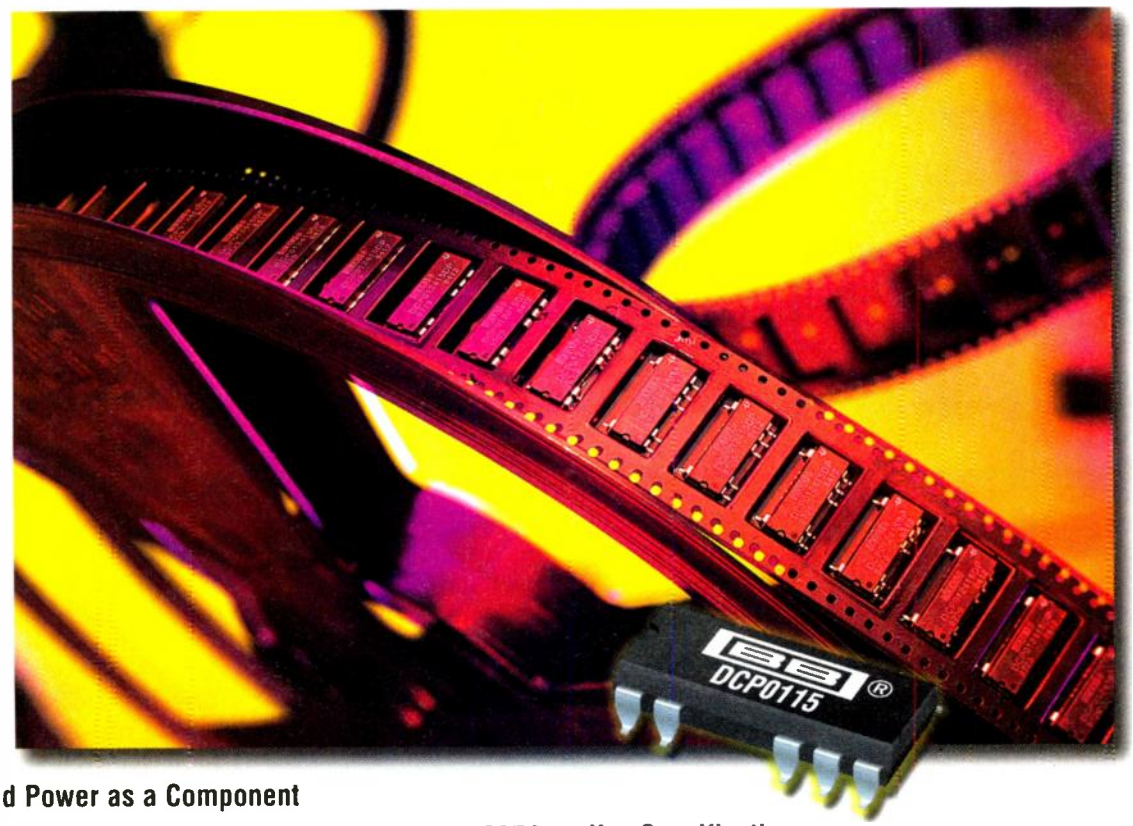

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other invited papers, in sessions 5A and 6A. The first is on how to best predict substrate design rules and performance levels, while 6A concentrates on predicting the costs of substrates, assembly, and assembly testing. Device and process characterization, as well as device physics, are covered in sessions 5C, 6A, and 6C.

Session 5C presents "BIST technology," the work of Yervant Zorian, LogicVision Corp., San Jose, U.S., and Gerald M. Oleszek and Kathy L. Kasley, University of Colorado at Boulder. They will deliver their invited talk together: "Reduction of hot-electron-induced degradation in n-channel MOSFETs at 25k using a floating-well contact."

Session 2B, for the most part, is devoted to interconnect issues for high-density and submicron designs. Fuzzy logic and neural nets are covered in sessions 1B and 2A. The invited paper in 1B focuses on "Neural-inspired VLSI implementations of parallel signal processors" by Volnet A. Pedroni, COPEL.

Design Automation

Design automation is an integral part of the technical presentations. Topics include hardware-software

Brazil: A Growing Electronics Market

Industrial development, in Brazil as well as the rest of Latin America, is growing rapidly. It is expected to be one of the most dynamic sectors of the economy, and includes the electronics industry. For example, Brazil is expected to be the fourth largest automotive manufacturer in the world by the turn of the century, after the U.S., Japan, and Germany. The entire Latin American automotive market is expected to grow by 70% over the next five years. Brazil is the world's sixth largest country in population and land area, and the eighth largest in gross domestic product.

Brazil consists of 26 states and a federal district *(see the figure)*. This country is already the third largest manufacturer of TV sets in the world. It's CATV market is set to explode from 2.7 to over 14 million subscribers in four years. The $90 billion invested in telecommunications in Brazil represents one of the world's largest projects, with over 30 million telephone lines and over 20 million cellular access lines being installed until the year 2003.

Motorola recently opened a design center in Brazil's state of São Paolo. According to the company, "it intends to back that design center with significant investments in people, capital, and infrastructure to duplicate the success we've had in other emerging markets such as China and Eastern Europe." According to a recent report by the research firm In-Stat, Scottsdale, Ariz., many of the electronic end-equipment manufacturers in Latin America will experience double- and triple-digit growth rates between 1997 and 2001. The automotive market, where Motorola has historically been a leader, is expected to grow at an annual rate of about 67% during this same period. Similarly, analog cellular handsets should grow at about 27%, while the growth in digital cellular handsets should explode to nearly 120%.

Latin America currently accounts for 20% of U.S. telecommunications exports. Larger than the European Union's telecom market, it's growing at a faster rate than Asia's. U.S. semiconductor industry exports to Latin America are expected to grow at 30% per year through the rest of this decade. By 2005, Latin America should account for about 10%, or more than $600 billion, of the $6-trillion global electronics market.

Brazil and the rest of Latin America sorely need more development projects and a greater presence of local electrical/electronics manufacturing operations to help cut down a growing trade deficit. Brazil's import deficit was $9.5 billion in 1997, and has been growing at a rate of 34% per year since 1993. This is one reason why many companies, like Motorola, are investing heavily in Latin America. There are federal and state organizations in Brazil, like INDI-MG (The Industrial Development Institute of Minas Gerais State), that are interested in providing resources to further develop the electronics industry. While average net investment between 1991 and 1994 was on the order of $1.3 billion, in 1995, it reached $4.3 billion, growing to $9.9 billion in 1996. Forecasts place year-end 1997 inflows at $15 billion.

The government has recently launched a series of 42 investment projects called "Brasil em Ação" (Brazil in Action). The projects are exclusively aimed at infrastructure and social development, involving the investment of over $50 billion between 1997 and 1998. The infrastructure projects involve investments in transportation, energy, and communication. Social projects focus on generating employment and fostering professional education.

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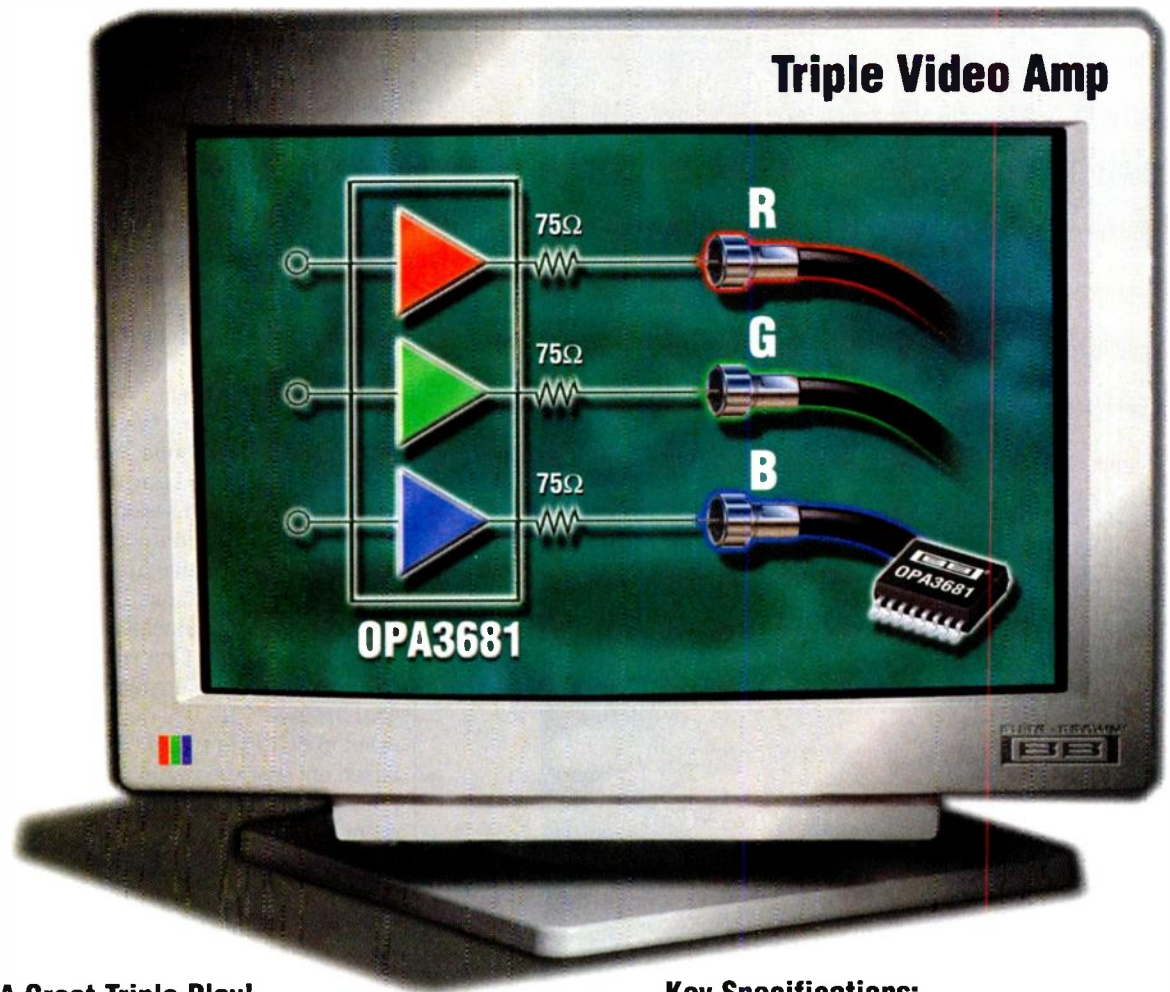

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codesign, prototyping, and simulation from papers in sessions 1A, 1B, 1C, 2B, 3A, 3C, 4C, and 5B. In fact, 1A leads off the program with an invited paper, "The ACM MOSFET model: A charge-based compact model for circuit simulation." This paper was authored jointly by A.I.A. Cunha of Bahia State Federal University, O.C. Gouveia Filho and M.C. Schneider of Santa Catarina State Federal University, andC. Galup Montoro of Parana State Federal University, Brazil. "System-level design" is the title of an invited paper in Session 1C by Diogenes C. da Silva, Jr.; Claudionor J.N. Coelho, Jr.; and Antonio Octavio Fernandes, Minas-Gerais State Federal University, Brazil.

MEMS and smart sensors are also on the program agenda, including papers in sessions 2C and 4A, respectively. Of interest in session 2C is a paper entitled "Silicon microstructures for neuroelectronics applications," University of São Paolo, Brazil.

Finally, Gerson Machado, ICMP '98 Tutorials Program Chairman and consultant for Technology For Industry, Cambridge, U.K., will deliver a talk in session 3C. It is titled "Technology-based entrepreneurship in Brazil: Opportunities and capability development in the semiconductors sector." Machado highlights many emerging business opportunities in his native country *(see "Brazil: Growth Electronics Market," p. 46).*

Poster Sessions

On Thursday August 13, at 4:00 p.m., 16 poster session papers will be presented to indicate the breadth of advances in the Brazilian electronics sector. Many of the papers deal with various process and design-automation advances including deep X-ray lithography as well as bipolar, CMOS and GaAs processes. One interesting paper is "Signal generator cores for mixed-signal systems-on-a-chip," a joint presentation by A Susin of Brazil's Federal University of Rio Grande da Sol State (UFRGS) and G. Roberts of Canada's McGill University , Montreal, Quebec.

For more information on ICMP '98 and its organizers, visit their website at www.lac.copel.br/sbmicro. For ICMP '98 sponsors, go to www.dsif.fee. unicamp.br/sbmicro and www.imaps.org.

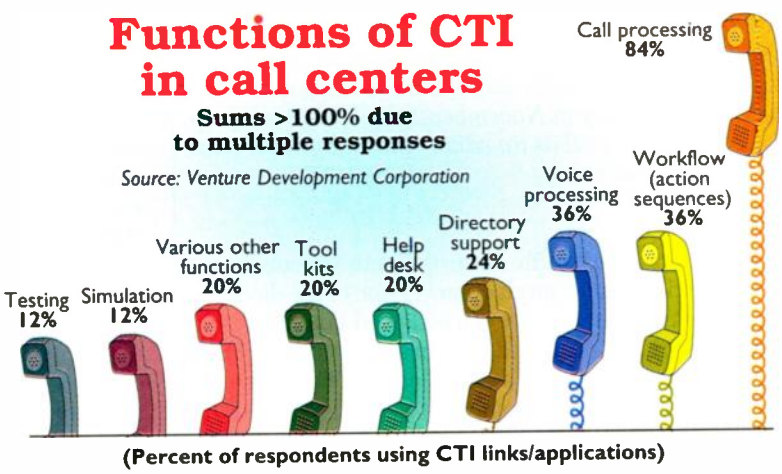
ELECTRONIC DESIGN QUICK LOOK

Edited by Debra Schiff and Nancy Konish

MARKET FACTS

Ring, Ring—It's The Future Calling

The recent leap in the interest level for computer telephony integration (CTI) is a direct result of the surge toward open platforms. There's finally a major rethinking of CTI in the marketplace from the managers' perspective. No longer is this technology relegated to just performing screen pops and other circus acts, but now it has been repatriated from exile to take its place as an integral part of the call routing and managing process. Industry estimates put the average percentage of call centers without CTI servers/application software at around half of the market. According to a recently released report from Venture Development Corporation (VDC), Natick, Mass., "U.S. Call Centers: Market Insight for Suppliers of Call Center Technology," the driver behind the renewed popularity of CTI in call centers comes from the migration to open, client/server environments. Open, systems-based platforms are better able to handle integration and seamless cooperation between front and back office systems. UNIX-based CTI will see a definite decline as the NT and IP platforms gain much ground. Driving the shift to PC-based CTI servers is the proliferation of PC-based systems and customer demand. An oft-debated issue is whether or not these new systems are as robust as the proprietary systems they are replacing. Regardless, any kinks are expected to be fully worked out over a relatively short period of time. Recent introductions based on sharing workloads with existing technology have created quite a stir in this market. Intelligent call routing (ICR) improves the routing capabilities of the operation while "running off the CTI." By handling the routing function with this technology, existing hardware/legacy systems are leveraged, reducing workload and enhancing functionality. Computer and interactive voice response (CIVR) is a hybrid CTI application combining the function of voice response with the ability of CTI. The CIVR server prompts the caller with questions before the call enters the routing path. Assuming a number of calls reach conclusion through the interactive voice response (IVR) function at this level, fewer calls are routed to the agent (less agent time = lower costs). If a customer at any time wishes to speak with an agent, a simple prompt-out sends the call to the agent pool along with the data on that caller already accessed at the start. Banking, financial services, and telecommunications are still the major consumers of this technology. Suppliers of IVR technology are, however, noticing an increase in shipments to customers elsewhere. IVR has been moving into utilities, government, transportation, and healthcare at an increasing rate. There could be a shadow looming on the horizon that won't necessarily spell doom for IVR usage in call centers, but may bring about significant change in how it is utilized. As with any technology, there is the danger that comes from ignoring the possible negative side-effects. In this case, there may be a "de-humanizing" effect on the customer-organization interaction. The abuse of this technology, in the form of overuse could create a backlash, as customers may begin to feel these companies to be impersonal, maybe even impolite. The impact of this on customer retention rates could be devastating.



(Percent of respondents using CTI links/applications)

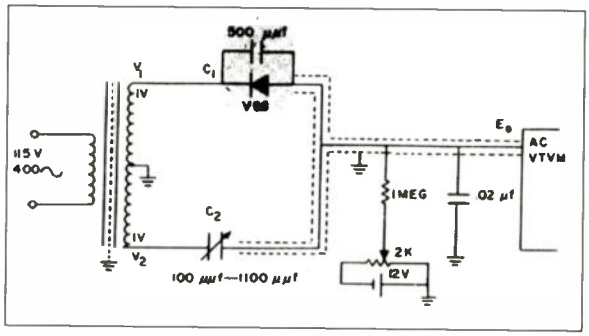
John A. Gordon is a project director for VDC, a technology market research and consulting firm specializing in telecommunications and electronics technologies. Gordon holds a MBA from Bentley College, Waltham, Mass. and a BS in Laboratory Science from Northeastern University, Boston, Mass. He may be reached at (508)653-9000, or by e-mail: jgordon@vdc-corp.com.

40 YEARS AGO IN ELECTRONIC DESIGN

Idea for Design: Bridge To Measure Voltage Variable Capacitors

We needed to measure the range of capacitance variation of the V56 Varicap (Pacific Semiconductor Industries) at 400 cps. This is a silicon pn junction device designed to work as a voltage variable capacitor. We wanted a bridge whose accuracy would not be affected by the impedance of the dc bias control.

The three terminal bridge, shown in the figure, did the trick. At null $E_0 = 0$, so the bridge accuracy is not affected by the dc supply impedance. C_2 is a calibrated voltage variable capacitor used to rebalance the bridge when the dc control function is varied.



The 500 μμf capacitor across the voltage variable capacitor brings C_1 to a capacity level in the range of C_2. Jerome Lyman, Electrical Engineer, Liquidometer Corp., Long Island City, N.Y. (*ELECTRONIC DESIGN, August 6, 1958, p. 174*)

This Idea for Design was submitted by Jerry Lyman, who in the mid '70s joined the editorial ranks as an editor with McGraw-Hill's Electronics magazine. He later joined the editorial staff of ELECTRONIC DESIGN. As an editor, Jerry became an expert in electronic components, packaging, and production techniques. He wrote many of the definitive articles on TAB bonding and other IC packaging methods. Jerry passed away in November, 1996. He left a legacy as a practical, no-nonsense engineer, as well as an editor who enjoyed the total respect of his colleagues.—Steve Scrupski

Auto Radar Undergoing Tests

Auto radar may soon warn the driver of traffic hazards. Tests are now being conducted under actual road conditions, and a production version of the device is under development. A radar antenna about the size of a hollowed-out steak platter is mounted in the front radiator grill of the car. Signals are sent out, which are converted into an automatically regulated "beep-beep" sound. The driver is thereby told whether he is closing the gap too rapidly between his car and the one in front, if he is approaching an object on a possible collision path, or if cross traffic threatens collision.

If a motorist is overtaking another car at moderate speed, or if the other car is still some distance away, the "beep-beep" warning is very light, the engineers said. But as the other car gets nearer, the radar warning signal becomes progressively louder and more insistent.

Developed by Bendix Aviation Corp., Detroit, Mich., the new device limits the signals to objects within the car's safe stopping distance, ignores situations in which the car in front is within distance but is pulling away, permits adjustment for open-country or congested-traffic driving, and reduces background noises that would confuse the signal. (*ELECTRONIC DESIGN, August 6, 1958, p. 15*)

Another one of those ideas that always seem to be just around the corner. Forty years later, we have police radar detectors and EZ-Pass automated toll-collection systems, but we still don't have automotive radar systems for safer driving.—Steve Scrupski

Steve Scrupski is a former Editor-in-Chief of ELECTRONIC DESIGN. Now semi-retired, he can be reached at scrupski@worldnet.att.net.

Ahoy, Pirates

Remember old Captain Hook, swashbuckling and eyepatch-wearing, out to steal gold from ships? That's the stuff of bedtime stories, Disney movies, and...software? Yep, in this day and age, pirates steal technology.

In Korea, piracy's huge success rate has created a constant need for copy protection. The Software Publishers Association reports that their software piracy rate is about 70% for personal computer business applications. Losses to U.S. business software publishers are estimated at almost $200 million.

It's no wonder, then, that Digital Media (DM) Technology Co., Seoul, Korea, and TTR Inc., Kfar Saba, Israel, forged a representation agreement. TTR creates such anti-piracy products as DiscGuard and DiscAudit. With DM Tech representing them, TTR hopes Korean software publishers and content providers will integrate TTR technology into mastering and disk manufacturing.

Arik Shavit, TTR's vice president of business development, marketing, and sales, says, "We feel strongly that DM Tech's strengths, combined with the DiscGuard advantage, now make it easier for Korean software and game developers, publishers, and disk manufacturers to protect their intellectual property and increase market share."

DiscGuard confronts the illegal mass production of software or other electronic contents, as well as the copying done by individual users with CD-ROM recorders. It works by laser marking a permanent digital "signature" on the optical media. The software cannot be used without the signature, which can be read by CD- and DVD-ROM disk drives. In the war against the optical disk piracy, DiscGuard may just leave the pirates with one hook tied behind their backs.

For more information, contact Digital Media Technology Co., 4-522, Electronics Dept. 51-30, Wonhyo 3-ga, Yongsan-gu Seoul, 140-113, Korea, +82 2 7198333; fax +82 2 7198334; KoreaSales@ttrtech.com.—**NK**

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MANAGING THE DESIGN FACTORY

Partial Colocation

In my last column, I wrote about the importance of colocation. As desirable as colocation is, very few product-development teams have the luxury of colocating all of their members for the full duration of the program. Unfortunately, many teams assume that the only alternative to full colocation is to leave the team members with their functional bosses, and invite them periodically to team meetings. I would call this the "all-or-nothing" approach to colocation.

There is another way to approach colocation. We can recognize that it is really a continuum between full colocation and none at all. Interestingly, the intermediate points on this continuum can be very attractive. They frequently capture the benefits of colocation without the disadvantages.

For example, consider the design team that requested a full-time buyer for their team area. "No way," said Purchasing digging in their heels. The design team compromised with a more creative solution. They created a purchasing desk in the team area, and requested that the buyer be there from 8:00 a.m. to 9:00 a.m. every day. The Purchasing Manager was willing to give up his buyer for an hour a day.

DON REINERTSEN

Once this had begun, the team was amazed at how well it worked. Team members no longer had to play phone tag with Purchasing. They knew that once every 24 hours, they could find the buyer in the team area. During his hour in the team area, the buyer devoted his full attention to team business. The overall result was buyer performance equivalent to a full-time, colocated buyer.

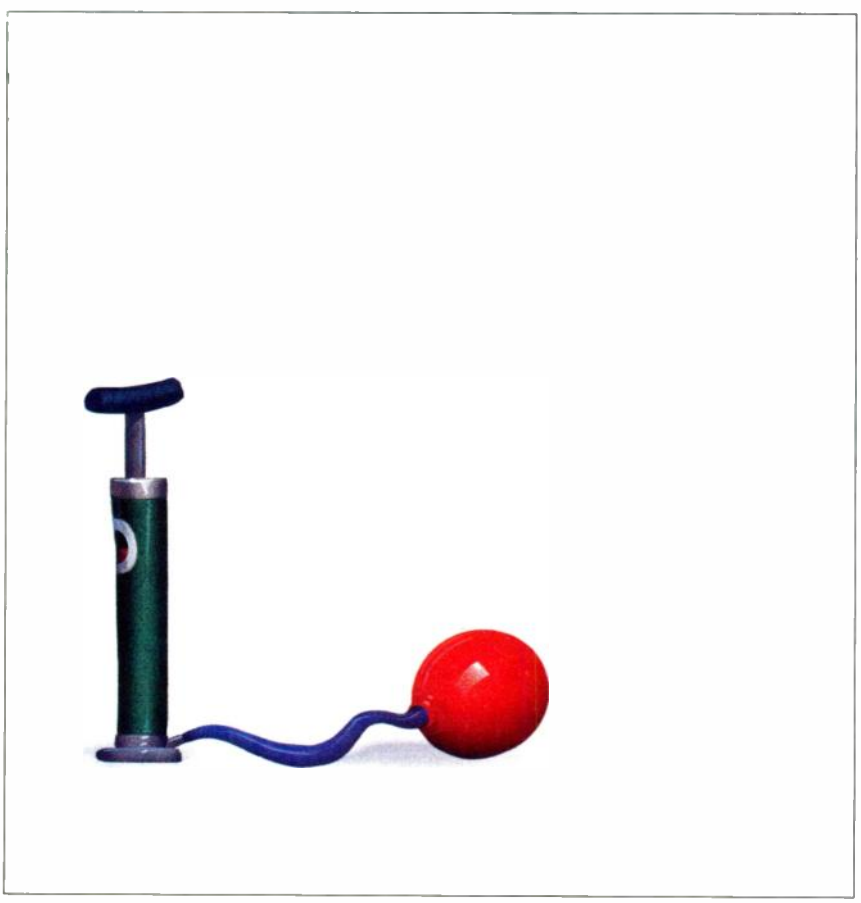
Consider another example. A semiconductor company locates a staff engineer on-site at key fabrication equipment vendors to buy-off this equipment. They find that having an engineer on-site for six months at the supplier gives them many advantages. They get a very accurate picture of project status. They can get problems solved much faster at the vendor site than if they bought off the same equipment at their plant, because all of the vendor's technical people are at the facility. In addition, they get the highest priority. In contrast, competitors who visit periodically get limited attention until a few days before their visit.

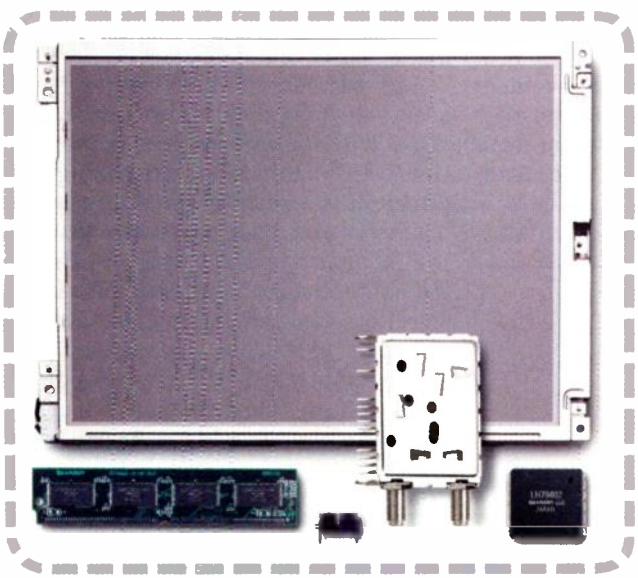
Finally, consider communications equipment manufacturers. They use a manufacturing engineer from a distant manufacturing site to support key development programs. The engineer visits monthly during most of the project. However, during the last eight weeks of the project, the approach changes. The manufacturing engineer physically moves to the site to act as liaison for the plant.

During this period, communication with the plant is critical. Having a plant representative continuously on-site dramatically improves such communication. Later, when the project is transferred to the factory, the manufacturing engineer returns to the plant to manage the ramp-up of the product. In this case, we do not colocate for the full project, just when we have intense communication needs.

In all of the above cases we're not colocating the entire team for the full program. This approach gives us many benefits for a fraction of the cost of full colocation. Try partial colocation. You'll be surprised by how well it works.

Don Reinertsen is president of Reinertsen & Associates, a consulting firm specializing in product development management. He can be reached at (310) 373-5332 or e-mail: DonReinertsen@compuserve.com.





Sharp components and services can help you cook up a thoroughly integrated design.

Even now, designers are aiming to develop kitchens that integrate appliances and automate everything from stocking up to washing down. That parallels Sharp's goal of giving you easy access to a huge range of mouth-watering components . . . and to doing more at our end to mix, blend and adjust them into custom integrated subsystems. For appetizers, consider these recent innovations:

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READER SERVICE 147

KMET'S CORNER

Occasionally, I can't get myself out of a rut. I get stuck, keep my head down, push forward as hard as I can, and usually, accomplish next to nothing. I gather, mostly from the feedback of others, that, while making some progress, they expect more of me. Suggestions come my way like the water pouring off Yosemite falls, but, in spite of the force, I comfortably operate within the artificial barriers of my mind.

This is dangerous, unproductive, self-centered, and self-serving behavior. If I stay in the rut, can I maintain reasonable order in my life, perform effectively on the job, and continue my professional advancement?

When the obvious answer is no, something has to change. How did I get into this state? What factor, or combination of things, keeps me here? What must I do to break out? Situational awareness, which oftentimes comes later rather than sooner, must present itself to initiate an exit strategy. I find it necessary to pay attention to subtle changes, to begin the process of discovery.

RON KMETOVICZ

In recent months, work, the variety of which I must perform to sustain my cash flow, began to accumulate at an alarming rate. I classified the bulk of the backlog into the highly creative bin, the safe place. Here, things just have to wait for that moment of inspiration, the time when the fog clears, and the spark is released that ignites the fire that explodes in a fury of high-octane output. All I had to do was get the routine stuff out of the way, and then wait for inspiration to strike. And wait I did....

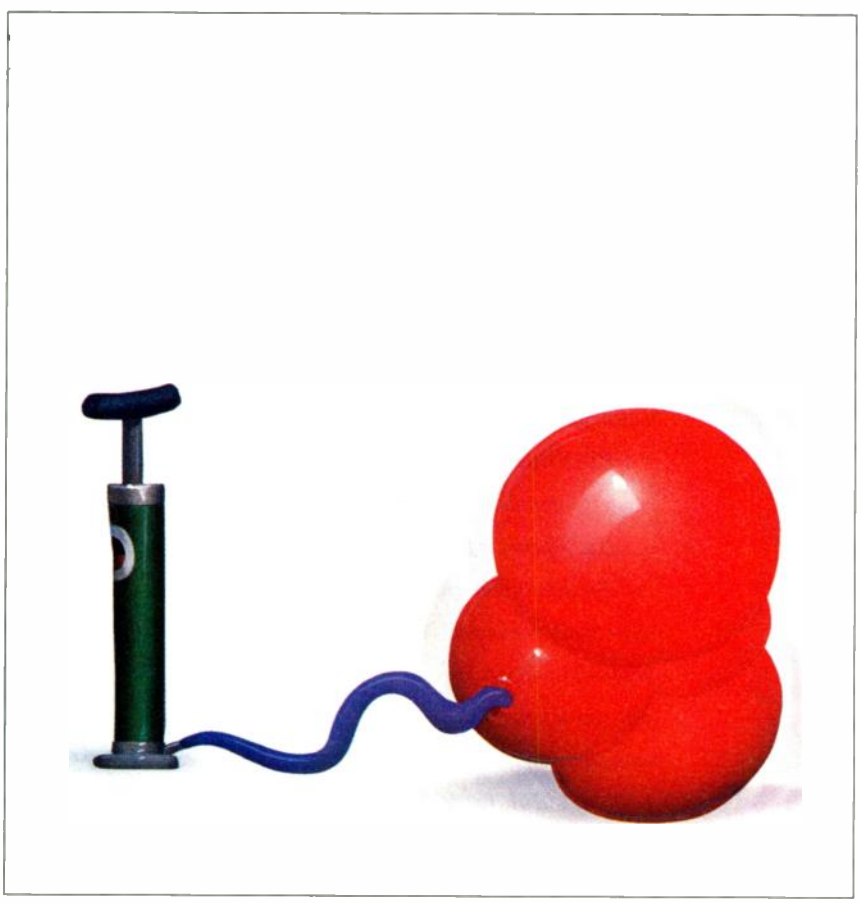
A seemingly unrelated incident, forgetting to pay my cable TV bill, initiated my getting out of the latest rut. I turned on the TV, and no CNBC appeared! My two-dimensional friends Kevin, Maria, and Joe were missing. The Dow and NASDAQ went up and down without my feeling the force of market gravity; others won and lost while I just thought. With the unscrewing of one coaxial connector, I became disconnected from the financial markets of the world, and lost a major source of random noise.

First, I thought of having service reestablished quickly, but then said "No, I'll just do without for a period of time." It hurt, at first, like taking a punch in the gut. I walked around, bent over a bit, and I was irritable.

But, after a few days with no cable TV, subtle change appeared. Some inspiration returned, motivation began to build, and creative thoughts led to the resumption of steady work output. I came to realize that much of my creative energy was being zapped by TV playing in the background. It's gone now, and it will not be back, much to the delight of those who depend on my creative contributions.

So, please take the message of this column into your work environment. Things lurk there to keep you in a rut, and suck up most, if not all, of your creative juices. When that happens, you're robbed of your productivity, and your company's future success is placed at risk. I strongly urge you to go on a mission of discovery, and seek out productivity killers. Where possible, starve them, cut them off from funds—doing so makes them disappear as you prosper.

Ron Kmetovicz, president of Time To Market Associates, is the author of "New Product Development, Design and Analysis." He helps new product development teams deliver profitable products to the market quickly. He can be reached at: P. O. Box 1070, 100 Prickly Pear Rd., Verdi, NV 89439; (702) 345-1455; fax (702) 345-0804; e-mail: kmetovicz@aol.com.



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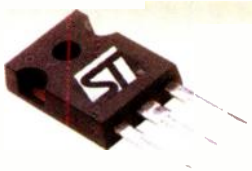

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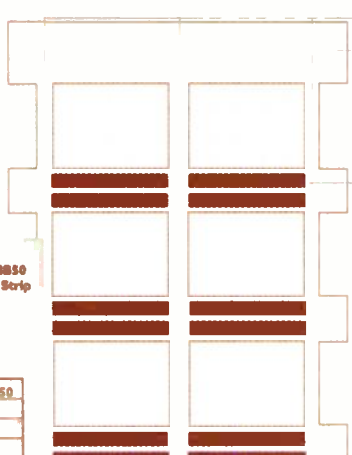

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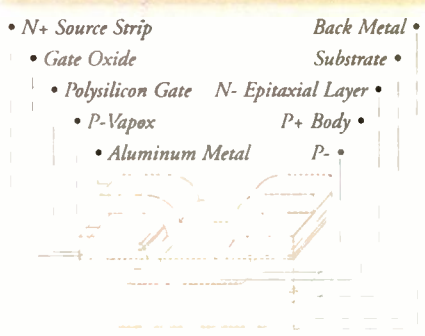

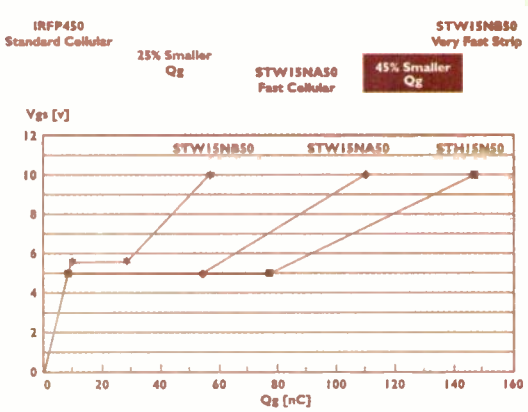

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READER SERVICE 142

THE ENVELOPE, PLEASE

The grand prize of $100,000 goes to...four telecommunications majors from the University of Perugia, Umbria, Italy. They are the lucky winners of Texas Instruments Inc.'s "DSP Solutions Challenge," the worldwide competition for innovative designs based on the company's DSP processors.

Their victory was announced at the recent International Conference on Acoustics, Speech, and Signal Processing (ICASSP), Seattle, Wash. The winning design—the Italian team's DSP solution for terrestrial digital-video broadcasting (DVB-T)—had to compete with 272 entries from 25 other countries. The DVB-T was based on TI's new generation, 32-bit fixed-point DSP architecture, called TMS320C6X.

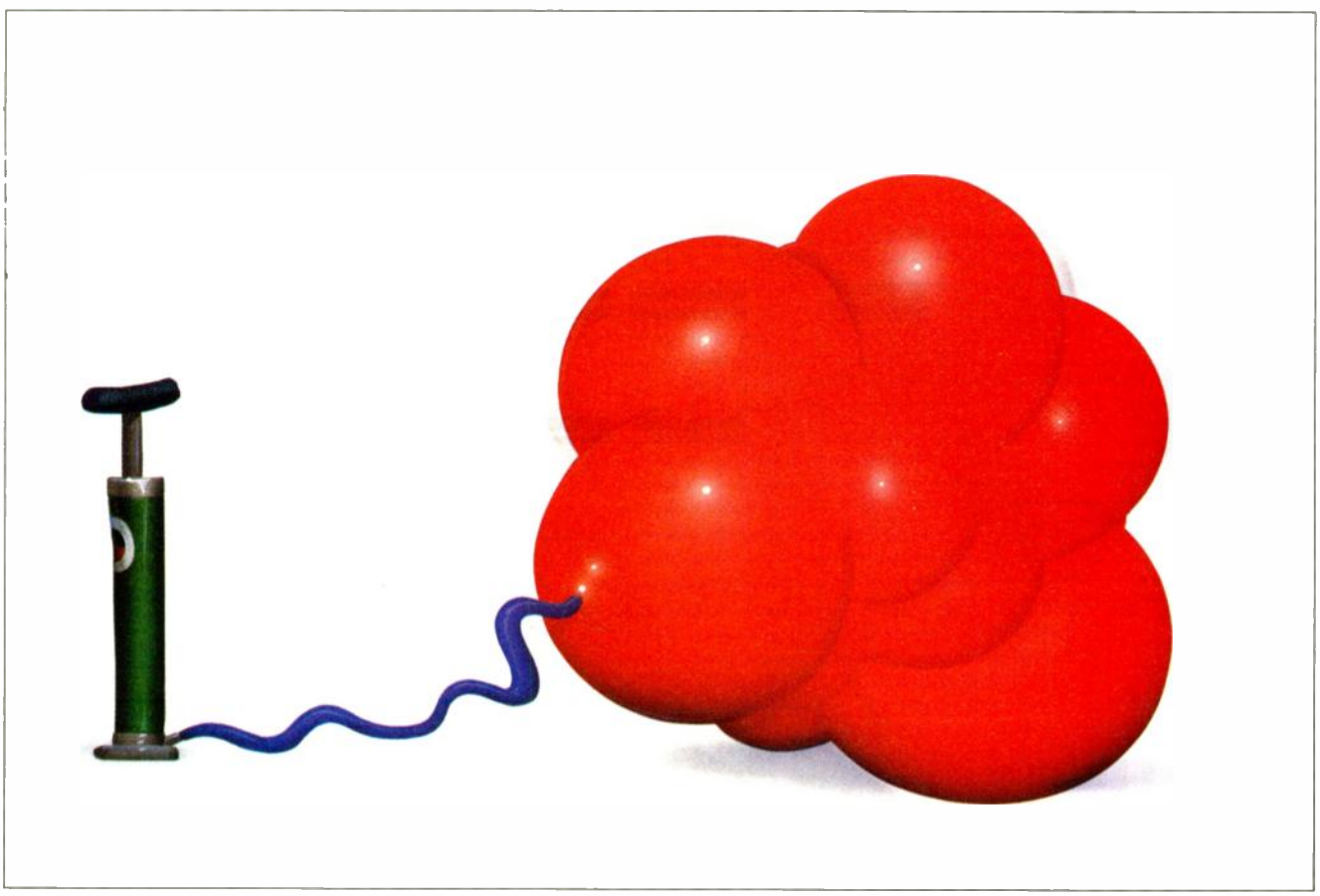
According to Fabrizio Frescura, advising professor to the Italian team, "The adoption of a 32-bit fixed-point architecture leads to a very low implementation loss, allowing it to obtain short processing delays." Short processing delays become meaningful in interactive, multimedia applications of DVB-T because the user is in the loop, clicking the mouse or other controller and waiting for a response. As the time delay becomes shorter, the user is more enticed by an interactive program, and tends to have more patience with it, notes Frescura. The programmable DSP solution also permits the DVB units to provide good quality video processing across varying hardware configurations and channel conditions.

Frescura also emphasized that the problem's complexity demanded a powerful processor with very high speed and precision. The team was able to use TI's TMS320C6201 because it met these requirements. The design implements demodulation, channel estimation, and equalization of the DVB-T signal in the C6201, running at 200 MHz. For this application, the team was required to develop parallel assembly code, using a graphical method for the allocation of the DSP resources.

The $100,000 prize will be shared by Euro Sereni, Stefano Gai, Alessandro Dini, and Stefan Pielmier. Professor Frescura will receive a cash prize of $15,000 and the opportunity to take part in a six-month sabbatical program at TI. To show their gratitude, the four students intend to give a portion of their cash prize to the Institute of Electronics at the University of Perugia. This contribution will finance research activities in the areas of DSP. Professor Frescura plans to donate his prize to the improvement of the Institute's DSP Lab.

For more information on Texas Instruments' University Program, contact them at www.ti.com/sc/university.

Ashok Bindra



TRUDEL TO FORM

We've been talking about how to improve business performance through superior new product development results. Because it's cheaper to copy products than to develop them, the first thing to do is keep competitors from stealing your work. Hence, the patent wars.

As I've said before: "In the past, nations fought wars over trade routes and raw materials. In the future, they will fight wars over the right to market unique products." Why? Because that right decides who gets the high-wage jobs and prosperity. The Cold War was replaced by the trade war.

Such diverse groups as America's Nobel laureates, the venerable Daughters of the American Revolution, and mainstream businessmen like Steve Forbes have joined the battle to save our patent system. As a result, the bill in Congress, S.507, to sell the patent office is stalled. I expect wannabe technology Czar Lehman will "resign" before this column runs.

Enough money is involved that the patent wars will continue at least until Washington fixes its "foreign donation" problem, but we're probably safe until after the elections. (We are the only major nation that hasn't outlawed foreign lobbying.) I am very happy to get back to my business and my life. I will keep news updates posted on my web page.

Let's talk about strategy, starting at a high level. The results of an effective strategy can be surprising. Consider Vietnam. Each side had a focused strategy, and each strategy was fully successful. America's was to win the military battles. North Vietnam's was to make the war costly in lives and win politically. In the end only one strategy mattered, theirs, but that wasn't clear until the end.

Information Age business faces a similar paradox. The West's economic strategy, especially America's, is to maximize profits. Where once the business schools taught that the purpose of business was to create customers, they now say business is about creating profits. That view makes cost-cutting popular, because it takes less skill to cut costs than to raise margins and sales.

The Pacific Rim strategy, led by Japan, is one of conquest, not profits. Listings of the largest firms in critical industries (banking, electronics, autos, etc.) show Japanese domination. If you list them by profits, American firms dominate.

JOHN D. TRUDEL

Wall Street says our system is better. Japanese policy setters like Fumio Kodama say theirs has won. His book, *Emerging Patterns of Innovation*, published by Harvard Business Press, is reviewed on my web site. Most strategies have problems—we lose good jobs and suffer trade imbalance, they have financial crises.

Today most people buy Pacific Rim products, but invest in U.S. stocks. Foreign lobbying is mostly legal. Commercial technology theft is mostly ignored.

That's the top-level picture. What are the strategic implications for engineers and technical managers in companies? In any given industry, about 80% of firms have been pursuing "cheaper and faster" as a generic strategy. This has made fast cycles and reengineering popular, but it has not led to sustained profits. Opportunities abound. Next time, we'll talk about how to renew corporations through innovation. In the Information Age, firms with unique, compelling products will prosper.

John D. Trudel, CMC, provides business innovation consulting services. He is the author of "Engines of Prosperity." The Trudel Group, 33470 Chinook Pl., Scappoose, OR 97056; (503) 638-8644; fax (503) 543-6361; e-mail: jtrudel@gstis.net; www.trudelgroup.com.

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JUST 4 THE KIDS

Do you have a young adult in the house who needs a little prodding before beginning a project? Does your teen complain about being bored by textbooks and laboratory science, but interested in anything to do with a computer? If you answered yes to any of these questions, this may be the thing for you; Stanford University's HAIL (Holographic Array for Ionospheric Lighting) Project.

Project HAIL is jointly funded by the National Science Foundation, Arlington, Va., and the Office of Naval Research, Arlington, Va., and is headed by Stanford electrical engineering professor, Umran Inan. It is an ongoing experiment that employs very low frequency (VLF) transmissions used by the US Navy for communications. Electromagnetic pulses, generated by lightning strokes, affect the ionosphere, and they are the subject of the study. The ionosphere is a region of electrically charged particles that exists about sixty miles overhead. Every minute, one thousand lightning strokes occur around the world. The flow of electrical charge between the ground and atmosphere makes lightning a vital link in, what scientists term, the global electric circuit. It may have an important influence on the Earth's climate.

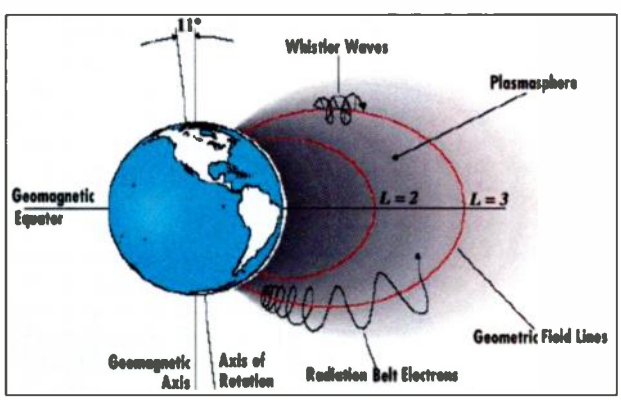
To help, researchers are measuring the size, shape, and duration of changes in the ionosphere caused by lightning. This is done by measuring changes in the strength and phase of VLF radio signals that travel intercontinental distances. This information can be used to understand lightning's impact on the upper atmosphere.

Much of the information is gathered using radio remote sensing methods. These methods probe regions of the atmosphere too high for weather balloons and too low for orbiting satellites. Radio remote sensing comes into use at ground stations. Ground stations are located where the receivers can pick up VLF signals after they've passed through areas of high lightening activity. Each location generates huge amounts of data; Stanford researchers only have the time and staff to examine about ten percent. So researchers decided to link the project with an educational outreach program. This program lets high school students provide the resources needed to help gather and analyze data.

MARIFRANCES WILLIAMS

A Stanford student outreach team, headed by Michael Johnson, set up receiving stations in eight high schools, five in Colorado and three in eastern Canada. Johnson visited each school to help bolster support for the project. He's given talks to teachers and students explaining how the instruments work and what they are measuring. He also kept a diary of his travels to an Antarctic ground station that can be accessed on the web, along with project information. Students can even e-mail questions directly to Johnson.

Participants are able to uncover details by gathering the data, and analyzing it as well. To help the students, Stanford researchers developed a computer program that starts and stops the data acquisition each day, and transfers the files to Stanford. This is important because students and teachers sometimes can't work on the project every day. Web pages and interactive tutorials have also been developed to explain the experiment to the students. A Java data-viewing program lets those interested view and download experimental data over the internet. Researchers are hoping this will allow students to access the data and pass it on to others. Hoping to involve students from many locations, researchers set the project up so that you don't need to attend a participating school to join in.



Since this field is relatively new and first order effects are still being looked at, participants can make unique scientific discoveries. To help students get started, Johnson offers several ideas for simple projects that require the student to read the information on web pages. They are:

1. Look at the data from one of the schools a few times a week. Choose a transmitter, look at the amplitude data for it, and write down an estimate of the average amplitude during a time period. After the period of time, plot these amplitudes. How do they change? Can you find information about solar and/or geomagnetic indices from other science groups? Are these measurements related?

2. During the sunrise and sunset a change in the amplitude of the transmitters is visible. Are these at the same time for the different transmitters? Why? How does this change with time (take measurements over several months)? Draw the shape of this curve each time you look at it. Study how it changes over the course of a season.

So, if this sounds like it might receive an enthusiastic response from a student you know, contact Professor Umran Inan, Durand 321/Starlab, Stanford University, Stanford, California 94305-9515; (650)723-4994;inan@nova.stanford.edu; or Michael Johnson, Stanford's Electrical Engineering; (650) 725-8446 or mikej@leland.stanford.edu.

Marifrances D. Williams holds a degree in Liberal Studies from San Diego State University, Calif. She is currently a fifth-grade teacher at Los Ranchos Elementary, San Luis Obispo, Calif. Williams specializes in the identification of advanced technology for the use of child-focused applications. She may be reached at williamsofsm@lightspeed.net.

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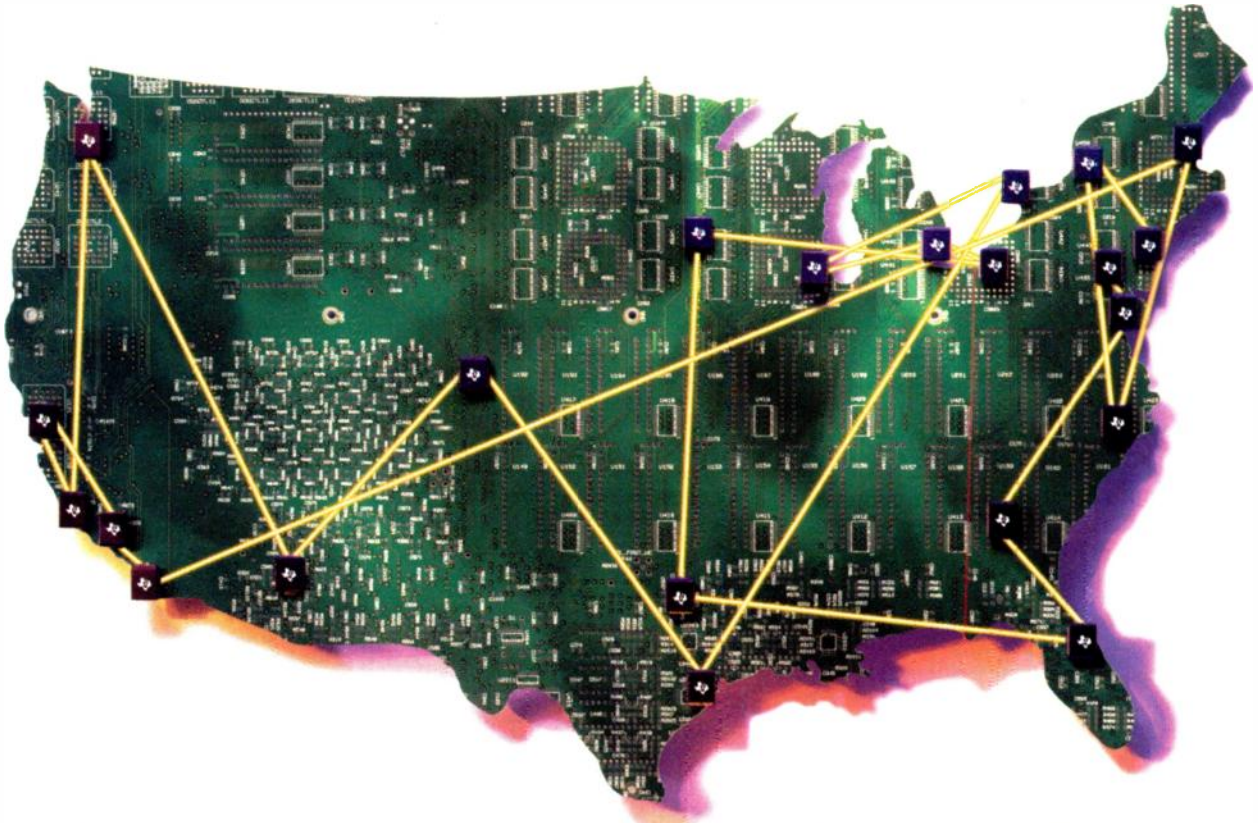

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HOW DOES IT SOUND?

Tube Freaks Hit The Motherlode

Sometimes the best rules of thumb are discovered in old volumes, especially tips on how to build high quality, tube-based audio amplifiers. Printed in 1954, "Valves For Audio Frequency Amplifiers," by E. Rodenhaus, is part of the Philips Technical Library. A practical, 144-page volume, it may well be the DIY "motherlode" for those audiophiles who eschew the sonic harshness of transistor for the soft, rounded edges of the tube.

The six chapter handbook begins with general hints on amplifier construction. Key to the discussion is the issue of hum. A good deal of space is devoted to eliminating this audio nemesis, focusing mostly on overall layout and assembly and wiring techniques. Chapter 2 outlines the valves for the various stages, and then describes, in detail, the following valves: EF 40, EF 86, ECC 40, ECC 83, EL 34, EL 84, and GZ 34. All charts, graphs, performance specifications, and ratings are provided, followed by hints on practical uses of the valve data.

Hints on practical uses of the valve data are supplied in chapter 4. Chapter 5 discusses components and circuits, with analysis of negative feedback and tone control, as well as the output transformer, microphones, and pickups. This is followed by a slew of practical amplifier-circuit implementations. Descriptions range from a 100-W amplifier with two EL 34 output valves in Class B operation, to a 3-W gramophone amplifier with two EL 84s in push-pull operation (for the real nostalgist).

Want to use this resource for "rolling your own" tube-based amplifiers? Then pay attention to the included disclaimer: "Philips no longer manufactures the valves referred to in this publication, and regrets it cannot engage itself in answering any inquiries from those who build the circuits." Unfortunate for some, but practical overall. Tubes have had their day in the sun. Let's focus on advancing the present, instead of regurgitating the past. For those diehard enthusiasts or victims of nostalgia still interested, the handbook costs $16.95, and is available from Audio Amateur Corp., Peterborough, Pa. Contact Laurel Humphrey at (603) 924-9464.

Quad Amp Has True FET Input

On a more modern note, Burr-Brown has introduced its SoundPLUS OPA4134 true-FET-input-stage quad amplifier. The amp's fully cascaded input stage minimizes distortion by ensuring that the bias current remains virtually unchanged throughout the full common-mode range.

Features include a total harmonic distortion of 0.00008%, a gain bandwidth of 8 MHz, a 20-V/ms slew rate, a noise level of 8 nV/MHz, and a 5-pA input bias current. The supply range is ±2.5 to ±18 V. The amplifier is available in 14-pin DIP and SO-14 surface-mount packages, and is specified for -40° to 85°C operation. Pricing is $1.70 each per 1000; delivery is from stock. Contact Linda Lopez at Burr-Brown Corp., 6730 S. Tucson Rd., Tucson, AZ 85706; (520) 746-1111; fax (520) 746-7401.

Capacitors Set To Aim For High-Quality Audio Use

Take a variety of metallized polypropylene capacitors, wrap them in plastic, and fit them into plastic or aluminum boxes. Then make them one part of a line of high-quality capacitors which specifically target high-end audio applications. Available with aluminum or tin-foil armatures, which minimize losses from the Joule effect, the devices come in nominal voltages from 100 to 1500.

The capacitance tolerance ranges from ±2 to ±5%. The operating temperature reaches -25° to 70°C, and the loss angle is less than 15×10^{-4} at 10 kHz. No piezoelectric effect is exhibited. For more information, contact Corinne Ajinca, Societe des Condensateurs Record, 17 Blvd. d'Anvaux, Z.I., 36000 Chateauroux, France; +33 254222724; fax +33 254340136.

Patrick Mannion

@IEEE

To make itself even more accessible to IEEE members, *Today's Engineer* has just put its publication online. It also has launched a package full of new and convenient offers. *Today's Engineer* boasts of being the only magazine entirely devoted to developing an engineer's nontraditional professional skills.

"Although *Today's Engineer* is aimed at engineers of all disciplines, it is published by IEEE-USA, which has a mandate from the IEEE Board to disseminate this valuable resource to members both here in the United States and worldwide," says Gus Gaynor, editor-in-chief. "Our new web version contains all of the content of the printed version, and will be simultaneously available—at the click of a mouse button—to readers all over the globe," he says.

The site contains articles promoting the development of cutting-edge professional skills. They also focus on providing a greater understanding of technical fundamentals. Pieces concentrate on improving the engineer's ability to think critically, creatively, independently, and cooperatively. The magazine encourages interpersonal and communications skills and, of course, high ethical standards.

The first two issues are currently available online. Any member that completes a short registration form (found on the web site) will receive the first two issues free. Members that visit the web site can subscribe for the rest of the year at half the usual price. A member subscription for both the web and printed version in 1998 is $8. The printed version alone costs $6.50, and the web version is $5. Nonmembers can subscribe to both versions for $16, the printed version at $12.95, or to the web for $10.

For more information or to subscribe, contact *Today's Engineer* at (800) 678-IEEE; (732) 981-0060; or visit the web page at www.todaysengineers.org.

Lisa Calabrese

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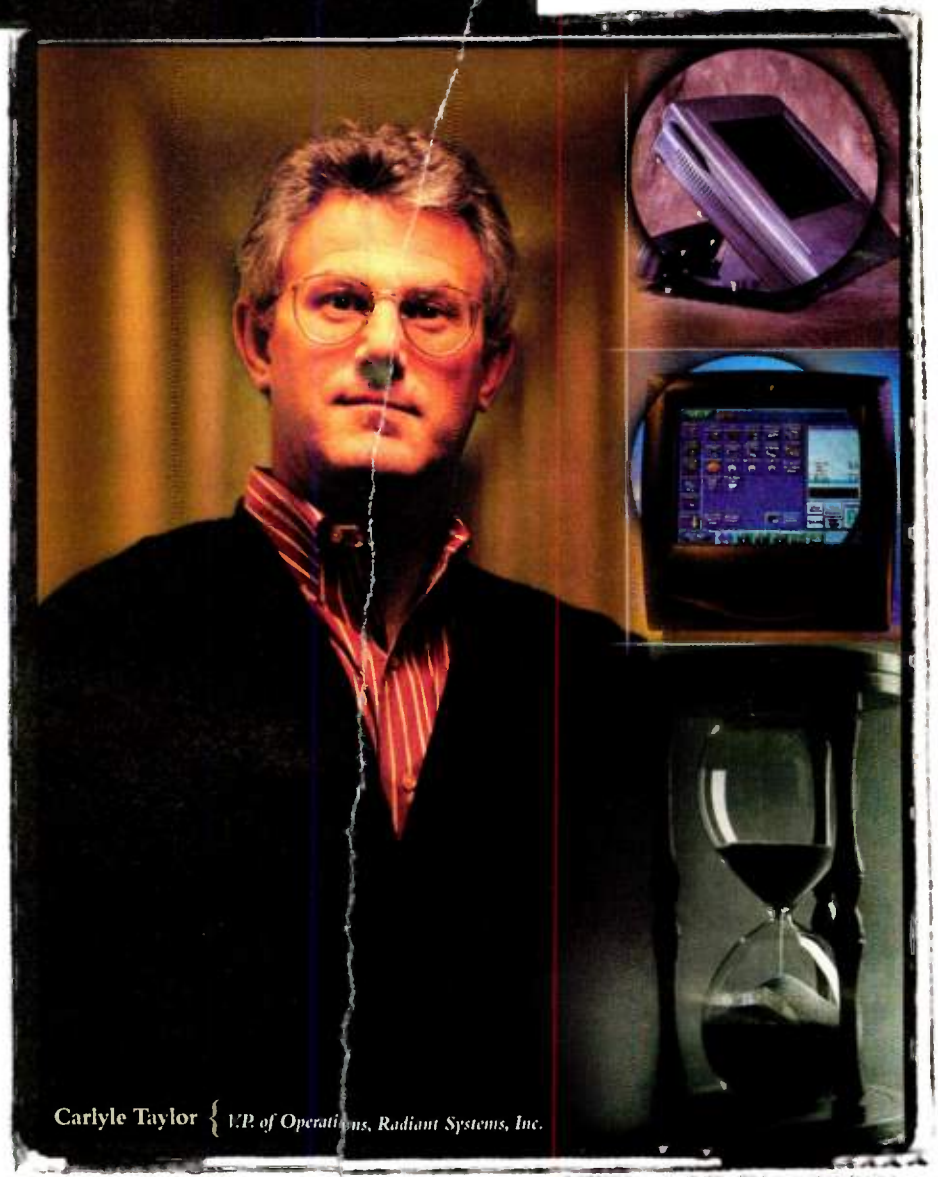

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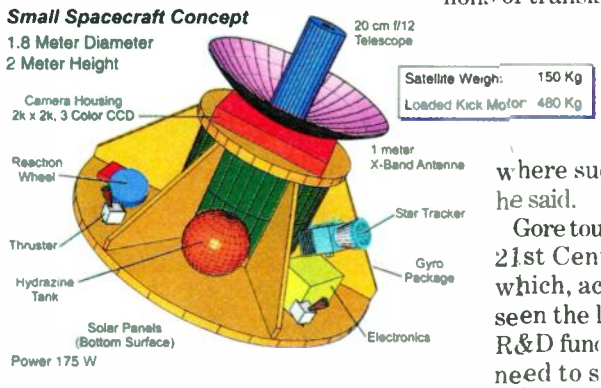
READER SERVICE #54

Gore Proposes Earth-View Satellite

In a speech at the National Innovation Summit at the Massachusetts Institute of Technology, Boston, Vice President Al Gore proposed that NASA scientists and engineers design, build, and operate a satellite providing live images of the Earth, 24 hours a day on the Internet.

Called Triana, the new satellite will be carried to low earth orbit, where a small motor will bring it out to 1-million miles from earth orbit, at the L1 point. Short for the Lagrangian libration point, L1 is the point between the Earth and sun where gravitational attractions are balanced.

Gore remarked that in the history of space exploration, there are few images of the full Earth. They include the famous "Earth Rising," shown in 1968, the "Blue Marble" image taken in 1972 by Apollo 17, and a short video feed from the Galileo satellite as it sped from earth. The 1972 image is the most widely printed photograph in the world.



The proposed Triana satellite is expected to be in place by 2000. Aside from its basic 24-hour video duty, it will be used for scientific projects and global weather observations.

Weighing approximately 330 lbs. and requiring 175 W of power, the craft will interface to three simple, low-cost ground satellites spaced equally around the globe to provide continuous downlink capability. One new downlinked image will arrive every few minutes. The maximum downlink speed will be 200 kbits/second maximum, resulting in a download time of two minutes per image. NASA plans to develop and build the craft within two years of competitive selection. Total cost is estimated at less than $50 million, including launch and operations.

Triana's basic payload will include an 8-in. diameter telescope paired with a full-color camera featuring a 2000-by-2000-pixel digital detector. Such a detector can provide better resolution than an HDTV image. The satellite also will carry solar panels for electrical power, an X-band radio for communications, hydrazine propellant, a star tracker, gyros, and reaction wheels for attitude control.

The day before his speech, Gore had returned from a meeting with Silicon Valley heavyweights. He remarked on insights he'd gained there, as well as the bright future of electronics technology. "Our economy is now driven by innovations," he said, "We are at the dawn of a true information age." Within three years there will be chips with billions of transistors, and wireless communication of up to 6.5 Gbit/s to and from any point on earth. "Sometimes it takes decades to know where such leaps are taking us," he said.

Gore touted the Administration's 21st Century Research Funds, which, according to the VP, has seen the largest increase ever in R&D funding. He emphasized the need to streamline U.S. patent laws by converting the Patent Office into an organization with a CEO and measured results.

In another speech at the Summit, Michael Porter, Harvard professor, presented data measuring the innovation performance of various countries, based on patents per capita among nations worldwide. The data revealed that adding government people results in a negative trend, while adding government funding is a positive trend.

Summarizing his data, Porter said "Innovation is more than just science. It's an economy where markets thrive and capital investments are plentiful."

For more information on the satellite, contact NASA, 300 E St. SW, Washington, D.C. 20546; (202) 358-1600. For more information on the National Innovation Summit, contact the Council on Competitiveness, 1401 H St. NW, Suite 650, Washington, D.C. 20005, (202) 682-4292.

Jeff Child

HOT PC PRODUCT

Instead of old, networked hard disks, you can use CD and DVD to store and retrieve data. Smart Storage Inc., Anaheim, Calif., introduced its SmartCD v. 3.0 software designed for Windows NT. It utilizes Universal Disk Format (UDF) standards to offer packet writing, DVD, and Macintosh support.

SmartCD v. 3.0 offers read/write network CD and DVD storage for Windows 3.x, 95, and NT, as well as UNIX, Macintosh, and media formats. It manages the CD and DVD media, permitting users to read and write from the storage device. By using the software to add a CD or DVD storage system to the network, you can store documents, imaging, prepress, CAD, and data.

Michael Peterson, president of Strategic Research Corp., comments, "Over the last few years, CD has established itself as a leading storage technology. Now DVD with its increased storage capabilities, will quickly gather market share. By making the CD and DVD drives appear and function just like the network hard disk, these storage technologies gain significant appeal for mainstream applications."

The SmartCD v. 3.0 has many new features. "UDF Drive-Letter Access" is a read/write file system which lets users utilize SmartCD as a networked hard disk. The "Capacity Management" option lets directories span multiple media and introduce data in a common directory.

"DVD Support" allows access to terabytes of information on DVD-ROM, UDF, ISO9660, and standard DVD discs. It's also compatible with recordable DVD formats. With "Macintosh Support" for Windows NT environments, Mac users can add HFS CDs to the file system. Finally, "Off-Line Media Management" lets administrators store CD and DVD media magazines off-line.

SmartCD v. 3.0 starts at $1640.

For more information, contact Smart Storage Inc., 100 Burtt Rd., Andover, MA 01810; (978) 623-3300; fax (978) 623-3310; e-mail: www.smartstorage.com.—**NK**

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- 1 - 4 Outputs
- Low Cost

Deltron inc.
POWER PRODUCTS

VR SERIES HI-REL SWITCHERS

Single Output • 300-700 Watts

DESCRIPTION

VR Series World Class switching power supplies are a family of single output models designed for applications requiring ***Ultra Reliability*** and ***Low Cost!*** These supplies have actual demonstrated MTBF ratings up to 1 million hours. The time tested design has been continually updated to take advantage of the latest technological improvements in circuits and components resulting in the fine performance of these supplies.

MODELS & RATINGS

Max Power	Output	Model
300W	5V @ 50A	VR300AXX
	12V @ 25A	VR300BXX
	15V @ 20A	VR300CXX
	24V @ 12A	VR300DXX
	48V @ 6A	VR300EXX
500W	5V @ 80A	VR500AXX
	12V @ 40A	VR500BXX
	15V @ 30A	VR500CXX
	24V @ 20A	VR500DXX
	48V @ 10A	VR500EXX
700W	5V @120A	VR700AXX
	12V @ 58A	VR700BXX
	15V @ 46A	VR700CXX
	24V @ 29A	VR700DXX
	48V @ 15A	VR700EXX

FEATURES

- *UL, CSA, TÜV (IEC, EN), CE.*
- *5.5 watts per cubic inch.*
- *80% typical efficiency.*
- *1,000,000 hrs. demonstrated MTBF.*
- *Stock delivery.*
- *Full complement of options.*

VR OPTIONS

Option Code	Function
00	None
01	Power Fail Monitor
02	Auto Ranger
04	Pilot Bias
08	Screen Cover
16	End Fan Cover
32	Top Fan Cover

To order, replace "XX" in model number with sum of Option Codes desired.

CV SERIES ENCLOSED SWITCHERS

Single Output • 360-600 Watts

DESCRIPTION

The CV Series is a line of low profile, fan cooled power supplies which utilize Deltron's field proven V Series components. CV units are single output models in a rugged enclosed package nominally 3 inches in height and 5 inches in width. With power ratings of 360 to 600 watts, these units are a space saving alternative to 5 x 8 inch shoe box modules.

MODELS & RATINGS

Max Power	Output	Model
360W	5V @ 72A	CV360AXX
	12V @ 30A	CV360BXX
	15V @ 24A	CV360CXX
	24V @ 15A	CV360DXX
	28V @ 13A	CV360JXX
	48V @ 7.5A	CV360EXX
500W	5V @ 100A	CV501AXX
	12V @ 42A	CV501BXX
	15V @ 33A	CV501CXX
	24V @ 21A	CV501DXX
	28V @ 18A	CV501JXX
	48V @10.5A	CV501EXX
600W	5V @ 120A	CV601AXX
	12V @ 50A	CV601BXX
	15V @ 40A	CV601CXX
	24V @ 25A	CV601DXX
	28V @21.5A	CV601JXX
	48V @12.5A	CV601EXX

FEATURES

- *UL, CSA, TÜV (IEC, EN), CE.*
- *4 watts per cubic inch.*
- *80% typical efficiency.*
- *200,000 hrs. demonstrated MTBF.*
- *Heavy duty enclosed chassis.*
- *Full complement of options.*

CV OPTIONS

Option Code	Function
00	None
02	Power Fail Monitor
04	Thermal Shutdown
08	Logic Inhibit
16	Auto Ranger

To order, replace "XX" in model number with sum of Option Codes desired.

V SERIES OPEN FRAME SWITCHERS

Single & Quad Outputs • 120-600 Watts

DESCRIPTION

V Series World Class switching power supplies are a family of single and quad output models designed for a wide variety of commercial and industrial applications. These industrial workhorses have demonstrated MTBF ratings greater than 500,000 hours. A proprietary proportional drive circuit prevents excess switch saturation and permits higher switching frequency operation. This makes possible increased reliability and a compact size.

One of the unique features of the V Series is a dual loop regulation system. This system provides a tightly regulated main output and eliminates cross regulation in the auxiliaries.

FEATURES

- *UL, CSA, TÜV (IEC, EN), CE.*
- *4.8 watts per cubic inch.*
- *80% typical efficiency.*
- *500,000 hrs. demonstrated MTBF.*
- *High power auxiliaries.*
- *High peak current capability.*
- *Full complement of options.*

SINGLE OUTPUT

Max Power	Output	Model
120W	5V @ 25A	V120AXX
	12V @ 10A	V120BXX
	15V @ 8A	V120CXX
	24V @ 5A	V120DXX
180W	5V @ 36A	V180AXX
	12V @ 15A	V180BXX
	15V @ 12A	V180CXX
	24V @ 7.5A	V180DXX
250W	5V @ 50A	V250AXX
	12V @ 21A	V250BXX
	15V @ 17A	V250CXX
	24V @ 11A	V250DXX

Max Power	Output	Model
270W	5V @ 54A	V270AXX
	12V @ 22A	V270BXX
	15V @ 18A	V270CXX
	24V @ 12A	V270DXX
360W	5V @ 72A	V360AXX
	12V @ 30A	V360BXX
	15V @ 24A	V360CXX
	24V @ 15A	V360DXX

Other voltages, e.g. 2V, 3.3V, 28V, and 48V available on special order.

Max Power	Output	Model
500W	5V @100A	V501AXX
	12V @ 42A	V501BXX
	15V @ 33A	V501CXX
	24V @ 21A	V501DXX
600W	5V @120A	V601AXX
	12V @ 50A	V601BXX
	15V @ 40A	V601CXX
	24V @ 25A	V601DXX

QUAD OUTPUT

Max Power	Output 1	Output 2	Output 3	Output 4	Model
225W	5V @ 30A	+12V @ 6(12)A	-12V @ 4A	-5V @ 4A	V225AXX
	5V @ 30A	+12V @ 6A	-12V @ 4A	+24V @ 4(8)A	V225BXX
	5V @ 30A	+15V @ 6(12)A	-15V @ 4A	-5V @ 4A	V225CXX
	5V @ 30A	+15V @ 6A	-15V @ 4A	+24V @ 4(8)A	V225DXX
	5V @ 30A	+12V @ 6(12)A	-12V @ 4A	+12V @ 4A	V225EXX
300W	5V @ 40A	+12V @ 4A	-12V @ 4A	-5V @ 3A	V300AXX
	5V @ 40A	+12V @ 4A	-12V @ 4A	+24V @ 3(5)A	V300BXX
	5V @ 40A	+15V @ 4A	-15V @ 4A	-5V @ 3A	V300CXX
	5V @ 40A	+15V @ 4A	-15V @ 4A	+24V @ 3(5)A	V300DXX
	5V @ 40A	+12V @ 4A	-12V @ 4A	+12V @ 3(5)A	V300EXX
325W	5V @ 45A	+12V @ 8(16)A	-12V @ 6A	-5V @ 4A	V325AXX
	5V @ 45A	+12V @ 8A	-12V @ 6A	+24V @ 4(8)A	V325BXX
	5V @ 45A	+15V @ 8(16)A	-15V @ 6A	-5V @ 4A	V325CXX
	5V @ 45A	+15V @ 8A	-15V @ 6A	+24V @ 4(8)A	V325DXX
	5V @ 45A	+12V @ 8(16)A	-12V @ 6A	+12V @ 4A	V325EXX
400W	5V @ 50A	+12V @ 8A	-12V @ 8A	-5V @ 4A	V400AXX
	5V @ 50A	+12V @ 8A	-12V @ 8A	+24V @ 4(6)A	V400BXX
	5V @ 50A	+15V @ 8A	-15V @ 8A	-5V @ 4A	V400CXX
	5V @ 50A	+15V @ 8A	-15V @ 8A	+24V @ 4(6)A	V400DXX
	5V @ 50A	+12V @ 8A	-12V @ 8A	+12V @ 4(6)A	V400EXX
500W	5V @ 60A	+12V @ 10A	-12V @ 10A	-5V @ 5A	V500AXX
	5V @ 60A	+12V @ 10A	-12V @ 10A	+24V @ 5(8)A	V500BXX
	5V @ 60A	+15V @ 10A	-15V @ 10A	-5V @ 5A	V500CXX
	5V @ 60A	+15V @ 10A	-15V @ 10A	+24V @ 5(8)A	V500DXX
	5V @ 60A	+12V @ 10A	-12V @ 10A	+12V @ 5(8)A	V500EXX
600W	5V @ 80A	+12V @ 10(20)A	-12V @ 10A	-5V @ 5A	V600AXX
	5V @ 80A	+12V @ 10A	-12V @ 10A	+24V @ 5(10)A	V600BXX
	5V @ 80A	+15V @ 10(20)A	-15V @ 10A	-5V @ 5A	V600CXX
	5V @ 80A	+15V @ 10A	-15V @ 10A	+24V @ 5(10)A	V600DXX
	5V @ 80A	+12V @ 10(20)A	-12V @ 10A	+12V @ 5A	V600EXX

V OPTIONS

Option Code	Function
00	None
01	OVP protects all auxiliaries
02	Power Fail Monitor
04	Thermal Shutdown
08	Cover
16	Logic Inhibit
32	Post Regulator for output 4

To order, replace "XX" in model number with sum of Option Codes desired.

NOTES:

1. *Numbers in parentheses ( ) are peak ratings for short duration service such as motor starting.*
2. *Output 1 is floating and can be either polarity.*
3. *Quads require 10% of maximum power distributed among auxiliary outputs for optimum performance.*
4. *Outputs can operate to no load with slight increase in specifications.*

SPECIFICATIONS

INPUT
90-132 VAC or 180-264 VAC, 47-440 Hz.
Consult factory for 400 Hz. operation.

EMISSIONS
FCC 20780 Part 15/EN 55022, Class A Conducted.
EN 61000-3-3, Voltage Fluctuations.

IMMUNITY
IEC 1000-4-2/EN 61000-4-2, Electrostatic Discharge.
IEC 1000-4-3/EN 61000-4-3, Radiated Field.
IEC 1000-4-4/EN 61000-4-4, Electrical Fast Transients.
IEC 1000-4-5/EN 61000-4-5, Level 3 Surge.
IEC 1000-4-6/EN 61000-4-6, Conducted Field.

INPUT SURGE
17 amps peak from cold start for models up to 250 watts and VR300, 68 amps for other models, from nominal 110 or 220 VAC.

EFFICIENCY
80% typical.

HOLDUP TIME
20 milliseconds after loss of nominal AC power.

OUTPUTS
See table of models.

LINE REGULATION
±0.1% for line change from nominal to min. or max. rating with 20% min. load on the measured output.
±0.05% with post regulator and no min. load.
Singles to no load.

LOAD REGULATION

5V main/singles	±0.2%
-5V aux.	±3%
±12V aux.	±2%
±15V aux.	±2%
+24V aux.	±1.5%

Post Regulated Outputs
Option 32 ±0.05%

for load change from 60% to 20% or 100% max. rating. With post regulator to no load. Singles to no load.

CROSS REGULATION
±0.2% for load change on the main 5V output from 75% to 50% or 100% max. rating with 20% min. load on the measured output.
±0.05% with post regulator and no min. load.
Not applicable to singles.

CENTERING

5V main/singles		±5% trim adj.
Aux. 1 and 2		±5% trim adj. tracking
Aux. 3:	-5V	±3%
	+12V	±2%
	+24V	±1%

with all outputs loaded to 50% max. ratings and output #2 set precisely at its rated value. With post regulator ±3% trim adj.

RIPPLE & NOISE
1% or 100 mV, pk.-pk., 20 MHz bandwidth.

OPERATING TEMPERATURE
0-70°C. Derate 2.5%/°C above 50°C.

COOLING

Models	Forced Air
V120, V180, V225, V250, V270, V300, VR300, V360	30 CFM
V325, V400, V500, VR500, V501, V600, V601, VR700	60 CFM

TEMPERATURE COEFFICIENT

5V main/singles	±0.02%/°C
Auxiliaries	±0.05%/°C
With post regulator	±0.02%/°C

DYNAMIC RESPONSE
Peak transient less than ±2% or ±200 mV for step load change from 75% to 50% or 100% max. ratings.

RECOVERY TIME
Less than 400 microseconds on main/singles output.
Less than 50 microseconds on post regulated auxiliaries.

SAFETY
Units meet UL 1950, CSA 22.2 No. 950, EN 60 950, IEC 950.

DIELECTRIC WITHSTAND
3750 VRMS input to ground.
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700 VDC output to ground.

SPACING
8 mm primary to secondary.
4 mm primary to grounded circuits.

LEAKAGE CURRENT
0.75 mA at 115 VAC, 60 Hz. input.

INPUT UNDERVOLTAGE
Proprietary proportional drive and low voltage lockout protects against damage for undervoltage operation.

SOFT START
Units have soft start feature to protect critical components.

OVERVOLTAGE PROTECTION
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REVERSE VOLTAGE PROTECTION
All outputs are protected up to load ratings.

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MODELS	H	x	W	x	L
VR300	2.50"	x	4.85"	x	8.50"
VR500, VR700	2.75"	x	4.85"	x	10.50"
CV360, CV501, CV601	3.15"	x	4.85"	x	12.63"
V120, V180, V250	2.50"	x	4.75"	x	8.50"
V270, V360, V501, V601	2.50"	x	4.75"	x	10.50"
V225, V325	2.50"	x	5.00"	x	10.50"
V300, V400, V500, V600	2.75"	x	5.00"	x	13.00"

OPTIONS & ACCESSORIES

POWER FAIL MONITOR
Optional monitor provides a TTL signal 2 ms. min. prior to loss of output power with outputs fully loaded from 100VAC/200VAC line loss.

THERMAL SHUTDOWN
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COVERS
Optional end and top fan covers for VR Series.
Optional safety/EMI cover for V Series.

INHIBIT
TTL logic inhibit input. Standard for VR Series. Optional for CV and V Series.

PILOT BIAS
Optional for VR Series only. SELV 5V @ 1A source for external use with provision for operating the inhibit either with a switch or TTL Logic. Either NO or NC can be selected.

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Special circuit provides automatic operation at specified input ranges without strapping. Optional for VR and CV Series. For V Series specify AR-1 accessory.

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SOC And Deep-Submicron Technology Drive New DFT Strategies

Designers Look To ATPG, Boundary Scan, And Various Flavors Of BIST To Test Increasingly Complex ICs

Joseph Desposito

SPECIAL REPORT

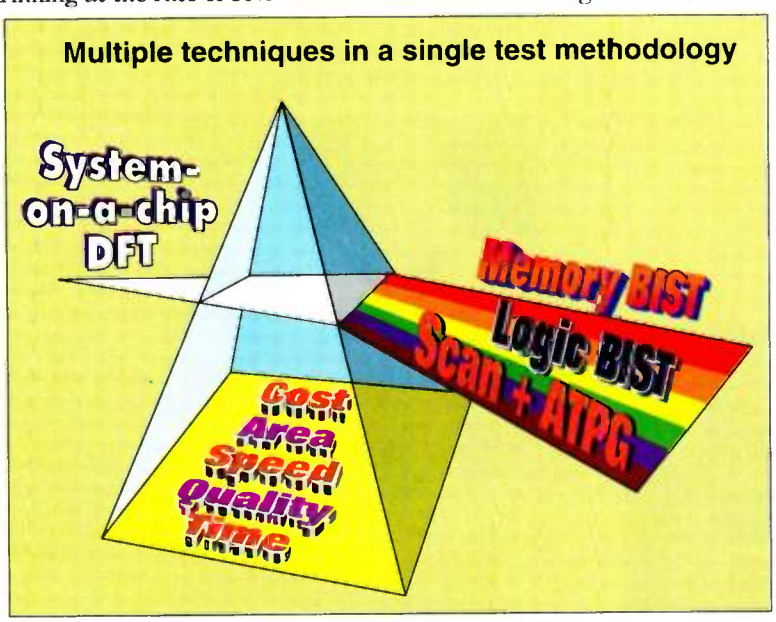
In this age of deep-submicron geometries and system-on-a-chip (SOC) ICs, design-for-test (DFT) faces serious challenges. To meet them head on, DFT companies are developing new test tools and employing older tools in new ways.

Deep-submicron geometries and systems-on-a-chip each have their own impact on DFT. Although geometries have been shrinking at the rate of 30% every three years (according to the 1997 SIA Roadmap), defect sizes are not shrinking in proportion. In other words, the contaminants are remaining fairly constant, spanning multiple gates and interconnects.

Additionally, gate delays have been drastically reduced as a result of the submicron geometries. Delays are now encountered in the interconnect. This arrangement affects the failure mechanisms of deep-submicron devices. Now, new fault models are needed to detect new failure types. Some of the fault models include path-delay testing, bridging faults, and interconnect faults. The result is that the DFT tools must have tighter integration with some of the design tools.

Not only are geometries shrinking, but die sizes are increasing. This results in a rise in overall gate count. Larger die sizes require a huge volume of data in order to store all the patterns required to adequately test the device. Typically, a single gate requires 1 kbyte of test data. Thus, a 10-million-gate IC requires 10 Gbytes of data. The requirements on automatic test equipment (ATE) continue to grow very rapidly to keep up with the gate count.

In addition, the test application time continues to increase. If you have a 100-MHz tester testing a one-million-gate design, it requires 10 seconds. Likewise, a 10-million gate design requires 100 seconds. The longer the test head is run, the more expensive the device will be.



Art Courtesy: Mentor Graphics, Inc.

Looking at systems-on-chips, many designs now use boundary-scan testing because it is a defined standard for interfacing internal tests. A system-on-a-chip routinely has legacy cores (*see "The Challenge of System-On-Chip Testability," p. 52*). When you're dealing with legacy cores, you really have no say in what the DFT strategy is. You're forced to adopt the test methodology your predecessor decided to put into it. You may have test-ready cores where an IP (Intellectual Property) provider has designed a core specifically with a test strategy in mind. For example, it may have scan, or logic BIST (Built-In Self-Test), or memory BIST, or a combination of these. There also may be user-defined logic. This is logic that the system integrator inserts as value-added product from a design house.

So, how do you develop a viable test strategy? According to Doug Wright, product manager at the Design-For- Test Group, Mentor Graphics Corp, "Increasing gate count requires multiple test tech-

niques because of the huge volume of data required to test the gates, as well as the huge test application time."

The approach may range from no DFT to functional patterns, to a more structured approach such as automated test-pattern generation (ATPG). It may have BIST, too, and it could have variants within each one of those.

This really poses a big problem when it comes to design reuse. "For design reuse to be effective, you really have to start attacking the problem of test reuse. If you don't, you are going to spend more time trying to figure out how to do the testing of these components than you are actually trying to design them. It really requires multiple test techniques in order to adequately come up with a system-on-a-chip DFT solution," says Wright.

Janusz Rajski, chief scientist at Mentor Graphics, uses the analogy of white light passing through a prism, "If you are looking at what it really requires to do system-on-a-chip DFT, when you pass this through the prism of cost, area, speed, quality, and time, you then can see the components." Rajski continues, "It really takes a combination of techniques such as memory BIST, logic BIST, scan, and ATPG to achieve an overall testing methodology for system-on-a-chip DFT."

According to Wright, technology trends still require ATPG to address deep-submicron issues. "ATPG is not a technology that is dying or going away. It is very valid technology; it is technology that is proven. It's been in the industry for years. ATPG makes it very easy to target complex fault models, such as interconnect faults, bridging faults, and delay faults. It's also a technology that can still be used for core-based design."

Wright continues, "We currently have customers of our ATPG tools, such as FastScan, interfacing to static timing tools, and feeding volumes of data (their critical paths) into the tool. Then they have the tool generate very specific tests to examine these long paths. So, this is technology that is emerging, but at the same time is in use today." About FastScan, he says, "It has built-in diagnostics that many manufacturing companies use to pinpoint failures within their process. Then, they can do process monitoring and yield improvements."

Wright insists that the industry is really requiring a core test strategy, "Because of all the complexity of delivering DFT solutions and trying to integrate them together, if you're going to do design reuse, test reuse is really imperative. If you are spending more time on back-end testing issues, you're not really gaining overall time-to-market advantages. And, in order to do that, we really need to have test interchange standards and architecture standards to maintain the efficiency of the design reuse."

Mentor Graphics' CTIntegrator, which was in beta testing at the time this article was written, attempts to solve the problem of effective test reuse by integrating multiple core test methodologies within a system-on-a-chip design (*Fig. 1*)."

Memory BIST is yet another BIST technology that is very common for system-on-a-chip DFT. Wright says, "We

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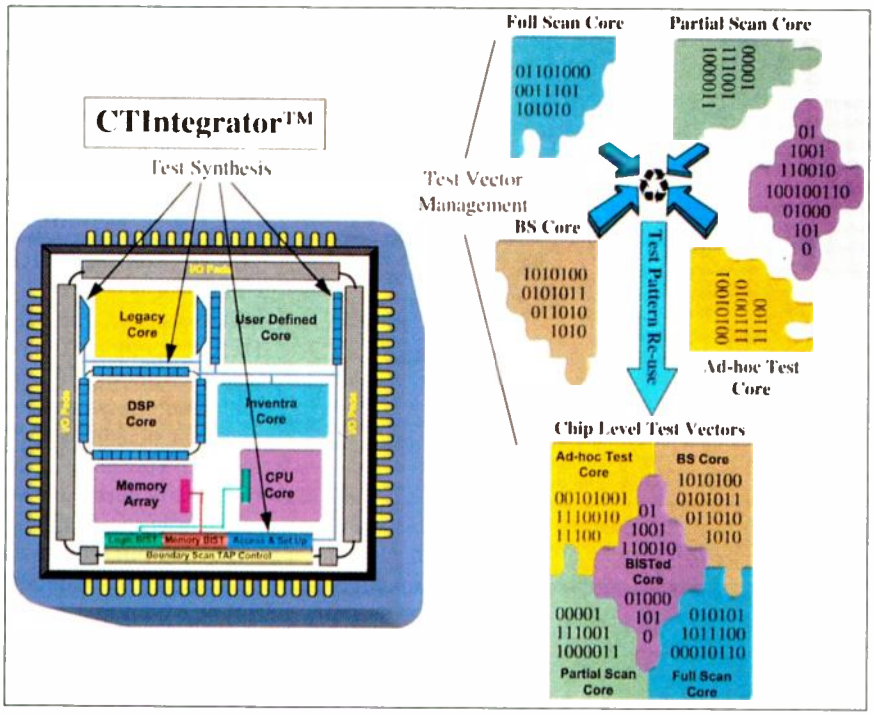

1. Mentor Graphics' CTIntegrator is a front-end design-for-test (DFT) software tool. It solves the problem of effective test reuse by integrating multiple core test methodologies within a SOC design. It takes complete advantage of a core's existing test patterns and fault coverage by establishing a system-wide test access and test bus architecture described in VHDL or Verilog.

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actually see many memories embedded in these large devices. That is one way to use up a lot of the silicon area. In fact, we have seen over a hundred different discrete memories embedded into a single design. So, it really requires doing BIST for memory testing."

Wright sees four key areas for memory BIST technology. One is the area of advanced algorithms and structures targeting different types of memory, for example, DRAM, flash, or SRAM. Each one of these has its own failure mechanism, so you need to look at advanced algorithms for detecting them.

Besides just looking at the types of memories to be tested with these algorithms, there is also an element of built-in self-repair. BIST can detect a failure and whether there is a manufacturing problem. For memories, it goes one step further. Not only is it possible to detect a problem, but it's also possible to swap in spare rows, columns, or small cache to recover this manufacturing defect, and still make the part usable. Therefore, BIST can be used as a technology at power-up to do a soft reconfiguration of the memory to bring in spare rows and columns, masking those manufacturing defects.

As memory sizes grow very large, yield will be dependent on these very dense memories. This hits a third area, design for manufacturability. Memories usually are densest part of a design, so they really could drive the yield. Therefore, it's very important to map defects into the process for process monitoring. The fourth area is where a company like Mentor Graphics plays a major role. Automating the tools and the flows gives the system integrator the ability to effectively use this type of technology.

As for logic BIST, Wright notes that for IP cores, it should be compatible with the overall design reuse. "We see this as being a one-time, up-front design effort that the IP provider would perform. Make it BIST-ready, if you will. Then the integrator can do simple integration with minimal knowledge and minimal processing of that IP core, while guaranteeing very-high, predictable, test core results."

Mentor Graphics is moving to provide tools and automation to support this type of methodology. "We see this as a trend that is really going to be in demand when the devices get very large and place tremendous burdens on the ATE equipment," Wright says.

Farhad Hayat, director of marketing for test automation for Synopsys Inc., sees a greater awareness of test

The Challenge Of System-On-Chip Testability: An EDA Perspective

It is a recognized fact that design reuse will play a crucial role in helping electronics manufacturers create higher-complexity designs on ever shorter design schedules. What is not as well known is that the productivity gains design reuse promises can only be realized if the issue of test reuse is resolved.

The test challenges surrounding system-on-a-chip (SOC) designs extend well beyond what test strategy to choose when creating a new core (predesign circuitry). Cores vary in design style and performance, and therefore, require different test strategies. A comprehensive test approach must also determine how to deal with "legacy cores" in use today that were designed without considering test reuse. Furthermore, today's system chips will become tomorrow's cores, magnifying the need to provide a solution that supports hierarchical test reuse.

Consequently, the primary challenge facing design engineers is integrating the diverse mix of cores into a comprehensive test strategy. The challenge for the EDA vendors is to provide a flexible solution and tool environment that places few restrictions on the core provider and integrator. These two challenges require a new level of design-automation capability that can accommodate a wide range of core test methodologies, while providing the means for efficient test-reuse.

Legacy-Core Test Issues

A close inspection of legacy cores shows many features that make test reuse difficult, if not, at times, impossible. Killer issues preventing practical test reuse include the lack of access to tristate and bidirectional control signals. Without these, little can be done to isolate a core from interference during testing.

Issues that make the test problem difficult, but not impossible, include isolation of a core from illegal input states, and the ability to drive constant values or tri-state, high-impedance output signals. The complexity involved in accomplishing these functions adds to the challenge in testing a core. Other concerns, although less problematic, serve to diminish the efficiency when testing legacy cores. Many cores were initially designed as a single-core device; that is, the core was the only block of logic in the design. As such, it was assumed that complete I/O access was available to the core, and test-data bandwidth was a secondary issue. Additionally, the test application time for the single core device was considered a single occurrence event. Little, if any, thought was given to the fact that this device may become a smaller piece of a larger design. Taking all of these issues into account, the result is a huge inventory of legacy cores that require a robust means of test integration and reuse.

Test-Ready-Core Considerations

Although the issues surrounding the test of legacy cores are significant in and of themselves, a comprehensive SOC test strategy must also consider the requirements of designing new, test-ready cores. The objectives of a test-ready core are to ease integration and provide efficient test reuse. This involves resolving access and isolation issues through design recommendations. Engineers need to design the core in such a way as to support a flexible SOC test architecture, while supplying all required test information necessary to automate test integration.

The preparation for a test-ready core occurs during the design phase, where a concerted effort is made to minimize test-data bandwidth, volume, and application time. New

(continued on page 56)

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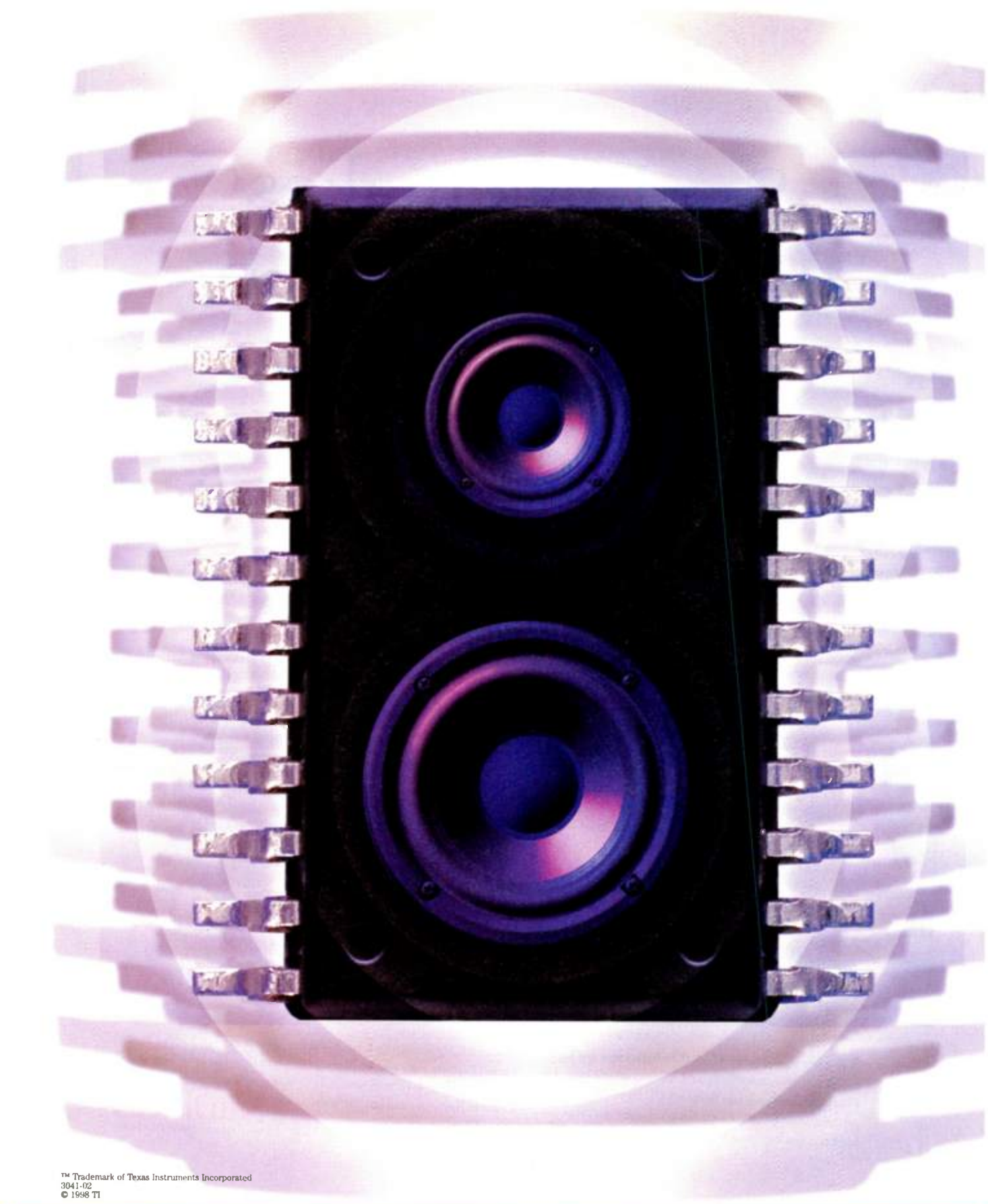

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on the part of designers, "Test is becoming more of an issue that the design teams are starting to worry about at the beginning of the project rather than at the end, when the design is complete, a net list is available, and the test department has to basically make the design testable." Hayat thinks this trend will continue, and that it's actually the right way to go. In other words, provide test tools to the designers so that they can transparently embed test in their design. Synopsys' solution for that is a product extension of Design Compiler called One Pass Test. It allows users to embed scanning into their designs during synthesis, while designing the RTL. It also provides early feedback on problems with testability of a design, and allows the RTL designers to get their design fully testable transparently.

Hayat concurs that deep-submicron design poses a number of challenges for test, "one, obviously, is that larger designs means a larger vector count. The other is new fault models." Hayat notes that the design may operate properly when you run the ATPG vectors and design at slow speed, but when you start running the design *at speed*, you run into new failure modes. These are primarily due to either excessive delays on the wires or excessive transition (slow-rising output) on the gate, which becomes more pronounced with deep-submicron designs.

Hayat continues, "we have products that will address this today. The product that is gaining a lot of popularity with both ASIC vendors and designers is called Path Test. Path Test works with static replication methodology, which is also becoming more popular with larger designs. One of the trends that we see is that as the gate count rises, designers rely more heavily on static replication to verify their timing, and less on functional vectors." He explains that as the design size increases, you may have thousands of critical paths to test. Functional vectors don't provide a guarantee that you are actually testing all of your critical paths.

Hayat points out another challenge of deep-submicron designs—increasing speed. "Scan-based methodology becomes more affordable from a timing point of view. Whereas in the past, because of the speed of the design, and what the process could do, you may not have been able to reuse full scan in your design. You could not afford the additional timing that you had to account for when using a scan cell," says Hayat. He continues, "as you move to faster

(continued from page 52)

enhancements to traditional DFT tools automate the generation of compact test sets, and reduce the I/O contact necessary to test a core. Core-centric built-in-self-test (BIST) and automatic-test-pattern-generation (ATPG) tools can prepare cores to meet the needs of test reuse. For example, steps can be taken in the preparation of a test-ready core to allow the final test methodology (scan or BIST) to be determined later during the core test integration phase. The process of creating a test-ready core will yield a corresponding core test description. This standard test description provides the portability necessary to efficiently integrate cores from various sources.

Considering test integration issues early in the design of a core ensures a high- quality test through test reuse, helping to fully realize the design efficiency and productivity gains offered by design reuse.

TAS And Core Testability

The remaining challenge is how to support the test of a heterogeneous mix of cores in a SOC. The test-access structure (TAS), originally developed by Mentor Graphics and now included in its proposal to the IEEE P1500 Embedded Core Test Working Group, creates a comprehensive test approach. It provides the data and control infrastructure necessary to test any and all cores, including legacy and test-ready cores.

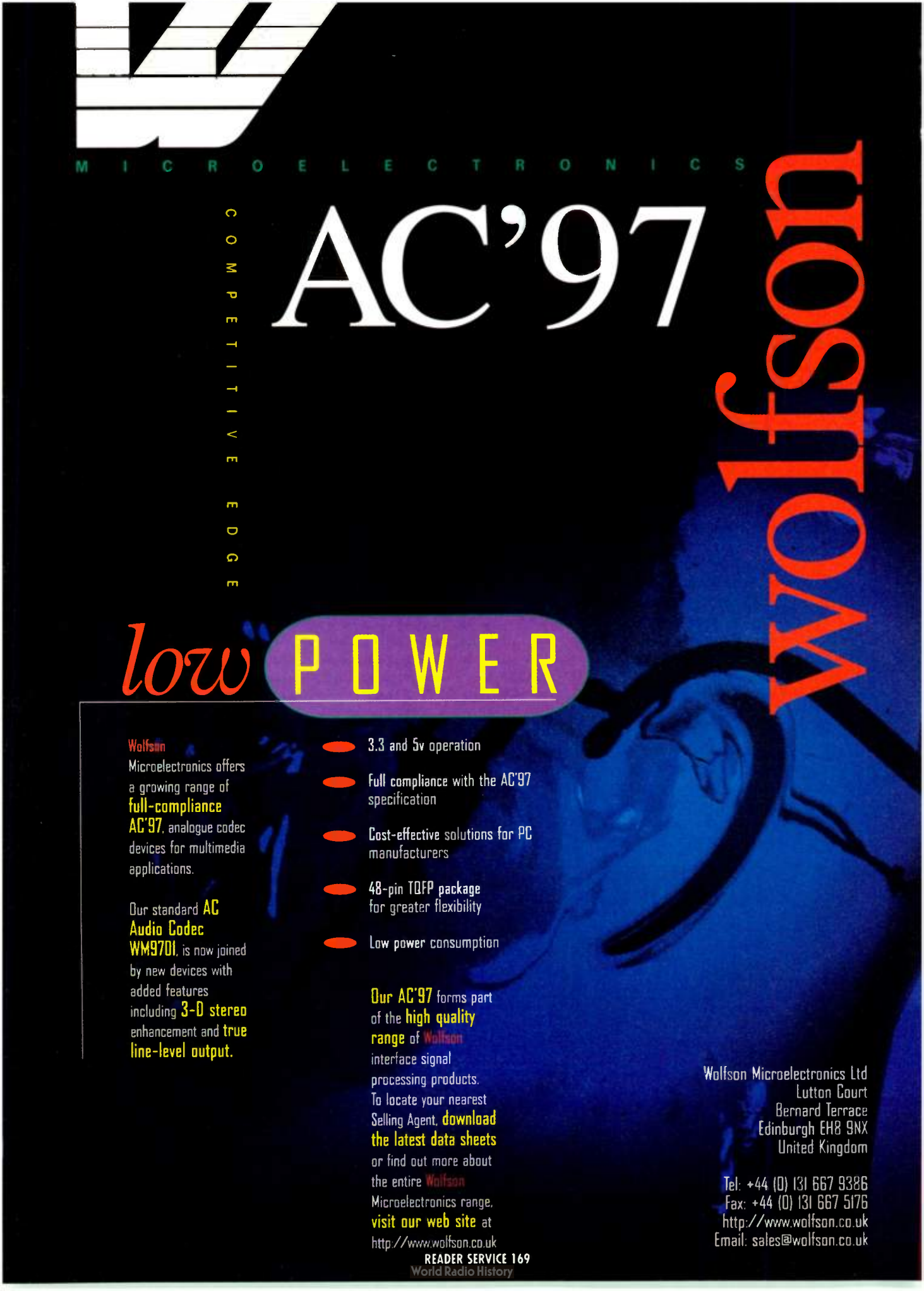
The objective of the TAS is to provide a flexible architecture that can be scaled during core test integration to meet the needs of the SOC design. Trade-off exploration during core test integration is necessary to optimize test-access bandwidth, area, and application time. These constraints vary depending on the level of test readiness of the cores, the test methodology of the cores, the number of test-accessible I/Os required for embedded cores, and the number of SOC I/O available for test.

Design automation is well suited to help manage all of these issues. Test synthesis of the TAS based on user constraints and trade-off exploration yields an efficient architecture tuned to a specific SOC design. The remaining step necessary to complete the SOC test strategy—test vector translation—again relies heavily on design automation. This involves manipulation of each core test vector set to translate and map the stimulus and response to the SOC I/O. During TAS synthesis, the test-access mapping for each core is saved. The test vector translation step then uses this mapping information to formulate the SOC test vector set for each core. As a result, the final test vector set is an arrangement of setup and isolation procedures interleaved with core test vectors that have been mapped to the test-access structure.

Realizing the full potential of design reuse requires an effective test reuse strategy that includes the ability to test legacy cores and test-ready cores. For the core provider, design guidelines and core-centric, automated DFT tools will ensure that new cores fully support test reuse. For the core integrator, the TAS approach, combined with a trade-off analysis, will result in the best test-access structure based on user and SOC constraints. In both cases, design automation provides the critical test capabilities for creating access to the core test architecture while translating and managing test vectors for the SOC.

For more information regarding test reuse and test-access architecture, see Mentor Graphics' DFT web page (*www.mentorg.com/dft/*) for the two presentations recently made (VTS '98, April 1998) at the IEEE P1500 Embedded Core Test Working Group meeting. The presentations are titled "Core Test Techniques, an EDA Perspective," and "Test Access Structure."

Contributed by Tom Eberle, core test product manager, Mentor Graphics Corp., Design-For-Test Division, Wilsonville, Ore.



processors, you can start using full-scan methodology, and still meet your timing goals. Also, because the available gate count is there, the penalty or the overhead that you may have had in the past with scan-based designs is not there anymore. So customers are moving to more full-scan design methodology. It offers full predictability, observability, and it's really becoming the methodology of choice when you are targeting high-fault coverage and a predictable flow."

Sometimes, designers have a more high-performance design where, for some portion of the design, they may not want to use scan testing. Basically, they want to get the maximum performance out of the design. Hayat explains, "that becomes more of what we call a partial-scan or near-full-scan design. And for those types of methodologies, we have the TestGen product, which allows you to use a full-scan methodology, and back off from full-scan testing for those portions of the design where you are not using scan-based methodologies to get the fault coverage that you need. Our recommended tool flow is to use DC Expert Plus for scan insertion and TestGen XP for ATPG (*Fig. 2*). The DFT portion is performed during the synthesis, which eliminates iterations."

Hayat's observation on logic BIST is that it must be made a transparent part of the design flow, integrated with the design flow. He notes that existing methodologies have more of a back-end type of approach, where after the designer has finished the design, meets the timing, meets the area goals, and everything is working, then someone has to come in and actually build the logic BIST for it. He says, "The methodologies that are out there in the marketplace are very iterative types of methodologies and very hard to use. So, we think what the market requires is a tool that is integrated with existing flows, and also provides some level of predictability."

He continues, "As time-to-market windows become shorter, you want a predictable methodology where you can say, 'I want to spend one week doing this, and I know that with this methodology I can get there.' Iteration loops that could set you off in a direction that may not have a solution typically are not desirable. We think full-scan DFT is becoming popular because it is a predictable methodology. You know that if you follow these steps you will get a predictable fault coverage, and get the quality that you want. The same thing needs to happen with logic BIST, which is to follow these steps and get the fault coverage you want. Obviously, we support full-scan methodology, and if a designer is using logic BIST, he or she can take advantage of Design Compiler, and so forth, and can choose to add logic BIST to that."

A New Type Of Memory BIST

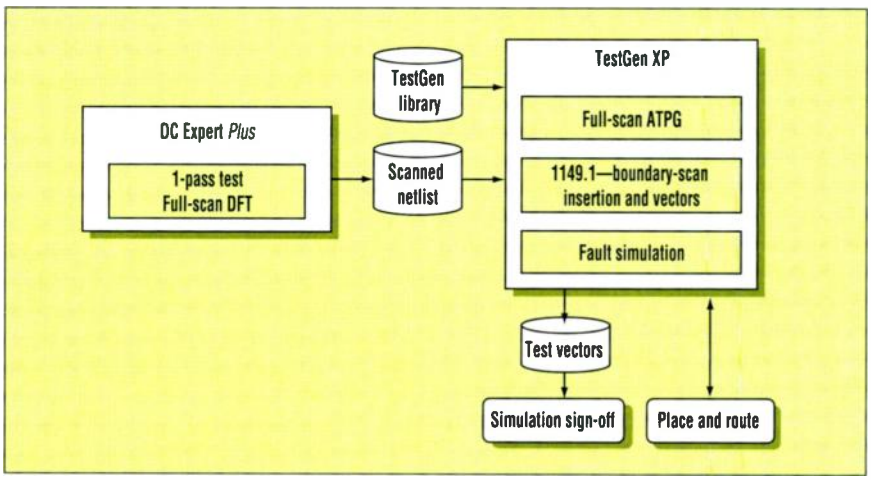
Mark Olen, vice president of worldwide marketing and sales at TSSI, has a special interest in BIST because TSSI has just announced the acquisition of BIST technology from HPL (Heuristics Physics Lab). HPL's product, called MemBIST, is viewed by Olen as a next-generation memory-BIST tool.

According to Olen, "One of the differences between MemBIST and other tools like it is that while the MemBIST tool does generate a variety of preprogrammed algorithms, the algorithm generator in the tool is fully programmable." Olen's observation is that testing static RAM is not a big problem. It's fairly straightforward to use some of the standard 13N or 17N March tests for testing static RAM. But when you start getting into DRAM or into flash or into FIFO, every semiconductor process is different.

For the actual layout of the arrays, you need a different algorithm to elicit the faults you need to test for. "In a sense, what we've actually done is implemented a little, mini-ATE system right on the tester. But it's a programmable system, not a fixed algorithm," says Olen. "There are actually 11 patents embedded inside this tool. One is called MRC. It's a reduced routing technique that allows for parallel access of memories. In a parallel mode, you can suffer large routing overhead, but these guys have done some interesting invention in this area to reduce the routing to the level that serial access would provide, yet still give you the benefit of parallel access."

MemBIST supports static RAM and DRAM, and will be the first to support flash memories, CAMs, ROMs, FIFOs, and simultaneous testing of multiport RAMs, according to Olen. "Multiport RAMs are becoming more common on systems-on-a-chip, but until now you had to test each of the ports separately. You couldn't actually test the ports to verify they could run simultaneously, the way they run in system operation," observes Olen.

Olen also has some views on logic BIST, "We took a look at logic BIST, and it offers some tremendous advantages and opportunities. But, clearly, the technology and methodology of logic BIST is still unacceptable to designers." He adds, "The thing to remember is that most logic-BIST technologies are actually built on top of full scanning. It is not an alternative to scanning. Therefore, whatever you pay in terms of area or performance degradation, you'll pay at least that much if not more in logic BIST."



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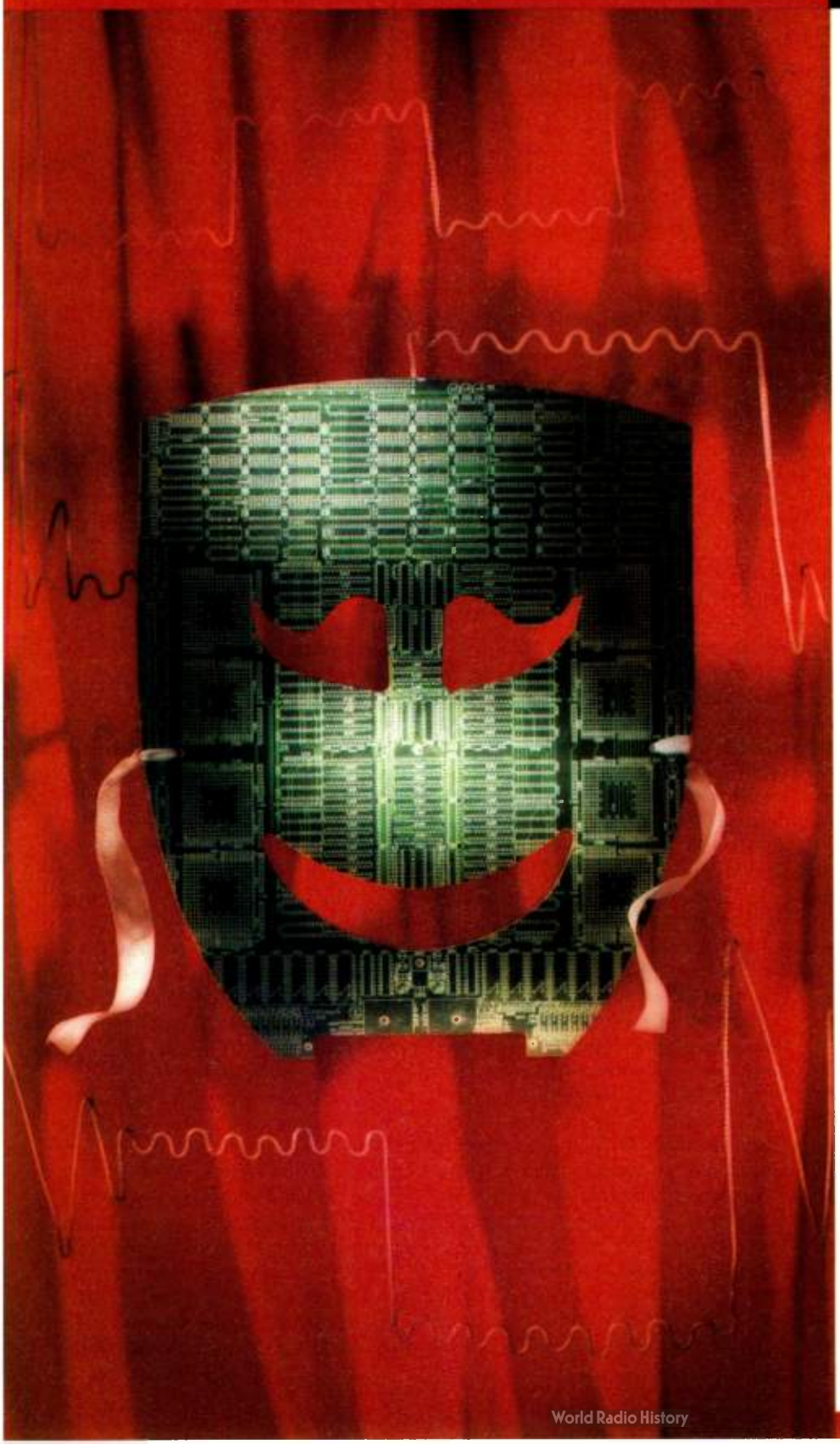

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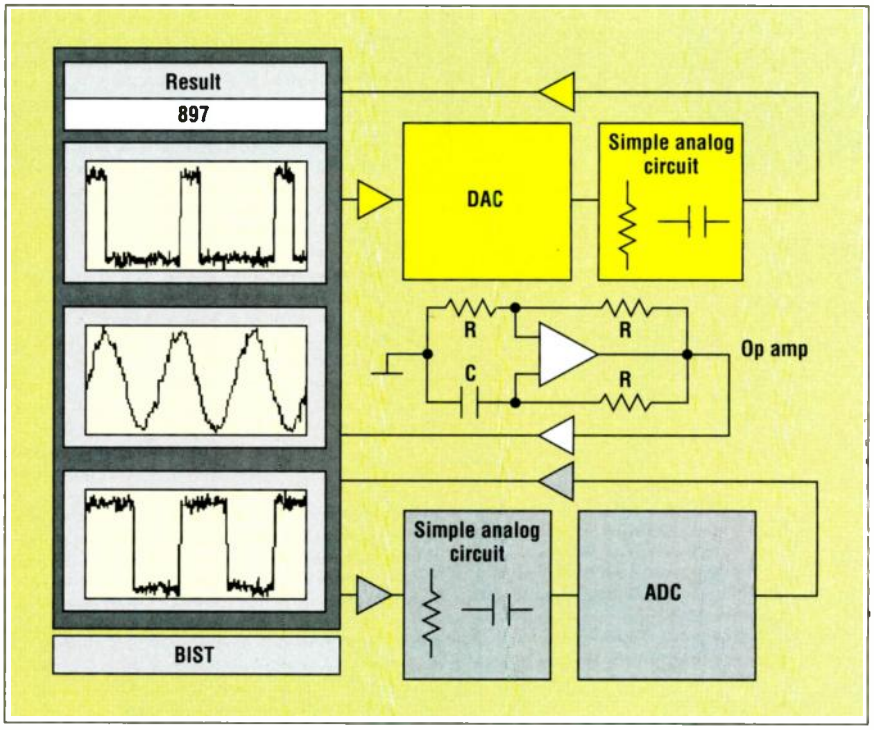
When would logic BIST work? Olen answers, "If I'm a core provider, and I want to provide a ready-made test solution to the customers of my core, but don't want to divulge my net list, then I typically want to encrypt it. To date, there are no test tools that can generate high-quality tests on a black box. But if I said, 'Here's the logic-BIST spec, I've already implemented logic BIST. All you have to do is hit this clock pulse here on this signal, and it will test itself.' Now there's a great application for logic BIST."

Olen has other problems with logic BIST. "It is area intensive, in some cases as much as 30% to 35% area overhead. This is very high. Also, there is still a design methodology constraint of fully understanding the X propagation within your circuit. In other words, if one part of a system is operating and another part is turned off, designers don't really care what's happening in the other parts. They are just making sure the I/O function works while the CPU is resting or vice-versa, whatever it is," says Olen.

"The problem is that when they do that, and in many cases they will gate clocks to save power in the areas of the circuitry that are not being used, that just wreaks havoc with logic BIST. Logic BIST doesn't know anything about mission mode or about the actual system-level operation. And, as soon as you have Xs or unknown states propagating through a circuit, the signature register at the end goes to an unknown state, and the whole thing gets thrown out of kilter.

"What we've seen is that in some cases, designers will manage the area impact, but when you tell them they have to design their circuit very carefully so that they never have unknown states propagating through their designs, then that can cause a lot of reluctance and resistance," he says.,

Olen believes one of the clear trends of systems-on-a-chip is that memory is taking up increasingly more of the die area. "Memory is very regular in structure, and lends itself to a BIST solution that, relative to the overall size of the memory, can be very small in terms of area overhead. And, we suppliers are getting better at designing BIST circuitry smarter so that we can even share one BIST controller across multiple arrays, and not lose anything in diagnostics, and, in fact, even gain in faster test time," notes Olen.



3. Opmaxx's new BISTMaxx tool offers oscillation BIST for analog, mixed-signal, and digital circuits. The figure shows how the technique displays different results depending on the type of circuit tested, for example, digital-to-analog converter, op amp, or analog-to-digital converter.

An Expanding Role For BIST

Michael Kondrat, vice president of marketing at Opmaxx Inc., says movement to deep-submicron technology, which is enabling systems-on-a-chip to really take off, creates some issues in terms of the design environment. Suddenly, digital designers have to understand what the process parameters are doing to their signals. The signals are going so fast that the process parameters are starting to impact the signal performance. So, the signals are becoming more analog-like in terms of their problems.

Kondrat sees the role for BIST continuing to expand. "As you are driving down to the very-deep-submicron technology, 0.18 µm and below, you see that the test requirements are starting to change as well. You're moving from a functional-type test to a structured test environment. Digital delay testing is really becoming an important issue as is interconnectivity testing. It is very important for designers to minimize interconnectivity in their designs. If you look farther into the future, speeds are increasing so much that designers are starting to look at embedding test instruments, embedding test probes, analog probes, you name it, actually on the chip itself, to measure the performance of the design," says Kondrat

Opmaxx has developed a new test technique called oscillation BIST or OBIST. According to Bozena Kaminska, vice president and chief technology officer at the company, BIST is not as popular as it could be because it has been very difficult to implement. Kaminska begins, "It should be easy and as uniform as possible. With this in mind, we have introduced oscillation technology. This is an easy and elegant way to implement BIST because we are transforming a building block into an oscillator. We are adding a feedback loop with some components, for example resistances and capacitances."

By obtaining oscillation frequencies, this technology can cover functional testing or structural faults. According to the company, significant advantages can be realized because frequency is very easy to translate into numbers. "So, basically, we have a digital output, which is very easy to combine with digital standards," says Kaminska

Oscillation BIST does not have noise problems, which is a major issue for

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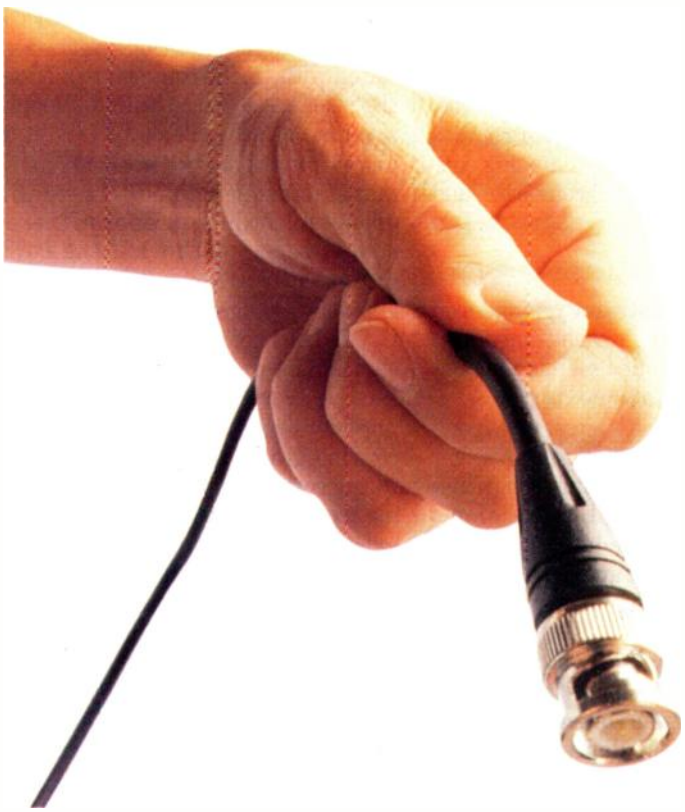

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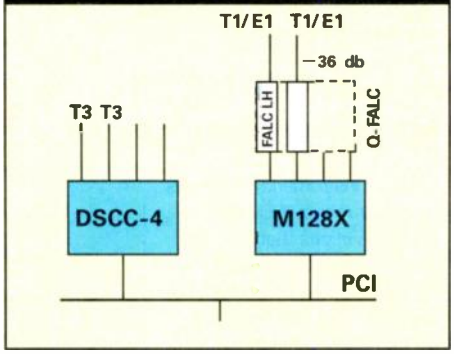

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analog and mixed-signal circuits. This tool is also appropriate for high frequencies, again, because of the digital output. By transforming blocks into oscillators, nothing inside the design changes. Kaminska explains, "We are adding just one or two very small switches to isolate the block. The impact on the circuit's performance is minimal. The nice part of this is that designers often know about oscillation techniques. On wafers, for example, designers are already using test structures based on oscillators."

Opmaxx's new product, BISTMaxx, is based on OBIST technology. BISTMaxx provides a uniform approach for testing a variety of analog, mixed-signal, and digital circuits ranging from converters, oscillators, phase-locked loops, and amplifiers to high-speed digital timing paths and interconnections. Figure 3 shows how typical results might look for a digital-to-analog converter, analog-to-digital converter, and and op amp.

Embedded ATE

One other test strategy, pioneered by LogicVision Inc., is called embedded ATE. This technique embeds the nonscalable portion of an external ATE into the chip itself. It's a test methodology for very-deep-submicron ICs that is compatible with existing design and test methodologies. LogicVision's icBIST3.0 is an embedded ATE solution for at-speed test and diagnostics of digital and mixed-signal system-on-a-chip devices.

Dr. Vinod K. Agarwal, LogicVision president and CEO, notes that, "Using icBIST3.0, a system-on-a-chip can be tested using a fully depreciated logic tester, saving millions in costs related to the purchase of a new ATE."

What About Standards?

Two organizations are looking into embedded core test standards. One is an IEEE organization, P1500. This group focuses on testing issues and the interchange of test descriptions as well as a language that describes this. It is also looking into the architecture and control to be included with these designs. So, when a system chip integrator tries to bring cores together, the industry has agreed upon the type of test data that needs to be exchanged. According to Tom Eberle, core test product manager at Mentor Graphics' Design-For-Test-Division, "It's clear that they're not trying to standardize on the test and methodology inside one of these cores, just the test information that describes them."

There are two task forces: architecture and language. The architecture group looks at those issues associated with the architecture of combining cores together; for example, should there be a common control method to describe that. The other is a language group within the P1500 working group that is interested in coming up with a language structure to describe the test data interchange.

Another organization is the VSI alliance or VSIA. The 180-company consortium examines various issues associated with IP, the commerce of IP, and the issues associated with developing system-on-a-chip designs. One of the development working groups is the manufacturing-related-test working group. According to Eberle, there is some overlap with what the P1500 group and VSIA are doing, but they are working together on that.

"VSIA is not just thinking of the design and interchange issues, it is interested in everything from what the core provider needs to do and provide to the core integrator, as well as the manufacturing company that would be fabricating the device. They are trying to take existing standards, for example test-vector interface standards like STIL (Standard Test Interface Language), and recombine these into more of a metastandards type of organization. So these two organizations get together, but again [the technology] is emerging, and it's just not clear how this is going to end up," explains Eberle.

Summary

The advent of deep-submicron technology has given rise to the system-on-a-chip, where multiple digital, analog and mixed-signal cores come together to form a complete product. Companies have come up with ingenious ways to test these chips including ATPG, boundary scan, memory BIST, logic BIST, oscillation BIST, and embedded ATE. These test techniques, as well as test standards emerging from the IEEE P1500 and VSIA groups, should give designers the tools they need to cope with this increasing complexity.

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The DI-730 communicates with a PCs printer port in EPP, bi-directional, or standard mode. In addition, it can be connected to a PC or notebook via an optional USB port, which provides hot-swap capability. For remote data acquisition or Internet-based monitoring/control, an optional Ethernet 10Base-T communication port is available. With an Ethernet interface in place, multiple 730 devices can be connected to the same network node at the same time from any desired location.

According to the company, the DI-730 can be used in virtually any type of industrial environment, because its wide dynamic range and high isolation protects both the board and PC from high common-mode voltages without disturbing sensitive control circuits. In effect, the DI-730 replaces multibox systems consisting of isolation amps, high- and low-voltage amps, and a separate data-acquisition subsystem.

The DI-730 is a blend of old and new technology. Old technology is incorporated in the form of gas-discharge tubes, which are applied directly across the input of each channel to protect them from extreme overvoltage situations. Input signals are connected simultaneously to 100:1 and 1:1 circuits. A multiplexer and programmable-gain amplifier work in tandem to provide both coarse and fine range selection.

Voltages passing through the 100:1 attenuator are reduced to safe levels and therefore pose no danger. On the other hand, signals passing through the 1:1 attenuator would, of course, destroy the remainder of the circuit at high voltage levels. Protection is provided via two back-to-back depletion-mode MOSFETs. These devices pinch off any voltages exceeding ±15 Vdc, which is well within the tolerance of the instrument's circuitry.

Features of the DI-730 are a DSP-based design; built-in pre- and post-triggering, programmable sample rates; digital calibration via software; and operation from any power supply source between 9 and 36 V. The unit also supports average, maximum, minimum, and last point acquisition methods. This feature enables the DI-730 to provide noise reduction or min/max detection in real time using the company's intelligent oversampling technique. It also enables acquisition of peak voltage or current, or both, at extremely low sample rates.

The system comes with WinDaq/

(continued on page 67)

(continued from page 66)

Lite acquisition and playback software and supports most other software environments including HP Vee, Excel, LabVIEW, and TestPoint. A Programmer's Software Development Kit supplied with the system provides language support for Windows-based programming languages, including Visual Basic, C, and C++. Price of the DI-730-P runs $2995, and is available from stock. Price of the USB port is $220; while the Ethernet port goes for $395.

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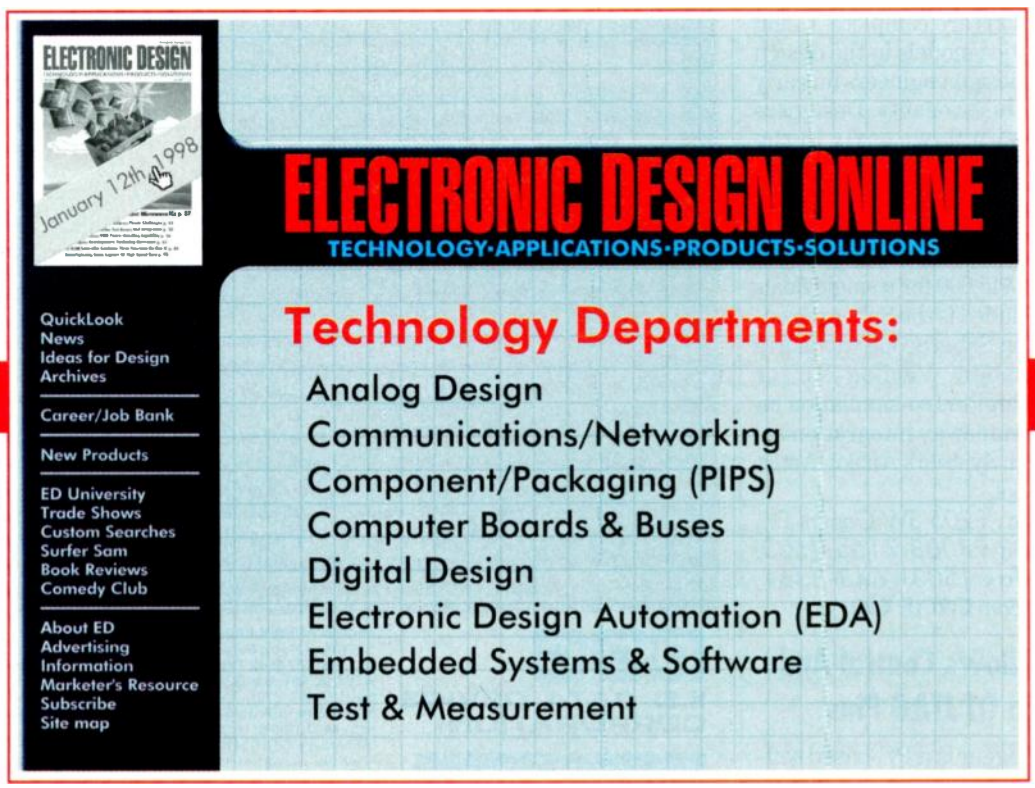

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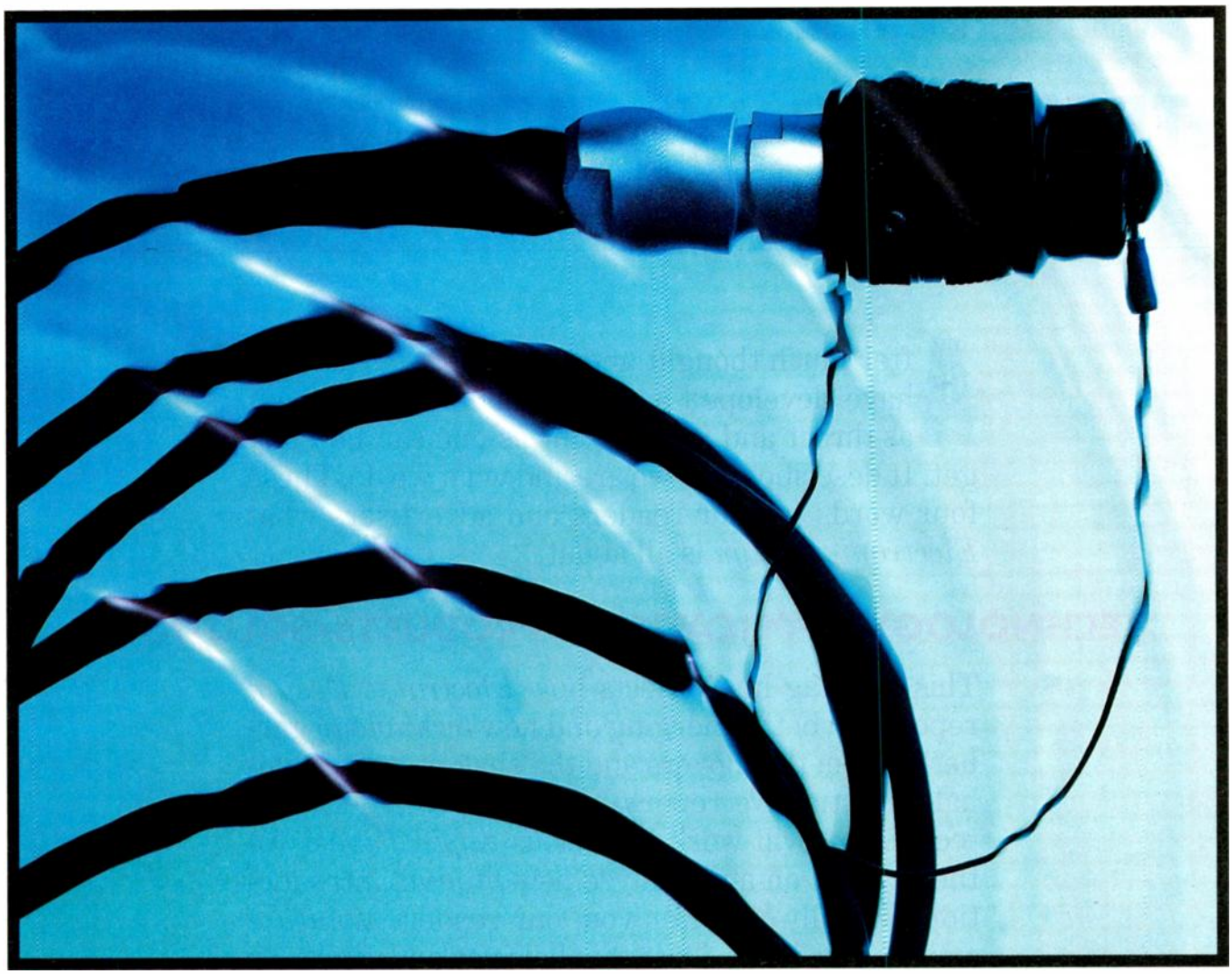

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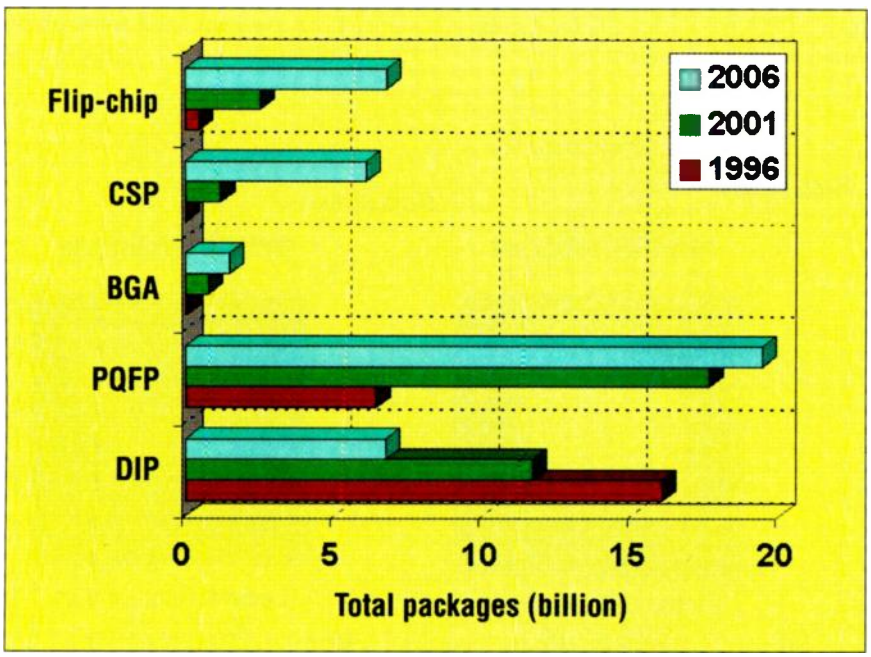
To date, surface-mount packages, whether J-lead or gull wing, have been key enablers in the drive to reduce the overall size of electronic systems and devices. Despite the maturity of this technology however, increasing pressure to enhance reliability, increase functionality, and reduce size while lowering costs has kept researchers and designers permanently at the drawing board.

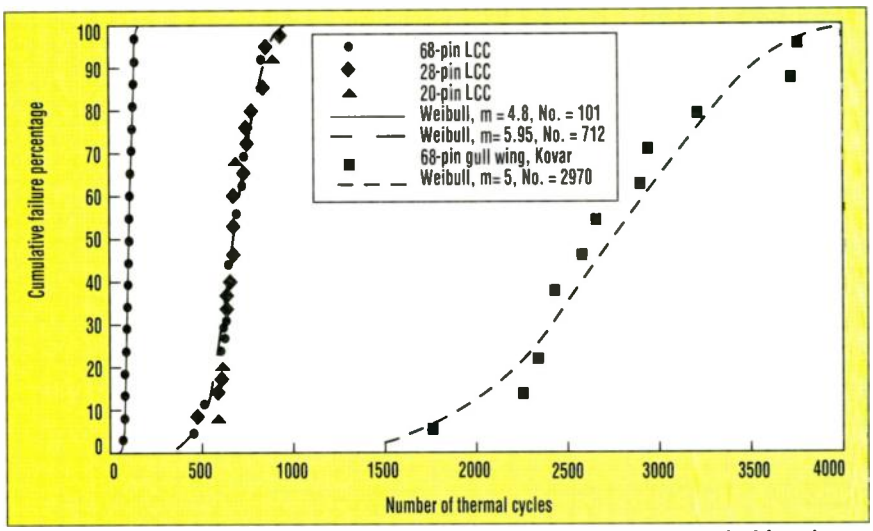
The current answers to these challenges are surface-mount (SMT), package options that can be loosely divided into two groups: ball-grid arrays (BGAs) and chip-scale packages (CSPs). While both of these technologies have been around for a number of years, their relatively high cost has relegated them to only the most space-constrained applications. Now, the pressure many designers face to reduce system dimensions has brought about a gradual migration toward these newer packages.



1. Projections regarding the use of the many available package options are significantly different. What is clear, however, is that user demands for higher speed and more functionality will help advanced packages, such as BGAs and CSPs, to steadily encroach upon the well-established DIP's market share. In addition, the projection for BGAs indicates that perhaps these packages were only an interim solution; the stepping stone for the industry's wider acceptance of flip-chips and CSPs.

Unfortunately, other major obstacles to the adoption of these technologies still exist. The very nature of these packages means that reliability is questionable and that conventional testing and rework methods no longer apply. Also, the competitive nature of the high-end IC business is such that many package/IC houses are loathe to divulge the exact failure rates of their package design. As a result, mistakes will be repeated, thereby slowing progress. In addition, the plethora of package options causes some confusion for designers who must choose from among them. Their decision is further hampered by the limited time they have to perform extended reliability and performance testing, thanks to ever-present time-to-market pressure.

As a result of all this, the Jet Propulsion Laboratory (JPL), Pasadena, Calif., undertook the task of performing extended, independent, performance and reliability testing of SMT packages, using the two categories outlined above (regular SMT BGAs and CSPs). Working for NASA, JPL is one of the few facilities that can independently test the devices over a long period of time without time-to-market pressures. While



2. The cycles-to-failure for 68-, 28-, and 20-pin LCC package assemblies are ranked from low to high, and failure-distribution percentiles are approximated for each using a median plotting position [$F_i = (i-0.3)/(n+0.4)$]. As expected, there was a large spread in cycles-to-failure due to the common variances associated with materials and manufacturing conditions, including solder-joint volume, quality of joint, and location.

still a work-in-progress, test results are available, along with information on lessons learned from the design, manufacturing, inspection, and reliability of these assemblies.

A review of the board-level reliability of CSP assembly and the projected values for specific environmental conditions were extracted from the data. These findings offer valuable information on package robustness, and provide a better understanding of the challenges associated with the implementation of SMT technology, particularly with the new, advanced, miniature CSPs.

Miniaturization Trends

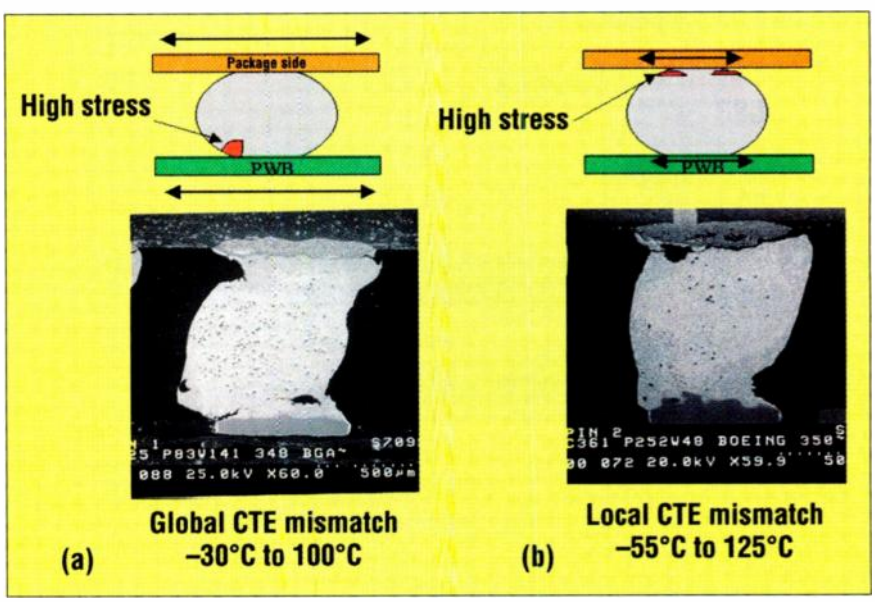
SMT electronic packages are mounted directly onto the board surface, as opposed to the insertion of leads into plated through-holes (PTHs). While SMT come in several different package styles, they can generally be divided into two categories: those with terminations of leads on the periphery of the component on two or four sides, called peripheral-array packages (PAPs), and those with terminations (either pads or solder bumps) over much of the bottom of the component, called area-array packages (AAPs). PAPs have less potential for significant size reduction with increased I/O counts, compared to AAPs. The BGAs from the latter category are now the mainstay alternative to PAPs. For example, the CSP version of the two-sided PAP is the lead-on-chip (LOC) package, and the versions for AAPs are micro- (or mini-) BGA packages, which generally use eutectic solder balls.

Another level of miniaturization is accomplished by directly attaching the bare die to the printed wiring board (PWB). The direct flip-chip on board (FCOB) is the ultimate miniaturization level, achieving a die-to-PWB footprint ratio of nearly 70%. In FCOBs, solder bumps are permanently attached to the face of bare die, and the flip side is mounted on the PWB. In chip-on-board packages, with about 50% use-of-area efficiency, the pads of the wire-bonded die are used for second-level wire bonding onto the PWB.

Projections regarding the use of these packages are significantly different, with the numbers dependent on the market source. One projection from the British Packaging Association (BPA), U.K., is shown in Figure 1.

Several trends are apparent. The dual-in-line package (DIP) shows the most reduction in use, decreasing from 16 billion in 1996 to about five billion over 10 years (roughly one billion fewer per year). In contrast, the use of surface-mountable packages including quad flat packages (QFPs) is expected to increase in the next decade. The increase for plastic QFPs is forecast to be from seven to 18 billion within the first five years, and will almost plateau with an increase of only two billion for another five years. Within 10 years, the flip-chip-on-board package (FCOB) is forecast to increase from five to 13 billion.

The rate of increase in the use of CSP and flip-chip packages is the same. Both are projected to reach up to six billion production units by the



3. The cross-section of failure sites for the CBGA 625 after 350 cycles shows both board (a) and package (b) interface cracking. Failure-mechanism differences could be explained by global-or local-stress conditions. Modeling indicates that the high-stress regions shifted from the board to the package when conditions changed from global to local.

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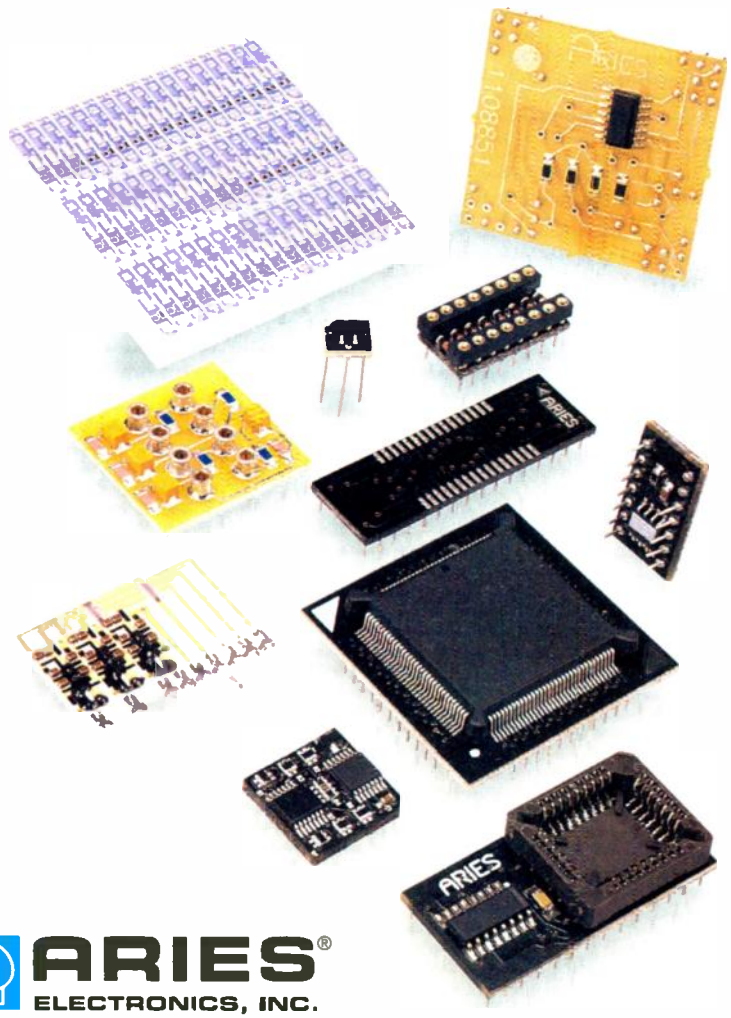

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year 2006. In contrast, the expected increase for BGAs for the next 10 years is minimal, reaching a total production demand of only 1.5 billion. The projection for BGAs suggests that these packages were only an interim solution, that the devices are a stepping stone for the industry's wider acceptance of flip-chip and chip-scale packages that better meet the demands for denser and lighter miniaturized applications.

System Approach

To meet the mission requirements or to bring a product into market successfully, many factors must be considered. Concurrent engineering approaches, which consider multifaceted areas of technology and the interaction among the various engineering disciplines, are key to meeting these objectives. Areas that must be included are:

- Design for manufacturability
- Design for testabililty
- Design for quality and reliability

A similar approach could be used when a subsystem of electronic assemblies is being investigated. The internal JPL teaming arrangement for SMT technology evaluation, as well as the industry-wide consortium of BGA and MicrotypeBGA follow the same idea of a concurrent-engineering approach. This approach has been extended here to include various aspects of electronic attachment, including manufacturing and design, for reliability from conventional SMT packages to emerging CSPs.

Attachment Approaches

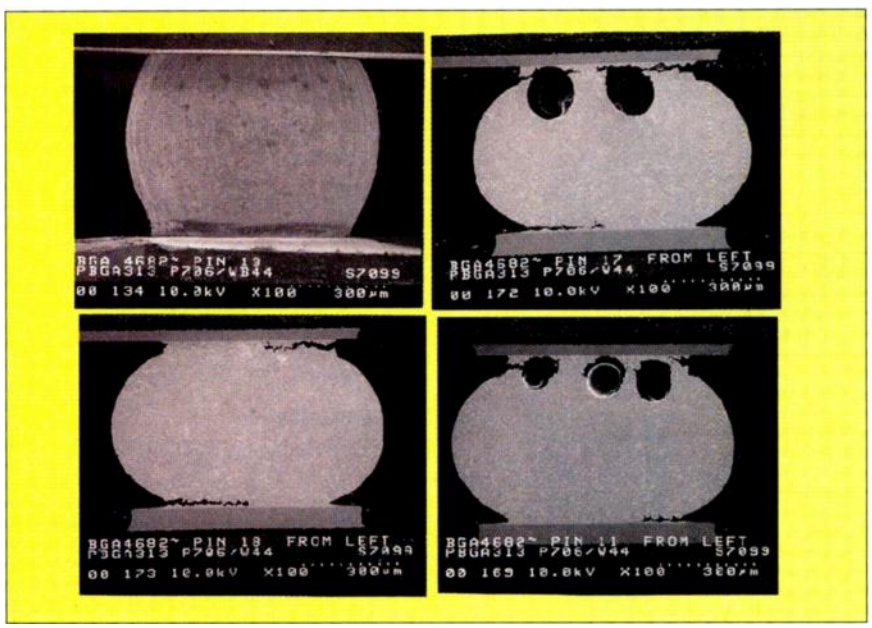
To connect I/O signals from the package to a subsystem of electronic hardware, the package is attached to a printed wiring board (PWB). The attachment can be accomplished by various techniques, including insertion, plated-through hole, surface mounting, and adhesive bonding. Here, we will focus on soldering.

Generally, packages are attached by soldering the leads (castellation or endcaps for leadless packages, balls for grid arrays) to the PWB. In the SMT application, solder has both electrical and mechanical functions. As a result, damage to the solder could easily affect the functional integrity of the system. Therefore, an analysis of the defects that cause changes, either in mechanical or electrical system characteristics, is critical.

The most common damage found in solder joints is induced by thermocycling—differences in thermal expansion of package and PWB materials. This is especially true for eutectic solder (63 Sn/37 Pb) which creeps at room temperature. Creepage generally occurs at temperatures above one-half the absolute melting temperature (T/Tm > 0.5). This value is 0.65 at room temperature for eutectic solder. Creepage and stress relaxation are the main causes of cycling damage. The primary source of damage in package attachment is caused when the system temperature changes. Damage to solder joints is most often caused by stress induced by the global coefficient of thermal expansion (CTE) differences between the package and board, and local CTE differences between solder attachments to components and the PWB. The package and board can also have temperature gradients through the thickness and at surface areas.

Reducing CTE differences between the component and the PWB reduces cycling damages, but the ideal condition depends on the thermal conditions of the components, the PWB, and the solder. An ideal condition could be the selection of PWB materials which have a slightly higher CTE than the components. This is based on the assumption that the global CTE is generally dominant, and that the component is hotter than the PWB.

There are other approaches that can be taken to help reduce damage to solder joints. Underfill application is a common technique which has been widely used for either the direct attachment of a chip to a board, or when package leads are not robust. Other, less-conventional approaches are aimed at absorbing CTE mismatches between the die and board, either internally or externally. These methods use strain-absorbing mechanisms, which reduce stresses on the solder-joint interconnect. These approaches have a tendency to introduce their own unique damage, because the weakest link is now transferred from the solder joint to other areas of the attachment system.



4. Among the plastic packages tested, the PBGA 313, with depopulated full-array solder balls, was the first to fail under both B and A thermal-cycling conditions. After the completion of 4682 cycles, the balls under the die see most of the damage due to local CTE mismatches. Voids appear to have concentrated at the package interface under the die.

Conventional SMT

The program at JPL focused on the use of SMT for high-reliability, ultra - low-volume spacecraft electronics, as used in the NASA community. Various aspects of the technology were investigated and documented, including

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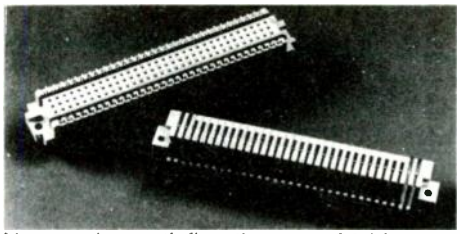

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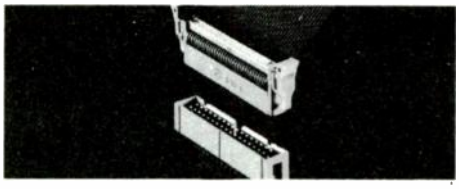
Removable temporary inserts allow any flat die to press the connectors. The straight header is shrouded by four plastic walls and available in versions from 6 to 64 contacts. The mating connectors are flat ribbon terminated socket connectors from HARTING's SEK range. These can be latched to the headers by using the locking levers installed onto the strain relief. The levers secure the socket connector to the end walls of the



header. Placing the locking levers on the socket instead of the PCB header saves valuable board real estate.

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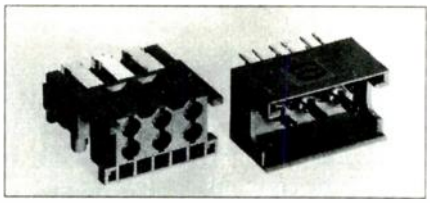

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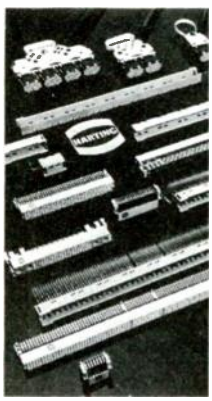

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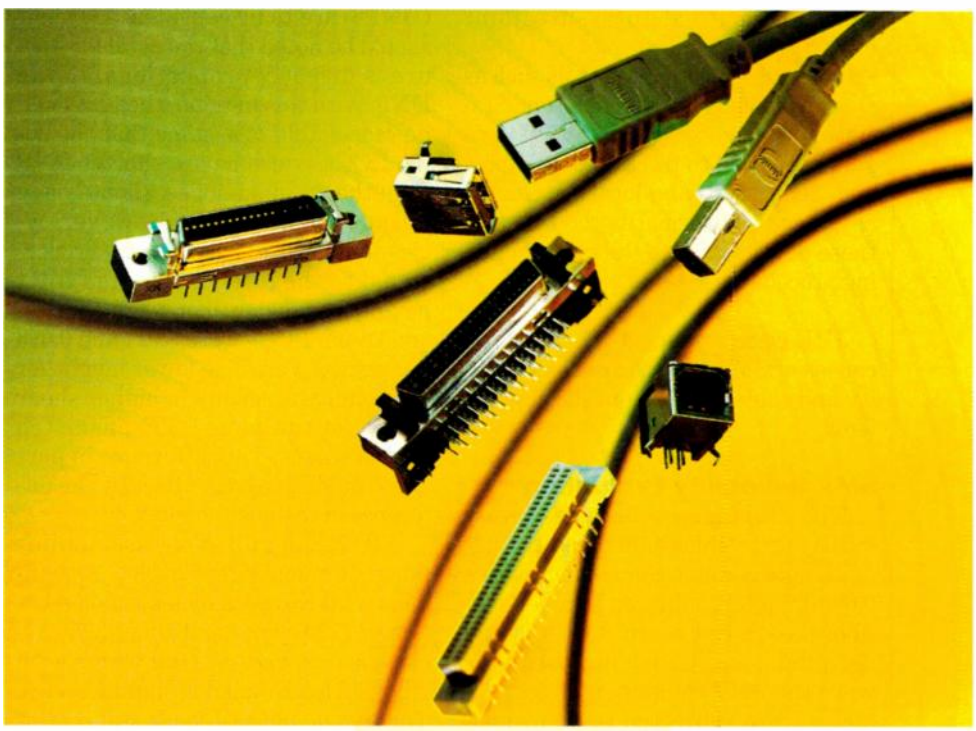

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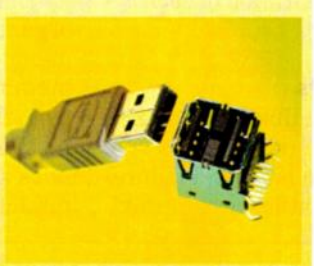

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an initial survey and research on the design, modeling, manufacturing, test, and deployment (aging) cycles. Findings from the survey and reliability results for conventional packages are discussed here:

- Coplanarity is extremely critical for leaded packages.
- The assembly defects most reported by the QA SMT survey are: insufficient solder, no solder, and poor wetting.
- Dewetting is the single most important feature that an inspector should flag.
- Paste qualification tests, inspection following the paste print, part placement, and after-solder-reflow inspections are critical to assure joint integrity.
- Manufacturing analysis tools such as Design of Experiment (DOE) and Statistical Process Control (SPC) are generally used to track solder defects and defect type and location. Generally, there is no formal method of tying these defects back to the manufacturing procedures.

JPL concludes that the leading causes of SMT rejects are solderability and solder-paste deposition problems.

SMA Reliability Evaluation

The surface-mount assembly (SMA) test vehicles involved the use of a single ceramic component, with a 0.050-in. pitch, soldered to an epoxy-fiberglass, FR-4 board. LCCs, J-lead cerquads, and gull-wing cerquads were the SMT components. Test vehicles were subjected to a thermal-cycle profile with long duration to ensure near-complete creeping. This long-duration cycle started at 25°C, with a decrease rate of 2°C/min. to –55°C, and with an oven-dwell setting of 45 min. The temperature was increased to 100°C at a rate of 2°C/min., with an oven-dwell setting of 45 min., followed by a decrease in temperature to 25°C. The duration of each cycle was 246 min.

SMA Test Results

The cycles-to-failure for 68-, 28-, and 20-pin LCC assemblies are ranked from low to high, and failure-distribution percentiles are approximated using a median plotting position [$F_i = (i-0.3)/(n+0.4)$] *(Fig. 2)*. As expected, there was a large spread in cycles-to-failure due to the common variances associated with materials and manufacturing conditions. These parameters incude solder-joint volume, quality of joint, and device location. The first failure for the 68-pin LCCs was detected at 53 cycles, while the last sample failed after 139, with 93 average cycles. The 28-pin LCCs failed at much higher cycles in the range of 352 to 908, with 660 average cycles. The 20-pin cycles-to-failure were in the same range as for those of 28-pins, and failed within 573 to 863, averaging 674 cycles.

If only distances to neutral points (DNPs) are to be considered, then it should be noted that the cycles-to-failure is directly proportional to the DNP With this in mind, then it would be reasonable to assume that the 20-pin LCCs, which have a shorter DNP than the 28-pin devices, should have failed at higher cycles. However, cycles-to-failure is also inversely proportional to the effective solder-fillet height. The solder-fillet heights for 20- and 28-pin LCCs were 0.021 and 0.033 in., respectively. The lower height for a 20-pin LCC results in higher shear strain for the same CTE-mismatch displacement. The difference in part sizes could have been offset by the difference in the fillet heights.

All 68-pin gull-wing assemblies failed at much higher cycles. Assemblies with Kovar-alloy leads failed between 1720 cycles and about 3750 cycles *(Fig. 2, again)*. Gull wings with Alloy 42 leads failed at higher cycles. The testing of the J-leads still continues, and as of March 1998, has reached more than 5000 cycles. This includes several hundred –55° to 125°C cycles. Most of the J-leads have now have failed, and are being checked for failure locations.

BGA Technology

To address the many common quality and reliability issues of BGAs, JPL organized a consortium with sixteen members in early 1995. The diverse membership, including individuals from the military, commercial, academia, and infrastructure sectors, permits a concurrent engineering approach to resolve many challenging technical issues.

BGA is an important technology for higher pin counts, without the attendant handling and processing problems of the peripheral leaded packages. BGAs also are robust during processing due to their higher pitch (0.050 in., typical), better lead rigidity, and self-alignment characteristics during reflow.

A BGA's solder joints cannot be inspected and reworked using conventional methods, and the devices are not well-characterized for multiple, double-sided-assembly processing methods. In high-reliability SMT assembly applications, such as space and defense, the visual inspection of solder joints has been standard practice and a key factor in providing confidence in solder-joint reliability.

Test-Vehicle Configuration

The two test-vehicle assembly types were plastic (PBGA) and ceramic (CBGA) packages. Both FR-4 and polyimide PWBs with six 0.062-in.-thick layers, were used.

Plastic packages covered the range from overmolded pad-array carriers (OMPACs) to SuperBGAs (SBGAs). They included:

- Two peripheral SBGAs (352 and 560 I/Os)
- A peripheral OMPAC (352 I/Os) and PBGAs (352 and 256 I/Os)
- A depopulated, full-array PBGA (313 I/Os)
- A 256-pin QFP with a 0.4-mm pitch

In an SBGA, the die is directly attached to an oversize copper plate. This design is intended to provide better heat dissipation than standard PBGAs. The solder balls for plastic packages were eutectic (63 Sn/37 Pb).

Ceramic packages with 625 and 361 I/Os were also included in our evaluation. Ceramic solder balls (90 Pb/10 Sn) with 0.035-in. diameters have a high melting temperature. They were attached to the ceramic substrate with eutectic solder (63 Sn/37 Pb). At reflow, package-side eutectic solder and PWB-side eutectic paste are reflowed to provide the electro-mechanical interconnects.

The plastic packages had dummy and daisy-chain patterns, with the daisy chains on the PWB designed to

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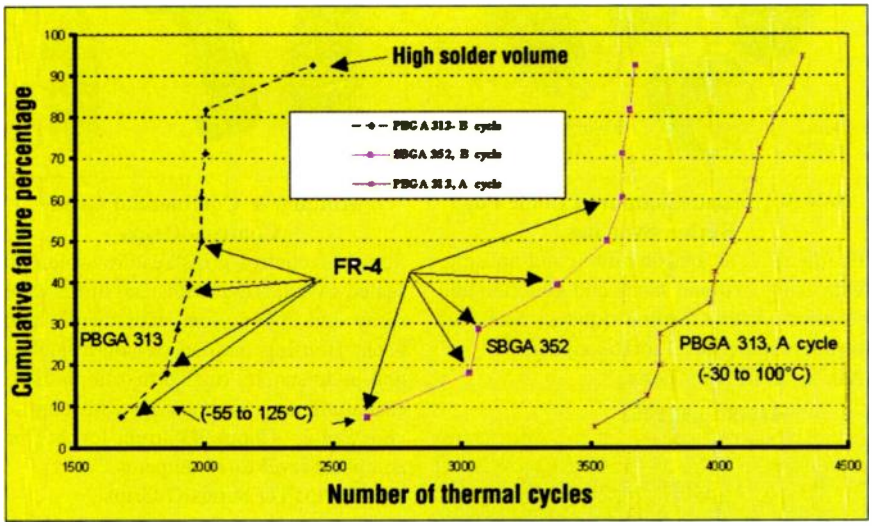

5. A graph of cycles versus cumulative failure percentages for first failure of PBGA 313 and SBGA 352 packages subjected to B cycling for assemblies on polyimide and FR-4 PWBs shows their relative advantages. The most current PBGA 313 assemblies that failed under cycle-A conditions are also included in the plots for comparison. These assemblies include those reflowed with low, standard, and high solder-paste levels.

allow the monitoring of critical solder-joint regions. Most packages had four daisy-chain patterns, 560-I/O units had five, and the QFP had one.

Thermal Cycling Of BGAs

Two significantly different thermal cycle profiles were used at two facilities. The cycle A condition ranged from –30° to 100°C, and had an increase/decrease heating rate of 2°C and a dwell of about 20 min. at the high temperature. This ensured near-complete creeping. The duration of each cycle was 82 min. The cycle B condition ranged from –55° to 125°C. It also could be considered a thermal shock because it used a three-region chamber: hot, ambient, and cold. Heating and cooling rates were nonlinear, and varied between 10° to 15°C/min., with dwells at extreme temperatures of about 20 min. The total cycle lasted approximately 68 min. BGA test vehicles were continuously monitored through a LabView system at both facilities.

The criteria for an open solder joint, as specified in IPC-SM-785, Sect. 6.0, were used as guidelines to interpret electrical interruptions. Generally, once the first interruption was observed, there were many additional interruptions within 10% of the cycle life. In several instances, a few nonconsecutive early interruptions were not followed by additional interruptions until significantly later stages of cycling. This occurred more frequently with plastic packages.

Damage Monitoring

Both board- and package-interface cracking were observed with an increasing number of cycles *(Fig. 3a and b)*. Failure under the A-cycle conditions were generally from the PWB. In the case of the B-cycle conditions, failures came from the package sites. Failure-mechanism differences could be explained by global or local stress conditions. Modeling indicates that the high-stress regions shifted from the board to the packages when stress conditions changed from the global to local. The A cycling, with slow heat/cooling ramping, allowed the system to reach a uniform temperature. Damage could therefore indicate a global stress condition. Damage during the B cycle, with rapid heat/cooling, could indicate a local stress condition.

Among the plastic packages, the PBGA 313, with depopulated full-array balls, was the first to fail under both the B and A thermal-cycling conditions. Various cross-sections of this package's solder balls from corner to the center at 4682 A cycles are shown in Figure 4. These photos represent the balls under the die where most damage occurs due to local CTE mismatches. Photos, with and without voids, were also included for comparitive analysis.

Voids appear to have concentrated at the package interface under the die. Cracking propagation occurred at package or board interfaces for sections with or without voids. The sections with voids were opens, as indicated by the seepage of mounting materials into voids. Except for the interface-connecting cracks, there appeared to be no crack propagation among the voids.

BGA Thermal Cycling Results

Cycles to first failure for PBGA 313 and SBGA 352 subjected to B cycling for assemblies on polyimide and FR-4 PWBs can be seen in Figure 5. The most current PBGA 313 assemblies that failed under cycle-A conditions are also included in the plots for comparison. These assemblies include those reflowed with low, standard, and high solder-paste levels.

Why CSPs?

Defined as packages that are up to 1.2 to 1.5 times larger than the perimeter or the area of the die, CSPs combine the small size and performance of the bare die or flip-chip, with the advantages of standard die packages. The technology competes with bare-die assemblies, and is now at the stage that BGAs were about two years ago. Many manufacturers now refer to the CSP as a miniature version of the previous generation. There are two types of CSPs: those with flex or rigid interposers, and those based on wafer-level molding and assembly redistribution *(Fig. 6)*.

The CSP packaging accomplishes many purposes, including:

- Provision of solder balls and leads that are compatible with the PWB pad metallurgy for reflow assembly processes.
- Redistribution of the tight pitch of the die to the pitch level within the norm of PWB fabrication. The small size of CSPs does not allow significant redistribution, and the current, cost-effective, PWB fabrication limits full adoption of the technology, especially for high I/O counts.
- Protection of the die from physical and alpha radiation damages, and dissipation of thermal energy.
- Overall s4implification of die-func-

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tionality testing.

Self-Alignment

CSPs can be categorized into grid arrays and leads (or no leads). The mini- (fine-pitch) grid arrays can accommodate higher pin counts, and, as in the case of BGAs, they have self-alignment (centering) characteristics. For BGAs, the ease of package placement requirements has been widely published as one of their attributes. This feature reduces the number of solder-joint defects to lower levels than conventional SMT packages. Grid CSPs have self-alignment characteristics, but there is disagreement on the best offset limits.

Reliability Of SMTs And CSPs

For comparison, projected cycles-to-failure for low-count CSPs as well as SMT assemblies were gathered from literature, and projected from a modified Coffin-Manson relationship. Board reliabilities of most CSP packages were found to be comparable or better than their LCC counterparts. These packages, however, are not as robust as leaded packages, including the popular gull wing and J-lead versions of these.

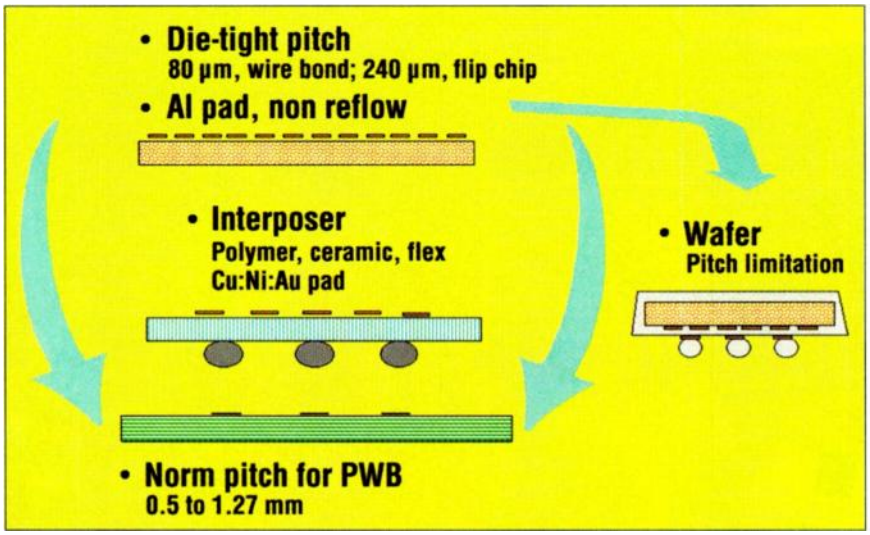
Lessons And Recommendations

Conventional SMT

- CTE differences between the package and board are the key factors affecting solder-joint failure by thermal cycling. Creep and stress relaxation are main causes of cycling damages.
- Package size and CTE, as well as the CTE absorption capability (e.g., leaded springiness versus no lead) are key factors that define solder-joint reliability.
- The leadless ceramic packages with 68 terminations showed the lowest cycles-to-failure, followed by 28 and 20 terminations.
- Both 68-pin QFPs and J-leads showed an order of magnitude higher number of cycles-to-failure than the leadless packages.
- Solder volume affects joint reliability, and must be controlled during the manufacturing process prior to part placement.
- The leadless packages with 20 and 28 terminations showed the same range of cycles-to-failure. The 28-termination version had higher solder volume (stand off). Cycles-to-failure increases with solder volume, but decreases with package size.
- J-leads showed higher cycles-to-failure than QFPs.
- QFPs with Alloy 42 lead materials showed higher cycles-to-failure than those with the Kovar materials.
- Lead planarity requirements for fine-pitch packages are much more stringent than for plastic or ceramic BGAs.
- Solder joints with signs of dewetting must be rejected.

BGA packages and assembly

- BGA ball planarities were dependent on package type, but irrespective of package type, decreased as the size decreased.
- Ceramic packages showed lower warpage and were more coplanar than their PBGA counterparts. Numerous ceramic packages had tilted solder balls.
- Solder-ball planarities were significantly higher for plastic than for ceramic packages.
- PBGAs are more robust in accommodating package nonplanarity than ceramic packages; PBGA balls collapse during reflow processes, whereas CBGAs do not.
- Solder volume controls for ceramic BGA packages are more critical than for plastic BGA packages.
- The BGA assembly void levels were the same as those generally observed by industry (less than 20%).
- BGAs were robust in assembly, compared to the 256-pin, fine-pitch, 0.4-mm QFPs. All QFPs showed bridging to some degree, and had to be reworked.
- Voids can be introduced if an improper reflow profile is used for a specific solder paste. Dwell temperature and time are two key factors that affect void levels.
- Voids for plastic BGAs were much higher, and generally concentrated at the package interface.
- Rosin mildly activated (RMA) and water-soluble reflow profiles evaluated in this study were significantly different and optimized separately for the applications.
- Ceramic BGAs failed much earlier than their plastic counterparts due to their much larger CTE mismatch on FR-4/polyimide boards.
- Cycles-to-electrical-failure for ceramic BGAs depended on many parameters including cycling temperature range and package size (I/Os).
- Ceramic packages with 625 I/Os were the first to show signs of failure among the ceramic (CBGA 625 and CBGA 361) and plastic packages (SBGA 560, SBGA 352, OMPAC 352, and PBGA 256) when cycled to different temperature ranges.
- Joint failure mechanisms for assemblies exposed to two cycling ranges at two facilities were different.
- Ceramic assemblies cycled in the range of –30°C to 100°C showed cracking initially at both interconnections,



6. Defined as packages that are up to 1.2 to 1.5 times larger than the perimeter or the area of the die, CSPs come in two types—those with a flex or rigid interposer, and those based on wafer-level molding and assembly redistribution.

LINEAR TECHNOLOGY

DESIGN NOTES

Optimized DC/DC Converter Loop Compensation Minimizes Number of Large Output Capacitors – Design Note 186

John Seago

There is a trade-off between the cost of a few extra passive components and the flexibility that external loop compensation provides. Internal loop compensation is fixed, so it uses fewer passive parts but it also limits the designer's choice of output capacitors. The output capacitor should be chosen to meet the load requirements, not the regulator requirements. The external loop compensation provided by the LTC®1435 family of parts allows the control loop to be optimized for the output capacitance required by the load.

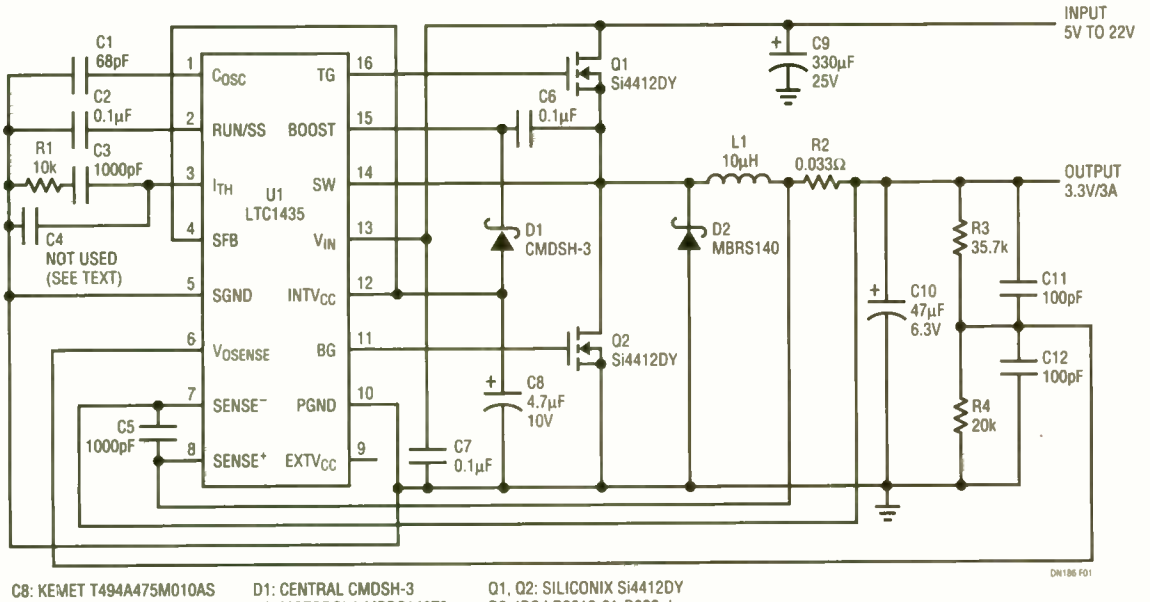
External Loop Compensation Can Save Money

By changing two or three passive component values, the LTC1435 allows the loop to be compensated for the output capacitor that meets the load requirements. External loop compensation allows the designer to optimize both the buck inductor and output capacitor for each application.

Although some loads have stringent transient requirements, many do not. The function of the output capacitor is to smooth the output voltage ripple and to source or sink output current until the regulator can respond to changes in load current. If the regulator can respond as quickly as the load current changes, very little output capacitance is required.

Figure 1 shows an LTC1435 configured for a 3.3V output with less than 50mV of output ripple and a 100mV transient response. The values for the primary loop-compensation components, C3 and R1, were selected by means of dynamic load testing, using the pulsed-load circuit shown in Figure 2. The load-pulser resistor values were selected to switch the load current between 1.5A and 3A at a 60mA/µs rate, to simulate actual load conditions. Figure 3 shows the output voltage transient waveform.

Briefly, the values of C3, C4 and R1 determine the voltage gain and phase of the internal error amplifier at different frequencies. The value of C3 determines the low frequency gain, R1 determines the midband gain and C4 reduces gain



C8: KEMET T494A475M010AS
C9: SANYO 25CV330GX
C10: SANYO 6SA47M
D1: CENTRAL CMDSH-3
D2: MOTOROLA MBRS140T3
L1: SUMIDA CDRH125-100
Q1, Q2: SILICONIX Si4412DY
R2: IRC LR2010-01-R033-J
U1: LINEAR TECHNOLOGY LTC1435CS

Figure 1. Low Output Capacitance Voltage Regulator

at high frequencies. Generally, the values of C3 and C4 should be as small as possible and the value of R1 should be as large as possible.

Loop Compensation Using a Dynamic Load

Although many engineers consider control-loop theory difficult, most of the work is already done when optimizing a circuit for a particular load. The component values shown in the data sheet will provide stable operation under all static load conditions and most dynamic load conditions. The process of optimizing component values is not difficult. Using a dynamic load, or the pulsed-load circuit shown in Figure 2, select the appropriate output capacitor and adjust the values of C3, C4 and R1 in Figure 1 to minimize the overshoot and ringing on the output voltage waveform. Now, verify that the output voltage transient waveform is correct over the entire input voltage range.

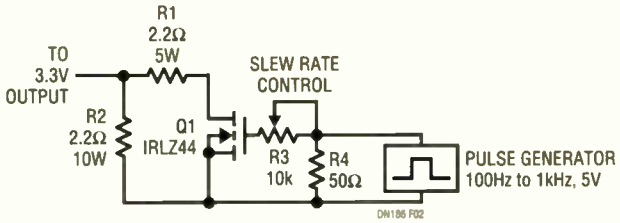


Figure 2. Pulsed-Load Circuit

It is also important to verify that the control loop is stable over the required operating temperature range. It is common to use a heat gun and freeze spray to test temperature extremes but it is important to monitor the actual temperature to avoid overtesting the circuit. It is best to use a temperature-controlled chamber for all temperature testing.

Testing loop stability over temperature is even more important when using regulators with fixed compensation. It may be necessary to add even more output capacitance to ensure stable operation over temperature.

Most labs don't have a dynamic load for power supply testing. The circuit in Figure 2 shows an inexpensive way to test load-transient response. The value of R2 was selected to draw the nominal, pretransient load current, whereas the value of R1 was selected for the required load-current step. Resistor R3 controls the slope of the load current step to better simulate actual load conditions.

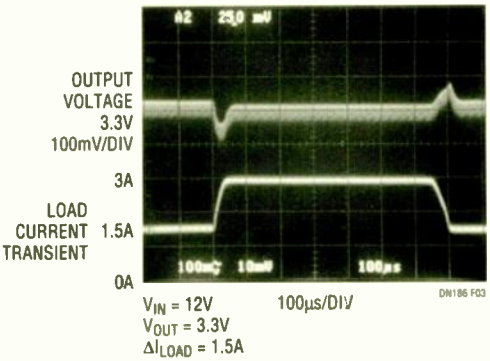


Figure 3. Transient Waveforms

The advantage of adjustable loop compensation is simple: optimizing loop compensation components allows the lowest cost output capacitor to be used for a given load requirement. Adjustable loop compensation is available on all of the LTC1435 family of parts. As shown in Table 1, both single and dual versions are available with a variety of additional features.

Table 1. LTC1435 Related Parts

PART NUMBER	DESCRIPTION	COMMENTS
LTC1436/LTC1436-PLL/ LTC1437	High Efficiency, Low Noise, Synchronous Step-Down Switching Regulator Controllers	Full-Featured Single Controllers
LTC1438	Dual Synchronous Controller with Power-On Reset and an Extra Comparator	Shutdown Current <30µA
LTC1439	Dual Synchronous Controller with Power-On Reset, Extra Linear Controller, Adaptive Power, Synchronization, Auxiliary Regulator and an Extra Uncommitted Comparator	Shutdown Current <30µA
LTC1538-AUX	Dual Synchronous Controller with AUX Regulator	5V Standby in Shutdown
LTC1539	Dual Synchronous Controller with the Same Features as the LTC1439	5V Standby in Shutdown

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with final separation generally from the board side through the eutectic solder. The board-side joints showed signs of pin-hole formation prior to cracking and complete joint failure.

- The failure mechanisms for ceramic BGAs that were cycled in the range of –30° to 100°C were similar to those reported in literature for 0° to 100°C thermal cycles.
- Ceramic and plastic BGAs showed different failure mechanisms, as evidenced from the total number of electrical interruptions with more cycles.
- The CBGA's first electrical interruption (open) was followed by consecutive additional interruptions, whereas the PBGA's was not followed by additional interruptions until a much higher number of cycles.
- The PBGAs with 313 I/Os, depopulated full arrays, were first among the PBGAs to fail within both cycling ranges.
- The 352 SBGA, with no solder balls under the die, showed much higher cycles-to-failure than the PBGA 313.
- For cycles with a 125°C maximum temperature, plastic package assemblies (PBGA 313 and SBGA 352 on polyimide) generally failed at a higher number of cycles than those on FR-4.

CSP assembly reliability

- The board-level reliabilities of most CSP packages are comparable to, or better than LCCs with similar I/O counts. These packages, however, are not as robust as leaded packages, including gull wing and J-leads.
- Grid BGAs and CSPs align themselves during the reflow process and, therefore, some misalignment is acceptable. Acceptable misalignment depends mainly upon package type, size, ball material, and weight.

Dr. Reza Ghaffarian has nearly 20 years of industrial and academic experience in mechanical, materials, and manufacturing process engineering disciplines. At JPL, Reza supports research and development activities in SMT, BGA, and CSP technologies for infusion into NASA's missions. He has authored over 50 technical papers, and has numerous patentable innovations. He received his M.S. inElectrical Engineering in 1979, and his Ph.D. in engineering in 1982 from UCLA.

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ELECTRONIC DESIGN
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PRODUCT UPDATE: SWITCHES & RELAYS

Manufacturer	Device	Description	Price and delivery	CIRCLE
SWITCHES				
APEM Components Inc. **Wakefield, MA** **Sales Dept. (781) 246-1007** **Fax (781) 245-4531** **info@apem.com** **www.apem.com**	9000 Series pushbutton switches	These single-pole, open or closed pushbutton switches have a diameter of 0.250 in. and a length 0.240 to 0.314 in. length. Both threaded and non-threaded bushings are available. The contacts are gold-plated brass rated 100 mA at 30 V dc and with a resistance of 30 mΩ(max). The dielectric strength is 500 V rms between terminals and 1000 V between terminals and case. The operating temperature range is -30° to 65° C.	Normally open version, 9533CD, $1.29 each per 1000.	525
C&K Components Inc. **Watertown, MA** **Sales Dept. (800) 635-5936** **Fax (617) 926-6846** **www.ckcorp.com**	KN Series tactile switch	This low-profile, ultra-miniature, tactile switch comes in both top- and side-actuated models with heights of 1.63 and 2.5 mm, respectively. Molded from high-temperature thermoplastic, the series can withstand surface-mount reflow soldering and have actuation forces that range from 120 to 450 g. Mechanical life ranges from 100,000 to 200,000 cycles. Tape-and-reel packaging is standard for all models.	$0.35 each per 10,000; stock to six weeks	526
C&K Components Inc. **Watertown, MA** **Sales Dept. (800) 635-5936** **Fax (617) 926-6846** **www.ckcorp.com**	CD Series, DIP-coded rotary switches	The company has expanded its CD Series of DIP-coded rotary switches to include an eight-position version on top of its 10- and 16-position models. The switch comes with gull-wing, thru-hole, or right-angle thru-hole terminations, and with real or complement output codes. Actuator styles include flush, extended, and knob. Contacts are gold plated and are rated at 0.4 A at 20 V dc or ac. Tape-and reel packaging is available.	$2.40 each per 1000; stock to four weeks	527
CP Clare Corp. **Beverly, MA** **Sales Dept. (800) CPCLARE** **Fax (978) 524-4900** **www.cpclare.com**	170 series optically coupled MOSFET switch	These optically coupled, integrated MOSFET switches come in a range of configurations, including single pole, double pole, Form A/B, and with multiple switches per package. Featuring logic-compatible 2-mW drive-power requirements, the devices have an on resistance of 50Ω, can handle a continuous current of 100 mA and a peak load voltage of 350 V, and provide 3750 V rms of I/O isolation.	Single pole, normally open, $1.08 each per 10,000	528
ITT Industries **Eden Prairie, MN** **Sales Dept. (612) 934-4400** **Fax (612) 934-9121** **www.ittind.com**	KST rubber tact switch	This rubber tact switch combines the dimensional and electrical characteristics of the dome-type tact switch family, with the long travel and tactile feel of conductive rubber. Features include a travel distance of 1.3 mm, silver-plated contacts, and J- or G-type, tin-plated terminals. The devices measure 6 by 6 mm and have operating forces of 200 or 350 g.	$0.16 to $0.45	529
OTTO Engineering Inc. **Carpertersville, IL** **Jim Flanigan (847) 428-7178** **Fax (847) 428-1956** **E-mail: jim.flanigan@ottoeng.com** **www.ottoeng.com**	U2-277 sealed rocker switch	Able to run over a million cycles and withstand extreme environmental conditions, these SPDT rocker switches have a completely enclosed housing that can be sealed to various levels. The devices come with gold-plated contacts, a 10-A rating, and a choice of terminations, including quick connects, printed-circuit tails, screw terminals, and pig tails. Intelligence can be added using an extra board and microchip.	$20 each; eight weeks ARO	530
Switches Plus **Milford, CT** **Dan DiGioia (203) 876-2697** **Fax (203) 876-7285**	Series 44 emergency stop switch	Designed to give a rapid positive response, these emergency stop switches come with UL and CSA approval, along with CE marking. Key features include a 22.5-mm hole mounting and the need to perform a deliberate twist of the bright-red actuator to reactivate the circuit. A key-based unlocking system is optional.	$19.95	531
Toko America Inc. **Mt. Prospect, IL** **Bill Edmiston (847) 297-0070** **Fax (847) 699-1194** **E-mail: Info@tokoam.com** **www.tokoam.com**	TK70001 solid-state switch	Designed for low-power devices, this low-noise, solid-state switch has a single input with two independently controlled outputs. Based on a PNP power transistor, the device features a high output impedance to bring power current flow to zero when the control pin is off. Other features include an output current of 130 mA, a power dissipation of 350 mW, a dropout voltage of 0.17 V, and a quiescent current of 3.5 mA.	$1.35 each per 3000	532
RELAYS				
Crydom Corp. **San Diego, CA** **Tony Bishop (800) 8 CRYDOM** **Fax (619) 715-7210** **E-mail: tony bishop@crydomsales.com** **www.crydom.com**	CMD series of SSRs	Available in 25-, 50-, 75-, 90-, 110-, and 125-A versions, these solid-state relays (SSRs) come with voltage ratings of 240, 480, or 600 V ac (heatsink required). All models are SPST (normally open) and are surface mountable. Other features include protective recessed contacts, back-to-back SCR switching, zero-voltage or phase-controlled turn on, and box-clamp I/O connectors. The devices meet EN60950 (Low Voltage Safety Directive) and are CE marked.	$26.50 to $34.04 each per 100; stock to four weeks	533
Crydom Corp. **San Diego, CA** **Tony Bishop (800) 8 CRYDOM** **Fax (619) 715-7210** **E-mail: tony bishop@crydomsales.com** **www.crydom.com**	CoolPak Series SSRs with heatsink	This series of SSRs come with an optimized integral heatsink that allows the devices to output currents of 35, 45, 55, or 65 A, at voltage ratings of 240, 480, and 600 V ac. Based on all-surface-mount technology, the relays feature DIN-rail or panel mounting. Other features include protective recessed contacts, back-to-back SCR switching, zero-voltage or phase-controlled turn on, LED status indication, and box-clamp I/O connectors.	$34.05 to $60.32 each per 100; stock to four weeks	534
Fujitsu Takamisawa America Inc. **Sunnyvale, CA** **Sales Dept. (800) 380-0059** **Fax (408) 745-4971** **E-mail: marcom@fta.fujitsu.com** **www.fujitsufta.com**	FTR-F2 miniature power relay	This subminiature power relay measures 24 (L) by 11 (W) by 25 (H) mm and is TV-5 rated for high-density pc-board mounting in consumer applications. Able to withstand 10-kV surges, the device comes with silver-alloy contacts capable of switching up to 5 A at 250 V ac or 30 V dc. The relay comes in SPST-NO format with coil ratings of 5 to 40 V dc. Other features include a dielectric strength of 4 kV and UL, CSA, and VDE approvals.	$1.23 each per 1000; stock	535

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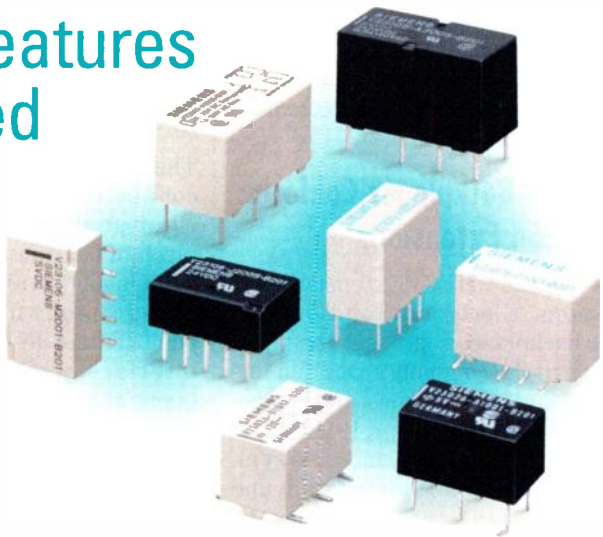

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Contact Rating	30W 60VA	30W 62.5VA	60W 62.5VA	60W 125VA	50-150W 250VA
Nominal Coil Power	30-150mW	100-200mW	70-140mW	150-300mW	75-360mW
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READER SERVICE 164

Ribbon Cable Has 175 Controlled-Impedance Lines

Featuring near-coax performance, this high-density, shielded, ribbon-cable assembly has up to 175 controlled-impedance signal lines. The assembly uses a single Berg Micro-Pax connector, has two ground lines between each signal, and employs the company's Sinusoidal Weave, controlled-impedance cable. The impedance is 90 Ω, ± 10%. Capacitance is 14 pF per ft., and the forward and backward crosstalk figures are given as 1% V_{IN} per ft. and 3% V_{IN} (max), respectively. UL and CSA approvals apply. Passive and active components can be embedded to specifications. Pricing for a typical assembly is $225 each per 100.

***Woven Electronics**, 1001 Old Stage Rd., Simpsonville, SC 29681; Doug Piper (864) 967-1751; fax (864) 963-1761; e-mail: doug.piper@internetMCI.com; www.wovenelectronics.com.*

CIRCLE 540

DC Power Jacks Come In A Range Of Configurations

This line of dc power jacks accepts female plugs with center-hole diameters ranging from 1.3 to 4.3 mm. The devices can be mounted—either right angle or vertical—onto pc boards, panels, and chassis. Molded from PBT thermoplastic, the power jacks can be specified as closed- or open-frame units, containing either nickel- or silver-plated internal components. Pricing for one version—the 0202 with a 2.1-mm center pin, right mounting, and nickel-plated internal components—is $0.18 each per 10,000. Delivery is 30 days.

***Shogyo International Corp.**, 45 Executive Dr., Plainview, NY 11803; (516) 349-5200; fax (516) 349-7744; e-mail: info@shogyo.com; www.shogyo.com.*

CIRCLE 541

10-Layer Backplanes Conform To VME64 Extensions

Able to meet VME64 Extension specifications, Electronic Solutions' 10-layer backplanes represent the latest entries to the company's Dot Ten line of enclosures, backplanes, and components. Available with 5, 7, 10, 12, 15, or 21 slots, the 7U backplanes use symmetrical stripline construction and are fully compliant with established VITA 1.1 specifications. The power connectors have been placed below J2 to eliminate interference when used in applications requiring rear plug modules. Other features include automatic daisy-chaining circuitry and a 2-mm JO connector that conforms to IEC 1076-4-101 Level 1. Pricing is $712 for 100 pieces.

***Electronic Solutions, A Zero Corp.**, 6790 Flanders Dr., San Diego, CA 92121-2902; Lori Mathios (619) 452-9333; fax (619) 452-9464; e-mail: lorim@elsol.com.* **CIRCLE 542**

Docking Connectors Come In Ultra-Slim Format

The EX series of ultra-slim docking connectors come in 80- or 240-pin, right-angle-mount versions with a pitch of 0.8 mm. A 200-pin stacking type is also available for slim notebook, top-down docking. The two-point contact design ensures a reliable interface, while the three-step sequential contacts allow signal connection status detection. Male contacts are protected by a molded barrier

(continued on page 85)

PRODUCT UPDATE: SWITCHES & RELAYS

Manufacturer	Device	Description	Price and delivery	CIRCLE
RELAYS				
International Rectifier **El Segundo, CA** **ProCenter (310) 252-7105** **www.irf.com**	PVT442 micro-electronic relay	Targeting telecom applications, this microelectronic relay comes with 1 Form B contacts and an I/O isolation rating of 4000 V rms. The contact ratings are 400 V dc or ac (peak) and 170 mA (ac) or 300 mA (dc). The contact resistance is 16 Ω (max) in ac mode and 7 Ω (max) in dc mode. UL and BABT certifications are pending	$1.52 each per 25,000; six-to-eight weeks ARO	536
Omron Electronics Inc. **Schaumburg, IL** **Sales Dept. (800) 55-OMRON** **Fax (847) 843-8081** **www.omron.com**	G6K low-signal relay	Designed for high-density, pc-board applications, this low-signal relay measures 5.3 by 10.2 by 6.7 mm, and comes with a multibend lead-frame design to reduce stress on the solder joint by up to 75%. Along with pc-board through-hole and SMT gull-wing versions, the device comes in the company's SMT inside-L version that allows relays to be placed both end to end and side to side. Other features include a power consumption of 85 to 100 mW, a rating of 1 A at 30 V dc and 0.3 A at 125 V ac, and a release and bounce time of 3 ms (max).	$2.22 each per 1000	537
SSAC Inc. **Baldwinsville, NY** **Dave Eastwood (800) 377-7722** **Fax (315) 638-0333** **www.ssac.com**	KRDB series time-delay relay	This ultra-compact, encapsulated, time-delay relay is rated at 10 A. The miniature, SPDT device combines microcomputer timing and on-board knob adjustment in a 2- by 2- by 1.2-in. molded package. The delay-on-break timer can be knob adjusted or factory set for delays ranging from 100 ms to 1000 min. in six ranges. The repeat accuracy is ±1%, and the input voltages include 12, 24, and 110 V dc, or 24 and 120 V ac. The contacts are rated at 10 A.	$20.80 each per 100	538
Wieland Electric Inc. **Burgaw, NC** **Sales Dept. (910) 259-5050** **Fax (910) 259-3691** **www.wielandinc.com**	WRS relay with plug-in jumpers	To avoid cutting and stripping jump wires when distributing input power to individual relays, this line comes with plug-in jumpers. The system allows a single power supply to power up to 15 WRS series modules. Available in single- or double-pole configurations, the relays target dc, single-phase, and three-phase applications.	$12 to $58; stock	539

(continued from page 84)
which prevents deformation, and a flexible metal shell absorbs stress. Per mated pair, pricing is $21.62 each in 1000-unit quantities. Delivery is six to eight weeks.

***Hirose Electric (USA) Inc.**, 2688 Westhills Court, Simi Valley, CA 93065; Sales Dept., (805) 522-7958; fax (805) 522-3217; www.hirose.com.* **CIRCLE 543**

Passive Copper GBIC Is Hot-Pluggable

Compliant with the Gigabit Interface Converter (GBIC) specification Rev. 4.5, this blind-mate, passive copper GBIC is hot-pluggable and comes with signal detect and inrush current limiting. The signal-detect feature enhances performance in applications where noise is an issue. The 20-position SCA 2 connector also meets Rev. 4.5 specifications, while the six-position HSSDC I/O connector conforms to Fibre Channel Ph-3. The interconnect supports connections via copper HSSDC cables for distances of up to 13 m. Pricing is $23 each per 25,000.

***AMP Inc.**, P.O. Box 3608, Harrisburg, PA 17105; Information Center (800) 522-6752; www.amp.com.*
CIRCLE 544

Angle DIMM Connectors Save On Space

Targeting high-end servers, graphics cards, and other space-constrained applications, these robust DIMM connectors come in both right-angle and 25°-angle versions. With a pitch of 0.050 in., the connectors are available with 168 or 200 circuits and in three tail lengths. The contacts are molded into the housing and plastic pegs hold the sockets to the pc board. Dual latches align modules for insertion, reduce micro motion, and have an audible click when closed. Pricing for the 25° version is $9.74 each per 5000. Delivery is from four to six weeks.

***Molex Inc.**, 2222 Wellington Court, Lisle, IL 60532; Sales Dept. (800) 78-MOLEX; fax (630) 969-1352.*
CIRCLE 545

Passive Junction Boxes Suit Harsh Environments

Hirschmann's line of passive junction boxes were developed to ensure dependable connections to sensors and actuators in harsh environments. Operating with 12-mm cabling, the boxes are preassembled to eliminate costly and time-consuming operations. Users simply screw the box directly to a mounting face in the vicinity of the sensors or actuators. Versions include a built-in terminal block or a box with a preassembled, integrally molded, 5- or 10-m connection lead coated in corrosion-resistant polyurethane. Both versions offer protection to IP 68, LED status display, four- or eight-way distribution, and handle up to 2 A per I/O at 10 to 30 V dc. Pricing for a four-way, 12-mm version with terminal block is $99. Delivery is from stock.

***Hirschmann**, Industrial Row, P.O. Box 229, Riverdale, NJ 07457; Dawn Gibbons (800) 225-0524, ext.350; fax (973) 835-8354.* **CIRCLE 546**

IndustryPack Connectors Are Surface-Mountable

These 50-pin, SCSI-3-style IndustryPack connectors are surface-mountable. Available in sizes 20 through 120, the connectors are designed for board-stacking applications to free up space. Pricing is $0.06 per contact in volume.

***Comm Con Connectors Inc.**, 1848 Evergreen St., Duarte, CA 91010; Sales Dept. (818) 301-4200; fax (818) 301-4212; e-mail: info@commcon.com; www.commcon.com.* **CIRCLE 547**

Combination Mini-DIN Connectors Are Stacked

The KMDG series of combination-contact mini-DIN connectors come in a stacked configuration. Targeting audio, video, and digital equipment applications, the connectors come in six-over-eight-position and six-over-four-position versions to save on-board space. All are fully shielded against EMI/RFI, use phosphor-bronze contacts with gold-flash plating, and are CSA/NRTL/C certified. The body is made from UL94V-O-rated PBT thermoplastic. The contact resistance (plug to terminals) is 60 mΩ (max) and the current rating is 1 A at 12 V dc. Pricing is $1.52 each per 5000; delivery is six to eight weeks.

***Kycon Inc.**, 1810 Little Orchard St., San Jose, CA 95125; Sales Dept. (408) 494-0330; fax (408) 494-0325; www.kycon.com/kycon.* **CIRCLE 548**

High-Temperature Pc-Board Headers Save Assembly Time

The Series 86 and 87 Eurostyle pc-board headers are spaced on 5.08-mm and 5.0-mm centers, respectively. The blocks are available in vertical and horizontal configurations and come in lengths of 2 to 12 circuits. The headers' polymer construction handles temperatures up to 250°C and makes them compatible with pin-and-paste and intrusive-reflow techniques. Other features include 94V-O inflammability rating and VDE/IEC compliance. Pricing per circuit is $0.15 each per 1000; delivery is three weeks ARO.

***Beau Interconnect**, 4 Aviation Dr., Gilford, NH 03246-6600; Sales Dept. (603) 524-5102; fax (603) 524-1627; e-mail: info@beauint.com; www.beauint.com.*

CIRCLE 549

CompactFlash Connectors Are Surface-Mountable

The FCN-560H CompactFlash connector consists of a right-angle SMT plug and a 50-position, single-sided or straddle-mount SMT socket. The plug has a single row of leads on 0.635-mm centers and also comes in a 1.64-mm elevated version. The connector is rated at 0.5 A dc and 250 V ac. The contact resistance is 80 mΩ, the insulation resistance is 1000 MΩ, and the insertion and withdrawal life runs 10,000 cycles. Pricing without ejector is $2.35 each per 10,000; delivery is six to eight weeks ARO.

***Fujitsu Takamisawa America Inc.**, 250 E. Caribbean Dr., Sunnyvale, CA 94089; Info. (800) 380-0059; fax (408) 745-4971; Internet: www.fujitsu.takamisawa.com.* **CIRCLE 550**

BGA Adapter And Socket Modules Target Development

The Mill-Max line of BGA adapter and socket modules convert a BGA package to a pluggable device. This makes it possible to remove the device without damaging the host pc board. Targeting ASIC and CPU development applications, the modules comprise a male pluggable adapter and an ultra-low-insertion-force socket that's surface-mountable. The insulators for both parts are made from FR-4 epoxy, which has a TCE to match the BGA and pc board. The modules accept high-pin-count packages, typically on 0.050-in. spacing. The pins and sockets are machined brass and plated gold; press fit into each mating socket is a beryllium-copper multi-finger contact. In quantities of 25, pricing for the adapter is $0.135 per pin, while the socket is $0.15 per pin position. Delivery is approximately four weeks.

***Mill-Max Mfg. Corp.**, 190 Pine Hollow Rd., P.O. Box 300, Oyster Bay, NY 11771-0300; Carla Rapacciuolo (516) 922-6000, ext.211; fax (516) 922-9253.* **CIRCLE 551**

Pc-Board-Mount Jack Comes With Bottom Entry

The 3026 Series modular RJ45 jack features bottom entry for applications in modems, computers, 10Base-T, and hubs. As the jack snaps over a cutout, its pins insert directly into the pc board. Available in either shielded or non-shielded versions, the standard jack (eight positions) features nickel-plated contacts with up to 35 µin. of gold plating. The series is constructed using UL-94V-O glass-filled polyester. Pricing is $0.90 each per 1000. Delivery is from stock to eight weeks.

***Bomar Interconnect Products Inc.**, 1850 Rte. 46 East, Ledgewood, NJ 07852; Sales Dept. (973) 347-4040; fax (973) 347-2111; Internet: www.bomar-inteconnect.com.* **CIRCLE 552**

Interconnect Targets Gigabit Serial Data Transfer

The High-Speed Serial Data Connector (HSSDC) allows for data transfer at rates of up to 2.125 Gbits/s through copper cable over distances of up to 30 m or more. Approved by the ANSI X3T11 committee for Fibre Channel, the HSSDC system also is being considered by ANSI X3T11.1 for Serial Storage Architecture and by IEEE 802.3 for Gigabit Ethernet. The connector itself is a controlled-impedance, fully shielded system with eight-positions. The system uses the proven CHAMP 0.050 Series II contact interface with high-durability contacts on 0.125-mm centerlines. Board-mount receptacles are available in straddle-mount or right-angle versions loaded with six or eight contacts. Features include a low profile to meet the 10-mm PCI requirement and make-first/break-last mating contacts. Pricing for a typical 5-m HSSDC cable assembly is under $40.00 each per 5000.

***AMP Inc.**, P.O. Box 3608, Harrisburg, PA 17105-3608; Product Info. (800) 522-6752; www.amp.com.* **CIRCLE 502**

Circle 520

Spice Simulator Tunes RC Active-Filter Circuits

LUTZ VON WANGENHEIM
Dept. of Electrical Engineering, Hochschule Bremen, Neustadtswall 30, 28199 Germany; fax (49) 421 5905 476; e-mail: wangenhm@etech.hs-bremen.de.

It's common practice to design active filter circuits by treating operational amplifiers as ideal devices. This simplification, however, can lead to significant deviations from the desired frequency response—primarily due to the finite gain-bandwidth product (GB) of real amplifiers.

Conventional techniques for reducing this influence (passive/active phase compensation, predistortion) aren't very effective because they consider only a single-pole op-amp model. Moreover, they neglect other imperfections (e.g., input, output, and load impedances; pin parasitics). Recently, National Semiconductor Corp., Santa Clara, Calif., published a design note[1] describing an alternative and somewhat cumbersome tuning method consisting of several iteration steps with alternating calculations and measurements or simulations. The method also requires knowing all parameter sensitivities that are specific to each filter topology.

This design idea presents a much simpler technique for compensating amplifier imperfections, using suitable simulation software supported by realistic amplifier macromodels. The basic idea of the proposed method is to adjust the filter's loop gain at the pole frequency (f_P) to the specified value, thereby correcting the pole location and, hence, the transfer function of the filter ("pole tuning"). For this purpose, a certain part of the feedback network has to be modified, whereby the new element values are calculated within one simulation run only.

COMPARISON OF POLE PARAMETERS

	Pole frequency f_p (MHz)	Pole Q Q_p	Gain H_p
Ideal	42.36	3.5	1.43
Real (not tuned)	36.2	2.2	0.775
Real (tuned)	43.15	3.37	1.21

The proposed technique uses the "Substitution Theorem," which allows an exchange between an arbitrary branch Z of a linear network and an independent source without influencing voltage-to-current ratios—provided there's only one solution for these ratios.[2] Since this is the case, specifically, for a feedback system having a loop gain of unity ($A_L = 1$), an artificial block TUNER is inserted into the feedback path of the filter *(see the figure)*. The transfer parameters of the tuner block must be identical to the reciprocal loop gain (magnitude A_{LP}, phase Φ_{LP} in degrees) of the ideal filter circuit at the desired frequency ($f_Z = f_P$). For this purpose, the following expression can be used to advantage:

$$H_{TUNER} = (1/A_{LP}) \times \exp[-\Phi_{LP}\pi s/(180|s|)]$$

where s = the complex frequency variable.

In addition, to preserve proper loading of the op amp, the TUNER input must be connected to an artificial current source simulating the output load under closed-loop conditions:

$$I_{LOAD} = I_T/H_{TUNER}$$

where I_T =the current through the TUNER output terminal.

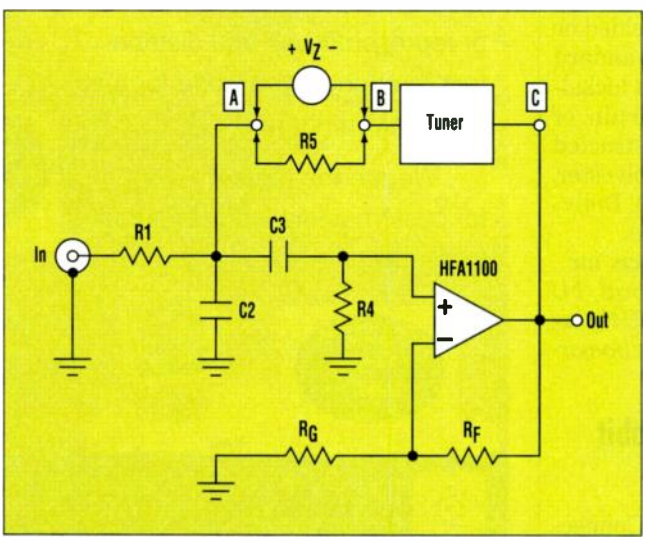
Hint: Both functions can be implemented very easily as a separate subcircuit using analog behavioral modeling techniques available in many simulation packages, such as MicroSim's PSpice.

In principle, the "pole-tuning" method can be applied to all second-order low-pass and bandpass topologies. The bandpass example presented in the figure is, for comparative purposes, identical to the Sallen-Key section A as given in the National Semiconductor design note. However, instead of NSC's CLC446, a similar part will be used (the HFA1100 from Harris Semiconductor), in conjunction with a feedback resistor (R_F = 560 Ω) as recommended by the manufacturer.

Assuming an ideal amplifier, the bandpass characteristic as specified in the table (first row) can be realized using the element set as given here (taken from NSC's design note):

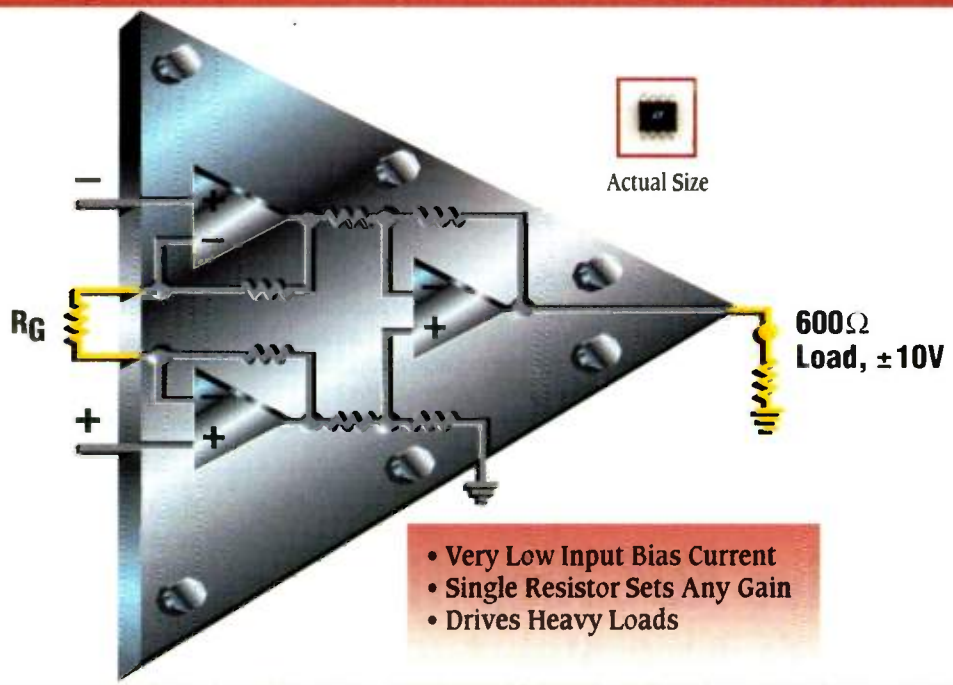
R1 = 120.3 Ω [121]; R4 = 747.9 Ω [750]; R5 = 20.4 Ω [20.5]; K = 1 + R_F/R_G = 1.29 [1.294]; R_F = 560 Ω [562]; R_G = 1.93k [1.91k]; C2 = 98.67 pF [100 pF]; C3 = 10.95 pF [11 pF]

The values in brackets are the nearest nominal standard 1% value that cause, together with a realistic HFA1100



Utilizing this loop configuration with R5 replaced by V_S and with a properly designed TUNER block, a circuit-simulation program calculates the modifications needed to compensate the effect of amplifier imperfections on the filter transfer function.

Industrial Strength Instrumentation Amp



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Industry Standard Pin Out And Gain Resistor

$G = 1 + 49.4k/R_G$

Gain	R_G
1	∞
10	5490Ω
100	499Ω
1000	49.5Ω
10,000	4.94Ω

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macromodel—a severe pole displacement *(see the table, second row)*.

Setting the TUNER parameters requires the ideal loop gain of the filter to be determined first. A simulation with the ideal components and with an open feedback loop between terminals B and C yields at the pole frequency (f_P = 42.36 MHz): A_{LP} = 0.8937 and $\Phi_{LP} = 0.0013°$.

Thus, closing the loop with a properly designed TUNER block would produce an overall loop gain $A_L = 1$ under ideal conditions. However, if the filter circuit contains real elements with parasitics and a realistic op-amp macromodel, the loop gain will *not* be unity—unless a suitable part of the network is modified in accordance with the Substitution Theorem. For this purpose, a closed-loop frequency analysis is performed with one element (in our case it's R5) being replaced by a voltage source V_Z (see the figure, again). Furthermore, to be realistic, standard element values are used (as given above in brackets) together with a parasitic capacitance of 0.5 pF across all resistors. Resulting from this analysis, the current-to-voltage ratio I_Z/V_Z at $f_Z = f_P$ gives a complex conductance to be utilized in place of R5, which can be realized by two parallel parameters:

$$R5^* = V_Z/RE(I_Z) = 13.47\ \Omega$$

and

$$C5^* = IMG(I_Z)/(2\pi f_P V_Z) = 28.7\ pF$$

Note that many graphical postprocessors have computational capabilities for displaying these simulation results directly with the aid of appropriate macro expressions (e.g., PSpice/Probe).

Hint: As an alternative, running the simulation at one frequency only (f_P) and stepping through a restricted C2 value range (e.g., ±50%) is recommended. In this case, C5* and R5* can be directly displayed as a function of C2, and it turns out that C5* = 0 and R5* = 16.9 Ω for C2* = 75.6 pF. Thus, no extra element C5* is required for compensating circuit imperfections.

A final simulation run using these values for C2* and R5* confirms that the dominant pole-pair of the filter circuit is shifted (i.e. "tuned") closely to the specified position *(see the table, last row)*.

References:

1. Blake, K., Application Note OA-29 "Low-Sensitivity Bandpass Filter Design with Tuning Method," National Semiconductor Corp., Oct. 1996.

2. Desoer, C.A., and Kuh, E.S., *Basic Circuit Theory*, McGraw-Hill International Edition, 1969, Chapter 16.

Circle 521

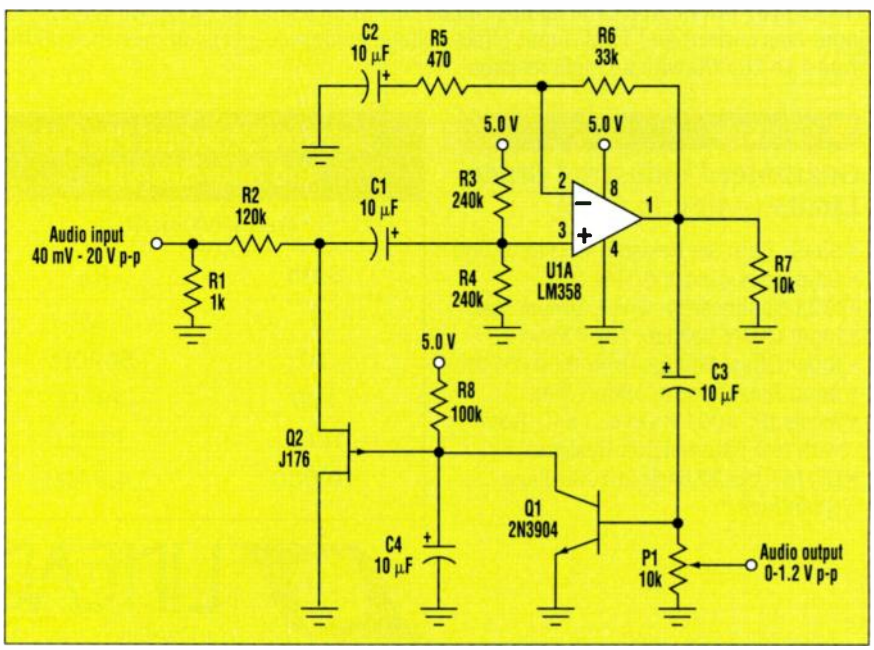
Effective AGC Amplifier Can Be Built At A Nominal Cost

JOSEPH P. GEORGE
New Venture Prototypes, 20082 Moontide Circle, Huntington Beach, CA 92646; (714) 968-2476.

Using the circuit presented here, you can construct a very inexpensive AGC amplifier with the following features: a dynamic range greater than 50 dB; negligible distortion to the output waveform; fast attack and slow decay; an adjustable output level from 0 to 1.2 V p-p; operation from a single 5-V supply; less than 1-mA current drain; and low cost (uses one half of a dual 8-pin op-amp package at less than $2.50 in parts). Better yet, if you need a second channel, the remaining half of the op amp can be used for that circuit.

Referring to the diagram, Q2 (a P-channel JFET), coupled with R2 and the equivalent resistance of R3 and R4, form a voltage divider to the input signal source. With input levels below 40 mV p-p, the input is evenly divided between R2 (120k) and R3 || R4 (120k). The output amplitude of U1A isn't large enough to turn on Q2, which acts as a positive peak detector. The gate of the JFET is pulled to +5 V, pinching its channel off and creating a very high resistance from drain to source. This essentially removes it from the circuit.

At input levels above 40 mV p-p, Q1 is turned on at the positive peaks of the output of U1A, lowering the JFETs gate to source voltage. The channel resistance decreases and attenuates the input signal to maintain the output of U1A at approximately 1.2 V p-p.



This inexpensive, yet effective, AGC amplifier has a dynamic range greater than 50 dB and is built using only half of an LM358 dual 8 pin op-amp package.

The circuit, as shown, was tested with a sine-wave input ranging from 300 Hz to 30 kHz at 40 mV to 20 V p-p, a 54-dB range. It maintained the output level at 1.2 V p-p, ±0.5 dB, with no visible distortion when comparing it with the input waveform. With a 40 mV to 20 V p-p input signal, the amplitude of the signal across the JFET (V_{DS}) measured less than 20 mV p-p.

Other JFETs with $V_{GS(OFF)}$ of 5V or under, such as the 2N5019 or 2N5116, should work equally well in this circuit, although they haven't been tried. To use JFETs with higher $V_{GS(OFF)}$, such as the 2N3993 (it was tried and worked equally well), increase the supply voltage to 12 V.

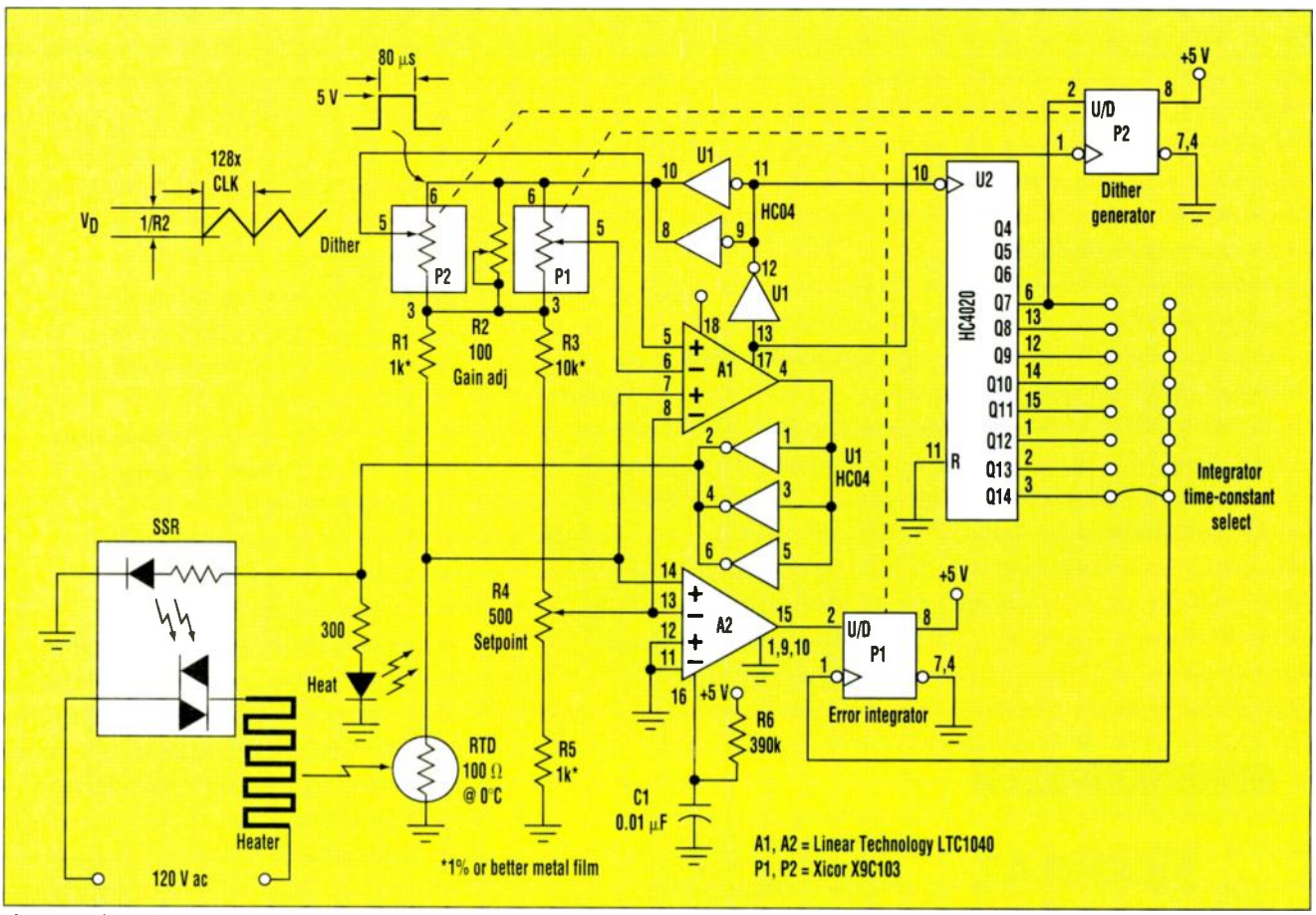
Circle 522

Hybrid Digital-Analog Proportional-Integral Temperature Controller

W. STEPHEN WOODWARD
Venable Hall, CB3290, University of North Carolina, Chapel Hill, NC 27599-3290; Internet: woodward@net.chem.unc.edu.

A classic scheme for precision temperature control is the proportional-integral or "P/I" algorithm. In this method, the heater control equation consists of two terms. One term ("P") is proportional to the instantaneous error differential between sensor and setpoint temperatures. The other ("I") is proportional to the time integral of the error. P/I controllers characteristically have reasonably good dynamic response due to the proportional feedback term, nominally zero steady-state error thanks to the error integration term, and relatively simple loop optimization because only three adjustments (setpoint, proportional gain, and integrator time-constant) are involved in the setup process.

The simplicity of the P/I feedback algorithm argues for a similarly simple analog-based controller design. But some temperature-control applications involve long time-constants (running to minutes and hours) and often must live in hostile (hot and contaminated) industrial environments. These gremlins



This controller achieves extended time constants without the delicate high-impedance analog circuits by using Xicor's X9C103 digitally-controlled potentiometers as feedback elements, combined with Linear Technology's LTC1040 sampled comparator.

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combine to make analog long-time-constant circuits problematic, with their high impedances and nano-ampere signal currents. This is so because nasty ambients exaggerate the leakage and bias currents of op amps, integrator capacitors, and even circuit boards.

The controller shown in the figure achieves adequate time-constants without the delicate high-impedance analog circuits. It uses Xicor's X9C103 digitally controlled potentiometers as feedback elements together with the Linear Technology LTC1040 sampled comparator.

Controller operation is based upon a positive-temperature-coefficient (3850 ppm/°C) platinum RTD sensor arranged in a standard ratiometric bridge with reference resistors R1, R3, and R5, and setpoint pot R4. Aiding controller stability and precision is high level (≈5 mA) bridge excitation. It produces a relatively large 1.7 mV/°C RTD output signal that competes well against noise pickup and thermal-EMF error sources. Typically, such a high RTD drive level would threaten to produce large and unacceptable sensor self-heating errors. But in this case, sensor excitation is pulsed (80 µs) under control of the LTC1040. This keeps average sensor dissipation duty factor low (≈1%) and self-heating error inconsequential.

On each measurement cycle, A1's lower input pair samples the bridge output. Depending on the result of the comparison, they tend to drive the pin 4 output bit to 0 or 1, as the bridge reports an RTD-setpoint differential that's negative or positive. Thus, the solid-state relay (SSR) and heater will most likely turn on when the temperature is low and off when it's high.

To make the resulting on/off heater drive have an average duty-factor that's nicely proportional to the magnitude of the temperature error signal and not just a simple "bang-bang" relationship, the bridge output voltage is summed with a triangular dither signal produced by P2. The combination of P2 and U2 causes P2 to output one full triangular dither waveform every 128 measurement cycles

Thermal inertia of the heater and the thermal load averages over the heater cycle rate (1 Hz in this example). Consequently, suitable selection of the R6-C1 oscillator RC will avoid significant temperature ripple. R2 adjusts the amplitude of the P2 dither signal and thereby sets the effective controller P-term gain that relates heater duty factor to temperature error to get adequate control loop "stiffness" without oscillation.

Meanwhile, error integrator A2 + P1 also samples the temperature difference signal. The integration sampling frequency, and therefore the integrator time constant, is set by the choice of which U2 output bit is connected to P1's clock. This arrangement causes the integrator to take one step in the direction of zero setpoint error every 1, 2, 4, 8, 16, 32, 64, or 128 heater dither cycles. As a result, it gradually converges on zero temperature error.

Selecting the right U2 bit sets the integrator time constant anywhere from one minute to more than two hours, and can thus accommodate even the longest generally encountered control-loop thermal time delays.

An I²C Fan For Personal Computers

JERRY STEELE
National Semiconductor Corp., Tucson Design Center,
6377 E. Tanque Verde Rd., Suite 101, Tucson, AZ 85715-3839;
(520) 751-2380; e-mail: jerry@galaxy.nsc.com.

The ultimate solution to elegant fan control and monitoring in the PC would be a cooling fan with an I²C or SMBus interface built in. However, this doesn't exist, at least not yet. A close emulation of this type of functionality can be achieved, though, by combining an LM81 hardware

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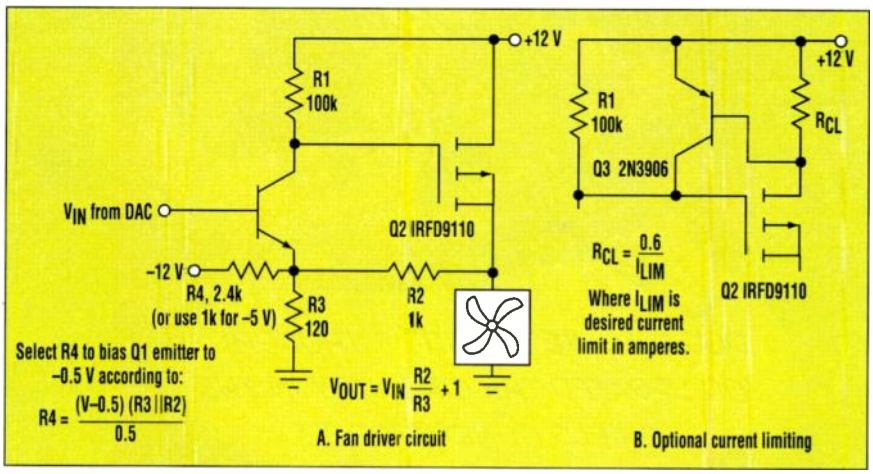

1. This fan driver circuit combines good saturation characteristics with the high-side drive necessary to preserve the fidelity of the fan tachometer outputs.

monitor IC with a cooling fan. This combination allows programming and monitoring of fan speed over the Serial Interface, as well as providing an Alarm output, particularly useful in SMBus environments. In addition, the LM81 can monitor the power supplies of both itself and the fan.

The LM81 provides a DAC for fan control. To drive a fan, simply amplify this signal with a circuit providing a low saturation voltage. To preserve the fidelity of the tachometer pulses from these fans, the fan voltage control must be performed on the high side of the fan rather than the ground side. These requirements are met by the topology of the fan drive circuit *(Fig. 1)*.

In the figure, R2 and R3 form a feedback network that provides the gain needed to boost the 0- to 1.2-V DAC output to a 0- to 12-V (less saturation) output. R4 biases Q1 into its linear region. R4 can optionally be returned to –5 V if a 1k resistor is used. Q2 doesn't incorporate any current limiting in the event the fan shorts, which often isn't a problem, because many 12-V supplies include current limiting.

Optional current limiting is shown in Figure 1b if needed. The IRFD9110 FET specified is one of several tested, and it's anticipated that this circuit will work satisfactorily with any FET chosen. At first glance it seems that stability and freedom from oscillation is a concern, but square-wave testing has shown plenty of phase margin on the circuit when tested with several fans.

Figure 2 depicts the complete I²C fan system along with an LM81 hardware monitor IC. The fan tachometer signal is returned to the LM81, which provides a count in an internal register that's inversely proportional to fan speed. The LM81 compares this value to a programmable threshold. If the limit is exceeded, it asserts the INT# output, which can then be connected to any available open-collector interrupt line or the SMBus Alert line.

Fans don't start reliably at reduced voltages, so when programming the DAC for slow fan speeds, the DAC should always be commanded to full output, then returned to the low speed value. Fans will have to be characterized for their functional operating range, which begins from 5 to 7 V. Avoid operating the fan in this "stalled" region by commanding the DAC to zero, because the fan will dissipate power without moving. The circuit in Figure 1 provides up to an 11.8-V output into a 200-mA fan.

IDEAS WANTED

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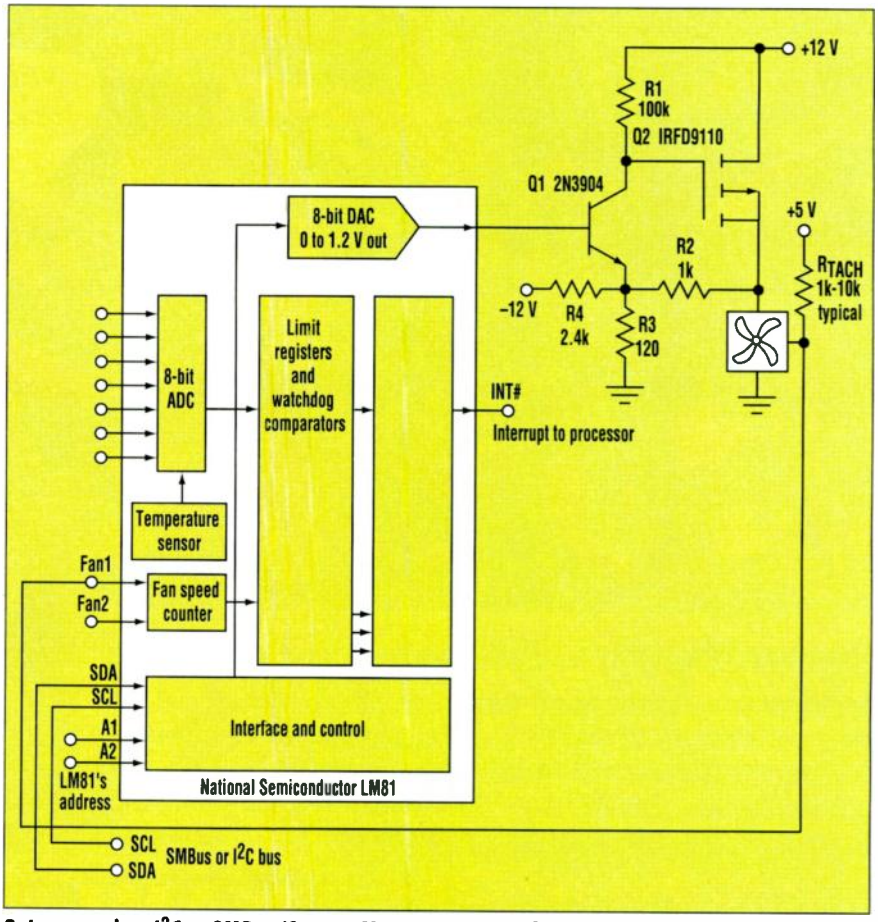

2. In a complete I²C or SMBus (System Management Bus) fan system, the LM81 hardware monitor provides the interface, fan control DAC, and tachometer counter.

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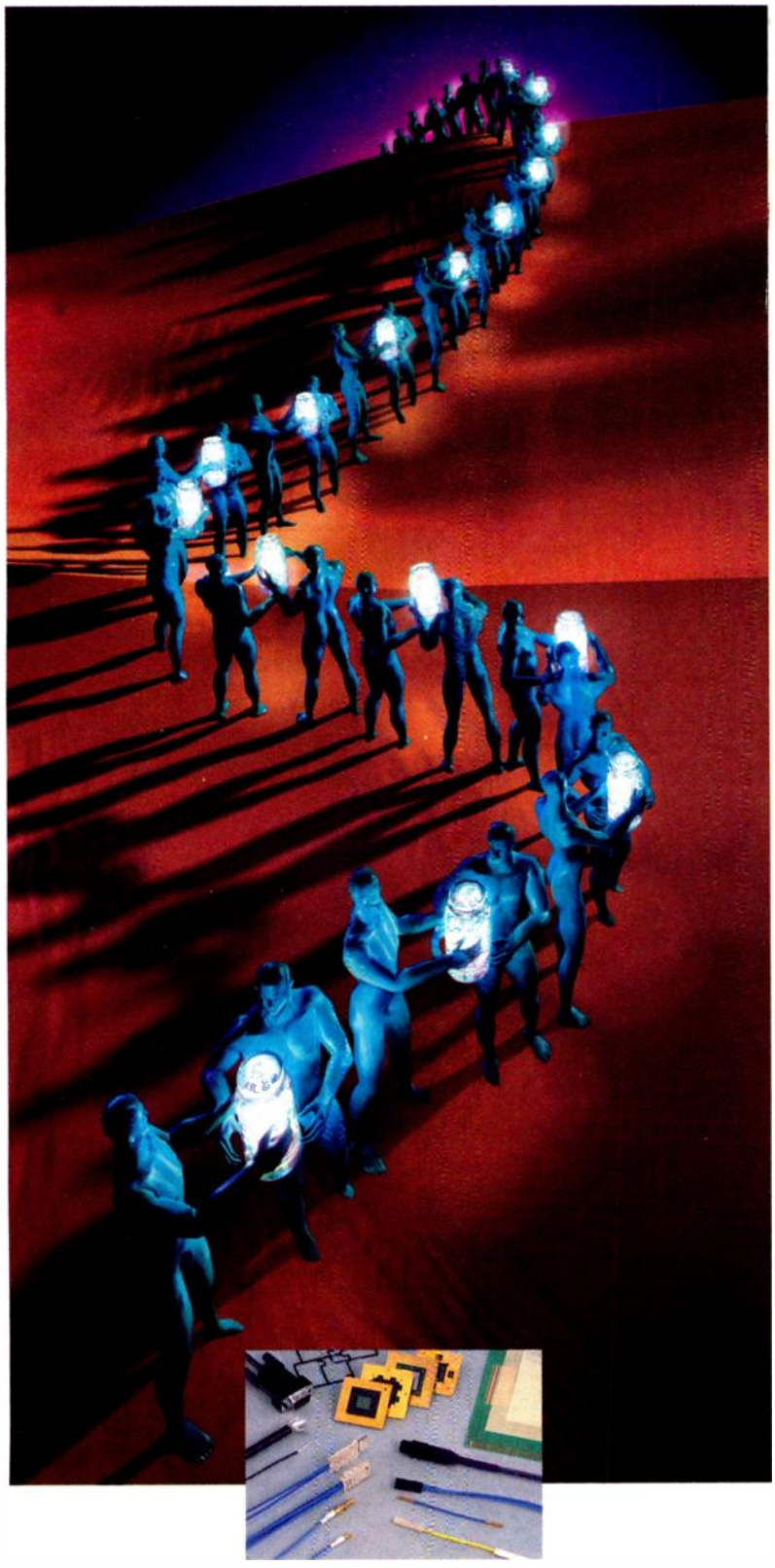

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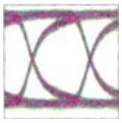

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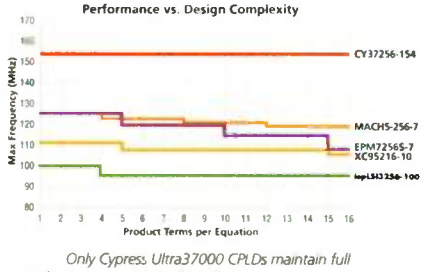

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CY37128	128	6.5	167	133	TQFP, PLCC
CY37192	192	7.5	154	125	TQFP, PLCC
CY37256	256	7.5	154	197	TQFP, PQFP BGA
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BOB PEASE

What's All This Circuits-In-Your-Car Stuff, Anyhow? (Part II)

Let's continue with some more of the circuits I am building to put in my newest car:

Burglar alarm, Mode IV: When the ignition is OFF, this circuit drives some brief, low-duty-cycle pulses through a couple of LEDs *(Fig. 3)*. You can use any low-power op amp you want. The overall battery drain is probably not enough to drain your battery in a month of disuse. I mount the LEDs near the lower corners of the windshield. These LEDs can also help you find your car in a dark parking lot. They stop blinking when you turn on the key.

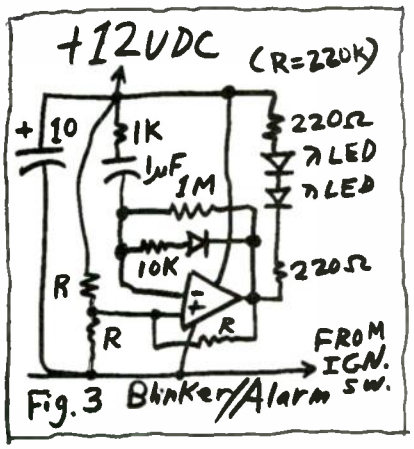
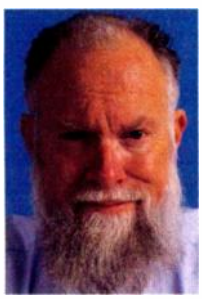


Fig. 3 Blinker/Alarm

Hand brake alarm: I am not going to put this on my new VW Beetle, because I never forget (or fail to notice) that I left my hand brake on. But, if I was setting up a VW Bus, I'd add that alarm. I would build a 400-Hz oscillator, and turn it on and off at about a 0.5-Hz rate *(Fig. 4)*.



BOB PEASE OBTAINED A BSEE FROM MIT IN 1961 AND IS STAFF SCIENTIST AT NATIONAL SEMICONDUCTOR CORP., SANTA CLARA, CALIF.

I'd couple this signal into my radio's speakers, perhaps through 150 Ω, so it would not be too loud or annoying—just in case I want to leave my hand brake on. This can prevent you from burning out your hand brake.

Of course, if you already have a warning light, you might not have to build it. But, if the warning light is not sufficient, an additional beeper might be helpful.

Horn modulator : I received a nice letter from a guy who had read my column on Reflex Response, where I was trying to warn a dog to get out of the high-speed lane. He explained that if you REALLY want your horn to work well, and get the warning across to a dog or a person—chop it at 4 Hz. I asked, "Won't it work better at 2 Hz?" He said, "No, 4 Hz." I will insert a horn chopper, so I can modulate the horn at 4 or 2 Hz. Of course, I will leave the wires set up so I can disable it, and leave the horn in a dc mode. I'll share this circuit with you in a future column.

Oil-temperature gauge: Am I going to wire up an oil-temperature gauge? Probably. It is pretty easy to tack-solder an LM35H to a piece of copper-clad, and slide that down the dip-stick hole. I did this once, 20 years ago. Not a big deal. I know my oil temperature gets up to 85° C, in a while. I don't really have to do this, but I guess I will. And, if the LM35 falls off because the solder melts, I'll know the oil temperature got too hot.

Tachometer: Am I going to put in a tachometer? No. I did that 30 years ago. It used a 2.6-V mercury cell, and every time the engine turned faster, the tachometer indicated that it was happening. When the engine was off, there was no drain from the battery. It ran fine for years, and then I quit running it.

I used to have an old Heathkit CD ignition module. It probably did give slightly longer life on accurate ignition timing. One of these days, I might get around to trouble-shooting it, but it quit working a few years ago, and I've done just fine without it.

Those are all the circuits in my car, until next month. I've been trying to figure out how to get my GPS receiver linked up, because you can't just leave it on, and you can't just turn off the power. But I think I have a solution. Now, as I said at the start of all this, these are kind of *chicken-manure* circuits. And we will all agree these circuits are not very sophisticated. But it is what you *do with them*—how you interface them to the world—that makes them effective.

All for now. / Comments invited!
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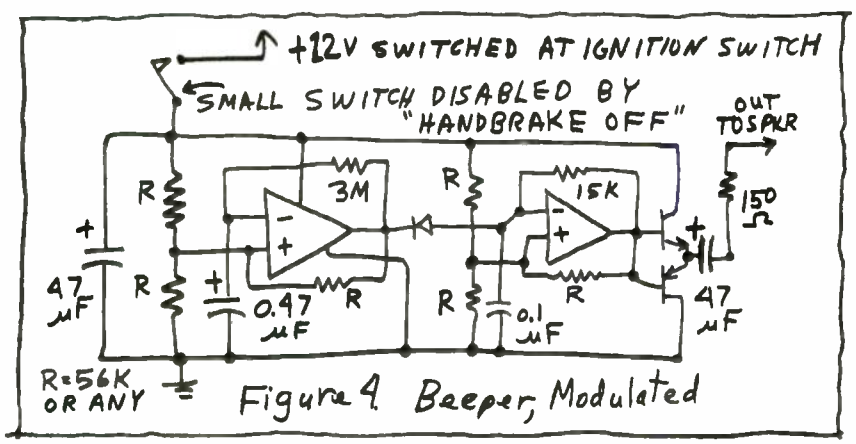

Figure 4 Beeper, Modulated

What's Best For Your PC?

Have You Considered Linux Vs. Windows?

In response to several readers' requests, this month we'll take a look at some of the pros and cons of engineering operations on a PC under alternative systems. One is the ubiquitous Windows operating system (OS), and the other is a UNIX-like alternative, Linux.

Linux, for those unfamiliar with the term, is basical ly a UNIX- compatible OS running on PC hardware. Thus, it has a fundamental advantage of being very low in total cost, as opposed to operating UNIX on a more traditional workstation. Linux supports AT and PCI bus structures, as well as standard CD-ROMs, floppy drives, hard disks, and many other peripherals, including a wide variety of video systems and monitors.

Written originally by Linus Torvalds, Linux is essentially an *open-standard* operating system, with development work being done by a wide range of disassociated individuals. Source code, drivers, and utilities etc. are freely available under the GNU's not UNIX (GNU) licensing concept. See www.gnu.org and www.linux.org/info/gnu.html. For the broadest collection of both general and detailed Linux documentation, see sunsite.unc.edu/LDP/.

In essence, Linux is an OS developed by its users, which is available at little or no cost. Several companies offer Linux packages (called distributions), such as Red Hat, Caldera, etc. A general listing of CD-based and downloadable sources can be found at the web site: pardis.sas.upenn.edu/uncompressed.shtml/howto/Distribution-HOWTO.html.

Note that this scenario is in sharp contrast to an OS such as Microsoft's Windows 95, 98, or NT, which are proprietary, and thus *closed-standard*, for-profit systems. Both Windows and Linux utilize the same underlying PC hardware platform, but the ways in which they make use of it differ enormously. A related comparative discussion of Windows NT 4.0 and UNIX systems (including Linux) can be found at www.kirch.net/unix-nt.html. In addition, for some grassroots engineering opinions of Linux vs. Windows NT for EDA, see www.isdmag.com/Editorial/1998/CoverStory9807.html.

I asked a couple of Linux-advocate correspondents for their personal views on an engineering development system using Windows 95 vis-a-vis Linux, as well as the general utility of Linux. First, Gary Huntress of the Newport Naval Undersea Warfare Center, Newport, R.I., (who had written previously within the May 1 column) offered Linux's merits.

Here are my thoughts about Windows 95 vs. Linux on a PC platform for engineering applications:

There certainly is a general dissatisfaction with Windows 95. I personally do not consider it to be a stable platform. Protection faults occur often while running resource-intensive software (and nowadays, what software isn't resource intensive?). The fact that I must tip-toe around OS limitations isn't acceptable for useful product development.

WALT JUNG

Linux was rated the best operating system of the year by Info World: www.infoworld.com/cgi-bin/displayTC.pl?/97poy.win3.htm#linux, and the Linux user community in general received the award for best technical support: www.infoworld.com/cgi-bin/displayTC.pl?97poy.supp.htm.

That's all well and good, but are there really applications available for Linux? Yes! See www.linux.org/apps/applications.html. Great, but are there any electrical engineering applications available? Yes! SAL.KachinaTech.COM/Z/1/.

Ok, I'll get off my Linux soapbox. I think an article about Linux and how it relates to the engineering community would be great. A complete walk-through of how to install it might not be necessary, as it's actually quite easy. The hardest part is probably setting up partitions properly, the rest is usually handled by scripts.

I think an article about why one should install Linux would be super. Some users do it just to save money. I would rather not spend the money (~$1000.00) for Matlab when I can do almost everything I need to using the GNU equivalent, Octave. And when I need to, I run Matlab on a remote server, and export the display to my system using Xwindows.

To judge Linux's popularity, do an Alta Vista search for +Spice +Linux, +EDA +Linux , or +DSP +Linux.

Just to sum up, and possibly repeat myself, I haven't found anything that can't be done better, faster, and cheaper than under Linux. The biggest obstacle is the learning curve.

I also asked Arnim Littek of Digitech in New Zealand for similar comments, specifically addressing some Linux issues as follows:

"Arnim, I have reserved some space on the new machine for another OS, which could be Linux or something else. But, I simply don't want to get into a 'fiddly' something, where my CD-ROM (or anything else) stops working for lack of a proper driver. And, even after all of it is working, there aren't useful applications to run on the 'superior' system. The best OS in the world is useless without software which provides utility toward doing the desired work."

I have to agree, Linux takes time up front. Maybe on those grounds, its not for you. I can't judge that.

In my experience, drivers appear for Linux faster than they do for NT—even weird ones. Sometimes it takes a bit of looking, but they're almost always there. CD-ROMs are pretty passé, to use your example.

Agreed, one needs apps. That is (or should be) the primary reason to use a computer, not the OS. The OS should be transparent. What are your needs?

- *Word processing, "office suites"*
- *E-mail*
- *Signal analysis/simulation, analog or digital*
- *Schematic/pc board is still weakest, but..*
- *Math packages*

All of these exist in multifarious offerings. None are Microsoft software. Some are commercial packages with similar support and features to Microsoft-style packages, others are

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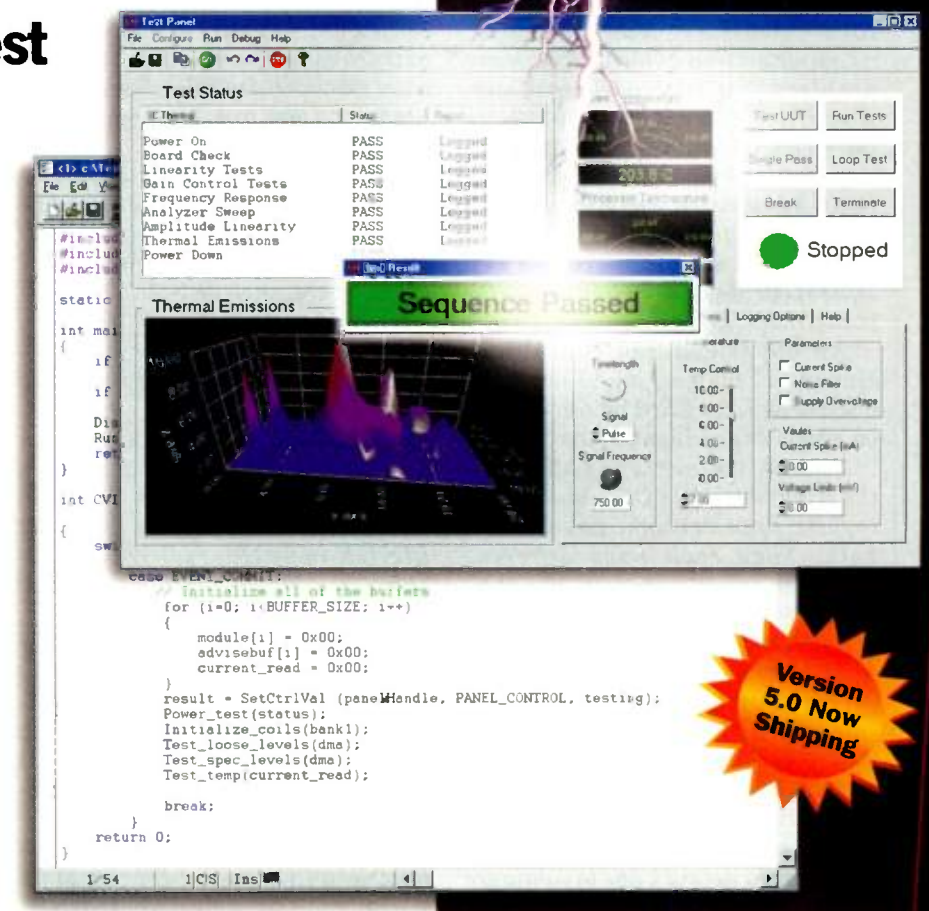

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more experimental and do more interesting things, with more attendant problems. In general, math and science packages abound.

The underlying strength of Linux, and the related open software movement, is that because so much is developed with source code widely available, one programmer's weaknesses are addressed by another's strengths. And, there is an active team of literally tens of thousands of people participating, around the clock in every time zone, because they are well motivated—they like what they're doing.

As for getting Linux going, there are also lots of other avenues of support. If you've got the time to sift, try the Usenet newsgroups: **comp.os.linux.announce** *(most highly recommended),* **comp.os.linux.networking**, **comp.os.linux.x**, *and a few others. I often get what I need from Usenet by a simple search on* **www.dejanews.com**, *definitely one of my favorite Web sites.*

An old friend and consultant, Hampton Childress, and I had been discussing Linux, and he commented on Windows and Linux systems:

Sounds like another adventure in the Windows/Linux OS wars is about to flare. I use 'em both, and need 'em both. They each have different strengths and weaknesses. The obvious strength of Windows is that it is supported by so many vendors, and has a common application (un)installer, aka InstallShield.

The forte of Linux is networking—an altogether different ball of wax. Linux allows, (ahem), persuades one to get close to the hardware and the low-level drivers. Anyone who has started up a network has to configure the ethx devices, ip masquerading/NAT, and, very importantly, security. Nothing substitutes for a strong firewall, and, I'm sorry to say, this takes a good deal of study. Ipfwadm has lots of power, and is used most effectively with subtle and imaginative scripting.

You've chosen wisely by going with a Red Hat 5.0 distribution, as that's probably easiest for a UNIX novice to get up and running. Sun Solaris is also pretty user friendly for network administration, but I'm not sure if it comes with a GNU license.

As you get into this more deeply, you'll appreciate Red Hat's RPM (Red Hat Package Manager) install/uninstall scheme. Many applications distributed as tarballs don't have a "make uninstall." So, if you really want to be thorough in cleaning out an oldie, you have to look at the original Makefile to see where things went.

This isn't all bad news. One great strength of Linux (from the perspective of a Windows user) is that apps generally don't affect one another when they are installed (unlike Windows 95.) The only problems I've encountered are the occasional necessity to upgrade a library to compile a new app, and some issue involving dependencies to the old libraries. These aren't always so obvious to resolve.

Of course, being free is a great attraction too! Still, there are some fine commercial apps available—WordPerfect, Corel Draw, Maple V. Some of the finest, such as Spice, are still free, and one doesn't need WordPerfect if you're comfortable with, say XEmacs. Another long learning curve... <sigh>

So, given all of this background, I first got myself a Linux book with a CD. Initially, I chose a Ball and Smoogen work, *Teach Yourself LINUX in 24 Hours*, ISBN 0-672-31162-3, $24.99 from SAMS: **www.mcp.com/mcp_publishers/sams**.

Later on I also acquired *Linux: The Complete Reference, 2nd Ed.*, by Richard Peterson, ISBN 0-07-882461-3, $49.99 from Osborne/McGraw-Hill, **www.osborne.com**. This one comes with a CD including Caldera's OpenLinux distribution, **www.caldera.com**.

Hampton had recommended to me *Running Linux, 2nd Ed.*, by Matt Welsh and Lar Kaufman, ISBN 1-56592-151-8, $29.95, published by O'Reilly and Associates, **www.oreilly.com**, which I also obtained. All three books are helpful, but differ in their scope and style. The *Teach Yourself LINUX...* book comes with Red Hat Software's version 5.0 Linux CD, **www.redhat.com**, the primary reason I selected it.

With just this single purchase, you have the potential of getting a Linux system going, but I hasten to add that you won't learn *everything* you'll need in just 24 hours. This one's better used as a "getting-started" book, and you should have at least one more for general reference. A (minor) caveat on this $24.99 book/CD combo is that one shouldn't expect support from Red Hat on this particular item. They do offer 90-day support on the current, full 5.1 release, priced at $49.95. Red Hat also has a free e-mail listserver as support; if you sign up for it, expect about 100 messages a day. But, potential Linux users should be aware that among the best support sources are the aforementioned newsgroups.

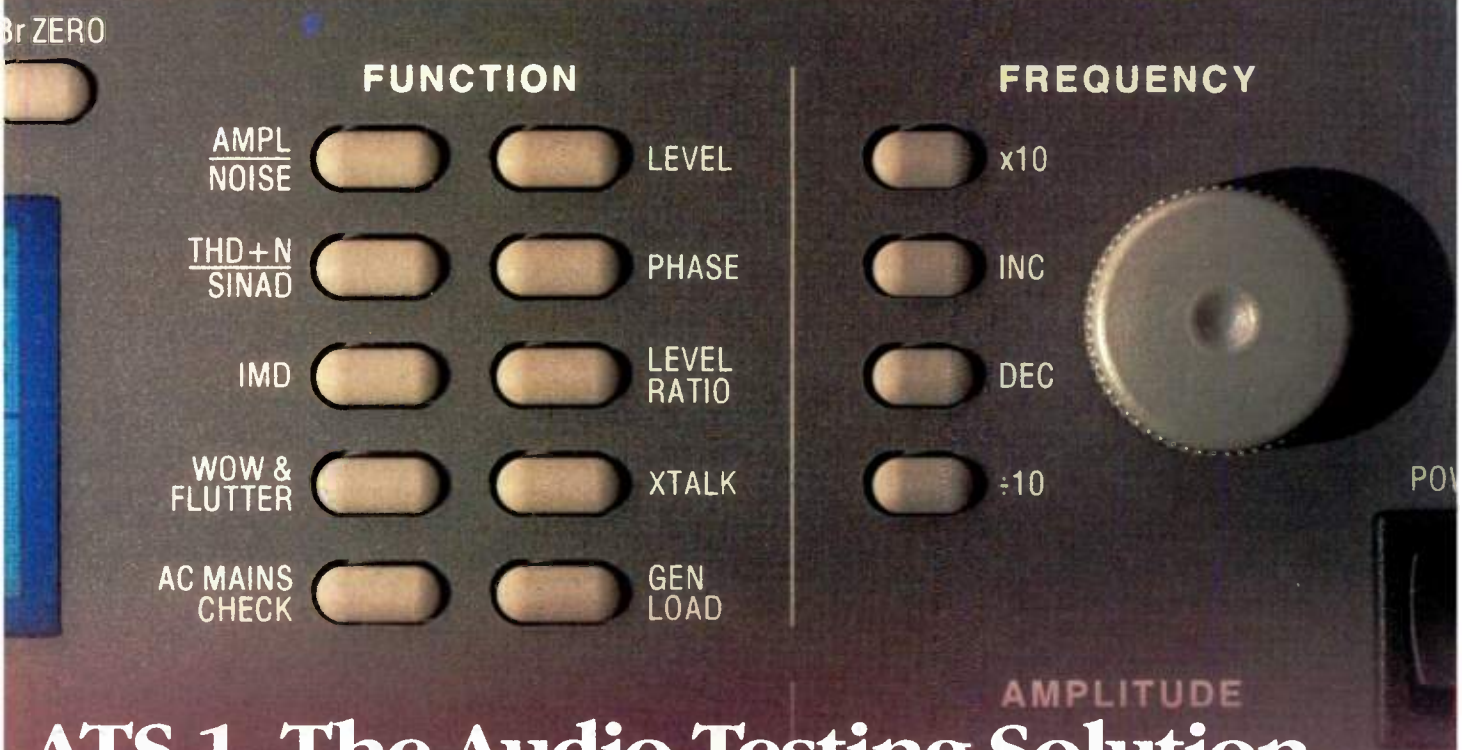
TIP: This is an appropriate point to note that a good source for these books and CDs is **www.cheapbytes.com**. You can also download Linux from the Net, but note that this route likely won't be highly practical, unless you've got a very fast connection.

Getting Linux Going: Armed with the Red Hat CD, I set out to try Linux for myself, on the new Micron Pentium II machine, using the *Teach Yourself LINUX...* as my installation guide. I first set up an ample (1.5-Gigabyte), dedicated hard-disk partition for Linux, with the use of Partition Magic, **www.powerquest.com**, which allows dynamic partition resizing. While this step of using Partition Magic in the partitioning setup isn't absolutely necessary, I'd still recommend it for ease-of-use, plus the fact that it comes with a useful boot manager, good for multibooting between Linux and Windows 95/DOS (or other OSs).

The Red Hat 5.0 installation went smoothly, although I did need to rerun it a couple of times, to get some settings correct. I was then able to selectively boot either Windows 95 or Linux in a just few hours.

The Linux setup wasn't 100% operational at first however, as I was forced to install a plain-vanilla VGA video driver for use with the Xwindows manager. This happened because the Micron's AGP video card (a Diamond Viper 330) used a new chip, an NVidia Riva 128. Both Arnim and Hampton pointed to a relatively new video server from S.u.S.e., **www.suse.com/**, which supported this device. After some digging and scratching around with the new driver, I was able to get full-capability, higher-resolution video working for my card.

Another fairly sticky hurdle was getting dialup PPP communication going via CompuServe as an ISP.



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But, this was also conquered with some timely info from the CompuServe UNIX forum, and some appropriate edits to the Red Hat default installation PPP script files. All in all, some fairly involved hacking, but not anything that any computer-literate engineer couldn't do, armed with a "can-do" attitude. But, don't expect a point-and-click process—that it isn't!

Generally, I'm highly impressed with number of ready-to-go programs that accompany the Red Hat installation. Another plus is that almost every hardware item on my PC, i.e., floppy disk, ZIP disk, two hard drives, a tape unit, and the aforementioned video system is supported. Alas, Linux did not recognize the plug-n-play modem, and I had to use another.

As of this writing, my Linux setup operates consistently, and the entire working time from unwrapping the CD to chasing down drivers and PPP debugging only took a few days. Very helpful here was reading the Usenet newsgroup, *comp.os.linux.setup*. And, I also appreciated the specific comments of Linux veterans Gary Huntress, Arnim Littek, and Hampton Childress, as well as those from Steve Reine and Scott Wurcer of ADI.

As for doing real, day-to-day engineering work under Linux, that report will need to come later, when things fully settle down. Overall, my PC needs are dominated by standard office tasks such as word processing, etc., so I will likely continue to use Windows 9x (or NT) indefinitely. But, as Gary so enthusiastically notes above, there are many engineering tasks that Linux can host extremely well, and therefore, could be a springboard for some readers out there. It should be interesting to see how Linux penetrates into uses within the engineering community over the months ahead.

That's it for another column. Enjoy Linux's tools, and stay in touch, especially with comments on alternative OS pros and cons.

Walt Jung is a corporate staff applications engineer for Analog Devices, Norwood, Mass. A long-time contributor to ELECTRONIC DESIGN, he can be reached via e-mail at: Walt_Jung @CSI.com.

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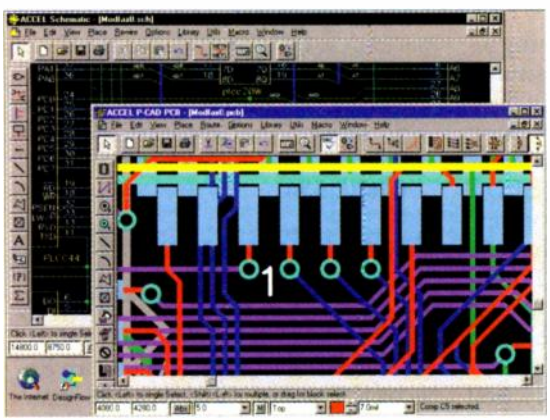

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Asynchronous Buck Controller Packs Two Switchers On-Chip

Designed to power processor core (V_{CORE}) and I/O circuitry (V_{IO}) on Pentium motherboards, Cherry Semiconductor Corp.'s CS-5127 is a fixed frequency dual output asynchronous buck controller that incorporates two switching regulators on one chip. Each output channel comprises a high gain error amplifier, a comparator, latch, and a totem-pole output driver that can supply a dc current of 100 mA (500 mA peak) to external n-channel power MOSFETs. Though independent, the two regulators share a common programmable oscillator that sets the operating frequency. There's also a sync pin for parallel supply operation or synchronization of the oscillator with other controllers. When not required, an enable feature shuts down one of the regulators to conserve power.

The controller implements proprietary V^2 architecture to attain fast transient loop response of 100 ns with tightly regulated outputs. According to the data sheets, typical load regulation is 15 mV and typical line regulation is 1 mV. The two separate control loops of the V^2 architecture enable this type of fast transient response, according to Cherry Semiconductor. Other features include two undervoltage lockouts, programmable soft start, and an on-chip 5-V reference for external circuits. The undervoltage lockouts keep the dual outputs turned off until both the input and reference voltages have reached a minimum value.

A single controller is able to create dual output dc-dc converters for Pentium processors with MMX capability. Thus, one of the CS-5127's channels delivers 2.8 V at 7 A for the processor core, while the other offers 3.3 V at 7 A for the I/O circuitry. The input voltage range for the device is 9.4 to 25.0 V. It comes in a plastic 16-lead SOIC package, and is priced at $1.90 in 1000-piece quantities.

Cherry Semiconductor
2000 South County Trail
East Greenwich, RI 02818-1530
(401) 886-3841
www.cherry-semi.com
CIRCLE 553
ASHOK BINDRA

Quad Analog Switch Shows Versatility

The MAX4613 is a quad, single-pole/single-throw (SPST) analog switch that has two normally closed switches and two normally open switches. It also can be configured as a quad SPST switch, two SPDT switches, or a single DPDT switch. Maximum turn-on time is less than 250 ns, while the turn-off time is 120 ns. The unit's maximum on-resistance is 85 Ω, which is matched to within 4 Ω (Max.) between the channels.

The switches conduct equally well in either direction, and consume only 35 µW while operating on a single +10 to +30 V or dual supplies of ±4.5 to ± 20 V. The device guarantees low charge injection and low off leakage current over the temperature range of less than 5 nA at +85 °C. It's capable of withstanding 2000 V minimum ESD per MIL-STD-883, method 3015.7.

According to Maxim, the MAX4613 is pin-compatible with industry-standard DG213. The digital inputs are TTL/CMOS-compatible. It's available in 16-pin QSOP, DIP, and TSSOP packages. In 1000 pieces, it carries a price tag of $1.05. AB

Maxim Integrated Products, 120 San Gabriel Dr., Sunnyvale, CA 94086: (408) 737-7600; www.maxim-ic.com.
CIRCLE 554

Analog I/O Mezzanine Offers 32-Channel A/D Conversion

The bitsi-ADC32 is a new analog I/O mezzanine developed by BittWare Research Systems. Featuring 32 channels of differential analog-to-digital conversion, the module is designed to give data-acquisition applications input flexibility without compromising I/O performance. The mezzanine supports programmable gains for each channel, and a maximum conversion rate of 100 kHz. Depending on the number of channels specified in the channel gain list, the bitsi-ADC32 pro-

(continued on page 108)

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(continued from page 106)

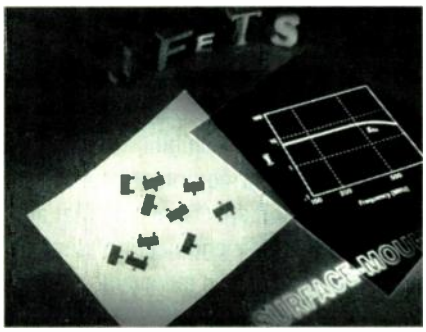
vides sampling rates from 6.25 to 100 kHz. In addition, the unit also features 32-bit digital I/O port, which provides an interface to external devices. Each of the 32 bits of digital I/O is individually configurable as input or output. According to BittWare Research, the bitsi-ADC32 I/O mezzanine is optimized to match the I/O capabilities of SHARC DSPs. The starting price for the bitsi-ADC32 is $1495. AB

***BittWare Research Systems**, 33 North Main St., Concord, NH 03301; (603) 226-0404; www.bittware.com.*

CIRCLE 555

JFETs Come in Surface-Mount SOT-23 Packages

Siliconix, a company of Vishay Intertechnology Inc., is offering five JFETs in smaller surface-mount SOT-23 packages. The new SOT-23 JFETs serve as alternatives to TO-92 packages. The five JFETs include two n-channel parts (SSTJ211/12) and three p-channel units (SST5460/61/62). The n-channel transistors feature low leakage current of 1 pA (typical), while the p-channel devices offer 3 pA. In addition, the JFETs provide low noise and low capacitance. For example, at 400 MHz, the n-channel parts offer a typical gain of 12 dB, while the noise is only 3 dB. Available in production quantities, the new JFETs in SOT-23 packages range in price from $0.15 to $0.45 in quantities of 100,000. AB



***Siliconix**, 2201 Laurelwood Rd., Santa Clara, CA 95054-1595; (408) 567-8220; www.siliconix.com.* **CIRCLE 556**

Stereo Audio DAC Fully Complies With USB Spec

Designed for next-generation multimedia PCs, a new stereo audio digital-to-analog converter is fully compliant with the Universal Serial Bus (USB) specification and provides digital audio playback. The DS4201 integrates a USB function core, a full-speed USB transceiver, a stereo 16-bit sigma-delta DAC, and digital signal processing. It takes the audio out of the CPU box and puts it in the speakers and multimedia monitors, resulting in much better sound. The single-chip digital audio device includes an on-chip analog mixer to support legacy analog audio technology and hybrid speaker designs. The DS4201 is available in a 28-pin DIP and 44-pin QFP. It's shipping now for $6.70 each in 1000-piece quantities. AB

***Dallas Semiconductor**, 4401 S. Beltwood Pkwy., Dallas, TX 75244-3292; (972) 371-4448; www.dalsemi.com.*

CIRCLE 557

EDA

Electromechanical Systems Design Targeted By EDA Tool

Transcendent Design Technology, a recent spinout from Synopsys' Viewlogic Systems Group, has now introduced a line of products targeted at the design and analysis of multiple domains within electromechanical systems. These products include TransCable, TransDatabook, and TransAnalysis.

The TransCable tool is the next generation of the net-based ViewCable product originally developed at Viewlogic Systems. It manages the electrical signal connectivity through physical components and enables electrical-connectivity checks and signal tracing through multilevel and multisheet electromechanical designs. It also drives physical design for manufacturing, provides a framework for analysis and simulation, and allows the automatic generation of manufacturing documentation (e.g., bill of materials, wire lists).

As a wire-based. as opposed to a net-based, capture tool, TransCable allows designers to intuitively create the interconnection of physical design objects accurately and quickly. Integrated into multiple design domains, the tool can, for example, interface to standard HDL simulators and/or to mixed analog/digital simulators for behavioral simulation. It can just as easily interface with TransAnalysis SI and TransAnalysis EMI for electromagnetic analysis, or Catia's 3D electrical design environment (E3D) and SDRC's Harness Design Product for mechanical design systems.

The TransDatabook tool is a parts library management system that can be easily synchronized with a company's existing parts information system. Once in place, it can be used to maintain and update parts lists, or browse according to specified criteria, such as parts attributes. Customized searches of the database also can be performed.

TransAnalysis is a suite of signal integrity and electromagnetic analysis products—TransAnalysis SI and TransAnalysis EMI—designed to identify signal integrity problems and verify compliance to EMI standards. The TransAnalysis SI tool calculates the electrical parameters of multiconductor configurations and simulates the inter-conductor coupling generated in complex systems. It also predicts system-level noise and interconnects prior to prototype fabrication. The TransAnalysis EMI tool simulates EMI radiation using advanced algorithms to accurately determine radiation from all nets in a structure.Furthermore, it supports "what-if" analysis.

The TransCable product will be available for $19,995. Its optional TransDatabook upgrade will sell for $4995. The TransAnalysis SI is priced at $24,995 and will be available in the third quarter of this year. TransAnalysis EMI, an optional upgrade to TransAnalysis SI, also is priced at $24,995. All products will be available on both UNIX and Windows NT platforms. CA

Transcendent Design Technology Inc., *1383 Del Norte Rd., Camarillo, CA 93010; (805) 278-7185.* **CIRCLE 558**

PCB Tool Enables High-Speed Packaging Of Designs

Interconnecting bare die into packages and onto pc boards has become increasingly difficult, causing even the most well-designed ASIC to fail if not adequately supported on a pc board. The recently introduced PowerBGA tool addresses this problem by offering designers a complete integrated solution that can meet the demand for more complex designs. The tool, which supports the design of BGAs, chip-scale packages, laminate-based MCMs, and chips on-board, works by automating the interconnect process between bare die and a pc board.

This solution offers a number of key features to help designers meet the requirements of high-speed advanced packaging, such as the ability to automatically produce wire bond diagrams. An Advanced Packaging Toolbox included in the Layout Editor contains functions specific to chip package design and common commands required to complete a design.

A Component IQ scans and stores die data, including chip size; bond pad locations; and pin, pad, and signal names. It also highlights component versus die discrepancies early in the design process. In doing so it can prevent errors and costly redesign. A

(continued on page 110)

(continued from page 109)
Netlist IQ accepts multiple schematic formats for input into PowerBGA and manages the interconnect differences between the packaged and bare versions of the die. Another capability, the Library IQ, automatically creates wire bond finger patterns based on input from the Component IQ and Netlist IQ, as well as wire-bond design rules. Placement is optimized based on logical connections and bond pads internally connected within the manufacturer's package.

The PowerBGA will be available in the fourth quarter of this year and, depending on the tools configuration, will cost $15,000 to $35,000. CA

***PADS Software Inc.**, 165 Forest St., Marlborough, MA 01752; (800) 554-7253 or (508) 485-4300; Internet: www.pads.com.* **CIRCLE 559**

Reuse Of Pre-DSM IP Made Easier

Though it's a valuable capability, reuse of pre-DSM (deep submicron) IP (intellectual property) has been nearly impossible to achieve due to the inability of linear shrink techniques to work properly at 0.35-µm geometries and below. The LACE tool that converts physical designs for reuse in SoCs (systems on a chip), coupled with newer DSM technologies, solved this problem by combining the predictability of hard IP while automatically optimizing it for a specific fab or technology.

The latest version, LACE 4.0, facilitates this process by offering faster, parallel conversions of hard IP using multiple workstations. It also maintains design hierarchy, improves technology file setup time, and includes a layout polygon editor for creating and editing layout for quick design-rule corrections and conversions known as LACEedit.

One of the prime features of LACE 4.0 is its hierarchical compaction capability, which allows it to hierarchically convert hard IP independent of the original design environment and the original process technology. An intelligent interprocess control algorithm is used to distribute a design over a local-area network (LAN). Then a multilevel hierarchy design conversion is run in parallel, converting hard macros and hard cores as well as hard IP like RAM, ROM, DRAM, datapaths, and microprocessors. The converted design, which is still hierarchical, can again be simulated and verified on a higher design level to shorten simulation and verification time.

As an added benefit, LACE 4.0 comes with predefined conversion and optimization templates that allow even the novice designer to easily use the tool. The available templates cover most of conversion tasks for compaction, optimization, design-rule correction, and increased performance, and can reduce the initial setup time up to 80% for an average technology conversion. Available for UNIX and Linux users on SUN, HP, and Pentium workstations, LACE 4.0 will be available in September 1998. Its starting price is $50,000. CA.

***Rubicad Corp.**, 1150 North First St., Suite 130, San Jose, CA 95112; (408) 995-3334; info@rubicad.com.*

CIRCLE 560

POWER

60-W Converters Come In Compact Format

Designated the MWA60 series, these 60-W dc-dc converters come in packages measuring 3.94 by 2.76 by 0.71 in. and take inputs of 9 to 18 V, 18 to 36 V, or 36 to 72 V. The converters are available in single-, dual-, or triple-output versions, with outputs of 3.3, 5, 12, or 15 V (single), or ±15, ±12, ±15 V (dual), or 3.3/±15, 5/±12, 5/±15 V (triple). The efficiency is 85% and the line and load regulations are ±0.5% (single) or ±1% (dual). Protection consists of output overvoltage and overcurrent, an isolation voltage of 1600 V dc, and an isolation resistance of 10^9 Ω. Pricing for the converters is $58 each per 1000; delivery is four to six weeks. PM

Polytron Devices Inc., P.O. Box 398, Paterson, NJ 07544; Sheri Lynn (973) 345-5885; fax (973) 345-1264; e-mail: polytron@erols.com; Internet: www.polytrondevices.com.

CIRCLE 561

DC-DC Converters Meet Military Specifications

The MI Family of dc-dc converters is designed to accommodate military requirements for non-developmental items and commercial, off-the-shelf

equipment. The devices meet military specifications for input power noise (MIL-STD-704, 1275A, 1399A, DO-160C, and QSTAG-307), conducted noise (MIL-STD-461), severe environments (MIL-STD-810 and -202, and DEF-STAN 07-55), and component derating (NAVMAT-P-4855-1A). Available in versions ranging from 50 to 100 W, the dc-dc converters include optional EMI filtering; single, dual, or triple outputs; or output ripple attenuator modules. Pricing for a 100-W, I-grade module is $280. PM

Vicor Corp., 23 Frontage Rd., Andover, MA 01810; Vicor Express (800) 735-6200; fax (978) 475-6715; www.vicr.com. **CIRCLE 562**

4000-W PFC Supply Is Hot-Pluggable

Aimed at telecom, broadcast, and ATM applications, the Model PM33213B-5 4000-W power supply features both power-factor correction (0.99) and an isolated front end. Measuring 5 by 5 by 15.5 in., the supply weighs 15 lb., runs off 170 to 264 V ac, and outputs 24, 28, 32, or 48 V dc. Standard features include overvoltage, overcurrent, and overtemperature protection, remote sense, and self-contained forced-air cooling. The operating temperature range is 0° to 50°C at full load, and the MTBF is 250,000 hours. UL, CSA, and VDE safety standards have been met; CE marking is available upon request. Pricing is $1685 each per 100; delivery is six to eight weeks. PM

Pioneer Magnetics Inc., 1745 Berkeley St., Santa Monica, CA 90404; Param Panesar (310) 829-6751; fax (310) 453-3929; e-mail: pmimag@ix.netcom.com; www.pioneermag.com.

CIRCLE 563

Low-Voltage Power Modules Output Up To 32 A

The PT7770 Series of power modules, designated the Sledge Hammer, can be programmed via five-bit input to output voltages from 3.5 down to 1.3 V at a current of 32 A. With a PT7746 current booster, this current can jump to 64 A. Another PT7746 in parallel can boost the output to 96 A of regulated, low-voltage power. Featuring efficiencies approaching 90%, the power modules come with compensation for any power drop from the module to the load. A standby pin controls module operation. Pricing for the PT7770 is $44, while the PT7746 costs $41.50. PM

Power Trends, 27715 Diehl Rd., Warrenville, IL 60555; Don Matthiesen (800) 531-5782; fax (630) 393-6902; e-mail: dam@powertrends.com; Internet: www.powertrends.com.

CIRCLE 564

DIGITAL ICs

Single-Chip Core Engine Pushes 2D/3D Graphics And Video Accelerator To Greater Performance Levels

By combining 2D, 3D, and MPEG-2 video acceleration support onto a single chip, the Savage3D accelerator delivers a high-performance single-chip solution for desktop systems. Lying at the heart of the chip is a 128-bit graphics engine with trilinear filtering. The engine delivers single-cycle command execution for greater performance plus high image quality.

The accelerator is S3 Inc.'s first to use the firm's proprietary S3TC compression/decompression technology. Microsoft Corp. has endorsed the technology as the standard texture compression technique to be used in its DirectX software. Such a scheme is needed to handle a larger number of textures and higher triangle/s rates targeted for next-generation games and other applications.

The high quality texture compression possible with S3TC allows six times the amount of texture storage and AGP bus bandwidth. As a result, the Savage 3D chip can deliver vivid and realistic images through its color rendering. The chip can handle 16 million colors at 800-by-600-pixel resolution, versus 64 k colors with some other approaches. A proprietary dithering algorithm used by the engine provides smoother color transitions. Internally, the chip operates in the 24-bit mode and the control at the last stage determines the actual output. Also included on-chip is an advanced triangle setup engine that delivers industry-leading 3D performance that provides very realistic user experience.

The chip's 3D engine is designed to handle AGP texturing from system memory and provides many features for high-quality imaging—trilinear filtering, specular and diffuse shading, perspective correction, and fogging. Because it deals with data latencies, the 3D engine can handle worst-case AGP latency. It also incorporates a texture look-ahead capability that requests textures before they're needed, thus preventing engine stalls. The tile-based architecture of the engine maximizes memory size and minimizes page breaks in system memory.

An on-chip video acceleration support helps reduce CPU overhead for MPEG-2 playback from interactive DVD systems and video-conferencing applications. The accelerator performs the planar-to-packed format conversion and motion compensation tasks and includes an enhanced scaling algorithm to deliver high-quality full-screen video playback. The chip also supports multiple video windows and image mirroring, and a 60-MHz video port allows low-cost connections to standard MPEG-2 decoders and video digitizers.

As part of the video support, an on-chip streams processor provides stretching, filtering, and the YUV color-space conversion required for full-screen video playback, with both software codecs and hardware MPEG sources. It can simultaneously display graphics and video, each with different color depths as well as vertical interpolation and color controls. An integrated TV-out capability also sets new quality levels for flicker reduction, filtered overscan compensation, and NTSC/PAL encoding. The encoder, along with Macrovision support, enables TV outputs of composite or S-video signals, which can be fed to monitors, VCRs, or other video systems.

Designed to connect directly to an AGP 2X bus interface, the chip is optimized to operate with the 440LX/BX motherboard chip sets, but also can support the PCI 2.1 33-MHz bus interface. Other chip features are both a flash memory and IIC serial communications interface, as well as a 250-MHz RAMDAC with Gamma correction. Housed in a 256-contact plastic ball-grid-array package, the Savage3D sells for $35 each in lots of 10,000 units. Samples are available immediately.

S3 Inc.
P.O. Box 58058
Santa Clara, CA 95052-8058
(408) 588-8000
www.s3.com

CIRCLE 565

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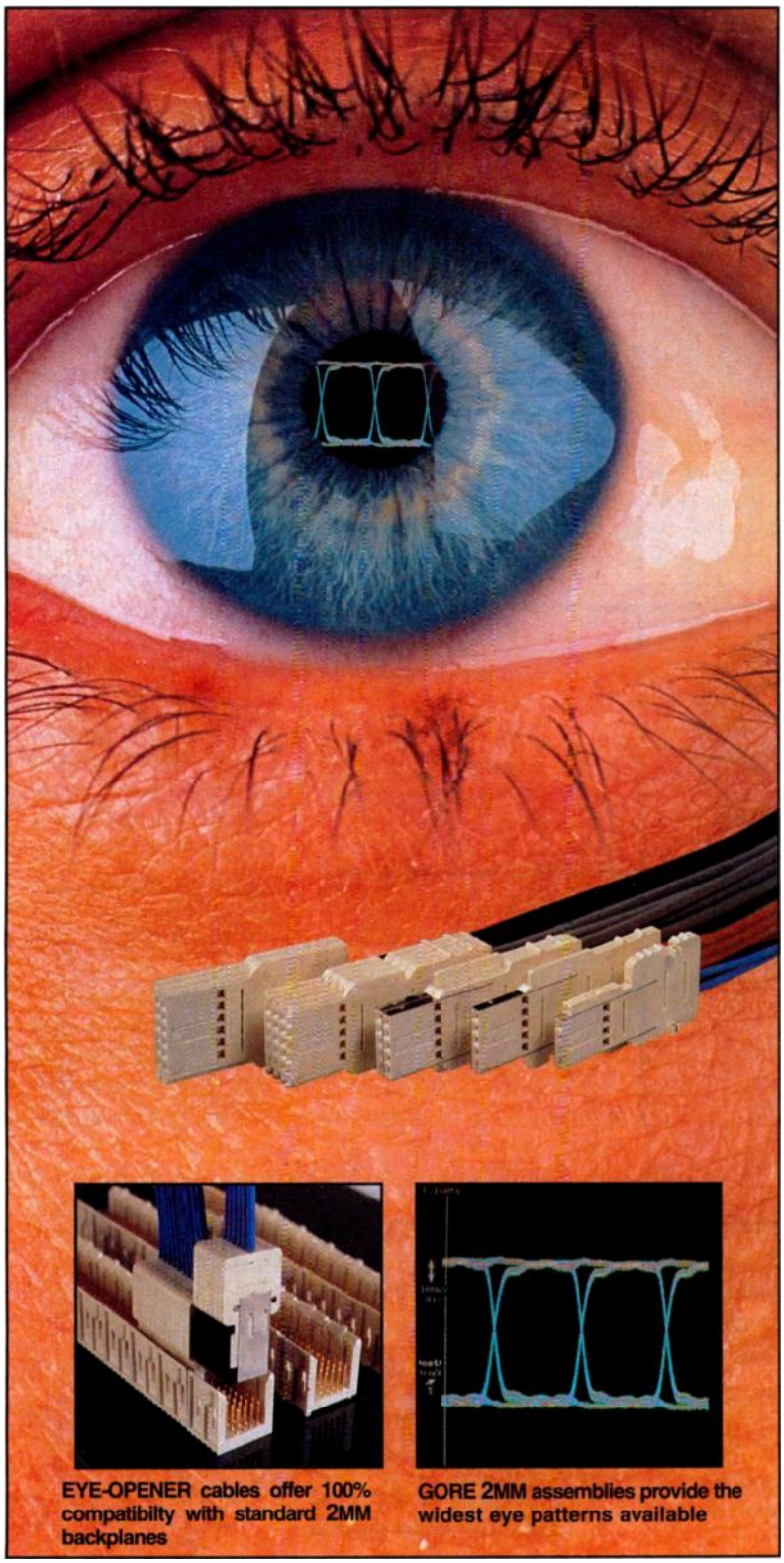

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Both Core and Protocol Specific Function (PSF) software modules are available. The Core product manages tasks, such as forced and controlled switchovers of the failed subsystem to the standby subsystem. Each PSF product is specific to a particular protocol layer and updates the internal states of the standby subsystem.

In its first release, the Core product and the related PSF products will support Application Part (TCAP) stack protocol layers for Signaling System 7 (SS7). Future releases will include PSF products for other SS7 layers and other protocol layers across its broad range of products, including Integrated Services Digital Networks (ISDNs), asynchronous transfer mode (ATM) and V5. The first release will be available this September. Licensing fees and other pricing available upon request. LG

Trillium Digital Systems Inc., *12100 Wilshire Blvd., Suite 1800, Los Angeles, CA 90025; (310) 442-9222; fax (310) 442-1162; www.trillium.com.*

CIRCLE 494

CDMA Chip And Reference Design Speed 2G/3G Cellular Products

The CDMA+ single-chip cellular baseband transceiver is a versatile platform that can support both current and future CDMA-based applications. Developers can use its associated reference development platform to quickly implement cost-effective IS-95-compliant handsets today and begin work on third-generation (3G) wideband CDMA products to meet the emerging IMT-2000 and cdmaOne standards.

The CDMA+ baseband processor incorporates a 50-MHz OAK DSP, a multispeed (16, 20, and 24 MHz) ARM RISC microcontroller, a dual-mode CDMA/AMPS modem, and an audio codec. It also contains all of the peripheral interface circuitry required to support a user interface.

The firmware-based solution includes QCELP and EVRC voice processing code for the DSP. The processor can be easily customized to support features like echo cancellation and voice recognition. The controller firmware includes type-approved protocol processing stacks that can be easily maintained and customized. Comprehensive development-tool support for both processors includes a development board, a debug toolkit, and a software suite that supports simultaneous development of code for both the DSP and controller on one JTAG port.

Additional development software and a complete reference design can be licensed from the third-party vendor, Dot Wireless. The complete, verified air-interface package includes hardware reference designs for the baseband, RF, and user interface sections, as well as complete operating software. The licensable design also includes a highly enhanced suite of software-development tools, which can speed design and customization.

Sampling now, with production slated for the first quarter of 1999, the CDMA+ processor comes in a 177-lead LQFP or a 180 FBPGA. Pricing will be under $20 in production quantities. The Dot Wireless reference development tools are available now. LG

VLSI Technology Inc., *1109 Mckay Dr., San Jose, CA 95131; (408) 434-3000; www.vlsi.com.* **CIRCLE 495**

Dot Wireless Inc., *6650 Lusk Blvd., Bldg B-103, San Diego, CA 92121-2774; (619) 678-0889; Internet: www.dotwireless.com.* **CIRCLE 496**

Advanced Mux/Demux Chips Cut Cost of 2.5-Gbit/s SONET/SDH

The VSC8161 and VSC8162, a next-generation physical-interface chip set for 2.5-Gbit/s SONET/SDH systems, should help reduce overall system cost of OC-48/STM-16 telecom systems. The two chips integrate all functions required to connect a CMOS system core to an optical network's laser modules. Integrated into the VSC8161 is a 2.5-Gbit/s clock multiplication unit, 16:1 multiplexer, and OC-48/STM-16 laser driver. The VSC8162 incorporates an OC-48/STM-16 clock and data recovery unit and 1:16 demultiplexer. Together, the two chips exceed Bellcore jitter specifications and can be used in DWDM systems, SONET/SDH terminal equipment, and SONET/SDH add/drop multiplexers.

The VSC8161 accepts 16 bits of parallel data at 155 Mbits/s and converts it to a serial data stream running at 2.5 Gbits/s. Its serial data stream is output through an on-chip laser driver circuit. Capable of sourcing 110 mA, The laser driver can interface directly to most laser diodes used in SONET/SDH applications.

The VSC8162 receives a 2.5-Gbit/s data stream, and uses the internal clock and data recovery unit to the data. It then deserializes the data and outputs it 16 bits wide at 155 Mbits/s. The on-chip clock-recovery unit lets users adjust for optimum placement of the recovered clock within the data eye and helps manufacturers overcome nonlinear effects inherent in optical transmission media. No external loop filter components are required for the analog clock multiplication and clock-recovery circuits. Parity calculation also is provided in both devices to verify data transfer to and from the low-speed parallel interface.

The VSC8161 and VSC8162 are available in 100- and 128-pin PQFPs, respectively. Volume production is scheduled for September. Pricing is $198 for the VSC8161 and $158 for the VSC8162 in 1000 unit quantities. LG

Vitesse Semiconductor Corp., *741 Calle Plano, Camarillo, CA 93012; (805) 388-3700; fax (805) 987-5896; www.vitesse.com.* **CIRCLE 497**

LAN Switch Chips Cut Cost Of 10/100 and Gig Ethernet Apps

The TNETX4090 ThunderSWITCH II and its associated Ethernet, Fast Ethernet, and Gigabit PHY-layer devices will enable network equipment manufacturers to develop high-performance desktop switches below $35 per

(continued on page 117)

Low-Power Design

Center Suisse d'Electronique et de Microtechnique SA & Electronic Design

This collection of papers focusing on the minimization of power consumption features general tutorials, digital circuits, devices and analog circuits of low-power systems.

Softcover book, $125.00, Item B4023PM

Portable by Design, Proceedings of the Fifth Annual Conference

Electronic Design

In an industry that is constantly changing from year to year, this 1998 conference overview features the latest developments on topics such as: Rechargeable Batteries, CPU's and DPU's for Portable Devices, Portable-System Software Issues, Infrared Data, Architectural Issues, Packaging Concerns, plus many other features relavant to those working inthe field of portable design. Held February 9-12, 1998 in Santa Clara, CA.

Softcover book, $175.00, Item P9014PM

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(continued from page 115)
Fast Ethernet port. The ThunderSWITCH II offers eight 10-/100-Mbit ports and one 100-Mbit/1-Gbit uplink port for fast connections to high-capacity backbones. It uses RDRAM, which provides performance and cost advantages over SDRAM-based solutions. The cascadable switch chip has 4 Gbits of memory bandwidth and 6 Gbits of internal switching bandwidth, enabling OEMs to develop ultra-high-performance non-blocking switches of varying port densities.

A complete switching solution can be constructed quickly using the switch's corresponding physical-layer devices. The TNETE2008 is a PHY-layer device that supports eight 10-Mbit ports. The TNETE2101 is a single-channel 10/100 PHY, and the TNETE2201 is a single-channel gigabit transceiver. A complete reference design and software/hardware development system are available.

The TNETX4090 will be delivered in a 352 BGA package. Samples are scheduled for July, with volume production scheduled for the third quarter of this year. Pricing is $90 per unit in quantities of 10,000.

All three PHY devices are in production now. In quantities of 10,000 units. The TNETE2008 comes in a 120-pin QFP and costs costs $10; the TNETE2101 comes in a 64-pin thin QFP and costs $5.75; and the TNETE2201 is housed a 100-pin TQFP and costs $13 each. LG

***Texas Instruments Inc.**, Semiconductor Group, SC-98056, P.O. Box 172228, Denver, CO 80217; (800) 477-8924, ext. 4500; www.ti.com/sc/docs/network/nbuhomex.htm.* **CIRCLE 498**

Multirate Data Pump For Pair Gain, xDSL At T1/E1 Speeds

The SK70725 DSP and SK70721 AFE comprise an enhanced MDSL Data Pump (EMDP) chip set that offers increased flexibility for IP, ATM, and voice, as well as better performance in long-distance applications. It's intended for use as a data pump for Internet access equipment, fractional or full T1/E1 transport systems, digital pair-gain systems, and wireless base station access systems. It supports data rates from 272 to 1168 kbits/s.

The chip set is a variable-rate transceiver that provides symmetric full-duplex communication on one twisted wire pair using a 2B1Q line code with echo-cancellation. The SK70725 incorporates all of the DSP required for analog-to-digital conversion, echo-cancellation, data scrambling, and adaptive equalization, as well as transceiver activation state-machine control. The SK70721 includes a DAC, filters, and transmit line drivers. Thanks to the DSP's embedded controller code, no external microcontroller chip is needed.

The data pump provides multiple framing modes, including transparent, ANSI T1 standard, and ETSI E1 standard. Its analog front end achieves greater performance over long loops in low-noise environments by widening the dynamic range and modifying the chip's digital gain-control algorithm.

The SK70725 Enhanced MDSL DSP and SK70721 IAFE are packaged in 44- and 28-pin PLCCs, respectively. The MDSL data pump is now available in volume production and priced at under $25.76 in quantities of 1000. LG

***Level One Communications Inc.**, 9750 Goethe Rd., Sacramento, CA 95827; (916) 854-1155; e-mail: litreq@level1.com, ask for literature package LO1P007; www.level1.com.* **CIRCLE 499**

ATM SARs With PCI Bus For Telecom, Datacom, xDSL Apps

The IDT77252 and IDT77222 are the first of a new breed of low-cost, single-chip, 155-Mbit/s segmentation and reassembly (SAR) controllers that support the recently approved Available Bit Rate (ABR) protocol. This allows users to maximally utilize network bandwidth. In addition, both chips support the PCI 2.1 bus specifications and are designed to support PC'98 specifications, providing plug-and-play solutions for Windows-based networking applications. These ABR SARs implement ABR in a way that enables bandwidth optimization on a per-VC basis. This is more efficient than the industry standard, which optimizes bandwidth on a per-chip basis.

Both devices can interface directly to a PCI bus at clock rates of up to 33 MHz. The IDT77252 allows up to 16K open-transmit and receive connections. The IDT77222 supports only 256 connections, which reduces the local memory requirements. This solution is ideal for the fast-emerging, cost-conscious xDSL market that requires fewer virtual circuits. A full range of support is available for the new IDT77252, IDT77222, and the existing IDT77211 SAR controllers. Such tools includes reference designs, evaluation boards, and software for VxWorks, Windows and WindowsNT.

Both devices are sampling now and will be in full production during the third quarter of this year. Pricing for the IDT77252 is $41 each, while the IDT77222 goes for $20 each, both in 10,000-piece quantities. LG

***IDT Corp.**, 2975 Stender Way, Santa Clara, CA 95054, (408) 727-6116, (800) 345-7015; fax-back 800/9-IDT-FAX; www.idt.com.* **CIRCLE 500**

Software Modem Supports 56K And V.90 Standards, PCI Bus

Designed for use with the high-speed PCI bus, the HSP56 Modem supports both the ITU V.90 and K56FLEX 56-kbit/s standards in a highly compact, full-featured package. A combination of host-resident signal processing software and hardware interface electronics allows it to offer PC and modem OEMs 56K data, 14.4-kbit/s fax, and voice and speakerphone capabilities in an affordable package. The two-chip solution integrates a PCI bus interface, and the analog front end (AFE) electronics required to connect to a standard POTS line.

Because the new chip set supports 3.3-V operation and consumes only 125 mW—less than half the power required by other modem solutions—it's well-suited for battery-powered applications such as portable computers. The HSP56 Modem also will support PCI-based power-management features, such as On Now or sleep mode, as they become available. The HSP56 Modem is available now in a TQFP100 package with the PC-TEL part number of PCT789. The unit price is $30.00 in quantities of 10,000 pieces. LG

***PC-TEL Inc.**, 630 Alder Dr., Milpitas, Calif., 95035; (408) 383-0452; fax (408) 383-0455; www.pctel.com.* **CIRCLE 501**

ELECTRONIC DESIGN CATALOG/LITERATURE REVIEW

SMSC SHORT FORM CATALOG

SMSC, a world supplier of ICs and MEMS, has shipped over 100 million input/output (I/O) circuits and supplies ICs for PC connectivity, LANs and embedded control systems.

CIRCLE 248

SMSC

SLIDE SWITCHES

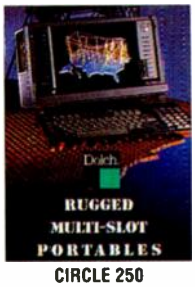
A/D Electronics' free Slide Switch catalog offers 46 pages of slide and side knob slide switches in different configurations. Design engineer can obtain complete specs, dimensional drawings and evaluation samples upon request. A/D Electronics also supplies a variety of interconnects for the OEM. Technical Support is available by contacting: A/D Electronics, (253) 851-8005; fax: (253) 858-9869; www.adelectroncics.com

CIRCLE 249

A/D ELECTRONICS

RUGGED PORTABLES

Dolch offers an ultra-rugged and environmentally protected system for any application with add-in expansion from one to ten slots, sunlight readable screens and CPUs to 400 MHz. e-mail: sales@dolch.com; web site: www.dolch.com



CIRCLE 250

DOLCH COMPUTER SYSTEMS INC.

Commercial & Medical Switching Catalog

Condor's 60-page catalog offers commercial and medical switching and linear D.C. power supplies. Commercial products meet latest international safety standards and medical products are certified to UL544, VDE0750 and IEC601. Call 800-235-5929, FAX (805) 487-8911. www.condorpower.com/~condordc

CIRCLE 251

CONDOR

THERMOCOUPLE MONITOR

The SR630 is a 16 channel thermocouple monitor for B, E, J, K, R, S, and T type thermocouples. Temperature can be read with 0.1 degree resolution, or each channel can monitor DC voltage with 1 mV resolution. Any and all channels can be scanned, and alarm limits can be set for monitoring and temperature deviation. RS-232 and GPIB (IEEE-488) computer interfaces as well as a Centronix printer port are standard.

CIRCLE 252

STANFORD RESEARCH SYSTEMS

MILLENIUM 2000

Introducing MIL-2000 the newest state of the art switching power supply. Featuring resonant pulse width modulation topology, up to 85% efficiency. From 1-7.5 kv, @1-10w in 2 sizes 50x60x5mm. Custom designing available. e-mail: ahv@ahv.com; website: www.ahv.com

CIRCLE 253

AMERICAN HIGH VOLTAGE

MELCHER 1998 DATA BOOK

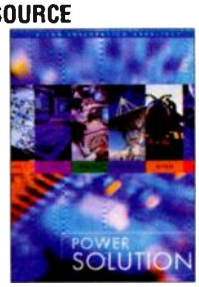
Melcher has introduced a new 1100 page data book, which details many new lines of innovative ac-dc and dc-dc converters. The data book is also an invaluable reference on standards in the power supply industry.

CIRCLE 254

MELCHER INC.

CUSTOM POWER RESOURCE

This free literature is helpful for users who rely on outside resources for their custom power requirements. In addition to general information on Vicor Integration Architects (VIAs), it also includes examples of custom power solutions that were designed and manufactured for the unique requirements of EOEMs in the EDP, Industrial, Communications, Test equipment, Medical and Defense (COTS) markets.

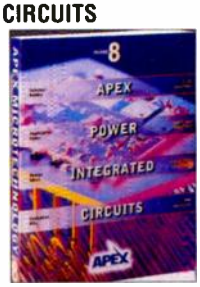


CIRCLE 255

VICOR CORPORATION

POWER INTEGRATED CIRCUITS

The 8th edition Apex Integrated Circuits data book contains complete product data sheets and applications notes for Apex Microtechnology's Power Amplifier, PWM Amplifier and DC/DC Converter product lines. Call: 1-800-862-1021; FAX: 1-520-888-3329; E-MAIL: prodlit@apexmicrotech.com

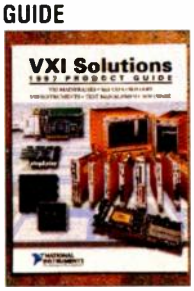


CIRCLE 256

APEX

FREE VXI SOLUTIONS GUIDE

The 1998 VXI Solutions Product Guide is a catalog and technical reference featuring product information on controllers, software, and our new VXI-DAQ instruments. VXI Solutions also includes a directory of over twenty VXI system experts from our Alliance program. (512) 794-0100; (800) 433-3488 (U.S. and Canada), Fax: (512) 794-8411; e-mail: info@natinst.com; www.http://www.natinst.com



CIRCLE 257

NATIONAL INSTRUMENTS

CONTACT MAGAZINE

CONTACT is a magazine for the embedded systems industry published by the SPACE Program (Siemens partner's Association for development tools supporting Siemens 8-, 16- and 32-bit microcontrollers). Published quarterly, it features applications articles, design tips and programming shortcuts, and informative articles in every issue. FREE Subscriptions available at www.spacetools.com

CIRCLE 258

SIEMENS

Magnetic Components & Integrated

Modules for LAN, Power and Telecom. Pulse, one of the largest magnetics components manufacturers in the world, has just released its Summer 1998 Short Form Catalog which summarizes Pulse's line of transformers, inductors, filter modules and mini RF inductors. Phone: (619) 674-8100; FAX: (619) 674-8262; www.pulseeng.com

CIRCLE 259

PULSE

GIANT NEW SWITCH CATALOG

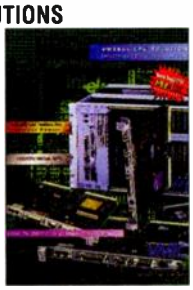
APEM's new 420 page full-line catalog is packed with their switch offerings. New products added: toggles, rockers, push-buttons, tacts, keys, industrial controls, DIPs, rotary DIPs, micro-limits, pushwheels, slides, keyboards, sealing boots. Many state-of-the-art switch models featuring process compatibility, surface mounting technology & electrostatic discharge withstanding. APEM Tel: 781-246-1007, Fax: 781-245-4531, URL: http://www.APEM.com E-Mail: info@APEM.com

CIRCLE 260

APEM

EMBEDDED CPU SOLUTIONS

This brochure features VMIC's line of 486, 586, AMD K6, Pentium®, Pentium Pro, and Pentium II processor-based CPU's. These VMEbus and CompactPCI boards are designed to meed the needs of the most demanding applications. A line of software products is also available to support the wide range of price/performance options. 800-322-3616; http://www.vmic.com



CIRCLE 261

VMIC

CONNECTORS

Harting's harmik® catalog shows and describes a range of miniature connectors designed to meet the requirements of internal and external connections of the future. Features include: reduced size (contact pitch of 1.27 mm) and high contact density. (847) 741-1500, fax: (847) 741-8257.

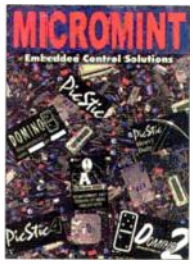
CIRCLE 262

HARTING INC. OF NORTH AMERICA

ELECTRONIC DESIGN CATALOG/LITERATURE REVIEW

CATALOG OF EMBEDDED CONTROLLERS

Micromint, Inc., is a leading supplier of single-board computers and peripherals of the OEM embedded control marketplace. Micromint's latest offerings include an assortment of component-sized direct-programmed high-level-language controllers and a family of network-connected data-acquisition modules. Phone: (860) 871-6170; fax: (860) 872-2202; http://www.micromint.com



CIRCLE 263

MICROMINT

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CIRCLE 264

ACCUTRACE INC.

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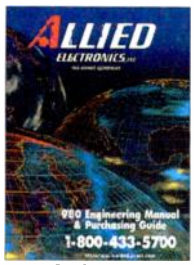
CIRCLE 265

ACCEL TECHNOLOGIES

ELECTRONICS ENGINEERING MANUAL

Allied Electronics Engineering Manual & Purchasing Guide contains reference data plus electronics from over 275 manufacturers. The Allied Catalog is available on CD-ROM. Allied Electronics is an Avnet Company with access to hundreds of millions of dollars of inventory. This breadth and depth gives you service capabilities found only at Allied Electronics, Inc. http://www.allied.avnet.com; 1-800-433-5700.



CIRCLE 266

ALLIED ELECTRONICS

FREE VHDL SIMULATOR

Aldec, Inc., announces the release of Active-VHDL version 3.1 a complete VHDL design environment. Active-VHDL is a complete IEEE 1076-93 VHDL design environment, including a VHDL editor, Behavioral Simulator, Automatic Test Bench Generator, interface to logic synthesis & FPGA/CPLD vendor P/R tools, VHDL design browser & Structural VHDL simulation. (800) 487-8743; (702) 456-1222; www.aldec.com

CIRCLE 267

ALDEC, INC.

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The new standard in high-end in-circuit emulators, SuperTAP solves tough hardware/software integration problems, debugs firmware and software, maximizes embedded system quality and performance. Palm-sized, full processor speed, easy set up, at half the price of chassis-based emulators 1-800-426-3925.

CIRCLE 268

APPLIED MICROSYSTEMS

HIGH VOLTAGE RF & DC RELAY CATALOG

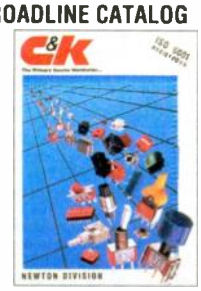
Product Guide from Kilovac, a division of CII Technologies, features a broad line of high voltage RF & DC power relays and contactors. Feature ratings and specifications on relays up to 70 KV including QPL. Choose from 28 Vdc 270 Vdc aerospace power relays, contactors and power controllers. Industrial contactors to 750 Vdc. Contact: Pat McPherson, 805-684-4560; 550 Linden Ave., Carpinteria, CA 93013.

CIRCLE 269

KILOVAC Div. of CII TECHNOLOGIES

C&K's EXPANDED BROADLINE CATALOG

C&K's expanded Newton Division Catalog #9801 is the most extensive switch catalong in the industry with 360 pages of models and options and process compatible switches. C&K Components, Inc., 57 Stanley Avenue, Watertown, MA 02172; Tel: (800) 635-5936 or (617) 926-6400; Fax (617) 926-6846.

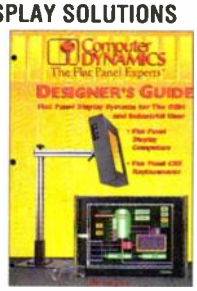


CIRCLE 270

C&K COMPONENTS, INC.

1998 FLAT PANEL DISPLAY SOLUTIONS

Designer's Guide offers the latest color displays ranging from 17.7" to 6.4" and XGA to VGA resolution. Sunlight-readable displays up to 900-nit. Variety of touchscreens, enclosures, and other mounting options. SBCs including MMX-Penitum. CALL for sunlight-readable, Ultra-HiBrite Assemblies datasheet. (864) 675-0106; e-mail: sales@dynamics.com; www.cdynamics.com



CIRCLE 271

COMPUTER DYNAMICS

DEVICE PROGRAMMERS & HANDLERS

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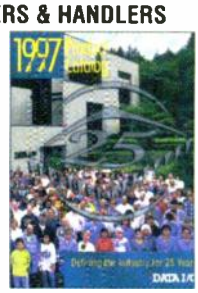

CIRCLE 272

DATA I/O

NEW OEM POWER SUPPLY CATALOG

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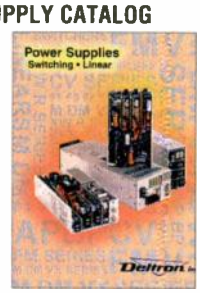

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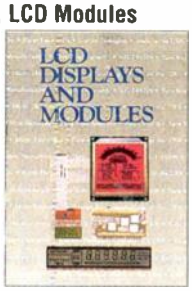
DELTRON

Custom LCD Displays, LCD Modules

DCI's catalog covers the complete line of standard, custom, and semi-custom LCD displays. A semi-custom display allows the user to specify custom annuciators on a standard display and not pay ful custom set-up costs. Detailed are DCI's capabilities for miniaturizing and assembly of complete LCD modules using wire bonding, TAB, surface mount, or thruhole technologies. 913-782-5766; fax, www.dci.incorporated.com.



CIRCLE 274

DCI INCORPORATED

INTERCONNECT SOLUTIONS

This catalog enables design engineers to easily locate the correct adapters, clips and test accessories. The catalog includes a Ball Grid Array Reference Guide along with information on over 4000 ET products, including emulator tools, logic analyzer/scope adapters, programming adapters, production/test adapters, debugging accessories, prototyping adapters, field-configurable adapters and custom adapters. 1-800-ADAPTER www.emulation.com

CIRCLE 275

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CIRCLE 276

EOS CORP.

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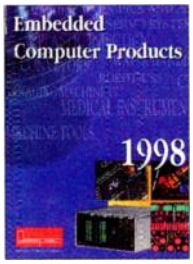
CIRCLE 277

GALVANTECH, INC.

ELECTRONIC DESIGN CATALOG/LITERATURE REVIEW

EMBEDDED COMPUTER PRODUCTS

Gespac's 1998 catalog features a full line of 3U embedded PCs, 68XXO SBCs, motion control and over 200 I/O functions. The G-windows GUI for real-time systems running. OS-9 is also offered. www.gespac.com or Phone 800-443-7722



CIRCLE 278

GESPAC INC.

A WEALTH OF SWITCH INFORMATION

Grayhill's 320 page catalog provides you with electromechanical switch data, reference material, dimensional drawings and photos. Catalog No. 1 includes information on DIP Switches, Rotary Switches, Keyboards and Keyboard Modules. The detailed information allows the catalog uses to select the proper product for their appliction right down to the part number. Phone: (708) 482-2131, Fax: (708) 354-2820.

CIRCLE 279

GRAYHILL, INC.

INDUSTRIAL PC POWER SUPPLY

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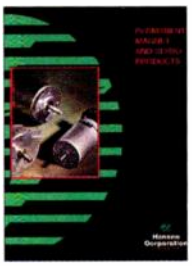
CIRCLE 280

ICP ACQUIRE, INC.

HANSEN PERMANENT MAGNET

and Servo Products. Hansen offers DC and Stepper motors. DC motors are used in automotive, office machine, and computer peripheral industries. Stepper motors are designed for precision motion control applications like computer peripherals, office machines and HVAC. Hansen is ISO 9001-94 registered. Sales phone (812) 385-3415. Fax (812) 385-3013.



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CIRCLE 282

IMAGINEERING

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CIRCLE 283

INNOVATIVE INTEGRATION

INTUSOFT ``SPICE'' NEWSLETTER

A quarterly publication containing application notes, technical articles and modeling techniques on spice circuit simulations and test design. Available in hardcopy or online (www.intusoft.com.). Modeling disks accompany annual subscriptions ($45.00).

CIRCLE 284

INTUSOFT

VLSI INTERCONNECTION SPECIALISTS

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CIRCLE 285

IRONWOOD ELECTRONICS

"No-Power" Cholesteric Crystal Displays

Kent Displays' brochure details the benefits of No-Power™ Reflective Cholesteric Liquid Crystal Displays. This technology requires no energy to maintain an image. Displays have wide viewing angles and are flicker free. Call (330) 673-8784.

CIRCLE 286

KENT DISPLAYS

KEPCO POWER ASSEMBLY PROGRAM

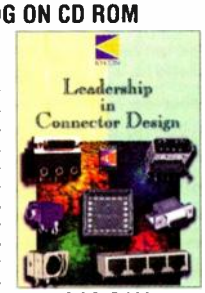
Selection of front & rear metering, connection, signaling and adjusting panels may be custom configured for your needs. Brochure 146-1863 describes Kepco's Power Assembly Program, how to select modules, options available for your assembly, how your system will be configured & documented. Kepco Inc., Tel: (718) 461-7000, email: hq@kepcopower.com, www.kepcopower.com.

CIRCLE 287

KEPCO

CONNECTOR CATALOG ON CD ROM

This 100 page catalog is available in both the standard full-line catalog and on CD ROM and includes many new products with complete specifications. Among the product highlights in Kycon's Catalog #11 are: •D-Subminiature connectors •Modular jacks •Mini-DINs • Stereo jacks •Power connectors •USB connectors • High temperature connectors • Ferrite and shielded connectors.

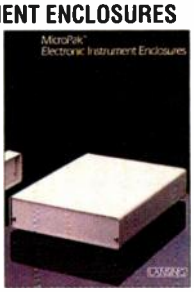


CIRCLE 288

KYCON, INC.

MICROPAK® INSTRUMENT ENCLOSURES

Lansing Instrument Corp. offers enclosures for smaller, free standing electronic instruments used in hand-held or desktop applications. Three body styles and a choice of end cap configurations are available, along with several finishes and colors. Literature includes information for stock and custom choices, and a no-risk offer at a special price. Contact Rich Kippola at Lansing Instrument Corp., (800) 847-3535.



CIRCLE 289

LANSING INSTRUMENT CORP.

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Master Bond Inc., Hackensack, NJ manufactures over 3000 grades of adhesives, sealants and coatings. Line cosists of epoxies, anaecobics, cyanoacrylates, silicones and acrylics. One and two part systems are available. Tel 201-343-8983.

CIRCLE 290

MASTER BOND INC.

1998 SRAM DATA BOOK

NEW! Includes detailed product data sheets on 1Mb, 2Mb, and 4Mb SyncBurst SRAM; 2 Mb and 4Mb ZBT™ SRAM; and 4Mb Late Write and Claymore SRAM. You'll find technical notes, package drawings and sales and service info. Be sure to visit our web site: www.micron.com/mti.

CIRCLE 291

MICRON SEMICONDUCTOR

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Enables you to solve your high speed design problems throughout the design process, from initial concept through manufacturing output. Address the critical issues you face with high performance circuitry, signal integrity, interconnect density and timing problems. 1-888-482-3322;e-mail: info@veribest.com; www.veribest.com

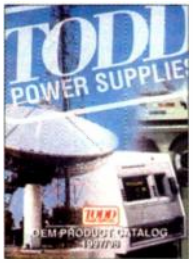
CIRCLE 292

VeriBEST

ELECTRONIC DESIGN CATALOG/LITERATURE REVIEW

FREE TODD OEM SUPPLY CATALOG

Features NEW SPH-1200 (at 38 cents per watt in OEM quantities) and NEW TCM-1000, (both with PFC, single output, slope program current sharing, hot swap); NEW TMX-350 (multiple output, 48 Vdc clone of RMX-350). Over 260 standard products from 1 to 1500 watts. 800-223-8633; 516-231-3366; fax: 516-231-3473; email: info@toddpower.com; http://www.toddpower.com

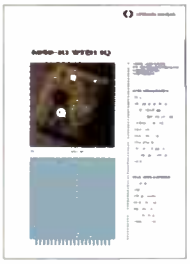


CIRCLE 293

TODD PRODUCTS CORP.

6050 I/O With I/Q

Octagon Systems has introduced a new family of single card industrial computers called the PC Microcontroller Series. The card family combines the industry standard PC architecture with industrial-class I/O and an extensive suite of embedded software in a small 4.5 X 4.9 package rated from - 40° to 85° C.

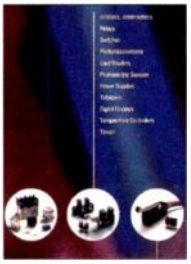


CIRCLE 294

OCTAGON SYSTEMS

NEW SHORT FORM CATALOG

Omron's Control Components Short Form Catalog contains 200-plus pages of relays, switches, photomicrosensors, card readers, photoelectric sensors, power supplies, totalizers, digital displays, temperature controllers and timers. Call 1-800-55-OMRON. E-mail: SFC2_EDLit@omron.com

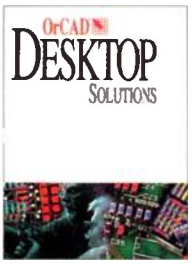


CIRCLE 295

OMRON ELECTRONICS, INC.

FREE EDA CD-ROM

OrCAD's new Desktop Solutions CD includes product overview, detailed data sheets and working demo versions of OrCAD's 32-bit Windows software- including new OrCAD Express and Capture CIS. Order today by calling 1-800-671-9505 or visit our website at www.orcad.com



CIRCLE 296

ORCAD

HARSH ENVIRONMENT CONNECTORS

Find exactly the connector you need in this well organized guide including illustrations, dimensions, layouts, & assembly instructions from PEI Genesis, Phone: 1-800-858-6903

CIRCLE 297

PEI GENESIS

Integrated Switching Regulators

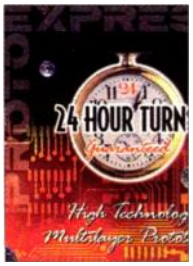
Power Trends' new 120 page full-line catalog details their complete line of Integrated Switching Regulators (ISR)s and DC to DC Converters. The catalog introducts significant new 5V, 12V, and 24V bus products along with extensions to existing product lines. Photos and standard applications are provided for each product. (800) 531-5782, Fax: (630) 393--6902; E-mail: sales@powertrends.com www: http://www.powertrends.com

CIRCLE 298

POWER TRENDS, INC.

MULTILAYER PROTOTYPE

Award winning quick turn multilayer prototype manufacture specializing in 24 hour to 5 day turns, for commercial and milspec boards (Milp-55110E) on FR4 and polyimide materials. Our capabilities also include "blind and buried" vias, full body gold, carbon baste, metal core boards, small hole drilling, and net list testing.



CIRCLE 299

PROTO EXPRESS

Challenging Cable Assembly Specialists

Precision Interconnect, a division of AMP Inc. has released a new brochure explaining their design and manufacturing approach for cable assemblies needing to perform in challenging electrical, mechanical or environmental applications. Solutions include miniaturization, dense packaging, precise electricals, sealed systems, etc. Phone (503) 620-9400; Fax (503) 620-7131.

CIRCLE 300

PRECISION INTERCONNECT

LIQUID CRYSTAL DISPLAYS

A division of Purdy Electronics has released its 1998 LCD short form catalog. The catalog features a full line of TFT and STN color panels and monitors plus intelligent graphic and character monochrome displays.

CIRCLE 301

PURDY ELECTRONICS CORP.

LITERATURE REVIEW

Complete selection of embedded single board computers featuring Intel's 386EX and 80188EB embedded microprocessors and I/O modules. All products fully software supported by C/C++ demo and drivers. Call 1-888-RLC-TECH, FAX (805) 466-9736 or visit our website at http://www.RLC.com

CIRCLE 302

RLC ENTERPRISES INC.

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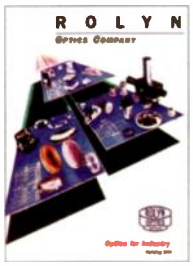
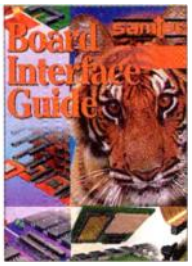


CIRCLE 303

ROLYN OPTICS CO.

NEW FULL LINE SAMTEC CATALOG

Samtec's new Board Interface Guide F-198 features Micro Board Interface Systems for Ultra Fine Pitch, Ultra Low Profile, Ultra High Density, One-Piece, Card-to-board and Off-Board Interfaces. Included are deatiled discussions of Flex Design and Flex Processing capabilities, as well as micro cable and application specific interfaces. 800-SAMTEC-9; (800-726-8329); fax: 812-948-5047.



CIRCLE 304

SAMTEC

Siemens Optoelectronics Data Book

Application notes and detailed specifications for: LED Intelligent Display® devices; LED lamps; LED numeric displays; optocouplers; solid state relays; fiber optic components, high power laser diodes, transceivers and subsystems; IR emitters, photodiodes, phototransistors, photovoltaic cells and data transceivers; optical DAA. 1-800-77-siemens;www.smi.siemens.com/opto4.html

CIRCLE 305

SIEMENS MICROELECTRONICS

INTERNATIONAL GUIDE

For 50/60 Hz Transformer Specifiers. Signal Transformer has issued the International Guide to Single Phase Voltage and Frequency Standards for design engineers who specify 50/60 Hz transformers used in equipment eqarmerked for export. Contact Signal Transformer Co., Insilco Technologies Group, 500 Bayview Ave., Inwood, NY 11096-1792. Phone: (516) 239-5777; fax: (516) 239-7208.

CIRCLE 306

SIGNAL TRANSFORMER CO.

RELAYS & CIRCUIT BREAKERS

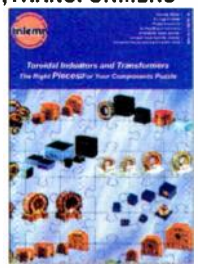
Stock catalog lists Potter & Brumfield and Siemens relays and circuit breakers. Electromechanical, solid state and time delay relays are detailed, as well as magnetic and thermal breakers. Many ratings and various coil, package and terminal options are offered.

CIRCLE 307

SIEMENS ELECTROMECHANICAL COMPONENTS

ELECTRONIC DESIGN CATALOG/LITERATURE REVIEW

TOROIDAL INDUCTOR,TRANSFORMERS



In addition to its legendary transformers, Talema Electronic offers a comprehensive line of standard toroidal components. Products available include current sense inductors, common mode chokes, magnetic amplifiers, low cost power inductors, highcapacity storage chokes, and high current surface mount inductors. Call (573) 265-5500 or fax (573) 265-3350; http://www.talema.com; e-mail: talema@talema.com

CIRCLE 308

TALEMA ELECTRONICS

IC DESIGN SOFTWARE

Tanner EDA offers innovative, feature rich yet easy to use software solutions for custom and semi-custom IC design entry, simulation, layout and verification on Windows platforms, all at cost-effective prices. With ten years of experience producing EDA software for the PC, we offer an outstanding price-performance combination. www.tanner.com/eda; (626) 792-3000; info@tanner.com.

CIRCLE 309

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Catalog describes the RelCalc for Windows software package, which automates MIL-HDBK-217 or Bellcore on your PC, and allows quick and easy reliability analysis of your electronic products. Phone: 818-991-0057, Fax: 818-991-1281, E-mail: info@t-cubed.com. Visit our web site for a FREE DEMO: www.t-cubed.com.

CIRCLE 310

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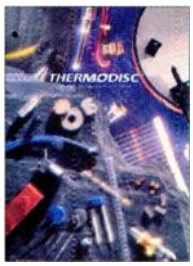
CIRCLE 311

TERN INC.

THERM-O-DISC CATALOG

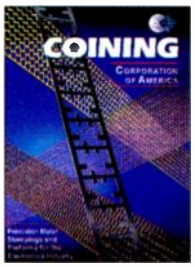


Therm-O-Disc's 20 page catalog showcases NTC and PTC thermistors including disc, rod, glass encapsulated, and surface mount chips, plus inrush current suppressors, ceramic current limiters, linear PTC's, temperature switches, varistors and NTC assemblies. 616-777-4100; fax: 616-773-4214.

CIRCLE 312

THERM-O-DISC

PRECISION METAL STAMPINGS



A new 10-page full-color brochure from Coining Corp. of America outlines the company's broad range of precision metal stampings and preforms for use in electronic component production. Users can select from a very extensive standard tooling list or specify virtually any custom shape. Phone: 201-791-4020; Fax: 201-791-1637; e-mail:coining-corp@worldnet.att.net.

CIRCLE 313

COINING CORP. OF AMERICA

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- ¥Advanced Triggering
- ¥Only 9 oz and 6.3 x 3.75 x 1.25 !
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1 to 32	$250	$275	$400	$480	$600	$750
33 to 72	$275	$300	$420	$510	$680	$870
73 to 108	$300	$320	$440	$540	$750	$990
109 to 144	$320	$340	$460	$570	$940	$1190
145 to 176	$340	$360	$480	$600	$1000	$1300
177 to 208	$365	$380	$500	$630	$1090	$1480
209 to 240	$380	$400	$520	$660	$1250	$1660
241 to 288	$400	$420	$540	$690	$1350	$1800

6 Pieces

in²	SS	DS	4L	6L	8L	10L
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33 to 72	$290	$320	$520	$620	$850	$1200
73 to 108	$325	$340	$580	$690	$960	$1450
109 to 144	$345	$360	$640	$760	$1090	$1700
145 to 176	$370	$380	$700	$880	$1200	$1950
177 to 208	$395	$400	$760	$1090	$1350	$2300
209 to 240	$425	$420	$820	$1370	$1500	$2700
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33 to 72	$340	$380	$620	$730	$1200	$1650
73 to 108	$360	$420	$700	$820	$1450	$2200
109 to 144	$390	$460	$780	$910	$1700	$2650
145 to 176	$420	$500	$860	$1100	$2000	$3100
177 to 208	$450	$540	$940	$1290	$2400	$3700
209 to 240	$490	$580	$1020	$1470	$2800	$4350
241 to 288	$530	$620	$1100	$1650	$3100	$5200

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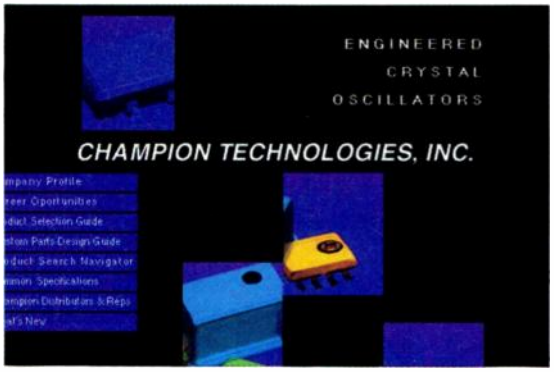

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Our Electronic Engineering Group is pleased to announce the launch of ***Career Opportunities in Electronic Engineering ON CAMPUS***. The Fall 1998 Launch issue will arrive on college campuses the first week of September, the prime time for recruitment.

Designed and written specifically for electronic design engineering graduates, this special magazine will offer career development strategies and "inside track" information on where the diverse and challenging opportunities are within the industry segments that make up the high-tech markets in America today.

DISTRIBUTION:

The fall '98 edition will be distributed to more than 55,000 electronic engineering graduates at over 230 colleges and universities through the career placement office, dean's office and career days.

EDITORIAL FOCUS:

Career Opportunities In Electronic Engineering ON CAMPUS creates a "customized editorial environment" for your recruitment advertising campaign.

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Company profile
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Added exposure for your company's recruitment needs will be delivered beyond your advertisement in our college magazine through CareerLink (the career section featured on Penton's corporate site - www.penton.com).

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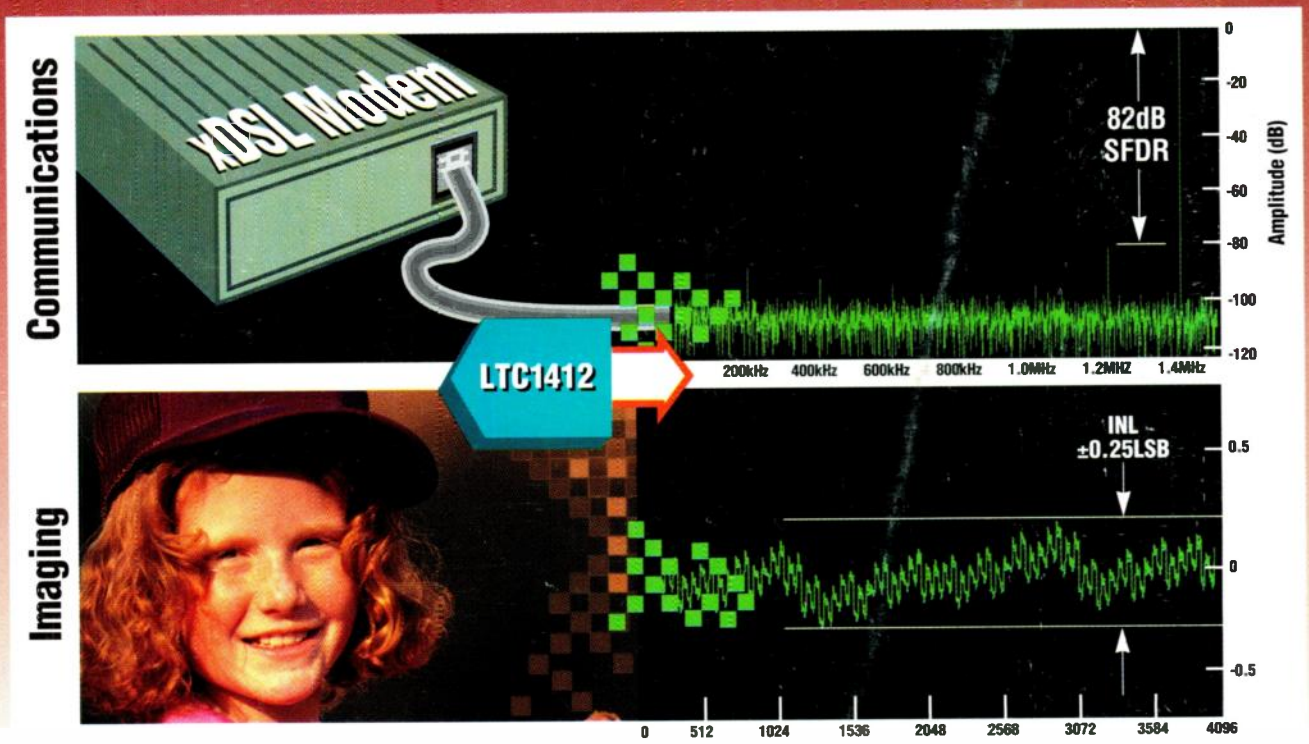

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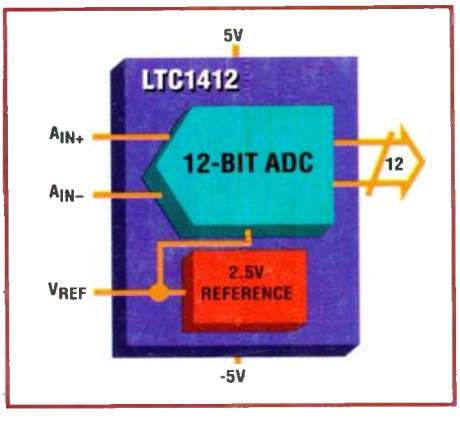

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