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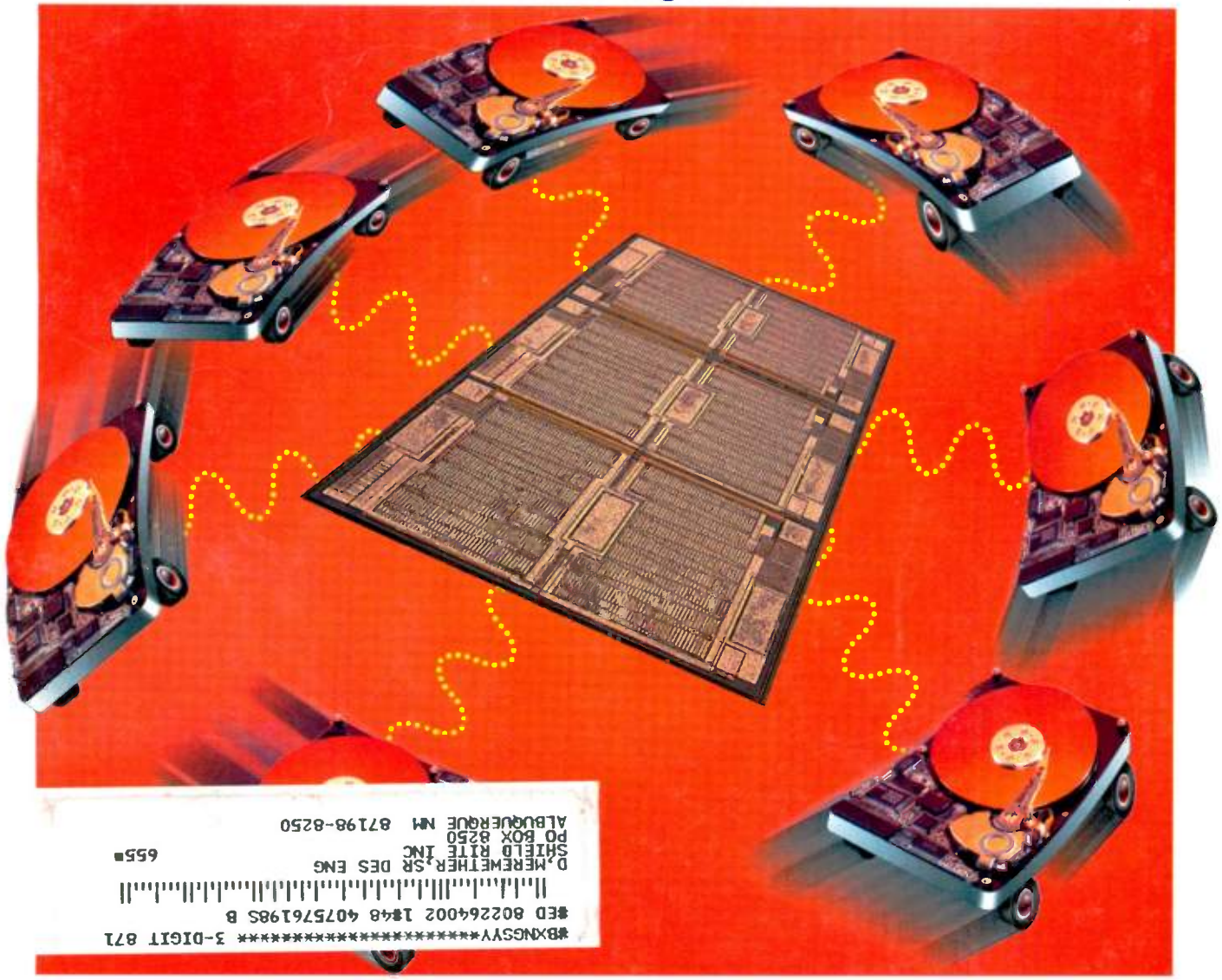
ELECTRONIC DESIGN

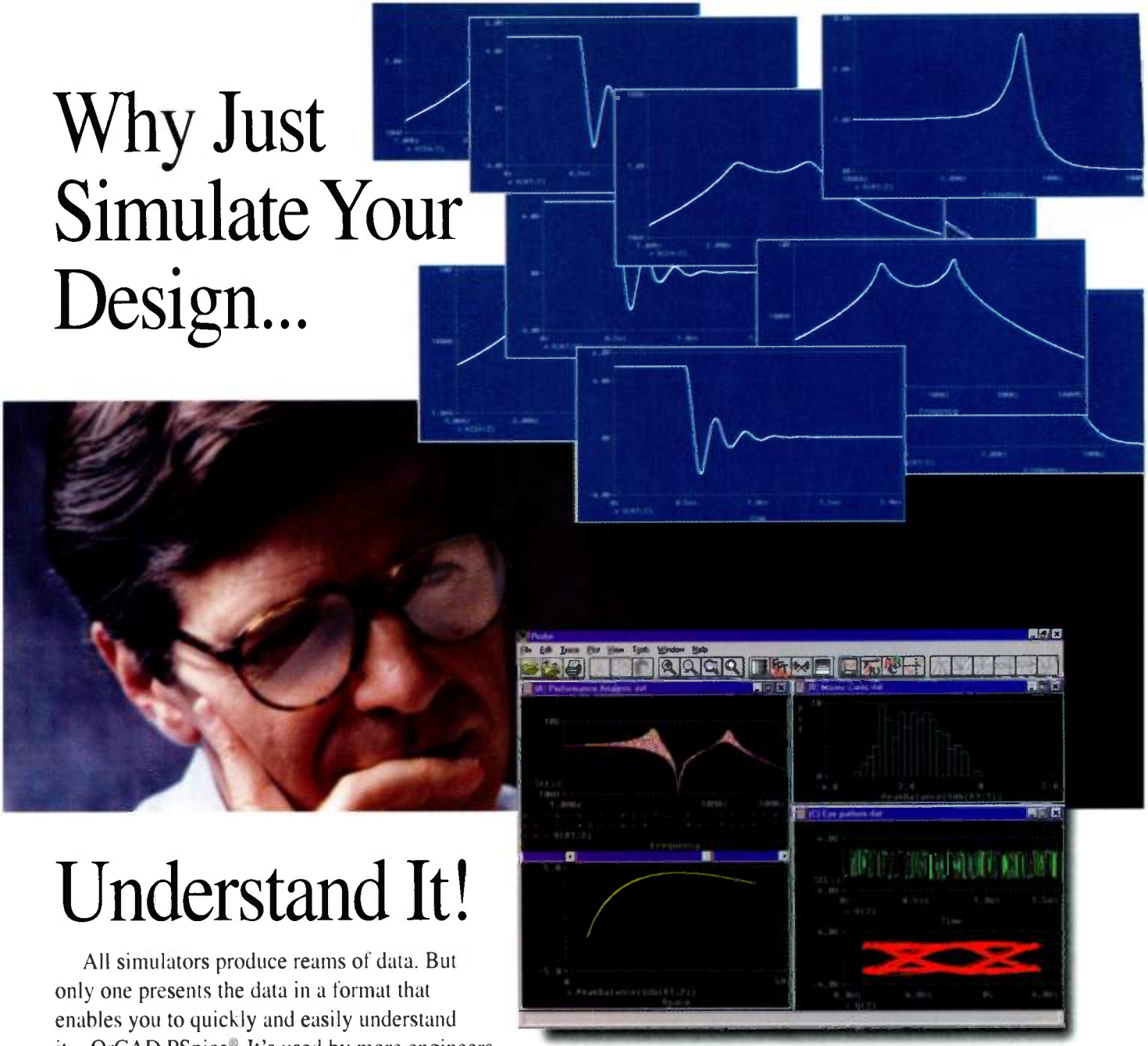
TECHNOLOGY • APPLICATIONS • PRODUCTS • SOLUTIONS

A PENTON PUBLICATION $8.00 www.elecdesign.com AUGUST 17, 1998



Triple Half-Bridge Forms New Motor-Control Design p. 32

Why Just Simulate Your Design...



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New PWM Selector Guide

New PWM Amplifier: SA07

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- Digital and analog input
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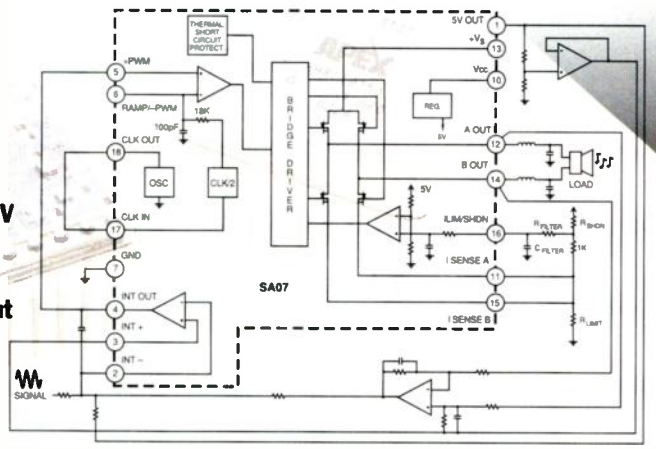
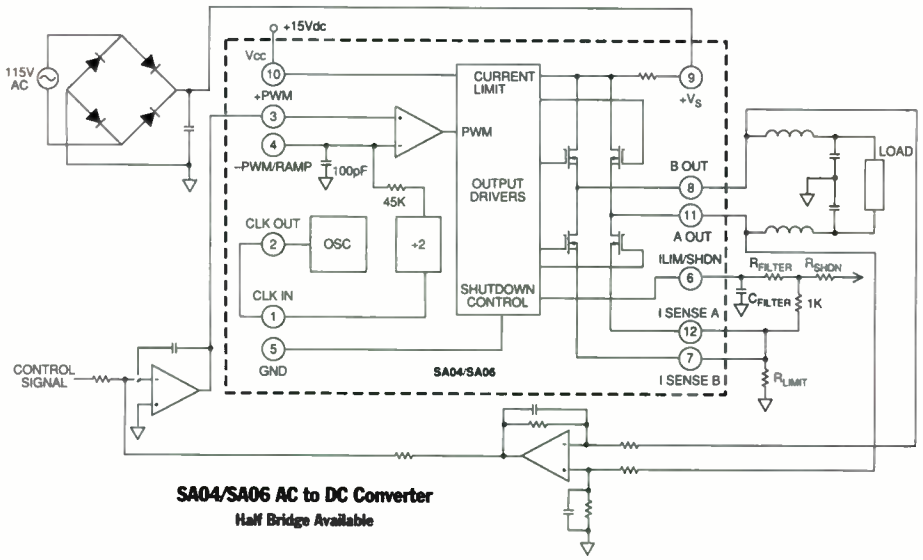
- Fault protection



High Fidelity Audio



SA04/SA06 AC to DC Converter

Half Bridge Available

PWM Amplifiers Product Selector Guide

Model	Efficiency	I_{OUT} Cont.	Supply	Switching Frequency	Thermal Protection	Power Delivery	Full or Half Bridge
SA01	97%	20A	16V-100V	42kHz	Yes	2000W	Full
SA02	94%	10A	16V-80V	250kHz	Yes	800W	Full
SA03	97%	30A	16V-100V	22kHz	Yes	3000W	Full
SA04	97%	20A	16V-200V	22kHz	Yes	4000W	Full
SA06	97%	10A	16V-500V	22kHz	Yes	5000W	Full
SA07	94%	5A	5V-40V	500kHz	Yes	200W	Full
SA13	97%	30A	16V-100V	22kHz	Yes	3000W	Half
SA14	97%	20A	16V-200V	22kHz	Yes	4000W	Half
SA16	97%	10A	16V-500V	22kHz	Yes	5000W	Half
SA50	97%	5A	up to 80V	45kHz	No	400W	Full
SA51	97%	5A	up to 80V	external set	No	400W	Full

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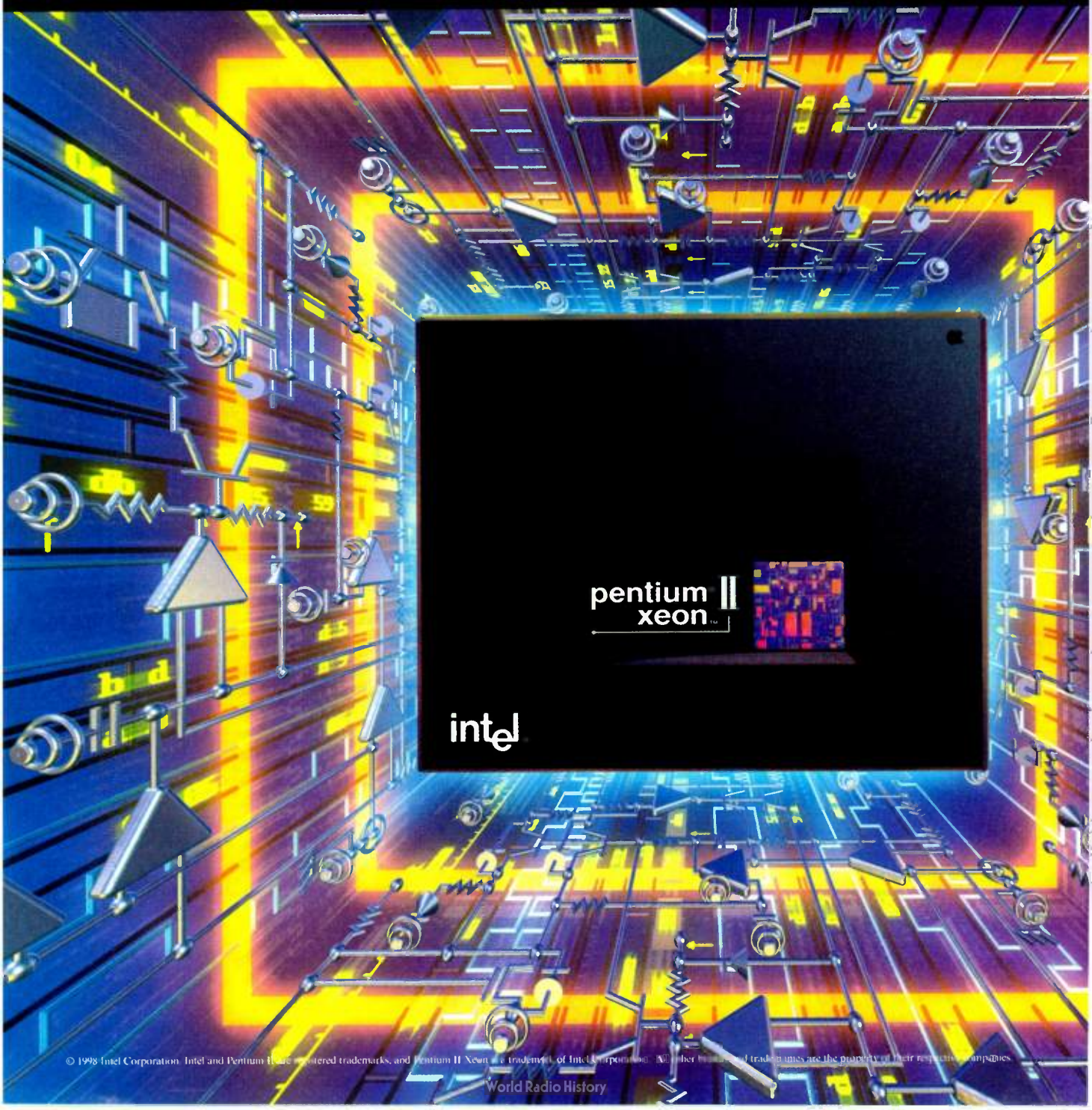

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August 17, 1998 Volume 46, Number 19

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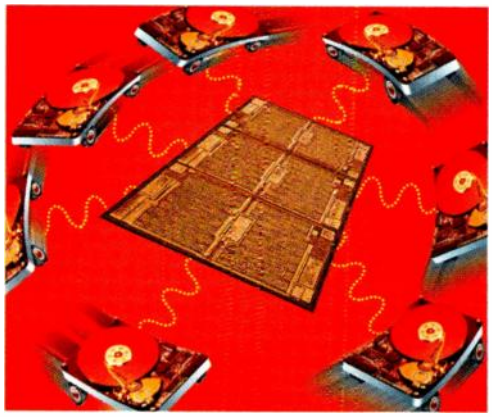

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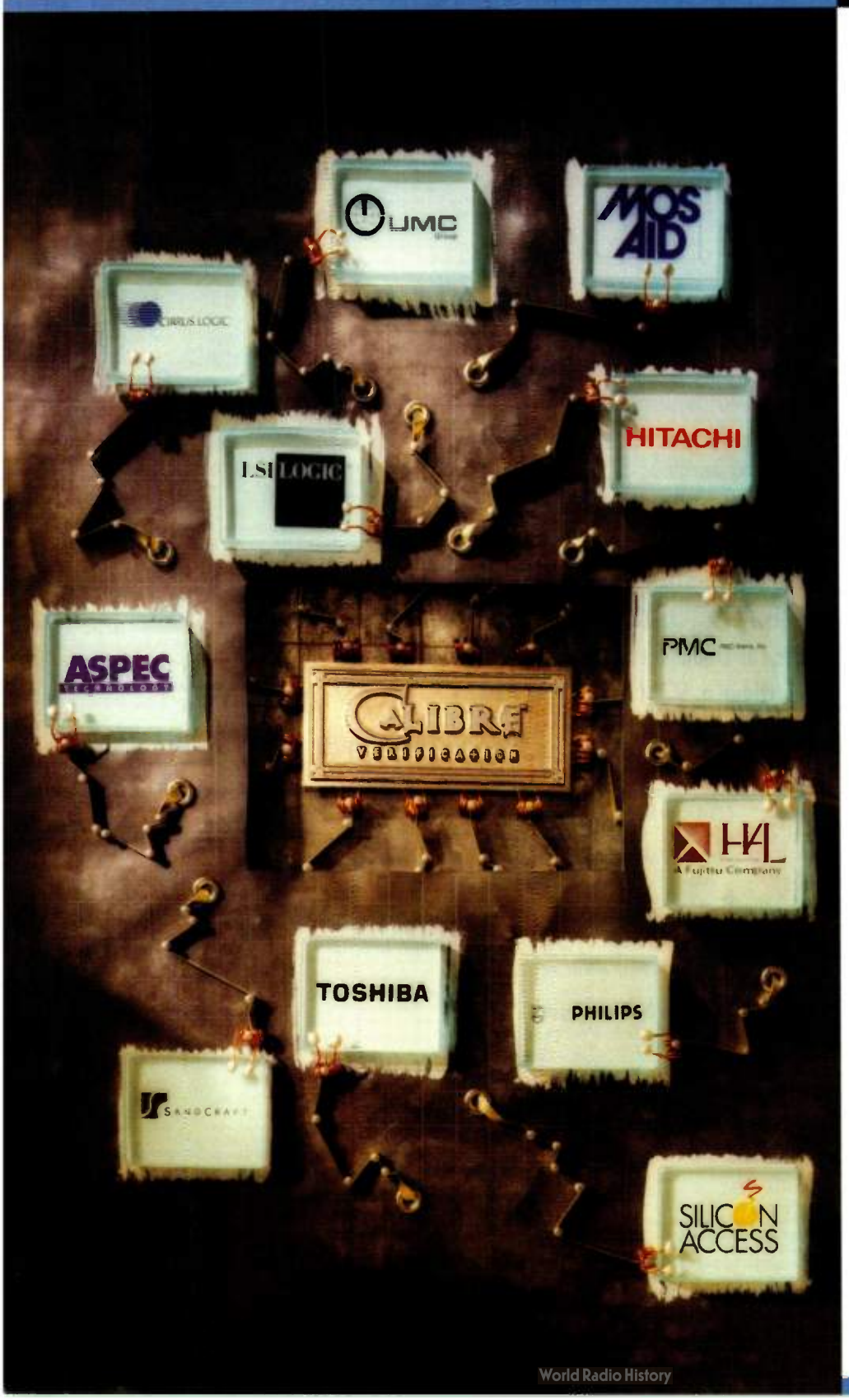

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TECHNOLOGY • APPLICATIONS • PRODUCTS • SOLUTIONS

August 17, 1998 Volume 46, Number 19

EDITORIAL OVERVIEW

DIGITAL DESIGN

QUICKLOOK

LOOKING AHEAD: September 1, 1998

Power Technology Focus:..... This annual look at advances in power technology will focus on benchtop and system supplies, and the latest in mobile power. Design applications will be preceeded by a staff-written report by Patrick Mannion on UPS developments.

Communications:..... How are LANs going to satisfy the insaitable demand for increased bandwidth caused by data-intensive applications? Communications Editor Lee Goldberg delves into one step being taken: emerging Internet Protocol (IP) standards.

Analog Design:..... Analog Editor Ashok Bindra takes a look at low-skew, low-jitter, phased-locked loops used for accurately distributing clock signals in high-speed memory modules and multimedia systems like DVD players and set-top boxes.

COVER ILLUSTRATION BY: BRUCE JABLONSKI

Jesse H. Neal Editorial Achievement

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August 17, 1998 Volume 46, Number 19

See Electronic Design Online's Table of Contents to preview what's in store for you on the web!

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For more information on the conference, including a listing of events and workshop schedules, see the link on Electronic Design Online's home page, www.elecdesign.com.

EDA: The Changing Design Process and Market

Download the presentation from the recent DAC Conference. Jointly sponsored by **Collett International** and **Electronic Design**, the presentation focuses on how electronic designers are developing circuits and systems.

To download the presentation, see the EDA Technology Lab at www.elecdesign.com

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ITU approves new audio quality measurement technique

NEWS

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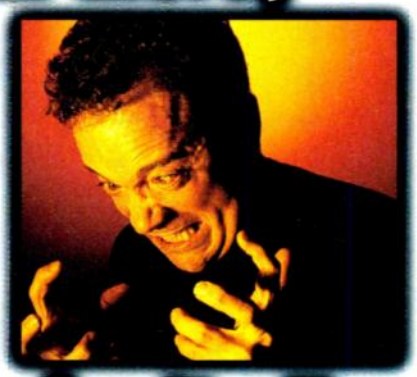

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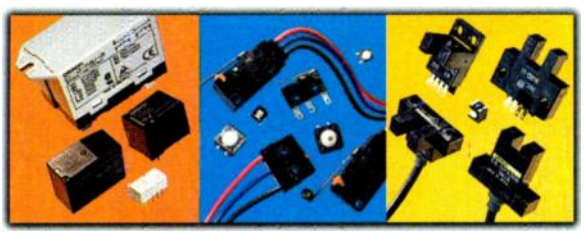

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EDITORIAL

KISS (Keep It Simple, Stupid)

I mutter the KISS message every now and then during the workweek. Building a magazine from scratch every two weeks requires a squadron of creative and talented people who all think that their deadlines and priorities are more important than mine! Of course, they're right. The troops know that our readers want this magazine in their hands every two weeks. There is no missing the press date. That is their mission. When they want answers, decisions, opinions, direction, arbitration, mediation, directives, and sometimes injunctions and restraining orders (just kidding), they expect management to a) make a decision, b) make a decision, c) all of the above.

Obviously, as you well know in your job, looming deadlines and 11th hour pressures force decisions that are not completely thought out, tested or put through the proper cause-effect analysis. And, we hope (and maybe pray) that our decisions pan out. But when a snap decision causes a product recall, lawsuit—or worse, injury or death, I'm sure the people who worked on the project said to themselves, "If I only had more time, I could have done more testing and analysis...." Of course, managers would say that they were forced by market and competitive pressures to "get the product out." Then the CEO would say that stockholders and Wall Street were hammering away for a better bottom line.

The KISS mantra works well for the majority of mundane problems that arise each day. But, if I were designing an airplane or automobile, I'd tweak KISS to say Keep It Superior, Stupid. I'm sure the Ford engineers who designed the old Pinto thought that packing a gas tank up against the rear bumper was a simple way to save valuable car length. Although, if the managers would have used the KIS(Superior)S model, someone might have foreseen the potential of a hand grenade on wheels. There are thousands of examples where poorly designed or manufactured products, drugs, etc. caused serious harm. When things go bad, who should be blamed, fired, or fined. Who should be held responsible or serve time?

Many of you design products that consumers blindly trust as safe to use. They have no choice but to believe that safety concerns were thought about during the design and manufacturing process. But we all know that isn't always the case. I'd like for you to share your thoughts on what you or your company is doing to ensure product safety. Send me an e-mail message; I'd like to post your comments on our web site.

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READER SERVICE 140

Dear Mr. Goldburg—Musings On Privacy

The error of an overworked typist at some anonymous data-entry mill was my first clue that I was a marked man. "Dear Mr. Goldburg," the letter began, a misspelling of my name that had first shown up in my junk mail a few weeks after I had applied for the mortgage. What kind of scam had I been targeted by this time? A time-share at Milwaukee's Cheese World theme park, or a hot investment opportunity in sod futures? No, it was worse.

"Congratulations, on the recent purchase of your new home at 1313 Mockingbird Lane, in beautiful Grovers Mill, N.J. It's one of the biggest and most important investments of your life," read the letter. "Yikes!" I thought, "They've dipped into the municipal database somehow, and pulled up my records!" It went downhill from there.

"When you and your wife, Catherine, purchased your home, did you give any thought to protecting this important investment?" "Cripes! How'd they get Catherine's name?" I wondered as I read on. "Have you considered how your family would deal with the mortgage payments on your lovely new home should something happen to you, Mr. Goldburg? With a balance of $138,752.38, your wife's salary of $45,275.82 might not be able to cover all her needs."

I started to get angry as I imagined the authors of this letter combing half a dozen quasi-legal databases to pinpoint my financial and legal status. "Of course," the letter continued, "considering your recent diagnosis of high blood pressure, and your family's average lifespan of 58.5 years, it might also be a good idea to protect your daughter Anwyn's chance to go to the college of her choice, too. We care about your family's future Mr. Goldburg, and that's why Acme Life Insurance is proud to offer you..." I finally tore the thing up, vowing to never open anything but bills and personal letters again.

LEE GOLDBERG
COMMUNICATIONS

Annoying as over-personalized junk mail is, it's just the telltale itch that tells you those "harmless" weeds you just ripped out might be poison ivy. The digital age holds a mixed bag of blessings and curses, as we've created a world where information is more easily accessible than any other time in history.

Today, there are few controls to keep credit companies, medical institutions, and other businesses from sharing information without our knowledge or permission. (We'll leave law enforcement agencies for another time.) While most of this activity is benign, what about a potential employer obtaining your medical history before making a job offer?

The Internet also raises some pretty hairy issues about free speech and privacy. Some corporations and organizations have successfully used legal maneuvering to gain the identities of, and silence critics who post true, but less-than-flattering, commentaries about them on IRC forums and web sites.

Privacy is also under attack in the U.S. legislature, as the White House and FBI are trying to make it illegal to have any cryptography technology that cannot be "cracked" by law-enforcement agencies. Does this buy us a more secure, drug- and crime-free country, or a land where we live under constant surveillance?

As citizens, and engineers, we have a special obligation to think hard about how to come up with a clear, fair-minded, and enforceable definition of privacy. We also need to push for laws that will get us off the path to an Orwellian future. Perhaps we should also ask ourselves tough questions about the kinds of work we are willing to do.

There aren't any easy answers, but there are a whole bunch of places where folks are debating these issues and taking action. The Electronic Frontier Foundation, (*www.eff.org*), the Global Internet Liberty Campaign (*www.glic.org*), the Stalker's Homepage (*www.glr.com/stalk.html*), and the politics and technology discussion forum at The WELL (*www.well.com/~declan/politech/*) are good places to start. Let me know what you think. *leeg@class.org.*

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READER SERVICE 135

Harmful Pacemaker/ EAS Interactions Being Studied

Two areas of the electronics industry are coming together to understand and prevent potentially dangerous interactions. The problem lies with the widespread use of electronic-article-surveillance (EAS) systems possibly interfering with sophisticated pacemakers, implantable defibrillators, and other sensitive medical devices. Researchers at Georgia Tech Research Institute, Atlanta, Ga., are working with developers of both types of equipment at a test center supported by surveillance-system manufacturers.

In the testing, pacemakers, defibrillators, and other devices are subjected to energy fields created by a representative group of eight EAS systems and two EAS-system tag deactivators. Using standardized test procedures, the medical devices' response is measured through their full range of operation. Resulting data is used by the manufacturers' design and quality assurance departments to improve their products, if necessary.

The devices are submerged in a tank of saline solution that simulates the electromagnetic behavior of the human torso. Using a computer-controlled positioner, the tank containing the medical device is moved through each merchandise control system in a manner that simulates the way customers might walk through such systems in retail stores. The test protocol also simulates customers standing in a checkout line near equipment used to deactivate the control tags.

Because of a nondisclosure agreement, the results generated by the research are given only to the manufacturers who submit the devices. The researchers don't have medical training, so judgements aren't rendered about the health implications of the measured data.

Contact Jimmy Woody at (404) 894-8326; e-mail: *jimmy.woody@gtri.gatech.edu*. Or contact Ralph Herkert at (404) 894-8602; e-mail: *ralph.herkert@gtri.gatech.edu*. RE

Carbon Composites Exhibit Negative Electrical Resistance

For the first time ever, carbon-fiber materials were observed to superconducted at room temperature—without cooling. Materials engineers at the University of Buffalo, N.Y., also discovered that when these materials were combined with others that are conventional, positive resistors, they exhibited zero resistance. To this point, zero resistance had been seen in superconducting materials, but only at temperatures of 125K, which is approximately –150°C or –234°F.

Without resistance, there's no energy loss, so the amount of energy that's put into a system is exactly the amount that it produces. Therefore, according to the researchers, the discovery has the potential to lead to much faster, much more efficient electronic devices that were previously assumed to be possible only with the development of room-temperature superconductors. Among the potential applications are simpler, more-powerful electronic circuits, and far-more-efficient "smart" structural components for aircraft and concrete structures.

Says Deborah D.L. Chung, PhD and leader of the research team, "With structural electronics, the structural composite itself can act as the electrical circuitry, but the fibers in the composite are far less conductive than copper. Our research shows that it is possible to overcome that resistance and make these structural electronics far more efficient."

The finding of negative resistance flies in the face of a fundamental law of physics—in that opposites attract. Chung explains that in conventional systems, the applications of voltage causes electrons, which carry a negative charge, to move toward the high, or positive end, of the voltage gradient. Here, though, electrons move the other way, from the plus end of the voltage gradient to the minus end.

Contact the UB's Office of Technology Transfer at (716) 645-3811; e-mail: *lohrman@research.buffalo.edu*. RE

Edited by Roger Engelke

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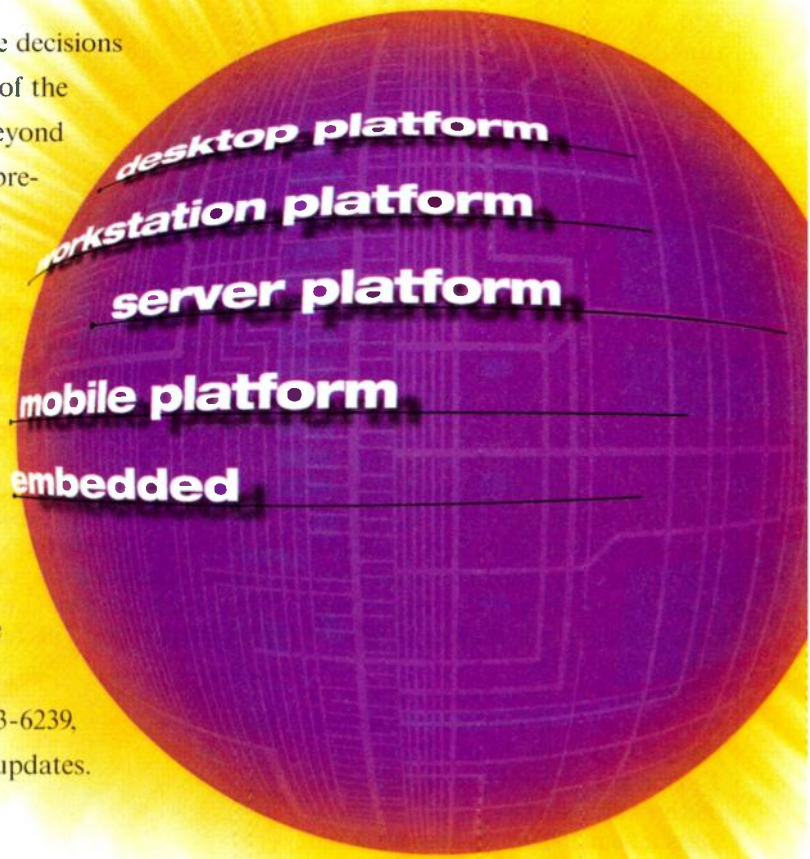

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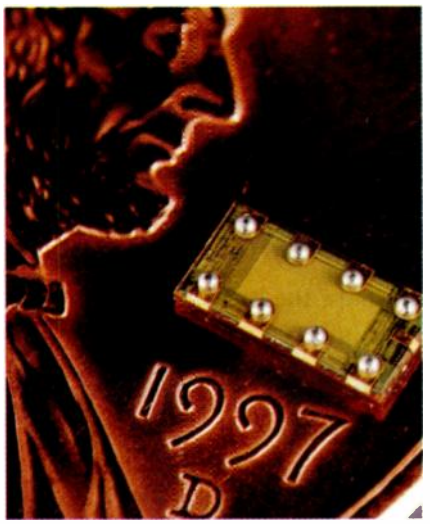
Chip-Area Packaging Scheme Trims Board Space, Weight For Low-Pin-Count Circuits

As designers attempt to shrink the size of portable systems, they encounter many hurdles. One formidable obstacle is the size of the IC packages used to hold low-pin-count devices such as serial EEPROMs. In a joint effort to remove the package as a size-limiting factor, designers at Xicor Inc., Milpitas, Calif., and Shellcase Ltd., Jerusalem, Israel, have fine-tuned a small-footprint, chip-area packaging scheme. The board area and clearance height required by the chip are drastically reduced, while the weight of the packaged circuit is also reduced considerably. Xicor plans to use the technique for a forthcoming family of serial EEPROMs.

Simply described, the "package" consists of the bare chip sandwiched between two thin layers of glass, which provide environmental protection for the circuit. Solder balls deposited on the contact regions supply connections from the IC to the circuit board *(Fig. 1)*. In actuality, there's a lot more magic to the manufacturing process that allows several thousand chips to be packaged simultaneously. The innovative technique lowers the per-device package cost, and allows the chips to be offered in large quantities.

The packaging process begins with the deposition of aluminum to extend the pad regions on the top of the wafer. Next, a thin epoxy layer is deposited on the wafer surface. A thin sheet of glass (about 100 µm) is then attached to the surface of the wafer. Once the epoxy cures, the wafer is flipped over, and the exposed surface is backlapped to reduce the wafer thickness from its initial value, 450 µm, to only about 50 µm *(Fig. 2)*.

After thinning, the wafer is etched from the back down to the extended aluminum pad regions to separate the individual chips. The glass that was attached to the top surface of the wafer keeps all the chips together, for now. Next, the back surface of the wafer is coated with epoxy and another sheet of 100-µm thick glass is attached, completing the "sandwich." The wafer is then flipped back over so the glass can be etched to open "windows" on the surface, and the pad areas are exposed.



1. This chip-area package, developed by Shellcase and Xicor, is about the same size as the date on a penny. It can be mass manufactured and offered at prices competitive to and potentially even lower than the popular SO-type epoxy packages.

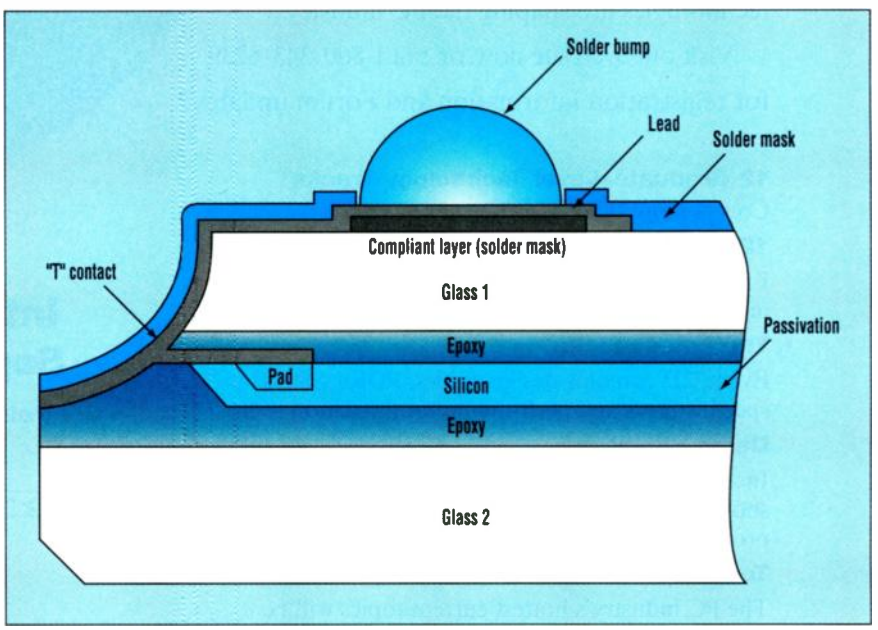
Once the pads are exposed, a compliant layer is added to reduce mechanical stress. Aluminum is sputtered on the surface and patterned with standard photolithography. This forms the leads from the pads to the region where the solder bumps will be deposited. Finally, all electrical leads are plated with zinc, nickel, and gold, and the solder bumps are screen-printed onto the wafer. A common wafer saw is used to cut the glass and separate all the chips.

Although the initial chip-area package was developed by Shellcase prior to the Xicor joint effort, the partnering resulted in an improved package. The compliant layers reduce stress under the solder ball, and the better passivation layer prevents moisture penetration. Both enhancements provide better long-term reliability.

Throughout the manufacturing process, all steps use standard processing and assembly techniques. This allows the packaging scheme to be transferred easily to just about any manufacturing facility that processes wafers. Because the scheme is applied at the wafer level, it eliminates the need for an epoxy package and leadframe, and can actually lower packaging costs versus popular SO-style epoxy packages. For now, the approach will be used to produce devices with 0.8-mm lead pitches, but the pitch should be able to migrate to 0.5 mm with little difficulty.

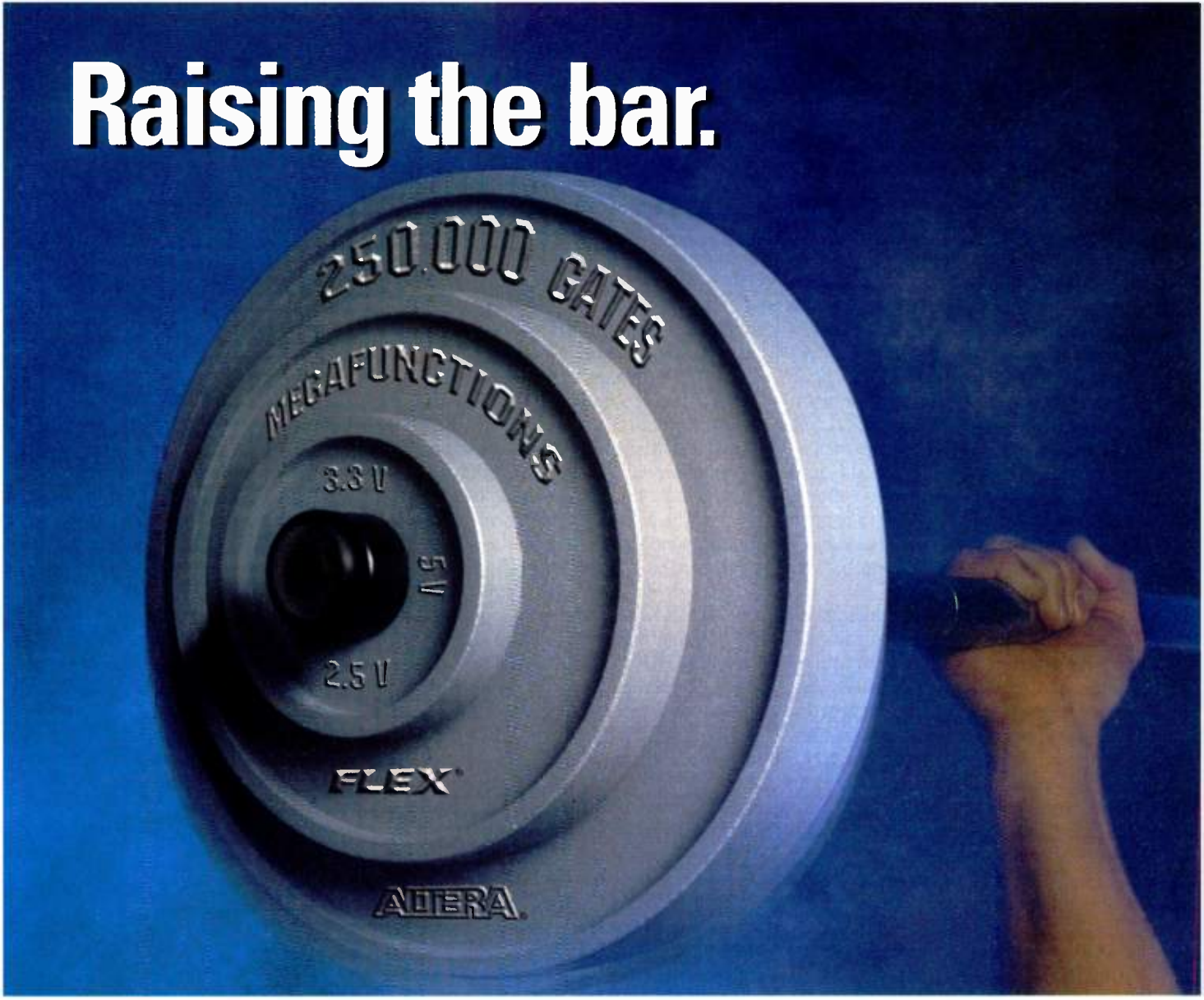
For licensing information on the packaging technology, contact Shellcase on the web at www.shellcase.com.

Dave Bursky



2. Produced using standard manufacturing techniques, the chip-area package scheme first sandwiches a thinned silicon chip between two layers of glass. It then adds the wiring and the solder-ball connections. A compliant layer reduces mechanical stress.

Raising the bar.



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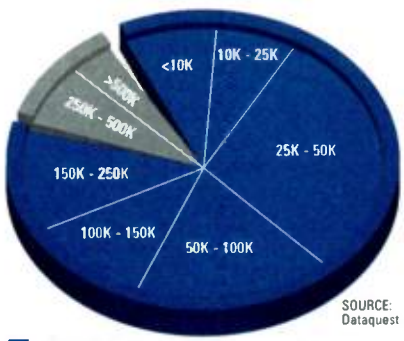

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Semiconductor Makers Pick Up Process Equipment To Deliver Multilevel Copper ICs

The quest is on for higher performance and lower power consumption in VLSI circuits. So far, the search is leading toward replacements for aluminum and tungsten metal systems in process technologies. Copper doping has been used in aluminum wiring to prevent electromigration. Yet pure copper, because of process incompatibilities, has never been used—until now. Research and partnership efforts have created a full end-to-end copper metallization flow that includes dielectric and metal layer deposition, as well as etch capabilities.

Circuits that use copper wiring can operate faster. The wiring resistance is much lower than that of aluminum or tungsten, thus reducing on-chip RC delays. Once mastered, the new process will allow higher wiring densities. Furthermore, the process to fabricate the copper metallization is actually simpler than standard metal deposition and etching, and could possibly lower the cost of manufacturing complex chips.

The new end-to-end technology, dubbed Damascus, was developed by designers at Novellus Systems Inc., San Jose, Calif. They worked in conjunction with LAM Research Corp., Fremont, Calif., and International Process Equipment Corp. (IPEC), Phoenix, Ariz. The process has already been demonstrated by Novellus.

At the heart of the process flow is the Sabre deposition system, also developed by Novellus. Sabre can deposit void-free copper using an electrofill process at rates of up to 50 wafers/hour. The electrofill capability can deposit copper in extremely narrow, high-aspect ratio structures—as small as 0.13 µm wide, with aspect ratios of up to 5:1. To complement the electroplating, designers must be able to deposit barrier layers. These layers provide complete containment of the copper and seed layers, ensuring the success of the copper fill in the deep, narrow structures.

Novellus developed a plasma-assisted vapor deposition (PVD) system, called INOVA, to perform these critical steps. The company worked with LAM to develop compatible etch and deposition equipment. With IPEC, Novellus developed compatible chemical-mechanical-polishing systems and deposition systems. Each company will sell its system independently. Together, the systems demonstrate the ability to implement a full-process flow.

The key to the Sabre system—a proprietary bath chemistry and chemistry control system—enables the high-quality copper fill. In addition, the system's novel cell design permits the films to be deposited with a uniformity of three sigma (<5%) within a wafer *(see the figure)*. The proprietary design of the wafer fixture, including a unique contact scheme, eliminates backside contact with the plating bath. It therefore eliminates potential backside copper contamination. During processing, the water bevel and the backside are kept dry by the wafer fixture's triple seal. The triple seal also provides an edge-exclusion to the plated film, which helps eliminate buildup at the bevel.

Playing an equally important role is the PVD system. This system leverages the proprietary 3D hollow-cathode magnetron source technology. The system deposits high-quality continuous films with excellent bottom coverage in high-aspect ratio structures. Such a capability is essential for both the barrier and seed layers in the copper interconnect structure.

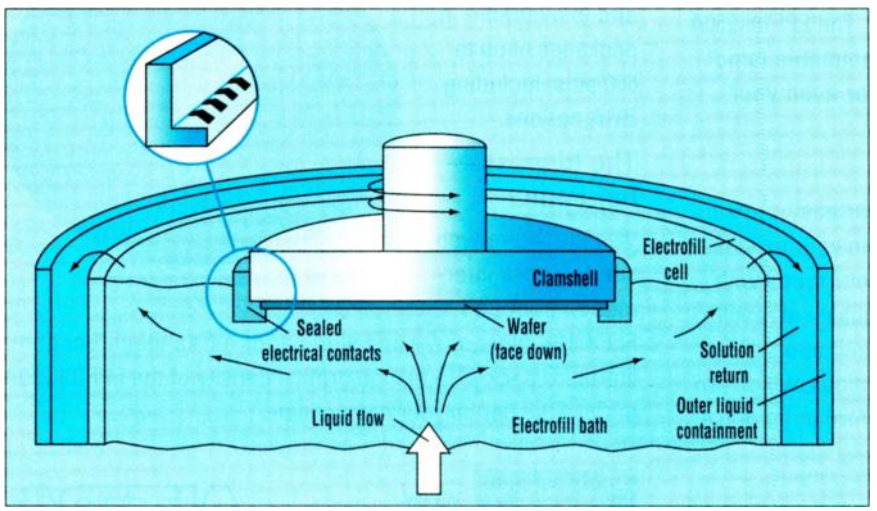
A tantalum barrier layer prevents copper migration by isolating the copper material from the rest of the device. The thin, copper seed layer that follows is essential to the success of the copper electrofill. It provides the continuity for the electrocurrent that serves as the "attractive pole" for the copper growth process. Lack of fill conformity can result in voids or discontinuities in the interconnects, which can be disastrous to device performance and yields.

Additional blocks complete the road to Damascus, including the Novellus Speed and Sequel systems. They provide the final deposition components needed for copper interconnects. The multiple dielectric process steps, needed to etch and form the various intermetal dielectric layers, are also performed by these systems. Dielectric layer constants as low as 3.5 can be achieved with fluorinated HDP layers. The system can also deposit silicon-dioxide intermetal dielectric layers and silicon-oxynitride anti-reflective layers. Specialty films, such as copper diffusion barriers and hard etch masks, can be deposited as well.

Although the new copper technology can eventually reduce manufacturing costs, the equipment won't come cheap. Base prices for the Inova and Sabre systems start at about $3 million.

For more information, contact Novellus at (408) 943-9700, or on the web at www.novellus.com.; Lam at (510) 572-5577, or on the web at www.lamrc.com; and IPEC at (602) 517-7217, or on the web at www.ipec.com.

Dave Bursky



The process fixture and cell design developed by Novellus Systems keeps the wafer's backside dry during electroplating, eliminating backside copper contamination. It also provides an edge exclusion to the plated film and copper seed layer, which eradicates buildup at the bevel edge.

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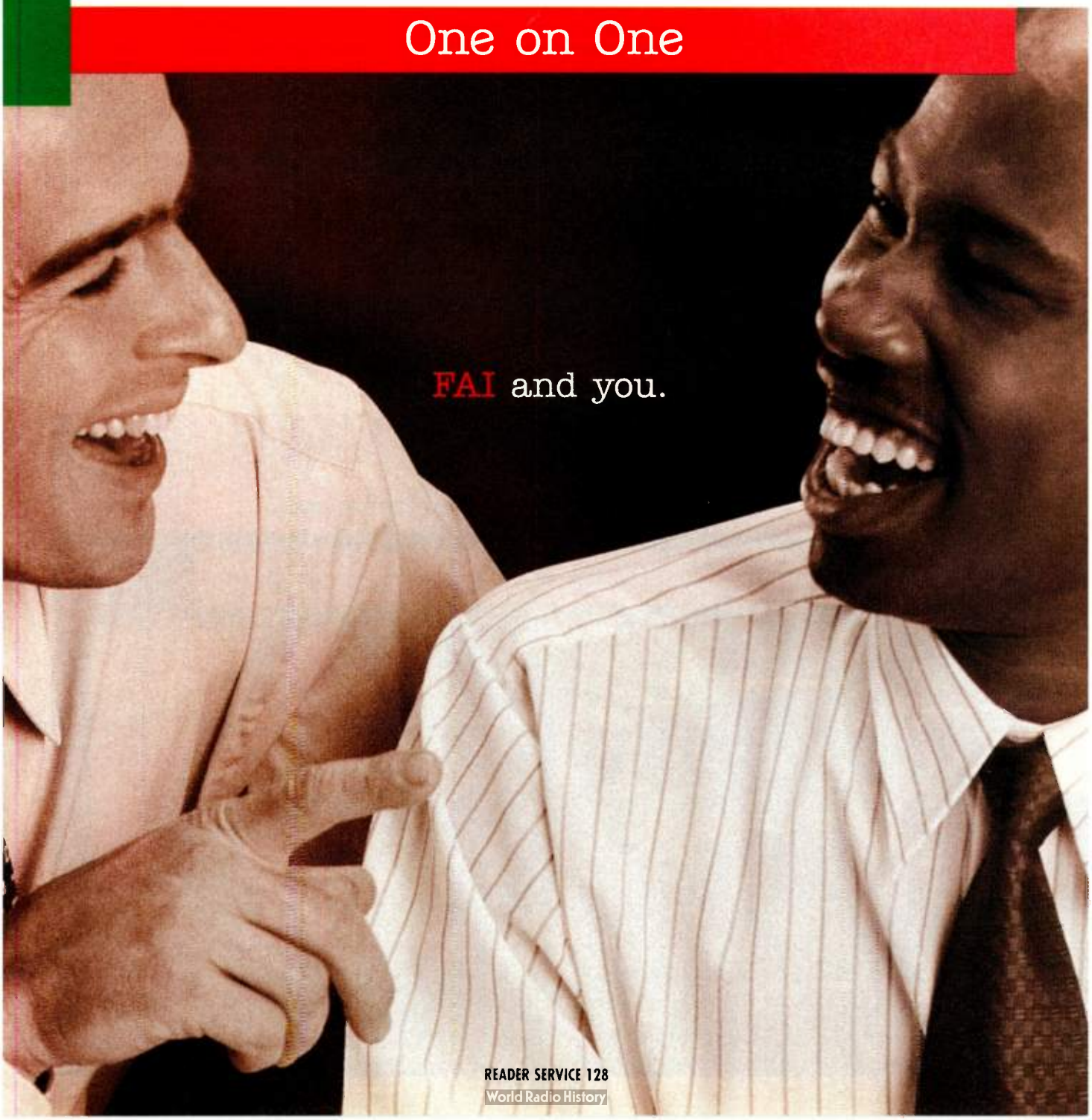

READER SERVICE 128

Test And Data On MEMS Failures Clear The Way For Mainstream Use

Why do microelectromechanical systems (MEMS) fail? Until recently, there has been very little information about failures of MEMS. But a team of researchers from Sandia National Laboratories, Albuquerque, N.M., hopes to change this by uncovering new information about the constancy of MEMS devices, and by using real data to finally answer that burning question.

To accomplish these goals, the researchers devised instrumentation known as SHiMMeR (Sandia high-volume micromachine measurement of reliability). Although predictability testing was previously possible, it was typically done on a small scale, looking at just one, two, or three devices at a time. Using SHiMMeR, researchers can now test up to 256 parts at a time.

SHiMMeR is a Plexiglass enclosure that contains a base for testing MEMS parts, and a high-powered, optical microscope and video camera to observe and record the failures. Each MEMS device under test is attached to a cable that sends it an activation signal when the testing begins. During testing, the humidity in the test enclosure is controlled by the operator. Researchers use the optical microscope to observe the operation of the micromachines.

Once a micromachine breaks, it is removed from the test structure, and a cross-section through its gears is taken using a focused ion beam. The cross-section is then observed through the microscope. Using this technique, researchers can draw conclusions about what makes a MEMS device fail, as well as when and where failures will occur *(see the figure)*.

As part of the team's efforts to determine micromachine reliability, members focused on adhesive wear as a major contributor to MEMS failures. Adhesive wear occurs when parts in a device rub together causing small pieces to rip off. These pieces attract and stick to each other, particularly in high-humidity environments, resulting in regions where the micromachines begin to catch and fail.

A Picture Develops

After intensive study of this failure mechanism, and over a year and a half of testing and compiling data on SHiMMeR, researchers began to arrive at a picture of micromachine failure which was drastically different than what they had originally predicted. The commonly held belief was that polysilicon, the material from which micromachines are made, is very brittle at micron-size dimensions. Therefore, most reliability concerns centered around material fractures.

The Sandia team discovered that, in reality, microengines don't malfunction due to polysilicon fractures, and that the polysilicon at these dimensions is actually extremely flexible and tough. As

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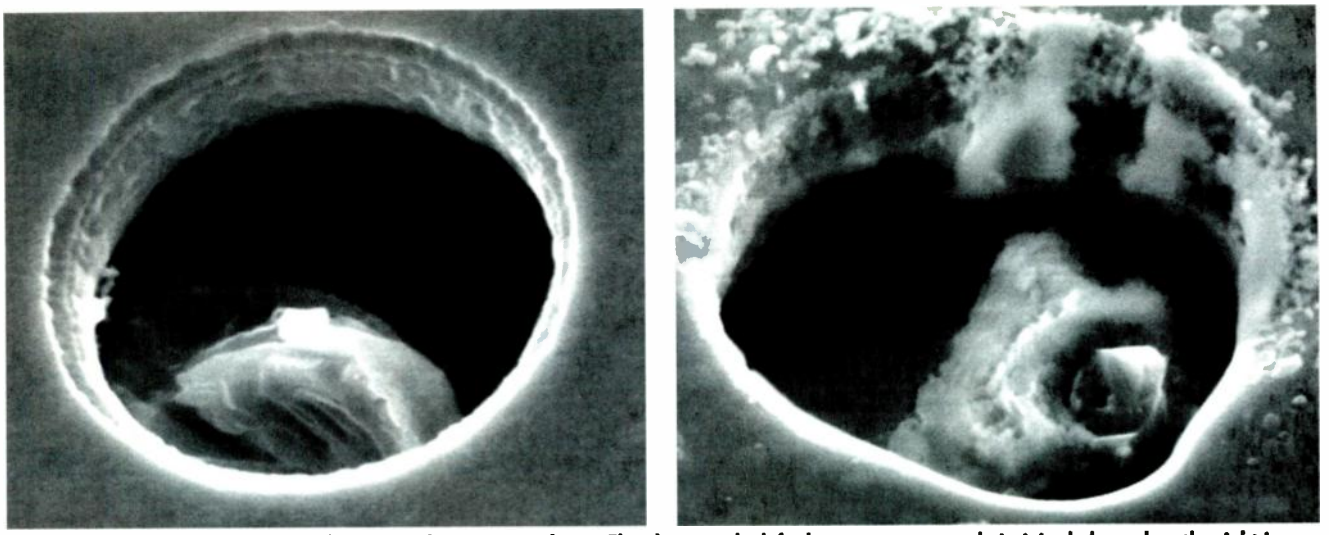

These images illustrate a failure mode in microelectronics machines. The photo on the left shows an unstressed pin-joint hole, and on the right is a stressed and worn pin-joint hole. The test technique uses a focused ion beam to examined the failed micromachines.

Bill Miller, manager of Sandia's Reliability Physics Department, explains, "We found that they fail by wear, much like a car engine fails without oil. The individual parts get so worn that they jam."

From this information, Miller developed a physics-based model that predicts when parts fail. The derived equation takes into account strength, adhesive wear, critical volume, pin-joint radius, applied force, resonant frequency, and quality factors. The results derived from the model match the actual results from the physical testing. With this predictive model, MEMS reliability may now be tested without waiting the days, weeks, or months that it typically takes for parts to fail.

For additional information, go to www.mdl.sandia.gov/micromachine.

Cheryl Ajluni

Mail-Order Supercomputer Available For A Mere $150,000

It wasn't that long ago that if you needed a supercomputer, you'd be looking at a price tag of well over a million dollars. That's no longer the case. Scientists at Los Alamos National Laboratory's Theoretical Astrophysics Group in New Mexico have built one such machine, Avalon, using off-the-shelf ordinary PC components. It wears a $150,000 price tag. The machine, which can perform over 20-billion mathematical operations per second (BOPS), made the 315th spot on the Top 500 fastest computers in the world list, released at the Supercomputer '98 Conference in Mannheim, Germany.

"It is now possible for a small group of motivated people to design and build their own parallel supercomputer using off-the-shelf parts and easily available software," Los Alamos scientist Michael Warren says. Working with Warren to build Avalon were David Neal, systems administrator for Los Alamos' Center for Nonlinear Studies, and David Moulton and Aric Hagberg from the Mathematical Modeling and Analysis Group.

Avalon is built out of 68 high-end PCs that use the Alpha processor from Digital Equipment Corp., Maynard, Mass. These are connected by network switches from 3Com Corp., Santa Clara, Calif., similar to those found in a university department or small business. Each of the supercomputer's processors is an ordinary PC, using the same type of memory and disk drives found in a conventional computer.

Off-the-shelf hardware is only part of Avalon's success. Software, the hardest part of getting multiple processors to work together on the same problem, was an even bigger part of Avalon. The Los Alamos team used an open-source Linux operating system and other software they downloaded from the Internet. As Warren explains, "The key to Avalon's success lies in its software, and the most important part of that software is the Linux operating system, which can be obtained at no cost through the Internet. And, that is minor compared to its other advantages. In my experience, the reliability and performance of Linux has no peer."

"We got most of the parts for Avalon on April 10," explains Warren. "Three days later, the machine was computing at over 10 billion instructions per second." By the following Wednesday, which was the deadline for the Top 500 list entries, Avalon achieved 19.2 floating-point operations per second (FLOPS). The computer did not suffer a single hardware failure or operating-system crash on any of its 68 processors during six weeks of operation.

Initial funds for building Avalon came from the Center for Nonlinear Studies. Other funding came from the Laboratory Directed Research and Development program and the Theoretical Division. Avalon is part of a class or computers known as "Beowulf" computers built using off-the-shelf technology. They're named after a project begun by Thomas Sterling at the NASA Goddard Space Flight Center, Greenbelt, Md.

For more information, go to: http://cnls.lanl.gov.avalon.

Roger Allan

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READER SERVICE 134

Triple Half-Bridge Forms New Motor-Control Design

BCD-5 Process Integrates Power And Digital CMOS Elements On A Single Chip, Delivering Endless Design Possibilities.

Alfred Vollmer

COVER FEATURE

It sounded too good to be true. Most engineers doubted that the BCD-5 process would become a reality when it was presented in *ELECTRONIC DESIGN'S* August 5, 1996 isssue. At about that time, STMicroelectronics, Lexington, Mass., decided to integrate "smart-power" functionality. By using its BCD-5 process, the company made the functionality capable of driving more than 10 A, as well as logic functions like memories, microcontrollers and other elements, from the digital library on a single chip. STMicroelectronics has begun selling the first products produced through this process, and many other smart-power devices are about to start sampling.

A glimpse of the smart-power possibilities created by the BCD-5 process, as well as programs currently being designed, will be discussed later in this story *(see "A Closer Look At The BCD-5 Process Features," p.36)*. Suffice it to say, the technology allows the integration of high-density logic, analog circuitry, and power stages on the same chip. It can also integrate power transistors with a low drain-source on-resistance, or $R_{DS}(on)$, on the same chip. That's what STMicroelectronics did when they produced the L6400 power device, a 6-FET array providing three half-bridges *(Fig. 1)*. The L6400 is manufactured in a simplified version of the BCD-5 process in which the number of mask steps is reduced from 22 to 14, including three metal layers. This results in a significant price reduction, even though the product still exhibits all of the process' specific power functionalities.

Basically, this chip is a collection of six n-channel DMOSFETs without predrivers. It is particularly suited for driving three-phase motors, such as those used to drive disk-drive spindles. Although specifically developed for hard-disk drives (HDDs), it is also usable in DVD drives, printers, fax machines, copy machines, power supplies, audio amplifiers, switching regulators, or step-up regulators. The L6400 operates at 16 V, but large quantities of 25- and 40-V versions are planned for next year.

For many application-specific ICs realized in the BCD-5 process, the standalone L6400 could be the basic core element. The L6400 contains two complete half-bridges, each consisting of two power DMOS transistors and two intrinsic diodes for ESD protection. All drains connect with each other, resulting in a reduction of $R_{DS}(on)$. The connection is made via the substrate on the backside of the chip. At a gate-source voltage of 5 V, the maximum for the device, the $R_{DS}(on)$ of the pure silicon device is less than 30 mΩ—almost 50 mΩ, including the package.

"Sixty percent of the shipped component's overall $R_{DS}(on)$ depends on the silicon, 30% on the metallization, and 10% on other factors," states Laura Formenti, product marketing manager at ST's Data Storage Division.

To reduce interconnect resistance, ST uses two bonding wires between every individual connection on both the silicon's bonding pads and the leadframe. $R_{DS}(on)$, consequently, is also reduced through this process. The use of the bonding wires reduces interconnect resistance to about 15 mΩ. ST has

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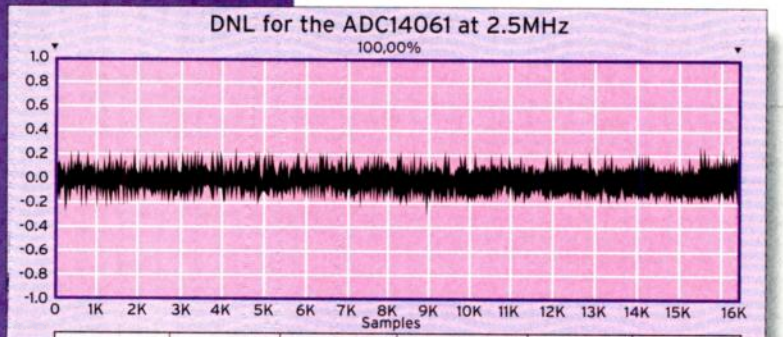

Part Number	Resolution	Conversion Rate	Power Consumption	DNL (LSB, typ)	Packages
ADC14061	14-bits	2.5MSPS	390mW	±0.30	52-TQFP
ADC14161	14-bits	2.5MSPS	400mW	±0.30	52-TQFP
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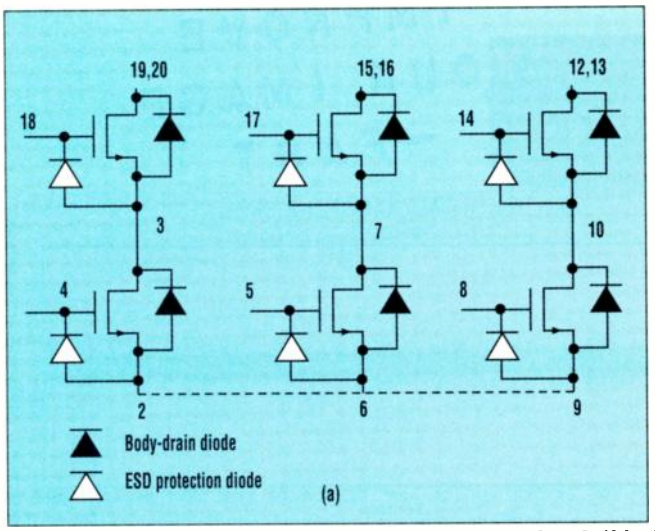
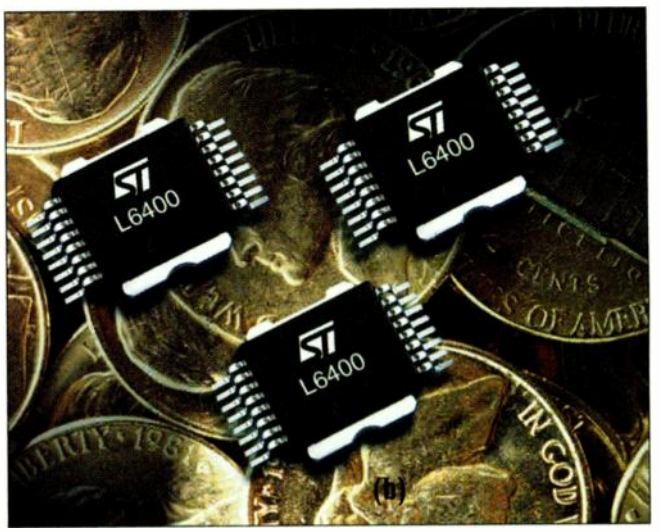




1. The STMicroelectronics L6400 is a single chip containing three half-bridges (a). It is capable of a typical dc drain current of 5 A (b).

also begun placing bonding pads inside the chip only, rather than at the edge.

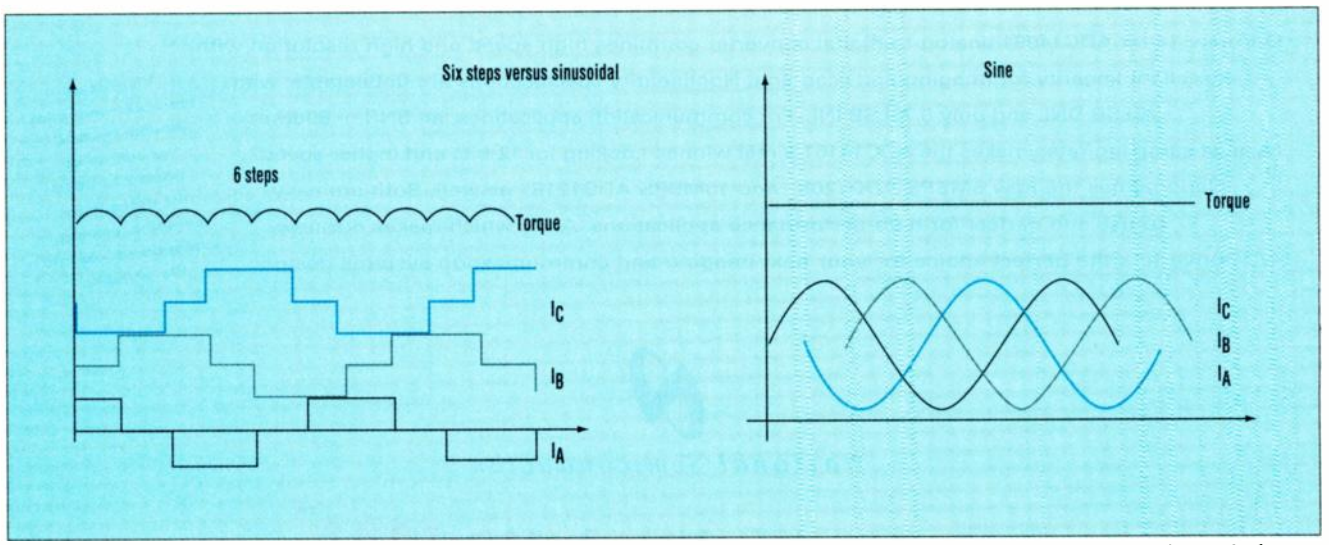
Maximum permanent dc current is about 6 A for each half-bridge, which means that 3 × 6 A can be controlled reversibly. In the saturation mode, it is even possible to switch a current of 100 A for a short time of 1 µs. Therefore, external efforts to limit power-on currents can be a lot lower.

"The L6400 is just one example of the power capabilities of the BCD-5 technology," explains Formenti. "It is also possible to add a 'brain'—e.g., a microcontroller with several kinds of memory—on the same power chip because the process is modular," she adds.

The BCD-5 process allows for a strong reduction in the area density of digital circuitry. Density is typically 3000 gates/mm^2. Because of this, ST is carrying out a special research program, focusing on the introduction of digital power processing (DPP) in power devices. The goal of this research is to replace analog circuitry with digital logic.

Aside from a reduction in chip size, digital designs also offer shorter design cycle times and significantly improved performance. The possibility of using automated design tools is what results in shorter design times. "We can completely simulate the device before starting the silicon design phase, because we can transfer the VHDL description of the digital circuit into an FPGA in order to emulate the chip," Formenti points out. Furthermore, it is possible to simulate and run the application using the FPGA in a customer's board. Once the functionality of the chip is approved, the silicon design phase starts. Debugging of digital logic is a lot easier than analog circuitry, and scan-test techniques may be applied as well.

Replacing analog circuitry with digital functions permits the designer to implement very complex filter algorithms. For example, by using DSPs and the appropriate software, adaptive control algorithms can be implemented. Moreover, when using a digital solution, no external components are required. Choosing a type of memory is just a matter of cost. Even though the implementation of, say EEPROM, makes a chip more expensive, overall system cost may be lower



2. Driving a motor with three sinusoidal waveform currents (right) instead of with square-wave currents (left) results in virtually ripple-free, constant torque. It also means less acoustic noise.

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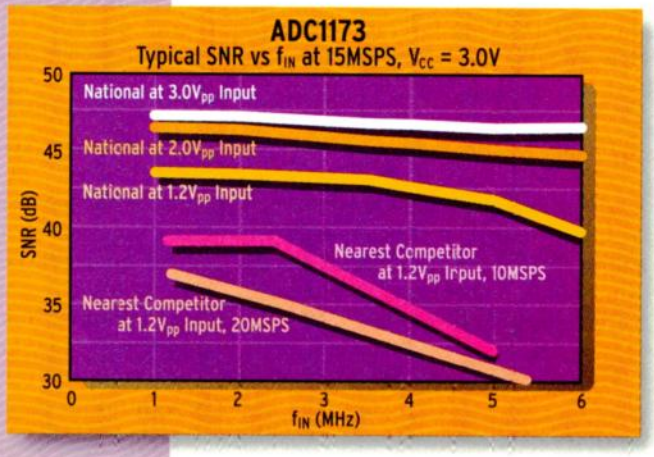

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because there's no need for an external component. This results in a smaller board space and increased reliability.

HDDs With Less Acoustic Noise

To understand how the L6400 array improves HDD designs, it helps to review some motor theory. The torque of a motor is defined by:

$$\text{Torque} = KT \times I_{MOTOR}$$

Controlling the current means controlling the torque, because KT is a motor-specific constant value. On the other hand, motor current is defined by the following function:

$$I_{MOTOR} = f(V_{MOTOR}, B_{EMF}, \Delta)$$

This means that motor current and respectively, its torque, are a function of the motor voltage, B_{EMF} (the electromagnetic force from the magnetic field), and Δ (the phase angle between the applied voltage and the B_{EMF}).

The "smooth-drive" solution is one of the new digital techniques developed by ST to control a HDD's spindle speed. "Since the implementation of smooth drive is mostly digital, using the BCD-5 process gives us high-density integration and allows us to integrate the power stage inside the same chip," comments Formenti. "No external components are required by this digital system, which means the solution is robust and system cost is low."

In today's most common motor-control systems, torque ripple creates a rate of change in the angular acceleration. This excites the mechanical assembly structural resonances and generates acoustic noise. In disk drives, most of the currently used three-phase, dc-control, brushless spindle motors are driven by six-step switched waveforms in which step commutations produce torque ripple. ST demonstrated this by applying three sinusoidal currents, spaced 120° apart, in the motor winding. The step commutations do not show up, resulting in zero torque ripple *(Fig. 2)*. A constant torque eliminates torque ripple, making it easier to follow the tracks in HDDs. It also significantly reduces the acoustic noise generated by the motor. The noise reduction comes from a decreased mechanical vibration which, in common approaches, is generated by the changes in torque.

To verify smooth drive performance in terms of acoustic noise reduction, ST made some acoustic measurements. For a commercially available eight-platter HDD, rotating at 10,000 rpm and driven in the smooth mode, ST discovered that acoustic noise is significantly reduced from 45.7 dB to 38.1 dB, compared with the common six-step bipolar drive mode. The optimum condition is achieved when the current is in phase with the electromagnetic force (B_{EMF}).

In contrast to common analog control of output currents, ST's smooth-drive concept uses a digital approach. The sinusoidal output current is formed by using amplitude modulation and a pulse-width converter.

This kind of motor control requires digital logic *(Fig. 3)*. In order to produce a really sinusoidal output current, a conversion table is stored in the memory of the control logic. This table contains specific voltage profiles for every motor, resulting in sinusoidal currents. To gain the relevant individual values of the conversion table, every motor-type's characteristics are sampled and then stored.

The sinusoidal driving approach used in the smooth-drive technique also allows reduced EMI. It is widely known that, due to high-order harmonics, sudden changes in the current produce EMI. Using a sinusoidal driving approach instead of the six-step mode significantly decreases EMI.

Because the digital-control blocks require just about 1 mm^2 of chip area, it's easy to use the BCD-5 process to integrate them into the L6400's triple half-bridge driver. This particular single-chip approach was put into silicon for a customer. It's not available as an off-the-shelf semiconductor product,

A Closer Look At The BCD-5 Process Features

The BCD-5 process is capable of handling maximum voltages in the range of 16 to 80 V. Other processes in the BCD family, without submicron structures, are capable of voltages up to 700 V. The 0.6-µm process is based on existing CMOS platforms, which means that existing digital CMOS blocks and nonvolatile memories can be reused and integrated on the power chip.

It's difficult to achieve a good compromise between density and lower resistance in the metal interconnects. Furthermore, power devices demand electromigration ruggedness. To optimize CMOS density requirements and the current-carrying capability of power devices, STMicroelectronics has replaced the third metal layer with a thicker layer. This thicker layer can carry high currents. The same technology steps, like those used in standard CMOS (e. g., tungsten plugs), are used to achieve the required CMOS densities.

Currently, STMicroelectronics is working on reducing overall resistance by optimizing the interconnections, which means changing the interconnect material—e. g., to copper. "Up to now, most efforts were made on the silicon," explains Dr. Bruno Murari, group vice president, dedicated products and R&D director at STMicroelectronics. "Today, the silicon is not the bottleneck anymore. Metallization, interconnection, and bonding are the bottlenecks which need to be improved" he adds.

For example, an LDMOS device for 20 V has an $R_{DS}(on)$ of 12 $m\Omega/mm^2$. But, the final component has about twice as much on-resistance.

Known as the "father of the BCD process," Murari predicts that, "In BCD-6, the silicon contribution to the overall $R_{DS}(on)$ will be reduced two or three times and it will be even more important to have a good metallization technique. The biggest problem is the bonding wire. In an audio amplifier device, for example, the cost of the gold material needed for the bonding wires is 25 cents for one single chip," he explains.

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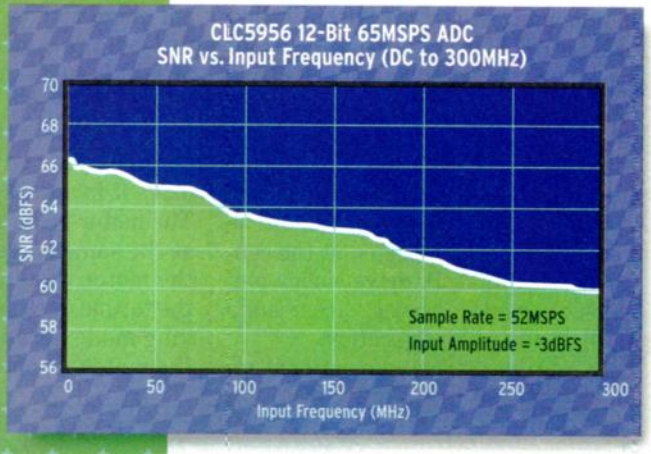

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but it certainly shows the process' possibilities *(Fig. 4)*.

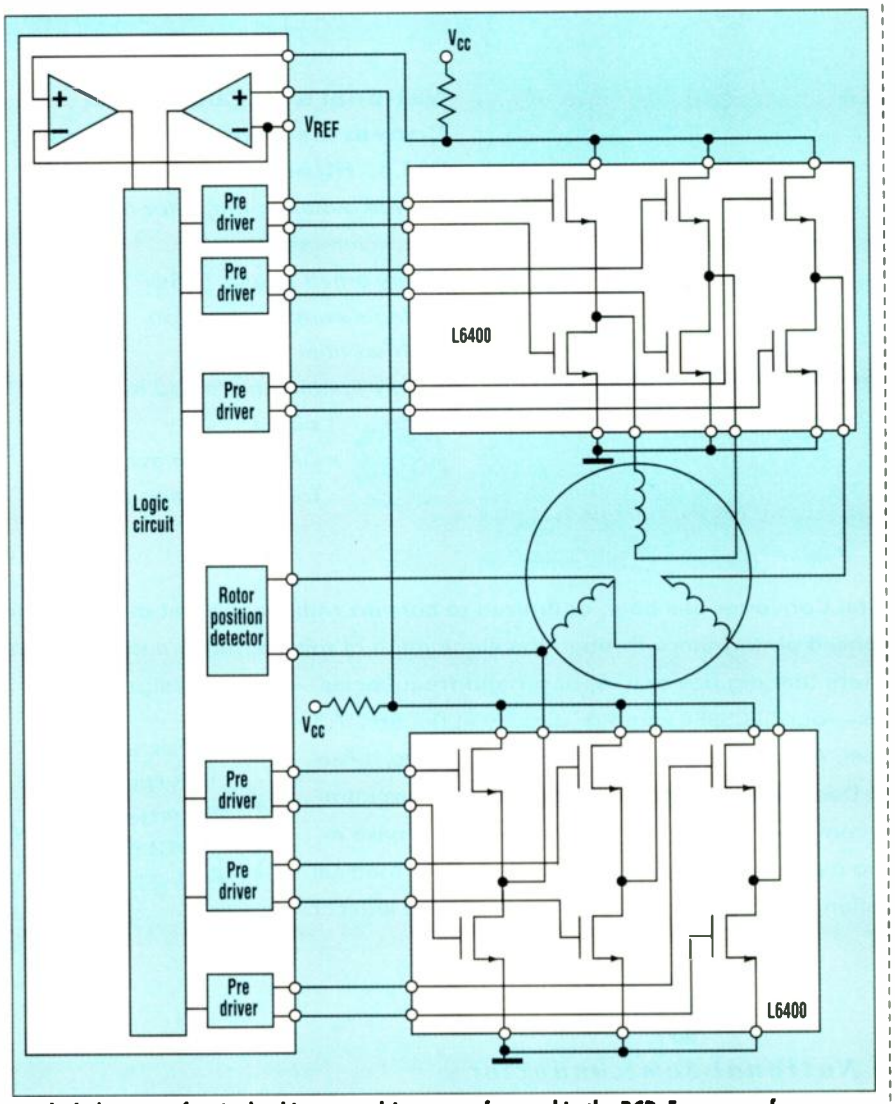
Increased Motor Speed

Another interesting driving technique for dc brushless motors, like spindle motors, is what ST has called "six by six." Normally, the three windings of such a motor are connected in a star configuration, which means that three terminals of these motors are wired out. The other three terminals are connected inside the motor. Quite often, this connection is wired out as well, and can be connected at the center tap terminal. To drive such a motor, six power transistors are needed in a half-bridge configuration.

In contrast to this conventional approach, the six-by-six technique does not have a center tap. All the terminals of the motor windings are wired out and driven individually *(Fig. 5)*. Therefore, such a motor has six wire terminals. For driving, it needs a power output stage with twelve transistors in a full-bridge configuration (one full bridge driving each motor winding).

Take a spindle motor, which is normally driven in the typical way. Disconnect the center tap in order to drive it in a six-by-six configuration. The motor generates the same torque at the same current flowing through the motor windings. This means that the torque does not depend on the driving mode because the torque (T) of the motor, as pointed out earlier, is a function of motor current.

Nevertheless, the six-by-six concept offers several advantages. The voltage dynamic range applied to the spindle motor is twice that of the traditional star-configuration drive. Each winding of a spindle motor driven in star configuration is applied to one-half the power-supply voltage ($\pm V_P/2$). While in six-by-six configuration, the dynamic voltage applied to each coil comprises the entire power supply range of $\pm V_P$.



3. Block diagram of a single-chip motor driver manufactured in the BCD-5 process of STMicroelectronics, which contains the L6400, as well as digital blocks. Combined, the sinewave lookup-table memory, the multiplier, the byte-to-PWM converter, and the 6-by-6 control logic require about 1.5 kgates for monolithic integration.

Moving Data Faster

The trend in HDDs is toward higher speeds of the spindle motor—e.g. 10,000 rpms—to allow for faster data-transfer rates and shorter access times. The maximum speed of a spindle motor is limited by the B_{EMF} generated by the motor itself. Once the maximum motor-driving voltage is defined, the maximum speed is determined by the B_{EMF}, which limits the current flowing in the windings. This B_{EMF} generates a torque that depends on the total resistive torque:

$$I_{MOTOR} = (V_P - B_{EMF})/R_{TOTAL}$$

where I_{MOTOR} is the current flowing through the motor. R_{TOTAL} is the total equivalent series resistance of the motor windings, plus $R_{DS}(on)$ of the power output stage.

In the case of a three-phase spindle motor with the center tap connected, B_{EMF} is set up by the vector sum of two vectorial (not scalar) phases. For example:

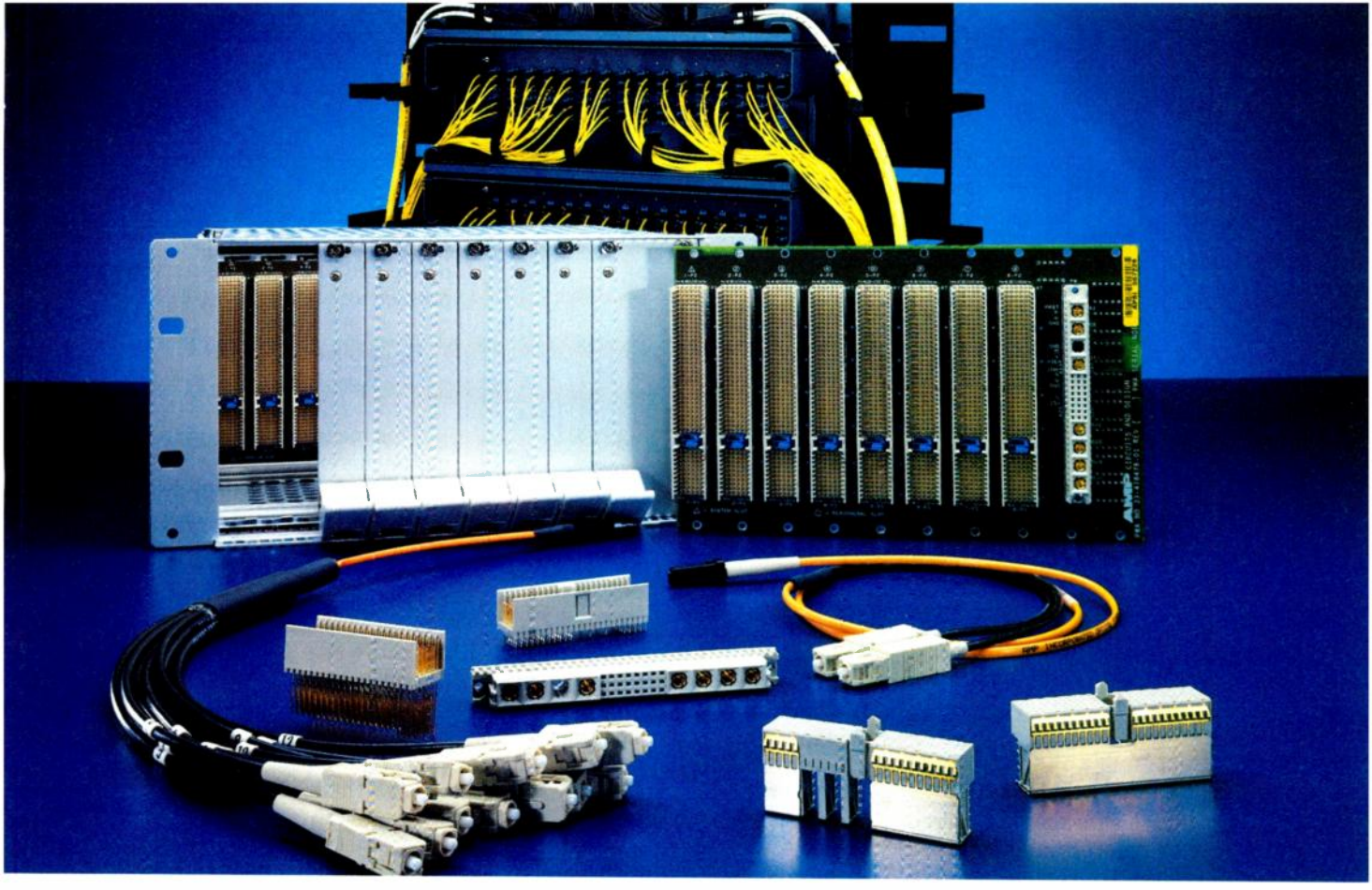
$$B_{EMF} = B_{EMFA} + B_{EMFC}$$

Typically, the power supply is fixed at 12 V ±10% for hard-disk applications. In order to increase the motor's speed, the B_{EMF} generated by the motor itself needs to be decreased. This can be achieved by reducing the motor's KT value because:

$$B_{EMF} = KT \times \omega$$

In this formula, ω is the angular frequency and KT is a motor constant. Together with the current, it determines total motor torque (T).

To reduce the B_{EMF}, it is possible to lower the typical motor constant Kt as the torque generated by the current in the motor winding. It may be ex-



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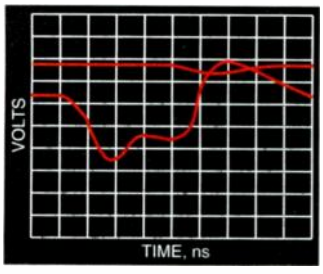

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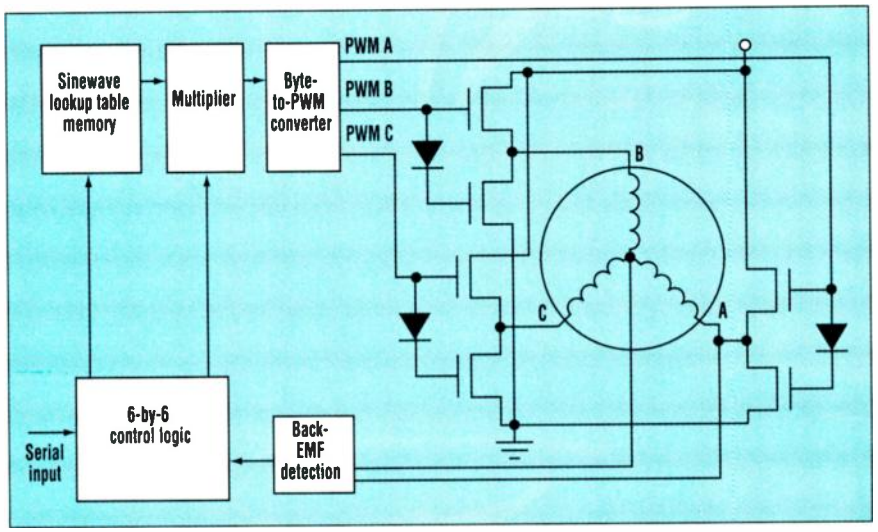


4. An example of a fully integrated motor-control circuit.

pressed as:

$$T = KT \times I$$

Basically, this means that current flow into the motor during startup must increase. It provides the total torque needed to run the motor whenever KT is decreased to reduce the B_{EMF}.

Today's common spindle motors, running at 7200 to 10,000 rpm, already require startup currents of more than 4 A. In terms of silicon integration, this requires output power stages with very low $R_{DS}(on)$.

In some cases, the silicon's $R_{DS}(on)$ is about the same as the resistance of the bonding wires. Furthermore, a current of 4 A requires packages with a low thermal resistance to manage all the power dissipated internally by the device.

The power dissipation is quite high, mainly during startup. This prerequisite is a big constraint in designing silicon drivers with low $R_{DS}(on)$ for these kinds of applications.

Without any modification of the motor's KT value, the six-by-six solution allows for a motor speed that's 70% higher than with a star configuration. This is made possible by the doubled dynamic voltage range and the independent driving of every winding. In fact, in six-by-six configurations, the total B_{EMF} limiting the current is only the B_{EMF} of a single phase.

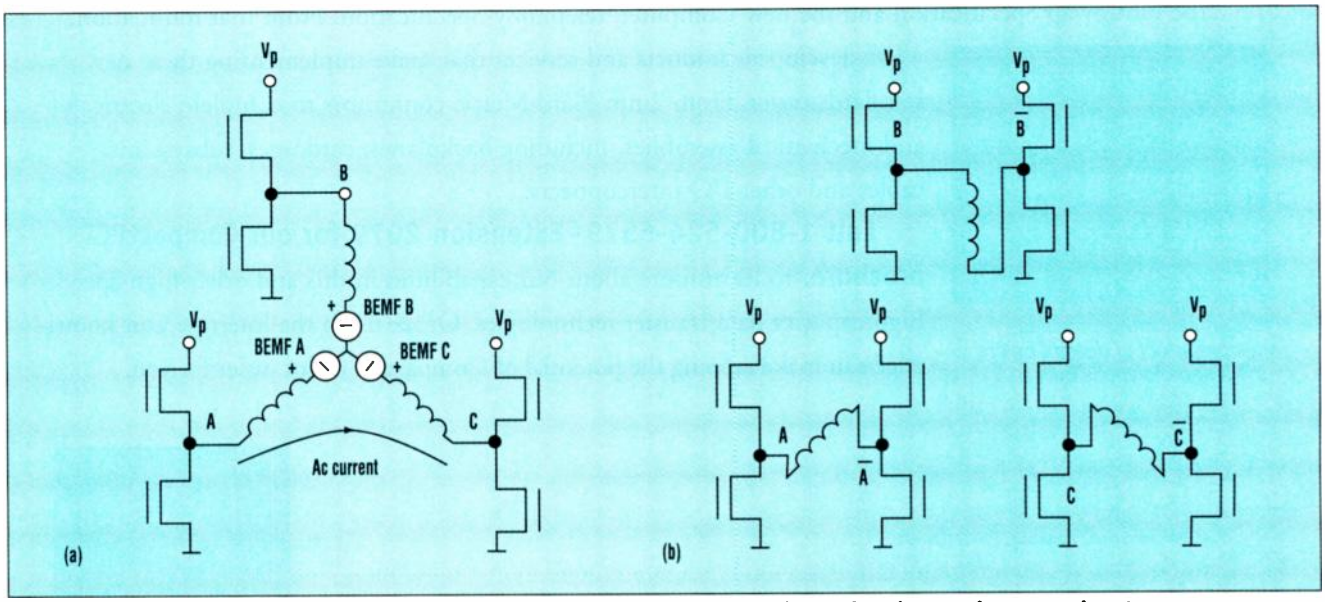
In a balanced three-phase motor, the relationship between phase-to-phase and phase-to-center tap is expressed as:

$$B_{EMF}\ \text{phase-to-phase} = \sqrt{3} \times B_{EMF}\ \text{phase-to-center tap}$$

This means the B_{EMF} limiting the motor current in six-by-six configurations is much lower than the B_{EMF} encountered in ordinary approaches. Therefore, the maximum motor spindle speed may increase by a theoretical factor of $\sqrt{3}$ (about 1.7) without changing the startup current or decreasing the $R_{DS}(on)$ of the power output stage.

"With the six-by-six technique, a motor is able to spin at speeds of up to 20,000 rpm," explains Formenti. Even though there is no need to decrease the overall $R_{DS}(on)$, the designer must integrate twice the number of output stages, which means twice as many transistors on the chip. To avoid a larger chip area, the $R_{DS}(on)$ needs to decrease again.

Driving a spindle motor with the windings in a star configuration, with a power stage operating in the PWM mode, power dissipation (P_D) of the device with a bipolar drive (exciting two phases simultaneously and leaving the third in the tristate) is expressed as:



5. Driving a spindle motor the traditional way (left) and in the 6-by-6 configuration (right). In the 6-by-6 configuration, there is no center-tap connection, resulting in the possibility of applying the entire power-supply voltage range to each of the individual windings.

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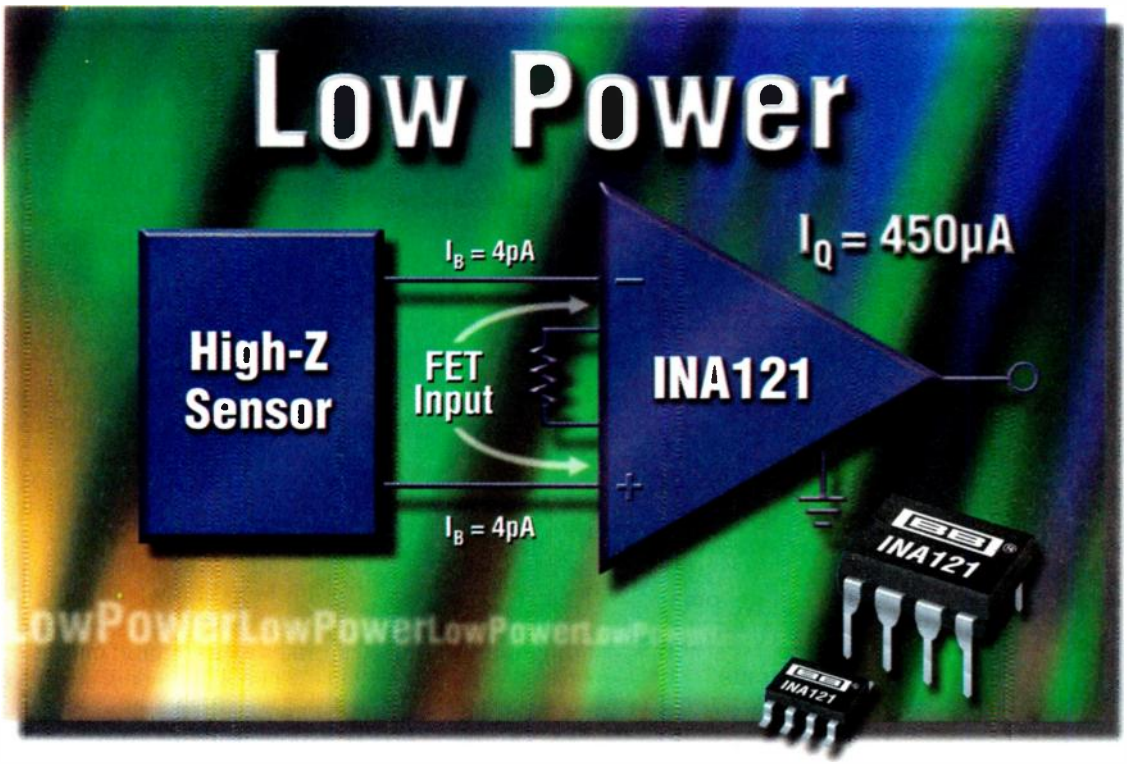

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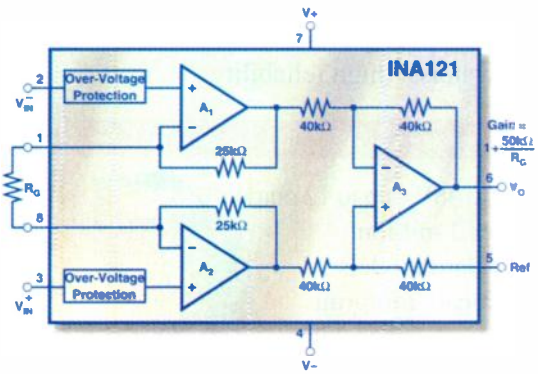

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$$P_D = 2 \times R_{DS}(on) \times I_{MOTOR2}$$

In a six-by-six configuration, each winding is driven independently, resulting in:

$$P_D = 4 \times R_{DS}(on) \times I_{MOTOR2}$$

To decrease the device's power dissipation, it's possible to use the six-by-six configuration, together with a PWM tripolar driving scheme, where each motor coil is driven by a current with a sinusoidal waveform. The phase shift between the motor coils is 120° each.

Power dissipation of the device now equals:

$$P_D = 6 \times R_{DS}(on) \times (I_{MOTOR2}/\sqrt{2})^2 = 3 \times RDS(on) \times I_{MOTOR2}$$

By combining the six-by-six approach with the smooth driving principle, it is possible to run a spindle motor at a speed that's 1.7 ($\sqrt{3}$) times higher than with conventional driving methods. Power dissipation rises by a factor of only 1.5.

The previous description was for increased speed with the same spindle motor. But, to use a different spindle motor, speed can be kept at a constant value. In a similar way, you can show that a device's power dissipation level is lowered by one-third if a bipolar driving method is used, or by 50% if sinusoidal currents are used for driving.

The silicon area of the driver chip decreases when the device's power dissipation is kept at a constant value. For this to happen, the on-resistance of every single element must be increased at the power stage.

In order to drive a spindle motor in such a six-by-six configuration, it is possible to use two L6400 devices. Or, use the BCD-5 process to integrate two L6400 devices, together with the control logic, in a single device.

Price And Availability

The L6400 is now available at a price of $1.50 each in 10,000-unit lots. Customer-specific products containing power and logic devices can also be obtained, as mentioned in this article's applications.

Contact STMicroelectronics, 10 Maguire Rd., Lexington Corporate Center, Lexington, Mass. 02421; (781) 861-2650; www.st.com; Laura Formenti, Italy, +39 39 603 64 61; fax +39 39 603 60 77; laura.formenti@st.com. **CIRCLE 504**

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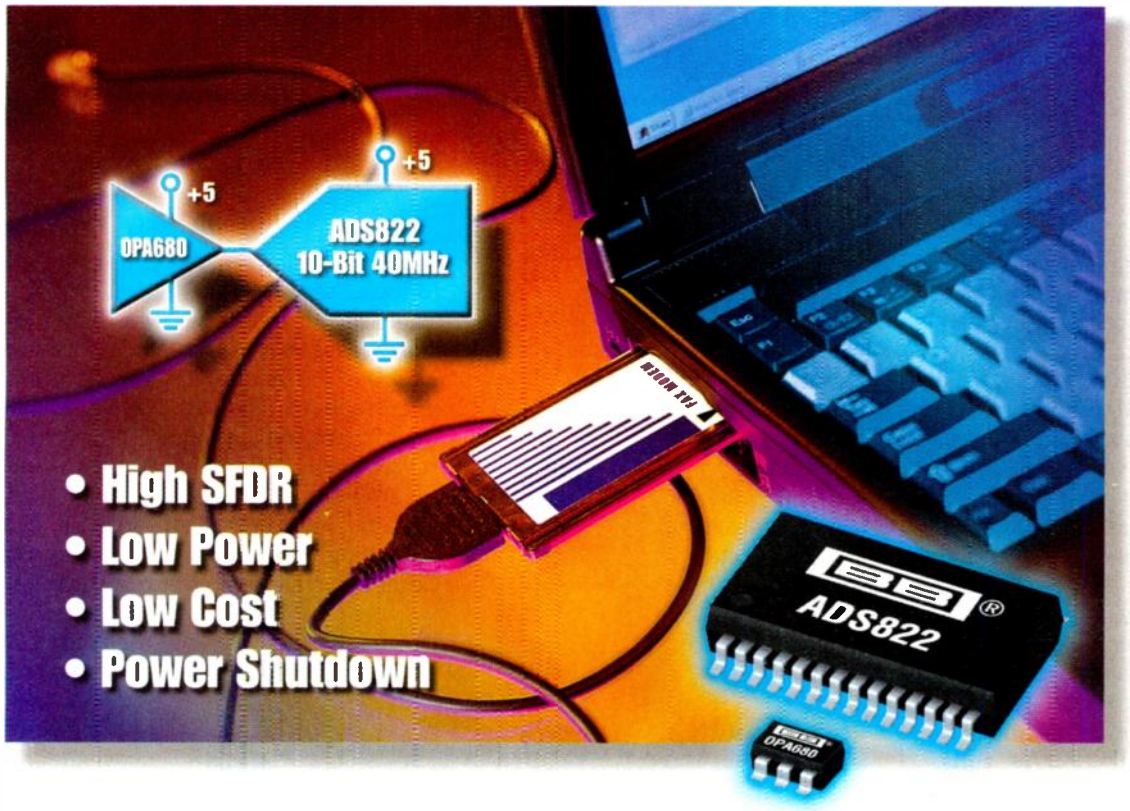

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Small And Mid-Size Flat-Panel Displays Heat Up The Mainstream

New Choices For Thin Graphics Displays Expand The Number Of Options Available For Designers.

Chris Chinnock

SPECIAL REPORT

Designers who use small, or mid-size, flat-panel graphics displays in their products can now expect to see several new technologies entering the arena. These include color reflectives, cholesterics, field-emission displays (FEDs), and digital audio/visual displays. In addition, display performance and reliability are improving through the use of multiline addressing techniques and chip-on-glass (COG) fabrication methods. These advances should soon be visible in a wide variety of consumer, industrial, and commercial products.

The small-to-mid-sized graphics segment is roughly defined as displays having less than 8.4 in. in diagonal. Such displays are used in personal information devices like PDAs, cell phones, GPS equipment, automobile navigation, and entertainment systems, along with countless other products. While laptop displays may garner most of the attention, the small and mid-sized graphics modules are becoming increasingly important to display manufacturers.

Art Courtesy: Sharp Corp.

Consider what is happening with reflective displays. Reflectives can save lots of power, space, and weight by eliminating the backlight. But until recently, no one had really figured out how to build a color reflective display with decent performance. Reflective twisted-nematic (TN) and super-twist-nematic (STN) LCDs have been popular in many cost-sensitive portable products, but they are typically monochrome, with limited gray scale.

But now, a host of display companies are promising new crops of color reflectives. Sharp, Toshiba, Sony, and Philips Flat Panel Co. are pursuing active-matrix LCDs (AMLCDs), while Hitachi, Casio, and Kyocera are choosing STNs. Epson America uses a matrix of thin-film diodes, and Matsushita appears to be evaluating both AMLCDs and STNs.

Setting the pace is Sharp, who has now begun production of a 2.5-in. AMLCD panel, and will soon follow it with 3.9- and 8.4-in. versions *(Fig. 1)*. These panels feature a 50-ms response, 10:1 contrast, a 260k color palette, and a 100° viewing cone.

One of the innovations they have developed is a microreflective structure which boosts reflected light from a conventional 5% to around 30%. This structure modifies the reflective surface of the LCD's back electrode to help it collect incoming light, and redirect that light back through the LCD, improving both contrast and reflectivity. Conventional reflective devices have a separate, laminated reflective layer placed in back of the display that produces a parallax effect. It makes the image appear to be floating above the back surface.

Philips, which showed 8.4- and 12.1-in. color reflectives at last May's SID '98 (Society for Information Displays) conference, thinks there's a need for color and real-time video response for portable products. Glenn Adler, Philips' manager for AMLCD handheld PCs, sees the development of front lights and touch screens as essential. "Customers want an integrated solution," says Adler, "but so far, I have not seen a really good front-light implementation." He believes games and Windows CE products are ripe for this technology.

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If most of the information to display is static, or needs only an occasional update such as maps or text, then a cholesteric liquid-crystal display (ChLCD) may be in your future. Kent Displays and Advanced Display Systems (ADS) are the principle suppliers of these reflective displays.

Cholesterics use a different type of liquid-crystal material that's stable in both on and off states. Once the image is written to the display, no further power is required to maintain the image—for hours or even

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- Low DLE 0.25LSB
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months. The technology is configured as a reflective display so no power-hungry backlights are needed. Furthermore, ChLCDs don't need polarizers, so they have a very wide viewing angle (180° cone). They also open up the possibility of using plastic substrates.

Kent Displays now offers a one-eighth VGA module (160 by 240 pixels) in yellow on black, white on blue, or green on black color combinations. The pixel pitch is 100 dots/in. and it takes 1.3 seconds to update the display. ADS is sampling a QVGA module (320 by 160 pixels) that has three color combinations, 200 dots/in., and 256 levels of gray scale.

1. Active-matrix LCD (AMLCD), thin-film-transistor (TFT), 2.5-in. flat panels like these from Sharp Corp. offer 50-ms response times, 256 colors, a 10:1 contrast ratio, and a 100° viewing cone. Following will be 3.9- and 8.4-in. versions.

With STN panels, a pixel typically switches between a fully on and fully off state. To achieve gray scale (variations in intensity or a color gamut), two techniques are used. In frame-rate control (FRC), the refresh time for the entire panel is divided into subframes. If a pixel is to remain in a light-transmitting state (white), it will not receive pulses in any of these subframes. If it needs the lowest light intensity, then it will be pulsed in all of the subframes to block light. If there are 16 subframes, then any pixel can achieve 16 gray levels.

The other approach is called dithering and can be used in conjunction with FRC. Dithering selectively turns adjacent pixels on or off, allowing the eye to spatially integrate the average intensity level to achieve gray scale.

Algorithms to control the FRC and dithering are usually contained within the display-controller chip set that every display needs to operate. The problem with these approaches however, is that flicker can develop with FRC if the frame rate isn't fast enough. Dithering can actually reduce the clarity of the display, causing text, for instance, to look a little fuzzy.

Three Five Systems has developed a multiline addressing technique they call LCaD (liquid-crystal active drive), which eliminates FRC and dithering algorithms. It addresses three rows (lines) simultaneously, instead of the standard sequential method.

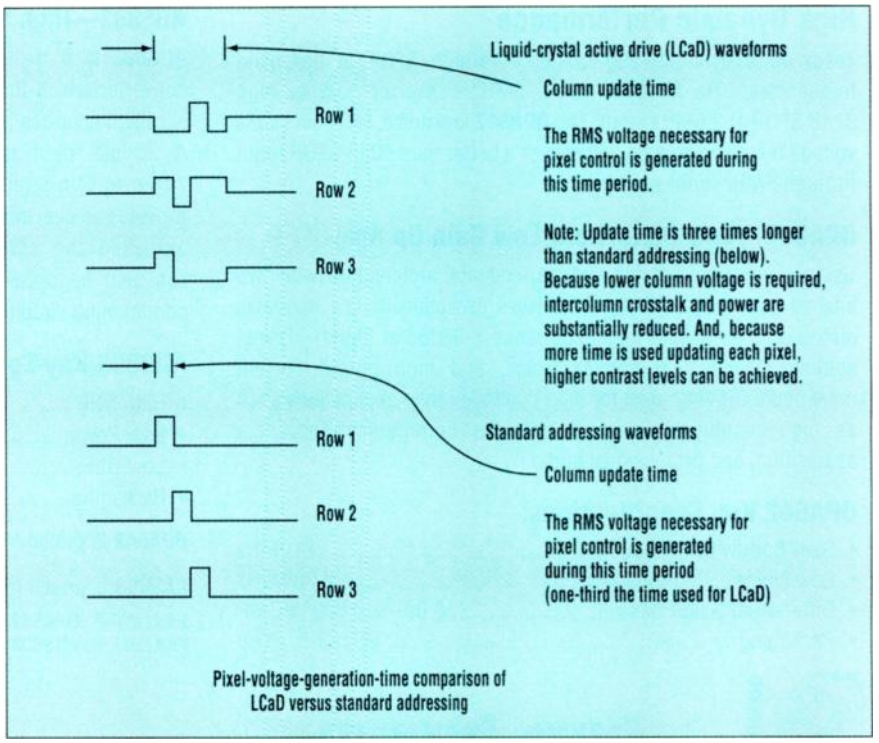
According to Michael Petera, director of advanced display concepts at Three Five, LCaD subdivides the multiline update time into four subperiods. A custom ASIC/controller within the display module, analyzes the selected rows to produce orthonormal signals for application to the rows and columns. Four amplitude-modulated voltage levels are applied to the columns during each of the four subperiods, within which various rows are selected. The combination produces 16 different gray levels *(Fig. 2)*.

Three Five Systems plans to sample QVGA (320-by-240-pixel) developer units with the new ASIC/controller by the end of this month. The pixels are actually updated faster, so the response time improves from 300 ms to between 60 and 150 ms. Also, lower drive voltages are used to switch the STN pixels, reducing crosstalk and power consumption.

The multiline addressing used by Optrex America also employs amplitude modulation, but addresses four rows at a time. In contrast, Sharp uses pulse-height modulation in conjunction with FRC and dithering in their multiline addressing technique. Their High-Contrast Addressing technology is currently available in a 12.1-in. SVGA (800-by- 600-pixel) color panel that can produce 262k colors (with an external graphics controller), a 40:1 contrast, and less than 2% shadowing.

Start To Think Digital

Most audio/visual (A/V) products,



2. LCaD (Liquid-crystal active-matrix) multiline addressing, developed by Three Five Systems, eliminates the need for frame-rate control and dithering algorithms (top). It addresses three rows (lines) simultaneously instead of the standard row sequential method (bottom).

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Key Specifications:

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like camcorders or handheld TVs, are designed to support analog-based video displays. Analog video signals are typically NTSC composite or RGB component. But the display driver circuits, which sequence data to the rows and columns, can be either digital or analog based.

For example, vendors such as Casio LCD Sales offer AMLCDs in 1.8-, 2.5-, 3-, 4-, and 5.5-in. sizes for pocket TVs and other handheld products. Purdy Electronics says they are seeing a lot of interest in their 1.8- and 2.5-in. color AMLCDs. All of these displays feature analog driver electronics, so no digital conversions or processing is needed.

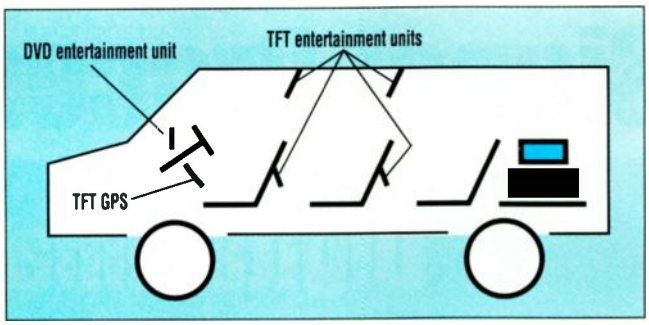
Epson America offers panels from 1.8 to 6.5 in., but the display features digital drivers. The drivers are used to control their on-screen matrix of diodes (instead of transistors) to control the light through the display. Now, analog video signals must be converted to digital before they can drive the flat panel.

"But," says Casio sales manager David Ross, "new products, like DVDs and digital cameras, produce digital outputs, so we are seeing more interest in digital interfaces." Many products have not yet adopted a complete digital interface, however. Ross notes that in their latest digital still camera, they convert the digital CCD signal to analog to drive the display.

"Keeping the signal all digital is less costly, and reduces losses that occur any time you change from analog to digital or vice versa," says Brian Platt, vice president at Purdy Electronics. "For the most part, digital drivers are in products larger than around 6.4 in., and analog drivers are in smaller-sized displays," Platt says.

Digital interface displays are now coming in smaller sizes, too. For example, Casio offers a QVGA display with a digital interface, and Epson offers a 1.8-in., 312-by-230-pixel panel that features 200 cd/m^2 of luminance, a 150:1 contrast ratio, and 262k colors. Analog panels are usually better at producing the wide array of colors associated with video, so digital panels will need to meet this performance level.

Interestingly, the automotive industry looks likely to adopt digital flat panels. This will consist not only of reconfigurable dashboards, trip computers, and GPS navigation systems, but also DVD-based systems that will serve up audio and video-based entertainment *(Fig. 3)*. "In fact," says Rob Harrison, the general manager of Hyundai's Flat-Panel Division, "the coming demand for auto-based information and entertainment systems has the potential to upset the supply-demand curve for AMLCDs. There could be over a million displays used in cars by 2002."

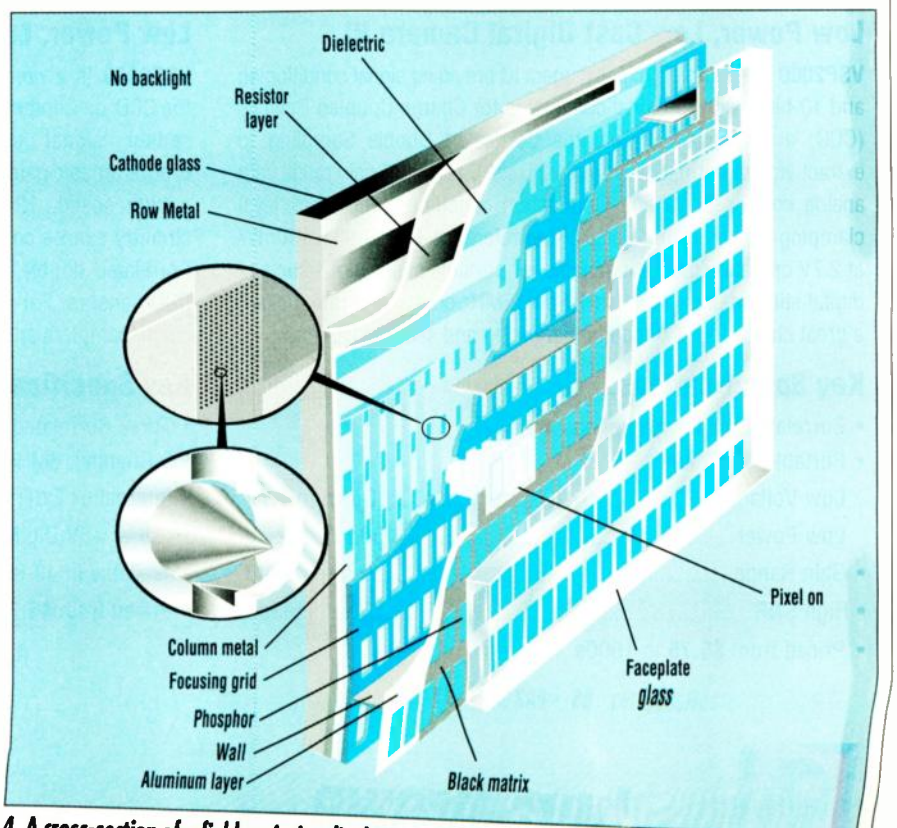


3. LCDs based on thin-film transistors (TFTs) are being supplied by Hyundai Electronics America for automotive applications. The displays can be found in GPS driver information systems and entertainment units. They can also be placed in car seat backs and overhead positions.

Hyundai currently sells STN panels to Mercedes Benz, BMW, and General Motors for instrument clusters, but is preparing an AMLCD in the 6-to-8-in. range that could flip-down from the roof for in-car entertainment. He notes that lots of displays are available in this size, but few companies have the experience to make both STNs and AMLCDs for the demanding automotive environment, where a wide temperature range (-30° to 85°C), shock, vibration, humidity, and corrosion protection are all needed.

Planar Systems is also looking at automotive and transportation markets as fertile ground for their electroluminescent (EL) displays. They recently introduced a new line of small graphics modules with the classic monochrome-green look; inherent, wide ter perature range; and rugged construction that's well suited to these applications.

On the LCD manufacturing front, a technology that has been around for a number of years looks like it is finally moving into standard, small to mid-size graphic products. It's chip-on-glass (COG) and, according to Seiko Instruments' product manager Don Feeney,



4. A cross-section of a field-emission display (FED), provided by Candescent Technologies, shows its elegant simplicity. It needs no backlighting.

A PENTON PUBLICATION

AUGUST 1998

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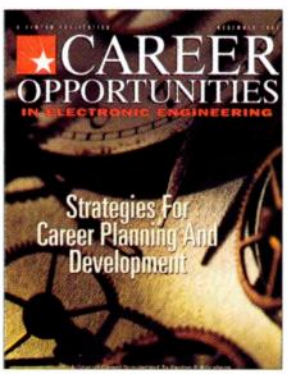

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Boosting Job Satisfaction By Defining And Pursuing Worklife Happiness

FIND OUT HOW YOU CAN TAKE STEPS TO INCREASE YOUR JOB SATISFACTION BY DEFINING YOUR JOB NEEDS

Lisa Hochgraf

According to one career expert, if you're 65% happy with your current job, you're doing pretty well.But what does 65% satisfied really mean?

"The whole idea of job satisfaction is a moving target, "says Robert " Lenburg, president of the Human Resources Group in Madison, Wis. "For many people, how satisfied they feel is a complex interplay of what's happening in their personal and business lives."

Job expectations also play into the elusive nature of job satisfaction.

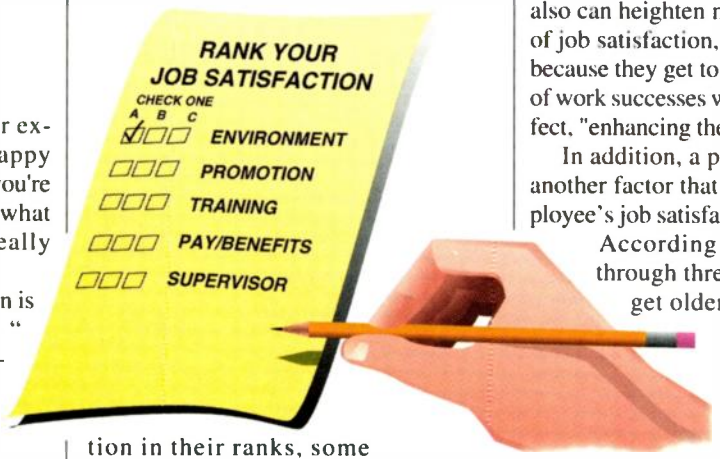
"People often ask me for an ideal job," says San Francisco career consultant Charles Prugh, who espouses the 65% satisfied standard."They describe all kinds of things that aren't going to exist. Jobs aren't Christmas presents. They're just work."

Despite the gray areas, taking a good look at what factors most often affect job satisfaction can help you understand your own situation. An examination of career stages can give you some guidance as to when and what changes might be warranted. Today's employers are offering programs to try to help. But, at the end of the day, individual engineers appear to have the ultimate responsibility for their own job satisfaction levels.

SOURCES OF SATISFACTION

Some job factors impact the satisfaction levels of most employees; others are particular to "knowledge workers," including engineers.

To find out the levels of job satisfaction in their ranks, some companies administer employee surveys such as those done by Organizational Skills Associates (OSA), a management and organizational development company based in Madison, Wis.



The surveys ask how people feel about their supervisors, how they rate their work environment, availability of promotions and career training, the level of information exchange, and the pay and benefits package, says Bob Morris, president of OSA. These factors are all part of overall job satisfaction.

Interestingly, the most common sources of satisfaction have changed somewhat in recent years. "It's no longer tied to things like company loyalty," Morris says. "You don't see very much of that anymore. People are loyal to other people. A lot of their satisfaction is tied up in the people--colleagues, supervisors, and so on."

In fact, studies show that an employee's direct supervisor has the most influence on whether he or she finds a job satisfying, says Lenburg. Working with a manager who "understands" them, and gives them some choices in their work lives, tends to improve the satisfaction level of most employees.

"Everyone seems to respond very well to a heightened sense of control, " Lenburg says. "People tend to feel put upon and not valued when they are overcontrolled."

Being part of a highly recognized team also can heighten most employees' sense of job satisfaction, Lenburg says. This is because they get to share the good feeling of work successes with other people, in effect, "enhancing the positives."

In addition, a person's stage in life is another factor that will influence an employee's job satisfaction.

According to Prugh, people go through three main stages as they get older. In the 25-to-45 age range, they tend to be focused on "achieving things." In this age group, people may be most interested in their ability to learn new things, in the availability of promotions, and in adding lines to their resumes.

From 45 to about 65 years of age, people seem to pay more attention to stability, and to protecting the things they've developed, established, and earned. At this stage they may find satisfaction from working for a financially stable company, getting regular pay increases, and making contributions to their retirement fund.

Finally, after age 65, people focus more on finding "meaningful" work, where they feel satisfied because they're making a difference in the world, Prugh says.

Engineers may be impacted by many of these "general" job satisfaction factors. The ability to be creative and to have ownership of their work may be particularly important for them, however.

"Electronics folks have an even higher tendency (than most) to view themselves as independent contractors," Lenburg says, "not in the legal sense, but in loyalty and deep grounded commitment to their profession."

Even compensation and upward pro-

motions, often debated as motivation and satisfaction tools, appear to be less important to knowledge workers overall.

"Job satisfaction comes more from the technology they're learning," says Matthew Malvese, Sr., manager of the Boston, office of Setford-Shaw-Najarian Associates, a technical recruiting company. "People are willing to take laterals (horizontal job moves that don't necessary include a pay raise) to learn new technology."

BEGINNING-MIDDLE-END

The above discussion and the exercise explained in the box should help you identify what factors are important to your job satisfaction *(see "Defining Your Job Needs").* It's hard to define a formula to find out if an engineer is 65% "satisfied," but other, more intuitive measures may help.

For example, Prugh asserts that every job has a beginning, a middle and an end.

At the beginning of this cycle, during the job interview and the first few months of work, everything seems perfect. Both employer and employee are enthusiastic.

In the middle, employees learn the system, understand the people around them more fully, and find challenges. It's at this stage that engineers realize this may not be the one job for the rest of their lives, Prugh says.

Toward the end, engineers may start to think this about their jobs: I've heard all this before and the challenge is gone. "That's the time when you figure out that it's time to move on," Prugh says.

Some people actually let their dissatisfaction level get so high that they can't get out of bed in the morning to go to work. Prugh calls this stage--beyond the end stage--the "unreasonably intolerable" stage.

Different kinds of changes may assist engineers in pulling up their level of job satisfaction depending on which job stage they're in. For example, Prugh says, engineers in the middle stage of realizing everything isn't perfect may be able to raise their satisfaction levels by undertaking a special project or pursuing professional development or formal degree programs. Adjustments at this stage may only be "tweaks" to an engineer's current position.

Sometimes tweaking your job means being creative about how to incorporate skills that you already have, but aren't currently using, Prugh says. For example, if you think your company would benefit from offering a new product, but managers aren't moving forward, you may be able to blend your business skills with your technical expertise and influence the decision.

If you do carefully researched reports

Defining Your Job Needs

Charles Prugh of Charles Prugh and Associates, a career consulting group based in San Francisco, Calif., often encourages people who feel dissatisfied with their current jobs to try this exercise:

Take a blank sheet of paper and write across the top "I need ..." Then, list the things you're interested in having that would make you happier with your current job. After you make your list, consider which needs are most important to you compared to what your current position offers.

Here are some possible need statements to get you started. I need:

- more challenging assignments
- more exposure to new technology
- more recognition from supervisors
- more opportunities to express my point of view
- more opportunities to attend training
- more opportunities to move in the company, horizontally or laterally
- more opportunities to work alone
- more people interactions
- less rigid hours
- less stress and fewer deadline pressures
- the culture offered by a larger company
- the culture offered by a smaller company
- more vacation
- better medical benefits
- assurance of salary increases

The Supervisor's Role In Boosting Job Satisfaction

Research shows that managers have a big influence over their employees' job satisfaction levels, notes Robert Lenburg, president of the Human Resources Group in Madison, Wis. Here's a list of do's and don'ts for managers interested in maintaining a high level of satisfaction among employees.

Do

- Look at systems and remove artificial barriers, such as unnecessary reports, from employees' duties. This frees employees to give their best effort to important projects.
- Articulate a clear vision. "If we're not out there constantly pushing customer service, we can hardly expect our employees to," Lenburg says.
- Avoid badmouthing the company. Managers are not "social directors of the cruise ship," Lenburg emphasizes, but they shouldn't let their bad day take its toll on employees either.

Don't

- Take credit for what employees have done. Rather, look for ways to commend employees to senior managers and let employees know when you have done this.
- Pass the buck to another department or function. Encourage employees to take responsibility for the work if responsibility really lies in your department.

of how the new product will benefit the company, management just might go for it. By doing this, you'll reap the satisfaction of being creative, doing something new, and putting your skills to work. "If you want a change, go after it," Prugh says.

In the "end" stage and certainly in the "unreasonably intolerable stage," engineers may need more drastic change to raise their level of satisfaction. Sometimes this will mean a lateral move or a promotion within the same company; other times it will mean getting a job with another company; and, in more rare cases, it may mean needing to change to another career entirely, Prugh says.

Don't discount the idea of looking for new responsibilities with your current employer. "Sometimes there are options in the company that are worth exploring," Prugh says. "If you've been there a couple of years, they have an investment in you," and might go along with defining some new job responsibilities for you.

COMPANY OFFERINGS

Besides what engineers can do for themselves in terms of raising job satisfaction levels, they also might take advantage of what companies are offering. Many organizations across the country, especially those that employ knowledge workers like engineers, are definitely

How Do Your Needs Compare?

Data from the 1985 National Engineering Utilization Study supports the idea that engineers value creative, challenging work. This study is detailed in the article, "Individual and Organizational Factors Influencing Engineering and Utilization," by William K. LeBold, Purdue University. The full article may be viewed on the web at http://fairway.ecn.purdue.edu/~lebold/p385.txlb.

Rank Order and Percentage of Engineers Who Valued Various Factors as "Extremely" and "Very" Important to Them Personally and Characteristic of Their Present Jobs

	Valuable Personally		Valuable to Employer	
Utilization	Rank		%Rank	%
Challenging work assignments	1	96	2	56
Adequate motivation to perform well	2	93	7	45
Utilization of experienced engineers	3	92	4	54
Match between job requirements & capabilities	4	92	3	55
Good working environment	5	90	1	58
Utilization of education and training	6	86	5	52
Sufficient support technical personnel	7	85	8	45
Utilization of talented young engineers	9	81	6	47
Opportunity to work on long-term goals	9	79	12	32
Opportunities for on-the-job training	10	76	10	43
Sufficient support nontechnical personnel	11	69	11	39
Time spent on nontechnical activities	12	32	9	45
Technical				
Use of overall technical competence	1	94	3	59
Opportunity to avoid technical obsolescence	2	88	7	41
Adequate facilities in general	3	87	1	60
Opportunity to increase technical competence	4	86	5	45
Opportunities for professional development	5	85	8	37
Adequate computer facilities	6	79	2	60
Use of highest technical competence	7	76	6	43
Time spent on technical activities	8	76	4	48
High-quality career guidance	9	63	9	16

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making an effort to keep satisfaction levels as high as possible, Morris says.

Companies hope that making greater investments in team environments,creative incentives, and flexible work schedules will help them avoid the high levels of grievances, absenteeism, and turnover, which often accompany high levels of employee job dissatisfaction, Morris says.

Depending on engineers' assessment of their needs for higher job satisfaction, they may be able to tap into a corporate offering that helps.

For example, an engineer frustrated with a two-hour daily commute may be able to get permission and the necessary equipment to work from home.

Interestingly, while companies are investing a lot of time and energy into such potentially satisfaction-enhancing offerings, job satisfaction levels haven't really risen too much over the last 10 years, Morris says.

Morris attributes this stable level of job satisfaction, to a large degree,to increased workplace stress.

The stress Morris sees in today's technical workplace comes from the pressure to create ever-higher quality goods and services, to be more productive, and to keep up with other nations. In part, companies are investing in new satisfaction-enhancing programs to respond to this higher level of stress.

"If they're going to get to that level of stress, how are you (as a company) going to inspire people to look for a way to meet the standard of a raised bar?" Morris asks.

In addition to the stress, satisfaction levels may not be rising because sometimes the programs companies hope will help alleviate the situation are not being implemented correctly, Morris says. In many ways, the best thing that companies can do is offer knowledge employees real opportunities for growth and career development.

This is definitely good news for engineers with a real interest in developing their skills and expertise, Morris says. While most companies care and will try their utmost to help, engineers are eventually "going to be in charge of their own satisfaction levels."

***Lisa Hochgraf** is a Pittsburgh-Pa.-based editor specializing in career issues. She may be contacted via e-mail at: lisa@topnotchtext.com.*

Tips On Coping For The First-Time Manager

THE TRANSITION FROM EMPLOYEE TO MANAGER IS EASIER BY DOING YOUR HOMEWORK AND EFFECTIVE COMMUNICATION

LISA HOCHGRAF

"Oh my goodness, I can't fire anyone!"

Having to discipline, or even terminate, a subordinate is a tough job for any manager. But it's probably even more daunting for the first-timer.

To survive this and other management tasks that come with their new roles, management experts suggest that first-time engineering managers do their homework and remember that positive interactions with people--both inside and outside their departments--will be their ticket to success.

First-time managers can't put off developing the new skills they need. While they may need three to five years to become fully effective in their new roles, they will need to hit the ground running.

If things aren't moving "within a month," says Florence Stone, author of *The Manager's Balancing Act* (AMACOM, New York, N.Y.), "you're in trouble."

Doing some homework right away can help first-time managers feel more comfortable in their new roles, Stone says.

"The first few days, even before you meet the employees, organize your office," says Stone. "Get historical perspective by talking to your boss about his priorities, strategic plans, previous problems, and things to keep carrying (through)."

First-time managers also will be more effective early on if they make learning new "languages" a top priority, says Don Frey, professor of industrial engineering and management science at Northwestern University, Evanston, Ill. These languages include "finance," "marketing," and "manufacturing."

Frey cites an example of what he means. While working for former U.S. Secretary of Defense Robert McNamara, he had to learn the meaning of the finance term "internal rate of discounted cash flow."

"The concepts (in the languages of other departments) are easier than technical concepts" that technical managers regularly work with, Frey says. "But they've got to learn the words."

And don't be afraid to sign up for some training, Stone says. Make sure you're up to snuff on performance evaluations, how to develop teams, and time management. Many organizations offer excellent seminars as well as books and other resources to help people develop their management skills.

"Don't assume that because you've seen other managers work, you can get up to speed right away," she says, noting that what new managers hated in managers they worked for may be just what's needed in certain work situations.

As first-time managers are getting up to speed on the basics, they'll also need to really shift their focus away from technology and onto people. After all, being an engineering manager means knowing how to get technical things done through other people.

To become more readily accepted by the people who report to you, let them know what your expectations will be, Stone says. Setting expectations can start by doing homework on each employee and the group as a whole, then holding a series of individual meetings and, finally, calling a group meeting.

If your office is organized, you've already had a chance to review each employee's past performance appraisal. Next, Stone suggests meeting with employees individually and listening to what they have to say.

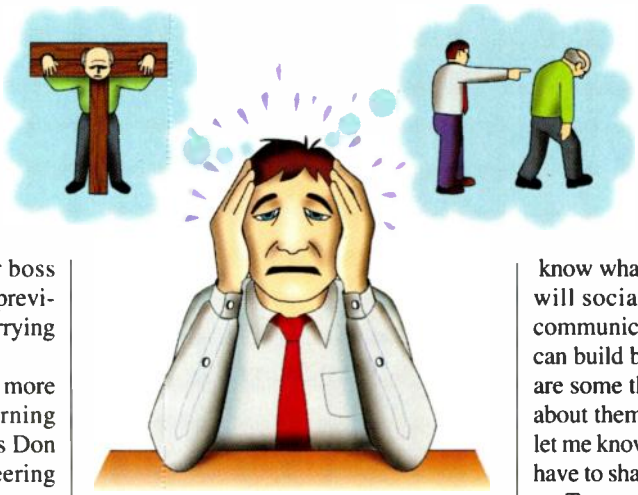
"Don't trust people right away; listen to them first," Stone suggests. "Don't make comments until you know where the bodies (of past problems and resentment) are."

These meetings also might be a time to talk with friends and enemies who are now adjusting to being your subordinate rather than your peer. Friends will need to know that you can no longer go out to lunch with them, but you can still be friends outside the office. Enemies will need to be told you want to get a fresh start with them; they need to be treated with the utmost professionalism.

After individual meetings, Stone says it's often a good idea to have another meeting with your reports in hand to further communicate your vision for the group.

"Most employees like to know what you want from them, how you will socialize with them, how you will communicate with them," she says. "You can build better rapport (by saying) 'These are some things I want to do and let's talk about them. Here's how I like to work and let me know if you can work with this.' You have to share your values."

Try to anticipate employees' responses,



Art: Tony Vitolo

Who? You?

Defining "Managment Material"

Sometimes technical people are named managers because they were recommended by their current supervisor. Other times, they are promoted because they are related to the boss. Still other times, they have been recognized as potential leaders.

Defining what makes someone a good candidate for promotion to manager is difficult, says Don Frey, professor of industrial engineering and management science at Northwestern University, Evanston, Ill.

"I can't define leadership, but I know it when I see it," he says, emphasizing the elusive nature of what makes a good manager. Still, he emphasizes, people skills and a broader vision of the project are usually far more important than technical ability.

Once the chief engineer for Ford Motor Company, Frey says he remembers technical meetings with technical project leaders who had a proven track record of leading technical employees and managing budgets, marketing, and manufacturing. As discussion went on about the progress of a particular project, he'd watch which "back row" technical people would contribute. Often, they were the ones who would be next up for a management slot.

These back-row standouts would demonstrate not only a grounding in the technology, but also an understanding of the bigger-picture issues.

"They can smell a problem and elucidate it, but not necessarily solve it," he says. Good managers "integrate technical issues with the size of the market, with cost-price positions and with how to distribute the product."

Stone says, and "have scripts ready" for addressing any concerns. "Speak honestly, don't bluff," she advises, but on the other hand, don't feel you have to make every decision on the spot.

It's extremely important (and sometimes very difficult) for new managers to trust their employees to do the hands-on technical work, Stone says. But this, too, will boost a new manager's rapport with employees.

To illustrate, Stone cites the example of two captains from the *Star Trek* television series: Kathryn Janeway and Jean-Luc Picard.

Stone says Janeway is a "lousy" manager, always involved in the technology that other people on the ship are more than capable of handling. Picard, on the other hand, knows how to delegate and say "Make it so." Taking a more Picard-like approach will help a first-time manager gain acceptance with the work group, Stone says.

In addition to managing relationships with the people in your group, first-time managers will want to nurture relationships

with other people in the company, putting their new skills in the language of finance, marketing, and manufacturing to work.

Frey estimates that good managers spend less than 50% of their time behind their desks because they're out "working the interfaces." A new technical manager needs to "go to the sales manager on the sales premises, get out from behind his/her desk, and get out into the work area" to develop the needed relationships, he says.

By doing so, a new technical manager will come to understand how the sales manager gets motivated, how the finance manager translates the budget and forecasts a project's financial position, and how the manufacturing manager handles labor pressures, Frey says.

"He's going to need those friends," he says. "At times, they (people) won't like what he's doing and he's going to need help.

Don't forget to build your relationship with your supervisor as well, Stone advises. "Find out what his/her strengths and weaknesses are."

In the development of a manager, some things must happen quickly. Others may take an entire career.

Soon after appointment, a new manager should have a vision of how the department should be operating, Stone says. Meetings with all employees should take place soon after.

Becoming an effective manager may take a few years, and perfecting your own personal management style may take 30, Frey says. As you develop a style, remember that though many strategies for becoming a better manager are the same for everyone, each person's approach to getting things done through others will be different.

"There's no cookie-cutter style," he says. "You could be humorous, serious, rigid, flexible. Everybody's different, but the results are all the same."

As you begin developing a management style, you may find it useful to read books on the latest trends in teamwork and flat-line organizational charts. Don't feel like you have to put the newest advice into practice unless you really believe in it, says Stone, pointing out that the latest management-through-teams rage doesn't work for everybody.

"Don't buy into all the fads, unless that is the way you want to work," she says. "Don't do it if you're not prepared to share decision-making. If it's not a democracy, say so."

If you're a first-time manager and all of this scares you, take heart, Stone says.

"We all get uneasy about something," she says. "A lot of new managers will be uneasy. Many problems (they face) will upset someone who's been in (management) for 10 years."

Once you've finished your homework on the administrative side of managing, you can begin focusing on the people, because they are the key to your success, says Frey.

Much information and know-how is stored away in people's heads for managers to tap on their way to success, he says. "That's what makes their places go."

Lisa Hochgraf *is a Pittsburgh, Pa.-based editor specializing in career issues. She may be contacted via e-mail at lisa@topnotchtext.com.*

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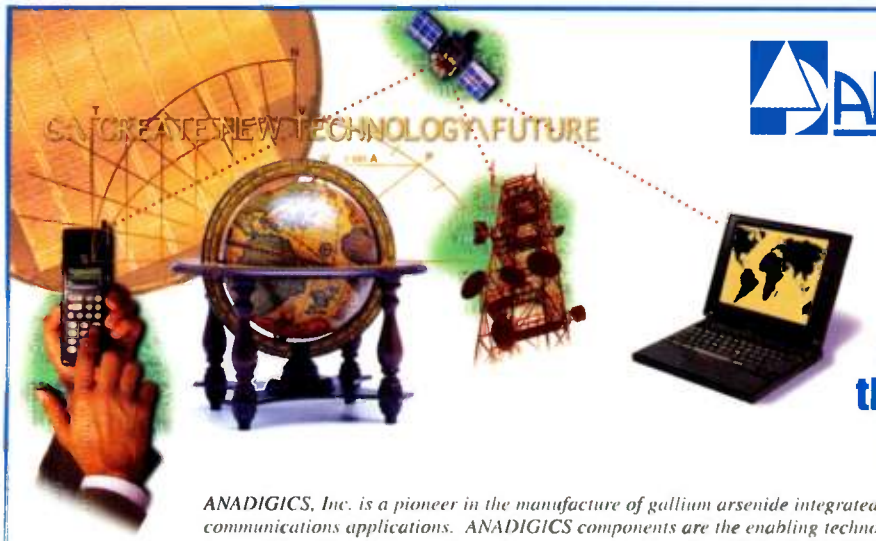

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COEE 98-115

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BSEE required. Must have 5-7 years in RF IC design (PA and/or receivers). Knowledge of RF tests and measurements and CAD tools essential.

Senior Engineer/ Manager Fiber Optic Applications
COEE 98-189

Provides support in the areas of applications, initial design-ins, marketing and engineering, including customer interfacing, data sheet responsibility, fixturing, application boards and plant/customer visits.

BSEE degree required. Must have 3 years experience in RF/High Speed Digital/Fiber Optic Transceiver IC design. 2 years experience in Board Level Fiber Optic Receiver/Transmittal Design and development is desirable. Good written and communication skills necessary.

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COEE 98-195

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COEE 98-188

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Senior RF Circuit Design Engineer
COEE 98-161

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BSEE or equivalent required. Must have at least 7 years of design experience and background in circuit simulation (i.e. Spice). Good knowledge of semiconductor physics and production/process methodology essential.

Design Engineer
COEE 98-187

Assists in device/circuit characterizations and circuit simulations within Fiber Optic Products segment; builds prototypes, test fixtures and tests/analyzes results with documentation; provides production support bringing up new products; implements new tests on engineering stations.

BSEE and 2+ years experience in RF testing required; optical test experience a plus.

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COEE 98-241

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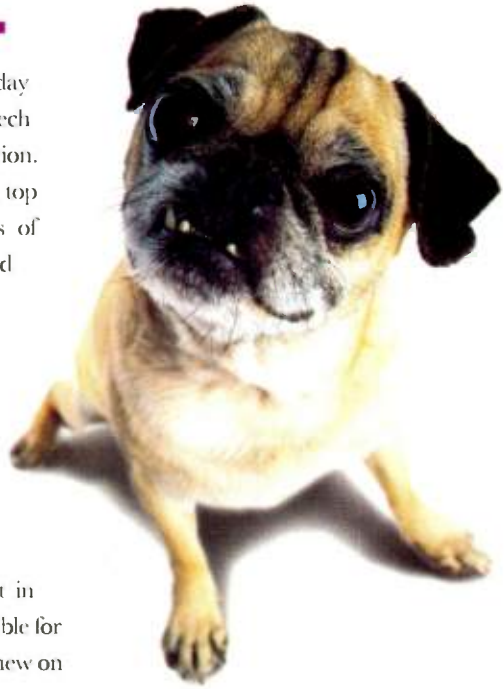

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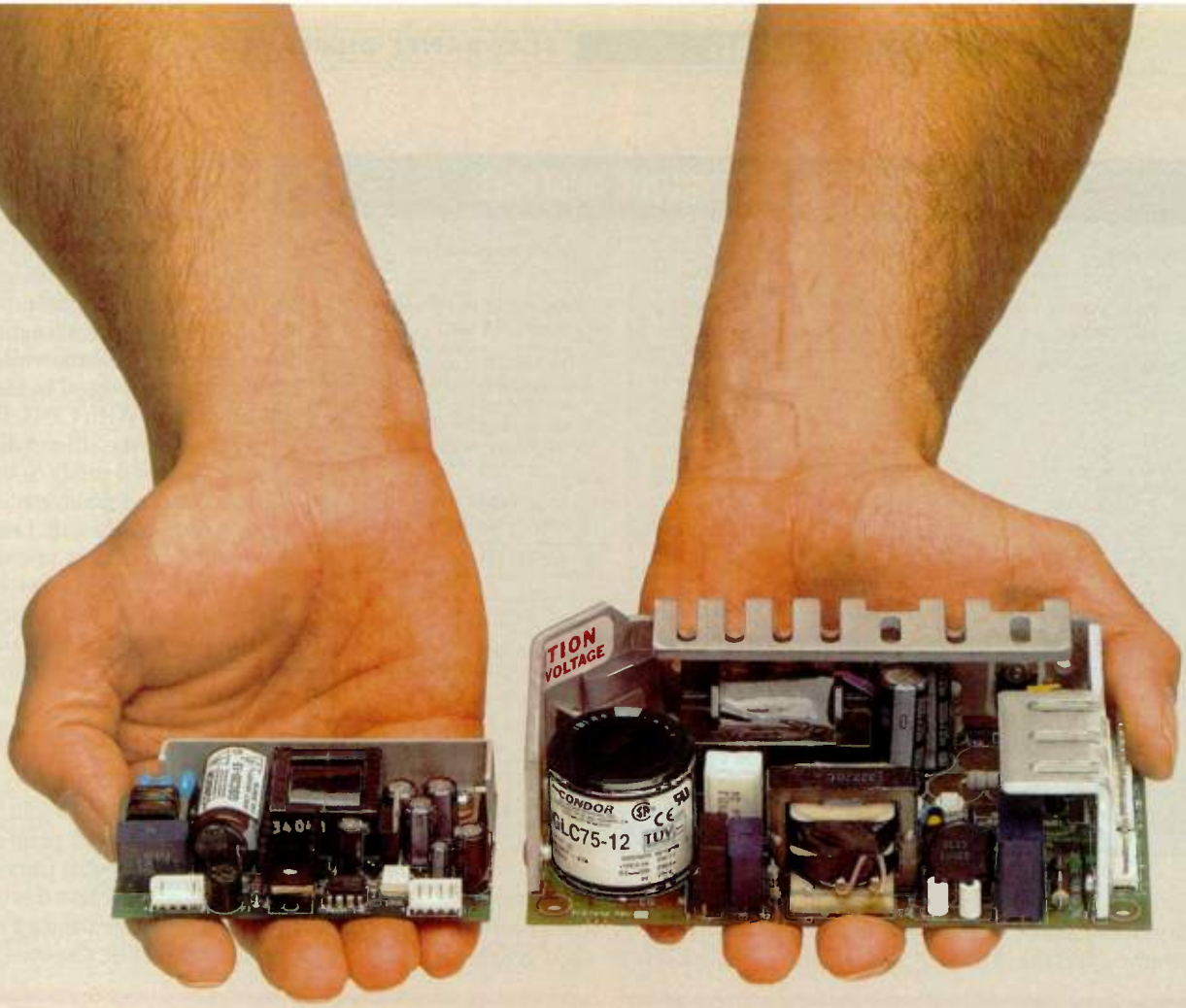

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CHIP-ON-GLASS TECHNOLOGY ANALYSIS

Features	Chip-On-Glass	TQFP construction
Ultra thin – Reflective – LED backlit	Less than 2.2 mm 5.5 mm maximum	Approx. 7.0 mm maximum Approx. 9.5 mm
Zero-insertion-force connector	1-to-18-pin connector	1 header pin connector slider to the pc board, in addition to either zebra strips or heatseals that provide the electrical interface between the LCD glass and the pc board
Light weight – Reflective – LED backlit	14 grams Approx. 26 grams	Approx.40-60 grams Approx. 55-85 grams
High contrast In reflective mode	7:1 typical	Approx. 5:1 typical
Power requirements	3.0 V at 10 mW	5.0 V at 25 mA
Lower cost	Eliminates peripheral components (i.e. bezel, interconnects, etc.); allows for a low-cost solution, when compared to other LCD technologies—$52 in 1k lots	Suggested resale for 1k lots of a 240-by-160 TQFP Module is $65-$80.

Source: Seiko Instruments
Information for the TQFP construction is based on industry standard parts utilizing products that have approximately the same glass size as the Vitrium G8 Chip-On-Glass display.

has only been available on graphics displays as a custom technology for high-volume customers (it is standard on many character displays). Now, Seiko has introduced what Feeney believes is the first off-the-shelf graphics display with COG as a standard assembly process *(see the table)*.

COG is a way to attach the display drivers that reduces space and weight, and increases reliability. In conventional processes, the drivers are attached to a small circuit board, which must be interconnected to the glass substrate. With COG, the drivers are bare silicon die, flip-chip bonded directly to the glass substrate using automated pick-and-place machinery. Due to the manufacturing set-up time, and the need for an integrated solution that includes a backlight, the use of COG has thus far been warranted only for high-volume products.

To move the COG process into the off-the-shelf realm, Seiko teamed with Lumitex to develop an LED backlight, part of a new 240-by-160-pixel display module. Seiko also provides an interface board that lets developers work with the display using a PC.

Casio's David Ross disputes Seiko's

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Osaka 569, Japan
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Motorola Flat Panel Display Div.
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Optrex America, Inc.
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Plymouth, MI 48324
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Philips Flat Panel Company
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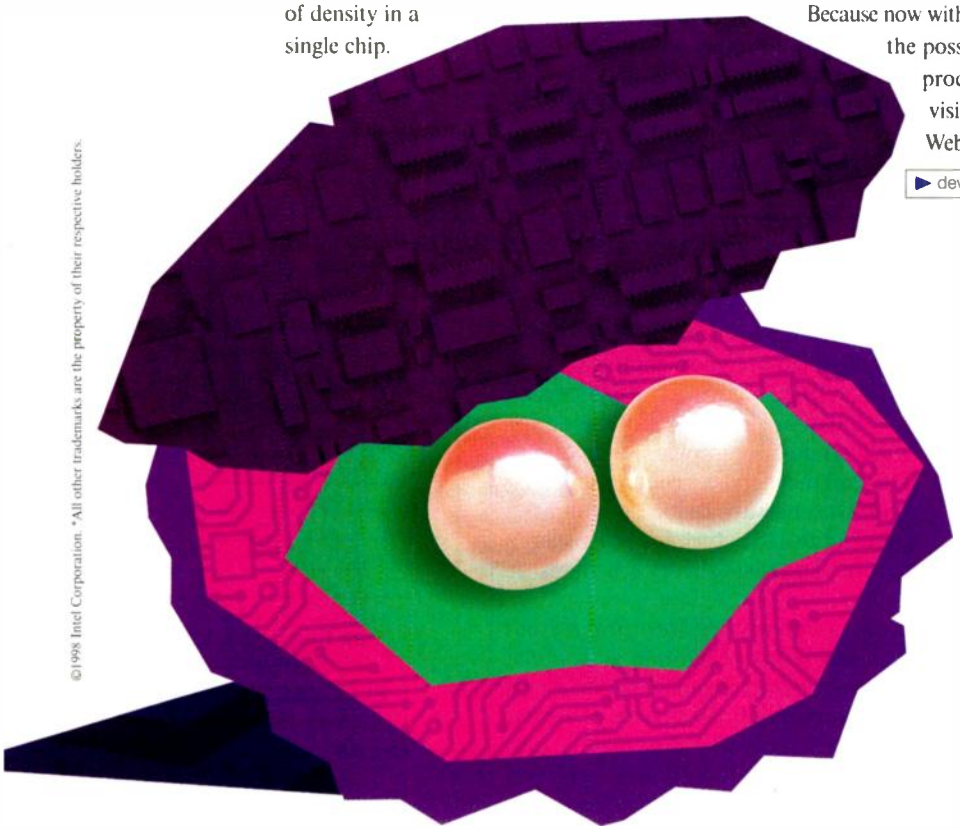

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"first standard COG graphics display" claim, however. He says they currently have a standard catalog QVGA display with COG drivers.

Hoping to challenge LCDs head on are field-emission displays (FEDs). FEDs use CRT phosphors, but provide a shower of electrons from an XY matrix of emitters *(Fig. 4)*. This means the displays can be quite thin, yet have the visual performance —wide viewing angles, the fast response times, and the excellent color gamuts—of CRTs.

For over a year, Pixtech has been selling monochrome displays for instrumentation applications, but the company has been having a hard time competing with STNs in terms of price. In June, however, Pixtech finally announced their first major product win—a portable cardiac defilbrillator.

Color FEDs are also coming from Pixtech, Motorola's Flat-Panel Division, and Candescent Technologies. By year end, Candescent will sample a 5.3-in. QVGA display, which they call a ThinCRT with 262k colors, 180° viewing, and about 100 cd/m^2 of luminance.

Motorola is sampling a 2.9-in., 512-color device for instrumentation applications, but is eyeing the automotive market for their 5.6-in. panel. That should sample in the third quarter, and offer a whopping 700 cd/m^2 of luminance, needed for legibility in sunlight.

"ThinCRTs must have excellent visual performance, but they also need to be cheaper and lower power than alternatives like AMLCDs," says Candescent's marketing manager Stewart Hough. "With some of the new technology we are integrating, we should be about half the power of a comparable backlit 5.7-in. AMLCD." To solve the price issue, the company is raising funds to build a high-volume plant to pump out a million 12-in.-equivalent displays/year.

Whatever your display needs for small to mid-size graphics modules are, there are more choices coming down the road. But, be sure to look beyond the specifications to determine the display's maturity and real delivery schedules.

Chris Chinnock holds a BSEE from the University of Colorado at Boulder, and reports on flat-panel displays and other emerging technologies. His company, Technical Marketing Service, provides writing, marketing, and public relations services to technology firms.

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SP4415	2.2 - 3	3	50nA	.5 - 2	1.5	112	256	4 selectable light levels
SP4422A	2.2 - 6	15	200nA	1 - 10	3	188	270	requires minimal board space
SP4423	2.2 - 6	6	200nA	1 - 10	2.4	170	800	low power operation
SP4424	2.2 - 5	8	200nA	1 - 10	4.4	216	114	dual oscillators for coil and lamp control
SP4425	1.1 - 2.2	32	500nA	.5 - 6	3.65	176	348	low voltage operation
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READER SERVICE 149

Hands off!

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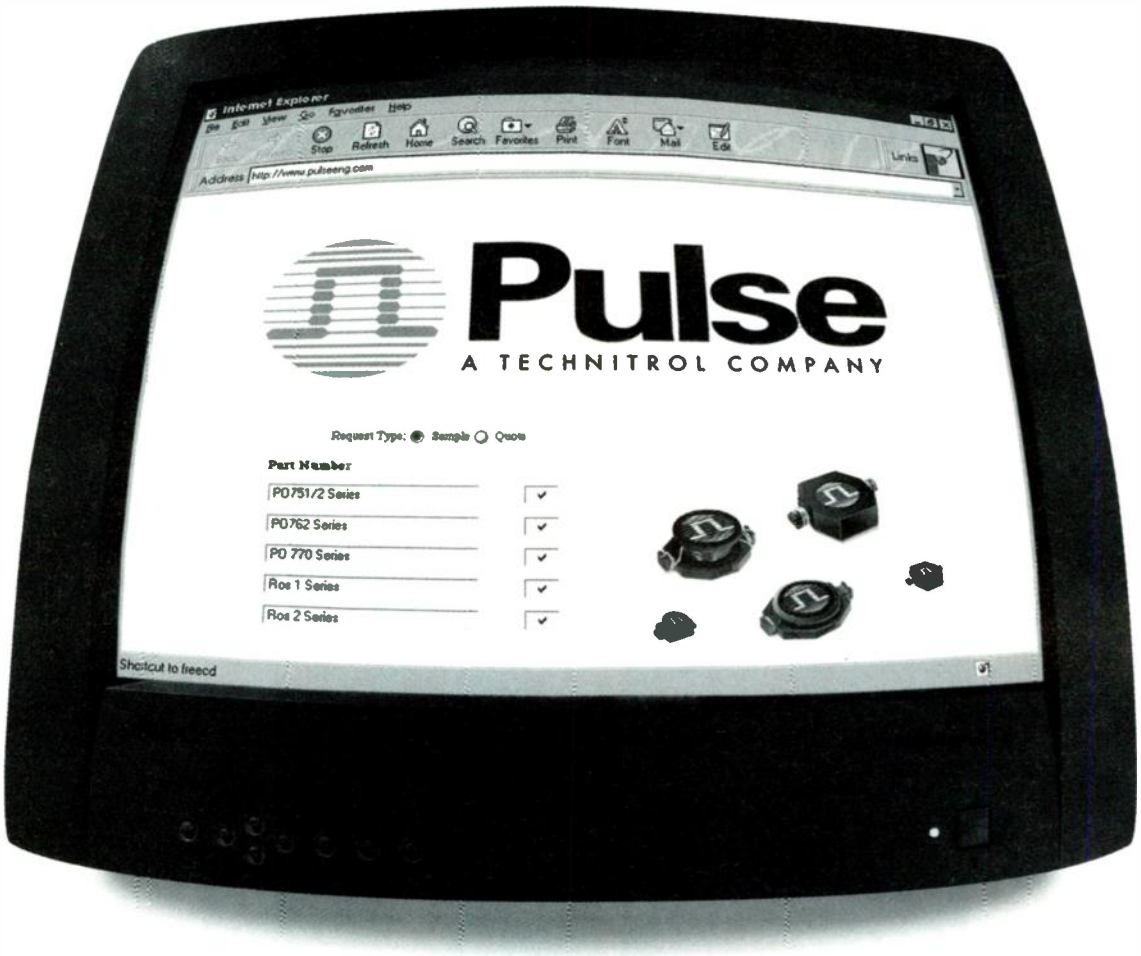

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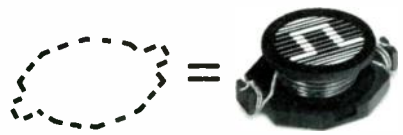

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READER SERVICE 144

CRYSTAL OSCILLATORS

Sample The Many Flavors Of Crystal-Controlled Oscillators

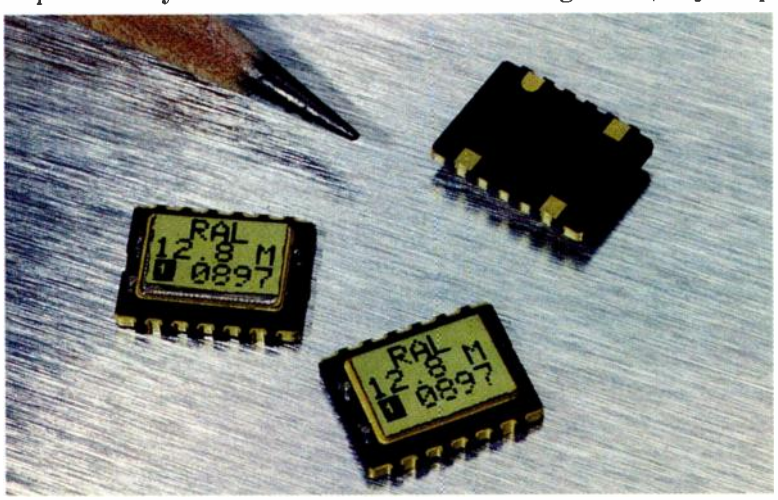
To Lower Phase Jitter And Raise Stability, Suppliers Look To High-Frequency, Fundamental Quartz Crystals.

Ashok Bindra

In the search for stability, precision, tighter tolerance, repeatability, and lower noise, designers traditionally turn to crystal-controlled oscillators. As a result, the suppliers continue to polish their wares to meet the ever-increasing need for higher frequencies with better performance from smaller packages at lower cost. Consequently, crystal oscillators (XOs) emerged in many varieties.

They've evolved from uncompensated, fixed-frequency XOs; voltage-controlled crystal oscillators (VCXOs); temperature-compensated crystal oscillators (TCXOs); and oven-controlled crystal oscillators (OCXOs), with outputs that can be CMOS, TTL, or ECL compatible. In addition, the number of variations in each category is on the rise. The recent trend shows a move toward digitally programmable and microprocessor-controlled XOs.

SPECIAL REPORT



Art Courtesy: Raltron Electronics Corp.

Speaking of higher frequencies, the conventional approach to designing crystal oscillators in the hundreds-of-MHz range has been the use of multiplication techniques such as phase-locked loops (PLLs) and analog frequency multipliers. However, these approaches bring with them their own set of problems like noise, jitter, reliability, instability, and so on. And, many emerging applications in telecom, wireless communications, instrumentation, and faster microprocessor-based digital systems, in fact, are seeking significant improvements in noise, jitter , and stability performance over time and temperature *(Fig. 1)*. To meet such stringent goals, XO manufacturers have developed oscillators based on fundamentally higher frequency quartz crystals.

Inverted Mesa

Valpey-Fisher Corp., for example, employs proprietary, chemically etched inverted-mesa technology to achieve lower-phase jitter from VCXOs that operate as high as 350 MHz. With this approach, the phase jitter is less than 1 ps rms. By comparison, PLL-synthesized crystal oscillators will offer up to 200 ps rms of phase jitter, according to Valpey-Fisher. In fact, the degradation in the phase jitter is determined by the square of the multiplying factor. Using analog multiplers, the degradation in jitter is even worse.

"Although, PLL-synthesized, higher-frequency XOs have cost advantages over oscillators based on high-frequency fundamental crystals, the difference is insignificant," says Valpey-Fisher's vice president, Roman Boroditsky. Plus, notes Boroditsky, "while offering improvement in phase-jitter performance, the design maintains all the mechanical properties." He adds, "phase jitter is a more useful specification to characterize short-term stability, because it provides a precise way to establish when a phase transition occurs."

Using the high-frequency fundamental crystals, the company has launched its VF596 family of very-low-phase-jitter with wide-pull-range oscillators in surface-mount packages. These oscillators offer frequencies up to 125 MHz for Gigabit Ethernet applications, and 155 MHz for fiber-optic communications. While the units up to 250 MHz are in production, the 350-MHz oscillators are only in the pilot-production stage The process is being tweaked for the production of high-performance, 350-MHz devices.

According to Boroditsky, although inverted-mesa-based, high-frequency fundamental quartz crystals were developed in the early 1990s, the demand for them has emerged only recently.

The call for such low-noise components has prompted many other key players to acquire such a process. Therefore, they'll be able to build oscillators controlled by crystals that operate at higher fundamental frequencies. Some of these suppliers include Champion Technologies Inc., Conner-Winfield Inc.,

COMPACT SMT VCXO

With a wide frequency range of 2 to 55 MHz, Champion's K1526A Series features compact ceramic construction in a 4 J-leads, SOJ-20 industry-standard footprint. Additionally, the Series provides ±25ppm stability performance.

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FULL PERFORMANCE SMT VCXO

The 5V and 3.3V Full Performance K1526B Series comes in a 6 J-leads SOJ-20 ceramic package including a standard tri-state selectable pin with optional -40°C to +85°C operating temperature range.

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Champion

LOW COST SMT VCXO

An efficient, low cost option in surface mount VCXOs, the K1526LC Series features an Absolute Pull Range (APR) that meets your PLL tuning needs. Tri-state output selectable with a frequency range from 2 to 55 MHz and 3.3 Volt optional supply.

READER SERVICE 120

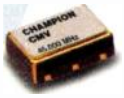
NEW SMT VCXO

The K1526C Series, Champion's newest innovation in 5 Volt Full Performance SMT VCXOs, features a 4 J-leads SOJ-20 industry-standard footprint. It also provides ±25ppm stability, optional 3.3 Volt operation and frequency performance to 55 MHz.

READER SERVICE 121

5x7mm SMT VCXO

Champion's newest SMT configuration is a 5 x 7mm 5V and 3.3V extremely low profile ceramic leadless chip carrier (CLCC). The CMV Series offers an operating temperature range option of -40°C to +85°C as well as a frequency range of 2 to 52 MHz.



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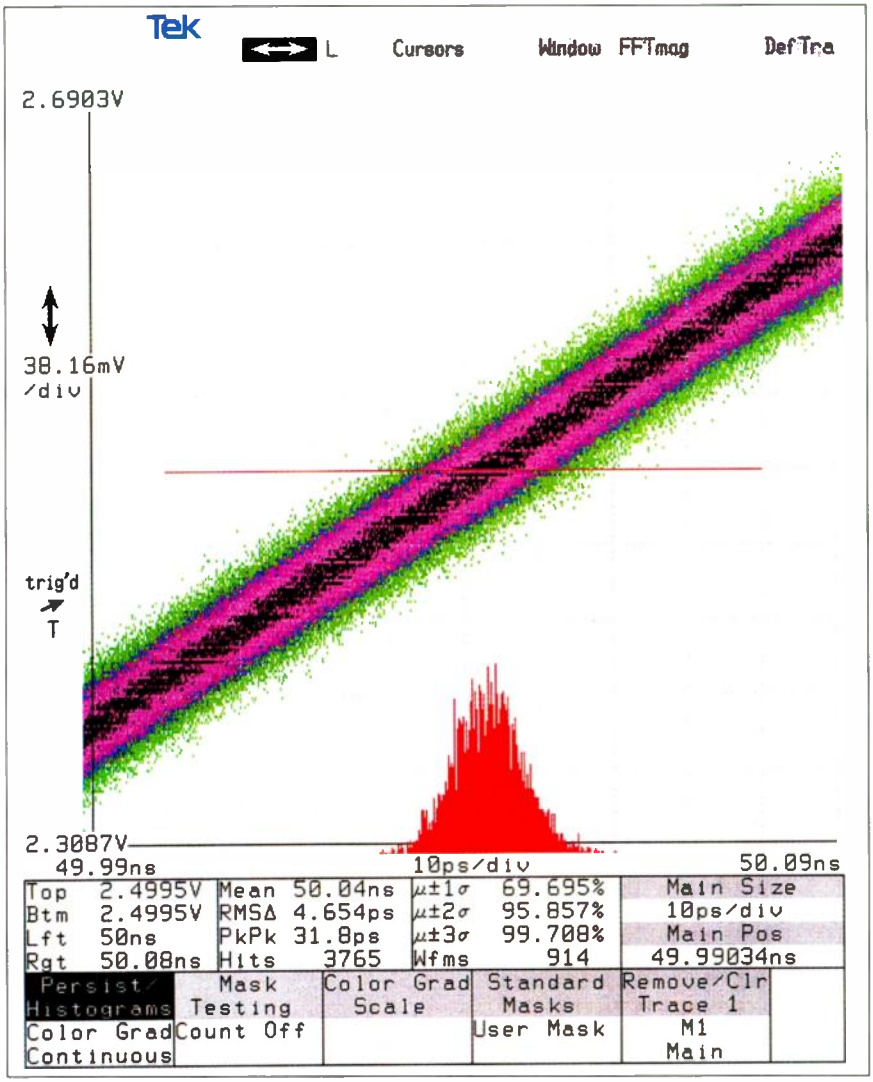

1. This oscillogram shows oscillator jitter in detail for a fundamental crystal. The peak-to-peak value is 31.8 ps, and the RMS value is 4.654 ps. Courtesy: MF Electronics.

Oscillator Suppliers Listed In This Article

Champion Technologies
2553 N. Edgington St.
Franklin Park, IL 60131
(847) 451-1000
www.champtech.com
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www.ofc.com
CIRCLE 480

Raltron Electronics Corp.
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www.raltron.com
CIRCLE 481

Valpey-Fisher Corp.
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Hopkinton, MA 01748
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www.valpeyfisher.com
CIRCLE 482

Vectron International
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and Grenchen, Switzerland-based Micro Crystal Co.

Connor-Winfield claims that its inverted-mesa process for AT-cut quartz crystals enables the manufacturer to obtain higher frequencies at lower cost. In reality, Conner-Winfield has optimized the etching process to realize the crystal's fundamental mode as high as 600 MHz. Presently, inverted-mesa, crystal-controlled oscillators up to 250 MHz are in production, while those in the higher-frequency range are in pilot production, according to the manufacturer. The company has developed the process to etch the quartz crystal at its center. This is done to achieve a higher fundamental mode of operation. In addition, Conner-Winfield offers these VCXOs with an industrial-temperature range of -40° to 85°C.

Champion Technologies, meanwhile, is readying VCXOs in the range of 50 to 200 MHz using its proprietary inverted-mesa technology. The supplier has filed several patents on its process.

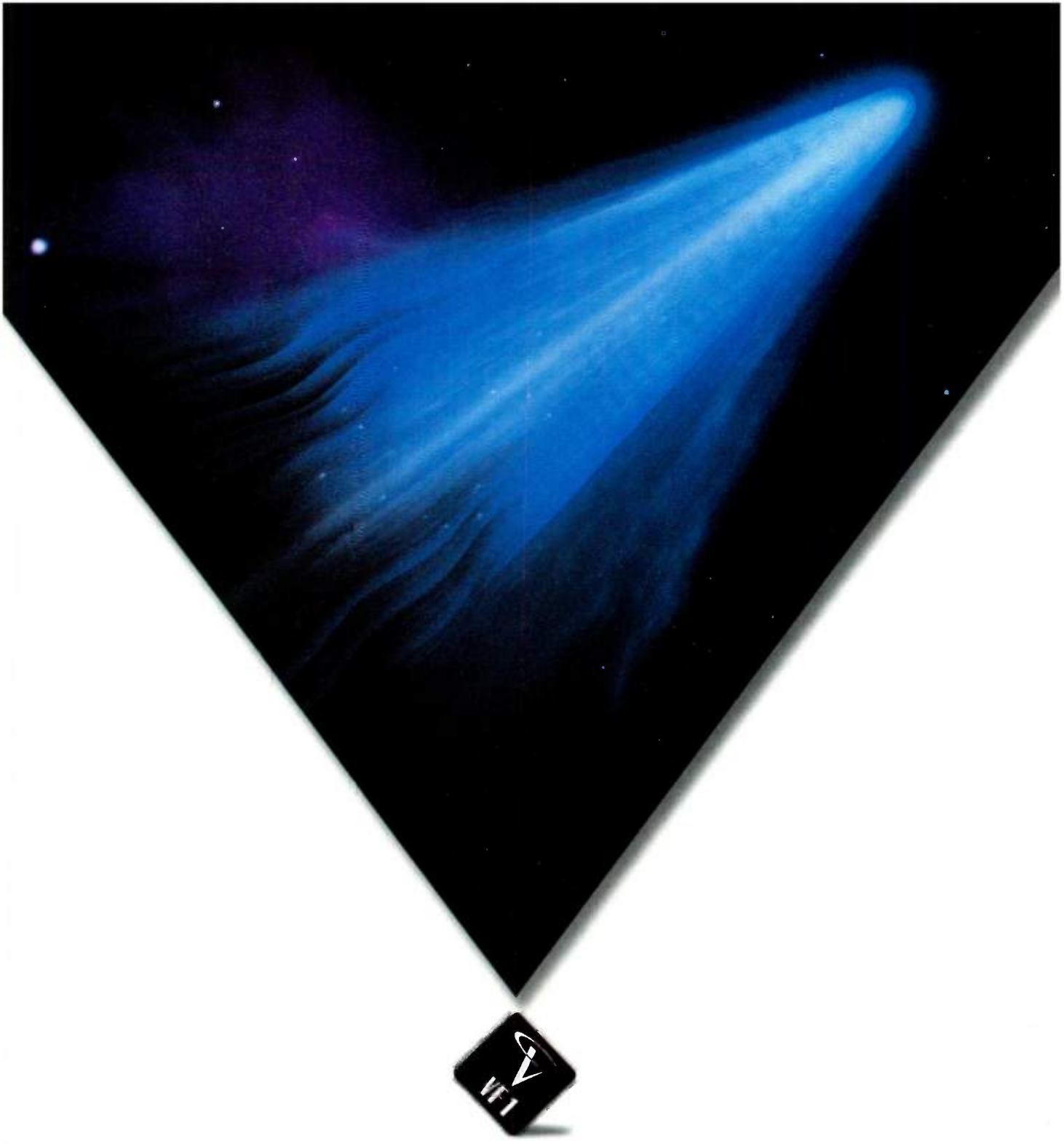
Micro Crystal has developed a cost-efficient production process by merging a photolithographic batch process with wet chemical etching on the wafer. As a result, Micro Crystal can produce "high-frequency, fundamental rectangular, AT-cut quartz resonators with inverted-mesa structures in volume at reduced costs," says Tom Lawrence, general manager for the company's U.S. division.

Engineers at Micro Crystal also have developed rugged, hermetically sealed SMD packages for these resonators. Using these high-frequency crystals, the supplier has produced high-performance oscillators in the range of 30 to 100 MHz, with a large pulling range and low spurious levels. The rugged ceramic packaging has enabled the manufacturer to offer these units in industrial (-40Υ to 85°C) and military (-55Υ to +125°C) temperature ranges.

Signal Integrity

Similarly, many communications and digital applications are using VCXOs to restore signal integrity and waveshape. In fact, these applications implement VCXOs in a PLL configuration to reconstitute clock and data signals. Here, the VCXO's wide-frequency-deviation range (pull range) and tighter center frequency tolerance is paramount.

To address the needs of these appli-



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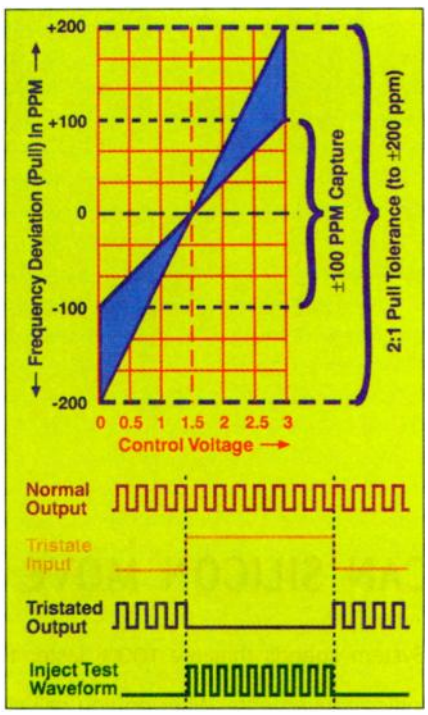
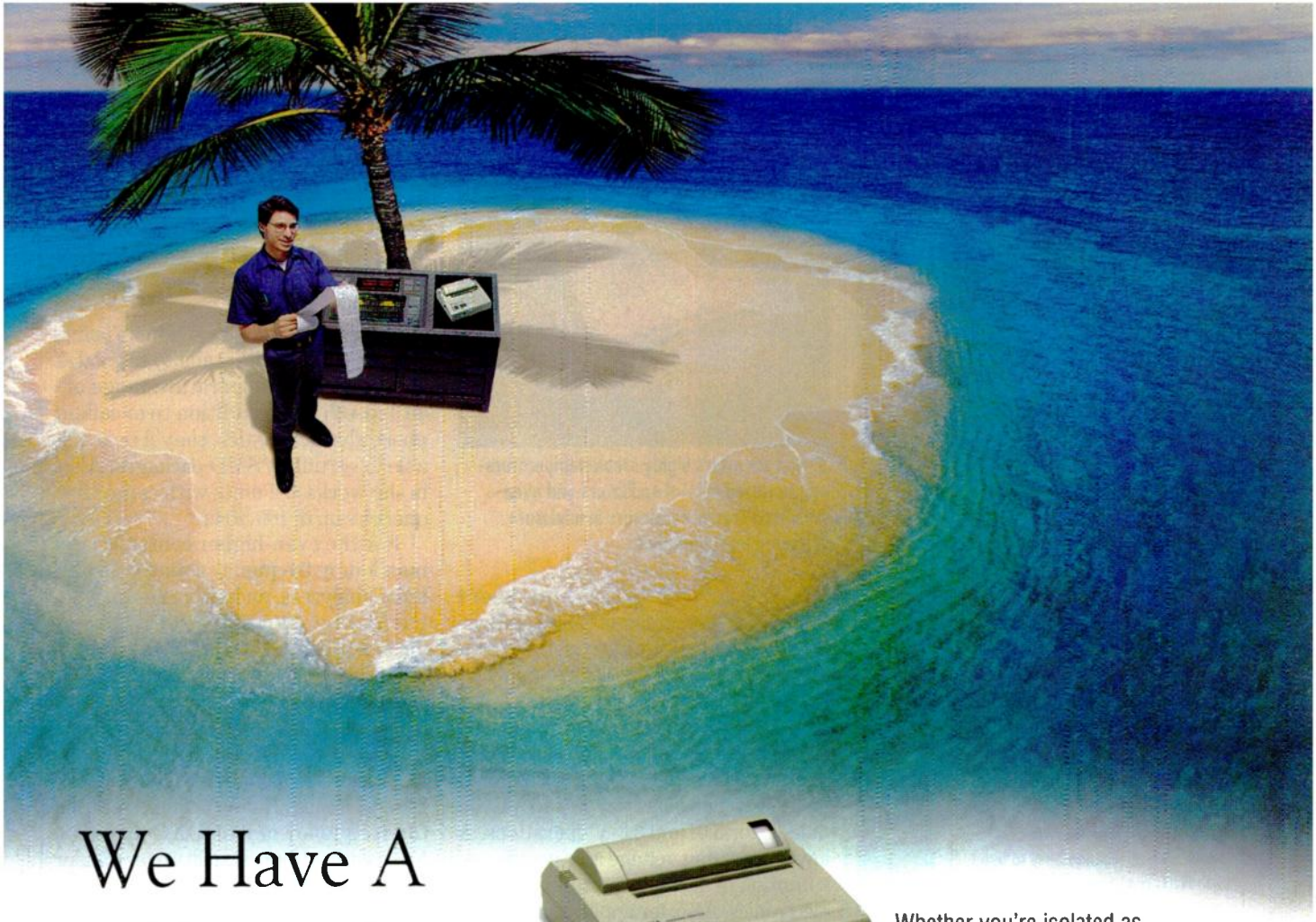
BEYOND PERFORMANCE

cations, MF Electronics has introduced a VCXO, model M2322, with a wide-frequency-capture range of ±100 ppm, and with center-frequency accuracy within ±25 ppm for all variations in dc supply voltage, load, and aging. Frequency deviation (pull) is controlled by a variable dc control voltage in the range of 0 to 3.0 V. "Its wide capture range enables the M2322 to remain synchronized to the input, even though noise and/or jitter cause significant frequency variations," says MF Electronics' president Marty Finkelstein. "In addition, control-voltage bandwidth of 20 kHz allows the VCXO's output frequency to remain locked to the input despite rapid jitter-induced frequency change," notes Finkelstein. "Also, the unit's 3-V operation minimizes power consumption and internal temperature rise to enhance reliability of the VCXO."

Other features of the M2322 VCXO include output waveform jitter of less than 10 ps rms, first-year drift of the oscillator of less than ±3 ppm, and long-term drift of ±1 ppm/year. The center frequency for the M2322 is over the range of 1 to 125 MHz. According to MF Electronics, the frequency capture specifications are guaranteed over 0 to 70°C.



2. Model M3322 from MF Electronics is a 3.3-V voltage-controlled crystal oscillator with tristate capability. This functionality permits automatic test equipment to inject its own special waveform for board/system testing.



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3. Raltron offers highly stable temperature-compensated crystal oscillators and oven-stabilized crystal oscillators in miniature surface-mount packages.

Many automatic test equipment (ATE) devices and circuit-board and system diagnostics require tristate functionality in crystal oscillators. This feature allows an ATE system to halt the VCXO's output, and inject its own special test waveform for board or system diagnostics *(Fig. 2)*. Toward that end, MF Electronics has developed VCXO models for 5.0- and 3.3-V operations. A lower operating voltage cuts power consumption in battery operated portable electronics. Also, for applications where space is at a premium, the units come in miniaturized, SMT packages.

These miniature VCXOs are the forte of suppliers like Vectron International, Raltron Electronics Corp., and Champion Technologies amongst others. Vectron, for instance, has unveiled a series of very tiny, high-frequency VCXOs for use in SONET and other telecommunication systems.

Stable Operation

For mobile telecom and radio applications that require stability beyond that offered by VCXOs, Raltron has introduced TCXOs that guarantee continuity over time and temperature *(Fig. 3)*. Recently, the company launched the RTXO-113 series that boasts a stability of ±2.5 ppm over an operating-temperature range of -30° to +80°C. Frequency variations with aging are less than ±1.0 ppm per year, according to Raltron. The company says that this performance is made possible by a network of passive elements whose collective temperature coefficient tracks and negates the natural, temperature-induced variations in crystal output frequency. The net result is an extremely high stability with temperature fluctuations. Operating at a single 3.0-V supply, the maximum current drain for the RTXO-113 is 1.5 mA. The device comes in a compact, surface-mount package that measures only 7 by 9 by 2 mm. The unit is available in standard communications frequencies from 12.6 to 20.0 MHz.

Raltron's technology roadmap points toward TCXOs with stability as good as ±1 ppm over a temperature range of -40Υ to +85°C. In addition to excellent phase characteristics, they'll be available in shrunken SMD packages. Also, in the works are units with center frequencies up to 100 MHz.

For the even-higher constancy demanded by frequency counters, spectrum analyzers, and airborne-/marine-navigation systems, Raltron has announced an OCXO with 0.1-ppm stability from 0 to 60°C. Long-term stability is better than ±0.3 ppm/year. The center frequency for the new OX-5000 series is from 10 to 60 MHz. It's offered in a surface-mount housing with IR solder-reflow capability. Raltron plans to extend the frequency of its OCXO up to 200 MHz, with 0.1-ppm stability over a wider temperature range of -40Υ to 85°C.

Interestingly, British C-Mac Quartz Crystal Co., has taken OCXOs a step further. C-Mac is talking of OCXO stability in the parts-per-billion (ppb) range. Employing SC-cut crystals, proprietary oven controllers, and optimized ASIC chips, C-Mac has developed a family of OCXOs that boast frequency stability of ±0.01 ppb over a temperature range of -20Υ to 60°C.

"These oscillators meet Bellcore's Stratum II Synchronization specification," claims Bob Pearson, C-Mac's N. American marketing arm manager. CPO-1 center frequency is between 5 and 10 MHz. For less-demanding applications, C-Mac has the CPO-10 line with stability of ±2 ppb. The CPO-10 complies with Bellcore's Stratum IIIE Synchronization specification. "Depending on the level of synchronization stability needed, CPO-1 and CPO-10 OCXOs are designed for use in SDH/Sonet, as well as base stations for GPS and other satellite navigation systems," notes Pearson.

The assortment of flavors that crystal-controlled oscillators come in will continue to increase. And, depending on the performance and stability needs of the applications, designers can opt for any number of variations on the VCXO, TCXO, or OCXO themes.

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NOW THERE'S A NONVOLATILE MEMORY DEVICE THAT'S AS ADVANCED AS YOUR LATEST DESIGNS. Whether you're designing a next generation CDMA or GSM phone that incorporates voice memoing...or a new Windows® CE palmtop...or an alphanumeric pager, conventional solutions just aren't adequate. You need a device that handles large or small amounts of frequently changing data easily and efficiently–that's Atmel's new DataFlash™! DataFlash gives you the advantage of an extremely small-sectored Flash memory array (264 or 528 bytes per sector), plus on-chip SRAM buffers that allow true EEPROM emulation. There's even built-in error detection circuitry and a hardware-controlled write-protection option. You also get single-voltage read/write operation, single-cycle programming that doesn't require a separate erase command, and a simple, high-speed interface designed to move data in and out quickly, even if it's only a byte at a time. And since it's nonvolatile, you eliminate the cost of backup batteries, charging circuitry or special voltage regulators. Atmel's DataFlash. Now your designs can have an advantage!

Device	Density	V_{CC}	Interface*	Sector Size
AT45D011	1M bit	5.0V	Serial	264 bytes
AT45D021	2M bit	5.0V	Serial	264 bytes
AT45D041	4M bit	5.0V	Serial	264 bytes
AT45D080	8M bit	5.0V	Parallel	264 bytes
AT45D081	8M bit	5.0V	Serial	264 bytes
AT45D161	16M bit	5.0V	Serial	528 bytes
AT45DB011	1M bit	2.7V	Serial	264 bytes
AT45DB021	2M bit	2.7V	Serial	264 bytes
AT45DB041	4M bit	2.7V	Serial	264 bytes
AT45DB080	8M bit	2.7V	Parallel	264 bytes
AT45DB081	8M bit	2.7V	Serial	264 bytes
AT45DB161	16M bit	2.7V	Serial	528 bytes

*All devices are sequential access

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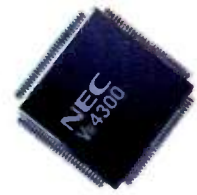
"WITH NEC PROCESSORS, WE CAN PUSH THE CLOCK WITHOUT HAVING TO PUSH OUR SANITY."

Designed for Microsoft® Windows®CE



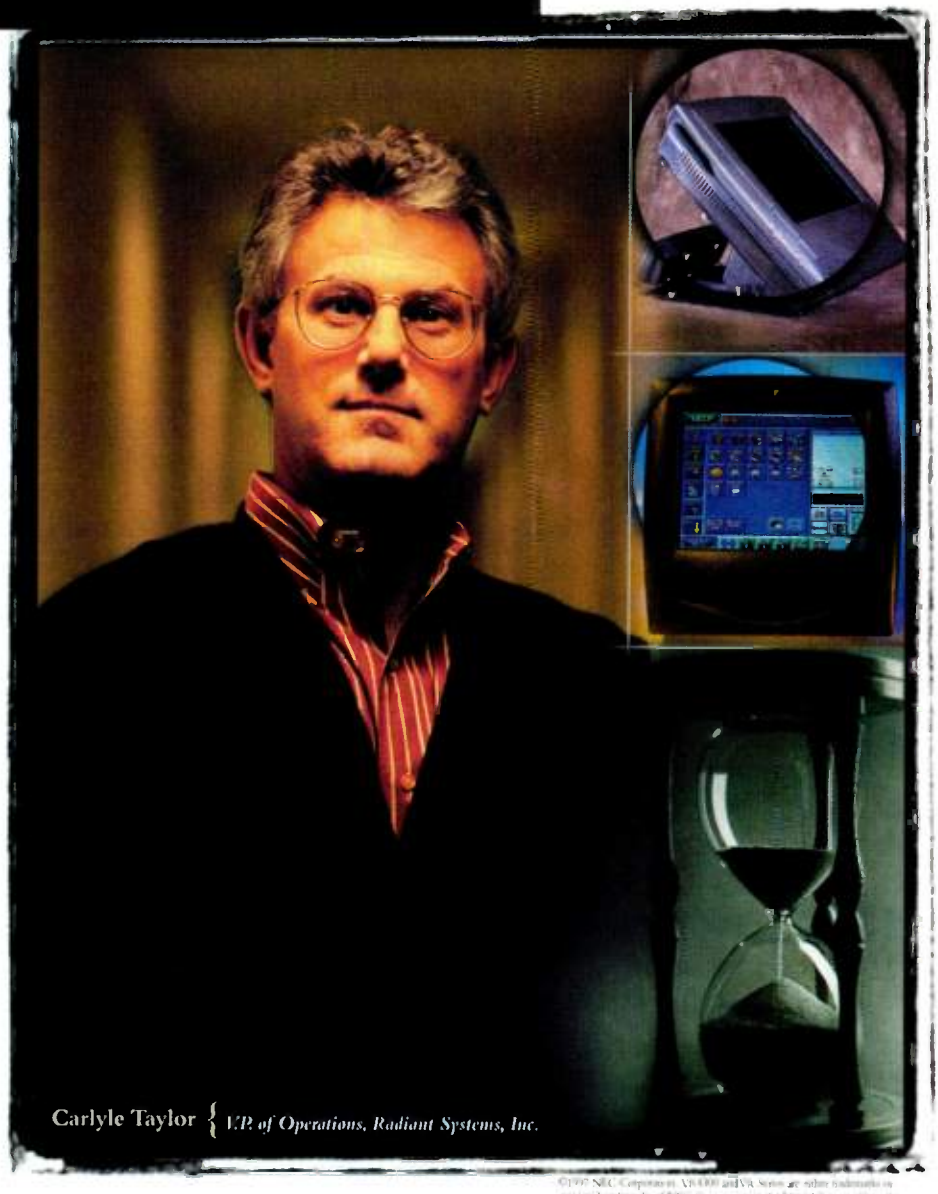
"With NEC's VR4300 processor, our latest Windows CE terminal went from concept to market in just three months."

"We have a pretty single-minded pursuit here at Radiant Systems: produce changes for the better by developing the most advanced products across a wide range of industries. And we have to do it in shorter periods of time. In fact, these days we go from concept to market in just three months.

"Well, just when you think you can't design any faster, you get hold of a product like NEC's VR4300™ MIPS® RISC processor and companion chip. They're the perfect price/performance solution for our MediaClient™– a revolutionary Windows® CE multimedia retail terminal. And because of NEC's innovative I/D cache, the VR4300 is ideally suited for our demanding throughput needs. And it's a proven product, fully integrated, with plenty of room for future scalability.

"You get something else, too. You get an exceptional level of confidence working with a company like NEC. There's the technical support, the design support and, of course, the manufacturing clout.

"Any engineer will tell you these are incredible times. Fortunately, Radiant Systems isn't stuck somewhere in the middle of all these changes– we're actually making them happen.



Carlyle Taylor { *VP of Operations, Radiant Systems, Inc.*

"And NEC? Well, without a doubt, their purpose is to help you speed the design process by providing a total solution that gets you to market fast, maybe even ahead of schedule."

For more information about NEC's VR Series, call 1-800-366-9782. Ask for Info pack #197.

VR SERIES PROCESSORS | WINDOWS CE

NEC

PROUD SPONSOR OF: NEC WORLD SERIES OF GOLF, AUGUST 27-30

READER SERVICE 136

ELECTRONIC DESIGN QUICK LOOK

Edited by Debra Schiff and Nancy Konish

MARKET FACTS

Germany Bullish On Semiconductor Growth

You'd think with all the noise the market made at this past winter's Asian financial crisis, we wouldn't be seeing such positive projections about the future of semiconductors. Yet, the numbers coming from the electronica 98 Press Office in Munich, Germany say otherwise. They say that despite a dip in sales in 1997, we can watch a rise of 14.7% in 1998, to continue on through 1999. At the moment, $140 billion worth of semiconductors are sold in the worldwide market, representing a large chunk of the $920 billion of electronics products sold worldwide. These statistics are based on the Deutchmark, so the sales in 1997 totaled 12.18 billion marks. If the translation is into U.S. dollars, the German market experienced a 10% loss. This year, the Germans expect to see an increase to 13.97 billion marks. In that market, by November 1996, there was an overall 16% increase in quantities sold, which was eventually balanced in February 1997, with a 12% price drop. The general state of the economy is so pleasant that we may witness an increase in volume to over $160 billion this year. Responsible for this rise are special-purpose ICs (38% of the overall volume), which are expected to rise 14%. Other contributors are standard components and commodities (increasing 13%), microprocessors (up 12%), and memories (rising 5%). Of course, according to electronica 98, the future of electronics is the consumer applications. Growth in that sector will be driven by automotive applications, digital television, home PCs, household appliances, mobile telephones, and smart cards. On the flip side, elements that are pushing growth in a negative direction include "unused capacities in semiconductor manufacturing." Specifically, we're looking at semiconductor memories and DRAMs. DRAMs have become such a "staple commodity" that their prices have been dropping faster than those sub-$1000 PCs. That results have become evident on the profit and loss statements of the chip manufacturers. Another source of sinking profits comes from the increasing ramp of obsolescence. Here, the battle is fought in the factory, as Moore's law has dictated. Fabs become obsolete in about 18 months, in some cases, as the time it takes performance to double clocks in at about 18 months. DRAMs hit a wall in 1996, dropping in sales by 80%. With a market volume of $41 billion in 1995, they bottomed out at $20 billion a year later. Meanwhile, DSPs, microcontrollers, and microperiphery components skyrocketed, as the PCs into which they were slated to go, had a compound annual growth rate of 17%. Projections from electronica 98 say that PC sales will nearly double from 71 billion to 132 billion units between 1996 and 2000. At the same time, the DSP market will jump from $1 billion to $5 billion. The big, electronics trade show, to be held at the new Munich Trade Fair Centre, Nov. 10-13, will be showcasing over 450 main exhibitors from the semiconductor industry, with the majority from Germany, the U.S., Great Britain, France, and Japan. Three of the halls (A4, A5, and A6) will be dedicated to semiconductor suppliers. Over 100 companies from Asia have registered through their European subsidiaries. As far as the Asian market crisis goes, the short-term effect just appears to mean that those analysts who predicted that we'd see $300 billion in volume by 2000, will have to accept that the volume will be closer to about $250 billion or less. As always, we'll keep an eye on it.

Sales of semiconductors in 1996 were down 9%, and only up 4% in 1997. Projections from electronica 98 show a startlingly large increase of 14.7% in 1998. The trend is expected to continue into next year.

For more information, contact Messe München GmbH, Messegelände, D-81823 München, Germany; +(0 89) 9 49-01; fax +(0 89) 9 49-09; www.electronica.de; e-mail: info@messe-muenchen.de—**DS**

40 YEARS AGO IN ELECTRONIC DESIGN

Ad: Fairchild Silicon Transistors

Fairchild Silicon Transistors offer an exceptional three-way combination:

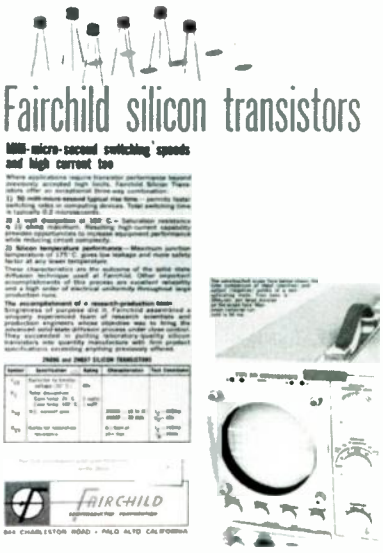
1) 50 milli-micro-second typical rise time

2) 1 watt dissipation at 100° C.

3) Silicon temperature performance.

These characteristics are the outcome of the solid-state diffusion technique used at Fairchild. Other important accomplishments of this process are excellent reliability and a high order of electrical uniformity throughout large production runs.

Fairchild assembled a uniquely experienced team of research scientists and production engineers, whose objective was to bring the advanced solid-state diffusion process under close control. They succeeded in putting laboratory-quality silicon transistors into quantity manufacture with firm product specifications exceeding anything previously offered. *(ELECTRONIC DESIGN, August 20, 1958, p. 8)*



The above text reproduces portions of this ad's fine print, which might be difficult to read. The scope in the ad shows input and output pulses with a time base of 20 ns per division. This is the first advertisement from Fairchild Semiconductor that I've come across in back issues of ELECTRONIC DESIGN. Fairchild Semi was formed in 1957 by such industry luminaries as Robert Noyce and Gordon Moore, who later founded Intel, along with Andy Grove. With its batch-oriented diffusion and planar processes in hand, Fairchild would go on to produce integrated circuits in the following year.—Steve Scrupski

How Long The "Moon"

The entire Soviet Satellite, Sputnik II, containing the dog "Laika," instrumentation, propellant tank, and motor, was from 74 to 84 ft long. This measurement was calculated from photographic evidence taken with the missile tracking camera, designed and built by the Perkin-Elmer Corp., Norwalk, Conn., for the Air Force Missile Test Center. Trained on Sputnik II as it passed over Patrick Air Force Base, Fla., on December 21, 1957, the Recording Optical Tracking Instrument took the sequence of photographs necessary to determine the length.

Russian Satellite Beta (Sputnik II) passed within 200 statue miles of the Missile Test Center. Approximately 400 ft of 70 mm film was used by the tracking telescope. The telescope has a 24 in. aperture and focal length up to 500 in. Maximum focal length was used for this series. Enlargements were made of the photographs, magnified 27.7 times from the original film. This magnification was determined from similarly enlarged photographs of the sprocket holes of the film and their known dimensions and spacing. Image size was measured on the enlargements. These values, divided by the magnification of 27.7, gave the size of the image on the original film. *(ELECTRONIC DESIGN, August 20, 1958, p. 9)*

Sputnik II was launched just a couple of months after the Soviet Union's first satellite. It's ironic that here, we had a case of ground-based equipment performing surveillance of satellites. Today, it's the satellites that perform surveillance of the ground-based operations.—Steve Scrupski

Steve Scrupski is a former Editor-in-Chief of ELECTRONIC DESIGN. Now semi-retired, he can be reached at scrupski@worldnet.att.net.

Play Today

Are computers taking over the television industry, or is it the other way around? Play Inc., Rancho Cordova, Calif., recently introduced two products that may make finding the answer to that question pretty tricky. SpaceCam and Gizmos 98 were introduced and displayed with Play's earlier innovations, Snappy Video Snapshot and Trinity.

The SpaceCam VideoPhone, priced at $139, is capable of transmitting live, high-speed video over the Internet, intranet, or any direct modem connection. The SpaceCam's claim to fame is that it produces a higher level of picture quality than was previously available with the desktop PC video cameras. This is mostly due to Play's experience in broadcast video and advanced image-processing algorithms.

Gizmos 98, priced at $49, is a software package with new tools for business, personal productivity, and entertainment applications. It includes Performer98, a television-style presentation tool that uses 60-frame-per-second special effects and transitions. It was designed for Windows 98 and Windows 95.

Play has received recognition for its Trinity desktop video production system, and their first product, the Snappy Video Snapshot. Trinity can replace every tool found in a high-end television studio, while Snappy can capture high-resolution images from any video source.

Play recently joined forces with Electric Image, Pasadena, Calif., a high-end 3D animator. Electric Image is widely recognized in the broadcast and motion picture industries for its work in 3D animation. Its credits include "Star Trek: First Contact," "Star Wars Special Edition," "The Mask," and "Terminator 2: Judgement Day." Through the merger, officials at Play hope to integrate powerful 3D animation and video technology. They plan to create graphics and video products unlike any that have ever been seen.

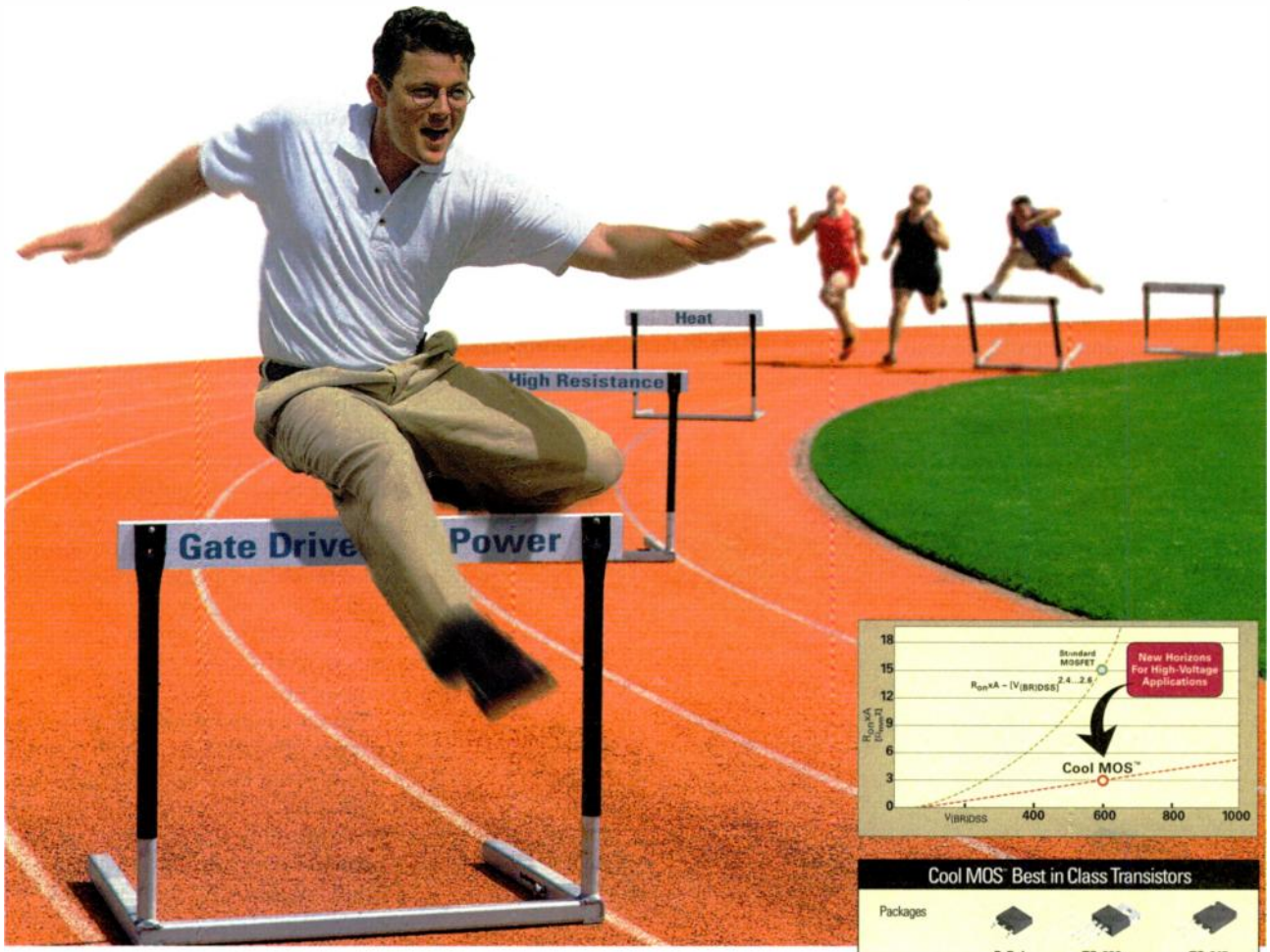
For more information, call (916) 851-0800 or visit the web site at www.play.com.

Lisa Calabrese

SIEMENS

Introducing high voltage MOS Transistors

Cool MOS™ puts you out in front with up to 5x better performance.



Get the competitive advantage with Cool MOS high-voltage transistors.

Siemens is the first off the starting block in the race to find smaller, more efficient power conversion solutions. And we've broken through the silicon barrier for dramatic improvements in MOS technology — with Cool MOS. It easily clears the hurdles of gate drive power, high resistance and heat dissipation. In fact, it actually reduces the area-specific $R_{DS(on)}$ at 600V — 5x better than any other previously existing technologies. And with comparable current ratings, Cool MOS delivers 2/3 the power loss and 1/2 the gate charge in a smaller conventional MOSFET package. The result is higher efficiency — and lower cost. That gives you a head start in developing applications previously thought to be impossible. So let Siemens help you really get the jump on tomorrow's winning high voltage designs.

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READER SERVICE 148

MANAGING THE DESIGN FACTORY

For Communication, Less Is More

It's the rare development team that doesn't complain about communication. People assume that the solution is increasing the quantity of communication. More e-mail is sent to more people. Memos are distributed to everyone. In-baskets overflow. Does this improve communications? No.

Team members continue to make bad decisions because they don't have information known to someone else on the team. Naively, we assume that we need more communication. The obvious solution is to increase information flow. All information known to anyone else on the team will be communicated to all other team members.

Although this causes file cabinets to bulge, it won't improve communication. Why? Because quantity of information is rarely the problem. What most people don't realize is that the first attack on any communication problem should be to eliminate the need for communication, not increase the volume of information transferred.

DON REINERTSEN

For instance, an increased need for communication is often a symptom of poor organization. It's usually a sign that either the decision making has been assigned to the wrong person, or the data needed for the decision is not available for the decision maker.

What happens if component certification information is hidden in an obscure proprietary database in the reliability engineer's office? Design engineers must communicate with the reliability engineer to get the information required to reuse a component. If the information had been available online, the need for communication would be eliminated.

Whenever people lack the information they need to do their job they must obtain it from other people by communicating with them. When the information required to make a decision is not available to a decision-maker the need for communications arises.

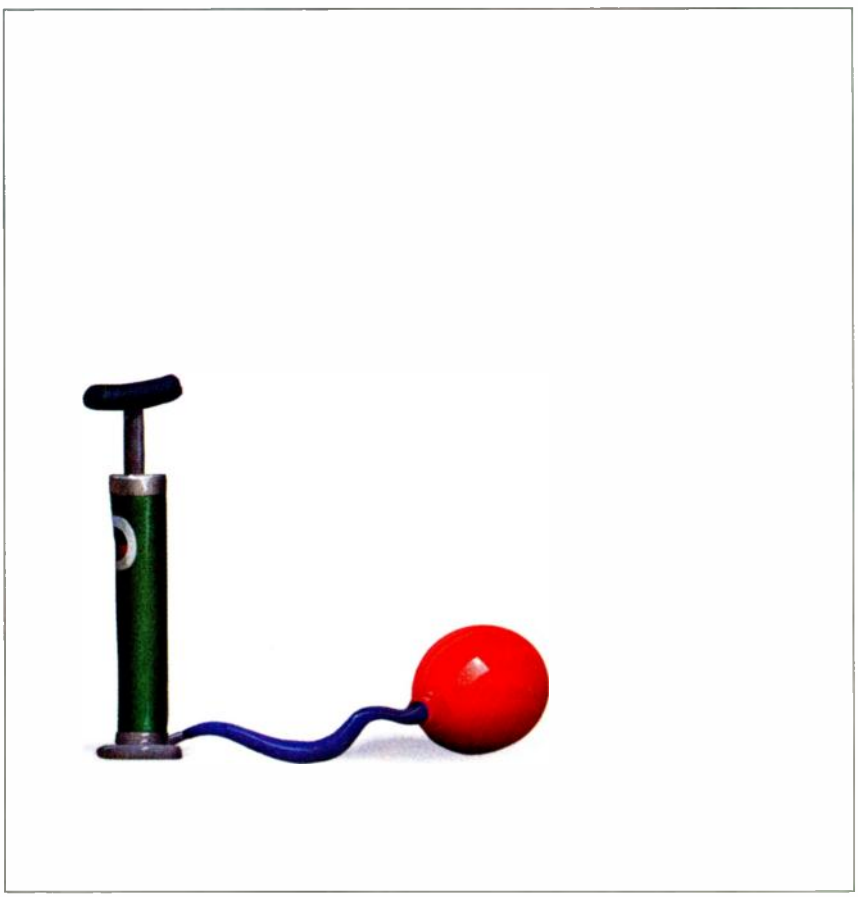
Interestingly, this is a case where "life imitates hardware." Whether one designs circuit boards or integrated circuits, too many interconnects is usually a sign of poor partitioning of the design. Repartitioning the design can have a huge impact on the number of interconnects. The same is true of organizational design.

Even when the work is well-partitioned we still need to make sure that people know how roles have been assigned, and where to get that information. For example, one company did not believe in publishing its organizational charts, in case they might fall into the hands of headhunters. The technique proved very effective, and headhunters were unable to figure out how the company was organized. Unfortunately, neither could employees.

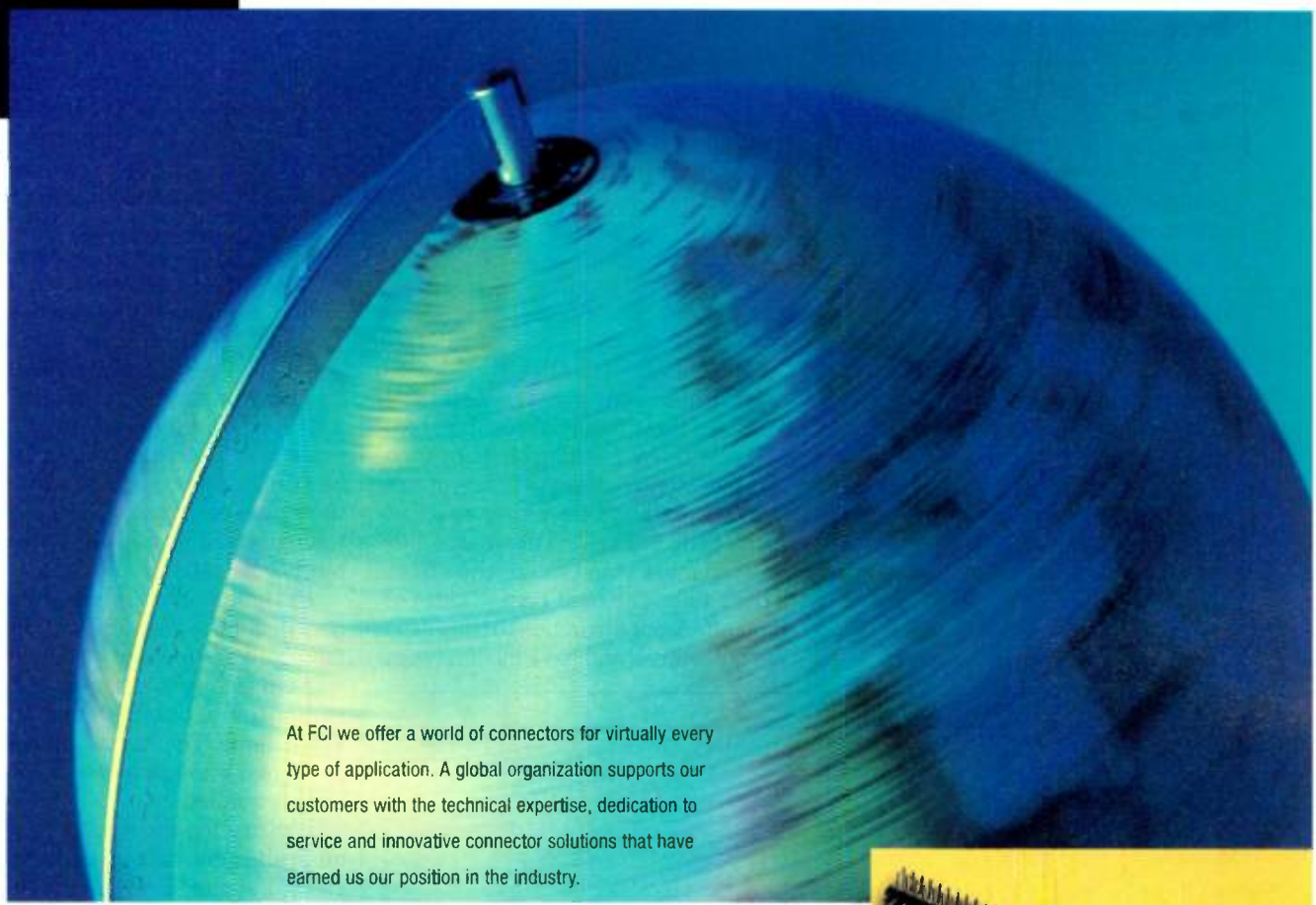
Because no one knew who was in charge of what, they would distribute e-mail to anybody who might have a remote chance of being responsible for a problem. This overdistribution backfired. As everyone saw 20 other action addresses on the message, they assumed that they had 5% chance of being responsible. As a result, nobody took action.

Remember, when you hear people saying that we need more communication, pause briefly and ask if this is the real problem. Look carefully at improving organization design and information systems. Quantity rarely is the answer to communications problems.

Don Reinertsen is president of Reinertsen & Associates, a consulting firm specializing in product development management. He can be reached at (310) 373-5332 or e-mail: DonReinertsen@compuserve.com.



The world is turning to FCI connectors.



At FCI we offer a world of connectors for virtually every type of application. A global organization supports our customers with the technical expertise, dedication to service and innovative connector solutions that have earned us our position in the industry.

Today, FCI is the world's third largest connector company.

FCI has specialized in micro-miniature and smart card products for more than 20 years. Our depth of product is available for the evolving digital phone market, set-top box, HD TV and GPS markets, as well as other standard industrial applications.

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See FCI's entire product portfolio at http://www.fciconnect.com

READER SERVICE 126

TRUDEL TO FORM

Let's revisit our last topic. The best companies (top 22%) do much better at product targeting than the rest. They also get a much higher percentage of sales from new products. What does that suggest for future action at your firm, or in your group?

First, let's discuss improving competitiveness. If your firm's new product success rate is low, say 50% or less, you may have a major competitive problem. If a low percentage, say 25% or less, of your sales come from new products, you almost certainly have a problem. The data (source: PDMA and Trudel Group surveys) shows that if your performance is this low, you can make major improvements.

Honesty is crucial when discussing such issues. I know of one electronics supplier with over $1 billion in sales, that shot itself in both feet. A top executive decreed that general management bonuses would henceforth be tied to the percentage of sales from "new" products. That sounded sensible, but the issue should have been behavior, not metrics. All of the firm's divisions quickly created trivial new products. Their engineers were put on projects that added little customer value. The company wasted scarce resources and did not improve its business position.

JOHN D. TRUDEL

The data reveals that most firms, in any given industry, can improve their financial results (sales and profits) by working on innovation, and moving to newer portfolios of substantive products. I encourage such efforts. Still, behavioral change is difficult, so most won't make the effort. That's fine. The next part of this column offers opportunities to those who are innovative, and have modern, compelling product lines.

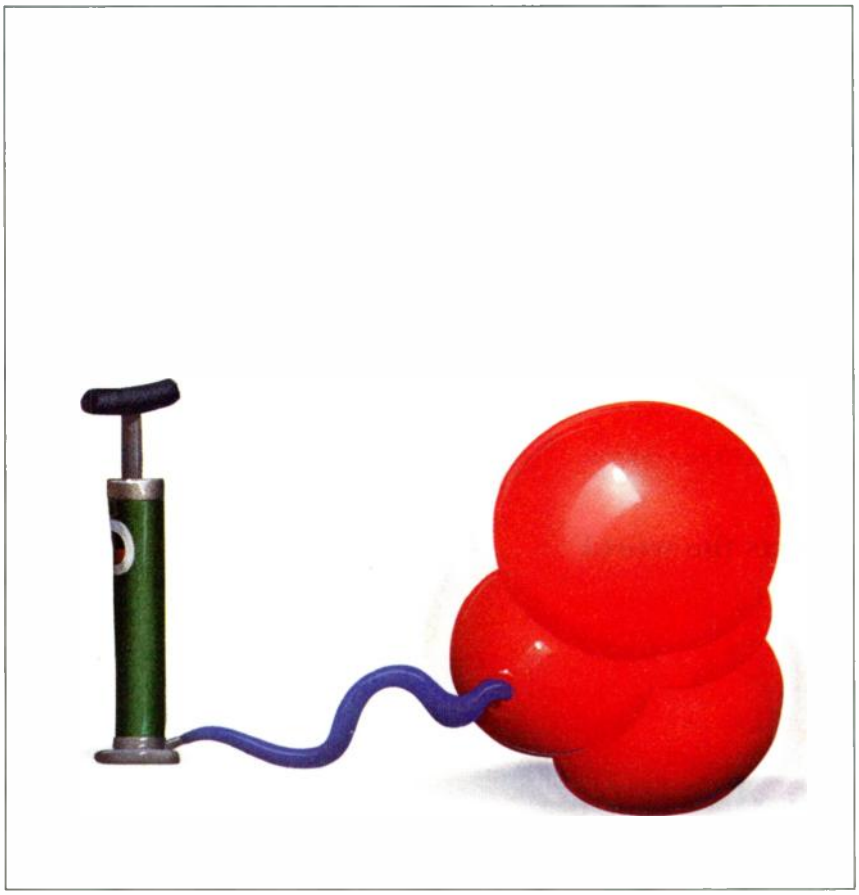
Remember the late '70s and early '80s, when the Japanese won market after market, simply by providing higher quality products? That strategy spawned a major quality frenzy. Firms with inferior quality lost market share and value to those with better quality. Firms that made similar products with significantly better quality could undercut the losers' prices with good margins, while stealing their customers. Detroit, Mich., and the U.S. consumer electronics firms learned all the verses of that song. The only firms that survived were those with consistently good quality.

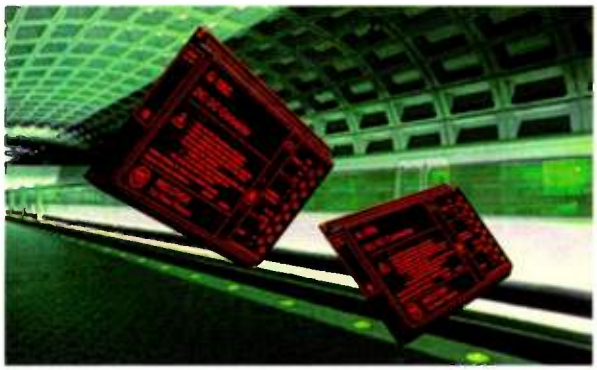
In the '90s, a similar thing happened, but the strategy was different: faster cycles for new products. Few wanted to buy last season's modem, computer, cellular phone, VCR, or video game. The firms that could not cycle fast enough were the ones becoming obsolete.

It's time for a new game, one based on brains, not just process. Why not create a strategic advantage from new product development proficiency? This game is trickier, but the business rewards are greater. It is very hard for downsized firms, which have lost their innovative capability, to recover. Even if it *is* possible, rebuilding will take years.

Why not target the firms that can't innovate well? Look for markets in which commodity products are based on old technology, where the basis of competition is "cheaper, faster." A decade of downsizing has left a target-rich environment. Make sure your innovations are original and inimitable. Then go make a lot of money.

John D. Trudel, CMC, provides business innovation consulting to selected clients. Lectures, keynotes, and workshops are available. He is the author of "High Tech with Low Risk" and "Engines of Prosperity." The Trudel Group, 33470 Chinook Pl., Scappoose, OR 97056; (503) 638-8644; fax (503) 543-6361; e-mail: jtrudel@gstis.net; www.trudelgroup.com.





Melcher's 100 W DC-DC sets new standard for railway industry.

Melcher is already the world leader in the provision of power supplies for use in trackside and railborne applications, we have established de facto standards in the industry with the M, K and S families of DC-DC converters. Now we are establishing a new lead with the Q- family of DC-DC Converters which are compliant with the latest harmonized European railway standard EN 50155 as well as the EMC directive. Featuring five different input voltage ranges from 14.4 to 168 V DC the units are suited to 24, 36, 48, 72 and 110 V DC traction batteries, and offer 100 W from a 3U x 4 TE x 160mm extruded aluminum case, free air rated to 71°C without derating. When operated to 50°C the output power increases to a maximum 144 W.

The ultra-slim profile of 20 mm is achieved by the use of a planar transformer, together with hybrid control circuits and a conversion efficiency of up to 90% to minimise losses and heatsinking. Single and dual output modules are available providing 5 to 48 V, or ±5 to ±24 V DC rails with external adjustment possibility in the range from 50 to 110% of $U_{o\,nom}$. Safety isolation levels are according to EN 60950 with approvals from UL and LGA. RFI performance is below EN 55011/22 level B, and transient susceptibility is according to specifications IEC/EN 61000-4-2, -3, -4 and -5.

4 W DC-DC Uses Planar Technology.

Melcher has released a new family of 4 watt DC-DC converters which set new standards for performance within a 24 pin DIL package. Designated IMX 4 series, the products feature a unique single substrate planar magnetic construction, with all components in SMD format mounted directly to a single multi-layer PCB which also forms the main isolating transformer.

This construction together with a high conversion efficiency of typically 82% has enabled Melcher to increase output power from the industry standard 3 W to 4 W, which reduces the profile to just 8.5 mm. At the same time, Melcher has increased the input voltage range to a very wide 4 :1 ratio, with a choice of either 8.4...36 V DC, 16.8...75 V DC or 40...121 V DC to suit 12, 24, 36, 48 and 72 V DC nominal systems. Available with single and dual outputs from 3.3 V DC to 24 V DC, the units are no load and short-circuit proof, and are fully rated over the ambient temperature range -25...71°C. An extended temperature range version of –40... 85°C is also available as an option. Isolation voltage is a standard 1500 V DC. The units offer excellent electrical immunity, complying with IEC/EN 61000-4-2, -3, -4, -5, and -6, and are UL, cUL, and LGA approved to IEC/EN 60950.

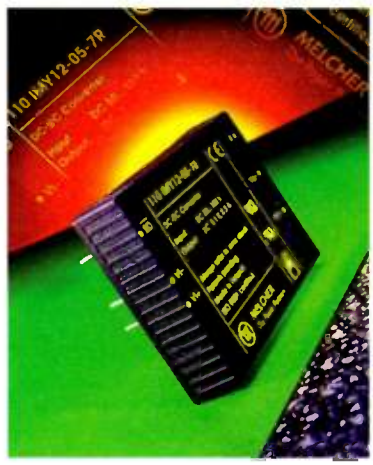
New Databook introduces 35 new products.

Melcher has introduced a new 1100 page databook which details many new lines of innovative AC-DC and DC-DC converters. The databook is also an invaluable reference on standards in the power supply industry.

Melcher manufactures more than 70 families of products, and are one of Europe's leading manufacturers for telecoms, industrial, transportation and military applications.

The databook is available in CD-ROM format. Data can also be downloaded from Melcher's website: www.melcher-power.com

NEW 12/15 W DC-DCs In 2" x 1.5" Package



Melcher has introduced two new ranges of 12 W and 15 W DC-DC converters featuring the latest single substrate planar construction. It offers unparalleled levels of performance in a compact case measuring 51 mm x 40.6 mm with a profile of just 10.5 mm. The IMX- and IMY-families are suited to "Rugged" grade applications and offers up to 17 W of output power from ultra-wide input ranges of 8.4...36 V DC, 16.8...75 V DC and 50...150 V DC. The IMS 15-family provides 17 W output power from input ranges of 14...36 V DC and 36...75 V DC and is suited to "Industrial" grade applications. Both families offer single and dual outputs from 3.3 V DC to 24 V DC and are fully rated over the temperature range -25...71°C. The IMX and IMY units are also available with an extended temperature range of -40...85°C.

MULTIMEDIA CORNER

Have you ever wanted to test out a piece of software before you bought it? Or maybe you've just wanted to get a certain part of a software package? Sometimes you have no choice but to purchase the entire software package. @Home Network, of Redwood City, Calif., and Arepa Inc., from Cambridge, Mass., have joined together to bring another option, "click-'n'-play," to the masses.

Click-'n'-play provides instant access to consumer software, including multimedia CD-ROM content. @Home Network provides high-speed Internet services, and Arepa designs the new broadband Internet software content platform. The partnership originated when Arepa began developing the first open platform for multimedia application delivery.

If all goes as planned with the technological and market trials, @Home users will be able to access many already-existing educational and entertainment multimedia applications thanks to the high-bandwidth platform. Subscribers to @Home can view quite complex and involved CD-ROMs without having to own the CD or the player. Here are a few examples of how click-'n'-play is expected to be used:

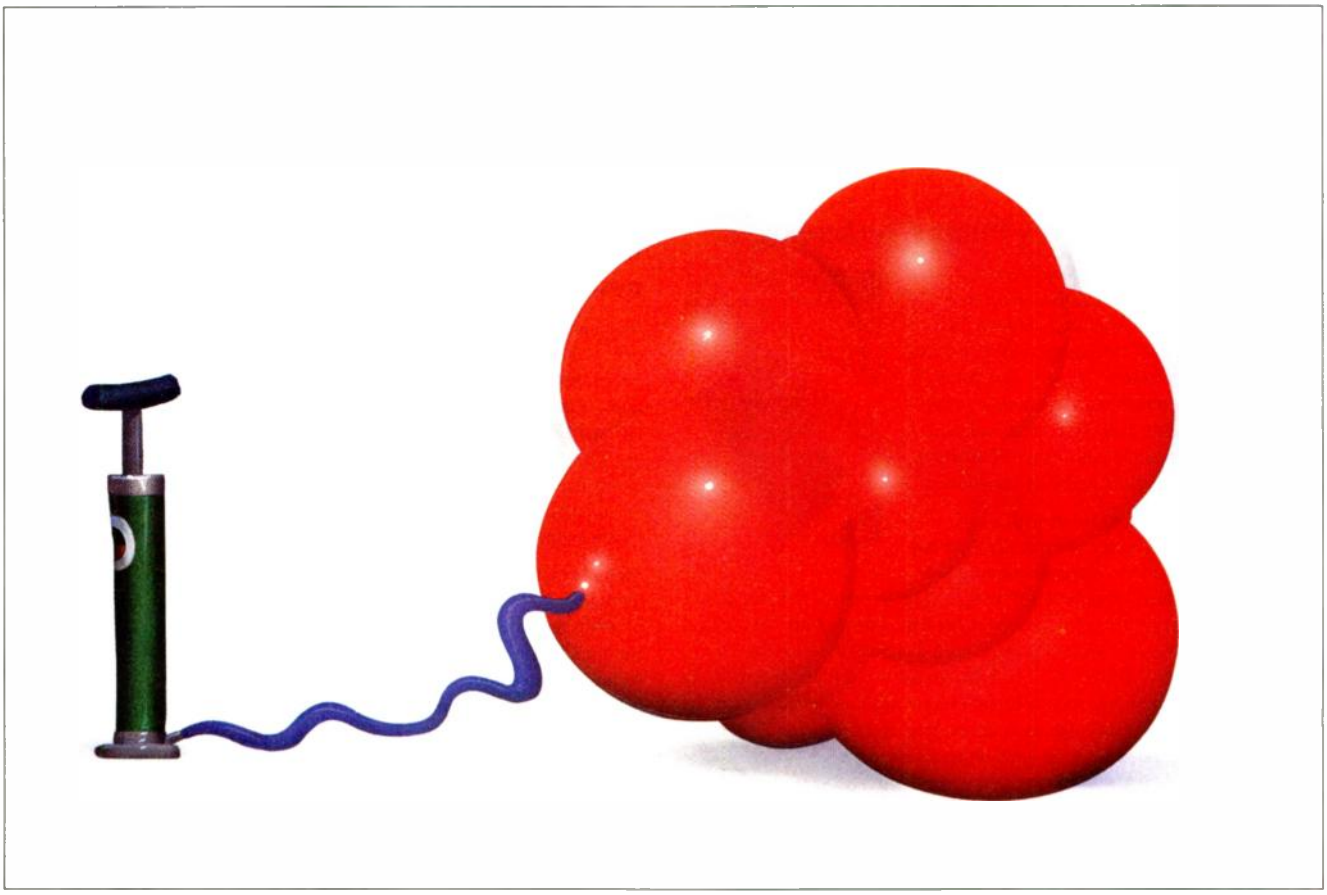
- Multimedia math and reading instruction for grades K-12
- Media-intensive foreign language instruction
- Entertainment (flight simulators or 3D action games)
- Utility programs which "tune-up" your computer
- Home productivity applications
- Interactive references, such as multimedia encyclopedias

A rather convenient feature is the fact that the publisher does not need to provide a special version of the software. A few models being discussed for premium service include pay-per-play, subscription, and advertising-supported transactions.

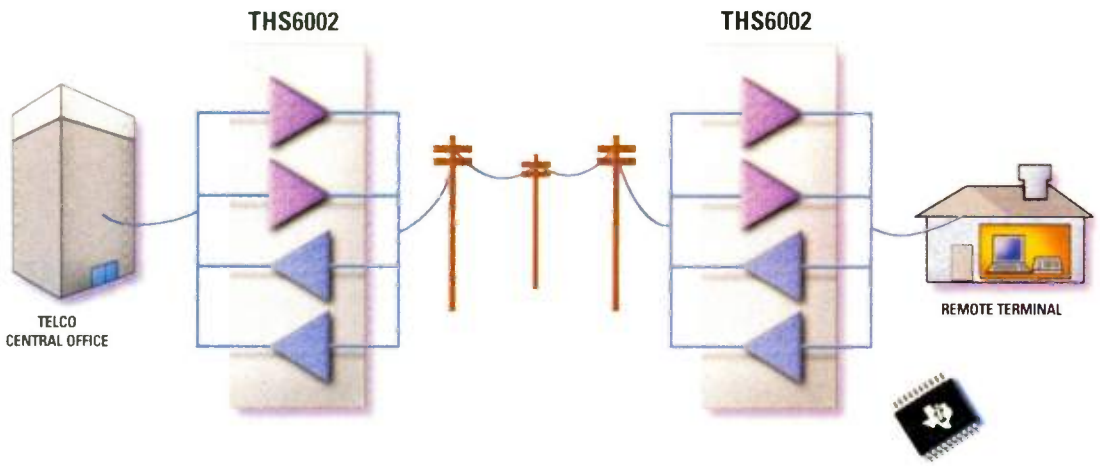
This system was designed with another in mind, the SoftwareNow store. This system allows @Home users to download titles typically available from online software stores. But, they are still small enough that they can be stored on the user's hard drive. @Home subscribers can either download software applications from SoftwareNow, or go through this new platform to gain instant access to titles that take up large amounts of disk space.

For more information, visit either @Home's web site, at www.home.net or Arepa's site at www.arepa.com.

Lisa Calabrese is a senior at Stevens Institute of Technology, Hoboken, N.J. Her major field of study is computer engineering.



INTRODUCING THE LOWEST DISTORTION xDSL LINE DRIVER/RECEIVER.



The THS6002 line driver/receiver from only $5.67*

- *THD = -72 dB @ 1 MHz (40 V_{pp}, R_L = 50 Ω)*
- *500-mA output drive*
- *Separate power supplies for each amplifier minimize crosstalk*
- *20-pin thermally enhanced surface-mount SOIC PowerPAD package*
- *EVM available*

**Price is per device in quantities of 1,000.*

High-speed xDSL Internet access technology requires drivers and receivers that transmit high data rates over low-impedance telephone lines with minimal distortion. The THS6002 from Texas Instruments is the answer. Its high 500-mA output drive and fast 1,000-V/µs slew rate combine to ensure ultralow THD under heavy loads. This integrated solution minimizes crosstalk by providing separate power supply connections to each amplifier. And because the THS6002 is packaged in TI's innovative surface-mount SOIC PowerPAD™ package, more heat can be dissipated in less PCB space than with heat sink or plug-type thermal packages.

For data sheets, PowerPAD application notes and EVM information, contact us at:
1-800-477-8924, ext. 5061, or www.ti.com/sc/5061

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JUST 4 THE KIDS

As the first day of another school year quickly approaches, many of us scramble to find fun ways to help our children brush up on their reading and math skills. You want your child to be prepared for the new school year. Like many other parents out there, you are probably searching for something—anything—to occupy your child's time in a productive way.

If this describes your situation, the New York-based Scholastic Incorporated may have just the thing for you. Their new CD-ROM, entitled I SPY, is so much fun that your child won't even realize they are learning. The "I SPY" CD-ROM was developed to accompany the popular series of photographic "I SPY" books, written by Jean Marzollo and Walter Wick. Intended for children ages five to nine, it brings the popular riddle books into the interactive world.

Like the book, the child "spies" objects in photos. But, the child also interacts with them and watches them come to life. This is made possible through the use of high-powered graphics, computers, and sophisticated two- and three-dimensional animation software. For example, selecting a photo-realistic butterfly causes it to flap its wings, lift up off the page, and fly to another place—complete with sound effects. The child can also use the mouse to click-and-drag an egg over to a nest, or draw a chalk line between two images to establish a relationship. The child interacts with the story's content in a way that is not possible in the I SPY books.

The basic object of this CD-ROM is to solve verbal riddles by finding objects hidden in densely populated pictures. To help find tiny items, it even provides a magnifying glass. The puzzles and riddles, as well as more than 1300 objects and word searches, are nestled within seven challenging games on the I SPY CD-ROM. These include the Balloon Popper, Code Breaker, Oops Hoops!, Make Your Own I SPY, Wood Block City, Nature, and Chalkboard.

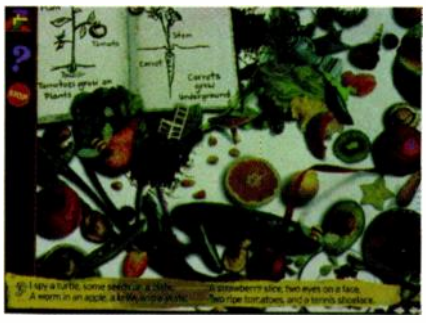
Each game is intended to help your child develop many essential skills, such as rhyming, logic and reason, math concepts, and strategic thinking. A parent's guide included in the CD-ROM describes the educational benefits of each game. The guide also offers ideas for fun family activities, which keep the child learning even when they're off the computer.

MARIFRANCES WILLIAMS

The 3D Balloon Popper game puts problem-solving skills to work. By putting devices together from parts found on-screen, your child makes a "Rube-Goldberg" contraption actually work. The child uses vocabulary and spelling to decipher three "clue" codes to solve an "answer" code in Code Breaker. A timer keeps track of how long it takes to solve the code and records the best solving time.

Oops Hoops! challenges the child to use visual discrimination and problem-solving skills to categorize objects according to multiple characteristics. To find items hidden from view in the 3D Wood Block City, the child must change perspectives.

The Nature Game consists of nine layouts, each with two or three riddles. Each layout ties into a specific nature theme, such as the beach, desert, or insects. The child listens to a riddle, and then figures it out using reading, vocabulary, and cause and effect. The child then hunts for objects requested in the riddle.



I SPY's Chalkboard activity taps visual memory and associative thinking. The child must hunt for objects while completing connect-the-dot puzzles, which helps them improve these skills.

By successfully solving riddles in Chalkboard, Nature, and Wood Block City, your child earns treasures from the Make Your Own I SPY treasure bin. Using these treasures, the child can create their own puzzles or riddles for friends to solve.

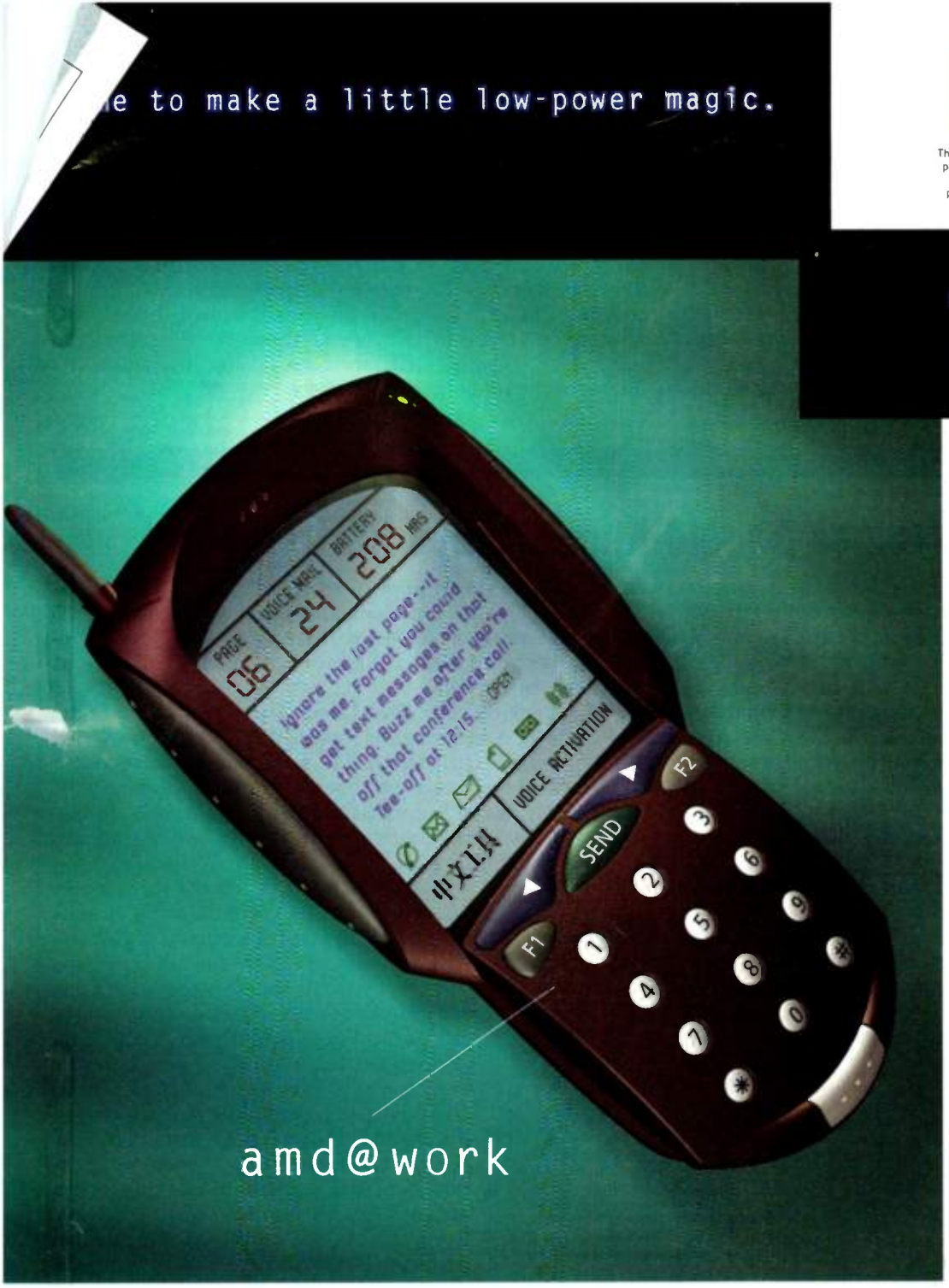
So, as the summer afternoons begin to stretch out, and you find yourself looking forward to school starting, you might take a look at the I SPY CD-ROM. Your child will enjoy a variety of fun and challenging games. And, you will reap the benefit of having exposed your child to a number of higher-level cognitive skills which are essential to learning.

The I SPY CD-ROM is now available in stores and sells for approximately $29. It's also available through Scholastic's Software and Book Clubs. In the fall, look for the I SPY CD-ROM to be packaged with the new I SPY mystery book and puzzle. If your child enjoys the CD-ROM and likes a challenge, there's also the *I SPY Super Challenger* book.

For more information, contact Scholastic Inc., 555 Broadway, New York, NY 10012-3999; (212) 343-7100; www.scholastic.com.

Marifrances D. Williams holds a degree in Liberal Studies from San Diego State University, Calif. She is currently a fifth-grade teacher at Los Ranchos Elementary, San Luis Obispo, Calif. Williams specializes in the identification of advanced technology for the use of child-focused applications. She may be reached at williamsofsm@lightspeed.net.

e to make a little low-power magic.



The Am29SL800: the first 1.8V-only, read, program and erase flash device. Our flash family offers a number of product and packaging options—including chip scale packaging—from which to choose.

Full Function 1.8V Flash

While you're reshaping things with 1.8V, we'll be busy developing the first 0.9 volt flash device for a generation of products yet to come.

This remarkable Perpetua cell phone from Studio Red is not yet available. But the flash technology that's making it possible is here today. From AMD.

For a data sheet, packaging information and links to other Flash memory products, visit

www.amd.com/magic/

If you doubt the existence of magic these days, wait 'til you see what's possible with an advanced piece of silicon like the Am29SL800. This remarkable 8 megabit, 1.8-volt-only flash memory chip is your opportunity to develop exceptionally low-power designs with extended operating life and a myriad of features. (Thanks in no small part to our advanced power management system with zero-power operation.) Next-generation cell phones can now offer increased levels of talk and standby time long enough to exhaust the most conversationally-addicted. So what's the easiest way to begin making it happen? That's no trick at all. Simply call 1-800-222-9323 or visit our Web site.

AMD

www.amd.com

Networking On A Smaller Scale

There's a new web site on the horizon, and it's designed to make networking easier. NDC Communications Inc., Sunnyvale, Calif., is a leading supplier of networking products for both home offices and smaller companies. NDC specializes in solutions for workgroup networking and wireless LAN connectivity products.

The new NDC web site, found at *www.sohoware.com*, was designed as a "how-to" page. It shows novice users and retailers the basics of networking, as well as its benefits.

According to Andy Chang, vice president of marketing at NDC, consumers want quick and easy networking solutions. The site should help NDC meet its customers' needs.

The site has the simple look of NDC's SOHOware product line. It is easy to navigate pages containing SOHOware products, retail sales tutorials, distributor listings, retailers and catalogs which carry SOHOware, service and support, and news updates.

For more information, contact NDC Communications, 265 Santa Ana Ct., Sunnyvale, CA 94086; (800) 632-1118; www.ndclan.com.—**NK**

TIPS ON INVESTING

Ten Things Women Should Know About Retirement

When we listen to tips about investing, we often overlook the fact that men's investment needs differ from women's. Henry's Tips below are important factors to consider for a new generation of female engineers.-Ed.

1. You are likely to live a long life. Anticipate that and plan accordingly. According to the U.S. Census Bureau, a woman who reaches age 50 today without serious health problems statistically can anticipate celebrating her 92nd birthday.

2. Statistically, there's a good chance that you'll outlive your spouse. Women, on average, outlive their spouses by about seven years. If investing has not always been a priority, you should start learning it now. (Source: The National Center for Health Statistics, Vital Statistics of the United States, annual estimates for women born in 1990)

HENRY WIESEL
CONTRIBUTING EDITOR

3. Pay yourself first. Invest in your future now. By investing systematically over a period of time, instead of paying monthly bills first and then saving whatever is left, you will be surprised how fast your nest egg can grow. Using Smith Barney's Systematic Withdrawal and Investment Schedule (SWIS), you can "pay yourself first" by purchasing shares of Smith Barney's funds or selected other mutual funds.

4. Fund your 401(k) or other employer-sponsored program to the maximum. You can build up a good portion of your retirement savings if you contribute at least as much as your employer will match into deferred-income. The tax-deferred compounding feature of these plans allows you to accumulate more than you would in a comparable account, which taxes earnings each year.

5. Choose an IRA that's right for you. Use the Roth IRA—a government giveaway. Our complimentary analysis, using the IRA & Pension Calculator, compares the projected results of contributing to different types of accounts. It also measures the outcome of transferring assets from a Traditional IRA to a Roth IRA.

6. Before you switch jobs, check on your complete benefits package, and the portability and vesting rules of your retirement plan. The U.S. Bureau of Labor Statistics reports that, on average, working women over age 25 switch jobs every 4.8 years. This prohibits the growth of retirement plan vesting requirements, which are often set at five years.

7. Check on your Social Security benefits. The Social Security Administration reports that 66% of retirees rely on Social Security for half or more of their income, with the average monthly payment for women totaling $601. Clearly, Social Security should be thought of as supplementary income during retirement, and not a main source of funds.

8. Beware of being overly conservative in your investments. There is a correlation between your age and the amount of risk you should assume when investing. But being too conservative could seriously erode the value of a retirement account that you may need to rely on for thirty years or more. Think of retirement as a long-term investment. Consider keeping a significant portion of your portfolio invested in stocks for as long as possible.

9. Consider long-term health insurance. You can't afford to ignore this important insurance need. The cost of spending a year in a nursing home could run as high as $60,000 or more. It could easily deplete your entire retirement reserve. (Source: Health Insurance Association of America, 1994)

10. Don't leave everything up to Uncle Sam. You owe it to your heirs to establish an appropriate estate plan. Without proper planning, estate taxes (which may range from 37% to 60%), state taxes, and income taxes on retirement plan distributions could reduce your estate by over 75% (if the majority of your assets are in qualified plans and individual retirement accounts). Essentially, your heirs may receive only a fraction of all you've worked so hard to accumulate.

For free information on establishing Retirement IRAs, and help with 401(k) choices, contact Henry Wiesel, Vice President-Investments, Qualified Plans Coordinator at Smith Barney, 1040 Broad St., Shrewsbury, N.J. 07702; (800) 631-2221 ext. 8653.

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- Prototypes in two weeks
- J.I.T. delivery

M Series
Moduflex® Power Supplies

- 1,000,000 + Models
- 250 - 1500 Watts
- 1 - 7 Outputs
- AC and DC Inputs
- Competitive Prices

Deltron inc.
POWER PRODUCTS

M ■ DM ■ VX SERIES MODUFLEX® SWITCHERS

DESCRIPTION

Moduflex® Series form a comprehensive line of open frame power supplies assembled from standard "off the shelf" modules. The design features "State of the Art" topology, a meticulous thermal structure and the use of high efficiency circuits and components to attain the desired power density. The modular system concept reduces manufacturing to submodule assembly, capable of high volume production with a superior quality level at moderate costs.

M Series are available in output power ratings from 250-750 watts. **DM Series** are available with a 48VDC input and output power ratings of 400 and 600 watts. **VX Series** units consist of four specialty units with output power ratings of 500, 750, 1000 and 1500 watts having the VXI standard voltages and currents.

Three classes of output modules are available. The **STANDARD** outputs allow short duration surge currents on all auxiliaries for hard starting loads. Optional **CURRENT LIMITED** outputs have square current limiting and feature wireless droop current sharing. Optional **ENHANCED** outputs have square current limiting, one wire star point current share, output good logic signal with LED, nominal 5V local bias, individual inhibit and margining. For requirements that cannot provide minimum load on the main output, the **ZERO PRELOAD** option is available for main outputs up to 500 watts.

DELIVERY

Choose stocked units or construct a model number using stocked modules for fast delivery. Otherwise, form a model from the adjacent page to meet your specific requirements. Contact factory for deliveries on models derived from non-stocked modules.

FEATURES

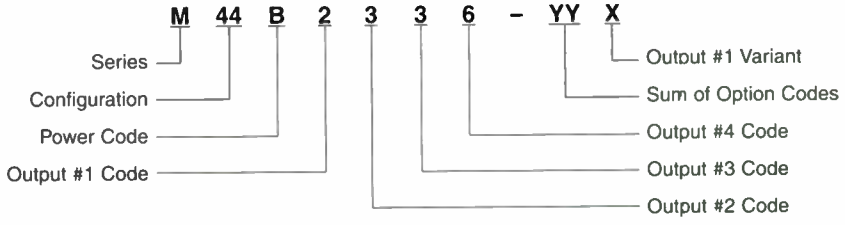
- UL, CSA, TÜV (IEC, EN), CE.
- 6 watts per cubic inch.
- 1-7 outputs, 250-1500 watts.
- AC & DC input models.
- VXI rated specialty models.
- 120 kilohertz MOSFET design.
- All outputs:
  - *Adjustable*
  - *Fully regulated*
  - *Floating*
  - *Overload and short circuit protected*
  - *Overvoltage protected*
- Standard features include:
  - *System inhibit*
  - *Load proportional DC fan output*
- Options include:
  - *Auto ranger*
  - *VME/VXI Monitor*
  - *End fan cover*
  - *Top fan cover*
  - *Current Limited Outputs*
  - *Enhanced Outputs*
  - *Zero Preload*
- Fast delivery.
- Replaces expensive high density systems using potted modules.

STOCKED MODELS - Available in 3 days.

Max Power	Output 1	Output 2	Output 3	Output 4	Model*
425W	5V @ 50A	12V @ 12A	5V @ 10A	12V @ 6A	M44R2323-47P
425W	5V @ 50A	24V @ 6A	12V @ 6A	12V @ 6A	M44R2633-47P
600W	5V @ 60A	12V @ 12A	12V @ 12A	5V @ 10A	M46C2332-47P
600W	5V @ 60A	12V @ 12A	24V @ 6A	12V @ 6A	M46C2363-47P

**Models shown in table include power fail monitor, auto ranger, current limited modules, zero preload and end fan cover options. 600W models Case #3.*

UNITS FROM STOCKED MODULES - Available in 2 weeks.



Configuration: Allowable quad output configurations are 42, 44, 46 and 48.
Power Code: Choose Power Code P, R, A through D for 250-750W models.
Output Codes: Select any outputs from the shaded area on the Output Types table consistent with the configuration chosen.
Option Code: Specify Option Code. Refer to the Option table. Codes 02 (redundancy) and 16 (enhanced) are excluded from models available in 2 weeks.

OPTIONS

Option Code	Function
00	None
01	Power Fail Monitor
02	Auto Ranger
04	Current Limited
08	Zero Preload
16	Enhanced
32	End Fan Cover*
64	Top Fan Cover

*Replace the YY with the sum of the option codes. *600 & 750 watt units require Case 5.*

MODEL SELECTION

Models are available in power ratings of 250 to 1500 watts, with corresponding code letters P, R and A through D. See Power Code chart. Contact factory for 1000 and 1500 watt models.

Output modules are available in six types—J, K, L, M, N and P in nominal power outputs from 75-500 watts. Type M, N and P modules are variable power rated depending upon the unit power rating. The M, N and P Module table directly below shows the corresponding multiplier applicable to the output current ratings of the M modules and allowable power ratings for the N and P modules. For example, a 750 watt multiple will have its M type module configured to produce 120A @ 5V or 12A @ 48V. The voltage and current rating of output modules are listed in the table of output types. This table assigns an alpha-numeric code designating the nominal voltage rating of the module.

Power Code	Unit Power Rating	M Module Current Multipliers: Single Output	M Module Current Multipliers: Multiple Output	N/P Module* Allowable Power Ratings
P	250W	0.5	0.3	175W
R	425W	0.85	0.5	250W
A	400W	0.8	0.6	250W
B	500W	1.0	0.8	300W
C	600W	1.2	1.0	400W
D	750W	1.5	1.2	500W

**When an N or P module is used as the main output, the allowable power and the module current ratings must not be exceeded.*

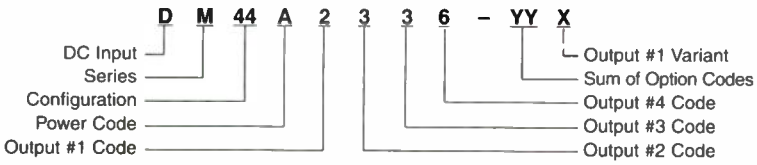
Output Types*						
Output		Module Type				
Code	Volts	J Amps	K Amps	L Amps	M Amps	N/P Amps
0	2	10	20	30	100	60
1	3.3	10	20	30	100	60
2	5	10	20	30	100	60
3	12	6	12	24	42	42
4	15	5	10	20	33	33
5	18	4	8	16	28	28
6	24	3	6	12	21	21
7	28	2.5	5	10	18	18
8	36	2	4	8	14	14
9	48	1.5	3	6	10	10
A	2.2	10	20	30	100	60
B	2.4	10	20	30	100	60
C	2.7	10	20	30	100	60
D	3	10	20	30	100	60
E	3.6	10	20	30	100	60
F	4	10	20	30	100	60
G	4.5	10	20	30	100	60
H	5.7	10	20	30	90	60
J	6.3	10	20	30	80	60
K	7	9	18	30	70	60
L	8	8	16	30	62	60
M	9	8	15	30	56	56
N	10	7	14	30	50	50
P	11	7	13	27	45	45
Q	13.5	6	11	22	37	37
R	17	5	9	18	30	30
S	19	4	8	16	26	26
T	21	4	7	14	24	24
U	23	4	7	13	22	22
V	26	3	6	12	19	19
W	29	3	5	10	17	17
X	32	2	5	9	16	16
Y	40	2	4	8	13	13
Z	44	2	4	7	12	12

*Multiple output modules of a given type are arranged in ascending order by voltage magnitude in the same sense as the output number sequence in the configuration diagrams. *Shaded ratings are stock.*

HOW TO ORDER

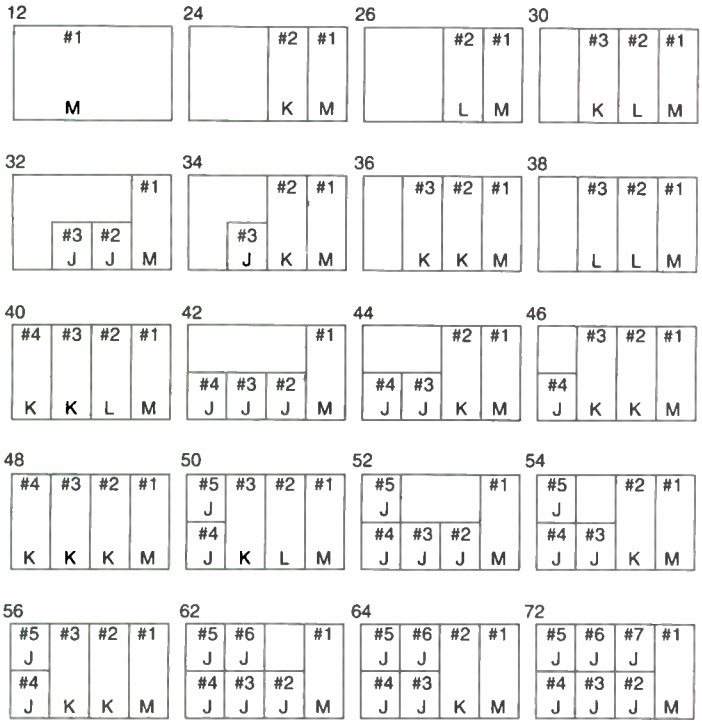
To form the proper model number defining a custom requirement, select the letters M or DM to designate the series, then choose the desired configuration of output modules and list the configuration code. Insert the power code letter for the power level and follow with the output code numbers or letters for each specific output. Enter a dash and from the option table insert the sum of the option codes. Where lower power is desired for the main module, an N module can be substituted and is denoted by a letter N in the output variant position. In addition, when no preload is available for the main output, choose Option Code 08 and add a P in the output variant position. For an **enhanced** main and **current limited** auxiliaries, specify both 04 and 16 option codes.

MODUFLEX 400W QUAD SWITCHER



OUTPUT CONFIGURATIONS

The boxes below are diagrammatic representations of the power supplies as viewed from the output end. The two-digit numbers above the boxes are the configuration codes.



Refer to the table below for allowable configurations by series.

Output Configuration	Unit Power Rating: 250W	400W	425W	500W	600W	750W
12	x	• x	x	x	• x	x
24	x	• x	x	x	• x	x
26					• x	x
30					• x	x
32	x	• x	x	x	• x	x
34	x	• x	x	x	• x	x
36		• x	x	x	• x	x
38					• x	x
40						x
42	x	• x	x	x	• x	x
44		• x	x	x	• x	x
46		• x		x	• x	x
48		• x			• x	x
50						x
52		• x	x	x	• x	x
54		• x		x	• x	x
56		• x			• x	x
62		• x		x	• x	x
64		• x			• x	x
72		• x			• x	x

• Represents allowable configurations for the DM Series.
x Represents allowable configurations for the M Series.

SPECIFICATIONS

INPUT
90-132 VAC or 180-264 VAC, 47-63 Hz. Strappable. 40-60 VDC for DM Series.

EMISSIONS
FCC 20780 Part 15/EN 55022, Class A Conducted.
EN 61000-3-3, Voltage Fluctuations.

IMMUNITY
IEC 1000-4-2/EN 61000-4-2, Electrostatic Discharge. IEC 1000-4-3/EN 61000-4-3, Radiated Field. IEC 1000-4-4/EN 61000-4-4, Electrical Fast Transients. IEC 1000-4-5/EN 61000-4-5, Level 3 Surge. IEC 1000-4-6/EN 61000-4-6, Conducted Field.

INPUT SURGE
34 amps peak from cold start for units under 400 watts, 68 amps for other models.

EFFICIENCY
75% typical.

HOLDUP TIME
20 milliseconds after loss of nominal AC power. 3 milliseconds for DM Series.

OUTPUTS
See model selection table. Outputs are trim adjustable ±5%.

OUTPUT POLARITY
All outputs are floating from chassis and each other and can be referenced to each other or ground as required.

LINE REGULATION
Less than ±0.1% or ±5mV for input changes from nominal to min. or max. rated values.

LOAD REGULATION
±0.2% or ±10mV for load changes from 50% to 0% or 100% of max. rated values.

MINIMUM LOAD
Main output requires a 10% minimum load for full output from auxiliaries. Use Option 08 if no minimum load is available for mains up to 500 watts. Singles require no minimum load.

RIPPLE & NOISE
1% or 100 mV, pk.-pk., 20 MHz bandwidth.

OPERATING TEMPERATURE
0-70°C. Derate 2.5%/°C above 50°C.

COOLING
A min. of 6 LFS* for models under 400 watts, 10 LFS for others, directed over the unit for full rating. Two test locations on chassis rated for max. temperature of 90°C. For convection ratings consult factory.
*Linear feet/second.

TEMPERATURE COEFFICIENT
±0.02%/°C.

DYNAMIC RESPONSE
Peak transient less than ±2% or ±200 mV for step load change from 75% to 50% or 100% max. ratings.

RECOVERY TIME
Recovery within 1%. Main output - 200 microseconds. Auxiliary outputs - 500 microseconds.

SAFETY
Units meet UL 1950, CSA 22.2 No. 950, EN 60 950, IEC 950.

ISOLATION
Conforms to safety agency standards.

INPUT UNDERVOLTAGE
Protects against damage for undervoltage operation.

SOFT START
Units have soft start feature to protect critical components.

OVERVOLTAGE PROTECTION
Standard on all outputs. VX Series - standard on main output.

REVERSE VOLTAGE PROTECTION
All outputs are protected up to load ratings.

OVERLOAD & SHORT CIRCUIT
Outputs protected by duty cycle current foldback circuit with automatic recovery. Standard auxiliaries have additional backup fuse protection. Options 04 and 16 have square current limiting with automatic recovery when overload is removed.

THERMAL SHUTDOWN
Circuit cuts off supply in case of local over temperature. Units reset automatically when temperature returns to normal.

FAN OUTPUT
Nominal 12 VDC @ 12 watts maximum.

INHIBIT
TTL compatible system inhibit provided. Option 16 has individual output inhibit.

REMOTE SENSING
On all outputs except standard and 04 Option outputs 75 watts or less.

SHOCK & VIBRATION
Shock per MIL-STD 810-E Method 516.4, Procedure I. Vibration per MIL-STD 810-E Method 514.4, Category 1, Procedure I.

MECHANICAL

CASE	WATTS	H		W		L	
1	250W/425W	2.50"	x	4.15"	x	8.00"	
2	400W/500W	2.50"	x	5.05"	x	9.00"	
3	600W/750W	2.50"	x	5.20"	x	9.63"	
4	600W/750W	2.50"	x	6.50"	x	9.63"	Config. 40 & 50 only.
5	600W/750W	2.50"	x	6.00"	x	9.63"	Option 32 only.
6	1000W	5.00"	x	5.05"	x	10.40"	
7	1500W	5.00"	x	5.20"	x	11.00"	

OPTIONS

POWER FAIL MONITOR
Optional circuit provides isolated TTL and VME/VXI compatible ACFAIL signal providing 4 milliseconds warning before main output drops by 5% after an input failure. A SYSRESET signal following VME timing requirements is provided when an N module is used as a main output. Both logic signal outputs can sink current per the VME specification.

AUTO RANGER
Optional circuit provides automatic operation at specified input ranges without strapping. Not applicable to DM Series.

CURRENT LIMIT
Option provides on all outputs:
- Square current limit with auto recovery.
- Wireless droop current share for parallel or N+1 redundant operation.

ZERO PRELOAD
Optional circuit removes need for preload on main output. Available for mains up to 500 watts.

ENHANCED
Option provides on all outputs:
- Square current limit with auto recovery.
- Single wire active current share for parallel or N+1 redundant operation.
- DC output good logic signal with LED indicator.
- Logic inhibit.
- Nominal 5V bias.
- Margining.

END FAN COVER
Optional cover with brushless DC ball bearing end fan which provides the required air flow for full rating.

TOP FAN COVER
Same as above with fan mounted on top of the power supply.

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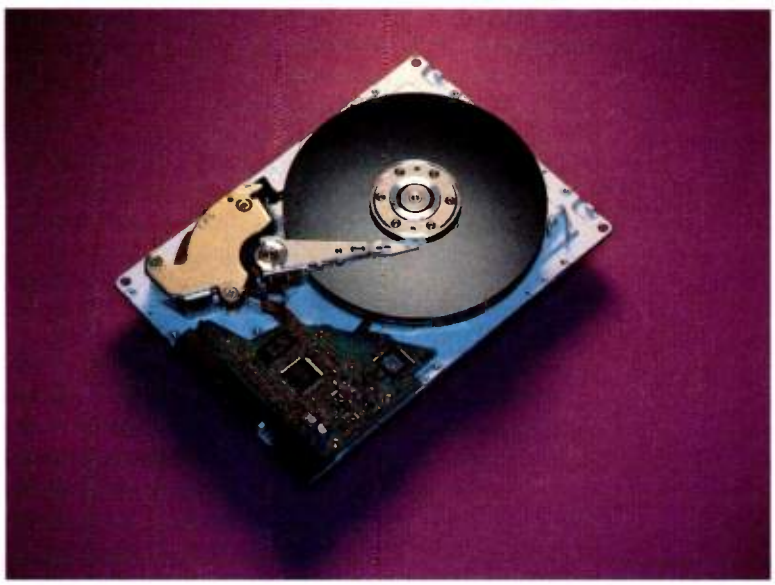
Technologies Vie For The Next Wave Of Disk-Drive Interfaces

Steady And Dramatic Evolution In The SCSI And IDE/ATA Interface Schemes Holds Competing Serial Schemes At Bay.

Jeff Child

SPECIAL REPORT

Parallel buses have traditionally been the only way to interface to disk drives, sending bits across cables, side by side, shoulder to shoulder, like soldiers marching off to battle. As buses grow wider, and the demand for bandwidth soars, it's difficult to go to wider cables and bigger connectors. There's an insatiable desire for more hard-drive density in desktop computers and fast access to that storage. And, massive amounts of data is moving back and forth between powerful servers—as well as to, from, and between huge hard drives.



Art Courtesy: Quantum Corp.

For years, designers had only two data-storage interface choices: small-computer-system interface (SCSI) and intelligent drive electronics (IDE). Previously, they had a ton of interface protocols to sift through. Because the number of parallel lines can't be increased infinitely, an alternate way to speed data transfers between computers and their storage peripherals is to put data words into packets, and ship them over high-speed serial links. That's been the argument for new serial standards moving into the disk-drive interface realm. Inside computer systems, the 1394 standard is a likely contender to the tried-and-true Enhanced-IDE ATA interface. For external connections and high-end systems, Fibre Channel is one serial technology vying to usurp SCSI's throne.

Choosing the serial route offers many advantages over parallel designs. First, you can connect over a greater distance. Second, switching and routing are easier than with a parallel interface. Through switching and routing, you can make a given resource (either disk or tape) available to any host in the environment.

As these new serial-bus technologies compete for design wins, parallel interfaces like SCSI and AT-bus-attachment (ATA) still haven't moved from the fray. In fact, SCSI and ATA, at least for now, are winning their respective fights. While many believe that a switch to serial technology is inevitable, there's disagreement about when the parallel style will run out of steam.

Used in over 80% of all disk drives sold, IDE/ATA still is the mainstream drive interface. It's used in nearly all desktop computers. "IDE/ATA is not at all the prettiest interface, nor is it the most sophisticated," says Skip Jones, director of planning and technology at Q-Logic, "but it's enough for the PC." He continues, "What PCs need is something with the lowest cost using the fewest possible components. With IDE, there's no adapter involved. Its interface can be implemented in a gate count that soaks right into other chips already on the boards. The firmware rarely exceeds 10 kbytes. It's the path of least resistance, because it's the path of least cost and least change."

Two years ago, as the 1394 serial bus standard began to emerge, ATA was a contender for the future interface technology. Then 1394 became standard

and made some headway on consumer digital electronics—for digital cameras, printers, etc. Consumer electroncis leaders like Sony and Philips looked at 1394 as an interconnect between devices. Their vision was never to have a computer in the middle. In contrast, Microsoft and Intel want to see the computer in the middle. The argument went like this: Because 1394 is going to be in a PC anyway, why not just connect the disk drive off it, and eliminate the ATA interface? That would save pin counts for PC core-logic chip sets.

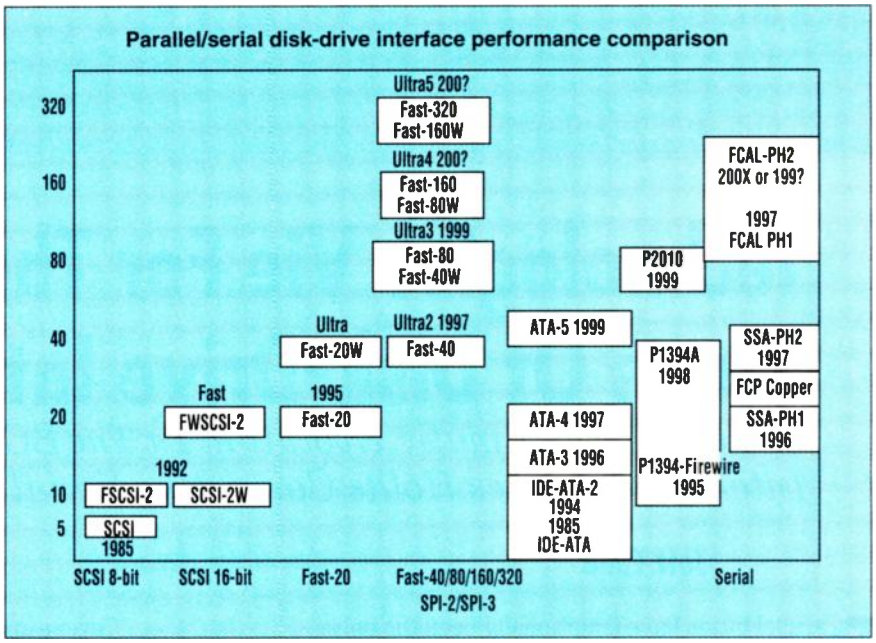
From a performance standpoint, at least, both the latest version of the ATA interface and 1394 have been perceived as potential candidates for the next PC-drive interface standard. IEEE 1394 was originally touted as a desktop LAN by Apple Computer. Since then, it has become a high-speed, "universal I/O interconnect" for linking PCs with all sorts of digital devices, including digital audio and video equipment, and computer peripherals such as hard drives.

Today, 1394 transmits data at up to 50 Mbytes/s—not much faster than the 33 Mbytes/s of the current PC-drive interface standard, Ultra ATA/33. But 1394 developers are working on a 100-Mbyte/s version that more closely matches real-time processing requirements of multimedia computing. That kind of performance, along with 1394's streamlined, scalable architecture; flexible peer-to-peer topology; and its ability to connect large numbers of devices on a single bus, makes it a likely enabler for home networks and other convergences between computer and consumer electronics. Consequently, 1394 has garnered considerable support from major computer players like Intel, Compaq, and Microsoft, as well as consumer electronics giant Sony.

Market-research predictions a few years ago said that by the end of 1998, 50% of hard drives targeted for PCs would feature the 1394 interface. Since it's already mid-1998, and no hard-drive vendor has shipped a 1394 drive, that forecast obviously missed the mark.

ATA Strikes Back

Meanwhile, the ATA interface has revved up to new speed levels. Drive vendor Quantum has developed Ultra ATA/66, an extension to the Ultra ATA/33 interface. The Ultra ATA/66 doubles the ATA/33 burst-transfer rate to 66 Mbytes/s, faster than current 1394 speeds. Unlike 1394, it also leverages mature, proven technologies to deliver fast data access plus other capabilities critical to data-intensive computing, such as enhanced signal quality and data availability.



1. For the first time in a decade, system designers have a choice of drive interface beyond IDE-ATA and SCSI. New serial bus alternatives have entered the game, for example, the 1394 serial bus intended for internal disk connections. And, Fibre Channel Arbitrated Loop (FC-AL) is challenging SCSI for high-end and external disk-drive links. As this performance comparison chart shows, however, neither 1394 nor FC-AL offers a compelling enough speed advantage over traditional solutions.

Over the past few months, Ultra ATA/66 has grabbed a substantial lead over 1394. Current adherents include all major hard-drive manufacturers and host-adapter suppliers, plus Intel, which recently postponed its support for 1394 in future interface controller chip sets. Intel now plans to introduce Ultra ATA/66 chips as an evolutionary step to 1394. Despite 1394's rosy picture, the first hard drives to support 21st-century desktop computing in a big way will be Ultra ATA/66 drives.

While the change to Ultra ATA/33 required some rewriting of protocols, the ATA/66 revision does not. The most significant ATA/66 revision change is that it needs an 80-conductor cable instead of 40. The connector does not change however. The 40 extra ground lines reduce crosstalk and improve signal integrity. A sensing mechanism lets the host know when the cable has the ground lines, so it won't send data at 66 Mbytes/s if a 40-conductor cable is used.

International Data Corp., Framingham, Mass., estimates that in 2001, hard drives with the 1394 interface will account for only about 10% of total PC drive shipments while Ultra ATA drives will capture the remaining 90%. The Ultra ATA/66 specification is ready for prime time, while 1394 is not.

Quantum presented the latest ATA interface to ANSI as a new industry standard this summer. Swift ANSI approval appears likely based on the specification's widespread industry support. That, in turn, will clear the way for hard drives and chip sets supporting Ultra ATA/66 to begin landing on the market by the middle of 1999.

Meanwhile, the 1394 100-Mbyte/s version—also known as S-800—remains at the early draft stage. Just as significant is the cost factor. Brand-new technologies are always expensive to implement, and a drive-level 1394 interface is no exception. A considerable amount of development still has to be done on the needed silicon, for example, which naturally makes producing 1394 controller chips more costly than rolling out Ultra ATA/66 devices.

1394 Is Costly

According to disk-drive vendor Quantum Corp., using the currently available technology, 1394 would add

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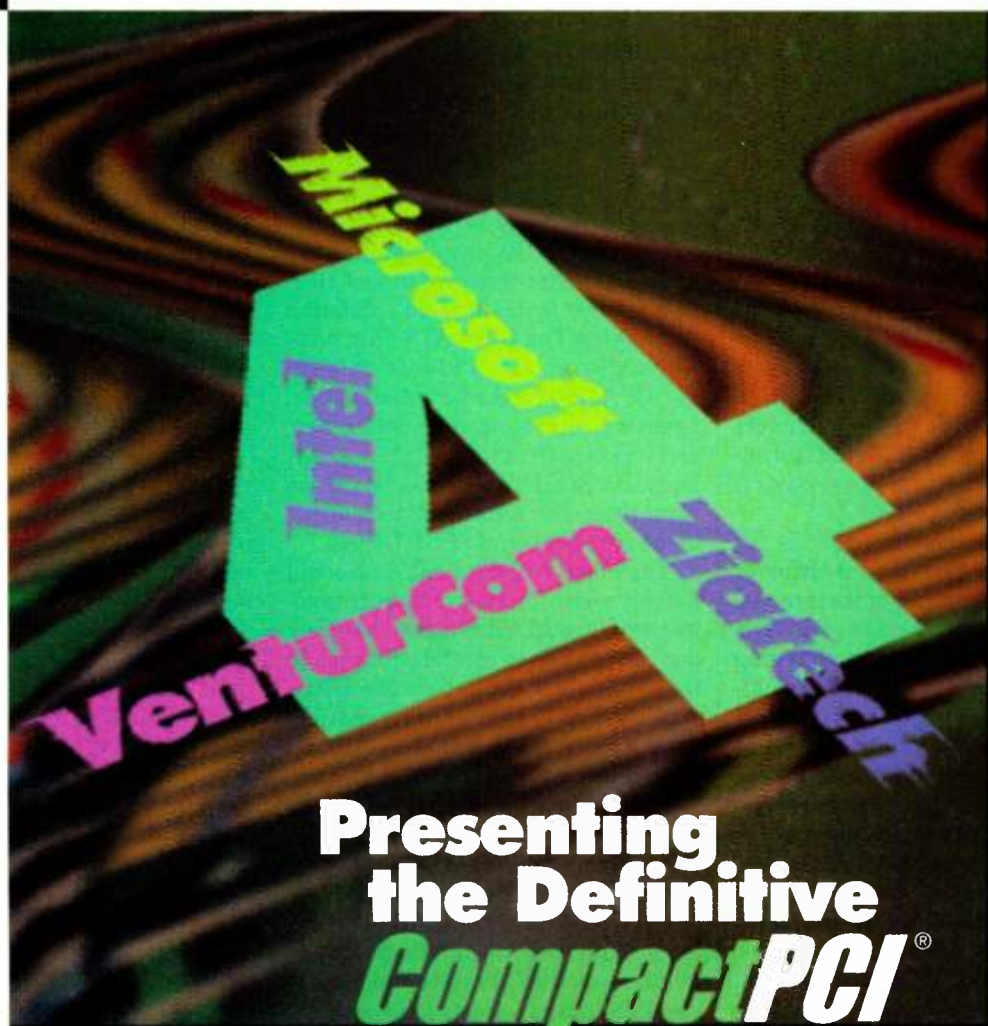

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$10 to PC costs on both the drive and host sides, compared with just pennies for Ultra ATA/66 implementations. Given the overriding trend in the desktop-computing arena toward sub-$1000 PCs, that kind of cost penalty currently knocks 1394 drives out of the running.

The hard-drive industry isn't abandoning 1394. As the technology falls down the cost and learning curve, most major drive vendors expect to begin developing 1394 product lines, possibly within four years. For several years after that, they will likely produce both 1394 drives and other drives featuring some variation of Ultra ATA technology to address the range of PC market requirements. Meanwhile, Ultra ATA/66 is poised to provide a much-needed transition to 1394 that can address PC users' data-access requirements at least until 2002.

Pushing the need for speed is the fact that a drive's external-transfer rate must keep ahead of its internal transfer speed to prevent the drive/host connection from bogging down. That's especially true for multimedia and other applications that produce large, complex files, which are typically read sequentially during file transfers between the drive and the host. Unless a drive's external-transfer rate significantly outpaces its internal transfers, the drive can end up filling its buffer faster during sequential reads than the host can empty it.

Because the new Ultra ATA/66 interface requires no changes to the Ultra DMA protocol, it also maintains 100% backward compatibility with current ATA systems and drives. Ultra ATA/66 uses the same cyclical-redundancy-check (CRC) technology proven in Ultra ATA/33 technology. CRC is a powerful data-protection-verification method for hard drives. With it, verification code is produced for each burst-data transfer by both the host and the drive, and is stored in their respective CRC registers. At the end of each burst, the host sends the contents of its CRC register to the drive, which compares it against its own register's contents.

The key to CRC is its significantly greater data-integrity assurance than that offered by traditional validation techniques. The Ultra ATA/66 specification also replaces a 40-conductor cable with an 80-conductor cable to ward against electronic noise interference, and enhance data integrity. Interestingly, the SCSI Trade Association has plans to use this same CRC technology in the next version of SCSI: Ultra3.

The noise-resistant cable also will make it easier for PC suppliers to qualify new Ultra ATA drives, because they don't have to be as careful with cabling inside the box. And, because Ultra ATA/66 is fully backward compatible with current ATA motherboards and controllers, it also will enable PC vendors and distributors to streamline their inventory management. It all adds up to considerable cost savings that can be passed on to end users.

Such backward compatibility also means that with Ultra ATA/66, IT organizations won't have to replace entire PC storage infrastructures to enable faster data access for functions or departments that need it. They can purchase Ultra ATA/66 drives and use them in newer ATA systems that take advantage of the higher-speed interface, and in older Ultra ATA/33 systems, where they will automatically fall back to Ultra ATA/33 speeds.

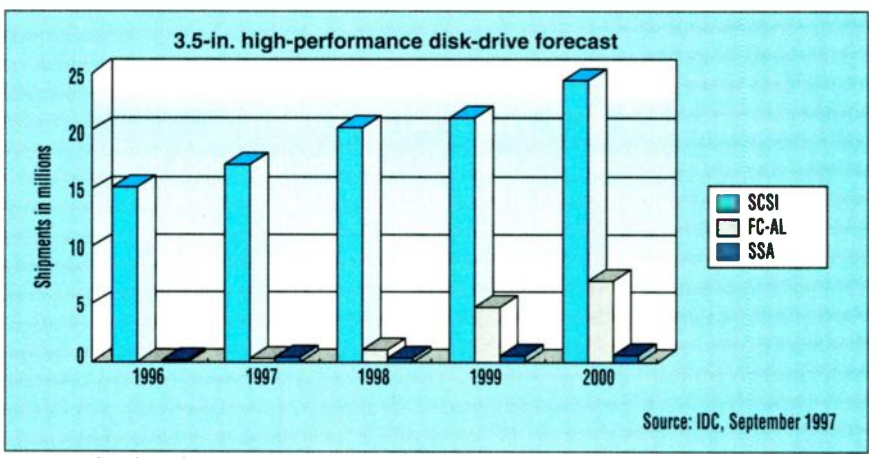
On the cost side, it looks like it will be some time before a drive-level 1394 interface can compete with Ultra ATA/66 for the general run of desktop-computing applications. The first "killer apps" for 1394 hard drives are shaping up to be desktop videoconferencing and other early manifestations of the computer/consumer-electronics convergence. In these environments, the connectivity capabilities of the 1394 serial bus will probably outweigh any lingering cost disadvantages compared with an Ultra ATA interface.

The necessary infrastructure support is already under development for 1394-enabled applications. For example, digital cameras using 1394 technology to interface with PCs are on the market, and 1394-based ROM drives will be appearing on desktop systems shortly. For applications that don't require industrial-strength connectivity, however, Ultra ATA technology has plenty of headroom left. Therefore, even when internal-drive transfer rates start catching up with Ultra ATA/66 speeds, drive vendors will continue leveraging a proven interface for the PC marketplace.

SCSI Versus Fibre Channel

For high-end disk drives, and external disk-drive links, SCSI has been the only game in town for decades (see *"The SCSI Standard: Past, Present, And Future," p. 70).* Like the ATA-versus-1394 fight, SCSI has its own serial bus rival in Fibre Channel. At one time, another alternative, IBM's Serial Storage Architecture (SSA) looked like a possible player, but that technology failed to get any support outside IBM. Fibre Channel appears well positioned in the market as the emerging technology for box-to-box (system-to-storage) connection schemes. Broader adoption is expected beginning next year in applications that require distances, or where less cabling clutter is required. Yet Ultra2 SCSI, with its low-voltage differential (LVD) signaling capabilities and new small form-factor connectors, has raised the bar for competition from Fibre Channel.

Systems designers from a SCSI



2. IDC market data shows steady growth in 3.5-in. hard drives. SCSI is expected to continue to dominate, while drives with FC-AL interfaces stake a niche. Meanwhile, the market for the Serial Storage Architecture (SSA), which has failed to achieve support outside IBM, isn't expected to grow.

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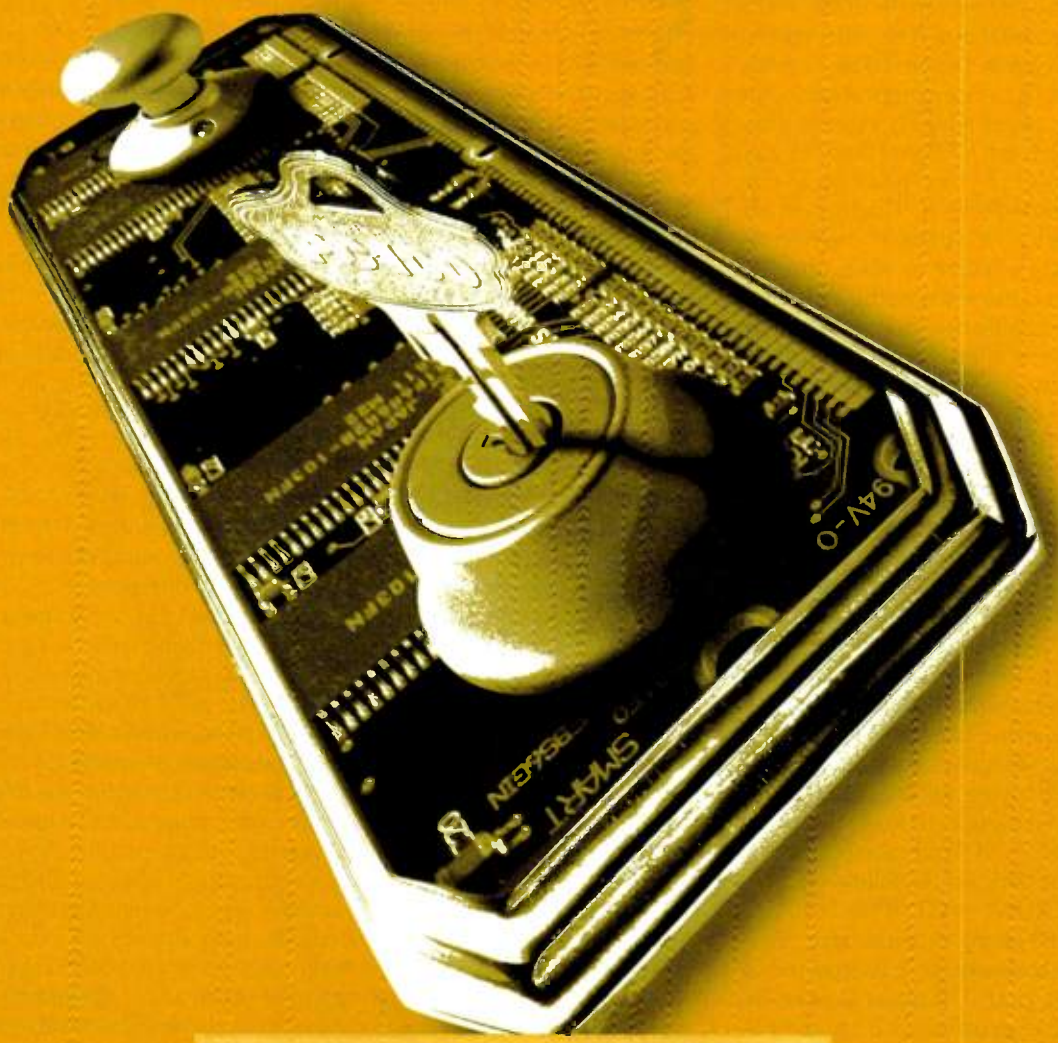

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background have to approach Fibre Channel carefully. In a sense, Fibre Channel tends to look more like a network (like Ethernet) than a channel. Designers coming from the SCSI world like to assume that a serial alternative is just as reliable. In parallel SCSI, with 15 devices and a few meters of cable, it's very easy to get a highly reliable link. In contrast, with Fibre Channel you have something that has a bit error rate associated with it. That means it's imperfect by definition. If you're running 10 km of fibre or other media, there's an inherent possibility of collecting errors. Fortunately, some of the developers of Fibre Channel were the original authors of SCSI. As a result, a lot of complexity was included in Fibre Channel to ensure its reliability.

Next: 160-Mbytes/s SCSI

For its part, the 80-Mbyte/s Ultra2-LVD SCSI is gaining widespread acceptance this year. The disk-drive industry is already shipping products with that technology. Ultra2 uses LVD signaling to overcome the skew problems at faster data rates. Now that the LVD transition in SCSI has already happened, designers are becoming familiar with laying out backplanes with differential signals to keep the skew down. The SCSI Trade Association is already working on the follow-on technology: Ultra3 SCSI. With transfer rates of 160 Mbytes/s, disk-drive products with that scheme are expected to ship next year. Ultra3 will even be backward compatible with ordinary 5-Mbyte/s SCSI.

As mentioned earlier, Ultra3 SCSI includes a new feature called domain validation. The concept is similar to what's done in modems, where a modem tests the line to see what speeds it can reliably run. This is expected to have significant implications in cost of ownership for system designers.

Rather than having to go through a laborious qualification for every possible configuration of a drive (SCSI, unlike ATA, has lots of configuration possibilities), the devices will be able, at run time, to test the physical connection. It can see if the user put in, for instance, substandard cabling, or made a Christmas tree out of the bus, etc. If it turns out that it's electrically unsafe to run at high speeds, than rather than just crashing, the drive will instead ne-

The SCSI Standard—Past, Present, And Future

SCSI remains the storage bus of choice for high-end PCs, workstations, and medium and high-end systems with a unique balance of cost and performance. Unlike some buses, it allows for flow control to avoid very large, high-speed caching memories. SCSI attaches hard, removable-media, optical and tape drives, plus CD-ROMs, CD recording systems, and high-end printers and scanners to PCs. Driven mainly by the SCSI Trade Association, SCSI has enjoyed a steady evolution in performance and functionality. From the 5 Mbytes/s of the mid-1980s to today's 80 Mbytes/s and tomorrow's 160 Mbytes/s, SCSI is keeping up with system performance needs.

SCSI began on PCs and workstations of the '80s, and worked its way up to the servers and high-end systems of the '90s, replacing proprietary buses, allowing common manufacturing of high-end storage devices, and dramatically reducing storage costs. SCSI-2, added a synchronous mode with 5- and 10-Mbyte/s rates. Unlike the original 8-bit data path, which allowed addresses for the controller and seven devices, SCSI-2 allowed for 16-bit data paths (16 addresses) and 32-bit data paths (32 addresses), with a second very awkward cable that was not accepted by the industry. The SCSI-3 wide bus, in the mid-'90s, changed the primary cable and became practical, resulting in 20-Mbyte/s rates with a single cable. During 1995 and 1996, Ultra SCSI emerged with a 40-Mbyte/s rate, effectively quadrupling the transfer rate in three years. The next year saw the introduction of Ultra2 SCSI using low-voltage differential (LVD) technology. This allowed longer distances, more devices, and twice the transfer rate, achieving 80 Mbytes/s. Maximum allowable cable length increased to 12 m for both narrow and wide Ultra2 SCSI, a significant increase over single-ended SCSI modes.

In addition, LVD signaling used in Ultra2 SCSI allows a maximum of eight (for narrow SCSI) and 16 (for wide SCSI) device loads. This increased the device loads allowed with the increased transfer rate—unlike its SCSI predecessors, where the number of device loads decreased from narrow to wide SCSI.

Significantly lower power consumption enables integration of LVD transceivers into SCSI protocol devices, giving Ultra2 a major edge over previous versions. LVD is not dependent on specific supply voltages, enabling migration to lower supplies such as 3.3, 2.5, or 2.0 V, while keeping the same signal levels and performance. LVD's constant current-mode drivers are independent of frequency changes. This allows for fairly constant driver power consumption over the operating frequency range, with most of the power dissipating at the termination. Ultra2 SCSI drive and interface chips are available from several vendors.

The T10 standards group within the National Committee for Information Technology Standards (NCIT) is starting to work on the next generation, Ultra3 and Ultra3P SCSI. These will allow up to 160-Mbyte/s rates by next year. At the heart of Ultra3/3P is the protocol interface specification, SPI-3, now in development in the T10 committee. It's running Fast-80, but uses both edges of the REQ and ACK clocks. The data and clocks now run at the same speed (at lower speeds, clocks run at twice the maximum data-line-change rate). CRC has been incorporated in the data phase for higher data integrity. Proposals for packetized SCSI, quick arbitration, and CRC are being reviewed, and will be in Ultra3P. The increased data rate begins to show the protocol overhead as a major factor; reducing the overhead will increase system throughput. A request was made for a 32-data-bit, single-cable system for SPI-3 capable of 320-Mbyte/s transfers for a point-to-point RAID or switch connection. The goal, for drive vendors, is to ship Ultra3 and Ultra3P devices in the first quarter of 1999.

Special thanks to Paul D. Aloisi, principal applications engineer at Unitrode Corp., Merrimack, N.H.; (603) 429-8687; aloisi@unitrode.com. Thanks also to Harry Mason, president of the SCSI Trade Association. For more information about the SCSI Trade Association, go to www.scsita.org. The T10 committee web site is www.symbios.com/x3t10. The National Committee for Information Tecnology Standards web site is www.ncits.org.

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Aside from domain validation, Ultra3 SCSI adds CRC error detection. As mentioned earlier, this same technology is used in ATA/33 and ATA/66 IDE drive interfaces. SCSI has traditionally used parity for error handling. "Parity has fundamental holes in it," says James McGrath, senior system engineer at Quantum. "Certain errors can manifest themselves at high speeds," he says. One example is intersymbol errors, where, on a given line, a proceeding bit that's being transmitted may affect the subsequent bit—and your ability to receive it.

At high speeds this is more likely to happen because you're packing the bits very tightly together in the time domain. "You really need something that's more of a longitudinal-type error-checking scheme; something that doesn't just check across all the bits off a given word, but also checks across the bits that are sent along one of lines on SCSI for multiple words," says McGrath. He continues, "that's what CRC brings. It provides both horizontal and vertical checking." Parity only provides the vertical checking (traditional word checking). Interestingly, CRC is far from new in the storage industry, going back to the 1970s. It was used in the original floppy-disk drives.

As SCSI creeps up in speed, the shift to Fibre Channel has become less urgent. Yet it offers a number of special features which attract some system designers. Fibre Channel provides long-distance connectivity, plug-and-play capability, and autoconfiguration—all the things that SCSI has tried to evolve toward through the years.

Fibre Channel is an ANSI standard that scales from 133 Mbits/s to 4 Gbits/s. It supports both channel and networking protocols. The heterogeneous interconnect scheme allows for any-to-any active/intelligent interconnections from tens to thousands of nodes designed for multiple, physical-media support (copper, fiber, mixed).

Fibre Channel has a bit rate of 266 Mbits/s, 531 Mbits/s, or 1062 Mbits/s. The bit rate of the data protocol is independent of media and distance. Using coaxial or twin-axial copper cables, you can connect Fibre Channel at up to 100 m. With short-wave lasers driving the fiber, the distance can be extended to 2 km. And, with a long-wave laser, distances of more than 10 km are possible.

With special engineering of the selection and connection, you can make a single length go much further (20-30 km). With repeaters, the link length can extend to hundreds of kilometers. Fibre Channel also offers several message classes, allowing for different operational, service, and cost environments.

Q-Logic, a maker of Fibre Channel disk-drive chips and adapter boards, has about 60 design-ins for its Fibre Channel technology. Most of those, they say, are box-to-box connections, using Fibre Channels' distance edge to connect to remote storage locations. "As much as we like to boast about 100 Mbytes/s in Fibre Channel, the reason people are adopting it so quickly is for connectivity and distances," says Q-Logic's Jones. "They get the ease of plug and play," he says. Most of those applications are using SCSI inside the systems. Today, you still only get a production Fibre Channel disk drive from Seagate at the same cost as a comparable SCSI drives.

"Moore's Law" For Storage

While system designers face some trade-offs these days, it's really only the disk-drive makers that have direct involvement in the densities of the media. They report a fairly bright future for increasing disk-drive density. They also have the head, read, and media technologies that will, for the foreseeable future, let them do the usual 60% increase every year in area density.

"That's our equivalent to Moore's Law," says Quantum's McGrath. "We double the capacity we can put on a piece of media every 18 months. And just as the semiconductor industry says they can't guarantee that for that next 15 years, we can't either."

Drive vendors get this boost partly by increasing linear-bit densities, or the number of data bits that can be aligned along each track on a disk. As linear-bit densities increase, a drive's internal-transfer rate naturally increases—even when drive rotational speeds stay the same. When drive manufacturers also boost rotational speeds, internal-transfer rates rise further. The upshot is that internal transfer rates typically get 35% to 45% faster every year. This continues to push the envelope out for disk-drive interface speeds.

For drive heads, the industry has, for the most part, made the transition to magneto-resistive head technology. That change allows drive vendors offer high capacities at reasonable prices. A year or two from now, drives will start to employ giant magneto-resistive heads. "Within a few years, you'll be seeing 100-Gbyte disk drives at very reasonable pricing," says McGrath.

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STANDARDS WATCH

Latest VESA Standard Gives Facelift To Plug-And-Display Solution

James E. Harris, Jr. and Ian Miller

Advances in PC graphics and multimedia technology have really exposed the limitations of the VGA display interface. Clearly, there's a need for a new, more expandable display interface. That's where the VESA Plug and Display standard, maintained within the VESA Display Committee, comes into play. It offers an industry-standard solution to the problems of changing display technology.

Increasing demand for high-quality, high-resolution, computer graphics displays has placed a new challenge on PC and monitor OEMs. The existing 15-pin, D-shell connector architecture is rapidly approaching the physical limits of its bandwidth. Nevertheless, applications continue to use larger display areas, and ergonomic display standards continue to tighten. Thus, a new analog interface is required to meet the resolution and refresh rates of tomorrow's PC applications.

Meanwhile, the introduction of low-cost, digital flat-panel monitors, and the growing trend toward merging consumer electronics with home PCs, have created a need for high-speed digital interfaces. A single digital interface which supports digital displays and other devices allows the development of more advanced multimedia systems. This brought about both "The VESA PC Theater Initiative" and "The VESA Home Network" (*ELECTRONIC DESIGN, April 1, 1997 p. 111*).

The VESA Plug and Display (P&D) standard published June 11, 1997, addresses these issues by providing a high-bandwidth analog interface, a robust digital-display interface, and support for the Universal Serial Bus (USB) and IEEE 1394 digital interfaces. P&D provides a clean interface with ample room for future expansion.

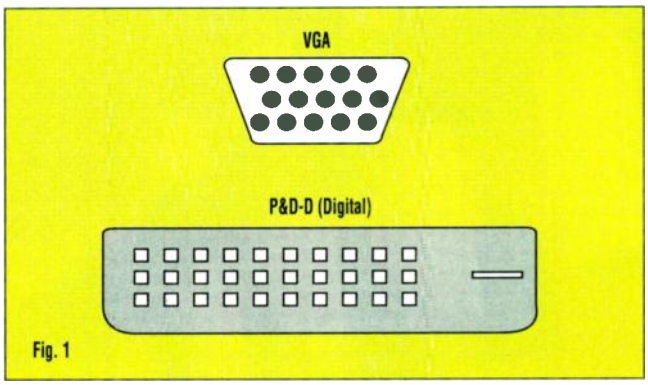


Fig. 1

Flexible Implementation

P&D is not a single, rigid solution, but a flexible set of solution options designed to meet the specific needs of the industry. To help the transition to this technology, the P&D standard defines a minimum implementation. The physical layer of this implementation, supporting a digital video interface only, consists of the P&D-D 30-pin connector with a minimum number of required signals (*Fig. 1*).

The next logical level of P&D implementation is P&D-A/D (analog/digital). It provides a way to support both analog and digital display interfaces on the same connector. TheP&D-A/D is implementation is similar to the P&D-D, but adds four quasi-coaxial signals for analog Red, Green, Blue video, and (optionally) a pixel clock with a cross-ground connection (*Fig. 2*). The Hsync, Vsync, and their returns are defined on pins not being used by the P&D-D connector.

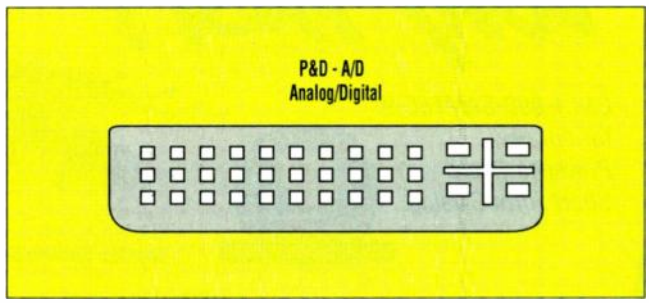
This approach has the benefit of allowing higher bandwidth analog connections, while maintaining the digital interface for flat-panel displays. P&D-A/D may be attached to legacy VGA displays by means of a dongle or alternate display cable.

P&D offers several optional signals for new functionality. For additional connectivity, both implementations of P&D may add USB, IEEE-1394, or both. For certain mobile applications, an optional charging pin has been defined. This pin permits notebook computers or other portable devices to recharge internal batteries from an externally powered display. The optional signals defined for P&D let display designers implement advanced features such as USB hubs and device bays into future monitors. It also allows display connectivity with consumer electronic devices.

P&D Expansion

The P&D connection has been carefully designed to maximize expandability while minimizing design difficulties. The analog interface is a prime example. Unlike the 15-pin VGA connector which has R, G, and B pins, with individual returns terminated at the host motherboard, the P&D connector borrows the Molex (Lisle, Ill.) MicroCross structure from the VESA EVC standard.

This standard comprises two mated, perpendicular ground planes (one cable, one host) arranged with the R, G, B, and (optionally) pixel-clock lines in a quasi-coaxial configuration. The improvement in bandwidth is quite dramatic. The VGA connector is limited to about 150 MHz, but P&D's analog configuration is capable of frequencies up to 2 GHz. The arrangement allows much longer cable lengths for analog displays than the 15 pin VGA, without creating EMI problems. The optional pixel-clock line makes it possible for the system digital-to-analog converter (DAC) to synchronize with an analog flat-panel dis-



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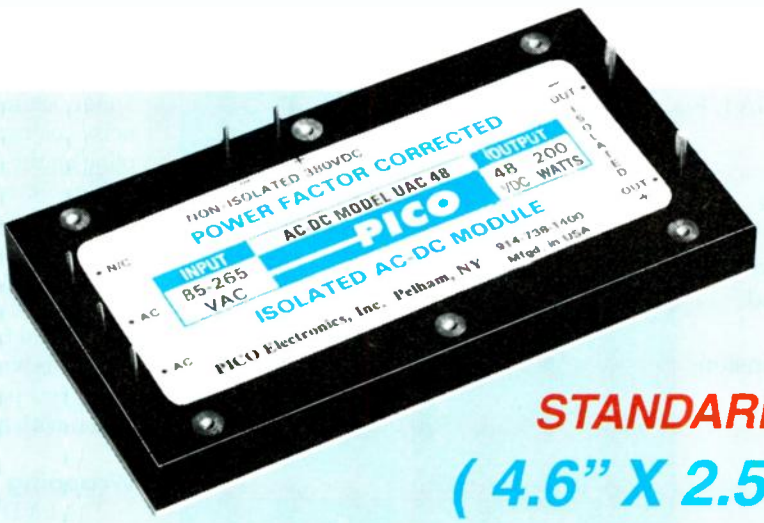

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play's analog-to-digital converter (ADC), removing many of the undesired visual effects associated with D/A-A/D systems.

P&D's mandatory digital interface is equally robust. The connector provides the pins for differential pairs necessary to support transition-minimized differential signaling (TMDS). TMDS provides a dc-balanced signal with a minimum number of transitions. It has been adopted as an industry standard for communication with flat-panel displays. Differential signaling provides a dedicated current return for every signal, providing very-high-speed transmission with excellent noise tolerance. P&D specifies ac coupling on the TMDS pairs.

The ac coupling removes any dc bias on the differential pair, and reduces occurrences of common-mode currents. This design allows longer cable lengths, looser power-supply tolerances, and better EMI performance. As of this writing, at least one P&D solution has passed FCC class B certification with a 10-m cable.

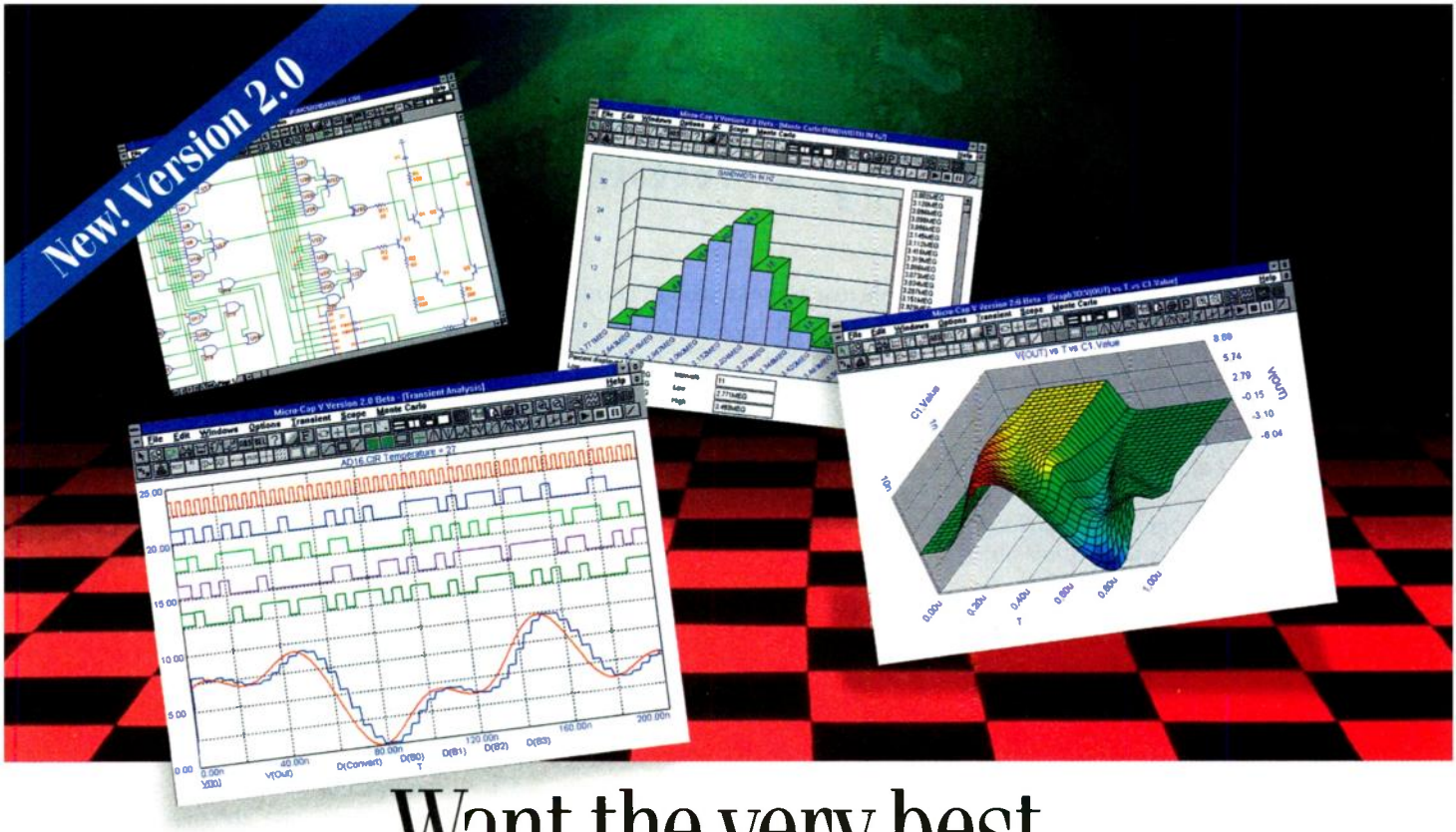
Wrapping Things Up

The P&D all-in-one cabling system, which includes TMDS, Analog, DDC2, USB, and IEEE-1394 in a single (long) cable gives system designers the ability to develop consumer PCs which merge home entertainment systems with computers. And, designers can produce commercial PCs which can be physically secured far away from the end user while still allowing the connection (through the display) of printers, scanners, and other self-configuring devices. Inclusion of USB and IEEE-1394 provides for future display functionality, helping to guarantee a long life for this standard.

For further information on the P&D standard, contact VESA at (408) 435-0333, or on the Internet at www.vesa.org.

James E. Harris, Jr. is a systems developer at IBM Corp. He can be reached at (919) 254-8163.

Ian Miller is a VESA board member and P&D committee chair. He can be reached at the IBM Development, Personal Systems Group, IBM UK Ltd., Greenock, Scotland; +44 1475 893530; or via e-mail: ian_miller @uk.ibm.com.



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READER SERVICE 151

A Peek Into Ray's Mailbox

Dear Mr. Alderman,

I recently read your interesting editorial in ELECTRONIC DESIGN. *Clear analysis and thinking. Coming from a transputer background, I've been advocating point-to-point communications and bit-serial buses for a while, because they have all of the advantages you mentioned. They didn't happen earlier because they're a big mental switch for people, comparable with other paradigm shifts, like:*

⟨ global state machines versus object-oriented and multitasking programming.
⟨ shared versus distributed memory (most people still haven't got this one).
⟨ gate-level design (bottom-up) versus system-level design (top-down).

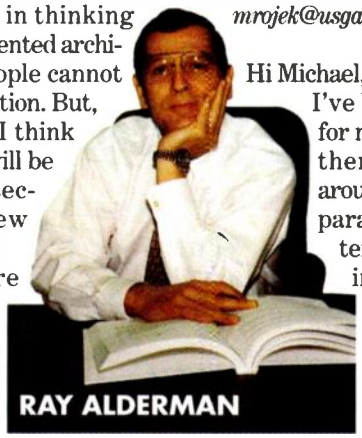
In this context, and as a member of the 1355 Association, I would also like to draw your attention to IEEE 1355. This interconnect standard has most of the features already built in. The designers are now trying to reinvent Gigabit networking so it will work with the built-in features. Based on variable-packet switching and an end-to-end protocol (supported in the hardware), it's been designed using standard CMOS, and is very reliable.

For example, look at the R-Cube switch that provides an eight-by-eight crossbar for 1 Gbit/s links. It consumes only 3 W, and each link goes up to 5 m with no external buffering. The chip is designed in 66 MHz and 0.5 µm. For more information go to: www.1355-association.org.
Best regards,
Eric Verhulst

Hi Eric,

I've worked with Colin Whitby-Strevens for some time on 1355 specs, including a specification he completed under VITA for the 1355 pinout on VME cards. VITA is an ANSI-accredited standards developer for computer architectures.

Much of the understanding I have on serial architectures has come from the 1355, the transputer architectures (specifically DS-Links), and networking (teaching me what NOT to do). You are absolutely correct—serial architectures are a big switch in thinking from traditional, bus-oriented architectures, and many people cannot make that mental transition. But, as my editorial noted, I think the market mentality will be driven to serial architectures in the next few years. It must happen.


RAY ALDERMAN

If the telecoms are sending us data in serial form, why do we parallelize those very efficient streams, and put the packets on a slow, synchronous parallel bus—bottlenecking the system? It's not smart engineering, from my way of thinking.
Best regards,
Ray Alderman

Ray,

Bravo on your article in ELECTRONIC DESIGN *about the "Death of PCI." I have been singing the "Serial Song" to my engineering colleagues for more than 20 years, and I am constantly amazed that I always seem to get a similar response from them. They all eventually agree with me, that we ultimately live in a serial world, and that a fast serial processing architecture would be simple and inexpensive.*

Almost all of them fall into the same rut that they have been in for decades. They say that no matter how fast the processor, they can get more processing power by envisioning 16, 32, or 64 of these elegantly simple systems all running together in parallel, using shared memory resources and a single connector etc.

It sounds just like the exact parallel mess that we have now! I say that we should all beware of engineers who can take simple devices and design a sloppy system with them. Let's hope that the newer engineers coming into the workforce can be convinced of the inherent superiority of serial architectures before their ways of thinking get set in concrete.
Best regards,
Michael Rojek
Assistant Electronics Coordinator
The U.S. Golf Association
mrojek@usga.org

Hi Michael,

I've been a serial advocate for many years myself, and there are not many of us around. Most engineers get parallel buses, drivers, interrupts, and wait-states in their blood early on, and they never seem to appreciate what serial machines can do.

With the progress in semiconductor geometries, clock speeds, and transistor density, we can now run serial connections at very-high (Gigabit) rates, with very-low latency and power consumption. When you consider that all the data streams coming through the telecom and cable interconnects are serial, it makes you stop and think. Why do we parallelize the data, and put it on a slow, synchronous, register-oriented, bit-thrashing bus?

I am chairing a new ANSI standards committee on dataflow architectures. You can follow the progress by coming to the VITA web site (*www.vita.com*), and checking out the VITA Standards Organization (VSO) section. We will be laying the foundation for networked backplanes, multiplexed data paths, and some point-to-point connected architectures. When we have the electrical layers, packet protocols, and the API completed, I hope to move the fabric to optical connections by 2000. Already, there are prototype optical machines that embed the fiber into the glass epoxy laminate of a backplane. We hope to achieve gigabit- and terabit speeds in the next few years.
Best regards,
Ray Alderman

To the Editor:

I am amused by the recent obituary for PCI announced by Ray Alderman in the June 8 edition of ELECTRONIC DESIGN. *It is especially ironic that Mr. Alderman is the executive director of VITA (VMEbus International Trade Association). Isn't VME dead? After all, VME's obituary has been proclaimed many times since PCI entered*

the scene.

Although "The Death Of PCI" may make a good headline, it, and the article, are flawed and misleading. To begin, Mr. Alderman stated that "It's time we dropped the variation-on-a-theme synchronous-bus model and adopted ...serial dataflow machines." He argues that serial buses are inherently superior to parallel buses. If we follow this argument to it's logical conclusion, then why not have every component in a system or on a motherboard talking serially? No need for that big Pentium II single-edge contact cartridge (SECC) socket anymore when we have something like high-speed serial I/O (HSSIO) to replace it.

By the same token, the advanced graphics port (AGP) could also be replaced with a serial bus. Why not interface to cache memory serially instead of using a "slow" parallel synchronous bus. In fact, why even have parallel buses inside chips if serial buses are superior? No, serial buses are not going to take over every application because parallel buses are faster when all other parameters (i.e.: driver speed and transmission line limitations) are equal.

Mr. Alderman has confused the serial/parallel issue with the software driver support issue. He associated the "bit-banging" register programming model solely with parallel buses. Obviously he's not aware of I_2O, a standard that allows PCI-based I/O subsystems to use a host driver that is independent of a particular I/O vendor's hardware implementation. Mr. Alderman believes that this type of flexibility is only possible with serial buses.

In reality, there will continue to be a place for parallel buses like PCI. Synchronous parallel buses have many advantages such as lower latency, higher speed for a given driver, and lower overhead. The emergence of new standards like CompactPCI will serve to make PCI even more successful. Although Mr. Alderman has over-stated the reach of serial buses, they will become more prolific mainly due to the consumerizing of the PC. There are applications where a serial bus makes sense, and other applications where a synchronous parallel bus is more appropriate. A more balanced analysis of the serial vs. parallel issue would conclude that the new serial bus standards will create new market opportunities without cannibalizing the growing market for PCI. The two are complementary.

Regards,
Mike Alford
VP Engineering
V3 Semiconductor

Hi Mike,

While you believe that parallel buses and register-oriented interrupt-driven architectures will rule the world, my opinion differs from yours. There will be applications where the centralized-I/O parallel-bus model of computing will continue. But, PCI exists today only at the whim of Intel. As the paradigm-shift to serial occurs, it will be the mainstream architecture, and PCI will become the ISA bus of the 90's.

The PC market is slowing, every major semiconductor manufacturer is downsizing. Japan's economy is declining while Europe's is teeter-tottering. The next great "killer-app" is the entertainment PC and digital TV in the consumer markets. PCI buses are too slow, too expensive, and the time and complexity required for the software is unacceptable. Next-generation PCs and TVs for this market must be priced under $500. You can't do that with PCI, parallel buses, and the present software paradigm. The year 2000 is the date that major marketshare holders plan to change paradigms for the 21st century. No company seems more motivated to change the computing paradigm than Intel.

While parallel buses will be used in the future, they will be in very small domains, like on-chip buses running only a few millimeters, and some MCM local buses. Past that, you run into so many physics problems that parallel buses are more trouble than they're worth.

Consider that the data streams coming to the office building or home are high-speed serial connections. What we do now is parallelize these highly-efficient streams, and put them on a slow, synchronous parallel bus. This clogs up the computing architecture. After all, that's why Intel moved the graphics system off the PCI bus— PCI performance was dismal.

Also consider that USB and 1394 are the bellweathers of the new computing model. But, USB is too slow, and 1394 has been festooned with protocol to the point where it looks like a TCP/IP network, with all the associated complexities and latencies. There's just too much financial, performance, and political pressure building up in the markets for mainstream computing to maintain the old architectural model. That's why Intel and others have embarked on their "Legacy-free PC" activities announced at the WINHEC conference earlier this spring. I'm speculating that the foundation for this new architecture is a serial connection, not a parallel bus. Based on what I know, I think I am right.

Our differences do not revolve around whether PCI will be a viable new-design technology, but only in how long it will be viable, and for which applications. As growth markets, ISA lasted about 12 years, EISA only eight years, and VESA about six. PCI was introduced in 1993/1994. The past would then say that PCI only has about two-to-three years left on the growth curve in the traditional PC market. Embedded design-ins may last longer, but they won't be long-term.

What I was really saying in my column is that, in the near future, hardware will drive software like it never has before. Serial architectures will enhance the shift to object-oriented programming models and away from the old register-and-driver models of the '90's.

If everything is really becoming connected, then the communications architectures will start to drive the computing architectures toward serial interconnects. Once that happens, the software architectures will follow suit. There's simply too much pressure in the marketplace supporting this paradigm-shift. The Japanese and European consumer product industries, and the U.S. PC industry, will usher in the shift to serial technologies.

It's already happening in Europe with the tremendous adoption of fieldbuses in industrial controls applications. We're on the path to distributed I/O systems and away from centralized I/O models like PCI. All we need are cheap Gigabit bandwidths, and Intel's announcement seems to indicate that we will have it by 1999.

Best regards
Ray Alderman

Ray Alderman is the executive director at VITA. He can be reached at exec@vita.com.

WHAT'S ON BOARD

Two USB circuits from Alcor Micro Inc., Sunnyvale, Calif., are single-chip solutions for keyboards or standalone hubs. The AU9412 has all the keyboard hub functionality, while the AU9216 implements a six-port hub. The former allows designers to add two USB ports to the keyboard, and includes a default keyboard matrix controller that handles an 18-by-8 key matrix. An optional 512-byte external serial EEPROM can be connected for OEMs to customize the encoding—vendor ID (VID), product ID (PID), and keyboard scan table can be stored in EEPROM. Also on the chip, which supports two bus-powered downstream ports, is a 3.3-V voltage regulator. The AU9216, supports six bus- or self-powered downstream ports. Besides power control and over-current sensing, each port supports an individual LED for port-device-communication error detection. A 256-byte external serial EEPROM can be attached, for system configuration customization(VID and PID codes). The keyboard and hub chips sell for under $2.00 and $2.60 apiece, respectively, in OEM lots. Less-expensive ROM versions are also available. Packages include DIPs, Shrink DIPs, and QFPs. Contact Dennis Chang at Alcor; (408) 541-9700, or on the web at www.alcormicro.com.

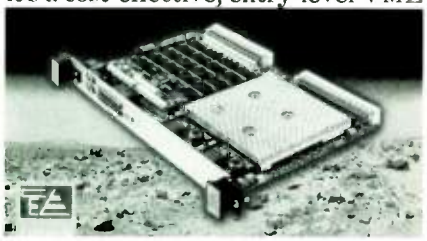
With almost a three-fold improvement in graphics performance, the Ticket to Ride IV graphics processor from Number Nine Visual Technology Corp., Lexington, Mass., combines a 128-bit graphics engine with fully-integrated 3D and 2D graphics acceleration and MPEG video support. Features include an intelligent resource processor (IRP), a programmable latency memory controller (PLMC), and a 250-MHz RAMDAC. Included as part of the PLMC is a 10-level-of-detail MIP-mapping capability with tri-linear filtering to produce high-quality images. Internally, the chip employs the company's proprietary 128-bit WideBus technology, and can channel graphics data through the IRP to multiple 128-bit-wide data paths into two separate, yet integrated and tightly-coupled 128-bit graphics engines. The 430-MFLOPS 3D pipeline includes a rendering setup engine to process 3D pixels at up to 32-bit color for precise rendering. On the chip is an 8-kbyte texture cache and full-scene antialiasing for high-quality images. The embedded graphics accelerator uses either SGRAM or SDRAM to deliver resolutions up to 1920 by 1200 pixels. The chip also packs a 2× AGP bus interface that allows graphics instructions and data to be transferred at up to 533 Mbytes/s. Once loaded into local memory of up to 32 Mbytes, data can be processed at up to 2 Gbytes/s. Supporting the controller is the HawkEye IV software, which simplifies the setup and control of monitors, colors, and screen resolutions without the need for system reboot. In OEM lots, the graphics processor sells for $65. Samples are immediately available. Contact the company at (781) 674-0009, or on the web at www.nine.com.

The latest member of the programmable system device family from WSI Inc., Fremont, Calif., has up to 3000 complex programmable logic gates, 160 kbytes of flash memory, 2 kbytes of scratchpad SRAM, several configurable I/O ports, and a programmable microcontroller interface. The PSD8xxF2 provides system support for microcontrollers and DSP chips. The 160 kbytes of flash is divided into two banks: 128 kbytes for program storage and 32 kbytes subdivided into four 8-kbyte sectors to store boot algorithms, programming algorithms, and data that must be retained when power is removed. The system can execute code from either array, allowing each section to be programmed concurrently with system operation. An in-system-programmable decode-PLD can be set to automatically handle the complex program and data addressing for MCUs like the 8031, letting the flash program space be written in data space during the erase/write operation. That allows chips like the 8031 to write to their program space, something not permitted in the standalone configuration. An on-chip JTAG serial interface provides designers with a high-speed serial in-system programming capability. In lots of 25,000 units, the PSD8xxF2-15J sells for $6.76 apiece and will be available in the fourth quarter. Contact David Raun at (510) 656-5400, or on the web at www.wsiusa.com.

Single-Slot UltraSPARC IIi VME Engine Is Cost-Effective

High-performance, Unix-based applications rely on the processing muscle of the Sparc platform to get the job done. To feed this hunger, Themis Computer has announced shipment of the USP IIi-IV, the industry's first true single backplane slot UltraSPARC VME engine.

In its base, single-slot configuration it's a cost-effective, entry-level VME



UltraSPARC platform. For more demanding applications, the USPIIi-IV allows system integrators to select two- and three-slot versions. These provide high-performance 3D graphics with Sun's Creator Graphics card, expanded I/O for high-availability applications, and three PMC slots.

The USPIIi-IV features the 300/333 MHz, 64-bit UltraSPARC-IIi processor with local PCI bus (PMC) peripheral controller expansion and VME64bus architecture. Support for SunSoft's Solaris 2.6 operating system speeds application development and deployment.

Memory on the USPIIi-IV is expandable using memory modules, from 64 to 512 Mbytes in the single-slot configuration, and up to 1 Gbyte in the two and three-slot versions.

The USPIIi-IV sports a a complete set of workstation I/O features. The USPIIi-IV features two ultra fast/wide SCSI ports, dual MII or 10/100Base-T Ethernet ports (second Ethernet port available only in two- and three-slot configurations), up to three PMC expansion slots (in the triple-slot configuration), dual RS-232 serial ports, and an IEEE 1284 parallel port.

Available now, list price for the USPIIi-IV, begins under $9500 in a base configuration with 300-MHz UltraSPARC-IIi, 128 Mbytes of DRAM, and 256 Mbytes of second-level cache.

Themis Computer Corp., *3185 Laurelview Court, Fremont, CA 94538; (510) 252-0870; fax (510) 490-5529; www.themis.com.* **CIRCLE 532**

LINEAR TECHNOLOGY

DESIGN NOTES

A New Low Power, High Output Current Dual CFA Makes xDSL Line Driving Clean and Easy – Design Note 187

Adolfo A. Garcia

Introduction

Driving the balanced lines of high speed modems has become a very popular application for high speed, high output current, dual operational amplifiers. High amplifier speed is required to faithfully process signal passbands of at least 1MHz bandwidth, and high output currents are required to meet peak drive levels into 100Ω or 135Ω termination. Taking into account peak-to-average signal ratios in these applications, Table 1 summarizes peak voltage/current drive levels required by current xDSL systems. The peak voltage and current drive values shown are for ADSL systems with 100Ω termination and HDSL/HDSL2 systems with 135Ω termination.

Table 1. Peak Drive Levels for Popular xDSL Systems

xDSL	Nominal Transmit Power	Peak Voltage	Peak Current
HDSL	13.5dBm	$5.6V_{P-P}$	$42mA_{P-P}$
ADSL DMT Upstream	13dBm	$15V_{P-P}$	$150mA_{P-P}$
ADSL CAP Upstream	13dBm	$8.5V_{P-P}$	$86mA_{P-P}$
ADSL CAP Downstream	20dBm	$18.9V_{P-P}$	$190mA_{P-P}$
HDSL2	16.5dBm	$19.6V_{P-P}$	$146mA_{P-P}$

There are amplifier products available today that can address at least one, but not all, of the xDSL applications listed in Table 1. These products are single application specific and suffer from one or more of the following shortcomings: limited supply voltage operation, excessive zero-load power dissipation, large packaging/heat sinking and/or limited dynamic performance (thermal and intermodulation crosstalk).

The LT®1497, a 50MHz, 125mA dual CFA from Linear Technology, is the fourth product in our family of high speed, high current dual current feedback amplifiers, capable of addressing any one or all five of the xDSL applications in Table 1. It operates from ±2.5V to ±15V supplies, consumes less than 7mA per amplifier and is available in both SO-8 and thermally enhanced S16 packages. With its 125mA output stage and available voltage swing to within 2V of either rail, the LT1497 is a good, economical choice because it allows the use of smaller turns-ratio (1:1 and 1:2) transformers to deliver power into the line. These transformers are less expensive than the high turns-ratio transformers required by some amplifiers that operate on a single supply voltage rail. In addition, its low quiescent supply current allows more

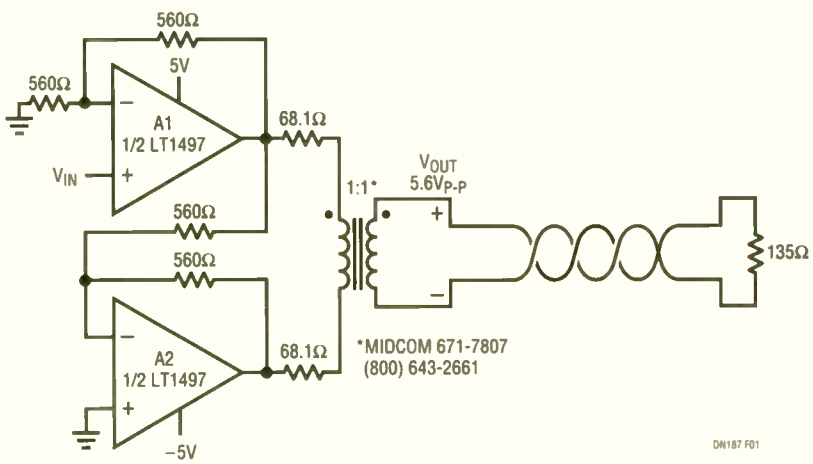


Figure 1. A Low Distortion, LT1497-Based Differential Transmitter Circuit for xDSL Applications

modem lines per card because less PC board area is required for the device and heat sinking. Its low input offset voltage match (±3.5mV) and low TCV_{OS} (10µV/°C)— not specified for other amplifiers—combine to eliminate output coupling capacitors used to block DC current flow through the transformer's primary windings.

A Low Distortion HDSL Line Driver

Figure 1 shows an HDSL differential line driver circuit that transmits signals over a 135Ω twisted pair through a 1:1 transformer. The driver amplifiers are configured for gains of two (A1) and minus one (A2) to compensate for the attenuation inherent in the back termination of the line and to provide differential drive to the transformer.

Even though the input circuit configuration is single ended, the circuit configuration can be very easily manipulated to accommodate differential output analog front ends (AFEs) and/or single supply rail operation for the line driver circuit. For HDSL applications, the LT1497's high output current and voltage swing drive the 135Ω line at the required distortion level of –72dBc. For an HDSL data rate of 1.544Mbps, the fundamental frequency of operation is 392kHz.

Performance

The circuit of Figure 1 was evaluated for harmonic distortion with a 400kHz sine wave and an output level of $5.6V_{P-P}$ into 135Ω, representing peak drive operation into the HDSL termination. Figure 2 shows that the second harmonic is –72.3dB relative to the fundamental for the 135Ω load. Third harmonic distortion is not critical, because received signals are heavily filtered before being digitized by an A/D converter.

With multicarrier applications, such as discrete multitone modulation (DMT), becoming as prevalent as single-carrier applications, another important measure of amplifier dynamic performance is 2-tone intermodulation distortion. This evaluation is a valuable tool for evaluating amplifier linearity when processing more than one tone at a time. For this test, two sine waves at 300kHz and 400kHz were used, with levels set to obtain $5.6V_{P-P}$ across the 135Ω load. Figure 3 shows that the third-order intermodulation products are well below –72dB.

Conclusion

The new LT1497 offers outstanding distortion performance in an SO-8 package with remarkably low power dissipation and very attractive high speed modem system economics. It is ideally suited for single-pair digital subscriber line systems, specifically DMT remote terminal, CAP central office/remote terminal, HDSL or HDSL2 line-driver applications.

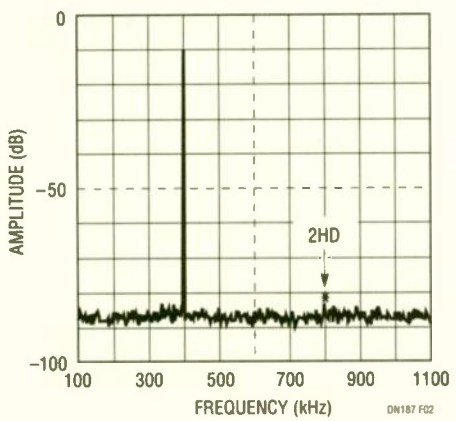


Figure 2. Harmonic Distortion Performance of Figure 1's Circuit with a 400kHz Sine Wave at $5.6V_{P-P}$ into 135Ω

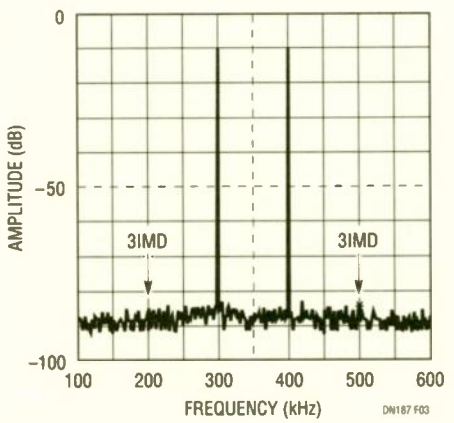


Figure 3. 2-Tone Intermodulation Distortion Performance of Figure 1's Circuit. Two Sine Waves at 300kHz and 400kHz Are Used to Obtain $5.6V_{P-P}$ into 135Ω

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Motherboard Supports 100-MHz System Bus

Once core logic chip sets began to roll with 100-MHz system bus support, true workstation-class PCs became feasible. Motherboards supporting the bus are already starting to emerge. Among them is a motherboard from Tyan Computer for Pentium II with 100-MHz system bus support.

Called the Tsunami AT(SI 830S/SL), the board sports the 440BX AGPset for Pentium II CPUs to 400 MHz and beyond, or Celeron CPUs. It features Intel's 440BX chip set with 100-MHz "Front Side" bus support.

The Tsunami provides room for AGP/PCI expansion with 4 PCI slots, 4 ISA slots, and 1 AGP slot. Memory is expandable to 1024 Mbytes with four banks of 168-pin SDRAM DIMMs. AMI's Plug-n-Play BIOS, designed specifically for the Pentium II CPU, is standard. Other features include Ultra-DMA/33 and Super I/O support; and optional system-management features such as LM79/LM75 control chips with on-board alarm to monitor heat, fan, and voltage. The board is priced below $150 in OEM quantities.

Tyan Computer Corp., *3288 Laurelview Court, Fremont, CA, 94539; (510) 651-8868; fax (510) 651-7688; www.tyan.com.* **CIRCLE 525**

Flash Disk Drives Employ Double-Density Technology

By incorporating its new 80-Mbit double-density technology, SanDisk Corp. is able to reduce flash prices 20% per Mbyte. This boosts the capacity in a number of the company's products, including Type II and Type III PC flash cards; CompactFlash cards; 1.8-, 2.5- and 3.5-in. flash drives; and flash chip sets. The double-density technology essentially doubles the capacity of flash storage products. This is done by storing two bits of information in each flash cell instead of the traditional one bit.

SanDisk's Type II PC cards increase from 220 to 280 Mbytes, while its Type III PC memory cards more than double in capacity from 220 to 500 Mbytes. The top capacity of the company's CompactFlash cards rises from 48 to 60 Mbytes. The 1.8-in. embedded flash drives, formerly exhibiting a top capacity of 140 Mbytes, now have a capacity of 240 Mbytes. The new 2.5-in. and 3.5-in. flash drives debut with a top capacity of 500 Mbytes. All SanDisk double-density products operate at either 3.3 or 5 V.

This is the company's second generation of flash products based on double-density technology. In moving from first to second generation, SanDisk doubled the write speed to 100 kbytes/s and the read speed to 1.8 Mbytes/s. SanDisk's standard, or non-double-density products differ from its double-density devices in that they have higher write performance but lower capacity. The company expects to sample the products in July and with full production in the third quarter of this year.

Pricing, in high-volume OEM quantities for the high-capacity products, is: 280-Mbyte Type II, $1095; 500-Mbyte Type III, $1995; 60-Mbyte CompactFlash, $199; 2400-Mbyte 1.8-in. flash drive, $995; 500-Mbyte 2.5-in. flash drive, $1995; 500-Mbyte 3.5-in. flash drive, $1995; and the 20-Mbyte flash chip set, $59.

SanDisk Corp., *140 Caspian Court, Sunnyvale, CA 94039; (408) 542-0500; fax (408) 542-0503; Internet: www.sandisk.com.* **CIRCLE 526**

IndustryPack Carrier Board Meets VME64x Requirements

IndustryPack modules enjoy the most widespread use among all mezzanines. SBS GreenSpring Modular I/O now offers a way to marry these mezzanines with the high-performance VME64-extension bus standard. The VIPC664-ET Quad IndustryPack carrier board meets I/O requirements for any VME64 Extension-based system deployed in military, telecommunications, and industrial automation applications.

The VIPC664-ET includes four IndustryPack sites and supports either four single-wide modules or two double-wide IP modules. It's compatible with over 125 IndustryPack modules for various I/O functions, such as analog, digital, serial, motion control, telecommunications, and Fieldbus.

Three interrupt modes are provided in the VIPC664-ET to provide a flexible programming architecture— seven interrupt modes, single level interrupt mode, and interrupt disable mode. Two megabytes of on-board nonvolatile flash memory is provided for general-purpose storage. Interrupt capabilities are available for interrupt-driven flash programming and erasure.

The power-check circuit and status registers verify power to the IndustryPack slots with both a visual LED indicator and software-accessible status bit and interrupt. EMI gaskets and ejector-injector handles are provided for the front panel to meet VME64x and IEEE 1101.11 requirements, and to reduce EMI emissions.

Priced at $1090, the VIPC664-ET Quad carrier board is available immediately. Two types of transition modules also are available now. The XM-664-80 and the XM-644-60 provide rear backplane I/O access and are priced at $295 each. The XM-664-80 supports IEEE 1101.11 form-factor enclosures, and the XM-644-60 provides support for alternative non-IEEE 1101.11 enclosures.

SBS GreenSpring Modular I/O, *181 Constitution Dr., Menlo Park, CA 94025; (650) 327-1200; fax (650) 327-3808; www.sbs-greenspring.com.* **CIRCLE 527**

Magneto-Optical Drive Stores 5.2 Gbytes Of Data

Magneto-optical (MO) disk technology continues to hold the price/performance edge over competing storage media. Verbatim now has announced its new 5.2-Gbyte MO drive and 5.2-Gbyte media. The 5200 drive meets the performance and capacity requirements for audio, video, and multimedia production and post-production applications.

The 5200 stores up to 5.2 Gbytes (equivalent to 21 four-drawer filing cabinets) of documents, data, and images on one removable 5.25-in. disk. When Verbatim's new media is used, the storage cost is only 3 cents per megabyte. Because the media in the drive can be easily replaced when additional storage is needed, users have virtually unlimited storage capacity.

The new 5.2-Gbyte drive incorporates proven technology to achieve sustained data-transfer rates of up to 10 Mbytes/s and burst-transfer rates of 20 Mbytes/s at a full 2942 RPM. With an average latency of 10.2 ms and an average seek time of 20 ms, the drive also provides fast access to volumes of information. A 4-Mbyte buffer further enhances the drive's performance. These features, and the drive's uninterrupted data streaming capabilities, also make

(continued on page 82)

(continued from page 81)
the 5200 the ideal solution for demanding video and audio production and post-production work because pauses, motion flicker, and sound distortion are eliminated.

Provided with a three-year limited warranty, the Verbatim 5200 costs under $2000. The price for Verbatim's lifetime-warranty 5.2-Gbyte MO media is $150. Both the drive and the media are available immediately.

Verbatim Corp., *1200 W.T. Harris Blvd., Charlotte, NC 28262; (704) 547-6500; fax (704) 547-6609; Internet: www.verbatimcorp.com.* **CIRCLE 528**

Compact PCI Box Offers 14 Slots, Telephony Bus, Hot Swap

System designers crafting telecom and telephony projects can't afford to waste time doing basic platform hardware. The ZT 5081, a 6U 14-slot development system, lets OEM project designers start with the basic feature set to develop their CompactPCI applications.

This CompactPCI development system brings a rack-mount system with a computer telephony bus and hot-swap capability to the company's family of preconfigured development systems. Featured is a single-board computer containing a Pentium processor with MMX technology, an IDE hard drive, a floppy drive, a SCSI interface, and two 150-W hot-swap power supplies.

The ZT 5081 feature set is housed in a 19-in., rack-mount IEEE 1101.1-compliant CompactPCI chassis with a 14-slot backplane, suitable for both general-purpose and telecommunications applications. In addition to accommodating 32- or 64-bit CompactPCI cards, the backplane supports the H.110 Computer Telephony Bus for voice and other telephony applications, as well as IEEE1101.1-style rear transition cards for simplified cabling.

The backplane also supports peripheral and I/O cards adhering to the Hot Swap Specification of the PCI Industrial Computer Manufacturers Group (PICMG). The new rack-mount system comes with MS-DOS, Ziatech's industrial BIOS and flash disk. The internal hard-disk drive is ready for the installation of PC-compatible operating systems, such as Windows NT, QNX, or VxWorks.

Ziatech offers development toolkits with additional files to help simplify the implementation of these OSs. The ZT 5081 costs $5595 in single quantities.

Ziatech Corp., *1050 Southwood Dr., San Luis Obispo, CA 93401; (805) 541-0488; fax (805) 541-5088.* **CIRCLE 529**

Pentium SBC Has Long Lifespan In Embedded Applications

OEMs who develop products for medical electronics, imaging, computer telephony, and industrial automation are hot on the idea of embedded PCs. But PC-compatible products' typical product life cycles are about 9 to 12 months. To help with this problem,vendors like Micro Industries are offering boards with support cycles of 5 to 7 years, up to a seven-fold increase.

Boards falling into this category include the 586PCI/64P3C, a highly integrated PICMG CPU card that offers a PC-compatible environment on a single plug-in card. A full-size PICMG passive backplane board, the card is based on the Pentium processor.

At the heart of the board is an Intel MMX Pentium processor with Intel HX chip set. The board supports Pentiums configured for 100, 133, 166, 200, or 233 MHz speeds. The option is available to upgrade with the Socket 7 technology. A Symbios SCSI/Ethernet controller, provides Ultra-wide SCSI support and 10/100 Mbits/s Ethernet. A Chips & Technologies 65554 graphics accelerator on board which enables the support of both CRT and flat panel display applications.

Tying the board together is a PCI/ISA bus interface with dual bus architectures. A SanDisk Flash IDE onboard enables support for embedded applications that require boot capabilities without the need for a hard drive.

The new products are available immediately in the United States and Europe.Volume OEM pricing for 586PCI/64P3C is $670 and for 586PCI/64P4C is $550.

Micro Industries Corp., *8399 Green Meadows Dr., North Westerville, OH 43081; (800) 446-6762; fax (740) 548-6184; www.microindustries.com.*
CIRCLE 530

RISC And CISC Processors Compete For Embedded Applications

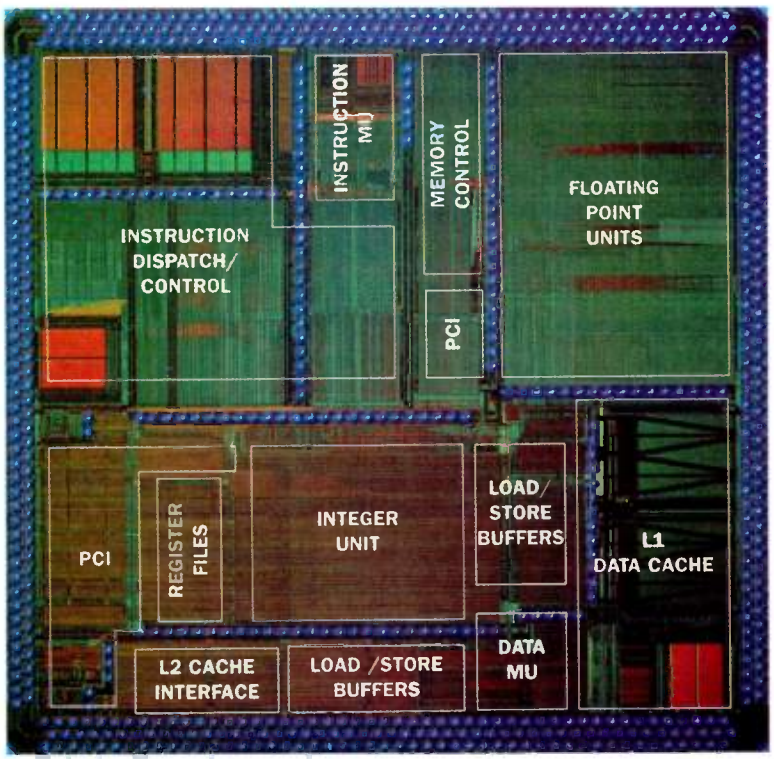
With Effective Throughputs Of 200 MIPS And More, Superscalar CPUs Tackle Throughput-Intensive Embedded Needs.

Dave Bursky

SPECIAL REPORT

No matter how fast a CPU is, new applications always seem to surface—and demand even more horsepower. Driven by image processing, communications, multimedia, and many other applications, CPU throughputs have climbed from the few million instructions per second (MIPS) of last decade's CPUs to over 2000 MIPS delivered by today's leading-edge chips. Such high-throughput CPUs are not being demanded just for desktop computing applications to power advanced workstations and servers. They are also wanted for many embedded applications, such as in high-speed printers, for network bridges and routers, and computer games.

Advanced CMOS processes are being called upon to achieve speed improvements. But, this is only part of the landscape. Other performance gains come from many architectural enhancements. In part, these gains are possible because of improved processing, which permits millions of transistors to be integrated on a single chip. Some enhancements include the use of superscalar architectures with multiple-integer and floating-point execution units, out-of-order instruction execution, and high levels of pipelining. In addition, designers have increased CPU word widths from 16 to 32 to 64 bits, and expanded the cache interface to bus widths as large as 128 bits.



Art Courtesy: Sun Microelectronics

New, more complex instructions have been added to many superscalar processors in order to leverage the wide data paths and new features. For example, a subdividable arithmetic unit can take 64-bit data words and divide them into two, four, or eight subwords. It can then perform up to eight parallel computations on the data words. Such instructions are critical to improving the CPU performance for applications such as digital-signal processing, image processing, and many other applications that deal with large arrays of data.

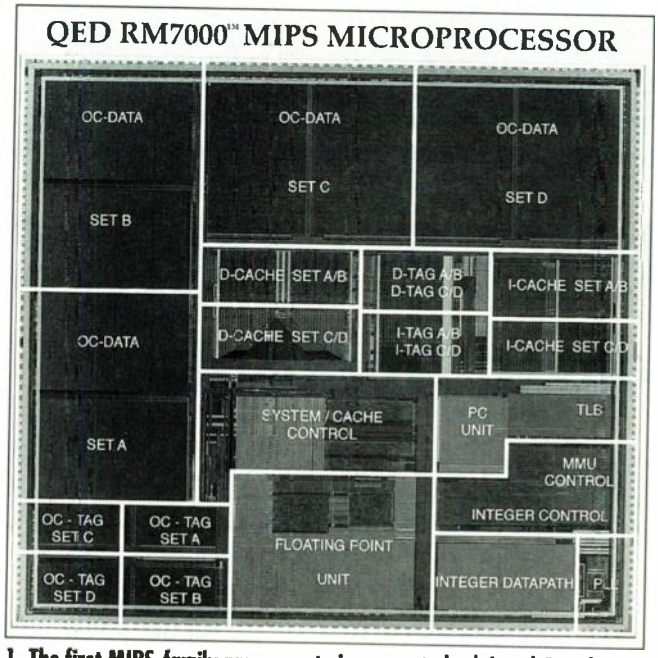
One common characteristic of all these superscalar RISC processors is high-throughput floating-point computation. Single- or two-cycle FP multiplication or multiply accumulate operations give users several hundreds of MFLOPS to almost 1 GFLOPS of math throughput—performance previously relegated to supercomputers or to dedicated signal-processing circuits. These and even more MFLOPS can be readily consumed by signal processing, ray tracing in 3D imaging, and many other applications.

The first company to implement such a feature in their PA-RISC processors was Hewlett-Packard Co., Palo Alto, Calif. However, they have not developed a commercial OEM market for these proces-

sors, and only use the CPUs in their own systems. Other RISC-processor families—Alpha, MIPS, SPARC, and PowerPC, as well as the suppliers of x86 high-end CPUs—have each, in turn, crafted their own instruction-set extensions to add visual computing capabilities. These instructions can speed up applications such as image processing, printing, and audio-signal processing. The performance improvement ranges from three or four times, up to peak improvements of eight to 12 times the chips' throughput (without the new instructions).

The superscalar, highly pipelined CPUs typically run at clock speeds of 200 MHz and faster. At the high end of the embedded controller market, they deliver supercomputer-like integer and floating-point computational performance—peak instruction throughputs of more than 2 billion instructions per second (BIPS) are already possible from a single CPU. In many cases, these CPUs were initially developed for desktop computers and servers. Not only do they perform well in single-CPU systems, but most include the necessary control signals and buses to be seamlessly connected in large multiprocessor arrays. They are now finding their way into performance-demanding applications, like raster engines in high-end laser printers, 3D graphic displays, bridges and routers, and many other systems.

To achieve the high throughput, designers of these CPUs spend all of their transistor budget on throughput-enhancing features—large caches, dynamic execution control, register renaming logic, advanced branch prediction, and, of course, multiple execution units. Interfacing these powerful CPUs to the rest of the system requires one or more support logic chips, which provide the control and I/O functions. Luckily, advances in ASIC technology have made it relatively easy to craft the desired support circuits, which typically run at bus frequencies of 66 to 120 MHz. In contrast, many "high-integration" embedded controllers use their transistor budgets to pack much of the system-support logic on the same chip, allowing designers to incorporate only a more moderate-performance CPU.

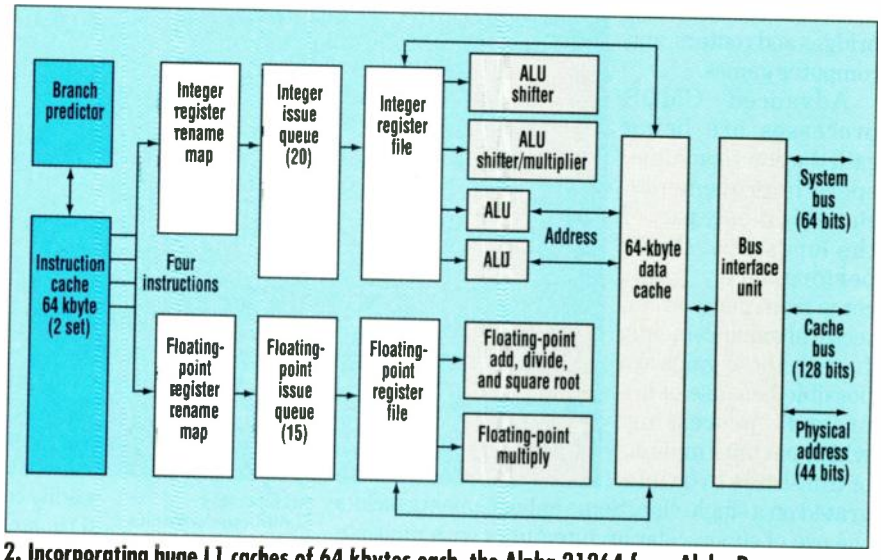


1. The first MIPS-family processor to incorporate both Level-1 and Level-2 caches on the chip, the RM7000 from Quantum Effect Design employs a superscalar architecture that initiates two instructions every clock cycle. It thereby achieves a peak throughput of over 500 Dhrystone 2.1 MIPS when docked at 300 MHz.

Larger instruction and data caches, from just a few kbytes at the beginning of this decade to as much as 64 kbytes each, as well as second-level caches on the chip, are improving memory bandwidth. These caches tie into 64- or 128-bit-wide buses on the chip, and those wide buses permit more data or multiple instructions to be transferred every cycle. That translates into higher instruction throughputs.

One of the major steps forward in CPU design has probably been the move to superscalar and superpipelined architectures. Superscalar architectures with multiple execution units can execute two or more instructions simultaneously—almost doubling or quadrupling the instruction throughput. Superpipelining adds more pipeline stages, which permits multiple instructions to be staged in the execution queue. A new instruction in each pipeline can then start every clock cycle.

For example, the RM7000 64-bit, dual-issue, superscalar processor from Quantum Effect Design packs dual 16-kbyte, Level-1 (L1) caches for instructions and data. It also includes a 256-kbyte unified, write-back Level-2 (L2) cache *(Fig. 1)*. An on-chip tertiary cache controller supports up to an 8-Mbyte Level-3 (L3) off-chip cache. With its L2 cache and dual instruction-issue pipeline, the chip achieves a raw throughput of 500



2. Incorporating huge L1 caches of 64 kbytes each, the Alpha 21264 from Alpha Processor can perform four-way out-of-order execution on the instruction stream. The pipeline consists of four integer execution units, two of which can perform memory address calculations, as well as two floating -point execution units.

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	PIC16C6XX PIC16C7XX PIC16F8X PIC16C9XX	512 x 14 1K x 14 2K x 14 4K x 14 8K x 14	80–368	28, 40, 44 64, 68	13–52	25	68HC05 68HC08 80C51 ST6, ST7 COP8
	PIC17C4X PIC17C7XX	2K x 16 4K x 16 8K x 16 16K x 16	232–902	40, 44 64, 68 80, 84	33–66	10	H8, 68HC11 68HC16, ST9 MCS251 80C51XA

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And, many architectural enhancements used by RISC processors have been applied to streamline instruction execution. The latest-generation chips also include multimedia and signal processing instruction-set extensions for 3D graphics and audio applications, putting them on par with many RISC processors. These products are available from Advanced Micro Devices, Cyrix/National Semiconductor/IBM, Centaur/IDT, and, of course, Intel.

Running at clock speeds of 266 to 400 MHz, the Pentium II, Xeon, and other x86 CISC CPUs (K6, 6x86, and WinChip) deliver throughputs competitive with, or even better than, many of the RISC solutions. Even the older 486, when clocked at 133 MHz (486/DX5 from AMD) will deliver performance comparable to MIPS-compatible RISC processors, such as the NEC4300i or the IDT 4640, running at 133 MHz *(Fig. 4)*.

From a software developer's viewpoint, leveraging the x86 instruction set can be beneficial. It has a wide selection of low-cost development software. And, an abundance of programmers are familiar with the processor programming model. Software development costs can thus be kept low, while applications can be developed very quickly. However, there are potential limitations with the CISC approach when it comes to handling performance-critical, real-time applications. CISC processors use variable-length instructions. This may make dealing with real-time events and handling interrupts a little harder than with the simple single-cycle execution model used by most RISC processors. That's due to the potentially slower interrupt-response time, which is caused by the delay imposed while waiting for the current multicycle instruction to complete before switching contexts.

In addition to the off-the-shelf x86 processors that come from the desktop world, AMD and several other companies have developed highly integrated low-power versions of the x86. They contain many of the system I/O and support functions, yet consume just a few hundred milliwatts. When clocked at up to 100 MHz, chips like the Elan SC400 and 410 from AMD provide computational throughputs comparable to moderate-performance RISC processors.

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Single (Isolated)	3-60 (105 Models)	3.3, 5, 5.2, 12, 15	0.2 - 18	4.5 - 9 4.7 - 7.5 9 - 18 9 - 36 18 - 36 18 - 72 36 - 75	1.25 x 0.8 1 x 1 2 x 1 2 x 2 2.4 x 2.3 2 x 3	$31
Dual (Isolated)	3-50 (65 Models)	±5, ±12, ±15	±0.1 - ±4			$31
Triple (Isolated)	8-40 (35 Models)	+5 and ±12 +5 and ±15	0.8 - 5 ① ±0.1 - ±1			$50

① For triple-output models, listed output currents are primary/auxiliary.

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Circle 520

INT 1Ch And PAL Controls Process Variables

J. JAYAPANDIAN
Materials Science Division, IGCAR, Kalpakkam,
PIN 603102, Tamil Nadu, India; jjp@igcar.ernet.in.

The design presented here provides a simple method for controlling process variables such as temperature, pressure, flow, etc., via user-selectable control functions (e.g., proportional, integral, and differential). The PAL chip 16L8 is programmed to work as a 4-bit subtractor. Two such PAL 16L8s, shown in the figure, accept two 8-bit data bytes representing the set-point value (B) and the measured process variable value (A). They provide an 8-bit error signal through the subtraction process. By selecting the PAL ICs through chip select $\overline{CS1}$, the PC reads this "Error Value." The error output is merely the deviation between the set and measuring parameters.

If the measured parameter is high in comparison with the set parameter, the PAL error output will be negative; otherwise it will be positive. The MSB of the error output indicates the sign bit. The logic high and logic low in the sign bit indicate that the error is negative and positive, respectively.

The "Special BIOS" interrupt, (INT 1Ch), available in all PCs, is used in this design to read the error value through the PAL port, as well as write the appropriate control responses to the DAC port by selecting the DAC through $\overline{CS2}$. The INT 1Ch interrupt is a hardware interrupt *(see "Special BIOS Interrupt for Real-time Data Acquisition and Control,"* ELECTRONIC DESIGN, *May 1, 1997, p. 173)*. It automatically occurs 18.2 times per second and is invoked by the BIOS timer interrupt after it updates the time-of-day count.

At startup, the vector for the interrupt points to an I_{RET} (interrupt return) instruction—when the interrupt is called, it simply returns. Changing this interrupt vector to point to a procedure in your program will cause the procedure to be called 18.2 times per second.

Variables in typical process control environments are very slow compared to the INT 1Ch interrupt rate. For every INT 1Ch, the ISR program in this application must read the PAL port and write the appropriate control function digital response in the DAC port. The data output to the control port may be for proportional, integral, differential, or on/off control functions, depending upon the procedure in the user program for INT 1Ch. Remember that once the vector is changed, the procedure will immediately begin to be invoked every 18th of a second.

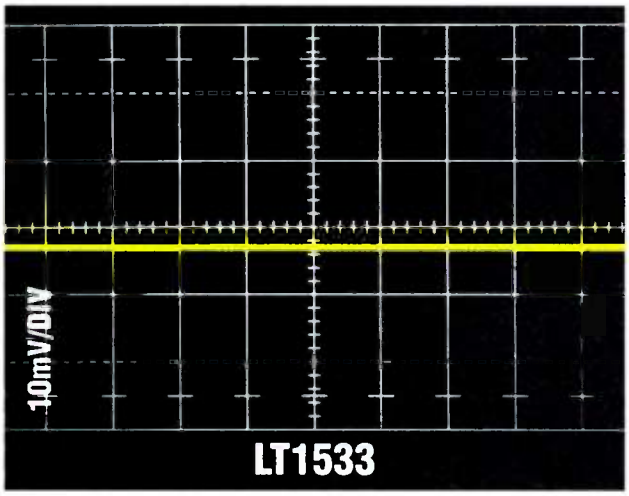
Care should be taken to save changed registers and to minimize code execution time in this interrupt handler. Depending upon the error value, the DAC output and hence the op-amp output that drives the load through the buffer will be updated at each INT 1Ch interrupt.

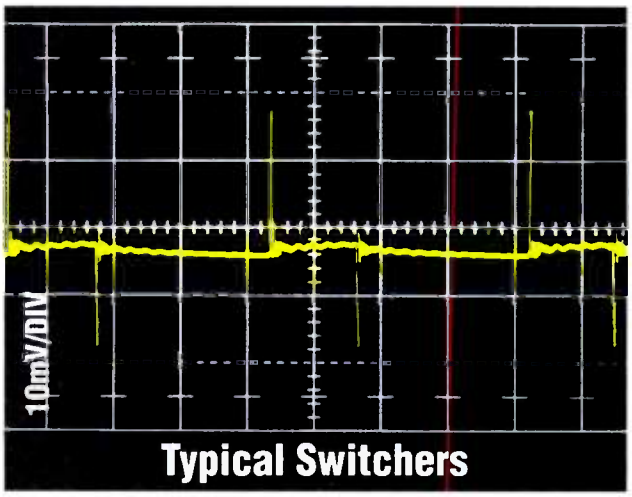
```
PAL16L8 Page 1
A3      HHHHLLLLLH      LHHHLLLLLH      HHHHHHHHHH      HHHHHHHHHH
A2      HHHLLLLLLH      LHHLHLLLHH      HHHHHHHHHH      HHHHHHHHHL
A1      HHLLLLLLLH      LHLHHLLHHH      HHHHHHHHHH      HHHHHHHHLL
A0      HLLLLLLLLH      LLHHHLHHHH      HHHHHHHHHH      HHHHHHHLLL
B3      HHHHHHHHLL      HLLLLLLLLL      LLLHHHHLHH      HHLHHHHHHH
B2      HHHHHHHLLL      HLLLHLLLLL      LLHHHHLLHH      HLLLHHHHHH
B1      HHHHHHLLLL      HLLHHLLLLL      LHHHHLLLHH      LLLLLHHHHH
B0      HHHHHLLLLL      HLHHHLLLLL      HHHHLLLLHL      LLLLLLHHHH
CIN     LLLLLLLLLL      LLLLLLLLLL      LLLLLLLLLL      LLLLLLLLLL
GND     LLLLLLLLLL      LLLLLLLLLL      LLLLLLLLLL      LLLLLLLLLL
Y0      LHHHHLLLLH      HLLLLLHHHH      LLLLHHHHLH      HHHHHHLHHH
BR0     LHHHHLLLLL      HLLLLLLLLL      LLLLLLLLLL      LLLLLLLHHH
Y1      LLHHHHHHHH      HHHLLHHHHH      HLLLLHHHLL      HHHHHLLLHH
BR1     LHHHHLLLLL      HLLLLLLLLL      LLLLLLLLLL      LLLLLLLHHH
Y2      LLLHHHHHHH      HHHHLHHHHH      HHLLLLHHLL      LHHHLLLLLH
BR2     LHHHHHLLLL      HLLLLLLLLL      LLLLLLLLLL      LLLLLLLHHH
Y3      LLLLHHHHHH      HHHHHHHHHH      HHHLLLLHLL      LLHLLLLLLL
BR3     LHHHHHHLLL      HLLLLLLLLL      LLLLLLLLLL      LLLLLLLHHH
VCC     HHHHHHHHHH      HHHHHHHHHH      HHHHHHHHHH      HHHHHHHHHH

PAL16L8 Page 2
A3      LHHHHLLLLL      LLLLLLLLLL      HLLLLLLLHH      HHHHHHHHHL
A2      LLHHHLLLLL      LLLLLLLLLL      HLLLHHHHLL      LLHHHHHHLL
A1      LLLHHLLLLL      LLLLLLLLLL      HLHHLLHHLL      HHLLHHHLLL
A0      LLLLHHHHHH      HHHHHHHHHH      HHLHLHLHLH      LHLHLHLLLL
B3      HHHHHHLLLL      LLLHHHHHHH      LLLLLLLLLL      LLLLLHHHHH
B2      HHHHHHLLLH      HHHLLLLHHH      LLLLLLLLLL      LLLLLHHHHH
B1      HHHHHHLHHL      LHHLLHHLLH      LLLLLLLLLL      LLLLLHHHHH
B0      HHHHHHLHLH      HLHLHLHLHL      HHHHHHHHHH      HHHHHHHHHH
CIN     LLLLLLLLLL      LLLLLLLLLL      LLLLLLLLLL      LLLLLHHHHH
GND     LLLLLLLLLL      LLLLLLLLLL      LLLLLLLLLL      LLLLLLLLLL
Y0      HHHHLLLHLH      LHLHLHLHLH      LLHLHLHLHL      HLHLHLHHHH
BR0     HHHHLLLLLL      LLLLLLLLLL      LLHLHLHLHL      HLHLHHHHHH
Y1      HHHLLHHHHH      HHHHHHHHHH      HHLHLHLHLH      LHLHLLLHHH
BR1     HHHHLHLHHL      LHHLLHHLLH      LLLLHLLLHL      LLHLLHHHHH
Y2      HHLLLHHLLH      HHHHHLLHHH      HHHHLHHHLH      HHLHHLLLHH
BR2     HHHHLHLHHH      HHHLLHHHHH      LLLLLLLLHL      LLLLLHHHHH
Y3      HLLLLHHLLL      LLLHHHHHHH      HHHHHHHHLH      HHHHHLLLLH
BR3     HHHHLHLHHH      HHHHHHHHHH      LLLLLLLLLL      LLLLLHHHHH
VCC     HHHHHHHHHH      HHHHHHHHHH      HHHHHHHHHH      HHHHHHHHHH

PAL16L8 Page 3
A3      LLLLHLHHHL      LLLLHHHHH
A2      LLLLHLHHLH      LLLHHHHHH
A1      LLLLHLHLHH      LLHHHHHHH
A0      LLLLHLLHHH      LHHHHHHHH
B3      HHHLLHLLLL      LLLLLLLLH
B2      HHLLLHLLLH      LLLLLLLHH
B1      HLLLLHLLHH      LLLLLLHHH
BO      LLLLLHLHHH      LLLLLHHHH
CIN     HHHHHHHHHH      HHHHHHHHH
GND     LLLLLLLLLL      LLLLLLLLL
Y0      HHHHLHHLLL      HLLLLLLLL
BR0     HHHHLHHHHH      HLLLLHHHH
Y1      HLLLHHLLLL      LHHHHLLLL
DR1     HHHHLHLHHH      HLLLLLHHH
Y2      HHLLHHHLLL      LHHHHHLLL
DR2     HHHHLHLLHH      HLLLLLLHH
Y3      HHHLHHHHLL      LHHHHHHLL
BR3     HHHHLHLLLH      HLLLLLLLH
VCC     HHHHHHHHHH      HHHHHHHHH
```

100µV Output Noise Switching Regulator





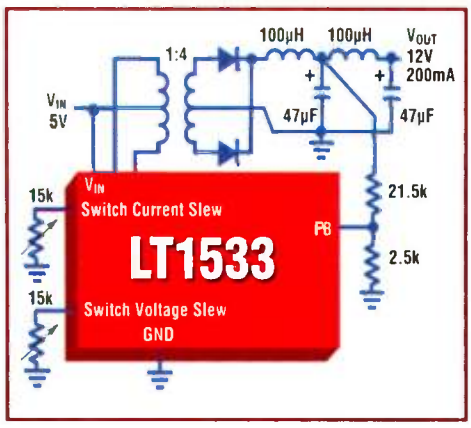
The Good. The Bad & The Ugly.

LT1533: The First Switching Regulator with Lower Noise than a Linear Regulator.

The LT1533 DC/DC converter produces less than 100µV peak-to-peak output noise over a 100MHz bandwidth. The internal power switches allow user-adjustable voltage and current slew rates, resulting in dramatically reduced conducted and radiated EMI. Finally, a switching regulator that can coexist with noise sensitive applications such as precision instrumentation and wireless communications.

Features

- Low Switching Harmonic Content: Up to 40dB Lower than Typical Switchers
- Independent Control of Voltage Slew Rates and Current Slew Rates
- 20kHz to 250kHz Oscillator Frequency
- Synchronizable to External Clock
- Regulates Positive and Negative Output Voltages
- Wide Input Voltage Range: 2.7V to 23V
- $4.95 Each for 1000-Piece Quantities



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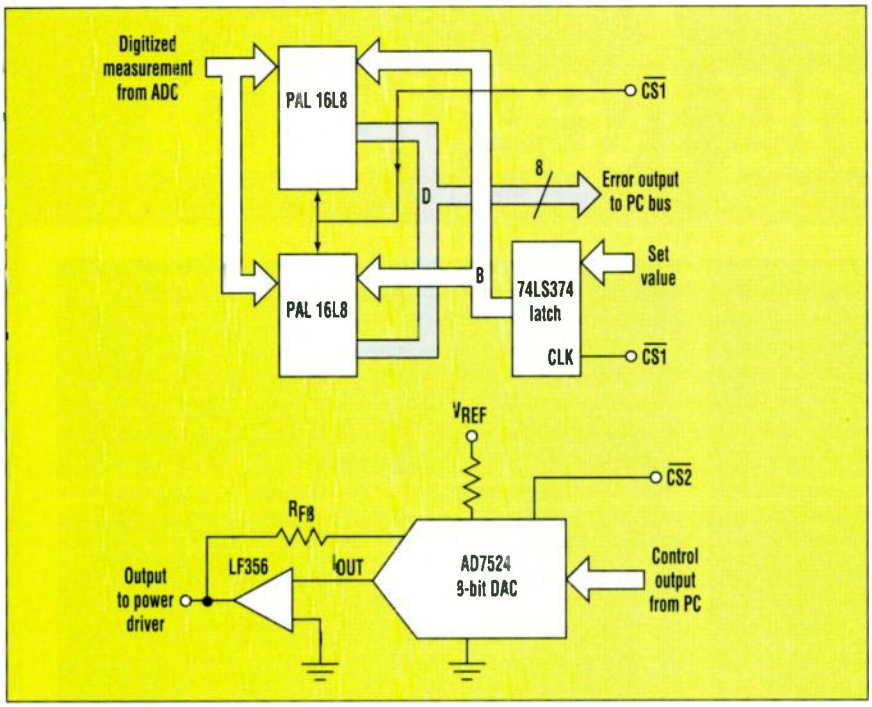


This process-control interface allows real-time control via a PC employing user-selectable control functions. These functions can be used for proportional, integral, differential or on/off control.

Circle 521

Build A "Hot-Swap" Interface Circuit

LEE SLEDJESKI
Fairchild Semiconductor, Logic Division, 333 Western Ave., M/S 10-26, South Portland, ME 04106; (207) 775-8376; fax (207) 761-6137; e-mail: Lee.Sledjeski@fairchildsemi.com.

In applications that require whole-board power cycling or actual board "hot-swapping," maintaining a high-impedance interface at power-off as well as the power-up and power-down cycles becomes a critical design problem. Ideally, system designers can create a high-impedance, low-capacitance interface to minimize any possible disruptions of system data resulting from inserting or removing a board.

At the heart of the circuit shown, which meets all of these design criteria, is the Fairchild Switch FST6800. It provides 10 bits of high-speed CMOS TTL-compatible bus switching. The low on-resistance (4 Ω) of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground-bounce noise.

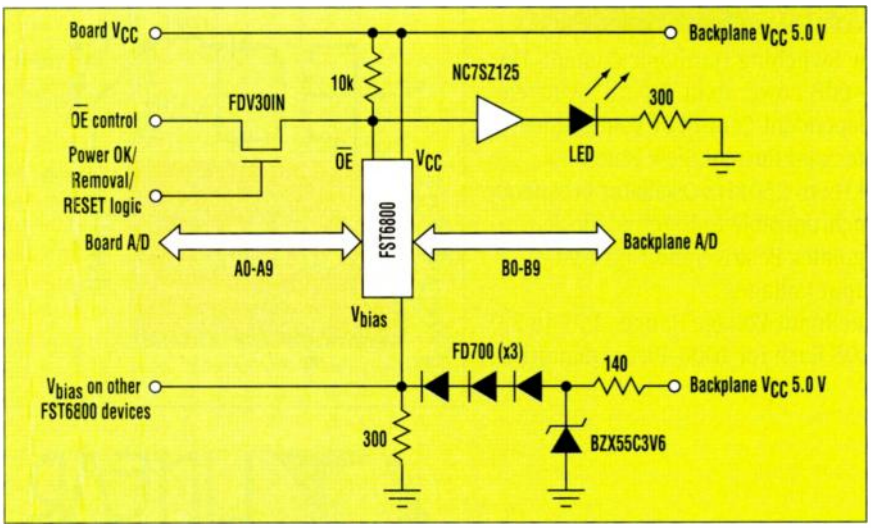
The FST6800 precharges the B-Port to a selectable bias voltage (V_{BIAS}) to minimize live-insertion noise. The FST6800 is organized as a 10-bit flow-through switch with an active low $\overline{OE}$ control pin. The $\overline{OE}$ control pin, when driven to the active low state, connects the A and B Ports together.

The bias voltage is set via a 3.6-V Zener diode stack and resistors. This circuit draws about 10 mA of current and has sufficient capacity to power several FST6800 V_{BIAS} networks. In cases where the backplane V_{CC} and board V_{CC} are separated and the FST6800 must be connected to the board or local V_{CC} supply, the diode stack on the V_{BIAS} pin will prevent sourcing the local V_{CC} supply to the backplane V_{CC}.

The $\overline{OE}$ voltage is set by either a pull-up resistor or on-board control logic. A simple pass gate shifts control between the two selections. Pass-gate control can include provisions for board-maintenance functions, low V_{CC}, and board-level RESET.

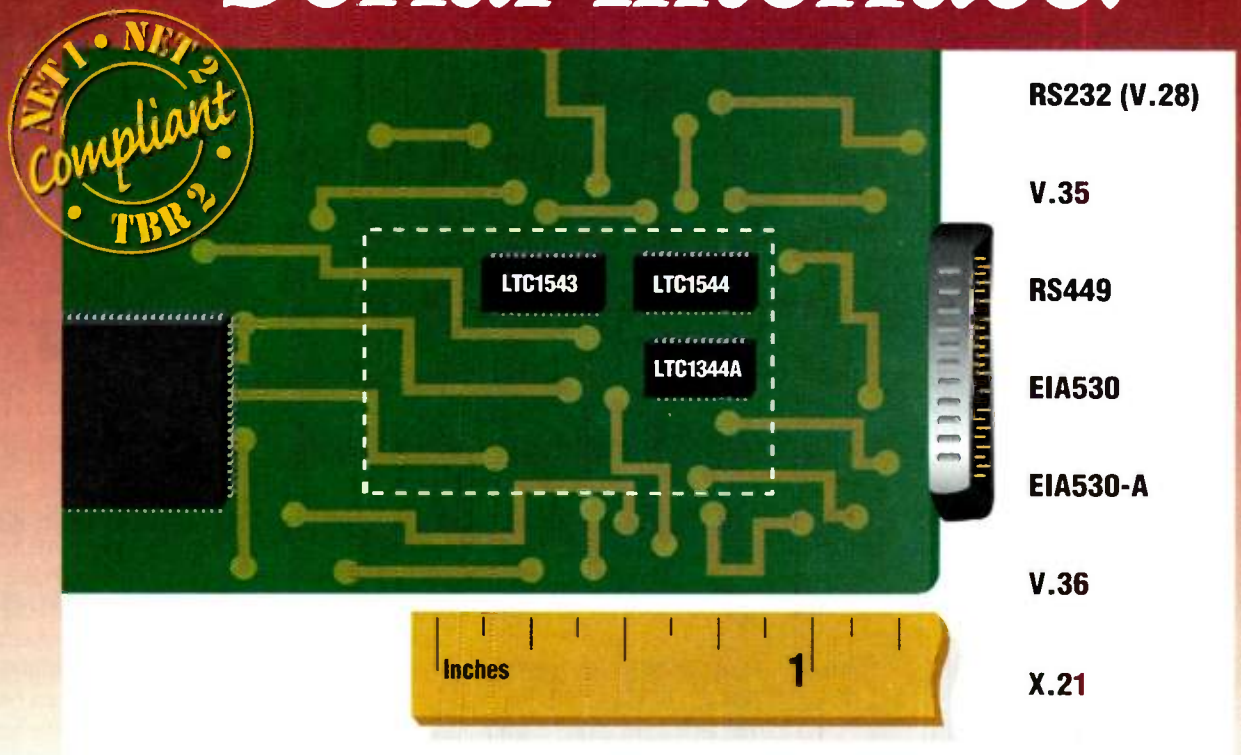
When the $\overline{OE}$ voltage is pulled up to a valid V_{IH}, the NC7SZ125 single-gate-buffer will drive an "OK to Remove" LED on the board.

In applications where the board V_{CC} and the backplane V_{CC} aren't hardwired together, the FST6800 should be connected to the backplane V_{CC}. This ensures that the backplane V_{CC} and the board V_{CC} won't be coupled together through the FST6800's internal V_{BIAS} circuits.



This high-impedance, low-capacitance interface minimizes possible data disruptions that result from "hot-swapping" pc boards and power-up/power-down cycling.

Multiprotocol Serial Interface!



LTC Multiprotocol: Interface any Router or Modem for Remote Access with a Single Connector.

The LTC1543, LTC1544 and LTC1344A include all of the transceivers for clock, data and control signals as well as switchable termination for the popular WAN serial protocols. And it's been certified for NET1, NET2 and the more stringent TBR2. No external resistors, no jumpers or relays and no time-consuming debugging for compliance testing—just drop it in and go!

Features

- LTC1543 - Triple Transceiver for Data and Clock
- LTC1544 - Quad Transceiver for Control Signals
- LTC1344A - Switchable Terminator
- Certified NET1, NET2 Compliant
- TBR2 Compliant
- Operates from a Single 5V Supply
- Configurable as DTE or DCE Port
- 28-lead /24-lead SSOP Packages
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Protocols Supported

- ☑ RS232 (V.28)
- ☑ V.35
- ☑ RS449
- ☑ EIA530
- ☑ EIA530-A
- ☑ V.36
- ☑ X.21

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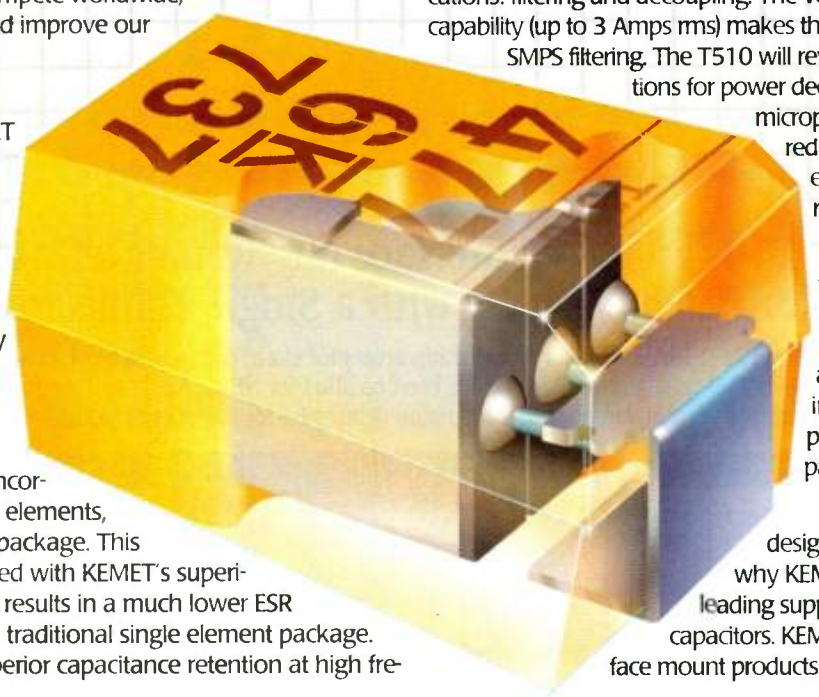
At KEMET, manufacturing a good capacitor has never been just "good enough". To compete worldwide, we continually develop and improve our capacitors.

In today's electronic requirements, we at KEMET are aware of the fact that space is at a premium. Space that requires more and more capacitors installed within smaller and smaller footprints while maintaining high CV and low ESR.

The innovative construction platform of the new KEMET T510 series incorporates multiple capacitor elements, in parallel, inside a single package. This unique assembly, combined with KEMET's superior processing technology, results in a much lower ESR than can be achieved in a traditional single element package. Other benefits include superior capacitance retention at high frequencies and reduced ESL.



The T510 series provides ultra low ESR for two specific applications: filtering and decoupling. The very high ripple current capability (up to 3 Amps rms) makes this part the ideal choice for SMPS filtering. The T510 will revolutionize design solutions for power decoupling of leading edge microprocessors by substantially reducing the part count necessary to achieve the total required cap and ESR.

The T510 series is initially available in a 470µF 6V device. A 680µF 4V part and a 330µF 10V are targeted for release in early '98. All T510 products are tape and reel packaged per EIA 481-1.

The T510's unique design clearly demonstrates why KEMET remains the industry's leading supplier of solid tantalum capacitors. KEMET offers leaded and surface mount products in both dielectric families.

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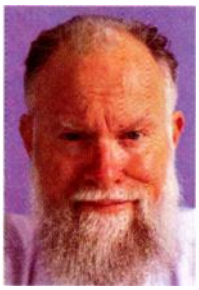
For instant relief, take one KEMET T510 series capacitor and just say "ahhhh!"

BOB PEASE

Bob's Mailbox



Hi Bob:

I read your column on soakage, and I can add only one thing to the phenomenon of capacitive discharge. Having been involved in electronics as a hobby since I was ten, and having worked repairing test instruments a few years later, I have often found myself in the path of a capacitive discharge. We actually had a policy at Philips that if you got a jolt, you had an EKG. It turns out that electric shocks can cause cardiac arythmia, even if you feel O.K.

MIKE McGINN
via e-mail

I presented your valuable idea to our health dept. Thanks, Mike.—RAP

Dear Bob:

In your column of Nov. 17, 1997, Chris Anderson bewailed the lack of instruction in component characteristics in EE programs. I agree wholeheartedly, and therefore, we teach about the differences between aluminum 'lytics, tantalums, and polyester caps, plus carbon-comp vs. metal-film resistors, aircore vs. ferrite-core vs. iron-core coils, etc. in our Electronics Engineering Technology program. Of, course, our graduates are technicians, not engineers—although some of their employers *call* them engineers, and put them to work designing motor-control devices and the like. But *we* don't claim they're EEs.

A local man had two sons. He sent the elder to a well-respected, state-supported university to major in EE. The younger son came to our school. When the elder was a junior, he visited his brother at our school, where he was shown some of the lab projects (design, build, calibrate, and test an analog multimeter; design and build a frequency counter, etc.) that kid brother had built. His response, "You have LABS? We haven't had a practical lab, yet!" Upon graduation, the two went to work for the family business of selling and maintaining woodworking equipment. The father decided that the younger had a more-valuable education for hardware and software maintenance of the machinery and the proprietary computer network than the elder.

The moral of this story is that as long as our educational system values credentials above practical experience, and rewards research grant acquisition rather than program quality, we will continue to graduate engineers who don't know a carbon-film resistor from a 100-µH coil. (Hey, they're both tan cylinders with stripes, aren't they?)

But, how do you get good students into good programs? Parents and counselors steer the best students toward a four-year degree—any degree—rather than an EET or CET two-year degree (which can serve as stepping-stones for a higher degree, by the way). I've bought shirts from guys with an MA in History. The fellow who buys used books here on campus has an MA in Psychology. And manufacturers are *crying* for technicians, starting at salaries from $25,000 to $35,000. When we finally realize that a BSEE with 15 years experience experience is at least the equivalent of a PhD who never worked in industry, and that the status of a degree in Oceanography or Political Science won't pay the grocer, maybe we'll stop exporting our lunch to other countries.

RICHARD HONEYCUTT
Electronics Instructor
Davidson Community College
Lexington, N.C.

We expect engineering schools to teach theory and analysis—both are important. But should we expect innovation from the brilliant theorist or the bright technician? In the real world, one, the other, both, or neither may be a good inventor.—RAP

All for now. / Comments invited!
RAP / Robert A. Pease / Engineer
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New Tester Optimized For 100-MHz-Plus SDRAM

The CMT3100 is a new high-speed memory-module test system optimized for testing 100-MHz-plus SDRAM. The system has the accuracy required for PC100 compliance testing and offers the capability of supporting additional memory architectures with upgrades. The base configuration is a single site system with 160 high-speed digital I/O pins, ten fully programmable device power supplies, and 20 dc power measurement units (PMUs). A fully configured version of the machine has four completely independent test sites, providing a total of 640 pins with one PMU per eight pins. When fully optimized, the CMT3100 can test four high-performance memory modules in parallel. JD

***Crimble Micro Test Inc.**, 2127 Ringwood Ave., San Jose, CA 95131; (408) 526-9150; fax (408) 571-0427; www.cmt.com.* **CIRCLE 553**

Adapter Enables "Hands-Free" Probing Of Fine-Pitch ICs

The HP Wedge probe adapter is designed to facilitate reliable, non-destructive, "hands-free" connections of probes to thin quad flatpack (TQFP) and plastic quad flatpack (PQFP) ICs. On one end of the adapter are compressible dual conductors. These fit in the space between adjacent IC pins and hold the adapter in place, with each conductor making physical contact with one side of an IC pin. This redundant physical connection created by the two contact points increases the reliability of the electrical connection, with little chance of shorting adjacent pins or damaging the device under test, according to the company. The compressible conductors connect to pins on the opposite side of the adapter, which are used to attach to scope or logic-analyzer probes. HP Wedge probe adapters are available in 3- and 8-signal versions for 0.5-mm and 0.65-mm IC pin spacing. Prices range from $39 to $79, depending on the size of the probe and the number of probes in the package. JD

***Hewlett-Packard Co., Test and Measurement Org.**, 5301 Stevens Creek Blvd., MS 54LAK, Santa Clara, CA 95052; (800) 452-4844, ext. 5935; www.tmo.hp.com* **CIRCLE 554**

BIST Tool Uniformly Tests System-On-A-Chip Designs

BISTMaxx is a built-in self-test (BIST) tool that provides a uniform approach for testing analog, mixed-signal, and digital circuits. BISTMaxx is based on the company's patented oscillation BIST technology. The first in a family of tools, it enables intellectual-property (IP) providers to incorporate test methodologies into their cores for system-on-a-chip (SOC) designs. BISTMaxx provides a uniform design environment compatible with digital scan techniques, such as IEEE 1149.1. According to the company, since BISTMaxx is digitally invoked with low area overhead, it's a relatively non-intrusive solution that performs structural and functional at-speed tests. The quality of the testing makes BISTMaxx suitable for wafer-probe, prototype, and production testing. BISTMaxx is available immediately, with technology licensing starting from $25,000. JD

***Opmaxx Inc.**, 8209 S.W. Cirrus Dr., Beaverton, OR 97008; (503) 520-9200; fax 503-520-1636; Internet: www.opmaxx.com.* **CIRCLE 555**

New Software Detects Jitter On PLLs In Next-Generation ICs

The latest version of Wavecrest's Virtual Instruments (VI) software is designed to make it easier and faster to detect jitter problems on phase-locked-loop (PLL) circuits in next-generation computer chips. Virtual Instrument software provides a graphical interface to the company's Digital Time System (DTS) hardware in a Windows 3.1, 95, NT, or X Windows format. The software includes an integrated suite of tools for data acquisition and rapid graphical analysis of measurements taken with the DTS hardware. The new PLL version of Virtual Instruments adds auto correction. Auto correction extends the usable frequency range and reduces the instrument jitter noise floor to a very low level so that analysis of high-frequency clocks and data-communications interfaces is possible. The VI/PLL software runs on various platforms, and is available now at $6295. JD

***Wavecrest Corp.**, 7275 Bush Lake Rd., Edina, MN 55439; (612) 831-0030; fax (612) 831-4474; Internet: www.wavecrestcorp. com* **CIRCLE 556**

Software Provides Remote Access For Control Applications

NetTrender is a client/server software component that provides remote access to any portion of a data-acquisition and control application via the World Wide Web and company intranets. Based on push technology, NetTrender allows software vendors and in-house programmers to add real-time remote process monitoring to their existing data acquisition and process control applications. The product accomplishes this by "pushing" real-time data from remote locations back to the "server," thus allowing any authorized user to monitor the process, regardless of where they are on the company network or Internet. A single browser page can show data from several different locations and provide historical trends of real-time data. NetTrender also includes ActiveX controls, which allows the software to run inside any ActiveX container application, such as custom VisualBasic programs. Pricing for the component is $495, and delivery is two weeks ARO. JD

***LabTech Corp.**, 2 Dundee Pk., Suite B09, Andover, MA 01810; (978) 470-0099; fax (978) 470-3338; e-mail: info@labtech.com; www.labtech.com.* **CIRCLE 557**

PCMCIA Data-Acquisition Card Provides 12-Bit Resolution

The DAQP-12H is a 12-bit, high-gain data acquisition adapter in the PCMCIA form factor. It has eight differential and 16 single-ended analog input channels, sampling rates to 100 kHz, and eight digital I/O channels. Programmable gains of 1, 10, 100, and 1000 allow the DAQP-12H to be configured for ±10 V, ±1 V, ±100 mV, and ±10 mV input ranges. The card is equipped with a 2 kbyte data FIFO. A scan FIFO size of 2048 entries supports full-speed, random-order channel scanning and gain selection. Included with the adapter are a universal software driver and the latest version of DaqEZ, a windows-based data acquisition application software package. Price of the DAQP-12H is $655. JD

***Quatech Inc.**, 662 Wolf Ledges Pkwy., Akron, OH 44311; (330) 434-3154; fax (330) 434-1409; Internet: www.quatech.com.* **CIRCLE 558**

COMMUNICATIONS

Versatile 10/100/1000 Switch Chips Build Low-Cost LANs

The GT48300 is a cascadable four-port 10-Gbit-class crossbar switch controller that forms the core of a family of Ethernet switch ICs. The switch controller combines a 10 Gbit/s, non-

blocking, butterfly crossbar switch and four high-speed data link ports. These ports employ a proprietary 16-bit "G.Link" interface that has a capacity of 1.2 Gbits/s in each direction. The G.Link interface supports hot swapping and can function like a backplane using inexpensive copper cables for distances of up to 10 meters.

The GT48300 also has a 66-MHz, 32-bit PCI 2.1 bus interface This permits up to eight controllers to be cascaded, for a total of 32 gigabit connections.

Network connections to the crossbar switch can be made through either the GT-48320 (a one-port Gigabit Ethernet switch and MAC controller), or the GT-48310 (an eight port Fast Ethernet switch). Both devices exchange traffic with the crossbar via a 2.4-Gbit/s G.Link interface. The GT-48310 also can be used as a standalone 10/100 switch, or connected via its G.Link interface with up to eight other devices to form larger switch arrays.

They support the full complement of standard management protocols, including port-based VLANs,, extended RMON, and priority queuing. In addition, they support advanced management features including IP multicast filtering, 802.IQ VLAN tags, 802.1p-based priority packet tagging, and support of Layer 3 switching via protocol filtering. Other advanced features include self-learning of up to 12,000 unicast and unlimited multicast/broadcast addresses, and automatic packet aging.

For extremely cost-sensitive applications, less sophisticated versions of the eight-port switch are available. The GT-48311 has standard management capabilities, and the GT-483112 is an unmanaged eight-port 10/100 switch.

Sampling now, the GT-48300 crossbar, GT-48310/1/2 10/100 switch devices are scheduled for production later this year. The GT-48320 Giagbit Ethernet switch controller will sample in the third quarter of this year. LG

***Galileo Technology**, 142 Charcot Ave., San Jose, CA 95131-1101; (408) 367-1400; fax (408) 367-1401; www.galileot.com.* **CIRCLE 559**

2.2-GHz Modulator/Synthesizer For Dual-Band Cellular Phones

The TRF3040 is a fully integrated modulator/synthesizer that will make the design of dual-band wireless applications easier and less expensive. Able to operate in both the 900-MHz cellular band and the 1.9-GHz PCS spectrum, the device supports both traditional analog (AMPS) transmission plus the IS-136 digital standard. The biCMOS RF chip integrates a 2.2-GHz fractional-N main synthesizer that has been optimized for fast frequency lock time, thus improving handoff performance. The synthesizer's internal fractional compensation minimizes output spurious content and phase noise. This enhances overall performance and lets designers employ less expensive filtering schemes in their designs.

A second 200-MHz auxiliary integer synthesizer and prescaler also comes on-chip to support a wide range of IF plans. The TRF3040 features a highly linear variable gain amplifier and output driver that provides up to 11 dBm of power with low distortion to minimize spectral regrowth. Operating power consumption at 3.75 V is 150 mA and 2 mA in standby mode. An evaluation board and reference design are available to speed the development of dual-band wireless products.

Housed in a 48-pin TQFP, the TRF3040 will be sampling in evaluation kits during August, and be in full production in the third quarter of this year. Pricing is $6.07 each in quantities of 10,000. LG

***Texas Instruments Inc.**, Semiconductor Group, SC-98054A, P.O. Box 172228, Denver, CO 80217; (800) 477-8924, ext. 4500; www.ti.com/sc/docs/wireless.home.htm.* **CIRCLE 560**

EDA

Verilog Simulator Supports IEEE-1364 Standard

A new simulator developed by SynaptiCAD, called the VeriLogger Pro, combines its own WaveFormer Pro interactive debugging waveform viewing environment, with the Wellspring Solution's VeriWell IEEE-1364 compliant Verilog simulator. In addition, the tool includes a host of debugging and editing features. This Verilog simulator fully supports the IEEE-1364 standard, including all of the RTL, behavioral, and synthesizable constructs.

The VeriLogger Pro waveform viewing environment contains advanced timing-diagram editing features for editing and documenting the waveforms. All traditional viewer features are included as well, such as zooming, scrolling, radix change, and grouping. The VeriLogger Pro simulator also incorporates a hierarchical browser that displays the structural relationships of the modules in a design. An internal editor provides color-syntax highlighting and point-and-click breakpoints.

The VeriLogger Pro simulator will begin shipping in August 1998. On a Windows NT/95 platform it will sell for $1500 on Windows NT/95. On Sun/Solaris/HP platforms, it's priced at $3000. A free evaluation disk is available. CA

SynaptiCAD Inc., *520 Prices Fork Rd #C4, Blacksburg, VA 24060; (800)-804-7073; (540)953-3390; Internet: www.syncad.com.* **CIRCLE 561**

EDA Tool Manages Simulation Projects and Models

One of the more time-consuming tasks facing any designer today is storing and managing projects, data files, and models. A recently introduced tool for board-level simulation—Simulation Desktop—manages simulation projects of any size and complexity, and simulation models across an engineering organization. The designer simply integrates schematics, model sources, and simulators through a graphical user interface. The tool automatically generates structural Verilog netlists and test fixtures based on user preferences. As the designer makes changes to the design, output files are automatically recompiled and synchronized to allow both consistent output and incremental simulation.

Based on a robust relational database, the tool not only offers enterprise-wide library management and model administration, but extensive reporting capabilities as well—all in a manner transparent to the designer. As such, it ensures a more unified and accurate verification environment.

The Windows NT version of the Desktop Simulation tool is now available at a cost of $5000. A UNIX-based version is scheduled for release in the second quarter of 1998. CA

Simerica Logic Semantics, *333 Clifton Ave., San Carlos CA, 94070; (650) 592-6705; www.simerica.com.*

CIRCLE 562

Tool Converts C/C++ To HDL Automatically

Many system-level designers, and those working at the behavioral level of abstraction, use C or C++ to develop design descriptions. Unfortunately, at some point, these descriptions must be converted into synthesizable VHDL or Verilog—an often tedious, error-prone, manual process. A new suite of tools, known as A/RT (Algorithm-to-Register Transfer), now offers another option: automatic conversion of algorithms to bit-accurate register-transfer-level descriptions.

The A/RT tool suite currently consists of two tools—the A/RT Library for the development of fixed-point C-descriptions, and the A/RT Builder for the direct conversion of fixed-point C-algorithms to VHDL or Verilog. The A/RT Library consists of a set of C++ classes that encapsulate the characteristics of fixed-point data types and operators. The A/RT Builder picks up where the A/RT Library leaves off, converting the C algorithm to an RT level VHDL or Verilog description that's ready for synthesis into a netlist for ASIC or FPGA implementation.

The A/RT Library is now available on a Unix platform and is free with a purchase of A/RT Builder. As a standalone tool it sells for $1000. A/RT Builder is priced at $20,000 and will be available in September on both HP and Sun workstations. CA

Frontier Design Inc., *9000 Crow Canyon Rd., Suite S-221, Danville, CA 94506; (310) 648-2683; Internet: www.frontierd.com.* **CIRCLE 563**

Nobody Does It Better!

Be sure to check out the best cutting-edge information for engineers and engineering managers, every two weeks. Here's the line-up of some of the important topics featured in our August and September issues.

OCTOBER 1, 1998 ISSUE

- **Analog Design:** Real-Time Clocks
- **PIPS:** Fiber Optics
- **Embedded Systems:** Embedded Operating Systems
- **Digital Design:** PLD/FPGA Products

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- **Electronic Design Automation**
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- **Communications/Networking Technology:** Advanced Telephony
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- **Analog Design:** Laser Drivers
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- **Digital Design:** High-Performance
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- **Communications/Networking:** Product Update
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ELECTRONIC DESIGN

TECHNOLOGY·APPLICATIONS·PRODUCTS·SOLUTIONS

Sager Electronics Builds New Distribution Center

Sager Electronics, Hingham, Mass., is building a new distribution center in Middleborough, Mass. The new facility will house all aspects of the distribution process, particularly design and layout, advanced software, and management personnel.

The new 100,000-ft^2 facility can be expanded by an additional 50,000-ft^2. The building itself will have eight dock doors; a 30-ft.-high clearance; and sealed, dust-resistant floors. Sager also is increasing its space efficiency by installing narrow aisle racks and high-density storage drawers. Sager's Semiconductor Storage Area, which complies with EIA 625 standards, will have twice its current capacity.

Sager is using OPTUM's MOVE software warehouse-management system (WMS), to automate the facility. The company hopes that it will increase its accuracy and efficiency ratings. The company is also trying to increase scalability, and the flexibility of the material-handling system. OPTUM will work in conjunction with the Rapistan Conveyor System and Diamond Phoenix Carousels to manage the workforce activities for greater efficiency. To assist in the overall supply-chain management strategy, OPTUM will also be connected to the company's new software, PeopleSoft ERP.

Sager recently hired Jim Neary as production manager in order to assist in the utilization of WMS. Previously Neary worked for UPS for nearly 20 years as a package-center manager. Neary will coordinate the functions of receiving, storage, order fulfillment, and shipping within the distribution center. The activities will include designated hot pick, multitote aggregation, kitting, and special packaging.

Sager decided to create this state-of-the-art distribution center in order to support a more aggressive sales objective that the company recently adopted. Its long term goal is to double sales volume and achieve a 25% growth rate by the end of the year 2000, therefore making Sager a $500 million company.

For more information on Sager Electronics, visit its web site at www.sager.com.

Fujitsu And Pioneer Sign Distribution Agreement

Fujitsu Microelectronics Inc., San Jose, Calif., and Pioneer-Standard Electronics Inc., Cleveland, Ohio, have signed a detailed distribution agreement. Pioneer can now offer Fujitsu's entire line of memory products, logic ICs, and flat-panel-display products.

Pioneer intends to distribute Fujitsu's memory, networking, embedded SPARC, wireless telecommunications, graphics, high-speed I/O, proprietary ICs, and flat-panel display. As new products move into the production process, they will be added to the list. The agreement covers North America, South America, and Mexico.

Mark VanZanten, acting vice president of sales for Fujitsu, believes the two companies are a good fit. Fujitsu's marketing strategy and product offerings are quite well-suited to Pioneer-Standard's market approach and core strengths, according to VanZanten. Fujitsu gains a greater coverage and market penetration, while Pioneer-Standard wins the technology required for the company's continuing growth.

For more information, contact Fujitsu at (800) 866-8608, or visit their web site at www.fujitsumicro.com. You can also visit Pioneer's web site at www.pios.com.

Wyle Electronics To Distribute White Mountain Tools

White Mountain DSP, Nashua, N.H., and Wyle Electronics, Irvine, Calif., have agreed to collaborate on the distribution of a line of White Mountain products. Wyle, a unit of VEBA Electronics Inc., will distribute the development tools for Texas Instruments' family of digital-signal processors (DSPs).

The agreement gives Wyle the right to distribute all of White Mountain DSP's TI-related DSP emulation and debug tools, White Mountain's 510-series of universal ISA, SBus, PCMCIA, PCI, and Ethernet-hosted DSP emulators, as well as multiprocessor and network-capable debug software. The GO DSP Code Composer integrated development environment is also featured.

Earle Zucht, senior vice president of marketing at Wyle, comments, "White Mountain DSP broadens Wyle's ability to provide the DSP development tools that engineers seek in order to bring their products to the market quickly. Wyle's considerable technical DSP resources, combined with the leadership in development tools of White Mountain DSP, gives customers an unprecedented value in the distribution channel."

For more information, visit White Mountain DSP's web site at www.wmdsp.com, or Wyle's web site at www.wyle.com.

Galco Named Distributor For Simpson Instruments

Galco Industrial Electronics, Madison Heights, Mich., recently signed an agreement authorizing it to distribute test equipment and instruments from Simpson, Elgin, Ill.

Jim Lawson, Galco's product line manager for Simpson, states, "I am pleased to be able to offer our customers a product that is synonymous with quality. And, furthermore, Simpson's commitment to providing total customer satisfaction mirrors our own customers' philosophies. The two companies are a natural fit."

For more information about the Simpson product line, contact the sales department at Galco Industrial Electronics at (800) 521-1615.

Lansdale Semi And Arrow Electronics Ink Agreement

Lansdale Semiconductor, Tempe, Ariz., and Arrow Electronics Inc., Melville, N.Y., have signed an agreement making Arrow/Zeus Electronics, a unit of Arrow. This makes them the sole distributor of all Lansdale's microelectronic component product lines in North America.

Lansdale produces diminishing-

manufacturing-source (DMS) military IC product lines in its Class 100 wafer-fabrication center. Included are high-reliability and critical military and aerospace ICs, which were discontinued by the OEM.

Vinnie Vellucci, president of Arrow/Zeus Electronics notes, "The U.S. military has a major procurement problem when DMS electronic components are needed for its mature, operational, aircraft, guidance, and weapons systems. Adding Lansdale to our line card will help solve this purchasing issue for our military customers." Lansdale's president, R. Lillard adds, "Arrow/Zeus' leadership position in military electronic component distribution and sales will enable Lansdale to rapidly increase our projected business growth in North America."

For more information, contact Arrow at www.arrow.com.

EBV To Handle MRV's Transceiver Products

EBV Electronics, San Diego, Calif., has signed an agreement making the company the sole distributor for MRV Communications Inc., Chatsworth, Calif. MRV is a leading manufacturer of LAN connectivity solutions, and digital and linear fiber-optic transmission products for computer networks, telephony, and cable TV communications.

MRV recently experienced a surge of growth as a result of the deregulation of the data communications industry. Linking to EBV assistance with design support and materials management in North America gives the company space for further growth. As a new product line, MRV will participate in EBVs Marketing-Innovative-Products program. MRV's newest products will be displayed by EBV's technical sales engineers in presentations made to customers' engineering design teams around the country each quarter.

For more information, visit www.ebv-electronics.com, EBV's web site.

EXAR Expands Reach With Help From Pioneer-Standard

Pioneer-Standard Electronics Inc., Cleveland, Ohio, has signed yet another agreement for distribution rights. This time it's with the EXAR Corporation, Fremont, Calif. Pioneer will distribute EXAR products in the U.S. and Canada.

Michael Class, vice president of EXAR's sales operations, stated, "The addition of Pioneer-Standard to EXAR's distribution network extends our reach into the communications, video and imaging, and silicon-sensing markets. This is consistent with our move to demand/design-in distributors and complements our existing market strategy."

To learn more about this, check out Pioneer's web site at www.pios.com.

Analog Reduces Distribution Channels

Analog Devices, Norwood, Mass., has decided to cut down its list of North American distributors. Rich Begen, Analog Devices' director of North American distribution, commented, "The analysis we conducted of our channel in North America, in context with current trends, has led us to proceed on a channel-reduction strategy aimed at more effectively servicing our end customers. We are, therefore, reducing our list of authorized North American distributors from nine to seven."

Mike Jacobs, vice president of North American sales for Analog Devices added, "The two affected distributors are Wyle and Bell Industries. This was a difficult decision and in no way reflects on their ability to act as our distribution channel, but rather is a direct result of our need to reduce the number of ADI distributors in certain geographic regions."

For more information, contact Analog Devices at (800) 262-5643; fax (781) 461-3700; and of course, you can check out their web page at: www.analog.com.

White Microelectronics And Arrow Team To Distribute

Arrow/Zeus Electronics, a business unit of Arrow Electronics in Melville, N.Y., has joined forces with White Microelectronics, Phoenix, Ariz., to distribute White Microelectronic's military lines in North America. White Microelectronics is a division of Bowmar Instrument Corp. They manufacture high-density memory products. The company has garnered a piece of the military market by offering products of high-reliability, such as SRAM, Flash, EEPROM, DRAM, and microprocessor-based products. White Microelectronic's facility is 50,000-ft^2, and has been certified, and approved by the Defense Support Center, Columbus as a Qualified Manufacturer.

Semi Dice To Distribute Analog Devices Bare Die

Effective July 31, Semi Dice becomes the sole distributor of bare die from Analog Devices, Norwood, Mass. Previous to this agreement, Semi Dice had been one of two authorized distributors of Analog Devices' bare die. "As we focus our distribution business through fewer strategic partners, we anticipate that Semi Dice will build on their successes with Analog Devices, and translate that into even better service for our mutual customers," said Gary Schneck, Analog Devices' corporate account manager.

Semi Dice is a die distributor for microelectronic circuit manufacturers. For more information contact Semi Dice at (800) 345-6633.

SEMI And ZMD Announce All-Location Agreement

All American Semiconductor (SEMI), located in Miami, Fl., announced an all-location authorization for Zentrum Mikroelektronik Dresden (ZMD), of Dresden, Germany. SEMI is a national distributor of semiconductors and electronic components, and ZMD is a veteran semiconductor manufacturer.

According to SEMI, ZMD will enhance their memory offering with a technically competitive alternative to the traditional battery modified SRAM method of building a Non-Volatile SRAM (NVSRAM). The ZMD will also continue to manufacture small-density DRAM and SRAM products. ZMD stated that SEMI will improve their customer support through local inventory and a new sales channel for their memory products.

Compiled and edited by Lisa Calabrese, editorial intern.

Turned On, Even When The Meter Isn't

Dear Mr. Novellino:

I just received the June 22 Special Analog Issue of *ELECTRONIC DESIGN*. Very nice issue, but the cover really caught my eye.

That's a pretty sad HP Model 410B you found (with tape on the side and rehashed leather handle), although I have seen some in far worse shape. The one on my bench at work is in somewhat better condition, and sitting right alongside multiple digital multimeters. I have BOTH a 410A and 410C in my home lab, both working fine and seeing frequent use. Complaint: It's turned off! What a pity.

I suspect that there are many younger readers who have little or no idea of just what a great series of instruments the 410s were. Not many analog meters were usable down to 15 mV, full scale (the 410C), nor was the ac probe on many other meters usable over a range that went from audio to at least 700 MHz. Alas, the 2-01C tube inside that probe handle is becoming a bit difficult to find, but they can be had.

Today's engineers and technicians can get active FET probes, of course, but these are generally used with spectrum analyzers. The rectifying probe, HP Model 11036, permitted a basically low-frequency device—the 410 meter—to become a rather sensitive RF testing tool at modest cost. I use it when someone else is using the spectrum analyzer.

Thanks for putting a real piece of nostalgia on your cover. It is much appreciated.

Sincerely,
Dale G. Svetanoff
Manager Electrical Development
Lindgren RF Enclosures Inc.

Dear Sir:

I am in receipt of the Special Analog Issue of *ELECTRONIC DESIGN*. I always enjoy reading the various special issues, and squirrel them away to a reference file—no sense in not using someone else's Lessons Learned!

It was a delight to see the Ol' HP vacuum-tube voltmeter (VTVM) on the front cover, too bad it wasn't turned on! One of my favorite home-builts as a lad was a Heathkit VTVM, which served me faithfully for many years. Later I built up Heathkit's transistorized voltmeter, which used a new-fangled FET at its front end, but I always went back to the VTVM. There was always something friendly about a box that sat there on the bench, slightly warm to the touch, and always showed a magical red glow from the tube filaments when you peeked inside.

Thanks for the fine magazine!
Karl Strauss
Jet Propulsion Laboratory
Pasadena, CA 91109

ELECTRONIC DESIGN's Managing Editor, Bob Milne answers:

Glad you liked the Ol' 410B on the cover. Sure, we could have cleaned it up and taken off the tape, but we decided to let our readers see it just as it was when it arrived at the office.

There it sat, showing all the obvious signs of heavy usage and the passage of time. How many hands had it been through? How many problems had this classic meter helped locate?

When we fired it up, it worked perfectly, and the switches felt solid. And, oh boy, those nice big knobs of yesteryear sure were easy to use. Have you been squinting at any little rows of tiny buttons with hard-to-read labels lately?

In many ways, that meter's like a lot of you analog designers out there—aged and battle scarred. But you can still cut the mustard when called upon to perform a little analog "magic."

It's not turned on, but it should be—and that's the point. How many other fine test instruments are laying around gathering dust when they could be put to good use?

And, the very careful observer may note that we have an HP meter from the '50s hooked up to a Tektronix prototyping system containing circuits designed several decades later. Can the 410B hack it? Send your comments to bmilne@class.org.

Correction

A software translation error at the press caused several incorrect mathematical expressions in "Reduce Component Sensitivity In Single-Op-Amp Filters," on page 10 of the June 22, 1998 Special Analog Issue. The expressions that appear as –fi and fi should have been –1/2 and 1/2.

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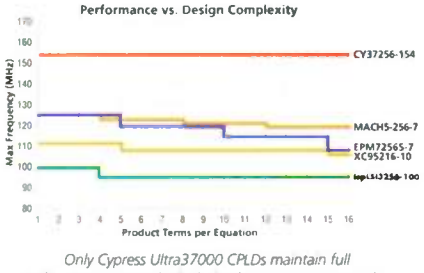

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Part No.	Macrocells	t_{PD} ns	f_{MAX} (MHz)	I/O Pins $_{MAX}$	Package
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CY37064	64	6.5	167	69	TQFP, PLCC
CY37128	128	6.5	167	133	TQFP, PLCC
CY37192	192	7.5	154	125	TQFP, PLCC
CY37256	256	7.5	154	197	TQFP, PQFP BGA
CY37384	384	7.5	154	197	PQFP, BGA
CY37512	512	7.5	154	269	PQFP, BGA

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