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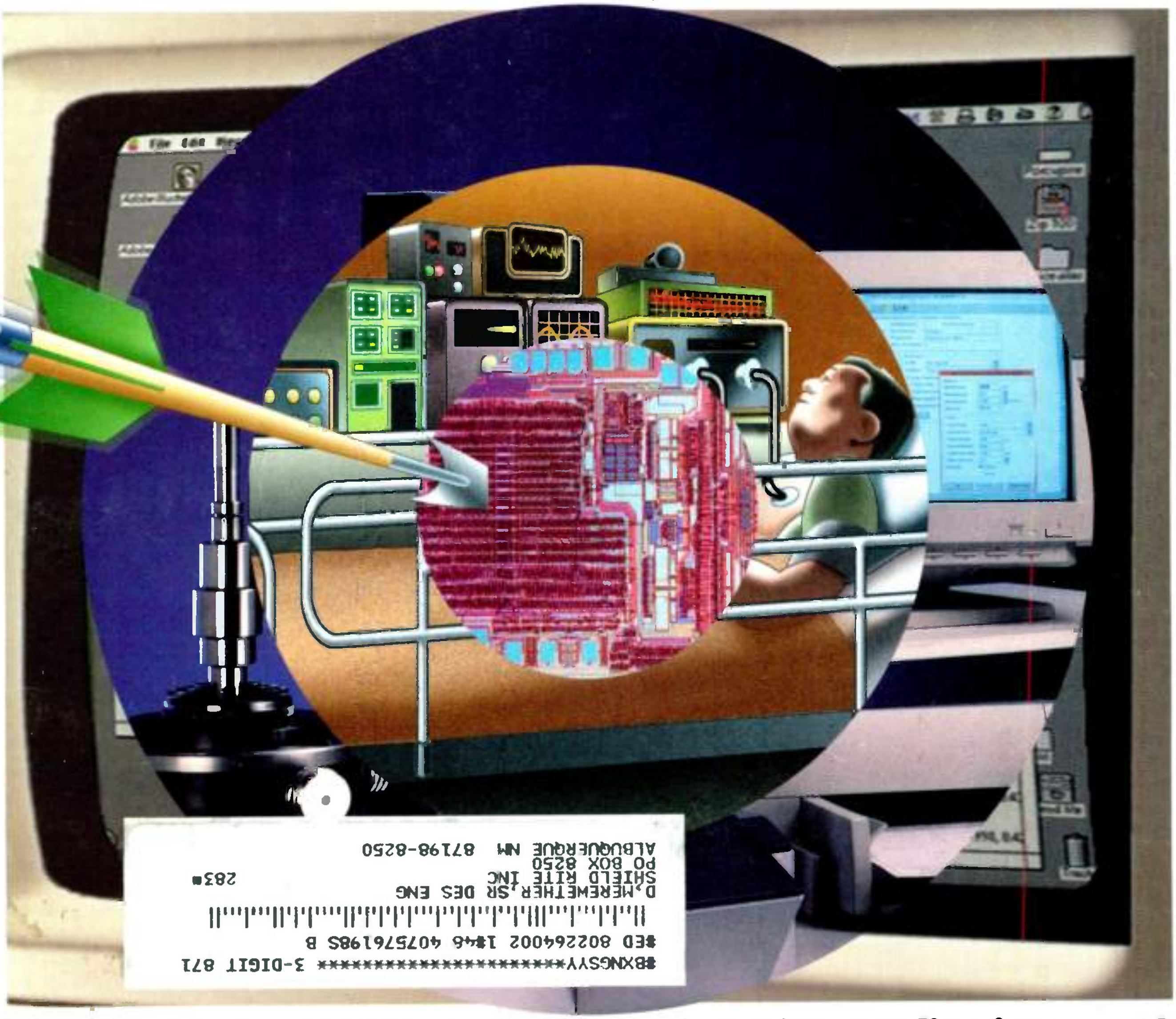
ELECTRONIC DESIGN

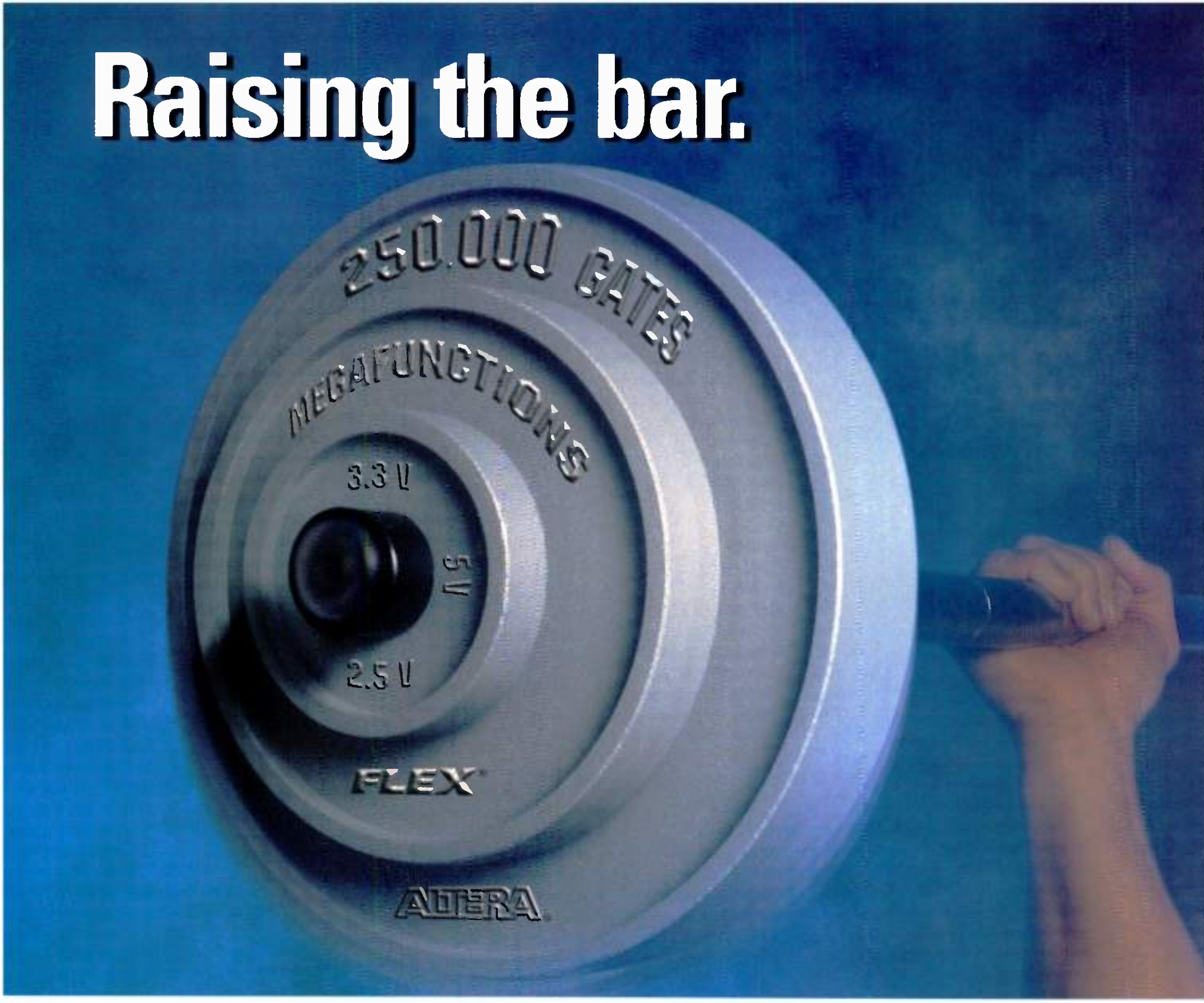
TECHNOLOGY · APPLICATIONS · PRODUCTS · SOLUTIONS

A PENTON PUBLICATION $8.00 www.elecdesign.com SEPTEMBER 1, 1998



High-Resolution ADC Targets Data-Acquisition Applications p. 68

Raising the bar.



250,000 gates strong.

The newest, largest member of the FLEX® 10K embedded programmable logic family — the EPF10K250A — is now available. The EPF10K250A device combines the flexibility of programmable logic with the capacity and speed you need for even your largest gate array designs.

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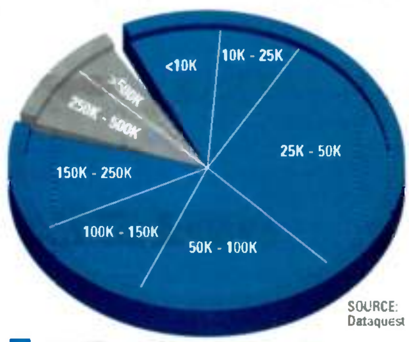
With 250,000 gates, the EPF10K250A covers 80% of gate array design starts. This device provides a 3.3-V core voltage with MultiVolt™ I/O to interface to 5.0-, 3.3-, and 2.5-V systems, and is available in packages of up to 600 pins, including BGA options.

The biggest — bar none.

Visit the Altera web site for more information about all FLEX 10K devices — and sign up for a free megafunction literature pack. Use the integration density of the EPF10K250A to raise the bar on your competition.

Gate Array Design Starts by Gate Count (1997)



FLEX 10K device density covers more than 80% of gate array design starts.

www.altera.com/bar

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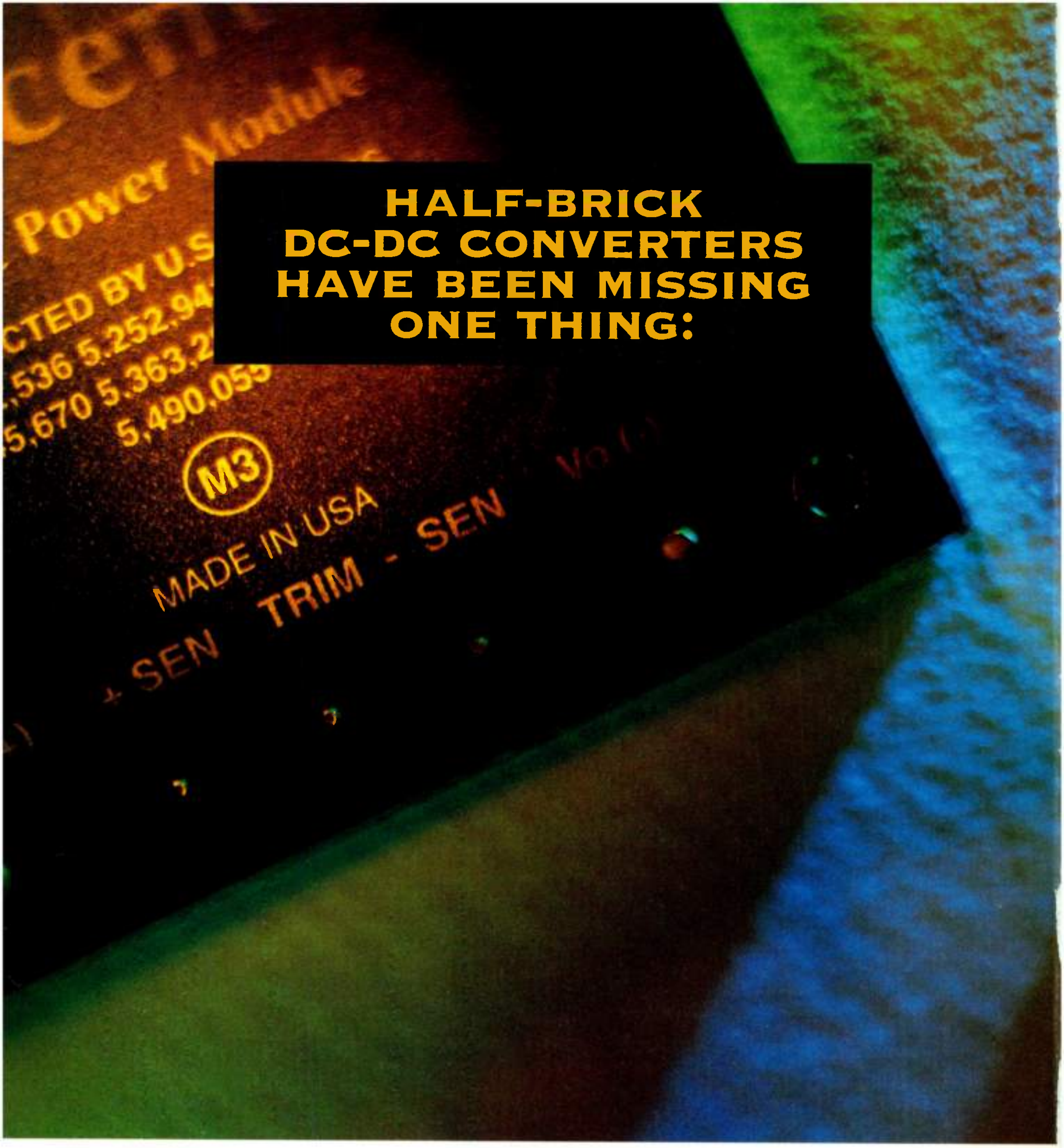
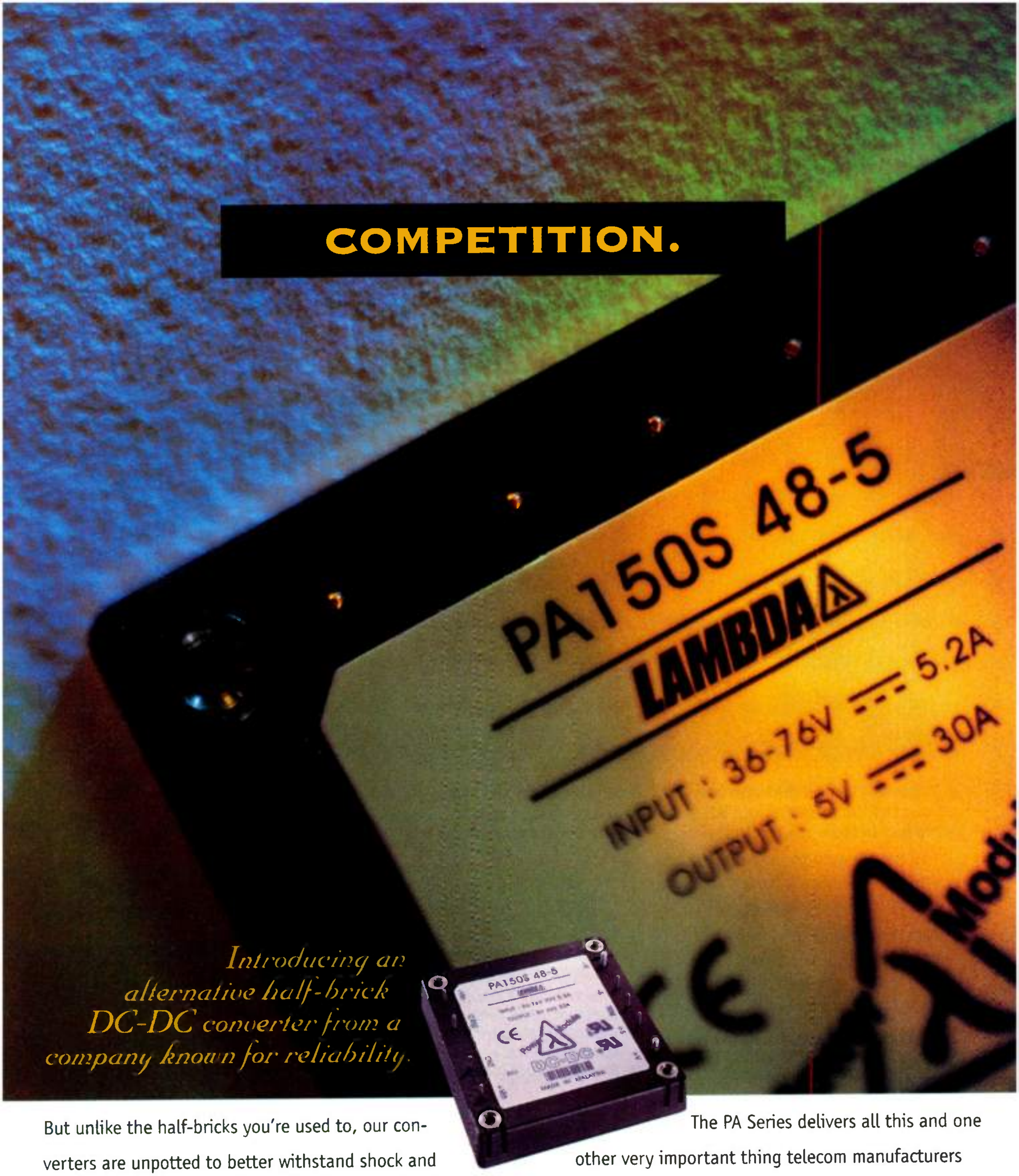


HALF-BRICK DC-DC CONVERTERS HAVE BEEN MISSING ONE THING:

Nobody likes being tied to a single source. So it's good news that there's an alternative pin-for-pin replacement for the "half-brick" DC-DC converter.

It's even better news when it comes from a company with fifty years experience making the most reliable power solutions for the most unforgiving applications.

Lambda's power modules have demonstrated over five million hours MTBF. Our new PA Series brings that proven performance to designs requiring industry standard half-brick pinouts. These modules are built to the highest quality standards, with a reduced part count that enhances reliability and allows us to offer high efficiency and power density at an economical price.



But unlike the half-bricks you're used to, our converters are unpotted to better withstand shock and vibration, require no pre-load, and provide 17% more current on a 3.3V output.

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A choice.

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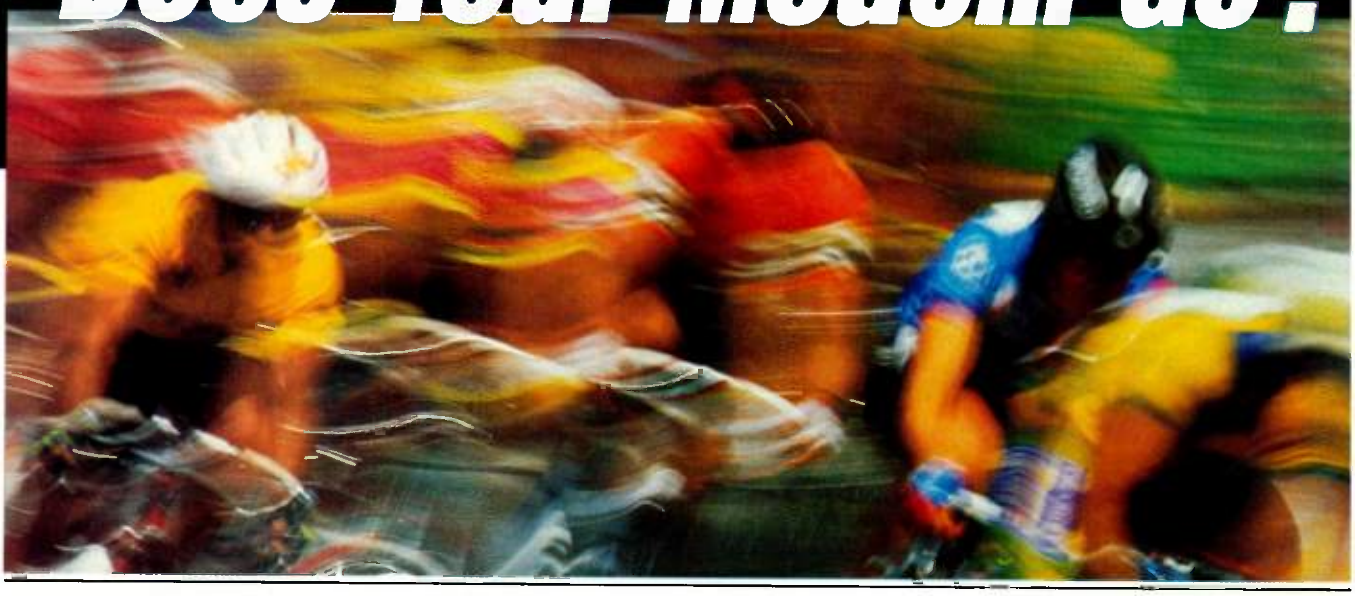
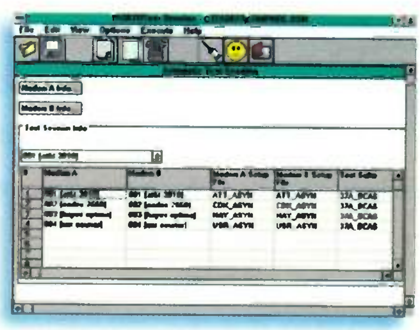
How Fast Does Your Modem Go?



In the hotly contested modem business, you need the tools that will put your product in the winner's circle.

TAS has been providing advanced test and evaluation solutions to modem industry leaders *for over twelve years.*

With the advent of *new* modem technologies **such as 56K,** *accurate and repeatable testing is more important than ever!*



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- ***Gemini & Gemini-PC*** *data analyzers thoroughly test the throughput and error-rate performance of external, PC-Card, and controller-less modems.*
- ***TASKIT® Software*** *automates the entire testing process and gives you comprehensive performance reports.*

If you are testing or evaluating subscriber or central site modems, give your product the best chance to win the race.

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ELECTRONIC DESIGN

TECHNOLOGY•APPLICATIONS•PRODUCTS•SOLUTIONS

September 1, 1998 Volume 46, Number 20

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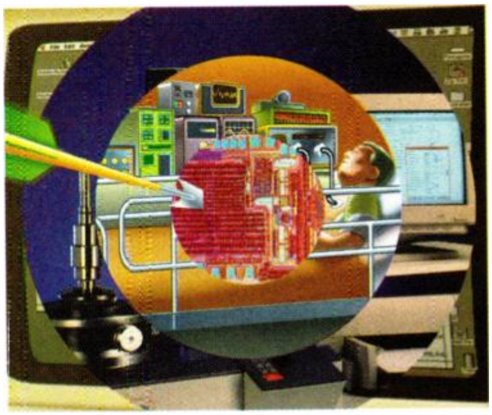

TECH INSIGHTS

TECH INSIGHTS

ANALOG OUTLOOK

DEPARTMENTS

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ELECTRONIC DESIGN

TECHNOLOGY • APPLICATIONS • PRODUCTS • SOLUTIONS

September 1, 1998 Volume 46, Number 20

EDITORIAL OVERVIEW

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BPA INTERNATIONAL

LOOKING AHEAD: September 14, 1998

● **T&M Update—VXIbus:**............ Test & Measurement Editor Joseph Desposito describes technology changes that will ensure VXIbus's viability well into the future, and a design application examines the use of VXIbus in accelerated design verification.

● **Boards & Buses:**....................... Computer Systems Editor Jeff Child reports that significant updates keep VMEbus as strong as ever after 17 years. Also, a columnist explains the impact of open networking on industrial automation.

COVER ILLUSTRATION BY: BRUCE JABLONSKI

Jesse H. Neal Editorial Achievement

1967 First Place Award	1978 Certificate of Merit
1968 First Place Award	1980 Certificate of Merit
1972 Certificate of Merit	1986 First Place Award
1975 Two Certificates of Merit	1989 Certificate of Merit
1976 Certificate of Merit	1992 Certificate of Merit


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About Electronic Design

ONLINE OVERVIEW

September 1, 1998 Volume 46, Number 20

See Electronic Design Online's Table of Contents to preview what's in store for you on the web!

NOW ONLINE:

A New Partnership

Beginning this month, **Electronic Design Online** and the **Electronics Design & Technology Network (EDTN)** will enter into a partnership that will create and deliver a single source for technical information, design solutions, and industry news for design engineers and managers, worldwide.

As a new partner of the **EDTN Network, Electronic Design Online** will continue to provide its audience the important technical information on the various architectures and other design challenges facing the engineering community. Now, using **EDTN's** news-gathering ability, we will be able to bring you up-to-the minute news and information on what's happening in the industry

EDTN network

TECHNOLOGY LAB
Debra Schiff reviews the newest books on the Y2K problem

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UNIVERSITY
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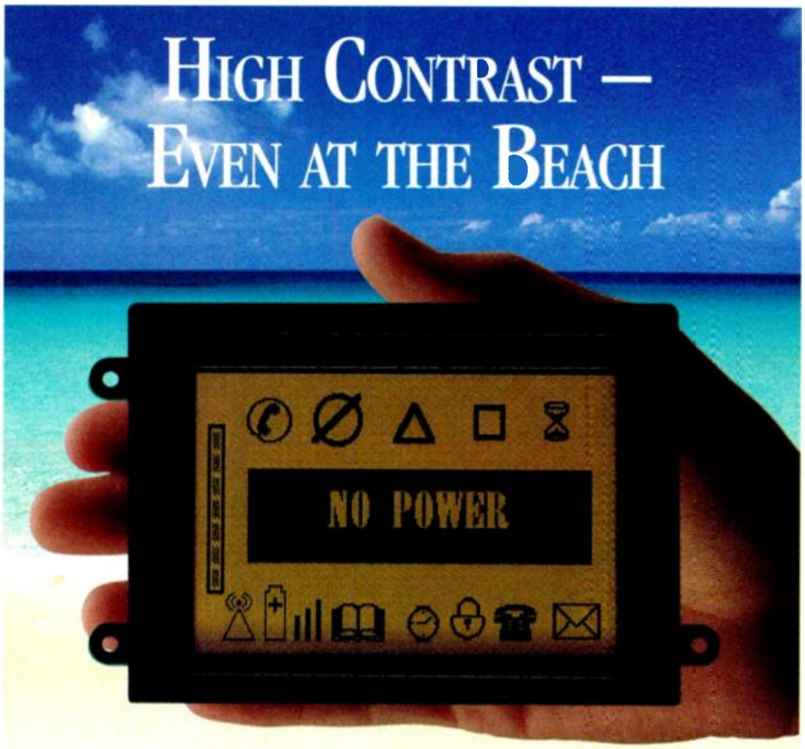
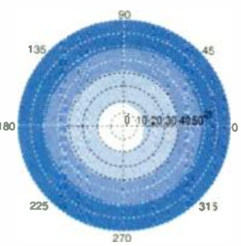


KENT ChLCD™ NO POWER DISPLAYS

EASIEST TO READ REFLECTIVE TECHNOLOGY

Compared to conventional LCD technologies, KENT Displays' ChLCD (Cholesteric Liquid Crystal Display) technology offers better reflectivity, a 360 degree viewing cone and exceptional daylight contrast, even in direct sunlight – all without backlighting.



This contrast ratio polar representation illustrates KENT's 360 degree viewing cone.

BREAK THE BATTERY-DRAIN BARRIER

Since ChLCD reflective and transparent textures are both stable states, an image can be displayed indefinitely without consuming battery energy – for seconds, hours, weeks, months or even years.

STANDARD OR CUSTOM DISPLAYS AVAILABLE

Standard ChLCD displays and modules are available in sizes and colors to meet your needs. Have a special application? KENT Displays offers ChLCD displays and modules custom designed to your requirements.

ASK FOR THE FACTS

To learn more about this technology that enables you to do more, ask for this package today.

KENT DISPLAYS INCORPORATED

A MANNING VENTURES BUSINESS UNIT

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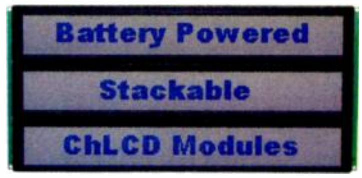
New Redesigned Infosign™

1997 Product of the Year Award
ELECTRONIC PRODUCTS MAGAZINE



Kent Displays' next generation of Infosign products, this Three-Panel Infosign is available with or without a controller. A single "Three Panel Infosign" with controller can control up to 9 additional displays for a total of 12. This means that you can combine individual Info-Strips with Three-Panel Modules in any combination to fit your particular signage needs. Like the original Single-Panel Infosign, this Three-Panel can be updated quickly from a remote computer with the Windows 95 compatible software that is included. Options include wall mount and floor stand enclosures in silver, black and gold, with or without battery pack, in 3, 6 or 12 display configurations.

Infosigns are ideal for point-of-sale displays, door signage, battery-powered signage, kiosks, airport- and bus-terminal signage and more.

Infosign displays feature ChLCD technology for high contrast and wide viewing angle. They are available with a standard resolution of 20 dpi and an active viewing area of three, 12 in. x 1.5 in. panels. Display color combinations of yellow/black, yellow-green/black, green/black and blue/white are available.

KENT Displays, Inc., 330-673-8784
E-mail: sales@kentdisplays.com

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1/4 VGA "No Power" Displays

Kent Displays' 1/4 VGA ChLCD "No Power" design not only provides exceptional readability but also requires no power to maintain displayed images, only to change them. Because power isn't constantly being drawn upon to retain the image, expect exceptionally long battery life. As such this display is ideally suited for portable battery-operated applications as well those information display projects where the display must be easily readable at any angle even in direct sunlight.

The 1/4 VGA format is ideal for portable communication devices, data collection products, global positioning systems and more. Available with or without an on-board controller, in 4 color combinations yellow/black, yellow-green/black, green/black or blue/white and featuring an imaging area of 4.48 in. x 3.36 in. with a pixel resolution of 72 dots per inch.

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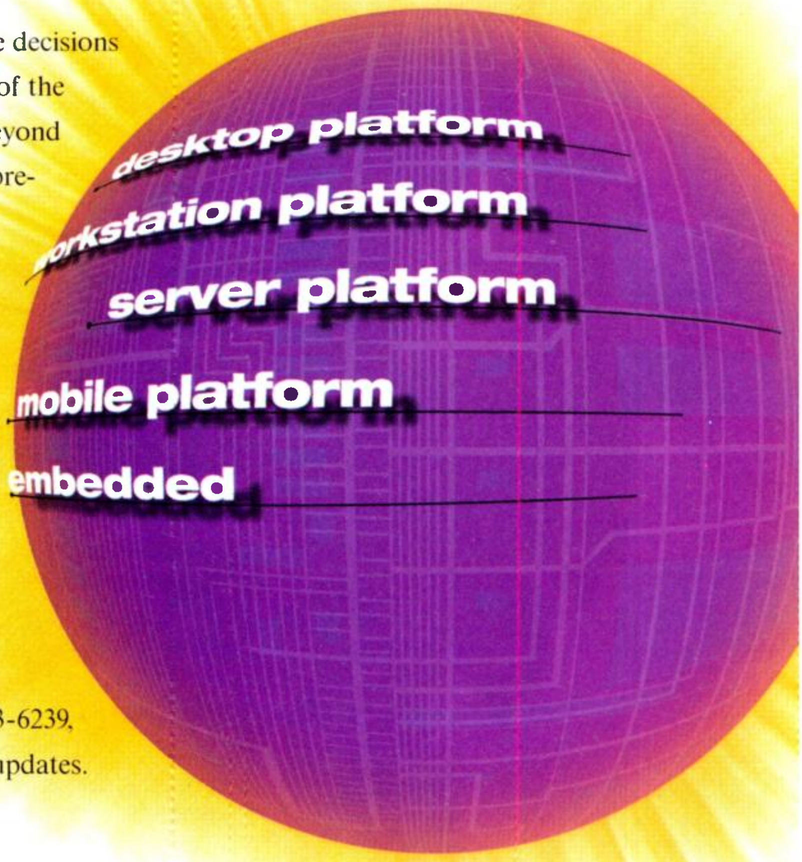

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Our analog-interface screens make it easy to design standalone LCD monitors that offer full compatibility with CRT monitors. They help designers simplify circuitry and shrink system size because they require no A/D conversion and complex image data processing. To slash your development time and costs, interface boards compatible with CRT monitors are available as an option.

Digital-interface models are the optimum solution for desktop PCs with an integrated LCD screen. They're also the first choice for many industrial applications. All our digital screens offer a low-voltage differential signaling interface (LVDS) and display 262,144 colors.

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Size	Resolution	Viewing angle	Model
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15.4"			NL128102AC23-01 (NEW)
15"		Ultra-wide	NL10276AC30-01
15"	1024 x 768	Wide	NL10276AC30-03
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14.1"			NL10276AC28-01
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An Alliance For The Future

"Andy Grove argued that at times of technological change, any business can face dramatic changes in its environment—changes that he called 'strategic inflection points.' Make the right decision at the inflection point, Grove said, and your company can look forward to sunny years of future growth. Get it wrong, and you will slide inexorably into decline."—from *Inside Intel*

We in the publishing industry have come face to face with a strategic inflection point. Actually, we've had it easy. The only real significant inflection point in the publishing business occurred back in 1456 when Johannes Gutenberg put a lot of monks out of business after he invented the first European printing press, and began cranking out bibles.

Now, some 542 years later, a technology has emerged that's beginning to revolutionize the way human beings send and receive information. What is amazing about this new consumer and business technology is that it's basically only a few years old, but already some 100-million-plus people worldwide are using it as their primary source of receiving information.

The technology is, of course, the Internet. And, I can tell you that there isn't a magazine or newspaper publishing executive alive who isn't tossing and turning at night, trying to figure out how to convert and expand their print publications to the web, and include a wide-ranging array of new, creative content.

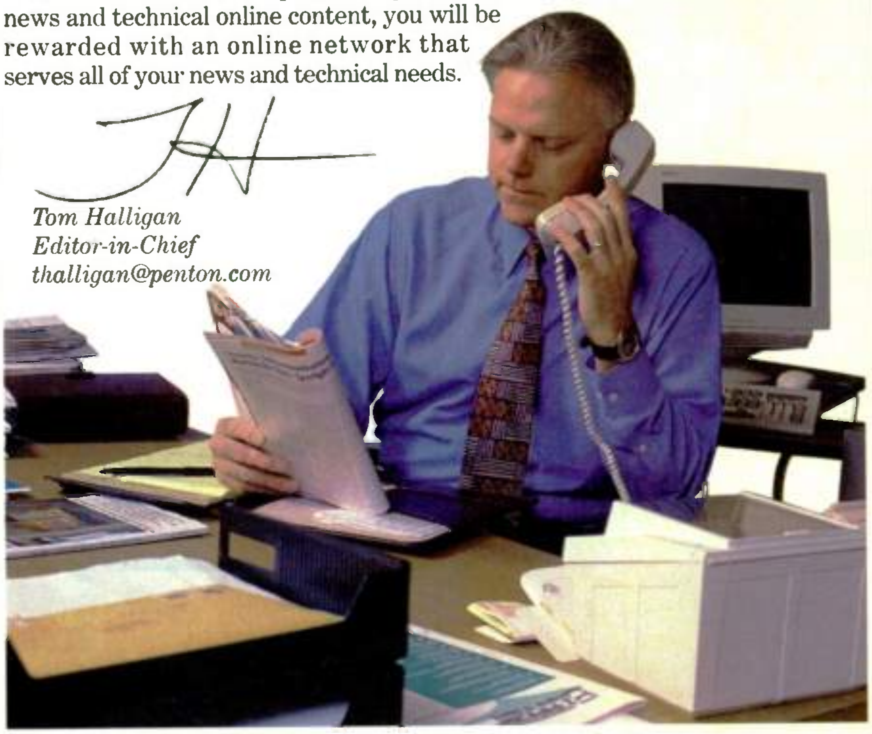
Previously, there was no single, all-inclusive web source for design engineers and engineering managers to go to for objective news, technical information, vendor data, and ancillary electronic engineering information.

Until now.

Realizing that no single publication had the wherewithal to become the complete news and technical resource and solutions center, Penton Media's *ELECTRONIC DESIGN* has partnered with CMP Media's EDTN (Electronic Design & Technology News) Network to offer the most comprehensive online news and technical network for design engineers and engineering managers.

Because EDTN draws a significant portion of its news from *EE Times*, by all accounts, the most respected industry news source, the addition of *ELECTRONIC DESIGN* and *ELECTRONIC DESIGN ONLINE* now brings to the Network the most comprehensive technical resource for design engineers and engineering managers.

We look forward to the partnership, and as both companies begin to merge our news and technical online content, you will be rewarded with an online network that serves all of your news and technical needs.



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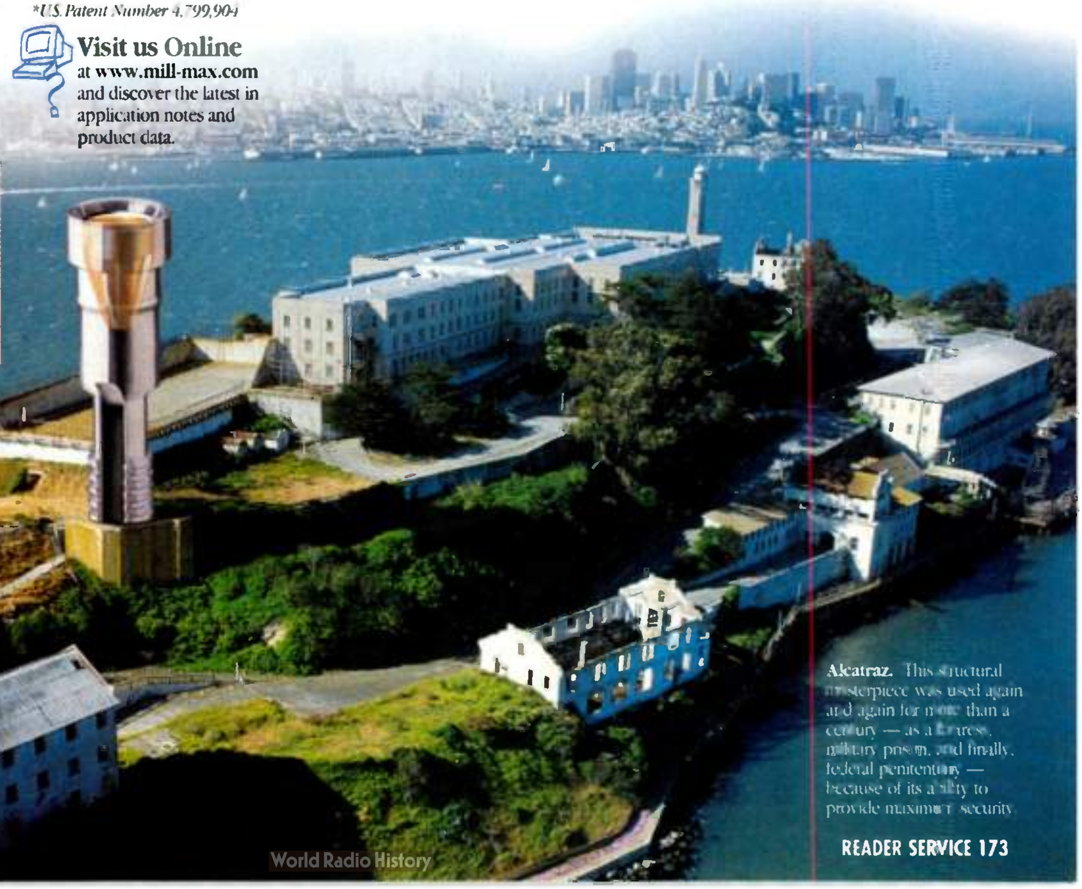

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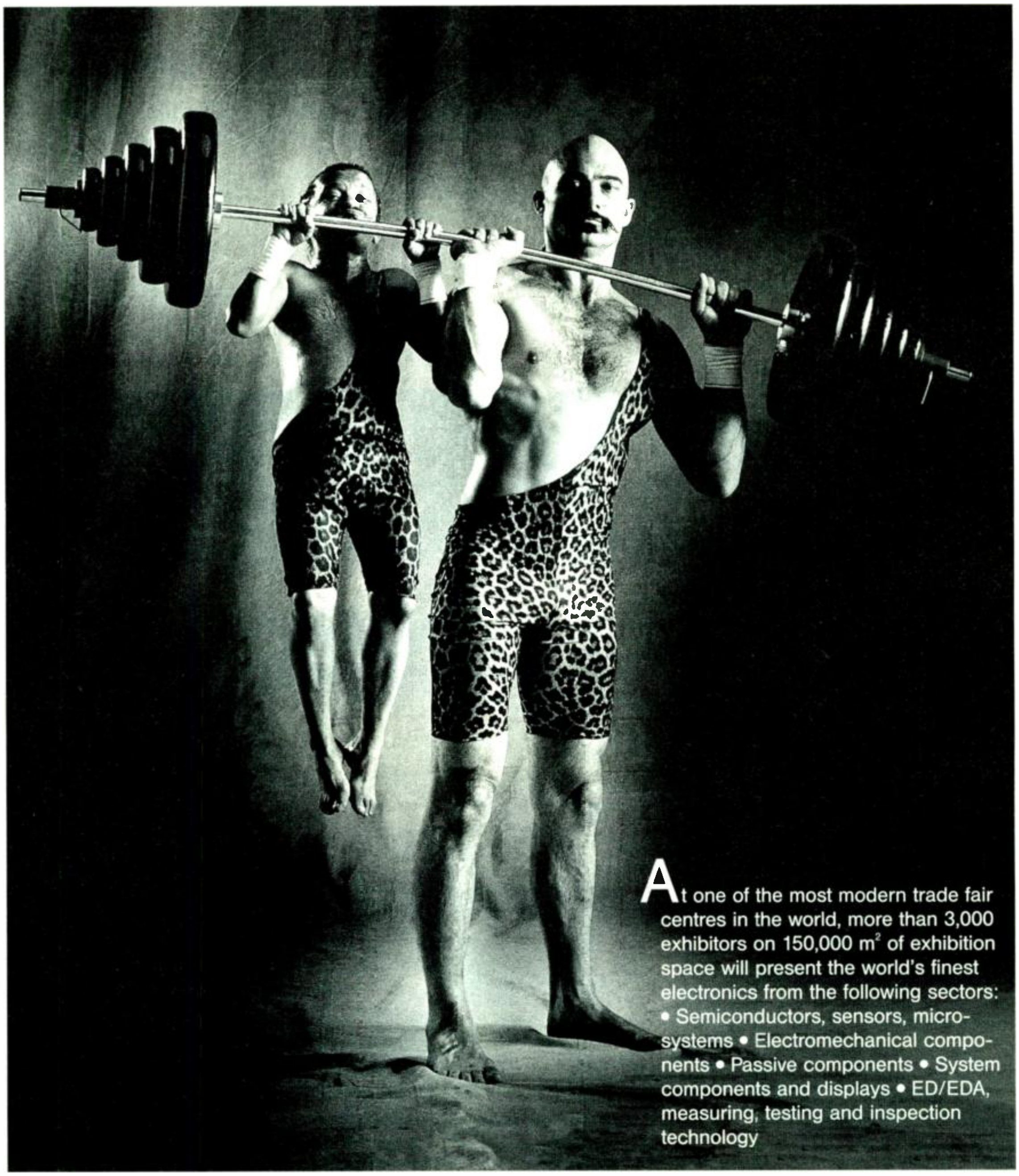

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Not Another Acronym!

Is there anyone out there who's as sick of this whole acronym business as I am? I'm sure you know what I mean. After all, if you work in the electronics industry, you face this problem daily. Depending on who you talk to, and the context of your conversation, a PC could, for example, refer to a personal computer or a printed-circuit board. And, don't get me started on IP. What does that stand for? Intellectual Property? Internet Protocol? Important Person? Despite the fact that my husband assures me that it stands for the latter, as in VIP, or Very Important Person, I've come to realize that dealing with acronyms is just not that simple anymore.

Part of the problem is that some acronyms are used differently by more than one segment of the industry—a practice that leads to much confusion. But that's only half of the problem. Sometimes acronyms don't even represent what they say they do. As a result, even though people may use a particular acronym day in and day out, chances are, half the time they don't even know what they are really saying. For example, have you ever heard the saying, "You'd better mind your Ps and Qs?" Would it surprise you to know that despite the way in which it is often used today, it actually stands for pints and quarts.

Which brings me back to why this whole acronym business has been on my mind lately. Actually, it's all thanks to Gary Smith, Electronic Design Automation (EDA) Analyst for Dataquest Corp., San Jose, Calif., who recently pointed out over lunch that my use of the acronym IP to mean Intellectual Property is incorrect.


CHERYL AJLUNI
ELECTRONIC DESIGN AUTOMATION

Often when I talk to him I feel like I'm having an E. F. Hutton commercial flashback. You remember the one that goes "When E. F. Hutton talks... everyone listens." Consequently, I found myself seriously pondering what he had said and why.

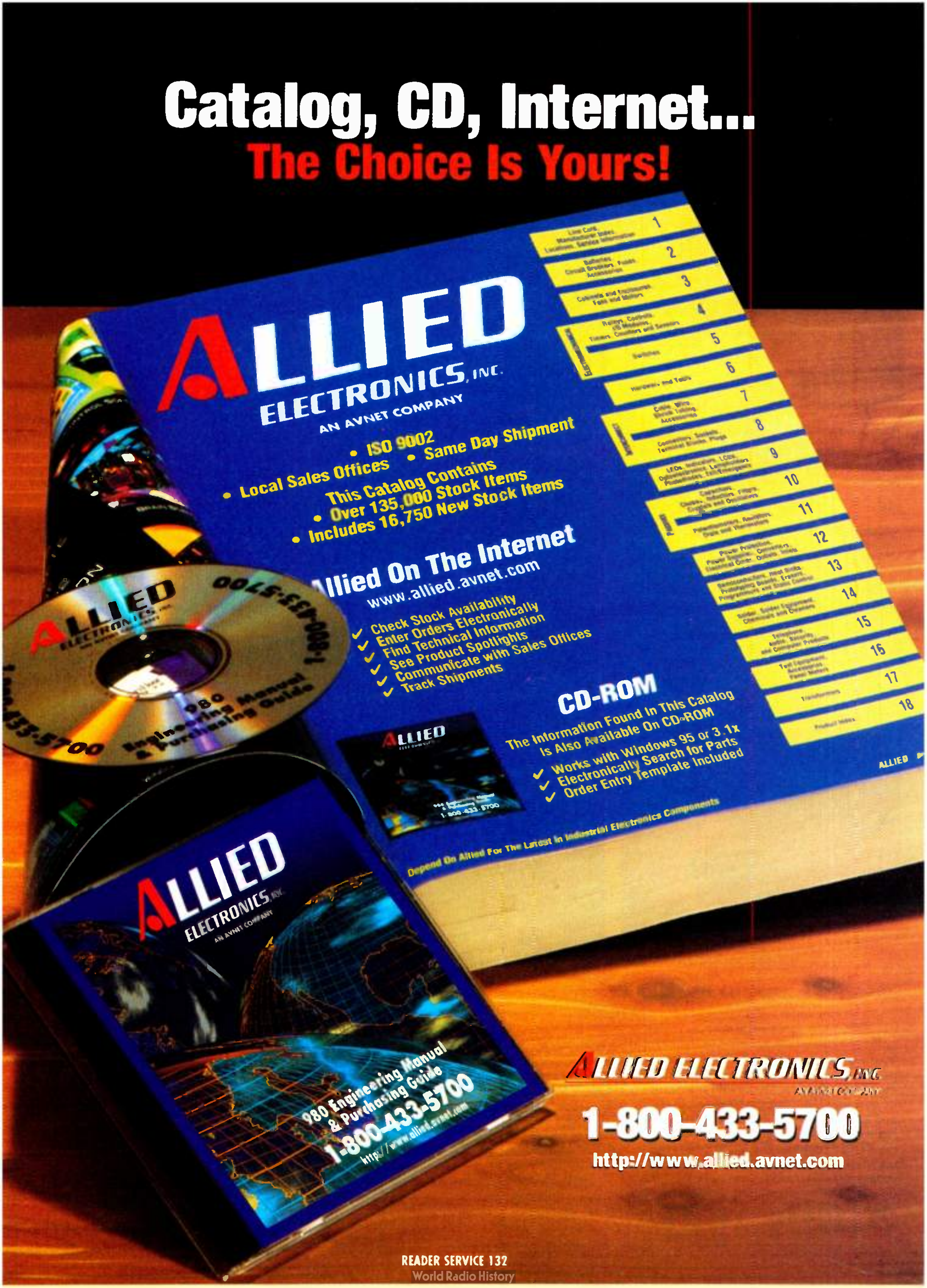
What I came to realize is that Smith is right. The way I, and many other people, have used the acronym IP is incorrect. Unfortunately though, it has been misused for so long now that it has literally become associated with something totally different than its original meaning.

In the EDA industry, we use the acronym IP to refer to some flavor of core which is used in a design. It is what makes design reuse possible, and helps speed time-to-market. But, I have it on good authority—Smith's daughter, a lawyer who works for a legal firm specializing in Intellectual Property Law—that this term is not really Intellectual Property. In fact, to actually have Intellectual Property, you need one of the following: a patent, maskworks, a copyright, a trade secret, or a trademark.

Now think about it. How many IP vendors do you know of today that claim to have any of these things? And, if not, then why do we keep using the acronym IP? Part of the answer boils down to money. IP vendors use the term because, as Smith explains, they are asking for royalties. But, in reality, only a select few actually get royalties.

Another reason is that while the acronym may be incorrect, people in the electronics industry typically understand what you mean when you use it. In fact, it has become quite the buzzword of the 1990s, offering an easy way to draw attention to your company or product. As Smith points out, "if you want a lot of web-site hits, you have to get it into your press release."

But the fact remains that IP stands for Internet Protocol, not Intellectual Property. And, what we have come to refer to as Intellectual Property is not even really Intellectual Property. So where does that leave us? Well, as my mother always said, "If it walks like a duck and talks like a duck, then it's a safe bet it's a duck!" So, for the time being, I've decided to talk about IP in terms of cores—at least until someone else tells me that this is wrong too, and comes up with a better alternative. Let me know what you think. *cjajluni@class.org*.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- IEC Touch-safe Eurostyle-type terminals

Agency approvals: UL 506, CSA C22.2 #66 1988, TUV Rheinland EN60742 / IEC 742

See Specs: www.signaltransformer.com/MPI/ed

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- 25-amp rated 5-mil copper screen
- IEC Touch-safe Eurostyle-type terminals

Agency approvals: (HPI-20, 27, 35) VDE 0550, UL 506, UL 2601-1, CSA C22.2 #66 1988; (HPI-12, 15, 17) TUV Rheinland, EN 60950 / IEC 950, CSA C22.2 #66 1988, NRTL / C ANSI UL 506

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Agency approvals: VDE 0805 / EN60950 / IEC 950, CSA C22.2 #66 1988, UL 506; also designed to meet construction requirements of UL 478, 1411, 1563, 1585, 2601-1, EN60742, IEC 601-1, IEC 742, IEC 65, IEC 1010

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Keynoter Hints At Changing Direction For Signal Processing

While more than 300 technical presentations from around the world will attempt to cover advances in over 30 applications areas for DSP, the highlight of this year's DSP World is the keynote address by Soenke Mehrgardt, president of Siemens AG's Signal Processing Div. The speech will shed light on the changing direction for signal processing, as software-driven digital technology pervades all walks of life.

The ninth DSP World, which also features the International Conference on Signal Processing Applications & Technologies (ICSPAT), will be held at the Toronto Metro Convention Center in Canada, Sept.13-16.

"The demands of system-on-a-chip design are driving the industry to new approaches in hardware/software codesign and reprogrammability for DSP cores," says Mehrgardt. In his keynote talk, Mehrgardt will review the demand for both general-purpose architectures and dedicated DSP solutions for specific applications. In addition, he will discuss parallel execution and superscalar structures, as well as other approaches to increasing the efficiency for future DSP applications. According to Mehrgardt, this fundamental shift in signal processing will dictate flexible configuration and integration of cores, memories, and peripherals under a common platform that will also support customer IP and application-specific designs.

Other conference highlights include the Industry Technology Forum (ITF) and panel discussions. The ITF will bring leading-edge DSP chips and boards, as well as new tools, from key players in the field. Panelists will debate various architectural alternatives that are available today and provide insights into the requirements of various applications. While the Monday (Sept.14) morning panel will debate superscalar RISC versus VLIW versus multi-MAC architectures, the Tuesday (Sept. 15) afternoon panel will discuss DSPs versus microcontrollers in embedded applications. The DSP World program also includes 44 one- and two-hour workshops for engineers with varying levels of DSP experience. Topics covered include the use of DSPs for microcontroller functions, the use of commercial off-the-shelf DSPs, optimizing DSP software for the latest microprocessors, and implementation of wavelet-based solutions.

For additional details on this year's DSP World/ICSPAT, check their web site at *www.dspworld.com.* AB

1394-Compliant IP Package Under Development

Integrated Intellectual Property (I_2P) and Technology Rendezvous Inc. (TRI), Santa Clara, Calif., are now collaborating on delivering 1394 Intellectual Property cores that comply with 1394 software stack and protocols. I_2P's current offering in this area is a 1394 soft-core solution for 1394-compliant designs featuring highly modular LINK and PHY synthesizable cores, as well as robust functional verification environments. Virtual sockets are provided to quickly adapt the 1394 cores to various 1394 applications. Technology Rendezvous offers FireStack software, which is a highly customizable stack and protocol solution for IEEE-1394. It's available with various protocols and is supported on a number of RTOSs, including Nucleus, OS/9, and WinCE.

As part of the development effort, the parties will pool their expertise in each of these areas to produce a comprehensive turnkey solution for 1394 device connectivity. The solution will contain both the I_2P 1394 cores and TRI's FireStack. For designers, this will mean a seamless integration between 1394 software and I_2P's cores, and drastically reduced design cycles and time to market. It also will provide an avenue for designers to design complete 1394 designs, including hardware and software. For more information, contact Technology Rendezvous at *www.trinc.com*, or Integrated Intellectual Property at *www.I2P.com.* CA

Photoresist Removal Process Could Cut Out IC Process Step

Recently announced breakthrough results have culminated in a new damage-free, residue-free photoresist removal process. Developed by GaSonics International, the novel high-dose/high-energy implant photoresist removal process (currently being beta tested at a leading European IC manufacturer) maximizes process effectiveness and productivity. At the same time, it reduces cost of ownership (COO) for this critical step in advanced IC fabrication.

As CMOS geometries tighten, the number and complexity of implanted photoresist removal steps in advanced devices increases. A low-energy/high-dose implant enables the creation of shallow junctions, which must have low sheet resistance to maintain high currents and corresponding high device speeds. The retrograde well structures and buried layers characterizing CMOS devices are the result of a high-energy implant.

During the implant process, a difficult to remove carbonized crust is formed on the resist surface. Outgassing subsequently occurs through this layer, and residues are left on the wafer that must be removed. Preliminary beta-test results indicate that the new process reduces implanted resist skin breakthrough time by up to 75% with no photoresist "popping," which typically occurs when implanted photoresist is heated during the photoresist removal process.

Because the new process is residue-free, it enables semiconductor manufacturers to reduce or eliminate the need for a subsequent wet process step. This lowers COO and reduces process time. A recently developed plasma source complements GaSonics' traditional downstream microwave source to provide this damage-free, residue-free process. The new process is compatible with GaSonics' PEP clean platform, which provides dual clean chambers that can be run sequentially, independently, or in parallel. Upon completion of the beta testing in late August, the new process will become available to other customers or may be retrofitted on existing PEP tools.

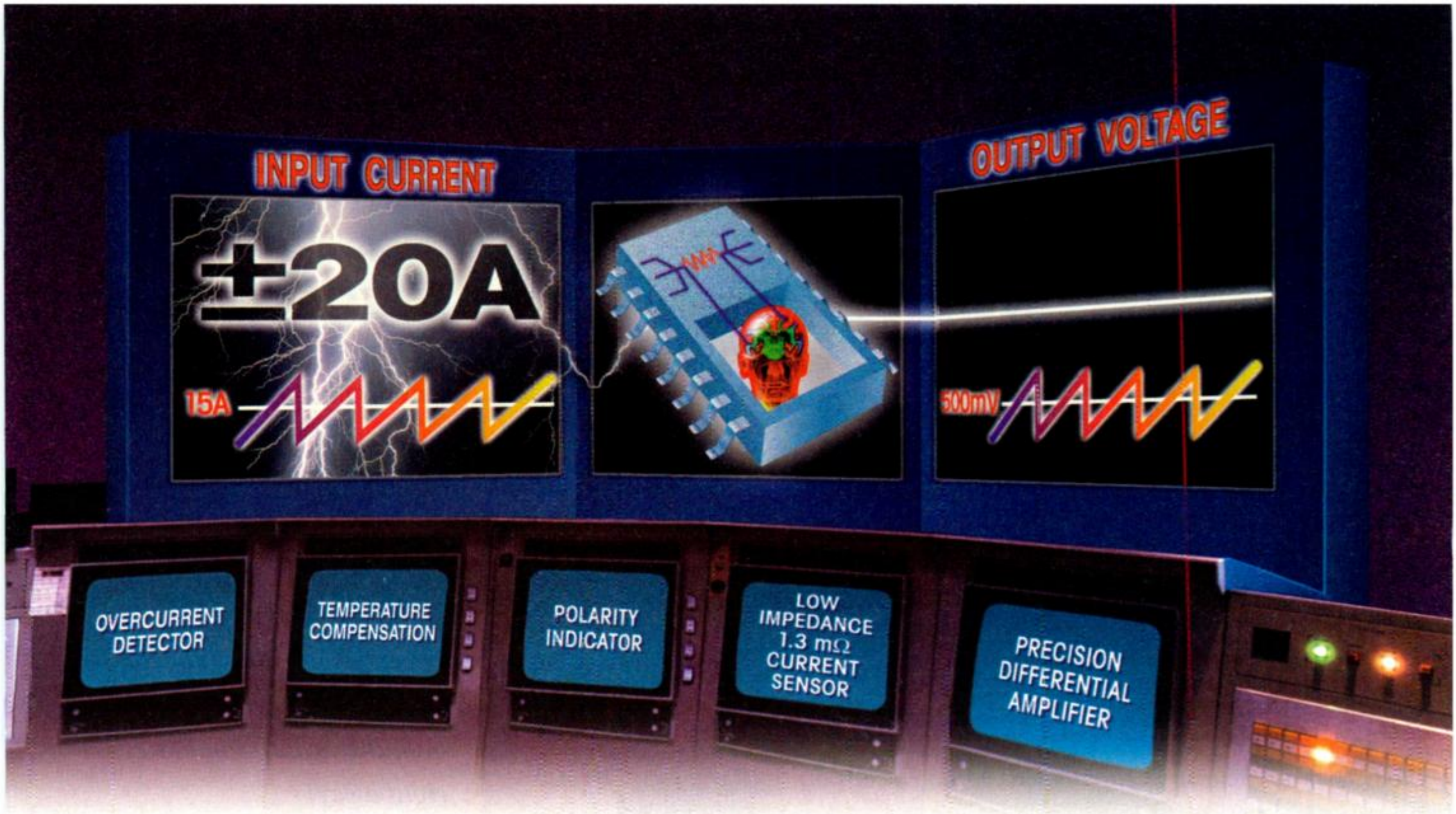
For more information, contact Andy Kirkpatrick at GaSonics International, 2730 Junction Ave., San Jose, CA 95134; (408) 570-7400; fax (408) 325-1222; *www.gasonics.com.* JC

Seven Vendors To Multisource 1-By-9 Optical Transceivers

Seven of the world's largest suppliers of fiber-optic components have decided to offer 1-by-9 duplex form-factor Gigabit Ethernet transceivers. These devices will feature a common termination, biasing, and signal-detect interface. The 1-by-9 package is a commonly available package style used in applications ranging from Fibre Channel to emerging Gigabit Ethernet LANs. The group comprises Sumitomo Electric Lightwave Corp., Siemens Microelectronics Inc., Optical Communication Products Inc., Molex Fiber Optics Inc., Honeywell's Micro Switch Div., Hewlett-Packard Co., and AMP Inc.

The key motivating factor behind the agreement is the need for designers to have a multiple source for transceivers to ensure continuity, compatibility, and lower costs. Each company has agreed to establish internationally compatible sources for gigabit-speed 1-by-9 form-factor transceivers, which will be offered for single- and multimode fiber. The devices will have common footprints and pin definitions, along with identical electrical interfaces at transmitter and receiver pins. Inputs and outputs will be dc-coupled, requiring that electrical biasing and termination be done external to the transceiver on the customer's pc board. The Signal Detect pin will use a positive emitter-coupled logic interface.

For more information, contact any of the above companies, starting with Paul Pace, Sumitomo Electric Lightwave Corp., Research Triangle Park, NC; (919) 541-8339; e-mail: *ppace@sel-rtp.com.* PM



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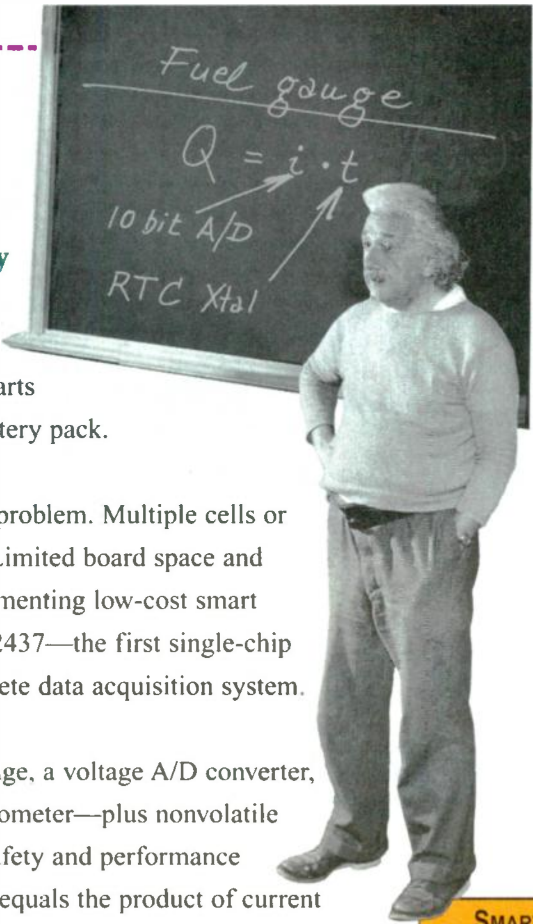

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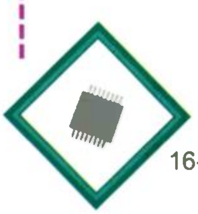

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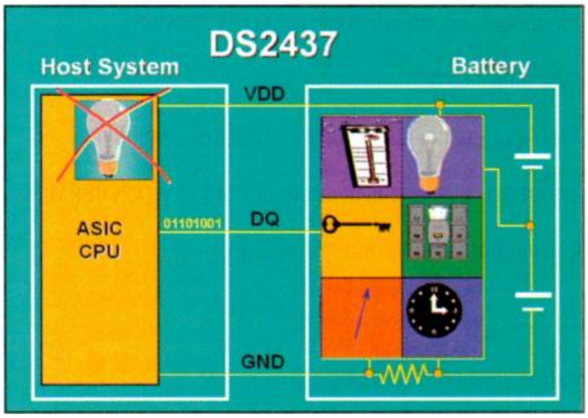

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Computers That Recycle Themselves? Maybe In The Future, With "Shape-Memory" Materials

If Joseph Chiodo, a researcher at Brunel University, Surrey, England, has his way, he'll give new meaning to the computer term, "disassembler." Instead of devising a program that renders raw binary code into human-readable format, he's working on technologies that may give your next computer the ability to take itself apart. This experimental "self-disassembling" technology may greatly increase the cost-effectiveness of electronics recycling programs.

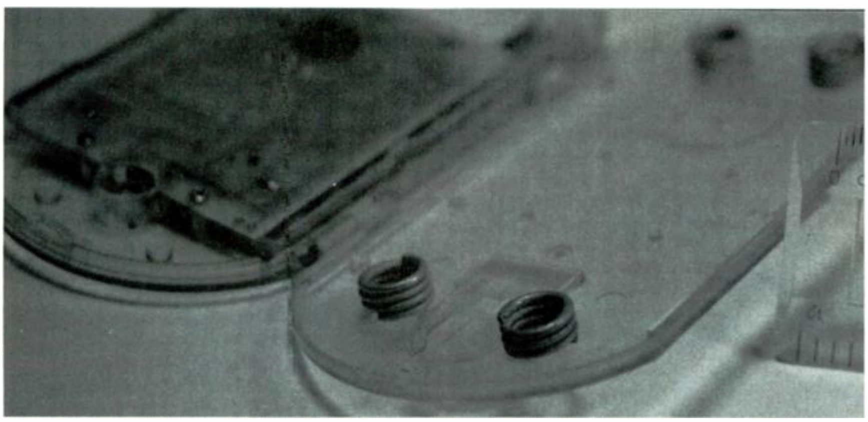
Chiodo has pioneered the development of industrial-grade fasteners that loosen their grip at specific elevated temperatures. These fasteners can now be used to allow complex electronic products to be quickly rendered into their component parts. This may solve one of the thorniest obstacles to the mass recycling of electronic products—the huge cost of labor required for disassembly. Until now, the high cost of disassembly has meant that many products containing valuable components have had to be dropped in a landfill or, at best, shredded for recovery of raw materials.

Using Memory Materials

To solve this problem, Brunel's Cleaner Electronics Research group has focused on exploiting the characteristics of a unique class of alloys and polymers, called "shape-memory materials." Originally developed as early as the 1940s, memory metal alloys are typically composed of nickel and titanium (NiTi), or a combination of copper, zinc, and aluminum (CuZnAl). Parts made from shape-memory alloys (SMAs) can be bent, twisted, or squeezed and made to retain their new shape using a combination of mechanical and thermal "training." The training process involves heating the deformed part to a bit over 400°C, and quickly cooling it in a water bath, thus freezing the material's crystalline structure in a new position. Due to the energetics of the crystal structure, the part is unable to resume its original shape unless external heat is applied.

Depending on its composition, the part will resume its original shape at a specific temperature, typically ranging between 60 and 120°C. Once that threshold is passed, memory alloys revert to their original shape very rapidly. According to Chiodo, surface velocities can go well over 1000 miles per hour. The researchers in his team took advantage of this effect by devising a series of clip-style fasteners and a compression spring-based actuator that could be triggered at one of several specific temperatures. Upon heating, the fasteners let go of their associated attach points and the spring actuators push the product's components apart.

The Brunel researchers speculated that SMA fasteners could be used with different release temperatures. A computer, stereo, or other electronic device could be sequentially disassembled by placing it in a thermal chamber, and gradually ramping up the heat. While higher than the usual temperatures encountered during normal operation, 100°C shouldn't harm most electronic and mechanical components. If needed, delicate components like LCDs could have low release temperatures and be removed early in the thermal cycle. During a typical disassembly cycle, the case could separate from the main electronics assemblies. As the temperature rises, board-level assemblies could push their way out of their chassis, and connectors could pop cables off where needed. The end result would be a mountain of parts that could be easily sorted for reclamation.



This calculator has been modified with shape-memory alloy fasteners and springs, which will automatically disassemble the device when heated to around 85°C. Researchers have successfully demonstrated self-disassembly in a variety of common electronic products, including computers, monitors, telephones, cameras, and cell phones.

Real-World Trials

In a series of trials, the researchers disassembled a variety of consumer products and replaced the original fasteners with the SMA components. These included a pair of keyboards, a 17-in. monitor, two computer mice, several calculators, cell phones, and a pair of small cameras *(See the figure)*. Once reassembled, the products were run through a stepped temperature cycle that was designed to release the fasteners and actuators in sequence.

Early tests and their somewhat disastrous results taught the team much about proper selection and location of the SMA components. More recent tests have proven that the sequential disassembly of complex products is feasible. All that's required is a carefully controlled thermal environment.

Since no manual labor is required except for sorting out components at the end, self-disassembling electronics could be much more cost-effective to recycle. Until now, the labor required to take apart products for recycling made it only cost-effective to recover high-value items, such as computers and copiers. The other problem for recovering value from consumer goods is that they get returned at random, leaving the recycler with a heterogeneous waste stream.

Chiodo foresees a day when disassembly temperatures are standardized, allowing recyclers to easily handle mixed batches of appliances.

A Bright Future

In his ideal scenario, a chamber full of scrap electronics would be heated to the point where all outer cases would release at a specific temperature, followed by the next layer of components, etc. He even speculates that valuable integrated circuits could be easily recovered from their circuit boards if they were mounted in self-extracting, SMA-actuated sockets. While memory metals are just beginning to catch the interest of the electronics design community, another class of memory materials is just on the horizon. Known as shape-memory polymers, these plastics have been demonstrated to have similar properties to their metallic cousins. These plastic fasteners cannot apply force, but can retain and release screws, tabs, and other fasteners just as well as alloy-based mechanisms. If successfully developed, memory polymer fasteners would be incorporated directly into a product's case at a similar or even lower cost than today's assembly techniques.

An added advantage of these nonmetallic mechanisms is that they can be formulated to be recycled along with the other plastic parts. Because of their ready compatibility, several manufacturers are already investigating the possibility of using memory polymers in their existing product designs. In many cases, the same molds can be used, with little or no alteration, to produce self-disassembling products.

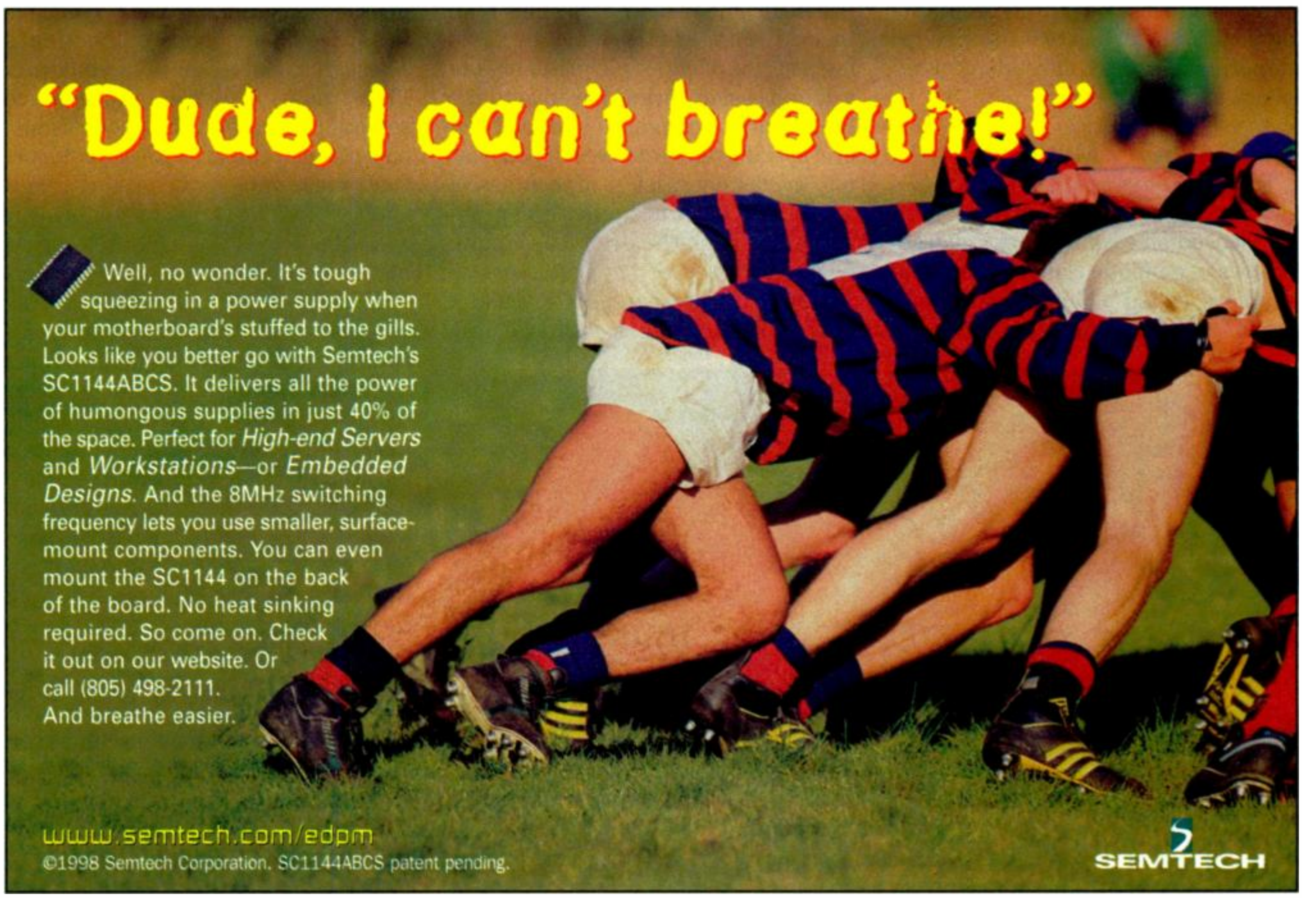
For further information, contact Joseph Chiodo, Cleaner Electronics Research, Brunel University, Runnymeade Campus, Egham, Surrey, TW20 OJZ, England; +44 (0)1784-431 341 ext. 238; fax +44 (0)1784-472 879; e-mail: joseph.chiodo@brunel.ac.uk.

Lee Goldberg

Work On Ballistic Conductance In Carbon Nanotubes May Bring Smaller Electronics

A team of scientists from the Georgia Institute of Technology recently observed *ballistic conductance*. This effect, which was observed in carbon nanotubes up to 5 µm long, occurs when electrons pass through a conductor without heating it.

According to Walter de Heer, a professor in Georgia Tech's School of Physics, this is the first time ballistic conductance has been seen at any temperature in a three-dimensional system of this scale. He believes this development would be of interest to those involved in ultra-small-scale electronics. The phenomena shows that it is possible to constrain current flows to nar-

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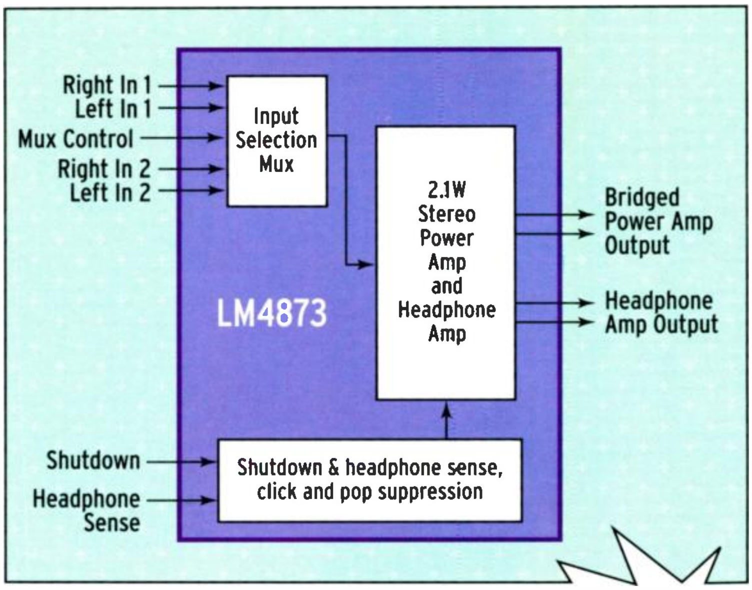

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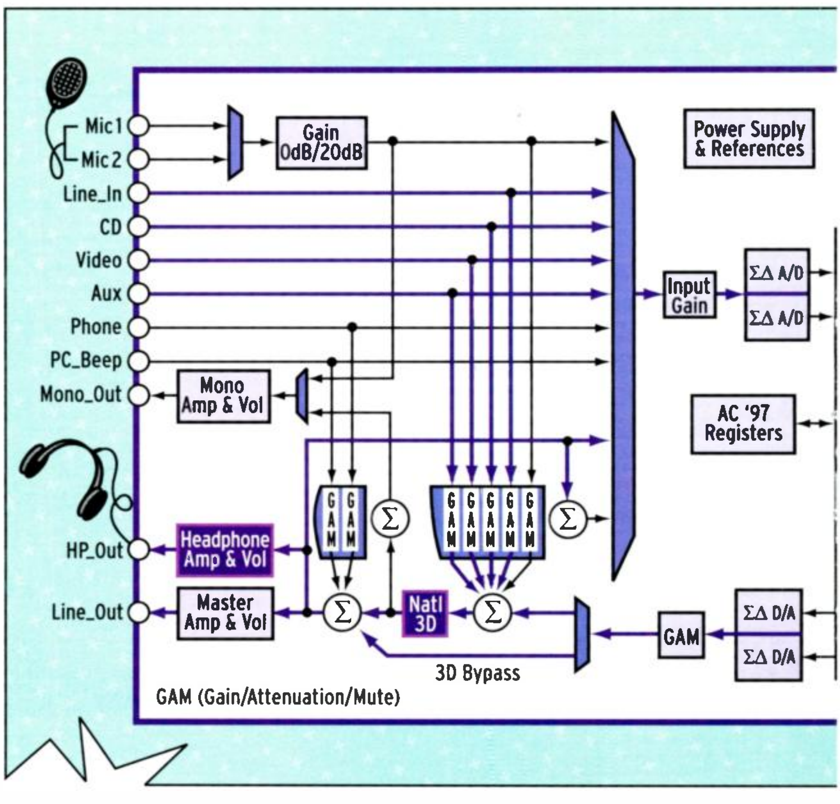

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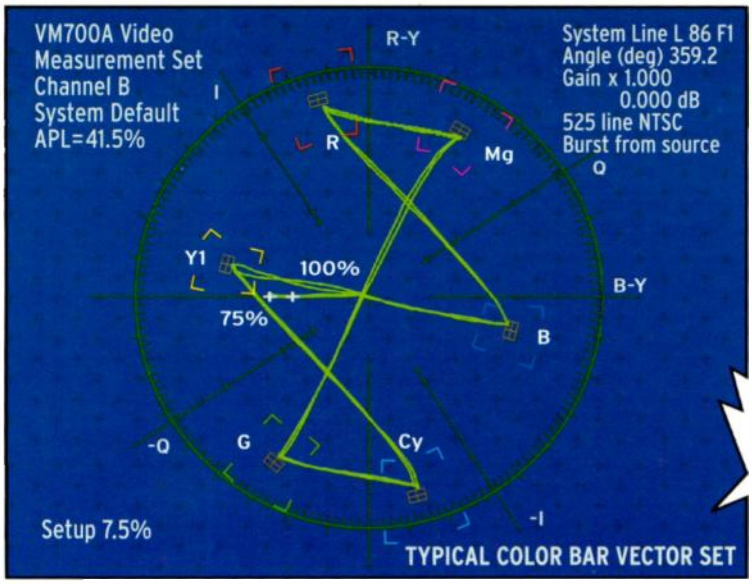
A/D CONVERTERS

3V 8-BIT VIDEO/IMAGING A/D CONVERTER



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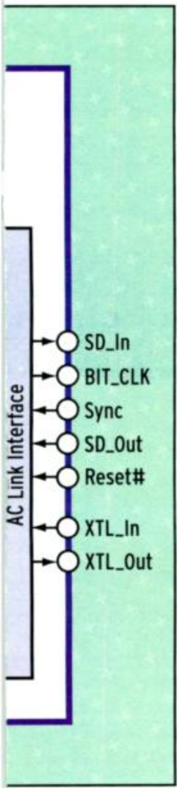

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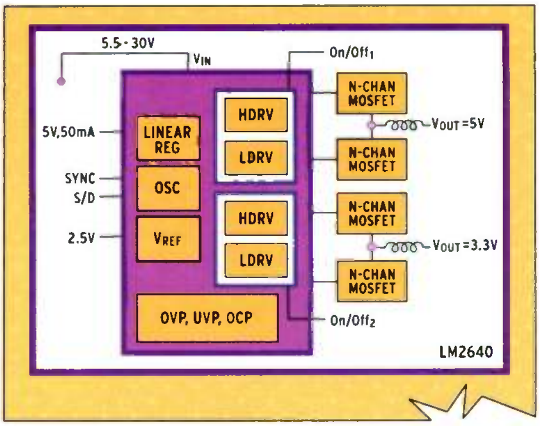

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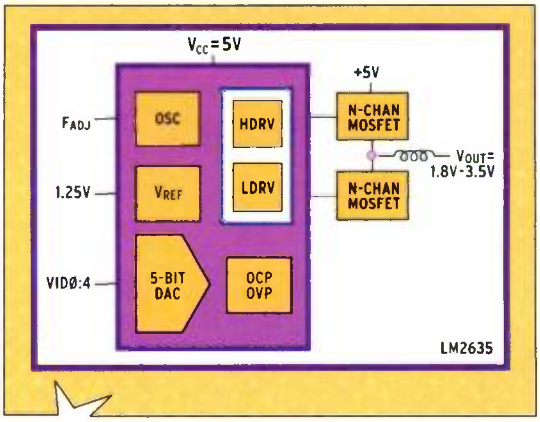
- Ultra-thin 28-ld TSSOP package

5-Bit Programmable Synchronous Buck Controller LM2635

Our new LM2635 desktop controller is designed specifically for use in synchronous DC/DC buck converters for Cyrix® M II®, Pentium II® and AMD® K2™ microprocessors. It comes with all Intel VRM-specified features, plus built-in ultra-fast comparators for the quickest possible response to large load transients.

- 2% output accuracy over line, load, and temperature variations
- Built-in dual fast-action comparators for fast response to large load transients
- Dynamic output voltage positioning
- Current limit without external sense resistor
- Powergood flag and output enable; over-voltage protection
- Precision 1.25V reference output

STEP-DOWN SYNCHRONOUS CONTROLLER FOR DESKTOPS



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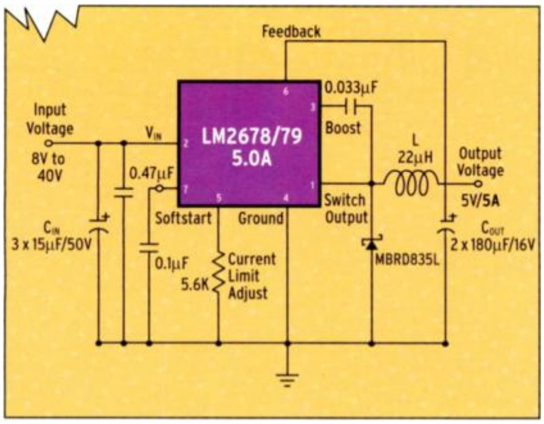
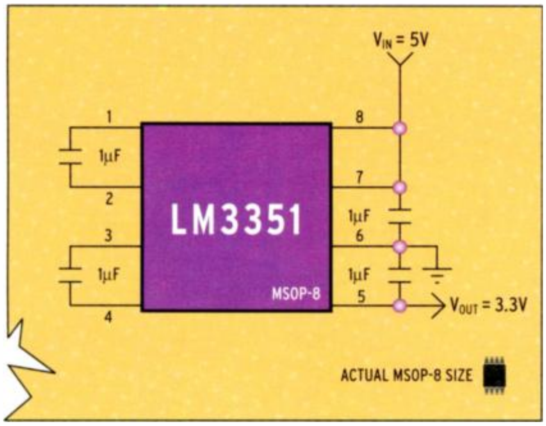
- LED drivers for visual indication of charge status

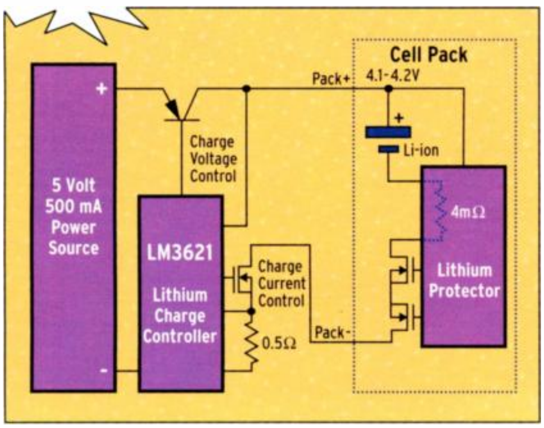
5.0A SIMPLE SWITCHER CONVERTERS



STEP-DOWN CONVERTER MSOP-8 PACKAGE



LITHIUM CHARGE CONTROLLER



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- Iload = 50mA, Ishutdown = 250nA

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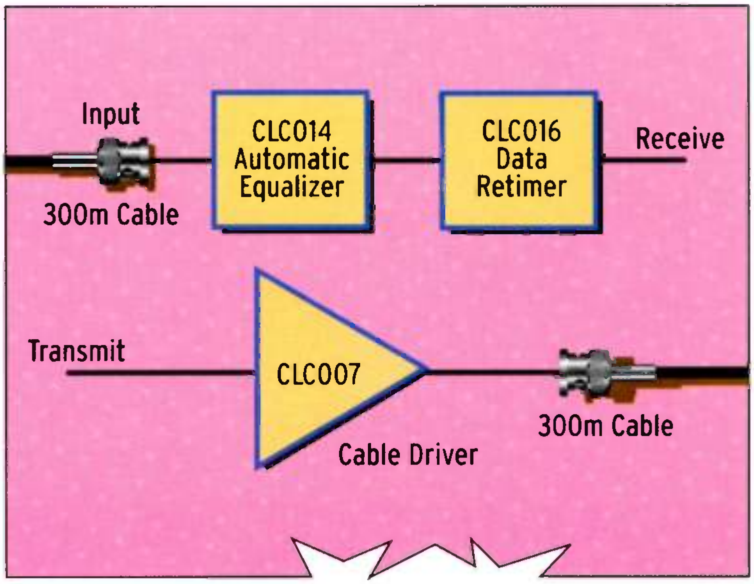
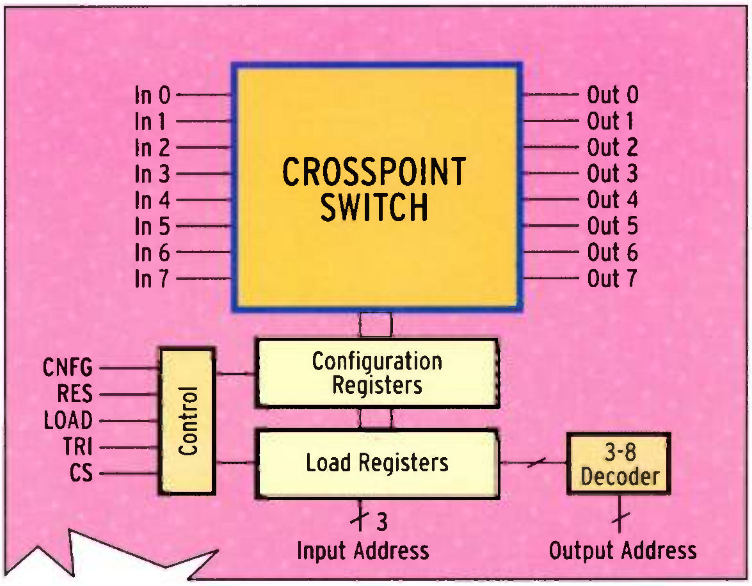
SERIAL DIGITAL INTERFACE CHIP SET



DIGITAL CROSSPOINT SWITCH



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	Single LMV821	Dual LMV822	Quad LMV824
GBW (MHz)	5	5	5
Supply Voltage	2.5-5.0	2.5-5.0	2.5-5.0
I_S (mA)	0.5	0.8	1.12
Slew Rate (V/µs)	2.0	2.0	2.0
R-to-R Output	Yes	Yes	Yes
Packages (shown actual size)	SOT23-5, SC70-5	SOIC-8, MSOP-8	SOIC-14, TSSOP

FAMILY AVAILABLE IN SOT23-5 PACKAGES

	CLC450	CLC451	CLC452	CLC453
Product Type	Amp	PGB*	Amp	PGB*
Bandwidth	100MHz	85MHz	130MHz	110MHz
Supply Current	1.5mA	1.5mA	3mA	3mA
Output Current	100mA	100mA	100mA	100mA
Slew Rate	280V/µs	260V/µs	400V/µs	370V/µs
2nd/3rd Harmonic Distortion 2Vpp @ 1MHz	-79/-75	-66/-75	-78/-85	-65/-84

+5V Performance specifications

*Programmable Gain Buffer (PGB)

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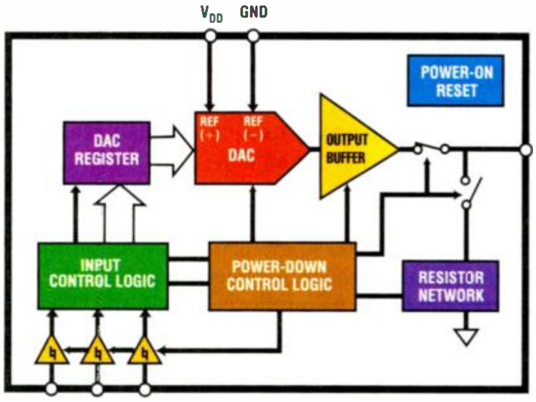

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As more and more portable products come to market, real estate continues to be a major issue.

That's why you'll like the new AD5300 family of pin-compatible 8-, 10- and 12-bit DACs in their SOT-23 packages. The world's smallest rail-to-rail, V_{OUT} DACs, the AD5300 family takes 40% less space than the nearest competitor. Yet as small as they are, they include their own on-chip reference (derived from the power supply) and output amplifier. Plus all the performance you could want. And they're coming soon in dual versions (AD5302/AD5303).

So, if you're working in a shrinking world, take a look at the AD5300 family. And get more performance in less space.

Part #	AD5300	AD5310	AD5320
Resolution (bits)	8	10	12
Package	6-lead SOT-23, 8-lead μSOIC	6-lead SOT-23, 8-lead μSOIC	6-lead SOT-23, 8-lead μSOIC
DNL (LSB)	±0.25	±0.5	±1
Current Consumption (μA)	100	100	100
Power-Down Current (nA)	50	50	50
Settling Time (μs)	4	6	8
Price ($)*	1.25	1.75	2.50

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row areas without heating up the electronics. It also introduces a new stage of electronics in which the wave nature of electrons becomes important.

"The electrons are passing through these nanotubes as if they were light waves passing through an optical waveguide," notes de Heer. "It's more like optics than electronics." The work was reported in the journal, *Science*.

In the absence of heating, extremely large current densities can flow through the nanotubes. Together, de Heer and Z. L. Wang, a professor in Georgia Tech's School of Materials Science and Engineering, measured current densities greater than 10 MA/cm^2. Normal resistance heating would have generated 20,000 K in the nanotubes. This is well beyond their combustion temperature of 700 K.

Wang noted that although these effects were measured only in nanotubes of less than 5 µm, such current densities are far greater than could be handled by any other conductor. At lengths of more than 5 µm, however, de Heer believes electron scattering may defeat the ballistic conductance effect.

In the laboratory, de Heer, Wang, and collaborators Stefan Frank and Philippe Poncaral, attached a tiny electrode to a bundle of nanotubes. A pronounced feature of the bundle was a long tube protruding from one end *(see the figure)*. They mounted the bundle in place of the probe normally used in an atomic force microscope, and connected a battery to the electrode.

They then used the microscope controls to raise and lower the single protruding nanotube into and out of a pool of mercury. The mercury completed the circuit back to the battery. The resistance measured during the raising and lowering procedure remained constant, changing only when a shorter tube protruding from the bundle made contact with the liquid metal.

The researchers measured the resistance of 20 nanotubes of different lengths and diameters through as many as 1000 raising and lowering cycles. Besides mercury, two other molten metals were used, gallium and Cerrolow-117. The tubes averaged 15 nm wide and 4 µm long, but ranged from 1 to 5 µm in length, with diameters from 1.4 to 50 nm. The quantum of resistance remained 12.9 kΩ.

The researchers hope to follow up their work with measurements of other predicted device properties of the nanotubes. The research is sponsored by the U. S. Army Research Office and the Georgia Tech Foundation. For more information, surf the Web at *www.gtri.gatech.edu/rco.html*.

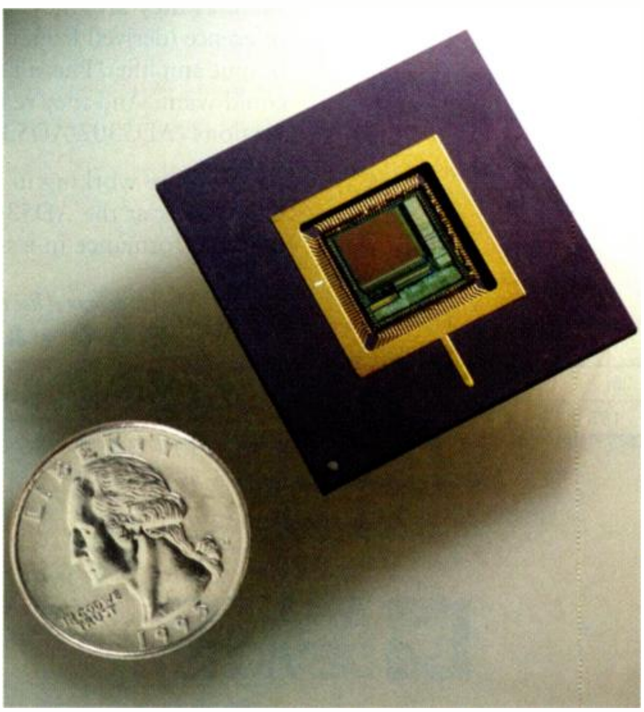
Joseph Desposito

CMOS "Camera-On-A-Chip" Uses Smart Pixels To Deliver High-Quality Digital Video

A recently developed, high-performance "camera-on-a-chip" technology may lead to marble-sized video cameras, ideally suited for PC video conferencing and security applications. The CMOS camera, which occupies a single, quarter-inch silicon chip, produces real-time video images that rival the quality produced by camcorders, which rely on a handful of more expensive and power-hungry mixed-signal ICs.

Traditionally, video cameras rely on a specialized charge-coupled-device (CCD) imaging technology. But the CCD manufacturing process is not well suited for making the different types of transistors necessary for the various non-image-capturing functions. So, the cameras required several chips.

The new technology, developed by Lucent Technologies' Bell Labs, Murray Hill, N.J., employs an imaging array comprising more than 100,000 optical sensors (or pixels) laid out in a two-dimensional grid on the silicon's surface *(see the figure)*. Each pixel generates a small packet of charge when illuminated by an image. Individual pixels are accessed using a two-dimensional arrangement of address and data buses, which is similar to how semiconductor memories are accessed. A small amplifier at each pixel helps reduce internal noise and distortion levels.



A new CMOS-based video camera technology uses more than 100,000 optical sensors plus noise- and distortion-reduction techniques to create a complete "camera-on-a-chip."

"Although the 'active pixel' approach was first proposed back in the early '70s, it's only been in the last few years that technology has progressed enough to where transistors can be included in each pixel without significantly increasing the size of the array," says Marc Loinaz, a researcher at Bell Labs.

Even with this change, however, CMOS-based cameras have been plagued by a defect known as "fixed-pattern noise." This is an annoying, stationary background pattern in the image that results from small differences in the behavior of the individual pixel amplifiers. Although some researchers believed this defect would prevent CMOS from ever seriously challenging CCDs, the Bell Labs team developed circuits outside the sensor array that detect and cancel this noise.

By developing a high-quality imaging array using conventional CMOS technology, the researchers integrated all of the functions normally associated with a camera—timing and control, analog-to-digital conversion, and the signal processing required to provide exposure control and color balance—onto one silicon chip.

The key to the CMOS camera's high performance is how Bell Labs' researchers improved upon state-of-the-art active pixel. The one-chip camera technology has been recently licensed to Vanguard International Semiconductor Corp., Hsinchu, Taiwan, an arrangement that will make it possible for third-party camera and computer peripheral manufacturers to package the camera chips with a small lens. The resulting camera eventually will sell for less than $50, according to Vanguard officials.

Besides requiring less space, CMOS cameras use less power than CCD cameras. A 9-V battery, for instance, powers a CMOS camera for 5 hours, but powers one of today's computer-based desktop cameras for only 30 min. As a result, CMOS cameras are well suited for handheld or security cameras. This could also make video conferencing a low-cost standard feature for future computing products — both laptop and desktop.

Another major advantage of the new CMOS camera is that it allows users to immediately access specific portions of an image. With today's video cameras, users first must produce the entire image before manipulating it. Immediate access to full-frame images could prove valuable to intelligent vehicle systems and other real-time machine vision applications.

Although the new technology initially will be used for computer and security cameras, future uses might include three-dimensional imaging and collision avoidance, like cameras detecting other vehicles in a car's blind spot. The camera also might become integrated into computer screens.

For further information, you can go check out Lucent Technologies' web site at: www.lucent.com. Additonal information is provided at Vanguard Semiconductor's home page. You can visit it at: www.vis.com.tw.

Lee Goldberg

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Full-System Verification Comes To The Masses

Automated Solution Boasts Stimulus Generation, Dynamic-Coverage Feedback, And Distributed Simulation Capabilities.

Cheryl Ajluni

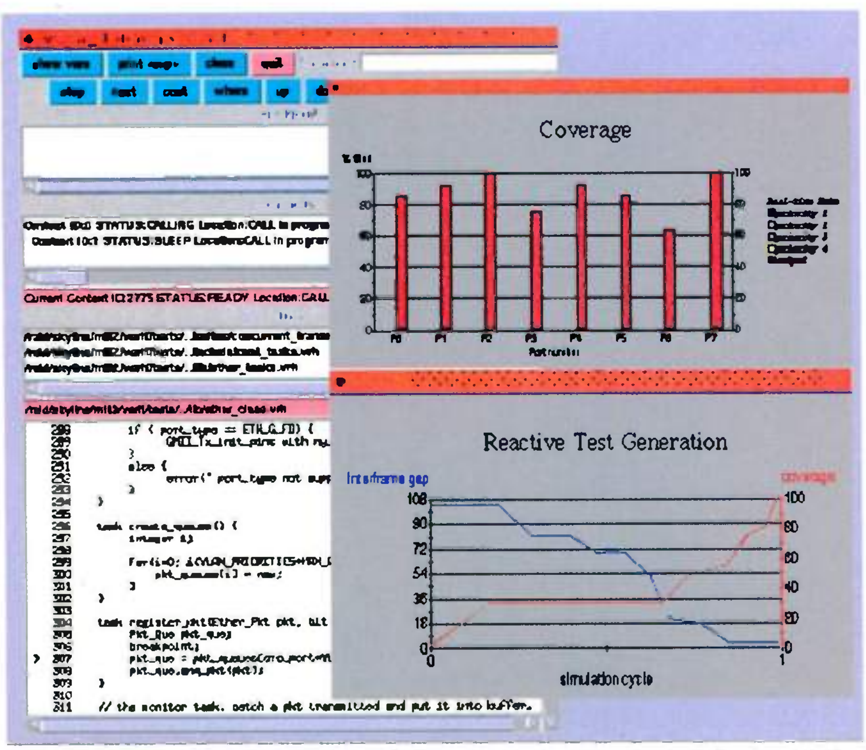
It's tough enough trying to design systems-on-a-chip without the bottleneck that comes from the added software content. But, as the software increases, a large amount of design time must be spent writing test benches, trying to understand what's going on inside the simulator to make sure any potential failures have been caught, and debugging those failures. As anyone who has ever been faced with these tasks knows, they are anything but easy.

The challenge is to accomplish these tasks quickly and effortlessly so more time can be spent in the design-exploration stage. But this requires a shift away from the traditionally separate, serial hardware and software verification processes, toward hardware/software coverification. The results are that software applications can run with hardware to properly verify a design, and subtle hardware/software interactions can be controlled and synchronized early in the design cycle, eliminating back-end integration issues. But where can you find such a tool?

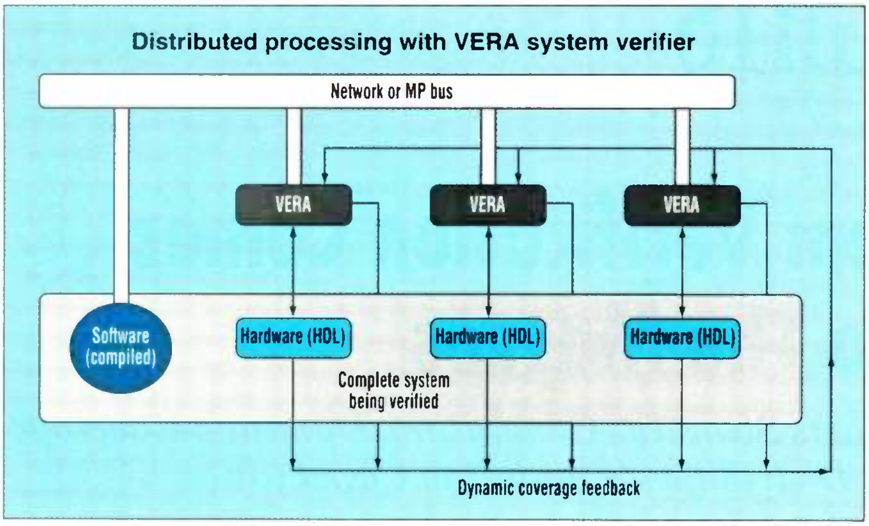
System Science, Palo Alto, Calif., may now have an answer in a mainstream automated solution. Targeted at system developers, the VERA System Verifier (VERA-SV) tool specifically addresses the traditional absence of software in the verification process until prototype hardware has been built *(Fig. 1)*. It allows introduction of software at the same time as hardware, so that both hardware and software verification and debugging can take place concurrently. This occurs long before the first physical prototype is ever built, and results in a significant time savings and improved overall design quality.

VERA-SV is based on the company's VERA-HVL (Hardware Verification Language). It features a number of capabilities in module form, including coverification, automatic stimulus generation, dynamic coverage feedback, data agents, and distributed simulation.

To use the tool, the user first writes a VERA-HVL program to test the design. VERA-SV takes this program as input, and automatically generates functional tests. These self-checking tests mimic the design's target environment, and allow VERA-SV to act as an automated virtual prototype, complete with all the software including device drivers and application code. The user then runs the simulator. At the same time, VERA-SV monitors coverage points in the design, and outputs a test failure report. Coverage results are then checked to verify whether the coverage was adequate. If not, the user writes another test program, and VERA-SV dynami-



1. The VERA-SV full-system verification tool allows systems designers to verify hardware and software concurrently, prior to first prototype.



2. One innovation of the VERA-SV tool is its use of multiprocessing technology to distribute the verification task over multiple platforms. This effectively allows the tool to handle larger, more complex designs, and to complete the verification task in a drastically reduced period of time.

cally generates new tests to cover untested areas. This iterative process is repeated until the user reaches a point where coverage is acceptable.

The new tool can execute software directly on a host machine at full speed. This means that the traffic between hardware and software can be minimized. And, as a result, the simulation process speeds up. By comparison, other commercially available hardware/software coverification products require special models for the processors. This forces the software content to be interpreted by the processor model. VERA-SV does not require any models for the processor.

VERA-SV's closed-loop verification approach offers a complete solution; from automatic test generation to coupling and synchronization of the hardware, software, and testbenches. It enables full system verification.

VERA-SV Modules

The VERA hardware/software coverification module allows engineers to run their software drivers, diagnostics, and/or applications at full speed, compiled on a workstation or PC, and interacting with the hardware. Hardware can be modeled in either Verilog or VHDL. The user has complete flexibility to connect the lowest-level software I/O with the hardware model pins, and to control synchronization granularity.

This module also enables the verification team to design and optimize test benches while the system is still being designed. This is possible because func-

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68HC705C9A	16K	352	31	40-DIP, 44-PLCC, 44-QFP
68HC705J1A	1.2K	64	14	20-DIP, 20-SOIC
68HC705L16	16K	512	39	80-QFP
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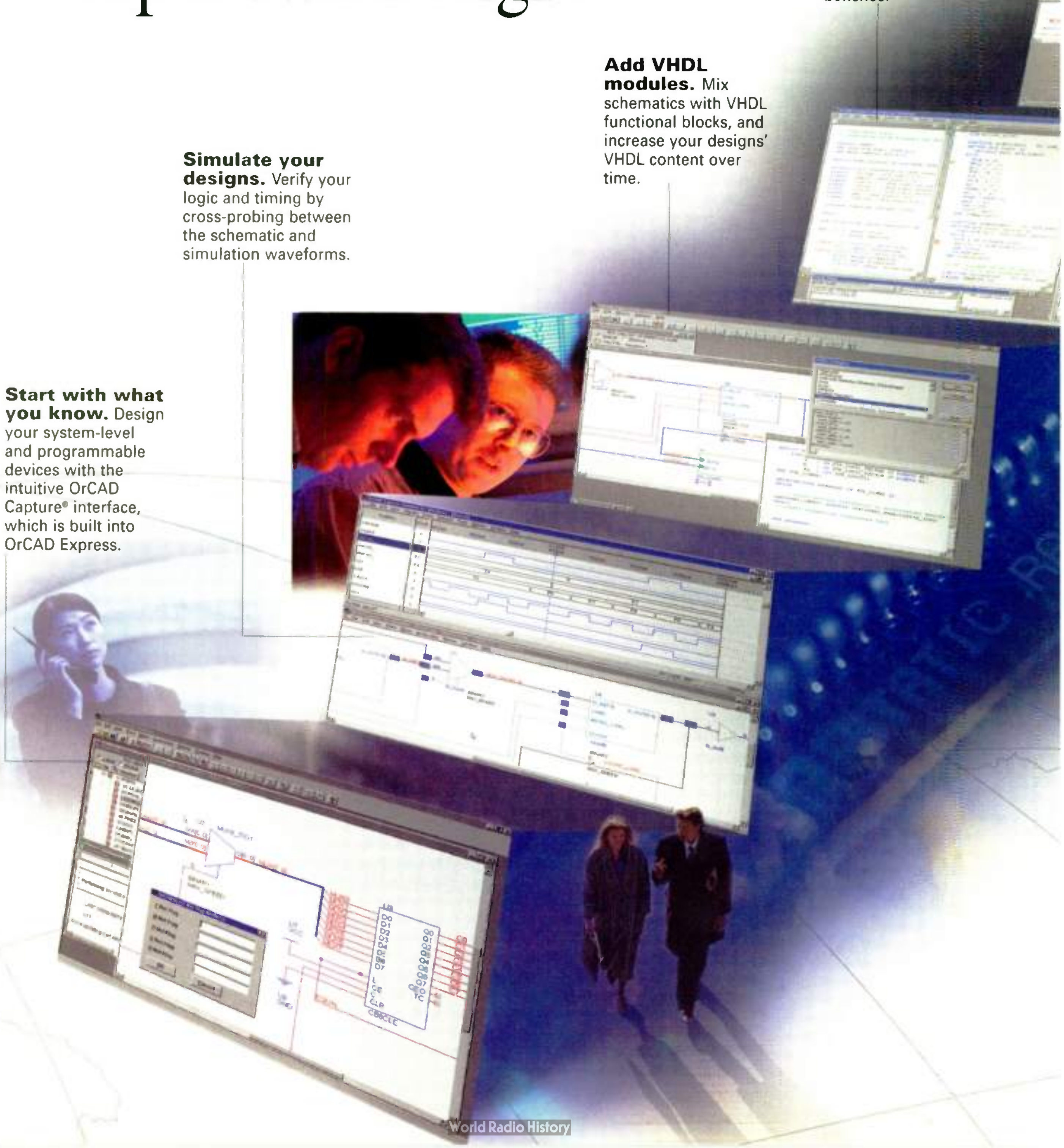

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Design your devices and your system with one application. OrCAD Express is the first design application of its kind. It combines schematic entry, VHDL-based entry and debugging, gate-level and post-route timing verification, synthesis and complete system simulation, all under a single interface. The project management system automatically handles the transition between the chip and board levels at every stage of your project.

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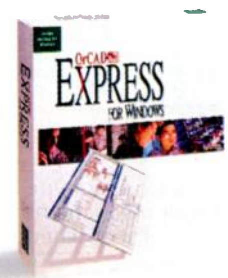
Take your designs to the next level. Many designers have made the transition to VHDL-based design with OrCAD Express, and are using it to create multi-device designs with high-density FPGAs and CPLDs. And so can you. Call to learn more about OrCAD Express — and ask about OrCAD Express CIS™, too. It allows you to access part data from your company's MRP system and the Internet.



For a demo CD and a copy of "Step up to Top-Down Design with OrCAD Express", visit our Web site at www.orcad.com or call OrCAD DIRECT at (800) 671-9506.

EDA for the Windows NT Enterprise

OrCAD

tional coverage of test benches can be performed without doing simulation.

Once the designer writes a VERA-HVL program, the Automatic Stimulus Generation (ASG) module generates stimuli for hardware and software functional verification. It also ensures that the test sequence is correct. In particular, the ASG module can generate random, constrained random, conditional random, and directed functional tests.

The Dynamic Coverage Feedback module allows the engineer to dynamically monitor the testbench generator and/or the design-under-test, and use the information to guide test generation. Besides commonly used, built-in coverage objects, VERA-SV supports user-defined coverage blocks. These blocks may be defined by the user as VERA-HVL or Hardware Description Language (HDL) modules. The user can also specify conditions under which those objects are to be monitored.

Coverage blocks can then be queried during simulation to help the user determine the quality and progress of verification. In that way, the user can steer subsequent stimulus generation toward specific verification goals. Effectively, this means that the user can write test benches to hit certain blocks of a design, performing a search defined by a set of criteria, as opposed to an exhaustive search. The result is that the user is provided with coverage only when it yields meaningful information.

The VERA-SV Data Agents module enables implementation-independent, self-checking tests by allowing verifiers to be associated with a test instead of a chip. Tests can thus be reused on future projects without needing reference models for the chip. An added benefit is that the user does not have to look at simulation results to identify failures. Rather, the user simply examines the test failure report generated by the VERA-SV tool. Because the self-checking tests are written using the VERA-HVL object-oriented programming language, and are verified against the simulator's results, the user is assured that the failure report is accurate.

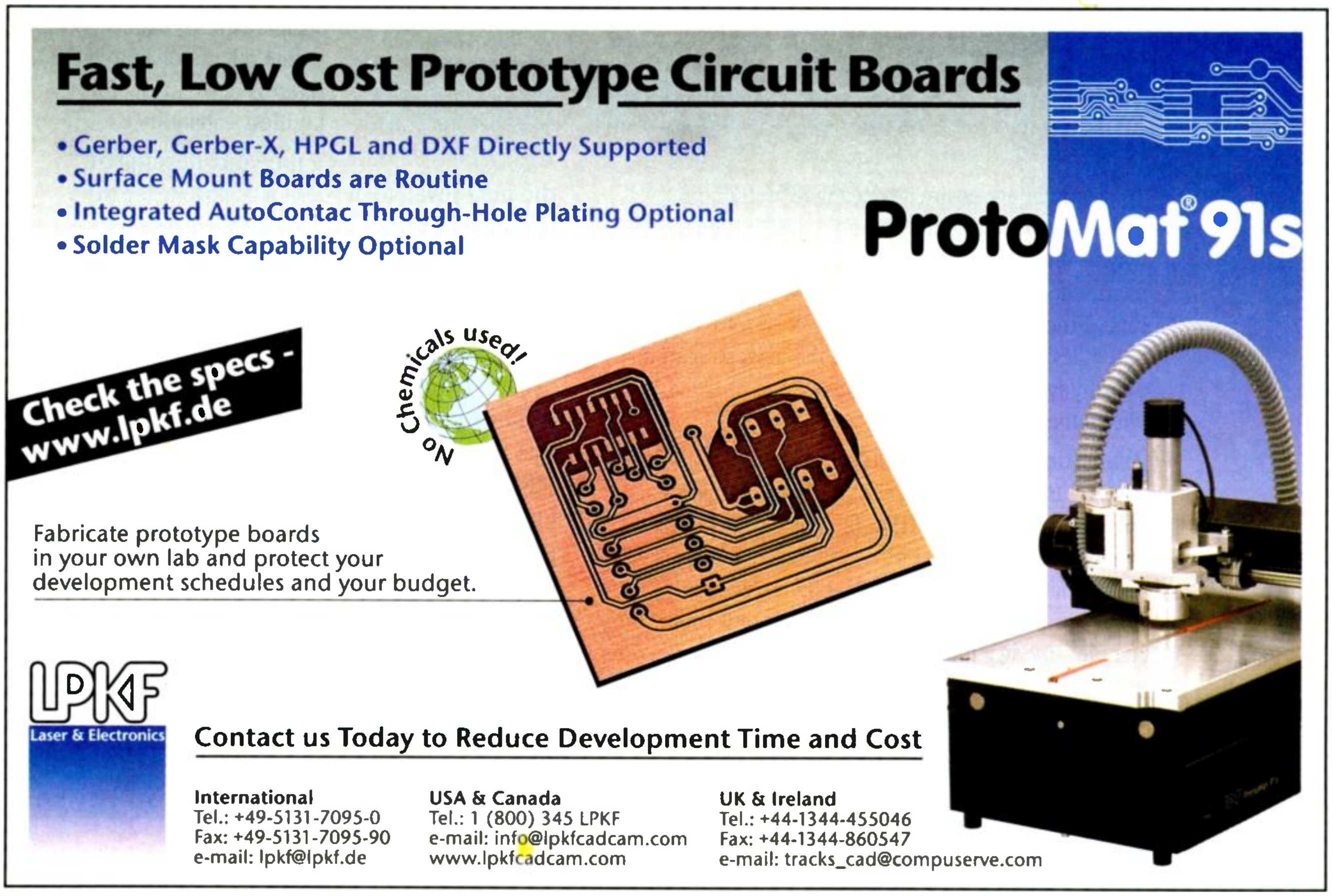
Another feature of the VERA-SV tool is its distributed-simulation capability, which allows VERA-SV programs to be distributed across multiple CPUs, including networks *(Fig. 2)*. Because the verification task can be partitioned into several independent tests, VERA-SV is able to handle very large designs. These tests are executed concurrently across multiple processors, and the end results summed together. Because software and HDL simulation are executed on different processors in a multiprocessor or a network, the hardware/software coverification process runs significantly faster than if it were run on a single processor.

Price And Availability

VERA-SV is now available with support for both Verilog and VHDL. It is priced anywhere from $9500 to $32,500, depending on the configuration. It runs on a variety of platforms including Sun, HP, Unix, and Windows NT. The VERA-SV tool replaces the company's VERA product, and is considered a free upgrade for existing VERA customers on the maintenance plan. Future releases of the VERA-SV product will address the intellectual-property (IP) verification issue.

System Science Corp., 1860 Embarcadero Rd., Suite 210, Palo Alto, CA 94303; (650) 812-1800, info@systems.com, www.systems.com.

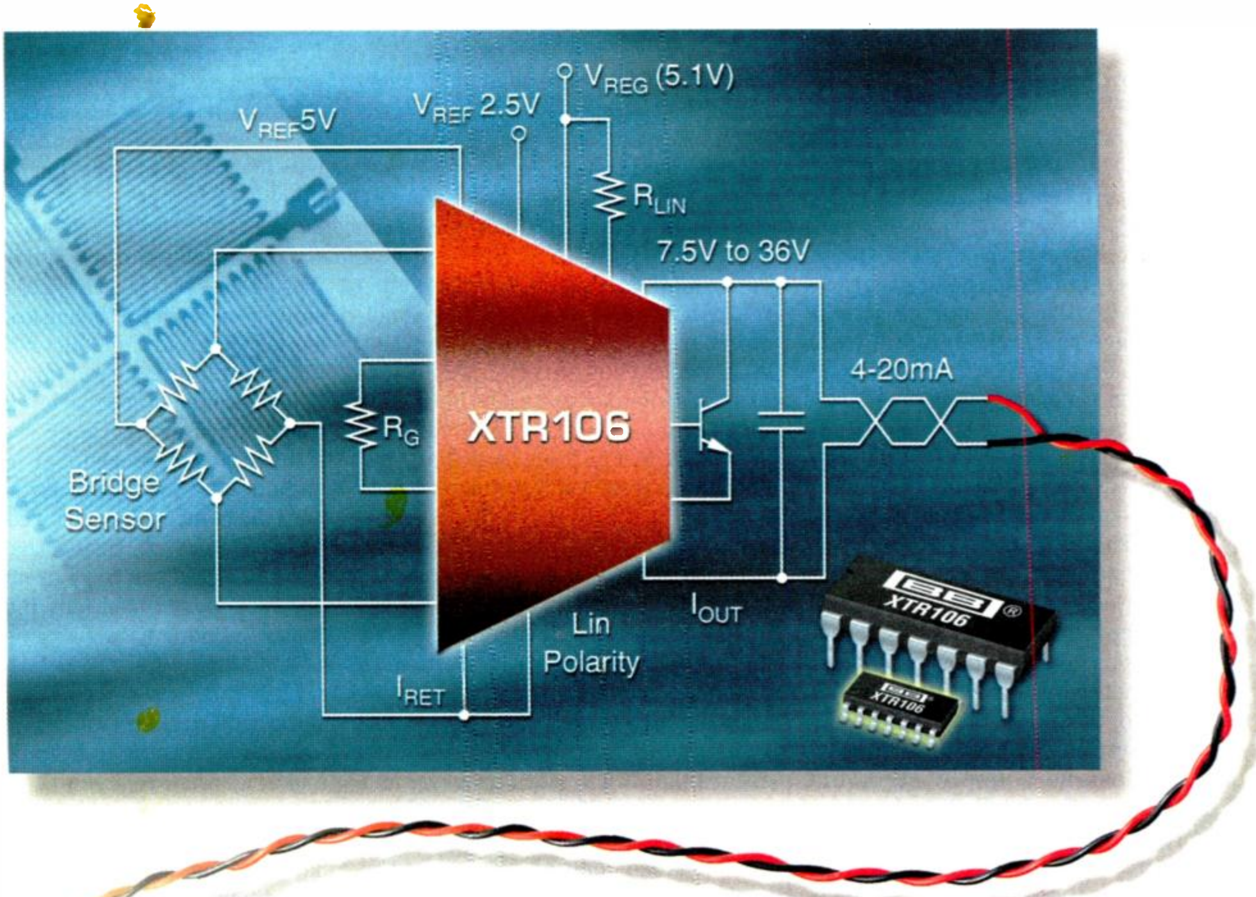
CIRCLE 489



READER SERVICE 121

Precision PLUS™

4-20mA Transmitter ICs



Low Cost, One-Chip Solutions

The **XTR105** and **XTR106** are third-generation 4-20mA current-loop transmitter ICs with precision input circuitry, current-loop output circuitry and sensor excitation all on a single chip. Their low-drift instrumentation amplifier input stage beats bulky discrete op amp circuits.

Sensor Excitation and Linearization

XTR105 has two 800μA current sources, ideal for RTD temperature sensor excitation. XTR106 has voltage excitation (2.5V or 5V) for pressure bridge or strain gages. Both products include sensor linearization circuitry.

Power for External Circuits

XTR105 and XTR106 also include a 5.1V regulated output voltage to power additional circuitry—all powered from the loop supply!

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FAX*LINE #*: **XTR106** – 11449 • Reader No. **245**

7.5V min Loop Supply

XTR105 and XTR106 remain accurate with loop supply voltages as low as 7.5V. There's plenty of operating "headroom" for series protection diodes and overvoltage protection. A complete 4-20mA two-wire loop can easily operate from a standard PC supply.

Key Specifications

- Loop Supply Voltage . . . . 7.5 to 36V
- Offset Voltage Drift . . . . 0.4μV/°C
- Sensor Excitation:
  - XTR105 . . . . 2 x 800μA
  - XTR106 . . . . 2.5V or 5V at 2.5mA
  - *Coming Soon — XTR112 . . . . 2 x 250μA*
  - *XTR114 . . . . 2 x 100μA*
- Packages SO-14, DIP-14

XTR105 and XTR106 are priced from $3.75 in 1000s

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EDA WATCH

Needed: System-Level Design Tools For More Structured Design Practices

According to British Aerospace, 80% of a system's ultimate performance is determined during the first 20% of the design cycle. Yet, there's still a lack of structured design processes exercised early on at the architectural level of the system design. Today's design teams need a methodology that will assure a high level of confidence that a design will work right the first time, before committing significant time, money, and resources to a project.

Ultimately, if more effort goes toward optimizing the hardware and software architectures in the beginning of the design, less time can be spent debugging and rearchitecting the design later to get it to work. For this to happen, design teams must take the responsibility for managing a disciplined methodology from the very beginning of the design process.

Unfortunately though, while today's designers apply stringent processes at the detailed implementation phase of their designs, many still rely on ad hoc, back-of-the-envelope calculations to make architectural decisions. Some designers perform spreadsheet analysis or create C language models for the purpose of making design trade-offs. Such methods are important in making design decisions, but they fail to consider many issues critical to making the necessary trade-offs when selecting the proper hardware and software.

The methodology does not, for example, tell the system architect anything about trade-offs, such as which hardware functions should be implemented in off-the-shelf components, versus which should be used in ASICs. It also fails to take into account which processors or DSPs will perform optimally in the system, and how to partition software algorithms to optimize the hardware/software interaction. And, it often neglects concurrency, making it nearly impossible to visualize potential network contention—which communications devices are necessary to meet performance goals, and how to arbitrate to avoid performance bottlenecks.

Other issues, such as how fast parts of a system must be designed to meet throughput and end-to-end latency requirements, how large each part of the system can be, and how much power is consumed, are often overlooked as well. In the end, many of these decisions are based on "guesstimates." And, while many experienced designers often make good choices, this methodology is often unreliable for such a critical part of the design, and needs to be replaced by a more formal process.

Structure In The Process

Without a structured methodology, design teams often overdesign some parts of the system and underdesign others. To compensate for underdesigned components, many times, designers will overdesign their system to ensure that it will work properly and requirements will be met. Often this is much easier and cheaper than missing performance goals altogether in the system design. But, this brute-force method causes components to cost more than they should. Instead of overdesigning the system, designers should be applying system-level discipline, ensuring that performance goals will be achieved. In the meantime, the cost of the system over its lifetime will be minimized.

Another problem with the current methodology is that designers are forced to spend too much of their time creating and validating hardware and software models. Engineers should be spending the majority of their time focusing on their added value to the system. But, due to a lack of high-level architectural models readily available, they often have no choice.

When creating models at this phase in the design, engineers tend to dive into the details of the models at the start, which detracts from their ability to explore many alternatives. In order to make architectural trade-offs quickly and easily, models must be abstracted to a level where performance is characterized accurately, and where much of the low-level functionality is not designed into the model. At the architectural design level, models must be uninterpreted so that designers can focus on how long it takes to perform a function rather than the result. For example, at the architectural stage, an engineer should be concerned with how long it takes to perform the operation 2 + 2 instead of figuring out that 2 + 2 = 4.

One final problem with today's methodology is the sequence of the design process where the hardware is designed first and then followed by software implementation. Many times, designers face integration problems that could have been addressed earlier if the hardware and software were designed in parallel. It is essential that hardware and software be considered simultaneously to ensure that optimal hardware and software architectures are chosen, and back-end integration issues are minimized.

A Better Way

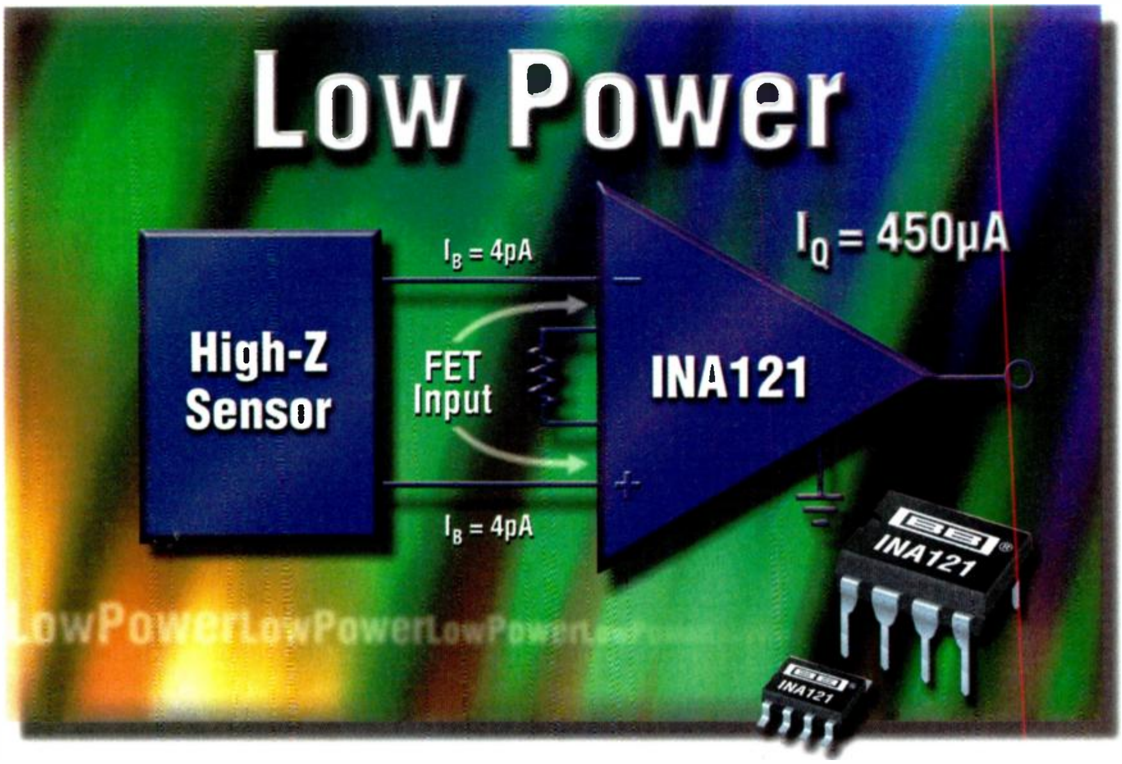
In high demand are new system-level design tools to help designers make rigorous architectural trade-offs. These tools must be able to adequately model both hardware and software behavior so that designers can gain value from their use.

These models need to be more abstract than typical behavioral models so they will simulate quickly and allow for trade-offs. At the same time, they must accurately characterize performance to give designers at least a 90% level of confidence that a design will work. This modeling library should contain abstract models of processors, DSPs, network devices, memories, I/Os, operating systems, and software functions that can easily be plugged together and simulated with minimal time and effort.

Hardware and software architectures must be modeled independently. This way, designers can determine which functions to implement while trying to leverage the development cost of core competency IP (Intellectual Property) that has already been developed. Hardware-independent software models will also allow designers to try different software architectures on the same hardware archi-

PrecisionPLUS™

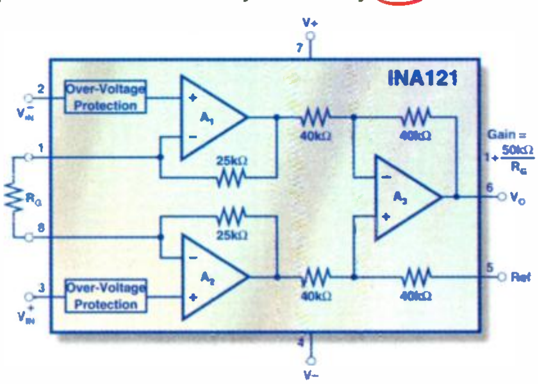
FET Instrumentation Amp



FET-Input for a Low Price!

More than just a precision op amp, the **INA121** is a true 3-op-amp instrumentation amp with FET inputs and precision resistors. With only 4pA input bias current, it's perfect for high impedance sensors, or multiplexed input applications where input bias current can cause errors.

Quiescent current of the INA121 is a mere 450μA and a single external resistor sets the gain from G=1 to G=10000. It makes precision signal acquisition a snap!



Of course the INA121 is input protected. It's completely safe with continuous ±40V on either input, with or without power supplies—robust in the toughest environments.

INA121 comes in SO-8 and 8-pin DIP. And the best of all (surprise)… it's only $2.35 in 1000s.

Key Specifications:

Quiescent Current......................450μA
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Input Protection................. ....±40V
Supply Range................±2.25 to ±18V
Packages...........................SO-8, DIP-8

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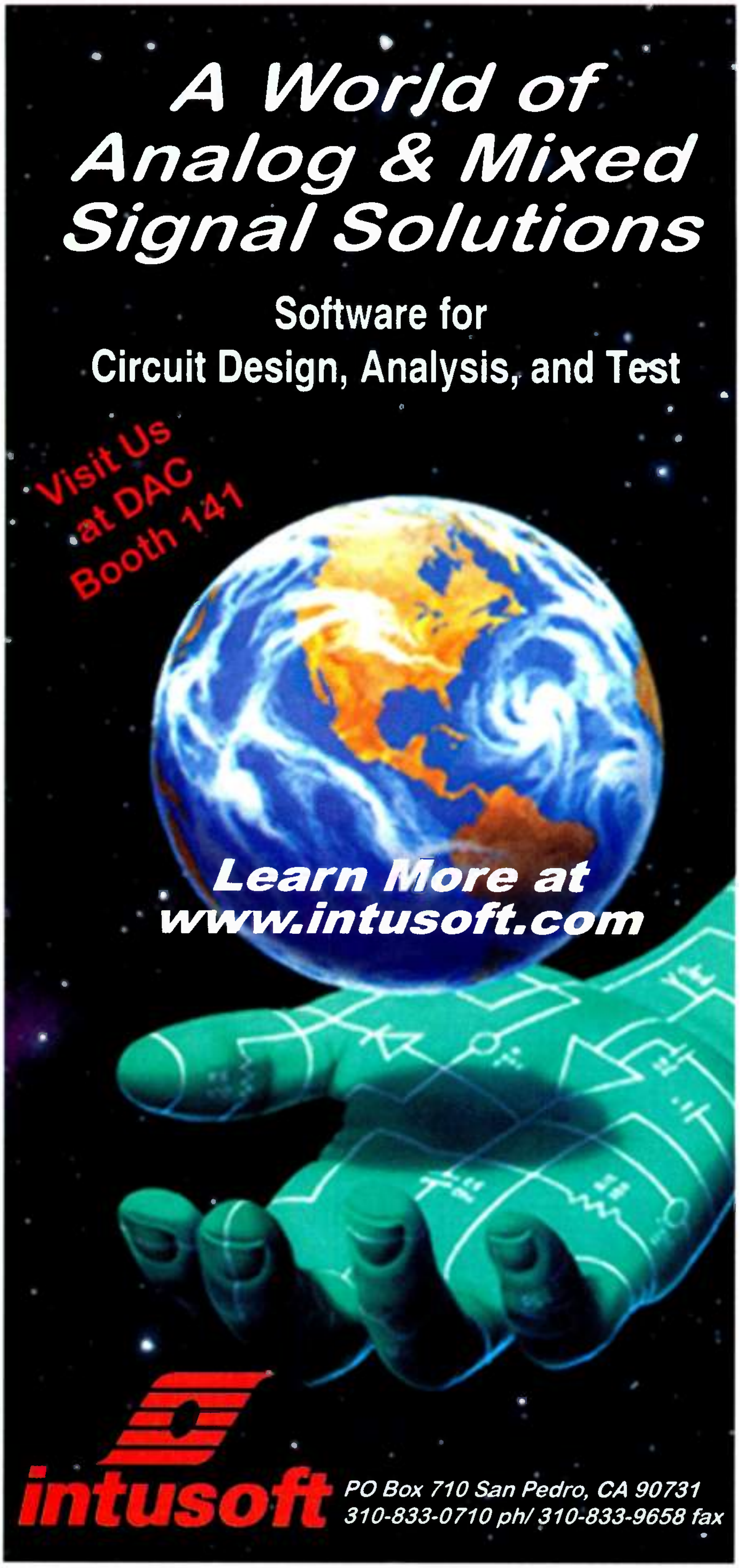

tecture, and vice versa.

Any groups designing systems and systems-on-a-chip will need these new tools. And, to meet this need, a number of companies are now either offering these tools or developing them. Omniview, for example, offers a system-level design tool known as Cosmos that features performance modeling for hardware/software codesign.

A Blurring Role

Ten years ago, the answer to "Who should be responsible for using these tools to define the architecture of the system?" would have been "the system architect." Today, however, the role of the architect and designer is blurring. As the sheer number of off-the-shelf hardware and software components increase, hardware and software engineers can focus more of their attention toward system-level design issues rather than on detailed implementation of these components. As a result, these system-level design tools should find widespread acceptance by most of the new breed of system designers. They include hardware engineers, software engineers, and system architects.

By working closely together from the very beginning of the design process all the way through the detailed implementation, system designers can optimize trade-offs between hardware and software. Using these new system-design tools, design teams can significantly reduce cycles and improve quality by maximizing performance, reducing cost, and achieving first-pass design success. The only way to ensure that significant gains will be realized is to reduce the amount of risk in the beginning and come to assurance as early as possible that a design will work correctly the first time.

Contributed by Ryan Fetter, application engineer for Omniview, Pittsburgh, Pa. Fetter's primary focus is on new design methodologies for performance modeling, hardware/software codesign, and design reuse. He holds a BS in Electrical and Computer Engineering from Carnegie Mellon University. He may be contacted at fetter@omnivw.com. For more information, check out the company's web site at www.omnivw.com.

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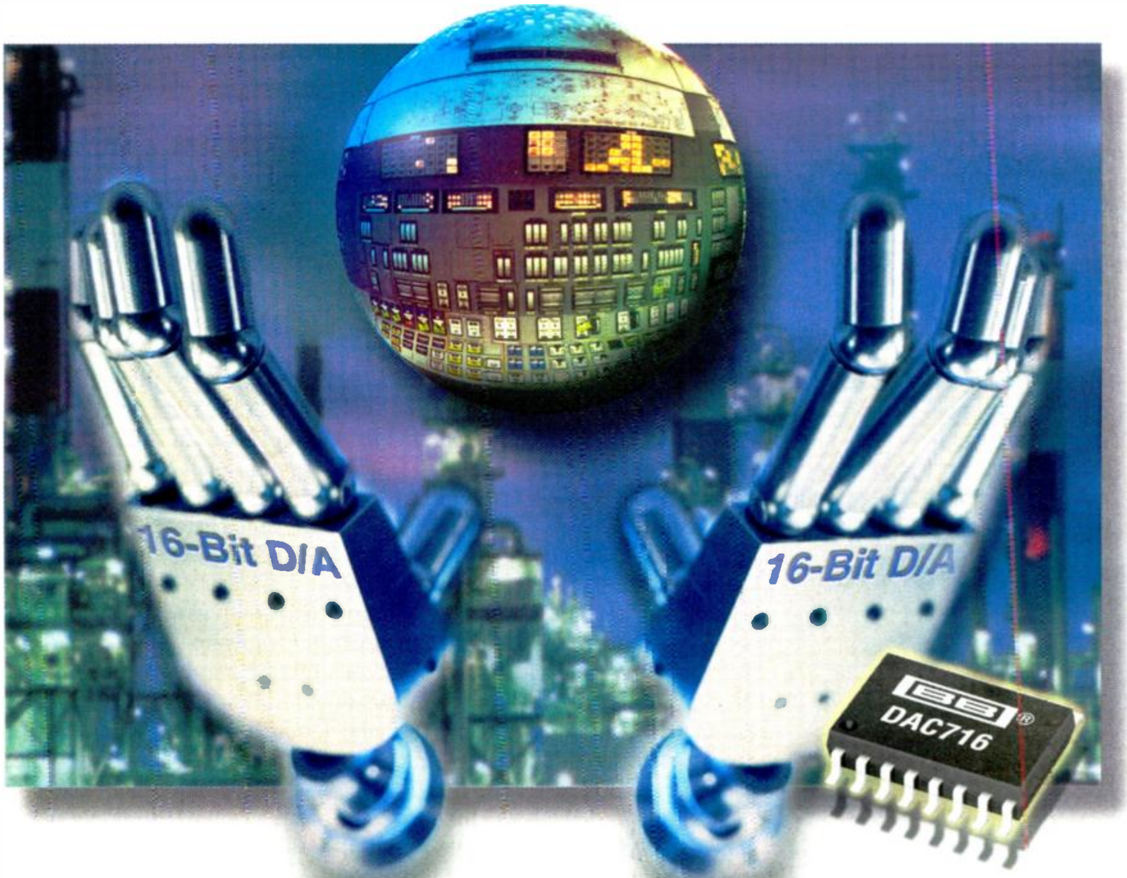

A Monolithic Solution without Compromise!

Burr-Brown's new **DAC716** is a *complete* D/A converter with on-board +10V temperature compensated voltage reference, high speed synchronous interface, and current-to-voltage amplifier—and best of all, there is no sacrifice to performance.

Industrial Process Control

The DAC716 has an asynchronous clear function which immediately sets the output voltage to zero, and a serial output which allows cascading multiple converters—great for robotic, motor speed control, and motion controller applications. Our DAC712 and DAC715 also offer a parallel data interface for applications on high speed buses. The DAC family offers a number of output voltage ranges while operating from ±12V to ±15V supplies.

Applications

For all your control system processing applications—hand off your next design challenge to Burr-Brown and get a grip on your designs.

DAC716 is available in 16-pin 0.3" PDIP and SO-16 packaging.

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DAC712	16	Parallel	±10	±2	16	10	$12.38	11164	136
DAC714	16	Serial	0 to +10, ±5, ±10	±1	16	10	$12.38	11252	137
DAC715	16	Parallel	0 to +10	±2	16	10	$12.38	11306	138
DAC716	16	Serial	0 to +10	±2	15	10	$12.38	11324	139

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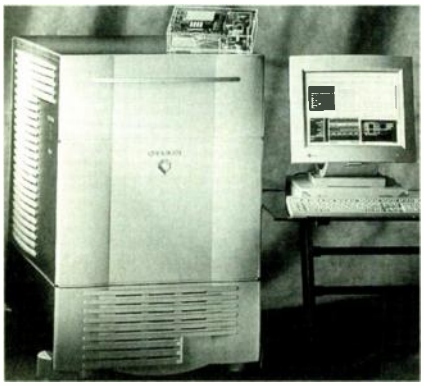
PRODUCT FEATURE

Emulation-Based Tool Offers Regression Testing And Design Verification Capabilities

Design and verification of systems and ICs in a deep-submicron (DSM) era dominated by shrinking design geometries and increased gate counts is anything but easy. A new tool developed by Quickturn Design Systems, called the Mercury Design Verification System, promises to ease the burden by guiding designers through design and verification of complex ICs—from concept to implementation—in a single continuous environment. The benefit is fast overall verification performance.

Mercury incorporates the company's fifth-generation FPGA-based emulation technology and a new mode of operation. With this novel operating



mode, event-driven simulation performance several orders of magnitude faster than previously available technologies is possible. As an emulation-based tool, Mercury can perform regression testing as easily as it can generate reprogrammable physical prototypes, or virtual silicon representations, of electronic circuit designs. Designers thus can concurrently verify entire target systems, including system software and applications, as well as perform iterative design changes prior to actual silicon fabrication.

The Mercury tool is introduced during concept validation. It can accept designs at any level of abstraction, including behavioral, C model, HDL code, RTL, gates, memory, or IP (Intellectual Property). The design then is automatically partitioned between the RISC processor-based SimServer engine and the programmable logic-based engine, and verified to assure that the right design is implemented.

Mercury, a configurable computing technology application, is able to accomplish the verification task quickly. Moreover, because the tool makes use of Quickturn's next generation Q/Bridge technology, it can be easily linked with any other tools a designer might be utilizing.

The tool boasts a number of innovative features, including the SimServer RISC engine, which delivers fast event-driven simulation. It allows accelerated (10-100 kHz) testbench co-simulation and is IEEE 1364-compliant. As an option to Mercury, it provides a platform for hardware/software co-design and for rapidly verifying designs with soft or protected IP models. As a result, Mercury is equally well suited for regression testing, as it is for design verification. SimServer also can perform Verilog behavioral simulation running from 5-15 kHz, and two-state, mixed-level functional simulation running up to 100 kHz.

Mercury's IMPX architecture is based on Quickturn's patented partial crossbar architecture and incorporates high-performance FPGAs optimized for fast design compilation and a custom interconnect chip. Offering support for high capacity in-circuit emulation, it can scale from 500,000 to 10 million gates in capacity and features hundreds of megabytes of memory capacity. An essential component of Mercury, IMPX provides improved utilization of hardware resources and offers the flexibility users need to easily make tradeoffs between design capacity and faster emulation speed.

Mercury's FullVision debug environment provides visibility into all nodes in a design without the need for incremental probe recompilation or having to restart the emulator. Running under the Quest II 98 emulation software, it features an integrated waveform viewer, a new schematic viewer that supports Verilog and EDIF, a new tabular data browser, and an HDL source code browser.

Another feature of Mercury is its support for IP-ready modeling—in the form of IP Tiles or IP-Flexiblox—to help facilitate IP security with partial visibility during the design and verification process. IP Tiles are provided by the core supplier as pre-emulated, pre-verified, pre-routed, and protected emulation databases. They don't require partitioning or internal routing for emulation. Also provided by the core supplier, IP-Flexiblox are binary models that users can mix with their own design netlists prior to partitioning and routing for emulation.

Mercury also supports multi-ASIC support via modular compilation. It compiles IP blocks, design modules, and ASICs separately and links them to create an image of the design for emulation. Engineering change orders (ECOs) are incrementally compiled without affecting unchanged parts of the design.

Another feature of Mercury is its three-level memory support. The tool can support FPGA internal memory, configurable memory chips on emulation boards, and specialized memory boards—with full control and observability of memories—while emulation is running. The tool also allows for automatic partitioning and clustering of memories across multiple chips for highly multi-ported and very wide memories.

The Mercury Verification System is now available and comes with two chassis options. The Mercury SE Series scales from 500,000 gates to two million gates in increments of 500,000 gates. The Mercury E Series scales from 1 million to 10 million gates in increments of 1 million gates.

An entry-level Mercury system is priced at $395,000 U.S. list. The SimServer option starts at $85,000 U.S. list. Mercury Replicants have a base starting price of $245,000 U.S. list for a 500,000-gate capacity, and can be used to support parallel product development and provide multiple team members access to the Mercury Verification System.

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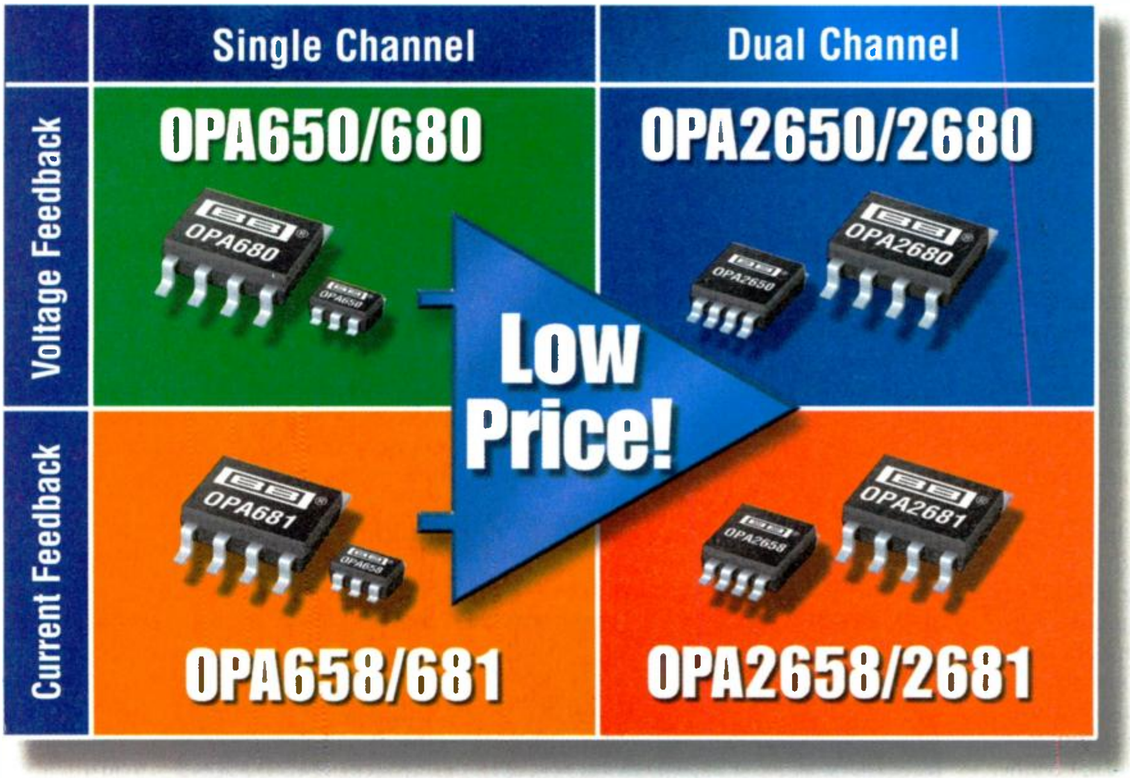

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Pick from two complete product families of high speed Single and Dual, voltage and current feedback op amps. At only 6mA/ch., the **OPA650 family** offers the lowest cost option for ±5V operation while the **OPA680 family** gives the highest performance. Triple and Quad versions are also available.

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OPA650	Single VFB	140	240	±3.0	+110/–85	SOT23-5	$1.29	11264	80
OPA2650	Dual VFB	108	240	±3.0	+110/–85	MSOP-8	$1.95	11266	81
OPA658	Single CFB	680	1700	±2.9	+120/–80	SOT23-5	$1.49	11268	82
OPA2658	Dual CFB	500	1700	±3.0	+120/–80	MSOP-8	$2.39	11269	83

Highest Performance Single +5V Supply Op Amps—Highest Output Power on ±5V—Power Shutdown Included

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OPA680	Single VFB	220	1800	±4.0	+190/–150	SOT23-6	$1.79	11426	84
OPA2680	Dual VFB	220	1800	±4.0	+190/–150	SO-8	$2.89	11433	85
OPA681	Single CFB	220	2100	±4.0	+190/–150	SOT23-6	$1.79	11427	86
OPA2681	Dual CFB	220	2100	±4.0	+190/–150	SO-8	$2.89	11440	87

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ADVANCED LAN PROTOCOLS

Teaching IP New Tricks: VLANs, QoS, And Other Advanced LAN Protocols

There's No Such Thing As Free Bandwidth, But You Can Make It Less Expensive Using Good Design Practices And Emerging Standards To Add Flexiblity And Manageability To Packet Networks.

Lee Goldberg

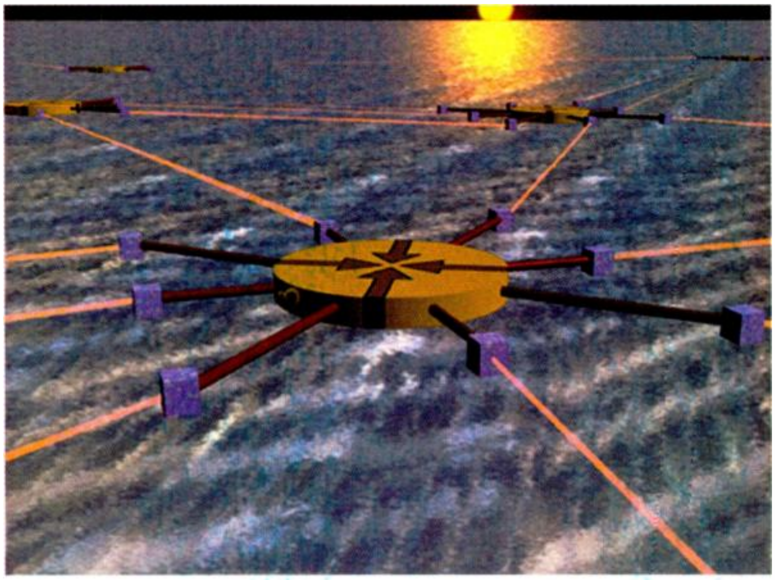
No matter how much bandwidth you give users, they find a way to consume it. Worse yet, they always come back begging for more. With the advent of streaming video, pointcast, and other bandwidth-intensive applications, today's LANs are often running at or near their capacity. Some of the problems are not due to the sheer volume of traffic, but the fact that unless properly managed, packet-based networks tend to squander their bandwidth in inefficient ways. Fortunately, networking IC and equipment designers are now taking advantage of a set of emerging standards to make some order out of the non-deterministic miasma that characterizes Ethernet traffic.

Several important Internet Protocol (IP) standards have been developed to help keep networks from collapsing in overheated heap. These include virtual LAN (VLAN) protocols, preliminary schemes for quality of service (QoS) signaling, as well as basic management policy monitoring and enforcement techniques. Over the past year or so, these functions have evolved from proprietary software protocols to firm networking standards, making it practical for IC designers to implement them in hardware.

Migrating support for VLAN and other protocols to silicon has had the dual effect of driving their cost down, while greatly raising the number of packets they can handle. Now, network product designers are finding that support for these protocols are becoming "must-have" features.

All the new Fast Ethernet switch chip sets, including those from Allayer, Galileo Technology, I-Cube, MMC Networks, PMC-Sierra, Texas Instruments, and Vertex Networks, have some sort of VLAN capability *(Fig.1)*. Most of the players also provide varying levels of support for QoS and policy enforcement-related functions. Before you pick a chip set or ASIC design for your particular application, it's important to understand these protocols a bit better, and how you can use them to provide your networking products with more performance and interoperability.

SPECIAL REPORT

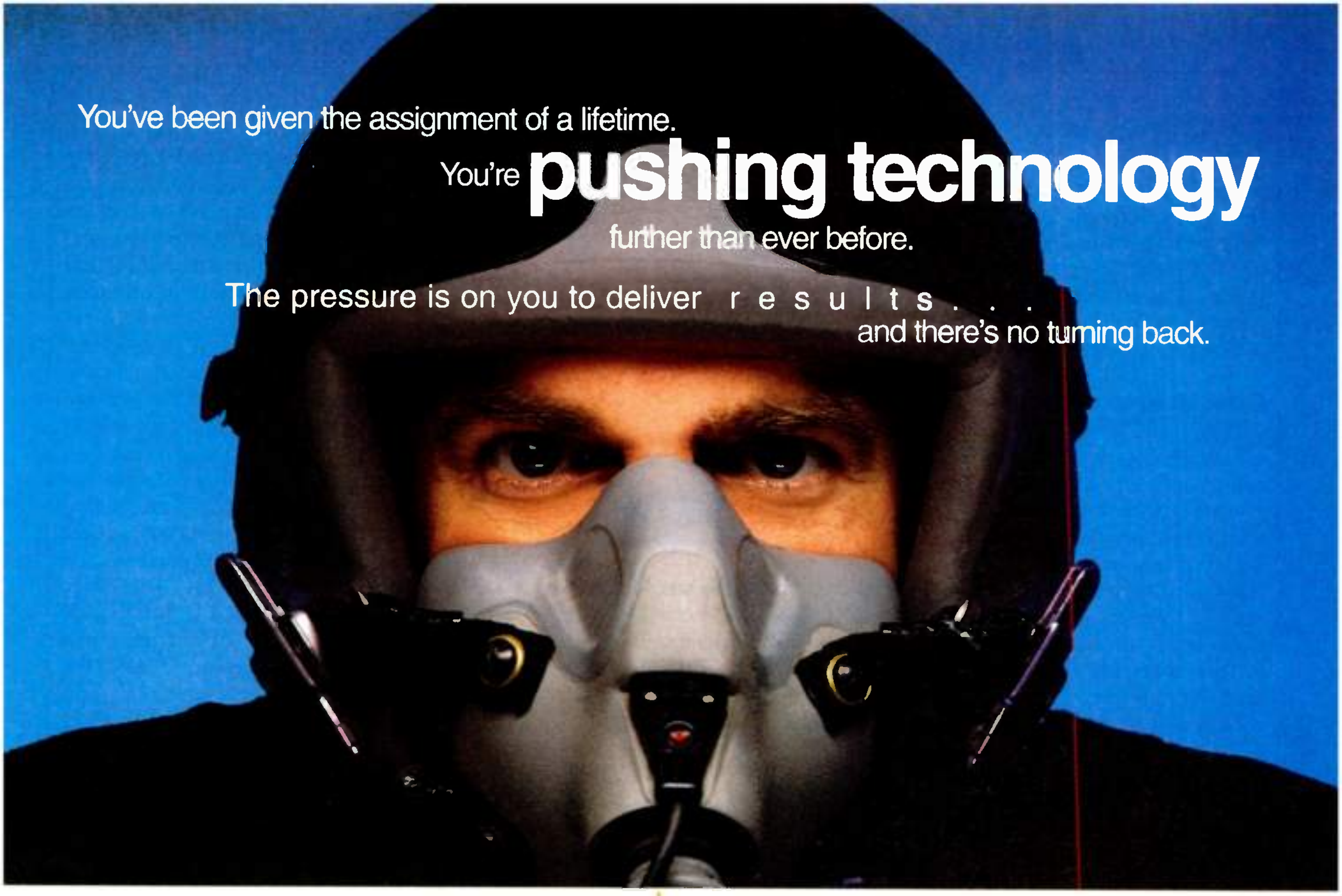


Art Courtesy: Allayer Technologies

Making IP Smarter

These new IP protocols are an attempt to add some level of intelligence to a technology that was originally designed to be rock-simple. The original Ethernet expected all members of the network to share a single 10-Mbit/s wire. Each terminal, PC, or workstation's network interface would see all the IP packets streaming by, and pick out only those it saw that had the proper address tucked away in the header. As traffic levels grew increasingly heavy, using switches gave each network segment their own dedicated pipe, but did not necessarily reduce traffic throughout the backbone. This was because routers were still bombarded with broadcast and multicast messages that they were obliged to pass on, regardless of whether they were needed on a particular port or not.

The other problem users faced with IP-based networks was managing them. This was in good part because standard routing methods use the PHY-layer media-access control (MAC) address to locate a computer, printer, or other device. Besides requiring network elements to maintain large routing tables, reliance on layer-2 MAC addresses makes it hard for LAN managers to reconfigure the network each time equipment is moved around a building or campus.



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Don't let limited technology keep your ideas grounded.

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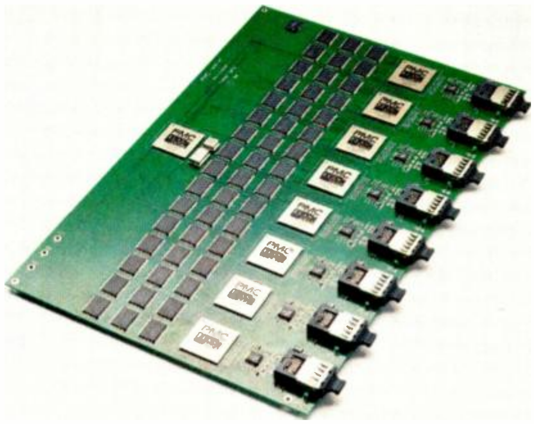
Several years ago, several networking companies realized that they could reduce traffic flows and improve manageability by identifying specific groups of users within a larger system who exchanged the bulk of their files with each other.



1. Highly integrated switch chip sets, like PMC-Sierras' EXACT solution, make it possible to pack a full-featured eight-port (or more) 10/100. Or, in this case, a Gigabit Ethernet switch is jammed onto a single board. The same high levels of integration make adding the hardware processing logic required to support advanced LAN protocols possible, such as VLAN tagging and priority queuing.

Enter VLANs

This would permit members of, say, an engineering or accounting group to establish a "network-within-a-network" which kept their data from being broadcast around the rest of the building at random. By defining these sub-groups, multicast traffic destined for one group can be easily filtered out from other router ports before it adds to network congestion.

In theory, the best way to direct traffic to group users was by keeping track of the MAC addresses associated with each piece of equipment. The manufacturers who used layer-2 MAC-based VLANs discovered that it was difficult to implement because it required a large table and a complex resolution function to map each lengthy address to a particular switch port. Worse yet, the level of complexity quickly swelled to uncomfortable proportions in large multi-switch environments.

Other early VLAN schemes created groups by identifying the router ports associated with a particular work group, and limiting broadcast traffic to those specific ports. Still other routers added tags to packets that identified them as belonging to a particular subnetwork. While these schemes worked well and made it possible for LAN managers to use Layer-3 management tools to configure their networks, their proprietary protocols required that all system elements be supplied by the same vendor. Manufacturers enjoyed good success in establishing ad-hoc groups to develop and implement open VLAN routing protocols, but their efforts were somewhat hampered by typical industry infighting.

The potential advantages of a vendor-independent VLAN protocol soon became apparent, and the IEEE set to work on developing them. By the time you read this, the 802.1Q and 802.3 AC VLAN standards should be close or past the approval process. This new family of VLAN standards are based on a tagging scheme where incoming IP packets get an additional four bytes added to their header just behind the source address. Two of these bytes specify packet type, while two bytes are used for the actual tag. The 16-bit tag contains a 12-bit VLAN ID field, a one-bit canonical format indicator (CFI), and a three-bit field which can indicate one of eight priority levels of the packet *(Fig 2)*.

Almost everybody's happy about this new protocol, but its introduction does not solve all networking problems. One mildly troublesome issue is the oversized packets that tagging generates and the potential problems it may cause with older equipment. Since people tend to upgrade their networks in small increments, the new tagging scheme has been carefully designed to interoperate with older equipment that is not VLAN-aware. Part of the protocol includes a discovery process that allows a switch to identify and build a table of the ports it sees which are connected to VLAN-capable devices and

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those that are not.

A VLAN-capable device must accomplish the following operations to work within the IEEE-sanctioned universe. First, it must perform filtering upon receipt. This means that it drops packets with unfamiliar ID tags that it cannot resolve, and keeps track of how many it has discarded. It must also insert tags on a per-packet basis. It also should strip out tags before shoving them out to VLAN-clueless edge devices or network interface cards (NICs) that can't make sense of the tags. In some cases, this may not happen, resulting in delivery of packets which may be longer than the 1518-byte maximum length for normal IP packets specified by the IEEE.

The VLAN tag was carefully placed within the header to permit non-VLAN devices to read a tagged packet header with only a little difficulty and then locate the beginning of its data field. There is some concern however, about whether older routers and NICs will notice the additional length and drop the packets.

Rich Seifert, networking consultant and president of Networks and Communications, Los Gatos, Calif., says that this problem is overrated. He claims that most modern NICs and port interfaces already have logic and buffer space that can support packets as long as 1536 bytes (12 k hex). For the most part, Seifert says, these cards will simply need new APIs or I/O drivers to help them properly read the longer tagged packet header.

For the most part, NICs and other end stations will not need to look at VLAN tags for the next few years. Extending a VLAN to the desktop does little for performance today, so VLAN domains will typically end at the final switch port and deliver untagged packets to users. One exception however, is servers. There are distinct advantages to extending a VLAN directly to these heavy traffic generators, opening the market for a profitable niche market in VLAN-capable server port cards.

Priority Is A Priority

With superfluous multicast traffic under control, the next task in streamlining network packet flows is to add some sort of QoS mechanism. The two most popular methods involve priority control and traffic policy enforcement.

Priority control assumes that certain types of traffic are more important than others and gives their 3-bit, 802.1Q priority tag field a higher number.

802.1Q assigns priority in the following manner:

- 7. Reserved for future use
- 6. Interactive voice
- 5. Interactive multimedia
- 4. Controlled load applications (such as streaming multimedia)
- 3. Excellent effort (for business-critical applications)
- 2. Standard priority
- 1. Background task
- 0. Best effort (default for untagged packets)

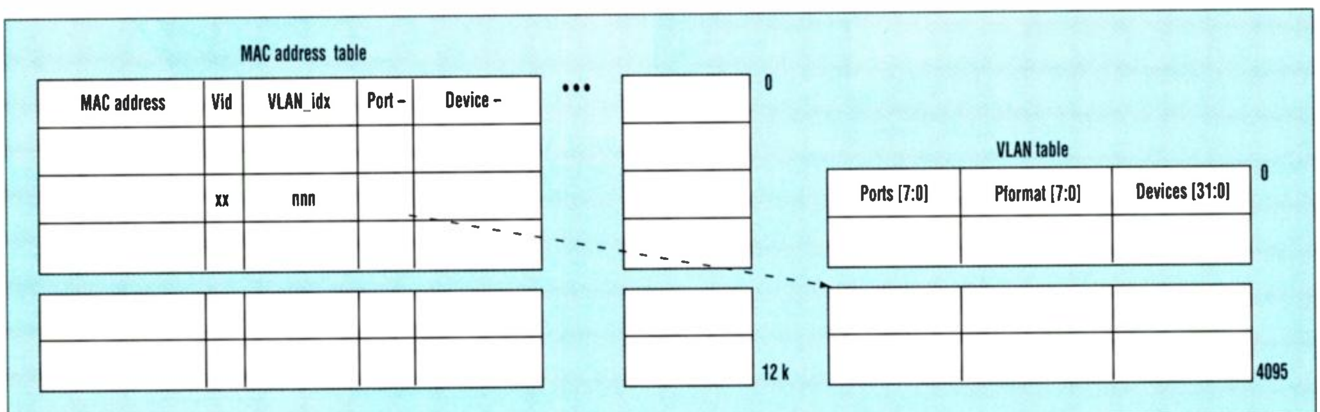
This allows switches to identify packets carrying time-sensitive information and move them through the network ahead of data that could stand a few hundred milliseconds of delay. Traffic from mission-critical applications can also be given first dibs on available bandwidth, allowing lower-priority e-mail and downloads from the Dilbert web site to flow on a space-available basis.

Tim Thompson, director of marketing for Vertex Networks, Irvine, Calif., says that in order to work with existing infrastructures, the 8-level VLAN priority field must be mapped down to lower levels of granularity. He says that most desktop NICs and Layer-2 switches are designed to handle two, or at most four priority levels. Thompson indicates that even most backbone switches have only four levels of priority flow today.

Network hardware should allow mapping to be determined either by a network administrator, although some sort of hardwired decision functions can be implemented for lower-end solutions. A VLAN-capable device must accomplish the following operations to work within the IEEE-sanctioned universe. First, it must perform filtering upon receipt. This means that it drops packets with unfamiliar ID tags that it cannot resolve, and keep track of how many it has discarded. It must also insert tags on a per-packet basis and remove them before sending them on to VLAN-clueless equipment.

Cheaters Don't Prosper

The priority field in the VLAN tag is already being used in some chip sets and equipment. Microsoft's WINSOC II drivers also support prioritization tagging for applications. Vertex's



2. The 802.1Q VLAN tag consists of four bytes inserted into the header after the MAC address. Galileo Technologies' tag-mode switching scheme uses these to build a VLAN table that contains linkages to its MAC address table. An incoming tagged packet is checked against both tables and forwarded to the appropriate port if a match is found. If no MAC address is found, the VLAN ID is used to index into the VLAN table using the VLAN_idx index field. The packet is then broadcasted to all VLAN members as an "unknown" for possible address resolution elsewhere.

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Thompson says that although it is tempting for software designers to enhance their product's performance by "spoofing" the network with a higher-than-deserved priority, new policy enforcement functions allow switches to detect and foil potential bandwidth thieves. Policy management tools, such as Transcend, from 3Com Corp. Santa Clara, Calif., do this by checking on what kind of application is requiring a particular priority. If a particular connection is violating the LAN's management policy, an administrator can remotely command a switch to adjust the flow's tags to the proper level.

Another complicating factor in the quest for true QoS is the fact that the Internet Engineering Task Force is also working on its own prioritization scheme. Known as Type of Service (ToS), it is intended to help untangle some of the traffic snarls found today on the Internet. ToS is still under development, but will most likely define a particular flow by the kinds of characteristics that are needed to support a particular application.

Properties such as maximum and minimum allowable delay, delay variation, precedence, and other critical characteristics will help set the priority of flows in the Layer-3 environment. In addition to smoothing traffic and improving service, ToS will also help in mapping IP traffic between QoS/priority-aware protocols, such as Frame Relay and ATM.

Sadly, VLAN priority tagging and ToS have been developed independently, with only partial coordination between them. This leaves the potential for conflicting priority levels between LAN and WAN segments.While no direct mapping scheme appears possible today, we can expect to see the industry develop patches that bridge these discontinuities as ToS becomes part if the Internet cannon.

Implementation Insights

Most equipment designed from now on will almost certainly need to support VLANs, and most likely priority/QoS management too. Designers will have a wide range of choices about implementing these features, but there are some good solid guidelines to follow.

Perhaps most fundamental is the old question of segmentation — whether to perform a function in hardware or software. For some boxes handling 10-Mbit/s traffic exclusively, it is still possible to have an all-software solution. But with the shift to 100 Mbit/s and especially Gigabit products, it becomes critical to implement at least some of the most MIPs-intensive packet-processing functions in hardware.

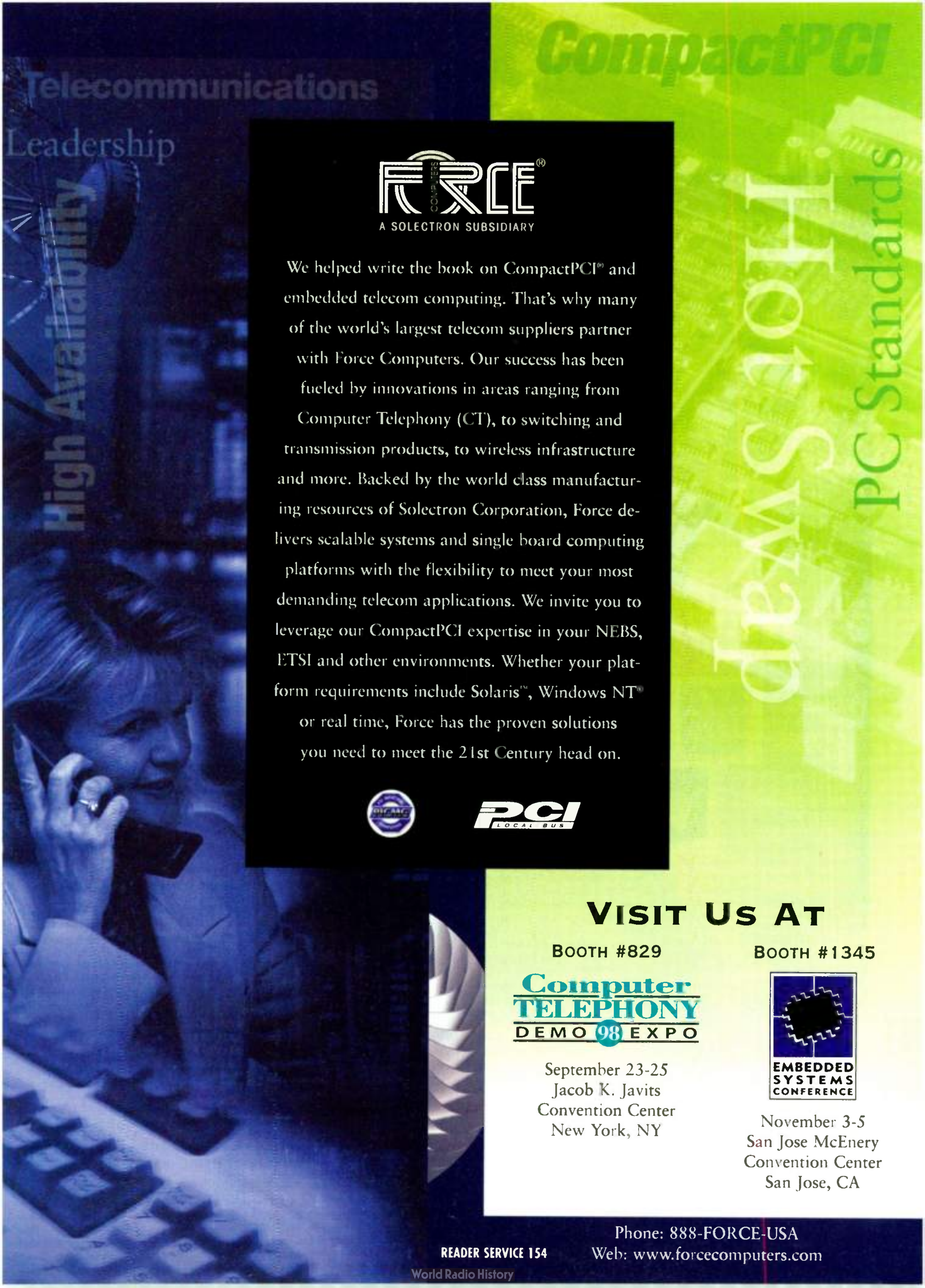
Consultant Rich Seifert suggests that designers divide these functions into two categories. Many tasks best suited for hardware are relatively simple, highly repetitive, and must often be performed on a per-packet basis. Checksum calculations, packet validation, lifetime control, and statistics collection lend themselves easily to hardware. Address lookup and translation is more difficult, requiring a switch to sort through multiple matches in large tables. Fast switching however, requires that at least most address resolution be done in hardware, with exception handling being kicked over to the control processor. The programmable controller should also handle complex, less frequent tasks, such as communication with other routers and generating alarms.

Priority management and policy enforcement fall between these two areas, requiring a combination of hardware and software to efficiently perform these complex tasks. One area of interest is queuing, where incoming packets are prioritized for transmission through the switch. This can be accomplished either by buffering the flow and allowing high priority packets to be processed first, or by setting up multiple queues for different priority traffic.

In a multiple-queue system, different algorithms can be implemented to insure at least some traffic from each queue is processed. One example is the fair-weighted round-robin method, which rotates regularly between each queue, and employs an adjustable weighting scheme that balances priority against queue depth.

Because these issues have been with us for some time, many silicon vendors have been following them and developing some interesting solutions. It is surprising to see how much hardware logic is being thrown at managing these complex problems.

Galileo Technology's new GalNet-II switching architecture, for example, employs a relatively simple but effective programmable 2-level priority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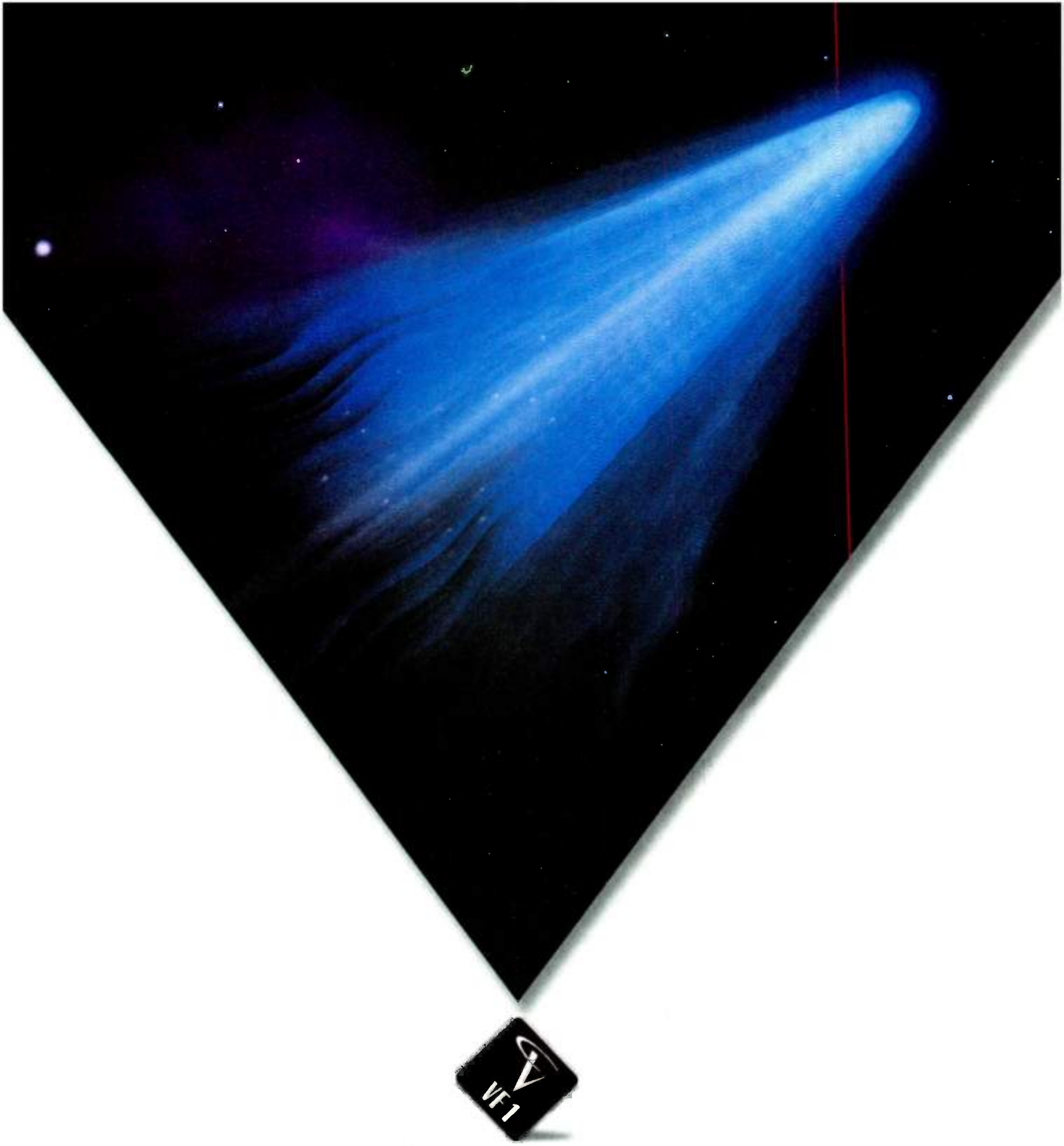
queuing scheme. Their new GT-48310 switch performs priority extraction from 802.1Q tagged packets and assigns packets to one of two queues per port. While the high-priority queue commands first rights to the port's bandwidth, programmable alarm thresholds in each queue can be used to prevent buffer overflow, either by reweighting the output queuing or by reducing incoming traffic through backpressure signaling.

Some companies, such as Vertex Systems, actually employ a specialized processor that has an architecture and instruction set that has been tailored for the kinds of operations performed in networking. The modified RISC engine embedded in the switch permits the Vertex chip set to perform real-time Layer-3 switching at Fast Ethernet speeds, including address resolution to the sub-net level. In addition to a relatively large memory to contain the address resolution table, Layer-3 switching requires the switch be able to modify the IP address on the fly. Although not exactly a full-up processor, MMC Networks' solution also employs a highly programmable switching engine that is flexible enough to handle the full range of priority queuing on a per-flow basis. Its outboard management engine allows it to support very detailed user-defined policy and priority weighting schemes.

While hardware can be used to offload a processor by managing queues, counting bytes, and performing routine manipulations, a programmable processor is almost always required to handle the subtleties and exceptions found in most policy enforcement schemes. Whether it is embedded within the chip set, or residing externally, these processors are responsible for making sure traffic stays within its assigned parameters and that the switch's priorities are observed.

Features like this will become increasingly important as networks carry more and more multimedia traffic and the emerging QoS standards become more commonly used. Can QoS protocols really help IP networks meet the challenges of Gigabit traffic, isochronous multimedia streams, and rapidly shifting usage patterns? There's only one way to find out: Stay tuned to this space for updates on these exciting technologies as they happen.


VF1

Wescon/IC Expo '98 Delves Into System-On-A-Chip Issues

The Wheels Are Turning As The SOC Concept Affects A Broad Range Of Disciplines, Such As EDA And Quality/Reliability/Test.

Joseph Desposito

Just as system-on-a-chip (SOC) issues have grabbed the attention of design engineers worldwide, so too has this topic grabbed center stage at Wescon/IC '98. The conference, which takes place Sept. 15-17, at the Anaheim Convention Center, Anaheim, Calif., will feature a system-on-a-chip SOC exhibit floor showcase and technical sessions. Furthermore, SOC technology is being established as a long-term focus area for the show. More than 35,000 electronic-design, test, manufacturing, and purchasing professionals are expected to attend.

The applications conference begins on Wednesday, Sept. 15, with workshops, short courses, and technical sessions at the Anaheim Marriott, which is adjacent to the convention center, as well as over 1400 exhibits at the Anaheim Convention Center. SOC technologies, tools, and applications are the focus areas for the conference.

The engineering workshops, which were introduced at last year's show, range from one to three hours in length, and offer application-specific training from engineers primarily on a variety of SOC topics. In addition, full- and half-day short courses provide in-depth information not only on SOC topics, but also on system environment and interface, and wireless and network system design. Technical sessions are available in all of the above areas and biomedical systems as well.

The workshops and short courses require additional fees. For a flat fee of $50, you can attend most of the technical sessions plus obtain a copy of the show's proceedings.

Wescon kicks off with a keynote roundtable entitled: "Systems-on-a-Chip: Economic and Industry Perspectives," from 9:00 a.m. to 11:00 a.m., on Sept. 15 at the Anaheim Marriott. The keynote will present the perspectives of six high-level industry executives concerning the successful advancement of SOC technology. The keynote roundtable is free; however, seating is limited, and reservations are required.

In the SOC area, workshops, short courses, and technical sessions are divided into tracks covering next-generation IP networks, chip-level and system design, embedded systems, aerospace applications, quality/reliability/test, and electronic design au-

WESCON/IC EXPO '98 TECHNICAL SESSIONS

Tuesday, September 15					
Keynote 1: Systems-on-a-Chip: Economic and Industry Perspectives 9:00 - 11:00 a.m.					
TS3 Smart sensors and MEMS (SOC: System design) 9:00 a.m. - 12:00 noon	**TS7** Scalable architecutre for direct execution of Java programs (SOC: Embedded Systems) 1:00 - 3:00 p.m.	**TS10** Monitoring system environment for improved performance/ reliability (Systems Environment) 1:00 - 3:00 p.m.	**TS5** EEMBC: MCU/DSP benchmarks for embedded market (SOC: Embedded Systems) 3:00 - 5:00 p.m.	**TS11** Thermal considerations for system design (System Environment) 3:00 - 5:00 p.m.	**TS13** Bus technologies (System interface) 3:00 - 5:00 p.m.
Wednesday, September 16					
TS17 Networking strategies (Network System Design) 9:00 - 11:00 a.m.	**TS4** System design issues (SOC: System Design) 9:00 a.m. - 12:00 noon	**TS16** Systems-on-a-chip for space exploration missions (SOC: Aerospace Applications) 9:00 a.m. - 12:00 noon	**TS1** Chip-level design issues (SOC: Chip-level design) 1:00 - 3:00 p.m.	**TS9** RTL verification (SOC: EDA) 1:00 - 3:00 p.m.	**TS12** Advances in high-speed parallel port performance/ sharing (System interface) 1:00 - 5:00 p.m.
TS14 Cellular telephony issues (Wireless System Design) 1:00 - 3:00 p.m.	**TS20** Development/capabilities of a joint venture SOC design complex (SOC: Chip-Level Design) 2:00 - 5:00 p.m.	**TS15** Wireless system design issues (Wireless System Design) 3:00 - 5:00 p.m.	**TS8** Windows CE for embedded applications (SOC: Embedded Systems) 4:00 - 5:00 p.m.		
Thursday, September 17					
TS6 Enabling technologies for embedded systems (SOC: Embedded Systems) 9:00 - 11:00 a.m.	**TS18** Biotechnology and bioengineering-integrated design (Bio-Medical Systems) 9:00 a.m. - 12:00 noon	**TS2** Hardware/software co-design (SOC: Systems Design) 10:00 a.m. - 12:00 noon	**TS19** Biotechnology and bioengineering-medical technology perspective (Bio-Medical Systems) 1:00 - 3:00 p.m.		

SmartLink Mini Instruments Give Precise RTD Temp Measurements

Two new SmartLink instruments, the KNM-RTD31 and KNM-RTD32, are designed for making PC-based laboratory-grade temperature measurements from RTDs in plant, field, and laboratory locations. The KNM-RTD31, which can measure a single-ended RTD or four-wire RTD, has two digital outputs. The KNM-RTD32 is a self-contained, signal-conditioning instrument for up to eight single-ended or 4 four-wire RTDs; it also has two digital outputs. Both models can be used for general-purpose resistance measurements as well. The 6.7 in. by 1.3 in. by 1.1 in. size of the instruments enables them to be placed just inches away from signals and sensors. This will minimize lead length errors and induced electrical noise. Both instruments feature a high-precision, 20-bit Σ-Δ analog-to-

digital converter. that delivers seven readings/s at full accuracy. The KNM-RTD31 is priced from $595 and the KNM-RTD32 is priced from $995. Both are available two weeks ARO.

***Keithley Instruments Inc.**, 28775 Aurora Rd., Cleveland, OH 44139-1891; (888) KEITHLEY; (440) 248-0400; fax (440) 248-6168; e-mail: product_info @keithley.com; www.keithley.com*

CIRCLE 485

Booth 2303

Next Generation Magnetic Joysticks Employ Hall-Effect Sensors

The new HFX line of magnetic joysticks are designed for original equipment manufacturers requiring a rugged, durable joystick. The HFX incorporates automotive-quality Hall-Effect sensors and solid magnets in a small, compact housing. Available in single-, dual-, and three-axis configurations with or without pushbuttons, the HFX joystick is ideal as a control for either stepping or servo motors. The HFX joystick is meant as a replacement for older inductive coil joysticks. By using Hall-Effect sensors and high-grade solid magnets, the HFX line of products offers significantly improved resistance to RFI and EMI distortions. In addition to its advanced stability, the HFX joystick has an operational temperature range from 25°C to 85°C. The HFX output also can be programmed for automatic fault detection. Production shipments will

start in July of 1998. Typical prices range between $35 and $108 at the 100 unit price break.

***CH Products**, 970 Park Center Dr., Vista, CA 92083; (800) 240-7282; (760) 598-2518; fax (760) 598-2524; e-mail: oemsales@chproducts.com; www.chproducts.com/oem.*

CIRCLE 486

Booth 3204

tomation (EDA).

Full-day short courses in the SOC tracks include such topics as "CPLD, FPGA, and ASIC Design Fundamentals;" "Signal Integrity Issues in High-Speed System Design;" "System-on-a-Programmable-Logic-Chip;" "Designing Complex, Bug-Free Chips;" "Built-In-Testable-Systems-on-a-Chip;" and "Systems-on-a-Chip Test Strategies." Other tracks cover "Radiated Emissions and EMC in ICs" and "Internetworking with TCP/IP."

Half-day short courses focus on "Reconfigurable Architectures," "Analog Aspects of PCB Layout," "Adding Mobility to ATM Core Networks," "Digital Wireless Communications for Third-Generation Cellular Systems," "Wireless/RF Design Fundamentals," "Implementing Gigabit Ethernet over Copper," "Networking Fundamentals—The Physical Layer," and "Networking Fundamentals—The Data Link Layer."

The system-on-a-chip workshop topics are arranged by track. The chip-level design track includes "Design Reuse" and "Embedded RAM, FPGAs, and HDLs for Fastest Systems-on-a-Chip Design Cycle." The system-design track includes "ASICs Replacing DSPs in Systems-on-a-Chip Designs," "Microcontrollers—Part I" and "Microcontrollers—Part II," "Mixed-Voltage System Design Issues," "Solving the Mixed-Signal Design Problem," and "Trends in Memory Technologies." The embedded-systems track includes "Consumer Appliance Design with Java Technology," "Mobile Communications Devices—Design and Software Challenges," "Systems-on-a-Chip: A Low-Power Solution," and "Systems-on-a-Chip Using Multiple RISC and DSP Processor Cores."

The quality/reliability/test track includes "Microchip Quality and Reliability." And, the EDA track includes two workshops, "Architectural Exploration through Behavioral HDL Design Methodologies: An Introduction," and "Verification Techniques for Embedded Core-Based Chips Using Emulation." One other workshop, under the system-interface track, focuses on "Bus and Backplane Interface Solutions and Signal Integrity."

The applications conference will present 20 technical sessions in three

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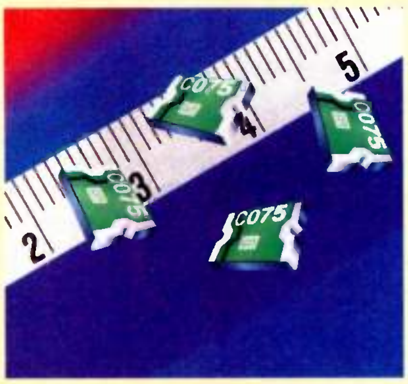
Booth 3259

Resettable Fuse Features Fast Trip And Miniature Footprint



The new PFMC series of resettable fuses are miniature-size, surface-mount-technology (SMT), polymer-based PTC (positive temperature coefficient) fuses. The PFMC series measure 3.0 by 2.35 mm and trip in 20 ms maximum (at 8 A, 23°C). They're available in ratings between 0.2 and 1.1 A, with interrupt ratings of 40 A and 6 to 15 V. The C-shaped, castalated terminal on the fuse enhances visual inspection of the solder connections, while the flip-chip design allows for mounting on either side. A fast trip time offers protection in applications such as PC motherboards, peripherals, mobile phones, and test and measurement equipment. The fuses are fully compatible with current industry standards can be used almost anywhere there is a low voltage power supply and a load to protect. The series has UL, CSA, and TUV approvals. The fuses are available on 1500-piece reels, priced at $0.39 each. Delivery is from stock to six weeks.

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CIRCLE 488

Booth 1438/1440

days, so attendees should keep a schedule handy (*see the table*).

SOC Technical Sessions

Eleven of the technical sessions deal with SOC issues, while nine cover topics related to other areas. In the SOC area, one of the hot topics is Windows CE. In the technical session entitled "Windows CE for Embedded Applications" (TS8), Matt Hershenson, systems development manager at Philips Semiconductor's Handheld Computing Group, Mountain View, Calif., explains how to design a Windows CE handheld computer. Hershenson notes that the next generation of Windows CE devices will have bigger caches, pseudo-DSP modem synthesis, and mixed-signal peripheral chips. Also, chips will be more powerful, have increased clock speeds, and require less power consumption. Hershenson will discuss how manufacturers design chipsets to meet these needs.

During the technical session on chip-level design issues (TS1), Will Remaklus, an applications engineer for PowerPC embedded processor solutions at IBM Microelectronics, Hopewell Junction, N.Y., will talk about an on-chip bus structure for custom-core logic designs. Typically, systems-on-a-chip contain numerous functional blocks representing a very large number of logic gates. Remaklus thinks designs such as these are best realized through a macro-based approach. Macro interconnectivity is ensured by using common buses for inter-macro communications. Remaklus will discuss three buses for interconnecting cores, library macros, and custom logic.

In the hardware/software codesign technical session (TS2), one of the presentations covers how to apply these techniques to systems-on-a-chip. Dr. Arnold Berger, director of R&D at Applied Microsystems Corp., Redmond, Wash., notes that system-on-a-chip design is reported to be five times more resource intensive than developers are estimating. Development tool immaturity is the root of the problem, according to Berger. This presentation will examine the status of development tools for SOC design, and compare them to traditional tools used for board-level development processes.

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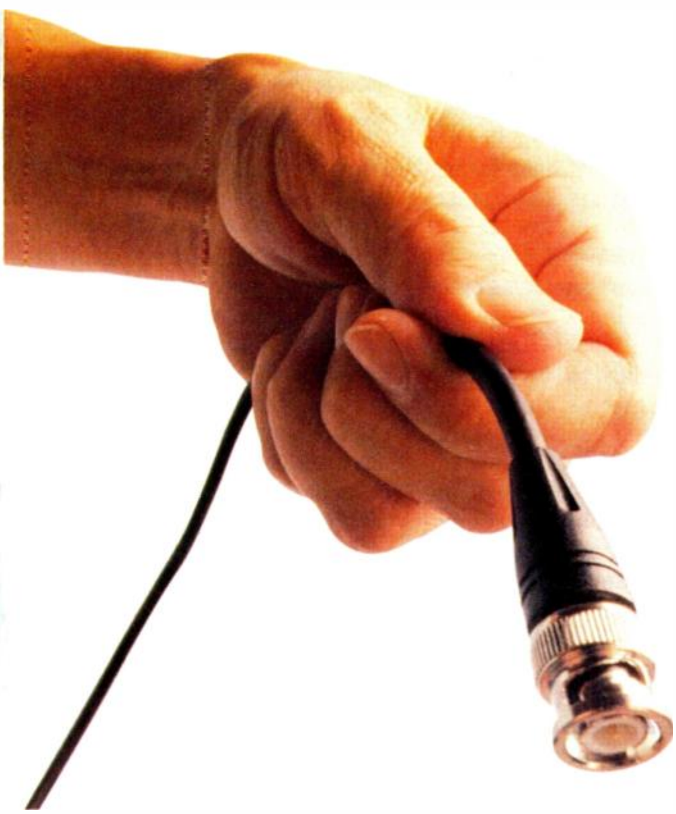

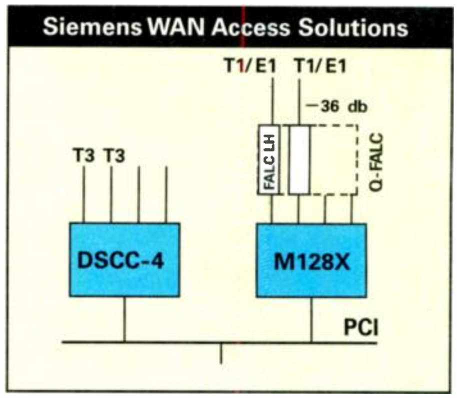

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electromechanical systems (MEMS), has improved sensor reliability and cost, and has made them practical for use in consumer electronics. In the technical session entitled "Smart Sensors and MEMS" (TS3), one of the presentations covers advances in wireless microsensor networks. Rockwell International Corp., Costa Mesa, Calif., and the University of California at Los Angeles are developing wireless sensor networks with highly integrated network nodes.

Each node contains multiple sensors, onboard signal conditioning, onboard logic and control, and extremely low-power RF transceivers. These intelligent microsensor nodes generate and operate on information at the point of data collections, and thus provide a path to scaleable networks. Prototypes have been applied in surveillance, security, and machinery monitoring applications. Dr. Henry O. Marcy, program director at the Rockwell International Science Center will describe the present status and ultimate vision for this work.

Standards are always an important part of system design issues. One of the presentations of technical session four (TS4) is on Virtual Socket Interface (VSI) standards. Mark Hahn, architect at Cadence Design Systems' Deep-Submicron Division, San Jose, Calif., notes that the VSI Alliance has made significant progress in standardizing the data created by a virtual component (VC) provider, and passed to a system chip integrator. This presentation describes the standards available today, how they can be used, and the latest work going on at VSI.

More About Technical Sessions

As mentioned, nine of the technical sessions do not fall under the system-on-a-chip banner. One of the sessions (TS14) covers cellular telephony issues. Gerry Pepenella, director for IC and system products at Lucent Technologies, Murray Hill, N.J., will address 3G cellular requirements and integration. These third-generation networks blend cell transport with traditional cellular system needs, causing base-station functionality to change significantly. Pepenella will present an overview of the requirements of 3G systems, and show how a combination of silicon technologies can produce high-function, low-cost, low-power, and yet, flexible solutions.

In the technical session on networ ing strategies (TS17), Ken Soohoo, chi technical officer at PlanetWeb, Inc Mountain View, Calif., will make a presentation about providing Internet capabilities for consumer electronic devices. He notes that more people are looking for affordable electronic devices that will provide convenient access to the Internet. This session will cover the available technologies, devices, and customer expectations for Internet-enabled devices.

Everyone knows it is only a matter of time before the bionic man and woman become a reality. The techn ogy session on integrated design biotechnology and bioengineeri (TS18) shows some of the progress b ing made in this area. Bob Katz, vi president of research and developme at Symphonix Devices Inc., San Jos Calif., will make a presentation on th vibrant sound bridge—implantable transducer technology for hearing loss.

Katz asserts that the vibrant sound bridge is the first of a new generation of implantable hearing devices intended to provide improved performance for sound amplification, producing more natural sound quality while eliminating occlusion, feedback and other disadvantages of acoustic amplification. The technology is based on an implantable trans ducer designed to operate in conjuncti with the native middle ear structures.

Another presentation in the sar session concerns silicon cochlea. I Bogdan Kuszta, ChE undergradu laboratories director at the Califor Institute of Technology, Pasaden Calif., will describe an electronic cochl designed at Caltech's C. Mead Lab. This device closely mimics the dynamics of the real cochlea in terms of frequency distribution along the transmission line. This line consists of several hundred filters with decreasing cutoff frequencies. The distribution of the active length of the delay line corresponds to the distribution of frequencies of the acoustic signal according to Kuszta. The silicon cochlea processes sound over six orders of magnitude in intensity, while dissipating less than 0.5 mW.

These are just a few highlights from the technical sessions. Keep in mind that each of the 20 sessions has several presentations, so there's a range of technical information available withir each specific topic.

ELECTRONIC DESIGN QUICK LOOK

■ Edited by Debra Schiff and Nancy Konish

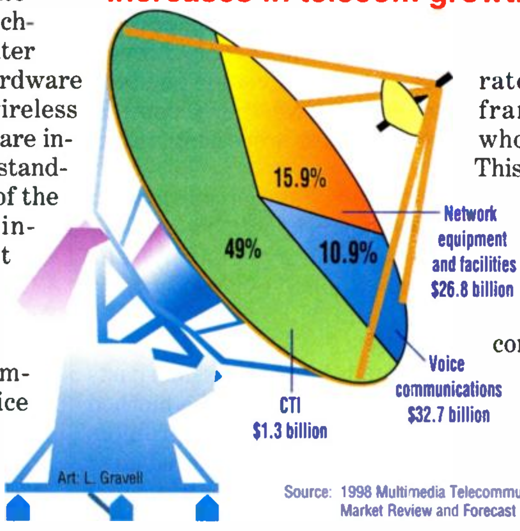
MARKET FACTS

I've Got Just One Word For You: Telecommunications

If you're looking to invest money somewhere these days, the direction to go with it is telecommunications. According to the recently released "1998 MultiMedia Telecommunications Market Review and Forecast," jointly produced by the Telecommunications Industry Association and the MultiMedia Telecommunications Association, U.S. spending on telecom equipment jumped 13% to \$106.4 billion. The overall telecommunications market (which they define as equipment and services) rose over 11% in 1997, seeing revenues of \$406.7. Of the fastest growing categories in that year, emerging technology skyrocketed 60%, computer telephony integration (CTI) hardware and software improved 49%, wireless handsets rose 37%, and groupware increased 30%. Aside from those standouts, the report states that all of the categories saw significant increases in growth. The market drivers here are: increased demand for larger volumes of information, a rise in spending on the part of small- and medium-sized firms, the demand for voice and data integration, the need for more interoperability, a call for cost-effective solutions, and a widening international market. The development of standards is pushing the desire for better interoperability in the telecommunications market. Looking at the network equipment and facilities segment, growth there (shown above) was a result of analog to digital and electromechanical to electronic conversion, in addition to the expanded use of fiber-optic cable. Another little jolt came from a rise in demand for ISDNs, and Internet and remote access. In the voice communications market, the focus was on the private-branch-exchange (PBX) sector. System upgrades, add-on lines, and new forays into applications typically covered by key-telephone systems and hybrid systems helped this sector maintain its growth pattern. One interesting trend exposed in the report was that of the fastest growth appearing in systems with 1000 or fewer lines. This statistic shows that the market is centering around those small- and medium-sized companies that can now grab the kinds of technology that used to be available only to the conglomerates. There also has been an increase in voice communications technology sales. It appears that shoppers are going after consulting services, end-user training, logistical support, and maintenance and repair. Not surprisingly, the mobile and wireless communications sector continues to grow. Fed by both the enterprise and consumer markets, these industries are indebted to personal communications services, and pager services for their rosy growth percentage rates. Emerging technologies, such as frame relay, ATM, and ISDN grew a whopping 60.4% to \$3.9 billion last year. This increase is evidenced in the ever-widening bandwidths found in industry. The report projects growth in this sector to increase at a compounded annual rate of 22% through 2001. Collaborative technologies, the most common one videoconferencing, saw the U.S. spending \$930 million in 1997, up 30.1%. Groupware, another evolving technology, is working through a face-lift as manufacturers are beginning to offer Internet-compatible packages. Last year's spending tally on groupware added up to \$425 million, a 25.7% increase from 1996. And, the increase in CTI growth, according to the report, can be attributed to declining CTI station prices, and rising customer knowledge of the technology. Exports of U.S.-made telecommunications equipment increased by about 24%, to hit \$21 billion in 1997. According to the report, the evolution to a global economy has set off the spark of foreign investment in places where telephone usage is just beginning to take off. The prediction for worldwide spending on telecom equipment is an increase from \$250 billion in 1997 to \$400 billion by the year 2001.

To obtain the market review and forecast, call (703) 970-7472; visit www.tiaonline.org or www.mmta.org, or e-mail vhancock@tia.eia.org.—**DS**

Increases in telecom growth



Source: 1998 Multimedia Telecommunications Market Review and Forecast

40 YEARS AGO IN ELECTRONIC DESIGN

High Speed Teletype Revealed by Army

Messages at the rate of 750 words a minute are being printed by a new message printer and code puncher, the first in a new family of superspeed combat teletypewriter units. The new device, reportedly the world's fastest, was developed for the U.S. Army Signal Research and Development Lab, Fort Monmouth, N.J., by Kleinschmidt Laboratories Inc., a subsidiary of Smith-Corona. The device has no ordinary typing keys. Instead, a whirling wheel rimmed with letters prints the high-speed messages. It spins at 3,750 rpm. At the precise instant the correct letter comes into position, a tiny hammer strikes the paper against the type wheel.

Messages are typed out on 7/8 in. paper tape. At the same time coded holes are punched out. Tape rate is more than seven and one-half inches per second. These tape messages can be relayed rapidly to other points or they can be printed on the spot in page form by automatic typewriters. The printer mounts on a jeep or truck teamed to a mobile forward area communications center. The printer-puncher could also be used to feed battle information into a new mobile combat computer now under development. In future commercial use, the device could speed the transmission of telegrams, stock market quotations, and weather reports. It may also have applications in the field of integrated data processing. (Electronic Design, September 3, 1958, p. 12)

This system was certainly state-of-the-art back then, but I have to wonder about it. How well could the printer stand up to the rigors of battlefield conditions and maintain the timing and alignment required in the print head? Also, how long would paper tape last in extreme conditions? —Steve Scrupski

Idea For Design: Cake Decorator for Potting

It's difficult to inject very viscous potting compounds into inaccessible parts of electronic assemblies. When production quantities are small, the method should be very inexpensive. A 49 cent cake decorator solves the problem neatly. It is disassembled easily for the very thorough cleaning required after use. T.H. Goodenough, Project Engineer, General Devices, Inc., Princeton, N.J. (Electronic Design, September 3, 1958, p. 122) (Comment below)

Idea For Design: Double Duty Formex Skinner

Removing insulation from Formex transformer wire is tricky. The usual technique of burning it off with a soldering iron doesn't work because most irons aren't hot enough. About the handiest way to do it consists of rigging some Nichrome resistance wire to a 6v transformer. This gets hot enough to melt off the Formex insulation, and serves as a handy cigarette lighter to boot. (Electronic Design, September 3, 1958, p. 122)

In the early years, the Ideas for Design section contained these types of practical lab tips as well as useful circuit designs. Engineering in those days consisted of a lot of ad hoc solutions to mechanical and thermal problems, and IFDs provided a forum for the exchange of any and all ideas.—Steve Scrupski

Steve Scrupski is a former Editor-in-Chief of Electronic Design. Now semi-retired, he can be reached at scrupski@worldnet.att.net.

Tele-Healthcare

Say you live in a country that lacks good health care. Your best option is to travel to a more advanced, neighboring country for treatment. But, if you're very sick, the trip could make you worse....Enter telemedicine.

In Gozo, patients in need of specialized health care traditionally travelled to Malta by ferry or helicopter. Now, a telemedicine link has been created between St. Luke's Hospital, Malta, and the General Hospital, Gozo. Live, real-time images are broadcast between the two hospitals, permitting physicians to exchange materials, like X rays, and discuss clinical cases.

With the videoconference, physicians consult each other on a case-by-case basis. This ensures that the two hospitals work together. The patients generally don't travel back and forth, and suffer less strain.

The system actually uses two links. One is between the Gozo General Hospital and the Maltese Government's information system for public hospitals and health centers. This link existed previously, but was upgraded to allow real-time videoconferencing. Formerly 64 kbits/s, it's now 2 Mbits/s. The second link is between the two hospitals in Malta and Gozo. It utilizes fiber-optic technology, as well as a digital radio-transmission network.

The internal communications network in both hospitals uses fiber-optic technology, while their telemedicine stations connect to the Malta Government Network. This high-bandwidth, local-area government network is also well-maintained. Both links were created with a lot of emphasis on the sustainability of the systems. The network is installed permanently for ongoing use. To serve its purpose—to further develop health services in Malta—it will need only be maintained and upgraded with new equipment.

For more information, contact the Telecommunication Development Bureau, ITU; +41 22 730 5433; fax +41 22 730 5484; www.itu.int/newsroom.—**NK**

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	new	AK4523	20	96 (DAC) 48 (ADC)	First High End Codec with Master/Slave Capability!
		AK4526	24 20	96 (DAC) 48 (ADC)	Ideal Solution For Six Channel Home Theatres, DVD's, etc!
ADCs		AK5352	20	96	Unbeatable Price/Performance!
		AK5392	24	48	Pro-Audio Performance at Consumer Prices!
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JUST 4 THE KIDS

Last year, a series of interactive Cyber pets were released into the world. I'm guessing that many of you have a daughter, son, or grandchild who, at one time or another, has asked you to buy them one of these cute keychain-like toys. Little did you know how captivating this new toy would be, or what a great alternative it could provide to purchasing your child a real pet. The makers of the original Cyber pets, Bandai Digital Entertainment, Cypress, Calif., have added a great deal of educational value to their products. They have introduced a CD-ROM, several new toy versions, and a new line of bean bag Cyber pets, called Cybies.

The first of the recently introduced products, the Tamagotchi CD-ROM, works to bring the interactive toy experience of virtual pet ownership to the computer screen. Specifically intended for users ages eight and up, this virtual pet needs to be cared for in order to flourish. To help bring the pet to life, the CD-ROM uses full multimedia animation and a broad range of visual and audio expressions. It offers a number of interactive games the user can play to extend the program's game play. Some of the other features to look for in the toy include:

- "See Them Hatch!" A feature which lets the user watch the egg hatch into a full-grown character. You can also measure its growth with a health meter.
- "Watch Them Grow!" It enables the user to care for the Cyber pet, including feeding, playing with, and disciplining it. The user can even dispense medicine when the pet is not feeling well.
- "Create Their World!" The user can select a background and create a special environment for their pet.
- "Play With Them!" Activate a screen-saver mode and view the Cyber pet's growth.
- "Learn More About Them!" Use a scrapbook to track all the characters raised. Past generations can even be traced, including names, dates, and funny comments about their lives on Earth.
- "Share Them With Friends!" The user can print snapshots of their current and past pets, and even e-mail them to friends.

MARIFRANCES WILLIAMS

In addition to the CD-ROM, Bandai Digital Entertainment has created a line of interactive electronic pets known as the Tamagotchi Angels. These four egg-shaped, pearlized toys come in pastel shades of pink, blue, yellow, and white. The user simply nurtures their pet via a touch-activated screen so that it will do good deeds. In doing so, it gains angel power. Other features of the Angels include a new shooting stars game, an optional no-sound feature, and a pause function.

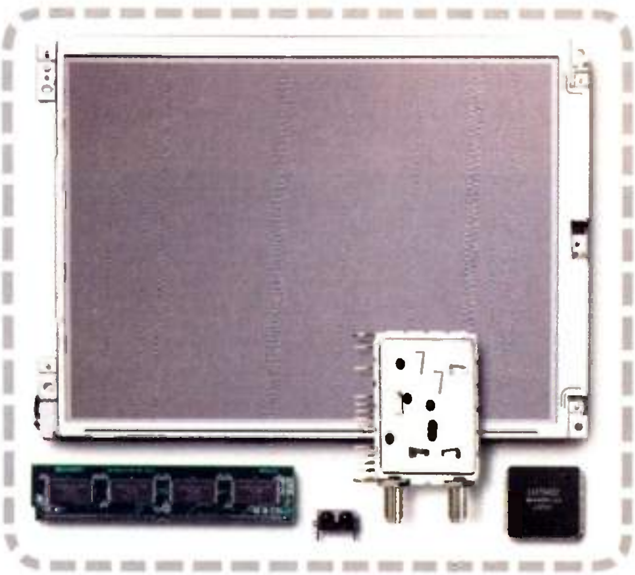
Bandai Digital Entertainment also developed two environment-themed toys—the Tamagotchi Garden and the Ocean. The Tamagotchi Garden consists of an entire family of garden characters just waiting to be discovered. It features bright garden colors, a foliage screen background, garden icons, and a leaf discovery game. The toy also includes the option of no sound, a unique touch screen, and pause features. The pause feature is especially beneficial, since most schools do not allow these toys on their premises due to distractibility. It also allows the child to complete homework, chores, and other tasks uninterrupted. The Tamagotchi Ocean features a new series of ocean characters. Focusing on the ocean theme, it offers the user ocean-like icons, an oceanic background screen design, and a treasure chest game.

In keeping with the Tamagotchi toys, Bandai Digital Entertainment also offers bean bag Cyber pets, called Cybies. Some examples of the Cybies now available include the Chestnut Angel, Smiling Angel, and Twin Angels. Cybies are available in a total of fourteen styles. Each four-and-a-half-inch tall figure is based on a character from the Tamagotchi toy line.

These Cyber pets are a great way to introduce your child to responsibility, while keeping it fun. They permit your child to see the actual amount of time and patience it takes to care for a pet. The Cyber pet also teaches the value of timeliness and the consequences of procrastination. A pet that is not well cared for will simply go back to planet Tamagotchi or die. As you can see, the Cyber pet has a lot to offer your child in the way of fun, entertainment, and learning. You can monitor just how much your child has learned, and then decide the amount of responsibility they can handle.

The Tamagotchi toys are available at most retail toy stores. The CD-ROM sells for approximately $19.95, while the Tamagotchi Angel, Garden, and Ocean are approximately $15.00 each. For more information, contact Bandai Digital Entertainment, 5551 Katella Avenue, Cypress, CA 90630; (714) 816-9700; or check out their web site at www.bdec.com.

Marifrances D. Williams holds a degree in Liberal Studies from San Diego State University, Calif. She is currently a fifth-grade teacher at Los Ranchos Elementary, San Luis Obispo, Calif. Williams specializes in the identification of advanced technology for the use of child-focused applications. She may be reached at williamsofsm@lightspeed.net.



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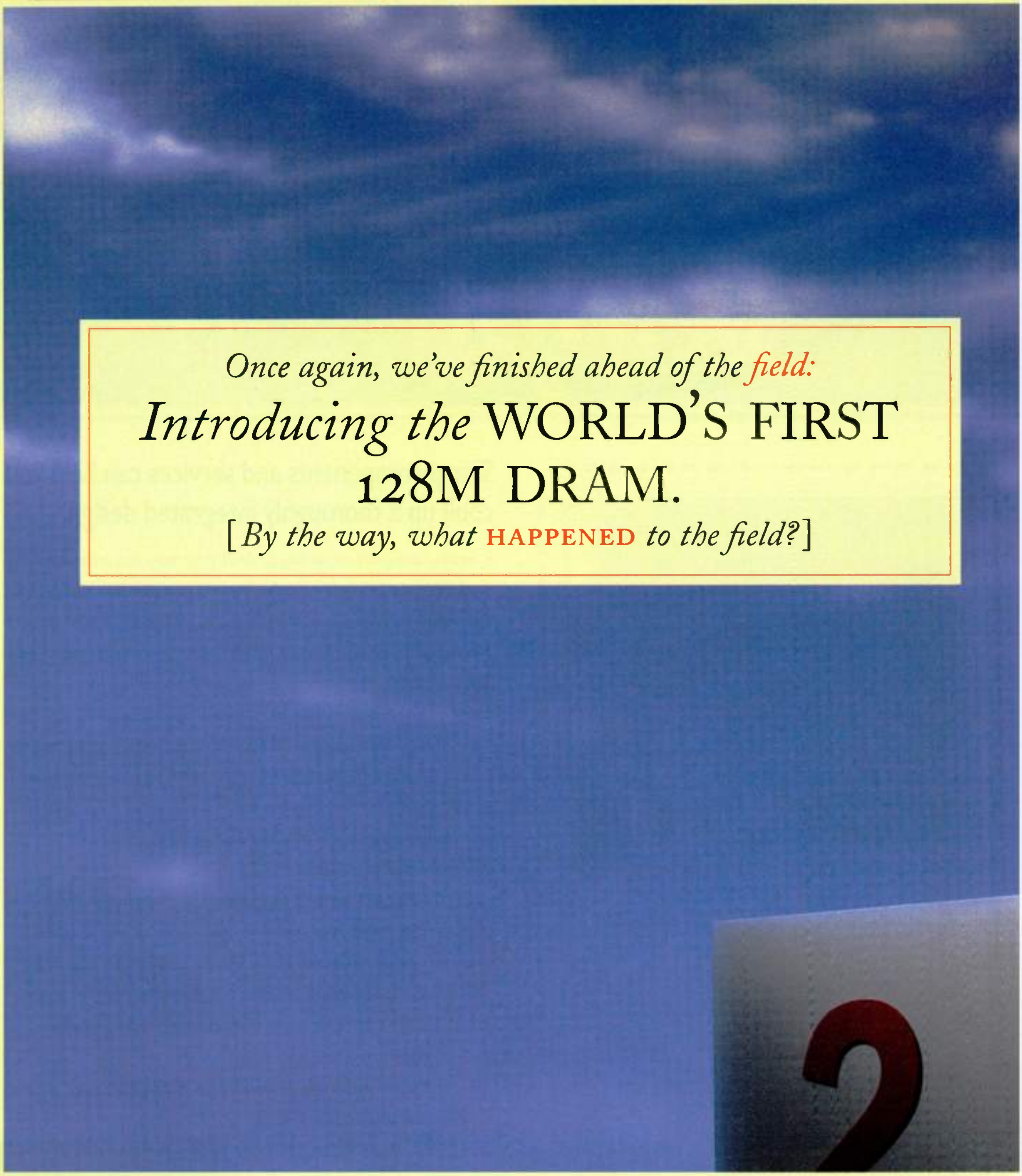

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DON REINERTSEN

While I see a certain value in project-management software, I am too experienced to believe it will cause you to complete your projects faster. In fact, I teach a two-day executive course on product development at CalTech five times a year. In the past five years, I have trained managers from 500 companies, large and small. At every class, I ask the attendees if project-management software really helps projects finish faster. The consistent answer is that there is no correlation between fast development and the use of project-management software.

Why? All project-management software array tasks in order of precedence. The next activity can begin when all its prerequisites have been completed. Thus, you know you have a problem when an activity is completed late—the essence of the problem. Using software to manage a project is like driving a car by looking through the rear-view mirror at the road behind you. You are looking at lagging indicators of project success, not leading indicators. Let's take a look at a few examples.

A good project manager walks through the team work area every day. He or she talks to all the members of the team. Here, you learn that your key firmware programmer just had twins, and his wife is unhappy with the 80-hour work weeks that he never complained about before. If you wait for this problem to show up in the project-management software, your first indication of trouble will be a missed milestone. "Why did we miss this milestone?" you ask. "Well, our key firmware programmer quit three weeks ago and we haven't found a replacement yet."

A good project manager stays in close contact with the customer. This way, you find out when the customer is planning to change product requirements. If you wait for the software to say you have a problem, your first indication of a problem is when your project is rejected in beta test.

A good project manager is constantly talking to the vendors. This is how you find out that the engineering manager for a critical, outsourced subassembly just got promoted, and a new hire has been placed in his or her spot. If you waited until the project-management software told you there was a problem, you'd discover it when the first article of the part wasn't delivered on time.

My key point is that a good project manager must concentrate on leading indicators of the road ahead. If you spend 75% of your time caring and feeding the project-management software, you will not have the time to do this. Instead, you'll be finding problems when they show up on your PERT chart, which is way too late.

Please recognize that the most valuable information you have for controlling the project will never appear in the project-management software, or if it does, it will show up months after you could have found the same problem by talking to team members, suppliers, and customers.

Don Reinertsen is president of Reinertsen & Associates, a consulting firm specializing in product development management. He can be reached at (310) 373-5332 or e-mail: DonReinertsen@compuserve.com.

Sun Revolution

You say you want a revolution...but do you want it in fiber optics? According to a recent report by a National Research Council (NRC) committee, the properties of light will be harnessed, bearing a revolution.

If this actually happens, engineering as we know it will end. Two conferences held in San Francisco, Calif., focused on such a future: Lasers and Electro-Optics and the International Quantum Electronics Conference.

This topic's also supported by the Coalition for Photonics and Optics (CPO), founded by 11 organizations from engineering, science, and trade backgrounds. Their goal is to prepare a resource and knowledge base for light technology.

The NRC's report, "Harnessing Light: Optical Science and Engineering for the 21st Century," specifies these plans. Their goals lay the groundwork for an instant jump into light technology. Several points spotlight the need to improve optics education, presenting it as a science *and* a technology.

In the workforce and research communities, the NRC urges agencies to build an initiative together. Government agencies, meanwhile, should support the revolution by ensuring that the broadband fiber-to-the-home infrastructure is developed and deployed quickly. In light of the possibilities of noninvasive monitoring and optical biomedical research, the NEC is promoting that the National Institute of Health dedicate more funding and research to optical science. According to the report, environmental, power, and other agencies will also be affected.

It is believed that optics will push technology to a new state, revolutionizing communications, medicine, energy, efficiency, and manufacturing.

For more information, contact the Optical Society of America, 2010 Massachusetts Ave. NW, Washington, DC 20036-1023; (201) 223-8130; fax (202) 223-1096; www.osa.org.—**NK**

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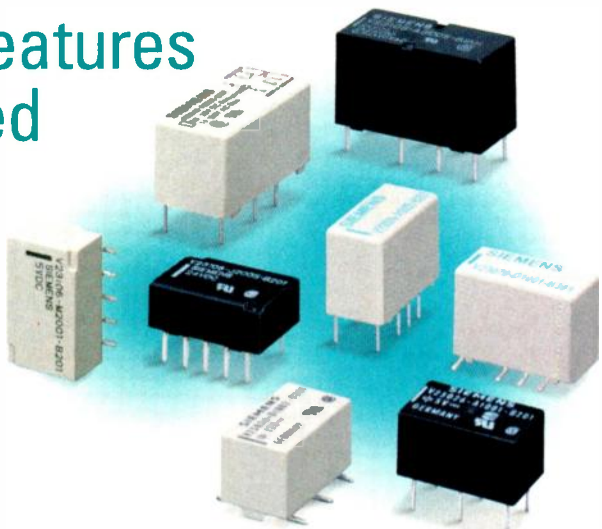

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Contact Rating	30W 60VA	30W 62.5VA	60W 62.5VA	60W 125VA	50-150W 250VA
Nominal Coil Power	30-150mW	100-200mW	70-140mW	150-300mW	75-360mW
Terminals	Pin or SMD	Pin or SMD	Pin or SMD	Pin	Pin
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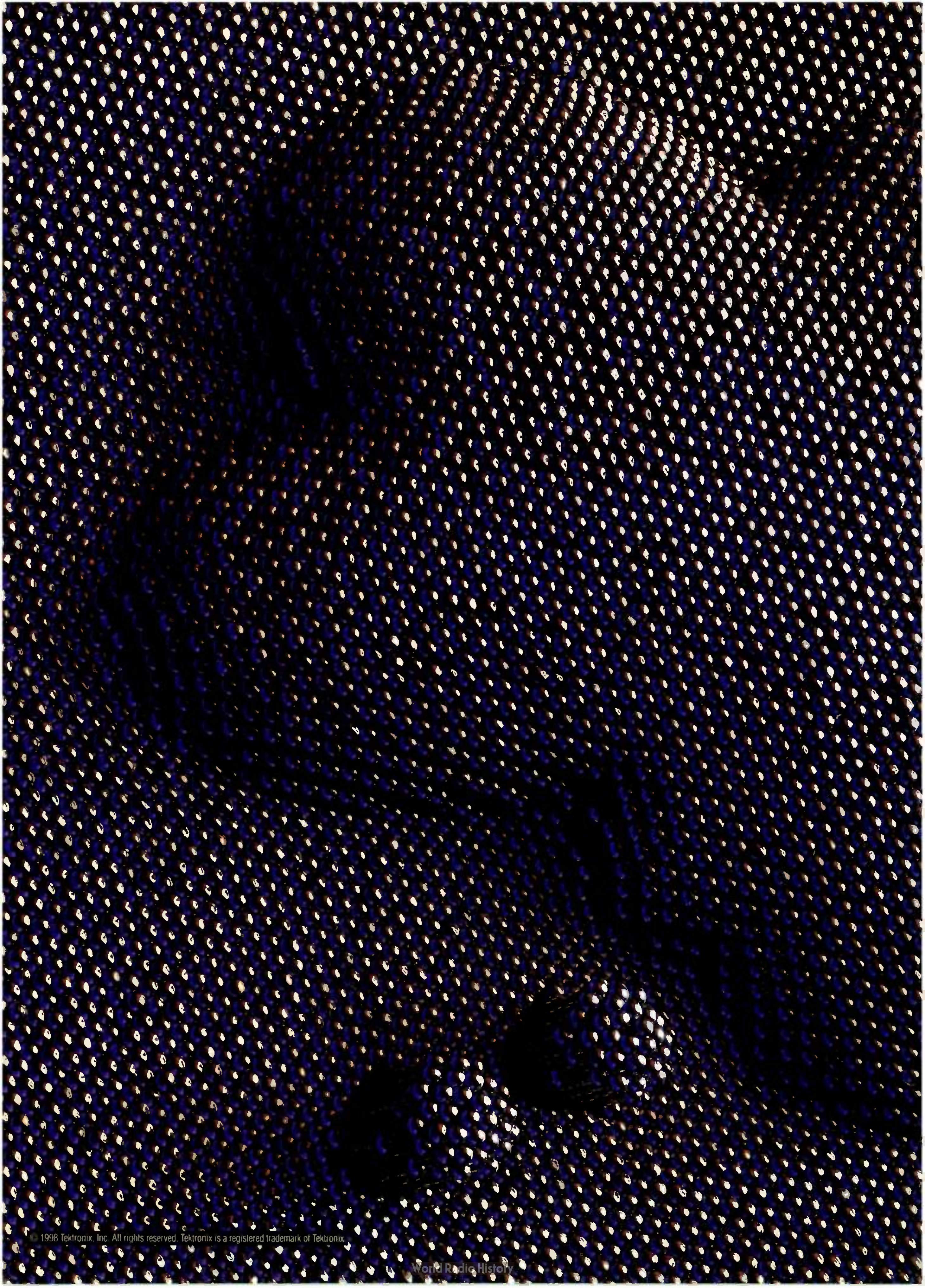
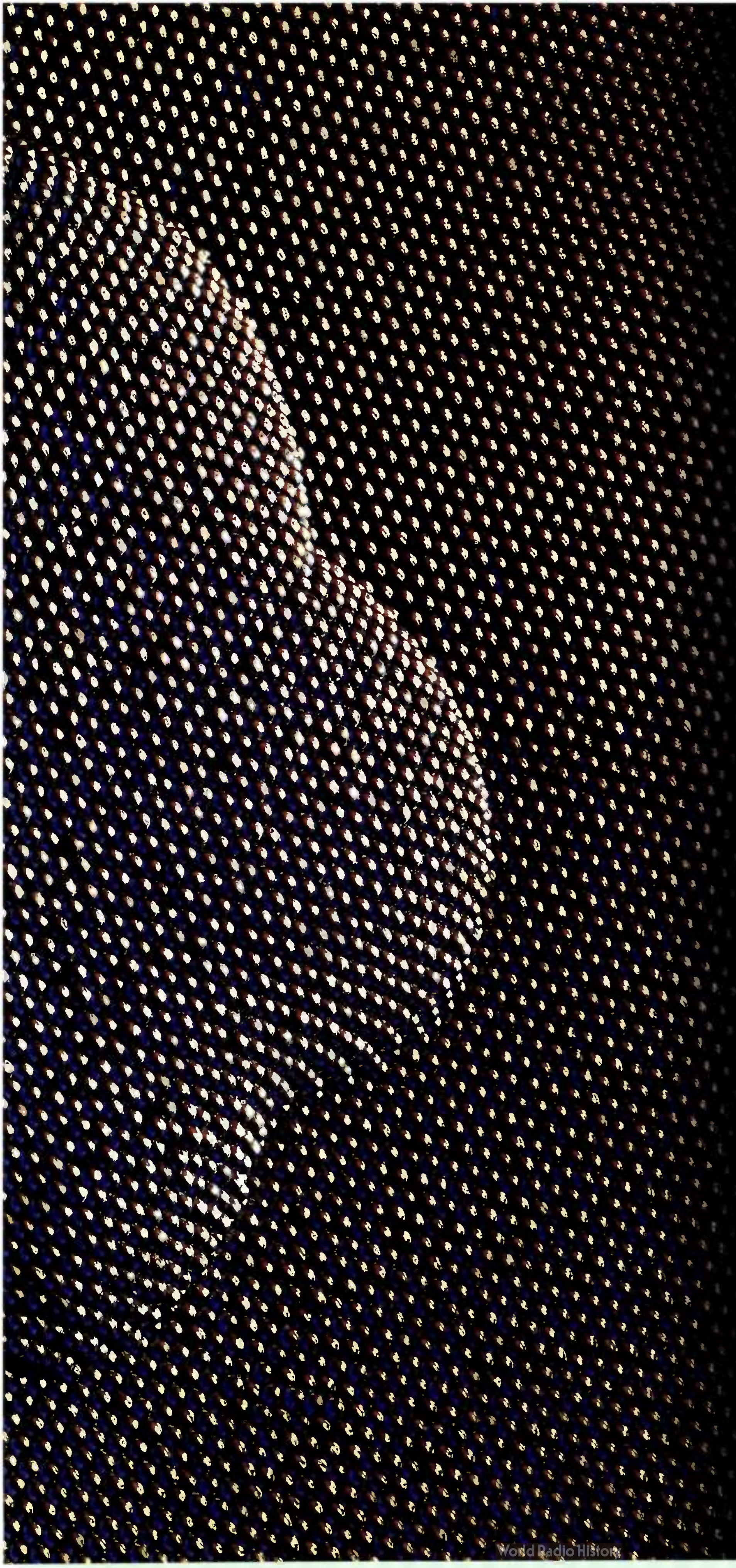




Watch Your Mouth For Buzzwords

Had enough of those same old motivational meetings? Does the inspirational dribble bore you, causing you to stare out the window? If so, you're the target market for Buzzword Bingo, which was developed by Benjamin Yoskovitz.

Rather than listen to the mumbo jumbo, hook up with some pals in the office. During presentations, you can play Buzzword Bingo in your portfolios, laptops, or Palm Pilots. Stash it out of sight and open your ears.

The game card looks like a normal Bingo card, but contains buzzwords instead of numbers. For example, words like "paradigm shift," as well as catch phrases like, "The ball's in your court," are printed on the cards. All you do is check off any buzzwords on your card that are spoken during the presentation. The person who checks off their whole game card wins. A cough usually signals the end of the game.

This game's sudden popularity caused some people to think about the nature of buzzwords. Buzzwords should motivate people to begin a new project, work as a team, etc. But, so often, the words fall flat. Due to either the abstract meaning or repetition of the words, they actually tend to have less impact than regular, everyday speech—not more.

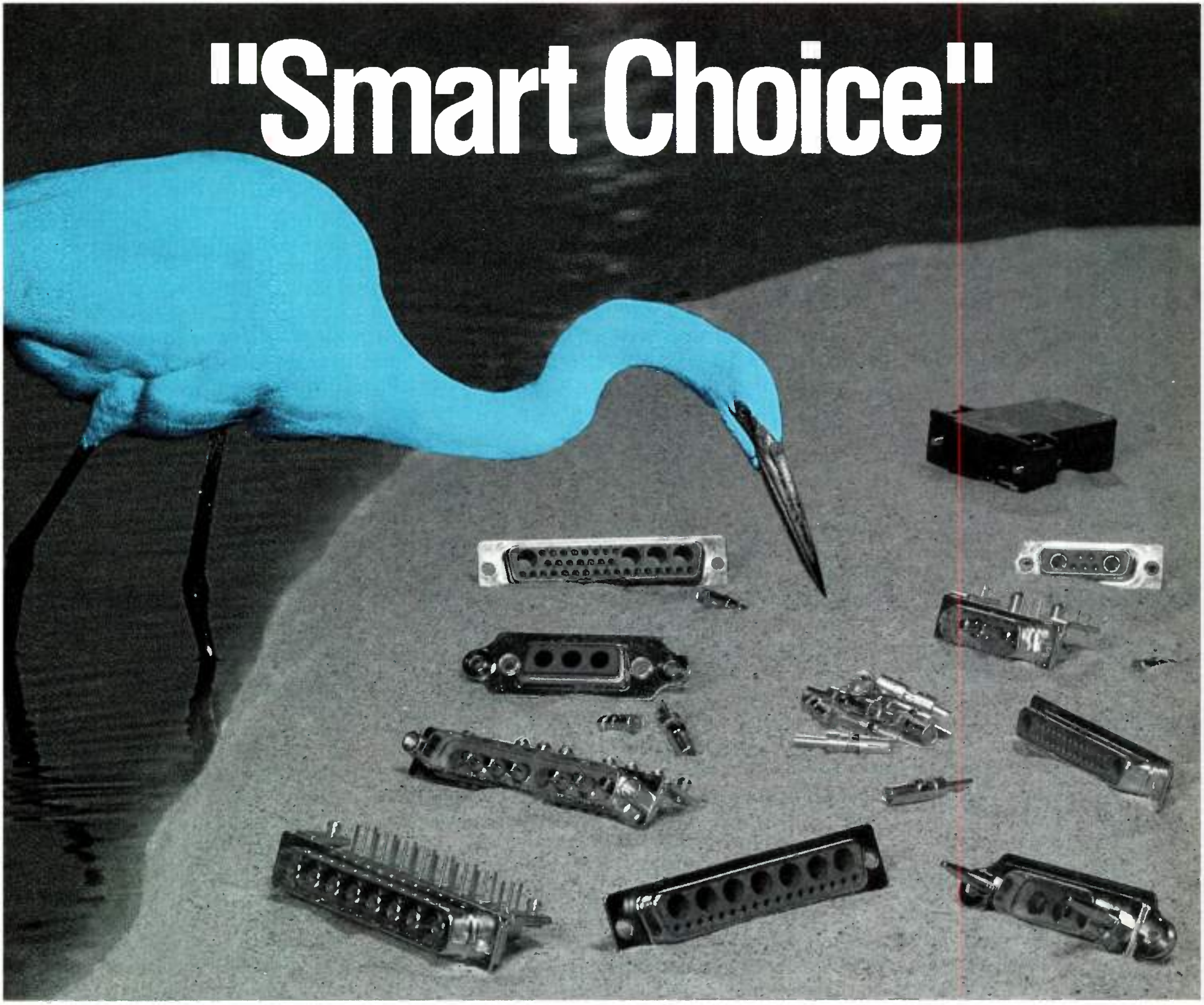
Kevin Daley, CEO of Communispond, a New York-based company focused on teaching communications skills, comments, "Words like 'operationalize,' 'deliverables,' 'optimize,' and 'actionable' are too abstract to convey much meaning. People can't picture what actions or emotions go into them. Buzzwords are too far removed from human life and personal experience to motivate anyone."

If you're a manager, look around at your next meeting. Those around you might seem to be paying suspiciously more attention while you're talking. Every once in a while, they might make a quick movement toward their computers....Yup, it looks like they're playing Buzzword Bingo. Don't get mad or be insulted. Think about the words you're using. If they're buzzwords, they're probably not registering. Not only are you failing to convey a solid message—it's likely that you're boring people.

Think of new ways to get your message across without buzzwords. Because these words have become a large part of our business vernacular, this is harder than you think. But, the possibility of actually reaching people should at least get you to try.

To check out Buzzword Bingo, go to Yahoo. Type in BuzzwordBingo.com. It's downloadable and constantly updated with new buzzwords. You can reload the page for the latest version.

For more information, contact meep! media inc., 390 Notre Dame West Suite 335, Montreal, Quebec, Canada H2Y 1 T9; (514) 288-5948; fax (514) 288-3409; www.meep.com. —**NK**


"Smart Choice"

HEADS UP

In what could be shaping up as a display interface war, several camps are now vying to become the next standard for connecting flat-panel monitors to computers. If these differences can't be ironed out soon, the dispute is likely to impede the adoption of flat-panel monitors—slowing their introduction just as they are poised to take off.

All of this activity is centered upon the newer digital interface for flat-panel monitors. Most flat-panel monitors today feature an analog interface, which uses a standard 15-pin VGA cable. This makes them direct replacements for CRT monitors. But, this approach requires at least one conversion of the digital graphics signal to an analog format.

Digital flat-panel monitors seek to keep the signal in a totally digital domain, thus avoiding artifacts that occur anytime there is conversion from analog to digital, or vice versa. Ultimately, this approach will also be more cost-effective, since it eliminates conversion electronics.

To make this happen, computer manufacturers, graphics card providers, connector vendors, and chip-set suppliers must develop new hardware, software, and standards to govern the digital interface. New computer graphics cards are needed, for example, to output digital signals from the computer (or possibly dual digital and/or analog signals). These digital graphics cards, and the monitors themselves, will also need to employ some sort of differential signaling protocol to allow high-frequency digital signals to properly travel the 10 to 15 feet common in desktop applications. In addition, computer manufacturers have to make product decisions that support a transition from analog to digital, and that offer the cost and connectivity features that consumers want.

All of these requirements have now produced three major digital-interface initiatives. The Digital Flat Panel (DFP) initiative, for instance, is being championed by Compaq Computer, Houston, Texas, and ATI Technologies, Thornhill, Ontario. It uses a 20-pin connector that supports the PanelLink digital-signaling concept forwarded by Silicon Image, Cupertino, Calif.

IBM, Greenoch, Scotland, and others are lining up behind the Plug & Display (P&D) interface, which uses a 34-pin connector. Newly entering the fray is a Japanese group headed by Hitachi and Toshiba, both of Tokyo, Japan, which is proposing the Display Interface Standard for Monitors (DISM). This approach includes existing P&D and DFP concepts, but expands consideration to include Sony's Gigabit Video Interface (GVIF) standard and several other interfaces. It includes support for 14-, 20-, 26-, and 40-pin connectors.


CHRIS CHINNOCK

Unfortunately, the current atmosphere is more likely to create confusion among consumers. Or, worse, it could result in a set of incompatible, digital flat-panel monitors. These camps, therefore, are now trying to find common ground to avoid a costly battle for the hearts and minds of consumers.

For example, P&D contains support for both a digital and a new analog interface, as well as Universal Serial Bus (USB) and IEEE 1394 connectivity. It has a monitor "hot-swap" capability, and should support monitor resolutions up to UXGA (1600 by 1200). Though it's a comprehensive interface standard, it may be too sophisticated for manufacturers to move to right away.

What DFP does is section out only the digital interface part of the P&D standard onto a 20-pin connector. A 15-pin legacy analog connection will also be supplied from the graphics card, but there is no support for USB or 1394. This allows PC manufacturers to transition only part of their line to digital flat-panel monitors. Moving to the full P&D standard can compel manufacturers to transition all of their monitor line—both analog and digital, flat panel, and CRT.

The DFP concept was originally developed as a subset of the P&D interface to lower the cost and supported features of P&D. Computer manufactures, like Compaq, think this approach is necessary in the early stages of digital flat-panel monitor introduction. DFP was conceived as a stepping stone to full P&D implementation, but some now view DFP as a viable competitor to P&D.

In theory, there is electrical and logical compatibility between the digital portion of P&D and DFP. They share the PanelLink technology and incorporate the Video Electronics Standards Association (VESA) display data channel (DDC) for plug-and-play monitor connection. But, the connectors are not the same. Perhaps adapters can allow both types of connectors to be used with either monitor type. But, do consumers really want to solve connection problems? More likely, they just want to plug it in and have it work.

Incompatibilities also exist between P&D and DFP in hot-swap capability, extended-display-identification data (EDID) structure, ac/dc coupling, and USB support. Some of these issues are reportedly being worked out, but not all.

The third camp, DMI, is also gearing up to confront both P&D and DFP. National Semiconductor (Santa Clara, Calif.) is leveraging their low-voltage differential signaling (LVDS) technology, which is a de facto standard for notebook computers, to produce an updated version for flat-panel monitors. The new concept, LVDS Display Interface (LDI), supports a 30-pin connector, EDID, and USB. And, don't forget about Sony's GVIF concept, which can use one-third the wires of the PanelLink or LDI approaches. Until all this confusion is straightened out, however, the effect could be just the opposite of these efforts—consumers may opt for the dependable analog interface.

Chris Chinnock holds a BSEE from the University of Colorado and reports on flat-panel displays and other emerging technologies. His company, Technical Marketing Service, provides writing, marketing, and public relations services to technology companies. Chinnock can be reached at (203) 849-8059; fax (203) 849-8069; e-mail: chrischinnock@compuserve.com.

E-Mail On The Go: Wireless Data Comes To Palmtops

Pocket organizers are a phenomenon in Silicon Valley and other high-tech enclaves across America. In both engineering and management circles, the Palm Pilot and its brethren have replaced the pocket protector and calculator (or slide rule, for us 40-somethings) as a symbol of geek macho. Due to the lack of communication capability, however, these clever little gadgets haven't realized their full potential until now. With the advent of the CONTACT palmtop computer and Minstrel wireless modem, busy people now access e-mail without a phone line or a laptop.

Novatel Wireless, Phoenix, Ariz., addressed the two major market segments of palmtop computing by offering solutions for both handheld PC users and pocket organizer devotees. The CONTACT is a full-featured Win CE palmtop/organizer, while the Minstrel is a modem adapter that turns the Palm Pilot into a wireless messaging terminal. Both employ cellular digital packet data (CDPD) technology to deliver two-way access to the Internet and other digital messaging services.

As Quick Lab's chief test pilot, I quickly jumped at the opportunity to test these little wonders. While I had hoped to test both units (I'm a big fan of the Pilot), Novatel had such a large demand for their products that I was only able to get a hold of the CONTACT HPC. While slightly bulkier than some of the really tiny HPCs I've looked at, it presents a fairly sleek package. The Hitachi SH3 32-bit processor seems to provide enough crunch to run the Win CE system and associated applications at a brisk clip.

The little unit bristles with features, including eight Mbytes of RAM, an IRDA-compliant infrared data port, a PCMCIA slot, and a 14.4 kbit/s wireline modem. A cable and synchronization software make it easy to exchange and update files with your PC. The big news, however, is the wireless CDPD modem. It sports 0.6 W of output power, enough to give reliable service in most coverage areas. CONTACT's specs claim that data can zip along at up to 19.2 kbits/s. Bell Atlantic and most other major cellular carriers offer services that support e-mail as if you were connected to a wireline service.

Although I had no way of verifying how fast I was getting my e-mail, the response time seemed good. For those so inclined, alphanumeric one- and two-way paging services are also available over CDPD.

LEE GOLDBERG
COMMUNICATIONS

Overall, my experiences with CONTACT were very favorable with a few complaints. The unit seems to be a very good platform for sending and receiving e-mail on the go. Even for a nontechnophile, it operates smoothly and easily enough once configured. But, configuration can be problematic, requiring some hand-holding from your service provider if you're not up on the intricacies of POP3 protocol. For example, I was able to easily access e-mail from the demo account provided by Novatel, but couldn't quite manage a way to get at my home account on another provider. I suspect this was simply because I didn't have the time to get in touch with the help desk for some advanced guidance.

In my month of using the CONTACT, I enjoyed the convenience of having a powerful HPC that let me handle my e-mail wherever I went. I didn't try the paging service, but I imagine it's awfully nice not to have to carry a second electronic lump on your belt.

The only two serious drawbacks I noted were the button-style keyboard (vaguely reminiscent of IBM's ill-fated PC-Junior) and the Win CE 2.0 operating system. It's tragic that such a bulky, user-indifferent piece of software is becoming as ubiquitous as its evil older brother. I can only hope the industry wises up and begins to explore the excellent alternatives available, such as the EPOC OS from Symbion. Despite these issues, I'd heartily recommend this machine to folks who need constant access to their e-mail. Just don't expect to write a novel or do a majority of your work on it.

The Minstrel modem is a hardware cradle that adds a couple of inches of length to the Palm Pilot, making it into a wireless communicator. This setup is a smart choice for somebody who doesn't need to deal with huge text files on the road. The wireless specs are the same for both CONTACT and Minstrel, so I'd guess that the Minstrel would turn the humble Pilot from an excellent organizer into an indispensable part of a busy person's life. Versions of the Minstrel are now available to support both the original Palm Pilot and the new Pilot III.

CDPD services are fairly reasonable, running from $29 a month for a basic subscription to $59 a month for unlimited use. At a list price of under $1050, CONTACT is a sizable, but affordable, investment into making life on the road less stressful and more productive. The Minstrel Costs under $450, plus the Palm Pilot itself.

For those wishing to add wireless capabilities to your laptop, Novatel also offers the Sage external CDPD modem. The compact unit plugs into your laptop's phone port and behaves just like a wired modem, delivering e-mail, remote LAN access, and Web pages at 19.2 kbits/s. At under $450, it may be an enticing upgrade for laptop owners who aren't ready to trade in their large screens and keyboards.

If you've read this far and can't wait to get your hands on one of these wireless wonders, contact Novatel Wireless Inc., 6540 Lusk Blvd., San Diego, CA 92121; (888) 888-9231, (619) 784-0620, fax (619) 784-0626, www.novatelwireless.com.

Lee Goldberg

CIRCLE 499

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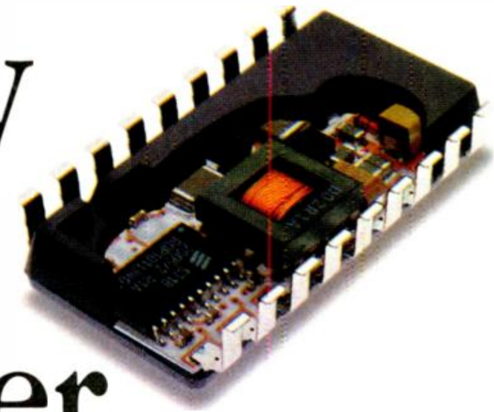

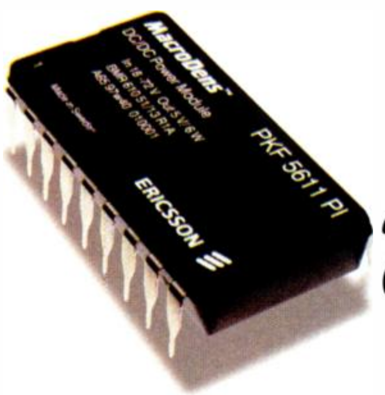

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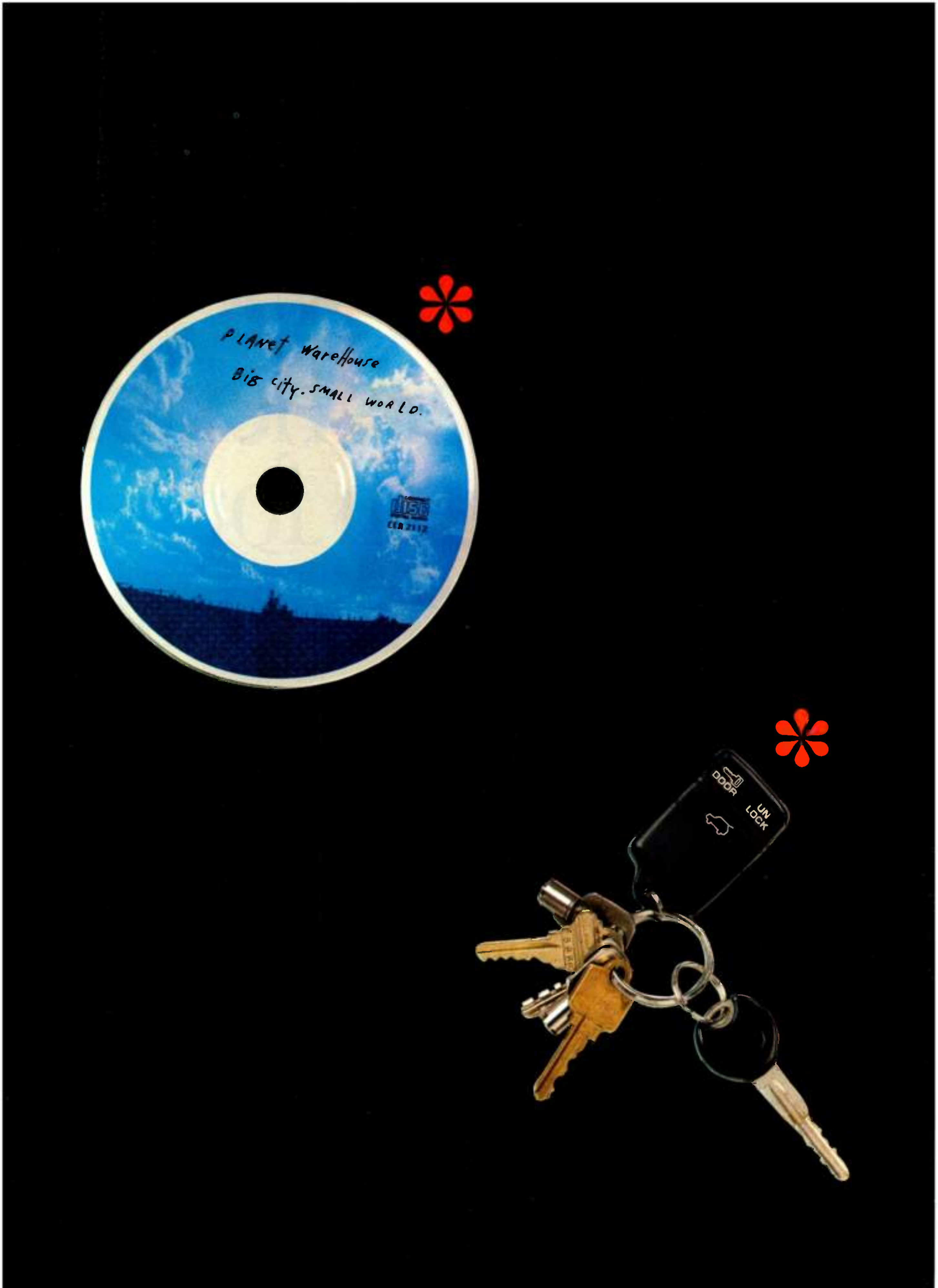
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High-Resolution ADC Targets Precision Data-Acquisition Applications

This Tiny Package Attains 24-Bit Accuracy By Combining A Third-Order Delta-Sigma Modulator With Digital Filtering.

Ashok Bindra

Momentum keeps building, pushing toward the next level of precision and accuracy in instruments, industrial-control tools, weighing scales, temperature monitors, and many other such data-acquisition products. Manufacturers of these precision tools continue to offer higher performance at lower cost, with reduced power consumption and, above all, in compact, elegant housings. The components constituting such products, like the semiconductor ICs, must advance at the same pace, if not faster. The analog-to-digital converters (ADCs) at the forefront of these systems, meanwhile, bear the maximum brunt of this challenge.

COVER FEATURE

Suppliers of high-performance ADCs are constantly under pressure to improve the speed, accuracy, and functionality of these parts without adding to the cost of the device. Meanwhile, they have to make sure that power dissipation is lower, and the solution's easier to implement. As a result, designers of high-resolution ADC ICs are optimizing analog CMOS processes. To achieve the end goal, they are combining these improvements with novel architectures and clever circuit designs.

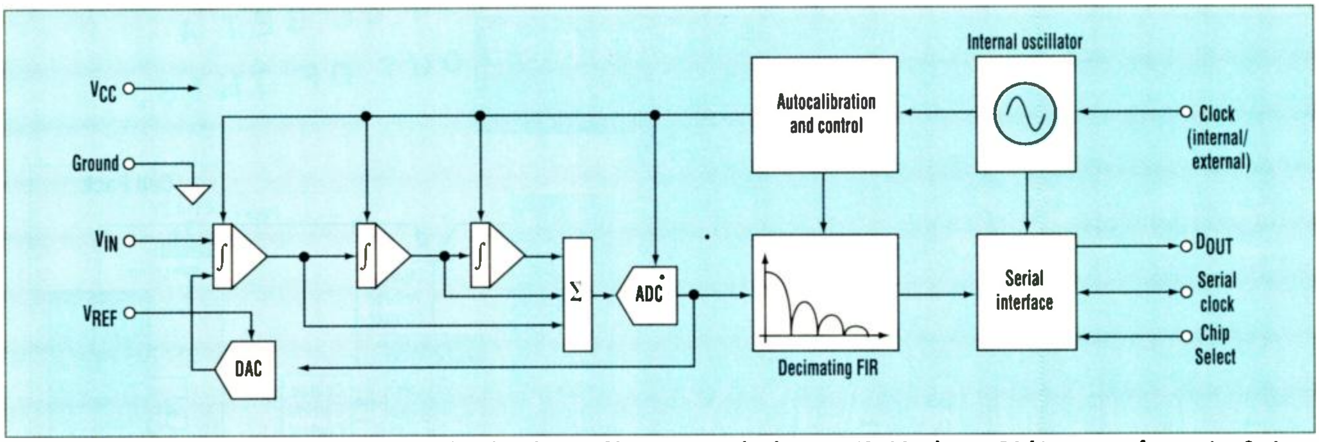
24-Bit ADC

Linear Technology Corp. (LTC) is no exception. This key supplier of analog and mixed-signal parts has made substantial enhancements to its 2-µm, single-metal analog CMOS process. In addition, the company has developed a third-order delta-sigma (Δ-Σ) modulator, and acquired digital-filtering capabilities. Implementing these capabilities in an optimized CMOS process, LTC's designers have crafted a high-performance, 24-bit ADC that is small enough to fit in a tiny, eight-lead small-outline package (SOP). As per the manufacturer, the die size of the new 24-bit ADC, the LTC2400, is under 10 kmils^2.

With the announcement of the LTC2400, LTC also expands its entry into the growing Δ-Σ-based ADC marketplace. Until now, the manufacturer focused on conventional, successive-approximation-register (SAR) ADCs. According to LTC, the LTC2400 is the first member of a family of Δ-Σ ADCs. "This new ADC offers a combination of the best characteristics of Δ-Σ and conventional converters," states Todd Nelson, product marketing engineer at LTC.

The optimized CMOS process actually enabled LTC to pack several important functions on-chip, such as a serial interface, a highly accurate oscillator, autocalibration, and control. It also provides many flexible modes of operation *(Fig. 1)*. In short, this integrated, 24-bit ADC is simple to use. The on-chip oscillator eliminates the need for an external crystal. The converter's small footprint, with minimum external components, permits the user to greatly reduce the board area of existing designs.

The LTC2400 is designed to offer excellent integral non-linearity (INL), differential non-linearity (DNL), noise, and rejection performance. It offers 24-bit DNL with a guarantee of no missing codes. Plus, the INL is a mere ±2 ppm or 0.0002% *(Fig. 2)*. "The DNL and INL performance defines



1. Combining a third-order Δ-Σ modulator with a fourth-order Sinc filter, Linear Technology's LTC2400 achieves 24-bit accuracy from a tiny 8-pin SOP package. Additionally, the 24-bit converter also offers many other bells and whistles to simplify its use.

the accuracy of the LTC2400," states Nelson. The company attributes this performance to feed-forward compensation and analog processing techniques employed within the higher-order modulator. "Plus," he adds, "the 1-bit ADC and DAC in the feed-forward path of the modulator guarantee monotonicity and exceptional performance of 2 ppm. In addition, the converter's noise characteristics is only 0.3 ppm." With this kind of performance, it resembles a digital voltmeter on a chip, claims LTC.

Decimating Filter

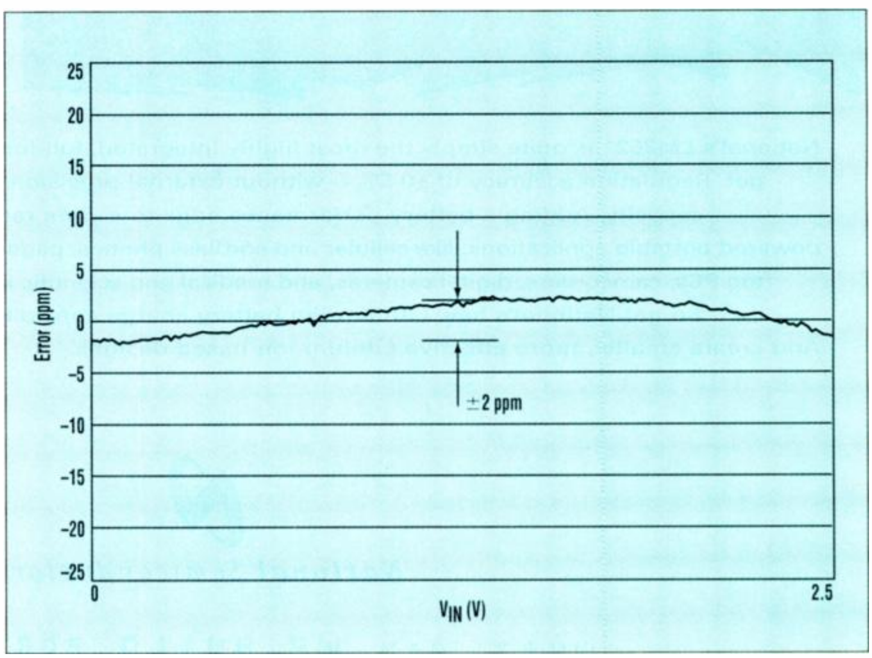
To achieve excellent line rejection, the LTC2400 ADC incorporates a fourth-order Sinc filter. In essence, the output of the Δ-Σ modulator is applied to the Sinc4 decimating digital filter, which removes the quantization noise from the modulator output. Besides decimating the output of the modulator, this fourth order Sinc4 filter attains at least 120 dB rejection of line frequency ±2% *(Fig. 3)*. "This level of line rejection is unheard of with other architectures, especially SAR or flash types," says Nelson.

Another highlight of the LTC2400 is the filter's notch frequency. It's set by the on-chip oscillator, "typically the line frequency for dc applications," adds Nelson. In order to achieve good line rejection, current Δ-Σ converters require an accurate external oscillator or crystal with a precise, uncommon value. "The LTC2400 addresses this problem by providing an accurate on-chip oscillator," notes Willie Rempfer, design manager for the data converter group at LTC.

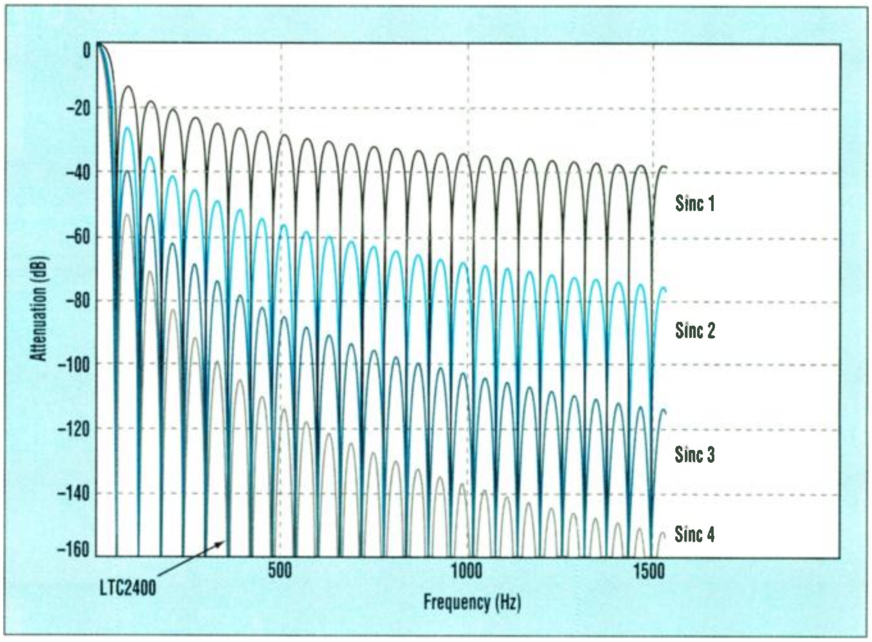
Rempfer adds, "The internal oscillator of the LTC2400 is so precise, the ADC rejects line frequency over a 2% range, independent of supply or operating temperature. Since line frequencies can vary up to 2% over a 24-hour period, converters using lower-order Sinc filters cannot achieve 120-dB rejection, even with exact external oscillators." According to LTC, the designers have also combined proprietary algorithms with serial logic and new methodology, keeping the size of the Sinc4 filter substantially smaller.

While traditional converters utilize bypass capacitors to minimize noise, the LTC2400's design eliminates such a capacitor on the supply pin. LTC attests that large noise errors applied to V_{CC}, V_{REF}, or V_{IN} pins have no effect on the ADC's noise and linearity performance. "Superior noise rejection, coupled with the design of the chip, allows the use of a single supply pin, a single ground pin, and a single-ended input," explains Rempfer. In addition, the internal oscillator further minimizes the number of device pins. The design was completed with only 8 pins, thereby minimizing the total pin count of the 24-bit converter.

The user also gains other advantages. For example, the V_{REF} can be tied directly to V_{CC} without compromising performance. There's also a simple, serial-peripheral-interface



2. Integral non-linearity (INL) for the converter is a mere ±2 ppm, or 0.0002%. It is designed to offer 24-bit differential non-linearity (DNL) with a guarantee of no missing codes.



3.The Sinc4 filter enables the 24-bit ADC to achieve a line rejection of 120 dB. Line frequencies of 50 or 60 Hz are selectable simply by tying the clock pin to V_{CC} or ground.

(SPI) compatible three-wire output. It can output data with a single-cycle setting. This technique gives the user a one-to-one correspondence between the start of a conversion and the output word. It simplifies the user interface by eliminating latency and redundant data normally associated with Δ-Σ ADCs.

Self-calibration, another key feature, is transparent to the user. The LTC2400 continuously executes self-calibration algorithms, enabling the high accuracy converter to automatically adjust the offset and full-scale. The worst-case offset is ±2 ppm, while the maximum full-scale error is 5 ppm. Typically, the offset error is ±1 ppm, as per LTC's data sheets.

Flexible Modes

The power-supply range for the new ADC is 2.7 to 5.5 V, with a reference voltage range of sub 10 mV to V_{CC}. At V_{CC} = 3.0 V, power consumption is just 750 µW. And, in the power-down mode, the 24-bit LTC2400 consumes only 45 µW.

In many data-acquisition applications, the input signal may exceed V_{REF} or fall below ground. To address this undesirable condition, the LTC2400 provides on-chip over-range circuitry. As a result, it continues to output 24-bit valid data for an effective input range of up to –12.5% of V_{REF} to +112.5% of V_{REF}.

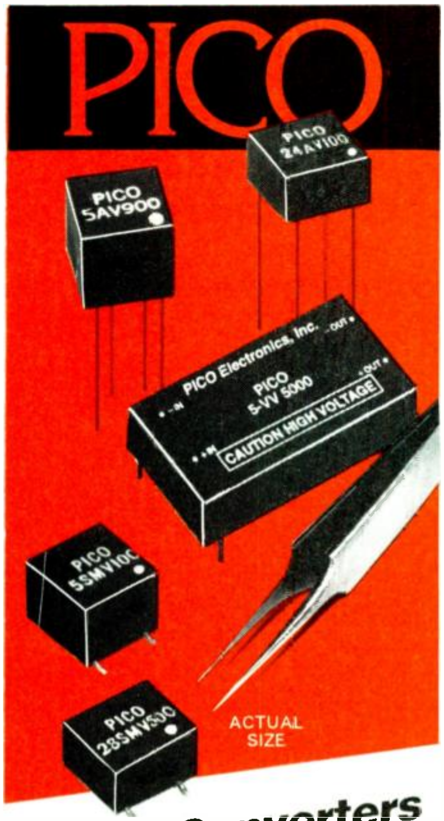
According to LTC, applications employing conventional ADCs can easily migrate to the Δ-Σ–based, 24-bit LTC2400. Single-cycle setting enables the user to place a multiplexer in the front of the converter without worrying about the latency or data being statistically dependent on previous conversion results. Plus, the 120 dB rejection of line frequency noise and its harmonics makes the converter suitable for noisy environments.

Furthermore, the converter is architected to furnish many flexible modes of operation. For instance, a capacitor tied to the Chip-Select (CS) pin provides a power-down mode. In fact, under this configuration, the LTC2400 performs one conversion, and then automatically enters the power-down mode, which is proportional to the value of the capacitor. Also, this ADC can operate with internal or external serial clock. The LTC2400 detects the state of the serial clock pin to switch the ADC to internal or external clock modes.

Price And Availability

Housed in an 8-pin SOP package, the LTC2400 is in production. In quantities of 1000 units, it's priced under $10.00. An evaluation board that plugs into the serial port of the PC is also available.

Linear Technology Corp., 1630 McCarthy Blvd., Milpitas, CA 95035; (408) 432-1900; www.linear-tech.com. **CIRCLE 519**



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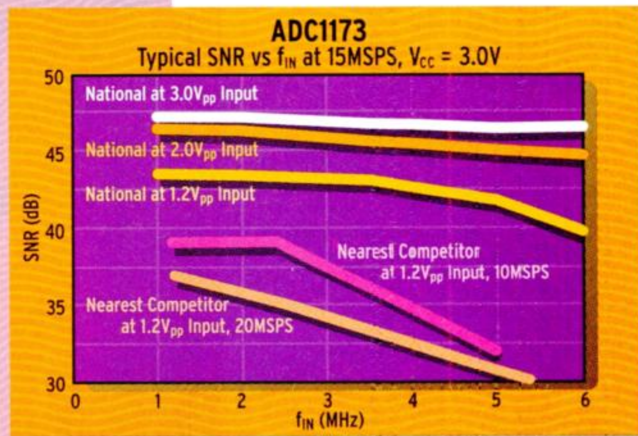

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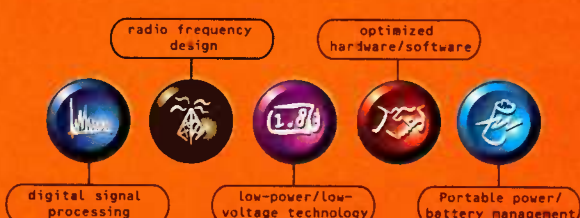

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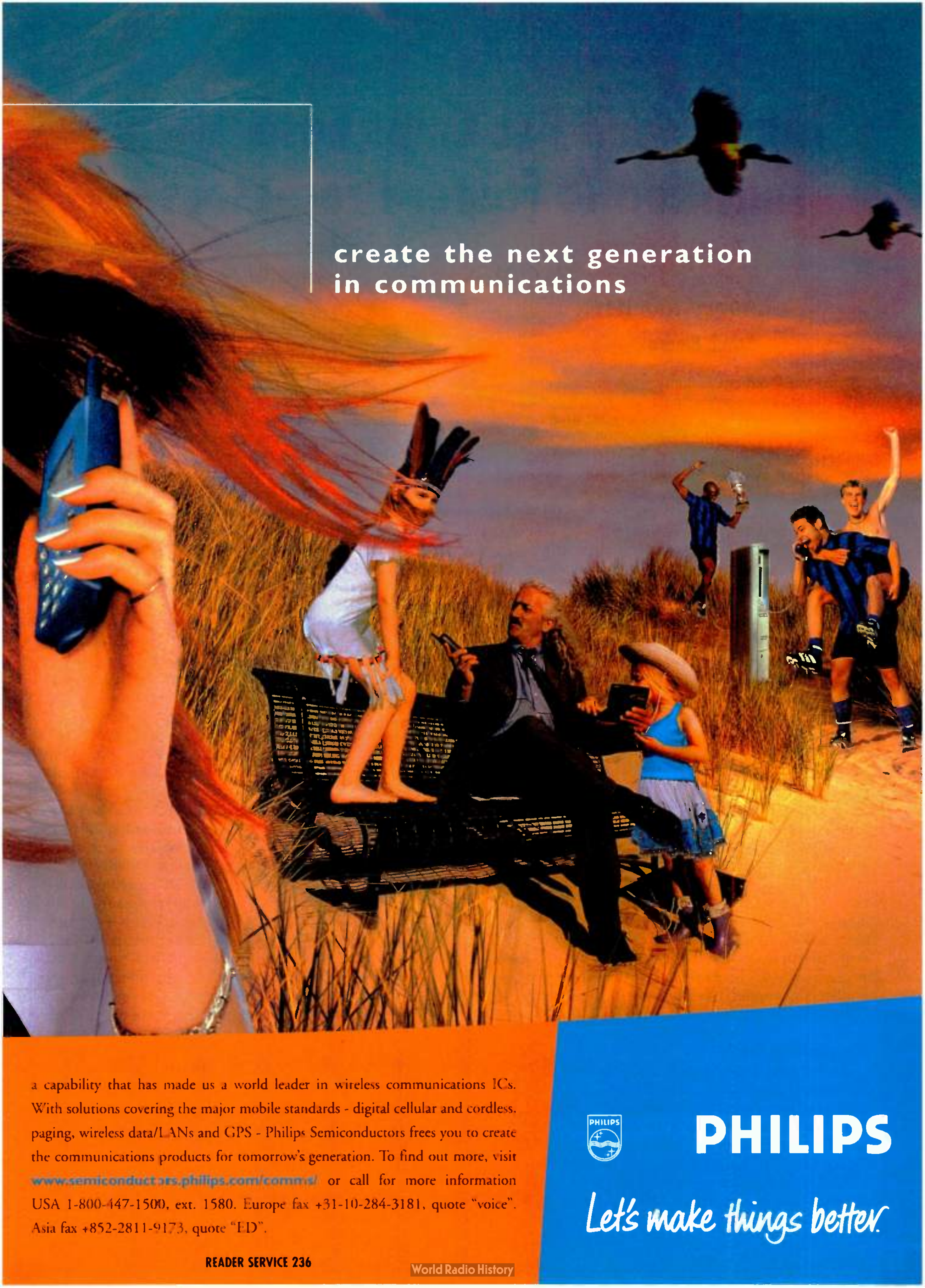
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High-Speed PLL Chips Ease Transition To Faster Processors

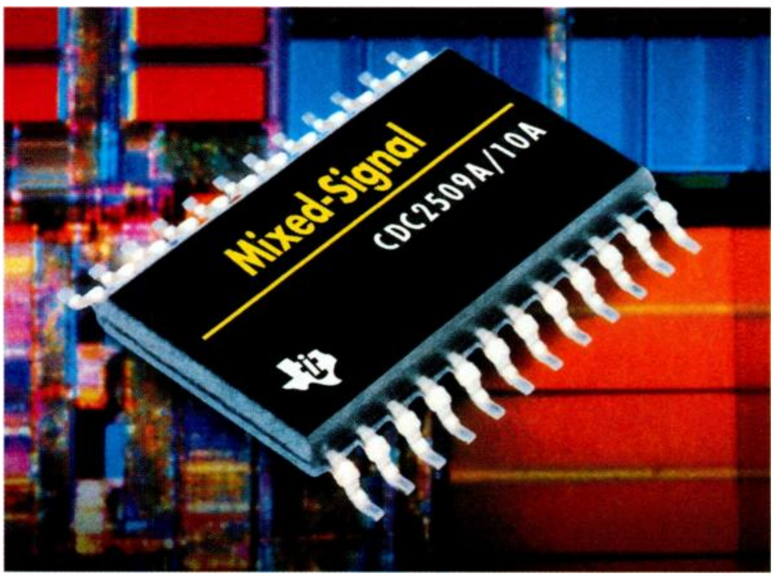
Phase-Locked-Loop-Driven, Clock-Distribution Devices Ensure Precise Data Access And Storage At Speeds Above 100 MHz.

Ashok Bindra

SPECIAL REPORT

As the PC industry adopts faster processors, the interface between the microprocessor and data-storage modules must also be equally fast to handle data rates of 100 MHz and higher. Consequently, the clock-distribution scheme that provides the timing signals to the memory modules and other functions must be fast, precise, and accurate. In fact, these high-speed PC systems are demanding low-skew, low-jitter copies of clock signals that are perfectly synchronized. In this way, they ensure reliable data access and storage at frequencies above 100 MHz.

To meet such stringent requirements, as well as those imposed by Intel's PC-100 high-speed bus specifications, semiconductor suppliers have readied standalone phase-locked-loop (PLL) based clock generator ICs. These provide perfectly timed, clock-distribution circuits for use with high-speed synchronous DRAM modules. In addition, these high-performance PLL chips are also employed to generate multiple system clocks from a single reference input frequency for multimedia applications, such as DVD players, DVD cards for multimedia PCs and HDTV.



Art Courtesy:Texas Instruments Inc.

Distributing Clock

Analog and mixed-signal IC manufacturers like Texas Instruments Inc., Hitachi Semiconductor (America) Inc., Pericom Semiconductor Corp., and Burr-Brown Inc., are among the early ones to respond to such high-speed, clock-distribution needs for the new SDRAM memory modules and multimedia systems. Others eying standalone PLL ICs for clock-distribution schemes include Integrated Device Technology (IDT) Inc. and Quality Semiconductor Inc.

Specifically developed for use with synchronous DRAM chips, TI has released PLL clock drivers that push the speeds up to 125 MHz. Compliant with PC-100 specifications, TI's clock distribution circuit series includes the CDC2509/2510/2516. While the 2509 is designed to offer nine low-skew, low-jitter copies of the input clock, the 2510 and 2516 are crafted to provide 10 and 16 precise signals aligned in both phase and frequency (*Fig. 1*). These clock-distribution circuits also support spread-spectrum modulation of timing signals, a technique that reduces the system's EMI. Version A is designed to support this capability. For applications that can tolerate some EMI, TI also offers versions without spread-spectrum techniques implemented on chip.

"Because the phase error needed for clock signals is very stringent as called for in the PC-100 specifications, it was necessary to design PLL-based clock-distribution chips as separate solutions," states Sameer Vuyyuru, worldwide marketing manager for TI's CDC business. "Long interconnect delays did not permit the use of conventional ways to connect clock signals to high-speed SDRAM chips," he adds. "Plus," he continues, "the high-speed PLLs are extremely sensitive to noise. Consequently, standalone PLL-based clock-distribution and generation circuits were created to be compatible with PC-100 specifications." According to the data sheets, the maximum phase error for these devices is ±150 ps.

Low-Skew, Low Jitter

While the CDC2509 and CDC2510 PLL clock

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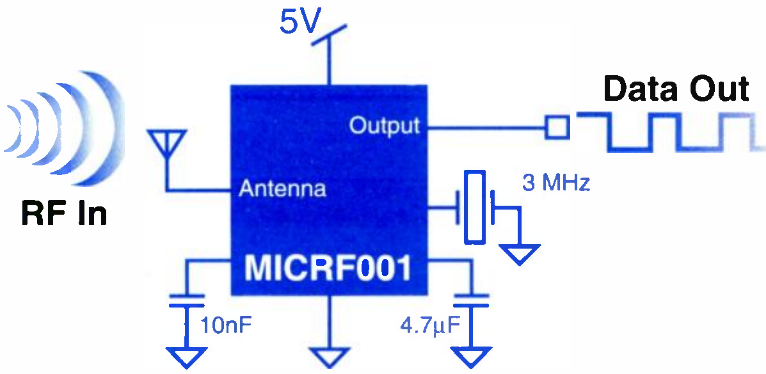

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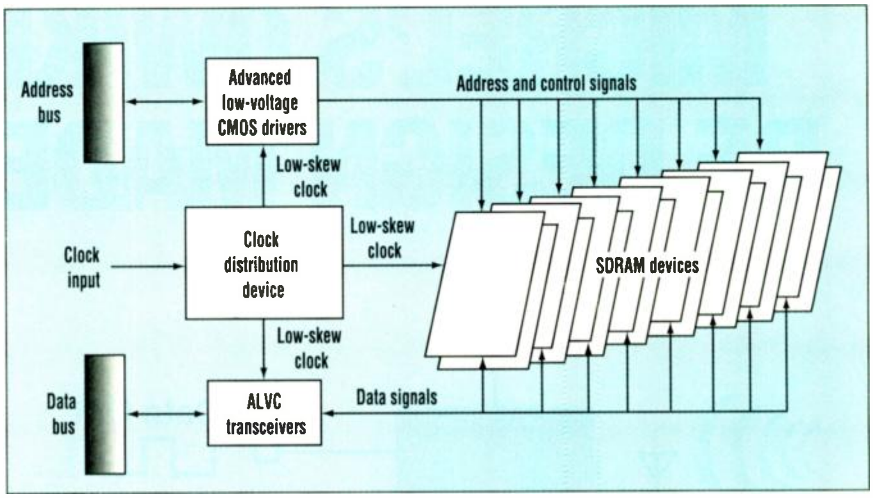
drivers are each designed to offer outputs in two banks and 1 bank, the CDC2516 is crafted to provide four banks of four outputs, for a total of 16 low-skew, low-jitter copies of the input clock. There is a separate output enable/disable control input for each output bank. For instance, CDC2509 offers two control inputs to control one bank of five outputs and the other of four outputs for a total of nine. Unlike others, CDC2510 provides only one bank of 10 outputs.

Additionally, an external feedback pin (FBIN) ensures synchronization of the clock outputs to the clock input. According to TI, unlike other PLL-based clock generators, these parts do not require external RC networks. The loop filter for the PLL is included on-chip, minimizing component count, board space, and cost. Furthermore, the output-signal duty cycles are adjusted to 50%, independent of the duty cycle of the clock input.

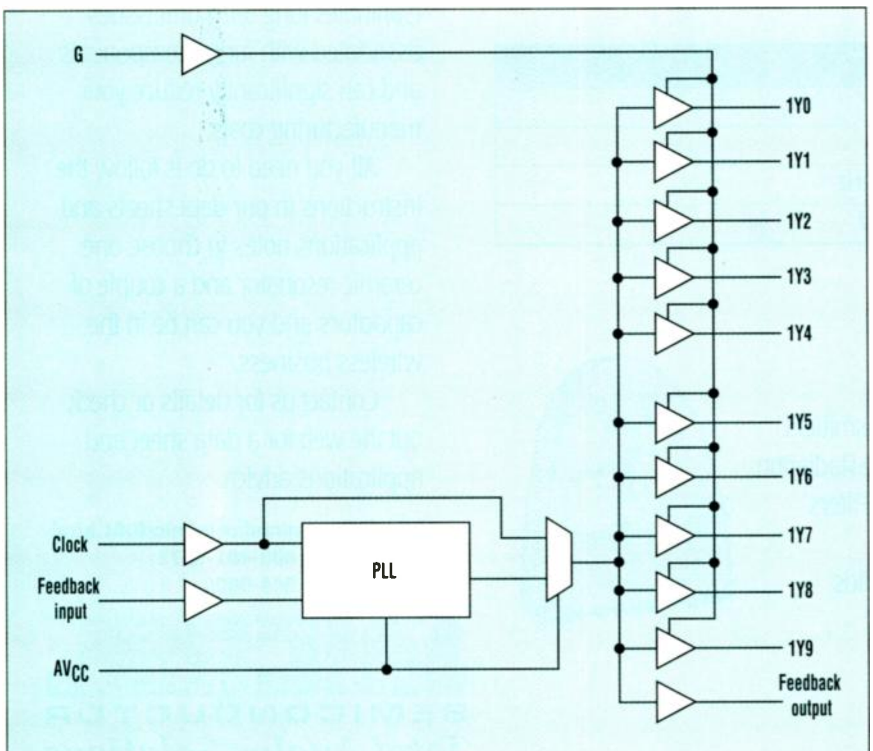
To achieve phase locking of the feedback signal to the reference signal, the CDC2509/2510/2516 PLL-based clock-distribution circuits require stabilization time. As per the manufacturer's data sheets, this time is required following the power-up stage and the application of a fixed-frequency, fixed-phase signal at the clock input. Additionally, following any changes to the PLL reference or feedback signals, the circuits need time for stabilization. This takes about 1 ms after power-up.

Based on a 0.5-µm CMOS process, the PLL clock driver chips operate at 3.3 V, and are available in thin, shrink small-outline packages (TSSOPs). The CDC2509/2510 ICs are housed in 24-pin TSSOPs, and the CDC2516 comes in a 48-lead TSSOP. Meanwhile, TI plans to push the speed of these devices to 133 MHz. While the A version is rated for upto 100 MHz, the B version can go upto 125 MHz clock speed, with better jitter and phase error characteristics.

On another front, TI has also announced support for Direct RAMbus technology in system memory. To that end, TI is readying a new line of PLL-driven clock generators capable of supporting Direct RAMbus data rates of 1.6 Gbytes/s. "This indicates our commitment to providing next-generation clocking solutions for memory," says TI's Vuyyuru.



2. Hitachi's PLL clock-distribution devices are used to route clock signals to the memory and logic chips in the SDRAM DIMMs. These devices meet a ±100 ps jitter specification as per PC-100.



1. Compliant with PC-100 specifications, Texas Instruments' CDC2510 is a low-skew, low-jitter, PLL-derived clock-distribution chip with ten outputs. It pushes the clock speed up to 125 MHz.

More Sources

Also in the race to deliver PLL-based, clock-distribution devices are Hitachi Semiconductor and Pericom Semiconductor. In fact, Hitachi's HD74CDC2509A/2510A are pin compatible with TI's CDC2509A/2510A. In reality, Hitachi is second sourcing TI's CDC2509/2510 devices.

Featuring a low-skew PLL design, the Hitachi clock-distribution chips use advanced low-voltage CMOS (ALVC) logic technology implemented in a 0.4-µm process. According to Hitachi, these devices meet the critical ±100-ps jitter specification required on the PC-100 registered SDRAM dual-in-line memory modules (DIMMs). However, "they are designed to perform better than ±100 ps jitter," claims Hitachi's product marketing manager, Jim Shupenis. Like

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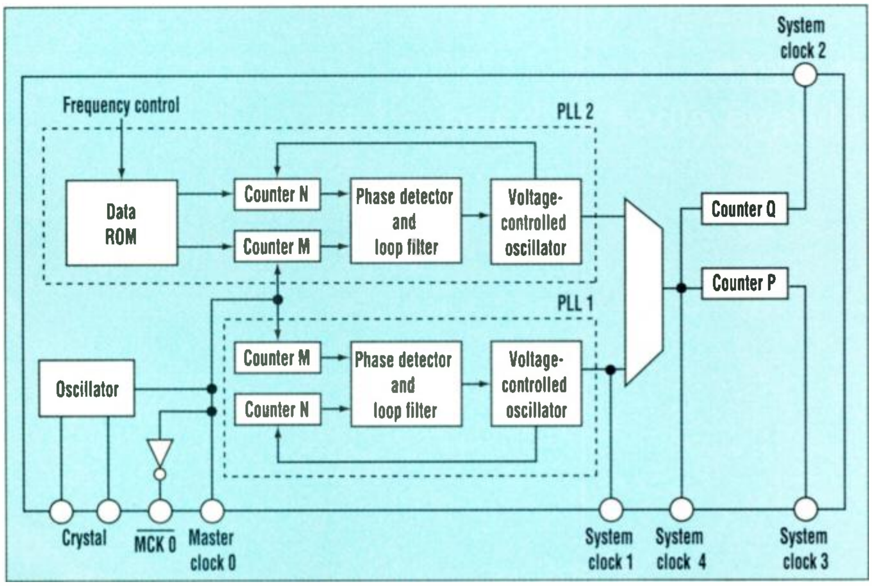

3. Burr-Brown's PLL1700 is a programmable device that can generate four system clocks for multimedia systems. It accepts a 27-MHz reference clock input.

TI's chips, Hitachi's PLL units also support spread-spectrum clock synthesizers used on registered DIMMs. The outputs are LVTTL-compatible for easy interfacing.

According to Shupenis, "for high-speed, memory module applications, the 3.3-V HD74CDC2509A/2510A ICs ensure the fidelity of the clock waveform and its timing, as that signal is routed through the module's memory chips, signal drivers, and transceivers. They also minimize the loading on the memory controller, which helps to maintain proper controller operation."

"For high-end workstations and servers, registered modules using PLL clock-distribution devices are the only means available to meet their needs for very large main memory," says Brett Etter, DRAM product marketing manager at Hitachi Semiconductor." Notes Etter, "These PLL devices give OEMs the capability to create modules that perform reliably at 100-MHz clock speeds."

The nine-output HD74CDC2509A is targeted at 64- and 128-Mbyte PC-100 compliant SDRAM DIMMs *(Fig. 2)*. The 10-output HD74CDC2510A is aimed at 256- and 512-Mbyte DIMMs. Like TI, Hitachi is also producing the B versions of these units. Concurrently, it's also readying faster PLLs, as well as exploring designs with differential outputs. These designs are being investigated for next-generation memory modules with almost twice the data rate.

Pericom Semiconductor also recently announced its entry into this camp. The mixed-signal maker has unveiled two new, near-zero-delay, PLL clock drivers to support Intel's PC-100 DIMM standard. To comply with the standard, both the PI6C2509A and PI6C2510A utilize Pericom's advanced PLL technology. They provide near-zero-delay clock distribution at speeds up to 133 MHz. However, current parts are rated for 100-MHz clock speeds. The 133-MHz versions are in the works, with plans to go into production when this article goes to print. Pericom's designers are also in the process of extending this speed to 150 MHz and above. The 150-MHz models are slated for release by the year's end, according to Ken Buntaran, Pericom's director of strategic marketing.

Present PLL clock circuits meet critical specifications of ±100 ps maximum for jitter, and offer very-low phase error of ± 150 ps maximum. "Our new PLL clock drivers are critical components to ensure reliable operation at 100 MHz of registered DIMM modules used in workstations and servers," says Buntaran.

In fact, Pericom is looking beyond memory module applications. The company is planning to tailor its PLL-based clock-distribution circuits for use in networking and printer products, as well as multimedia systems. For those applications, Pericom has readied PI6C9930 and PI6C9910. Capable of providing eight synchronized outputs of the reference input, the PI6C9930 incorporates a divide-by-two function to deliver slower secondary clocks for peripheral devices.

For instance, when the Q_0 output is connected to the feedback input, the outputs Q_1 - Q_7 provide seven copies of the reference input. Similarly, when one of the Q_1- Q_7 outputs is connected to the feedback input, the Q_0 is twice the reference input, while all other outputs are identical to the reference input. The PI6C9910 provides eight clock copies of the reference input, but the specs are more relaxed. It is de-

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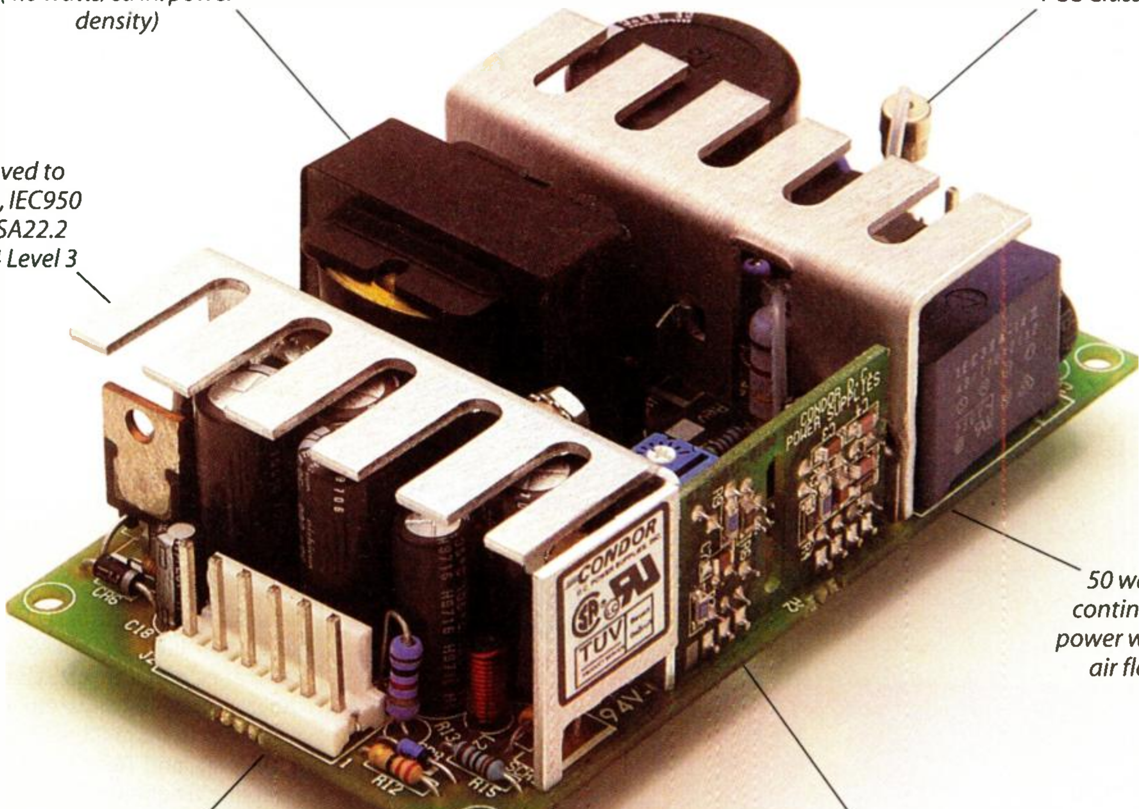

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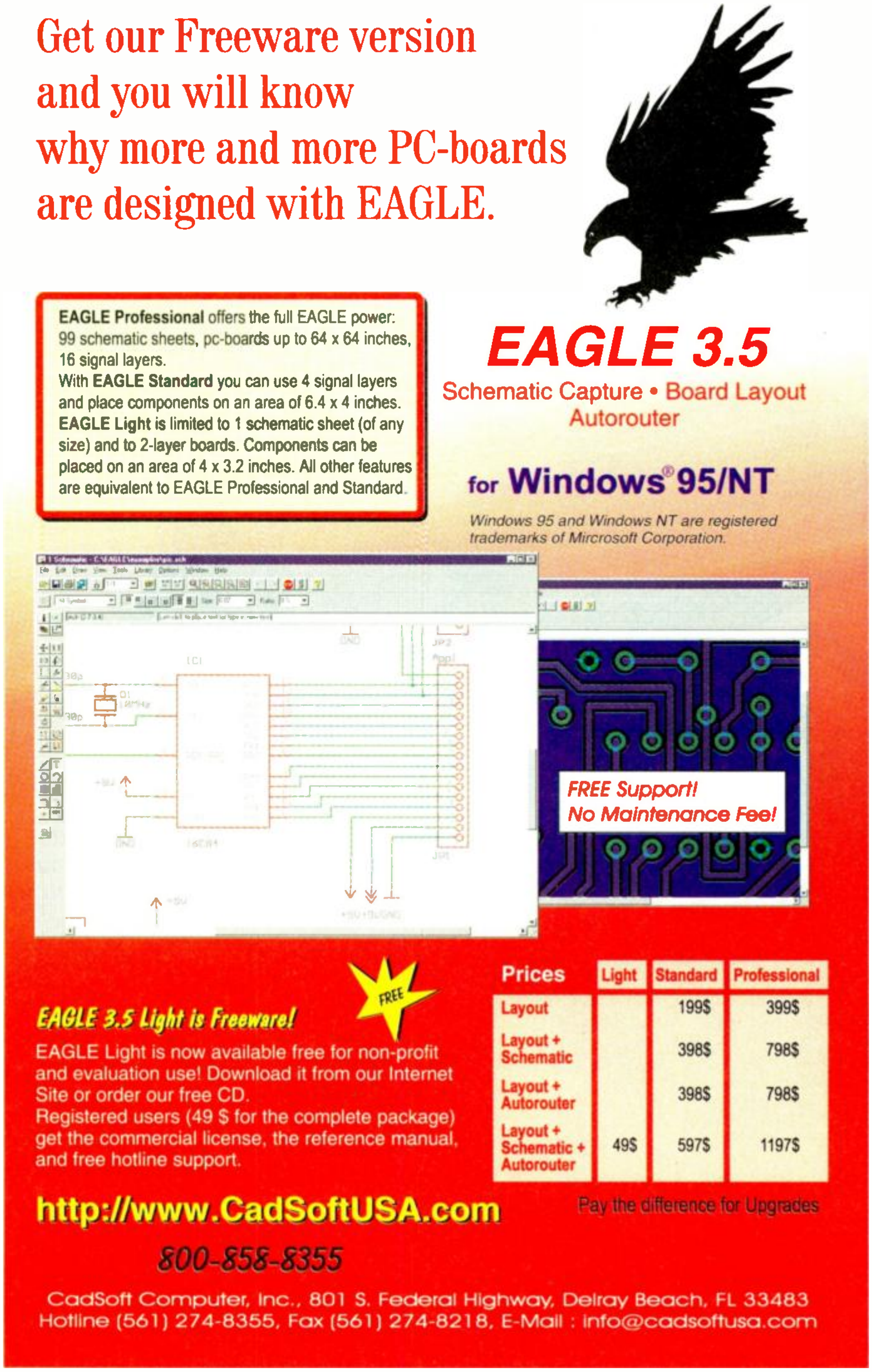

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signed to offer jitter of about 200 ps (peak-to-peak). The parts are crafted for operation between 15 to 80 MHz.

Not far behind is IDT. Implementing clever, PLL-based clock-distribution schemes in 0.5-µm CMOS processes, IDT has disclosed the first results of this effort. The CSP2509A with nine outputs is PC-100 compliant, with pinouts similar to those of TI's CDC2509A. "The CSP2509A's jitter is significantly lower than what the PC-100 specifications call for," says IDT's director of marketing Tony Walker. According to IDT, jitter is as low as 10 to 15 ps.

Meanwhile, IDT is readying the 10-output CSP2510A version , which is expected to be introduced in the fourth quarter.

System Clocks

In many multimedia applications, multiple clocks are needed. And, these clock frequencies must be precise with extremely low jitter. Plus, the master clock must be synchronized with the multiple system clocks. The standalone PLL circuits have come to play crucial roles in these high-performance audio and video systems.

To address these issues, Burr-Brown has unveiled a programmable PLL clock generator, the PLL1700, for DVD players, DVD cards for multimedia PCs, digital HDTV, and digital set-top box (STB). Using a 27-MHz reference clock input, the PLL1700 can generate four system clocks (*Fig. 3*). These include 33.8688 MHz, 256 × f_S, 384 × f_S, and 768 × f_S, where f_S is the sampling frequency. The sampling frequencies can be 32, 44.1, 48, 64, 88.2, or 96 kHz. Clock jitter for this circuit is 150 ps. Operating at +5 and 3.3 V, the PLL1700 comes in a 20-pin SSOP.

"For high-performance DVD systems, we recommended keeping the PLL clock generation circuit separated," notes Mike Centorino, Burr-Brown's manager for audio products . "This prevents any synthesized clock noise from coupling onto the analog portion of the digital-to-analog converter [DAC]," he adds. By generating all the necessary system clocks for the AC-3 decoder and the high-quality DAC in the DVD system from the reference input, the PLL1700 alleviates digital noise coupling to substantially boost the product's performance.

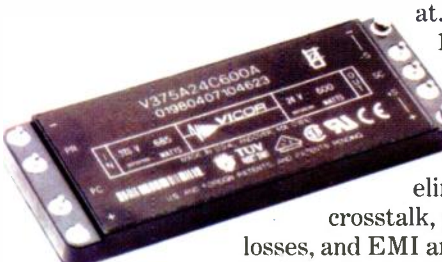
Pride of Ownership: The Path To A Successful Design

With Power Quality Now A Major Concern, Customer Satisfaction Has Ramifications Way Beyond "Just Meeting The Specs."

By Patrick Mannion

PATRICK MANNION
Power, Packaging, & Components Editor

OK, you've finally completed the project on time, and only slightly over budget—but it's worth it. You've got the best power distribution system money can buy. You've used second-generation, high-efficiency converters, and strategically placed the latest tweaked-out buck regulators. These are supplying banks of low-equivalent-series-resistance, high-stability capacitors across widely spaced, parallel power lines on a stripline board armed with more grounds than you can shake a stick at. All to deliver those 10- to 30-A, fast-switching currents right to the load, on demand.



You've all but eliminated noise, while crosstalk, parasitics, inductive losses, and EMI are a distant memory. You've got UL, CSA, TUV, and VDE approvals, and the CE mark is pending. It's beautiful, a work of art, and you're feeling pretty smug. You can't wait to show it off.

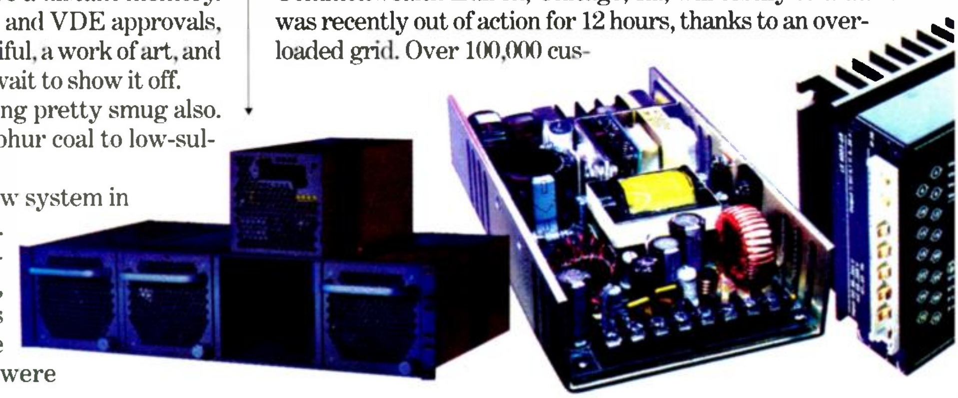
Not far away, someone else is feeling pretty smug also. They've just switched from high-sulphur coal to low-sulphur coal.

Two days later you fire up your new system in front of your first potential customers. You smile to yourself as the system cycles through its diagnostic routines, and delivers the expected green lights at every stage. They said it couldn't be done. The regulation requirements were too tight, the currents too high, and the voltage levels too varied. But here it is, working like a charm. Then, lights out. Everywhere.

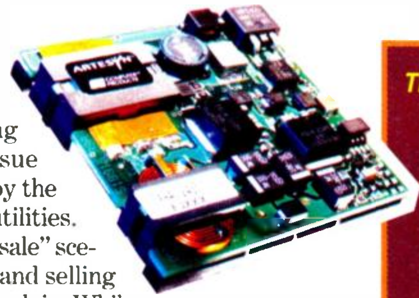
In the darkness, you hear a crash. When the emergency generator finally kicks in, you see that during the unsupervised power-down sequence, the serum-transfer arms collided, sending one crashing down into the optics—destroying the core of the system. As the visibly upset, not-so-potential customers file out, you're not feeling very smug anymore.

Neither is the manager of the nearby power plant where the fine coal dust, generated by the low-sulphur coal, has just exploded, cutting the power to over 25 customers in the immediate area, including you.

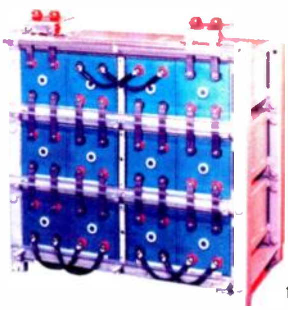
Such was the case at the Stateline power plant in Hammond, Ind., during July. As a result of that explosion, the third one of its kind in three months, many companies were left dangling. Such blackouts are not unusual, unfortunately. Commonwealth Edison, Chicago, Ill., will testify to that. It was recently out of action for 12 hours, thanks to an overloaded grid. Over 100,000 cus-



tomers were affected.



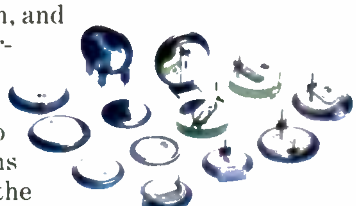
Such incidences raise many questions concerning the quality of power coming into any given site. The issue has only been exacerbated by the recent deregulation of the utilities. This has led to a "power-for-sale" scenario, with brokers buying and selling power to startups eager to cash in. While this may seem like a good idea in the context of our free-market economy, where competition theoretically leads to a happier customer, there is the little matter of infrastructure. With established utilities holding back on infrastructure support and maintenance, the already over-extended grid is only going to get worse as electronic systems and devices proliferate. With poorly financed startups now taking over in the hopes of a windfall, where is the necessary support going to come from?



Until the initial shakeup is completed, and the smaller fish have been eaten by the bigger ones, the outlook is bleak with regard to the quality of power coming into both industrial and domestic sites. And the situation is not expected to improve for at least another 10 years.

All of these problems are, for the most part, man-made. Another category of problems can be blamed on "acts of God." Ranging from lightning strikes, to car crashes and ice storms, these acts occur on a daily basis. Any one of them can put a power grid out of action. And if someone tells you that lightning doesn't strike twice in the same place, don't believe them. I personally have had two modems "nuked" in this way. So I'm ready to believe present estimates that put the number of power-related disturbances in a typical computer system at about 120 per month.

Backup Options



So between God, man, and coal dust, what's the overworked, underpaid, and obviously concerned designer supposed to do? The solutions are as varied as the problem itself, and they range from voltage suppressors, to uninterruptible power supplies (UPSs), to gas generators. With numerous options in between, the path taken boils down to a simple balance of cost of protection against the consequences of system failure.

If you're designing a computer system for home use, where games, Internet surfing, and basic word processing are the extent of the mission, there is little incentive (or room) to add cost through extensive power backup sys-

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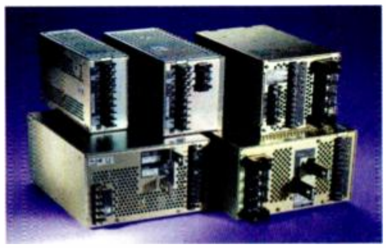

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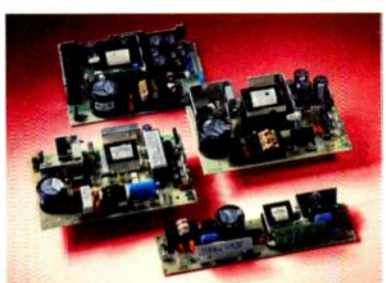

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- PC card style for OEMs.
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tems. Simply advising the buyer to purchase a surge suppressor will at least protect the hardware (your end).

This is the bottom rung of the protection ladder, and as such, it is served by a slew of products from any number of companies. Some are reputable and reliable, but most you wouldn't trust with last year's laptops. Two companies at the top of their game are Tripp Lite, Chicago, Ill., and American Power Conversion (APC), West Kingston, R.I. Known for its Isobar line of line-, and now data-protection devices, Tripp Lite is no stranger to power management. Neither is APC, which has a loyal following for its PowerManagement and SurgeArrest lines.

The next rung of the protection ladder is where many designers face their first real decision in the context of power protection. Here they must decide whether or not to provide battery backup. They can either include it in the form of an internal UPS, or let the customer purchase their own protection and backup as a peripheral. While this is an old debate, it has taken on a new face in light of the smaller form factors and higher-power batteries with longer run times. These improvements make internal UPSs a much more attractive option than they used to be.

Essentially, battery-backed switch-mode power supplies (SMPSs), internal UPSs are being offered by companies such as Technology Dynamics, Bergenfield, N.J., and Amsdell, Richmond Hill, Ontario, Canada. An interesting variation on the internal UPS is the Power Card from Guardian On Board, Austin, Tex. The device comprises a bank of NiCd batteries on an ISA or PCI board that simply plugs into the motherboard.

Regardless of the format, or how interesting the design, the old argument still stands against an internal UPS: Who wants to put a battery, which is destined to fail at some stage, inside a system that no one wants to open?

For now at least, most designers are content to leave it to customers to purchase their own backups. And there's no shortage of options for them. Between standby and online UPSs, Tripp Lite and APC are joined by the likes of MGE UPS Systems Inc., Costa Mesa, Calif.; Para Systems Inc., Carrollton, Tex.; Liebert Corp., Cleveland, Ohio; and Clary Corp., Monrovia, Calif. All offer a range of systems to cater to most system users, from the home office to mid-size systems in more crucial operations such as networking for telecommunications and financial institutions.

It is in this mid- to large-operation environment that some of the more interesting changes are taking place. This is also where designers can take advantage of recent developments to really make a value-added difference in their design. The key is software. With recent advances, such as Tripp Lite's PowerAlert Version 10.0, and LanSafe III/FailSafe III V4.0 from Exide Electronics, Raleigh, N.C., users can remotely monitor a system, and constantly get updates on its status, either over the phone line or over the web.

So, looking beyond the regular computer, designers who want to add value to any new system can include a power-monitoring UPS that will immediately notify them of potential problems or failures of a system in the field. And, who knows, if the battery is big enough, you might even get to the system before the failure becomes catastrophic. Now that's technical support.

While UPSs have their place in any environment where data integrity is essential, there is another route to reducing system downtime. Always expensive, system downtime has been estimated to cost anywhere from $1000 to $50,000 per hour, depending on the facility. Of all the causes of downtime, power disturbances, are, coincidentally, number one at 45.3% *(see the table)*. To help alleviate the problem, APC offers its Power Audit service.

MOST COMMON SYSTEM DOWNTIME CAUSES	
Power failure/surge	45.3%
Storm damage	9.4%
Fire or explosion	8.2%
Hardware/software error	8.2%
Flood and water damage	6.7%
Earthquake	5.5%
Network outage	4.5%
Human error/sabotage	3.2%
HVAC failure	2.3%
Other	6.7%

Source: Contingency Planning

Based on the premise that the National Electrical Code (NEC), which is primarily focused on safety, is insufficient for computer networks, Power Audit looks to the IEEE-1100 standard for wiring and computer networks. Taking this standard to heart, APC will audit a facility, old or new, to ensure that it complies with the IEEE guidelines. The most common problem the company has found relates to grounding—specifically, the overuse of ground-to-neutral bonds that cause current to flow where it shouldn't. Out of 350 customers to date, the program has a 100% track record, when it comes to finding and eliminating wiring mistakes that led to keyboard hang ups, power dips/brownouts/outages, and any other anomaly that poor wiring can introduce.

While prevention is better than curing, even the healthiest of systems get sick sometimes, and UPSs aren't always the way to go. For major industrial sites, they can be akin to a Band-Aid on a whale. In these instances, flywheels, which are based on the principal of kinetic energy, are a popular method of supplying the megawatts of energy needed to keep a system up until an external generator kicks in. A realm unto themselves, these high-power devices are the top of the rung when it comes to power backup.

For the designer worried about adding cost to what may already be an over-budget system, preempting the hand of God or compensating for human error can be something of a last resort. For many, it's enough that all the specs have been met, or even beaten. They just want to wash their hands of the whole affair, and leave it up to the customer to handle the consequences of a power failure at the site.

In many instances, however, the sheer cost associated with a system, whether it be computer or industrial, means that the customer needs—and deserves—more than just a quick hand off. The degree to which you ensure reliable system operation—whether it's through suggestions for the site or ideas to include in the initial design spec—shows pride of ownership. A very marketable commodity.

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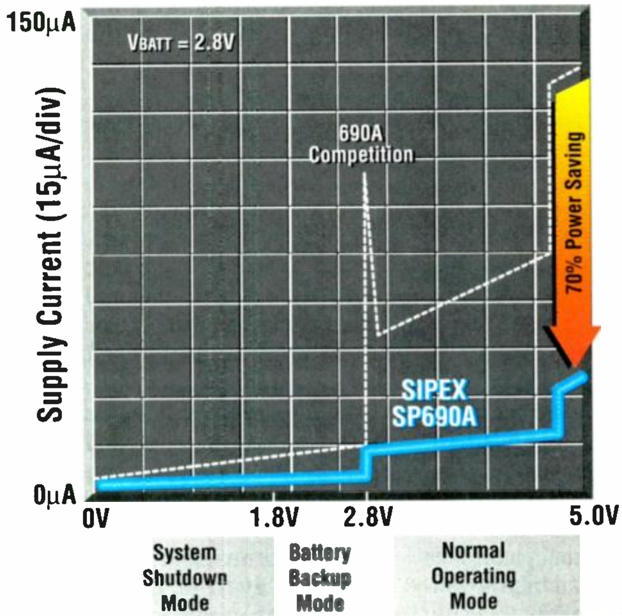

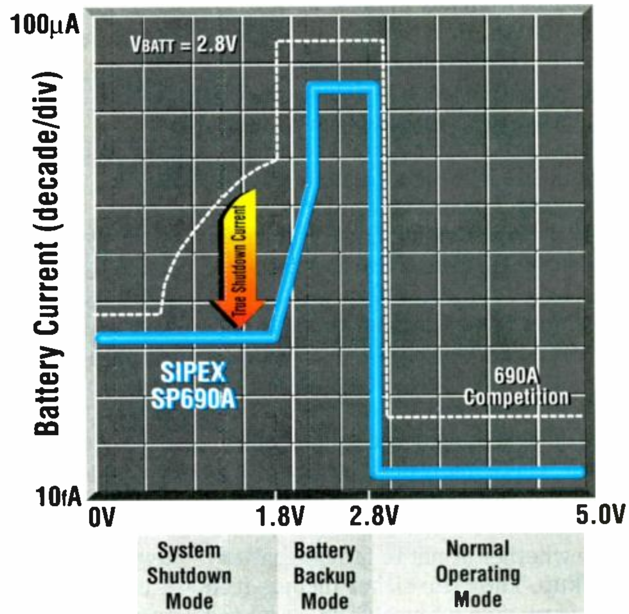

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SP690A	60µA	4.65V	YES	125mV	LOW	4%	0.6Ω	5Ω
SP692A	60µA	4.40V	YES	125mV	LOW	4%	0.6Ω	5Ω
SP802L	60µA	4.65V	YES	75mV	LOW	2%	0.6Ω	5Ω
SP802M	60µA	4.40V	YES	75mV	LOW	2%	0.6Ω	5Ω
SP805L	60µA	4.65V	YES	125mV	HIGH	4%	0.6Ω	5Ω
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READER SERVICE 188

Modular Converters Speed Power Designs

Though Easy To Use, Modular DC-DC Converters Must Still Be Chosen Carefully To Get A Jump On Noise, Heat, And Safety Issues.

Dennis Pendergast
Vicor Corp., 23 Frontage Rd., Andover, MA 01810;
(978) 470-2900; fax (978) 475-6715.

Modular dc-dc converters, in numerous standard designs, provide reliable, field-proven, power solutions. While users can easily specify inputs, outputs, and power levels, the main advantage of these devices is that a user need not be an expert in power conversion to design them into a pc-board application. Their successful use, however, does require the designer to carefully consider noise, heat, and safety issues. In addition, the design choices made by dc-dc converter manufacturers can have a profound impact on the modules' design-in process. This makes it imperative that the designer select carefully among these relatively standard products.

These issues have always been at the forefront of power-system design. However, user demands for higher power densities, higher efficiencies, and smaller packages continue to raise the ante.

The main and most obvious reason behind opting for a modular solution is design simplicity. A complete power system using modular components can be implemented with an ac-dc front end, dc-dc converters for each of the outputs needed, and a few discrete components. More output voltages can be obtained with additional dc-dc converters and filters. A simplified set of inputs and outputs is all a designer needs to consider.

With thousands of dc-dc converters and multiple manufacturers to choose from, the process of selecting the right module can be a major challenge. What's more, each supplier is, of course, seeking a competitive edge. As a result, one supplier provides the highest efficiency, another the smallest footprint, and yet another a new high for power density, and so on. Unfortunately, each achievement likely comes with trade-offs elsewhere in the specification.

Noise And Topology

Noise can vary widely among converters from supplier to supplier and model to model. The reasons range from the fundamental technology employed, to simple differences in design choices, to variations in intended applications.

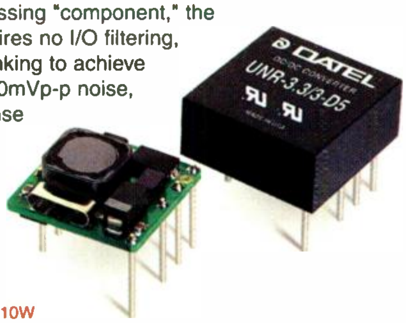
Many converter topologies are used to produce the output voltage, power, and regulation needed by electronic equipment. These topologies reduce to essentially two classes—pulse-width modulation (PWM) and quasi-resonant designs, such as zero-current-switching (ZCS).

In switch-mode converters, common-mode conducted noise is a function of the dv/dt across the main switch in the converter, and the effective input-to-output capacitance of the converter. It's not always easy to identify the specific noise generator, so here are some typical sources, derived from real-life modules:

Topology: Noise is highly dependent on the topology. A PWM topology, for example, often produces noise at high frequen-

5V-to-3.3V, 3A
1" x 1" Package, No External Caps

A true power-processing "component," the UNR-3.3/3-D5 requires no I/O filtering, trimming or heat sinking to achieve ±50mV accuracy, 30mVp-p noise, 40µsec step response and +70°C operation. Its low cost (<<$20 in qty.) makes "building your own" totally impractical.



Web Data Sheet: UNR, 10W
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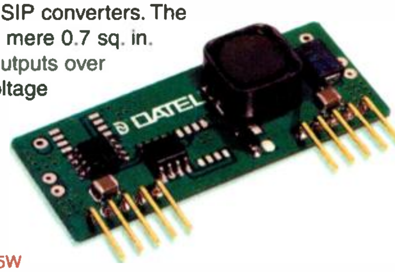
5V-to-3.3V, 3A
Low-Cost, Space-Saving SIP Package

When board space is at a premium and power processing at the "point of use" is the requirement, consider these low-cost, space-saving SIP converters. The UNS Series occupies a mere 0.7 sq. in. and offers 3.3V or 5V outputs over extremely wide input voltage ranges (4.75-13.6V for 3.3V outputs, 6-16.5V for 5V outputs).



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cies (above 5 MHz). The most likely source of that noise is construction-method parasitics generated by the high dv/dt and di/dt associated with this topology. Components such as diodes and MOSFETs generate heat, so they are mounted on an insulating ceramic substrate, which is mounted to the aluminum baseplate of the module. Because ceramic is a dielectric, there is capacitance from the diode and the FET to the baseplate. So, while this construction facilitates heat removal, it also produces parasitic capacitance, which generates noise.

Switching harmonics: Multiples of the 300-kHz switching frequency up to 9 MHz—or 30 times the switching frequency—have been found in some modules. Such converters, used with a typical EMI filter, have been known to fail VDE0871 B requirements for conducted noise.

Packaging and circuit-design: High capacitive coupling, common in metal pc boards and planar-transformer designs, can produce noise as much as 25 times higher than a typical module. Although isolation is normally thought of as a safety issue, the high capacitive coupling associated with nonisolated converters, or those with low isolation voltage, also contributes to higher system noise.

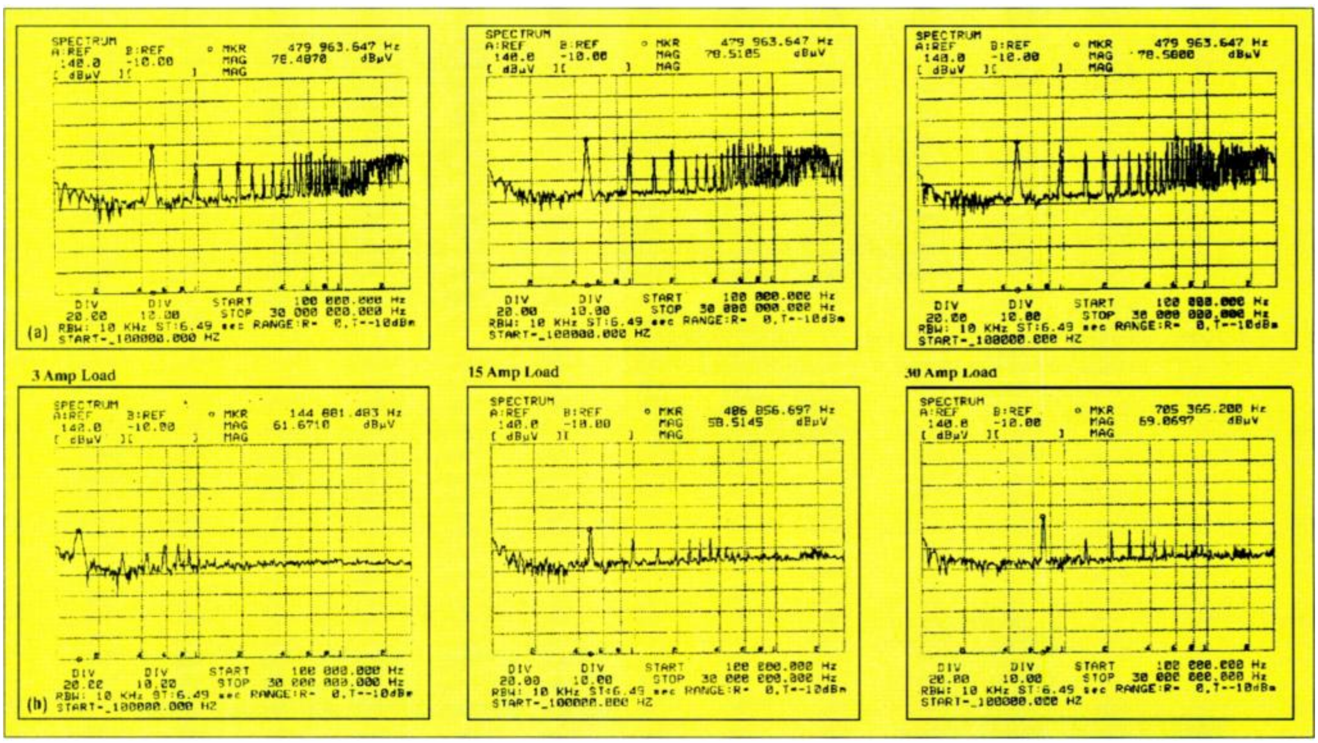
A comparison of the noise produced by converter modules of different design is shown *(Fig. 1a and 1b)*. The fundamental comparison in this case is technological: one module employs pulse-width modulation (where the frequency is fixed and the duty cycle is variable) *(1a)*, while the other uses a quasi-resonant topology (where the pulse-repetition rate is variable) *(1b)*.

A partial explanation for the difference in noise is the relative ease or difficulty with which each topology filters harmonics of its pulse-repetition rate or operating frequency. In PWM converters, most of the energy is found at the fixed frequency or at an odd harmonic of it. A 100-kHz PWM converter will have most of its conducted noise at 100 kHz, and some at 300 and 500 kHz. They also have significant harmonics at or above 1 to 2 MHz due to non-zero-current-switching (high di/dt). The input conducted filter has to be sized to handle maximum power at 100 kHz.

Quasi-resonant converters simplify the design of the conducted line filter because the energy that needs to be filtered is spread between 1/T2 (where T2 is the pulse repetition rate) and approximately 2 MHz. For example, if the converter is operating at its maximum frequency of 1 MHz, all of the energy is contained in a narrow band. This band is easily filtered due to its high frequency. If the converter is operating at a relatively low 100 kHz, the energy is spread between 100 kHz and 2 MHz. In the case of energy spread, for example, by a factor of 10, the peak amplitudes of the harmonics are reduced by a factor of 10.

Thermal Management

Thermal management can be a challenge in any system, but manufacturers of modular dc-dc converters can employ a range of strategies to cope



1. A comparison of the noise produced by converter modules shows the relative ease or difficulty with which each topology filters the harmonics of its pulse repetition rate or operating frequency. In PWM converters (a), most of the energy can be found at the fixed frequency or an odd harmonic of it. These converters also have significant harmonics at or above 1 to 2 MHz, due to non-zero current switching (high di/dt). The quieter, quasi-resonant converters (b) simplify the design of the conducted line filter because the energy that needs to be filtered is spread between 1/T2 (where T2 is the pulse repetition rate), and is approximately 2 MHz.

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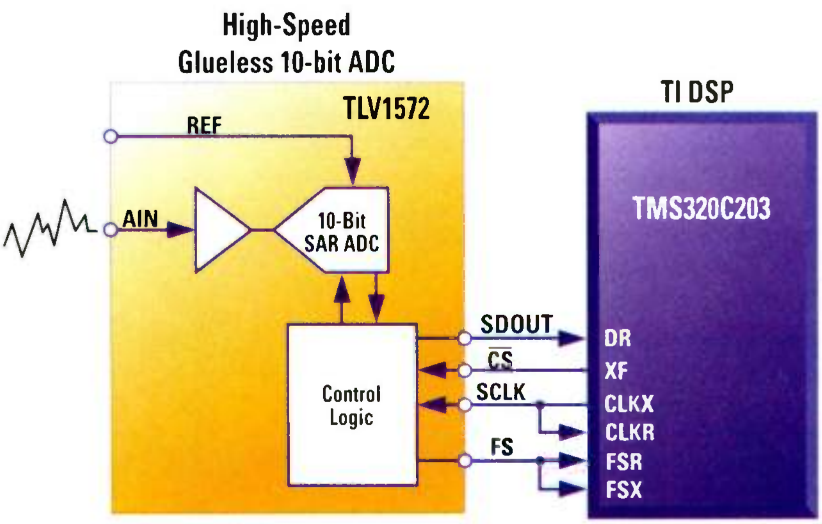

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TEXAS INSTRUMENTS

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with the unavoidable generation of heat. All, of course, strive to make their modules as efficient as possible, and design their packaging to manage the generated heat. High operating efficiency minimizes heat loss, while the use of electrically isolated, low-thermal-resistance interfaces facilitates the removal of heat.

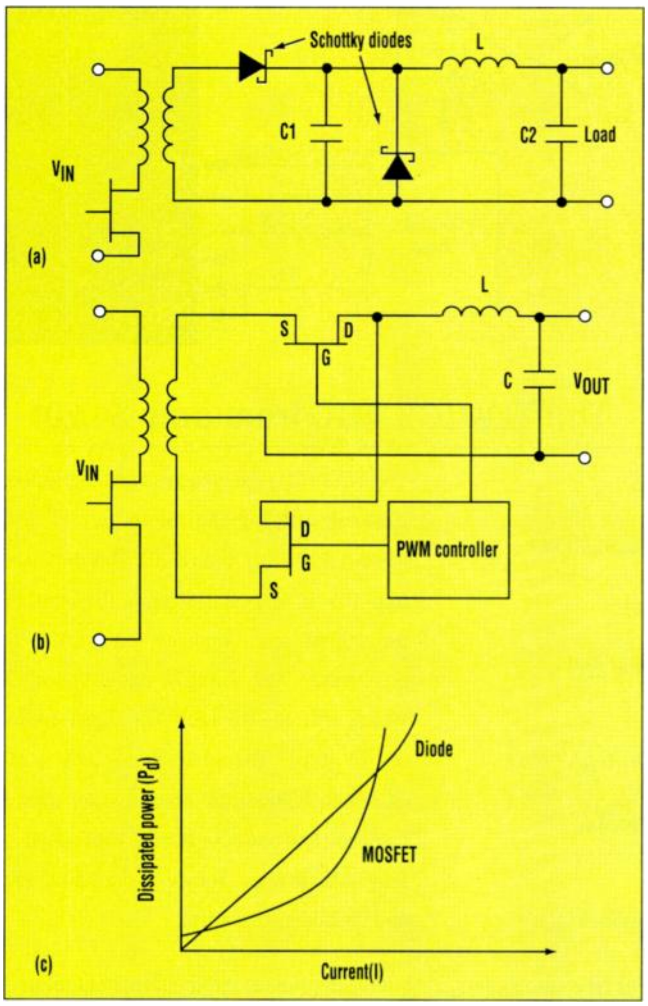
A distributed approach (rather than a centralized architecture) spreads the heat throughout the system, minimizing the need for heatsinks or high-velocity airflow. With the temperature more evenly maintained throughout the system, reliability specifications are easier to meet. Most modular dc-dc converters are well suited for use in distributed power systems.

As you might expect, the heat problems faced by designers using modular components also depend on the many design decisions made by suppliers. These decisions can include design approach (PWM versus quasi-resonant), packaging (potted versus removable plastic cover), component selection (Schottky diode versus MOSFET), material (ceramic versus insulated metal substrate), and many more.

By way of illustration, one such choice is whether to use diode rectification or synchronous rectification. Diode rectification uses a Schottky diode, which has a small resistance and an essentially constant voltage drop *(Fig. 2a)*. Consequently, the dissipated power is roughly proportional to the current through the diode.

Synchronous rectification, on the other hand, operates a little differently, with additional cost and complexity. It employs a MOSFET switch, or switches, to accomplish rectification *(Fig. 2b)*. The MOSFET has a small internal resistance called $R_{DS(ON)}$, which is the resistance from the drain to the source when the MOSFET is on. The power dissipated in this case is roughly proportional to the square of the current *(Fig. 2c)*. At lower currents, the MOSFET will generate less heat than the diode until the output current is reduced to a point where the switching or ac losses in the FET again exceed the essentially dc losses in the rectifier. After a crossover point, perhaps about 20 A, diode rectification will generate less heat loss than the MOSFET, and at no load or light loads, ac losses result in lower efficiencies.

Unlike diodes, where the forward voltage drops as junction temperature increases, when the temperature rises in a MOSFET, $R_{DS(ON)}$ increases for the same amount of current. As a result, the power dissipated in the MOSFET increases, thereby lowering efficiency, which increases the heat generated *(Fig. 3)*.



2. Diode rectification (a) uses Schottky diodes, which have a small resistance and an essentially constant voltage drop. Consequently, the dissipated power is roughly proportional to the current through the diode. Synchronous rectification, on the other hand, uses a MOSFET switch, or switches, for rectification (b). Due to the MOSFET's internal resistance, RDS(ON), the power dissipated is roughly proportional to the square of the current (c).

Safety

A modular design can simplify the time-consuming agency approval process because many modules—unlike traditional designs—have already earned safety-agency approvals such as UL, VDE, CSA, and TÜV. Prequalified approvals can shave significant development time and cost from a project.

Isolation, the electrical separation between the input and output of a power supply, is a basic safety issue in the selection process. For ac-input or high-voltage, dc-input systems, isolation is a must to protect the end user from dangerous voltages and currents. Isolated dc-dc converters simplify a design by using internal transformers to supply the needed isolation. Nonisolated converters need an external transformer to reduce the input voltage to a safe level, and provide protection from the ac-line voltage.

A look at data sheets from a number of converter suppliers will reveal that some units have no isolation, some have isolation up to 3000 or 4000 V, and many fall in between. A design, for example, with 500 V of I/O isolation, can have Safety Extra-Low Voltage (SELV) outputs only when the inputs are SELV. An application using such a module would have to obtain its "safety" isolation from some other source, because the module does not provide it. This can add cost, increase space requirements, and reduce the mean-time between failures (MTBF).

Bus voltage is also an important factor. The higher the voltage, the lower the power loss and the smaller the con-

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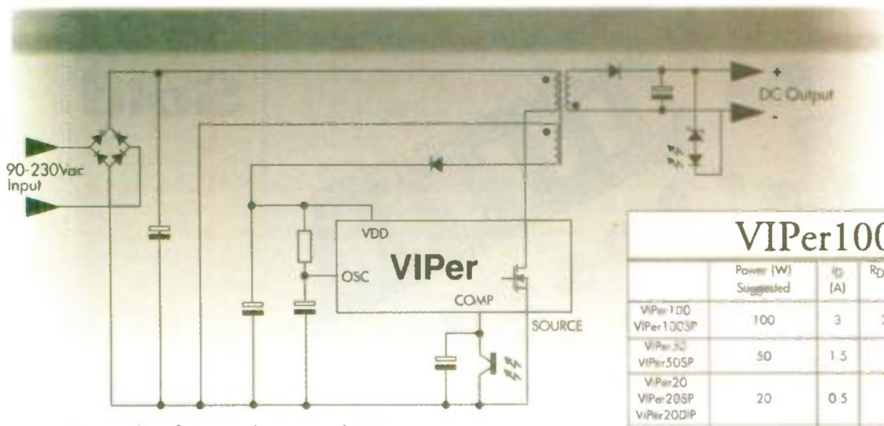

Example of secondary regulation.
VIPer can also be used in primary regulation.

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	Power (W) Suggested	I_D (A)	$R_{DS(on)}$ Ω	$V_{(BR)DSS}$ (V) Protected	Package
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VIPer50 VIPer50SP	50	1.5	5	620	5-pin TO-220 PowerSO-10
VIPer20 VIPer20SP VIPer20DIP	20	0.5	16	620	5-pin TO-220 PowerSO-10 DIP-8
VIPer20B VIPer20BSP VIPer20BDIP	20	1.3	8.7	400	5-pin TO-220 PowerSO-10 DIP-8
VIPer31SP (Batt. Charger)	30	1	6.5	600	PowerSO-10

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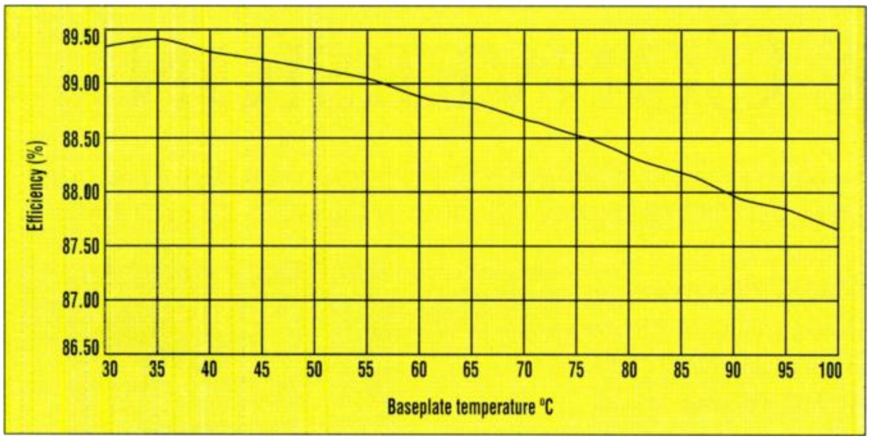

3. Unlike diodes, where the forward voltage drops as junction temperature increases, when the temperature rises in a MOSFET, the device's RDS(ON) increases for the same amount of current flow. As a result, the power dissipated in the MOSFET increases, thereby reducing the efficiency, and increasing the overall amount of heat generated.

ductor size. However, safety standards typically conflict with the selection of a higher bus voltage. SELV is a requirement of most countries, and restricts the voltage to which personnel may be exposed.

Packaging Issues

The modular form factor of dc-dc converters helps a designer shape the power supply to fit the available space. A supply can be designed to almost any physical configuration rather than just a box. The "industry-standard," full-size module package measures 2.4 by 4.6 by 0.5 in. Half-size and one-third-size packages are also available *(Fig. 4)*.

These small modules, in combination with high power densities, have been achieved as a direct result of high-frequency operation. High-frequency, zero-current-switching, quasi-resonant converters do, in fact, dramatically reduce the size of energy-storage elements and, thus, the size of the complete module. What's more, the high efficiency of such converters allows operation in excess of 1 MHz while avoiding energy losses in the switching element. These energy losses are the leading cause of electrical and thermal stresses that undermine reliability.

Dc-dc converter modules come in a very wide range of standard input-voltage, output-voltage, and output-power combinations, and virtually any special combination. Some manufacturers, however, provide just high- or low-

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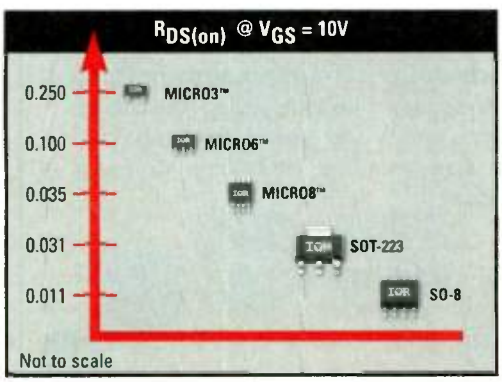

IR small outline packages offer the lowest $R_{DS(on)}$ at the highest power density.

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Dual N-Channel	20-55 Volts	Lowest $R_{DS(on)}$ @ V_{GS} = 10V	0.029Ω
Single P-Channel	20-30 Volts	Lowest $R_{DS(on)}$ @ V_{GS} = 10V	0.020Ω
Dual P-Channel	20-30 Volts	Lowest $R_{DS(on)}$ @ V_{GS} = 10V	0.058Ω
N&P-Channel	20-30 Volts	Lowest $R_{DS(on)}$ @ V_{GS} = 10V	0.029Ω

SOT-223 HEXFET® 1.68mm x 6.50mm

Single N-Channel	30-100 Volts	Lowest $R_{DS(on)}$ @ V_{GS} = 10V	0.031Ω
Single P-Channel	60-100 Volts	Lowest $R_{DS(on)}$ @ V_{GS} = 10V	1.500Ω

Micro8™ HEXFET® 1.01mm x 3.0mm

Single N-Channel	20-30 Volts	Lowest $R_{DS(on)}$ @ V_{GS} = 10V	0.035Ω
Dual N-Channel	20-55 Volts	Lowest $R_{DS(on)}$ @ V_{GS} = 10V	0.135Ω
Single P-Channel	20-30 Volts	Lowest $R_{DS(on)}$ @ V_{GS} = 10V	0.090Ω
Dual P-Channel	20-30 Volts	Lowest $R_{DS(on)}$ @ V_{GS} = 10V	0.270Ω
N&P-Channel Complimentary	20-30 Volts	Lowest $R_{DS(on)}$ @ V_{GS} = 10V	0.135Ω

Micro6™ HEXFET® 1.63mm x 2.90mm

Single N-Channel	20-30 Volts	Lowest $R_{DS(on)}$ @ V_{GS} = 10V	0.100Ω
Single P-Channel	20-30 Volts	Lowest $R_{DS(on)}$ @ V_{GS} = 10V	0.200Ω

Micro3™ HEXFET® .96mm x 2.87mm

Single N-Channel	20-30 Volts	Lowest $R_{DS(on)}$ @ V_{GS} = 10V	0.250Ω
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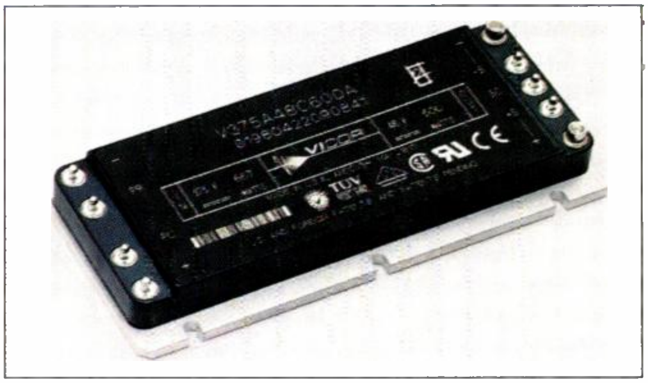
power converters, or specialize in converters for a specific marketplace. Other manufacturers also produce modules of different power levels in the same physical package with identical pinouts. If a specification change requires more power—for example, the 12-V output now requires 150 W instead of 100 W—a higher-power module can easily be used with a minimum of design changes.

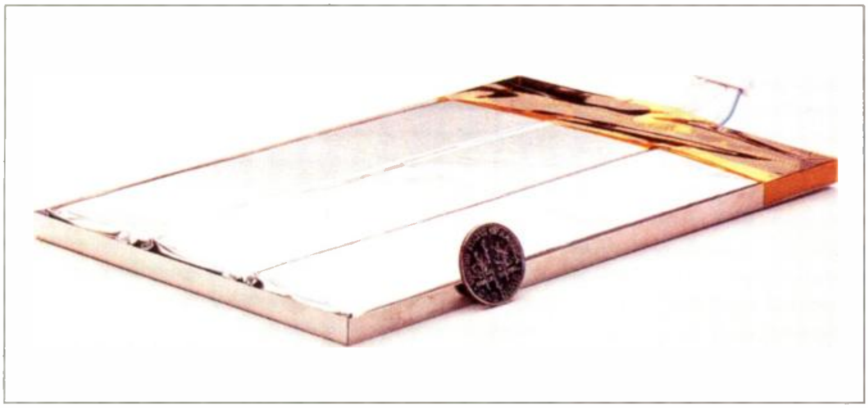
Both potted and unpotted modules are available. Potting, in general, gives more uniform thermal distribution, while also providing improved shock and vibration resistance. All contribute to a more reliable module. Some packaging designs, however, lead to lower-quality, less-reliable modules. The use of trimpots and bonding materials with very different coefficients of thermal expansion, are good examples of undesirable design. Another involves the bonding of large ceramic capacitors directly to the aluminum baseplate. This is a significant failure mechanism.

While the more common, hard design issues revolve around noise, heat, safety, and packaging, less tangible factors, such as technical support, agency approvals, price, and delivery, can often be the key differentiators among manufacturers or suppliers. With time-to-market and cost issues breathing down the necks of most designers, these latter issues cannot be ignored. Leading suppliers are likely to have the range of products and technical and physical resources to help engineers specify the right products for their application, and enjoy timely deliveries of the required volumes.



4. Typical of the level of integration and modularity available in what are now second-generation dc-dc converters, this "full-brick"-sized, power-factor-corrected converter operates off 48 V, outputs up to 600 W, and has a power density of 120 W/in.^{3}

Dennis Pendergast is a product marketer at Vicor Corp. For over 25 years, he has written a wide range of military and commercial marketing and technical documentation. Pendergast received his BSEE from the University of New Hampshire at Durham.



1. The solid-polymer, Li-ion battery—with its excellent combination of safe operation, more flexible packaging, and high performance—is the next step in the evolution of mobile power.

accommodate the repeated migration of lithium ions *(Fig. 2)*.

The rocking chair action gives Li-ion batteries both a long shelf life (self-discharge is only about 8% per month) and a long cycle life. At the capacity (C) rate and 100% depth of discharge, solid-polymer, Li-ion batteries will retain more than 80% of initial capacity after 500 cycles. (The C rate is how long it takes to discharge the battery in one hour. For an 800-mA-hr cell, the C rate would be 800 mA.) There are significant differences, however, between the liquid and solid polymer Li-ion systems.

Liquid-Electrolyte Cells

Liquid Li-ion cells are currently mass produced for use in many notebook computers, camcorders, and cellular telephones. However, this technology has several major drawbacks that hinder a more rapid acceptance of these batteries in the marketplace. Most of these drawbacks are in the areas of packaging, cost, safety, and size. All stem from the battery's basic construction.

Packaging: The liquid electrolyte requires that liquid Li-ion cells be routinely packaged in rigid, hermetically sealed metal "cans." These housings reduce practical energy density, especially in large, multicell packs. As the number of cells in a battery pack increases, the cells' metal housings cause the pack's inert weight and volume to increase as well. In addition, placing cylindrical cells side by side within a pack creates gaps of empty space between cells, further reducing the proportion of energy-producing material in the pack.

Cost: The high manufacturing cost of liquid Li-ion batteries is prohibitive in many applications. That cost results from two factors. The winding, canning, and hermetic sealing processes are complex and costly, and the cathodes of most liquid Li-ion cells use cobalt oxide, a relatively expensive material. Cobalt is also environmentally suspect.

Safety: For safety reasons, liquid Li-ion cells are designed to vent automatically when certain abusive conditions exist, like a drastic increase in internal cell pressure caused by overheating. If the cell did not vent under extreme pressure, it could explode. The problem is that the liquid electrolyte used in liquid Li-ion cells is extremely flammable. If the electrolyte escapes when a cell vents, and if the external cell environment is hot enough, the electrolyte can flame as it is vented. This is cause for considerable concern to design engineers, especially those developing consumer-electronic products.

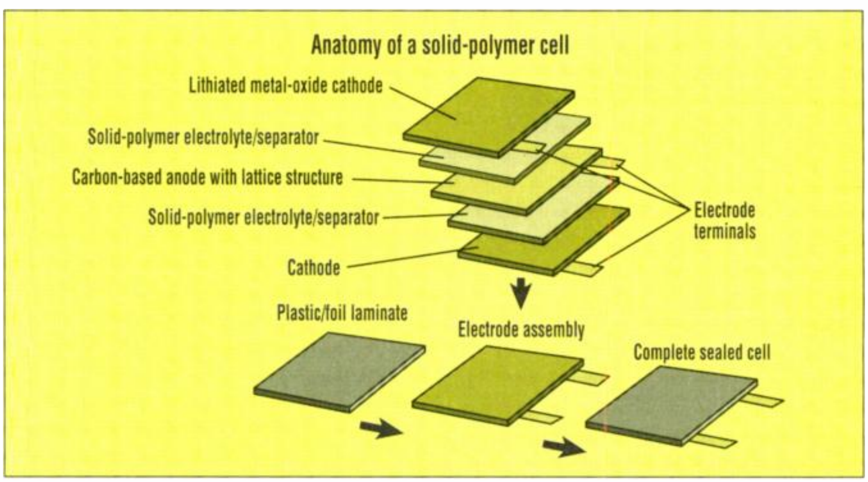
Size: All of the disadvantages outlined above are overshadowed by the significant size limitations of liquid Li-ion cells—both large and small. Due to the safety considerations stemming from the presence of a liquid electrolyte, liquid Li-ion cells cannot be too large. The most common liquid Li-ion cylindrical cell, the 18650, is only 65 mm high by 18 mm in diameter.

However, some applications, including cellular telephones, are better suited to a single, larger cell (combining multiple cells in a pack reduces the battery's energy efficiency). Other applications, such as electric vehicles, are best served by a series of large-size cells.

Ironically, the slimness of a battery pack is also restricted by the limitations of liquid Li-ion cells and their metal housings. Currently, the thinnest liquid Li-ion cells range from about 6 mm thick (prismatic cells) to about 14 mm thick (cylindrical cells). This limits the slimness of portable electronic product designs.

Design Flexibility

The cutting edge of Li-ion technology is in batteries based on a solid-polymer electrolyte, a technology



2. Sometimes called "plastic batteries," solid-polymer batteries offer major reductions in cost thanks to the use of a rolled-sheet format for all components. This allows for exceptionally cost-effective, high-speed, high-volume battery production.

Solid-Polymer Electrolyte Makes Lithium-Ion Safe

With A Proven Safety Record, These Electrolytes Eliminate One Of The Key Impediments To Lithium-Ion's Full Market Penetration.

Gregory B. Smith
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With designers demanding smaller, lighter, and more powerful energy sources, lithium-ion (Li-ion) batteries have rapidly replaced nickel-cadmium (NiCd) and nickel-metal hydride (NiMH) chemistries as the dominant force in the high-performance, rechargeable-battery arena. While the focus to date has been on Li-ion batteries that use a liquid electrolyte, this technology's basic design creates problems in terms of packaging format, size, cost, and safety. As a result, much research has been put into realizing a Li-ion battery technology based on a solid polymer electrolyte. Such batteries have proven to be cost effective, safe under abusive conditions, and environmentally acceptable, all while offering virtually limitless design flexibility and higher performance.

Indicative of the extensive research taking place in the area of Li-ion batteries are the number of other lithium-based designs that have come and gone. Combined with the established and popular liquid-electrolyte batteries, these "imposters" have left a legacy of confusing terminology that can quickly be cleared up with a better understanding of the operation, features, and benefits of solid polymer Li-ion technology.

Over the next five years, according to Arthur D. Little Inc., Li-ion batteries are expected to earn more than a 50% share of the high-performance rechargeable market, while the market share of NiCd batteries is projected to dwindle to less than 10%. Why is this so? The answer starts with a basic chemistry lesson. Lithium is atomic number three on the periodic table of elements, meaning that it has the lightest weight and highest energy density of any solid (only two gases, helium and hydrogen rise above it). As a result, lithium is the ideal material for batteries, producing exceptionally high energy per unit weight and volume *(see table)*. Rechargeable Li-ion batteries are also desirable because they have a high unit-cell voltage—in the 3.0- to 4.2-V range, as compared to 1.5 V for NiCd and NiMH cells.

Li-Ion Varieties

Currently, there are two types of Li-ion technology, about which there seems to be some confusion in the industry. The first, which has been on the market for a few years, uses a liquid electrolyte. The second, which is now starting to make an impact in the marketplace, uses a solid-polymer electrolyte *(Fig. 1)*.

These two technology types share a fundamental intercalation, or "rocking chair," system of operation: Lithium ions move back and forth between electrodes as the battery is charged and discharged. The anodes and cathodes of Li-ion batteries are made from carbonaceous (carbon-based) materials and metal oxides, respectively, with layered structures that

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now being pioneered primarily by U.S.-based companies. Solid polymer Li-ion batteries have outstanding attributes in the essential areas where liquid Li-ion is weakest. The cells offer virtually limitless design flexibility with cost-effective materials and construction, have proven safe under abusive conditions, improve greatly on overall performance, and are environmentally acceptable.

Because there is no liquid that has to be contained by a hermetically sealed, rigid metal can, this new type of battery can be housed in an ultra-thin laminated foil material that can be used to house each cell *(Fig. 1, again)*. This design creates a number of distinct advantages.

For one, solid-polymer, Li-ion cells can be made as thin as 0.64 mm (25 mils), or about one-tenth the thickness of the thinnest prismatic liquid Li-ion cells. The cells can also be stacked in series or parallel to form ultra-thin battery packs with a wide range of voltages and capacities. Such design flexibility allows engineers to obtain the required performance from the flattest-profile battery possible. This point was vividly illustrated by Mitsubishi Electric Corp., Tokyo, Japan, which in October 1997, introduced the world's thinnest (less than 0.75-in. thick) and lightest (3.1 lb.) notebook computer. The computer was powered by a 0.25-in.-thick, Ultralife solid-polymer rechargeable battery.

In addition, the widths and lengths of solid-polymer, Li-ion cells are as flexible as their thicknesses. As a result, cells can be configured in virtually any size, making solid-polymer Li-ion a stronger candidate than liquid Li-ion for electric vehicles and other large-cell applications. Even non-rectangular shapes are possible. This unique size flexibility allows for maximum energy efficiency within a given battery cavity.

Additionally, a laminated foil housing makes solid-polymer, Li-ion cells flexible—literally. This allows them to conform to cavities with curved surfaces. Furthermore, the foil housing material is considerably lighter than the metal used for liquid Li-ion cells.

From a cost perspective, the solid-polymer, Li-ion system also promises considerable advantages. Instead of the relatively expensive cobalt oxide found in liquid Li-ion cells, cathodes in solid-polymer, Li-ion cells use an inexpensive metal oxide material. Even more significantly, every component of a solid-polymer, Li-ion cell is fabricated in rolled-sheet form. This technique allows for exceptionally cost-effective, high-speed, high-volume battery production.

Electrodes, electrolyte, and foil packaging—all on continuous-feed rolls—are sandwiched together into finished batteries in one smooth process. In comparison, the winding and canning processes used to produce liquid Li-ion cells are time consuming and expensive. Ultimately, solid-polymer, Li-ion batteries will cost in the range of $1 to $2/Whr. As a point of reference, NiCd batteries, with five decades of manufacturing improvements, cost a bit below $1/Whr.

As with other Li-ion batteries, solid-polymer batteries require individual cell monitoring. Cells are charged at a constant 4.2 V, with the charging current limited to the C rate *(Fig. 3)*. Charging cuts off when the charging current declines to the C/10 rate (80 mA for an 800-mAhr cell). The temperature range for charging is 0° to 45°C. As can be seen from the table, the energy density of solid-polymer batteries ranges from 115 to 150 Whr/kg, compared to 70 to 110 Whr/kg for liquid-electrolyte Li-ion cells. In addition, solid-polymer batteries can be recharged more than 500 times, and have no trouble taking a one-hour charge.

Safety Issues

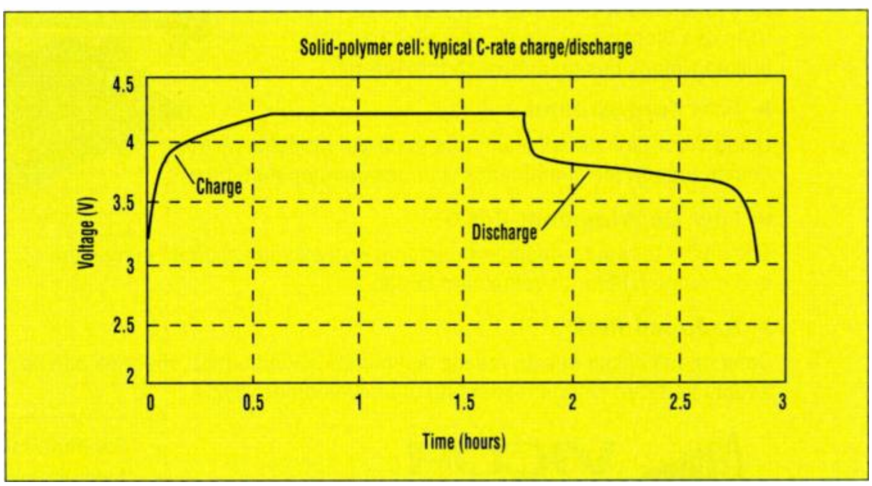
Because its electrolyte cannot leak, a solid-polymer, Li-ion cell is intrinsically safer than a liquid Li-ion cell. Venting is simply not an issue. Moreover, the solid electrolyte, a plastic compound, is a non-volatile material capable of withstanding severe safety testing, including:

Pressure: The cells have been pressurized to 1500 psi under electrical testing. No signs of electrode shorting were observed.

Short circuit: A high-capacity, solid-polymer, Li-ion battery pack was short circuited with a maximum current of 85 A. The external temperature of the battery increased only a few degrees, and the battery was able to accept a subsequent charge without any adverse effects.

Overcharge/overdischarge: Solid-polymer cells were overcharged as high as 20 V at up to a 3C rate, and overdischarged at up to a 3C rate. The cells ceased to function, but no flaming or any other hazard occurred.

Penetration: A nail was fired through the center of a high-capacity, solid-polymer, Li-ion battery pack during discharge. The output voltage dipped briefly, and only 60% of battery



3. Solid-polymer batteries require individual cell monitoring, as do other Li-Ion batteries. The cells are charged at a constant 4.2 V, with the charging current limited to the C rate. Charging stops when the current drops to a C/10 rate. The temperature range for charging is 0° to 45°C. The batteries can be discharged at up to a 2C rate, with pulses as high as 5C.

RECHARGEABLE BATTERY COMPARISON				
Chemistry	NiMH	NiCd	Liquid-Li-ion prismatic	Solid-polymer
Energy density				
(Wh/kg)	50 to 60	30 to 35	70 to 110	115 to 150
(Wh/l)	150 to 175	80 to 105	190 to 250	200 to 300
Minimum thickness	>6 mm	>6 mm	>6 mm	0.64 mm
Cycle life (to 80% capacity)	~800	~1000	>500	>500
Self discharge (% capacity/month)	>25	>15	5 to 8	5
Temperature range (°C)	?	?	–20 to 60	–20 to 60
Safety	Safe	Safe	Less safe	Safest
Environmental	Potential problem	Major problem	Potential problem	No problem

capacity was achieved during that particular discharge cycle. However, on a subsequent recharge/discharge cycle, the battery recovered to 95% of initial capacity.

These crucial safety factors have allowed certain solid-polymer rechargeable batteries to meet the safety standards of the Japan Storage Battery Association, the International Electrochemical Commission, the Canadian Standards Association, and Underwriters Laboratories. This makes solid-polymer, Li-ion batteries particularly attractive to manufacturers of portable consumer electronics, such as cellular telephones and notebook computers. In addition, because the test data indicate a high degree of safety in multicell battery packs with a broad range of capacities, as well as in individual cells, the technology is attracting the interest of electric vehicle manufacturers and other large-battery designers.

Finally, on top of its other advantages, the solid-polymer, Li-ion system is environmentally friendlier than other batteries, especially the nickel-based chemistries. The materials used, including the metal oxide in the cathode, are benign. As a result, solid-polymer batteries do not require any special handling, nor do they face any transport or disposal regulations.

Lithium-Metal Confusion

Part of the industry's confusion over the different types of lithium-based, rechargeable batteries may stem from a rechargeable, lithium-metal (Li-metal) technology that has struggled to achieve commercial acceptability. Rechargeable Li-metal is a "Holy Grail" of sorts because it offers an extremely high energy-density potential—theoretically about 150 Whr/kg, or over 300 Whr/l. But while metallic lithium works extremely well in primary batteries, a truly viable, rechargeable Li-metal technology has been elusive.

One of the main problems is that lithium, in its metallic form, is highly reactive. As such, it presents unique difficulties in rechargeable configurations. Repeated charge/discharge cycles can cause a build-up of surface irregularities on the lithium electrode. These irregular structures, known as dendrites, can grow to such an extent that they penetrate the separator between positive and negative electrodes and create an internal short circuit. At best, this phenomenon shortens the useful life of a rechargeable Li-metal battery to 150 cycles or less. At worst, an internal short circuit could cause the battery's internal temperature to rise above lithium's melting point (181°C), which could cause severe flaming.

It's almost impossible to safeguard rechargeable Li-metal batteries against potential catastrophic failure under extremely abusive conditions. Without adequate safeguards, rechargeable Li-metal batteries are high-risk items, especially for consumer products.

While there still are one or two manufacturers offering rechargeable Li-metal cells, it's hard to imagine a consumer-products company that would take a chance with them. The use of rechargeable Li-metal cells, if they achieve commercial success at all, will likely be restricted to specialized military and industrial applications.

Another term, lithium-polymer, is associated with a developmental Li-metal system that by the mid-1990s was found to be non-viable. It must be stressed that this was a lithium-metal battery. Some have used the term "lithium-polymer" incorrectly to describe solid-polymer, Li-ion batteries. The company that first touted the lithium (metal)-polymer battery gave up on the idea long ago, and has switched its focus to a Li-ion technology similar to the solid-polymer rechargeable battery.

Solid-polymer, Li-ion batteries, at the leading edge of rechargeable battery technology, offer the best combination of design flexibility, performance, cost, and safety demanded by the highest-volume consumer electronics applications. The next questions still to be answered are: How soon will these batteries reach mass production, and how much energy can be packed into a cell?

To answer the first question, certain companies anticipate higher-volume, automated production capability during 1998. To the second question: Much research is being done to improve the conductivity of solid-electrolyte materials, and alternative electrode materials are being studied closely. In addition, IC manufacturers are designing new battery-management chips that are steadily improving the precise cell-by-cell monitoring required by Li-ion batteries. With these efforts underway, and mass production imminent, solid-polymer, Li-ion technology is poised to become the dominant force in the high-performance, rechargeable-battery arena.

Gregory Smith is a 12-year veteran of the battery industry, and has authored more than a dozen articles on the subject. He has spent the last five years with Ultralife Batteries Inc., where he is a technical marketing manager.

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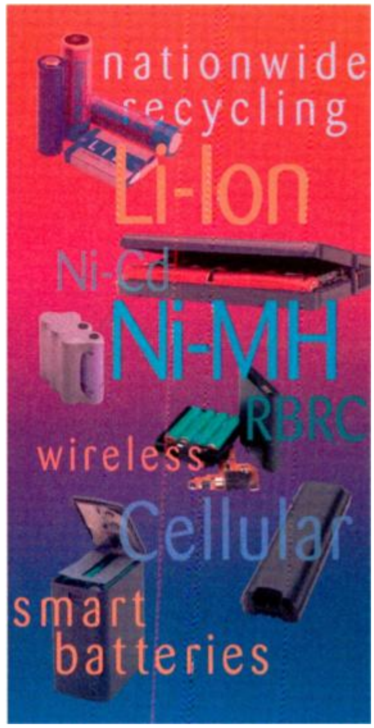

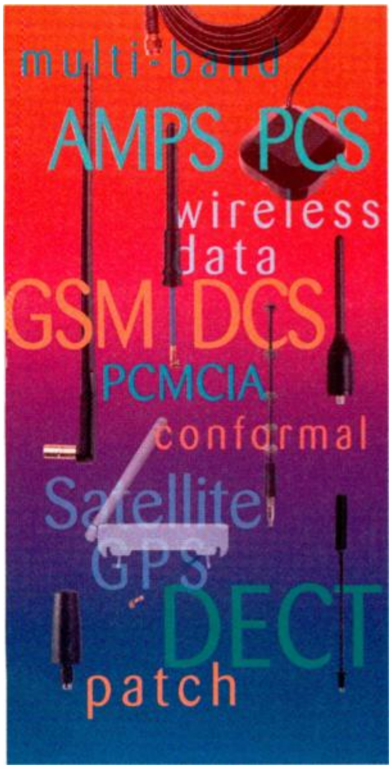

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Online UPSs Save "Mission-Critical" Applications

But Designers Must Understand The Various Architectures and Options Available In Order To Make The Right Choice.

Aron Levy
Nova Electric Div., Technology Dynamics Inc., 100 School St., Bergenfield, NJ 07621; (201) 385-0500; fax (201) 385-0702

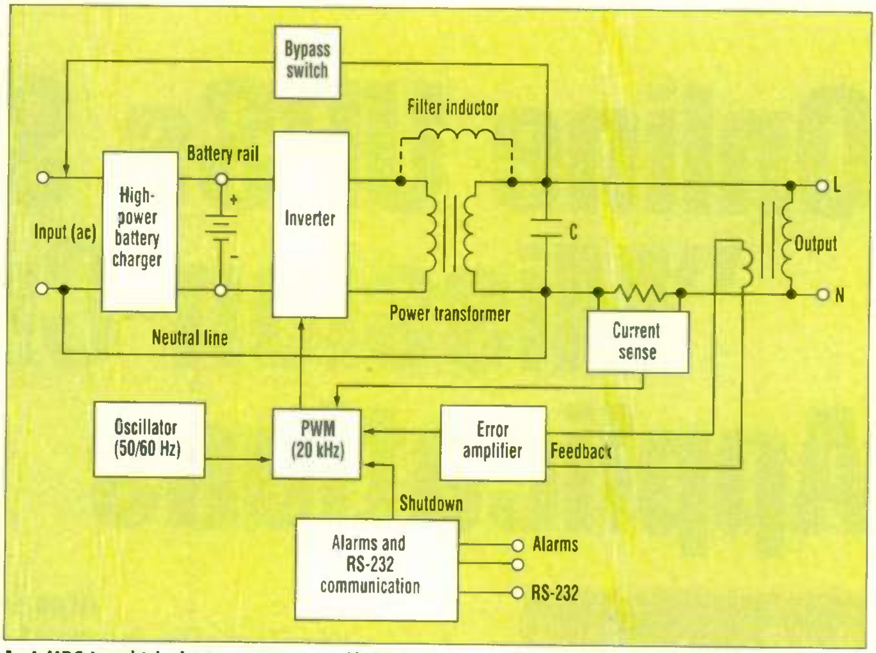
Uninterruptible power supplies (UPSs) fall into two distinct classes—standby or online. While the relatively low-cost, standby UPS has found favor in the consumer desktop market, the 5- to 10-ms delay these devices introduce when switching from utility to battery cannot be tolerated in critical applications. Here, the online UPS, which avoids this switching action, is preferred. But not all UPSs are created equal; each has its own balance of size, weight, cost, reliability, and performance. So system designers and integrators must understand the internal workings of these devices to ensure that choosing among the various topologies does not result in costly error.

The basic premise of all online UPSs is that the output is glitch free—a sinewave, well regulated, and well protected against overloads and shortcircuits. Also, it should be able to drive both resistive and certain reactive (nonlinear) loads. Because most systems running on UPSs are not purely resistive, their current and voltage consumption are not completely in phase, resulting in a reactive power component known as the "power factor." The rating of a UPS reflects its ability to deal with this reactive load. So, UPS capacity is measured in volts × amperes (VA), rather than watts.

Commonly available online UPSs start at 1 kVA (the size of a computer box), and go as high as several hundred kVA (large cabinets weighing hundreds or thousands of pounds). For backup, sealed, maintenance-free, lead-acid batteries are used for their ruggedness, durability, and ability to supply high inrush currents. They are easy to charge, and they maintain that charge over long periods when not in use. However, the batteries deteriorate at temperatures of 60°C and above, and at low temperatures they lose capacity—in terms of ampere hours (Ahr)—very quickly. The batteries are connected in series to arrive at the desired voltage (12 V × the number of batteries), and in parallel to arrive at the desired capacity.

If the inverter within the online UPS runs on battery at all times, the batteries must be charged continuously from the utility supply. The charger is rather large because it supplies the entire current needs of the inverter, as well as furnishing current to charge the battery. Because the charger is a dc-dc converter (from the rectified utility voltage to battery voltage), and the inverter follows it, this online topology, in effect, completes a double conversion. Hence, the name "double-conversion UPS."

The inverter does not recognize a utility failure because, during the absence of utility power, it will continue running on the battery and delivering its output. But the battery is now in a discharge mode, and will run the inverter for a pe-

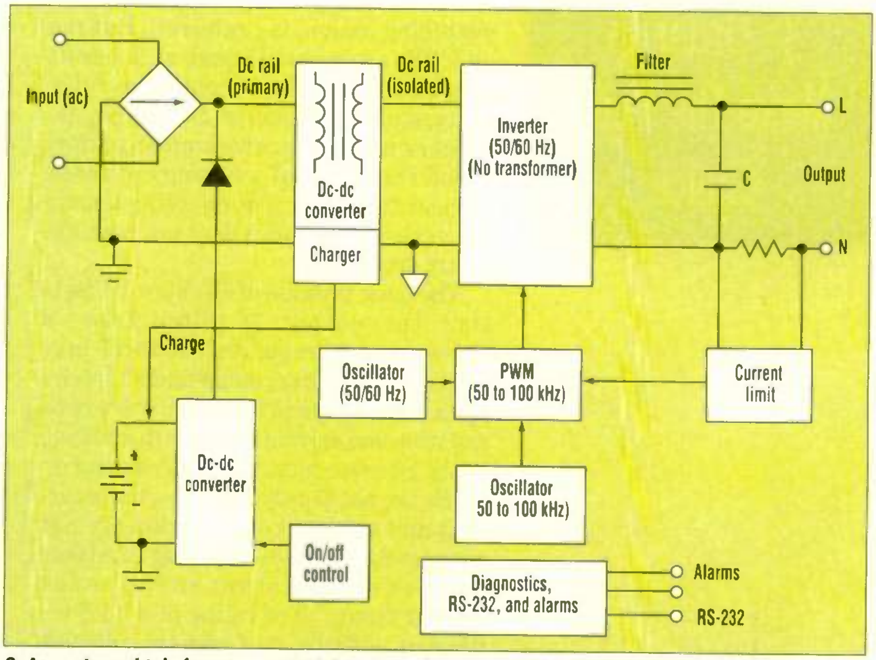


1. A UPS in which the inverter runs off the battery at all times requires a high-power battery charger to allow it to supply the battery and inverter simultaneously. The inverter stage resembles a switch-mode power supply, except that its output is ac rather than dc.

riod proportional to its capacity, temperature, and current drain. The smaller the load, the longer the backup time.

Several Architectures

Online UPS manufacturers employ several major design architectures. All of them are in common use in commercial, industrial, and military UPSs. As noted, in online UPS, the battery powers the inverter stage at all times. The utility (ac) drives the high-power battery charger, which



2. Inserting a high-frequency (100-kHz), dc-dc converter dramatically reduces the UPS's size and weight. However, the dc-dc converter can add significantly to the unit's cost, while the absence of the massive transformer at the output can compromise reliability.

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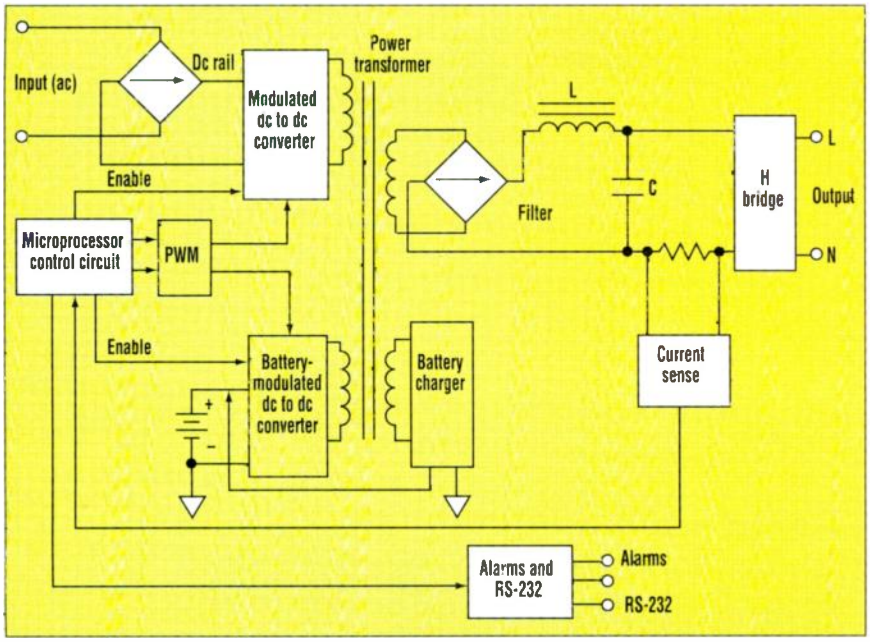

3. By using a reference voltage (for the dc-dc converter PWM) that looks like a rectified sinewave instead of a dc voltage, it is possible to eliminate the inverter stage. This is done by modulating the dc-dc converter stage to obtain a wave shape that resembles a rectified sinewave.

charges the battery, and supplies the inverter simultaneously *(Fig. 1)*. The inverter stage—equipped with a stable oscillator, pulse-width-modulator (PWM), and feedback loop—resembles a switch-mode power supply, except that its output is ac rather than dc. The high-frequency PWM stage is modulated by the line frequency (50 or 60 Hz) in a class D fashion, resulting in a high-quality sinewave (after some minimal filtering).

Were it not for the fact that the inverter is limited in capacity and peak current capability, the load would not know the difference between the utility and the UPS output. The UPS proves advantageous however, as it is well regulated (±2%), while the utility voltage fluctuates widely (±15%). This regulation is provided by the feedback loop. A small transformer at the output generates a signal for the feedback loop for error amplification. A ±2% regulation at the output is feasible in this topology from no-load to full-load conditions. The battery-voltage fluctuation is ±15%.

The power transformer at the output of the inverter is a line-frequency transformer, and is, therefore, large and heavy (depending on the UPS capacity). After the battery bank, this transformer is the single most dominant weight and size element within what could already be quite a heavy UPS system.

Notice also, that this transformer, together with the capacitor across its output, acts as a filter inductor (shown by dotted lines)*(Fig. 1, again)*. This bonus feature is accomplished by purposely allowing a high leakage inductance between the primary and secondary of the transformer. The result is a virtual filter inductor, which, together with the capacitor, forms a low-band filter for the high-frequency carrier.

The current-sense circuitry provides overload and short-circuit protection to the output. In addition, the input is bridged to the output of the UPS by a bypass switch. This switch can connect its output to the input utility in case of inverter failure. The transfer switch is a key feature in on-line UPSs, but it is not standard. Far-East manufacturers make another good use of this switch. At turn on, they connect the load to the utility for 10 s, and only then transfer it to inverter. The first 10 s permits loads with high inrush current—such as switch-mode power supplies (SMPSs), motors, and compressors—

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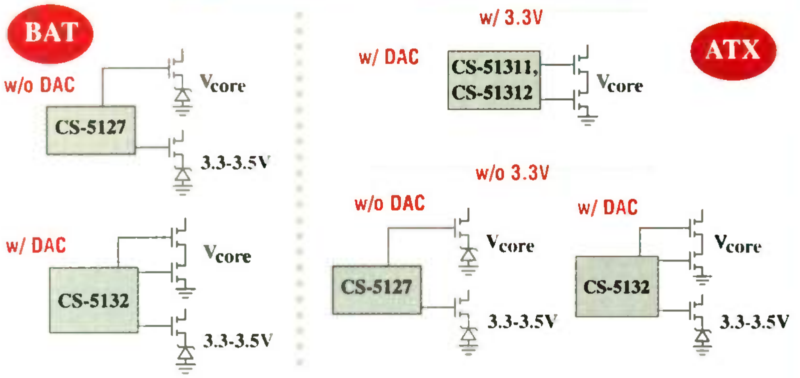

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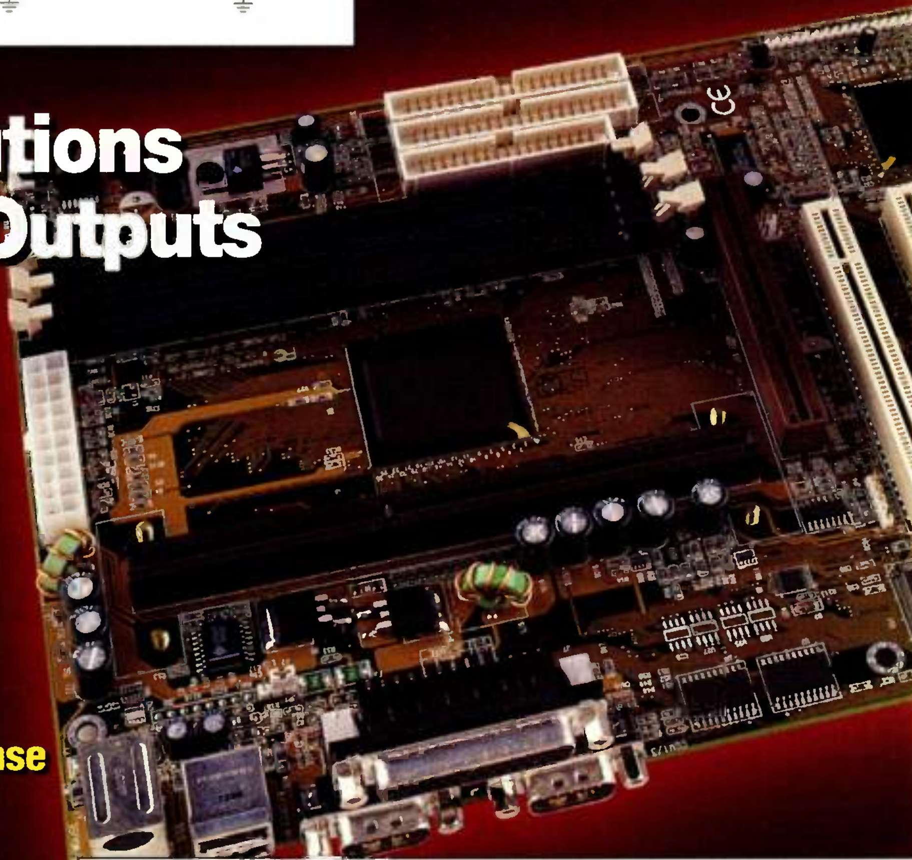

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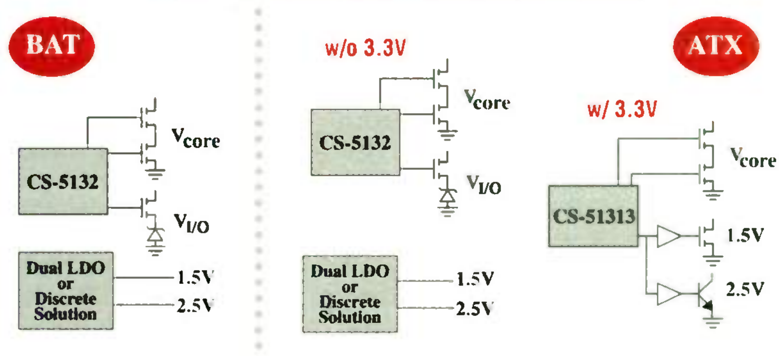

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to start well on utility, and only then transfer to the inverter under more stable conditions.

Obviously, the line-frequency transformer makes this type of UPS relatively heavy and bulky. On the other hand, it is also the most reliable. The 60/50-Hz transformer acts as a buffer between the inverter and the load, absorbing harmful transients. It makes the bypass switch less sensitive and the entire UPS more rugged and solid. Although this topology reflects somewhat old technology, it's the UPS of choice for many customers who don't mind the extra size and weight, but like the extra reliability.

A variation on the theme of the "heavy UPS" involves driving the inverter from the rectified utility voltage rather than the battery. In this case, a relatively small charger supplies current only to the battery, and not to the inverter. This approach offers advantages, in terms of size, weight, cost, and performance. Also, because there is no real double conversion, the efficiency is significantly higher (80% compared to 65%).

However, the rectified line voltage produces significantly higher voltage (150 V dc for rectified 115 V) than the battery voltage (84 V dc for a 115-V UPS). Thus, the inverter is subjected to a severe "bump" in the form of a voltage step function every time the utility falls and comes back. The bump may be reflected on the output somewhat, even in UPSs with a quick response time. Worse, it may cause a latchup of the UPS, especially when the utility comes back, causing the inverter dc rail to jump by up to 70 V.

The latchup (and subsequent shutdown) occurs when the overload and short-circuit protection circuit senses a severe hike in inverter current. This may be caused by a momentary saturation of the power transformer, or by a sporadic noise pulse that propagates through the system. As a result, circuitry must be added to mitigate the impact of the bump, and slow it down enough, so that it looks more like a ramp than a steep front. This circuitry adds a bit to the circuit's complexity.

High Frequency, Lightweight

To get around the hefty size and weight of the line-frequency transformer, a high-frequency (100-kHz) dc-dc converter can be used *(Fig. 2)*. Dramatic savings in weight and size are accomplished in this way, though the dc-dc converter can add a significant cost of its own.

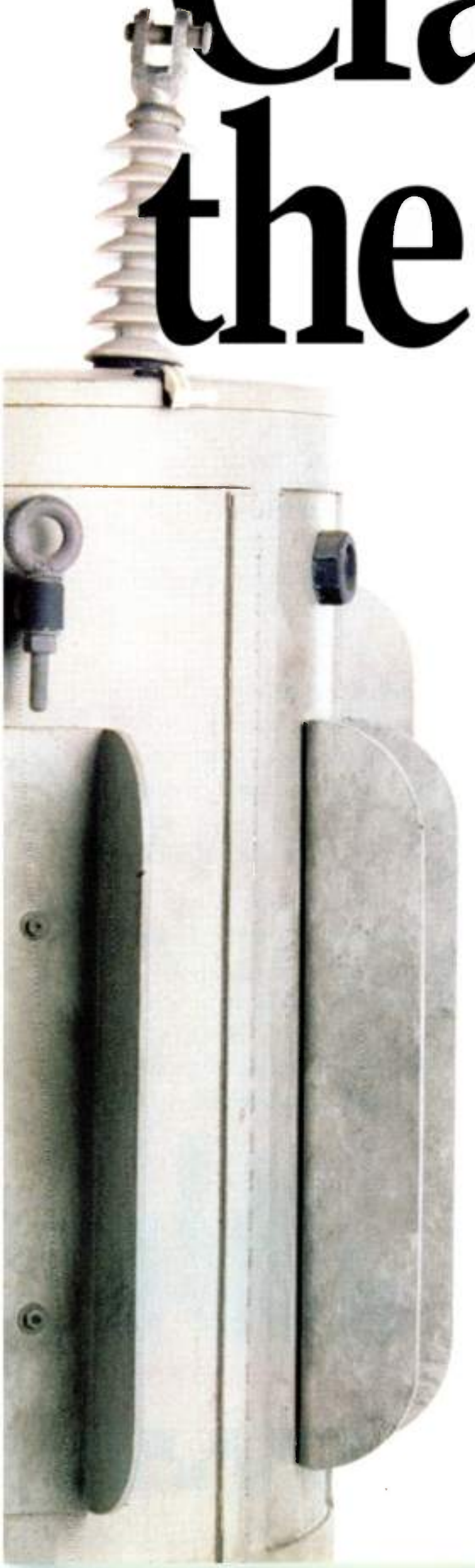
The absence of the massive transformer at the output means that the load is connected to the inverter transistors (H-bridge topology) directly, without any buffering. This tends to diminish reliability in two ways. Firstly, the reliability of the dc-dc converter (high power) is substantially lower than that of an iron and copper transformer. Secondly, the energy pumped back from the load (due to parasitics or back EMF) may cause transients that can damage the inverter's power transistor. Despite these negatives, there are airborne, portable, or military applications in which the lightweight approach is the most appropriate choice.

All of the design approaches discussed above incorporate galvanic isolation. This is important for the attenuation of high-frequency noise and the elimination of transients riding on the input line. Even so, it's best to tie the input and output neutral lines for safety reasons. It's also worth mentioning that some of the lightweight, online UPSs coming from the Far East are not equipped with galvanic isolation—a move to reduce cost.

Integrated Designs

UPS designers can essentially eliminate the inverter stage by modulating the dc-dc converter to obtain a wave shape resembling a rectified sinewave *(Fig. 3)*. The change involves a reference voltage (for the dc-dc converter PWM) that looks like a rectified sinewave instead of dc. Because the frequency of the dc-dc converter is relatively high (60 to 100 kHz), the reference frequency of 60 Hz will be treated as a varying dc signal by the PWM.

After rectification, the resulting signal looks like a rectified sinewave with a period of 8.33 ms (for 60 Hz modulation), and a peak amplitude of 160 V. Now it is necessary to invert every second pulse to create an ac voltage of 60 Hz. This is done simply



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by an H-bridge circuit synchronized to the 60-Hz reference voltage.

The integrated approach is obviously more efficient and less expensive (one conversion instead of two), but it has its problems. For one, the wave shape at the output is not as pure as in the previous approaches (due to crossover distortions). Also, it cannot handle a transfer switch. Our attempts to incorporate a solid-state transfer switch in this topology ended repeatedly with the destruction of the output H bridge.

In newer designs, many of the functions within the UPS are delegated to one microprocessor. These include sinewave generation, PWM, monitoring, and control. It's also possible to incorporate the RS-232 communication into the same microprocessor, though it's not recommended. The microprocessor provides a good approach to circuit simplification, leading to labor and cost reductions.

Power-Factor Correction

The majority of online UPSs in the market lack power-factor correction (PFC) at their input. As a result, these units behave exactly as SMPSs due to their input rectification and large filter capacitor. This capacitor causes high-current impulses at the input, causing a substantial amount of harmonic power to be pumped back to the line. The new European Safety and EMC regulations (CE) do not permit such harmonics to be injected into power lines, and as a result, create pressure on exporters to include PFC in their UPSs. The PFC circuit entails conversion (by booster topology), and therefore causes a reduction in the overall efficiency of the UPS—not to mention a 10% to 15% cost increase over non-PFC systems.

Adding to the power-factor problem is the fact that online UPSs range in power into the hundreds of KVA. It is not easy to design-in PFC for such power levels. Above a certain power level, it is likely the European regulations will exempt such apparatus from meeting the recent PF limits set by the EEC.

Nonlinear Loads

Many users are oblivious to the fact that some loads (like SMPSs) are extremely reactive, with a poor power factor at their input and, consequently, a very high peak-current demand. Therefore, users tend to purchase a UPS with capacity equal to or slightly higher than their power-system needs, resulting in a useless, undersized UPS.

It should be realized that a UPS rated for 1000 VA is good, at best, for 700 to 750 W. This is how UPS manufacturers specify their units, and it implies that a user cannot expect 1000 W from a 1000-VA UPS. However, what's more important to remember is that high-inrush-load impulses (as in the case of compressors and switch-mode power supplies), are not compatible with UPS capabilities. The end result is that the UPS shuts down to protect itself. SMPS loads are particularly painstaking, and because SMPSs are very common (they are in almost all computer systems), the likelihood is very high that the UPS will be driving an SMPS at its output. However, the UPS and the SMPS can be made more compatible by equipping the SMPS with PFC at its input from the start.

Not all UPSs are the same though, as some are designed for highly reactive loads and will perform better with SMPSs. Some are marginal. The moral of the story is that the user cannot go blindly into this. The best route is to provide the manufacturer of the UPS with an actual (measured) profile of the system's input current to make sure the UPS can handle the expected load. Experience has shown that the user should purchase a UPS with a capacity of at least three times the system's need in watts. This rule of thumb may be challenged by various manufacturers, but for the sake of generalization, we found it to be true time and again.

Aron Levy is the president of Technology Dynamics Inc., and its divisions, Nova Electric and Mid Eastern Industries. He holds a BSEE from Long Island University, Greenvale, N.Y., and a master's degree in Business from Columbia University, New York, N.Y. He has published over 25 articles on power-conversion subjects in technical magazines, both in the U.S. and abroad.

Unscramble The European Power Directives

While The New Standards Facilitate Trade Within Europe, They Perplex The Many Foreign Companies Targeting That Market.

Per Lindman
Ericsson Components AB, Energy Systems Div., S-164 81 Kista-Stockholm, Sweden; +46 8 721 6000; fax +46 8 721 7001.

By implementing harmonized standards that remove the barriers to free movement of electronic products, the European Union (EU) is rapidly realizing its goal of creating a single market. This unified market eliminates the confusion and cost associated with multiple local laws and standards. This move could potentially simplify the technical and commercial task of creating products for Europe, and make it easier to use products from any country in Europe.

The result is a major opportunity, but it does demand that designers be at least familiar with a completely new set of rules. The good news is that these rules have been written as a coherent set, building on national experiences gained over a number of years. However, the sheer volume of material, and the labeling system employed, can be confusing. In the context of power supplies, approximately 116 standards and amendments govern EMC alone. Of all the standards and recommendations, nowhere is the hierarchical structure of European standards clearer, but the application more open to interpretation, than in the CE mark.

TABLE 1: DETAILED EUROPEAN NORMS

Directive	Standard	Application
LVD	EN 60950	Information technology (ITE)
	EN 60601-1	Medical devices
	EN 61010-1	Industrial and scientific measuring (ISM) and process control
EMC	EN 50081-1/2	Generic standards for emission
	EN 50082-1/2	Generic standards for immunity
	EN 55011	Emission for ISM
	EN 55022	Emission for ITE
	EN 300386-2	Telecom network equipment
	EN 61000-3-2	Emissions of harmonics to the mains

The Basic Nomenclature

Before we get too deeply into the topic, it may help to clarify a few terms:

- *Directive:* The name given to an official EU document that defines the requirements.
- *Apparatus:* A finished product delivering an intrinsic function, and directly usable by the end user.
- *CE Marking (93/68/EEC):* Products subject to Directives must comply with those Directives, and be marked in a prescribed way with the CE logo to be legally offered for sale in any EU state.
- *Competent body:* A body recognized as fulfilling the criteria of Annex II of the EMC Directive, and responsible for issuing reports or certificates under Article 10.2 of that Directive.
- *Notified body:* A body specially defined to the European Commission by a member state as having responsibility for issuing EC-type examination certificates for radio communications equipment under Article 10.5 of the EMC Directive. The body is also required to match the criteria of Annex II of that Directive.
- *Compliance:* Unlike approval sys-

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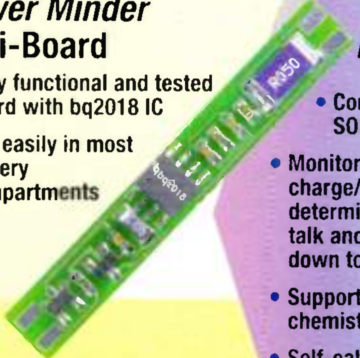


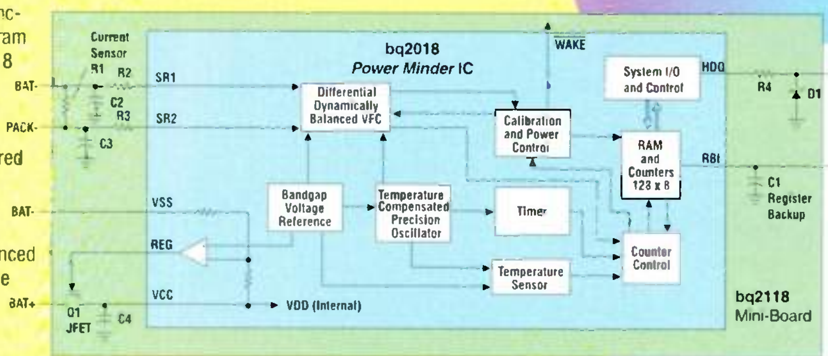
The bq2018 *Power Minder* IC

- Compact 8-pin SOIC package
- Monitors battery charge/discharge to determine remaining talk and standby time down to the minute
- Supports any battery chemistry
- Self-calibrating feature assures accuracy
- Low power drain: <80 µA operating, <10 µA in sleep mode or <100 nA in data-retention mode
- Single-wire control/ data serial interface
- 115 bytes user-programmable NVRAM store battery data, charge information, & ID codes

How It Works

The bq2018 *Power Minder* IC is a multifunction charge/discharge counter that works with an intelligent host controller to provide state-of-charge information for rechargeable batteries. The functional block diagram shows the bq2018 and bq2118 mini-board.

Charge/discharge is monitored via the low-value sense resistor, R1. A differential dynamically balanced VFC integrates the charge and discharge levels sensed by R1.



By using the accumulated counts in the charge, discharge, and self-discharge registers, an intelligent-host controller can accurately determine battery state-of-charge for any type of battery. Self-discharge is estimated using the internal temperature sensor and timer.

Host controller interface is via the HDQ serial line, allowing access to battery status registers, including read/write access to 115 bytes of the NVRAM (128 bytes total).

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tems like UL, which always require testing, there are several ways to justify a claim of compliance with a Directive.

- *EMC Directive (89/336/EEC amended 92/31/EEC):* The EU specification for EMC emission and susceptibility *(see Table 1)*.
- *Low-Voltage Directive (LVD) (73/23/EEC):* Safety requirements for equipment normally operating at from 50 to1000 V ac or 75 to 1500 V dc *(see Table 1, again)*.
- *New Approach:* A set of Directives intended to harmonize product safety throughout the EU.

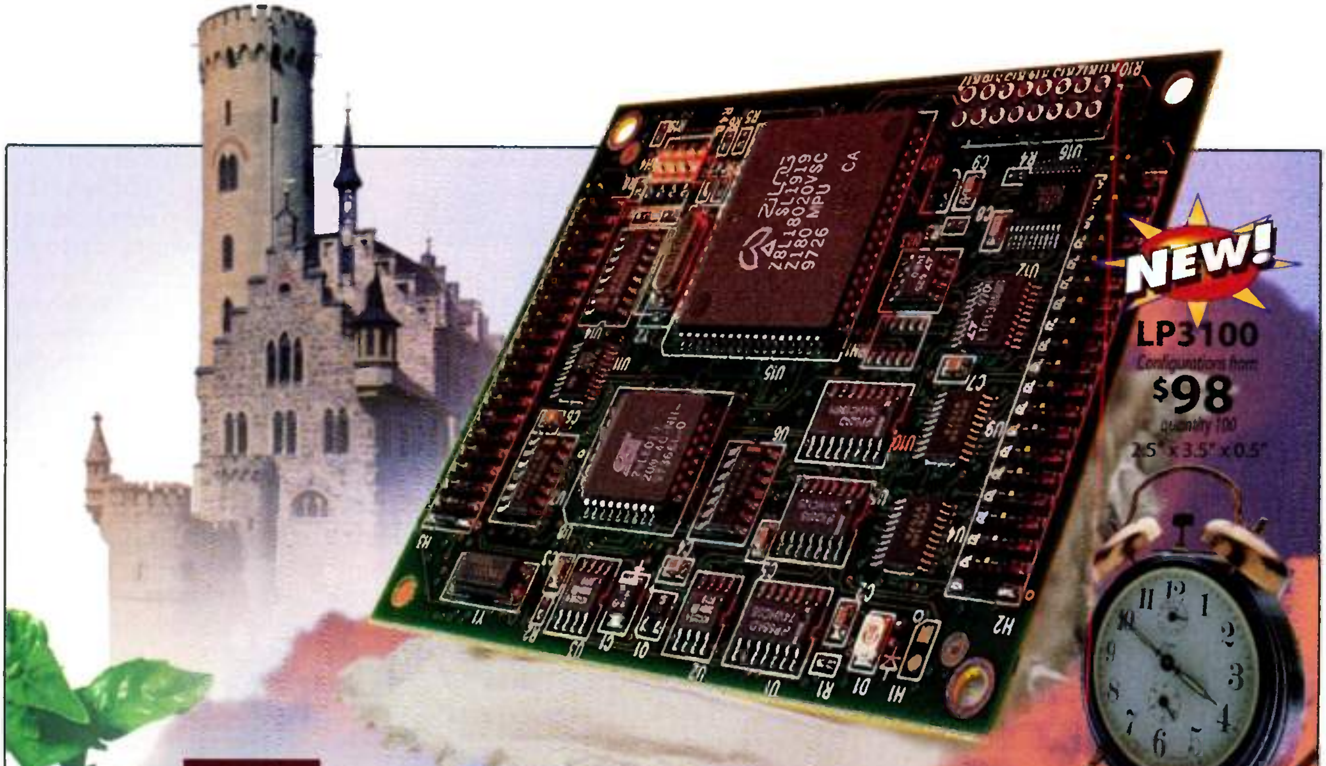
Due to the high cost of final compliance testing at specialized laboratories, many manufacturers have set up in-house facilities for precompliance testing, like this one for EMC emissions and susceptibility. Though not as rigorous as final testing, precompliance testing can save multiple trips to the contract lab.

Equipment meant for distribution or use in any European Union country must comply with the applicable directives. The directives lay down equipment requirements, and leave it to the standards, primarily European harmonized standards, to define the technical requirements. The manufacturer, or its European representative, must ensure that the product complies with applicable directives and CE mark the product.

Note that the CE mark does not claim conformance with a particular standard. A plastic toy duck and a TV set will both need the CE mark, although they meet totally different standards (toy safety was, in fact, the subject of one of the early directives).

Power-supply designers and users must consider the EMC Directive, LVD, and CE-marking amendment together, remembering that since Jan. 1, 1997, it is mandatory to CE mark under the LVD if the directive is applicable *(Table 2)*.

Even within Europe itself, there has been significant discussion about when a subassembly such as a power supply needs CE marking. Some guidelines have been established by the European Power Supply Manufacturers Association (EPSMA). A web site provides ac-



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INNOVATION IN CONTROL TECHNOLOGY

cess to these recommendations, but they are summarized below *(see Table 3)*.

All line-powered power-supply units fall within the LVD, and the EMC Directive applies to all standalone units. Thus both types of devices required the CE mark. Provided that their input and output are not within the voltage range of the LVD, dc-to-dc converters do not fall under the LVD regulations, so all that's left is the EMC Directive.

The basic requirement of the EMC Directive is that electrical equipment may not cause a disturbance, or be affected by reasonable disturbance levels in its environment. The directive covers radiated and conducted emissions, RF electromagnetic susceptibility, electrostatic discharge, and fast transients.

The guidelines to the Directive state that components performing no direct function, such as components of electrical or electronic circuits, shall not be CE marked, as the EMC Directive does not apply to them. This matches practical experience because the EMC performance will depend on the details of the components' installation in the final equipment. Although a recent revision of the guidelines modified the list of specified components having no direct function, and omitted the explicit reference to "power supplies intended to be incorporated in apparatus," the EPSMA recommends that the EMC Directive, and therefore the CE marking, is still not relevant to component power supplies such as dc-to-dc modules.

TABLE 2: APPLICABLE STANDARDS FOR POWER SUPPLIES

	EMC	LVD	CE
Component PSU in LVD range	No	Yes	Yes
Component PSU outside LVD range	No	No	No
Standalone power supplies	Yes	Yes	Yes

Unlike the process for approvals like UL, there are three routes to EMC compliance:

- *Self-certification (89/336/EEC Article 10.1):* Administratively, this is the simplest route, and may be achieved either with in-house testing or by a specialty test facility. The manufacturer declares that the products conform to the applicable harmonized European standards.
- *Technical Construction File (TCF) (89/336/EEC Article 10.2):* This requires a detailed record of drawings, specifications, design details, and full information to enable vetting by the authorities. The TCF should enable a competent body (usually an accredited laboratory) to vet the design and con-

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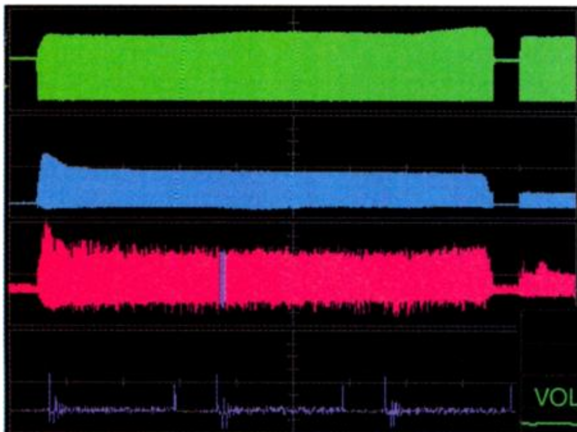

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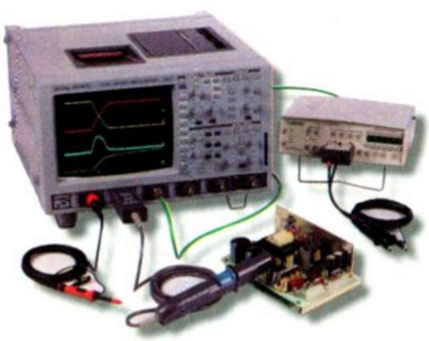

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firm that it would comply if retested independently. This route is used when the manufacturer has not applied the harmonized standards, or has applied them only in part, or applied them in the absence of relevant standards.

• *EC-type examination by a notified body (89/336/EEC Article 10.5):* This specialized route is applicable only to radio communications equipment.

The costs involved in using external services have led many companies to invest in in-house facilities to undertake so-called precompliance testing *(see the figure)*. Work is done in-house until the company believes that a product will pass the first time in compliance testing.

The facilities required for precompliance testing are less stringent, and are therefore, less expensive than full testing. Nonetheless, they allow engineers to more easily make the iterative design changes often required to reduce EMC problems. As usual, however, it is better to design out as many problems as possible from the beginning.

Even though a dc-to-dc converter is outside the LVD voltage range, and does not require CE marking, any equipment into which it is built will need to comply with the EMC Directive. Therefore, it is essential that the module be designed with the regulations in mind. In fact, designing converters to have low emissions and low susceptibility is critical to meeting the short time-to-market window many designers are facing. Allowing designers to meet this window is one of the major benefits of using on-board dc-to-dc converters.

EMC is becoming almost an industry in its own right, and considering the power supply's place between the line and the equipment, the supply has a key role to play. Although the performance is determined more by the layout of the equipment than by the supply itself, a few tips can enhance the advantage of using on-board dc-to-dc converters.

Using converters with built-in radio-frequency-interference filtering will minimize the disturbance on the supply lines. Practical experience shows that in order for the final equipment to meet the typical requirement of EN55022 class B, the converter must be designed with EMC control in mind, ideally meeting EN55022 class A. This sort of performance is only possible with LC-type filtering in the power module. Check the specification first.

When planning decoupling, the goal is to minimize path length and loop area. Dc-to-dc converters offer a significant intrinsic ability to decouple fast transients close to the load, minimizing the antenna effect of long supply lines. Keep any additional output filtering below 100 µF/A to avoid longer settling times and reduced stability.

A number of smaller-value capacitors, evenly distributed around the board, will be more effective than a single component, especially for the high-frequency decoupling. Don't forget that while parallel capacitors are additive, parallel resistance and inductance reduce, providing a double gain in the time constant.

An earth or ground plane in the printed-wiring board will not only provide some screening, but improve the EMC performance. It does this by introducing distributed decoupling capacitance for the highest frequencies, and reducing the inductance in both the ground path and signal distribution.

Surface mounting offers significant benefits in terms of reduced lead inductance and high-frequency radiation from the leads and traces. With surface-mount dc-to-dc converters now available that can handle up to 15 W, this is an increasingly practical and effective option.

The SLIM Initiative And EMC

The European Commission has recognized the complexity of the legislation that has established the Single Market, and in May 1996, it embarked on a program of simplification known as the Simpler Legislation for the Single Market (SLIM). The activity is planned to be completed in phases, with the EMC legislation coming under attention in phase III.

The SLIM team's report is expected to be presented by the end of the year, complete with conclusions and recommendations, which it is hoped will streamline and reinforce the Single Market concept.

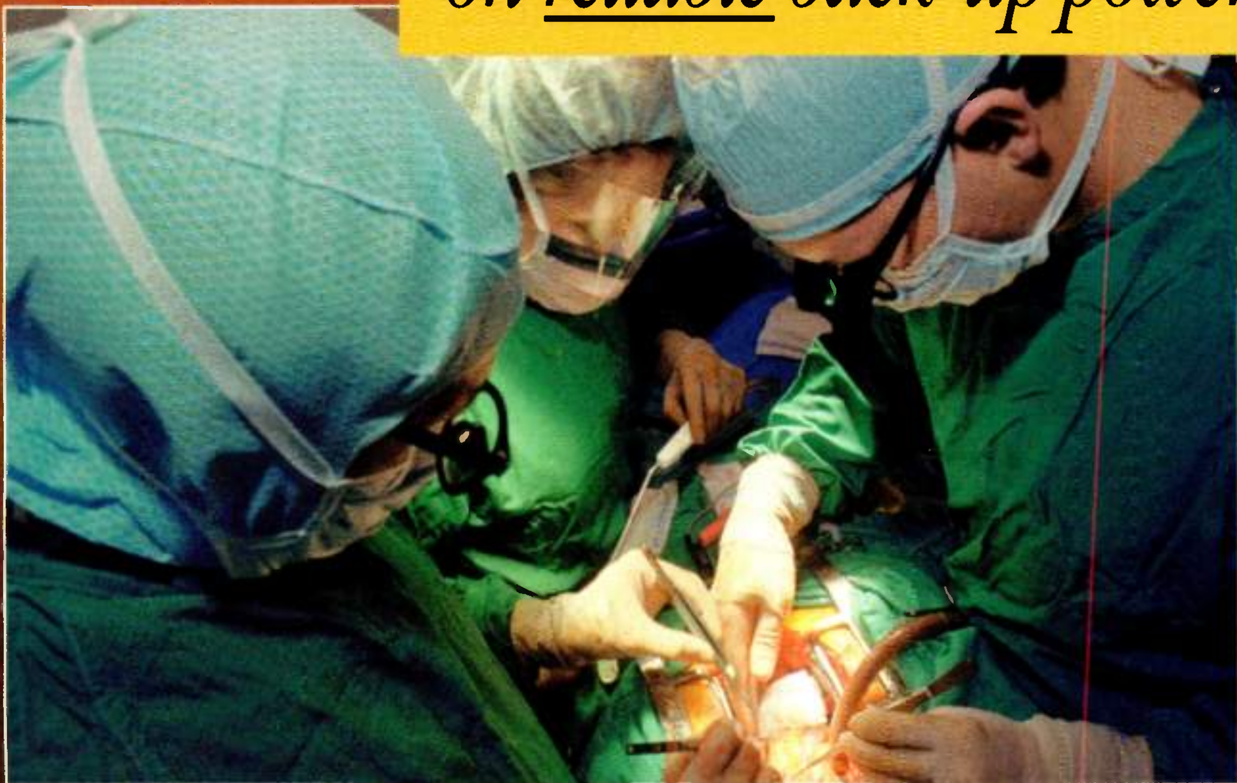
In closing, please remember that the EU legislation has teeth. Equipment found to contravene the EMC Directive can be seized and banned from sale throughout the EU. In addition, the penalties for knowingly supplying or CE marking noncompliant equipment include fines and imprisonment.

Per Lindman is a system analyst in strategic marketing at Ericsson Components' Power Modules Division. He received his MSEE from the Royal Institute of Technology, Stockholm, Sweden. He has authored several articles for professional journals and conferences. Lindman is a power- supply expert in the IEEE Future Bus+ Working group, and is a committee member of the EPSMA.

TABLE 3: SOME USEFUL INTERNET SITES

Internet address	Content
www.open.gov.uk/radiocom/emc/emc.htm	European commission's guidance document to the EMC Directive 89/336/EMC
www2.echo.lu/nasd	EU standards and directives
www.cix.co.uk/~approval	The engineering guide to European quality, standards, and regulations. Includes UK DTI guidance notes and list of standards.
www.safetylink.com/lvd.asc	Full text of the Low-voltage Directive
www.safetylink.com/	Useful links to safety and compliance sites
www.emc-journal.co.uk	UK EMC journal site
www.lyons.demon.co.uk/epsma.html	CE marking on power supplies; guidance from the EPSMA
www2.echo.lu/nasd/whatsnew.html	Updates on new EU regulations or amendments
world.std.com/~techbook/seec2_l.htm	Introduction to sce.engr.electrical.compliance newsgroup
world.std.com/~techbook/seec2_3.htm	EMC FAQs and net sources
www.netc.ie/lvdfaq.htm	Useful list of FAQs on the LVD, National Electronics Technology Center, Dublin, Ireland

Can you really put a price on reliable back-up power?



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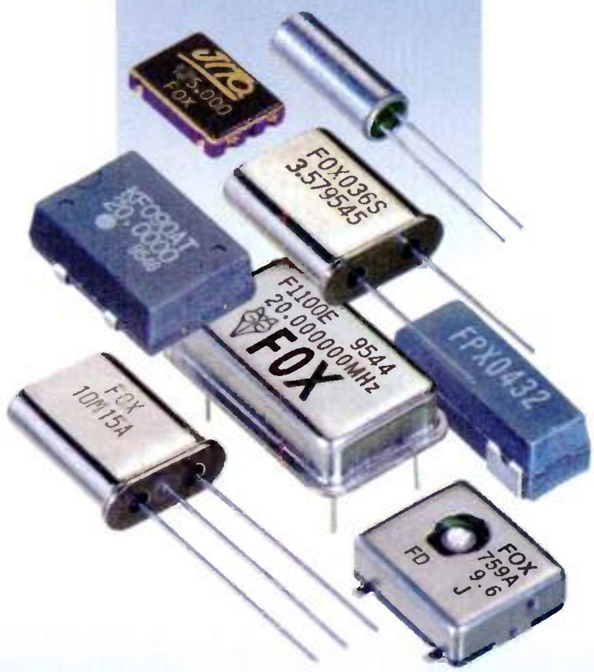


FOX036S
3.579545
F1100E 9544
20.000000MHz
FOX
FOX
10M15A
FPX0432
FOX
759A
9.6
J
FD

Buck Regulator Answers Portable Challenges

Multiple Voltage Levels Add To An Already Complex Puzzle Of Space, Heat, And Transient-Response Requirements.

Bruce D. Moore
Maxim Integrated Products, 120 San Gabriel Dr., Sunnyvale, CA 94086; (408) 737-7600; fax (408) 737-7194.

As portables, like notebook computers, PDAs, and barcode readers get slimmer, lighter, and sexier, the demands on the power electronics continue to rise. Along with the numerous low-voltage supply rails have come brutal, zero-to-maximum-CPU-load transients that characterize power-minimizing, clock-throttling techniques. All this is coming at a time when the shrinking size of notebooks makes waste-heat dissipation a serious problem for system, thermal, and mechanical designers.

For the moment, the classic solution—the standard buck topology—remains the design of choice. Armed with the latest MOSFETs and inductors from the desktop world, the buck topology can tame the waste-heat problem as well as any esoteric configuration. In addition, new controllers, tailored to the demanding CPU loads, allow the hot dc-dc circuit to be placed at least somewhat distant from the already-hot CPU. However, designers can employ a number of additional techniques to mitigate these electrical and thermal problems. Although the techniques used for managing future power needs currently apply to notebook computers, soon they will be used with a broader range of portable and handheld equipment.

Upcoming Power Needs

As chipset supply voltages migrate downward, the main power distribution rails in a typical notebook are shifting from 5/3.3 V down to 2.5/1.8 V. These lower voltages, which don't exist in today's systems, power RAMbus, RDRAM, and chipset rails, are scheduled to appear in notebook systems in 1999.

Regardless of what the CPU supplies do, motherboard supplies are becoming more complicated as new voltages are introduced, without getting rid of old power supply rails first. For example, the move from 3.3 V to 2.5 V for DRAM won't eliminate 3.3 V for a long, long time, due to the legacy of 3.3-V Cardbus cards. At some point, the 12-V rail might disappear, but even that won't happen soon.

Along with dropping voltages, the complexity of notebook power supplies has been evolving at a tremendous rate. Six years ago, we were seeing only one supply rail (5 V), sometimes obtained by powering the entire system directly off a naked stack of four NiCd cells. In 1999, there will be at least seven rails (12, 5, 3.3, 2.5, and 1.8 V, plus $V_{I/O}$, and V_{CORE}). Amazing!

Topology Choices

As more supply rails appear, our job as power-supply designers is to make each dc-dc converter physically smaller while generating less heat. Accomplishing this mandates a complete reexamination of the fundamental power-supply design products available, and specific tricks and trade-offs used—particularly for the demanding CPU core supply.

Choosing the right switching topology can be vexing. There are a surprising number of choices, each with merits and drawbacks. Sadly, many of the niftier choices from past designs are unusable today. For example, linear regulators, desirable due to their fast transient response, are now forbidden because their efficiency (equal to V_{OUT}/V_{IN} to a first order) has gone downhill as voltages have dropped. At sub-2-V levels, even the most minimal 200 to 300 mV of headroom needed for adequate transient response makes the waste-heat picture bleak. So, linear regulators are out, even when used as post-regulators to improve the transient response of switch-mode supplies.

Coupled-inductor buck regulators, which stack a flyback winding on top of the main buck output to generate a second output almost for free, are tempting as an easy way to make V_{CORE} and $V_{I/O}$ simultaneously. However, the exact value of V_{CORE} is a fast-moving target (a colleague jokingly calls it "voltage du jour"), which could force a painful transformer re-design with every processor upgrade. Most other multiple-output schemes must be rejected for this reason, or due to low efficiency or poor cross-regulation.

Some topology candidates do make it through the initial weeding-out process *(see the table)*. Efficiency is listed two separate ways because of the importance of the impact worst-case waste-heat generation has on thermal design.

Three-Terminal Devices

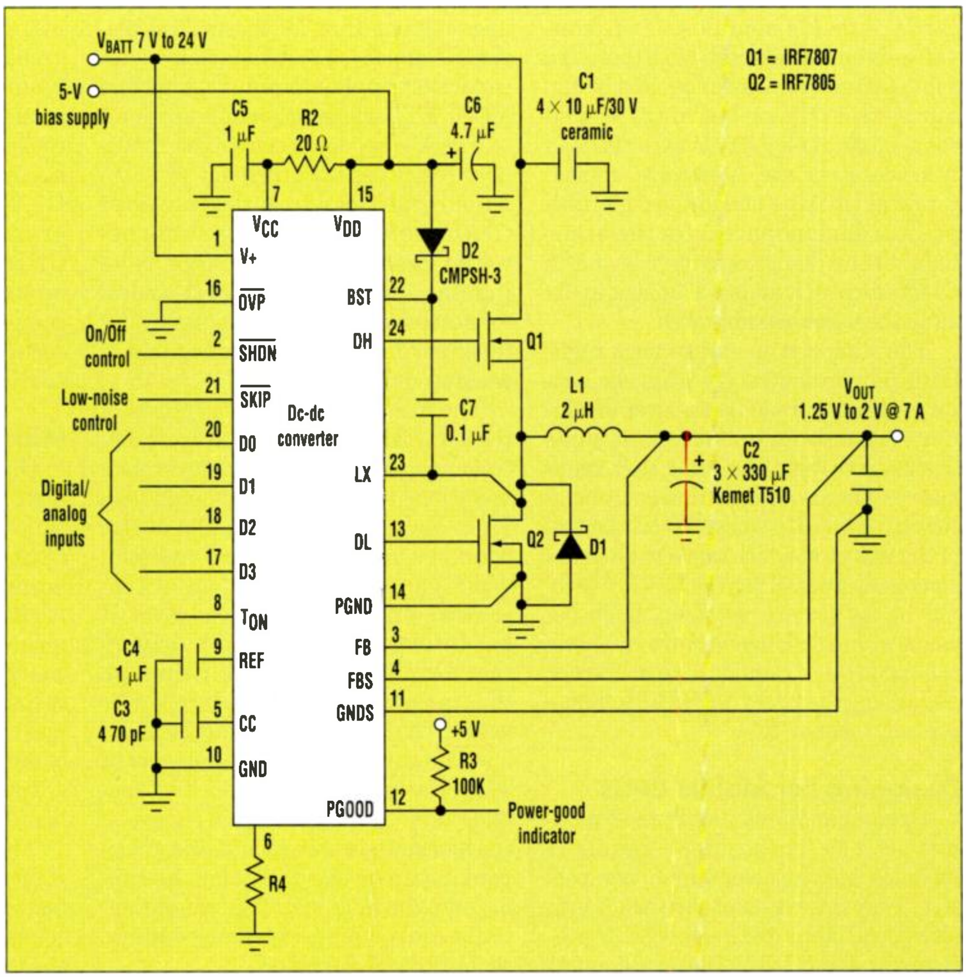
The three-terminal autotransformer buck topology is interesting because it can be employed to adjust the duty factor by changing the turns ratio. This eases the power-dissipation burden on the synchronous (low-side) switch, which otherwise sees greater than 90% duty. Equalizing the duty between high- and low-side switches also helps when designing the pulse-width-modulation (PWM) control loop, because extremely short control-switch on-times are avoided. However, the switch-stress voltage and switching losses are increased—and you have to add an extra termination to the inductor (an expensive redesign when the total series resistance needed for good efficiency is less than 4 mΩ).

High-Frequency Converters

The classic forward converter also is nice, because it deals effectively with high input/output-voltage ratios, and can be made small enough to be placed close to the CPU. But the need for a transformer, and the extra complexity of two magnetic components, makes the forward topology unattractive.

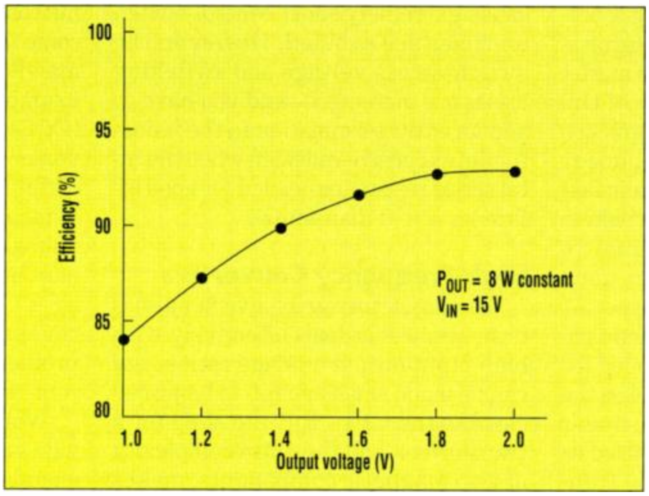
On the surface, resonant-mode topologies look promising due to small component sizes. However, under the microscope, these topologies all show some fatal flaw when placed in the demanding notebook environment. For example, the zero-current-switching (ZCS), parallel-resonant buck converter has high peak currents (bad for efficiency due to I^2R losses) and hideous output ripple, while the zero-voltage-switching (ZVS), quasi-resonant buck has high switch-stress voltage; needs a back-to-back, reverse-blocking MOSFET; and has problems dealing with wide load-current variations.

While the resonant schemes do provide very small size, all of the schemes examined have penalties in terms of efficiency and waste heat when compared to conventional buck regulators. Why make a tiny dc-dc converter that you can place close to the CPU (for



1. Today's power-management solutions must juggle numerous conflicting requirements. Many of these challenges are being met by highly integrated converters/controllers which avoid wasteful current-sense resistors, and by brawny MOSFET gate drivers that lower ac losses. Also, features like two-wire remote sensing allow the heat-generating controller to be located at a distance from the CPU.

good transient response), when it can overheat your already-hot CPU?



2. This graph shows the efficiency of a 7-A notebook CPU circuit that uses an IRF7807 high-speed MOSFET (an experimental device at the time) optimized for PWM use. Note the dramatic drop-off in efficiency as the output voltage is reduced from 2 V to 1 V.

Buck Converters

Two-stage buck regulators, where a miniature, fast dc-dc converter is powered from the system 5-V supply rather than the battery, will win out in some designs. Small, local converters can be placed very close to the CPU, where they can rely on the existing bank of ceramic bypass capacitors for output filtering. This raises the partitioning issue of where to place the CPU V_{CORE} dc-dc converter.

For manufacturing ease, modern notebook CPUs are usually placed on daughter-cards or inside modules. If the converter is on the motherboard, there are a lot of parasitic resistances and inductances from the pc-board traces and connectors to play havoc with the load transient response. A massive "capacitor farm" may be needed to cope with pc-board impedances. On the other hand, if the dc-dc converter is on the daughtercard, it adds waste heat in exactly the worst possible area.

The standard one-stage buck regulator powered directly from the battery still appears to be the overall winner, depending, of course, on your design priorities. The basic buck regulator is elegant, simple, and extremely tough to beat. Its worst flaw is the size of the inductor, which tends to push the converter away from the CPU (which, maybe, isn't such a bad thing, again, because of heat). However, we can hone the basic buck regulator to a sharper edge using the latest MOSFETs, inductors, and control ICs.

Designing For Mobile CPUs

Upcoming Mobile Pentium II modules act a lot like desktop Pentium II modules from a power-supply perspective. They draw a lot of current (7 A) in sharp load steps and need good dc precision at about 1.5 V. One version has voltage-identification codes (called "VID codes" in the desktop world) present on connector pins to set the power-supply voltage. The worst-case continuous current draw for thermal calculations is about 5.5 A, which helps with capacitor ripple-current ratings and MOSFET package-power dissipation.

The V_{CORE} dc-dc converter shown here features 90% efficiency *(Fig. 1)*. An integral digital-to-analog converter (DAC) sets the output voltage between 1 and 2 V in 50-mV steps. Note that the 4-bit DAC codes (VID codes) for notebook CPUs are completely different from the 5-bit codes used in desktop computers.

The MAX1710, which is typical of the many fast, high-precision dc-dc controllers available today, has several innovations that designers should look for in V_{CORE} applications. The device requires no current-sense resistor, which gains the circuit at least 4% increased efficiency at any load level. It has brawny MOSFET gate drivers that force the FETs quickly through the transition region to ensure low ac losses. The 3-A pull-down device in the low-side gate driver is especially beefy. This prevents parasitic capacitive coupling (due to the gate-drain charge of the monster synchronous switch) from yanking up on the gate when its supposed to be held low. This can potentially cause noisy, efficiency-killing, shoot-through currents.

Two-Wire Remote Sensing

Two key circuit blocks allow this battery-powered converter to be located remote from the CPU, while providing nearly the same transient response as a two-stage local converter operating at 1 MHz. First, dc voltage drops in the ground, and power buses are dealt with by an uncommon, two-wire remote sensing scheme. This scheme requires a total of four pins on the controller: the fast feedback and ground (FB and GND) pins regulate large dynamic changes seen at the converter, while the slow feedback and ground-sense (FBS and GNDS) pins regulate the remote dc voltage at the CPU.

The integrated remote-sense signal is summed into the fast feedback loop with just enough gain to correct for 25 mV of ground or power-bus drops. Some chips have separate power and analog ground pins (PGND and AGND), but really need to have both these pins connected to the ground plane close to the IC. This new class of chip has three ground pins—PGND, AGND, and GNDS—allowing the GNDS trace to be snaked around the pc board to the remote load while keeping the analog section of the IC quiet (by connecting AGND close to the IC).

Making A "Fast Buck"

Once the dc drops are dealt with, the next problem is pc-board trace resistance and inductance. The solution here, as in most situations, is to put a large portion of the required bulk capacitance fairly close to the CPU. To make this work in practice, your dc-dc controller must have a fast transient response and a stable feedback loop. It must have this stability in the presence of fairly high values of capacitor-series resistance caused by the added pc-board resistance.

The instant-on nature of the constant-on-time PWM gives this circuit a fast response. When a nasty load step comes along and causes the output voltage to sag, the PWM turns on the high-side MOSFET within 100 ns of the load step, and dumps massive amounts of current into the load. This admittedly whacks the battery supply pretty hard,

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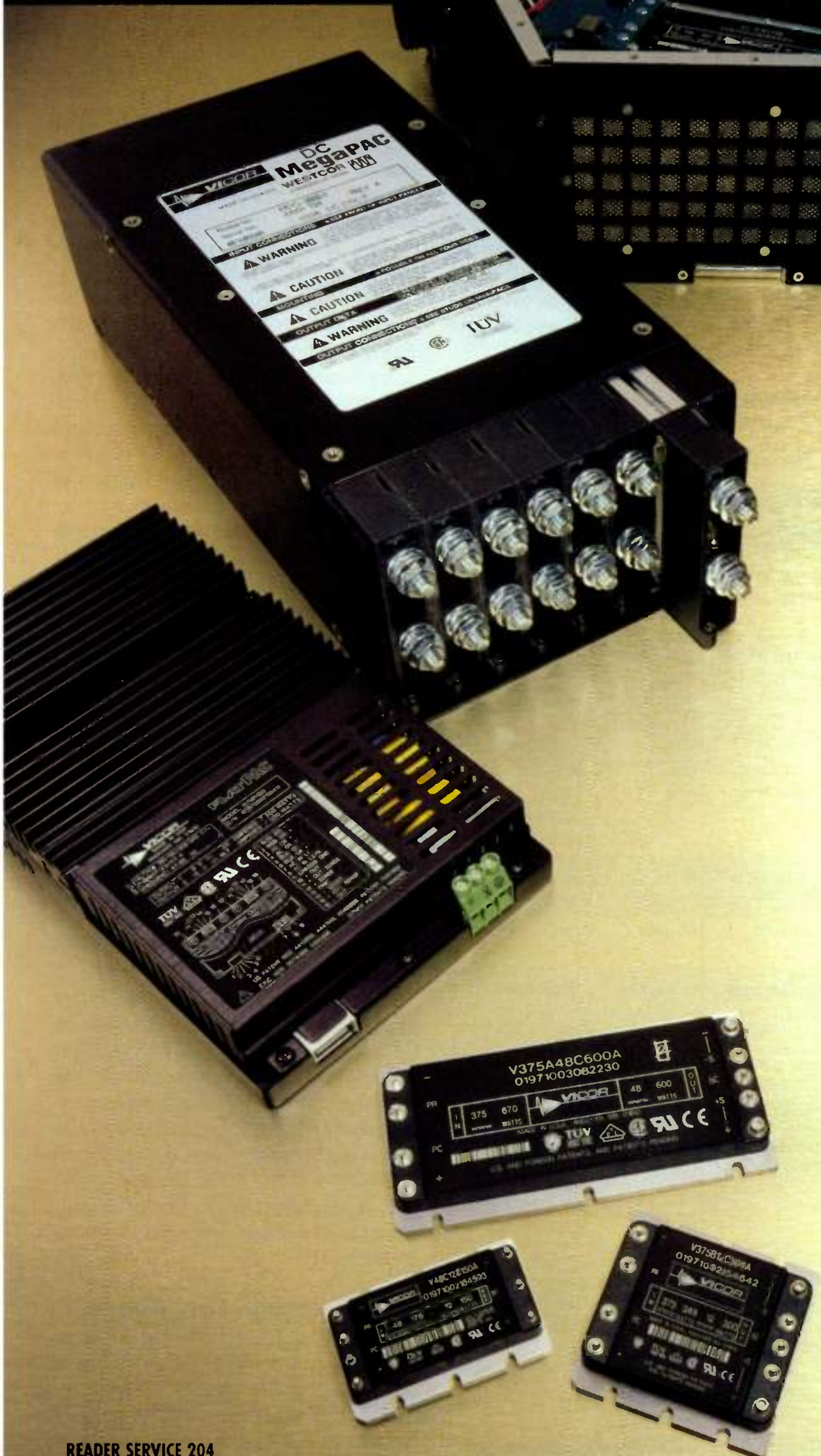

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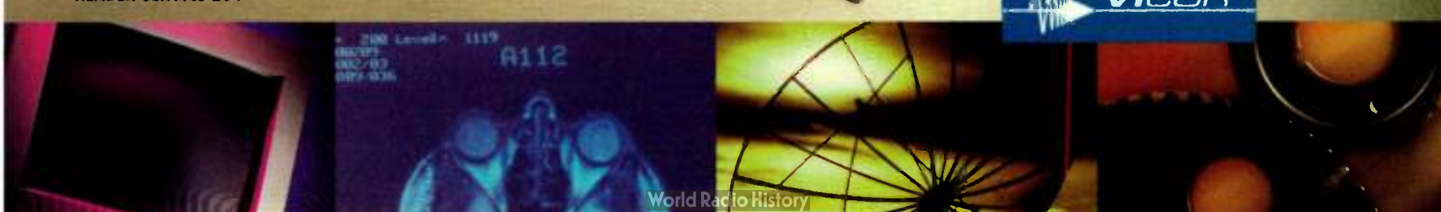

but the surge-current problem is much easier to deal with at 15 V than down at 1.5 V. This is a result of the less-stringent voltage tolerances and greater energy-storage capability of capacitors up at the battery voltage level.

The V_{CORE} converter is designed for a wide range of input voltages. The circuit here accepts inputs from 7 to 22 V, which accommodates the entire input-voltage spectrum—from a discharged, three-cell, lithium-ion battery to the maximum ac adapter voltage seen in four-cell systems when the battery has been removed.

There's a 5-V power input as well as a battery input, so that gate-drive power can be derived from the highly-efficient system 5-V supply, rather than inefficiently from the battery by way of a linear regulator. The lack of this particular feature (a 5-V linear regulator for chip biasing and standalone capability) indicates how specialized dc-dc controller chips have gotten, to the extent that a complex, feature-laden, 24-pin device must have another IC generate the chip bias power.

Newer Inductors And MOSFETs

As usual, the maximum input voltage and the switching frequency dictate the inductor size. Frequencies in the range of 200 to 400 kHz are the sweet spot for use with today's MOSFETs. Operating moderately deep in the continuous-conduction region, with 30% inductor ripple, provides a good compromise between efficiency and transient response. These design decisions dictate a 2-µH, 10-A inductor. Fortunately, the cutthroat, high-volume desktop market has created some excellent low-cost surface-mount inductors from companies such as Coilcraft, Coiltronics, Panasonic, and Sumida, among others. For this design, a 2.2-µH, ferrite E-core design having flat wire is chosen, thanks to a winning combination of small size and low dc resistance.

There's a small, but vicious struggle occurring between the three leading-edge notebook MOSFET manufacturers—namely Fairchild, South Portland, Maine; International Rectifier, Segundo, Calif.; and Vishay-Siliconix (formerly Temic), Santa Clara, Calif. Each wants to dominate the expanding market for dc-dc-optimized, 30-V, SO-8 MOSFETs. Each company also tries hard to improve switching speeds by reducing gate charge while simultaneously reducing $RDS_{(ON)}$ to sub-5-mΩ levels. International Rectifier is winning at this time, but before shipping a new design, you should call each company for samples of their latest devices to evaluate your prototype board's efficiency.

Shown in Figure 2, this efficiency graph was made with the 7-A notebook CPU circuit using an IRF7807 high-speed MOSFET optimized for PWM use. The low-side MOSFET was an experimental device, not available to the public at the time of writing, but it will probably be out by the time you read this. Note the dramatic drop-off in efficiency as the output voltage is reduced from 2 to 1 V.

CPU V_{CORE} TOPOLOGY COMPARISON

Name	One-stage buck	Two-stage buck	Resonant-mode	Forward converter	Auto-transformer buck
Description	<500 kHz synchronous buck powered from V_{BATT}	>1 MHz synchronous buck powered from 5 V	Various >1 MHz switchers, such as quasi-resonant, ZVS or ZCS buck	1 MHz push-pull transformer smoothing coil, synchronous rectifier	Tapped inductor with synch switch at center tap
Efficiency (waste heat)	85%	Compounded losses: 90% x 90% = 81%	70% to 80%	80%	83% (increased ac losses vs. buck)
Efficiency (battery life)	90%	87%	Usually poor at light loads	85%	89%
Transient response	1 to 10 µsec; can be improved	<0.5 µsec	<0.5 µsec	<1 µsec	<1 to 10 µsec
Output noise	Low ripple subject to line transients	Best; lowest ripple, pre-regulated input	Excess ripple	Low ripple	Low ripple
Size	Benchmark	Approx. 70%	50% to 60%	Approx. 75%	Same as buck
Partitioning	Big inductor, belongs on motherboard	Can be near CPU for better transient response	Can be near CPU for better transient response	Possibly near CPU	Big inductor, belongs on motherboard
Complexity	Very good	Very good	OK to poor	Poor	Good
Component stresses	Good; low-side switch has high current at >90% duty	Very good; switch voltage stress is only 5 V	Usually have either high switch stress voltages or high switch currents	Higher switch stress voltage	Higher switch stress voltage, depends on pri:sec ratio
Cost	Good	Best, but 5 V supply affected	Esoteric components	Poor due to complexity	Good
Comment	Still best overall	Close runner-up; always suffers more waste heat	Too many problems; ultra-small, but never best efficiency	Classic military way of getting high efficiency with wide in/out ratios, too complex, expensive	Equalizes duty ratio between high- and low-side switches

Output-Voltage Error Budget

In many cases, the published specs for CPU dc voltage tolerances, transients, and ripple voltages set requirements on each of the ac and dc accuracy parameters. In particular, the allowed ripple, dc error, and transient response are often specified separately. However, the real need, based on numerous discussions with CPU architects and process design engineers, is to main-

tain the voltage at the CPU pins within a specified window. The power-supply designer should feel free to make whatever design decisions that result in the best overall converter, allocating the error budget as needed between ac and dc errors.

For example, take a hypothetical CPU whose datasheet specifies 1.5 V ±2% dc error, plus 1% peak-to-peak ripple and 2% transient load regulation. What this spec is really saying is that there's a ±4.5% window around 1.5 V. The dc-dc designer should meet this ±4.5% window without regard to the ±2% dc accuracy spec. A tighter dc accuracy in the controller IC, for example, allows for greater noise and ripple, a fact that can be taken advantage of by reducing the size and cost of the output filter capacitors.

Staying In The Window

In addition to budgeting the error sources to meet their own priorities, savvy designers will read between the lines of the spec, and violate it selectively where and when it makes sense to do so (at this moment the author offers up a prayer to the great CPU god that he will not strike the author down for his insolence). For example, it's usually not necessary to maintain ±2% dc accuracy when the load is less than one-quarter of the full load. Instead, it's allowable (and actually desirable for better transient response) to let the output float, perhaps 1% high, when in light-load, pulse-skipping mode.

The upper limit of the voltage window is determined by the thermal limitations of the CPU. The CPU manufacturers will also say that you shouldn't exceed this value because that's the point where the CPU is tested. Realistically, however, allowing the voltage to float 1% high under light loads isn't going to hurt anything. Similarly, a momentary 1% overshoot when going from heavy to light load isn't going to be a problem. The upper limit of the voltage window is really determined by thermal issues, not transients.

In contrast, the lower limit to the voltage window is a much more sacred barrier. If the voltage ever dips below the magic line, even for a microsecond, data may be corrupted, and the computer may lock up. So, don't push your luck on the lower limit. Improve the transient response of your converter by reducing the inductor value until all the bad effects of high inductor ripple become a headache, back off a little, then pile on the local bypass capacitors to finish the job of staying within the window.

Bruce Moore is a senior scientist with Maxim, where he is responsible for power-supply applications. In his seven years at Maxim, he has developed precision op amps, linear arrays, and power-supplies for notebook and palmtop computers. Moore graduated with a BSEET from Heald Engineering College, San Francisco, Calif., in 1977, and is attending San Jose State University, Calif.

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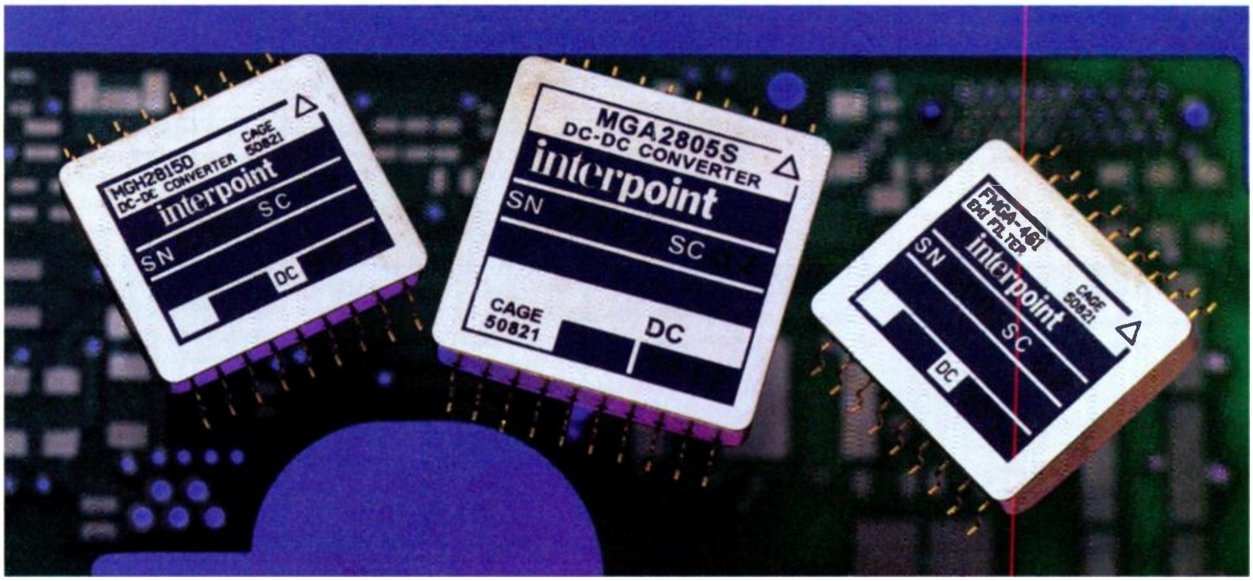

Model	Output	Outputs (V)	Input (V)	Operating Temp (°C)	Case Size Inches (mm)
MGH Converter	Power 1.5 W	5, 12 or 15 single 5, 12 or 15 dual	Continuous: 12–50 Transient: 80 V/120 msec	–55 to +125	1.010 x 0.880 x 0.250 (25.65 x 22.35 x 6.35)
MGA Converter	Power 5 W	5, 12 or 15 single 12 or 15 dual	Continuous: 16–40 Transient: 50 V/50 msec	–55 to +125	1.110 x 1.110 x 0.250 (28.19 x 28.19 x 6.35)
FMGA Filter	Throughput Current 0.8 A	**Noise Reduction** 40 dB minimum at 200 kHz 60 dB minimum at 500 kHz and 50 MHz		–55 to +125	1.010 x 0.880 x 0.250 (25.65 x 22.35 x 6.35)

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PRODUCT UPDATE: SWITCHING POWER SUPPLIES

Manufacturer	Device	Description	Price and delivery	CIRCLE
Astec **Carlsbad, CA** **Tom Tillman (760) 930-4708** **Fax (760) 930-4700** **E-mail: tomtillman@astec.com**	LP series 40- to 60-W medical supplies	As an addition to the company's LP series, these switchers come in 40- and 60-W versions. The devices meet UL 2601, IEC 601, and CSA 22.2 no. 125 low-leakage current standards for use in non-patient-connected devices. A built-in filter ensures conformance to noise-emission standards such as FCC Class A, CISPR 22 Class A, EN55022 Class A, and VDE 0873 PT3 Class A. The supplies have both single (5- to 24-V dc) and triple (5- and ±12- and 5- and ± 15-V dc) outputs. The inputs autorange from 85 to 264 V ac or 120 to 370 V dc, with an input frequency of 47 to 440 Hz. The footprint is 3 by 5 in.	$35 to $45; samples in third quarter	554
	VS series three-phase switcher	Available in 2500-W versions, these three-phase supplies operate off 185 to 264 V ac and can be configured with up to 12 outputs in any combination from 2- to 48-V dc. Targeting industrial and instrumentation applications, the devices come with protection and status indication. Features include UL, CSA, CE, and IEC compliance; operation under phase-loss conditions; and pin compatibility with single-phase models.	$0.50/W in quantity; four to six weeks	555
Astrodyne **Taunton, MA** **Paul Charrette (508) 823-8080** **Fax (508) 823-8181**	500-W to 2-kW switchers with PFC front ends	Rated at 500, 600, 1200, or 2000 W, these SMPSs come in package sizes down to 7.3 by 4.8 by 3.7 in. and include a power-factor-corrected (PFC) front end of up to 0.99. Outputs of 5, 12, 15, 24, or 48 V are available, while the input can handle voltages of 88 to 264 V ac. Features include foldback-current-overload protection and output overvoltage protection. The operating temperature range is -10º to 50ºC and UL1950 and EN60950 approvals have been obtained.	$149 (500 W) to $999 (2 kW); four to six weeks	556
	OFM series, miniature, open-frame switchers	Measuring 2.28 by 1.8 by 0.83 in. (5-W version), these open-frame modules are available with ratings of up to 15 W. Available in 12 versions, the modules accept inputs of 85 to 265 V ac, and provide single outputs of 5 to 24 V dc. Features include an integral power-good LED, an output adj. potentiometer, and an operating temperature range of 0º to 45ºC. The devices are UL, CSA, TUV, and CE approved.	$17 each in quantity; stock to two weeks ARO	557
Deltron Inc. **North Wales, PA** **Jack Philips (215) 699-9261** **Fax (215) 699-2310**	V series 120 to 600 W; single output	Available in ratings between 120 and 600 W, these single-output supplies have an MTBF of over 200,000 hours. The supplies include a proprietary proportional drive circuit that prevents excess switch saturation, and allows higher switching-frequency operation. The devices measure from 8.5 by 4.75 by 2.5 in. to 10.5 by 4.75 by 2.5 in. Additional features include 80% efficiency, dual-line spike suppression, a power-fail monitor, and a thermal-shutdown circuit.	$135 to $322 each in quantity; available from stock	558
	FT series 600-W supplies with PFC	Offering 600 W of 0.99-PFC power, these supplies have from one to six outputs, and feature UL, CSA, TUV (IEC, EN), and CE approvals. Including built-in fans, the modules measure 2.56 by 5.08 by 10.03 in., have a universal input, and are fully regulated. Overload, overvoltage, and short-circuit protection is provided, while options include a power-fail monitor, redundancy, and current-limited or enhanced outputs.	$445 to $569 each in quantity; stock to six weeks	559
Digital Power Corp. **Fremont, CA** **Bruce Haug (510) 657-2635** **Fax (510) 657-6634** **www.digipwr.com**	UPF150; 150 W with multiple outputs	Featuring active PFC to 0.98, this supply takes an input of between 90 and 264 V ac, measures 6.8 by 3.8 by 1.5 in., and can be configured for any voltage from ±2 to ±48 V. All standard models are scheduled for UL1950, UL, and TUV safety approval.	$141 each per 100 (single output)	560
EOS Corp. **Camarillo, CA** **Sales Dept. (800) 293-9998** **Fax (805) 484-5854** **E-mail: info@eoscorp.com** **www.eoscorp.com**	VLT 60; "world's smallest" 60-W SMPS	Measuring 2 by 4 by 1 in., this multi-output, open-frame SMPS is offered as the "world's smallest" 60-W power system. The supply features an efficiency rating of over 85%, has output voltages of 24 V dc down to -15 V dc, covers an input range of 90 to 264 V ac, and has an MTBF of up to 300,000 hours. The device meets worldwide safety standards, including FCC and CE.	$39 to $43	561
Melcher Inc. **Chalmsford, MA** **Sales Dept. (888) MELCHER** **Fax (978) 256-4642** **www.melcher-power.com**	PSS/PSK rugged switching regulators	Packing an efficiency figure of up to 97%, these rugged switching regulators output up to 576 W without any need for heatsinking or forced-air cooling. The units measure 60 by 168 by 111 mm, operate over the temperature range of -40º to 71ºC, run off up to 114 V dc,and output voltages of 0 to 48 V at 9 or 12 A. The devices can be supplied directly from a battery or transformer, and comply with CE, SEV, UL1950, IEC/EN60950, and CISPR 14 regulations, as well as various EMC standards.	$300 each per 1000	562
Pioneer Magnetics **Santa Monica. CA** **Sales Dept. (800) 269-6426 ext. 628** **Fax: (310) 453-3929** **E-mail: pmimag@ix.netcom.com** **www.pioneermag.com**	PMI1450 hot-plug rack system	Designed for glitch-free operation in critical applications, this hot-plug power system uses the company's line of 99.9% PFC supplies. The system can provide from 3 to 15 kW in a standard 3U, 19-in. rack, or from 4 to 20 kW in a standard 3U, 24-in. rack. The supplies come in 5- by 5-in. modules, each capable of handling from 1 to 5 kW; standard voltages are from 1.2 V to 60 V dc.	$0.30/W	563

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READER SERVICE 243

READER SERVICE 164

Hot-Swap DC Power Modules Include Battery Backup

The PD-200 Series of 200- to 240-W N+1 hot-swap dc power supplies come with a battery-backup option and an MTBF in excess of 1 million hours. The supplies come in a closed-frame, 3U DIN configuration with nominal input voltages of 24, 48, and 300 V dc. The series is fully scalable and available with one to four outputs from 0 to 24 V dc. Targeting mission-critical applications, the supplies have an efficiency of 75%, a line regulation of 0.2%, a typical load regulation of 0.5%, a transient response of 400 µs, and an operating case temperature of –40° to 100°C. The units measure 5.06 by 2 by 6.30 in., and weigh approximately 1.7 lb. Pricing starts at $298.

Power & Data Technology Inc., *81 Great Oaks Boulevard, San Jose, CA 95119; Stewart Nowak (800) POWER-85; fax (520) 204-9799; e-mail: snowak@powerdatatech.com; Internet: www.powerdatatech.com.* **CIRCLE 455**

Converter Outputs 3.3 V At 5, 10, And 15 W

Measuring 1.0 by 2.0 by 0.375 in., this 2:1 wide-input-voltage converter has a single 3.3-V output with a line and load regulation of ±1%. With an efficiency of 86%, the 5-, 10-, or 15-W converter use a switching frequency of 200 kHz. It has a ripple and noise level of 50 mV p-p. The operating temperature range is –25° to 71°C, and protection includes short circuit and overvoltage. Pricing is $29 each in quantity; delivery is eight weeks.

Polytron Devices Inc., *P.O. Box 398, Paterson, NJ 07544; Sheri Lynn (973) 345-5885; fax (973) 345-1264; e-mail: polytron@erols.com; Internet: www.polytrondevices.com.* **CIRCLE 456**

Secondary Batteries Provide Reliable Power Backup

Based on manganese-dioxide-lithium material, the ML1220, 2016, and 2430 batteries have capacities of 12-, 25-, and 90-mAh, respectively. Ideal for low-

drain current backup applications, the batteries come with multiple pin-out options in through-hole and surface-mount configurations. The series delivers up to 10-µA discharge current for up to one year. The cycle life depends on discharge depth, with life cycles of up to 3000 achievable at 5% discharge depth. Typical applications include PC Cards and other thin-format devices. Pricing is $2 each in volume; delivery is from stock to 16 weeks ARO.

Plainview Batteries Inc., *23 Newton Rd., Plainview, NY 11803; Timothy Votapka (800) 642-2354; fax (516) 249-2876.* **CIRCLE 457**

READER SERVICE 185

16-Bit GPIB Card Controls Four-Quadrant Supplies

The BIT 4886 is a 16-bit GPIB controller card for the company's line of four-quadrant BOP high-speed operational amplifiers. The card can be factory installed in new supplies, or may be added to existing 100-, 200-, or 400-W BOP models. The BOP supplies are rated from ±20 to ±200 V and the card resolves to 0.0015%. Pricing is $849; delivery is from stock to 30 days.

***Kepco Inc.**, 131-38 Sanford Ave., Flushing, NY 11352; (718) 461-7000; fax (718) 767-1102.* **CIRCLE 458**

Maxim-Compatible Transformers Target SMPS Designs

Offering an extended operating temperature range of -40° to 85°C, and isolation voltages of up to 6 kV dc, the 76253 series of Maxim-compatible, dc-dc converter transformers specifically target switch-mode power-supply applications. Available in 5- and 3.3-V versions, the devices work with Maxim's MAX253 chip set. The 5-V version supplies a maximum of 1 W, while the 3.3-V unit provides up to 500 mW. Operable at frequencies up to 500 kHz, the transformers come in a UL94-VO-rated DIP. Pricing is $1.82 each per 1000.

***Newport Components Inc.**, 88917 Glenwood Ave., Raleigh, NC 27612; Rob Hill (919) 571-9405; fax (919) 571-9262; www.newport.co.uk.* **CIRCLE 459**

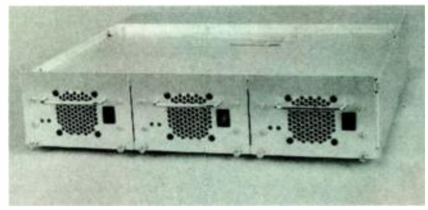
Li-Ion Rechargeable Battery Pack Uses "Smart" Technology

The ME201 Li-ion-based rechargeable battery pack complies with the Smart Battery Standard (SBS). The battery runs at 11.1 V and provides 43.3 Wh of energy. The battery uses ICR1760 cells, each measuring 17 (diameter) by 67 mm. The cells consist of a lithium-cobalt-oxide-cathode and graphite-anode material. Each cell operates at 3.7 V nominal and provides 4.8 Wh of energy. Pricing for the ME201 ranges from $90 to $100 each in large quantities.

***NEC Electronics Inc.**, 2880 Scott Blvd., P.O. Box 58062, Santa Clara, CA 95052; Sales Dept. (800) 366-9782; fax (800) 729-9288; www.nec.com.* **CIRCLE 460**

400-W Power Modules Are Hot-Pluggable

The TNQ Series dc-input, N+1 power system uses 400-W, hot-plug modules with up to four outputs and an input EMI filter. In a rackmount configuration, the system produces up to 800 W



in a 2+1 redundant configuration, or up to 1200 W non-redundant. Single-output modules have outputs from 3.3 to 48 V dc, while multi-output modules have a main output of 3.3 or 5 V dc at 60 A, or

(continued on page 144)

(continued from page 142)
24 V dc at 12.5 A. Auxiliary outputs range from 3.3 to 24 V dc and are fully isolated. Each module features an input range of 40 to 75 V dc, integral output isolation diodes, self-contained fan cooling, and high-reliability connectors. Other features include LED indicators, and control and supervisory functions. Pricing is $330 each per module. Delivery is from six to eight weeks ARO.

***Unipower Corp.**, 3900 Coral Ridge Dr., Coral Springs, FL 33065; Eugene Zuch (954) 346-2442; fax (954) 340-7901; www.unipower-corp.com.*
CIRCLE 461

Inverter Powers Two CCFTs For Large LCDs

The L Series dc-ac inverter is designed to handle two cold-cathode fluorescent tubes (CCFTs) with an efficiency range of 85 to 90%. The open-frame device measures 1 by 6.12 by 0.36 in., and comes equipped with input and output connectors. Pricing is $26.37 each per 1000; delivery is from eight weeks ARO.

***Endicott Research Group Inc.**, P.O. Box 269, Endicott, NY 13760; Jeanine Hardy (800) 215-5866; fax (607) 754-9255; e-mail: sales@ergpower.com; www.ergpower.com.* CIRCLE 462

High-Output Supplies Can Be Programmed

The XFR 150-8, 300-4, and 600-2 are 1.2-kW, high-voltage power supplies

for research, test, and industrial applications. The devices use zero-voltage switching and come with optional RS-232, GPIB, and isolated analog programming. All are rack-mountable and have a five-year warranty. Other features include remote sensing and a standby mode. Pricing is $1395 each.

***Xantrex Technology Inc.**, 8587 Baxter Pl., Burnaby, British Columbia, Canada V5A 4V7; Johnanne MacKinnon (604) 415-4600; fax (604) 421-3029; e-mail: xantrex@xantrex.com; www.xantrex.com.* CIRCLE 463

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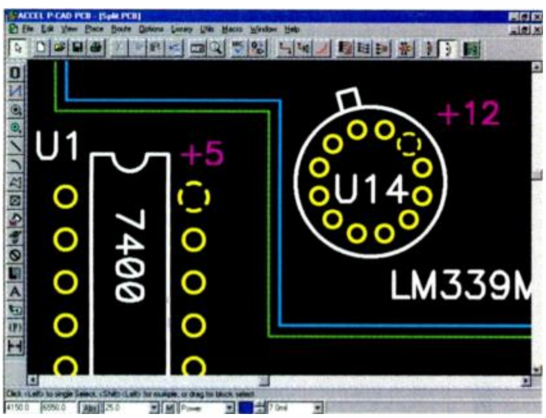

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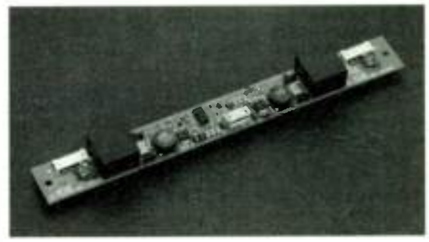
Inverter Drives From Four To Six CCFTs

The CXA-0240 Series inverters deliver up to 16 W with either four or six outputs for high-brightness LCDs.

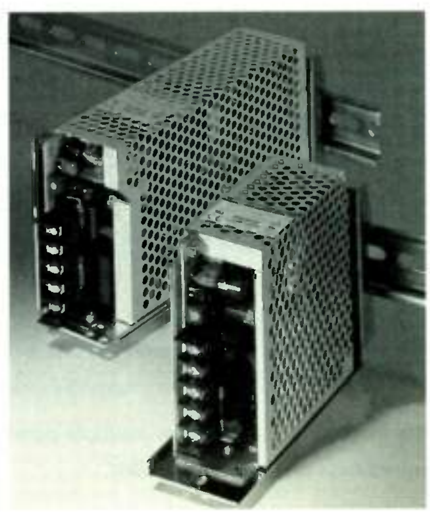


The devices feature a dual current feedback scheme, an integrated soft-start circuit, an output of 5.5 mA into each tube, and a brightness control of 0 to 100%. The devices are mounted on a 24- by 210-mm, double-sided pc board with Molex or Honda connectors. Pricing is $25 each per 1000.

TDK Corp. Of America, Power Conversion Group, 1600 Feehanville Dr., Mt. Prospect, IL 60056; Pat Carson (847) 390-4478; e-mail: power@tdktca.com; http://power.tdk.com. **CIRCLE 464**

Industrial Power Supplies Mount On DIN Rails

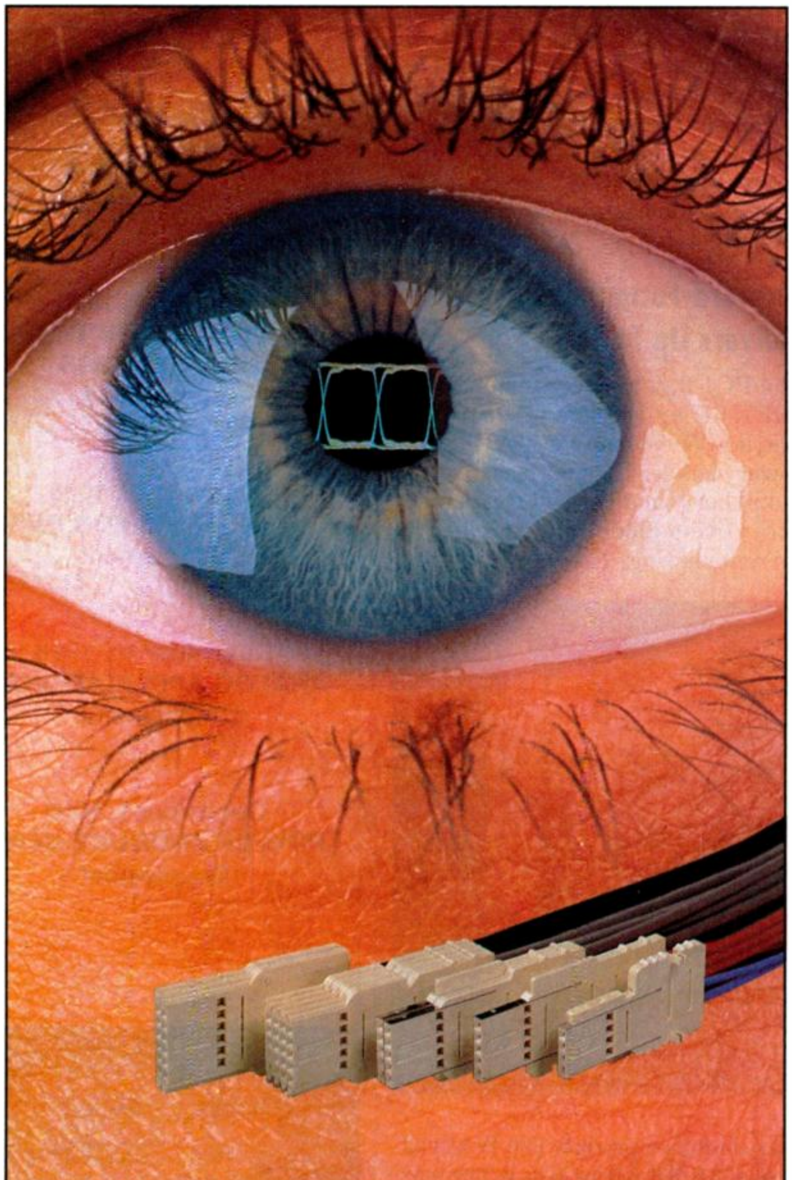
The NES/DRP, JWS/RWS, and JFS Series DIN-mount power supplies output between 15 and 2000 W. Designed

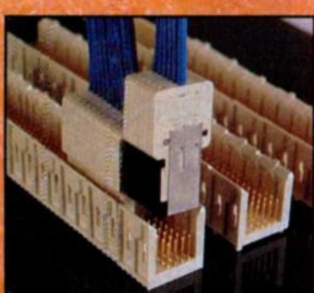


for the industrial environment, the supplies mount on either 7.5- or 15-mm rails, while the JFS Series include integral wall-mount capability. All have a universal input (85 to 265 V ac) except *(continued on page 148)*

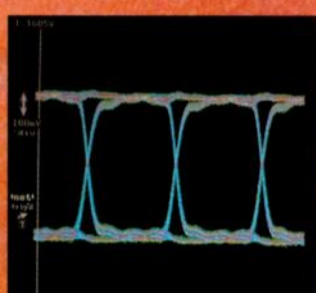
Gore's New 2MM Cables -

An Eyeful of Fidelity and Reliability





EYE-OPENER cables offer 100% compatibilty with standard 2MM backplanes



GORE 2MM assemblies provide the widest eye patterns available

1.2 Gbits/sec Intercabinet Links for 2MM Backplanes

Gore's new EYE-OPENER Family of 2MM assemblies provides unmatched performance and reliability in a package that is 100% compatible with all standard 2MM backplane connector systems.

The only source for all 2MM needs
Now Framatome's Millipacs™ 1 and 2, Metral™, Z-Pack™ HM, HDM and all the others can be optimally cabled with EYE-OPENER cable assemblies.

EYE- OPENER assemblies were designed using Eye Pattern Analysis techniques to achieve maximum synergism between cable and connector. GORE-TEX® expanded PTFE dielectric coax and twinax cables help EYE-OPENER assemblies to maintain signal integrity, even on today's fastest digital drivers and receivers. They can provide bandwidth densities greater than 2 Gbits/sec. per mm.

Designed for reliability
Premium connector materials such as Beryllium Copper contacts and Liquid Crystal Polymer housings provide abuse protection without affecting performance. A unique ruggedized version prevents plugging and unplugging damage to the small pins found in 2MM backplane connectors. EYE-OPENER cables are perfect for Telecom, Test Equipment and other high data rate applications.

Gore's EYE-OPENER family is fully scalable in size, performance and configuration and comes in differential and single ended versions. *If you want your eyes opened call:*

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READER SERVICE 162

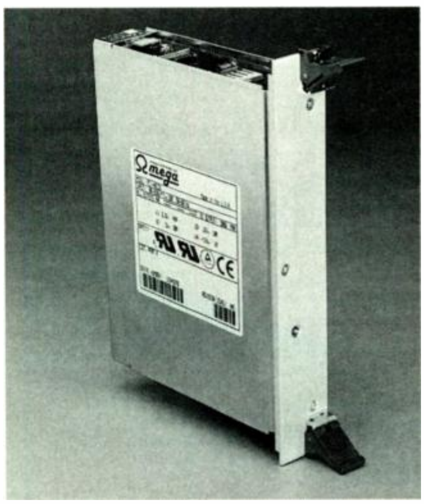
(continued from page 146)
for the DRP Series, which accepts 110/120 three-phase ac. The output voltages range from 3.3 to 48 V, and all supplies meet FCC regulations for EMI. Pricing ranges from $54 to $1400 each per 100; delivery is from stock.

***Lambda Electronics Inc.**, 515 Broad Hollow Rd., Melville, NY 11747; Ian Kolker (516) 694-4200; fax (516) 293-0519; www.lambdapower.com.*

CIRCLE 465

Eurocard-Format Supply Delivers Up To 350 W

The PCI-3, which conforms to the IEEE 6U by 160-mm pc-board format, is a 350-W, four-output (V1 to V4) power module. The unit features N+1 redundancy and hot-swap capability with ORing diodes and single-wire current sharing. The V1 and V2 outputs combined produce 200 W at voltages of 2.0, 3.3, 5.0, or 12.0 V. The maximum current rating is 45 A for the 2.0- and 3.3-V outputs. The V3 output delivers 2.0 or 24.0 V at up to 180 W, while the V4 output delivers up to 3 A at any of the specified voltages. The wide-range inputs accept from 36 to 72 V dc, or from 90 to 265 V ac (PFC to 0.99). Other features include input transient protection, 0.1% line regulation, 0.5% load regulation, remote sensing, and an efficiency of 75%. UL, CSA, and European approvals are included. Pricing is $525 each, and delivery is from one to four weeks.



***Omega Power Systems**, 8966 Mason Ave., Chatsworth, CA; Sales Dept.*
(continued on page 150)

(continued from page 148)
(818) 727-2216; fax (818) 727-2276; e-mail: sales@omegapower.com; www.omegapower.com. **CIRCLE 466**

1500-W AC-DC Converters Come In A Miniature Package

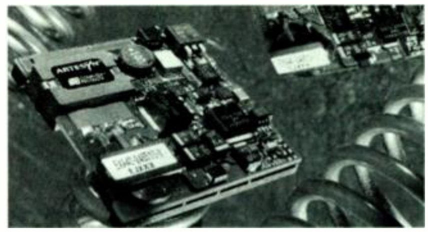
The UFM Series of ac-dc converters convert ac-line voltages to 300 V dc. Measuring 1.45 by 2.28 by 0.5 in., the series is available in two models—the UFM500 and UFM1K—that produce between 500 and 750 W and 1000 to 1500 W, respectively. Both lines are complete front-end solutions, requiring only a filter, an input fuse, transient protection,

and appropriate holdup capacitors. Internal inrush current limiting is provided, and the efficiency is rated at 97%. The units can operate at up to 100°C and come with approvals that include UL, VDE, and CE marking. Pricing for the UFM500 is $44 each per 100, while the UFM1K costs $66 each per 100.

***Powercube**, 9340 Owensmouth Ave., Chatsworth, CA 91311; Customer Service (800) 866-3590; fax (800) 866-3589; e-mail: shrram@prodigy.net.*
CIRCLE 467

Low-Cost, Miniature Converter Outputs Up To 40 W

Available in seven models, the EXA40 Series dc-dc converter produces up to 40 W and comes in an open-frame package measuring 2.2 by 2.2 in. The converter has an output voltage of 1.8 to 5 V, with efficiencies ranging from 84% to 91%, respectively. The line regulation is 0.05% and the load regulation is 0.20%; input-voltage ranges are 18 to 36 V and 36 to 75 V. Features also include an operating temperature range of –40° to 70°C (convection cooling), or up to 100°C (forced-air cooling). The series comes with ETS300-386-1, EN60950, UL1950, and CSA C22.2 No. 234/950 approvals. Pricing is $98 each per 100.



***Artesyn Technologies**, 7575 Market Place Dr., Eden Prairie, MN 55344; Mike Szpyt (508) 424-2871; fax (612) 829-1837; e-mail: mike.szpyt@artesyn .com; www.artesyn.com.* **CIRCLE 468**

Linear-Regulated Modules Handle 25 W At 1.5 To 56 V dc

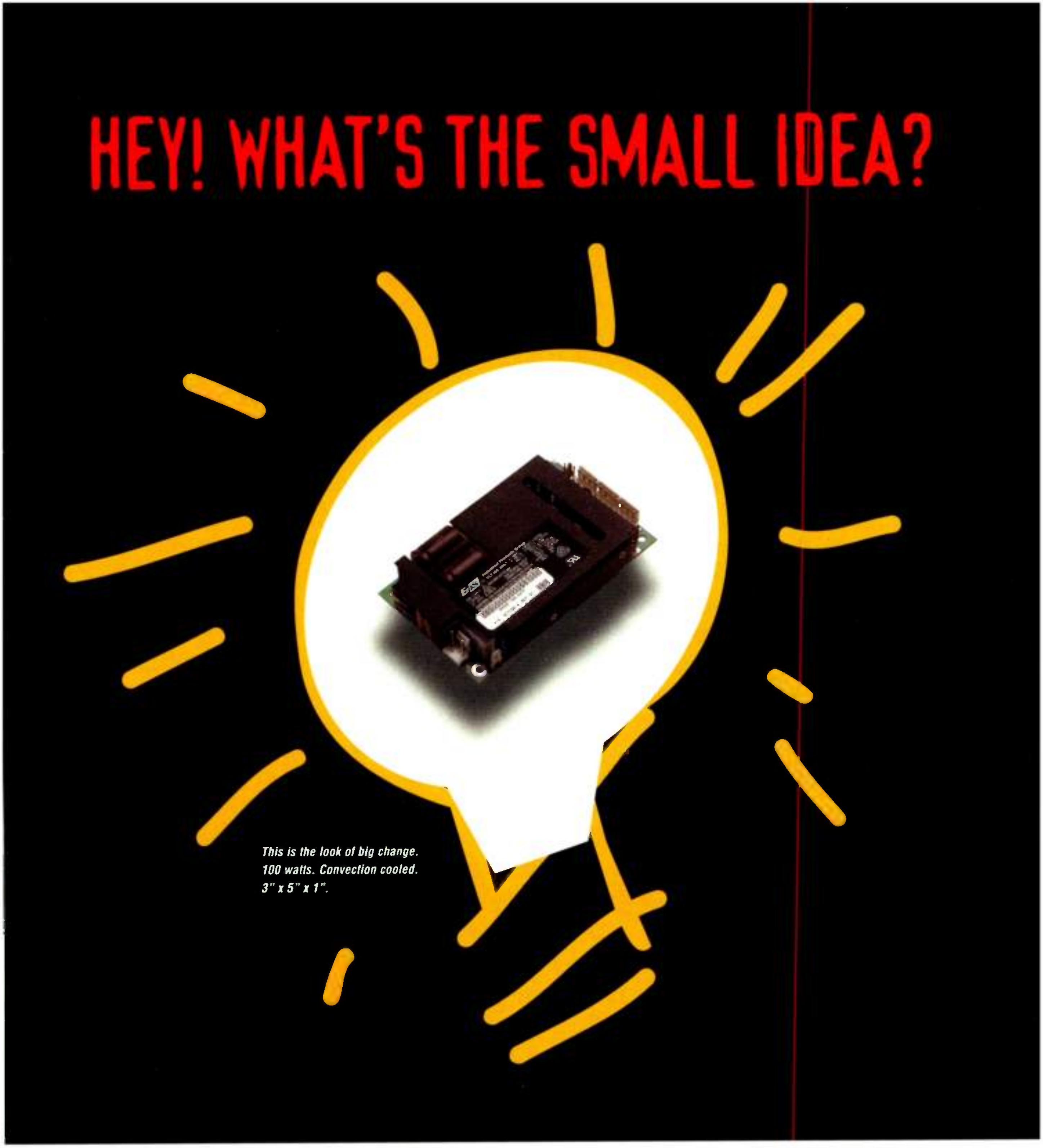
The Cardflex CF800 Series line of 25-W ac-dc encapsulated linear-regulated modules cover the voltage range of 1.5 to 56 V. The input range is 115 to 230 V ac and the output current ranges from 440 mA up to 7 A. Measuring 4.5 by 3.5 by 2 in., the modules have a line regulation of 0.02% and a load regulation of 0.2 or 0.3%—depending on the output voltage. The modules operate over the temperature range of –25° to 100°C, feature an output ripple of 1.0 to 2.0 mV (rms), and have UL and CSA approvals pending. Pricing is $98 each; delivery is from stock.

***Hyperlab Corp.**, 330 Millway Ave., Concord, Ontario, Canada L4K 3W2; Andrew Calkin (905) 761-0055; fax (905) 761-6203.* **CIRCLE 469**

Point-Of-Load Power Module Targets High-End Servers

Occupying one-third the space of conventional VRMs, the Titania-series power module featuring an MTBF of five million hours targets high-reliability servers and workstations. The module uses a low-cost, 50-pin connector to eliminate the need for special handling. The module will be available with inputs of 3.3 to 48 V dc, while the outputs are programmable from 1.3 to 3.5 V dc. The output current ranges from 16 to 20 A. The module also meets VRM 8.3 output transient specifications without external output capacitors. Pricing is $25.10 each per 10,000.

***Lucent Technologies**, 3000 Skyline Dr., Dept. PR2001, Mesquite, TX 75149; Customer Response (800) 526-7819; www.lucent.com/networks/power.*
CIRCLE 470



It's a bright idea! At Eos we're onto something big in a tiny package. Our new VLT line of 60-watt and 100-watt power systems pack up to 7.5 watts per cubic inch, with footprints up to four times smaller than the competition. Eos power supplies are so small they're setting a new industry standard. This means a competitive advantage for you.

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READER SERVICE 152

Circle 520

"Virtual Switched-Capacitor" LCD Bias Control

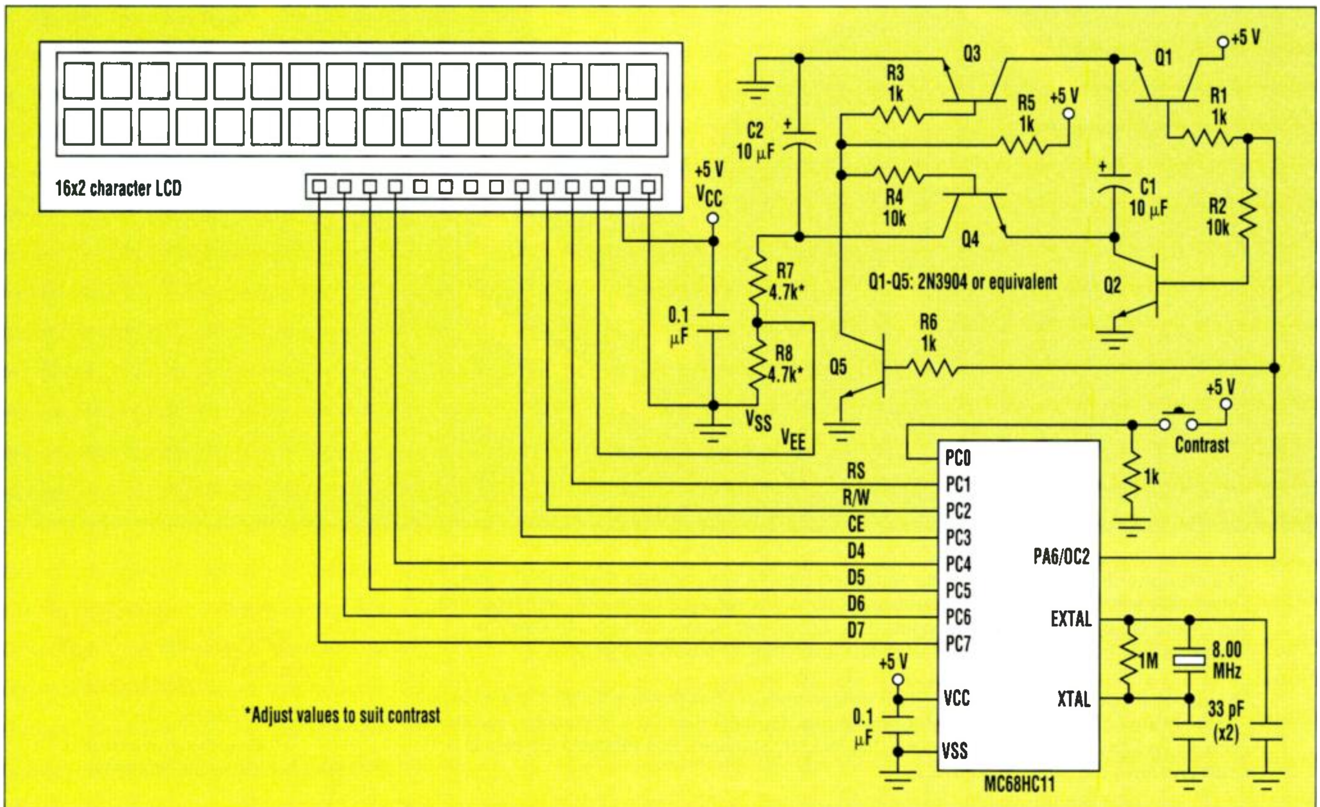
ALEC R. BATH
Motorola Inc., Automotive and Industrial Electronics Group,
4000 Commercial Ave., Northbrook, IL 60062; (847) 480-5171;
fax: (847) 205-2503; e-mail: g13093@email.mot.com.

In a low-cost microcontroller-based design, it's possible to generate the negative voltage supply required to bias extended-temperature character LCD modules without a dedicated voltage inverter IC. Using five inexpensive general-purpose npn switching transistors (2N3904 or equivalent), two storage capacitors, a handful of resistors, and a periodic square wave generated by the microcontroller, an elementary switched-capacitor or "flying-capacitor" negative voltage supply can be realized.

The figure details an HC11's "timer output compare" that generates a 1-kHz square wave. When OC2 goes high, Q1 and Q2 are switched on, charging C1. Q5 also turns on, turning off Q3 and Q4. When OC2 goes low, Q1, Q2, and Q5 are shut off. Q3 and Q4 then are turned on via pullup resistor R5, which transfers C1's charge to C2, and inverts its voltage with respect to ground. The cycle is repeated, thus forming a charge pump. A 1-kHz, 50% duty cycle produces a peak negative voltage output of about –3.8 V, with a 4-mA load.

By increasing or decreasing the duty cycle of OC2, the output voltage, and thereby the contrast, may be varied. This would eliminate a digital or resistive potentiometer. A switch attached to port PC0 is used to increase or decrease this contrast. Also, by using the LCD module in 4-bit mode, only 8 control lines plus the "timer output compare" output are needed for full LCD control. Adjusting the values of R7 and R8 may be necessary to optimize the contrast range for a particular display type and viewing angle.

The software listing details assembly code for a Motorola HC11 8-bit microcontroller. It consists of three subroutines and an interrupt service routine. SWCAP_ON enables the OC2 squarewave output, at a 1-kHz rate and a 50% duty cycle. SWCAP_OFF disables OC2. SWCAP_INT is the interrupt service routine. For a 50% duty cycle, the routine is called every 500 microseconds, and takes 47 cycles. SWCAP_SWITCH increments the duty cycle of TCMP in 5% increments. The routine limits the duty cycle between 20% and 80%. When the switch is pressed while at an 80% duty cycle, it jumps to a 20% duty cycle. At a 20% or 80% duty cycle, SWCAP_INT generates a minimum interrupt period of 200 µs (200 µs ON / 800 µs OFF or vice versa).



An elementary switched-capacitor, or "flying-capacitor," negative voltage supply can be achieved using a minimal amount of low-cost parts. Here, an HC11's "timer output compare" will generate a 1-kHz squarewave.

LINEAR TECHNOLOGY DESIGN NOTES

Inexpensive Circuit Charges Lithium-Ion Cells – Design Note 188

David Bell

Introduction

A single Lithium-Ion cell is often the battery of choice for portable equipment because of its high energy density. The 3V to 4.1V provided by a Lithium-Ion cell is also a good match for modern low voltage circuits, often simplifying the power supply. Despite these advantages, designers are often frustrated when attempting to design precision charging circuitry that meets battery manufacturers' specifications. Figure 2 is a simple, cost-effective linear charger that satisfies these precision Lithium-Ion charging requirements.

Lithium-Ion cell manufacturers generally recommend a constant-current/constant-voltage (CC/CV) charging technique. Although conceptually simple, charging a Lithium-Ion cell requires very accurate control of the float voltage to obtain high capacity with long cycle life. If the voltage is too low, the cell will not be fully charged; if the voltage is too high, the cycle life is significantly degraded. Excessive voltage to the cell can also result in venting and other hazardous conditions (specific hazards depend upon the cell's construction and chemistry).

Figure 1 depicts CC/CV charging characteristics for a typical Lithium-Ion cell. A fully discharged cell will initially be charged by a constant current, since the cell's voltage is below the 4.1V constant-voltage limit. (Most Lithium-Ion cells require either a 4.1V or 4.2V float voltage, depending on the cell's chemistry.) Once the cell's voltage rises to the float voltage of 4.1V, the charger limits further rise in terminal voltage and the charging current naturally begins to fall off. Most battery manufacturers recommend that charging be terminated roughly one hour after the current has fallen to 10% of its peak value. Alternatively, a timer can be started when charging begins, with time-out used to suspend charging once sufficient time has elapsed to charge a fully depleted cell.

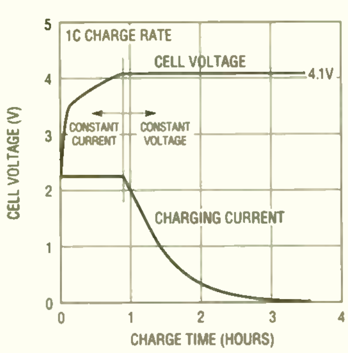


Figure 1. Typical Lithium-Ion Charge Characteristics

Circuit Description

Figure 2 depicts a simple and inexpensive linear charger that can be used to charge a single Lithium-Ion cell. The circuit provides constant-current/constant-voltage (CC/CV) charging from an inexpensive, unregulated 6V wall adapter. The charger is built around a single LTC®1541, which contains a voltage reference, op amp and comparator. The high accuracy voltage reference (±0.4%) regulates the battery float voltage to ±1.2%, as required by most Lithium-Ion battery manufacturers. Even tighter accuracy can be obtained by specifying higher accuracy for feedback divider resistors R6 and R7. The charger may be configured to float at either 4.1V or 4.2V by changing the value of R6. Use 252k for a 4.1V float voltage; use 261k for a 4.2V float voltage.

Transistor Q1 is used to regulate battery charging current. Q1's base current is controlled by the op amp output (Pin 1) and buffered by transistor Q2 for additional current gain. Diode D1 is needed to prevent reverse current flow when the wall adapter is unplugged or unpowered. Because this is a linear regulator, the designer must consider power dissipation in Q1. As shown with a 6V wall adapter, Q1 dissipates a maximum of about 1W and can be heat sinked directly to the printed circuit board. Higher current levels or higher input voltages will increase dissipation and additional heat sinking will be needed.

Battery charging current is sensed by R11 and fed to the op amp's noninverting input via R10. IC1's internal 1.2V reference voltage is divided to 44mV by R4 and R2 and connects to the op amp's inverting input. The op amp compares the current sense voltage against the 44mV reference and adjusts the base drive to Q1 as needed to regulate current to 300mA. The op amp's ±1.25mV

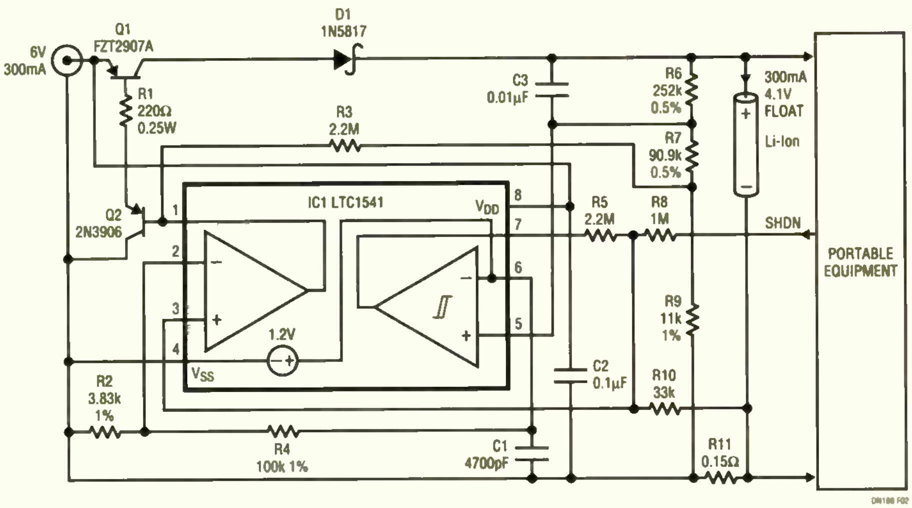


Figure 2. Lithium-Ion Battery Charger

maximum input offset voltage guarantees accurate charge current regulation while dropping only 44mV across the sense resistor.

Once the battery charges to 4.1V, the voltage loop begins to reduce charging current to maintain the desired float voltage. A resistor divider comprising R6, R7 and R9 generates a feedback voltage to IC1's comparator (Pin 5). Once the voltage at this node reaches 1.2V, the comparator output goes high, pulling the current sense signal high via R5. During voltage regulation, the comparator output (Pin 7) is a pulsed waveform; however, the low slew rate of the micropower op amp smoothes this signal to a small amplitude triangle wave at Pin 1. In fact, the voltage at Pin 7 may be monitored by a microprocessor to detect the onset of constant-voltage regulation.

Current sense resistor R11 is in series with the battery charging path and would normally result in voltage regulation beginning at around 4.05V instead of the desired 4.1V (44mV is dropped across the sense resistor). However, the addition of R3 and R9 compensates for this voltage drop, and results in activation of the constant-voltage loop at 4.1V. In essence, R3 and R9 create a negative output impedance from the regulator that cancels the 0.15Ω resistance of R11. By carefully selecting the values of R3, R7 and R9, one can produce an even larger negative output resistance and compensate for the internal resistance of the battery and its internal protection circuitry. The result is faster recharge times without exceeding the 4.1V limit within the cell itself.

Because the current sense loop actually monitors the total current drawn from the wall adapter, the charger will automatically "load share" with the portable equipment. In other words, when the equipment draws no power, all of the 300mA is available to charge the battery. However, any current drawn by the equipment will simply subtract from the battery charging current, keeping the wall adapter load limited to 300mA. The charger may also be shut down by logic control, as shown in Figure 2. Pulling high on the shutdown signal forces the current feedback signal above the 44mV threshold, thereby turning off Q1. The charger operates normally when the shutdown pin is a high impedance state—the default state on most microprocessor port pins. R8 may be eliminated if the shutdown feature is not needed.

Other Charging Options

The simple linear charger described above is suitable for many handheld portable products, where total charging current is modest. For higher current or multicell applications, a high efficiency switching regulator charger, such as the LT®1510 or LT1511, may be appropriate. The LT1510 is a CC/CV charger capable of delivering up to 1.25A of charging current from an SO-8 package. The LT1511 can deliver up to 3A and includes an input current limiting feature.

The CC/CV charging technique is not limited to Lithium-Ion batteries; sealed lead-acid (SLA) batteries may also be charged using similar circuitry. The constant-voltage control loop can easily be converted to a "hysteretic charger" for optimal SLA charging. Contact Linear Technology Applications Engineering for additional details.

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```
****************************************************************
*       Switched Capacitor LCD Driver Routines
*       Alec Bath  HC11 Version
****************************************************************
*       8.00 MHz/4/8 = 250kHz, 4uS = Timer Count Rate
*       For 1 Khz, 250 kHz/ 1 khz = 250 cts,
*        125 cts / half wave, ~12 cts / 5% duty cycle
*
*       Counts(Hi/Lo)          Hex (Hi/Lo)         % Duty Cycle
*       ------------   ------------   ------------
*       197 / 53               $00C5 / $0035       80
*       185 / 65               $00B9 / $0041       75
*       173 / 77               $00AD / $004D       70
*       161 / 89               $00A1 / $0059       65
*       149 / 101              $0095 / $0065       60
*       137 / 113              $0089 / $0071       55
*       125 / 125              $007D / $007D       50
*       113 / 137              $0071 / $0089       45
*       101 / 149              $0065 / $0095       40
*       89 / 161               $0059 / $00A1       35
*       77 / 173               $004D / $00AD       30
*       65 / 185               $0041 / $00B9       25
*       53 / 197               $0035 / $00C5       20

************* Register Equates ******************
* Register Equates offset from $1000 (X-register)

PORTA  equ      $00     ; Port A
TOC2   equ      $18     ; Output Compare Register 2, Low Byte
TCTL1  equ      $20     ; Timer Control Register 1
TMSK1  equ      $22     ; Timer Mask Register 1
TFLG1  equ      $23     ; Timer Flag Register 1
TMSK2  equ      $24     ; Timer Mask Register 2

**************** RAM Equates ******************
RAM_START      org      $0000     ; Start of RAM
DUMMY1         rmb      1         ; Dummy MSB Byte
SWCAP_HI       rmb      1         ; Hi Freq PWM RAM location
DUMMY2         rmb      1         ; Dummy MSB Byte
SWCAP_LO       rmb      1         ; Lo Freq PWM RAM location

**************** Subroutines ********************
*       Descriptions:
*
*       SWCAP_ON:          Enable Voltage Inverter, 50% duty
*       SWCAP_OFF:         Disable Voltage Inverter
*       SWCAP_INT:         Interrupt Rtn for Timer Output Compare
*                                      47 cycles max
*       SWCAP_SWITCH:      Contrast Switch subroutine, Up/Down
*
*                          79 bytes total ROM space, 4 bytes RAM

org     $f800                     ; start of code
```

```
SWCAP_ON                                  ; enable output
        ldaa    #!125                     ; 1 kHz freq, 50% duty cycle
        staa    SWCAP_HI                  ; store high-side pulse byte
        staa    SWCAP_LO                  ; store low-side pulse byte
        bset    TMSK2,X,$02               ; divide by 8 prescaler
        ldaa    #%01000000                ;
        staa    TCTL1,X                   ; toggle OC2 on successful
                                          ; compare
        staa    TMSK1,X                   ; enable OC2 interrupt
        staa    TFLG1,X                   ; clear flag
        cli                               ; enable interrupts
        rts                               ; exit subroutine

SWCAP_OFF                                 ; disable output
        bclr    TCTL1,X,$40               ; disable OC2 output
        bclr    TMSK1,X,$40               ; disable OC2 interrupt
        rts                               ; exit subroutine

SWCAP_INT                                 ; update OC2 settings
        ldx     #$1000                    ; register offset
        brclr   PORTA,X,$40,SWCAP_INT_HI          ; H/L level?
SWCAP_INT_LO                              ; update for low-side pulse
        ldd     TOC2,X                    ; load OC2
        addd    SWCAP_LO-1                ; add low-side pulse value
        std     TOC2,X                    ; update
        bra     SWCAP_INT_DONE            ; exit
SWCAP_INT_HI                              ; update for high-side pulse
        ldd     TOC2,X                    ; load OC2
        addd    SWCAP_HI-1                ; add high-side pulse value
        std     TOC2,X                    ; update
SWCAP_INT_DONE                            ; exit
        bclr    TFLG1,X,$BF               ; clear OC2F
        rti                               ; return from interrupt

SWCAP_SWITCH                              ; increment OC2 duty cycle 5%
        ldaa    SWCAP_HI                  ; load high-side pulse value
        cmpa    #!197                     ; 80% ?
        beq     SWCAP_SW_OVER             ; rollover if max'ed out
        ldaa    SWCAP_HI                  ; load high-side pulse value
        adda    #!12                      ; 12 counts / 5% duty cycle change
        staa    SWCAP_HI                  ; update high-side pulse value
        ldaa    SWCAP_LO                  ; load low-side pulse value
        suba    #!12                      ; 12 counts / 5% duty cycle change
        staa    SWCAP_LO                  ; update low-side pulse value
        rts                               ; exit subroutine

SWCAP_SW_OVER                             ; rollover (20% duty cycle)
        ldaa    #!53                      ; high-side pulse value = 53 counts
        staa    SWCAP_HI                  ; update
        ldaa    #!197                     ; low-side pulse value = 197 counts
        staa    SWCAP_LO; update
SWCAP_SW_DONE                             ; finished
        rts                               ; exit subroutine
```

Circle 521

Phase-Locked Digital Synthesizer

SAMUEL KEREM
Patton Electronics, 7622 Rickenbacker Dr.,
Gaithersburg, MD 20879; (301) 975-1000; e-mail: samuelkerem@juno.com.

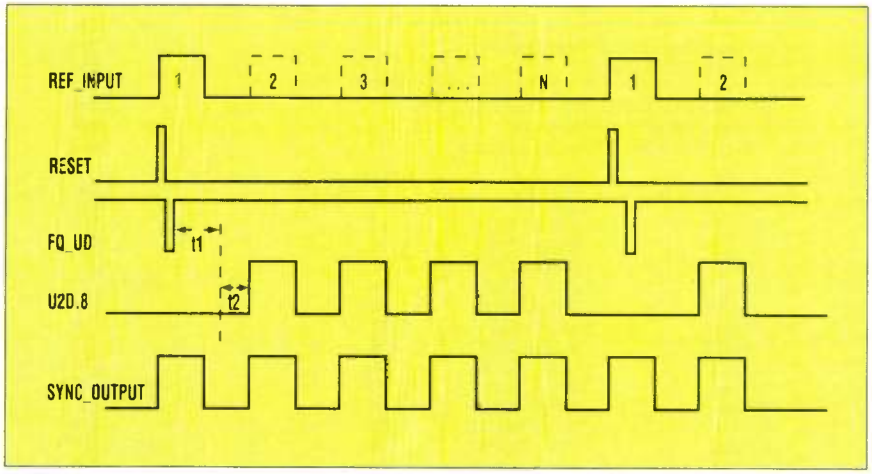
The circuitry shown in Figure 1 demonstrates the technical features from both phase-locked-loop (PLL) and direct-digital-synthesis (DDS) designs. The design represents a phase-locked oscillator with practically zero lock-in and recovery time, and jitter less than 4 ns. The device is significantly more tolerant to the absence of synchronous pulses, and it stays in phase much longer than PLL-based devices. There's no loop in the design, and the absence of a feedback makes the design quite simple.

Designs requiring this performance include applications such as clock recovery and synchronous frequency multiplication. This circuit also can also be used whenever any two frequencies need to be synchronized at a particular moment in time.

The maximum input (reference) frequency range is 5 MHz and can be doubled, tripled, and so on with a simple modification. The output frequency can reach 50 MHz. There's one condition, though—the frequency of the input (reference) signal should be known in advance. This situation is common in telecommunications, when synchronization of two remotely located clocks (transmitter and receiver) is required, and a number of sync-pulses are absent in the transmitted signal. Such is the case in Figure 2, in which the reference pulses following reference pulse #1 are absent.

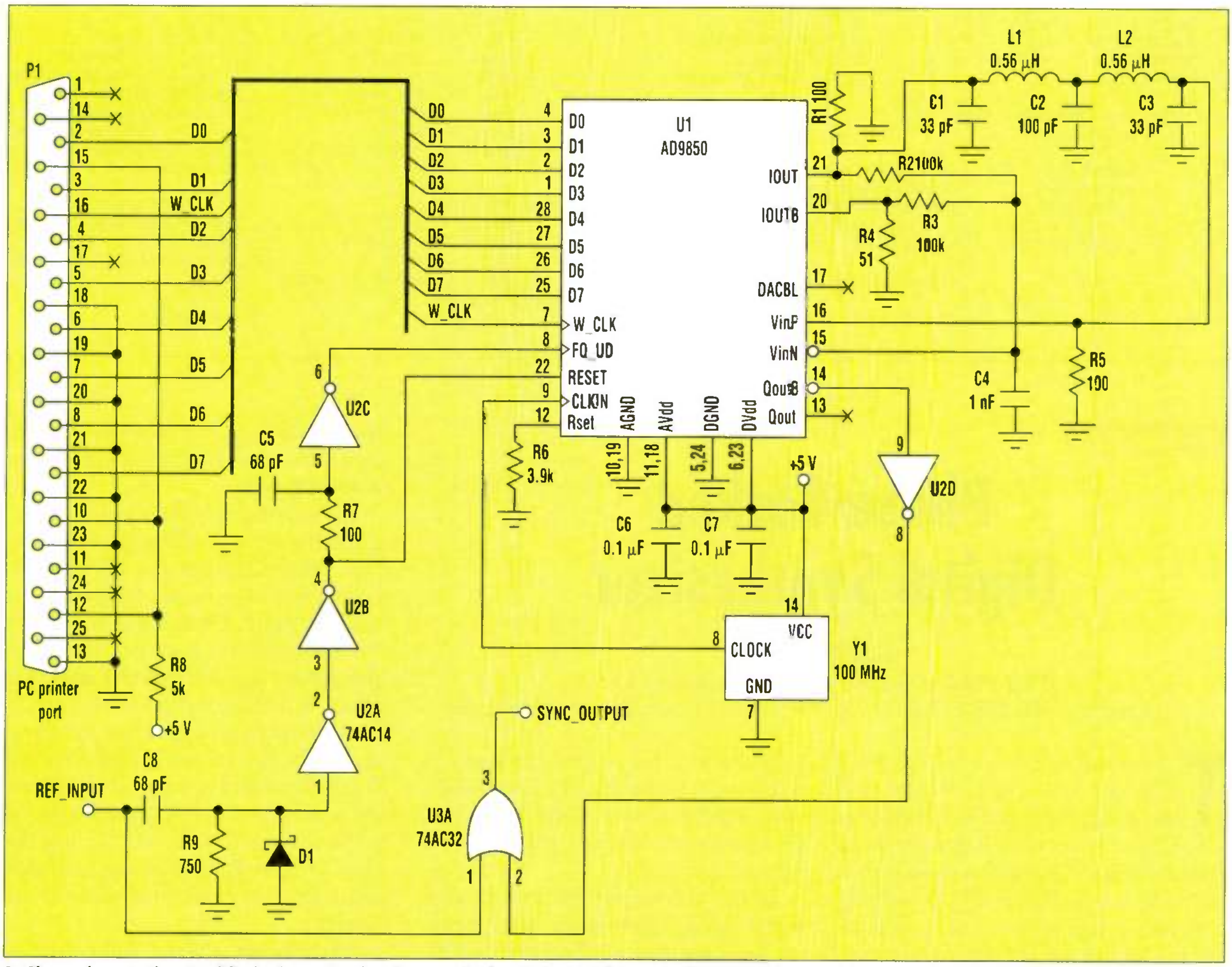
At the heart of the circuit is Analog Device's AD9850 DDS chip. The chip produces a digitally synthesized sinewave using a frequency value programmed from a master device (in our case, the PC printer port). The frequency value is latched through the data bus into the U1 input registers by W_CLK, coming from PC.

To produce the output frequency (U1.21), the chip must be clocked by the FQ_UD signal, usually supplied by the same master device. In our case, the FQ_UD comes from the reference signal. The reset signal, formed from the same reference signal (C8, R9, U2A, U2B), will bring all of the AD9850's internal registers into the predefined state, but will not affect the data stored. After a short delay following the reset pulse (R7, C5, U2C), the FQ_UD signal will be created and a digitized sine wave is produced at the output (U1.21). The sine wave is applied through a low-pass filter (C1, C2, C3, L1, L2) to the internal comparator input, resulting in a squarewave output (U1.14) with the programmed frequency.



2. Missing reference pulses are recovered and resynchronized with the reception of each detected reference pulse.

The time interval t1 *(Fig. 2, again)*, between the rising edge of the reference signal and the moment when updated data appears at the U1 output is predetermined and remains constant. For different frequencies, the initial phase shift t2 is program-controlled (0xd0 in our case) and will place pulse #2



1. Shown here is the simplified schematic of a phase-locked oscillator with practically zero lock-in and recovery time. Jitter is less than 4 ns.

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```
/* Phase Locked Synthesizer.  Samuel Kerem
This program sends data to the AD9850.
Frequency = 1.544000 MHz +/- lHz
Phase = 146.25° */

#include <dos.h>

const PRN_DATA = 0x378;
const PRN_CNTR = 0x37A;
const W_CLK_1 = 0x04;
const W_CLK_0 = 0x00;

main()
{
     // 2^32(9850 resolution)/100*10^6(Yl clock)
     const float CLOCK=42.9497;
    // frequency and phase values
    unsigned long fr = 1544000;
    int ph = 0xd0;
    void syn(unsigned long fr, int ph);
    fr *=CLOCK;
    syn(fr, ph);
    return(0);
}

void syn( unsigned long freq, int phase )
{
    int byte_1, byte_2, byte_3, byte_4;

byte_l = freq/0xffffff;
    byte_2 = (freq%0xffffff)/0xffff;
    byte_3 = (freq%0xffff)/0xff;
    byte_4 = (freq%0xff);

   //control word + phase value
   outp(PRN_CNTR, W_CLK_0);
   outp(PRN_DATA, phase);
   outp(PRN_CNTR, W_CLK_1);
   outp(PRN_CNTR, W_CLK_0);
   // first byte loading
   outp(PRN_DATA, byte_1);
   outp(PRN_CNTR, W_CLK_1);
   outp(PRN_CNTR, W_CLK_0);
   // second byte
   outp(PRN_DATA, byte_2);
   outp(PRN_CNTR, W_CLK_1);
   outp(PRN_CNTR, W_CLK_0);
   // third byte
   outp(PRN_DATA, byte_3);
   outp(PRN_CNTR, W_CLK_1);
   outp(PRN_CNTR, W_CLK_0);
   // fourth byte
   outp(PRN_DATA, byte_4);
   outp(PRN_CNTR, W_CLK_1);
   outp(PRN_CNTR, W_CLK_0);
}
```

from U1 after the period equal to the reference signal period.

U3 will logically add reference pulse #1 and the following DDS pulses. Therefore, the first pulse and every subsequent reference pulse will synchronize the pulse sequence coming from DDS. These pulses are quartz-generated and their frequency variation will be significantly less than the VCO. The squarewave signal is produced from the spectrally pure DDS sinewave, with negligible phase noise. There is no feedback signal, which usually oscillates, even when the PLL is in the lock-in state. This also degrades the phase noise performance.

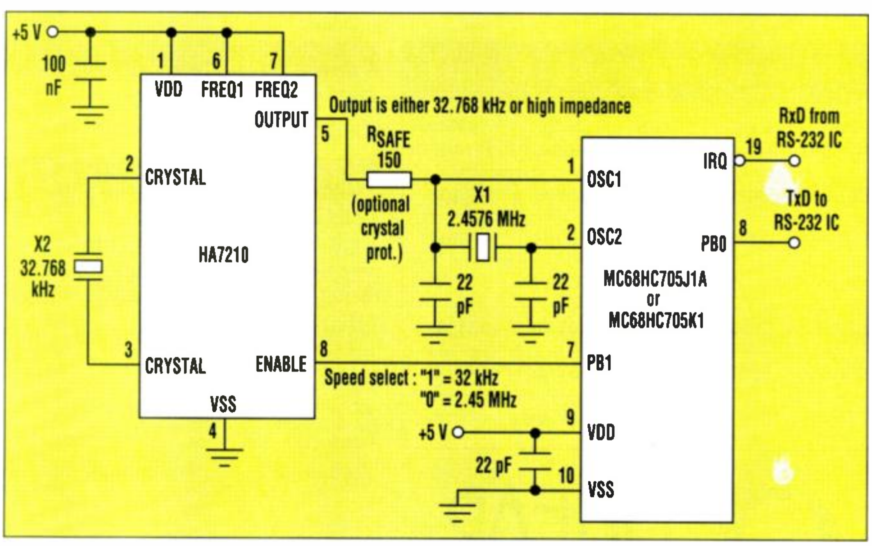
The supplied source code sample *(see the listing)* is for a 1.544-MHz frequency case.

Circle 522

Microcontroller Controls Its Own Clock Speed

THORSTEIN BLOMSTRAND
EISCAT Scientific Association, Ramfjordmoen, N-9020 Tromsdalen, Norway; phone: +47 776 92166; e-mail: Thorstein.Blomstrand@eiscat.uit.no.

When working with low-end microcontrollers like the Motorola MC68HC705J1A or the earlier 'K1, some features available on larger chips, like selectable "full speed" and "standby" clock oscillators, are sorely missed. This circuit idea arose from a need to run a 'K1 microcontroller at a slow clock to conserve battery power, while still enabling the MCU to "wake itself" at a much higher speed to perform RS-232 serial communications.



This circuit is able to slow the microcontroller's speed to conserve battery power, yet can "wake itself" at a higher speed to perform RS-232 serial communications.

The basis for the switchable clock oscillator is the Harris HA7210, a chip that's very easy to use and requires few extra components, such as the crystal itself and some decoupling capacitors. The output can be disabled (i.e. set to a high-impedance state), where it also has very little additional capacitance. The HA721 supply current is only 5 µA operating at 32.768 kHz, and it runs on a 2- to 7-V supply.

In this application, the MC68HC705J1A is used with bit 1 of port B set for speed control. The "high-speed" crystal (2.4576 MHz) generates serial communication (RS-232) baud rates. When the HA7120 oscillator is disabled, it's essentially disconnected from the ordinary oscillator circuit of the MCU. This allows the MCU oscillator to function as normal, generating a "high-speed" clock of 2.4576 MHz. About 5 pF is added to the OSC1 pin by the HA7210, but this has no noticeable effect on frequency. An optional protection resistor is shown as a precaution against voltage overdrive for X1 *(see the figure)*.

When the MCU's program needs to, it can slow down the clock with a simple "BSET 1 PRTB1" command. This enables the HA7210 output, overriding the crystal of the ordinary MCU oscillator. The OSC1 pin now follows the logic-level squarewave output of 32.768 kHz. The microcontroller now runs at a slow clock speed using very little current.

Circle 523

Single-Transistor Constant-Current Generator

MARK HUGHES
17 Canterbury Dr., Ashby De La Zouch, Leicestershire LE65 2QQ, United Kingdom.

Perhaps this circuit is stating the obvious, but sometimes the obvious can elude us! Though not as good as many other constant current generators, it's very simple and very inexpensive. The figure shows the basic idea. The circuit, which would usually be considered as an emitter-follower output stage, is ideally suited to bias current generators with a small compliance. It also could be used in other applications where its poor accuracy and temperature dependence aren't a problem.

R_B is chosen to provide the required output current, I_G, and is calculated as follows:

$$I_G \cong \frac{V_{BE}}{R_B} \cong \frac{0.65 + 0.1\ V}{R_B}$$

This ignores base currents, etc.

R_E is chosen so that at the maximum compliance voltage, the transistor current $I_T > 0$. Stated in another way, the current I_E is greater than I_C, and therefore the transistor is always conducting.

$$\frac{V_A - V_{BE} - V_{G(MAX)}}{R_E} > \frac{V_{BE}}{R_B}$$

where V_G is the generator's output voltage.

The variation in transistor current, I_T, will directly affect the circuit's performance. For example, a 10:1 variation in transistor current will cause about 10% variation in I_G, and a 2:1 variation in transistor current will cause about 2.5% variation in I_G. Assuming a constant V_A.

with $K = V_{BE}\left(1 + \frac{R_B}{R_E}\right)$,

transistor current ratio L =

$$\frac{V_{A(MIN)} - V_{G(MAX)} - K}{V_{A(MAX)} - V_{G(MIN)} - K}$$

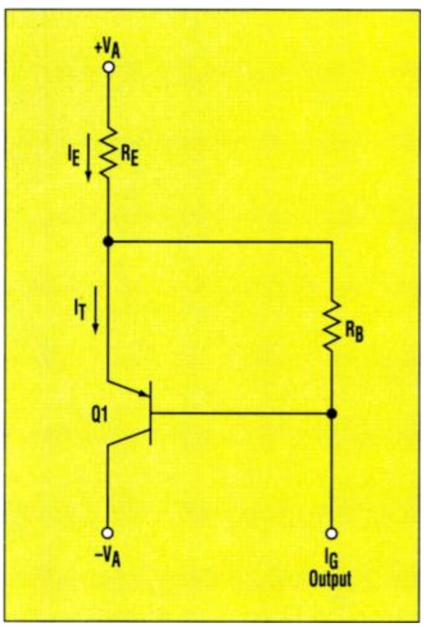
Current generator variation M ≅

$$\frac{|25\ mV\ \ln(L)|}{0.65\ mV}$$

Equivalent resistance R_G ≅

$$\frac{(V_{G(MAX)} - V_{G(MIN)})R_B}{|25\ mV\ \ln(L)|}$$

For example with a supply of V_A = 15 V driving a circuit of compliance 1 V to 3 V, putting $R_B = 680\ \Omega$ and $R_E = 6.8k$ gives an output of about 1 mA, a transistor current ratio L of 0.7, a current generator variation M of about 1% and an equivalent resistance R_G, of about 150k. Keep in mind that the circuit has –0.3% per °C temperature dependence.



This inexpensive constant-current source is as simple as it is useful.

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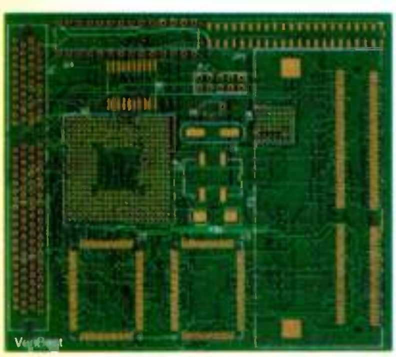
Placement (20)	14	15	18	16	15	14	10	13	0	0
Libraries (14)	11	13	11	13	13	13	9	8	0	0
Miscellaneous (27)	22	25	15	23	19	20	17	14	0	0
Quality in Manufacturing Output Data* (40)	33	17	25	15	14	24	21	17	0	0
GRAND TOTALS	137	123	122	116	114	111	109	101	0	0

* The Quality in Manufacturing Output Data consisted of 10 categories with grades of excellent, very good, good, poor and bad.
For numerical interpretation, we assigned the following values: Excellent = 4 pts., Very Good = 3 pts., Good = 2 pts., Poor = 1 pt., Bad = 0 pts.
VeriBest received 6 excellent, 1 very good and 3 good marks in the 10 categories.



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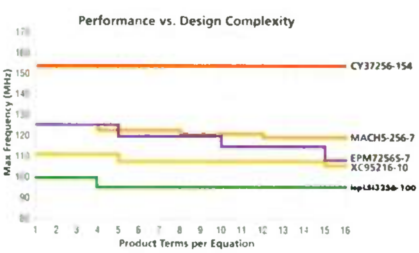

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CY37128	128	6.5	167	133	TQFP, PLCC
CY37192	192	7.5	154	125	TQFP, PLCC
CY37256	256	7.5	154	197	TQFP, PQFP BGA
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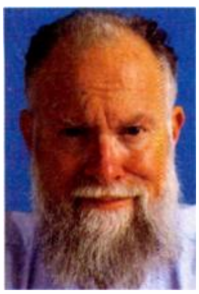
BOB PEASE

What's All This "Driving Into Accidents" Stuff, Anyhow?

A while back, I decided what I would write about for my next book. It took a year longer than I expected, but it's here: *How to Drive Into ACCIDENTS—And How NOT To*. It's 488 action-packed pages. (OK, one page is blank.)

What is the book about? I want beginning drivers to learn thoughtful, advanced techniques for making decisions, driving defensively, and avoiding accidents. So, I wrote about all the ways that funny little habits or quirks become bad habits, and how these can work together with other factors—*conspiring* to cause accidents.

For example, most people have figured out that the phrase "Speed Kills" is baloney. Yet, driving fast CAN compound with other factors to get you in trouble, cause accidents, and get you killed, or, even worse, get you badly injured.... Whereas bad visibility is much more perilous than merely speeding.



BOB PEASE OBTAINED A BSEE FROM MIT IN 1961 AND IS STAFF SCIENTIST AT NATIONAL SEMICONDUCTOR CORP., SANTA CLARA, CALIF.

Why am I qualified to write this book? I have driven over 1,000,000 mi. I have seen other people's accidents, and discussed them. I think that I know enough about cars. And I think I understand the physics, the mechanics—and human nature.

Why did I think I could write this book? Hey, I have already written one book, so I knew I could write another. Word by word, paragraph by paragraph, topic by topic, file by file—I knew I could do it.

Process those words. CRUNCH those topics. I was confident that by September, I'd have 90% of the draft typed up. Yeah, but back in 1995, I neglected to say, September of *which year*.

Who is the book for? It's for any inexperienced or new driver. Now, a person who doesn't know much about driving yet, or doesn't drive, is not going to appreciate all this stuff, until later. That's OK. This is a good book for beginning and intermediate drivers. I do not think it will screw up the head of the non-driver, but it won't do him a lot of good, either. I mean, if you have never held a tennis racquet in your hand, a book about how to play better tennis is not going to sink in really well. (This book is NOT intended to teach you to drive. You need a smart driver, a good teacher, for that. Then, this book can be helpful to teach you to be a *better* driver.)

Who is going to buy this book? Obviously, that is where the mothers and fathers of the young drivers come in. They are going to buy a LARGE number of the books. That part is easy. Obviously, I can sprinkle around just enough guilt-oriented comments that people will buy. What parent would not buy this book, for his kid? Then, after the kid starts to read the book, I have to keep his interest—with good writing; interesting ideas; and, most of all, examples. Examples of accidents and near-accidents.

Obviously, this book has to get good reviews, well-targeted advertising, etc. I have a *lot* of good ideas about how to promote this book.

What's in the book? There's about 61 chapters, about 380 pages of important topics. Additionally there's about 100 pages of appendices that give you good advice on driving competently. There are four of my columns reprinted from ELECTRONIC DESIGN—on Reflex Response, Dead Cars, Stupid Dangerous Stuff, and Double-Clutching.

Where's the incentive for me to write this? Lots of $$$? Well, I am going to give one-third of the profits to safer-driving organizations, and one-third to safer-flying organizations. The other one-third (after taxes) will probably not be enough for me to retire on. But that's ok. My motivation is to save lives and save pain. Maybe in the long run, our automobile insurance rates will stop rising!

What was the first motivation for the book? My cousin lost her daughter, Christine, in an unfortunate car accident, a few years back.The idea began to grow, but I got sidetracked until the fall of 1994.

What's the big deal about safe flying? I lost three friends who flew into the ground. Chuck Everhart used to work for National, 20 years ago. He was a test engineer in National's ALIC group—he programmed our first Teradynes. He was an excellent, safe, conservative, and cautious pilot with over 5000 hours of flying time. All of his friends were confident that Chuck would be a long-term survivor, and would retire from flying at the age of 85. He was flying up in the foothills, up near Tuolomne City, Calif., in December of 1994. He was too low for a ridge, in heavy clouds; he barely cleared the ridge, but clipped a tree. Killed instantly. Too darned bad.

Ron Brown was taking a student on a lesson. A plane sneaked up behind him and did not see him. It clipped off his tail, and he lost control. They crashed and died.

Kathy Raphael was flying with her instructor and one other student, a couple years ago. They were all three good, smart pilots. They flew *up* a canyon in the Sierras, near Sonora Pass, Calif. The canyon got too tight, and they could not climb out of it, nor turn. They tried to loop out of it, crashed, and were killed instantly. They all *knew* enough to not try to fly up a canyon. But somehow, inadvertently, they did fly up the canyon. Paid a terrible price. Sigh. That motivated me.

I wish I could write a book to save the lives of young pilots, but I am not wise enough to do that. I'll let somebody else do that. But I CAN write a book to help young drivers. So I did. It just took all my spare time for a couple years.

The format of the book is explanations about how to drive correctly, and interesting stories about accidents, indicating how the various factors conspired to cause the accident.

How did this accident "happen?" What were the drivers THINKING? If you were in the same situation, could you avoid the accident by thinking? Or would you be better off if you were just trained to *react*? This book is as much about thinking, as it is about driving. I certainly am not going to teach kids anything by being preachy, but I think I can teach them with examples.

All along, I said that I wanted the list price to be not much more than 12 or 14 gallons of gas. Paperback. Affordable. (But if the price of gas goes down or up, I am not going to change the price of my book.)

I pitched this book to several publishers. I got a nice rejection letter from each one. That's OK. I just decided to self-publish. I'll show all those guys they were wrong! (Revenge is a GREAT motivator!)

Is there a possibility of a sequel, a video, a CD-ROM? Quite possible, if I get suggestions from readers. But I want to get this book out promptly, and start saving lives.

Ah yes, and what is the theme of the book? That quote from Count Otto von Bismarck, that was on the back cover of my older book: "Fools you are ...who say you like to learn from your mistakes.... I prefer to learn from the mistakes of others, and avoid the cost of my own."

For more information on this book, send a note to the address below, or you can also check out my new web sitew and obtain complete information: *www.transtronix.com*. To order this book, now in stock, send a check for $21.95 (tax and shipping included) to: Robert A. Pease, Pease Publishing, 682-E Miramar Ave., San Francisco, CA 94112-1232.

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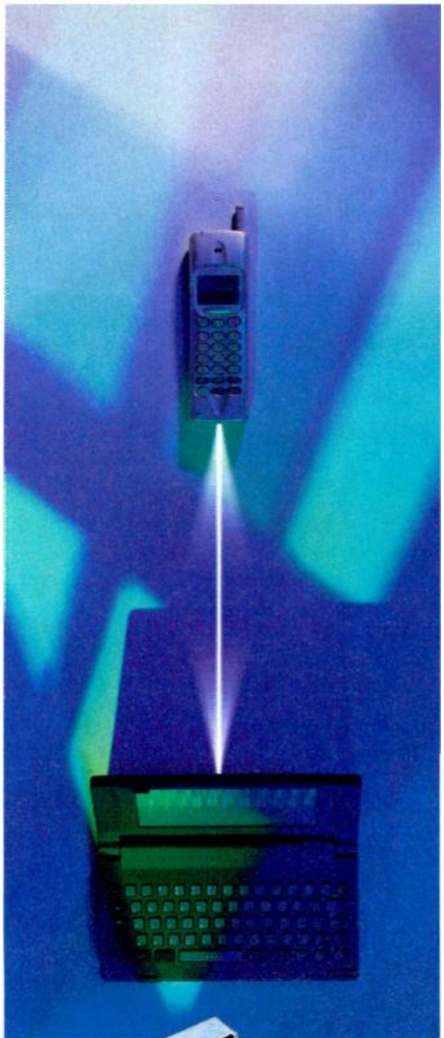

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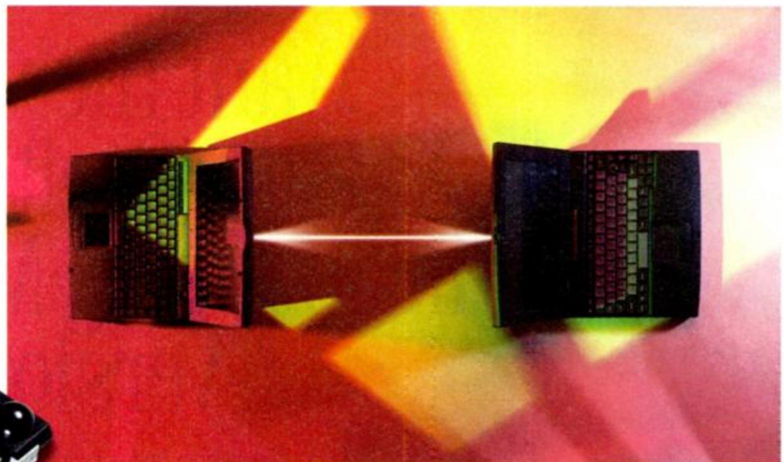

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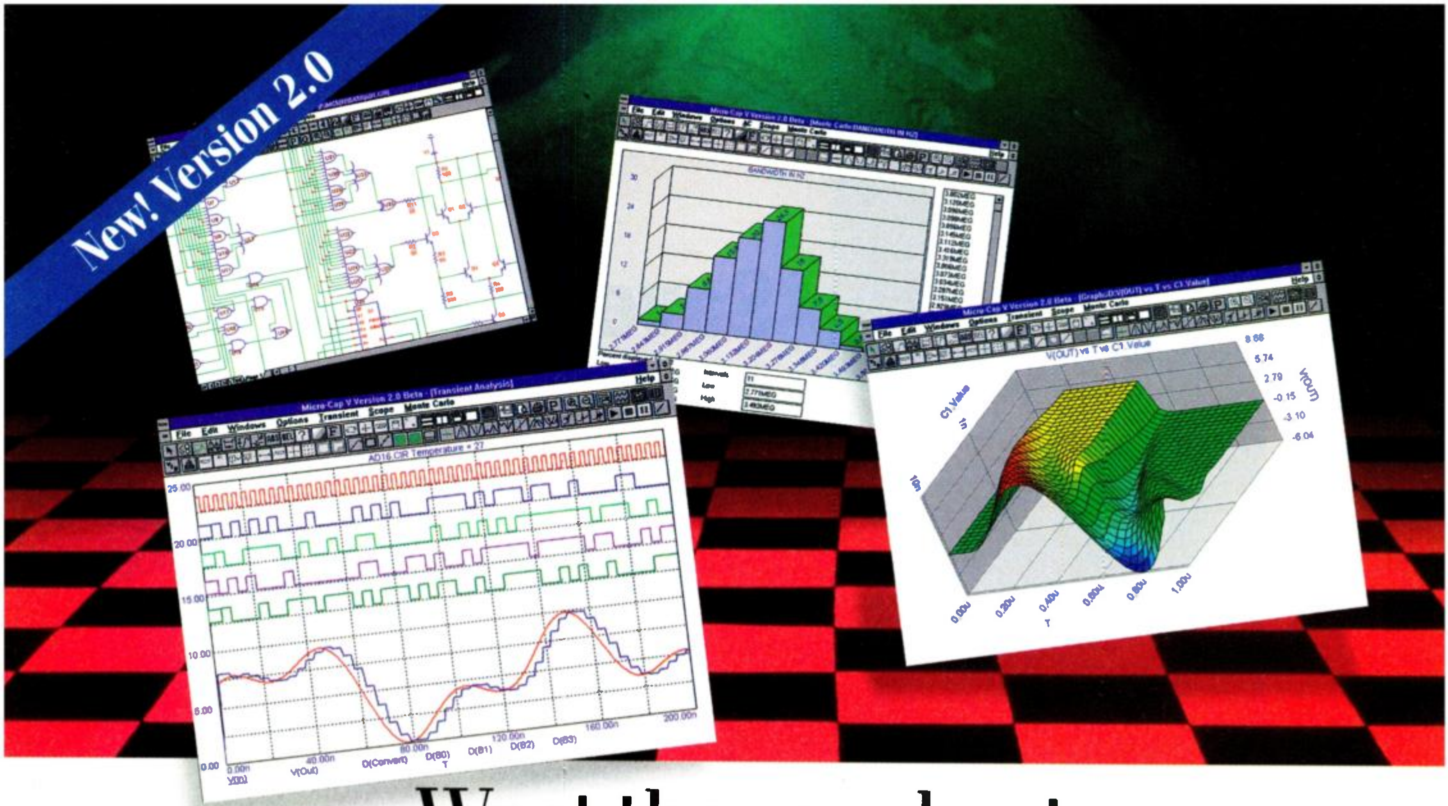

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Op-Amp Audio

Realizing High Performance: Buffers (Part I)

In this and the next few columns, we will take a departure from the immediate past, and focus some overdue attention on real circuits. We'll cover some op-amp issues related to realizing high performance in audio and other ac applications. This venture has been inspired in part by reading some USENET newsgroup postings, with such confidence-boosting headers as: *"Op Amps always inferior to discrete?"* and others equally as upbeat in tone.

While I can't promise any panaceas, I do have confidence that a greater understanding can come from some focused discussions of op-amp audio pitfalls. Topics to be covered are: buffering, the IC op amp's best friend (this and next installment); matching an op amp to an audio application; and op-amp wisdom and witchcraft.

How many inputs does an op amp have? I find it useful to look at op-amp performance in terms of errors in response to various inputs. These inputs can come via the normal differential ones at pins two and three, *plus at least three others*. Aha! Stumped on that one? So, what else constitutes an input, beyond the two familiar power-supply-rejection-ratio (PSRR) errors for an amp's $+V_S$ and $-V_S$ terminals, disregarding any offset pins?

Well, it may or may not be obvious, but the *output* terminal of an IC op amp can actually be the source of the fifth *input* error, one which results in load-induced changes in offset voltage. Although all modern, single-IC op amps are designed with thermally symmetric, input-stage layouts vis-a-vis the output (for minimum thermal feedback), life isn't completely perfect here. Consider the fact that just microvolts of undesirable offset change can be significant at low audio frequencies. Take a 5-MHz bandwidth op amp as one example, where a 1-V p-p/100-Hz output swing requires an effective 20-µV p-p differential input.

So, whatever their source, extraneous signals might easily be comparable to actual signals of this magnitude. In a low-noise, bipolar-input op amp, a thermal change resulting in a few degrees Celsius temperature differential to the input stage might induce a fraction of a microvolt or more offset shift. Although such an error seems numerically small, it's still relatively large with respect to a 20-µV p-p, real signal. The point is not that this example represents any real device or conditions. It is more to frame some perspective and sensitivity for monolithic-IC-based technology, and the resulting application implications.

The figure shows a typical op-amp gain stage, configured here as an example application with an ideal gain of 5x, driven by a signal V_{IN}. The previously mentioned op-amp error sources are as noted, represented by sources V1 to V5. The dotted lines are intended to convey a general relationship of a given error to the source.

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For example, the output-power-dissipation-related errors are reflected back to the op-amp input as a thermally coupled offset change, V5. For this installment of the overall discussion, I'll concentrate on this error, picking up the others further down the road.

Both single, as well as multiple, op amps built on common monolithic substrates can be susceptible to thermal errors. This is simply because a potentially high-dissipation output stage and the error-sensing input stage are part of the same basic monolithic IC chip. In the classic reference, thermal effects in IC op amps were discussed, and modeled as an additional feedback path, which can limit available gain.[1]

It is worth noting that IC designs are a diverse extreme away from conventional pc-board discrete circuits, which are by definition, loosely-coupled thermally. *Hybrid* op amps may or may not be thermally sensitive, depending on their specific substrate and layout details. *Modular* op amps should be relatively insensitive to thermal effects, unless potted with a thermal compound.

Testing for thermal errors: Quantifying op-amp input-offset errors due to output loading isn't totally straightforward, but it isn't impossible either. For audio-oriented use, one straightforward technique is to measure output THD+N and/or other distortions under both heavy and light output-loading conditions. This will reveal degradation due to thermal-coupling effects. However, dc and low-frequency testing may actually give some greater insight into what happens to an op amp as it undergoes heavy loading. This is because one can literally *see* the changes in transfer function, as output loading changes.

Relatively simple, dc X-Y plots can give visual indications of amplifier linearity under load. See Reference 2 for an example of a single-op-amp test circuit for plotting amplifier input drive on the Y axis vs. loaded ± output swing on the X axis. This test is easily expanded to include loaded and unloaded comparison conditions, which can then reveal dynamic-thermal-error components, as well as transfer nonlinearity.

For this article, I modified the test circuit as follows. I changed the summing-node attenuation resistors from 1MΩ/10 Ω to 100 kΩ/10 Ω, added a 10-Ω balancing resistor in the positive input, and made the total load resistance 530 Ω. To test various op amps, I made the offset trim universal by summing a stable, variable ± voltage into the 10-Ω summing resistor via 100 kΩ. If you repeat this setup, use clean, well-balanced layout techniques and stable supplies, and you'll be able to observe 1 µV/division on your scope.

These steps make the new V_Y error scaling 100 µV/V, which is easily sensitive enough to see µV-level input changes with 10-mV/division scope scaling. The display allows you to measure loaded and unloaded gain, as well as associated changes in slope, which represents device nonlinearity.

With a ±10-V output, and 530-Ω loading, nonlinearity is readily evident with standard 5534 audio IC op amps. In one sample, the offset shift and slope changes from low load to full load. This results in about 60 µV of offset change, with a steep slope change with polarity reversal (although this is a large shift in terms of the error change, it is still relatively small vis-a-vis the ±10-V output).

Precision low-noise op amps such as the AD797 and LT1115 are much more well-behaved for this test, with similar-

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conditions errors of about 1 μV, and no radical slope changes. Look for low- and linear-slope errors, which represent linear gain, as opposed to radical changes and transfer function kinks.

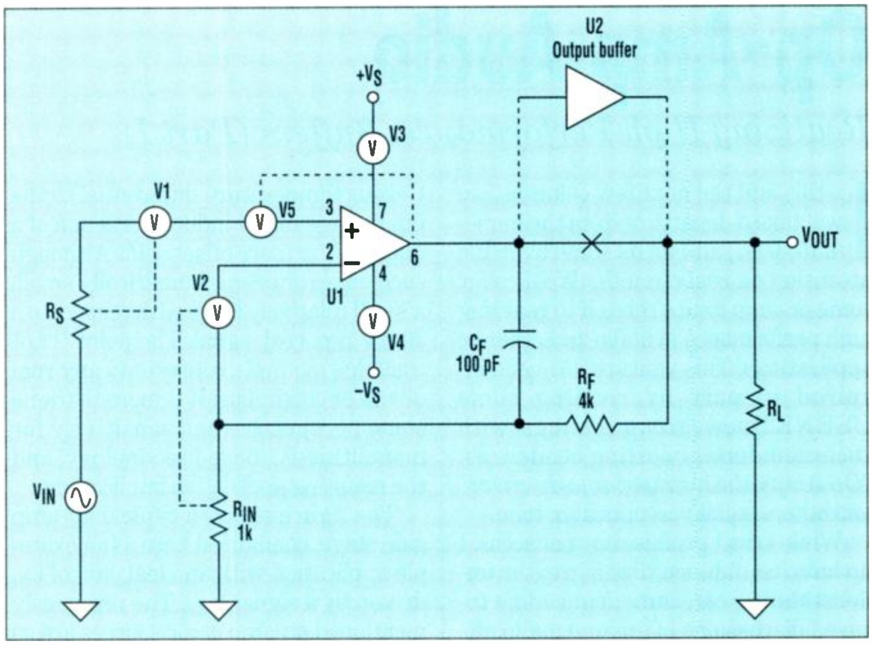
Dual IC op amps are very popular, and can also be easily tested for power-dissipation-related crosstalk.[3] One of the more simple, yet useful tests, is to connect channel A of a dual op amp as a grounded-input follower, with channel B configured in a closed-loop, gain-of-1000 circuit. By driving current into the A side, A-B thermal coupling can be measured at the B output. By controlling the polarity, frequency, and duty cycle of the driving current, useful information on a device's channel-to-channel thermal coupling can be obtained.

What may be surprising about some thermal errors is the relatively high frequencies at which they can be noticed. For example, a dual-output power-driver circuit, using a composite topology can be monitored for the effects of thermal crosstalk between the driven and undriven channels.[4] Crosstalk components were noted up to several kHz.

Minimizing thermal errors: By using one or more of the tests above, various amplifiers can be exercised for thermal errors, and comparisons can be made to find types with the lowest thermal errors for loaded conditions. But, audio op amps tend to be more specialized, and it may be that your favorite chip just doesn't look so good for thermal errors. Not to worry, there is still a worthwhile *system* solution, one which really turns out to be optimized for solving thermal problems and maximizing performance.

As shown in the figure, the answer is to simply split the voltage amplification (U1) and power-delivery functions (U2) by *buffering* the output of an IC op amp with a dedicated circuit, chosen (or designed from scratch) for more-than-sufficient drive current. The burden of current delivery and associated power dissipation is simply (entirely) removed from op amp U1. This is shown conceptually as the optional (dotted connection) buffer stage in the figure. The buffer is activated by breaking the output line at "X," and connecting the unity-gain buffer U2 as noted.

With the buffer used, the main feedback path through R_F is taken after the buffer, and across the load, R_L. The buffer circuit proper may include some specific details, such as bypassing, parasitic suppression resistances, etc.; this will be an individual thing. There should almost always be some sort of isolation impedance between the buffer output and the output terminal, to isolate any cable capacitance. This can either be a small, 20- to 100-Ω resistor, or the LR network described in Reference 4.



There is also a high-frequency, ac-feedback path through C_F, which has the effect of removing the buffer from the circuit at very high frequencies, in this case at $1/(2\pi R_F C_F)$. This also aids with stability when driving long cables or other difficult loads.

Choosing a buffer circuit: One has a basic two-path choice—an IC or a discrete circuit. ICs tend to be more desirable from points of size and efficiency, but they may not be lower in cost, or useful beyond about several hundred mA in non-heatsink packages. Discrete circuits can be tailored for any current level, but they tend to be quite busy in terms of component count, especially with such bells and whistles as current limiting and protection circuits.

Performance-wise however, both of these circuit approaches to buffering can be used, and either will allow the highest realizable performance for a given op amp. If an IC buffer is used, one can almost have the cake while eating it, too. This is done by packaging a simple, four-lead IC buffer like the BUF04, and a highly linear IC op amp such as the AD744, together as a (isolated) two-chip solution in a common package. Other dedicated IC buffers I have used successfully in the past have been the OPA633, EL2003, LT1010, LH0002, and LH0033, all of which deliver ±100 mA (or more). Video op amps like the AD811 and AD817, also work well as buffers, due to their good linearity and high-current output stages.

The U1 op-amp-circuit part can really be left to optimize from other standpoints. Whatever it is, it will be most happy when lightly loaded via a fast, linear, high-current buffer.

TIP: In the next installment we'll look at some more issues associated with buffering, and describe in detail a suitable discrete-circuit version.

References:

1. Solomon, J., "The Monolithic Op Amp: A Tutorial Study," *IEEE Journal of Solid State Circuits*, December 1974; Vol. SC-9, No. 6.

2. "Open-Loop Gain Linearity Test Circuit," Figure 3, Analog Devices OP177 data sheet.

3. "Crosstalk from Thermal Effects of Power Dissipation," Figures 24-26, Analog Devices AD708 data sheet.

4. Jung, W., "Composite Line Driver with Low Distortion," *ELECTRONIC DESIGN Analog Applications*, June 24, 1996, p. 78.

Walt Jung is a corporate staff applications engineer for Analog Devices, Norwood, Mass. A long-time contributor to ELECTRONIC DESIGN, he can be reached via e-mail at: Wjung@usa.net.

Redesigned DSP Workshop Accelerates Development Cycles

The MathWorks has unveiled the newest version of its DSP Workshop suite that accelerates the development process between algorithms and implementation into a product. In short, the new DSP Workshop is designed to further narrow the gap between concept and prototyping of real-time DSP software, according to The MathWorks.

The tool suite integrates algorithm design, block diagram simulation, code generation, and analysis tools into a single interactive development environment. To achieve that, the company has bundled MATLAB, Simulink, DSP Blockset, and Signal Processing Toolbox into one package.

Besides improving simulation speed by an order of magnitude, the redesigned DSP Workshop provides tighter migration path between its tools, says The MathWorks market segment manager Anne Mascarin. It also improves design efficiency, as well as enables DSP engineers to simulate an entire system-level design. As a result, DSP engineers working on telecom and consumer applications can now perform real-time algorithm design and simulation, and generate C code in the shortest possible time, says Mascarin. Plus, the availability of these tools on a PC platform further brings DSP simulation and implementation to a broader base, claims The MathWorks.

At the core of the improved DSP Workshop suite is the fundamental architectural improvements in the DSP Blockset version 3.0, which offers much faster design cycles and simulations. In fact, the DSP Blockset 3.0's frame-based processing allows users to process blocks of data, as well as individual data samples within a time-driven simulation.

According to The MathWorks, the redesigned DSP Blockset 3.0 leverages the new infrastructure in Simulink 3.0 for use in real-time speech, audio, and communications applications. Each block now automatically adapts to the incoming signal's data type, sampling rate, and frame size. These enhancements reduce the size of the simulation models and generated real-time code, while eliminating the time-consuming and error-prone task of manually verifying the properties of each individual block. Consequently, says The MathWorks, the simulation speed of the new version is 10 times or greater than the previous version.

Other enhancements to the DSP Workshop include usability and scalability. Simulink 3.0 comprises complex data types, sample-rate propagation, and efficient support for multirate systems that support real-time DSP algorithms. In essence, the revised DSP Blockset 3.0 now contains all of the essential matrix math and signal processing functionality required for the devel-

(continued on page 169)

(continued from page 168)
opment of DSP algorithms. Earlier DSP developers had to depend on tools like the MATLAB and the signal processing Toolbox.

With the addition of over 50 new blocks, the DSP Blockset 3 now can support linear algebra, spectral estimation, multirate filters, and filter banks, as well as perform control operations. As a result, according to The MathWorks, users are able to move MATLAB-derived algorithms directly into simulation, and then map the system-level design into implementation. This seamless migration between initial concept and simulation is unique, and dramatically shortens design-cycle time, says Ken Karnofsky, DSP marketing manager at The MathWorks.

Likewise, the filter design software within the Workshop also has been streamlined to allow an integrated design flow. For example, the graphical user interface added to the Signal Processing Toolbox 4.3 enables visualization of filter designs. Consequently, by using the pole-zero editor of the Toolbox 4.3, an engineer can design the filter through graphical placement of poles and zeroes. Also, the DSP Blockset 3.0's filter realization wizard automatically generates efficient block diagrams from the user's specifications. The DSP Blockset now supports fixed-point FIR filters of word lengths up to 128 bits.

For rapid prototyping, an optional ANSI C code generator, called Real-Time Workshop, is available. This allows DSP designers to generate ANSI-standard C code from Simulink block diagrams for any floating-point DSP targets. The optional Real-Time Workshop costs $9995. Designed to run on PCs, Macintosh, and Unix workstations, the new DSP Workshop is priced at $5900.

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GMT Microelectronics Corp., *1735 N. First St., Suite 302A, San Jose, CA 95112; (408) 487-9050; Internet: www.gmtme.com.* **CIRCLE 591**

Embeddable Engine Stuffs RMON2 Into Gigabit Networks

The MeterFlow application recognition engine provides designers with a drop-in solution for implementing powerful application recognition. It can be used to provide management features in switches at a very low cost per port.

The engine is an advanced parallel processing architecture that can be implemented in either hardware or software. The embeddable engine provides a scalable solution for implementing RMON2, QoS, policy management, security, and other embedded traffic-management applications in 100-Mbit and Gigabit Ethernet products.

MeterWorks Pro 5.0 is a new release of an RMON2 software development kit (SDK) that's optimized to take advantage of hardware or software implementations of the MeterFlow engine. When used with MeterFlow, MeterWorks Pro provides a 1000 to 1 reduction in processing requirements over traditional packet-counting routines used for implementing RMON2.

MeterFlow is available as a complete synthesizable, RTL-ready Verilog implementation or as C code. Licensing fees vary according to application and volume of usage. LG

***Technically Elite Inc.**, 6330 San Ignacio Ave., San Jose, CA 95119; (408) 574-2300, (800) 474-7888; fax (408) 629-8300; www.tecelite.com.*
CIRCLE 592

Versatile Multiport DSL Chip Set Targets Central Office Apps

Targeted at telcos and their equipment suppliers, the Rockwell eight-port central-office ADSL device is intended for central-office applications that require low power consumption and high port density. The highly integrated chip set supports the full-rate ANSI T1.413 Issue 2 Discrete Multitone (DMT) ADSL standard. It also features a flexible, scalable design. Consequently, it can simultaneously support the industry's forthcoming G.lite standard for easy-to-deploy, "always-on,"consumer-oriented 1.5-Mbit/s Internet access services.

The Octal central-office ADSL device set's low-power RISC controller manages eight ADSL line transceivers so that it can support eight ADSL channels in DSL Access Multiplexers (DSLAMs) and other central-office remote-access devices. The device set also includes a companion ATM Utopia Level II PHY chip that concentrates eight lines of data-pump traffic to reduce pin count.

Power consumption is limited to 1.9 W per channel in G.lite mode and 2.7 W per channel in full-rate mode, making it a good solution for digital loop carriers (many of which are powered remotely).

Samples of the central-office Octal G.lite/ADSL device set will be available in late 1998, and volume production is scheduled to begin in the first quarter of 1999. The device set is priced at $67.50 per port in 10,000-unit volumes. LG

***Rockwell Semiconductor Systems**, 4311 Jamboree Rd., P.O. Box C, Newport Beach, CA 92658-8902; (800) 854-8099 or (949) 221-6996; e-mail: rockwell@salessupport.com.*
CIRCLE 593

System Two

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Leading edge performance has been a defining feature of Audio Precision products since the inception of our company in 1984. Thousands of our System One audio analyzers are in use worldwide, selected by design engineers for high performance and by test engineers for our comprehensive programmable analog and digital audio measurement capabilities.

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System Two is a true Dual Domain analyzer. Other test instruments may have both analog and digital inputs and outputs ... but they're not true Dual Domain! They rely on performance-limiting converters to pass analog signals back and forth to a DSP core of digital-only hardware. Passing signals through a/d or d/a converters for every measurement robs the test instrument of performance. System Two includes separate, independent hardware for direct audio measurements in both domains, plus additional and extensive interface measurement capability including jitter measurements, eye patterns and all other parameters described in AES3, the serial audio interface standard.

The new standard of System Two is represented by performance specifications such as guaranteed analog generator and analyzer residual THD+N of -108 dB, guaranteed analog signal flatness of ±0.01 dB for the generator and analyzer; and 24 bit digital signal generation with 48 bit FFT dynamic range.

From aircraft to automobiles, satellites to cell phones, headsets to hearing aids, System Two represents a new standard for audio frequency test & measurement applications. Compare for yourself - our worldwide force of representatives will be pleased to provide comprehensive specifications and a true Dual Domain on-site demonstration.

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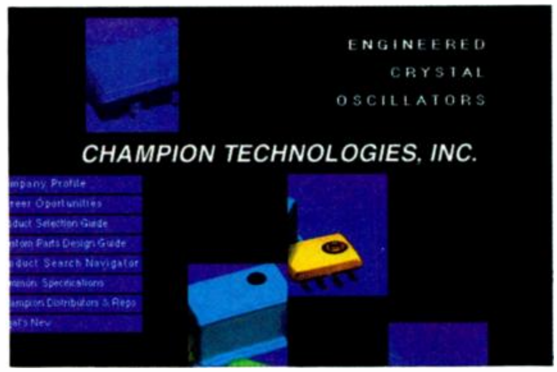

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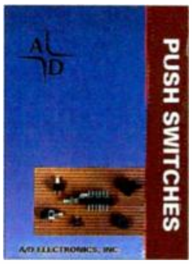

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A/D ELECTRONICS

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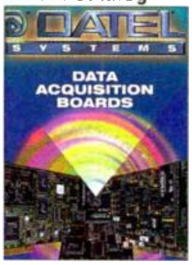

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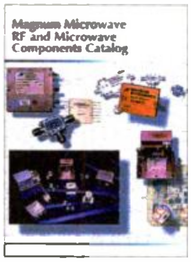

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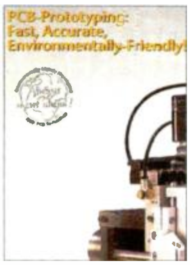

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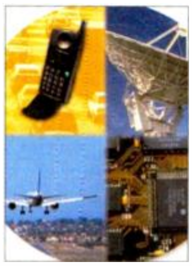

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MENTOR GRAPHICS

GIANT NEW SWITCH CATALOG

APEM's new 420 page full-line catalog is packed with their switch offerings. New products added: toggles, rockers, push-buttons, tacts, keys, industrial controls, DIPs, rotary DIPs, micro-limits, pushwheels, slides, keyboards, sealing boots. Many state-of-the-art switch models featuring process compatibility, surface mounting technology & electrostatic discharge withstanding. APEM Tel: 781-246-1007, Fax: 781-245-4531, URL: http://www.APEM.com E-Mail: info@APEM.com

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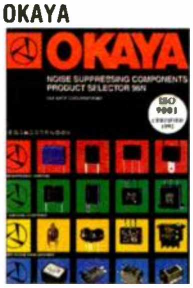

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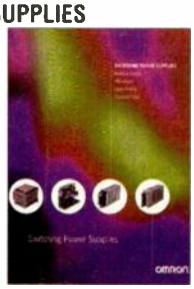

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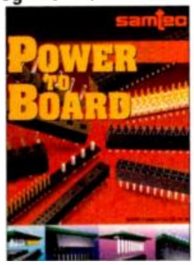

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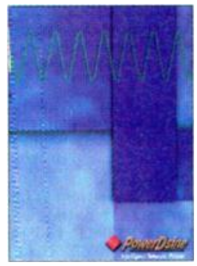

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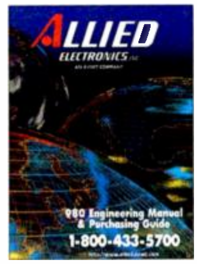

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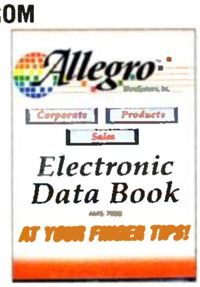

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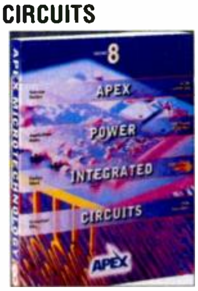

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APEX

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C&K's EXPANDED BROADLINE CATALOG

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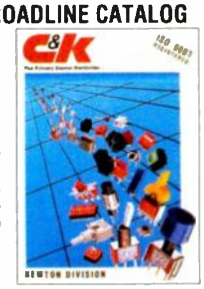

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ELECTRONIC DESIGN CATALOG/LITERATURE REVIEW

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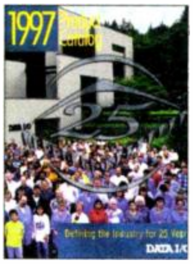

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DELTRON

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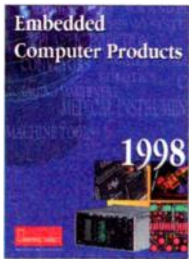

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GESPAC INC.

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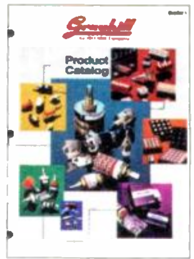

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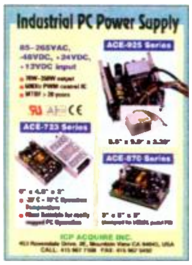

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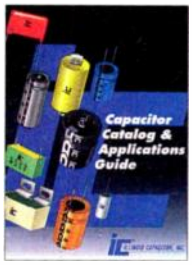

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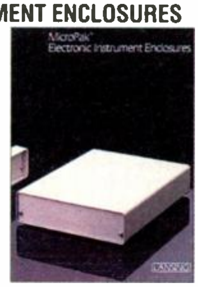

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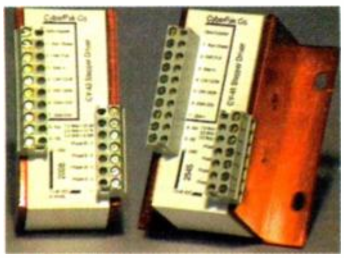

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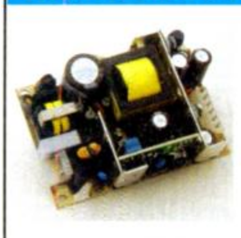

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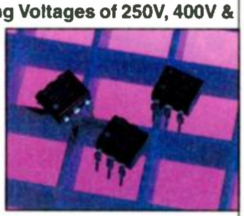

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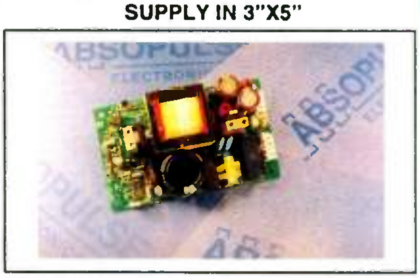

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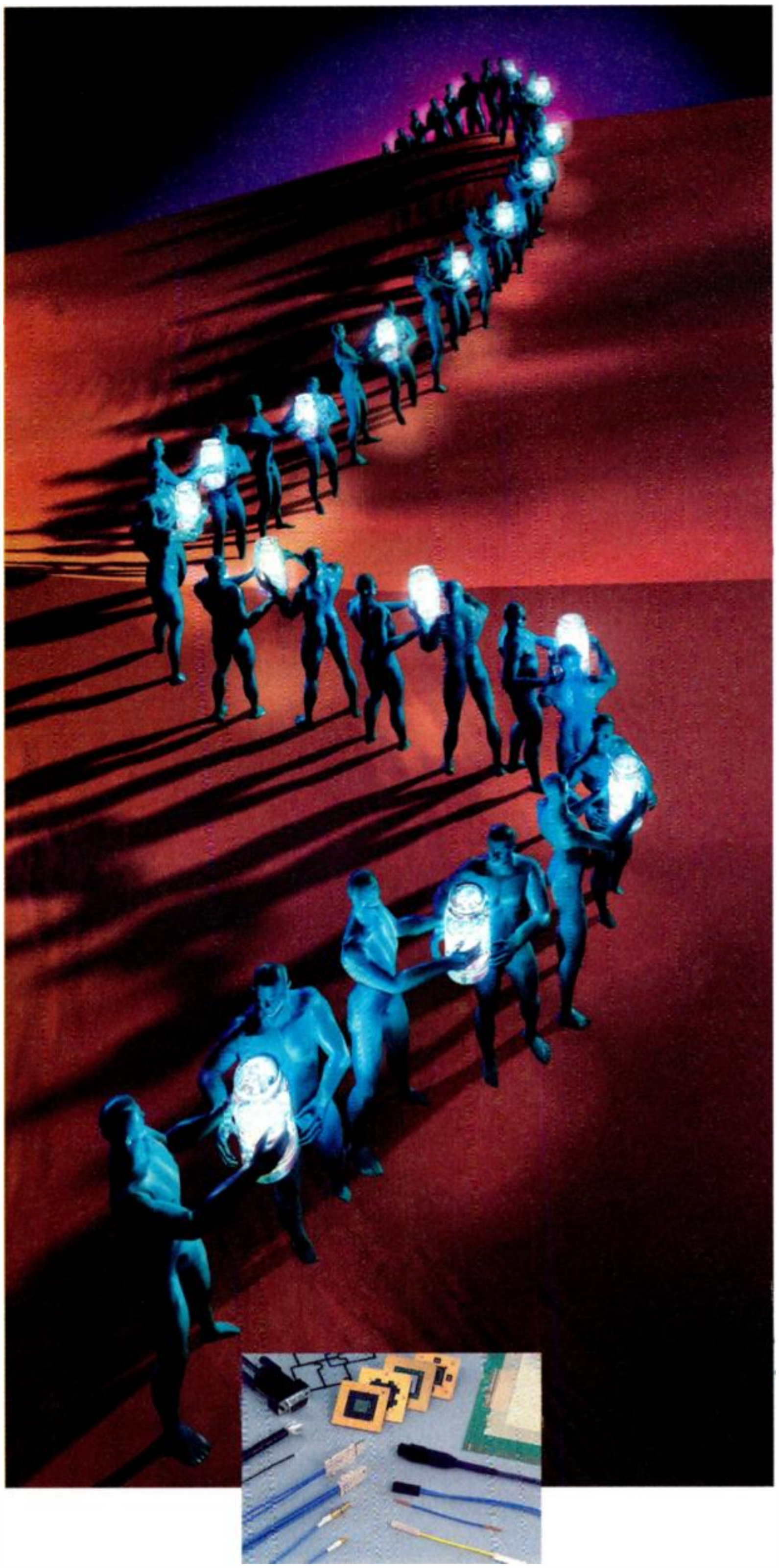

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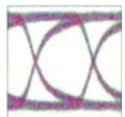

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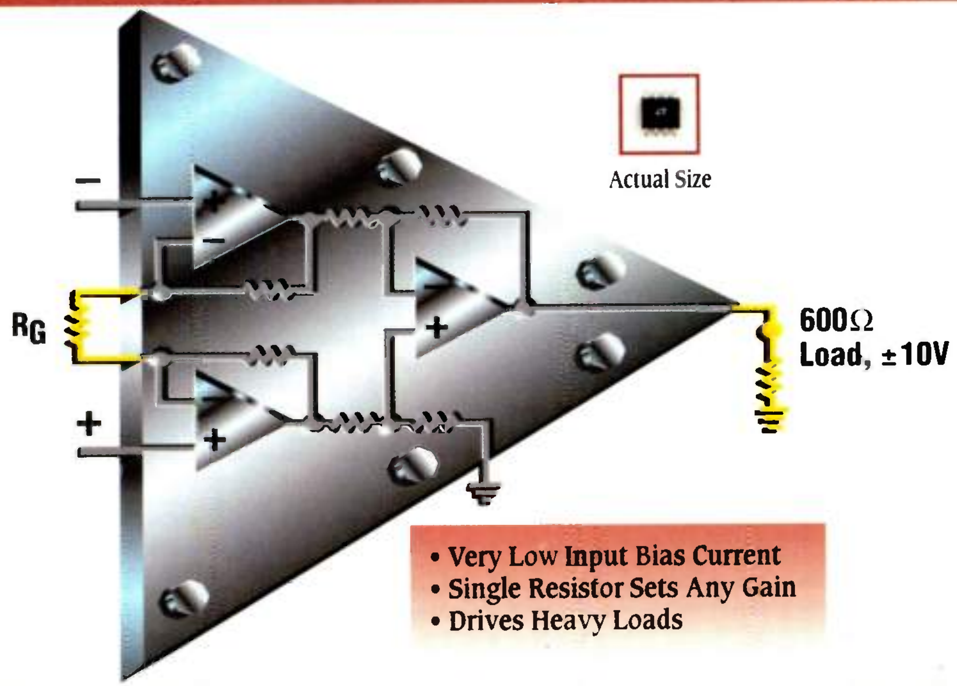

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