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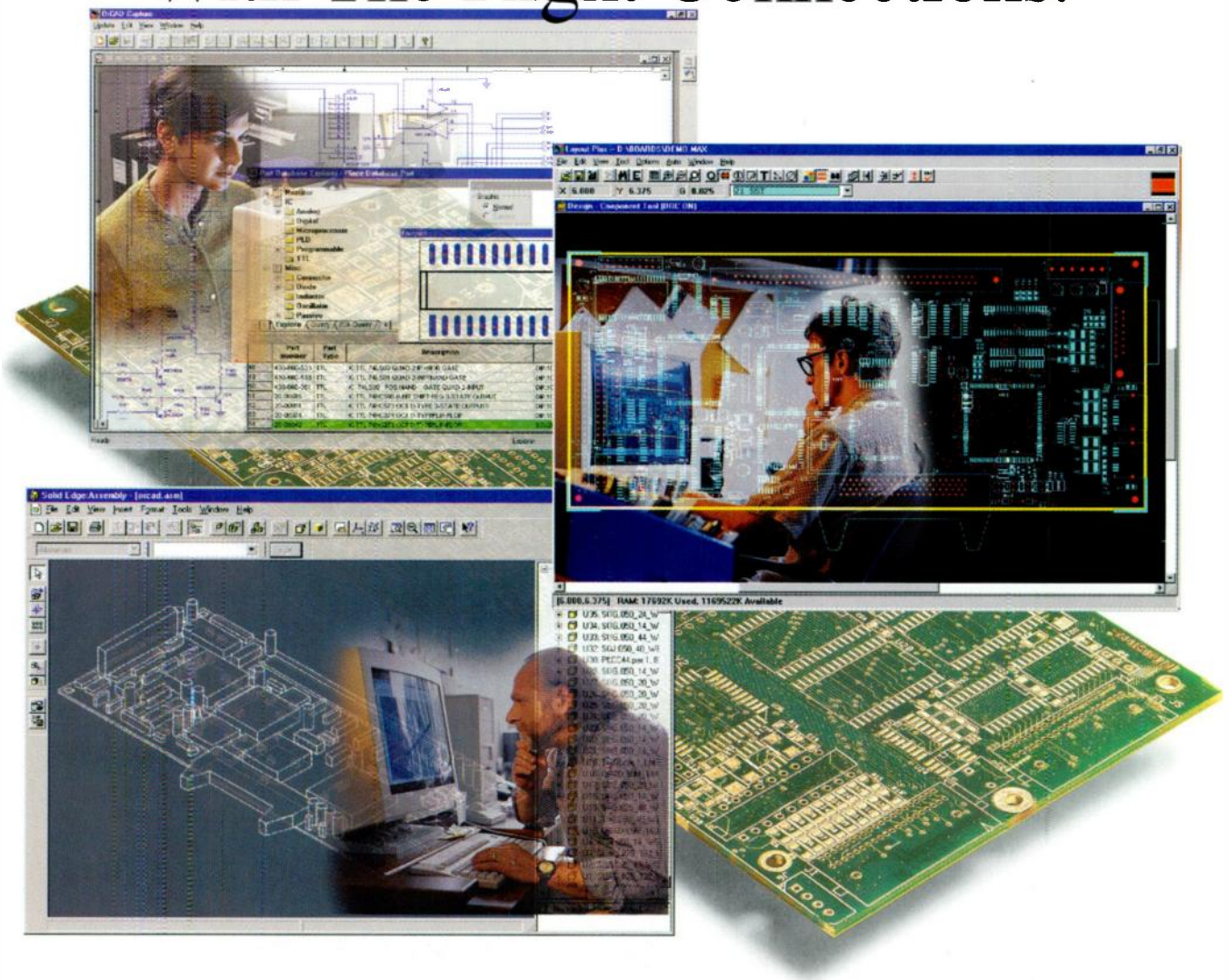
TECHNOLOGY • APPLICATIONS • PRODUCTS • SOLUTIONS

A PENTON PUBLICATION $8.00 www.elecdesign.com SEPTEMBER 14, 1998

Comm-Fusion Engine Bridges Multiple Protocols p. 34

Amazing What You Can Do With The Right Connections.



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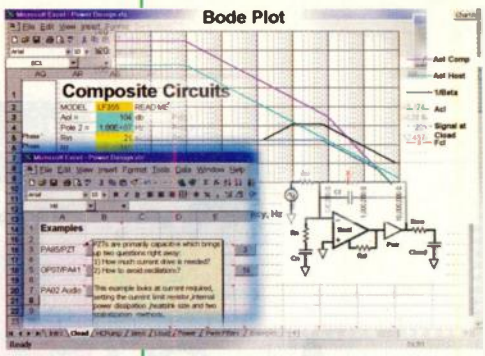
Applications 101: Power Amplifiers

APEX MICROTECHNOLOGY

Hand Tools or Power Tools?



New Computer Aided Power Design Tool

Apex's new computer aided Power Design Tool is a self-documented spreadsheet that automates the tedious calculations associated with:

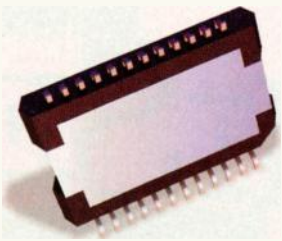
- stability analysis
- internal power dissipation
- current limit
- PWM filter design

This spreadsheet also includes examples which can be used as tutorials on power op amp design. This design tool is **free** and can be downloaded from the Apex web site at www.apexmicrotech.com. Upon execution it is suitable for Excel 5.0 through Excel 97.

New Computer Aided Design Tool Automates Designing With High Voltage Amplifiers

PA44

New Surface Mount 350V, 120mA Monolithic Power Op Amp



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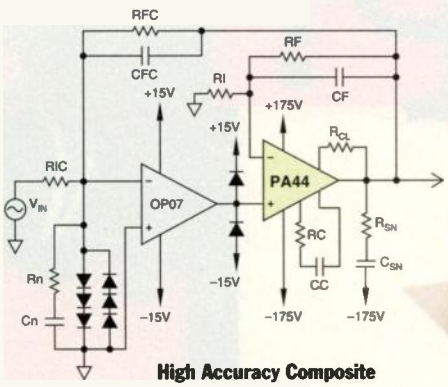

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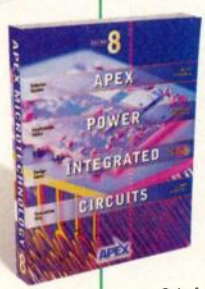

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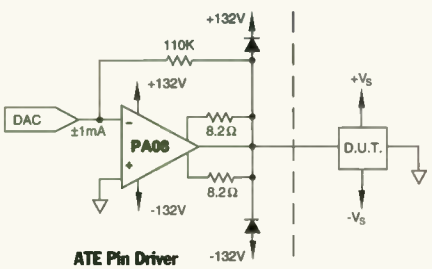
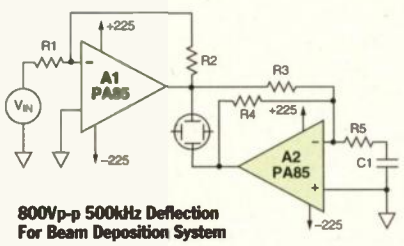


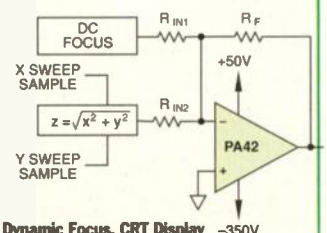
ATE Pin Driver



800Vp-p 500kHz Deflection For Beam Deposition System

High Voltage Amplifiers Product Selector Guide

Model	Supply	I_{OUT} Peak	$I_{STANDBY}$ Max	Slew Rate	Package
PA08	30V-300V	200mA	8.5mA	30V/µs	TO-3
PA41	100V-350V	120mA	2mA	40V/µs	TO-3
PA42	100V-350V	120mA	2mA	40V/µs	SIP
PA44	100V-350V	120mA	2mA	40V/µs	PSOP
PA85	30V-450V	350mA	25mA	1000V/µs	TO-3
PA88	30V-450V	200mA	2mA	30V/µs	TO-3
PA89	150V-1200V	100mA	6mA	16V/µs	PowerDip



Dynamic Focus, CRT Display

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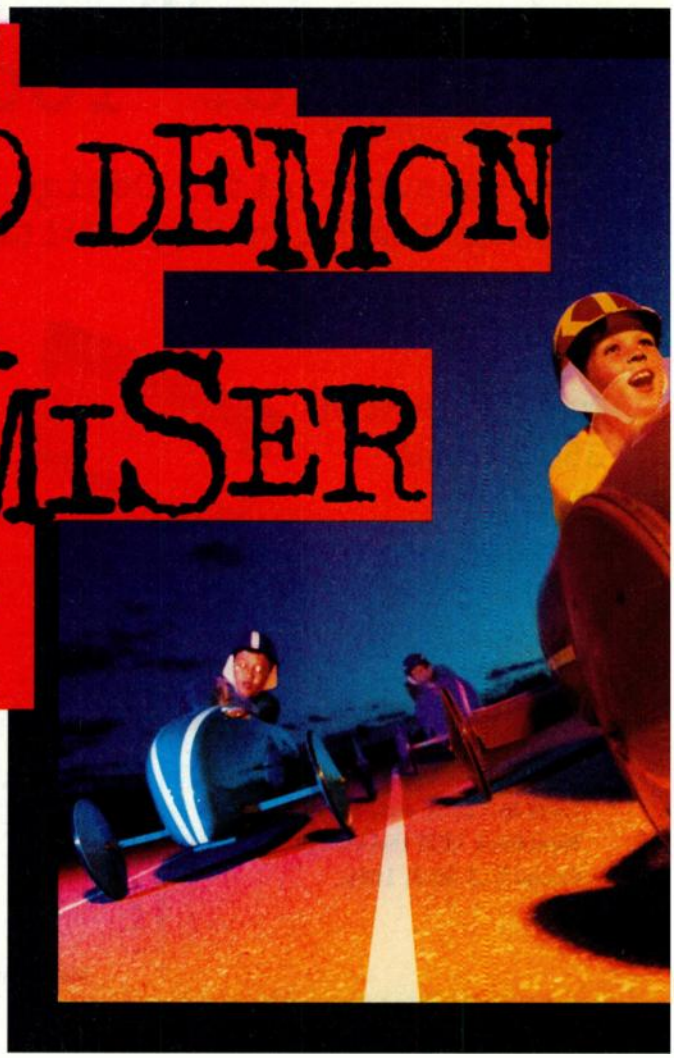
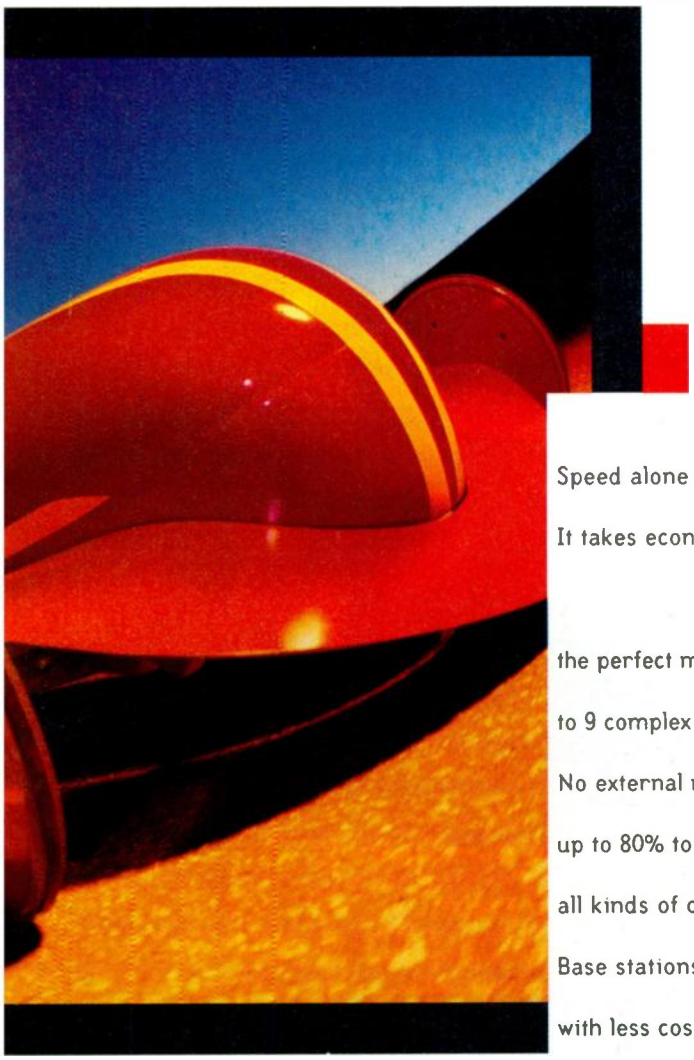
What's it going to take

TO PUT A SPEED DEMON IN A POWER MISER CHIP?





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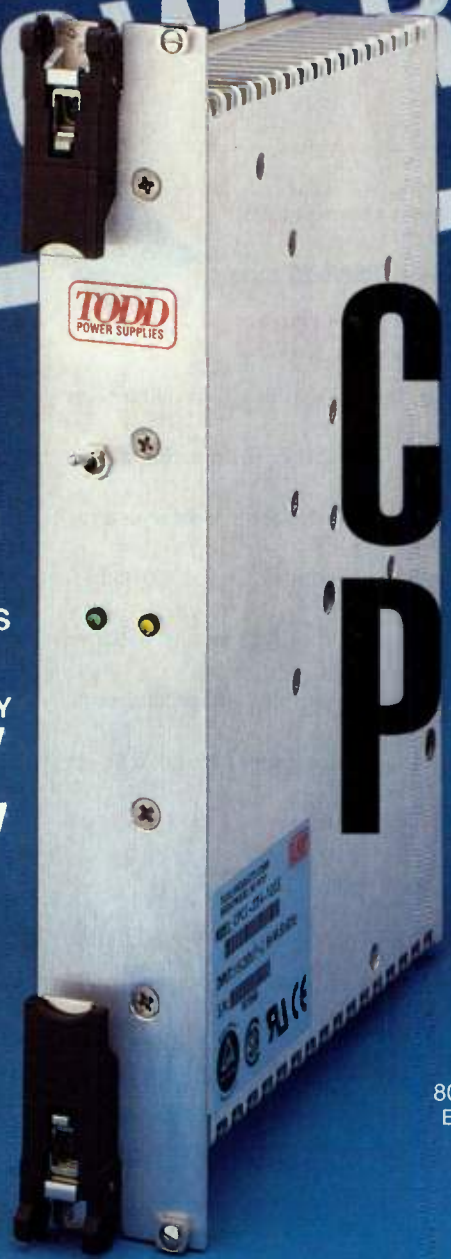

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ELECTRONIC DESIGN

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September 14, 1998 Volume 46, Number 21

EDITORIAL OVERVIEW

TECH INSIGHTS

BOARDS & BUSES

DEPARTMENTS

Penton

ELECTRONIC DESIGN (ISSN 0013-4872) is published twice monthly except for four issues in May, three issues in February, three issues in August, three issues in October, and three issues in November by Penton Media Inc., 1100 Superior Ave., Cleveland, OH 44114-2543. Paid rates for a one year subscription are as follows: $100 U.S., $170 Canada, $180, $200 International. Periodicals postage paid at Cleveland, OH, and additional mailing offices. Editorial and advertising addresses: ELECTRONIC DESIGN, 611 Route #46 West, Hasbrouck Heights, NJ 07604. Telephone (201) 393-6060. Facsimile (201) 393-0204. Printed in U.S.A. Title registered in U.S. Patent Office.

Lots of people sell chip inductors. But only ours come packaged with new ideas.

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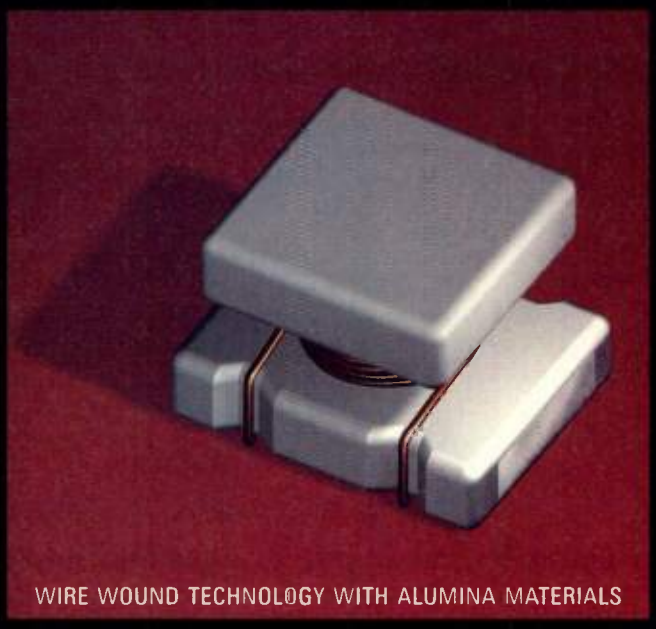
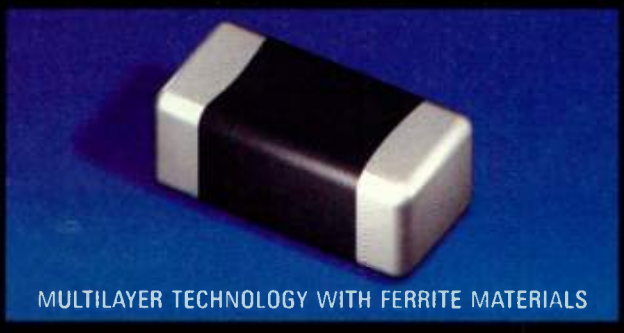


WIRE WOUND TECHNOLOGY WITH ALUMINA MATERIALS



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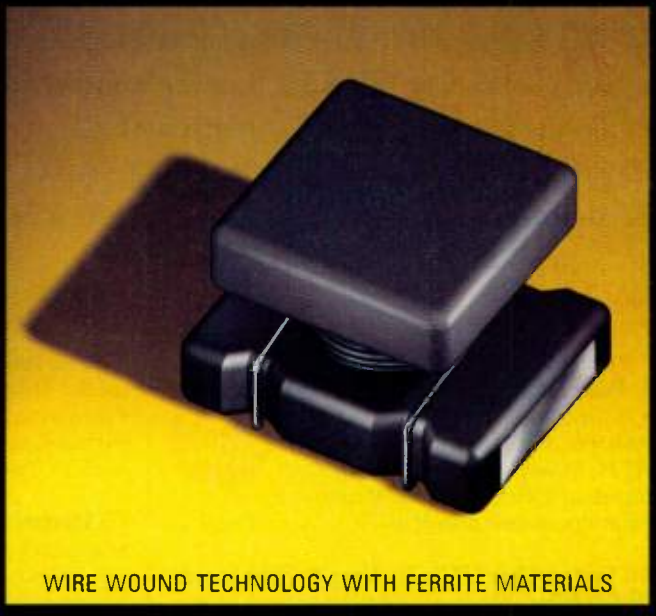

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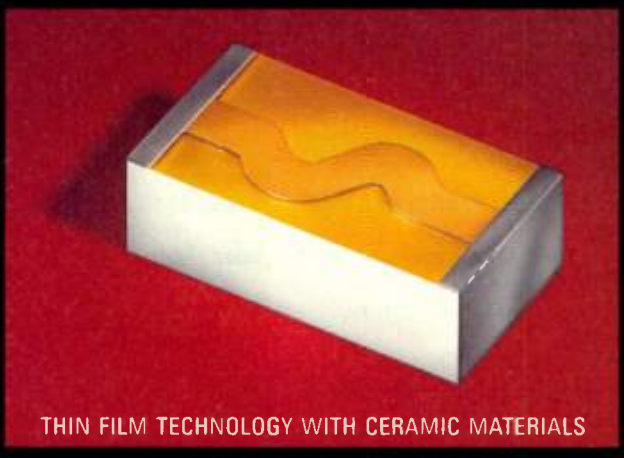

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ELECTRONIC DESIGN

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September 14, 1998 Volume 46, Number 21

EDITORIAL OVERVIEW

TEST & MEASUREMENT

QUICKLOOK

LOOKING AHEAD: October 1, 1998

- **Special Digital Section:** Digital IC technology is the focus of this section, which will contain a half-dozen Design Application articles on tips for using CPLDs, as well as a Special Report on CPLD technology.
- **Embedded Operating Systems** This special report by Contributing Editor Loren Werner will examine how embedded operating systems are striving to meet the need for enhanced productivity levels.
- **Portable-By-Design/Wireless Supplement:** Abstracts of several technical presentations made at the Wireless Symposium, as well as the Portable By Design Conference, Feb. 9-13, are contained in this supplement.

COVER ILLUSTRATION BY: BRUCE JABLONSKI, BOB MOYER

Jesse H. Neal Editorial Achievement

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ONLINE OVERVIEW

September 14, 1998 Volume 46, Number 21

See Electronic Design Online's Table of Contents to preview what's in store for you on the web!

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Beginning October 1, **Electronic Design** will be holding a contest for EEs who fancy themselves as creative writers. If you like to write short stories or enjoy composing poems, now's your chance to show off your skills. But here's the catch--your prose must contain as many names of EDA tool vendors as possible, and the piece cannot exceed 300 words in length.

The contest will run until November 30. Winners will be announced via **Electronic Design Online** on December 15, and they will be awarded one of a group of prizes donated by EDA tool vendors. Sound like fun? For further details, see our home page at **www.elecdesign.com.**

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EDITORIAL

The 1000-Year Digital Reich?

I scan a lot of business and consumer magazines because I want to know the high-tech information de jour of my non-trade editorial cousins. I'll peruse *Business Week*, *Fortune*, and *Forbes* to see which technology articles the Captains of Industry are digesting. And I'll read *UPSIDE*, *Fast Company*, and *Wired* to see what the techno-hip are reading.

Although I'm pleased to see more science and technology replacing mutual fund and retirement planning articles in the business magazines, I'm dismayed to see a lack of objective, critical analysis, and the overuse of market projections that seem a bit high at times. But, at least they're trying to inform, even if it's at a basic level. Of course, the surge in computer advertising is also a great motivator for these magazines to boost their high-tech coverage. Hey, they're capitalists writing to capitalists.

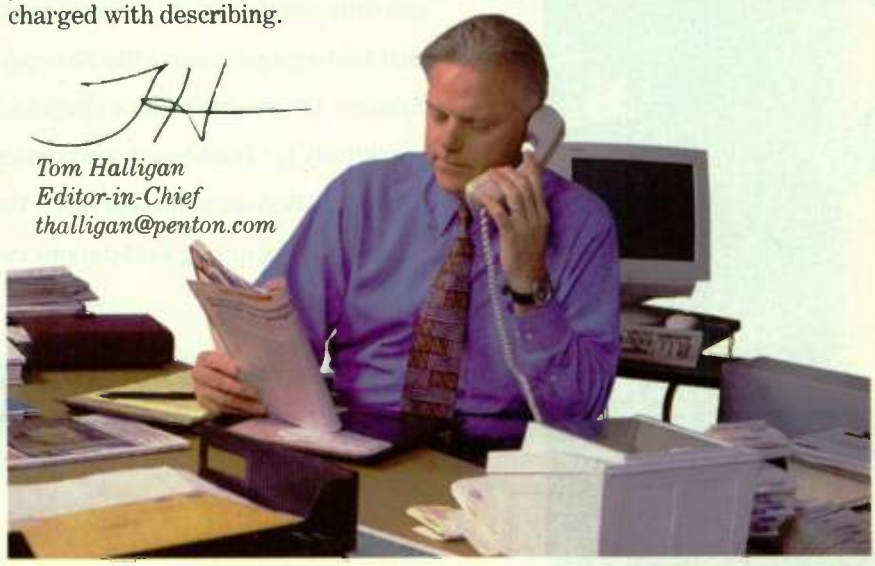
Then we have the new wave of technology magazines that are written by the technohip to a readership who want to be technohip. I coined that name after I read the cover article in the August issue of *UPSIDE* that contained the following words: technoimperialists, technofailures, technoanarchists, technoreactionaries, technoutopians, technojugen, technoabsolutism, and technofascists. (Obviously you can see why I'm in a techno state of mind right now, but I'm hoping it will wear off in a few days).

The article, and articles like it, read as if the writers all double-majored in English and history. It's amazing how many demons these writers can find under the motherboard. This particular article basically warns us that if we don't watch out, a couple of the above technogroups could be the incubator for "building the 1000-year Digital Reich." Scary? Nah. But it was a better August beach read for me than a Stephen King novel.

ELECTRONIC DESIGN and other technical trade magazines stay focused on the technology. That's definitely our mission. You go elsewhere for your general technology news and information—to sources that you trust, which probably coincide with your personal and political views. But, I do wonder if technology is getting a fair shake from the mass media. Is technology being presented fairly, accurately, and objectively? Are those general-interest business and technology writers and commentators doing a decent job?

Overall, I'll give them a C rating. Their main failures are not providing well-thought-out critical analysis, and continuing to go back to the same tired "expert" sources for quotes.

As more high-tech tools creep into our daily lives, I would hope that business and general technology editors and writers will soon go beyond the popular industry analysts' quote machines, and dig deeper to find the technical people who can really help them understand and explain the technologies they are charged with describing.



Tom Halligan
Editor-in-Chief
thalligan@penton.com

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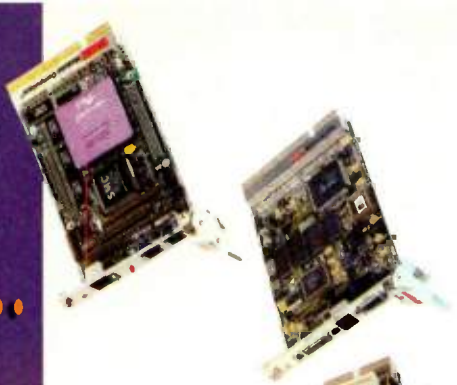
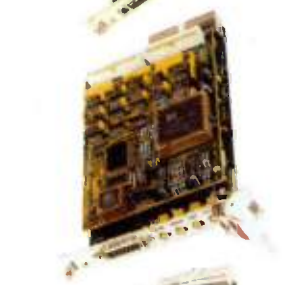
When you need *just* the right CompactPCI solution...





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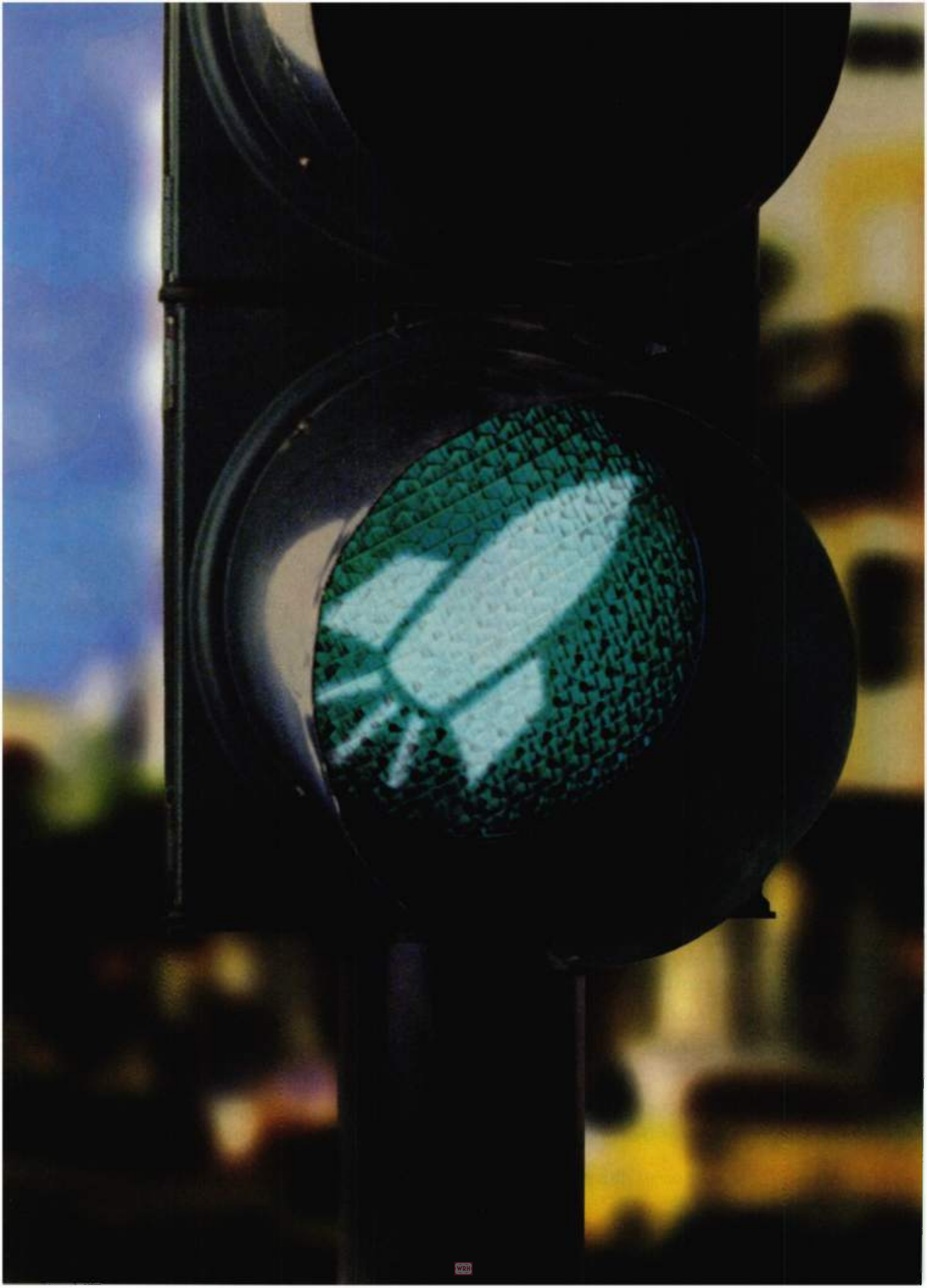

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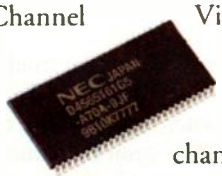
New memory core technology boosts PC graphics performance up to 100%. Without changes in motherboard design.

Microprocessors keep getting faster while memories struggle to keep pace. Most new memory devices provide faster data transfer rates by improving I/O interface. NEC takes a more radical approach. We've redesigned the memory core and introduced a powerful new architecture called Virtual Channel Memory (VC Memory).

The new architecture features flexible, multiple channels with cache SRAM between memory cells and the I/O interface. The channels store prefetched data while the cells perform read and write operations. These innovations result in higher throughput, faster random access and lower latency.



Introducing 64Mb Virtual Channel Synchronous DRAMs

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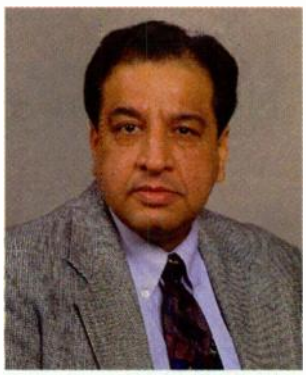
READER SERVICE 181

Integration Trend Builds Steam

Dictated by end systems that must continue to offer more for less, analog and mixed-signal IC manufacturers continue to refine their processes to pack more functions on the same chip. And, this is especially true in digital cellular and personal communications service (PCS) telephones that shrink so rapidly with time. Every new generation offers more features, including smaller housings that fit in a user's palm—without penalizing the battery or the wallet.

This drive is gathering momentum as semiconductor suppliers strive to put system-level solutions on a single die. While the single chip solution is far fetched for now, the level of functional integration rises ever higher. In fact, the most recent trend is to integrate power management and conversion functions on the same analog and mixed-signal chip, and offer such combinations at cost-effective prices.

Until now, the power-supply elements like voltage regulators and dc-dc converters, as well as management and supervisory functions, were always considered on a separate chip. But, with Texas Instruments' development of the LinEPIC-III analog 0.37-µm Leffective CMOS process, that chip landscape is changing. TI is now confident that such power-control functions can be integrated with the analog front-end processing functions on a single die, thereby cutting the number of components in a wireless phone.



ASHOK BINDRA
ANALOG, POWER DEVICES, & DSP

The LinEPIC is an analog/mixed-signal version of TI's digital CMOS process known as Enhanced Performance Implanted CMOS (EPIC). This third-generation technology is a high-performance, analog CMOS process with good parasitic bipolar components. Plus, it features dual gate oxides that allow 3.3-V and 7.0-V transistors on the same die. Other features of the enhanced process include precision poly-poly capacitors, high-value resistors, N+ buried layers, and other processing steps to make such integration feasible. As a result, it has enabled merging of the RF interface, audio codec, speaker drivers, and microphone preamplifier with low-dropout regulators (LDOs), switching regulators, and charging switches. This is currently implemented in custom designs for next-generation cellular terminals. Standard products using the LinEPIC III technology are slated for release sometime next year.

While the technology is cost-effective, smaller, and easier to design, it still maintains the overall system performance. In addition, the user doesn't need to worry about the power issues. Meanwhile, efforts are underway to extend this capability to include small-signal RF functions on the same chip. The result will be one integrated analog chip for the celluar market. Additionally, TI intends to extend this capability to other analog/mixed-signal product lines.

TI is not the only company that sees the significance of integrating power-control functions with analog/mixed-signal devices. In fact, Intel's design engineers embarked upon such integration with the development of multilevel flash memory cells, for example, the StratFlash high-density memory chips unveiled last year. This multibit/cell flash-memory technology required nonstandard voltages to perform accurate program and read operations, forcing designers to implement a dc-dc voltage converter on the same memory chip. While eliminating the need for an external dc-dc converter, the built-in voltage converter allows precise control of the cell voltages required to reliably and reproducibly place precise amounts of charge on the floating gate of the multibit cell.

Other analog/mixed-signal players are reviewing such a path. It won't be long until many others will join the fray. And, a new integration trend will emerge. Maybe some of you are already ahead of the game....

Send your comments on this subject to me at *abindra@penton.com*

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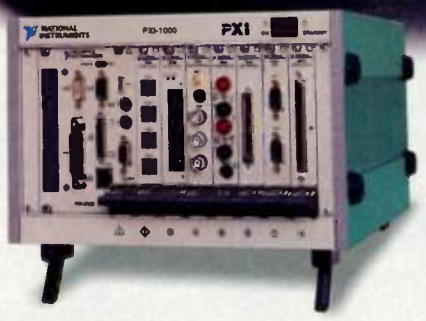

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READER SERVICE 151

Multi-Protocol Serial Interface Transceiver

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SP502	6	7	RS-232 RS-422 RS-485 RS-449 V.35 EIA-530	+5V	6 drivers and 7 receivers, ideal for Wide Area Network interface applications
SP503	7	7	RS-232 RS-422 RS-485 RS-449 V.35 EIA-530	+5V	7 drivers and 7 receivers, supports DTE or DCE applications
SP504	7	7	RS-232 RS-422 RS-485 RS-449 V.35 EIA-530 V.36 EIA-530A	+5V	on-chip switched resistors for simplified V.35 termination, supports DTE or DCE applications
SP505	7	7	RS-232 RS-422 RS-485 RS-449 V.35 EIA-530 V.36 EIA-530A	+5V	single chip multi-protocol serial interface transceiver no external termination resistors.
SP522	2	2	RS-232 RS-422 RS-485 RS-423	+5V, +10V, -10V	low cost multi-protocol transceiver integrated circuit, individual tri-state control
SP524	4	4	RS-232 RS-422 RS-485 RS-423	+5V, +10V, -10V	low cost multi-protocol transceiver integrated circuit, ideal for V.36 applications

Download our easy-to-use multi-protocol designers guide at:
www.sipex.com/dsheets/mpdesmn.pdf

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READER SERVICE 168

OVI Announces HDL Interoperability Standard

Open Verilog International (OVI), Los Gatos, Calif., an EDA industry organization, recently announced its approval of the Verilog HDL synthesis interoperability standard. This OVI standard specifies the RTL and behavioral coding style best suited for synthesis, as well as some of the formal pragmas and directives for new tools. Its foundation consists of a combination of contributions provided by Synopsys, Mountain View, Calif., and California-based Cadence's Synergy semantics and syntax that was used to seed the synthesis interoperability language subset.

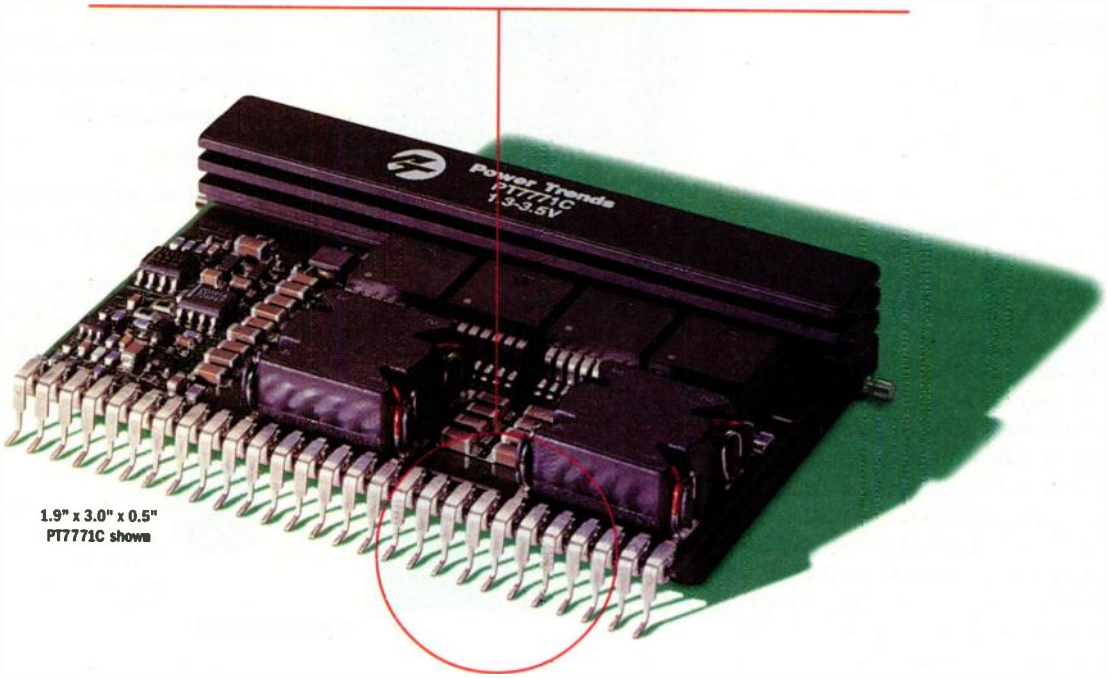
The Verilog HDL interoperability standard ensures consistent results across a broad spectrum of applications when designers reuse designs and intellectual property from other sources. Moreover, it will provide a way to exchange and protect intellectual property. To download a copy of the standard, go to *www.eda.org/vlog-synth*. Additional information on the standard can be obtained by contacting OVI directly at (408) 358-9510; or at *www.ovi.org*. CA

Joint MEMS EDA Development Gets Underway

The MEMS (Microelectromechanical Systems) industry has virtually exploded in recent years driven by many new applications in the areas of consumer, aerospace, and telecommunications, coupled with advances in micromachining technology. To help support this growth, two prime players in the MEMS industry, Mentor Graphics, Wilsonville, Ore., and MEMSCAP, Grenoble, France, have joined forces.

The prime focus of the partnership will be to develop designs tools for MEMS-based systems. Mentor's contribution to this effort will be to leverage its expertise in the area of analog

32 AMPS SURFACE MOUNT



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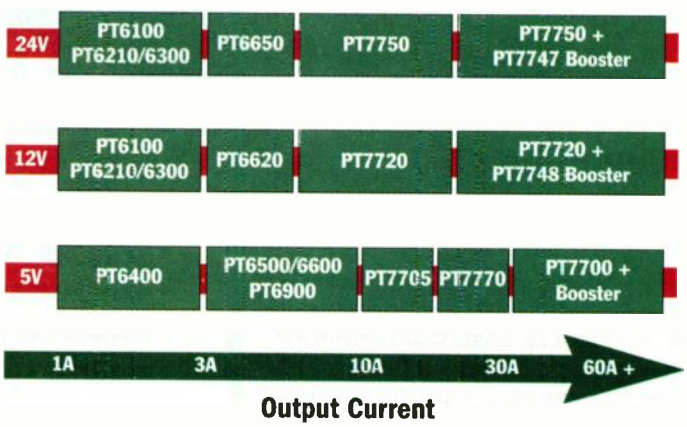

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behavioral modeling through its HDL-ATM analog behavioral language. The language is specifically tuned for multi-domain applications, such as MEMS. MEMSCAP will contribute its expertise as a provider of IP (Intellectual Property) for MEMS.

Under the terms of the partnership, the two companies will work closely with silicon foundries to provide design teams with access to MEMS components, as well as the latest process technology developments. They will develop design-for-manufacture methodologies that will improve yield and performance characteristics around Mentor's Opsim and Aspire yield management tools. In addition, the two companies also will cooperate to provide customers a range of solutions for MEMS design challenges, including the development of MEMS engineering kits that offer designers a mixed-technology MEMS design flow. Check out the *www.mentorg.com* web site. CA

Firms Team Up To Develop Biometric Verification ICs

Keyware Technologies, Boston, Mass., and ST Microelectronics, Milan, Italy, announced an agreement concerning the development of integrated circuits implementing Keyware Technologies' Layered Biometric Verification (LBV) technology. Biometrics is the science of measuring the unique physical characteristics of a person, such as a voice, a face, or a fingerprint. These personal features are analyzed and stored as "bioprints" in a reference database, on a smart card, or an embedded chip. They're used to verify the person's identity by comparing them to the previously stored bioprints.

Keyware Technologies combines several biometric technologies in one control system—called the LBV Security Server—which increases the security and reliability of the system. The system is in charge of the intelligent decision process that combines the different results, thus enhancing the performance of the biometric authentication. User-friendly and non-intrusive layered biometrics help to restrict physical access, verify identity for financial transactions, and control access to information over computer and telephony networks.

ST will implement Keyware's software on a proprietary DSP chip, creating one processor chip for video and one for audio. The voice signal processor chip also will include voice-recognition software based on technology developed by Lernout & Hauspie, Burlington, Mass., licensed to ST in 1997 and employed for car information-system applications.

Contact Keyware Technologies Inc. at (781) 933-1311, ext 230; *www.keywareusa.com*; or ST Microelectronics at +33 4 50 40 25 58; *www.st.com*. JC

GEM Satellite Program Selects Two Partners

Hughes Space and Communications Company (HSC) announced that it has chosen LogicVision and IBM to participate in its Geomobile (GEM) satellite program. Hughes GEM satellites will feature a 12.25-meter deployable reflector, on-board digital signal processing, circuit switching, and digital beam forming. Once launched, the satellites will be able to provide telephony services to users of portable cell-phone-sized handsets.

A crucial part of the communications payload is the GEM's on-orbit reconfigurable digital processor, because it enables the satellites to meet the needs of multiple customers, or adapt to the changing needs of a single customer. The first ASIC design for this digital processor is well over two million gates in size. Unfortunately, with such a high gate count and device complexity, testing the devices becomes difficult.

This is where LogicVision and IBM enter the picture. Hughes will leverage LogicVision's icBISTTM to test the devices, while IBM will exercise its expertise in building and testing reliable, highly complex, multi-million-gate devices to supply the ASICs. To date, LogicVision and IBM have completed the integration of LogicVision's icBISTTM embedded ATE solution into the IBM ASIC design flow for the SA-12 process technology. They also have begun qualifying icBISTTM for customer product-level test of designs using the IBM SA-12 design system.

For more information on the GEM satellite program, contact LogicVision at (408) 453-0146, or go to the web site at *www.logicvision.com*. CA

New Online Privacy Alliance Puts Out Guidelines

IBM, along with approximately 50 other American companies and associations, have banded together to create the Online Privacy Alliance—a cross-industry coalition that will protect the privacy of individuals in cyberspace. As its first official business, the alliance released guidelines for online privacy policies and a set of principles to safeguard the privacy of children.

The guidelines require that alliance members implement a set of privacy policies that address notice and disclosure, choice, data security, data quality and access. The alliance's children policy states that sites intended for children must not collect online contact information from a child under 13 without prior parental consent or without direct parental notification of the nature and intended use of the information.

As part of the alliance's ongoing privacy efforts, it will now focus its attention on plans for an education campaign. The campaign, designed to reach a million businesses to encourage them to adopt alliance policies and practices, will target consumers and seek to teach people how to protect personal data.

The creation of this alliance is significant because it represents the most widespread effort ever undertaken by business to create an online environment that respects privacy. The list of companies and associations are listed at the Online Privacy Alliance web site. For further details, check out IBM's web site at *www.ibm.com* or go to the Online Privacy Alliance web site at *www.privacyalliance.org*. CA

Edited by Roger Engelke

Forum Beefs Up Advanced Graphics Port Spec For Workstation Applications

While the Advanced Graphics Port (AGP) continues to thrive in PCs, it lacks the punch needed for advanced simulation, mechanical CAD, financial modeling, and creation of digital content. Such applications still fall within the realm of advanced graphics workstations. It was with that in mind that Intel and the AGP Forum crafted a workstation-specific extension to the AGP 2.0 specification, called AGP Pro.

Intel recently released the final version of that spec, which had been announced earlier this year. AGP Pro is designed to offer up to four times the electrical power of today's AGP interface specification. It includes an enhanced connector; improved cooling system; form factor specifications, such as graphics card size; and layout specifications to meet the demands of workstation graphics users on both IA-32 and IA-64 platforms. The new specification supports both AGP2X and AGP4X modes.

AGP Pro includes advanced capabilities like high-performance, single- and multiple-image display, integrated video and 3D functionality, and advanced realism.

Higher-Power Operation

At its heart, the purpose of AGP Pro is to deliver added electrical power to graphics add-in cards. The AGP Pro definition includes an extended connector, thermal envelope, mechanical specifications for cards, I/O brackets, and motherboard layout requirements. AGP Pro extends the existing AGP connectors on both ends to deliver additional power on the 12- and 3.3-V rails.

The specification is intended to supplement, not replace, the existing AGP connector set. While ordinary AGP supports both ATX and NLX motherboard form factors, AGP Pro is defined only for ATX form-factor implementations.

An AGP-Pro-compliant system must have two PCI slots adjacent to the AGP Pro connector. The PCI slots will guarantee at least 33-MHz/32-bit operation. As an option, the PCI slots can be used by an AGP Pro card for electrical, mechanical, or PCI functions.

AGP Pro defines two types of cards: high-power (50 to 110 W) and low-power (25 to 50 W). Both versions require sufficient space on the component side to facilitate cooling. Two adjacent PCI slots must be left unoccupied to provide this space. The unused PCI connections provide 2.17 in. of clearance space for the card.

A special three-slot-wide I/O bracket installed on the AGP Pro High-Power card will reserve the use of this space. The spec insists that all retail-channel, High-Power AGP Pro cards use the three-slot bracket. Low-Power AGP Pro cards must use a two-slot-wide bracket.

The AGP Pro connector is designed as an extension to the existing AGP connectors, which are extended on both ends to build the AGP Pro version. It is a monolithic connector.

Any of the specified AGP connectors can be extended to build the AGP Pro connector. This section illustrates the use of the Universal AGP connector to build the AGP Pro connector. The Universal connector can be replaced with 3.3- or 1.5-V AGP connectors to build the AGP Pro.

Power ID Pins

Two-pins are defined specifically for the AGP Pro connector. They're used for two purposes: indicating that an AGP Pro card is physically present in the slot, and providing information on the maximum power requirements of the card plugged into the AGP Pro connector. When providing the power level, the pin strapping must indicate the total maximum power consumption of a fully configured AGP Pro card.

The maximum power consumption may be more than that consumed in the card's shipping configuration, taking into account sockets for memory expansion, for instance. System designers may use these signals for system configuration, diagnostics, or power allocation.

If the signals are used by the motherboard, the system designer must provide pull-up resistors for both of them. Designers can chose the value of the resistor and the pull up voltage based on the associated circuitry.

Details on the AGP Pro interface specification, included as an addendum to the AGP Interface Specification Rev 2.0, can be found at www.agpforum.org. For more information, contact Jane Rauckhorst at Intel, (408) 765-7026; jane.rauckhorst@intel.com.

Jeff Child

Silicon-On-Insulator Technology Boosts Performance In Mass-Produced CMOS ICs

Researchers have apparently found the answer to a 30-year-old question—how to make high-density, silicon-on-insulator (SOI) CMOS circuits in commercial volumes. Using a process called separation by implantation of oxygen (SIMOX), scientists at the IBM Microelectronics Research Division's Advanced Silicon Technology Center, East Fishkill, N.Y., have qualified a 0.22-µm SOI CMOS process. The team is now in the early stages of developing a 0.15-µm technology.

According to Aiden Kelly, IBM's manager of custom logic design services in Europe, a number of microprocessor and SRAM ICs have been qualified, and will be debuting in IBM AS/400, S/390, and RS/6000 servers soon. Kelly says that SOI options will be offered in IBM Microelectronics' merchant catalog of standard parts before the year end. He notes that the effect on prices will be marginal, because the new process stage increases costs by less than 10% at the wafer level. Yields, he says, are unaffected.

The SIMOX process involves implantation of very heavy doses of oxygen followed by annealing at high temperatures, until a thin layer of silicon-dioxide film is formed. The result is a complete wafer with a thin layer of N++ silicon separated from the substrate by a defect-free ultra-flat layer of oxide *(Fig. 1)*.

The wafer can then be processed conventionally through standard

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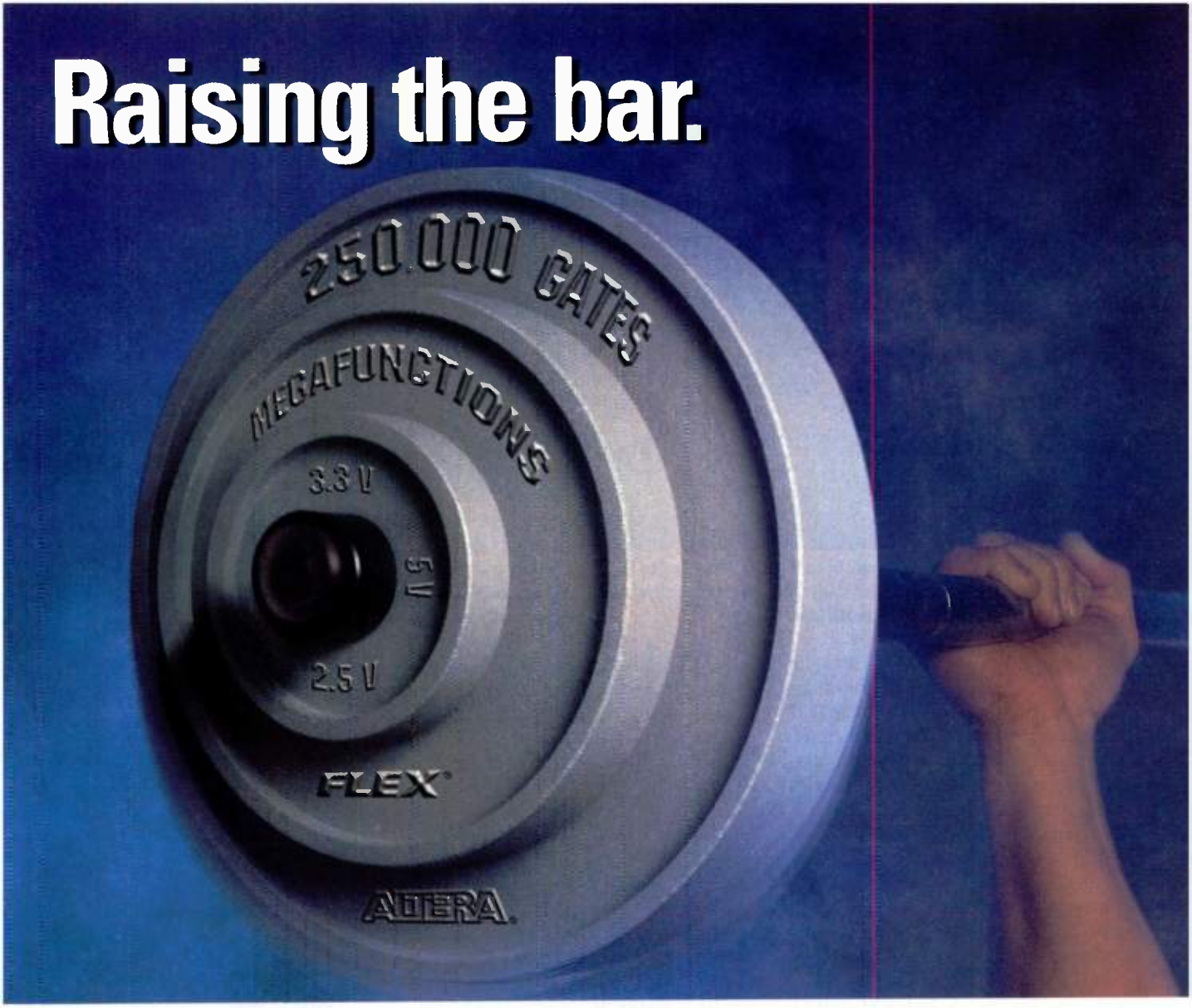

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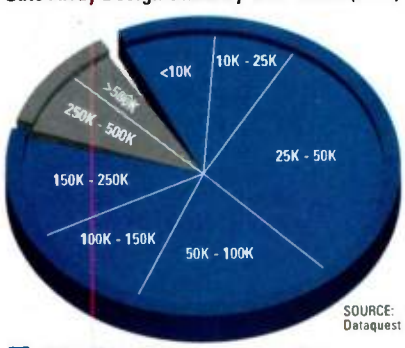
Gate Array Design Starts by Gate Count (1997)



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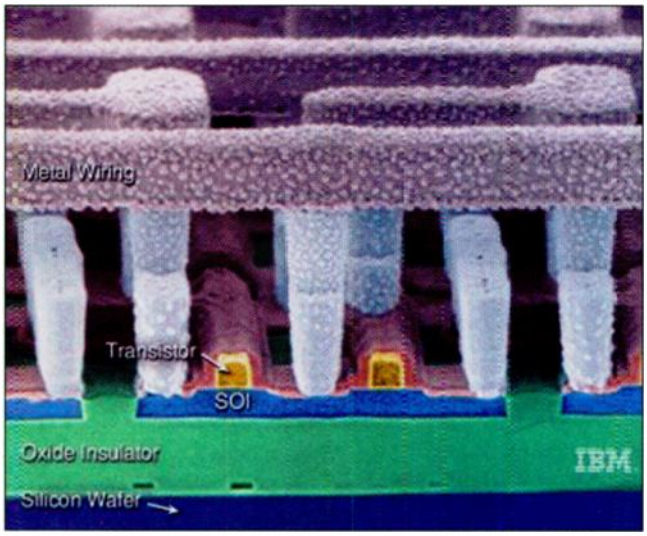
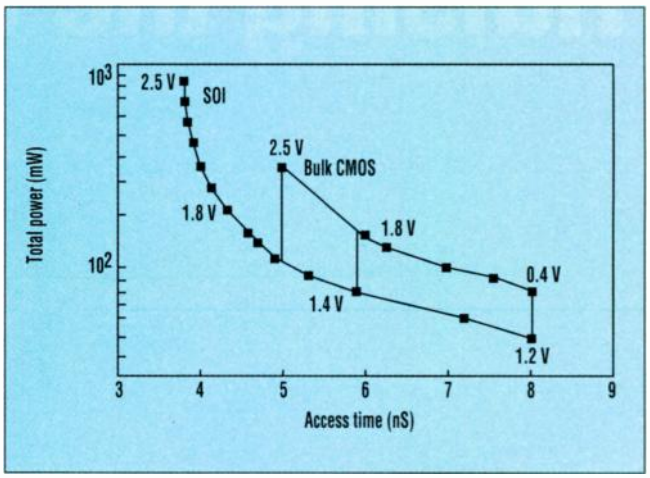


1. This cross-section photomicrograph of an IBM device built using the newly developed silicon-on-insulator (SOI) CMOS technology shows the relationship of the transistors to the SOI layer.



2. Silicon-on-insulator CMOS devices can use lower voltages than standard CMOS circuits without degrading performance. That gives them an advantage in handheld systems. For example, these measured results show that a 4-Mbit SRAM made with the SOI process consumes significantly less power for similar access speeds.

CMOS production cycles. Because implantation of the insulating layer takes place during wafer preparation "offline," it can be applied retrospectively to all IBM Microelectronics' standard CMOS product ranges, and added to all the company's wafer fab lines.

The result is a 25% to 35% increase in performance in terms of cycle time, and up to 35% better high-frequency performance than equivalent bulk CMOS devices. This boost derives from the elimination of area junction capacitance and "body effect." In conventional CMOS circuits, this results in lower current and reduced performance in MOS transistors, if they are stacked or if their source electrodes are not grounded.

In addition to higher speeds, the SOI-based devices offer the prospect of better low-power options for handheld equipment. The reason is that compared with standard CMOS circuits, lower voltages can be used in SOI CMOS without degrading performance. As an example, Kelly cites the case of a 4-Mbit SRAM made with the SOI technique. Compared with a standard CMOS device, IBM engineers say they measured a significant reduction in power consumption for a similar access speed *(Fig. 2)*.

Other benefits claimed include a significant reduction in "soft error" rates. These are errors caused by the impact of cosmic rays, and background radioactivity upsetting data held in memory. As device geometries get smaller and operating voltages ever lower, these effects become more significant. In fact, interest in SOI technology was first developed as a way to harden silicon devices against radiation for space applications.

Peter Fletcher

Hot-Plug, Limited Bus-Mastering Retry Time Highlight PCI Version 2.2 Specification

Now finished with a 30-day member review, version 2.2 of the Peripheral Component Interconnect (PCI) specification is ready for prime time. The latest version of the PCI standard includes the new functionality of PCI Hot-Plug and PCI Power Management, in addition to a roll-up of engineering change notices (ECNs) and errata since version 2.1 was completed in 1995 *(see the table)*. While the latest update is essentially a "clarification release" of the spec, a number of recent additions may have interesting implications for multimedia and interrupt handling.

The major elements of PCI version 2.2—PCI Hot-Plug and PCI Power Management—have been in the works since last fall, and contain no major surprises. The former allows users to insert and remove PCI adapter cards without shutting down the system. The latter addresses the issues of power management and energy conservation on the PCI bus. Warren Questo, chair of the of the PCI Special Interest Group (SIG) reports that the comments received during the member review period involved mostly minor issues on mechanical concerns and, in fact, were primarily requests for clarifications.

Two of the more recent additions to version 2.2 include a maximum retry time for bus-mastering requests, and support for message-signaled interrupts. The only major point on which there was significant comment was on maximum retry time, which prevents any device on a PCI bus from monopolizing it. While several device classes have been guilty of that, graphics boards were the worst offenders. There had been some worry among graphics vendors that a limit on retry would hurt performance benchmarks of their products.

Avoids Data Losses

Because PCI supports bus mastering, any device can become a master on the bus at any time. To do so, a device has to get the attention of the controller (the Northbridge part of a PC chip set.) Without a limit on the retry time, a device can keep trying until an overhead loop occurs, and buffers must handle the data build up. Be-

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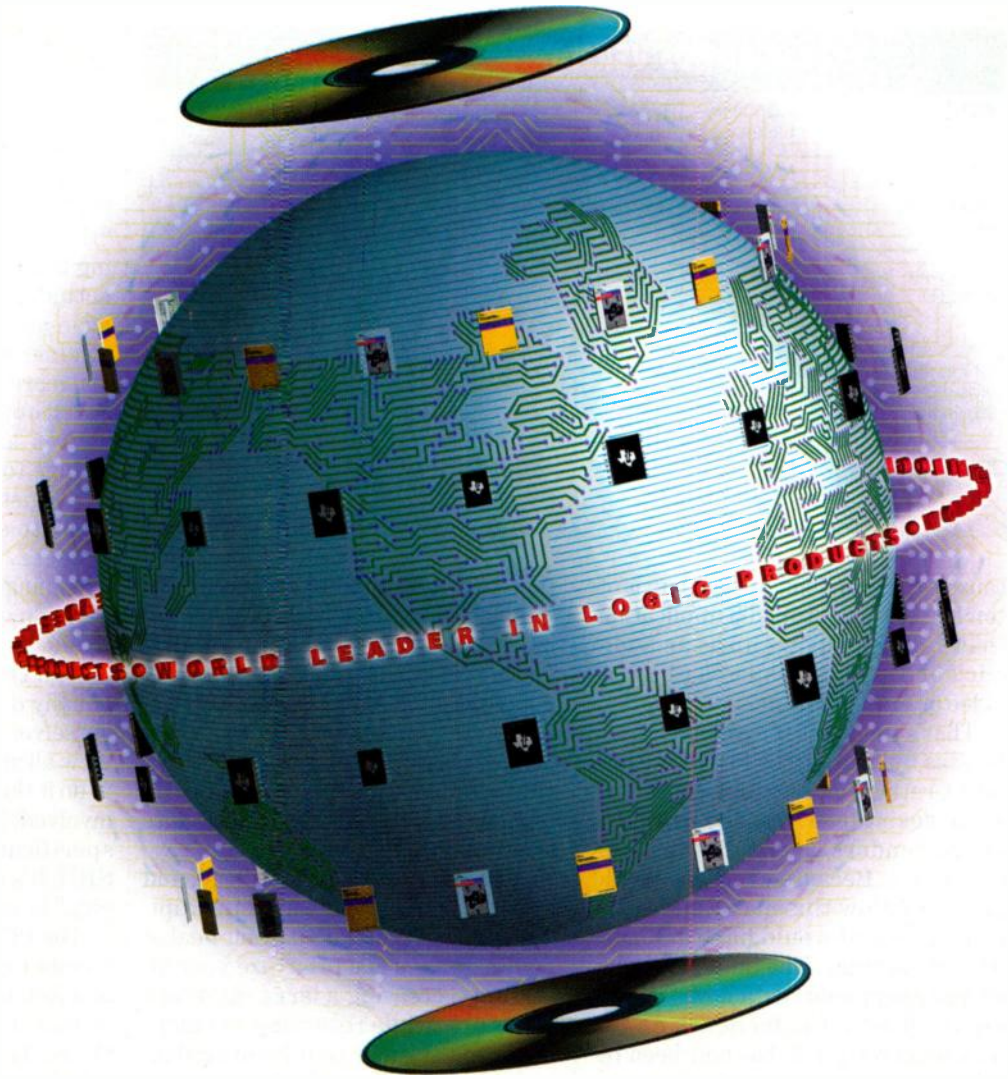

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TEXAS INSTRUMENTS

PCI LOCAL BUS VERSION 2.2 MAJOR ECNs

ECN	Software change	Type of change	Required/ Optional	Description
Subvendor ID	X	Enhancement	Required	Subvendor configuration space.
Maximum retry time		Enhancement	Required	Devices cannot retry request for longer than 10 μs.
Message-signaled interrupts	X	Enhancement	Optional	Method for I/O controllers to send message-based interrupt signals.
3.3-V auxiliary signal (PCI Power Management)		Enhancement	Optional	Assigns reserved pin as 3.3-V auxiliary supply for wake-event logic.
PCI Hot-Plug	X	Enhancement	Optional	Ability to insert and remove PCI adapter cards without shutting down the system.

cause buffers are only so big, data is often lost. In a multimedia application, that data loss shows up as an audio click or a pop, and missing bars of video or graphics frames.

That's the problem version 2.2 addresses by limiting the bus master request retry time. At first there was some resistance, but the graphics board vendors warmed to the idea eventually. Because everyone would have to follow this maximum retry rule, no board would have a benchmark advantage. The limit also helps ensure isochronous data flow. According to Questo, the feedback on the maximum retry rule has now been resolved to everyone's satisfaction.

In general, PCI issues are becoming less relevant for vendors of graphics boards anyway. Just about all of the graphics chip and board makers are migrating to the Accelerated Graphics Port (AGP) which is faster that PCI. Unlike PCI, AGP is a point-to-point link, and has all the built-in structure to handle high-performance graphics operations.

We Interrupt This Message

Another recent addition to the PCI 2.2 spec is message-signaled interrupts (MSI). By getting around PCI's limited interrupt capacities, MSI may have important implications for both high-end and low-end system designs. MSI adds to the PCI spec a scheme for doing message-based interrupts.

PCI supports 12 usable interrupts, which are routable on only four PCI bus signals. The interrupt controller can share interrupt pins. This limitation hasn't been a problem for most PC systems because most hosts only need interrupts for four card slots. MSI lets you add interrupts, not in hardware, but with software messaging. The system posts an interrupt message to the host, and the host services that interrupt when it gets the message. The number of message-based interrupts is virtually unlimited.

MSI requires more overhead, and isn't as fast as a hardware interrupt, but it gives designers a great deal of flexibility. You can prioritize your interrupts, creating a large interrupt structure, while reserving the more important stuff for your hardwired interrupts. This is particularly important for PCI bridge operations.

MSI also lets designers reduce costs by opting to eliminate a hardware interrupt scheme altogether. Using MSI you can create a pathway for interrupts via software, and save $2 or $3 on interrupt-control silicon. Such savings aren't trivial in the multimillion-unit desktop PC business.

PCI Spec Matures

According to Questo, the success of the PCI bus is reaching a new plateau. "Even though the spec itself is starting to reach its change maturity, the actual applications of the PCI bus have not reached maturity," he says. "In fact we see it moving into more and more areas [beyond the PC]."

Although the PCI SIG actually writes an ECN for every major change to the specification, the difficult logistics require the official revisions to encompass a collection of changes. "It would have been overwhelming in logistics to do a complete revision of the document every time we did an ECN," says Questo.

"On the other hand, it would be equally difficult if we held them all to ourselves and released the spec for review all at once. It takes a little longer to do it this way, but it keeps everyone involved. That's key because it is their specification [the members of PCI SIG]. It's an open-developers community," he says.

The PCI SIG now includes over 800 member companies worldwide, each of which is entitled to see the changes to the spec and offer feedback on them. This number is up from 600 members in 1996.

For more information, contact PCI SIG at (800) 433-5177 (within the U.S.), fax the group at (503) 693-8344, or visit the PCI SIG web site at www.pcisig.com.

Jeff Child

Lone-Transistor Memory Cells Deliver SRAM-Like Speed With DRAM-Like Density

When it comes to selecting which type of memory to use, most designers follow a basic premise: For speed and ease of use, choose static RAMs; for density, use dynamic RAMs. Now, designers at Mosys Inc., Sunnyvale, Calif., have found a way to combine the best features of each. The technique they developed will be used in several new families of memory chips that function just like SRAMs, but employ the very dense, single-transistor memory cells found in DRAMs. Over the years, designers at various companies developed pseudostatic RAMs, as well as several other self-refreshing DRAMs. But, such memories performed no better than standard, slow DRAMs.

The novel 1-T SRAM structure developed by Mosys changes that. By delivering memory chips that offer random read or write cycle times of less than 10 ns, such memories can op-

erate in systems with CPU bus speeds of up to 133 MHz. Even faster versions, with external access times of less than 5 ns, are in development.

The technology is basically a superset of the MCache technology unveiled by the company a few years ago. But, it eliminates the shortcomings of that technology—the most critical of which was the "transparency" issue. The new chips can function just like SRAMs. And, unlike MCache chips, they require no changes to any control signals. Designers just drop them into the same system without changing anything surrounding the memory.

At the heart of the 1-T SRAM is, of course, the single-transistor/single capacitor DRAM memory cell. In contrast to the four- or six-transistor SRAM cells, these allow at least a five- to 15-fold reduction in area and a four-fold increase in density.

Outside the 1-T memory array, however, is where Mosys designers work their magic. They developed an improved version of their multibank memory architecture, which employs a fast charge-sensing technology and various patented circuit approaches. As a result, logic on the memory chip manages the internal refresh of the memory cells totally transparently. This architecture exacts no system overhead penalty in access time or other performance-critical parameters. In fact, the first implementations will be a family of pipeline burst cache memories. They can drop directly into the sockets now occupied by the full SRAM-based chips.

The fast charge-sensing scheme eliminates dc power consumption in the memory sense amplifiers, while offering fast access to the data. Thus, the scheme reduces memory power consumption. In addition, the multibank memory architecture permits the company to implement dynamic power management. Because only a small portion of the memory array must be active during an access cycle, overall chip power also is lessened. Furthermore, the small memory array size provided by the 1-T cells means shorter wire lengths, which reduces the overall parasitic capacitance and resistance. Since signal propagation delays are shorter, that decreases the power losses due to signal switching and improves the memory's overall performance.

Thus, the combination of the small cell and innovative circuit techniques allows the 1-T SRAM to achieve very low operating power levels compared to similar capacity and performance SRAMs. For a 64-kword-by-64-bit, pipeline-burst cache memory implemented with the technology, Mosys estimates that the chip power consumption is only about 10% to 20% that of the equivalent SRAM version. The chip area is only about 25% that of the SRAM, which lowers the manufacturing cost. Furthermore, the lower power levels consumed by the chips reduces the heat that must be dissipated, and that improves the long-term reliability of both the chips and the system.

For more information, check out www.mosys.com.

Dave Bursky

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ELECTRONIC DESIGN QUICK LOOK

Edited by Debra Schiff and Nancy Konish

MARKET FACTS

Video Game Giants Are Neck And Neck For The Profit

Most of us have seen those silly commercials featuring people dressed up like characters from popular video games. Or, we've been visually inundated with fast-moving, flashy action scenes from the games themselves. The commercials are so prevalent and the products are so well known, they've become part of our pop culture vocabulary. Find one person who doesn't see the word "PlayStation" and automatically hear it pronounced by that computerized-sounding voice. The point is, why this huge resurgence in video game advertising? Basically, because the video game market is thriving. And, as DFC Intelligence explains in their annual report, "The U.S. Market for Video Games and Interactive Electronic Entertainment," this is a market that's going to keep on growing. It's sure seen its ups and downs, especially thinking back to those old Atari games. Those lost their appeal, and Nintendo came along as the next major player. The market settled again, but then began rebuilding in 1997. Now, Nintendo and Sony PlayStation are the two major players competing for the market. With video games, once a product or brand becomes established as the one most commonly bought and owned, it's easy to increase profits by creating new games and other side products. David Cole, DFC Intelligence president, sees 1997 as the year in which the Nintendo 64 and Sony PlayStation both set down those roots, establishing themselves in homes across America. U.S. sales rose 26% that year, which brought them up to $6.66 billion. Out of this growth, there was a 40% rise in video game software. PC games shot up 20%. So, it looks like Sony and Nintendo are basically neck and neck for these profits and the market share. Differences do exist, however, because each company has cornered their own segment of the market. The Sony PlayStation generally reaches an audience 14 and older, while the Nintendo 64 is favored by a younger crowd. One question that has arisen is whether Nintendo's growing focus on sports games and role-playing games can help boost its market share in the older segment. Those types of games usually attract more teens and adults. If that indeed happens, Nintendo may pull ahead of Sony PlayStation in both revenues and market share. The race is on because there is more money to be made. This year is predicted to finish up with continued growth. Video game software should see another 40% increase in sales, as PC games are expected to hold steady with another 20% rise. Predictions say profits will then peak in 1999. The DFC post-1999 forecast looks a little unstable. Since Sony PlayStation has gained somewhat of a lead, the initial belief is that it will keep that position, selling more than 14 million hardware units by the end of 1998. But, with 11 million hardware units predicted for that same year, Nintendo 64 isn't lagging far behind. And, as previously mentioned, if Nintendo 64 keeps nosing into Sony's market, it might not be Nintendo that's losing ground. But, all this might be for naught because by late 1999, consumers will probably be itching for the next new thing. And, there'll be someone there to give it to them. Sega's cooking up a new system, and there's even rumor of a successor to the Sony PlayStation. If the Sega turns out to be the new, most sought-after video game hardware system, Sony and Nintendo might be put out to pasture. Or, they'll keep their pace into the year 2000 and even 2001. Whatever the outcome, the market is expected to keep its steady growth, reaching sales of $2.5 billion by 2001. Beyond 2001, there is concern over whether the industry will once again suffer a recession as it makes the transition to another new game system. It's too early in the race to tell, but be sure to keep an eye on it. It'll probably be a photo finish.

To obtain the market review and forecast, contact DFC Intelligence, P.O. Box 720673, San Diego, CA 92172; (619) 484-5145; fax (619) 484-0819; or visit their web site at www.dfcint.com.—**NK**

40 YEARS AGO IN ELECTRONIC DESIGN

Computer Simulation Speeds TV, Speech Research

Use of general purpose digital computers in the simulation of new coding and transmission devices shows promise of accelerating and broadening speech and television research, according to scientists at Bell Telephone Laboratories.

In speech research, speech is sampled; each sample is quantized into 10 bits or 1024 amplitude levels, and delivered to a magnetic tape recorder. These coded samples are recorded in seven parallel tracks, with 200 characters to an inch of tape. These tapes are fed into the computer, and the processed signals are then re-recorded, decoded and played back for analysis and listener evaluation.

Computer memory requirements for speech processing are severe, due to the large amount of data generated by even a short section of speech. A speech transmission scheme, known as the "Extremal" method, illustrates the advantages of this new technique. In its simplest form, only the extremes, or peaks and valleys, of a speech wave are sampled. The amplitudes and time of occurrence of these points are then transmitted, instead of using detailed representation of the entire wave. At the receiver, an approximation of the speech wave is generated by interpolating a suitable mathematical function between these points. Listener evaluation of the simulated speech showed that intelligibility is high—above 90 percent sentence intelligibility—but the quality is somewhat below that of commercial telephones.

Picture coding research has also been carried on by computer simulation. In order to hold machine time and memory requirements to a reasonable level, the system uses an input picture of 100 x 100 elements, corresponding to an area about 1/25 that of a conventional TV frame.

A magnetic tape recording of the video signal is prepared by scanning a square picture with 100 scanning lines in 2.4 seconds. Each picture dot is quantized to 10-bit accuracy, and recorded in the same form as the speech samples. *(ELECTRONIC DESIGN, September 17, 1958, p. 5)*

Bell Labs was the early leader in coding techniques to reduce data transmission requirements. This article also describes "predictive quantizing," coding for TV transmissions.—Steve Scrupski

All Quiet on Any Front With New Army Headphone

Development of an experimental electronic earphone, which shuts out loud noises that interfere with combat communications, was announced by the Department of the Army. The artificial quiet is created by adding more noise with a miniature microphone in the earpiece to create a second noise, just as loud, but opposite in phase. This phase opposition greatly reduces the noise level. The earphones, which are expected to also have many commercial uses, resulted from early noise reduction experiments at RCA, Camden, N.J. Application of the concept of earphones was conceived at the U.S. Army Signal Engineering Laboratories, Fort Monmouth, N.J. *(ELECTRONIC DESIGN, September 17, 1958, p. 12)*

Noise-cancellation techniques now are rather common, but it's interesting to see that the idea was being put into practice 40 years ago.—Steve Scrupski

Steve Scrupski is a former Editor-in-Chief of ELECTRONIC DESIGN. Now semi-retired, he can be reached at scrupski@worldnet.att.net.

@IEEE

Consultants, this one's for you. On October 17 of this year, the IEEE-USA National Consulting Workshop will take over Schaumburg, Ill. Because it's the 10th annual conference, this one's expected to pack a special punch.

The all-day workshop, running from 8:30 a.m. to 4:00 p.m., is geared toward consultants practicing in the electrotechnology and information-technology fields. Topics will cover some practical how-to's for those aspiring consultants out there, such as getting started in consulting.

Survival tips for juggling full-time employment with part-time consulting also will be thrown around, along with pointers on finding clients. Ways to network more effectively and beef up the referrals are some other planned highlights.

Specialists on hand will explain the financial aspects of self-employment, spotlighting specific issues like setting fees and paying taxes. On the other end of the spectrum, a perspective on 30 years spent in consulting will cover the highs and lows, as well as how electronics and the consulting profession evolved with the times.

For hot topics, there's the changing consulting arena and the Internet. The World Wide Web transforms everything from jobs and companies to the general work life. Another burning topic—Intellectual Property—is passed around a lot in industry speak. Yet, it signifies something different for everyone. Most importantly, it's changing the way companies do business in real ways. Consultants need to arm themselves with knowledge about these topics so they can bring their clients through this transition and into the technical information age.

To register, send a check (payable to IEEE) or credit card information, along with IEEE member number, to Dr. Gary L. Blank, P.O. Box 70155, Plato Center, IL 60170; fax (847) 464-4081; e-mail: g.l.blank@ieee.org. Registration costs $65 for IEEE members, and $75 for nonmembers. For registrations received by October 9, there's a $10 discount.—**NK**

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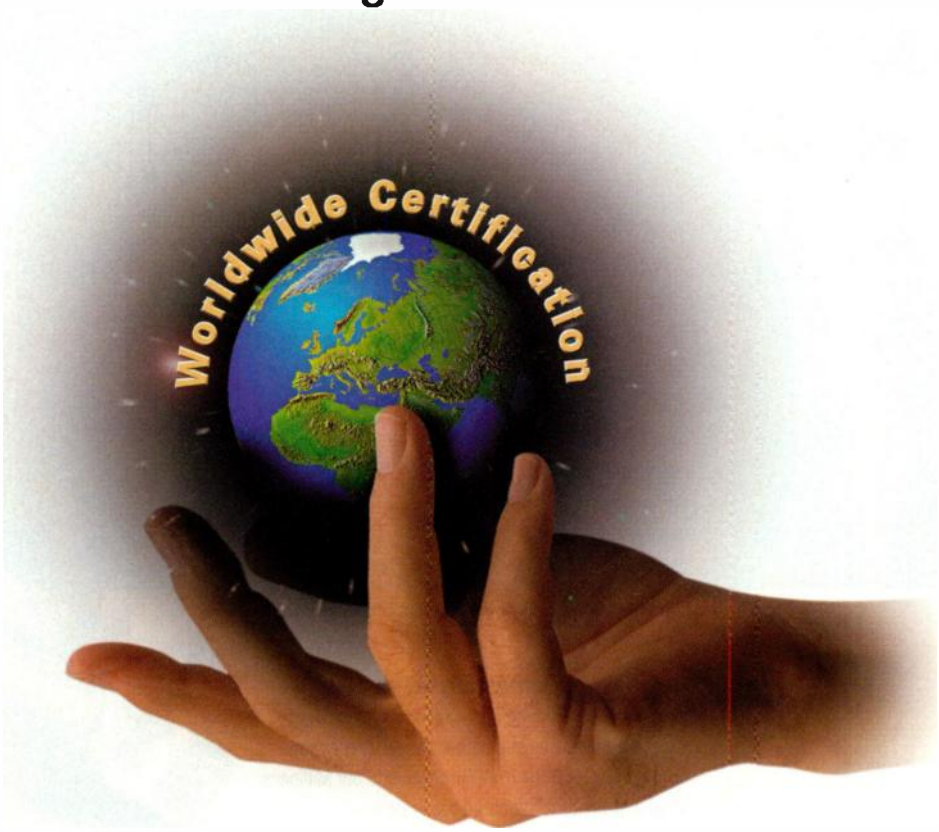

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Holland	prTBR-21	Certifiable under TBR-21
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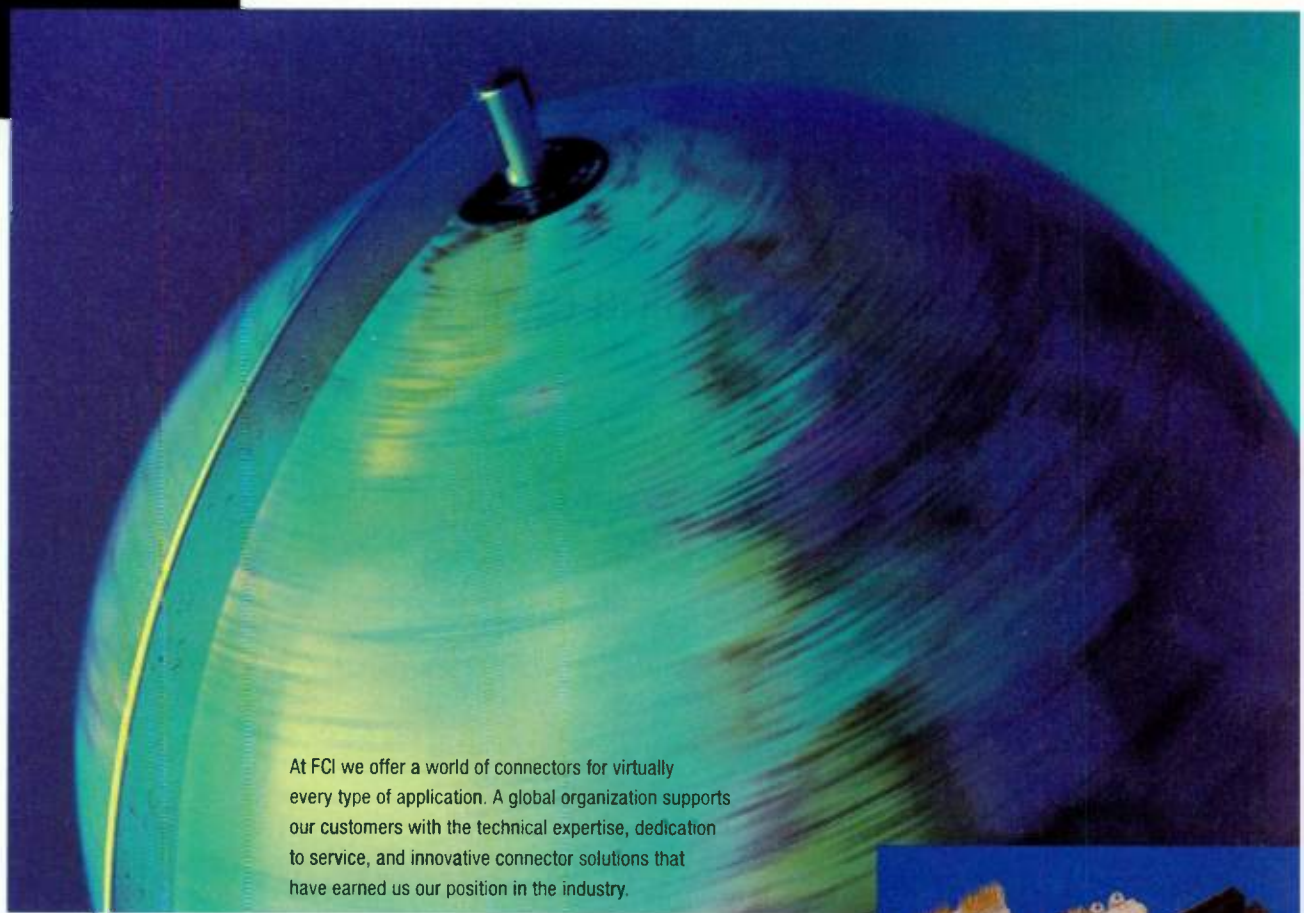

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MANAGING THE DESIGN FACTORY

Attack Of The Space Police

DON REINERTSEN

Many strange tales are told late at night, in engineering departments, by the eerie glow of cathode-ray tubes, but none so strange as those of the Space Police. These entities of superhuman strength are capable of making partitions move to distant corners of the building, and arranging chairs and tables in strange geometrical patterns, reminiscent of the mysterious crop circles in English cornfields. Many years ago, a project manager at a large telecommunications company related such a tale to me. It still gives me chills to think of it.

"We had just started a project with a large team. I had a standard office with a desk and chair. As team leader, I thought it'd be useful to have a table and chairs in my office, so that I could meet with other team members. Being naive and resourceful, we found an unused table out in no-man's land, and moved it into my office. It worked fine."

"The next morning, we discovered our work had mysteriously come undone. As if responding to an unknown power, the table and chairs had moved back to their original spot. Searching for a natural explanation, we assumed it was an overly zealous cleaning crew. Little did we realize that something far more powerful was at work."

"Being engineers, we were not unaccustomed to things going awry on our first try, so we moved the table and chairs back again. We left special instructions in several languages. 'No mueva la mesa! Don't move the table!'"

"The following day, we returned to discover that our work had been undone again. It was starting to get spooky. We found a mysterious note on the table this time. It looked like a corporate form, but not one that anybody had ever seen before—a Furniture Anomaly Reporting Ticket. The form said that it was a violation of corporate rules to have a large square table in the office of a team leader. Such tables were only for common meeting areas. The 'second violation' box was ominously checked. Large red letters warned that a third violation would trigger the 'SEVEREST' consequences."

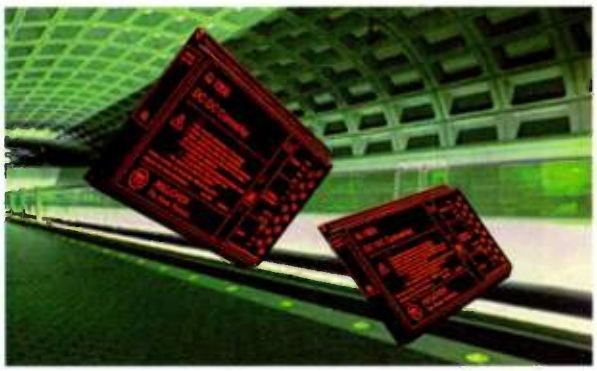
"At first discouraged, we later realized that it's wisely said that every problem contains the seeds of its own solution. We found a *round* table and moved it into my office. The Space Police had no instructions for round tables, so the table stayed there that night, and for the rest of the project."

"What did we learn from this? It's hard to put such a profound experience into words. We didn't try to beat the Space Police with raw power; that would have been suicide. Instead, we discovered that their enormous power was not matched with an equally enormous intelligence, and this proved to be their weak spot. If you can't wear them out, at least you can outsmart them."

Some of you may not have been around long enough to encounter the Space Police. Do not assume that they can't exist. Instead, try a simple experiment. Before you go on your next vacation, align your partitions at a 45° angle from those of your neighbors. Then, wait and see.

Forces far more powerful than you can imagine are at work ensuring that all partitions on the planet Earth run North-South and East-West. If they did not, the very fabric of the universe might come unraveled, with consequences we could only imagine.

Don Reinertsen is president of Reinertsen & Associates, a consulting firm specializing in product development management. He can be reached at (310) 373-5332 or e-mail: DonReinertsen@compuserve.com.



Melcher's 100 W DC-DC sets new standard for railway industry.

Melcher is already the world leader in the provision of power supplies for use in trackside and railborne applications, we have established de facto standards in the industry with the M, K and S families of DC-DC converters. Now we are establishing a new lead with the Q- family of DC-DC Converters which are compliant with the latest harmonized European railway standard EN 50155 as well as the EMC directive. Featuring five different input voltage ranges from 14.4 to 168 V DC the units are suited to 24, 36, 48, 72 and 110 V DC traction batteries, and offer 100 W from a 3U x 4 TE x 160mm extruded aluminum case, free air rated to 71°C without derating. When operated to 50°C the output power increases to a maximum 144 W.

The ultra-slim profile of 20 mm is achieved by the use of a planar transformer, together with hybrid control circuits and a conversion efficiency of up to 90% to minimise losses and heatsinking. Single and dual output modules are available providing 5 to 48 V, or ±5 to ±24 V DC rails with external adjustment possibility in the range from 50 to 110% of $U_{o\,nom}$. Safety isolation levels are according to EN 60950 with approvals from UL and LGA. RFI performance is below EN 55011/22 level B, and transient susceptibility is according to specifications IEC/EN 61000-4-2, -3, -4 and -5.

4 W DC-DC Uses Planar Technology.

Melcher has released a new family of 4 watt DC-DC converters which set new standards for performance within a 24 pin DIL package. Designated IMX 4 series, the products feature a unique single substrate planar magnetic construction, with all components in SMD format mounted directly to a single multi-layer PCB which also forms the main isolating transformer.

This construction together with a high conversion efficiency of typically 82% has enabled Melcher to increase output power from the industry standard 3 W to 4 W, which reduces the profile to just 8.5 mm. At the same time, Melcher has increased the input voltage range to a very wide 4 :1 ratio, with a choice of either 8.4...36 V DC, 16.8...75 V DC or 40...121 V DC to suit 12, 24, 36, 48 and 72 V DC nominal systems. Available with single and dual outputs from 3.3 V DC to 24 V DC, the units are no load and short-circuit proof, and are fully rated over the ambient temperature range -25...71°C. An extended temperature range version of -40... 85°C is also available as an option. Isolation voltage is a standard 1500 V DC. The units offer excellent electrical immunity, complying with IEC/EN 61000-4-2, -3, -4, -5, and -6, and are UL, cUL, and LGA approved to IEC/EN 60950.

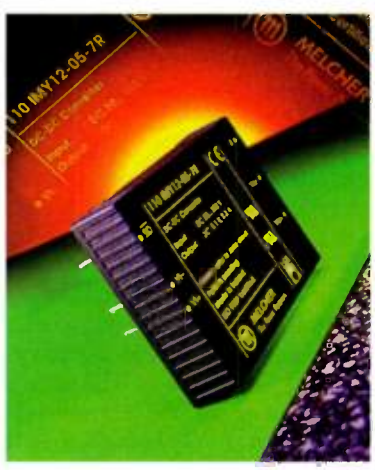
New Databook introduces 35 new products.

Melcher has introduced a new 1100 page databook which details many new lines of innovative AC-DC and DC-DC converters. The databook is also an invaluable reference on standards in the power supply industry.

Melcher manufactures more than 70 families of products, and are one of Europe's leading manufacturers for telecoms, industrial, transportation and military applications.

The databook is available in CD-ROM format. Data can also be downloaded from Melcher's website: www.melcher-power.com

NEW 12/15 W DC-DCs In 2" x 1.5" Package



Melcher has introduced two new ranges of 12 W and 15 W DC-DC converters featuring the latest single substrate planar construction. It offers unparalleled levels of performance in a compact case measuring 51 mm x 40.6 mm with a profile of just 10.5 mm. The IMX- and IMY-families are suited to "Rugged" grade applications and offers up to 17 W of output power from ultra-wide input ranges of 8.4...36 V DC, 16.8...75 V DC and 50...150 V DC. The IMS 15-family provides 17 W output power from input ranges of 14...36 V DC and 36...75 V DC and is suited to "Industrial" grade applications. Both families offer single and dual outputs from 3.3 V DC to 24 V DC and are fully rated over the temperature range -25...71°C. The IMX and IMY units are also available with an extended temperature range of -40...85°C.

Food For Thought

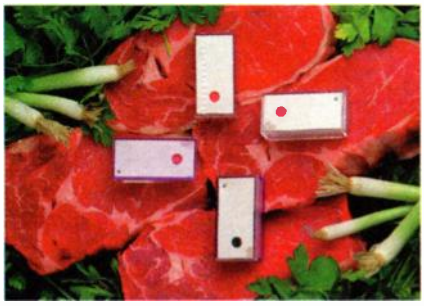
We've all heard the news about unsafe meat-handling practices and the potentially disastrous effects of eating improperly cooked meat. But, who's given thought to the transportation of frozen meat products? If food thaws on the delivery truck and is then refrozen, you wouldn't be able to tell it wasn't fit to eat. You might even purchase it.

Unfortunately, it seems that for most consumers, getting good, safe meat is strictly luck of the draw. But what if there was a way to stack the odds in our favor? Thanks to David Martinez, manager at Sandia National Laboratories, Albuquerque, N.M., and Mo Shahinpoor, engineering professor at the University of New Mexico, we may now have an option. With a little help from the electronics industry, they've developed a simple, low-cost, refrozen food detector that determines when food is not fit to eat.

This innovative invention is a by-product of a solar research project at Sandia. According to codeveloper David Martinez, it depends on an inexpensive "smart" material—a thin wire that "remembers multiple shapes and acts as a sensor." The wire is about the size of a piece of thread and less than 3/8 in. long. It can easily be mass produced using conventional manufacturing processes. Costing just a few pennies for the raw materials, the refrozen food detector is also a very cost-effective solution.

The detector does not require a power source to operate, other than warming and cooling. As the wire's temperature rises above 32° F—the point above which harmful bacteria multiply—the shape of the wire changes. The wire moves, tearing a green-colored piece of paper and revealing a red piece underneath. If the wire's temperature drops below freezing again, the wire returns to its prior position, but the color does not change because the paper has already torn. As a result, the red warning color constantly remains visible.

This detector can easily be placed with meat or any other frozen product during transport. If the product has begun to spoil in any way due to temperature change, the handler will



know simply by checking the indicator's color.

While the device itself is quite simplistic, its potential should not be underestimated. It could save the consumer from suffering everything from a mild bout of food poisoning to perhaps even death. Spoiled food is believed to cause a large number of unexplained illnesses each year.

To date, eight preliminary designs have been developed and patented by the detector's codevelopers. Each design has the smart-material sensor as its key component, and works by exposing a color-coded paper. The smart material used in the designs is nitinol—a combination of nickel and titanium.

The thaw indicator sensor is not yet commercially available. It is, however, being looked at by the New Mexico-based Waste Education and Research Consortium (WERC)—a consortium interested in commercializing certain technologies concerning food safety. Talks are now underway between WERC, the U.S. Department of Agriculture, and the U.S. Food and Drug Administration.

As Martinez explains, "When there's pressure from Washington on food processors, transporters, and displayers to protect consumers against spoiled food, we have a technology patented to do just that." Until then, what's the best low-tech solution to this problem? Keep handling your meat or other frozen food properly. More than anything, cook it well.

For more information on this detector, contact Sandia National Laboratories at (505) 844-8066 or check out its web site at www.sandia.gov.

Cheryl Ajluni

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TRUDEL TO FORM

Doesn't the need to couple new products with corporate strategy infer that product development is a corporate responsibility, not just an engineering issue? I think so. The trick is to develop a continuous flow of compelling new products while using innovation to renew corporate growth and profitability.

Where to start? It depends. New product development excellence is a journey, not a destination. Any trip depends on preferences and capabilities. Where do you want to go? What abilities and limitations do you have? Where are you starting from? I need to know these things, and more, before I can offer useful advice.

Also, successful innovation depends more on leadership than management. Pulling up the flowers to inspect their growth is not helpful. In general, "less is more." When top management tries to micromanage innovation, it usually makes things worse. Support is needed, not control and fear.

Question: "How many psychologists does it take to change a light bulb?" Answer: "Only one, but it must want to change." I'm not optimistic about a company's ability to change from the bottom up. I've worked in high tech all my life, and had my consulting practice for a decade. I've NEVER seen a company do consistently well at commercial products unless top management *really* wanted to solve that problem.

I'm a national judge for the Product Development Management Association's Outstanding Corporate Innovator (OCI) award. We select candidates from firms with superior business results. Every firm we've examined is different. Still, I've never seen a finalist whose top management did not view new product success as crucial.

My most successful consulting engagements tend to be personal and custom. I'm convinced that interventions, carefully focused to help managers improve business success, add more value for my clients. (A strategic choice. Standard solutions are much more popular—reengineering, for example.)

I start my engagements by asking questions, not offering solutions. A good question to ask is, "What problem are you trying to solve?" Sometimes the answers surprise you.

Once I was retained by the president of a larger consulting firm. They were competent, but stumped. That should have been a warning. Their client had a large defense plant in southern California. The need for the products that plant produced was going away.

JOHN D. TRUDEL

The assignment was to find commercial markets for the plant's exotic, expensive technology. We looked at dozens of markets, several technologies, and numerous methods of financing the total rebuild of this division.

It didn't look promising, but fate intervened. California had a major earthquake. The epicenter was almost under our client's plant. It leveled the place!

The real problem turned out to be the special economic considerations our client received for building in a distressed area and hiring locally. They'd have faced severe penalties for voluntarily closing the plant or shifting the workforce.

We'd certainly solved that problem! Our client was delighted. Still, not being able to count on timely earthquakes, I resolved to ask more questions before I took assignments.

John D. Trudel, CMC, provides business innovation consulting to selected clients. Lectures, keynotes, and workshops also are available. He is the author of "Engines of Prosperity." The Trudel Group, 33470 Chinook Pl., Scappoose, OR 97056; (503) 638-8644; fax (503) 543-6361; e-mail: jtrudel@gstis.net; Internet: www.trudelgroup.com.

HOT PC PRODUCTS

Looking for great sound? Well, if a dozen editors' choice awards are to be believed, the next great thing might be the A3D-enhanced sound cards. Based on the Vortex AU8820 audio processor from Aureal Semiconductor Inc., Fremont, Calif., these sound cards even bring prizes to video games and desktop computers.

Originally developed for NASA, the purpose of A3D was to create realistic audio simulation during astronaut training. After being implemented in Aureal's Vortex chip, A3D worked its way into a variety of PCI sound cards. Using only two speakers or a pair of headphones, the A3D positional audio permits PC sound cards to produce a true 3D sound field for the listener.

This technology grew out of the fact that people hear sounds three dimensionally, but use only two ears. According to Aureal, it follows that the same effect could be replicated using two speakers. Aureal 3D recreates the hearing cues that permit people to perceive sounds in the real world. The speakers surround the individual with sounds in all three dimensions.

To bring this sound to PCs, the Aureal 3D utilizes the Vortex AU8820, which delivers more than 300 MIPS of digital processing over the PCI bus. In this process, the digital processing is already optimized for high-quality audio. The host CPU joins the Vortex AU8820 with its MMX-based software, performing the hardware resource allocation and control functions.

The final product is a sound card that provides a realistically perceived sound experience. To check it out, look to over 200 games on the Microsoft Windows platform, such as the Jedi Knight from LucasArts and Freespace from Interplay. Or, find A3D on the Internet, where it's now providing major VRML browsers with lifelike sound. In the PC market, Compaq and Dell now include A3D in some products.

Aureal has also shaken hands with Diamond, agreeing on a broad strategic partnership in which Diamond uses Aureal Vortex chips exclusively in its retail line. It probably didn't take much persuasion, considering that Diamond recently received several awards for its A3D-based Monster Sound Cards.

Vortex was under development for two years before its release. It enables better quality and features, but maintains support of existing DOS legacy audio functions. It can also interface to existing ISA telephony/modem solutions, so OEMs don't have to use an ISA bus. By delivering features like positional 3D audio, pro-quality wavetable music synthesis, and DirectSound acceleration, Vortex should lift PC audio up to another level of quality.

For more information, contact Aureal Semiconductor, 4245 Technology Dr., Fremont, CA 94538; (510) 252-4245; fax (510) 252-4400; e-mail: www.aureal.com. —NK

SCAMP-ering Along The Arctic Ocean's Floor

I'm sure most of us have heard about the potential mysteries of the deep. The Earth's oceans are so vast that no one knows exactly what they might contain. Giant squids, Loch Ness monsters, proof of Atlantis...the myths and speculations go on and on.

Though these mystical creatures and things remain largely a mystery, the seafloor of the Arctic doesn't have to be...especially since the Columbia Earth Institute got involved. Researchers there have created a new sonar system, known as the Seafloor Characterization and Mapping Pods (SCAMP), in an effort to reveal the geography of the Arctic Ocean.

SCAMP consists of two sonar mapping systems. One of these, a swath mapping system, measures seafloor depths. From each side of a submarine, it gages the seafloor depths out to about six miles on each side. Linking together these measurements creates a map of the ocean floor.

The swath mapping system also collects backscatter data. By revealing aspects like lava flows, this data elucidates the texture of the seafloor. The other mapping system being utilized is a sub-bottom profiling system. It complements the swath mapping system by identifying and outlining structures as far as 100 meters below the seafloor.

The SCAMP sonars work by being mounted on the bottom of a U.S. Navy nuclear-powered submarine—in this case the USS Hawkbill. According to Dale Chayes, a Columbia engineer, the submarine has the capacity to get further under the ice more quickly than an icebreaker. Combined with its stability and quietness, it seems that acquiring high-quality sonar data of the ocean floor will indeed be possible.

The resulting data will be used by geophysicists to create 3D images of the seafloor. Scientists will then be able to visually study some of its features. One example, the Gakkel Ridge, lies between the North American and Eurasian tectonic plates. There, a spreading center is creating a new seafloor. The new data may help explain the formation of the oceanic crust and the way that magma is brought to the surface.

The Gakkel Ridge is just one part of the Arctic Ocean that scientists don't understand. For reasons that haven't been discovered, the Arctic also has a great effect on the Earth's climate. Water samples also will be taken to gain some understanding of these issues and the Arctic Ocean's circulation. As the SCAMP rides the Hawkbill through this 75-day trek, scientists say it will collect as much data as a lawnmower cuts grass. Hopefully, no weeds will obscure the big picture.

To find out more about SCAMP, contact Columbia University, 2690 Broadway, New York, NY 10027-6902; (212) 854-1754; www.columbia.edu.—**NK**

Implantable Medical Devices Are Mall Proof, So Keep On Shopping

Implantable medical devices and pacemakers grant people more independence. They are, to some extent, free to move around and live a normal life—while being treated. Because these devices are so successful, research and development is being dedicated to new implantable devices, such as nerve stimulators and insulin pumps. Amidst all the applause for these inventions, however, few hear about their potential complications.

Evolution has made these components smaller and smarter, leading to better pacemakers, implantable defibrillators, and other such devices. But, cultural changes also have prompted the development of the electronics encountered every day. For example, almost every retail store is now protected by an electronic article surveillance (EAS) system. While operating, these systems generate fields of electromagnetic energy. The problem? These electromagnetic fields can possibly affect the operation of these sensitive, electronic medical devices.

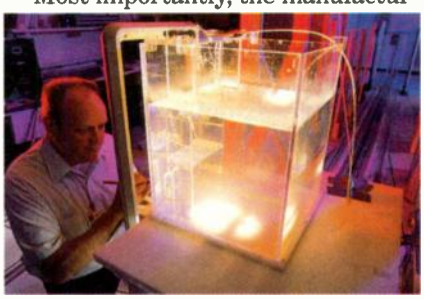
This is where the Georgia Tech Research Institute (GTRI) steps in. Researchers there are doing tests to make sure that individuals using implantable defibrillators or pacemakers can safely walk into a store. The manufacturers of these devices are helping to conduct the research. By donating their actual devices, they assist researchers in testing their specific equipment for possible interactions between the electromagnetic fields and the electronic components. The hope is that if the interactions are understood through research, they can then be prevented.

The research is a direct result of the cooperation between both sets of manufacturers: the makers of the energy source and those that produce the medical devices. Testing is done at the EAS/Medical Device E3 Test Center, which is supported by the International Electronic Article Surveillance Manufacturers Association (IEASMA). This association estimates that there are about 400,000 EAS systems in use worldwide.

Of these, the most common systems are those that are placed near a store's entrance and exit. By using electromagnetic energy, the EAS system can detect tags that have been attached to the store's products. The test center has eight EAS systems, as well as two EAS system tag deactivators, which were provided by the manufacturers.

Jimmy Woody, GTRI senior research engineer and manager of the test center, and Ralph Herkert, research engineer, activate the EAS products for their research. They then subject devices like pacemakers and defibrillators to the EAS systems' energy fields. With standardized testing procedures, they can discern the medical devices' responses in every range of operation. The data that results is sent back to the manufacturers' design and quality assurance departments. That way, they can improve their products based on the information.

Most importantly, the manufacturers gain the assurance that interference will not affect the medical devices. No harm, therefore, will come to the person using the medical device if they go somewhere where there's an EAS system.



The testing process itself is quite interesting. The medical devices are submerged in a tank of saline solution. This works to simulate the electromagnetic behavior of a human torso. The tank, with the medical device inside, is then moved through a merchandise control system. By using a computer-controlled positioner, the tank is moved in a way that imitates customers walking through these systems in stores. There's even a simulation of customers standing in line, within the vicinity of EAS equipment used to deactivate the anti-theft tags.

According to the researchers, the devices come through the tests with flying colors. They've been designed to handle interference. Any response to an electromagnetic field that's been measured during testing is subtle, according to Woody. For example, pulse rates suffer temporary changes or beats are missed. But, the devices always get back on track right away.

The devices recover normal operation as soon as they are moved out of the vicinity of the electromagnetic field, or if the field is turned off. In addition, the devices revert to the exact operational mode that they were in before testing. So, even if there is slight interference, no skewing of the rate of treatment will occur.

From an outside standpoint, it seems that these devices really should be made foolproof as far as interference is concerned. But in this instance, the medical devices' strength is also their weakness. The most recent pacemakers and implantable defibrillators work by sensing the body's heartbeat. In this way, it can respond to the specific needs of the heart. Upon detection of an abnormal rhythm, they send out electrical pulses which regulate the heartbeat. The heartbeat is thus prompted to return to normal.

The problem lies in the fact that electronic equipment, such as the EAS systems, also generate signals. These signals can be very similar to those of the heart. According to Woody, the electromagnetic field or its modulation can imitate a heartbeat. If it does, a pacemaker or another medical device could detect the signal and become confused.

Manufacturers have invented several ways of dealing with this issue. Filters included in the devices keep out most external signals. There's also a "noise" mode, used when the device is receiving confusing signals. It shifts the device to a generic heart rate and pace until the interference goes away.

Woody says the devices have come a long way, because an electromagnetic field could make a device stop pulsing 30 years ago. The researchers have also tested the effects of microwave ovens, cell phones, electric power equipment, radar systems, and radio broadcasts. So far, these devices are surviving the wireless age just fine.

To find out more about medical device testing, contact the Georgia Tech Research Institute, Georgia Institute of Technology, Atlanta, GA 30332-0800; (404) 894-3411; fax (404) 894-9875; e-mail: www.gtri.gatech.edu.

—NK

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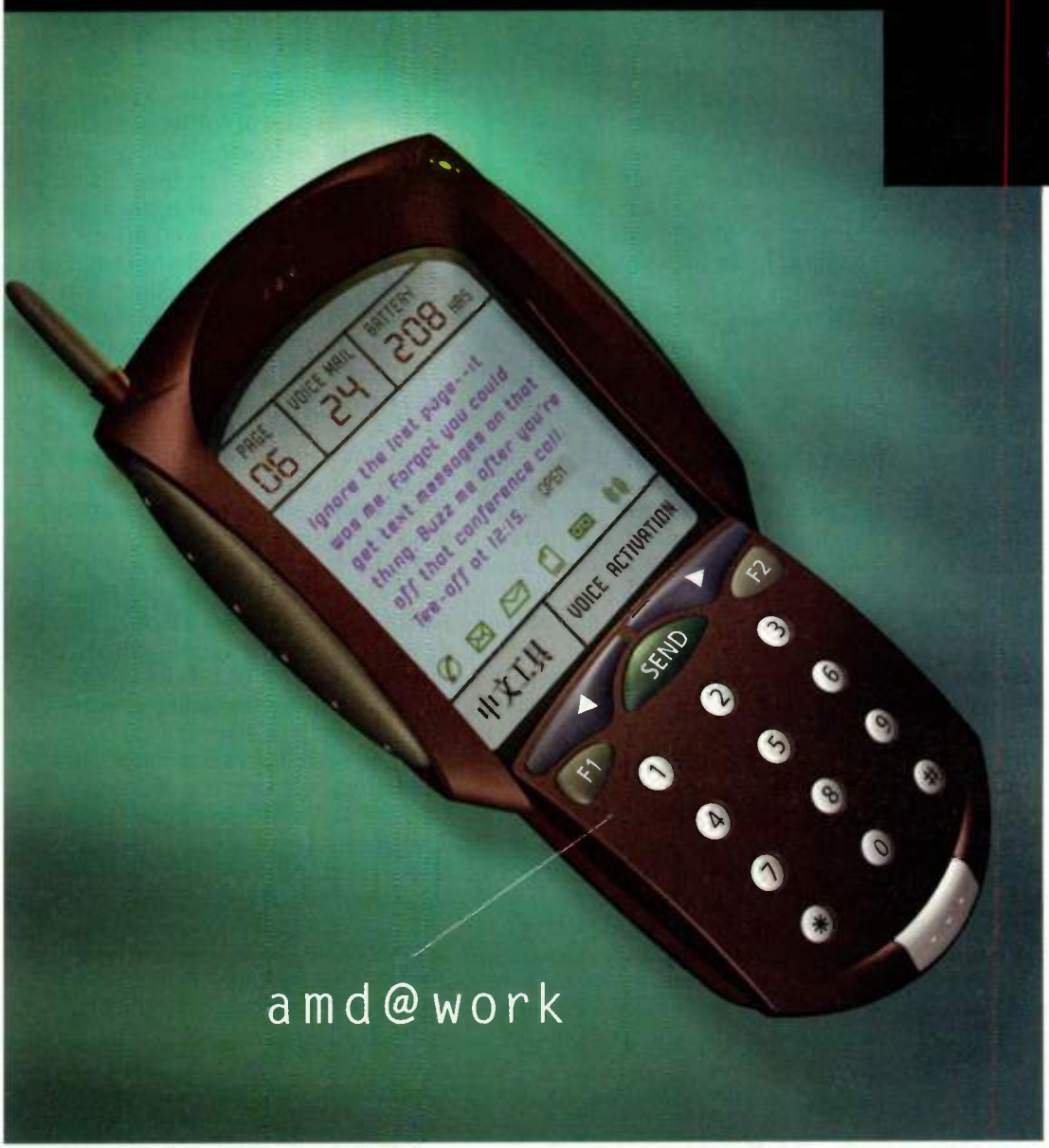

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JUST 4 THE KIDS

Computer technology traditionally brings disparate groups of people closer together. To remain competitive in this global market, it's increasingly necessary for many adults to learn to speak, read, and write different languages. Those of us with children know that when they're young, their minds are like sponges—eager to soak up any new information. It would benefit our children if we would take advantage of this willingness to learn and teach them other languages.

Thanks to a new series of CD-ROMs, called Kidspeak, we may now have a quick and easy way to do this. The basic technology for Kidspeak was developed by the Australian-based Smarty Pants Publishing. Transparent Language, Hollis, N.H., modified it to make it reflect the needs of the American consumer. Focusing on the fact that younger children are apt to learn new languages faster, the Kidspeak series of foreign language titles is specifically intended for children ages six to 12.

Kidspeak offers 11 language titles from which to choose: Spanish, French, German, Italian, Portuguese, Hebrew, Japanese, Mandarin Chinese, Korean, Indonesian, and English. Through the immersion method, the CD-ROMs engage the child in learning.

The child is directed by an animated talking friend and his or her pet. This friend, speaking only the target language, is the guide for more than 40 games, songs, and other fun learning exercises. Each Kidspeak language CD-ROM features a different friend. Titles include Pepa Teaches Spanish, Claudine Teaches French, Pip Teaches German, Mike Teaches English, Michio Teaches Japanese, Budi Teaches Indonesian, and so on.

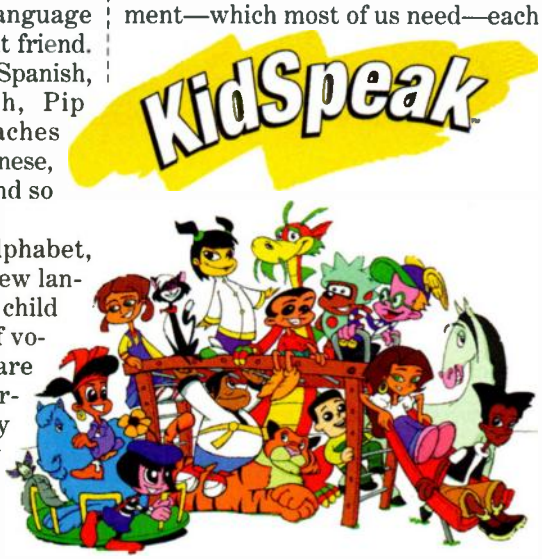
The basics, such as the alphabet, numbers, and songs of the new language, are taught first. The child then advances to a variety of vocabulary words. Activities are divided into five learning areas: Play with Numbers, Play with the Alphabet, Play Happy Birthday, Play with the Animals, and Play with the Backpack. Five activities comprise each learning area. For example, the Play with Numbers learning area is divided into Play Bingo, Add and Subtract, Connect the Dot, Sing the Number Song, and Play Dominoes. In addition, each of these activities have three levels of difficulty so the child learns at his or her own pace.

MARIFRANCES WILLIAMS

Kidspeak CD-ROMs educate in both written and spoken languages, while teaching simple math skills, computer literacy, and problem solving. They focus on specific skills, including correct pronunciation, word recognition, simple sentence structure, plural and singular forms, basic addition and subtraction, and over 700 key words and phrases. Each language program uses the voices of native speakers and features an illustrated, online audio dictionary.

Kidspeak comes with the Language Series Parent's Guide, which provides tips and ideas to assist the child's learning. It even offers an English language help screen. This is a big help to parents who don't speak the language the child's learning, especially if they're concerned about being faced with questions.

Kidspeak also contains printed activities and exercises to extend the learning experience beyond the computer. And, for positive reinforcement—which most of us need—each language program awards an official Kidspeak Diploma and a free Kidspeak T-shirt when the program's completed.



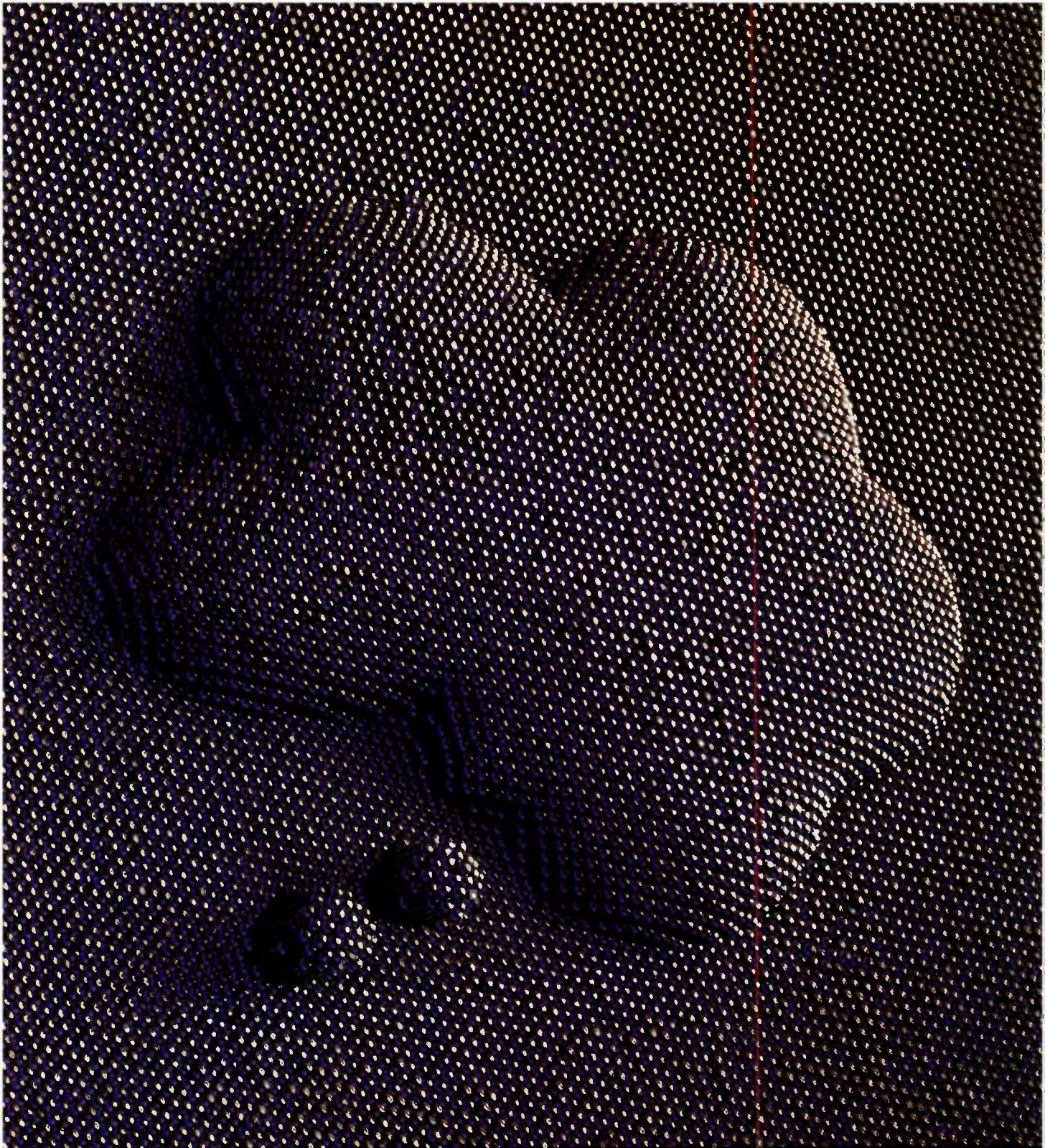
Language is an integral part of our lives. It ties us together, both personally and professionally. The Kidspeak language-teaching tool offers a user-friendly, fun, interactive way to jumpstart a child as he or she learns to communicate effectively. Best of all, the child is immersed in a playful and friendly foreign language environment. This appeals directly to the child's innate ability to acquire language. The games, activities, great sound effects, and colorful animation make the learning natural.

If you want to brush up on your skills or learn a new language, Transparent Language offers a foreign language program for adults, called 31 Languages of the World. Its innovative, three-step process keeps learning both engaging and enjoyable. The program even includes practice conversations with native dialogues. Other CD-ROM's available from Transparent Language are Language Now!, WordAce!, Talking Translation Dictionary, and Easy Translator.

Kidspeak CD-ROM is now available at retailers. It costs approximately $19.95 for individual language programs, or $39.95 for the ten-in-one multilanguage package. The 31 Languages of the World sells for $39.95. Transparent Language's other programs are in the same price range.

For more information, contact Transparent Language Inc., 22 Proctor Hill Rd., P.O. Box 575, Hollis, NH 03049; (603) 465-2230; www.transparent.com.

Marifrances D. Williams holds a degree in Liberal Studies from San Diego State University, Calif. She is currently a fifth-grade teacher at Los Ranchos Elementary, San Luis Obispo, Calif. Williams specializes in the identification of advanced technology for the use of child-focused applications. She may be reached at williamsofsm@lightspeed.net.



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KMET'S CORNER

RON KMETOVICZ

Parents, or those headed in that direction, please read this column. I provide insight on raising your child to become an engineer.

During the past few weeks I've found myself speeding down memory lane. My father's death in late March launched these trips. I've gone in many directions, but keep returning to one primary topic: my childhood and formative years with Dad. And, of all things considered, my father laid the foundation for my becoming an engineer.

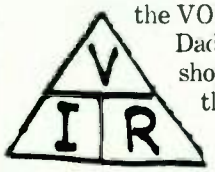
I honestly cannot remember when I started using hand tools. A hammer, screwdriver, wrench, and pliers extended from my body. These were no kid's tools, they were the genuine articles. I'm sure I played with each of them, but more important, I'd imitate what Dad did.

On those projects where I might harm myself or the work that needed doing, he set me up, assisting on the side, doing busy work. With my age still in the single digits, I became quite skilled using simple hand tools. And remarkably, the smashed fingers that were cut and bruised in the process of learning retained not a single scar or deformity.

Also, while still under the age of 10, after learning how to add, subtract, multiply, and divide (but way before I knew the concept of an equation or algebra), I learned Ohm's Law. Dad provided me with the illustration here on a sheet of paper. He told me it was Ohm's Law, and I accepted it.

He showed me how to use it with a battery, volt-ohm meter (VOM), and a light bulb. We measured the V of the battery, and the R of the light bulb. He then told me that once I knew two of the three items, I could use math to figure out the third by following the picture. In this case, because I knew V and R, I needed to divide R into V to calculate I.

After doing the long division, he showed me how to measure I with the VOM to check my work.



Ohm's Law

Dad's passing made it necessary for me to handle the "stuff" in his shop. This activity really woke me up! His shop changed very little over the years, but since leaving for college 33 years ago, I've had no need to use it.

The sensation was strange. I resided in the shop in the present, but saw a kid and his dad working with the tools and instruments as I handled many of the items. I became reacquainted with the oscilloscope, RLC meter, audio oscillator, and sweep generator.

I remembered the instructions Dad provided on the use of these instruments, and the atmosphere of learning by destruction he tolerated. Oh how nice it would be to blow-up a few capacitors once again! My dad made messing around with electronics interesting and fun.

He even made it possible for me to win a science fair competition with a Tesla coil he helped me build. We finished this project two years before blowing up the garage on our final science project!

So parents, follow my dad's example. Introduce your child to tools early in life, spend time teaching by doing. Then teach your child the art of instrumentation. You'll have to spend money on the basic items such as a VOM and oscilloscope. And, most important, give of your knowledge and time in an unselfish manner as you watch your child attempt to destroy the world you've created.

Ron Kmetovicz, president of Time To Market Associates, is the author of "New Product Development, Design and Analysis." He helps new product development teams deliver profitable products to the market quickly. He can be reached at: P. O. Box 1070, 100 Prickly Pear Rd., Verdi, NV 89439; (702) 345-1455; fax (702) 345-0804; e-mail: kmetovicz@aol.com.

INTERNET NEWS

Here's a chance to try a new file expander and win a travel voucher, accessory bag, and software. All that's required is a trip to Aladdin's web site to download their new Aladdin Expander version 2.0 for Windows.

Geared toward online users, this freeware product was created to make expanding files easier. Able to work with all popular compressed and encoded files, it's supposed to make downloading from the Internet or online services a breeze.

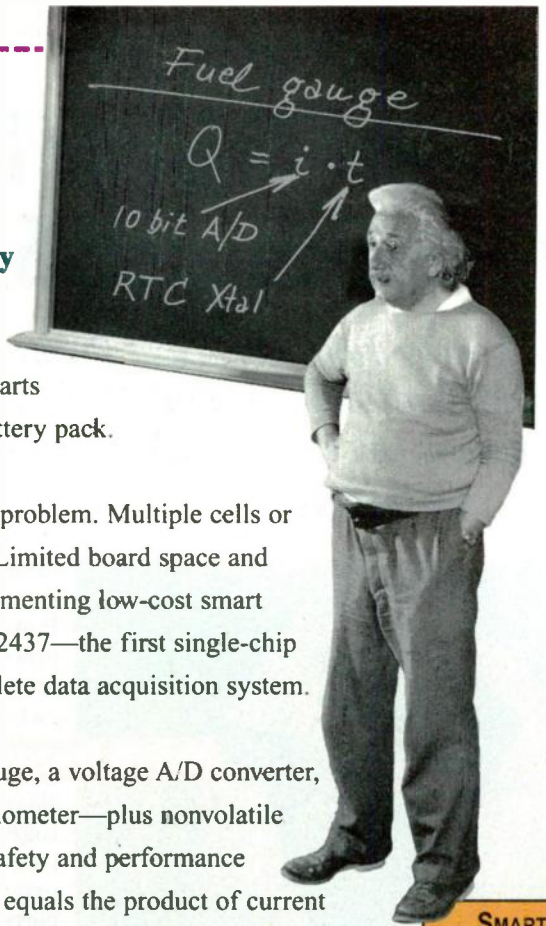
The Aladdin Expander 2.0 is also the first Windows decompression tool that can expand StuffIt-compressed files. Because StuffIt's usually used for decompression on the Macintosh, Windows and Mac users can finally exchange files—despite access or platform compatibility. It also permits users to connect StuffIt Deluxe's segmented archives for the Macintosh. Those big Mac files, divided into smaller pieces for manageability, can now be put back together in Windows.

For convenience, the Expander supports long file names and 32-bit operation. And, if a user upgrades their operating system, the Expander's universal decompression adapts to the new features. Since it works with most file formats—such as Zip, UUencode, Binhex, and MacBinary, to name a few—access to files should never be a problem. It also expands self-extracting archives from StuffIt, Zip, and Arj.

For those privacy lovers out there, Private File decryption capabilities are included. Encrypted documents can be sent to other Private File users, as well as those who have installed Aladdin Expander. These documents travel safely over the Internet, where they cannot be decompressed and decrypted without the correct password.

To download the Aladdin Expander 2.0, just go to www.aladdinsys.com. For more information, contact Aladdin Systems Inc., 165 Westridge Dr., Watsonville, CA 95076; (831) 761-6200; fax (831) 761-6206.—**NK**

WANT A BETTER BATTERY? GIVE IT A BETTER BRAIN!



It doesn't take a *genius* to prevent overcharging and undercharging. The **DS2437 Smart Battery Monitor** provides all the real-time data required to analyze a battery. It's the smarts you need to build a better battery pack.

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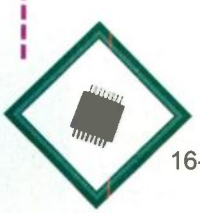
For more information, call us at 972-371-4448, and start building brainier batteries right away!



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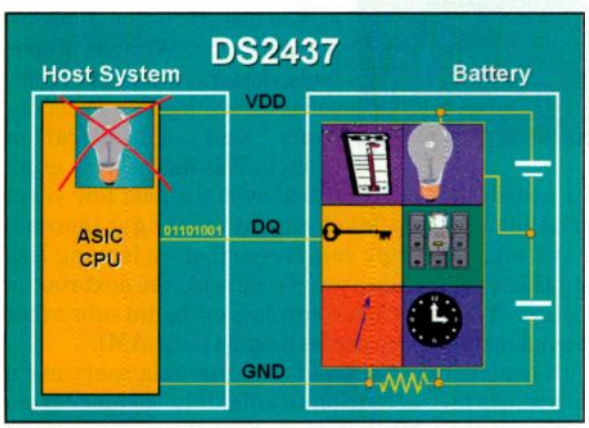

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Lee Goldberg

COVER FEATURE

The age of convergence is upon us, bringing with it a screaming need for tools that can handle high-speed, multiprotocol data streams. Designers face daily challenges as they try to equip the next generation of networking and telecom products with sufficient intelligence and bandwidth to survive in an environment where information is likely to arrive over a series of asynchronous-transfer-mode (ATM) cells, a time-division-multiplex (TDM) packet stream, or a group of Ethernet frames. Fortunately, help has arrived in the form of Motorola's PowerQUICC II, a powerful family of communication controllers and development tools. They give designers the speed and versatility to support applications with highly heterogeneous traffic mixes increasingly common in today's networks.

The controller chip is made on a five-layer, 0.29-µm CMOS process. It integrates a 200-MHz (280-MIPS), 603e PowerPC core; a highly optimized communication processor; memory-management logic; and a collection of programmable communication ports *(Fig. 1)*. These ports can interface with nearly any LAN or WAN in the civilized world. Together, they can route, process, and control data connections with aggregate speeds of up to 710 Mbits/s. Connections with external memory, a host system, or other processors are accomplished by a unique, dual-bus architecture. This enables easy access to external memory, as well as seamless integration with larger systems for applications in enterprise-scale networking products or telco switch equipment.

Speed Alone Isn't Enough

Simply stuffing enough gates and processing power onto a chip is not enough to make it a great controller. Flexibility is important, allowing the designer to fully optimize a design. This is an area where the PowerQUICC II excels. Each processor has its own external bus, allowing it to access its own external memory or I/O at full speed. This also makes it easy to slave several PowerQUICCs together for larger applications. Its communication processor can configure its ports to accommodate a nearly endless combination of ATM, TDM, and Ethernet traffic.

With a chip this complex, ease of use also becomes an important factor. Without proper tools, designers can find themselves drowning in a sea of options and configuration choices. This has become especially critical over the past few years as development cycles get increasingly compressed, often leaving less than a year to develop the next router, switch controller, or digital subscriber loop access module (DSLAM).

To avoid this, Motorola paid careful attention to shielding the user from "integration shock." Using a suite of interactive, online-style design tools, developers can be quickly guided through many time-consuming early design stages *(see "An Innovative Tool And Documentation Approach," p. 38)*. The development software package also comes with a collection of

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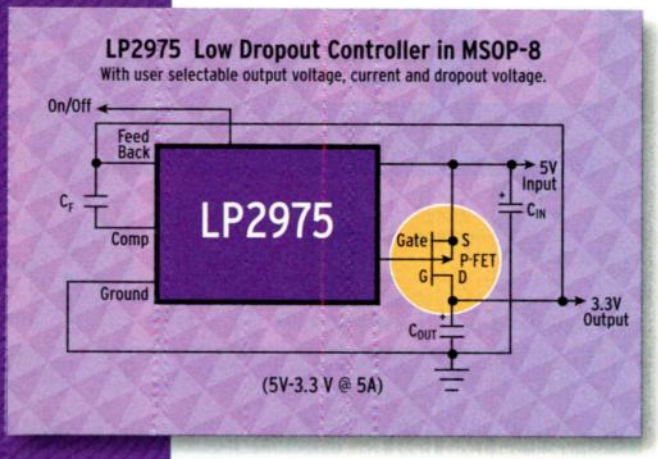

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An Innovative Tool And Documentation Approach

The need to get to market quickly takes top priority today, especially in the fiercely competitive communications and networking industries. With that in mind, designers these days dread designing in a new chip without complete and effective tool support, and equally important, good documentation.

As obvious as it may seem, good tool and documentation support is rare in the chip business. The complexities and intricate details of a communication controller or other highly integrated device can be near-impossible to document in a clear and concise manner using conventional media. Designers get very frustrated when they can see what they're missing. Just look at the web; the proliferation of multimedia PCs; and well-supported, shrink-wrapped software. It's clear that chip support just hasn't kept up with the times.

Bucking that stereotype, Motorola has attempted to provide a level above the usual documentation and tool support with its new Power QUICC II communications processor. Motorola has been working since the beginning of this year on a complete package of elements to help designers use and understand their chip.

At the heart of the package is a user's manual that's well organized and well written, according to the folks at Motorola. They've incorporated improvements based on comments and feedback from long-time users of the PowerQUICC II's predecessors: the 68302, the 860, and the PowerQUICC. Designers using the device typically have experience and background in high-level communications protocols, and don't want to spend too much time designing the hardware.

Motorola has published the manual on CD-ROM in an HTML-hyperlinked format. Whenever it refers to another page or figure, users will be able to just click to go there. A hard-copy of the manual is also provided. The nature of the device involves lots of different modes and configurations, and there are many different details to read through to get the most out of the part.

Motorola has always offered a training course for its QUICC line of processors. If a designer wants to spend four days in a training course, that's available, but starting with the PowerQUICC I, Motorola is putting the training course on a multimedia CD. You can just sit at your computer, watch, and listen to the entire course. You can start and stop it at your leisure, or spend more time on the sections most critical to you. If you want to learn about the ATM controller function, you can go to that chapter and start the player there.

The next element of the support offering is the Decision Package. The Decision Package is basically a set of benchmarks with a software shell organizing them. These benchmarks let users determine whether they have enough MIPS for their applications, and whether your applications can run effectively in the chip's 603 core CPU. You can use the benchmarks to figure out if your memory system is right. Are you going to need SDRAM? Do you need a Level-2 cache? Do you need to put the chip into a slave mode, and run it with a separate 750 RISC processor? Is PowerQUICC II is the right platform or not?

Another part of the Decision Package is a utility called SimSurf. It's essentially a browser-based tool that lets you enter different communications parameters to see if they're possible with the PowerQUICC II. You can, for example, tell it you're going to use a Fast Ethernet controller, an ATM controller running at an OC-3 rate, and a T1 link. Then, it tells you whether it's possible to run those combinations, and if you have enough performance. It will give you a percentage of the performance being used, and show you what you have left over.

For the design phase of the project, the tool package includes Design Assistant. Design Assistant has both hardware and software sides. The hardware side is basically a collection of minimal schematics for the most common applications. If you want to connect the PowerQUICC II to an SDRAM, for example, there's a schematic that shows you how, connecting the resets and clocks. The package is basically one big OrCAD design file with lots of pages, and you can collect the pages with the schematics you need, and then cut and paste a schematic together. Within hours you can piece together a hardware design. Designers can start with the answers and figure out the questions later. There's documentation with each of these schematics explaining some of the non-trivial aspects.

Motorola has attempted to include every common schematic scenario. Examples include schematics connecting to common memory systems, schematics for for running PowerQUICC as a slave to a 750 RISC processor, and a schematic for linking the chip to a PCI interface. There are also schematics for the serial connections—Ethernet, ATM , and so forth.

The software side of Design Assistant includes a collection of drivers for all the serial modes on the chip—a multichannel serial controller driver, a Fast Ethernet controller driver, etc. These drivers, along with the API, allow you to drop code into your application.

Because many developers would rather write their own drivers, the package offers examples that start with minimal driver functions. The functions, for example, include initializing all the parameter RAM, initializing the registers, setting up the buffer descriptors, and sending one packet of data and receiving it back. These are documented with explanations down to the level of why particular bits are set.

Rounding out the package, the PowerQUICC Support includes a rather extensive set of development boards and simulation models. Two boards are provided: one with two PowerQUICCs IIs working together—one as a master, the other a slave; and one sporting a PowerQUICC with a PCI bridge (MPC106). Simulation models available today include a complete set of bus-functional models and full-functional models.

Jeff Child

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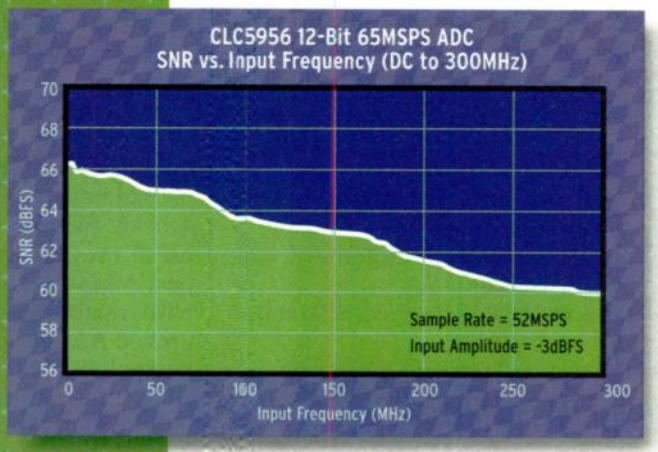

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are several companies which supply seamless PCI bridge intreface solutions *(see "Motorola Communication Controllers And PCI: A Perfect Fit," below)*.

Connections to communication channels are accomplished via a large array of I/O controllers which include:

- Three fast-communication controllers (FCCs)
- Two multichannel controllers (MCCs)
- Four serial-communications controllers (SCCs)
- Two serial-management controllers (SMCs)
- A serial bus interface (SPI) and an I^2C bus controller

The chips' three FCCs can be programmed to handle either 10/100-Mbit/s Fast Ethernet connections (full or half-duplex), or perform the segmentation-and-reassembly (SAR) function for three 155-Mbit/s (OC-3) ATM connections. In their Ethernet mode, the FCCs support the full carrier-sense/collision-detection-multiple-access (CS/CDMA) control protocol, and connect to PHY-layer devices via an industry-standard media-independent interface (MII).

When supporting ATM connections, each FCC can be configured to provide either a UTOPIA or TDM synchronous interface. Its firmware-based, protocol-handling routines support AAL0, AAL1, and AAL5 traffic, with capabilities for the recently approved AAL2 specification under development. On-chip RAM can store connection parameters for up to 128 virtual channels (VCs). The addition of external RAM can enable each FCC to maintain up to 16,000 VCs. The FCCs also can be configured for a transparent mode, or to handle HDLC traffic at up to T3 rates (45 Mbits/s).

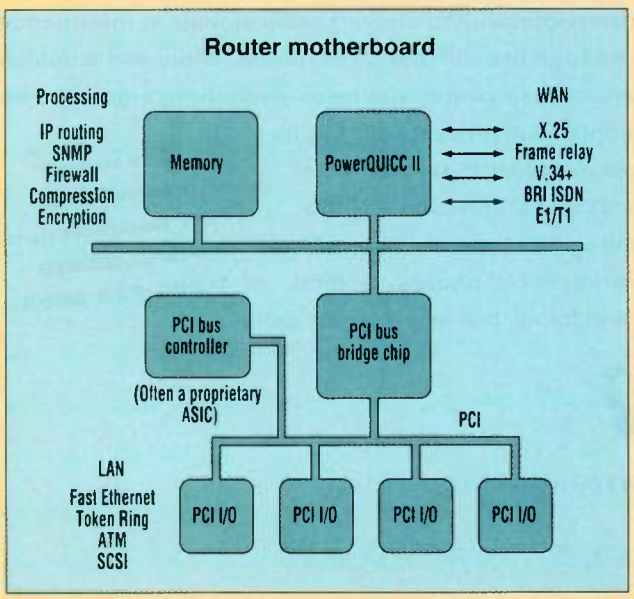
The chips' two MCCs are intended primarily for connecting to TDM-based traffic from public-switched telephone networks (PSTNs), private-branch exchanges (PBXs), or other telephony-based systems. These full-duplex serial channels can handle an aggregate of 256, 64-kbit/s HDLC or transparent channels, multiplexed across up to eight TDM interfaces. The controller allows bandwidth aggregation into larger super channels, as well as subchanneling within a single 64-kbit/s stream.

An additional four channels of Ethernet, high-level synchronous data-

Motorola Communication Controllers And PCI: A Perfect Fit

Pop open the hood of any contemporary data-communications system, and odds are that you'll find the PCI bus lurking there. A key factor driving PCI into the communications market is its ubiquity amongst I/O controllers: 10/100-Mbit/s MACs, HDLC controllers, etc. At the same time, a large proportion of these same systems are based on Motorola communications controllers, notably the MPC860 (PowerQUICC). Beginning with the 68302 in 1989, Motorola has built a wide-ranging communications controller dynasty with the 68360, the MPC860, and now the MPC8260.

However, with PCI originally intended for the PC/server market, PCI bridge vendors focused on Intel processors (e.g. the i960). About three years ago, this created a requirement for a PCI bridge targeted at Motorola communications controllers. To understand this requirement, it's helpful to review a common communications system architecture.



Within an embedded communications system (say, a router), PCI is the glue that brings the various I/O controllers onto a common I/O bus *(see the figure)*. This means that the PCI host bridge occupies a central position, connecting CPU and system memory to I/Os on the PCI bus. Control information flows out to the PCI bus from the CPU, while I/O controllers on the PCI bus transfer data between their LAN/WAN ports and ring buffers maintained in host memory. The transfer of packet data between the I/O controllers and host packet memory places the PCI target channel of the host bridge on the critical performance path.

As systems migrate toward the MPC8260 with its 64-bit data bus running at 80 MHz and above, the PCI host bridge becomes a potential bottleneck between host packet memory and I/O. To meet this need, chips like the QSpan chip from Tundra Semiconductor, Kanata, Ontario, Canada, were designed to fill the gap between Motorola's communications controllers and PCI. They provide direct connect power-up modes for the 68360, 68040, and the MPC860. However, there is a need to go beyond conventional 32-bit PCI bridges. Some of the architectural approaches for high-performance embedded host bridging for the MPC8260 will include multiple PCI ports and 64-bit/66-MHz PCI. Along with new performance requirements, the industry is adopting new standards like I^2O and CompactPCI hot-swap as vigorously as it had with the PCI bus itself.

Contributed by Tom Wilson, director of marketing, Tundra Semiconductor Corp., Kanata, Ontario, Canada.

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erQUICCs should feel right at home.

Thanks to its versatile architecture, the PowerQUICC II can be configured in an almost limitless series of speeds, feeds, and protocols. The processor's architecture permits a designer to allocate the unit's 710-Mbit/s throughput to the I/O ports in almost any conceivable combination.

A Dramatic Shift

This makes the processor a cost-effective candidate for many applications previously out of reach for a single-chip device *(see the table)*. In fact, Cam Witt, program manager for Motorola's Networking Group, anticipates that the processing power available in this controller should move an entire class of communication products to a lower cost point.

For example, it is conceivable that a high-end router could be constructed out of little more than one or more PowerQUICCIIs, along with their associated RAM and PHY-layer interface devices *(Fig. 2a)*. Other applications already proposed by Motorola's applications group include remote access concentrators, LAN-to-WAN bridges/routers, and remote-access servers *(Fig. 2b)*.

The PowerQUICC's ability to serve as master or slave on a PCI bus will open the door to many PCI-based telecom applications *(Fig. 3)*. In the telecom world, Motorola anticipates the PowerQUICC II powering cellular base stations and switch controllers, and controlling ADSL access equipment such as DSLAMs.

The few applications listed here are only the tip of the iceberg. The development software supplied by Motorola contains the outlines for a veritable galaxy of communication-related products. In reality, however, the best applications will probably emerge as designers across the globe begin to get their hands on this powerful new chip.

Price And Availability

The PowerQUICC II will be packaged in a 401-pin ball-grid array. Alpha sampling will begin this month, with general sampling starting in January 1999. Full production is scheduled for May 1999. Pricing for the 133-MHz version is anticipated to be $105 each, in 10,000-piece quantities.

Motorola Semiconductor Networking and Computing Systems Group, 6501 William Cannon Dr. West, Austin, TX 78735-8598, M/S OE216, attn: Cam Witt; (512) 895-6082; fax (512) 895-8807; e-mail: ra7162@email.sps.mot.com.

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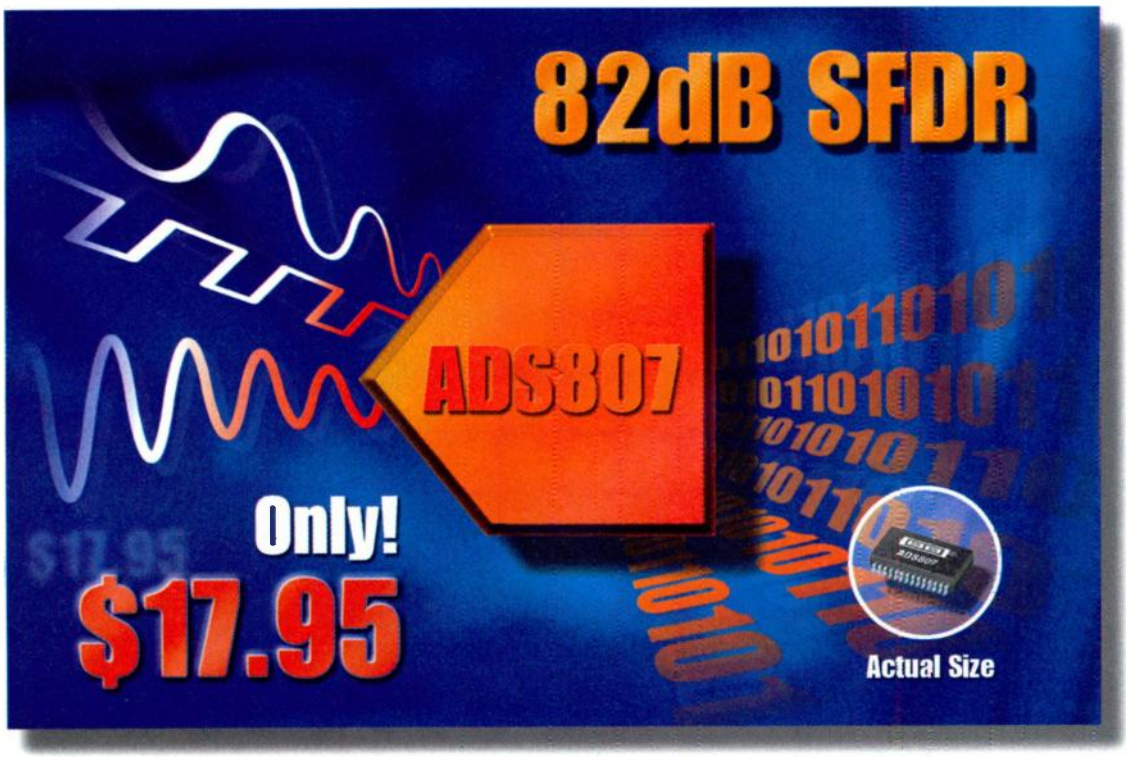

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Dave Bursky

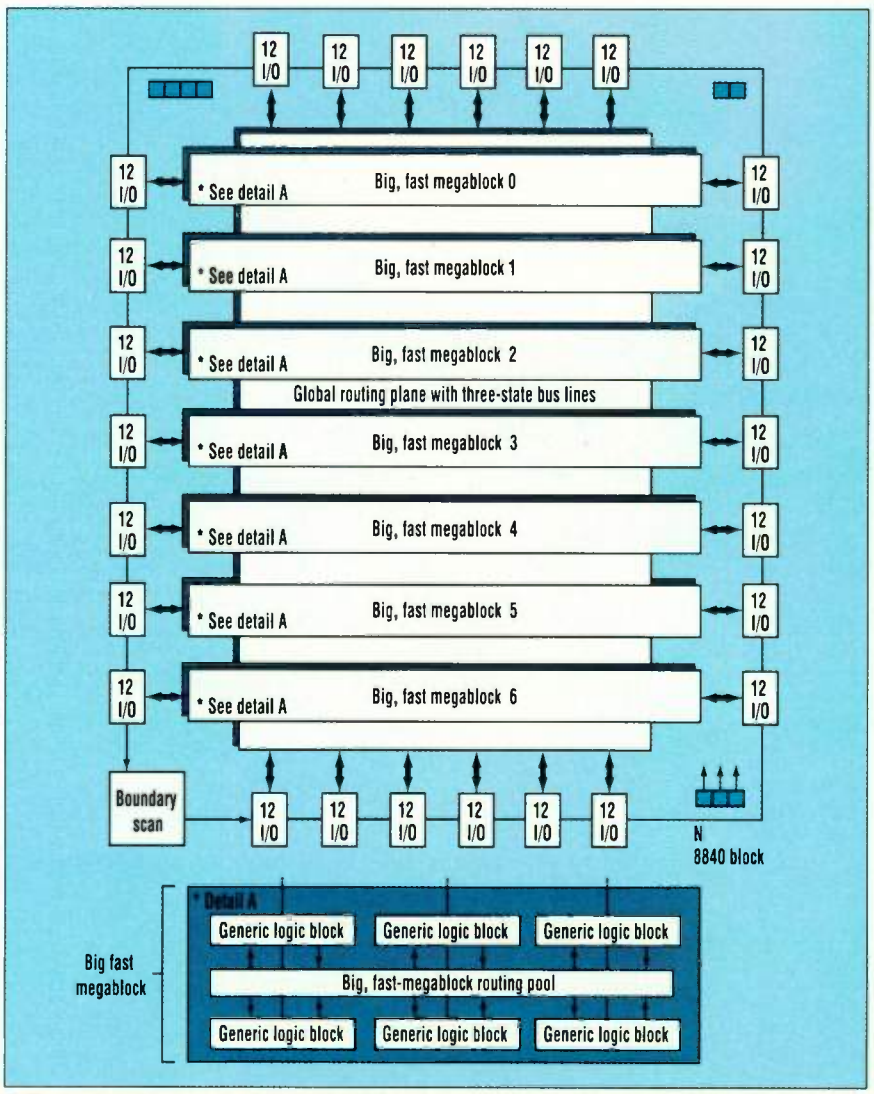
As system designers continually try to cut system chip counts, complex programmable logic devices (CPLDs) move to the forefront. Chip densities have increased, allowing the CPLDs to offer more gates and I/O cells. And recently, developments from various suppliers have started to push CPLD complexities beyond the 10,000 gate and 300 I/O mark. With such resources at their disposal, designers can leverage the programmability to craft flexible system solutions.

Following in that trend, the latest development is the in-system programmable ispLSI 8000 family from Lattice Semiconductor. This series not only delivers chips with top capacities, but package options that allow extremely high pin counts for a CPLD—the largest family member packs 43,750 equivalent PLD gates in 840 macrocells. Pin counts range from 148 to 312 I/O pins, and from 204 to 432 total pins (depending on the chip and the package). The architecture is also extensible to structures with more than 1000 macrocells—it's just a matter of the cost-effectiveness of the larger chips.

Thanks to some innovative architectural design and the use of the company's high-performance, 0.3/0.35 µm E^2CMOS nonvolatile memory technology, these chips can operate from a 5-V supply (including in-system programming), and run at maximum clock rates of 110 MHz. To achieve those speeds, the internal logic and routing resources keep the pin-to-pin propagation delays as short as 8.5 ns, and provide clock-to-output delay times of just 8 ns.

Those short delay times allow functions such as a 20-bit counter to run at 110 MHz, a wide multiplexer (32:1) to have a delay of just 13.5 ns, and a state machine with wide decode (up to 28 product terms, 44 inputs) to operate at 110 MHz. The ispLSI 8000 series is also the first family of CPLDs to include internal three-state buses in the chip's global routing plane. Such buses allow the multiple global logic blocks to drive the same track, thus more efficiently using the routing resources.

The basic architecture of the family is register intensive. On the largest member, the ispLSI 8840, Lattice designers provide up to 1152 registers with which large state machines,



1. The basic architecture of the ispLSI 8000 series of CPLDs consists of multiple big, fast megablocks (BFMs) that are supported by a global routing plane, and surrounded by an abundance of I/O cells. Each BFM, in turn, comprises six smaller, generic logic blocks that are locally interconnected through the BFM routing pool (see detail A).

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AT17C256	256K x 1	5.0 V	No	In Stock
AT17LV256	256K x 1	3.3 V	No	In Stock
AT17C512	512K x 1	5.0 V	Yes	In Stock
AT17LV512	512K x 1	3.3 V	Yes	Q2 98
AT17C010	1M x 1	5.0 V	Yes	In Stock
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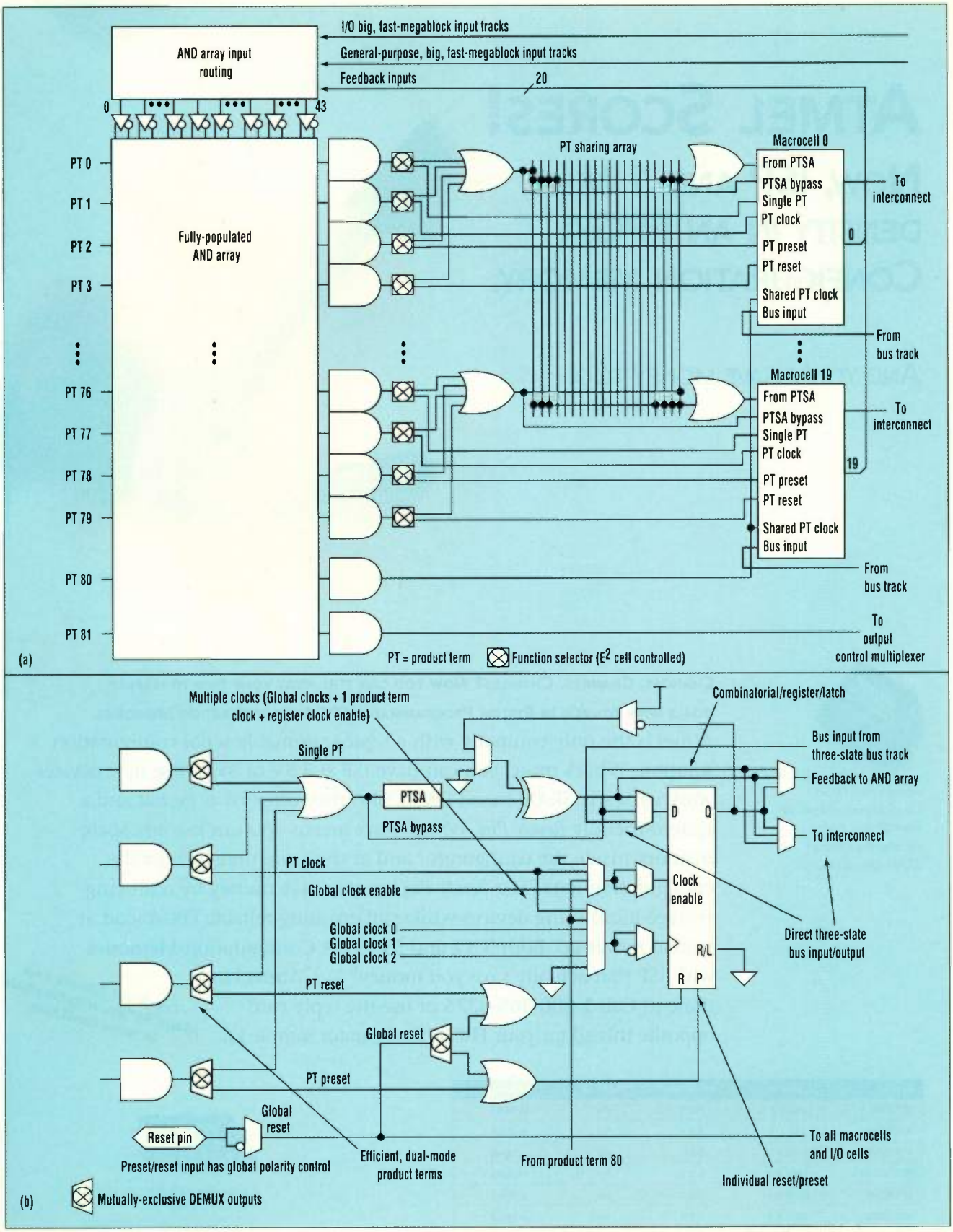
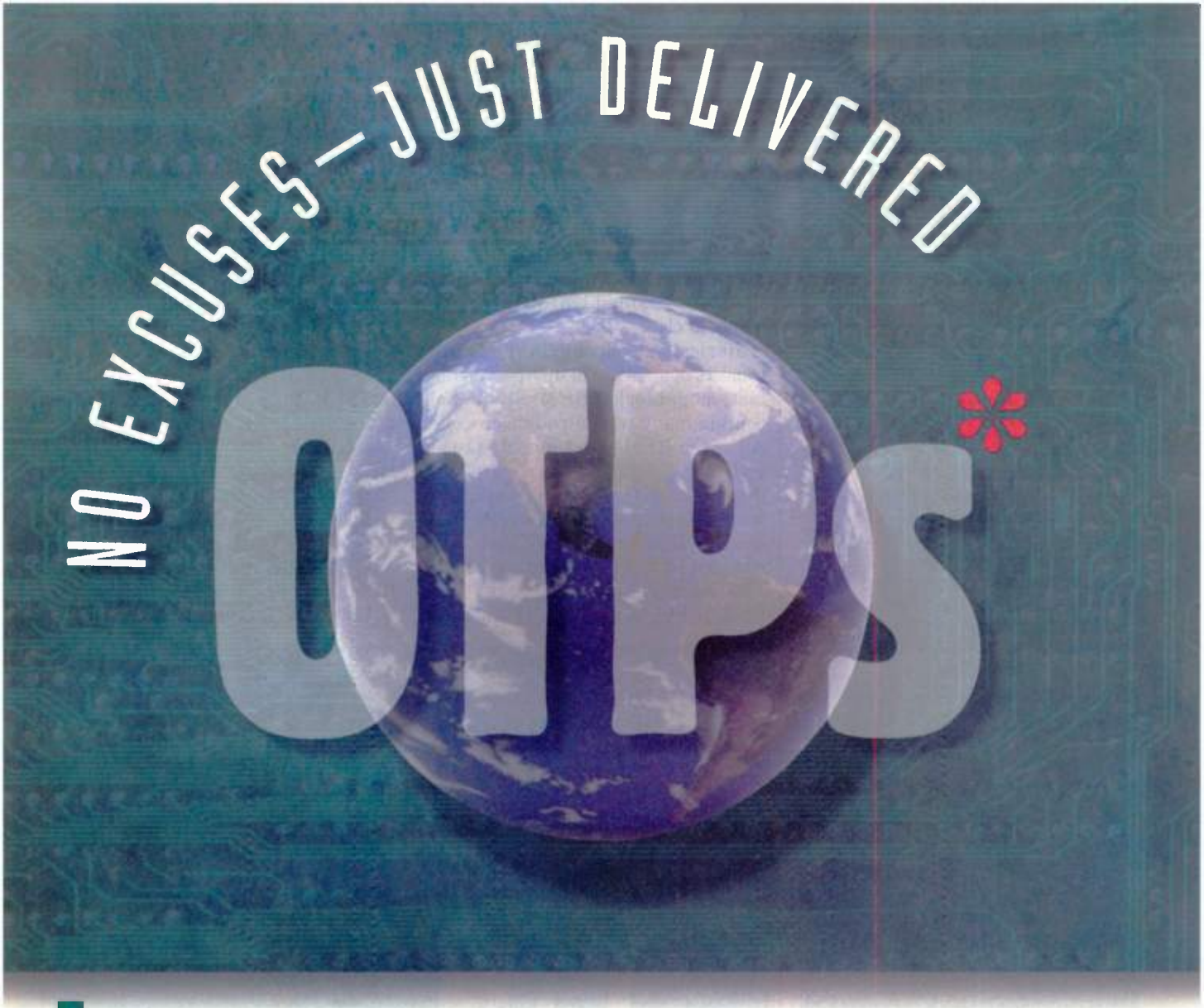


2. Each generic logic block (GLB) in the array contains a fully populated AND array and product-term sharing arrays that allow up to 28 product terms to be shared for a single function (a). Also included in each GLB are 20 macrocells, each of which includes an XOR gate, and a configurable logic element that can serve as a combinatorial function, a register, or a latch (b).



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68HC705J1A	1.2K	64	20	M68ICS05J	KITMMEVS05KJ	KITMMDS05KJ
68HC705P6A	4.6K	176	28	M68ICS05P	KITMMEVS05P6A	KITMMDS05P6A
68HC705C8A	8K	304	40,44	M68ICS05C	KITMMEVS05C	KITMMDS05C
68HC705C9A	16K	352	40,44	M68ICS05C	KITMMEVS05C	KITMMDS05C
68HC705B16	15K	352	52,64	M68ICS05B	KITMMEVS05B	KITMMDS05B
68HC705L16	16K	512	80	KITPGMR05L16	KITMMEVS05L16	KITMMDS05L16

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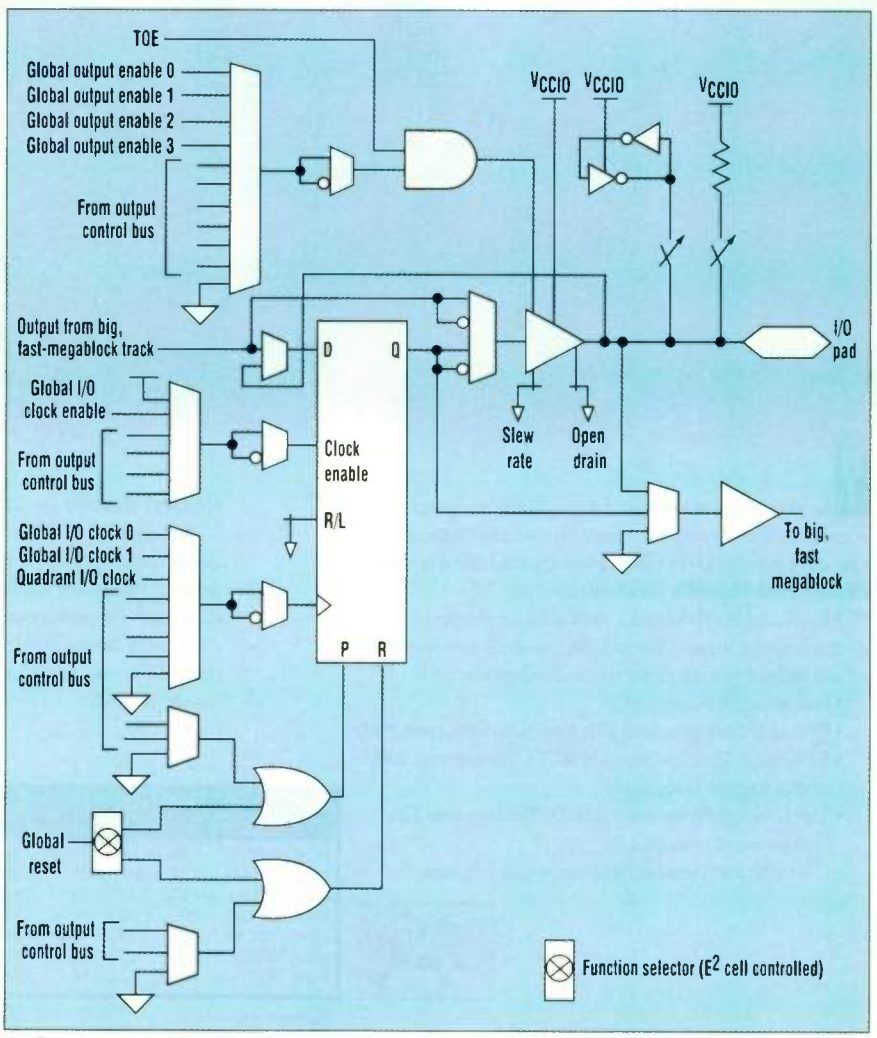
pipeline registers, and other flip-flop-intensive functions can be implemented. Two smaller family members, the ispLSI 8480 and 8600 have also been defined; they will offer 25,000 and 31,250 gates, and depending on the package used to house the chips, from 148 to 240 and 176 to 264 I/O pins, respectively.

Basically, each chip in the family consists of an array of up to seven big, fast, megablocks (BFMs) that each contain many registered macrocells. All of the BFMs are connected to an underlying global routing plane (GRP) that contains the interconnection resources to route signals between them *(Fig. 1)*. The array of BFMs is surrounded by blocks of I/O support and JTAG-based boundary-scan logic. Each I/O block, in turn, contains 12 configurable I/O cells. In-system programming is performed through the industry-compliant JTAG boundary-scan test port using either the BSCAN protocol or Lattice's proprietary ISP protocol.

Each BFM contains 120 registered macrocells that are divided into six groups of 20, with each of the smaller groups referred to as a generic logic block, or GLB *(Fig. 1, inset)*. Within each BFM is a "local" block of programmable interconnects, referred to as a BFM routing pool (BRP). This BRP interconnects the six GLBs to each other and to 24 BFM I/O cells with optional I/O registers (left and right sides of each BFM in Figure 1). The GRP under the entire array of BFMs provides an additional resource of 144 global I/O cells, each with op-



3. The programmable I/O cell packs many configuration options that allow designers to set it as registered input, registered output, combinatorial input, combinatorial output, or bidirectional. The register can be clocked from any of several global, logic, or product-term clock signals that can be selected by control signals on the I/O control bus.

tional I/O registers (top and bottom I/O cells in Figure 1).

Each of the GLBs contain a fully populated, programmable AND array, with 80 logic product terms, in addition to the 20 macrocells *(Fig. 2a)*. The GLB also has 44 inputs from the BRP, and those signals are available in both true and complement form for every product term. Up to 20 of these inputs can be switched to provide local feedback into the GLB for logic functions that require such feedback. The 80 product terms delivered by the AND array are divided into 20 sets of four. Each set is sent to a product-term sharing array (PTSA) that allows the sharing of up to 28 product terms for a single function. Alternately, the PTSA can be bypassed if functions of four or fewer product terms are needed.

Inside each of the 20 macrocells in the GLB is a programmable exclusive-OR (XOR) gate, a programmable register/latch/toggle flip-flop, and the necessary clocks and control logic to allow combinatorial or registered operation *(Fig. 2b)*. The macrocells each have two outputs, one of which can be fed back into the GLB's AND array, while the other drives both the BRP and the GRP. This dual-output capability allows the software tools to more efficiently use the hardware resources. For example, one output can be a registered function, while the other output can be an unrelated combinatorial function.

The programmable register in the macrocell can be configured as a D-type register, a D-type latch, or a T-type flip-flop. It also can be clocked from one of several global, local, or product-term clocks available on all the ispLSI 8000 family members. A clock-enable product term is available for each option as well, eliminating the need to gate the clock to the macrocell registers. Additionally, the Reset and Preset signals for the macrocell register are provided by either global or product-term signals. The polarity of all these control signals is also selectable on an individual macrocell basis.

Tying all the BFMs together, the GRP employs a 108-line embedded three-state bus that allows multiple GLBs to drive the same track. This bus can be partitioned into six 18-line, or three 36-line sub-buses as well, allowing several independent data transfers to take place simultaneously, and improving system bandwidth. The GLBs can dynamically share a subset of the GRP tracks, which permits the same routing resource to be reused. That also eliminates the need to convert three-state buses to wide multiplexers on the programmable device.

Up to 18 of the macrocells in each GLB can be connected to drive a three-state bus. The remaining two macrocells in each GLB are used to generate the internal three-state driver control signals. Additionally, the embedded three-state bus can also be configured as an extension of an external three-state bus by using the bidirectional capability of the I/O cells that are connected to the GRP.

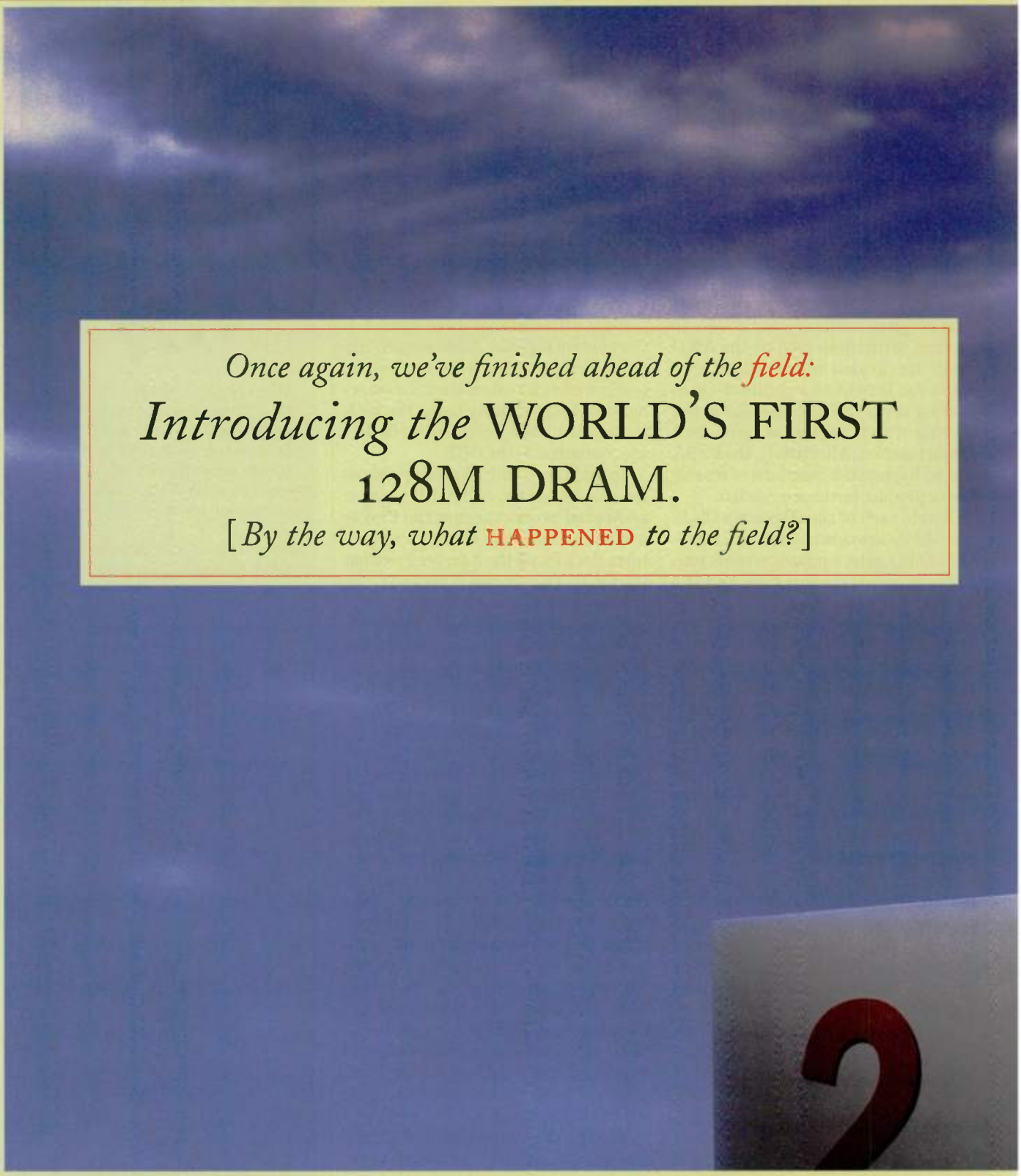
In addition to the 80 product terms mentioned earlier, each GLB has two additional product terms; the first is used as an optional, shared product-term clock for all the macrocells within the GLB. The second is routed to an I/O control bus using a separate routing structure from the BRP. This separate control-bus structure allows the I/O registers to have many control signals without an impact on the interconnection of the GLBs and BFMs.

The I/O control bus is split into four quadrants, each servicing the I/O cell control requirements for one edge of the chip. Signals in the control bus can be independently selected by any or all I/O cells to act as clock, clock enable, output enable, reset, or preset.

As mentioned earlier, the programmable I/O cells that surround the logic blocks are very flexible. They are configurable as combinatorial input, combinatorial output, registered input, registered output, or bidirectional *(Fig. 3)*. The register in each cell can be configured as either a D-type register or latch, and is clocked from one of several global, local, or product-term clocks. These clocks can be selected via the I/O control bus.

As with the macrocells, the I/O cells have a global and a product-term clock-enable option, eliminating the need for designers to gate the clock to the I/O cell registers. Reset and Preset for the I/O cell register are provided from both global and product-term signals as well. Signal polarity is also selectable on a cell-by-cell basis.

Inputs and outputs of the I/O cells are PCI compatible, with the input



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threshold fixed at TTL levels. The output drivers can source 4 mA and sink 8 mA. Additionally, the output drivers have a separate V_{CCIO} power-supply input that is independent of the main V_{CC} supply for the chip. This allows the output drivers to run from either 3.3- or 5-V supplies while the device logic is always powered by a 5-V supply.

Programmable output features include the option of pull-up resistor or open-drain connections, or a programmable bus-hold latch that can hold the three-state outputs in their last valid state until the bus is driven again by another device. Output signal slew rates are also programmable, allowing the chips to minimize signal noise.

Many of the architectural features of the ispLSI 8000 series were designed to be very "friendly" to design synthesis tools, because the chips provide all frequently encountered logic features without restrictions. Tools have access to global or individual macrocell and I/O register control features such as Reset, Preset, Clock, Clock Enable, and register or latch elements. And, the tools can make good use of the three-state bus, which permits designers to use high-level-design-language bus constructs for faster and more efficient designs. Furthermore, the PTSA allows sharing across multiple macrocell outputs, reducing the amount of logic needed to implement wide functions. And, last but not least, the macrocells allow concurrent registered and combinatorial functions, which improve logic utilization and give the tools more resources to work with.

To support the new family, Lattice has developed a new release of its software tools, Release 6.0. There are actually two versions of support software available—a basic version called ISPDS, and the 6.0 release. Additionally, third-party support is available from Synplicity and ViewLogic, which provide design synthesis and design capture tools.

Price And Availability

Samples of the ispLSI 8840 will be available next quarter. In lots of 1000 units, the chip will sell for $95 each. Prices for the other chips will be lower, but they will not be released until ready for sampling in early 1999.

Lattice Semiconductor Corp., 5555 NE Moore Court, Hillsboro, OR 97124-6421; Steve Stark, (503) 681-0118; or on the web at www.latticesemi.com. **CIRCLE 452**

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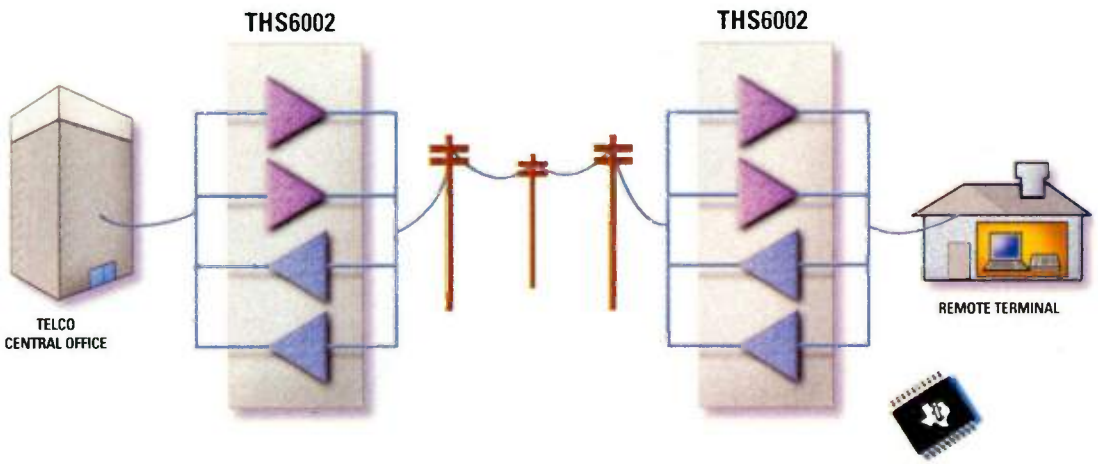

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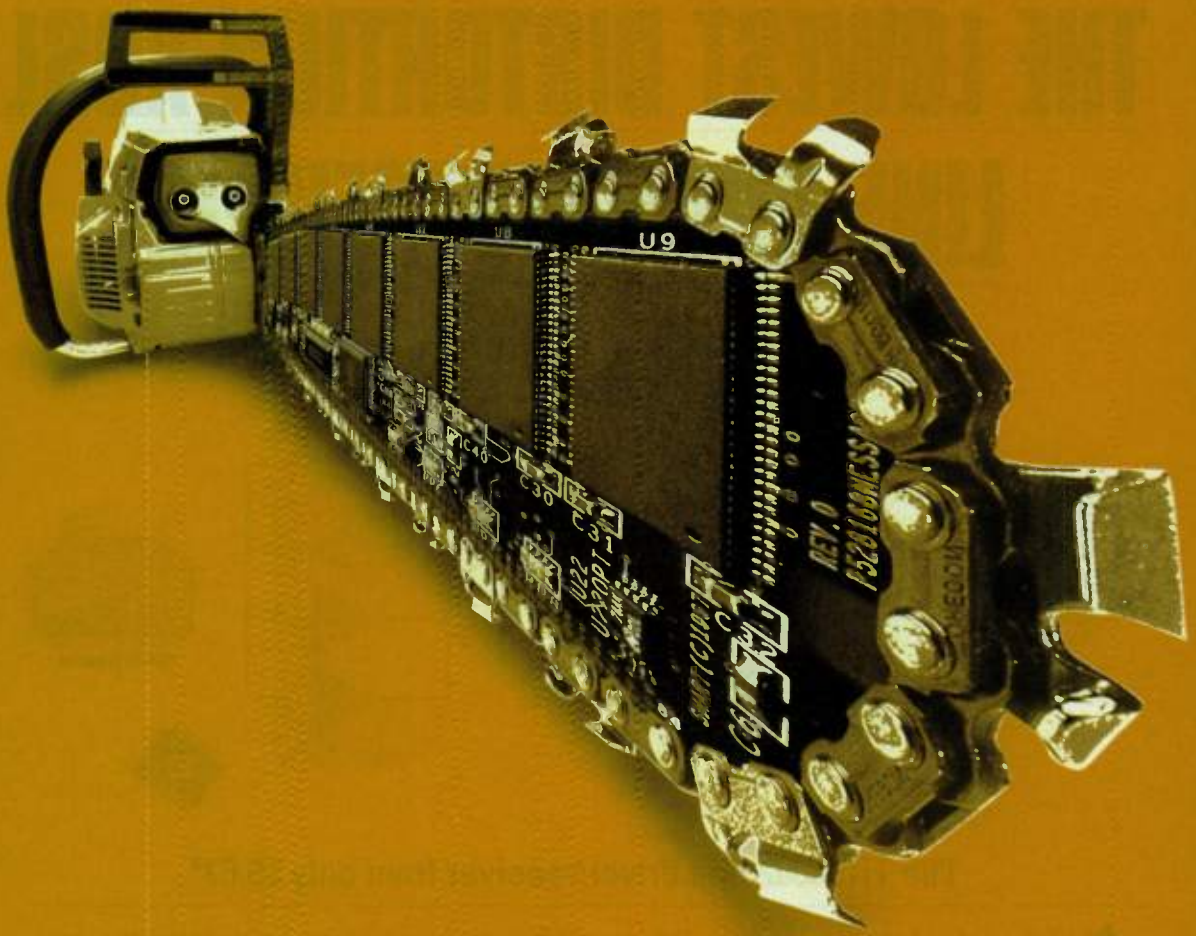

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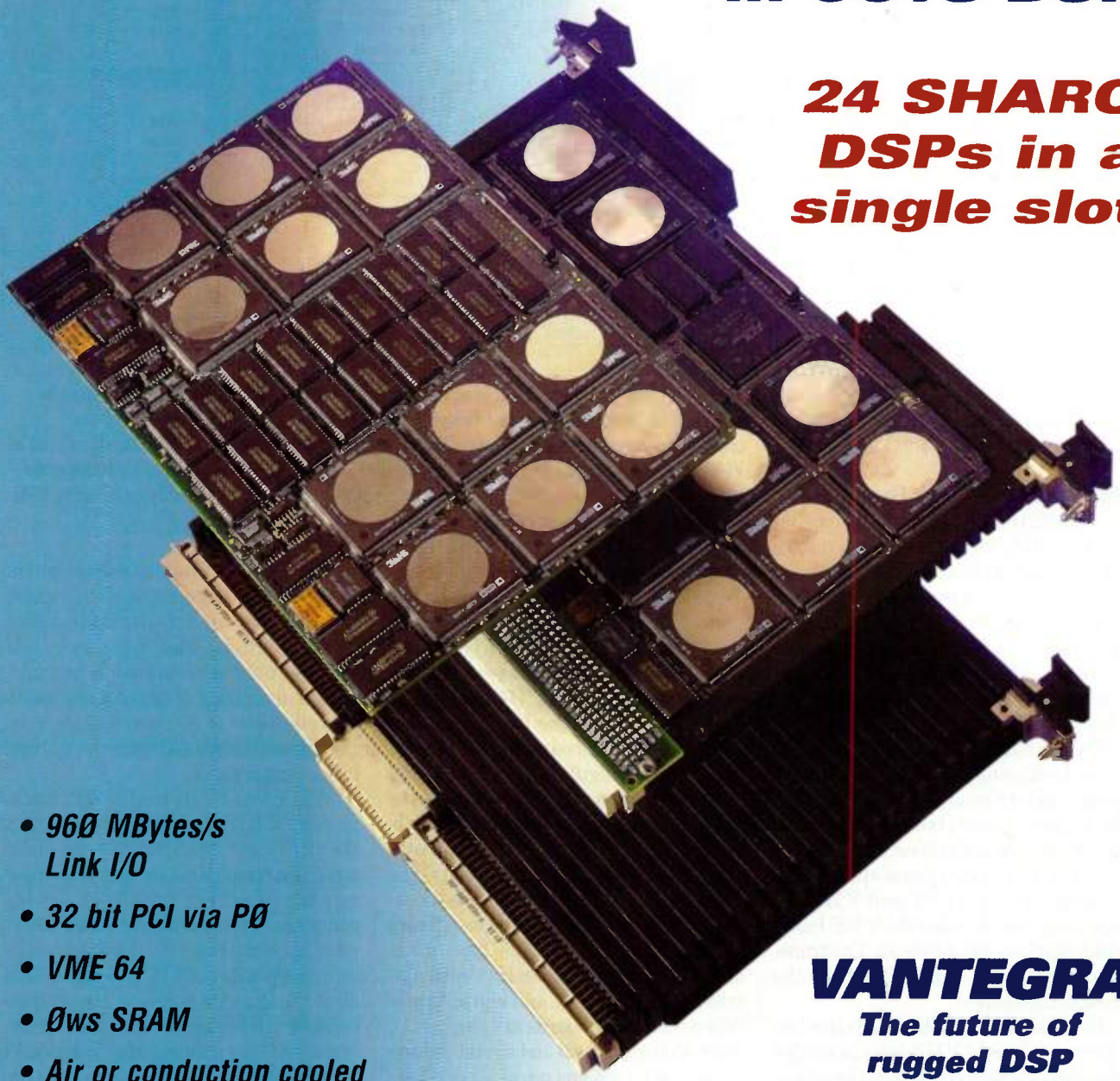

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VME320 backplane standard. While it's not necessary to use that backplane, it will improve the implementation of 2eVME. Achieving the full 320 Mbytes/s of VME320 requires a source-synchronous transfer (SST), which necessitates a VME320 backplane.

So far, Force is the only VME board vendor to offer a 2eVME product. It's questionable whether other vendors will move to 2eVME in light of the VME industry's efforts toward VME320. Why settle for 110 Mbytes/s when you can get to 320? A joint effort between Arizona Digital and Bustronic, the VME320 backplane technology, was first announced in January last year. Since then, companies within VITA have been working to analyze and construct a skew model for the standard. This model will prove that the technology does, in fact, offer 320-Mbyte/s performance.

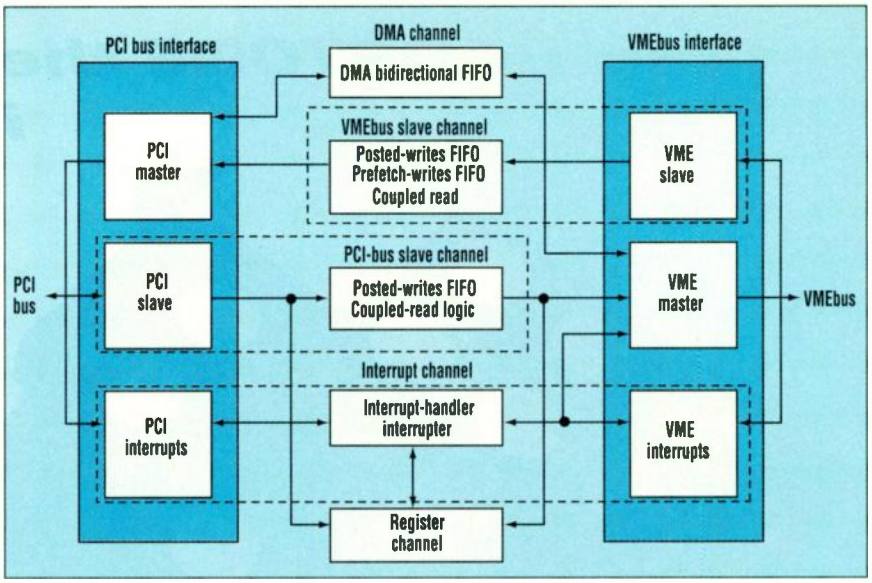
VME320: The Next Leap

VME320 offers yet another leap beyond 2eVME. The 2e SST protocols are just one part of the puzzle. Those protocols get the speed up to 320 Mbytes/s. Unfortunately, the backplane as electrically defined in VME, maxes out at 160 Mbytes/s. After that, reflections aren't given enough time to settle out, and the transfer becomes an incoherent mess.

To clean it up, the patented backplane technology developed by Bustronics and Arizona Digital, mentioned earlier, uses a special routing technique to minimize the reflections, significantly improving the backplane speed. The combination of 2eSST and VME320 technology has doubled the VME bandwidth again to 320 Mbytes/s. The transfer rate of 2eSST is limited only by the skew in the system.

Because most VME boards use the Universe series of VME interface chips form Tundra Semiconductor, the industry is awaiting the next version that incorporates the 2eSST/VME320 technology, Universe III. While the first efforts for VME320 were done by Bustronics and Arizona Digital, a number of other vendors have proposed similar schemes that solve the backplane electrical issues.

"The protocols that we're working on in the task groups within VITA, and that will ultimately be put into Universe III, just need that kind of physics to be in the backplane," says Rick O'Connor, director of business development at Tundra. "From our point of view, it doesn't much matter. If someone provides the physics in a backplane that allows for incident-wave switching, our chip will support it," O'Connor says.



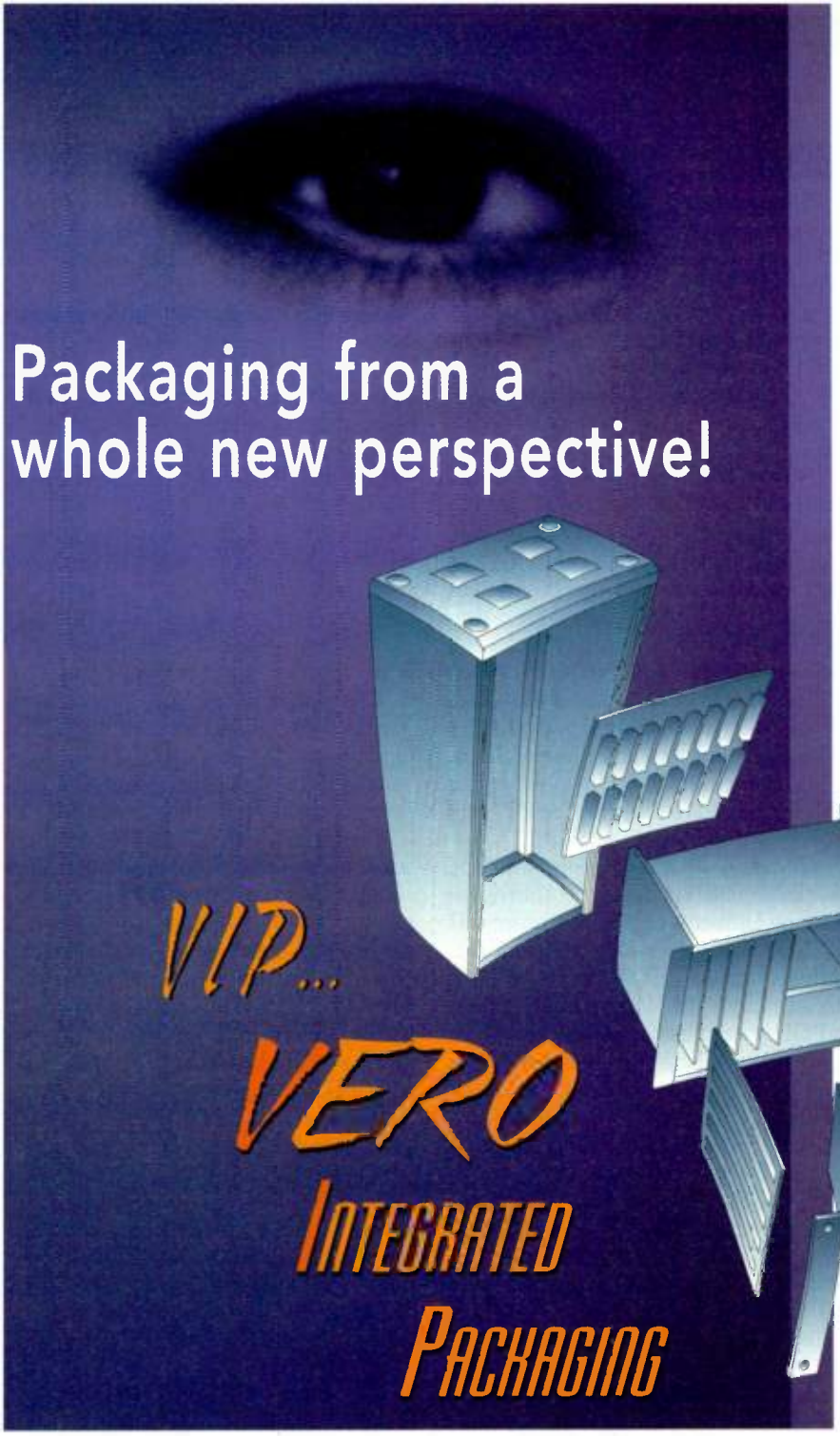
3. The Universe II, Tundra Semiconductor's second-generation, PCI-to-VME bridge, is used by several VME board designs today. Tundra's vPCI technology won't be available until the company releases its third-generation Universe chip. In theory, if the proper protocols existed in VME, you could architect a vPCI system using the existing Universe chip. What's missing is the transaction-recognition scheme. Such a scheme is needed to let boards identify an incoming VME transaction as a PCI-originated signal.

At the heart of the Bustronic/Arizona Digital approach is the use of a stared bus configuration. Conventional backplanes are wired from slot to slot so that a given pin in each connector is stitched to the next connector, and so on down the backplane until all such pins are connected. Usually, there is a network of pull-up and pull-down resistors at each end of the bus. This type of bus acts like a transmission line with distributed inductance and capacitance. When the circuit boards are plugged in, their additional stub and circuit capacitance makes the bus act as a very-low-impedance transmission line with a very-slow propagation time. The fully loaded impedance can be as low as 25 Ω, with end-to-end propagation times of up to 8 ns for a 21-slot backplane.

Fully loaded buses have severe reflections and ringing that limit how fast they can go. Incident-wave switching (where the first voltage transition crosses the switching threshold) is impossible. The "termination networks" of pull-up and pull-down resistors do not begin to eliminate reflections because the drivers are unable to drive at the low levels of resistance needed to match the characteristic impedances and minimize reflections. The only way to reliably use such a backplane is to wait a sufficient amount of time for the multiple reflections to die down before using the signal. This is extremely slow and hurts performance.

While conventional VME backplanes "stitch" the bus from slot 1 to 2, then 2 to 3, etc., the VME320 runs a signal trace from slot 1 to slot 11, a separate trace from slot 2 to slot 11, still another trace from slot 3 to slot 11, etc., until all slots have been wired to the common point at slot 11 This means that all of the trace capacitance, the stub capacitance and the circuit capacitance, appears to be concentrated at slot 11 rather than distributed as in the conventional backplane. The result is that the equivalent circuit of the backplane is a simple, lumped, 200-pF capacitance—not a transmission line. When the circuit cards are added, the equivalent circuit doesn't change *(Fig. 2)*. Rather, it just looks like a larger, lumped capacitance. The signal waveforms are excellent, and can allow much faster data transfers.

Because the backplane acts as a lumped capacitance, the rise and fall times of the signals are very clean and



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mono-tonic—that is, they transition through the switching threshold without hanging or changing direction. This allows a much faster signaling protocol to be used, such as SST. With SST protocols, data is sent without waiting for the previous strobe to be acknowledged. Propagation time does not affect the speed at which data can be streamed. Only the skew on the data and strobe affect the transfer speed.

VME Over PCI

Along with 2eSST and support for VME320, Tundra intends to add another goodie into its Universe III interface chip. Tundra has crafted a scheme called VME-on-PCI (vPCI). This technology effectively lets boards in a VME backplane talk to one another as though they're PCI boards. This technology may put an end to the "bus wars" between VME and Compact PCI.

While there's little doubt that PCI has become the bus of choice for all types of microprocessor-based systems, it has a major stumbling block. To maintain the 33-MHz bus bandwidth that's specified by PCI, you have to keep the number of the loads on the bus to 10. A load, in this case, could be a chip or a connector. The slot limitations of PCI are particularly an issue for embedded applications, many of which require several I/O cards in the system. Part of the appeal of VME, in contrast, is its ability to have 21 slots in a system.

Because every major processor architecture links to PCI, most embedded boards—VME included—already have PCI on them as a local bus. vPCI allows you to run a local PCI bus on your CPU card. The Tundra chip with vPCI, for example, acts as a bridge to the backplane. vPCI maintains the command type for the protocol that's going across VME, and tells the destination PCI bridge that it's receiving a PCI transaction that originated someplace else in the system. The transaction is then translated back into a PCI transaction on the destination-board's local PCI bus.

To implement vPCI, Tundra is taking advantage of an extension capability that the VITA Standards Organization (VSO) put into VME's address modifier codes a few years ago. These codes describe what kind of transaction actually is taking place on the VMEbus. By having the capability to extend those and add more address modifier codes, the VME community can add increasingly more protocols.

Tundra is using these extended-address-modifier (XAM) codes to map PCI transactions onto the VMEbus. The codes let the destination card know when a transaction is PCI-originated, and converts that into an equivalent PCI transaction on the local bus. "There's no new technology here," admits O'Connor, "We just have to settle on which XAM codes mean what."

System designers can reap all the software compatibility benefits of PCI, and also enjoy the reliability and 21-slot count of VME. That technology is proven in terms of protocols and data integrity. Meanwhile, any operating system that is PCI-aware (virtually all of them these days) can deal with a vPCI system as if it were a pure PCI system. To the operating system, the vPCI silicon looks just like a PCI-to-PCI bridge. So, VME just becomes a fabric, and you're transporting PCI protocols over the top of that fabric.

Tundra's vPCI technology won't be available until it releases its third-generation Universe chip. The Universe II is its second-generation PCI-to-VME bridge. In theory, if the proper protocols existed in VME, you could design a vPCI system using the existing Universe chip. What's missing is the transaction-recognition scheme. Such a scheme is needed to allow boards to identify an incoming VME transaction as a PCI-originated signal.

Tundra's Universe III will incorporate the new VME protocols—2eVME and 2eSST—as well as put in the foundation for engineers to be able to build vPCI systems. Tundra already has talked to a number of systems and CPU board companies about the technology, and it's been well-received.

vPCI also has implications for fault tolerance. It links the hardware live-insertion technologies of VME with the software live-insertion efforts of the WindowNT server world. Compaq Computer, Austin, Tex., and Microsoft, Redmond, Wash., have been working on schemes to do live insertion on boards in PC servers. As a consequence, an upcoming version of Windows NT will be able to recognize a live-insert or a live-withdrawal event.

By linking to PCI, vPCI opens the door to using Intelligent I/O (I_2O) on a VME backplane. I_2O provides an I/O device-driver architecture that is independent of both the specific device being controlled and the host operating system. It logically separates the portion of the driver that's responsible for managing the device, from the specific implementation details of the operating system that it serves. I_2O also acts to hide the nature of the communication between various mechanisms, and in doing so, provides processor and bus-technology independence.

Because I_2O uses PCI as its communications layer, you can use I_2O on anything with PCI. If system designers have two I_2O-equipped vPCIs with or without intelligence other than I_2O-messaging capability, they could talk to each other inside the vPCI system without any support needed from the host processor. Such I_2O-capable boards would be able to take over VME bus mastership, and send messages back and forth while the host CPU does something else further downstream.

For anyone who has followed the bus/board industry for a while, there's a strange irony in the message-passing aspect that I_2O brings to VME via vPCI. Message-passing was the heart of the Multibus II bus architecture. For years, Multibus II and VME competed for design wins. While Multibus II has an established base of users, there's been little activity there for years.

Like Compact PCI itself, vPCI is another example of what seems like a new sensibility in the board market. It makes more sense to ride an evolutionary wave, leveraging existing technologies, than to jump to some radical new scheme. vPCI exemplifies this trend by combining the benefits of older and well-established VME with younger, yet ubiquitous, PCI.

It's clear the the entire world of embedded computers is growing. Other segments may even grow faster than VME, but VME isn't going away anytime soon. With VME in so many applications—military in particular—it has such a history and investment, that it's guaranteed many years of success.

"Who can say what VME will be like in about 50 years, but in a decade, VME will certainly be around," says Lynn Patterson of Ixthos. "The fact that they're doing VME320 and faster shows that it's not sitting on its laurels. It's working to stay alive as a real technology," she adds.

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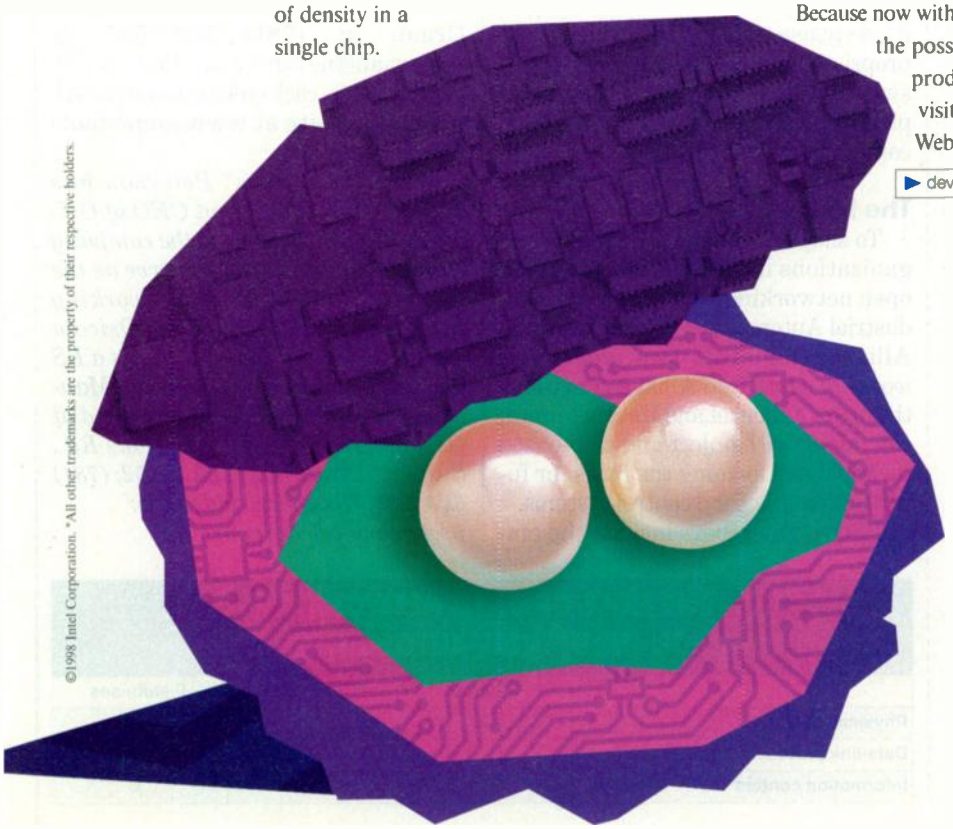


intel

STANDARDS WATCH

Open Networking Fuels The Next Major Advancement In Industrial Automation

Cornelius "Pete" Peterson, President, Embedded Networking Solutions Division, Osicom Technologies, Inc.

The migration of devices onto networks will have a great impact in people's lives in the next five to 10 years. No where will this be more true than in industrial automation. This area will evolve from rigid command and control centers, dominated by proprietary control networks, limited device intelligence, and control schemes, to an environment of open networking. Here, the intelligence moves to devices, which operate automatically without human intervention.

How will this happen? Through open networking. Just as the convergence of the common transmission protocols associated with the Internet (TCP/IP) and LANs (Fast Ethernet), along with the web as the common interface, facilitated the extensive open networking of PCs, the same convergence will come into play for the larger market of embedded devices.

Currently, we're in the fourth stage of information technology (IT) expansion, which began with mainframes, progressing through minis, PCs, and now the Internet for the general public. The next stage will see the Internet moving to devices on the network, all operating independently. This stage will be 1000× bigger than the fourth stage, which was 1000× bigger than the third stage, etc. And the fifth stage will happen twice as fast as the fourth, which happened twice as fast as the third, etc. As a result, network-ready devices will be available in just a few years, compared with the 15 years it took for manufacturing automation to evolve to the third-generation, PCs.

Industrial Automation Vision

In industrial automation, proprietary Fieldbus standards will merge with open networking. Ethernet hardware, media-access-control (MAC) topology, and the data carrier protocols of TCP will comprise the data communications infrastructure, while Fieldbus objects will continue to supply information and control content as they do now. Accordingly, the richness of Fieldbus will be preserved, transmitted over the Ethernet and TCP, and made accessible via web-based management *(see the table)*.

OEMs are now turning to their designers to integrate open networking hardware and software into their devices. Within the next two years, industrial automation designers will have network-enabled their devices, and begun to move basic intelligence to the devices themselves.

Some opponents downplay Ethernet as the backbone for control networking, but progress is underway. Due to its low cost, multivendor support, and easy migration from 10 Mbytes to 1 Gbyte, every major manufacturer has some significant Ethernet effort in progress. Critics cite its lack of determinism, but with technological advances like 100-Mbit/s throughput, its response time is 5 ms, which is appropriate for almost all devices. And, if switching hubs are used with full-duplex 10/100BaseT wiring, operation becomes fully deterministic.

The IAONA Alliance

To shape this vision into reality, organizations interested in advancing open networking have formed the Industrial Automation Open Networking Alliance (found at: *www.iaopennetworking.com*). The Alliance envisions the use of Ethernet and Internet protocols, along with object and web-based technologies forming the basis for future automation and control systems.

IAONA members include the embedded networking division of Osicom Technologies; Automation Research Corp., Dedham, Mass., a leading market research firm focusing on industrial and enterprise automation; Performance Software, Black Canyon City, Ariz., a developer of embedded software for mission-critical systems; Hirschmann Network Systems, Stuttgart, Germany, a leading supplier of "industrial strength" networking products; Schneider Automation, Paris, France, a world leader in industrial control products; Object Automation, Santa Ana, Calif., an innovator in industrial automation software; JETTER PROCESS-PLC, Lugwisburg, Germany, a process control manufacturer; and Parker Hannifin's Compumotor Div., Cleveland, Ohio and Rohnert Park, Calif., a U.S. manufacturer of motion control equipment. Members intend to facilitate open networking by publicizing its benefits, overcoming barriers to implementation, and issuing recommendations to standards groups such as the IEEE.

The Alliance will hold its first conference at the ISA Expo 98 in Houston, Tex., Oct. 20, 1998, at 7:00 p.m. Anyone interested in discussing the issues and implementation alternatives for open networking is invited to attend. For more information, contact Nita DeGraan at (781) 398-4592 or ndegraan@netarm.com. For conference updates, click on Events on the Alliance Web site at www.iaopennetworking.com.

Cornelius "Pete" Peterson has served as president and CEO of Osicom/DPI since founding the company in 1984. He continues to serve as the president of Embedded Networking Solutions Div., a division of Osicom Technologies Inc. Peterson holds a BS and MS from the Sloan School of Management at MIT. He can be reached at Osicom/DPI, 411 Waverly Oaks Rd., Suite 227, Waltham, MA 02452; (781) 647-1234; His e-mail address is: ppeterson@osicom.com.

THE ROLE OF OPEN NETWORKING IN INDUSTRIAL AUTOMATION

	Ethernet	TCP/IP (Web)	Fieldbuses
Physical layer	X		
Data-link protocols		X	
Information content		X	X

VME Maintains Its Ironclad Position As A High-End Bus Architecture

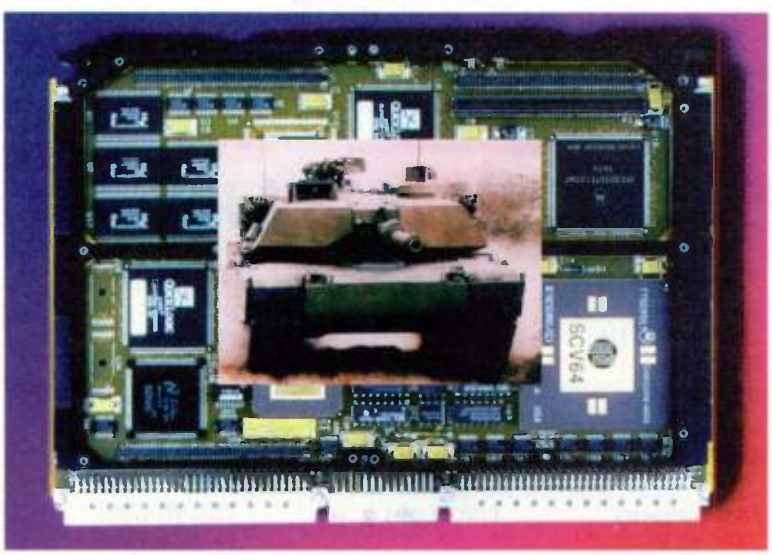
Its Heritage And Infrastructure Are Unmatched, And New Schemes Such As VME320 and vPCI Are Paving The Path To The Future.

Jeff Child

SPECIAL REPORT

Now in its 17th year, and still going strong, the VMEbus continues to dominate the high-performance, standard bus realm. While alternative bus architectures are displacing VME in some market segments, it's expected to enjoy continued respect and success. In military and avionics, it's expected to be the bus of choice for the next 10 years. Blessed with an effective and well-established trade association and standards body, VME has weathered a number of battles in its long history.

"VME is on a continuing evolutionary cycle," says Ray Alderman, executive director of the VMEbus International Trade Association. "And it's the only bus in history that's been able to do that. There are two basic reasons why," explains Alderman. "First, it's asynchronous, so every time we double the clock speed, we don't make all the old hardware obsolete. While some boards are running on edges, and some on levels, it's the backward compatibility that makes VME still a viable choice. That's why the military is all over it. Second, some of the brightest people in the world for the last 17 years have been working on VME," asserts Alderman.



Art Courtesy: DY-4 Systems Inc.

Early Momentum

A key reason for VME's success is the momentum it gained within the first five to 10 years of its existence. That momentum created a large pool of suppliers. VME fills a need in certain markets that would be hard to satisfy with any other current technology available today, which is why the defense industry and parts of the industrial market and telecom industry continue to embrace it. The telecom segment is under a bigger threat from CompactPCI than any other market segment.

As far as the defense industry is concerned, VME is the de facto standard because it's independent of any one vendor's core technology. It's independent of any processor, bus silicon, or operating system constraints. Unlike PCI, it's independent of market forces like the desktop PC. "That independence is how and why the standard has been so successful for those segments of industry that don't want to be constrained to tracking the desktop, or tied to one processor's or operating-system's paradigms," says Duncan Young, director of marketing, DY-4 Systems. "With VME," he continues, "you can run just about any operating system, and interface to just about anything you want. It's self-sustaining for now, but the technology has to move it forward."

Pushing Ahead

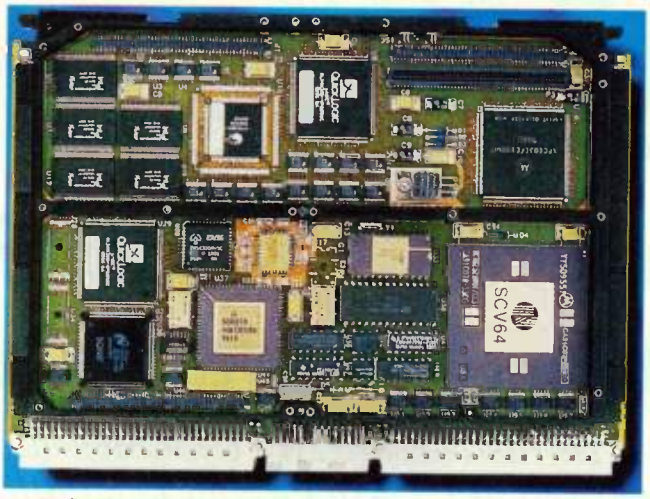
VME hasn't been standing still. Over its history, the VME community has evolved the specification. VME speed-ups started early this decade with the emergence of VME64, a protocol that allowed VME to run at up to 80 Mbytes/s. Over the past few years, there's been interest in moving to the new, high-

speed VME protocols under development *(see "VMEbus Protocol Keeps Edging Forward," p 62).*

First there was 2eVME, a protocol that increases VME bandwidth to 160 Mbytes/s. Now, there's work underway on 2eSST, which doubles that bandwidth to 320 Mbytes/s, with potential for 533 Mbytes/s, and perhaps even 1 Gbyte/s. Simultaneously, a clever scheme for sending VME transactions over PCI, called vPCI, is in the works.

Meanwhile, closer on the horizon, the VME64 Extensions Draft Standard, also known as VME64x, is beginning to reach critical mass, as board vendors implement several of the extensions. Helping to fuel that fire, connector vendor AMP Inc., has begun to sample its first five-row, 160-pin DIN connectors. Needed for VME64x, these connectors were, until now, only available from one vendor, Harting, Inc. AMP doesn't typically exert effort on this connector design unless there's a considerable volume demand expected. It's a good sign for VME.

VME64x is an extension of the VME64 standard, VITA 1-1994. It defines a set of features that can be added to VME and VME64 boards, backplanes, and subracks. The major new features defined in this draft standard include expanded 160-pin P1/J1 and P2/J2 connectors; an optional 95-pin, 2-mm hard metric P0/J0 connector for more user-defined I/O; 3.3-V and auxiliary power voltage; plus more 5-V power. The specification also incorporates 35 more signal ground returns, 46 more user-defined I/O pins on the P2/J2 connector, and 14 spare bused signal pins. Mechanical aspects of VME64x include support for EMC protection, ESD protection, solder side covers, an injector/extractor handle with locking, and board keying to specific subrack slots.



1. VMEbus boards, like the 200-MHz SVME/DMV-177 from DY-4 Systems depicted here, are designed to function in rugged industrial and military environments.

What drove VME DSP board vendor Ixthos to VME64x wasn't simply performance, but also a desire to use the five row pins and the 3.3-V power coming off the backplane. VME64x defines 11 new, 3.3-V pins (on the P1 connector.) With the last generation of VME cards, most designs drew all the power off the 5-V supply, and used onboard regulators to convert to all the other voltages they needed on board. Much more of the signaling is now 3.3 V and below, as IC technology advances. And, it's getting difficult to generate all of those diverse voltages off the 5-V supply.

Lynn Patterson, vice president of product development for Ixthos says, "it is a challenge to handle systems that use both 3- and 5-V supplies off the backplane. The VME specification doesn't define how power sequencing is handled—the sequencing of whether 3.3 or 5 V comes up first, or whether it's

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VMEBus Protocol Keeps Edging Forward

People in the VME user community as well as potential users are talking about the new, high-speed VME protocols under development. First there was discussion about 2eVME, a protocol that increases VME bandwidth to 160 Mbytes/s. Now there's talk about a new VME protocol, 2eSST, that doubles the bandwidth to 320 Mbytes/s, with potential for 500 Mbytes/s. There have even been rumors that 2eSST can go much higher.

How has VME, a 15-year-old technology, managed to continue to reinvent itself, and keep itself relevant while other technologies languish in the metaphorical trash bin of the embedded world? Simply put, VME started with a flexible protocol and well-designed environment that has enabled more performance and features to be integrated seamlessly as demands require.

VME speed-ups started early this decade with the emergence of VME64, a protocol that allowed VME to run at speeds up up to 80 Mbytes/s. Standard VME block transfers (or BLTs) are transactions consisting of an address phase followed by multiple data phases. During the data phases, the address lines sit idle. VME64 took advantage of this by putting another 32 bits of data on the unused address lines during the address phase, and created multiplexed block transfers (MBLTs) as shown in the figure *(a)*.

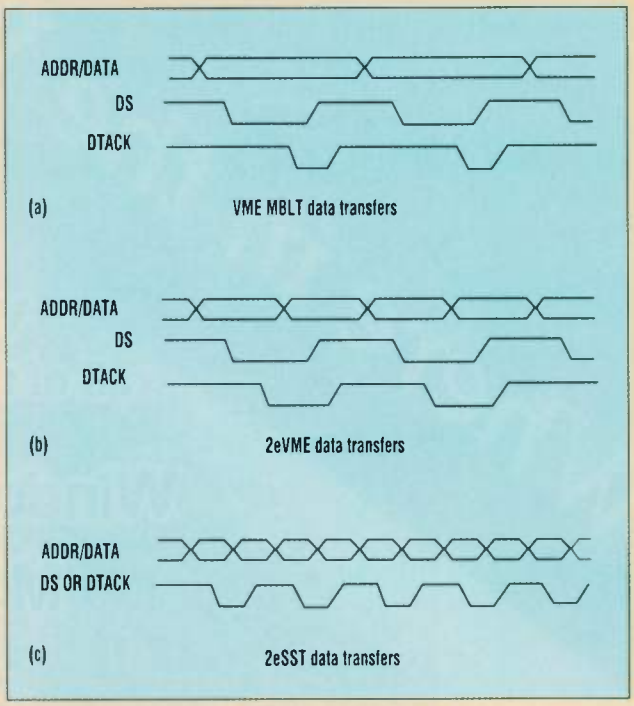
Today, those 80 Mbytes/s available with VME64 prove insufficient for routing huge amounts of Internet traffic, decoding infrared telemetry, or manipulating 3D images from CAT-scan equipment. To get more performance out of VME, 2eVME was developed. This protocol cleans up a current inefficiency in the MBLT protocol. Take another look at the protocol in the future: Data is put onto the bus and qualified by the master with a strobe (DS). The slave acknowledges the transfer with DTACK. Upon seeing the assertion of DTACK, the master negates its strobe, and in turn, the slave negates its DTACK, before the next data phase begins.

The inefficiency comes in the negation of those strobes. This transaction requires four-way signaling for the data transfer to be completed: assert strobe, slave responds with DTACK, master responds to DTACK with negation of strobe, and slave responds to strobe negation with DTACK negation.

Of course, a more efficient protocol would remove those last two transitions, or better yet, take advantage of them to transfer more data. This is what 2eVME, or 2-Edge VME transfers, does *(see the figure, b)*. It uses these negating edges to qualify an extra 64 bits of data. The overall frequency of the strobes remains the same as standard MBLTs, but now, twice as much data is being transferred. The result is a theoretical transfer rate of 160 Mbytes/s of bandwidth.

2eSST: Sourcing More Bandwidth

Not satisfied with just 160 Mbytes/s, the VME community worked on getting even more out of VME. The result was a modification of the 2eVME protocol to make it source-synchronous. Just as 2eVME doubled the throughput by getting rid of some of the handshaking, 2eSST increases it again, by getting rid of all the handshaking. There is now just a single strobe, with no acknowledgment from the receiver of the data. This is referred to as a "source-synchronous" transfer. Hence the name 2eSST, or 2-Edge Source Synchronous Transfers *(see the figure, c)*. The source of the data sends it at a predetermined maximum rate. The receiver must be capable of taking the data without relying on inserting wait states or throttling the throughput.



An Improved Backplane

There's a wrinkle to achieving higher performance with this protocol, however. The VME backplane, as it has electrically been defined in the past, maxes out at 160 Mbytes/s. After that, reflections aren't given enough time to settle out. To clean this up, a patented backplane technology called "VME320" is used. This new type of backplane uses a special routing technique to minimize the reflections, significantly improving the backplane speed. The combination of 2eSST and VME320 technology has doubled the VME bandwidth again to 320 Mbytes/s. But 2eSST doesn't stop there. The transfer rate of 2eSST is limited only by the skew in the system.

Special thanks to Rick O'Connor, director of business development at Tundra Semiconductor for his help with this article. For more information about VME standards go to the VITA web site at www.vita.com.

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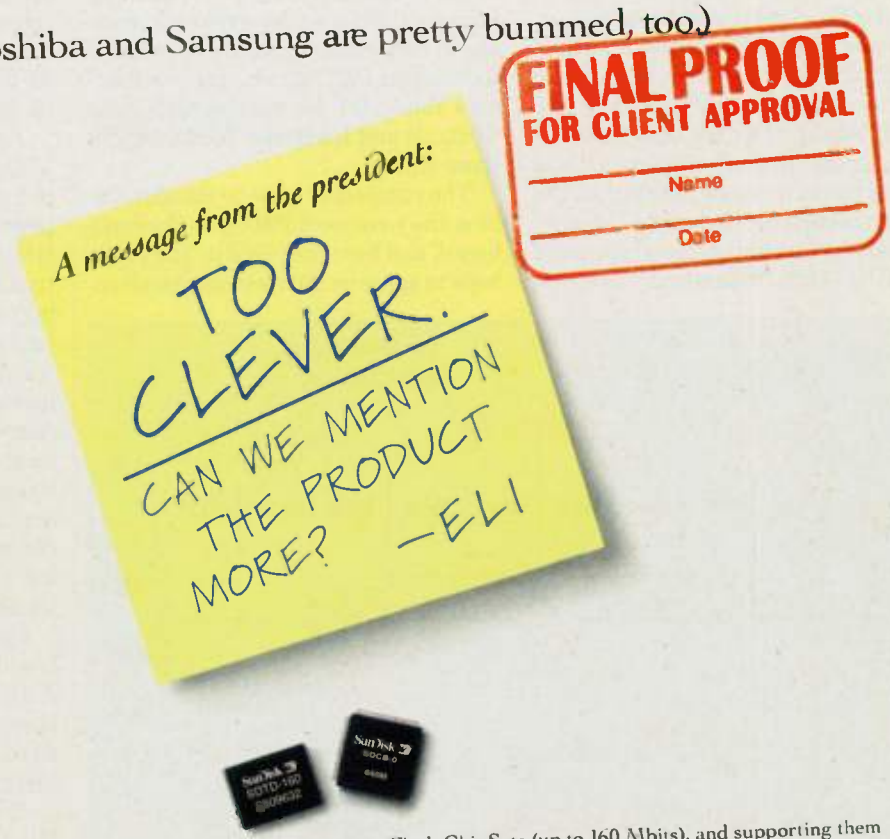

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just 5 V," she says.

"The timing between the two is also significant," Patterson continues, "If you draw the power right onto your board with no protection, you can have parts of your board turning on before others, and you slowly damage your cards." With that in mind, Ixthos added circuitry to its VME64x boards to monitor the power up of the different voltages on the backplane. "The circuitry lets them turn on power to the card under our control, rather than control of the power supply," she adds.

DY-4 Systems, a maker of conduction-cooled VME boards for military applications, has implemented most of the extensions, but not all of them *(see Fig. 1 and the opening illustration)*. Not all of them are applicable to conduction-cooled cards. "We've used the five-row, P1 and P2 connectors, and we use the P0 connector on VME64x," says DY-4's Young. "That's a significant advance for us. On conduction-cooled and rugged cards we need to bring all the I/O out through the backplane," he says.

VME 64x includes the adoption of the IEEE 1101.10 standard. It's a new front panel that also includes polarizing keys. Conduction-cooled cards don't use the same front panel, but instead use one with a slightly smaller overall profile than a VME card. "That means we can't implement a polarizing mechanism that is used on VME 64x," says Young. A new VITA working group has formed to provide an alternative method for keying a conduction-cooled card. DY-4 and Harting are developing a slightly different keying method for conduction-cooled cards, which involves polarization around the P0 connector. It's expected to be completed this year.

DY-4, along with a number of other companies, is also working on a conduction-cooled, PCI Mezzanine Card (PMC) standard. "We're essentially taking a PMC module, conduction cooling it, and trying to retain as much of the existing PMC standard as possible," says Young. DY-4 is working with Vista Controls and Radstone Technology in these efforts.

The companies hope to standardize how they connect PMCs to the base board, and how they cool it. They also hope to agree on the thermal characteristics, and how they're measured. Also, they're working on additions to that specification to cover higher-powered PMC modules. "You find quite a lot of commercial PMC vendors that already exceed 7.5 W by a considerable margin," says Young, "We're looking at added thermal interfaces on the conduction-cooled standard to allow that to happen."

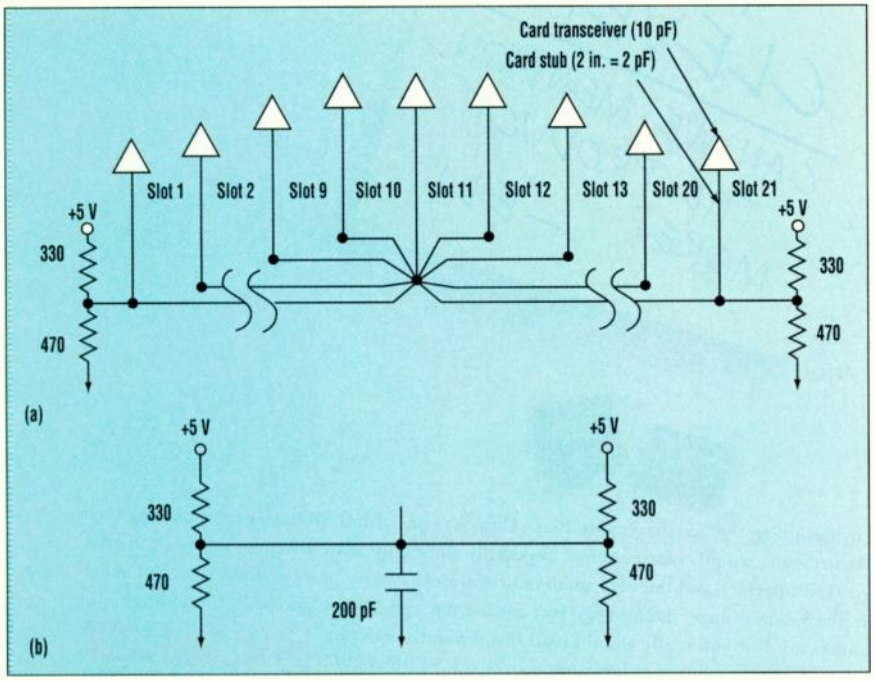
While VME64x gains momentum, the next evolution of VME, 2eVME, doesn't seem to be gathering steam. As part of the VME 64 Extensions draft standard, 2eVME increases available VMEbus bandwidth by reducing the number of handshake signals per transfer from four to two. With a two-edged protocol, signaling information is transferred across the backplane only twice. This cuts the total time in half for each 64-bit data transfer—resulting in double the bandwidth.

Last year, the number-two player in VME, Force Computers, rolled out the industry's first VME board that supports the 2eVME standard. The board is the first to do faster than 100-Mbyte/s transfers on a VME backplane. According to Force, the benefit of 2eVME is its better utilization of the VME bandwidth. Many systems have lots of bus masters, and they can get close to bus saturation. 2eVME frees them up to allocate more processor bandwidth to the application, also get a lot closer to implementing bandwidth-hungry applications. Such applications include moving ATM cells, high-bandwidth graphics, and video across the bus.

Called Sparc CPU-20VTe, the new board uses Force's own Sbus-to-VME ASIC, the FGA-5100. The chip combines the capabilities of the 64-bit Sbus and 2eVME. The combination of the 25-MHz, 64-bit Sbus and the 2eVME protocol results in an I/O bandwidth of 110 Mbytes/s. The board is compatible with Sun's SPARCstation 20 workstations.

The 2eVME protocol is not completely compatible with earlier forms of VME. It can talk to slower boards, but not at the 2eVME rate. Boards that participate in the protocol need enhanced transceiver logic (ETL). The board can, however, participate with other boards to complete transfers, block transfers, and perform multiplexed block transfers (MBLTs.)

According to Force, the Sparc CPU 20VTe is compatible with the new



2. While conventional VME backplanes "stitch" the bus configuration, the VME320 backplane runs signal traces in a star configuration (a). This means that all of the trace capacitance, stub capacitance (typically 2 pF per 2 in.), and circuit capacitance appear to be concentrated at slot 11, rather than distributed as in the conventional backplane. The result is that the equivalent circuit of the backplane is a simple, lumped 200 pF capacitance—not a transmission line (b). When the circuit cards are added, the equivalent circuit doesn't change. Instead, it just looks like a larger value of lumped capacitance, for example, 450 Pf. The signal waveforms are excellent, and can allow much faster data transfers.

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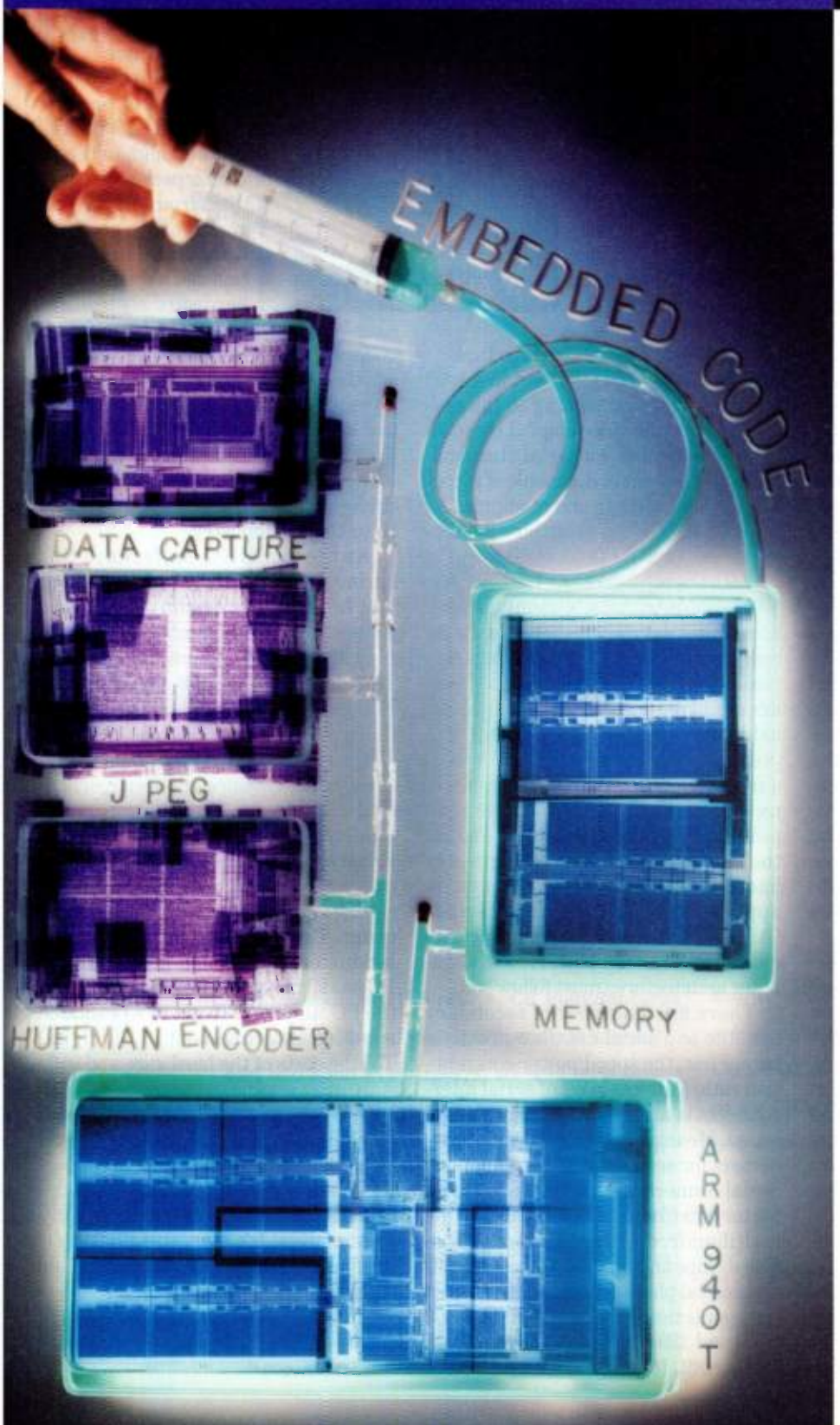

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WHAT'S ON BOARD

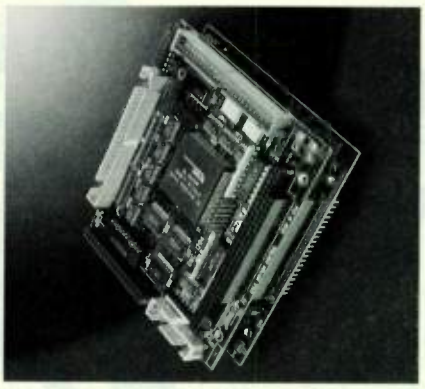
To help designers evaluate their miniature VGA-resolution, gray-scale display, The MicroDisplay Corp., San Pablo, Calif., has created an evaluation kit for the 0.5-in.-diagonal display. The MD640G1 MicroMonitor provides a 640-by-480-pixel display that has a 50:1 contrast ratio in direct view using ambient light and a viewing angle of up to 160°. The 50:1 contrast ratio is the highest value to date for a reflective miniature display. The display typically consumes less than 15 mW, and can run gray-scale video at a frame rate of 30 Hz. The display in the evaluation kit comes mounted on a full-size pc board that allows access to all signals. The board also includes a VGA feedthrough output so that designers can view the images or video on a full-size monitor simultaneously with the MicroDisplay. The display itself can be removed from the board to allow designers to test the mechanical characteristics of the chip-sized display in eyepieces, viewfinders, and other configurations. For applications that require more light than available in ambient conditions, or where dedicated lighting must be used, the MicroDisplay will appear uncommonly bright due to the 85% fill factor of the display patterning. In comparison, most transmissive displays have a fill factor of approximately 35%, because the light must pass through the material. The evaluation kit sells for $999, and is immediately available. Contact the company at (510) 243-9515; *www.microdisplay.com.*

A field-programmable timing generator, the FS6370, allows last-minute factory configuration, eliminating the need to stock devices with preset frequencies. Developed by American Microsystems Inc., Pocatello, Idaho, the CMOS device is part of a larger timing-generator product family. It incorporates three on-chip phase-locked loops that can each be independently programmed so that the chip can deliver the desired frequency outputs. From a single clock input, the chip can deliver four output frequencies. The outputs can be set independently by programming the desired bits into an on-chip EEPROM that controls the divide ratio of the PLLs. A Select input pin allows one PLL frequency and two multiplier/post-divider combinations to be easily modified by a logic-level input. The clock generator can provide timing for PC motherboards, 100-MHz SDRAM DIMM buffers, RAMbus timing generators, and other systems. Once the desired frequencies are established during prototyping and beta testing, a lower-cost ROM-based chip can be substituted to reduce manufacturing cost. In lots of 25,000 units, the FS6370 sells for $1.75 apiece. Other timing generators in the family offer from one to five outputs, and sell for $0.57 to $1.75 apiece in similar quantities. Contact Joe Gallagher at (208) 233-4690; *www.amis.com.*

A family of low-power pipeline-burst static RAMs developed by Mosys Inc., Sunnyvale, Calif., offers the lowest power consumption compared to any comparable product, according to the company. Available in several organizations—64 kwords by 64 bits, 256 kwords by 32 bits, and 128 kwords by 32 bits—the memories are based on the company's proprietary, single-transistor SRAM cell. That cell trims the memory array area by 75%, against standard SRAM cells, and trims power consumption by 80% to 90% versus standard PBSRAMs. The lower power drain and smaller area makes the MC80364K64, 80364K32, and 803128K32 very cost-effective in notebook and subnotebook computers, and other low-power applications. The memories also include a sleep mode that helps to further extend battery life. The 64k by 64 device is housed in a 128-lead, space-saving LQFP that measures just 14 by 20 mm—about 50% smaller than the board area required by standard 64-k-by-32-bit PBSRAMs. Although the memories are low power—just 50 mA when operating from a 3.3-V supply, and dropping to as little as 1 mA when placed in sleep mode—they can operate in systems with clock speeds of 133 and 166 MHz. Samples of the memories are immediately available. In high volumes, the MC30364K64 sells for $7 apiece, while the MC803128K32 goes for $5 apiece. Flow-through versions will also be available later this quarter, and both 8- and 16-Mbit capacities will be released in late 1999. Contact Andre Hassan, (408) 731-1826; *www.mosys.com.*

Eight-Axis Motion Controller Fits Into Small Spaces

Applications using motion control electronics come in all shapes and sizes. For those that need a small form factor, Galil Motion Control's DMC-1 200 Series of motion controllers are now available in multiaxis for the PC/104 bus. They come in 1- through 8-axis formats, which enables control



of both step motors and servomotors on any combination of axes.

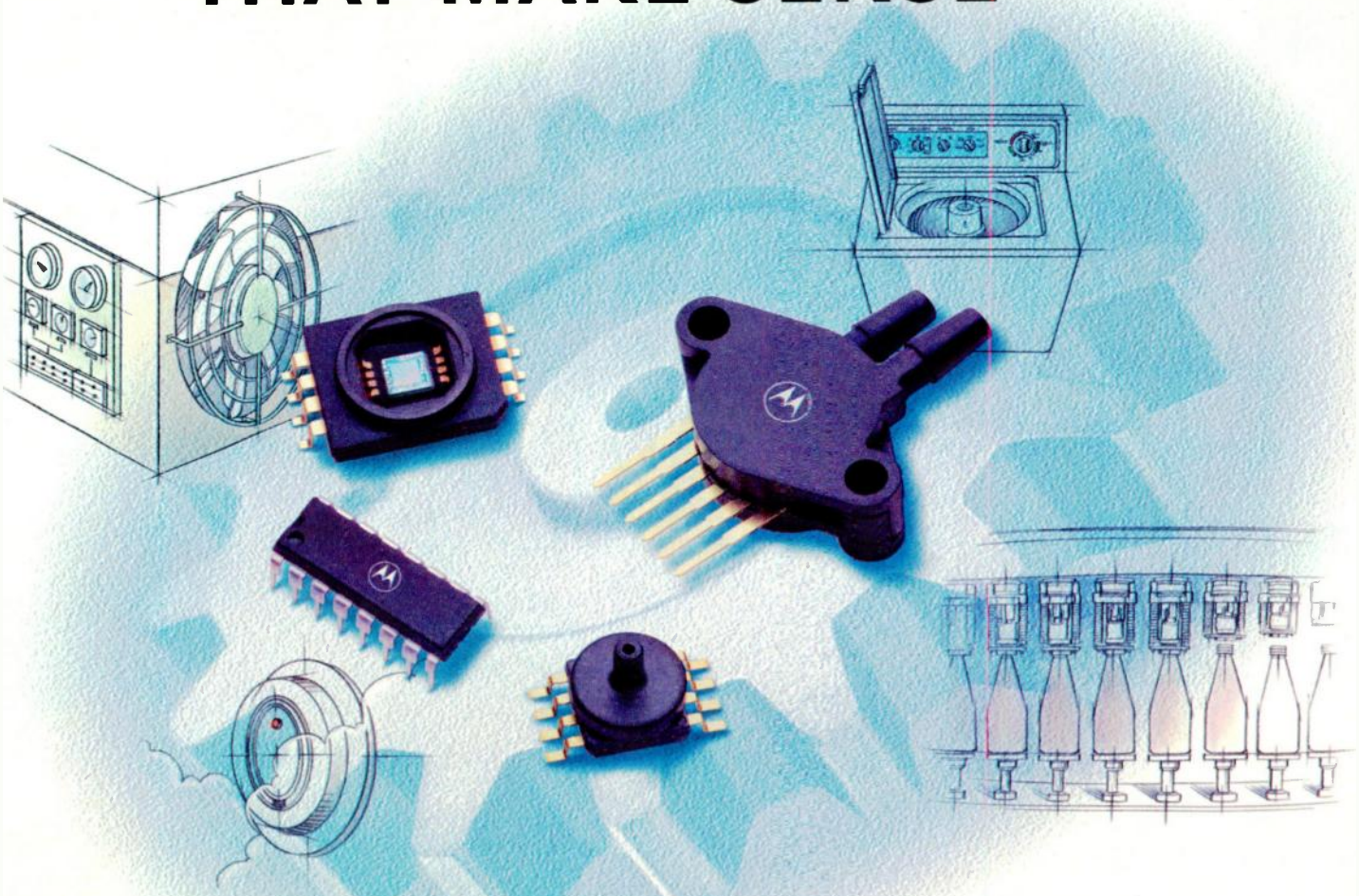
Because of their small 4.4 in. by 4.15 in. size, DMC-1200 controllers are ideal for applications where all of the electronics need to be embedded within a compact area. Such applications include semiconductors, medical equipment, and other applications that demand multiaxis, coordinated motion within limited space. The series consists of the DMC-1210 through DMC-1240, which support 1-4 axes controllers comprised of two stacked cards; and the DMC-1250 through DMC-1280 supporting 5-8 axes controllers consisting of three stacked cards.

The DMC-1200 includes such high-performance features as linear and circular interpolation, contouring, and electronic gearing. Nonvolatile memory provides permanent storage for custom application programs, variables, and arrays. Multitasking of up to eight programs permit numerous motion and PLC events to run concurrently.

Pricing for the DMC-1240 is $2195 for a four-axis controller in single quantities, and $995 for quantities of 100.

Galil Motion Control Inc., *203 Ravendale Dr, Mountain View, CA 94043; (800) 377-6329; fax (650) 967-175; www.galilmc.com.* **CIRCLE 453**

SENSING SOLUTIONS THAT MAKE SENSE



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In 1983, Galil introduced the first digital, single-axis motion controller without tachometer feedback.

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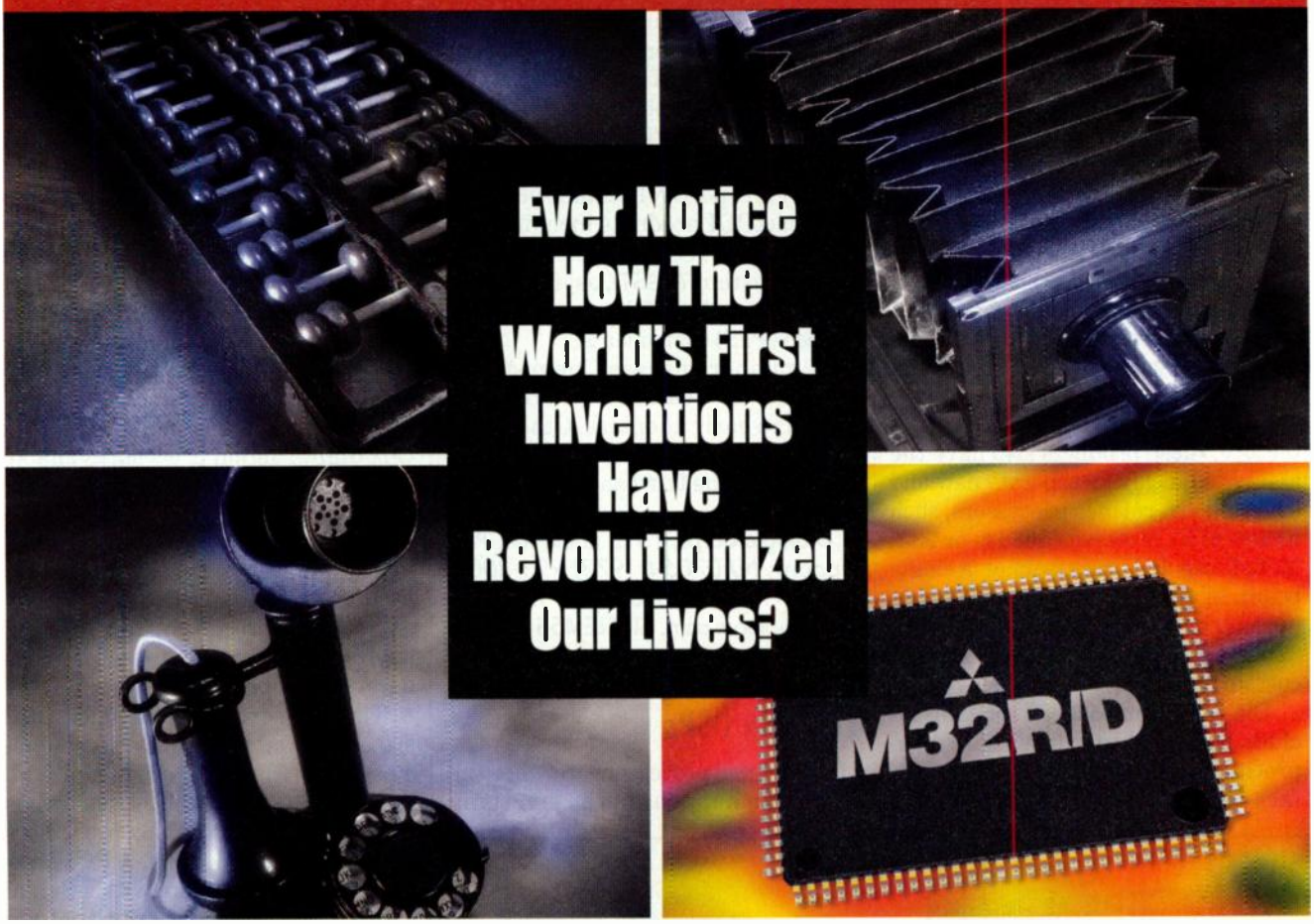
READER SERVICE 133

World's First RISC Processor With Large DRAM On A Single Chip.



32-bit RISC CPU core (52.4-80MIPS@66.7-100MHz) with 2 Mbytes of embedded DRAM

Single-cycle DSP functionality on-chip

High-speed processing using ½ typical power consumption

128-bit wide, 66.7 MHz internal bus optimizes CPU-to-memory data transfer

Industry-standard embedded real-time operating system porting enhances code development

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READER SERVICE 127

Technology Integration For Emerging Applications℠

Line Of Compact PCI Telephony Boards Roll Out

Open-architecture computer telephony systems continue to be the fastest growing segment of the telephony market. Such systems have harnessed the advances in PC hardware and software technology, as well as the latest advances in DSPs. The Compact PCI bus standard is at the center of this trend.

Feeding this monster market,Dialogic Corp., has announced the roll out for the company's CompactPCI products. Based on the Dialogic DM3 architecture, these products also have the ability to quickly incorporate new and leading-performance processors, such as 100-MHz Motorola 56303s or 233-MHz PowerPC processors on a single board. In addition, Dialogic will be supporting the Texas Instrument TMS 320C6x DSPs in the near future for custom development programs.

Dialogic's CompactPCI solutions include the QuadSpan series of voice-processing and digital network interface products with four spans of T-I/E-1 network interface and up to 120 ports of voice processing in a single slot; the DM3 IPLink, a fully H.323 compliant IP telephony gateway platform; and the DM/F240 and DM/F300 offering 24 and 30 channels of fax processing, respectively. Other plans for CompactPCI products include automatic speech recognition (ASR), Signaling System 7 (SS7), asynchronous transfer mode (ATM), and text-to-speech (TTS) components.

A number of these CompactPCI products and features have been released to early adopters. Others will become available to customers throughout the third and fourth quarters of 1998.

Dialogic Corp., *1515 Route Ten, Parsippany, NJ 07054; (973) 993-3000; fax (973) 993-3093; Internet: www.dialogic.com.* **CIRCLE 455**

CompactPCI Board Serves Up Four C6x DSPs

Digital signal processors are where all of the fun happens in the emerging Compact PCI/telecom revolution. Blue Wave Systems recently announced a Compact PCI board, the CPCI/C6400, that offers up to four Texas Instruments TMS320C6201 (C6x) processors, network interfaces, and a dedicated real-time system controller in a single slot. The architecture of the CPCI/C6400 is optimized for resilient multichannel processing, such as modem pools and transcoder banks that can be used in Voice over IP applications and cellular radio base stations.

Up to four independent, 200-MHz C6x digital signal processors enable designers to apply peak processing power of 6400 MIPS to multiple voice or data channels in parallel, using minimal system volume. The board sports up to 16 Mbytes of SDRAM for each digital signal processor along with 512 kbytes of zero-wait-state synchronous burst SRAM per DSP.

The two serial ports of each DSP are connected to a Lucent Technologies T8100 Timeslot Assigner, providing an H.110-compliant telephony bus interface between the C6x processors and a H.110 timeslot bus. A PCI Mezzanine Card (PMC) site with a Signal Computing System Architecture (SCSA) compatible connection to the T8100 time-slot assigner provides for modular system expansion. This enables designers to add a dual or quad T I /E I network interface PMC module to achieve a high-density voice-processing unit that can process up to 128 ports in a single slot.

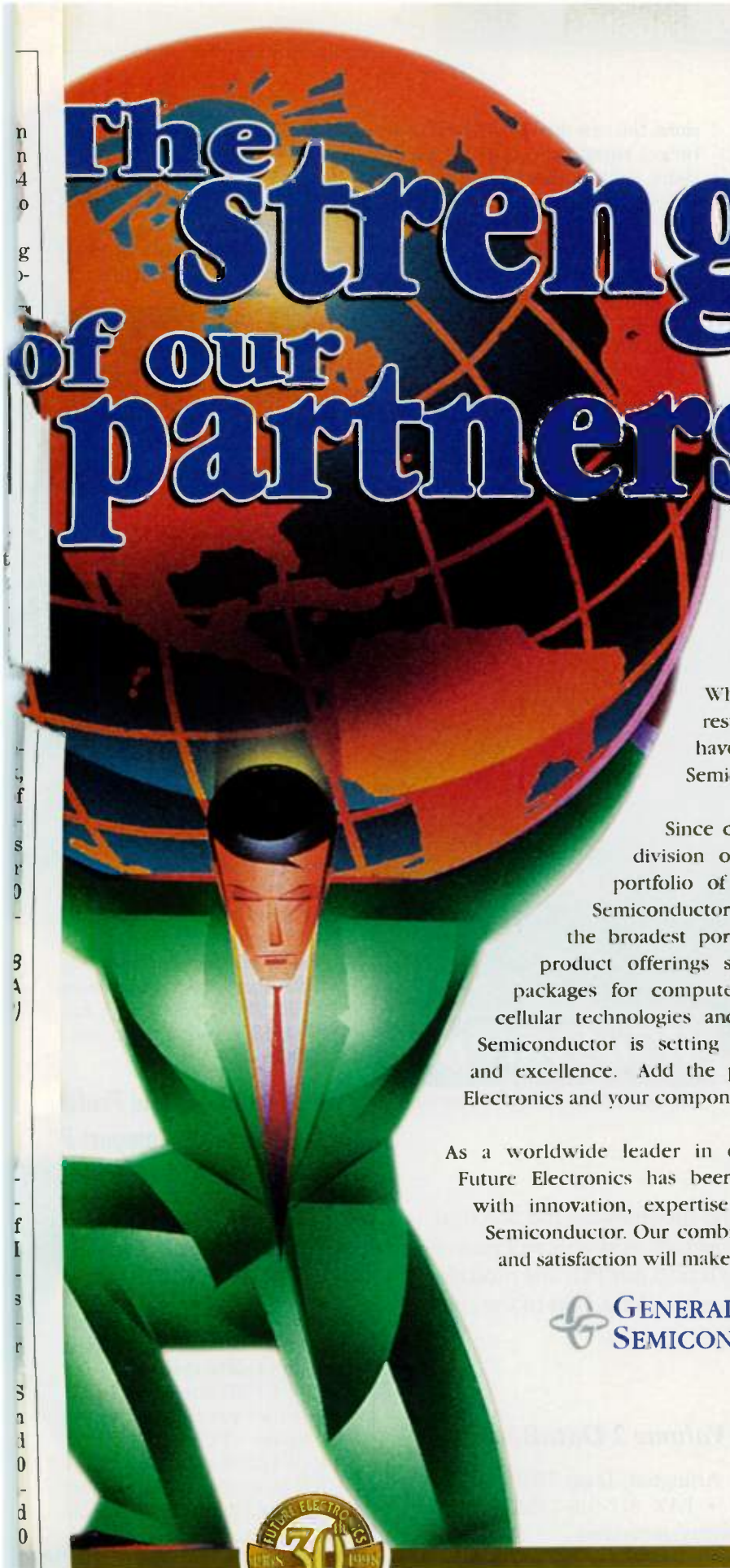
A Motorola MPC860 PowerQUICC processor provides real-time, onboard control, signaling, and data management independent of the host. A range of operating systems are supported, including Windows NT and Solaris 2.x systems. Prices start at $2000 for OEM quantities.

Blue Wave Systems Inc., *2410 Luna Rd, Suite 132, Carrollton, TX 75006; (972) 277 4600; fax (972) 277 4666; www.bluews.com.* **CIRCLE 456**

Dual 450-MHz Pentium IIs Available On Compact PCI

The days are long gone when RISC processors lead the performance race. It's even debatable whether Pentium-class CPUs are technically CISC or

(continued on page 80)



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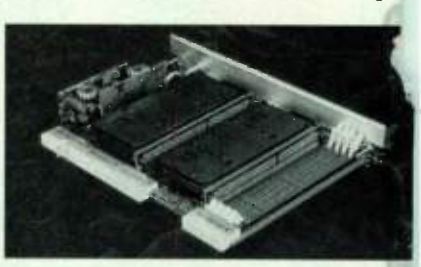
READER SERVICE 132

(continued from page 78)
RISC these days. Pentium II Dechutes processors are available at speeds of 450 MHz. By packing two of these processors with 1 Gbyte of memory on a two-slot 6U VME64 or CompactPCI board,General Micro Systems can claim to have the industry's fastest single-board computer. Available in both VME64 (named V2P2) and CompactPCI (named C2P2) versions, the new dual-Pentium II boards target compute-intensive applications, such as telecommunications, aerospace, and imaging.

The boards offer 1 Gbyte of main memory, and a 1 Mbyte of L2 cache. They also incorporate Intel's 82443BX and the 640 Advanced Graphics Processor (AGP). The boards provide a 100-MHz implementation of Intel's FSB (Front Side Bus), a high-performance local bus that connects Pentium II processors with cache and mai memory. It also sports the DEC 215 Draw Bridge Chip on CompactPCI t allow for multiprocessing.

In addition to its raw processin performance, the V2P2 and C2P2 pr



vide an array of I/O and networking options. Included are dual Etherne interfaces (twisted pair) operating a either 10 Mbits/s or 100 Mbits/s, a 40 Mbyte/s Ultra Wide SCSI interface with auto termination, and a 64-bi AGP graphics engine with eig Mbytes of video RAM optimized fo 3D rendering.

For applications that must be de ployed without a rotating hard disk the boards also provide 72 Mbytes o M-Systems' Disk-On-Chip flash mem ory (M-Systems) and up to 750 Mbyte SanDisk 1.5-in. Flash IDE. Pricing fo the V2P2 and C2P2 starts at $720 with 0.5-Gbyte memory and two 400 MHz Pentium-II processors.

***General Micro Systems Inc.**, 835 Maple Place, Rancho Cucamonga, C 91730; (909) 980-4863; fax (909 987-4863; www.gms4vme.com.*

CIRCLE 457

Intelligent CAN And Profibus Take A Ride On Compact PCI

The Compact PCI standard is start ing to see products supporting spe cialized I/O interfaces. The latest o these are two new Compact PC Fieldbus controllers for industrial au tomation applications. The CP350 i an intelligent CAN controller de signed to communicate with othe master or slave systems.

The CP351 intelligent PROFIBU controller provides a link betwee Compact PCI computers an PROFIBUS networks. The CP35 CAN controller is available with sin gle or dual independent optoisolate interfaces.. The on-board SJA100

(continued on page 82)

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- Prototypes in two weeks
- J.I.T. delivery

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- 200K - 1 Million Hrs. MTBF
- 120 - 700 Watts
- 1 - 4 Outputs
- Low Cost

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POWER PRODUCTS

VR SERIES HI-REL SWITCHERS

Single Output • 300-700 Watts

DESCRIPTION

VR Series World Class switching power supplies are a family of single output models designed for applications requiring ***Ultra Reliability*** and ***Low Cost!*** These supplies have actual demonstrated MTBF ratings up to 1 million hours. The time tested design has been continually updated to take advantage of the latest technological improvements in circuits and components resulting in the fine performance of these supplies.

MODELS & RATINGS

Max Power	Output	Model
300W	5V @ 50A	VR300AXX
	12V @ 25A	VR300BXX
	15V @ 20A	VR300CXX
	24V @ 12A	VR300DXX
	48V @ 6A	VR300EXX
500W	5V @ 80A	VR500AXX
	12V @ 40A	VR500BXX
	15V @ 30A	VR500CXX
	24V @ 20A	VR500DXX
	48V @ 10A	VR500EXX
700W	5V @120A	VR700AXX
	12V @ 58A	VR700BXX
	15V @ 46A	VR700CXX
	24V @ 29A	VR700DXX
	48V @ 15A	VR700EXX

FEATURES

- *UL, CSA, TÜV (IEC, EN), CE.*
- *5.5 watts per cubic inch.*
- *80% typical efficiency.*
- *1,000,000 hrs. demonstrated MTBF.*
- *Stock delivery.*
- *Full complement of options.*

VR OPTIONS

Option Code	Function
00	None
01	Power Fail Monitor
02	Auto Ranger
04	Pilot Bias
08	Screen Cover
16	End Fan Cover
32	Top Fan Cover

To order, replace "XX" in model number with sum of Option Codes desired.

CV SERIES ENCLOSED SWITCHERS

Single Output • 360-600 Watts

DESCRIPTION

The CV Series is a line of low profile, fan cooled power supplies which utilize Deltron's field proven V Series components. CV units are single output models in a rugged enclosed package nominally 3 inches in height and 5 inches in width. With power ratings of 360 to 600 watts, these units are a space saving alternative to 5 x 8 inch shoe box modules.

MODELS & RATINGS

Max Power	Output	Model
360W	5V @ 72A	CV360AXX
	12V @ 30A	CV360BXX
	15V @ 24A	CV360CXX
	24V @ 15A	CV360DXX
	28V @ 13A	CV360JXX
	48V @ 7.5A	CV360EXX
500W	5V @ 100A	CV501AXX
	12V @ 42A	CV501BXX
	15V @ 33A	CV501CXX
	24V @ 21A	CV501DXX
	28V @ 18A	CV501JXX
	48V @10.5A	CV501EXX
600W	5V @ 120A	CV601AXX
	12V @ 50A	CV601BXX
	15V @ 40A	CV601CXX
	24V @ 25A	CV601DXX
	28V @21.5A	CV601JXX
	48V @12.5A	CV601EXX

FEATURES

- *UL, CSA, TÜV (IEC, EN), CE.*
- *4 watts per cubic inch.*
- *80% typical efficiency.*
- *200,000 hrs. demonstrated MTBF.*
- *Heavy duty enclosed chassis.*
- *Full complement of options.*

CV OPTIONS

Option Code	Function
00	None
02	Power Fail Monitor
04	Thermal Shutdown
08	Logic Inhibit
16	Auto Ranger

To order, replace "XX" in model number with sum of Option Codes desired.

V SERIES OPEN FRAME SWITCHERS

Single & Quad Outputs • 120-600 Watts

DESCRIPTION

V Series World Class switching power supplies are a family of single and quad output models designed for a wide variety of commercial and industrial applications. These industrial workhorses have demonstrated MTBF ratings greater than 500,000 hours. A proprietary proportional drive circuit prevents excess switch saturation and permits higher switching frequency operation. This makes possible increased reliability and a compact size.

One of the unique features of the V Series is a dual loop regulation system. This system provides a tightly regulated main output and eliminates cross regulation in the auxiliaries.

FEATURES

- *UL, CSA, TÜV (IEC, EN), CE.*
- *4.8 watts per cubic inch.*
- *80% typical efficiency.*
- *500,000 hrs. demonstrated MTBF.*
- *High power auxiliaries.*
- *High peak current capability.*
- *Full complement of options.*

SINGLE OUTPUT

Max Power	Output	Model
120W	5V @ 25A	V120AXX
	12V @ 10A	V120BXX
	15V @ 8A	V120CXX
	24V @ 5A	V120DXX
180W	5V @ 36A	V180AXX
	12V @ 15A	V180BXX
	15V @ 12A	V180CXX
	24V @7.5A	V180DXX
250W	5V @ 50A	V250AXX
	12V @ 21A	V250BXX
	15V @ 17A	V250CXX
	24V @ 11A	V250DXX

Max Power	Output	Model
270W	5V @ 54A	V270AXX
	12V @ 22A	V270BXX
	15V @ 18A	V270CXX
	24V @ 12A	V270DXX
360W	5V @ 72A	V360AXX
	12V @ 30A	V360BXX
	15V @ 24A	V360CXX
	24V @ 15A	V360DXX

Max Power	Output	Model
500W	5V @100A	V501AXX
	12V @ 42A	V501BXX
	15V @ 33A	V501CXX
	24V @ 21A	V501DXX
600W	5V @120A	V601AXX
	12V @ 50A	V601BXX
	15V @ 40A	V601CXX
	24V @ 25A	V601DXX

Other voltages, e.g. 2V, 3.3V, 28V, and 48V available on special order.

QUAD OUTPUT

Max Power	Output 1	Output 2	Output 3	Output 4	Model
225W	5V @ 30A	+12V @ 6(12)A	-12V @ 4A	-5V @ 4A	V225AXX
	5V @ 30A	+12V @ 6A	-12V @ 4A	+24V @ 4(8)A	V225BXX
	5V @ 30A	+15V @ 6(12)A	-15V @ 4A	-5V @ 4A	V225CXX
	5V @ 30A	+15V @ 6A	-15V @ 4A	+24V @ 4(8)A	V225DXX
	5V @ 30A	+12V @ 6(12)A	-12V @ 4A	+12V @ 4A	V225EXX
300W	5V @ 40A	+12V @ 4A	-12V @ 4A	-5V @ 3A	V300AXX
	5V @ 40A	+12V @ 4A	-12V @ 4A	+24V @ 3(5)A	V300BXX
	5V @ 40A	+15V @ 4A	-15V @ 4A	-5V @ 3A	V300CXX
	5V @ 40A	+15V @ 4A	-15V @ 4A	+24V @ 3(5)A	V300DXX
	5V @ 40A	+12V @ 4A	-12V @ 4A	+12V @ 3(5)A	V300EXX
325W	5V @ 45A	+12V @ 8(16)A	-12V @ 6A	-5V @ 4A	V325AXX
	5V @ 45A	+12V @ 8A	-12V @ 6A	+24V @ 4(8)A	V325BXX
	5V @ 45A	+15V @ 8(16)A	-15V @ 6A	-5V @ 4A	V325CXX
	5V @ 45A	+15V @ 8A	-15V @ 6A	+24V @ 4(8)A	V325DXX
	5V @ 45A	+12V @ 8(16)A	-12V @ 6A	+12V @ 4A	V325EXX
400W	5V @ 50A	+12V @ 8A	-12V @ 8A	-5V @ 4A	V400AXX
	5V @ 50A	+12V @ 8A	-12V @ 8A	+24V @ 4(6)A	V400BXX
	5V @ 50A	+15V @ 8A	-15V @ 8A	-5V @ 4A	V400CXX
	5V @ 50A	+15V @ 8A	-15V @ 8A	+24V @ 4(6)A	V400DXX
	5V @ 50A	+12V @ 8A	-12V @ 8A	+12V @ 4(6)A	V400EXX
500W	5V @ 60A	+12V @ 10A	-12V @ 10A	-5V @ 5A	V500AXX
	5V @ 60A	+12V @ 10A	-12V @ 10A	+24V @ 5(8)A	V500BXX
	5V @ 60A	+15V @ 10A	-15V @ 10A	-5V @ 5A	V500CXX
	5V @ 60A	+15V @ 10A	-15V @ 10A	+24V @ 5(8)A	V500DXX
	5V @ 60A	+12V @ 10A	-12V @ 10A	+12V @ 5(8)A	V500EXX
600W	5V @ 80A	+12V @ 10(20)A	-12V @ 10A	-5V @ 5A	V600AXX
	5V @ 80A	+12V @ 10A	-12V @ 10A	+24V @ 5(10)A	V600BXX
	5V @ 80A	+15V @ 10(20)A	-15V @ 10A	-5V @ 5A	V600CXX
	5V @ 80A	+15V @ 10A	-15V @ 10A	+24V @ 5(10)A	V600DXX
	5V @ 80A	+12V @ 10(20)A	-12V @ 10A	+12V @ 5A	V600EXX

V OPTIONS

Option Code	Function
00	None
01	OVP protects all auxiliaries
02	Power Fail Monitor
04	Thermal Shutdown
08	Cover
16	Logic Inhibit
32	Post Regulator for output 4

To order, replace "XX" in model number with sum of Option Codes desired.

NOTES:

1. *Numbers in parentheses ( ) are peak ratings for short duration service such as motor starting.*
2. *Output 1 is floating and can be either polarity.*
3. *Quads require 10% of maximum power distributed among auxiliary outputs for optimum performance.*
4. *Outputs can operate to no load with slight increase in specifications.*

SPECIFICATIONS

INPUT
90-132 VAC or 180-264 VAC, 47-440 Hz.
Consult factory for 400 Hz. operation.

EMISSIONS
FCC 20780 Part 15/EN 55022, Class A Conducted.
EN 61000-3-3, Voltage Fluctuations.

IMMUNITY
IEC 1000-4-2/EN 61000-4-2, Electrostatic Discharge.
IEC 1000-4-3/EN 61000-4-3, Radiated Field.
IEC 1000-4-4/EN 61000-4-4, Electrical Fast Transients.
IEC 1000-4-5/EN 61000-4-5, Level 3 Surge.
IEC 1000-4-6/EN 61000-4-6, Conducted Field.

INPUT SURGE
17 amps peak from cold start for models up to 250 watts and VR300, 68 amps for other models, from nominal 110 or 220 VAC.

EFFICIENCY
80% typical.

HOLDUP TIME
20 milliseconds after loss of nominal AC power.

OUTPUTS
See table of models.

LINE REGULATION
±0.1% for line change from nominal to min. or max. rating with 20% min. load on the measured output.
±0.05% with post regulator and no min. load.
Singles to no load.

LOAD REGULATION

5V main/singles	±0.2%		
-5V aux.	±3%	**Post Regulated Outputs**	
±12V aux.	±2%	Option 32	±0.05%
±15V aux.	±2%		
+24V aux.	±1.5%		

for load change from 60% to 20% or 100% max. rating.
With post regulator to no load. Singles to no load.

CROSS REGULATION
±0.2% for load change on the main 5V output from 75% to 50% or 100% max. rating with 20% min. load on the measured output.
±0.05% with post regulator and no min. load.
Not applicable to singles.

CENTERING

5V main/singles		±5% trim adj.
Aux. 1 and 2		±5% trim adj. tracking
Aux. 3:	-5V	±3%
	+12V	±2%
	+24V	±1%

with all outputs loaded to 50% max. ratings and output #2 set precisely at its rated value. With post regulator ±3% trim adj.

RIPPLE & NOISE
1% or 100 mV, pk.-pk., 20 MHz bandwidth.

OPERATING TEMPERATURE
0-70°C. Derate 2.5%/°C above 50°C.

COOLING

Models	Forced Air
V120, V180, V225, V250, V270, V300, VR300, V360	30 CFM
V325, V400, V500, VR500, V501, V600, V601, VR700	60 CFM

TEMPERATURE COEFFICIENT

5V main/singles	±0.02%/°C
Auxiliaries	±0.05%/°C
With post regulator	±0.02%/°C

DYNAMIC RESPONSE
Peak transient less than ±2% or ±200 mV for step load change from 75% to 50% or 100% max. ratings.

RECOVERY TIME
Less than 400 microseconds on main/singles output.
Less than 50 microseconds on post regulated auxiliaries.

SAFETY
Units meet UL 1950, CSA 22.2 No. 950, EN 60 950, IEC 950.

DIELECTRIC WITHSTAND
3750 VRMS input to ground.
3750 VRMS input to output.
700 VDC output to ground.

SPACING
8 mm primary to secondary.
4 mm primary to grounded circuits.

LEAKAGE CURRENT
0.75 mA at 115 VAC, 60 Hz. input.

INPUT UNDERVOLTAGE
Proprietary proportional drive and low voltage lockout protects against damage for undervoltage operation.

SOFT START
Units have soft start feature to protect critical components.

OVERVOLTAGE PROTECTION
Standard on main output/singles. Optional on auxiliaries.

REVERSE VOLTAGE PROTECTION
All outputs are protected up to load ratings.

OVERLOAD
Outputs short circuit protected by current foldback with automatic recovery. Post regulators have individual current foldback protection.

REMOTE SENSING
On singles/5V mains which are fully isolated from all auxiliaries.

SHOCK & VIBRATION
Shock per MIL-STD 810-E Method 516.4, Procedure I.
Vibration per MIL-STD 810-E Method 514.4, Category 1, Procedure I.

MECHANICAL

MODELS	H	x	W	x	L
VR300	2.50"	x	4.85"	x	8.50"
VR500, VR700	2.75"	x	4.85"	x	10.50"
CV360, CV501, CV601	3.15"	x	4.85"	x	12.63"
V120, V180, V250	2.50"	x	4.75"	x	8.50"
V270, V360, V501, V601	2.50"	x	4.75"	x	10.50"
V225, V325	2.50"	x	5.00"	x	10.50"
V300, V400, V500, V600	2.75"	x	5.00"	x	13.00"

OPTIONS & ACCESSORIES

POWER FAIL MONITOR
Optional monitor provides a TTL signal 2 ms. min. prior to loss of output power with outputs fully loaded from 100VAC/200VAC line loss.

THERMAL SHUTDOWN
Special circuit cuts off supply in case of local over temperature. Unit resets automatically when temperature returns to normal. Standard on VR Series. Optional for CV and V Series.

COVERS
Optional end and top fan covers for VR Series.
Optional safety/EMI cover for V Series.

INHIBIT
TTL logic inhibit input. Standard for VR Series. Optional for CV and V Series.

PILOT BIAS
Optional for VR Series only. SELV 5V @ 1A source for external use with provision for operating the inhibit either with a switch or TTL Logic. Either NO or NC can be selected.

AUTO RANGER
Special circuit provides automatic operation at specified input ranges without strapping. Optional for VR and CV Series. For V Series specify AR-1 accessory.

POST REGULATOR
Optional for output #4 on V300, V400, V500, V600 models. Ratings available are -5V @ 4A, +12V @ 3A, or +24V @2A.

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(continued from page 80)
supporting transmission rates of up to 1 Mbaud. An on-board 40-MHz SAB C165 microcontroller manages all high-level protocol stack handling, relieving the system CPU of these tasks and ensuring high data throughput. The CP350 supports extended CAN protocol V2.08.

The CP351 PROFIBUS controller provides a high-speed (up to 12 Mbaud) interface to PROFIBUS networks. Master/slave, and DP master (class 1 and class 2) protocols are supported.

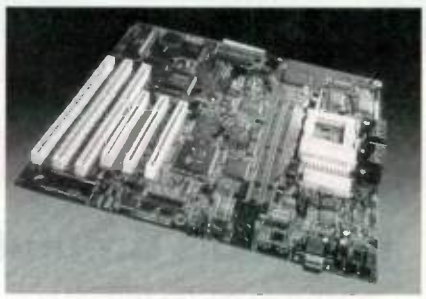
An ASPC-2 PROFIBUS controller on the board is responsible for PROFIBUS Layer 2 and most of the DP communications. A 25-MHz MC68360 microcontroller handles the remaining protocol stack functions. This ensures high data throughput and system performance and relieves the CPU of network chores. The CP351 provides 1000-V optoisolation between the controller and the Fieldbus interface. The CP350 and CP351 are designed to perform in the extreme temperatures of today's industrial environments, with operating temperatures of 0 to +70°C.

Pricing for the CP350 starts at $785, and $945 for the CP351.

PEP Modular Computers Inc., *750 Holiday Dr., Bldg. 9, Pittsburgh, PA 15220; (412) 921-3322; fax (412) 921-3356; www.pep.de.* **CIRCLE 458**

Motherboard Features Mpact 2 Media Processor

The heavy processing demands of multimedia can slow even a Pentium II CPU to a crawl. Proside attacks this problem by using the Mpact 2 media processor as a trusty sidekick to the CPU. By taking over multimedia-processing tasks, the Mpact 2-based ATX conserves precious resources on the



main CPU. For example, in a typical multimedia application, such as 3D rendering, a PC equipped with the Mpact 2-based ATX will consume 20 to 50% fewer CPU resources.

Proside has introduced a Mpact 2-based ATX multimedia motherboard, which combines accelerated 3D/2D graphics, DVD playback, DVD to TV, and digital Dolby AC-3 audio. Available in a choice of Pentium II configurations, the Mpact 2-based ATX motherboard features the new Mpact 2-based multimedia processor developed by Chromatic Research, Sunnyvale, Calif. The Mpact 2 chip is capable of performing 6 BOPS.

The Mpact 2-based ATX motherboard sells for the base price of $449.

Proside Corp., *400 Cottontail Ln., Somerset, NJ 08873; (732) 271-7395; fax (732) 271-7357; Internet: www.mpactworld.com.* **CIRCLE 459**

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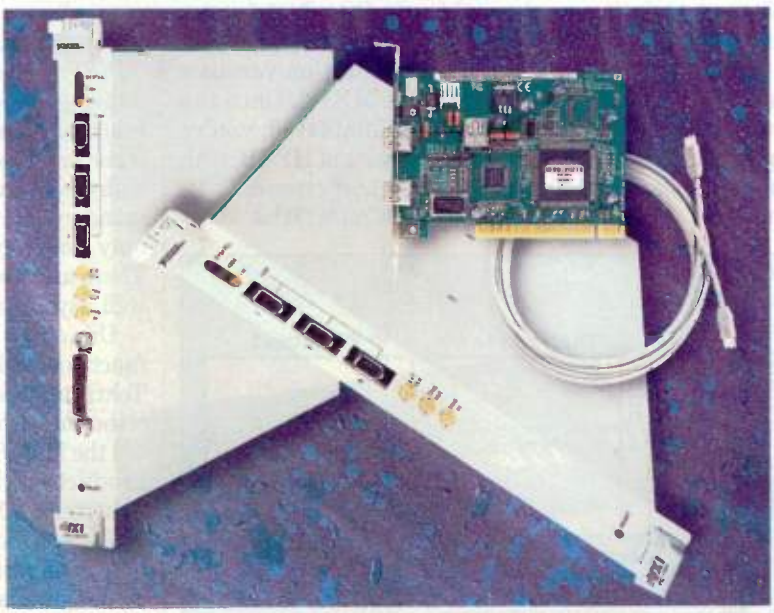
FireWire Heats Up The Action On The VXIbus

IEEE-1384 Interfaces, Multifunction Cards, And Other Updates Make This Test Industry Standard A Good Bet For The Future.

Joseph Desposito

SPECIAL REPORT

Back in 1987, a small group of manufacturers from the test and measurement industry released an open, multivendor specification for instrumentation systems called the VXIbus. Now, just over 10 years later, this bus has become a robust standard, supported by many companies and more than 1000 products. Although well established, the VXIbus still faces change. VXI products are breaking new ground, VXI hardware specifications are being reworked and improved, and a new software architecture is being touted as the next major step in the history of instrument programming.



Art Courtesy: National Instruments

One of the big developments in the product area is the use of the high-speed, IEEE 1394 serial bus, equally well-known as FireWire, to link Windows 98/NT PCs to the VXI chassis. Prior to this development, there were three choices for a slot 0 device (the card that sits in the leftmost slot of the VXI mainframe).

One is a GPIB-to-VXI controller. The drawbacks to this solution are a big, clunky cable and slow speed. The specification goes up to about 1 Mbyte/s, but most implementations are 300 to 600 kbytes/s. Contrast this with the speed of the VXIbus, which has a theoretical transfer rate of 40 Mbytes/s. GPIB-to-VXI is a good way to get systems up and running, and is still the number one interface people use to connect to VXI. Why? Because it's easy and relatively inexpensive, about $2500. But, again, the big drawback is performance.

Another choice is the embedded controller, a PC or Unix workstation built into a module, and plugged directly into the VXI backplane. Then you connect a monitor, keyboard, and in some cases a disk drive, and you end up with a working computer built into the card cage. Some older models were actually four slots wide. Embedded controllers have the bandwidth through the backplane, but are very expensive solutions. According to Lee Atchison, product customization manager for Hewlett-Packard's Measurement Systems Div., a two-slot, VXI Pentium-based PC runs about $9000 and up. "Nothing can touch it, though, for performance," says Atchison. Embedded controllers also have an advantage from a space standpoint—you don't need a PC in the rack. "Embedded controllers have a lot of advantages, but not if you are price conscious," notes Atchison.

Darren Kwock, a project manager for HP, points out that an embedded controller gives you the best backplane performance, but doesn't necessarily give you the best computing performance. Embedded controllers lag behind standalone PCs when it comes to performance. "Right now HP's high-end embedded controller is a 166-MHz Pentium. There are no Pentium II systems, although there will be

many as eight modules onto the card.

According to Mike Phipps, U.S. business development manager for performance, oscilloscopes and other products at Tektronix, some vendors have cards that hold eight modules, but each module has the same function. "The thing that is slightly different with Tektronix is that we provide six different functions on one card," notes Phipps, "And keep in mind that this card is only one slot wide." Most VXI chassis are either three, six or 13 slots.

Phipps continues, "We want to keep the customer from having to go to a second chassis. The first card in that second chassis costs a fortune. Part of the challenge for this card, and some of the other VXI products we've built, is to keep them down to one or two slots wide, and at the same time, jam as much functionality as possible into the card."

Multifunction cards may also enable you to make do with a 6-slot chassis as opposed to one with 13 slots. Obviously, this provides a less-expensive solution.

How Cool Is VXI?

Besides the technological advances occurring in VXI products, things are happening within the VXI specification. Cooling is one area where work is being done. The techniques used to measure and determine the cooling specification have changed dramatically. The specification now includes a secondary measurement that has been much more repeatable and reliable. But, only minor changes occurred in the top-level specification, which is how it is viewed by VXI users.

The manufacturer of a VXI card has to provide the user with a cooling specification. Sometimes it is printed right on the card. If not, it has to be available in the product specifications. The user must know how much cooling a VXI card needs to run reliably in its stated temperature range.

One of the advantages of VXI here is that the mainframe provides the cooling for the cards. Cooling and EMC shielding requirements are some of the extensions added for instrumentation. VXI requires that a mainframe manufacturer specify how much cooling the mainframe provides. A module manufacturer, on the other hand, has to specify how much cooling it needs. And then, it's left to the system integrator generally, to match those up, and make sure they are compatible.

With cooling, more is truly better. One of the trends within VXI mainframes right now is greater cooling capability. As Calvin Erickson, R&D project manager at HP's Measurement Systems Division, puts it, "system reliability is at the top of most all integrators' lists. So, the more cooling you provide, the better. You almost can't have too much. Even if you don't dissipate much power in a module, it's still nice to have a lot of cooling—again, because of the relationship between failure rate and the temperature of the components themselves."

The trade-off, of course, is acoustic noise. HP has been trying to develop mainframes that produce a high amount of cooling without producing too much noise. "If you're too loud nobody's going to want your product," explains Erickson. "If it's racked up, many people don't care, but certainly if it's sitting on a bench or in a development environment, acoustic noise is a huge thing."

The way HP has balanced the two requirements is by placing an intelligent closed-loop control in the mainframe, for a variable-speed fan. The fan runs as quietly as possible while still keeping the card within its specified limits. The mainframe also has a full array of temperature sensors that monitors the cards. If a card heats up, the

Understanding IVI Driver Architecture

The IVI Foundation (Interchangeable Virtual Instruments) is an open consortium whose charter is to define interchangeable instrument drivers. The model for achieving instrument interchangeability is found through instrument classes or types. First, you define a standard programming interface for instrument classes such as oscilloscopes, digital multimeters, and function generators. Then, when test developers write test code, it is independent from the instrument hardware. They can switch to other manufacturers' instruments or to other form factors such as from GPIB to VXI or PXI (PCI extensions for instrumentation). At the introduction of the IVI Foundation two weeks ago, five instrument class specifications were completed—oscilloscope, digital multimeter (DMM), arbitrary waveform generator, switch, and power supply.

Instrument classes are defined as a collection of instrument attributes and a standard application programming interface (API) for programming these attributes. For example, the oscilloscope class contains a collection of characteristics common to all oscilloscopes. These are VerticalRange, VerticalOffset, HorizontalTimePerRecord, TriggerType, and so forth. The class also contains functions the programmer can use to set these attributes or retrieve data from the instrument, such as ConfigureVertical, ConfigureHorizontal, ReadWaveform, and so forth. By defining a standard for each of these functions and attributes, it is possible to write test programs for any oscilloscope.

Of course, most instruments differ in functionality or capability. This makes it virtually impossible to create a single programming interface that works with all of them. For this reason, the IVI Foundation instrument class specifications are divided into fundamental capabilities and extensions. The fundamental capabilities, as the name implies, are the common functions and attributes of an instrument class. Extensions are functions and properties that represent more specialized features of an instrument class. The IVI Foundation specification for oscilloscopes includes extensions for different oscilloscope trigger types, such as video, runt, width, and so forth. Through extensions, new capabilities will eventually fit under a standard programming interface to allow for interchangeability. In the meantime, with the IVI generic instrument driver architecture, developers can call around the IVI driver class to use these specific, unique features that are not yet standardized.

For more information about the IVI Foundation, check out their web site at *www.ivifoundation.org*.

system speeds up the fan.

According to HP's Erickson, a real benefit of VXI in general is that the instrument environment is really protected, far more than in VME or other card cages out there. "And we do that through this kind of closed-loop control of the cooling, and through a lot of EMC factors. We really want users to feel confident that the instrument environment is protected."

HP is also trying to keep the air flow consistent from front to back and side to side in its mainframes. "It's pretty easy to get all this air to come right up to the front and pile up. You get all your airflow right there, and none in back—you get hot spots. So consistency of airflow is a big deal in addition to the sheer amount of air that comes through," says Erickson.

Another area where the VXI specification is likely to improve is bus speed. VXI was based on the VMEbus, and basically uses the same data bus as VME. However, VXI is a little bit different form factor, and it defines pins on the backplane for triggering and instrumentation functions. Some pins are also used for automatic configuration and slot identification. Currently, the standard VXIbus is 32 bits wide. But this will change soon. A new specification, VME64, expands the VMEbus to 64 bits without additional hardware. The VXIbus will follow suit.

According to James Kimery, marketing manager for Test and Measurement at National Instruments (NI), every one of NI's new controllers is already VME64-compliant. VME64 is being discussed by the VXI Consortium. The current draft of the VXI specification is 1.4, but a new revision is on the way, and they will adopt a VME64 specification. That will double the throughput on the VXI bus from 40 Mbytes/s maximum to 80 Mbyte/s.

VXI*plug&play* Revisited

On the software side of things, there is VXI*plug&play*, which appeared in 1993. Driven by several companies, the main thrust of VXI*plug&play* was to standardize software. So, when you bought an instrument from HP or Tektronix and plugged it into your VXI system using a National Instruments' controller, the software that was delivered with the three products all worked in the system with no problem. "VXI*plug&play* is one of the most successful alliances of its kind that I've ever seen," says Kimery, "VXI*plug&play* really did achieve its goals." When you buy a VXI instrument, the VXI*plug&play* driver comes with it.

As far as additional work goes, there are still groups in VXI*plug&play* looking at new technologies such as ActiveX, and how it works in a test and measurement system. In other words, how does ActiveX relate to instrument drivers? "Every time the computer industry has a new technology, such as ActiveX, the VXI*plug&play* group has to assess its impact, and determine if there is any way to take advantage of the technology to make VXI systems easier to use," explains Kimery. "And there's still a little bit of work left on instrument drivers, making them more robust, and delivering a lot more capability."

Before VXI*plug&play*, a manufacturer could build a VXI instrument, and didn't have to provide any software for it. Engineers had to write quite a lot of software to use the instrument. Now, all VXI instruments have to come with an instrument driver. VXI*plug&play* instrument drivers are written on Virtual Instrument Software Architecture (VISA), which is the lowest-level software in the system. The instrument driver is automatically installed in defined directories, to which all the instrument manufacturers have agreed and adhere. A user can just go into the Windows Explorer (or other operating-system file manager) and find the plug-and-play directory to see all the drivers that are stored in the system. VXI*plug&play* standardized the installation process, the directory structure, and the I/O software.

Another new development that should have an effect on the software side of VXI, is the formation of an open consortium know as the Interchangeable Virtual Instruments (IVI) Foundation. John Pasquarette, Test and Measurement Software marketing manager at National Instruments, calls IVI, "the next major step in the history of instrument programming." The IVI Foundation builds on VXI*plug&play* driver standards to allow instruments to be interchanged in test systems, with no software modifications required. Standard instrument programming specifications for various instrument types makes interchangeability possible.

For example, an IVI oscilloscope driver will work with all IVI-compatible oscilloscopes, regardless of manufacturer or form factor (GPIB, serial, VXI, PXI, etc.). The bottom line is that engineers can preserve their investment in test programs regardless of any changes they make to their instrumentation hardware or form factor. *(For more details on this new programming standard, see "Understanding IVI Driver Architecture," p. 90).*

Easy To Use And Reliable, Too

In addition to the new developments mentioned thus far, manufacturers who build VXI products are always trying to improve ease-of-use and reliability. Ease-of-use features that come to mind are LCDs on VXI mainframes, which provide diagnostic information, and small handles on card connectors, which make it easier to install the cards in mainframes.

Reliability is enhanced by increased cooling, which we've already covered, as well as increased power capability. For example, the power supply in the HP E8404A mainframe can supply 1000 W to the modules. According to HP's Erickson, "Typically, applications are 300 W or less. Very few times do we run into somebody that truly needs 1000 W. But there are some reasons why customers want that. One is that they don't know what they are going to do with the system tomorrow or the next day or next year. So, having that kind of capability available is important to them. It's like they're buying it for insurance." He continues, "a lot of customers like a higher-power supply for reliability reasons. If you have a 1000-W supply and are running it at 300 W, think about your derating factor compared to, say, running a 400- or 500-W supply at 300 W. There's much less stress on the system, and it's much more likely to stay up and running."

It's clear that in the more than 10 years of its existence, the VXIbus has earned the support it has garnered from the test and measurement industry. And, with all the new developments, the VXIbus should provide a viable testing platform for many more years to come.

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The 5066 uses 100% CMOS circuitry and a 3.3V CPU to reduce heat generation and improve reliability. The stock unit includes embedded DOS 6.22 and diagnostic software in flash, two serial ports, floppy and enhanced parallel port, watchdog timer, opto-isolated interrupt, ISA Bus interface and –40° to 70° C operation. The antivibration DIMM socket allows DRAM expansion to 33 MB. The card can operate in any ISA Bus backplane or be a stand-alone SBC with the application of 5V.

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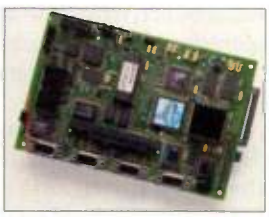

The PC-325D is a mobile PC with a GPS interface, PCMCIA, 24 lines of digital I/O, 6 serial ports with IEC1000 ESD protection, bulkhead style connectors, floppy/hard disk ports, 1.5 MB flash memory, 16 MB DRAM, NT compatible, 133 MHz CPU, resident DOS 6.22, PC/104 expansion, –40° to 85° C operation, and 5V supply. The PC-325D has a small 5.9" x 7.5" footprint, dissipates less than 5W, withstands high shock and vibration, and has a MTBF of 16.3 years.

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5664 SNAP I/O interface

The 5664 provides a seamless interface to the OPTO 22, SNAP I/O systems. It supports 32 opto-isolated analog and digital I/O modules (max. 64 analog or 128 digital channels). The analog modules support RTD, thermocouple, voltage and current inputs and outputs. The digital modules support high voltage/current inputs/outputs with 2500V of isolation. The SNAP I/O systems allows mixing and matching within the same rack. The 5664 operates from –40° to 85° C, requires only 5V, is ISA Bus compatible and withstands 40g of shock and 10g of vibration. The number of I/O modules can be expanded to 224 in a single Octagon card cage.

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Accelerated Design Verification And VXI Make A Perfect Match

Need To Account For Unexpected Operating Environments? The VXIbus Is The Way To Go For Hardware-In-The-Loop Testing Techniques.

DWIGHT ANDERSON, Hewlett-Packard Co., Measurement Systems Div., 815 14th St. SW, Loveland, CO 80537; (970) 679-3734; dwight_anderson@hp.com

To paraphrase a famous quote, electronic devices, and embedded systems in particular, sometimes boldly go where no other device has gone before. Simply put, the devices find themselves in a multitude of unexpected operating environments—some of which may not have been intended by the design engineer.

How, then, do design teams verify a new device's operation over the breadth of situations it may encounter? To answer this question, it's beneficial to understand the interdependence between the fault spectrum and the use model. One potential technique, adapted from software design, is hardware-in-the-loop, or accelerated-design-verification, testing. Thanks to recent advances in computational and measurement technology, the VXIbus (VME eXtensions for Instrumentation bus) lends itself to hardware-in-the- loop testing as a means to gain sufficient information regarding the fault spectrum in a dynamic environment.

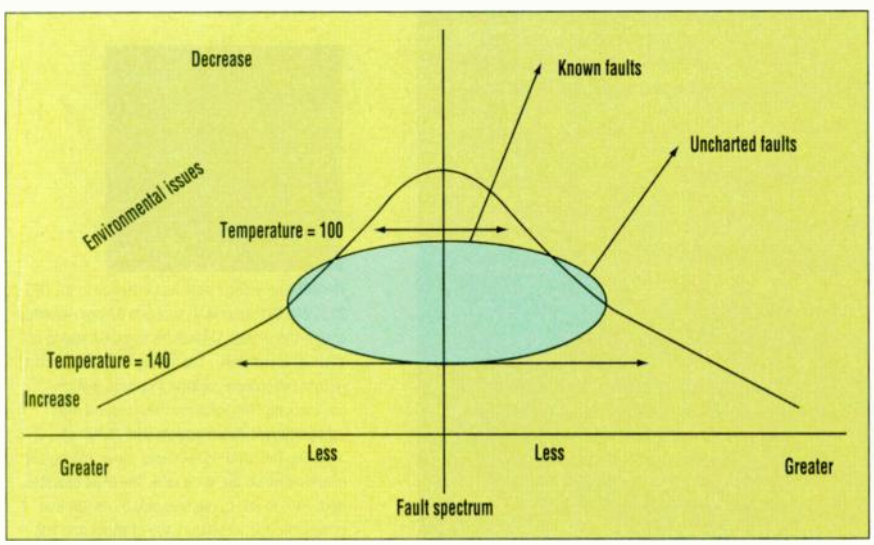
Figure 1 shows a map of the size of the fault spectrum as it relates to the complexity of an operational environment for an electronic device. In this case, as the operational environment becomes more complex, the fault spectrum increases. An example might be the use of a personal computer in the confines of a home, versus one used as an operational component onboard a jet aircraft. The noise, shock, and cooling issues of the jet may precipitate more faults than the PC used in the home. This is depicted here as a larger circle when the temperature increases. This assumes, of course, a benign home environment rather than one where a two-year-old places a peanut butter sandwich in the fan on the back of the PC.

An excellent example of accelerated testing is illustrated in the automotive industry. Every July, auto racers from around the world arrive in Colorado Springs, Colo., to face the challenges of a race whose venue is the beautiful, but rugged, terrain of the Rocky Mountains. The challenge for both car and driver is the Race to the Clouds, a grueling hill climb to the summit of 14,110-ft Pike's Peak. The course is a twisting and winding gravel road called the Pike's Peak Highway. In just over 12 mi., drivers will experience a 10,000-ft change in elevation, and must manage their cars through 156 hairpin turns.

Casual observers might wonder about the race team's concern for the design of their car's electronic control module (ECM). Each second, this module relates the oxygen sensor input to the torque, and mixture of gas and air as the altitude increases. An engine that starts to lose power as the finish line approaches reflects poorly on the module and its designers.

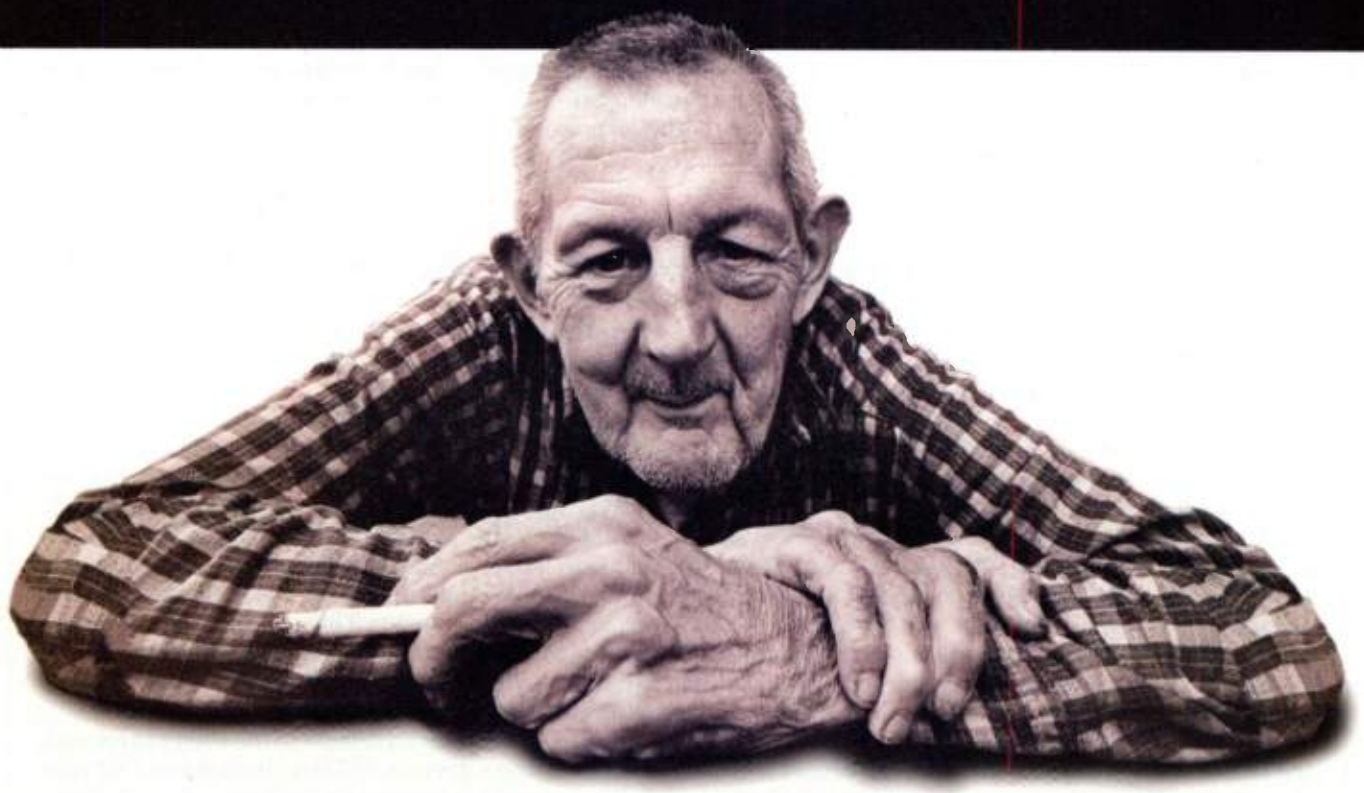
A highly complex and dynamic environment such as this precipitates incipient failures in engine control modules. After talking with a number of ECM designers, we made a proposal regarding a design-verification scheme that provided greater fault coverage. The idea was to subject the ECM to electronic emulation of the race's environmental conditions. The system would emulate the signals for the ECM with very-large changes in altitude, temperature, pressure, and throttle, along with dynamic changes in the revolutions per minute. This accelerated test process would precipitate incipient failures. The goal was to test design alternatives before moving to manufacturing.

One other example points out that this style of verification can cross industry segments. Designers of telecom amplifiers have reached quality production rates with faults in the parts-per-million



1. Here, a fault-spectrum map plots the complexity of an operational environment for an electronic device. In this case, as the operational environment becomes more complex—due to an increased temperature range—the fault spectrum increases.

So then I said "let's not use Xilinx FPGAs." Ya know, I miss being VP of Engineering.



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(PPM) range. It began when members of an engineering team were confronted by an experienced technician who had the reputation of "knowing" which amplifiers would fail first. Much to the designers' amazement, the track record for this technician was indisputable. After much cajoling, the technician let the engineers in on the secret. The technician would put the amplifiers into operation, then loosen the connectors and monitor which amplifiers provided the best output.

In this case, the technician would make a measurement of the outgoing signal on an oscilloscope with a degraded signal on the input. If the amp gave an output that was sustained within the grease marks on the scope, the technician was fairly certain the amplifier would stand up better than the other amplifiers.

This gave the designers an idea about how to improve the quality of the amplifiers. They used the more-difficult, degraded-signal test as part of their design verification when selecting alternate amplifier designs to pass on to manufacturing. By doing so, the designers were able to precipitate failure modes early in the design process, and not in the field.

In an eye diagram, for example, amplifiers within the light-green area yield better longevity (*Fig. 2*). This saves time, money, and resources. Now, instead of failure rates measured in the 1% range, designers were boasting of failures in the parts-per-million range.

The idea of accelerated testing is not just focused on temperature or the signals found in a mechatronic device. Another example is accelerating the crystal frequency of an oscillator to higher and lower frequencies. The idea is to uncover hidden faults by pushing and pulling the system into a metastable state. This may mean changing the

VXIbus Specifications Light The Way For Accelerated Testing

The VXIbus is ideal for hardware-in-the-loop or accelerated design-verification testing. VXIbus specifies three 96-pin DIN connectors called P1, P2, and P3 (*Fig. a*). The P1 connector, the only mandatory connector in the VME or VXIbus, carries the data transfer bus (up to 24 bits addressing and 16 bits data), the interrupt buses, and some power.

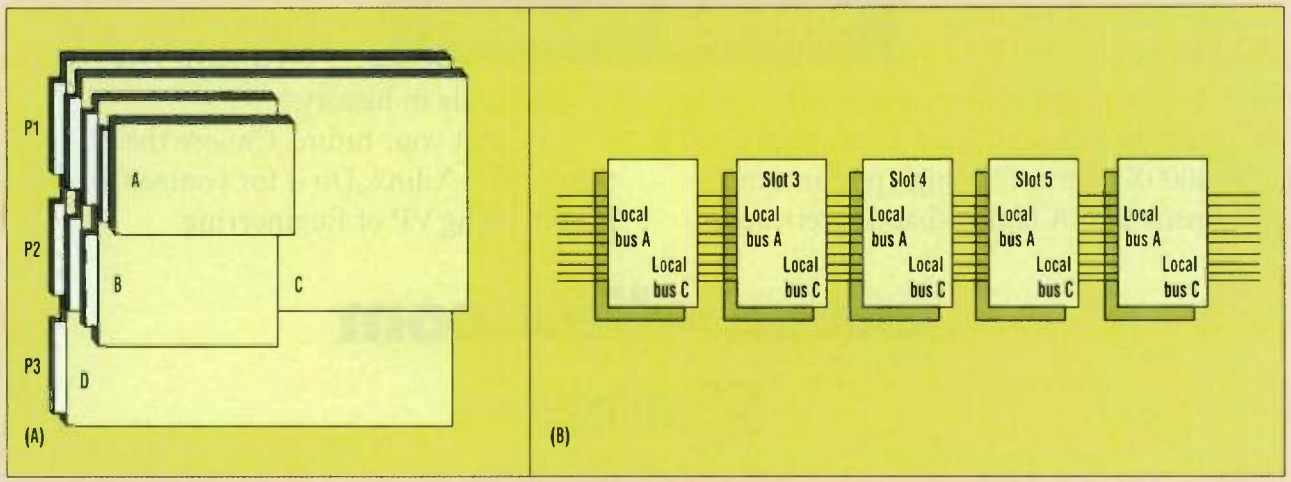
The optional P2 connector, available on all card sizes except A, expands the data transfer bus to its full 32-bit size. It also adds many other resources including four additional power-supply voltages, the local bus, and the module-identification bus. The module-identification bus allows a VXIbus module's slot number to be determined via software control.

The analog summing bus, a current summing bus, runs the length of the backplane. In addition, transistor-transistor-logic (TTL) and emitter-coupled-logic (ECL) trigger buses run the length of the backplane with four trigger protocols, and a 10-MHz differential ECL clock signal that is buffered to each slot.

An optional P3 connector, available only on D-size, expands P2 resources for specialized applications. P3 provides 24 more local bus lines, additional ECL trigger lines, and 100 MHz clock and star trigger lines for precision synchronization.

The Local Bus adds significant capability to VXIbus measurement systems. It is a very-flexible, daisy-chain bus structure (*Fig. b*). In essence, every inner slot in a VXIbus mainframe has a set of very-short, pseudo 50-Ω transmission lines running between adjacent slots on either side. The local bus is 12 lines wide in each direction through the P2 connector, and an additional 24 lines wide through the P3 connector. This bus allows for adjacent modules to perform private communication. For example, a scanner module can multiplex a number of analog nodes to the input of a digital multimeter.

Each of these areas contribute to the ability to communicate between devices, VXIbus backplane, and controllers or computers as an integral part of any VXIbus test system. This communication can occur at the top speed of 40 Mbytes/s. Contrast this against the maximum data transfer rate of 1 Mbyte/s of IEEE-488. It is the backplane speed of the VXIbus that allows the system to be used in an accelerated test scheme.



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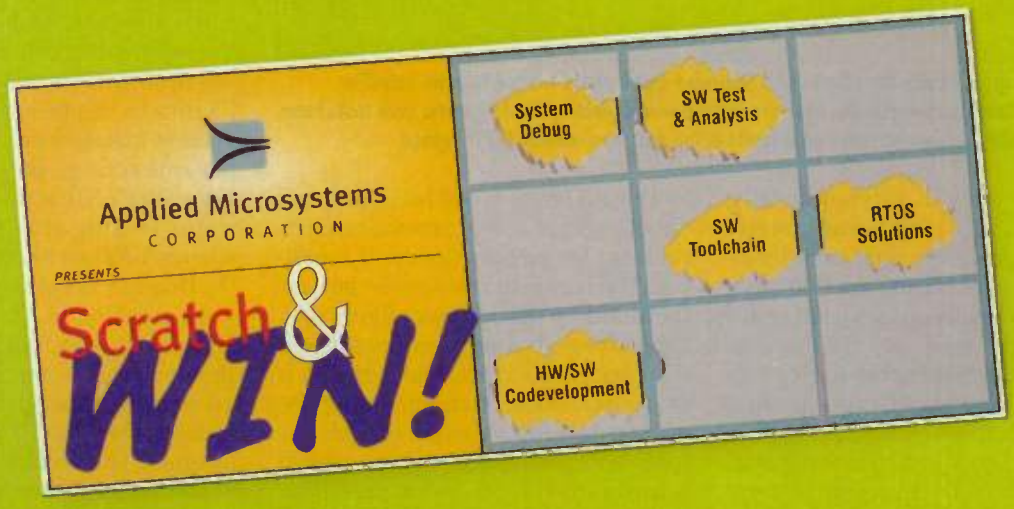

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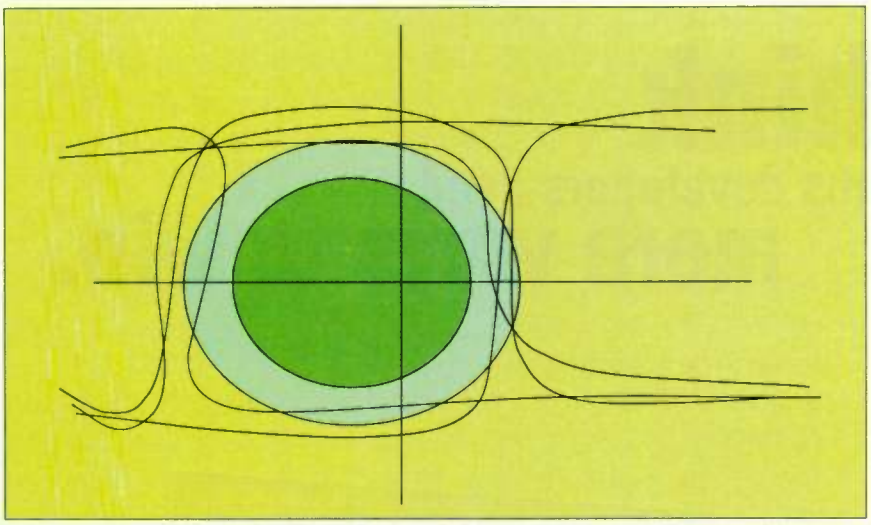


2. This eye diagram shows the effects of a degraded-input-signal test on telecom amplifier performance. Amplifiers within the light-green area would yield better longevity. Such tests have resulted in quality production rates with faults in the parts-per-million (PPM) range.

clock frequency in a dynamic way, rather than with simple static steps. That is, the designer might consider increasing and decreasing the frequency as if it were modulated by 60, 120, or 400 Hz. Designers could vary the power to the board by oscillating the supply voltages, or injecting larger surges as might be found on a "poor-quality" power line.

The idea is not just to look for catastrophic failures, but to measure irregularities, or look for changes in a waveform signature as a device operates in this mode. The technique is somewhat analogous to identifying modes of resonance in a mechanical system. In this case, however, the impetus for failure is an electrical impulse.

The goal is to develop a map of the fault spectrum as it relates to changes in the environment. To reach this goal, designers need an electronic stimulus and measurement architecture that lends itself to accelerated testing. It must be one that adapts to complex environmental models with very-fast system throughput.

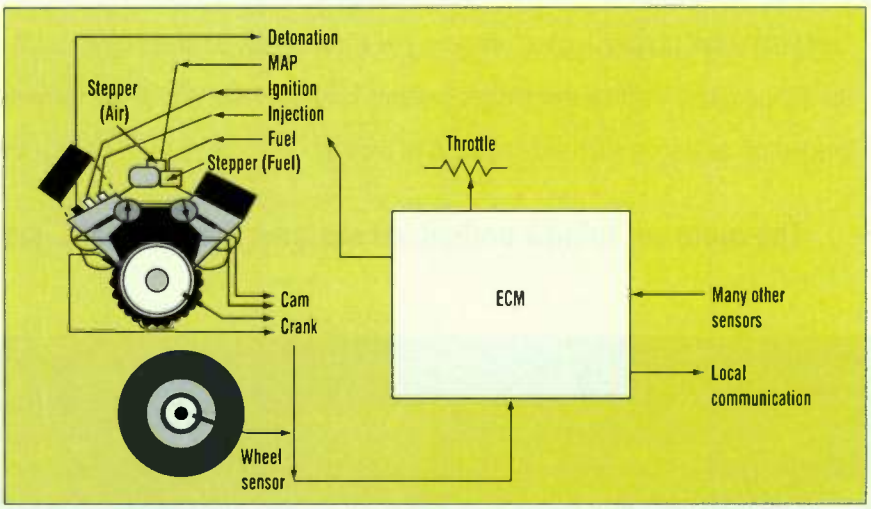
The VXIbus architects, made up of a consortium of vendors, forged a unique standard that provides fast measurement speed and high data throughput in a well-defined mechanical environment. In addition to these operating parameters (but outside the scope of this article), stringent EMC and noise requirements are specified to prevent any module from radiating enough energy into another module to affect its measurement integrity and reliability.

The VXI high-speed backplane and direct register access provide an environment for greater system throughput. The backplane also gives the user the ability to quickly reconfigure systems to provide design verification on a changing product mix. Furthermore, it provides an ideal environment for the user to develop a custom module for special-purpose measurements needed in hardware-in-the-loop design verification. For example, system designers can combine DSPs and high-speed analog-to-digital and digital-to-analog converters to act as a high-performance stimulus and measurement system for design verification.

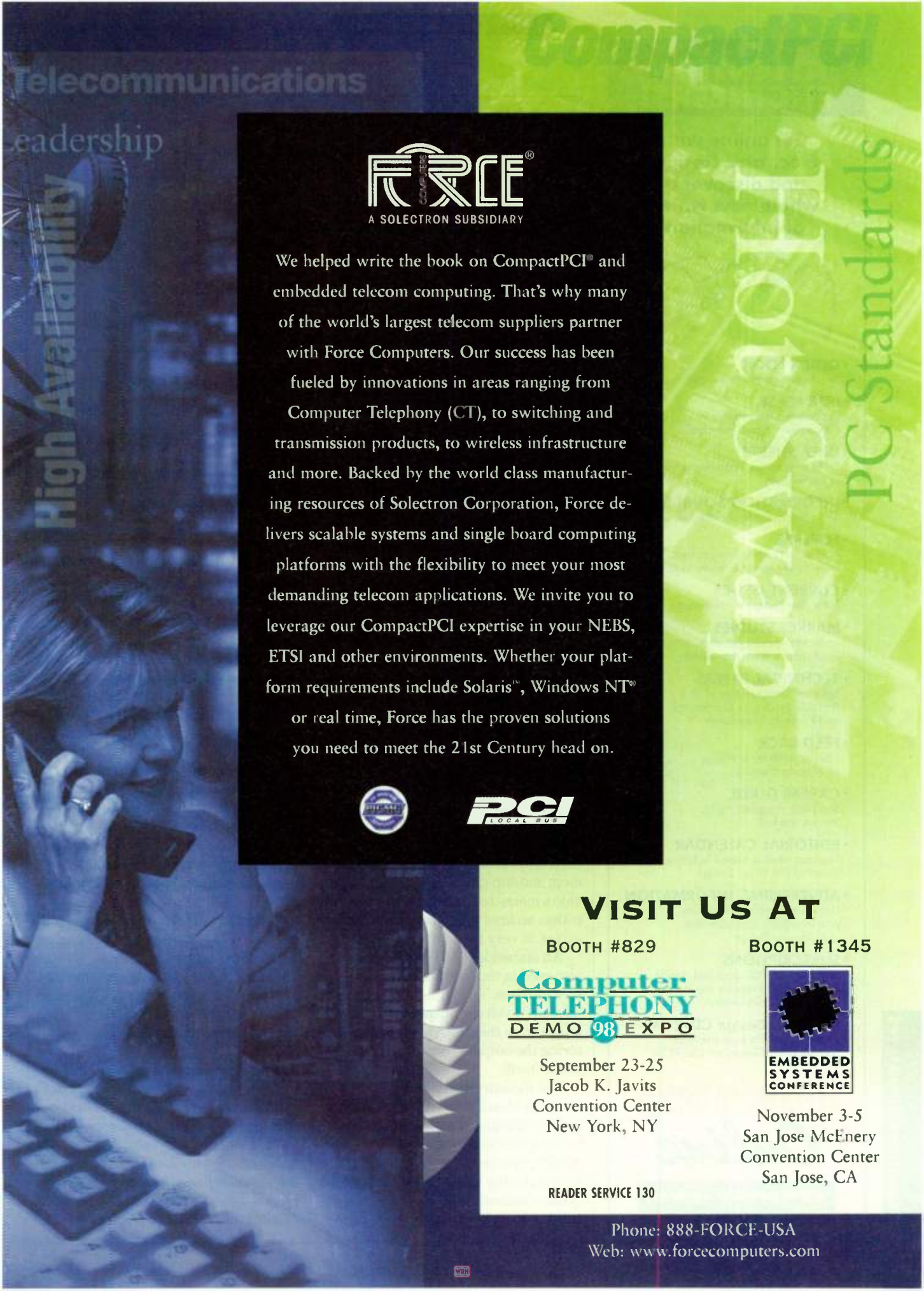
The VXI backplane is defined around the popular VMEbus architecture, known for its excellent computer backplane. Along with the necessary communication protocols, the VXI backplane has high-speed data rates of 40 Mbytes/s. This makes it ideal for building instrument systems with high throughput and performance.

The VXI consortium has provided other resources for instrumentation. These include additional power-supply voltages for analog and ECL circuits, and instrumentation buses for measurement synchronization and triggering. Also included are an analog sum bus and a set of local bus lines for private module-to-module communication. A more-standardized set of communication protocols was developed for the VXIbus to handle autoconfiguration, resource management, and device communication. Some important specifications of the VXIbus that facilitate accelerated testing are described in the sidebar *VXIbus Specifications Pave The Way For Accelerated Testing.*

As mentioned, the design of the ECM and its controlling firmware is a complex process, one that demands a fast coupling between the various VXI modules. Once the ECM is electrically designed, the architecture and optimization of the firmware that controls it must be verified. This really needs to be done in close coordination with the engine for which the ECM and its firmware are intended (*Fig. 3*). This is true in other applications as well—telecommunications, aerospace, military, and a world of other devices and systems.



3. Designing and optimizing really needs to be done in close coordination with the engine for which the ECM and its firmware are intended. Once again, the VXIbus architecture provides flexibility that allows signal switching in concert with measurement and stimulus.



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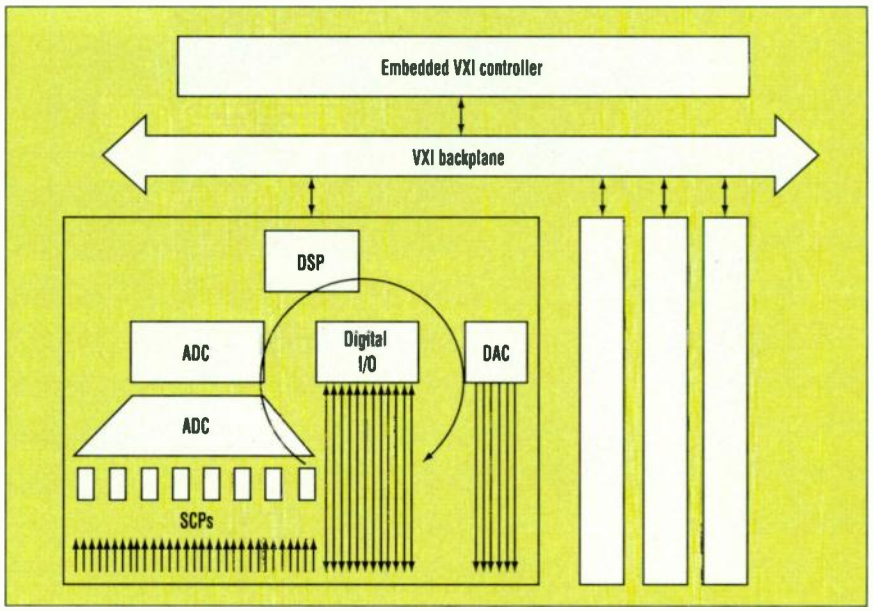

4. Hardware-in-the-loop testing requires tight coupling between the computer/controller and the measurement subsystems. This is accomplished through the VXI backplane, which directly connects to the subsystems.

The VXI specifications and backplane speed, along with the local bus, create a robust environment in which to build interdependent emulation of real-world signals that operate with various phases of a design. In the automotive application, the engine signals are emulated and brought to extreme circumstances, approaching what may not even be possible with a real engine. This is done so that the system pushes the firmware's work envelope. The goal in this case would be to uncover hidden faults that may exist just outside the boundaries of the real- world engine. In this situation, the VXI backplane throughput, along with the measurement and stimulus interoperability, provide a means to reach this area of verification, an area previously unattainable except in very rare circumstances.

An embedded VXI oscilloscope was also used in this system to capture elusive glitches. The high-speed digitizer measured voltage outputs and current inputs from the ECU, along with monitoring the outputs from the engine emulator itself.

The measurements then provided a map that identified the faults as they related to changes in various environmental or operational variables. The information gleaned from the state of the device during this process provided a greater understanding of the fault spectrum than had been previously known. The end result was a more-informed and quantitative means to select the best designs. Design verification with accelerated testing using a VXI system provides a pathway for higher quality, reduced design costs, and ultimately more satisfied customers.

In the VXI architecture, the VXI backplane directly connects to the measurement and computation subsystems *(Fig. 4)*. It is this tight coupling of the embedded controller and measurement subsystem that allows a design engineer to span the measurement spectrum. The ability of the VXI architecture to make this jump is somewhat akin to a move from simple math functions like addition, subtraction, multiplication, and division, to the more-complex math functions of integrals and derivatives. Just as moving to higher forms of math provide paths to greater understanding, so too do systems that provide accelerated testing. They yield greater insight into the fault spectrum of newly designed devices.

Dwight Anderson is a business development manager for Hewlett- Packard's Measurement Systems Division. Previously, he was an applications consultant and market researcher for VXI applications in manufacturing for the division's engineering group. Anderson received his BSEE from the Steven's Institute of Technology, Hoboken, N.J.

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	PIC16C6XX PIC16C7XX PIC16F8X PIC16C9XX	512 x 14 1K x 14 2K x 14 4K x 14 8K x 14	80–368	28, 40, 44 64, 68	13–52	25	68HC05 68HC08 80C51 ST6, ST7 COP8
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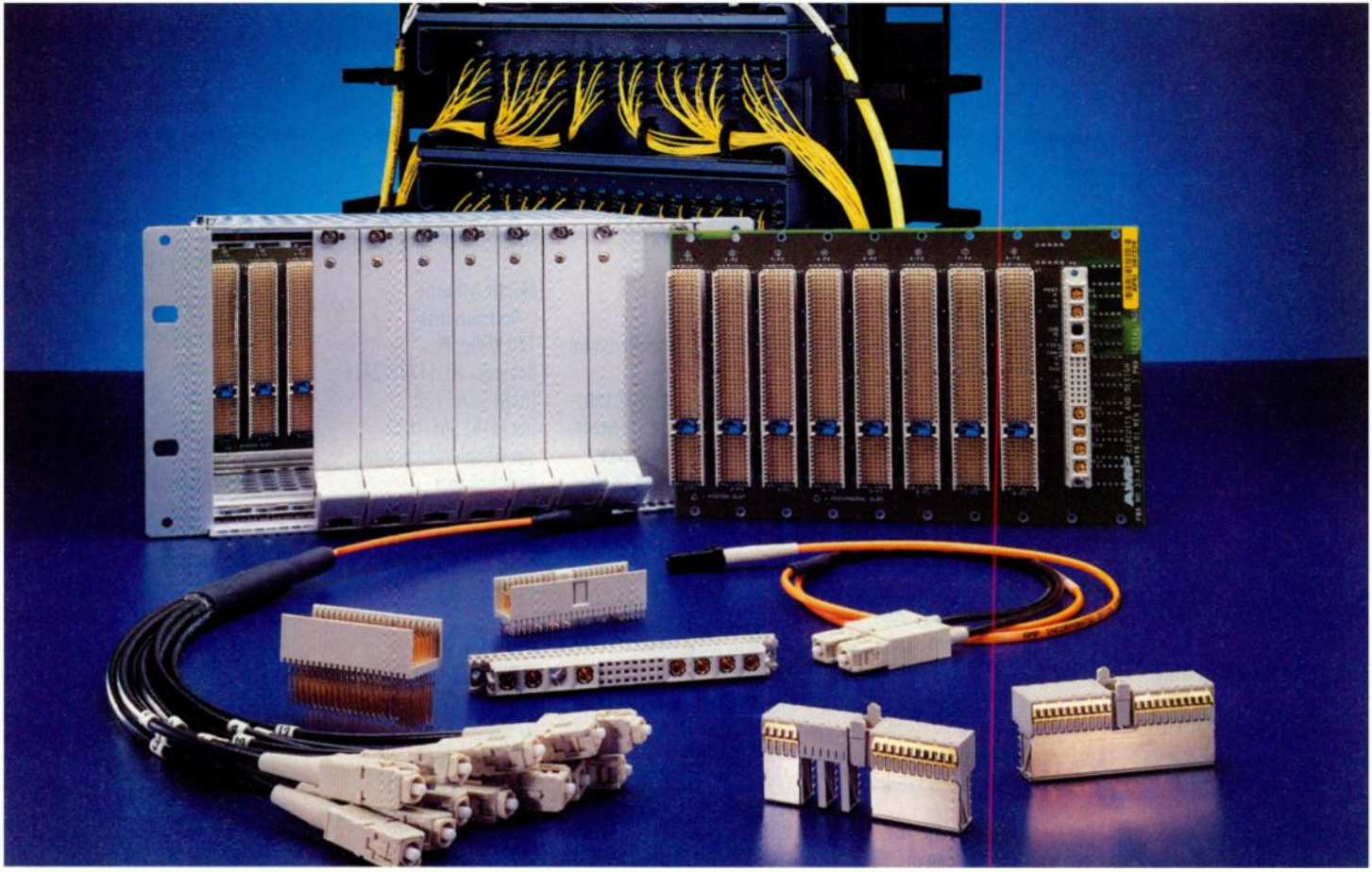

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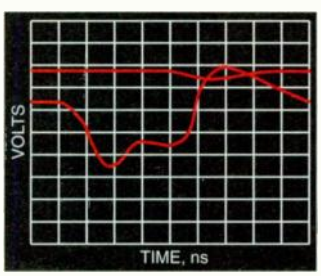

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READER SERVICE 111

(continued from page 102)

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Milpitas, CA 95035
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fax (408) 263-5896
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email: infos@microsignal.com
www.microsignal.com
ANA, DSP
CIRCLE 559

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Austin, TX 78730
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fax 49 (0) 40 60 87 305 20
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(continued on page 106)

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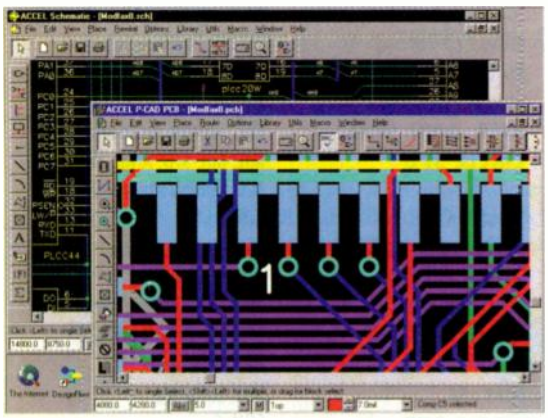

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TEST & MEASUREMENT PRODUCTS

VXI Card Supports SAE J1850 Standard Messaging

The IP201S is a single-wide industry pack (IP) that supports the SAE J1850 standard. Specifically, the card supports the standard's variable-pulse-width (VPW) messaging practices for Class B multiplexed communication network interfaces. The IP is designed for use with C&H Technologies' own VXI IP carrier cards or with cards for VME, PC-AT, PC,I and NuBus. The IP201S features 10.4-kbit/s transmit/receive rate; 41.-kbit/s receive rate; 64 kbytes of memory for a transmit/receive buffer and message filter definition; long message support; automatic framing of the transmitted message with start-of-frame and CRC bytes; and global transmit/receive enable/disable. The IP201S is fully compliant with ANSI/VITA standard 4-1995 for single-wide IP modules. Typical applications include automotive electronic module testing, automotive electronics simulation, and communications. The IP201S is priced at $825 in single quantities.

***C&H Technologies**, P.O. Box 14765, Austin, TX 78761-4765; (512) 251-1171; fax (512) 251-1963; Internet: www.chtech.com.* **CIRCLE 483**

6.5-Digit DMM Module Features FIFO And DMA

The VM2710A is a high-performance, autoranging, 6.5-digit multimeter with FIFO and direct memory access. It's designed for fast system throughput, with greater than 2000 readings/s across the VXI backplane. For applications that require multiple input monitoring, the VM2710A provides for on-board limit checking and the option of generating VXIbus triggers if the input exceeds these limits. This approach further speeds system throughput by freeing up the VXIbus controller and backplane from having to continuously monitor these limits. Two differential isolated input channels are provided on the VM2710A to allow one channel to be connected directly to a scanning multiplexer, while the other can be brought directly out for manual test and debug of the unit under test. This DMM belongs to the VMIP family of products, which gives users the added flexibility of combining it with other instruments to create a multifunction C-size card. Price of the VM2710A is $1900; delivery is four weeks ARO.

***VXI Technology, Inc.**, 17912 Mitchell, Irvine, CA 92614; (949) 955-1VXI; fax: (949) 955-3041 e-mail :sales@VXI Tech.com; www.vxitech.com.*

CIRCLE 484

VXIbus Card Tests, Simulates MIL-STD-1553 Systems

The BUS-65536 is a versatile C-size, 16-bit VXIbus card designed for the testing and simulation of MIL-STD-1553 systems. The card provides full intelligent interfacing between the serial dual-redundant MIL-STD-1553 data bus and IBM PC-compatible computers, allowing the computer to simultaneously simulate a MIL-STD-1553B bus controller (BC), multiple remote terminals (RTs), and an intelligent bus monitor (MT). Errors can be injected into the BC messages and any of the emulated RT responses. The BUS-65536 currently supports Hewlett-Packard's HP7500 software package Series C with V743 controller and HP VTL 3.0 library for HP-UX 10.01. Real-time libraries allow users to bypass the menu-driven software and control the BUS-65536 directly through C and C++. Other program features include the ability to emulate up to 31 RTs that meet both the MIL-STD-1553A and MIL-STD-1553B response times.

***ILC Data Device Corp.**, 105 Orville Dr., Bohemia, NY 11716-2482; (516) 567-5600; fax (516) 567-7358; www.ilcddc.com.* **CIRCLE 485**

Firewire VXI Controllers Link Windows PCs To VXI Chassis

The VXI-1394 and VXI-1394/G interface kits are VXI*plug&play*-compliant IEEE 1394 interfaces. The kits use the 400-Mbit/s IEEE 1394 serial bus to link Windows NT/98 PCs to VXI chassis. Both products are compatible with standard instrumentation software. The VXI-1394 kit includes a PCI-1394 board for a Windows PC, a C-size VXI-1394 slot 0 module that plugs directly into a mainframe, an IEEE 1394 serial cable, and NI-VXI/VISA software for Windows NT or '98. The VXI-1394/G has the same features as the VXI-1394. However, it adds a GPIB connection on the front panel to simplify the integration of GPIB instruments into VXI-based instrumentation systems. A computer equipped with the VXI-1394/G can transparently control GPIB instruments through the IEEE 1394 link by employing the same software used with a typical PC plug-in GPIB board. VXI-1394 pricing starts at $2395, while the VXI-1394/G starts at $2995.

***National Instruments**, 11500 N. Mopac Expressway, Austin, TX 78759-3504; (512) 794-0100 or (800) 258-7022; fax (512) 794-5759; e-mail: info@ natinst.com; www.natinst.com.*

CIRCLE 486

Modular Building Blocks Offer Switching Flexibility, Density

The SM1000 series of switch modules consists of the SM1000A single-slot base unit and the SM1000B double-slot base unit.The SM1000A can house two high-density switch modules, and the SM1000B can house up to six high-density switch modules. Switching modules can be mixed and matched for flexibility and density. The modules are part of a new switch modularity and interface platform (SMIP). The goal of the SMIP series is to reduce the size of switching solutions by at least one-third compared to other solutions. Each SM1000 base unit includes a switch control interface board. The interface is designed to provide all of the features of a message-based switching system, but with the speed of a register-based switching system. This is achieved in hardware on the control interface board, rather than within a driver. Pricing is $500 for the SM1000A and $750 for the SM1000B. Switch modules start at $1000. Delivery is eight weeks ARO.

***VXI Technology Inc.**, 17912 Mitchell, Irvine, CA 92614; (714) 955-1894; fax (714) 955-3041; e-mail: sales@ vxitech.com; www.vxitech.com.*

CIRCLE 487

VXI Multifunction Card Merges Six Instruments In One Slot

The VX4101A MultiPaq instrument combines six core functions in a single C-sized slot. All six functions operate *(continued on page 110)*

The Kepco Bipolar, 4-Quadrant Series BOP.

An amplifier?
A servo driver?
An electronic load?
A power supply?

The Kepco BOP is ALL of these!

Kepco's unique BOP are wideband amplifiers with four-quadrant source and sink capabilities. They respond like an amplifier to analog input signals into the upper audio range or can be interfaced to a test system with optional GPIB or VXI cards. A 16-bit interface is available.

The BOP can sink as much as they source so they can exercise batteries through a full charge-discharge cycle or can be used to characterize active devices. For all of their dynamic agility (especially appreciated when stabilizing current), Kepco's BOP are stable d-c sources capable of sustaining a setting indefinitely with excellent stability and low ripple.

Applications include test and simulation, beam steering, magnet driving, position control, waveform amplification, and motor drive.

Where can you use a BOP?

BOP MODEL TABLE

MODEL	d-c OUTPUT RANGE E_0 max.	I_0 max
100 WATT		
BOP 20-5M	± 20V	± 5A
BOP 50-2M	± 50V	± 2A
BOP 100-1M	± 100V	± 1A
200 WATT		
BOP 20-10M	± 20V	± 10A
BOP 36-6M	± 36V	± 6A
BOP 50-4M	± 50V	± 4A
BOP 72-3M	± 72V	± 3A
BOP 100-2M	± 100V	± 2A
BOP 200-1M	± 200V	± 1A
400 WATT		
BOP 20-20M	± 20V	± 20A
BOP 36-12M	± 36V	± 12A
BOP 50-8M	± 50V	± 8A
BOP 72-6M	± 72V	± 6A
BOP 100-4M	± 100V	± 4A

BOP-HV MODEL TABLE

MODEL	d-c OUTPUT RANGE E_0 max.	I_0 max.
BOP 500M	±500	±80mA
BOP 1000M	±1000	±40mA

This KEPCO product is backed by a firm **5-YEAR WARRANTY**

AN ISO 9001 COMPANY

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THE POWER SUPPLIER™
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For information about these amazing instruments, contact Martin Lachhmanen at 718-461-7006, ext. 5132, e-mail him at mlachhmanen@kepcopower.com or visit the BOP page at http://www.kepcopower.com/bop.htm

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THE POWER TO MAKE IT WORK

(continued from page 108)

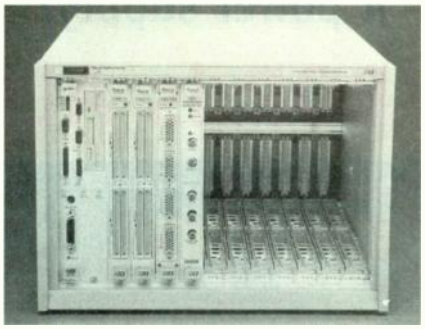
from one VXI interface and include a 5.5-digit DMM, a 250- or 500-MHz universal counter, and a SurePath Master switching control as standard features. Options include 32 bits of digital I/O, eight digital-to-analog converters offering eight independent analog output channels, and eight relay drivers. The resolution of the two-channel universal counter is 10 digits/s, with 250-ps single-shot resolution. An optional prescaler input allows frequency and period measurements to 3 GHz for microwave signals. A high-stability TCXO timebase also is available. The SurePath Master controls any of the six-member family of Tektronix's VXI switching modules. The VXI MultiPaq with standard features is priced at $5395. The digital I/O and relay drivers are $895, and the DACs $1195. Delivery is four weeks ARO.

***Tektronix Measurement Group**, P.O. Box 1520, Pittsfield, MA 01202; (800) 426-2200 (press 3, code 1068); Internet: www. tek.com/Measurement.*

CIRCLE 488

13-Slot VXIbus Chassis Features Fault-Tolerant Cooling

The 1261BL is a 13-slot VXIbus mainframe with fault-tolerant cooling. Appropriate for medium-power measurement systems, the 1261BL C-size mainframe provides up to 600 W of usable power to the VXIbus backplane. The chassis is designed for benchtop applications and features new fans with reduced acoustic noise. Current and voltage monitoring is accessible through a rear panel. An advanced, fault-tolerant cooling design provides three cooling fans for the VXIbus modules to prevent damage in the event of a fan failure. A fourth cooling fan is dedicated to the power supply. Racal's pressurized air-duct design and specially crafted slot blockers ensure a high volume of cooling air to the modules. Price of the 1261BL chassis is $3995 when purchased with any three Racal Instruments VXI modules. When purchased separately, the price of the 1261BL is $4195.



***Racal Instruments, Inc.**, 4 Goodyear St., Irvine, CA 92618; (714) 859-8999; (800) 722-2528; fax (714) 859-7139; www.racalinst.com.* **CIRCLE 489**

Multichannel VXI Receivers Are Multifunctional

The HP E650X series are three digital signal processing VXI receivers with multichannel, multifunction capability. The receivers are designed as subsystem building blocks for systems integrators' custom search, collection, and direction-finding (DF) systems. The receivers can tune from 2 to 3000 MHz

(continued on page 112)

arting Introduces USB onnector

w HARTING Universal Serial Bus Connector -- ies A and B add a new dimension of flexibility to sktop/ Notebook PC and a variety of peripheral vices. Single USB port is used for connecting ipheral devices, including those that use serial, allel, keyboard, mice or game ports. Peripheral vices are connected to the PC through the same nector allowing a reduction of required PC slots. ers will be particularly interested in these tures: Plug and Play; Hot Swapping Capabilities; mputer / telephony integration: and Port solidation. HARTING's new units permit transfer es up to 12 Mb / s and support up to127 devices. e USB has subchannel for 1.5 Mb / s signaling d allows daisy chaining of peripheral devices. Up 5m per cable segment, Isochronus and ynchronous data transfer and built-in power tribution for low power devices are important ecifications.

ADER SERVICE 158

har-pak® 2.5mm Connector System...

High Density, Board To Board, Analog Coax Solution

HARTING's micro coaxial connector system can provide more than twice the number of contacts in the same board space of typical SMA or DIN connector styles. The coax system can increase the quantity of high speed analog signal nsity and save space on your PCB. The ARTING ***har-pak®*** coax and signal connector stems are robust and have densities reaching 35 is per inch. The larger 2.5 mm contact spacing proves crosstalk and high frequency performance. e ***har-pak®*** system is made for high volume plications with SMD compatibility and reliable lderless compliant pin terminations for both signal d coax applications. The ***har-pak®*** connector stems can provide a competitive advantage to crease your system performance, reduce anufacturing cost, and increase system reliability.

EADER SERVICE 161

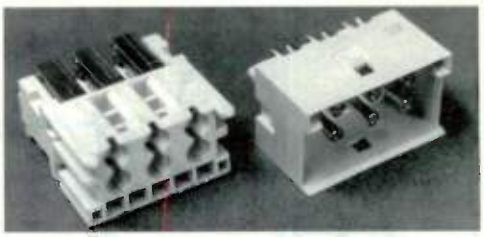
ARTING Introduces SCA-2 onnectors for Storage Devices

ie new SCA-2 connectors serve as the only eans of electrically attaching a small form factor rd disk drive. Available with 40 and 80 contact sitions for fiber channel and SCSI drives spectively. Connectors contain make-first / break- it contacts that enable users to "hot-swap" storage vices without taking the entire storage unit off-line. nd mating is accomplished through a pair of ideposts on the plug connector that have a nerous lead-in and are equipped with grounding ntacts. The plug ground contacts mate with a pair of ground contacts on the receptacle before any other electrical connection is made thus protecting the storage device from electrostatic discharge. Final alignment is performed by the "D" shape of the mating connector bodies. Highly reliable bellows style contacts

are used for signal contacts. The plastic connector housings are made of high temperature thermoplastic for surface mount compatibility.

READER SERVICE 159

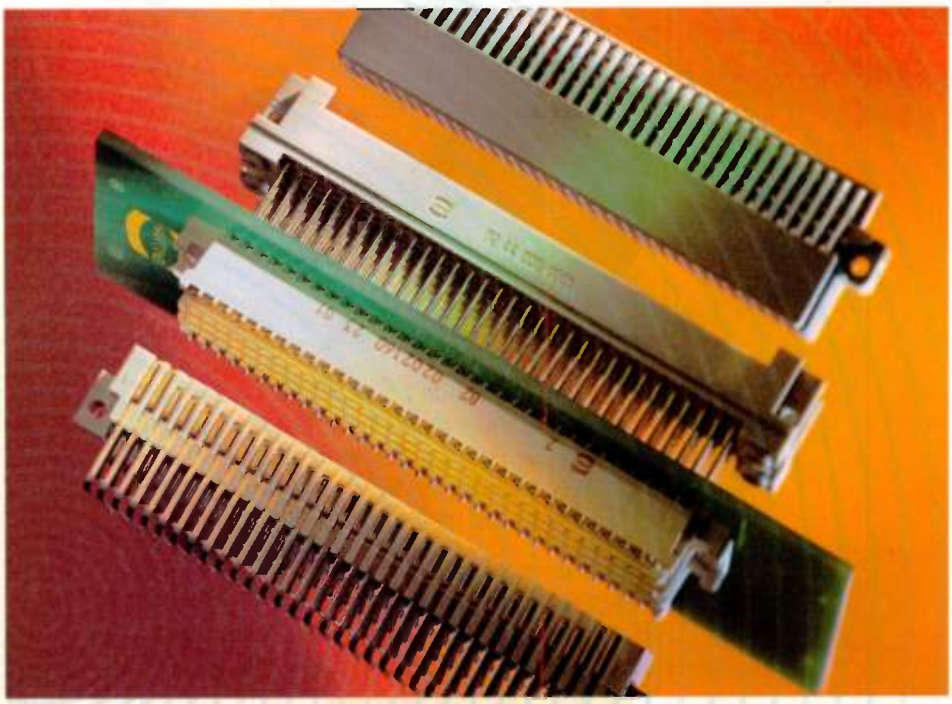
New High Density Micro-Coaxial Contacts



Designed for high speed data transfer rates. Can be used in the iec 1076-4-2 2.5mm High Density connector system, *har-pak®* Provides more space efficiency, high frequency capability, easy handling, low applied cost and application with current equipment and emerging metric equipment practices. Designed for PCB termination on both daughter card to backplane connection; allowing users to bring signal directly into the backplane without cable transition.

READER SERVICE 160

Back to the Future



har-bus 64® Backward and Forward Compatibility

To satisfy the demands for higher transmission speeds and increased shielding requirements HARTING has introduced a range of har-bus 64® connectors.

The five row har-bus 64® range incorporates 160 contacts with a pitch of 2.54 mm offering full backward compatibility with existing VME standard systems utilizing type C male connectors according to DIN 41 612.

The new connector allows users to take full advantage of the benefits of the third generation VME 64 system, including the ability to insert boards into a live backplane without disrupting data transfers on the backplane. It also incorporates pins for 'plug and play' signal lines.

Now all bus systems based on the existing 3 row connector can be upgraded to meet the demands of higher transfer rates and increased I/O

- **For use in VME based systems and as a backward compatible 5 row DIN 41 612 connector**

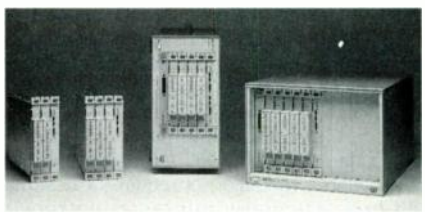
READER SERVICE 162

HARTING, Inc. *of North America*
1370 Bowes Road
Elgin, IL 60123
Tel. 847-741-1500 Fax 847-741-8257
E-Mail: more.info@HARTING.COM

HARTING® People Power Partnership

(continued from page 110)

and demodulate up to 10 signals simultaneously by taking advantage of a wide bandwidth architecture. The HP E6501A receiver is designed for wideband signal search and demodulation. It consists of a VXI tuner and a 21.4-



MHz VXI intermediate-frequency (IF) processor. The HP 6502A consists of a dual-channel IF processor and two complete receiver channels for independent tuning. The HP E6503A is a dual-channel receiver for DF applications that's designed for integrators with DF algorithms and calibration expertise. VXI*plug&play* drivers for Windows NT 4.0 are provided with each receiver. Prices start at $25,300.

Hewlett-Packard Co., Test and Measurement Org., *5301 Stevens Creek Blvd., MS54LAK, Santa Clara, CA 95052; (800) 452-4844, ext. 5900; www.tmo.hp.com.* **CIRCLE 490**

Emulators Aid 3G Wireless Characterization and Testing

The 4500 FLEX4^{PLUS} RF channel emulator and the 4600A noise and interference emulator are instruments designed to test third-generation (3G) wireless systems. The 4500 FLEX4^{PLUS} provides accurate and repeatable emulation of multipath fading, delay spread, and path loss characteristics of wireless communications channels. The 4600A allows accurate characterization of carrier-to-noise and carrier-to-interference performance of wireless systems over a wide range of repeatable test conditions. Both instruments are part of the CDMA-LAB and CDMA-ATS integrated test systems. Prices start at $34,950 for the FLEX4^{PLUS} and $44,950 for the 4600A. The instruments are available now; lead time is four to six weeks.

Telecom Analysis Systems Inc., *34 Industrial Way East, Eatontown, NJ 07724-3319; (732) 544-8700; fax (732) 544-8347; sales@taskit.com; www.taskit.com.* **CIRCLE 491**

LINEAR TECHNOLOGY

DESIGN NOTES

Step-Up/Step-Down DC/DC Conversion Without Inductors

Design Note 189

Sam Nork

Introduction

Many applications require a regulated supply from an input source that may be greater than or less than the desired output voltage. Such applications place unique constraints on the DC/DC converter and, as a general rule, add complexity and cost to the power supply. A typical example is generating 5V from a 4-cell NiCd battery. When the batteries are fully charged, the input voltage is around 6V. When the batteries are near end of life, the input voltage may be as low as 3.6V. Maintaining a regulated 5V output for the life of the batteries typically requires an inductor-based DC/DC converter (for example, a SEPIC converter) or a complex, hybrid step-up/step-down solution. The LTC®1514/LTC1515 family of switched capacitor DC/DC converters handles this task using only three external capacitors (Figure 1).

A unique architecture allows the parts to accommodate a wide input voltage range (2.0V to 10V) and adjust the operating mode as needed to maintain regulation. As a result, the parts can be used with a wide variety of battery configurations and/or adapter voltages (Figure 2). Low power consumption (I_Q = 60µA typical) and low external parts count make the LTC1514 and LTC1515 well suited for space-conscious, low power applications, such as cellular phones, PDAs and portable instruments. The parts come in adjustable and fixed output voltages and include additional features such as power-on reset capability (LTC1515 family) and an uncommitted comparator that is kept alive during shutdown (LTC1514 family).

Regulator Operation

The parts use a common internal switch network to implement both step-up and step-down DC/DC conversion. The action of the switch network is controlled by internal circuitry that senses the voltage differential between V_{IN} and V_{OUT}. When the input voltage is lower than the output voltage, the switch network operates as a step-up voltage doubler with a free-running frequency set by the internal oscillator (650kHz typ). When the input voltage is greater than the output, the switch network operates as a step-down gated switch. Regulation is achieved by comparing the divided output voltage to the internal reference voltage. When the divided output drops below the reference voltage, the switch network is enabled to boost the output back into regulation. The net result is a stable, tightly regulated output supply that can tolerate widely varying input voltages and load transients (Figures 3 and 4).

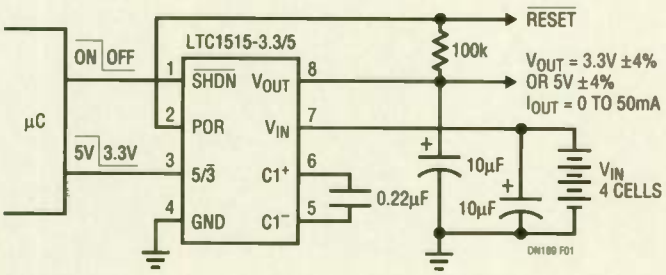


Figure 1. Programmable 5V/3V Power Supply with Power-On Reset

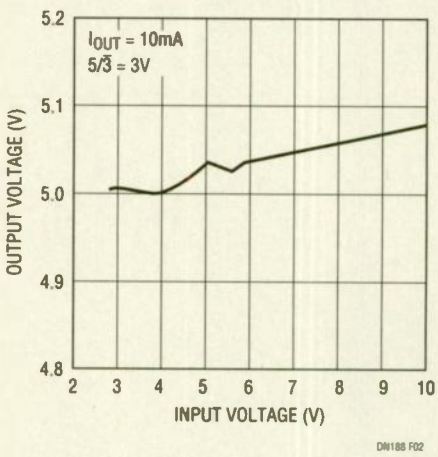


Figure 2. LTC1515-X 5V Output Voltage vs Input Voltage

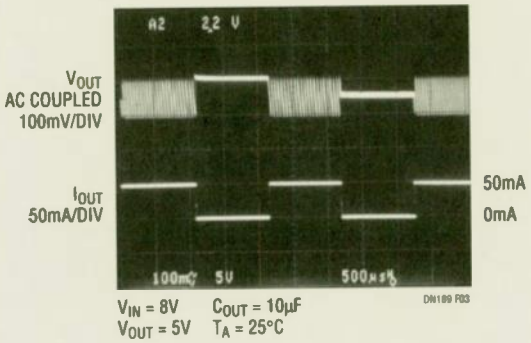


Figure 3. LTC1515-X Step-Down Mode 5V Load Transient Response

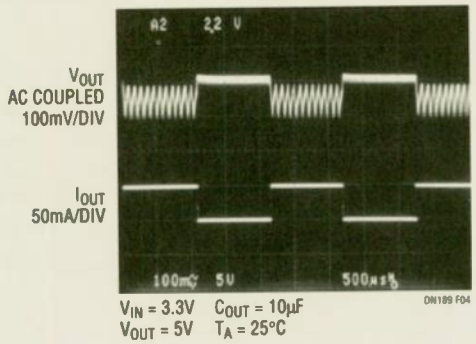


Figure 4. LTC1515-X Step-Up Mode 5V Load Transient Response

Dual Output Supply from a 2.7V to 10V Input

The circuit shown in Figure 5 uses the low-battery comparator to produce an auxiliary 3.3V regulated output from the V_{OUT} of the LTC1514-5. A feedback voltage divider formed by R2 and R3 connected to the comparator input (LBI) establishes the output voltage. The output of the comparator (LBO) enables the current source formed by Q1, Q2, R1 and R4. When the LBO pin is low, Q1 is turned on, allowing current to charge output capacitor C4. Local feedback formed by R4, Q1 and Q2 creates a constant current source from the 5V output to C4. Peak charging current is set by R4 and the V_{BE} of Q2, which also provides current limiting in the case of an output short to ground. With the values shown in Figure 5, the auxiliary regulator can deliver up to 50mA before reaching its current limit. However, the combined output current from the 5V and 3.3V supplies may not exceed 50mA. Since the regulator implements a hysteretic feedback loop in place of the traditional linear feedback loop, no compensation is needed for loop stability. Furthermore, the high gain of the comparator provides excellent load regulation and transient response.

Conclusion

With low operating current, minimal external parts count and robust protection features, the LTC1514 and LTC1515 offer a simple and cost-effective solution to low power step-up/step-down DC/DC conversion. The shutdown, POR and low-battery-detect features provide additional functionality. The ease of use and versatility of these parts make them ideal for low power DC/DC conversion applications.

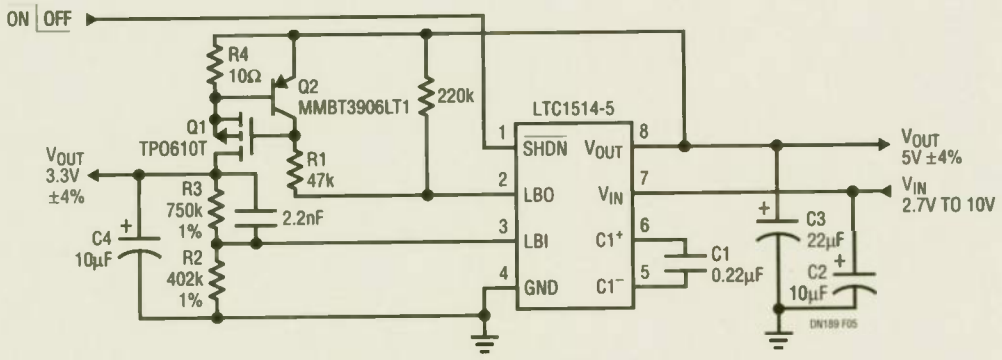


Figure 5. Low Power Dual Output Supply (Maximum Combined I_{OUT} = 50mA)

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Circle 520

Power Amplifier Buffer Features Digital Bias Adjustment

W. STEPHEN WOODWARD
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Chapel Hill, NC 27599-3290; e-mail: woodward@net.chem.unc.edu.

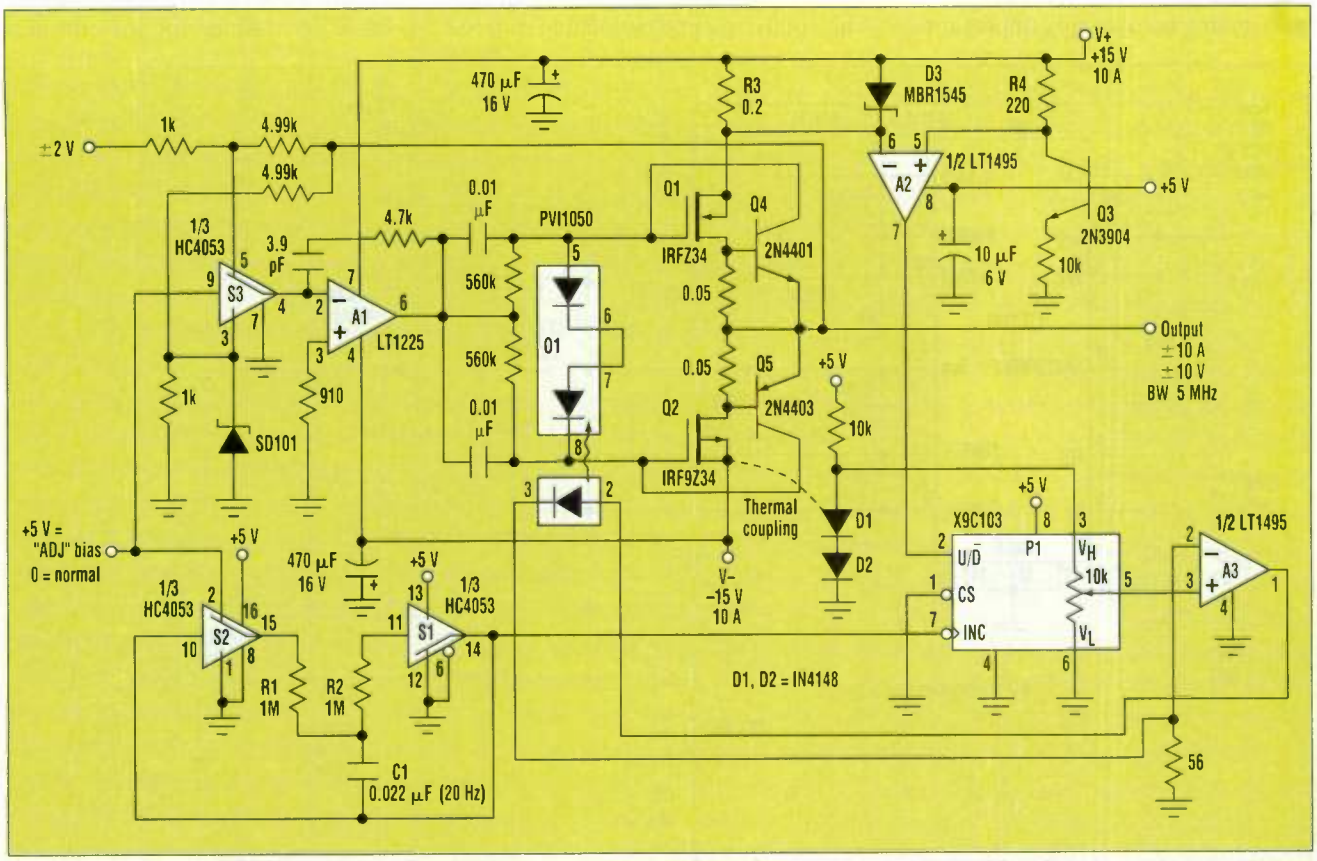
The day may be near when every amplifier application can be served simply by finding the right off-the-shelf standalone chip. Maybe. But for now, many jobs require that even the best monolithic devices be supplemented with a sprinkling of active discrete devices. One such category of application is the high-output-current, high-frequency buffer amplifier.

Of course it's simplicity in itself to add an arbitrary amount of muscle to a "milquetoast" op amp by following it with a class AB complementary bipolar emitter-follower or FET source follower pair like Q1 and Q2 in the figure. Many successful driver designs are based on just this elementary topology. But all such designs must confront the problem of stable dc biasing of the follower while avoiding unconscionable amounts of quiescent power draw and unbearable levels of harmonic distortion. This is a problem fraught with the classic twin-design-bogeymen of thermal runaway and crossover distortion.

The new solution to this old puzzle described here comprises an automatic bias adjustment loop consisting of a Xicor digital potentiometer P1, International Rectifier photovoltaic optoisolator O1, CMOS switches S1-S3, and Linear Technology op amps A2-3. The resulting adjustment loop includes two modes of operation selected by the CMOS/TTL-compatible ADJ input.

When ADJ = 0, S3 closes a normal feedback loop around A1 and the Q1/Q2 pair thus forcing the circuit to become a fairly normal, gain of –5 amplifier with a bandpass of dc to 10 MHz, full power bandwidth (limited by A1 slew) of 5 MHz, and output limits of ±10 V and ±10 A. Harmonic distortion over the full operating range is minimized by the impressive GBW of capacitive-load-compatible A1 combined with stable quiescent biasing of the Q1/Q2 pair to a thrifty no-signal value of 50 mA. The trick behind these performance numbers is the way an appropriate bias level for the follower is achieved, one that's independent of temperature and component tolerance variations.

To understand how this is done, consider how the circuit rearranges itself when ADJ =1 causes S3 to disconnect A1's input from the signal source and substitute a ground reference. Simultaneously, the S1/S2, 20-Hz multivibrator is enabled and begins clocking P1. In response, P1 begins to vary the input to A3, which then servos the control cur-



This high-output-current, high-frequency buffer amplifier uses an automatic bias adjustment loop, utilizing a Xicor digital potentiometer P1, to minimize harmonic distortion while drawing a thrifty no-signal supply current of only 50 mA.

rent into Q1 and thus the net gate bias voltage at the follower MOSFETs.

This action combines with A2 to establish a feedback loop, which tends to drive the follower pair to the desired zero-signal bias. This action occurs because, if the follower bias current I_Q is less than 50 mA, then the drop across R3 will be less than the drop across R4. As a result, A2 drives the Up/Down input of P1 high (Up). Therefore, on the next negative transition of the clock, the V_W terminal of P1 will make one step toward the V_H terminal. This increases the drive to C1, which ups the follower bias.

If I_Q is more than 50 mA, then A2's output state will reverse, causing P1 to step V_W toward V_L and decrease the follower quiescent bias. Consequently, after a maximum of 5 seconds and 99 multivibrator cycles, the follower bias will have been forced to converge to the bias level set by the R4/R3 ratio. ADJ then may be reset to zero for normal amplifier operation; the final bias setting will be retained by P1 until either power is removed or a new ADJ cycle initiated. Thermal coupling between D1/Q1 and D2/Q2 improves overall bias stability between adjustment cycles.

Although illustrated with ±15-V supplies, the unique "Over-The-Top" input topology of A2 is compatible with V+ voltages as high as 36 V (but be careful to observe A1 limitations). Also, there is no requirement that the V+ and V– voltages be symmetrical. Many variations are possible when selecting A1 and the follower MOSFETs to achieve different combinations of output capabilities.

Circle 521

Maximum-Power-Point-Tracking Solar Battery Charger

W. STEPHEN WOODWARD
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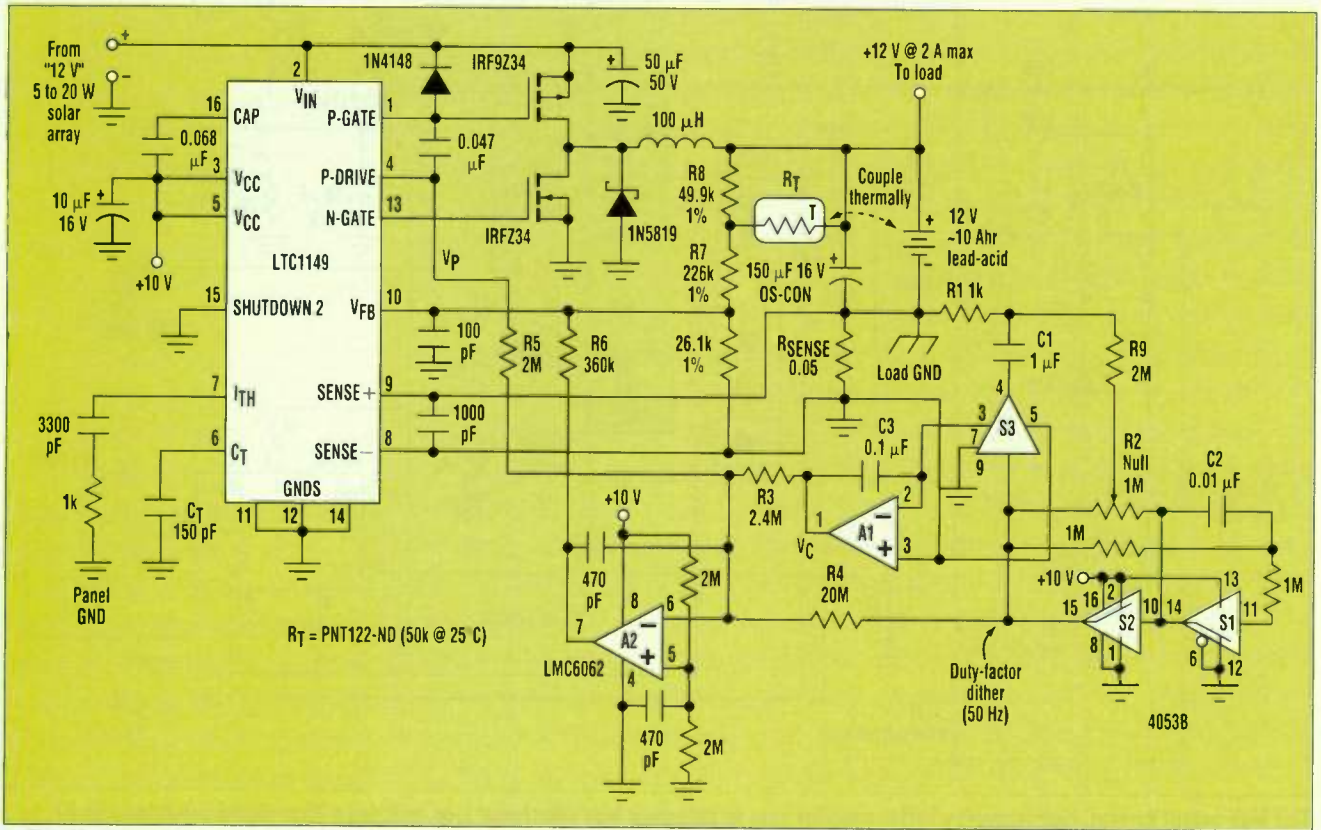
Chapel Hill, NC 27599-3290; e-mail: woodward@net.chem.unc.edu.

Sustainable electrical sources like solar photovoltaic arrays are becoming increasingly important as environmentally friendly alternatives to fossil fuels. But, while they're nice for the environment, sustainable sources aren't always easy to apply. These sources are characterized by both stringent peak-power limitations and "use it or lose it" availability. Successful application of sustainable energy sources therefore depends on strict attention to efficiency in both power conversion and energy storage.

For small systems, workable energy-management schemes usually include a rechargeable battery and battery charger. A shortcoming of this solution is that ordinary battery chargers, even efficient ones, do an imperfect job of squeezing the last milli-



1. This Maximum-Power-Point-Tracking charger, used in small solar power systems, overcomes the shortcomings of ordinary battery chargers.

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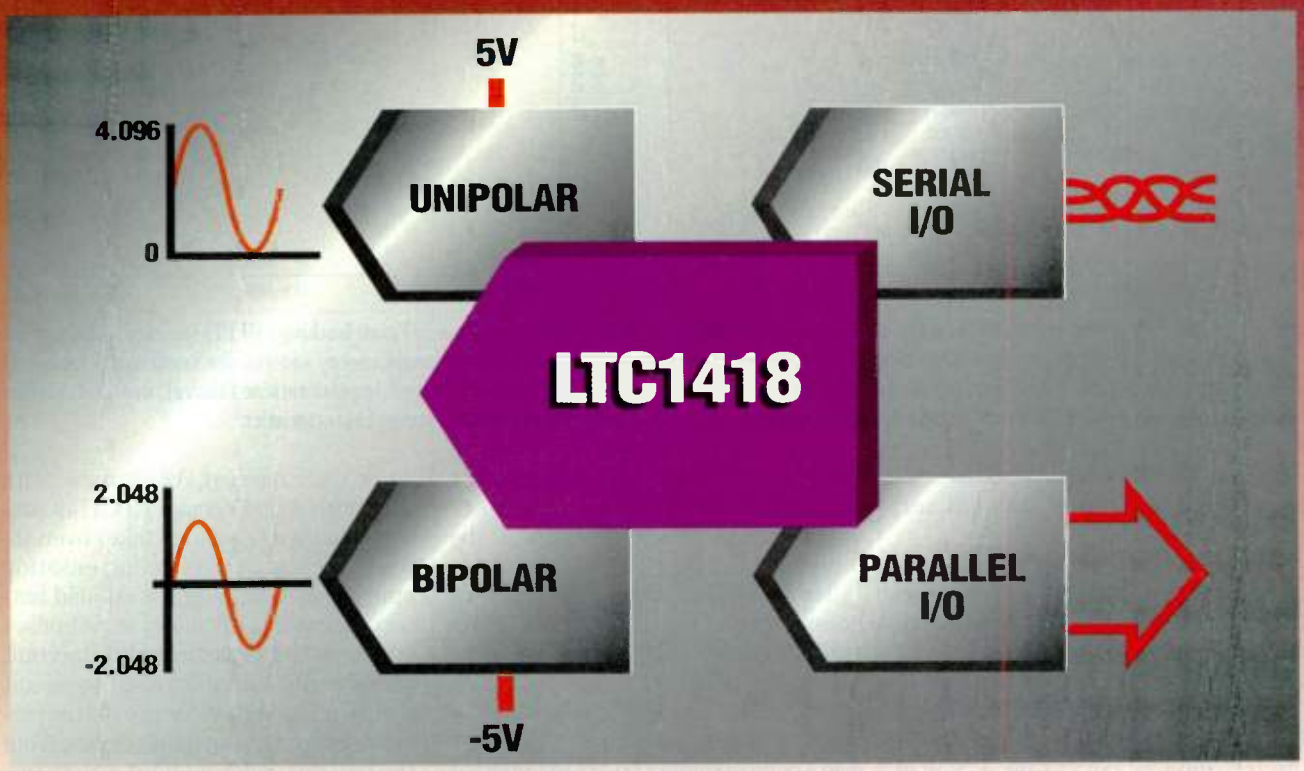

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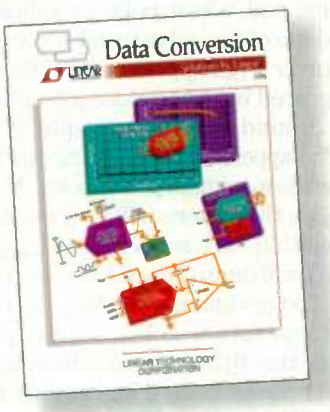

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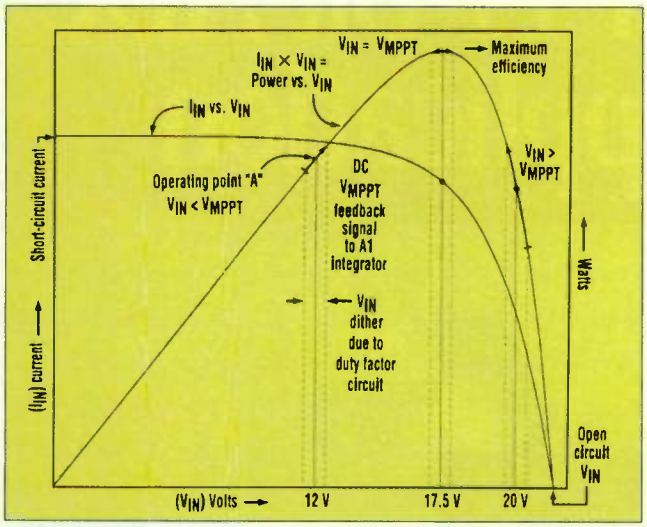
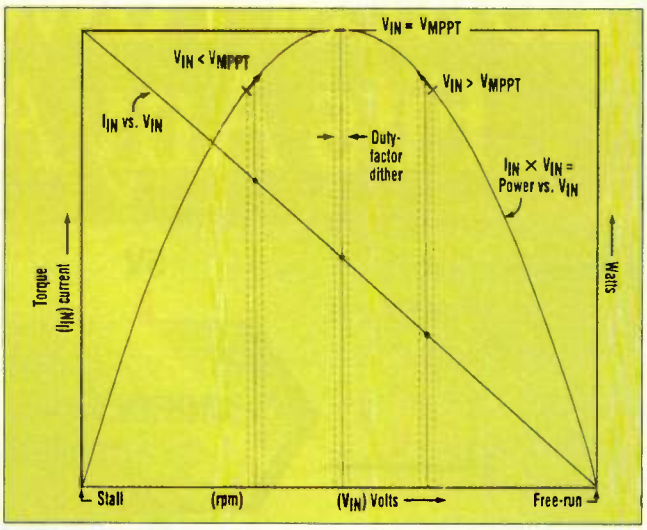


2. The I/V and P/V curves are given for a typical photovoltaic array when exposed to "standard" sunlight intensity of 1 kW/m². Standard design approaches dictate an increased number of cells to provide usable charging currents for "normal" ranges of solar insolation.



3. The Maximum-Power-Point-Tracking (MPPT) technique also can be applied to other sustainable energy sources like small water turbines, such as the "Pelton-wheel" impulse turbine (above), due to its similar power output versus loading characteristics.

watt from sustainable sources over realistic combinations of ambient and battery conditions.

The circuit shown addresses this problem in small solar power systems *(Fig. 1)*. It works by continuously optimizing the interface between the solar array and battery. The principle in play, sometimes called Maximum Power Point Tracking, is illustrated in the I/V and P/V curves for a typical photovoltaic array *(Fig. 2)* exposed to "standard" sunlight intensity (insolation) of 1 kW/m².

To accommodate a useful range of insolation and battery voltage variation, designers of solar panels make the number of cells large enough so that a useful level of charging current is provided even when the light level is low and the battery voltage is high. Consequently, when lighting conditions happen to be more favorable, these panels can produce up to 50% more voltage and 30% more power than the battery wants. Simple direct connection of panel to battery will therefore cause inefficient operation at point "A," with the excess power lost as heat in the solar panel.

Figure 1 does better than that by combining a high-efficiency (≈95%) SMPS circuit (LTC1149) with an analog power-conversion optimization loop. To understand how it works, assume battery B1 is in a state of discharge. In this condition, E1 will accept all of the current the SMPS can supply (subject to the ≈2.5-A current limit set by R_{SENSE}) at a voltage around 12 V. If U1 drives Q1 to a 100% duty factor, inefficient operation at the direct-connect point "A" will result.

However, the optimization circuit doesn't let that happen. Instead, 50-Hz multivibrator S1/S2 causes A2 to continuously dither Q1's duty factor by about ±10%. The result is a dither of approximately ±1 V in V_{IN}. There's also a corresponding 50-Hz modulation of the average power extracted from the solar panel as reflected in the return current through R_{SENSE}.

The 50-Hz ac waveform across R_{SENSE} is filtered by R1C1 and synchronously demodulated by S3. This dc error signal, whose polarity indicates the slope of the solar panel I/V curve wherever V_{IN} happens to be sitting, is integrated by A1 to close a feedback loop around A2. For example, if the SMPS happens to be operating at a V_{IN} below the maximum power point ($V_{IN} < V_{MPPT}$), then there will be a positive correlation between V_{IN} and I_{SENSE}, and A1 will ramp toward lower average duty factors and higher V_{IN}. By contrast, operation at $V_{IN} > V_{MPPT}$ reverses the dither phase relationship and A1 ramps toward higher duty factors and lower V_{IN}. Either way we get convergence toward V_{MPPT} and maximum charging current for B1.

This mode of operation continues as B1 charges and its voltage rises to the ≈14.1-V terminal-voltage setpoint determined by the R6-R7-R8-R_T network. Once reached, A2 saturates with zero output and normal LTC1149 constant-voltage regulation takes over. R_T provides temperature compensation appropriate for typical lead-acid battery chemistry. R2 allows for A1 offset nulling, which is particularly important at low panel output levels. The circuit makes no provision for preventing reverse current from being drawn from the battery under no-light conditions, but since the drain—even in total darkness—is less than 3 mA (comparable to typical battery self-discharge rates), adding a blocking diode would actually reduce overall efficiency.

The MPPT technique has much wider application than just photovoltaics alone. That's because conceptually similar functionality of power output versus loading can be seen in the I/V curves of other sustainable energy sources. Such sources are small water turbines (e.g. the "Pelton-wheel" impulse turbine of Figure 3) and fixed-pitch-rotor wind-power turbines, when either is combined with constant field alternators.

The voltage, current, and power produced by any of these sources is highly variable in response to ambient conditions (insolation, hydrostatic head, or windspeed) and dramatically dependent on the electrical impedance of the imposed load (V vs. I). Under any combination of ambient conditions, each of these sources is characterized by exactly one ideal load impedance,

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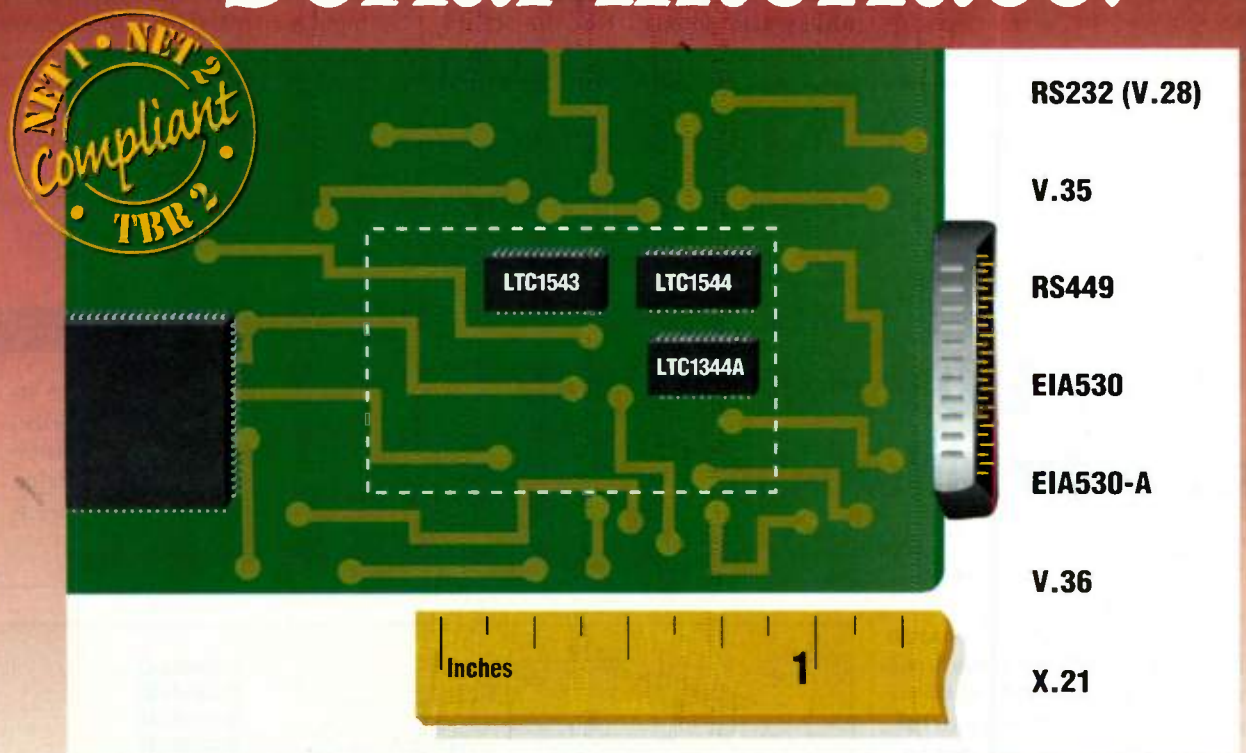

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which will result in operation at V_{MPPT} and maximum power transfer. Also of benefit is the simplifying absence of confusing local maxima in the power versus voltage curves.

Of course, the actual physics behind the I/V curves for the various sources are very different. In the case of photovoltaics, the primary energy-producing process is recombination of photoelectric charge carriers and how the rate of such recombination varies with output voltage, temperature, and insolation. For wind-power generators, the dominant parameter is the interaction of "Tip Speed Ratio" (defined as turbine peripheral velocity divided by wind speed) with the aerodynamic design of the turbine. For small hydroelectric generators, it's the fluid dynamics of the turbine or "runner" as they relate to the pressure and volume of the available water source. But the MPPT charger really doesn't care about these details. It just blindly climbs the I/V curve to the V_{MPPT} summit.

Figure 1's circuit can therefore be easily adapted to any of these systems. The only modification necessary is a bigger C2 (0.1 µF to 1 µF) to slow the dither rate to 5-Hz to 0.5-Hz frequencies compatible with the inertial time constant of mechanical power sources. In addition, wind-power applications will benefit from an overspeed preventer. This V_{IN}-limiting circuit is basically just a big Zener diode connected across the input terminals that dumps excess power in conditions of high wind speeds and low battery demand. Consequently, it prevents overrevving of the turbine and alternator. For higher power applications (25 W and up) or other output voltage ranges, consult Linear Technology LTC1149 application literature.

Circle 522

Predict ESD Response Using First-Order Differential Equations

JOHN DUNN
Ambertec Inc., 181 Marion Ave., Merrick, NY 11566

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Read the Ideas for Design in this issue, select your favorite, and circle the appropriate number on the Reader Service Card. The winner receives a $300 Best-of-Issue award.

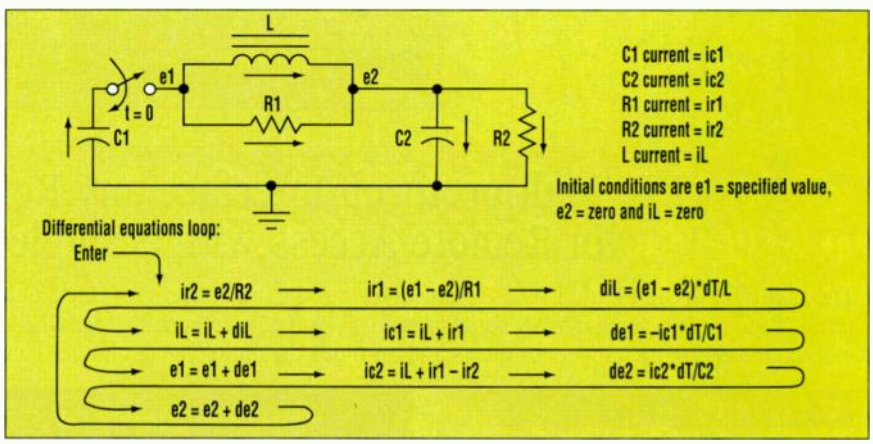
Tests for electrostatic-discharge (ESD) susceptibility sometimes call for charging a test capacitor to a specified voltage (example: 100 pF charged to 15,000 V) and then connecting that capacitor to discharge into the circuit being tested.

Voltage transients in the circuit under test can be estimated with LaPlace transforms or with several different software packages. However, it may be possible to use first-order differential equations and just a few simple lines of code, as demonstrated in the following example.

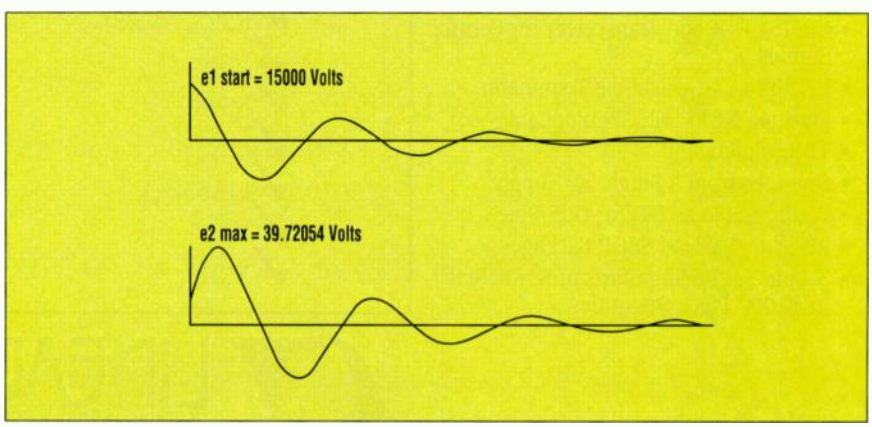
A circuit under test is taken as resistor R2, for which some kind of input filtering has been provided *(Fig. 1)*. That filtering can be taken as an RLC low-pass filter. As a result, we can write our descriptive set of first-order differential equations for the filter.

When defining the initial conditions, the inductor's current is zero and the voltage across capacitor C2 is zero. As a result, we enter the loop of differential equations and trace each voltage and current over very small time intervals (dT).

In this example, when we plot the values of voltages e1 and e2, we find that e2 will peak at almost 40 V in response to an initial 15,000 V on C1 *(Fig. 2)*.



1. The circuit under test is taken as resistor R2 with an RLC low-pass input filter.



2. In this example, the simulation predicts that voltage internal to the circuit under test (e2) will peak at almost 40 V in response to an initial 15,000 V discharge from capacitor C1.

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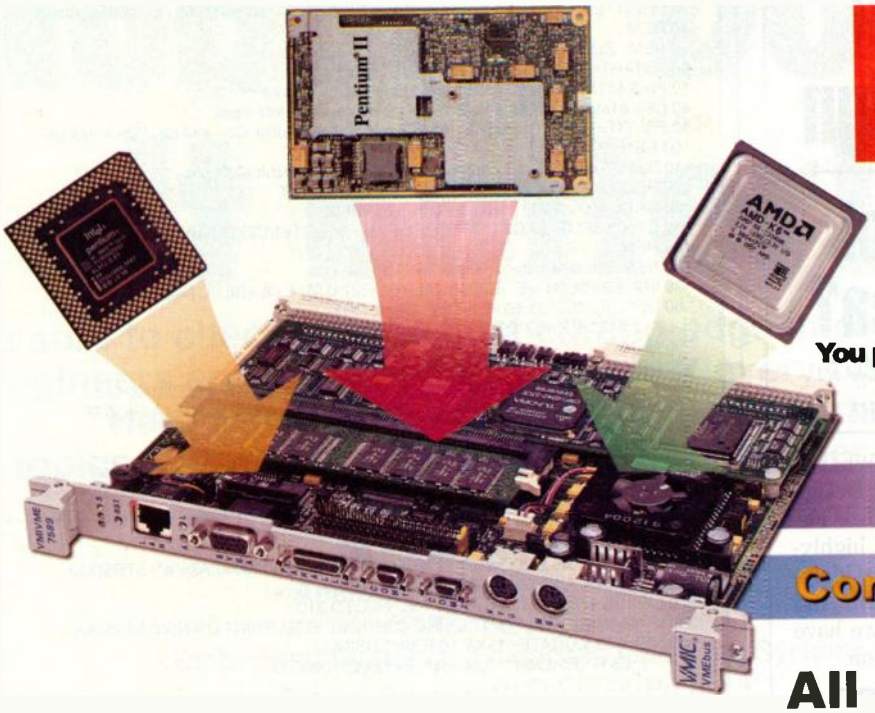

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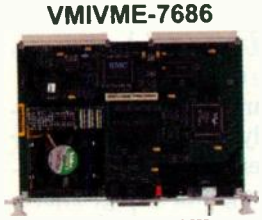
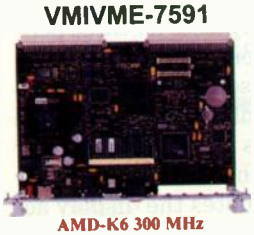


Pentium Pro 200 MHz

VMEbus shown
VMIVME-7591



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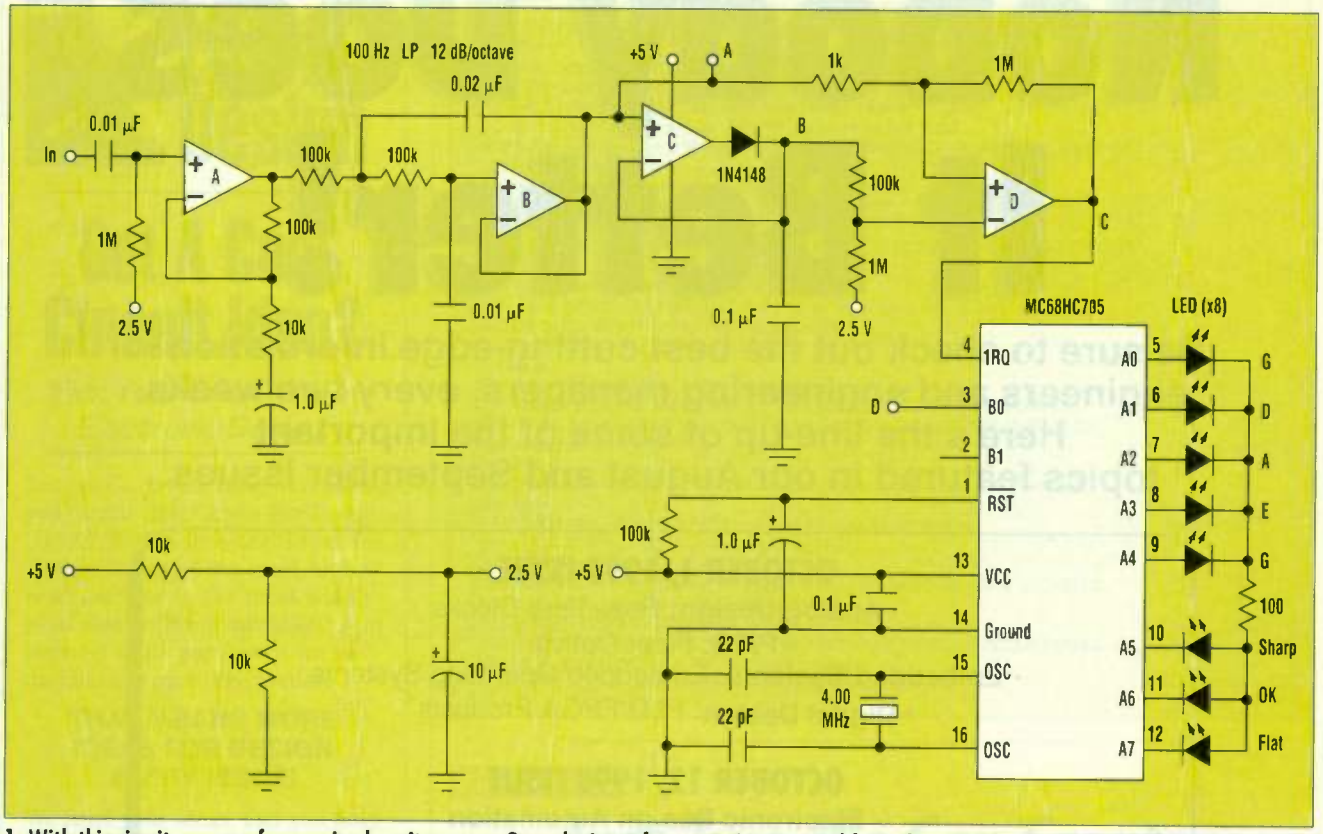


1. With this circuit, you can form a simple guitar tuner. Once the input frequency is measured from the guitar input signal (In), the LED display will indicate both the note being played (A0-A4) and whether it's Sharp, OK, or Flat (A5-A7).

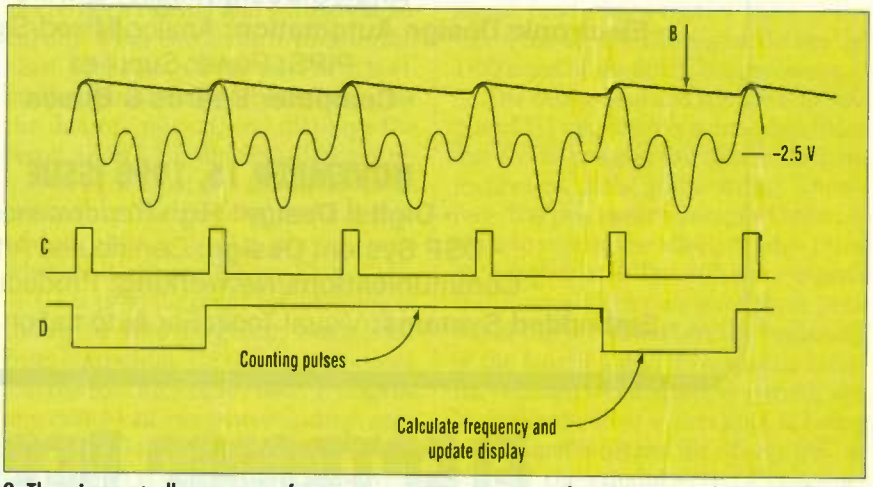
cordingly. At the next input pulse, the process starts again. If the counter ever overflows (from no input provided), the LEDs are turned off, indicating no valid input.

The basic timing accuracy is determined by the crystal used in the HC705 oscillator circuit. Using the 4.00-MHz crystal shown, the microprocessor can resolve to the nearest 2 µs of period, much more accuracy than required for guitar tuning. The LED display uses very little power. When in use, one of processor outputs A0 through A4 is driven high, and one of A5 through A7 is pulled low. This allows about 3 mA to illuminate both selected LEDs. High-output LEDs will give a clear indication at 3 mA. The B0 port of the chip produces the waveform shown in Figure 2, as an aid in making the circuit work with very complex waveforms.

Note: This circuit was developed to tune a five-string bass guitar. The lowest note is a low B with a frequency of 30.8677 Hz and a period of 32.3963 ms. The highest note is a G with a frequency of 97.9989 Hz and a period of 102.0420 ms. The range for OK was set arbitrarily at ±0.5% of exact pitch. Also, the decision threshold for determining whether the note was a G or a D was placed midway between the notes.

This method can be used to determine other low-frequency periods by adapting the number of periods counted and setting the acceptance threshold accordingly. For simple digital signals, the front-end analog processor can be eliminated. More complex front-end signal processing may be needed for instruments other than a bass guitar. This particular software has a maximum period measurement of 130 ms, corresponding to approximately 23 Hz.

(To see the complete software listing for this guitar tuner, go to Electronic Design's web site at "www.elecdesign.com" and click on "Ideas For Design" icon on the home page.)



2. The microcontroller averages frequency measurements over three input periods and produces the D waveform at its B0 port, as a diagnostic aid for use with very complex input waveforms.

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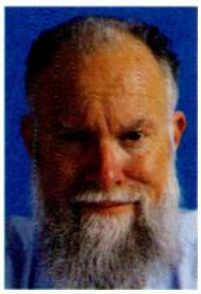
BOB PEASE

Bob's Mailbox



Hiya Bob:

In case 450,000 people haven't suggested this already, here goes: Our new car (which, alas, is new) keeps the radio playing until you open a door. I like that! *(But what if I want to listen with the door open? I don't like that. /rap)* A timer isn't a bad idea, but what if you need 10 more seconds to hear whatever it was you wanted to hear? *(I just turn on the ignition for another 2 seconds, and the timer runs again. I don't have to wait for it to shut off. I just turn the key momentarily. /rap)*

I assume you have a door-activated dome light, as you mention using a door switch for some items. You could build that for your car, too.

BURCH SEYMOUR
via e-mail

Yeah, but I don't WANT a setup like yours. When I get out of my car, I want the radio to keep playing until I get in the house. With your setup, I would have to climb out the window. No, thanks!—RAP

Hi Bob:

Several years ago, I came across a neat little circuit that would flash my motorcycle's main headlamp alternately between low and high four times a second. I thought this little attention getter might give me a tad more visibility. It certainly did. A police officer informed me that only emergency vehicles could have this sort of display. Until your laser hologram becomes available, I'll just treat everyone as though I'm invisible and give 'em (and me) lots of room.

DARAL R. MAKAHUSZ
via e-mail

I've seen motorcycles with their headlights blinking away wildly like this. At least in the daytime it ought to be OK. I can't imagine anybody complaining. Check your state traffic laws—the cop might be wrong.—RAP

Dear Mr. Pease

I always enjoy your column, and was amused about the round manhole covers. Here in England, most of them are square or rectangular, and we don't seem to drop them into the manholes!

On another topic: Breadboarding. I use strip board with strips and holes at 0.1-in. spacing. I've found it easier to use it upside down, i.e. soldering the devices into the strip side. At HF, I "super glue" copper foil onto the other side to form a ground plane. It may not be very good above 50 MHz, but it's OK up to there using phenolic-based strip board. I haven't anything so crude as figures to back that up, but things seem to work.

Sorry to hear about your VW Beetle. I've never had one, but they are a cult car here, too. (I'm not a professional, but a Ham Radio man.)

DICK BIDDULPH
via e-mail

Yeah, there are lots of breadboarding styles. So long as the ground plane is nearby, they work well. My newest (1970) Beetle sure runs strong. And—HA!—it has 10% more trunk space than the New Beetles.—RAP

Dear Bob:

I get so many trade publications I can't possibly ever read them all. Well, anyway, just a note to tell you that no matter how many Tech. Pubs. I get, I ALWAYS seek out your articles for a breath of fresh air. When work is unusually hectic, I can always read one of your columns and bring immediate sense to my day....

MICHAEL WRIGHT
via e-mail

Thanks, Mike. Yes, I even go back and read my own stuff, to find out what I wrote! Sometimes it makes a good break from THINKING!—RAP

All for now. / Comments invited!
RAP / Robert A. Pease / Engineer
rap@web team.nsc.com—or:

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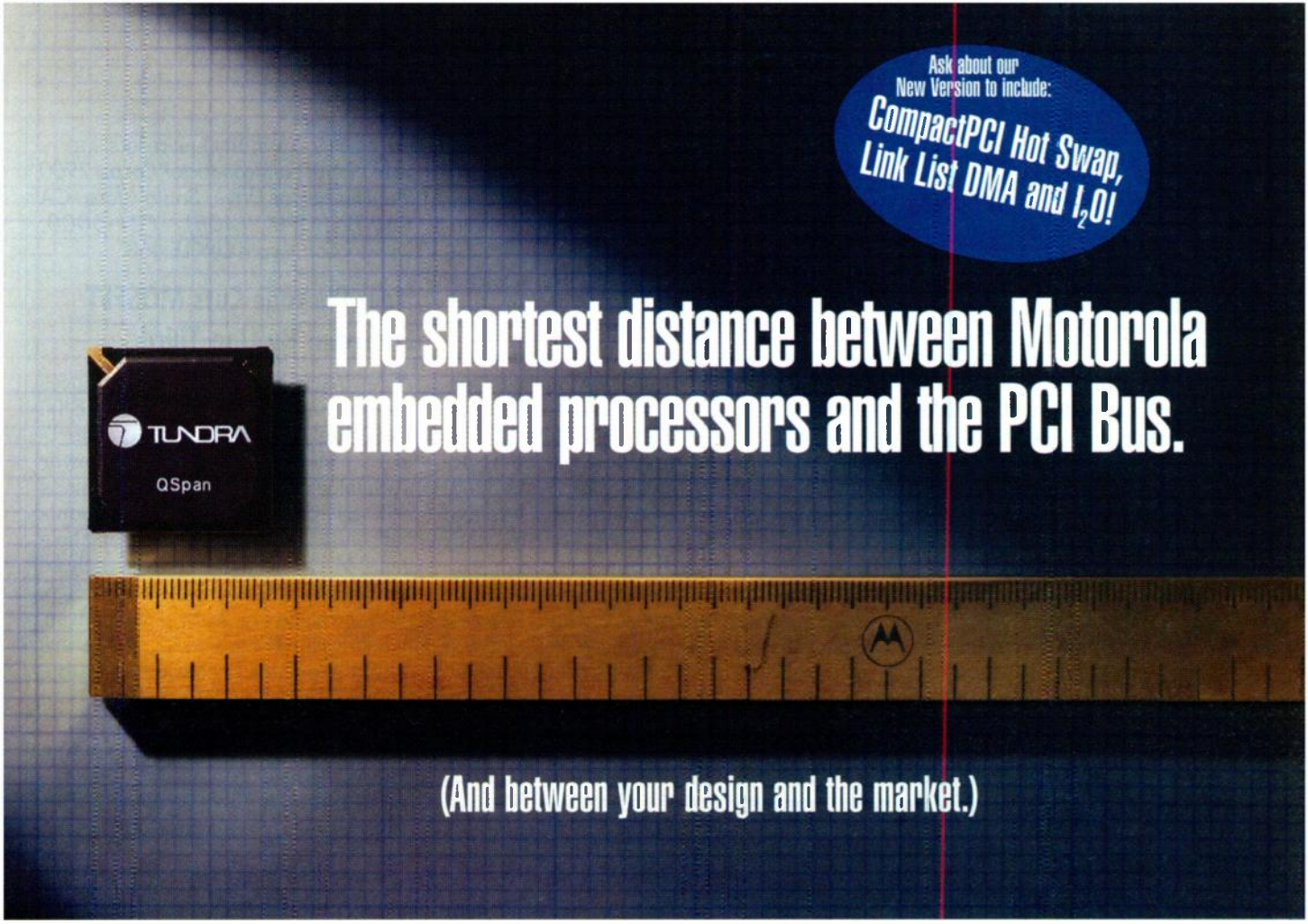
National Semiconductor
P.O. Box 58090
Santa Clara, CA 95052-8090



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READER SERVICE 152

Buck Controller Packs Two Switchers In A Single IC

Cherry Semiconductor now offers a dual-output nonsynchronous buck controller that incorporates two switching regulators in one IC. The CS-5127 is designed to power V_{CORE} and V_{IO} on computer motherboards, and it simplifies board layout and reduces heat within a computer case. Using the dual switcher cuts component cost by about 25% by eliminating the need for a second separate switching regulator. Each of the CS-5127's two regulators drives one external n-channel power MOSFET with a totem-pole output driver that can supply a dc current of 100 mA (500 mA peak) to a variety of MOSFET types. The two regulators are independent, but share a common programmable oscillator that sets the operating frequency. The CS-5127 comes in a plastic 16-lead wide-body SOIC package rated for an operating junction temperature range of 0-150°C. Pricing for the buck controller in 1000-unit quantities is set at $1.90 each. AB

Cherry Semiconductor Corp., *2000 S. County Trail, East Greenwich, RI 02818-1530; (401) 885-3600; Internet: www.cherry-semi.com; e-mail: info@cherry-semi.com.* **CIRCLE 465**

PWM Servoamplifier Delivers Sinusoidal Commutation

Copley Controls' Model 7426DC servoamplifier provides sinusoidal drive for brushless servomotors to 2.5 horsepower. The amplifier develops ±20-A peak or ±10-A continuous output while operating on a 45- to 373-V supply. The amplifier's control and feedback circuits are optoisolated from the motor's high-voltage circuits to ensure electrical safety. Model 7426DC is designed for operation with linear brushless servomotors equipped with analog Hall sensors for sinusoidal commutations. The amplifier processes the servomotor's analog U and V Hall signals to create U, V, and W motor phase currents. Pricing for the Model 7426DC servoamplifier is set at $508 in 100- to 249-unit quantities. Delivery is from stock to four weeks ARO. AB

Copley Controls Corp., *410 University Ave., Westwood, MA 02090; (781) 329-8200 or (800) 659-2675; www.copleycontrols.com.* **CIRCLE 466**

Pressure Sensors Work Over A Wide Temperature Range

The newest TO-8 Series pressure sensors from EG&G use the company's UltraStable technology to enhance performance over a broader temperature range without raising the price over that of previous models. UltraStable micromachining technology improves performance by minimizing the drift typical of piezoresistive pressure sensors. The TO-8 Series includes four basic pc-board-mountable package types. Models 16/17/46/47 measure absolute and gauge pressures, and are top entry packages with the pressure port operating away from the pc board. Models 26/27 are bottom entry and measure gauge pressures. Finally, models 36/37 measure differential pressure in a dual-port design that utilizes a combination of both the top and bottom entry packages.

All models come in 6- and 8-pin packages, and are available in standard ranges from 0-15 and 0-250 psi. The calibrated temperature range is –20° to +85°C. Unit pricing is below $20 in 10,000-piece quantities. AB

EG&G IC Sensors Inc., *1701 McCarthy Blvd., Milpitas, CA 95035; (408) 432-1800 or (800) 767-1888.* **CIRCLE 467**

Li-Ion Battery Charge Controller Is Accurate And Inexpensive

The LM3620 is a low-cost controller for controlling charge and end-of-charge voltages for single-cell and dual-cell lithium-ion rechargeable battery packs. Rated at 1.2% regulation accuracy, the LM3620 precisely controls charge voltage from current-limited dc-dc switching or linear chargers. It can operate from 4- to 30-V dc input sources. With no charger supply connected, the controller draws a quiescent current of only 10 nA to minimize discharging of a connected battery pack. In addition, the LM3620 offers pin-selectable charge termination voltage for either coke (4.2 V) or graphite (4.1 V) anode lithium-ion cells. On chip, the controller includes an operational transconductance amplifier, a bandgap voltage reference, an npn driver transistor, and precision voltage-setting resistors. As a result, with this device only four inexpensive external components are needed to complete the charge control design. Available in 5-lead SOT-23 package, the LM3620 is priced at $0.75, in 1000-piece lots. AB

National Semiconductor Corp., *2900 Semiconductor Drive, Santa Clara, CA 95052-8090 (408) 721-5000; www.national.com* **CIRCLE 468**

New Package Cuts MOSFET Footprint By One-Third

A new package called T-MAX reduces the cost and size of power MOSFETs. Designed for clip-mounting, the T-MAX package from Advanced Power Technology has the same dimensions as a TO-247 package without the mounting hole. Eliminating the mounting hole lets T-MAX accept die as large as those mounted in the larger TO-264 package, with the same low $R_{DS(ON)}$ and power-handling capability. T-MAX devices are available with a breakdown voltage from 100 to 1000 V, $R_{DS(ON)}$ from 11 to 500 mΩ, and current rating from 21 to 75 A. All devices are single-pulse Avalanche Energy Rated at 2500 mJ, and repetitive-pulse Avalanche Energy Rated at 50 mJ with Avalanche Current equal to the continuous current rating of the device. Small-volume pricing ranges from $14 to $25, depending on voltage rating. AB

Advanced Power Technology, *405 S.W. Columbia St., Bend OR 97702; (541) 382-8028 or (800) 522-0809; www.advancedpower.com.*
CIRCLE 469

CMOS Voltage Comparators Feature Push-Pull Driver

The ALD2302 and ALD2302A CMOS precision voltage comparators offer a typical input impedance of 10^{12} Ω, typical input bias current of 10 pA, response time of 120 ns, and a power dissipation of 175 µA per comparator. They operate on a single power-supply voltage of 4 to 12 V, or a dual supply range of ±2 to ±6 V. The devices operate at high speed for both large and small signals, and feature push-pull outputs that allow for current sourcing and sinking. Both comparators come in 8-pin CERDIP, SOIC, or standard plastic DIPs. Pricing starts at $1.42 and $1.13 in 100-unit and 1000-unit quantities, respectively. AB

Advanced Linear Devices Inc., *415 Tasman Dr., Sunnyvale, CA 94089-1706; (408) 747-1155; fax (408) 747-1286.* **CIRCLE 470**

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READER SERVICE 140

FPGA Software Boasts Enhanced Timing Capabilities

The latest version of the Designer Series FPGA design software, version R2-1998, has been enhanced to ensure a greater level of timing-analysis accuracy, precision, and ease of use. This will allow designers to work at the high-frequency capabilities of Actel's new SX FPGA family—including the 32,000-gate A54SX32 and 16,000-gate A54SX16—with an internal clock rate in excess of 320 MHz.

The tool enhances timing in various ways. For example, it reports pin-to-pin timing delays between modules instead of lumping routing delays and module delays together. And, its flip-flop report allows designers to determine the number of sequential and combinatorial macros used in a design for accurate prediction of device utilization. Other refinements made to the Designer Series software include the addition of clock resource checking and a speed/utilization performance improvement to the ACTmap feature. In addition, there's a new user interface, new macro types, behavioral VHDL and Verilog model generation capability, and improved reporting to the ACTgen feature.

The Designer Series R2-1998 is now available and sells for $995. The tool comes as a free upgrade to all existing customers with a valid maintenance contract. A Designer Lite version of R2-1998 also is available and can be downloaded free of charge from the company's web site. CA

***Actel Corp.**, 955 East Arques Ave., Sunnyvale, CA 94086-4533; (408) 739-1010; www.actel.com.* **CIRCLE 471**

Interconnect Service Calibrates RC Extraction Tools

One of the crucial hurdles facing designers today is the need to physically tune design tools to match silicon data. This is done to ensure accurate RC extraction information. A recently introduced interconnect characterization service now makes this possible by calibrating RC layout extraction tools. It achieves this by using a set of test structures with less than 0.001-pF (sub-femtofarad) resolution capability. The test structures have features that heighten specific physical dependencies—such as spacing between parallel metal wires—which allow the physical parameters to be extracted. The characterization service is now available and has a US starting price of $50,000. Included in this price is the test structure design, measurement, and RC layout tool calibration. Customers who opt to employ their own or non-BTA test chips can use the measurement portion of the service only at a cost of $15,000. CA

***BTA Technology**, 4633 Old Ironsides Dr., Suite 200, Santa Clara, CA 95054; (408) 986-1011; www.btat.com.*
CIRCLE 472

Software Targets Tube Fabrication Market

A software tool jointly developed by Ditek Software Corp. and the Michigan-based Advanced Tubular Technologies, is designed to provide tube fabricators with a powerful method for drawing and engineering tube shapes. The tool, TubeCAD, is targeted at the automotive, aerospace, shipbuilding, and HVAC design and manufacturing industries. Powered by Ditek's high-performance graphics engine, DynaCADD, it not only offers an advanced command set and user interface, but automatic layout features as well. As such, it provides a complete engineering solution that will literally allow tube fabricators to develop tube layouts in a manner of minutes. The TubeCAD product is now available and supports both the Windows 95/98 and Windows NT platforms. Contact the company directly for pricing information. CA

***Ditek Software Corp.**, 60 West Wilmot St., Richmond Hill, Ontario, Canada L4B 1M6; (905) 771-0560; www.ditek.com.* **CIRCLE 473**

Extranet Solution Improves Product Development Process

IpTeam Suite version 2.0 is an Internet-based, secure product development environment that enables companies to include their suppliers in the development process. This extranet/intranet product works by making relevant information and processes accessible to team members across time, space, and organizations.

With the ability to host all aspects of a team's activity, the tool facilitates the capture, organization, and dissemination of product development information, including documents, messages, design rationale, multimedia objects, supplier knowledge, and events. One of its components is the Internet Notebook, which captures free-form drawing, audio, text, and snapshots of CAD drawings and features a comprehensive link and search capability. There's also the Internet Workbench, which is a general project centric framework; and the Document Vault document-management system. Other capabilities include the Tracking Center—a module for tracking the progress of the team against milestones and interdependencies; the Procurement Center—an RFP negotiation module; and the Supplier Center—a Java-based module for capturing and organizing knowledge on preferred suppliers.

Operating as a client-server application, the ipTeam Suite 2.0 runs on the Internet and can support multiple levels of standard security. Its functions are accessed through standard browsers. The ipTeam Internet Notebook comes as a separate client. Pricing depends on the configuration. CA

***NexPrise Inc.**, 2041 Mission College Blvd., Santa Clara, CA 95054; (408) 327-0330; www.NexPrise.com.*
CIRCLE 474

PDM Solution Now Available On Windows NT

The latest version of the PDM (product data management) solution, known as CMS version 6.6, can support a Windows NT application server. This is critical because the platform's cost-effective nature will make it possible to extend the CMS solution and the necessary product design and development information to multiple sites. It will also distribute applications throughout a company's entire enterprise or supply chain.

Capitalizing on NT's familiar graphical user interface, CMS 6.6 is able to minimize the learning curve of the average user. In fact, CMS 6.6 can be adapted to a company's specific business needs and deployed to production within just a few weeks. The CMS 6.6 enterprise-wide PDM solution is available now. Pricing depends on the specific tool configuration purchased. CA

***Workgroup Technology Corp.**, 91 Hartwell Ave., Lexington, MA 02421; (781) 674-2000; Internet: www.workgroup.com.* **CIRCLE 475**

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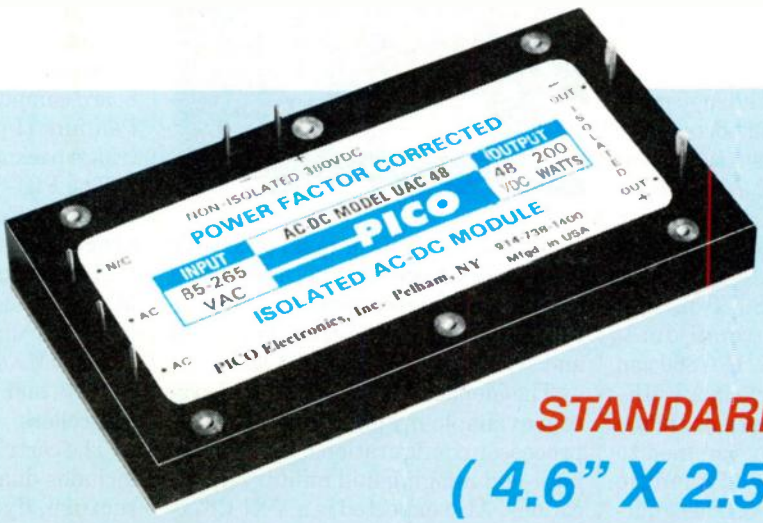

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READER SERVICE 99

IndustryPack Carrier Board Sports Power PC

The IndustryPack standard enjoys more widespread adoption and support than any other mezzanine standard. Now users can upgrade to higher performance and still retain their particular I/O scheme using the VIPC860 intelligent IndustryPack carrier board. The VIPC860, which is designed for high-end embedded applications that call for a mix of I/O requirements, features the 50-MHz MPC860T PowerPC processor, four modular IndustryPack (IP) sites, a high 100Base-T Fast Ethernet port, and four high-speed serial ports.

The VIPC860 features 4 Mbytes of nonvolatile flash memory as boot code and 16 Mbytes of EDO DRAM for MPC860T code and communications data. The flash and DRAM memories, in addition to the MPC860T on-chip RAM and registers, are all dual-ported and 32 bits. The VIPC860 can be run as a master or slave in a VME-bus system. Four independent IndustryPack sites can be programmed to either 8 or 32 MHz per IP module specification VITA 4-1995. This guarantees compatibility with over 300 IndustryPacks currently available in today's market.

Available now, the VIPC860 is priced at $2695. An optional board support package for the VxWorks operating system also is available for $1995. JC

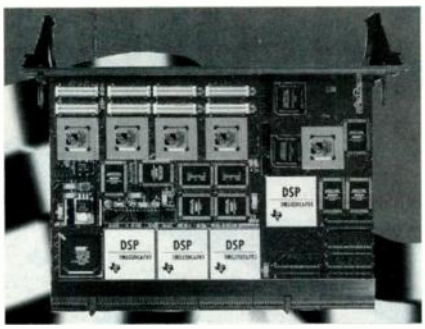
SBS GreenSpring Modular I/O, *181 Constitution Dr, Menlo Park, CA 94025; (650) 327-1200; fax (650) 327-3808; www.sbs-geenspring.com.*

CIRCLE 476

DSP Development Board Suite Supports C67 DSP Architecture

Because of the difficulty and time involved in creating DSP-based software, developers want access to all of the hardware they can get their hands on long before a new DSP chip becomes available. With this in mind, Spectrum Signal Processing announced four DSP systems supporting Texas Instruments' C67 DSP architecture. These four initial products are expected to become available one month after Texas Instruments releases the C67x silicon.

Spectrum's initial entry into the C67x arena will be with four system solutions. The Detroit67 is a cost-effective single-processor system suitable for both high-volume OEM products and for application-development systems. The Daytona67, a single- or dual-processor PCI system, and the



Barcelona67, a dual or quad processor CompactPCI product, both feature a distributed shared-memory architecture provided by the Hurricane chip and synchronous-burst SRAM.

The Monaco67 is a VME-based system available in single, dual, or quad processor configurations, suitable for high-end imaging and military applications. Also expected is a VXI C67x-based system for the wireless market, thereby providing a migration path to implement TI's latest floating-point processor to customers who are currently using C4x-based VXI systems.

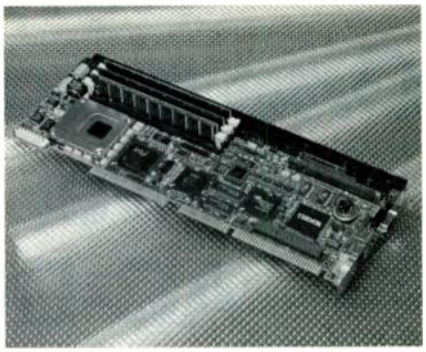
Spectrum's C67x systems feature Spectrum's PCI-to-DSP bridge called Hurricane. This ASIC was designed to increase I/O dataflow to and from the PCI interface at a sustained transfer rate of 132 Mbytes/s, and to use space very efficiently (low profile allows rear-board mounting). This performance feature is complemented by additional I/O capabilities.

The C6701 product series will be priced approximately 5 to 10% higher than the current C6201-based product line. JC

Spectrum Signal Processing, Inc., *8525 Baxter Pl., Burnaby, B.C., Canada; (604) 421-5422; fax (604) 421-1764; www.spectrumsignal.com.* **CIRCLE 477**

Industrial PCI Board Sports Pentium II Mini-Cartridge

The Pentium mini-cartridge is one way around the awkward packaging style of Intel's Pentium II. Teknor Industrial Computers from Quebec, Canada, announced the release of the PCI-941, the first industrial single-board computer using the Intel Mobile Pentium II processor in the mini-cartridge package.



The PCI-941 CPU features a 64-bit 233- or 266-MHz Mobile Pentium II processor, 440BX AGPset; a 64-bit PCI flat-panel/CRT controller with 2 Mbytes of EDO DRAM; a PanelLink interface; and high-performance PCI Ultra DMA/33 IDE, Ultra Fast/Wide SCSI 3, and 10/100Base-TX Ethernet controllers.

The cartridge Pentium II processor includes dual-independent bus architecture, dynamic execution, Intel MMX technology, and a closely coupled 512-kbyte, 64-bit, level 2 cache. Error checking and correction (ECC) is done using standard 72-bit, 66-MHz SDRAM. Universal Serial Bus (USB) ports, serial/parallel ports, a floppy interface, CompactFlash disk support, and PC/104-Plus connectors also are on-board.

The Award BIOS, in bootable flash memory, supports serial/parallel port remapping, disable, keyboard disable, console redirection, and the Advanced Configuration and Power Management Interface (ACPI). Among the other features are a CPU temperature monitor, a two-stage watchdog timer, a power/fail circuit, and a two-year warranty.

Available this summer, the single unit price of the PCI-941 with an Intel 233-MHz Mobile Pentium II processor (without video controller or SDRAM memory) is $2650. JC

Teknor Industrial Computers Inc., *616 Cure-Boivin, Boisbriand, Quebec, Canada J7G 2A7; (514) 437-5682; fax (514) 437-8053; or on the Internet: www.teknor.com.*

CIRCLE 478

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Mini-DIL Laser Diode For Subscriber Optical Networks

A new low-cost 8-pin plastic Mini-DIL (Dual In-Line) laser diode is now available for use in high-bandwidth subscriber optical data networking systems. Featuring an output power of 0.4 mW at a 1310-nm frequency wavelength, this new laser device provides an ideal light source for fiber-optic communications systems, providing data-transmission speeds of up to 622 Mbits/s.

In addition to reducing volume by 40%, the new package eliminates the time-consuming and expensive lead-bending operation normally required to prepare conventional 14-pin coaxial-type packages for installation onto a pc board. Furthermore, these new laser devices utilize the 8-pin assignment jointly proposed by Lucent Technologies, Nortel Ltd., and Hitachi, Ltd. that serves as a drop-in replacement for the 14-pin components. The plastic Mini-DIL laser diodes comply with Bellcore's 983 specification for temperature tolerances by offering a –40 to +85°C operating range.

The plastic Mini-DIL laser diode (part #HL1328DJS) is available for $60 each in quantities of 10,000. Samples can be purchased in the third quarter of this year, with volume quantities available in the first quarter of 1999. LG

Hitachi Semiconductor Inc., *2000 Sierra Point Pkwy., Brisbane, CA 94005; (800) 285-1601; fax (303) 397-0447; www.hitachi.com/semiconductor.*

CIRCLE 600

Multi-Rate DSL Data Pump For Many XDSL Applications

The SK70721 SK70725 chips comprise an Enhanced MDSL Data Pump (EMDP) chip set, which offers increased flexibility for IP, ATM, and voice, as well as better performance in long-distance applications. The SK70725 is a digital-signal-processing (DSP) component, and the SK70721 serves as the pump's analog front-end device. It's intended to be a cost-effective transport solution for Internet access equipment, fractional or full T1/E1 transport systems, digital pair-gain systems, and wireless base-station access systems.

The chip set consists of a variable-rate transceiver, which provides symmetric full-duplex communication on one twisted wire pair using a 2B1Q line code with echo cancellation. The SK70725 incorporates all of the DSP required for analog-to-digital conversion, echo cancellation, data scrambling, and adaptive equalization, as well as transceiver activation state-machine control. The SK70721 includes an DAC, filters, and transmit line drivers. Together, they support data rates from 272 to 1168 kbits/s. The EMDP achieves better performance than earlier products over long loops in low noise environments by widening the dynamic range and modifying the digital gain-control algorithm.

An on-chip, programmable activation controller and flexible framing options enables users to design interoperable systems when the opposite end is designed with data pumps from other IC vendors. A new enhanced micro-interruption feature allows the chip set to automatically maintain the connection during short term line disturbances like lightning strikes.

The SK70725 Enhanced MDSL Digital Signal Processor is packaged in a 44-pin PLCC. The SK70721 IAFE comes in a 28-pin PLCC. The MDSL data pump chip set is now available in volume production and priced at under $25.76 in quantities of 1000. LG

Level One Communications Inc., *9750 Goethe Rd., Sacramento, CA 95827; (916) 854-1155; e-mail: litreq@level1.com; www.level1.com—ask for literature package LO1P007.*

CIRCLE 601

GaAs Push-Pull Power FETs Push 120 W for PCS and MMDS

A family of six GaAs power RF FETs offers designers levels of output power ranging from 35 to over 120 W. The "FLL400IP-2/-3, FLL600IQ-2/-3 and FLL1200IU-2/-2A" family members are characterized for linear Class AB base-station applications from 1.8 to over 2.7 GHz using a supply voltage of only 12 V. Typical gains exceeding 10 dB and linear efficiencies better than 43% permit design of high-efficiency transmitter output stages for PCS, PCN, MMDS, and WLL utilizing GSM, TDMA, CDMA, and complex xPSK modulation techniques. Ultra linear "Class A" operation is permitted with a reduced supply voltage of 10 V.

By combining two GaAs power FETs into a single ceramic and metal, low-thermal-resistance, high RF performance package, the devices simplify the physical construction of high powered base stations for new L, S, and C band "point to point" and "point to multipoint" systems. This dual transistor construction also simplifies the electrical and RF design by permitting the use of simple 50-Ω baluns for impedance matching in both the input and output networks.

Available now, pricing for 100-piece orders ranges from $103 for the 35-W-rated FLL400IP through $307 each for the FLL1200IU, which can handle a maximum of 120 W. LG

Fujitsu Compound Semiconductor, Inc., 2355 Zanker Rd., San Jose, CA 95131-1138; (408) 232-9500; fax (408) 428-9111; e-mail: sales@fcsi.fujitsu.com; www.fcsi.fujitsu.com/technews/documents/construct.htm.

CIRCLE 602

G.Lite ADSL Chips Use Host CPU To Cut Cost and Power

The SAM (Scalable ADSL Modem) chip set uses a combination of its own logic and it's host PC's surplus MIPS to add low-cost, high-performance ADSL capabilities to PCs, set-top boxes, notebook computers, PDAs, etc. The two-chip set and its host processing software support the ANSI

T1.413 standard for ADSL, as well as the emerging G.Lite standard for splitterless service. The SAM chip set consists of host software, the IX9816 digital chip, and the IX8134 analog front end. The host software is provided on a diskette as assembled Windows 98 object code. It performs the high-level ADSL processing functions, and communicates to the

(continued on page 133)

(continued from page 132)
IX9816 via a PCI interface.

The IX9816 digital chip uses state-machine architecture to execute partial ADSL modulation functions, and FFT and IFFT processing. The IX8134 analog front-end chip uses two 12-bit digital-to-analog converters and a set of filters to shape the ADSL waveforms going out over the telephone lines. The SAM chip set includes software that does ADSL processing using the available power of a PC's host CPU. This allows the software to be modified to conform to changes in future ADSL standards. Together, they can achieve downstream transfer rates up to 1.5 Mbits/s, and 384-kbit/s upstream transfer rates in accordance with the proposed G.Lite standard.

The SAM Chip Set and software will be sampling in November with production in the first quarter of 1999. The chip set, including software, is priced at $40 in 1000s. The IX9816 digital chip is available in a 160-pin PQFP, and the IX8134 analog front-end chip comes in a 64-pin TQFP. LG

Integrated Telecom Express Inc., *2710 Walsh Ave., Santa Clara, CA 95051; Yi-Ju Chen, (408) 980-8689, ext.252. e-mail: yi-ju.chen@itexinc.com www.itexinc.com.* **CIRCLE 603**

3-Port Ethernet Switch Cuts Cost Of Cascadable 10/100 Hubs

The NP313 is a three-port, 10/100-Mbit/s Fast Ethernet switching engine, designed to make cascadable dual-speed hubs available to the price-sensitive SOHO and workgroup markets. This system-level IC enables hub vendors to build full-performance, cascadable dual-speed hubs at a total system cost of less than $10 per port. It provides both 10/100 bridging in a dual-speed hub configuration, plus traffic regulation between workgroups.

The switch's three MII ports enable designers to provide separate data paths for 10- and 100-Mbit/s traffic, eliminating the bottlenecks associated with traditional repeaters. Because the NP313 has a switch-based bus, it can carry both 10- and 100-Mbit/s traffic at full wire speed. The third MII port provides a full-speed, full-duplex, 100-Mbit/s uplink port for cascading between workgroups or connection to a backbone. Because the circuit has an automatic MAC address learning and aging capability of up to 8000 addresses, it automatically isolates the traffic of 10- and 100-Mbit/s segments from each other, allowing workgroups to maintain the full data-transfer performance between nodes on the segment.

The NP313 can intelligently manage three operation modes, including store-and-forward mode. All three ports are self-managed, and can automatically sense half-duplex and full-duplex mode. It features a cut-through mode with a very short latency of 3 µs, making it ideal for multimedia-intensive networks. Backpressure flow control regulates traffic, while intelligent buffer management provides efficient switching and fairness among all ports.

A complete reference system design and evaluation kit for a 16-port, cascadable, dual-speed switching hub also is available. It includes an evaluation board with the NP313, a bill of material, pc-board schematics, Gerber files, and embedded software.

Housed in a 208-pin PQFP package, the NP313 is available now in full production quantities. Samples of the NP313 are $40 and $15 to $25 per unit in production quantities.LG

NeoParadigm Labs Inc., *2730 Orchard Pkwy., San Jose, CA 95134; (408) 432-0900; fax (408) 432-9021 www.neoparadigm.com.* **CIRCLE 604**

1024-Channel SAR Links Local ATM To Telco Voice Networks

The MT90500 is a multichannel ATM AAL1 SAR that performs ATM Adaptation Layer 1 (AAL1) segmentation and reassembly (SAR) tasks. It's capable of simultaneously processing as many as 1024 bidirectional ATM virtual-channel (VC) connections in compliance with ANSI T1.630 and ITU I.363 requirements, in order to terminate 1024 full-duplex voice channels at 64 kbits/s. In addition to ATM Adaptation Layer 1 SAR functions, the MT90500 device also provides the means to handle 'AAL0 voice' or 'AAL5 voice', following the ATM Forum standards for Voice and Telephony Over ATM (VTOA).

The device directly interfaces with off-the-shelf ATM transceivers to telephony-based backplanes typically found in PBXs, Central Offices and ATM Access Concentrators, making it ideal for highly integrated multiservice access platforms that use hybrid ATM and TDM bus backplanes. Other applications include PSTN ATM Edge switches and DSLAM to PSTN interface system design. It can concentrate connections originating from up to 42 T1s or 32 E1s in a single-chip solution. The versatile SAR features flexible aggregation (n by 64) allowing any combination of 64-kbit/s TDM channels to be assembled into a particular ATM VC while maintaining frame integrity.

Its TDM bus supports ST-Bus, SCSA, MVIP and other popular serial data streams at 2.048-, 4.096- and 8.192-Mbit/s rates. Due to the TDM backplane termination capabilities and built-in clock state machines, the MT90500 suits systems that handle TDM clocks in ATM networks. The MT90500 device can also be used in multichassis switching systems for larger CTI apps. An evaluation platform, the MEB90500, is offered in PC form-factor cards with an ISA bus connection and runs on the Windows NT operating system.

The MT90500 is offered in a 240-pin PQFP package, and is priced at $150.45 in 1000-piece quantities. The evaluation kit is available now for $2695. LG

Mitel Corp., *350 Legget Dr., P.O. Box 13089, Kanata K2K 1X3, Canada; (613) 592-2122, fax (613) 592-6909, www.mitelsemi.com.* **CIRCLE 605**

High-Performance Line Driver For G.Lite ADSL

The DRV1101 is a low-cost, 5-V line driver offering the linearity and speed required for high speed data transfer in Asymmetrical Digital Subscriber Line (ADSL) systems employing the G.Lite standard. Operating on a single 5-V supply, the DRV1101 can supply up to 230-mA peak output current with an output voltage swing of 7 V p-p. In an ADSL system, the DRV1101 supplies 10-dBm average line power with a crest factor of 5.3 for a peak line power delivered of approximately 25 dBm. The DRV1101 is priced from $2.95 in 1000s and is available in an 8-lead SOIC package. Delivery is from stock. LG

Burr-Brown Corp., *6730 S. Tuscon Blvd., Tuscon, AZ 85706; (800) 548-6132, (520) 746-1111, fax-back: (800) 548-6133; e-mail: pawlik_mike@burr-brown.com, www.burr-brown.com.*

CIRCLE 606

Low-Power Design

Center Suisse d'Electronique et de Microtechnique SA & Electronic Design

This collection of papers focusing on the minimization of power consumption features general tutorials, digital circuits, devices and analog circuits of low-power systems.

Softcover book, $125.00, Item B4023PM

Portable by Design, Proceedings of the Fifth Annual Conference

Electronic Design

In an industry that is constantly changing from year to year, this 1998 conference overview features the latest developments on topics such as: Rechargeable Batteries, CPU's and DPU's for Portable Devices, Portable-System Software Issues, Infrared Data, Architectural Issues, Packaging Concerns, plus many other features relavant to those working inthe field of portable design. Held February 9-12, 1998 in Santa Clara, CA.

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A New Service Model Of Distribution For Avnet

Avnet Inc., of Phoenix, Ariz., has integrated three divisions of the company, Hamilton Hallmark, Time Electronics, and Penstock, into one operating group, Avnet Electronics Marketing. The new operating group consists of a customer management organization divided by the customers needs.

Customers will now have complete access to to the products and services of the former Hamilton Hallmark, Time Electronics, and Penstock divisions. Steve Church, formerly president of Avnet OEM Marketing Group, will serve as president of the new operating group in the Americas.

The new division will also be able to offer their customers access to more focused services and financial models. Within the new division are smaller more specific departments, Avnet Design Services, Avnet Integrated Materials Services (IMS), Allied, Avnet Personal Computer Components. Avnet Design Services is trying to become a one-stop shop for engineering and technical services for its customers. It's offering many new services, such as turnkey logic designs, reference designs, and product designs. It also gives creation services for suppliers. The IMS provides customer-specific materials management. It includes leading-edge information technology-based services, and pinpoint logistics. Allied offers catalog, CD ROM, and Internet sales to R&D, MRO, and small OEM customers. Avnet Personal Computer Components offers microprocessors, motherboards, memory, networking products, as well as mass storage to PC OEMs and systems integrators in North America.

This reorganization is the result of an extensive four-month evaluation. The company interviewed approximately 1,200 customers, 15 suppliers, and 1000 employees. It also performed benchmarking surveys on best-in-class companies in the electronics distribution industry and several others. The main findings of the evaluation were that customers wanted access to Avnet's entire line card and value-added services through a single account manager. Customers also wanted account managers who focused on customers with similar business and technical needs, and sales representatives who are product experts and work in close geographic proximity.

Avnet Electronic Marketing has the following five objectives:

- To deliver more services at a lower cost.
- Become a company that can move more quickly and be more flexible.
- Reduce or eliminate the time spent on internal issues to better focus on customers
- Employ sales experts with more selling time, devoted to understanding and meeting the needs of customers
- Improve specific product and general product expertise

For more information, visit Avnet's web site at www.avnet.com.

Galco Named Distributor For Extech And Hoyt

Galco Industrial Electronics, Madison Heights, Mich., has been rather busy lately. It has just been named the authorized distributor for both Extech Instruments, in Waltham, Mass., and Hoyt Electrical Instruments Works.

Extech is a major manufacturer and supplier of test instruments, data loggers, calibration equipment, and portable printers. Specifically, Extech's product offerings include calibrators, multimeters, lightmeters tachs, thermometers, strobes, scales, power supplies, displays, and temperature probes. Galco hopes that Extech will assist them in providing their customers with high quality products, at reasonable prices.

Hoyt is a leading manufacturer of analog panel meters. According to Galco, the two companies plan for Galco to become a full service modification center. They hope to use their kit-building abilities to offer a wide range of analog meters, and still stock the few required components to build the numerous models.

For more information on either Extech's or Hoyt's lines, visit Galco's web site at www.galco.com or call Galco at 1-800-521-1615.

BestSystems To Distribute For Alta Technology In Japan

Alta Technology, Sandy, Utah, has named BestSystems Inc., Tsukuba Science City, Japan, as its Japanese distributor, effective immediately. BestSystems will take over the distribution in Japan, as well as begin handling all of the customer service and technical support issues for the area.

BestSystems will focus most of their efforts on the distribution of Alta's high performance CompactPCI products and the brand new AltaCluster product line. Compact PCI consists mainly of processor and peripheral board-level products, and fully integrated systems. The leading product is the CPCI/SBC-A500, a 500 MHz single board computer based on the ultra fast Digital Semiconductor Alpha 21164 microprocessor. It includes 2 MB of L3 cache, up to 1024 MB of DRAM, and a PMC slot for flexibility. They plan to announce a 21264 version, with clock speeds of 700 MHz and greater in the third quarter of 1998. Other products from Compact PCI include the PCI mezzanine cards (PMC) carrier boards, 3D graphics accelerators, FPDP interfaces, and multifunctional I/O and system expansion boards.

The AltaCluster systems are modular and scaleable clustered computers that provide eight compute nodes in a box. Each node has a standard ATX motherboard with 533 MHz Alpha or Pentium II processors that run at up to 400 MHz. Alta has also developed a system for power sequencing, temperature monitoring or control, and remote reset of individual nodes. If you want faster inter-processor communication, Alta also offers Gigabit Ethernet and Myrinet solutions.

For more information, visit Alta's web site at www.altatech.com, or BestSystem's web site at www.bestsystems.co.jp/.

Sager Goes World Wide For SEI Electronics

SEI Electronics, Raleigh, N.C., authorized Sager Electronics, of Hingham, Mass., to distribute all of SEI resistive products on a world-wide basis. SEI has been manufacturing solely resistive products since it was founded over 80 years ago. Just about every aspect of the electronics market uses SEIs products. According to Sager, both companies feel that the union is a good match. The main focuses of each is customer service, and using technology to simplify the way that business is done.

For more information, visit Sager's web site at www.sager.com, or SEI's web site at www.seielect.com.

Hitachi Flat Panel Displays To Be Distributed By Avnet

Hitachi Electronics Devices (USA Inc.) has agreed to have Avnet Electronics Marketing distribute their flat panel displays. The deal includes the Active Matrix TFT, STN, and Super TFT panels.

Hitachi's flat panel displays feature "Super TFT" technology with in-plane switching which offers 160 degree viewing angle, 200 cd/m^2 brightness level, and deep color saturation levels. The TFT flat panel display has Flip Chip Attachment (FCA) technology that has added durability, and reliability, and allows the user to use fewer interconnects. Also, the color and monochrome passive matrix displays offer transmissive, transflective, and reflective modes in a range of resolutions from 1/8 to full VGA.

The deal benefits Avnet in a number of ways as well. It has full integration capabilities, including interface boards, custom cases, and systems integration.

For more information, contact Avnet at em.avnet.com.

Compiled and edited by Lisa Calabrese, editorial intern.

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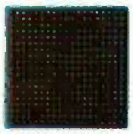

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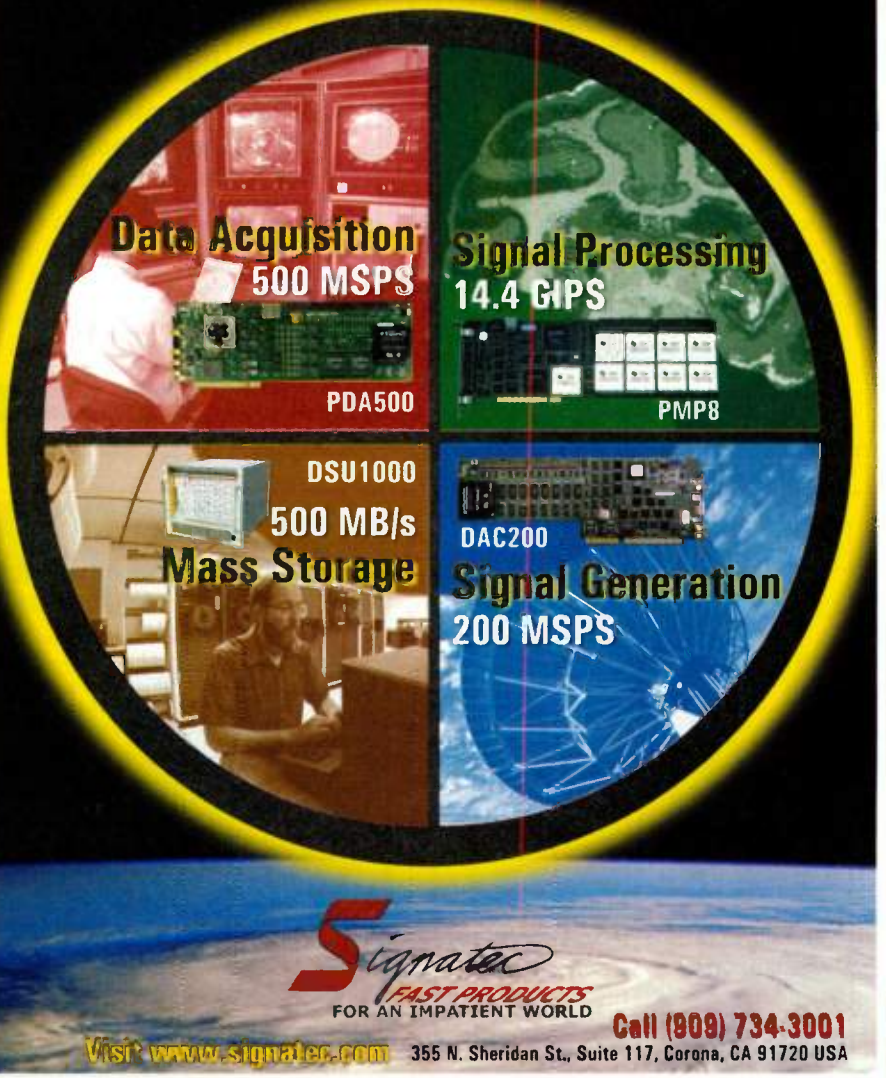

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January 26	12/16/97
Febuary 9	12/30/97
Febuary 23	1/3/98
March 9	1/27/98
March 23	2/10/98
April 6	2/24/98
April 20	3/10/98
May 1	3/21/98
May 13	4/2/98
May 25	4/14/98
June 8	4/28/98
June 22	5/12/98
July 6	5/26/98
July 20	6/9/98
August 3	6/23/98
August 17	7/7/98
September 1	7/22/98
September 14	8/4/98
October 1	8/21/98
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October 22	9/11/98
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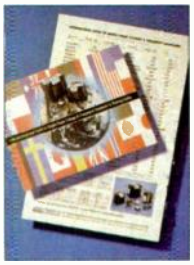

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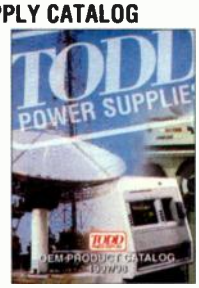

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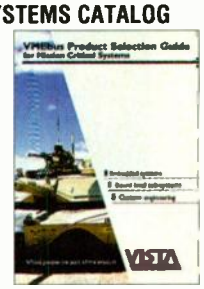

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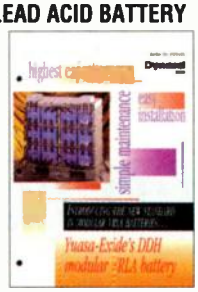

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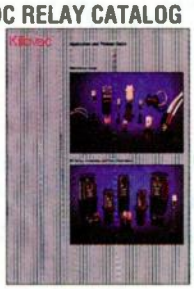

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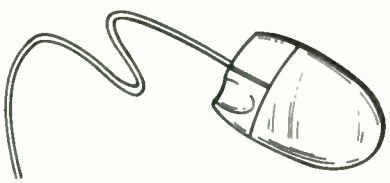

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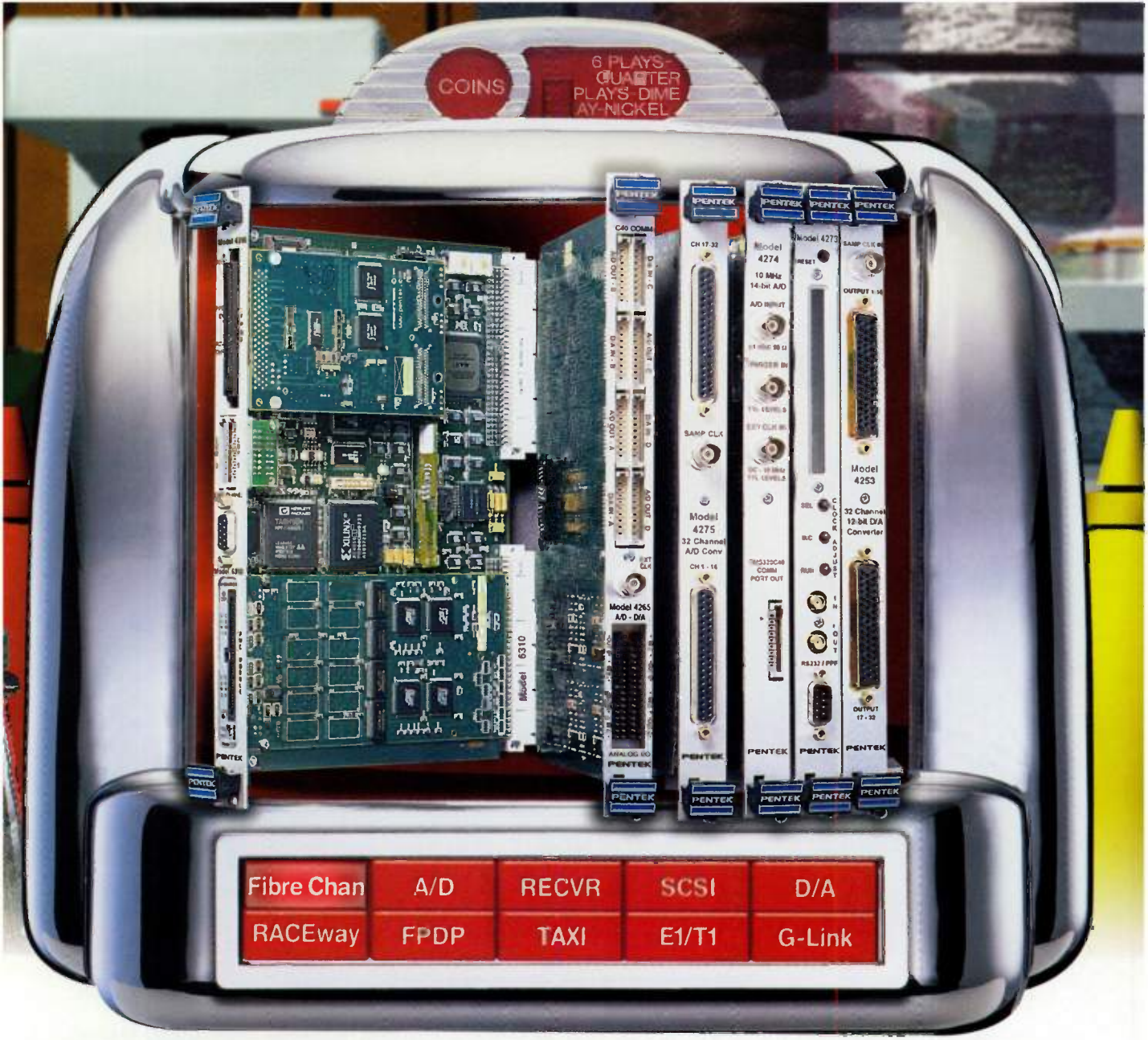

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