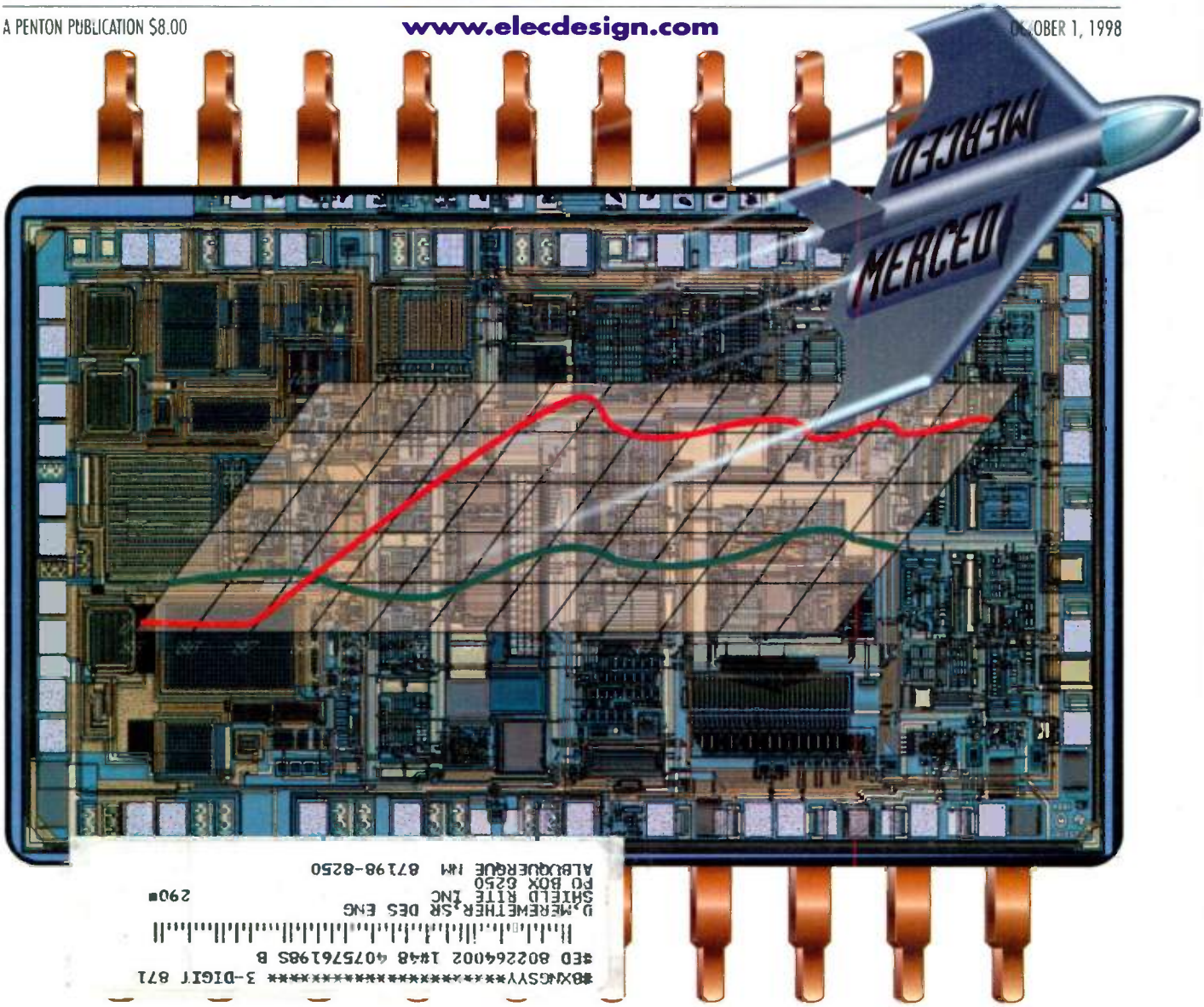
Periodicals Postage Paid USPS Penton Automatable Poly

ELECTRONIC DESIGN

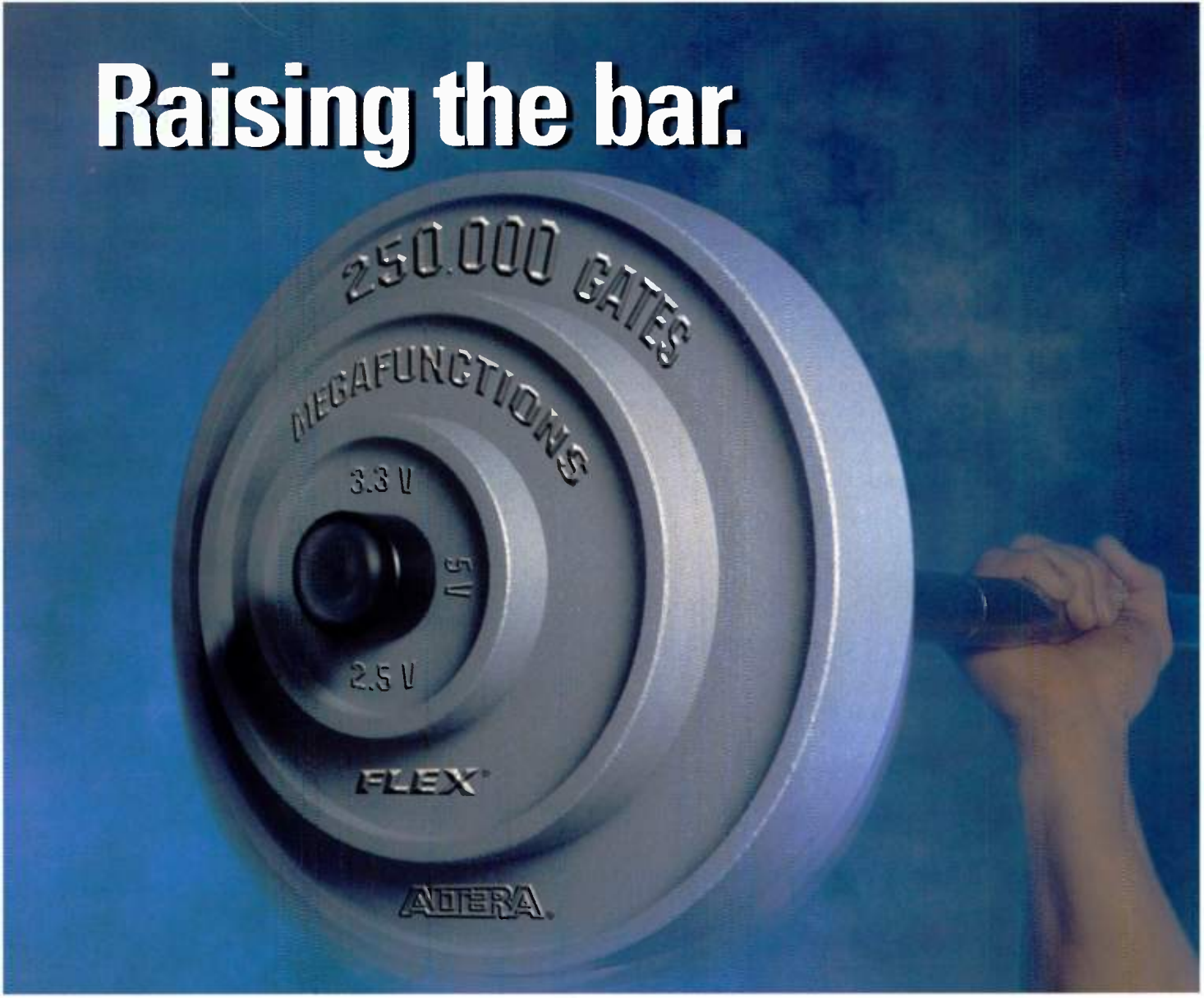
TECHNOLOGY • APPLICATIONS • PRODUCTS • SOLUTIONS

A PENTON PUBLICATION $8.00 www.elecdesign.com OCTOBER 1, 1998



Ripple Regulator Lets Merced Take Flight p. 33

Raising the bar.



250,000 gates strong.

The newest, largest member of the FLEX® 10K embedded programmable logic family — the EPF10K250A — is now available. The EPF10K250A device combines the flexibility of programmable logic with the capacity and speed you need for even your largest gate array designs.

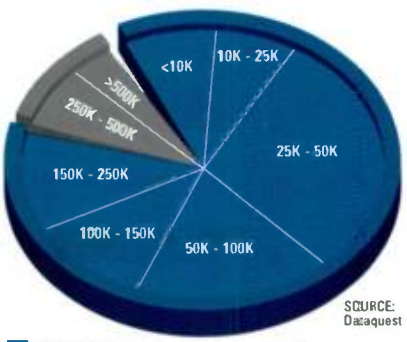
Pump up your design efficiency.

Whether you use VHDL or Verilog HDL, our easy-to-use MAX+PLUS® II development system fits into your existing design flow. The MAX+PLUS II software interfaces with all leading EDA tools, giving you the best quality of results with the most efficient combination of speed and area. Altera MegaCore™ and AMPP℠ megafunctions, which are optimized for Altera device architectures, further increase design efficiency.

When only the biggest will do.

With 250,000 gates, the EPF10K250A covers 80% of gate array design starts. This device provides a 3.3-V core voltage with MultiVolt™ I/O to interface to 5.0-, 3.3-, and 2.5-V systems, and is available in packages of up to 600 pins, including BGA options.

Gate Array Design Starts by Gate Count (1997)



SOURCE: Dataquest

FLEX 10K device density covers more than 80% of gate array design starts.

The biggest — bar none.

Visit the Altera web site for more information about all FLEX 10K devices — and sign up for a free megafunction literature pack. Use the integration density of the EPF10K250A to raise the bar on your competition.

www.altera.com/bar

The ALTERA Advantage

WRH

Double your port density and reduce your system costs with HP's new MT-RJ fiber optic transceivers.

Next generation networking equipment can now achieve the same port spacing as RJ-45 copper systems - but with fiber optics. That's because the MT-RJ transceiver family is approximately half the width of today's duplex-SC fiber interface. This increased port density means more bandwidth per card with lower overall system hardware cost compared to existing fiber interfaces.

HP's MT-RJ transceivers are available in a 2x5 multi-source Small Form Factor (SFF) package for a variety of applications including Fast Ethernet, Gigabit Ethernet, ATM, SONET/SDH and Fibre Channel with speeds ranging from 100 Mb/s through 1.25 Gb/s. Add to that, availability of multimode and singlemode capability with 850 nm VCSELs, 1300 nm LEDs and 1300 nm FP lasers and you have the largest selection in the smallest packages.

Not only has HP reduced the size, but we know how to reduce your design worries too. With our proven, high-volume manufacturing and world-class application support, we'll work with you now to design your higher-bandwidth, lower-cost systems and get you to market faster.

MT-RJ - the next generation transceiver. Available now.

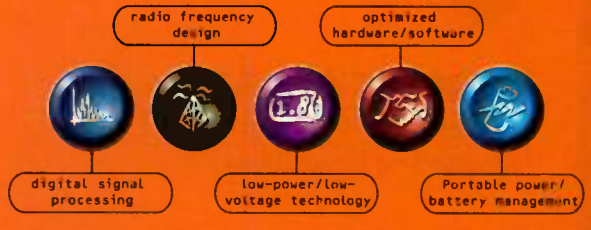
www.hp.com/info/small

Check out our website or call:
1-800-537-7715 ext. 9978

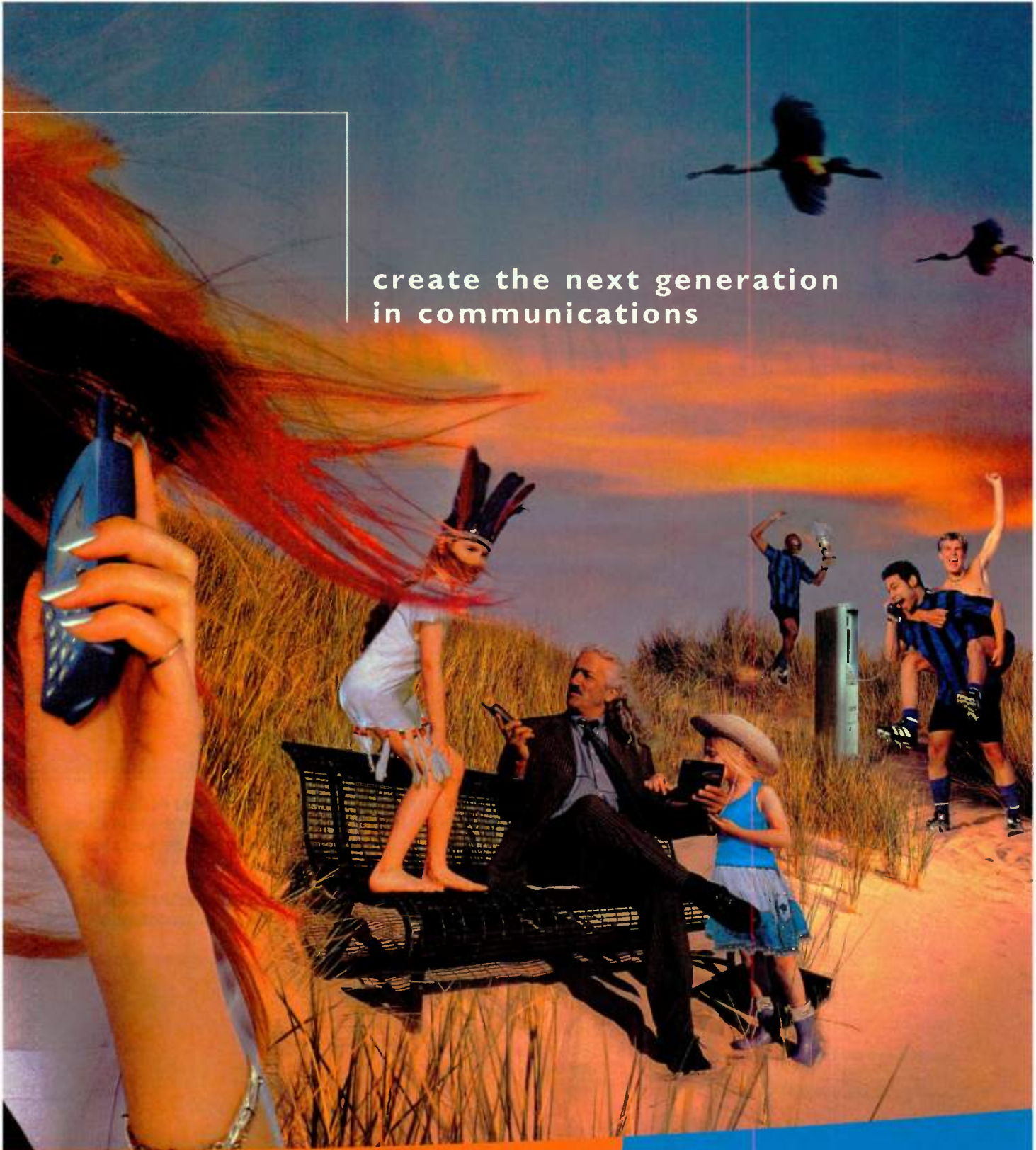
HEWLETT® PACKARD
Expanding Possibilities

CSSD9804
READER SERVICE 107

Let's...



Mobile phones mean freedom to communicate wherever and whenever we choose. **Philips Semiconductors** is ready today with the competences and solutions you need to take that freedom to the next generation. Baseband (embedded DSPs), RF design and low-voltage/low-power technologies are at the core of our expertise. And our competence in hardware/software optimization, power management, mixed-signal ICs, speech recognition, LCD driver technology, packaging and MCMs, - along with the industry's broadest range of discretes - adds up to

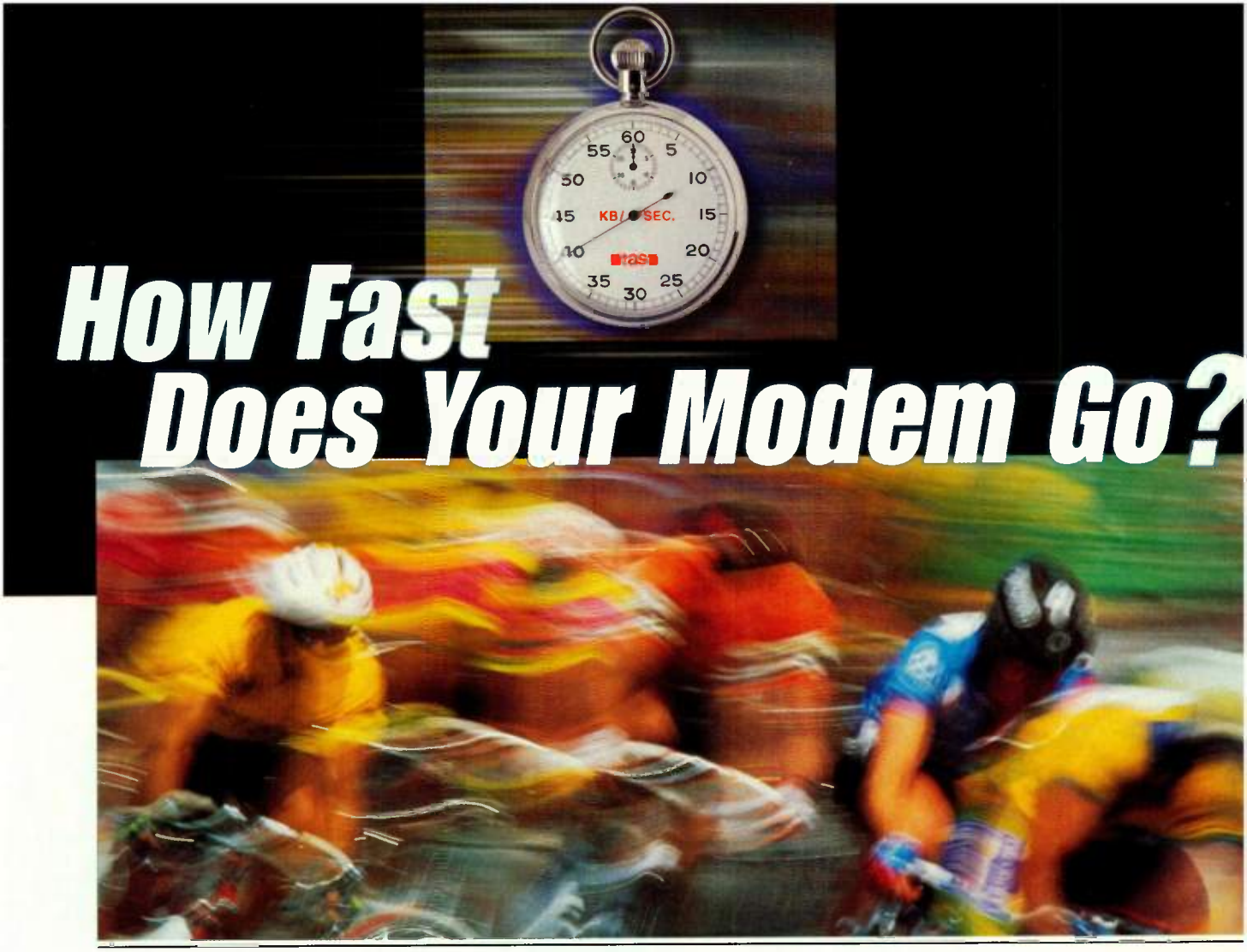


a capability that has made us a world leader in wireless communications ICs. With solutions covering the major mobile standards - digital cellular and cordless, paging, wireless data/LANs and GPS - Philips Semiconductors frees you to create the communications products for tomorrow's generation. To find out more, visit www.semiconductors.philips.com/comms/ or call for more information USA 1-800-447-1500, ext. 1580. Europe fax +31-10-284-3181, quote "voice". Asia fax +852-2811-9173, quote "ED".

READER SERVICE 143

PHILIPS

Let's make things better.

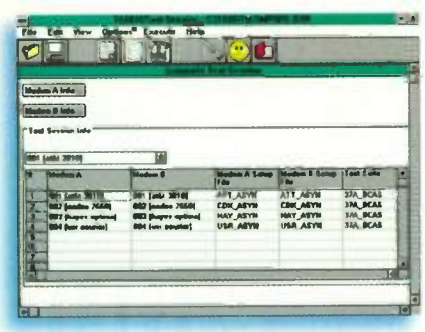


How Fast Does Your Modem Go?

In the hotly contested modem business, you need the tools that will put your product in the winner's circle.

TAS has been providing advanced test and evaluation solutions to modem industry leaders *for over twelve years.*

With the advent of *new* modem technologies **such as 56K,** *accurate and repeatable testing is more important than ever!*



Now TAS modem test systems deliver even more power and flexibility to help ensure the success of your product.

- ***TAS Series II PLUS*** *and 100 Series Telephone Network Emulators are the "gold standard" of modem testing worldwide. These advanced instruments provide accurate, repeatable emulation of telephone exchange conditions, analog impairments, and digital transmission facilities.*
- ***The TAS 240*** *Subscriber Loop Emulator tests your modem's ability to deal with the wide variety of central office to subscriber connections — an especially critical factor for V.34 and 56K modems.*
- ***Gemini & Gemini-PC*** *data analyzers thoroughly test the throughput and error-rate performance of external, PC-Card, and controller-less modems.*
- ***TASKIT® Software*** *automates the entire testing process and gives you comprehensive performance reports.*

If you are testing or evaluating subscriber or central site modems, give your product the best chance to win the race.

Go with the advanced modem test and evaluation solutions from TAS.

tas®

Telecom Analysis Systems, Inc.

34 Industrial Way East ▪ Eatontown, NJ 07724-3319 ▪ Phone: (732) 544-8700 ▪ FAX: (732) 544-8347 ▪ Email: sales@taskit.com ▪ Internet: http://www.taskit.com

READER SERVICE 132

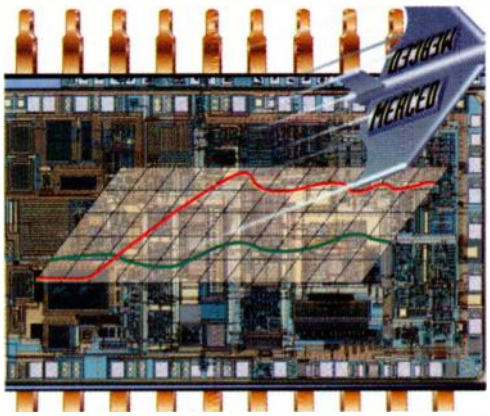
A Penton Publication

ELECTRONIC DESIGN

TECHNOLOGY • APPLICATIONS • PRODUCTS • SOLUTIONS

October 1, 1998 Volume 46, Number 22

EDITORIAL OVERVIEW



DEPARTMENTS

TECH INSIGHTS

EMBEDDED SYSTEMS

PIPS

Penton

ELECTRONIC DESIGN (ISSN 0013-4872) is published twice monthly except for four issues in May and October, three issues in February, and three issues in November by Penton Media Inc., 1100 Superior Ave., Cleveland, OH 44114-2543. Paid rates for a one year subscription are as follows: $100 U.S., $170 Canada, $180, $200 International. Periodicals postage paid at Cleveland, OH, and additional mailing offices. Editorial and advertising addresses: ELECTRONIC DESIGN, 611 Route #46 West, Hasbrouck Heights, NJ 07604. Telephone (201) 393-6060. Facsimile (201) 393-0204. Printed in U.S.A. Title registered in U.S. Patent Office.

When A Leading Canadian Electronics Company Needed Reliable Infrared Switches,

It Got Them From QT Optoelectronics.

Our Willingness To Work With You Sets Us Apart.

The standard plastic encapsulated IR switch couldn't survive the OEM's manufacturing process, much less the demanding application for which it was intended.

So design engineers from QT Optoelectronics worked with the customer's test engineers to develop and produce a metal case IR switch.

This is not unusual for QT Optoelectronics. Besides providing a wide range of standard components, the company is a leader in the design and production of custom IR products.

What is unusual is that the metal IR switch proved so popular with so many customers QT Optoelectronics now offers it as a standard product.

Of course we offer good products at a competitive price. We couldn't stay in business if we didn't. But it's our willingness, as well as our ability, to help a customer meet a unique requirement that sets us apart.

Call **1-800-LED-OPTO** for more information, or browse our on-line product catalog at **www.qtopto.com**.

QT OPTOELECTRONICS

United States 800-533-6786 • France 33 01/43.99.25.12 • Germany 49 089/96.30.51 • United Kingdom 44 01296/39.44.99 • Asia/Pacific 603/735-2417

WRH

A Penton Publication

ELECTRONIC DESIGN

TECHNOLOGY • APPLICATIONS • PRODUCTS • SOLUTIONS

October 1, 1998 Volume 46, Number 22

EDITORIAL OVERVIEW

DIGITAL DESIGN

SPECIAL SUPPLEMENT

QUICKLOOK

LOOKING AHEAD: October 12, 1998

Analog Design: A contributed Design Application article examines complex video signals that must be switched efficiently using commercially available switching arrays.

EDA Special Report: EDA Editor Cheryl Ajluni looks at the latest developments in advanced packaging tools for pc boards, that bridge the gap between IC and pc-board designs.

Test & Measurement: Test & Measurement Editor Joseph Desposito previews this year's International Test Conference (ITC), with emphasis on embedded cores.

COVER ILLUSTRATION BY: BRUCE JABLONSKI

Jesse H. Neal Editorial Achievement

1967 First Place Award	1978 Certificate of Merit
1968 First Place Award	1980 Certificate of Merit
1972 Certificate of Merit	1986 First Place Award
1975 Two Certificates of Merit	1989 Certificate of Merit
1976 Certificate of Merit	1992 Certificate of Merit

www.elecdesign.com

ELECTRONIC DESIGN ONLINE

TECHNOLOGY APPLICATIONS PRODUCTS SOLUTIONS

Info Source
- QuickLook
- Ideas For Design
- New Products Section
- Recent Issues

Technology Lab

Careers
- Job Bank
- Currents & Careers

Extras
- Columns
- Distributors

Community
- Book Shelf
- University
- Trade Shows
- Engineer Store
- Comedy Club

e-link

About Electronic Design

ONLINE OVERVIEW

October 1, 1998 Volume 46, Number 22

See Electronic Design Online's Table of Contents to preview what's in store for you on the web!

NOW ONLINE:

Get In On The Fun!

Beginning October 1, **Electronic Design** will be holding a contest for EEs who fancy themselves as creative writers. If you like to write short stories or enjoy composing poems, now's your chance to show off your skills. But here's the catch--your prose must contain as many names of EDA tool vendors as possible, and the piece cannot exceed 300 words in length.

The contest will run until November 30. Winners will be announced via **Electronic Design Online** on December 15, and they will be awarded one of a group of prizes donated by EDA tool vendors. Sound like fun? For further details, see our home page at **www.elecdesign.com.**

EDTN network

EXCLUSIVES

European telco industry group addresses issues close to their heart

NEWS

Up-to-the-minute industry news updates via the **EDTN Network**

TECHNOLOGY LAB

New standard enhances interactive cable TV services

NEW PRODUCTS SECTION

Link to the latest product features as reviewed by **EE Product News**

ELECTRONIC DESIGN ONLINE

—your best source for technical information on the World Wide Web!

One Powerful Web Site.

Power-One's on-line PROBE helps you select the right power supply for your application.

www.power-one.com

AC/DC and DC/DC — One to 4000 Watts	
DC/DC Converters	Over 100 Models from 1-30 Watts
AC/DC Linears	Over 70 Models from 6-280 Watts
AC/DC Low-Power Switchers	Over 100 Models from 30-250 Watts
AC/DC Mid-Power Switchers	Over 30 Models from 225-550 Watts
AC/DC High-Power Switchers	Over 10 Million Configurations from 500-4000 Watts

POWER-ONE®
POWER SUPPLIES

740 Calle Plano • Camarillo, California 93012
(800) 765-7448 • FAX (805) 388-0476

READER SERVICE 124

XILINX.
The leader in programmable logic design software.

Design Advantage	Ours	Theirs
1 Million Gate FPGA	✓	
Fastest Timing Driven Compile Time	✓	
Min. Timing Support	✓	
Volt/Temp Prorating	✓	
Graphical Constraint Entry	✓	✓
Push Button Performance	✓	

Check it out for yourself! Xilinx scores as the industry's most flexible and complete software solution available for programmable logic. And, with the introduction of version 1.5 for both our Alliance™ and Foundation™ Series Software, we now set a new standard for design simplicity.

It all starts with a push-button interface that delivers high-performance results for every device we make. From our 3.3V FastFLASH™ CPLDs, to our 1 million gate Virtex™ FPGA, Alliance and Foundation Series Software now offers an unrivaled feature set that guarantees optimized performance. We call it AKA *speed*™ technology. You'll call it the most intuitive and efficient tool-set you've ever used!

It's All About Software leadership

From the industry's broadest selection of pre-verified cores, to lightning fast compile times and board-level verification, Xilinx Foundation and Alliance Series software is designed to work the way you do. To deliver "hand-crafted" results...automatically!

www.xilinx.com

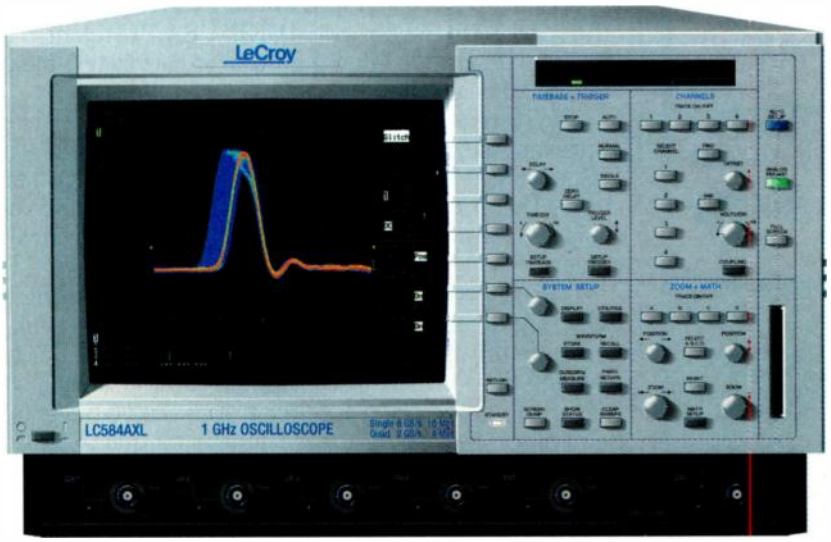
XILINX®
The Programmable Logic Company

READER SERVICE 138

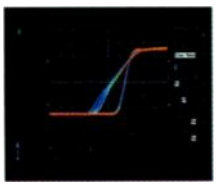
DPO?

Been there.
Done that.

Better. Faster.



Introducing the new LeCroy LC584AXL



- **Second-Generation Persistence Technology**
- **Longest Acquisition Memory**
- **Powerful CPU**

While some vendors have just announced the capability of capturing repetitive signals, formatting the data into a pixel map and then "digitally" aging the persistence display, LeCroy has provided this capability for two years. And now we have second-generation persistence technology that allows all the data in a persistence map to be used for precision measurements. The newest member of the LC family of color oscilloscopes sets two industry records: it provides 4 Mbytes of data acquisition memory per channel, and it offers a powerful CPU. If you work with complex signals, the extra memory and computing power will give you more precise signal capture and faster answers. Visit us on the web and see how to get there better and faster with LeCroy.

LeCroy

www.lecroy.com/axl 1 800 4LeCroy

READER SERVICE 163

EDITORIAL

IEEE Down On H-1B

The IEEE issued an "action alert" last month, urging its members and other technical professionals to tell Congress not to expand the H-1B visa program without providing worker safeguards. The IEEE has opposed the version of H.R. 3736 (passed by the House in July) which would raise H-1B visa limits by 190,000 over the next five years. This bill would also limit recruitment and no-layoff provisions only to employers whose H-1B employees constitute at least 15% of their workforce.

You'll recall that many high-tech industry suits want Congress to lighten up on restricting the number of foreign workers allowed to enter the land of opportunity. That way, those workers can catch the first available bus to their office parks. On the flip side, IEEE-USA President John R. Reinert isn't too thrilled with the idea that a portion of his 220,000-member U.S. engineering team could be standing in unemployment lines.

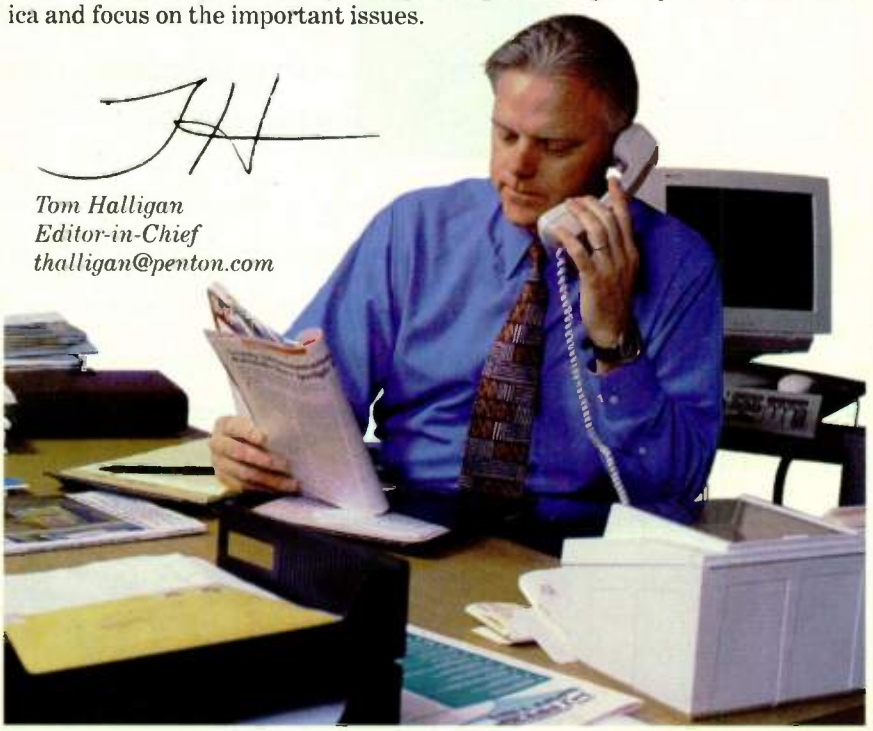
"The increase is too large and too long, and the worker safeguards too lax to prevent harm to our high-tech workforce and the long-term vitality of the U.S. technical infrastructure," says Reinert. He also fueled his argument by stating that in the past few months, 220,000 jobs have been cut by technology companies. And, the unemployment rate for electrical engineers has nearly tripled.

"If there ever was a bad time for Congress to bring in a half-million indentured, high-tech guestworkers, this is it," Reinert said.

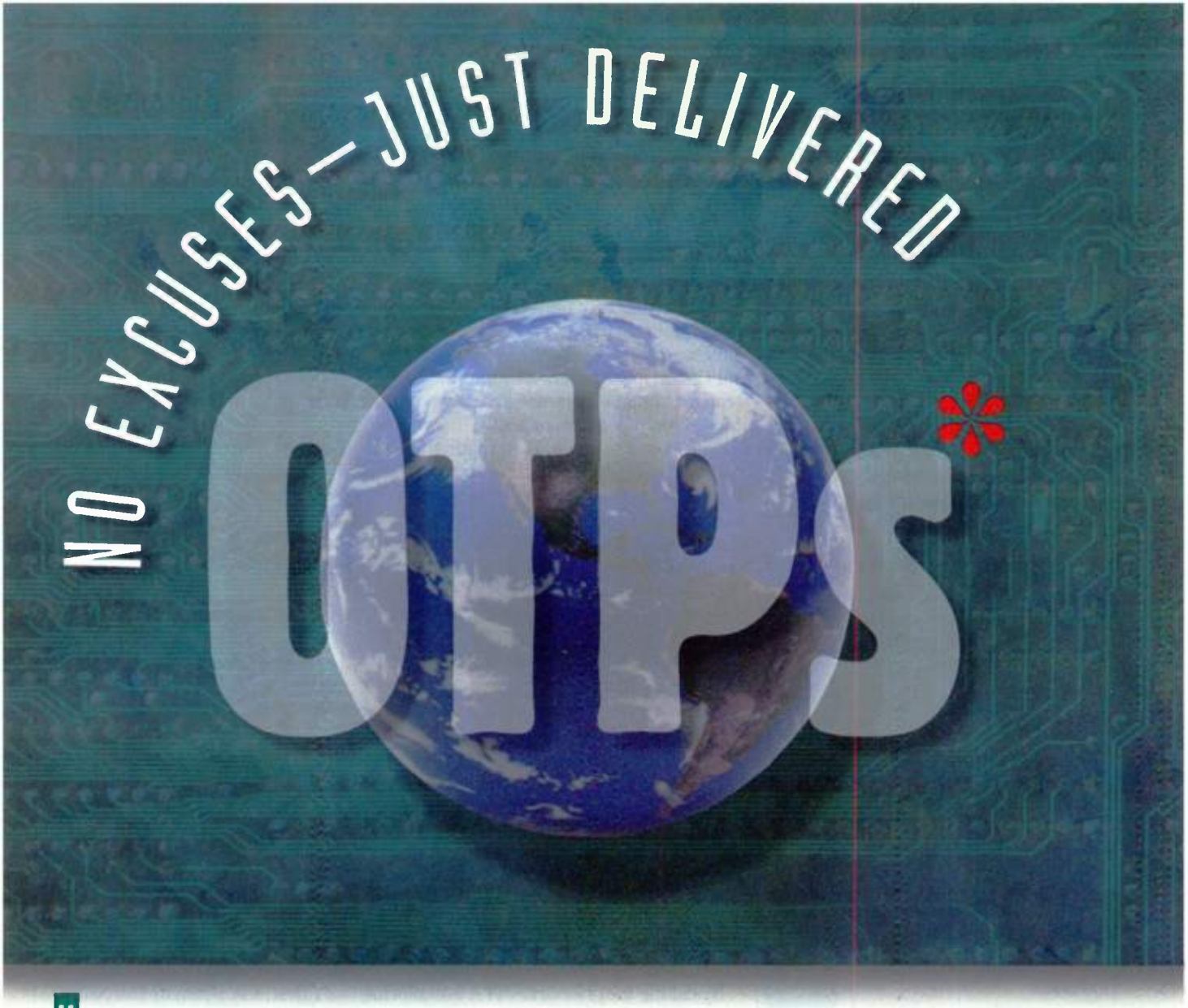
Apparently, proponents are scheduling a lot of lunch dates in Georgetown lobbying their favorite congressman to back the bill, which was scheduled to come to a vote in mid-September. And the IEEE is (as I write this in early September) getting its PR machine in motion to light a fire under its membership so they will voice their opposition to their favorite politician.

I received a ton of e-mail and letters from you when I addressed the U.S./foreign worker problem in previous editorials. The majority of you do not believe there is a shortage of skilled engineers in the U.S. And if there is, you point out, shouldn't the company invest in additional training to bring its engineers up to snuff? Or, as some e-mail noted, shouldn't the burden to upgrade skills be placed on the individual?

All very good questions. I just hope Congress can get beyond Bill and Monica and focus on the important issues.



Tom Halligan
Editor-in-Chief
thalligan@penton.com



You already know our "No Excuses" one-time programmable microcontrollers are available right now—right off the shelf. Our most popular OTPs listed below are available worldwide through most Motorola distributors.

Also available off that same shelf are four different levels of development support for each device—from free software on our website to high performance development tools.

- Free Windows® software
- $99† In-Circuit Simulator Kits (complete-fully assembled)
- $950† Real-Time In-Circuit MMEVS Development Kits (complete-fully assembled)
- $3,450† High Performance MMDS Development Kits (complete-fully assembled)

. . . all with complete documentation and software.

Visit our website for complete information

You don't need to search the universe to find everything you need—OTP device specs, application notes, development tools, third-party developers, product availability, distributors and additional information—all you have to do is reach for your mouse and visit our virtual OTP shopping mall on the Web.

We're dedicated to getting you the OTPs with the development support you need. When you need them. Visit www.motorola.com/semi/otp and see for yourself.

DEVICE	EPROM (bytes)	RAM	PINS	DESIGN-IN KIT	MMEVS KIT	MMDS KIT
68HC705KJ1	1.2K	64	16	M68ICS05J	KITMMEVS05KJ	KITMMDS05KJ
68HC705J1A	1.2K	64	20	M68ICS05J	KITMMEVS05KJ	KITMMDS05KJ
68HC705P6A	4.6K	176	28	M68ICS05P	KITMMEVS05P6A	KITMMDS05P6A
68HC705C8A	8K	304	40,44	M68ICS05C	KITMMEVS05C	KITMMDS05C
68HC705C9A	16K	352	40,44	M68ICS05C	KITMMEVS05C	KITMMDS05C
68HC705B16	15K	352	52,64	M68ICS05B	KITMMEVS05B	KITMMDS05B
68HC705L16	16K	512	80	KITPGMR05L16	KITMMEVS05L16	KITMMDS05L16

†Suggested resales

Digital DNA™ from Motorola

Paper Cuts, Ammonia Fumes, & Lawyers

I used to be a young engineer-in-training. "Drafting dog" was my informal job title. As part of Northeastern University's co-op program, I was a drafting dog on six-month cycles. During alternate six-month cycles, I studied toward my EE degree. The major requirements of the job included doing all the "dog" work in the drafting department.

I was constantly filing and making copies of engineering drawings—everything from schematics and fabrication drawings to assembly drawings. Occupation hazards arose, like the paper cuts made by the sharp edges of blueline paper and the strong stench of ammonia from the blueline machine. But, I stayed strong. I hung in there and actually became rather territorial about the drawing storage room. If someone took a drawing out to look at, I wouldn't let anyone file it again except me. I didn't want anything misfiled or misplaced. I ran a tight ship.

Recently, memories of those days filtered up from the depths of my brain. Late this summer, the VMEbus International Trade Association (VITA) called upon its members to search for prior art (drawings and other documents) related to a pair of patents that Nortel intends to enforce. Prior art, in this case, refers to documents dated before the Nortel patents were issued in 1985. Hearing about this, all I could picture were hundreds of managers of engineering departments sending drafting dogs like me searching through old flat files for drawings. I then imagined the drafting dogs making stacks of copies on the blueline machine.

JEFF CHILD
COMPUTER SYSTEMS

In case you haven't heard, there's a major tussle over patents going on in the bus/board business. Nortel, a formidable player in telecom and a member of VITA, claims the front-panel implementations that comply with the IEEE 1101.10 standard require technology for which Nortel holds the patents. Nortel sent letters to a number of companies with IEEE 1101.10-compliant products, asking them to contact Nortel regarding licensing requirements. Both front-panel keying and EMI shielding, as specified in IEEE 1101.10, is an important part of VITA 1.1-1997 (VME64x extensions to VME64), a proposed ANSI standard.

By calling for prior art, VITA is exploring two questions. First, do the Nortel patents cover 1101.10-compliant implementations? Second, if they do, does prior art exist that may not have come to light when the Nortel patents were issued? While patent examiners have a working familiarity with patent databases—and access to them—they may have missed prior art held in the public domain. Naturally, the manufacturers and users of VME technology are the best source for "public domain" prior art. VITA asked its members and VMEbus users to provide them with any prior art which may be applicable to front-panel EMI shielding and keying.

It's too soon to tell what the impact of the Nortel patent situation will be on the VME business. If forced to pay licensing fees on the technologies, some of the smaller VME vendors will suffer the most. CompactPCI board vendors are caught up in this, too, because CompactPCI also makes use of the IEEE 1101.10 front-panel technology.

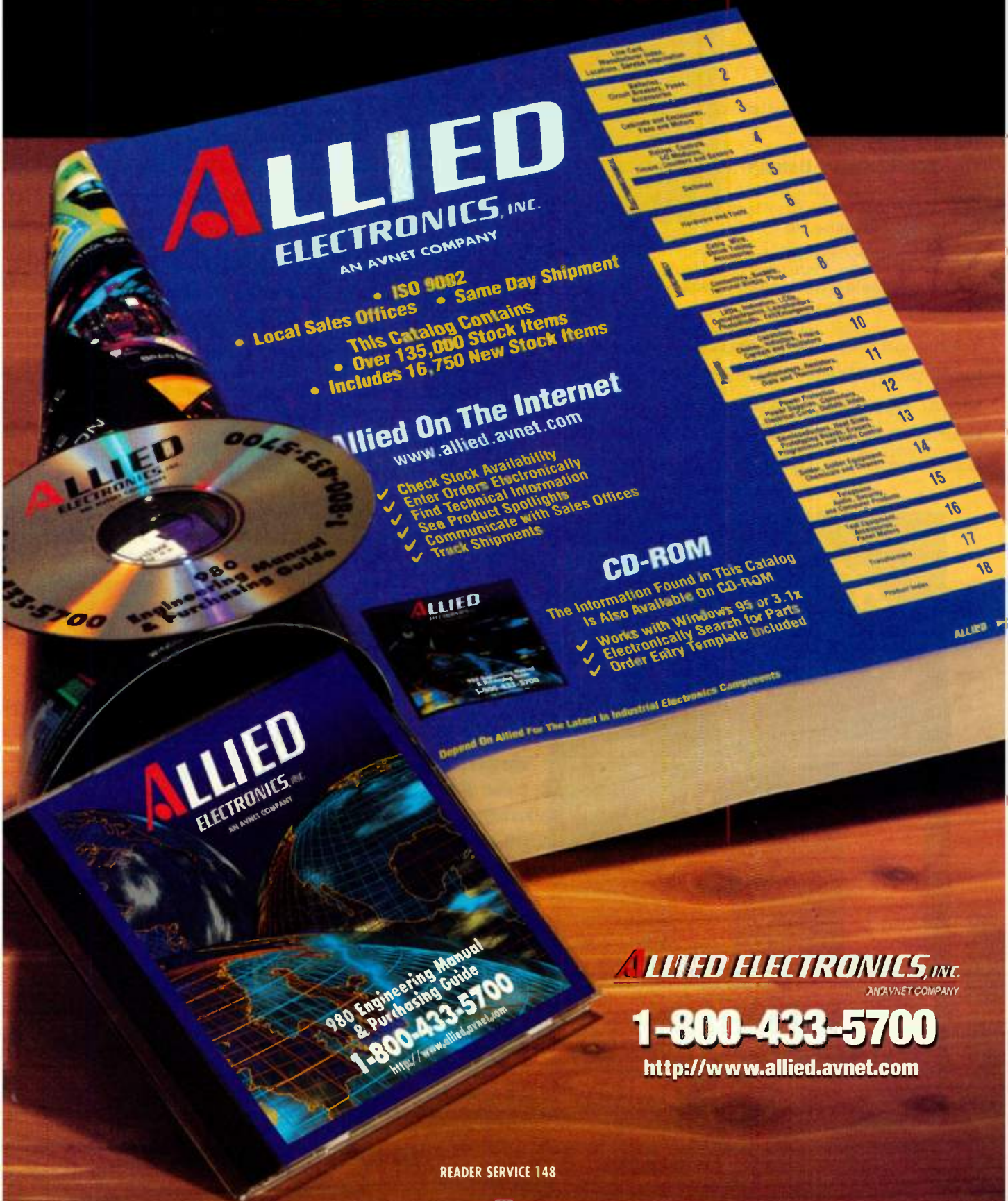
The growing importance of IP and patents makes the job of engineers, and particularly engineering mangers, all the more complex. In the past, engineering managers "only" had to worry about meeting their very aggressive time-to-market schedules and cost budgets, as well as the difficulties of concurrent software/hardware development and test. Now, every time an engineer has a new idea on how to hook two gates together, he or she has to do a patent search to make sure no patent has been infringed.

In my career, I never did rise to the level of engineering management. I wonder—would I rather deal with paper cuts and the smell of ammonia than with lawyers and patent disputes? It's a tough call.

Readers can reach me via e-mail at jeffc@empire.net

Catalog, CD, Internet...

The Choice Is Yours!



ALLIED ELECTRONICS, INC.
AN AVNET COMPANY

1-800-433-5700

http://www.allied.avnet.com

READER SERVICE 148

Conference To Study State Of Telecomm In Bosnia-Herzegovina

A conference to be held later this month in Geneva, Switzerland, will review the state of telecommunications in Bosnia and Herzegovina, and adopt a blueprint for the reconstruction of the network, systems, and facilities. The conference, sponsored by the President of Bosnia and Herzegovina, Mr. Alija Izetbegovic, will also be among the first public gatherings where the new telecommunication law, elaborated under the aegis of the International Telecommunication Union (ITU), will be presented and explained. The ITU will work in close cooperation with the European Bank for Reconstruction and Development (EBRD) and the Office of the High Representative (OHR). Its aim is to inform business and economic partners of the measures taken to provide a clear and transparent telecommunication environment with a view to enlisting their support in the reconstruction efforts.

The draft law is the result of more than one year of consultations and negotiations between the representatives of Bosnia and Herzegovina, which took place at the ITU Headquarters in March, April and May of this year. The law is regarded as one of the first major joint "products" arising from a consensual approach between all parties, and hopes to consolidate the country's longer-term political and economic base through solid telecommunications institutions. For the first time, representatives of the Council of Minister of the State as well as the two entities of Bosnia and Herzegovina—the Federation of Bosnia and Herzegovina and the Republika Srpska—have unanimously agreed on the country's telecommunication legal framework. For more information, go to the ITU's web site at *www.itu.int/newsroom*. RE

Alliance Promotes PXI For Measurement And Automation

More than 40 test, measurement, and industrial companies have banded together to form the PXI Systems Alliance. Its purpose is to promote and maintain the PXI (PCI eXtensions for Instruments) specification. This specification adds instrumentation capabilities to CompactPCI, an industrial computer standard supported by more than 300 companies. National Instruments, Austin, Texas, announced PXI and the PXI specification in September 1997.

The Alliance is composed of compa-

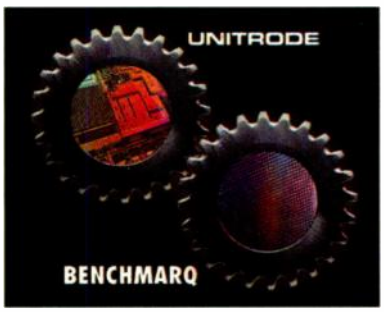
(continued on page 24)

Autumn UNITRODE Highlights

The Linear IC Company Everyone Follows

Issue 5

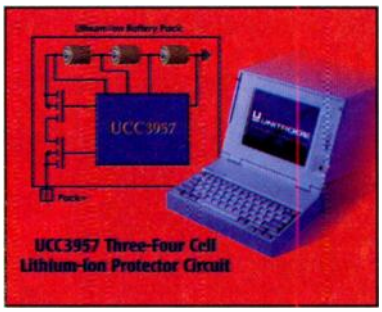
This season's IC highlights from Unitrode help your designs perform with greater efficiency at substantial savings. We'll provide samples and free application information. Give us a call today.



Integrating Our Strengths

Unitrode Corporation and BENCHMARQ Microelectronics, Inc. have merged. This combination is unbeatable! Together, Unitrode and Benchmarq now offer a complete line of IC solutions for portable and standard power management applications, with much more to come. Check our website for more info!

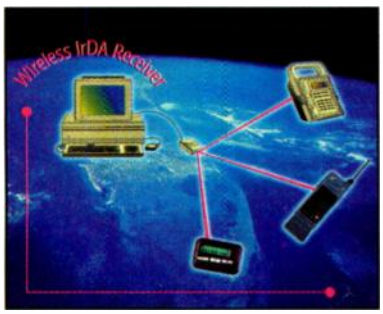
www.unitrode.com **Reader Service 165**



UCC3957

The UCC3957 battery protector provides complete voltage protection and over-current protection for three or four cell lithium-ion battery packs. This device is used in conventional and "smart" battery packs for equipment such as laptop computers and portable instruments.

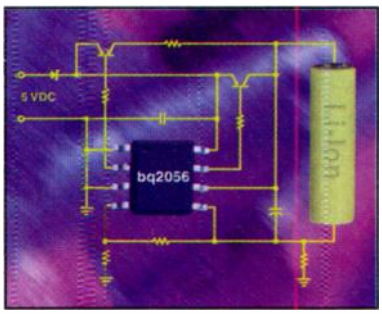
www.unitrode.com/products/portable/ucc3957.htm **Reader Service 166**



UCC5341 and UCC5342

Receiver and transceiver low current devices, these IrDA ICs are used in portable electronics applications. These devices support the analog section of the IrDA 1.0 standard, and have very low current consumption when active, making them excellent when power savings is at a premium.

www.unitrode.com/products/portable/ucc5341.htm
www.unitrode.com/products/portable/ucc5342.htm **Reader Service 167**



bq2056

The bq2056 charge-control IC for single-cell lithium-ion battery packs is ideal for precision low-dropout linear regulator design using a minimum number of components. Its proprietary AutoComp™ technique enables the battery to reach optimal capacity in the shortest time.

www.benchmarq.com/prod/bq2056.html **Reader Service 168**

UCC5638

The UCC5638 SCSI Multimode active terminator provides a smooth transition from single ended to low voltage differential (LVD SCSI). It contains all functions required to terminate, auto detect and switch modes for SPI-2 bus architectures. With the Quad Flat Pack packaging, the UCC5638 offers the smallest footprint for space-constrained boards.

www.unitrode.com/products/interface/ucc5638.htm **Reader Service 169**

UCC3831/38531

Unitrode's UCC3831/38531 family of hub power controllers provides a complete, fully USB-compliant power management solution for self-powered USB hubs. The devices offer four separately regulated 5V port power outlets, each capable of delivering at least 500mA, providing a single chip solution for most hub power applications.

www.unitrode.com/products/linear/ucc3831.htm
www.unitrode.com/products/powsup/ucc38531.htm **Reader Service 170**

UNITRODE

The Linear IC Company Everyone Follows

Tel: 603-429-8610 • http://www.unitrode.com • Fax: 603-424-3460
7 Continental Boulevard, Merrimack, NH 03054

(continued from page 22)
nies from North America, Europe, and Asia. Members share a common commitment to end-user success with open, multivendor PXI systems for applications in test and measurement, industrial automation, data acquisition, and instrumentation. Their primary goal is to improve the effectiveness of Compact-PCI solutions in measurement and automation through use of the PXI specification. The charter of the group is to promote PXI, ensure multivendor interoperability, and maintain the PXI specification. PXI Systems Alliance membership is open to vendors who share the PXI philosophy and objectives, and want to produce and promote solutions compatible with alliance goals.

Membership information is available on the PXI Systems Alliance Web page at *www. pxisa.com.* JD

OVI Approves IEEE 1364 Verilog-AMS Standard Extension

The EDA (Electronic Design Automation) industry organization known as Open Verilog International (OVI), Los Gatos, Calif., has recently announced its approval of the Verilog-AMS (analog and mixed signal) standard. This standard, which serves as the analog/mixed-signal extension to the IEEE 1364 Verilog HDL (hardware description language) standard, will help expand the reach of Verilog to both analog and mixed-signal designers. In addition, it's expected to serve as a key enabling technology for the design of next-generation complex systems and ICs.

The standard, which traces its origin back to work done by OVI's Technical Subcommittee (TSC) for Verilog-A in 1994, is based on fundamental principles of mathematics and physics. As a result, it enables the description of systems composed of mechanical, electromagnetic, and electrical sub-systems. In particular, it allows designers to work within the context of a top-down design methodology for analog and mixed-signal modeling. Here, they can use a single language to model and simulate a mixed system, such as a car's entire brake system with its mechanical, electrical, and digital controls, as well as motors and analog drivers.

Currently a number of companies are either planning to support, or are already using, the standard. These companies include Analogy, Apteq, Cadence, Motorola, National Semiconductor, and Transcendent Design Technology. Efforts are now underway by OVI to pursue IEEE standardization of the Verilog-AMS standard. For more information, or to receive the latest draft of the Verilog-AMS standard, contact OVI at (408) 358-9510; *www.ovi.org.* CA

Edited by Roger Engelke

The Fastest ISP™ CPLDs at 3.5ns. NOW!

Crack the system speed barrier with Lattice's SuperFAST ispLSI 2000E family of In-System Programmable High Density PLDs, the fastest PLDs at any density. With 32 to128 macrocells, user selectable 5.0- or 3.3-V outputs, PCI compliant I/O and space-saving TQFP packaging from 44 to 176 leads, the four devices in this unique family provide an unbeatable combination of industry-leading performance and features.

The first CPLDs to claim the world speed record, the 3.5ns/200MHz ispLSI 2032E and 5ns/165MHz ispLSI 2128E devices also feature clock-to-output times to 2.5ns to support the fastest synchronous I/O requirements. World class Lattice ispJTAG™ in-system programming in 3 seconds or less will help you set new records for fast, low-cost manufacturing.

The SuperFAST ispLSI 2032E and ispLSI 2128E devices—they're available now with performance that's a generation ahead of the competition. But then you'd expect that from Lattice.

Download SuperFAST information from the Lattice website:

www.latticesemi.com

READER SERVICE 109

Lattice® Semiconductor Corporation

The Leader in ISP™ PLDs

WRH

First Commercial OSMs Shift I_2O Momentum Into High Gear

Taking a major step toward true software-driver independence for computer systems, the Intelligent I/O (I_2O) Special Interest Group (SIG) has announced the availability of Operating System Service Modules (OSMs) from Microsoft Corp., Redmond, Wash.; Novell Inc., Provo, Ut.; and SCO, Santa Cruz, Calif.

Hewlett-Packard Co., Palo Alto, Calif.; IBM Corp., Armonk, N.Y.; and Sun Microsystems, Palo Alto, Calif., have also announced their support for the I_2O architecture in future operating-system products.

An OSM is an integral component of the I_2O architecture. It provides the interface between the host OS and the I_2O message layer. It also represents the portion of the driver that forwards host-OS requests to a hardware device module (HDM) for processing. I_2O OSMs now include Microsoft NT 4.0 (storage), Novell NetWare 4.11 (Storage and LAN), and SCO UnixWare 7 (storage, management OSM, and LAN beta).

More On The Way

In addition, HP has announced that it plans to support the I_2O architecture in its 64-bit, HP-UX 11 operating environment in the first quarter of 1999. IBM will support the I_2O specification in the next version of its OS/2 Warp Server in early 1999. And, Sun Microsystems has announced that it will implement the I_2O specification in its Solaris products.

Traditionally, hardware vendors have had to write a specific driver for their card, then get it validated in the OS. With an I_2O OSM, the company writes the top half of the driver as linked to a common interface. If all the hardware vendors write to that standard interface, the OS vendor only has to validate one driver interface, yet, has access to many hardware drivers. Conversely, designers on the hardware side can write one driver, and have access to all of the operating systems that support I_2O.

"For over a year, the major OS vendors have been in process with beta versions of these OSMs, which are available to SIG members on the I_2O SIG web site," says Michael Rex, Intel's marketing manager for I_2O. "That's helped product development, but now that there are commercial I_2O implementations, computer system vendors can shift toward delivering products based on the I_2O architecture specification," says Rex.

Formed in early 1996, the I_2O SIG now boasts more than 135 members. Its basic objective is to provide an I/O device-driver architecture that is independent of both the specific device being controlled and the host operating system. This is achieved by logically separating the portion of the driver responsible for managing the device from the specific implementation details for the OS it serves.

By doing so, the device management portion of the driver becomes portable across multiple operating systems. I_2O also acts to hide the nature of the communication between various mechanisms, providing processor and bus technology independence.

Meanwhile, the I_2O SIG is working on a new version of the overall I_2O specification. Code-named Yellowstone, this release will include three key elements: support for Hot-Plug PCI, support for 64-bit addressing (or greater than 4 Gbytes of memory), and a new messaging model capable of polling.

The new message scheme is expected to enhance performance. The SIG has task forces focusing on each of the three areas, and they're developing a demo for proof of concept. By the end of the year, Rex expects those efforts will be complete. Following that, the documentation will be prepared, and Yellowstone ratified in the first quarter of next year.

While most of the initial market of I_2O is in LAN server and data-storage applications, there's growing interest among specialty and embedded applications. Today, storage and LAN are two very-well-defined classes for I_2O. And, board vendor Cyclone Microsystems Inc., New Haven, Conn., wants to ensure that within the I_2O specification there is a generic class that doesn't have to be classified as LAN or storage.

With that in mind, the company crafted a generic OSM that lets very primitive messages do the work. Cyclone made a proposal to the I_2O steering committee to make that generic class driver a part of the spec. Currently, the committee and the I_2O architects are reviewing the proposal, and "if everyone is favorable to it, we'll approve it," says Rex.

Chip Vendor Participating

For it's part, chip vendor PLX Technology Inc., Sunnyvale, Calif., the only vendor actively participating in the I_2O SIG, focuses on embedded applications. The company recently announced the newest version of its I_2O software development kit (SDK). The SDK allows designers to create industry-standard and private-platform PCI and I_2O designs using the IBM PowerPC 401, Motorola MPC860 PowerQUICC, and other microprocessors. The new SDK version 1.5b leverages advanced programming interface (API) libraries in PLX's new PCI SDK 2.0 software development kit for PCI design.

Software written for PCI 9080 reference design kits requires minimal modifications to add support for new I_2O-compatible chips, like PLX's recently introduced PCI 9054 I/O accelerator and IOP 480 I/O processor.

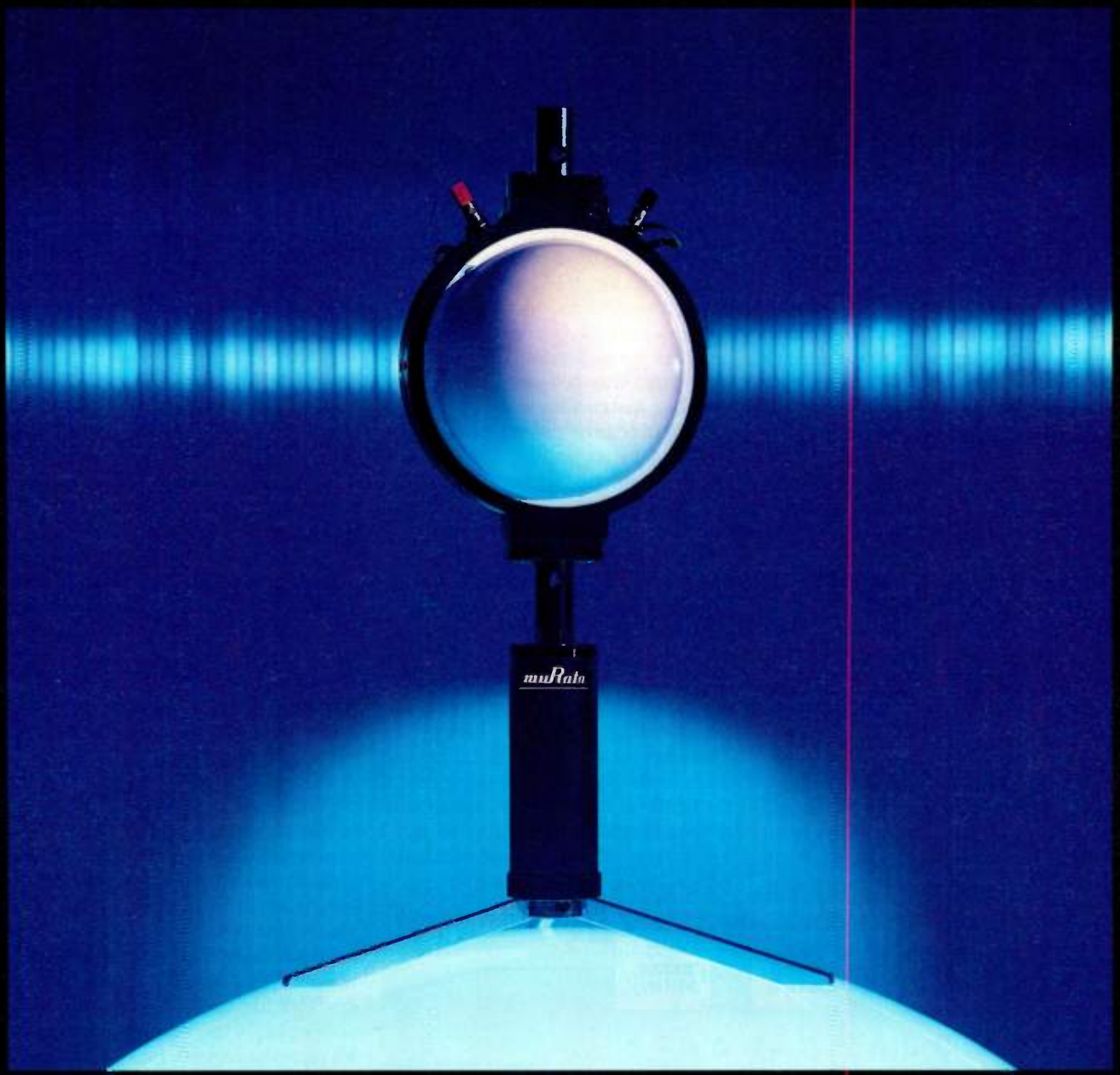
The I_2O SDK 1.5b features the PLX I_2O Manager, which includes all the functions required to implement an I/O processor (IOP) as required by the I_2O version 1.5 specification. These include the I_2O shell message-passing protocol, configuration commands, and a set of general purpose commands. The libraries included in the I_2O Manager may be linked to other control software for the IOP, and do not require an I_2O real-time operating system.

IOP developers only need add the actual device-driver software appropriate to the PCI chips on top of this messaging layer to create the finished IOP. I_2O Manager relieves the developer of the task of creating an I_2O-architecture-based messaging interface.

For more information on I_2O, contact the I_2O SIG, 404 Balboa St., San Francisco, CA 94118; (415) 750-8352; (415) 751-4829 (fax); www.i2osig.org.

Jeff Child

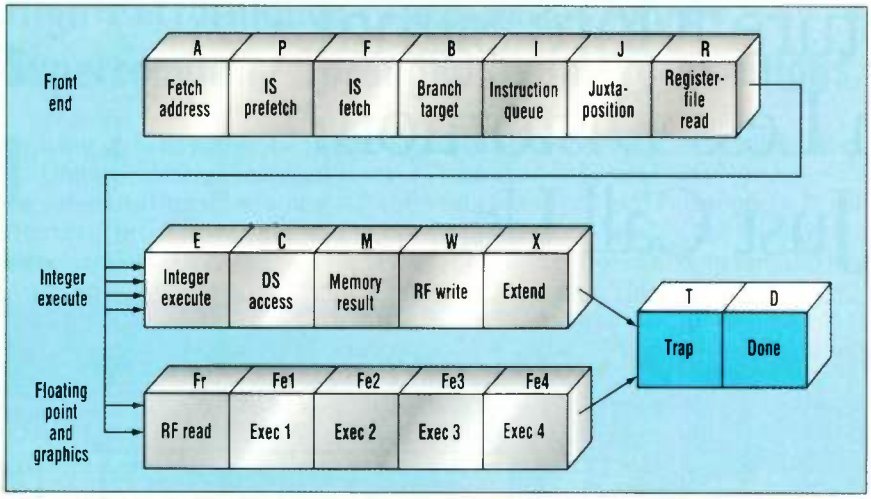
It doesn't matter what it is. What's fascinating is what we made it do.



It projects sound in 360 degrees and operates up to 100KHz. And you may be surprised to learn it's a speaker. We tried something new with piezoelectric ceramic technology and wound up with something new in sound. It's this kind of innovative thinking that makes Murata a sought-after partner in design engineering. We're constantly pushing the envelope to develop the kind of leading-edge technologies that result in breakthrough applications. Like our piezoelectric vibrating gyroscope that's now used in camcorders and car navigation systems. And our multilayer technology that led to chip antennas and chip LC filters for cell phones and paging systems. So if you're starting a new design project and need an innovative partner to help make it work, count on Murata. Call 1-800-831-9172 or visit www.murata.com.

muRata

Innovator in Electronics



2. The pipeline in the UltraSPARC III RISC processor, being developed by Sun Microelectronics, has two major sections. The front end does most of the instruction setup, and the back end performs integer execution and in-parallel, floating-point, or graphics instruction execution.

structions, as well as for floating-point add and multiply. Divide and square-root instructions have longer latencies: 17 to 24 cycles depending on the operation, and whether it's single or double precision. A five-read-port/four-write-port register file supports the floating-point/graphics pipeline.

Like the Alpha processor, the UltraSPARC III will employ a 64-kbyte, level-1 data cache, but it will be four-way set associative rather than two-way. However, in addition to the data cache, the Sun processor includes a 2-kbyte, level-1 prefetch cache and a 2-kbyte, level-1 write-cache, both of which are also four-way set associative. The processor supports an off-chip, L2 direct-mapped cache of from 1 to 8 Mbytes, using a 256-bit-wide data bus to achieve a data-transfer bandwidth of 6.4 Gbytes/s. Internal caches use 64-bit buses to move data, but also operate faster, with data transfer rates as high as 18.4 Gbytes/s (L1 prefetch cache).

The prefetch cache allows concurrent fills and dual reads to occur. It handles eight outstanding software prefetch requests. The cache also manages autonomous hardware stride prefetches and fully coherent operation.

Examining ways to lower cost and improve performance in their mainframe systems, designers at IBM developed a multichip CMOS processor, the G5, to replace the G4 CPU in the S/390 mainframes. The multichip module gives the S/390 faster cycle times; a better clocks-per-instruction ratio; improved reliability, availability, and serviceability; and architectural features that also improve performance. The result is 150 MIPS in a uniprocessor configuration, and 1040 MIPS in a 10-way CPU configuration. Those numbers are about double that achieved with the G4 and previous bipolar implementations.

Based on a 0.25-µm (drawn) CMOS process with up to six levels of metal, and operating from a 1.9-V power supply, the CPU developed for the module packs about 25-million transistors, and consumes about 25 W. Integrated onto a 14.6-by-14.7-mm chip, the processor has been clocked in various laboratory test systems at up to 600 MHz. Initial commercial units, though, are specified for 500-MHz operation.

On the chip is a 256-kbyte, level-1 cache (four-way set associative) that holds instructions, operands, and millicode data. (Millicode is a type of microcode used to implement complex S/390 instructions). The chip uses a 256-byte line size, and the cache is complemented by a 1024-entry, translation look-aside buffer and a 2048-entry branch-target buffer. The chip also includes a 32-kbyte writeable control-store that holds routines for 64 of the most commonly used instructions executed by millicode.

The CPU architecture is a single-issue, in-order execution structure, with a seven-stage pipeline. To deal quickly with interrupts and other operations, a special recovery-register unit (R-unit) on the chip holds a check-pointed copy of the processor's microarchitected state (256 registers, each 32/64 bits long). And, shadow copies of the general-purpose registers, floating-point registers, and certain R-units are distributed throughout the chip's instruction and execution units. So if something goes awry, the processor can quickly recover its state and continue operation.

The on-chip floating-point unit (FPU) supports IBM's traditional S/390 hex floating-point architecture, but now also supports IEEE-754-compliant execution. The FPU includes 121 new opcodes to support extended operations and new capabilities.

As mentioned, the CPU is part of a multichip module that holds up to 12 processor chips (10 active, two as spares); two L2 cache control chips; and up to eight, L2 cache dataflow/array chips. Additional resources on the module include four I/O channel interface chips, each with six ports that connect to the S/390 channel subsystem. Each port can run at 333 Mbytes/s in each direction, and all 24 ports can run simultaneously. Complementing the CPU module are up to four memory cards, each containing four banks. Each card can hold 6 Gbytes of DRAM.

Taking a different approach to system integration, designers at Hewlett-Packard opted to cram as much cache as they could onto one of their PA-RISC processors. Consequently, in a presentation at Hot Chips, they wowed many attendees with the details of the PA-8500, a 64-bit processor with 1.5 Mbytes of level-1 cache. With all the other associated memory support functions for the branch-target cache, tag bits, register files, etc., about 80% of the 140-million transistors on the chip are used by memory-related circuits. The extensive use of memory also helps keep power consumption to an expected 10 to 15 W.

The main caches are divided into a 500-kbyte instruction cache with four-way set associativity, and a 1-Mbyte data cache that is also four-way set associative. Both caches support either 32- or 64-byte line sizes. The I-cache provides four instructions per cycle to the CPU core, while the D-cache allows two accesses per cycle. This way, the CPU can rapidly access the data it needs, reducing latency. The data cache also employs a store queue for faster writes back to the memory, and allows data prefetching so that it can be prestaged for the CPU.

Dave Bursky

ANNOUNCING SLDRAM

LET FREEDOM RING

The people have spoken, and now there's a choice. The industry's first 64Mb SLDRAM samples are available from Micron. So you have a cost-effective, industry-standard alternative to other high-bandwidth solutions. • Since SLDRAM is supported by a 24-member consortium of companies, you can count on high volume from multiple suppliers, with a clear road map to the future. Micron is currently sampling 400 MHz, 2.5V devices in both 4 Meg x 16 and 4 Meg x 18 organizations, with both horizontal and vertical 64-pin configurations. • Call 1.208.368.3900 or visit www.micron.com/mti for more about sampling SLDRAM. Because there's nothing so sweet as the taste of freedom.

MICRON®

w w w . m i c r o n . c o m / m t i

READER SERVICE 119

TECH INSIGHTS

Exploring power-management design issues for advanced microprocessors

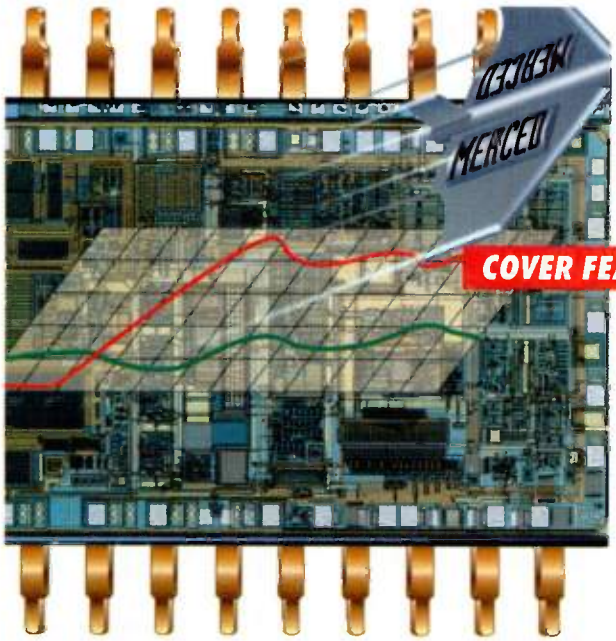
Ripple Regulator Takes Off On Merced's Command

Hysteretic Controller Enables Speedy And Efficient Programmable Voltage-Regulator Modules For The 64-Bit Processor.

Ashok Bindra

As microprocessor design rapidly jumps from 32- to 64-bit architectures, stringent design requirements follow right on its tail. Issues such as the load transient response and the amount of power a processor can dissipate have led to a demand for complex, low-voltage power controllers that push the performance envelope to new heights.

Intel's upcoming 64-bit Merced processor, for instance, requires about 30 A of operating current at lower voltages. This is in stark contrast to the 18 to 20 A needed by current generation 32-bit Pentium IIs and comparable processors. In addition, the power requirements for this type of processor shift rapidly with changes in load. The voltage regulator module (VRM) or dc-dc converter powering such a processor must be able to respond to these demands, while furnishing the multiple voltages needed by the processor's CPU core and I/Os. Needless to say, the new generation power-controllers are expected to consume very little power. They've raised the efficiency bar, but can all these features come at a low cost?



Powering 64-Bit Processors

Key semiconductor manufacturers of power-supply controllers have begun addressing the strict voltage and current requirements of the high performance 64-bit Merced procesor. Texas Instruments Inc. leads the pack with an early announcement of working silicon that powers the Merced and any other foreseeable processor. TI exploited its 1.0-µm LinBiCMOS process to create the TPS5210. A programmable, synchronous-buck-regulator controller, the TPS5210 meets—and even beats—the Merced's power demands.

To comply with Intel's VRM specifications for the 64-bit processor, which is expected to be released sometime next year, the TPS5210 is in production in 28-pin SOICs, as well as in the thermally enhanced optional TSSOP packages Evaluation boards and application notes for the latest controller also are available. Because the new part is highly integrated, TI estimates that the TPS5210-based dc-dc converter solution will cost less than $9.00 (*Fig. 1*).

The goal was to accomplish faster load-current transient response, as well as high conversion efficiency at both lower voltages and power dissipation. TI engineers adopted a synchronous buck ripple regulator topology with a built-in hysteretic controller as opposed to standard voltage or current-mode operation. This clever topology combines the high efficiency of pulse-width regulation with the dynamic regulation capability of series or shunt dissipative regulators. In essence, the hysteretic power controller uses the output ripple as an error to control the output regulation. According to Dale Skelton, system design section manager for TI's power management products, "This creates fast transient response by allowing the switching frequency to vary in proportion to load transients."

For this type of converter, typical operating frequency ranges from 120 to 250 kHz. "The input and output voltage values, the output filter components, and the the hysteresis win-

dow set the operating frequency," explains Skelton. The device provides a user-selectable hysteresis window, which is set by two external resistors around the reference voltage (*Fig. 2*). The synchronous-buck-regulator controller compares the output voltage to the programmed window, turning the high-side MOSFET on and off to maintain the output voltage within the window. The maximum hysteresis setting is 60 mV. Propagation delay from the comparator inputs to the output drivers is less than 250 ns. As a result, according to Skelton, "the regulation is instantaneous."

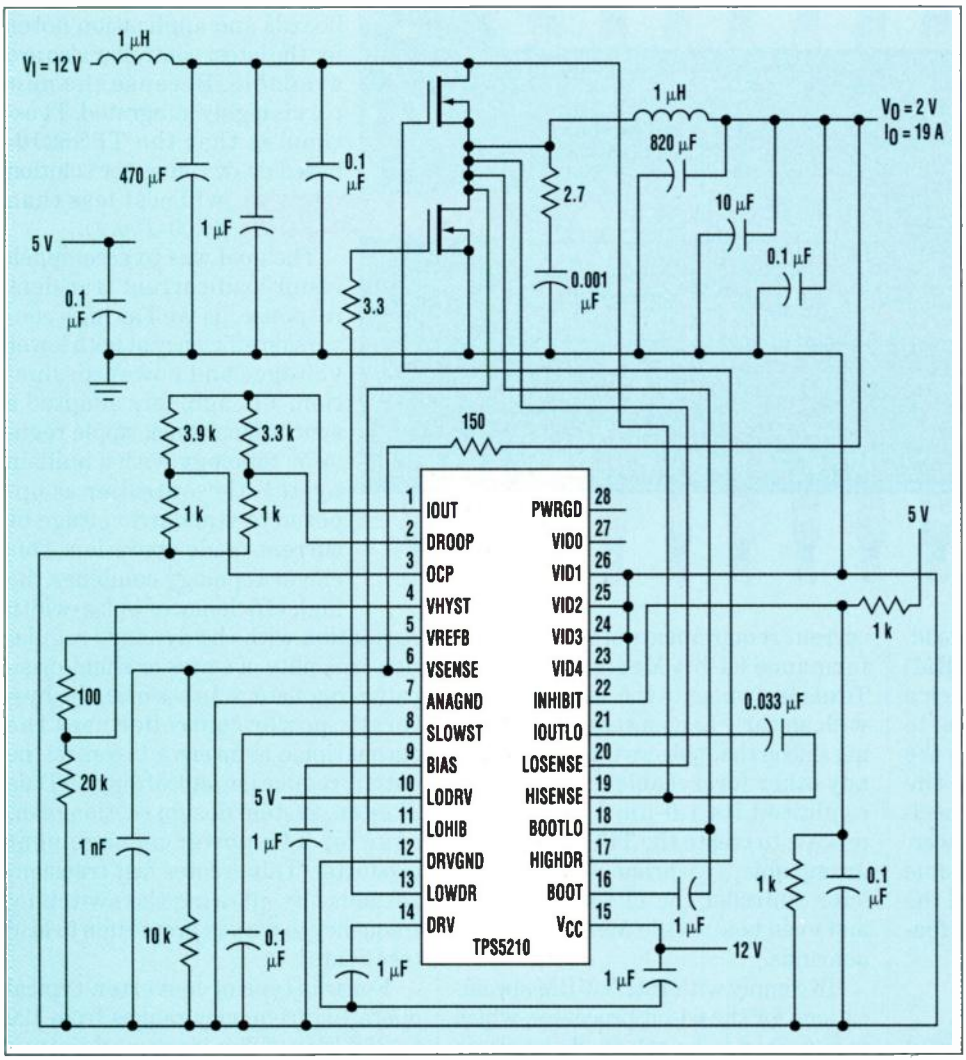
"The user-selectable hysteretic controller and the droop compensation in the TPS5210 dramatically reduce the overshoot and undershoot caused by the load transients," notes Les Hodson, system engineering manager for TI's power management products. "Consequently," he adds, "despite high current transient rates, the controller can recover to the original output value in about 2 µs." Internal tests indicate that, at a 2.0-V output, the TPS5210 power controller can meet step load increases from 0.1 to 20.4 A in 1.0 µs (*Fig. 3*). With the droop compensation circuit, V_{OUT} transient regulation does not fall outside of a 2% limit. The tests show that the transient peak-to-peak ripple is 111 mV for a 2.0-V output. Recovering to full value, however, takes about 2.2 µs.

Higher Efficiency

According to TI, the synchronous-buck regulator controller design achieves 90% or better efficiency over a wide range of load currents. At a low load, however, the efficiency drops below 80%. The total power dissipation for the device is only 120 mW.

"Using the optimized LinBiCMOS process keeps the power dissipation low, while permitting higher functionality on-chip," states Hodson. "Plus," he adds, "the output accuracy is within ±1% over the full operating temperature range." The controller even maintains the specified accuracy at output voltages as low as 1.3 , according to TI. This accuracy is maintained over the full operating temperature range, says TI.

Other key features of this highly integrated device include active deadtime control, noise immunity circuitry, 2-A synchronous-buck drivers, an internal-drive regulator, and programmable soft-start capability. The integrated controller chip also has lossless current sensing, adjustable current limiting, overvoltage protection, V_{CC} undervoltage lockout, an inhibit comparator, user adjustable droop compensation, 30 V rated bootstrapped high-side driver and a "power-good" output circuit (*Fig. 4*).



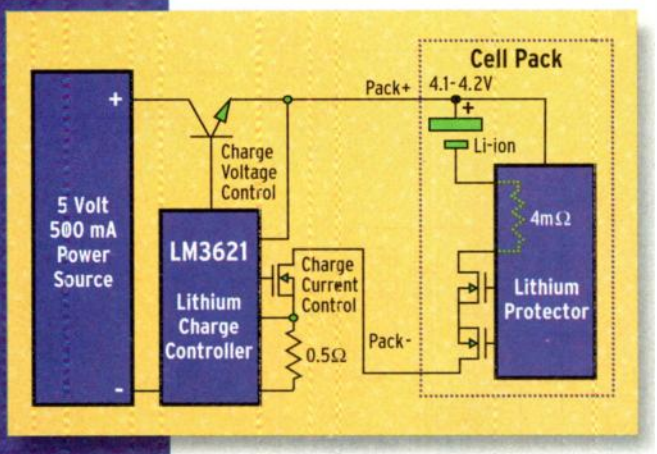
1. This typical design schematic uses the TI TPS5210 controller for a 2-V output at 19 A. The supply voltage for this circuit is 12 V. For such a dc-dc converter, TI estimates the total bill for materials can be under $9.00.

The deadtime control prevents shoot-through current from flowing through the main power FETs during switching transitions. To do this, it actively controls the turn-on times of the MOSFET drivers. "This period is less than 100 ns with the TPS5210," says Hodson. "Conventional designs offer twice as much. The hysteretic power controller provides improved noise immunity to make the unit less sensitive to layouts on pc boards," states Hodson. "With conventional converters, this aspect of dc-dc converter design is very critical, as it affects noise pickup and generation to degrade the end performance of the design." Nevertheless, TI recommends proper layout for the TPS5210 and provides guidelines for laying it out in a dc-dc converter design.

The on-chip, 2-A low- and high-side drivers are designed to drive low-on-resistance n-channel MOSFETs. Internally, they're connected to an 8-V gate-voltage regulator. The

YOU'LL GET A CHARGE OUT OF THIS.

±0.5% ACCURACY CVCC Li+ CHARGE CONTROLLER



National's New Lithium-ion Charge Controller—the high accuracy you need to boost your wireless designs.

- *±0.5% output voltage accuracy for maximum protection without degradation of cell capacity*
- *Pin selectable for coke or graphite chemistries (4.1V or 4.2V)*
- *Adjustable charge current control*
- *Numerous fault-detection flags for safe and reliable cell charges*
- *Five charge modes for 100% charge under all conditions*
- *LED drivers for visual indication of charge status*
- *High-gain constant voltage, constant current (CVCC) control loop architecture*

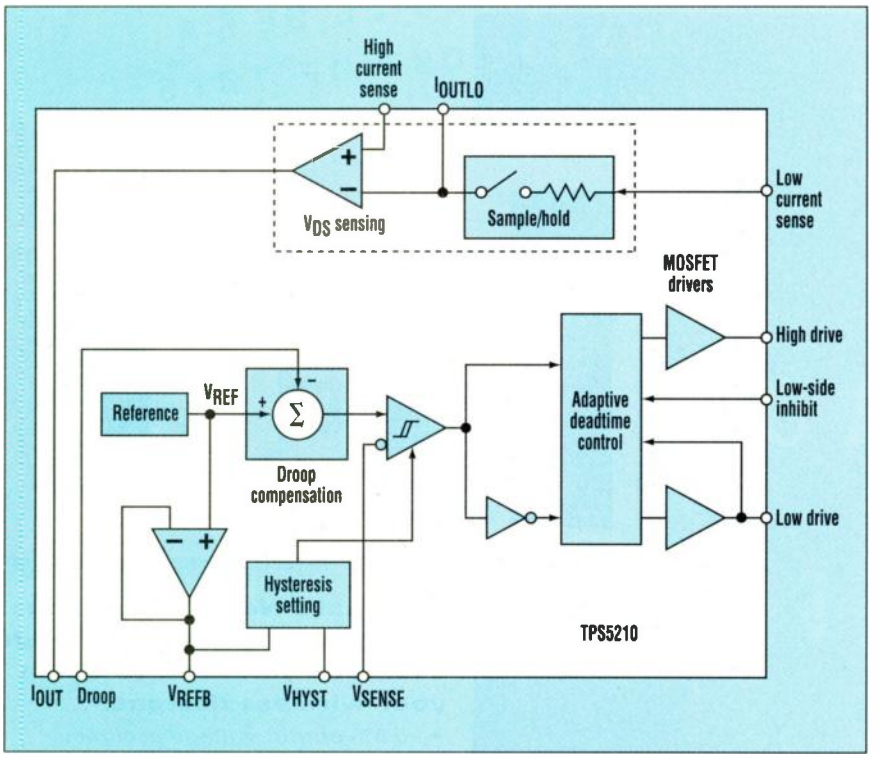
National's LM3621 is quite simply the most highly integrated, full-function Lithium-ion charger IC you can get. Regulation accuracy of ±0.5%—without external precision resistors—increases the cell's rated capacity. Adding a battery-performance edge to a wide range of Lithium-ion-powered portable applications, like cellular and cordless phones, pagers, PDAs, palm-top PCs, camcorders, digital cameras, and medical and scientific instruments.

So get National's new Lithium-ion battery charge controller. And create smaller, more effective Lithium-ion based designs.

For more information:
www.national.com/see/LM3621
1-800-272-9959

National Semiconductor

WHAT CAN WE BUILD FOR YOU?™



2. The ripple regulator utilizes a hysteretic controller to accomplish ultra-fast load-current transient response, as well as over 90% efficiency over a wide output-current range.

high-side driver can be configured either as a ground-referenced or floating bootstrap driver. Likewise, the output drivers incorporate overcurrent shutdown and crossover protection to eliminate destructive faults in the output FETs.

A softstart current source, made proportional to the reference voltage, minimizes variations in the softstart timing when changes are made to the output voltage. It controls the rate at which the output powers up. A built-in overvoltage circuit disables the output drivers if the output voltage rises above the 15% of the nominal value. The latch remains set until the V_{cc} goes below the undervoltage lockout value. A 3–µs deglitch timer is included for noise immunity. Likewise, the overcurrent protection circuit monitors the current through the high-side FET. As a result, it also protects the high-side FET from short circuits. The power-good circuit monitors for an undervoltage condition.When the output drops below 7% of the nominal output voltage, the power good pin is pulled low.

While the TTL-compatible inhibit pin enables the controller, it also can dominate power sequencing. To do this, it just locks out controller operation until the system logic supply exceeds the input threshold voltage of the inhibit circuit. Consequently, the inhibit and undervoltage lockout circuits ensure that the system supply voltages (12.0, 5.0, or 3.3 V) are within operating limits prior to controller operation.

Programmable Output

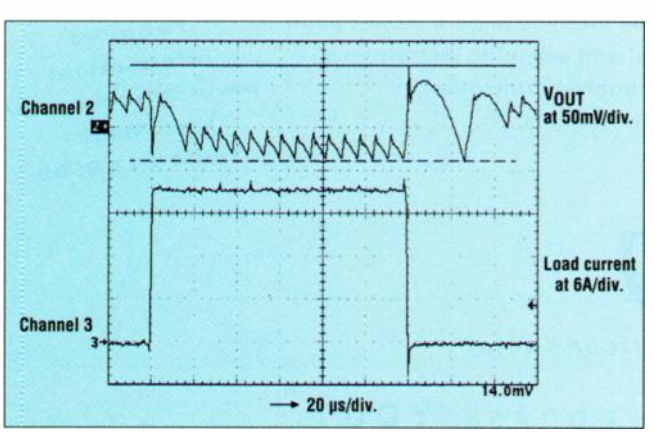
An internal, 5-bit digital-to-analog converter (DAC) supplies a programmable output voltage in accordance to Intel's 5-bit voltage-identification (VID) codes. The 5 VID pins are inputs to this network. Also, the TTL-compatible inputs are internally pulled upto 5 V. The programmable output-voltage range is 1.3 to 3.5 V. While the step increments between 1.3 and 2.1 V are 50 mV, the increments between 2.1 and 3.3 V are in steps of 100 mV. The output voltage is within ±1.0% of the nominal setting over the junction temperature range of 0 to +125 °C.

The input supply voltage range for the synchronous-buck-regulator controller is 11.4 to 13.0 V. The typical supply current for the controller unit is rated at 3 mA.

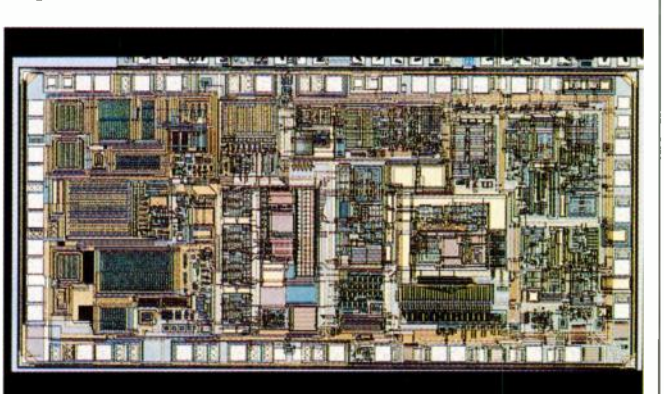
Price And Availability

The TPS5210 is available in 28-pin SOICs and TSSOPs from TI and its authorized distributors. In quantities of 10,000, the hysteretic power controller is priced at $2.25 each. Starting now, designers can also obtain a TPS5210 evaluation module.

Texas Instruments Inc., Semiconductor Group, SC98075, P.O. Box 172228, Denver, CO 80217; (800) 477-8924 ext. 4500; www.ti.com. **CIRCLE 519**



3. This load-transient waveform shows that the TPS5210 can respond to a load step of 0.1 to 20.4 A in less than 1 µs.

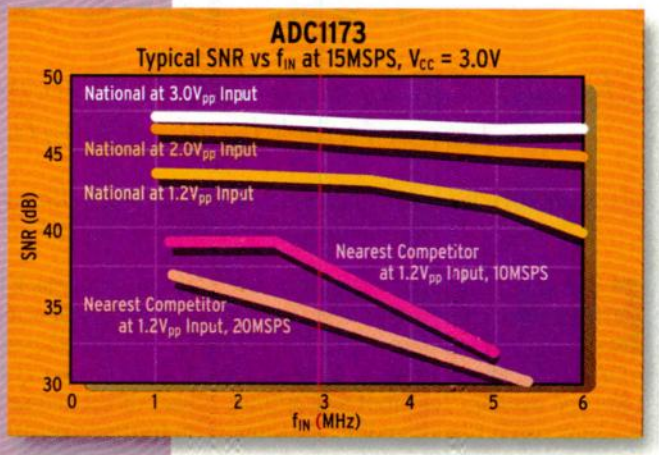


4. The higher on-chip functionality of TI's TPS5210 hysteretic controller can be achieved at low power dissipation using the semiconductor supplier's 1.0-µm LinBiCMOS process.

NEW

LOWEST POWER IN THE SMALLEST PACKAGES.

8-BIT 15MSPS 3V ADC @ 40mW



National's high-speed ADC1173 A/D Converter. Small TSSOP package. Superior dynamic performance.

- *Low power: 3V ±10%, 40mW (max)*
- *TSSOP: smallest package available*
- *46dB SNR @ Nyquist input signal*
- *5V ADC1175 @ 55mW, 20MSPS also available*
- *National's WaveVision™ evaluation board with Windows®-based software*

National's ADC1173 Analog–to–Digital Converter is specifically built for portable imaging and video. Available in a space-saving TSSOP package, our 3V A/D converter consumes less power while providing the industry's best performance. And converting high-speed analog signals into 8-bit digital words at 15MSPS while using only 40mW of power is no small feat. That's why National's ADC1173 is perfect for digital cameras and camcorders, not to mention consumer and PC video. Basically, it's all the performance you can carry.

For more information www.national.com/see/ADC1173 1-800-272-9959

National Semiconductor

WHAT CAN WE BUILD FOR YOU?™

Solving The Year 2000 Real-Time Clock Dilemma

Failure Of Any Part Of A System To Provide, Recognize, Or Process Dates Into The Next Century Can Cause Catastrophes.

JIM LOTT, Dallas Semiconductor Corp., 4401 S. Beltwood Pkwy., Dallas, TX 75244; (972) 371-4000; fax (972) 371-4370; e-mail: jim.lott@dalsemi.com.

Ever since the development of the electronic computer, we have shot up the development curve. Instead of a single, large computer tied to a teletype machine for input and output, we now use interdependent systems, connected over networks, capable of sending, receiving, and processing data from around the world. In essence, the mainframe computer serves as the brain for these complex networks, with PCs acting as gateways between the mainframe and the embedded systems generating data. While microprocessors lie at the heart of the computers that handle most of the communications and control functions, microcontrollers dominate the embedded applications.

Open And Closed Systems

Microprocessor-driven computers fall into the category of open systems, while microcontrollers pervade the low-end, closed systems. An open system is loosely defined as a system that can be programmed by the end user, with full access to the hardware. The best example of an open system is the personal computer. The supplier can't control the compliance of applications developed by the end user. However, the liability of the supplier is greatly diminished when it provides a fully year-2000-compliant platform along with the hardware specifications and a year-2000 (Y2K) impact statement.

In fact, the open PC-AT architecture has become a major force in the embedded-systems arena. PC motherboards are used in applications ranging from ATM machines to monitoring and control systems in electric power plants. Systems range in size from the ruggedized rack-mount, highly visible industrial chassis to the single-board computers in small black boxes. The flexibility of open systems makes them attractive for embedded-systems applications.

The closed system denies the end user direct access to the hardware. The manufacturer installs the operating system (OS) or hardware interface, and end-user applications can only access the underlying hardware through the OS. The system is supplied with the OS interface specifications only. Information covering direct access to the hardware is not provided.

Y2K Failure Points

All of the layers of a computer system must process date-related information before, during, and after the century date change. If any part of a system fails to provide, recognize, or process dates into the next century, complete system failure may occur.

When viewed from a data-processing perspective, applications programs occupy the top level of the system hierarchy. While the OS lies between the program and the hardware.

The applications program handles the manual and automatic database entries, and manipulates the data. Date entry should require a four-digit year with valid date checking. Invalid dates such as February 30, 1999, must not be allowed. If the two-digit-year method is used, the application program should use a windowing technique to expand the year to four-digits prior to entry into a database. Database sorts will fail if it is not compliant. An applications program requiring the current date will either access the system clock through the OS or bypass the OS and go directly to the hardware clock.

Most OSs will maintain a system clock. The OS, of course, gets the time for the system clock from the Real-Time Clock (RTC). Some OSs do not maintain a system clock, and depend on direct access to the RTC for the date and time information.

Some closed systems do not have a true OS. The applications program handles all of the OS functions. This type of program consists of a compiled, higher-level language intermixed with assembly language. The assembly language routines take the place of the compiler run-time routines that make OS calls to access the hardware.

The Software Clock

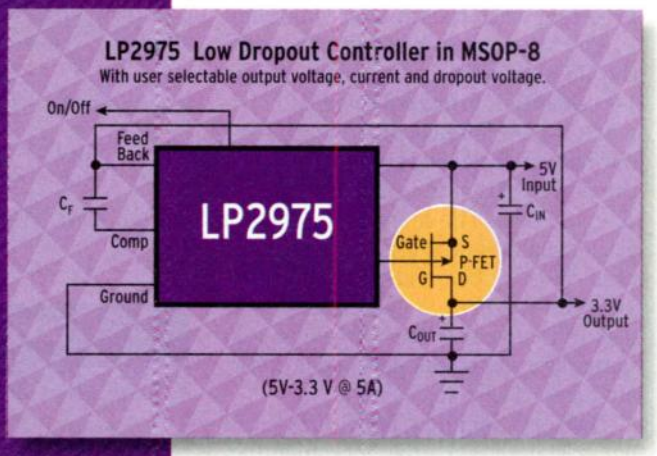
The system clock maintained by the OS is actually a software clock. Software clocks exist in a umber of systems, even those with a hardware RTC. The software clock is synchronized with a

TABLE 1: SIMPLE CLOCK ARCHITECTURE

Y2K Capable	Y2K Compliant
Seconds	Seconds
Minutes	Minutes
Hours	Hours
Day of week	Day of week
Date of month	Date of month
Month	Month
Year	Year
	Century

>>1A ULTRA-LOW DROP-OUT CONTROLLER

THE FLEXIBILITY YOU NEED IN POWER CONTROL.



National's Ultra-low Drop-out (LDO) Controller. Output current. Power dissipation. Drop-out voltage. It's your call.

- *Customer-selectable high current (>>1A) ultra LDO (~.10V) controller*
- *Design flexibility in output current selected by choice of P-FET*
- *Only 5 external components required when compared to N-FET design*
- *Low operating current (180µA typical @ V_{IN} = 5V)*
- *Onboard current sense amplifier*
- *Mini SO-8 package*  *(actual size)*

National's LP2975 LDO Controller was designed to be flexible. By simply choosing a different external P-FET, it can be an ultra low drop-out regulator, a high-current LDO, or both. Add the fact that it comes in 12.0V, 5.0V and 3.3V—with other voltages available by selecting two external resistors—you can begin to see how flexible our controller really is. Now, you get to decide on output current, power dissipation and drop-out voltage. And considering our LP2975 and external P-FET circuitry combinations are usually smaller and cost less than other comparable LDO controllers, you'll have even more flexibility in your next modem, PC, mobile phone, pager or PDA design. Perfect for any application that requires input voltage to drop very low without losing system operation, and where regulator power dissipation must be minimized.

For more information: www.national.com/see/LP2975 1-800-272-9959

National Semiconductor

WHAT CAN WE BUILD FOR YOU?™

time tick derived from a crystal oscillator, and provides a periodic interrupt to the processor. It's usually maintained by the OS in the form of a binary counter, which is incremented by the processor with each time-tick interrupt.

The system clock usually provides the OS higher time resolution than the 1-s resolution provided by most hardware RTCs. The resolution appears normally in fractional seconds based on the period of the time-tick interrupt of the processor. The count in the system clock usually represents the passage of time since the beginning of a reference year. The reference year, or epoch, is usually the year that a particular system or OS was developed, and is different for each system.

Battery-backed CMOS RTCs did not exist in the early days of computing. The current time was entered manually every time the system was powered-up. Modern systems have a battery-backed RTC built-in to remove the requirement for manual time entry.

The current time, whether entered manually or read from the RTC when the system is powered up, has to be converted to the correct format needed to initialize the system clock. The conversion process involves subtracting the epoch from the current year. The remainder is the elapsed time since the epoch that needs to be converted to seconds. The elapsed time is used to initialize the software clock, which will count from that value at the period of the time tick.

A common source of error with the system clock is the failure to service the time-tick interrupt every time it occurs. The operating system will normally service interrupts from multiple sources as part of its housekeeping functions. Critical service routines will leave the interrupts disabled until they are finished. If the interrupt cannot be serviced fast enough, two or more time-tick interrupts can occur while the interrupts are disabled. Only one of the time-tick interrupts can be serviced under these conditions. All critical interrupt-service routines that can not be interrupted must complete their service within one time tick.

If the system clock is in a format that is not readable by humans, problems arise for the OS, and in some cases, applications programs. Date and time entry to the system is in a human-friendly format, as is the date and time output. There are three conversion routines that can be a source of errors. The routines that convert data from the RTC format to the system format, humanly readable format to system format, and system format to humanly readable have to be written and tested for correct date conversion before, during, and after the century date change.

TABLE 2A: Y2K CAPABLE REAL-TIME CLOCK

DS1643: Y2K-Capable Real-Time Clock

Address	Data B7	B6	B5	B4	B3	B2	B1	B0	Function
1FFF									Year 00-99
1FFE	X	X	X						Month 01-12
1FFD	X	X							Date 01-31
1FFC	X	FT		X	X	X			Day 1-7
1FFB	X	X							Hour 00-23
1FFA	X								Minutes 00-59
1FF9	$\overline{OSC}$								Seconds 00-59
1FF8	W	R							Control

TABLE 2B: Y2K COMPLIANT REAL-TIME CLOCK

DS1743: Y2K-Compliant Real-Time Clock

Address	Data B7	B6	B5	B4	B3	B2	B1	B0	Function
1FFF									Year 00-99
1FFE	X	X	X						Month 01-12
1FFD	X	X							Date 01-31
1FFC	BF	FT		X	X	X			Day 1-7
1FFB	X	X							Hour 00-23
1FFA	X								Minutes 00-59
1FF9	$\overline{OSC}$								Seconds 00-59
1FF8	W	R				Century tens		Century units	Century 19-20

Leaping With The RTC

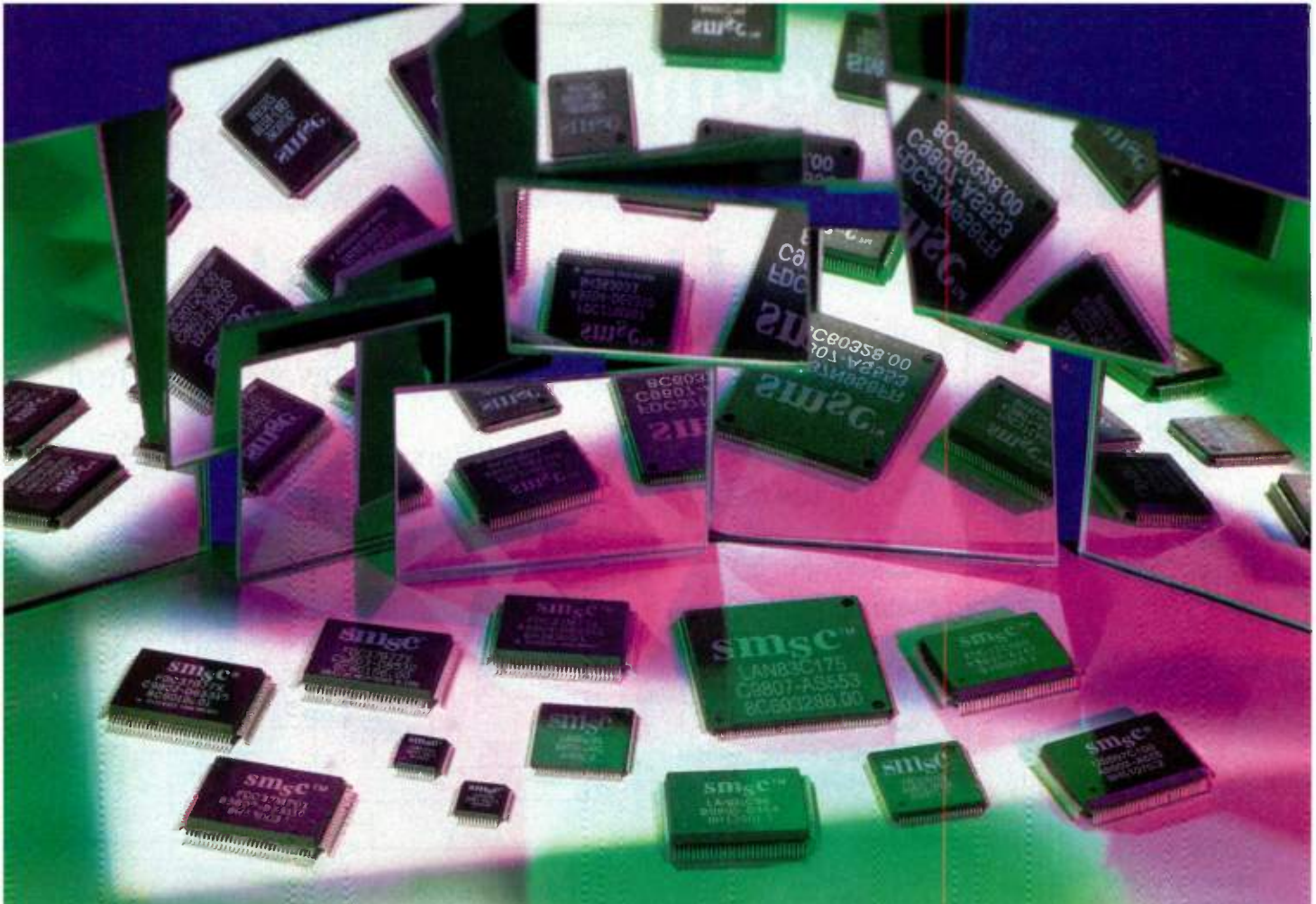
The typical RTC has all of the counting circuitry needed to provide seconds, minutes, hours, days of the week, dates of the month, months, and two-digit years. Only two of the clock registers will be examined here. The day-of-the-week counter has a counting range of 1 to 7. The RTC does not have enough processing power to calculate the day of the week from the information entered into the date-of-the-month, month, and year counters. The day of the week has to be calculated externally, and entered into the RTC when the other registers are loaded. The two-digit year counter has a counting range of 00 to 99; it will count from 00 to 99, then roll over to 00.

Basically, RTCs fall into two categories: Y2K capable and Y2K compliant. The limitation of the Y2K-capable RTC is that it only has a two-digit year counter. It will provide the correct time of day, date of the month, month, and two-digit year with proper leap-year compensation up to 2099. Software intervention is required to determine if the first two fields are 1 and 9 or 2 and 0.

Close examination of the leap-year rules shows that using the rule of four is all you need to provide correct compensation to 2099. The leap-year rules, as shown below, are that every year evenly divisible by four is a leap year, except if the year is evenly divisible by 100—unless it is also evenly divisible by 400, in which case it is a leap year. The year 2000 is evenly divisible by four and 400, which makes it a leap year. The years 1900 and 2100 are evenly divisible by four and 100, which prevents them from being leap years.

Leap-Year Calculations:

```
leapyear = NO;
if((year mod 400) == 0)
  leapyear = YES;
else
```



From every angle it's easy to see, we're more than a PC I/O Company.

As an American semiconductor component manufacturer for 27 years, Standard Microsystems Corporation has established the familiar image of a quality supplier of PC I/O solutions. It is a picture we are proud to project. But it's time to take a closer look. Today, we are so much more. Our new corporate symbol reflects a new SMSC — a company that casts its expertise far beyond the Personal Computer, across all high technology digital and analog integrated circuit disciplines. Our dramatically expanded breadth of product brings tangible value to every customer.

OEM developers are enjoying increased choice and access to a wider diversity of solutions, all with the cost, ease and convenience advantages of a proven single-source supplier. Distributors are offering a broader line card, expanding their ability to deliver. SMSC is now bigger, broader and more diversified than we've ever been before. So, call 516-443-SEMI today, and view us from a whole new perspective. You, too, will soon agree; we're more than a PC I/O company.

smsc
STANDARD
MICROSYSTEMS
CORPORATION

More to Build From.

READER SERVICE 131

Apex Microtechnology

PWM Amplifiers • Power Amplifiers • DC/DC Converters

8th Edition Data Book

Here's your Power Linear and PWM Amplifier applications text book. Now available on CD-ROM. The new 8th edition *Apex Power Integrated Circuits* data book contains:

- 24 Application Notes
- 75 Power Linear product data sheets
- 11 PWM Amplifier product data sheets

Request your free copy today!

On the web:
www.apexmicrotech.com

By E-mail:
prodlit@apexmicrotech.com

By phone:
1-800-862-1021

Australia, New Zealand (08) 8277 3288
Belgium/Luxembourg (323) 458 3033
Canada (613) 828 6881
Daehan Minkuk (02) 745 2761
Danmark 70 10 48 88
Deutschland (089) 614-503-10
España (1) 530 4121
France (01) 33-1-46878336
Hong Kong 2389 0800
India 22 413 7096
Israel 972 3 9274747
Italia (02) 6640-0153
Nederland (10) 288 2500
Nippon (3) 3244-3793
Norge (63) 898 900
Österreich (1) 203-79010
Peoples Rep. of China 852-233-48188
Rep. of South Africa (021) 23 4943
Singapore 842 5840
Sverige (8) 795 9650
Taiwan-Rep. of China (02) 696 2700
United Kingdom (1438) 364194

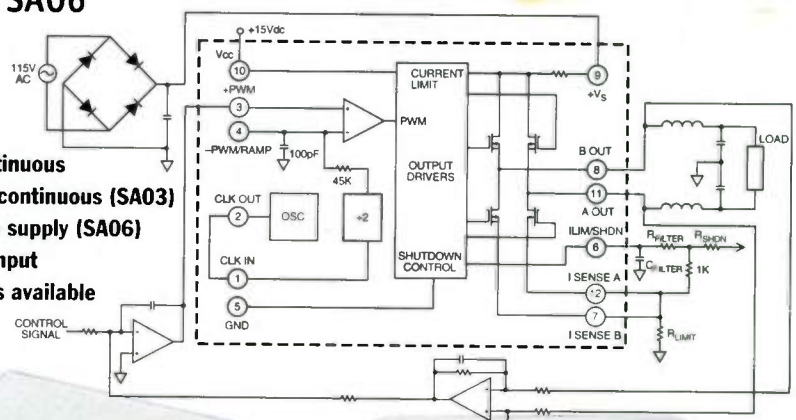
Hand Tools or

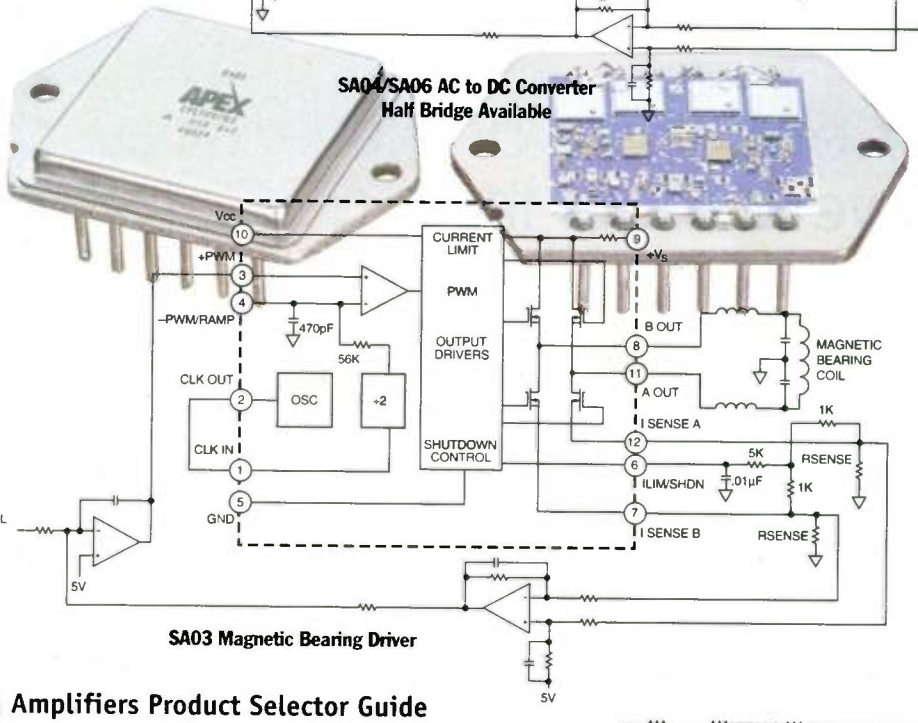
New Computer Aided Power Design Tool,

High Power Delivery PWM Amplifiers: SA03/SA04/SA06

Features

- **Up to 5000W continuous**
- **Up to 30A output continuous (SA03)**
- **Up to 500V bridge supply (SA06)**
- **Analog or digital input**
- **Half bridge models available**



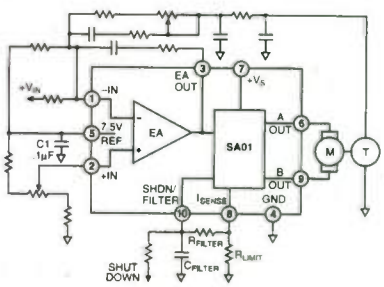


SA04/SA06 AC to DC Converter Half Bridge Available

SA03 Magnetic Bearing Driver

PWM Amplifiers Product Selector Guide

Model	Efficiency	I_{OUT} Cont.	Supply	Switching Frequency	Power Delivery	Full/Half Bridge
SA01	97%	20A	16V-100V	42kHz	2000W	Full
SA02	94%	10A	16V-80V	250kHz	800W	Full
SA03	97%	30A	16V-100V	22kHz	3000W	Full
SA04	97%	20A	16V-200V	22kHz	4000W	Full
SA06	97%	10A	16V-500V	22kHz	5000W	Full
SA07	94%	5A	5V-40V	500kHz	200W	Full
SA13	97%	30A	16V-100V	22kHz	3000W	Half
SA14	97%	20A	16V-200V	22kHz	4000W	Half
SA16	97%	10A	16V-500V	22kHz	5000W	Half
SA50	97%	5A	up to 80V	45kHz	400W	Full
SA51	97%	5A	up to 80V	external set	400W	Full



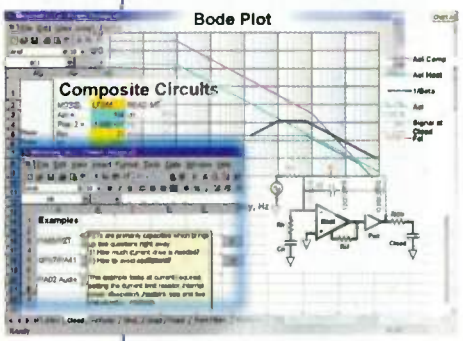
Motor Driver with Tach Feedback

Power & PWM Amplifiers

Download our Power Design Tool and design the easy way!

Power Tools?

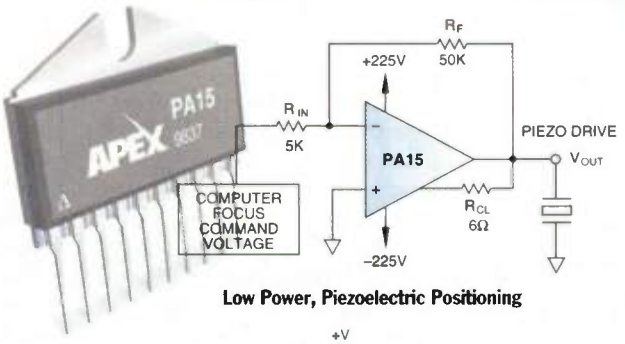
New PWM Amplifiers, New Power Amplifiers



New High Voltage Power Op Amp in Power SIP: PA15

Features

- 450 Supply (±225V)
- 3.8mA MAX Standby current
- 200mA Output current
- 1.0" L x .25" W Footprint
- Programmable current limit

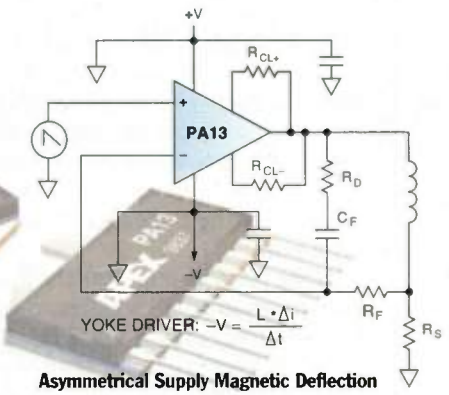


Low Power, Piezoelectric Positioning

New High Power Power Op Amp in Power SIP: PA13

Features

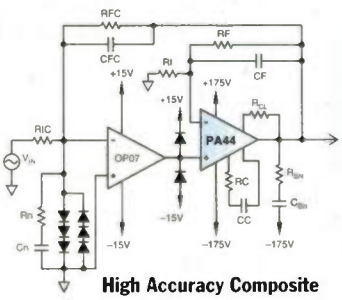
- 10A output PEAK
- ±10V to ±45V supply
- 135W internal power dissipation
- 1.22" L x .25" W Footprint



Asymmetrical Supply Magnetic Deflection

High Voltage Amplifiers Product Selector Guide

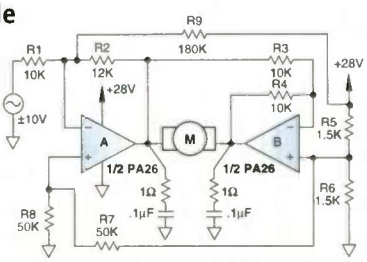
Model	Supply	I_{OUT} Peak	$I_{STANDBY}$	Slew Rate	Package
PA08	30V-300V	200mA	8.5mA	30V/µs	TO-3
PA15	100V-450V	300mA	2mA	20V/µs	PowerSIP
PA41	100V-350V	120mA	2mA	40V/µs	TO-3
PA42	100V-350V	120mA	2mA	40V/µs	SIP
PA44	100V-350V	120mA	2mA	40V/µs	PSOP
PA85	30V-450V	350mA	25mA	1000V/µs	TO-3
PA88	30V-450V	200mA	2mA	30V/µs	TO-3
PA89	150V-1200V	100mA	6mA	16V/µs	PowerDip



High Accuracy Composite

High Current Amplifiers Product Selector Guide

Model	Supply	I_{OUT} Peak	Slew Rate	Power Dissipation	Package
PA03	30V-150V	30A	8V/µs	500W	PowerDip
PA05	30V-100V	30A	100V/µs	250W	PowerDip
PA04	30V-200V	20A	50V/µs	200W	PowerDip
PA10	20V-90V	5A	3V/µs	67W	TO-3
PA12	20V-90V	10A	4/µs	125W	TO-3
PA26	5V-40V	2.5A x 2	1.2V/µs	36W	SIP
PA45	30V-150V	5A	27V/µs	85W	TO-3
PA46	30V-150V	5A	27V/µs	85W	PowerSIP



Bidirectional Small Motor Drive

READER SERVICE 140

New Computer Aided Power Design Tool

Apex's new computer aided Power Design Tool is a self-documented spreadsheet that automates the tedious calculations associated with:

- stability analysis
- internal power dissipation
- current limit
- PWM filter design

This spreadsheet also includes examples which can be used as tutorials on power op amp design. This design tool is **free** and can be downloaded from the Apex web site at **www.apexmicrotech.com**. Upon execution it is suitable for Excel 5.0 through Excel 97.

Efficient Hybrid and Monolithic Designs

With more than 85 models of high power, high voltage and PWM amplifiers, Apex Microtechnology has the off-the-shelf solutions to help trim your design time. You'll work smarter, faster. You'll reduce your circuit's overall size and weight, plus reduce procurement time and costs. Many Apex power and PWM amplifiers have evaluation kits available to provide the hardware and PC boards to get our amplifiers wired into your circuits *fast!* All Apex amplifiers are available for purchase in single unit quantities.

APEX MICROTECHNOLOGY

5980 N. Shannon Road
Tucson, Arizona 85741-5230

www.apexmicrotech.com

Power-Conversion Chip Cuts Energy Wastage In Off-Line Switchers

High-Voltage Controller Enables Energy-Efficient, Economical Alternatives To AC Wall Adapters And Standby Power Supplies.

Ashok Bindra

While the efficiencies of power-conversion chips and power sources continue to improve, energy wastage in stand-by mode remains astonishingly high. For example, ac wall adapters are still plugged in and consume power, even though gadgets like TVs, VCRs, and cordless phones are supposedly off. And, the problem is expected to worsen as more electronic consumer products pervade the home.

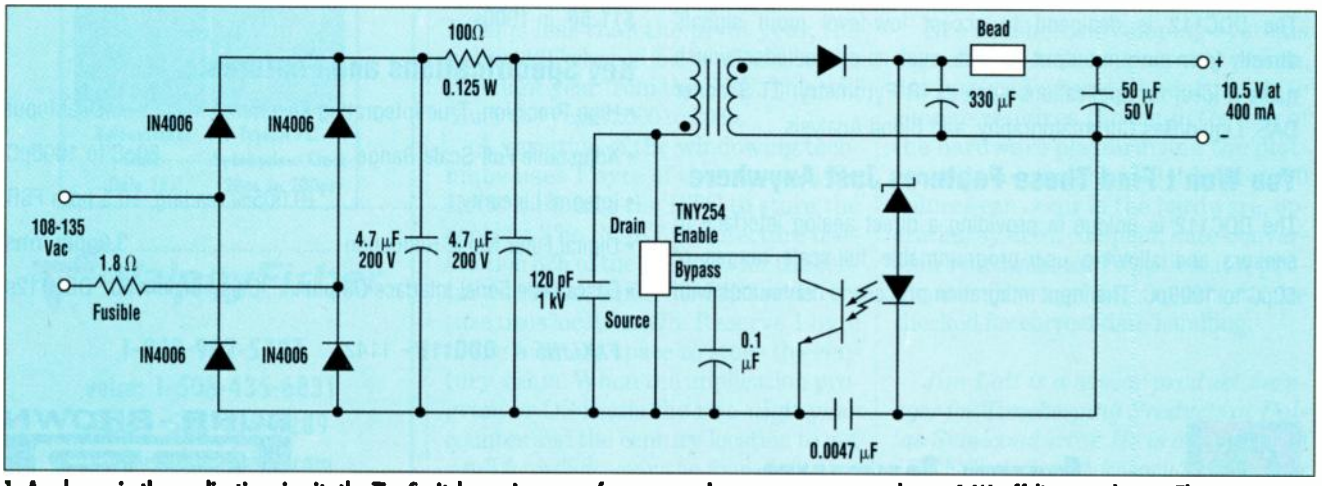
This wasted energy costs money, as well as contributes to pollution. According to a study conducted by Lawrence Berkeley National Laboratory, Berkeley, Calif., in the U.S. alone, consumers pay over $3.5 billion annually to keep a variety of electronic widgets in stand-by mode. To curb such wastage, several energy-saving guidelines have been established around the world. The U.S. Energy Star program, for example, has been extended to consumer electronics, with efforts underway to cover home audio and DVD players. Likewise, Germany's Blue Angel legislation is catching momentum in Europe.

To enable a new class of energy-efficient off-line ac adatpers and stand-by power supplies, Power Integrations Inc. has crafted a radically new switcher solution for low-power (10 W and below) applications (*Fig. 1*). And, at the heart of this solution is a proprietary controller chip called TinySwitch.

"This new design reduces the energy wastage from the 1.2 W (typical) seen in today's conventional, linear, ac wall adapters (or bricks) to less than 100 mW," says Shyam Dujari, director of marketing at Power Integrations. Plus, he adds, it provides a compact, light-weight adapter or stand-by supply with universal input. Because fewer low-cost external components are needed with this solution, the total system cost is also significantly cut, notes Dujari. By comparison, pulse-width-modulated (PWM) based off-line switchers are bulky and cost more, according to Dujari.

Designed to be a simple, on/off control device, the TinySwitch integrates on-chip a 700-V power MOSFET; oscillator; high-voltage, switched-current source; current limit; and thermal shutdown circuitry (*Fig. 2*). Unlike the conventional PWM controller, it uses an on/off control to regulate the output voltage. In this scheme, when the on-chip oscillator is enabled, it turns the power MOSFET on at the start of each cycle. The MOSFET is turned-off as soon as the output current reaches the upper limit.

The maximum on-time of the power MOSFET is determined by the duty cycle signal (D_{MAX}) of the internal oscillator. Also, the current limit and switching frequency for a given TinySwitch is fixed, while the power delivered is proportional to the primary inductance of the transformer. Because the TinySwitch is powered directly by the incoming high voltage, it eliminates the need for an auxiliary bias winding and associated circuitry, thereby simplifying the design of the transformer. In fact, the manufacturer recommends standard, low-cost transformers based on ferrite cores like



1. As shown in the application circuit, the TinySwitch requires very few external components to complete a 4-W, off-line ac adapter. The output power is proportional to the primary inductance of the transformer, and is independent of the input voltage.

Speed PLUS™

CCD Signal Processing

Low Power, Low Cost Digital Camera IC

VSP2000 is a complete digital camera IC providing signal conditioning and 10-bit analog-to-digital conversion for Charge Coupled Devices (CCD) array signals. It features Correlated Double Sampling to extract video information from the pixels, 0 to +34dB gain range with analog control for varying illumination conditions, and black level clamping for an accurate black level reference. VSP2000's 150mW at 2.7V operation makes it suitable for portable applications such as digital still cameras, while its 10-bit 18MHz conversion rate make it a great choice for PC/Video conferencing and security cameras.

Key Specifications:

- Correlated Double Sampling
- Portable Operation:
  - Low Voltage ..... Down to 2.7V
  - Low Power ..... 150mW at 2.7V
- Gain Range ..... 0 to +34dB
- High SNR 53dB
- Priced from $5.75 in 1000s

FAX*LINE* # 11432

Low Power, Low Cost Digital Scanner IC

VSP3000 is a complete, three channel Image Signal Processor for CCD or Contact Image Sensors (CIS). Each channel contains sensor signal sampling, black level adjustment and a programmable gain amplifier. The three inputs are multiplexed into a high speed, 12-bit 10MHz analog-to-digital converter. Input circuitry can be configured by digital commands for CCD or CIS. Correlated double samplers and a black clamp are provided for CCD sensors. For CIS devices, the VSP3000 provides correlated single samplers and reference input.

Key Specifications:

- Three Correlated Double Samplers
- 3-Channel, 6MHz Color Mode
- Internal or External Voltage Reference
- +3V or +5V Digital Output Compatibility
- Available in 48-lead LQFP Surface-Mount Package
- Priced from $5.75 in 1000s

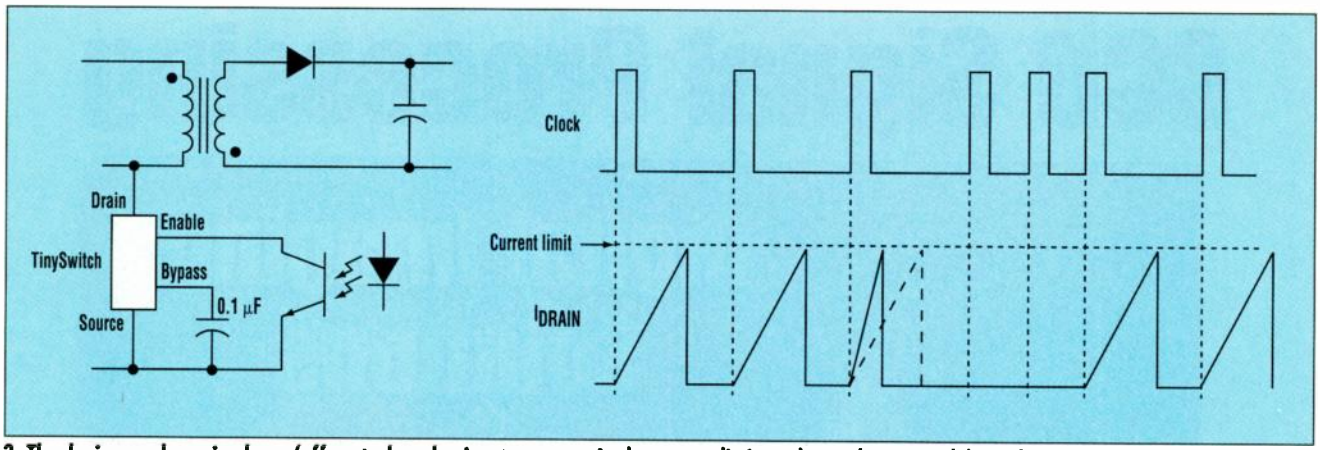
FAX*LINE* # 11444

www.burr-brown.com

BURR-BROWN®

Burr-Brown Corporation • P.O. Box 11400 • Tucson, AZ • 85734-1400 • Call **(800) 548-6132** or use FAX*LINE* **(800) 548-6133** • **http://www.burr-brown.com/**

Distributors: Arrow: (800) 777-2776 • Digi-Key Corp: (800) 338-4105 • Insight Electronics: (888) 488-4133 • J.I.T. Supply: (800) 246-9000 • Sager Electronics: (800) 724-3780 • SEMAD (Canada): (800) 567-3623



3. The device employs simple on/off control mechanism to operate in the current limit mode, so that it can deliver the same energy every cycle. The current-limit operation rejects line-frequency ripple. The current limit and clock cycle for each device is fixed.

EE16, which is available from multiple sources.

Novel Operation

The very-high loop bandwidth of the device provides excellent transient response and fast turn-on, with practically no overshoot, claims Dujari. As per the data sheets, the turn-on time is about 1.0 ms at no load. Plus, he adds, the fixed current-limit operation rejects the line ripple, as the energy delivered is independent of the input voltage (*Fig. 3*). Other features include glitch-free output when the input is removed, and thermal protection. No loop compensation is needed. The thermal shutdown threshold is set at 135°C, with 70°C hysteresis. Consequently, when the junction temperature exceeds 135°C, the power MOSFET is disabled. It remains disabled until the die-junction temperature goes under 70°C, at which point it is re-enabled.

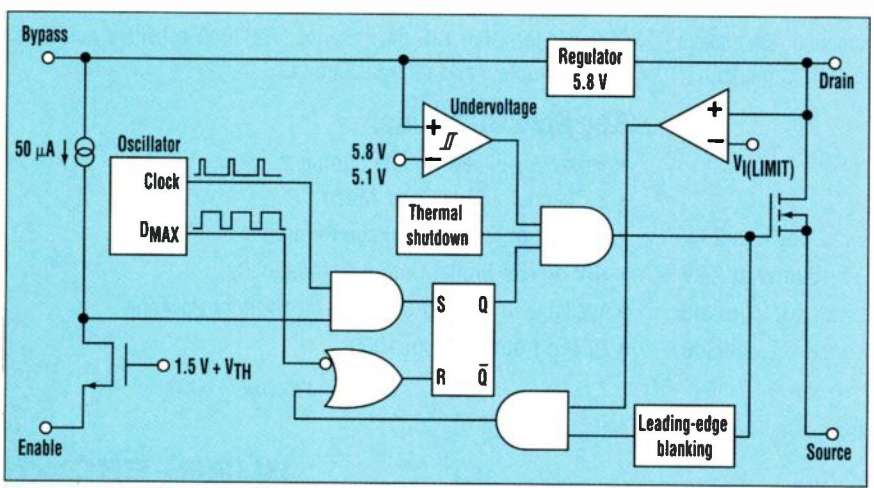
Under no-load condition, the TinySwitch consumes only 30 to 60 mW at 115/250-V ac input. As a result, stand-by supplies based on the TinySwitch can meet Blue Angel, Energy Star, Energy 2000, and European cellular phone standards. This smart integration of a high-voltage MOSFET switch with low-voltage control and protection functions is made possible by the company's proprietary CMOS process.

The TNY253/254/255 are the first three members of the TinySwitch family. Aimed at TV/VCR stand-by solutions, the TNY253 is rated for 5-W supplies. Likewise, TNY254 delivers up to 8 W for cellular phone chargers and PC stand-by supplies. Both the TNY253 and TNY254 switch at 44 kHz to minimize EMI filtering requirements, and permit the use of a simple snubber clamp to limit drain spike voltage.

However, the TNY255 uses a higher switching frequency of 130 kHz to deliver up to 10 W for applications like cell phone chargers and PC stand-by power. All three units allow the use of low-cost, EE16 core transformers. Typical conversion efficiency offered by a TinySwitch-based power converter is 70%-to-75%.

"The efficiency is constant all the way down to very-low power," states Power Integrations' vice president of engineering, Balu Balakrishnan. In PWM-based switchers, the losses stay fixed, as a result, the efficiency goes down with load, Balakrishnan says. By comparison, he adds, the TinySwitch skips cycles at low load to keep the switching losses lower and efficiency higher.

To simplify using TinySwitch devices in power-supply applications, Power Integration's engineers have readied several reference designs and application notes. These include a 1.5-W TV/VCR stand-by circuit, an 8-W PC stand-by supply, and a 3.5-W cellular phone charger. In addition, there is a 0.5-W off-line ac adapter. Evaluation boards are also available for these applications.

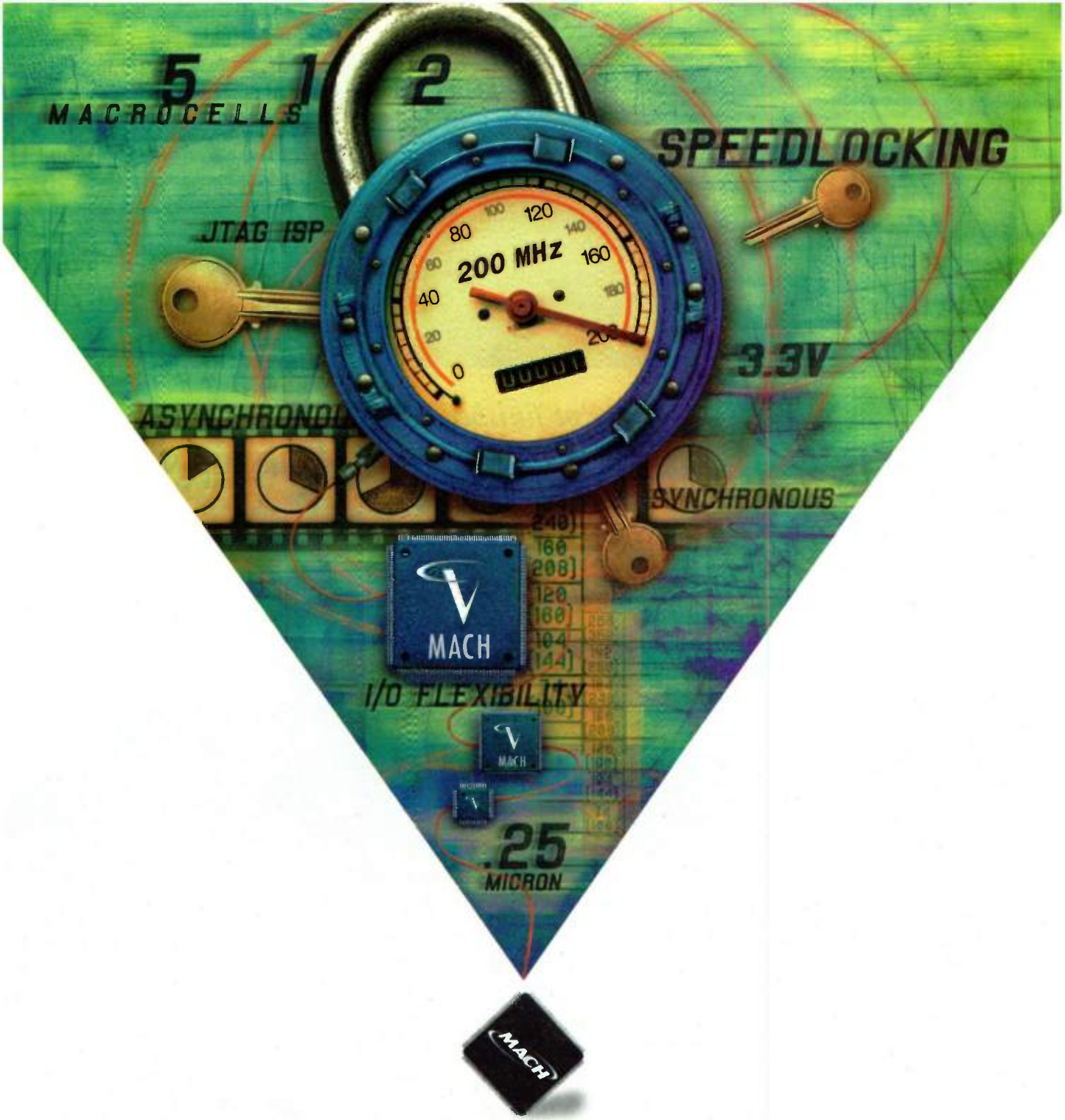


2. This functional block diagram shows that the TinySwitch controller packs an oscillator, Enable circuit, 5.8-V regulator, under-voltage circuit, hysteretic over-temperature protection, current limit, leading-edge blanking, and a 700-V lateral power MOSFET. This is made possible by the semiconductor supplier's proprietary 3.0 µm single metal CMOS process.

Price And Availability

The TinySwitch TNY253/254/255 devices are available in 8-pin DIP and 8-pin SMD packages. In 10,000-piece quantities, the prices range from $0.75 to $0.81 each.

Power Integrations Inc., 477 N. Mathilda Ave., Sunnyvale, CA 94086; (408) 523-9265; www.powerint.com **CIRCLE 451**



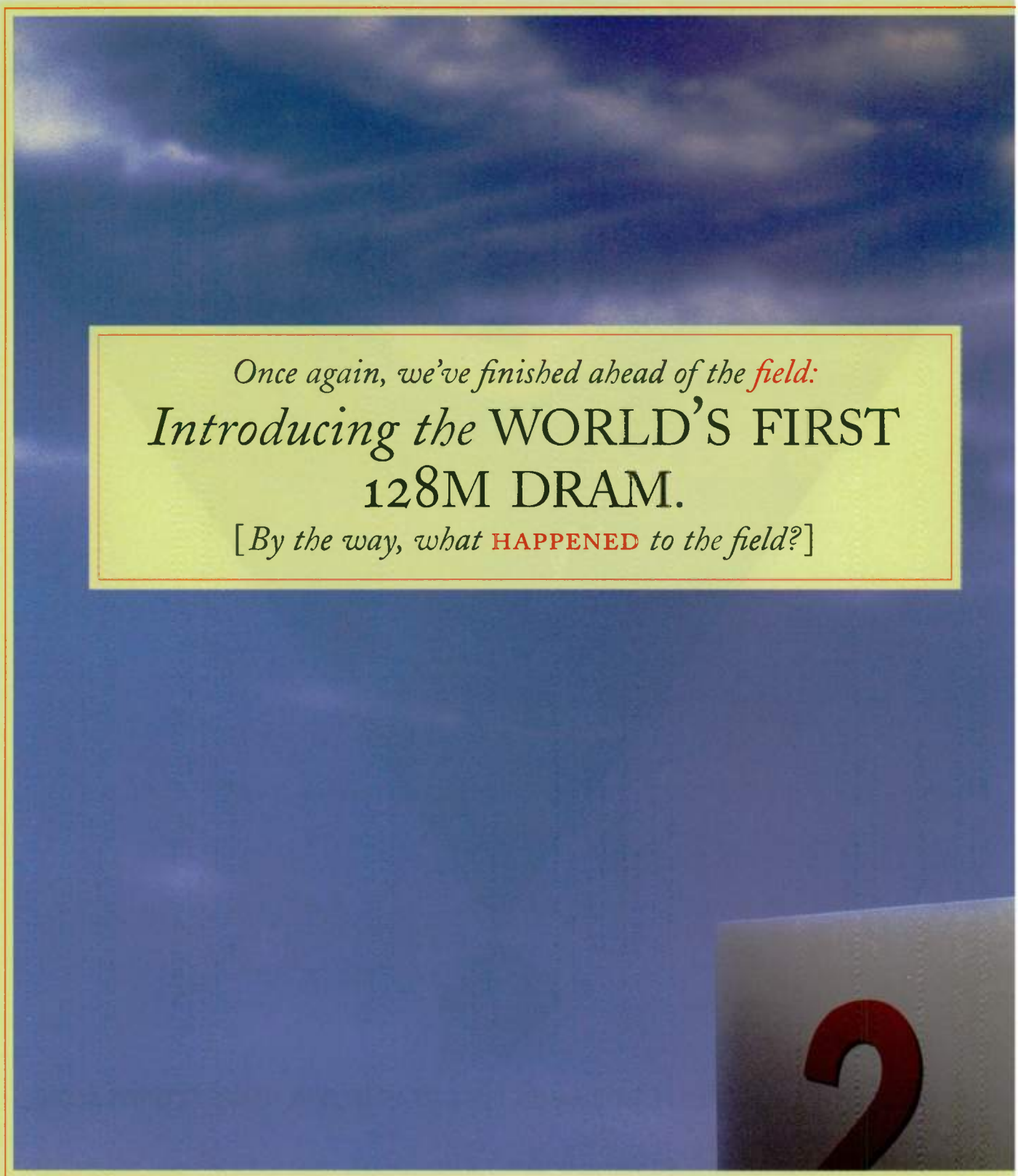
AT 5ns THEY RIP. BUT CPLD PERFORMANCE ISN'T MEASURED IN NANOSECONDS ALONE.

The MACH® family of CPLDs. 32 to 512 macrocells. 32 to 256 I/Os. Speed is speed (and in this case, 5ns). But high density and maximum flexibility also provide cost-effectiveness and faster time to market. Pick your definition of performance. Call 1.888.862.8472.

VANTIS
BEYOND PERFORMANCE

www.vantis.com/machad

An AMD Company.



Once again, we've finished ahead of the field:

Introducing the WORLD'S FIRST 128M DRAM.

[*By the way, what* HAPPENED *to the field?*]

It's the highest-density DRAM ever made available in production volume.

It's a single chip that has hundreds of times the capacity of the computer that took Apollo 11 to the moon.

It's the 128M Synchronous DRAM,

The PC 100*-Compliant,* 128M SDRAM

COMPONENTS	
KM416S8030T-GL	8M x 16
KM48S16030T-GL	16M x 8
KM44S32030T-GL	32M x 4
MODULES	
KMM377S6427T1-GL	512MB DIMM*
KMM377S3323T-GL	256MB DIMM
KMM466S1723T2-FO	128MB SODIMM

and if you want it in quantity, the place where you can get it now is Samsung.

The 128M is particularly notable when you put it into a module. For instance, we offer a 128-megabyte SODIMM, for notebooks. And DIMMs

 **Assembled with Samsung* 128M DRAMs, *stacked by packaging-technology partner* STAKTEK.®

with capacities up to 512 megabytes, for high-end applications like servers.

When you think about what that kind of capacity will do for your customers' applications, you see one thing.

A product that will let you—like us—finish well ahead of the field.

For complete information, visit www.samsungsemi.com, now. Or call 1-800-446-2760 or write to DRAM Marketing, Samsung Semiconductor Inc., 3655 N. First St., San Jose, CA 95134.

SAMSUNG
SEMICONDUCTOR

Still A *Generation* Ahead.

READER SERVICE 144

40 YEARS AGO IN ELECTRONIC DESIGN

Ad: High-Speed Switching

High-speed switching...with reliable T/I silicon transistors. New improved TI 2N337 and 2N338 specifications provide greater design flexibility for your switching circuits...nuclear counters...pre-amplifiers...RF amplifiers...455 KC IF amplifiers...and many other high-frequency applications.

You get high gain at low current levels with TI diffused silicon transistors. High alpha cut-off...10 mc min for 2N337, 20 mc min for 2N338...and extremely low collector capacitance assures optimum performance in your switching and high-frequency amplifier applications. *(Advertisement, ELECTRONIC DESIGN, October 1, 1958, p. 43)*

One of the good things about semiconductor device ads in the transistor era was that they could include actual circuit diagrams, always welcomed by design engineers. This ad highlights TI's emergence as one of the leaders in the semiconductor industry. In the lower left hand corner, the ad trumpets the claim, "World's Largest Semiconductor Plant."—Steve Scrupski

Editorial: Have Convention, Must Travel

A glance at the calendar of meetings, conferences, and symposiums in this issue presents the engineer with a problem. If he wants to keep up with the "latest developments" in electronics and see the "latest products," he must say goodbye to his wife, kids, and office. Even the convention commuter will miss some meetings, since there are many overlaps.

Which one will you attend? Can you afford to miss that one? Tradition underlines many get-togethers and they must go on. A check on the freshness of technical papers to be presented reveals the paucity of new disclosures. You frequently see a lack of theme; a frantic futility for the meeting agenda to be all things to all people. Take in such gatherings to renew social acquaintances or to see some new geography, not to keep up with electronics. Only the large conventions, such as this month's NEC, can appeal to broad numbers and at the same time provide a solid diet for the specialist. If travel is not an obstacle, conventions on single subjects offer the best meat.

Of course, an impelling reason to attend conferences is to meet engineers working in the same field. The swapping of notes is often worth the rail fare. But isn't this area the least well planned by most convention sponsors? Even the most gregarious engineer has small chance of gaining useful information by randomly sampling strangers. Small talk at cocktail parties reigns over shop talk. One of the most effective mediums for channeling multilateral communication is a workshop or scheduled discussion session. A good leader can set group dynamics into motion. Everyone picks up worthwhile ideas.

It looks like conventions will continue to spawn. The discriminating convention goer will have to choose wisely if he is not to waste his time. A few protests (ours included) over the dull reading of papers has burgeoned into a campaign for improvement. Voice your opinion on the planning of conventions to facilitate the exchange of information by engineers. It will pay off.—James A. Lippke *(ELECTRONIC DESIGN, October 1, 1958, p. 15)*

The NEC was the National Electronics Conference, usually held in Chicago. Although the editorial is obviously dated—note the references to only male engineers and to the rail trip—its major points are still relevant.—Steve Scrupski

Steve Scrupski is a former Editor-in-Chief of ELECTRONIC DESIGN. Now semi-retired, he can be reached at scrupski@worldnet.att.net.

Think Ethernet

Looking for news on the Gigabit Ethernet market? "Gigabit Networks," from IGI Consulting, might be worth checking out. This 1998 study has been updated with some current and in-depth research. Also thrown in are bits of information and viewpoints from market leaders and individuals in the Gigabit Ethernet Alliance.

The report ranges from the evolution of Gigabit Ethernet to an explanation of the technology and the most up-to-date Gigabit Ethernet standards. It addresses current issues in the market, such as the pros and cons of copper and fiber cabling. Problems and issues that could arise from this usage, such as fiber differential mode delay, are discussed.

The battle between Gigabit Ethernet and ATM technologies is also spotlighted. With their individual strengths, each of these applications can win out against the other. Yet, their weaknesses, as well as the fact that each aims toward different applications, make it hard to predict a winner.

Great emphasis is placed on the driving forces behind the Gigabit Ethernet market. A five-year forecast takes a close look at obstacles that may hinder market growth.

As technology moves from Ethernet to Fast Ethernet and then on to Gigabit Ethernet, it would help to have a strategy to effect a quicker and smoother transition. The study provides one, as well as an outline of factors that will ensure a successful Gigabit Ethernet market.

Background information on Gigabit Ethernet fills in essential information, such as hardware, network use, characteristics tables on network interface cards, Gigabit Ethernet switches, and routing switches. Vendor and product information examines Gigabit Ethernet vendors and their products, including company information, product applications, and prices.

For more information, contact the Information Gatekeepers Inc., 214 Harvard Ave., Boston, MA 02134; (617) 232-3111; fax (617) 734-8562; www.igigroup.com.—**NK**

Time For A Little Noise Reduction?

The New Allegro A6800 Series Soothes the Irritations Usually Found in VF Display Drivers

If you work with vacuum-fluorescent displays, then you know that electronic noise can really disrupt system capabilities. Allegro's new A6800 series VF display drivers feature slew rate limiting to reduce noise and optimize your display performance.

Brighter, clearer, and now a lot less noise... the A6800 Series Vacuum-Fluorescent display drivers from Allegro.

Over the years, Allegro has developed a track record of leadership and expertise in the VF display driver market with the design and manufacture of the industry-standard UCN5800 series. The A6800 is our latest generation of VF display driver technology incorporating the new features that today's systems demand at a competitive price.

The A6800 series features a serial input with CMOS shift registers and latches for direct interfacing to microprocessor-based systems. All members of the series achieve data rates up to 33 MHz (with 3.3 V or 5 V logic supply). They also include inter-digit blanking and npn darlington outputs with 40 mA source capability.

The A6800 series... It's the new baby on the block that comes with a little peace and quiet— from Allegro.

Call us today to sample its performance. For more information on our complete line of power ICs, mixed-signal ICs, and sensors, check our web site at www.allegromicro.com or e-mail us at PowerInterface@deceater.orgella.com

Allegro A6800 series comes in 10-, 12-, 20-, or 32-bit configurations, designed to pacify all your applications.

The Clear Choice for Power Interface Displays

Allegro™ MicroSystems, Inc.

CALL • 1 • (508) • ALLEGRO

115 Northeast Cutoff, P.O.Box 15036, Worcester Massachusetts 01606 www.allegromicro.com

READER SERVICE 98

TECH INSIGHTS/QUICKLOOK

JUST 4 THE KIDS

For years, people have adored Dr. Seuss. Many held on to their childhood copies of classics like *Green Eggs and Ham*. So, it's no surprise that these books still introduce children to reading. Thanks to Broderbund Software Inc., Novato, Calif., these works are now available as a series of three interactive CD-ROMs. Known as Dr. Seuss Preschool, Dr. Seuss Kindergarten, and Dr. Seuss Kindergarten Deluxe, these CD-ROMs don't just entertain your child. They also teach reading and math skills.

The Dr. Seuss Preschool CD-ROM features graphics, five original songs, and over 200 animations for children ages two to four. It begins with the child being greeted by a singing Cat in the Hat as he travels to Seussville. Once there, the child is introduced to some of the CD-ROM's starring characters. The elephant hero Horton uses positive reinforcement to guide the child through learning experiences. Horton and the child help baby Elma Sue find her mother. This adventure leads the child through multiple activities, including more than 250 lessons.

Through the interaction with the Seuss characters, the child engages in many different reading and math activities. These include:

- Mayzie ABC, which teaches letter recognition, alphabet sequence, and upper- and lowercase letters.
- Floob Phonics focuses on phonics, reading readiness, and vocabulary.
- Pop's Rhymes instructs the child in auditory discrimination, book basics, and sentence building.
- In Monkey Matching, the child learns phonics, listening, and memory skills.
- Yertles Counting Turtles focuses on numbers, quantities, and counting.
- Fox in Socks Sorting teaches sorting, classifying, sizes, colors, and patterns.
- Fish Follies helps the child learn attributes, shapes and sizes, and following directions.
- Sneezlebee 123s covers counting, numbers, and matching.

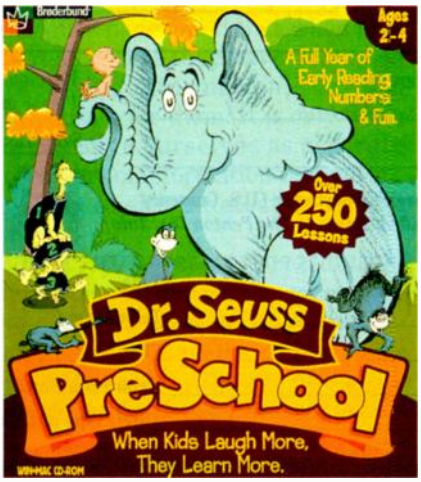
The child's progress is tracked, letting parents see what skills their child successfully completed, as well as the areas that may require practice. With three skill levels for each activity, the child remains challenged.

The Dr. Seuss Kindergarten and Kindergarten Deluxe CD-ROMs star more than 50 popular Dr. Seuss characters. Targeted at children ages four to six, they teach skills needed for Kindergarten.

In each CD-ROM the child joins the zany zookeeper, Gerald McGrew, on a search for exotic animals. Along the way, they travel to exciting places like Bumble Tub Creek and the storybook land of Barbaloots, where they can harvest truffula fruits.

Travelling through this virtual world exposes the child to a host of reading and math activities, including:

- Bippo Alphabet, which teaches alphabet sequencing, upper- and lowercase letters, and reading readiness.
- Bumble Tub Phonics focuses on phonics, consonant blends, and spelling.
- Thidwicks Rhymes concentrates on reading, sentence building, and auditory discrimination.



MARIFRANCES WILLIAMS

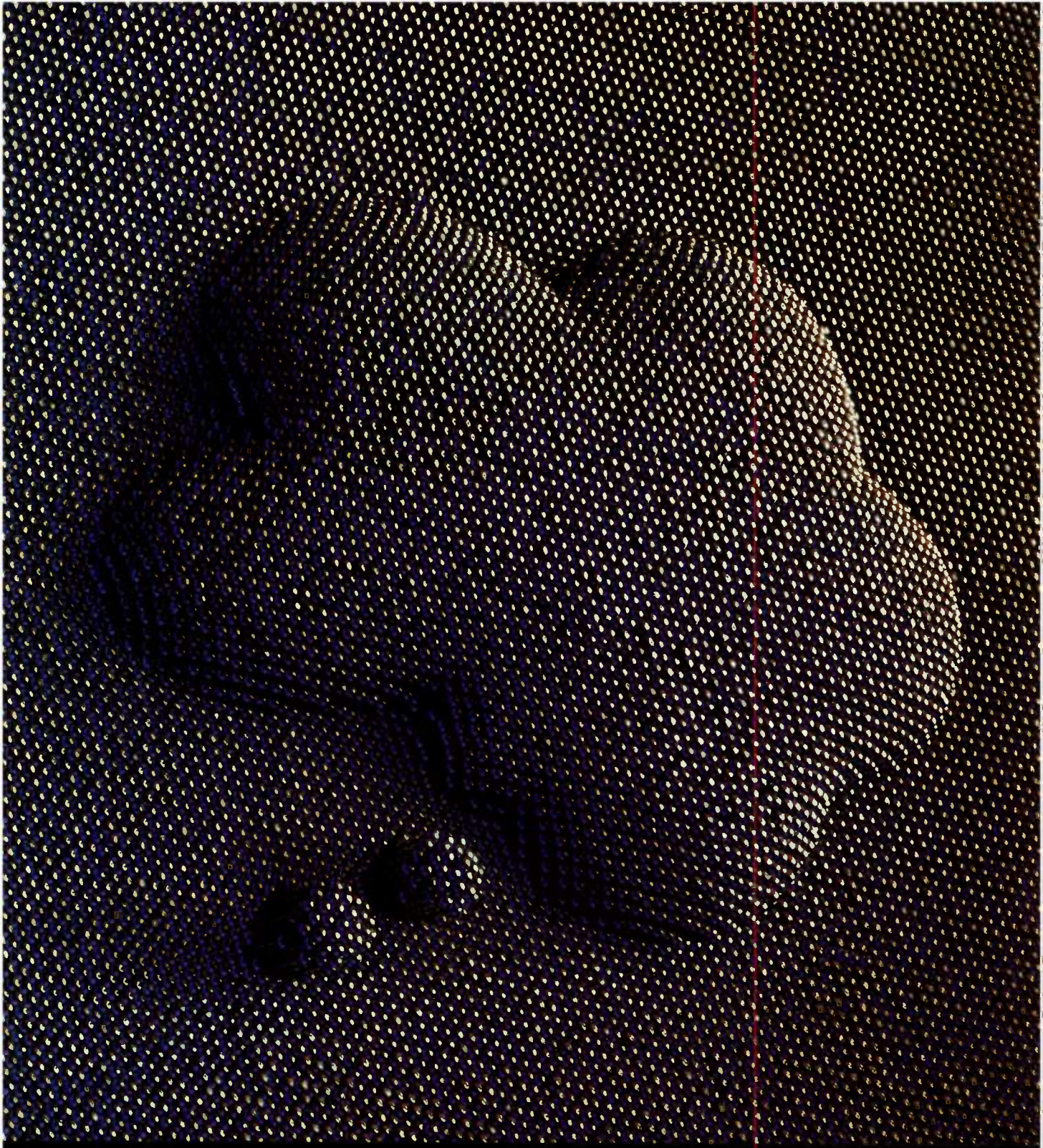
- East/West Beast Logic focuses on discerning similarities and differences, as well as classifying and logic.
- Sneetch Patterns teaches pattern recognition, sequencing, and attributes.
- Snuv Glove Matching concentrates on counting, shapes and patterns, and memory skills.
- Birthday Pet Measurement introduces the child to measurement, estimation, and quantities.
- Barbalot Math teaches addition, subtraction, and counting.

Much like the Preschool CD-ROM, this program tracks the child's progress and skill level. The skills acquired should put the child ahead of the class upon entering Kindergarten. Each Kindergarten Deluxe CD-ROM contains a full year of Kindergarten basics, along with a printable workbook CD-ROM that includes more reading and math lessons, math flashcards, and a number- and letter-writing tool.

If you grew up reading Dr. Seuss, you'll appreciate these animated, interactive CD-ROMs which blend colors, original music, a rich mix of sound effects, and zany graphics. The action is so engaging that your child will want to use the CD-ROM's over and over—much like reading a book. But luckily, you won't have to do all the reading. Best of all, the child learns as they play.

Dr. Seuss Preschool, Kindergarten, and Kindergarten Deluxe are now available at retail stores for $19.95, $19.95, and $29.95, respectively. For more information, contact Broderbund Software Inc., 500 Redwood Blvd., P.O. Box 6121, Novato, CA 94948; (415) 382-4400; www.broderbund.com.

Marifrances D. Williams holds a degree in Liberal Studies from San Diego State University, Calif. She is currently a fifth-grade teacher at Los Ranchos Elementary, San Luis Obispo, Calif. Williams specializes in the identification of advanced technology for the use of child-focused applications. She may be reached at williamsofsm@lightspeed.net.



WHAT WOULD IT TAKE TO PUSH YOUR IDEA OF AN OSCILLOSCOPE INTO A NEW DIMENSION?

Let's start with a completely new class of oscilloscopes. They're called Digital Phosphor Oscilloscopes, or DPO for short. With them you can understand complex, rapidly changing waveforms at a glance. Find even the rarest glitches. And get real-time visual and statistical insight into the distribution of edge jitter. Even when you're pushing data at gigabit speed. Because with DPO, being able to see more means you can work faster. For a quick demonstration, go to www.tek.com/dpo1/ Or call 1-800-426-2200, ext. 3023, to learn about the next dimension in oscilloscopes.

Tektronix®

WRH

Test Your Skill And Win Big Prizes!

So you work in the electronics industry. You probably have a laundry list of impressive credentials. Well, we at *ELECTRONIC DESIGN* would like to add one more credit to that list: Winner of the 1998 Electronic Design Automation (EDA) Challenge. All you have to do is enter the 1998 *ELECTRONIC DESIGN* EDA Challenge contest, running from October 1 to November 30.

The rules are simple. You pick a topic. Then, write about it in any format you choose. Your submission cannot exceed 300 words. Sound easy enough for you? There's just one catch—you have to use as many names of EDA tool vendors as you can. For example, you can work their names into the regular text or just talk about them as vendors. There's probably tons of ways to include their names, so it's basically up to you.

Just remember that the person with the most EDA tool vendors in their text, along with the most creative use of the vendors' names, wins. For quick reference and some extra help, a list of all EDA tool vendors will be provided on *ELECTRONIC DESIGN'S* web site. Winners will be announced via the web on December 15, and some of the more innovative entries may even be published in the magazine.

Winners will receive a prize donated by sponsoring EDA tool vendors, including Accel Technology, IKOS, InterHDL, Model Technology, MINC, Novas Software, Orcad, Transcendent, VeriBest, and Xynetix. There's no catch. You don't have to buy anything. Guaranteed! And, just look at some of the exciting prizes you could win: a Magellan GPS 400XL Satellite Navigator, a Tripmate GPS navigation system, a Palm Pilot, and an Iomega Zip Drive. There's also EDA tools such as Novas Software's Debussey or MINC's VHDL Easy, a CD player, cash awards, a Dilbert Survival Pack and Dilbert desk calendar, and—a gift for anyone who has a child—Beanie Babies. And, this is only the beginning!

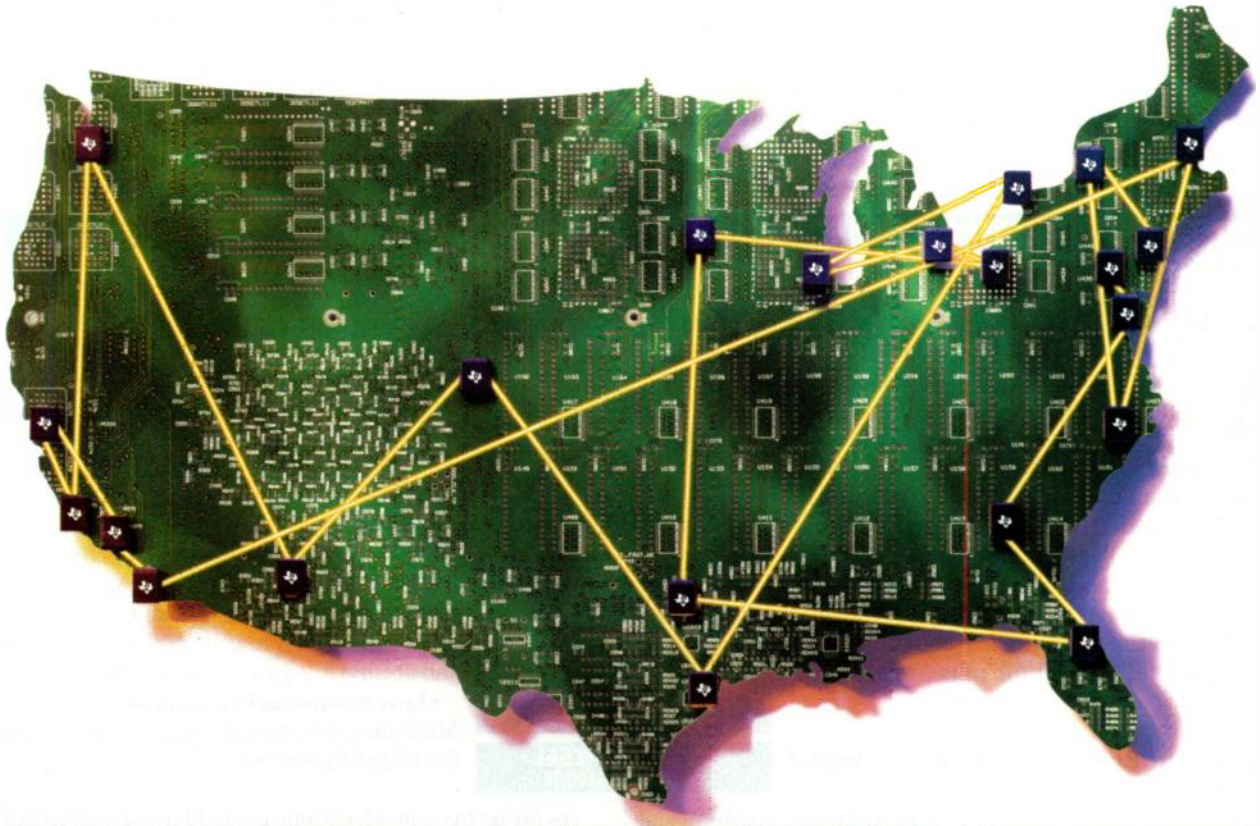
Log onto the *ELECTRONIC DESIGN* web site to get a complete listing of all prizes, participating EDA tool vendor sponsors, and contest details. While you're there, check out our latest addition to the EDA Technology Lab: EDA Technical Company Profiles. This section will provide you with the information you need to determine which EDA tool vendors can provide the type of solutions you want. It outlines which companies solve which problems, how much these solutions cost, and what platforms they support.

Instead of just telling you which companies do verification, for example, you can find out which ones offer code coverage, formal verification, and HW/SW coverification tools. Or, if pc-board design is your game, you can find out which companies offer signal integrity, packaging, and virtual prototyping solutions. The best part of this web information is that it isn't marketing hype. It's just valuable technical information that can position you in the right direction. Don't pass this or the contest up. You don't want to miss out on the fun!

Please send all entries to Cheryl Ajluni, 2025 Gateway Pl., Ste. 354, San Jose, CA 95510, or via e-mail at cjajluni@class.org. Be sure to include your name, address, company affiliation, phone number, and e-mail address. All *ELECTRONIC DESIGN* readers are eligible to participate, unless employed by EDA tool vendors.

Cheryl Ajluni

THERE'S A FREE WAY TO THE LATEST DSP/ANALOG INFORMATION.



REGISTER FOR THE TI DSP/ANALOG SEMINARS.

In 22 cities in 40 days, Texas Instruments will hold free seminars on the latest high-performance DSP and Analog products.

It's a great opportunity to find out why TI is the technology and performance leader in DSP, Analog and Mixed-Signal, making us the ideal semiconductor partner to help bring your designs to market faster, at a lower cost and with more differentiation.

We'll provide up-to-the-minute information on the newest devices, design methods and real-world applications that can help you maximize your potential. The first-day seminar is DSP-exclusive. The second day, Analog-exclusive. For the broad picture, attend both.

And of course you won't leave empty-handed. You'll have access to free and discounted items including all the tools you'll need to be most productive when working with TI.

To register, or for more information, call 1-800-477-8924, ext. 1998, or visit our Web site.

Sept. 28-29	Philadelphia, PA
Sept. 29-30	Baltimore, MD
Oct. 1-2	Atlanta, GA
Oct. 5-6	Orlando, FL
Oct 6-7	Dallas, TX
Oct. 7-8	Minneapolis, MN
Oct. 8-9	Cleveland, OH
Oct. 12-13	Chicago, IL
Oct. 13-14	Detroit, MI
Oct. 14-15	Toronto, Ontario
Oct 15-16	Houston, TX
Oct. 19-20	Denver, CO
Oct. 20-21	Phoenix, AZ
Oct. 21-22	Seattle, WA
Oct. 22-23	Woodland Hills, CA
Oct. 26-27	San Jose, CA
Oct. 28-29	Newport Beach, CA
Oct. 29-30	San Diego, CA
Nov. 2-3	Boston, MA
Nov. 3-4	Raleigh, NC
Nov. 4-5	Rochester, NY
Nov 5-6	Fairfield, NJ

www.ti.com/sc/seminar

15-8957R

THE WORLD LEADER IN DSP SOLUTIONS

TEXAS INSTRUMENTS

Lolli-Pop Tunes

Okay, so we've all heard those strange stories about people actually receiving radio signals through the metal plates in their head. Wacky stories also come around about the same thing happening from a filling or some other metallic object implanted in the body. Those stories, though bizarre, might not even measure up to the strangeness of music emanating from a lollipop.

Actually, the music comes from the lollipop holder. This new toy, called the Silent Shout, is battery operated. To play music inside people's mouths, it vibrates a lollipop that has been inserted into the device. There's a selection of songs that can be played, including a hip-hop rhythm. The sound is conducted through the teeth. It then echoes into the inner ear, which means that no one else can hear it.

This invention comes from Bandai Co., the same people who brought Tamagotchi pets to the world. Most adults I know find those little electronic pets about as cute as Barney. They must be on to something, though, because the kids just love them.

The toy will be released in Japan first, selling for the equivalent of about $10. Meanwhile, back in the U.S., a similar toy has been introduced. Called Sound Bites, it comes from CAP Candy, a division of Hasbro Inc.

For more information, contact Bandai America, 5551 Katella Ave., Cypress, CA 90630; (714) 816-9500; fax (714) 816-6711; www.bandai.com.—**NK**

TIPS ON INVESTING

New All-In-One Investment For Family Savings

All investors face the same dilemma: How can one participate in the high returns of the stock market, but deal with the fear of losing principal at the same time? Parents in particular feel like they're stuck on the horns of this dilemma. Financially, they have to meet the college objective. The older the child, the more accelerated the growth needs to be...Introducing a new Smith Barney all-in-one investment for growth and safety, particularly well-suited for parents and children's savings.

HENRY WIESEL
CONTRIBUTING EDITOR

Principle Protection Equity-Linked Notes

These unique securities, if held to maturity, combine the growth potential of stocks with the principal protection of bonds.

How Principal-Protected Equity-Linked Notes Work

Each equity-linked note is a debt obligation of an issuer. It provides a return, which is tied or "linked" to the performance of a particular stock index, or basket of stocks. Unlike a typical bond, which generally pays semiannual interest and returns the principal amount at maturity, principal-protected equity-linked notes pay little or no semiannual interest. Instead, at maturity, they repay all of the principal plus a percentage of any appreciation in the stock index you've chosen.

Benefits of Principal-Protected Equity-Linked Notes

The terms of each equity-linked note vary. Collectively, however, they offer these benefits to investors:

- **Growth potential**

The return at maturity on principal-protected equity-linked notes is tied to the performance of a particular stock index or basket of stocks, offering investors participation in these potential growth opportunities.

- **Diversification**

Their link to a variety of stock indices can further diversify an existing portfolio mix of stocks, bonds, mutual funds, and cash.

- **Preservation of capital**

At maturity, principle-protected equity-linked notes return your original investments (or the predetermined percentage of principle), regardless of market performance.

- **Liquidity**

While most principle-protected equity-linked notes are structured as "buy-and-hold" investments, they are typically listed and traded on a major exchange to buy or sell at anytime prior to maturity.

- **Low minimum investment**

Minimum investments start as low as an affordable $15 per unit.

As far as tax considerations go, holders of equity-linked notes issued after August 13, 1996 are required to recognize interest income at a predetermined rate in each tax year—prior to the note's maturity. This amount is determined by using the yield that would be paid by the issuer on noncontingent debt that has similar terms and conditions as the equity-linked note. A schedule of the income amount will be provided in the prospectus. Investors should consult with their tax advisors and review the prospectus for this and other tax considerations.

Although the note's principal is protected at maturity, depending on the market prior to maturity, it can trade above or below the issue price. Some of the market movements that can affect the value of a note include the index level, the volatility of the index, interest rates, and the remaining time to maturity. Holding all else constant, as the index level and volatility rise, the value of a note should increase. As they decline, the value of a note should decrease. When interest rates rise, on the other hand, the value of a note should decrease. The value of a note should go up as interest rates decline.

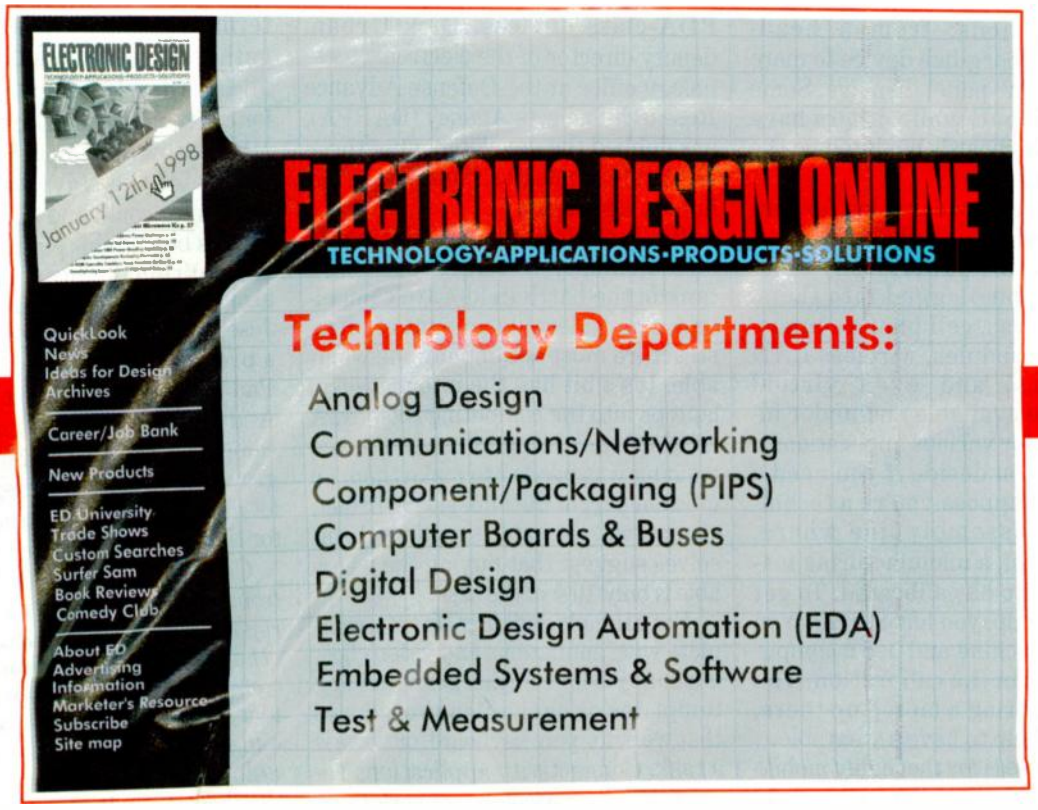
For a free brochure and help in setting up an "Equity-linked note account," write or call Henry Wiesel, first vice president of investments, qualified plans coordinator at Smith Barney, 1040 Broad St., Shrewsbury, N.J. 07702; (800) 631-2221 ext. 8653.

ELECTRONIC DESIGN ONLINE

TECHNOLOGY·APPLICATIONS·PRODUCTS·SOLUTIONS

Get Immediate Online Access To Worldwide Technology

Electronic Design Online has been created for you, the design engineer, as the world's most comprehensive technical information resource and solution center. It offers a compendium of topics—from the contents of current *Electronic Design* issues including all the articles, schematics, and QuickLook features to ED University, Pease Porridge, Career/Job Bank, and more. Link up to our web site today for online forums, direct links to industry organizations and advertisers, trade show previews, industry surveys, technology archives, and humor. In addition, you can now utilize ED JetLINK, the industry's fastest "drill down" tool to find application- and market-specific product solutions and vendors with a minimum number of clicks in one site visit.



www.elecdesign.com

HEADS UP

The wearable is coming into its own. These body-worn computers have been around for a few years, but earlier machines were underpowered and too clunky for practical use. New hardware is starting to look a lot better. The support software, input/output, and communications infrastructure require the brunt of the effort, but the possibilities leave us wondering. Can the benefits justify the considerable efforts needed to deploy a wearable-based computing solution?

A wearable computer repackages a full-function PC into a form factor that can be worn on the body. Commercial providers like Xybernaut, Fairfax, Va., and Interactive Solutions Inc., Sarasota, Fla., favor a box-like PC configuration. Along with a battery pack, it mounts on a user's belt. ViA Inc., Northfield, Minn., configures their product as two interconnected modules in a flexible belt configuration. All are Pentium-class machines, with big hard drives and lots of memory.

Wearables come with voice-recognition software, microphones, and earphones. Users can choose several display options: from a head-mounted, Cyborg-like device to more traditional flat-panel displays. Some allow pen input, while others have miniature keyboards mounted on the user's wrist.

What's more, wearables feature serial, parallel, and PCMCIA (PC Card) slots that permit many other modules to be plugged into them. Video cameras, cell phone connections, GPS modules, wireless LAN connections, and even virtual toolsets are available and under investigation for various applications.

How do you decide if you need a wearable? Suppose you're a technician on an assembly line where, every so often, a manufacturing machine needs to be calibrated. To get the line back up, you have to climb on top of the machine and use a computer to perform the calibration. You really can't bring a laptop up there, so it would help to have a wearable.

Another use is for the highly mobile inspectors gathering data on aircraft, bridges, or industrial equipment. With a wearable, the user can construct a voice-activated template to complete reports right in the field. And, hands are still free to use tools or hoist oneself into position to do the inspection.

CHRIS CHINNOCK

Repair and maintenance technicians can load entire libraries of documentation onto the wearable as Interactive Electronic Technical Manuals (IETMs). With the tiny video camera and wireless network, they can send a picture back to a remote, expert help desk to solve a problem. Also, parts can be located and ordered through the web. These potential capabilities are exciting the military and commercial transportation and equipment industries.

The list goes on. The point is, wearables are evolving into a human computer hub, permitting users to mix and match modules to fit certain applications. They enable a new class of mobile computing, eliminating some shortcomings in laptop portability. Yet, they have more horsepower than PDA-class devices. Dick Urban, deputy director of the electronic technology office at the Defense Advance Research Projects Agency (DARPA), has dubbed the development of these related technologies, "humionics," or human electronics.

While the benefits—getting a production line up faster, or repairing a tank in the battlefield—are compelling, a considerable amount of infrastructure must accompany the wearable. It's a bit like the integration of laptops into the computing toolbox. A lot of software, support hardware, and training was needed to make them an efficient part of the infosphere. In fact, commercial wearable suppliers themselves suggest that buying the wearable is only 10% of the task.

For example, building IETMs, complete with animations and video clips, is a huge job for complex gear. Building templates or navigation procedures that work for pen, keyboard, or voice is a task. Connectivity applications require an entire wireless network to be installed over the work area. Hooking everything together to make it work smoothly is no walk in the park. Nevertheless, many organizations are moving ahead with these projects.

Major automobile and aircraft manufacturers are now looking at production, inspection, or repair scenarios. Transportation infrastructure organizations are evaluating wearables to gather and process information on bridges, signs, and other elements. And, the military is interested in repair and maintenance, as well as military police and logistics services applications.

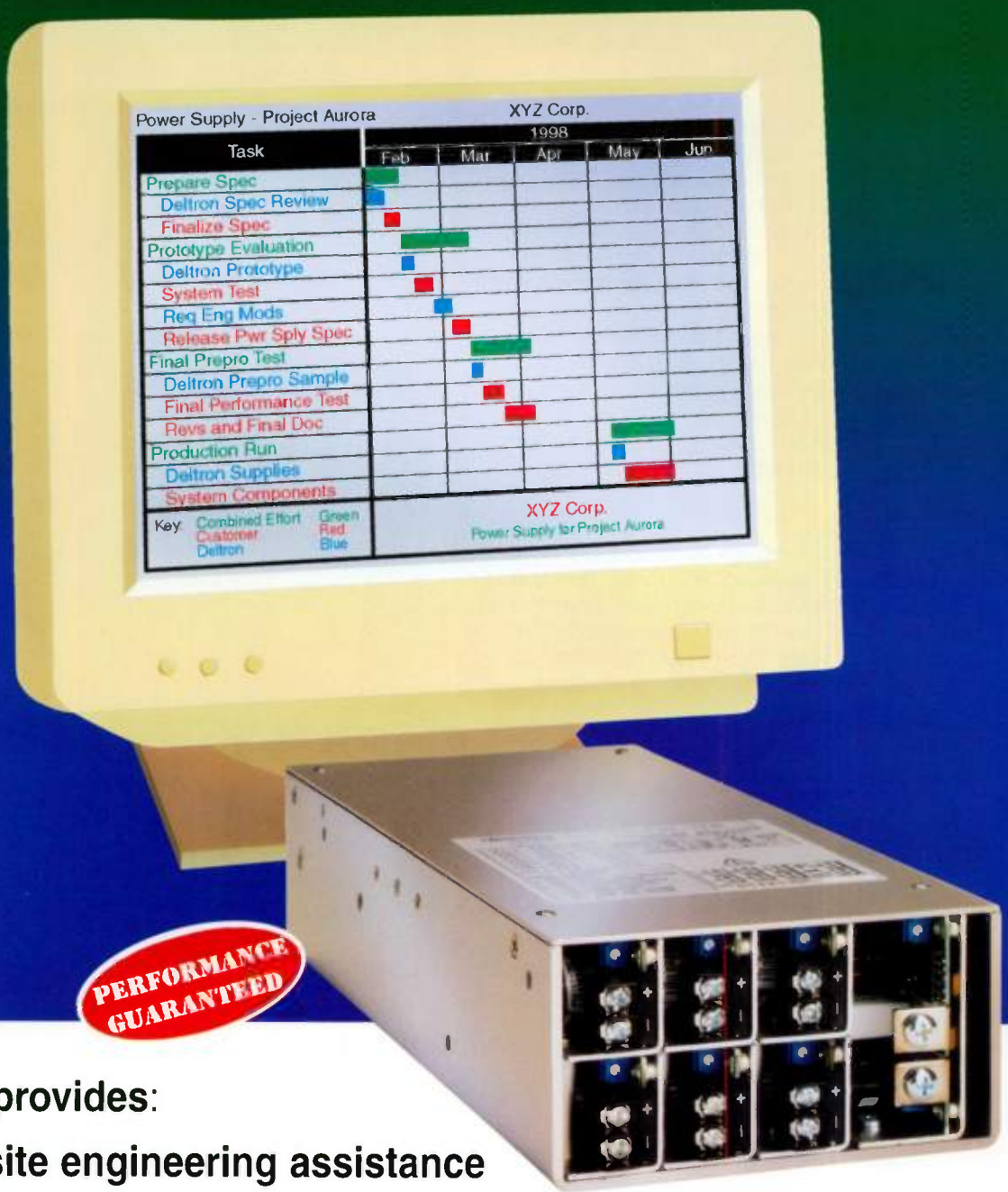
So, where are we in this nascent industry? I would call it the late evaluation phase. My guess is that these tests will soon prove the worth of some highly targeted wearable applications. Sales should begin to pick up from current low levels.

Perhaps the key to the wearables market, like many others, will be tested, usable software that solves specific problems better than the alternative solutions. The players are gathering. General Motors, Detroit, Mich., is developing extensive IETMs for car repair, while Lockheed Martin, Moorestown, N.J., is doing similar things for the Navy's ships. Large companies could end up being the big drivers behind this platform.

Traditional laptop makers could also expand into this area. IBM, San Jose, Calif., has already demonstrated a prototype of a repackaged Think Pad 760 in a wearable configuration. And smaller, specialized devices from companies like FEDEX or UPS could grow into devices that begin to look a lot like wearables. So, keep an eye out for the latest in computer fashion.

Chris Chinnock holds a BSEE from the University of Colorado and reports on flat-panel displays and other emerging technologies. His company, Technical Marketing Service, provides writing, marketing, and pblic relations services to technology companies. Chinnock can be reacheaat (203) 849-8059; fax (203) 849-8063; e-mail: chrischinnock@compuserve.com.

We partner with you to get the job done right and on-time.



PERFORMANCE GUARANTEED

Deltron provides:

- On-site engineering assistance
- Prototypes in two weeks
- J.I.T. delivery

CE UL CSA ISO9002 CERTIFIED

Deltron inc.
POWER PRODUCTS

F Series Power Supplies
0.99 Power Factor
- 1,000,000 + Models
- 400-1000W
- 1 - 7 Outputs
- Ultra Compact Size

WRH

FT • FS SERIES MODUFLEX ® SWITCHERS

DESCRIPTION

The FT and FS Series are comprehensive lines of ultra compact power factor corrected models derived from our Moduflex® family of switching power supplies. This series utilizes advanced technology to produce a high quality input current wave form that is compliant to the harmonic requirements of EN61000-3-2. Based on modular construction, "off the shelf" modules permit high volume manufacturing with an outstanding quality level assuring timely delivery at a competitive cost.

Three classes of output modules are available. The **STANDARD** outputs allow short duration surge currents on all auxiliaries for hard starting loads. Optional **CURRENT LIMITED** outputs have square current limiting and feature wireless droop current sharing. Optional **ENHANCED** outputs have square current limiting, one wire star point current share, output good logic signal with LED, nominal 5V local bias, individual inhibit and margining. For requirements that cannot provide minimum load on the main output, the **ZERO PRELOAD** option is available for main outputs up to 500 watts.

DELIVERY

Choose stocked units or construct a model number using stocked modules for fast delivery. Otherwise, form a model from the adjacent page to meet your specific requirements. Contact factory for deliveries on models derived from non-stocked modules.

FEATURES

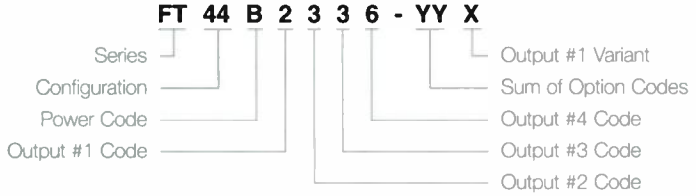
- 0.99 power factor.
- 5.5 watts per cubic inch.
- 1-7 outputs, 400-1000 watts.
- 120 kilohertz MOSFET design.
- Universal input.
- UL, CSA, TÜV (IEC, EN), CE.
- FCC, EN Class A EMI.
- IEC, EN Immunity.
- All outputs:
  - *Adjustable*
  - *Fully regulated*
  - *Floating*
  - *Overload and short circuit protected*
  - *Overvoltage protected*
- Standard features include:
  - *System inhibit*
  - *Fan output*
- Options and accessories include:
  - *Power fail monitor*
  - *Redundancy*
  - *Current Limited Outputs*
  - *Enhanced Outputs*
  - *Zero Preload*
  - *End fan cover*
  - *Top fan cover*
  - *Rack Assemblies*

STOCKED MODELS - Available in 3 days.

Max Power	Output 1	Output 2	Output 3	Output 4	Model*
400W	5V @ 50A	12V @ 12A	12V @ 12A	5V @ 10A	FT46A2332-45P
400W	5V @ 50A	12V @ 12A	24V @ 6A	12V @ 6A	FT46A2363-45P
600W	5V @ 60A	12V @ 12A	12V @ 12A	5V @ 10A	FT46C2332-13P
600W	5V @ 60A	12V @ 12A	24V @ 6A	12V @ 6A	FT46C2363-13P

**400W models include power fail monitor, current limited modules, zero preload and end fan cover options. 600W models include the same options except fan cooling is built into the unit.*

UNITS FROM STOCKED MODULES - Available in 2 weeks.



Configuration: Allowable quad output configurations are 42, 44, 46 and 48.
Power Code: Choose Power Code A through D for 400-750W models.
Output Codes: Select any outputs from the shaded area on the Output Types table consistent with the configuration chosen.
Option Code: Specify Option Code. Refer to the Option table. Codes 02 (redundancy) and 16 (enhanced) are excluded from models available in 2 weeks. Fan cooling is built into 600 and 750W units.

OPTIONS

Option Code	Function
00	None
01	Power Fail Monitor
02	Redundancy
04	Current Limited
08	Zero Preload
16	Enhanced
32	End Fan Cover
64	Top Fan Cover

Replace the YY with the sum of the Option Codes.

MODEL SELECTION

Models are available in power ratings of 400 to 1000 watts, with corresponding code letters A through E. See Power Code chart.

Output modules are available in six types: J, K, L, M, N and P in nominal power ratings from 75 - 500 watts. Type M, N and P modules are variable power rated depending upon the unit power rating. The M, N and P Module table directly below shows the corresponding multiplier applicable to the output current ratings of the M modules and allowable power ratings for the N and P modules. For example, a 750 watt multiple will have its M type module configured to produce 120A @ 5V or 12A @ 48V. The voltage and current rating of output modules are listed in the table of output types. This table assigns an alpha-numeric code designating the nominal voltage rating of the module.

Power Code	Unit Power Rating	M Module Current Multiplier		N/P Module*
		Single Output	Multiple Output	Allowable Power Rating
A	400W	0.8	0.5	250W
B	500W	1.0	0.6	300W
C	600W	1.2	0.8	400W
D	750W	1.5	1.2	500W
E	1000W	2.0	1.5	750W

**When an N or P module is used as the main output, the allowable power and the module current ratings must not be exceeded.*

Output Types*						
Output		Module Type				
Code	Volts	J Amps	K Amps	L Amps	M Amps	N/P Amps
0	2	10	20	30	100	60
1	3.3	10	20	30	100	60
2	5	10	20	30	100	60
3	12	6	12	24	42	42
4	15	5	10	20	33	33
5	18	4	8	16	28	28
6	24	3	6	12	21	21
7	28	2.5	5	10	18	18
8	36	2	4	8	14	14
9	48	1.5	3	6	10	10
A	2.2	10	20	30	100	60
B	2.4	10	20	30	100	60
C	2.7	10	20	30	100	60
D	3	10	20	30	100	60
E	3.6	10	20	30	100	60
F	4	10	20	30	100	60
G	4.5	10	20	30	100	60
H	5.7	10	20	30	90	60
J	6.3	10	20	30	80	60
K	7	9	18	30	70	60
L	8	8	16	30	62	60
M	9	8	15	30	56	56
N	10	7	14	30	50	50
P	11	7	13	27	45	45
Q	13.5	6	11	22	37	37
R	17	5	9	18	30	30
S	19	4	8	16	26	26
T	21	4	7	14	24	24
U	23	4	7	13	22	22
V	26	3	6	12	19	19
W	29	3	5	10	17	17
X	32	2	5	9	16	16
Y	40	2	4	8	13	13
Z	44	2	4	7	12	12

Multiple output modules of a given type are arranged in ascending order by voltage magnitude in the same sense as the output number sequence in the configuration diagrams.
**Shaded ratings are stock.*

HOW TO ORDER

To form the proper model number defining a custom requirement, select the letters FS or FT to designate the series, then choose the desired configuration and list the configuration code. Insert the power code letter for the power level and follow with the output code numbers or letters for each specific output. Enter a dash and from the option table insert the sum of the option codes. Where lower power is desired for the main module, an N module can be substituted and is denoted by a letter N in the output variant position. In addition, when no preload is available for the main output, choose Option Code 08 and add a P in the output variant position. For an enhanced **main** and **current** limited auxiliaries, specify both 04 and 16 option codes.

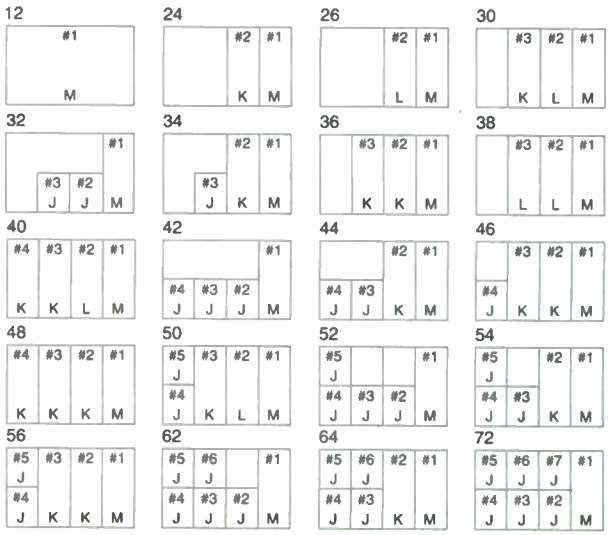
HARMONIC CORRECTED 500W QUAD SWITCHER

FT 44 B 2 3 3 6 - YY X

- FT — Series
- 44 — Configuration
- B — Power Code
- 2 — Output #1 Code
- 3 — Output #2 Code
- 3 — Output #3 Code
- 6 — Output #4 Code
- YY — Sum of Option Codes
- X — Output #1 Variant

OUTPUT CONFIGURATIONS

The boxes below are diagrammatic representations of the power supplies as viewed from the output end. The two-digit numbers above the boxes are the configuration codes.



Refer to the table below for allowable configurations by series.

Output Config	Unit Power Rating				
	400W	500W	600W	750W	1000W
12	•	•	• x	• x	x
24	•			• x	
26		•	• x	• x	x
30					x
32	•			• x	
34	•	•	• x	• x	
36	•	•	• x	• x	x
38					x
40					x
42	•	•	• x	• x	
44	•	•	• x	• x	x
46		•	• x	• x	x
48			x		x
50					x
52	•	•	• x	• x	x
54		•	• x	• x	x
56			x		x
62		•	• x	• x	x
64			x		x
72			x		x

• Represents allowable configurations for the FT Series.
x Represents allowable configurations for the FS Series.

SPECIFICATIONS

INPUT
90-264 VAC, 47-63 Hz.

POWER FACTOR
0.99 typical.

EMISSIONS
FCC 20780 Part 15/EN 55022, Class A Conducted. EN 61000-3-2, Harmonics. EN 61000-3-3, Voltage Fluctuations.

IMMUNITY
IEC 1000-4-2/EN 61000-4-2, Electrostatic Discharge. IEC 1000-4-3/EN 61000-4-3, Radiated Field. IEC 1000-4-4/EN 61000-4-4, Electrical Fast Transients. IEC 1000-4-5/EN 61000-4-5, Level 3 Surge. IEC 1000-4-6/EN 61000-4-6, Conducted Field.

INPUT SURGE
230 VAC - 38 amps max. 115 VAC - 19 amps max.

EFFICIENCY
75% typical.

HOLDUP TIME
20 milliseconds from loss of AC power.

OUTPUTS
See model selection table. Outputs are trim adjustable ±5%.

OUTPUT POLARITY
All outputs are floating from chassis and each other and can be referenced to each other or ground as required.

LINE REGULATION
Less than ±0.1% or ±5mV for input changes from nominal to min. or max. rated values.

LOAD REGULATION
±0.2% or ±10mV for load changes from 50% to 0% or 100% of max. rated values.

MINIMUM LOAD
Main output requires a 10% minimum load for full output from auxiliaries. Use Option 08 if no minimum load is available for mains up to 500 watts. Singles require no minimum load.

RIPPLE & NOISE
1% or 100 mV, pk.-pk., 20 MHz bandwidth.

OPERATING TEMPERATURE
0-70°C. Derate 2.5%/°C above 50°C.

COOLING
A min. of 10 LFS* for models without internal fans directed over the unit for full rating. Two test locations on chassis rated for max. temperature of 90°C. 600 watt, 750 watt and 1000 watt models have built-in ball bearing fans.
*Linear feet/second.

TEMPERATURE COEFFICIENT
±0.02%/°C.

DYNAMIC RESPONSE
Peak transient less than ±2% or ±200 mV for step load change from 75% to 50% or 100% max. ratings.

RECOVERY TIME
Recovery within 1%. Main output - 200 microseconds. Auxiliary outputs - 500 microseconds.

SAFETY
Units meet UL 1950, CSA 22.2 No. 950, EN 60 950, IEC 950.

ISOLATION
Conforms to safety agency standards.

INPUT UNDERVOLTAGE
Protects against damage for undervoltage operation.

SOFT START
Units have soft start feature to protect critical components.

OVERVOLTAGE PROTECTION
Standard on all outputs.

REVERSE VOLTAGE PROTECTION
All outputs are protected up to load ratings.

OVERLOAD & SHORT CIRCUIT
Outputs protected by duty cycle current foldback circuit with automatic recovery. Standard auxiliaries have additional back-up fuse protection. Options 04 and 16 have square current limiting with automatic recovery when overload is removed.

THERMAL SHUTDOWN
Circuit cuts off supply in case of local over temperature. Units reset automatically when temperature returns to normal.

FAN OUTPUT
Nominal 12 VDC @ 12 watts maximum.

INHIBIT
TTL compatible system inhibit provided. Option 16 has individual output inhibit.

REMOTE SENSING
On all outputs except standard and 04 Option outputs 75 watts or less.

SHOCK & VIBRATION
Shock per MIL-STD 810-E Method 516.4, Procedure I. Vibration per MIL-STD 810-E Method 514.4, Category 1, Procedure I.

MECHANICAL

CASE	SERIES	WATTS	H	x	W	x	L
1	FT	400W/500W	2.50"	x	4.93"	x	8.00"
3	FT	600W	2.56"	x	5.08"	x	10.03"
4	FS	600W	2.56"	x	5.08"	x	11.00"
5	FT	750W	2.63"	x	5.20"	x	10.03"
6	FS	750W	2.63"	x	5.20"	x	11.63"
7	FS	1000W	2.56"	x	7.13"	x	11.63"

OPTIONS

POWER FAIL MONITOR
Optional circuit provides isolated TTL and VME/VXI compatible ACFAIL signal providing 4 milliseconds warning before main output drops by 5% after an input failure. A SYSRESET signal following VME timing requirements is provided when an N module is used as a main output. Both logic signal outputs can sink current per the VME specification.

REDUNDANCY
Optional Or-ing diodes for hot pluggable N+1 redundant operation. For FT Series 500 watt & 750 watt models with 1-4 outputs. Main output current limited to 100 amps. Remaining outputs 16 amps max.

CURRENT LIMIT
Option provides on all outputs:
- Square current limit with auto recovery.
- Wireless droop current share for parallel or N+1 redundant operation.

ZERO PRELOAD
Optional circuit removes need for preload on main output up to 500 watts.

ENHANCED
Option provides on all outputs:
- Square current limit with auto recovery.
- Single wire active current share for parallel or N+1 redundant operation.
- DC output good logic signal with LED indicator.
- Logic inhibit.
- Nominal 5V bias.
- Margining.

END FAN COVER
Optional cover with brushless DC ball bearing end fan which provides the required air flow for full rating.

TOP FAN COVER
Same as above with fan cover mounted on top of the power supply.

ACCESSORIES
RA50 and RA75 Series 2U high rack assemblies provide hot pluggable interface and hold up to 3 FT Series 500 watt or 750 watt units respectively.

Specifications subject to change without notice.

Deltron inc. POWER PRODUCTS

290 WISSAHICKON AVENUE, P.O. BOX 1369, NORTH WALES, PA 19454
PHONE: 215-699-9261 • FAX: 215-699-2310 • TOLL FREE: 1-800-523-2332
E-MAIL: sales@deltroninc.com • VISIT OUR WEB SITE: www.deltroninc.com

a man is known by the company he seeks out to help him design next-to-impossible products with sophisticated memory technologies like PC'00 and Rambus. And when he discovers Celestica,

he keeps it to himself.

With the right design partner, even your most outrageous, most advanced, "they-said-it-couldn't-be-done" ideas can beat the competition to market. Which is why so many of the world's leading OEMs would prefer to keep Celestica their little secret.

For 10 years we've been working with the biggest names in technology to design and build solutions that make cutting-edge technology—well, cutting edge. In the process, we've acquired perhaps the broadest range of memory manufacturing experience in the industry, from high-volume, industry-standard modules to highly customized, one-of-a-kind solutions.

We've also invested millions in testing equipment. Our two new Advantest® T5581 testers, for example, deliver high throughput while testing modules at the higher speeds demanded by today's technologies—which is how we test every module we build. (We thought you'd like to know that.)

Our connections are no small potatoes, either: Our memory for the latest Pentium® II processor–based systems and our PC100 memory are already on the market. And plans for Rambus RIMM modules and DDR memory are well under way.

So call us at **1-888-899-9998** and ask for document #7123. We'll send you a copy of "Breaking the Speed Limit: PC100 Memory" with a list of our latest Intel Pentium II–compatible memory upgrades. Or look for it at www.celestica.com/memory/100mhz.html. Because the secret to making sure your designs become great products is often in the company you keep.

www.celestica.com

ALLIED ELECTRONICS EBV ELECTRONICS HAMILTON HALLMARK Insight Pioneer TIME ELECTRONICS

CELESTICA

READER SERVICE 102

All the LCD features you need for outstanding FA systems

Factory environments vary widely. That's why NEC TFT LCD screens let you pick the optimum features for your application. Features include a 12.1" size, 800 x 600 resolution, ultra-wide viewing angle and high luminance. Touch-sensor panels are attachable.

Whatever your requirements for FA systems, we have a TFT LCD screen that will make your system look its best. For further information, contact NEC today.

Features	Large screen High luminance	High resolution	Ultra-wide viewing angle	High luminance Wide viewing angle	
Model number	**NL8060AC31-12**	**NL8060AC26-11**	**NL6448AC33-24**	**NL6448AC33-27**	**NL6448AC33-18**
Screen	12.1"	10.4"	10.4"	10.4"	10.4"
Pixel numbers	800 x 600	800 x 600	640 x 480	640 x 480	640 x 480
Display colors	262,144	262,144	262,144	262,144	262,144
Luminance	250cd/m² typ.	190cd/m² typ.	190cd/m² typ.	250cd/m² typ.	200cd/m² typ.
Viewing angle	Up 35°/down 55° Right/left ±60°	Up 20°/down 45° Right/left ±45°	Up/down ±80° Right/left ±80°	Up 55°/down 40° Right/left ±60°	Up 30°/down 20° Right/left ±45°

Operating temperature: 0°C to +50°C A backlight inverter is attached to all models.

The right components to build your reputation

On the Internet at http://www.ic.nec.co.jp/compo/lcd/index_e.html

For fast answers, call us at: **USA** Tel:1-800-366-9782.Fax:1-800-729-9288. **GERMANY** Tel:0211-650302.Fax:0211-6503490. **THE NETHERLANDS** Tel:040-445-845.Fax:040-444-580. **SWEDEN** Tel:08-638-0820.Fax:08-638-0388. **FRANCE** Tel:1-3067-5800. Fax:1-3067-5899. **SPAIN** Tel:1-504-2787.Fax:1-504-2860. **ITALY** Tel:02-667541. Fax:02-66754299. **UK** Tel:1908-691133.Fax:1908-670290. **HONG KONG** Tel:2886-9318.Fax:2886-9022. **TAIWAN** Tel:02-719-2377.Fax:02-719-5951. **KOREA** Tel:02-551-0450.Fax:02-551-0451. **SINGAPORE** Tel:253-8311.Fax:250-3583. **AUSTRALIA** Tel:03-8878012.Fax:03-8878014. **JAPAN** Tel:03-3798-6148.Fax:03-3798-6149.

just imagine

NEC MULTIMEDIA

NEC

READER SERVICE 121

Embedded Operating Systems Face Greater Productivity Demands

Customizable Off-The-Shelf Software And Integrated Networking Solutions Speed Time-To-Market For Embedded Systems.

Loren Werner

SPECIAL REPORT

Converging market forces, evolving technologies, and new paradigms for creating application software inspire designers to consider issues beyond operating system (OS) compactness, and productivity tool capabilities when developing embedded systems. Mounting pressure to implement ever more functionality in software, made possible by increasingly powerful, cost-effective microprocessors, fuels "feature wars" among segments of the embedded systems marketplace, particularly in consumer electronics. Shrinking market windows for each generation of consumer electronics products force embedded systems designers to bring more capable products to market under stringent time constraints. Today, the consequences of errors in software development that result in time-to-market delays may have enterprise-wide effects, whose impact can cost millions of dollars in lost revenues, or even drive companies out of business.

Art Courtesy: Bombadier Inc.

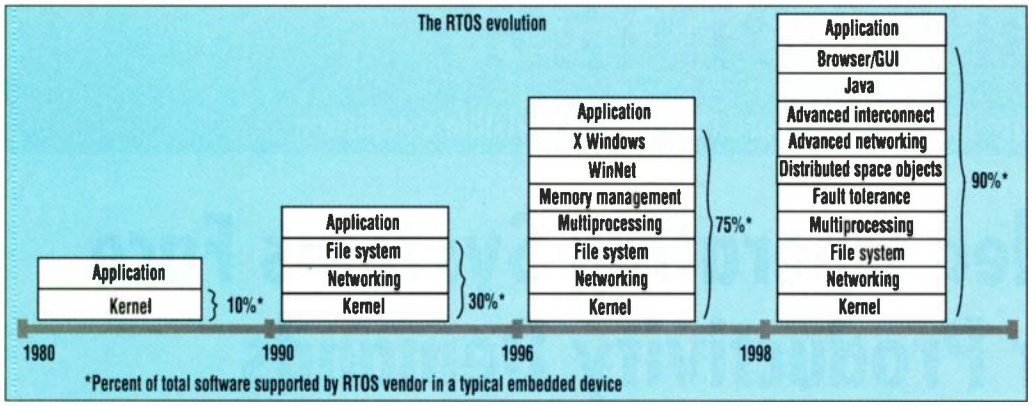
Quest For Standards

No resolution appears forthcoming that will address the industry split between OSs based on proprietary application programming interfaces (APIs), and those with open system architectures. Early movement toward some industry-specific standardization has begun among companies whose products depend upon embedded systems. Cooperative meetings are being held between leading companies, such as the Wireless Application Protocol (WAP) Forum, originally founded by Nokia, Ericsson, Motorola, and Unwired Planet. They were joined in June by RTOS vendor Geoworks, a supplier of smart-phone software. Similar meetings among leading consumer electronics manufacturers seeking to develop standards within their industry are underway.

New Paradigms

Market desire for increased productivity and standards has raised expectations over the level of functionality and integration delivered by embedded OSs and software development tools suppliers *(Fig. 1)*. Chief among the paradigm shifts for embedded systems is the transition to large software development teams with hundreds, or even thousands, of programmers. They may be spread across several continents, working on joint projects between major multinational corporations. Large design groups must evaluate such issues as the choice of appropriate hardware platforms, embedded OSs, development/debugging tools, and vendor service and support, to optimize application software productivity, reliability, and overall speed of system integration.

Today, products using embedded systems range from resource-constrained and price-sensitive products using 4-, 8-, and 16-bit processors, to robust programs that may contain millions of lines of code, im-



1. Increasing demand by designers for greater functionality drives on-going expansion of operating-system capabilities in off-the-shelf RTOS products. (Courtesy: Wind River Systems)

plemented on powerful 32-bit processors, in memory-rich environments. Embedded OSs are also used in advanced surveillance systems like the CL-327 Guardian Vertical Take-Off and Landing (VTOL) Unmanned Aerial Vehicle (UAV) from Bombadier Inc. *(see the opening illustration)*. The system's flight-control software has been debugged and optimized by Cygnus Solutions' GNUPro Toolkit for Windows NT.

Although home-grown, real-time executives and very-lean, real-time OS (RTOS) kernels still account for the lion's share of applications built with 4-, 8-, and 16-bit processors, some highly scaleable, off-the-shelf products play effectively under tight design constraints. In a 16-bit automotive controller used by General Motors, for example, Wind River's WindStream, an engineered subset of the company's VxWorks RTOS, runs along with user application code in just 40 kbytes. Forth Inc. reports its compact Forth language runs in a real-world multitasking application, on an 8-bit 8051 processor.

Shipments of 4-bit processors hit an all-time high in 1997, and industry demand for low-end devices shows no indication of diminishing. The automotive industry alone, producing 40 million cars annually that typically incorporate four major microprocessors and upwards of a dozen low-end chips each, consumes about one-half billion low-end processors annually.

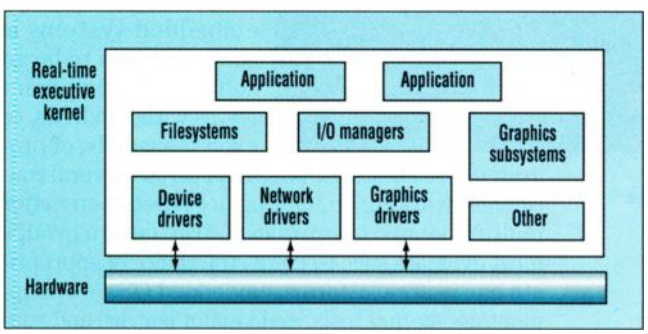
While demand for low-end devices remains strong, it's high-end microprocessors that are reshaping the design of embedded systems. Competitive pressure to span the broadening range of processors available, from low-end chips to high-end, 32- and 64-bit devices (with 128-bit offerings coming), influences offerings from RTOS vendors. While high-end design environments tend to reduce emphasis on OS compactness, RTOS product features move closer together as competing vendors strive for a "lean, highly-modular, feature-rich" model. Significant differences remain between OSs in modularity, proprietary APIs versus open-system architecture, interrupt handling, available development tools, target processor support, and hardware memory protection.

Unique OS architectures, vertical market-specific capabilities, and OS vendor focus within specialized markets, are contributing to the relative suitability of different OSs for particular applications. Designers in the smart-phone market, for example, might benefit from the specialized capabilities Geoworks incorporates into its GEOS-SC OS. These include hooks to facilitate graceful recovery from lost data-transmission connections when sending e-mail, which may occur when wireless phone users drive through tunnels.

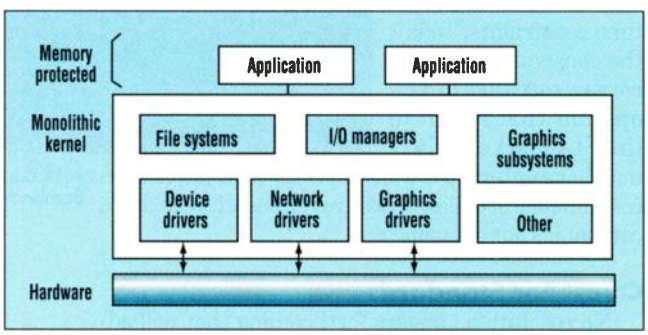
Memory Protection

The need for hardware memory protection to facilitate software development for large, complex programming tasks, underscores one significant, differentiating characteristic between RTOSs. Although real-time executives and OSs, which do not support hardware memory protection, remain suitable for applications in which code and OS run together in global address space, they depend entirely on software mapping to lay out memory space, and such software protocols as mutexes to avoid memory corruption *(Fig. 2)*.

Programming schemes like these are



2. Real-time executives provide no memory protection for multithreaded executable code. All processes and operating-system components run unprotected in the kernel mode. As a result, a failure (like a corrupted pointer) in any kernel component causes the system to crash or become unstable. The only way to recover is to reboot. (Courtesy: QNX Software Systems Ltd.)



3. Under a monolithic kernel architecture, MMU-based protection for all application processes running in the user mode prevents their memory space from being overwritten. But, a significant number of operating-system components and system drivers still run unprotected in the kernel mode. The likelihood of kernel faults increases as the amount of code running in the kernel increases. (Courtesy: QNX Software Systems Ltd.)

Vicor Releases The 48 Volt Family.

48 Vdc Input Family

Designed for communications and other distributed power systems

24 New Modules

2nd Generation DC-DC Converters

8 Outputs

2V, 3.3V, 5V, 12V, 15V, 24V, 28V, 48V

3 Package Sizes

Maxi—4.6 x 2.2 x 0.5 in
Mini—2.28 x 2.2 x 0.5 in
Micro—2.28 x 1.45 x 0.5 in

50-500 Watts

Power densities up to 100W/in³

Available From Stock

Call 800-735-6200 now to order!

2nd Generation

VICOR

Component Solutions For Your Power System

25 Frontage Road, Andover, MA 01810 Tel: 978 470 2900 • Fax: 978 475 6715

READER SERVICE 134

w w w . v i c r . c o m

vulnerable to system-wide crashes from a variety of conditions. These include a single errant pointer, accidental data-structure corruption, or unintentionally modifying code regions. The vulnerability of non-memory-protected coding schemes makes them prescriptions for disaster, where large software development teams are tasked with creating complex applications. Hardware-based memory protection provides the appropriate alternative.

While most RTOS vendors now offer memory protection, not all provide the same degree of support for the processor-based memory management unit (MMU). In particular, some OSs only perform hardware allocation of physical memory to different regions. More complete OS MMU support, like the Reliable Processing Environment of the LynxOS from Lynx Real-Time Systems, facilitates virtual addressing that translates logical addresses to the physical address space. Furthermore, many real-time OSs do not implement runtime memory protection for both application-level processes and OS components. This would be done to avoid performance degradation due to MMU-induced overhead.

In contrast to the real-time executive architecture shown in Figure 2, the monolithic kernel architecture of many real-time OSs separates OS functions within the kernel from application code outside the kernel mode *(Fig. 3)*. While application code benefits from MMU protection under this architecture, drivers and other system elements that run in the kernel mode remain in what is essentially a global address space. They also are subject to kernel faults, which can cause system crashes.

OSs built around microkernel architectures, like QNX from QNX Software Systems Ltd., implement only core services in the kernel *(Fig. 4)*. QNX provides such higher-level OS services as file system, device I/O, and networking, through optional processes running in the protected mode, along with user application code *(Fig. 5)*.

Reliability

Hardware memory-protection support plays one key role in the vital issue of how the OS supports reliability in embedded systems. While the need to select an embedded OS with a demon-

Companies Supplying Operating Systems, Tools, Or Integrated Solutions For Embedded Systems

Accelerated Technology Inc.
720 Oak Circle Dr. East
Mobile, AL 36609
(334) 661-5770
www.atinucleus.com
CIRCLE 452

Agranat Systems Inc.
1345 Main St.
Waltham, MA 02154
(781) 893-7868
www.agranat.com
CIRCLE 453

Annasoft Systems
11838 Bernardo Plaza Ct.
San Diego, CA 92128
(619) 674-6155
www.annasoft.com
CIRCLE 454

BSQUARE Corp.
Delphi Bldg.
3633 136th Pl. SE, Ste. 100
Bellevue, WA 98006
(425) 519-5900
www.bsquare.com
CIRCLE 455

Bytebos Integrated Systems
12032 Broadway Terr.
Oakland CA 94611
(510) 658-7797
www.bytebos.com
CIRCLE 456

CAD-UL Inc.
6330-1 E. Thomas Rd., #100
Scottsdale, AZ 85251
(602) 945-8188
www.cadul.com
CIRCLE 457

Chorus System [now Sun Microsystems' Embedded Systems Software Group (ESSG)]
1999 S. Bascom Ave.,
Ste. 400
Campbell, CA 95008
(408) 879-4100
www.chorus.com
CIRCLE 458

CMX Co.
680 Worcester Rd.
Framingham, MA 01702
(508) 872-7675
www.cmx.com
CIRCLE 459

Cygnus Solutions
1325 Chesapeake Terr.
Sunnyvale, CA 94089
(408) 542-9600
www.cygnus.com
CIRCLE 460

Diab Data Inc.
323 Vintage Park Dr.
Foster City, CA 94404
(650) 571-1700
www.diabdata.com
CIRCLE 461

Embedded System Products Inc.
10450 Stancliff, Ste. 110
Houston, TX 77099
(281) 561-9990
www.rtxc.com
CIRCLE 462

Enea OSE Systems AB
P.O. Box 232,
Nytorpsvägen 5B
SE-183 23 Täby, Sweden
+46 8 638 50 00
In U.S.: Enea OSE Systems Inc.
5949 Sherry Ln., Ste. 1710
Dallas, TX 75225
(214) 346-9339
www.enea.com
CIRCLE 463

Eyring Corp.
6918 S. 185 West
Midvale, UT 84047
(801) 561-1111
www.eyring.com
CIRCLE 464

Forth Inc.
111 N. Sepulveda Blvd.
Manhattan Beach, CA 90266
(310) 372-8493
www.forth.com
CIRCLE 465

Geoworks
960 Atlantic Ave.
Alameda, CA 94501
(510) 814-1660
www.geoworks.com
CIRCLE 466

Green Hills Software Inc.
30 W. Sola St.
Santa Barbara, CA 93101
(805) 965-6044
www.ghs.com
CIRCLE 467

Hewlett-Packard Co.
3000 Hanover St.
Palo Alto, CA 94304-1185
(650) 857-1501
www.hpconnect.com/embeddevm
CIRCLE 568

Integrated Systems Inc.
201 Moffett Park Dr.
Sunnyvale, CA 94089
(408) 542-1500
www.isi.com
CIRCLE 569

Intrinsyc Software Inc.
550 Kirkland Way, Ste. 205
Kirkland, WA 98033
(604) 801-6461
www.intrinsyc.com
CIRCLE 470

JMI Software Systems Inc.
PO Box 481, 904 Sheble Ln.
Spring House, PA 19477
(215) 628-0840
www.jmi.com
CIRCLE 471

Kadak Products
206-1847 W. Broadway Ave.
Vancouver, B.C., Canada
V6J 1Y5
(604) 734-2796
www.kadak.com
CIRCLE 472

(continued on page 56)

INTEL, MICROSOFT & VENTURCOM JOIN FORCES WITH ZIATECH.

SEPTEMBER

3RD • DALLAS

15TH • PARIS

17TH • MUNICH

■

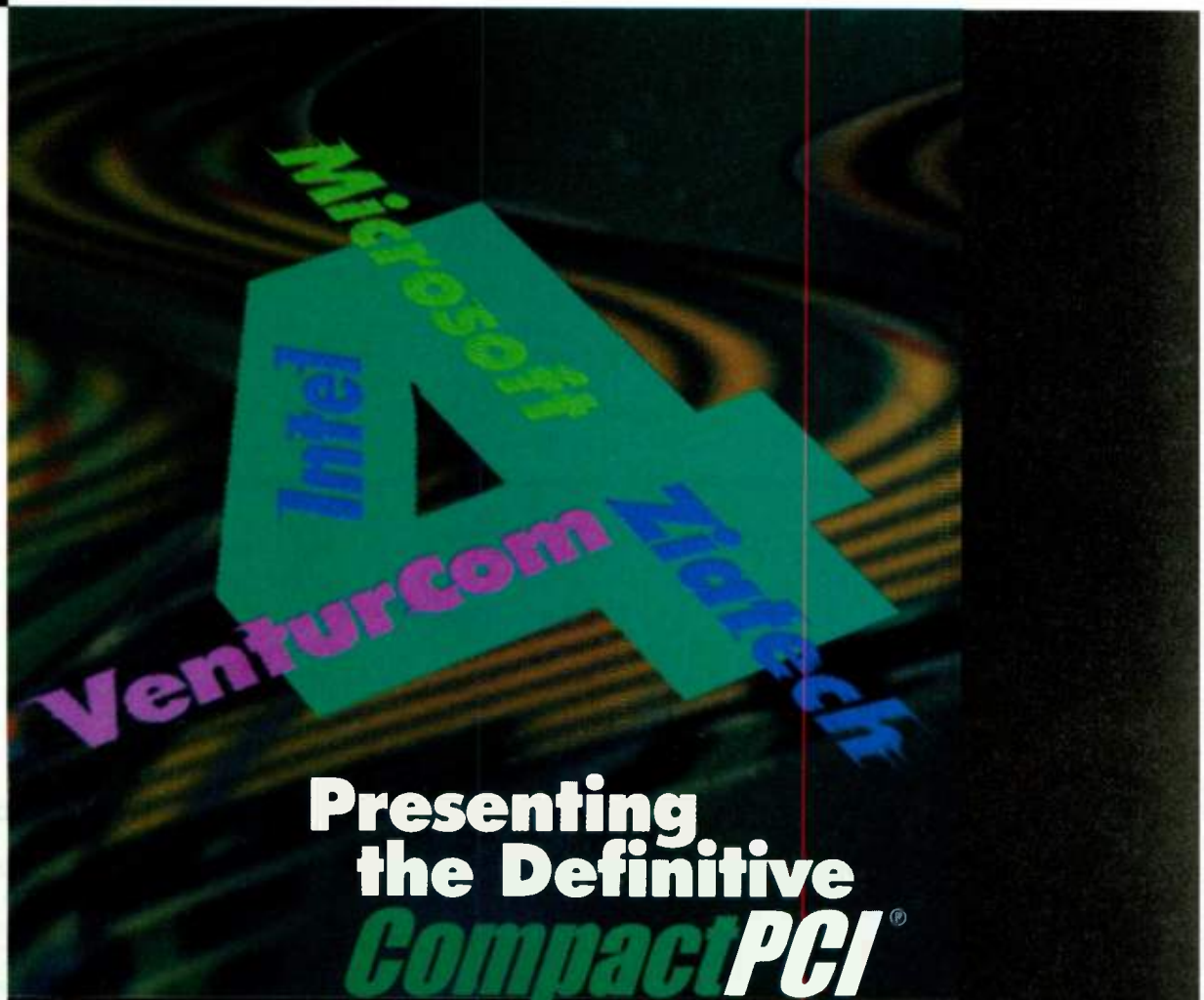
OCTOBER

15TH • SAN DIEGO

■

DECEMBER

2ND • TOKYO



Presenting the Definitive CompactPCI® Seminar.

**DON'T MISS IT —
COME AND GET THE INSIDE TRACK!**

Get up-to-the-minute information on emerging apps from the four major movers and shapers of CompactPCI and its future. This full-day, in-depth seminar is an unprecedented event in the rapid evolution of this exciting bus architecture.

Attendance is limited, so act now. Visit our website today for information and reservations.

805-541-0488; Fax: 805-541-5088
E-mail: info@ziatech.com
Web: http://www.ziatech.com

ZIATECH CORPORATION
The Original CompactPCI Company

READER SERVICE 139

strated track record of reliability is self-evident in such life-critical applications as avionics and medical instrumentation, it's importance in mission-critical and highly-available applications such as communications switches, factory control, and even consumer electronics, should not be overlooked. While system failures in consumer electronics products may not put lives at risk, consumer intolerance of unreliable products can put the livelihood of companies at significant risk. Overall system reliability often becomes a part of the design requirement for embedded systems in such highly-available and fault-tolerant applications as those associated with infrastructure equipment in telecom, avionics and industrial control.

Steps taken by OS manufacturers to meet such application requirements vary. High levels of reliability have been achieved under a variety of different OS architectures. The effectiveness of the QNX microkernel architecture is demonstrated in its performance, running one Olin chemical factory non-stop for eight years, without a single shutdown for code maintenance. Code maintenance has been performed on the Olin control application over the last eight years on a real-time, hot-swap basis.

Many OSs deliver the high levels of reliability required for applications like avionics and air traffic control systems. All such systems for domestic use are subject to extensive FAA testing and certification before going into service. Typically, an OS does not receive such testing by itself, but undergoes FAA testing as part of a system intended for avionics/air traffic control.

Microtec, for example, has taken its VRTXsa OS a step further in the FAA certification process by putting it through the testing procedure on a standalone basis. The company's VRTXsa multitasking kernel, run-time library, and BSP device drivers and initialization software have all passed the FAA's most stringent level of testing, and have received FAA Level A certification—the highest level possible.

Software Productivity

As time-to-market pressures decrease developers' tolerance of hurdles to software productivity, vendors place increasing emphasis on providing solutions to promote faster product devel-

(continued from page 54)

Lynx Real-Time Systems Inc.
2239 Samaritan Dr.
San Jose, CA 95124
(408) 879-3900
www.lynx.com
CIRCLE 473

Metrowerks Inc.
9801 Metric Blvd., Ste. 100
Austin, TX 78758
(512) 873-4700
www.metrowerks.com
CIRCLE 474

Microsoft Corp.
One Microsoft Way
Redmond, WA 98052
(425) 882-8080
www.microsoft.com
CIRCLE 475

Microtec Division of Mentor Graphics Corp.
8005 S.W. Boeckman Rd.
Wilsonville, OR 97070
(503) 685-7000
www.mentorg.com/microtec
CIRCLE 476

Microware Systems Corp.
1500 N.W. 118th St.
Des Moines, IA 50325
(515) 223-8000
www.microware.com
CIRCLE 477

Motorola Inc.
6501 William Cannon Dr.
Austin, TX 78735
(800) 262-5486
www.mot.com/rtek
CIRCLE 478

NewMonics Inc.
2625 N. Loop Dr., Ste. 2120
Ames, IA 50010
(515) 296-0897
www.newmonics.com
CIRCLE 479

On Time
88 Christian Ave.
Setauket, NY 11733
(516) 689-6654
www.on-time.com
CIRCLE 480

Osicom Technologies Inc.
9020 Junction Dr.
Annapolis Junction, MD 20701
(888) OSICOM8
www.osicom.com
CIRCLE 481

Phar Lap Software
60 Aberdeen Ave.
Cambridge, MA 02138
(617) 661-1510
www.pharlap.com
CIRCLE 482

Phoenix Technologies Ltd.
411 E. Plumeria Dr.
San Jose, CA 95134
(408) 570-1000
www.phoenix.com/pico
CIRCLE 483

Precise Software Technologies Inc.
106 E. Sixth St., Ste. 900
Austin, TX 78701
(800) 265-9833
www.psti.com
CIRCLE 484

Psion Software PLC
85 Frampton St.
London
NW8 8NQ
United Kingdom
+44 171 2081800
www.psion.com
CIRCLE 485

QNX Software Systems Ltd.
175 Terence Matthews Cr.
Kanata, Ontario, Canada
K2M 1W8
(613) 591-0931
www.qnx.com
CIRCLE 486

Radisys
5445 N.E. Dawson Creek Dr.
Hillsboro, OR 97124
(503) 615-1100
www.radisys.com
CIRCLE 487

Spyglass Inc.
1240 E. Diehl Rd.
Naperville, IL 60563
(630) 505-1010
www.spyglass.com
CIRCLE 488

STMicroelectronics (formerly SGS-THOMPSON)
10 Maguire Rd.
Lexington, MA 02421
(781) 861-2650
www.st.com
CIRCLE 489

Sun Microsystems Inc.
901 San Antonio Rd.
Palo Alto, CA 94303
(650) 960-1300
www.sun.com
CIRCLE 490

Tasking Inc.
333 Elm St.
Dedham, MA 02026-4530
(781) 320-9400
www.tasking.com
CIRCLE 491

Texas Instruments Santa Barbara (formerly Spectron Microsystems)
315 Bollay Dr.
Santa Barbara, CA 93117
(805) 968-5100
www.spectron.com
CIRCLE 492

Trillium Digital Systems Inc.
12100 Wilshire Blvd.,
Ste. 1800
Los Angeles, CA 90025-7118
(310) 442-9222
www.trillium.com
CIRCLE 493

U S Software
7175 N.W. Evergreen Pkwy,
Ste. 100
Hillsboro, OR 97124
(503) 844-6614
www.ussw.com
CIRCLE 494

Wind River Systems
1010 Atlantic Ave.
Alameda, CA 94501
(510) 748-4100
www.wrs.com
CIRCLE 495

The RTOS that delivers:

With our advanced MMU-protected OS, prototyping, debugging, testing – everything – takes less time. So you have more time to innovate. Visit www.qnx.com/literature for a free white paper.

Quick. What's the one thing that makes an RTOS worthy of the term "mission critical"? The engineers at COBE® BCT™ can tell you: **Architecture**.

Architecture? That's right. By taking advantage of the advanced microkernel architecture of the QNX® RTOS, the COBE Trima™ development team created a next-generation blood collection system that not only meets, but exceeds rigorous safety requirements. Better yet, QNX architecture accelerated the team's design cycles dramatically. And gave them more time to innovate.

The result? COBE BCT delivered ahead of schedule — with a system so advanced it has an expected life cycle of over 10 years. Mission: accomplished.

Free QNX eval system!
Call 800 676-0566 ext. 2267

www.qnx.com

QNX®
The Leading Realtime OS for PCs
now multiplatform

READER SERVICE 125

opment. These include various approaches to powerful, integrated development tool sets; complete pre-integrated packages for such services as networking and connectivity; vertical, market-specific, customizable applications software; and full-blown design/prototyping services.

Examples include Wind River's Tornado tool set, integrated with the company's VxWorks OS, and the pRISM+ integrated tool environment for the pSOS+ OS from Integrated Systems Inc. (ISI). ISI provides access to third-party tool solutions to enhance pRISM+ through the Common Object Request Broker Architecture (CORBA) standard. pRISM+ also provides a consistent user interface across the broad range of compilers ISI supports. ISI evaluates industry compiler offerings, and supports those which provide the tightest, most efficient code for each target microprocessor.

Attention to relevant details in application language support can play an important role in promoting software development productivity, and run-time code reliability under real-time conditions. ISI notes that many RTOS vendors support only standard libraries supplied by compiler vendors for C and C++ application codes. ISI augments support for standard libraries by providing reentrant versions. With reentrant libraries, code operations that are interrupted in mid-execution can return to execution without suffering data corruption. ISI claims that use of its reentrant libraries promotes code reliability and productive code development by preventing very obscure, difficult to track bugs in embedded applications.

Suppliers of compilers and development tools seek to shorten access to tools for new chips through close relationships with semiconductor manufacturers. Chip makers, RTOS vendors, and tool makers frequently cooperate early in new chip design cycles to promote effective alignment between chip capabilities and software support. This sometimes creates software simulators that allow code development for new target processors long before the chips are ready for delivery.

Increasingly, software vendors, such as Cygnus Solutions, speed access to development software for new chips through porting agreements. These allow chip manufacturers to ship licensed software with their semiconductor products. Cygnus Solutions specializes in supplying highly optimized GNU compilers and associated development/debug tools.

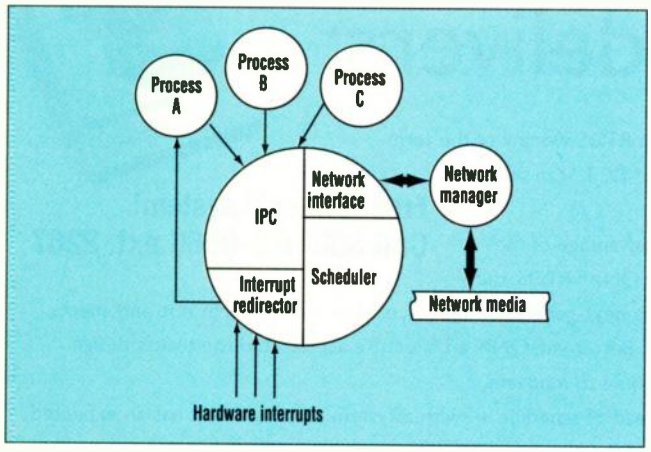
Customizable Solutions

Another class of solutions that speeds embedded product development involves integration of software functions onto a chip. This technique saves developers code generation and integration time. Some of these products are targeted for particular markets, such as STMicroelectronics' STPC multimedia, "PC on a chip." The chip is designed to provide multimedia capabilities for such high-volume digital consumer devices as set-top boxes, game consoles, and web-enabled TVs. The STPC integrates a high-performance, x86 processor; graphics subsystem; video pipeline; comprehensive core logic with support for PCI, ISA, IDE, DMA; and interrupt controllers.

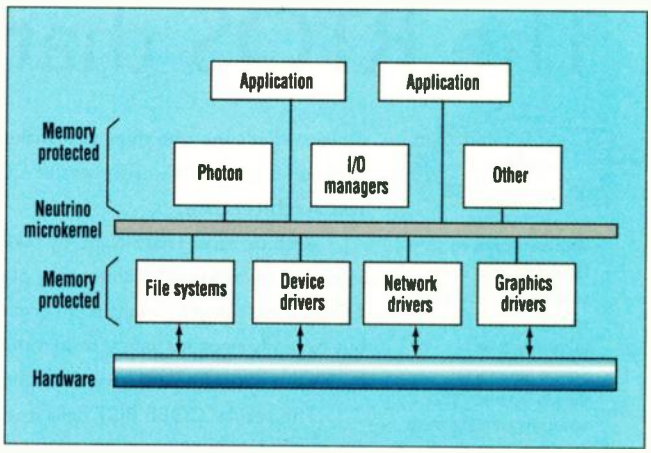
Other solutions, such as the NET+ARM offering from Osicom, provide integration of the processor, RTOS, and a full suite of networking protocols and applications. These are necessary to enable networking for the rapidly-emerging classes of such web-manageable devices as office equipment (printers, photocopiers, and fax machines), and industrial switches *(Fig. 6)*.

While shrink-wrapped software solutions are nowhere near a reality for embedded systems, customizable, off-the-shelf software is appearing from Spyglass Inc. and Agranat Systems Inc., among others. They provide embedded web browsers and embedded web microservers. Designers can enable Internet connectivity and web-manageable products more quickly by customizing and integrating products like these into their systems, than by creating home-grown equivalents.

Another path to rapid product development involves accessing design, consulting, software engineering, and initial product prototyping services, available from a number of RTOS vendors. Last March's merger between Annasoft Systems and Intrinsyc Software Inc., for example, provides con-



4. The QNX microkernel implements four services: interprocess communication, low-level network communication, process scheduling, and interrupt dispatching. There are a few kernel calls associated with these services. In total, these functions occupy roughly 12,000 lines of code, and provide the functionality and performance of a real-time executive. (Courtesy: QNX Software Systems Ltd.)



5. Under a microkernel architecture that implements full memory protection at run time, very little code is run in the kernel mode that could cause it to fail. This architecture allows individual processes and operating-system components to be started and stopped dynamically, and updated or changed on the fly, without having to bring the system down. (Courtesy: QNX Software Systems Ltd.)

Boldly Go Where No Designer Has Gone Before.

Push Designs To The Limit With Microchip. The Only Complete 8-bit RISC MCU Solution.

Welcome to Planet Microchip. Here you'll find the ultimate embedded control solution: performance and flexibility, extensive microperipherals, world-class applications engineering and development tools support, a broad range of pin-counts from 8 to 80 and virtually zero lead time—all at down-to-earth prices. Climb aboard and we'll take you well *beyond* the final frontier where you'll discover the limitless possibilities of PICmicro™ based designs. Call or visit our web site to request your FREE Planet Microchip PowerPak.

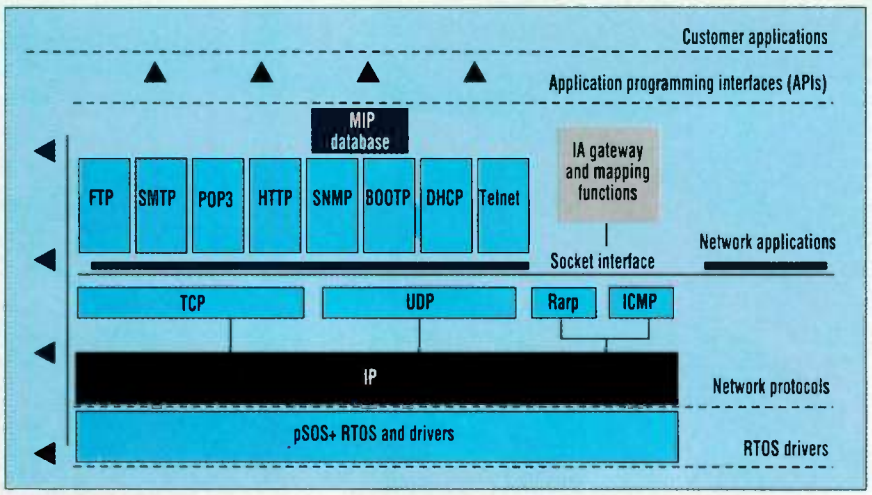
1-888-MCU-MCHP ✸ **1-888-628-6247**

PICmicro MCU Features	Family	Program Memory (words)	RAM (bytes)	Pin Count	I/O	No. of Products	Replaces
OTP/ROM/FLASH/EEPROM Program Memory, In-Circuit Serial Programming™ ADC, USART, SPI/I²C Timers/Counters, Capture/Compare/PWM, Comparators, EEPROM Data, Internal OSC, LCD Driver, Brown-Out Detect	PIC12CXX PIC16C5X PIC16C55X PIC16C6X PIC16C7XX	512 x 12/14 1K x 12/14 2K x 12/14 4K x 14	25–368	8, 14 18, 20, 28	6–22	40	68HC05 8051 Z8, ST6 COP8
	PIC16C6X PIC16C7XX PIC16F8X PIC16C9XX	512 x 14 1K x 14 2K x 14 4K x 14 8K x 14	80–368	18, 20, 28, 40, 44, 64, 68	13–52	33	68HC05 68HC08 80C51 ST6, ST7 COP8
	PIC17C4X PIC17C7XX	2K x 16 4K x 16 8K x 16 16K x 16	232–902	40, 44 64, 68 80, 84	33–66	10	H8, 68HC11 68HC16, ST9 MCS251 80C51XA

Explore the Universe of Embedded Control at www.microchip.com

MICROCHIP
The Embedded Control Solutions Company®

READER SERVICE 118



6. The NET+ARM-12, from Osicom Technologies, provides an integrated solution for enabling Ethernet/Internet connections in embedded systems. It combines a 12-MIPS ARM microprocessor, the pSOS+ RTOS from Integrated Systems, and networking software designed for loading into user-supplied RAM and/or ROM. (Courtesy: Osicom Technologies Inc.)

sulting engineering services addressing every critical phase of the embedded systems design process, from platform-level integration (including hardware design and packaging), through application-level integration, for projects based on Windows CE and NT.

Evaluating the cost-performance provided by services like these requires weighing their fees against reducing time-to-market for new products. ISI Design Center (formerly Doctor Design) may offer special appeal to risk-sensitive companies. Among its comprehensive range of engineering consulting services, it offers risk reduction in such areas as test and verification, project management, cost containment, resolving performance and technical challenges, and addressing regulatory/environmental concerns.

Embedded Java

While enhanced software productivity through Java's "write-once, run-everywhere" ideal has not been achieved for embedded systems, progress toward a viable, embedded Java is underway at Sun Microsystems, Hewlett-Packard, and NewMonics Inc. Sun's measured approach to defining a stable, meaningful specification for a deterministic, real-time, embedded Java involves a comprehensive analysis of industry needs, as well as an in-depth review of how Java can be trimmed for embedded applications.

For those not content to wait for Sun, HP and NewMonics offer their own cleanroom virtual machines that support deterministic Java for embedded applications. HP's virtual machine, originally conceived for internal use in the company's embedded devices, is now commercially available. HP says its virtual machine supports the same kind of deterministic behavior available from C and C++. This makes it suitable for use as the primary implementation language for many classes of embedded real-time applications.

Similarly, NewMonics says its virtual machine for Java, called Portable Executive Reliable Control (PERC), also provides fully deterministic behavior. Both HP and NewMonics agree that further testing is in order to determine whether Java on their virtual machines will be speed-limited for some real-time applications.

While a fully viable form of embedded Java edges toward emergence, other methods to achieving portable code, such as the recent embedded C++ initiative, are being explored. Forth has also been used to create virtual machines that execute portable bytecode. One such application runs in Europay International's processor-independent Open Terminal Architecture (OTA) for smart-card terminals in Europe.

Opinions vary as to whether the real-time version of Windows CE, expected mid-year 1999, will give Microsoft the kind of dominance in the embedded market that the software giant has in the desktop market. Some established RTOS and tool vendors predict abject failure for Microsoft, while others foresee sweeping success. Many are hedging their bets by adding Windows CE to their product offerings while waiting to see where the chips fall.

Critics point to Microsoft's missing support infrastructure when it comes to addressing the specific needs of embedded systems designers. They also express doubts as to whether Windows CE will be sufficiently lean for embedded systems environments, or fast enough for hard, real-time applications.

On the other side of the question, Microsoft proponents see the Win32 API that underlies Windows CE, as a means to achieving code portability between applications for embedded systems. Microsoft supporters also view the 5,000,000 programmers familiar with Win32 as an attractive solution to scarce software development resources. But, independent software vendors made gun-shy by their experience with Microsoft in the desktop market may prove reluctant to develop applications for Windows CE.

Microsoft hopes to circumvent shortcomings due to the lack of support infrastructure by distributing Windows CE through established RTOS vendors. The company will rely on them to provide required consulting, service, and support to Windows CE customers. As for real-time performance for the coming version of Windows CE, Microsoft is targeting a sub-50-µs response time (on a Pentium 133), support for nested interrupts, semaphores, and 32 or more priority levels. Whether Microsoft will deliver all this in a package sufficiently modular to achieve the compact footprint required remains to be seen.

The entry of other industry giants, drawn by the huge potential of the embedded market could influence Microsoft's future in this arena. Some embedded OS vendors hint at possible alliances with major computer companies to champion their established, credible, RTOS technologies. If such alliances develop, the coming turf war could make things very interesting.

Loren Werner is a former trade journal editor who now provides marketing communications and writing services through his consulting company, TechSource, Phoenix, AZ. Werner obtained his BA degree from the University of California at Irvine.

"Microtek in-circuit emulators gave me more features for the best price."

You want to do it right, and meet project deadlines. That's not easy, especially when your debug environment includes RTOS and C++ support. And more hardware hides deeper inside silicon.

You can't escape these challenges, and neither can we. That's why we pack more features and interoperability into our emulators..

Only Microtek emulators offer integrated state analysis with clock-cycle time stamping – *a traditional logic analyzer feature* – which allows you to track down the cause for system crashes that's impossible for a software debugger to find. At the same time, we have integrated high-level source display... *the kind logic analyzers can only show with a complicated connection to the target, multiple tool interfaces and non-interactive, post-processed source display.*

You can quickly view executed code coverage from your emulator without a separate tool interface, and without instrumenting your code or maintaining separate builds. Plus, now you can run your Microtek emulator from any seat on the network.

No other emulator offers integrated state analysis. No other emulator offers our advanced trace and trigger system. No other emulator offers SWAT™ Software Analysis Tools.

While other so-called emulator companies are de-emphasizing their emulator business, we continue to build ours. This means you can choose the performance options you need – *from entry-level to the most advanced in the industry, all at competitive prices.*

MICROTEK
IN-CIRCUIT EMULATORS

1 (800) 886-7333

Phone: (503) 645-7333 Fax: (503) 629-8460
Email: info@microtekintl.com
www.microtekintl.com

READER SERVICE 112

Ask for our latest technical papers:

1. Using Microtek Emulators with WindRiver's Tornado™
2. How to Emulate a Single Target System on a Network
3. Instruction-Level Execution and Branch Code Coverage
4. Emulator Integrates Logic Analyzer State Analysis and High Level Trace
5. Mature, Cost-Effective In-Circuit Emulators for NT Workstations

FREE AppNotes

for the following processors:

Pentium® II
Pentium®
National NS486™
Intel486™
Intel386™ EX/CX/SX
Am186/188™
Intel 186/188
683xx/HC16
8051/52/251

Financing Options Available

Optical Interconnects Penetrate Local-Network Realm

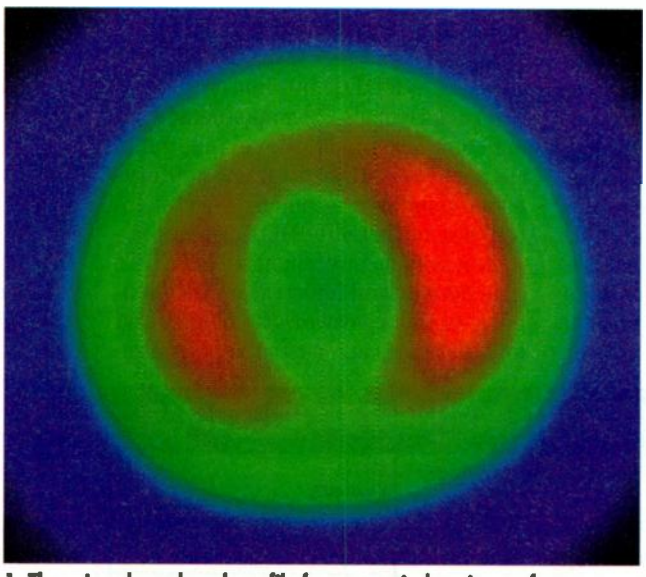
Thanks To Advances In Laser, Packaging, And Test Technology, Optical Interconnects Prepare To Give Moore's Law New Life.

TIM BOUR, Cielo Communications Inc., 325 Interlocken Pkwy., Bldg A, Broomfield, CO 80021; (303) 460-0700; fax (303) 466-0290; www.cieloinc.com.

The evolution of computer systems over the past two decades shows a tremendous increase in processing ability per square inch, as postulated by Moore's Law. However, a closer look at the progression of interconnection technologies shows growth trends that, while impressive, have not kept pace with processing capabilities. As a result, the movement of acres of data generated by high-speed processors has been hampered, making the interconnect a major bottleneck. To relieve it, systems and network designers are moving away from copper-based interconnects, with their inherently high capacitance, noise susceptibility, and relatively poor signal-loss/distance ratios, to more advanced, high-speed optical connections.

While copper links still carry the bulk of the load for workgroup-level networks, optical links are emerging as the preferred media for campus backbones, central-office networks, and WANs. These systems demand the low noise, faster transmission rates, zero crosstalk, and wide bandwidth that only optical systems can provide. Despite inherent advantages, the proliferation of optical connector technology has been slow, due to its relatively high cost of implementation. Recent advances in laser, packaging, and testing, however, are lowering this technology's cost premium, such that it is now penetrating both WANs and LANs.

As costs come down, technologies such as Gigabit Ethernet (GbE), which leverage existing Ethernet standards, are ideally positioned to provide the bridge between existing, copper-based, 10/100Base-T local networks and new, higher-bandwidth optical infrastructures. At the same time, fiber-based, high-speed data-storage networks, such as Fibre Channel, are rapidly being deployed to support enterprise-wide data warehousing strategies.

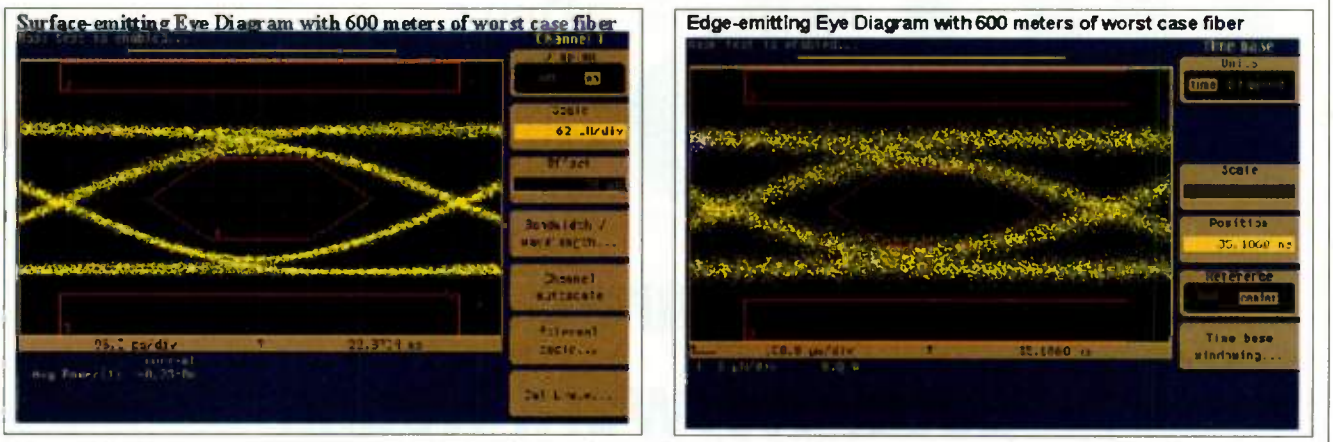


1. The unique laser-launch profile from a vertical-cavity, surface-emitting laser (VCSEL) shows a donut pattern of light. This eliminates the differential-mode delay effect that may occur when light is launched uniformly across worst-case multimode fiber. Launching the light in such a fashion eliminates smearing over distances as much as three times longer than broadly launched signals of the same output power.

Implementation Challenges

A major challenge to the effective implementation of these new, high-speed optical links will be the creation of cost-effective, robust, standards-based optical transceiver components that can support Gbit/s bandwidths. As the demand for gigabit optical links accelerates, system designers need access to readily available, high-volume supplies of reliable, electro-optical, physical-layer components.

These optical transceivers will spark the gigabit revolution in much the same way the availability of standard Ethernet physical-layer components (PHYs) helped fuel the ubiquitous deployments and falling cost curves of 10Base-T and 100Base-T over the past decade. However, the design and production of optical interconnects presents a totally new and unique set of problems. These are associated with the cost-effective production of gigabit-speed lasers using standard semiconductor processes, and the effective packaging and alignment of



2. To meet the rigorous specification requirements of gigabit-speed networks, every optical interconnect component must consistently produce an eye diagram that conforms to a predetermined eye-diagram mask. Using a "worst-case" fiber at 600 m, the vertical-cavity surface-emiting laser (VCSEL) still meets the conformance eye mask designed for Gigabit Ethernet (a). Under the same conditions, the edge-emitting CD eye diagram shows significant degradation in the eye-opening (b). At extreme degradation, the link integrity will be compromised.

these devices to optimally launch light into standard optical fiber.

The evolution of higher data rates and the migration toward optical links has created a need for greater flexibility in interconnect form factors. For instance, link distances and data rates in 10BaseT or 100Base-T links could typically be handled by a single type of physical-layer component, which could cost-effectively be soldered directly onto a system-level pc board, whether it's a network interface or a switch card.

But, the greater data rates required by optical gigabit links present network-configuration challenges that cannot always be cost-effectively resolved by a common interconnect or transmission methodology. For example, GbE links may be implemented either as 1000Base-SX links using less expensive, short-wavelength (850-nm) laser technology over multimode fiber, or as 1000Base-LX links using more expensive, long-wavelength (1300-nm) laser technology over multimode or singlemode fiber. Depending upon the fiber diameter used, 1000Base-SX can support distances up to 550 m on 50-µm multimode fiber, and up to 275 m on 62.5-µm multimode fiber. On the other hand, 1000Base-LX can support distances of 550 m on either 50- or 62.5-µm multimode fiber, and up to 5000 m on 9-µm single-mode fiber *(see the table)*.

Because long-wavelength transceivers for 1000Base-LX interconnects are inherently more expensive than short-wavelength, 1000Base-SX components, it's important to instill a higher degree of configuration flexibility into the deployment of optical transceivers. Along with the traditional 1 by 9 (1 row by 9 pins) solderable component form factor used throughout copper-based Ethernet and Fiber Distributed Data Interface (FDDI) implementations, GbE links can also be implemented using complete module-level pluggable transceivers based on the widely-adopted industry-standard Gigabit Interface Converter (GBIC) form factor.

Not only do interchangeable GBICs give network administrators the flexibility to tailor network topologies and link distances and costs to specific requirements, they also allow for subsequent network reconfiguration as needs change—without wholesale replacement or system-level investments.

Design Issues

The design and manufacture of cost-effective, optical interconnect solutions for use in Gbit/s GBICs, hinges on successfully meeting reliability and distance requirements of the GbE specifications. At the same time, companies need to drive down packaging, alignment, and test costs of these devices to support high-volume deployments.

Reliability and distance: The most critical factor impacting the reliable transport of optical signals over practical distances is differential mode delay (DMD), important because light traveling through multimode optical fibers tends to bounce through the fiber at different angles, depending upon its distance from the center of the fiber. This results in different propagation paths (modes) for different parts of the fiber. As a result, a signal launched across the entire fiber tends to "smear" as it goes through the fiber. In essence, the same signal is being simultaneously propagated down the fiber following different path lengths in the center than at the edges. Thus, a digital pulse of a given output power will tend to move toward a bell-shaped curve as the signal is smeared over a given distance.

Ideally, the fiber is constructed to compensate for this by allowing light travelling on the outside of the fiber to move at a higher velocity. In some fibers, however, construction is non-op-

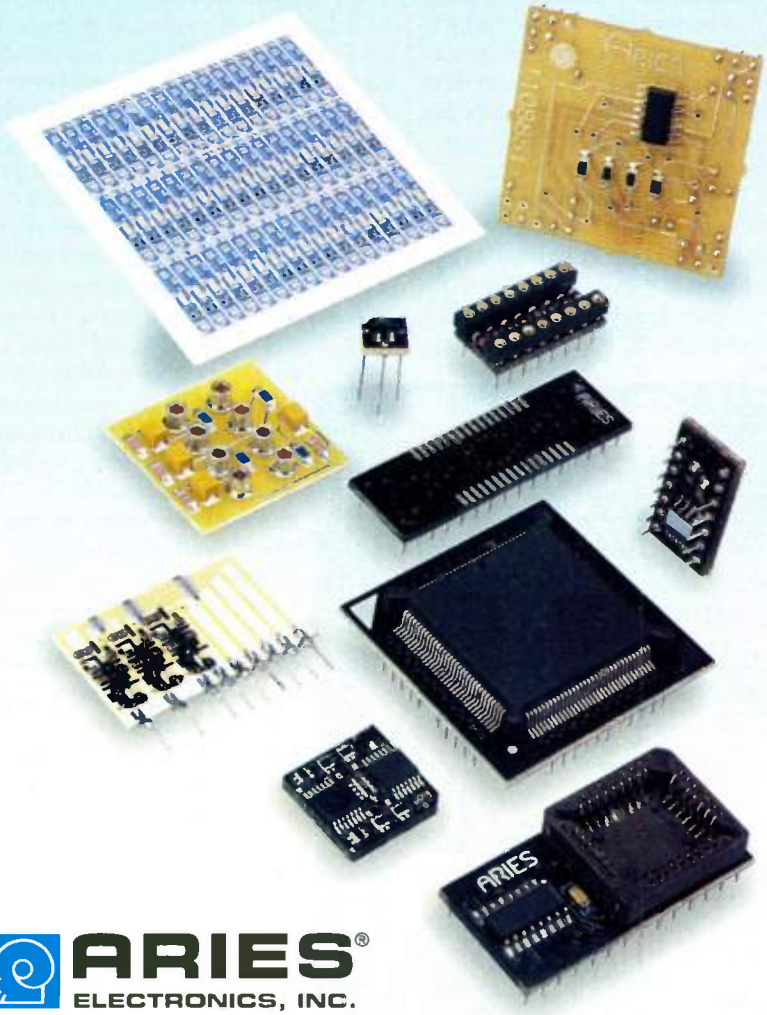
EVOLUTION OF NETWORK INTERCONNECT TECHNOLOGIES

Network standard	Data rate	Maximum distance per link	Media flexibility
Ethernet	10 Mbits/s	2 km	Soldered discrete components
Fast Ethernet	100 Mbits/s	2 km	Soldered 1 by 9 transceiver
FDDI	100 Mbits/s	2 km	Soldered 1 by 9 transceiver
Gigabit Ethernet 1000Base-SX	1.0 Gbit/s	550 m (multimode fiber)	Soldered 1 by 9 transceiver or pluggable GBIC transceivers
Gigabit Ethernet 1000Base-LX	1.0 Gbit/s	550 m (multimode fiber) 5 km (single-mode fiber)	Soldered 1 by 9 transceiver or pluggable GBIC transceivers

Relax... call Aries

Upgrades by Design, not Redesign...

Aries Correct-A-Chip™



Whoever said "the more things change, the more they stay the same" sure wasn't referring to *your* business! Change is what drives the business and it's also what can drive you crazy when it comes to designing new devices into your existing products.

That's precisely why Aries Correct-A-Chip™ technology is so popular with designers who are always looking to upgrade: it lets them (and you) take advantage of device enhancements *without* board rework, redesign or delays.

Change is good. With Correct-A-Chip, it's also easy!

With Correct-A-Chip, you can change from one footprint or package type to another, from surface mount to through-hole, from one pinout to another, from one...you get the picture. If there's a way to upgrade your product with a new chip, there's a Correct-A-Chip that lets you do it quickly and economically.

With Correct-A-Chip, you can even add additional componentry and circuitry while you upgrade to a new device – all in the same space! And, for even greater miniaturization and performance, Aries also provides fast-turn MCMs.

The Proof Awaits You

Correct-A-Chip isn't magic. It just works like it. Want proof? Visit our comprehensive website or call for our catalog. We'll show you how easy it is to change... for the good.

ARIES® ELECTRONICS, INC.

P.O. Box 130 Frenchtown, NJ 08825
Phone: (908) 996-6841
Fax: (908) 996-3891
e-mail: info@arieselec.com
web: www.arieselec.com

ISO 9002 Certified

Sensible Solutions... Fast!

READER SERVICE 149

timal, resulting in increased DMD. With uncontrolled DMD, a string of pulses can spread out so much that they interfere with each other to the extent that data cannot be recovered reliably.

Extensive analysis of DMD characteristics in today's fiber-optic cabling system has shown that optimum signal-propagation distances can be achieved by selectively launching light into the fiber in a donut shape that uniformly encircles the fiber's center *(Fig. 1)*. This allows for maximum light output across a minimum number of propagation modes. This eliminates smearing over distances up to three times longer than broadly launched signals of the same output strength.

Packaging and alignment: The main contributor to packaging cost is the process of aligning light coming out of the semiconductor with the optical fiber. Physical packaging of optical transceiver components involves all of the normal semiconductor packaging issues—plus a giant step in difficulty with regard to alignment. The effective launching of light from the semiconductor into the fiber demands precise and consistent alignment relationships between the internal positioning of the semiconductor and the external plug points for the fiber connector. In addition, these critical coupling-efficiency alignments must remain intact during subsequent shipping, handling, and systems assembly, as well as throughout a wide range of operating conditions.

Test: The nature of optical interconnects, combined with the wide range of operating environments for gigabit-speed networks, makes rigorous testing critical in component manufacturing. To meet specification requirements, every optical interconnect component must be able to consistently produce an eye diagram that conforms to a predetermined eye-diagram mask *(Fig. 2a and b)*. Only by ensuring that light pulses actually emitted by the component are consistently grouped within the GbE standard's eye diagram, can the designer predictably rely on it to produce the required propagation distances.

It's also vitally important to keep in mind that the component must meet the eye-diagram mask test at more than just a single-point operating temperature. Typically, today's network-equipment manufacturers must design their systems for full test compliance at operating temperatures across a range from 0° to 70°C. Therefore, it is important that optical-interconnect component-level suppliers ensure compliance with the specification over the full operating range. This is especially true at the high end (70°C) where it's difficult to maintain output stability. Vendors can deal with this by extensive over-temperature device characterization and on-going production verification testing.

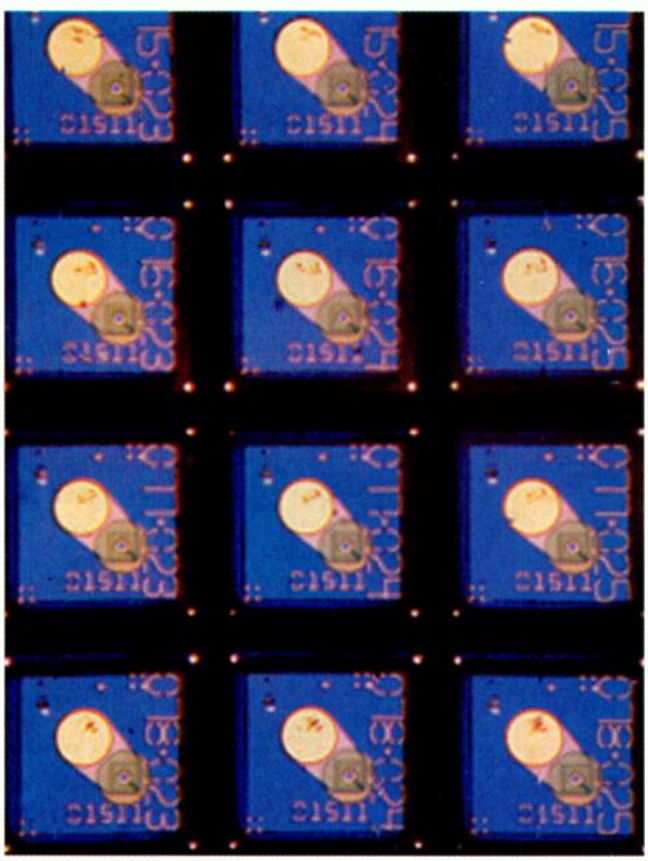
Initially, GbE implementations were cost constrained due to the need to use expensive, edge-emitting lasers for both long-wavelength (1000Base-LX) and short-wavelength (1000Base-SX) implementations. While edge-emitting designs remain the primary method for producing long-wavelength, Fabry-Perot (FP) transceivers, vertical-cavity, surface-emitting lasers (VCSELs) have emerged as a more effective method for creating short-wavelength transceivers. It does this at less than half the cost of edge-emitting FP lasers.

As gigabit-level optical networks move into wider deployment levels, requiring greater configuration flexibility, VCSEL-based GBICs open the door for cost-effective volume installations of 1000Base-SX solutions. VCSEL technology meets and exceeds the critical challenge of providing reliable signal propagation up to, and beyond, specified distances, all while allowing for straightforward packaging/ alignment methodologies and efficient production-level testing and verification.

As its name implies, a vertical cavity laser is formed through the vertical stacking of crystalline mirrors. Sandwiched within these mirrors are the epitaxial layers of an active, light-emitting semiconductor. As many as 120 mirror layers may be combined within a total thickness of <10 µm, to accomplish the required lasing action for a gigabit-speed communications interface. Unlike edge-emitting lasers, the output from a VCSEL is emitted from a relatively small area (5 to 25 µm) on the chip's surface, directly above the active region. An edge-emitting laser requires much more wafer area, due to the relatively long waveguide needed (200 to 500 µm).

From a practical standpoint, a VCSEL's physical structure yields many inherent design advantages like compact size and surface area, high reliability, and size and shape flexibility in the output aperture. Through tight fabrication control, VCSEL crystalline structures can also be specifically tailored to overcome DMD. This is done by optimizing their launch patterns to match the specific characteristics of existing multimode fiber-optic cabling installations.

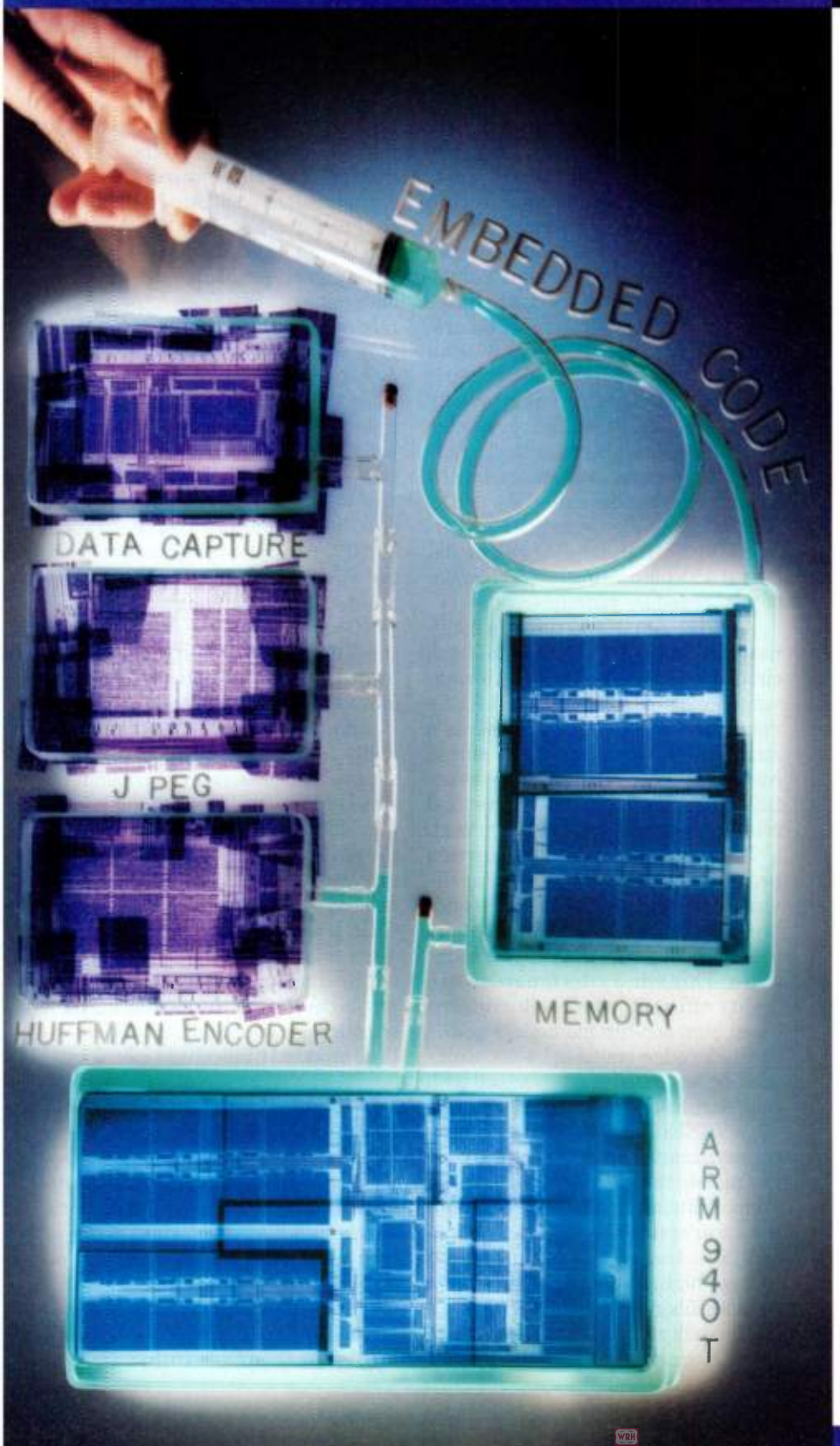
A VCSEL's smaller size means that it requires much less operating current to turn



3. The VCSEL fabrication process produces complete lasing devices on the wafer. This way, every device can be fully tested while it's still in a wafer state, and therefore, take advantage of lower-cost semiconductor techniques. In contrast, edge-emitting lasers must be cleaved and separated to form their mirrors prior to testing.

YOU'RE ABOUT TO INFUSE SEVERAL MEGABYTES OF A FOREIGN SUBSTANCE INTO YOUR ARM9 SYSTEM-ON-CHIP DESIGN.

what now?



SEAMLESS CVE™

HARDWARE/SOFTWARE CO-VERIFICATION

Theoretically, your system's completed, but will it boot? Will the hardware diagnostics pass? Will you be coding your way around hardware problems? Will it take another spin?

In short, how do you ensure your software and hardware will come together harmoniously on silicon?

Fear not. Seamless Co-Verification Environment will tell you. Before it's too late. By creating a virtual prototype that fully validates your embedded software and hardware together. Months before your physical prototype hits the lab.

So design with ARM.

And validate with Seamless.

Come see why. Visit us at **www.mentorg.com/seamless/** and find out how you can sign up for a Seamless workshop in your area.

The ARM940T is a complete, pre-designed cached processor macrocell that incorporates instruction and data caches, a write buffer, and a new protection unit designed especially for embedded applications.

Mentor Graphics

The Power To Create™

READER SERVICE 111

the light pulse on and off. For example, a VCSEL's lasing threshold can be as low as 1 to 2 mA, while larger, edge-emitting FP lasers need about 30 mA to drive the lasing activity. VCSELs thus use less power and dissipate significantly less heat during normal operation. Not only do their lower power requirements increase circuit reliability, VCSELs also greatly simplify overall design challenges for the system designer. They do this by minimizing support-circuitry and power-supply requirements, while reducing the complexity of EMI compliance for the transceiver module.

VCSELs greatly reduce both the cost and complexity of creating a complete, fiber-coupled transmitting device. Traditionally, the need to hermetically seal edge-emitting lasers, combined with the alignment difficulties associated with their asymmetric diffraction patterns, drives up overall packaging costs. VCSELs provide high reliability without hermetic sealing because their active regions are buried several microns beneath the surface, with no exposed active facets. Non-hermetic VCSEL packaging can be designed with plastics instead of ceramics to further reduce materials costs.

Also, the output aperture of a multimode VCSEL is typically a 5- to 20-µm circular aperture, producing a low-divergence circular beam. The VCSEL's vertically-emitted beam presents a straightforward mechanism for simple coupling of the device directly to the optical fiber. This minimizes the cost and complexity of packaging and alignment.

Because the VCSEL fabrication process produces a complete lasing device on the wafer, prior to scribe-and-break operations, it is possible to fully test every device while still in a wafer state. This allows designers to use highly efficient, semiconductor-oriented, step-and-test methods *(Fig. 3)*.

Unlike edge-emitting lasers, which must be separated and assembled with their mirroring structures prior to testing, a VCSEL allows interconnect component manufacturers to push the yield loss up into the lower-cost, wafer-state arena. Ultimately, this translates into the lower optical-interconnect-component costs that system designers need to meet higher volumes in the short-distance, fiber-optic-link GbE market.

The ability to monolithically produce VCSEL arrays also opens the door for expanded architectural options at the transceiver-module level. The combination of closer edge-to-edge spacing for discrete VCSEL devices, consistently uniform alignment characteristics, low power consumption, reduced heat dissipation, and minimal crosstalk susceptibility, allows designers to pack more interconnects within existing size and power constraints. The monolithic nature of VCSEL device manufacturing also has the potential to be adapted to support multiple lasing devices within a single chip-level package. Such configurations could someday provide the key for the practical implementation of parallel, optical-gigabit links.

As gigabit-per-second networks and data communications systems begin to rely on optical-interconnect technologies, the current combination of surface-emitting VCSEL technology for short wavelengths, and edge-emitting Fabry-Perot technology for long wavelengths, provides optimal cost/performance trade-offs for both 1000Base-SX and 1000Base-LX transceivers. It's also likely that future improvements to VCSEL fabrication processes will pave the way for cost-effective VCSEL implementations of long-wavelength (1300-nm) lasers. That will allow all of the VCSEL's reliability, alignment, testing, and cost advantages to migrate into 1000Base-LX transceivers as well.

From a systems standpoint, the flexibility to configure systems with hot-swappable transceiver components, instead of 1-by-9 soldered solutions, will provide a significant cost reduction. At the same time it will shrink the inventory levels needed to meet customer demand. The widespread adoption of the GBIC transceiver form factor allows today's solutions to be easily deployed within dynamic and diverse network topologies, laying the foundation for a smooth migration to tomorrow's innovations in optical transceiver technology.

Tim Bour, president and CEO of Cielo Communications Inc., has over 20 years experience in manufacturing, product development, business planning, financial planning, and strategic marketing, including eight years in high-speed fiber optic components and transceivers. He received a BS in Chemical Engineering from the University of Cincinnati, Ohio, and an MBA from Ohio State University.

CAPACITORS

NEW

1000µF Tantalum SMD
20mΩ ESR (typ.) at 100 kHz/25°C

R Case Size

Industry's lowest ESR per cap value

- **Volumetric Efficiency** The largest capacitance in the smallest size. Up to 40000 cv/cc (1000µF/6.3V in .16cc pkg.)
- **Maximum Capacitor Rating** 1000 µF available now, 1500 µF available soon.
- **Package Capability** Available in standard, thin or special packages. All ratings.
- For Flash Fax service call 1-800-487-9437 and enter document #40050.

POWER SEMICONDUCTORS

4mΩ On-Resistance
75A-30V Breakdown in a D^2PAK
SMD Power MOSFET

Lowest on-resistance (4mΩ) in D^2PAK

- **Breakdown Voltages** Up to 60V at 4.5V gate ratings.
- **Optimized MOSFETs with 3.5nC Gate Charge** Efficient switching in dc/dc power conversion applications.
- **ESD Protected 30mΩ MOSFETs in TSSOP-8.** Ideal for Li Ion battery applications.
- **Broadest Offering of N- and P-Channel MOSFETs** Enables designers to optimize space and performance – SO-8, TSSOP-8, TSOP-6, SOT-23, DPAK, D^2PAK, TO-220.
- For additional information about our SMD Power MOSFETs call 1-800-554-5565.

www.vishay.com

Passive Components
Bulk Metal® Foil Resistors • Metal Film Resistors & Networks • Thick Film Resistors & Networks • Thin Film Resistors & Networks • Current Sensing Resistors • Wirewound Discrete Resistors • Thick Film R/C Networks • Tantalum (Solid) Capacitors • Tantalum (Wet) Capacitors • MLCCs • Ceramic Capacitors • Film Capacitors • Aluminum Capacitors • Trimming Potentiometers • Panel Controls • Custom Magnetics • Inductors

Discrete Semiconductors
Optoelectronic Components • Small Signal Transmitters • Power Integrated Circuits • Diodes • Power MOSFETs • RF Suppressors • Analog Switches and Multiplexers

MANUFACTURER OF THE WORLD'S BROADEST LINE OF DISCRETE ELECTRONIC COMPONENTS

VISHAY

VISHAY INTERTECHNOLOGY, INC.
Dale • Draloric • Foil Resistors
Lite-On PSC • Roederstein • Sfernice
Siliconix • Sprague • Telefunken
Thin Film • Vitramon

READER SERVICE 135

PRODUCT UPDATE: FIBER-OPTIC AND INFRARED COMPONENTS

Manufacturer	Device	Description	Price and delivery	CIRCLE
Allied Telesyn International Corp. **Sunnyvale, CA** **Sales Dept. (800) 424-4282** **Fax (408) 736-0100** **www.alliedtelesyn.com**	AT-MX40F/SM and AT-MX500F/SM transceivers	These microtransceiver modules target 10Base-FL and 100Base-FX applications, respectively. The '40F/SM uses ST connectors, and connects to almost any data terminal or hub at rates of up to 10 Mbits/s (single mode). The '500F/SM uses SC connectors, and provides connectivity between standard 40-pin media-independent interfaces and standard Fast Ethernet cabling. Data rates reach up to 100 Mbits/s, again with single-mode fiber.	AT-MX40F/SM, $586; AT-MX500F/SM, $1048	553
Clairex Technologies Inc. **Plano, TX** **Albert Bomchill (972) 422-4676** **Fax (972) 423-8628**	CLE234E quad-chip, infrared diode	Designed for high-power applications, this quad-chip infrared (IR) diode produces 600 mW of power, at a wavelength of 880 nm, when pulsed with 10 A at a low duty cycle. Comprising 12-mil^2 IR diodes rated at a continuous forward current of 100 mA, the device measures 30 mil^2, and is rated at 500 mA. The chip is mounted in a TO-46 package with a water-clear epoxy dome and a uniform 140° radiation pattern. The operating temperature reaches as high as 150°C.	$5.92 each/100; two to three weeks ARO	554
Connect-Tech Products Inc. **Carson City, NV** **Sales Dept. (800) 809-2751** **Fax (702) 883-4874** **www.connect-tech.thomasregister.com**	FC and SC connectors and adapters	Designed for telecom and network applications, this line of fiber-optic connectors and adapters come in FC and SC configurations. The FC-style adapters are available in single-mode or multimode versions, while the SC connectors and adapters are available in single- or dual-wide versions; both suit 3.0- or 900-µm-diameter cable.	$0.69 each; four weeks ARO	555
	Fiber-optic patch cords	Available in ST, FC, and SC single-mode versions, these fiber-optic patch cords meet FDDI and SNA 905 requirements. The cords are designed to work with plastic optical-fiber cables and fan-out cables with various style connectors. Typical lengths are 1, 2, 3, 4, or 5 m, but custom lengths are available.	From $14; four weeks ARO	556
Finisar Corp. **Mountain View, CA** **Dick Woodrow (650) 691-4000** **Fax (650) 691-4010** **E-mail: sales@finisar.com** **www.finisar.com**	FTR-8520 and -1320 GBIC transceivers	These hot-pluggable, gigabit interface converter (GBIC) transceivers come in short-wavelength; multimode; and long-wavelength, single-mode versions, respectively. Fully compliant with the GBIC specification, the converters can determine the Open Fibre Control (OFC) or non-OFC preference of the opposite end of a Fibre Channel Link, and adopt that mode of operation. Other features include built-in self test, diagnostics, automatic start up, a transmission distance of 30 km, and a data rate of 100 Mbits/s to 1.25 Gbits/s. The bit-error rate (BER) is less than 10^{-16}.	FTR-8520, $169; FTR-1320, $336	557
Hamamatsu Corp. **Bridgewater, NJ** **Sales Dept. (800) 524-0504** **Fax (908) 231-1218**	Infrared laser diodes	This series of infrared, pulsed, laser diodes targets both industrial and scientific applications. Available with output wavelengths ranging from 807 nm up to 870 nm, the diodes have an output power capability ranging from 700 mW to 20 W, depending on the device chosen and its mode of operation. A typical version, the L7055-04, has a rise time of 0.5 ns, a spectral radiation bandwidth of 4 nm, a beam spread of 8°, and a duty ratio of 0.075%.	From $160; five days ARO	558
Hirose Electric (U.S.A.) Inc. **Simi Valley, CA** **Sales Dept. (805) 522-7958** **Fax (800) 879-8071**	HO7 series duplex connector	Conforming to IEEE 1394b, S100 standard, as well as the ATM Forum standard for P/N connectors, these duplex connectors suit plastic-fiber applications. The connectors have a single-body design, with metal ferrules. Features include an improved friction-lock mechanism and coupling stability.	$1.82 each per 1000; six to eight weeks	559
Hitachi Semiconductor (America) Inc. **Brisbane, CA** **Sales Dept. (800) 285-1601** **Fax: (303) 297-0447** **www.hitachi.com/semiconductor**	HL6321G and HL6322G red laser diodes	These AlGaInP-based, multi-quantum-well, red laser diodes come in a type-G package, and output up to 15 mW of power at a wavelength of 635 nm. Operating off 2.7 V, the devices have an operating temperature range of -10° to 50°C, and a typical horizontal and vertical beam divergence of 8° and 30°, respectively.	$130 each per 1000; samples now, volume Q4	560
Honeywell's Micro Switch Div. **Freeport, IL** **Sales Dept. (800) 537-6945** **Fax: (815) 235-6545** **E-mail: info@micro.honeywell.com** **www.honeywell.com/sensing/.**	HFE438X series connector-ized VCSEL	Intended for high-speed data transmission, these connectorized, vertical-cavity, surface-emitting laser (VCSEL) components have an output wavelength of 850 nm. Features include a lensed and pre-aligned SC connector sleeve, and a photodetector that assists in optical-power monitoring.	$22.01 each per 1000; stock	561
	HFE408X series VCSEL	Emitting at a wavelength of 850 nm, these VCSEL lasers come in a TO-46 package with an operating temperature range of 0 to 70°C. The devices have an operating frequency of 1 GHz, and can operate in a single longitudinal mode, but with multiple transverse modes.	$12.71 to $15.50; stock	562
Lucent Technologies **Microelectronics Group** **Murray Hill, NJ** **Customer Response (800) 372-2447** **www.lucent.com/micro**	Speed-Blaster miniature transceivers	Part of the company's NetLight family of transceivers for Gigabit Ethernet, ATM, SONET, and Fibre Channel applications, these miniature devices follow the industry footprint of 0.5-in. wide. Half the common standard of 1 in., the devices double the port density while providing a bandwidth of between 155 and 2.5 Gbits/s. Available in 10- and 20-pin configurations, the transceivers operate off 3.3 V, and include features such as clock recovery and laser-diode monitoring and control. The receptacle is LC compatible.	$905 each per 1000; samples Q4	563

Harting Introduces USB Connector

New HARTING Universal Serial Bus Connector -- Series A and B add a new dimension of flexibility to Desktop/ Notebook PC and a variety of peripheral devices. Single USB port is used for connecting peripheral devices, including those that use serial, parallel, keyboard, mice or game ports. Peripheral devices are connected to the PC through the same connector allowing a reduction of required PC slots. Users will be particularly interested in these features: Plug and Play; Hot Swapping Capabilities; Computer / telephony integration: and Port consolidation. HARTING's new units permit transfer rates up to 12 Mb / s and support up to127 devices. The USB has subchannel for 1.5 Mb / s signaling and allows daisy chaining of peripheral devices. Up to 5m per cable segment, Isochronus and Asynchronous data transfer and built-in power distribution for low power devices are important specifications.

READER SERVICE 178

har-pak® 2.5mm Connector System...

High Density, Board To Board, Analog Coax Solution

HARTING's micro coaxial connector system can provide more than twice the number of contacts in the same board space of typical SMA or DIN connector styles. The coax system can increase the quantity of high speed analog signal density and save space on your PCB. The HARTING ***har-pak®*** coax and signal connector systems are robust and have densities reaching 35 pins per inch. The larger 2.5 mm contact spacing improves crosstalk and high frequency performance. The ***har-pak®*** system is made for high volume applications with SMD compatibility and reliable solderless compliant pin terminations for both signal and coax applications. The ***har-pak®*** connector systems can provide a competitive advantage to increase your system performance, reduce manufacturing cost, and increase system reliability.

READER SERVICE 179

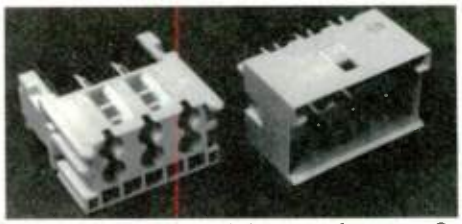
HARTING Introduces SCA-2 Connectors for Storage Devices

The new SCA-2 connectors serve as the only means of electrically attaching a small form factor hard disk drive. Available with 40 and 80 contact positions for fiber channel and SCSI drives respectively. Connectors contain make-first / break-last contacts that enable users to "hot-swap" storage devices without taking the entire storage unit off-line. Blind mating is accomplished through a pair of guideposts on the plug connector that have a generous lead-in and are equipped with grounding contacts. The plug ground contacts mate with a pair of ground contacts on the receptacle before any other electrical connection is made thus protecting the storage device from electrostatic discharge. Final alignment is performed by the "D" shape of the mating connector bodies. Highly reliable bellows style contacts

are used for signal contacts. The plastic connector housings are made of high temperature thermoplastic for surface mount compatibility.

READER SERVICE 180

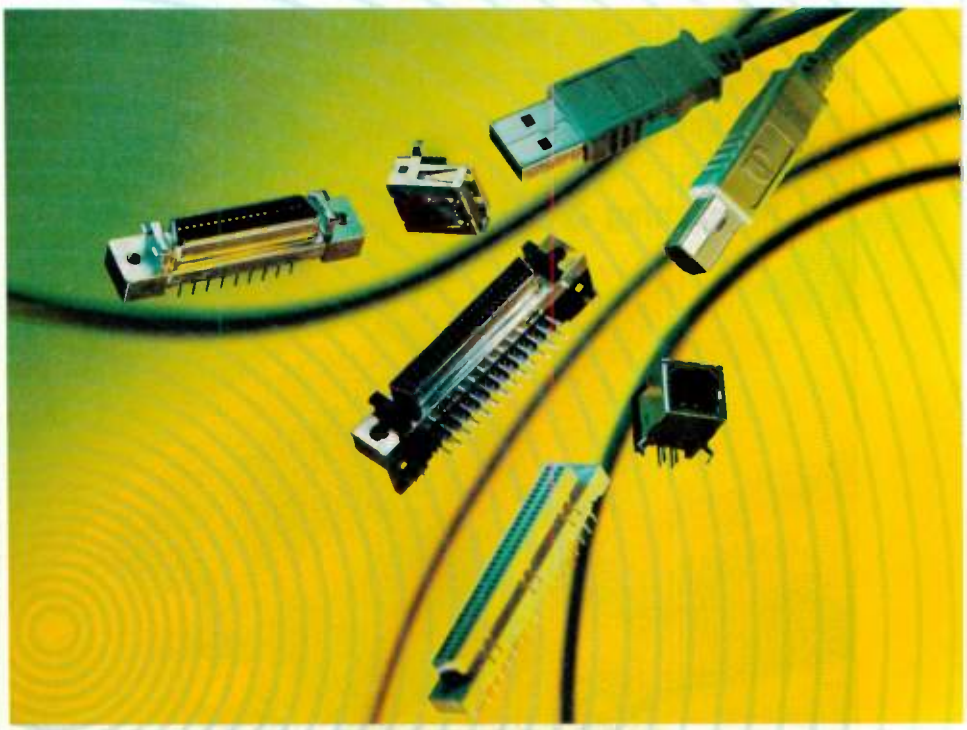
New High Density Micro-Coaxial Contacts



Designed for high speed data transfer rates. Can be used in the iec 1076-4-2 2.5mm High Density connector system, *har-pak*® Provides more space efficiency, high frequency capability, easy handling, low applied cost and application with current equipment and emerging metric equipment practices. Designed for PCB termination on both daughter card to backplane connection; allowing users to bring signal directly into the backplane without cable transition.

READER SERVICE 181

The Future is fine Pitch



har-mik® – High Density I/O Connector Systems

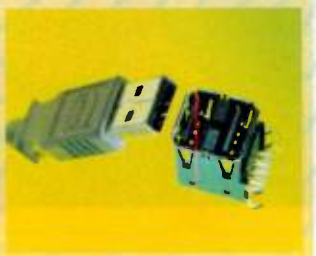
The har-mik® connector family is designed to meet the requirements of the new generation of parallel and serial bus applications.

New developments in the SCSI 2 & 3 range offer significant advantages in weight saving and termination techniques.

The new lightweight version provides a weight saving of more than 35% when compared to standard versions.

In addition HARTING now offers a press in version for plated through holes of 0.55 to 0.67 mm, which can be terminated using 'flat rock' tooling.

For PC and peripheral applications requiring a single USB port HARTING now offers a comprehensive range of USB jacks, plug connectors and cable assemblies for PC and peripheral applications. Key features include full "plug and play" compatibility and "hot swapping" connection and disconnection.



- **Applications in storage equipment and EDP standardization**

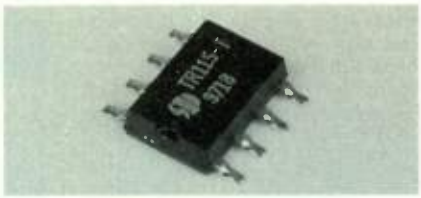
HARTING, Inc. *of North America*
1370 Bowes Road
Elgin, IL 60123
Tel. 847-741-1500 Fax 847-741-8957
E-Mail: more.info@HARTING.COM

HARTING People Power Partnership

READER SERVICE 182

Solid-State Telecom Relay Uses Optical Isolation

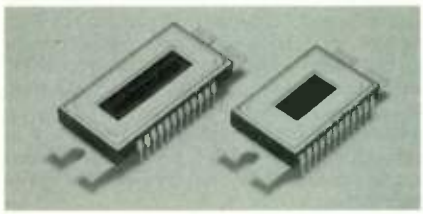
The TR115 is an optically coupled, solid-state relay for telecom applications. Available in an 8-pin package, the device uses an ac switch comprising an LED optically coupled to a dielectrically isolated IC. The IC drives a pair of DMOS transistors. A pair of back-to-back LEDs, coupled to a bipolar transistor, make up the ac detector. Together, the two circuits can provide hookswitch and ring detection in one package. The device has a height of 0.093 in. Pricing is $1.99 each per 10,000; delivery is two to four weeks.



Solid State Optronics Inc., 2 North First St., San Jose, CA 95113; Anna Highsmith (888) 377-4776; Internet: www.ssousa.com. **CIRCLE 530**

CCDs Operate In Line-Binning And Area-Scanning Modes

The S7030 and S7031 series of back-thinned CCD image sensors come in uncooled and thermoelectrically cooled versions, respectively. Able to operate in both line-binning and area-scanning modes, both sensors use FFT CCDs and have a pixel size of 24 by 24 µm. The devices, which come in 24-pin packages, feature a quantum efficiency of over 90% and a spectral response of 200 to 1100 nm. Pricing for the S7030 is $1470, and $1935 for the S7031; availability is five weeks.



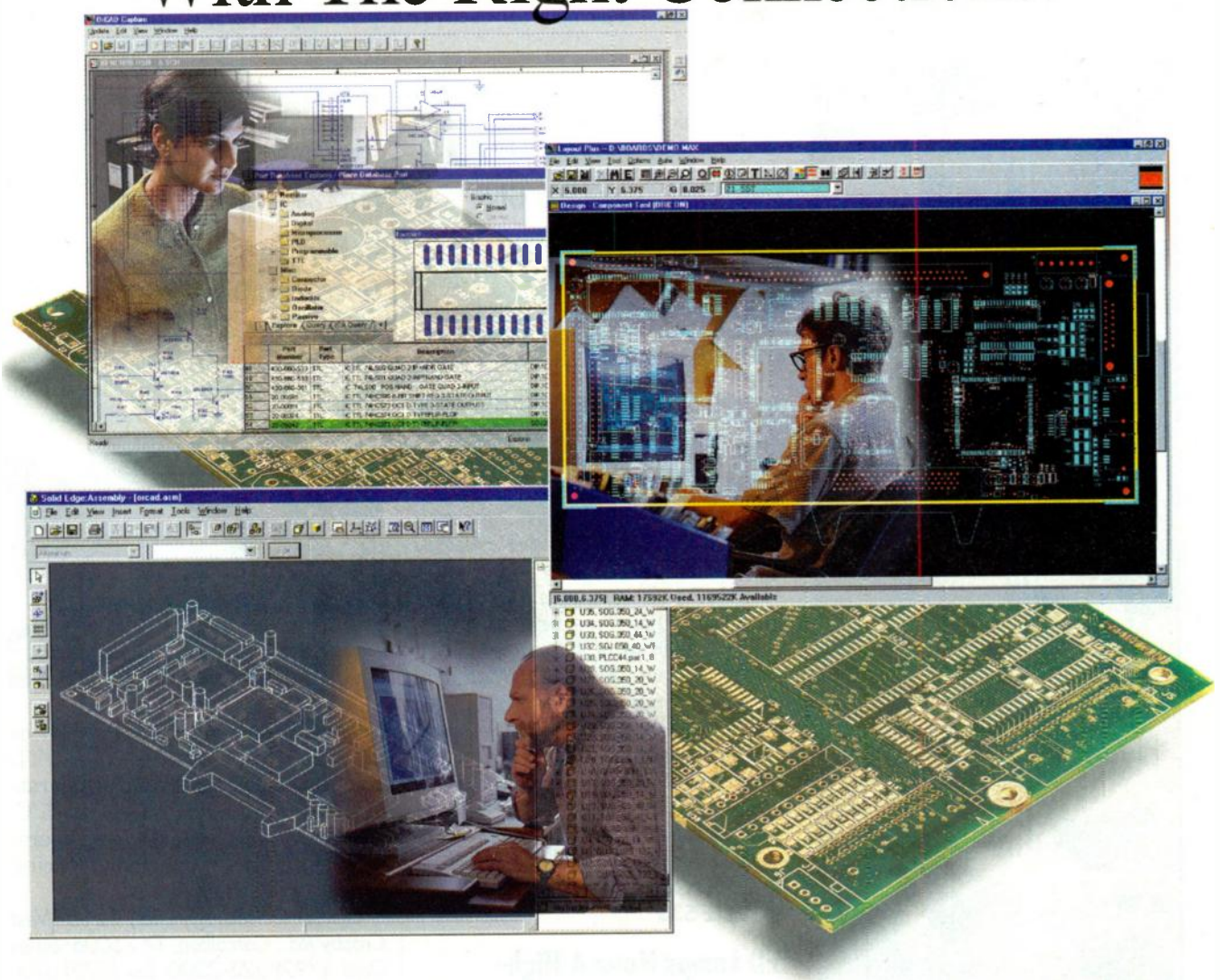
Hamamatsu Corp., 360 Foothill Rd., Box 6910, Bridgewater, NJ 08807-0910; Sales Dept. (800) 524-0504; fax (908) 231-1218. **CIRCLE 531**

Visible Laser Diode Outputs At 650 nm At Low Currents

Designed for DVD and bar-code scanner applications, the RLD-65MC/PC laser diode outputs light at a wavelength of 650 nm. Manufactured using a strained MQW active layer, the diode has a luminous intensity of 7 mW and a guaranteed high operating temperature range of 70°C. Typical

(continued on page 74)

Amazing What You Can Do With The Right Connections.



With New OrCAD Layout®, You'll Improve Communication Across The Board.

It takes more than a netlist to turn your ideas into a working PCB.

It takes new OrCAD Layout. No other PCB solution connects you electronically with so many kinds of information, to reduce rework and deliver an accurate, correct board faster.

Start your board design with OrCAD Capture CIS™. As you place parts, it automatically imports all the component data you need, including company part numbers, PCB footprints and simulation models, then passes it to OrCAD Layout.

OrCAD Layout also accepts mechanical constraints and floor plan data from ProEngineer, SDRC, and SolidEdge. It includes OrCAD's shape-based autorouter, and a Cadence SPECCTRA interface for high-speed designs. GenCAD/GenCAM outputs pass completeCAD information to fabrication, assembly and test systems.

Want better communication across your entire design process? Connect with OrCAD and get the details on new OrCAD Layout. **Visit us at www.orcad.com/layout or call 1-800-671-9506.**

EDA for the Windows NT Enterprise

OrCAD®

READER SERVICE 123

OPTOELECTRONICS

(continued from page 72)

operating current is 50 mA. Other features include an output efficiency of 0.4 mW/mA at 2 mW, and an operating voltage of 2.3 V. Pricing is $10 each per 500.

***Rohm Corp.**, 3034 Owen Dr., Antioch, TN 37013; Sales Dept. (888) 775-ROHM; fax (615) 641-2022; Internet: www.rohmelectronics.com.* **CIRCLE 532**

Four-Pin Power LEDs Give Even Light Distribution

The QTLP320C and QTLP321C series four-pin LEDs have a viewing angle of 70° and 50°, respectively. The devices are available in TsAlGaAs red and

AlInGaP yellow and amber with a clear lens. Other features include a forward current of 300 mA (peak), a power dissipation of 160 mW, and an operating temperature range of –40° to 100°C. Compatible with automatic placement equipment, the devices are available in 60-piece tube packages at a price of $0.90.

***QT Optoelectronics**, 610 North Mary Ave., Sunnyvale, CA 94086; Sales Dept. (800) LED OPTO; www.qtopto.com.* **CIRCLE 533**

LED Lamps Have A High-Intensity White Output

Using InGaN technology to achieve the elusive blue element, the 200-NWW model LED outputs white light with a luminous intensity of 1100 mcd

and a viewing angle of 50°. The typical forward current is 15 to 17 mA. The lamps, which come in panel-mount or lamp-based versions, feature a wide range of operating voltages from 5 to 120 V ac, dc, or bipolar. Options include snap-in, cartridge-mount, or bolt-on panel lights with secondary optics. The lamp-based design can replace any T-1 3/4, T-3 1/4, or T-4 1/2 incandescent bulb. Pricing for the T-1 3/4 flange-base lamp is $5.43 each per 1000. Delivery is six to eight weeks.

***Data Display Products**, 445 South Douglas St., El Segundo, CA 90245-4630; Sales Dept. (310) 640-0442; fax (310) 640-7639.* **CIRCLE 534**

Reflective Sensor Senses Over Long Distances

The OPB715 series of reflective sensors can accurately detect paper at a distance of up to 0.5 in. They come with 18-in. wire leads and dissipate

300 mW. Panel-mountable, the devices have either TTL totem-pole or TTL open-collector outputs and an operating temperature range of –40° to 85°C. Custom options include lenses, apertures, filters, and connectors. Pricing is $4.90 each per 1000.

***Optek Technology Inc.**, 1215 West Crosby Rd., Carrollton, TX 75006; Sales Dept. (792) 323-2200; fax (972) 323-2396; optek1@optekinc.com; Internet: www.optekinc.com.* **CIRCLE 535**

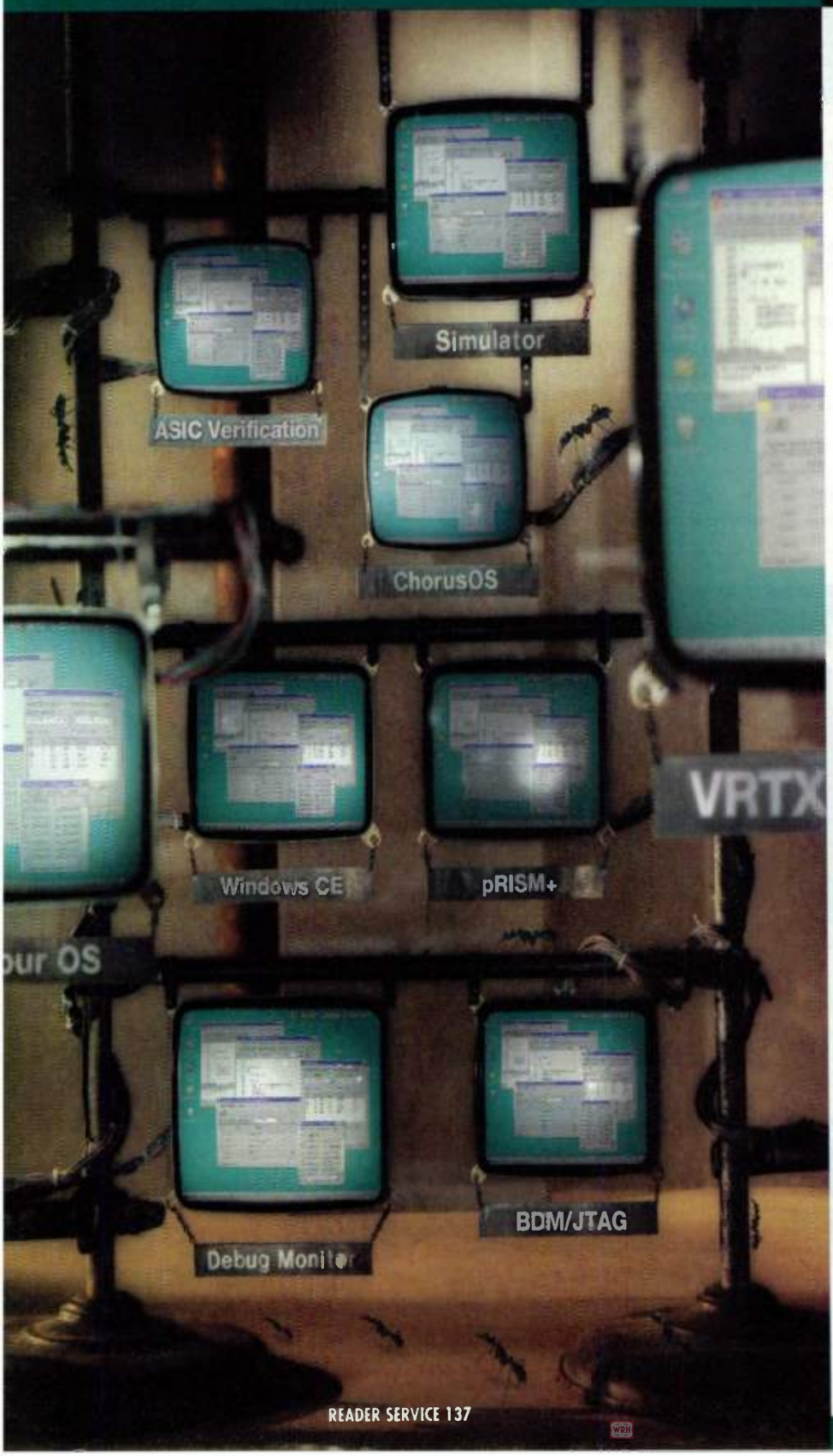
1.8- And 2.5-in. TFT Displays Target Instrumentation

Aimed at instrumentation applications, the AND-TFT-18DM and AND-TFT-25DM are 1.8- and 2.5-in. active-matrix TFT LCDs, respectively. Both displays have a resolution of 160 by 234 pixels and take an analog RGB input. The 1.8-in. display has a brightness of 230 nits, overall dimensions of 51 by 39 by 13 mm, and a total power consumption is 0.90 W, with an external dc-dc converter. The 2.5-in versions has overall dimensions of 68 by 55 by 13 mm, a brightness of 300 nits,

(continued on page 76)

NEW PROCESSOR.
NEW RTOS.
NEW CONNECTIONS.

what now?



XRAY® DEBUGGER

You need a powerful, proven debugging solution that's flexible enough to work with any combination of processor, RTOS or target connection.

XRAY® Debugger, the debugger that's set the standard for a whole generation of embedded software designers, now supports most major RTOSs, including Microsoft® Windows® CE. It's also available on most popular 32-bit embedded processors, such as the ARM® and PowerPC™ families. Furthermore, XRAY supports virtually any connection, including BDM, serial, Ethernet and leading hardware-assist solutions. And to top it all off, XRAY can simulate your target before your hardware is even ready!

No other debugger gives you this much functionality or flexibility. That's why XRAY is everywhere.

Visit **www.mentorg.com/microtec/xray/info.html** or call **800-950-5554 ext. 7025, dept. 525** for more information about XRAY Debugger. And while you're there, register to win your own state-of-the-art satellite dish system!

See it all in our booth #1028 at ESC!

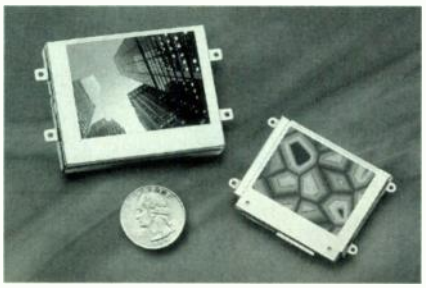
Mentor Graphics

The Power To Create™

Microtec Solutions

READER SERVICE 137

(continued from page 74)



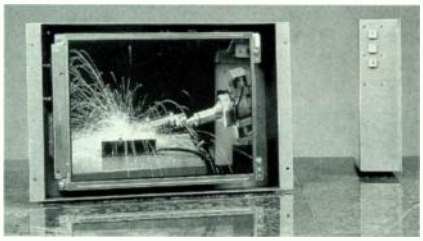
and a total power consumption of 0.97 W. Pricing is $67 for the AND-TFT-18DM, and $96 for the AND-TFT-15DM.

Purdy Electronics Corp., *720 Palomar Ave., Sunnyvale, CA 94086; Paul Balbas (408) 523-8218; fax (408) 733-1287; e-mail: pabpurdy@ix.netcom.com; www.purdyelectronics.com.*

CIRCLE 536

Flat-Panel Monitors Come In A Wide Range Of Sizes

The BareVue line of flat-panel monitors are available in an array of sizes and resolutions for system integrators and OEMs. Mountable in custom cabinets and remote enclosures, the displays use the company's SmartSync technology so that analog input can be translated to a digital format to directly drive the display. The panels, which act as drop-in replacements for CRTs, range in size from 10.4 to 14.1 in. and in resolution from 640 by 480 to 1280 by 1024. A touchscreen is optional. The 10.4-in. version with VGA resolution costs $1200 each in volume.



National Display Systems Inc., *761-A University Ave., Los Gatos, CA 95032; Sales Dept. (408) 395-8688; fax (408) 395-5288; Internet: www.nationaldisplay.com.* **CIRCLE 537**

Five-Inch TFT LCD Comes With Multiple Input Formats

The V-LCD5V is a 5-in. TFT LCD that features a resolution of 960 by 234 pixels and the ability to switch between VGA, NTSC, and RGB inputs.

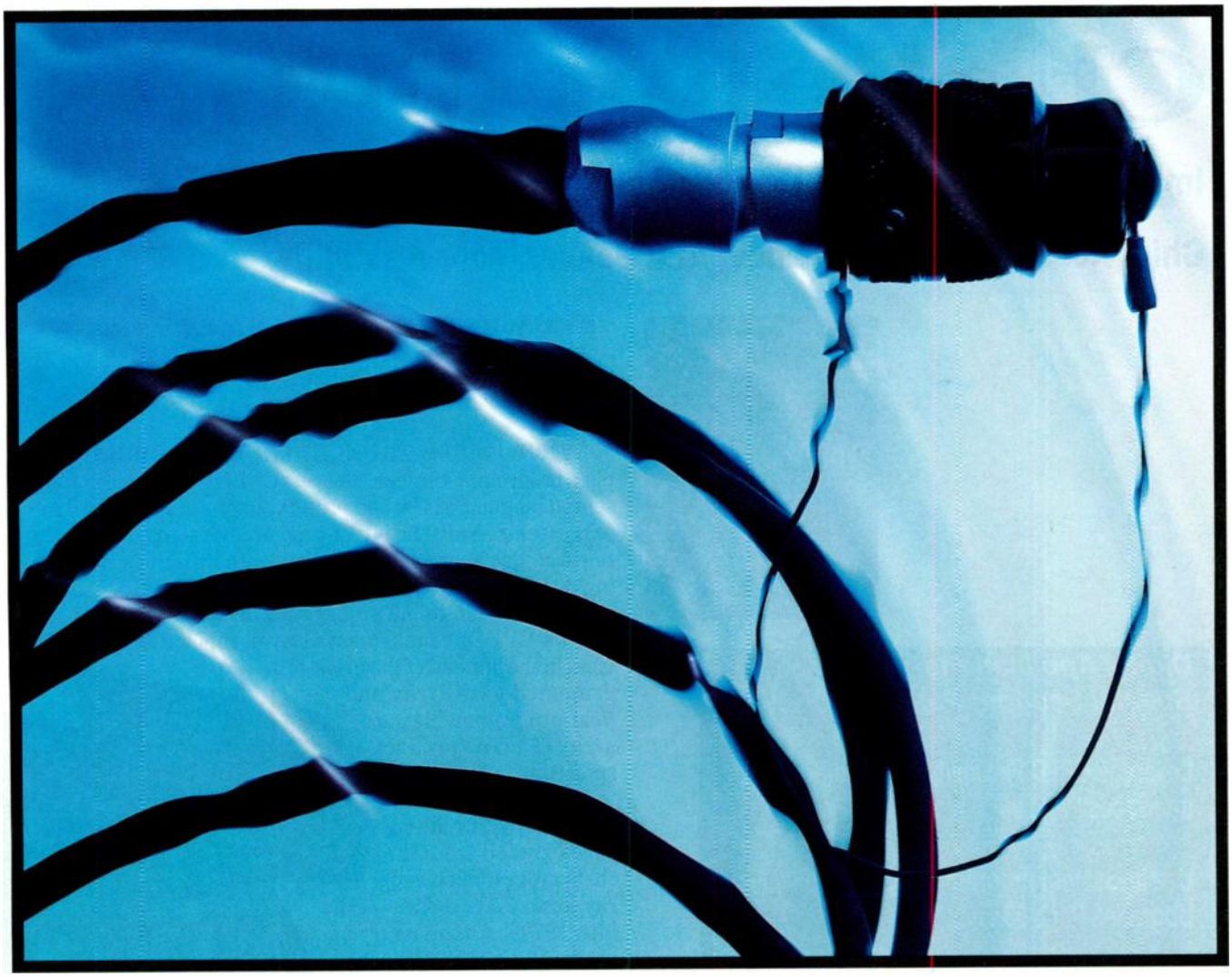
Targeting wall-display and single-board-computer applications, the displays come with a touchscreen option. Pricing is $599 each.

Marshall Electronics Inc., *P.O. Box 2027, Culver City, CA 90231; Nathan Mordukhay (800) 800-6608; fax (310) 391-8926; e-mail: webmaster@mars-cam.com; www.mars-cam.com.*

CIRCLE 538

Problem:

Build a high performance interconnect system tough enough to survive challenging environments. Even sterilization.



No Problem.

For Precision Interconnect.

Providing the complete interconnect systems for hand-held surgical devices has given us the expertise to meet severe environmental challenges as well as precise electrical demands. Rigorous testing, simulating exposure to chemicals, heat, humidity, and other physical abuses, confirms the ruggedness and reliability of these assemblies.

Even if your products don't face the challenge of repeated disinfectant and sterilization processes, our experience in the design and manufacture of flexible, high performance cables with sealed terminations can help your products endure.

Dealing with severe environments is just one of our capabilities. We specialize in tight tolerances, extended flex-life and the micro-miniaturization of complete interconnects. Want to know more? Ask for our "No Problem" brochure.

AMP

PRECISION INTERCONNECT

16640 S.W. 72nd Avenue, Portland, Oregon 97224-7756, USA, Phone (503) 620-9400, Fax (503) 620-7131. For more information, visit our website at www.precisionint.com

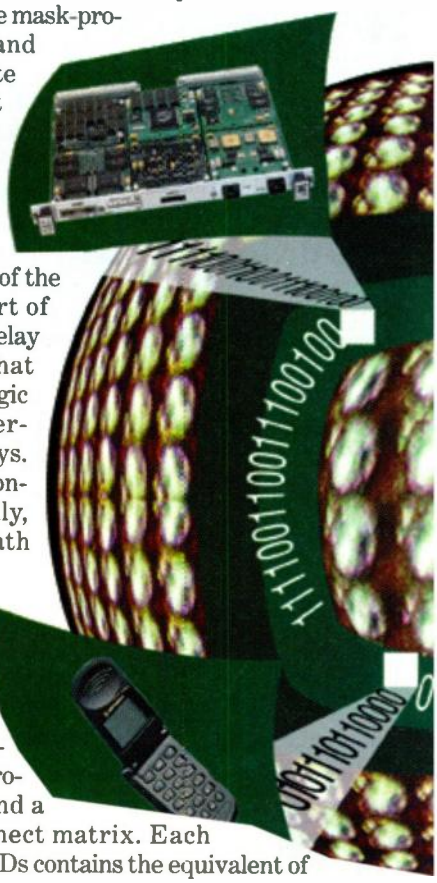
READER SERVICE 161

Advanced CPLD A
Challenge FPGAs,

Improved Processes And Designs Add More Gates Per Chip, Accelerate Performance, And Deliver More Flexibility.

BY DAVE BURSKY, *DIGITAL ICs EDITOR*

With 1000+ gates in their arsenals, complex, programmable logic devices (CPLDs) have become essential building blocks and prototyping tools for many digital systems. And, the latest crop of high-density CPLDs released this year includes devices with capacities surpassing 40,000 gates (PLD-equivalent gates). Such densities, coupled with pin-to-pin propagation delays as low as 3.5 ns, now let CPLDs complement or even replace devices in the low end of the mask-programmed gate array and field-programmable gate array (FPGA) product spectrum.



What we now know as the CPLD architecture evolved from the early programmable-array-logic (PAL) devices of the late 1970s. At the heart of most CPLDs is a fixed-delay interconnect matrix that routes logic inputs to logic outputs with predetermined propagation delays. Surrounding the interconnection array (physically, probably located beneath the array) are the configurable logic blocks, typically referred to as macrocells. These macrocells are somewhat reminiscent of the 22V10 PAL, a 28-pin device that contained 10 programmable I/O cells and a configurable interconnect matrix. Each macrocell in today's CPLDs contains the equivalent of

Digital Applications Special Section: Part 1

Leverage CPLD Flexibility In Customized PCI Interfaces Page 88

Use In-System Programming To Simplify Field Upgrades Page 93

Part 2, November 2:
- *A Standard Language*
- *CPLD-Based HDLC Controller*
- *Prototypes To Production*

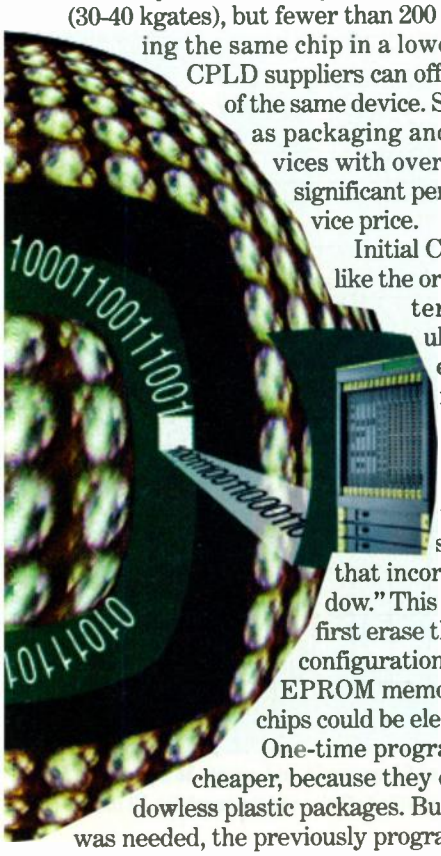
chitectures Gate Arrays

between 150 and 400 programmable gates. Macrocells can be connected to programmable I/O cells through the hierarchy of routing resources.

Not only are CPLDs being called on to implement increasingly larger blocks of system logic, but they are used to handle large, and even multiple, buses. These can include 32- and 64-bit PCI buses, 64- and 128-bit cache data buses, 32-bit and larger address buses, etc. Thus, the I/O pin counts are also growing to keep pace with system demands.

Early CPLDs typically came in 44- to 84-lead packages, while today's high-density devices can be had in ball-grid-array packages with as many as 492 pins (384 signal pins). Even larger devices are planned for 1999.

However, the number of pins a designer needs depends on whether the application is I/O- or register-intensive. Therefore, CPLD vendors can offer various cost points for the same basic chip. For instance, a register-intensive application may need the complexity of the highest-density chip (30-40 kgates), but fewer than 200 or so I/O pins. By placing the same chip in a lower-pin-count package, CPLD suppliers can offer a lower-cost version of the same device. Such an option is critical as packaging and testing costs for devices with over 300 pins account for a significant percentage of the final device price.



Initial CPLD implementations, like the original devices in the Altera EPLD family, used ultra-violet erasable, but electrically programmable memory (UV EPROM) cells. If these devices were to be reprogrammed, they had to be housed in expensive, ceramic packages that incorporated a quartz "window." This way, the UV light could first erase the contents of the chip's configuration memory (just like UV EPROM memory chips), and then the chips could be electrically programmed.

One-time programmable devices were cheaper, because they could be housed in windowless plastic packages. But, if a new configuration was needed, the previously programmed device had to be thrown away, and a new device programmed. So, if two or three configuration iterations were needed, it became more economical to purchase reprogrammable devices.

EE Alternatives

CPLD designers eventually found ways to lower the manufacturing cost of electrically erasable technology without compromising CPLD performance. As a result, over the last few years, electrically erasable memory technology (both EEPROM and flash-type cells) has basically taken over the task of storing the on-chip configuration data. Flash and EEPROM technologies offer designers the best of both the non-volatile world and of the UV EPROM, because they can employ low-cost plastic packages, yet be erased from 100 to 10,000 times to accommodate configuration updates.

Initial EEPROM-based devices required a 12-V supply for programming, in addition to the normal 5-V supply. In recent years, however, designers have not only eliminated the need for the programming supply, but developed ways to program (configure) CPLDs after they are installed. To eliminate the need to place a programming clip over the entire device, Lattice Semiconductor and other companies have developed serial in-system programming (ISP) interfaces. Now, circuit designers can daisy-chain CPLDs, and shift in the configuration data through one device to the next until the data is properly positioned.

More recently, proprietary ISP interfaces have given way to the serial JTAG test port (from the IEEE-1149.1 boundary-scan standard initially developed by the Joint Test Automation Group). A JTAG port is available on almost every CPLD and many other ICs.

Static-RAM-based configuration memory, which is used in many FPGAs, is not a cost-effective solution for the older, low-density CPLDs. SRAM-based devices require a back-up memory to download the configuration pattern, and SRAM cells take up a large chip area. Thus, circuit performance was not topnotch, and the devices were too large and expensive. However, today's fine-line, multilevel-metal CMOS processes make RAM cells smaller and faster, so CPLDs can pack more gates per chip. And, because the main value of a CPLD is in the logic that can be loaded onto one chip, the higher ratio of logic area to memory area makes the device more attractive.

To show the viability of SRAM in a CPLD, designers at Philips unveiled the first chip in an SRAM-based family of CPLDs several months ago, the CoolRunner 960. The de-

vice contains 960 macrocells (about 30,000 usable gates) and 384 I/O cells. It has a typical worst-case, pin-to-pin propagation delay (t_{PD}) of 11.5 ns through the interconnect array between logic blocks called Fast Modules and back off the chip. (If an input goes through the PAL array of a Fast Module or through the PLA, it's 1.5 ns longer.) Internal delays through just the Fast Module block are about 7.5 ns.

The IC combines a second-generation version of the company's patented, extended-programmable-logic-array (XPLA2) architecture, and its patented, fast-zero-power (FZP) power-management technology. As a result, the CPLD can operate from 3.3-V supplies, and consumes minimal power, just 100 µA on standby and 320 mA with 60 16-bit counters running at 100 MHz.

On power-up, the SRAM cells must be loaded with the configuration data. To do that, the chip offers seven configuration modes: master serial, slave serial, master parallel up, master parallel down, slave parallel, synchronous peripheral, and asynchronous peripheral. The many configuration modes allow designers to select the optimal one for their system. Because the device is SRAM-based, and needs no "store" cycles (as EEPROM or flash-based CPLDs do), load times are less than 1 s.

The logic architecture of the CoolRunner 960 (also known as the PZ3960) comprises 12 logic blocks called Fast Modules. Each contains 80 macrocells. All the Fast Modules are interconnected through a global zero-power interconnect array (GZIA), which behaves like a virtual crosspoint switch. Each Fast Module accepts 64 signals from the GZIA, and delivers 64 signals back to it. Eight dedicated input clocks are available, and each fast module can select any two of the clocks as timing inputs. (There are also asynchronous clocks in the Fast Modules.)

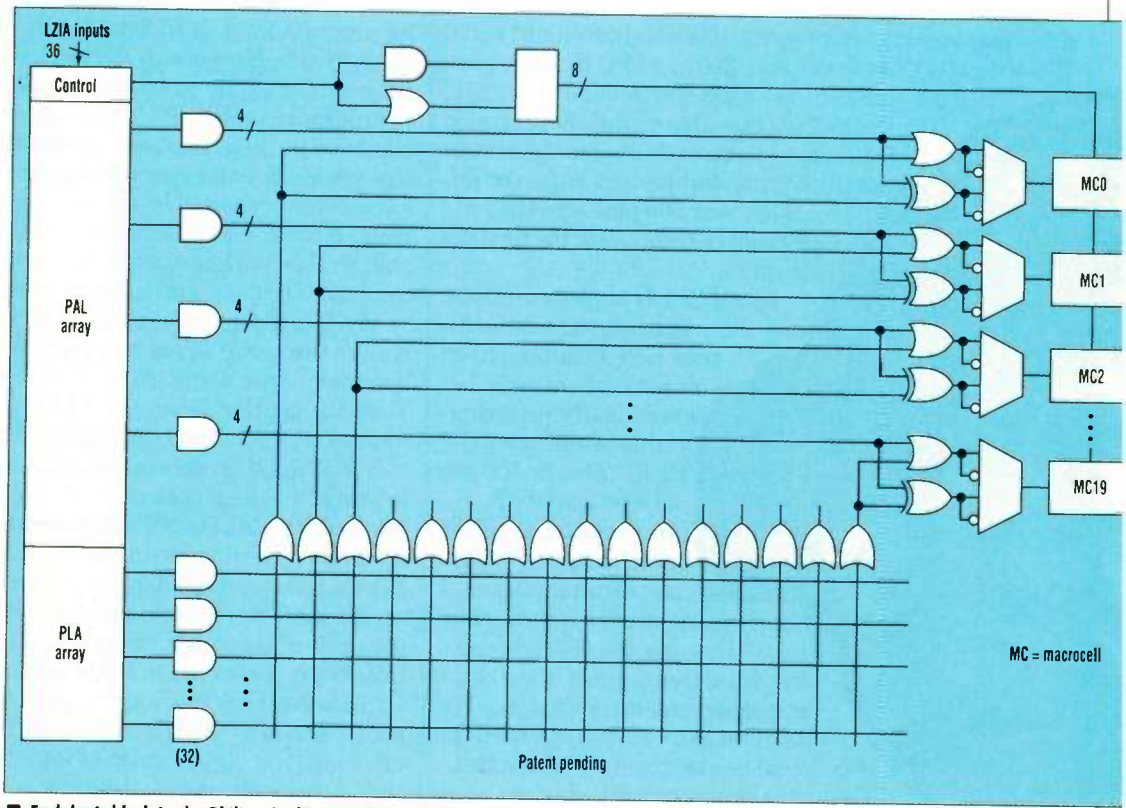
Within each Fast Module, the 80 macrocells are grouped into four blocks of 20, and interconnected through a minimal-delay, local zero-power interconnect array (LZIA). Each group also includes an XPLA2-based logic block that combines the best features of both the PAL and PLA structures.

The PAL structure in the logic block delivers four dedicated product terms to each macrocell. An additional 32 product terms from the PLA portion can be shared through the fully programmable OR array to any of the 20 macrocells. Of the 20 macrocells associated with each XPLA2 logic block, eight are connected to I/O pins, and the remaining 12 can be used as buried nodes *(Fig. 1)*.

The configurable macrocell has a two-input XOR gate, with the dedicated PAL inputs connected to one input and the PLA product terms on the other. Designers can program the internal flip-flop in each macrocell as either a D- or T-type flip-flop. Or, the cell can be bypassed if it is used for a combinatorial logic function. D flip-flops tend to be more useful for state machines and data buffering, while T flip-flops are handy in counters.

Each macrocell has eight control inputs as well as inputs from the PAL and PLA arrays. The internal asynchronous clocks use two of the control terms and the remaining six govern the asynchronous preset and reset of the flip-flops and the enable/disable of the output buffers in each macrocell.

In addition to the CoolRunner 960, Philips will release the CoolRunner 320, with 320 macrocells, later this year. The CoolRunner family also includes electrically erasable devices that offer 32, 64, and 128 macrocells, and operate from 5-V supplies. In late



Each logic block in the Philips CoolRunner 960 contains a PAL array, a PLA array, and 20 macrocells, and accepts 36 inputs from the local zero-power interconnect array (LZIA). Eight of each block's macrocells connect to I/O pins and the remaining 12 can be used as buried nodes.

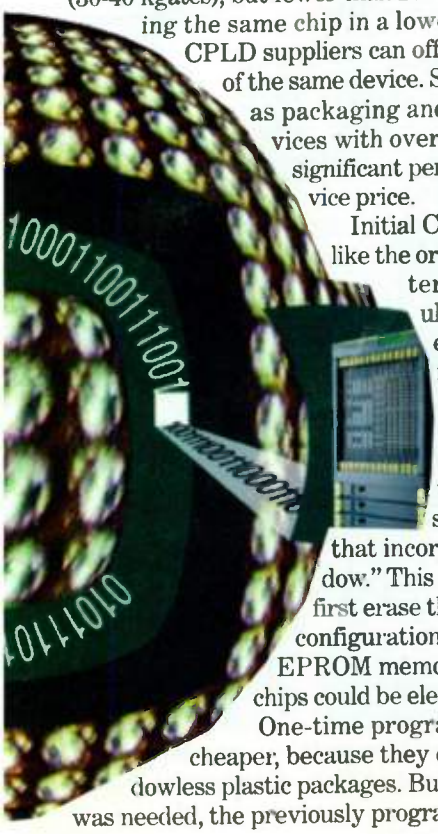
chitectures Gate Arrays

between 150 and 400 programmable gates. Macrocells can be connected to programmable I/O cells through the hierarchy of routing resources.

Not only are CPLDs being called on to implement increasingly larger blocks of system logic, but they are used to handle large, and even multiple, buses. These can include 32- and 64-bit PCI buses, 64- and 128-bit cache data buses, 32-bit and larger address buses, etc. Thus, the I/O pin counts are also growing to keep pace with system demands.

Early CPLDs typically came in 44- to 84-lead packages, while today's high-density devices can be had in ball-grid-array packages with as many as 492 pins (384 signal pins). Even larger devices are planned for 1999.

However, the number of pins a designer needs depends on whether the application is I/O- or register-intensive. Therefore, CPLD vendors can offer various cost points for the same basic chip. For instance, a register-intensive application may need the complexity of the highest-density chip (30-40 kgates), but fewer than 200 or so I/O pins. By placing the same chip in a lower-pin-count package, CPLD suppliers can offer a lower-cost version of the same device. Such an option is critical as packaging and testing costs for devices with over 300 pins account for a significant percentage of the final device price.



Initial CPLD implementations, like the original devices in the Altera EPLD family, used ultra-violet erasable, but electrically programmable memory (UV EPROM) cells. If these devices were to be reprogrammed, they had to be housed in expensive, ceramic packages that incorporated a quartz "window." This way, the UV light could first erase the contents of the chip's configuration memory (just like UV EPROM memory chips), and then the chips could be electrically programmed.

One-time programmable devices were cheaper, because they could be housed in windowless plastic packages. But, if a new configuration was needed, the previously programmed device had to be thrown away, and a new device programmed. So, if two or three configuration iterations were needed, it became more economical to purchase reprogrammable devices.

EE Alternatives

CPLD designers eventually found ways to lower the manufacturing cost of electrically erasable technology without compromising CPLD performance. As a result, over the last few years, electrically erasable memory technology (both EEPROM and flash-type cells) has basically taken over the task of storing the on-chip configuration data. Flash and EEPROM technologies offer designers the best of both the non-volatile world and of the UV EPROM, because they can employ low-cost plastic packages, yet be erased from 100 to 10,000 times to accommodate configuration updates.

Initial EEPROM-based devices required a 12-V supply for programming, in addition to the normal 5-V supply. In recent years, however, designers have not only eliminated the need for the programming supply, but developed ways to program (configure) CPLDs after they are installed. To eliminate the need to place a programming clip over the entire device, Lattice Semiconductor and other companies have developed serial in-system programming (ISP) interfaces. Now, circuit designers can daisy-chain CPLDs, and shift in the configuration data through one device to the next until the data is properly positioned.

More recently, proprietary ISP interfaces have given way to the serial JTAG test port (from the IEEE-1149.1 boundary-scan standard initially developed by the Joint Test Automation Group). A JTAG port is available on almost every CPLD and many other ICs.

Static-RAM-based configuration memory, which is used in many FPGAs, is not a cost-effective solution for the older, low-density CPLDs. SRAM-based devices require a back-up memory to download the configuration pattern, and SRAM cells take up a large chip area. Thus, circuit performance was not topnotch, and the devices were too large and expensive. However, today's fine-line, multilevel-metal CMOS processes make RAM cells smaller and faster, so CPLDs can pack more gates per chip. And, because the main value of a CPLD is in the logic that can be loaded onto one chip, the higher ratio of logic area to memory area makes the device more attractive.

To show the viability of SRAM in a CPLD, designers at Philips unveiled the first chip in an SRAM-based family of CPLDs several months ago, the CoolRunner 960. The de-

vice contains 960 macrocells (about 30,000 usable gates) and 384 I/O cells. It has a typical worst-case, pin-to-pin propagation delay (t_{PD}) of 11.5 ns through the interconnect array between logic blocks called Fast Modules and back off the chip. (If an input goes through the PAL array of a Fast Module or through the PLA, it's 1.5 ns longer.) Internal delays through just the Fast Module block are about 7.5 ns.

The IC combines a second-generation version of the company's patented, extended-programmable-logic-array (XPLA2) architecture, and its patented, fast-zero-power (FZP) power-management technology. As a result, the CPLD can operate from 3.3-V supplies, and consumes minimal power, just 100 µA on standby and 320 mA with 60 16-bit counters running at 100 MHz.

On power-up, the SRAM cells must be loaded with the configuration data. To do that, the chip offers seven configuration modes: master serial, slave serial, master parallel up, master parallel down, slave parallel, synchronous peripheral, and asynchronous peripheral. The many configuration modes allow designers to select the optimal one for their system. Because the device is SRAM-based, and needs no "store" cycles (as EEPROM or flash-based CPLDs do), load times are less than 1 s.

The logic architecture of the CoolRunner 960 (also known as the PZ3960) comprises 12 logic blocks called Fast Modules. Each contains 80 macrocells. All the Fast Modules are interconnected through a global zero-power interconnect array (GZIA), which behaves like a virtual crosspoint switch. Each Fast Module accepts 64 signals from the GZIA, and delivers 64 signals back to it. Eight dedicated input clocks are available, and each fast module can select any two of the clocks as timing inputs. (There are also asynchronous clocks in the Fast Modules.)

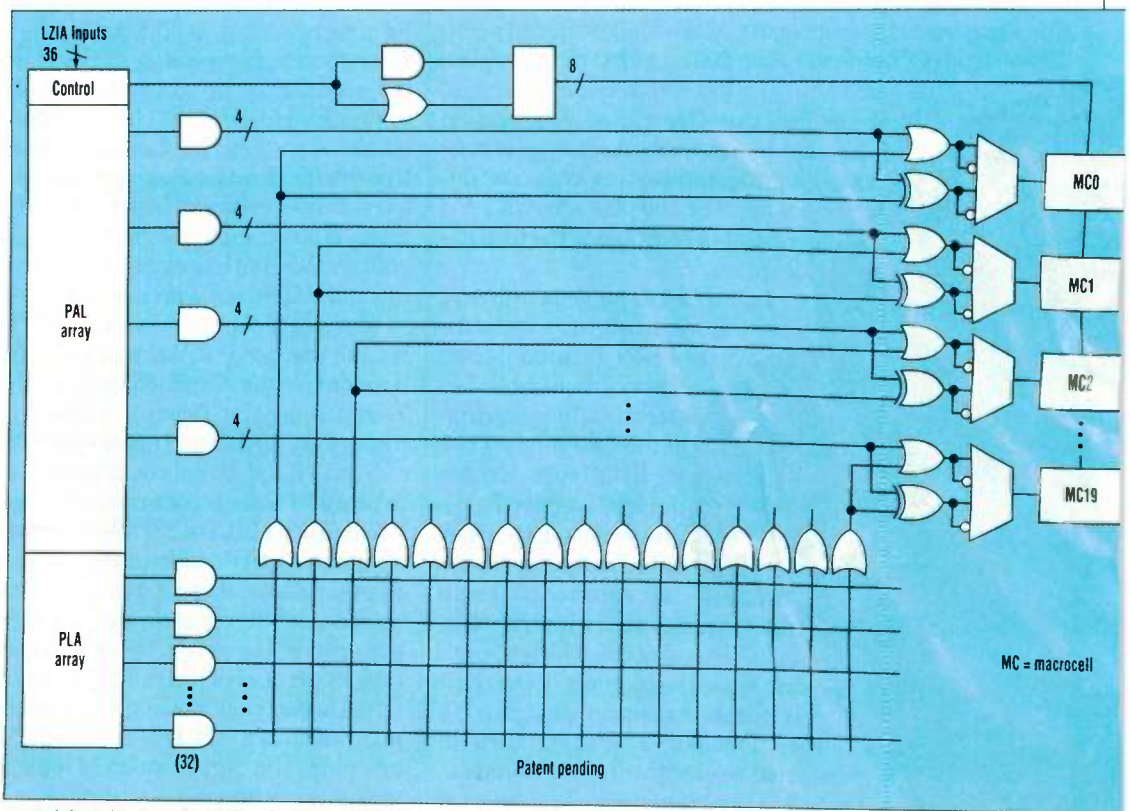
Within each Fast Module, the 80 macrocells are grouped into four blocks of 20, and interconnected through a minimal-delay, local zero-power interconnect array (LZIA). Each group also includes an XPLA2-based logic block that combines the best features of both the PAL and PLA structures.

The PAL structure in the logic block delivers four dedicated product terms to each macrocell. An additional 32 product terms from the PLA portion can be shared through the fully programmable OR array to any of the 20 macrocells. Of the 20 macrocells associated with each XPLA2 logic block, eight are connected to I/O pins, and the remaining 12 can be used as buried nodes *(Fig. 1)*.

The configurable macrocell has a two-input XOR gate, with the dedicated PAL inputs connected to one input and the PLA product terms on the other. Designers can program the internal flip-flop in each macrocell as either a D- or T-type flip-flop. Or, the cell can be bypassed if it is used for a combinatorial logic function. D flip-flops tend to be more useful for state machines and data buffering, while T flip-flops are handy in counters.

Each macrocell has eight control inputs as well as inputs from the PAL and PLA arrays. The internal asynchronous clocks use two of the control terms and the remaining six govern the asynchronous preset and reset of the flip-flops and the enable/disable of the output buffers in each macrocell.

In addition to the CoolRunner 960, Philips will release the CoolRunner 320, with 320 macrocells, later this year. The CoolRunner family also includes electrically erasable devices that offer 32, 64, and 128 macrocells, and operate from 5-V supplies. In late



Each logic block in the Philips CoolRunner 960 contains a PAL array, a PLA array, and 20 macrocells, and accepts 36 inputs from the local zero-power interconnect array (LZIA). Eight of each block's macrocells connect to I/O pins and the remaining 12 can be used as buried nodes.

LINEAR TECHNOLOGY

DESIGN NOTES

Op Amp, Comparator and Reference IC Provides Micropower Monitoring Capability – Design Note 190

Jim Williams

Introduction

The LTC®1541 combines a micropower amplifier, comparator and 1.2V reference in an 8-pin package. The part operates from a single 2.5V to 12.6V supply with typical supply current of 5µA. Both op amp and comparator feature a common mode input voltage range that extends from the negative supply to within 1.3V of the positive supply. The op amp output stage swings from rail-to-rail. Figure 1 lists additional features along with a block diagram of the device. The part's attributes suggest low power monitoring applications and two such circuits are presented here.

Pilot Light Flame Detector with Low-Battery Lockout

Figure 2 shows a pilot light flame detector with low-battery lockout. The amplifier ("A"), running open loop, compares a small portion of the reference with the thermocouple-generated voltage. When the thermocouple is hot, the amplifier's output swings high, biasing Q1 on. Hysteresis, provided by the 10M resistor, ensures clean transitions, while the diodes clamp static generated voltages to the rails. The 100k–2.2µF RC filters the signal to the amplifier.

The comparator ("C") monitors the battery voltage via the 2M–1M divider and compares it to the 1.2V reference. A battery voltage above 3.6V holds C's output high, biasing Q2 on and maintaining the small potential at A's negative input. When the battery voltage drops too low, C goes low, signaling a low-battery condition. Simultaneously, Q2 goes off, causing A's negative input to move to 1.2V. This biases A low, shutting off Q1. The low outputs alert downstream circuitry to shut down gas flow.

SUPPLY RANGE: 2.5V TO 12.6V
$I_{QUIESCENT}$: 5µA
OP AMP V_{OS}: 700µV
COMPARATOR V_{OS}: 1mV
COMPARATOR HYSTERESIS: ±3mV
COMMON MODE RANGE: 0V TO (V_{SUPPLY} – 1.3V)
INPUT BIAS CURRENT: 1nA MAX, 10pA (25°C) TYP
REFERENCE: 1.2V ±0.4%

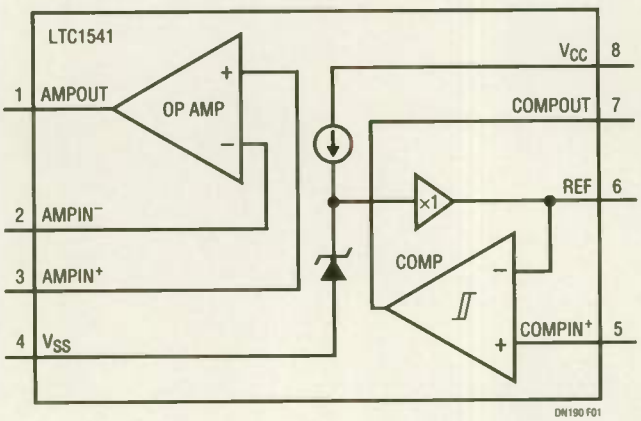


Figure 1. LTC1541 Block Diagram and Features of the Micropower Op Amp, Comparator and Reference

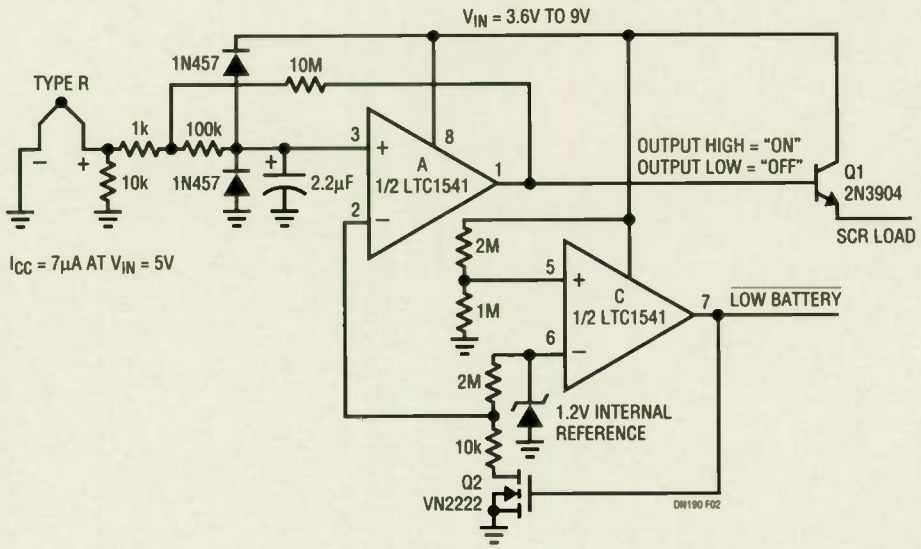


Figure 2. Pilot Light Flame Detector with Low-Battery Lockout

Tip-Acceleration Detector for Shipping Containers

Figure 3's circuit is a tip-acceleration detector for shipping containers. It detects if a shipping container has been subjected to excessive tipping or acceleration and retains the detected output. The sensitivity and frequency response are adjustable. A potentiometer with a small pendulous mass biases the amplifier ("A"), operating at a gain of 12. Normally, A's output is below C's trip point and circuit output is low. Any tip-acceleration event that causes A's output to swing beyond 1.2V will trip C high. Positive feedback around C will latch it in this high state, alerting the receiving party that the shipped goods have been mishandled. Sensitivity is variable with potentiometer mechanical or electrical biasing or A's gain. Bandwidth is settable by selection of the capacitor at A's input. The circuit is prepared for use by applying power and pushing the button in C's output.

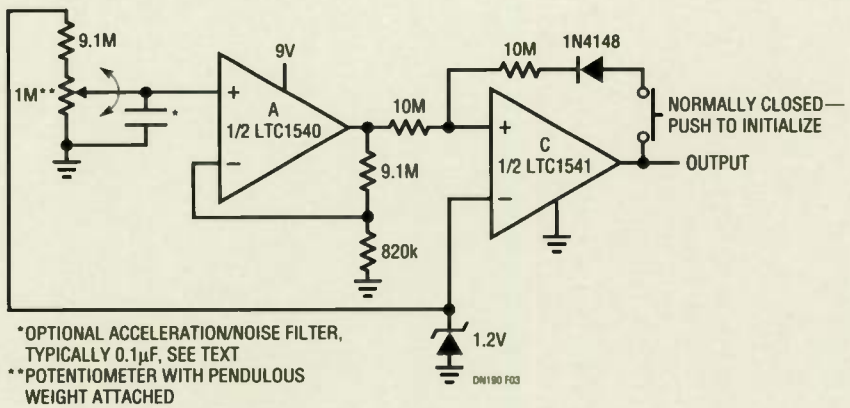


Figure 3. Tip-Acceleration Detector for Shipping Containers Retains Output if Triggered. Sensitivity is Adjustable Via Amplifier Feedback Values. Capacitor Sets Acceleraton Response Bandwidth

For literature on our Comparators,
call **1-800-4-LINEAR**. For applications help,
call (408) 432-1900, Ext. 2593

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408)432-1900 • FAX: (408) 434-0507 • www.linear-tech.com

dn190f LT/TP 0998 340K • PRINTED IN THE USA

WAY COOL!

BOARD INTERFACE SYSTEMS


ULTRA FINE PITCH


ULTRA HIGH DENSITY


ULTRA LOW PROFILE


ONE-PIECE INTERFACES


POWER TO-BOARD


MICRO CARD-TO-BOARD


RIGHT-ANGLE INTERFACES

Samtec **ULTRA HIGH DENSITY** interfaces with three-row, four-row, six-row and eight row designs are *Way Cool* ways to reduce your board size...

WAY FAST!

*Call **1-800-SAMTEC-9** for our new Board Interface Guide featuring a Full Line of micro and standard pitch systems.*

samtec

Samtec Sudden Service: *Information • Samples • Delivery*

SAMTEC USA • P.O. Box 1147 • New Albany, IN 47151-1147 USA
Tel: 1-800-SAMTEC-9 or 812-944-6733 • Fax: 812-948-5047 • Internet: www.samtec.com • E-mail: info@samtec.com

READER SERVICE 128

five-level-metal, 0.25-µm process technology to shrink features and boost performance. The devices trim propagation delay to just 3.5 ns—the shortest to date for a CPLD. Additionally, the small features allow the chips to operate from a reduced supply voltage of just 2.5 V. The I/O pins, however, can tie into systems with 3.3-, 2.5-, or 1.8-V logic interface levels, thanks to the MultiVolt I/O cell structure. The lower core voltage also reduces power consumption by an estimated 75% versus standard 5-V devices.

Packing In The Macrocells

Available with from 128 to 512 macrocells, the six devices in the MACH 5 family from Vantis offer designers from 68 to 256 signal I/O pins. Based on a 0.35-µm process, the devices have a t_{PD} of 7.5 ns across the entire family. That translates to a top operating frequency of 125 MHz. Designed for operation from a 3.3- or a 5-V supply, the circuits can be programmed with and interface with either voltage level. Additionally, the chips include a programmable power-down mode that reduces power drain when idling.

The older MACH 4 series offers from 32 to 256 macrocells, and propagation delays of 7.5 or 10 ns. These devices employ the company's novel SpeedLocking capability, which provides fast performance regardless of product-term loading or interconnect routing.

Recently, Vantis released details of its enhanced MACH 4 and MACH 5 families. Fabricated using a 0.25-µm process, the MACH 4A and 5A will sport shorter propagation delays—just 5 ns pin-to-pin for the MACH 4A series, 50% better than the initial versions, and 6 ns for the MACH 5A, a 20% improvement.

The architecture of the MACH 5 consists of multiple PAL blocks interconnected with a two-level hierarchy of metallization. The first level, called the block interconnect, groups four PAL blocks to form a segment. The second level, the segment interconnect, ties a number of segments together. Therefore, the only difference between any two MACH 5 devices is the number of segments on the chip.

The PAL block used by the MACH 5 contains 16 macrocells, a programmable-AND/fixed-OR matrix to generate the product terms, a logic allocator, 16 I/O cells, and logic to generate the output-enable and register-control signals. I/O cells associated with a PAL block have a path directly back to the block (local feedback). However, if the I/O signal is used in another PAL block, the interconnect feeder array (a switch matrix) assigns a block interconnect line to that signal.

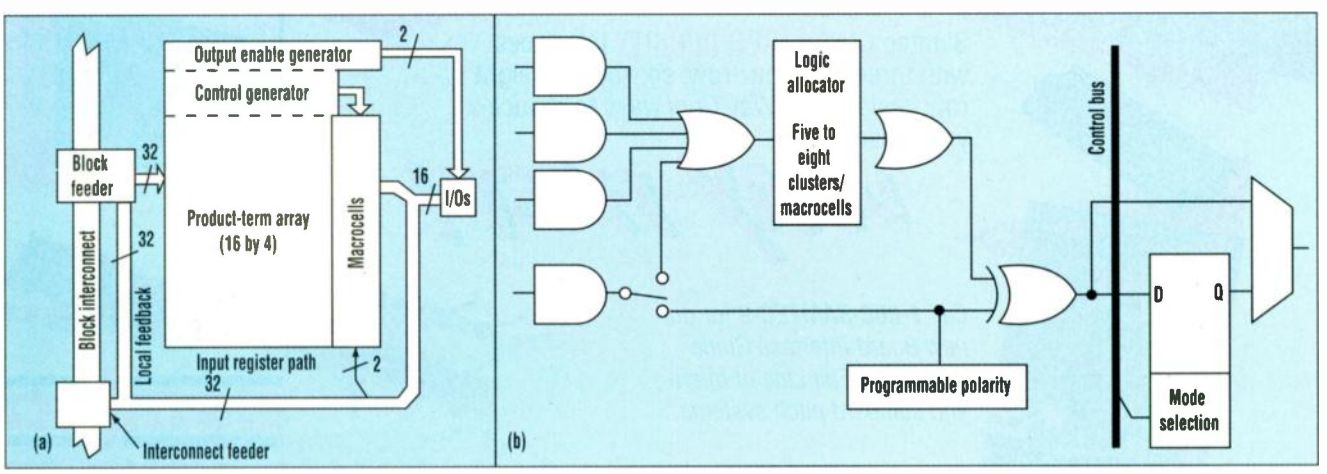
Within the PAL block, a logic allocator assigns product terms to the macrocells. Up to eight clusters of four product terms can be steered to one macrocell, and product terms can be steered in basic clusters of three or four. This process replaces the output-switch matrix typically used in other CPLDs to reroute signals and retain the pinout *(Fig. 3)*.

The XC9500 family from Xilinx also offers some high-performance options, thanks to its 5-ns pin-to-pin propagation delays and maximum operating frequency of 125 MHz. The six devices range in density from 36 to 288 macrocells, and from 34 to 192 I/O pins. The newest member is the XC95144, a 144-macrocell device (about 3200 usable gates) with a 7.5-ns t_{PD}.

It's the first device fabricated on the FastFlash 0.5-µm process used by Xilinx's latest foundry, United Semiconductor Corp., Hsin-chu, Taiwan. The new process shrinks the chip area by 50%, compared with devices made with the existing 0.6-µm process. All other XC9500 devices will eventually be transitioned to the new process.

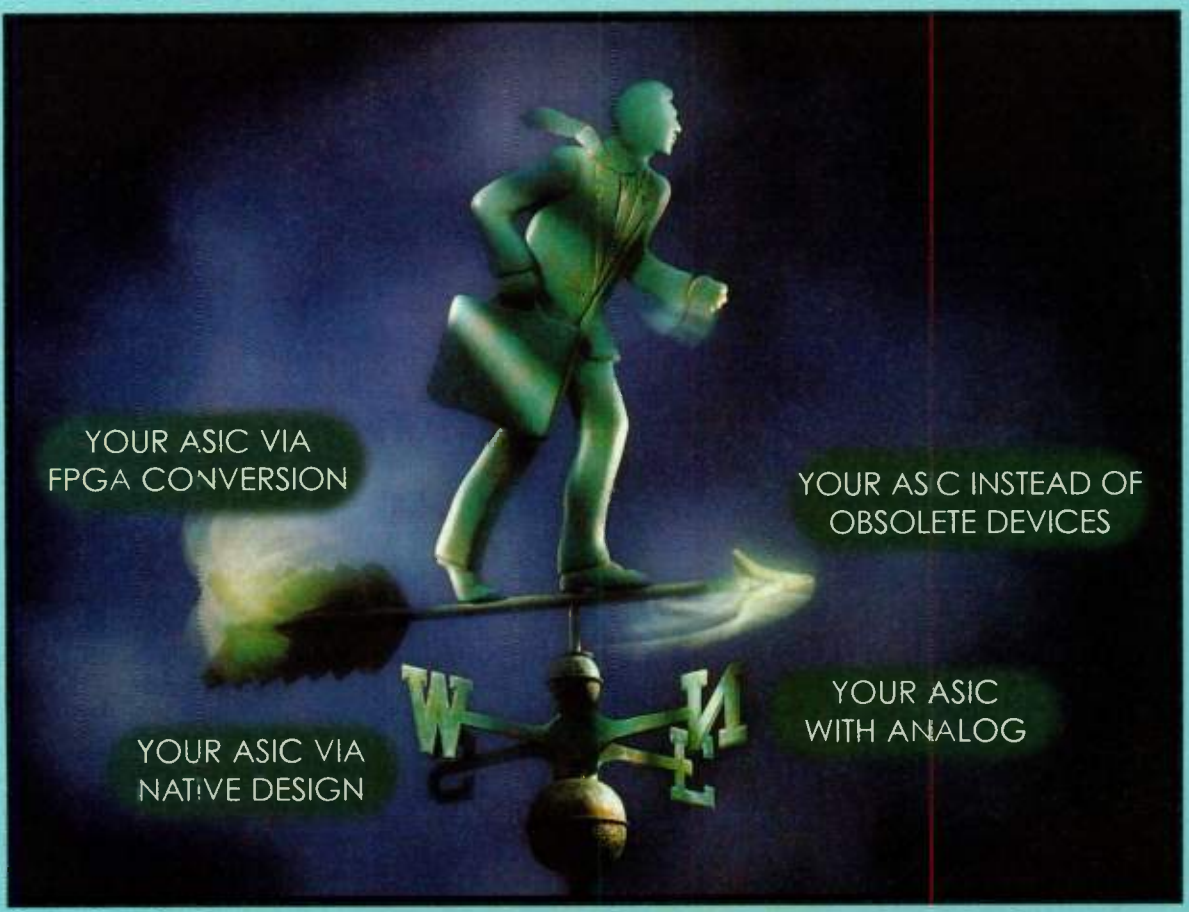
Inside the XC9500 devices are multiple function blocks, each of which is like a large PAL device, in this case, a 36V18 (with 18 macrocells and 36 inputs). The function block provides 90 product terms from a programmable AND array. Those terms are generated from the 36 inputs (plus 36 complement signals) at the FastConnect switch matrix that interconnect all the cells. The product terms can drive any or all of the 18 macrocells in the block.

Designers can configure each macrocell individually for a combinatorial or registered function. Each cell includes five direct product terms from the AND array. These can be used as primary data inputs (to the



3 At the heart of the Vantis MACH 5 series is a PAL-like logic block that contains a product-term array and 16 macrocells (a). Each macrocell contains a storage element, an XOR gate, a control bus, and routing resources (b). The XOR gate can be used for logic or polarity control.

ORBIT GETS YOU & Your ASIC THERE



IN ANY WEATHER ...

- **300,000 USEABLE GATES**
- **MULTIPLE SYNTHESIZABLE CORES**
- **ANY VOLUME**
- **LOW NRE**
- **OVER 1500 CONVERSIONS**
- **QUICKTURN PROTOTYPES**
- **ANALOG CAPABILITIES**
- **SHORT PRODUCTION CYCLES**

Orbit offers a full line of gate arrays to satisfy your digital design needs. Additionally, Orbit's ***Mixed-Signal*** and ***Foundry Services*** complement that effort and can assist you in mapping out your next project.

Call Orbit for more information on keeping your design on course, or visit our website at www.orbitsemi.com.

ORBIT
SEMICONDUCTOR, INC.
A Dii GROUP COMPANY

Orbit Semiconductor Inc. 169 Java Drive, Sunnyvale, CA 408 744-1800; FAX 408 747-1263

READER SERVICE 122

OR and XOR gates) in the cell to implement combinatorial functions, or as control inputs, such as clock, set/reset, and output enable. The product term allocator with each macrocell selects how the five direct terms are used. Also, the flip-flop in the cell can be configured as either a D- or T-type device, or can be bypassed when the cell is used for combinatorial functions.

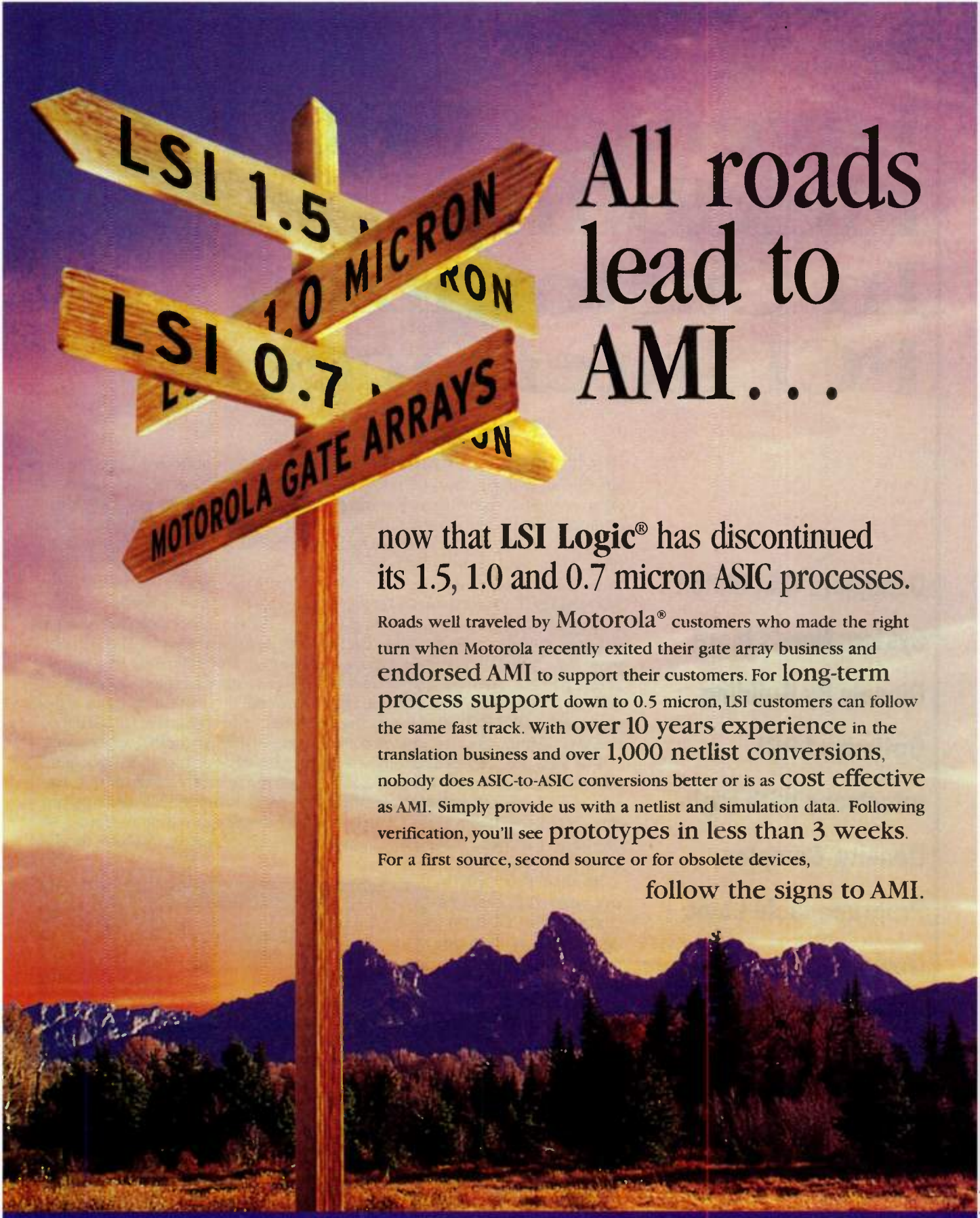
Unlike many other CPLDs, which offer 4- or 8-mA drive capabilities on the I/O pins, the XC9500 familiy can drive loads of up to 24 mA on each output. And, designers can configure the I/O cells to interface with either 3.3- or 5-V systems. To reduce system noise, the circuits include user programmable ground pins. Like most of the other CPLDs, the cells have a programmable slew rate to reduce signal noise generated by sharp edges.

The last of the standard CPLD families, the ATF1500 from Atmel, delivers up to 256 macrocells and maximum propagation delays of 10 ns (in the ATF1516AS/L). The circuits offer five product terms per macrocell, but that can be expanded to 40. Each macrocell includes a flip-flop that can be configured as a D, T, or latch-style element, and has both global and individual register control signals, global and individual output-enable signals, a programmable output slew rate, and a programmable output open-collector option.

Power management features keep idle power levels low. An "L" version consumes less than 3 mA on standby, while a pin-controlled stand-by mode drops current drain to 4 mA from the over 200 mA drawn when active.

In addition to the CPLDs that are *only* CPLDs, WSI has crafted a unique series of programmable system devices that incorporate about 3000 gates of programmable logic, several kilobytes of SRAM, port expansion signals, and even a host processor interface. The PSD family includes flash-based devices with a zero-power standby mode, and devices with various feature combinations. Such devices make very tightly coupled peripheral support components for devices like microcontrollers and digital-signal processors.

The breadth of CPLD architechtures and densities now gives designers a wide array of options for their systems. Technology choices have also increased as the CPLD manufacturers add new configurations—such as the use of SRAM in addition to the now-common EEPROM/Flash-based devices. Additionally, even higher-density devices are on the horizon. Densities of between 50,000 and 100,000 PLD gates are expected by the turn of the millennia, as manufacturers move toward finer-line processes. And, that will allow the CPLDs to tackle even larger pieces of the system logic.



All roads lead to AMI...

now that **LSI Logic**® has discontinued its 1.5, 1.0 and 0.7 micron ASIC processes.

Roads well traveled by Motorola® customers who made the right turn when Motorola recently exited their gate array business and endorsed AMI to support their customers. For long-term process support down to 0.5 micron, LSI customers can follow the same fast track. With over 10 years experience in the translation business and over 1,000 netlist conversions, nobody does ASIC-to-ASIC conversions better or is as cost effective as AMI. Simply provide us with a netlist and simulation data. Following verification, you'll see prototypes in less than 3 weeks. For a first source, second source or for obsolete devices,

follow the signs to AMI.

(800) 639-7264 dept.**9163** • **www.amis.com/9163**

AMI
AMERICAN MICROSYSTEMS, INC.

READER SERVICE 127

Leverage CPLD Flexibility In Customized PCI Interfaces

Designers Can Match System Needs More Closely By Building Optimized PCI Interfaces With High-Density, Complex Programmable Logic Devices.

RICH KAPUSTA
Cypress Semiconductor Corp.

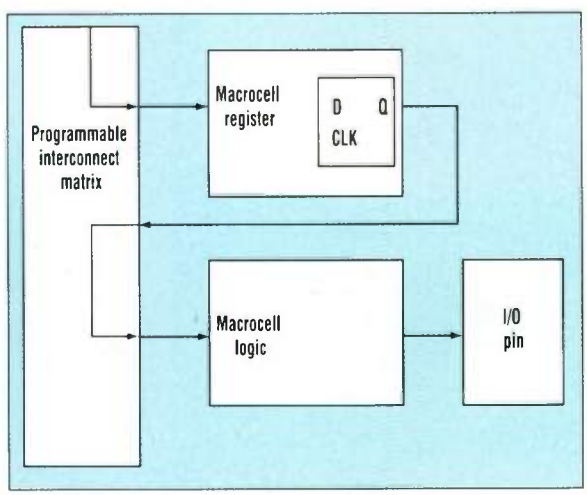
Although developed specifically for the PC industry, the peripheral interconnect bus (PCI) tackles everything from desktop peripherals to advanced network switches. For industrial or communications systems, which often use proprietary solutions, designers don't have to maintain 100% PCI bus compliance. There, programmable logic devices (PLDs) offer tremendous flexibility, allowing designers to implement just the right combination of PCI features. The challenge, however, is to find a PLD with the performance required for full-speed PCI transactions, and enough logic capacity to handle the functions.

Historically, field-programmable gate arrays (FPGAs) have been big enough, but until recently, were too slow. On the other hand, complex PLDs (CPLDs) were fast enough, but until recently, were too small. However, over the last two years, FPGAs have speeded up, and CPLDs have grown larger, so designers have an abundance of devices from which to choose. But while both types of devices can handle a PCI implementation, the recent improvement in CPLD densities, and their intrinsic features, make them very attractive for PCI applications.

For instance, CPLD architectures are inherently good for state-machine-based designs, and many areas of a PCI design can take advantage of this. Another CPLD advantage is that performance is predictable, and remains constant throughout the design cycle. CPLDs also have abundant routing resources, so meeting a particular pinout, or using all of the logic resources available is relatively straightforward.

To show how CPLDs can be used to create a customized PCI interface, let's examine the design of a simple application that can be implemented with 128 macrocells. Larger CPLDs can also be used for PCI designs with more functionality, such as initiators or designs that incorporate more of the system logic on the chip. Soon, when CPLDs incorporate on-chip memory blocks, designers will be able to implement an entire PCI interface, including FIFO memory.

Designers must consider several issues



1 A single pass through the logic of a CPLD flows from the programmable interconnect matrix through the macrocell register, back into the programmable interconnect matrix, and out again into the macrocell logic, and finally out through an I/O pin. Going through a macrocell combinatorially constitutes a pass of logic.

when implementing PCI applications in programmable logic. The demands of PCI require high speed, generous routing resources, high I/O count, pinout flexibility, and a consistent-performance timing model.

Compliance with the 33-MHz PCI specification demands a set-up time no longer than 7 ns. In many implementations, especially in FPGAs, the fanout requirements for the address and data buses affect set-up time. One solution is to capture the address and data values in a register at every clock cycle, then route them to where they're needed. However, this adds a clock cycle of latency. A key advantage of CPLDs is that their performance specification doesn't depend on the fanout. So the system can maintain the 7-ns set-up requirement regardless of where the address and data bus signals go.

Next, bused signals must be driven valid between 2 and 11 ns after the clock signal. In FPGAs, many delays contribute to a signal's total clock-to-output delay. These include clock-to-Q logic paths, routing, and I/O buffer delays. Often, they can add up to more than 11 ns, which would then require a wait-state to be added to the PCI interface. However, because most CPLDs have a fixed-delay timing model, they can easily propagate an output from a register to an output pin in less than 11 ns. This is done regardless of the routing, while incorporating an entire "pass" of logic *(Fig. 1)*. In fact, most CPLD datasheets guarantee this timing delay, typically referred to as t_{CO2}.

Another critical requirement is that the PCI device must respond to a transaction within three clocks after the address phase. If the PCI initiator does not get a response within four clock cycles, it will abort the transaction. In fact, the PCI device can respond as early as one clock cycle. This is called a "fast-response" device. Remembering that it has to meet a 7-ns set-up time, most programmable logic implementations fall into the medium or slow (two- or three-clock-cycle response) categories. By using a CPLD, designers get performance that is both fast and predictable. Additionally, CPLDs can perform a large number of logic operations within one pass of the device (or one clock cycle).

The ability to handle high-fanout signals is yet another important characteristic. Many signals within the PCI interface must be routed to 36 or more signal nodes simultaneously. This can cause significant loading problems for most FPGAs, so some type of buffering, duplication, or special routing must be used to handle these signals. Such additional support complicates the implementation significantly. However, most CPLDs have fanout-independent routing, so routing a signal to 36 nodes is no problem. Any signal from a pin or macrocell within a CPLD can be routed to as many places as needed with no change in device performance.

With most of the baseline conditions now established, let's examine the design of a PCI target interface using a CPLD containing 128 macrocells (in this case a Cypress Ultra 37128). This version can hold the smallest possible PCI target design, and allows engineers to craft a cost-effective solution while maintaining high performance and flexibility.

The design was entered using VHDL (Cypress' Warp2 development tool) with no device-specific structural components. The custom application ties into the PCI bus through a generic user interface that can easily be customized by modifying the VHDL source code. The design performs the protocol interactions of a PCI target interface (TRDY, DEVSEL, and STOP signals), throttles the data bus between PCI and the user interface using two-cycle reads and one-cycle writes, includes an address counter for bursts, and determines transaction hits.

This design targets the smallest CPLD possible. It does not implement a parity generator or the configuration space registers. The designer could implement both of these functions on a separate device, leaving the CPLD to focus on the most essential, and usually most challenging, part of PCI interfacing: the control logic *(Fig. 2)*. A minimum PCI target design incorporating parity generation and configuration space registers requires approximately 140 macrocells in a CPLD. Using a 192- or 256-macrocell device would leave sufficient resources for custom logic.

The design also includes an external FIFO memory to handle memory-write operations. This reduces latency, as the CPLD generates all FIFO control signals. Thus, the PCI target interface implements writes in 2-1-1-1 bursts, and reads in 2-2-2-2 bursts. To select between user-application data and configuration-space data, the CPLD generates a mode signal to switch between the two bidirectional data buses.

Different applications will require different size address spaces. Modifications of the VHDL design description to match these needs are expected when implementing PCI in a PLD. Because a device's address space is determined by the number of hardwired zeroes in the lower bit positions, decreasing the address space

Code Listing

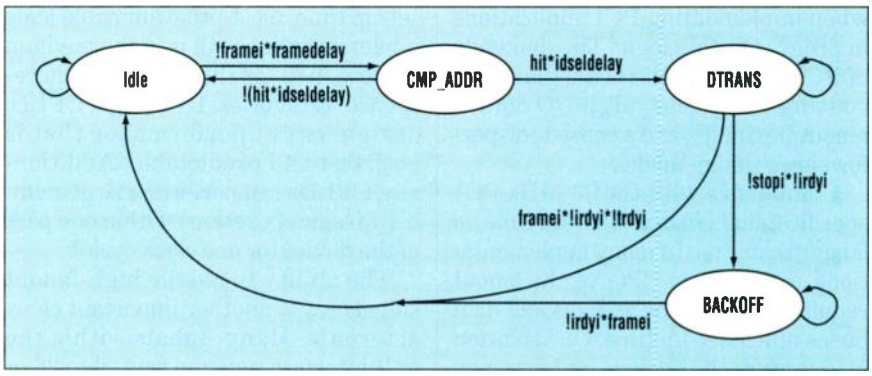
```
ac: process (clk,rst)
begin
        if(rst='1')then
                usraddr<=b"00000000000000";
        elsif(clk'event and clk='1')then
                if(state=IDLE)then
                        usraddr(15 downto 2 )<=pciad(15 downto 2);
                elsif(
                        (state=DTRANS and mem_write='1' and fifowrite='0')or
                        (state=DTRANS and mem_read='1' and
                                ztrdyi0'0' and irdyi='0')
                        )then
                        usraddr<=usraddr + 1;
                else
                        usraddr<=usraddr;
                end if;
        end if;
end process;

address(15 downto 2) <= usraddr(15 downto 2);
address(1 downto 0) <= b"00";
```

size actually increases the resources required in a PLD. The reason is that hard-wired zeroes require minimal resources within a CPLD device, while address bits must be stored in the macrocell registers of a CPLD.

Decreasing the number of hard-wired zeroes also increases the address-compare portion of the design, because more real bits need to be compared. Changing the address space can also impact the address counter used for burst reads and writes.

Another possible modification to the PCI design is the support of aborts and retries. This logic would be added to the control block, and would need to recognize the REQ_ABORT and REQ_RETRY signals. Finally, designers can replace the FIFO memory with internal registers within the device. The number of bits stored will affect the resources required for the PCI design.

The input registers at the PCI address/data bus continuously capture data on every clock cycle. As soon as the state machine transitions to the CMP_ADDR (compare-address) state, the control logic knows that the address of a new transaction is contained within the input registers. This data is used to determine a transaction hit in the AddrCompare block, and is captured in the AddrCounter block. In parallel, the command-decode logic determines which (if any) of the internal command flags should be raised.



3 When the PCI target interface waits for a request, it stays in its idle state; when a request comes in, it will enter one of three other states depending on the conditions of several signals.

For write transactions, when the state machine is in the TDATA state, the data-input register provides write data to the user data bus. The active-low FIFOWRITE signal is asserted when data on the user bus is valid, and should be taken on that clock cycle. The data is available for one clock cycle only, and must be taken at any clock during which the FIFOWRITE signal is asserted.

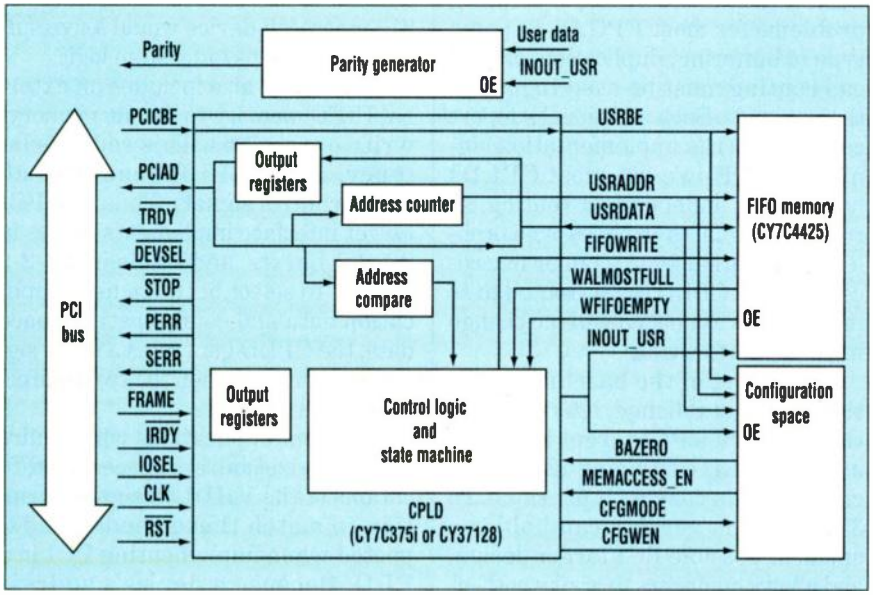
For read transactions, the data buses from the user ports are routed to the PCI data bus. On the user interface, the address bus contains the address of the desired data. The user must produce the data as soon as possible (approximately 10 ns). If more time is required, additional wait states may be introduced. This is accomplished by modifying the TRDYIVAL equation. The high-impedance outputs of the user read-data-bus are controlled by the INOUT_USR signal. INOUT_USR in the high state indicates a write operation, which disables the user output drivers.

Finally, the mode of the transaction is reflected by the CFGMODE signal. When it is in the high state, the external configuration-space device responds; when in the low state, the user device responds.

The state machine within the PCI target design is the primary control circuit. Basically, the state machine remains in the idle state until it determines that the PCI initiator is attempting to interface to this target device. From there it moves to one of three other states as determined by various conditions *(Fig. 3)*.

When the PCI bus is inactive, or the transaction on the PCI bus does not involve this particular target, the state machine remains in IDLE. Here, the C/BE bus is predecoded to assert the appropriate internal command mode. As soon as a new transaction is initiated (the $\overline{\text{FRAME}}$ signal is asserted in this state), the state machine will move to the CMP_ADDR state.

In the compare-address state, the logic uses a two-stage, pipelined comparator to determine transaction hits. The first stage is completed in IDLE, and the second stage is completed in the compare-address state. If an address hit is determined, then the state machine will move to DTRANS, oth-



2 The CPLD implementation of a PCI target interface, using a device with 128 macrocells, requires that the parity generation, FIFO memory, and configuration space registers be located off the chip. Although this results in a multichip solution, it allows designers to optimize the interface for their system.

erwise it will return to IDLE.

All PCI read and write data transfers occur in the DTRANS state. The state machine will remain here until the last transfer takes place ($\overline{\text{TRDY}}$ and $\overline{\text{IRDY}}$ are asserted, $\overline{\text{FRAME}}$ is de-asserted), or a disconnect is signaled by the target ($\overline{\text{STOP}}$ is asserted, and known to be recognized by the initiator because the $\overline{\text{IRDY}}$ signal was also asserted). For these cases, the state machine will move back to IDLE or BACKOFF, respectively.

The state machine will change to BACKOFF when the initiator recognizes that the target is signaling a disconnect ($\overline{\text{STOP}}$ and $\overline{\text{IRDY}}$ both asserted). In this state, the target waits for the initiator to complete the transaction. The initiator will assert $\overline{\text{IRDY}}$ and de-assert $\overline{\text{FRAME}}$ to terminate the transaction. When this occurs, the state machine moves back to IDLE.

Although the VHDL code describing the PCI target design can be used in any VHDL synthesis tool, the particular code shown in this article is intended for use with the Cypress Warp2 VHDL development system. The VHDL design is divided into several sections: state machine, output registers, three-state I/O logic, pipeline registers, signal equations, data-path, address-compare block, and address counter.

CPLD architectures in general appear to be inherently better at implementing state-machine designs than their FPGA counterparts. This is true for several reasons:

- The product-term logic implements equations in sum-of-product form, which is the natural, optimal form for state-machine designs.
- CPLDs have a higher logic-to-register ratio than FPGAs. That simplifies the design because most state machines require more logic than registers, especially when using sequential encoding.
- CPLDs have a fixed-delay timing model. This allows state-machine equations to run at a predictable frequency regardless of the routing or the logic in between. Another important aspect of the fixed-timing model versus FPGAs is that design changes in the CPLD implementation will deliver the same predictable performance.

To meet the PCI specification, remember that clock-to-output delays must be between 2 and 11 ns. In a CPLD implementation, this is done by registering all of the PCI bus-control signals, and updating them on every clock cycle. At reset, the signals are preset to a logic high.

Furthermore, the PCI specification dictates that the PCI-bus data and control signals must not drive the bus when not actively participating in a transaction. This is easily implemented in a CPLD using the output-enable product terms at each I/O cell. In some architectures, such as the Cypress

CPLDs, these product terms are dedicated to performing output enable. Thus, they don't take logic resources away from the rest of the design.

To deal with the pipeline registers and signal equations in the VHDL design, the code simply has to register necessary signals and define the logic equations for all internal and external PCI signals. The Warp2 development software can then optimize the equations for the CPLD architecture, and provide a summary of the final implementation in a report file.

The output-data bus path is also registered to meet the timing requirements of PCI. When wait states are induced by the initiator ($\overline{IRDY}$ is sampled, de-asserted), the data path must be halted until the initiator is again ready to accept data. The VHDL code must also describe that behavior as well as provide registers for the data, byte enables, and a write-enable signal to the FIFO memory.

To recognize ownership of an initiated transaction, PCI target devices must latch the address on the PCI bus, and compare it to the contents of their base address register (BAR) to determine a match. The CPLD implementation performs a bit-to-bit equality comparison of the address and the BAR value. This produces a product-term-based solution that requires only two passes through the CPLD.

The final section of the VHDL design description is the address counter. During burst transfers, the target device must increment the address; this target design uses a 14-bit counter (counts on double word boundaries) to perform that task. The counter is loaded whenever the state machine is in IDLE (in anticipation of a new transaction), and is incremented whenever data is transferred.

The inclusion of a T flip-flop in each macrocell makes CPLDs inherently good at implementing binary counters. The CPLD's architecture allows it to implement fully loadable counters that can operate at well over 100 MHz. And a benefit to designing with VHDL is that the counter's description is simple and straightforward *(see code listing)*.

This design, although it provides only a basic target-PCI interface, can be embellished with larger FIFO memories to improve the data transfer efficiency. Also, a larger CPLD would allow the designer to include more system logic functions and to implement a PCI initiator interface, which would require several thousand additional gates of logic.

RICHARD KAPUSTA is strategic marketing manager for PLDs at Cypress Semiconductor. Kapusta received a BS in computer science from the University of Illinois at Urbana-Champaign. He can be reached at Cypress Semiconductor Corp., 3901 N. First St., San Jose, CA 95134; (408) 943-2600.

Use In-System Programming To Simplify Field Upgrades

The Latest Complex Programmable Logic Devices Help Designers Reduce System Upgrade Costs And Speed Time-To-Market

JESSE H. JENKINS,
Xilinx Inc.

One of the more important features designers look for these days is the ability to handle both planned and unplanned logic changes as system development progresses, and even after systems have been shipped. By incorporating the latest complex programmable logic devices (CPLDs), designers get this flexible logic capability. These CPLDs have even evolved to the point where they're supplying significant logic resources (many thousands of gates) to support system designs, just as their smaller brethren, the PLDs, did.

The growing need for in-system programming (ISP) capabilities, especially after systems have been shipped, stems from two key issues. First, time-to-market pressures often don't let manufacturers fully test systems. That means hardware anomalies may reach the field. If the system supports ISP, a field-service technician, or even the customer, can download new configuration information without taking the system apart. That reduces the cost of "servicing" the equipment. Second, feature upgrades often can be done in much the same way. Using the ISP capability, the logic could be reconfigured to add new functions or speed up existing functions.

Early CPLD architectures were not designed with ISP field upgrades in mind. However, the latest offerings from various suppliers provide robust architectures and, in a few cases, the ability to update individual sections of the CPLD. Supporting a wide range of change options suggests the need for a "finer-grain" organization than most CPLDs provide, but some of the latest CPLD designs do provide a finer-grained architecture.

Another aspect of robust architectural design includes the ability to redirect a product term from one macrocell to another, at the single-product-term level (rather than groups of product terms). Having an abundance of product terms, as well as global resources, such as clocks, sets, resets, and three-states, is another important capability. Local inversion control and independent macrocell clocking are other features that further improve the flexibility of ISP.

Software Requirements Too

Beyond the architecture are the software requirements. These include careful budgeting of resources (p-terms, clocks, etc.) when assigning position-sensitive functions within a CPLD function block. By spreading resources around and retaining pockets of functional capability, the design software delivers significant extra flexibility for making future changes.

Underlying both the architecture and software is the device technology, which must support an arbitrary number of reprogramming cycles—frequently termed "endurance." CPLD suppliers have already moved away from nonvolatile, ultraviolet-erasable EPROM technology, and every CPLD supplier now offers devices that employ some type of flash- or EEPROM-based configuration scheme.

Thus, a key factor in selection becomes the chip's endurance. Xilinx CPLDs, for example, currently allow 10,000 reprogramming cycles, allowing wide lati-

tude for future design changes without impacting device speed or reliability. Most other vendors have opted to provide lower endurance guarantees (that is, 100 cycles), supported by the argument that anyone can get a design right in 100 attempts, and might only have to do one or two final updates.

That argument would be acceptable if the 100 attempts were only for the CPLD, and typically only if the device is used for prototypes or product development. However, the most frequent development model today is the single-controller model, in which all reprogrammable devices (SRAM, SDRAM, flash memory, FPGA, and CPLD) reside on a common JTAG download chain. To simplify on-board logic, these systems use a strategy to "reprogram everything when anything changes." To simplify matters further, the CPLDs and FPGAs are also changed even when any software update (SRAM/flash memory) occurs. In this situation, it is questionable whether even 1000 programming cycles will suffice.

Supporting Changes

Finally, all components must play together to deliver pinout retention or "pinlocking." That's the ability to retain device pinouts, therefore avoiding pc-board wiring changes for all but the most complex design changes. Where many designers get into trouble is with small changes, such as adding a p-term to an equation, inverting a signal, or adding an input to an existing p-term. When CPLDs can't support this kind of change while maintaining the previous pinout, the value of the CPLD becomes questionable. For ISP to be useful, the architecture and software must be designed to maintain pinouts for multiple design edits. Field upgrades without ISP and pinlocking have no real value, especially when older EEPROM architectures are employed.

When designing a system with CPLDs, engineers typically encounter three basic types of field upgrades:

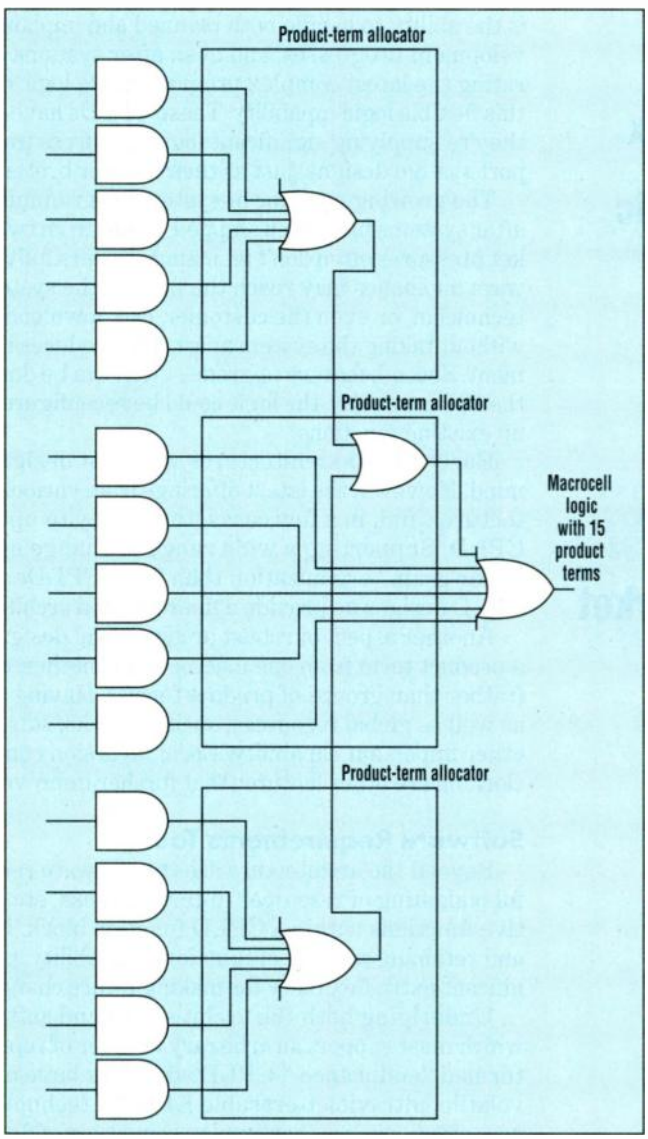
Compensating: This can be also thought of as correcting a design error due to inaccurate system knowledge. Such an approach is frequently found in data-processing applications, as today's designers confront a massive challenge when they start to design with a new CPU or other logic part prior to actually using it.

For example, the datasheets for popular microprocessors easily exceed 100 pages, and synchronous DRAM datasheets exceed 30 pages. Therefore, there's plenty of room for unexpected behavior in a design, simply due to inaccurate system knowledge. A classic situation would be misunderstanding whether data was available on a leading or falling edge of a clock. Frequent interrupt or direct-memory access (DMA) request conditions are vague enough to be sites where a few product terms may be needed to correctly cover the requesting condition.

Adding capability: An example of this case is a board that was developed with software to operate over a target address range. However, a new version is then created to expand the memory space with new applications. But board demand requires that the new version be shipped early without the appropriate software debuggging for the new applications and memory range.

After the board has shipped—and the impact of the new applications is fully understood—a field upgrade can be used to increase the address range. Typically, this involves enabling additional memory modules and adjusting the appropriate timing signals to support the additional memory (control signals, wait states, etc.). To obtain a faster response with newer memory chips, designers may need to involve the elimination of wait states or early enabling (via clock-phase adjustment).

Planned changes: These can cover a myriad of topics. For example, in the past, board customization was a standard capability. Simple things like a font enhancement to a high-end printer were implemented by a service technician making a visit, opening the printer and setting a couple of dip switches. Today, that change would involve simply attaching an external cable and



1 A typical CPLD-based design that often must be expanded is a wait-state generator like this one, which takes 15 product terms and delivers a single output that drives the microprocessor's wait input.

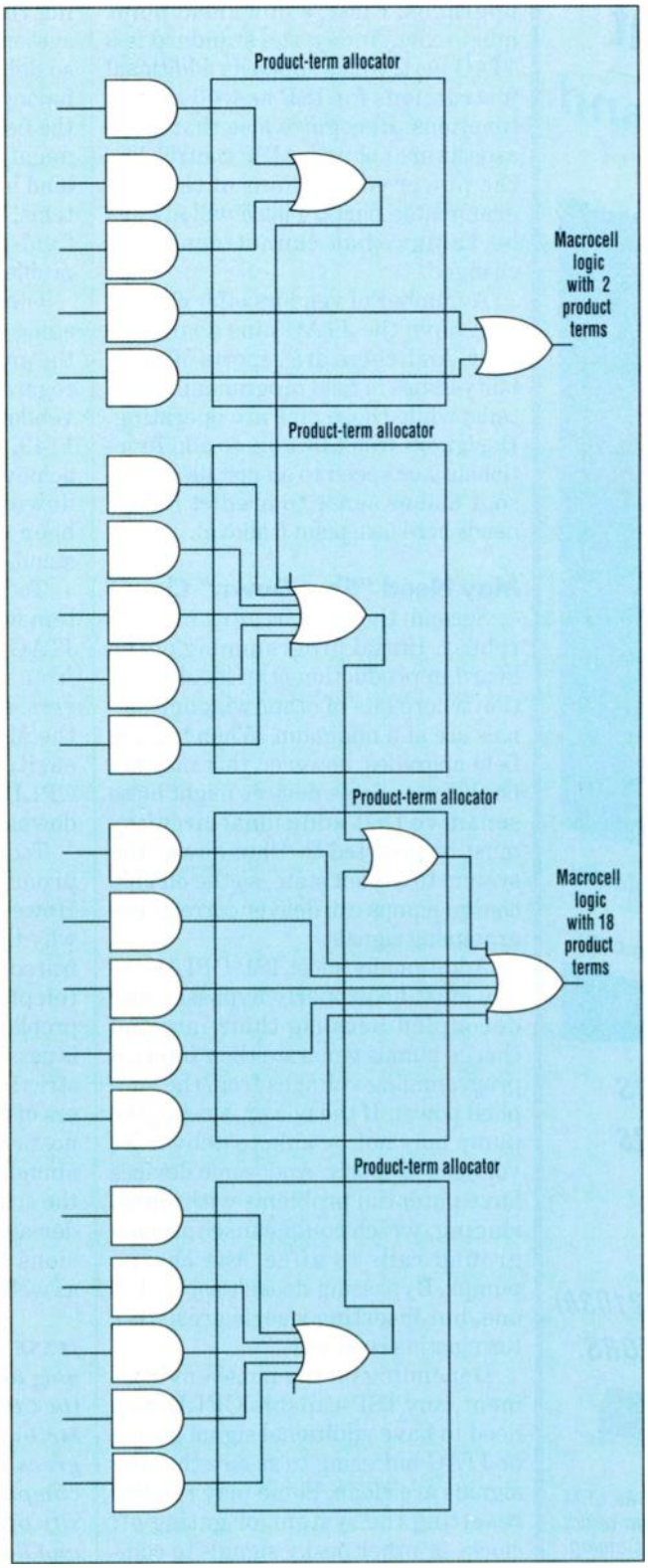
downloading the new pattern to the appropriate programmable device. And, it would not require a visit from a technician.

To gain a better understanding of how some of these techniques are applied, let's examine a specific example of an upgrade to a board that was installed in a system while in the field. Part of the board's circuitry includes an implementation of a standard microprocessor wait-state signal generator *(Fig. 1)*. Here, most of the XC9500 macrocell logic is not shown (that is, no flip-flops or extra gates).

The circuit focuses on delivering 15 product terms worth of logic to an output pin, which drives the microprocessor wait input. At field-upgrade time, an additional I/O board is added to the system, warranting a change in the wait-state logic to account for the new board.

To compensate, three more product terms must be added *(Fig. 2)*. The top macrocell site must retain two product terms at the existing site, but does have three available p-terms to forward down to the wait-state site to augment the previous tally to 18 p-terms. Bidirectional p-term assignment, along with individual p-term resolution, makes this sort of upgrade very easy in XC9500 CPLDs, while retaining the original design pinout.

Other applications of the same, basic field upgrade could include making coefficient changes on DSP filters, enabling (or even creating) I/O ports or adding test circuits. Although not strictly a "field upgrade," last-minute board configurations prior to shipment are similar to field upgrades. In this case, there may be multiple configurations of a single board sold as different products. The company can inventory one product, then make last-minute changes to reconfigure and test the "standard" product on a demand basis.



2 The addition of three p-terms to the wait-state generator is a minimal circuit change, but if the PLD can't easily handle the addition/sharing of the p-terms, it may force a change in the external pin assignment. That would force an alteration to the printed-circuit board's layout—something most system designers would consider unacceptable.

Planning Needed

Designing for field upgrades demands sound planning. First, engineers must select the right CPLD to ensure that functional and architectural resources exist for the future. This not only means adequate gates and flip-flops for a field upgrade, but also, available CPLD connection paths. Likewise, it's vital to use design software that reserves function and connection resources for future changes. Anticipating the need for higher speeds in the future is equally important.

Here are some guidelines that are appropriate for the XC9500 CPLDs, as well as for other manufacturers' CPLDs:

- Choose a CPLD family with a good pinlocking architecture.
- Select a part that meets current design requirements with speed to spare.
- Choose a part with ample remaining capacity (headroom) if significant field upgrades are expected in the future.
- Direct the design software to distribute logic resources.
- Check that connection resources remain, so future paths can be found.
- If capacity exceeds 90%, and speed is near the limit, consider the advantage of a larger or faster pin-compatible part. This will minimize future risk.

A number of other practical issues exist, and understanding them can reduce risks and ensure successful field

upgrades. First, a download point must exist. Today, the standard is a JTAG port, which supports additional instructions for ISP as well as test functions. Recognize also that some aspects are not under ISP control, like the power connections of the programmable parts. There will always be things that cannot easily be changed.

A number of vendors offer circuits that have the JTAG pins do double duty. And, there are reports of reliability issues in field programming systems while those pins are operating. Designers won't be able to add functionality or speed to an installed part, so it makes sense to predict future needs here (see point 6 above).

May Need "Shut-Down" Circuit

Second, the ISP circuitry must be robust. Initial programming of the board in production is an ideal situation where lots of other wiggling signals are at a minimum. When making field upgrades, however, that may not be the case. Some devices might be so sensitive that additional circuitry must be inserted to "shut down" the system to a quiet state, so the on-chip charge pumps can deliver correct programming signals.

Additionally, most ISP CPLDs today must be properly bypassed and decoupled because their internal charge pumps generate their internal programming voltages from the supplied power. If the power is noisy, the pump may not be able to deliver its voltages properly. And, some devices have potential problems with signal ringing, which could cause internal ground rails to affect the charge pumps. Bypassing doesn't solve that one, but inserting a series resistive termination reduces it.

Depending on the noise environment, any ISP-capable CPLD may need to have additional signal gating or JTAG buffering to assure that the signals are clean. Some may require resetting the system, or gating off clocks or other pesky signals to complete the ISP operation. Each system is different.

One interesting, practical payoff is that, with sufficient planning, field upgrades can often occur without opening the box. This greatly improves system reliability. Some systems are so delicate that they cannot tolerate having their boards loosely seated by the field technician, or they may react negatively to a screwdriver left behind inside the chassis. For those systems, having an externally accessible field-upgrade port solves a critical problem.

Other practical limitations to leveraging ISP capabilities revolve around the present lack of industry standards regarding the devices. Although many vendors are working with the IEEE-1149.1 subcommittee on ISP to achieve practical standardization for downloading, no standard has yet been released, and, in fact, several standards may evolve.

Today, it's common to see one system with as many as three different JTAG download cables being driven from three download software drivers. For Xilinx programmable logic, the M1.5 JTAG download software easily handles Xilinx FPGAs and CPLDs from one utility and just one download cable.

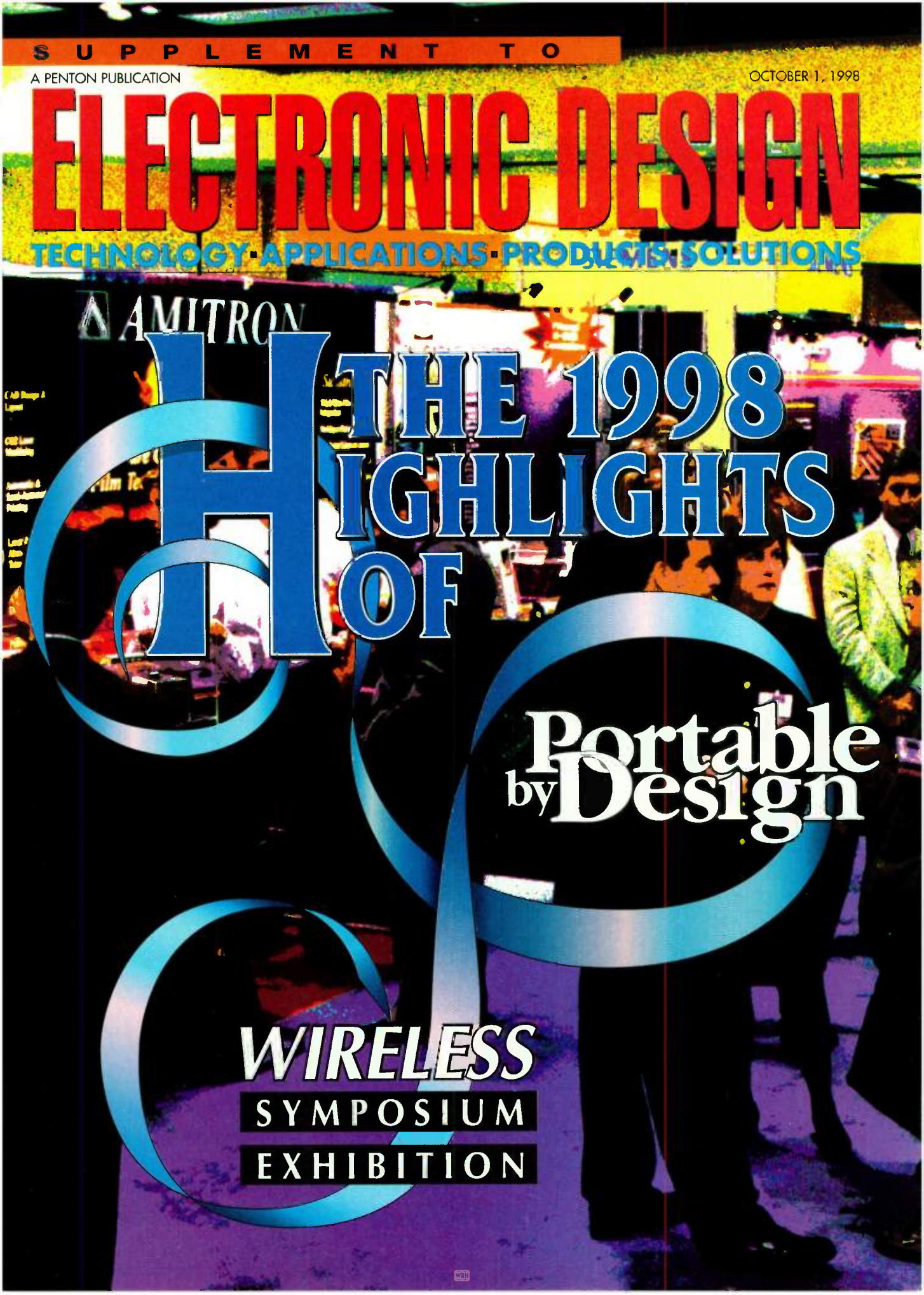
Today, the standard download approach is to attach a simple cable. However, there is no physical reason why the connection couldn't be an infrared or RF link, a modem, a cellular telephone, or even a laser. The only problems will be in how the bitstream is passed, and whether it requires a restrictive protocol. Third-party suppliers of downloading software and diagnostic tools are also on the rise, so an abundance of technology to improve the solution is also expanding. As the demand for ISP increases, the dimensions of field upgrades will change as well.

JESSE H. JENKINS is product planning and applications manager with the CPLD Business Unit at Xilinx Inc. He has BSEE, MSEE, and PhD degrees in electrical engineering and computer science from the University of California at Santa Barbara, and holds three patents. He has also authored a textbook "Designing with FPGAs and CPLDs," and dozens of technical papers. Jenkins can be reached at Xilinx Inc. 2100 Logic Dr., San Jose, CA 95124; (408) 559-7778.

SUPPLEMENT TO
A PENTON PUBLICATION
OCTOBER 1, 1998

ELECTRONIC DESIGN

TECHNOLOGY • APPLICATIONS • PRODUCTS • SOLUTIONS



THE 1998 HIGHLIGHTS OF

Portable by Design

WIRELESS SYMPOSIUM EXHIBITION

One-Stop Shop!

Call, write, fax or visit us on the Internet for your FREE CATALOG today!

Digi-Key®

Digi-Key Corporation
701 Brooks Ave. South
Thief River Falls, MN 56701
Toll-Free: 1-800-344-4539 • Fax: 218-681-3380
Order Online www.digikey.com

SAME-DAY SHIPMENT

On orders entered by 5:00p.m. central time

Your Ultimate Source For Quality Electronic Components!

#1 for Availability of Product
#1 for On-Time Delivery
#1 for Overall Performance

For volume pricing on passive, interconnect and electromechanical product, call and ask for:

DIGI-KEY® Volume Business Division

READER SERVICE 154

BENCHMARQ

Introducing the NEW *Power Minder*™ series from Benchmarq...

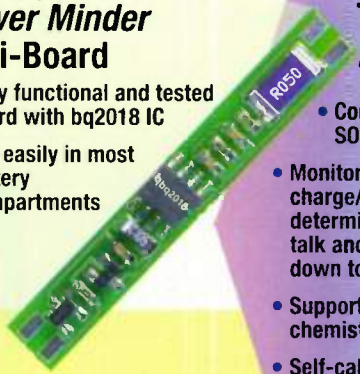
Which battery display would your customers want?

Actual Talk Time or Guessing Bars

Benchmarq's bq2018 *Power Minder* series offers price/performance and gives customers precision battery status.

The bq2118 *Power Minder* Mini-Board

- Fully functional and tested board with bq2018 IC
- Fits easily in most battery compartments



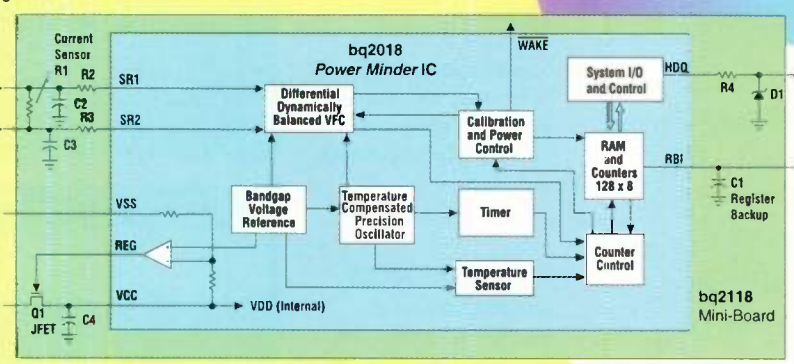
The bq2018 *Power Minder* IC

- Compact 8-pin SOIC package
- Monitors battery charge/discharge to determine remaining talk and standby time down to the minute
- Supports any battery chemistry
- Self-calibrating feature assures accuracy
- Low power drain: <80 µA operating, <10 µA in sleep mode or <100 nA in data-retention mode
- Single-wire control/ data serial interface
- 115 bytes user-programmable NVRAM store battery data, charge information, & ID codes

How It Works

The bq2018 *Power Minder* IC is a multifunction charge/discharge counter that works with an intelligent host controller to provide state-of-charge information for rechargeable batteries. The functional block diagram shows the bq2018 and bq2118 mini-board.

Charge/discharge is monitored via the low-value sense resistor, R1. A differential dynamically balanced VFC integrates the charge and discharge levels sensed by R1.



By using the accumulated counts in the charge, discharge, and self-discharge registers, an intelligent-host controller can accurately determine battery state-of-charge for any type of battery. Self-discharge is estimated using the internal temperature sensor and timer.

Host controller interface is via the HDQ serial line, allowing access to battery status registers, including read/write access to 115 bytes of the NVRAM (128 bytes total).

Backup current for the NVRAM is less than 100 nA, which means data can be held for very long periods with just a capacitor or single-cell battery source.

MARQY'S Message:
Contact Benchmarq or see http://www.benchmarq.com

BENCHMARQ®

BENCHMARQ Microelectronics, Inc.
17919 Waterview Parkway
Dallas, Texas 75252 U.S.A.
800-966-0011 or 972-437-9195
E-mail: benchmarq@benchmarq.com
WWW: http://www.benchmarq.com

BENCHMARQ...THE BRAINS BEHIND THE BATTERY™

READER SERVICE 152

INTRODUCING

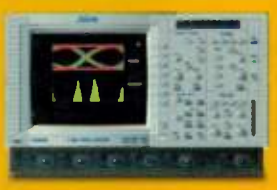
JitterTrack™

It's about Time!

The New Jitter and Timing Analysis Software Package. Easier and More Precise with Breakthrough Tools.

IF JITTER AND TIMING MEASUREMENTS ARE IMPORTANT TO YOUR WORK, THE NEW JTA PACKAGE FROM LECROY IS FOR YOU. CAPTURE SIGNALS USING THE ULTRA-STABLE TIMEBASE OF A LECROY DIGITAL SCOPE AND VIEW THE ORIGINAL SIGNAL PLUS JITTERTRACK-ANALYSIS OF PERIOD, CYCLE-TO-CYCLE, TIME INTERVAL ERROR AND OTHER TIMING PARAMETERS. SPOT PROBLEMS IN THE TIMING ANALYSIS AND VIEW THE PORTION OF THE SIGNAL THAT CAUSED THE PROBLEM! YOU CAN MAKE VERY PRECISE JITTER MEASUREMENTS WITH A REPEATABILITY OF 400 FEMTOSECONDS.

IF TIMING IS EVERYTHING, THEN THE JTA SOFTWARE PACKAGE IS EVERYTHING TO TIMING!



To learn more about JTA or our special offer, call

1 800 4LeCROY

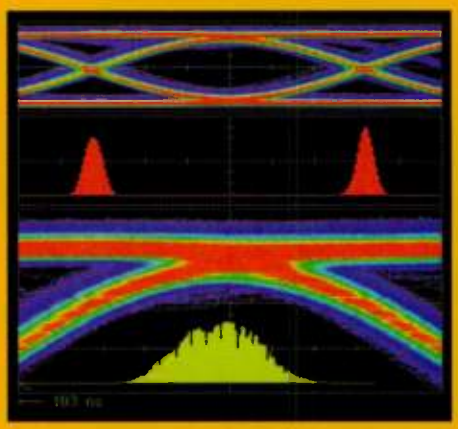
LeCroy

700 Chestnut Ridge Road
Chestnut Ridge, NY 10977-6499
www.lecroy.com

TIMING FUNCTIONS

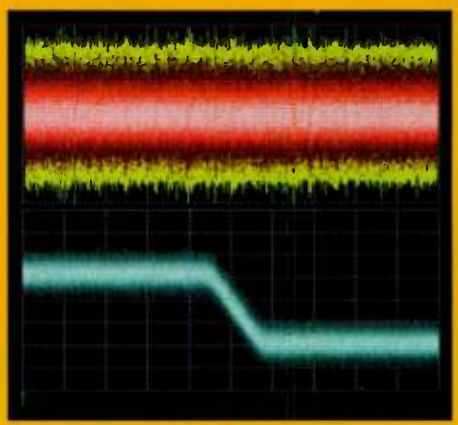
Persistence Histogram on an eye diagram. The crossover asymmetry shown is an important criterion for characterizing SONET/SDH signals.

The vertical cut shown below reveals a bimodal behavior which could adversely affect the signal's SNR (Signal-to-Noise Ratio).



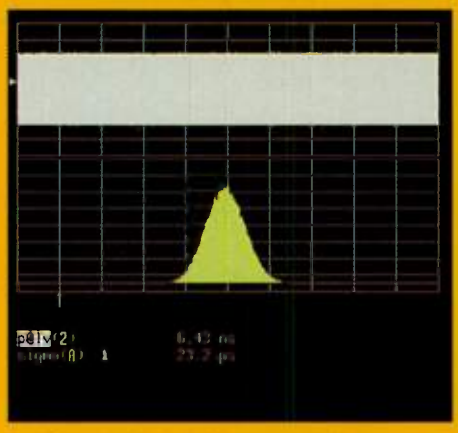
JITTERTRACK VIEW

The latest feature from LeCroy – JitterTrack – is so innovative, we've got a patent pending! Two JitterTrack functions characterize a PLL (Phase Locked Loop). The period JitterTrack (below) shows a progressive frequency transition. To keep the PLL on track, cycle-to-cycle period transition (above) should not be too abrupt and remain within the 5 sigma range signified by the yellow envelope.



STATISTICAL TOOLS

JTA timing parameters feature an unlimited number of cycle calculations on single-shot acquisitions of up to several million points. The period-at-level parameter has been calculated on over 300,000 cycles and analyzed with the histogram function, one of JTA's statistical tools.



READER SERVICE 155

INTRODUCTION

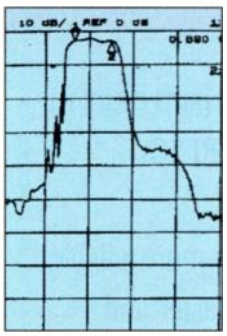
Welcome to the latest Highlights of the Portable By Design Conference and the Wireless Symposium. This supplement to *Electronic Design* is based on the proceedings of the fifth and sixth editions, respectively, of the two conferences and trade shows. The events, which ran concurrently February 9-13 at the Santa Clara Convention Center, Santa Clara, Calif., were sponsored by *Electronic Design* and its sibling publications, *Microwaves & RF* and *Wireless Systems Design.*

The two proceedings combined contain nearly 130 papers in more than 950 pages. Obviously, this supplement, with several brief summaries of selected papers, can only hope to give readers a glimpse at what the conferences were about, and what some of the concerns are in the fields of endeavor covered by the two technical programs. Besides their interest to the readers, the papers were chosen based on the ability to summarize them briefly while maintaining technical integrity. Of course, this means that many excellent papers could not be presented here. For those papers, as well as the complete versions of the papers summarized in this supplement, we refer you to the individual proceedings.

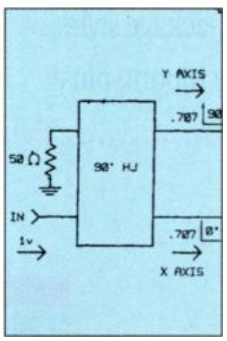
The supplement also includes reprints of articles written as previews of the Portable By Design Conference and Wireless Symposium and published just prior to the events. The articles offer a good overview of the conferences and the topics covered, as well as some insight into the products introduced at the exhibitions.

The next Portable By Design Conference and Wireless Symposium will be held February 22-26, 1999 at the San Jose Convention Center, San Jose, Calif. For more information, check out *www.Wireless-Portable.com* or contact Wireless & Portable Shows, Penton Institute, 1100 Superior Ave., Cleveland, OH 44114; (888) 947-3734; fax (201) 393-6297; instant fax-back (800) 561-SHOW.

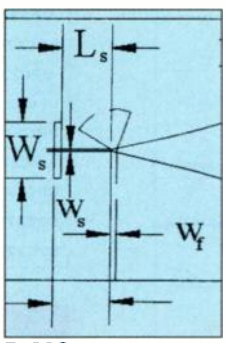
JOHN NOVELLINO
Managing Editor,
Special Projects



P. 96J



P. 96L



P. 96Q

Penton

BPA

NEC Silicon RF IC Solutions... from 25¢

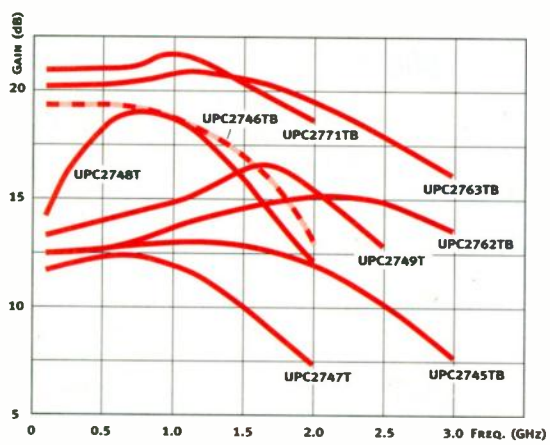
Want to make life simpler? Reduce the parts count in your design with low cost NEC Silicon RF ICs.

But be aware of the side effects!

Fewer parts can make your design more reliable. Your QC easier. And your assembly faster and more efficient.

NEC RF ICs come in a variety of package styles, including low cost plastic and surface mount, plus they're available on tape and reel. Best of all, their quality and reliability are proven. With a production rate exceeding 20 million RF ICs a month, no one knows this technology like NEC.

Our *Silicon RF IC Selection Guide* lists specifications for these and dozens of other devices. For a copy, call CEL or one of our distributors. Or call our Fax Hotline and request *Document #502*.



GAIN VS. FREQUENCY

NEC

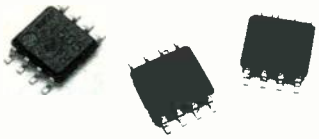
5V WIDEBAND RF IC AMPS—FROM 25¢

PART	FREQ. RANGE	GAIN (dB)	NF (dB)	P_{1dB} (dBm)	I_{CC} (mA)	f_{TEST}
UPC1678GV	50MHz–2.0GHz	23	6	+15.9	49	500MHz
UPC2708T	50MHz–2.9GHz	15	6.5	+9.2	26	1.0GHz
UPC2709TB	50MHz–2.3GHz	23	5	+8.7	25	1.0GHz
UPC2710T	50MHz–1.0GHz	33	3.5	+10.8	22	500MHz
UPC2711TB	50MHz–2.9GHz	13	5	-2.6	12	1.0GHz
UPC2712TB	50MHz–2.6GHz	20	4.5	-0.4	12	1.0GHz
UPC2713T	50MHz–1.2GHz	29	3.2	+0.3	12	500MHz
UPC2776TB	50MHz–2.7GHz	23	6.0	+6	25	1.0GHz
UPC2791TB	50MHz–1.9GHz	12	5.5	+1	17	500MHz
UPC2792TB	50MHz–1.2GHz	20	3.5	0	19	500MHz

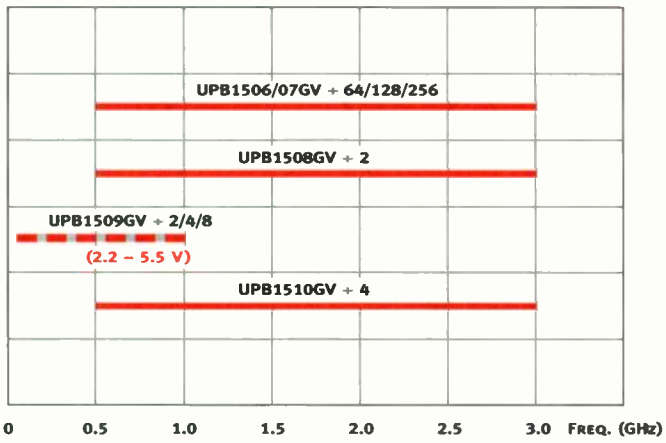
3V WIDEBAND RF IC AMPS—FROM 35¢

PART	FREQ. RANGE	GAIN (dB)	NF (dB)	P_{1dB} (dBm)	I_{CC} (mA)	f_{TEST}
UPC2745TB	50MHz–2.7GHz	12	6	-3.0	7.5	500MHz
UPC2746TB	50MHz–1.5GHz	19	4	-3.7	7.5	500MHz
UPC2747T	100MHz–1.8GHz	12	3.3	-11	5	900MHz
UPC2748T	200MHz–1.5GHz	19	2.8	-8.5	6	900MHz
UPC2749T	100MHz–2.9GHz	16	4	-12.5	6	1.9GHz
UPC2762TB	100MHz–2.9GHz	14.5	7	7	27	1.9GHz
UPC2763TB	100MHz–2.4GHz	20	5.5	6.5	27	1.9GHz
UPC2771TB	100MHz–2.1GHz	21	6	11.5	36	900MHz

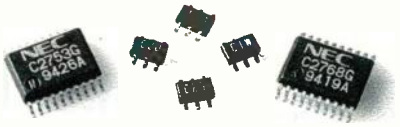
Prices at 100K quantity



5V Prescalers—from 70¢



Frequency Range



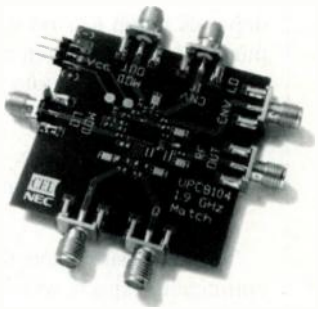
3V Frequency Converters—from 60¢

PART	RF Frequency (MHz)	I_{CC} (mA)	Conversion Gain (dB)	Output IP_3 (dBm)
UPC2756T[1]	100 - 2000	5.9	14	0
UPC2757T[1]	100 - 2000	5.6	13	0
UPC2758T[1]	100 - 2000	11	17	+6
UPC2768GR[1]	10 - 450	7	80	-17
UPC8106T[2]	100 - 2000	9	9	+1
UPC8112T[1]	800 - 2000	8.5	13	-10
UPC8116T[3]	100 - 500	4.1	6.5	—

1. Downconverter 2. Upconverter 3. AM/ASK Receiver IC

UPC8104GR
IQ Modulator

Evaluation boards for most NEC MMICs are available free from CEL



PLUS DISCRETES...!

These NEC biploars are ideal for amplifier and oscillator applications in your portable wireless designs. Priced from 20¢.

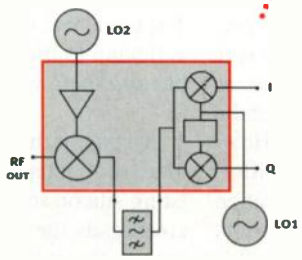
NE686 Bipolar Transistors
- High f_T (15 GHz)
- Low Noise
- Excellent Insertion Power Gain

NE687 Bipolar Transistors
- Low Noise (1.3 dB @ 2 GHz)
- High Gain Bandwidth
- Noise match close to 50 ohms

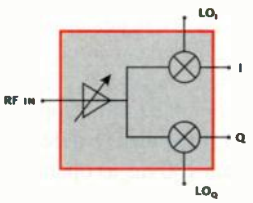
NE688 Bipolar Transistors
- Low Phase Noise Distortion
- Low Noise, High f_T
- Large Absolute Max Collector Current

All are available in eight different low cost surface mount packages.

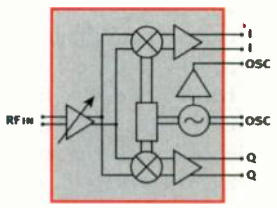
Mods & Demods—from $1.60



UPC8104GR
IQ Modulator w/Upconverter
- 3 – 5 Volt operation
- Ports for IF filter
- 10 MHz I/Q BW
- 400 MHz IF Bandwidth
- 1.9 GHz RF Output



UPC2766GR
IQ Demodulator
- RF BW – DC to 1 GHz
- IF BW – DC to 100 MHz
- 35 dB typ AGC dynamic range
- 30 dBc typ distortion



UPC2781GR
IQ Demodulator
- RF BW – 440 to 520 MHz
- IF BW – 0.3 to 20 MHz
- On Chip 90° Phase Shifter
- 35 dBc typ distortion

Need Product Information Fast? Use CEL's Automated Fax System!

CEL FAX
800-390-3232
(U.S. and Canada Only)

CEL California Eastern Laboratories

4590 Patrick Henry Drive ▪ Santa Clara, CA 95054 ▪ 408 988-3500 ▪ http://www.cel.com

DISTRIBUTORS: Reptron Electronics (888) REPTRON Bell Industries (800) 525-6666

Mouser Electronics (800) 346-6873 Electro Sonic (800) 567-6642 (Canada)

READER SERVICE 97

Designing Low-Power/High-Performance Handheld Systems

Selecting a microprocessor for PDAs, PICs, and HPCs involves careful evaluation in a three-dimensional space. HPCs greatly resemble laptops, so they need to be expandable, have a broad base of ISVs targeting their customers, and have a standard operating system and GUI. Additionally, product differentiation depends on CPU speed, "user-perceived" performance, amount of memory, and cost. Finally, increasing density levels achieved by current CMOS processes allow the implementation of systems-on-silicon geared to optimizing performance, with minimum cost and power consumption.

Laptops traditionally run the Microsoft Windows 95 operating system. Therefore the choice of architectures for those devices is limited to members of the x86 family of devices. HPCs, on the other hand, have Microsoft Windows CE as a de facto standard. Windows CE, contrary to Windows 95, is not limited to the x86 architecture, and is available to a number of microprocessor families, including MIPS and SH derivatives. As a consequence, the selection of an architecture for an HPC depends much less on the software compatibility issue and much more on other relevant parameters.

Relevant parameters when selecting an architecture for HPCs are:

- system performance,
- system power consumption, and
- system cost.

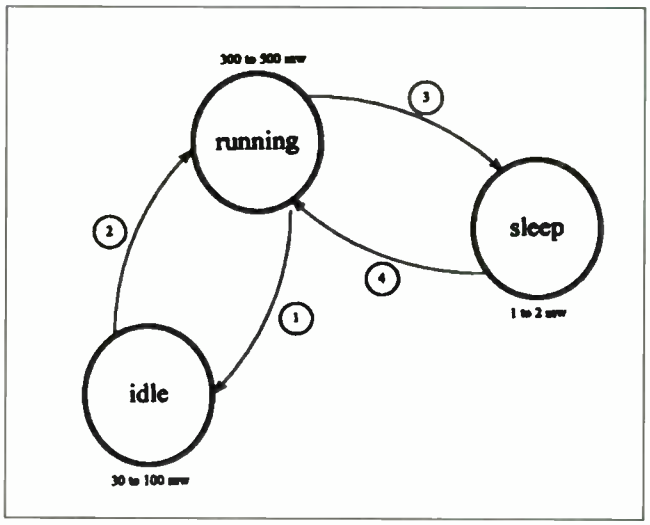
The three parameters listed above form a three-dimensional optimization space, which requires careful analysis.

It is very important to realize that system performance in HPCs is only relevant for two distinct ends. The first, "user-perceived" performance, is the difference in performance that a user actually can see. For example, a user can perceive the difference between a device that takes 2 sec. to open an application and a device that takes only 1 sec. to open the same application. However, it would be much harder for the user to perceive the difference between a device that takes 200 ms to open an application and another that takes only 100 ms to open the same application.

The second is performance as a technology enhancer. In this case, ever increasing performance levels enable applications previously deemed impossible or the migration of functionality previously implemented in hardware onto software running on the CPU. System performance. contrary to widely held beliefs in the PC desktop world, is not only a consequence of CPU speeds, but is also very much dependent on the CPU architecture, cache sizes, memory speeds, bus latencies, etc.

A typical HPC will contain two types of batteries in its power subsystem: a rechargeable main battery set and a backup battery. Typically, the main battery will be NiCd or NiMeH batteries in a AA form factor, while the backup battery will usually be a 3-V coin cell. The main battery is meant to provide power to the device while "on the road," while the backup battery will maintain the "illusion" of a persistent memory, even when the main battery fails.

A Windows CE-based device will present three operating modes related to power consumption *(see the figure)*.



•*Running mode:* In this mode, the CPU is executing code, scheduled tasks are being executed, and the LCD panel is being refreshed. In summary, the system is receiving and processing input. As soon as there are no tasks to be executed, the system changes into idle mode. If the system does not have any tasks scheduled in a "long time," it will change into sleep mode.

•*Idle mode:* In this mode there are no tasks scheduled to be executed. Therefore, the clocks to the CPU and all non-essential parts of the system are disabled. The LCD panel is being refreshed and the system is typically waiting for user input.

•*Sleep mode:* In this mode, the device is on power-off state. The contents of memory are preserved, and the real-time clock is ticking to preserve time and date. The system is waiting for the user to power it up or for an alarm to wake it up.

Reducing the cost of handheld computer devices involves increasing integration of system components. Most of the existing silicon solutions for HPCs today available in the market are already the result of some integration effort. Most of them present themselves as two-, three-, or four-chip solutions. Further integration is likely. A lot can be done to reduce the cost of the power supply circuitry through integration. Future HPCs will likely provide built-in wireless capabilities, and that will present further opportunities for integration.

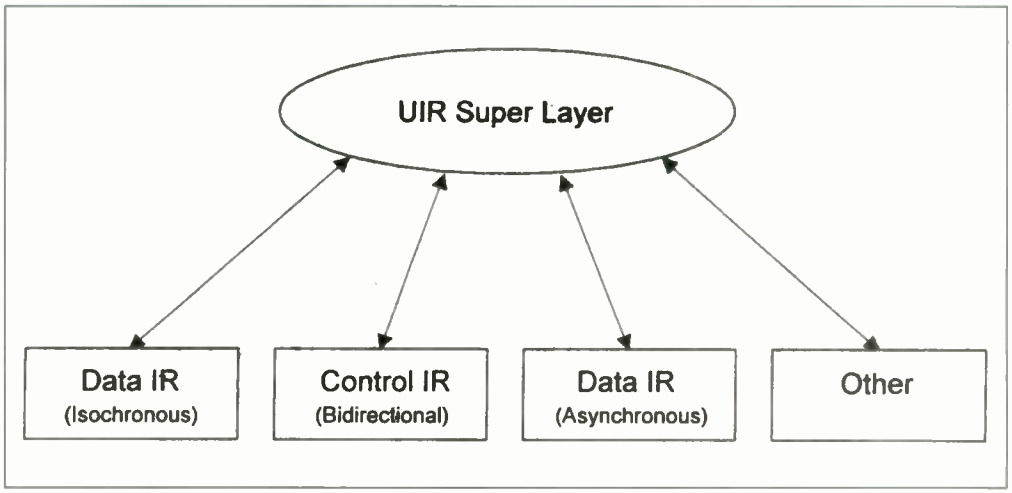
For the time being, integration will probably still be limited to a two-chip solution. Fully digital designs can migrate to smaller feature-size processes and to lower voltages much faster than analog or mixed-signal designs can. That makes it very likely that IC manufacturers will continue to try to optimize these two systems components separately, as Philips Semiconductors has been doing.

Integration leads to increased performance through increased clock speeds and careful design of the bus architecture. It leads to reduced power consumption through careful design and the lowering of system voltages. It also leads to reduced system costs through the reduction of chip count and of the required PCB real estate.

Milton Ribeiro, Philips Semiconductors. From the 1998 Portable By Design Conference.

Current IrDA Solutions And Future Plans

There are three main classifications of IR protocols: 1. consumer electronic remote control; 2. proprietary data transfer; and 3. IrDA data transfer. As infrared use continues to increase, close attention to interference/coexistence will be necessary to ensure that all equipment will be able to operate as desired and the end-user experience will remain positive. This paper will focus on the IrDA standards and show what is being done to accomplish these goals.



IrDA solutions have been included in notebook and desktop computers for a number of years. Starting with IrDA 1.0, data rates up to 115 baud were achieved. With the addition of the IrDA's high-speed extensions, referred to as IrDA 1.1 or Fast IR (FIR), data rates up to 4.0 Mbps are now available.

Areas where ongoing infrared activity is occurring include power consumption, component size, cost, and infrared link robustness. To reduce power consumption and thus increase battery life, optical transceiver manufacturers are developing more efficient infrared LEDs. In addition, most optical transceivers have power down modes and some are available with programmable transmitter power levels.

Small size is also significant in portable equipment. In the electronic industry, many new portable devices are being developed which include an infrared port. To enable these very small portable devices, optical transceiver manufacturers have continued to reduce the size of their components. In addition, National Semiconductor has integrated the infrared controller IC into many of its SuperI/O devices and has released a stand-alone device (PC87109) specifically for the digital camera market.

System cost is always a factor in a manufacturer's desire to be successful in a market. To this end both optical transceiver vendors and infrared controller IC vendors are reducing component costs as the market matures and volumes increase. Not only component cost but system costs are being reduced as more functionality is being integrated into the components. In the area of system performance, significant efforts have been exerted to improve the noise immunity of the infrared receivers to reduce bit error rates and increase the reliability of the infrared link.

National Semiconductor and others have been working on improving system flexibility to facilitate future expansions of the IrDA specifications. National has been working closely with optical transceiver manufacturers in defining the control interface between the infrared controller IC and optical transceiver. This is important since it will allow for future upgrades in a graceful and low-risk fashion. To keep this interface low-cost and expandable, a serial signalling scheme has been proposed which will allow future enhancements while keeping the same pinout and PCB layout. This serial interface uses soft addressing which allows multiple optical transceivers to share the same wires. The interface defines a message-based protocol that determines how control, status, and data are transferred. In defining the protocol, allowances were made for future extensions.

Coexistence between IrDA and Consumer Remote Control protocols should rely on frequency separation. This solution is relatively simple and it should lead to low-cost implementations. It empoys a TDM bearer mechanism within the PHY layer.

The control of the infrared medium is centralized. Only one station, acting as the host, is responsible for it. This station may also contain the main controller for control-oriented protocols (e.g., IrBus). A UIR [National's Universal Infrared architecture] super layer within the host controls the infrared medium allocation via a simple token-passing mechanism *(see the figure)*.

Each protocol is allocated a time slot within a periodic TDM frame, and it is allowed to use the infrared medium only for the duration of the time slot. The durations of the individual time slots as well as the TDM frame should all be programmable to accomodate different system requirements. If only one protocol is being used, the TDM mechanism can be disabled and the protocol will have total ownership of the infrared mechanism.

The handling of the token is very simple for a control-oriented protocol since the protocol controller uses a polling scheme and it is always responsible for initiating a communications operation.

Among all the requirements mentioned above, perhaps the most critical is the one related to coexistence. This issue was not addressed properly by IrDA 1.0 and IrDA 1.1, and therefore these protocols do not coexist well with new protocols designed to support future applications. It is imperative that future IrDA developments give the coexistence issue top priority.

Other issues, like interoperability, expandability, cost, etc., should also be kept in mind. We believe that a general framework with a well-defined set of rules should be created in order to assist in the development of new protocols. New protocols developed under this framework would, at a minimum, be guaranteed to coexist harmoniously. Regarding the existing IrDA 1.0 and IrDA 1.1 protocols, some minor modifications at the software level would make them more "coexistence friendly."

Franco Iacobelli and Robert Speckman, *National Semiconductor. From the 1998 Portable By Design Conference.*

Balanced Device Evaluation For Mobile Phones Using Modal Decomposition Technique

The use of balanced components is becoming popular in hand-held phones. Example components are: surface acoustic wave (SAW) filters, amplifiers, and some of the I/O ports of large-scale integrated circuits. In some cases a component may have both balanced and unbalanced ports. In the past, balanced components were measured by using balanced-to-unbalanced transformers (baluns). This allows the use of a conventional unbalanced 50-ohm test system.

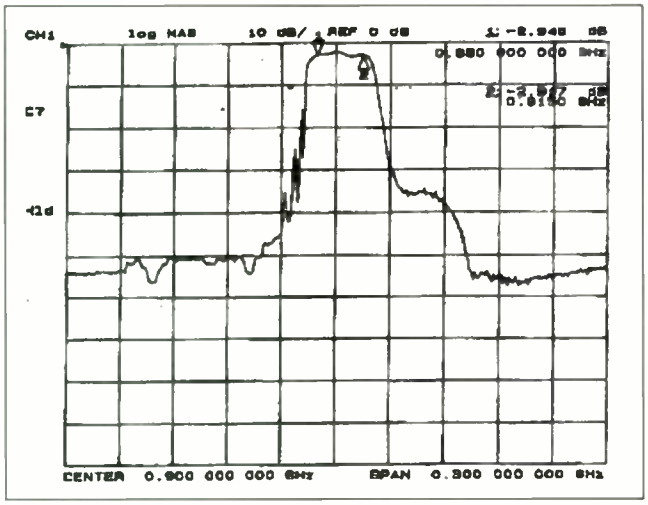
The problem with the balun approach is that as the frequency increases above about 100 MHz, the characteristics of the balun transformer are not well known and it is difficult to calibrate the test system because of the lack of balanced standards. Since the balanced impedance (Z_O) of a balun is part of its physical construction, a different balun is required for each different port impedance. If an impedance-matching network is used between a balanced component and a balun, and is adjusted for minimum insertion loss, the network may not be correct for use with other balanced components because it is matching the balun to the component, not matching the the component to a given Z_O.

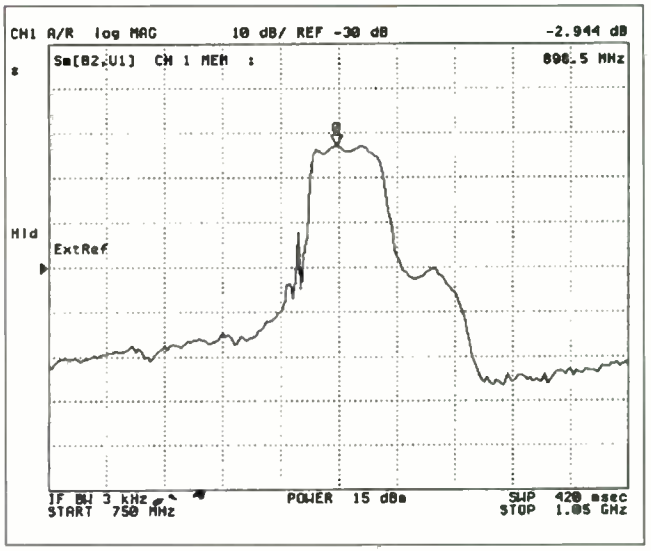
In early 1900, the technique of "modal decomposition" was known in relation to the testing of twisted-pair cables. With the advent of modern computers that can handle large matrices of complex numbers, the use of this technique has become practical. It is based on the idea of measuring unbalanced parameters and then converting them into balanced parameters.

The modal decomposition technique is not limited to twist-pair cables but can be used for any component that is linear with power level and time. It also has the capability to measure unbalanced parameters along with the balanced parameters. This allows components that have both balanced and unbalanced ports to be tested. The S-parameter test set used for this technique requires two physical ports for each "modal" port.

The steps in making the modal decomposition measurement are:

• Perform a classical vector network analyzer calibration on all physical test ports using conventional unbalanced 50-ohm calibration standards.





• Connect a device under test and measure the S parameters.

• Convert the S parameters into Z parameters.

• Transform the Z parameters into modal Z parameters (Z_m).

• Convert the Z_m parameters into modal S parameters (S_m).

• Select the parameter to display and download that 2-port parameter set as a complex matrix into the network analyzer for display.

The only part of the above procedure that is new is the transformation of the classical Z-parameter matrix into the Z_m matrix. The basis of this transformation is the use of "mathematical baluns."

Unlike the h-parameter method (Reference [3]), the modal decomposition technique allows the unbalanced (Z_{ou}) and balanced (Z_{ob}) termination impedance to be set in software. This is very important when making measurements of mode-conversion devices such as a balun transformer.

We measured a 900-MHz balanced-unbalanced SAW filter by using the conventional measurement technique *(above)* and the modal decomposition technique *(left)*. The measured insertion loss within the passband is well matched at less than 0.5-dB data difference. There are 5- to 10-dB data differences in the rejection band.

This worked because the balun had near theoretical performance. In other cases the results may not agree if the SAW filter is being tuned to compensate for the parasitics of the balun. This technique can be used to make balanced device evaluation much easier, simpler, and more accurate.

[3] Peeters, Steyaert, Sansen, "High-frequency measurement procedure for fully differential building blocks," *IEEE Transactions on Instrumentation and Measurement*, Aug. 1977, Vol. 46, Num. 4, pp. 1039-1043.

Shigeki Tanaka and Brooke Clark, *Hewlett-Packard Co.*
From the 1998 Wireless Symposium.

Comparing PCMCIA, Cardbus, And Small PCI

PCMCIA is the Personal Computer Memory Card International Association. The first and second release of the card spec still referred to the cards as PCMCIA cards. However, with the addition of Cardbus capability, the PCMCIA organization has changed the terminology by which they refer to the different generations of cards. PCMCIA still refers to the organization while "PC Card" or R2 Cards" (represents Release 2 of the standard) still refers to the 16-bit cards. Cardbus refers to the 32-bit interface, which is closely related to the PCI bus.

PC Cards come in three physical sizes: Type I, Type II, and Type III. They are all 85.6-mm long, 54.0-mm wide, and 3.3-mm thick. Type II has a thickness of 5 mm in the substrate area, and Type III has a thickness of 10.5 mm in the substrate area. The guide rails for the host socket can accept all three types of cards as long as the opening is large enough for the Type III.

The memory interface for the PCMCIA cards has 64 Mbytes of direct addressability (or unlimited if addressed in an indexed fashion). That data can be accessed in single bytes or double bytes. Virtually any type of silicon storage can be used on cards; however, the primary use of memory is for non-volatile storage. There is a register memory or attribute memory space provided to store the card's configuration. And, of course, it contains the standard control functions such as read/write, card enable, etc.

The I/O capabilities follow pretty much the same addressability and data width as the memory cards. However, there are many more signals needed to configure and control I/O functions. The most important is the interrupt line. Any event that happens outside of the computer's direct control needs to be signaled back to the system via the interrupt line.

Cardbus is a 32-bit multiplexed address/data interface that runs at PCI speeds of 33 MHz. It uses the same 68-pin interface as the R2 Cards or the 16-bit cards. The host can distinguish between 16-bit cards and Cardbus cards even before power is turned on to the socket. It is a requirement that Cardbus host controllers also support the older 16-bit cards in the same socket. This feature prevents obsolescence of the 16-bit cards.

Once a Cardbus card is configured, it effectively becomes a PCI application with PCI performance.

A typical two-slot host controller like the TI PCI1220 can support up to two 68-pin Cardbus slots and can be combined in a system to give any multiple number of slots *(see the figure)*. There is an RAS application today that uses 16 Cardbus controllers in one box for a total of 32 Cardbus cards.

There are only a few Cardbus cards available today. These are applications that need the 132-MB/s performance of Cardbus. Some functions that can benefit from Cardbus are 100-Mbit LANs cards. 100-Mbit LAN applications can be run using 16-bit cards, but do not achieve 100-Mbits/s, while the Cardbus LAN cards can easily achieve full performance.

Small PCI (SPCI) cards are functionally the same a PCI cards, but use a form factor equivalent to PC Cards in width, length, and thickness. However, they use a 108-pin connector and are keyed to prevent accidental insertion of PC cards into an SPCI socket and vice versa. It is possible to have an adapter card that electrically connects an SPCI socket to a PCI socket.

Some features and design points for SPCI cards are:

•Full performance and electrical characteristics of standard PCI.

•Small form factor (same as PC Cards but with a 108-pin connector.

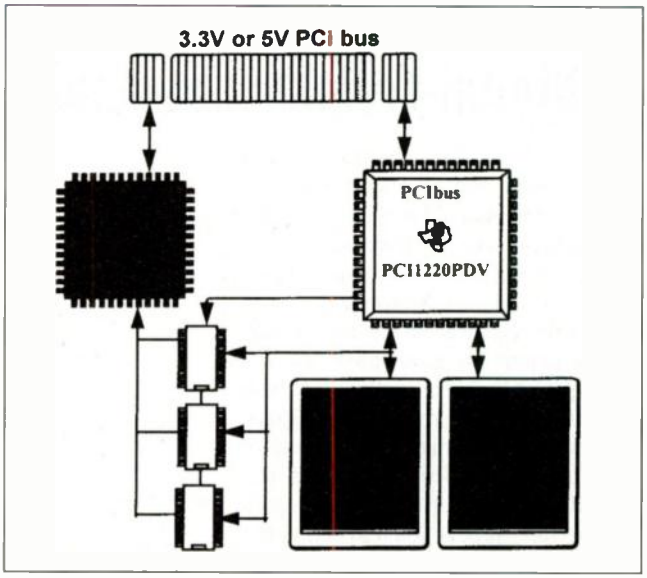
•Requires no socket-controller silicon or software.

•Incorporates CLKRUN signal for energy conservation.

•Incorporates PRSNT[1:2}# signals for optimizing power supplies.

•I/O is cabled to bulkhead for design flexibility.

•Enables 3.3-V and 5-V operation, with universal option for smooth migration.



Reduced power requirements enable the use of smaller power supplies and result in cooler system operation.

Some benefits to OEMs and card manufacturers are:

•Provides the ability to incorporate PCI into smaller mechanical packages.

•Frees up standard PCI slots for additional adapters.

•Reduces the need to integrate continually changing subsystems onto the system board.

•Results in lower system-board costs due to manufacturing economies of scale. The system board can offload many of the unique applications to these SPCI cards and one planar board design can fill multiple system design points.

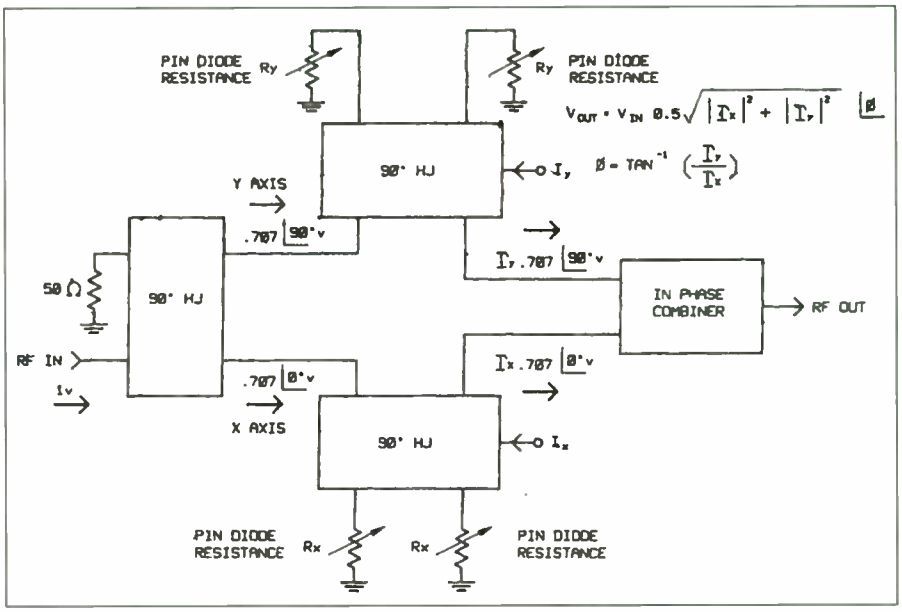
SPCI cards perform at PCI speeds by definition, but they do have some drawbacks. SPCI cards are plug-n-play but not hot pluggable. To make SPCI cards hot pluggable, the host needs to isolate the SPCI socket for insertion and removal of SPCI cards. The OS and third-party software needed to handle system resources that come and go are not as developed for SPCI cards as it is for PC Cards and Cardbus cards.

SPCI and Cardbus cards can handle all of the application capability of PCI functions, while the 16-bit PC Cards are primarily used for functions requiring less than 5 MB/s performance.

Anthony Wutka, Texas Instruments. From the 1998 Portable By Design Conference.

Vector Modulator Realized On A Single Subtrate For Feedforward Response Cancellation In Digital Cellular Communications Systems

The demanding signal purity requirements and digital modulation schemes encountered in wirelesss communications services have accelerated the development of feedforward amplification techniques. Adjustment of both amplitude and phase in the cancellation loop is required to accomplish this, and it has generally been implemented with variable attenuators and phase shifters. However, these components do notprovide the most effective solution and have drawbacks that make them a poor choice for production environments. The vector modulator (or vector attenuator) provides the desired control of gain and phase without the "side effects" encountered with more conventional techniques.



The vector modulator, as a variable resistive device, solves the most limiting problems of the conventional approach without creating additional constraints in the process.

A digitally controlled vector modulator such as the one described in this paper resonds to a direct command from a control source to produce specific phase and amplitude values without intermediate steps.

As a result, the time required to adjust a typical feedforward amplifier is reduced by 25% or more. In addition, this vector modulator handles an input power of more than 500 mW, which makes it suitable for use in adjusting feedforward power amplifiers.

The vector modulator consists of an input 90° hybrid that feeds two additional 90° hybrids that have PIN diodes connected to form a reflective phase shifter/attenuator. Both signals are summed in an in-phase power combiner *(see the figure)*.

By phase-combining the attenuator outputs, and by controlling their values with a digital word, any combination of amplitude and phase can be rapidly obtained. Both of the vector modulator's I and Q attenuator inputs are controlled, in contrast to the phase and attenuation of a phase shifter and an attenuator. In addition to replacing the sequential determination of phase angle, the vector modulator has very little group delay distortion and is extremely stable in its delay in the presence of changes in control inputs. As a result, the depth of the feedback loop can be maintained at an optimum level.

The reflective phase shifter/attenuator control current inputs are referred to as I_y and I_x. These inputs apply bias to four PIN diodes designated as equivalent resistance R_x and R_y. The x-side at 0° and y-side at 90° can be considerd the x and y axes to form the output voltage.

The bias is applied through the hybrid to the two pairs of diodes. The I_x current is isolated from the I_y current, providing independent variation in an amount necessary to provide a desired combination of attenuation and phase at the output.

The vector modulator was fabricated by a process that utilizes a single piece of low-cost alumina for both the circuit and hybrid header package. It was developed by KDI/triangle using the Surfpac process. Gold plating, glass firing, and Kovar typical of conventional hybrid packages are eliminated. This often produces as much as a 2:1 reduction in size and volume over conventional thick-film architectures. Multiple circuits are manufactured and tested on a single substrate so that unit-to-unit consistency is greatly improved.

The performance gains provided by Surfpac are substantial. For example, a traditional 120° phase shifter hybrid for operation at PCS frequencies from 1.9 to 2.1 GHz costs about $500. A comparable Surfpac phase shifter costs about $50, and delivers the same or better performance. The device measures 1.5 by 1.0 by 0.375 in. versus 3 by 2 by 1.5 in. for its hybrid counterpart. Weight is also reduced, from 11 oz. to less than 2 oz.

The advantages of the vector modulator in the final tuning of feedforward amplifiers are derived from its ability to produce a change in values within 0.5 dB with 2.5° steps for 9 dB of attenuation. The vector modulator described in this paper provides the additional benefits of relatively high power-handling capability, high repeatability, small size, and low cost, which are derived from realization in the Surfpac process.

The result is a vector modulator with a range of attenuation from 0 to 18 dB and digital phase shift from 0 to 360°. The use of this vector modulator design in production amplifiers can potentially reduce final tuning time by at least 25%, depending on the design of the host test system.

Larry Silverman, KDI/triangle Corp. From the 1998 Wireless Symposium.

Methods To Qualify ACPI Smart-Battery Implementations

The Advanced Configuration Power Interface (ACPI) defines the software and hardware interface between the operating system (OS) and the SMBus system. The interface goes through an embedded controller. This definition allows the OS to directly communicate with the Smart Battery system, which provides the OS with consistent and accurate battery data while optimizing battery system performance. Maximum run time requires the OS to get accurate battery data and for the battery system to deliver optimal charging and discharging performance. This is accomplished by allowing the battery to determine its own charging algorithm. Thus an ACPI-compliant Smart Battery system is both accurate and chemistry independent.

In order to test Smart Battery data, we are proposing a software controllable tool, the Battery Test Workbench (BTW). This tool must have many test and measurement capabilities:

- ability to measure voltage and current at the battery terminals,
- a programmatically controllable load,
- a programmatically controllable charger,
- an ohmmeter to measure thermistor pin values, and
- an SMBus activity monitor.

The BTW consists of the battery to be tested, the test fixture, and a computer to control the test fixture. Its use will be described at a general level with its possible uses to test Smart Batteries and other Smart Battery system components. While the particular hardware and automated control is only a proposal, the tests and test methodologies can be done with off-the-shelf test equipment.

The capability to perform automated battery tests, although time consuming, is highly desirable. Smart Batteries are electro-chemical systems coupled with electronics. These electrochemical systems change with use, and the electronics try to compensate for these changes. With age, battery errors can grow, so it is important to cycle the battery a number of times to accurately gauge the capacity and reported run times. Measuring battery data accuracy is the key goal of the BTW. Smart Batteries, unlike other batteries, must report data within tolerances of 1%.

The type and characteristics of the load placed on the battery during testing are very important. Battery vendors normally use a constant-current load based on a 5-hr. rate to report capacity. However, a notebook computer presents an entirely different type of load, a rather dynamic constant-power load.

The most important characteristics that must be tested are the capacity, the alarms, and the remaining-time data. Additionally, there is other information that can and should be tested at the same time. For example, the reported error can be tested along with the amount of remaining energy actually left when the battery reports that it is fully discharged. There are certainly other data values that may be tested as well.

The test methodology is to use the charge voltage and current commands to set the output of the programmable power supply. The voltage and current reported by the battery should be compared to the values read by the data acquisition system. When the battery tries to end charging by sending a zero charging current or voltage, or a terminate charge alarm, the programmable power supply should be turned off. The battery at this time should be fully charged. Several battery data values should be read and recorded, including battery capacity, last full charge capacity, max error, and the status.

There are three types of discharge tests that need to be run. First is the C/5 test, where the battery's design capacity in milliamp-hours is divided by five and used as the load placed on the battery. The battery is discharged until it sends a terminate discharge alarm or a predetermined cutoff voltage level is reached. The measured capacity is then compared with the reported capacity. If the battery terminate-discharge alarm causes the discharge to end (normal case), the battery should then be discharged until the cutoff voltage is reached.The energy extracted from the battery at this step is useable energy that is unavailable to the user. The battery is recharged and the test repeated.

The second test is much like the first except the battery is placed in the power mode and a P/5 constant-power load is applied. This test is important to confirm that the battery reasonably reports its capacity in terms of energy.

The third test is more extensive, testing the battery capacity using the simulated notebook load. In this case the charge cycle remains the same, but the remaining time is tracked throughout the discharge cycle.

Unlike the previous tests, the use of a dynamically changing load means that the remaining time will not monotonically decrease and the remaining capacity will not track with the energy delivered. The most important information from the OS point of view is the alarm information. The user wants accurate remaining time and both want to extract all the available energy. In this case, the remaining time is recorded and plotted. At the end of each discharge run, the actual run time can be overlaid as a straight line on top of the remaining times returned by the battery. The net area between the two curves should approach zero.

Additional testing should be done to simulate a typical user's charge/discharge pattern. For this test, the battery should be fully discharged and then fully charged. This should allow the battery electronics to accurately determine the end points and establish a known capacity. The battery should accurately report capacity and remaining time, taking max error into account.

The SMBus Implementers Forum is responsible for publishing and maintaining the SMBus Specification as well as the Smart Battery Data Specification, the Smart Charger Specification, and the Smart Battery Selector specification. Join and participate in the SBS Implementers Forum to help maintain and improve these specifications. Build products that comply with the specifications and test them for compliance.

In particular, test the system ACPI compliance. Focus on the Smart Battery's data to ensure that it accurately reports information and is able to supply all its available energy. This ultimately will ensure consumer satisfaction and help the OS take full advantage of the battery.

Robert A. Dunstan and Phil Mummah, *Intel Corp., Mobile Handheld Products Group. From the 1998 Portable By Design Conference.*

Battery Options And System Design Considerations: A Comparison Of Primary And Secondary Battery Systems For Handheld PC Devices

Determining which type of battery is best for a given product depends on which performance parameters are the most important for the application. This paper helps identify the important performance characteristics of the main battery system in handheld PCs (HPCs). Characteristics discussed include system self-discharge, thermal capabilities, internal operating impedance over discharge, cycle life, and product safety. The discussion includes the advantages and disadvantages of primary (alkaline) and secondary (rechargeable alkaline, lithium-ion, and nickel-metal hydride) chemistries in HPCs. It also looks at contact theory and circuit design options that can increase reliability in any battery-powered product.

Also important are an understanding of thermal capabilities, effects of the operating environment, and battery-life requirements of the product. Thus designers must consider two interacting paths: the consumption of the active electrochemical components and the effects of thermal wear out. Self-discharge and thermal wear out must be treated as separate issues because designers can sometimes compensate for self-discharge by increasing battery capacity, but thermal wear out can be addressed only by selecting a more thermally capable battery.

Nickel-metal hydride cells, like their NiCd counterparts, are 1.2-V cells with a very similar internal impedance profile. They have a stable voltage profile, decent pulse-rate current drain capability, and quick recharge regimes (up to a 3C rate), but they do not suffer from memory-effect problems bought on by repetitive shallow discharge cycles. However, they have a high self-discharge rate, about 3% per day.

The lithium-ion battery is a relatively high-energy-density rechargeable system which allows designers to reduce the form factors of their products.

Unlike metallic lithium cells, lithium-ion batteries keep the lithium in an ionic state. Metallic lithium is very volatile and reactive, to the point of burning in the presence of water. Lithium ion cells retain the electrochemical properties of lithium, while eliminating the inherent safety issues of metallic lithium.

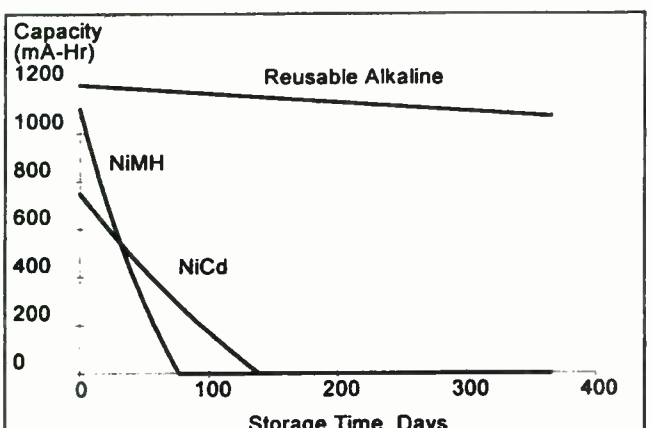


Figure 2. Estimated Charge Retention (20°C)

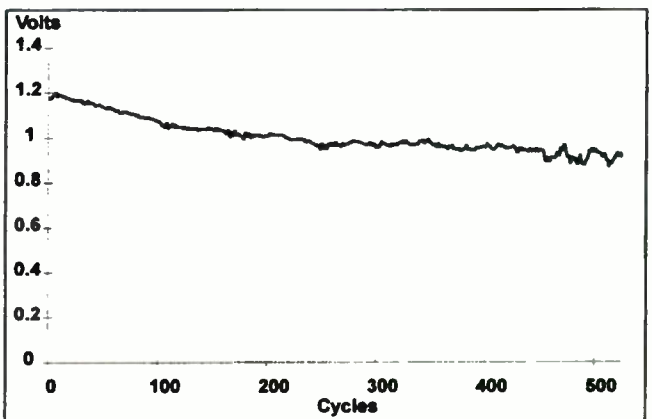


Figure 3. Partial Discharge Response (Voltage at the end of 200 mA / 90 min. discharge)

The clear advantage of using primary alkaline batteries is reliability; there are no concerns about shelf-life, no concerns about retail availability of replacement cells. The big drawback can be cost, especially in power-hungry devices.

The discharge capacity of rechargeable alkaline cells fades with each cycle, with the majority of the fade occurring in the early cycles. Two key benefits of rechargeable alkalines are low self-discharge *(Fig. 2)* and excellent shallow-discharge performance *(Fig. 3)*.

These characteristics make the rechargeable alkaline system ideal for intermittent use and/or frequent-recharge applications. Ideal applications for rechargeable alkalines include low- and moderate-power portable applications such as handheld PCs, cordless phones, CDMA phones, or portable terminals.

The design criteria for a device which uses discrete cells has additional contact reliability concerns not associated with a battery pack design. When designing a battery contact system for discrete cells, both the mechanical and electrical atributes of the contact design must be considered.

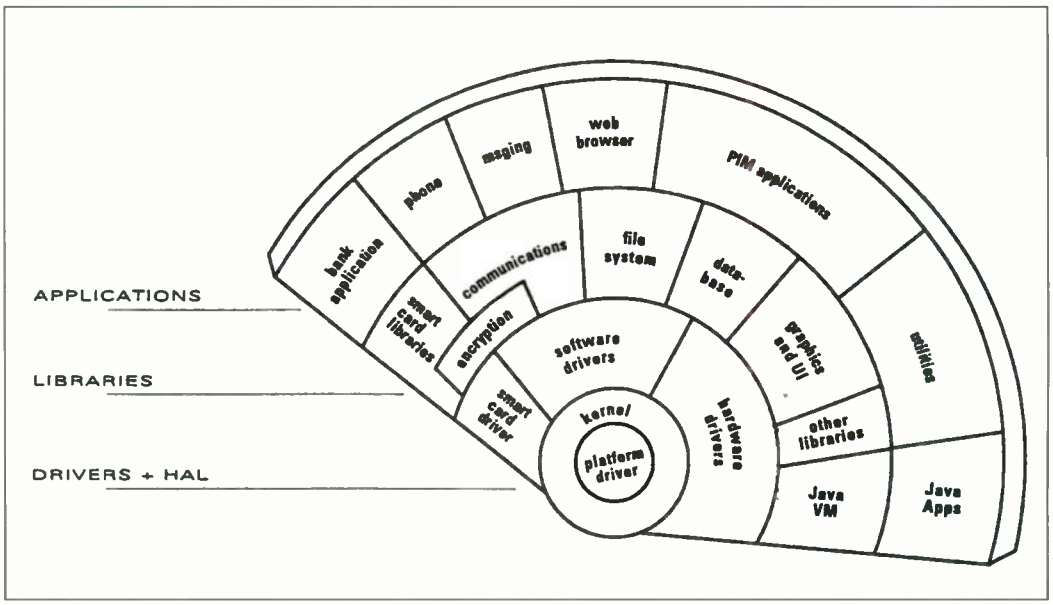
By designing a contact system that exploits the mechanical difference between Renewal cells and other chemistries of the same cell size, a contact scheme can be created which allows for the discharge of any voltage-compatible cell chemistry but discriminately charges only Renewal cells.

This duality offers the user the option of secondary battery cost savings without giving up the convenience typically associated with primary alkaline cells, should the need arise.

The life-cycle performance of rechargeable alkaline battery packs can be optimized by the use of appropriate battery management techniques.

***Jim Pilarzyk**, Rayovac Corp. From the 1998 Portable By Design Conference.*

Personal ATMs: Secure, Portable, Electronic Commerce With Smart Phones And Smart Cards



An estimated US$8 billion will be spent at electronic commerce (e-commerce) Web sites this year, and that amount is projected to grow to US$546 billion by the year 2000. The growth of e-commerce may help drive the adoption of electronic cash (e-cash) cards.

As e-cash becomes viable, people will use it to settle transactions, both at real-world retail outlets and at virtual-world Web-based e-commerce sites. E-cash card users will reload value onto their cards from the ATMs (automatic teller machines) from which they withdraw cash today. For added convenience, e-cash providers will also enable users to reload via their PCs, as well as from devices connected to their phone lines. But for the utmost in convenience, what better way to reload e-cash cards than using mobile smart phones?

Though this paper concentrates on the software issues of creating a portable PersonalATM, it is the mobile phone's hardware constraints that drive those of the software. Successful mobile phones must be small, lightweight, and inexpensive. Such phones typically use inexpensive electronics that consume little power. This means slow, less powerful CPUs and small memory capacities. Consequently, the smart phone system software must be small (to reduce ROM and RAM memory requirements) and efficient (to achieve satisfactory performance on slow CPUs, and to reduce power requirements).

All mobile phones do not need a software operating system. Many of today's mobile phones use microcontrollers and hardware DSPs (digital signal processors) that are controlled by custom firmware written by the mobile phone manufacturer. Smart phones benefit from incorporating a true operating system (OS) to control the phone and its features and applications, to optimize CPU usage. Such an OS must be "portable by design," to be compact, modular, efficient, well-integrated, easy to program, and extensible.

Using this assumed OS, a software architecture for a smart phone-based PersonalATM is shown in the figure. Layered and modular, the architecture provides basic OS functions (e.g., task scheduling and management, memory management, synchronization, timers); hardware and software drivers, to insulate higher-level application code from the particulars of the mobile phone hardware; shared libraries that provide common functionality for applications to use (e.g., file system, database, graphics and user interface, communications); and applications, for smart phone and PersonalATM functionality.

The software modules specific to the PersonalATM include a driver, a set of libraries, and an application. The smart card driver provides an interface for software to communicate with the smart card reader hardware. The smart card libraries provide high-level APIs to applications, so that the applications can communicate with different types of smart cards. PersonalATM would require libraries for an e-cash system, like Mondex or Visa Cash, but might also use additional libraries if more features besides just e-cash are supported. For example, the smart card could also be the SIM (subscriber identity module) for GSM (Groupe Speciale Mobile) mobile phones (GSM is a global standard for wireless digital telephony).

The PersonalATM concept uses the mobile phone to provide a service to the user of an e-cash card: convenient, anytime, anywhere reloading of stored value onto the card.The mobile phone, however, could provide more than just a convenient ATM for the user. Consider a smart phone with Web browsing capability—either unrestricted random URL surfing, or restricted visitation of targeted sights chosen specifically for their appropriate content for mobile users. Then smart phone users could visit these sites and access information.

Currently, Web site content providers have no means for collecting low-value payments (or "micropayments") for content. Billing systems aren't well-equipped to handle charging and collecting of sub-dollar payments, and sub-dollar credit card transactions aren't economically feasible. Stored-value smart cards could aid merchants on the World Wide Web. With a smart card inserted into the smart phone connected to the Web, content providers and merchants could collect minuscule amounts of money for individual Web pages, or for a single stock quote, or for a crossword puzzle.

***Paul Chen**, Geoworks. From the 1998 Portable By Design Conference.*

Engineering Lithium-Ion Batteries Into Your Application

One of the big challenges for design engineers in this fast changing world of portable designs is choosing the right battery to meet their product's requirements. Today, there are many options in cell chemistry, cell size, and configuration, making this choice even more difficult. To further complicate this process, the engineer must make decisions on battery-management circuitry, regulatory issues, and choose between a standard or custom package.

The question any product designer has to ask is, does my product really need this lithium-ion technology? Well, the answer is not completely cut and dried. Lithium-ion does have three advantages over its main competitor, NiMH: better high-temperature cycle life, better gravimetric energy density, and a low rate of self discharge.

For handheld portable equipment, where light weight is high on the design priorities, lithium-ion is the best choice, providing a high energy-to-weight ratio. Lithium-ion batteries will also provide a high energy-to-volume (space) ratio, although today's best NiMH batteries can nearly match lithium-ion in volumetric energy density.

In today's laptop computers, where heat dissipation is the performance-limiting factor, the lithium-ion battery produces less heat on charge and discharge than NiMH, allowing the designer to increase the performance of the processor. This, along with the better life cycle characteristics of the lithium-ion batteries at the elevated temperatures seen in laptops today, is making lithium-ion the choice for this type of product. It is estimated that by the end of 1998, 80% of laptops will use litium-ion batteries. Some manufacturers produce lithium-ion batteries that have good low-temperature performance. If this is a requirement for your product, check with each of the manufacturers. You may want to test their products under your low-temperature conditions to determine the best battery for your application.

Lithium-ion batteries are not the perfect choice for all applications. Any product that is very cost sensitive, like toys, could probably not justify the cost of using a lithium-ion battery. Applications that demand a continuous high-rate discharge (greater than 2C) would probably be better suited to NiCd or some other chemistry. An example of this type of high-rate application would be portable power tools. Products that do not require portability or are mounted on a vehicle may be able to choose a heavier battery technology that is less expensive than lithium-ion.

There are several cell-size options in both cylindrical and prismatic (flat or square) cells. The table shows some of the various sizes and typical capacities of products available today. Note the dimensions listed in the table are rounded off and that the exact dimensions of one manufacturer will not necessarily match those of another. Lithium-ion polymer cells have been omitted from the table, because they are not commonly available today.

Prismatic cells should be designed into the product only if there is a real need for the battery pack to be thinner than 17 or 18 mm. The 17- and 18-mm cylindrical sizes are made in great quantity and designing these into a product will give better "bang for the buck," when compared to a similar pack using prismatic cells.

Cylindrical	Dimension	Typical Capacity (mAhr)
	18 x 65	1350-1500
	17 x 67	1200-1300
	17 x 50	850-900
Prismatic	22 x 8 x 48	400-600
	34 x 9 x 48	800-900
	30 x 6 x 48	550-600

There are two methods used in determining the state-of-charge of a lithium-ion battery pack. The first and simplest method is to measure the open-circuit voltage of the battery. The second and more complex method is to use some kind of microcontroller to measure the current flow both in and out of the battery pack, to track the battery's remaining capacity. A voltage-based fuel gauge is a valid option, as the open-circuit voltage of a lithium-ion battery will indicate the state-of-charge. This type of gauge is only accurate under low- or no-load conditions (up to about C/10 discharge rates).

In systems where the equipment is required to report information like remaining run-time or puts a high or unstable current drain on the battery, the better choice for a fuel gauge would be the "coulomb-counting" option. This type of gauge is usually a microcontroller built into the battery pack that accurately measures and tracks the current flow out of and into the battery pack.

The most common charge method for lithium-ion batteries is constant-voltage with a maximum current limit. This is often called CC/CV or constant-current, constant-voltage. This type of charge requires a two-step charging algorithm. The charger should provide a constant current until the battery reaches the specified upper charge voltage.

At the upper charge voltage (4.1 V, for example) the charger should change to the constant-voltage mode and the current would taper off. This is similar to the charging techniques employed to charge lead-acid batteries. The difference for lithium-ion cells is that the charge sequence should be terminated and the tolerance for the charging voltage must be more tightly controlled.

Some manufacturers allow their lithium-ion batteries to be pulse charged. This technique is generally used in applications where a lithium-ion battery is an optional battery, used in place of the original NiMH battery. With this type of charge, the control circuitry is placed inside the battery pack. The host unit supplies a constant current and the control circuitry switches this charging current on until the upper charge voltage is reached. The control circuitry then switches off the charging current, allowing the battery voltage to relax. At some preset voltage limit, the control circuitry switches the charging current back on and the cycle repeats.

Mark Reid, Moli Engergy Ltd. From the 1998 Portable By Design Conference.

Extremely Wide-Band Antennas For Wireless Communication

The type of antenna presented in this paper was used for more than thirty years in some military applications where the bandwidth requirements are a few octaves. This antenna appears in the literature [1]-[5] bearing different names: the notch antenna, the LTSA (Longitudinal Tapered-Slot Antenna), etc.

The notch antenna is a printed travelling-wave antenna, which consists of a slot in the circuit ground plane fed by a microstrip line. The paper discusses the different characteristics of the notch antenna and its applications in wireless communication systems. Measured data proves the capability of this type of antenna to simultaneously cover a number of wireless communication bands.

The main advantages of the LTSA antenna are: 1. broadband operation, 2. low sidelobes, 3. excellent crosspolarization characteristics, and 4. integrability with other printed circuits.

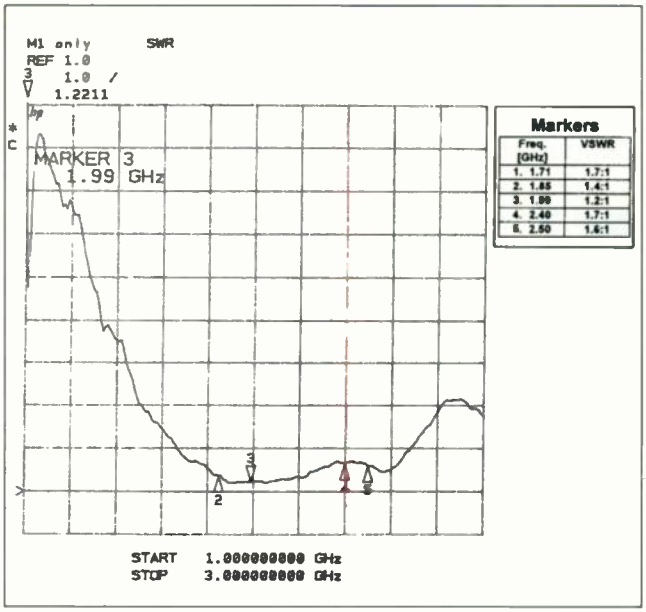
They are planar in nature, etched on a dielectric substrate and suitable for feeding by a variety of transmission lines: 1. microstrip lines, 2. stripline, 3. fin-line (waveguide), and 4. probe.

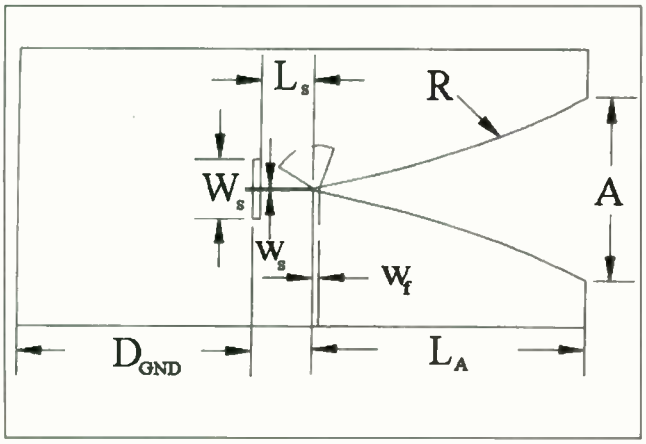
The basic geometry of the notch antenna is shown below. It consists of a cladded dielectric substrate, which on one side has etched a slot that ends in a stub, while the other end of the slot is flared and radiates in the endfire direction of the dielectric substrate. The shape of both the flare and the slot stub determines most of the characteristics of the antenna. The straight section of the slot is fed by a microstrip (in some configurations by a stripline) which ends in a stub.

The radiation is based on a travelling wave propagating in a slot with a phase velocity smaller than that of light, which results in an endfire radiation. Unfortunately, all the parameters have a direct impact on the input impedance. A comprehensive study of the impact of the parameters was done by Schaubert et al. [4,5]. Although the study deals with the scanning properties of infinite arrays of notch antennas, very useful information can be learned about the behavior of the single element.

An array of four notch antennas was designed and built. The figure above shows the VSWR of the array. The H-plane radiation patterns [at 1.71 GHz and 2.5 GHz] of this antenna are very wide, making it very suitable for base-station applications.

The fact that a printed circuit of approximately 4.0" by 3.0" ($0.45\lambda_0$ by $0.33\lambda_0$ at the lower end of the band) is efficiently radiating over a 1.71-GHz to about 2.7-GHz band (more than 50% bandwidth for VSWR less than 2:1) makes this type of antenna very attractive. A microstrip single-patch with similar dimensions would have a 4-8% bandwidth. This specific design can cover a number of wireless communication bands: PCN, PCS, low-ISM, and the 3.4-3.5-GHz European band.





The main, and probably only, two drawbacks of the notch antenna are: 1. Only linear polarization can be obtained (without complex construction). 2. The array has to be in the polarization plane—i.e., if the polarization needs to be vertical, the arraying has to be in the vertical plane, etc.

[1] K.S. Yngvesson, D.H. Schaubert, T.L. Korzeniowski, E.L. Kollberg, T. Thungren, and J. Johansson, "Endfire tapered-slot antennas on dielectric substrates," *IEEE Transactions on Antenna Propagation*, Dec. 1985, Vol. AP-33, pp. 1392-1400.

[2] L.R. Lewis, J.H. Pozgay, and A. Hessel, "Design and analysis of broadband notch antennas and arrays," *Digest, IEEE International Symposium on Antenna Propagation,* Amherst, Mass., Oct. 1976, pp. 44-47.

[3] D.H. Schaubert, "TSAAIR-analysis of tapered-slot antennas with air dielectric," Antenna Lab Report, 1992, University of Massachusetts, Amherst, Mass.

[4] J. Shin and D.H. Schaubert, "Toward a better understanding of wideband Vivaldi notch antenna arrays," *Proceedings, 1995 Antenna Applications Symposium,* Allerton Park, Sept. 1995.

[5] D.H. Schaubert, "Characteristics of single polarized phased-array of tapered-slot antennas," *Proceedings, IEEE International Symposium on Phased-Array Systems and Technology,"* Oct. 1996, pp. 106.

[6] P.J. Gibson, "The Vivaldi aerial," *Proceedings, 9th European Microwave Conference,* 1979, pp. 101-105.

Naftali Herscovici, Cushcraft Corp. *From the 1998 Wireless Symposium.*

Technical Program Highlights A Variety Of Wireless Applications

The Sixth Annual Wireless Symposium Focuses On Practical Solutions For Component- And System-Level Designs. **Victor Perrote**

Keeping up to date with technological progress is an essential part of any engineer's professional development, particularly in the constantly evolving and competitive wireless industry. Fortunately, technical professionals attending the sixth annual Wireless Symposium and Exhibition will be provided with a wide array of presentations and workshops that promise to satisfy their continuing-educational needs in this dynamic field.

Jointly sponsored by Microwaves & RF, Wireless Systems Design, and Electronic Design, the Wireless Symposium is scheduled to be held Feb. 9-13 at the Santa Clara Convention Center, Santa Clara, Calif. The conference features nearly 70 half-hour technical presentations and 14 workshops that will offer attendees the opportunity to learn from leading engineers in the wireless field as well as to exchange design ideas.

This year's keynote presentation, addressing the theme "Building on the wireless boom," will be given by Mark Golden, senior vice president of industry affairs for the Personal Communications Industry Association (PCIA), Washington, D.C. Golden directs the organization's legislative, regulatory, and industry development activities.

THREE KEYNOTES SCHEDULED

Attendees at this year's event also will be treated to three "visionary keynote" sessions that provide insight on topics of interest to the wireless and portable engineering community. Gilles Delfassey, vice president of the Texas Instruments Semiconductor Group, Dallas, Texas, and worldwide general manager of the company's Wireless Communications Business Unit, will cover the theme "Making wireless work in the next century." Bob Pease, veteran analog engineer at National Semiconductor, Santa Clara, Calif., and popular columnist for Electronic Design, will offer his views on the future of portable and wireless technology. Amory Lovins, director of research for the Rocky Mountain Institute, Snowmass, Colo., will focus on energy-conservation issues in a session titled "Laptops to hypercars—the wide-ranging impact of portable technologies on traditional industries."

This year's meeting features the return of several popular courses. Randall Rhea, well-known in the high-frequency community as founder of computer-aided engineering (CAE) software developer Eagleware Corp., Stone Mountain, Ga., as well as Noble Publishing, Tucker, Ga., will be joined by Glenn Parker, chief engineer at Eagleware, to deliver a two-day workshop on "Active, digital, and RF filter design." The course describes time- and frequency-domain approaches as well as transfer functions, emphasizing practical design issues at frequencies from baseband to the microwave range.

In addition, Rhea will present a one-day workshop on "Oscillator design for wireless applications." This course covers such topics as S-parameter calculation, noise, biasing, broadband tuning, and linearity. Design examples based on quartz crystals, inductor/capacitor (LC) networks, surface-acoustic-wave (SAW) devices, and transmission lines also will be presented.

Also returning is a three-day workshop titled "Wireless RF circuit design." The first part of the workshop is a one-day course on small-signal and low-noise amplifiers taught by Dr. Les Besser of Besser Associates, Los Altos, Calif., a pioneer in the fields of microwave CAE and continuing education. Besser will address such topics as S-parameter analysis, noise-figure, matching, and stabilization. Design trade-offs will be examined with the help of graphical tools.

The second part of the workshop is a two-day course on high-efficiency power-amplifier design. Presented by industry veteran Dr. Steve Cripps of Besser Associates, this course will examine design techniques for bipolar- and FET-based amplifiers, focusing on practical applications. Load-pull and linearization techniques will also be described.

Aimed at technical managers and marketing professionals, a two-day course titled "Wireless made simple" offers a tutorial-level overview of RF and wireless technology. Taught by Allan Scott of Besser Associates, the workshop will devote one day to RF principles, systems, and devices—with the second day focusing on wireless terminology and design. Modulation techniques, system functions (including error correction and voice coding), and wireless markets will be overviewed.

Returning for the sixth consecutive year, Professor Jack Holtzman of Rutgers University's Wireless Information Network Laboratory (WINLAB), New Brunswick, N.J., will offer a half-day course on the fundamentals of spread-spectrum modulation. The workshop reviews the implementation and benefits of spread-spectrum techniques on system design. Among the topics to be covered are system capacity, processing gain, code sequences, and power control.

Techniques for accurate evaluation of wireless signals will be explained in a one-day course titled "Measuring the wireless transmission spectrum" taught by Morris Engelson, long-time chief engineer at Tektronix, Beaverton, Ore., and now the president of Joint Management Strategy, Portland, Ore. Regarded by many as the "father of the spectrum analyzer," Engelson will discuss such topics as the measurement of digitally modulated signals, EMI, pulsed signals, and television signals, focusing on the use of this versatile evaluation tool.

WORKSHOPS ADDED THIS YEAR

This year marks the introduction of several half- and full-day workshops to the Wireless lineup. For instance, Dr. Steven Best, director of engineering, and Dr. Naftali Herscovici, chief scientist at Cushcraft, Manchester, N.H., will deliver a one-day workshop on "Antenna and array design for wireless communications." This course covers topics such as electromagnetic-field analysis, selection of antenna types, propagation, and simulation. These concepts will be applied to the design of an actual antenna.

The complex transmission formats used in wireless communications systems will be explained in a one-day course titled "Introduction to digital modulation methods." Presented by Harold Walker, chief executive offer of Pegasus Data Systems,

Middlesex, N.J., this workshop will review the latest advancements in digital modulation as well as the operation and implementation of these techniques. The characterization of systems using signal-to-noise ratio (SNR), carrier-to-noise (C/N) ratio, and bit-error rate (BER) will be discussed.

Also being offered for the first time is a one-day workshop on wireless transceiver design. Taught by Syed (Moti) Ahmed, president of Analog Communications, Flemington, N.J., this course will review the design and implementation of RF transceivers and their functional blocks—including the antenna, duplexer, receiver, transmitter, and synthesizer subsystems. Digital signal processing and modulation techniques also will be discussed.

FOR ENTREPRENEURS

Targeting prospective entrepreneurs, a half-day workshop titled "Strategic financing and high-growth business paradigms" will discuss such topics as market research, product penetration, market share, and strategic planning. Ken Schoniger and Al Juodikis of KC Press International, San Jose, Calif., will be joined by experts in technology and finance to share their views on these key business issues. The course aims to provide attendees with the tools needed to communicate with the investment community.

Another half-day workshop being given for the first time at the conference is "Phase-locked loops and frequency synthesis for wireless design engineers." Presented by Eric Drucker of Fluke Corp., Everett, Wash., this course will cover the fundamentals of phase-locked loop (PLL) analysis, design, and modeling while keeping mathematical theory to a minimum. Among the topics discussed are the effects of phase noise as well as real-world problems such as power-supply noise and isolation.

The technical sessions in the Wireless program run Feb. 10-12. The sessions include "Cellular/cordless design," "Digital communications systems," "Modulation techniques," "Point-to-point and base-station design," "Materials and packaging technologies," "Test and measurement solutions," "Wireless data transmission," "Automotive and satellite systems," "Integrated-circuit solutions," "Wireless local-area networks," "Personal communications services," and "High-power design."

Victor Perrote is senior editor at Microwaves & RF magazine, a sister publication of Electronic Design.

***Originally published** in Electronic Design, January 12, 1998.*

Design Conference Becomes Launch Pad For Portable Components

The Latest Products And Technologies Boasting Small Size And Reduced Power Are Unveiled At Portable By Design. **Richard Nass**

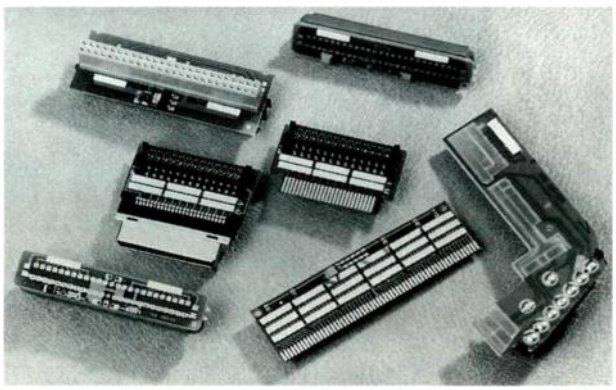
If you crave the latest in portable products and technologies, the place to go is the Fifth Annual Portable by Design Conference and Exhibition, held at the Santa Clara Convention Center, Santa Clara, Calif., February 9-12. As in previous years, the exhibition proves to be the showcase for portable-component vendors to unveil their latest products. Such products range from batteries to displays to passive components.

It's no secret that battery technology has come a long way recently. One example is the Molicel lithium-ion battery, from NEC Electronics Inc., Santa Clara, Calif. The cylindrical and prismatic rechargeable batteries target consumer applications as well as portable devices. the batteries are deemed as replacements for traditional nickel-metal-hydride and nickel-cadmium batteries.

According to the company, the lithium-ion batteries incorporate a "smart" technology, called SBS, which means that it can measure, calculate, update, and communicate accurate battery-status and usage information to the host device. Running at 11.1 V nominal, the battery provides 45 Wh of energy. The SBS compliance also ensures that the battery can send its charging requirements to an SBS-compliant charger, allowing it to configure the charging supply with the necessary current and voltage. This helps maintain a full-charge potential. Most of the batteries are available immediately.

A second battery type hails from AER Energy Resources Inc., Atlanta, Ga. The company will display its line of zinc-air products at Portable by Design. The company's latest products are of the smaller variety, specifically for hand-held computers. For example, a prototype cell is about 70% smaller than its replacement. A battery pack containing three of these cells should provide up to five times the battery run time of two conventional AA alkaline batteries. As a result, users can get several weeks of run time between recharges.

Displays promise to be another area of discussion at the conference. Kent Displays Inc., Kent, Ohio, will show its latest display, a one-eighth VGA Cholesteric LCD (ChLCD) module. The company claims that its ChLCDs offer better reflectivity, a 360° viewing cone, and exceptional daylight contrast—even in direct sunlight—all without the need for back lighting. Other features include a peak reflectivity of 40% and a 25:1 contrast ratio. In addition, the ChLCD technology offers the power-management features needed for portable applications. ChLCDs are bistable, meaning that once an image is written to the display, it doesn't require the power-draining refresh cycles associated with standard LCDs to remain visible.



A line of surface-mount chip resistor networks can replace discrete resistors and arrays. The variable thick-film leaderless chip resistor networks offer a 25% to 35% space savings over SIP networks, discrete resistors, and arrays.

A line of interdigitated capacitors (IDCs) give circuit designers inductance values as low as 175 pH, whereas a conventional capacitor could have an inductance of more than 1200 pH. Developed by AVX Corp., Myrtle Beach, S.C., the decoupling capacitors are designed for use with high-speed microprocessors, digital-signal processors, and memory devices operating at speeds greater than 300 MHz.

The capacitors' low inductance is achieved by connecting the capacitor with a series of eight vias to the power and ground planes in an alternating (interdigitated) pattern. The geometry of these elements is alternated, which alternates the inductance values, ultimately canceling each out.

A wide range of doubly rotated crystals was designed by Oak Frequency Control Crystals, Whitby, Ontario. The family includes SC, FC, and IT cuts from 4.333 to 160 MHz in various conventional through-hole and SMD holders. The devices are suited for use in ovenized oscillator applications with oven temperatures from 60° to 110°C. They feature long-term stability (as low as 10 ppb/yr. aging) and improvements in phase noise, frequency-temperature stability, and vibration sensitivity when compared to equivalent AT-cut devices.

Portable by Design attendees will witness the debut of a line of surface-mount chip resistor networks which can replace discrete resistors and arrays. Made by the Methode Development Company, Chicago, Ill., the variable thick-film leaderless chip resistor networks offer a 25% to 35% space savings over SIP networks, discrete resistors, and arrays *(see the figure)*. The leaderless design enables circuit miniaturization and offers a lower surface profile than many other surface-mount components.

The resistor arrays are printed on a 96% Alumina substrate. Multiple values of resistors can be printed on one substrate. Standard and custom-sized packages are available in either isolated or bused configurations. Tolerance ranges are ±1% to ±20% with a power capability of up to 0.25 W. Suitable applications include automotive electronics, PCs, cellular communications, and consumer electronics.

One technology that's starting to pervade portable electronics is the Miniature Card, which can be employed to record and store information. Removable and reusable, the matchbook-sized cards are employed in digital cameras, voice recorders, smart pagers, cellular telephones, and personal digital assistants. Such a card was developed by Duel Systems, San Jose, Calif. The card measures 38 by 33 by 3.5 mm, and is currently available in 3.3-, 5-, and 3.3/5-V combinations. The card's two-piece design snaps together for easy testing prior to welding.

***Originally published** in Electronic Design, January 26, 1998.*

Technical Conference Zeros In On Portable-Product Design

All Aspects Of The Portable Design Process Will Be Discussed, Including Batteries, CPUs, And Analog And Digital Circuitry. **Richard Nass**

Like its four predecessors, the Fifth Annual Portable By Design Conference and Exhibition promises to be an event that designers of portable products would label as a "must attend." The conference, which runs Feb. 9-13, is comprised of twelve application-oriented technical sessions, augmented by three detailed workshops. In addition, this year's keynote speech, given by David Hancock, president and CEO of Hitachi PC Corp., San Jose, Calif., will give designers a fascinating peek into the future of the industry. Hancock's speech will take place during the keynote luncheon on Tuesday, Feb. 10, at 11:30 a.m.

The three workshops will be held on Monday, Feb. 9. The first is titled "EMC problems and solutions for portable electronics." The bulk of the discussion will center on common electromagnetic compatibility (EMC) problems in portable electronic equipment. More importantly, it will offer numerous practical solutions for solving those problems. It starts with the physics of electromagnetic interference (EMI), emphasizing the FAT-ID (frequency-amplitude time impedance and dimensions) approach to grounding and shielding as related to portable design. It continues with a number of case histories of EMC problems, along with how they were solved. The workshop will be presented by William Kimmel of Kimmel Gerke Associates, West St. Paul, Minn. Kimmel has over 30 years of experience in EMC design and troubleshooting in military, automotive, industrial, medical, and commercial applications.

The second workshop focuses on infrared data transfer. Titled "Working with the IrDA serial infrared protocol," this class looks at different aspects of the IrDA (Infrared Data Association) standard, including the physical layer, the link access protocol (IrLAP), the link management protocol (IrLMP), the tiny transport protocol (TinyTP), and serial and parallel port emulation (IrCOMM). The instructors will begin with an overview, then go into detail on each of the subjects. They will conclude with a series of implementation and testing strategies. The presenters have served on various IrDA committees and have lectured on many subjects concerning infrared connectivity.

The final workshop covers "Battery basics." Delivered in a tutorial fashion, it develops the basis for total battery-system management, including control of charge, discharge, and storage modes, and how these modes affect system reliability. A review will be given of important physical fundamentals and how these cell attributes relate to a battery system's performance and reliability. A detailed review will be given of the electrical double-layer structure and mass-transport properties that dominate the performance of the battery system. A control method will be described whereby the applied electromotive force optimizes the electrokinetic behavior of the charged particles to maximize the performance and reliability of the battery system. The workshop will be presented by Floyd Williamson of ZAE Research Inc., Huntsville, Ala.

IT ALL STARTS WITH THE BATTERY

The conference's technical sessions, which take place from Tuesday, Feb. 10 to Thursday, Feb. 13, each run for three hours. The first, called "Rechargeable batteries: Today and tomorrow," is chaired by Barry Huret, Huret Associates, Yardley, Penn., and Anthony Wong, Energizer, Westlake, Ohio.

It's no secret that sufficient run-time, lighter weight, and ease of use are the criteria that remain in the sights of portable-system designers. As electronic packaging becomes smaller and denser, and demands more energy, the batteries that power the systems need to make corresponding increases in power density and available run time.

While the responsibility is on the battery manufacturers to develop newer and improved chemistries, it also is up to the system designers to utilize the technology that is best suited to their products. Unless a single, all-encompassing battery technology appears, there will continue to be many options to choose from, and a need to evaluate the best correlation between form, fit, function, and cost-benefit. This session will help correlate these two issues by discussing battery chemistries that are currently available, and new technologies expected in the near future.

Low-power microprocessors, including standard embedded processors, microcontrollers, and digital-signal processors, have become an essential component in almost every portable system, from battery-powered games to portable medical instruments to cellular telephones. The session called "CPUs and DSPs for portable devices" will provide an overview of the latest low-power 8-, 16-, and 32-bit embedded processors and microcontrollers and digital signal processing (DSP) chips aimed at battery-powered applications. The technical papers will examine the various architectural directions taken by each family and the new application areas they open up thanks to improvements in performance and integration.

While designers of portable systems know that some knowledge of a battery subsystem is required to develop a battery-based system, it's often important to deal with the battery as a "black box," meaning that the most important element is how to deal with the signals that are coming from and going to the battery, not necessarily what's happening inside the battery itself. The "Battery subsystem session," chaired by David Heacock of Benchmarq Microelectronics, Dallas, Texas, deals with the battery as a "pins-out" subsystem, giving designers just the information needed to build a battery-powered system.

With customers demanding more functionality, smaller size, and greater reliability in their mobile systems, designers continue to wrestle with IC packaging, system cooling, and shock/vibration issues. To help designers meet this challenge, the "Mobile-system packaging concerns" session will discuss some of the latest IC packaging options, along with novel system-cooling techniques. In addition, an analysis of system behavior under severe shock will show attendees what to expect and how best to isolate a portable system from its effects.

"Portable-system software issues" covers a number of critical software topics that affect the design of portable systems. Among

them are how to make efficient and modular operating systems that work with compact programs to minimize memory space and support the newest peripherals, such as flash memory. Other issues include using power-management software, which can play a vital role in maximizing battery life. In addition, network and Internet software will play a role in helping portable devices communicate. The last portion of the discussions will involve Java, as it appears destined to have a major influence on the design of portable and handheld systems.

RESPONSIBLE ENGINEERING

The session title says it all: "Designing for the environment doesn't have to be expensive." Within the next decade, we can expect to see environmental concerns becoming an integral part of the design process. Practices such as designing for recyclability and analyzing the environmental costs of producing a product will be as much a part of the engineer's responsibilities as designing for cost and manufacturability. In this session, attendees will meet with some of the pioneers in the Design For the Environment (DFE) movement who are charting the course of this emerging technology. In addition to providing an overview of the field, they will present an array of papers covering everything from "green computer" design to working with the new ISO 14001 environmental audit standard. Wherever possible, emphasis will be on practical solutions that can be implemented in a globally competitive business environment.

The common thread for the "Battery management" session is the Advanced Control and Power Interface (ACPI). Chaired by John Milios of USAR Systems, New York, N.Y., the session will focus on the role ACPI plays in system design, from the operating system, to smart batteries, the chip set, the SMBus, and embedded controllers.

Infrared ports are now popping up in the strangest places, including pay phones, cellular phones, fax machines, and medical equipment. The low cost, simplicity, speed, and versatility of infrared data transfer is quickly making it the wireless equivalent of the ubiquitous RS-232 port. Presenters in the session titled "Infrared data: A technology for universal connectivity" will introduce the fundamentals of infrared technology, as well as explore some of the latest developments in the field. Attendees also will have the opportunity to learn about several innovative applications of infrared data and how they can incorporate it into their next design. The session is chaired by Dr. Keming Yeh of ACTiSYS Corp., Fremont, Calif.

Designing for portable applications requires that designers make a number of critical decisions that will significantly impact the end product, not the least of which is identifying the most appropriate system, architecture, and bus. The session dubbed "Systems, buses, and architectural issues" will discuss some of the choices now available, how they can be implemented, and the benefits to be derived from such an implementation choice.

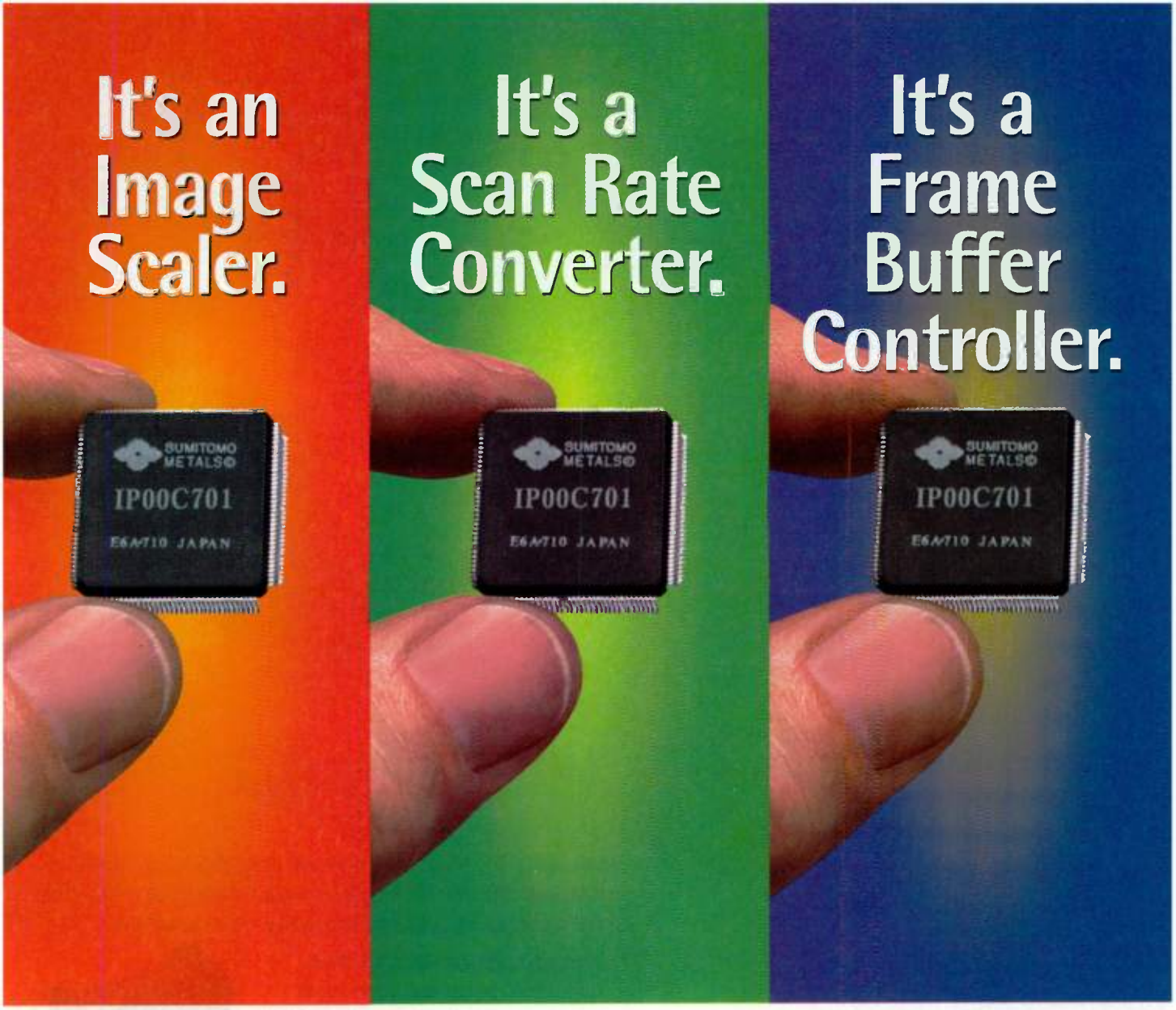
What good is a rechargeable battery if it can't be charged properly? The "Charging circuits session" will explore what techniques are available to charge different types of batteries, and how the charging techniques can be employed to get the fastest charge, while maintaining the maximum number of charge cycles for the battery.

It's no surprise that portable equipment contains a number of different components that are strictly governed by size, cost, and performance requirements. In fact, size and cost requirements often compete with demanding performance specifications. As a result, many low-power electronic components are designed and integrated into modules that combine different types of technology. This session, "Low-power analog circuit design," chaired by James Harrer of LG Infocom, San Diego, Calif., will attempt to identify the latest advances in components and integrated modules for use in the highly competitive portable marketplace.

Finally, with displays playing such an integral role in the proliferation of today's portable applications, it's becoming more critical than ever to develop components and technologies suited for such environments. "Displays for portable and handheld computers" will attempt to identify some of the latest display developments that address many of the needs of present portable applications, and some of the other, not yet viable, applications.

***Originally published** in Electronic Design, January 12, 1998.*

INDEX OF ADVERTISERS



Now it's all on one LSI.

When it comes to interfacing video – from NTSC up to SXGA to Flat Panel displays and beyond – SMI's new "Screen" LSI, the IP00C701, is the one chip you need.

And we don't dither around! You get true digital (four point bi-linear) interpolation with our proprietary sharpening filter for high-quality scaling. Two high-speed totally independent and asynchronous ports have no wait states. Plus, the port configuration and window can be changed dynamically on the fly, both input and output ports can be interlaced or non-interlaced, and frame buffer memory can be up to 128 MB SDRAM or SGRAM.

SMI's advanced LSI is designed to exceed your specs at a better total solution price. It's also easier to implement, uses less space and offers a more dynamic design than the competition.

For complete specifications on the C701 and information on SMI's entire family of pipeline processors for image processing and machine vision, contact us now.

SUMITOMO METALS

1-800-392-4447

Park 80 West Plaza 1, 3rd Floor, Saddle Brook, NJ 07663 • Phone: (201) 845-0980 • Fax: (201) 845-5139
5201 Great America Parkway, Suite 320, Santa Clara, CA 95054 • Phone: (408) 982-2503 • Fax: (408) 982-2522
Visit us at: www.smi-lsi.com

READER SERVICE 156

We Have Thermal Printer Mechanisms To Meet Any Demand.

(wherever it may be)

Making the jump to portable and wireless print solutions can be risk-free with Seiko's LTP Series high-resolution thermal micro printer mechanisms. And keeping record of the experience will be even more exciting.

They feature the lightweight, low power consumption performance you need, for everything from battery-powered applications to demanding POS and field testing environments. There's a model for just about any idea you can think of, along with one of industry's best reputations for customer service and reliable performance.

Models LTP2342 and LTP1245
ISO 9001 Certified

For more information, visit our web site for applications guides, complete technical data and more. You can call too at (800) 553-6570, ext. 827, fax (310) 517-8154 or e-mail: siumpd.id@salessupport.com

Because when you want to reach new heights in quality, Seiko thermal printers really hit the mark.

www.seikoprinters.com

SII
Seiko Instruments

Total Solutions In Thermal Technology

READER SERVICE 157

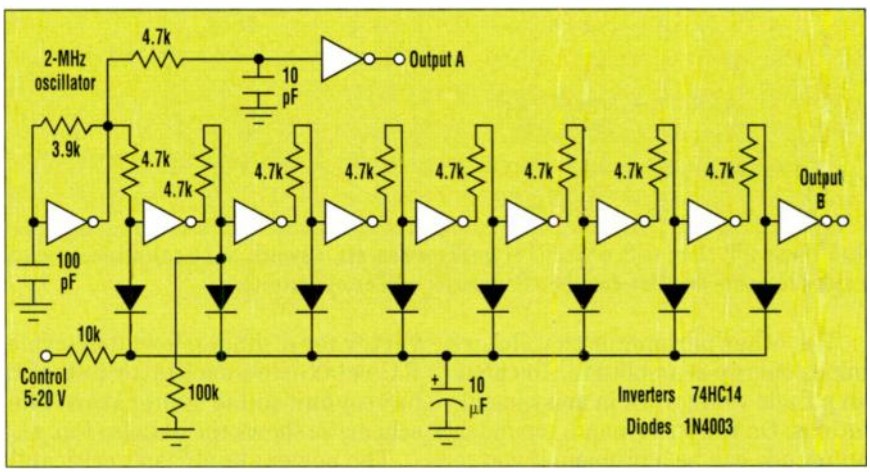
Circle 520

Variable-Capacitance Diode Phase Modulator

PAUL BENNETT
6 Dighton Gate, Stoke Gifford, Bristol, BS34 8XA, United Kingdom;
phone: 44 117 9793883; e-mail: paul.bennett@trikon.com.

This circuit varies the phase between two squarewaves through at least 180°. This capability finds application in fixed-frequency, phase-shift, resonant-mode converters. ICs such as the UC3875 usually only work up to about 500 kHz, whereas this circuit can be extended up to tens of megahertz. In addition, the circuit shown uses low-cost components. This example was used for a high-efficiency 2-MHz RF power supply.

The signal is delayed at each gate by the RC network formed by the 4.7k input resistor and capacitance of the 1N4003 diode. The capacitance of the diode, and hence delay, can be varied by controlling the reverse dc bias applied across the diode. The 100k resistor to ground at the input to the second stage corrects a slight loss of 1:1 symmetry. The fixed delay for output A adjusts the phase to be approximately in phase at a 5-V bias. Note that the control voltage should not drop below approximately 3 V, because the diodes will start to be forward-biased and the signal will be lost.



This inexpensive phase-control circuit can operate at input frequencies up to tens of megahertz.

Circle 521

Build Your Own "Cable Radar"

GUNNAR ENGLUND
S-691 92 Granbergsdal, Sweden; phone: 46 586 12266;
fax: 46 586 12316; e-mail: gke@swipnet.se.

A time domain reflectometer (TDR) is a handy but rather expensive instrument, and isn't commonly found on every bench. I used to rent them, but after having paid large bills for several years, I decided to make my own. I saved a bundle and was able to customize it for my needs.

A TDR performs a number of tasks, such as:

- sending a well-defined voltage pulse down the line and waiting for the echo.
- displaying the pulse and echo on a fast oscilloscope screen.
- measuring echo time to find cable length or distance to fault.

If you look at the list, you will find that a modern oscilloscope will do most of the job. The only thing needed for the TDR function is pulse generation. It turned out to be much easier to build than I had expected. A simple hex inverter in Advanced CMOS technology (74AC14) does the job admirably.

There are five basic design parameters that must be addressed: rise time, pulse width, amplitude, impedance, and PRF.

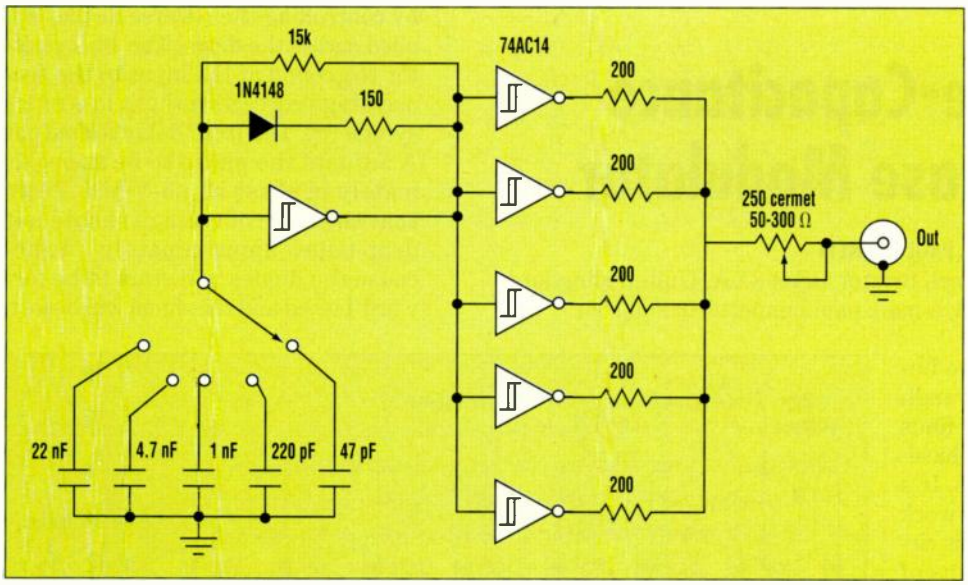
To be useful, the pulse should have a rise time that corresponds to the desired distance resolution. If you need 1-m resolution, then better than 10 ns is required. This design has a resolution better than 5 ns.

The pulse width can be quite short for short cables, but needs to be longer for greater length cables so that enough energy is introduced in the cable. If the energy is too low, there won't be enough energy in the return wave to be detected reliably. This design allows a choice between 15 and 2500 ns. The 2500-ns pulse width will produce enough energy for a 5- to 10-km cable.

IFD WINNERS

Jim Hagerman, Science & Technology International Inc., 733 Bishop St., Suite 3100, Honolulu, HI 96813. The idea: "*π Filter Has Notch Just Outside Passband.*" October 1, 1997 Issue.

W. Stephen Woodward, University of North Carolina, Venable Hall, Chapel Hill, NC 27599-3290; The idea: "*Single-Supply Op-Amp Bias-Current Cancellation*" October 13, 1997 Issue.



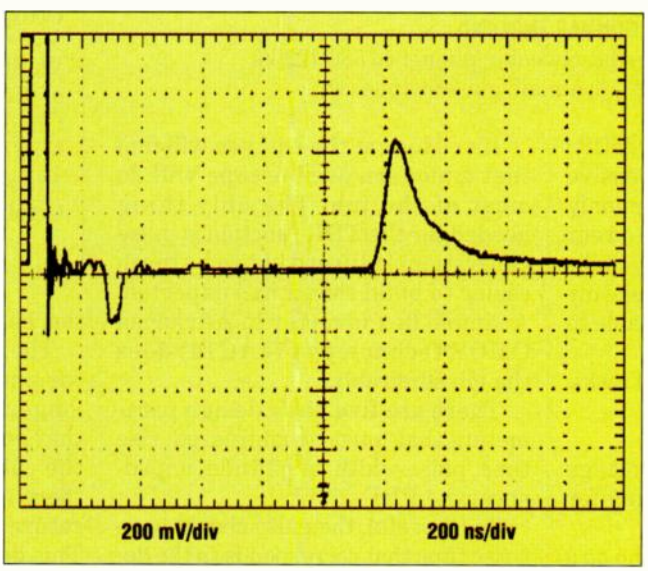
1. A 14-pin DIP, along with a handful of small components, a switch, and a potentiometer are all that's needed to create this time-domain-reflectometer oscilloscope accessory.

The other parameter that determines energy is amplitude. Too little amplitude won't work in noisy installations. On the other hand, too much amplitude can be a problem if you're working in installations with other cables that can pick up EMI and cause undesired responses in the system. Amplitudes between 1 and 10 V seem to serve most applications. This design uses 4 to 5 V as dictated by battery voltage.

Ordinary cables have impedances in the 50-300Ω range. Using a 250-Ω potentiometer (the low-inductance type) and a fixed generator impedance (50 Ω), any impedance in that range can be achieved.

A 14-pin DIP, a handful of small components, a switch, and a potentiometer is all that's needed. The 74AC family has quite hefty specifications. Among the features are 24-mA symmetrical sink/source current, and output impedance in the tens of ohms range. A 200- or 220-Ω resistor in series with each output will produce approximately a 250-Ω impedance. Paralleling five such circuits will give you close to 50-Ω impedance. And that's about as low as you are likely to need. Most cables are in the 50- to 300-Ω range. Use the spare inverter for a simple, low duty-cycle RC relaxation oscillator and you have your pulse generator. The schematic shows the details *(Fig. 1)*.

The power supply isn't critical; I used three alkaline AA cells. Battery operation is very favorable—the batteries seem to last forever. If you use a battery-operated scope, like the THS 720 or 730, you will get better results than possible with an ac-powered instrument. The reason for this effect seems to be that some noise is introduced via the power-supply transformer capacitances.



2. The detected echo signal for a 100-m cable with 500-Ω shunt resistance located approximately 20 meters from the start. The big echo at 1.1 µsec indicates where the cable ends.

Construction is very straightforward. I used a ground plane and hook-up wire for my prototype. Later, I had a pc board made, and it works just as well. One factor must be kept in mind, though—good power-supply decoupling. I use a small (1 nF) ceramic disk and a 1-µF foil capacitor.

Figure 2 shows a 100-m cable with 500-Ω shunt resistance some 20 m from the start. The pulse that's being sent down the cable starts at 40 ns.

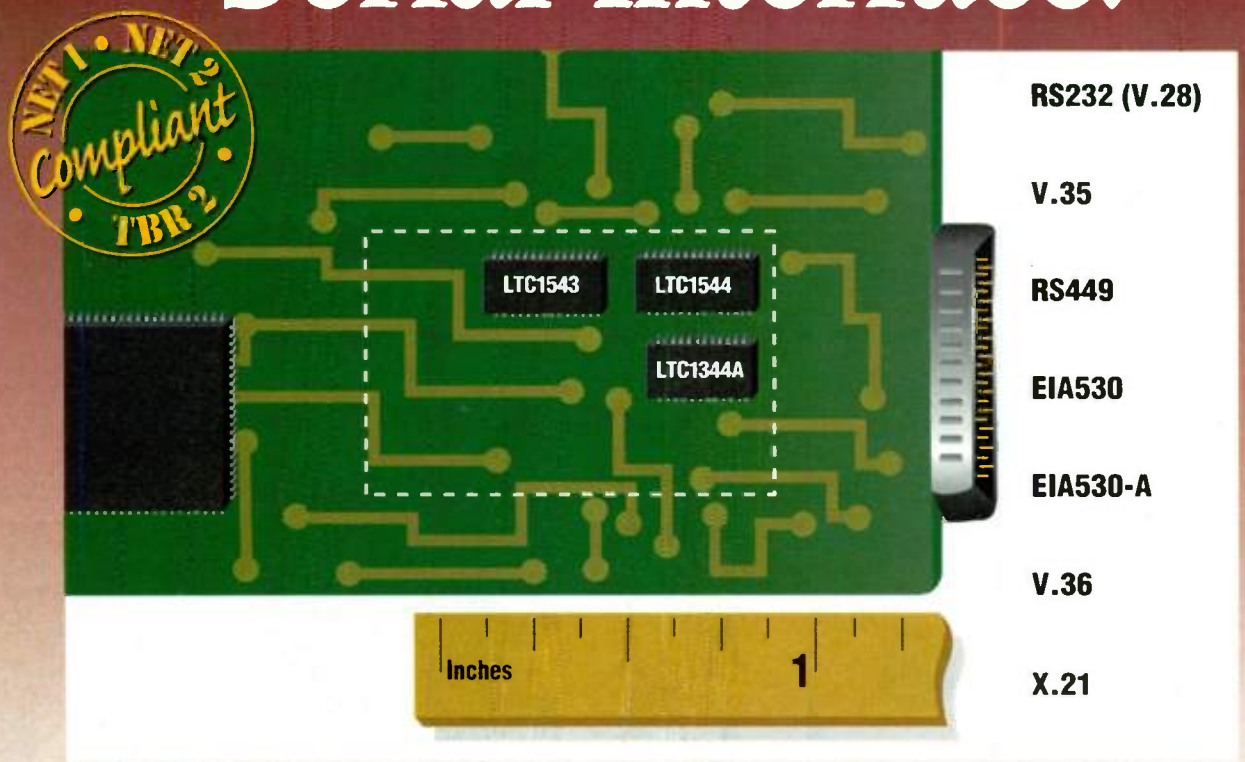
In this case, the wave impedance of the cable is approximately 150 Ω. The propagation speed is a little less than 200 m/µs. Because the wave has to travel both ways, the large echo at 5.5 divisions (1.1 µs) from the pulse's front edge tells us where the cable ends. The fact that it goes positive tells us that the cable is open at the end.

The little echo observed 280 ns from the start is from a 500-Ω shunt resistor that should not have been there. The echo goes negative since this extra load lowers the impedance at this point.

Checking a LAN cable using this TDR is easy. By connecting to one end of the cable and looking at the echoes (there should be no echoes in a well-terminated cable), you can easily see if anything is wrong with the loading, terminators, or joints.

It's just as easy to locate a fault in a buried cable using this TDR. Connect the TDR to one end of the cable and see if there's any extra echo (going down if there's an extra load or a short, going up if there's a bad connection or an open cable). If one exists, you can be certain where the fault is located. The distance can be calculated from the delay (most cables have bidirectional wave speeds between 100 and 110 m/µs, so the calculation is very easy). By doing this, you will not need to dig an unecessarily long trench to repair the cable. You only dig where the fault is. The "cable radar" also is a great tool when checking antenna cables.

Multiprotocol Serial Interface!



LTC Multiprotocol: Interface any Router or Modem for Remote Access with a Single Connector.

The LTC1543, LTC1544 and LTC1344A include all of the transceivers for clock, data and control signals as well as switchable termination for the popular WAN serial protocols. And it's been certified for NET1, NET2 and the more stringent TBR2. No external resistors, no jumpers or relays and no time-consuming debugging for compliance testing—just drop it in and go!

Features

- LTC1543 - Triple Transceiver for Data and Clock
- LTC1544 - Quad Transceiver for Control Signals
- LTC1344A - Switchable Terminator
- Certified NET1, NET2 Compliant
- TBR2 Compliant
- Operates from a Single 5V Supply
- Configurable as DTE or DCE Port
- 28-lead / 24-lead SSOP Packages
- 3-Chip Set Pricing Starts at $17.65 each in 10,000 Piece Quantities

Protocols Supported

- ☑ RS232 (V.28)
- ☑ V.35
- ☑ RS449
- ☑ EIA530
- ☑ EIA530-A
- ☑ V.36
- ☑ X.21

Data Sheet Download

- www.linear.com/go/LTC1543/edes
- www.linear.com/go/LTC1544/edes
- www.linear.com/go/LTC1344A/edes

Free CD ROM

Call: 1-800-4-LINEAR
Visit: www.linear-tech.com

More Information

Lit: 1-800-4-LINEAR
Info: 408-432-1900
Fax: 408-434-0507

LINEAR TECHNOLOGY

FROM YOUR MIND TO YOUR MARKET
AND EVERYTHING IN BETWEEN

READER SERVICE 162

MORE SRAMs.
MORE THROUGHPUT.
MORE TALK TIME.
MORE SOLUTIONS.

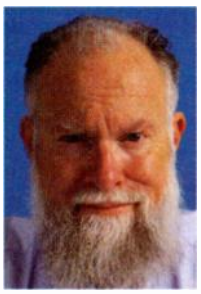
Presenting more of the SRAM solutions you need most. Whatever your SRAM needs, turn to Cypress—the SRAM solutions company. Need more throughput? Consider our synchronous NoBL™ (No Bus Latency™) SRAMs. They'll double your networking bandwidth by eliminating memory bus bottlenecks. They're available in 2- and 4-Mbit versions and are 100% ZBT™-compatible. More talk time? Our micropower SRAMs are circling the globe in Motorola digital handsets and Ericsson pagers, and our next generation—the industry's lowest-active-power family of devices—is just around the corner. More choices? From our base 1-Kbit to 4-Mbit asynchronous line to our rapidly expanding line of synchronous flowthrough, pipeline, and NoBL products, in 100-pin TQFP packages, our SRAM portfolio is among the broadest in the business. More information? For a sample request card and literature kit, call 800 858 1810 and ask for Kit #S016. Or see us at www.cypress.com/srams.

Arch.	Mode	Density	Freq.(max) (FT/Pipe)	Config
NoBL	FT/Pipe	2 Mbit	66/133 MHz	x32
NoBL	FT/Pipe	4 Mbit	66/133 MHz	x18, x36
Sync	FT/Pipe	2 Mbit	117/133 MHz	x18, x32, x36
Sync	FT/Pipe	4 Mbit	117/133 MHz	x18, x32, x36

CYPRESS

BY ENGINEERS. FOR ENGINEERS.™

Bob's Mailbox



I know you're probably expecting a column this issue, but I switched things around due to unforeseen stuff. /rap

Hello Bob:

Just thought I would add my two-penny worth to the child punishment debate. Whilst bringing up our three children (the eldest is now 8), my wife and I have always considered that a swift but scaled punishment (i.e., a smack) is always preferable to a deferred punishment (i.e., no biscuits for a week). *(I would never say that is NEVER an appropriate punishment. It might be appropriate for some premeditated crime. /rap)*

In my experience, a young child loses focus of *what* the punishment is *for* after a few minutes. I think it is very important, however you punish your children, to allow the child to relate the punishment to the crime. *(I tend to agree. /rap)*

If the child does not understand what is wrong, punishment will only cause confusion. *(Even for DOGS, people have learned this! /rap)* We have both found that the threat of punishment has diminished its occurrence. We now smack our children very rarely; it just isn't necessary. *(Ah—they have learned. I think your teaching is working pretty well. At our house, we were able to get on the same learning curve. /rap)* I think the real problem here is that the "thought police" are out and about in force. *(Check. I have not run into them, but I have ducked that for years. The "politically correct" movers are swarming in some such areas. /rap)*

I know many people who don't smack their kids who have brought up fine children. I equally know families who have struggled. I think that what works is best. And, within reasonable bounds, people should be left to bring kids up without the worry that the local social services will remove them. After all, bringing up children is probably the most difficult job going. *(Check. /rap)* There are very few role models. Most of us only get two to view close up. *(But there are others we can learn from, while we watch from some distance. /rap)*

Keep up the good work. I am strictly a 0's and 1's man, but I always read your articles. Some of it loses me, some of it sinks in. I hope you're never too old to learn.

ALUN HUNT
via e-mail

Well, Alun, some people have learned the concept of NEVER hitting a child. Others of us have not agreed on that. I don't think either side is wrong, and neither side has an easy task. My main tack would apply when a small child tries to reach for a hot item, such as a stove or soldering iron. I would reach out my big PAW and SWAT her hand away from the hot object to interdict the harm. Then, I would immediately try to EXPLAIN why the hot item would be very painful. Every kid has to learn how to recognize hot objects. I have been fairly successful at explaining to my kids why they should not do something. I want them to learn to trust me when I say, "STOP!—DON'T do that, and I'll give you five reasons not to." Then I would have to explain five good reasons why they should not march out into traffic (because a car is coming) or some more obscure danger. We adults are not perfect, but we have to teach our kids to trust us when we warn them, "NO!!" Fair enough? But, as a matter of semantics—or of degree—I have always been willing to give my child a calibrated SWAT, but not a SMACK. We certainly agree that we should not beat kids —or wives—or anybody else.—RAP

Dear Bob:

I always enjoy reading your column. Regarding Bob Becker's letter and your comments (*ELECTRONIC DESIGN*, July 20, p. 113), I would like to draw your attention to a simple truth found in the 24th verse of the 13th chapter of the book of Proverbs:

"He that spareth his rod hateth his son: but he that loveth him chasteneth him betimes."

For those who would question the ultimate author of these words, consider, at least, the reputation of their human author concerning wisdom. Regarding conventional "wisdom," note the 22nd verse of the first chapter of the book of Romans:

"Professing themselves to be wise, they become fools."

The full chapter provides the proper context for this statement.

JEFF MUMMA P.E.
via e-mail

Jeff, we tend to agree that sometimes children need an education. As I said at the end of the previous letter, maybe a swat betimes. But, I don't ever recall taking a rod or switch to my kids. Just a swat.—RAP

Dear Bob:

I'm not sure what you mean by "linking up your GPS receiver," or even why you'd want to. But, a friend of mine showed me his GPS, playing through a laptop that was running a portion of the "Precision Mapping" program. The result was very nice—a large, moving map display of the area being intercepted by the GPS receiver. As we drove, you could shift your eyes from the laptop screen to the street signs as they went past—in total agreement!

BOB SWINNEY
via e-mail

Hello, Bob. I am not trying to get perfect linkage of my ACTUAL position and my GPS position to read out. I just want to be able to turn the GPS off when I turn the key off—without sucking down the battery. Yes, YOU, the passenger, could see the laptop display and the street signs. But, was there a way the DRIVER could do this, without getting into accidents?—RAP

Dear Bob:

As I read your article on touch typing, I gave pause to reflect on why I took typing in high school some 33-odd years ago. And, I remembered that I was one of two males in a class of 24 females. I never got much above 30 wpm. The funny thing is I can't remember any of the girls, but I never forgot how to touch type.

DAN VANDAME
via e-mail

PEASE PORRIDGE

BOB PEASE

I'm typing up around 30 wpm, and I can't gripe. I learned at home from my mother and a couple of simple books. I never forgot the girls in school, though!—RAP

Dear Bob:

After reading your "What's All This Circuits-In-Your-Car Stuff" column in the Aug. 3 issue, I was reminded of the time that I "improved" upon the "blinker audibility" in my 1984 Cadillac Cimarron. It was very hard to hear the blinker's thermally activated contact reed. So, I decided to use a salvaged Mallory Sonalert sounder, fed by a couple of isolation diodes (one for the right, one for the left blinker circuit). This would better alert the driver when the turn-signal blinker was "on."

It worked fine, and the audibility was great from the driver's perspective. What I hadn't thought of, however, was how it would affect my wife when she was riding along with me as a passenger! Women, in general, seem to be more sensitive to high-frequency sounds than men. And, as just a passenger, the Sonalert's frequency drove her crazy (even at a deliberately reduced volume level).

So, the bottom line would perhaps be: Before finalizing any sort of audible alert in your car, it might be prudent to fly it past "she who must be obeyed" first. Try to pick a sound that won't be terribly annoying to others in the car who are "captive" to our creative genius!

DAVE MILLER
via e-mail

Maybe an adjustment pot in series with that Sonalert will let you control its volume. Or, tape some foam over it! And, beam it toward the DRIVER!! They are fairly directional, right?—RAP

All for now. / Comments invited!
RAP / Robert A. Pease / Engineer
rap@web team.nsc.com—or:

Mail Stop D2597A
National Semiconductor
P.O. Box 58090
Santa Clara, CA 95052-8090

Note: RAP will be trekking in Nepal all of October. Don't expect much response to your mail or e-mail until November 10.

Op-Amp Audio

Realizing High Performance: Buffers (Part II)

Taking up where last month's column left off, here's the second part of our discussion on output-buffer techniques as part of audio op-amp applications.

A flexible Class A buffer: To fulfill the function of the discrete version of a unity-gain buffer, consider the schematic in the figure. A number of features lend this circuit utility, and can either be built as-is or modified for specific needs. Functionally speaking, this buffer's intended to drop directly into the U2 stage of last month's general diagram.

The hookup's basic function is that of a complementary buffer, with a nominal input/output dc offset near (but not exactly at) zero. Actually, this is quite a common circuit type. It's often realized with a complementary output transistor pair, biased in turn by a pair of forward-conducting diodes driven at their midpoint by the input op amp. I used such a circuit years ago in my op amp book.[1]

Here, replacing the two diodes with complementary transistors still has the same basic advantage of near-zero input/output offset. But, it lowers input bias current substantially, due to the transistor gain. It can also reduce distortion due to better load isolation.

The cancellation of the forward V_{BE}s of Q1-Q3 and Q2-Q4 is somewhat imperfect, however, as these are different device pairs. Output transistors Q3 and Q4 are 1-A types, for best gain linearity at 100 mA or more current peaks. Driver-stage devices Q1-Q2 are general-purpose types, suitable for currents of up to 100 mA and more (much higher than used here). A version of this general complementary topology was used in the classic LH0002 buffer, where the Q1-Q2 emitter currents were set simply by resistors to the supplies. A discrete version, the "0002," was also offered.[2]

In this case, the respective Q1-Q2 emitter currents are set up by current sources, Q5 and Q6. Their output current levels, along with the use of emitter-stabilization resistors R3-R4, work to indirectly set up the output-stage quiescent current. With about 4.5 mA of current flowing in R3, Q1 is biased stably. With the V_{BE}s of Q1-Q3 nominally equal, it can be seen that R3 and R6 will drop comparable voltages. This means that Q3 will conduct about twice the current in Q1, for the 2:1 ratio values. Thus currents set by Q5 and Q6, along with the relative resistance ratios, determine the output quiescent current.

Here, the V_{BE}s aren't exactly equal between complements Q1-Q2, or for Q1-Q3, and the idle current in Q3 is more than 10 mA (about 13 mA). Similar reasoning applies to Q2-Q4. Either more or less output-stage current through Q3-Q4 can easily be affected, simply by adjusting the relative values of R3/R6 and R4/R7 together. This is best done via the choice of R3-R4 value, leaving R6-R7 fixed.

At 13 mA of current in Q3-Q4, they operate rather rich in Class A mode—at least until heavier loads should appear. For this bias level, departure from Class A will occur somewhere around 1.5 V, for a 150 Ω load.

The Q3-Q4 dissipation is about 200 mW each on ±15-V supplies, which will be OK for plastic-packaged devices like the original TO-237 devices, or the Zetex "E-line" version. Either of these packages should be used with ample pc-board copper area on the collector leads to aid in heat transfer. All circuit parts are available from international suppliers, such as Digi-Key.[3]

If much higher sustained currents are needed, even lower-thermal-resistance device packages can be used with Q3-Q4, such as the MJE171/181 or D44/D45 families. And, a lower-output-current version can be implemented by using PN2222A and PN2907A types for Q3-Q4.

Protection of this circuit is provided by several means. Without D3 and D4, the upper current limit for Q3-Q4 is set either by the limited-drive current (5 mA) times the gain (50 to 250), or by the R6-R8 values and the supplies. This current can easily reach several hundred mA, so active current limiting is very useful. The optional Red LEDs D3 (D4) provide this, clamping the drive to Q3 (Q4) when the emitter current reaches about 1.2/R6, or ~240 mA as shown. For lower levels, the LEDs don't conduct and signals pass normally. The LEDs are Panasonic types as noted.

When used within an overall feedback loop with an op-amp driver feeding R1, this buffer might need protection from overvoltage. The optional diode clamps D5-D6 provide this function. They clamp the drive to Q1-Q2 when and if the R8 output is shorted—so large reverse voltages aren't seen in the circuit. With normal signals, there's just a few mV across the diodes and they don't conduct.

Performance: Ideally, a buffer such as this is transparent to signals with differing loads and with diverse levels.

WALT JUNG

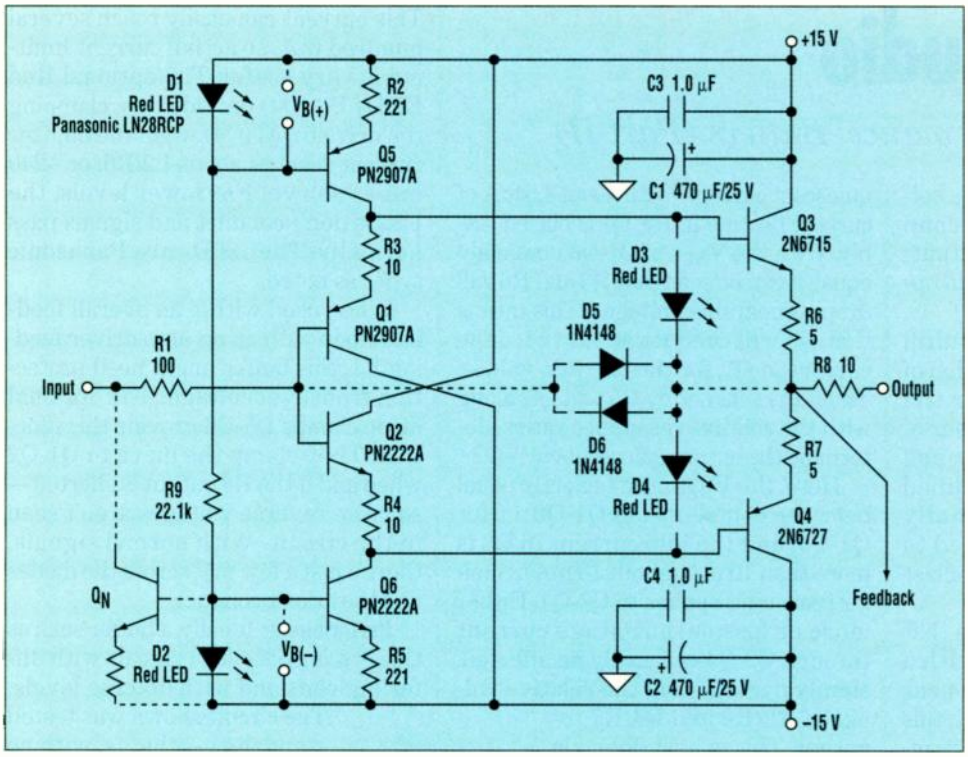
The circuit shown was tested standalone—that is, with no driving op amp. Tested for THD+N with both low- (150 Ω) and high-impedance (100 kΩ) loads, it holds up well over levels from 0.5 to 8 V rms. At the highest levels of 8 V into a low impedance, THD+N reaches a high of 0.15%. But, it quickly drops to 0.02% at 2V, and is appreciably less than .01% at 0.5 to 1 V, or within the Class A range.

For high-impedance loading, distortion for all levels is well below 0.01%, typically 0.002% for 1 V. And, for either load impedance, THD+N is also relatively independent of frequency (below 100 kHz). Harmonics within the distortion residual at the output are predominantly third at 1- to 2-V levels.

The circuit's output impedance is essentially resistive and about 15 Ω, most of which is the R8 value. Voltage offset of the buffer will be high, in the 20- to 30-mV range, due to the inexact V_{BE} cancellations. When used within an overall feedback loop, as illustrated last month, this offset isn't consequential. It's suppressed by the feedback loop.

Housekeeping details: Some parts of the schematic aren't directly involved with the buffer function, but nevertheless still have utility. An example is the optional npn current-source transistor, Q_N. This can be used to set up a fixed-

WALT JUNG



current drain directly from the driving op amp's output stage, thus operating it in a richer-than-normal Class A current range and minimizing any internal Class AB effects for alternating output-signal polarities. By using the high dynamic impedance of a transistor for this function, a fixed steady current can be taken from the op amp without loading it dynamically (and possibly increasing distortion). Q_N's LED bias scheme of $V_{B(-)}$ will cause a current of 1.2 V divided by the emitter resistance to flow in the collector. For example, 1 kΩ would source 1.2 mA. For opposite polarity (*current sink*) loading, a pnp current source "Q_P" is biased by D1, with a similar emitter resistance. If used, Q_N or Q_P are PN2222A or PN2907A types.

As noted, this buffer circuit functionally drops into the hookup of last month—that is, between the op amp and the load. The feedback path is taken *before* isolation resistor R8, providing simple, effective load isolation for the buffered op amp.

When driving low-impedance loads, decoupling of the high-load currents is accomplished with large, local electrolytic bypasses C1-C2, with their shared point returned to the load common. Because of the wide transistor bandwidths used, layout and wiring can also be critical. C1-C2 should be augmented by local, low-inductance high-frequency bypasses, such as 1-µF/50-V stacked-film types C3-C4, located physically near Q3-Q4.

It's worth noting that long lines, which appear as a capacitive load, are low-impedance loads. Even if terminated at the far end in a moderate resistance value (~10 kΩ)—for high frequencies, the effective load such lines present to the amplifier is still low (X_C for 10 nF looks like 800 Ω at 20 kHz). R8 is a load isolator, and can be increased if necessary.

Further suggestions: It should be obvious that this circuit is readily adaptable for various needs. If used on other supply voltages, the current in LEDs D1-D2 would benefit by being stabilized, perhaps by something as simple as a 1-mA JFET current diode in place of R9.

The output transistors (and their operating point) are best chosen to maintain the lowest distortion for the particular loads and operating level. Remember: The distortion figures quoted are for the buffer alone. A well-chosen driver can lower it even further.

TIP: These first two installments on high-performance audio with ICs and discretes have focused on choosing (or designing) a buffer stage for best overall performance. In IC op amps with poor thermal design, heavy output loading can cause shifts in effective input offset, as well as associated linearity changes. These load-dependent shifts can be identified with testing, allowing easier device selection to minimize this problem.

However, simply buffering the amplifier's output with an isolated-package circuit removes this source of error, and maximizes op-amp linearity. This step is recommended wherever it's practical and needed. Buffer circuits can be chosen from a number of ICs expressly designed for such tasks, as was noted last month. Or, they can be designed to match a given set of conditions, as in this example.

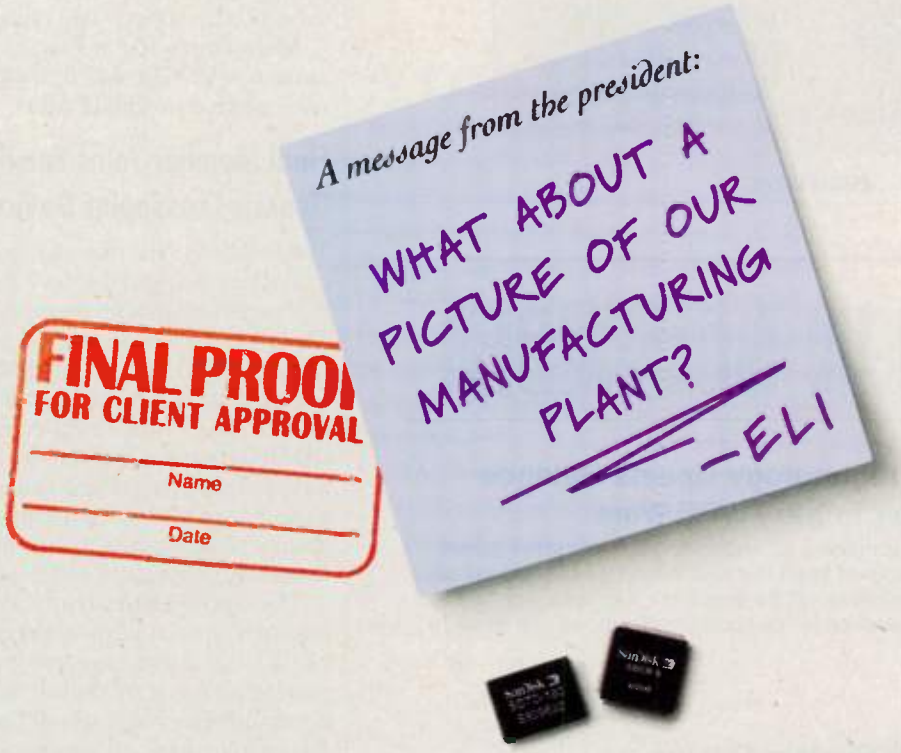
The ability to adapt and hone a circuit's operational characteristics precisely to an application is a major hallmark of discrete circuitry, as this example shows. In contrast, adaptability to different drive and bias levels isn't something IC buffers can do, at least not in the manner here. One needs to choose either the flexibility and diversity of the discrete approach (at the expense of component count), or the small size and component efficiency of the IC approach (at some expense of bias and drive flexibility). In any event, enjoy those low distortion, Class A sounds!

Acknowledgments: In preparing the last two columns, I appreciated helpful comments from audiophile friend and design consultant John Curl.

References:
1. Jung, Walter G., "Output Buffering," Fig. 7-32, Ch. 7, *IC Op-Amp Cookbook*, Third Edition, Prentice Hall, 1986.
2. Jung, Walt, and Childress, Hampton, 'Output Ills' and 'High Speed Buffers,' sections in "POOGE-4: Philips/Magnavox CD Player Mods, Part 2," *The Audio Amateur*, issue 2/1988.
3. Digi-Key Corp., 701 Brooks Ave. South, Thief River Falls, MN 56701-0677; (800) 344-4539; *www.digikey.com*.

Walt Jung is a corporate staff applications engineer for Analog Devices, Norwood, Mass. A long-time contributor to ELECTRONIC DESIGN, *he can be reached via e-mail at: Wjung @usa.net.*

SanDisk makes the highest density Flash ChipSets you can buy.



You want high density Flash ChipSets, we've got high density Flash ChipSets. In fact, we make the highest density Flash ChipSets (up to 160 Mbits) available, and support all our high density Flash ChipSets with one small footprint. And only SanDisk high density Flash ChipSets give you built-in ECC for reliability, together with a standard IDE interface and the best combination of performance, power and price. All of which has helped make SanDisk the leader in flash data storage. For more information about our great high density Flash ChipSets, go to www.sandiskchipsets.com or call 949-595-2197.

SanDisk
More Memory. More Possibilities.

Attention other ad agencies: This company will soon be looking for a new shop. YOU DON'T WANT THEM. They care more about making great Flash Memory than making great ads.

READER SERVICE 126

DIGITAL ICs

Low-Power CPLD Offers In-System Programmability

A novel 3.3-V CPLD provides 128 macrocells and pin-to-pin speeds as fast as 5 ns. The EPM7128A is the first 3.3-V member of the company's high-performance, high-density Max 7000A family. It features Altera's MultiVolt interface that allows I/O support for 5.0-, 3.3-, and 2.5-V logic interface levels. In addition, in-system programmability is made possible with the Jam programming and test language. All Max 7000A devices are supported by Altera's Max+Plus II development system. The EPM7128A is available now in a 100-pin TQFP package, and will soon be available in 84-pin PLCC, 144-pin TQFP, and Altera FineLine BGA packages. By the end of this year, pricing for the EPM7128A is expected to be $7.00 in 100,000-unit quantities.

***Altera Corp.**, 101 Innovation Dr., San Jose, CA 95134; (408) 544-7000; www.altera.com.* **CIRCLE 500**

Final Member Joins Family Of Generic Crosspoint Devices

The third and final member was added to Lattice Semiconductor's family of ISP generic digital crosspoint devices. The company released the high-performance ispGDX80-A for production, completing the 5-V family that also includes the ispGDX120A and isp GDX160 parts. All three devices are targeted at signal routing and interface logic design with such features as in-system programmability and high performance, integration, and flexibility.

The ispGDX80A architecture consists of 80 special-purpose programmable I/O cells interconnected by a global routing pool that minimizes signal delays and delivers high speed. The device features any-input-to-any-output signal delays of 5 ns, clock-to-output delays of 5 ns, and operating frequencies of 111 MHz. Other features include boundary-scan test logic. The ispGDX80A-5 (5-ns speed grade) is priced at $11.65 and the ispGDX80A-7 (7-ns speed grade) is priced at $8.20 in 100-pin TQFP packaging (1000-piece quantities). Both parts are available immediately.

***Lattice Semiconductor Corp.**, 5555 NE Moore Ct., Hillsboro, OR 97124-6421; (503) 681-0118; Internet: www.latticesemi.com.* **CIRCLE 501**

Tool Vendor Information Now Available Online

The latest addition to the EE Design Center is the EDA Index. It's a web site intended to help engineers research, select, and purchase ICs for product and systems design. The Index, specifically targeted at engineers working on first simulation and validation as well as design and resimulation, serves as an online catalog of design-automation tools available to engineers worldwide. Currently, the Index features over 30 manufacturers, and that's expected to grow rapidly in coming months.

The information found at the site will provide engineers with the compare and contrast information they need, in areas such as programmable-logic and system-design tools, to make smarter design decisions. In particular, the site includes such information as classes of design automation products ranging from specific, niche tools to mainstream global solutions and associated tool details. Access to the EE Design Center and its EDA Index is now available 24 hours-a-day, seven days a week. It's free of charge to users. CA

***QuestLink Technology Inc.**, 100 Congress Avenue, Suite 400, Austin, TX 78701; (512) 322-3220; Internet: www.questlink.com.* **CIRCLE 502**

Computer Power Gives Automated Test Tool A Boost

A simulation-based test synthesis product called Test Designer version 8.5 offers access to a store of computer power known as the "SpiceFarm" via the Internet. The main function of the tool is to automate test program development for analog and mixed-signal systems, circuits, and ICs. Because today's complex design often require a large number of simulations, this newest feature promises to drastically cut down on simulation time. It achieves this by allowing the simulation in parallel. Interface to the SpiceFarm is virtually seamless for the user and can be set up for intranet or Internet usage. The data exchanged between the SpiceFarm and Test Designer is encrypted and compressed to ensure security and data integrity.

Another new feature of the tool is its web-based help capability, which is available directly from within the schematic capture tool. By simply selecting a new help menu item in the tool, users gain access to technical support and the Intusoft home page. Because the help menu is expandable, users can add their own web links to the menu.

Test Designer 8.5 is a complete system and includes a schematic entry tool, model libraries with over 13,000 part models (most of which include predefined failure modes), a SPICE3-based analog and mixed signal simulator, a graphical data host processor, and an array of features to handle the test data analysis and reporting. The tool is available now and is compatible with both Windows 95 and NT platforms. It sells for $12,000. Product maintenance is 15% of the purchase price. CA

***Intusoft**, 222 W. 6th St., Suite 1070, San Pedro, CA 90731; (310) 833-0710; www.intusoft.com.* **CIRCLE 503**

PCI DAQ Board Features High Level of Integration

The DT3016 is a high-resolution, multifunction data-acquisition board for the PCI bus. The board features 32 single-ended/16 differential inputs at 250 ksamples/s, two analog outputs at 200 ksamples/s, 16 digital I/O lines, four counter-timers, and a custom-designed PCI-bus interface chip. This chip allows for high-speed, bus mastering data transfers to the PC, enabling the DT3016 to run multiple subsystems simultaneously without losing data. By setting aside a block of memory in the PC, the DT3016 performs bus-master data transfers without CPU intervention, freeing the CPU for other tasks, such as data analysis or display. The DT3016 ships with Windows 3.1/95/NT and DT-Open Layers compliant drivers. List price of the board is $1495. JD

***Data Translation Inc.**, 100 Locke Dr., Marlboro, MA 01752-1192; (800) 525-8528; (508) 481-3700; fax (508) 481-8620; e-mail: info@datx.com; www.datatranslation.com.* **CIRCLE 504**

Ethernet DAQ System Offers 16-Bit Resolution

The EDAS-1031E high-accuracy multifunction system offers 16-bit (1 part in 65,536) sampling of remote signals that require wide dynamic range measurement. Typical applications for the system include monitoring of temperature sensors, flowmeters, load cells, LVDTs, spectroscopes, and gas chromatographs. The system communicates over any Ethernet LAN or the Internet, allowing real-time data to be shared with any number of PCs and workstations located virtually anywhere. The EDAS-1031E provides 16 single-ended/8 differential analog inputs at 16-bit resolution, two 12-bit analog outputs, and 16 digital I/O channels. The 16-bit ADC samples waveforms at up to 100 kHz. Digital I/O channels are programmable as inputs or outputs. The EDAS-1031E systems will begin shipping in October 1998 at a price of $1295. JD

***Intelligent Instrumentation Inc.**, 6550 S. Bay Colony Dr., MS130, Tucson, AZ 85706; (800) 685-9911; (520) 573-0887; fax (520) 573-0522; e-mail: sales@instrument.com; Internet: www.instrument.com* **CIRCLE 505**

Programmable DC Power Supplies Have Modular Design

The DHP series of programmable dc power supplies provide a wide range of power levels delivered from a thin (2U to 6U) rack-mount profile. The high-power supplies deliver dc outputs from 2 to 30 kW. The total power is achieved by paralleling up to six individual power modules per rack-mount chassis. The output current is shared equally among the internal power modules. For ease of use, the DHP series supplies are programmable from a front panel keypad or remotely through user-selectable standard 5- or 10-V analog inputs. All programmable voltage, current, and auto sequence settings can be stored and recalled. Also, the ac input voltage, ambient air inlet temperature, dc output voltage, current, and power can be displayed from the front panel at any time. Pricing starts at $1995. JD

***Sorensen, Division of Elgar**, 9250 Brown Deer Rd., San Diego, CA 92121; (800) 525-2024; (619) 450-0085; fax (619) 458-0237; e-mail: sales@elgar.com.* **CIRCLE 506**

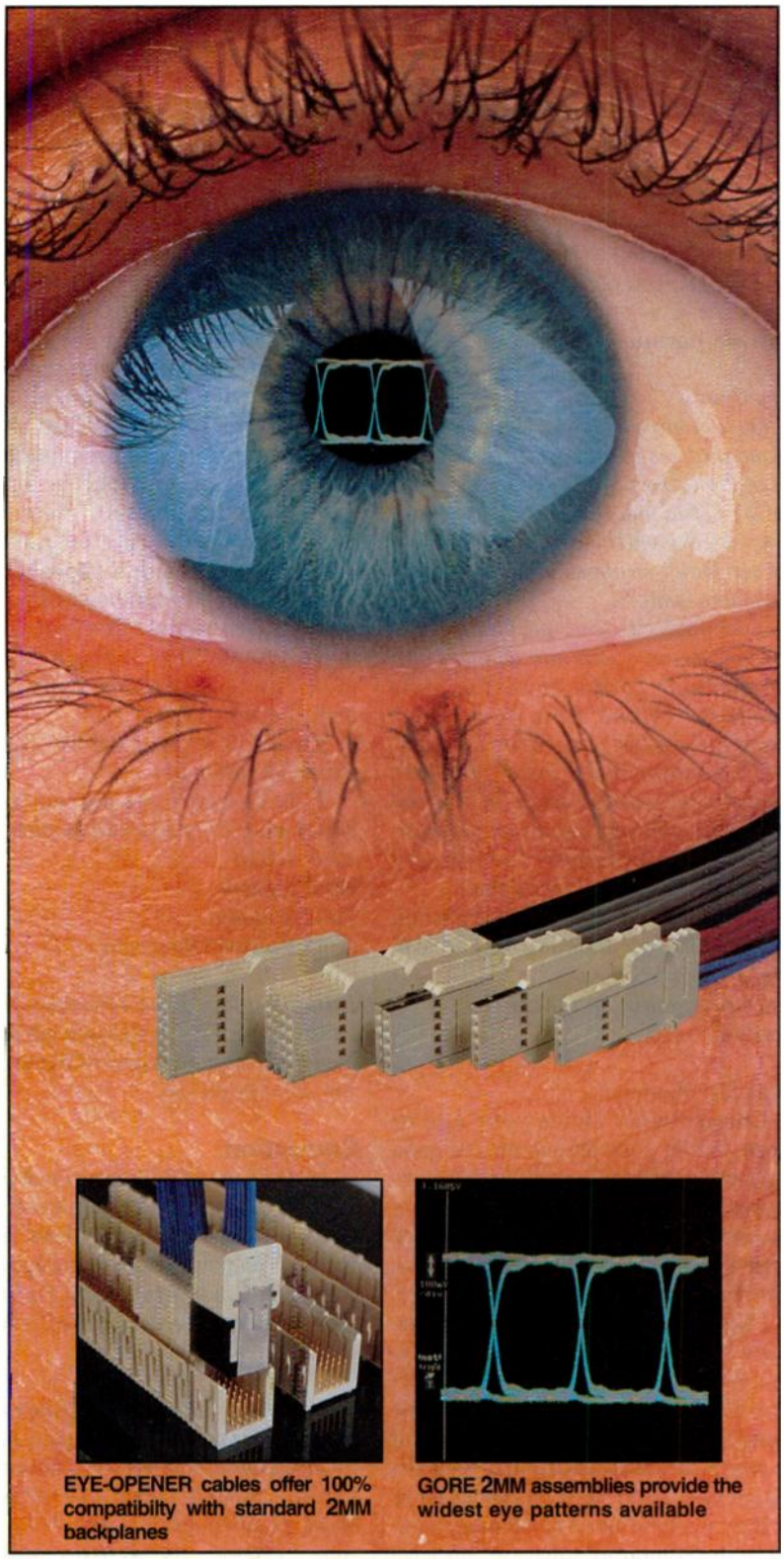
Universal Instrument Measures Voltage and Power

The 5230 series of universal RF power/volt meters are instruments capable of making both power and voltage measurements. Designed for EMC and board testing environments, the 5230 series measures RF voltage from 10 Hz to 2.5 GHz and covers 10 kHz to 100 GHz when measuring power. If operating as a power meter, the 5230 series can make more than 200 measurements per second. It measures power levels from –70 dBm to +44 dBm within a 90-dB dynamic range. The Model 5232, a dual-channel meter, allows input and output measurements to be made and viewed simultaneously. For voltage measurements, the 5230 series has a voltage range of 200 mV to 10 V with true RMS response below 30 mV. It also features a zero correction function that stores the zero offsets of each range. The single-channel Model 5231 is priced at $3450, while the Model 5232 goes for $4450. JD

***Boonton Electronics Corp.**, 25 Eastmans Rd., Parsippany, NJ 07054-0465; (973) 386-9696; fax (973) 386-9191; www.boonton.com* **CIRCLE 507**

Gore's New 2MM Cables -

An Eyeful of Fidelity and Reliability



EYE-OPENER cables offer 100% compatibilty with standard 2MM backplanes

GORE 2MM assemblies provide the widest eye patterns available

1.2 Gbits/sec Intercabinet Links for 2MM Backplanes

Gore's new EYE-OPENER Family of 2MM assemblies provides unmatched performance and reliability in a package that is 100% compatible with all standard 2MM backplane connector systems.

The only source for all 2MM needs
Now Framatome's Millipacs™ 1 and 2, Metral™, Z-Pack™ HM, HDM and all the others can be optimally cabled with EYE-OPENER cable assemblies.

EYE- OPENER assemblies were designed using Eye Pattern Analysis techniques to achieve maximum synergism between cable and connector. GORE-TEX®expanded PTFE dielectric coax and twinax cables help EYE-OPENER assemblies to maintain signal integrity, even on today's fastest digital drivers and receivers. They can provide bandwidth densities greater than 2 Gbits/sec. per mm.

Designed for reliability
Premium connector materials such as Beryllium Copper contacts and Liquid Crystal Polymer housings provide abuse protection without affecting performance. A unique ruggedized version prevents plugging and unplugging damage to the small pins found in 2MM backplane connectors. EYE-OPENER cables are perfect for Telecom, Test Equipment and other high data rate applications.

Gore's EYE-OPENER family is fully scalable in size, performance and configuration and comes in differential and single ended versions. *If you want your eyes opened call:*

1-800-445-4673

(In Europe call +49-9144-601-389)

GORE
Creative Technologies Worldwide

Chip-to-Chip Signal Integrity

READER SERVICE 106

Beaming Down Memory Lane

Patrick,

Amazing! Another *2000 A.D.* fan *(ELECTRONIC DESIGN, July 20, 1998, p. 20)*. Wow! That was 20 years ago! I still have the Christmas edition you mentioned, on my bookshelf next to *Troubleshooting Analog Circuits*. The pages are a bit yellow now, but still look great.

Regards,
Peter Dutton
London, England
PETERDUT@aol.com

Patrick Mannion responds:

Hey there!

Do you have any idea what I'd give to see that issue again? Talk about a blast from the past!! I've printed out the .JPG file you sent along, and have it up on the wall in my office as we speak. Don't suppose you can e-mail the whole issue?

Now you've teased me, so I have to go hunt down a web site where I can beg, hustle, or borrow that issue. Mine was lost (we had a big house with many kids) a few years after I got it.

It's a shame that I lost it, as that's what stirred my interest in Sci-Fi, and probably what got me through engineering school to where I am now (if you want to extrapolate on that).

It must have had the same effect on you, considering that you still have it. Did it? Let me know.

Thanks again for the .JPG.
Patrick.

Dear Mr. Mannion:

I'm probably twice your age or more. While your article makes good copy, there are millions of us out here in good old keyboard land who have learned, and are comfortable with their typing skills. These skills have transferred well to the computer age.

I think that the argument could be made that without the standard keyboards as an input device, Eckert-Mauchly, IBM, and DEC would still be using punched cards. The millions of us who were brought up on typewriters moved easily to word processors as they evolved from electromechanical to the computer software miracles they are today.

I am not opposed to innovation, but I am opposed to destructive innovation where everyone marches to a different drummer. Without one standard that has held throughout this amazing revolution, the evolution might have stopped in its tracks long ago.

Yours truly,
George Garwood
Wynnewood, PA.

Hello Patrick:

I read your opinion in *ELECTRONIC DESIGN*, July 20, 1998, and completely agree with you. I have been using computers since the punch-card days though, and I will tell you that programming in the latest version of Visual Basic is a far cry from writing AppleBasic, even 12 years ago.

As designers, we must listen to the sages of our time, and we must also listen to those around us. These sages will give us the fun jobs of creating the next transportation system, or future tools for learning, but those who we live with will give us the ideas to solve today's problems. Computers are merely tools to get things done, no more, no less. May we continue to make better tools!

Also, where can I get the *Bioelectronic Handbook*?

Thanks again for a great piece. What else do you read besides old *2000 A.D.s*?

Kind regards,
Tim Economu
economu@whidbey.com

Editor's note: "Bioelectronics Handbook: MOSFETS, Biosensors, and Neurons" can be found at www.Amazon.com for $89.50.

Correction

In the August 3, 1998 issue of *ELECTRONIC DESIGN*, "Multiphase Controller Meets Pentium's Power Demands," on page 28, incorrectly stated Semtech Corp.'s telephone number. The correct phone number is: (805) 498-2111.

Letters to the Editor, including the writer's name, address, and phone number, should be sent to: Letters Editor, ELECTRONIC DESIGN, 611 Route 46 West, Hasbrouck Heights, NJ 07604; fax (201) 393-0204; e-mail: dschiff@penton.com. Letters may be edited for space and clarity. Names will be withheld upon request.

Convert your FPGA to a 66 MHz PCI-compliant ASIC

Catch a Cutthroat™ Gate Array

Representative Conversions

Altera Device	Equivalent AMI Gate Array	AMI Pricing 50K Units
EPM7128ALC84-7	AMI5G15S	$2.50
EPF6016ATC144-1	AMI5G33S	$4.25
EPF10K50VRC240-1	AMI5G109S	$8.50
Xilinx Device		
XCS10XL-4PC84C	AMI5G15S	$2.50
XC95144-7TQ100C	AMI5G15S	$3.10
XC4013XLT-09PQ208C	AMI5G74S	$6.00

For more comprehensive device compatibility data, please visit our web site.

AMI's Cutthroat™ family of PCI-compliant gate arrays is uniquely adapted for the most demanding environment – the elusive 66 MHz spec.

Fast, agile and far less expensive than FPGAs, AMI's Cutthroat gate arrays are now in season. Running at 66 MHz and featuring 6ns clock-to-out (Tpco), AMI's Cutthroat ASICs are a trophy catch for designers who can't achieve high-speed PCI compliance in FPGAs. Drawing on its proven ASIC expertise, and over 12 years of conversion experience, AMI developed the Cutthroat family of gate arrays specifically for FPGA conversions. And now you can reel in the benefits. Contact AMI today. We'll help you hook a Cutthroat.

(800) 639-7264 dept.9183 • www.amis.com/9183

READER SERVICE 99

AMI
AMERICAN MICROSYSTEMS, INC.

CMP

EDTN network

ELECTRONICS DESIGN, TECHNOLOGY & NEWS NETWORK

SPONSORS

Altera

American IC Exchange

Cherry Semiconductor

Digi-Key Corporation

Hamilton Hallmark

Harris Semiconductor

Hitachi Semiconductor America

Marshall Industries

Mathworks

OrCAD

PMC Sierra

Sharp Microelectronics

Siemens Microelectronics

Summit Design

Sun Microsystems

Tektronix Inc.

Toshiba America

VIEWlogic Systems Inc.

Wind River Systems

Xilinx

If you think the EDTN network looks IMPRESSIVE on paper,

NETWORK MEMBERS

EE TIMES

ELECTRONIC BUYERS NEWS

semiconductor BUSINESS NEWS

Aspect Development, Inc.

ELECTRONIC DESIGN

you should see it ONLINE

Experience the site today and judge for yourself!

www.edtn.com

EDTN network

ELECTRONICS DESIGN, TECHNOLOGY & NEWS NETWORK

Audio Solutions

We'll help you put the pieces together.

Audio testing requires specialized solutions.
Audio Precision offers three lines of audio analyzers.

ATS-1
- ❖ Analog audio test system - 2 channel
- ❖ Advanced LCD front panel display and controls
- ❖ Smart GPIB interface w/HP 8903B compatible mode
- ❖ High performance, cost effective: Residual Noise 1.5μV, 22Hz-22kHz System THD+N ≤0.0025%+3μV

System One
- ❖ The Recognized Standard for analog & digital audio
- ❖ versatile and fast
- ❖ PC or GPIB interface
  - APWIN for Windows 95™
  - GPIB drivers for National Instruments LabView/LabWindows
- ❖ High speed FASTTRIG synchronous multitone testing on DSP versions
- ❖ Dual Domain™ version includes digital I/O
- ❖ Total analog system THD+N residual ≤0.001%+1.5μV, 22Hz-22kHz

System Two
- ❖ A new standard for today's digital and analog systems
- ❖ Analog and digital audio testing
- ❖ Digital interface testing and measurement
- ❖ PC/Multimedia audio testing
- ❖ Reduced bit-rate codec testing for audio & telecom
- ❖ Digital converter testing
- ❖ Analog residual THD+N ≤0.0004% (≤-108dB)
- ❖ Digital analyzer noise ≤-140dBFS, wideband

Thousands of customers worldwide choose Audio Precision analyzers because we offer a complete family of audio testing solutions.

Our worldwide force of Audio Precision representatives will be pleased to provide further information and help you find solutions for your audio testing.

Audio precision

P.O. Box 2209
Beaverton, OR 97075-3070
(503) 627-0832, 1-800-231-7350
FAX: (503) 641-8906

READER SERVICE 100

INTERNATIONAL DISTRIBUTORS: ***Australia:*** IRT Electronics Pty. Ltd., Tel: 2 439 3744 ***Austria:*** ELSINCO GmbH, Tel: (1) 815 04 00 ***Belgium:*** Trans European Music NV, Tel: 2 466 5010 ***Brazil:*** INTERWAVE LTDA., Tel: (21) 325-5351 ***Bulgaria:*** ELSINCO Rep. Office Sofia, Tel: (2) 956 12 45 ***Canada:*** GERRAUDIO Distribution, Tel: (416) 595-2779 ***China, Hong Kong:*** A C E (Int'l) Co. Ltd., Tel: 2824-0387 ***Croatia:*** ELSINCO Rep. Office Zagreb, Tel: 1 611 09 14 ***Czech Republic:*** ELSINCO Praha spol. s r.o., Tel: (2) 48 66 89 ***Denmark:*** npn Elektronik aps, Tel: 86 57 15 11 ***Finland:*** Genelec OY, Tel: 17 813 311 ***France:*** ETS Mesurout, Tel: (1) 45 83 66 41 ***Germany:*** RTW GmbH & Co. KG, Tel: 221 70913-0 ***Greece:*** KEM Electronics Ltd., Tel: 1 67 48514/5 ***Hungary:*** ELSINCO Budapest KFT, Tel: (1) 269 18 50 ***India:*** Electro Dynamics, Tel: 512 364713 ***Israel:*** Dan-El Technologies Ltd., Tel: 3-647 8770 ***Italy:*** Audio Link s.n.c., Tel: 521 648723 ***Japan:*** TOYO Corporation, Tel: 3 [5688] 6800 ***Korea:*** B&P International Co., Ltd., Tel: 2 546-1457, B&P (Kumi Office), Tel: 546 53-7347/8 ***Malaysia:*** Test Measurement & Engineering Sdn (Selangor), Tel: 3 734 1017, Test Measurement & Engineering Sdn (Penang), Tel: 4 8422088 ***Netherlands:*** Heynen B.V., Tel: 485 498 111 ***New Zealand:*** Audio & Video Wholesalers, Tel: 7 847-3414 ***Norway:*** Lydconsult, Tel: 69-179050 ***Poland:*** ELSINCO Polska sp. z o.o., Tel: (22) 39 69 70 ***Portugal:*** Acutron Electroacustica LDA, Tel: 1 9414067 / 9420862 ***Singapore:*** TME Systems Pte Ltd., Tel: 747-7234 ***Slovakia:*** ELSINCO Slovensko s.r.o., Tel: (7) 794 165 ***South Africa:*** SOUNDFUSION MFG., Tel: 11 477-1315 ***Spain:*** Telco Electronics S.A., Tel: 1 531-7100 ***Sweden:*** TTS Tal & Ton Studioteknik AB, Tel: 31 52 51 50 ***Switzerland:*** Dr. W.A.Gunther AG, Tel: 1 910 41 41 ***Taiwan R.O.C.:*** Double Advance Tech., Tel: 2-595 0696 ***Thailand:*** Maswaroj Company Ltd., Tel: 2-294-4930 ***United Kingdom:*** Thurby Thandar Instruments, Ltd., Tel: (1480) 412451

ELECTRONIC DESIGN CATALOG/LITERATURE REVIEW

RELIABILITY PREDICTION

Catalog describes the RelCalc for Windows software package, which automates MIL-HDBK-217 or Bellcore on your PC, and allows quick and easy reliability analysis of your electronic products. Phone: 818-991-0057, Fax: 818-991-1281, E-mail: info@t-cubed.com. Visit our web site for a FREE DEMO: www.t-cubed.com.

CIRCLE 248

T-CUBED SYSTEMS

WE BUILD CUSTOM BATTERY PACKS

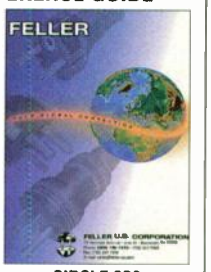
Southwest Electronic Energy Corp. is an innovative value-added distributor of energy management components and custom-designed energy storage devices for your electronic products. We have the resources and expertise to support our customers with in-house engineers & product design teams from the initial stage of product development through manufacturing. 800-231-3612; Fax: 800-240-4535; www.swe.com

CIRCLE 249

SOUTHWEST ELECTRONIC ENERGY

NEW POWE CORD REFERENCE GUIDE

This all new 48-page catalog portrays Feller's complete line of high quality domestic, hospital grade and international power cords. It provides detailed specifications illustrations, application, features and benefits. Many new products and services were added, including in-house cord assemblies, extensive packaging services and custom molding capabilities. 800-736-7333; Fax: 732-247-7279; E-mail: sales@feller-us.com; http://www.feller-at.com

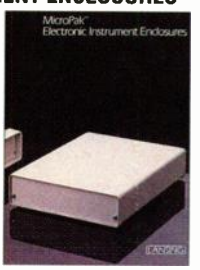


CIRCLE 250

FELLER U.S. CORPORATION

MICROPAK® INSTRUMENT ENCLOSURES

Lansing Instrument Corp. offers enclosures for smaller, free standing electronic instruments used in hand-held or desktop applications. Three body styles and a choice of end cap configurations are available, along with several finishes and colors. Literature includes information for stock and custom choices, and a no-risk offer at a special price. Contact Rich Kippola at Lansing Instrument Corp., (800) 847-3535.



CIRCLE 251

LANSING INSTRUMENT CORP.

Test & Measurement Accessories Catalog

ITT Pomona Electronics' 1998 full line catalog highlights newly designed DMM accessories, a new family of high performance oscilloscope probes, and the first IEC1010 compliant minigrabber ever offered. Phone: (909) 469-2900; Fax: (909) 629-3317; www.ittpomona.com

CIRCLE 252

ITT POMONA ELECTRONICS

GIANT NEW SWITCH CATALOG

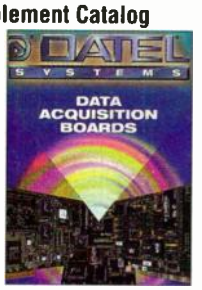
APEM's new 420 page full-line catalog is packed with their switch offerings. New products added: toggles, rockers, pushbuttons, tacts, keys, industrial controls, DIPs, rotary DIPs, micro-limits, pushwheels, slides, keyboards, sealing boots. Many state-of-the-art switch models featuring process compatibility, surface mounting technology & electrostatic discharge withstanding. APEM Tel: 781-246-1007, Fax: 781-245-4531, URL: http://www.APEM.com E-Mail: info@APEM.com

CIRCLE 253

APEM

Data Acquisition Supplement Catalog

FREE! DATEL SYSTEMS' new 48 page, 1998 supplement catalog offers a wide range of high speed, high performance and multi-function Data Acquisition boards. Over 50 new products are offered including advanced performance boards for PCI, ISA and VME bus. For a free copy of the 1988 supplement catalog contact us at: 800-233-2765, fax: 508-339-8784; www.datel.com, e-mail: sales@datel.com



CIRCLE 254

DATEL SYSTEMS

SOFTWARE SHOWCASE 1998

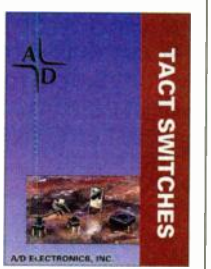
Software Showcase 1998 provides you with information & demonstrations of industry-leading National Instruments application software for measurement & automation applications, such as LabVIEW™ 5.0, LabWindows™ CVI 5.0, Lookout™ 3.8, HiQ™ 4.0, and more. Free multimedia CD offers direct access to product, order information via Internet. (512) 794-0100; (800) 433-3488; Fax: (512) 683-8411; E-mail: info@natinst.com; www.natinst.com

CIRCLE 255

NATIONAL INSTRUMENTS

TACT SWITCHES

A/D electronics' free Tact Switch catalog features a variety of Tact Switches in different configurations. 8 page catalog offers standard and non-standard tact switches. Design engineer can obtain complete specs, dimensional drawings and evaluation samples upon request. A/D Electronics also supplies a variety of interconnects for the OEM. Technical Support is available by contacting: (253) 851-8005; Fax: (253) 858-9869; www.adelectronics.com



CIRCLE 256

A/D ELECTRONICS

Product Selector Features LCD Display

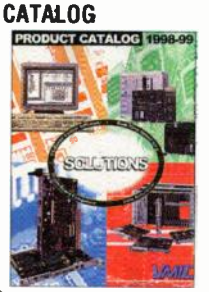
Okaya's Supertwist LCD Module Product Selector includes the latest information on Okaya's Alpha/numeric and Graphic LCD Display Modules. Featured are 32 Character Modules and 16 Graphic Modules. Both series have on-board negative voltage and temperature compensation options. 219-477-4488; Fax: 219-477-4856; E-mail: sales@okaya.com

CIRCLE 257

OKAYA ELECTRIC

NEW VMIC PRODUCT CATALOG

VMIC is a supplier of PC Control Software (IOWorks®), embedded PC single board computers for VMEbus and CompactPCI®, Rtnet™ - real-time networking products (Reflective Memory) for most popular computer systems, PLCs, and bus structure; I/O products for VMEbus, CompactPCI, PCI, USB, and ISA; and industrial systems based upon VME and CompactPCI. 800-322-3616; http://www.vmic.com

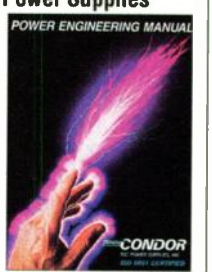


CIRCLE 258

VMIC

Commercial / Medical Power Supplies

Condor's 60-page catalog offers commercial and medical switching and linear D.C. power supplies. Commercial products meet latest international safety standards and medical products are certified to UL544, VDE0750 and IEC601. Call 800-235-5929, FAX (805) 487-8911. www.condorpower.com /~condordc



CIRCLE 259

CONDOR

Handy Surface Mount Resistor Kit™

Kit contains 56 popular values of 10Ω to 1MΩ, 1% tolerance, 1206 size, thick film chip resistors. All resistors are sorted, stuffed in a set of handy enclosures - minimize the time for accessing a particular resistor, takes a small space on work bench. Ideal prototyping, field service. $149 - 100 PC/value, $199 - 200 PC/value, $450 set - 500 PC/value, and $10/refill for 500 PC. (248) 349-7250; fax: (248) 349-8108; www.analog-tech.net

CIRCLE 260

ANALOG TECHNOLOGIES

MILLENIUM 2000

Introducing MIL-2000 the newest state of the art switching power supply. Featuring resonant pulse width modulation topology, up to 85% efficiency. From 1-7.5 kv, @1-10w in 2 sizes 50x60x5mm & 70x60x5mm. Custom designing available. e-mail: ahv@ahv.com; website: www.ahv.com

CIRCLE 261

AMERICAN HIGH VOLTAGE

FREE APPLICATION CD

This appliction CD is designed to help system designers make the most of their available space using Vicor power components. It includes the Vicor Applications Manual, seven product configurator programs, and the complete selection of downloadable Vicor product data sheets. (800) 735-6200; Fax: (978) 475-6715; www.vicr.com

CIRCLE 262

VICOR CORPORATION

ELECTRONIC DESIGN ENGINEERING CAREERS

RATES: $190 PER COLUMN INCH, COMMISSIONABLE TO AGENCIES

MATERIALS

Ad material to: Penton Publishing, Classifieds Dept.
Attn.: GREG MARTHE, 1100 Superior Ave.
Cleveland, OH 44114

SALES STAFF

RECRUITMENT ADVERTISING MANAGER:
GREG MARTHE
(800) 659-1710, (216) 931-9589

CAREER OPPORTUNITIES

OUR TECHNOLOGY IS IN USE EVERY SECOND.

You can help us do better.

Founded in 1973, Symbol is the undisputed world leader in laser bar code technology and designs and manufactures over 250,000 portable computers a year. With annual company sales well over $850 million and expanding product lines, we pride ourselves on our corporate stability, revenue growth and talented 3000+ employees. We are currently seeking motivated professionals for the following positions:

POWER SUPPLY DESIGN ENGINEER

Design and test low power, high efficiency switch mode power supplies. A BS/MSEE and experience with Maxim and LT DC/DC converters is a must. Ideal candidates will have six years' applicable experience in low power design techniques for portable computers, including suspend and instant on functionality. Experience with Li-Ion, NiMH and NiCd battery technologies and chargers is highly desired. Familiarity with PCMCIA card implementations, EMI/ESD issues, speakerphones and PC sound circuits is also desirable for this full-time, on-site, regular position.

RF/EMI ENGINEERS

In this position, you will be responsible for the design and integration of antenna for portable products (planar inverted-F antenna, microstrip/patch, dipole, etc.) A BSEE (MSEE beneficial) and four years' relevant experience are expected. Demonstrated skills with RF and EMI/ESD issues and solutions for portable devices are required. Resume must show RF design experience in portable computer products (WLAN, WWAN, short-range point-to-point transceivers, GPS, etc.) to be considered for this full-time, on-site, regular position.

Symbol provides a very competitive benefits package including a 401(k) plan and on-site fitness and day care facilities. From our headquarters in suburban Suffolk County, on Long Island in New York, you can reach Manhattan or Bridgeport, Conn in an hour, pristine beaches in minutes. Homes and parks are plentiful, neighborhoods friendly, and the schools are nationally ranked.

For immediate consideration, fax your resume with salary requirements and **Dept. Code ELME** to **(516) 738-3814** or e-mail to **jobopps@symbol.com** (Please use the job title above as the subject line of your e-mail.) For more information about our company, visit our Web site at **http:\\www.symbol.com** We are proud to be an equal opportunity employer. m/f/d/v

symbol®

POWER SUPPLY ENGINEER

CSS Power, Inc. is looking for a self-motivated, hands-on, practical individual with 8-10 years of experience in power supply design. Successful candidate must have BSEE and be available for limited travel. Strong positive attitude and the ability to handle pressure situations and tight schedules within small company are a must. Technical requirements include:

- DESIGN EXPERIENCE FOR 5W TO 3.5KW POWER SUPPLIES
- KNOWLEDGEABLE ABOUT DIGITAL AND MICROPROCESSOR CIRCUITS
- UNDERSTAND FEEDBACK LOOPS USING VENABLE ANALYZER
- DESIGN MAGNETICS COMPONENTS FOR POWER SUPPLIES
- PROFICIENT WITH EMI COMPLIANCE REQUIREMENTS
- PROFICIENT WITH UL1950, UL1801, AND BELLCORE STANDARDS FOR POWER SUPPLIES

Excellent salary and benefits package available.
Please e-mail resume to:

sales@csspower.com

or mail to:

CSS Power Inc., Attn: Keith Barbalace
10552 Philadelphia Rd.
White Marsh, MD 21162

ELECTRONIC DESIGN

Upcoming issues....

November 2 issue:
✔ Bonus distribution at Electronica '98!

Plus...November will also feature our "Career Opportunities in Electronic Engineering Supplement"

☛ Closing... *NOW*

Call Greg Marthe TODAY at 1.800.659.1710 ext 9589

CAREER OPPORTUNITIES
IN ELECTRONIC ENGINEERING

Reaching 173,000* Electronic Engineers in all Disciplines

Designed for Companies Recruiting Electronic Engineers

WIRELESS SYSTEMS DESIGN

Microwaves & RF

ELECTRONIC DESIGN

November Issue...

- **Space reservation deadline...**

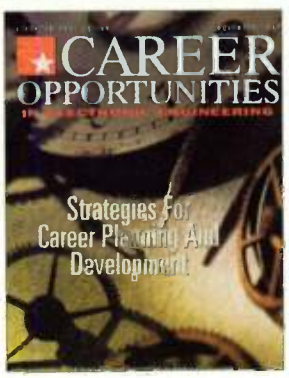
October 5

- **Deadline to submit artwork...**

October 12

Last chance for 1998!

Don't be left out!



Contact:

Greg Marthe
Recruitment Advertising Mgr.
Penton Media
1100 Superior Avenue
Cleveland, Ohio 44114
216.931.9589
fax 216.696.8206

* Unduplicated. Selected circulation from *Electronic Design, Microwaves & RF and Wireless Systems Design.*

FOR SALE

SPECTRUM ANALYZER
in a probe.
$249 Display on your inexpensive scope. Measure
µv/m,µv,ma.www.SPECTRUMPROBE.COM

SURPLUS INVENTORY

SURPLUS SALE

1,000,000 WALL TRANSFORMERS

5.8VDC/1.2A	CS119	$2.95
7.5VAC/3A	CS035	$6.25
9VDC/1.2A	CR147	$5.50
12VDC/1A	CR069	$4.90
12VDC/1.7A	CS182	$8.90
14.5VAC/1A	CR833	$3.75
16VAC/1.25A	CR924	$4.50

Min 1000/type -- Call for other types

SURPLUS TRADERS
PO Box 276,
Alburg, VT 05440
Tel: (01) 514-739-9328
Fax: (01) 514-345-8303

FREE CATALOG!

CIRCLE 240 ON READER SERVICE CARD

CAREER OPPORTUNITIES
IN ELECTRONIC ENGINEERING
www.penton.com
www.penton.com
www.penton.com

In most cases, advertisements contained in Electronic Design employment section indicate that the companies are equal opportunity employers. The Federal Civil Rights Act of 1964, and other laws, prohibit discrimination in employment based on race, color, religion, national origin, sex or for any reason other than lack of professional qualification for the position being offered. It should be noted that employment advertisements in Electronic Design are published for the readers convenience and in no way, to the best of our knowledge, promote unlawful discrimination.

ELECTRONIC DESIGN

A Penton Publication

Penton

Penton Media, Inc.

Thomas L. Kemp, *Chief Operating Officer*
Daniel J. Ramella, *President/Chief Operating Officer*
Joseph G. NeCastro, *Chief Financial Officer*
David B. Nussbaum, *Executive Vice President/Group President*
James D. Atherton, *Group President*
James Zaremba, *Group President*
Preston L. Vice, *Senior Vice President, Publishing Services*
Stephen A. Sind, *Vice President, Trade Show Development*
Russell S. Carson, *Vice President/Group Publisher*
John G. French, *Vice President/Group Publisher*
Joseph M. DiFranco, *Vice President/Group Publisher*
Susan J. Grimm, *Vice President Publishing Systems & Support Services*
Charles T. Griesemer, *Vice President/Controller*
Katherine P. Torgerson, *Vice President, Human Resources & Executive Administration*
Andrew C DeSarle, *Vice President, Ancillary Product & Sales*
Mary E. Abood, Director, Corporate Communications

Publisher: John French
Hasbrouck Heights, NJ; (201) 393-6060
Director Of Global Sales: Russ Gerches
Hasbrouck Heights, NJ; (201) 393-6045
Director Of Marketing: Walker Johnson
San Jose, CA (408) 441-0550, FAX: (408) 441-6052
Production Manager: Eileen Slavinsky
Hasbrouck Heights, NJ; (201) 393-6093
Marketing Research Administrator: Deborah Eng
Hasbrouck Heights, NJ; (201) 393-6063

Advertising Sales Staff
Hasbrouck Heights: Judith L. Miller
Sales Asst.: Jeanne Sico
611 Route #46 West, Hasbrouck Heights, NJ 07604;
Phone: (201) 393-6060, Fax: (201) 393-0204
Boston & Eastern Canada: Ric Wasley
Sales Support: Karen Harrison
60 Hickory Drive, Waltham, MA 02454;
Phone: (617) 890-0891FAX: (617) 890-6131
Chicago/Midwest: Lisa Zurick
Sales Assistant: Dawn Heili
180 N. Stetson Ave., Suite 2555 Chicago, IL 60601;
(312) 861-0880 FAX: (312) 861-0874
San Jose:
Jeff Hoopes, Mark Allen, Tina Jamison
Sales Support: Liz Torres, 2025 Gateway Pl.,
Suite 354 San Jose, CA 95110;
(408) 441-0550 FAX: (408) 441-6052 or (408) 441-7336
North California/Colorado/Utah: Tina Jamison (408) 441-0550
North California/N.Mexico/Arizona:
Mark Allen (408) 441-0550
Pacific N.W. & Western Canada:
Jeff Hoopes (408) 441-0550
Los Angeles/Orange County/San Diego: Ian Hill
Sales Asst: Audrey Pantoja,
9420 Topanga Canyon Blvd.,
Suite 200, Chatsworth, CA 91311;
(818) 349-1100 FAX: (818) 349-1181
Texas/Southeast: Bill Yarborough
908 Town & Country Blvd. Suite 120. Houston, TX 77024;
Phone: 713-984-7625. FAX: 713-984-7576
Telemarketing Manager: Kimberly A. Stanger
(201) 393-6080
Direct Connection Ads & Direct Action Cards:
Judy Stone (201) 393-6062
Reprints Manager: Anne Adams (216) 931-9626

General Manager, European Operations: John Allen
36 The Green, South Bar Banbury. Oxford OX 16 9AE, U.K.
Phone: 44 (0)-1- 295-271003 FAX: 44 (0)-1- 295-272801
Netherlands, Belgium: Peter Sanders,
S.I.P.A.S. Int'l Media Representative, Rechtestraat 58-Postbus 25
1483 ZG DeRyp, Holland, 31-299-671303 Fax: 31-299 671500
France: Fabio Lancellotti
Defense & Communication
10 Rue St. Jean 75017 Paris France
Phone: 33-142940244. FAX: 33-143872729
Spain/Portugal: Miguel Esteban
Publicidad Internacional Pza.
Descubridor Diego de Ordas,
1 Escalera, 2 Planta 2D 28003 Madrid, Spain
Phone: 91/4416266 FAX: 91/4416549
Scandinavia: Paul Borrett
Hartswood Media, Hallmark House.
25 Downham Road, Ramsden Heath,
Essex, CM 11 1PV, UK.
Phone: 44-1-268-711560, Fax: 44-1-268-711567
Germany, Austria, Switzerland: Friedrich Anacker
InterMedia Partners GmbH Deutscher Ring 40
42327 Wuppertal, Germany
Phone: 49 (0) 202 271 690 Fax: 49(0) 202 271 6920
Hong Kong: Tom Gorman, Kenson Tse
CCI Asia-Pacific Ltd.
101 Pacific Plaza, 1/F, 410 Des Voeux Road West, Hong Kong
Tel: 852 2858 0789 Fax: 852 2857 6309
Israel: Igal Elan, Elan Marketing Group
24 Daphna St., Tel Aviv, Israel
Phone:972-3-6952967 FAX: 972-3-268020
Toll Free in Israel only: 177-022-1331
Japan: Hirokazu Morita,
Japan Advertising Communications
Three Star Building 3-10-3-Kanda Jimbocho
Chiyoda-Ku, Tokyo 101, Japan
Phone: 3 3261 4591. FAX:3 3261 6126
Korea: Young Sang Jo,
BISCOM
Rm 521, Midopa Building 145
Dangiu-Dong, Chongo-Ku, Seoul, Korea
Phone: 82 27 397 840 FAX: 82 27 323 662
Taiwan: Charles Liu, President,
Two-way Communications, Co., Ltd.
11F/1, No.421, Sung Shan Road
Taipei 110, Taiwan R.O.C.
Phone: 886-2-2727-7799;FAX: 886-2-2728-3686
United Kingdom: John Maycock
John Maycock Associates
Provincial House
Solly St. Sheffield S1 4BA

INDEX OF ADVERTISERS

Domestic*
International **

OK. Find SFRxxx in 70ns (before getting MADxxx)

Need Help Making Prompt Connections? So do Internet Switches.

The Genesis of Internet Address Processing: **MUSIC MUAC4K64 Routing Co-Processor (RCP™).** IP switching performance depends on the efficient recognition of IPv4 addresses that identify the route and destination of each packet. Based on **MUSIC CAM** technology, **RCP** speeds Internet packet identification. Latency is minimized, address processing related jitter vanishes, and bandwidth is relieved of IP recognition.

RCP takes advantage of IP Classless Inter Domain Routing (CIDR) to find the best prefix, "longest match" in an IP routing table. **MUAC4K64** recognizes the best prefix match of any IPv4 address in 70ns, exceeding a compare rate of **14M** packets per second – enough to support 8 ports of Gigabit Ethernet or over 80 ports of 100Mb ***at wire speed!***

MUSIC RCP also finds exact matches for 48 bit MAC addresses. This function can be mixed with IPv4 addressing within the same device, making the **MUAC4K64** perfect for L2/L3 switches. With a 4K density, they are cascadable to handle lists of any practical depth. At 3.3v in a 100 PQFP, VHDL and Verilog models add to design ease. Starting @ $30, **MUSIC RCP** ***is the best fare going.***

USA	**Voice 888-CAM-MUSIC** **Fax 908-979-1035**
In Europe: Holland	**Voice +31 45546 2177** **Fax +31 45546 3738**
In Asia: Manila	**Voice +6392 549 1480** **Fax +6392 549 1024**

Distributors in USA:

Sager Electronics	**800-SAGER800**
All American	**800-573-ASAP**

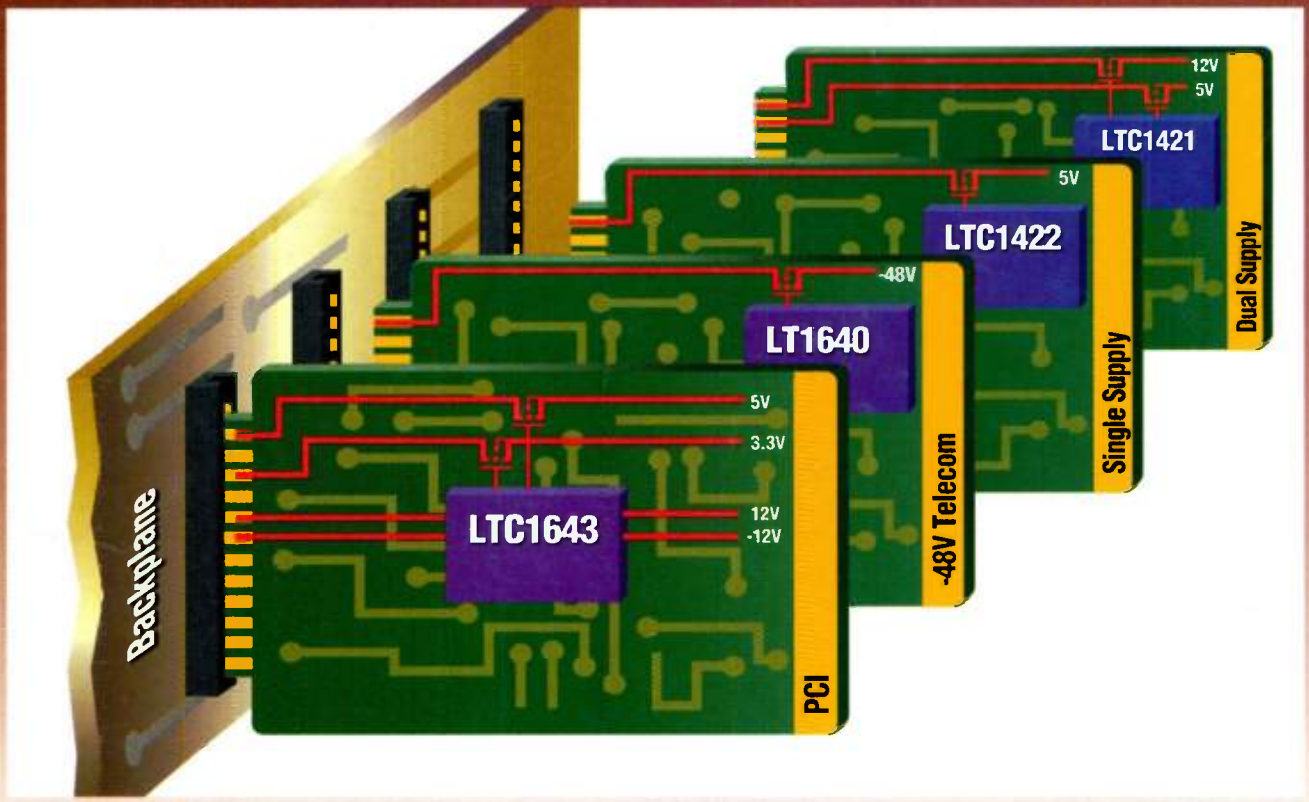
Email info@music.com

Application Notes and Data Sheets at www.music.com

MUSIC SEMICONDUCTORS

READER SERVICE 120

Hot Swap 'Em All!



A Complete Family from PCI to -48V Telecom

Controlling your power supply during hot swap demands attention to the unique details of your application. So choose an application-specific hot swap controller with the flexibility to meet your unique demands—from PCI to -48V applications. LTC Hot Swap Controllers can be programmed for most aspects of supply ramping, current limiting and voltage monitoring. Choose Linear Technology and hot swap safely.

Features

- Allows Safe Insertion and Removal from a Live Backplane
- Programmable Current Limit
- Programmable Power Up Rate
- High Side Driver for N-Channel MOSFETs
- LTC1421, $4.90 each in 1k qty.
- LTC1422, $2.75 each in 1k qty.
- LT1640, $1.90 each in 1k qty.
- LTC1643, $4.25 each in 1k qty.

Hot Swap Controllers

Part	Supplies	Voltages
LTC1421	2	3V to 12V
LTC1422	1	3V to 12V
LT1640	1	-48V (-10V to -80V)
LTC1643	4	3.3V, 5V, ±12V

Data Sheet Download

www.linear-tech.com/go/LTCHotSwap/edes

Free Sample/CD ROM

Call: 1-800-4-LINEAR
Visit: www.linear-tech.com

New CD-ROM! LinearView 3.0

More Information

Lit: 1-800-4-LINEAR
Info: 408-432-1900
Fax: 408-434-0507

1630 McCarthy Blvd., Milpitas, CA 95035-7417

LINEAR TECHNOLOGY

FROM YOUR MIND TO YOUR MARKET
AND EVERYTHING IN BETWEEN

READER SERVICE 110