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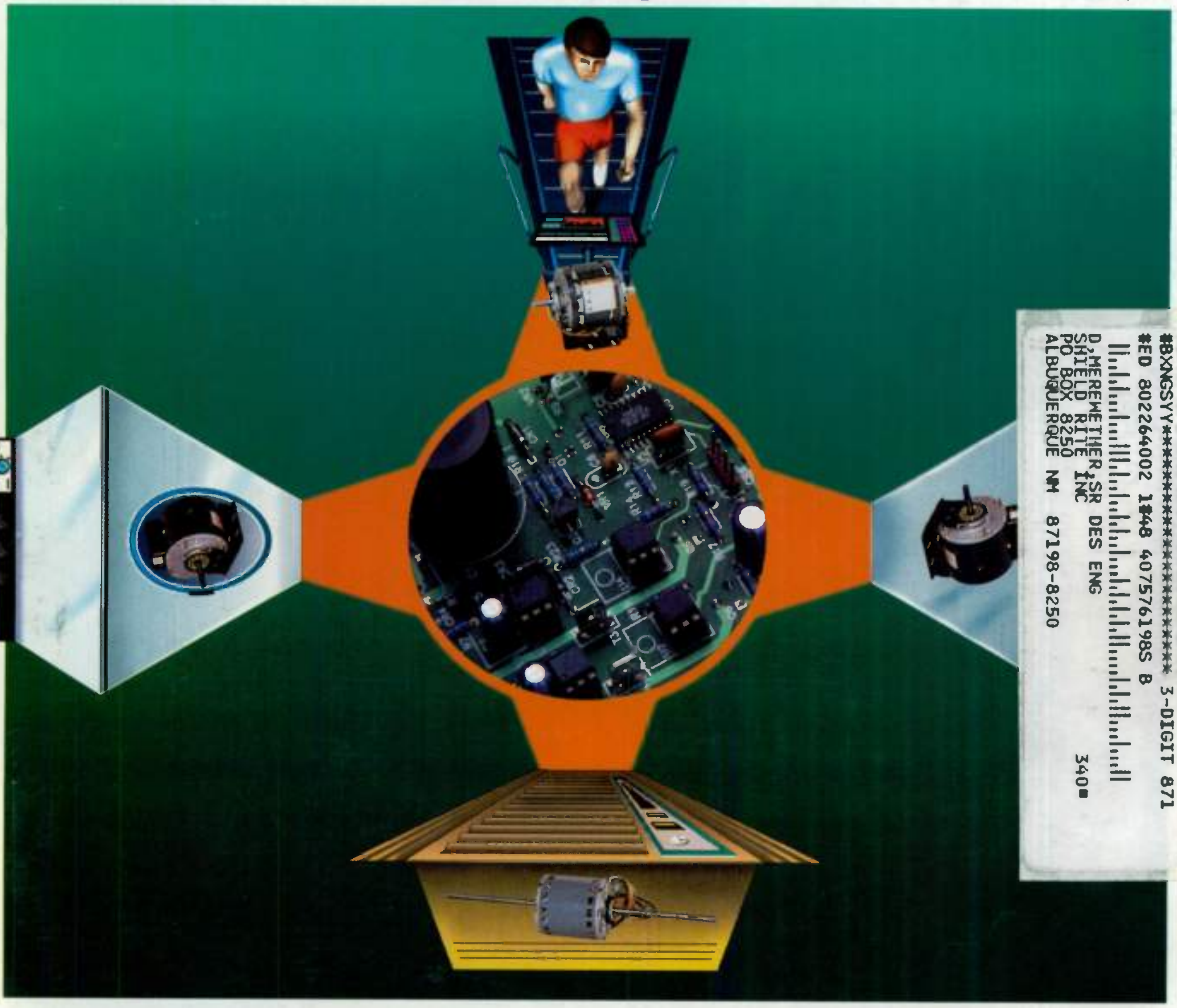
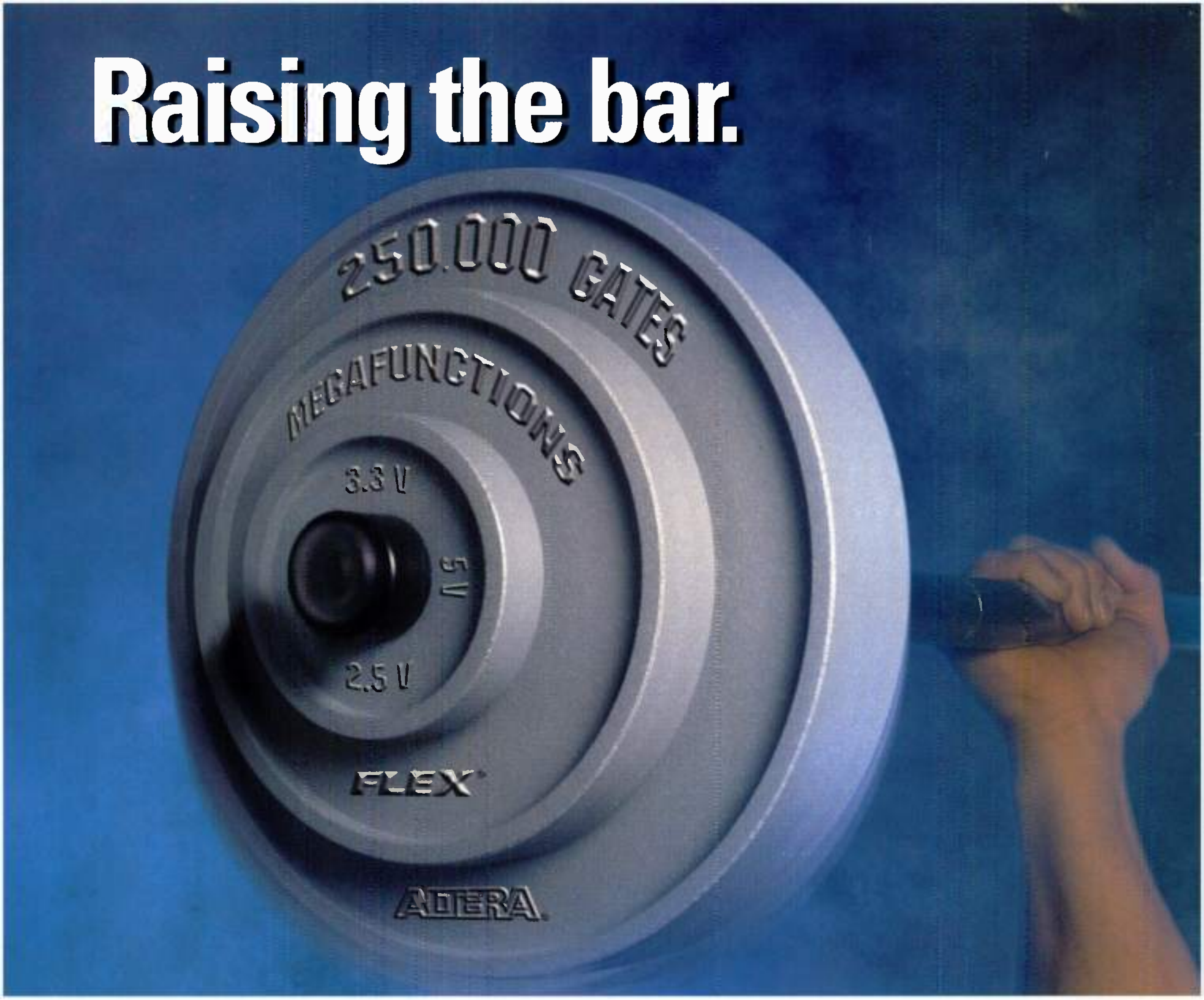
ELECTRONIC DESIGN

TECHNOLOGY · APPLICATIONS · PRODUCTS · SOLUTIONS

A PENTON PUBLICATION $8.00 www.elecdesign.com OCTOBER 22, 1998



Controller Eyes AC Motors In Consumer Applications p. 36



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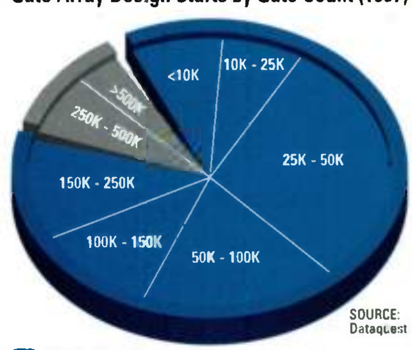

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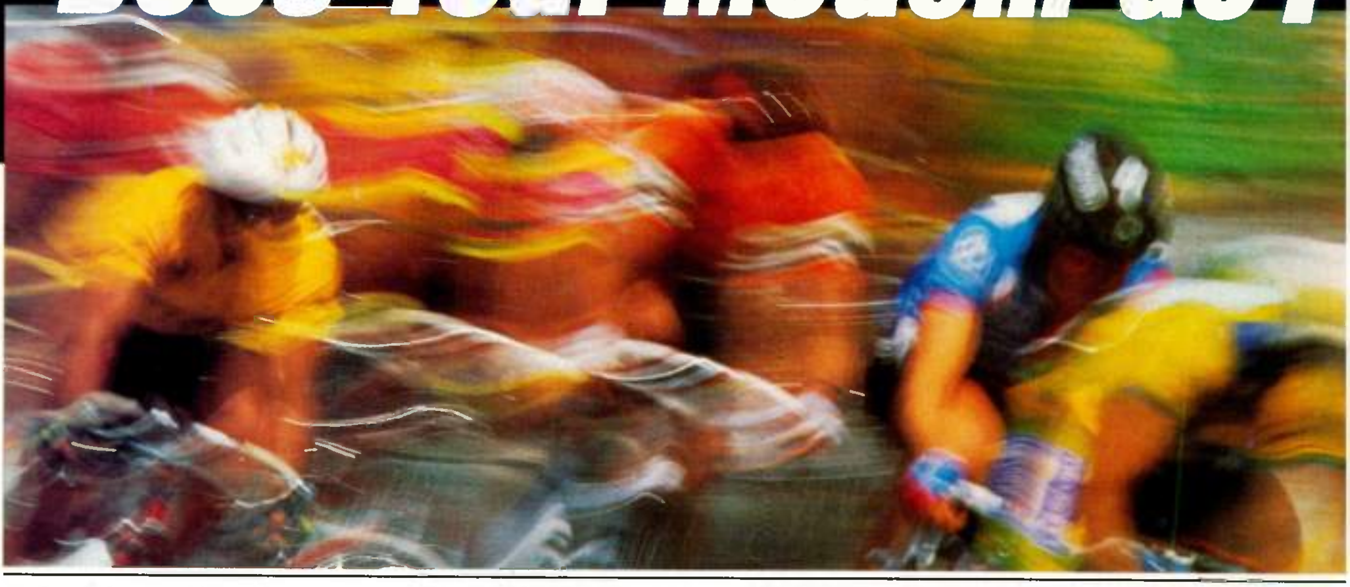
How Fast Does Your Modem Go?



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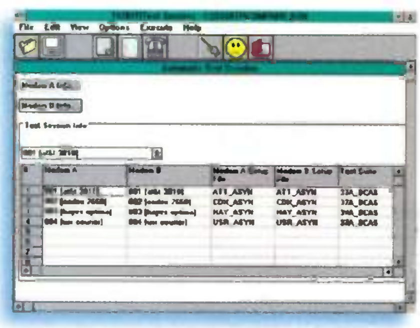

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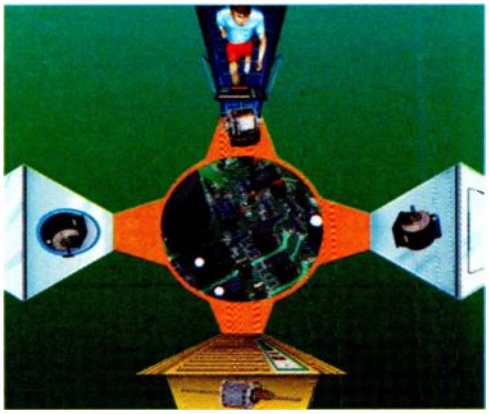
ELECTRONIC DESIGN

TECHNOLOGY• APPLICATIONS• PRODUCTS• SOLUTIONS

October 22, 1998 Volume 46, Number 24

EDITORIAL OVERVIEW



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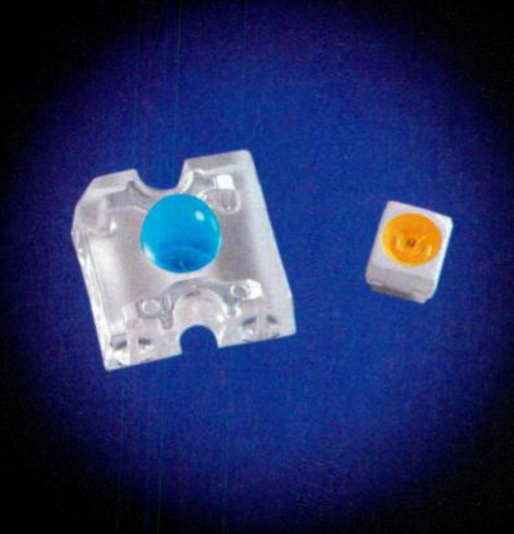
When A Leading European Automotive Company Needed Reliable LED Lamps,



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October 22, 1998 Volume 46, Number 24

EDITORIAL OVERVIEW

QUICKLOOK

COVER ILLUSTRATION BY:
TONY VITOLO

LOOKING AHEAD: November 2, 1998

- **Previewing Fall Comdex:**.......... Consumer issues, software, Java, Internet topics, and platforms are all on the agenda for this annual Fall Comdex Show previewed by Computer Systems Editor Jeff Child.
- **A Preview Of Electronica '98:**... Read all about the latest wares at the world's largest component show, Electronica '98, previewed by our Munich, Germany, correspondent Alfred Vollmer.
- **Special Report On Laser Drivers:**.. This Special Report by Digital ICs Editor Dave Bursky takes the wraps off the latest techniques to drive laser diodes as optical data rates shoot into the gigahertz range.
- **Special Report On Bus Bridges:**... All the chip and board solutions designers use to solve complex bridging issues are examined by Computer Systems Editor Jeff Child in this Special Report on bus bridges.
- **Special Digital Section, Part 2:**.. This two-parter concludes with a report by T&M Editor Joe Desposito on a standard programming and test language for PLDs, as well as design applications on the use of complex PLDs.

Jesse H. Neal Editorial Achievement

1967 First Place Award	1978 Certificate of Merit
1968 First Place Award	1980 Certificate of Merit
1972 Certificate of Merit	1986 First Place Award
1975 Two Certificates of Merit	1989 Certificate of Merit
1976 Certificate of Merit	1992 Certificate of Merit


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About Electronic Design

ONLINE OVERVIEW

October 22, 1998 Volume 46, Number 24

See Electronic Design Online's Table of Contents to preview what's in store for you on the web!

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Could you use a Palm Pilot? Or an IOmega Zip drive? How about a Magellan GPS 400XL Navigation System? Or, what about a seat in a Verilog or VHDL class (a $1395 value)? Well, you could win any one of these great prizes by using your creative writing skills!

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	PIC16C6XX PIC16C7XX PIC16F8X PIC16C9XX	512 x 14 1K x 14 2K x 14 4K x 14 8K x 14	80–368	18, 20, 28, 40, 44, 64, 68	13–52	33	68HC05 68HC08 80C51 ST6, ST7 COP8
	PIC17C4X PIC17C7XX	2K x 16 4K x 16 8K x 16 16K x 16	232–902	40, 44 64, 68 80, 84	33–66	10	H8, 68HC11 68HC16, ST9 MCS251 80C51XA

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Enhance graphics power with 16Mb synchronous GRAMs

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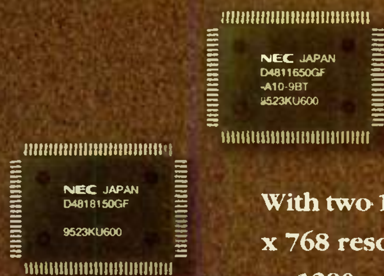

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Density	8Mb	16Mb
Organization	128K x 32 x 2 banks	256K x 32 x 2 banks
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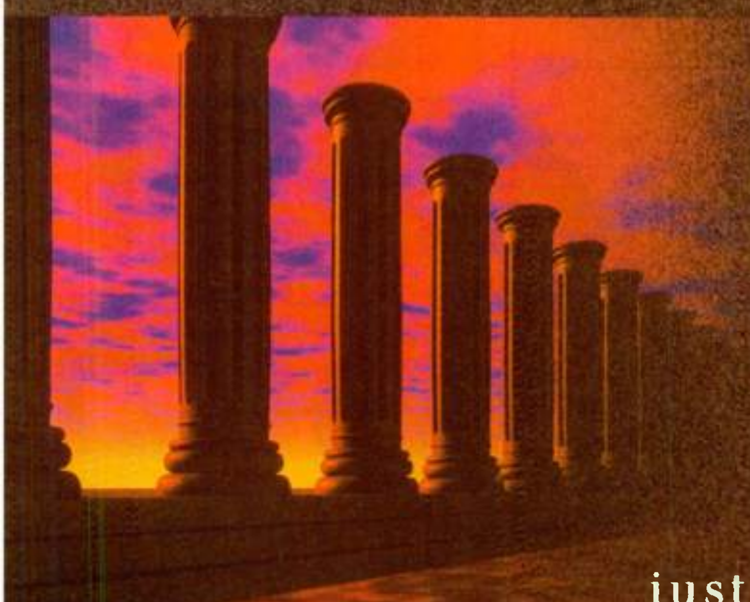
Supply voltage	3.3V±0.3V	
Operating frequency	83/100MHz (max.)	83/100/125/143MHz (max.)
Interface	LVTTL	
Refresh cycle	1K cycles/16ms	2K cycles/32ms
Graphics function	Write-per-bit, 8-column block write	
Package	100-pin QFP (14 x 20mm)	100-pin thin QFP (14 x 20mm)



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EDITORIAL

Look Beneath The Cover

On a recent California road trip, I stopped by a microelectronics company to say hello and get an update on what's going on. While waiting in the reception area, a poster on the wall immediately caught my eye. It was a blown-up cover of an *ELECTRONIC DESIGN* issue that had featured the company's new product as the cover article.

As you may or may not know, we demand exclusivity when we write a cover story. We want our cover articles to stand out from the competition because we tell you, our readers, that we're taking a stand. Utilizing our expertise and credibility, we say, "We Believe This Product/Technology Is Important!"

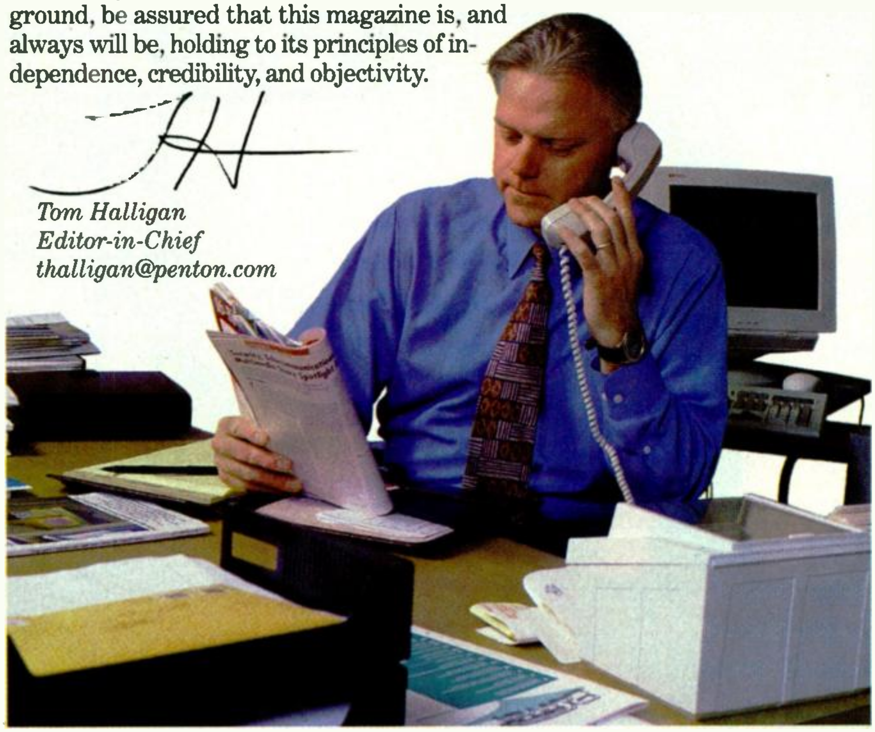
No other magazine takes that risk. And, it is a risk. Throughout this magazine's history, our editors discovered and proposed cover features from little known companies whose product, they believed, would excite our readers. Obviously, it's easier to find technological breakthroughs or products from the industry giants. But, the company's size or longevity never factors into our decision. When a cover article proposal is submitted, the managers analyze and debate the product/technology on its worthiness to win a cover—period. The majority are rejected because they fall short of meeting our standards. Is the product a major technological advancement? Does it offer a quantum leap in performance? Our review team of executive and managing editors—all degreed engineers with more than 15 years in the business—conclusively makes a decision based solely on those high criteria.

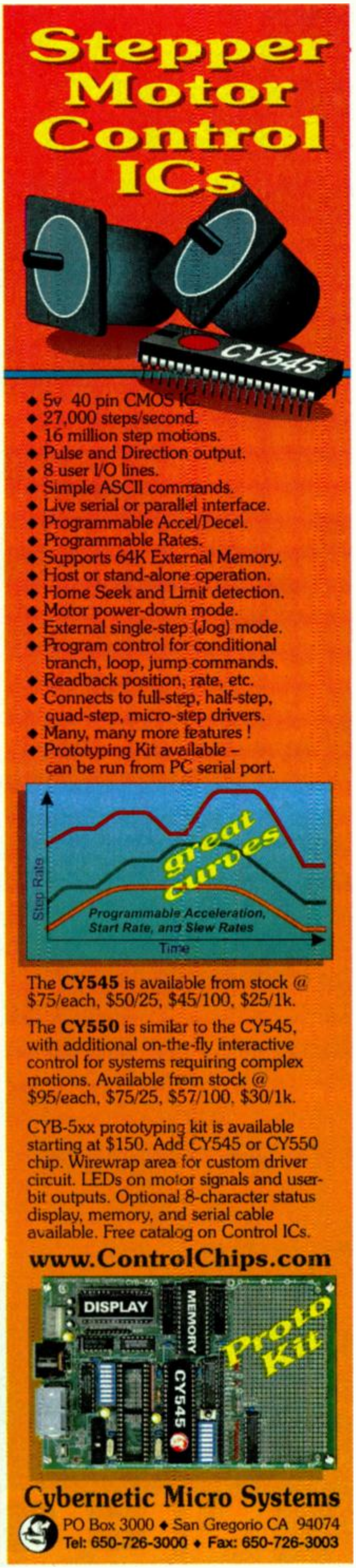
We get the story first because we're willing to put our editorial independence and credibility on the line. However, it's not always easy. There are a lot of new products/technologies being rolled out almost every day that vie for only 25 cover articles per year. But, we're confident that we select the products/technologies that will make a difference to you.

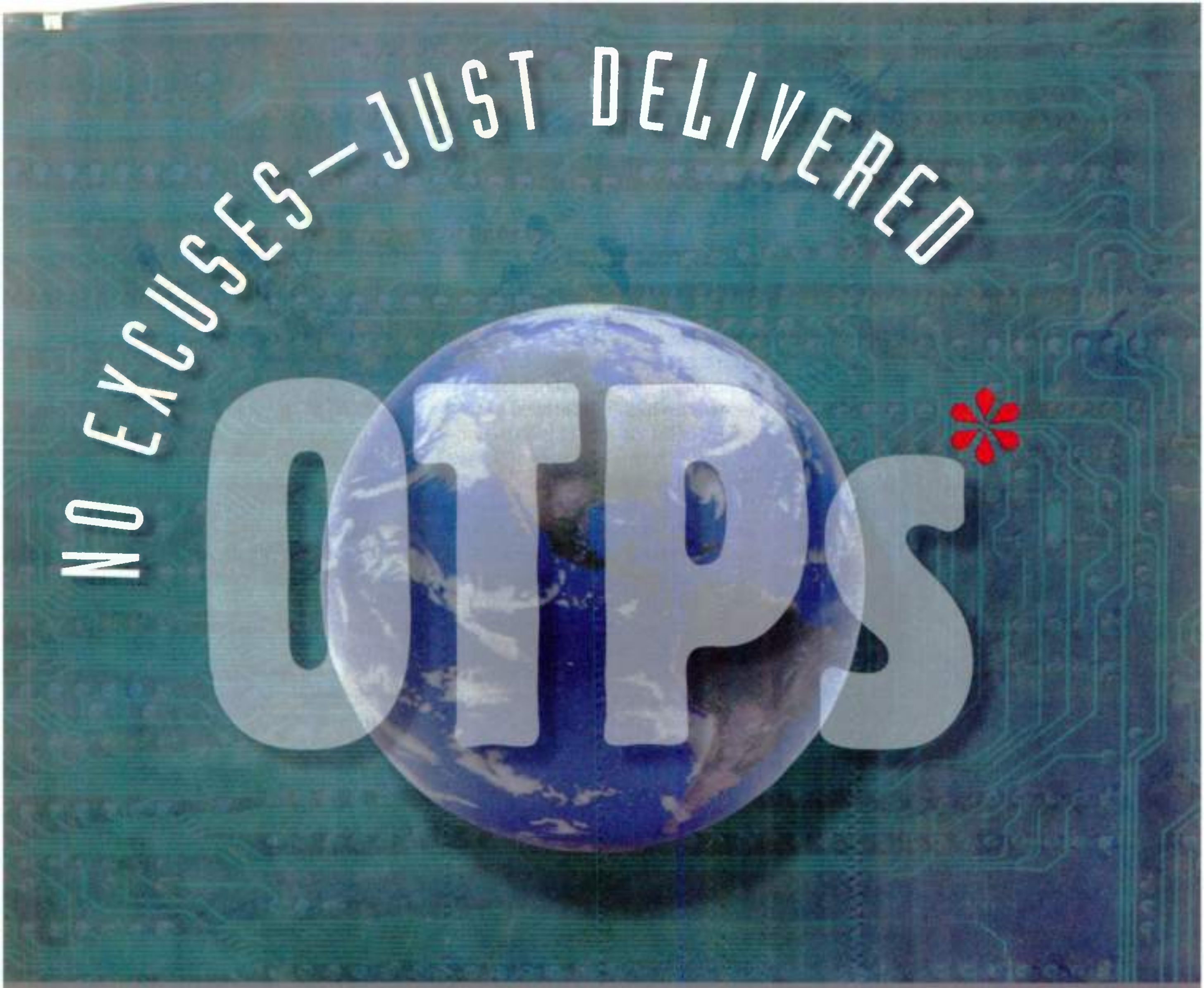
Credibility and independence, in my mind, are the two most important principles that I have to uphold as Editor-in-Chief. From cover articles to back-of-the-magazine new product announcements, we decide what editorial fills our magazine based solely on its value to you. As a board member of the American Business Press Editorial Committee, I insist that our editors follow the recently introduced Editorial Code of Ethics. Basically, this code is a guideline trade publishing editors and writers can follow to ensure editorial integrity and credibility.

In today's world, where the words "integrity" and "credibility" stand on shaky ground, be assured that this magazine is, and always will be, holding to its principles of independence, credibility, and objectivity.

Tom Halligan
Editor-in-Chief
thalligan@penton.com







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68HC705P6A	4.6K	176	28	M68ICS05P	KITMMEVS05P6A	KITMMDS05P6A
68HC705C8A	8K	304	40,44	M68ICS05C	KITMMEVS05C	KITMMDS05C
68HC705C9A	16K	352	40,44	M68ICS05C	KITMMEVS05C	KITMMDS05C
68HC705B16	15K	352	52,64	M68ICS05B	KITMMEVS05B	KITMMDS05B
68HC705L16	16K	512	80	KITPGMR05L16	KITMMEVS05L16	KITMMDS05L16

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Batty Over Batteries? You Aren't Alone.

With the 1997 worldwide market for batteries estimated at around $22 billion and expected to expand to $41 billion by 2002, no one can underestimate the lengths to which many companies will go to corner their share of this most lucrative of markets. For many, these lengths include lies, propaganda, and misinformation. For other, more reputable companies, the path to success has been that of solid research, product development, and customer information—though even these companies would be reluctant to "cast the first stone." Most happily take advantage of the many shades of skullduggery that are actually acceptable, if not expected, in this open market economy. In the world of batteries, few topics highlight ethical extremism as much as the ongoing debate over the safety of lithium-ion (Li-ion) technology and its recent descendent, Li-polymer.

To set the record straight, Li-ion technology, in its present-day form, is safe. So where's the debate? The debate stems from the fact that Li-ion technology is not "inherently" safe. It has achieved its safety qualification through the use of checks and stops that all but guarantee it won't explode under duress. Each of these precautions require add-on components, thereby tacking substantial cost onto an already expensive item. Unfortunately, removing any one of these components can reduce the battery's safety rating by a factor of 10.

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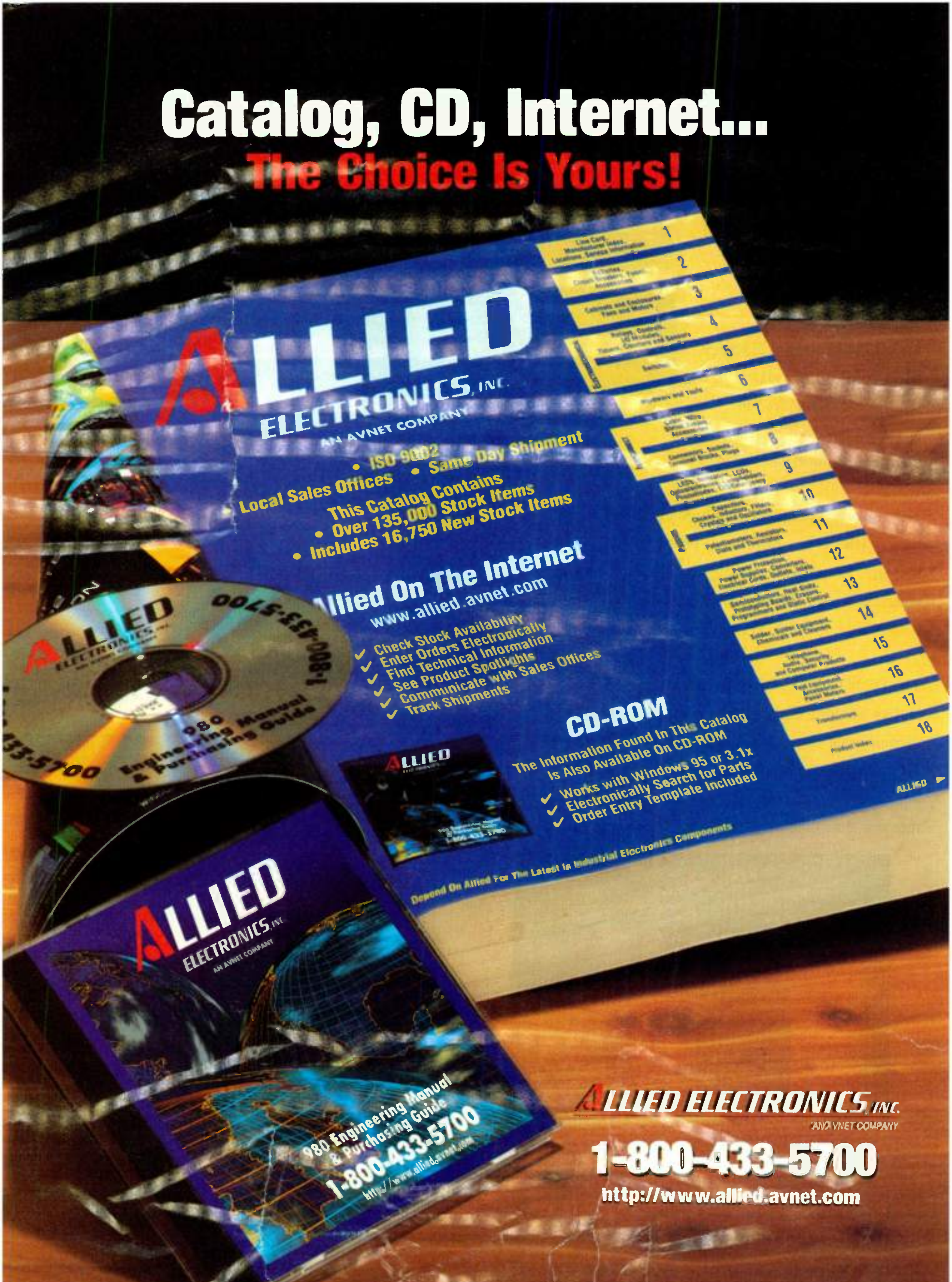
For most reputable battery companies, the choice is obvious—safety at all costs. Unfortunately, safe is a relative term. In a world where most everything boils down to the almighty dollar, its definition gets painfully stretched on the altar of commerce with numerous, unheard-of battery manufacturers lying prostrate before it. Cognizant of the billions of dollars at stake, these companies—many of whom are unable or unwilling to perform their own research—introduced low-cost, "me-too" Li-ion batteries with a catch. Many safety checks mandated by the more established companies have been left out—hence the cost savings.

We've all heard about the laptop that exploded on an airplane, or the cell phone that burned up. But, these stories remain anecdotal. Even the devices without all the safety checks have yet to be proven deadly. Nonetheless, for the designer in a cost crunch, it's still very much a case of buyer beware when you forsake mainstream suppliers.

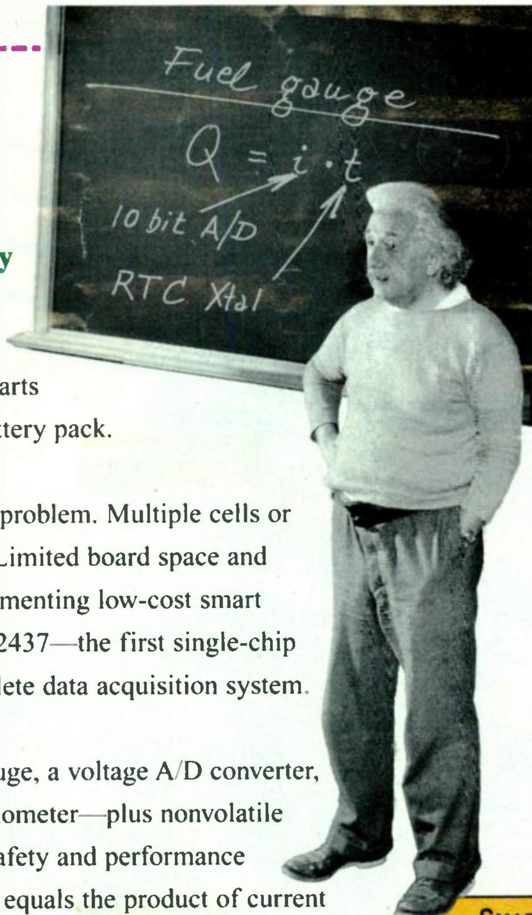
With newer technologies, such as Li-polymer, the picture would remain pretty much the same—but for the polymer. By eliminating the liquid electrolyte, which has a tendency to ignite should it escape from the cell in a hot environment, manufacturers have removed yet another obstacle to the proliferation of Li-ion technology. Along with its packaging advantages and power-density improvements, Li-polymer batteries promise to open up a whole new range of applications—should they ever actually become available. So far, they've been a classic example of vaporware—all tell and no show. As a result, these batteries have been the subject of much preemptive hype from companies buying time at the designer's expense as they iron out the technology's wrinkles. This has not been good for Li-polymer's image, so it is with much relief that a number of companies finally lie on the cusp of announcing product en-masse in the coming months.

The safety advantages Li-polymer offers, however, may not be enough. At the Power'98 conference this weekend (Oct. 4 to 6), Santa Clara, Calif., the ongoing debate over whether or not batteries should be allowed to be recharged, or even permitted on airplanes, comes to a head. With anyone who's anyone in the industry set to share their thoughts on the matter, it'll be anything but dull. The topics for heated discussion not only revolve around the charging and safety factors, but also involve the toxic effects should the airplane go down over water. Not too many rescue divers want to approach an underwater crash site laden with lithium. Possible solutions to this problem abound, and will be one of many subjects relating to Li-ion technology that will be dealt with in an upcoming report in *ELECTRONIC DESIGN*. Feel free to contribute by contacting me at pcmann@ibm.net.



READER SERVICE 103

Want a Better Battery? Give it a Better Brain!

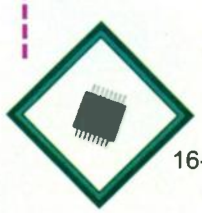


It doesn't take a *genius* to prevent overcharging and undercharging. The **DS2437 Smart Battery Monitor** provides all the real-time data required to analyze a battery. It's the smarts you need to build a better battery pack.

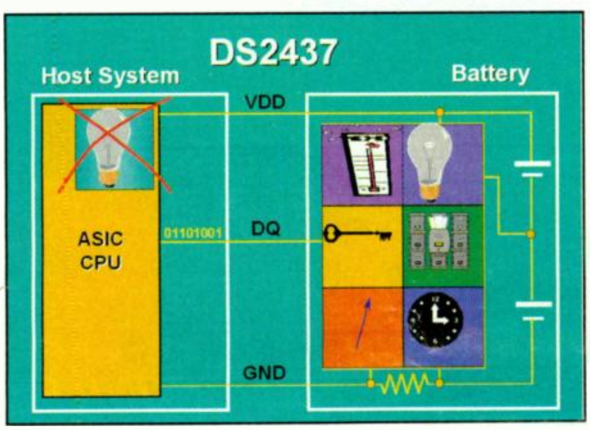
Your favorite chemistry? No problem. Multiple cells or battery packs? No problem. Limited board space and budget? No problem. Implementing low-cost smart batteries is easy with the DS2437—the first single-chip battery monitor with a complete data acquisition system.

The DS2437 packs a fuel gauge, a voltage A/D converter, and an accurate digital thermometer—plus nonvolatile memory that stores critical safety and performance information. Because charge equals the product of current and time, the Smart Battery Monitor calls upon an accurate real-time clock crystal. Now you can optimize battery performance by adjusting the charging process or system operation. With the exclusive 1-Wire™ interface, the pack needs just three connections with the host CPU. Other chips need five or six.

For more information, call us at 972-371-4448, and start building brainier batteries right away!



16-pin SSOP



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READER SERVICE 110

Star*Core's First Joint DSP Architecture Previewed At Forum

The first results of the joint DSP architecture development work between Lucent Technologies' Microelectronics Group and Motorola's Semiconductor Sector, announced in June, were disclosed at the recent Microprocessor Forum in San Jose, Calif. At the Forum, the two companies described Star*Core 400, a highly scalable and compiler-friendly digital-signal-processor architecture that's radically different than the current types based on multi-MAC, superscalar, or the very long instruction word (VLIW).

"The Star*Core 400 is the first DSP architecture that is truly scalable," says Kevin Kloker, Star*Core architecture director, and formerly Motorola's director of DSP architecures for the Wireless Subscriber Systems Group, Schaumburg, IL. Fundamentally, the Star*Core 400 is a scalable instruction model with variable length execution sets (VLESs) and explicitly parallel instruction computing (EPIC).

In this architecture, adds Kloker, the computational resources, such as data and address ALUs, registers, instruction set accelerators, data bandwidth, and memory accesses can be scaled by implementation. Consequently, multiple traditional digital-signal-processor cores, as well as massively parallel cores, can be derived from this architecture, claim the Star*Core designers. Furthermore, because the instruction parallelism is scaled by the compiler in this architecture, the Star*Core 400 offers code density that's comparable to embedded RISC processors, according to Kloker.

From the specifications presented at the Forum, the Star*Core 400 offers 1200 DSP MIPS at a 300-MHz clock frequency, based on 4 multiply-accumulates per cycle. Implemented in a 0.13-µm CMOS process, it incorporates 16-bit data, 32-bit address, and 40-bit accumulators. Other features of the architecture include unified data and program space, and eight data words per clock (4.8 Gbytes/s). The basic instruction is 16 bits, while VLES is 128 bits.

According to James Boddie, the executive director of the joint Star*Core center and Bell Labs Fellow, the complete software tools, design information, and architectural details for the Star*Core 400 will be available in the first half of 1999. The core silicon implementation is expected in the second half of 1999.

This architecture comes as a response to emerging wideband communications systems. These include 3G wireless standards, software radios, MPEG-4, and video-on-demand, as well as other Internet applications that require enormous processing power. While the two companies have been quietly developing this architecture for about a year, the Atlanta, Ga.-based joint Star*Core design center will officially open in November of this year. AB

VXI Technology Opens Its Modular Platform

For the past several years, VXI Technology Inc., Irvine, Calif. has been developing products for its VXI Modular Instrumentation Platform (VMIP). During this time, according to the company, VMIP has become the most widely used modular instrumentation product on VXI, with thousands of users worldwide. This success has led VXI Technology to make VMIP an open platform.

Up to three of the smaller VMIP instruments, which can be mounted in a single C-size VXIbus card, can be mixed and matched for greater flexibility. Nothing is lost in the downsizing of the instruments, since the VMIP offers all of the VXIbus' features. Each module is treated as a separate VXIbus device with its own unique logical address and VXI*plug&play* driver. All seven supply lines available on the VXIbus are brought to the internal VMIP connectors for use by the modular instruments. For this reason, virtually any type of VMIP instrument can be designed for the VXIbus.

An open VMIP means vendors other than VXI Technology can develop instrumentation on a modular footprint and leverage the cost, size, and modularity benefits. Also, custom functionality can be added to a customer's test station without taking up a complete VXIbus card slot. For more information about VMIP, check out VXI Technology's web site at *www. vxitech.com.* JD

Wafer-Level Packaging Shrinks CMOS Image Sensors

The CMOS imaging sensor, whose small size, efficiency, and low cost has propelled its quick domination of the low to medium end of the imaging market, is about to shrink even further. An agreement forged between ShellCase Ltd., Manhat Technology Park, Jerusalem, Israel, and Tower Semiconductor, Migdal Haemek, Israel, allows Tower to use ShellCase's proprietary, wafer-level Opto-CSP manufacturing technology for the packaging of ICs with CMOS image sensors.

Though the CMOS imager isn't inherently much smaller the the CCD imager it now replaces in many applications, according to ShellCase's Avner Badihi, it has far more integration capabilities than the CCD technology. Thus, it can integrate functions such as digital signal processing, amplifiers, memories, etc., on the die. The CCD would have required a complete die set, in addition to the imaging device, to carry out all of these functions. On the board, this translates to a smaller total area need.

Now, using Shellcase's expertise, the already established CMOS advantages can be combined with the advantages of the company's wafer-scale packaging of optoelectronic devices. Among these advantages are: a true die-size package, configurable spectral transparency, optional dichroic optical filters integrated into the package, optional mosaic-colored die integrated into the package, a thickness of 0.5 to 1.0 mm, a peripheral- and area-array configuration, and a complete mechanical enclosure of the die. While CCDs have recently begun to compete favorably with CMOS sensors with respect to cost, both Tower and Shellcase expect to keep the cost of highly integrated CMOS sensors within that of the die itself—between $5 and $10.

For further information, contact Tami Mazel, ShellCase Ltd., at (888) 870-7225; e-mail: *marketad@shellcase.com; ww.shellcase.co.il.* PM

Edited by Roger Engelke

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SP503	7	7	RS-232 RS-422 RS-485 RS-449 V.35 EIA-530	+5V	7 drivers and 7 receivers, supports DTE or DCE applications
SP504	7	7	RS-232 RS-422 RS-485 RS-449 V.35 EIA-530 V.36 EIA-530A	+5V	on-chip switched resistors for simplified V.35 termination, supports DTE or DCE applications
SP505	7	7	RS-232 RS-422 RS-485 RS-449 V.35 EIA-530 V.36 EIA-530A	+5V	single chip multi-protocol serial interface transceiver no external termination resistors.
SP522	2	2	RS-232 RS-422 RS-485 RS-423	+5V, +10V, -10V	low cost multi-protocol transceiver integrated circuit, individual tri-state control
SP524	4	4	RS-232 RS-422 RS-485 RS-423	+5V, +10V, -10V	low cost multi-protocol transceiver integrated circuit, ideal for V.36 applications

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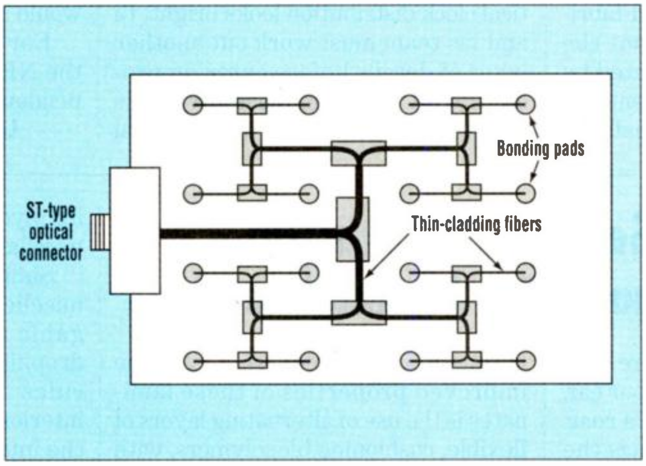
Optical Fibers Promise To Send Gigahertz Clocks Across Circuits Without Skew Or EMI

As clock speeds in computers and communication systems approach 1 GHz, designers face a formidable task. They must create distribution and de-skewing schemes to ensure the accurate, synchronized flow of data. The answer to their dilemma may lie in optical fibers embedded within printed-circuit boards, according to a team of researchers at NEC Research Laboratories, Princeton, N.J.



1. To test the concept of optical distribution of signals on a pc board, the NEC team built a test article that incorporated a standard ST-type optical connect. All fiber runs from the connector were kept the same length to ensure in-phase arrival of the signal at each end point.

To come up with a practical fiber-optic distribution system within a pc board, the team, headed by NEC's Yao Li, is experimenting with a variety of materials and methods. Li and his team members believe such a board production environment can be realized within a few years.

Because of the parasitic effects of signal traces and unequal path lengths, the very fast clock speeds will produce disastrous timing offsets between chips. Noise generated by these signals also is becoming a problem. The sharp-edged logic signals create strong interference across the RF band, which can wreak havoc with neighboring circuits and any radio or analog signal components unlucky enough to be nearby. Shielding can help at the expense of extra design time, increased board area, and additional ground plane layers in the pc board.

Optical distribution of clock and timing signals across a board or system forms one solution. Some state-of-the-art supercomputers already employ optical clock distribution at the cabinet level, but these are expensive, semicustom applications. The NEC team's goal is to develop technologies that can inexpensively merge with current methods of manufacturing commercial equipment.

While some work has been done on free-space distribution systems, the researchers have concentrated on accomplishing this task with common plastic optical fibers. Team member Jan Popelek explains that fibers embedded within a garden-variety pc board aren't subject to most of the effects that skew electrical signals. Popelek adds that it's relatively easy to provide each chip with equal lengths of fiber to ensure exact arrival times.

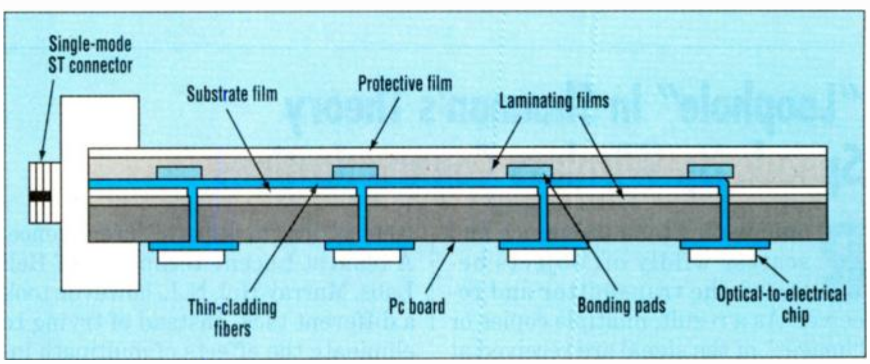
Initial experiments employed silica (glass) fibers because of their superior optical properties. But, for this application, plastic optical fiber (POF) proved more practical. POF's greater attenuation matters little on runs of a few feet, and it costs much less to manufacture. Plus, the brittle nature of silica fibers limits their bend radius, making it difficult to accomplish the tight turns required to fit multiple runs onto a relatively small board. POF, on the other hand, easily tolerates the tight radius (0.58 mm or smaller) 90° bends used to guide the fiber up through a via hole to its destination, the input of an IC.

Plastic's larger, softer fibers are easier to cut, handle, and terminate than the thinner silica counterparts. This trait helps POF adapt to the automated assembly techniques utilized to mass produce fiber-copper pc boards.

After initial tests confirmed that POF had acceptable losses when bent, the team fabricated several test articles to evaluate the feasibility of embedding the fiber within a pc board. For these proof-of-concept experiments, they used step-index polymethyl methacryliate (PMMA) fibers with a core diameter of 107 µm. A thin (7-µm) cladding was added for mechanical protection, as well as to provide a surface that could easily fuse to other fibers.

Using temperature and pressure, a group of fibers was fused at one end to create a small bundle. All fibers were then trimmed to an identical length. The fused end of the bundle was placed inside a standard ST optical connector and secured with epoxy. The entire fiber assembly was then placed onto the substrate of a partially laid up pc board (*Fig. 1*). Subsequent layers were laminated on top of the POF, leaving it embedded in the pc board.

Pressure-sensitive tapes on one side of the board held the fibers in place during assembly. Via holes were placed at the ends of these paths, with the fibers inserted into them so their ends



2. This vertical section of a POF-enhanced circuit board shows how the fiber is laminated onto the circuit's backside and fed to optical-to-electrical interfaces via feedthrough holes. A heat-resistant polymer film protects the fibers. To seal the board, the via holes were filled with epoxy.

reached the surface. A heat-resistant polymer sheet was then laminated over the fibers to protect them *(Fig. 2)*. To seal the board and secure the fibers, the via holes were filled with epoxy.

Initial results from the hand-fabricated prototypes indicate that the process could easily be automated by adapting existing wire placement and bonding equipment. Other tests involved embedding POF terminations into commercially available boards to make sure they wouldn't upset any critical electrical parameters.

While the future for POF-based optical clock distribution looks bright, Li and his team must work out another layer of details before entering production. Among the most obvious is the need to translate the optical signal back to electrons for use at its destination. No specific answers have been released at this time, but the researchers' papers indicate a surface-mounted, optical-to-electrical device would accomplish this task.

For further information, contact the NEC Research Institute, 4 Independence Way, Princeton, NJ 08540.

Lee Goldberg

Researchers See Seashells As Shortcut To Stronger Laminates For Material Coatings

Chances are, if you hold future electronic components up to your ear, you won't hear the ocean's roar. But, a new process that mimics the structure of common, ordinary seashells could lead to stronger material coatings that will improve the durability of those components.

Researchers have sought better material coatings for years, primarily because such laminates would enhance a wide range of applications, including automotive and electronic component finishes, and optical lenses. One effort that's bearing fruit is jointly sponsored and conducted by the National Science Foundation's Center for Microengineered Materials at the University of New Mexico (UNM), Albuquerque, and Sandia National Laboratories, Albuquerque, N.M.

The two concerned have devised a rapid and efficient way to self-assemble diverse materials into coatings that imitate the structure of seashells. While, at first glance, the creation of a laminate based on a seashell model might seem odd, the reality is that seashells are known for their strength, hardness, and ruggedness. Key to the improved properties of these laminates is the use of alternating layers of flexible, cushioning biopolymers, with hard layers of calcium carbonate. Historically, scientists have struggled to find the secret of easily accreting these very-thin laminates.

An interesting feature of the seashell design is its ability to stop cracks in their tracks, thanks to a high tolerance to fractures. When a crack does begin, for example, it is immediately intercepted by a polymer layer. As a result, the crack requires more energy before it can propagate through succeeding calcium carbonate layers.

The new process isn't just based on the seashell model; it uses a scientific property known as the micelle. A micelle is a spherical molecular assembly that spontaneously forms when two-sided detergent molecules composed of hydrophilic (water-loving) and hydrophobic (water-hating) portions come together. In water, micelles arrange themselves so that the water-loving part of the detergent is in contact with water, while the water-hating, hydrophobic part is shielded in the micellar interior.

Similarly, in the composite process, micelles separate and organize inorganic molecules around their hydrophilic exterior, and organic molecules within the hydrophobic interiors. During the coating process, the intentional evaporation of water further arranges the micelles into alternating layers of organic and inorganic molecules. Then, using a low-temperature heat treatment, the organic and inorganic layers are polymerized and their bonds interfaced.

The newly formed coatings are not only optically transparent, but more than twice as hard as the same materials mixed randomly. Other nanocomposite assembly processes involve tedious, sequential deposition of individual organic and inorganic layers that result in only layered construction. In contrast, the new UNM and Sandia process takes only a few seconds, and can easily be modified to achieve 1-, 2-, or 3-dimensional connectivity of the reinforcing polymer phase.

For additional information on this ongoing research into developing stronger laminates see Sandia National Laboratories' web site at www.sandia.gov.

Cheryl Ajluni

"Loophole" In Shannon's Theory Speeds Up Wireless Communications

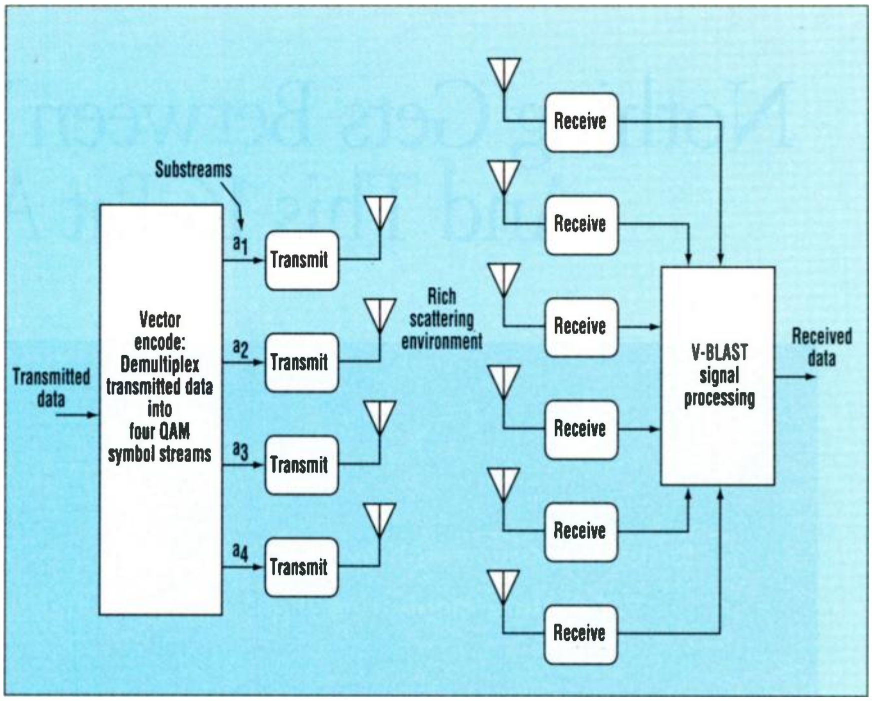
Radio waves tend to bounce and scatter wildly off objects between the transmitter and receiver. As a result, multiple copies or "images" of the signal are received at slightly different times. Researchers have labored long and hard to come up with better ways to mitigate the effects of this "multipath" interference. A team at Lucent Technologies' Bell Labs, Murray Hill, N.J., however, took a different tack. Instead of trying to eliminate the effects of multipath interference, the scientists developed a way to exploit them. In doing so, the team managed to shatter the limits sets by a 50-year-old theory on information-carrying capacity.

Known as Bell Labs Layered Space-Time (BLAST), the new wireless technique may boost the capacity of certain wireless links 10 to 20 times, according to its developers. The inspiration for BLAST can be traced to a challenge from Rich Gitlin, chief technical officer and data networking technology vice president in Lucent's Data Networking Systems business unit. Gitlin asked the researchers to take a

fresh look at an important mathematical principle, known simply as Shannon's Theory, which was originally developed at Bell Labs in 1948.

Rising to the challenge, Bell Labs scientist Gerard Foschini developed a novel interpretation of Claude L. Shannon's "Information Theory" capacity formulas. While Shannon's Theory dealt with point-to-point communications, the theory used in BLAST relies on "volume-to-volume" communications, which effectively gives the Information Theory a third, or spatial, dimension besides frequency and time. This added dimension, says Foschini, is important because "when and where noise and interference turn out to be severe, each bit [of data] is well prepared to weather such impairments." The end result is a multiple-antenna transmission system that uses new signal-processing techniques to take advantage of multipath, and put much more information in the same bandwidth.

Because multipath images arrive at slightly different times, they can in-



The Bell Labs Layered Space-Time (BLAST) architecture breaks a datastream into multiple substreams, and sends each to one of several transmitters operating at the same frequency. A multi-antenna receiver array uses each stream's unique multipath characteristics to extract the data. All of the substreams are transmitted in the same frequency band.

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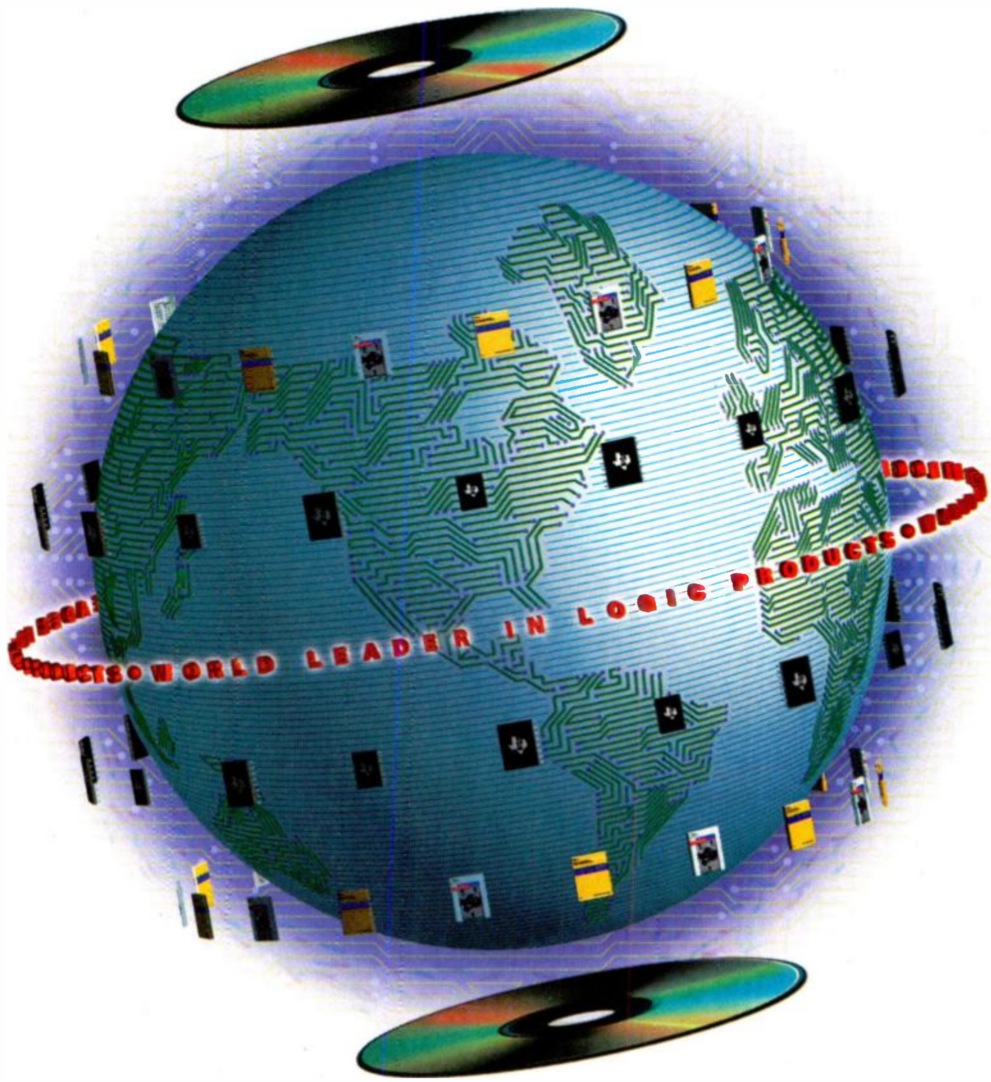

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terfere destructively, effectively canceling each other out. But the BLAST approach makes the most of multipath. It uses the scattering characteristics of the propagation environment to enhance, rather than degrade, transmission accuracy by treating the multiplicity of scattering paths as separate, parallel subchannels.

BLAST accomplishes this by splitting a single user's data stream into multiple substreams. It also uses an array of transmitter antennas to simultaneously launch the parallel substreams *(see the figure)*. All of the substreams are transmitted in the same frequency band, so spectrum is used very efficiently. Because the user's data is being sent in parallel over multiple antennas, the effective transmission rate is increased roughly in proportion to the number of transmitter antennas used.

At the receiver, an array of antennas is again used to pick up the multiple transmitted substreams and their scattered images. Each receiving antenna "sees" all of the transmitted substreams superimposed, not separately. However, if the multipath scattering is sufficient, then the substreams are all scattered differently, since they originate from different transmit antennas located at slightly different points in space.

Using sophisticated signal processing, these differences in the scattering of the substreams allow them to be identified and recovered. In effect, the unavoidable multipath in wireless communication offers a very useful spatial parallelism that can boost bit rates.

The signal-processing algorithms used at the receiver are the heart of BLAST. At the bank of receiving antennas, high-speed signal processors look at all the signals from all the antennas at once. They first extract the strongest substream from the morass, then proceed with the remaining weaker signals, which are easier to recover once the stronger signals have been removed as a source of interference.

Under the widely used assumption of independent Rayleigh scattering, the theoretical capacity of the BLAST architecture grows roughly linearly with the number of antennas, even when the total transmitted power is held constant. In the real world, scattering will be less favorable than the independent, Rayleigh distributed assumption. It remains to be seen how much capacity is actually available in various propagation environments.

Even in relatively poor scattering environments, BLAST should provide significantly higher capacities than conventional architectures. A laboratory prototype has demonstrated spectral efficiencies of 20 to 40 bits/s/Hz of bandwidth, numbers that are unattainable using standard techniques. The prototype uses eight transmit and 12 receive antennas. During its first weeks of operation, it achieved wireless capacities of at least 10↔ the capacity of today's fixed wireless-loop systems, which provide phone service in rural and remote areas.

Under ideal operation in a Rayleigh propagation environment, at a signal-to-noise ratio of 18 dB, using 12 transmit antennas and 16 receive antennas, and assuming no other impairments, a simplified, easily implemented version of the BLAST technique can achieve a theoretical spectral efficiency of 36 bits/s/Hz, as compared to the full-blown BLAST ideal of 71 bits/s/Hz. Actual results will be significantly lower than 36 bits/s/Hz, due to non-ideal scattering and the presence of numerous practical impairments.

The capacity increase afforded by BLAST technology may eventually allow fixed wireless technology to rival the capabilities of today's wired networks, while providing faster and more cost-effective deployment. One potential application would be in businesses, where wires would no longer be necessary to transmit data between desktop computers, notebook computers, and handheld devices. Another possible use is in providing phone service to remote and rural areas, where wireless networks would connect homes and businesses to copper-wired public telephone service providers.

The BLAST technology does, however, have its limitations. It is not well-suited for mobile wireless applications, such as handheld and car-based cellular phones, because multiple antennas, both transmitting and receiving, are needed. In addition, tracking signal changes in mobile applications would dramatically increase the computational complexity of the system.

Remarkably, the initial BLAST experiment designed by researchers Glenn Golden and Peter Wolniansky, did not use the technology of error-correction coding to correct signal errors. The transmitter also lacked prior knowledge of which signal components would propagate easily, and which would be severely impaired.

The research performed by team member Michael Gans includes the determination of optimal placement and number of transmitting and receiving antennas. If, for instance, the distances between antennas on each end were further reduced, the number of potential applications, such as mobile communications, might increase. In addition, researchers are trying to increase capacity even further, and are exploring how to enhance BLAST for all wireless formats.

"This new technology represents an opportunity for future wireless systems of extraordinary communications efficiency," said Reinaldo Valenzuela, who heads the BLAST research team. The team is excited that this experiment is only the first step in the development of higher-capacity RF systems.

Technical information about BLAST can be found at www.bell-labs.com/news/1998/september. More information is available at www.bell-labs.com/projects/blast. Also, see Gerard J. Foschini's, "Layered Space-Time Architecture for Wireless Communication in a Fading Environment when Using Multiple Antennas," *Bell Labs Technical Journal*, Volume 1, Number 2, Autumn 1996, pp 41-59; or go to: www.lucent.com/ideas2/perspectives/bltj/autumn_96/paper04/main.html. For more information on Claude Shannon's Information Theory, see www.lucent.com/informationtheory.

Lee Goldberg

Controller Eyes AC Induction Motors In Consumer Applications

ASIC Chip Incorporates 8-bit RISC Core And Associated Firmware To Precisely Control Single-Phase Motors.

Ashok Bindra

COVER FEATURE

Ac motors are everywhere, dominating the overall marketplace. Yet, their design complicates speed-control functions. Variable-speed designs only add to this problem. As a result, control solutions for variable-speed ac motors have grown pricier than their dc counterparts.

Controllers for single-phase, variable-speed ac motors cost approximately three times more than their dc versions. Controllers for three-phase ac motors can be six times more expensive—or higher. Although analog triacs provide a low-cost solution for variable ac induction motors, they're imprecise, inefficient, and noisy. Plus, they're unsuitable for manufacturers seeking to comply with the IEC-61000-3-2 harmonic standard.

Programmable fixed-point DSP-based digital-control solutions recently emerged to address the woes of motor control. But, the majority of these solutions are targeted at brushless dc, switched reluctance, and three-phase ac induction motors in which a sufficient amount of computational power is needed. The solutions are based on reference designs supplied by DSP vendors. Moreover, the programmable, fixed-point DSP chips involved aren't as inexpensive as microcontrollers. Nevertheless, major DSP suppliers like Texas Instruments Inc., Dallas, Texas, and Analog Devices Inc., Norwood, Mass., continually push the price point downward for motor-control applications. Recent announcements indicate prices falling below $3.00, in volume quantites.

8-Bit Controller

For low-cost motor-control applications, 8-bit microcontrollers—the workhorses of embedded applications—dominate and sell for under a dollar in volume quantities. Anacon Systems Inc. decided to exploit its proprietary 8-bit RISC microcontroller design and motor-control algorithm. By adding the right amount of optimized peripherals and memory around its proprietary 8-bit RISC core, it crafted an ASIC controller chip for low-cost, single-phase ac induction motor-control applications (*Fig. 1*). Target applications include those used in various consumer appliances , HVAC, pumps and compressors, health and medical equipments, as well as automotive.

The company's next step was to employ in-house system-level design experts. Their mission would be to create board-level turnkey solutions for single- and three-phase ac induction motors. "We offer a total solution that includes all the hardware and software required for controlling an ac induction motor," states Anacon Systems' president and CEO, Bala Padmakumar. According to the company, their controller solution provides low-cost, high-efficiency, silent operation for ac induction motor control, matching the functionality and characteristics of brushless dc motors. "What differentiates us from the chip vendors is that we come to the market with system-level knowledge and expertise," notes Zahid Ansari, vice president of operations at Anacon Systems. " In many applications, all the motor manufacturer has to do is simply add the controller card or module to its motor, and it is in busi-

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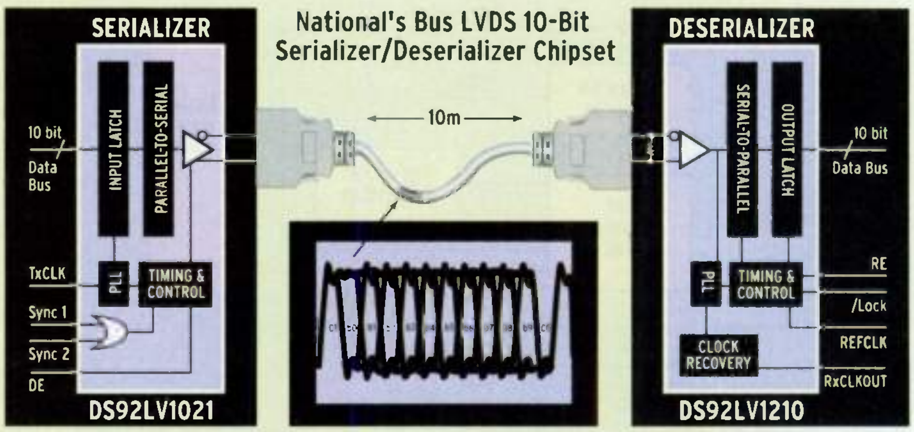

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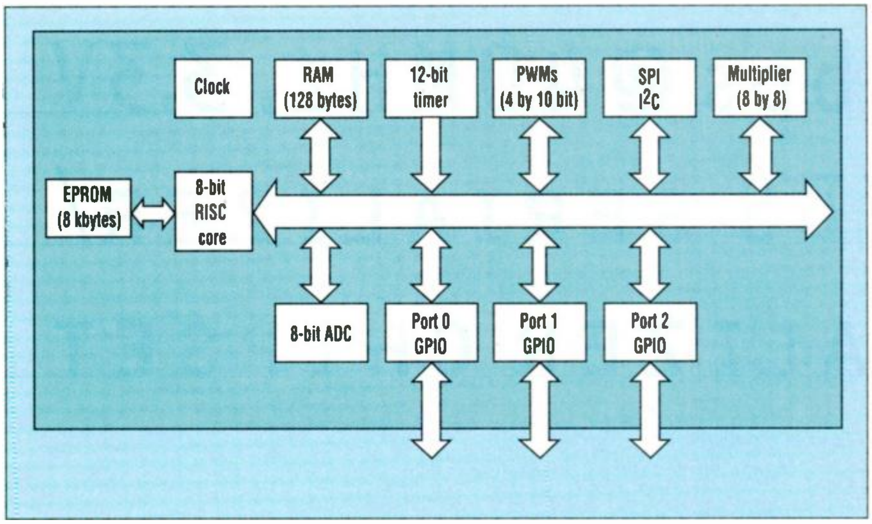
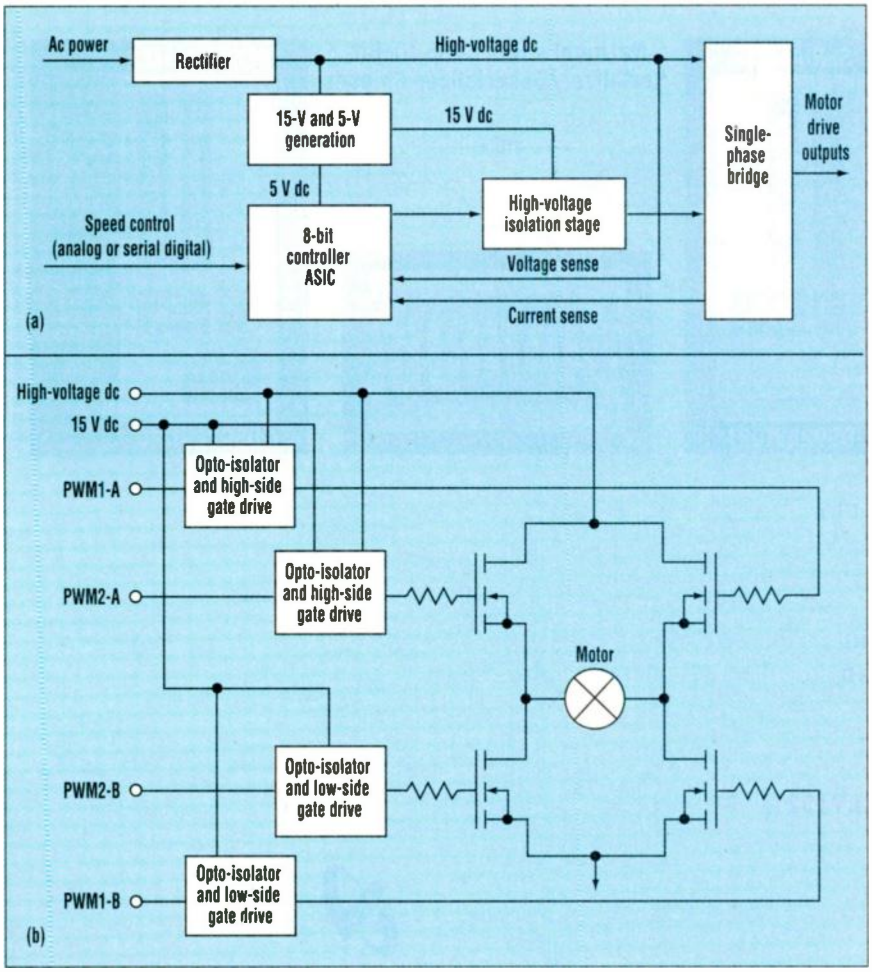


1. This ASIC controller chip from Anacon Systems, specifically optimized for single-phase ac induction motor control, incorporates an 8-bit RISC core licensed from Cypress Semiconductor. It's implemented in Cypress Semiconductor's advanced 0.6-µm double-polysilicon, double-metal CMOS process with non-volatile embedded EPROM capability.



2. This block diagram shows all the key functions on Anacon Systems' controller board for variable-speed control of single-phase ac induction motors (a). The design implements an optoisolation technique to isolate low-voltage components from the high-voltage power stage (b). The PWM-A and PWM-B outputs are complementary and non-overlapping, ensuring that pull-up and pull-down states aren't on simultaneously.

ness," he adds.

Using the proprietary ASIC controller chip, Anacon Systems has developed complete pc boards, including software, for variable-speed ac induction motors. While the initial introduction, the VSAC1000, is aimed at single-phase applications, next year should see the VSAC3000 three-phase solution. As long as the power constraints are met, the VSAC3000 family will be capable of driving three-phase motors using a single-phase ac supply input.

The company expects to sample the system-level VSAC3000 by the first quarter of 1999, with production slated for the second quarter. A high-performance RISC core for the three-phase application is under development, according to Anacon System's vice president of marketing, Charles F. Bellavia. "We're evaluating both 16- and 32-bit RISC architectures for this application," states Bellavia. According to the company, that decision will be made by the time this article goes to print. Padmakumar explains, "This decision will be market driven, and not engineering driven." Interestingly, Padmakumar sees the 16-bit control solution in no mans land He then adds, "To access every high-end application, we're moving toward a 32-bit RISC architecture."

Turnkey Solution

The ASIC controller used in the VSAC1000 is based on an 8-bitRISC core licensed from Cypress Semiconductor, San Jose, Calif. Cypress Semiconductor also will serve as foundry for AnaCon Systems' 8-bit optimized controller chip. This motor control chip is implemented in an advanced 0.6-µm double-polysilicon, double-metal CMOS process with non-volatile embedded EPROM capability.

The chip consists of the microcontroller core, a 8k-by-8-bit EPROM, and a 128-by-8-bit SRAM. It's also got an 8-by-8-bit multiplier, control logic, an eight-channel 8-bit analog-to-digital converter (ADC), a 12-bit timer, four 10-bit pulse-width modulators (PWMs), and a serial interface. The chip also includes a comparator designed to monitor faults in the system and perform rapid shut-down. The die size of this chip is less than 10,000 mils^2. "Our die size is less than a third

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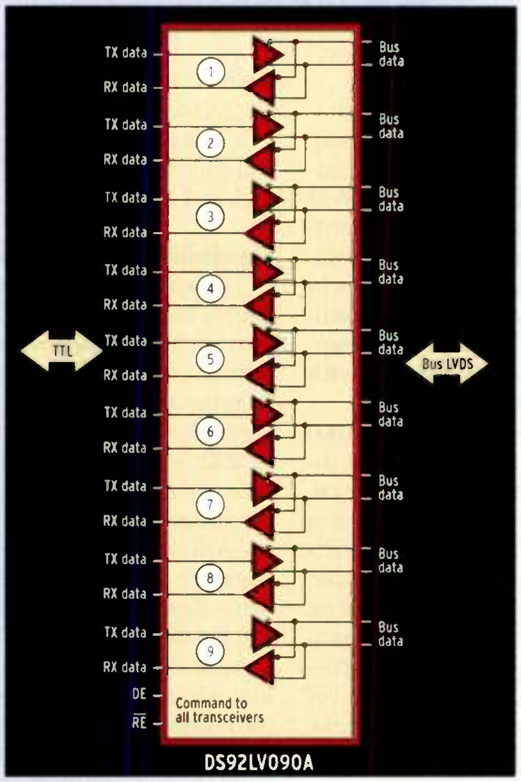
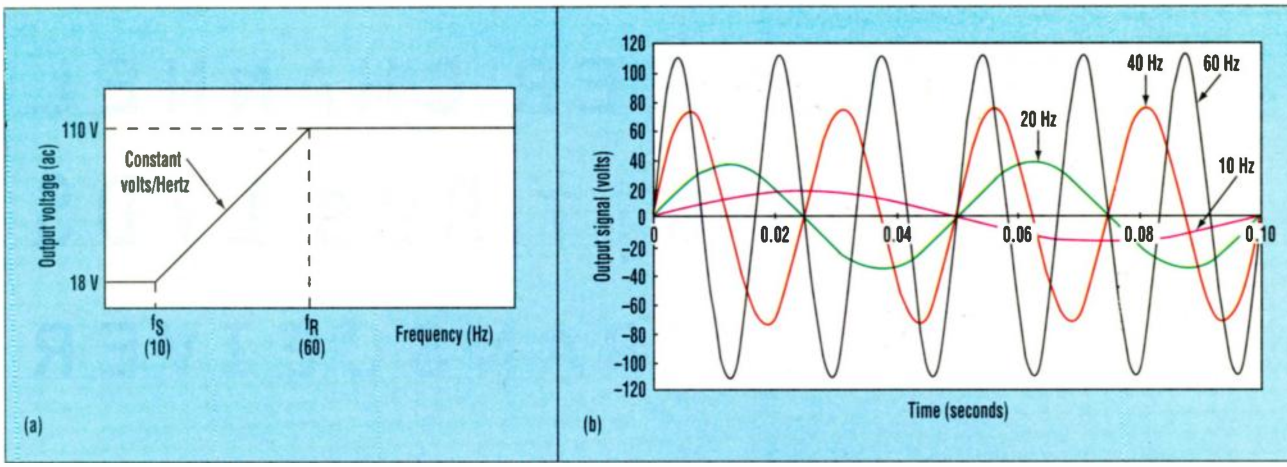


National Semiconductor



3. For optimum performance, the amplitude of the motor-drive output sinusoidal signal changes with frequency to provide a constant volts/Hertz ratio for frequencies greater than f_S and less than the motor's rated frequency f_R (a). Internal tests show that a 60-Hz output has a maximum amplitude of 110 V, while the 10-Hz signal is below 20 V (b) to keep the volts/Hertz ratio constant..

of a typical 8-bit microcontroller," notes Bellavia.

While the EPROM stores the motor-control firmware and the lookup table, the SRAM serves as general-purpose memory. The dedicated PWM state machines enable effective hardware implementation of PWM outputs, with modulation frequencies in the range of 20 kHz—beyond the audible range. The PWM outputs are complementary and non-overlapping with a programmable dead time.

As for Anacon Systems' VSAC1000 variable-speed controller card, it includes the rectifier for ac-dc conversion, , a regulated dc-dc voltage converter, a high-voltage isolation circuit, high-voltage power source for driving the motor, and an 8-bit RISC-based ASIC control chip. The output power electronics provides appropriate voltage and frequency for variable-speed control of fractional-horsepower ac induction motors (*Fig. 2*). Designed to handle up to 1/3-horsepower motors, versions of the controller card are available for ac and dc inputs. Ac input models accept 80-125 V ac, 50/ 60 Hz. Dc versions, designed for battery-based systems, operate from 12 to 48 V dc.

The controller card is targeted at consumer appliances such as white goods and range hoods, heating, ventilation, and air conditioning (HVAC), and exercise equipment like treadmills. The company also is developing other inputs to enable the controller boards to operate in regions like Europe and Asia. A version with a 184-265 V 50/60-Hz ac input range, as well as one with a universal input, are planned for early next year . As a result, Anacon Systems' will offer a portfolio of motor controller products that will support a range of power levels as high as 1 hp.

Flexibility And Customization

The variable-speed controller card allows both analog and digital speed control. The analog control takes the form of voltage in the range of 0 to 5 V, whereas the digital control is realized through a serial input that can be an RS232, 3-wire serial peripheral interface (SPI), or 2-wire I^2C bus. Using the programmed PWM outputs from the ASIC chip, the controller card synthesizes low-distortion sinusoidal drive signals at frequencies from 1 to 120 Hz for the ac motor. The low-distortion signal minimizes motor heating, while cutting losses to improve the efficiency of the design.

To isolate the low-voltage devices from the high-voltage sector, the design implements optoisolators. Other features include constant programmable volts/Hertz excitation of the motor up to the rated speed, third-harmonic injection to improve motor efficiency, and soft-start and safety shutdown capabilities.

The controller maintains a constant volts/Hertz between the starting frequency (f_S) and the rated frequency (f_R) of the motor to prevent the iron core of the motor from saturating (*Fig.3*). Below f_S, the starting voltage characteristics is customized to a minimum value to ensure the starting torque. The controller keeps the output voltage constant beyond the rated frequency of the motor.

Although the VSAC1000 is a standard controller card, it offers flexibility for customization. For example, the algorithm can be optimized for specific markets that need special features. The pc-board also can be built to custom form factors so that it fits inside the desired motor case. Depending on the motor's requirements, the output wave shape can be modified by changing the values in the lookup table. Some applications need this variation to optimize the rms voltage of a given output signal, enhancing the performance of the motor. Filtering and power-factor correction (PFC) also could be added for applications requiring such features.

In short, Anacon Systems brings a novel turnkey control solution to the low-power, single-phase ac induction market as it slowly transitions to variable-speed digital control. Efforts are in progress to extend this capability to three-phase applications. The startup's roadmap also points to solutions that can handle power levels as high as 2 hp.

Price And Availability

The variable-speed controller card for single-phase ac induction motors is available with both ac and dc inputs. The ac input VSAC1000 is priced at $20.00 in quantities of 100,000. Single unit price for the evaluation board is $149.00. A complete reference design with evaluation card costs $199.00.

Anacon Systems Inc., 1043 Shoreline Blvd. Suite 202, Mountain View, CA 94043; (650) 934-3355; www.anaconsystems.com.

CIRCLE 519

Current-Feedback Op Amps Set New Performance Goals

With Very-Low Quiescent Currents, These Amplifiers Promise Higher Slew Rates And Wider Bandwidths From Smaller Packages.

Ashok Bindra

Slowly but steadily, operational amplifiers continue to advance on all fronts. More bells and whistles are being added to these ubiquitous devices, as processes and circuit techniques improve. As a result, semiconductor manufacturers continue to bring specialized, as well as general-purpose, op amps in miniaturized packages with enhanced ac and dc specifications, into the market. All are aimed at improving current designs, while addressing the requirements of a myriad of emerging architectures.

SPECIAL REPORT

The need for high-speed, wideband, low-noise op amps in communications, imaging, and high-quality video applications is forcing designers to tap the virtues of current-feedback topologies. Lately, several key players have tweaked current-feedback op amps, while exploiting improvements in complementary bipolar and biCMOS technologies. They're doing this in order to deliver a variety of amplifiers for driving xDSL lines, switching high-speed video signals, amplifying RF and IF signals, as well as buffering high-resolution analog-to-digital and digital-to-analog converters (ADCs and DACs).

Art Courtesy: Burr-Brown Corp.

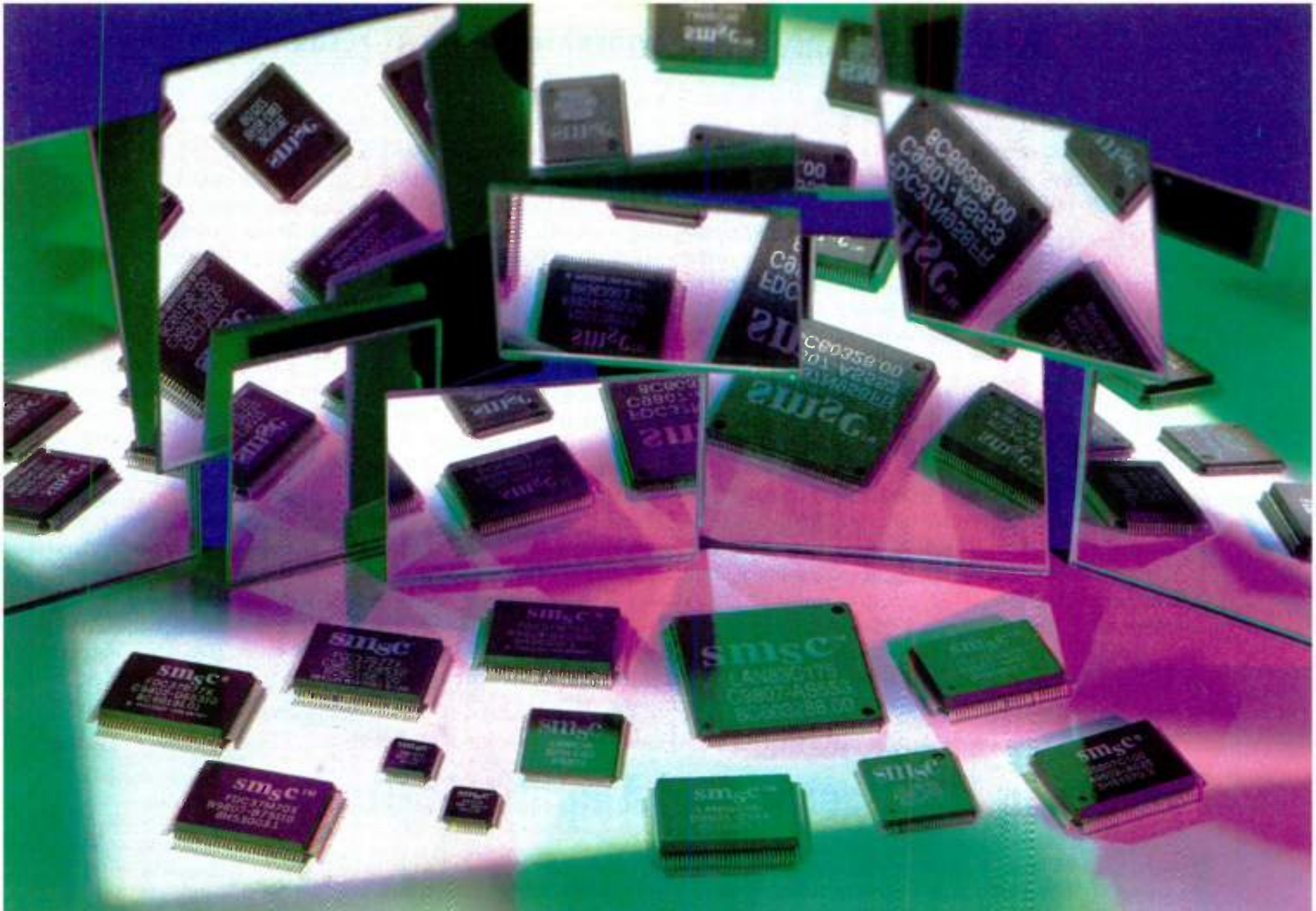
Bandwidth And Slew Rate

Hoping to serve the needs of high-speed video systems, Texas Instruments Inc. (TI) has combined its high-voltage, complementary-bipolar (HVbiCOM) process with dielectric-isolation (DI) techniques. This process ensures high isolation and fast transient response with very-low distortion. The result is the newest current-feedback op amp with an extraordinarily fast slew rate *(Fig. 1)*. TI believes that the THS3001's 6500-V/µs slew rate, its 420-MHz bandwidth, and low distortion of -96 dB is unmatched. In addition, it maintains a 0.1-dB gain flatness to a bandwidth of 115 MHz, and offers low, 0.01% differential gain and 0.02Υ differential phase errors. All of these features make the amplifier well suited for other applications as well, such as wireless base stations, and ultra-fast ADC or DAC buffers.

Though the slew-rate figure looks attractive, the manufacturer's application note cautions that this performance can be affected by internal and external factors to the amplifier (*Fig. 2*). For example, the THS3001's configuration as an inverting or non-inverting amplifier can impact the output slew rate. Data-sheet results indicate that the slew rate is faster in the inverting mode than in the non-inverting configuration. Also, pc-board parasitic capacitance on the input nodes degrades the transient response further because there is now more capacitance to charge. Likewise, lowering the supply voltage to the chip lowers this rate, as there is less current available to charge the input capacitance.

Although this op amp incorporates output current-limiting protection, it does not offer thermal shutdown protection. This warrants special attention concerning power dissipation, even though the amplifier comes in a thermally enhanced, 8-pin SOIC package. "The THS3001 is one of the fastest 30-V amplifiers," says Jim Quarfoot, TI's senior member of the technical staff for Advanced Analog Products.

"The process impacts the performance of the amplifier, as the parasitics have been minimized due to dielectric isolation. The current-feedback topology affords users the ability to control the amplifier



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gain independently of the bandwidth—a major advantage over conventional voltage-feedback counterparts," he says. "Therefore," Quarfoot continues, "once the desired frequency is ascertained for the given application, the user can simply adjust the gain resistor to increase or decrease overall amplifier gain."

While the THS3001 is a general-purpose device, TI has also developed amplifiers specifically intended to drive ADSL lines. Two such recent introductions are the THS6012 and THS6022. These op amps are crafted to deliver high output drive at high speeds and low distortion. The THS6012 is targeted at central-office ADSL equipment, and the THS6022 is designed for ADSL modems in PCs. Both the ADSL differential line drivers offer low distortion of -72 dB at 1 MHz, over low-impedance telephone lines. In addition, they feature a 140-MHz bandwidth at a slew rate of 1000 V/µs. Each unit contains two high-speed amplifiers to drive differential lines. While the THS6012's typical output drive capability for each amplifier is 500 mA, the THS6022 delivers 250 mA per driver.

To minimize crosstalk, these amplifiers incorporate independent power-supply connections. Also, the units are designed to operate over a wide range of power-supply voltages, ranging from ±4.5 to ±16 V. Both come in TI's thermally enhanced PowerPAD packages. Sampling now, the high-speed current-feedback amplifiers are expected to go into production later in this quarter.

Low Supply Current

"These devices are well suited for applications demanding wide bandwidth, high slew rate and low distortion at low supply current," confirms Michael Steffes, strategic marketing manager at Burr-Brown Corp. Plus, he adds, the ac performance (bandwidth and distortion) of current-feedback op amps is independent of signal gain. Subsequently, the current-feedback topology provides a nearly constant bandwidth as a signal is increased.

In order to drive xDSL lines, Burr-Brown engineers are readying these parts with more output-power capability. A good example is the recently introduced OPA681. A revised output stage provides high output current with minimal headroom and crossover distortion. "The current-feedback OPA681 provides all these attractive features using single-supply operation," notes Steffes. "Using a single +5-V supply,

Presetting The Operational Amplifier's Gain

Fixed-gain op amps are not new. But, 27 standard-gain values covering the range from 1 to 100, with accuracy within 0.1% (typical) over the full temperature range is unheard of. And, Maxim Integrated Products has embarked on this route to make the designer's job easy. Another manufacturer adding spice to the otherwise unexciting op amp is Xicor Inc. Employing its smart-analog technology, Xicor has combined analog, digital, and non-volatile memory functions on the same die to produce programmable op amps. Xicor's product line manager Bob Anderson believes that it initiates a new category of op amp previously unavailable. The programmable capability will enable engineers to add features such as self-calibration and self-testing, he adds.

Packing a general-purpose op amp and precision gain-setting resistors on the same die, Maxim has cranked out a new line of op amps called Gain-Amps. The newest Gain-Amp family, the MAX4174/4175/4274/4275, offers 27 different R_F/R_G, factory-trimmed resistor settings for inverting and non-inverting amplifier gains ranging from 0.25 to 100. To save additional external components, some members of the Gain-Amp family offer $V_{CC}/2$ bias resistors at the non-inverting input. Besides shrinking the real estate, the on-chip resistors also trim the overall gain error, as the drift in the R_F to R_G ratio over the specified temperature range is lower than 0.1%. This translates into overall gain error of no more than 0.5% maximum over the temperature range of –40°C to +85°C.

According to the manufacturer, the Gain-Amps improve gain accuracy and lower power, because the op amp is compensated at the factory for the required gain-bandwidth product. All the devices will feature a useable bandwidth greater than 100 kHz, and gain-bandwidth product greater than 1.25 MHz. For a gain of 100V/V, the Gain-Amp offers a 20-MHz gain-bandwidth product for a supply current of only 325 µA. The key to this performance is a proprietary two-stage design (patent pending) that overcomes open-loop gain fluctuations of rail-to-rail amplifiers. Unlike conventional op amps, it provides internal circuitry that compensates for the loading effects of the output.

Additionally, this family also features single 2.5- to 5.5-V operation, a rail-to-rail output stage, an input common-mode range that includes ground, ±17-V input fault protection, and capacitive load driving beyond 250 pF. The Gain-Amps come as singles in 5-pin SOT23 or duals in 8-pin µMAX packages. Sampling now, the Gain-Amp op amps are slated for production later in this quarter.

To bring programmability to such components, Xicor's X943X family integrates two digitally controlled potentiometers and two voltage op amps, with 16 bytes of EEPROM on the same die. Each potentiometer is a resistor array of 63 elements and four non-volatile data registers to store four distinct wiper positions. Plus, it includes a wiper counter register (WCR) that controls the position of the wiper on the resistor array.

The WCR can be written directly or changed by transferring the contents of one of the four data registers. Similarly, each amplifier is associated with four data registers and an analog control register to control offset voltage and power modes of the amplifier. Consequently, the X943X op amps can be programmed by an 8- or 16-bit microcontroller via a serial interface like SPI or I^2C. While the X9430 provides the SPI interface, the X9438 offers a two-wire I^2C interface. The programmable op amps come in 24-pin TSSOP and SOIC packages. Sampling now, the X943X devices are expected to go into production next month.

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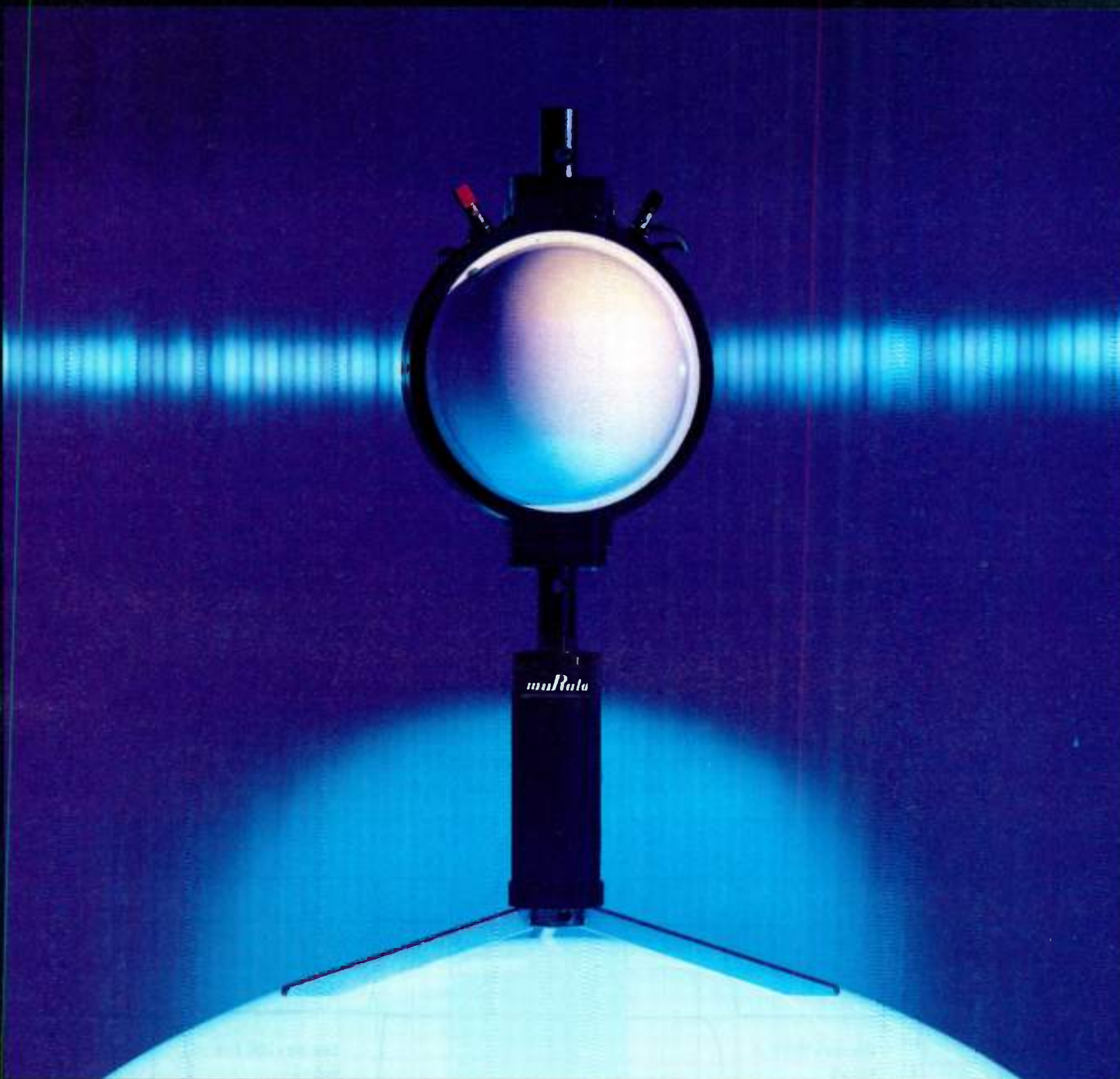

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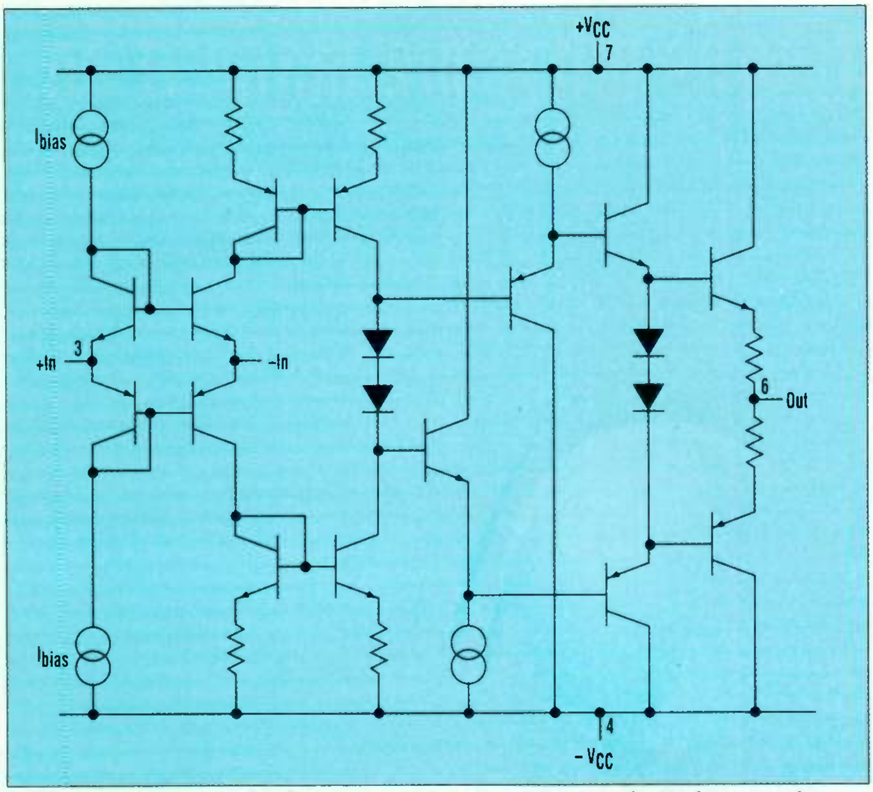


1. This figure shows a simplified schematic of TI's high-speed, current-feedback op amp, the THS3001. It's implemented in the company's 30-V, complementary bipolar process, the HVBiCom, with dielectric isolation to obtain high bandwidth and fast slew rates.

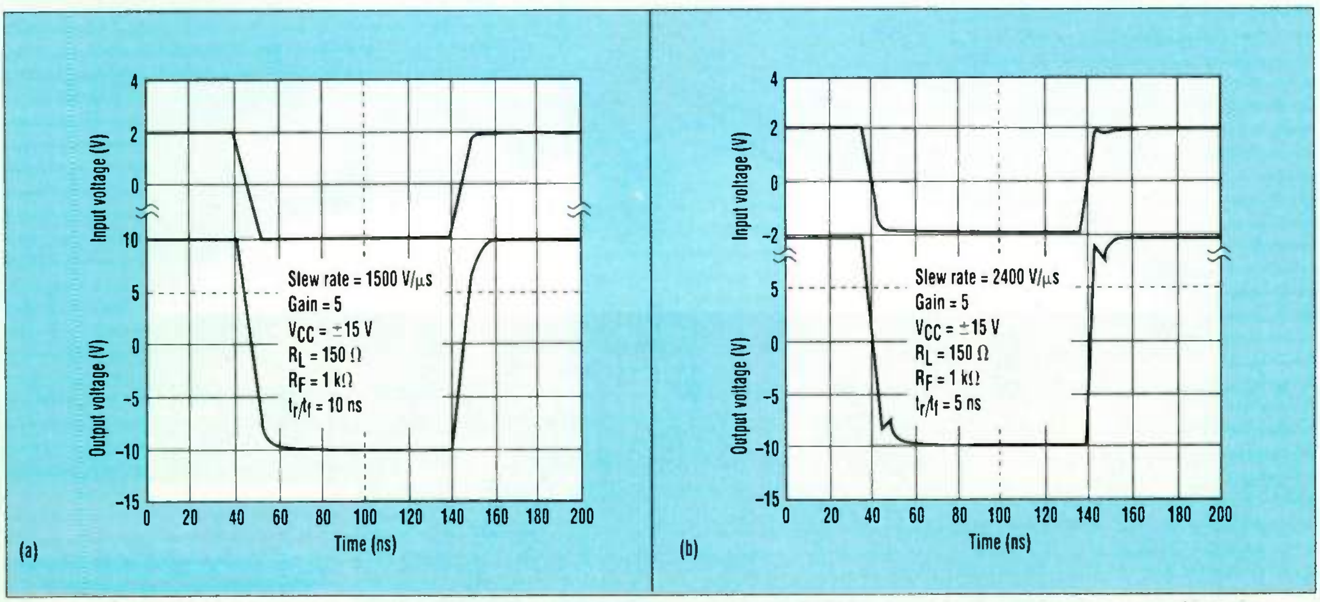
the unit can deliver a 1- to 4-V output swing with 100 mA of drive current, and a 150-MHz bandwidth. Earlier designs have suffered from poor crossover distortion as the output current goes through zero," he says.

The op amp also offers an optional disable-control pin for power savings or multiplexing circuits. For normal operation, this pin is left open or held high. When pulled low, amplifier supply current drops below 200 μA, and the output goes into a high-impedance state.

For driving xDSL lines, a dual version is offered, the OPA2681. It can provide the required upstream ADSL full-line power using a 1:2 step-up transformer and a single +12-V supply (*Fig. 3*). The OPA2681 comes in both SO-8 and SO-14 packages. However, only the 14-pin SO offers the disable-control pin for the dual version. Meanwhile, for applications like wideband RGB line drivers and wideband instrumentation amplifiers, Burr-Brown has packed three 681s in single, 16-pin SSOP and SOIC packages. The triple version is designated OPA3681.

There are many other applications that require broadband, fixed-gain buffer amplifiers. To that end, Burr-Brown has readied the OPA682. Depending on the external connections, the internal resistor network of the current-feedback OPA682 can be used to provide a gain of 2, 1, or –1. According to the manufacturer, the specifications for OPA682 are slightly better than the OPA681's at a gain of 2. Consequently, the 682 offers a bandwidth of about 350 MHz at a gain of 2. By comparison, the OPA681 is rated to provide bandwidth of 225 MHz at a gain of 2. It comes in 8-pin SO and 6-pin SOT-23 packages.

To attain performance from its current-feedback line, Burr-Brown manufactures its op amps on a complementary bipolar process. The company's



2. Several factors, both internal and external, influence the output performance of TI's THS3001 op amp. As shown, for slew rates of less than 1500 V/ms, the output waveform is clean as it transitions between initial and final voltages (a). For slew rates greater than 1500 V/μs, the output waveform shows an aberration due to the brief saturation of the internal current mirrors (b).

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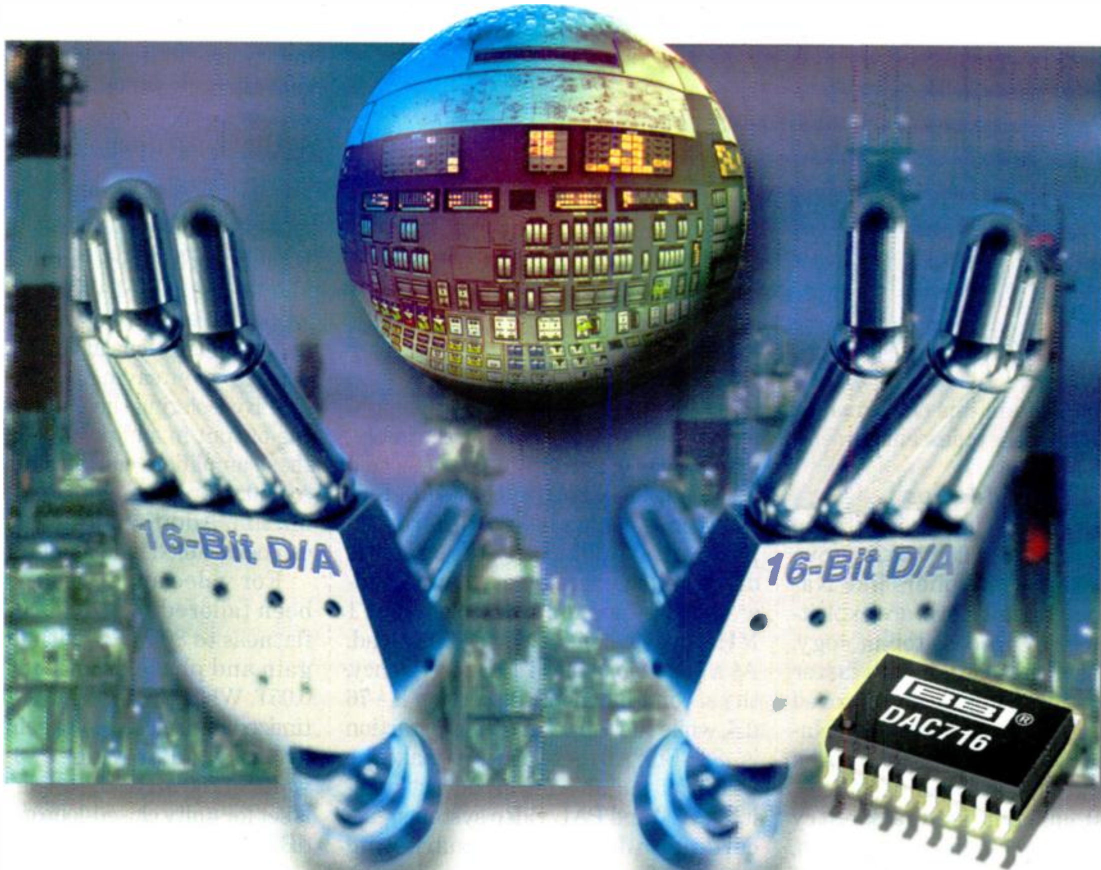

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COMPARING NPN AND PNP CHARACTERISTICS FOR ANALOG DEVICES' CURRENT AND FUTURE CB PROCESSES

NPN	XFCB 1.0 (current)	XFCB 1.5 (future)	PNP	XFCB 1.0 (current)	XFCB 1.5 (future)
Beta	103	130	Beta	70	80
V_A (V)	100	80	V_A (V)	20	20
$\beta \bullet V_A$ (V)	10,300	10,400	$\beta \bullet V_A$ (V)	1,275	1600
BV_{CEO} (V)	>12 (15)	>8	BV_{CEO} (V)	>14 (16)	>8
$f_T$peak (V_{CE}) (GHz)	4.0 (2 V)	8.0 (2 V)	$f_T$peak (V_{CE}) (GHz)	3.0 (2 V)	5.0 (2 V)
I_{fT}peak (mA)	0.3	.3	I_{fT}peak (mA)	0.15	0.15
R_B (Ω)	732	750	R_B (Ω)	399	350
C_{JE} (fF)	12.4	3.8	C_{JE} (fF)	12.1	4.1
C_{JC} (fF)	17	7.4	C_{JC} (fF)	19	8.5
C_{JS} (fF)	16	6.3	C_{JS} (fF)	16	6.3

thrust is to maintain this performance while decreasing the quiescent current.

Enable/Disable Modes

There isn't much one can do with the current-feedback topology to improve performance. So, suppliers like National Semiconductor Corp. are exploiting advances in process technology. Coupling trench isolation with faster pnp and npn transistors in an improved complementary bipolar process, National has cranked out a faster version without any cost and power penalties.

Newest current-feedback entry from National's Comlinear products, the CLC5665, provides a slew rate of 1800 V/µs, with a 90-MHz unity-gain bandwidth. Plus, it offers a fast output-disable function. The output disable changes the output from a low- to a high-impedance state, and reduces power wastage. It takes about 200 ns for the amplifier to switch to the high-output-impedance state. Furthermore, it features 0.1-dB gain flatness to a bandwidth of 20 MHz, 0.05% differential gain error, and 0.05Υ differential phase error. Additionally, the op amp is designed to generate very-low second- and third-harmonic distortion at 1 MHz, even when driving a 100-Ω load. At a 100-Ω load and 1 MHz frequency, the second-harmonic distortion is –76 dB, while the third-harmonic distortion is –82 dBc. "All these features make the CLC5665 suitable for broadcast-quality NTSC and PAL video systems," according to Jeff Hooker, marketing manager for National Semiconductor's Comlinear products.

Besides video applications, Comlinear is also extending its high-speed op amps to cable drivers, xDSL line drivers, and DAC buffers. In addition to speed, it has a large voltage swing (28 V p-p), and continuous output-current capability of 85 mA, needed for a variety of applications. Offered in 8-pin DIP and SOIC packages, the maximum supply voltage for the CLC5665 is ±16V. Meanwhile, process improvements are underway to lower quiescent current, while driving the supply voltage to ±5 V.

High-speed enable/disable modes are other features added to Maxim Integrated Products' wideband, low-power current-feedback amplifiers. Recent offerings have been the MAX4188 and MAX4191. These op amps are aimed at video and multiplexer applications in portable systems where power savings is the top priority. "By isolating the input, and placing the output in a high-impedance state, these amplifiers cut the supply current to 450 µA per on-chip amplifier," says Maxim. Additionally, each amplifier can be disabled independently.

For video applications, they have been tailored to provide 0.1-dB gain flatness to 80 MHz, with differential gain and phase errors of 0.03% and 0.05Υ. While the triple MAX4188 is optimized for a closed-loop gain of 6 dB or greater, and provides a -3-dB bandwidth of 200 MHz, the triple MAX4189 is set for unity closed-loop gain with a 3-dB bandwidth of 250 MHz.

The amplifiers operate from a single 5-V supply or from dual supplies in the range of ±2.25 to ±5.5 V. Each amplifier draws only 1.5 mA, and can deliver output currents of ±55 mA. Other features include low switching transients (45 mV p-p), a settling time of 22 ns to 0.1%,

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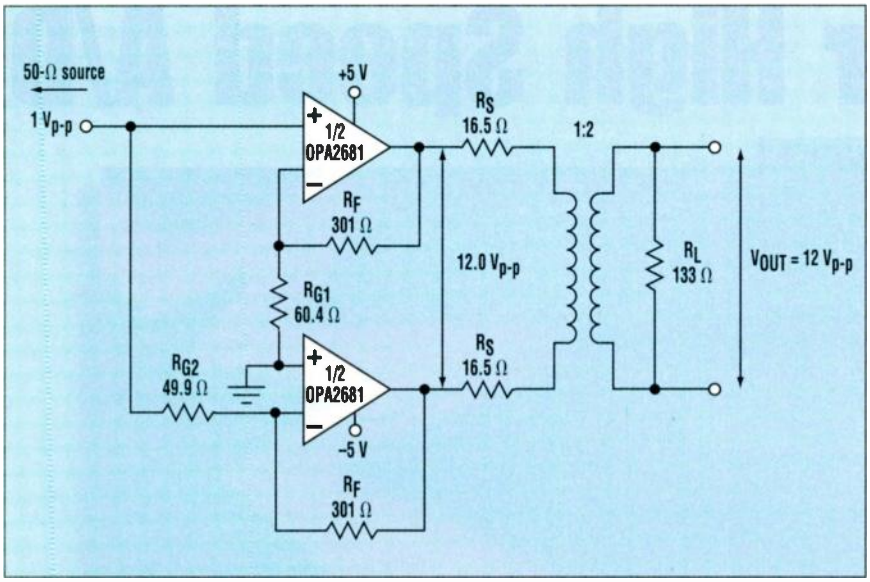


3. Burr-Brown's high-speed driver OPA2681 is a dual-wideband current-feedback amplifier that can deliver sufficient power to drive differential xDSL lines.

a slew rate of 350 V/µs, and an SFDR of –70 dB at 5 MHz. The MAX4188/89 are encased in 14-pin SO and 16-pin QSOP packages, respectively. Corresponding single versions, the MAX4190/91, come in 8-pin SO and µMAX packages, respectively.

For professional video, Maxim offers the MAX4223-28 family of current-mode amplifiers. They feature a gain-bandwidth of 1 GHz, a 0.1% gain flatness to 300 MHz, and slew rates up to 1700 V/µs. Plus, they provide a low THD of –65 dBc, and a fast settling time of 5 ns to 0.1% (*Fig. 4*). Package options for these low-power amplifiers include 6-pin SOT23s or 8-pin SOICs for the single MAX4223/24, 8-pin SOs for the dual MAX4225/27, and 10-pin µMAXs or 14-pin SOs for the dual MAX4226/4228.

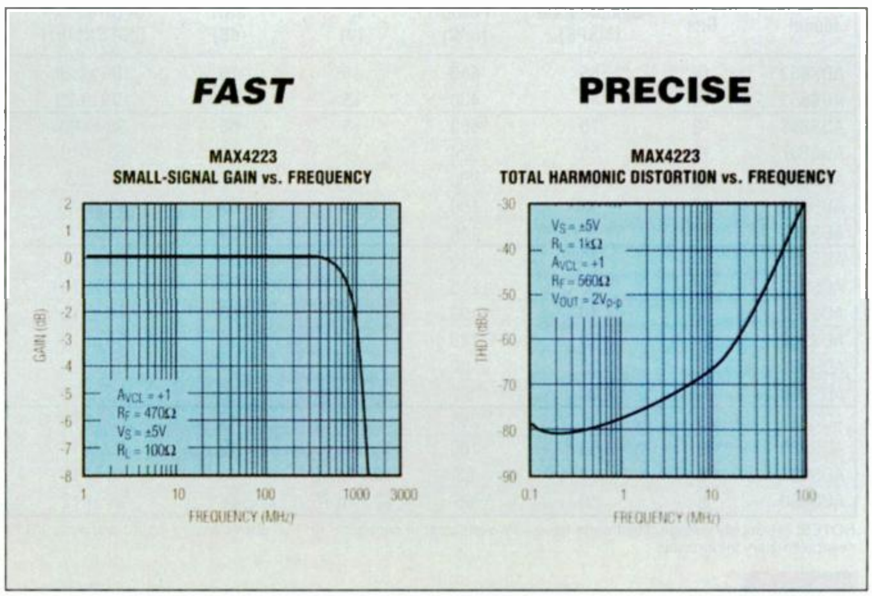
While all the current-generation amplifiers are based on Maxim's complementary bipolar process, the CB2, the manufacturer is readying an advanced version, the CB3, for future devices. "Using smaller geometries, the CB3 process is aimed at shrinking the die and package size to offer high performance at lower cost," asserts Paul Crolla, Maxim's design engineering manager. Products based on the latest CB3 pocess are planned for release in the first quarter.

Extra-Fast CB Process

To obtain very-high bandwidth and slew rates, Analog Devices has also taken the process route. Combining proprietary current-feedback topology with an extra-fast CB (XFCB 1.0) process, the company has unveiled a number of high-speed op amps intended for use in xDSL line drivers, ADC buffers, ultrasound equipment, and digital cameras. Based on the 12-V XFCB process, Analog Devices has unwrapped the AD8014, which boasts a 3-dB bandwidth of 400 MHz at unity gain, a slew rate of 4000 V/µs, and very-low noise and distortion. For all these features, the operating current required is only 1.1 mA (max) at a 5-V supply. It comes in 5-pin SOT23 and 8-pin SOIC packages.

Additionally, employing the XFCB 1.0 process, the company has also developed a low-power, high-speed dual amplifier for driving differential xDSL lines. With only 1.7 mA per amplifier supply current, the AD8012 offers a 3 dB bandwidth of 350-MHz, a 2250-V/µs slew rate, and 125-mA output-drive capability. "Low supply current translates into low current noise," states Bob Briano, Analog Device's product manager for high-speed amplifiers. Offering low distortion and voltage noise, the AD8012 comes in 8-lead SOIC and µSOIC packages.

In fact, the company's direction is to improve the output-drive capability of the high-performance amplifiers at increasingly lower quiescent or operating current. "This is critical for xDSL applications," says Analog Device's product manager for high-performance amplifiers, Ed Spence. He adds, "The efficiency of the drive amplifier is an issue in this application." Indeed, to address it, the company has enhanced its XFCB process to handle 24-V breakdowns. It means ±12-V versions with more output power and voltage swing. "We need this voltage to get better reach," explains Spence. Meanwhile, ADI's roadmap indicates



4. Aimed at professional video applications, Maxim's MAX4223 op amp provides the high speed, wide bandwidth, and low distortion and power consumption demanded by these applications. It also offers low differential gain and phase errors (0.01% and 0.02°), 0.1% gain flatness to 300 MHz, and slew rates up to 1700 V/µs.

that a very-high-speed version of XFCB process, labeled XFCB 1.5, is also in the works, with product introductions planned starting this quarter *(see the table)*. The XFCB 1.5 will offer f_T greater than 5 GHz for pnp transistors.

Implementing the high-voltage XFCB 1.0 process, Analog Devices is readying high-output-current xDSL line drivers like the AD8016. Each AD8016 amplifier can deliver a low distortion, 10-V (peak) signal on a 12-V rail, with 400 mA of output current in the power-down mode. Other highlights include a 100-MHz; a 1000-V/µs slew rate; and a 12.5-mA/amplifier (typical) supply current.

Operating from ±12-V supplies, the AD8016 consumes only 1.4 W of total dynamic power when running full-rate ADSL lines into 25 Ω. It is housed in thermally enhanced, 20-pin PSOPs and 24-pin SOICs. For single-supply operation in customer-premise equipment, the company has developed the AD8017 for delivering 10.2 V(p-p) at 200 mA output current into a 25-Ω load. It offers a 160-MHz bandwidth and a slew rate of 1500 V/µs. The quiescent current for this chip is 7 mA/amplifier. It is implemented in the XFCB 1.0 process, and comes in 8-pin SOICs.

Also in the race are Linear Technology Corp. and Elantec Semiconductor Inc. Exploiting its 5-GHz CB process, Linear Technology is ready to unveil the triple amplifier LT1399, with 500-MHz bandwidth at unity gain, and a slew rate of 1000 V/µs. Capable of delivering ±80 mA output drive current at ±2.5 V, the LT1399 is primarily aimed at RGB drivers. It is encased in 16-pin SOICs and SSOPs. Operating on ±5 V supply, the typical supply current per amplifier is 4.2 mA. Presently, this part is being fully characterized for distortion and other ac performance specifications. Single and dual versions of the high-speed op amp are also in the works.

Even as the new line of high-performance current-feedback op amps are released to address the present design issues, the push to get even more is higher. Processes are being tweaked to attain wider bandwidth, higher-speed, lower distortion, and bigger drive, while keeping the quiescent current as low as possible.

CONFERENCE PREVIEW

Embedded Systems Conference Focuses On Getting The Job Done

A Plethora Of Classes And Tutorials Cover Project Management And Solutions-Oriented Topics For Hardware And Software Designers.

Jeff Child

Is it because the conference presenters do such a good job? Perhaps it's the fact that embedded-systems technologies are growing in importance? Actually, it's because of these two factors combined that each fall, an increasing number of embedded-systems developers flock to the Embedded Systems Conference. This conference attracts both software and hardware developers looking for the tools, strategies, and hardware they need to get to market quicker—with faster and more functional embedded systems.

If there's an underlying trend among this year's conference topics, it's a focus on helping developers and engineering managers get the job done. This year's conference runs Nov. 1 through 5 at the San Jose Convention Center, San Jose, Calif. Classes run in ten parallel tracks, packing 148 classes and 12 tutorials in five days *(see the table)*.

Some classes focus on the basics, such as C and C++, real-time programming, debugging strategies, kernels, interrupt handling, project management, and real-time operating systems. Others get into advanced areas like embedded Internet, DSP development, hardware/software codesign, Java, Windows CE, and Universal Serial Bus (USB). A panel discussion, "Windows CE: Hype or Hope?," will explore the merits of that emerging operating system.

Keynote Address

The conference spotlights both a keynote address and special guest lecture. Robert X. Cringely, a Silicon Valley author and columnist, will deliver the keynote. In his talk, entitled "Jimmy Hoffa and Other Embedded Systems," Cringely discusses why the next five years will see a total upheaval in the power structure of information technology, as well as significant changes in the market leaders. Such changes, he says, are influenced by the growing importance of embedded systems. Jerry Fiddler, cofounder of Wind River, Alameda, Calif., is giving a special guest lecture entitled, "Enabling the Embedded-Systems Revolution." He'll discuss the ways in which embedded-systems developers are directly affecting an evolution toward a more intelligent world. The lecture addresses the developmental, economic, philosophical, and ethical implications of this information revolution.

Identity Crisis

Because of the overlap between various topics, categorizing those covered by the Embedded Systems Conference has grown more difficult. Identifying just where one area ends and another begins is next to futile. What's unique about embedded systems is that nearly every topic overlaps or relates to another. For example, there are strong links between project management and hardware/software codesign. With C++ and Java gaining acceptance, you can't talk about languages without talking about methodologies. Important relationships even exist between choosing a microcontroller and deciding on an RTOS/kernel strategy.

Sessions covering project management topics range from broad basics to specifics. In the "Starting Your Project With a Great Plan" workshop, the presenter illustrates how to modify your process and give control of a project's methodology to project teams. Using a case study of an embedded-product development organization, this class explains how to separate what you need to do when developing an embedded product (procedures) from how you do it (the development plan).

The tutorial, "Managing Embedded Projects," takes a management perspective. The course deals with managing schedules, dealing with difficult developers, creating and managing project specifications and expectations, forming an environment where developers will thrive, and learning from mistakes and successes. Another tutorial, " Software Estimation and Scheduling," focuses on improving the estimation process, using Gannt and PERT charts, adjusting resources, and when (and when not) to use automatic resource leveling.

In "Longer Lasting Product Designs: Cost Reductions and More Functionality are Possible," attendees get an inside look into how product design can improve "shelf life." It also describes how product redesigns can save money and the potential for streamlined designs to increase functionality (all at the same time).

Complexity Issues

Dealing with the growing complexity of embedded software is among the greatest challenges facing today's developers. Several sessions are devoted to that: "Solving the Big Problems: Architecting a Development Framework for Large-Team Software Projects" speaks directly on such issues. This class presents run-time and development methodologies that take advantage of the memory management unit (MMU). Real-life examples are provided by developers who have adapted these methodologies in their own large-team embedded projects. "Modeling Complex Behavior Simply" discusses the expressive power of a modeling language and the associated complexity reduction it offers.

Taking a solutions perspective is

1998 Embedded Systems Conference

Tutorials
Sunday, November 1
8:30 am - 5:30 pm

100 Designing Fuzzy Logic and NeuroFuzzy Applications
101 Managing Embedded Projects
102 System Design: Architectures and Archetypes
103 Stepping up to C++, Part 1
104 Real-Time Object-Oriented Modeling
105 Software Estimation & Scheduling

Tutorials
Monday, November 2
8:30 am - 5:30 pm

110 Object-Oriented Programming in Java
111 Embedded Controller Area Networking (CAN)
112 Stepping up to C++, Part 2
113 Guaranteeing Real-Time Performance using RMA
114 IrDA Infrared Communications
115 Usage-Centered Engineering for Embedded Systems

Classes
November 2
8:30 am - 10:00 am

200 Solving the Big Problems: Architecting a Development Framework for Large-Team Software Projects
201 Implementing Web-Based Management of Networked Devices
202 Incorporating Windows CE into an Embedded System from Start to Finish
203 Complex Breakpoints and Real-Time PC Trace for On-Chip System Debug

10:30 am - 12:00 pm

220 Fuzzy Logic and NeuroFuzzy Applications in Industrial Automation
221 Inside Real-Time Kernels
222 Developing Flexible, Predictable, Real-Time Systems Using CORBA, Part 1
223 Debugging ISRs

2:00 pm - 3:30 pm

240 Fuzzy Logic and NeuroFuzzy Technologies in Appliances
241 Flash Memory Technology and Techniques, Repeat
242 Developing Flexible, Predictable, Real-Time Systems using CORBA, Part 2
243 68HC12 Software Debugging via Background Debug Mode (BDM)

4:00 pm - 5:30 pm

260 Fuzzy Logic in Automotive Engineering
261 Microprocessors for Consumer Electronics, PDAs, and Communications
262 Repairing Software Faults and Updating
263 Debug of High-Speed DSPs in Real-Time Environments

Classes
Tuesday, November 3
8:30 am - 10:00 am

300 Commercial Support for Embedded C++
301 New DSP-Based Motor Controllers Reduce System Cost, Part 1
302 Understanding USB, Part 1
303 Usability Inspections for Embedded Systems
304 State Machines and State Charts, Part 1
305 Simulating Embedded Real-Time Applications
306 Writing NDIS Drivers
307 Finite State Machines in Distributed Systems
308 Hardware/Software Trade-offs of Hard Disk Drives and other Mass Storage Systems
309 Internet Technologies for Embedded Systems
310 Migrating 68K Code to ColdFire Microprocessors

10:30 am -12:00 pm

320 How to Evaluate C++ as a Language for Embedded Programming
321 New DSP-Based Motor Controllers Reduce System Cost, Part 2
322 Understanding USB, Part 2
323 Improving the Software Process for Embedded Systems, Part 1
324 State Machines and Statecharts, Part 2
325 Building the Right Host Bridge: Advances in Embedded PCI Applications
326 Windows CE in Embedded Applications
327 Integrating the JetSend Communications Protocol into Your System
328 Hardware/Software Codesign for Next-Generation Embedded Systems
329 The How-To's of Flash: Implementing Downloadable Firmware, Part 1
330 Configurable Embedded Systems: Using Programmable Logic to Compress Embedded-System Design Cycles

2:00 pm - 3:30 pm

340 Reducing Run-Time Overhead in C++
341 Programmable DSP Architectures, Part 1
342 USB-Based Microcontrollers in Telecom Peripheral Equipment for PCs
343 Improving the Software Process for Embedded Systems, Part 2
344 State Machines and Statecharts, Part 3: Advanced State Machines and Reactive Systems
346 Enabling Windows CE-Aware Microcontrollers
347 The Inevitability of Embedded Open Networking
348 Software Development and Debug Methods for Systems-on-Silicon
349 The How-To's of Flash: Implementing Downloadable Firmware, Part 2
350 Virtual Memory in Embedded Systems: Uses and Abuses

4:00 pm - 5:30 pm

360 Representing and Manipulating Hardware in Standard C and C++
361 Programmable DSP Architectures, Part 2
362 Remote Device Control with Java and RPCs
363 Starting Your Project with a Great Plan
364 Modeling Complex Behavior Simply
366 Re-Targeting Windows CE for Custom Hardware
367 Issues in Communications Software Design and Development
368 Hardware/Software Trade-offs in Microcontroller-Based System

1998 Embedded Systems Conference, continued

Design
369 Adopting Programming Conventions
370 Efficient Interrupt Processing

Classes
Wednesday, November 4
8:30 am - 10:00 am
400 Develop "Smart" Hardware Devices Using Database Technology
401 Using C++ Efficiently in Embedded Applications
402 Roll Your Own RISC
403 Creating Bootable C Code for Embedded Systems
404 Fundamentals of Class Design
405 Fundamentals of Firewire
406 CAN Physical Layer Options & Data Link Layer Implementations
407 Merged Architecture Approach Embeds Digital-Signal Processing and Improves Real-Time Performance of Microcontrollers
408 Embedded Systems in the Networked World
409 Getting Started with Object Modeling, Part 1
410 Introduction to Microcontrollers, Part 1

10:30 am - 12:00 pm
420 Inside Real-Time Kernels, Repeat
421 Representing and Manipulating Hardware in Standard C and C+, Repeat
422 Debugging ISRs, Repeat
423 Incorporating Windows CE into an Embedded System from Start to Finish, Repeat
424 Implementing Web-Based Management of Networked Devices, Repeat
425 Microprocessors for Consumer Electronics, PDAs, and Communications, Repeat
426 Solving the Big Problems: Architecting a Development Framework for Large-Team Software Projects, Repeat
427 Flash Memory Technology and Techniques
428 Useful Design Patterns in Java
429 Getting Started With Object Modeling, Part 2
430 Introduction to Microcontrollers, Part 2

2:00 pm - 3:30 pm
440 Designing with Real-Time Kernels
441 Multitasking Design and Implementation Issues in Embedded Systems, Part 1
442 An Introduction to Application-Specific Integrated Circuit (ASIC), Part 1
443 Designs That Fly! An Approach to Software Architectural Design
444 Networked Embedded Systems: A Look at the Issues, Approaches, and Trade-offs, Part 1
445 Finalizing Microprocessor and DSP Benchmarks for the Embedded Market
446 Addressing Codesign Issues in Multimedia Set-Top Box Systems
448 PERC: Standard Real-Time Extensions with the Java Language
449 Ensuring Project Success through an Object-Oriented Development Process, Part 1
450 Mixed-Signal Microcontroller Measures Real-Time, True RMS Value of Nonlinear Narrow Pulse Current Waveforms

4:00 pm - 5:30 pm
460 Embedding HTTP Functionality for Web-Based Configuration and Management of Devices
461 Multitasking Design and Implementation Issues in Embedded Systems, Part 2
462 An Introduction to Application-Specific Integrated Circuit (ASIC), Part 2
463 Adding Removable Media to Embedded Systems
464 Networked Embedded Systems: A Look at the Issues, Approaches, and Trade-offs, Part 2
465 8-bit Micros: Onward & Upward
466 Designing Solutions for Advanced Digital Set-Top Applications
468 Garbage Collection Algorithms for Java in Embedded Systems
469 Ensuring Project Success through an Object-Oriented Development Process, Part 2
470 Prototyping Embedded Microcontrollers in FPGAs

Classes
Thursday, November 5
8:30 am - 10:00 am
500 Abstracting a Real-Time Operating System for Hardware Portability
501 Integrating DSP in System-on-a-Chip Design
502 Key Features for Developing Hot Swap PCI Silicon for CompactPCI Adapter
503 Code Generation from Object Models, Part 1
504 Controlling Radio Frequency Interface and Electromagnetic Radiation in Pc Board Designs
505 Simplifying Complex Real-Time Applications: A New Approach
506 Unified Object-Oriented Methodology, Part 1
507 Focus on Threads: An Introduction
508 Architecture of Device I/O Drivers, Part 1
510 Communication Algorithms Implemented in General Purpose Programmable Digital-Signal Processors, Part 1

10:30 am - 12:00 pm
520 Meeting the Requirements for Certifiable Software
521 Moving IP to the System Level: What Will It Take?
522 Hot Swap Software for Windows NT 5.0 and CompactPCI
523 Code Generation from Object Models, Part 2
524 Interfacing High-Performance ASICs to the Pc Board Transmission Line Environment, Part 1
525 A Free Java Virtual Machine for Embedded Systems
526 Unified Object-Oriented Methodology, Part 2
527 Security: Process, Threads, or Both?
528 Architecture of Device I/O Drivers, Part 2
529 An Introduction to FPGA Design, Part 2
530 Communication Algorithms Implemented in General Purpose Programmable Digital-Signal Processors, Part 2

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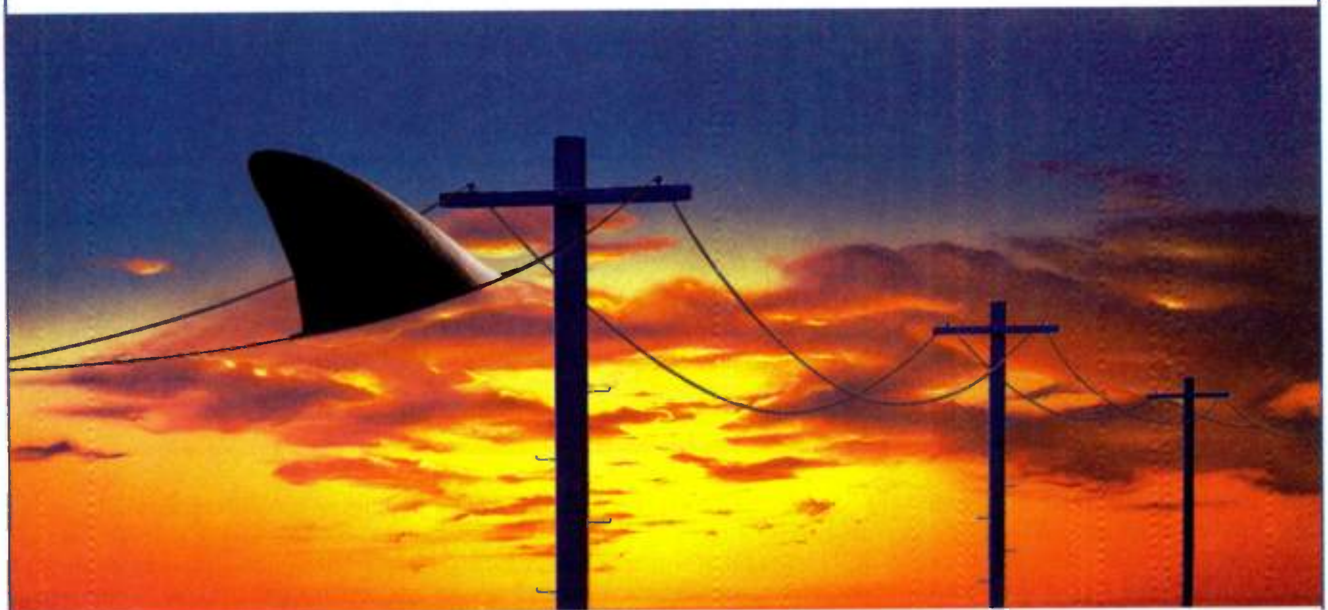

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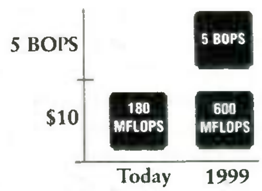

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1998 Embedded Systems Conference, continued

2:00 pm - 3:30 pm

540 Creating Embedded PCs Super-Workshop, Part 1
541 Software Development Methodology for System-on-a-Chip
542 Exploring the Intel Pentium's Features to Support Today's Embedded Applications, Part 1
543 Implementing the LonTalk Protocol for Intelligent Distributed Control, Part 1
544 Interfacing High-Performance ASICs to the Pc Board Transmission Line Environment, Part 2
545 Mixing C and Java in Embedded Systems
546 Unified Object-Oriented Methodology, Part 3, Design Patterns for Embedded Systems
547 Reliability Testing
548 RTOS Design: How Your Application Is Affected, Part 1
549 Design for an Embedded ATAPI Device Driver
550 DSP Techniques and Features for Embedded Micro-Controller Applications

4:00 pm - 5:30 pm

560 Creating Embedded PCs Super-Workshop, Part 2
561 Software/Hardware Codesign for Platform Chips
562 Exploring the Intel: Pentium's Features to Support Today's Embedded Applications, Part 2
563 Implementing the LonTalk Protocol for Intelligent Distributed Control, Part 2
564 Embedded C and C++ Compiler Evaluation Methodology
565 STREAMS Architecture for the Real-Time Environment
566 Capturing, Recapturing, and Building Solutions: Why a Single Architecture is Not Enough
567 High-Integrity Ada Tasking Is Not an Oxymoron
568 RTOS Design: How Your Application Is Affected, Part 2
569 Translating Java to C
570 Longer Lasting Product Designs: Cost Reductions and More Functionality Are Possible.

the class, "Capturing Requirements and Building Solutions: Why a Single Architecture is Not Enough." It presents the concept of a solution architecture. This architecture describes how a system will achieve a solution in terms of objects, tasks, and processor boards. The class discusses the models required in each architecture, and how requirements are evolved into or mapped onto the solution to provide traceability and enable verification. Along similar lines the tutorial, "Usage-Centered Engineering for Embedded Systems," explores usage-centered engineering—an integrated systems approach to designing embedded systems that meet user needs with simpler, more usable controls and interfaces.

With embedded software moving into more life-critical systems, developers are looking for ways to both increase software reliability and verify that reliability. In "Meeting the Requirements for Certifiable Software," attendees find out about the certification process in general. This session takes a close look at the steps required to produce software that is certifiable, using the RTCA/DO-178B standard of the United States Federal Aviation Administration (FAA) as an example. Another class, "Reliability Testing," covers general procedures that companies can apply to their own reliability testing analysis, permitting them to check their own risk analysis and improve testing.

The magic of semiconductor integration has brought complete systems down to the chip level. This doesn't make life any easier for embedded software integration. The class, "Software/Hardware Codesign for Platform Chips," discusses why radical changes are needed in the way the systems are designed.

This class covers aspects of the market/product segmentation and definition, interactive system partitioning/mapping, and software/hardware coverification. "Hardware/Software Codesign for Next-Generation Embedded Systems" takes a more fundamental look at the role of performance modeling in designing next-generation embedded systems.

Please Mind Your Languages

If microcontrollers and embedded processors are the heart of embedded systems, software languages are the blood. With C++ and object-oriented programming getting more mainstream, there's no longer a dividing line between languages and methodologies. As usual, this year's conference devotes a significant number of sessions to topics like C, C++, and other programming fundamentals. Java also is creeping into the conference this year.

The tutorial, "Stepping up to C++," highlights the differences between C and C++ programming styles, and offers advice on migrating people and projects from C to C++. "Commercial Support for Embedded C++" talks about Embedded C++, a subset of the draft C++ standard better suited for embedded applications. This class outlines that subset, describing the compilers, libraries, development tools, and training materials needed to implement embedded C++.

Going beyond the basics, several papers focus on improving C++ expertise. "Reducing Runtime Overhead in C++" examines the cost of various C++ language features. The paper also presents programming techniques that can help reduce those costs. Exploring the data structure side is "Representing and Manipulating Hardware in Standard C and C++." This session looks at the features of standard C and C++ that can be used to represent hardware as data structures. Describing the common idioms for controlling typical devices, it focuses on what can be done using only standard language features. Finally, "Using C++ Efficiently in Embedded Applications" discusses the use of exception handling, inlined code, and object-oriented design in producing efficient C++ embedded applications.

While Java is still catching on as a programming language, it's not a sure bet for embedded systems. To help de-

velopers sort out the issues, the conference offers a generous selection of classes on Java. "Translating Java to C" provides attendees with the information needed to begin assessing whether to use Java as a development language for embedded systems. "Mixing C and Java in Embedded Systems" gives a step-by-step description of adding an HTML-plus, Java-based GUI to an embedded application written in C or C++.

Getting A Taste For Java

For those ready to learn the language itself the tutorial, "Object-Oriented Programming in Java," provides an introduction to the Java language and object-oriented programming. Designed for people who are familiar with C, it doesn't cover the sections of the Java language that are also found in C. It teaches the fundamentals, such as how object-oriented concepts are integrated in the Java programming language.

A number of classes delve into specific Java subtopics. In "PERC: Standard Real-Time Extensions with the Java Language," learn how the PERC extensions enable real-time software components to enjoy the same high-level portability benefits that make Java so attractive to developers of web and desktop applications. The session, "Remote Device Control with Java and RPCs," explains why the lack of pointers makes it very difficult to manipulate hardware from a Java Virtual Machine. It will focus on developing and using a Java application to communicate with remote system devices using the Remote Procedure Call (RPC) protocol.

Embedded-systems developers continually face the challenge of managing limited memory resources. The Java language run time utilizes garbage collection to automatically manage memory use. The class, "Garbage Collection Algorithms for Java in Embedded Systems," aims to help developers understand, fine tune, and select the appropriate garbage-collection algorithm for their embedded system.

The operating system or real-time kernel is the place where an embedded system all comes together. It's the part of the system that ensures that hardware and software are getting along. Like last year, Windows CE remains the conference's hot topic. For those who need an introduction to the OS, "Windows CE in Embedded Applications" outlines the major features of the operating system. It then discusses some of the issues in designing hardware for Windows CE, including the trade-offs of capability and cost as relevant to embedded systems.

Providing a soup to nuts look is the session, "Incorporating Windows CE into an Embedded System From Start to Finish." This class provides a comprehensive look at planning an embedded design for running Windows CE.

Using Windows CE in custom embedded designs involves many tricky issues. The class, "Re-Targeting Windows CE for Custom Hardware," explains the adaptation of Windows CE to target custom hardware with non-standard peripherals and memory. Look for more on the hardware issues in "Enabling Windows CE-Aware Microcontrollers." This class describes the support required for a high-integration microcontroller to be designed into an OEM product running the Windows CE operating system.

Real-Time Kernels.

Whether you design your own or buy one off the shelf, real-time kernels are key to an embedded system's reliability, performance, and functionality. The class, "Inside Real-Time Kernels," introduces real-time kernels by showing how one of these kernels works. At a more sophisticated level, "Designing with Real-Time Kernels" describes the uses of a real-time kernel in an embedded system. Learn how to split an application into separate tasks, assign priorities to tasks, use kernel services such as semaphores, message mailboxes, message queues, time delays, and so on. Also, see how interrupts interact with tasks.

At the center of any embedded system is the CPU, running the code. Whether that CPU is an 8-bit microcontroller, a 32-bit RISC processor, or a DSP, this choice will affect the performance and code size of the embedded software. Classes on these topics range from basic to complex and general to specific. In "Introduction to Microcontrollers," attendees learn the basics of microcontrollers: what they are, how they're composed, and how they work. For a more comparative look, "8-bit Micros: Onward and Upward," checks out the 8-bit front. This class compares the latest offerings in everything from 8 pins to 80 MIPS.

In consumer electronics, PDAs, and communications, 32-bit RISC microprocessors are fueling a true revolution. The session, "Microprocessors for Consumer Electronics, PDAs and Communications," looks at the 32-bit chips succeeding in these booming markets, as well as what features to look for when designing a new system.

Processor-Specific Topics

Getting more processor-specific, two classes focus on 68k processors. Examine the process of debugging 68HC12 systems in "68HC12 Software Debugging via Background Debug Mode (BDM)." This session pays particular attention to configuring targets for real-time debugging, developing code on single-chip targets, debugging C code resident in flash/EEPROM, and resolving time-dependent bugs in the field. Another class, "Migrating 68k Code to ColdFire Microprocessors," discusses techniques and tools for migrating 68k application code to the ColdFire technology, including the use of automated code-conversion tools.

DSP gets a healthy representation this year. Several looks are taken at the unique challenges of integrating DSPs in embedded systems. For an overview of the choices available, there's "Programmable DSP Architectures." This two-part class touches briefly upon introductory DSP and native signal-processing concepts. It then outlines important features of DSPs, modern processor microarchitectures, and design techniques.

"Integrating DSP in System-on-a-Chip Design" introduces systems designers to the issues involved in incorporating DSP in a system-on-a-chip design. Items to be explored include justifying DSP integration, trade-offs in DSP/host task partitioning, DSP architectures that enable easy integration, host-DSP interaction, and DSP software-development issues. DSP techniques aren't only important on DSP chips. As microcontrollers move to higher speeds and/or integrate DSP cores, they can benefit from DSP programming tactics. The class, "DSP Techniques and Features for Embedded Microcontroller Applications,"

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- 180 million fixed-point OPS
- 8 I²S serial ports
- 0.31 ms 1024-pt FFT
- Byquad filter: 67 ns each section
- 544 Kbits configurable SRAM
  - up to 10 Kwords program
  - up to 16 Kwords data
- 10 nonintrusive DMA channels
- Glueless, 32-bit SDRAM interface
- Code compatible with ADSP-210xx

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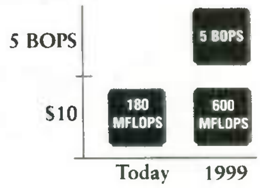

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presents signal-processing techniques and DSP core features that are attractive to microcontroller applications.

Connected Embedded Systems

Among the emerging trends in embedded systems, the most compelling is the idea of "connected everything." William Peisel, president of Osicom, Waltham, Mass., predicts that within five years, everything from Coke machines to cardiac monitors will most likely be networked for command and control purposes. A swath of classes focus on embedded-Internet, network, and web technologies.

Along these lines, "The Inevitability of Embedded Open Networking" is set to discuss how to use the inter/intra protocols to install, monitor, transfer data, and diagnose problems on devices. It covers application examples and explores the potential business benefits, as well as the architecture alternatives for implementing embedded networking.

"Internet Technologies for Embedded Systems" looks at the browser side. This class compares several solutions for applying Internet technologies in embedded systems, including embedded Web servers, Java, and distributed solutions. Sample applications and demonstrations help participants see the benefits and drawbacks of various embedded-Internet solutions.

Covering similar ground is the class, "Embedding HTTP Functionality for Web-Based Configuration and Management of Devices." Attendees find out how to embed 100-kbyte HTTP servers ("microservers") into products such as network hardware, office equipment, and industrial products. Users can then remotely monitor, configure, and diagnose vital systems.

Some specific network issues are found in "Implementing Web-Based Management of Networked Devices," like using the Simple Network Management Protocol (SNMP) for management, monitoring, and control over the network. This class explores implementation issues in devices and talks about SNMP, HTTP integration, and future directions.

For more information about the Embedded Systems Conference, call (800) 789-2223 or (817) 255-8050, or reach them on the Internet at *www.embedded.com.*

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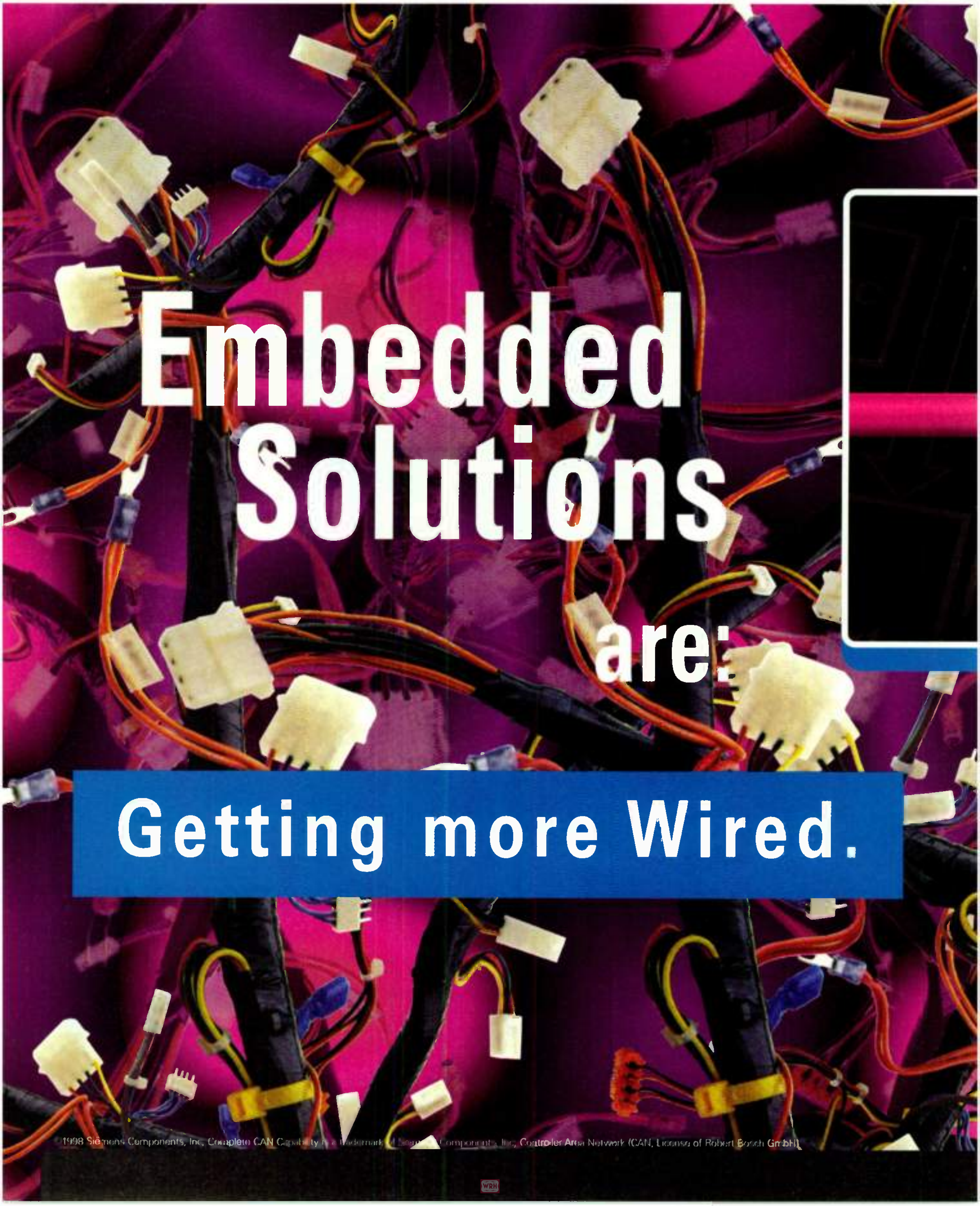

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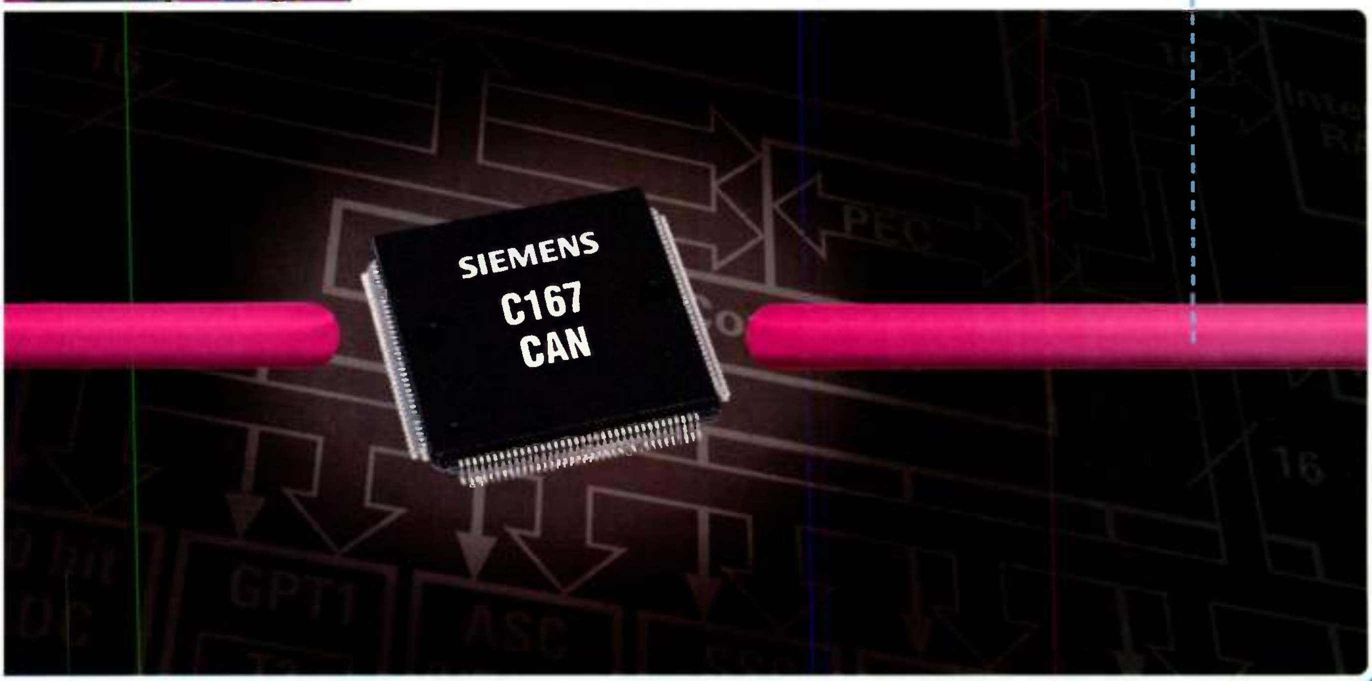

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READER SERVICE 155

Embedded Solutions from Siemens Semiconductors.

ELECTRONIC DESIGN QUICK LOOK

■ Edited by Debra Schiff and Nancy Konish

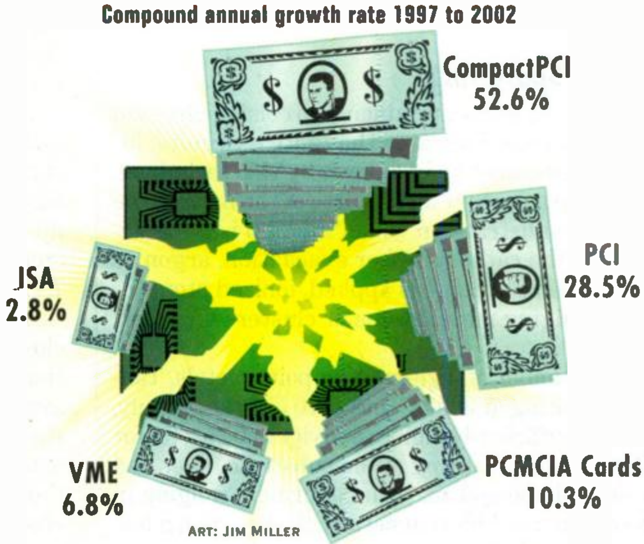
MARKET FACTS

Data-Acquisition Analog I/O Boards Explode With Riches

The predictions are in. According to the crystal ball, the overall U.S. market for plug-in data acquisition analog I/O boards will keep growing, starting at $137 million in 1997 and hitting $219 million in 2002. This information came from a recently released market study and forecast, "The U.S. Market for Data Acquisition Products," by Venture Development Corporation (VDC). These numbers come out to a compound annual growth rate (CAGR) of just under 10%. The growth rates for boards with PCI and CompactPCI bus architectures, however, are expected to be even steeper. VDC projects the PCI plug-in analog I/O board segment will grow at a 28.5% CAGR, rising from $15 million in 1997 to almost $53 million in 2002. Profit looks even brighter on the side of the CompactPCI boards. VDC estimates that the U.S. market for these will grow at a 52.6% CAGR, rising from just under $2 million in 1997 to almost $15 million in 2002. Much of this robust growth in PCI is expected to come at the expense of ISA, and to some extent VME, in many applications. Intel created the PCI bus for commercial PCs, mostly to provide a high-speed data path between the CPU and peripheral devices (video, disk, network, etc.). Users are expected to increasingly choose computers with this bus architecture for its high bandwidth, high sample data rates, high reliability, and flexible form factor. Plus, PCI can be used in computers with a combination of ISA/PCI architecture. PCI plug-in analog I/O boards are expected to do very well in applications requiring high speed and broad bandwidth, such as automotive engine testing and simulations in the military and aerospace industry. Despite the displacement of ISA in many applications, VDC is not predicting a death nell for this bus architecture—at least not within the next five years. ISA analog I/O boards accounted for $75 million of the U.S. market in 1997. This segment is expected to grow to $86 million in 2002, at a low 2.8% CAGR. A growing shift in this market segment to purchase replacement boards, rather than new PCs, is expected to help maintain sales growth. In many applications, large share of the explosive growth projected for CompactPCI also is expected to come at the expense of ISA and VME bus architectures. The CompactPCI bus is an adaptation of the PCI specification that provides a more robust mechanical form factor. CompactPCI uses standard Eurocard mechanical components and metric connectors. This bus architecture has the advantage of providing high reliability, as well as ruggedness, small form factor, and broad bandwidth capability. CompactPCI plug-in boards possess connector and card guides that firmly hold the boards in position, making these ideal for tough industrial and field environments. It is expected that OEMs will be leaders in adopting CompactPCI bus architectures. It should be noted, however, that despite CompactPCI's explosive growth rate forecast, this bus architecture is expected to still represent a small share, less than 6%, of the overall U.S. plug-in data-acquisition analog I/O board market in 2002.

U.S. market growth forecast for plug-in data-acquisition analog I/O boards

Compound annual growth rate 1997 to 2002



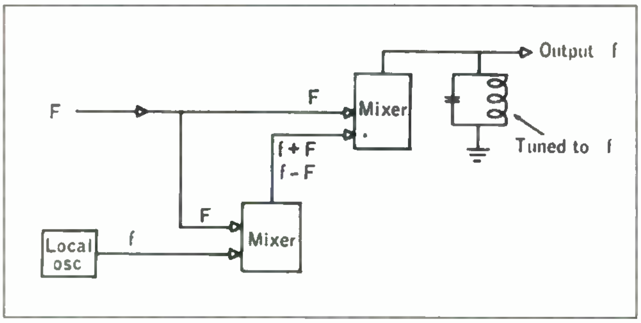
J. Timothy Shea is a project manager for Venture Development Corporation, a market research and consulting firm specializing in electronic technology. Shea holds a BS in marketing from Bentley College, Waltham, Mass. and an MBA from F.W. Olin Graduate School of Business at Babson College, Wellesley, Mass. He can be reached at (508) 653-9000, ext. 132 or via e-mail: tims@vdc-corp.com.

40 YEARS AGO IN ELECTRONIC DESIGN

Idea For Design: One RF Frequency From Many

We needed a circuit to accept rf at any frequency and, without tuning, deliver a known and constant rf frequency, despite any input frequency changes. The block diagram shows the solution.

The local oscillator is tuned to the desired output frequency *f*. This is mixed with any incoming frequency *F* in mixer 1. The output of mixer 1 is *f* + *F* and *f* – *F*. These are heterodyned against the incoming *F* in mixer 2. Mixer 2 provides *f* + *2F*, *f* – *2F*, and *f*.



A tank at the mixer output can assure that the output frequency will always be *f*, regardless of the input frequency. The local oscillator can be crystal controlled, so the output frequency can be as stable as if it were crystal controlled.—J. Frank Brumbaugh, Senior Marine Engineer, Heath Co., Benton Harbor, Mich. *(ELECTRONIC DESIGN, October 29, 1958, p. 98)*

It's hardly surprising that the Heath Co. was a rich source for practical circuit-design ideas—their equipment had to be designed so that it worked the first time, even if it had been put together by a technically precocious high-school student.—Steve Scrupski

Printed Circuits Made By Metal Sputtering

Cathode metal sputtering may be useful in producing precision circuits. Research at Bell Telephone Laboratories indicates that entire circuits, including resistors, capacitors, and leads, may be laid down by this technique. In cathode sputtering, an effect noted a century ago, a plate of the metal to be deposited is used as a cathode. The substrate on which the film is to be deposited is placed on a table close to the cathode. After evacuation, argon or other suitable gas is introduced. When a voltage is applied, ionized atoms of the gas bombard the cathode, dislodging metal atoms or clusters of atoms, which then deposit on the substrate.

Bell has produced thin films of a number of high-melting-point metals. Tantalum and titanium, for example, melting at 3000 C and 1670 C, respectively, can be laid down in films which show sufficiently high resistivity to be useful for resistors in printed circuits. With proper masking of the substrate, lines and patterns of practically any desired shape and size can be formed, ranging in widths down to a few mils. These sputtered films generally are between a few hundred and a few thousand angstroms thick.

Printed capacitors have been produced by a combination of sputtering and chemical methods. A tantalum film of the proper shape and size is first sputtered onto the substrate, and then anodically oxidized to form a tantalum oxide dielectric film. The counter electrode, a film of gold, can then be evaporated to a dielectric to form the completed capacitor "sandwich." *(ELECTRONIC DESIGN, October 29, 1958, p. 10)*

Another Bell Labs success story. The Murray Hill Labs continued to be a leader in the development of thin-film technology right up until the breakup of the Bell System.—Steve Scrupski

Steve Scrupski is a former Editor-in-Chief of ELECTRONIC DESIGN. Now semi-retired, he can be reached at scrupski@worldnet.att.net.

Help Still Wanted

As the worldwide economy remains in flux, many voice concern over the state of the industry. The electronics industry typically retains a pretty good reputation for keeping its job market steady. And, this isn't going to change anytime soon, according to a recent survey by Management Recruiters International Inc. (MRI).

The forecast reveals a healthy industry, with consistent opportunity and growth. It also exposes a wealth of opportunity for those in the more peripheral areas of the industry: the executive, professional, and sales people in electrical and electronic products.

The forecast pinpoints the second half of 1998 as its focus. Most of its information was gained from executives. Those surveyed stand responsible for hiring in the electronics industry, and the survey outlook was garnered from their plans. Of the responses, 55.4% indicated plans to increase their staff size. Though this is down 4.6 points from the first half of the year, the difference is small enough that the market is still considered steady.

About 36.9% answered that they intend to maintain their current staff numbers. This number rose by only .8 of a point. Of those that plan downsizing or some type of decrease in staff size, there were only 7.7%—up 3.8 points.

The results of this survey stand closely within the range of the national average. The United States average for projected new hires in the electrical and electronic products industry is 56.5%. Those that intend to retain their current size check in at 37%. And, the number of executives looking to make reductions in staff came out to 6.5%, just slightly lower than the results garnered from those surveyed by MRI.

For more information or to obtain a copy of the survey, contact Management Recruiters International Inc., 200 Public Square, 31st Floor, Cleveland, OH 44114; (800) 875-4000; fax (216) 696-3221; www.mrinet.com.—**NK**

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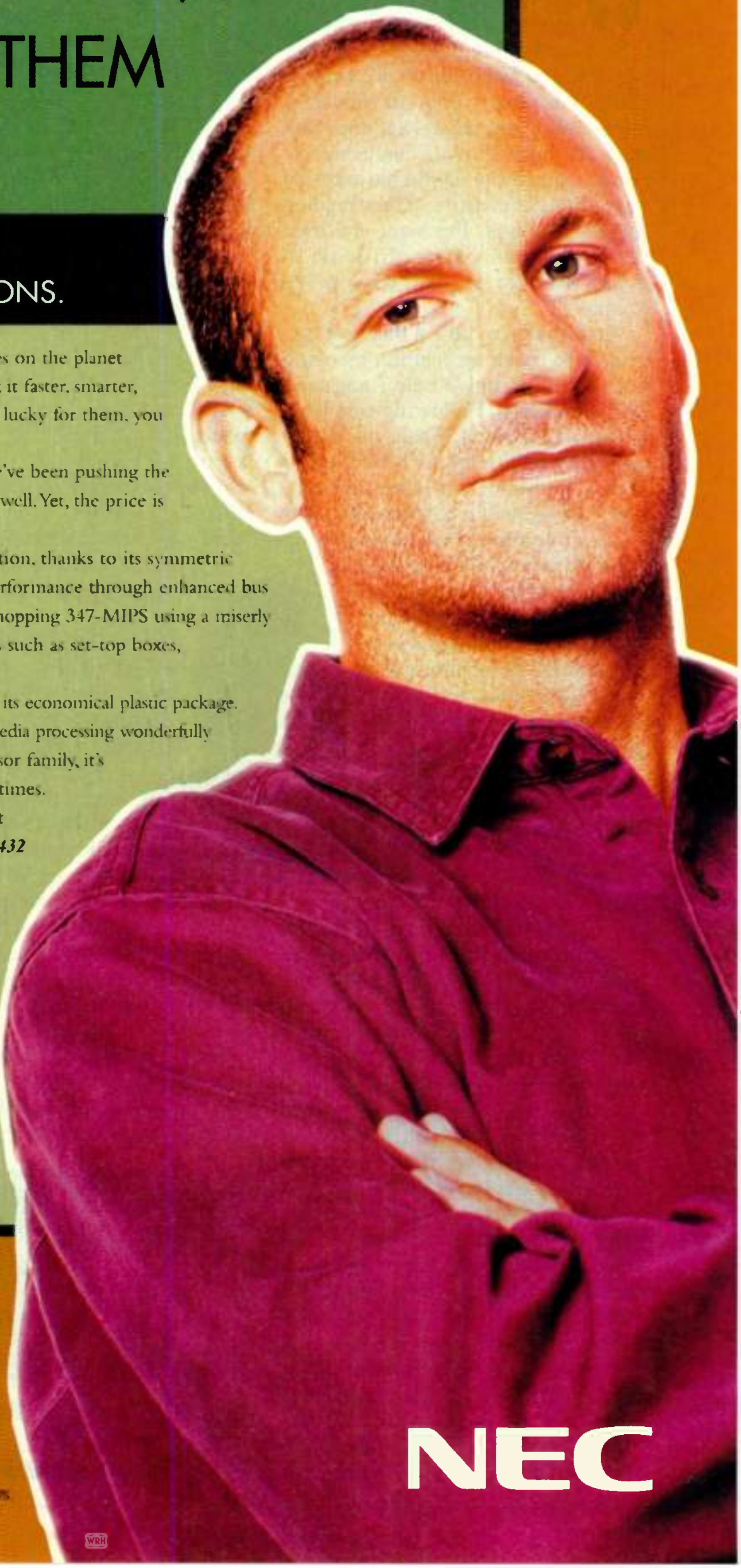
CPU Speed	167 MHz	Dhrystone MIPS	347
System Interface	32 Bit	On-Chip Debugging	Yes
Bus Speed	67 MHz	Power Consumption	2.5W Peak
I Cache Size	32 KB	Multimedia Extensions	Yes
D Cache Size	32 KB	Floating Point Unit	IEEE-754
Pin Count/Package	208 PQFP	Chip Set Support	Yes



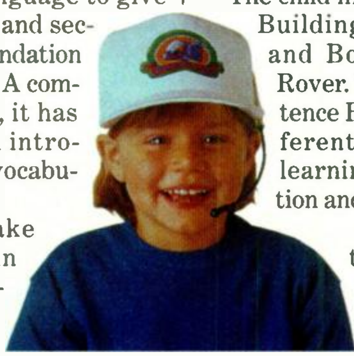
NEC

READER SERVICE 133

JUST 4 THE KIDS

With a new school year now under way, many parents' prime concern is whether their child is learning to read. Recognizing reading as the cornerstone of all learning, many of us want to give our children a headstart. Unfortunately, it's not that easy. At times it's even confusing, especially since the media has painted very different pictures of how reading should be taught. For some children, these differences are difficult to grasp. But for others, it's a piece of cake.

Most teachers take a balanced approach to teaching reading by using both Phonics and Whole Language Methodologies. Following this lead, Edmark, Redmond, Wash., has developed an early reading CD-ROM called "Let's Go Read! An Island Adventure." Designed for children ages four to six, it combines the strengths of phonics and whole language to give kindergartners, first, and second graders a solid foundation for successful reading. A comprehensive program, it has over 175 lessons and introduces more than 400 vocabulary words.



Designed to make learning to read a fun adventure, the CD-ROM uses colorful graphics and speech-recognition technology. This technology utilizes mathematical models of the way words are pronounced and used in context to permit the computer to hear spoken words. As the child reads a word out loud, the computer can listen and respond. This motivates the child to use the words he or she is learning to read. Reading each word aloud also helps the child remember how the word sounds, which improves memory recall.

The child also can use his or her voice to interact in two more ways: voice activation and record and playback. With voice activation, the child's voice directs the computer's actions. With record and playback, the child can listen to his or her own voice by reading 12 interactive books included in the program.

When a child first enters the world of this CD-ROM, he or she meets a raccoon named Robby and his squirrel pal, Emily. Together, they embark on an interactive adventure in an incredible flying machine called the Reading Rover. They travel to Letter Island and meet the shy inhabitants—letters of the alphabet that won't come out to play unless the child calls out their sounds.

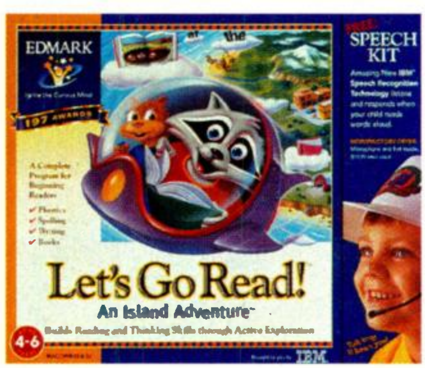
MARIFRANCES WILLIAMS

While soaring through the clouds aboard the Reading Rover, the child can participate in over 35 activities. In Sight Words, for example, the child encounters special word clouds and is asked to say each word he or she sees. When the word is spoken, the cloud disappears with a "poof" and the flight continues.

The child may also engage in Word Building, Sentence Building, and Books on the Reading Rover. Word Building and Sentence Building contain two different modes for additional learning—explore and question and answer mode.

After traveling to Letter Island, the child can visit one of four areas: the beach, farm, jungle, or Vowel Village. There, the child can participate in several different activities, such as Letter Sound Introduction, Letter Recognition, Letter Form Awareness, Letter Sound Recognition, and Letter Sounds in Words.

Tools are included to help track the child's progress easily. A Letter Chart tracks the letters a child has successfully mastered. And, as the child completes specific activities, a Bookshelf collects and displays books correlating to the child's newly learned skills. There's an adult option, featuring a Grow Slide that measures the child's progress. As the child masters questions, the slider on the Grow Slide automatically advances. More difficult questions and new letters are then introduced. Manual manipulation can add focus in weaker letter areas.



A Pilot Training Overview familiarizes the child with speech recognition and the meaning and usage of directional terms. Once the program is installed, the child simply puts on their first-class pilot hat and travels the road to reading.

As the children learn to read, they're entranced by the fun found in the CD-ROM. Positive reinforcement balances humor and encouragement, making the child feel successful and motivated to continue learning. The activities, pilot training, and speech-recognition technology make this program a worthwhile addition to any learning library.

Let's Go Read! An Island Adventure CD-ROM is available at local retailers for an estimated price of $44.95. It comes with a booklet that explains how the parent and child can spend time together after using the CD-ROM to enhance the child's new skills. Other Edmark selections you might check out include Thinkin' Science, Mighty Math Grades K-2, and Mighty Math Grades 3-6.

For more information, contact Edmark at 6727 185th Ave. NE, P.O. Box 97021, Redmond, WA 98073-9721; (800) 426-0856; www.edmark.com.

Marifrances D. Williams holds a degree in Liberal Studies from San Diego State University, Calif. She is currently a fifth-grade teacher at Los Ranchos Elementary, San Luis Obispo, Calif. Williams specializes in the identification of advanced technology for the use of child-focused applications. She may be reached at williamsofsm@lightspeed.net.

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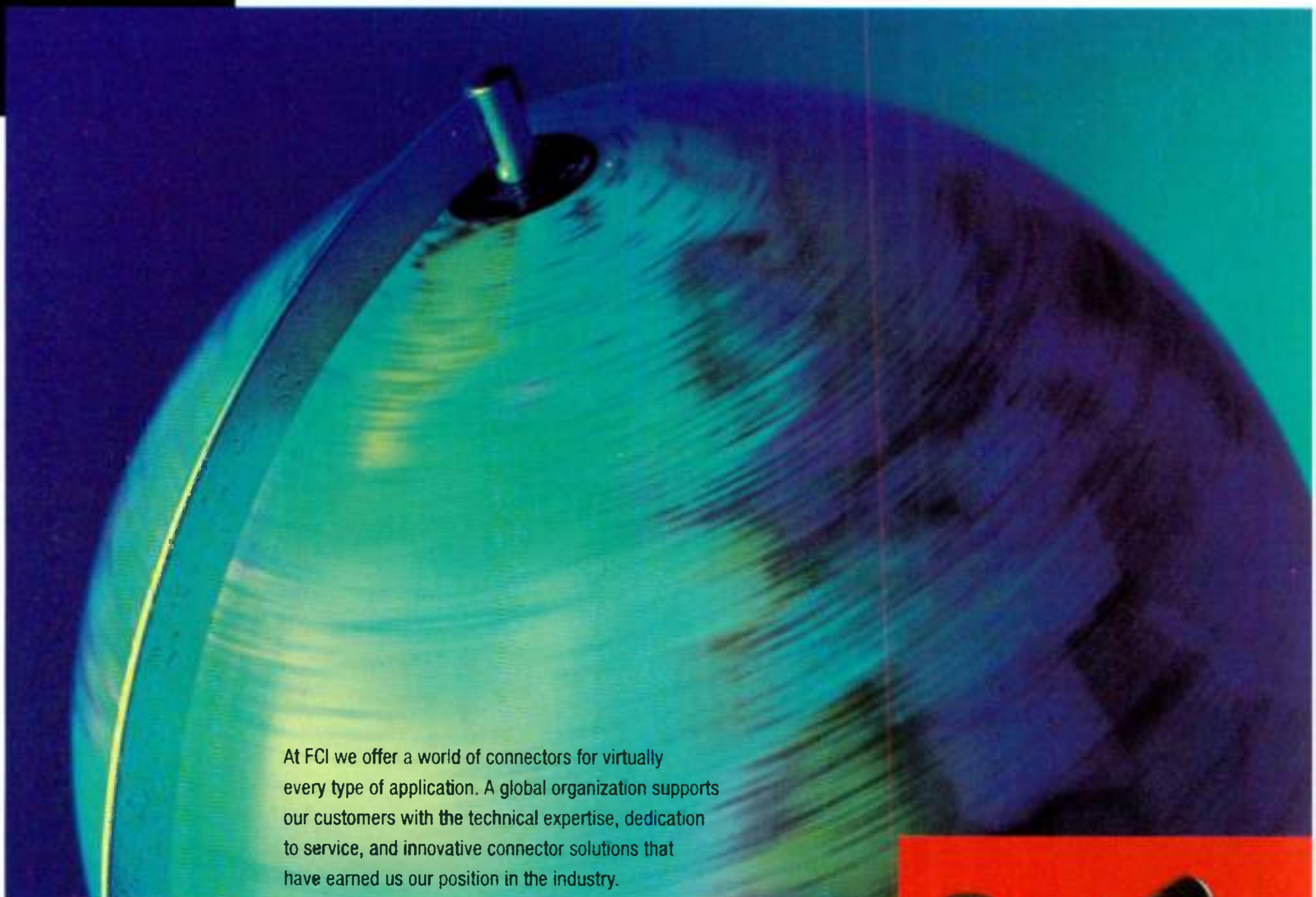

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READER SERVICE 112

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READER SERVICE 153

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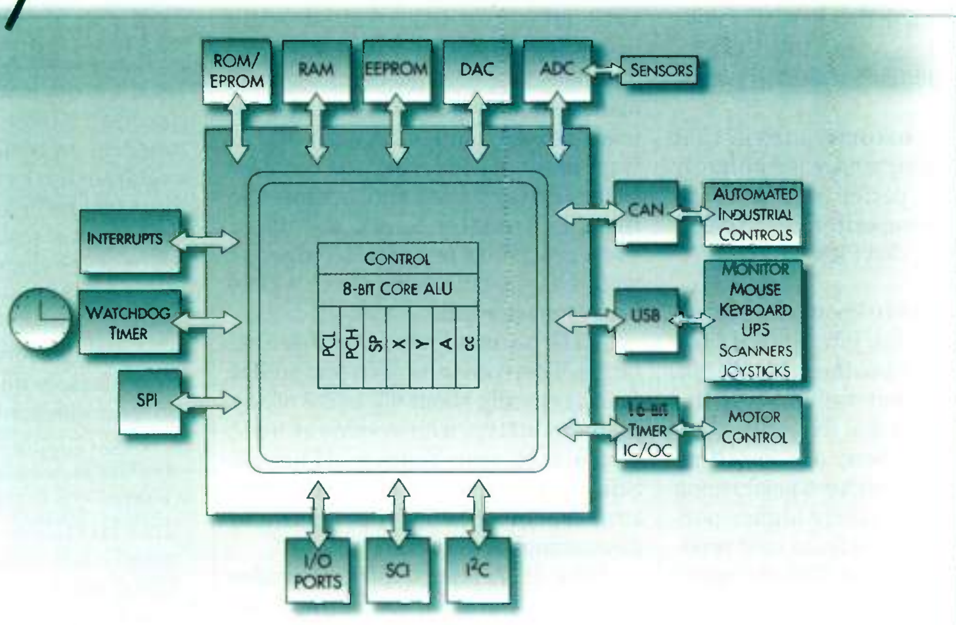
DEVICE	ROM/ EPROM	RAM	EEP	TIMERS	SERIAL COMM	A/D 8-Bit	I/Os	PCKG
ST72101	4-8K	256	-	1x16 bit	SPI	-	22	SDIP32/SO28
ST72121	8-16K	384-512	-	2x16 bit	SPI/SCI	-	32	SDIP42/TQFP44
ST72213	8K	256	-	2x16 bit	SPI	6	22	SDIP32/SO28
ST72311	8-32K	384-1024	-	2x16 bit	SPI/SCI	8	44	SDIP56/TQFP64
ST72331	8-16K	384-512	256	2x16 bit	SPI/SCI	8	44	SDIP56/TQFP64
ST72251	8-16K	256	-	2x16 bit	I²C/SCI	6	22	SDIP32/SO28

ST7 Micros



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TRUDEL TO FORM

JOHN D. TRUDEL

Let me start, dear readers, by asking a few questions to help steer this discussion thread. Please mark up a copy and drop it in the mail, or respond by e-mail. I will also post these on my web page for your convenience:

1. Does your upper management care about consistently delivering innovative new products? __ yes, __ some, __ not at all, __ don't know.

2. Does your firm have a clear strategy, beyond increasing profit or stock price? (Not a slogan on the wall, but some committed-to policy that includes purpose and values) __ yes, __ some, __ not at all, __ don't know.

3. Does your firm encourage doing new things and allow learning mistakes? __ yes, __ some, __ not at all, __ don't know.

4. Approximately what percentage of your sales comes from products that are "new?" (You define new.) __ none, __ few (<10%), __ some (10% to 25%), __ a fair amount (25% to 50%), __ most (>50%).

5. Do your customers think that your firm's products have significantly better features, performance, or quality than your competitor's? __ yes, __ maybe, __ no, __ don't know.

Why do I want to know, you ask? To help improve your job content, and your employer's business condition. Let's review what we've been discussing in my past few columns:

First, there is body of compelling evidence that the highest performing firms get a significantly higher percentage of their sales from new products (Source: Product Development and Management Association).

Second, firms with sound strategies for new products financially outperform those with no strategy or solely financially based strategies (Source: Robert G. Cooper, "Portfolio Management Results of New Product Portfolio Best Practices Study," Product Development and Management Association Research Conference, Monterey, Calif., Oct. 19-20, 1997).

Third, in the Information Age, businesses cannot make money on a sustained basis from anything that is standard and routine. Those things quickly fall to third-world wages, and razor-thin margins. In fact, there are whole economies with "conquest" strategies that are delighted to sell below cost to gain share and discourage competition in key markets.

My own experience, spanning three decades, convinces me that most firms do what their CEOs want, eventually, whether it's good or bad. This trend gets stronger, and many CEOs don't care about innovation or new products.

This logic chain leads us to interesting conclusions. A firm that can innovate consistently can deliver sustained prosperity. It can outperform the firms whose strategies are "cheaper, faster." But, it can only hope to succeed at innovation if its top management really wants to do that.

About 10% of firms innovate well, and another 10% try. The rest cling to machine-age routine. Because the old ways aren't working, the pressures for change are extreme. And, because the firms I encounter tend to be either very proficient or quite troubled, I would like a calibration as to where your employers fall.

All firms need not resemble Dilbert's. There are always a few stellar firms, typically about 6% to 8% of any given industry, whose sales at least double each year. Yours could be one. Still, overall, most are stuck. The Fortune 500 has been flat in sales and downsizing for decades.

John D. Trudel, CMC, provides business innovation consulting to selected clients. Lectures, keynotes, and workshops also are available. He is the author of "Engines of Prosperity." The Trudel Group, 33470 Chinook Pl., Scappoose, OR 97056; (503) 638-8644; fax (503) 543-6361; e-mail: jtrudel@gstis.net; Internet: www.trudelgroup.com.

Alta-ing Your Card

Introducing...Alta Technology, Sandy, Utah. Along with Packet Engines Inc., Spokane, Wash., they've designed a Gigabit Ethernet network interface card (NIC) in a PCI Mezzanine Card (PMC) design. With use, this PMC mezzanine form factor is expected to provide superior performance, interoperability, and ease of use.

The PMC/GNIC card operates in 32- and 64-bit systems. As a 64-bit adapter, it provides 2 Gbits of full-duplex throughput to the host computers while running at a PCI bus speed of 33 MHz. The card also allows 10 times the bandwidth of Fast Ethernet.

The adapter's Rx and Tx instruction prefetch ensures that the packets are not held in queues waiting for instructions. Using Packet Engines' G-NIC technology, this reduces latency. Plus, the G-NIC adapter's dual PCI burst FIFOs enable data pipelining between the host and the NIC in both Rx and Tx directions. It maximizes throughput by minimizing retransmission during extended bursts due to its large external packet buffers.

The on-board independent Rx and Tx descriptor-based DMA processors reduce host CPU utilization. They stream Rx and Tx data to and from the host memory without host intervention. The host CPU utilization is also reduced by transmit packet chaining, which transfers multiple packets from the host memory to the PMC/GNIC adapter with a single interrupt. These combined factors give the PMC/GNIC adapter maximum CPU.

Packet Engine's Gigabit Ethernet Media Access Controller (MAC) technology, the PE-MAC, permits the PMC/GNIC adapter to comply with IEEE 802.3x full duplex and IEEE 802.3z draft standard for the broadest interoperability.

The PMC/GNIC has driver support for WindowsNT, UNIX, and Linux. Priced at $1395, it's available immediately. For more information, visit Alta's web site at www.altatech.com.

Lisa Calabrese

Cut This Class And End Up With Culture Clash

As technology makes doing business overseas as convenient as a videoconference, people often forget that cultural differences exist. Unfortunately, it's pretty easy to accidentally offend someone just by having different mannerisms and not being aware of their cordialities.

Etec Systems, Hayward, Calif., does more than half of its business overseas. They produce the machines which generate the master patterns for producing semiconductor chips. The prices for these machines peak at $12 million, making each sale vital. The sale itself can take months of negotiation, effort, and meetings. Customers visit the company's headquarters to train and learn about the equipment. And, once a machine is sold, an Etec engineer goes along to get it up and running.

Because so much of its business relies on communication with companies outside of the U.S., Etec saw a need to provide training on international culture. The result of this brainstorm, "Passport Days," focuses on educating employees about the business practices of other cultures.

Admirably, Etec sends every single one of its 1000 employees through this training—not just the sales staff. For the presentations, a trainer from each country comes in to present the practices of that country. This is moderated by a panel of Etec personnel that were born or are doing business in the country being studied.

There's lots of choices on which country or area to study. The European and Pacific Rim Passport Days cover several countries in one session, while all-day focus groups go into more detail on the particular business cultures of France, Germany, Japan, Korea, Taiwan, or the United Kingdom.

The goal of this education is to avoid any cultural misunderstandings that might be obstacles to completing a sale or supporting a customer. One would think that cultures differ mainly in areas like food, clothing, history, etc. But, the reality is that every culture contains sort of a rule book, filled with manners, practices, or faux pas of which people outside the culture probably aren't aware.

For example, the French prefer to close a deal over dinner. Writing on a business card or stashing it in your hip pocket is considered impolite in some Asian countries. And as for faxes and e-mails, some countries don't find them an acceptable form of communication.

Looking at Etec, it's clear that as technology creates more of a global environment, learning about each other's cultures won't be just for high-tech manufacturers. We'll all have to learn how to do business with each other.

For more information, contact Etec Systems, 26460 Corporate Ave., Hayward, CA 94545; (510) 783-9210; fax (510) 887-2870; www.etec.com.—**NK**

Fill Up On Burgers And Cash With Smart Cards

Smart cards have landed—at McDonald's? That's the case in Germany, where over 870 of the fast food restaurants already have, or plan to install, smart-card terminals. Customers will now be able to download electronic cash and then turn around and buy fast food or other items.

The ATM may become extinct if more stores and restaurants follow suit. In the chain's first trial with the terminals, they recorded more than 30,000 transactions in just 10 weeks. Taking into account the fact that almost 40 million smart cards are in use in Germany, that's a good start.

The smart cards look like credit cards, but contain an embedded computer chip. Though they've been in use in Japan and Europe, U.S. banks are still experimenting with them. At least some form of the card is sure to come into use here. Visa and Mastercard, for instance, want to replace their magnetic stripe cards with a smart card that handles more functions.

The terminals that McDonald's employs are unique in that they don't require users to load cash at a bank or ATM. Known as the Geldkart system, the terminals are a product of VeriFone, a division of Hewlett-Packard.

A company in the U.K., Schlumberger, has created a new smart card system of its own. Its cards support the JavaCard 2.0 specification and include developer tools that support the PC/SC interface, the standard required for the cards to work in Windows. Plus, the company already unveiled the Cyberflex Open 16k, which boasts twice the memory of previous models.

For school children, Schlumberger makes use of multimemory options by including bus passes on the smart card. Called Easypass, this card lets a single ticket be accepted at different bus companies. This effort should reduce fraud. And, because it's got extra memory, more than one application can be used on each card.

Schlumberger also hit the McDonald's in Quebec, Canada. More than 210 McDonald's there have given members of the Quebec Soccer Federation a sponsorship smart card containing promotional offers. Next year, players and individuals also will receive them. These cards can be used at movie rental and sporting goods stores. Plus, a percentage of all sales made on a card are donated to the member's local club.

It shouldn't be too long before we start seeing smart cards here in the U.S. Previously, concerns have been voiced over privacy in purchasing. But looking at the bus passes and sponsorship cards being created in other countries, it's clear that smart cards stand to offer many positive uses.

To find out more, contact Schlumberger Cards, Carr Rd., Felixstowe, Suffolk IP11 8BY United Kingdom; + 44 (1394) 699200; fax + 44 (1394) 699201; www.schlumberger.com.—**NK**

GREENLOOK

CO_2-Based Stripping Process Cuts Pollution And Water Use

Keep an eye out for semiconductor manufacturers to start reducing water use and hazardous waste volume. The U.S. Department of Energy's Los Alamos National Laboratory worked with the Hewlett-Packard Company, Palo Alto, Calif., to develop a system that removes photoresists from semiconductor wafers without using toxic chemicals. The technique uses a supercritical carbon dioxide fluid formulation to achieve results that are equal to, or better than, conventional acid-based stripping processes.

The selective removal of hardened coatings, or resists, typically uses a "wet-strip" process which employs toxic, corrosive combinations of sulfuric acid and hydrogen peroxide or organic solvents. Both processes produce large quantities of toxic liquids, and require large volumes of ultrapure rinse water to clean the wafer before it's processed further.

The alternative system uses carbon dioxide to remove both positive and negative photoresists. Dubbed the Supercritical Carbon diOxide Resist Remover (SCORR), the process places ordinary CO_2 under high pressure and temperature, transforming it into a "supercritical" phase which gives it useful properties of both gas and liquid. It behaves like a gas, filling its container and diffusing into the tiniest pores of a wafer's surface. But, it has a high density and can dissolve and carry materials like a liquid.

The SCORR system delivers CO_2 mixed with a few percent of polypropylene carbonate, a nontoxic, nonhazardous organic cosolvent. It's passed across the face of the resist-coated wafer using a novel pulsed-flow system. A wafer is stripped in half the time required for wet stripping or alternative chilled ozone systems.

Its developers claim that if adopted by the semiconductor industry, the SCORR system will greatly reduce the costs associated with solvent disposal and water treatment, as well as posing much less hazard to clean room personnel. By using pure carbon dioxide for its final rinse step, it eliminates the need for high volumes of water.

For further information, contact the Los Alamos National Laboratory, P.O. Box 1663, Los Alamos, NM 87545; (505) 667-7000; *www.lana.gov*.

Nonpolluting Polymer-Based Fuel Cells Gear Up To Go Commercial

A small hydrogen tank (about the size of a quart of milk) and a fuel cell from Rensselaer Polytechnic Institute will power your portable fluorescent lantern nonstop for more than 40 hours. "Or you can wear out about 80 D-cell batteries," says Scott Ehrenberg of Dais Corporation, a Rensselaer incubator company that developed the fuel cells in partnership with Rensselaer's New York State Center for Polymer Synthesis.

The Dais "Power-Cell" uses hydrogen and air to create electricity for laptop computers, small TVs, and other portable devices that usually depend on batteries. "Someday soon, fuel cells will power cars and entire homes," says Dais president Timothy Tangredi.

In its smallest size (as big as a half gallon of ice cream), the quiet, air-cooled unit can power multiple devices requiring up to 30 W. Produced commercially, this unit would cost about $200 and last more than 4000 hours, says Ehrenberg. "The only thing you replace is the hydrogen that costs about two dollars a cylinder," he adds.

In July, Dais will unveil a 2500-W unit produced with partial funding from the New York State Energy Research and Development Authority (NYSERDA) and the Wright Malta Corp. Dais is working on a device that generates its own hydrogen from rods or pellets that dissolve in water.

For more information, contact Timothy Tangredi at the Rensselaer Polytechnic Institute, Troy, NY 12180; (813) 942-8353; e-mail: *tnt@dais*.

Lee Goldberg

One-Stop Shopping For Design Equipment?

Here's a dilemma people face every day. A new product is designed. All it needs is to be built so it can be presented, tested, etc. But then, complications like budget and time constraints enter into the scene. In the middle of all of it, someone has to take the time to find the sources for the materials and parts needed to complete the design. Seminar leaders would say this is where time management steps in, but most people just pray some kind of miracle will let them get it all done.

A group of engineers at ThomasNet Inc., New York, N.Y., felt this dilemma was all too familiar and way too common. Their idea to alleviate the situation was a light bulb that would become SoluSource—an interactive sourcing and specifying tool. SoluSource works off of a centralized database, from which users can search actual OEM catalogs to find the information they need.

The products are indexed by hand—a process that extensively details the attributes and functionalities of the OEM products. With an intelligent search engine, SoluSource also lets people use their own words to look for products. Most indexing systems require users to enter their search topic according to a fixed, hierarchical system. SoluSource actually promises to adjust to the user's way of thinking—their word association—in determining the path or subject of the search.

What's pretty convenient is that searches can be done by functionality, not just keyword or product attributes. The user just selects a product, and then has the system check the database. Every product that is similar in function will be listed for the user, which basically puts the alternatives right in view.

Leave it to a bunch of engineers to think of all the little details, promising nice side amenities like easy downloading. The image-cropping feature permits users to only download the information they need. Upon selecting a product, there's an option to download the whole catalog page or just parts of it, such as product features.

SoluSource is kept current by being updated daily. Because the pages consolidate information from many different OEM catalogs, the user can opt to get a customized report, or scrapbook, to compare the specific features of similar products.

Even security has been provided, which should be helpful for those projects hidden "under wraps." It can be customized to protect information transferred over the web, direct dial, or a dedicated line.

SoluSource is available on a subscription basis. It can be accessed from a desktop PC or laptop via the Internet, dial-up or direct lines.

For more information, contact ThomasNet Inc., 5 Penn Plaza, New York, NY 10001; (212) 613-3491; fax (212) 613-3499; www.solusource.com.

—NK

MANAGING THE DESIGN FACTORY

Beware The Zombie Project

They are the unliving and the undead—projects that aren't bad enough to kill, but not good enough to support properly. They are the zombie projects. They lurk everywhere in development organizations. They crawl eerily into our development queues when we aren't looking, and resist all attempts to exorcise them.

Zombie projects aren't harmless little annoyances. They clog up the development process and suck the lifeblood out of the projects that really count. They clutter time reports and management agendas. We try to keep them in the background, but they keep showing up in inconvenient places, tying up resources that we want to use on the important projects.

DON REINERTSEN

Where do they come from? No zombie project is born that way. In its youth, it's an exciting project with real resources. But, things change. Markets shift perversely. Promising technologies renege on their promises. Management's feet start getting chilly. Momentum drops. It's easy to see why zombies aren't adequately supported. But, why don't they die? It would be logical to expect them to go into a quick death spiral. Diminished prospects lead to diminished support, which leads to even more diminished prospects, ad infinitum. The zombie project should implode on itself. But, it doesn't!

If we can understand the strange force that sustains zombie projects, we'll know the secret to killing them. Some cynical engineers believe zombie projects derive their life force from management stupidity. They think their managers are simply too dumb to accept reality. They ignore the fact that, in most cases, it's the engineers themselves that defend the zombie projects to the managers.

The real problem is human psychology. Many years ago, psychologists observed a phenomenon called cognitive dissonance. Their experiments showed that whenever people choose to pursue a course of action, they exaggerate the wisdom of this course. Simply, it's difficult for humans to accept the fact that they're investing time and effort in a worthless endeavor. They deal with the dissonance between their beliefs and actions by altering their beliefs. They start believing that they've invested in something inherently worthwhile.

Since this effect is proportional to the amount of effort invested, the engineers at the lowest level in the organization are most vulnerable to it. As long as we have humans working on projects, they'll kid themselves into believing their zombie project has meaning and value.

This provides the key to killing the zombie projects. We need to undermine the factors that cause this distortion of our reasoning processes. First, review the projects before they've accumulated too much inertia. Since our tendency to distort their value grows with their size, we must kill them when they're small. Second, ensure that zombies are reviewed by people who haven't worked on them. Once you invest in a project, you're unlikely to assess it objectively.

Third, if you kill a zombie project, make sure you nail the coffin shut. If you don't, the lid will slowly creak open and it will reemerge, usually disguised as a real project. Finally, don't stigmatize failure. If killing the zombie includes finding guilty parties and punishing them, people will try to keep their zombies alive as long as possible. It's more attractive to keep the marginal project alive than to acknowledge failure and risk being blamed for it.

So remember, even YOU can kill a zombie project—if you do it right. It's all a question of technique.

Don Reinertsen is a consultant specializing in product development management. He is coauthor of "Developing Products in Half the Time" and author of the new book, "Managing the Design Factory." Reinertsen & Associates, (310) 373-5332; e-mail: DonReinertsen@compuserve.com.

Go Telecommute

The population keeps growing, and America's highways grow narrower and more crowded. People don't want to take that ugly commute into work anymore. Luckily, telecommuting has been born. The question is, can it evolve? Or, can we evolve to the point where we accept it?

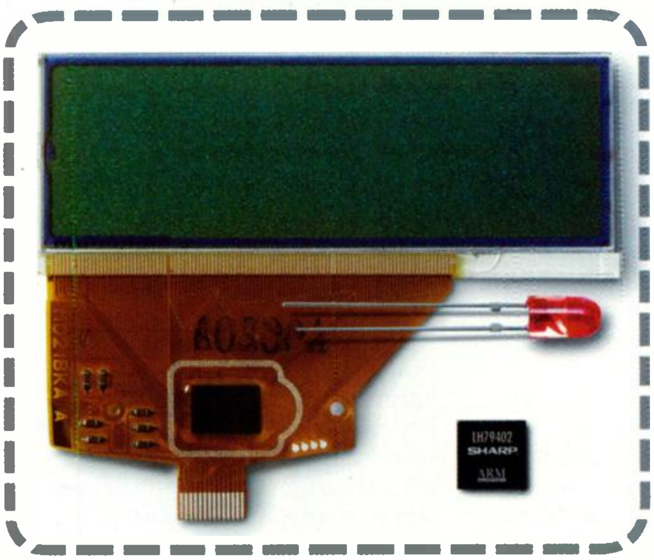
According to a recent article in *Today's Engineer* magazine, "Working@home.com," studies have found that telecommuters have a higher level of satisfaction with both the job and life, as well as increased work productivity (summer 1998 issue, p. 10). But for some reason, many employers still refrain from implementing work-at-home programs.

The author, Trudy Bell, asserts that hidden psychological and cultural barriers must be overcome before telecommuting becomes widely accepted. Bell looks at many companies with telecommuting programs and examines how they deal with issues like worker isolation, educating management and workers on the benefits of telecommuting, and performance concerns.

These things have to be addressed before such a program can be successfully implemented. Organizing things at work can be difficult enough. Companies in this country are typically built on hierarchies. There's a big boss, a medium boss, a little boss, and the employees. Actually, it's more likely to be medium and little bosses. Look around next time someone's trying to get all these people to a meeting.

Then, throw in the element of telecommuting. It's a wild card that people fear. How can things be physically controlled, fully communicated, and even done right if not all participants are present? How does a boss know that his or her employee is being productive and putting in a full day?

The only answer is trust. Telecommuting works. People are happier, their work is better, and they still take care of all the details and messages. Accept telecommuting into our business culture. Trust the employees, trust that it works, and get out of rush hour.—**NK**



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SHARP
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READER SERVICE 129

KMET'S CORNER

This column, and the subsequent installment, will focus on the sale of privately held businesses. Here, I will discuss the details of a sale that actually worked. The follow-up column looks at an attempted transaction that failed to materialize, but came very, very, close to the mark.

RON KMETOVICZ

For many years, the three founders of Company Sold worked within the confines of large Silicon Valley institutions. Through networking and a bit of luck, the three became acquainted. Years passed as each individual performed admirably for their respective employers. But, working for a large corporation began to take its toll as the men completed their fourth decade of existence. They began talking about starting their own business. A few idea grains led to the formation of a business avalanche. The three found themselves owners of a new business, deep in debt, and straining personal net worth. Yet, they also possessed the confidence that they would make it.

One of the three is a friend of mine. This man bet it all on this business. His entire net worth was at risk. And each day, in the early years, much doubt surfaced about succeeding in the endeavor. There was a time when he went for a period of half a year without pay just to keep the business afloat. He and his family endured significant financial hardship. But gradually, the winds of fortune began to blow in a favorable direction.

With each passing quarter, the company grew. Business volume surged each period. To keep up, new employees and equipment were added. Quickly, growth literally caused the company to expand beyond its walls. This made it necessary to add new real estate to the operation. The pace of business became energized with success. By the time a few more years elapsed, the firm sold millions of dollars of products and services each month.

Once again, the owners became restless as they aged another decade.

To initiate the sale of the business, they used a low-key, network approach. There were a few individuals who they thought might want to buy their company. They made contact with them and let them know it was for sale. Telling two led to four, to eight, and eventually to a party interested in buying the business.

This process happened quickly and so fast that the owners were taken by surprise. The sellers quickly hired legal and business advisors to negotiate, specify, and monitor the terms of the sale. In just under two months, the business was sold. My friend sent me the following e-mail announcing the completion of the transaction:

"He's 40-something, he just sold his company, and he was going to sail the South Pacific....But after paying the lawyers, the accountants, the landlord, and everyone else with a handout, he's going to settle for a rubber raft down the Truckee river."

With the sale, two of the three founders moved on to seek new adventure. One remained to lead on the company as a steward to the new owners. Employees, and the management team, felt little from the transaction, except they now owned an interest in a publicly traded company. They reaped their financial reward from working for a startup, and now hold easily traded securities. As for the business, it too continues to grow and prosper, largely attributed to the fact that the business experienced almost no turnover in its talented staff. For now, it looks as though all involved in the transaction won.

Ron Kmetovicz, president of Time To Market Associates, is the author of "New Product Development, Design and Analysis." He helps new product development teams deliver profitable products to the market quickly. He can be reached at: P. O. Box 1070, 100 Prickly Pear Rd., Verdi, NV 89439; (702) 345-1455; fax (702) 345-0804; e-mail: kmetovicz@aol.com.

Bare Die Stays Alive

For those of you worried about chip scale packaging's effect on the bare die market, fret no more. Results from the 1998 "Semi Dice Inc. Bare Die Survey" find the bare die market in safe waters.

Twenty-one major semiconductor companies participated in the study. Of these, a mere 8% predicted that chip scale packaging (CSP) will actually replace bare die. To round out the responses, the survey called upon 27 circuit manufacturers. At 54%, a little more than half asserted that they don't have any plans to replace bare die with CSP. Circuit manufacturers that do want to use CSP instead of bare die checked in at 25%. Yet, they responded with plans to replace only a quarter of the amount of current bare die.

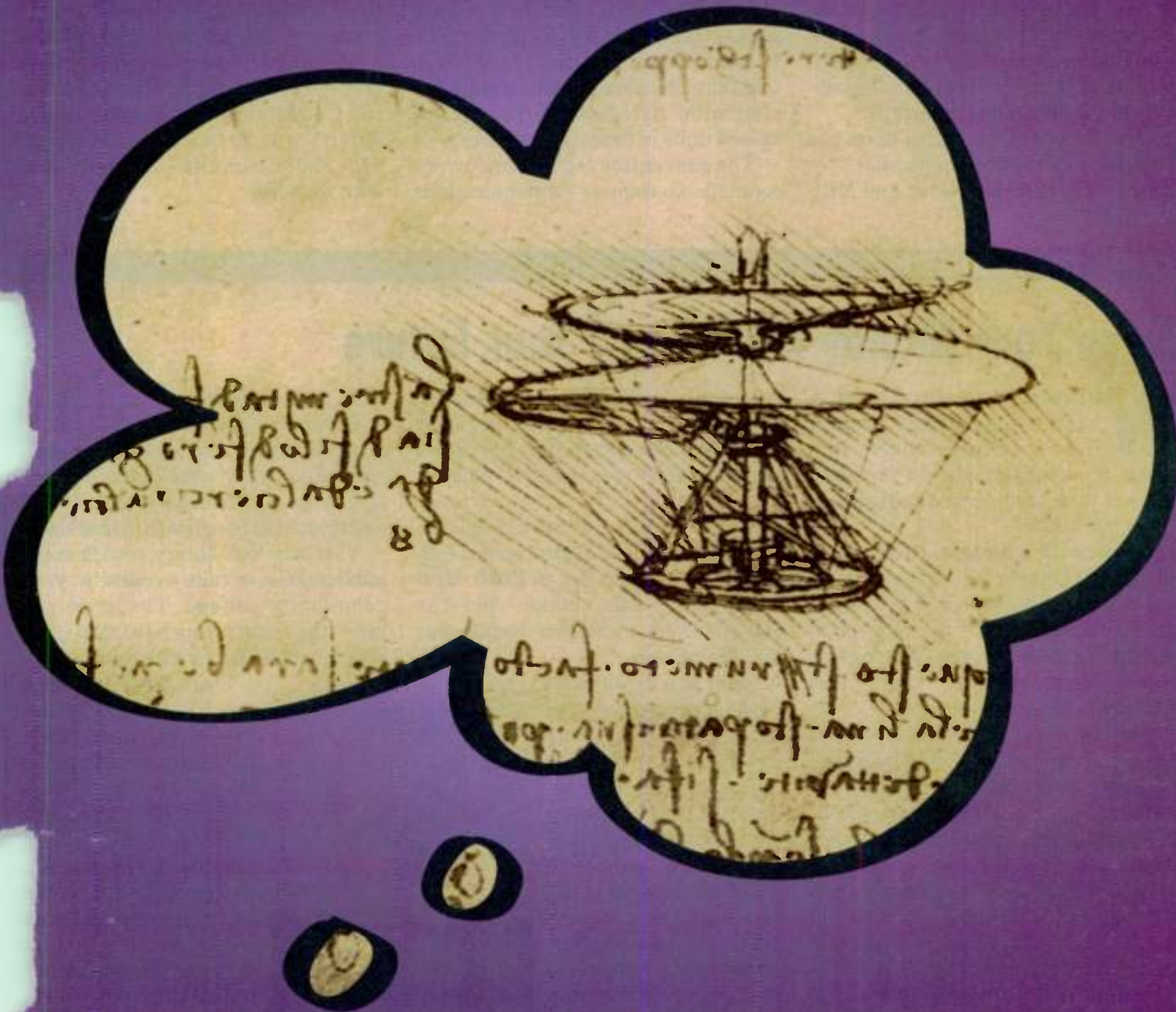
According to Mitch Myers, president and chief operating officer of Semi Dice Inc., bare die is the one and only solution to the quest for smaller packaging. Ideally, no package would be needed. But, Myers insists, nothing could come along that's smaller than bare die.

As in any market, when a technological choice comes along, manufacturers may feel as if they've been left adrift without a compass. Yet, they must make decisions about how much resources to devote to the latest advancement. The only way to stay on course in their industry, however, is usually by changing with the times—adjusting to market needs without sailing into uncharted waters.

The polls reveal that only 25% of semiconductor manufacturers intend to replace surface mount devices. This still doesn't mean great change for the market, though. From that same group, just 8% confirmed plans to replace both bare die and surface mount devices.

The survey also explores the importance of known good die, as well as the present and future outlook for bare die use.

For more information about the survey, contact Semi Dice Inc., 10961 Bloomfield St., P.O. Box 3002, Los Alamitos, CA 90720; (562) 594-4631; fax (562) 430-5942.—**NK**



Disaster Relief Gets Wired

From now until June 21, 2003, an agreement is in effect to expedite disaster relief and humanitarian aid operations. Rather than center on bottled water, canned food, and money, this humanitarian effort reaps the benefits of the electronics industry.

The Tampere Convention on the Provision of Telecommunication Resources for Disaster Relief and Mitigation hosted representatives from 33 countries in Tampere, Finland. The conference's goal was to attain a signed treaty that legally binds countries to facilitate the use of the latest telecommunications equipment by humanitarian agencies and disaster response units in times of emergency.

The convention legally empowers countries to request communications equipment, such as mobile phones an radios, after a natural or man-mad disaster. Most importantly, normal li censing fees and importation restrictions are waived. The equipment arrives immediately, without having to maneuver through any legal red tape.

For more information, contact Mr. Hans Zimmermann, UN Office for the Coordination of Humanitarian Affairs; +41 22 917 3516; fax +41 22 917 0208; e-mail: zimmermann @itu.int.—**NK**

TIPS ON INVESTING

Keep Your Money And Guard Your Future

Work hard. Save for a rainy day. A penny saved is a penny earned. These are all great adages. But, more importantly, how do you keep more of your hard-earned cash and secure your future?

Begin with a budget. Realistically speaking, planning a budget and sticking to it is the best method to achieve your financial goals. It permits you to see the big picture: where your money comes from, where it's going, and where you need to make cuts.

Get out of debt. If you find yourself paying out more than you're taking in, consider consolidating some of your debts into one low-interest account. Even increasing your monthly payments by as little as $10 will get you out of debt sooner and save you money in the long run. This small sacrifice will not seriously affect your lifestyle, but mounting debt surely will.

Tithing is the answer. Pay yourself first. It cannot be over-emphasized. Just as some churches tithe their members by expecting them to donate a percentage of their income, you must tithe yourself with 5 to 10 % of your income. Before you pay a single bill, set aside a specific amount in an account where it will be hard to get.

Set up a cash reserve. Tuck away three to six months income in readily available cash equivalents (like savings accounts or money market funds) to meet any unexpected expense. This emergency reserve will give you the psychological advantage of knowing that the money is there if you need it.

Enroll in a "forced" savings plan. If your company offers a 401(k) or alternative retirement plan, contribute the most you can. For women this is particularly important, since they can expect to outlive their spouses by as much as seven years (source: *The National Center for Health Statistics*, Vital Statistics of the United States, annual estimates for women born in 1990). Usually, you can make pre-tax contributions, thereby reducing your taxable income.

Develop an investment strategy. Are you saving or investing? Saving is accumulating money. Investing is making that money earn more money. Simply putting a portion of your income in low-yielding CDs or money-market funds may not ensure your long-term success or well-being. Although savings and term deposits do earn a fixed amount of interest, you need to put your money into investments that will grow over the long term.

HENRY WIESEL
CONTRIBUTING EDITOR

Educate yourself and your children about money. Using good judgment when it comes to money matters is a lesson your children can learn from you. And, it's one they're likely to carry with them for a lifetime. While most parents don't want to unnecessarily burden their kids with financial worries, it's never too early to begin teaching them good saving and spending habits. Help them start developing practical attitudes toward the value of money and investing.

Before you buy another brand nam product for your son, daughter, or you self, take a look at what that company stocks are worth. Odds are, you've all contributed to the growth of that stock.

Visit your local library, read financial publications, or take a course at your community college. The more you know, the easier it may be to make your investment decisions with confidence.

Start small, but start now! You can begin investing in mutual funds, for example, with as little as $100 or $250 a month. Stick with it for the long term to achiev maximum results. A tual performance cann be predicted, but co sider that $10,000 i vested in mutual func in 1978 would be wort about $150,000 today (assuming a rate of return of 14.5% compounded annually over a 20 year period). Simplicity of investment and a fixed pattern of savings are keys to building your nest egg.

Finally, seek the advice of a skilled, trustworthy professional as you develop your financial plan. Ask questions, and make sure you understand before you invest.

For a free consultation or to get your investment questions answered, write or call Henry Wiesel, vice president qualified plans coordinator at Smit Barney, 1040 Broad St., Shrewsbur N.J. 07702; (800) 631-2221 ext. 8653.

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- 1 - 4 Outputs
- Low Cost

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POWER PRODUCTS

VR SERIES HI-REL SWITCHERS

Single Output • 300-700 Watts

DESCRIPTION

VR Series World Class switching power supplies are a family of single output models designed for applications requiring ***Ultra Reliability*** and ***Low Cost!*** These supplies have actual demonstrated MTBF ratings up to 1 million hours. The time tested design has been continually updated to take advantage of the latest technological improvements in circuits and components resulting in the fine performance of these supplies.

MODELS & RATINGS

Max Power	Output	Model
300W	5V @ 50A	VR300AXX
	12V @ 25A	VR300BXX
	15V @ 20A	VR300CXX
	24V @ 12A	VR300DXX
	48V @ 6A	VR300EXX
500W	5V @ 80A	VR500AXX
	12V @ 40A	VR500BXX
	15V @ 30A	VR500CXX
	24V @ 20A	VR500DXX
	48V @ 10A	VR500EXX
700W	5V @120A	VR700AXX
	12V @ 58A	VR700BXX
	15V @ 46A	VR700CXX
	24V @ 29A	VR700DXX
	48V @ 15A	VR700EXX

FEATURES

- *UL, CSA, TÜV (IEC, EN), CE.*
- *5.5 watts per cubic inch.*
- *80% typical efficiency.*
- *1,000,000 hrs. demonstrated MTBF.*
- *Stock delivery.*
- *Full complement of options.*

VR OPTIONS

Option Code	Function
00	None
01	Power Fail Monitor
02	Auto Ranger
04	Pilot Bias
08	Screen Cover
16	End Fan Cover
32	Top Fan Cover

To order, replace "XX" in model number with sum of Option Codes desired.

CV SERIES ENCLOSED SWITCHERS

Single Output • 360-600 Watts

DESCRIPTION

The CV Series is a line of low profile, fan cooled power supplies which utilize Deltron's field proven V Series components. CV units are single output models in a rugged enclosed package nominally 3 inches in height and 5 inches in width. With power ratings of 360 to 600 watts, these units are a space saving alternative to 5 x 8 inch shoe box modules.

MODELS & RATINGS

Max Power	Output	Model
360W	5V @ 72A	CV360AXX
	12V @ 30A	CV360BXX
	15V @ 24A	CV360CXX
	24V @ 15A	CV360DXX
	28V @ 13A	CV360JXX
	48V @ 7.5A	CV360EXX
500W	5V @ 100A	CV501AXX
	12V @ 42A	CV501BXX
	15V @ 33A	CV501CXX
	24V @ 21A	CV501DXX
	28V @ 18A	CV501JXX
	48V @10.5A	CV501EXX
600W	5V @ 120A	CV601AXX
	12V @ 50A	CV601BXX
	15V @ 40A	CV601CXX
	24V @ 25A	CV601DXX
	28V @21.5A	CV601JXX
	48V @12.5A	CV601EXX

FEATURES

- *UL, CSA, TÜV (IEC, EN), CE.*
- *4 watts per cubic inch.*
- *80% typical efficiency.*
- *200,000 hrs. demonstrated MTBF.*
- *Heavy duty enclosed chassis.*
- *Full complement of options.*

CV OPTIONS

Option Code	Function
00	None
02	Power Fail Monitor
04	Thermal Shutdown
08	Logic Inhibit
16	Auto Ranger

To order, replace "XX" in model number with sum of Option Codes desired.

V SERIES OPEN FRAME SWITCHERS

Single & Quad Outputs • 120-600 Watts

DESCRIPTION

V Series World Class switching power supplies are a family of single and quad output models designed for a wide variety of commercial and industrial applications. These industrial workhorses have demonstrated MTBF ratings greater than 500,000 hours. A proprietary proportional drive circuit prevents excess switch saturation and permits higher switching frequency operation. This makes possible increased reliability and a compact size.

One of the unique features of the V Series is a dual loop regulation system. This system provides a tightly regulated main output and eliminates cross regulation in the auxiliaries.

FEATURES

- *UL, CSA, TÜV (IEC, EN), CE.*
- *4.8 watts per cubic inch.*
- *80% typical efficiency.*
- *500,000 hrs. demonstrated MTBF.*
- *High power auxiliaries.*
- *High peak current capability.*
- *Full complement of options.*

SINGLE OUTPUT

Max Power	Output	Model
120W	5V @ 25A	V120AXX
	12V @ 10A	V120BXX
	15V @ 8A	V120CXX
	24V @ 5A	V120DXX
180W	5V @ 36A	V180AXX
	12V @ 15A	V180BXX
	15V @ 12A	V180CXX
	24V @ 7.5A	V180DXX
250W	5V @ 50A	V250AXX
	12V @ 21A	V250BXX
	15V @ 17A	V250CXX
	24V @ 11A	V250DXX

Max Power	Output	Model
270W	5V @ 54A	V270AXX
	12V @ 22A	V270BXX
	15V @ 18A	V270CXX
	24V @ 12A	V270DXX
360W	5V @ 72A	V360AXX
	12V @ 30A	V360BXX
	15V @ 24A	V360CXX
	24V @ 15A	V360DXX

Other voltages, e.g. 2V, 3.3V, 28V, and 48V available on special order.

Max Power	Output	Model
500W	5V @ 100A	V501AXX
	12V @ 42A	V501BXX
	15V @ 33A	V501CXX
	24V @ 21A	V501DXX
600W	5V @ 120A	V601AXX
	12V @ 50A	V601BXX
	15V @ 40A	V601CXX
	24V @ 25A	V601DXX

QUAD OUTPUT

Max Power	Output 1	Output 2	Output 3	Output 4	Model
225W	5V @ 30A	+12V @ 6(12)A	-12V @ 4A	-5V @ 4A	V225AXX
	5V @ 30A	+12V @ 6A	-12V @ 4A	+24V @ 4(8)A	V225BXX
	5V @ 30A	+15V @ 6(12)A	-15V @ 4A	-5V @ 4A	V225CXX
	5V @ 30A	+15V @ 6A	-15V @ 4A	+24V @ 4(8)A	V225DXX
	5V @ 30A	+12V @ 6(12)A	-12V @ 4A	+12V @ 4A	V225EXX
300W	5V @ 40A	+12V @ 4A	-12V @ 4A	-5V @ 3A	V300AXX
	5V @ 40A	+12V @ 4A	-12V @ 4A	+24V @ 3(5)A	V300BXX
	5V @ 40A	+15V @ 4A	-15V @ 4A	-5V @ 3A	V300CXX
	5V @ 40A	+15V @ 4A	-15V @ 4A	+24V @ 3(5)A	V300DXX
	5V @ 40A	+12V @ 4A	-12V @ 4A	+12V @ 3(5)A	V300EXX
325W	5V @ 45A	+12V @ 8(16)A	-12V @ 6A	-5V @ 4A	V325AXX
	5V @ 45A	+12V @ 8A	-12V @ 6A	+24V @ 4(8)A	V325BXX
	5V @ 45A	+15V @ 8(16)A	-15V @ 6A	-5V @ 4A	V325CXX
	5V @ 45A	+15V @ 8A	-15V @ 6A	+24V @ 4(8)A	V325DXX
	5V @ 45A	+12V @ 8(16)A	-12V @ 6A	+12V @ 4A	V325EXX
400W	5V @ 50A	+12V @ 8A	-12V @ 8A	-5V @ 4A	V400AXX
	5V @ 50A	+12V @ 8A	-12V @ 8A	+24V @ 4(6)A	V400BXX
	5V @ 50A	+15V @ 8A	-15V @ 8A	-5V @ 4A	V400CXX
	5V @ 50A	+15V @ 8A	-15V @ 8A	+24V @ 4(6)A	V400DXX
	5V @ 50A	+12V @ 8A	-12V @ 8A	+12V @ 4(6)A	V400EXX
500W	5V @ 60A	+12V @ 10A	-12V @ 10A	-5V @ 5A	V500AXX
	5V @ 60A	+12V @ 10A	-12V @ 10A	+24V @ 5(8)A	V500BXX
	5V @ 60A	+15V @ 10A	-15V @ 10A	-5V @ 5A	V500CXX
	5V @ 60A	+15V @ 10A	-15V @ 10A	+24V @ 5(8)A	V500DXX
	5V @ 60A	+12V @ 10A	-12V @ 10A	+12V @ 5(8)A	V500EXX
600W	5V @ 80A	+12V @ 10(20)A	-12V @ 10A	-5V @ 5A	V600AXX
	5V @ 80A	+12V @ 10A	-12V @ 10A	+24V @ 5(10)A	V600BXX
	5V @ 80A	+15V @ 10(20)A	-15V @ 10A	-5V @ 5A	V600CXX
	5V @ 80A	+15V @ 10A	-15V @ 10A	+24V @ 5(10)A	V600DXX
	5V @ 80A	+12V @ 10(20)A	-12V @ 10A	+12V @ 5A	V600EXX

V OPTIONS

Option Code	Function
00	None
01	OVP protects all auxiliaries
02	Power Fail Monitor
04	Thermal Shutdown
08	Cover
16	Logic Inhibit
32	Post Regulator for output 4

To order, replace "XX" in model number with sum of Option Codes desired.

NOTES:

1. *Numbers in parentheses ( ) are peak ratings for short duration service such as motor starting.*
2. *Output 1 is floating and can be either polarity.*
3. *Quads require 10% of maximum power distributed among auxiliary outputs for optimum performance.*
4. *Outputs can operate to no load with slight increase in specifications.*

SPECIFICATIONS

INPUT
90-132 VAC or 180-264 VAC, 47-440 Hz.
Consult factory for 400 Hz. operation.

EMISSIONS
FCC 20780 Part 15/EN 55022, Class A Conducted.
EN 61000-3-3, Voltage Fluctuations.

IMMUNITY
IEC 1000-4-2/EN 61000-4-2, Electrostatic Discharge.
IEC 1000-4-3/EN 61000-4-3, Radiated Field.
IEC 1000-4-4/EN 61000-4-4, Electrical Fast Transients.
IEC 1000-4-5/EN 61000-4-5, Level 3 Surge.
IEC 1000-4-6/EN 61000-4-6, Conducted Field.

INPUT SURGE
17 amps peak from cold start for models up to 250 watts and VR300, 68 amps for other models, from nominal 110 or 220 VAC.

EFFICIENCY
80% typical.

HOLDUP TIME
20 milliseconds after loss of nominal AC power.

OUTPUTS

See table of models.

LINE REGULATION
±0.1% for line change from nominal to min. or max. rating with 20% min. load on the measured output.
±0.05% with post regulator and no min. load.
Singles to no load.

LOAD REGULATION

5V main/singles	±0.2%
-5V aux.	±3%
±12V aux.	±2%
±15V aux.	±2%
+24V aux.	±1.5%

Post Regulated Outputs
Option 32 ±0.05%

for load change from 60% to 20% or 100% max. rating. With post regulator to no load. Singles to no load.

CROSS REGULATION
±0.2% for load change on the main 5V output from 75% to 50% or 100% max. rating with 20% min. load on the measured output.
±0.05% with post regulator and no min. load.
Not applicable to singles.

CENTERING

5V main/singles		±5% trim adj.
Aux. 1 and 2		±5% trim adj. tracking
Aux. 3:	-5V	±3%
	+12V	±2%
	+24V	±1%

with all outputs loaded to 50% max. ratings and output #2 set precisely at its rated value. With post regulator ±3% trim adj.

RIPPLE & NOISE
1% or 100 mV, pk.-pk., 20 MHz bandwidth.

OPERATING TEMPERATURE
0-70°C. Derate 2.5%/°C above 50°C.

COOLING

Models	Forced Air
V120, V180, V225, V250, V270, V300, VR300, V360	30 CFM
V325, V400, V500, VR500, V501, V600, V601, VR700	60 CFM

TEMPERATURE COEFFICIENT

5V main/singles	±0.02%/°C
Auxiliaries	±0.05%/°C
With post regulator	±0.02%/°C

DYNAMIC RESPONSE
Peak transient less than ±2% or ±200 mV for step load change from 75% to 50% or 100% max. ratings.

RECOVERY TIME
Less than 400 microseconds on main/singles output.
Less than 50 microseconds on post regulated auxiliaries.

SAFETY
Units meet UL 1950, CSA 22.2 No. 950, EN 60 950, IEC 950.

DIELECTRIC WITHSTAND
3750 VRMS input to ground.
3750 VRMS input to output.
700 VDC output to ground.

SPACING
8 mm primary to secondary.
4 mm primary to grounded circuits.

LEAKAGE CURRENT
0.75 mA at 115 VAC, 60 Hz. input.

INPUT UNDERVOLTAGE
Proprietary proportional drive and low voltage lockout protects against damage for undervoltage operation.

SOFT START
Units have soft start feature to protect critical components.

OVERVOLTAGE PROTECTION
Standard on main output/singles. Optional on auxiliaries.

REVERSE VOLTAGE PROTECTION
All outputs are protected up to load ratings.

OVERLOAD
Outputs short circuit protected by current foldback with automatic recovery. Post regulators have individual current foldback protection.

REMOTE SENSING
On singles/5V mains which are fully isolated from all auxiliaries.

SHOCK & VIBRATION
Shock per MIL-STD 810-E Method 516.4, Procedure I.
Vibration per MIL-STD 810-E Method 514.4, Category 1, Procedure I.

MECHANICAL

MODELS	H	x	W	x	L
VR300	2.50"	x	4.85"	x	8.50"
VR500, VR700	2.75"	x	4.85"	x	10.50"
CV360, CV501, CV601	3.15"	x	4.85"	x	12.63"
V120, V180, V250	2.50"	x	4.75"	x	8.50"
V270, V360, V501, V601	2.50"	x	4.75"	x	10.50"
V225, V325	2.50"	x	5.00"	x	10.50"
V300, V400, V500, V600	2.75"	x	5.00"	x	13.00"

OPTIONS & ACCESSORIES

POWER FAIL MONITOR
Optional monitor provides a TTL signal 2 ms. min. prior to loss of output power with outputs fully loaded from 100VAC/200VAC line loss.

THERMAL SHUTDOWN
Special circuit cuts off supply in case of local over temperature. Unit resets automatically when temperature returns to normal. Standard on VR Series. Optional for CV and V Series.

COVERS
Optional end and top fan covers for VR Series.
Optional safety/EMI cover for V Series.

INHIBIT
TTL logic inhibit input. Standard for VR Series. Optional for CV and V Series.

PILOT BIAS
Optional for VR Series only. SELV 5V @ 1A source for external use with provision for operating the inhibit either with a switch or TTL Logic. Either NO or NC can be selected.

AUTO RANGER
Special circuit provides automatic operation at specified input ranges without strapping. Optional for VR and CV Series. For V Series specify AR-1 accessory.

POST REGULATOR
Optional for output #4 on V300, V400, V500, V600 models. Ratings available are -5V @ 4A, +12V @ 3A, or +24V @2A.

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The Low-Voltage Limbo Saga: Operating Voltages Continue To Drop

As Densities Increase, New Circuit Techniques And Processes Come Online To Reduce Operating Voltage And Power Drain.

Dave Bursky

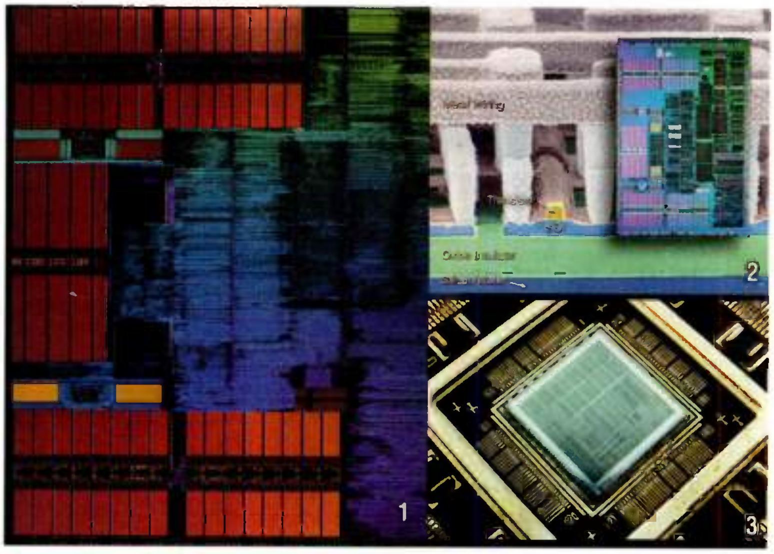
SPECIAL REPORT

As designers push to create more complex logic circuits, power consumption becomes critical. One of the first remedies for trimming power drain is to lower the limbo bar of the supply voltage. That change provides one of the largest benefits, since power consumption is directly proportional to the square of the supply voltage. The first major step in this direction was taken several years ago when designers starting moving to 3.3-V supply levels from the decades old 5-V standard. Currently designers are lowering the bar again, decreasing the supply voltages from 3.3 V to the next standard, 2.5 V.

As circuit operating speeds escalate to achieve higher performance, power-consumption levels continue to rise. Still lower operating voltage levels will be needed. Designers are looking toward a horizon filled with operating voltages of 1.8 V and lower. To achieve those levels, additional circuit techniques and process tricks must be brought forth.

In the past, lowering the operating voltage usually resulted in a trade-off in performance. As the voltage went down, so did the maximum operating clock frequency. Thus the maximum operating clock frequency of 5-V circuits, when powered by 3.3-V supplies, typically had to be derated because the process used to fabricate the circuits was optimized for operation at 5 V.

That has completely changed over the last few years as semiconductor manufacturers revamped their processes, fine tuning them for optimum performance at 3.3 V. CPU manufacturers, such as Advanced Micro Devices Inc. and National Semiconductor Corp. (which acquired the CPU manufacturer Cyrix Corp.), also jumped into the rink. Their fine tuning lead to chips using dual power supplies—typically 3.3 V for the I/O circuits and a lower supply, say 2.8 or 2.9 V, for the logic circuits in the CPU core and memory blocks.



Art Courtesy: Clockwise from left, **1.** Motorola's 1.9-V MPC750/740 PowerPC microprocessor; **2.** IBM's SOI version with a copper die insert; and **3.** Honeywell's HX30001.8-V SOI gate-array.

Voltages lower than this are in the offing as Intel Corp. fabricates its next-generation Xeon and future processors with supply voltage levels of just 1.6 V. And, both IBM Corp. and Motorola have crafted 1.9-V versions of the PowerPC 750 microprocessor to target the mobile computer and embedded-systems markets. Running at 1.9 V and 300 MHz, the PowerPC 750 consumes less than half the power of its 2.6-V predecessor *(see the opening illustration)*.

Lower The Bar Again

Look for the limbo bar to drop even further with the introduction of next-generation processors: the UltraSPARC III from Sun Microelectronics Inc., the Alpha processor now being developed by Compaq Computer Corp., Houston, Texas, and others. These companies plan to power their next-generation processors from supplies as low as 1.8 V. Operating at such low voltages isn't new. Low-speed watch chips and other moderate-performance circuits have been operating from sub-2-V supplies for several years. Such circuits were optimized for low power, however, not high speed. With chips like the UltraSPARC III, optimized to deliver peak throughput at 600 MHz or so, operating at such low voltages wasn't really practical until now.

Just as lowering the operating voltage reduces power consumption, using smaller feature sizes to fabricate more complex chips demands lower voltages. With feature sizes dropping below 0.2 µm, designers must reduce the high electrical-field stresses that arise due to the thin oxide layers and shallow junctions used to build the high-speed transistors. As the power-supply voltage goes down, however, so must the threshold voltages (V_Ts) of the transistors themselves to improve their switching characteristics. But, as threshold voltages drop, leakage currents can increase due to sub-threshold effects. Those same sub-threshold effects, which appear detrimental, can be leveraged to create high-performance circuits *(see "Leveraging Sub-Threshold Logic," p. 68)*.

Dual Thresholds

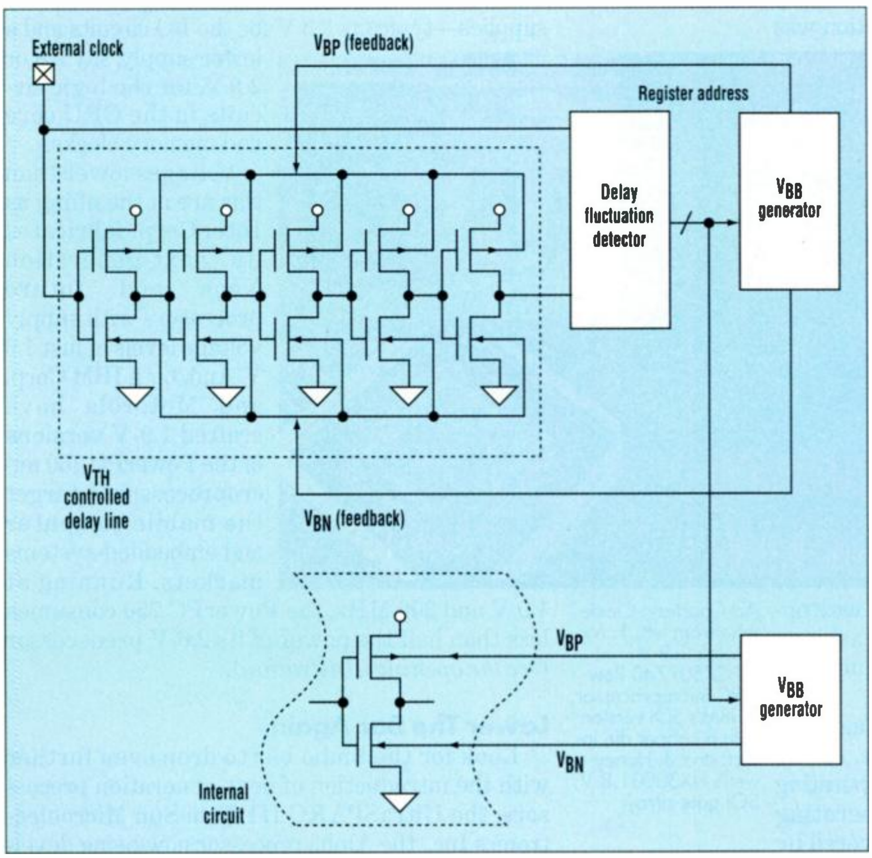
To counter that problem, many designers are researching schemes that use dual threshold voltage levels. In some approaches, both low- and high-threshold devices are fabricated and used in different portions of the circuit. In other schemes, low-threshold-voltage devices are used when the circuit is active. High-threshold-voltage devices are then switched in when the circuit goes into its standby mode. These techniques and others were the subject of many papers presented this past August at the IEEE International Symposium on Low Power Electronics and Design that was held in Monterey, Calif.

In a paper presented by Hitachi Ltd., Tokyo, Japan, in Session M3, designers created a speed-adaptive, threshold-voltage CMOS structure. The substrate bias in this structure is controlled so that the delay in the circuit stays constant. This constant delay reduces the fluctuation in operating frequency and boosts the worst-case operating frequency from 20 to 55 MHz in a test circuit used by the researchers.

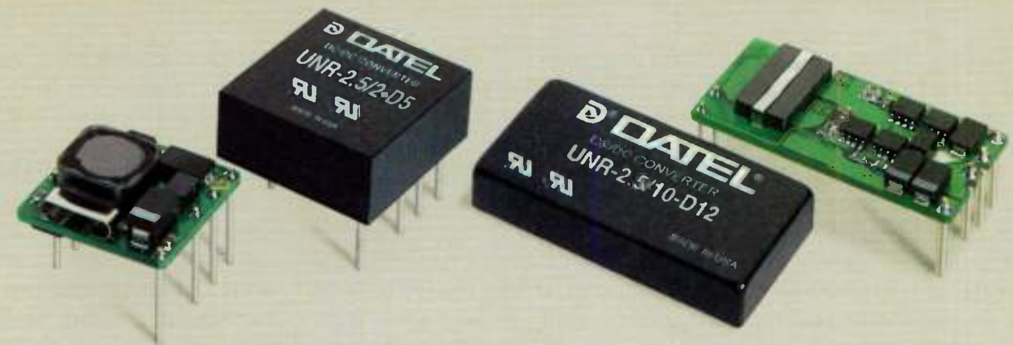
To control the bias, the circuit consists of a delay line controlled through the threshold voltage, a delay-fluctuation detector, and a substrate bias generator *(Fig. 1)*. The delay of the 200 series connected inverters in the delay line is managed through the substrate bias. The delay-fluctuation detector measures the delay from an external clock signal to an output signal of the delay line, converting the amount of delay into a register address. The substrate bias generator supplies the substrate bias voltages to the delay line and internal circuits according to the register address. When the delay of the delay line corresponds to the external clock, the delay-fluctuation detector and the bias generator form a stable feedback loop.

In an opening keynote address, Dr. Christer Svensson of Linkoping University, Sweden, examined digital-circuit techniques for low-power systems. He found significant differences in power consumption versus delay characteristics for different forms of dynamic latches. Different but equivalent logic structures also show significantly different power/delay characteristics. In comparing static CMOS to complementary pass-transistor logic (CPL), it was found that for some logic structures—ExOR and adders—CPL seems better. But, for larger logic functions, static CMOS appears to have the performance edge.

One of the highest-performance, low-voltage logic presentations at the symposium was prsented by researchers at the Institute of Microelectronics, Stuttgart, Germany. A paper in Session P1 provided details on a novel T-gate transistor structure prepared with silicon-on-insulator (SOI) technology. The 50-nm gate widths employed by the T-gate devices were leveraged by designers to craft an 8-by-8-bit multiplier that performs 150 million multiplies per second at an energy level of only 30 fJ when powered by a supply voltage of just 0.5 V. The circuit structure is based on a novel



1. This speed-adaptive, threshold-voltage control scheme developed by Hitachi uses a chain of 200 inverters and a delay-fluctuation detector to control the substrate bias generator, thus controlling operating-frequency fluctuation. That results in a significant improvement in the worst-case operating frequency of the circuit employing the control scheme.



2.5 Volt DC/DC Converters

Invest Design Time in Signal Processing...Not Power Processing

As the supply voltage of new CPU's, ASIC's and DSP's drops below 3.3V and reliable off-the-shelf power supplies become harder to find, you're tempted to design your own. Don't waste your time? The small size, high efficiency, ease-of-use, and affordable pricing of DATEL's new 2.5V UNR Series tilts the make-vs.-buy decision to buy. Evaluate one now.

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- **+2.5V (±25mV), 2-20 Amp outputs**
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- **V_{OUT} factory adjustable down to 1.5V**
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V_{OUT} ① (Volts)	I_{OUT} (Amps)	Input Range (Volts)	Ripple/Noise (mVp-p) ②	Efficiency (%)	Package Size (Inches)	DATEL Model Number	Data Sheet @ www.datel.com	Price (OEM, USA)
2.5	2	4.75-5.5	30	85	1 x 1 x 0.45	UNR-2.5/2-D5	UNR, 5W	$22
2.5	8	4.75-5.5	40	90	2 x 1 x 0.385	UNR-2.5/8-D5	UNR, 20/25W	$33
2.5	8	10.4-13.6	60	88	2 x 1 x 0.385	UNR-2.5/8-D12	UNR, 20/25W	$33
2.5	10	4.75-5.5	40	89	2 x 1 x 0.385	UNR-2.5/10-D5	UNR, 20/25W	$33
2.5	10	10.4-13.6	60	86	2 x 1 x 0.385	UNR-2.5/10-D12	UNR, 20/25W	$33
2.5	12	4.75-5.5	40	89	2 x 1 x 0.45	UNR-2.5/12-D5	UNR, 30W	$36
2.5	20	4.75-5.5	50	88	2 x 2 x 0.45	UNR-2.5/20-D5	UNR, 50W	③

① All devices guarantee ±25mV accuracy under nominal line voltage and full-load conditions. Output voltage is factory adjustable down to 1.5V.
② The UNR-2.5/2-D5 requires no exterenal I/O caps to achieve specified performance. All others require a 470µF, low-ESR C_{IN} and a 22µF C_{OUT}.
③ Preliminary product information. Contact DATEL for details.

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Hiperlogic 8-bit adder, which employs a differential Manchester carry chain for its inherent speed and noise immunity *(Fig. 2)*.

Signal Levels Also Decrease

As operating voltage levels go down, so must the I/O signal levels. IC chips that operate at power-supply voltages 2.5 V or less can no longer readily support conventional TTL I/O levels. For instance, circuits targeted for 2.5-V operation typically offer I/O voltage levels that are compatible with 2.5 and 3.3 V.

Reducing the I/O voltage levels to better deal with these lower supply voltages is only part of the challenge with I/O buffers. Faster switching speeds also require smaller signal swings so the buffers can switch faster. A plethora of I/O standards results, comprising a veritable alphabet soup of acronyms that define the standards' signaling characteristics. This in turn means ASICs and field-programmable logic must include a wide array of I/O buffer options as part of their design libraries.

Even in today's PCs, you can find three or four different types of signal interfaces at work. Synchronous DRAMs typically employ some form of series stub-terminated logic (SSTL) interface (there are at least three SSTL variations). Some CPU chips use a form of Gunning transistor logic (GTL+). Motherboard logic chips usually support GTL+, SSTL, and both PCI and advanced graphics port interfaces. The GTL+ interface generally utilizes a 1-V reference level, while SSTL variants operate with reference voltages of 1.1, 1.32, or 1.5 V. AGP ports use a 1.32-V reference level. All of these signal levels are worlds away from the basic TTL and LVTTL signal levels on which most seasoned designers grew up.

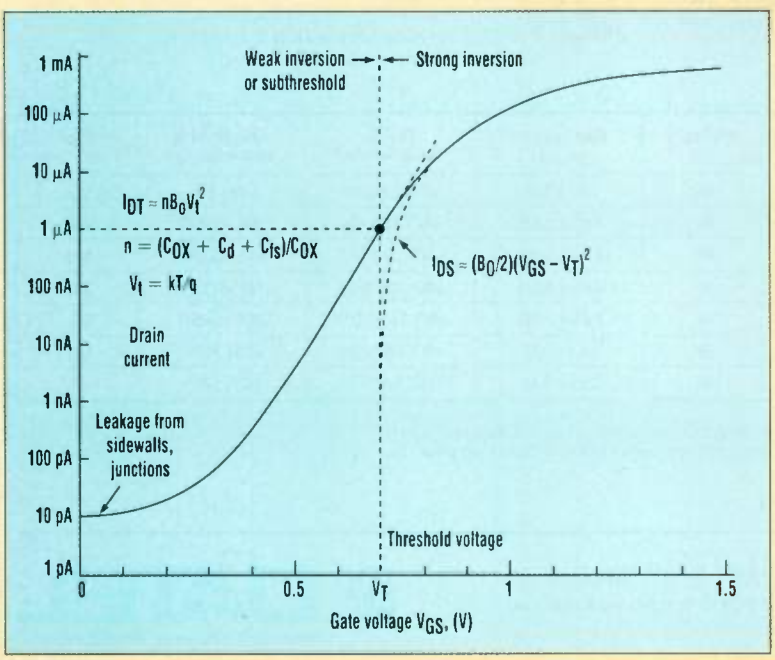
Rekindled Interest In SOI

Implementing high-performance circuits that can operate at low-voltage levels is the key to any of the systems. To reach that goal, designers have been focusing most of their efforts on standard, deep-submicron CMOS technology. Alternative approaches such as silicon on insulator have existed for many years. But, they were considered too expensive and not production worthy enough for the large-area processors and other logic chips of just a few years ago.

But now, SOI technology is coming into its own. It can deliver higher-performance circuits, as well as circuits that operate at much lower power levels. That's because SOI eliminates

Leveraging Sub-Threshold Logic

Since the energy consumed for signal processing remains in proportion to the capacitances involved and to the square of the voltage swing, reducing the voltage swing effectively minimizes the energy consumption of CMOS circuits. Although CMOS logic circuits are quite tolerant to low supply voltages, the available switching currents are also reduced, resulting in slower switching speeds. A common belief is that CMOS logic circuits become exceedingly slow if voltage swings and the supply voltage approach the magic level of two or even one transistor threshold voltage, V_T. According to Dr. Bernd Hoefflinger, a professor at the Institute for Microelectronics, Stuttgart, Germany, this has led to a general trend of staying well above $2V_T$ for the supply voltage and signal swings. This is achieved by lowering V_Ts or bootstrapping the circuits for higher signal levels. Also, at lower V_T levels, transistor currents are considered leakage currents and are detrimental to desired circuit operation.



There is, however, a sophisticated class of CMOS circuits designed to operate at supply voltages of just $2V_T$, V_T, and lower. The electric watch industry and CMOS watch circuits emerged in the late 1960s and operated in this regime. Designers of those circuits accumulated much now-neglected know how. With the reputation of CMOS gates in watches only switching once every four years, this domain has received little attention by the VLSI community. Although a low-voltage watch transistor in 1970 may well have had an intrinsic delay time of 1 µs, the general progress in VLSI technology offers scaled transistors with delay times of less than 100 ps at a few hundred mVs.

According to Dr. Hoefflinger, the MOS transistor at a gate voltage below V_T more closely approaches the ideal transistor with a transconductance equal to its drain current divided by a thermal voltage, V_t (25 mV at room temperature). Due to the exponential current-voltage characteristics of a MOS transistor in the subthreshold mode, the MOS devices in the late 1960s were called "bipolar transistors in dis-

(continued on page 70)

We hate the fact we had to resort to advertising to sell our Flash ChipSets.

(Intel, Toshiba and Samsung are pretty bummed, too.)

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FOR CLIENT APPROVAL

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Date

A message from the president:

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More Memory. More Possibilities.

(As the ad agency for SanDisk, we'd like to warn other agencies that these guys are so obsessed with making great Flash ChipSets, they'll never do a good ad.)

many detrimental parasitic elements that occur in standard bulk CMOS processes. Silicon implantation of oxygen (SIMOX) is one form of SOI technology that's gained a strong foothold. This process implants oxygen atoms produced by a high-energy ion implanter to form a buried layer. The oxygen atoms then combine with the silicon to form a buried insulating layer of silicon dioxide.

The latest version of this SOI process features a second wafer with a standard deposited silicon-dioxide coating. This wafer bonds to the silicon surface of the one that's implanted. Afterwards, the implanted wafer is "fractured" at the "weaker" implanted silicon-dioxide layer. The bonded layer left on the second wafer is then polished and used as the active layer—the one in which the circuits are fabricated. The fractured wafer also is repolished and used as the "second" base wafer, to be bonded to the next implanted wafer.

The resulting bonded silicon wafer provides an ideal isolated silicon layer in which to form high-performance circuits. Both IBM and Honeywell Inc., as well as many other companies, have developed SOI processes in which they fabricated complex circuits, such as PowerPC microprocessors and megagate arrays. IBM already announced it will offer an SOI version of the PowerPC at a minimal price premium over the standard bulk devices. Although forming the wafer is a bit more complicated than with a bulk wafer, the SOI layer permits the simplification of subsequent fabrication steps. In full-scale production, the cost of the final SOI chips should be comparable to bulk circuits.

Targeting aerospace applications, designers at Honeywell crafted both gate arrays and a static RAM using a similar SOI process. Their latest offering, the HX3000 series, will offer options for supply voltages of 3.3, 2.5, or 1.8 V. The 1.8-V option trims the active power of a gate to less than 23 nW/MHz—one of the lowest power numbers to date *(see the opening illustration)*. With the SIMOX process, circuits operate 1.5 to 2 times faster than bulk silicon circuits at comparable power levels.

The SOI technology also brings other benefits: no latch-up performance, a 10 to 20% better transistor-packing density relative to bulk CMOS, and no soft errors due to alpha-particle strikes. And, circuits fabricated with the SOI technology work at elevated temperatures. Honeywell's HX3000 series, for example, can operate at temperatures up to 225°C.

(continued from page 68)

guise." In the early 1970s, researchers showed CMOS inverters operating down to 100 mV (about four thermal V_t levels), proving that this mode allows the lowest energy for information processing in an electronic system at room temperature.[1]

The drain current in the sub-threshold mode flows across the source-to-channel barrier much like the current that flows across the emitter-to-base barrier in a bipolar transistor. The appearance is similar because the source-to-channel barrier is lowered not only by the gate bias, V_{GS}, but also by the drain bias. Designers can model and evaluate the threshold current, I_{DT}, by extending the sub-threshold and above-threshold continuous model concept for MOS transistors published in 1984 by Vittoz, Grotjohn, and Hoefflinger.[2] In the model extension, the familiar above-threshold or strong-inversion model yields zero drain current as the gate-source voltage approaches V_T. As seen in the figure, the real current is approximately:

$$I_{DT} \sim n{*}Bo{*}V_t^2$$

where

$n = (C_{OX} + C_D + C_{FS})/C_{OX}$ where FS are fast interface states

Bo = transistor constant of (mobility ↔ oxide capacitance Co)/L2 where L is the gate length

$V_t = kT/q$ where k is Boltzman's constant

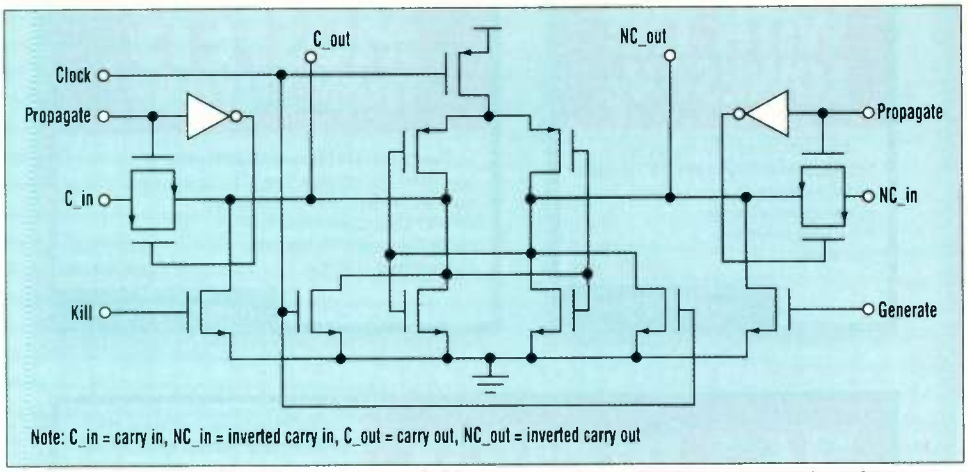
This threshold current, I_{DT}, at the top of the exponential sub-threshold regime, is a good reference to assess the usability of the sub-threshold regime for low-energy, high-performance CMOS logic. As the transistors' effective channel length began decreasing from 20 µm to 80 nm over the generations of technology, the threshold current has steadily increased from about 1 nA/µm in 1970 to almost 1 µA/µm today. At this rate, it's bound to hit 10 µA/µm for 2010. The extremely short effective channel length of less than 80 nm of a novel T-gate transistor offers a high I_{DT}—well beyond 1 µA/µm—with a minimal capacitance that's free from fringing parasitics. That results in an internal delay time of less than 50 ps at a voltage level of just 400 mV. The T-gate structure was described this past August by the Institute for Microelectronics, Stuttgart, Germany, at this year's International Symposium on Low Power Electronics And Design, Monterey, Calif.

To boost the threshold current even further, connect the gate and channel, thus operating the transistor in a hybrid model. The result is the parallel action of a MOS transistor and a bipolar transistor, best described by a body bias that lowers the threshold voltage as the gate-source voltage increases. This operating mode effectively doubles the I_{DT} value. And at lower currents, it may offer an order-of-magnitude improvement over a transistor that has its channel tied to the source.

With use and the significant future potential, circuits with sub-threshold MOS transistor operation probably won't stay confined to slow watches. They'll be too busy offering ultimate merits in high-speed circuits, like several hundred megahertz operation at minimal energy levels.

For more information, contact Dr. Hoefflinger via e-mail at hoefflinger@mikro.uni-stuttgart.de.

1. Meindl, J.D. and Swanson, R.M., "Fundamental Performance Limits of MOS Integrated Circuits," *Proceedings of the IEEE International Solid-State Circuits Conference*, 1975; pp. 110-111.
2. Grotjohn, Tim and Hoefflinger, Bernd, "A Parametric Short-Channel MOS Transistor Model for Subthreshold and Strong Inversion Current," *IEEE Journal of Solid*



2. Fabricated using novel T-gate transistors and able to operate from a 0.5-V supply, an 8-by-8-bit multiplier created by the Institute for Microelectronics employs this differential Manchester carry-chain adder building block. This building block has good noise immunity and can operate at high clock speeds.

Currently, Honeywell offers both a 256-kbit and a 1-Mbit SRAM fabricated with the SOI technology. Next year, the company expects to start sampling a 4-Mbit memory.

Designers at Synova, a customer of Honywell, have implemented a radiation-hardened 32-bit RISC processor fabricated in the previous 0.35-µm version of the process. Called the Mongoose-V, it's based on the MIPS R3000 architecture. The chip combines 150 kgates of logic and embedded memory (both cache and RAM). When powered by a 5-V supply, the chip consumes less than 1 W. The company plans to migrate the design to the HX3000 gate-array family and estimates that power consumption will drop to just 100 mW when powered by a 3.3-V supply.

Although it won't employ SOI technology, a second-generation CMOS process targeted at communications applications was recently unveiled by Lucent Technologies Inc. The COM-2 process, expected to go into volume production in the first half of 2000, allows circuit operation at supply voltages of 3.3, 1.5, and 1.0 V. In its transition from a 0.25-µm to the latest 0.16-µm process, Lucent designers have continuously improved circuit-packing density and speed while drastically reducing power consumption per gate *(Fig. 3)*.

High Packing Densities

At such low power-supply levels, the power per gate level is very low—just 4.3 nW/gate/MHz. That allows very high packing density and the fabrication of circuits with up to 40 million usable gates (160 million transistors). To achieve the low operating voltages, designers at Lucent Technologies trimmed the transistor threshold voltages from the 500 mV used for 3.3-V devices to just 250 mV for the 1.5-V transistors.

Companies Mentioned In This Article

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www.amd.com
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www.fairchildsemi.com
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Microelectronics Division
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Endicott, NY 13760
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www.ibm.com
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Institute for Microelectronics
Allmandring 30a
D-70569 Stuttgart, Germany
(49) 711-685-5778
Contact Volker Dudek at
dudek@ieee.org
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Linkoping University
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Linkoping, Sweden
(46) 13-281-223
Contact Christer Svensson at
chs@ifm.liu.se
CIRCLE 492

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To implement complex high-performance functions such as DSP chips, the process permits such circuits, when powered by a 1.5-V supply, to deliver 250 MIPS and yet consume just 0.25 mW/MIPS. With a 1-V power supply, the top performance level drops to 150 MIPS and power goes down to 0.11 mW/MIPS.

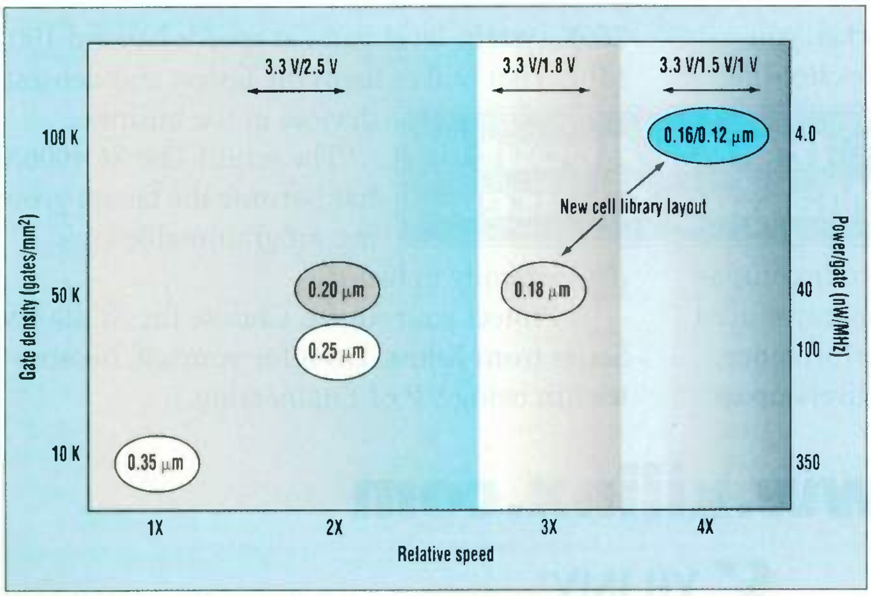
The COM-2 process is based on 0.16-µm (drawn) design rules. For performance-critical requirements, it offers a special 0.12-µm fast-gate option. Up to six levels of metal interconnections can act as joiners between all the devices on the chips. The process also includes an option for biCMOS circuits that operate at power-supply voltages of 3.3 V and deliver top cutoff frequencies of more than 50 GHz.

The COM-2 process has the unusual ability of allowing the integration of high-Q inductors (Q values greater than 10) and metal-oxide-metal capacitors on the chip. These two elements are key building blocks for communications systems and the eventual goal of a single-chip radio. That single chip would incorporate the digital baseband processing, the high-frequency RF circuitry (filters, low-noise amplifiers, and mixers/voltage-controlled oscillators), and additional custom logic.

Another major player in the communications market, Motorola Inc., has been developing many low-power circuits for cellular communications, paging, and personal digital assistants (PDAs). These are just a few of the applications well suited to low-voltage and low-power circuits. Motorola's designers have been researching a special graded-channel transistor structure that promises adequate circuit performance for pager and other battery-powered applications that must function with a power-supply voltage as little as 1 V.

Although they've demonstrated a 1-V DSP chip to show the feasibility of such low-voltage logic, researchers at Texas Instruments Inc. don't expect such circuits to be practical until the next century. Mainly, that's because there are few circuits, if any, with which the 1-V processor could communicate. In addition, boosting the I/O levels up to 2.5 or 3.3 V is counterproductive for such a low-voltage circuit, since the I/O circuitry would consume significantly more power than the processor.

That's not to say that designers at Texas Instruments aren't pushing forward. Last month, the company released what it claims are the world's lowest-power DSP chips based on the company's 0.18-µm process. The TMS320C5420 DSP chip can deliver a throughput of up to 200 MIPS, with a power consumption of less than 120 mW when powered by a 1.8-V supply. A slightly less powerful version, the TMS320C5402, provides a throughput of 100 MIPS, but trims power consumption to 58 mW.



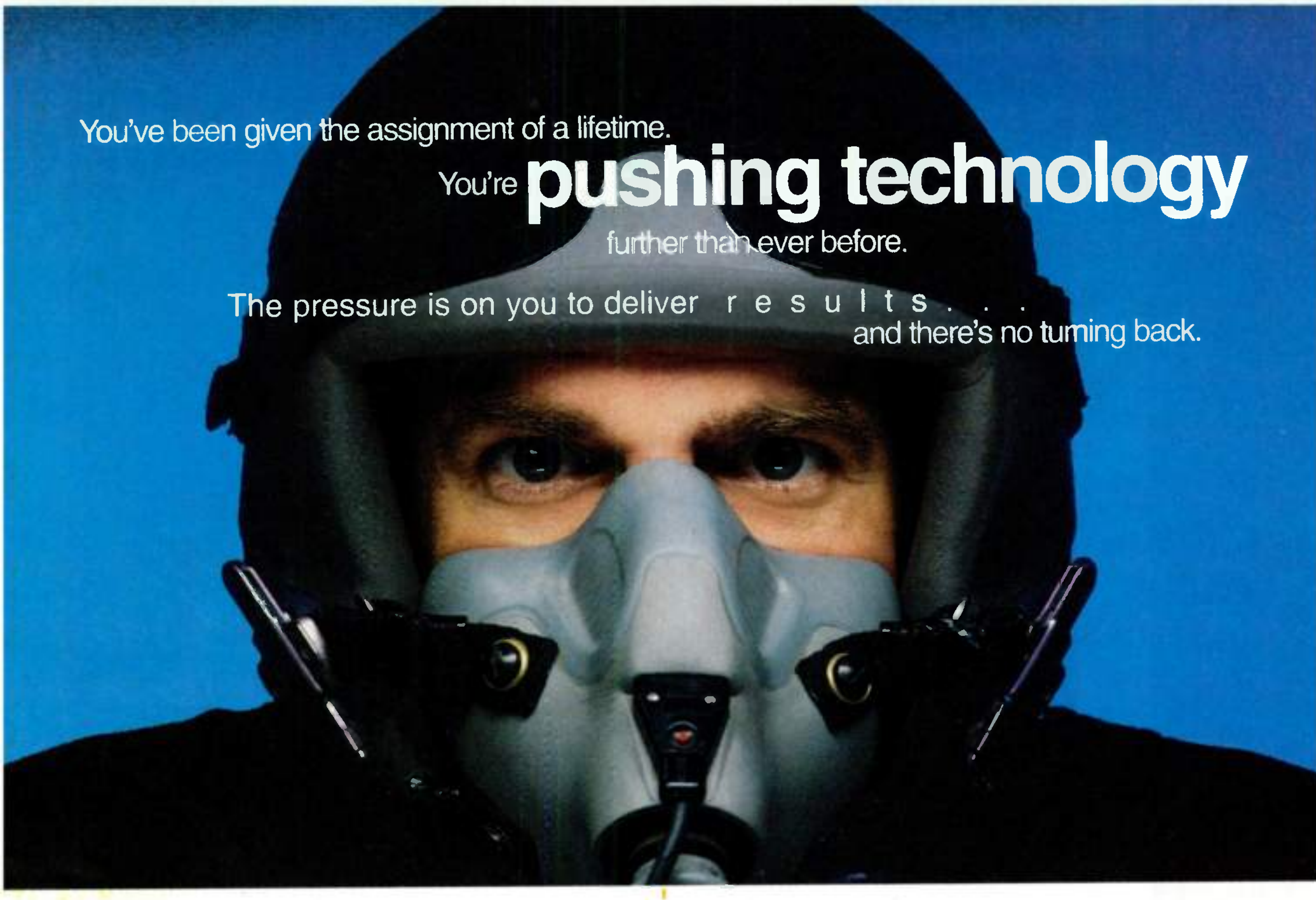
3. The reduction in critical gate dimensions in Lucent Technology's CMOS roadmap shows how gate density dramatically increases while the power per gate drops by an order of magnitude as the feature size decreases from 0.25 to 0.16 µm.

Logic Also Drops The Bar

Outside the DSP arena, TI designers also have released a high-performance, low-voltage logic family that keeps the propagation delays to less than 2 ns. Designed for operation at 2.5 V, the advanced very low-voltage CMOS (AVC) family supports mixed-voltage systems. It's also compatible with both 3.3- and 1.8-V devices. To handle the wide range of I/O levels, the chips include TI's dynamic output control (DOC) circuitry, which automatically varies the output impedance of the circuit during signal transitions to reduce noise. The DOC circuits provide enough current to achieve high signaling speeds, but quickly switch the impedance level to reduce the undershoot and overshoot noise often found in high-speed systems. This feature eliminates the need for damping resistors, which reduce noise but increase the propagation delay by slowing signals as they pass through the damping elements.

The AVC logic circuits also have a power-off feature that disables outputs from the device to support live or hot-insertion of boards into system backplanes. Such a feature is critical for applications such as networking, telecommunications systems, and other high-availability applications that can't be shutdown for repair. Also incorporated is a bus-hold capability, which lets the logic chips hold the last state of the bus line until the line switches again. TI expects to sample four AVC devices before the end of 1998: a 16-bit bus transceiver, a 16-bit buffer/driver, a 16-bit D-type transparent latch, and a 16-bit D-type flip-flop. But, a complete family of devices is planned, ranging from gates and octals to Widebus and Widebus+ devices. Military versions of selected AVC functions are also in the works.

Going toe to toe with the AVC group, Fairchild Semiconductor's VCX family has been optimized for operation at 2.5 V. At that supply level, the chips have propagation delays of about 3 to 3.5 ns—just a little slower than the AVC devices. Like the AVC chips, the VCX circuits can operate with 3.3- or 1.8-V supplies and incorpo-



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ADSL Technologies: Moving Toward The "Lite"—And Beyond

Products Supporting Second-Generation, Digital Subscriber Line Standards Will Help Deliver Low-Cost, Megabit Internet And Multimedia Services To Homes And Small Businesses.

Lee Goldberg

SPECIAL REPORT

1998 marks the year that digital subscriber line (DSL) technologies displace ATM, 56k, and QoS as the most over-hyped three-letter acronym within the communications industry. The goal of DSL's proponents is to transform the aging, twisted-pair voice-band infrastructures into cost-effective, Megabit-class data pipelines for residences and small businesses. Because asymmetric DSL's (ADSL's) initial roll-out has been slow, many within the industry are counting on the emerging "G.lite" DSL standard to jolt the telecom industry out of its torpid waddle and into a gallop toward a broadband future. Scheduled for initial ratification around the time this article goes to press, G.lite claims to trade off some of the full-rate standard's performance for lower cost, ease of deployment, and solutions to some of the technical challenges posed by T.413, its full-rate cousin.

Art Courtesy: Texas Instruments

Although it was finalized well over a year ago, there has been some reluctance to aggressively develop and deploy systems using the original, full-rate, T.413 ADSL standard. Approved by the International Telecommunications Union (ITU) and ANSI's T1 committee, T.413 boasts data rates up to 6 Mbits/s downstream, and 640 kbits/s back to the central office over standard twisted-pair copper. Despite its potential, ADSL has faced a complex web of technical, economic, cultural, and political issues that have delayed its universal acceptance.

As of late, the local exchange carriers (LECs) are finally beginning to realize that they cannot count on their semi-monopoly status to protect them much longer. Part of this pressure comes from the cable-modem market, as well as competitive access carriers and competitive LECs (CLECs). These groups are itching to sell their own brands of high-speed Internet access, and grab a chunk of the LECs' last-mile business. As one highly placed manager at a leading IC house noted, "[the LECs] must learn from the semiconductor industry about the importance of cannibalizing their young [their existing markets] before somebody else does."

If this shock therapy works, incumbent and CLECs will find an interesting arsenal of weapons under development as they prepare to battle with cable and wireless broadband delivery technologies.

Higher levels of integration and fine-tuning from data collected in field trials are making full-rate ADSL much more practical. Meanwhile, lower-cost, lower-power alternatives such as G.Lite, HDSL2, and WildWire are rapidly arriving to provide quick solutions to some of T.413's most pressing technical problems.

Before we get any deeper into these issues, it might be a good idea to get a quick refresher course on the basics of DSL, a broad term for technologies which re-use existing copper-pair voice lines for high-speed data.

ADSL 101

ADSL uses the spectrum above the 4-kHz voice band to create a data pair of channels on a single pair of telephone lines. As it stands today, the ITU-approved version of ADSL employs discrete multitone (DMT) technology that creates a series of 4.3125-kHz-wide data subchannels to carry the data *(Fig. 1a)*. Much like a conventional voice-band modem, each subchannel, or tone, is phase/amplitude modulated to carry multiple bits per symbol.

In the T.413's basic-frequency use plan, upstream and downstream traffic are split into two separate bands, both placed well above the 0-to-3.5-kHz spectrum used for voice-band POTS service. The upstream band (from subscriber to telco) occupies the spectrum between 25.875 and 138.8 kHz, while a second band between 138 kHz and 1.1 MHz handles the downstream (from telco to subscriber) channel *(Fig. 2)*.

Data fed into a DSL modem for transmission is distributed across these subchannels, and reassembled into a single data stream on the receiving side. Each of these channels encodes blocks of symbols using quadrature/amplitude modulation. Reed-Solomon forward error correction (FEC) and an optional trellis-coding scheme are used to increase the channel's capacity, bit-error rate, and noise margin.

Twisted-pair copper is not the world's greatest high-frequency transmission medium, with a sharp and unpredictable attenuation curve for frequencies above a few tens of kHz. This means that a receiver will see a 50-dB or more difference in signal strength between subchannels at the lower end of the ADSL spectrum and those operating at around 1 MHz. To compensate, ADSL uses heavy equalization and a variable line-coding scheme. The line-coding scheme varies the amount of information carried on a particular subchannel, based on the attenuation characteristics it encounters.

Tones at the lower end of the spectrum might support deep phase/amplitude modulation that permits as many as 15 bits to be encoded in a single symbol *(Fig. 1b)*. As the signal strength rolls off and the SNR decreases further up the spectrum, a subchannel might encode as little as 2 bits, or even be shut down altogether.

For these reasons, an optional plan (known as Category 2 in the T.413 specification) has been developed to let both upstream and downstream channels share the "sweet spot" of the ADSL band (cb). It uses digital echo cancellation to enable both upstream and downstream signals to coexist in the lower part of the available spectrum where attenuation is much less of a problem. Although Category 2 operation requires much more signal pro-

For More Information On ADSL

The ADSL Forum

This industry consortium factored heavily in the development of the T.413 specification. They have a wealth of information on ADSL, along with contacts for most industry players. Membership is essential if you want to work with ADSL technologies. Contact them at: The ADSL Forum, 39355 California St., Suite 307, Fremont, CA 94538; (510) 608-5905; fax (510) 608-5917; www.adslforum.com; e-mail: adslforum@adsl.com.

The Universal ADSL Working Group (UAWG)

A spin-off of the ADSL Forum, it helps develop the foundations for the G.Lite standard. There is no real office for this organization, but you can catch up on the latest developments, or find out how to become a member at their web site: www.uawg.com.

International Telecommunications Union (ITU)

This is the grandfather of all telecommunications groups. The U.N.-chartered organization oversees global communication standards, and is a repository for tons of useful information—provided you can decipher their somewhat arcane documentation system. Contact them at: ITU, Place des Nations, CH-1211, Geneva 20, Switzerland; main switchboard +41 22 730 5111; fax +41 22 733 7256; www.itu.org; e-mail: itumail@itu.int.

Paradyne Corp.

This little spin-off from Lucent is heavily involved with applying its proprietary technologies to the DSL world. Their booklet, *The DSL Source Book*, contains a mixture of detailed technical information and revisionist history on the origins of ADSL. Good reading and very informative, just watch out for the propaganda. Contact (800)-PARADYNE, or (813)-530-8623.

Texas Instruments Inc.

A leader in DSP, TI has put together an informative little guide on some of the deep technical issues of ADSL. Although conceived as a series of viewgraphs to accompany a lecture, the slides contain lots of information not commonly available. One example is a concise summary of the infinite series of transforms involved in creating a DMT ADSL waveform. Ask for your copy of *Applications of Programmable DSPs For DMT and ADSL* by writing to: Texas Instruments Inc., Semiconductor Group SC-98082, Literature Response Center, P.O. Box 172228, Denver, CO 80217; (800) 477-8924 ext. 4500.

Virata Corp.

Virata is a relatively unknown player in ADSL, but is a technical heavyweight. They have made many important contributions to meshing the technology with the ATM protocols that it uses to transport data. These folks have put together a very useful booklet titled *Personal Broadband Services: DSL and ATM*. It contains lucid descriptions of the intricacies of ADSL network architectures and the protocols they use. Contact them at: Virata Corp., 2933 Bunker Hill La., Suite 201, Santa Clara, CA 95054; (408) 566-1000; www.virata.com.

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cessing, it offers the possibility of even higher line capacity and better overall performance.

DMT's Little Secret

Echo cancellation will also help modems cope with one of the "dirty little secrets" that DMT advocates don't like to talk about. It turns out that the DMT upstream algorithm produces signal artifacts, or sidelobes, which can create near-end cross-talk (NEXT). This interferes with the lower downstream bands. It can be addressed by either turning off the first two or three tones, or by using echo cancellation.

In the interest of interoperability, units capable of Category 2 echo can-

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attn: Paul Osiecki
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adsl_ran@www.alcatel.com,
Comments: The MTK-2031 DynaMite three-chip set has AFE, modem, and controller.
CIRCLE 453

Advanced Micro Devices Inc.
One AMD Place
P.O. Box 3453
Sunnyvale, CA 94088-3453
(408) 732-2400
www.amd.com
Comments: ADSL and G.Lite modem chip sets license Alcatel's architecture
CIRCLE 454

Analog Devices Inc.
Ray Stata Tech Center
804 Woburn St.
Wilmington, MA 01887
(800) ANALOG-D
(718) 937-1428
fax (781) 821-4273
www.analog.com
Comments: ADI places emphasis on long-reach capabilities using fast DSPs and extremely linear AFEs with lots of power margin. It also has high-performance AFEs.
CIRCLE 455

Aware Inc.
40 Middlesex Tpk.
Bedford, MA 01730-1432
(781) 276-4000
fax (781) 276-4001
www.aware.com.
Comments: Aware is a heavy player in the development of xDSL technologies. Licenses software algorithms, and other DSL-related IP.
Circle 456

Broadcom Corp.
16251 Laguna Canyon Rd.
Irvine, CA 92618
(949) 450-8700
fax (949) 450-8710
www.broadcom.com
Comments: Currently supports VDSL, QAM-based ADSL, and QAM-based ADSL Lite.
CIRCLE 457

Burr-Brown Corp.
6730 Tuscon Rd.
Tuscon, AZ 85706
(800) 548-6132, (520) 746-1111
fax (520) 889-1510
www.burr-brown.com
Comments: A specialist in analog front ends, Burr-Brown has developed high-performance, power-efficient solutions for both T.413 and G.Lite modems.
CIRCLE 458

GlobeSpan Semiconductor
100 Schultz Dr.
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(732) 345-7500
www.globespan.net
Comments: Claims to have a programmable, multi-standard, DMT/CAP chip set.
CIRCLE 459

Integrated Device Technology Inc.
2975 Stender Way
Santa Clara, CA 95054
(800) 345-7015
(408) 492-8674
www.idt.com
Comments: Producer of ATM SARs and SwitchStar switching memory/controller for ADSL transport.
CIRCLE 460

Integrated Telecom Express Inc.
2710 Walsh Ave.
Santa Clara, CA 95051
(408) 980-8689 ext. 252
e-mail: yi-ju.chen@itexinc.com
www.itexinc.com
Comments: Has a software-based host processing solution for G. Lite, plus a T.413-compliant chip set.
CIRCLE 461

Level One Communications Inc.
9750 Gothe Rd.
Sacramento, CA 95827
(916) 855-5000
fax (916) 854-1101
www.levelone.com.
Comments: Current products support MDSL, HSDL, and HDSL II. Expect new developments to be coming soon.
CIRCLE 462

Lucent Microelectronics Group
Customer Response Center
Room 30 L-15P-BA
555 Union Blvd.
Allentown, PA 18103
(800) 372-2447
fax (610) 712-4106
Comments: Dual-DSP WildWire chip set has both analog and ADSL modem capability.
CIRCLE 463

Motorola Semiconductor Products Sector
3501 Ed Bluestein Blvd.
Austin, TX 78721
attn: Rick Hall
(512) 934-8295
fax (512) 934-7991
e-mail:
rwbc30@email.sps.mot.com
wwwmot.com/adsl.
Comments: CopperGold ADSL T.413 chip set combines DSP core, ATM processing logic, and mixed-signal technologies.
CIRCLE 464

PairGain Technologies Inc.
14402 Franklin Ave.
Tustin, CA 92680
(714) 832-9922
fax (714) 832-9924
www.pairgain.com.
Comments: Codeveloped Falcon ADSL modem with Rockwell. G.Lite and other solutions are on the way.
CIRCLE 465

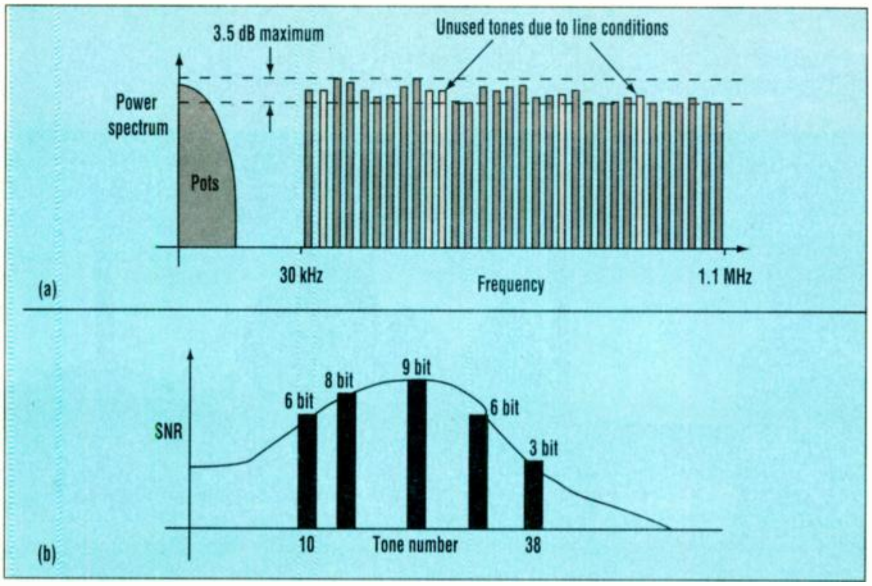
Rockwell Semiconductor Systems Inc.
4311 Jamboree Rd.
Newport Beach, CA 92658
(949) 221-6996
e-mail:
rockwell@salessupport.com
Comments: Zipwire SDL chip set uses 2B1Q to deliver symmetric data at rates from 144 to 2.3 Mbits/s. Future versions will support G. Lite ADSL. Developed ADSL modem with PairGain.
CIRCLE 466

Texas Instruments Inc.
Semiconductor Groups SC-98058 and SC-98030B
Literature Response Center
P.O. Box 172228
Denver, CO 80217
(800) 477-8924 ext. 4500
Comments: Heavy DSP technology, plus ASIC capability enables aggressive solutions. Watch for upcoming developments.
CIRCLE 467

STMicroelectronics Inc.
10 Maguire Rd.
Lexington, MA 02421
attn: Roy Harvey
(781) 402-8543
fax (781) 861-2664
www.st.com
Comments: Has a DMT-based ADSL chip set. Working on VDSL modem with Telia Research.
CIRCLE 468

Transwitch Corp.
8 Progress Dr.
Shelton, CT 06484
(203) 929-8810
fax (203) 926-9453
www.transwitch.com
Comments: Makes cost-effective ATM interfaces and switch chip sets for ADSL transport infrastructure.
CIRCLE 469

Virata Corp. (formerly ATM Ltd.)
2933 Bunker Hill La.
Suite 201
Santa Clara, CA 95054
(408) 566-1000
fax (408) 980-8250
www.virata.com
Comments: Chip sets for ADSL modems have extensive protocol processing ability, plus software and firmware support including RTOS for ISO and ATM stacks, and IP protocols
CIRCLE 470



1. A discrete multitone modem uses 256 subchannels, spaced 4.3125-kHz apart, to encode data in a QAM format (a). Subchannels least affected by line impairments are modulated the most deeply to encode a larger numbers of bits (b).

cellation will also have to support basic FDM operation. This is achieved thanks to a uniform startup sequence and control channel defined by the T.413 specification. As a connection is first made, the modems negotiate their highest levels of operation. During startup, they also probe the line to determine its spectral response by sending tones from both ends, and measuring their attenuation. From this data, they set up their initial equalization parameters, and decide how many bits are assigned to each subchannel.

Because a line's attenuation characteristics can vary significantly over the duration of a call, an ADSL modem must constantly probe the health of each subchannel. This is done using bit-error rate and signal strength as indicators of carrier integrity. If a particular tone grows stronger or weaker, the modem uses an in-band signaling protocol to ask the unit at the other end for upward or downward adjustments of the encoding levels.

Trellis coding is another option for modem manufacturers. By adding another bit to the quadrature-amplitude-modulation (QAM) constellation to create some redundant symbols, and only allow certain phase/amplitude transitions, trellis coding can add another few dB of noise immunity.

Of course, the number of bits that ADSL can squish down a pair of wires decreases as line length increases. Powerful line-equalization and noise-cancellation algorithms are used to compensate for poor line quality, but they have their limitations. Under ideal conditions, a T.413-compliant system can theoretically deliver 8 Mbits/s to a home, over 12,000 ft of wire. At 18,000 ft, capacity rolls off sharply to 1.5 Mbits/s, as attenuation, cross-talk, and other factors force the modem to encode fewer bits per subchannel.

Despite the massive equalization and error correction employed, there are some subscriber lines that are long enough or have impairments severe enough to confound even the abilities of the clever DMT modem. Multiple changes in wire gauge (24 to 26 AWG and back again) can be found in older lines which have been repeatedly serviced. Multiple wire gauges are not usually showstoppers, but the impedance variations can cause unwanted reflections and attenuation that force the modem to lower the number of bits carried in some tones, or even cut them out altogether.

Bridge taps hanging off a wire are also common in some service areas, and can create even more serious reflections and impedance mismatches that degrade reach and channel capacity. The real DSL-killer is the loading coil; a passive device used to boost signal levels in lines that go beyond 18,000 ft. No amount of processing will bring back these blocked signals.

Finally, there's concern that ADSL lines sharing the same cable bundle with T1, ISDN, HDSL, or possibly other ADSL wire pairs will experience some level of crosstalk. Spectral compatibility with T1 services isn't a big issue in suburban and rural America, but many metropolitan subscribers may be sharing a wire bundle with a nearby business that has a T1 or ISDN line.

Also, Europe and Asia have lots of residential ISDN lines, which will require some accommodation to coexist with ADSL. For example, ISDN lines employ 2B1Q encoding in the U.S., and 4B/3T encoding in Germany to deliver 128 kbits/s to homes and offices. Both schemes have spectral components that extend up to 100 kHz, well into the normal ADSL band. Recent analysis has shown that ADSL must relocate its operation above 80 kHz to become compatible with the 2B1Q coding scheme used in many U.S. T1 lines. Solutions under consideration include shifting up the entire ADSL spectrum, or simply turning off the bottom five or so tones.

Despite these problems, current estimates indicate that a high percentage of U.S., Asian, and European homes can be reached by T.413 or one of its variants. There are, however, still a number of problems with which the industry still wrestles.

Technical Obstacles

The two primary technical issues hindering full-rate ADSL acceptance have been complexity and power requirements. The complex algorithms used to shove broadband data across 2+ miles of twisted-pair copper require loads of DSP computation (500 to 1000 MIPs or more, depending on the complexity of the filtering and equalization performed). Most solutions employ some sort of hardware assistance to lower the demands on the DSP, but you can still wind up with expensive, power-hungry silicon. While submicron processes have cut the size and power of ADSL chips substantially, it will be early next year before most manufacturers can offer a chip set that's highly integrated enough to support a full-rate ADSL modem with a sub-$200 price tag.

DSL also raises some serious issues for analog designers concerned with the interface between the DSP and the copper line. In fact, one wag suggested that the ADSL standard had been pro-

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Noise-free resolution	18-bits	16-bits
Bipolar/unipolar input ranges	25mV, 55mV, 100mV, 1V, 2.5V, 5V	2.5V
Instrumentation amplifier	Chopper-stabilized	—
Drive circuitry	On-chip charge pump	—
Output latch	4-bit	6-bit
Interface	Three-wire serial; SPI™, Microwire™ compatible	Three-wire serial; SPI™, Microwire™ compatible
Filter settling time	One conversion cycle	One conversion cycle
Calibration	System, self with read/write registers	System, self with read/write registers
Power supply	Single +5V analog, +3V or +5V digital	Single +5V or dual ±2.5V analog, +3V or +5V digital
Power consumption	4.5mW	2.5mW

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duced by a group of digital engineers who developed marvelous DSP algorithms with little attention to the havoc they would cause for analog designers to implement.

One of the big challenges for designers of analog front ends (AFEs) is the fact that the DMT modulation techniques used in full-rate ADSL requires drivers which can yield large voltage swings with high linearity. Although the average power level of a DMT signal is reasonable (about 20 dBm), the signal's crest factor can run as high as 5.3. This necessitates a transmitter with a wide dynamic range and correspondingly higher power consumption.

Current demands on a line driver can be substantial. T.413's linearity requirements also add to the power issue. Mike Steffes, strategic marketing manager at Burr Brown, notes that in order to transmit a full series of DMT QAM constellations cleanly, a line driver must also meet very-high linearity requirements (70 dB SNR or better). This forces the transceiver's line drivers to be run at high bias levels, increasing the power requirements even further.

At 8- to 12-W per channel for a typical, end-to-end, full-rate ADSL system, the heat dissipation limits in the cramped environment of a telco equipment shelf could severely limit the number of channels a manufacturer could pack onto a single line card. Providing power to line cards is expensive in a central-office environment (around $30/W), an added incentive to keep the W/line ratio low. All these factors are driving companies like Analog Devices, Lucent Semiconductor, and Texas In-

VDSL: The Future Is Here

VDSL, or very-high bit-rate digital subscriber line, has extended the bandwidth of the twisted-pair copper loop to about four times that of asymmetrical digital subscriber line (ADSL). Therefore, it can deliver high-quality, switched digital video service on a mass-market basis. Because it enables delivery of services over 3000 to 4000 ft of telephone line, providers pull fiber deeper into the local loop. The fiber is terminated in remote cabinets or optical network units at the interface to the twisted pair. At the customer's premises, a VDSL modem converts the signal back into a format such as MPEG-2, IP, or DS0.

VDSL is specified for symmetrical and asymmetrical operation. Asymmetrical VDSL provides 19.44 to 25.92 Mbits/s downstream. Using ATM as a transport protocol, it can support three or four digital MPEG-2 video streams, plus a primary and basic-rate voice/data connection. Upstream 3.24 Mbits/s are also available for high-speed uploading and web hosting. Symmetrical operation has been specified up to 52 Mbits/s for the shortest reaches.

There are four major issues that must be dealt with when transmitting high-speed data over twisted-copper wire pairs: noise, crosstalk, distortion, and narrowband interference. These channel impairments place limits on how far and fast links can be established. New, highly integrated silicon ICs use a number of techniques to combat these impairments. Reed-Solomon forward-error-correction algorithms are employed to combat errors induced by wideband noise sources.

Convolutional interleaving, typically caused by the operation of nearby electrical equipment, is also used to battle the effects of impulse noise. Crosstalk, caused by other transmitters in the cable, exhibits itself as colored or shaped noise, which can degrade the received SNR. High-speed, feed-forward equalizers are used to spread out , or "whiten," this noise. Receivers prefer white noise because it evens out the noise power over the signal bandwidth. Other techniques, such as trellis decoding, can then be used to take advantage of potential coding gains.

Broadband signals are distorted as they pass along the line, causing inter-symbol-interference (ISI). Receiving signals with large ISI is difficult because the receiver cannot tell the difference between the current symbol and the previous one. To compound matters, feed-forward equalizers increase ISI as they whiten noise. Decision-feedback equalizers are used to clean up the ISI generated by the channel and the feed-forward equalizer. The equalizer also helps cancel the effects of narrowband interference, caused by AM radio stations and amateur radio operators, for example.

There are two main modulation schemes used by VDSL modems: single-carrier, carrierless amplitude phase/quadrature amplitude modulation (CAP/QAM) and discrete multitone (DMT). Both techniques have nearly identical theoretical capacities. The differences lie in the implementation details. Proposed DMT systems modulate up to 2000 subcarriers in the transmitter. The cost and power penalty of these solutions up to now, has been prohibitive, and restricts their use to early prototype work and feasibility studies. QAM, on the other hand, mixes a Nyquist-filtered symbol with a digitally synthesized, single carrier. Because VDSL data rates are much higher than ADSL's, it is critical that the modulation scheme chosen should scale easily to the higher rates. Programmable digital frequency synthesis and variable-rate modulator techniques are now being employed to provide fully scalable ADSL to VDSL data rates. Practical semiconductor solutions are based on single-carrier QAM technology using dedicated hardware processing elements to reduce cost and power.

Finally, VSDL spectral compatibility with other services using the same distribution cable is important. VDSL systems must be able to provide a flexible allocation that can accommodate POTS, ISDN, primary-rate, and ADSL variants. Like ADSL, VDSL operates above POTS, and needs some filtering to separate analog POTS from digital VDSL. Since VDSL operates at much lower transmit power than ADSL, and its frequency band is much higher, separating POTS and VDSL traffic with splitterless filtering is relatively straightforward.

VDSL has made its way out of the lab and onto our streets. The technology works, and the chips and boxes are coming. Now it's up to the marketeers.

Contributed by Aidan O'Rourke, director of marketing, Broadcom Corp.

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EPF10K50VRC240-1	AMI5G109S	$8.50
Xilinx Device		
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quency constellation. Yi-Jen, product manager at Integrated Telecom Express, Santa Clara, Calif., estimates that the overall processing requirements for a baseline G.Lite system are only 20% of its full-rate cousin. As we shall see, however, some of the proposed enhancements to splitterless DSL will end up reabsorbing many of the processor cycles that were originally "saved" by reducing the modem's data rates.

Of course, engineers can't leave a simple solution alone, and seem to live for the chance to "enhance" a design like Universal ADSL. UADSL has had a series of performance-oriented options added to it even before the ink dried on the original specification. The original proposal for UADSL employs FDM, with separate frequency bands for upstream and downstream traffic. While not finalized, there is a strong movement to allow G.Lite modems to use Category-2-like echo cancellation to allow both upstream and downstream channels to share the relatively good transmission characteristics of the lower part of the spectrum. Trellis coding is also under serious consideration.

Rick Hall, strategic marketing manager for Motorola's xDSL product line estimates that using echo cancellation can add 15% to 20% to the channel capacity of an average ADSL connection. This might be a good option for designers, because the much lower processing load required for basic G.Lite ADSL lets it support the demands of an echo-cancellation algorithm with a medium-performance DSP. Some industry analysts speculate that when echo cancellation is added, the additional cost of the extra MIPs it requires is equal to, or less than, the cost of the passive com-

HDSL2 Set For Deployment

For years, the high-speed, digital-subscriber-line (HDSL) standard has been deployed by telcos as a broadband connection to the central office, and as a zippier connection to fiber trunk lines. As the Internet continues to fuel explosions in data traffic, HDSL2 has emerged, based on the same specifications of the popular and proven HDSL. HDSL2 is moving steadily toward implementation, as a means for network providers to optimize the use of the existing cable plant by allowing full T1 or E1 data rates on a single twisted-copper pair. The technology caters to unconditioned copper lines, and it costs less. Only a single transceiver is required at either end of the telephone line.

HDSL2's objectives are straightforward: to provide the same robust performance of HDSL at full-carrier service-area lengths of 12,000 ft, over a single set of twisted-pair wires. This doubles the capacity of a carrier's installed wiring plant. HDSL2 also addresses another critical market factor: spectral compatibility with other services. It's important for a new technology to work seamlessly with the existing services used in the same 50-pair cable.

Requirements include a 1.552-Mbit/s symmetric data rate, with a 5-dB noise margin in worst-case crosstalk conditions. Latency requirements are less than 500 µs. HDSL2 achieves the speeds and latencies of HDSL, and maintains spectral compatibility with existing services, such as ISDN, ADSL, T1, E1, and of course, HDSL. HDSL2 has also been designed to be robust in a mixed-crosstalk environment, and will deliver 5 dB of noise margin.

By meeting these criteria, HDSL2 becomes an ideal alternative to the asymmetrical digital subscriber line (ADSL). It supplies the symmetrical, highly reliable, bandwidth required by business applications. ADSL, in contrast, is fine for Internet home use, but not nearly as suitable for business applications such as web hosting, video conferencing, and servicing multiple voice lines.

One element of HDSL2's design is a shaped pulse-amplitude modulation, which controls the spectral energy emitted to other services in a local-loop cable bundle. To determine the appropriate shaping, the crosstalk spectrum from multiple services is analyzed. Two key characteristics emerge. First, downstream and upstream channels have significantly different crosstalk noise environments. In the downstream channel, there is a spectral null in the power-spectral density (PSD) region between 200 and 300 kHz. The fact that the downstream signal will experience relatively low crosstalk noise in this region allows the system to introduce more "self-crosstalk," so that the designer can boost the power spectral density of the upstream channel in this region.

To minimize overall HDSL2 crosstalk noise into other services, the downstream spectrum is notched in this same region. The result: an upstream and downstream PSD template carefully defined for the noise environment in North America. This PSD template has been carefully shaped to operate in the kind of mixed-crosstalk environment that exists in 50-pair cable bundles and with no interference with other services.

A forward-error-correction (FEC) scheme is also used to ensure that the system can provide a sufficient signal-to-noise ratio margin for reliable service—over 5 dB for mixed services with a bit-error-rate of over 10^{-7}. This symmetric, low latency allows combined services like interactive video and data, and enables digital delivery of multiple voice connections. In contrast, while ADSL can provide high data rates over 1.5 Mbits/s, it's one-way only—downstream, from the central office to subscriber. Upstream rates cannot top a few hundred kbits/s.

In addition to T1 and E1 services, HDSL2 also is an ideal high-speed connection to a small office or home office where symmetric service is required. For the small office, HDSL2's low latency and symmetric nature allows the combination of digital voice, and data on the subscriber line. These benefits are also required for video conferencing, which is in the plans of many CLECs and ISPs.

With demand from telecom equipment suppliers high and the initial HDSL2 chipsets now in early testing and applications, HDSL2 technology appears to be well on its way to rapid deployment.

Contributed by James Quilici, technical marketing manager, DSL products, at Level One Technologies.

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ponents required to build the bandpass filters used in FDM modems.

Caveats For Lite Stuff

As any engineer knows, anything with this many advantages must have something skulking in the shadows, and Universal ADSL is no exception. For example, Kevin Cone, marketing manager at Lucent Technologies Semiconductors, estimates that only about 50% to 60% of American homes will be able to deploy G.Lite-type splitterless ADSL without any changes to their wiring or telephone equipment.

He explains that Lucent's field studies indicate that many of the remaining problems are due to one or two pieces of "offending telephones." These are typically older (antiques) or very cheaply made handsets that don't meet current network standards. Among other things, the high-inductance ringers of older electromechanical handsets create incredible voltage spikes, while the Zener diodes in the protection circuits of some newer telephones can react unpredictably with ADSL's high-frequency components *(Fig. 3)*.

These rogue telephones can either be replaced or put back into service with an in-line filter installed to keep ADSL's frequency components out. Lucent's Cone cautions that you can probably only use about three in-line filters on a given loop before they drop its impedance far enough to affect signal level and frequency response. A smaller minority of homes will require substantial rewiring to eliminate serious reflections. An even smaller percentage may have network line conditions which won't support ADSL at all.

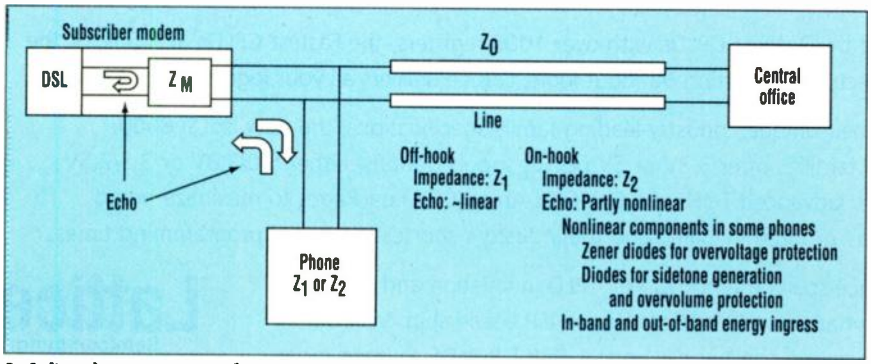
Off-hook operation is a very serious concern, which is still under careful study by most ADSL chip and equipment makers. When a regular telephone call or modem transmission is made on a line sharing an ADSL connection, several phenomena occur. An incoming call is accompanied by a series of sharp ring pulses with spikes of around 40 V or more, which can punch holes in one or more subchannels.

When it's picked up, the off-hook telephone drastically changes the line impedance and frequency response that the two modems had so carefully calculated, causing a sharp increase in dropped or scrambled bits. Finally, harmonics from the conversation or fax tones can seriously degrade the SNR of the ADSL band. These phenomena were not problems for T.413 systems, because the mandatory splitter isolates them from most of the issues raised by the telephones.

A Warm Start For DLSL Lite

To cope with this sudden interruption in service, a UADSL modem must sense the cause, adjust itself to the new line conditions, and begin a recovery sequence. Victor Lee, vice president of marketing at Integrated Telecom Express, explains that because ADSL modems can take a minute or more to establish a new connection, it's essential that they perform an abbreviated "fast-retrain" sequence. This sequence can restore interrupted service in only a second or two.

Lee says that during a "warm start," the modem reuses parameters it obtained during startup, such as the distance to the central office, the initial transmitter and receiver gains, and the basic attenuation characteristics for the connection. It employs these initial parameters as starting values for an abbreviated characterization which involve probing the line with several simultaneous tones. This procedure quickly measures changes in frequency response and SNR at various frequencies. If done correctly, Lee claims that the modem can be up and operating at reduced data rate in as little as 1.5 s. When the voice-band connection ends, both modems perform a second warm start, and resume a higher-speed connection over a less-impaired line.



3. Splitterless operations for ADSL modems pose several challenges. The most difficult is dealing with the sudden changes in line characteristics that occur when a telephone, fax machine, or voice-band modem goes "off the hook."

DSL Alternatives

Of course, DMT ADSL is not the only way, or even the best way in all cases, to get lots of data down a copper loop. For example, advocates of alternate technologies point to strong evidence that schemes such as QAM or carrierless amplitude/phase (CAP) modulation are somewhat more power-efficient and require far fewer DSP processor cycles to implement.

The spectral power-density distribution of QAM- and CAP-based systems is also much kinder to AFEs and receivers, making them less difficult to design and build. Despite this, we will be living with DMT-based ADSL in most early systems, thanks to its status as an ITU standard. Nevertheless, the politics of patents and the technical merits of these other technologies should be enough to give them a reasonable market share. For the short term, we can expect to see CAP/QAM-based DSL solutions appearing in campus settings and other places where standards are not as large an issue.

In the long term, QAM-based versions of very-high-speed DSL (VDSL) will most likely be used to deliver tens of megabits worth of multimedia services directly to homes. Although VDSL has a shorter reach than ADSL (3000 ft or less for really fast connections), it requires much less processing power per unit of bandwidth and versatility than ADSL. In fact, large-scale commercial deployment, involving tens of thousands of homes should be underway in a major southwestern city by the time you read this *(see "VDSL: The Future Is Here," p. 88.)*

Several variants of high-speed DSL (HDSL) are also making inroads into the digital-access market. These technologies challenge the faster ADSL by delivering symmetrical T1-speed services (around 1.5 Mbits/s) over longer distances of ungroomed copper pairs. Another important feature is that HDSL variants have carefully tailored spectral profiles that were designed specifically to peacefully coexist with existing ISDN, voice, and T1 services.

Symmetric, reliable, T1-style data connections at a significantly reduced cost are sure to find homes in already T1-capable businesses, as well as new ventures needing symmetric bandwidth to support remote networking, large bidirectional transactions, or web site hosting. Companies like GlobeSpan, Lucent, Rockwell, and PairGain, have all developed technologies that can deliver HDSL-type service. Among the more interesting is the HDSL2 standard, developed by Level One Communications, PairGain Technologies, ADC, and Adtran *(see "HDSL2 Set For Deployment," p. 92.)*

Chip-Set Architectures

The current offerings of DSL modems show a wide spectrum of implementation philosophies. Some companies, like GlobeSpan and Alcatel choose to rely heavily on dedicated logic and ASICs to optimize performance and keep the per-unit costs low.

Others, like TI, prefer to capitalize on their high-performance DSP capabilities to deliver a software-intensive solution. Advocates of an all-DSP modem say that full programmability and a surplus of processing power will help designers deliver products that can track evolving standards more easily, and accept feature enhancements with a simple software upgrade.

Most chip vendors are taking a middle-of-the-road approach, with a moderately fast DSP (2-400 MIPS) coupled to hardware logic, which is used to perform some of the more repetitive and predictable tasks. Firms like Analog Devices and Virata, represent this middle path. Chip makers are reluctant to talk about exactly what operations they perform in hardware, but one imagines they would be things such as FFT and IFFT calculations and Reed-Solomon FEC functions. Even the staunchest DSP advocates admit that once the field matures, we will see most chip sets using hardware logic to enable the use of lower-power, easier-to-integrate medium-speed DSP cores in next year's crop of single-chip ADSL modem ASICs.

One very novel, all-software modem delivers UADSL service with a minimum of hardware by performing signal processing on the host PC. Developed by Integrated Telecom Express, the firm's software modem uses an analog line-interface circuit, a codec, and a buffer to couple the incoming signals to the host computer via its PCI bus. All signal processing and control tasks are performed in a standard Windows environment, using a 300-MHz Pentium II-class processor.

Trojan Modems

Part of the ADSL deployment strategy rests in making standardized modems that are inexpensive enough to offer through retail stores. By letting consumers buy their own equipment, the telcos hope to avoid having to go into the modem business. As a result, the big question being asked of the telcos is: how do you create a demand for the modems before the service arrives in their neighborhood?

The solution to this chicken-and-egg dilemma is the hybrid modem. Because a DSP capable of supporting G.Lite can easily handle all the functions of a V.90 audio modem, many IC houses are hoping to offer chip sets that can do both tasks. They reason that if such a modem could be sold for a few dollars more than a V.90-only model, many customers would buy it as "insurance," and wait for their LEC to make ADSL available. This "Trojan Modem" tactic could be the key that opens the market for widespread adoption of ADSL.

Even today, the second AFE, codec, and extra software required to add V.90 capability adds up to 20% to a unit's bill of materials, and the differential is expected to drop much lower as ADSL chip sets continue to integrate.

Several chip sets like Lucent's dual-DSP WildWire are already capable of supporting UADSL or V.90 operation, with more to follow by the end of the year. IC makers have already charted the next step: a modem chip set that can send or receive a voice-band fax while supporting an ADSL connection.

ADSL's Slow Roll Out

Given the promise of ADSL, it's surprising how little of the technology has been put in the field—even in trials. Amusingly, one of the biggest obstacles to a rapid ramp-up of ADSL has been the telcos themselves. It's been hard for them to seriously contemplate offering low-cost broadband services that could provide direct competition to their very lucrative monopoly on more expensive ISDN and T1 digital connections.

This uncomfortable situation has not provided much incentive for LECs to work quickly at resolving the technical barriers that stand in the way of delivering cost-effective ADSL service. Consequently, ADSL deployment has been limited to trials, serving tiny pockets of the population, while cable companies continue to deploy HFC data services as quickly as their plant upgrades permit.

Telcos also face some genuine problems in getting into the DSL business. For one thing, DSL represents a complete departure from their traditional technical and business models. DSL is designed to split off data traffic into a separate network once it reaches the central office, freeing up the expensive and bandwidth-limited telephony infrastructure. While this is something they desperately want, it means that telcos must also equip each central office with switches, concentrators, and other paraphenalia to feed traffic into the Internet or other backbone networks. A retrofit of this magnitude takes money, time, and a certain level of experience in building, provisioning, and managing a datacom network—something the LECs may or may not have.

The telcos have also been justifiably shy to jump on the DSL bandwagon because they know it's an immature technology. The limited field experience for ADSL shows that nobody has a full understanding of the kinds of interference and line impairments that LECs and their equipment will be expected to deal with. This almost guarantees that early ADSL adopters will be on a steep learning curve as they deal with bugs, flaws, and hidden technical problems that are not usually tolerated in a culture that delivers near-universal service, and prides itself on limiting service interruptions to seconds per year.

It's true that all these concerns will take time to resolve, but the only way to do this is begin aggressive deployment of commercial services. Now that the technology and products are here to enable cost-effective ADSL service, it's up to the LECs, CLECs, and other telephone system operators to deliver them.

Circle 520

Tiny Microcontroller Provides 4-Channel A/D Conversion For A PC Serial Port

YONGPING XIA
Teldata Inc., 8723A Bellanca Ave., Los Angeles, CA 90045.

Microchip's PIC12C671 is a low-cost 8-pin microcontroller that has everything needed to perform a four-channel 8-bit analog-to-digital conversion without external components. To create a plug-in four-channel analog-to-digital converter for a PC, the circuit in Figure 1 uses a PC's serial port to power and communicate with the PIC12C671.

Pin 4 of the PC's serial port supplies power to the microcontroller through a 5-V reference device. The PIC12C671's V_{DD} also serves as an A/D conversion reference voltage. The PC sends commands to the microcontroller through pin 7, and the device sends information back to the PC through pin 2. Figure 2 shows the details of the communication protocol.

Once the 12C671 powers up, it will count how many pulses are generated on the serial port's pin 7 within 16 ms.

```
; 4-channel A/D conversion for a PC Serial Port
; author:  Yongping Xia
;
LIST            P=12C671

        TMR0        equ     0X01
        PCL         equ     0x02
        STATUS      equ     0x03
        GPIO        equ     0X05
        INTCON      equ     0x0b
        ADRES       equ     0x1e
        ADCON0      equ     0x1f
        ADCON1      equ     0x9f
        OPT         equ     0X81
        port_dir    equ     0x85
        temp_1      equ     0x21
        temp_2      equ     0x22
        temp_3      equ     0x23
        send_data   equ     0x24
        channel     equ     0x25
        Z           equ     2
        C           equ     0

                    org     0x00
                    goto    main

                    org     0x04
                    call    get_channel
                    decfsz  channel, 1      ; select an A/D input
                    goto    next_1
                    movlw   0x41            ; channel 0
                    goto    set_channel
next_1
                    decfsz  channel, 1
                    goto    next_2
                    movlw   0x49            ; channel 1
                    goto    set_channel
next_2
                    decfsz  channel, 1
                    goto    next_3
                    movlw   0X51            ; channel 2
                    goto    set_channel
next_3
                    movlw   0x59            ; channel 3
set_channel
                    movwf   ADCON0
                    movlw   0X05
                    movwf   temp_1
                    call    delay
                    bsf     ADCON0, 2       ; start A/D conversion
loop_1
                    btfsc   ADCON0, 2
                    goto    loop_1
                    movf    ADRES, 0
                    movwf   send_data
                    call    send_out
                    bcf     INTCON, 0
                    retfie
get_channel
                    clrf    temp_2
                    clrf    temp_3
                    clrf    channel
get_ch_lp
                    btfss   GPIO, 3
                    goto    input_low
                    movlw   0X01
                    movwf   temp_3
get_ch_1
                    moviw   0x1a
                    movwf   temp_1
                    call    delay
                    decfsz  temp_2 ,1
                    goto    get_ch_lp
                    return
input_low
                    movf    temp_3, 0
                    btfss   STATUS, Z
                    incf    channel, 1
                    clrf    temp_3
                    goto    get_ch_1
send_out
                    movlw   0X08
                    movwf   temp_2
                    bsf     GPIO, 5         ; training bit
                    clrf    temp_1
                    call    delay
                    bcf     GPIO, 5
                    clrf    temp_1
                    call    delay
                    bsf     GPIO, 5         ; start bit
                    clrf    temp_1
                    call    delay
send_lp
                    rrf     send_data, 1 ;
                    btfss   STATUS, C
                    goto    send_low
                    bsf     GPIO, 5
send_1
                    clrf    temp_1
                    call    delay
                    decfsz  temp_2 , 1
                    goto    send_lp
                    bcf     GPIC, 5         ; stop bit
                    clrf    temp_1
                    call    delay
                    return
send_low
                    bcf     GPIO, 5
                    goto    send_1
                    delay
                    decfsz  temp_1, 1
                    goto    delay
                    return
delay
                    decf    temp_1, 1
                    goto    delay
                    return
main
                    clrf    GPIO
                    bsf     STATUS, 5       ; bank 1
                    movlw   0X88
                    movwf   OPT
                    movlw   0x1f
                    movwf   port_dir
                    movlw   0X00
                    movwf   ADCON1
                    bcf     STATUS, 5       ; bank 0
                    movlw   0X88
                    movwf   INTCON
loop                                        ; endless loop
                    goto    loop
                    end
```

LINEAR TECHNOLOGY

DESIGN NOTES

12-Bit 3Msps SAR ADC Solves Pipeline Problems

Design Note 192

Dave Thomas and Kevin R. Hoskins

A new 12-bit 3Msps ADC brings unparalleled levels of performance and ease of use to the high speed ADC user. Its successive approximation (SAR) method eliminates many problems found in pipelined and subranging ADCs in that speed range. This note describes these problems and introduces a new, simple-to-use alternative, the LTC®1412.

The LTC1412 offers an ideal combination of speed, performance and size. Some of its features and benefits include:

- Complete low power 12-bit 3Msps ADC
- Great AC performance: 72.5dB SINAD and 83dB SFDR at Nyquist
- Great DC performance: ±0.25LSB typical INL and DNL (±1LSB max)
- Three-state output bus with no pipeline delay (parallel I/O with DSP interface signals)
- Tiny 28-lead SSOP package

PIPELINE PROBLEMS

Pipelined ADCs are great for giving the fastest speed short of that provided by a full-flash converter. In fact, LTC manufactures both pipelined and subranging ADCs. However, at resolutions of 12 bits and higher, these architectures can have a number of fundamental drawbacks. These drawbacks include poor noise and SNR, complex reference circuitry, complicated input circuitry, pipeline latency and poor frequency domain performance. These parts have large package size and high power dissipation. They also lack three-state outputs.

THE LTC1412 BENEFITS

The LTC1412's block diagram is shown in Figure 1. Some of the benefits offered by the LTC1412 SAR ADC design, when compared to pipelined ADCs, are discussed below. The August 1998 issue of *Linear Technology* magazine contains more information.

Benefit #1: Cleaner Behavior and Great Linearity

The LTC1412 depends solely on capacitor matching for accuracy (it has no pipeline amplifiers or interstage S/Hs with their resulting errors). This results in typical 0.25LSB INL and DNL that have virtually zero drift. Figure 2 shows the LTC1412's typical INL and DNL performance. Another benefit is freedom from sparkle codes, to which pipelined ADCs are susceptible.

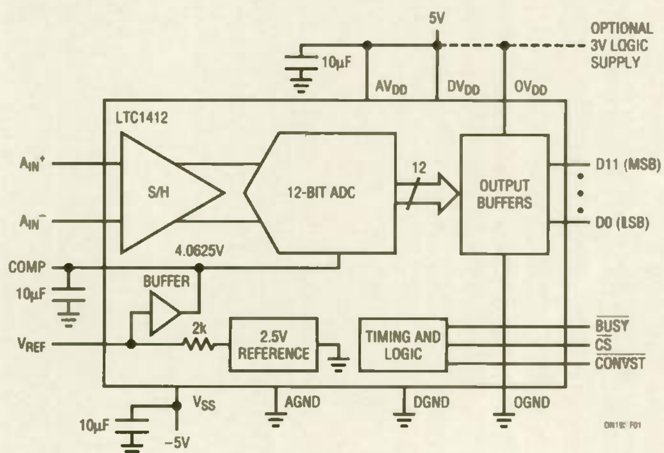


Figure 1. The LTC1412 Combines the Inherent Linearity of a High Performance 3Msps S/H and 12-Bit ADC with an Onboard Reference, µP/µC Logic Interface and Three-State Parallel Output Data Buffers

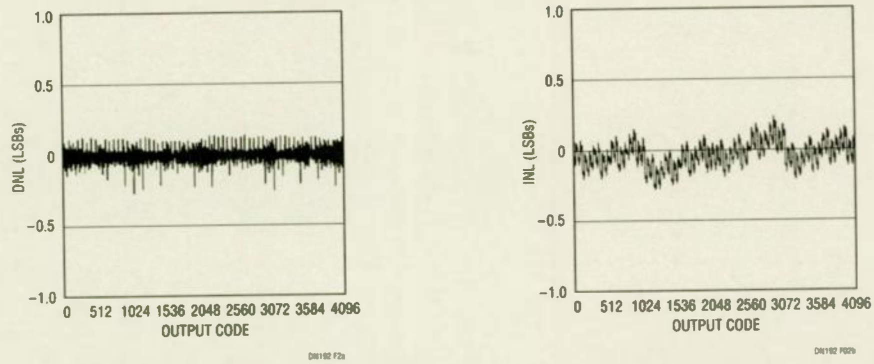


Figure 2 The LTC1412's Inherent Linearity is Shown in These INL and DNL Curves

Benefit #2: Lower Noise and Higher SNR

Pipelined ADCs add noise to their conversion because they resample the input signal as the conversion moves through the pipeline. Conversely, the LTC1412 has nearly perfect noise performance because its single S/H and single-pass conversion SAR architecture add almost no noise. This results in unsurpassed performance at 3Msps. Its 73dB (typ) SNR is within 1dB of the theoretical 12-bit ADC quantization noise. The LTC1412 also has premier distortion performance of 83dB spurious free dynamic range at Nyquist. Figure 3 shows an FFT of the LTC1412 at Nyquist.

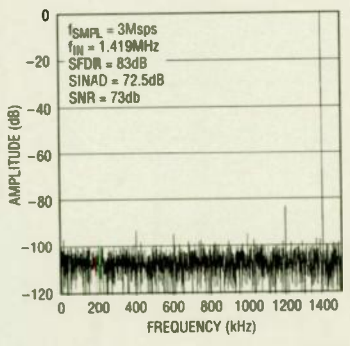


Figure 3. The LTC1412's Simple SAR Achieves 72.5dB SINAD and 83dB SFDR When Converting at 3Msps

Benefit #3: Simple Input and Reference Circuitry

The LTC1412's high impedance, differential input S/H and built-in reference greatly simplify analog support circuitry. The LTC1412's S/H eliminates the level shifting, complementary differential input signals or transformers typically required by pipeline ADC circuits. The LTC1412's reference does away with the multiple reference pins, multiple bypassing capacitors and fast reference buffer amps commonly required by pipeline converters. The LTC1412's internal reference maintains linearity over a 2:1 span adjustment voltage range. This flexibility covers a wide range of applications from communications to imaging.

Benefit #4: Easy Interface: Eliminates Pipeline Delay, Provides Three-State Outputs

Conversion data is present at the LTC1412's three-state output 300ns after the conversion begins, eliminating the pipeline delay, or latency, between the input sample and the corresponding output data. Having no pipeline, the LTC1412 does not suffer from time delay or phase shift, making it the choice in applications such as high speed servo-loop control systems and DSP, motor control, asynchronous or event-driven sampling and multiplexing.

Benefit #5: Small Package Size and Low Dissipation

While equaling the 3Msps pipeline ADCs' speed, the LTC1412's simple, efficient design and low power dissipation (150mW) allow small 28-lead SSOP surface mount packaging. This is much smaller than the packages used for pipeline ADCs, which can be as large as 44-lead PLCCs. Figure 4 compares the size of packages used for various pipeline ADCs and the SSOP packaged LTC1412.

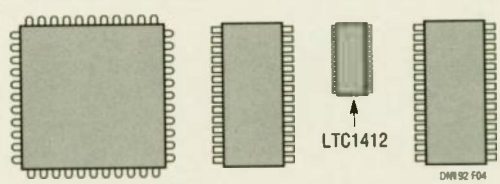


Figure 4. A Benefit of the LTC1412's Size and Power-Efficient Architecture is the Smallest Package Among 3Msps Parallel Output ADCs

Conclusion

Pipelined ADCs are useful at very high sample rates but they do have problems, as we have seen. Now, designers using pipelined 3Msps converters have a clean SAR alternative: the LTC1412. It is a sure cure for pipeline drawbacks and problems.

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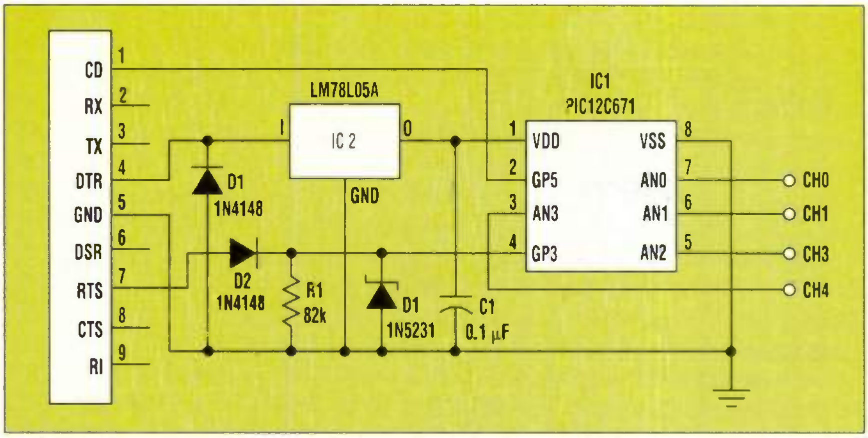
If there's one pulse, then channel 0 is selected for the A/D conversion. If the pulse count is 2, 3, or 4, channel 1, 2, or 3 will be selected. After the channel information is received, the microcontroller will start to perform the A/D conversion for the selected channel. Then the 8-bit A/D conversion data will be sent back to PC through the microcontroller's pin 2.

Since the PC may have a different serial port baud rate, it's necessary to send a training pulse to the PC before starting transmission of A/D conversion data. The PC program contains a loop to accept the training pulse. The number of loop iterations that execute before the training pulse reception is completed determines the baud rate used for reception of the A/D conversion data from the microcontroller.

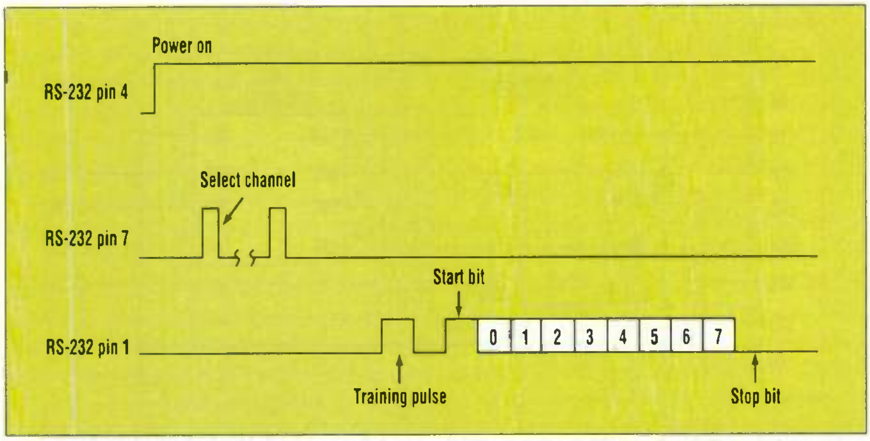


1. This simple circuit uses an 8-pin microcontroller to implement an 8-bit, 4-channel analog-to-digital converter that can plug directly into the serial port, needing no external power supply.

Listing 1 is the assembly program for PIC12C671 microcontroller and Listing 2 is the C program for the PC.

The C program will read four inputs every second and will display the results on the PC screen.

```
/*---------------------------------------------------------*/
/* 4-channel A/D conversion for a PC                       */
/* author:          Yongping Xia                           */
/*---------------------------------------------------------*/

#include <stdio.h>
#include <dos.h>
#include <conio.h>

#define MCR         4       /* control register     */
#define MSR         6       /* status register      */
#define REF_VOL     5       /* reference voltage    */

int     i, j, k,
        data, read_ad, dly_cnt, dummy,
        temp_1, temp_2,
        base_add1=0x3f8,
        base_add2=0x2f8;
float   dis_data;

void set_port( void )
{
        outportb( base_add1+MCR, 0x00 );    /* power off, reset uC  */
        delay(100);
        outportb( base_add1+MCR, 0x01 );    /* DTR high, power on   */
        delay( 200 );
}

void dly_lp( int count )
{
        dummy=1;
        for ( j = 0 ; j<count ; j++ )
        {
                read_ad=inportb( base_add1+MSR ) & 0x00;
                if ( dummy!=0 )
                        dummy++;
        }
}

void find_error( int error_num )
{
        printf( "Communication error %d, hit any key to quit", errorvnum ), exit(1);
}

void get_delay( void )
{
        dly_cnt = 0;
        for ( j = 0 ; j<30000 ; j++ )
        {
                read_ad=inportb( base_add1+MSR ) & 0x80;
                if ( read_ad=0 )
                        dly_cnt++;
                else
                        j=30000;
        }
        if ( j == 29999 )
                find_error(1);
}

int ad_conversion( int channel )
{
        for ( k = 0 ; k<channel+1 ; k++ )
        {
                /* send channel number          */
                outportb( base_add1+MCR, 0x03 );
                delay(1);
                outportb( base_add1+MCR, 0x01 );
                delay(1);
        }
        data = 0; j = 0;
        do {
                /* waiting for training bit     */
                temp_1=inportb( base_add1+MSR ) & 0x80;
                temp_2=inportb( base_add1+MSR ) & 0x80;
                j++;
        } while( ( temp_1 == 0 || temp_2 == 0 ) && j<10000 );

        if ( j == 10000 )
                find_error(2);
        get_delay( );
        dly_ lp( dly_cnt/2 );
        j=0;
        do {    /* waiting for start bit        */
                temp_1 = inportb( base_add1+MSR ) & 0x80;
                temp_2 = inportb( base_add1+MSR ) & 0x80;
                j++;
        } while( ( temp_1 == 0 || temp_2 == 0 ) && j<10000 );

        if ( j == 10000 )
                find_error(3);
        dly_lp( dly_cnt*1.5 );
        for ( k = 0 ; k<8 ; k++ ) {
                data /= 2;
                temp_1 = inportb( base_add1+MSR ) & 0x80;
                if ( temp_1 != 0 )
                        data += 0x80;
                dly_lp( dly_cnt );
        }
        return data;
}

void main( void )
{
        set port( );
        do {
                clrscr( );
                for ( i = 0; i<4; i++ )         /* scan 4 channels      */
                {
                        dis_data = (float) ad_conversion( i )*REF_VOL/256;
                        printf( "Channel %d = %.2fV\n", i, dis_data );
                        delay( 20 );
                }
                gotoxy( 60, 24 );
                printf ( "Hit any key to quit" );
                delay( 1000 );
        } while( !kbhit( ) );
}
```



2. Commands are sent to the PIC12C671 microcontroller by the PC through pin 7, and the microcontroller sends information back to the PC through pin 2.

Circle 521

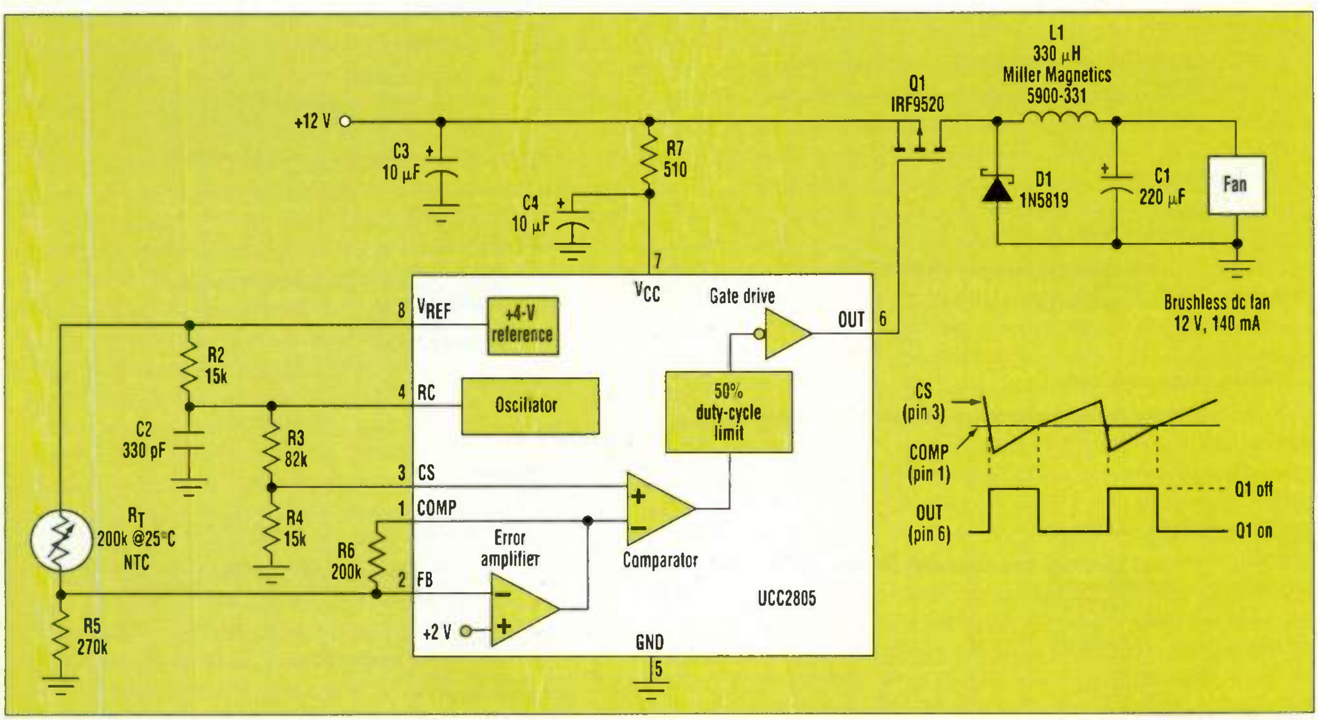
Improved Efficiency Fan-Speed Control

JOHN MCNEILL, NINA TJOA, LUIS MENEZES, AND JEFF KULESZA
Worcester Polytechnic Institute, 100 Institute Rd., Worcester, MA 01609; (508) 831-5567.

Reducing the operating speed of a system cooling fan not only saves power, but also extends the operating life of the fan and lowers acoustic noise. Fan speed can be controlled by sensing the ambient temperature in the system enclosure and reducing the fan supply voltage unless a temperature rise is detected. A previous design by Don Alfano (*"Fan Speed Control Adjusts to Temperature,"* ELECTRONIC DESIGN, *Analog Applications Issue, Nov. 18, 1996, p. 83*) for a 12-V brushless dc fan used a linear-voltage-regulator approach to provide fan voltages ranging from 6 to 12 V.

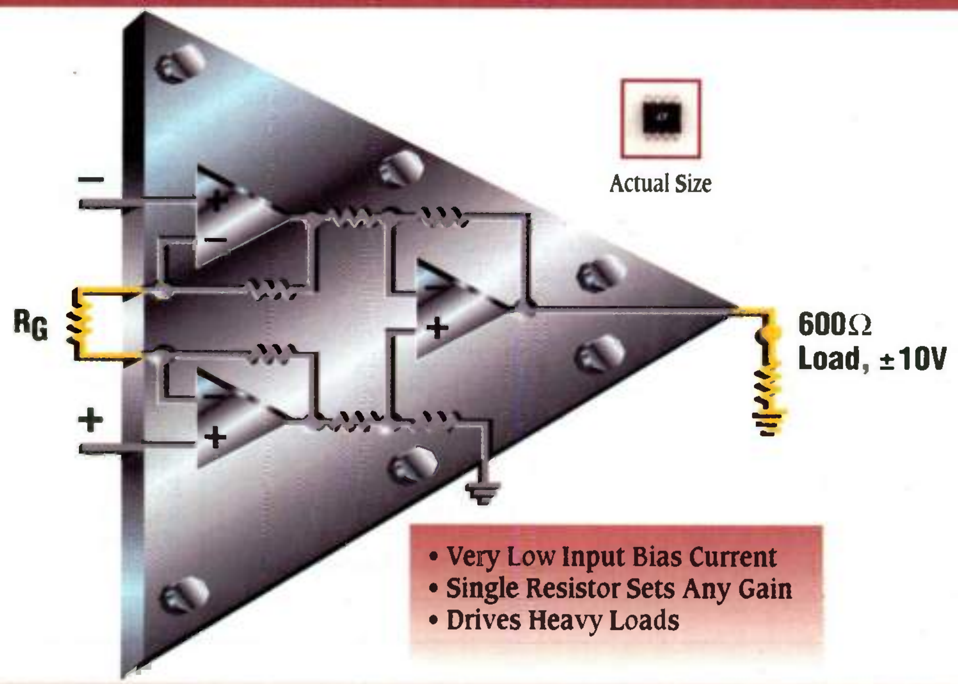
An alternative to the linear regulator, which provides even greater power savings, is the temperature-controlled pulse-width-modulator (PWM) approach *(Fig. 1)*. The circuit is a buck-converter based on the Unitrode UCC2805, a single-chip biCMOS PWM controller that contains all of the necessary circuitry (voltage reference, error amplifier, comparator, MOSFET gate drive, and oscillator) for closed-loop PWM power-supply control.

The UCC2805, which can be configured for either voltage-mode or current-mode feedback, is used here in a voltage-mode configuration controlling the buck-converter formed by Q1, D1, L1, and C1. A P-channel MOSFET is used, rather than N-channel, because the required gate drive for the P-channel device is much simpler. The lower $r_{DS(ON)}$ of an N-channel device isn't necessary, given the modest power requirement. As shown in the



Power efficiency can be improved dramatically by using this temperature-controlled pulse-width-modulator (PWM) buck-converter to drive the brushless dc cooling fan. Extended fan life and reduce acoustic noise are secondary benefits of this approach.

Industrial Strength Instrumentation Amp



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$G=1+49.4k/R_G$

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100	499Ω
1000	49.5Ω
10,000	4.94Ω

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timing diagram in Figure 1, the duty cycle of the switch drive signal OUT at pin 6 is determined by on-chip comparison of the control voltage, COMP (pin 1), to a sawtooth waveform, CS (pin 3).

The frequency of the on-chip PWM oscillator is set to 120 kHz by R2 and C2. The R3/R4 network attenuates the charge/discharge waveform on the oscillator timing capacitor C2. As a result, a sawtooth waveform is developed at CS of the proper amplitude for comparison with the COMP.

Temperature information is incorporated into the control voltage by R_T, a negative-temperature-coefficient (NTC) thermistor that's included in the R_T/R5/R6 network of the error amplifier. The effect of temperature on the fan speed can be seen by following the control signal around the loop from R_T to the fan supply voltage. When the ambient temperature increases, the value of R_T decreases, increasing the current in R_T, and reducing the value of the control voltage, COMP, at the output of the error amplifier. This changes the duty cycle of the comparator output and MOSFET gate drive so that Q1's "on" time increases. This in turn increases the output voltage of the buck-converter supplying the fan, thus boosting the fan operating speed.

The fan speed versus temperature profile is characterized by two temperature points: T1 (below which the fan runs at half speed, with a supply voltage of 6V) and T2 (above which the fan runs at full speed, with the full 12V supply). The desired temperatures for T1 and T2 determine the values of resistors R5 and R6, which scale and shift the control voltage at the output of the error amplifier. The resistances are determined from the values of the thermistor R_T(T1) and R_T(T2) at temperatures T1 and T2:

$$R5 = \frac{1.2 \times R_{T(T1)} \times R_{T(T2)}}{\left[2.2 \times R_{T(T2)}\right] - \left[R_{T(T1)}\right]}$$

$$R6 = \frac{0.3 \times R_{T(T1)} \times R_{T(T2)}}{R_{T(T1)} - R_{T(T2)}}$$

The values shown in the schematic correspond to T1 = 77°F and T2 = 86°F, at which the thermistor had values of 200k and 154k, respectively.

An on-chip control block limits the minimum duty cycle to 50%, corresponding to a minimum fan voltage of 6 V. This prevents stalling, which occurs at a fan supply voltage of about 4 V. Measurements on the circuit show an efficiency greater than 90%. The power consumed by the fan when operating at half speed was 26% of the full speed power consumption.

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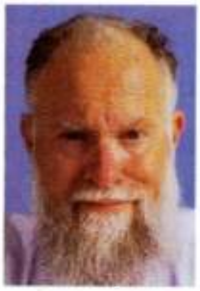

Dear Mr. Pease:

Re: "What's All This Stuff, Anyhow? Volume Three," that accompanied the Aug. 3, 1998 issue of *ELECTRONIC DESIGN*:

Laboring under a stereotype of my youth until I read your memories of Bob Widlar, I thought of you as nearer my own age. I apologize! In my younger days, the old codgers wore the beards. Now that I'm past 80, it's the young bucks who wear them!

Seriously, though, I can empathize with your typing trials and tribulations. Since my mother was only a farm girl and a housewife, she couldn't teach me how to type. I did take a year of typing in high school (which I barely passed) because my penmanship was atrocious. And, I wanted to be able to submit legible papers in college.

It did teach me the fundamentals of touch typing. However, I suffered from the same problem as you. It wasn't until I got my Commodore 64, with a word processor known as SpeedScript, that I became a real touch typist. Being able to correct errors easily, without resorting to an eraser, Erasable Bond, correction tape, or Liquid Paper, gave me the confidence I needed to become good at it. (I still cheat occasionally, though!) Now I use a homebrewed 486DX40, running WordPerfect 6.0 under DOS. (I refuse to bow to Gates, unless a total meltdown forces me.)

About carpal tunnel syndrome: We never heard of it among the thousands of women (secretaries and stenographers) who—before Selectrics, computers, and word processors—spent their days banging away on manual typewriters. All—or most of them—were touch typists. The only time I experienced it was in 1980 when I had to spend hours on a Model 33 Teletype, punching paper tapes to program a minicomputer. If you ever experienced one of those atrocities, you'll know that you had to literally HAMMER the keys to accomplish anything. The only way to do that was by WRIST motion—fingers were too weak.

I doubt if many, or any, of those who suffer from carpal tunnel syndrome as a result of operating computer keyboards are touch typists. I'd venture that most of them use the "two-finger punch" method, with lots of lateral wrist motion. If they won't learn to touch type, they could avoid a lot of pain and suffering by changing to a stiff-wrist, forearm motion.

ROBERT J. NEDRESKI
via e-mail

Yeah, I'm just a kid of 58. (When I graduated from MIT, I was barely 21.) The earlier you start learning touch-typing—or any other strange "language"—the better. My mother was a farm girl—and a housewife—and a MOTHER—and a TEACHER. Ain't every mother a teacher? Hope so!—RAP

Dear Bob:

Thanks for the "What's All This Widlar Stuff, Anyhow?" in the Aug. 3, 1998, "What's All This Stuff, Anyhow? Volume Three." I have always enjoyed Bob Widlar anecdotes. I used the early LM709 op amps and most of the other Widlar creations. Wasn't the LM108 Widlar inspired? If he were alive today, we might be working with monolithic 26-bit digital-to-analog converters, etc. What a genius!

BILL BILLINGSLEY
via e-mail

Yeah, Widlar invented the LM108 about 30 years ago. But if he were still around, we would have 31-bit op-amps. However, we now DO have 30-bit (resolution) op-amps such as the LMC2001. Twenty-six bits is not a big deal.—RAP

All for now. / Comments invited!
RAP / Robert A. Pease / Engineer
rap@web team.nsc.com—or:

Mail Stop D2597A
National Semiconductor
P.O. Box 58090
Santa Clara, CA 95052-8090

256-Macrocell CPLD Boasts 7.5-ns Pin-To-Pin Delay

The 3.3-V EPM7256A CPLD offers industry-leading performance with pin-to-pin delays as fast as 7.5 ns. Designed using the company's second-generation Multiple Array Matrix (MAX) architecture, the 256-macrocell EEPROM-based device features 16-logic array blocks, 164 I/O pins, and up to 5000 usable gates.

Altera's patented MultiVolt interface enables I/O support of 5.0-, 3.3-, and 2.5-V interface voltage levels, and in-system programmability with support of the Jam programming and test language. The EPM7256A is a true 3.3-V CPLD fabricated using a 0.35-µm process. It's available now in a 208-pin PQFP package, and will soon be available in 100-pin TQFP, 144-pin TQFPs, and Altera's new FineLine BGA packages. By the end of this year, volume pricing is expected to be $15.50 in 25,000-unit quantities. DB

***Altera Corp.**, 101 Innovation Dr., San Jose, CA 95134; (408) 544-7000; www.altera.com.* **CIRCLE 525**

Gate Arrays Target The FPGA Conversion Market

The Cutthroat gate-array family is targeted at communication and EDP companies looking to perform FPGA-to-ASIC conversions. Cutthroat delivers PCI-ready ASICs with I/O performance of 66 MHz and clock-to-out performance in the 5-ns range. The gate-array family was created using an enhanced version of AMI's 3.3-V, 0.5-µm digital CMOS process. Such enhancements include refinements to the I/O architecture so that users can take advantage of the high-speed core logic. The family also features multiple speed indexes for all library components. This feature has been fine-tuned to work with the latest generation of synthesis technology to produce high-performance and area-efficient designs.

Cutthroat products are offered in both 5- and 3-V core processes with 5-V tolerant I/O. The core operating voltage can be different from the I/O voltage. Cutthroat also offers a 3.3-V chip with both 5- and 3.3-V supply pins. Cutthroat users are offered vectorless translation of FPGAs to ASICs, which requires only the netlist and critical timing information. Typical translation costs include a NRE cost ranging from $10,000 to $50,000, depending on the design's size and complexity. Delivery is less than four weeks. DB

***American Microsystems Inc.**, 2300 Buckskin Rd., Pocatello, ID 83201; (208) 233-4690; www.amis.com.* **CIRCLE 526**

Timing Simulator, FSM Editor Added To Low-Cost PLD Tool

Cypress Semiconductor has plans to include Aldec's timing simulation and finite-state-machine (FSM) editing in its Warp2 programmable-logic tool. The company will include these new features in an upcoming release with no additional cost to users, maintaining the software's $99 price tag. The FSM Editor enables graphical design entry and automatic HDL generation. The timing simulation is based on a structural VHDL netlist for post-fitting simulation. The simulation technology being used by Cypress is a subset of Aldec's complete product, and will enable timing simulation for Cypress device families only. The PC-based Warp2 tool can be purchased over the Internet and by phone. DB

***Cypress Semiconductor Corp.**, 3901 N. First St., San Jose, CA 95134-1599; (408) 943-2600; www.cypress.com.* **CIRCLE 527**

Look For Rad-Hard Version Of AT6010 Reconfigurable FPGA

Atmel and Honeywell have teamed to develop a radiation-hardened version of Atmel's 30,000-gate 6400-register AT6010 FPGA. The development effort is being funded and managed by the NASA Goddard Space Flight Center. Honeywell will develop a CMOS silicon-on-insulator (SOI) version of the part to meet the rad-hard levels required by commercial and military space and missile systems. SOI technologies offer lower power consumption and improved speed over other silicon technologies. The new device will be fully compatible with Atmel's commercial FPGA, allowing users to take advantage of the company's existing design software. For more information on the rad-hard technology, visit the Honeywell web site at *www.honeywell.com*. DB

***Atmel Corp.**, 2325 Orchard Pkwy., San Jose, CA 95131; (408) 451-2855; www.atmel.com.* **CIRCLE 528**

2.7-V MCU Support Chip Cuts Power Drain By 97%

Designers can add logic or program store to their MCU-based designs without adding a lot of power drain. The 2.7-V ZPSD6XXV MCU support IC integrates a 2500-gate CPLD, 128 kbytes of EPROM, 512 bytes of SRAM, extra I/O, and a programmable interface to most 8- or 16-bit microcontrollers. However, the ultra-low-power device consumes 97% less power than a discrete solution with comparable functionality, making it an ideal choice for portable battery-operated systems. In a system operating at 1 MHz, the ZPSD6XXV consumes only 0.76 mA, including I/O loading. This is 97% less than the 25.1 mA consumed by a 3-V solution that includes the same memory and logic densities, and the same I/O. In standby mode, the support chip requires just 1 µA, 99% less than the discrete solution. The ZPSD6XXV MCU support IC is available now in 52-pin ceramic and PLCC packages. Prices start at $5.15 in quantities of 10,000. DB

***WSI Inc.**, 47280 Kato Rd., Fremont, CA 94538; (510) 656-5400; e-mail: info@wsipsd.com.* **CIRCLE 529**

Dense, High-Speed CPLD Aims At Value-Minded Users

The newest member of the 5-V XC9500 family targets the sweet spot of the in-system programmable CPLD market with a very low price per macrocell. The XC95144 device has 144 macrocells, a 7.5-ns pin-to-pin speed, and is the first family member built on a new advanced process technology. Xilinx' FastFlash process technology developed by United Microelectronics Corp. in Taiwan offers more than a 50% die size reduction compared to the initial 0.6-µm process. Smaller die size allows Xilinx to offer a very low priced, high-performance CPLD. The XC95144 device is available in a100-pin PQFP for $12.50 in 100-piece quantities. High-volume pricing is expected to be $6.95 by mid-1999. DB

***Xilinx Inc.**, 2100 Logic Dr., San Jose, CA 95124-3400; (408) 559-7778; www.xilinx.com.* **CIRCLE 530**

Multi-line Code XDSL Chip Set Runs DMT, CAP, 2B1Q

The new G7000 family of multi-line code DSL chip sets is capable of supporting virtually all xDSL line codes, including 2B1Q, CAP, and DMT T1.413 Issue 2 with upgradability to G.lite and T1.413 Issue 3. All G7000 products employ a low-power, fully programmable, highest-performance DSP that can support current and anticipated DSL standards. The most recently introduced version of the chip set is interoperable with widely deployed DSL systems that use 2B1Q, CAP, or DMT line codes, allowing designers to easily migrate their designs.

The chip set is based on a programmable billion-operations-per-second (BOPS) DSP core specifically designed to support all popular xDSL line codes, including 2B1Q, CAP, and DMT. It allows the G7000 DSP chip to offer very low power consumption at less than 0.5 W for operation, making it especially suited for high-density products located in central-office and digital loop carrier systems.

A design kit for the G7000 is available today, complete with DSL reference designs, evaluation systems, and device drivers to speed up product development. The manufacturer also offers development assistance, including access to its world-class xDSL system test lab for DSL product performance and standards interoperability compliance testing.

The G7000 chip-set family is available now in a variety of packages, with OEM volume prices starting at $39. LG

GlobeSpan Semiconductor Inc., 100 Schulz Dr., Red Bank, NJ 07701; (732) 345-7500; fax (732) 345-7592; www.globespan.net. **CIRCLE 531**

GaAs HBT RFICs Offers Power, Price, And Performance

Targeted at a wide range of mobile wireless applications, a new family of six RF ICs uses the advantages of GaAs HBT technology to deliver high levels of power efficiency and performance. The family consists of an isolation amplifier, a variable gain amplifier (VGA), a broadband driver amplifier, a low-noise amplifier (LNA), and a pair of upconverters. These parts are intended for use in receivers and transmitters operating in the 500-MHz to 3-GHz range that require high linearity and operation on a single voltage power supply as low as 3.0 V.

The EC-0006 high-isolation limiting amplifier provides top reverse isolation and excellent VSWR characteristics. It yields a typical gain of 25 dB and achieves a typical isolation level of 40 dB at 1900 MHz. Its companion, the EC-0017, is a high-performance, internally matched VGA that offers low power consumption while delivering 12 dB of gain and a control range of 50 dB. It features internal 50-Ω matching, high linearity, and very low power consumption (55 mA operating, 0.5 mA standby). The EC-1017is a broadband driver amplifier that contains an internal matching network. It boasts a typical gain of 9 dB, with an output signal level of +15 dBm at 1 dB of compression.

Receiver applications are covered with the EC-5007, an integrated LNA and broadband mixer. It provides 7 dB of conversion gain. The EC-5057 and EC-5117 are upconverters, delivering typical gains of 4.5 dB and 8 dB of gain, respectively. Output power for the two chips is –3 dBm and –6 dBm, respectively.

All parts are packaged using either plastic SOICs or QSOPs to minimize board space and volume in critical mobile applications. The EC-0006, EC-0017 , EC-1017, EC-5007, EC-5057, and EC-5117 are available now. In sample quantities, a collection of ICs suitable for a transceiver should cost less than $25, with substantial volume discounts available. LG

EiC Corp., 45738 Northport Loop W., Fremont, CA 94538; (510) 445-4700; fax (510) 445-4701. **CIRCLE 532**

0.25-mm ASICs And System IP Target Communication Apps

A family of deep-submicron ASIC products is now available in combination with a library of intellectual property (IP) and design tools for the design of complex communication ICs. Fabricated in 0.25-µm CMOS, the MG113P/114P/115P gate-array series and the MG73P/74P/75P embedded-array series gives engineers up to 5.4 million raw gates, allowing them to embed large RAM arrays and make use of a wide range of IP cores in their designs. These include a Gigabit Ethernet MAC, an ARM RISC CPU, DSPs, codecs, DRAMs, ROMs, ATM SARs, and PCI controllers. Up to five layers of metal interconnect are supported. Specialized electrical I/O also is supported, including PECL and LVDS. All products operate on nominal supply voltages as low as 2.5 V and as high as 3.3 V. Packaging is available in QFP and BGA formats, with up to 868 contacts.

The full specifications and design tools for the full family of ASIC products is available now, with full production slated for the fourth quarter of this year. Pricing in a QFP package will be around 0.005 cents per gate. LG

Oki Electric Industry Co. Ltd., 785 N. Mary Ave., Sunnyvale, CA 94086-2909; (408) 720-1900; fax (408) 720-1918, www.okisemi.com. **CIRCLE 533**

Wireless LAN PC Cards Deliver Up To 11 Mbits/s

Offering full interoperability with the IEEE 802.11 wireless LAN standard, the Aironet 4500 series of products uses direct-sequence spread spectrum (DSSS) for reliable data transport in the 2.4-GHz band. The current generation of products supports both the 1- and 2-Mbit/s data rates specified by 802.11, and an upgraded series of products capable of 11 Mbits/s will be available later this year. The current family of products includes a type-II PC-card-sized mobile LAN adapter. It comes with software drivers for most popular operating systems (Microsoft, Novell, and others), and features an advanced power-management system that helps conserve battery power. Also available are two access points which can provide connectivity to either Ethernet or token-ring wired networks. The base stations can be configured and monitored remotely using standard protocols, such as Telnet, FTP, SNMP, and most web browsers.

Available now, the PC card mobile LAN adapter costs $595 in single-piece lots. The Access point costs $1795 each with an Ethernet interface, and $2395 with a token-ring interface. LG

Aironet Wireless Communications Inc., 367 Ghent Rd. Suite 300, P.O. Box 5292, Fairlawn, OH 44334-0292; (330) 664-7900; fax (330) 664-7922. **CIRCLE 534**

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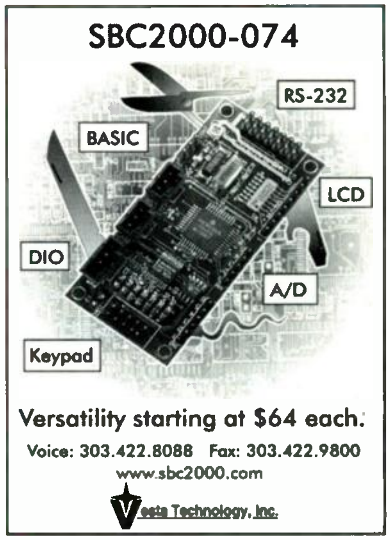

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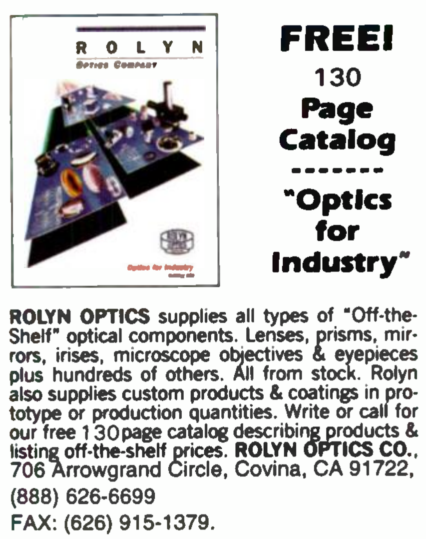

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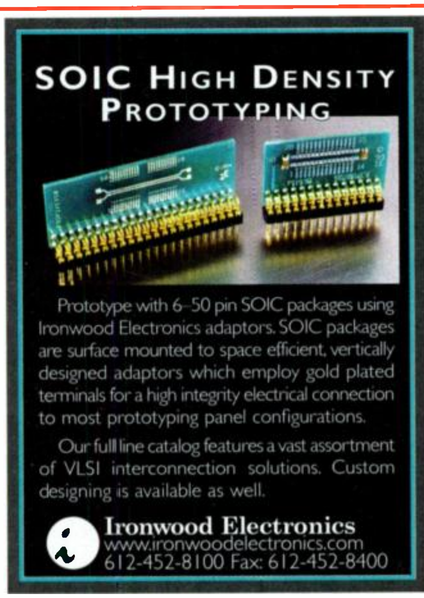

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Ideal candidates will have a minimum of two years experience in analog/digital circuit design and control modules. Knowledge of PSPICE and MATHCAD are a plus. Individuals in this position will be responsible for the design and development of control modules; schematic capture; circuit design and simulation; worst case analysis; development of prototype hardware; and program management of module design development schedule and delivery.

AUDIO PRODUCTS DESIGN ENGINEER (V8-360)

This position is responsible for development of the next generation of audio systems. A minimum of two years experience in either audio subsystem, product engineering, electronic circuit design, IC applications, or audio component design is required. To achieve this goal, the chosen individual will interface with component engineers on radio rear seat control, steering wheel control, CDDJ's, and CD players. Additionally, this position will provide program management for outsourced audio product development.

ELECTRICAL SYSTEMS ENGINEER (V8-597)

Degrees in Mathematics, Physics, or Control Systems will also be considered. A minimum of five years experience designing electrical or electronic systems or hardware is required. This individual will apply their skills toward the integration of electronics subsystems into complex products or vehicles from concept level to prove out. To handle this successfully, candidates must be experienced in using established systems engineering methodology; system-level behavioral modeling, simulation, and model validation; and applying control theory. Familiarity with cooling and packaging electronics and software design or specifications is a plus.

MECHANISMS DESIGN ENGINEER (V8-988)

With a minimum of two years experience, this position will offer the engineer the opportunity to work with an experienced group of fellow engineers to integrate current and advanced multimedia systems. The engineer will design and release multimedia playback mechanisms; conduct feasibility studies; and work with suppliers to support manufacturing engineering, resolution of quality issues, cost reduction efforts, and development of related technology road-map.

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Two or more years experience in 32-bit embedded design using PLD's, memory, peripheral IC's, 16/32 bit microprocessors, DSP's, and PCI bus is required. Experience with serial interfaces, and LCD/CRT controllers is essential. Assembly, C, and real time operating systems knowledge preferred. This hardware engineer will handle the design of a PC in the car that supports a variety of applications such as voice recognition, navigation, audio, wireless services, GPS, and Internet. The individual must be able to design and deliver system functionality from system level requirements and block diagrams.

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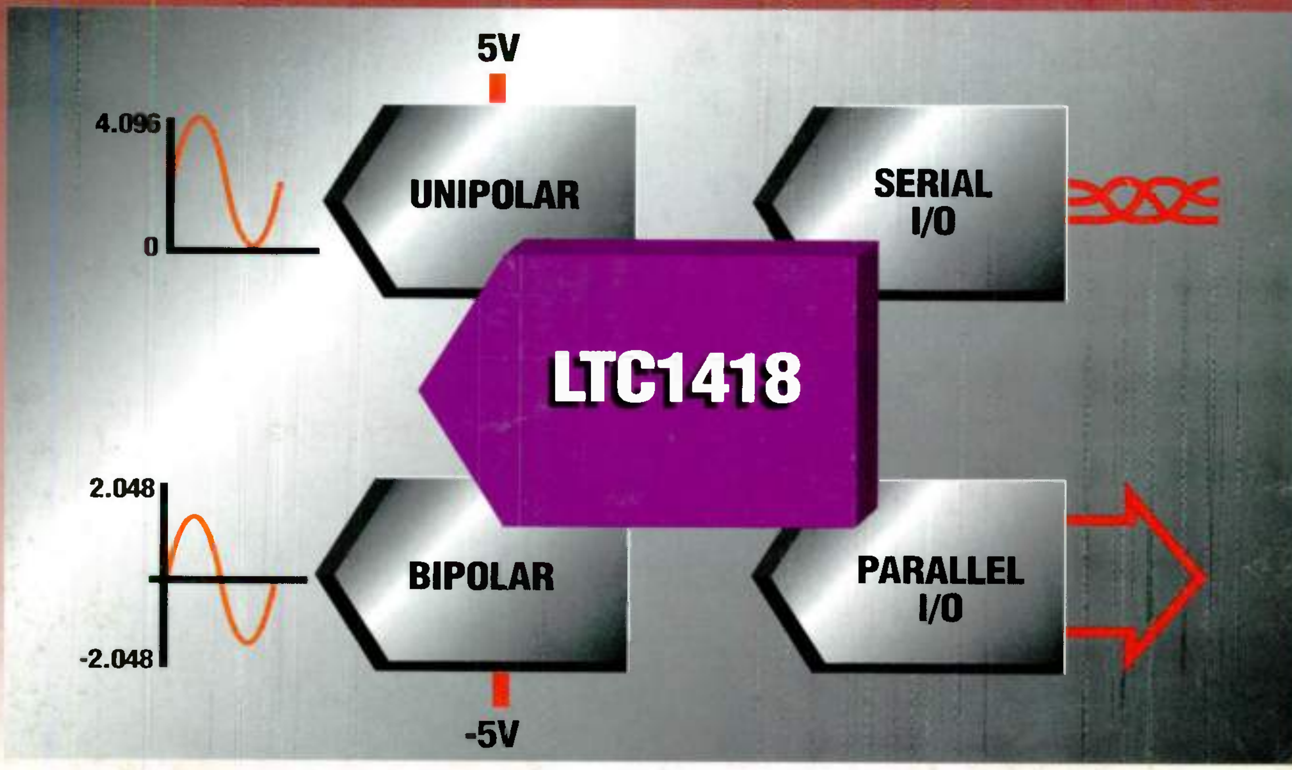

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