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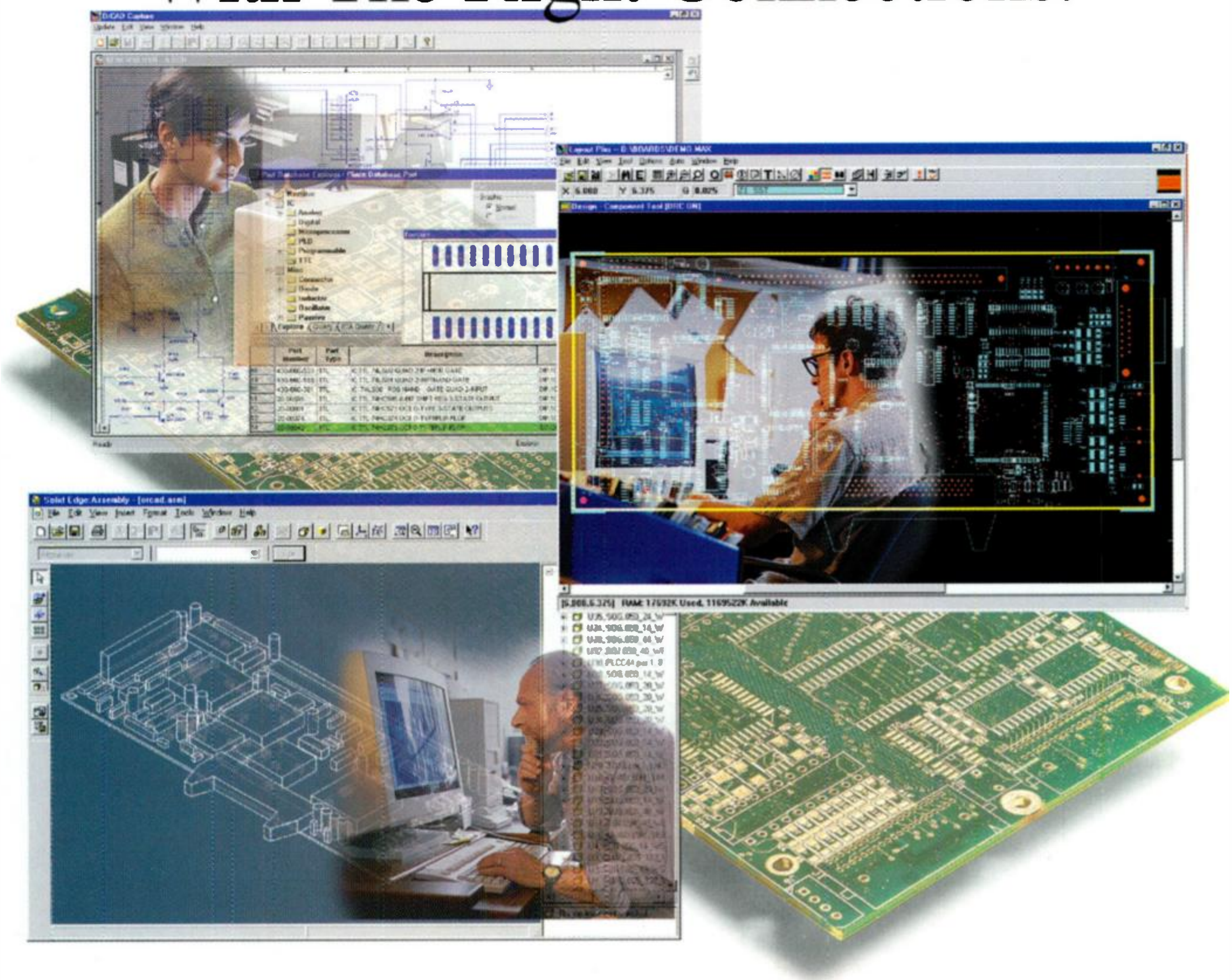

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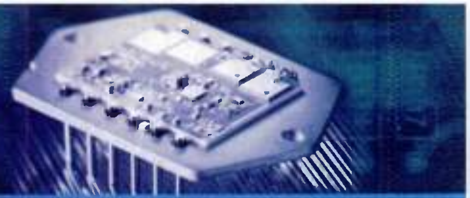

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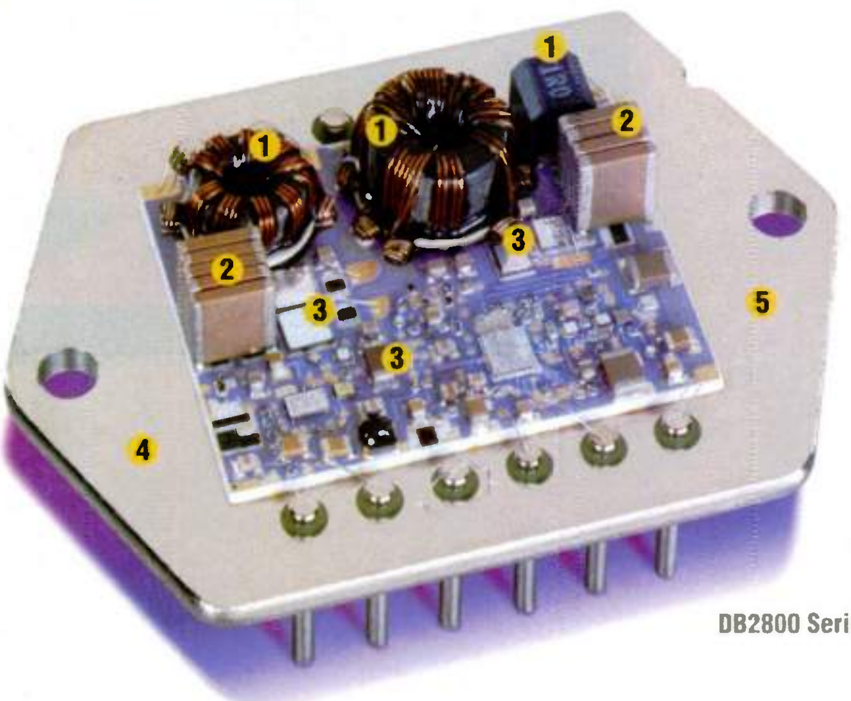

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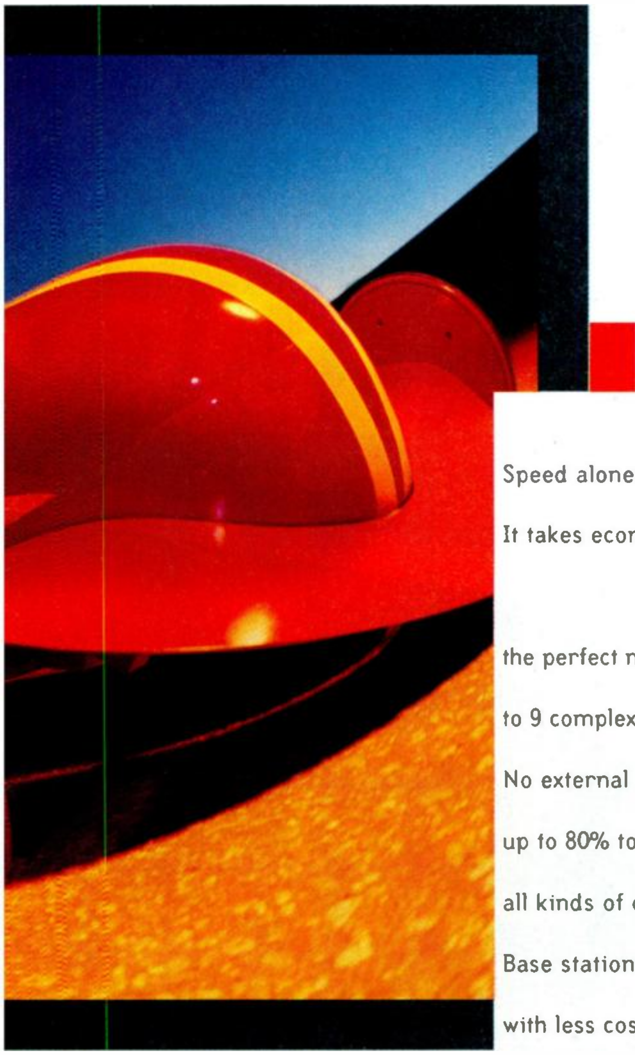

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November 2, 1998 Volume 46, Number 25

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TECH INSIGHTS

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November 2, 1998 Volume 46, Number 25

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LOOKING AHEAD: November 16, 1998

● Digital Technology: A Special Report by Digital ICs Editor Dave Bursky takes the wraps off the latest generation of x86 microprocessors—the ones designers can expect to get their hands on.

● Embedded Systems: Test & Measurement Editor Joseph Desposito explores the role visual tools are playing in embedded systems for factory automation and process control in this Special Report.

● Special Analog Supplement: Analog, Power Devices & DSP Editor Ashok Bindra discusses the trend toward adding digital functions and memory on analog ICs. Design articles and briefs round out the issue.

Jesse H. Neal Editorial Achievement

1967 First Place Award	1978 Certificate of Merit
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1972 Certificate of Merit	1986 First Place Award
1975 Two Certificates of Merit	1989 Certificate of Merit
1976 Certificate of Merit	1992 Certificate of Merit

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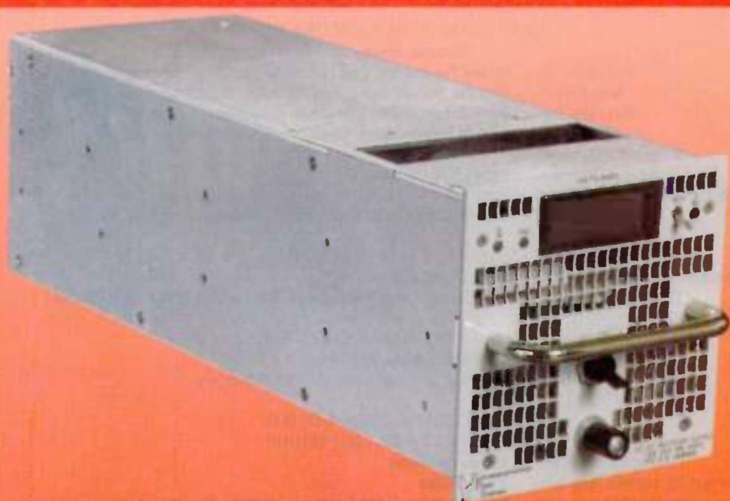

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Working In An E-Lance World

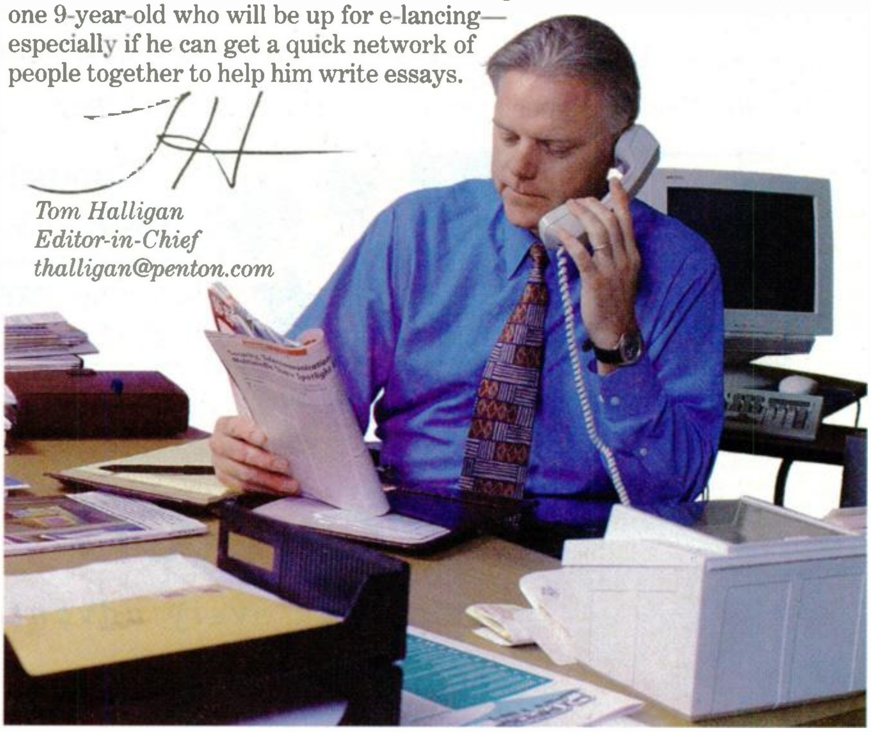
My 9-year-old son's school assignment was to write a 150- to 300-word essay on, "How Computers Have Changed Your Educational Experience." After reading his first draft, I sadly informed him that although what he penned was OK, his work was about 100 words short of the minimum requirement. By the look on his face, you would have thought he was being asked to write an epic the size of *Ulysses*.

After spending some time actually thinking about all the things a computer can do, he proudly returned with his word-count-verified, 151-word essay. I can't blame him for the less-is-more approach. After all, he's the son of an editor. But, what caught my eye reading his final draft was the amount of emphasis he put on the Internet over the other programs and tools the computer provides: "Looking up stuff" (research); "Talking to people" (e-mail); and "Buying Beanie Babies" (e-commerce) were the neat things a computer could do to enhance his fourth-grade "educational experience."

Routine functions such as word processing, playing games, and creating graphics are old hat to most of today's kids because they've always had access to a computer. They don't understand the convenience of it. To them, the computer is just a tool used to get their homework done and kill some time playing CD-ROM games. But, add an Internet connection and the computer morphs into a whole new animal for kids. I guess I shouldn't be surprised that the focus of his essay was on what the Internet can do, rather than the computer itself. To update Sun Microsystems' mantra: The Internet (not the network) is the computer, and it's the reason that sub-$1000 PCs are selling a heck of a lot more than their brawny and more expensive siblings.

I recently read an article in the *Harvard Business Review* authored by two scholarly guys who contend that we're now moving into the "Dawn of the E-Lance Economy" (September/October 1998). Not knowing what an "e-lance" was, I inquired and was told that, "The dominant business organization of the future may not be a stable, permanent corporation, but rather an elastic network that may sometimes exist for no more than a day or two (to complete a project). Once the project is done, the network will disband and the e-lancers (workers) will move on to their next job via the Internet."

Some of us may have doubts about working in an e-lance world. But, I know one 9-year-old who will be up for e-lancing—especially if he can get a quick network of people together to help him write essays.



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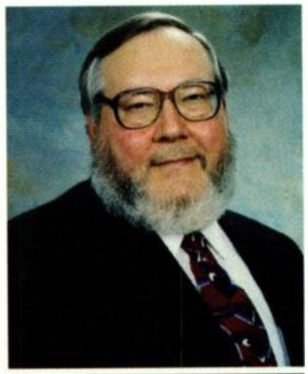
The Incredible Shrinking Transistor

It wasn't so long ago that designing ICs with 1-µm minimum feature sizes was considered the leading edge. However, at next month's IEEE International Electron Devices Meeting at the San Francisco Hilton and Towers Hotel in California, Dec. 6 through 9, I'm reminded as to how fast the semiconductor industry moves. At the upcoming conference, researchers will detail various approaches to achieving circuits based on features an order of magnitude smaller—just 0.1 µm. Such small feature sizes present tremendous challenges to designers responsible for developing the fabrication tools and processes required to implement the transistors and interconnect structures.

As the minimum feature size decreases, so must the width of the metal lines that interconnect the smaller transistors. Thinner lines do not bode well for circuit performance, since wiring resistance will go up. And, unless new low-K dielectric materials are used, parasitic coupling capacitances will increase. The higher R and C values can significantly impact the performance gains expected by moving to smaller feature sizes, since the higher RC product will have a doubly negative effect on signal delay.

Of course, researchers have been hard at work coming up with solutions for that problem. For instance, in Session 37, Motorola Inc., Austin, Texas, will detail a 0.1-µm CMOS technology that operates from a 1.5-V supply and employs a scaled copper-metallization scheme and a dielectric material with a dielectric constant (K) of less than 3.5. To create the small features, Motorola's designers employ complementary phase-shift masks and six levels of scaled copper interconnects to tie all the transistors together. For physical fabrication, a chemical-mechanical-polishing approach planarizes the shallow trenches that were first optimized with a high-energy retrograde well profile to provide good electrical isolation between transistors, even with active spacings of just 0.175 µm between transistors. That very tight packing density, coupled with six levels of metal interconnect, permits extremely dense circuits to be fabricated.



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Motorola is just one of many companies pushing to craft circuits with 0.1-µm or smaller minimum features. In Session 22, Texas Instruments Inc., Dallas, Texas, will detail the process and design issues for a 1.2-V, 0.1-µm CMOS process. Researchers from IBM Corp., Hopewell Junction, N.Y., will describe a sub-0.08-µm dual-gate-oxide process that achieves inverter delay times of just 9.7 ps when operating at 1.5 V. An overview of the progress in achieving 0.1-µm devices will also take place in that session by researchers from Bell Laboratories and Lucent Technologies, Murray Hill, N.J. Additional presentations by Fujitsu Ltd., Tokyo, Japan, and Philips Research Labs, Eindhoven, The Netherlands, in conjunction with the University of Twente, Enschede, The Netherlands, will highlight other techniques to fabricate 0.1-µm and smaller structures.

How much smaller can the transistor gates get? Researchers aren't totally sure, since the 0.1-µm features now being fabricated are already well below the size that was thought practical just a decade ago. Most researchers feel that another order of magnitude decrease might be possible some time after 2010, or as soon as they can figure out how to draw the features on the silicon and perform the material etching and deposition.

At the other end of the design spectrum, yet another challenge awaits designers. What types of products should be created using these ultra-dense technologies that will permit hundreds of millions to a billion transistors to reside on a single chip? Such chips could pack the equivalent of a half-dozen 64-bit processors, tens of megabytes of memory, and other logic—probably just barely enough power to handle Windows 20x0.

Let me have your opinions at *dbursky@penton.com*.

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Hypersonic Aircraft Could Revolutionize Air Travel

A hypersonic aircraft that could conceivably fly between any two points on the globe in less than two hours has been designed by Preston Carter, an aerospace engineer from Lawrence Livermore National Laboratory, Livermore, Calif. The aircraft design—dubbed HyperSoar—can support speeds of approximately 6700 mph (Mach 10), while carrying roughly twice the payload of subsonic aircraft of the same takeoff weight.

The key to the HyperSoar design is the skipping motion of its flight along the edge of the Earth's atmosphere. During operation, it would ascend to about 130,000 ft. then turn off its engines and coast back to the surface of the atmosphere. There, it would again fire its air-breathing engines and skip back into space. The craft would repeat this process until it reached its destination.

While many might question the plausibility for a passenger to withstand this swaying motion, the aircraft's angles of descent and ascent during the skips would only be 5 degrees. As such, passengers would feel 1.5 times the force of gravity at the bottom of each skip—like riding on a child's swing, though HyperSoar's motion would be 100 times slower. In space, the passenger would experience weightlessness.

Speed of travel is only one of the benefits offered by the HyperSoar design. Compared to previous hypersonic designs, the HyperSoar promises less heat buildup on the airframe of the aircraft—a challenge that has until now limited the development of hypersonic aircraft. In fact, the design not only addresses the primary issues in building hypersonic aircraft, but does so in a manner that creates a number of different uses for HyperSoar. Among them are for a passenger aircraft or freighter, and for space lift.

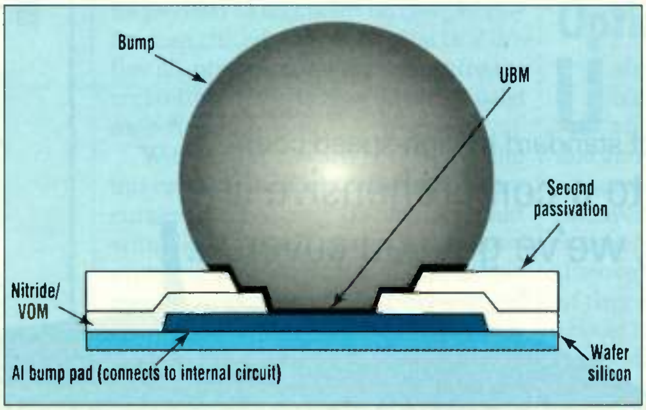
Researchers believe this develop-

(continued on page 26)

Wafer-Level Packaging Allows Die-Size, Dual CMOS Op Amp In Existing Assembly Processes

Taking advantage of recent advances in die packaging, National Semiconductor Corp., Santa Clara, Calif., has announced a die-size dual CMOS op amp that promises to turn the tables in favor of the portable electronics designer scrambling for board space. Using proprietary techniques, National joined a recent move to wafer-scale packaging that shrinks the final product to the size of the die itself. In this case, the package ends up with a footprint of 1.40 by 1.45 mm and a height of 0.9 mm.

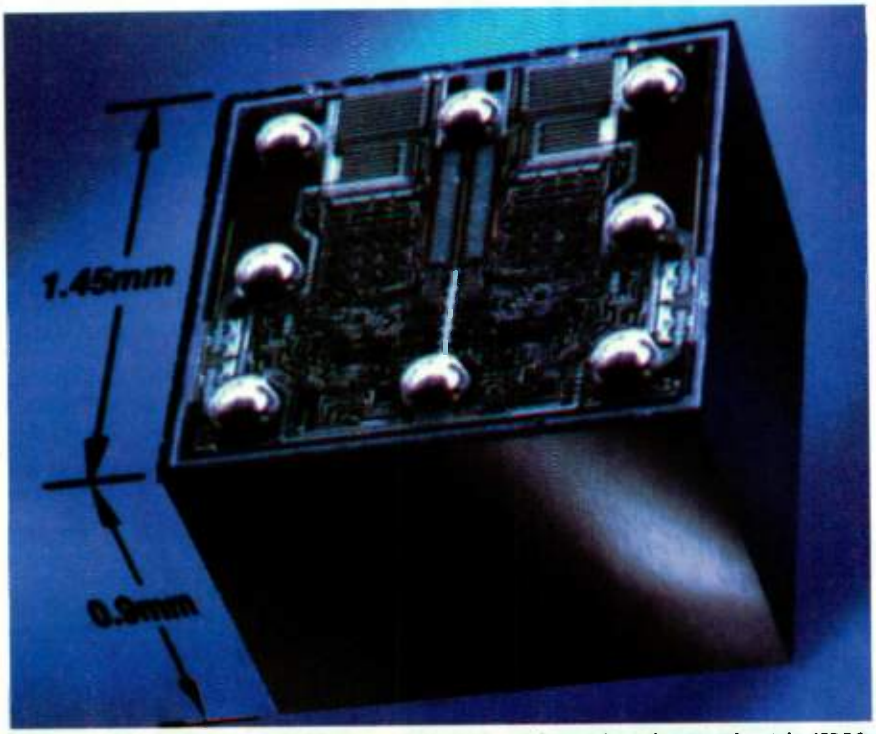
The IC, the LMC6035IBP, is a general-purpose op amp optimized for low-power applications. It uses the company's leadless, Micro-SMD (µSMD) package, which is applied entirely at the wafer level. Connections to the outside world are through eight standard, JEDEC-compatible (MO-195) eutectic-solder bump pads with a 0.5-mm pitch *(Fig. 1)*. The bump-pad design is such that it allows placement using existing passive-component assembly processes.



2. The solder bumps sit on a passivation layer that acts as a mechanical stress buffer. A three-layer under-bump metal (UBM) makes the connection between the bumps and the metal interconnection of the die through windows in the second passivation and nitride/VOM layers.

The bumps themselves sit on a proprietary passivation layer that serves as a mechanical stress buffer. This second passivation layer, an element of the package construction, lays on top of the wafer's regular passivation *(Fig. 2)*.

Reliable connection to the bumps—through windows in both the second passivation layer and nitride/VOM layer—to the metal interconnection of the die is achieved using a three-layer under-bump metal (UBM). The side of the package opposite the active geometry side is protected with a proprietary encapsulation. This is the side seen from the top view of the board, as the device is



1. The LMC6035IBP is a dual CMOS op amp in wafer-level chip-scale packaging. The eight JEDEC-compatible bump pads have a pitch of 0.5 mm, allowing the device to be placed using standard pick-and-place equipment.

mounted bump-side down. As such, it is laser marked for both identification and orientation purposes.

Reliability testing completed by National includes: 500 hrs. of operational life at 150°C (board mounted) and 2300 hrs. of temperature cycling from 0° to 100°C (board mounted), as well as a board-mounted drop test, three-point bend test, and random vibration test.

Key features of the LMC6035IBP include an input-supply range of 2.7 to 15 V and an input bias current of 20 fA at 25°C. The output-voltage swing is within 200 mV for a 2.7-V supply with a 600-Ω load, and 5 mV with a 100-kΩ load. The device can be shipped in standard polycarbonate conductive carrier tape with pressure-sensitive adhesive cover tape. National expects pricing to be no more than that of current devices.

Future development will include adding regulators, timers, sensors, and other devices to the Micro-SMD lineup. For more information, visit National's web site at www.national.com/design/.

Patrick Mannion

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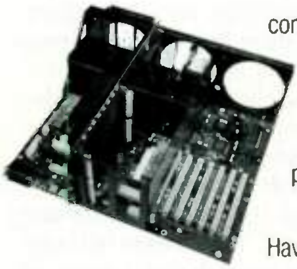

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ISN'T IT TIME WE DID TOO?

C-Language Superset Handles Complex, DSP-Specific Programming Tasks

Developing software for digital signal processors (DSPs) has always been a challenge. Unlike RISC processors, DSPs aren't friendly to high-level languages like C. Standard C does not directly support the fixed-point arithmetic operations used by DSP processors, leaving programmers with no option but to hand-craft most of their algorithms in assembler.

To address this problem, Associated Compiler Experts (ACE), Amsterdam, The Netherlands, has introduced DSP-specific extensions to the ISO/ANSI C programming language. ACE, a vendor of development technology for building optimizing compilers for DSPs, hopes the extensions will catch on as an industry standard and, eventually, become an official standard. Prominent DSP companies such as Atair Computing Inc., Troy, Mich.; Ericsson Radio Systems AB, Stockholm, Sweden; NEC Corp., Mountain View, Calif.; Philips Semiconductors, Eindhoven, The Netherlands; and Zilog, Campbell, Calif., are already developing C compiler products supporting the extensions.

Called DSP-C, the extensions overcome the inability of C to handle some DSP-specific concerns. These include fixed-point data types, divided memory spaces, dedicated register sets, and circular buffers. All these issues are fundamental to DSP performance.

Using DSP-C, programmers can enjoy the productivity and portability of writing in C, while at the same time generating code that closely approximates that achieved by hand-optimized assembly language programming. In consumer DSP applications, like digital mobile telephony, where increased functionality, lower cost, and shorter time-to-market are critical, the shorter development times and code reusability achieved by C-level programming are particularly attractive.

DSP-C adds a fixed-point data type to the language, able to be defined in a range of word sizes and saturation criteria. Using this information, fixed-point data is supported as easily as integer and floating-point data throughout the compiler, including the optimizers that lead to highly efficient DSP code.

By allowing the programmer to declare the memory space in which a specific data object must be placed, DSP-C also can support the multiple memory spaces of dual-Harvard-architecture DSP processors. That means optimizing compilers can take advantage of these devices' ability to read data from two separate memories in a single cycle to maximize execution speed. Simultaneous flow of coefficient and other data to the multiplier/accumulator of processors designed for FIR filtering, for example, is critical to their operation.

Many DSP algorithms, including finite-impulse response filters and fast-Fourier transforms, frequently use the same block of data over and over again, working from the start of the block to the end, and then looping back to the beginning. The best way to do this is to create a circular buffer. Unfortunately, such buffers are not easily defined in standard C programs. To address that situation, DSP-C allows the size and memory space of circular buffers to be defined so that they can be easily generated during program compilation.

Developed in collaboration with Philips Semiconductors, DSP-C is a superset of ISO/ANSI C that allows DSP programs to be written and compiled for virtually any target DSP processor. Because it maintains full compatibility with ISO/ANSI C, programmers can easily replace existing sections of assembly language code that are called from C programs with their DSP-C equivalent. The resulting program is much more maintainable and reusable.

To provide a generic, multivendor, multiarchitecture solution for implementing DSP-C, ACE already includes it as an integral part of the company's CoSy compiler development system. All of the optimizers and code generators in the DSP-C release of CoSy directly support the language extensions.

Additionally, ACE's code generators support architecture-specific attributes of target DSP processors, such as instruction-level parallelism, dedicated registers, and heterogeneous register sets. Because architectural descriptions in CoSy are easily defined and modified, developers can use it to experiment with new DSP architectures, and perform true hardware/software/application codesign.

The idea of extending C for DSP-specific use isn't new. Over the years, a number of tool and chip vendors have proposed similar strategies. All have failed to become true open standards across diverse DSP architectures. The reason has to do with the nature of the DSP market. While the broad embedded-system market includes an army of software tool vendors, the DSP niche contains very few. So, the burden has fallen on DSP chip vendors to make tools supporting their own processors. Naturally, the chip vendors aren't keen on making it easy for customers to port software over to a competing device.

However, as DSP technology moves into more commercial and high-volume applications, the time may be right for DSP-C. As code size in DSP applications gets larger, the desire for soup-to-nuts, high-level language use grows.

Rob E. H. Kurver, ACE managing director, says he's talking to standards bodies about making DSP-C an official standard. He's not optimistic about it happening quickly, though. Language standards often take four or five years to get approved. While official approval may be far off, it's realistic to expect DSP-C to catch on as an industry standard, if enough developers adopt it.

For more information, contact Marco Roodzant, vice president of marketing and sales, at Associated Compiler Experts, Van Eeghenstraat 100, 1071 GL Amsterdam, The Netherlands; +31 20 6646416; fax: +31 20 6750389; e-mail: marco@ace.nl; www.ace.nl.

Jeff Child

Broadcast PC Reference Design Explores New Applications Horizons

Handling MPEG and AC-3 Streams From Cable, Satellite, Or DVD, A Novel Multimedia Front End Brings New Capabilities to PCs.

Lee Goldberg

COVER FEATURE

The close of the 20th century is giving rise to many important questions, ranging from how to define and enforce electronic privacy to the ethics of patenting genetic material. The consumer electronics community, however, is considering far more weighty matters. A debate rages over whether computers will absorb the functions of TVs, or if TVs will acquire enough intelligence to do many of the things computers do. As we round the final turn towards 1999, the dialectic is hardly resolved. But, a new development by LSI Logic, Milpitas Calif., sheds light on this turgid topic. The unveiling of the "Broadcast PC," their new multimedia architecture, marks a novel and perhaps crucial point in the evolution of the multimedia computer.

LSI Logic's concept for the Broadcast PC was to develop a low-cost, universal platform which could serve as a front end for PCs to receive and process incoming audio and video signals from nearly any conceivable source. This would include analog and digital cable, VCRs, direct broadcast satellites (DBSs), and digital video disks (DVDs). Other interfaces, like the IEEE's1394 Firewire, could be used to exchange digital video with the new generation of digital VCRs and camcorders. While the first generation of Broadcast PC systems will be playback-oriented and have limited editing features, a mid-range PC could eventually be transformed into a full-featured video-editing studio.

For the concept to gain acceptance, it would have to be inexpensive and easy to integrate with current and future PC designs. Since ease of application is a critical factor, LSI Logic created an entire reference design that would permit manufacturers to produce their own PCI cards directly from the supplied parts lists, schematic, pc-board artwork, and driver software.

Driver software for the Broadcast PC front end has been carefully developed in conjunction with Intel and Microsoft to take advantage of the extensive multimedia capabilities they embedded in their PC 98 and PC 99 design guidelines. For example, both hardware and software work together to make best use of the Windows 98 DirectShow software (formerly known as ActiveMovie), which provides access to hardware acceleration of MPEG-1 playback. This is expected to be important for integrating high-quality video into things like games, multimedia Internet browsers, computer-based training, and video conferencing.

A Market-Driven Design

When starting the project, LSI Logic's marketeers and engineers agreed that if it could be done for the right price, adding Broadcast PC capability would be a very attractive option for PC makers. This is for several reasons. First of all, a ubiquitous multimedia front end that was inexpensive to embed in a "vanilla" PC could stimulate many new applications and help boost PC sales. Equally important, computer manufacturers could embed this added functionality into their products to slow the relentless price erosion that forces them to slash prices or add performance with each succeeding model.

Logically, a multistream, multimedia processor is not too difficult, since most entertainment mediums have settled on using the MPEG-2 protocol to move video between storage and display. In addition, Dolby AC-3 and linear pulse-

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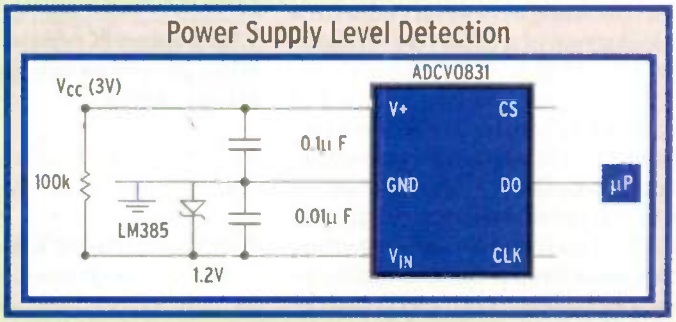

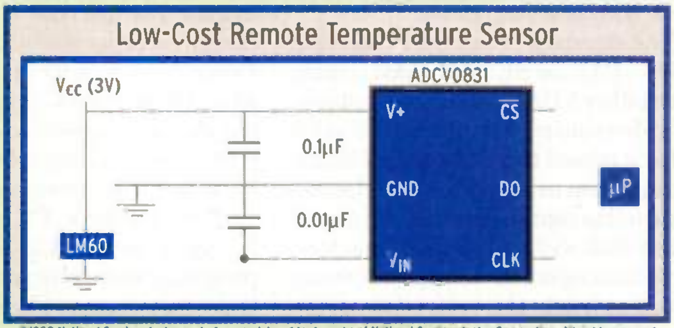

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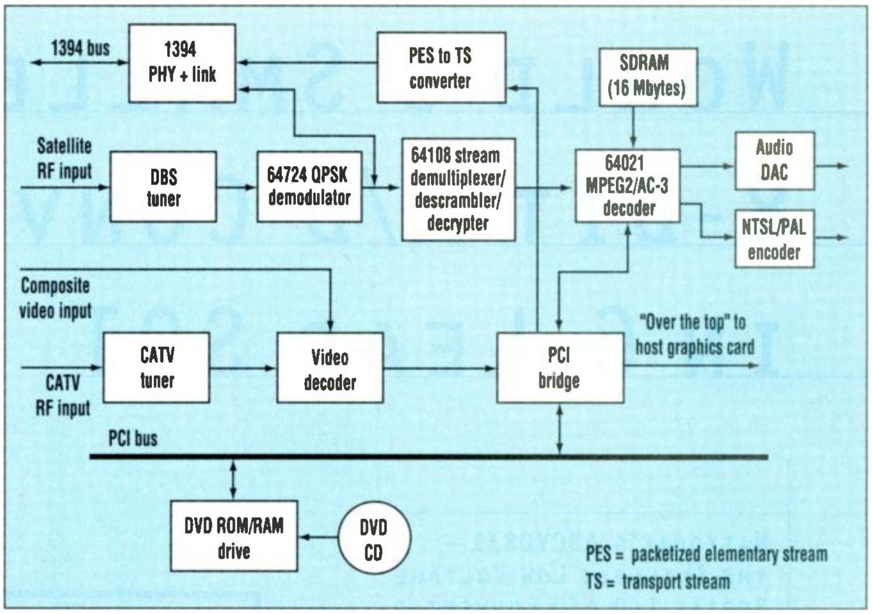
code-modulation (PCM) decoding were added to handle home theater and other audio requirements.

In reality, LSI Logic's designers had to thread across some rocky ground to add a multiple-source processing pipeline to the standard PC's innards. Aside from requiring two separate tuners for cable and DBS programming, demodulated signals from satellites contain a MPEG-2 transport stream. This stream must be demultiplexed to extract the audio and video channels of a particular program stream before being decoded into audio and video. Because security measures vary between different broadcast media, multiple encryption and authorization schemes must be handled by a single chip set.

It took months to weigh alternatives. Then, the designers emerged with a block diagram of a relatively straightforward marriage of a series of previously developed LSI Logic chips and other relatively basic components to a standard PCI bus *(Fig. 1)*. Besides providing a cost-effective, open solution for use in computer products, the Broadcast PC architecture's building-block nature lends itself a mix-and-match approach for building more specialized devices, such as set-top boxes.



1. The Broadcast PC reference design accepts inputs from DBS satellites, cable TVs, or DVD ROMs. Enhanced versions may have DVD RAM and exchange multimedia streams across a Firewire interface.

The standard broadcast PC accepts NTSC, PAL, or SECAM video coming from either a CATV tuner or a composite video source. For display, decoded video is passed to a PCI bridge chip for transmission to a graphics card. Incoming satellite signals pass through a quad phase-shift-keying (QPSK) demodulator to a transport stream demultiplexer, which extracts the desired program from the multichannel MPEG II stream. The transport chip also handles descrambling of the bit stream and can support various conditional-access schemes for decryption, if necessary.

From there, the transport stream is fed to a decoder. The video and audio channels are decoded and passed to the appropriate output channel. The video bit stream can be routed to the PC's monitor via the computer's graphics card, or for conversion into NTSC or PAL analog output signals. Decoded PCM or AC-3 audio signals also output here via an on-chip, two-channel audio DAC. Audio or video signals read from a DVD player are passed across the PCI bus to the MPEG II decoder for display. In this way, a single PCI card can funnel a variety of media into the computer for display or further processing.

But Wait, There's More!

High-quality sound is also a major factor in today's demanding multimedia market. For this reason, the LSI Logic design incorporates a fully functional Dolby AC-3 decoder in its design. This lets a Broadcast PC support the multichannel surround-sound effects that are encoded into many movies for use in home theater environments.

The Broadcast PC architecture's flexibility permits it to "assimilate" any promising new transport technologies which may emerge. Plans are already in the works for an enhanced multimedia card which can also exchange digital video via the IEEE 1394 Firewire interfaces beginning to appear in high-end video equipment *(Fig. 1, again)*.

Firewire's low-power, 200+ Mbit/s interface promises to be an ideal way to transport high-quality MPEG signals between a VCR or camera and a computer or video workstation. To turn the Broadcast PC into a Firewire-capable "Convergence PC," add a 1394 transceiver and a converter turns its packet elementary stream (PES) into a transport stream (TS). These can be easily digested by the MPEG II decoder.

Another planned enhancement of the Broadcast PC would add an interface to support a rewritable DVD unit, known as a "DVD RAM." With a DVD RAM or two on board, a computer would have enough storage to do large editing tasks. MPEG spends most of its time transmitting the changes of a video image from frame to frame. But, complete pictures are usually only transmitted when the scene changes. Because of this, a Broadcast PC's editing capabilities will initially be limited to splicing scenes together. In time, software should become available that uses MPEG's scene-change data to interpolate images between full scenes, permitting frame-by-frame editing.

A Chip's Eye View

LSI Logic's first version of the reference design uses a series of currently available chips to fill some functional blocks in the architecture diagram. This stable includes the L6724 QPSK demodulator/forward error correction (FEC) processor, the L64108 transport chip, and the L64021 audio/video decoder. The remaining blocks currently include hybrid modules, FPGAs, or commercial silicon from other vendors.

At the center of the Broadcast PC is the L64021 decoder. It takes MPEG-2 PES or ES program streams and produces a pair of decoded digital bit streams to be fed to an audio DAC and an NTSC or PAL encoder *(Fig. 2)*. Its video decoder normally produces images at up to 740 by 480 pixels at 30 frames/s

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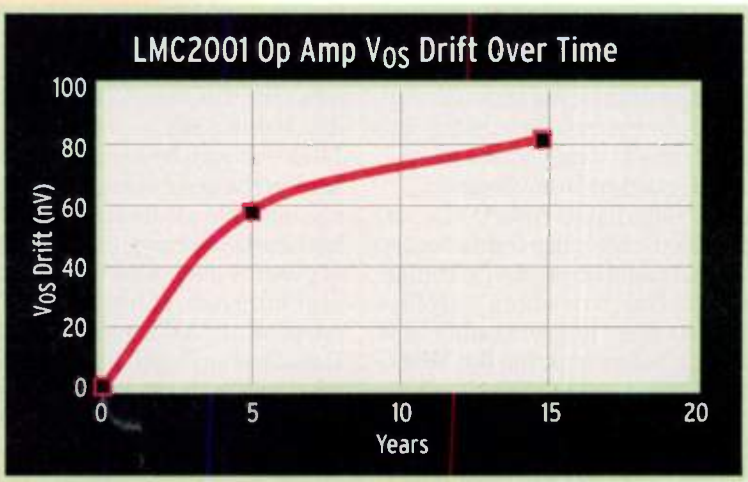

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in the NTSC mode, or 720 by 576 pixels at 25 frames/s for the PAL mode.

Images below full resolution are interpolated by the L60421's on-chip filters to expand them to full size. Besides allowing easy translation between video formats of different resolutions, the programmable on-chip filters can perform pan and scan functions on MPEG images with 1/8-pixel accuracy. Support for other features, such as letterbox format, on-screen display, and on-screen graphics, also is available with no external circuitry. The 64021's PES decoding circuitry can parse critical parameters for the presentation time stamp (PTS) and decoding time stamp (DTS) information needed for synchronization.

The chips' audio-decoder block can produce a pair of down-mixed, digitized, stereo audio channels from either AC-3 or PCM signals. Alternatively, an AC-3 audio stream can be fed through a bypass path for external processing into the full home-theater, multichannel, surround-sound audio environment.

Audio/video inputs from DVDs and descrambled cable video from a set-top box come straight across the PCI bridge interface. But, raw-signal satellite broadcasts must get some additional processing before entering the MPEG decoder *(Fig. 2, again)*. The Broadcast PC uses the 64724 QPSK demodulator/FEC decoder to take the I/Q outputs of a standard satellite tuner and turn it into an MPEG transport stream. It has a pair of high-speed ADCs that digitize the incoming I/Q waveforms in preparation for the QPSK demodulation performed in the digital domain. The self-tuning demodulator chip also performs the Viterbi decoding and Reed-Solomon forward error correction employed by all digital satellite transmissions to keep bit-error rates as low as possible.

From the demodulator, the satellite video signal emerges as a scrambled MPEG transport stream. Scrambling guards against program theft by unauthorized users. Several different schemes are commonly used, so a merchant-class, general-purpose device must be programmable to accommodate them all. In this case, the L64108 transport chip provides the descrambling, as well as most of the other function required for a DBS set-top box.

The transport chip has its own embedded 32-bit mini-RISC-processor core *(Fig. 3)*. Combined with an on-chip data bus and cache system, it gives the L64108 enough brains and speed to ride herd on the descrambling process, manage multiple media streams, and still have enough left over to support a series of general-purpose peripherals and a user interface. It integrates a DVB-compliant, iCAM 2.0-compliant, News-Data-System (NDS) conditional-access descrambler. It can be programmed to handle most commonly used scrambling schemes (DSS, DVB, and Japan's Multi-2), and to handle proprietary functions required in specialized applications.

Thanks to the large array of I/O on the chip, designers will be able to make glueless interfaces to nearly any kind of user or system function. The IEEE 1284 and three RS-232 UART ports make intrabox communication easy, while the I^2C-style master/slave bus facilitates intrachip exchanges of control signals. A pair of SmartCard interfaces promise to simplify interfacing personality modules, configuration upgrades, or personalized billing arrangements into their products. Finally, a teletext port is available for displaying alphanumeric information over the video images.

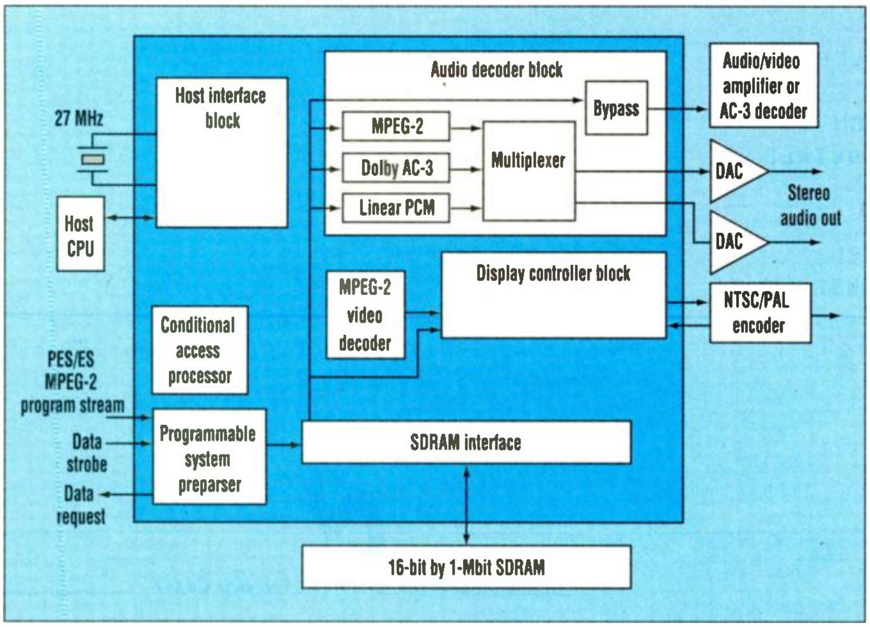
The other task performed by the L64108 is demultiplexing of the incoming MPEG stream. It can take a raw broadcast signal and demultiplex it into as many as 32 packet IDs, which might include audio, video, or general-purpose data services. Other non-DBS signals, such as video over 1394 Firewire, can use this demultiplexing function to get their data ready for MPEG decoding and processing *(Fig. 1, again)*.

Got Apps?

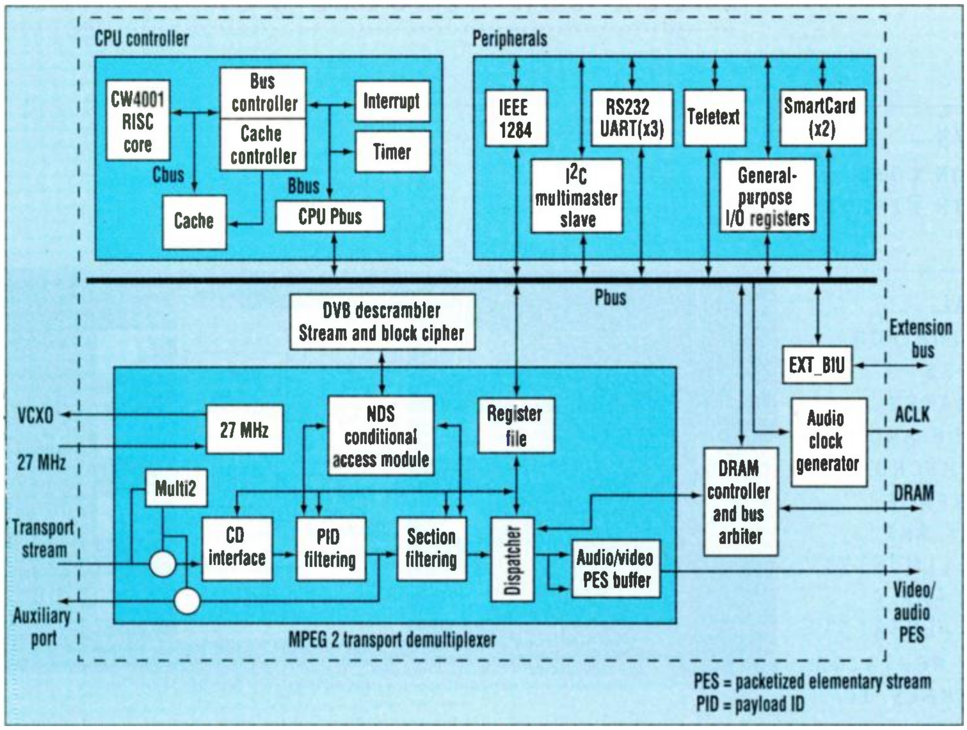
So, now that you've got all of this technology under the hood of your computer, what the heck is it good for? LSI Logic believes that Broadcast PC will first find applications within industry and government, distributing information and training material. The standard hardware and software architecture will make it easy to create highly interactive programming material for the dissemination of policy and procedure changes, or for use in providing personnel with detailed technical information. In the consumer realm, a computer with MPEG and AC-3 capability opens up the possibility of expanding LAN and Internet communications beyond static e-mail, fuzzy audio, and grainy video clips.

Multimedia capability may also help the PC displace the TV in markets like offices, classrooms, and college dormitories. Plug-in broadcast tuners are already bringing radio and TV to the desktops of busy executives and the cramped quarters of dorm rooms—a trend likely to accelerate with the advent of a "cable-ready" computer.

While the prototype version of the Broadcast PC is designed to be a multimedia enhancement device for PCI-bus-based PCs, it can easily adapt to become the key element in a wide range of other jobs within the embedded-systems market. The modular, software-



2. The L64021 audio/video decoder chip processes both MPEG-2 video and AC-3 audio streams.



3. The L64108 transport demultiplexer extracts video and audio streams out of a multichannel MPEG transport stream. The chip also performs descrambling, decryption, and other conditional-access functions.

programmable reference design can easily adjust to handle more dedicated applications. By removing unnecessary components and adding a custom interface and additional software, designers can rapidly create a wide range of multimedia products. These would include items such as smart set-top boxes, information kiosks, and satellite-based information-distribution systems.

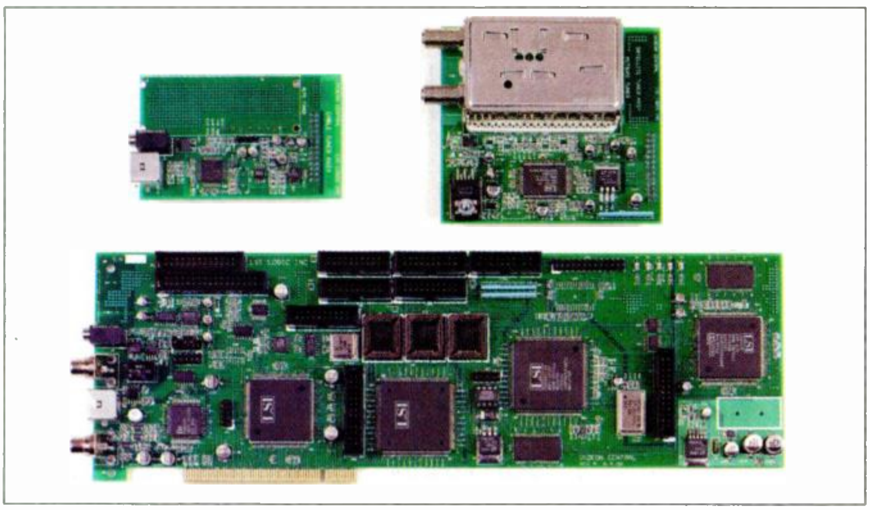
LSI Logic's other immediate goal is to support the vision of the Broadcast PC that's been brewing at Microsoft Corp., Redmond, Wash., for the past couple of years. Microsoft has set its sights on becoming the gatekeeper for the interactive content spewing from the Internet, satellites, and other broadcast media.

Using the Broadcast PC hardware model and Windows 98 DirectShow software, Microsoft hopes to provide a framework that allows viewers to combine video and Internet information from any combination of sources. Microsoft wants to get content providers to produce new types of programming based around their technologies by declaring them a de facto standard.

When furnished with suitable content, a Broadcast PC could use datastreams from cable TV, cable modems, satellite links, and DVDs to let viewers retrieve more information about shows they watched. Users also could purchase the stuff they saw on the program using online transactions. One day, viewers could even participate in chat sessions to discuss the program they're watching, or visit web sites with program-related information. Imagine a soap opera which uses instant polling from online viewers to determine the plot twists of the next day's installment.

Besides a complete reference design, LSI Logic is offering a hardware-evaluation kit and development software. A PCI-based main board houses the PCI connection to a standard PC, transport demultiplex and conditional-access functions, and the MPEG decoding circuitry *(Fig. 4)*. The evaluation board also comes with two mezzanine cards for adding a satellite and a cable-capable analog tuner. A 1394 mezzanine card is expected to be available next year.

The hardware side of the reference design includes schematics, component list, Gerber plots for pc-board artwork, and a full set of technical manuals and data sheets. Software and firmware included in the Broadcast PC's development kit includes a complete listing of source code for the L64108's mini-RISC controller. Included are a PSOS-based RTOS, user-interface drivers, code debug tools, and JTAG support. Drivers included allow access to free-to-air programming from DVD and cable sources. Software to support conditional-access satellite programming is available under separate license.



4. The Broadcast PC hardware-development kit includes a PCI-bus-based MPEG/AC-3 decoder card and a pair of mezzanine boards for interfacing to cable or satellite sources.

Price And Availability

The LSI Broadcast PC reference design kit will be available during the first half of 1999 at a price of $7500.

For more information, contact LSI Logic, attn: PC Multimedia Marketing Group, 1551 McCarthy Blvd., Milpitas, CA 95035; (800) 574-4286, (408) 433-8000; www.lsilogic.com.

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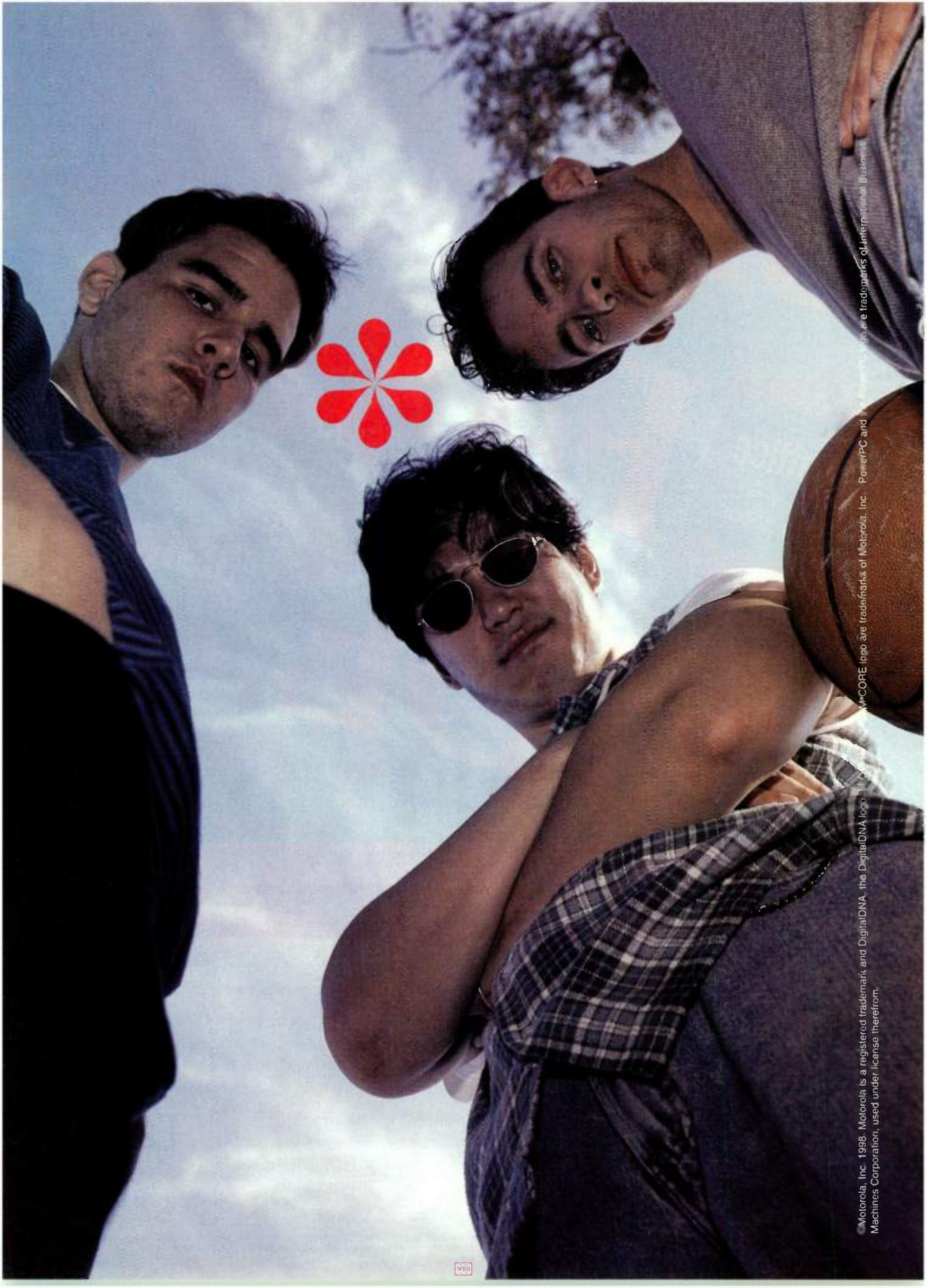

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CONFERENCE PREVIEW

Fall Comdex Conference Reflects Expanding Definition Of Computing

Go High-Tech With Classes And Tutorials Covering Platforms, Consumer Issues, Software, Java, And Internet Topics.

Jeff Child

Fall Comdex has become, hands down, the key meeting place of the computer industry. Today, the term "computing" encompasses a wide range of areas and sub-areas including PCs, notebooks, handhelds, networks, intranets, the Internet, and the web. This year's conference reflects that, with a new twist. There's a special "Technical" stamp next to each session relevant to developers and engineers. These sessions are led by seasoned programmers and implementers who will deliver the theory, as well as the practice, of the designated topics.

Running this year from November 16th through the 20th in Las Vegas, Nevada, at the expanded Las Vegas Convention Center, the Sands Exposition and Conference Center, and the Las Vegas Hilton, Comdex conference topics include over 100 sessions. They cover a wide range, including Java System Programming, Object-Oriented Development, the Connected Home of the Future, Understanding TCP/IP, Streaming Web Video, Developing Apps for Windows CE, Digital TV and Internet TV, and much more.

A Word From Bill

This year's show features no less than eight keynote speeches. Kicking off the show the Sunday before Comdex week is a keynote by Bill Gates, arguably the most influential person in computing. In his speech, entitled, "Today and Beyond: Innovation, Integration and Simplification," the Microsoft, Redmond, Wash., CEO explores what the future holds for computer technology. He'll talk about striving toward simplicity, lower cost and more manageable systems, and how the Internet will become an even stronger medium of communications to bring the world closer together.

In another keynote, Craig Barrett, the new President and CEO of Intel Corp., Santa Clara, Calif., will address the Comdex audience for the first time. He'll outline his vision for Intel and the computer industry, and the core technologies and applications that will shape the use of computers beyond the end of the decade. The remaining six keynotes are provided by a variety of industry heavyweights across a mix of disciplines.

Although Comdex naturally caters to a wide range of attendees, its conference program includes a significant percentage of highly technical sessions that are worth the attention of engineers. The classes marked with skill level 300 are the most technical. Because many topics such as Java and Windows CE are new to many engineers, even some of the more basic sessions may be of interest.

Start With Platforms

As PC microprocessors race to ever faster speeds, the PC is no longer considered a "trade-off" architecture. PC platforms now rival workstations in performance, while maintaining the leading edge in cost effectiveness. Two tutorials take an in-depth look at the latest and greatest PC microprocessor architectures. In "Understanding Merced and IA-64," attendees get an overview of Intel's new IA-64 architecture. Called the biggest shift in microprocessors since the introduction of RISC in the 1980s, Merced, the first IA-64 processor, will begin shipping in 1999. IA-64 introduces a new style of instruction-set architecture that promises a significant performance boost. This tutorial explores what's different about IA-64 and how it will affect the computing landscape.

Taking a more comparative view is a tutorial entitled, "Microprocessors for PCs: Intel Versus Its Competitors." Produced in cooperation with *Microprocessor Report*, this informative session compares chips from Intel; AMD, Sunnyvale, Calif.; Cyrix, Richardson, Texas; and IDT, Santa Clara, Calif. It includes technology road maps, price projections, company prospects, and risks—everything you need to take advantage of the processor "buyer's market."

Beyond those two tutorials, attendees can find a variety of other platform discussions in the "Desktop and Platforms" track. This track takes a deep look at next generation platforms and explores their implications. The session, "Thin Clients: Platform Strategies," offers an in-depth discussion of prevailing thin-client strategies, such as the Windows terminal approach versus the network computing (NC) approach.

Along more conventional lines, "NT Workstation 5.0: Migration Strategies" focuses on preparing for a Windows NT 5.0 migration. Meanwhile, in "Linux: The Windows Alternative?," speakers debate whether Linux represents a realistically deployable solution in business environments, or whether its future is constrained to an enthusiastic cult with no fear of the command line.

Playing With Software Fire

Software is like the gasoline of a computer-based system. Like gasoline in a car, computers can't run without software. And, if software isn't handled and formulated properly, it can cause damage like exploding gasoline. Helping attendees wrestle with software issues are the sessions in the "Developers Toolbox" track. These in-

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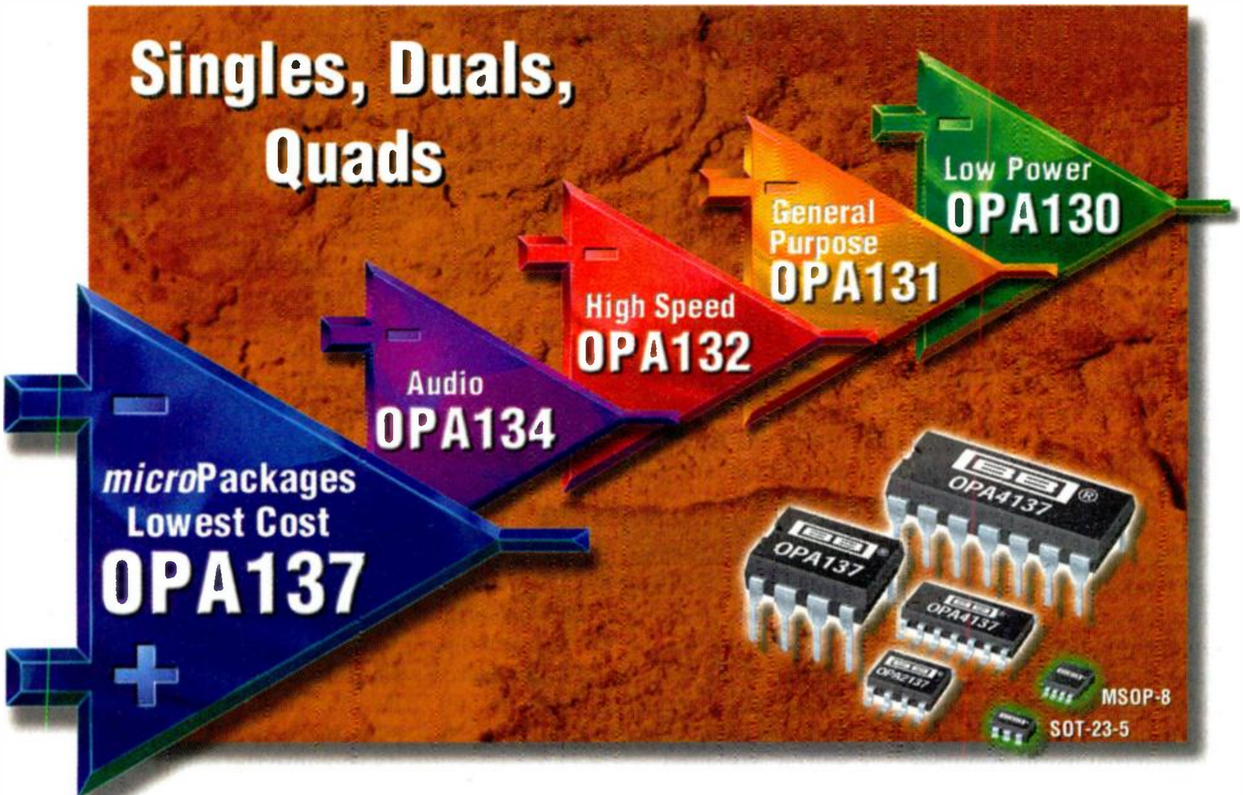

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depth technical sessions help attendees update their skill set and walk away with some new, solid development skills—spanning the gamut from design to implementation.

Developers of various modeling languages have worked together to define a new standard for modeling languages, the Uniform Modeling Language (UML). The session, "An Introduction to UML for Object-Oriented Development," starts with a brief synopsis of the history of UML, followed by an introduction to the concepts, notation, and processes of using UML. For those who want to jump in and use UML, "Object-Oriented Development Using Visual Basic" focuses on using Visual Basic to define, create, and use objects. It will cover how to design a three-tier application and implement this technology in your application.

Cover a more fundamental software skill in "Mastering Design Patterns." Software developers are discovering the power of design patterns, which organize and present a catalog of proven design idioms for structuring, creating, and manipulating objects. This session teaches you to effectively recognize and apply design patterns using real-world examples.

Meanwhile, component architecture is reshaping the software development process. The Component Object Model (COM) can accommodate language-independent components, distributed computing using DCOM, and run-time customization. "Microsoft COM: Past, Present, and Future" gives an overview of the history of COM, looks at how it's used today, and shows how new technologies like COM+ will affect the future of software development.

Another session, "ActiveX Controls: An Intelligent Choice for Distributed Computing," looks at an offshoot of COM called ActiveX. ActiveX controls can be specifically designed to facilitate their distribution across networks and the Internet and to allow integration of components into web pages. This session looks at what ActiveX controls are, and how they are used.

On the software language side, attend the session, "Real-World C++," to learn the complexities of C++. Used without discipline, C++ can lead to code that's hard to maintain, inextensible, inefficient, and just plain wrong. This session introduces guidelines for developing clean, fast, correct C++—the kind you need when developing large, complex, real-world systems.

Java University A La Sun

To help attendees join the Java revolution, Comdex includes a special set of "Java University" sessions. Training is designed and presented by expert Java technology engineers from Sun Microsystems, Palo Alto, Calif., and other industry leaders using Java technology. The full-day seminar, "EmbeddedJava Technology Applications," provides detailed descriptions of the products, technologies, and development tools based upon the Java platform.

For the hardware side of the Java coin, check out "picoJava Processor Architecture for Embedded Applications." This technical seminar begins with an in-depth technical introduction to the architecture of picoJava processors, including a detailed architecture overview, and a technical discussion of picoJava 1 and 2 and microJava 701. All available software tools and operating systems available also will be presented.

At a broader level, "Java Technology Applied" explores Java Card, EmbeddedJava, PersonalJava, JINI, and picoJava architecture technologies and development tools. Technical presentations by Sun's licensees and engineers cover telecom, telephony, television, and automotive.

For developers with Java experience already under their belts, there's a number of advanced Java sessions. "Java System Programming on Windows NT" explores the issues surrounding purity and impurity via direct system calls. It also focuses on using various "bridge" technologies to gain access to system resources like Component Object Model (COM) and ODBC-based databases. Coverage of complementary and competing tools from Sun Microsystems and Microsoft Corp. arm the programmer with the information necessary to complete the picture of the Java programming language paradigm on a Windows NT-based system.

For the advanced Java-head, the session, "Java 3D API: Developing 3D Applications with Java Technologies," introduces the Java 3D application programming interface (API). API is used to write 3D graphics applications and applets. Java 3D extends the Java technology philosophy, "Write Once, Run Anywhere," into a third dimension, allowing for the construction and viewing of large virtual worlds.

Finally, for the very advanced, "JINI Technology: Distributed Java Technology Programming" provides experienced developers using Java technology with a detailed and comprehensive understanding of how JINI combines groups of devices and software components into a single, dynamic distributed system. This system includes spontaneous networking, JINI Federations, JINI System Components, Remote Method Invocation (RMI), JavaSpaces technology, and Lookup and Discovery. This technical lecture reviews the major components of distributed computing using JINI technology.

Hook That Consumer

While business users still dominate the computing market, the industry has launched a full-court press on consumers. As digital technology makes its way into the hands of the masses, exciting changes happen in the business and home markets. Comdex looks at many segments of consumer computing. Operating systems issues are explored in "Windows CE versus Personal Java: The Battle for Control of the Digital Consumer." A panel of experts views the emerging digital consumer landscape, discusses the role these operating systems will play, details the pros and cons of each, and outlines how this market will develop.

The next generation of handheld devices is destined to change the way we work in any environment. The session, "Palm-Size and Hand-Held Devices: The Next Generation of Truly Mobile Devices," explores the exciting world of mobile device technology as it now extends to smaller form factors. Panelists discuss the newest technologies in this area, including the Windows CE devices that compete with 3Com's PalmPilot and the PC Companion platform that's set to compete with mini and low-end notebooks.

Two years ago, it looked like digital video disk (DVD) was the hottest

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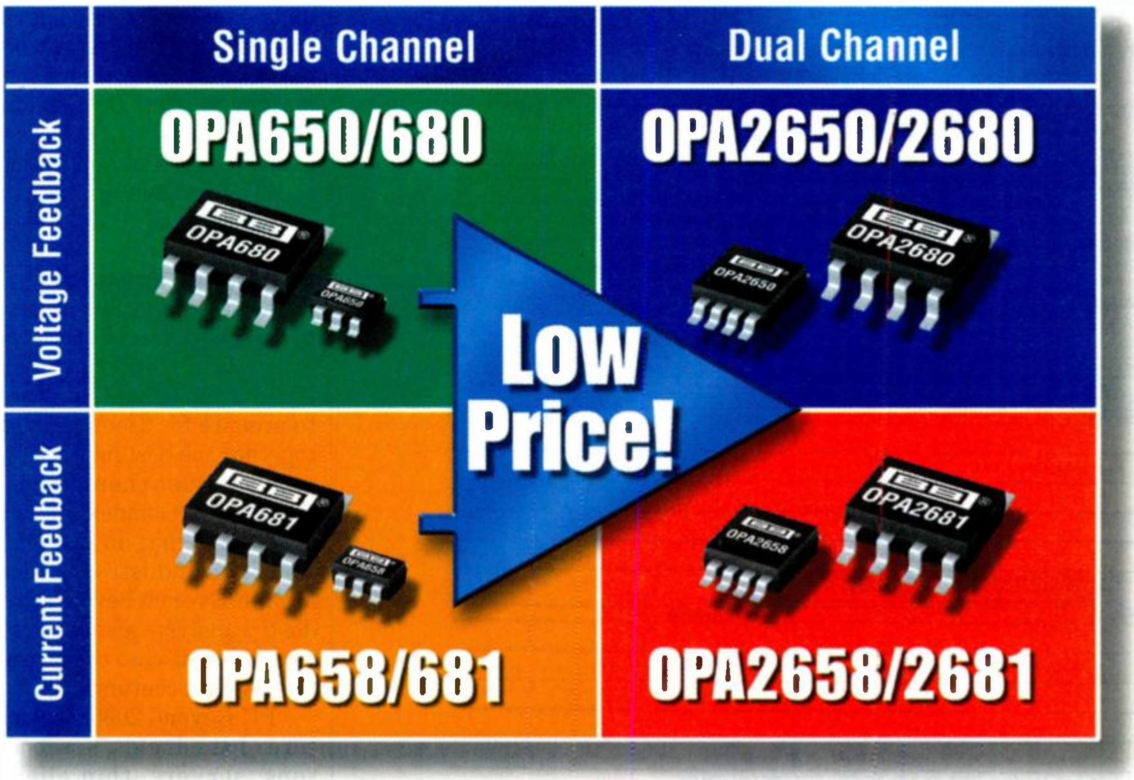

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technology in the consumer market. As it turns out, it's been slow to take off and hasn't come close to realizing its potential. Attendees can find out why in "DVD: Is It Finally Poised to Take Off?" This session provides an update on DVD technology and looks at the DVD-ROM. A key focus will be the standards battle for perhaps the most important DVD technology of all—DVD read/write. The session also examines current applications or uses of DVD in both business and consumer markets.

United We Speculate

In the computer industry, the future seems to arrive faster and faster every year. Until someone invents a time machine, however, the best way to prepare for the future is to gather together the best forward-looking experts and let them debate among themselves. Comdex offers a number of sessions that do just that. In "Vision 2001: Industry Luminaries See Mobile Everywhere," a panel of industry analysts and editors in mobile computing discuss their vision for the twenty-first century.

"PC Beyond 2000" looks at the future of handhelds, notebooks, desktops, servers, thin clients, thick clients, and an ever widening variety of configurations and form factors. Discussion includes the ideas of "neo-PCs" with embedded computer functionality but in the form factors of other devices, television-connected PCs, and the changing nature of personal computing of the future.

Computers now need to serve a broader range of users than ever before—essentially everyone, everywhere. Under those circumstances, a single user interface, no matter how cleverly designed or executed, isn't going to make everyone happy. New approaches to interface design now make user-interface schemes that assist both the novice and the expert possible. The session, "Interfacing the User," checks out how user interfaces have changed and how the future will permit us to use technology readily and without barriers.

For more information about Comdex/Fall '98, visit COMDEX online at www.comdex.com or contact Amy Groden at (781) 433-1756; e-mail: amy_groden@zd.com.

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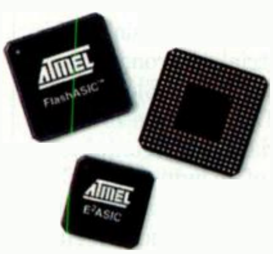

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CONFERENCE PREVIEW

Electronica '98 Flaunts Tiny ICs That Host Incredible Shrinking Systems

Need Some New "Components" For Your Designs? How About A Single-Chip Computer, Or A Digital Video Camera On An IC?

Alfred Vollmer

The last time it was held in 1996, Electronica was by far the biggest components show in the world. This year it'll be even bigger—and, once again, the biggest. This year also is the first time Electronica 1998, which takes place from November 10 to 13 in Munich, Germany, will be held at the brand new Munich fairgrounds opened earlier this year. This move allows a significant increase in the number of exhibitors— from 2800+ to more than 3400. As always, exhibitors from more than 50 countries will display their latest and greatest offerings.

In contrast to the previous show, Electronica '98 will have a new structure. It will be divided into seven product sectors. Product sector 1 comprises the entire range of semiconductor products—from memories to microcontrollers and DSPs to ASICs, as well as discrete semiconductors like transistors, diodes, MOSFETs, etc.

Passive components like capacitors, resistors, and inductors will be displayed in sector 2. This sector also includes piezoceramic components, surface-acoustic-wave (SAW) filters, and RF and microwave subsystems.

Totally new at Electronica '98 is product sector 3, where sensors and microsystems will be presented. This includes any kind of sensor offering an electrical output signal, as well as sensor modules. Sector 3 will most likely attract a lot of medium-sized European companies, which are traditionally strong in this area.

Product sector 4 comprises electromechanical components and connectors including pc boards, switches, relays, cables, and network-technology components. Manufacturers of displays show their products in sector 5.

System components like image/pattern recognition, printers, CPU peripheral assemblies, hybrid modules, multichip modules, power supplies, and servo technology will star in product sector 6. This sector also features packaging technology, thermal management, and EMC/ESD solutions.

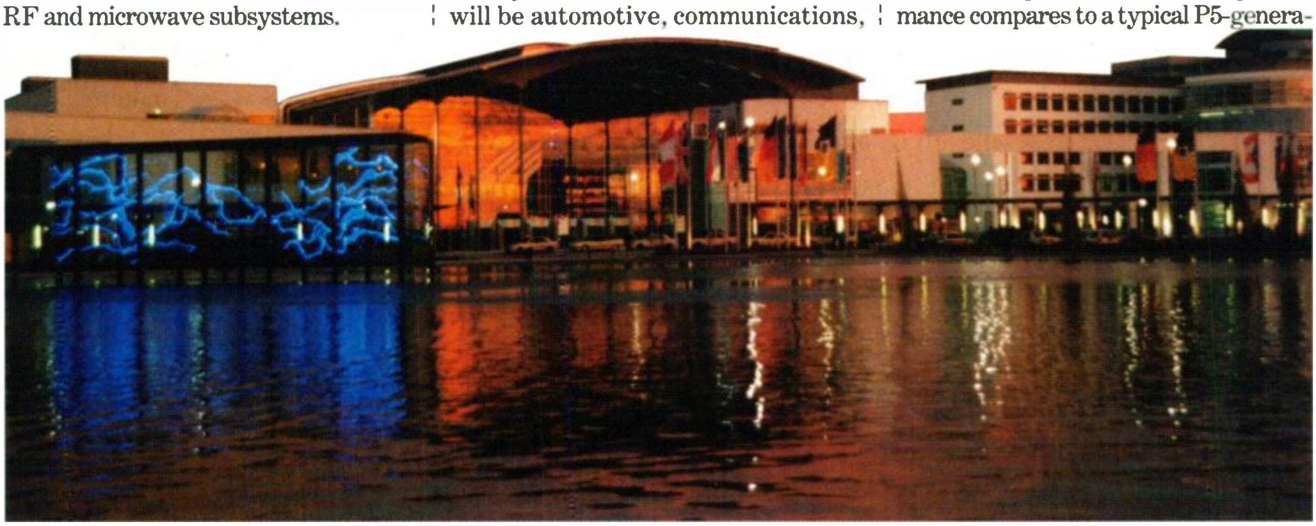
The last sector is on electronic design automation (EDA), test and measurement (including laboratory/test equipment), CAD/CAE tools, and design and development systems.

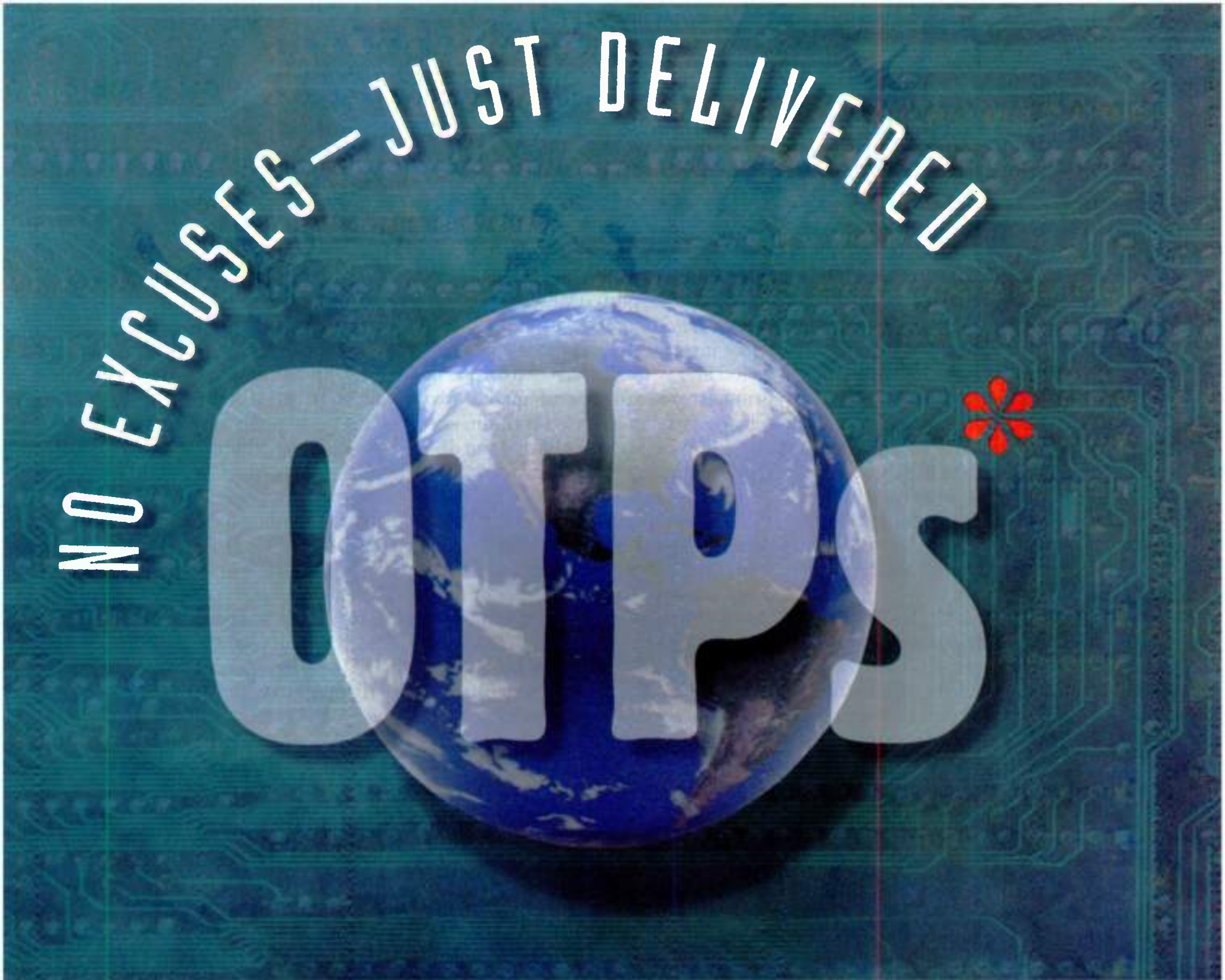
Major focus areas of most exhibitors will be automotive, communications, and multimedia applications. Consumer and industrial applications, however, also will be addressed. A trend which mainly started at Electronica 1996 will continue. The days of neatly arranged components in glass displays are over, because today's booths show complete solutions. For example, STMicroelectronics (ST), Saint Genis, France (Internet: *www.st.com)*, only wants to provide a forum where the semiconductor manufacturer is able to meet with customers.

Single-Chip Industrial PC

Nevertheless, one major discussion topic will be ST's brand new single-chip ST PC for industrial environments, to be officially presented at Electronica. Except for the DRAMs, the so-called "ST PC Industrial" really contains all the components of an industrial PC including the x86 processor core, a graphics accelerator, and bus and interface controllers. The chip is manufactured using a low-voltage, 5-layer metal, salicided 0.35-µm CMOS process, and is then integrated in a BGA 388 package.

According to ST, the device's performance compares to a typical P5-genera-





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68HC705J1A	1.2K	64	20	M68ICS05J	KITMMEVS05KJ	KITMMDS05KJ
68HC705P6A	4.6K	176	28	M68ICS05P	KITMMEVS05P6A	KITMMDS05P6A
68HC705C8A	8K	304	40,44	M68ICS05C	KITMMEVS05C	KITMMDS05C
68HC705C9A	16K	352	40,44	M68ICS05C	KITMMEVS05C	KITMMDS05C
68HC705B16	15K	352	52,64	M68ICS05B	KITMMEVS05B	KITMMDS05B
68HC705L16	16K	512	80	KITPGMR05L16	KITMMEVS05L16	KITMMDS05L16

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tion system. With its internal 32-bit x86 processor, it's fully PC compatible and will run DOS, Windows, OS/2, and Oracle n/c software.

Based on an entirely static DX-1 processor running at clock frequencies of 66, 75, or 80 MHz, the ST PC Industrial offers 8 kbytes of L1 cache, a floating-point unit, and a DRAM controller working with up to 128 Mbytes of system memory in four banks (with a minimum size of 2 Mbytes). It supports 4-, 8-, 16-, and 32-Mbyte, single-sided and double-sided DRAM SIMMs (Fast Page Mode and EDO DRAMs). Memory speeds of of 60, 70, 80 and 100 ns are supported. Programmable DRAM parameters include CAS pulse width, CAS precharge time, and RAS-to-CAS delay.

A tightly coupled, Unified Memory Architecture (UMA) is employed, so the same memory array is used for the CPU main memory and graphics frame buffer. This approach results in smaller system-memory requirements and higher memory bandwidth. Its 64-bit Windows graphics accelerator provides hardware acceleration for text (generalized bitmap expansion), bitblts, transparent bits, and fills. It also contains a linear frame buffer, which may be up to 4 Mbytes deep.

The accelerator supports graphics hardware cursors of up to 64 by 64 bits, as well as 8-, 16-, 24-, and 32-bit pixels. It's also completely backwards compatible with VGA and SVGA standards. Drivers for Windows and other operating systems are available. In addition, a CRT controller with an integrated 135-MHz RAMDAC is located on the single-chip PC. The controller can drive a 1280-by-1024 display at 75 Hz, in interlaced or noninterlaced modes.

Its integrated TFT interface works with panel sizes up to 1024 by 1024 pixels and supports VGA, as well as SVGA, active-matrix TFT flat panels with 9-, 12-, or 18-bit interfaces (1 pixel per clock). XGA and SXGA active-matrix TFT flat panels with a 2-by-9-bit interface are supported with 2 pixels per clock cycle. Image positioning, blank space insertion in text mode, and horizontal and vertical image expansion in graphic mode are programmable. Two fully programmable pulse-width-modulated (PWM) signals control the display's brightness and contrast.

The chip contains controllers for a PC/AT+-compatible keyboard, a PS/2-compatible mouse, and serial and parallel ports. Its local-bus interface works in either asynchronous or synchronous mode with a 66/80 MHz low-latency bus (22-bit address, 16-bit data). This local bus lets the system boot up from flash memory to cater to real-time applications. The monolithically integrated PCI controller fully complies with the PCI version 2.1 specification and eliminates the need for a separate PCI bridge.

Using ST PC Industrial's integrated PCI arbitration interface, up to three bus masters can be connected directly. If an external PAL is added, more than three are possible. The new device also handles translation of PCI cycles to the ISA bus, ISA master-initiated cycles to the PCIbus, and burst read/write from a PCI master. The PCI clock runs at either 33 or 50% of the CPU clock speed.

The built-in PC Card/CardBus interface supports one PCMCIA 2.0/JEIDA 4.1 68-pin standard PC Card socket, as well as the following standards: PCMCIA/ATA, I/O PC Card with pulse-mode interrupts, and the video part of Zoom Video. This PCMCIA 2.0 controller makes the device suitable for applications requiring high data bandwidths, including 100 Mbit/s Fast Ethernet, fast SCSI peripherals, and flash storage cards. The ST PC Industrial also offers an ISA master/slave interface. It generates the ISA clock from either a 14.318 MHz oscillator clock, or from the system clock, and supports programmable wait states for ISA cycles.

Its 15540-compatible serial interface offers a programmable word length, stop bit and parity, a 16-bit programmable baud-rate generator, and an interrupt generator. An 8-bit scratch register, two 16-bit FIFOs, and two DMA handshake lines are also integrated. The universal parallel port supports all protocols of the IEEE 1284 standard. And, it's equipped with a 16-byte ECP FIFO buffer.

To operate with peripheral devices, the ST PC Industrial works with two 8237/AT compatible 7-channel DMA controllers. The device operates in a temperature range between –40°C and +85°C, at a voltage of 3.3 V.

Its power management allows four separate power saving modes: on, doze, standby, and suspend. Power down puts the device into suspend mode, where the processor finishes executing the current instruction, any pending decoded instructions, and associated bus cycles. During suspend mode, internal clocks stop. After removing power down, the processor resumes instruction fetching and begins executing the instruction stream at the stop point. Due to the static nature of the core, no internal data are lost.

The ST PC Industrial was designed utilizing reusable modular-design tech-

Video Sensors And Smaller Feature Sizes

A 2-µm process just allows the integration of a sensor (720 by 576 pixels) on a single chip. But, if a 0.6-µm technology is used, there will still be space available on the chip for an analog-to-digital converter and some digital logic. At 0.25 or 0.18 µm, the sensor part and the digital part both decrease in size. This means that more logic may be integrated for a given chip size, increasing cost effectiveness.

Basically, this is well known. However, the maximum resolution of cheap optics results in an area of about 5 by 5 µm, where the light intensity has a constant value. This means that the optical resolution limits the minimum sensor size. At a sensor pixel size of 5 by 5 µm, the photo diode requires about 40% (10 μm^2) of this area (25 μm^2), while 60% (15 μm^2) of this area can be used for other purposes. Using 0.6-µm technology lets two transistors integrate on the remaining 15 μm^2. But, with a 0.1-µm CMOS process, 72 transistors can be integrated on the same 15-µm area. Siemens is currently working on using these "dead" areas within the sensor array.

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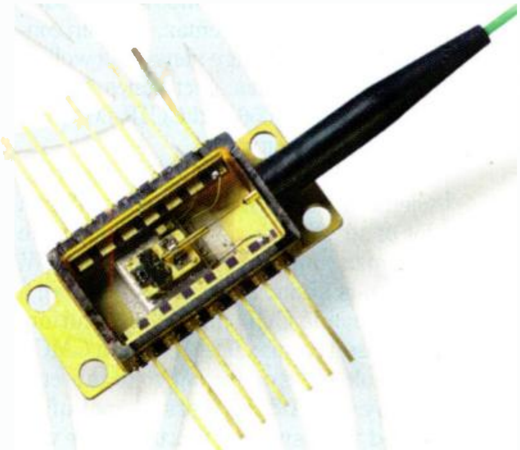

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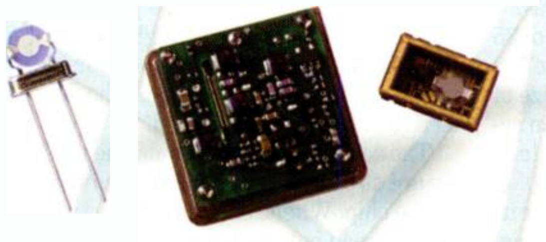

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niques. Thus, custom variants can be rapidly created. The individual modules all have full test-vector sets. The complete chip can be tested using a multiplexing boundary-scan approach, which can extend to full IEEE 1491.1 compliance if required.

One-Chip Digital Video Camera

Perhaps this year's major highlight hails from Siemens Semiconductors, Munich, Germany (Internet: *www.siemens.de)*. The Semiconductor Group of Siemens AG will show the world's first single-chip digital video camera. Dubbed Eyemax, the chip contains a CMOS image sensor, as well as the entire camera electronics. It produces a CCIR-656 and CCIR-601 compatible video output.

Compared to CCD sensors, Siemens' new CMOS approach offers a lot of advantages. A camera using the Eyemax chip consumes less than 0.5 W, which is about 80 to 90% less than a comparable CCD multichip solution. Because Eyemax uses a 0.6-µm CMOS technology, its operating voltage is currently 5 V. A 3.3-V version manufactured with smaller feature sizes will soon follow *(see "Video Sensors And Smaller Feature Sizes," p. 52)*. CCDs still require +12 V.

The higher level of integration results in a smaller camera size and, most likely, one that's cheaper. Siemens thinks the Eyemax is a good choice for applications like Video PCs, Notebooks, PDAs, and mobile videophones, along with digital photo and video cameras.

Eyemax offers a sensor array of 35 mm^2, with a maximum resolution of 720 by 576 pixels and an active pixel size of 9.6 by 9.6 µm. The optical sensor, an active linear type, uses an optical lens with a diameter of 1/3 in. (8.5 mm). It can be operated in three different modes: video at 50 frames/s, still picture, and a sequence of still pictures. Video modes may be 625/50 and 575/60, with progressive or interlaced scan modes. Plus, the chip contains an active sensor array, analog-to-digital converters (ADCs), a clock generator, memory (including 35 kbits of RAM), a controller, and a DSP.

In CCD approaches, the contents of the sensor array are multiplexed to a single, high-speed ADC. But, high frequency also means high power consumption. This, in turn, results in a higher operating temperature. Because the dark current increases as a function of the temperature, it's also dependent on the operating frequency. To reduce the conversion frequency, Eyemax reads 720 columns simultaneously by using its 720 monolithically integrated ADCs—one ADC for every individual column.

The linearity of every single ADC needs to be corrected, and the offset needs to be compensated. Eyemax's DPS takes care of these tasks. The DSP also performs the fixed-pattern-noise (FPN) correction which is necessary with every CMOS sensor.

This first model of a single-chip camera suits the low-end and medium performance market. A high-end version is expected within the next year. Compared to a CCD camera, an Eyemax prototype shows good results. Siemens took pictures of a candle with the aperture wide open, resulting in significant overexposure of parts of the picture. CCDs show a strong blooming effect in such a situation. A high accumulation of charge carriers are injected into the neighboring sensor pixels, making the candle flame appear bigger than it actually is. The CMOS Eyemax sensor didn't show this effect. Even when the candle was moved, no afterglow or effects of inertia were visible.

The contrast resolution of Eyemax is better than 1%, and the optical dynamic range beats 100 dB. Gain and gamma correction may also be adjusted by using a special DSP algorithm. As with CCDs, some pixels of the CMOS image sensor might be defective. Therefore, every sensor is tested after manufacturing, and the defective pixels are determined.

The addresses of these unusable pixels are stored in a permanent memory on the chip. Whenever such a defective pixel is read out, its value is automatically extrapolated on the fly, without significant memory demand. Eyemax only needs the addresses in its pixel memory. Eyemax's DSP is able to correct up to 512 defective pixels, but the expected defect ratio is lower by more than an order of magnitude.

Further details are scheduled to come out at the International Solid State Circuits Conference (ISSCC '99) in San Francisco next February. Siemens also is working at top speed on a single-chip color video camera. First samples of the device can be seen at Electronica '98. Such a single-chip element would provide an RGB signal at its output.

The currently available black and white single-chip camera has a 16-bit interface to the microcontroller, even though 8 bits are sufficient. The reason for this is that Siemens is currently testing the chip for special applications, like reading the sensor at 100 frames/s with a resolution of 360 by 576 pixels. That would be useful, for example, in car vision systems. Because such a feature isn't required in ordinary video cameras, only an 8-bit bus to the exterior world is needed.

Displays

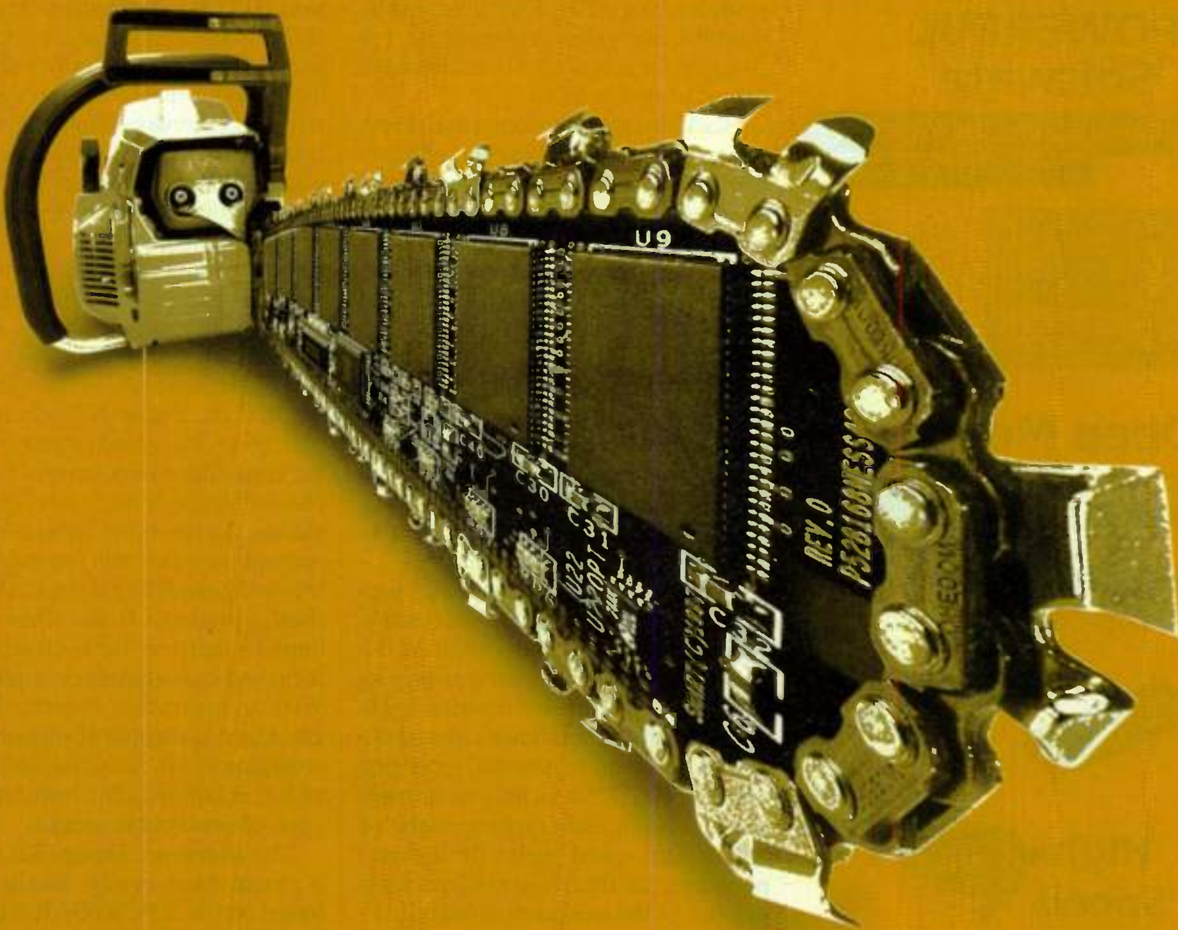
At the Sharp booth, you'll encounter highly reflective (HR) TFT color displays which require no backlight, resulting in significant power savings. Sharp also will exhibit reflective, full-color LCDs manufactured with CSTN technology.

Since the Japanese company now uses a new manufacturing process, it's able to produce plastic LCD modules that are only about half as thick and one fourth the weight of conventional glass versions. By using the new fabrication process, Sharp reduced the permeability of the transparent plastic material to gases—up to now, the most critical factor.

Thanks to the increased flexibility and pliability, the danger of breaking the display is almost eliminated. This is good news for manufacturers of mobile phones or other compact mobile devices. They can now omit the space-consuming display frame.

Look for Sharp to also show its so-called continuous-grain silicon (CGS) technology, which forms a bridge between display and semiconductor technology. They apply electrically homogeneous polysilicon crystals in an extremely thin, but highly organized layer, onto a sheet of glass. This CGS film allows the integration of ICs. Performance will be demonstrated with a CGS projector, where an LC module manufactured in CGS technology is said to provide a brilliant resolution.

Motorola Semiconductors (Internet: *www.motorola.com)* will exhibit its BlackBird Development Environment. Intended for interactive multimedia applications requiring high-performance



graphics, audio, animation, and full-motion video, the new environment can be used for applications ranging from a basic 3D-games player to true convergence multimedia products. This product includes DVD and DVD games, as well as a variety of network interface modules like ATM, Firewire, cable, satellite, and video conferencing. It's also open for new applications that have not yet been developed.

Blackbird was developed in Europe. According to Motorola Semiconductors in Munich, Germany, "Blackbird is the first open platform to support interactive 3D graphics, Java, MPEG digital video, high-fidelity audio, Internet access, electronic commerce, and broadband networking in a single integrated unit."

By combining its PowerPC CPU and communications capabilities with the so-called Project X Media Architecture, Motorola says it's created the industry's first practical "soft" set-top box. Project X offers a peak performance of 1500 MIPS.

Powered by an independently programmable CPU coupled with communications and multimedia engines, the platform can instantaneously change its role. It can go from one function to another to suit the consumer's immediate wishes, or adapt to new and emerging requirements. "With a full convergence of video, audio, and graphics, combined with a high-speed bridge for in-home networks, the Blackbird platform is positioned as the successor to today's set-top box in the same way that the PC provides far more possibilities than the single-function typewriter and a stand-alone word processor," claims Axel Streicher, product manager for Blackbird in Munich, Germany.

Motorola established an aggressive sales model to accelerate the adoption of this new technology, making it available to consumer electronics companies in reference form; as a fully assembled and software-loaded motherboard to systems OEMs; and as a complete turnkey, private-label box to be used by customers developing their systems. "Both hardware and software developers for multimedia appliances can create their own low-cost, Blackbird-derived designs quickly and easily to meet the demands of the emerging interactive multimedia market," Streicher emphasizes. An integrated development environment (hardware and software) is now available that's said to significantly reduce design and development time, while providing for very low-cost market entry.

Blackbird integrates a new software set, including a real-time operating system (RTOS), Java support, and an HTML-based Internet content engine and user interface. There's also high-level multimedia APIs, embedded security, and extensive support for broadband networking. Networking support includes complete support for ATM and IP protocols, as well as for bridging between broadband networks and the attached IEEE 1394 and Ethernet ports. Furthermore, Blackbird is capable of downloading new protocols, APIs, or applications on the fly.

The inclusion of VM Labs Inc.'s, Los Altos, Calif., ProjectX Media Architecture gives Blackbird interactive gaming capabilities that are said to exceed those of today's dedicated game machines. At the same time, it unifies a content base that will extend from entry-level consumer systems to high-end theatre products. It also offers comprehensive features for both cross-platform and cross-industry applications. With an insertable security module, Blackbird is capable of supporting the emerging North American and international standards for implementing point-of-deployment security.

The Reference Design Kit includes a production-ready motherboard based on the MPC860SAR integrated PowerPC CPU/Communications processor, and the ProjectX media processor with memory configurations ranging from 8 to 32 Mbytes of DRAM and 2 to 16 Mbytes of programmable ROM. The reference platform is configured with Motorola's media-ready, real-time operating system based on OS-9000TM, MAUI 2.1.1 and the DAVID 2.2 development environment. Blackbird also comes with a Device Mosaic 3.0 content manager supporting HTML, Javascript, e-mail, SurfWatch parental control, and SSL security. A complete documentation package contains schematics, bill of material, source code for I/O drivers, binary images of the RTOS and core application set, and executable licenses for redistribution.

More information on Electronica '98 can be obtained at *www.electronica.de.*

Laser-Driver Options Evolve As Data Rates Escalate Past 2.4 Gbits/s

As Optical Data Rates Shoot Past The 1-Gbit/s Mark To 2.4 Gbits/s And Beyond, Techniques To Drive Laser Diodes Set The Pace.

Dave Bursky

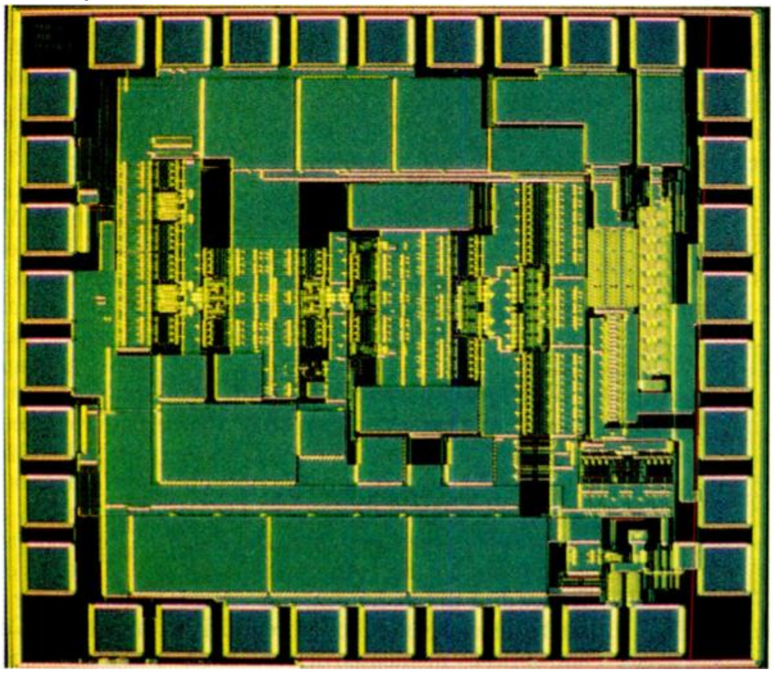
SPECIAL REPORT

As optical communication systems and optical data links move up in speed, the circuits used to drive them—laser drivers—also must improve to keep the data flowing at rates of 1, 2.4, and 10 Gbits/s and beyond. Complete optical transmitters with the laser driver and laser diode in one package, or full transceivers that pack the transmitter and receiver in a single package, are readily available. Such pre-designed solutions provide designers with standardized building blocks for established optical interfaces such as the Fibre Channel (FC), the fiber distributed data interface (FDDI), or the synchronous optical network (Sonet).

However, for designers who must deliver something with more value-added content or different performance specifications, the data interfaces must be crafted from the individual building blocks—laser diodes, laser drivers, photodetectors, and so on. Many of the key decisions revolve around the design of the basic transmit subsystem (the selection of the laser diode and the drive methodology). At data rates of 2.5 Gbits and below, the light output of laser diodes can be driven directly by a relatively simple driver circuit *(Fig. 1a)*. On the other hand, a newer technique that provides effective control of the light output at frequencies of 2.5 Gbits/s and higher, and is easier to implement than direct drive, modulates the light of a continuous-wave laser diode *(Fig. 1b)*[1].

In the direct drive approach, a bias-point is set by the driver to establish an "off" (or dim) current value that keeps the diode on, but with a very low light-emission level. Then, each time the driver pulses the diode, the light output increases dramatically. That higher light output level becomes the "on" state (bright). Therefore, the driver modulates the laser gain by pulsing the current level, switching the diode between dim and bright states.

The direct drive approach is inherently simple. But, at data rates beyond 2.5 Gbits/s, driving difficulties arise due to a change in charge-carrier density in the laser diode. That change is associated with the transition of the input current, which not only changes the optical gain of the diode material, but also changes the real part of the index of refraction within the diode's optical cavity.



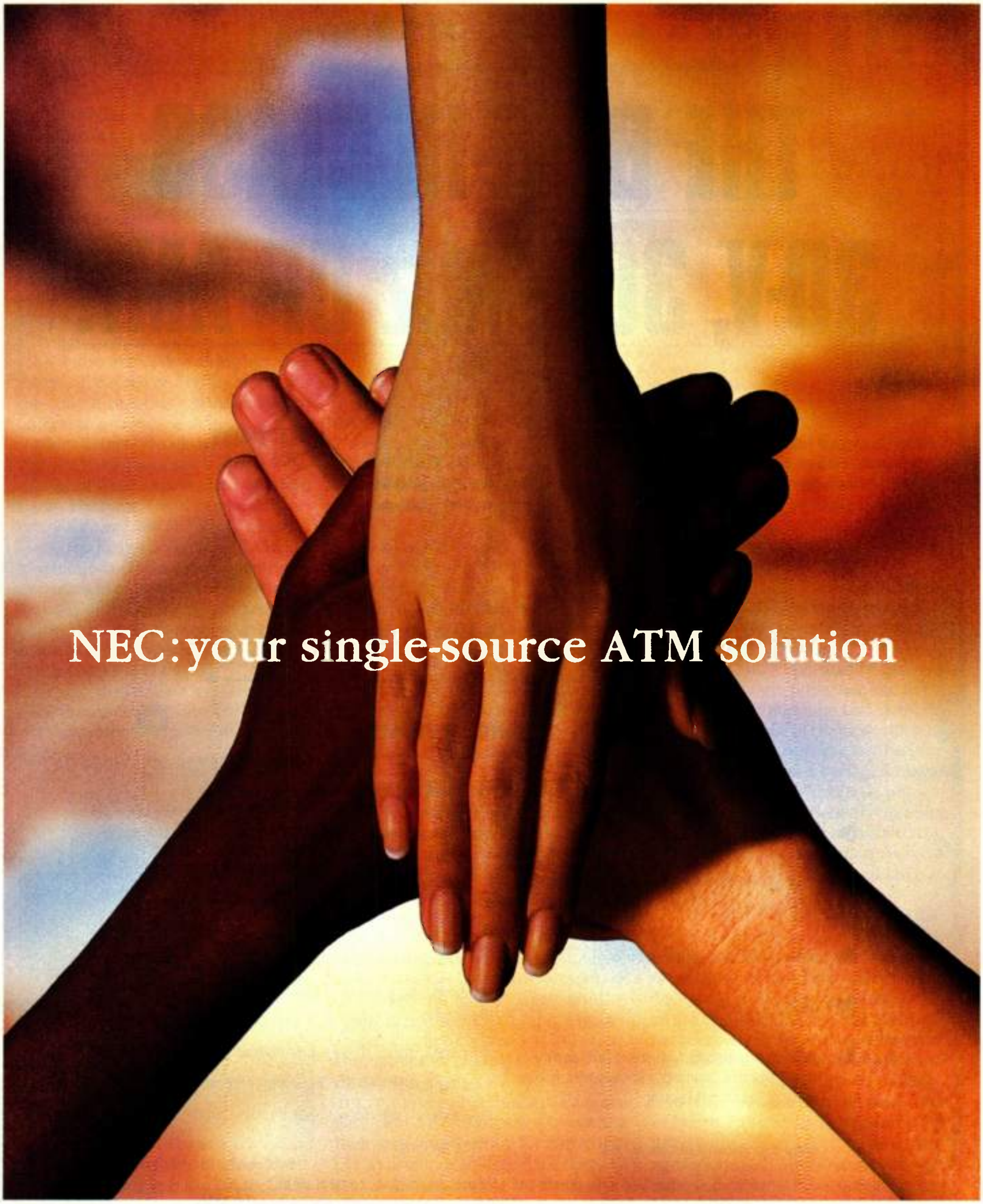
Art Courtesy: Vitesse Semiconductor

This unwanted effect, known as a "chirp," causes a shift in the lasing frequency of the diode, which, in turn, causes the optical spectrum of the transmitted pulses to broaden. A broader spectrum, along with the chromatic dispersion of the fiber itself, will limit the distance that a signal can propagate down the fiber—the more the chirp, the shorter the distance. That does not bode well for Sonet data links which can go thousands of kilometers.

The alternative to direct drive, optical modulation, minimizes the effect of chirp since rather than switching large currents, optical modulation uses a voltage to control an external light modulator. In this case, the laser is used in a continuous mode and keeps its light output constant, eliminating all chirp. The electrical data stream goes into a voltage driver, which encodes the data onto the laser beam by using the data to modulate the light output.

Direct Modulation

Direct drive circuits must deliver high-drive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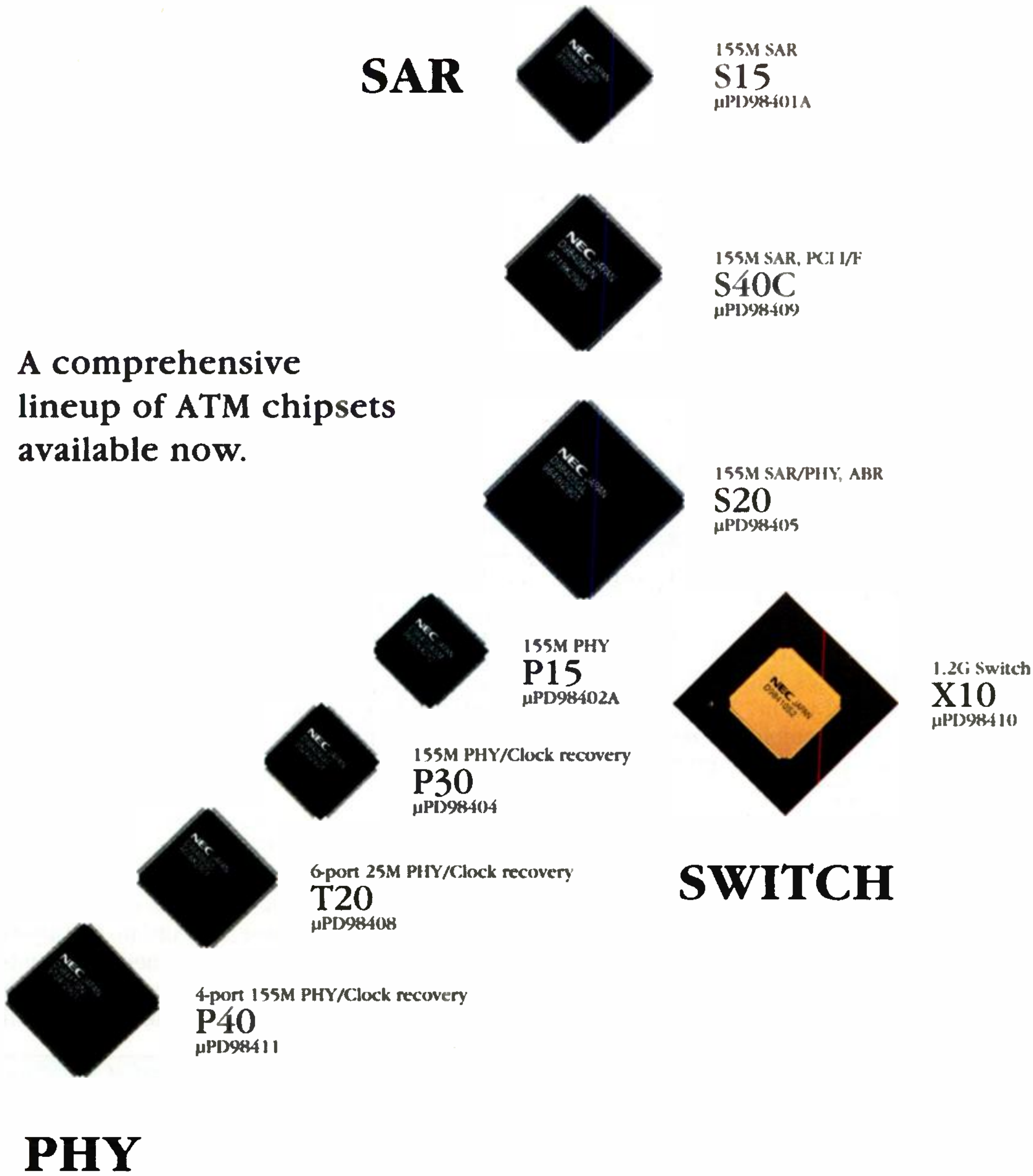

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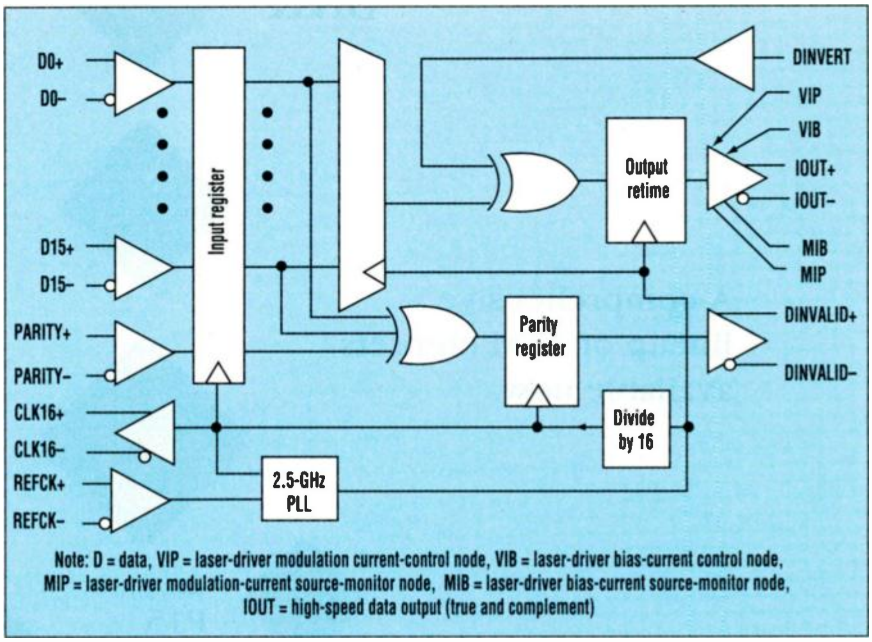
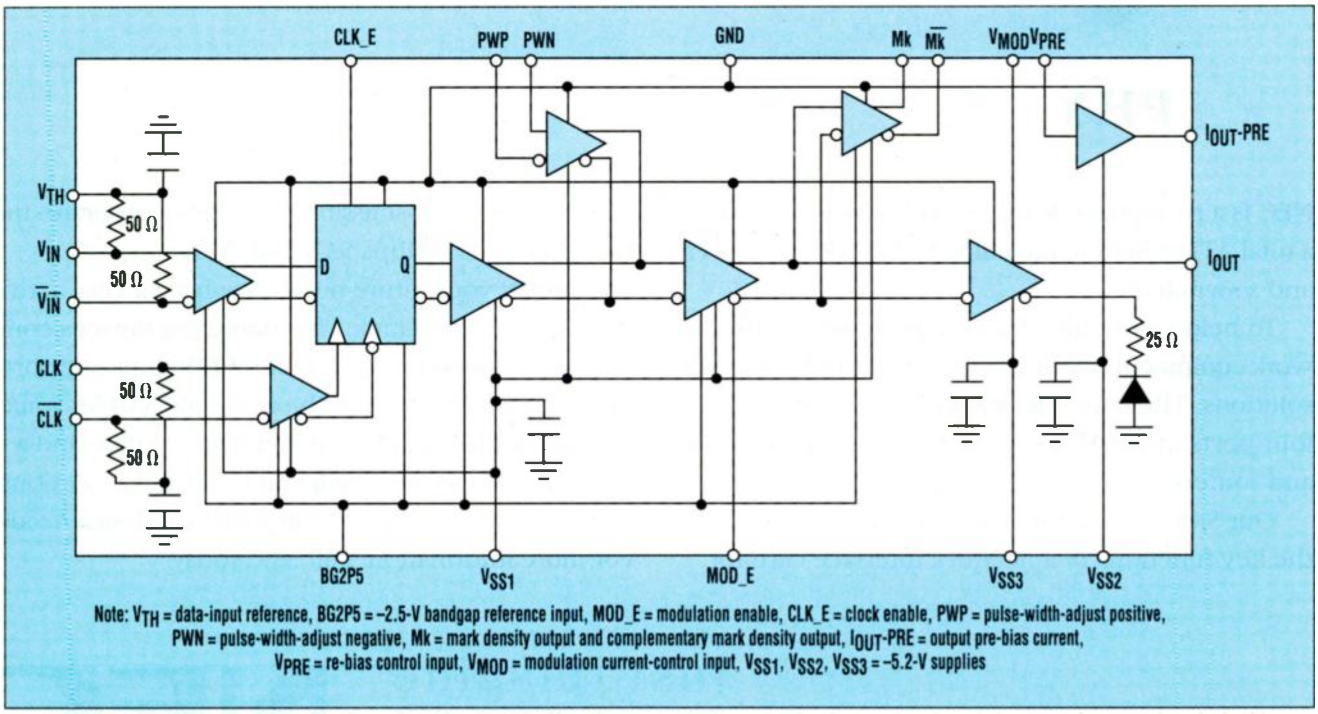
ining various integration strategies and has developed a clocked driver, the LG1627 *(Fig. 3)*. The inclusion of a flop-flop on the input stage helps reduce the signal jitter according to David Harrison, Lucent's product manager. The clocked laser driver, fabricated using a 0.9-µm-gate, will employ GaAs heterojunction FET structures. This can reduce the jitter to just 6 ps rms, compared with a significantly larger number if the clock synchronization were not used. The chip requires an external 2.5-Gbit/s clock source and a 2.5-V bandgap reference to ensure stable operation over temperature and varying supply voltages. Also available is the LG1626DXC, an optical modulator driver without clock synchronization.

Targeted at voltage-modulated lasers and operating at 10 Gbits/s, the LG1618A, also developed by Lucent, employs a balanced distributed amplifier architecture that provides 50-Ω input and output matching. The chip has differential- or single-ended outputs with a 3-V pk-pk swing. That swing, though, can be adjusted from 0.5 V up to 3 V pk-pk. The pulse width of the output swing also can be adjusted by ±30%. Also included on the chip is an output offset control circuit that allows designers to adjust the offset and reduce chirp.



4. One of the highest levels of driver integration will be the VSC8161 under development at Vitesse Semiconductor. The GaAs chip will combine a 16:1 input multiplexer, a PLL clock generator, and a 2.488-Gbit/s laser driver on a single chip, considerably reducing system complexity.

A highly integrated solution that combines a 16:1 multiplexer, clock generator, and laser driver will shortly be sampled by Vitesse Semiconductor. The VSC8161 goes one more level up the integration ladder by combining three separate functions into one chip, considerably simplifying the system *(Fig. 4)*. The chip can latch in a full 16-bit word using an internal version of the reference clock, and will bit-multiplex the word up to 2.488 GHz. An on-chip PLL generates the internal 2.488-GHz clock, which remains locked to the 155.52- MHz externally supplied



3. By including a synchronization flip-flop after the input buffer, designers at Lucent Technologies developed the LG1627AXC. This clocked laser driver can thus synchronize the input data to an externally supplied reference clock and reduce the signal jitter to just 6 ps rms.

reference clock. The laser driver portion of the chip can provide up to 60 mA of modulation current for a direct-modulated diode, and up to 50 mA of bias current. A companion chip, the VSC8162, performs the 1:16 demultiplexing and clock recovery.

Vitesse also has an extensive family of basic 2.5-Gbit/s laser drivers that are part of the V-Drive 2.5 family. The VSC7923, 24, 25, 26, and 27 drive the lasers directly, while the VSC7934 and 37 are modulator drivers. Additionally, the VSC7925 and 26 provide data-reclocking capability, while the VSC7927 and 37 offer the reclocking feature as a user-selectable option.

Optical communication systems promise tremendous improvements in data rates as designs start to proliferate at 2.5-Gbit/s OC-48 rates. And in the near future, the 10-Gbit/s systems that follow the OC-192 standard will become mainstream as laser drivers provide the power needed to modulate the optical data.

1. M. Meghelli, M. Bouche, and A. Konezykowska, France-Telecom-CNET, "High Power and High Speed InP DHBT Driver ICs for Laser Modulation," IEEE Journal of Solid State Circuits, Vol. 33, No. 9, September 1998, p. 1411.

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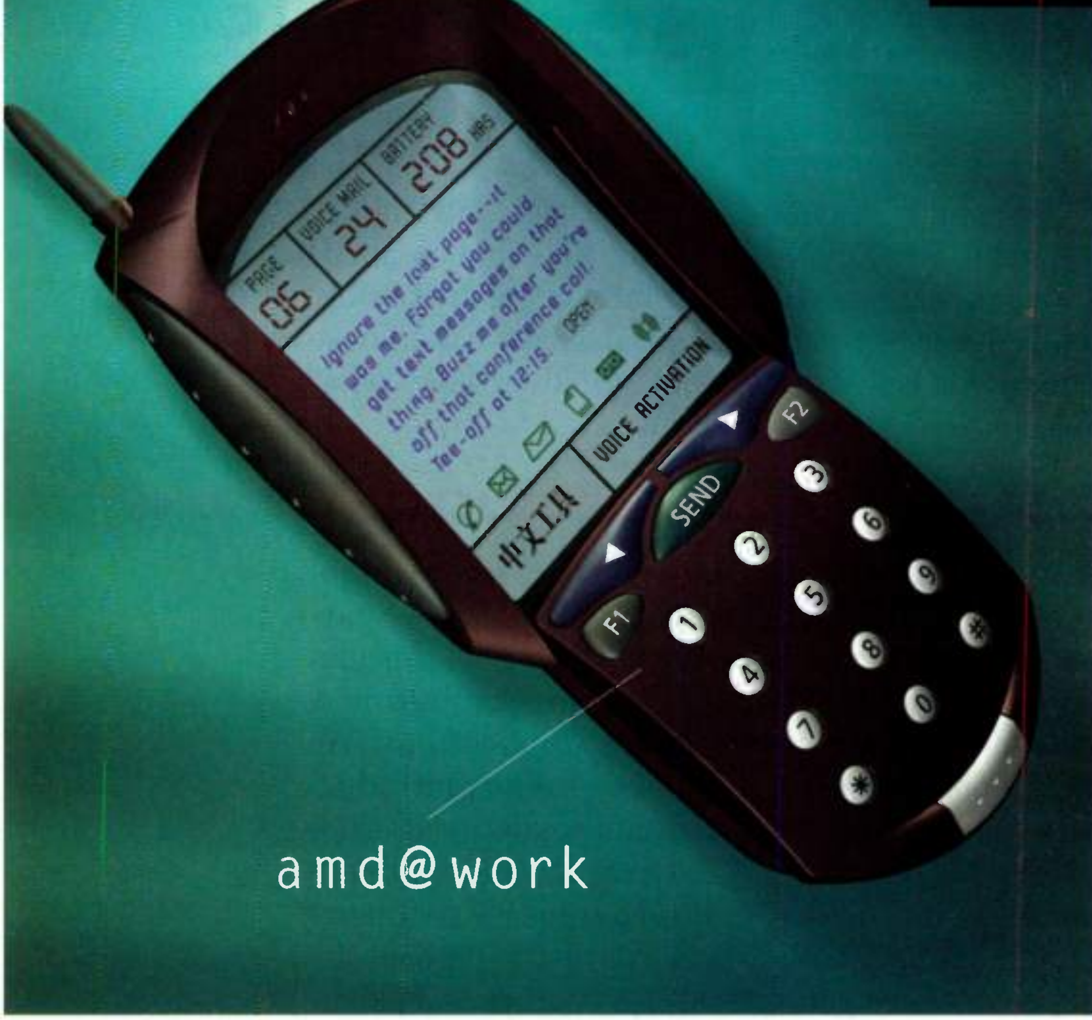

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ELECTRONIC DESIGN QUICK LOOK

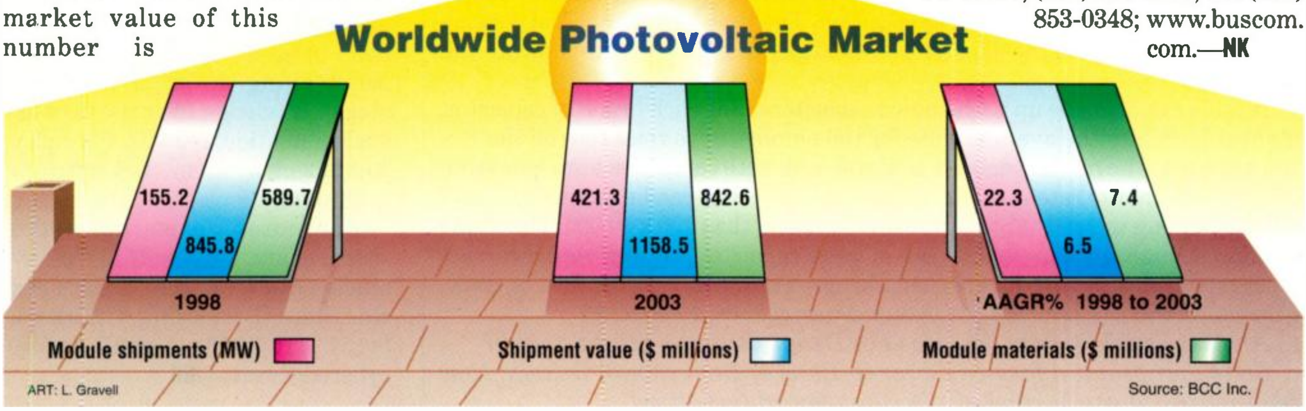
■ Edited by Nancy Konish

MARKET FACTS

Photovoltaics Market Charges Up To Make Money

Remember the gas shortage of the late 70s? Everyone had to think about whether it was worth it to drive across town for something, and the lines at gas stations seemed to grow longer each day. People started thinking about the possible shortage of oil, as well as other natural resources. We pondered whether there was another technology—one that would reduce pollution, expense, and the ravaging of our natural resources. Scientists looked around for an alternative, and solar energy broke through the clouds. Discovered in the 50s, photovoltaics was used commercially in the space program. It was basically left in the dark, however, until the oil shortages about 20 years later. Efforts then grew to develop this technology. But, oil prices stabilized and the incentives to develop solar energy, such as government investment and tax credits, virtually disappeared. Federal funding for research and development also dropped considerably. Despite these obstacles, efforts to bring photovoltaics (PV) technology into broader use have continued. The 90s have boasted more R&D funding, industry activity, and cost-sharing programs, once again providing an opportunity for solar energy to take hold. According to a study by the Business Communications Company Inc. (BCC) called, "Photovoltaics: Markets and Technologies," total shipments of PV modules hit 124.3 megawatts (MW) in 1997. The growth rate for these shipments is predicted to increase at an average annual growth rate (AAGR) of 22.3%, reaching 421.3 MW by 2003. As for the worth of these PV modules, the total shipment value is projected to grow at an AAGR of 6.5% into 2003. The market value of this number is $1.1 billion. BCC predicts that single crystal silicon will be the biggest PV technology through this forecast period, with shipments growing at an AAGR of 21.4%. That means they'd be at 201.5 MW by the year 2003. Coming in second are PV modules made out of polycrystalline silicon. Cast polycrystalline modules should go from shipping 52.1 MW in 1998 to 132.1 MW in 2003—an AAGR of 20.5%. Ribbon polycrystalline PV modules will hit 11.2 MW as long as they live up to their predicted AAGR of 19.5%. As far as worth goes, the total market value for module materials is expected to be $842.3 million by 2003, from its 1998 beginnings of $589.7 million. In 1997, traditional silicon PV modules made up 86.2% of the total market. They'll probably end up at 86% for 1998, but are expected to drop to 81.9% of the total market by 2003. They'll slow down as modules made from silicon film and thin-film materials speed up due to flexibility and low fabrication costs. Look out for these modules, which will be made from silicon film deposited on inexpensive substrates, amorphous silicon thin-film modules, and modules created from cadmium telluride thin films. As far as concentrator and other modules go, including compound semiconductor structures, they're supposed to reach 6.4 MW—an AAGR of 33.5%. One thing's for sure...the future of photovoltaics looks bright. And, as more common uses are found, the technological benefits could change and improve the quality of life. Better put your shades on to see what's below the glare of profits.

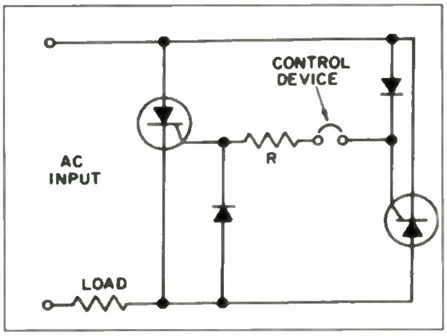
For more information, contact Business Communications Company Inc., 25 Van Zant St., Norwalk, CT 06855; (203) 853-4266; fax (203) 853-0348; www.buscom.com.—**NK**



40 YEARS AGO IN ELECTRONIC DESIGN

Silicon-Controlled Rectifier

Silicon-controlled rectifiers will be rolling off production lines in commercial quantities before the end of this year. Up till now, experimental models of the device have been the talk of the electronics industry. Developed by the Semiconductor Products Department of General Electric, Syracuse, N.Y., the three-terminal semiconductor, type ZJ-39A, unit is able to handle 16 amp at piv ratings ranging from 25 to 400 v. The control rectifier is similar to the gas thyratron. Unlike the thyratron, the silicon-controlled rectifier is activated by *current* flowing into its gate element.



When using a silicon-controlled rectifier, thought should be given to:

Voltage. Excess voltage in forward direction cannot harm the unit, but reverse voltages can.

Cooling. Heat sinks should be used to keep the unit within its specified temperature range: –65 to +125 C.

Connections. Soldering is sufficient, but a screw and a nut can be used on the cathode.

Switching Speed. Triggering can occur with gate current pulses as narrow as 0.3 µs. For resistive loads, switching time goes down as voltage goes up.

As an ac static switch, as shown in the diagram, the circuit provides high-speed switching of ac power loads. It is ideal for applications with a high duty cycle, such as welder controls, furnace heat controls, or X-ray supplies. Resistor R is provided to limit gate current. Its value depends on the magnitude of supply voltage and the current required for positive firing of the controlled rectifier. *(ELECTRONIC DESIGN, November 12, 1958, p. 46)*

Through the years, the SCR hasn't had as much publicity as, say high-density integrated circuits. But, as a power-control device, it and its offshoots have continued to be among the most useful components in the semiconductor device catalog.—Steve Scrupski

Idea For Design: Stopwatch Measures Tantalum Capacitors

Tantalum capacitors often have their markings removed in use. They're normally hard to measure, since most bridges have internal signals greater than the peak voltage ratings of these capacitors. It's inconvenient to use an external dc power supply for polarizing the capacitors. The unknown capacitor can usually be identified as to manufacturer. And, knowing this and the physical size, the possible range of capacity voltage can be narrowed down.

An easy approximation of the capacity (above 4 µfd) can be obtained with an ohmmeter and a watch. The unknown capacitor is discharged, then charged by the ohmmeter in the R x 10,000 position. The time from the initial connection to the time when the capacitor discharges to 100 is used to indicate the capacity.

A table can be made up with known capacitors. For each brand of capacitor, it should indicate the average time for the ohmmeter to read 100 (on the R x 10,000 scale). The method doesn't work too well with capacities less than 4 µfd, since the discharge rate is too fast. The discharge time can be increased somewhat by timing the discharge to a reading greater than 100 x 10,000. This value is small enough to keep the leakage of large capacitors from giving incorrect discharge times. James R. Zoerner, Design Engineer, Crosley Div. of Avco, Cincinnati, Ohio. (*ELECTRONIC DESIGN, November 26, 1958, p. 86*)

Another useful tip from the Ideas For Design section.—Steve Scrupski

Steve Scrupski is a former Editor-in-Chief of ELECTRONIC DESIGN. Now semi-retired, he can be reached at scrupski@worldnet.att.net.

Virtual Survey

Someone is finally making a go of officially looking into the visual simulation and virtual reality industry. Like the products it includes, this market has remained abstract and shrouded in some type of otherworldly mystery.

That's all about to change, however. At the hands of CyberEdge Information Services (CEIS), a market analysis corporation, the second edition of "The Market for Visual Simulation/Virtual Reality Systems" is being born. As this study evolves, it's expected to reveal and predict much of what happens in the virtual marketplace.

This is a groundbreaker because it's the first study to lead a continuous, multiyear examination of this market. This time around, CEIS even extends the breadth and depth of the study population. By combining methodical research, such as interviews with industry leaders, with surveys of existing data, they plan to reveal the first trends in this brand new, booming market.

Last year, the study showed significant growth and business opportunities in the virtual reality industry. It also uncovered some important facts for investors, developers, and manufacturers. For instance, the 1997 marketplace was worth approximately $480 million in value. In 1998, only one year later, it was predicted to reach $1 billion dollars.

More predictions and forecasts were made, but stayed within the United States. This year's study branches out to include Europe and Asia, which should result in a more global view of the virtual reality market. It will also cross the bridge from industry leader to average user, taking the opportunity to glean knowledge from users of visual simulation and virtual reality equipment, systems, and software in all applications.

For more information on the study, contact CyberEdge Information Services Inc., 1 Gate Six Rd., Suite G, Sausalito, CA 94965; (415) 331-3343; e-mail: info@cyberedge.com.—**NK**

Fill It Up With Premium Unleaded Electricity, Please

Global warming, pollution, the image of the majority of the population needing to wear oxygen masks to walk outside—this is the future that some scientists paint for us. But, what can we do to change it, aside from the basics like recycling?

Let's start with our vehicles. It's a known fact that there are more cars per person in the U.S. than basically anywhere else. Extrapolate on that, and realize that equals substantially more emissions. How much of a difference could electric vehicles make?

Last May, electric vehicles were driven in the 1998 Northeast Sustainable Energy Association (NESEA) American Tour de Sol in New York City. This association promotes the awareness, understanding, and development of nonpolluting, renewable energy technologies. The vehicles featured in the event were built by Solectria Corp., Wilmington, Mass.

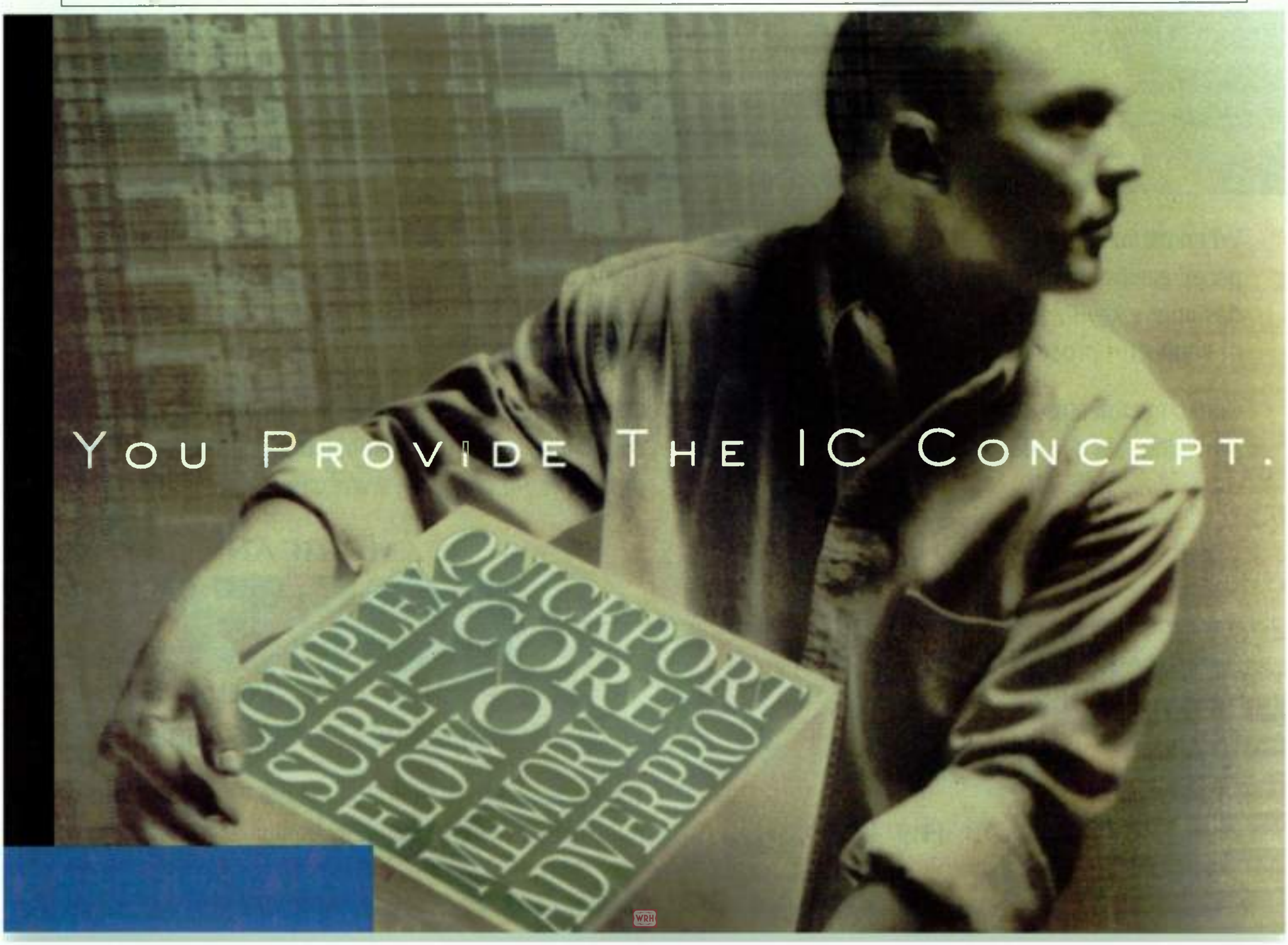
The vehicles generated 80% less greenhouse gas emissions and used one quarter the amount of energy than conventional vehicles. Keep in mind that transportation produces approximately 30% of the greenhouse gas emissions in the U.S., and these gases are the biggest contributors to global warming.

The cars in NYC also used 96.3% less petroleum than conventional gasoline automobiles. Numbers like that prove that electric vehicles also could minimize our dependence on foreign oil.

The extent to which the greenhouse gas is reduced in electrical vehicles does depend, however, on the fuels used by the local electric utility company. Con Edison, which provided electricity for the cars in the New York City event, produces electricity from about 50% natural gas, 25% nuclear, and 11% each of oil and hydro. Yet, the mixes vary with each provider. Still, even if the company used more than 50% coal to produce electricity, the reduction in greenhouse gas emissions would be reduced by at least 50% in city driving conditions.

By actually driving the electric cars along with standard vehicles, the NESEA also discovered that the electric vehicles are amazingly efficient. They took their New York City driving conditions with class, traveling four to five times as far as gasoline vehicles on the same amount of energy. To gather this information, a conventional GeoMetro was driven alongside an electric GeoMetro, and a Penske truck traveled next to an electric truck for two hours through downtown Manhattan. The electric vehicles survived the elements of the big city—the standard beeping, cut offs, taxis, and speeding—and still came out way ahead of their gas-guzzling cousins.

For more information, contact Northeast Sustainable Energy Association, 50 Miles St., Greenfield, MA 01301; (413) 774-6051; fax (413) 774-6053; Internet: www.nesea.org.—NK



Environmental Monitoring System Nabs Contaminants

A revolutionary environmental monitoring system promises to reduce the time and costs involved in analyzing contaminants. Dubbed the Environmental Systems Management, Analysis, and Reporting neTwork (E-SMART), the system was developed by a team of researchers that includes Georgia Institute of Technology engineers.

The system, which operates in real time and measures very small amounts of contaminants, consists of data management hardware and software, combined with integrated optical sensors. "Right now, the only way technicians have for field analysis is to go out and take samples, bring them back to the laboratory, and perform wet chemistry tests," says Nile Hartman, a principal research engineer at the Georgia Tech Research Institute (GTRI). "It's expensive—about $200 a sample, plus the technician's time. So instead, we have developed a sensor that operates in situ (at the site of contamination), and continuously monitors the site."

These smart sensors detect a variety of chemical contaminants, including heavy metals, solvents, and petroleum oil and lubricants. The integrated optic inferometric sensors were developed over the past decade and patented in 1997 by Hartman and the Georgia Tech Research Corp.

Laser-based technology lets the multichannel microsensor, fitted with the proper coatings, detect multiple contaminants in soil, groundwater, and air. Hartman explained that the speed of light increases or decreases when passing through materials of differing optical properties. A contaminant is detected by measuring its influence on the sensor's optical properties. Researchers observe the effects of these properties through changes in the transmitted laser light. The sensors are integrated into the E-SMART team's standardized smart sensor networks that collect, manage, and analyze the sensor data. This analysis will let environmental site managers predict the fate and transport of contaminants, perform remedial design, and gain regulatory and public approval of remedial approaches.

The sensor was licensed commercially by the Atlanta-based Photonic Sensor Systems Inc., a recent graduate of Georgia Tech's Advanced Technology Development Center—a business incubator for high-tech companies.

An E-SMART field test, expected to begin later this year, will probably be conducted at a U.S. Air Force base where cleaning agents have seeped into soil and groundwater.

For technical information, contact Nile Hartman, Georgia Tech Research Institute at (404) 894-3503; e-mail: nile.hartman@gtri.gatech.edu; or John Edwards, president, Photonic Sensor Systems Inc. at (404) 875-1028.—**NK**

KMET'S CORNER

Selling financial interests in a privately held company often presents a considerable challenge. One of three primary mechanisms serves to complete a transaction. One, a private party buys some or all of the outstanding stock; two, a publicly traded party buys the outstanding stock; or three, the privately held company attempts to go public. Shareholders generally profit significantly under any of the three options. But, what happens to shareholders and the company if a sales attempt fails, going bust?


RON KMETOVICZ

I'll describe one real data point. It offers insight into factors to consider, but by no means generalizes the situation.

Private owners of this particular company decided, for various reasons, to sell their respective interests to either a private or public party. They didn't feel that a public stock offering was in their, or the company's, best interest. To attract a buyer, the owners decided to utilize the services of an institutional dealmaker with a reputation for closing transactions of this type.

Representatives from the brokerage firm came in and inspected every facet of the business. They looked at sales, marking, accounting, product development, quality, and the facilities in a thorough fashion. Attention focused primarily on financial performance. Their quest for information led to the production of financial highlights much like you would see in an annual report. In support of the numbers, the brokers added text and graphics. Much of the story line, and text, was developed by the management team, employees, and owners of the company. In about a month, a very professional sales document on the company was available for distribution.

The brokerage house then went to work finding buyers. Anyone with an active interest came in to "kick the tires." With each visit, the owners and managers provided an in-depth review of the company. This was an attempt to inspire interest and a monetary offer. After each visit, the owners' confidence in making a sale grew as suitors indicated they would be making offers. Shareholders began to place a per share price on the stock, and from that could calculate their return. The more confidence in the sale built, the more shareholders thought about life in the future. It was time to cash in on working for a startup. It was time for dreams to come true.

As expected, serious offers began to arrive. A few buyers were bottom fishing, but two offers were both sincere and near the anticipated sales price. Majority share holders were convinced they were in a seller's market. They thought they would succeed in having the buyers raise their bids or someone else, not yet identified, would step forward with a higher bid. Neither event happened. No newcomer arrived, and higher offers weren't made. The business didn't sell, and the dreams and aspirations of shareholders exploded.

One by one, minority shareholders became convinced that the company's majority stock owners were holding out for a sum greater than what the market would bear. Under unrealistic conditions, these people began to view their stake in the startup as worthless and took the appropriate action. Gradually, a few exited for greener pastures. Those remaining reformed their views of the company. Most lost their hard-charging, long hour, company-first spirit. The will to compete and win evaporated.

The company has yet to recover. It's about one quarter its former self. Need I ask what should have been done?

Ron Kmetovicz, president of Time To Market Associates, is the author of "New Product Development, Design and Analysis." He helps new product development teams deliver profitable products to the market quickly. He can be reached at: P. O. Box 1070, 100 Prickly Pear Rd., Verdi, NV 89439; (702)345-1455; fax (702) 345-0804; e-mail: kmetovicz@aol.com.

Guide To Graphics

We all like stuff that's free, especially if it's something we need. Intergraph Computer Systems, Huntsville, Ala., has an offer. As a member of the interactive graphics industry, the company has come up with *Graphics Supercomputing on Windows NT*.

This 147-page guide comes at no charge. It contains thorough explanations of modern graphics technology and introduces key concepts behind 2D and 3D graphics. Extra help can be found in its 127 full-color images, as well as its comprehensive glossary.

Topics include:

- Bitmapped and vector graphics
- 8-, 15-, 16-, 24-, and 32-bit color
- 2D and 3D graphics and textures
- 3D graphics pipeline
- Bilinear and trilinear interpolation of multim-in-parvum (MIP) mapped images
- Gouraud and Phong shading
- Ray tracing and radiosity

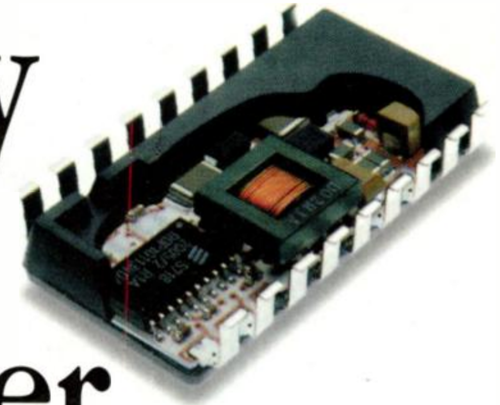
Graphics Supercomputing on Windows NT was authored by Intergraph. This company has stayed ahead in the graphics industry by being the first to offer hardware-based geometry acceleration on Windows NT, as well as the first to go beyond the 100 CDRS-03 Viewperf benchmark score on NT and support 2.5 million pixel displays without comprising performance or color.

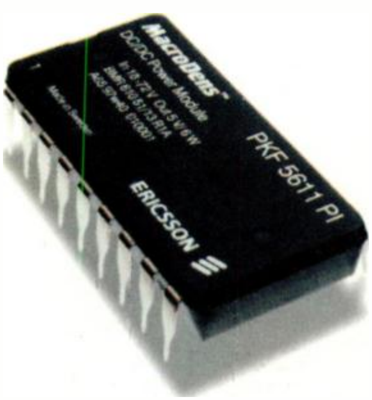
This guide is, in essence, a chance for Intergraph to provide users with the wealth of information held by the company. The goal is to keep professionals abreast of the very latest in graphics developments.

The booklet, *Graphics Supercomputing on Windows NT*, is free of charge. It's available immediately. The only catch is a $7.95 shipping and handling fee. To order it, go to *www.intergraph.com/graphicsbook.*

For more information, contact Intergraph Computer Systems, Corporate Headquarters, Huntsville, AL 35894-0001; (256) 730-2000; Internet: www.intergraph.com.—**NK**

At last, a truly advanced DC/DC power module that's flexible enough for any application





In existing designs you can boost performance and save money with the MacroDens™ PKH drop-in replacement for converters with industry standard pin out.

In new designs you can choose from through-hole or surface mount versions.

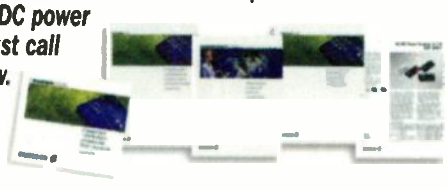
The revolutionary MacroDens™ DC/DC power module has set twenty-first century standards for performance and reliability for new electronic systems. And it dramatically cuts costs!

Now Ericsson has adapted this remarkable component for use in existing designs, without the need for board modification. The PKH is simply a full performance PKF converter with a compact 5-pin mounting adapter.

Of course, the ultimate combination of cost savings and performance is realized with the surface mount PKF. A power module which is set to become the next industry standard.

So, whether you're developing a new design, or simply want to cut costs and improve the performance of an existing one, Ericsson has the answer in the MacroDens™ power module. Flexible, twenty-first century performance delivered today.

For full technical specifications and an information pack on the wide choice of DC/DC power modules from Ericsson, just call the relevant number below.



Specification summary

- True component power: a DC/DC module in an 18-pin DIL, or 5-pin industry standard package.
- Size: 49 mm x 24 mm x 8 mm (1.89" x 0.94" x 0.31")
- Rated from 3 to 10 Watts
- Through hole and surface mount versions (PKF), both suitable for automatic placement
- Overmoulded package withstands aqueous washing
- 18/36 Vdc, 38/72 Vdc and 18/72 Vdc input versions
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RISC, *and* DSP, *and yes, multiple memories.*

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(Putting it together was a bit of a stunt.)

At Samsung, we're doing some pretty acrobatic things these days with system-on-a-chip ASICS.

For instance, our new Memorized ASIC™ is the first offering anywhere that can actually embed multiple *kinds* of memory onto one ASIC.

DRAM up to 128M, SRAM up to 4M, and Flash up to 32M are some of the possibilities. So are compiled ROM and as much as 64M of SuperRAM.™

And *with* that, we also offer you a variety of cores that includes ARM 7 TDMI, OakDSP Core, A-to-D and D-to-A cores, plus a plethora of others.

That kind of integration—onto .25 micron process technology—offers some pretty extraordinary benefits in terms of price/performance, lower power consumption, higher bandwidth (up to 17Gb/second), and of course, increased reliability.

Applications include networking, I/O subsystems, and high-end graphics. And in the low-power area: PDAS, wireless, graphics for notebooks, and GPS.

We've had some notable design wins lately—both because of sheer product prowess, and because we give you outstanding design methodology and design-center support, as well as manufacturing capacity virtually no one can match.

Talk to Samsung about Memorized ASIC and system-on-a-chip, or about cell-based, gate array, or COT ASICS.

And to think: not so long ago, system-on-a-chip was only vaporware.

If memory serves.

For complete information, visit www.samsungsemi.com, now. Or call 1-800-446-2760, or write to ASIC Marketing, Samsung Semiconductor Inc., 3655 North First Street, San Jose, CA 95134.

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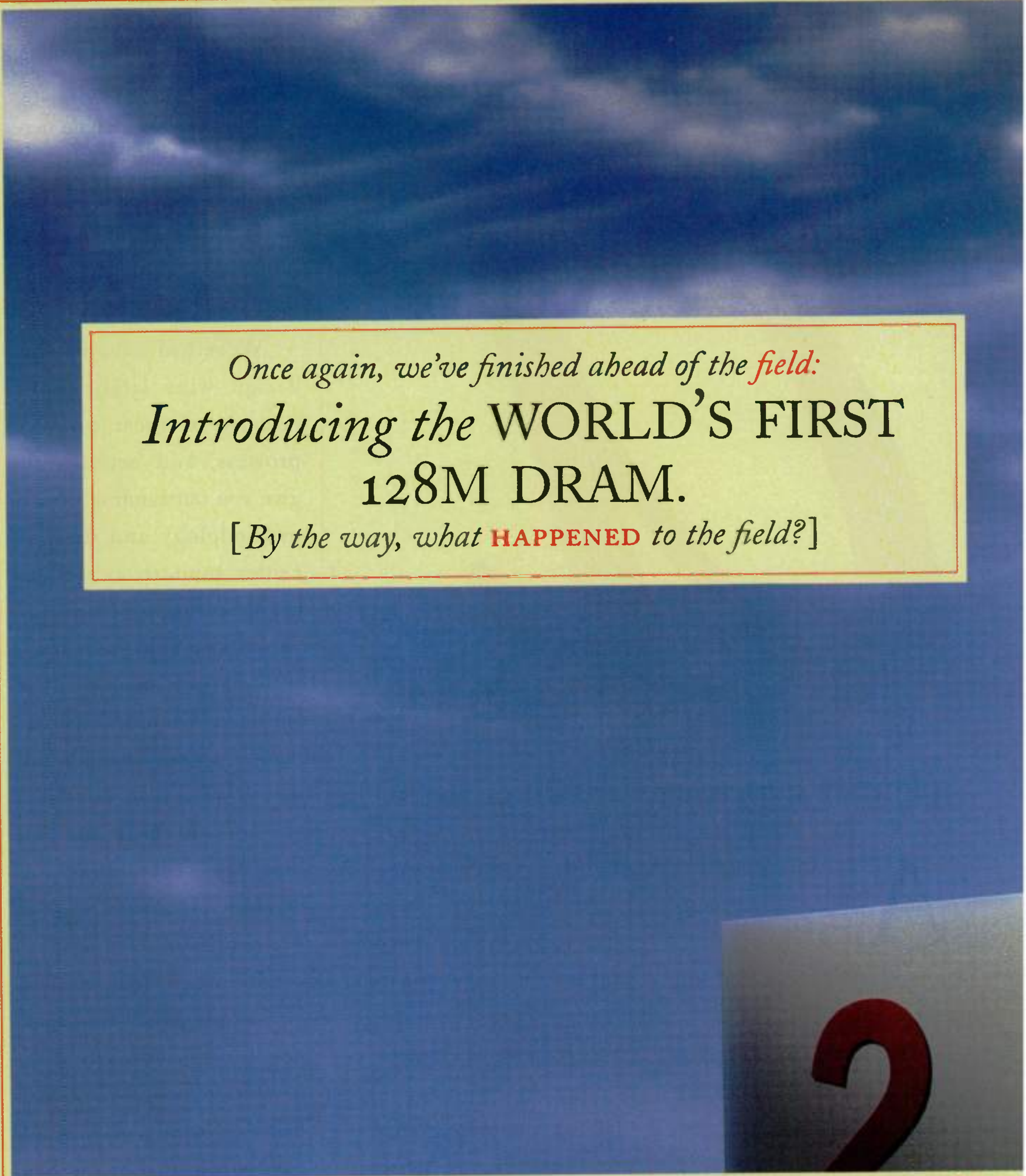
STILL A *Generation* AHEAD.



Once again, we've finished ahead of the field:

Introducing the WORLD'S FIRST 128M DRAM.

[*By the way, what* HAPPENED *to the field?*]

It's the highest-density DRAM ever made available in production volume.

It's a single chip that has hundreds of times the capacity of the computer that took Apollo 11 to the moon.

It's the 128M Synchronous DRAM, and if you want it in quantity, the place where you can get it now is Samsung.

The 128M is particularly notable when you put it into a module. For instance, we offer a 128-megabyte SODIMM, for notebooks. And DIMMS

The PC 100*–Compliant,* 128M SDRAM

COMPONENTS	
KM416S8030T-GL	8M x 16
KM48S16030T-GL	16M x 8
KM44S32030T-GL	32M x 4

MODULES	
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KMM377S3323T-GL	256MB DIMM
KMM466S1723T2-FO	128MB SODIMM

 **Assembled with Samsung* 128M DRAMs, *stacked by packaging-technology partner* STAKTEK.*


1
3
TRIPLE CROWN
16 64 256
DRAM

Now, You Really Can Read That ATM!

ATM machines can be pretty tricky. You've got to slide the card or insert it the right way, punch the correct options, and remember that darn password—all before you even tell the machine how much money you want. And, if that's not bad enough, how many of you have ever stopped at an ATM to withdraw or deposit money only to find that you couldn't see the menu because of the sun reflecting off the display screen? If so, then like me, you've probably tried anything and everything to block the sun—from a briefcase, coat, or umbrella to the good old hand-and-face-shoved-up-against-the-screen technique.

It's actually quite an amazing and funny feat to maneuver to block the light so you can see the screen and still manage to punch all the necessary buttons needed to get your money. Kind of makes you wonder whether or not you might turn on the TV one day and see yourself—briefcase held high, faced shoved up against the ATM—on an episode of "Candid Camera."

But, all humor aside, it's really a pretty serious problem that has led to—among other things—the installation of housing structures around ATM machines. Obviously, though, this is not always a feasible solution to this bothersome problem. Another solution, the MITRA sunlight-immune liquid crystal display (LCD), comes from EMCO Electronics Inc., Charlotte, North Carolina.

This display was specifically designed to address the issue of sunlight readability in even the toughest high ambient light environments. In fact, it provides such exceptional improvement on one's ability to see that it can be viewed in environments that have typically made traditional LCDs impossible to read.

So, just how is it possible for the MITRA to go where other displays have failed? Very simply, it's because of the combination of four things: an innovative backlight, the manner in which the displays lamps are driven, the optical system within the backlight module, and the use of front-of-screen filters. The latter factor provides excellent contrast at a considerably lower power when compared to other products currently on the market.

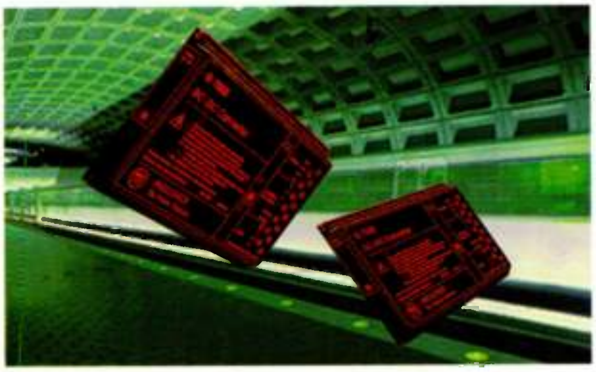
The low-profile, low-power MITRA display comes in a variety of configurations, ranging from a screen size of 6.5 to 12.1 in. with a depth of 3 cm. These dimensions are up for changing, however, as a 20.1-in. screen size is now under development. Specific characteristics include a resolution ranging from VGA to 1280 by 1024, a brightness of 1700 cd/m^2, a configuration-dependent power consumption of between 11 and 29 W, and up to 16.8 million colors. The color feature also depends on the display configuration. Additionally, the display can accommodate an analog, digital, panel link, or LVDS interface. And, its lamps are guaranteed for a minimum of 25,000 hours of continuous use.

One of the crucial benefits of the MITRA display is its plug-and-play ability, which allows for simple, no hassle set up to an existing Sharp LCD panel. And, because it comes as a complete display package and not just a collection of parts, it significantly cuts down on production time and is much more cost effective than having to purchase individual components.

The MITRA sunlight-immune LCD display is now available and will be coming your way soon in a whole host of applications aside from ATMs. In the marine market, for example, MITRA is now under investigation for use in such things as fish finders, global-positioning-satellite (GPS) navigation systems, and other on-board equipment. Other areas where you can expect to see this technology utilized include public information kiosks, as well as medical and instrumentation markets.

For more information, contact EMCO Electronics Inc., 5925 Carnegie Blvd., Suite 500, Charlotte, NC 28209; (888) 675-1117; www.emco-displays.com.

Cheryl Ajluni



Melcher's 100 W DC-DC sets new standard for railway industry.

Melcher is already the world leader in the provision of power supplies for use in trackside and railborne applications, we have established de facto standards in the industry with the M, K and S families of DC-DC converters. Now we are establishing a new lead with the Q- family of DC-DC Converters which are compliant with the latest harmonized European railway standard EN 50155 as well as the EMC directive. Featuring five different input voltage ranges from 14.4 to 168 V DC the units are suited to 24, 36, 48, 72 and 110 V DC traction batteries, and offer 100 W from a 3U x 4 TE x 160mm extruded aluminum case, free air rated to 71°C without derating. When operated to 50°C the output power increases to a maximum 144 W.

The ultra-slim profile of 20 mm is achieved by the use of a planar transformer, together with hybrid control circuits and a conversion efficiency of up to 90% to minimise losses and heatsinking. Single and dual output modules are available providing 5 to 48 V, or ±5 to ±24 V DC rails with external adjustment possibility in the range from 50 to 110% of $U_{o\,nom}$. Safety isolation levels are according to EN 60950 with approvals from UL and LGA. RFI performance is below EN 55011/22 level B, and transient susceptibility is according to specifications IEC/EN 61000-4-2, -3, -4 and -5.

4 W DC-DC Uses Planar Technology.

Melcher has released a new family of 4 watt DC-DC converters which set new standards for performance within a 24 pin DIL package. Designated IMX 4 series, the products feature a unique single substrate planar magnetic construction, with all components in SMD format mounted directly to a single multi-layer PCB which also forms the main isolating transformer.

This construction together with a high conversion efficiency of typically 82% has enabled Melcher to increase output power from the industry standard 3 W to 4 W, which reduces the profile to just 8.5 mm. At the same time, Melcher has increased the input voltage range to a very wide 4 :1 ratio, with a choice of either 8.4...36 V DC, 16.8...75 V DC or 40...121 V DC to suit 12, 24, 36, 48 and 72 V DC nominal systems. Available with single and dual outputs from 3.3 V DC to 24 V DC, the units are no load and short-circuit proof, and are fully rated over the ambient temperature range -25...71°C. An extended temperature range version of –40... 85°C is also available as an option. Isolation voltage is a standard 1500 V DC. The units offer excellent electrical immunity, complying with IEC/EN 61000-4-2, -3, -4, -5, and -6, and are UL, cUL, and LGA approved to IEC/EN 60950.

New Databook introduces 35 new products.

Melcher has introduced a new 1100 page databook which details many new lines of innovative AC-DC and DC-DC converters. The databook is also an invaluable reference on standards in the power supply industry.

Melcher manufactures more than 70 families of products, and are one of Europe's leading manufacturers for telecoms, industrial, transportation and military applications.

The databook is available in CD-ROM format. Data can also be downloaded from Melcher's website: www.melcher-power.com

NEW 12/15 W DC-DCs In 2" x 1.5" Package

Melcher has introduced two new ranges of 12 W and 15 W DC-DC converters featuring the latest single substrate planar construction. It offers unparalleled levels of performance in a compact case measuring 51 mm x 40.6 mm with a profile of just 10.5 mm. The IMX- and IMY-families are suited to "Rugged" grade applications and offers up to 17 W of output power from ultra-wide input ranges of 8.4...36 V DC, 16.8...75 V DC and 50...150 V DC. The IMS 15-family provides 17 W output power from input ranges of 14...36 V DC and 36...75 V DC and is suited to "Industrial" grade applications. Both families offer single and dual outputs from 3.3 V DC to 24 V DC and are fully rated over the temperature range -25...71°C. The IMX and IMY units are also available with an extended temperature range of -40...85°C.

JUST 4 THE KIDS

Have you ever considered hiring a tutor to help your child with homework, but couldn't find the right person? Microsoft, Edmond, Wash., may have a viable alternative. The company recently introduced CD-ROM software, called "My Personal Tutor First and Second Grade." Essentially, it provides assistance for kids ages six to eight learning crucial math, reading, and thinking skills.

Research has shown that children who work one-on-one with a partner or tutor learn more and learn better. With its TutorAssist Learning Technology, this CD-ROM attempts to provide this partnering capability with the educational approach called scaffolding. That approach asserts that children learn best when they're free to do it at their own pace. The tutor constructs a scaffold of instructional support, which provides help when the child has difficulty with a particular concept and assistance when he or she is ready for the next level. Until then, children can climb in any direction.

In practice, the TutorAssist Technology is able to assess the child's progress, recognize when help is needed, and provide targeted instructions to assist the child in learning difficult new skills. When the child needs help, Professor P.T. Presto appears and offers an engaging, multimedia tutorial to help the child learn and apply the skill in question. In fact, he stands by on every screen in his Communicator box, ready to leap into the activity and lend a hand. Meanwhile, the child continues to play without a break in the action.

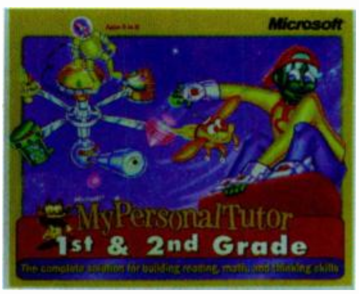
To give the child just the right amount of instruction, the TutorAssist Technology tracks more than 1000 types of errors and incorporates two levels of tips. When the child has made a few errors, Professor Presto offers a brief tutorial. If the problems continue, Professor Presto explains the concept and shows how to complete the problem—just like a real tutor.

MARIFRANCES WILLIAMS

Full of activities, games, colorful animations, engaging songs, and friendly characters, this package actually consists of three separate CD-ROMs. Each spotlights different areas of learning and interest, such as space, museums, and the ocean.

The first CD-ROM, Sky's Space Station Voyage, targets math skills. It teaches addition, subtraction, multiplication, money, fractions, comparing numbers, and place value. To do this, it uses seven games, multiple levels of difficulty, and more than 700 multimedia tutorials.

The child helps Sky—who lives on a space station—collect clues to find an alien stowaway. While there, the child can participate in many different activities. He or she can help the space gardener plant extraterrestrial trees, boogie at the alien disco, use the observatory and laser filter to search for the stowaway, or visit the costume shop to go undercover with the space police. If those aren't appealing, the child can sort space junk at the recycling center, fuel the rocket at the launch pad, or be a space sleuth—learning new skills all the while.



The second CD-ROM, Sam's Hide and Seek Adventures, focuses on reading skills. It teaches reading comprehension, phonics, vocabulary, spelling, parts of speech, rhyming words, synonyms, and antonyms. Reading comes to life with six reading games, 20 songs, 24 interactive storybooks, more than 2000 vocabulary words, 400 skill-building questions, and over 150 multimedia tutorials.

The child also helps Sam the monkey find his friends by playing hide-and-seek in a museum. The child can explore six different rooms: the toy room, folklore room, art room, travel room, nature room, and music room. Within each of these is a fun activity that corresponds with the theme of the room.

The third CD-ROM, Turru's Daring Sea Quest, targets thinking skills. The child learns geography, sorting, classifying, patterns, problem solving, and telling time—all this within five adventure games and more than 150 tutorials.

The child also sets sail with Turru the pelican on a mission to free endangered sea creatures from Captain Scratch. Along the way, they collect keys needed to liberate the creatures. The child practices time skills with Eduardo's Alarm and Edison the Eel, sorts and classifies to help Melody's Band rock the reef, uses patterns as Herb's Racers get ready for a race, builds logic at Barlow's Lighthouse, and learns about geography as he or she sets sail with Turru to guide the freed sea creatures home.

For parents, a progress report sums up the child's achievement across all skill objectives and subject areas. Rewards and certificates may be printed to encourage the child's continued success. And, each child's progress and needs are tracked individually. Even with more than one child, you only need to purchase one software set.

My Personal Tutor First and Second Grade CD-ROM set is now available and sells for approximately $34.95. For more information, contact Microsoft Corp., One Microsoft Way, Redmond, WA 98052-6399; (425) 882-8080; www.microsoft.com.

Marifrances D. Williams holds a degree in Liberal Studies from San Diego State University, Calif. She is currently a fifth-grade teacher at Los Ranchos Elementary, San Luis Obispo, Calif. Williams specializes in the identification of advanced technology for the use of child-focused applications. She may be reached at williamsofsm@lightspeed.net.

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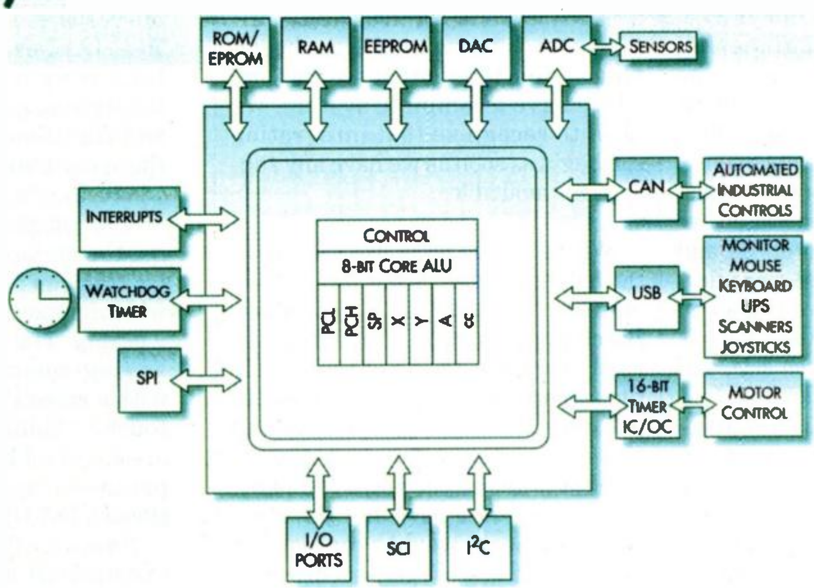
- Packages: SDIP32/42/56, SO28/34, TQFP44/64

DEVICE	ROM/ EPROM	RAM	EEP	TIMERS	SERIAL COMM	A/D 8-Bit	I/Os	PCKG
ST72101	4-8K	256	-	1x16 bit	SPI	-	22	SDIP32/SO28
ST72121	8-16K	384-512	-	2x16 bit	SPI/SCI	-	32	SDIP42/TQFP44
ST72213	8K	256	-	2x16 bit	SPI	6	22	SDIP32/SO28
ST72311	8-32K	384-1024	-	2x16 bit	SPI/SCI	8	44	SDIP56/TQFP64
ST72331	8-16K	384-512	256	2x16 bit	SPI/SCI	8	44	SDIP56/TQFP64
ST72251	8-16K	256	-	2x16 bit	I²C/SCI	6	22	SDIP32/SO28

ST7 Micros



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MANAGING THE DESIGN FACTORY

The Batch Size Problem

Many of the readers of this column work in companies that use just-in-time (JIT) manufacturing techniques. Starting in the early 1980s, JIT transformed the manufacturing scene in America by achieving huge reductions in work-in-process inventory and big drops in cycle time. The underlying mechanism for this improvement was changes in the batch size of our manufacturing processes.

Given the extraordinary impact of batch size reduction in manufacturing, it's surprising how few companies pay any attention to the batch size of their development processes. Sadly, many development processes are aptly described as the elephant traveling through the boa constrictor. We permit information to move in large batches, and stand amazed at the problems this causes.

DON REINERTSEN

For example, a company may hold a manufacturing readiness review and, upon completion, release 300 engineering drawings to purchasing. Then, the following day, they complain about purchasing being far behind in placing orders. Or, we might implement a phased development process requiring that we complete all detailed design before we build a prototype, and that we complete all product verification and testing before we engage in any preproduction activities. This is maximum theoretical batch size, and will lead to maximum cycle time.

There is another way to design development processes: We can make batch sizes smaller. Doing this, we achieve much higher levels of overlap between process steps, which leads to cycle time improvement. The striking lesson of JIT is that we can achieve order of magnitude improvements in cycle time by tackling the batch size problems in our processes.

Where are these batch size problems? Almost everywhere in the typical development process. I'll give you a half dozen ideas to help you start creating your own list:

Product Specification: Too many companies will not start development until they have 100% of their product specification completed.

Project Funding: Many have a binary approach to funding projects. Either you get nothing or you get a budget large enough to last until the end of the program.

Purchasing: We often wait until a drawing is 100% complete and then start our vendor working. We haven't learned to start our vendors off early with partial information.

Prototyping: Before we prototype any piece of the system, we wait until the entire thing is designed.

Testing: We complain about the number of test cycles the product goes through instead of recognizing that multiple, small test cycles generate critical performance information faster than one big "megatest."

System Integration: Before beginning system integration, we wait until we have a complete system. We need to recognize that integration can begin as soon as we have any subsystems available.

Whenever we minimize the size of the batch transfers in our process, we minimize cycle time as a byproduct. Batch size reduction is an extraordinarily valuable way to shorten cycle times—one that most companies fail to exploit. Interestingly, you can find a lot of expertise on how to do this inside the walls of your own company. But, it lurks in a place few development engineers would ever look...in manufacturing. Just give them a call.

Don Reinertsen is a consultant specializing in product development management. He is coauthor of "Developing Products in Half the Time" and author of the new book, "Managing the Design Factory." Reinertsen & Associates, (310) 373-5332; e-mail: DonReinertsen@compuserve.com.

PCs You Can Poke

There are many times people would like to put PCs where no PC has gone before. Say a local county hospital wanted to integrate a PC-based medical management system throughout its operating rooms, nurse stations, intensive-care units, and outpatient department. Or "Brown Sugar," a popular Tex-Mex restaurant, wanted to install PC workstations in its serving stations, behind the bar, in the kitchen, and in the manager's office.

Sure, they could've tried hooking up a standard PC, monitor and keyboard. But, those situations really called for full PC performance in a package smaller and more durable than your average computer setup. That's where Advantech's Panel PC enters the picture.

Integrate a PC into a unit 3.67 in. thick, throw in an LCD panel, use a touchscreen for the user interface, and you wind up with the Panel PC. Now, you can mount a PC anywhere—above a dentist's chair, in a kitchen, next to a hospital bed, etc.—just use your imagination.

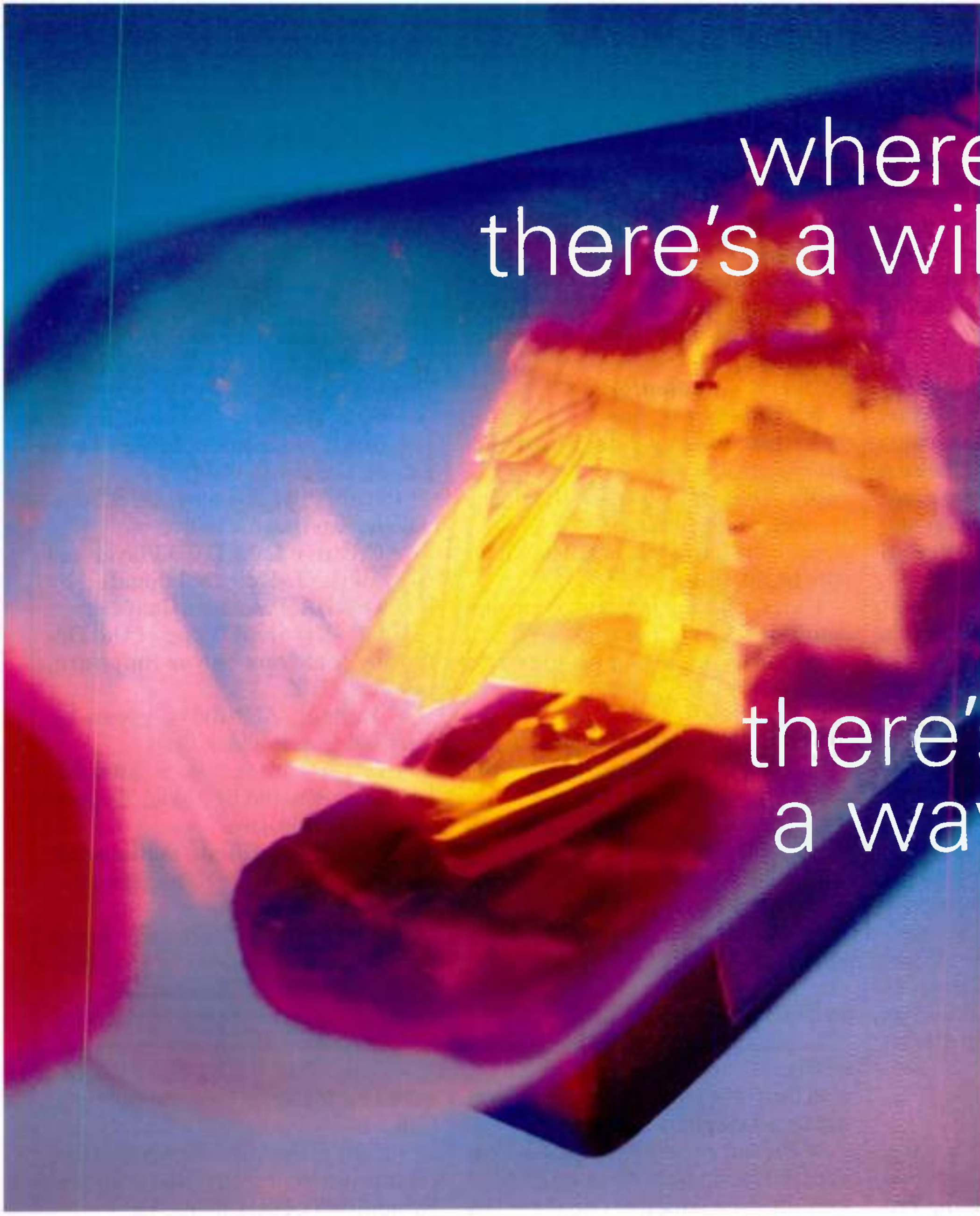
There's a full line of Panel PCs: 386, 486, Pentium, and Pentium MMX systems with integrated 5.7-, 10.4-, 12.1-, and 13.8-in. LCD panels. Each computer is high-temperature tested, as well as dust, water, and vibration resistant. Because these computers can be kept anywhere, they've got to be tough.

You can also network them using the on-board Ethernet interface (Novell NE2000-compatible), which supports 100/10 Base T networking. The user interface is an analog-resistant touchscreen with a rated lifetime of 30 million touches. Multimedia applications are handled by a built-in sound processor, speakers, and an optional CD-ROM drive.

Based in Taiwan, Advantech maintains 20 offices in 10 countries worldwide. The company focuses on embedded computing, industrial automation, telecommunication, and Panel PCs.

For more information on the Panel PC, visit Advantech's web site at www.advantech.com.

Bob Milne



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READER SERVICE 124

Contest Alert! Contest Alert! Contest Alert! Contest Alert!

It's Friday night and you—like the rest of us—have had a long, hard week at work. Your computer crashed, your boss just got another undeserved promotion by taking credit for your great idea, you found out that the bonus you were promised won't become effective until January 2001...And, to make matters worse, you had a flat tire on the way home.

But, do you really want to be a couch potato, letting life pass you by, eating that gallon of ice cream and watching yet another rerun of "America's Funniest Home Videos?" Why not pick yourself up off that couch and do something fun for a change? Who knows, you may even win a prize. All you have to do is enter the 1998 *ELECTRONIC DESIGN* EDA CHALLENGE.

"What?," you ask. You've never heard about this contest before? Oh, I get it, too busy watching the Clinton fiasco on CNN. Or, maybe you're just waiting for that next Elvis sighting. Well, for those of you who have been otherwise preoccupied, here's the specifics. And this time, PLEASE pay attention! (Complete contest details also can be found on *ELECTRONIC DESIGN*'s web site at *www.elecdesign.com.*)

What You Have To Do:

The rules are simple. Pick a topic, then write about it in any format you choose. There's just one catch: You have to use as many names of EDA Tool Vendors as you can. You can work their names into the regular text or just talk about them as vendors. You could even change the words to a popular song like "Jingle Bells" or "Frosty the Snowman." There's tons of ways to include their names, so basically the choice is yours. Winners will be judged according to how many EDA Tool Vendor names are referenced, as well as the general creativity of the submission.

Here's a few examples to get you started:

A Designer's Life:
The roses are wilted,
The violets are dead.
ASICs are running around in my head.
My days are spent thinking of what to build next,
So we can get to market ahead of the rest
But my data is bad,
And my computer just broke.
I wonder if they have this problem at ***IKOS***?
Dilbert's my ***Mentor.***
My ***Cadence*** is gone.
No matter what I do, I just can't get along.
My ***Frequency*** of visits to the counselor has increased.
If I don't leave this job soon, I'll for sure be deceased.
But, ***CoWare*** won't hire me and ***Analogy*** won't either.
So until something changes, I'll have to stay a designer.

Ode to ***Harris*** the Designer:
There once was a designer from ***Orcad,***
Whose design's flopped so much that he felt bad.
The ***Accolade's*** he missed, and his boss just got pissed,
So he quit and went to work for ***Synopsys.***

Submission Guidelines:

1. Submissions cannot exceed 300 words.
2. Only one submission per person will be accepted.
3. Please refer to the EDA Tool Vendor List on *ELECTRONIC DESIGN'S* web site for a listing of current EDA Tool Vendors.
4. All *ELECTRONIC DESIGN* readers are eligible to participate, unless employed by an EDA Tool Vendor.
5. The contest runs from October 1 through November 30, 1998.

Where To Send Submissions:

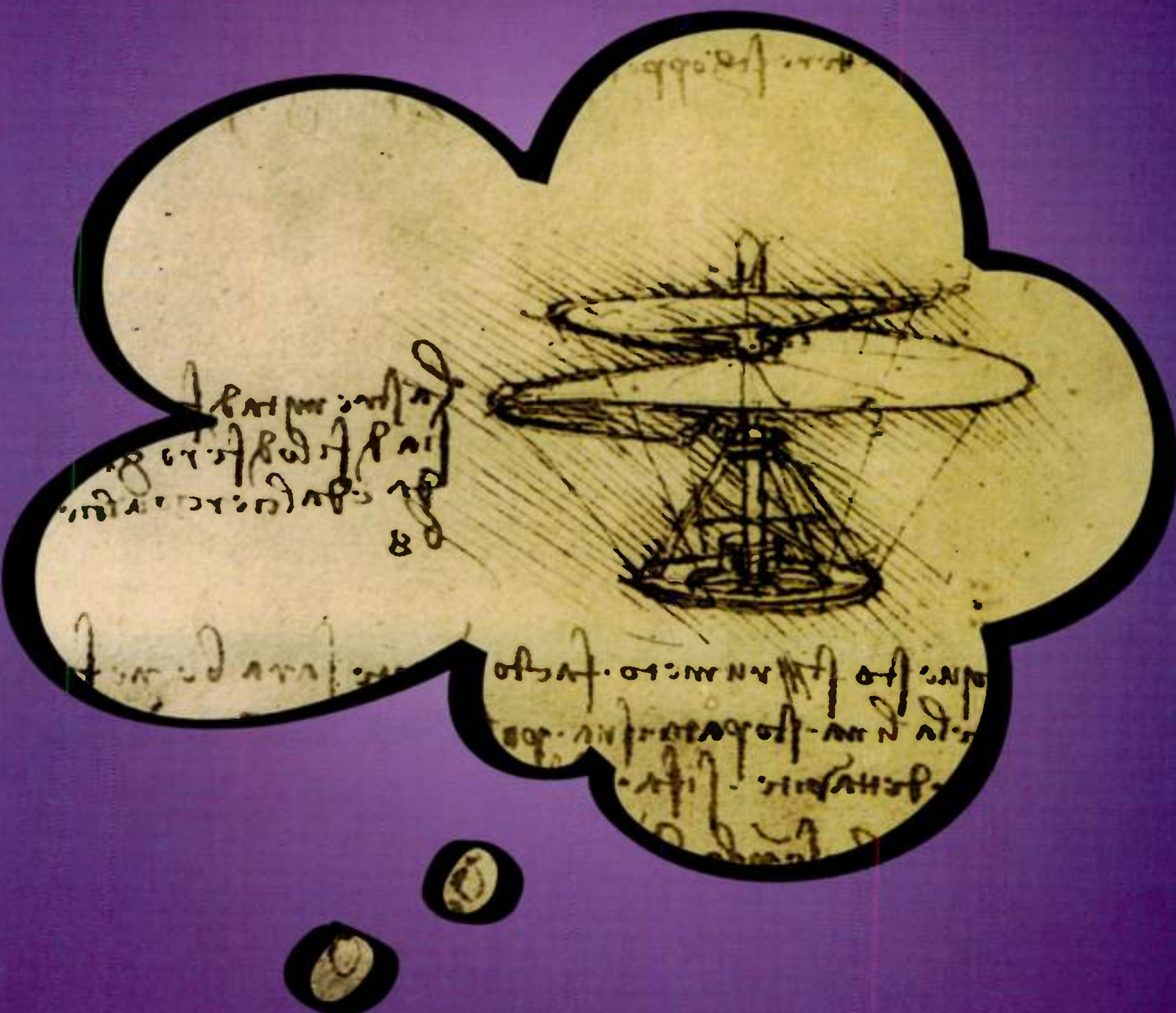
Submissions must be received no later than November 30, 1998. Send all entries to Cheryl Ajluni, Electronic Design Automation (EDA) Editor c/o Electronic Design, 2025 Gateway Place, Suite 354, San Jose, CA 95510, or via e-mail at cjajluni@class.org. Be sure to include your name, address, company affiliation, phone number, and e-mail address.

Now for the really good part! Winners will be announced via the *ELECTRONIC DESIGN* web site on December 15, 1998. Some of the winning entries may even be published in the magazine. Winners will receive one of the following prizes:

- Magellan GPS 400XL Navigation System donated by Orcad, Beaverton, Ore.
- GPS Tripmate Navigation System from Transcendent Design Technology, Camarillo, Calif.
- Palm Pilot given by Accel Technology, San Diego, Calif.
- Creative Labs DVD Player and copy of the L-Edit tool donated by Tanner EDA, Pasadena, Calif.
- CD Player and copy of the Debussey tool from Novas Software, Milpitas, Calif.
- Iomega ZIP drive given by Veribest Inc., Boulder, Colo.
- Dilbert Survival Pack ($200 dollar value) donated by Model Technology, Beaverton, Ore.
- $200 gift certificate for dinner at Eulipia donated by Synopsys Inc., Mountain View, Calif.
- $100 gift certificate and copy of the TK Solver tool given by Universal Technical Systems, Rockford, Ill.
- $100 gift certificate from IKOS Systems, Cupertino, Calif.
- Copy of the VHDL Easy tool donated by MINC, Colorado Springs, Colo.
- Copy of the Waveformer Pro tool (Windows version) donated by SynaptiCAD, Blacksburg, Va.
- Seat in a Verilog or VHDL class (a $1395 value) donated by Seva Technologies, Fremont, Calif.
- 100 Ty Beanie Babies, donated by InterHDL, Los Altos, Calif.
- Dilbert Desk Calendar donated by Xynetix, Fishers, N.Y.

Did you get all that? Granted, there's no ***MINC*** coat. But, with so many fabulous prizes to win, how can you afford not to at least try your hand at this contest? Don't think about it. Just follow the contest guidelines I've provided above and do your ***VeriBest*** to ***Accel!*** I promise it will be worth the effort. You may even surprise yourself. Besides, can you really afford to gain an extra pound or two from eating all that ice cream?

Cheryl Ajluni



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READER SERVICE 175

Mobile Phones Link Straight To Domestic Violence Hotline

There's always hope that all of this new technology will make life safer and easier. Unfortunately, companies are often so busy designing and developing that they can't devote time to finding philanthropic uses for their technology. The best intentions often fall by the wayside.

Occasionally, though, someone sees a way that they can help out. Bell Atlantic Mobile, Bedminster, N.J., recognized such a gap and filled it. This company is the first wireless carrier to introduce a toll- and airtime-free link to the National Domestic Violence Hotline. Users can now reach the hotline simply by dialing *HOPE from their wireless phones.

This feature enables customers in abusive situations to obtain advice anytime and from anywhere, as long as they're within the company's Maine to Georgia footprint. Bell Atlantic Mobile's ongoing relationship with the Family Violence Prevention Fund also has prompted the company to distribute awareness cards to its 200 communications stores and 7000 employees. The cards detail tips on how women can protect themselves from an abuser.

According to the hotline, this free service provides valuable support to women in need. Women who fear or experience abuse often live in danger. The home phone may be turned off, or it can't be used safely because the conversations are monitored. In serious domestic disputes, it can simply be unsafe for the woman to remain present in the house. In these instances, the ability to easily connect to a hotline from a wireless phone is invaluable. It could literally save lives.

Bell Atlantic is concentrating on bringing its employees a greater awareness of violence against women, as well as to its customers and the world at large. Denny Strigl, group president and CEO of Bell Atlantic Global Wireless, emphasizes the company's desire to educate employees. The information cards are one example of this effort. By alerting employees, the company provides essential tools to those who are in a position to help victims. Hopefully, employees will be able to better recognize the symptoms and play an active role in both the domestic violence prevention and life rebuilding processes of those they see around them.

Bell Atlantic's community service program utilizes the company's resources and technology in many ways. Its HopeLine program provides free voicemail boxes to victims living in shelters. The program also has donated pre-programmed wireless 911 phones to police departments and district attorneys' offices to be distributed to women at risk. This year, $100,000 was earmarked to help victims by providing wireless technology solutions.

To find out more, contact Bell Atlantic Wireless at www.bam.com.—**NK**

TIPS ON INVESTING

Good News Comes From D.C.—Unbelievable? Read On.

This is a special tax legislation update. Now, more investments qualify for 20% capital gains tax. For the third time in less than two years, President Clinton and Congress have approved significant tax legislation that will impact millions of Americans. The latest legislation, signed into law on July 22, 1998, is the IRS Restructuring and Reform Act of 1997. While the bill focuses primarily on IRS restructuring and revisions to previous legislation, investors should be happy to learn of a specific provision that reduces the holding period for long-term capital gains rates.

Following, find a brief overview of the key provisions that we believe will have the most impact on our clients:

A lower, long-term capital gains holding period brings good news for investors. Retroactively, for sale of securities after December 31, 1997, the new law eliminates the requirement that individuals and other non-corporate taxpayers hold their securities for more than 18 months to qualify for the maximum long-term capital gains tax rate of 20%. The 20% tax rate is now available for sales of securities held for more than 12 months.

HENRY WIESEL
CONTRIBUTING EDITOR

Convert to a Roth IRA by December 31, 1998 and receive new tax options. If you convert your regular IRA into a Roth IRA by December 31, 1998, you can elect one of two tax treatments:

1. Report the taxable amount from the conversion as 1998 income.

2. Report the taxable amount from the conversion equally over a four-year period.

To help determine if the Roth IRA is right for you, ask your financial advisor for an analysis of your financial status.

Consolidate Roth contributions and conversions into one account. All Roth IRAs, whether containing contributions or converted amounts, are now aggregated for the purposes of determining the taxation of distributions. Therefore, if you maintain separate contributory and conversion Roth IRAs, you may wish to consider consolidating your accounts into one.

Please keep in mind that the scope of this legislation is quite broad, containing more than 160 provisions.

For a free brochure on the IRS Restructuring and Reform Act of 1998, or help in opening or converting Roth IRAs, write or call Henry Wiesel, vice president, qualified plans coordinator at Smith Barney, 1040 Broad St., Shrewsbury, N.J. 07702; (800) 631-2221 ext. 8653.

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TRUDEL TO FORM

My last column asked a few questions, which are posted on my web page for your convenience. With your answers, I can better serve your interests.

We've been discussing how firms can obtain sustainable competitive advantage through innovation. The questions help me gauge whether your employers are even close to being ready for this. I expect most to not be ready.

For this, there are several reasons. The greatest is the "dead horse" syndrome. In past ages, our society was wise enough to know to dismount when the horse died. Today, we have the technology to flog life support and MBA management harder. We've created the living dead. These dead horses can still stumble along, and they eat less.

JOHN D. TRUDEL
CONTRIBUTING EDITOR

You can squeeze profits from dying firms for years. Even experts can't discern the balance sheets of businesses going out of business profitably from those of firms investing in growth. For a time, Wang—savagely downsized, totally hollow, and just coming out of bankruptcy—had the best balance sheet in the computer industry. Wall Street, of course, only cares about stock price, not corporate health.

A recent article in the *IEEE Engineering Society Newsletter* by Cindi Voegtli scolded engineers for not taking management seriously ("Being 'Relevant' as Managers," Vol. 48, No. 1). It blamed Dilbert for fostering disrespect and noted that management was necessary. That misses the point. Management itself disrespects management. Doesn't upper management tend to promote the content-free bureaucratic wonks who obey orders? Hence, the pointy-haired boss.

The second reason that firms avoid innovation is that change is scary. The Machine Age was about incremental refinement and avoiding embarrassment. The Information Age is about innovation, and that road is bumpy.

All new products are imperfect, and the "killer products" usually come from years of experimentation. Consider pen-based computing. A string of strong firms fumbled for years: GO Corporation, several of AT&T's and Japan's companies, Apple's notorious Newton, etc. After all this, U.S. Robotics got it right with the Palm Pilot.

You can tell you have it right if large predators attack. GO supposedly got taken advantage of by Microsoft, who was given their plans under nondisclosure. They didn't disclose. They did it themselves, but it didn't work for them either. History repeats, so now we have the Windows Palm, or whatever.

Lastly, people shun innovation because abuse and creative accounting can temporarily produce better profits. I think America Online (AOL) is a master at this. They started from innovation—a simple-to-use Internet service with a GUI interface.

AOL's stock soared. But, they wrote off $385 million in 1996. Years of profits vanished. They had flooded the world with "free" floppies as bait to sell expensive service. Three million customers per month were trying to cancel, but AOL dragged it out to squeeze several extra months of billing.

To recover, AOL sold a product they didn't have—unlimited service. Users couldn't get connected, and service was poor. Lawsuits resulted. This year, AOL got sued again for putting unauthorized charges on customer's cards. They are now getting slammed for "fancy accounting" (source: *Wall Street Journal*, *Oregonian*).

AOL's practices are very profitable: $20 ↔ 3 million ↔ 3 months = $180 million, so a few million in legal costs is nothing. Problem is, customers catch on. Innovation is better, but that takes ability, commitment, and staying power.

John D. Trudel, CMC, provides business innovation consulting to selected clients. Lectures, keynotes, and workshops also are available. He is the author of "Engines of Prosperity." The Trudel Group, 33470 Chinook Pl., Scappoose, OR 97056; (503) 638-8644; fax (503) 543-6361; e-mail: jtrudel@gstis.net; Internet: www.trudelgroup.com.

PC Apparel

Pretty soon, going out could mean getting dressed, putting on shoes and accessories, and then—before heading out the door—clipping on a wearable computer. Despite the drawbacks of being "wired" all the time, even on the go, the convenience of this technology is prompting it to forge ahead.

At the IBM Fair '98, Tokyo, Japan, IBM demonstrated its Kopin CyberDisplay-enabled wearable PCs. The working prototype comprises an IBM ThinkPad 560x shrunk to the footprint of a Palm Pilot. Weighing only 10.5 oz., including the battery, it boasts 240 Mbytes of storage and 64 Mbytes of EDO RAM.

Geared toward maintenance, repair, and system installation personnel, the wearable will be used to display wiring diagrams, inventory lists, schematics, and video. According to IBM, it's an extremely convenient tool, due to its size and capability. Its 233 MHz even lend it enough power to run IBM's Via Voice speech software.

As for its high-quality image, the optical images come from the Kopin Corp.'s CyberDisplay 320. This display produces a high-resolution image on a small-format .24-in. diagonal AMLCD screen. The technology is the same as that used in high-end notebook PC screens. And, the CyberDisplay optics have an appearance similar to those seen on a standard desktop PC monitor.

With such advanced technology successfully combining to create a prototype, there's no doubt that the wearable is coming. Once it becomes the standard method of repair or service, it's only a matter of time before the industry finds more places to wear it.

For more information about the display, contact the Kopin Corporation, 695 Myles Standish Blvd., Taunton, MA 02780; (508) 824-6696; fax (508) 824-6958; Internet: www.kopin.com.

To find out more about the wearable prototype, get in touch with the IBM Corporation at their web site: www.ibm.com.—**NK**

DESCRIPTION

The FT and FS Series are comprehensive lines of ultra compact power factor corrected models derived from our Moduflex® family of switching power supplies. This series utilizes advanced technology to produce a high quality input current wave form that is compliant to the harmonic requirements of EN61000-3-2. Based on modular construction, "off the shelf" modules permit high volume manufacturing with an outstanding quality level assuring timely delivery at a competitive cost.

Three classes of output modules are available. The **STANDARD** outputs allow short duration surge currents on all auxiliaries for hard starting loads. Optional **CURRENT LIMITED** outputs have square current limiting and feature wireless droop current sharing. Optional **ENHANCED** outputs have square current limiting, one wire star point current share, output good logic signal with LED, nominal 5V local bias, individual inhibit and margining. For requirements that cannot provide minimum load on the main output, the **ZERO PRELOAD** option is available for main outputs up to 500 watts.

DELIVERY

Choose stocked units or construct a model number using stocked modules for fast delivery. Otherwise, form a model from the adjacent page to meet your specific requirements. Contact factory for deliveries on models derived from non-stocked modules.

FEATURES

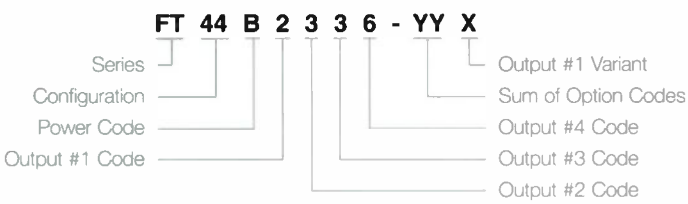
- 0.99 power factor.
- 5.5 watts per cubic inch.
- 1-7 outputs, 400-1000 watts.
- 120 kilohertz MOSFET design.
- Universal input.
- UL, CSA, TÜV (IEC, EN), CE.
- FCC, EN Class A EMI.
- IEC, EN Immunity.
- All outputs:
  - *Adjustable*
  - *Fully regulated*
  - *Floating*
  - *Overload and short circuit protected*
  - *Overvoltage protected*
- Standard features include:
  - *System inhibit*
  - *Fan output*
- Options and accessories include:
  - *Power fail monitor*
  - *Redundancy*
  - *Current Limited Outputs*
  - *Enhanced Outputs*
  - *Zero Preload*
  - *End fan cover*
  - *Top fan cover*
  - *Rack Assemblies*

STOCKED MODELS - Available in 3 days.

Max Power	Output 1	Output 2	Output 3	Output 4	Model*
400W	5V @ 50A	12V @ 12A	12V @ 12A	5V @ 10A	FT46A2332-45P
400W	5V @ 50A	12V @ 12A	24V @ 6A	12V @ 6A	FT46A2363-45P
600W	5V @ 60A	12V @ 12A	12V @ 12A	5V @ 10A	FT46C2332-13P
600W	5V @ 60A	12V @ 12A	24V @ 6A	12V @ 6A	FT46C2363-13P

**400W models include power fail monitor, current limited modules, zero preload and end fan cover options. 600W models include the same options except fan cooling is built into the unit.*

UNITS FROM STOCKED MODULES - Available in 2 weeks.



Configuration: Allowable quad output configurations are 42, 44, 46 and 48.
Power Code: Choose Power Code A through D for 400-750W models.
Output Codes: Select any outputs from the shaded area on the Output Types table consistent with the configuration chosen.
Option Code: Specify Option Code. Refer to the Option table. Codes 02 (redundancy) and 16 (enhanced) are excluded from models available in 2 weeks. Fan cooling is built into 600 and 750W units.

OPTIONS

Option Code	Function
00	None
01	Power Fail Monitor
02	Redundancy
04	Current Limited
08	Zero Preload
16	Enhanced
32	End Fan Cover
64	Top Fan Cover

Replace the YY with the sum of the Option Codes.

MODEL SELECTION

Models are available in power ratings of 400 to 1000 watts, with corresponding code letters A through E. See Power Code chart.

Output modules are available in six types: J, K, L, M, N and P in nominal power ratings from 75 - 500 watts. Type M, N and P modules are variable power rated depending upon the unit power rating. The M, N and P Module table directly below shows the corresponding multiplier applicable to the output current ratings of the M modules and allowable power ratings for the N and P modules. For example, a 750 watt multiple will have its M type module configured to produce 120A @ 5V or 12A @ 48V. The voltage and current rating of output modules are listed in the table of output types. This table assigns an alpha-numeric code designating the nominal voltage rating of the module.

Power Code	Unit Power Rating	M Module Current Multiplier		N/P Module*
		Single Output	Multiple Output	Allowable Power Rating
A	400W	0.8	0.5	250W
B	500W	1.0	0.6	300W
C	600W	1.2	0.8	400W
D	750W	1.5	1.2	500W
E	1000W	2.0	1.5	750W

**When an N or P module is used as the main output, the allowable power and the module current ratings must not be exceeded.*

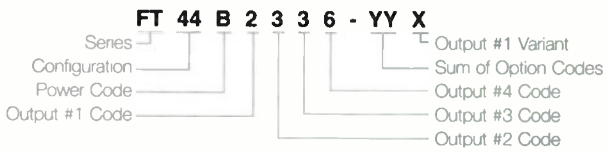
Output Types*						
Output		Module Type				
Code	Volts	J Amps	K Amps	L Amps	M Amps	N/P Amps
0	2	10	20	30	100	60
1	3.3	10	20	30	100	60
2	5	10	20	30	100	60
3	12	6	12	24	42	42
4	15	5	10	20	33	33
5	18	4	8	16	28	28
6	24	3	6	12	21	21
7	28	2.5	5	10	18	18
8	36	2	4	8	14	14
9	48	1.5	3	6	10	10
A	2.2	10	20	30	100	60
B	2.4	10	20	30	100	60
C	2.7	10	20	30	100	60
D	3	10	20	30	100	60
E	3.6	10	20	30	100	60
F	4	10	20	30	100	60
G	4.5	10	20	30	100	60
H	5.7	10	20	30	90	60
J	6.3	10	20	30	80	60
K	7	9	18	30	70	60
L	8	8	16	30	62	60
M	9	8	15	30	56	56
N	10	7	14	30	50	50
P	11	7	13	27	45	45
Q	13.5	6	11	22	37	37
R	17	5	9	18	30	30
S	19	4	8	16	26	26
T	21	4	7	14	24	24
U	23	4	7	13	22	22
V	26	3	6	12	19	19
W	29	3	5	10	17	17
X	32	2	5	9	16	16
Y	40	2	4	8	13	13
Z	44	2	4	7	12	12

Multiple output modules of a given type are arranged in ascending order by voltage magnitude in the same sense as the output number sequence in the configuration diagrams.
**Shaded ratings are stock.*

HOW TO ORDER

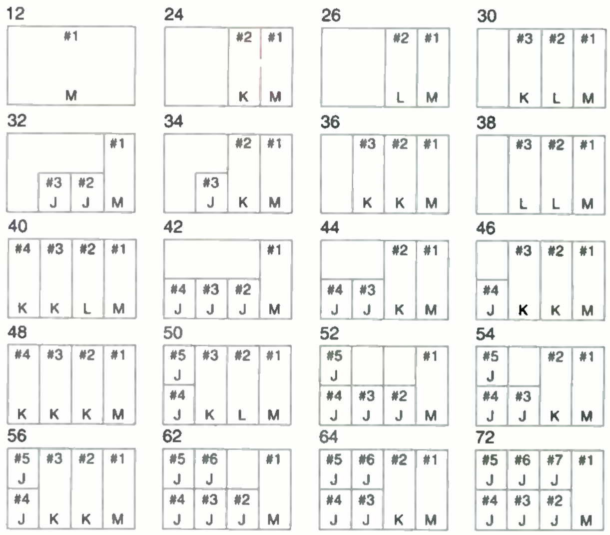
To form the proper model number defining a custom requirement, select the letters FS or FT to designate the series, then choose the desired configuration and list the configuration code. Insert the power code letter for the power level and follow with the output code numbers or letters for each specific output. Enter a dash and from the option table insert the sum of the option codes. Where lower power is desired for the main module, an N module can be substituted and is denoted by a letter N in the output variant position. In addition, when no preload is available for the main output, choose Option Code 08 and add a P in the output variant position. For an enhanced **main** and **current** limited auxiliaries, specify both 04 and 16 option codes.

HARMONIC CORRECTED 500W QUAD SWITCHER



OUTPUT CONFIGURATIONS

The boxes below are diagrammatic representations of the power supplies as viewed from the output end. The two-digit numbers above the boxes are the configuration codes.



Refer to the table below for allowable configurations by series.

Output Config	Unit Power Rating				
	400W	500W	600W	750W	1000W
12	•	•	• X	• X	X
24	•			• X	
26		•	• X	• X	X
30					X
32	•			• X	
34	•	•	• X	• X	
36	•	•	• X	• X	X
38					X
40					X
42	•	•	• X	• X	
44	•	•	• X	• X	X
46		•	• X	• X	X
48			X		X
50					X
52	•	•	• X	• X	X
54		•	• X	• X	X
56			X		X
62		•	• X	• X	X
64			X		X
72			X		X

• Represents allowable configurations for the FT Series.
x Represents allowable configurations for the FS Series.

SPECIFICATIONS

INPUT
90-264 VAC, 47-63 Hz.

POWER FACTOR
0.99 typical.

EMISSIONS
FCC 20780 Part 15/EN 55022, Class A Conducted. EN 61000-3-2, Harmonics. EN 61000-3-3, Voltage Fluctuations.

IMMUNITY
IEC 1000-4-2/EN 61000-4-2, Electrostatic Discharge. IEC 1000-4-3/EN 61000-4-3, Radiated Field. IEC 1000-4-4/EN 61000-4-4, Electrical Fast Transients. IEC 1000-4-5/EN 61000-4-5, Level 3 Surge. IEC 1000-4-6/EN 61000-4-6, Conducted Field.

INPUT SURGE
230 VAC - 38 amps max. 115 VAC - 19 amps max.

EFFICIENCY
75% typical.

HOLDUP TIME
20 milliseconds from loss of AC power.

OUTPUTS
See model selection table. Outputs are trim adjustable ±5%.

OUTPUT POLARITY
All outputs are floating from chassis and each other and can be referenced to each other or ground as required.

LINE REGULATION
Less than ±0.1% or ±5mV for input changes from nominal to min. or max. rated values.

LOAD REGULATION
±0.2% or ±10mV for load changes from 50% to 0% or 100% of max. rated values.

MINIMUM LOAD
Main output requires a 10% minimum load for full output from auxiliaries. Use Option 08 if no minimum load is available for mains up to 500 watts. Singles require no minimum load.

RIPPLE & NOISE
1% or 100 mV, pk.-pk., 20 MHz bandwidth.

OPERATING TEMPERATURE
0-70°C. Derate 2.5%/°C above 50°C.

COOLING
A min. of 10 LFS* for models without internal fans directed over the unit for full rating. Two test locations on chassis rated for max. temperature of 90°C. 600 watt, 750 watt and 1000 watt models have built-in ball bearing fans.
*Linear feet/second.

TEMPERATURE COEFFICIENT
±0.02%/°C.

DYNAMIC RESPONSE
Peak transient less than ±2% or ±200 mV for step load change from 75% to 50% or 100% max. ratings.

RECOVERY TIME
Recovery within 1%. Main output - 200 microseconds. Auxiliary outputs - 500 microseconds.

SAFETY
Units meet UL 1950, CSA 22.2 No. 950, EN 60 950, IEC 950.

ISOLATION
Conforms to safety agency standards.

INPUT UNDERVOLTAGE
Protects against damage for undervoltage operation.

SOFT START
Units have soft start feature to protect critical components.

OVERVOLTAGE PROTECTION
Standard on all outputs.

REVERSE VOLTAGE PROTECTION
All outputs are protected up to load ratings.

OVERLOAD & SHORT CIRCUIT
Outputs protected by duty cycle current foldback circuit with automatic recovery. Standard auxiliaries have additional back-up fuse protection. Options 04 and 16 have square current limiting with automatic recovery when overload is removed.

THERMAL SHUTDOWN
Circuit cuts off supply in case of local over temperature. Units reset automatically when temperature returns to normal.

FAN OUTPUT
Nominal 12 VDC @ 12 watts maximum.

INHIBIT
TTL compatible system inhibit provided. Option 16 has individual output inhibit.

REMOTE SENSING
On all outputs except standard and 04 Option outputs 75 watts or less.

SHOCK & VIBRATION
Shock per MIL-STD 810-E Method 516.4, Procedure I. Vibration per MIL-STD 810-E Method 514.4, Category 1, Procedure I.

MECHANICAL

CASE	SERIES	WATTS	H	x	W	x	L
1	FT	400W/500W	2.50"	x	4.93"	x	8.00"
3	FT	600W	2.56"	x	5.08"	x	10.03"
4	FS	600W	2.56"	x	5.08"	x	11.00"
5	FT	750W	2.63"	x	5.20"	x	10.03"
6	FS	750W	2.63"	x	5.20"	x	11.63"
7	FS	1000W	2.56"	x	7.13"	x	11.63"

OPTIONS

POWER FAIL MONITOR
Optional circuit provides isolated TTL and VME/VXI compatible ACFAIL signal providing 4 milliseconds warning before main output drops by 5% after an input failure. A SYSRESET signal following VME timing requirements is provided when an N module is used as a main output. Both logic signal outputs can sink current per the VME specification.

REDUNDANCY
Optional Or-ing diodes for hot pluggable N+1 redundant operation. For FT Series 500 watt & 750 watt models with 1-4 outputs. Main output current limited to 100 amps. Remaining outputs 16 amps max.

CURRENT LIMIT
Option provides on all outputs:
- Square current limit with auto recovery.
- Wireless droop current share for parallel or N+1 redundant operation.

ZERO PRELOAD
Optional circuit removes need for preload on main output up to 500 watts.

ENHANCED
Option provides on all outputs:
- Square current limit with auto recovery.
- Single wire active current share for parallel or N+1 redundant operation.
- DC output good logic signal with LED indicator.
- Logic inhibit.
- Nominal 5V bias.
- Margining.

END FAN COVER
Optional cover with brushless DC ball bearing end fan which provides the required air flow for full rating.

TOP FAN COVER
Same as above with fan cover mounted on top of the power supply.

ACCESSORIES
RA50 and RA75 Series 2U high rack assemblies provide hot pluggable interface and hold up to 3 FT Series 500 watt or 750 watt units respectively.

Specifications subject to change without notice.

Deltron inc. POWER PRODUCTS
290 WISSAHICKON AVENUE, P.O. BOX 1369, NORTH WALES, PA 19454
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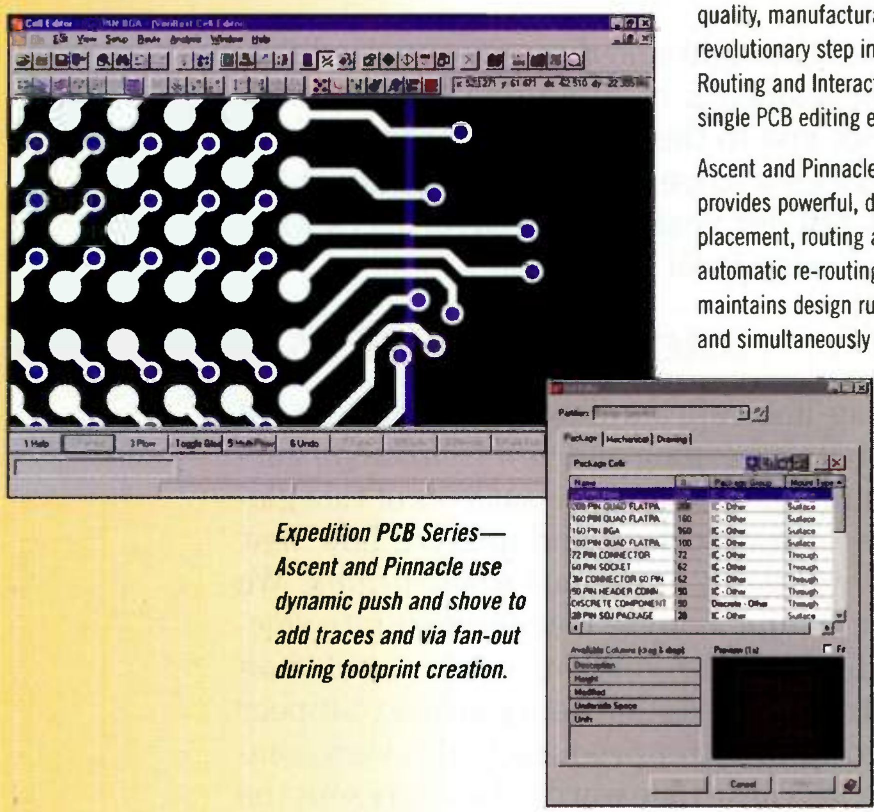

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EDA WATCH

Verilog-A/AMS Extends Design Beyond The Digital Realm

The Open Verilog International (OVI) organization, Los Gatos, Calif., will soon release the first draft of a Verilog-AMS Language Reference Manual (LRM) that defines a behavioral language for analog and mixed-signal systems. The Verilog-AMS HDL (High-Level Design Language) is derived from the IEEE 1364 Verilog HDL Specification. It will cover the definition and semantics of Verilog-AMS HDL as proposed by OVI.

While the initial focus for the OVI technical committee was on Verilog-A, the LRM specific to Verilog-A has now become a subset of Verilog-AMS, and now ceases to exist as a separate entity. Because Verilog-AMS is still emerging, simulators available are based upon the Verilog-A LRM, although several companies have been developing with reference to the latest, emerging Verilog-AMS specification.

Verilog-AMS HDL's intent is to let analog, mixed-signal systems, and IC designers create and use modules that encapsulate high-level behavioral descriptions, as well as structural descriptions of systems and components. In fact, this is one of Verilog-AMS' prime benefits : its ability to enable designers to use various levels of abstraction throughout the design, from architectural study to physical implementation.

The behavior of each module can be described mathematically in terms of its terminals and external parameters applied to the module. Each component's structure can be described in terms of interconnected subcomponents. These descriptions can be used in many disciplines such as electrical, mechanical, fluid dynamics, and thermodynamics. Consequently, a mixed-technology representation, say one with mechanical and electrical functions, is possible *(see the figure)*.

The OVI technical subcommittee is presently editing version 1.2 of the LRM, with plans to deliver the draft to the OVI board of directors for approval sometime before the end of this year. Another technical subcommittee is defining extensions to the Programming Language Interface (PLI) to handle tasks specific to analog. The Verilog PLI provides a set of interface routines to read and write to internal data representation, and extract information about the simulation environment.

Previously, the working LRM had been available on the OVI web site. Although this has made the document readily available, it provided no indication of how many copies were downloaded, where they were, or even if the

Finding The Help You Need

By all accounts, adding the Verilog-A/AMS language to current design flows will be relatively easy. Because the legacy of existing digital and analog models are maintained along with the investment in support tools and training materials, users with access to Verilog and its new extensions will be able to learn to use them gradually. Aiding in this process will be support from several software tool suppliers who are now offering Verilog-A-compliant simulators. But arguably, some designers may need a little extra help to get them up and running with the Verilog-A/AMS language. If you happen to fall into that category, don't despair. There are a number of resources just right for you.

Primarily, there are several white papers, reviews in journals, and conference proceedings from the Design Automation Conference, International Verilog Conference, Mixed Signal Applications Conference, and *Analog Integrated Circuits and Signal Processing* journal (published by Kluwer Academic Publishers).

Cadence's Ken Kundert authored an informative paper, entitled "Modeling and Simulation of Jitter in Phase-Locked Loops," in an issue of *Analog Circuit Design* published by Kluwer Academic Publishers in 1997. In the paper, he presents Verilog-A models that include jitter effects, and reviews a frequency divider, phase-frequency detector and charge pump, fixed-frequency oscillator, voltage-controlled oscillator, and a differential voltage-controlled oscillator.

Apteq's Dan Fitzpatrick and Ira Miller, senior technical staff member of Motorola, Chandler, Ariz., co-authored a text on "Analog Behavioral Modeling with the Verilog-A Language," that covers the basics of Verilog-A. It is now available, and comes with a disk that contains a limited version of a Verilog-A simulator. It may be purchased from Kluwer Academic Publishers, or from various book distributors such as Amazon.com. The material in the text provides a good starting point for those wishing to familiarize themselves with Verilog-A.

Other information on this topic can be accessed on a number of different web sites. Here is a partial listing of some you might investigate: www.anasift, www.apteq.com, www.cadence.com, www.e2w3.com/ivcconf.html, www.mentorg.com/ams, www.ovi.org, www.prenhall.com, www.tdes.com, and www.wkap.nl.

Companies That Contributed To The Creation, Editing, And Review Of The LRM

Analogy
9205 SW Gemini Drive
Beaverton, OR 97008
(503) 626-9700
www.analogy.com
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CIRCLE 467

latest version was being referenced. As a result, in an attempt to maintain better control of the final version of the Verilog-AMS LRM, it will only be made available directly from OVI *(see "Finding the Help You Need," p. 67)*.

Models Anyone?

Model development and characterization for Verilog-AMS is no less important than what is presently required for digital Verilog or Spice models. But, tools are starting to emerge from software companies that will help the model development process. One of the companies developing modeling tools is Anasift Technology Inc., Fremont, Calif., a provider of analog-centric software tools for circuit analysis, behavior modeling, design optimization, and automation. One of the company's products, Anascope, is a symbolic analysis and macro-modeling tool. The tool works by generating behavioral models that can be used in analog HDLs for high-level simulation.

To further ease the behavioral model development burden, Mentor Graphics recently introduced a library containing 250 models targeted at telecommunication systems development. The library reportedly allows engineering teams to modify model equations to develop variant models at a fraction of the original development time. All models will be compliant with the emerging Verilog-AMS standards.

In addition to its library announcement, Mentor recently disclosed a joint language-development program with Motorola that offers new options for system-on-a-chip (SoC) development. Intended to spur the growth of multi-domain, mixed-signal applications, including electromechanical sensors and RF-communications chips, it will enable engineers to transition away from a traditional, Spice-based analog design methodology to a simpler system-style, top-down approach. The relationship will enable mixed-signal pieces from different behavioral languages to be used together to verify entire designs. As part of the project, the Verilog-AMS technology developed at Motorola will be distributed by Mentor Graphics as part of Mentor's AMS tool solutions.

Cadence Design Systems has been participating in the analog HDL arena for some time now, with its Spectre-HDL. This product supports the emerging Verilog-AMS standard. The online documentation that comes with it contains an extensive library of baseline models to use as is, or as a starting point in new model development.

The baseline product, Spectre, incorporates an advanced Spice-type simulator that supports a wide variety of models such as BISIMv3.3, EKV, and VBIC, with an option for RF circuit simulation. By incorporating different simulation algorithms and analysis, along with the emerging Verilog-AMS standard and the traditional Spice netlist representations, the same simulator can be used at different levels of a design flow. Cadence also offers a language debugger and GUI for Verilog-A.

Apteq Design Systems also delivers model examples with their Verilog-A products. It offers a unique Verilog-A plug-in for Spice, which adds OVI-compliant Verilog-A HDL functionality to an

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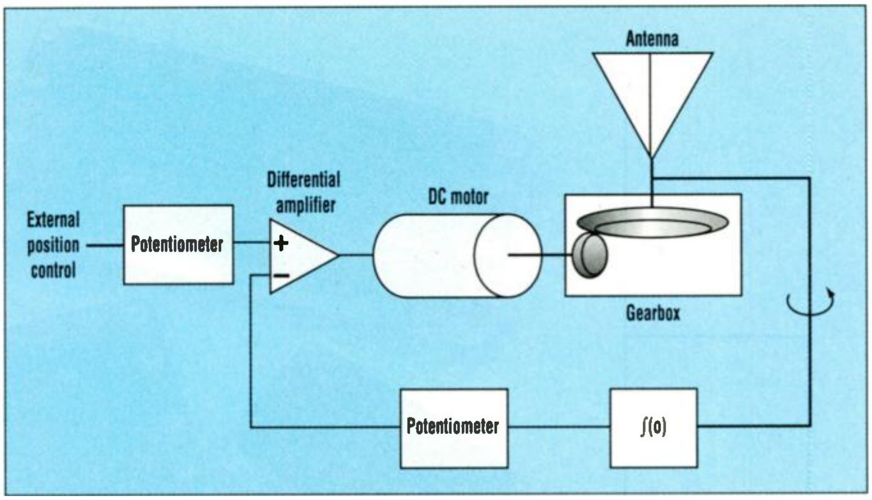


This antenna-position-control system provides one example of a mixed-technology model.

existing Spice simulation environment. The product provides a consistent, high-performance, analog HDL interface to any Spice-class simulator through a unique socket approach, ensuring portable HDL compilation and evaluation across different Spice simulators.

Like the software plug-ins that expand capabilities in an Internet browser, Apteq's Verilog-A Plug-in expands a Spice simulator to support the Verilog-A behavioral modeling language. With the plug-in architecture, you can analyze and simulate Spice device model primitives, as well as Verilog-A behavioral descriptions. The plug-in approach also allows designers to instantiate behavioral Verilog descriptions in standard Spice syntax, thus alleviating the need for learning new tools and languages.

The Verilog-A Plug-in from Apteq integrates easily with all Spice-class (direct method) analog simulators. By using the existing simulator's Spice device model API, the plug-in architecture minimizes integration impact on the Spice circuit simulator. From the user's point of view, this means that moving to Verilog-A doesn't require the purchase of a new analog simulator or transition and training costs. It also allows the reuse of legacy models.

The Verilog-A Plug-in works by compiling the analog behavioral code into an intermediate representation used by the Spice HDL Socket for performing tasks common to other Spice elements, such as instantiation, parameter setting, loading, and evaluation. The plug-in offers options such as analog behavioral code debugging, optimization, and profiling. And, for demanding simulations and full-chip verification and test, the Verilog-A plug-in has an optional second-pass compilation mode to provide high-speed, native-code simulation performance.

Transcendent Design Technology offers a Verilog-A/AMS simulation capability in a product known as TransVerSE. The product is aimed at simulating complex electromechanical systems, and is targeted at a number of different industries including automotive, aircraft, aerospace, and consumer electronics. TransVerSE supports Verilog-A, the emerging Verilog-AMS language, Spice with its models and subcircuits, and models written in C.

Several software tool suppliers to the electronics industry are presently offering simulation capabilities based on the Verilog-A LRM, and are now developing tools based on the emerging Verilog-AMS LRM. This is destined to bring a new dimension to virtual prototyping of mixed technology systems. Early implementation of the specification is providing valuable feedback to the standards process. The results of the OVI Verilog-AMS technical working group will be transferred to an IEEE standards working group in 1999, and will form the basis for work on producing a Verilog-AMS IEEE standard.

Contributed by Ira Miller, senior member of the Technical Staff at Motorola, and chairman of the OVI Verilog-AMS technical subcommittee. His focus is in mixed-signal design and analog behavioral modeling. He holds a BSEE from Michigan State University and a MSEE from the University of Arizona.

EDA WATCH

Using The Analog/Mixed-Signal Virtual Socket Interface To Augment SoC Design

Designing and integrating analog/mixed-signal intellectual property (IP) cores into systems-on-a-chip (SoC) means facing great challenges. Obstacles pop up disguised as advances in process technologies, the consumerization of electronics, and the increasing need for diverse sets of real world interfaces in even the simplest of handheld systems. In response to the global SoC challenge, the industry has embarked on a paradigm shift, fundamentally changing both the technical methodologies and the business practices of IC design. This resulted in the appearance of new IP providers selling a wide gamut of virtual components (VCs), ranging from microprocessor cores to I/O building blocks, including analog/mixed-signal blocks.

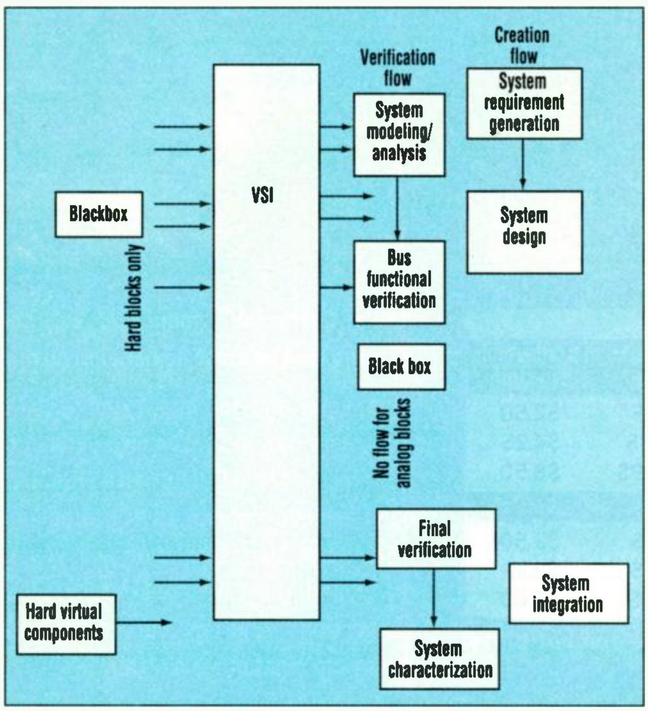
Common analog/mixed-signal blocks today include high-quality audio codecs, video analog-to-digital and digital-to-analog converters (ADCs and DACs), and high-frequency PLLs. Though less commonly sold, VCs that include analog/mixed-signal components such as arrays for digital imaging, sensors, actuators, and RF/IF blocks for SoCs are slowly emerging in the marketplace. Unlike designs of its digital counterpart, analog/mixed-signal VCs require design techniques for noise isolation and high-frequency effects, as well as sensitivity to process parasitics and variation. To produce these circuits process by process and function by function requires intensive handcrafted design efforts.

The Analog/Mixed-Signal VSI Extension, ratified by the Virtual Socket Interface Alliance (VSIA) and released to the public in June (accessible at *www.vsi.org*), addresses an aspect of analog/mixed-signal design issues in SoC. The Virtual Socket Interface Alliance (VSIA) comprises over 180 companies. It's chartered with creating specifications for exchanging IP between provider and integrator. The analog/mixed-signal specification was developed over an 18-month period by VSIA's mixed-signal development working group (DWG), represented by over a dozen companies. The DWG focuses on the additional analog/mixed-signal requirements for analog/mixed-signal VC exchange. One of seven development working groups, the analog/mixed-signal group extends the work of the other groups. Implementation/verification (I/V), system-level design (SLD), manufacturing-related test, on-chip bus, VC transfer, and IP protection are all brought into the analog/mixed-signal domain.

Specification Details

This first specification, Analog/Mixed-Signal VSI Extension, augments the work of the I/V DWG's first specification, "Structural Netlist and Hard VC Physical Data Types," and the VSI Architecture Document v1.0. It provides a comprehensive list of deliverables or specifications to which analog/mixed-signal VC providers should adhere when delivering analog/mixed-signal hard or manufacturing-process-specific VCs for SoC VC integrators. Because analog/mixed-signal VCs are more sensitive to their environment and process than digital blocks, more information needs to be exchanged from the analog/mixed-signal VC provider to the VC integrator to ensure proper integration.

The analog/mixed-signal VSI extension focuses on the hand-off between VC provider and VC integrator, which only occurs at the end of the block design process, i.e. when the layout is complete *(see the figure)*. Soft and firm VCs allow for hand-off prior to layout. But, for hard VCs, designing the VC provider is considered to be a "black box" and is left to the discretion of the VC designer. Similarly, for hard VCs, no intermediate hand-off of soft or firm is allowed. There's no flow for analog/mixed-signal block design in the VC integrator's design process. Ultimately, the methodology used by analog/mixed-signal VC providers to rapidly design high-quality analog/mixed-signal VCs will be what differentiates them in the marketplace.



This diagram illustrates how the Virtual Socket Interface (VSI) can help in the process of handing off information between the virtual-component (VC) provider and the VC integrator.

The VSI Architecture Document v1.0 divides the required deliverables into several sections by data category type. The analog/mixed-signal VSI requires additional information in the user guide, process requirements, test requirements, and physical design sections. For example, in the physical design section, constraints on resistance, capacitance, and/or inductance on analog nets between VC pins and bonding pads can be specified. Typical analog/mixed-signal VC integration will require this information. Table 1 illustrates examples of deliverables in the physical design sections for digital hard VCs. Table 2 depicts examples of analog/mixed-signal extensions to that section. Both tables illustrate the important need for not only specification of the type of information to be delivered, but also the data format in which the informa-

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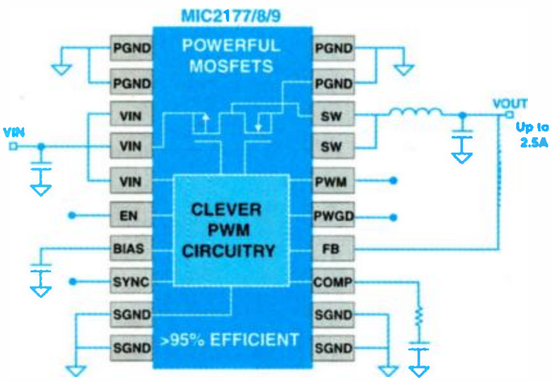

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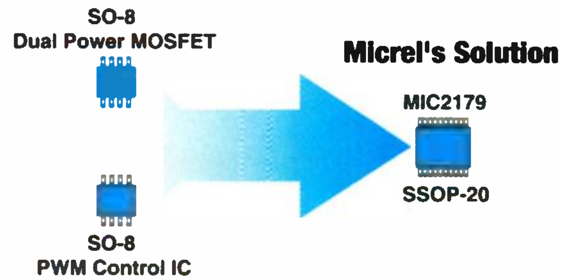

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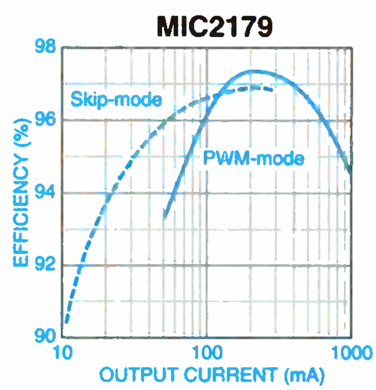

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The Specs

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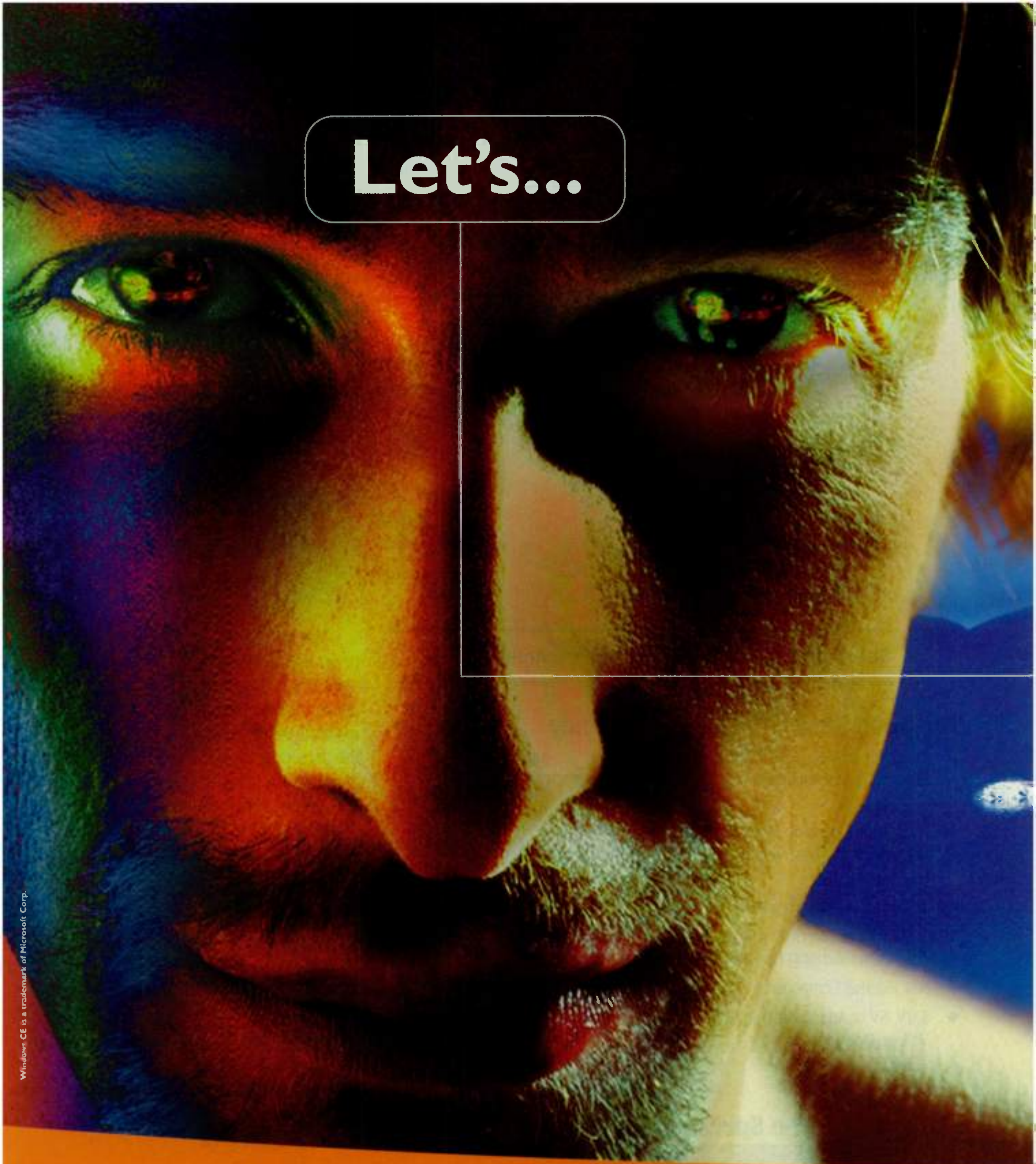

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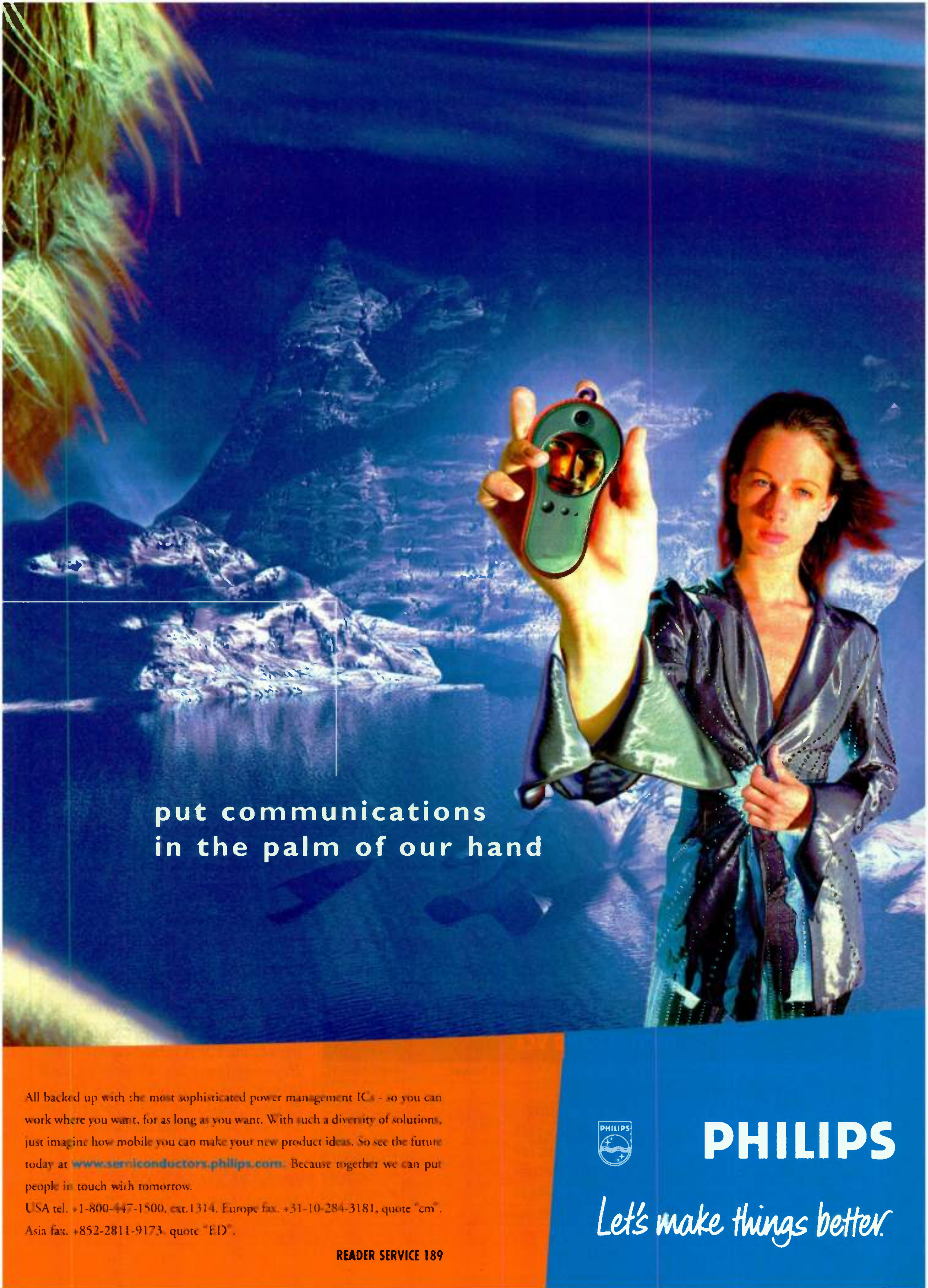
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ing with Tundra's Universe VME-to-PCI bridge. With an incoming transaction on VME, the PCI side of the Universe chip would try to request access to the PCI bus on the board to complete the transaction. At the same time, there's an outgoing transaction coming out of the Triton chip set destined for VME space somewhere else on the backplane.

In this example, the Triton clearly owns the bus, but the Universe can't give it access to the VME side because it's already accepted the initiation of the transaction on that side. But, the Triton will retry until it gains access. Retry protocol in PCI is very well defined and understood. The PCI agent to be retried is supposed to release its bus request. The arbiter takes away the bus grant, and that device is no longer an active agent on the bus. In O'Connor's example, the Triton chip set backs off. But, it never relinquishes the bus through the bus requesting and granting mechanism. That phenomenon is referred to as deadlock.

Livelock happens when both sides back off, but then get into a cycle where the tasks that originated those transactions come back at the same time. They then back off again, and this just goes on and on. The system looks like it's operating and hasn't crashed. Code is still churning, but the system isn't making any forward progress.

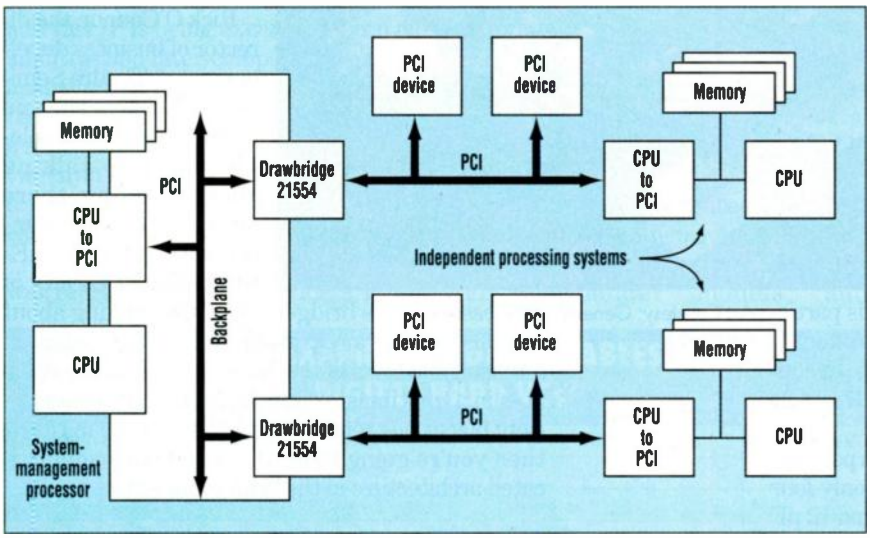
According to O'Connor, handling livelock and deadlock must be done in the overall system architecture, not just the bridging architecture. Worse, some processors don't support retry cycles at all. Once they've dispatched instructions and data into the instruction path in the CPU, it's gone. The processor expects it to be completed.

In some processor environments, there are no hardware hooks to let you deal with this and it has to be done in software. The software has to make sure that the resources required to complete a given transaction are available. It then locks them up in some sort of semaphoring protocol and completes the transaction. That requires software overhead—a must-have in a time-critical or task-completion-critical application.

Bridges For Multiprocessing

If a system is comprised of one Pentium host CPU and a set of dumb peripherals, the standard PCI-to-PCI bridge chips are usually sufficient. But for anything more sophisticated, like multiprocessing or intelligent I/O subsystem architectures, more sophisticated bridging is required.

Digital Semiconductor, now owned by Intel, is for the most part the only game in town for PCI-to-PCI bridge silicon. The company came out with the first PCI-to-PCI bridge in 1994 and now offers a broad family of such chips. Over the last year, the company broke new ground with an embedded PCI-to-PCI bridge chip called the Drawbridge, or 21554 *(Fig. 1)*.



1. Telecom system designers are accustomed to architectures where they can have multiple slave processors and add more processing to the system. Without Drawbridge from Digital Semiconductor (now part of Intel), they haven't been able to do that on PCI. When there's a processor on either side of the bridge, the embedded bridge allows the two processors to communicate with each other and access each other's memory. The two domains could run two separate Windows NT implementations, or even a real-time operating system on one and Windows NT on the other. The bridge serves as a configuration barrier between the various processors.

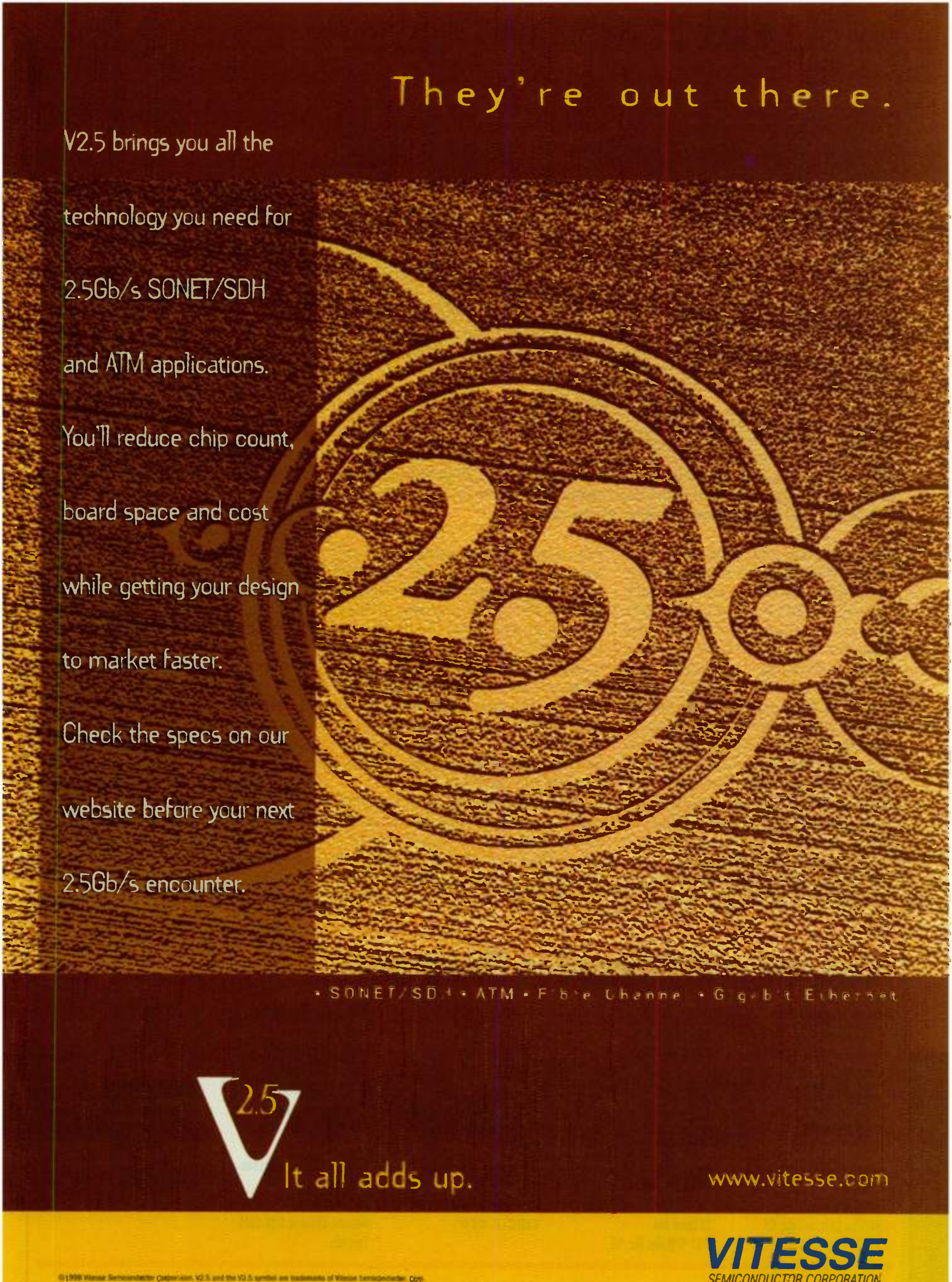
The differences between an embedded PCI bridge and a standard PCI bridge are subtle. Both meet the PCI local bus specification 2.1 (and 2.2 when that's approved). Standard PCI-to-PCI bridges are typically used in applications where you want to add more PCI slots on the motherboard or more PCI devices on an add-in card. In contrast, an embedded PCI bridge is found in applications where there's a host processor located behind the bridge.

Other differences exist. A standard bridge is transparent, which means that a host CPU can see all the PCI devices located behind the bridge. It can control and configure all these devices, and load the necessary drivers for them. An embedded PCI bridge hides everything in the subsystems from the host CPU. "What an embedded bridge does that's unique is it gives you independent PCI clocks, whether you're in the local domain or whether you're in the host domain. It also gives you independent PCI address spaces," says Todd Comins, bridge architect at Intel. "Because you have independent address spaces, you also need the capability to do address translation. The embedded bridge will translate the addresses from the local system to the host system," he adds.

Looks Like One PCI Device

The embedded bridge presents everything that's behind it—everything found in the subsystem—as the same PCI device to the host processor. So, when the host CPU is out polling for PCI devices and it gets to the embedded bridge, it sees everything in the local system as a single device. It will load a single device driver for the subsystem, then be free to go off and do everything else it needs to do. In effect, everything that's in the local subsystem can be controlled and configured exclusively by the local processor. You can open up windows through the embedded bridge to either move data across the bridge or access local memory.

When there's a processor on either



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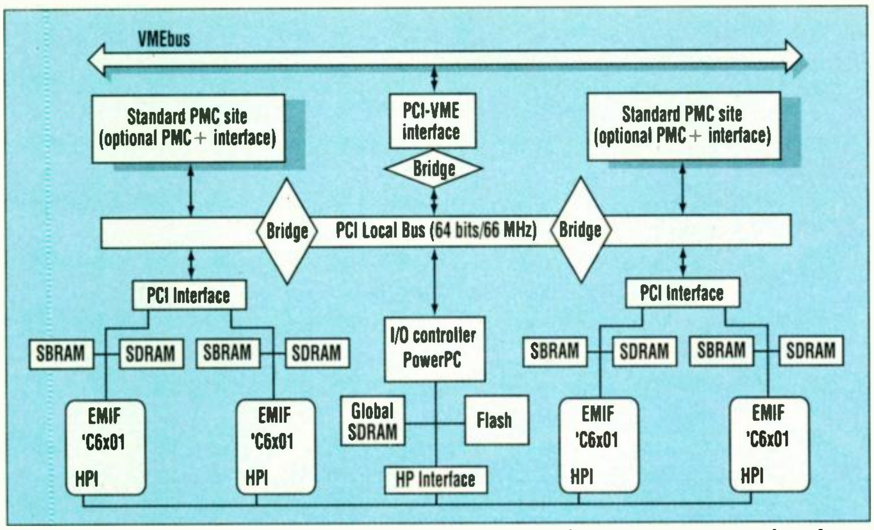

2. DSP board vendor Ixthos uses PCI-to-PCI bridging extensively on its IXC6701 DSP board architecture. Bridging makes the PCI backbone much more applicable to DSP applications. Bridges let them isolate out pieces to get the performance needed. The board use the interfaces for the DSPs to deal with issues of address translation and flexibility.

side of the bridge, the embedded bridge permits the two processors to communicate with each other and access each other's memory. Furthermore, it lets each processor specify what address range it wants to use so the other can access its resources. Between the way that these two separate PCI domains want to be configured and how the resources want to be mapped, there can be conflicts. The value in an embedded PCI bridge, like Drawbridge, is that it can resolve differences between the address maps of these two separate processing domains. You can actually run independent operating systems on these two processor subsystems.

The domain pair could run two separate Windows NT implementations, or even a real-time operating system on one and Windows NT on the other. The bridge serves as a configuration barrier between the various processors. This in particular attracted the interest of CompactPCI board vendors. The key markets for CompactPCI, telecom, and datacom are accustomed to architectures that can have many slave processors, where they can add more processing to the system *(Fig. 1, again)*. Without Drawbridge, they haven't been able do that on PCI.

Intel's Drawbridge chip serves basically two kinds of applications. As described earlier, one application is where there are slave processor cards running an operating system totally independent of the host. The other is an intelligent subsystem, like a RAID controller. In terms of bus requirements, there are a lot of similarities between the two. But, the applications are fairly different.

For the intelligent subsystem applications, one key point is that Drawbridge presents the entire subsystem to the host at a high level of abstraction. Rather than seeing a collection of SCSI controllers, a processor, and a memory array, the host sees a single device with a single PCI address space. It doesn't require any intelligence on the host side to figure out that this collection of components is, in fact, a particular RAID controller.

Configuration Boundary

The higher level of abstraction drives a need to create a configuration boundary between the host domain and the subsystem domain. The Drawbridge creates a configuration boundary where the resources of the subsystem are really hidden from the host. This provides an intelligent processor in the subsystem with much more control and flexibility in terms of how it allocates those resources and assigns them in the address space. It also lets the local processor put resources at a specific address, which otherwise might conflict with an address used by the host.

Drawbridge's address-translation capabilities are important for intelligent I/O subsystem applications. You might use an address range in the top 1 Gbyte of the local address-range space to address the first Gbyte in the host space. To do that, you have to be able to translate between the host and local address

Companies Mentioned In This Report

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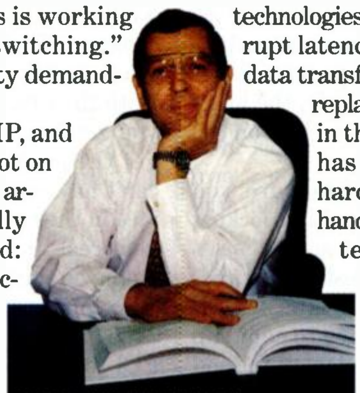
See, I Told You So!

Earlier this year, I wrote a column on "The Death of PCI" predicting the mainstream computing transition to high-speed serial I/O from parallel buses (*ELECTRONIC DESIGN*, June 8, 1998, p. 100). These predictions didn't go unnoticed by the readership of *ELECTRONIC DESIGN*. I received a plethora of letters from everyone but Bob Pease telling me that I was wrong, serial channels could never replace parallel buses, and my predictions were hallucinations. Several of those letters were printed in August, including a few that agreed with me on the move to serial I/O ("A Peak Into Ray's Mailbox," *ELECTRONIC DESIGN*, August 17, 1998, p. 78). Now I can say, "I told you so!"

In early September, Compaq Computer, Hewlett-Packard, and IBM presented Intel with the new PCI-X specification that increases the bus clock frequency to 133 MHz. I haven't seen the spec, so I can't say how they're doing this, or over what distance these lines can run. But clocking a bus over 100 MHz will certainly have its restrictions unless they've figured out a way around the laws of physics, have very few loads on the bus, or started using 200-mA transceivers.

As a rule of thumb, every time you double the clock frequency, you halve the bus-line length. A really good designe could move data on the clock's rising and falling edges. This would give the illusion that you've doubled the clock rate, when you're actually working at the old, 66-MHz frequency. If you take this tack, you don't invoke the wrath of the Gods of Physics immediately.

The PCI-X spec's coming to light caused Intel to play their cards on PCI extension plans earlier than they wanted. They revealed their ideas about extending PCI by tinkering with the transaction protocols to make them more efficient, but leaving the bus clock at 66 MHz. Again, I don't have a copy of the spec, and can't say for sure what they're doing. PCI's original frequency of 33 MHz works with 30-ns clock cycles. At 66 MHz, we're working with 15-ns cycles. If the clock rate is effectively doubled to 133 MHz by moving data on the rising and falling edges of a 66-MHz clock, data is shifted in 7.5-ns cycles. If that's the case, the bus is working with "incident-wave-switching." Such schemes are pretty demanding of the designer.


RAY ALDERMAN

Because Compaq, HP, and IBM have stirred the pot on PCI upgrades for server architectures, Intel finally played its trump card: high-speed serial connections. Surprisingly, Intel did not detail its PCI upgrade plans or gigabit-serial I/O technologies, dubbed NGIO (Next Generation I/O), at the September Intel Developers Conference in Palm Springs, Calif. However, an Intel spokesman stated that, "There's a general recognition that we have to move I/O to a higher plane. We have to get to a more mainframe-like channel-based architecture."

We have to eliminate interrupts, shared buses, and bit-thrashing driver software at the desktop and in servers. Serial connections can do just that. But, if the serial connections use protocols like TCP/IP, the performance moves back into the dismal category, and you're better off with the old bus problems. That's why the serial protocols on NGIO will be a message-passing model. Dealing with the software imperatives of a message-thrashing machine is much easier than drivers for a register-thrashing machine.

But there's more to the story here. What Intel, Compaq, HP, and IBM are saying is that PCI has one last enhancement due before it's relegated to the mainstream technology graveyard. If they can just clean-up the PCI protocols at 66 MHz, and gain some incremental performance benefits over the next two years, then PC and server architectures can move to NGIO by 2000, and we can put this lurid register-oriented past behind us. Like the mainframe "channel" architectures of old, NGIO will change the I/O model from a tightly coupled to a loosely coupled architecture.

Will PCI survive in some form past the year 2000? Probably. But, it will be a niche technology, used in industrial controls and other applications where the tightly-coupled I/O model makes sense. Other buses have survived as niche technologies. With PCI's high-interrupt latency and fast burst-mode data transfer, it stands a chance of replacing the older PC buses in the long run. But no bus has ever replaced VME's hard, real-time interrupt-handling capability. With Intel's move to NGIO, I doubt we'll see another interrupt-driven backplane or local bus in the mainstream markets.

So, the future of parallel buses boils-down to VME for hard real-time, interrupt-driven applications, and some incarnation of PCI for soft, real-time tasks that need efficient, burst-mode data transfers. Depending on the speeds of the serial links, NGIO machines could fall right between the two parallel-bus architectures in basic performance measurements. Ultimately, if we can handle an interrupt packet as fast as toggling interrupt lines on a bus, we could then move to a distributed-interrupt, event-handling architecture, like the original concepts developed in the Futurebus work back in the early 1990s.

The Chinese have a proverb that's both a blessing and a curse: "May you live in interesting times." If you're a bus nut like me, these recent events are an opportunity and a blessing. If you're managing a P&L that's dependent on desktop technology at the bus level, then you might see these transitions as a threat and a curse. Either way, we can see that the PCI game is almost over in the PC and server markets, and the NGIO game is just beginning.

For now, it will be business as usual in the PCI board and chip markets. Once we know the speeds and the pricing of gigabit NGIO silicon, there could be a wholesale move to serial I/O in PCs and servers. After that, NGIO could spill into the burgeoning embedded computer and bus-board markets. If there's a split in the PCI camp, and two incompatible versions are running around out there, I predict NGIO will be mainstream technology much faster than anyone expects.

Ray Alderman is the executive director at VITA. He can be reached at exec@vita.com.

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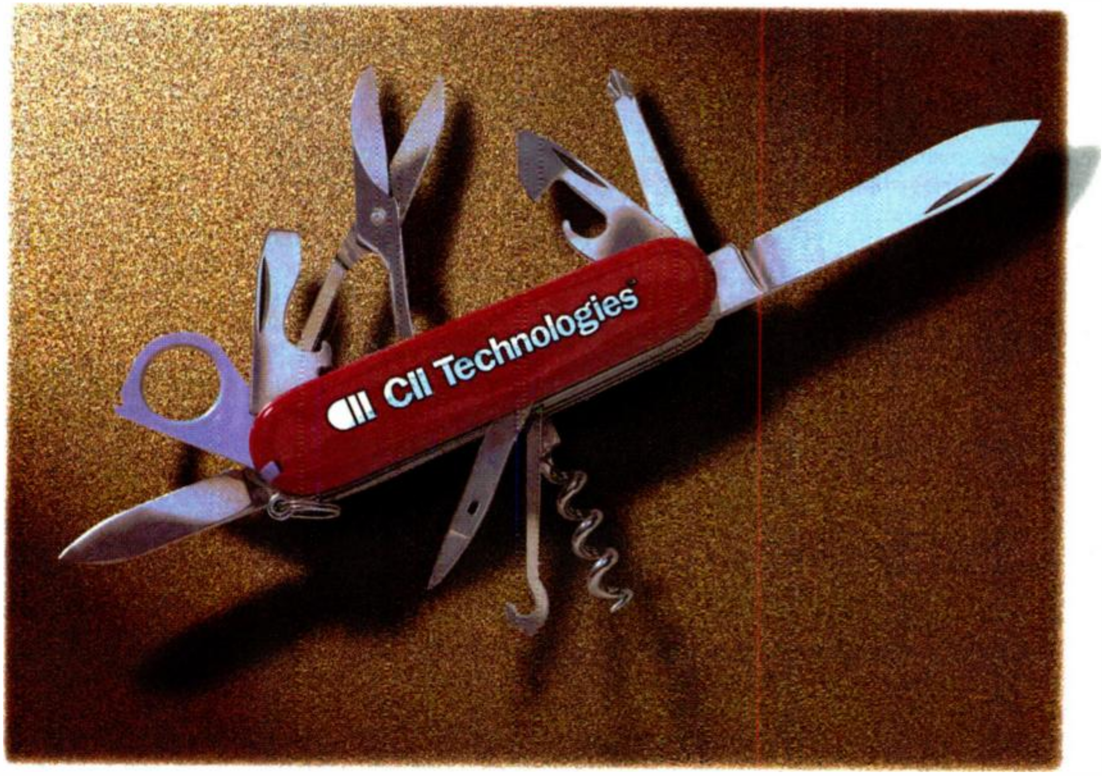

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WHAT'S ON BOARD

Close to sampling, the MB86290 Marquis 2000 2D/3D graphics engine from Fujitsu Microelectronics Inc., San Jose, Calif., has most of the features called out by the Microsoft Talisman specification: a floating-point triangle setup engine, single-cycle trilinear filtering, 32-bit color rendering, motion compensation for full-screen DVD playback, a triple 10-bit RAMDAC, and a 2X-AGP interface with sideband signaling. Optimized for Direct3D and DirectX 6.0, it can render to multiple target surfaces using a compositing engine that delivers data at two pixels/clock. For 3D operations, it supports anisotropic texture filtering, multiple textures, reflection and environment mapping, shadows, motion blurs, lens flare, and per-pixel range-based fog. Able to address 16 Mbytes of SDRAM or SGRAM, the IC has a 128-bit external memory interface. Its triple 10-bit RAMDAC operates up to 250 MHz and supports resolutions up to 1600 by 1200 pixels at 85 Hz. Features include full-scene anti-aliasing and the ability to deliver megapixel rendering of full-featured pixels. A "chunking" sprite compression/decompression architecture accelerates graphics rendering by eliminating the need to recomposite an entire image when parts of a scene change. The IC can drive two monitors and deliver NTSC or PAL TV outputs. Available in early 1999, it will be housed in a 432-contact BGA, operate from a 2.5-V core supply and have 3.3-V-tolerant I/O lines. Contact Rick Humphrey at (408) 922-9772, or at www.fujitsumicro.com.

A full development environment for the forthcoming IA-64 "Merced" processor, in the works at Intel Corp., Santa Clara, Calif., and Hewlett-Packard Co., Palo Alto, Calif., will allow software predevelopment for the IA-64 architecture. The Intel environment includes compilers, debuggers, libraries, performance-tuning software, and various languages. Running on an IA-32 Unix or Windows NT platform with 128 Mbytes of RAM, it will permit designers to develop application software and leverage hardware, such as I_2O boards and PCI cards, that can plug into the IA-32 platform. IA-32 applications execute completely unmodified, letting all existing applications run, and can be recompiled, to leverage the 64-bit architecture and features like speculative execution and predication, as well as other enhancements that speed up application execution. In development are 64-bit operating systems, key device drivers, and APIs to permit systems to power-up in late 1999. I_2O subsystems and drivers are already compatible with the IA-64. Plus, emulation software lets PCI devices plug in and look like IA-64 devices. The software environment handles multiprocessor simulation and the ability to simulate the entire platform. It also develops and exercises device drivers and BIOS software. Designers can thus work out many system issues and optimize software before hardware is available. The Merced will offer software development aids like event address registers to improve monitoring accuracy for branch mispredicts, cache misses, and TLB miss events; an opcode matcher to focus on specific instructions and monitor speculative or predicated instructions; and both data and instruction address range checking for blocks of code or specific data structures. Contact Intel at http://support.intel.com/newsgroups/developers.htm.

A full 340-Mbyte disk drive compressed into a space of 42.8 by 36.4 by 5 mm, features the most compact and high-density mechanical storage to date. Developed by IBM Corp., San Jose, Calif., the MicroDrive sets a new compact-flash socket standard—a Type II package with the same length and width of the standard Type I package, but 5 mm thick instead of the Type I's 3.3 mm. Targeted at portable systems like digital cameras, PDAs, and battery-powered systems, the MicroDrive will sample in the first half of 1999 in 170- and 340-Mbyte options. The drive has a giant magnetoresistive (GMR) recording head and a glass disk substrate with a 3000 Oersted magnetic coating. Raw data transfer rates off the R/W head are 35 to 42 Mbit/s. A 128-kbyte buffer is one of four chips that perform all drive operations. The three other chips include a hard-disk controller/data processor, a R/W channel chip, and an analog chip for spindle and other motion-control circuits. A shock sensor also is included on the circuit board. Drive prices have yet to be established. Contact Michelle McIntyre at (408) 256-7589.

VME Boards Offer Application-Centered DSP Solutions

Defense, intelligence and surveillance, wireless communications, and wireline telecommunications are some of the largest and most promising emerging markets for DSP-based systems. Blue Wave Systems is attacking those markets with a new family of VME DSP boards.

The family consists of three separate products, the VME/C6450 *(see the photo)*, VME/C6420, and VME/C6400. Each product has been carefully tuned to meet the unique requirements of a specific vertical market application type. The VME/C6450 is targeted toward high-performance, multiprocessing applications typical in defense and high-end image processing.

The VME/C6420 offers scalibility and high-bandwidth data throughput essential in wireless communications and surveillance applications. The cost-effective VME/C6400 completes the family and is ideal for channelized wireline communications applications requiring standard telecom interfaces.

The VME/C6450, provides up to 4 GFLOPS/ 6400 MIPS from four TMS320C6000 DSPs. A crossbar sits at the heart of the board and acts as a high-speed switch providing a fully interconnected solution. The VME/C6420 is targeted at wireless applications and is fully compatible with the SoftBand Software Radio product line.

The final product in the family is the VME/C6400. The VME/C6400 is a quad processor board with a channelized architecture and is designed for wireline telecommunication applications such as transcoding and echo cancellation. The VME/C6000 board family is priced from $7000 in single quantities.

***Blue Wave Systems Inc.**, 2410 Luna Rd., Suite 132, Carrollton, TX, 75006; (972) 277 4600; fax (972) 277 4666; www.bluews.com.* **CIRCLE 554**


20.1"
18.1"
15"
15"
15"
14.1"
14.1"
14.1"

Take your pick of LCD screens for monitors

LCD monitors are springing up all over the corporate environment. With their brilliant colors, space-saving design, energy-efficient operation and contemporary styling, LCD monitors are uprooting CRTs in a wide range of office, factory and POS applications.

Since monitor applications require screens with a variety of interface, resolution, size and color capability, our LCD lineup includes ten different models. NEC is the only vendor who offers both analog- and digital-interface models. We've recently expanded our analog line with new 18.1" and 15.4" models. Featuring full color display, our analog lineup now includes seven screens in sizes ranging from 14.1" to 20.1."

Our analog-interface screens make it easy to design standalone LCD monitors that offer full compatibility with CRT monitors. They help designers simplify circuitry and shrink system size because they require no A/D conversion and complex image data processing. To slash your development time and costs, interface boards compatible with CRT monitors are available as an option.

Digital-interface models are the optimum solution for desktop PCs with an integrated LCD screen. They're also the first choice for many industrial applications. All our digital screens offer a low-voltage differential signaling interface (LVDS) and display 262,144 colors.

Whatever your requirements for monitors, we have an LCD screen that can make you look your best. For more information, contact NEC today.

Size	Resolution	Viewing angle	Model
Analog-interface models (Full color)			
20.1"		Ultra-wide	NL128102AC31-01
18.1"	1280 x 1024	Ultra-wide	NL128102AC28-01 (NEW)
15.4"			NL128102AC23-01 (NEW)
15"		Ultra-wide	NL10276AC30-01
15"	1024 x 768	Wide	NL10276AC30-03
14.1"		Ultra-wide	NL10276AC28-02
14.1"			NL10276AC28-01
Digital-interface models (262,144 colors)			
15"		Ultra-wide	NL10276AC30-02
15"	1024 x 768	Wide	NL10276AC30-04
14.1"			NL10276AC28-05

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Board Enables Compact PCI Multiprocessing

Conventional CompactPCI processor boards incorporate a transparent CompactPCI bridge that maps on-board PCI addresses directly to CompactPCI bus addresses in one complex memory map. A new Compact PCI board, the MCPN750 has a non-transparent bridge allowing addresses from multiple processor boards to be mapped onto different address spaces on the CompactPCI bus. As a result, a conventional system-slot processor board and multiple MCPN750 processor boards can operate in the same backplane without address conflicts.

MCPN750 boards operate in non-system slots, allowing the configuration of loosely coupled multiprocessor systems. It sports a PowerPC 750 processor. In addition, the board complies with the latest revision of the PICMG Hot-Swap specification, reducing the downtime needed for system repair or upgrade and enabling it to be used in high availability systems.

On-board memory and I/O functions allow the MCPN750 to address a wide range of applications. Up to 128 Mbytes of ECC-protected DRAM, 5 Mbytes of flash memory, 10/100Base-TX Ethernet interface, a USB Host/Hub interface, a real-time clock, and four serial ports are incorporated. An IDE interface allows a CompactFlash memory card to be added to an external transition module. As a result, it provides a convenient and inexpensive boot option.

Two PMC sites make it possible to add PMC modules, which tailor the board to the exact needs of a specific OEM application. Most I/O interfaces are accessible via front-panel or rear connectors making the design of system cabling straightforward. Available today, list price starts from $2095.

***Motorola Computer Group**, 2900 S. Diablo Way, Tempe, AZ 85282; (602)-438-3025; www.mcg.mot.com.*

CIRCLE 560

PC•MIP Mezzanines Roll For Ethernet And SCSI

The emerging PC•MIP mezzanine standard offers the best aspects of PMCs and IndustryPack modules. Products have already started to appear, such as Mikro Elektronik's (MEN's) recent announcement of two new PC•MIP modules.

The P3 is a standard Ethernet interface based on the Ethernet controller DEC DS21041. It supports 10Base-T via a 9-pin D-Sub connector at the front panel. The P3 has a high 2-kV isolation voltage and offers full duplex support. The module comes ready to run with DEC's standard Plug and Play driver for Windows95/WindowsNT.

The next PC•MIP module is the P4, a fast SCSI interface-based on the SCSI controller SYM53C895 by Symbios. It supports Ultra2SCSI up to 40 Mbytes/s in single-ended (Fast SCSI and Ultra SCSI modes), and LVD (Ultra2 SCSI mode) signaling environments, as well as big/little endian. The

(continued on page 92)

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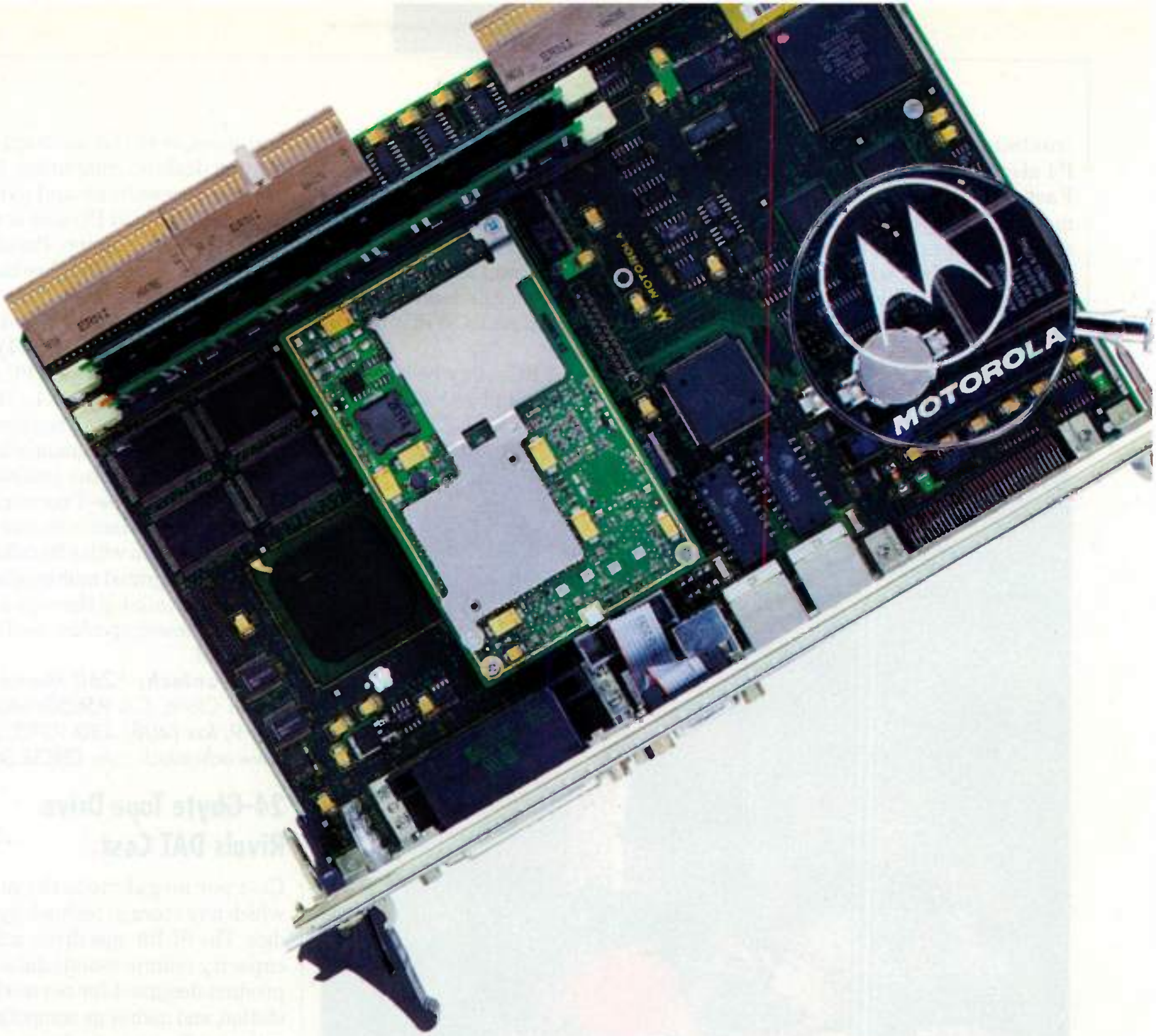

There are hundreds of CompactPCI products. But only one comes from the Leader in Embedded Computing.

You expect more from the leader. At Motorola, we offer more. Like our commitment to quality, life-cycle management, and worldwide service. And that's just the beginning. We offer a broad spectrum of reliable CompactPCI products that will help you get to market faster and more affordably. Our open architecture lets you choose between Pentium, Pentium II or PowerPC processors. From single board computers to low-cost OEM systems to high-end telecom platforms, we have just the product you'd expect from the Leader — Motorola. Give us a call at 1-800-759-1107. Or check out our Web site at www.mcg.mot.com.

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MOTOROLA
Computer Group

READER SERVICE 180

(continued from page 90)
P4 also is backward-compatible to Fast (Wide) and Ultra (Wide) SCSI modes. The module runs with the standard Plug and Play driver for Windows95/WindowsNT by Symbios.

MEN Mikro Elektronik GmbH, *Wiesentalstr. 40; 90419 Nürnberg, Germany; phone 49/911/99335-0; fax 49/911/99335-99; www.men.de.* **CIRCLE 561**

Touchscreen LCD PC Is Thin And Lightweight

If your embedded application needs an LCD, why not embed the computer right into it? Advantech's Panel PC is an entire PC integrated into a 3.67-in.-thick unit, with an LCD display and touchscreen.

The Panel PCs may be used as a desktop or mounted on a wall, swing-arm, panel, or rail for use in applications beyond desktop computing. Offering greater accessibility and portability than a traditional PC and with more durability than a laptop, Panel PCs offer a unique human interface that's easy to install and can fit anywhere.

The Panel PCs are offered as a full product line with 386-, 486-, Pentium-, and Pentium MMX-based PC systems with integrated 5.7-, 10.4-, 12.1-, and 13.8-in. LCD displays. They are fully capable of network communications with an on-board Ethernet interface that supports 10/100Base-T networking.

The user interface is an analog-resistant touchscreen with a 30 million touch lifetime. Integrated multimedia options are made available through a built-in sound processor, speakers,and available CD-ROM.

Advantech, *1260 Memorex Dr., Santa Clara, CA 95050; (408) 330-9399; fax (408) 330-9393; Internet: www.advantech.com.* **CIRCLE 562**

24-Gbyte Tape Drive Rivals DAT Cost

Cost per megabyte is the metric by which any storage technology lives or dies. The SLR6 tape drive, a 24-Gbyte capacity (compressed) data storage product designed for network, workstation, and midrange computing applications, offers a cost edge over identical-capacity digital-audio-tape (DAT) alternative.

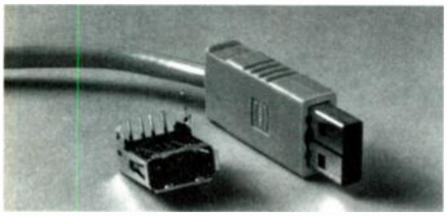
The SLR6 features a 16-bit Fast Wide SCSI-2 interface and is available as an internal bare drive, or as internal or external versions of a complete storage-management solution (internal versions install in a standard 5.25-in. half-height drive bay).

With transfer rates of up to 8.6 Gbytes per hour and 2.4 Mbytes/s (hardware data compression mode), the SLR6 possesses a faster transfer rate than DDS-3 products, as well as superior reliability.

Available immediately, the new SLR6 is priced staring at $1023 for the internal bare drive, $1221 for the internal version of the complete storage management solution, and $1353 for the external version of the package.

Tandberg Data Inc., *2685-A Park Center Dr., Simi Valley, CA 93065; (805) 579-1000; fax: (805) 579-2555; www.tandberg.com.* **CIRCLE 563**

Harting Introduces USB Connector



New HARTING Universal Serial Bus Connector -- Series A and B add a new dimension of flexibility to Desktop/ Notebook PC and a variety of peripheral devices. Single USB port is used for connecting peripheral devices, including those that use serial, parallel, keyboard, mice or game ports. Peripheral devices are connected to the PC through the same connector allowing a reduction of required PC slots. Users will be particularly interested in these features: Plug and Play; Hot Swapping Capabilities; Computer / telephony integration: and Port consolidation. HARTING's new units permit transfer rates up to 12 Mb / s and support up to127 devices. The USB has subchannel for 1.5 Mb / s signaling and allows daisy chaining of peripheral devices. Up to 5m per cable segment, Isochronus and Asynchronous data transfer and built-in power distribution for low power devices are important specifications.

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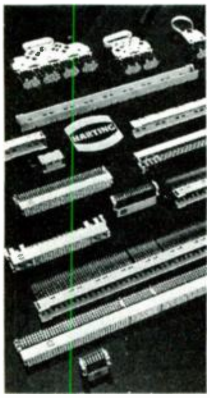


har-pak® 2.5mm Connector System...

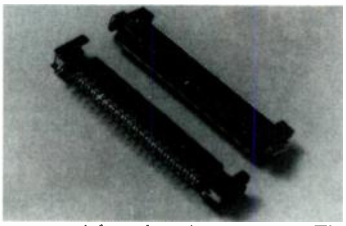
High Density, Board To Board, Analog Coax Solution

HARTING's micro coaxial connector system can provide more than twice the number of contacts in the same board space of typical SMA or DIN connector styles. The coax system can increase the quantity of high speed analog signal density and save space on your PCB. The HARTING ***har-pak®*** coax and signal connector systems are robust and have densities reaching 35 pins per inch. The larger 2.5 mm contact spacing improves crosstalk and high frequency performance. The ***har-pak®*** system is made for high volume applications with SMD compatibility and reliable solderless compliant pin terminations for both signal and coax applications. The ***har-pak®*** connector systems can provide a competitive advantage to increase your system performance, reduce manufacturing cost, and increase system reliability.

READER SERVICE 197

HARTING Introduces SCA-2 Connectors for Storage Devices

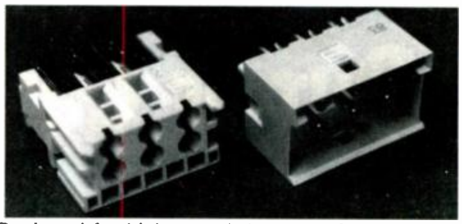
The new SCA-2 connectors serve as the only means of electrically attaching a small form factor hard disk drive. Available with 40 and 80 contact positions for fiber channel and SCSI drives respectively. Connectors contain make-first / break-last contacts that enable users to "hot-swap" storage devices without taking the entire storage unit off-line. Blind mating is accomplished through a pair of guideposts on the plug connector that have a generous lead-in and are equipped with grounding contacts. The plug ground contacts mate with a pair of ground contacts on the receptacle before any other electrical connection is made thus protecting the storage device from electrostatic discharge. Final alignment is performed by the "D" shape of the mating connector bodies. Highly reliable bellows style contacts



are used for signal contacts. The plastic connector housings are made of high temperature thermoplastic for surface mount compatibility.

READER SERVICE 198

New High Density Micro-Coaxial Contacts



Designed for high speed data transfer rates. Can be used in the iec 1076-4-2 2.5mm High Density connector system, *har-pak*® Provides more space efficiency, high frequency capability, easy handling, low applied cost and application with current equipment and emerging metric equipment practices. Designed for PCB termination on both daughter card to backplane connection; allowing users to bring signal directly into the backplane without cable transition.

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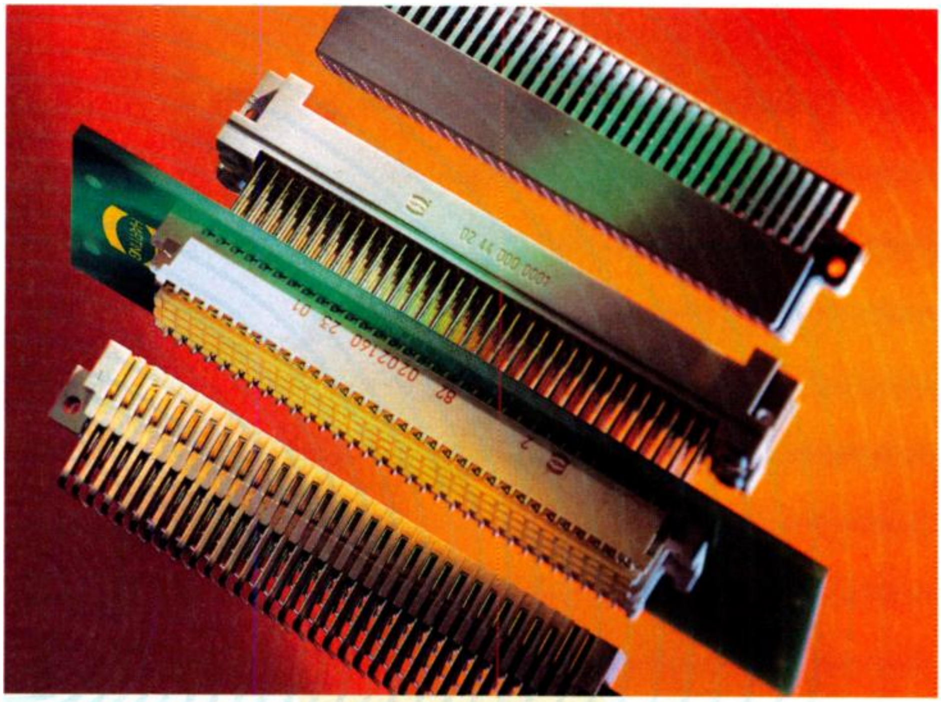
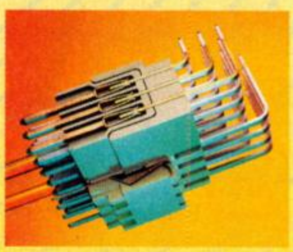




main parameter that determines if a lumped-load or a transmission-line model should be used. If the edge rates are slow, then the cards inserted into the backplane may be treated as one lumped load, since the transmission-line effects (reflections) that occur will die out in a short period of time compared to the signal's pulse width (unit interval). This gives sufficient time for the signal to settle out into a stable state before sampling occurs.

A general guideline is to compare the unit interval to six flight times (or to three round trips). A flight time is the electrical length of the backplane; in other words, it is the time it takes the signal to travel from one end of the backplane to the other. A round trip is simply two flight times. Six flight times should be less than 30% of the unit interval to generate a stable state at the 50% point.

Another way to avoid transmission-line problems is through the use of specially designed trapezoidal drivers such as the DS3862 Octal bus transceiver. These drivers feature slow edge rates which are greater than the electrical length of the backplane; thus, the backplane can again be modeled as a lumped load.

A common TTL backplane driver (F245 Octal bus transceiver) driving a 21-slot unloaded backplane is shown *(Fig. 1)*. Transmission-line problems are evident. The waveforms show overshoot, undershoot, and reflections. However, at a relatively low speed (1 MHz), these problems may be ignored because the unit interval is very large and settle out relatively quickly, but can cause other system issues such as EMI (because of overshoot and undershoot, and ringing). As the unit interval is decreased (20 MHz), the width of valid sample area also is decreased. Now the transmission-line effects take up a significant portion of the unit interval.

The second model is for higher-speed applications (>33 MHz) in which the backplane must be treated as a transmission line. If incident-wave switching is desired and the round-trip delay is greater than the edge rate (rise time) of the signal, then you have a transmission line. The simple, lumped-capacitance model no longer applies, and now a distributed model must be used. Incident-wave switching is generally desired at higher data rates.

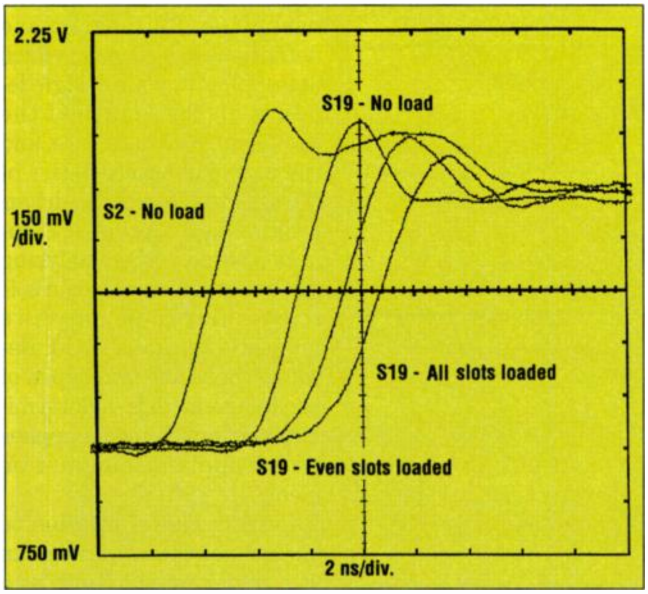
Such switching requires a clean signal environment to allow the receivers to properly detect the correct state as the signal travels down the backplane. There is not enough time to wait for reflections to step up the voltage, as the pulse widths are very short. For these reasons, a properly terminated bus is very important, as it will prevent the generation of undesired reflections. If you are not sure which model to apply, treat the system as a transmission line.

The first step in working with the high-speed model is to calculate the true bus (loaded backplane) impedance. The bus impedance is not the generic pc-board impedance. The generic impedance is a function of the stripline layout dimensions and the dielectric insulation and is typically in the range of 40 to 60 Ω. This impedance can be verified with a TDR when all cards are removed, but the real system has cards installed that add capacitance, and this alters the impedance of the backplane. The net result is that the fully loaded impedance will be lower than the "unloaded" impedance. This loaded characteristic impedance of the backplane, termed Z_L, is calculated by the following equation:

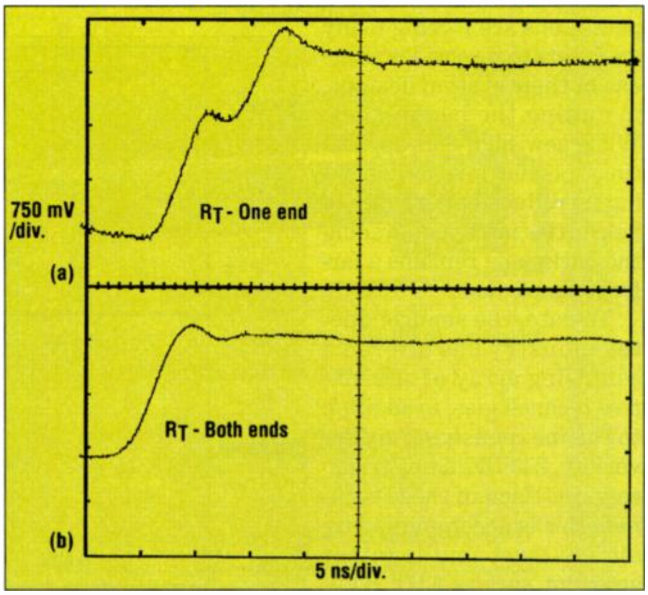
$$Z_L = Z_0 / \sqrt{1 + C_L / C_0}$$

where:

$$Z_L = \sqrt{(L_0 / C_0)}$$



2. A BTL signal was monitored as more cards were added to a 21-slot backplane and two observations were made. First, the flight time increased as cards were added to the backplane. Second, when the backplane was fully loaded the existing terminations were matched to the loaded backplane impedance. Thus, a better termination match was made and the amount of overshoot was far less.



3. Terminating a BTL signal on one end prevents the signal from operating as an incident edge. The reflections from the unterminated end produce a step on the waveform, causing signal-integrity problems such as signal delay, mis-triggering, or double triggering by a clock (a). A signal terminated correctly on both sides does not exhibit this step, which eliminates the problem (b).

Z_L = Impedance of loaded line.

Z_O = Bus characteristic impedance (known).

L_O = Distributed intrinsic inductance per unit length.

C_O = Distributed intrinsic capacitance per unit length (known).

C_L = Distributed load capacitance per unit length (known; includes capacitance of the cards, connectors, vias and output capacitance of the chosen backplane IC).

Knowing the correct loaded impedance is very important, as a mismatched backplane will have major signal-integrity issues, such as negative reflections and undershoot, which may prevent incident-wave switching or overshoot. It also can cause ringing that may lead to EMI problems. These can not be tolerated due to the high speed and small unit intervals required.

The distributed capacitance not only affects the impedance, but it also affects the line propagation delay. The delay is calculated by the equation:

$$t_{PL} = t_{PO}\sqrt{(1 + C_L / C_O)}$$

where:

t_{PO} = Unloaded line delay (propagation delay).

C_O = Distributed intrinsic capacitance per unit length.

C_L = Distributed load capacitance per unit length.

t_{PL} = Loaded line delay.

In addition, a BTL signal was monitored as more cards were added to the backplane *(Fig. 2)*. The delays added to the line are shown to be considerable, and must be added to the overall evaluation of the backplane and used in system timing equations.

To examine this phenomenon, a 21-slot backplane was used. Two of the slots were occupied by termination cards (V_t) which were located at slots 1 and 21 (the two ends of the backplane). A BTL driver was installed in slot 2; no other cards were installed, and the BTL signal was monitored at slots 2 and 19. The observed delay is the time for the signal to travel from slot 2 to slot 19. We then populated the even-numbered slots (4,6,8,...18) and monitored the signal at slot number 19. The result shows that by installing more cards (capacitive load) into the

BACKPLANE DRIVER ALPHABET SOUP

ACRONYM	TECHNOLOGY
ABT:	Advanced biCMOS technology
BTL:	Backplane transceiver logic
ABTE:	Advanced biCMOS technology enchanced
Bus LVDS (BLVDS):	Bus low-voltage differential signaling
CBTL:	CMOS backplane transceiver logic
CMOS:	Complementary metal-oxide semiconductor
ECL:	Emitter coupled logic
ETL:	Enchanced transceiver logic
FAST:	Fairchild advanced Schottky TTL
FACT:	Fairchild advanced CMOS technology
GTL:	Gunning transceiver logic
LCX/LVC:	Low-voltage CMOS
LVT:	Low-voltage technology
LVDS:	Low-voltage differential signaling
TTL:	Transistor-transistor logic
PECL:	Positive emitter-coupled logic

backplane, the flight time for the same signal increases by approximately 2 ns. The fourth waveform is our signal monitored at slot 19 in the backplane with all 19 slots populated.

We observed two points from this evaluation: first, the flight time increased as we added cards to the backplane; second, when the backplane was fully loaded, the existing terminations were matched to the loaded backplane impedance. A better termination match was made and the amount of overshoot was far less.

It is important to remember that as the loading is increased (capacitive load), the resulting f_{MAX} (maximum switching speed) is decreased and the propagation time of the signal (flight time) is increased. This is the challenge presented to the bus driving technologies and the system designer.

Reflections And Terminations

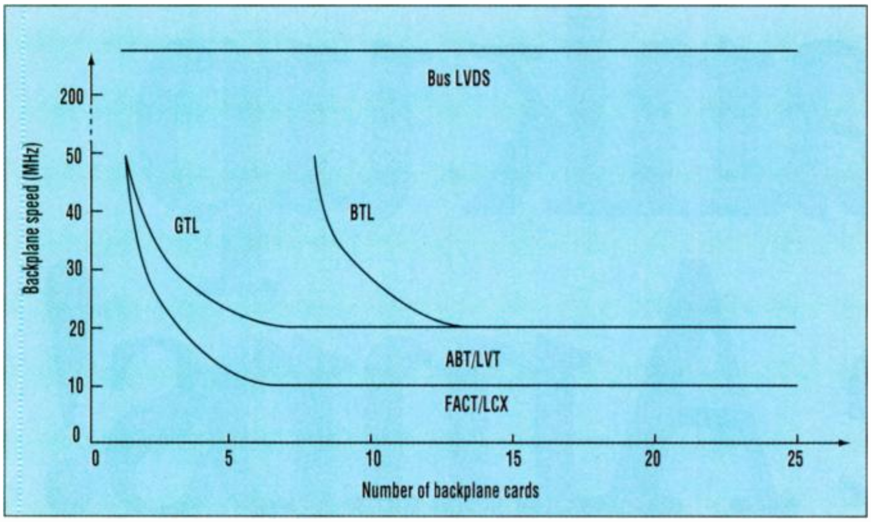
Reflections are caused by mismatched impedance (changes of impedance along the line), which may occur as the result of stubs, board layer changes, or incorrect termination values. If the backplane has been determined to be a transmission line, the use of terminations is typically required. When the signal travels down the backplane and encounters a matched termination $R_T = Z_L$, no reflections occur. This is the best case for signal quality. If the termination is not matched to the backplane's loaded impedance, reflections will occur and degrade signal quality.

Fully loaded, single-ended backplanes typically have a Z_L value of around 30 to 45 Ω as their ac (loaded) impedance. Again, for the matched case, the termination resistor value is equal to Z_L, and the resistors are located at both ends of the backplane.

The effect of terminating a BTL signal on one end only is shown *(Fig. 3a)*. This termination method prevents the signal from operating as an incident edge. The reflections from the unterminated end cause a step on the waveform, causing signal-integrity problems such as signal delay, mistriggering, or double triggering by a clock. Since the waveform is not operating as an incident edge and must wait for reflections to fully change state, it adds to the system's overall delay time.

The step caused by signal reflection occurs within the threshold region; therefore, a clock may trigger at more than one point on a single edge. The waveform of a BTL signal terminated correctly on both sides is also shown *(Fig. 3b)*. The termination value is matched with the loaded backplane's impedance, and thus does not allow reflections; therefore, no additional time delay or false triggering occurs. Note that the dc level is reduced with two terminations, this is due to the driver operating with a larger sink current (I_{OL}).

When low-impedance (30-Ω) termination resistors have been selected,



4. A comparison of backplane performance with respect to loading can only be relative, as the capabilities of the common technologies incorporate a significant degree of overlap. Given enough design and debug time, each technology can be pushed beyond the limits described here.

we also must consider the resulting amount of load current (I_{OL}) that the backplane ICs will have to sink (per channel). The worst case is when driving a backplane with 30-Ω loaded impedance and a signal with a 3-V swing (for example with a F244 device). This will require 200 mA of I_{OL}, but if the signal swing is reduced to 1 V (BTL), the current required decreases to only 67 mA.

Most TTL backplane ICs do not have the required current drive to pull the signal out of their wide threshold area; therefore, they must rely on reflections to change state. This is not the case with BTL, as it supports an 80-mA sink capability, thus providing incident-wave switching. The loaded bus impedance is the reason backplane drivers are required to sink large currents. This must be done while maintaining their V_{OL} ratings to maintain noise margins.

Backplane Driver Technologies

Having determined which backplane model applies, we can start to narrow down the selection of upgrade technologies. In addition to drive capability, other factors such as noise margin, backward compatibility, bus configuration, and live insertion should be considered.

Technologies for driving backplanes have developed along two paths. The first path we will examine improves the overall performance of the system while maintaining standard TTL signaling levels. This may be desired when it has been determined that the chassis (backplane) of a deployed system must remain in service due to capital costs, remaining life, or other infrastructure reasons.

Therefore, of great concern to many system designers is the ability to maintain backward compatibility with previous equipment. This simplifies many facets of system support, especially inventory and maintenance. By maintaining a compatible backplane interface it is possible to allow customers to add new boards to existing systems.

However, mixing boards with higher performance drivers that are compatible with the existing technology into a system will not improve the overall system performance. An example of this is installing a card with FCT drivers into an existing backplane using standard TTL drivers. Only by converting the entire backplane to a new technology will the end user see performance improvements in the system.

These improvements are achieved by decreasing the width of the signal's threshold region and by improving the skew specification. Standard TTL signaling maintains a signal swing of approximately 0.55 to 2.4 V and a wide threshold region from 0.8 to 2.0 V. Most CMOS devices have a wider signal swing, but still maintain the same threshold levels, thereby providing additional noise margin. The 74FCT245T/AT is a good example of this category of device.

Advanced biCMOS technology, or ABT, was introduced to improve on this type of device. While ABT maintains the same threshold region as TTL logic, it specifies a much tighter channel-to-channel skew specification than most TTL/CMOS-compliant families. Typical skew between channels can be up to 5 ns on standard logic families, whereas ABT guarantees a much tighter 2 to 3.5 ns, depending upon the output load. ABT also offers a very fast propagation delay, with a maximum of 3.5 to 4.5 ns specified depending on the manufacturer.

All in all, this offers a significant performance boost over standard (older) logic families. ABT also reduces concerns over bus contention by offering a much shorter disable delay than enable delay. This means that devices sharing a common bus can be switched on-to-off and off-to-on immediately following the other, because the device with preceding control of the bus is guaranteed to be shut down prior to the new device being enabled. However, contention can also be timed out from system timing equations. Low-voltage technology (LVT) is the 3.3-V version of ABT and offers similar features.

A recent enhancement to ABT has been introduced by Texas Instruments (TI). This technology is known both as ABT enhanced (ABTE) and enhanced transceiver logic (ETL). This technology was developed and specified by the VME64bus committee to provide extended performance to VMEbus systems. ETL improves the noise margin by reducing the width of the threshold range from the 1.2 V of standard TTL down to a tight 200 mV. This has two immediate effects: the noise margin is dramatically increased, and the window for sampling a valid signal is increased while still maintaining compatibility with older TTL systems.

Noise margin is calculated by comparing that portion of the total swing in which the signal is in a known state (outside the threshold region) to the total signal swing. By maintaining the same overall signal swing (0.5 V for low, 2.4 V for high) but reducing the threshold region to 200 mV, ETL raises the overall noise margin to 90%,

compared to 35% for a standard TTL family. As a result, signal integrity will be maintained even if the environment is significantly more noisy. The magnitude of the noise must be much greater to push a valid signal into the threshold region in an ETL system.

The other path to upgrading backplane technology involves a more dramatic change in signal levels. While this precludes backward compatibility with TTL systems, it does offer great advancements in performance. Backplane transceiver logic (BTL), Gunning transceiver logic (GTL), emitter-coupled logic (ECL), low-voltage differential signaling (LVDS), and Bus LVDS (BLVDS) fall into this category, with each offering unique capabilities to address specific application issues. However, all trend towards narrower thresholds and reduced signal swings.

The first two technologies are single-ended, which means the logic state is indicated by the signal voltage referenced to ground alone. The last three are differential data transmission technologies (see *"Single-Ended Vs. Differential Transmission," p. 104*). Using two active signal lines, the logic state is the differential voltage between the two. This improves the noise margin by a multiple of the signal swing. Recall that single-ended noise margins are only a fraction of the signal swing.

BTL was invented by National Semiconductor in 1984 in support of the initial Futurebus protocol specifications. Although Futurebus and its enhancement Futurebus+ have yet to attain significant market share, the underlying physical-layer technology, BTL, has enjoyed significant market success. High bandwidth in a heavily loaded environment became a key requirement for enterprise LAN hubs and large telecommunications systems. BTL, used in conjunction with proprietary protocols, offered performance and benefits similar to those of a full Futurebus implementation at a substantially lower cost. BTL is commonly used in 20- to 66-MHz systems with as many as 20 cards.

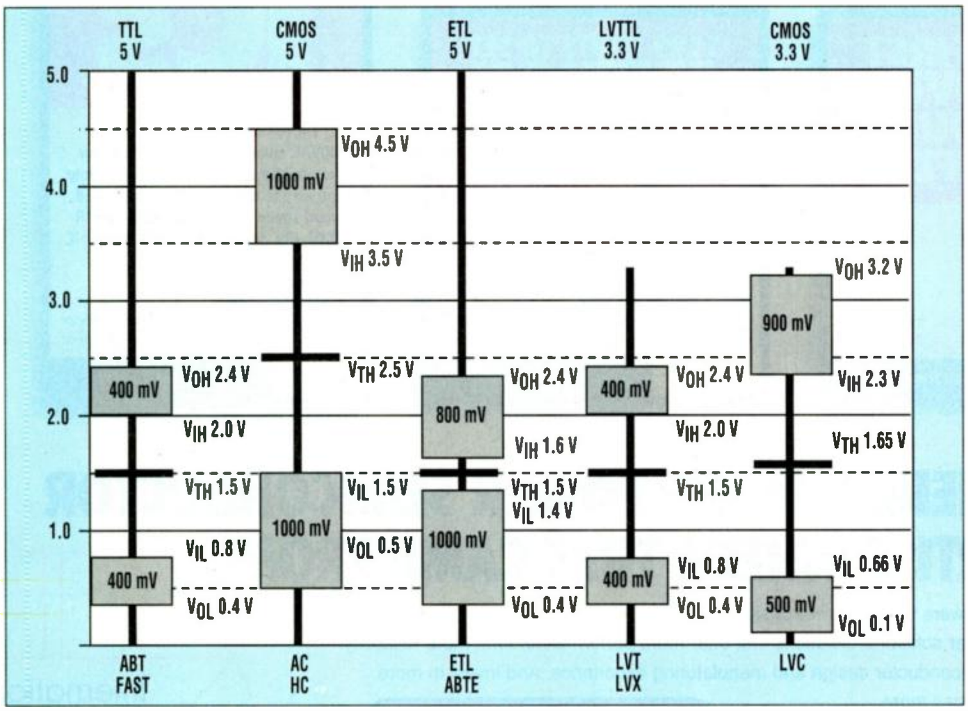
The BTL signal structure offers a compressed signal swing—almost half that of TTL. The threshold region has been reduced as well, down to 150 mV. It also has a high drive capability (sink) of 80 mA and is an open-collector design. For the high level, a termination to 2.1 V is required. What really makes BTL unique for backplane applications is its extremely low output capacitance—typically below 5 pF, whereas most TTL-compliant technologies are two to four times higher. This reduced loading has a significant impact on the maximum performance of the bus, and allows BTL-based systems to have either increased performance or significantly better timing margins than comparable ABT or ETL systems.

For this reason, BTL is often considered when a combination of high speed and a heavily distributed load of many boards are required. For dense parallel applications, National Semiconductor has recently announced CMOS BTL (CBTL). This is a pure CMOS technology that provides the full feature set of BTL with reduced I_{CC} currents, thus easing system power-supply design and distribution.

Both BTL and ETL feature additional protection in the form of live-insertion circuitry. These devices offer designers the capability to pre-bias the driver before insertion into the backplane, thereby avoiding system glitching and damage to the inserted board. Live insertion, or hot swapping, is of particular importance to the telecommunications marketplace. In these applications it is critical that maintenance and repair be performed without shutting down the entire system, or causing disruption to the traffic on the backplane.

Many of these same features are offered by GTL. Invented in 1991 by Xerox, GTL further reduces the overall signal swing (0.4 to 1.2 V) and threshold (100 mV). This technology was specifically created to address very fast chip-to-chip interfacing issues, such as those between microprocessors and memory devices. As such, the drive capability of GTL is specified at 40 mA, half that of BTL. Some devices on the market today have been specified to have 60-mA drive capability to boost performance.

Although originally intended for low-voltage, high-speed computer applications, GTL is finding acceptance in some areas of small backplane design. Due to the low drive capability (40 mA), it is not appropriate for a heavily loaded environment, but for systems that require



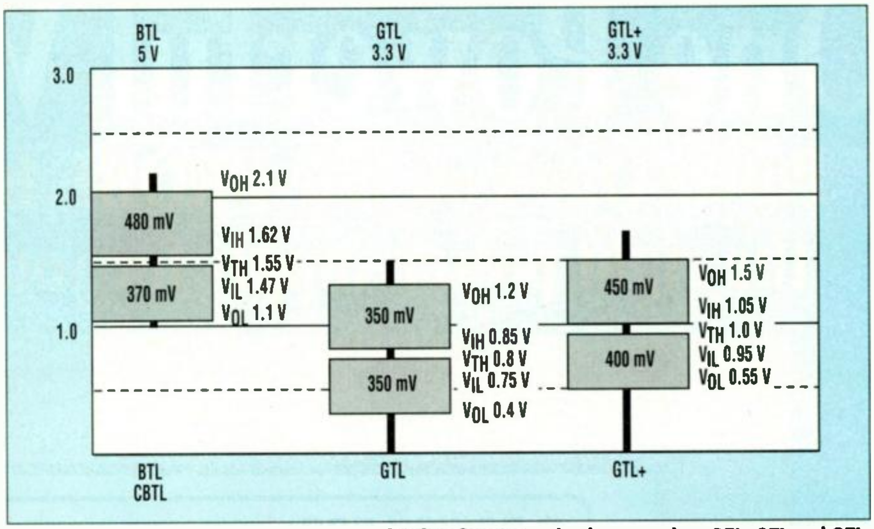
5. The noise margin for common 5- and 3.3-V standard logic technologies may be calculated by subtracting V_{IH} from V_{OH} and V_{OL} from V_{IL}. Among these technologies, ETL/ABTE has a greatly decreased threshold region to increase the noise margin.

high-speed (30 to over 50 MHz) performance between fewer than a dozen cards, it is a very good fit.

The GTL specification has been modified slightly and reintroduced in some applications as GTL Plus, or GTLP. The difference here is that the entire signal swing has been widened slightly to 0.95 V (0.55 to 1.5 V) while maintaining the 100-mV threshold. This results in a slightly higher noise margin and pushes the threshold region slightly further away from ground—a consideration implemented to avoid potential ground-bounce issues. Both varieties of GTL are available on the market, and it is likely that the personal computing marketplace will determine the future of this standard.

In applications where extremely high backplane speed is required, ECL has been adopted. This technology can provide backplane clocking speeds beyond 100 MHz, far greater than single-ended bus-driving technologies. This performance requires trade-offs in terms of both power consumption and power-supply design. ECL achieves its high performance (>100MHz) by making use of a low output impedance and a reduced threshold (120 mV).

Commonly operating at negative voltages, an ECL backplane places additional cost in the design and routing of the system power supply. Interfacing the rest of a system to the ECL backplane can also be a design issue; some ECL backplane designs require associated ECL logic in the rest of the system in order to maintain system throughput. Translator devices may be needed to interface between TTL and ECL such as the 100328 devices.



6. From a noise-margin/level comparison of reduced-swing technologies such as BTL, GTL and GTL +, it can be seen that although the output swings have been reduced the noise margins have actually been improved—relative to some full-swing logic technologies such as TTL, LVC, and ABT.

Positive ECL (PECL) offers yet another choice, this version of ECL supports positive-voltage, power-supply operation. Even with its power and complexity limitations, ECL is uniquely suited to meet the requirements of high-bandwidth systems. These are obtained by designing the drivers as Class A amplifiers operating in the linear region, thus providing fast balanced ac specifications, and an extremely low output impedance for high-speed data transmission.

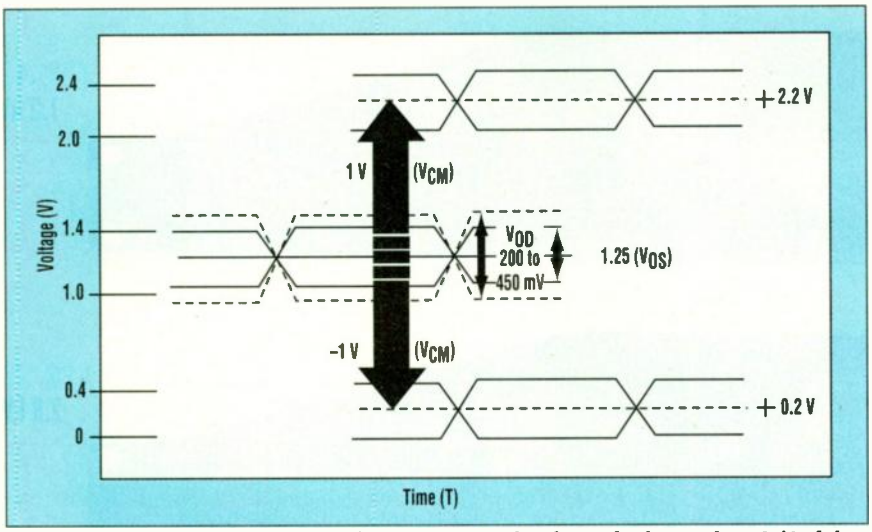
LVDS is a high-speed (hundreds of megabits per second) differential data transmission technology that operates at very low power-dissipation levels from common power-supply rails (5 or 3.3 V). Being differential, and supporting a ±1-V common-mode range,

Single Ended Vs. Differential Transmission

In many applications, the use of differential transmission technologies is ruled out by myths alone. When the word differential is spoken, it immediately generates a vision of two pins per signal and gigantic buses. It is true that differential transmission uses two lines per signal, as the logic state is denoted by the difference voltage, whereas single-ended transmission relies on a voltage level and only one active signal line. However, in designing large single-ended backplane buses, the large return current must be taken into account. To provide a low-impedance path, it is common to assign many ground pins. The ratio of grounds to signals is application dependent but ranges on the low side commonly as 3:1 to as high as 1:1. If the 1:1 ratio is selected, then the "pins required" for a differential bus and the single-ended bus come close to par.

Differential can even beat the 3:1 applications, and reduce pins required even further. Since differential technologies use small swings to enable high-speed operation, faster signal paths are possible. Combining differential bus driving and a serializer/deserializer function reduces pin count to almost zero. Two pins for the serial signal, and a single common (GND) reference. This reduction in bus width requires less pc-board real estate, allows for smaller connectors and smaller interconnect media, and even eases the termination design.

Differential data transmission provides higher noise rejection than single-ended technologies, especially low-swing families such as GTL. With differential transmission, noise is coupled onto both lines, thus is seen as common by the receivers and rejected. For this reason, the common-mode range of the differential technologies should be compared to the noise margin of the single-ended technologies. In general, differential systems will provide twice the noise rejection of single-ended systems. This is also the reason that differential transmission works best on closely-coupled interconnects (pc-board traces close together and twisted pair cable) as it helps to ensure that noise is coupled common.



7. The active signal swings of LVDS and Bus LVDS are reduced even further to about 1/4 of the reduced-swing technologies illustrated in Figure 6. However, because LVDS is differential, the common-mode range should be compared to single-ended noise margins. The effective noise margin is two to four times better using LVDS.

LVDS provides about twice the noise margin of GTL or BTL. Termination is greatly simplified, as no active pull-up voltages are required (as in the case of BTL and GTL technology). A single surface-mount resistor is all that is required. LVDS drivers swing from 250 to 450 mV, centered around 1.25 V, while the receivers support thresholds less than 100 mV. Standard LVDS drivers and receivers are commonly employed in point-to-point or multidrop (multiple receivers) applications, thus they can be used in switched-backplane applications, or on other special links across a backplane.

BLVDS also is a high-speed (hundreds of megabits per second) differential data transmission technology that extends the benefits of standard LVDS into multipoint bus configurations supporting bidirectional half-duplex bus communication. It differs from standard LVDS by providing a higher drive, which provides similar small-signal swings (about ±250 mV) while loaded with two terminations (one at both ends of the bus).

Since the signal swing is greatly reduced, fast transition times are possible, thus allowing the drivers to address high data rates ranging from hundreds of megabits/s to over 1 Gbps. The differential data transmission scheme provides a ±1-V common-mode range and live insertion (hot plug) of devices into an active bus. Additionally, the low voltage swing minimizes power dissipation and noise generation (crosstalk and EMI). BLVDS greatly simplifies the area of bus termination as it does not require special active termination devices, nor does it require a unique termination rail (such as 2.1 V for BTL) to be supplied. It simply requires a single surface-mount resistor across the pair at each end of the bus.

BLVDS also utilizes common power-supply rails (3.3 or 5 V), minimizes power dissipation in the interface devices, generates little noise, supports live insertion of cards, and drives heavily loaded multipoint busses at hundreds of Megabits/s. BLVDS addresses many of the challenges faced in a high-speed bus design and products are available as simple transceiver devices, optimized parallel bus transceivers with ultra low skew, and 10-bit serializer/deserializer devices.

Fitting It All Together

Having examined the benefits and features of each technology, and applying transmission line theory, a comparison of backplane performance with respect to loading can be produced *(Fig. 4)*. This comparison is purely relative, as the capabilities of the common technologies incorporate a significant degree of overlap. Given enough design and debug time, each technology can be pushed beyond the limits described here. A comparison of levels and the resulting noise margins are shown in Figures 5, 6, and 7. Figures 5 and 6 are common, single-ended technologies, while Figure 7 is specific for LVDS and Bus LVDS.

Note that the common-mode range in differential data transmission technologies is what should be compared to the standard noise margins of single-ended technologies. Therefore BLVDS and LVDS, with their 250-mV swings, both provide about twice the noise margin of GTL- or BTL-based systems. For lower-speed systems, regardless of load conditions, a standard TTL family such as LCX or FACT may be used.

If a performance improvement is required, but backward compatibility is necessary, LVT or ABT or ETL may be considered. Very fast systems with a few boards (light loading) could find GTL a good design choice, provided live insertion is not required. For more heavily loaded systems running at high speed, BTL or even ECL/PECL may be required. If ultra-high performance is required, and ultra low power dissipation is a must, then Bus LVDS is the driver technology of choice. In each case, regardless of the technology chosen, proper design rules should be followed to minimize reflections, crosstalk, and other transmission-line related issues. Upgrading driver technologies can help eliminate these problems, but no transceiver can mask a fundamentally poor design.

John Goldie is the applications engineering manager responsible for Interface Products for National Semiconductor. He has published a number of articles on topics such as LVDS and is chair of the TIA TR30.2.1 Electrical Subcommittee on Interface Standard. Mr. Goldie earned his Bachelor of Science Degree in Electrical Engineering from San Francisco State University in 1988.

Bruce Motavaf is a senior applications engineer for the Interface business unit at National Semiconductor in Santa Clara, California. He joined National Semiconductor in 1989. Mr. Motavaf completed his Bachelor of Science degree in Electrical Engineering at Northwestern University and is currently working on his Masters in Business Administration at Golden Gate University.

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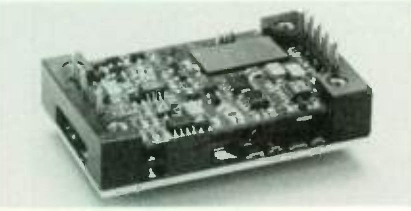
PRODUCT UPDATE: RESISTORS/CAPACITORS/INDUCTORS

Manufacturer	Device	Description	Price and delivery	CIRCLE
		RESISTORS/CAPACITORS		
AVX Corp. **Mytle Beach, SC** **Joe Rana (843) 448-9411** **Fax (843) 448-1943** **www.avxcorp.com**	Z Chip integrated resistor/capacitor	Packaged in an 0603 format, this impedance-matching, integrated, series resistor/capacitor chip targets termination applications in laptops or handheld devices. The chip is made from a resistive electrode material that creates the resistor value, rather than screen-printing a capacitor onto a resistive element. The electrode material also acts as the electrode plate to form the capacitance rating. The chip is available with capacitor values of 33, 47, 68, 100, and 150 pF, with a tolerance of ±20%. The resistor values are 22, 33, 47, 51, 80, 100 and 150 Ω, with a tolerance of ±10%. The dc rated voltage is 25 V.	$0.05 each per 100,000	493
Isotek Corp. Swansea, MA Mark Ferreira (508) 673-2900 Fax (508) 676-0885 E-mail: tekinfo@isotekcorp.com www.isotekcorp.com	Model EQ chip resistor	This ultra-precision, wire-bond, etched nickel-chrome foil resistor targets power-conversion and motor-drive module applications. The device is available in resistance values ranging from 5 to 60 kΩ, with tolerances down to ±0.05%. The power rating is 0.125 W (continuous) and the TCR is 0.4 ppm/°C.	Typically less than $1 each per 1000	494
Janco Corp. **Burbank, CA** **Tom Kira (818) 846-1800** **Fax (818) 842-3396** **E-mail: jancoengr@aol.com**	PB Series micro-miniature potentiometers	These miniature, high-reliablity potentiometers meet MIL-R-39023 and MIL-S-3786 environmental demands and come rated at 0.50 W (max) in values ranging from 1 to 50 kΩ. Options include shaft resistance, travel, torque, detents, and shaft diameter. Mounting can be done using quick-connect or flying-wire leads.	$100; eight weeks ARO	495
Kemet Electronics Greenville, SC Sales Dept. (864) 963-6300 Fax (864) 963-6521 E-mail: capmaster@kemet.com www.kemet.com	T491 series surface-mount tantalum capacitor	Designed for low-profile applications, this EIA 6032-footprint, molded, surface-mount tantalum capacitor has a maximum height of 1 mm. Initially available in a 15-µF, 6-V version, the device will soon be available in a 22-µF, 4-V, and a 10-µF, 10-V version.	$0.45 each per 1000	496
	T510 low-ESR tantalum capacitor	Measuring 7.3 by 6.0 mm, this latest addition to the company's T510 line of low-ESR tantalum capacitors has a resistance at 100 kHz of 15 mΩ for the 1000-µF version. The device has a height of 3.8 mm and conforms to EIA 7260. Other features include a voltage rating of up to 6 V and the ability to handle up to 4 A of ripple current.	From $1.40 each per 500	497
Seacor **Westwood, NJ** **Sales Dept. (800) 662-7322** **Fax (201) 664-8544** **E-mail: upsales@seacorinc.com**	GTO low-loss damping capacitors	This line of low-loss, polypropylene, metallized GTO damping capacitors is designed for commutating power inverters and linking control and power electronic devices. The high-dielectric, self-healing, low-inductance devices are rated from 15 to 60 A at 800 to 2100 V ac. Standard values range from 0.5 to 7.5 µF. Termination is via screw terminals.	$55 each in quantity; six to eight weeks ARO	498
Spectrol Electronics Corp. Ontario, CA Gene Stauffer (800) 624-8902 Fax (909) 923-6765 E-mail: gstauffer@spectrol.com www.spectrol.com	Series 202 instrument-grade potentiometers	These wirewound, 1.75-in. diameter, full MIL-spec. potentiometers target military, industrial control, and aerospace applications. The devices come with either ball (servo mount) or sleeve bearings and in values ranging from 50 Ω to 50 kΩ, with tolerances of ±3% and with a linearity of ±0.25%. The operating temperature range is from –55° to 125°C, with a rated power of 5.4 W at 40°C.	$150; six weeks	499
State Of The Art Inc. **State College, PA** **Bernie Hoy (800) 458-3401** **Fax (814) 355-2714** **E-mail: sales@resistor.com** **sales@resistor.com** **www.resistor.com**	High-voltage chip resistors	Three new sizes have been added to the company's line of high-voltage chip resistors. The new sizes measure 0.250 by 0.125 by 0.25 in. (2512), 0.375 by 0.180 by 0.025 in. (3818), and 0.375 by 0.375 by 0.025 in. (3838). The devices are made from a thick-film resistor element on an alumina body, and range in value from 22 kΩ to 100 MΩ. The maximum voltage rating is 5 kV.	Under $1 each in quantity	500
Tocos America Schaumburg, IL Robert Kruse (847) 884-6664 Fax (847) 884-6664 E-mail: sales@tocos.com www.tocos.com	Series GF063 and GF06 /-in. trimmer potentiometers	These /-in.-square, cross-slot trimmer potentiometers come in three versions: with a large-diameter rotor for automatic machine adjustment, with an adjustment knob, or tuned using a standard tuning tool. Able to withstand wave soldering and immersion, the devices have a resistance range of 10 Ω to 5 MΩ, a power rating of 0.5 W at 70°C, and a working voltage of 250 V dc (max).	GF063 with knob, $0.63; GF06, $0.42 each per 1000	501
Ventronics Inc. **Kenilworth, NJ** **Sales Dept. (908) 272-9262** **Fax (908) 272-7630** **E-mail: ventronics@prodigy.net**	X-2 and Y capacitors	The X-2 metallized polypropelene film capacitors are rated at 250/275 V ac with values of 0.0047 to 1.0 µF. The self-healing devices come in flame-retardant cases. The X types are rated at 1250 to 4000 V ac and come in values ranging from 100 to 10,000 pF. The dielectric strength is 2600 V ac for 60 seconds.	X-2, $0.25; Y, $0.12 each in quantity; two to three weeks ARO	502
Vishay Dale Norfolk, NE Gary Bruns (402) 371-0800	Model CRCA12 E & S resistor/capacitor array	Combining both a resistor and capacitor on one chip, these thick-film devices target high-frequency line-termination, EMI/RFI-filtering, and timing-circuit applications. The devices have a capacitance range of 10 to 1800 pF, a tolerance of ±20%, and a voltage rating of 50 V dc. The resistors range from 10 Ω to 1 MΩ, have a tolerance of ±5%, and a power rating of 1/8 W at 70°C.	From $0.08 to $0.10	503

Quarter-Brick Converters Output Up To 150 W

The QBS/QES series of miniature converters measure 1.45 by 2.28 by 0.50 in. and output up to 150 W. The devices take an input of between 18 and 36 V or

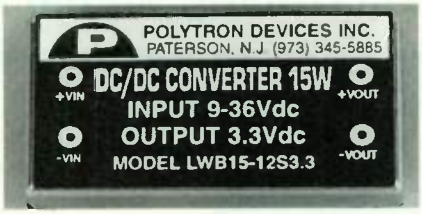


36 and 75 V dc, have an efficiency of 88%, and include a version with an output of 5 V at 20 A. Other features include 1500-V dc isolation, remote on/off, fast startup, and ±10% voltage adjustment. Pricing is $54.

International Power Devices, 20 Linden St., Boston, MA 02134; James Crehan (617) 783-3331 ext.5103; fax (617) 782-7416; e-mail: james@ipdconverters.com. **CIRCLE 587**

4:1-Input-Range Converters Output 3.3 V DC

These 5-, 10-, and 15-W dc-dc converters add 4:1-input-range capability to the company's line of 3.3-V-dc devices. Able to take from 9 to 36 V or 36 to 72 V, the units come in a package measuring 1.0 by 2.0 by 0.375 in., and have an efficiency of 86%. Protection includes output overvoltage and short circuit. Among the other features are line and

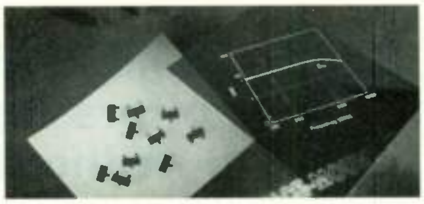


load regulations of ±1% and a ripple and noise figure of 50 mV p-p (max). The transient response is 200 µs (max) to 1% of final value, and the operating temperature range is –25° to 71°C. Pricing is $34 each in quantity.

Polytron Devices Inc., P.O. Box 398, Paterson, NJ 07544; Sheri Lynn (973) 345-5885; fax (793) 345-1264; e-mail: polytron@erols.com; Internet: www.polytrondevices.com. **CIRCLE 588**

N-Channel And P-Channel JFETs Come In SOT-23 Package

Until recently only available in a TO-92 package, the SSTJ211 and '12 and SST5460, '61, and '62 n-channel and p-channel JFETs, respectively, now come in a SOT-23 package. All have a low leakage current of 1 pA (typical)



for the n-channel devices, and 3 pA for the p-channel devices. Pricing ranges from $0.15 to $0.45 each per 100,000 units.

Siliconix, 2201 Laurelwood Rd., Santa Clara,CA 95054; Joyce De Sorbo (800) 554-5565; fax (408) 467-8995; www.siliconix.com. **CIRCLE 589**

20-W DC-DC Converter Is Surface-Mountable

The SM20 is a 20-W, surface-mountable dc-dc converter that's fully compatible with existing pick-and-place equipment. The device has a footprint of 46.48 mm^2, a height of 0.4 in., and meets UL1459 and BS6301 telecom applications approval. Features include a 10-ms startup time, remote on/off, and inputs of 24 or 48 V. Pricing is $50 each per 1000.

Lambda Electronics Inc., 515 Broadhollow Rd., Melville, NY 11747; Sales Dept. (619) 575-4400; e-mail: smseries@lambda.com; Internet: www.lambdapower.com. **CIRCLE 590**

PRODUCT UPDATE: RESISTORS/CAPACITORS/INDUCTORS

Manufacturer	Device	Description	Price and delivery	CIRCLE
RESISTORS/CAPACITORS				
Vishay Angstrohm Hagerstown, MD Teresa Wilhide (301) 739-8722 Fax (301) 797-6852 E-mail: angstrohm@compuserve.com www.vishayangstrohm.com	RNR/ RNN75 hermetically sealed metal-film resistors	Qualified to MIL-PRF-55182, these high-reliability, metal-film resistors come in a hermetically sealed glass enclosure with a diameter of 0.250 in. The devices have a resistance range of 49.9 Ω to 1.21 MΩ, a tolerance of ±0.1%, ±0.5%, or ±1.0%, and a temperature characteristic of ±25 ppm/°C.	From $13.04 each per 100	504
TRANSFORMERS/INDUCTORS				
Prem Magnetics Inc. McHenry, IL Sales Dept. (815) 385-2700 Fax (815) 385-8578 E-mail: sales@premmag.com www.premmag.com	SLP-24-500 series 6.0-VA transformers	Designed for instrumentation and HVAC applications, these 6.0-VA transformers handle inputs up to 24 V ac and outputs from 5.0 to 28 V ac. The output current ranges from 200 mA to 1.2 A. The devices are hi-pot tested to 2500 V ac, measure 1.625 by 1.312 by 1.290 in., and have UL Class B insulation.	$2.44 each in quantity	505
Pulse San Diego, CA Sales Dept. (619) 674-8130 www.pulseeng.com	B4001 and B4003 common-mode choke for ADSL	These common-mode chokes are designed to reduce noise in asymmetrical digital subscriber lines (ADSLs) and very high-bit-rate ADSLs. The chokes have a rejection rating of up to 49 dB, a winding isolation of 1500 V, and comply with Bellcore 1089 requirements. Through-hole and surface-mount versions are available.	$1 each per 5000	506
Toko America Inc. Mt. Prospect, IL Pat Moroney (847) 297-0070 Fax (847) 699-7864 E-mail: info@tokoam.com www.tokoam.com	FSLM and FSLB series wirewound SMD chip inductors	Assembled using a proprietary wirewound structure and welded terminations, these surface-mount chip inductors have a footprint of 2.5 by 2.0 mm and a profile of 1.6 mm. The FSLM series has an inductance of 100 nH to 220 µH, while the FSLB series has an inductance range of 1 to 47 µH.	$0.20 each per 10,000	507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PRODUCT FEATURE

Direct-Drive, Quad-Lamp Inverter Targets 18-in. LCDs

As desktop computers start to take advantage of the falling cost of large-screen LCDs, the backlights behind these devices are coming under closer scrutiny from both a quality and power-dissipation standpoint. In addition, the particularly pernicious cost pressures in the desktop arena continue to exact their toll from everyone from systems to component suppliers.

It's with these issues in mind that LinFinity Microelectronics has introduced its RangeMAX digital dimming backlight inverters—the latest version of which is the LXM1641-01 for 18-in. LCDs from manufacturers such as Sharp and LG Electronics.

The inverter is based on the company's proprietary direct-drive digital dimming circuitry that uses a fixed lamp-current value with duty-cycle control. Traditional methods involve varying the lamp current magnitude to adjust the light output. Along with lowering cost and size by eliminating the need for a resonant inductor and capacitors, the LXM1641-01 achieves a usable dimming range in excess of 100:1. The device also incorporates a video-synchronization feature. It allows the wide dimming range while preventing display disturbances caused by beat frequencies between the lamps and the video frame rates.

Measuring 250 by 32 mm, the inverter powers up to four lamps, takes a 9- to 12-V input, and outputs up to 7 mW per lamp at an individual operating voltage of 300 to 800 V rms. A soft-start current-drive method prevents cathode wear. Other features include a sleep current of 75 µA, and a fail-safe mechanism that keeps the application running should a lamp fail. Protection includes output short circuit and open circuit, as well as line fusing. Pricing is $59 each per 1000; delivery is immediate.

LinFinity Microelectronics Inc.
11861 Western Ave.
Garden Grove, CA 92841
George Henry (714) 372-8357
fax (714) 372-3566
www.LinFinity.com
CIRCLE 553

PATRICK MANNION

DESIGN NOTES

SMBus Accelerator Improves Data Integrity – Design Note 193

David Bell and Mark Gurries

Introduction

The System Management Bus (SMBus) is gaining popularity in portable computers as a communication link between smart batteries, the battery charger and the power management microcontroller. The convenience of this simple 2-wire bus is prompting designers to use it for communication with other peripherals such as battery selectors, backlight controllers, temperature monitors, power switches and other devices. Before long, the SMBus will become what its creators envisioned—a general purpose system management bus that connects various low speed peripherals throughout a portable computer (see Figure 1).

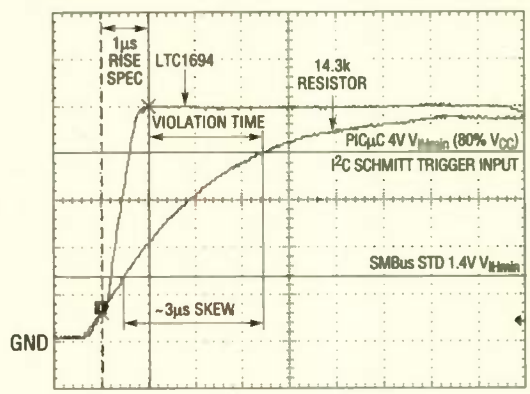
The SMBus uses the open-drain I^2C® protocol for its physical layer, with respecified logic thresholds and pull-up current. Whereas the I^2C bus allows pull-up currents as high as 3mA, the SMBus has been specified with a maximum pull-up current of only 350μA. The maximum 400pF bus capacitance allowed by I^2C is reduced to only *50pF* because of the low pull-up current provided by the SMBus. Although the lower logic thresholds specified for SMBus peripherals mitigate the rise time problem, most SMBus systems include devices with I^2C CMOS logic thresholds that can be as high as $0.8 \bullet V_{CC}$ (microcontrollers are a good example). All it takes is one such peripheral with high logic thresholds, and SMBus rise times can seriously restrict bus capacitance.

The SMBus rise time problem can result in data integrity problems, or in severe cases, cause the bus to stop operating entirely. Because 50pF can easily be exceeded with just a few feet of cable, SMBus systems often fail to operate reliably when simply connected together on the lab bench. The problems of SMBus capacitive loading can become worse when more peripherals are connected by long traces running throughout a portable computer.

The Solution

Linear Technology developed the LTC®1694 SMBus Accelerator* active pull-up circuit to alleviate the SMBus rise time problem. This SOT-23 packaged part simply replaces the two external pull-up resistors and reduces the SMBus rise time by a factor of 3× to 4×. Figure 2 compares an SMBus signal rise time using a standard resistor pull-up

*Patent pending



VERT: 1V/DIV HORIZ: 1μs/DIV
Test Conditions: Linear Technology DC134C Demo Board (5.0V SMBus Supply, PIC16LC73A μC, Smart Battery)

Figure 2. SMBus Open-Drain Signal Rise Times

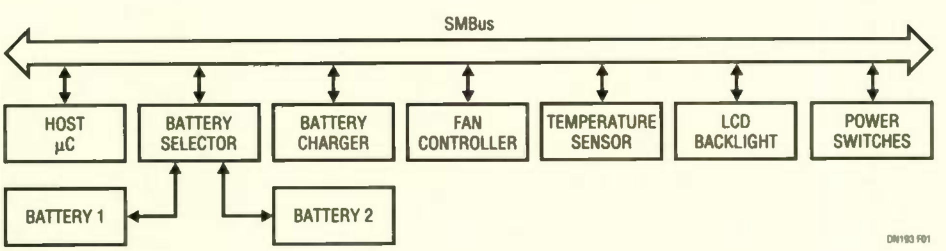


Figure 1. SMBus Applications in a Notebook Computer

a signal produced with the SMBus accelerator. SMBus ystems that work unreliably (or not at all) with the inimum value pull-up resistor perform as intended with e LTC1694.

gure 3 is a functional block diagram of the LTC1694 MBus accelerator. Two identical pull-up circuits are ontained within the LTC1694: one for the clock line (SCL) nd one for the data line (SDA). When both open-drain gnals remain high (SMBus idle), the LTC1694 provides 100μA pull-up current to each line to keep them in the gh state. When either signal is pulled low by an SMBus iver, the pull-ups source approximately 275μA. Because this pull-up current is less than the 350μA allowed the SMBus specification, the logic low (V_{OL}) level on e bus is reduced, resulting in improved low state noise argin.

ne biggest improvement occurs when an SMBus driver leases the open-drain signal. If the signal voltage exeeds 0.65V and the positive slew rate exceeds 2V/μs, then a 2.2mA pull-up current source is activated the LTC1694. This 2.2mA current source quickly pulls e signal high until it hits the supply rail. After a short elay the current is reduced to the 100μA level with the signal at a steady state high level. Noise immunity is also built into the slew rate detector to avoid false tripping on narrow noise spikes. In essence, the LTC1694 provides light pull-up when the open-drain signal is static or falling, but accelerates the rising edge once a rising signal is detected.

Making the Upgrade

Retrofitting an existing SMBus system is easy—the LTC1694 simply replaces the two pull-up resistors. PCB area is approximately the same, owing to the small 5-pin SOT-23 package. Because SMBus peripherals may operate from either 5V or 3.3V, the LTC1694 is designed to operate equally well from either supply voltage. The SMBus accelerator powers down to only 60μA when both SMBus signals are high, so impact on battery life is also insignificant.

SMBus data integrity is vital, especially since Lithium-Ion battery charge control may be communicated via the bus. It's not always obvious that "flaky" SMBus operation is the result of excessive rise time, but the test is easy to implement—simply replace your pull-ups with the LTC1694.

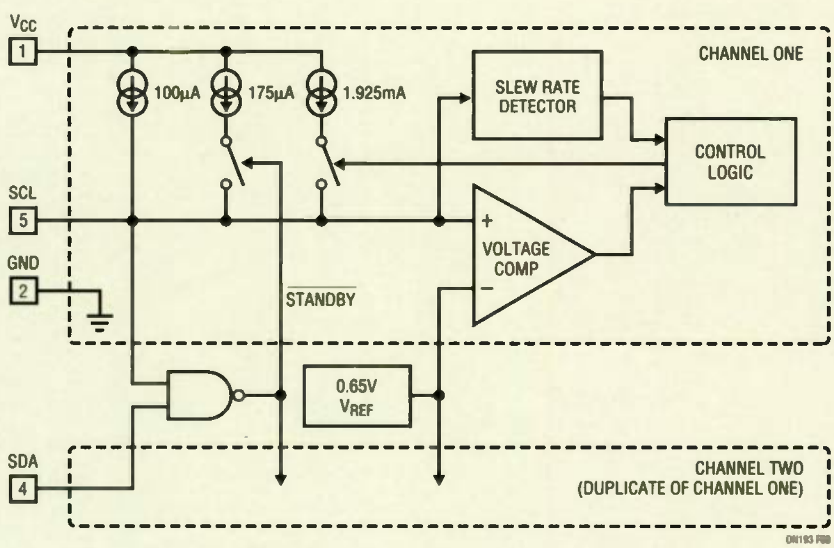


Figure 3. LTC1694 Functional Block Diagram

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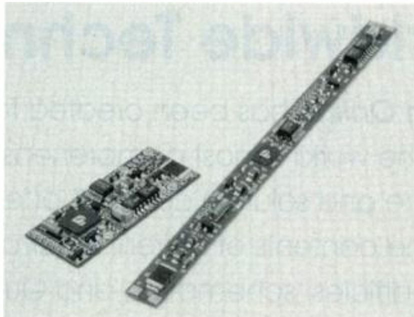
The PS30xZ-403 and 404, and PS30xZ-413 and 414 are SMBus 1.0-compatible, smart-battery modules that can be integrated into any three- or four-cell Li-ion pack. Measuring 45



by 17 mm and 120 by 7 mm, respectively, the devices use patented, self-learning algorithms to track charge and discharge to provide ±1% accuracy. The modules are pre-tested and fully assembled and come with high-side switching safety electronics to disconnect the charge or discharge if necessary. Pricing is $15 each per 10,000.

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7-W DC-DC Converter Comes With Dual Outputs

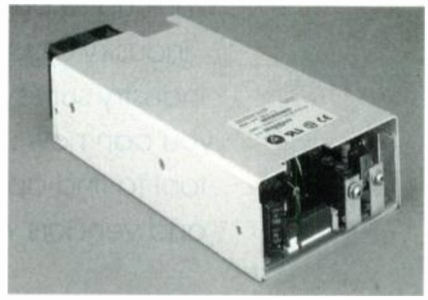
Part of the company's MacroDens PKF family, the PKF 4629 takes in 38 to 72 V and outputs 5 and –12 V. The 7-

W module can have any combination of output currents up to 1.2 A on the 5-V line and up to 0.5 A on the 12-V line. Measuring 48 by 24 mm, the module provides full output at up to 95°C with a heat sink or forced cooling. The module has a ramp-up time of 1 ms, a ripple of 50 mV, and a supply-voltage rejection of 45 dB. Other features include an MTBF of 4.9 million hours and EMI compliance to VDE, FCC, and CISPR specifications. Pricing is $24 each per 1000; samples are available from stock.

Ericsson Components, *Pyramidbacken 1. Kungens Kurva, Kista, Stockholm, Sweden; Sales Dept. (888) 85-ENERGY; e-mail: ed.christmas@ericsson.com.* **CIRCLE 601**

500-W, Single-Output Supply Has Power-Factor Correction

The SPF-500 series, 500-W, switching power supply comes with power-factor correction to 0.99. The single-output supply outputs from 12 to 48 at between 42 and 10.4 A, and includes forced current sharing, ac power-fail



signaling, true remote inhibit, and monotonic turn on and off. Measuring 9.65 by 5.0 by 2.07 in., the supply has a line and load regulation of ±1%, an efficiency of 75%, and comes with overload and overvoltage protection. The output is user adjustable over ±5%. Pricing is $325 each in quantity. Delivery is approximately eight weeks ARO.

Todd Products Corp., *50 Emjay Blvd., Brentwood, NY 11717; Robert Schaefer (516) 643-5466; fax (516) 231-3473; e-mail: info@toddpower.com; Internet: www.toddpower.com.* **CIRCLE 602**

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(continued on page 116)

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(continued from page 114)
MOD, and MicroMOD, measure 4.6 by 2.2 by 0.5 in., 2.28 by 2.2 by 0.5 in., and 2.28 by 1.45 by 0.5 in., respectively. A stepped profile allows the devices to be recessed into a board for an above-board profile of 0.45 in. Other features include a baseplate operating temperature of 100°C, a programmable output from 10% to 110% of nominal, and compatibility with N+M fault-tolerant systems. Pricing is from $95 to $112; delivery is two weeks ARO.

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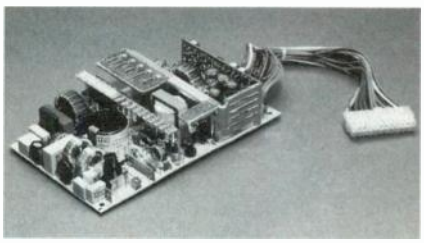

current standards. Available in both single- and triple-output models, the supplies output from 5- to 24-V dc, and 5 V and ±12 V dc or 5 V and ±15 V dc, respectively. The devices take inputs of 85 to 264 V ac or 120 to 370 V dc, with an input frequency of 47 to 440 Hz. Other features include overvoltage and overload protection, an operating temperature range of 0° to 50°C, and a footprint of 3 by 5 in. Pricing is from $35.

***Astec**, 6339 Paseo del Lago, Carlsbad, CA 92009; Tom Tillman (760) 930-4708; fax (760) 930-4700; Internet: www.astec.com.* **CIRCLE 604**

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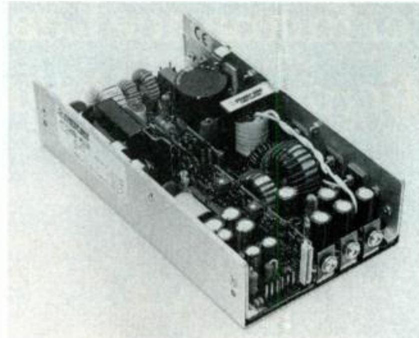

Measuring 8.5 by 4.75 by 2.0 in., the supply allows for current sharing and comes with dual remote sense, dc power-good signaling, and various protection features. The input range is 85 to 264 V ac. Agency approvals include UL1950, CSA, TUV, EN60950, and FCC. Pricing is $253; delivery is from stock in six to eight weeks.

***Power-One**, 740 Calle Plano, Camarillo, CA 93012-9951; Technical Support (800) 678-9445; fax (805) 388-0476; www.power-one.com.* **CIRCLE 605**

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***Yuasa Inc.**, P.O. Box 14145, Reading, PA 19612-4145; Sales Dept. (800) 538-3627; fax (610) 372-8613; www.yuasainc.com.* **CIRCLE 606**

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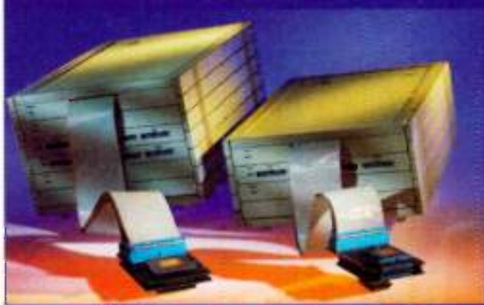

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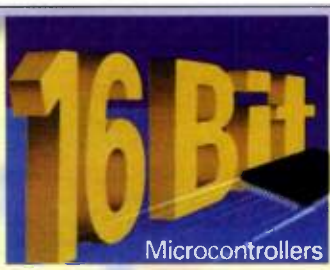

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	Have used	Would consider
Base: Those who have used RTOS	143	176
Base: Those who are considering using RTOS	100.0	100.0
RTXC (Embedded Sys Prods)	8.4	10.2
VMEexec (Motorola)	4.2	6.8
Nucleus (Accelerated Tech)	3.5	

Embedded Systems

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Which 16 or 32 BIT RTOS kernel or executive vendors have you used in the last 12 months for your embedded designs?
Which 16 or 32 BIT vendors would you consider when purchasing RTOSs kernels or executives for your embedded projects?

	Have used	Would consider
Base: Those who have used RTOS	143	176
Base: Those who are considering using RTOS	100.0	100.0
VxWorks (Wind River)	33.6	44.9
PSOSystem (ISI)	23.6	29.0
QNX (QNX Software Sys)	[illegible]	21.0
VRTX (Microtec Research)	[illegible]	21.6
RTXC (Embedded Sys Prods)	8.4	14.2
Windows CE (Microsoft+Partners)	7.0	18.2
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Nucleus (Accelerated)	[illegible]	
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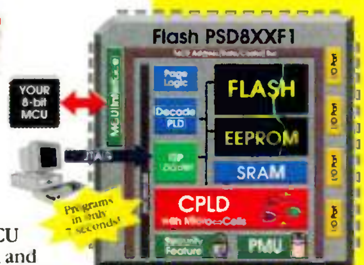

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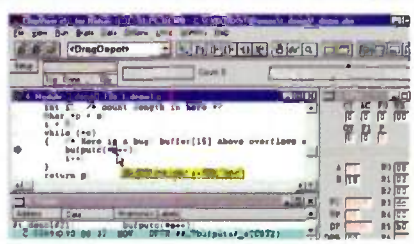

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ELECTRONIC DESIGN
DIGITAL APPLICATIONS

Standard Language Aims To Get PLDs Out Of A Jam

A Programming And Test Language Called Jam Gains Support As Compliant Products Emerge.

BY JOSEPH DESPOSITO, ***TEST AND MEASUREMENT EDITOR***

Digital Applications Special Section: Part 2

As with most new technologies, programmable logic devices (PLDs) have suffered from a lack of standardization. In the case of PLDs, a common programming and test language was the pressing need. The solution appeared last year, when an industry consortium unveiled a new language called Jam. Now, Jam-compatible products are coming to market even as the Joint Electronic Devices Engineering Council (JEDEC) considers adopting the language as an industry standard.

Jam works with all PLDs that offer in-system programming (ISP). ISP enables the programming and reprogramming of PLDs after they have been mounted on a pc board. The language was originally developed by Altera Corp; the consortium includes programmers, test equipment makers, and PLD manufacturers.

Before Jam arrived on the scene, in-system programming of PLDs was plagued by proprietary file formats, vendor-specific programming algorithms, large file sizes, and long programming times. This resulted in a confusing array of options and poor return on investment for design and manufacturing engineers trying to implement ISP in PLDs. The Jam language addresses each of these issues by providing a software-level standard to specify ISP for PLDs. Vendor and platform independent, Jam produces small files sizes and reduces programming times.

The Jam standard is an interpreted language, similar to BASIC, optimized for programming devices via the IEEE-1149.1 test-access-port (TAP) controller, commonly know as JTAG (Joint Test Action Group). The Jam language lets the user specify both the programming data and algorithm in a single file. Once created, a Jam file contains all the information required to program a specific design into a targeted device.

Code Listing

```
Initialize instruction and data arrays
BOOLEAN read_data[32];
BOOLEAN I_IDCODE[10] = BIN 1001101000; 'assumed
BOOLEAN ONES_DATA[32] = HEX FFFFFFFF;
INTEGER i;
'Set up stop state for IRSCAN
IRSTOP IRPAUSE;
'Initialize device
STATE RESET;
IRSCAN 10, I_IDCODE[0..9]; 'LOAD IDCODE INSTRUCTION
STATE IDLE;
WAIT 5 USEC, 3 CYCLES;
DRSCAN 32, ONES_DATA[0..31], CAPTURE read_data[0..31];
'CAPTURE IDCODE
PRINT "IDCODE:";
FOR i=0 to 31;
PRINT read_data[i];
NEXT i;
EXIT 0;
```

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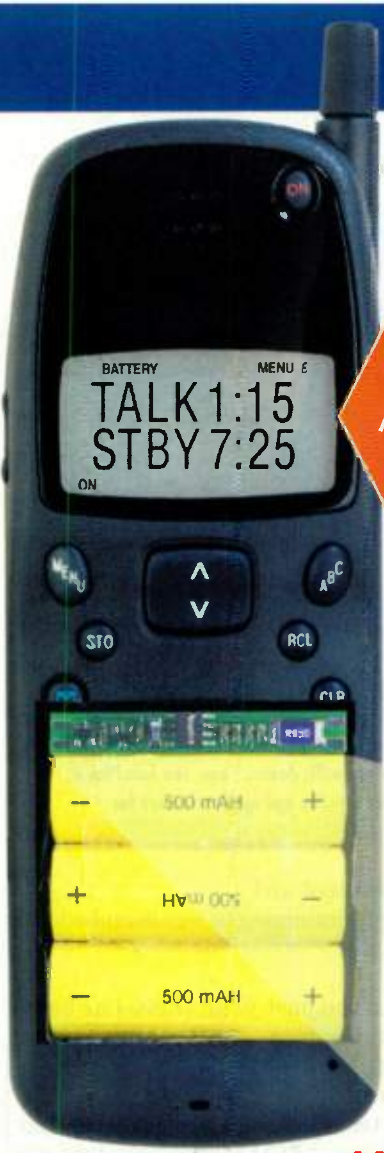

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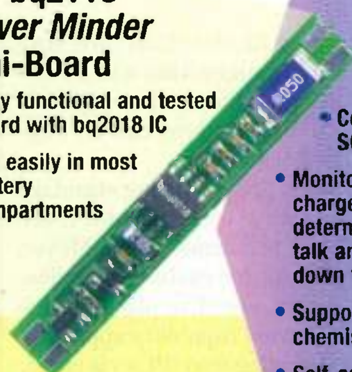

The bq2018 *Power Minder* IC

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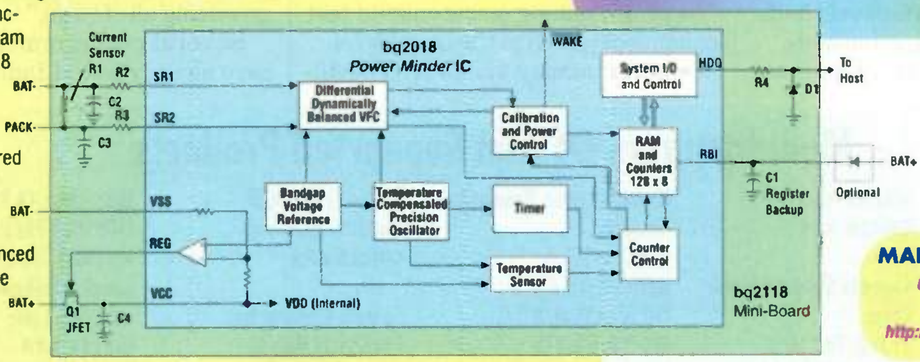
- Single-wire control/ data serial interface
- 115 bytes user-programmable NVRAM store battery data, charge information, & ID codes

How It Works

The bq2018 *Power Minder* IC is a multifunction charge/discharge counter that works with an intelligent host controller to provide state-of-charge information for rechargeable batteries. The functional block diagram shows the bq2018 and bq2118 mini-board.

Charge/discharge is monitored via the low-value sense resistor, R1. A differential dynamically balanced VFC integrates the charge and discharge levels sensed by R1.



By using the accumulated counts in the charge, discharge, and self-discharge registers, an intelligent-host controller can accurately determine battery state-of-charge for any type of battery. Self-discharge is estimated using the internal temperature sensor and timer.

Host controller interface is via the HDQ serial line, allowing access to battery status registers, including read/write access to 115 bytes of the NVRAM (128 bytes total).

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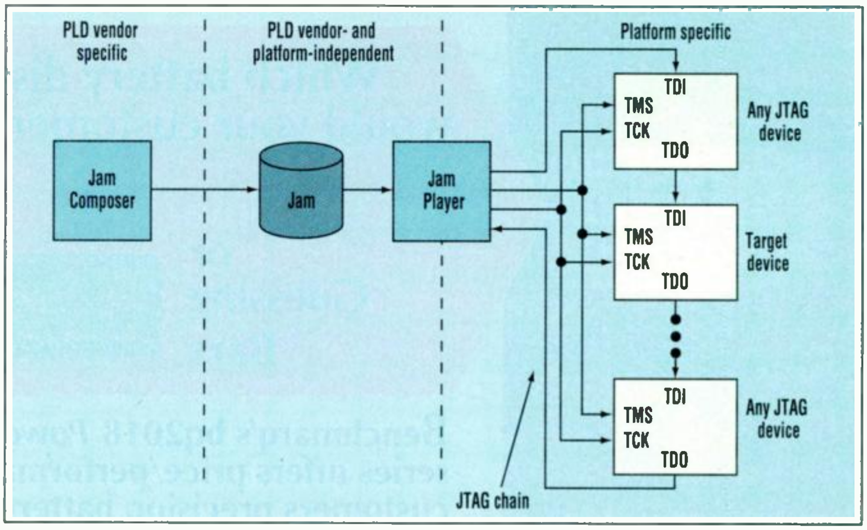
STANDARD LANGUAGE

Jam has two software components, the Jam Composer and the Jam Player *(see the figure)*. Usually, a PLD vendor uses the Jam Composer to write the Jam file required to program a specific design into a specific device. Then, the programmer or tester vendor writes the Jam Player, which interprets the file, and applies vectors for programming and testing devices in a JTAG chain. These elements constitute a universal language and toolset that address all PLDs and all programming methods. See the *Code Listing* for an example of Jam programming code.

As mentioned, the Jam Programming and Test Language has several key attributes, among them vendor and platform independence, smaller file sizes, and shorter programming times. Vendor independence means any Jam Player can read any file created by any Jam Composer. Platform independence means that any Jam file is compatible with any Jam Player running on any platform. In other words, PLD vendors do not have to generate different programming files for different programming platforms.

To limit file size, the Jam language uses high-level commands, FOR-NEXT loops, and data compression. For example, an 8-kbyte programming file delivers the same functionality as a 20-Mbyte file. To shorten programming times, sometimes by a factor of 10 over previous methods, Jam employs branching commands.



Jam has two software components, the Jam Composer and Jam Player. PLD vendors use the Jam Composer to write the Jam file required to program a specific design into a specific device. Then, the Jam Player, written by a device programmer or tester vendor, interprets the Jam file and applies vectors for programming and testing devices in a JTAG chain.

Besides these features, Jam is not specific to any PLD architecture. Any programming algorithm can be described in a Jam file, so that all existing and future devices can be supported by the language.

Creating a programming standard and finding ways to implement it are two different problems. Bryon Moyer, senior manager for customer applications at Altera, sees five places where the Jam software capability applies:

- programming from PCs via cable,
- programming on standalone programmers,
- programming on automated test equipment (ATE) at the board level,
- programming via a JTAG development tool, and
- programming *in situ* in embedded systems.

"In the past year, there has been some progress in all of those categories," says Moyer. "Programming from PCs via cable was probably the first technique that was possible," he continues, "At DAC this past July, we demonstrated a Jam board containing chips from Altera, Lattice Semiconductor, Cypress Semiconductor, and Xilinx. We were successfully programming all of them."

Several programmer companies have already added Jam support, ac-

Manufacturers Of Jam Supported Products

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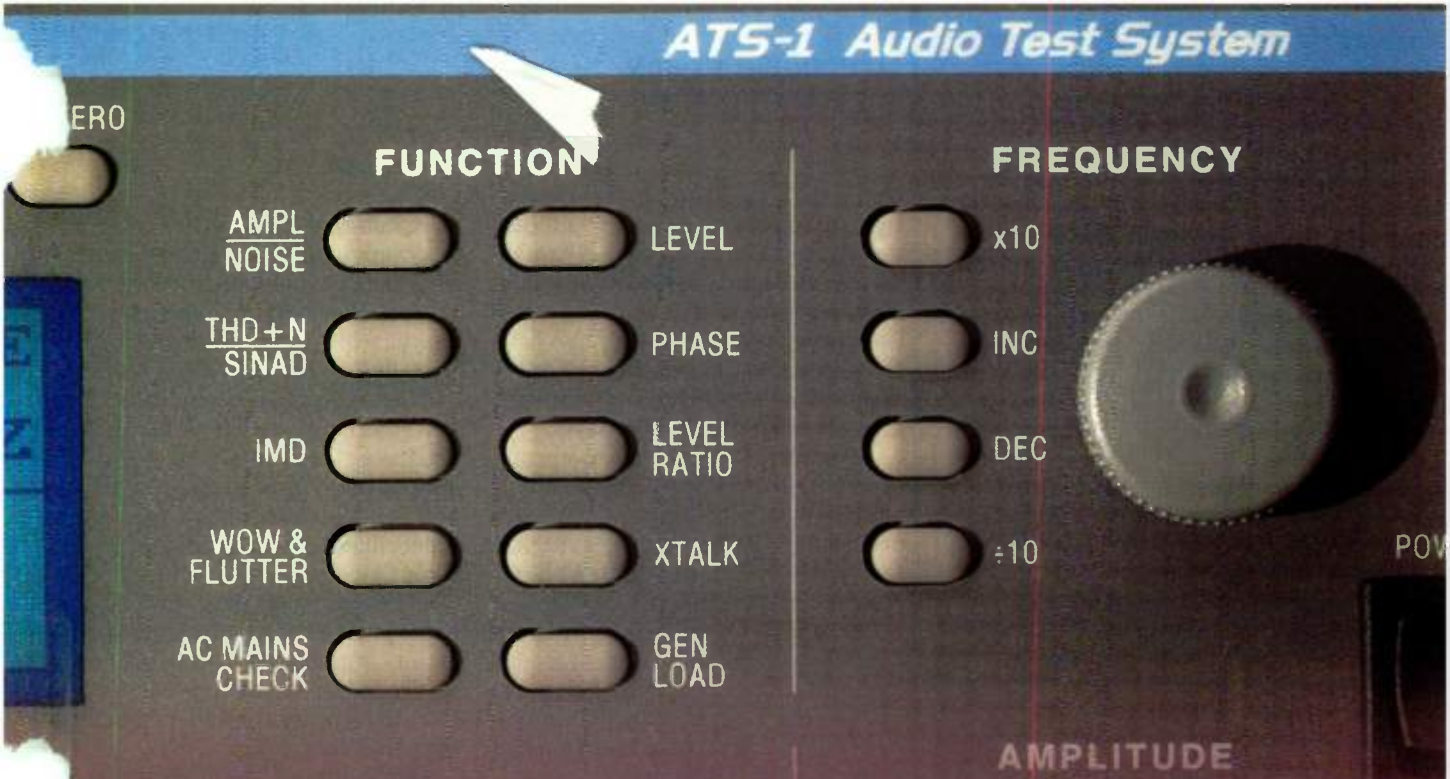

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cording to Moyer. These include Advin, System General, Xeltek, and Hi-Lo Systems. "Programmer companies may have just a plain Jam Player in their programmer. But they also have the opportunity to build a shell or additional user interface capabilities around the Jam file," says Moyer.

Altera has just announced a prototype version of a byte-code Jam. "It essentially reduces file size, improves programming time, and, most importantly, allows Jam to port to 8-bit-microprocessor and microcontroller environments by reducing the memory space required—that is, the memory footprint," Moyer explains. "Now, we have a beta version of an 8051 implementation. It is an area that Jam had been challenged to support."

Norman Taffe, programmable logic marketing manager for Cypress Semiconductor, agrees that the pending standardization of on-board programming based on Jam simplifies the process of complex PLD (CPLD) development. He notes that Jam is a language designed to provide a universal means of describing programming algorithms and data for CPLDs that come from different silicon vendors. With Jam, ATE manufacturers can program CPLDs from multiple suppliers by writing a single piece of software, the Jam Player. Each device vendor is responsible for writing a Jam Composer to create the standard Jam files to program its devices.

Similarly, Jam will ease the implementation of on-board processor-based programming, Taffe says. Instead of writing device-specific algorithms to program each unique CPLD, a Jam Player written for a processor can program any CPLD with a Jam file.

In response to increasing design complexity, CPLD vendors are making device, software, and programming advances that support rapid development efforts at even the highest densities, Taffe says. CPLD architectures are being designed with a focus on pin-locking and speed-locking features that make design iterations fast and easy. CPLD design methods are moving to open languages like VHDL, Verilog, and Jam to support efficient retargeting to multiple solutions.

The first programmer maker to support Jam was Advin Systems Inc. Advin's universal programmer, PILOT-JVP, includes software drivers, which run on Windows 95, and a core Jam Player, which interprets Jam programming files produced by PLD vendors.

More recently, System General Inc. (SG) has begun to support Jam in its products. "After studying the specifications of the Jam language, we were able to offer a Jam solution for both engineering and production," says Don Yang, vice president of marketing. "Our programmers can now program these PLDs directly from the specifications supplied by Altera. This system reduces the lead time currently in place and ensures problem-free development," Yang says.

Depending on the application, S[illegible] provides either a traditional, P[illegible] based Jam algorithm for engineeri[illegible] use, or a high-speed programming (HSP) solution for production applications. The first option is a PC system connected to SG's Turpro Universal or AllWriter programmer with single-socket programming. This is optimal for engineering and laboratory uses.

The HSP solution uses proprietary hardware circuitry operating at nanosecond speeds to eliminate almost all the software overhead and program the devices very quickly. According to SG, the HSP solution has the following advantages compared t[illegible] the typical Jam algorithm:

- programming speed on HSP is 1[illegible] times faster;
- there is no need to connect eac[illegible] programming socket to a PC; and
- HSP/Jam on SG's Multi-APR[illegible] programmer provides asynchrono[illegible] gang solutions for Jam programming.

The Jam language is a freely licensed and open standard. Most of the source code required for the Jam Player is contained in the Jam Device Programming and Test Language Developer's Kit available at www.altera.com. The only software routines required to complete the Jam Player are those needed to access the JTAG chain. To find out more about the Jam Device Programming and Test Language visit the Jam web site at www.jamisp.com.

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Further Readings:

LT Magazine: *The LT1495/LT1496: 1.5μA Rail-to-Rail Op Amps*, June '97, p. 8
DN163: *1μA Op Amp Permits Precision Circuitry.*

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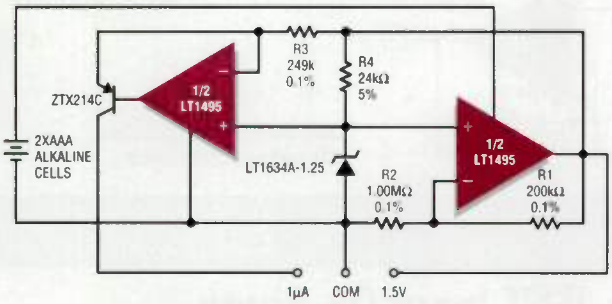

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1.5μA		LT1495	LT1496	375	100	2	100	0.7	2.2 to 36
18μA		LT2178	LT2179	70	250	1.8	97	5	2.3 to 44
45μA		LT1462	LT1463	800	**1.2**	20	100	10	5 to 40
50μA		LT1490	LT1491	800	800	4	106	**20**	2.5 to 44
50μA		LT2078	LT2079	70	250	1.8	106	5	2.3 to 44
75μA		LT1466L	LT1467L	390	3.6nA	7	112	10	2.3 to 16
150μA		LTC1047		**10**	60	**0.05**	**120**	0.2	4.75 to 16
200μA	LT1635			1.3mV	600	7	100	10	**1.2** to 14

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- Common Mode Range:
  0V to 3.5V (on 5V)
- Output Swing (on 5V):
  Low: 9mV Max
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  2.3V to 44V
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  LT2078: 4pA$_{P-P}$
  LT2178: 2.5pA$_{P-P}$

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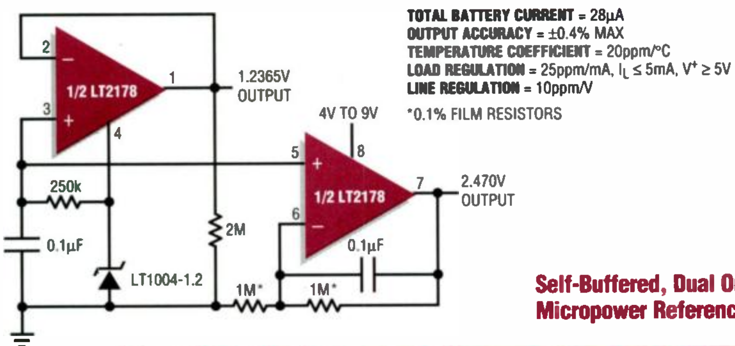

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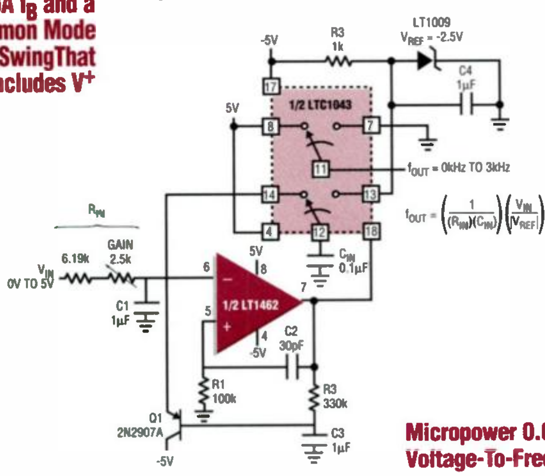

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Further Reading:

DN136: *Micropower Dual and Quad JFET Op Amps Feature pA Input Bias Currents and C-Load™ Drive Capability*

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  LT1462: 45µA Max
  LT1464: 200µA Max
- Common Mode Range:
  Includes positive rail
- Output Swing (on ±5V):
  ±3.5V Min
- Single Supply Range:
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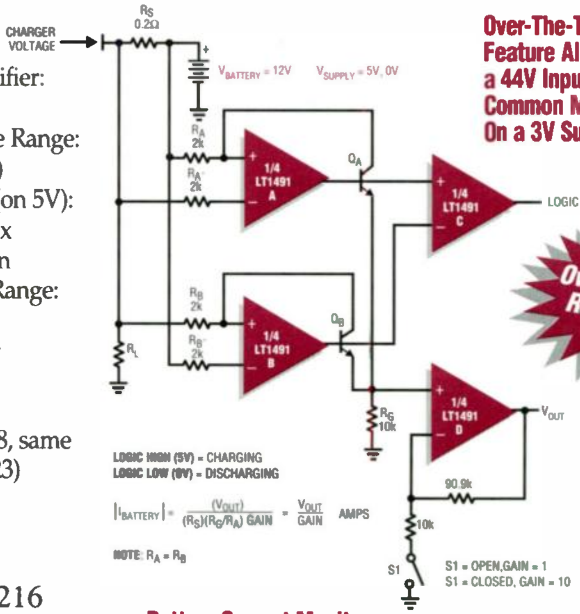
Further Reading:
LT Magazine: *LT1490/LT1491 Over-The-Top Dual and Quad Micropower Rail-to-Rail Op Amps*, Feb. '96, p. 18.

Features:
- I_{SUPPLY}/amplifier: 50µA Max
- Common Mode Range: V^- to (V^- + 44V)
- Output Swing (on 5V): Low: 50mV Max High: 4.95V Min
- Single Supply Range: 2.5V to 44V
- Reverse Battery Protected
- 8-pin MSOP (1/2 size of SO-8, same height as SOT-23)

Circle No. 216



Battery Current Monitor – an Over-The-Top Application

Over-The-Top Feature Allows a 44V Input Common Mode On a 3V Supply

Over-The-Top, Rail-to-Rail

Dual LT1490: $1.95 ea. for 1K-Piece Qty. Quad LT1491: $3.30 ea. for 1K-Piece Qty.

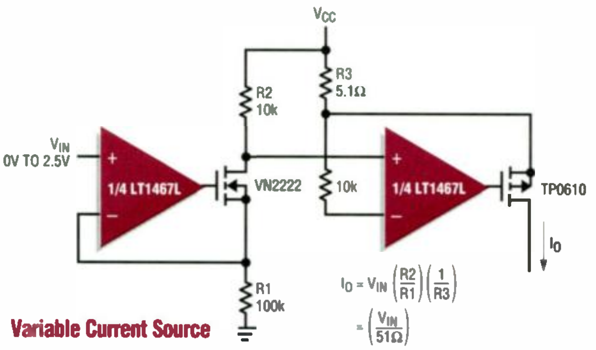
75µA Precision Rail-to-Rail Op Amp

The LT1466L dual rail-to-rail requires only 75µA and delivers 12-bit accuracy from a 3V supply.

Input offset voltage is trimmed at the rails guaranteeing a 390µV V_{OS} Max.

The LT1466L is ideal for battery powered applications and operates from supplies as low as 2.3V.

The quad version, the LT1467L, is also available.



Variable Current Source

Further Reading:
LT Magazine: *New Rail-to-Rail Amplifiers: Precision Performance from Micropower to High Speed*, Dec. '96, p. 18

Features:
- I_{SUPPLY}/amplifier: 75µA Max
- Common Mode Range: V^- to V^+
- Output Swing: (On 5V) Low: 6mV Max High: V^+ -52mV Min
- Single Supply Range: 2.3V to 44V
- V_{OS}: 390µV Max
- CMRR: 83dB Min

Circle No. 218

Eases Design By Guaranteeing a Maximum Value For V_{OS} at Both Supply Rails

Dual LT1466L: $4.15 ea. for 1K-piece Qty. Dual LT1467L: $7.20 ea. for 1K-piece Qty.

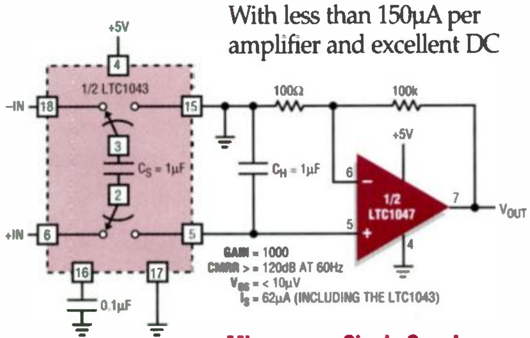
Ultra High Precision at Less Than 150µA

Almost Error-Free DC Performance, Very Little Drift Over Temp and Time

The LTC1047 is a dual, zero drift op amp that has less than 10µV offset voltage and an ultra low 0.05µV/°C Max input offset drift.

With less than 150µA per amplifier and excellent DC precision, the LTC1047 is ideal for battery powered instrumentation.

For rail-to-rail operation with similar DC precision, see the LTC1152. For ±15V operation, the LTC1151 is available.



Micropower Single Supply Instrumentation Amplifier

Further Readings:
AN52: *High Accuracy Instrumentation Amplifier*
LT Magazine: *The LTC1047: New Dual Micropower Zero-Drift Op Amp*, Jan. '93, p. 12.
A Twelve-Bit, Micropower Battery-Current Monitor, Feb. '93, p. 16.

Features:
- I_{SUPPLY}: 150µA Max
- Common Mode Range: 0V to 3.9V (on 5V)
- Output Swing (On 5V): Low: 100mV Max High: 4.8V Min
- Single Supply Range: 4.75V to 16V
- V_{OS}: 10µV Max
- Long Term Offset Drift: 100nV/√mo Typ

Circle No. 220

Dual LTC1047: $4.85 ea. for 1K-piece Qty.

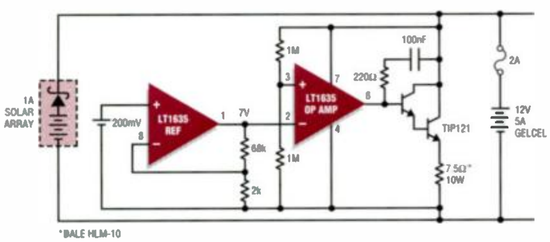
1.2V µPower Op Amp

Includes All Necessary Functions to Design a Compact Precision Battery Level Indicator

The LT1635 includes a rail-to-rail output op amp, a precision reference, and a buffer, yet consumes less than 200µA of supply current.

Because it operates from supplies as low as 1.2V, the LT1635 is ideal for monitoring batteries as they near their full discharge voltage.

The 0.2V on-board reference and the buffer offer flexibility in that the reference voltage can be amplified or the reference amplifier can be used as a comparator.



1A Shunt Battery Charger (I_{DARK} = 230µA, V_{FLOAT} = 14V)

Further Reading:
LT Magazine: *LT1635 1A Shunt Charger*, Aug. '97, p. 22

Features:
- I_{SUPPLY}: 200µA Max
- Common Mode Range: 0V to 4V (On 5V)
- Output Swing (On 5V): Low: 10mV Max High: 4.975V Min
- Single Supply Range: 1.2V to 14V
- V_{OS}: 1.3mV Max
- Drift: Op Amp: 7µV/°C Max Reference: 100ppm/°C Max

The LT1635 is available in 8-pin SO and DIP.

Circle No. 222

LT1635: $1.75 ea. for 1K-piece Qty.

For more details, contact Linear Technology Corporation, 1630 McCarthy Blvd., Milpitas, CA 95035-7417, Web Site: www.linear-tech.com. (408) 432-1900. Fax: (408) 434-0507. For literature only: 1-800-4-LINEAR.

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CPLDs Outshine HDLC Controllers In A Multichannel Design

Programmable Logic Handles Performance Needs While Offering Customization Not Available With Off-The-Shelf Controllers.

BERTRAND LEIGH, MICHAEL FINGEROFF, AND DOUGLAS MORSE
Lattice Semiconductor Corp.

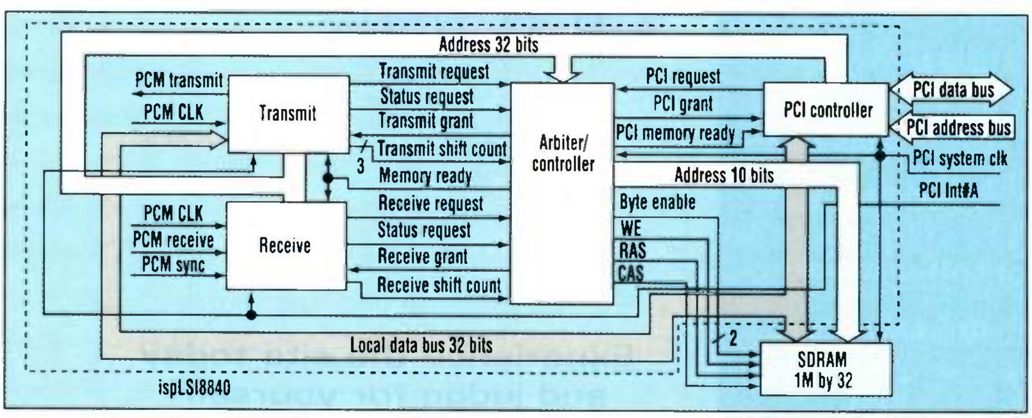
High-level data link control (HDLC) is one of the most enduring and fundamental standards in communications. With its roots in IBM's x.25 protocol, today it is found in a wide range of communications applications. These include leading-edge systems that use xDSL transport, frame relay, and ISDN. Because the HDLC standard also forms the basis of Signaling System 7 (SS7), it's present in most of the worldwide telecommunications network, including cellular base stations.

A variety of HDLC controller chips are available from companies like Rockwell Semiconductor, PMC-Sierra, and Siemens. In addition, microprocessors from Motorola and AMD integrate HDLC controllers on-chip. All of these solutions strive to offer flexibility and high performance. This article describes a complex programmable-logic-device-based approach that fulfills high-performance requirements, while offering a degree of customization that's not available with off-the-shelf products.

Implements OSI Model

HDLC fulfills Level 2 of the Open System Interconnect (OSI) model of communications. It includes an 8-bit begin-frame flag, a 16-bit address, an 8- or 16-bit control field, variable-length payload data, a 16- or 32-bit cyclic-redundancy-check (CRC) field, and an 8-bit end-of-frame flag. HDLC is specified in the ISO/IEC 3309 standard. It provides a convenient method of transporting packet information through a network, whether it's by x.25 transactions, Switch Virtual Circuits (SVCs) in frame relay, ISDN D-channel, call setup in a cellular base-station, or Internet Protocol (IP) on xDSL transport.

The HDLC controller consists of a pulse-code-modulation (PCM) highway



1 This HDLC controller design can functionally divide into four distinct sections: transmit, receive, bus arbiter/SDRAM controller, and PCI interface. External memory is required because large frame buffers are needed to ensure host CPU efficiency. The external memory can also store PCI configuration and HDLC state-machine information.

for the full-duplex HDLC interface, memory controller/SDRAM buffer, and peripheral-components-interconnect (PCI) interface *(Fig. 1)*. The interface accepts 32 full-duplex HDLC frames from a PCM highway interface, which operates at 2.048 MHz. Each channel occupies one 8-bit timeslot on the PCM highway. The SDRAM frame buffer serves as the interface point between the PCM highway and the PCI bus. The configuration registers are also stored in SDRAM. Memory controller performs arbitration between PCI and HDLC accesses and DRAM refresh.

Receive Frame Processing

Receive HDLC frames are processed according to the HDLC protocol, and data octets are submitted to the memory controller to be written into the SDRAM frame buffer. Receive-buffer-full and end-of-frame events generate a PCI interrupt. The host on the PCI bus then reads the interrupt status register (ISR) to determine the source channel of the received frame data. The frame buffer stores frame status and error bits, along with the receive packet data.

From data deposited by the host CPU in the SDRAM frame buffer, the HDLC transmitter creates HDLC frames. Once a buffer has been transmitted, the HDLC controller signals an interrupt. The host CPU then writes more frame data into the transmit buffers.

Using as few CPLD macrocells as possible to implement the large number of HDLC and PCI registers is a major challenge. A brute force implementation of a 32-channel, HDLC state machine and PCI configuration register space could require as many as 5000 macrocells. Normally, one would consider using a high-register-count device beyond the largest CPLDs available in the market.

Because large frame buffers are required for host CPU efficiency, however, external memory is required. This memory can also be used to store PCI configuration and HDLC state-machine information. Taking advantage of the external memory, the HDLC controller is implemented using only one state machine and CRC generator. As each channel is processed, the state and CRC of the current channel is stored in the SDRAM frame buffer. The next channel's state and CRC information is restored from the SDRAM.

The design takes advantage of the time-division-multiplexing (TDM) nature of the PCM data, allowing the high-speed CPLD to reuse the state-machine logic for each channel. The high-speed CPLD is also used for arbitration logic between different functional blocks. This permits the design to be realized in significantly fewer macrocells.

The HDLC interface consists of a PCM Transmit (PCMT), a PCM Receive (PCMR), a PCM Clock (PCMCLK), and a frame sync (PCMF) signal. PCMCLK operates at 2.048 MHz. The PCMT and PCMR signals are time-division multiplexed in a fashion commonly referred to as a PCM highway *(Fig. 2)*. There are 32 8-bit timeslots, numbered 0 to 31. Each timeslot repeats at a 125-µs interval. Timeslot 0 is denoted with the high-to-low transition of the PCMF signal. The PCMF signal will remain low for at least one timeslot.

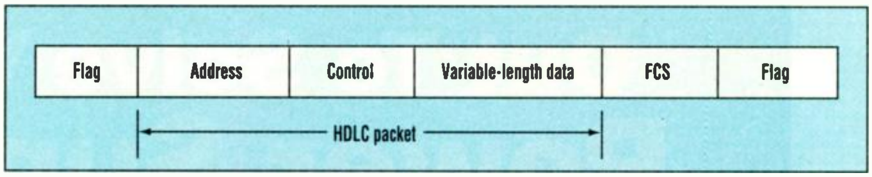
Each timeslot contains one channel of HDLC traffic at 8 bits/125 µs, or 64 kbits/s. Timeslot 0 is assigned as HDLC channel 0. The rest of the timeslots are similarly assigned up to 31.

The HDLC frames that are multiplexed/demultiplexed onto the PCM highway consist of a start flag, address field, control field, variable-length data packet, frame-check sequence (FCS), and end flag *(Fig. 3)*. For this implementation, the address and control fields are decoded by the system software.

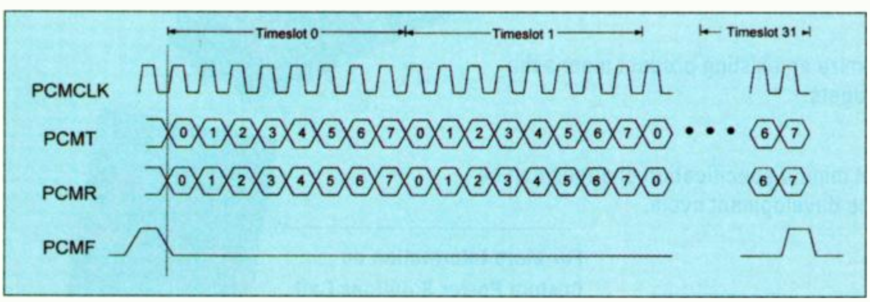
The flag byte (01111110) indicates both the start and the end of an HDLC frame. Zero stuffing/destuffing is performed on the HDLC packets whenever five contiguous 1 bits are transmitted/received.

Memory Map

The HDLC controller 1-Mbyte memory map is divided into two sections *(Fig. 4)*. Lower memory is used to store the PCI configuration, interrupt-service registers (ISRs), channel enable register, command register, databank register, status registers, buffer pointer/state registers, and CRC registers. These registers occupy the first 1536 bytes in memory. The remaining portion of lower memory, 0x00600 through 0x7FFFF, is available for other use. All these registers are located in system SDRAM,



3 The frames that are multiplexed/demultiplexed onto the PCM highway include a start flag, address field, control field, variable-length data packet, frame-check sequence (FCS), and end flag. The flag byte (01111110) indicates both the start and the end of an HDLC frame. In this implementation, the address and control fields are decoded by the system software.



2 The HDLC interface consists of a PCM Transmit (PCMT), a PCM Receive (PCMR), a PCM Clock (PCMCLK), and a frame-sync (PCMF) signal. PCMCLK operates at 2.048 MHz. The PCMT and PCMR signals are time-division multiplexed (TDM) in a fashion commonly referred to as a PCM highway.

except for the interrupt service and command registers, which are mapped into the CPLD.

Upper memory, 0x80000 through 0xFFFFF, provides transmit and receive buffers for all 32 HDLC channels. Each transmit and receive channel has two 4-kbyte buffers. The buffer addresses are aligned so that the address decoding can be done directly from the state and status bits.

Transmit

After system initialization, the HDLC transmitter checks the command register and waits until transmission is enabled. The command register is set/reset by the system software. Once transmission is enabled, the channel enable register is examined to see if each channel is enabled for transmission. If the channel is disabled, the byte value stored in the databank register is transmitted during that timeslot.

Channels are processed sequentially and multiplexed onto the PCM highway. When the HDLC controller sees a channel enabled for transmission, it loads the channel's state, status, and CRC registers from memory *(Fig. 5)*. The state register is decoded to determine which channel buffer and status register are currently active. After each 8-bit timeslot is transmitted, the channel's state, status, and CRC registers are written back into the SDRAM memory.

Once the system CPU has written data into a transmit frame buffer, the CPU sets the Go and Done bits and the number of bytes to be transmitted in the transmit status register. The HDLC transmitter tests the Go bit as it prepares to transmit that channel's data. If a frame transmission is in progress and the Go bit is not set, the HDLC controller sends an end-of-frame delimiter. The controller then sets both the Abort bit in the channel status register and the appropriate bit in the ISR register, generating a PCI interrupt. The transmitter sends back-to-back start and stop flags until more data is available.

The HDLC frame buffers are employed in "ping-pong" arrangement with the HDLC transmitter—reading from one while the CPU writes to the other. The HDLC controller decodes the ping-pong bit in the channel state register to determine the active status register and channel buffer. Bit stuffing is performed as the channel frame data is read from the buffer. After every five consecutive ones, a zero is inserted.

Once the last byte has been read from the buffer, the HDLC controller clears the Done bit in the channel status register and generates a PCI interrupt, indicating that the buffer is now available. The CPU indicates an end of frame by setting the EOF bit in the channel status register. When the HDLC detects the EOF, it transmits the FCS and end-of-frame delimiter. The FCS, a 32-bit CRC, is computed using a 32-bit, linear-feedback shift register.

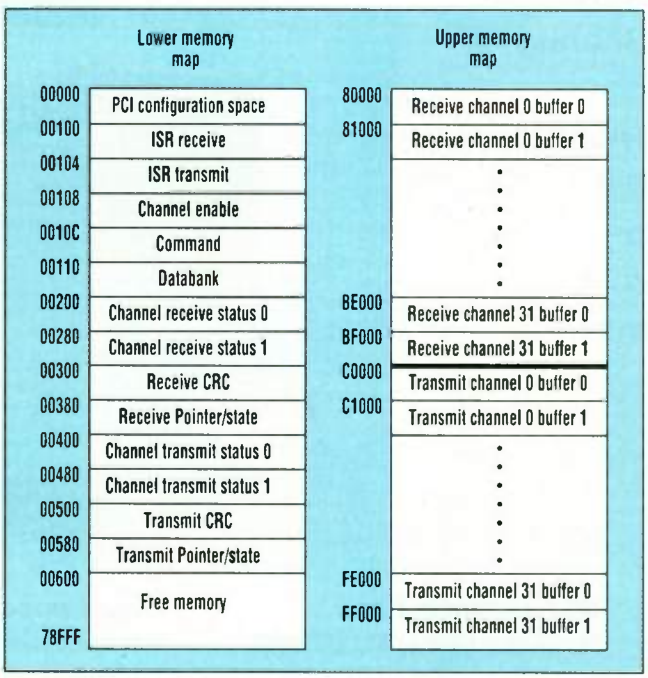
After system initialization, the HDLC receiver checks the command register and waits until reception is enabled *(Fig. 5, again)*. The command register is set/reset by the system software. Once reception is enabled, the channel enable register is examined to see if each channel is enabled for reception. When the HDLC controller sees a channel enabled for reception, it loads the channel's state, status, and CRC registers from memory. The state register is decoded to determine which channel buffer and status register are currently active. After each 8-bit timeslot is received, the channel's state, status, and CRC registers are written back into the SDRAM memory.

Receiver Does Demultiplexing

The receiver demultiplexes the PCM highway and processes the channels sequentially. After a channel is enabled, the receiver waits for the start-of-frame (SOF) delimiter. Once SOF is detected, the receiver begins writing the channel data into the receive buffer. Bit unstuffing is performed on the incoming data stream, along with CRC calculation.

When the HDLC receiver has filled a frame buffer, it sets the Full bit in the channel status register. The receiver also toggles the ping-pong bit, indicating that the alternate frame buffer should be used. If the EOF delimiter is also detected, the EOF bit is set. A CRC and frame-length check is performed. If a CRC error is detected, the CRC bit is set as well. In addition, if the frame is either too long or too short, the long and short bits are set. If the transmission was error-free, the OK bit is set. A PCI interrupt is then generated, indicating that the buffer must be emptied.

The bus arbiter/SDRAM controller interfaces directly with the SDRAM. It generates the row-address-strobe (RAS) and column-address-strobe (CAS) signals during memory



4. The HDLC controller 1-Mbyte memory map is divided into two sections. Lower memory is used to store the PCI configuration, interrupt-service registers, channel enable register, command register, databank register, status registers, buffer pointer/state registers, and CRC registers. Upper memory is used for transmit and receive buffers for all 32 HDLC channels.

accesses, performs refresh cycles, and arbitrates between memory requests from the HDLC transmitter, receiver, and PCI host. Both the arbiter/controller and the SDRAM operate at the 33-MHz PCI bus speed.

All memory accesses are made through the SDRAM controller. Because the SDRAM supports burst mode, the arbiter/controller supports different types of bus requests to optimize available bus bandwidth. Status requests are given the highest priority during arbitration.

Within a single HDLC timeslot, up to 17 possible memory accesses can occur. This includes the loading and storing of channel enable, state, status, and CRC registers, as well as frame data.

The PCM highway, 2.048-MHz data rate, however, is relatively slow compared to the 33-MHz PCI bus speed. Each HDLC timeslot is approximately 3096 ns. At the PCI bus speed, this translates to up to 103 possible memory accesses. By allowing the memory accesses to occur without any priority assigned, there could be more than 17 page faults for every HDLC timeslot. This would leave very little available time for the PCI host to load and unload the transmit/receive buffers.

By assigning the highest priority to status/state/CRC register requests, any page faults can be avoided while loading and storing these registers from memory. Memory requests are prioritized in the following order: status request, refresh, Rx/Tx request, and PCI request. Memory requests are made by asserting the appropriate request signals. If a request is accepted, the arbiter/controller grants the bus to the requester by asserting the appropriate bus grant signal. If a refresh cycle is in progress during a memory access, the arbiter/controller will insert wait states.

The PCI host, HDLC transmitter, and HDLC receiver all interface to the SDRAM using the same address, data, and write-enable buses. This is easily accomplished in a CPLD with internal tristate buses. For this design implementation, the address bus is 20-bits wide, the data bus is 32-bits wide, and the write enable bus is 1-bit wide.

PCI Interface

For a PCI interface, a CPLD must have PCI compatible I/Os, which permit the PCI bus to be driven directly. The CPLD must also have a sufficient number of macrocells to implement a PCI master interface, along with the HDLC transmitter/receiver and arbiter/SDRAM controller. A minimum of 47 signals must be supported to implement a PCI master.

The PCI specification requires the first 256 bytes of lower memory to be reserved for the PCI configuration space. All PCI-compliant devices must support the vendor ID, device ID, command status, revision ID class code, and header-type fields. The PCI controller initializes these PCI registers during power-on reset. To indicate that INT#A is enabled, the PCI interrupt-pin register is also initialized.

The ISRs are set by the HDLC controller during transmit/receive. They indicate whether the buffer is empty or full, or if a frame must be aborted during a transmission error or buffer time-out. The outputs of all the ISRs are OR'd together and drive the PCI Int#A pin. The PCI host responds to interrupts by checking the ISRs and servicing the appropriate channel. After the channel interrupt has been serviced, the PCI host clears the appropriate bit in the ISR.

CPLD Logic Utilization

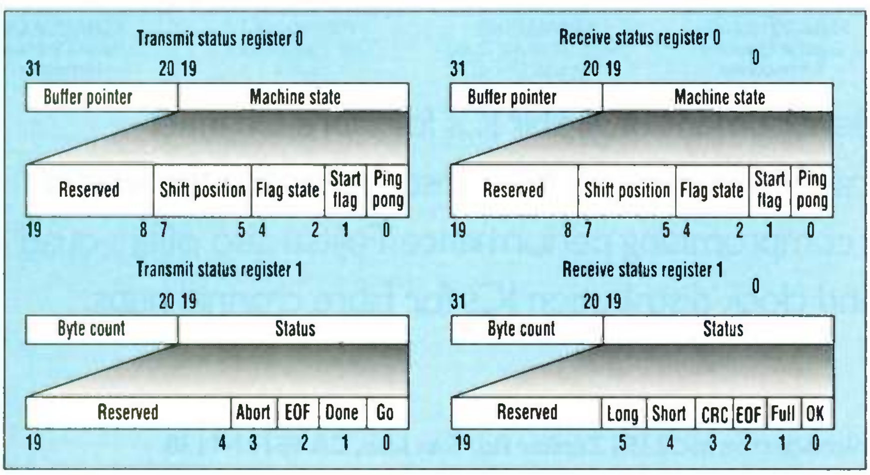
The CPLD macrocell-utilization requirement can be divided into three parts: HDLC transmit/receive, arbiter/SDRAM controller, and PCI master interface.

A large percentage of the macrocell utilization for the HDLC controller is devoted to the Channel Enable, status, state, CRC, and ISR registers. The number of macrocells used in the transmit and receive state machines is small in comparison. It is not practical to implement a different set of these registers for each channel, nor is it necessary. Because the PCM highway data rate is relatively slow, and the channels are processed sequentially, the same set of transmit/receive registers can be used for each channel.

Approximately 450 macrocells are used for the HDLC controller implementation. The arbiter/SDRAM controller takes up approximately 128 macrocells, which includes 20-bit memory-decode logic and a refresh state machine, as well as tristate bus arbitration.

The PCI master interface can be implemented in approximately 128 macrocells. This includes the minimum signals needed for a PCI master and the initialization of the registers in the PCI configuration space. A total of 706 macrocells are required for the CPLD implementation.

The I/O utilization is minimal, due largely to the implementation of address and data buses with the CPLD's internal tristate buses. The PCI master interface requires 47 I/Os, plus one for the Int#A to interface to the PCI



5 When the HDLC controller sees that a channel is enabled for transmission or reception, it loads the channel's state, status, and CRC registers from memory. The state register is decoded to determine which channel buffer and status register are currently active.

bus. For the HDLC interface, the HDLC transmitter/receiver requires four I/Os. Finally, the SDRAM controller requires 47 I/Os to interface to the SDRAM. This includes the 32-bit SDRAM data bus. In total, 99 I/O cells are needed in the CPLD.

The implementation example is shown in the Lattice ispLSI8840. There are a total of 840 macrocells and 312 I/O cells with register capability. The example employs the PCI drive capability and the 108-bit-wide tristate bus feature of the ispLSI8840 to implement the HDLC controller.

For this given implementation, approximately 85% of the macrocells (706/840) and 32% of the I/O pins (99/312) on the ispLSI8840 are used. This leaves room for customization and additional logic implementation for the system. In-system programmability (ISP) of the CPLD makes the modifications and customizations—such as reconfiguring the buffer sizes by manipulating the SDRAM configuration, the arbitration priorities, and the HDLC timeslots—as easy as rewriting software via the VHDL code.

The hardware reconfiguration is handled by simply downloading the new fusemap through the four- or five-wire standard JTAG interface. The JTAG port also provides access to the on-chip boundary-scan test registers.

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***MICHAEL FINGEROFF** is an applications engineer at Lattice Semiconductor. He received his BSEE and MSEE from Temple University, Philadelphia, Pa., where he specialized in microprocessor and DSP technology.*

***DOUGLAS MORSE** is telecommunications product project planning manager for Lattice Semiconductor. He Holds a BS in Computer Science from Northern Arizona University at Flagstaff, and an MBA from the University of San Diego, Calif.*

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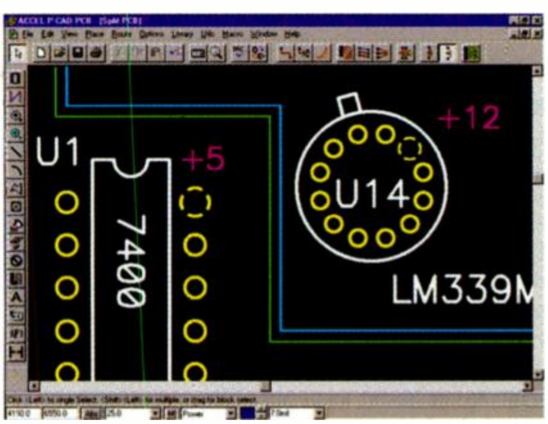

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Programmable Logic Speeds Prototypes Into Production

To Reap The Benefits Of More Feature-Rich PLDs, Designers Must Integrate The Right Device Into Their Development Cycle.

TOM TROKSA and STEVE DABELL
Packet Engines Inc., P.O.
MARTIN S. WON,
Altera Corp

System design no longer involves simply seeing a single vision through to completion. It represents the struggle to successfully join together several evolving technologies and standards. Even the development tools, circuit fabrication options, and software development tools needed to design systems are evolving. But somehow, designers must complete their projects faster than ever before to meet market demands.

One of the system designer's assets that has emerged as an increasingly useful tool in dealing with these issues is programmable logic. With programmable logic comes many decisions—like which device to use, how to integrate it into an existing design flow, and how to plan the development cycle to maximize its effectiveness. To illustrate the use of programmable logic in system design, we'll examine a Gigabit Ethernet device recently developed by Packet Engines Inc.

The device is a PowerPC-compliant system controller that is the heart of the PR5200, a high-performance wire-speed router designed for the core of enterprise networks. Such devices are replacing traditional routers, whose low performance makes them system bottlenecks. Wire-speed routers perform complex routing functions in custom ICs, making them significantly faster and more cost-effective. One of the major reasons is the system controller, which supplies massive amounts of system bandwidth between the PowerPC and the Gigabit Ethernet switch fabric.

Higher Density, More Flexibility

Familiar to many designers in their role as interface or glue logic, complex programmable logic devices (CPLDs) have undergone many improvements in complexity (density) and flexibility. These advances make it possible, and even desirable, to implement large subsystems on one chip. Add to this the historic advantages of CPLDs (flexibility and rapid design turn-around), and you can apply programmable logic in a wider array of design situations than ever before.

The controller examined here was prototyped in a CPLD. The design supports a 6-Gbit/s memory bandwidth, a 2-Gbit/s direct memory access (DMA) receive channel, a 2-Gbit/s DMA transmit channel, an industry-compliant I^2C (inter-IC) interface, and a high-performance 32-bit local bus. When coupled with a local-bus controller, the engine controls the entire computer system. Functionally, the Gigabit Ethernet controller integrates two independent, synchronous DRAM controllers; a receive DMA channel; a transmit DMA channel; a 32-bit local bus; an I^2C controller; an interrupt controller; and a system-configuration controller *(Fig. 1)*.

An internal, multimaster/multislave parallel-bus structure connects six independent execution units, and allows up to seven concurrent transactions. An internal arbiter coordinates the switching and interconnection of the system execution units. Each execution unit supports a multidepth pipeline that allows for the execution of at least two concurrent transactions within each execution unit.

We estimated that the logic of this design would take about 100,000 gates,

WRH

purposes. There are no hard and fast rules for choosing the right pin count; some designers prefer a buffer of anywhere from 5% to 10% extra I/O pins.

As estimated earlier, the Ethernet controller subsystem required roughly 450 I/O pins and about 100k gate-array gates (the actual gate total will be reviewed later). An additional 4-kbytes of internal single-port memory are needed for the buffers. Among the embedded-memory PLDs, the EPF10K130 in the Altera 10K family appears to be a good fit. It offers up to 130,000 usable gates (including 32 kbits of RAM) and 470 I/O pins.

An added advantage is the pin-compatibility between members of the FLEX 10K family. Several PLD suppliers offer this capability, which is useful not only for flexibility with your present design, but also for planning upgrades or cost reductions. Upgrades presumably would require more logic and memory resources while using the same I/O. Accordingly, the EPF10K250, with nearly twice the logic and memory resources as the EPF10K130, could be dropped into the same socket, because it has the same pinout and package options.

Will It Go With The Flow?

Before committing to a specific PLD, look at how it fits into the existing design flow. For most devices, this is not a problem in principle, but the exact details of integrating a PLD into the flow of capture and verification tools will vary depending on the company, and possibly the family, of devices. Describing all the possible variations that exist could fill another article, so we'll focus on the design of the Ethernet controller, noting the areas that will likely apply to all design flows regardless of tools and methodology.

As with most ASIC design flows, the design of the controller begins with design capture using an industry-standard hardware description language. Following the successful implementation and verification of the design at an RTL level, the HDL is input into a synthesis tool to create a gate-level representation targeted toward a specific technology. From there, the physical design of the implementation is conducted which, when targeting CPLD technology, is the responsibility of the logic designer as opposed to the silicon provider *(Fig. 2)*.

Programmable devices (especially CPLDs) require device-specific design compilation tools that are provided by the vendor. These tools can typically be used either standalone exclusively to develop PLD designs, or together with gate-array design tools, like those from Cadence and Synopsys, as part of a larger flow.

In this design, the Synopsys synthesizer was directed to produce a netlist that served as the input to the programmable logic tools. The synthesis process involves the creation of a set of scripts with a specific synthesis script associated with each Verilog design file. A bottom-up strategy produces gate representations of each synthesizable leaf-level module.

The gate-level output files produced by each of the leaf-level synthesis scripts are stored in a common directory. In the bottom-up synthesis strategy, the gate-level design files are connected (using scripts within the Synopsys environment) at higher levels of the hierarchy, until a top-level design file representing the entire design structure as a hierarchical gate-level netlist is created. This file is then tested against the original test fixture before being transferred from the Synopsys environment to the remaining tools as an Electronic Design Interoperability Format (EDIF) hierarchical netlist. It is this netlist that is transferred to the physical place-and-route tools. Here, the physical place-and-route tool was the Altera MAX+PLUS II compiler.

Hierarchical EDIF is useful because it allows the designer to manage the place-and-route timing/area requirements with constraints assigned to any module within the hierarchy, at any level. MAX+PLUS II provides a detailed design hierarchy viewer/editor that serves this purpose well. Logic assignments that will carry over to MAX+PLUS II can also be made from within the Synopsys synthesis tool environment (in the case of Design Compiler, it requires entering commands at the dc_shell prompt).

The PLD vendor's own tools can provide much more accurate post-

route timing information than can be provided with a pre-route estimate from the logic synthesis tool. Although this post-route information can be imported into the Synopsys static-timing tool for analysis, in this example, the MAX+PLUS II static-timing analyzer was used to verify the timing of critical paths. To check the functionality of the design, a Verilog file that includes the timing information can be exported from MAX+PLUS II. This file can then be imported into Cadence's gate-level simulator, Verilog-XL.

To cut time-to-market, separate design groups developed the controller's logic in parallel with the pc board and the embedded software. Although programmable logic is designed for flexibility, in many cases, a designer can reap benefits from intelligent placement of I/O pins, depending upon the device architecture and the needs of the design. In this controller, all the pins were expected to be used, so there would be no opportunity to change the pinout after the pc board was completed.

Accordingly, designers identified the I/O buses early that require the most stringent timing, and placed them on pins that corresponded to "rows" in the FLEX 10K device. This placement is best because the FLEX architecture employs rows and columns of interconnect. A simple observation of the FLEX architecture reveals that more I/O pins and logic resources are associated with a given row than with any column.

One implication of this structure is that for applications in which many data buses are passed through several levels of processing, it makes sense to orient these signals along rows. With this I/O placement scheme, the designer can lay out the board before the Verilog code is synthesized, and still achieve the desired timing. The 20 "spare" I/O pins in the device were brought out to probe points for diagnostic use later in the prototyping stage.

Incremental Releases

By incrementally releasing the PLD design, the team allowed early hardware/software integration using strategic subsets of the final PLD logic. That allowed designers to functionally check out portions of the logic as the design progressed, reducing the chance that the final circuit wouldn't work. For the level of complexity in the Ethernet controller, four prototyping releases, the fourth being the first production-ready release, were made.

The first release, which took about five weeks to develop from specification to completion, contained the PowerPC interface, memory controllers, and the superscalar bus fabric. This release allowed software developers to get to work quickly with their PowerPC emulator, testing routines for transactions between the PowerPC and its DRAM.

A second release (about a week later), added the I/O bus, which offered access to several data sources in the overall system. These included a UART (to provide a monitor interface), flash memory, and a PCMCIA port. With this release, the software team developed code for the PowerPC (a 603 in this example) to talk to the data sources. One method is to boot from the flash memory or the PCMCIA port, and load the corresponding instruction sets into the DRAM.

With the inclusion of PowerPC-to-DRAM routines, the software team could focus on developing routines that deal with the new data sources. A few weeks later, a more-complete third version added the DMA engine and the single-port RAMs for communicating between the external switch fabric and the PowerPC.

The final (fourth) release followed a few weeks after. It contained minor enhancements, and permitted the software team to perform intensive software testing.

Following the formal release of the completed design in PLD format, the the team began retargeting it to gate-array technology. The only design difference between the two is the structure of the single-port memory associated with the DMA engines. To manage this situation, the design was configured from its conception to isolate the logic implementing the interface to the memory into a single module within the design hierarchy. That ensured a relatively smooth changeover. But, the timing and functionality of this portion of the design had to be be carefully scrutinized during Verilog simulation and testing of the actual gate-array design. The reason is that it's the one area in which the PLD logic deviates from the gate-array logic.

One of the greatest benefits of using programmable logic is the ability to test real hardware under actual operating conditions. This capability proves the design, and potentially verifies some of its more difficult-to-simulate aspects, such as system timing. The testing was performed in parallel with the completion of the gate-array design, so that any required changes could be made before building the first gate-array samples.

Testing Performed Also

While the team was retargeting the controller in Verilog to produce the gate-array version, it also subjected the PLD implementation to literally billions of Ethernet packets. At this time they fully sounded out the design and tested its capabilities. Simulating the controller design within the context of the physical board, and using the actual software on a physical PowerPC 603 provided a very powerful verification platform. Additional operating insights regarding the logic are also possible, as the spare I/O pins were used to form a probe bus.

A note on the time it takes to compile a PLD design: As with gate arrays, times will vary with the size and complexity of the design and will definitely be a factor the overall design-cycle efficiency. In this project, compilation times for the early releases were about 20 minutes (using MAX+PLUS II on a Sun UltraSPARC 2-based workstation). The final releases required compile times of up to six hours.

The final production version of the controller, when implemented in the EPF10K130, occupied 82% of the logic resources, and all of the memory resources of the device. (A comment on gate counts: Altera documentation states that the EPF10K130 provides from 82 to 211 kgates, depending on the logic is implemented, and how the memory structures are used.) In comparison, a gate-array version required 95 "gate-array" kgates and two 2-kbyte single-port RAMs. So by the measure of this design, the total logic elements in an EPK10K130 could provide a maximum of about 115 kgates, and the EABs could provide a total of 4 kbytes of memory.

Early releases of a product, thanks to the use of programmable logic, provided extra months of market penetration and revenue generation that would have been lost if a gate-array-only strategy had been employed. Furthermore, the PLD-based version provides an invaluable verification platform for testing the logic design in an actual environment prior to converting it to a semicustom implementation. In addition to mitigating the risk associated with releasing a complex system to custom silicon, the programmable logic approach provides a contingency position just in case something delays the release of the gate-array or ASIC version.

Programmable logic and EDA tool vendors continue to make great strides in integrating PLDs into the familiar gate-array design flows. Moreover, future generations of PLDs will offer the system designer even more gates and memory, allowing direct system upgrades. For example, a future version of the controller will employ a FLEX 10KE device, which offers a higher memory-to-logic ratio than previous FLEX 10K family members. As a result, the FLEX 10KE solution in the same pinout and package could support deeper transmit and receive buffers, improving data bandwidth.

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Circle 520

Quad Op Amp Performs Matching Of Discrete NPN Transistors

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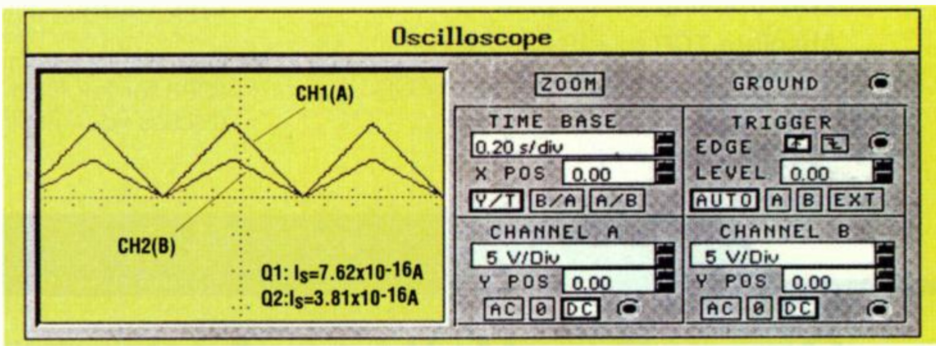
Many discrete analog circuits require precisely matched transistor pairs. Logarithmic and antilogarithmic functions, differential amplifiers, and multipliers possess inherent matching features generally not obtainable with discrete components. The most common method of matching discrete components is by using a curve tracer. However, this is a tedious and expensive method. The circuit shown is an inexpensive circuit that can be used to match two discrete transistors based on their saturation current (I_S) *(Fig. 1)*.

If two transistors are operated at the same base-emitter voltage, then the ratio of their collector currents is equal to the ratio of their saturation currents:

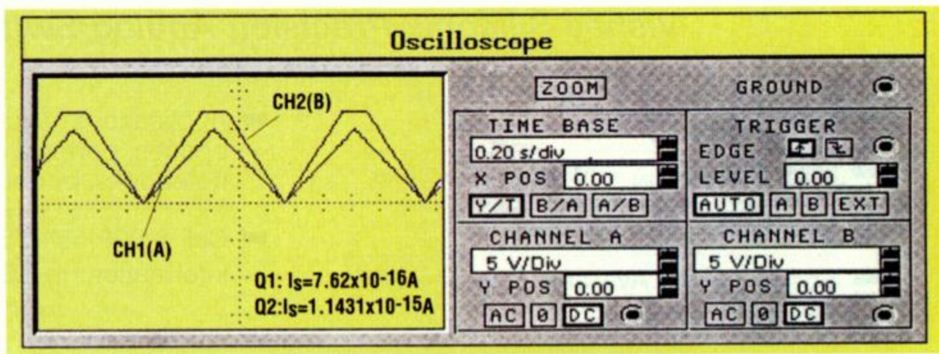
$$I_{C1}/I_{C2} = I_{S1}/I_{S2}$$

If the collector currents are equal, then the saturation currents will be equal and the pair will be closely matched. This assumes that the V_{BE}, V_{CE}, and V_{CB} of each transistor are identical. In Figure 1, Q1 is connected in the feedback path of U1A. The summing junction of the op amp forces the collector voltage to zero (within the offset voltage specification of the OP-497, or 50 µV).

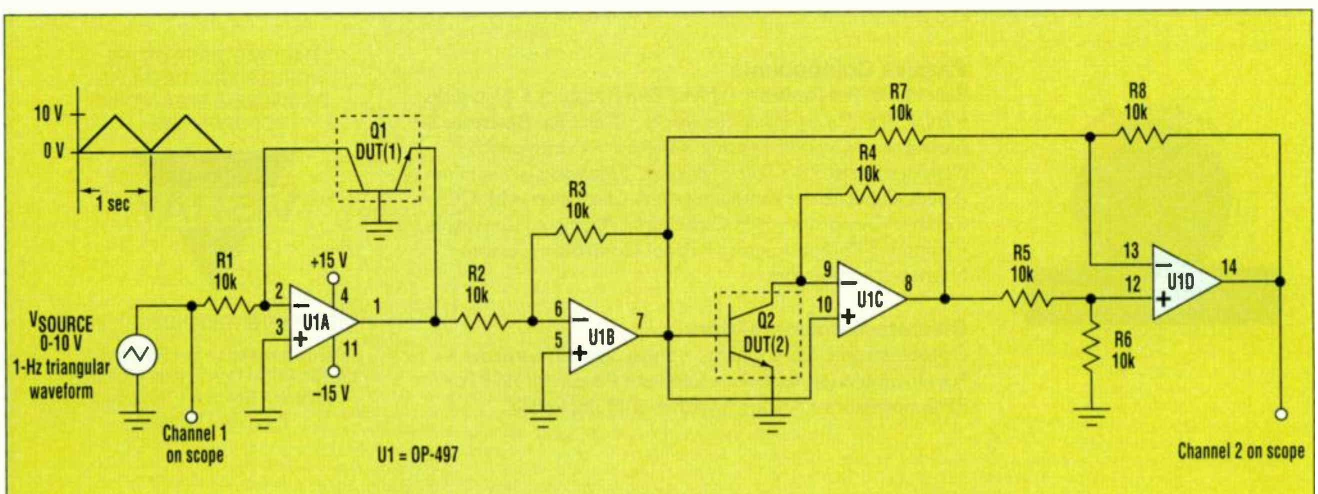
With the base connected to ground, the collector-base voltage is zero. The collector current of Q1 is set by R1 and the input voltage, which is a unipolar 0- to 10-V triangular, 1-Hz



2. Shown are the waveforms that result when I_{S2} is 50% smaller than I_{S1}.



3. Depicted here are the waveforms that result when I_{S2} is 50% larger than I_{S1}.



1. This inexpensive circuit can be used to match two discrete transistors, Q1 and Q2, based on their saturation current, I_S.

waveform. This sweeps the collector current of Q1 from 0 to 1 mA, independent of Q1's beta. The output of U1A is the inverted V_{BE} of Q1, so U1B is used to change the sign of this voltage. This V_{BE} is applied to the base of Q2, which is connected as the antilog element of U1C. The noninverting input of U1C is connected to the same V_{BE}, which forces the collector voltage of Q2 to track its base voltage (again, within the offset voltage limits of U1), forcing the collector-base voltage of Q2 to zero.

If the saturation current of Q2 is matched with the saturation current of Q1, the output voltage of U1C will be the source voltage plus the base-emitter voltage of Q1. U1D subtracts this V_{BE}, leaving a voltage proportional to the collector current of Q2. If the saturation currents are equal, the output voltage of U1D will be identical to the source voltage.

Figure 2 shows the waveforms that result when I_{S2} is 50% smaller than I_{S1}, while Figure 3 depicts the results when I_{S2} is 50% larger than I_{S1}. Good performance of the circuit depends on close matching of all resistors.

A byproduct of the circuit configuration is the ability to measure or display the I_C versus V_{BE} characteristic of Q1. With the source voltage connected to channel 1 and the output of U1B connected to channel 2, set the oscilloscope in the X/Y mode with channel 1 on 5 V per division and channel 2 on 200 mV per division.

IFD WINNER

Samuel Kerem, Infrared Fiber Systems, 2301-A Broadbirch Drive, Silver Spring, MD 20904; e-mail: samuelkerem@juno.com. The idea: *"Use A Tiny Microcontroller With A Large Keypad"*. November 2, 1997 Issue.

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Circle 521

Low-Voltage Oscillator Features Increased Spectral Purity

EDUARD BERTRAN AND GABRIEL MONTORO
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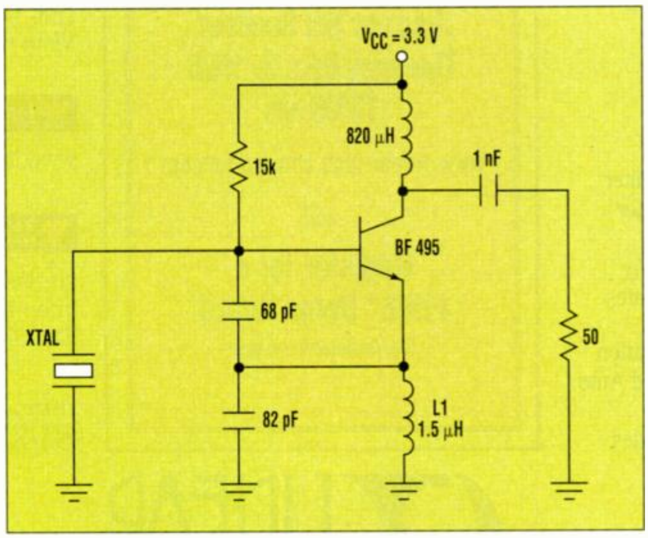
A common problem in crystal sinusoidal oscillators is the excitation of unwanted modes of the quartz crystal that degrade the spectral purity of the oscillator. This problem is significant in overtone crystals, particularly if the oscillator is intended for low-voltage applications. In this case, there's a compromise between the operating point of the transistor and the drive level of the crystal. If the operating point of the transistor produces a low current level in the crystal, it can't reach the minimum energy for correct vibration startup. The proposed circuit is a simple modification of a Colpitts oscillator, in which the transistor's emitter is grounded through an inductor *(see the figure)*.

The inductor L1 increases the voltage gradient in crystal plates during the transient response of the oscillator (after power is applied), facilitating the crystal vibration startup. A detailed analysis reveals that, in overtone crystals, the impedance is inductive at the crystal fundamental frequency, whereas this impedance becomes capacitative at the desired overtone. Therefore, the desired overtone oscillation will be easily started and the undesired fundamental frequency perturbations are avoided. In addition, the overall transfer function has a low-pass behavior that eliminates higher harmonics in the oscillator output.

This circuit has been used in the production of a 27-MHz oscillator for an industrial communication application. Without the proposed modification, 23% of the oscillators failed, with the failure rate noticeably dependent on the production series (manufacturer reference) of the crystal. With the modification shown, practically all of the oscillators run correctly. On the other hand, the total harmonic distortion (THD) of the oscillator shown, when L1 is replaced by a 4.7k resistor (classical Colpitts oscillator), is 28%. With the proposed modification (inductor L1), the distortion is reduced to 0.32%. In all of these measurements, the power supply was 3.3 V.



A simple modification of a Colpitts oscillator, grounding the emitter through inductor L1, improves the low-voltage startup performance of overtone crystal oscillators, as well as enhancing the spectral purity.

Circle 522

Design A 3-Pole, Single Amplifier, LP Active Filter With Gain

CARL RUTSCHOW
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Designs for single-amplifier, two-pole, low-pass, active filters with gain are relatively common in the literature, but little information is available for such filters with three poles. Determining the component values for a three-pole filter requires solving three simultaneous equations with three unknowns. These equations are rather messy, particularly for gains other than one. Therefore, the usual cookbook solutions for this filter have typically been done at a gain of one. However, with the advent of programs that iteratively solve such equations for their roots, it becomes relatively easy to derive a filter solution for any value of gain.

The general equation for a three-pole low-pass filter is:

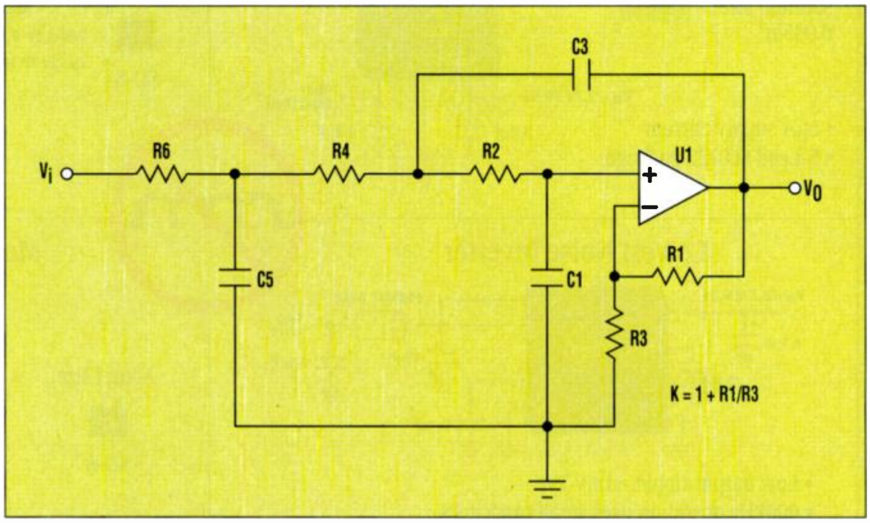
$$\frac{V_O}{V_I} = \frac{A0}{A3s^3 + A2s^2 + A1s + A0}$$

The filter characteristics are determined by the values for A0, A1, A2, and A3, and are shown in Table 1 for several common filter types. The values for the desired filter type are plugged into the transfer function equation of the three-pole active filter circuit *(Fig. 1)*, and then the equation is solved to derive the circuit component values.

The equations to solve for the circuit component values using Mathcad 5.0 are shown in Figure 2. The values at the top are the initial variable values, including the filter gain and frequency response, that the program uses to solve the equations. The program holds these values constant, except for those in the "Find" equation.

To determine the filter components, set the variables A1, A2, and A3 at the top equal to the designated values for the desired filter type from the table given. Because there are six component variables and only three independent equations, the usual procedure is to initially set the three resistor values equal to each other and solve for the capacitor values. The example shown is for a Butterworth filter with a gain of 3, a corner frequency of 1 kHz, and resistor values of 10 kΩ. The bottom "Find" equation generates the calculated capacitor values (in farads).

These calculated values then can be optimized to standard available component values, as is typically desired.



1. For this three-pole active filter, the filter characteristics provided in the table are plugged into the transfer function equation shown. The equation then is solved using MathCad 5.0 to derive the circuit component values and optimized to use standard component values.

Mathcad
3-Pole Active Filter With Gain
K is gain, f is frequency

Initial Values

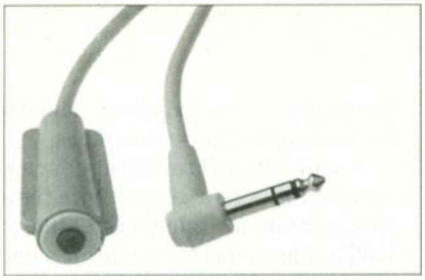
R2 := 10000   C1 := 1•10^{-8} A1 := 2   A0 := 1
R4 := 10000   C3 := 1•10^{-8} A2 := 2   K := 3
R6 := 10000   C5 := 1•10^{-8} A3 := 1   f := 1000

Given

A1 = ((1 - K)•(R6 + R4)•C3 + R6•C5 + (R2 + R4 + R6)•C1)•2•π•f
A2 = ((1 - K)•R6•R4•C5•C3 + R6•(R2 + R4)•C1•C5 + R2•(R6 + R4)•C1•C3)•$(2•π•f)^2$
A3 = R6•R4•R2•C5•C3•C1•$(2•π•f)^3$

$$\text{Find(C1,C3,C5)} = \begin{bmatrix} 1.37833 \cdot 10^{-8} \\ 9.82338 \cdot 10^{-8} \\ 2.97747 \cdot 10^{-8} \end{bmatrix}$$

2. These equations are used to solve for Figure 1's circuit component values.



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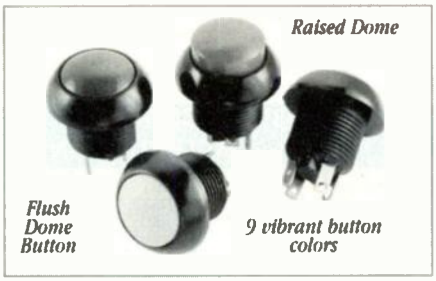

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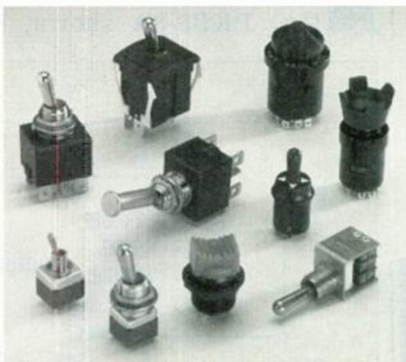

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FILTER TYPE	FEATURES	A1*	A2*	A3*	CORNER ATTENUATION
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Chebyshev -1dB Ripple	Equal 1 dB passband ripples and rapid cutoff	2.52071	2.01164	2.03537	1dB
Chebyshev -3dB Ripple	Equal 3 dB passband ripples and very rapid cutoff	3.70466	2.38334	3.99058	3dB
Optimal	Rapid cutoff and monotonic in passband	2.35529	2.27036	1.7331	3dB
Bessel	Approximates Gaussian response. Minimizes phase delay distortion	1	0.4	.06667	0.84dB
Paynter	Excellent time domain response. Minimal overshoot	3.2	4	3.2	10.4dB

*Normalized to A0 = 1

To do this, substitute the standard capacitor values closest to the calculated values for the values of C1, C3, and C5 at the top. Then calculate the revised resistor values by replacing Find(C1, C3, C5) with Find(R2, R4, R6) at the bottom. The closest standard values to these calculated resistor values, as well as the standard capacitor values, will be used in the circuit. The nominal response now becomes generally as close to the desired frequency as can be obtained using standard component values.

A particular filter's frequency response will, of course, vary with the actual component tolerance values, as well as the selected amplifier's gain-bandwidth. The circuit is somewhat sensitive to the actual value of gain (K), so its variation should be given particular attention. An easy way to determine the circuit response is with a Spice-type circuit simulator program, such as Pspice, ICAP, or Electronic Workbench. Doing a Monte Carlo analysis with these programs can give the response variation for a random selection of component tolerances.

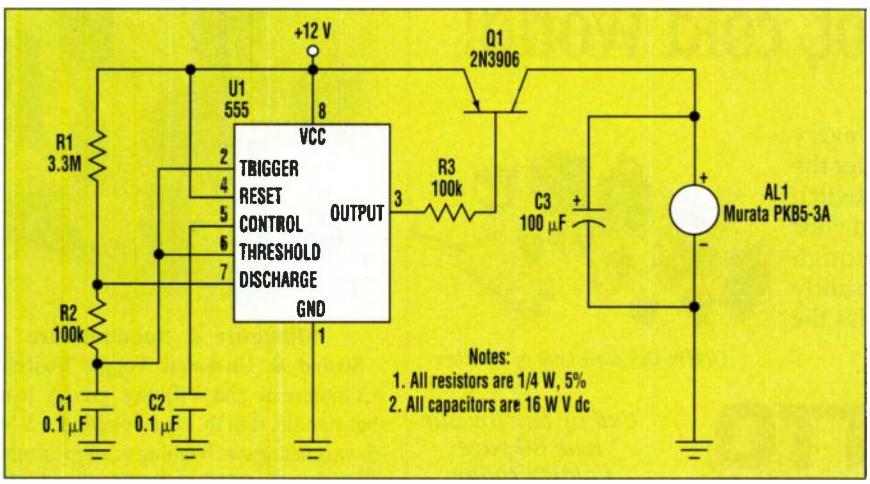
Note: If Mathcad has a problem finding a solution, try substituting different values for the "Find" unknowns at the top in Figure 2. Mathcad uses these values as guesses for its initial calculations. The closer these guesses are to the correct value, the more likely the program will converge to a solution.

Circle 523

Piezoelectric Alarm Rings Clear As A Bell

DENNIS EICHENBERG
Parma Heights, OH 44130; (216) 433-8360.

A common piezoelectric alarm, such as the Murata (Smyrna, GA) PKB5-3A shown, has many valuable attributes. It is compact, lightweight, efficient and reliable. However, the loud, high-pitched sound output can be quite irritating in many applications. The simple and inexpensive circuit provided here transforms this obnoxious little buzzer into a pleasant-sounding bell *(see the figure)*.



With some simple adjustments, an common piezoelectric alarm, with its annoyingly loud and high-pitched tone output, can be transformed into a pleasant-sounding bell.

At the heart of the circuit is the popular 555 timer U1, which is configured as an astable multivibrator. The output low time is a short pulse that initiates the bell strike. The strike time is 0.693 ↔ R2 ↔ C1. For the component values shown, the strike time is 6.93 ms. The output high time is the sustain time during which the amplitude of the bell tone decays continuously. The high time is 0.693 ↔ (R1 + R2) ↔ (C1). For this circuit, the high time is 236 ms.

When the output of U1 is low, the series transistor switch Q1 turns on through bias resistor R3 to energize the piezoelectric alarm AL1 and charge capacitor C3. When the output of U1 is high, Q1 is off and the output of AL1 decays until C3 is discharged. When C3 is discharged again, the cycle is repeated.

The values of timing components R1, R2, and C1, along with decay capacitor C3, aren't critical; various sound effects can be produced by experimenting with them.

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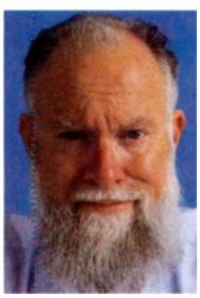
READER SERVICE 167

BOB PEASE

What's All This Recipe Engineering Stuff, Anyhow?

TAKE one pound of red kidney beans. Sort them carefully and reserve any pebbles and stones. (After you have saved a pound of stones, you can take them to the store for a refund.) Put the beans in 6 cups of water, in a large (5 or 6 quart) pot. Bring the pot to a boil, and boil for two minutes. Turn off the heat, cover, and allow to soak for two hours. Pour yourself a beer and take a break; you deserve it. Plan to chop veggies....

When I was a kid, I could not tolerate the mealy taste of beans. But eventually I learned to appreciate them, and now I am making up for lost time. Thus, whenever my wife goes away on a trip, I make up a big pot of chili con carne. It's not that she never makes chili, and it's not a gas problem. I just like this recipe.



BOB PEASE
OBTAINED A BSEE FROM MIT IN 1961 AND IS STAFF SCIENTIST AT NATIONAL SEMICONDUCTOR CORP., SANTA CLARA, CALIF.

This started as a recipe from a *Woman's Day Encyclopedia of Cookery*, a rather good cookbook. But the printed recipe had several flaws, so I started customizing it—re-engineering it. (Someday I'll tell you how I reverse-engineered the recipe for Joe's Special Starlite Lobster, but that's a whole 'nother story. Has anybody seen this recipe recently? Last I heard, Maurice the Chef had moved from Sunnyvale to Sacramento—and that was 30 years ago.)

The original chili recipe had 2 lbs. of lean chopped beef, plus 1/3 cup of suet for frying the vegetables. It only takes one try at finding suet—when there is none at the Safeway or four other markets—to begin to realize that if you start with ordinary hamburger, fry it, and save the fat, it's substantially equivalent to the fat from suet. Plus, it's much cheaper—and more available. Similarly, the original recipe called for 3 teaspoons of salt and 3 teaspoons of chili powder. I amended that to 1/4 teaspoon of salt and 12 teaspoons of chili powder.

What's a mere factor of three or four or twelve?? I have made this recipe over twenty times. (My wife does a lot of travelling.) I usually make 1.5 recipes, and it makes a great breakfast for 10 mornings in a row. Here's the complete recipe:

RAP's Chili con Carne con Frijoles (with Beans):

1 lb. red kidney beans, sorted
6 cups water
2 lbs. coarsely chopped beef or hamburger, *not* very lean
2 onions
2 green peppers
3 garlic cloves, minced
28 oz. canned tomatoes or fresh tomatoes, chopped coarsely
1/4 teaspoon salt
6 to 12 to 18 teaspoons chili powder
1 teaspoon paprika
1/4 teaspoon tagarashi (Japanese HOT chili powder) *(optional)*
1/4 to 1/2 teaspoon red pepper flakes

Set the sorted beans to boil in the 6 cups of water for two minutes. Then turn off the heat, and cover and soak for two hours. Meanwhile, chop the onions and green peppers into fairly small pieces (1/5 by 1/3 in., or as you prefer). Chop or crush the garlic. Chop the tomatoes.

Fry the beef 1 lb. at a time over high heat in a large skillet, browning it well in some places. (It will be well-cooked later, so you do not have to cook it uniformly.) Set the beef aside in a bowl, draining the fat back into the skillet. There should be 3 or 4 tablespoons of this fat in the pan. Or, add a little shortening to bring it up to at least 2 tablespoons.

Fry the onions, green pepper, and garlic over high heat so some of it is browned and most of the onions are at least translucent.

IMPORTANT: Now, drain off most of the fat from the onions. You might put back a little fat later. But, as the fat takes in the spices, you have to do it now or lose the spices when you take off the fat later.

Then, add the tomatoes. When it gets back to bubbling, turn down the heat to simmer. Add the basic spices: salt, paprika, pepper flakes, and about 6 teaspoons of chili powder.

NOTE: As there are such great variations in the strength and heat of purchased chili powder—and such differences in each person's taste and enjoyment of hot food—you must start with a little chili powder. Add more, to taste, later.

Stir and mix. Add beef. Stir and mix. Allow to simmer at least an hour.

After the beans have soaked two hours, apply heat and bring to a boil. Simmer covered for an hour or two until the beans are more or less cooked, *al dente*. (Some people change the water, but this recipe doesn't seem to need that.) Add water as needed to keep beans covered.

NOW add the meat and spices and veggies to the pot of beans. Bring to a boil. Simmer at least 20 minutes.

Stir the chili and sample. Start to correct the seasonings, adding a little more salt, chili powder, pepper flakes, etc., per your taste. This is a good time to bring in 4 or 8 or 10 more teaspoons of chili powder. But, take it easy on the pepper flakes; they can always be added later. After the flavors have melded for 30 minutes, you will probably be hungry and eat some. But, if you let it simmer another hour or two, it gets better. It gets even better when you re-heat it the second day.

Serving options: Serve with grated cheese on top. Serve over rice. Serve with tortillas. Use green beans or broccoli on the side—or on top. Try a dab of sour cream. It's great with a

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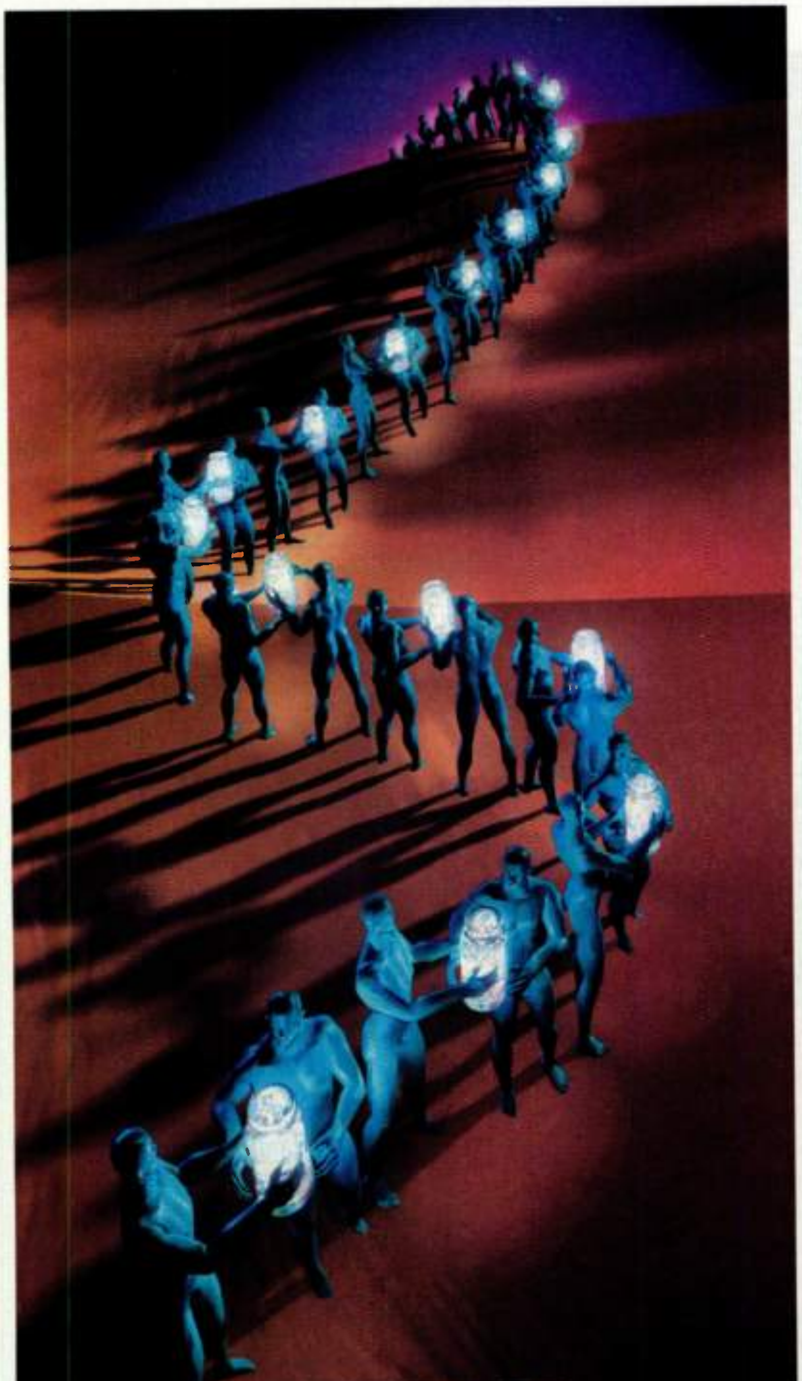

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fried egg for breakfast. That's what I am eating right now as I type. And it goes good with red wine, too.

Variations:

1. Take a pint of the chili and add a tablespoon of water. Blend for several seconds in the blender. Return it to the pot to make a richer, thicker sauce.
2. Take 2 cups of the chili, hot, and add 1 square (1 oz.) of UNSWEETENED chocolate. Heat gradually until the chocolate is melted. Stir in completely. You have an excellent *molé*.
3. Add veggies: carrots and more tomatoes. Add corn.
4. Fool around with the spices. Try more of this and less of that. I often sprinkle a little of the hot pepper flakes on top of my bowl so the main batch is not so HOT, but my bowl can be as hot as I want.
5. Try some different kinds of meat, such as ground lamb, turkey, or whatever is marked down this week. (But turkey is so lean, you'll have to add shortening or butter to fry the veggies.)

When you are finished with the chili for the first day, cool off the pot for an hour in a sink full of cold water so it will not overload the refrigerator. I usually heat up one bowl at a time in a microwave oven. But, you can reheat the whole pot, stirring almost continuously.

Cooking and recipe engineering can be fun, challenging, and tasty. And, if you avoid making a stupid move, you can avoid a huge pot of inedible "food."

Does the engineering of a recipe take good planning, good *processing*, good *JUDGEMENT*—and good skills at interfacing with *people*? Yeah, for sure. That's why my wife is a much better cook than I am, in general. (But, I can honestly say that I am, at least, an adequate cook on many dishes....)

All for now. / Comments invited!
RAP / Robert A. Pease / Engineer
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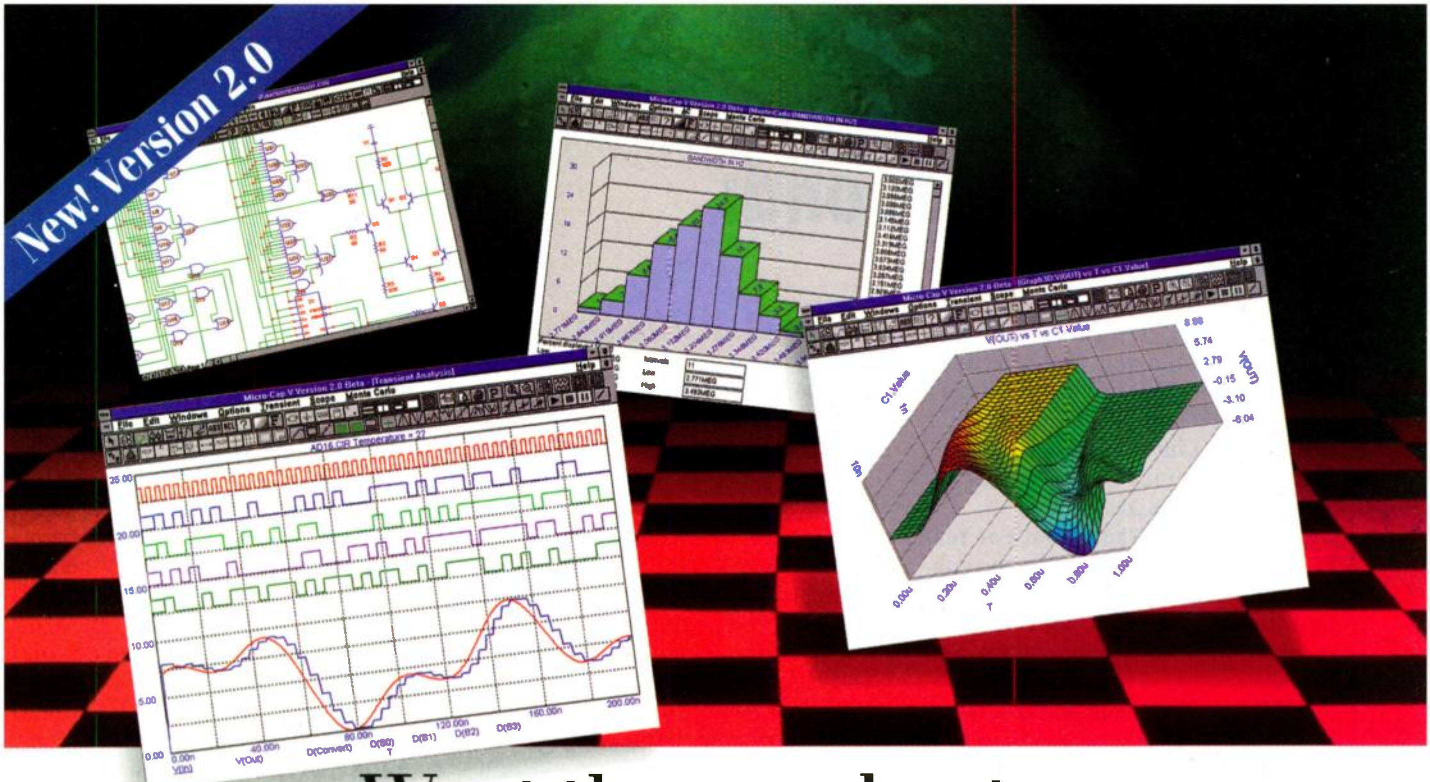

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READER SERVICE 172

WRH

Readers Respond:

Another Mailbag

This month, we'll take a look at some column mail that's accumulated since the July issue. While a variety has come in, most of it has been on the Linux column. Boy, is the Linux community ever a vocal one! Tons of mail, as below.

Aug. 3, 1998: "What's Best For Your PC?": Mail really came in on the subject of Linux, more than anything else I've discussed thus far. The comments received broke down into three general areas:

1. Many offered suggestions to try Staroffice (*www.stardivison.com*). A 4.03 version of the office suite had been previously available. Now, this has apparently been replaced by version 5.0, which is promised "within the next days" (as per the web site on Oct. 5, 1998). The beauty of this office suite is reported to be the read/write compatibility with Microsoft applications. When it does appear, it could well offer good utility in that regard.

2. Many also sent in suggestions to try the KDE desktop (*www.kde.org*). This is a replacement desktop environment for Linux which, at this writing, I have not had a chance to try. But, from the numerous enthusiastic comments received, it's worth the time to investigate if you're serious about using Linux.

3. Suggestions of what to do about "Plug-n-Play" (PnP) devices and "Winmodems" running under Linux came in from various readers.

I'll confess to some oversight here on the optimum modem configuration originally reported. The situation described in the Aug. 3 column reflected what actually transpired with the modem. But, as life would have it, a bit more time working with that original modem would actually have revealed it wasn't really any great mystery to Linux. (That's what happens when you face deadlines.) Here's what's happened since then...it's much more encouraging to potential Linux tire-kickers.

Some time after the original article, I caught a note on the Micron USENET newsgroup about the availability of free V.90 modem upgrades for recent buyers. I checked this out, and found that indeed there was an EXE file available to flash the internal USR 56k X2 modem that came with the machine. I downloaded it, installed the upgrade per the instructions, and all went OK.

Since this PnP modem device didn't originally work under Linux, I then set out to explore what happened when the card's jumpers were reset for a Windows 95 non-PnP mode, on COM2. After some false starts and non-recognition problems, I shortly had the modem with the V.90 upgrade running OK under Windows 95, and was able for the first time to get ~50 kbits/s downloads—life in a (relatively speaking) faster lane.

Overall, I was very fortunate in one sense. This particular modem had jumpers available for setting COM ports and interrupts, making the above reconfiguration under Windows 95 a rather simple one. More importantly, the modem's ability to work in either PnP mode, or as a standard modem, meant Linux life became much simpler. Had the modem been a Winmodem, as many readers indicated, it may not have been salvageable under Linux.

WALT JUNG

On the Linux side of the machine, I also was now able to talk to the USR V.90 modem after a simple Linux software reconfiguration, redefining the "/dev/modem" link as serial device "cua1" (equivalent to COM2). Things went fine dialing out under Red Hat's networking tool from within X-windows. Two COM ports are now reported under the Linux boot sequence, as they should.

I also have to confess to a mis-statement in the original column. I actually *don't* have the Micron XKU PnP sound "card" (part of the Intel 440LX MB) working under Linux. I was quite pleased to receive a lengthy and thorough analysis of the way to approach this from Mat Butler. Mat recommended using Pnpdump, a Linux utility which reports PnP device details. From this, the correct PnP device settings can be edited into a configuration file, which is then saved and subsequently read by Isapnp at boot up, configuring the PnP device appropriately. Thanks for the help on this, Mat!

Nelson Goewey of ESPN sent in some nice comments, and offered a tip on the Red Hat 5.1 CD's availability for $29.95 at MEI/Micro Center. This package is a complete REDHAT distribution, including boot diskette, installation manual, and three CDs. MEI/Micro Center can be reached at (800) 634-3478, or *www.mei-microcenter.com*.

Since this seemed to be too good to pass up and I was doing this follow up, I ordered the Red Hat 5.1 package and upgraded my original 5.0 installation. Everything went smoothly. I was soon running under Red Hat's 5.1 Linux with an updated kernel and no loss of prior settings. As it evolves, I'll try to continue reporting on Linux progress here.

Sept. 1, 1998: "Op Amp Audio (Part 1)": I got a variety of mail on this first audio-oriented column. And, as I'm writing this (early October), the second part is just out. More than a few readers have written to simply express their general appreciation on seeing columns discussing audio topics, as opposed to any specific points. In fact, a couple requested advance copies of future installments! While this interest is appreciated, advance copies are unfortunately not possible.

What makes sense to me is to collect reader mail on this series until some later point in time when reactions have jelled, and then reply to the overall context. The installment for this month's ELECTRONIC DESIGN Special Analog Issue should stir up some interest.

Acknowledgements: My thanks to all of those Linux users for offering various points, as well as their willingness to share technical knowledge. This spirit of helpfulness is greatly appreciated, and is certainly one of the Linux community's more remarkable traits!

Walt Jung is a corporate staff applications engineer for Analog Devices, Norwood, Mass. A long-time contributor to ELECTRONIC DESIGN, *he can be reached via e-mail at: Wjung @usa.net.*

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READER SERVICE 173

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The 3066 spectrum analyzer is a dc-to-3 GHz real-time instrument aimed at mobile-phone, wireless-component, and base-station design applications. The 3066 can acquire and display a 5-MHz band of frequencies simultaneously. The instrument can capture time, frequency, and modulation characteristics as they change over time, and display the analysis results for all three in a single view. The 5-MHz reach covers the full width of a channel for all leading wireless technologies, including GSM, IS-136, PDC, CDMA, and the 4.096-Mchip/s Wideband-CDMA. A zoom mode makes it possible to analyze specific areas of interest with the 5-MHz capture range. A frequency-mask trigger function provides a way to trigger on a user-selected event and capture a pre- and post-trigger record. Applications of this function include detecting CDMA partial-rate randomized bursts and oscillator phase hits. The 3066 starts at $43,500, with delivery 12 weeks ARO. JD

Tektronix Measurement Business Div., P.O. Box 3960, Portland, OR 97208-3960; (800) 426-2200, ext. 1085; fax (503) 222-1542; www.tek.com/ Measurement.

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National Instruments, 11500 N. Mopac Expressway., Austin, TX 78759-3504; (512) 794-0100; (800) 258-7022; fax (512) 794-5759; e-mail: info@natinst.com; www.natinst.com.

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To complete a 5-V, 622-Mbit/s receiver, the MAX3760 must be combined with a photodiode and a limiting amplifier IC like MAX3761/62. In 1000s, the preamp starts at $8.30. AB

Maxim Integrated Products, *120 San Gabriel Dr., Sunnyvale, CA 94086; (408) 737-7600; www.maxim-ic.com.*
CIRCLE 705

Audio DAC Offers Precision And Linearity

The PCM1704 is a precision 24-bit digital-to-analog converter (DAC) with high dynamic performance and very low distortion and noise. When used with a digital interpolation filter, the PCM1704 supports 8X oversampling at 96 kHz. According to Burr-Brown, it's designed to deliver 112-dB dynamic range, 120-dB signal-to-noise ratio (SNR), and a total harmonic distortion plus noise (THD+N) of 0.0008% (typical). Fabricated in a biCMOS process, the 24-bit DAC's high performance and improved sound quality is attributed to sign-magnitude architecture and use of precision laser-trimming techniques. The architecture eliminates glitches and other nonlinearities. Packaged in a 20-pin SOIC, the PCM1704 starts at $12.95 in quantities of 1000. AB

Burr-Brown Corp., *6730 S. Tucson Blvd., Tucson, AZ 85706; (520)746-1111; www.burr-brown.com.*
CIRCLE 706

Power MOSFET Is Protected Against Voltage Spikes

Crafted for automotive anti-skid braking systems, the STP80NS04Z and STP60NS04Z are two new rugged n-channel power MOSFETs developed by STMicroelectronics. These MOSFETs are fully protected from voltage spikes and ESD. They also provide ruggedness in inductive load switching to permit operation in harsh automotive environments. This is made possible by the manufacturer's mesh overlay process with strip layout geometry. In addition, the power MOSFETs incorporate back-to-back gate-source and gate-drain Zener diodes for clamping voltage spikes and ESD.

Housed in TO-220 packages, the 80-A STP80NS04Z offers a typical on-resistance of 7.5 mΩ, while the 60-A STP60NS04Z presents a typical on-resistance of 10 mΩ. The minimum clamping voltage (drain-to-gate breakdown voltage) for the two power MOSFETs is 34 V, which gives a wide safety margin

(continued on page 170)

READER SERVICE 100

(continued from page 168)
even under load dump conditions, according to the company. Specified for operation with a maximum junction temperature of 175 °C, the MOSFETs are 100 percent avalanche tested. In quantities of 10,000, the STP80NS04Z is priced at $1.10 and STP60NS04Z at $0.90. AB

***STMicroelectronics Inc.**, Lexington Corporate Center, 10 Maguire Rd., Bldg. 1, 3rd Floor, Lexington, MA 02173; (781) 861-2650; www.st.com.* **CIRCLE 707**

Integrated 24-Bit ADC Ensures Data Integrity

Crystal Semiconductor Products Division of Cirrus Logic Inc. has added three new 24-bit analog-to-digital converters (ADCs) to its CS552X family of high-precision data-acquisition ICs. The 24-bit CS5522/24/28 are highly integrated Δ–Σ converters with an on-chip instrumentation amplifier, a programmable-gain amplifier (PGA), a multichannel multiplexer, digital filters, and system and self-calibration circuitry. Also, it incorporates on-chip charge pump drive circuitry, thereby permitting these single-supply converters to measure negative voltages with respect to ground. The digital filters provide programmable output data rates. When operated at word rates of 15 Hz or less, the digital filters reject both 50- and 60-Hz line interference ±3 Hz simultaneously. In short, these high-resolution ADCs include all of the functionalities required to design complete data-acquisition solutions for industrial applications. Linearity error is rated at 0.0007% full scale.

While the two-channel CS5522 comes in 20-pin plastic DIP and SSOP packages, the four- and eight-channel CS5524/28 are available in 24-lead plastic DIPs and SSOPs. In 1000-piece quantities, the CS5522/24/28 are each priced at $6.20, $7.40, and $7.80, respectively. AB

***Crystal Semiconductor**, 4210 S. Industrial Dr., Austin, TX 78744; www.crystal.com.* **CIRCLE 708**

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Burr-Brown's new DRV101 is a single-chip low-side power switch that employs a PWM output to lower power dissipation and reduce heat rise, thereby increasing the device's reliability. Its rugged design is well suited for driving electromechanical and thermal devices such as valves, solenoids, actuators, and lamps. The PWM output function includes an internal 24-kHz oscillator, pulse-width modulator, digital control input, external delay and duty-cycle adjust, thermal shutdown, and over/under current detection. An output flag indicates fault conditions. Other features include output drive of 2.3 A, supply range of +9 to +60 V, and full protection against overheating and over current. Pricing for the DRV101 is set at $3.60 in 1000-unit quantities, with delivery from stock. Package options include a compact 7-lead TO-220 package and a 7-lead surface-mount DDPAK plastic power package.

***Burr-Brown Corp.**, P.O. Box 11400, Tucson, AZ 85734; (520) 746-1111 or (800) 548-6132; Internet: www.burr-brown.com.* **CIRCLE 709**

IF-Sampling ADC Targets Digital Radio Receivers

Analog Devices introduced the AD6640 IF-sampling 12-bit ADC for emerging wideband and multichannel digital radio receivers. Designers can use the AD6640 to digitize intermediate frequencies directly, and therefore replace analog mixers, gain blocks, I/Q demodulators, and filters with their digital equivalents. Applications for the part include cellular/PCS base-station receivers for CDMA, GPS anti-jamming receivers, and phased array receivers. The single-chip AD6640 guarantees sample rates up to 65 Msamples/s with 80 dB of spurious free dynamic range. Its fully differential analog input stage features 300-MHz input bandwidth, which enables direct IF sampling at up to 70 MHz for multichannel and 200 MHz for single channel.

The AD6640 comes packaged in a standard 44-pin plastic TQFP, and sells for $57.20 in 1000-piece quantities. Samples and high-volume production quantities are available from stock. Two evaluation boards that combine the chip with fast digital downconversion and filtering also are available. AB

***Analog Devices Inc.**, Ray Stata Technology Center, 804 Woburn St., Wilmington, MA 01887; (781) 937-1428; www.analog.com.* **CIRCLE 710**

Low-Distortion PHY For XDSL And Other Twisted-Pair Apps

The EL1502 "II" is a transceiver intended for delivery of large, low-distortion signals over twisted-pair lines. Designed for telecom and networking equipment suppliers, it supports the stringent requirements of ADSL and HDSL interfaces. The Slide II is built with two wideband high-voltage drivers, and two low-noise receive amps. It also can drive full DMT or increased CAP power levels. Its low-distortion output helps optimize bit-error rates.

Signal levels are +22 dBmW at 1 MHz with distortion of –66-dBc driver output. Typical receive distortion at 15 V and 1 MHz is –70 dBc. Linear peak output reaches 450 mA. In addition to ADSL and HDSL lines, the device also can be applied in video twisted-pair line drivers or video-distribution amplifier applications.

The EL1502 is housed in a 20-pin SO package that eliminates the need for an external heat sink and reduces board space requirement. It's available now, with pricing beginning at $5.00 in production quantities. LG

__Elantec Inc.__, 675 Trade Zone Blvd., Milpitas, CA 95035; (408) 945-1323, (408) 945-9305; www.elantec.com.

CIRCLE 711

12-Bit, 65-MSPS ADC Samples At IF For Digital Radio Apps

Digital radio applications are becoming more practical and affordable with the introduction of the AD6640, an IF-sampling, 12-bit ADC. Intended for use in commercial wideband and multichannel digital radio receiver systems, its applications range from new cellular/PCS base-station receivers for CDMA, GSM, and new third-generation systems, to GPS anti-jamming and phased array receiver systems. The single-chip converter guarantees sample rates of up to 65 Msamples/s with 80 dB of spurious-free dynamic range (SFDR). Its fully differential analog input stage has a 300-MHz input bandwidth, which allows direct IF sampling up to 70 MHz (multichannel) and 200 MHz (single channel).

The AD6640's ability to directly digitize intermediate frequencies lets receiver designers to replace analog mixers, gain blocks, I/Q demodulators and filters with their digital equivalents. This reduces receiver size, cuts manufacturing costs and improves filter accuracy. Its high sample rates and IF capability also allows designers to position harmonics "out of band" while reducing the overall noise floor via processing gain. One ADC digitizes the entire input spectrum, allowing designers to replace multiple analog front ends with a single wideband, multichannel sampler.

The AD6640 requires a single +5 V power supply and dissipates a nominal 710 mW. The digital output stage may be powered from +5 V or +3.3 V for easy interface to digital ASICs. Two evaluation boards, the AD6640ST/PCB and the AD6620S/PCB, plug together to form an IF-to-baseband receiver subsystem and come with complete filter design and control software.

The AD6640 is housed in a standard 44-pin plastic TQFP and sells for $57.20 in 1000-piece quantities. Samples and high-volume production quantities are available from stock. LG

__Analog Devices Inc.__, Ray Stata Technology Center, Woburn St., Wilmington, MA 01887; (617) 937-1428; fax (617) 821-4273; www.analog.com.

CIRCLE 712

Baseband Processor Speeds GSM Phone Development

The GSM baseband processor (GBP) performs all of the baseband and mixed-signal processing functions required to implement a GSM handset. Its flexible design provides engineers with a quick, flexible, and cost-effective way to develop a phone. The design is based either on the off-the-shelf IC, or with a semi-custom chip that incorporates some or all of the product's licensable cores. The GBP architecture can be used to design various equipment, including mobile terminals for GSM 900, DCS 1800, and PCS 1900 applications.

The GBP contains a TinyRISC MIPS-16 control processor that performs all control tasks, including the phone's protocol stack, user interface, and hardware interface control. Also on-board is an OAK DSP signal processor, which handles all of the speech processing and compression tasks, as well as translation to and from baseband signals. Special hardware acceleration logic allows the DSP to support codec

(continued on page 172)

(continued from page 171)
functions for both full-rate speech and data/fax services, with optional enhanced full-rate speech processing.

The GBP also integrates a complete set of mixed signal cores, including a voice codec, a modem, and a set of analog interfaces to microphone, speaker, and power-control functions. The chip's 3-V, 0.25-µm technology and a power-efficient design (63 mA active, 1.5 mA standby) give the design extremely long standby and operational times on a small battery pack.

Rapid development is aided by the GBP's GSM development system (GDS). It comes with reference designs for both hardware and software that supports an on-chip RTOS and the GSM phase 2 protocol stack. A large base of third-party software also is available. Designers can develop their own custom ASIC by mixing-and-matching any of the GBP's cores with others from a large library of functions.

Housed in a 208-contact plastic mini-BGA, the GBP is available now. Pricing is $15 in volume quantities. LG

***LSI Logic Corp.**, 1551 McCarthy Blvd., Milpitas, CA 95035; attn: Dept. CPNR14, (800) 574-4286; (408) 433-7700; www.lsilogic.com.* **CIRCLE 713**

Ethernet Accelerator Engine Speeds Networking Apps

Fast Ethernet and Gigabit Ethernet NICs, switches, and other networking products can enjoy higher performance using the JT1001 is a single-chip Ethernet network accelerator. It allows servers or workstations to interface seamlessly with 10-, 100-, or 1000-Mbit/s Ethernet network. Its integrated protocol processing functions provide LAN-equipment designers to give their NICs and LAN on Motherboard (LOM) products much higher performance at a low cost.

By handling many repetitive low-level protocol functions, such as IP, TCP, and UDP checksum calculations, the host CPU is offloaded for work on other tasks. The accelerator also eliminates the need to embed an additional processor on a NIC, allowing designers to thereby reduce the cost and complexity to their products.

The JT1001 has a 33-MHz PCI 2.1-compliant interface with 32/64-bit operation, 64-bit addressing, and efficient PCI master operation. On-chip control logic minimizes bus arbitrations and eliminates logical to physical address translation. It supports dual address cycles and has 96-kbyte FIFO memory buffers, allowing multiple packets to be loaded into the buffer and burst across the bus for maximum efficiency—a particularly important feature for gigabit applications. Connections to PHY-layer devices are accomplished through a gigabit media independent interface (GMII) for 1000Base-T a media independent interface (MII) for 10/100Base-T or a Ten-Bit Interface for 1000Base-X.

Housed in a 272 (PBGA) package, the JT1001 is sampling now, with production beginning October 1998. In 1K quantities, the chip costs $65 each. LG

***Jato Technologies**, 505 E. Huntland Dr., Suite 550, Austin, TX 78752; (512) 407-2100; fax (512) 452-5592; www.jatotech.com.* **CIRCLE 714**

Midsize TFT LCDs Feature Slim Profile

These 5.8- and 7.0-in. TFT LCDs measure 145 by 89 by 14.8 and 167 by 102 by 15.5 mm, respectively. Targeting car navigation, amusement, and TV-monitor applications, the displays have a resolution of 400 by 234 pixels, an aspect ratio of 16:9, and a luminance of 350 cd/m^2. Both composite video and analog RGB interfaces are provided. The displays weigh 210 and 265 g, respectively, and come with a single CCFL edgelight and an anti-glare coating. Pricing for samples is $500 for the 5.8-in. version, and $700 for the 7.0-in. display. PM

***Toshiba America Electronic Components, Inc.**, 9775 Toledo Way, Irvine, CA 92618; Sales Dept. (800) 879-4963; www.toshiba.com/taec.*
CIRCLE 715

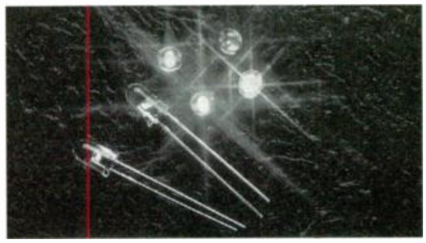
Mini-DIL Laser Diode Targets Subscriber Optical Networks

The HL1328DJS is an 8-pin Mini-DIL laser diode designed for use in high-bandwidth subscriber optical data networks. Featuring an output of 0.4 mW at a wavelength of 1310 nm, the diode allows for data speeds of up to 622 Mbits/s. The device requires no reshaping upon installation, and acts as a drop-in replacement for 14-pin components. The device, which complies with Bellcore 983, has an operating temperature range of –40° to 85°C. Pricing is $60 each per 10,000. Sample availability will be in the third quarter this year, with quantities due in the first quarter of 1999. PM

***Hitachi Semiconductor (America) Inc.**, 2000 Sierra Point Pkwy., MS-080, Brisbane, CA 94005-1835; Sales Dept. (800) 285-1601, ext.11; Internet: www.hitachi.com/semiconductor.*
CIRCLE 716

LEDs Enable Full-Color, Full-Motion Outdoor Signs

Designed for full-color, video outdoor signs, these 5-mm LEDs have an oval-shaped radiation pattern (35° by 70°) and a luminous intensity of up to 400 mcd at 20 mA. The devices use AlInGaP material for amber and red, and InGaN material to achieve blue and green. Each LED includes both UV-A and UV-B inhibitors. Pricing ranges from $0.17 to $0.72 each per million, depending on color. PM



***Hewlett-Packard Co., Components Response Center**, 3175 Bowers Ave., M/S 88U Santa Clara, CA 95054-9929; Sales Dept. (800) 537-7715; www.hp.com.* **CIRCLE 717**

Audio Board Delivers 360 MFLOPS Performance

Appreciating good quality audio may be an art, but crafting an engine to achieve that quality is definitely a science. Along such lines, the Spinner is a high-performance audio board designed for professional-audio OEM applications. The Spinner provides pro-audio equipment designers a signal-processing platform for demanding audio applications by integrating 24-bit, 96-kHz analog and digital audio interfaces with Analog Devices' new low-cost ADSP-21065L SHARC chip.

The Spinner achieves 360 MFLOPS of floating-point power from the board's two 30-MHz ADSP-21065L processors. The Spinner has up to four channels of A/D and D/A. The board supports standard interface protocols ,such as AES/EBU, for transferring digital audio data between professional digital audio equipment like PCM and DAT mastering recorders, modular multitrack recorders, and other equipment.

The Spinner is available with either one SHARC processor and an 8-bit digital I/O port for data acquisition, or with two SHARC processors and a 16-bit digital I/O port. A megabyte of flash is available as nonvolatile memory space. A 16-Mbyte bank of SDRAM is available to the 21065L processors at a 60-MHz clock rate, and a dual UART allows the Spinner to communicate with external serial devices. The Spinner starts at $495. JC

***BittWare Research Systems Inc.**, 33 North Main St., Concord, NH 03301; (603) 226-0404; fax (603) 226-6667; www.bittware.com.* **CIRCLE 718**

64-Bit PCI Board Supports Eight Slots

You don't need to suffer the expense of CompactPCI to get an eight-slot PCI system. The SB-923 is a 64-bit PCI system board that gets there with ordinary PCI. In a Mini ATX form factor, the board features eight PCI slots that can accommodate 64-bit PCI I/O cards on two independent 64-bit PCI buses. The two 64-bit PCI buses are hosted by Intel's i960 RN I/O processor.

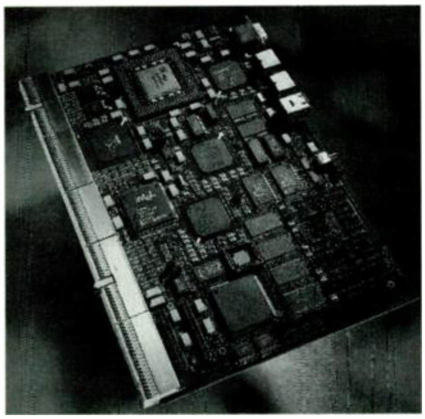
The processor provides an internal 64-bit bus and a 528-Mbyte/s SDRAM controller that opens I/O bottlenecks. The controller enables new levels of data throughput for embedded applications. The SB-923 is equipped with 16 to 128 Mbytes of SDRAM with ECC (error-correction code) in a 168-pin DIMM socket. The 66-MHz SDRAM is accessible by the processor or either PCI bus.

For system designers interested in a complete packaged system, the SB-923 also is offered in a rack-mounted chassis. The BX-923 is an SB-923 System Board mounted and tested in a rack-mounted industrial PC enclosure. The BX-923 is UL listed and FCC certified. The SB-923 and BX-923 will begin shipping this month and will be priced starting at $612 and $1224, respectively. JC

***Cyclone Microsystems Inc.**, 25 Science Park, New Haven, CT 06511; (203) 786-5536; www.cyclone.com.* **CIRCLE 719**

Boards Boast Asynchronous Bridging Capability

Sophisticated bus-bridge technology can enhance the capabilities of a PCI-based systems. Micro Industries offers three boards based on asynchronous bridge connectivity, specifically, on the Intel 21554 (also called Drawbridge), a non-transparent PCI-to-PCI bridge product. The first board,



the 586PCI/64PMC, is a Pentium processor-based PCI Expansion Board with a PMC interface. Its Intel HX chip set supports Intel, Cyrix, and AMD MMX Pentium-compatible processors up to 233 MHz and 192 Mbytes of SDRAM.

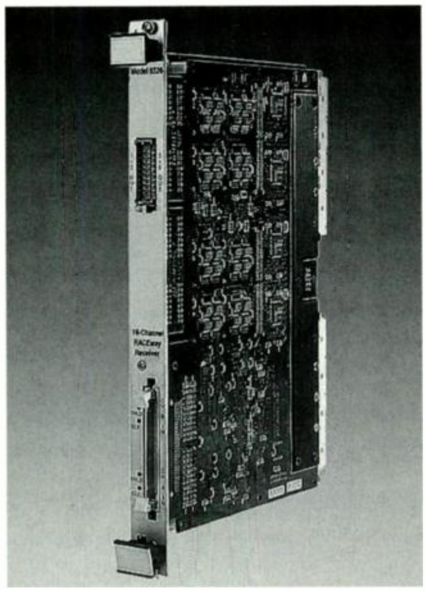
The second board, 586PCI/64PCI, is a Pentium processor-based dual PCI bus board. This product provides the same basic features as the 586PCI/64PMC. However, it replaces the PMC interface with a PCI Industrial Computers Manufacturers Group (PICMG)-compatible interface that expands the number of I/O slots which can access the bridged PCI bus on the board. The third board *(see the photo)*, the 586cPCI/64R3, is a Pentium processor-based Compact PCI expansion board with a secondary PCI interface. The board inserts the same features of the 586PCI/64PMC into a Compact PCI board format, providing primary and secondary bus access through the J I and J4 connectors.

Volume OEM pricing (excluding processors) for the 586PCI/64PMC is $695; for the 586PCI/64PCI is $695; and for the 586cPCI/64R3 is $795. JC

***Micro Industries Corp.**, 8399 Green Meadows Dr. North Westerville, OH 43081; (800) 446-6762; fax (740) 548-6184; www.microindustries.com.*
CIRCLE 720

First RACEway Digital Receiver Board Developed

Bandwidth is the name of the game for for high-end software-based radio systems. They require high-density, DSP intensive applications such as beam-



forming, signal tracking and mobile communications systems. The 6526 is the industry's first digital receiver to attack the bandwidth need with RACEway. The RACEway communications fabric can span up to 20 VMEbus slots, provide simultaneous data paths and support an aggregate transfer rate of over 1 Gbyte/s.

The 6256, which has sampling rates up to 62.5 MHz and 16-bit accuracy, is a 16-channel, 2-input narrowband digital receiver. This single-slot 6U VME board has front-panel connections for input clock, data, and synchronization signals. It includes a 32-bit VMEbus slave interface for control and status. The parallel inputs operate at TTL or differential ECL logic levels and support up to 16 bits of data at sampling rates up to 62.5 MHz for ECL, 50 MHz for TTL, and 40 MHz for FPDP.

The board uses four Graychip GC4014 quad, narrowband digital tuner chips to provide a total of 16 receiver channels. The 16 identical channel formatter sections accept serial output data from the GC4014s, convert the data to 32-bit parallel words, and then form single-channel data packets.

The 160-Mbyte/s RACEway interface allows individual packets of data from each receiver channel to be directed to specific processors on any RACEway-equipped DSP boards in the VMEbus system. The Model 6526pricing starts at $14,850. JC

***Pentek Inc.**, One Park Way, Upper Saddle River, NJ 07458-2311; (201) 818-5900; fax (201)818-5904; www.pentek.com.* **CIRCLE 721**

Storage Unit Offers 500-Mbyte/s Transfers

Scalable, high-speed memory storage can make or break applications such as digital video, satellite communications, and data acquisition. The DSU1000 is a data storage unit (DSU) utilizing PAID technology. PAID (parallel array of inexpensive disks) is an advanced information storage concept created by Signatec that offers more performance than traditional RAID (redundant array of inexpensive disks) products. The PAID architecture is designed to provide ultra-high sustained transfer rates for very long files.

The DSU1000 consists of one to four System Interface Modules (SIMs), a Disk Control Module (DCM), and multiple Disk Storage Modules (DSMs) installed in a VME-like chassis. Each Disk Storage Module has a transfer-rate capability of at least 40 Mbytes/s. These modules are added to increase the transfer rate or storage capacity of the unit.

A single DSU1000 with 19 DSMs can handle a sustained transfer rate of 500 Mbytes/s and provide a maximum storage capacity of 608 Gbytes. A single Data Storage System (DSS) can contain multiple DSUs, providing multiple terabytes of storage.

The DSU1000 employs distributed processing technology. Each module has its own processing unit and program RAM. This allows the processsing unit to be programmed for optimum performance in a variety of system applications.

Prices for the DSU start at $23,000. These prices vary based on the selected chassis and number of DSMs required to obtain transfer rate and storage capacity. JC

***Signatec, Inc.**, 355 N. Sheridan St, Suite 117, Corona, CA 91720; (909) 734-3001; fax (909) 734-4356; www.signatec.com.*
CIRCLE 722

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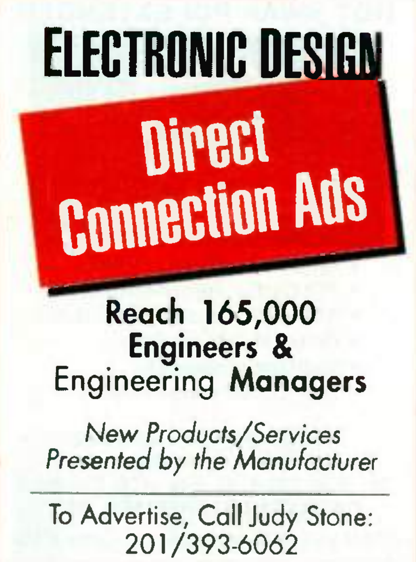

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