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ELECTRONIC DESIGN

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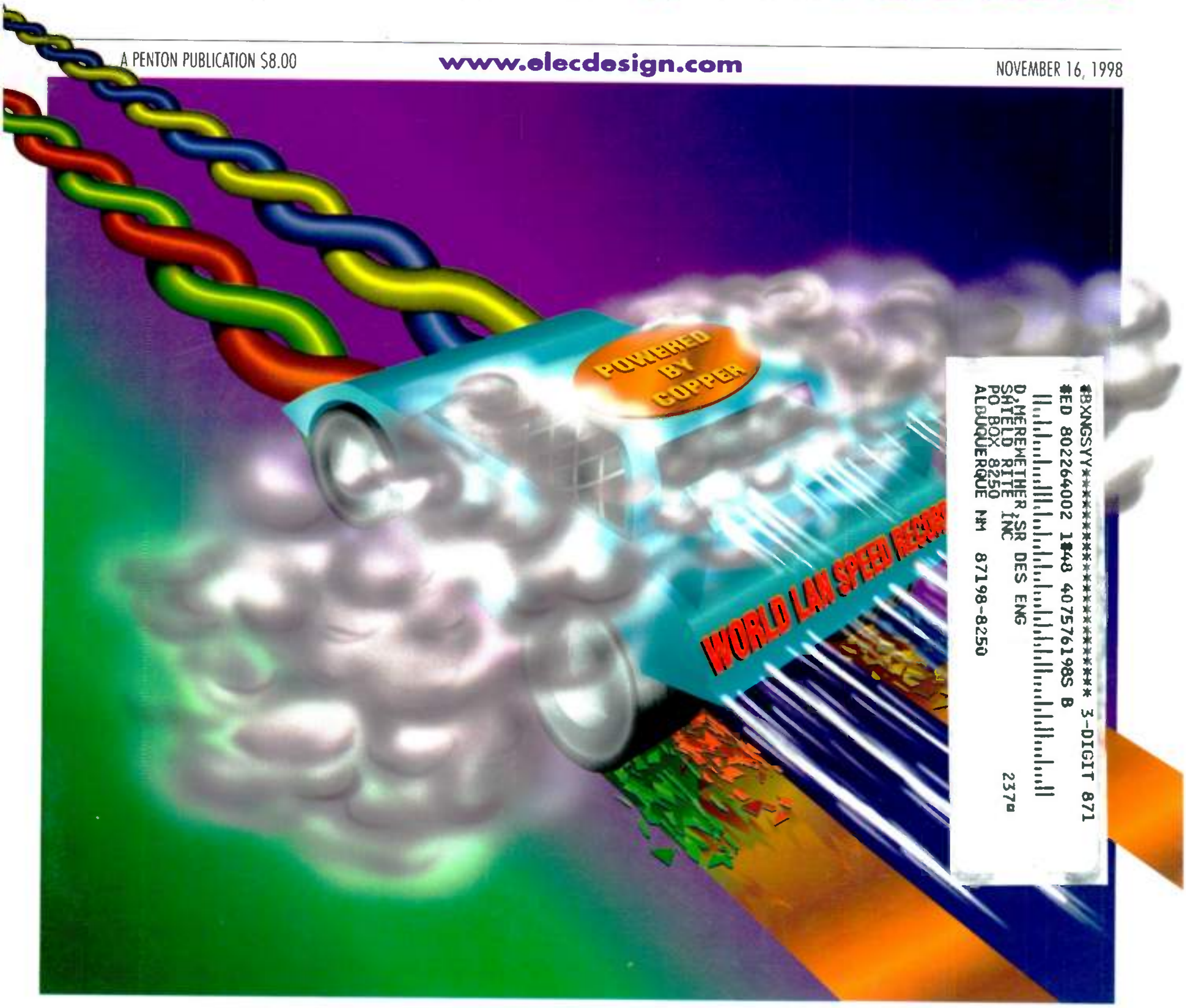

Gigabit Ethernet IC Sets LAN Speed Record For Copper p. 40

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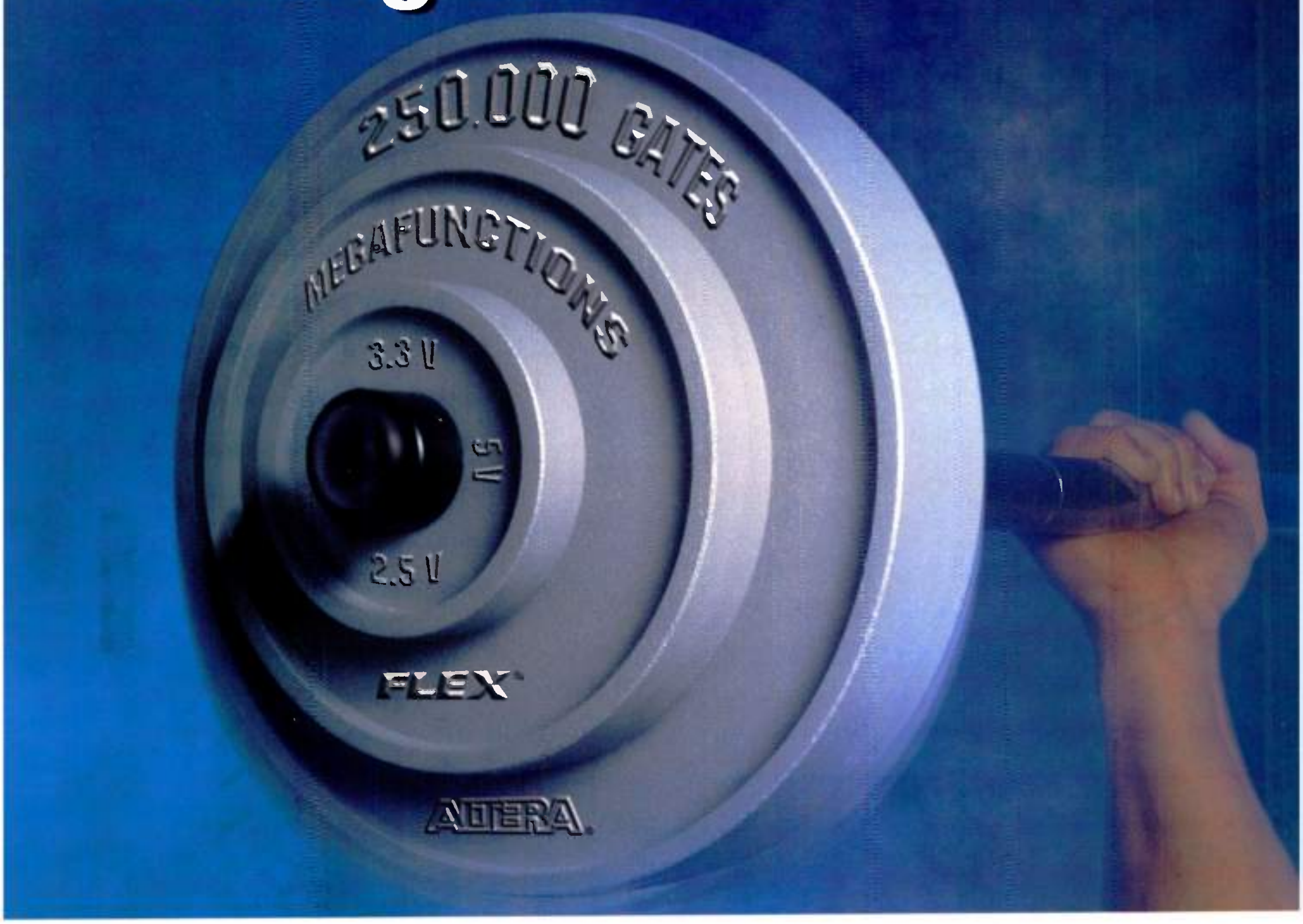

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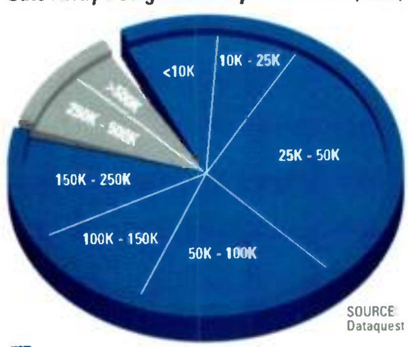
Gate Array Design Starts by Gate Count (1997)



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ELECTRONIC DESIGN

TECHNOLOGY•APPLICATIONS•PRODUCTS•SOLUTIONS

November 16, 1998 Volume 46, Number 26

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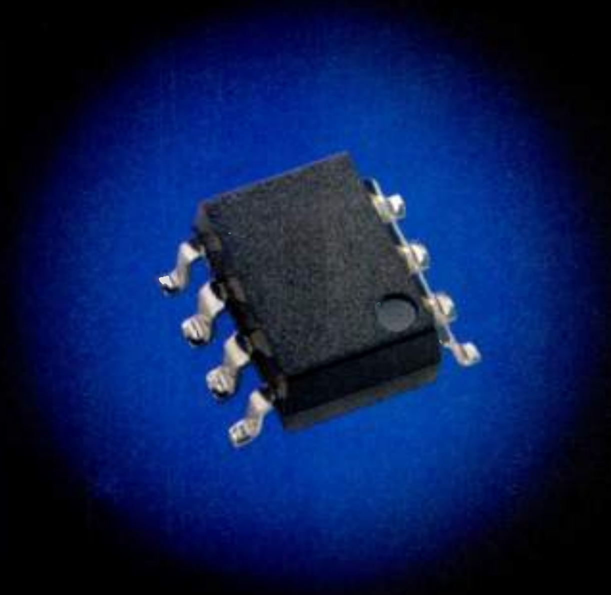
When A Leading U.S. Telecommunications Company Needed Optocouplers On Demand,



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ELECTRONIC DESIGN

TECHNOLOGY•APPLICATIONS•PRODUCTS•SOLUTIONS

November 16, 1998 Volume 46, Number 26

EDITORIAL OVERVIEW

LOOKING AHEAD: December 1, 1998

● A Special Report on Formal-Verification Tools and Techniques (Cover Story):......... This Special Report by EDA Editor Cheryl Ajluni will explain how formal verification—a mathematical and exhaustive methodology for proving that logic designs are correct and work the first time—is evolving into more powerful tools

● Previewing the International Electron Devices Meeting (IEDM):.......... Digital ICs Editor Dave Bursky looks at digital device developments; EDA Editor Cheryl Ajluni previews advanced models for complex designs, as well as the latest advances in sensors and displays; and Analog, DSP & Power Editor

● A Special Report on the Latest Board-Level DSP System Architectures:.......................... In this Special Report, Computer Systems Editor Jeff Child shows us how DSP-board vendors are solving computer data-bottleneck problems. They're employing clever architectures to make DSPs even faster.

● Special PIPS Supplement—Packaging, Interconnects, and Power Supplies:....................... The supplement will include reprints of articles by Patrick Mannion—*Electronic Design's* specialist for power, packaging, interconnects, components & optoelectronics—and design applications from experts in the field.

COVER ILLUSTRATION BY:
MARGARET ENDRES-BANGS

Jesse H. Neal Editorial Achievement

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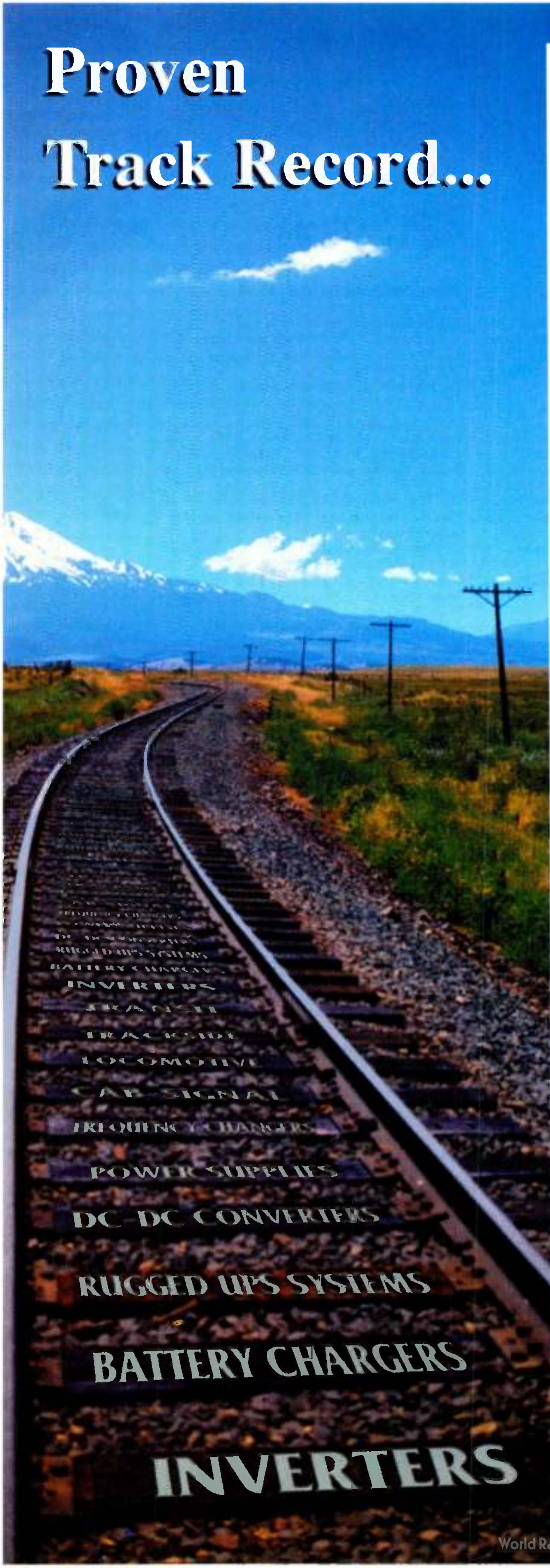

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NORTH AMERICAN EDITION

EDITORIAL

No Y2K Shelter For Me

While channel surfing late one night, I stumbled upon a news show featuring a story on the Y2K issue. An interview with a California software programmer overtook my urge to keep flicking the remote. This guy was building a secret, self-sufficient compound in the mountains to house him and his family after the upcoming computer clock glitch causes the country to go belly-up on January 1, 2000.

Now, I'm old enough to remember sensible people in the 1960s building makeshift basement bomb shelters or constructing elaborate and remote reinforced concrete hideaways that would protect them from Russian ICBMs. But, stockpiling canned soup and powdered eggs because of a faulty computer date? Can't we just hide under our desks for a little while until the Y2K thing passes, just like we did during the Cuban missile crisis? Apparently not.

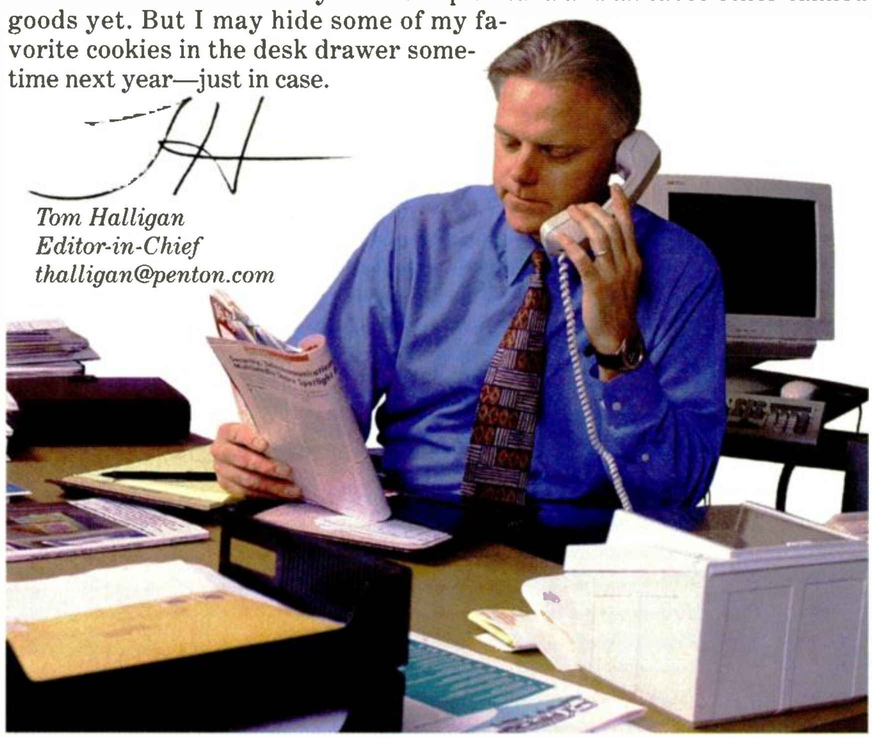
Although I think heading to the hills to wait out the alleged mayhem that will be caused by the Y2K issue is extreme, the guy being interviewed was a well-educated software programmer—not your typical American Joe. And, his dire predictions of what *could happen* because of the computer glitch actually sounded feasible—as long as MIS departments worldwide don't quickly fix their systems. Could banks fail? Could the stock market crash? Could people die in hospitals? Could planes crash? Could the food supply dwindle because of transportation snafus? Could governments be forced to shut down?

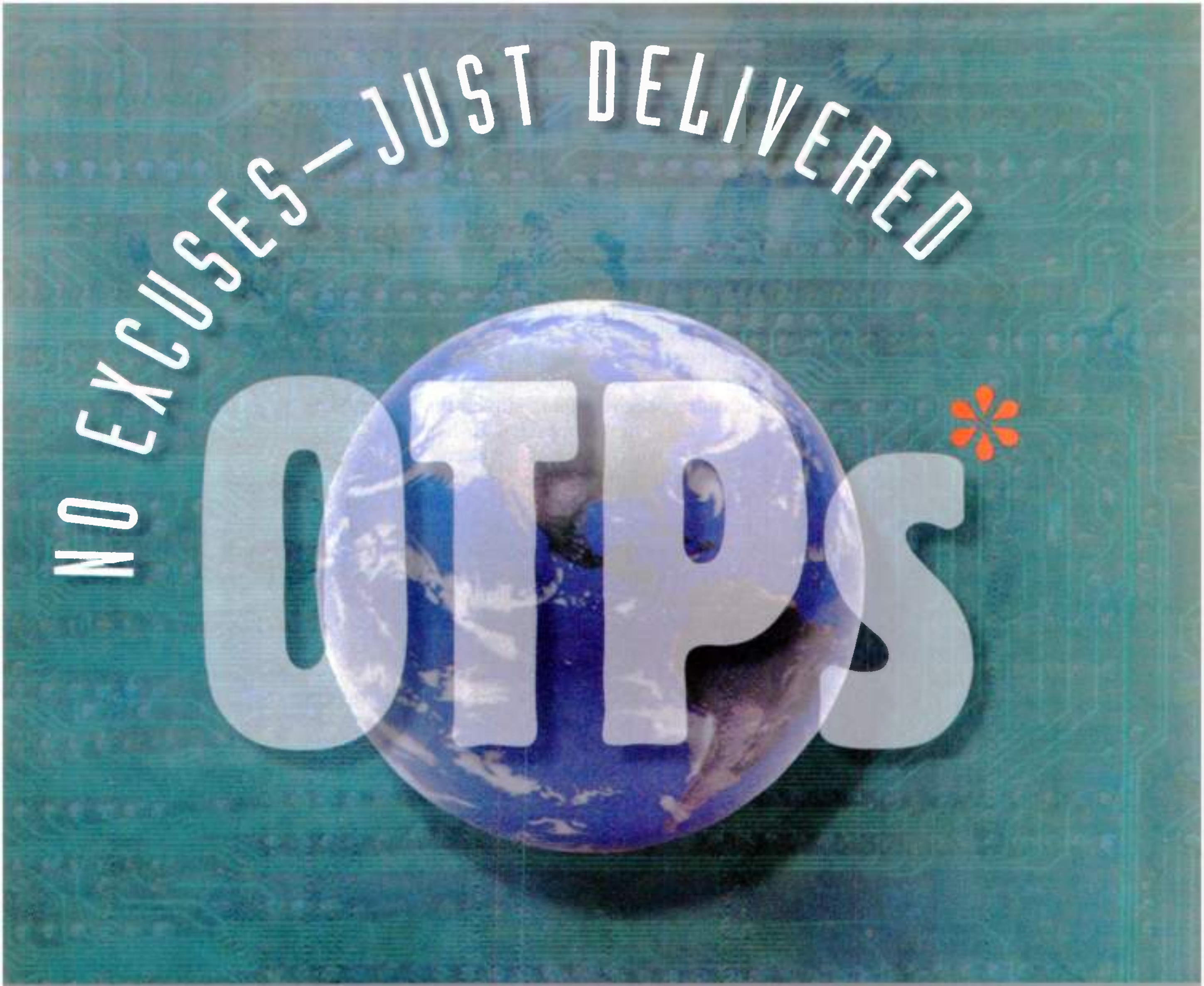
These thoughts ran through my head as I watched the other guest on the show—a man in charge of fixing our government networks and systems to make sure it's business as usual after New Year's Day. In contrast to the first guy, he seemed confident that our nation's critical network infrastructure will survive the glitch. But he wasn't very optimistic about other countries beating the deadline. And because the U.S. economy is a multinational octopus, even a minor foreign disruption usually causes the stock market to blink. So, if critical networks in Spain, Norway, and Bombay go down, I'd say we'll be in for some interesting times.

From what I read and from the people I talk to about the Y2K problem, the consensus seems to be that it's just a *computer problem*. Everyone believes that it will surely be fixed in the nick of time.

But will it? I'm not ready to stock up on tuna and all those other canned goods yet. But I may hide some of my favorite cookies in the desk drawer sometime next year—just in case.

Tom Halligan
Editor-in-Chief
thalligan@penton.com





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68HC705P6A	4.6K	176	28	M68ICS05P	KITMMEVS05P6A	KITMMDS05P6A
68HC705C8A	8K	304	40,44	M68ICS05C	KITMMEVS05C	KITMMDS05C
68HC705C9A	16K	352	40,44	M68ICS05C	KITMMEVS05C	KITMMDS05C
68HC705B16	15K	352	52,64	M68ICS05B	KITMMEVS05B	KITMMDS05B
68HC705L16	16K	512	80	KITPGMR05L16	KITMMEVS05L16	KITMMDS05L16

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Toddlers, Teens, Rebellion, & Revolution

Around the time my daughter Anwyn celebrated her second birthday, it became apparent that she was trying to take over our house. I then realized that what people call "the terrible twos" is not a passing phase, but a preview. After watching her undergo the mysterious alchemy that propelled her from infancy to personhood, I'm convinced that her uncharacteristic outbursts of evil-tempered, self-centered behavior are simply a rehearsal for her adolescence a decade from now. Most of the issues she'll face during her teen years are all there in miniature now: the discovery of one's self and one's place in the world, the testing of limits, the impatience with parents, and of course, the rebellion. Maybe I'm just hallucinating all this. But, at least it gives me some compassion for her plight and makes me feel less like strangling her with a piece of her Barney videotape.

Actually, I'm rather looking forward to Anwyn's adolescence—even the rebellion (or perhaps especially the rebellion). Having survived a "colorful" childhood myself, I find I can relate to my friends' teenage kids who seem to challenge every rule and convention laid upon them by the adult world. It seems to me that to be truly happy as adults, we must strike a delicate balance between moderating some of our less acceptable impulses and remaining friends with our "inner adolescent." Without some measure of this in our lives, we risk becoming over-socialized zombies.


LEE H. GOLDBERG
COMMUNICATIONS

I guess that's why I was so disappointed the other day when I heard about the hackers who broke into the *NY Times'* web site in protest of the incarceration of fellow-hacker-cum-felon, Kevin Mitnick. It's obvious that these kids are bright and were looking for something challenging to do. From the results, I'd say they accomplished their mission. They'd make great engineers. The only thing that bugs me is that they picked such a dopey hero to get all fired up about. I'd expect such smart people to choose a better role model than a semi-clever, misguided person like Mitnick.

Take Linus Torvalds and Richard Stallman, for instance. When they wrote the now-famous Linux operating system and GNU tools, they were looking to create less restrictive, royalty-free environments in which they and their friends could work and play. In doing so, these kid-geniuses unleashed a full-fledged assault on the conventional wisdom about the economics and programming practices of the modern PC. While Linux and GNU won't drive Novell or Microsoft off the desktop, they're certainly going to change the way they do business and give a large community of creative souls great alternatives.

Then there's Phil Zimmerman, inventor of Pretty Good Privacy public encryption. He has spearheaded a movement to bring cyber-privacy into the hands of the ordinary citizen. Without him and the equally responsible rebels at the Electronic Frontier Foundation, the debate over constitutional rights in cyberspace would most likely be decided by a bunch of suits in Washington.

Thankfully, creative rebellion is not limited to the young. Among the middle-aged heroes I could name are Tom Mahon and his merry band of Engineers Without Frontiers *(www.ewof.org)*. This emerging, Internet-based group of volunteers formed to render technical assistance to folks in need—both in the U.S and abroad. Modeled after the medical group, Doctors Without Borders, they are challenging the inequities of our world by giving technology to those who need it most. EWOF is looking for volunteers to help tackle projects ranging from communication, education, and healthcare to setting up MIS infrastructures to support developing businesses.

As I prepare for Anwyn's second adolescence a decade from now, Catherine and I struggle with the difficult job of helping our daughter become socialized without breaking her fiery spirit. Meanwhile, I'll take comfort in watching today's rebels become tomorrow's leaders. *leeg@class.org*

Third-Generation TigerSHARC DSP Unveiled At Forum

The much awaited third-generation SHARC digital signal processor DSP) architecture from Analog Devices Inc. has arrived. The details of ADI's TigerSHARC were presented at last month's Microprocessor Forum in San Jose, Calif.

Implementing static superscalar architecture, the TigerSHARC is created to bite at the rate of 2 billion multiply/accumulates (MACs) per second using 16-bit data, when clocked at 250 MHz. Consequently, it can execute eight 16-bit MACs/cycle, or 500 million 32-bit MACs. In fact, it can change data types, thereby supporting 8-, 16-, and 32-bit data processing. According to ADI, each of these data types is critical to the next-generation telecom protocols. While many telecom algorithms require 32-bit data processing, the 8-bit native support is for image processing.

"The chip achieves a new level of flexibility in software programming. The ability to scale the performance to the data type within the same chip will change the way DSPs are used today and into the next millennium," says Bob Conrad, ADI's product line director for DSP systems.

The TigerSHARC is targeted at large-scale and multichannel signal processing tasks in wireless base stations and Internet remote-access server equipment. That's because it offers two computation units, each fed by a 128-bit wide data bus. Each computational block contains a multiplier, ALU, and 64-bit shifter. Also, each block has access to a fully orthogonal 32-word register file that simplifies the programming task.

The three 128-bit buses offer high internal bandwidth, with memory accesses of up to 12 Gbytes/s. The high internal bandwidth allows complete context switch in just about 20 cycles. In addition, there are 128 interlocked registers that simplify the programming model, which is fully interruptible, according to ADI. Furthermore, the TigerSHARC architecture incorporates a 128-entry branch target buffer (BTB) that supports branch prediction. There's a two-cycle delay for every instruction. Consequently, all instructions have deterministic execution.

While supporting efficient, high-level language compilation, the TigerSHARC architecture has features that are attractive for assembly language programming, claims ADI. In short, it offers a flexible programming model. A complete tool suite consisting of a compiler, assembler, simulator, software libraries, and more is under development.

Based on 0.25-µm CMOS, the company hopes to sample the TigerSHARC, with 250- MHz clock speed, by early next year. For additional details call (800) 262-5643, or check the web site at *www.analog.com/dsp*. AB

ITU Agrees On High-Speed DSL Internet Standard Specs

The International Telecommunication Union (ITU), Geneva, Switzerland gave the nod to technical specifications for digital subscriber line (DSL) "Lite" high-speed Internet modem technology. This should pave the way for quick introduction of products to the market, according to Lucent Technologies' Microelectronics Group.

Thanks to this agreement, consumer will benefit from the rapid delivery of DSL "Lite" products and services into homes and businesses over regular phone lines that adhere to the approved technical specifications. DSL "lite" services transmit Internet data up to 25 times faster than today's fastest analog modems, without requiring voice/data splitters.

Lucent Technologies, Murray Hill, N.J., contributed extensively from the beginning in the development of the DSL "Lite" standard, also referred to as G.992.2 (previously known as G.Lite). Lucent's Microelectronics Group initiated and submitted several technical contributions that resulted in the ITU's important power-management specification for G.992.2 connections.

The spec allows a PC equipped with Lucent's DSL "Lite" power-management features to work with a DSL modem without breaking the communications link with the Internet Service Provider. Lucent plans to incorporate the complete set of power-management features and benefits into its WildWire DSL "Lite" solution. Formal ratification of the G.992.2 standard for the technology is scheduled for next June.

Aware Inc., Bedford, Mass., which was a provider of software and technology for WildWire, also made substantial technical contributions to the standards committee. Aware supplied key technical submissions involving "splitterless" DSL "Lite" technology, which alleviates the costs and inconveniences associated with a phone company's techni-

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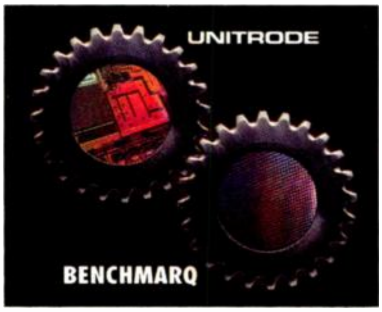

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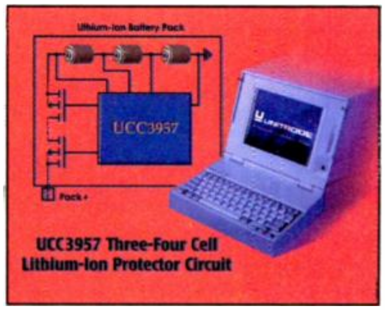

UCC3957

The UCC3957 battery protector provides complete voltage protection and over-current protection for three or four cell lithium-ion battery packs. This device is used in conventional and "smart" battery packs for equipment such as laptop computers and portable instruments.

www.unitrode.com/products/portable/ucc3957.htm

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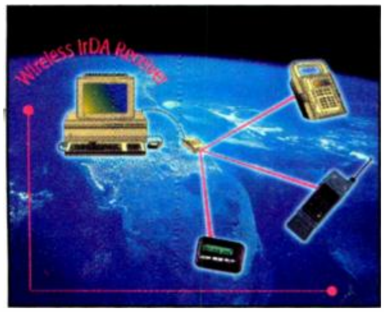

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Receiver and transceiver low current devices, these IrDA ICs are used in portable electronics applications. These devices support the analog section of the IrDA 1.0 standard, and have very low current consumption when active, making them excellent when power savings is at a premium.

www.unitrode.com/products/portable/ucc5341.htm
www.unitrode.com/products/portable/ucc5342.htm

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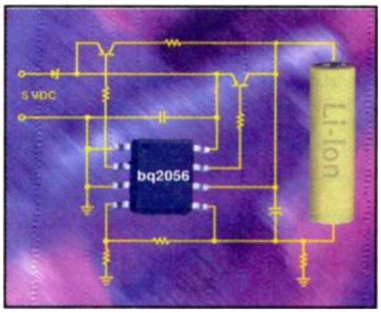

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UCC5638

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cian who needs to install splitters in homes. Aware also provided low-complexity algorithm technical submissions that enable lower costs of DSL "Lite" services for consumers.

Further information on the high-speed modem technology can be found on Lucent's Internet site at: *www.lucent.com/micro/WildWire*. RE

Partnership Gives LCoS Microdisplays A Significant Boost

With portable devices proliferating, it's only a matter of time before the processing power and bandwidth required for full video display becomes available. It's with this in mind that a number of companies are scrambling for a toehold in the microdisplay market. These high-resolution displays project video or still images onto large screens, or even more exciting, can display graphics on small personal information devices such as pagers or cell phones.

One of the key developers of this technology, Three-Five Systems, Tempe, Ariz., has come to the forefront of development with its liquid crystal-on-silicon (LCoS) process. Now, Three-Five has signed a letter of intent to form a development partnership with Varian Associates Inc., Palo Alto, Calif. The agreement will define both companies' responsibilities for developing an SXGA projection LCoS display system to be supplied by Three-Five to Varian on an exclusive basis. Three-Five will develop both the display system and electronic interface architecture.

For more information, contact Elizabeth Sharp, Three-Five Systems Inc., at (602) 389-8837, or visit the company's web site at *www.threefive.com*. PM

Qualification Program Eases Signoff Burden

Obtaining signoff status for an EDA (electronic design automation) tool in a design flow is a time-consuming and expensive task for the ASIC vendor. Now, as a way to help ease this burden, Si2 (Silicon Integrated Initiative Inc.), Austin, Texas, has instituted a qualification program to focus on one aspect of the overall signoff process. The program consists of exhaustive library regression testing against the target tool, design flow testing, and other stress tests performed by individual ASIC vendors.

In particular, the Si2 Labs qualification program will specifically address the issue of library regression testing. The tests are based on libraries and test cases from five participating ASIC vendors—IBM, Lucent, LSI, Motorola, and VLSI Technology—with each vendor setting its own criteria for including

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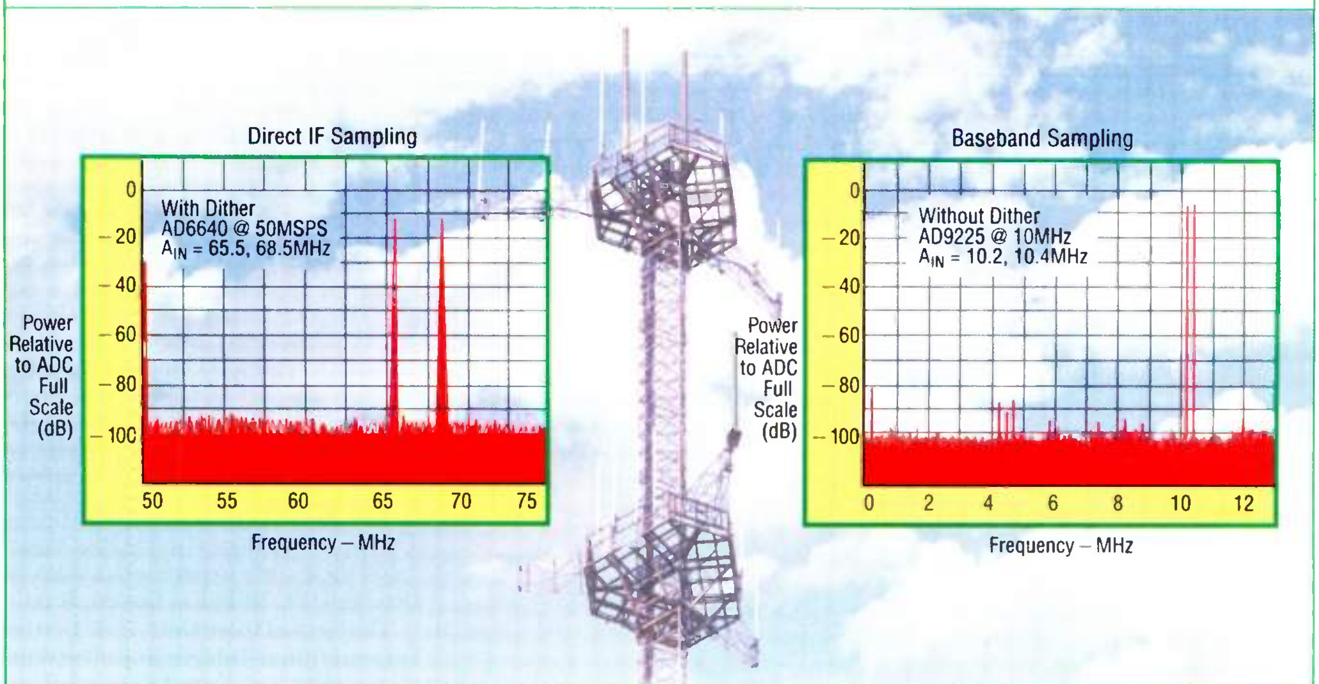

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a new EDA tool, or a new version of an existing tool, into its design flows. Testing performed at the lab will result in quicker tool evaluations and help streamline the qualification process.

All testing will take place at the Si2 Labs (formerly known as the ASIC Test Lab and originally established by the ASIC Council). When testing is completed, participating EDA tool vendors will receive a conformance label. To date, one vendor—Model Technology, Beaverton, Ore.—has received the Si2 Labs conformance label. The "Library Tested and Approved" designation was issued for the company's Verilog Simulator ModelSim VLOG.

The Si2 Lab is now in the process of testing other vendor's products. And, while this initial test program focuses on ensuring Verilog timing accuracy and functionality, it's expected that the Labs also may develop programs to test for the other two components in the signoff status process. Check out Si2's web page at *www.si2.org*, or Model Technology's web page at *www.model.com* for more details. CA

Intel, Cisco Complete H.323 Video-Conferencing Tests

Successful completion of interoperability tests for video-conferencing technologies, accomplished by Intel Corp., Santa Clara, Calif. and Cisco Systems Inc., San Jose, Calif, will provide businesses with high-performance, standards-based solutions for H.323 (LAN) video-conferencing deployment. The two companies successfully replicated their tests in demonstrations at October DVC '98 Fall in Boston, Mass.

The focus of these tests, H.323, is the International Telecommunications Union (ITU) standard for real-time multimedia communications and conferencing over packet-based networks. By completing interoperability testing, Intel and Cisco seek to resolve customers' difficulties with identifying and deploying H.323-compliant products that work together seamlessly.

In a laboratory environment, testing included point-to-point and multipoint H.323-based calls with full audio, video, and data sharing. Calls were routed over both local- and wide-area networks, using gatekeepers to manage bandwidth and provide address translation. LAN-based conferencing systems were connected with legacy ISDN-based systems through H.323 to H.320 gateways. In addition, products were tested in various configurations, including endpoint to gatekeeper, gatekeeper to gatekeeper, endpoint through a gateway, and endpoint through a gateway to a multipoint control unit.

For further info, contact Cisco Systems' Alison Wesley at (408) 525-9819; *www.cisco.com*. JC

Edited by Roger Engelke

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SP4415	2.2 - 3	3	50nA	.5 - 2	1.5	112	256	4 selectable light levels
SP4422A	2.2 - 6	15	200nA	1 - 10	3	188	270	requires minimal board space
SP4423	2.2 - 6	6	200nA	1 - 10	2.4	170	800	low power operation
SP4424	2.2 - 5	8	200nA	1 - 10	4.4	216	114	dual oscillators for coil and lamp control
SP4425	1.1 - 2.2	32	500nA	.5 - 6	3.65	176	348	low voltage operation
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New Chaos-Based Computing Technique Evolves Its Answers—Very Quickly

A new computing technique that uses a network of chaotic elements to "evolve" its answers could provide an alternative to the digital computing systems widely used today. The technique may be suited for optical computing using ultra-fast chaotic lasers and computing with silicon/neural tissue hybrid circuitry.

The system, developed by researchers at the Georgia Institute of Technology's Applied Chaos Laboratory, so far demonstrates an ability to handle a wide range of common operations. These include addition and multiplication, as well as Boolean logic and more sophisticated operations like finding the least common multiplier in a sequence of integers. Because it depends on interaction among its coupled elements, the system is naturally parallel.

For years, scientists have observed the rich variety of behavioral patterns created by chaotic systems, including those found in living organisms. Georgia Tech professor William Ditto, along with collaborator Sudeshna Sinha of the Institute of Mathematical Sciences, Madras, India, reasoned that these natural chaotic systems would have been eliminated through evolution unless they actually served a purpose.

Ditto and Sinha devised an experiment to see if a simple network of chaotic computer elements could be made to handle computations. By using an adaptive connecting mechanism that would open whenever an element exceeded a certain critical value, they joined the chaotic elements into a lattice. The mechanism was designed so that the researchers could set a wide range of critical values allowing them to vary the connection between elements.

They then encoded values into the chaotic lattice using a variety of techniques. In some cases, they chose patterns in the chaotic elements to represent numbers. In other instances, the numbers were represented by the amplitude of waves emitted by the chaotic elements or the frequency of "spiking" behavior.

After encoding the numbers, they stimulated the elements to begin interacting. Elements containing values above the critical level triggered the connecting mechanism, allowing the excess value to "avalanche" into neighboring elements. That transfer created additional avalanches in other connected elements. With added stimulation, the domino effect continued until the imbalance was conducted out of the system—as the answer to the mathematical problem.

In a simple example, values of three and four would be encoded into a system set with a critical value of one. The values would create an imbalance that would avalanche through the chaotic elements until it was conducted out of the system as the value of seven *(see the figure)*.

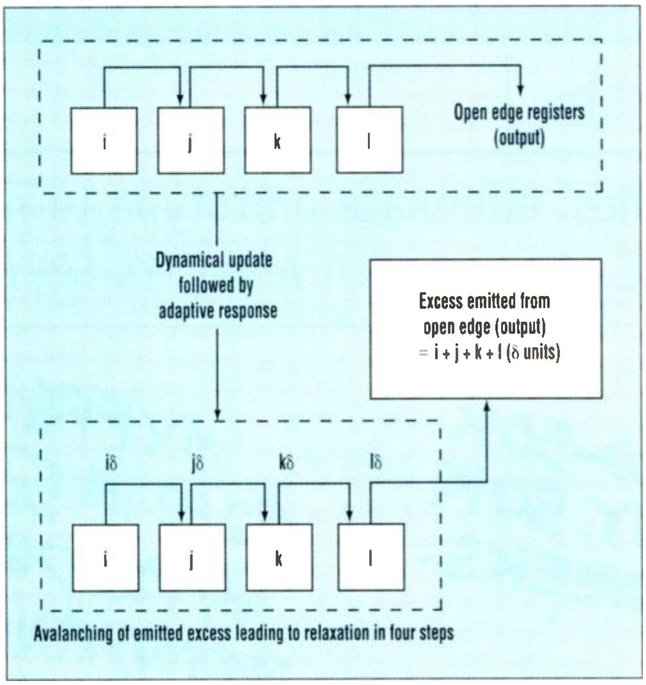
Chaotic elements are useful to this system because they can assume an infinite number of behaviors that can be used to represent different values or systems, such as logic gates. Because of this flexibility, altering the initial encoding and changing the connections between the chaotic elements permits one generic system to perform a variety of computations using its inherent self-organization. In conventional computing, systems are more specialized allowing them to perform certain operations.

Ditto says the researchers aren't really setting up rules in the same sense that digital computers are programmed. Rather, the system develops its own rules that the team simply manipulates. It uses pattern formation and self-organized criticality to organize toward an answer. Ditto emphasizes that the team doesn't micromanage the computing, but lets the dynamics do the hard work of finding a pattern which performs the desired operation.

Just as the numbers can be encoded in a variety of ways, the answer comes out in a multitude ways: a rate of change, an amplitude, or a specific chaotic behavior.

Because this new system differs dramatically from existing digital computers, it is likely to have different strengths and weaknesses. For those activities that digital computing does not do very well, like pattern recognition or detecting the difference between two pieces of music, this new system might even be better than digital computing.

Ditto compared dynamics-based computation to DNA and quantum computing, both of which are new computing paradigms still in their early stages of development. He believes the new technique would work particularly well in optical systems. Having done theoretical work applying dynamics-based computing to an ammonia laser system, Ditto hopes to see the



In this example, threshold-coupled chaotic elements emulate an adding machine. The four numbers to be added—i, j, k, and l—are each encoded by an element with a threshold set so that they emit i, j, k, and l units of excess respectively (where the unit of excess is δ). These elements are threshold-coupled in a chain, with the ejected excess from element i (= iδ) driving element j, etc., onto element l, from whose open boundary the collective excess is emitted to the output lead.

system implemented experimentally.

According to Ditto, you could stimulate a very fast system of coupled lasers to perform highly complicated functions like very fast arithmetic operations, pattern detection, and Fourier transforms. This would provide an alternative to existing efforts, which try to make optical systems do operations more like transistors. Ditto acknowledges a number of engineering issues that may hamper the development of a practical system based on this new computing paradigm. But, he notes that in their early days, digital computers had to overcome a daunting set of obstacles to overtake earlier techniques.

Support for the research has come from the U.S. Office of Naval Research and Control Dynamics Inc., a company partially owned by Ditto.

For more information, contact Ditto at (404) 894-5216; fax: (404) 894-9958; e-mail: wditto@acl2.physics.gatech.edu; www.gtri.gatech.edu/rco.html.

Jeff Child

Is The Paperless Society Finally Near? Well, Maybe Less Paper Anyway

We've all heard the line about computers making paper obsolete. It's certainly an intriguing possibility. The only problem is, it hasn't happened. Most of us still print out documents to read. It's just easier to take a printed document and read it at your leisure. Who really enjoys the eye strain caused by scrolling from page to page and zooming in and out to capture the fine details of a document on the screen?

Thanks to a development out of IBM Research, San Jose, Calif., we may finally have a solution to this latter problem: a 200-pixels-per-inch (ppi) active-matrix liquid-crystal display (AMLCD) that boasts a resolution very near the limits of human perception. The prototype display, dubbed Roentgen after the German discoverer of the X-ray, delivers clear, crisp images that are more than double the resolution of today's typical desktop displays. With a screen full of more than 5 million full-color pixels (2560 by 2048)—almost seven times that of the average desktop display—Roentgen can produce images so sharp that the fidelity is virtually indistinguishable from a printed page. In fact, the resolution is so good that a complete street map of Manhattan, including every street and avenue name, is readable with the naked eye.

The Roentgen prototype is 21-in. high by 16.5-in. wide, with a total depth, including base, of 9.5 in. The display itself is 2.5-in. thick and has a 16.3-in. diagonal viewing area. Weighing less than 20 lbs., Roentgen is less ın a third as heavy as today's conıtional cathode-ray tube (CRT) disys. In addition, the Roentgen disy has an aperture ratio of 27.3%, a ghtness of 130 cd/m², and a backıt power of 44 W. Its power dissipaı is less than half that used by an orary 18-in. CRT display.

This unique display technology c. nes on the heels of IBM's Monet—a 10.5-in. diagonal, 150-ppi Super XGA LCD. Building on this technology, researchers developed the Roentgen display by incorporating a combination of advanced display design techniques and low-cost manufacturing processes. The display's screen uses a new technology that incorporates both aluminum and copper. The result is electronic documents that not only look as good and e as easy to read as the paper equivat, but also are easier to search ough, reproduce, send, and store.

Another benefit of Roentgen is its lity to display more data on screen one time than the conventional CRT. Today, viewing the fine detail of a document on a CRT means having to limit the field of display to a small area and constantly pan and zoom. With Roentgen, this is no longer necessary. And, because of the display's high resolution, jagged edges that distort angled and curved lines and surfaces are virtually eliminated—without the need for anti-aliasing.

Roentgen's high performance, however, carries some challenges that must be overcome before the display can be commercialized, much less make its way into the mainstream. Having a screen with four times the number of pixels of a typical CRT means that the quantity of data also quadruples, creating a significant bottleneck. Wider, faster, and more numerous graphics pipes will need to be developed to address this traffic jam. In addition, the need to deliver acceptable frame rates will drive the demand for new hardware with high-performance geometry engines. Another foreseeable problem is that many web sites today are drawn by pixel size, so they will have to be revamped to take advantage of the denser screens.

Of course, IBM researchers anticipated these problems and are addressing them. They've already devised a scalable graphics-adapter architecture, based on off-the-shelf components that can handle the Roentgen's high-image content display. Its architecture is compatible with all current operating systems.

While IBM presently has no plans to turn the Roentgen display into a product, the technology could benefit a wide range of applications. As a result, the company is now actively involved in discussions with a number of potential customers around the world. Some of the applications ideally suited for this type of technology include any area where an electronic format for documents is essential, like desktop publishing and imaging, medical imaging, graphics design, web surfing, computer-aided design, oil and gas visualization systems, and digital content and creation.

For further information on the Roentgen technology, check out IBM's web site at www.research.ibm.com.

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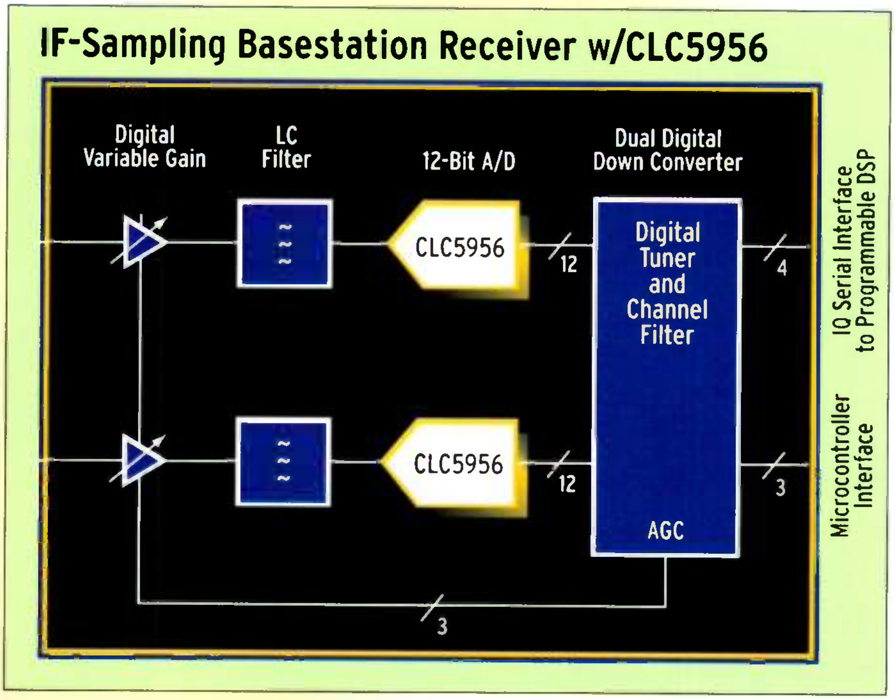

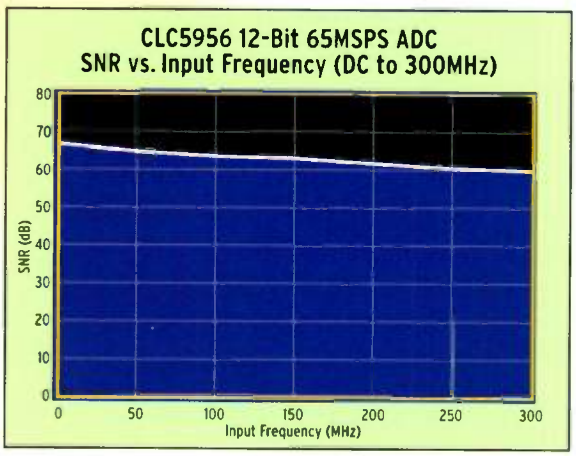

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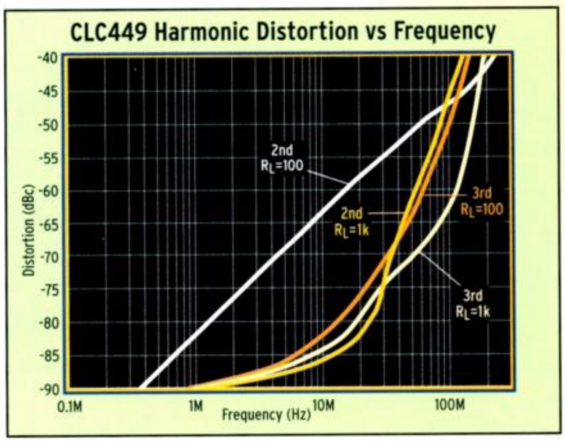

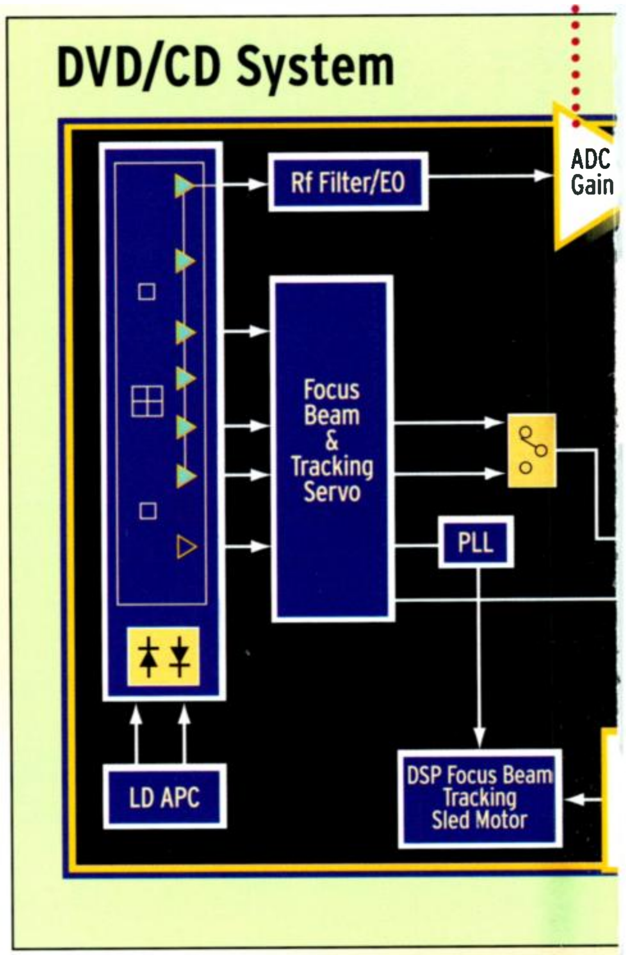

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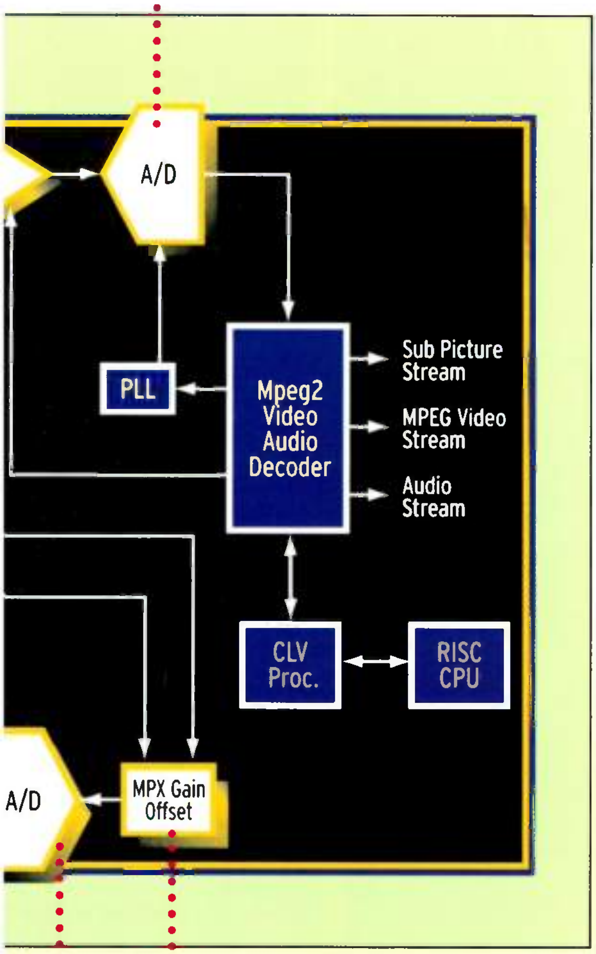

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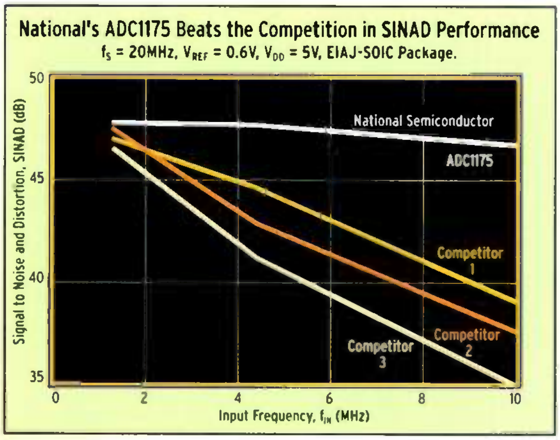

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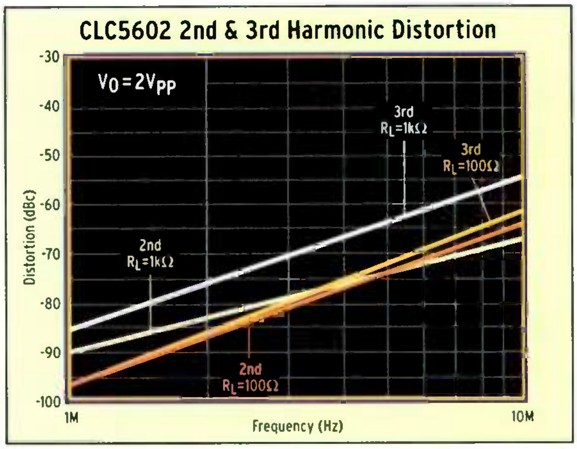

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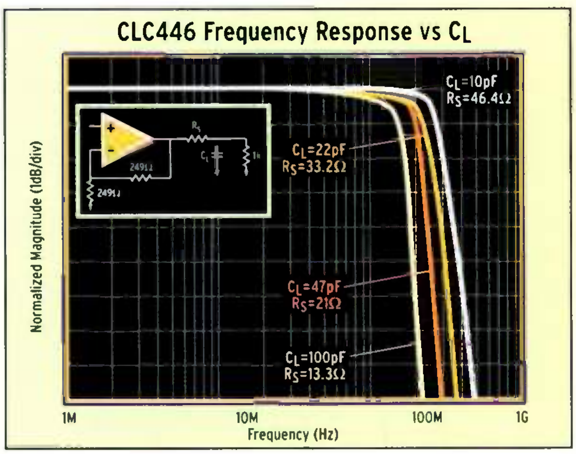

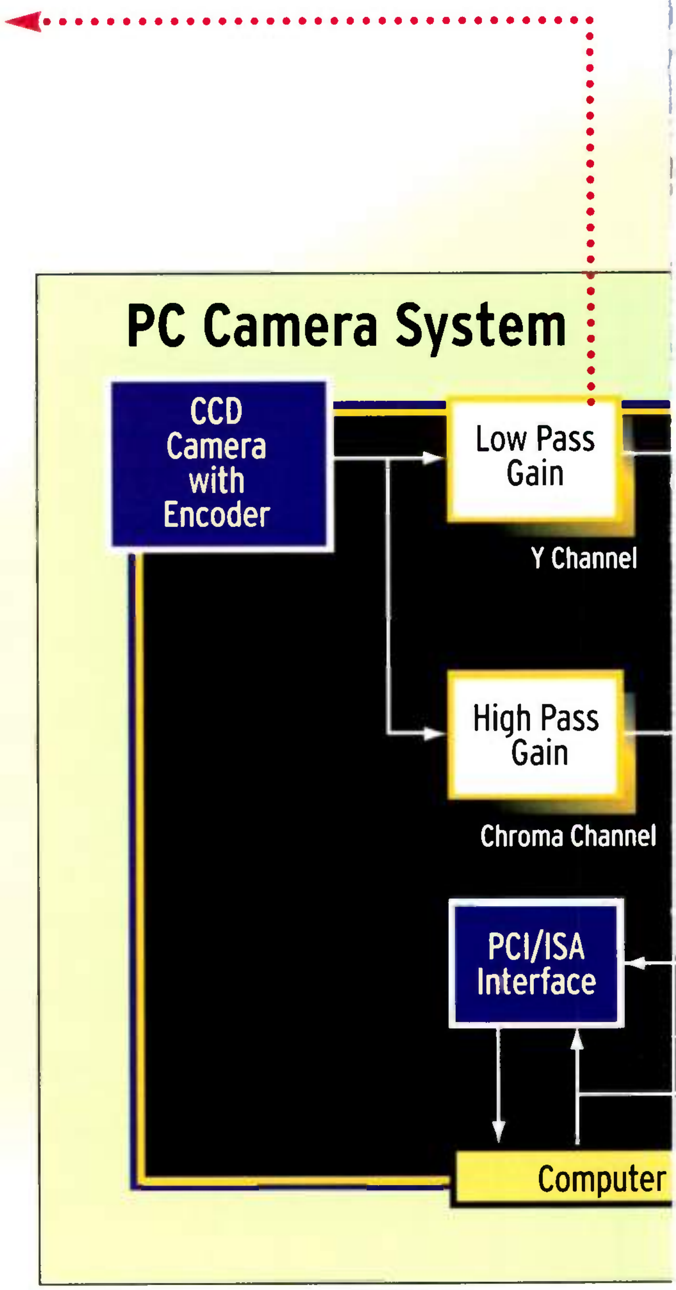

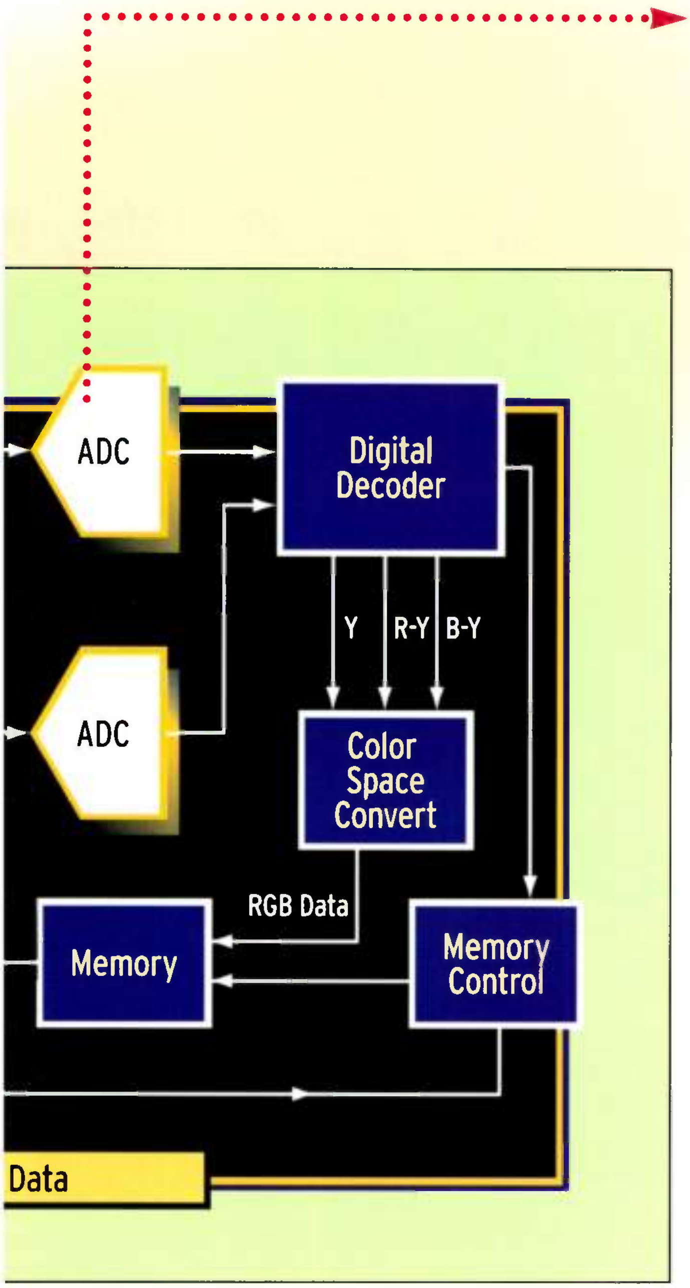

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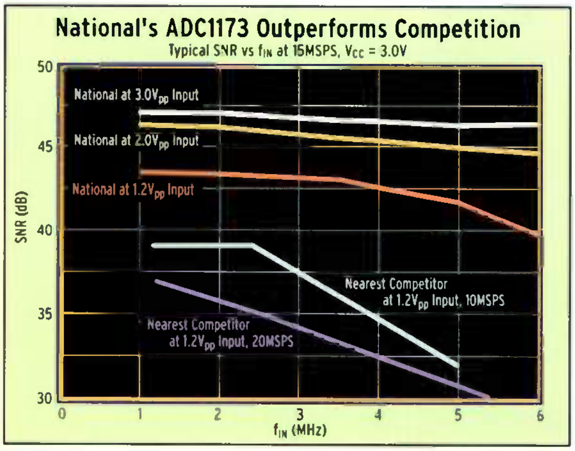

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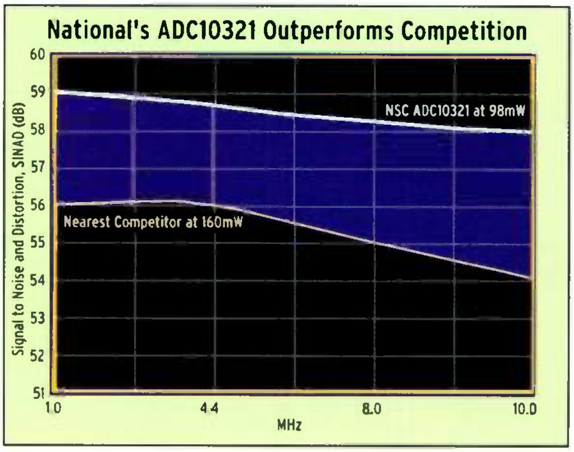

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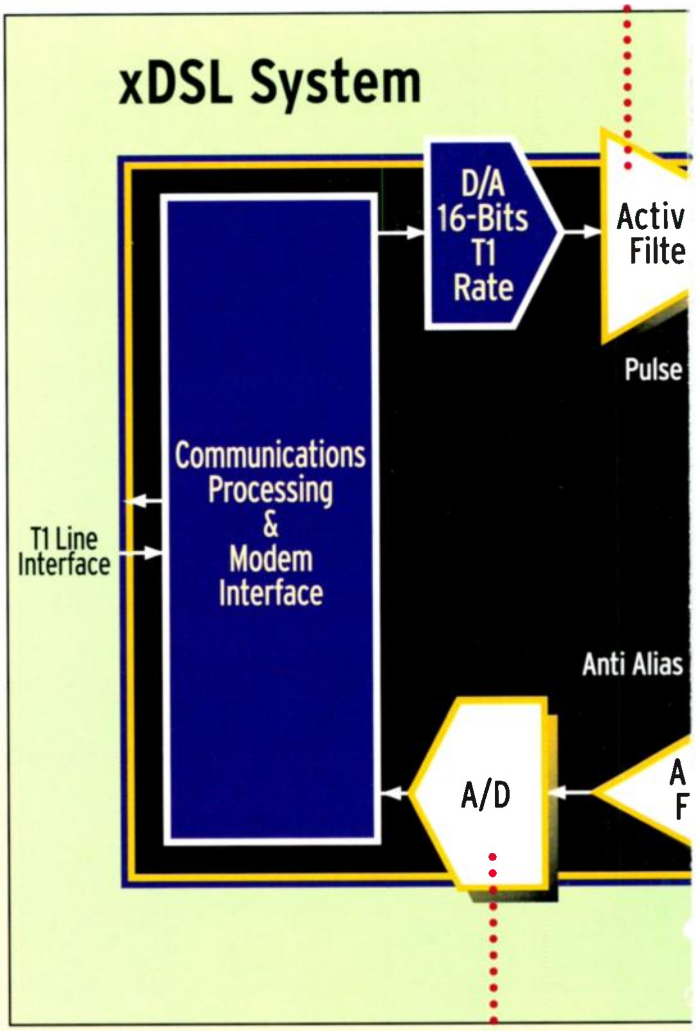

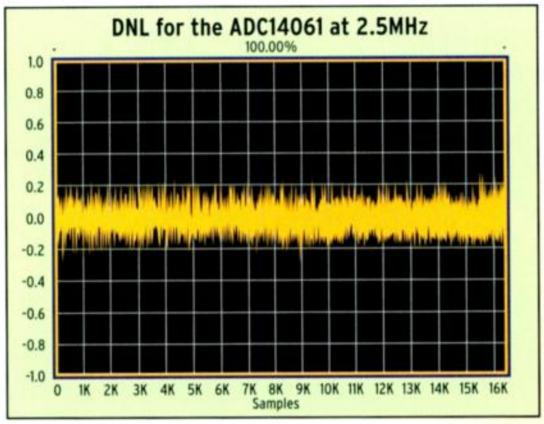

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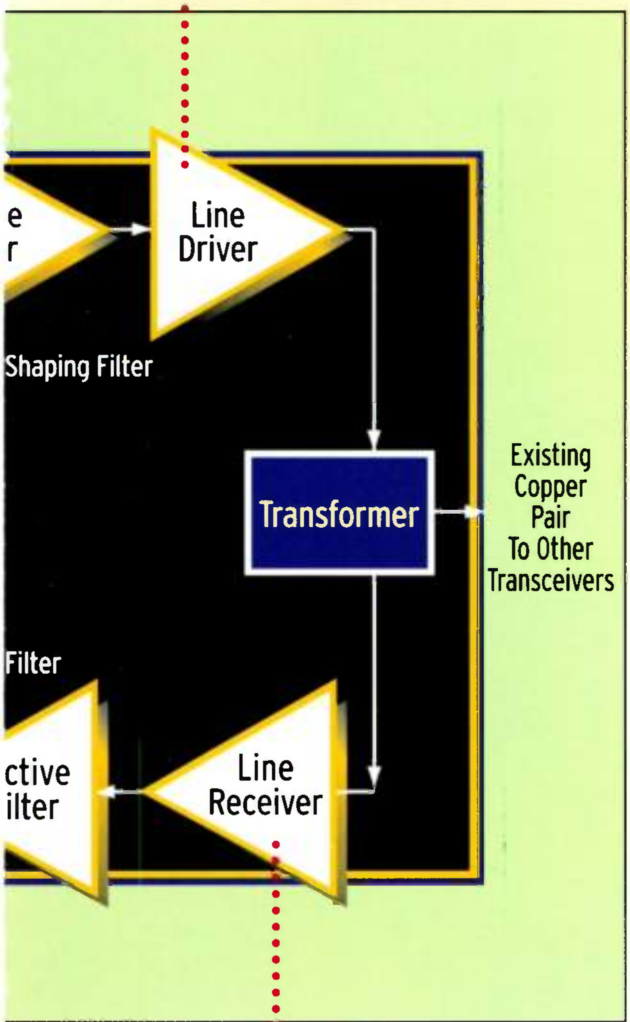

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- 100mA output current

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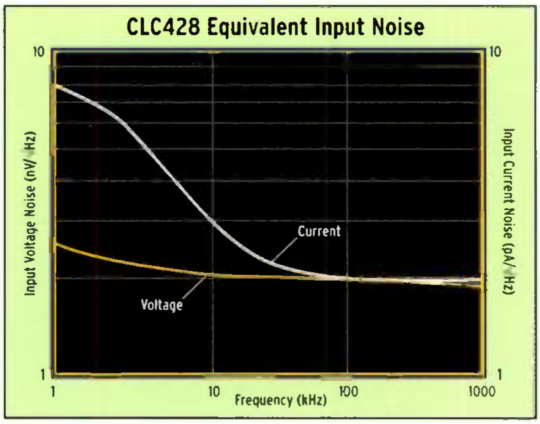


National's High-Speed Receiver Amplifiers
CLC428, CLC425, CLC440, LM6172

CLC428
High-Speed and Low Noise Amp Provides Wide Dynamic Range

- 80MHz small signal bandwidth ($A_V=+2$)
- 2.0nV/√Hz input voltage noise
- 2.0pA/√Hz input current noise

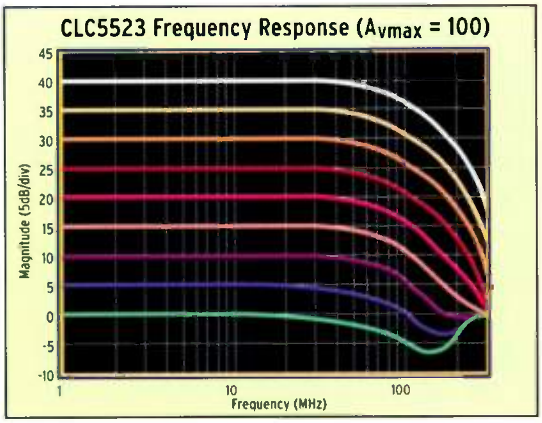
CLC440
Wideband, Low-Power Amp for Video

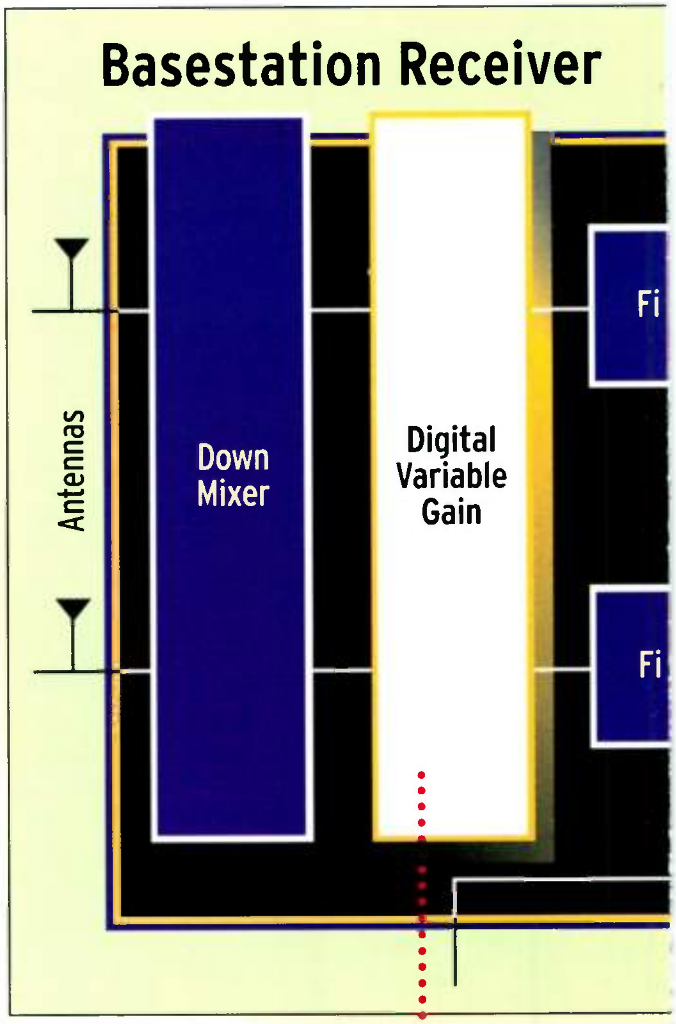
- 260MHz small signal bandwidth ($A_V=+2$)
- 3.5nV/√Hz input voltage noise
- 2.5pA/√Hz input current noise

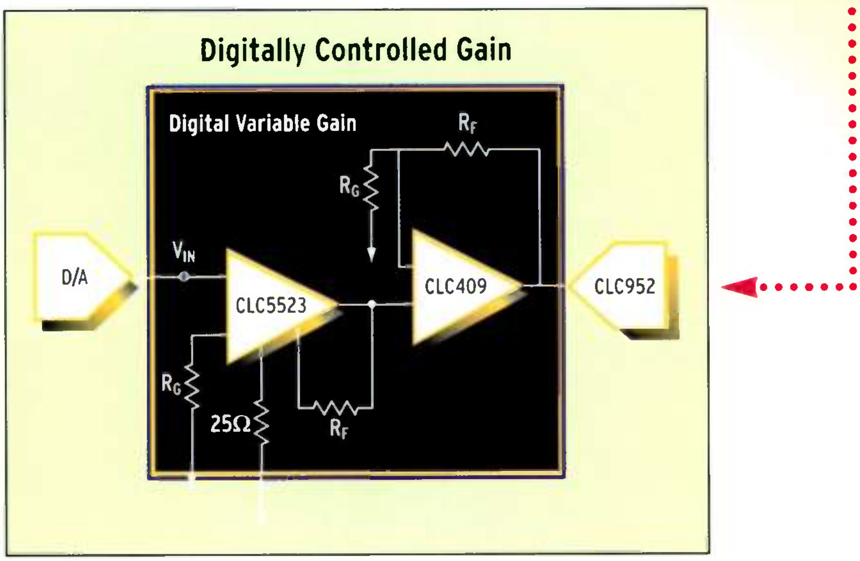
NATIONAL'S ADC AND AMPS FOR DIGITALLY CONTROLLED GAIN CLC5523, CLC409, CLC952

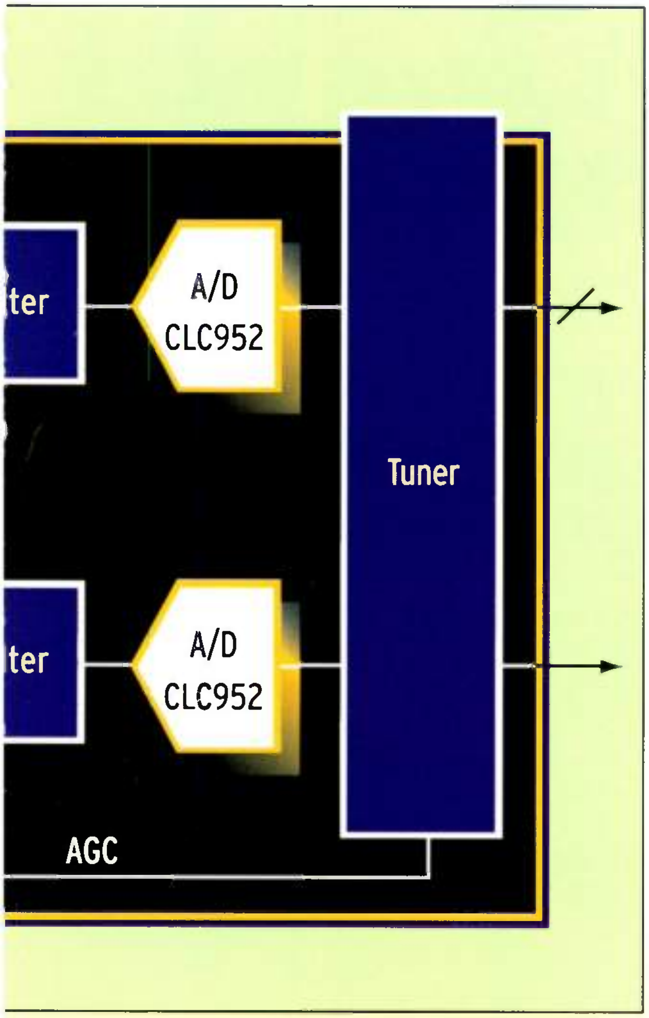
CLC5523 VARIABLE GAIN AMPLIFIER

- 250MHz BANDWIDTH (A_{VMAX} = 10V/V)
- >60dB GAIN ADJUSTMENT RANGE
- +/-3.8V CMIR







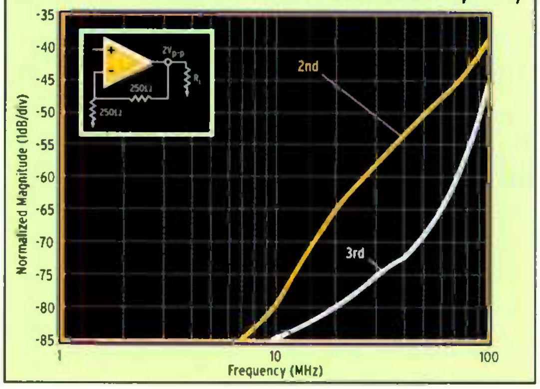


CLC409

LOW DISTORTION HIGH-SPEED AMPLIFIER

- 350MHz BANDWIDTH
- -65/-80 dBc HD AT 20MHz INTO 1kΩ LOAD
- 1200V/μs SLEW RATE

CLC409 Harmonic Distortion vs Load and Frequency

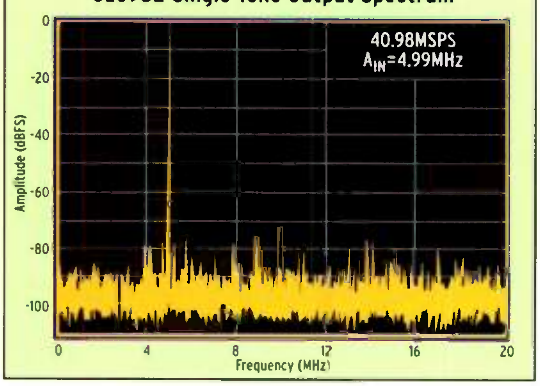


CLC952

41MSPS 12-BIT MONOLITHIC ADC

- 660mW POWER DISSIPATION
- 72dBc SFDR; 64dB SNR
- 28-PIN SSOP PACKAGE

CLC952 Single Tone Output Spectrum



If you are sensing or digitizing a signal and require speed and performance, we have the solutions for you.

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The explosion in internet traffic has placed increasing demands on communications systems. Complex, high-speed analog signals must be transformed into the digital realm with no conversion artifacts. Our products have great performance for communication applications.

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- IF Sampling up to 300MHz
- Excellent Spurious-Free Dynamic Range
- High Signal-to-Noise Ratio
- Small Package Outlines; i.e. TSSOP, TQFP

Amplifiers:

- High Bandwidth (1.1GHz)
- High Output Current to Drive Lines: 85mA, 28Vpp Outputs, -89/-92 HD2/HD3
- Variable Gain Amplifiers (VGAs) for High-Speed AGC Circuits (250MHz Bandwidth) with
    - Programmable Attenuation of Over 80dB
    - Maximum Gain 2 to 100
- TinyPak™ SOT-23
- 5V Single Supplies

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Today's DVD systems, camera systems and camcorders require fast update rates, excellent image quality and small footprints. At National Semiconductor, we understand these requirements.

A/D Converters:

- Excellent Dynamic Performance up to Nyquist Sample Rates
- Superior DNL
- Small Package Outlines; i.e. TSSOP, TQFP

Amplifiers:

- NTSC Diff G/P 0.06/0.02, 130mA Output Current Drive
- TinyPak™ SOT-23
- 5V Single Supplies
- up to 130mA for driving cables

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High-Speed Amplifier Selection Guide

Device	Single/Dual Triple/Quad	Mode	SSBW MHz	A_V at V/V	2nd/3rd HD into R_L = 100Ω	Slew Rate V/μs	I_{CC} mA/ch	NTSC Diff G/P	I_{OUT} mA	Settling Time (to 2V) ns to %	V_{OS} mV	V_{CC} Supply Range	Special Features
CLC109	S	BUF	270	1	-46/-55 at 20MHz	350	3.5	0.7/0.03	30	12 to 0.05	1	±5	Available in SOT23-5
CLC111	S	BUF	800	1	-62/-62 at 20MHz	3500	10.5	0.15/0.04	60	16 to 0.1	1.4	±5	
CLC114	Q	BUF	200	1	-50/-58 at 20MHz	450	3	NA	25	20 to 0.01	0.5	±5	
CLC115	Q	BUF	700	1	-62/-62 at 20MHz	2700	11.25	0.08/0.04	60	12 to 0.1	2	±5	
CLC400	S	CFB	200	2	-60/-60 at 20MHz	700	15	0.01/0.03	70	12 to 0.05	2	±5	
CLC401	S	CFB	150	20	-45/-60 at 20MHz	1200	15	NA	70	10 to 0.1	3	±5	
CLC402	S	CFB	195	2	-50/-60 at 20MHz	800	15	0.01/0.05	55	25 to 0.0025	0.5	±5	
CLC404	S	CFB	175	6	-53/-60 at 20MHz	2600	11	0.07/0.03	70	10 to 0.2	2	±5	
CLC405	S	CFB	110	2	-72/-70 at 1MHz	350	3.5	0.01/.025	60	18 to 0.05	1	±5	Disable Feature
CLC406	S	CFB	160	6	-46/-50 at 20MHz	1500	5	0.02/0.02	70	12 to 0.05	2	±5	Available in SOT23-5
CLC409	S	CFB	350	2	-49/-59 at 60MHz	1200	13.5	0.01/0.01	70	8 to 0.1	0.5	±5	Available in SOT23-5
CLC410	S	CFB	200	2	-60/-60 at 20MHz	700	16	0.01/0.01	70	5 to 0.05	2	±5	Disable Feature
CLC411	S	CFB	200	2	-48/-52 at 20MHz	2300	11	0.02/0.03	70	15 to 0.1	2	±15	Disable Feature
CLC412	D	CFB	250	2	-46/-50 at 20MHz	1300	5.1	0.02/0.02	70	12 to 0.05	2	±5	
CLC416	D	CFB	120	2	-65/-57 at 10MHz	400	3.9	0.01/0.03	60	22 to 0.05	1	±5	
CLC420	S	VFB	95	2	-50/-53 at 20MHz	1100	4	NA	70	18 to 0.01	1	±5	
CLC425	S	VFB	95	20	-53/-75 at 10MHz	350	15	0.04/0.025	90	22 to 0.2	0.1	±5	Available in SOT23-5
CLC426	S	VFB	130	2	-62/-68 at 10MHz	400	11	NA	80	16 to 0.05	1	±5	Adjustable Supply Current
CLC428	D	VFB	160	1	-62/-72 at 10MHz	500	11	NA	80	16 to 0.1	1	±5	
CLC430	S	CFB	75	2	-89/-92 at 1MHz	2000	11	0.03/0.05	85	35 to 0.05	1	±5 to ±15	Disable Feature
CLC431	D	CFB	62	2	-65/-75 at 1MHz	2000	7.1	0.12/0.12	60	70 to 0.05	3	±5 to ±15	Disable Feature
CLC432	D	CFB	62	2	-65/-75 at 1MHz	2000	7.1	0.12/0.12	60	70 to 0.05	3	±5 to ±15	
CLC440	S	VFB	750	1	-64/-70 at 5MHz	1500	7	0.015/0.025	90	10 to 0.05	1	±5	
CLC446	S	CFB	400	2	-54/-50 at 50MHz	2000	4.8	0.02/0.03	48	9 to 0.1	2	±5	
CLC449	S	CFB	1100	2	-44/-62 at 50MHz	2500	12	0.03/0.02	90	11 to 0.1	3	±5	
CLC450	S	CFB	135	2	-86/-65 at 1MHz	370	1.6	0.03/0.3	130	15 to 0.05	2	+5 to ±5	
CLC451	S	PGB	100	2	-72/-65 at 1MHz	350	1.6	0.3/0.3	130	20 to 0.05	3	+5 to ±5	Available in SOT23-5
CLC452	S	CFB	160	2	-77/-72 at 1MHz	540	3.2	0.05/0.08	130	20 to 0.05	1	+5 to ±5	Available in SOT23-5
CLC453	S	PGB	130	2	-82/-73 at 1MHz	460	3.2	0.3/0.1	130	20 to 0.05	7	+5 to ±5	Available in SOT23-5
CLC501	S	CFB	75	32	-45/-60 at 20MHz	1200	18	NA	70	12 to 0.05	1.5	±5	Available in SOT23-5
CLC502	S	CFB	150	2	-50/-60 at 20MHz	800	17	NA	55	25 to 0.0025	0.5	±5	
CLC505	S	CFB	50	6	-50/-65 at 20MHz	800	1	NA	45	35 to 0.05	2	±5	Adjustable Supply Current
CLC5602	D	CFB	135	2	-86/-85 at 1MHz	300	1.6	0.06/0.02	130	15 to 0.05	2	+5 to ±5	
CLC5612	D	PGB	90	2	-74/-86 at 1MHz	290	1.6	0.15/0.02	130	17 to 0.05	3	+5 to ±5	
CLC5622	D	CFB	160	2	-95/-95 at 1MHz	370	3.2	0.05/0.03	130	18 to 0.05	1	+5 to ±5	
CLC5623	T	CFB	148	2	-78/-94 at 1MHz	370	3.2	0.06/0.06	130	18 to 0.05	1	+5 to ±5	
CLC5632	D	PGB	130	2	-82/-69 at 1MHz	410	3.2	0.08/0.02	130	17 to 0.05	7	+5 to ±5	
CLC5633	T	PGB	130	2	-73/-92 at 1MHz	410	3.2	0.03/0.06	130	20 to 0.05	7	+5 to ±5	
CLC5644	Q	CFB	170	1	-72/-79 at 5MHz	1000	2.5	0.04/0.07	70	16 to 0.1	2.5	±5	
CLC5654	Q	CFB	450	1	-71/-82 at 5MHz	2000	5	0.03/0.03	70	12 to 0.1	2.5	±5	
CLC5665	S	CFB	90	1	-89/-92 at 1MHz	1800	11	0.05/0.05	85	35 to 0.05	1	±5 to ±15	Disable Feature

HIGH-SPEED AMPLIFIER SELECTION GUIDE: CONTINUED

Device	Single/Dual Triple/Quad	Mode	SSBW MHz	Av at V/V	2nd/3rd HD into $R_L = 100\Omega$	Slew Rate V/µs	I_{CC} mA/ch	NTSC Diff G/P	I_{OUT} mA	Settling Time (to 2V) ns to %	V_{OS} mV	V_{CC} Supply Range	Special Features
LM6171	S	VFB	160	1	-72/-70 at 1MHz	3600	2.5	0.03/0.5	100	35 to 0.1	1.5	±5 to ±15	
LM6172	D	VFB	160	1	-72/-70 at 1MHz	3000	2.3	0.28/0.6	90	65 to 0.1	0.4	±5 to ±15	
LM6181	S	CFB	100	2	-50/-55 at 10MHz	2000	7.5	0.05/0.04	100	50 to 0.1	2	±5 to ±15	
LM6182	D	CFB	100	2	-50/-55 at 10MHz	2000	7.5	0.05/0.04	100	50 to 0.1	2	±5 to ±15	
LM7121	S	VFB	235	1	NA	1300	5.3	NA	20	74 to 0.1	0.9	±5 to ±15	Available in SOT23-5
LM7131	S	VFB	90	1	-74/-94 at 1MHz	120	7.0	NA	65	NA	0.02	±5, +5, +3	Available in SOT23-5
LM7171	S	VFB	220	2	-70/-51 at 5MHz	4100	6.5	0.01/0.02	100	42 to 0.1	0.2	±5 to ±15	

HIGH-SPEED A/D CONVERTER SELECTION GUIDE

						Static		Dynamic								
Device	Resolution	Speed	Power	Supply	V_{IN}	DNL	INL	ENOB	SINAD	SNR	THD	SFDR	BW	Package	Eval Board	1K Price*
ADC1173	8-Bit	15MSPS	37mW	3V	$2V_{pp}$	±0.4	±0.5	7.4 Bits	46dB	47dB	-54dB	-51dB	120MHz	24 pin TSSOP, EIAJ	Yes	$2.84
ADC1175	8-Bit	20MSPS	67mW	5V	$2V_{pp}$	±0.35	±0.5	7.4 Bits	46dB	47dB	-53dB	-53dB	120MHz	24 pin TSSOP, EIAJ	Yes	$2.84
ADC08351	8-Bit	50MSPS	65mW	3V	$2V_{pp}$	±0.5	±0.5	6.5 Bits	41dB	42dB	-47dB	-48dB	150MHz	20 pin TSSOP	No	$2.05
ADC10321	10-Bit	20MSPS	98mW	5V	$2V_{pp}$	±0.33	±0.39	9.2 Bits	57dB	58dB	-60dB	-65dB	–	32 pin TQFP	Yes	$3.18
ADC12081	12-Bit	5MSPS	105mW	5V	$2V_{pp}$	±0.35	±0.6	10.9 Bits	67.6dB	68dB	-79dB	-79dB	100MHz	32 pin TQFP	Yes	$15.42
ADC12181	12-Bit	10MSPS	235mW	5V	$2V_{pp}$	±0.4	±0.7	10.4 Bits	64.5dB	65dB	-74dB	-73dB	100MHz	32 pin TQFP	Yes	$16.92
ADC12281[1]	12-Bit	20MSPS	400mW	5V	$2V_{pp}$	±0.4	±0.7	10.2 Bits	62dB	63dB	-73dB	-73dB	100MHz	32 pin TQFP	Yes	$19.98
CLC952	12-Bit	41MSPS	660mW	±5V	$1V_{pp}$	+1.4/-1.0	±3.0	10.2 Bits	63.2dB	64dB	-70dB	-72dB	180MHz	28 pin SSOP	Yes	$20.70
CLC5956	12-Bit	65MSPS	615mW	5V	$2V_{pp}$ (Diff)	±0.65	±1.7	10.5 Bits	65.2dB	67dB	-71dB	-73dB	300MHz	48 pin TSSOP	Yes	$29.80
ADC14161[2]	14-Bit	2.5MSPS	390mW	5V	$2V_{pp}$	±0.3	±0.75	12.8 Bits	79dB	80dB	-88dB	-90dB	8MHz	52 pin TQFP	Yes	$29.40
ADC16061[2]	16-Bit	2.5MSPS	390mW	5V	$2V_{pp}$	±1.0	±3.0	12.8 Bits	79dB	80dB	-88dB	-91dB	8MHz	52 pin TQFP	Yes	$36.90

VARIABLE GAIN AMPLIFIER PRODUCTS

Device	Single	Single Channel BW (MHz)	Control Channel BW (MHz)	Gain Adjust Range (dB)	Slew Rate (Typ) SR (V/µs)	Supply Voltage V_S (V)	Supply Current (Typ) I_S (mA)	Common Mode Input Range (typ) CMIR (V)	Comments
CLC520	S	$\lvert A_V \rvert = 2$ 500	100	-40	2000	±5	28	±2.2	Non-Linear Gain Control (dB/V)
CLC522	S	$\lvert A_V \rvert = 2$ 330	165	-40	2000	±5	46	±2.2	Linear Gain Control (V/V)
CLC5523	S	$\lvert A_V \rvert = 10$ 230	95	-60	1700	±5	14	±3.8	Non-Linear Gain Control (dB/V)

* Price shown is for 1000 units in USD, FOB Santa Clara, CA USA [1] f_{in} = 4.4MHz [2] f_{in} = 500KHz All specifications typical unless otherwise noted.

570266-001

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New Home Network Technologies Piggyback On Existing Phone And Power Lines

Home local-area networks (LANs) are on their way, thanks in part to the demand caused by the increasing use of computers at home and the deployment of residential broadband data services. A savvy public has begun to realize that computers are no longer isolated devices, and to demand a convenient way to enjoy the same convenience that LANs give them at work. If electronics manufacturers have their way, products will be available by the end of 1999 that let a user connect to an ADSL or cable modem and share the broadband pipe with all other PCs or devices in the home. Doing this will simply require plugging into the telephone jack with an adapter or network interface card.

While manufacturers have recognized this need, they also know that most consumers aren't interested in rewiring their homes for networking. This has led to a concerted effort to find ways to ship data around using whatever's already there. While some promising wireless technologies are on the horizon, two important players recently have emerged in a race to use existing wiring within the home to deliver high-speed data.

One promising scheme is a technology promoted by the Home Phoneline Networking Alliance (HomePNA). It's an adaptation of the mature IEEE-802.3 CSMA/CD technology used for Ethernet, which can transport up to 1 Mbit/s over a home's phone wiring. Major backers of HomePNA include 3Com, Santa Clara Calif.; AMD, Sunnyvale, Calif.; AT&T Wireless, Seattle, Wash.; Compaq, Houston, Texas; Epigram, Sunnyvale, Calif.; Hewlett-Packard, Palo Alto, Calif.; IBM, Yorktown Heights, N.Y.; Intel, Santa Clara, Calif.; Lucent Technologies, Berkeley Heights, N.J.; Rockwell Semiconductor Systems, Redondo Beach, Calif.; and Tut Systems, Pleasant Hill, Calif.

The other emerging home networking technology has been developed by Intellon Corp., Ocala, Fla. It uses enhanced orthogonal frequency-division multiplexing (IeOFDM) and spread-spectrum carrier (SSC) techniques developed by Intellon to achieve data rates of 1 Mbit/s over existing power lines. Microsoft Corp., Redmond, Wash., is the first licensee of this technology and has become an ally in Intellon's "No New Wires" initiative. Together, they hope to develop affordable networking devices that can send digital voice, video, and Internet data to and around a home, office, or other buildings. According to developers at Intellon, this same OFDM technology is applicable to RF links and provides the foundation for establishing robust, high-rate wireless networks within a home or office.

HomePNA: Old MAC, New PHY

The HomePNA technology uses straightforward IEEE-802.3 carrier sense multiple access/collision detect (CSMA/CD) methods for multiple access to a common communications medium—the foundation of Ethernet. In simple terms, it's a 1-Mbit/s Ethernet over a phoneline. This is an important design criterion, since it allows the HomePNA network to leverage the tremendous amount of Ethernet-compatible software, applications, and hardware in the market today. The PCI bus device driver (NDIS 4/5) sees an Ethernet MAC to drive. Initially, users will be able to connect up to 25 PCs, peripherals, and network devices inside a home.

Transmitting data accurately over the random phoneline topology is only part of the problem. For a high data throughput, one must encode as much data as possible so that multiple data bits are sent in each signal pulse, rather than single pulse bits.

The core technology in the HomePNA scheme is the time-modulation line-coding method, which allows the system to transmit data on an arbitrary topology of unterminated wires found in homes. A line-coding mechanism incorporates an adaptive circuit which, by design, can adapt to varying noise. Within each network interface, the receiver circuit adapts to varying noise levels that might appear on the line. In addition, the transmitting circuit can vary its level of output signal strength. Both transmit and receive circuits continually monitor line conditions and adjust accordingly.

The HomePNA specification is designed to ensure compatibility with other communications services within the home, like voice, ISDN, and xDSL data services. One common method for simultaneously operating multiple services over a single pair of wires is frequency-division multiplexing (FDM). With FDM, each communications service is assigned to a different frequency spectrum. Frequency-selective filters allow devices using one type of service to exchange information without interference from other services that communicate in another band.

The HomePNA technology employs the 5.5-to-9.5-MHz portion of the RF spectrum. Passband filters in this region attenuate frequencies below 5.5 MHz very rapidly, so there's no interference with other DSL services or traditional phones. The technology also coexists with the new splitterless Universal ADSL standard. It's fully compatible with the Ethernet MAC layer standard (IEEE-802.3 CSMA/CD with a new physical layer) and meets applicable FCC regulatory requirements.

In accordance with its goal of delivering parts for HomePNA interface cards for under $50 (retail) within the year, AMD expects to announce a part this month. Intended for PC motherboards and add-on cards, it will have full HomePNA capability and cost under $20.

While the 1-Mbit/s rate will be more than adequate for most applications today, the HomePNA alliance is looking toward the future. It has created a technical subcommittee whose sole responsibility is to specify, design, and implement the next-generation technology. Epigram, as a founding member, is focusing its effort on developing these next-generation products and technologies, aiming to achieve 10 Mbits/s and higher while maintaining backwards-compatibility with the initial specification. Other current and future members also will contribute to developing the next-generation home phoneline specification.

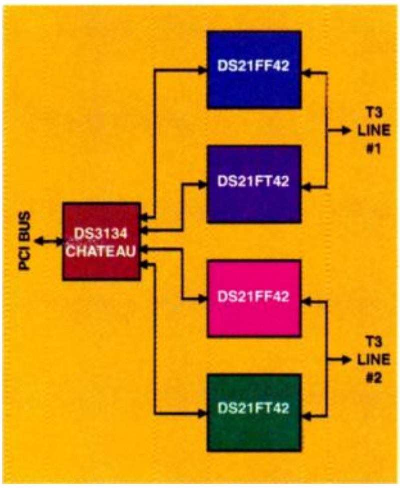
OFDM: Data Over AC Lines

Intellon's enhanced version of OFDM (IeOFDM) is essentially the simultaneous transmission of a large number of narrow-band carriers, sometimes called subcarriers. Each is modulated with a

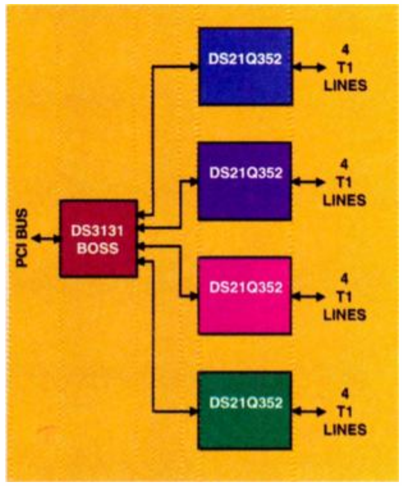
Pack It In.

High Density T1/E1 Chips From Dallas Semiconductor

At crowded T1 and E1 junctions, you need more interface in less space. To meet the challenge, new chips from Dallas Semiconductor define density at a higher level. For instance—



Need an HDLC controller for a channelized T1/E1 design? Try putting 256 channels through one chip. The new DS3134 CHATEAU docks 64 T1 or E1 lines—or two T3/E3/HSSI lines.



Designing a DSLAM? POS? Any high-density, clear-channel T1/E1 application? One DS3131 BOSS (Bit- and Octet-SynchronouS) HDLC Controller masters up to 40 DSL lines or 40 T1/E1 lines.

In each case, five high-density chips from Dallas Semiconductor replace 16 fluffier chips from the competition. Both controllers rely on extra-deep FIFOs and super-efficient DMA engines to boost performance. Programmable options, onboard Bit Error Rate Testing and local bus access give them flexibility.

Alongside the HDLC controllers starring here, supporting players star on their own:

- **4- 12- and 16-Channel T1 & E1 Framers:** These chips supply multiple density options for maximum flexibility with the smallest footprint and lowest cost.
- **Quad T1 & E1 Transceivers:** Four long- and short-haul line interfaces and four full-featured framers team up in one space-saving package, available in 3.3V and 5V options.

Enough talk. Give us a call or check out our Web site. Find out how these new high-density chips can help your design win the T1/E1 game.

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low data rate, but the total yields a very high data rate. To obtain high spectral efficiency, the frequency responses of the subcarriers are overlapping and orthogonal, hence the name OFDM. Each narrow-band subcarrier can be modulated using various formats. BPSK, QPSK, and QAM (or the differential equivalents) are commonly used.

Since their modulation rates are very low, each subcarrier experiences flat fading in a multipath environment and is easy to equalize. The need for equalization can be eliminated by selecting a relatively small subcarrier spacing and using differential QPSK (DQPSK) modulation, where data is encoded as the difference in phase between subcarriers. Each subcarrier pair experiences flat fading due to the narrow bandwidth it occupies. The difference in phase and amplitude error between them is small. Differential modulation also can be encoded as the difference in phase between present and previous symbols in time on the same subcarrier.

To prevent signal loss and inter-symbol interference caused by the many reflected signals within a power line network, a cyclic prefix is added to the IeOFDM symbol. This helps to maintain complete orthogonality in a time-dispersive channel. This prefix copies the last part of the symbol and adds the copy to the beginning of the symbol. The long IeOFDM symbol time (generally many microseconds), combined with the cyclic prefix (usually a small percentage of the IeOFDM symbol time), are key factors that enable performance in a time-dispersive channel.

Future Developments

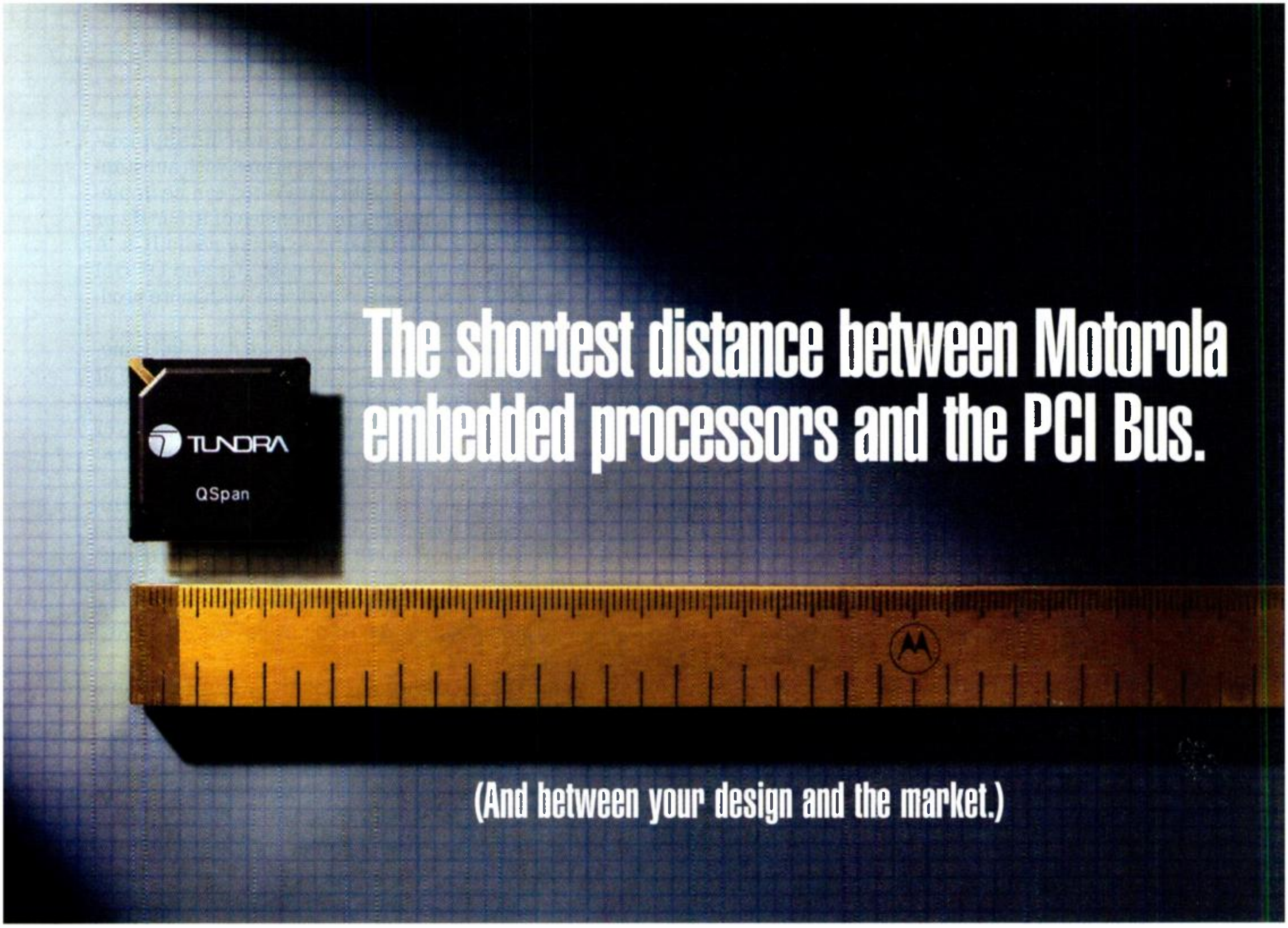
As part of Intellon's IeOFDM research program, VHDL has been used to develop the FFT processor, the heart of an IeOFDM receiver. A fast FFT processor is the key to attaining high data rates. The exercise proved that the required speeds could be achieved within a low cost CMOS IC. VHDL was also used in the design of a Viterbi decoder, which was tested in an FPGA. Reliable data rates of up to 10 Mbits/s can be achieved on power lines at frequencies above 2 MHz.

In addition to power-line applications, wireless systems with substantially higher data rates can be implemented at frequencies of 915 MHz or 2.4 GHz using existing radio ICs. A number of low-cost ICs and OFDM modules are available, with more products in development.

For general information on HomePNA, visit the alliance's Web site at www.homepna.org. For more information HomePNA's transmission layer technology, contact Amanda Burman at Tut Systems, 2495 Estand Way, Pleasant Hill, CA 84523; (925) 682-6510; www.tutsys.com. For more information on HomePNA and related semiconductor products, contact AMD, One Technology Place, MS-52, Sunnyvale, CA 94088, (800) 222-9323, (408) 749-5703; www.amd.com.

For more about the No New Wires initiative and associated technologies, contact Intellon Corp., 5100 West Silver Springs Blvd., Ocala, FL 34482; (352) 237-7416; e-mail: kurt.kyvik@intellon.com; www.intellon.com.

Lee Goldberg



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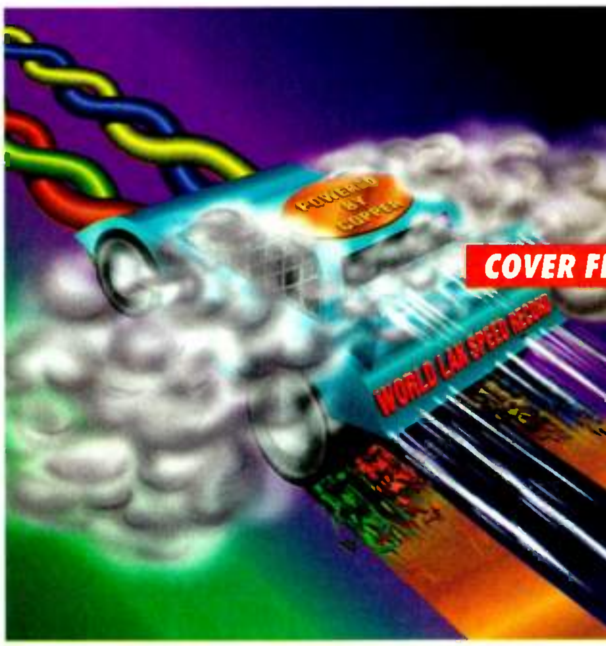
READER SERVICE 131

Gigabit Ethernet PHY Chip Sets LAN Speed Record For Copper

With 150 Billion DSP Operations/s, The First IEEE 802.3ab-Compliant IC Delivers Gigabit Ethernet Over CAT-5 Twisted Pairs.

Lee Goldberg

COVER FEATURE



Give me your tired networks, your poorly budgeted LAN managers, your huddled, bandwidth-starved masses, yearning to FTP freely," says Yossi Cohen, director of Broadcom Corp.'s networking business unit. With apologies to poet Emma Lazarus[1], he's justifiably proud of the BCM5400, Broadcom's new physical-layer device for 1000Base-T Ethernet. This innovative chip may soon make it possible for networks to have Gigabit connections over their copper wiring at only a small premium over the cost of standard 100-Mbit/s Fast Ethernet.

Copper's Hot Again

Developed by Broadcom Corp., Irvine, Calif., the BCM5400 is a single-chip PHY device. It moves Ethernet frames at full-duplex Gigabit speeds for up to 100 meters over four pairs of ordinary Category-5 (Cat-5) twisted-pair copper wire *(see the figure)*. It's the first implementation of the IEEE's 803.3ab, 1000Base-T standard for UTP-based (unshielded twisted pair) Gigabit Ethernet.By enabling the inexpensive re-use of already installed wiring bases, Broadcom and other 1000Base-T supporters hope to encourage rapid adoption of Gigabit Ethernet technologies. Then, they could meet the demands for bandwidth, which are increasing much more rapidly than the budgets of most network managers' budgets.

While Gigabit Ethernet has been around for a while, practical copper-based technologies are the new kid on the block. Borrowing heavily from FibreChannel technology, fiber-based optical systems have now been around for a year or more. The only copper Gigabit solutions have been limited to short coaxial-cable links intended to span a few meters between servers, switches, or routers sharing the same wiring closet. This all changed with the recent approval of the 1000Base-T standard *(see "The ABCs Of 803.3ab," p. 42)*.

Copper Gigabit's proponents point to a couple of important factors that convince them that it's a winner. The first is the cost of a connection. Although the price of optical transceivers has come down sharply as demand climbed, the cost of making an optoelectronic assembly remains much higher than producing a PHY-layer silicon chip and its associated passive components. Optical terminations also are more complicated and expensive to make than copper, requiring splicing and inspection equipment along with extensive training.

The extensive installed base of Cat-5 wiring found in most buildings makes another compelling case for the Broadcom solution. By allowing network managers to "recycle" their copper infrastructure, a 1000Base-T transceiver makes upgrading connections between backbone and edge devices much easier and less expensive. In many cases, it could simply mean changing line cards in two boxes at each end of the cable.

1500 GOPS??!

To accomplish this, Broadcom's designers pushed the leading edge of commercial design practices. Among other things, the BCM5400 relies heavily on advanced digital filtering and signal processing to deal with the considerable attenuation, crosstalk, and echoes experienced by high-speed signals when traveling over common

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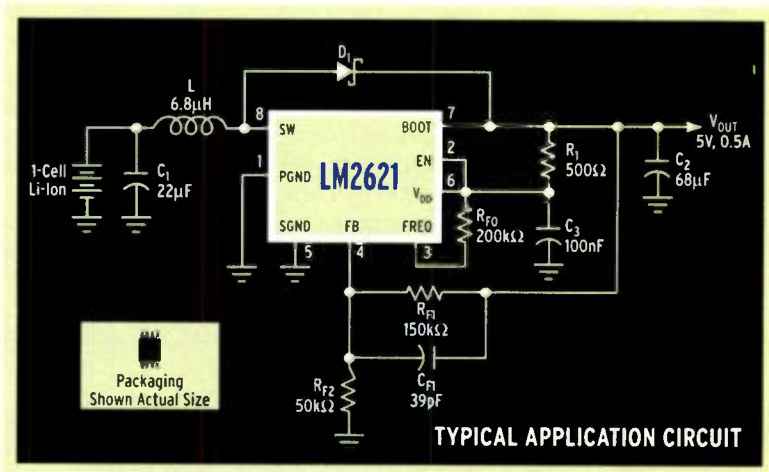

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The ABCs Of 802.3ab: A Gigabit Ethernet Primer

Gigabit Ethernet over a copper medium is a follow-up to the very popular and widely used Fast Ethernet 100-Mbit/s technology for copper media and desktop LANs. Communication throughput of 1 Gbit/s is achieved with four pairs of twisted-pair cables and eight transceivers (four at each end) operating at 250 Mbits/s each *(Fig. a)*. The necessity of full-duplex bidirectional operation dictates the use of hybrid circuits at the two ends of each pair, as well as a series of echo canceller circuits on each channel.

While the transmitter on each end has a relatively simple task to perform, the receiver has to operate under the the harsh conditions experienced by high-frquency signals as they pass through the uncontrolled environment that characterizes the modern LAN cable infrastructure. To work properly, a Gigabit Ethernet transceiver must cope with the following line impairments :

- Worst-case cable attenuation
- Worst-case echo from its own transmitter
- Worst-case near-end crosstalk (NEXT) from the three transmitters in adjacent wire pairs
- Worst-case far-end crosstalk (FEXT) from the transmitter at the other end of the cable

To reliably recover the transmitted information in a noisy environment, the receiver has to perform a considerable amount of digital adaptive filtering for channel equalization, NEXT cancellation, and echo cancellation.

Modulation And Coding

The IEEE 802.3ab task force settled on baseband 5-level pulse-amplitude modulation (PAM), combined with trellis coding and partial-response shaping, as the basis for the transmission scheme employed for a Gigabit Ethernet copper transceiver known as a 1000Base-T transceiver. The scheme uses a five-level (-2, -1, 0, +1, +2) PAM signal on each pair of wires to code 2 bits of information (2 bits/symbol) at a symbol rate of 125 MHz, resulting in a 250-Mbit/s transfer rate on each pair *(Fig. b)*. Coding 2 bits of information requires only 4 levels; the extra level in the PAM-5 scheme used here provides a code redundancy. This can be used for control signals, as well as improving the performance using a trellis coder at the transmitter and a Viterbi decoder at the receiver.

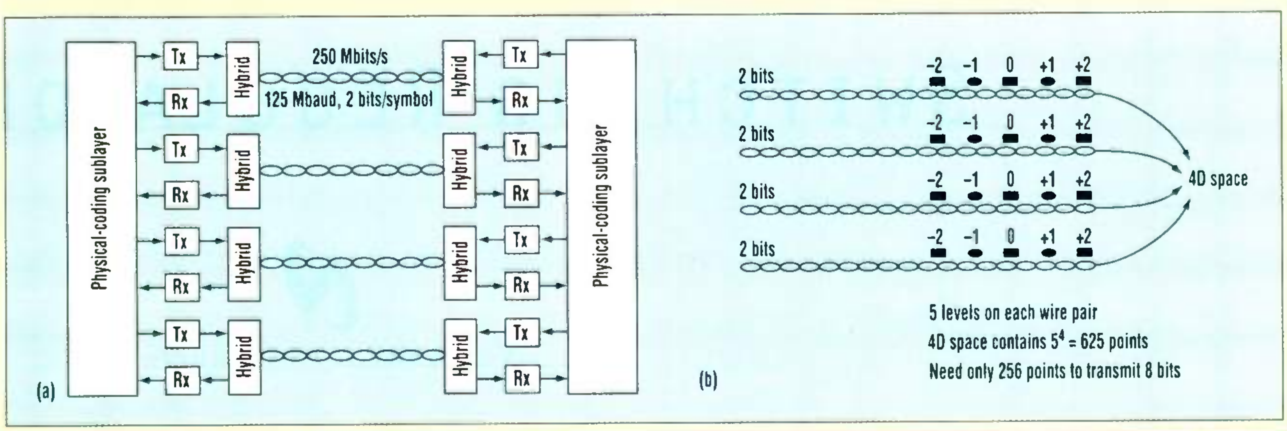
A total of 8 bits is being transmitted at the 125-MHz symbol rate over the four pairs of wires. Each pair uses a five-point, 1-dimensional (1D) constellation containing the symbols (-2, -1, 0, +1, +2). Looking at the four pairs collectively to form a 4-dimensional constellation (each wire pair represents one of the dimensions), the total number of available 4D points is $5^4 = 625$. To transfer the 8 bits of information, only 256 points are needed. The existing redundancy can be used to achieve a gain of either 3 or 6 dB, depending on whether or not a Viterbi decoder is used at the receiver.

The minimum squared distance between the points in each subset of transmitted symbols combines with a trellis encoder at the transmitter and a Viterbi decoder at the receiver to provide up to 6 dB of gain in SNR. With this gain, the required SNR for achieving a bit error rate (BER) of 10^{-10} is 19.3 dB.

In this case, the detection at the receiver is no longer performed on a symbol-by-symbol basis, but rather on a sequence basis where the Viterbi decoder selects a sequence of symbols with the lowest probability of error (maximum likelihood sequence estimation).

The PAM-5 modulation scheme for the Gigabit Ethernet long-haul copper standard (1000Base-T) uses partial-response spectrum shaping of the form $0.75 + 0.25z^{-1}$ to limit emissions within the FCC's requirements. This simple filter shapes the spectrum at the output of the transmitter so that its power-spectral density falls under that of the 100Base-Tx—a widely used and accepted Fast Ethernet standard for 100-Mbit/s operation on two pairs of Category-5 twisted-pair cables. In this way, Gigabit Ethernet is able to gracefully overlay any existing 10/100Base infrastructure that is already in place.

Contributed by Medhi Hatamian, director of DSP microelectronics technology; Oscar E. Agazzi, senior staff scientist; and John Creigh, staff scientist at Broadcom Corp., Irvine, Calif.



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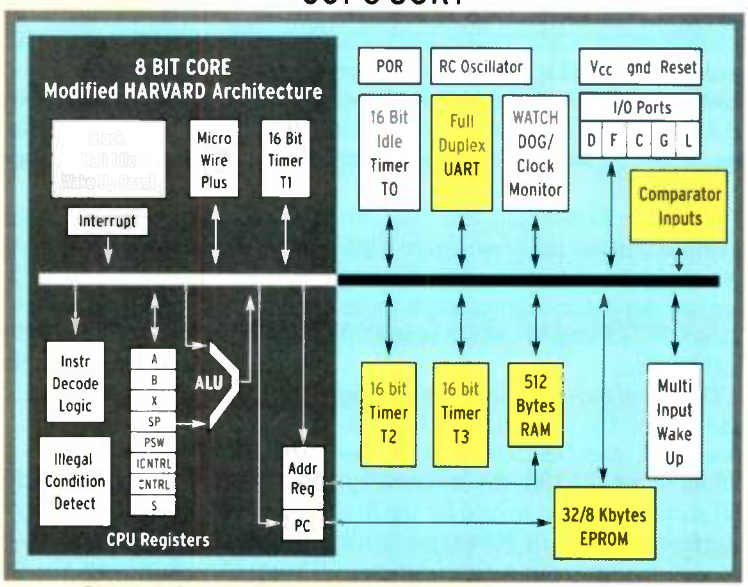

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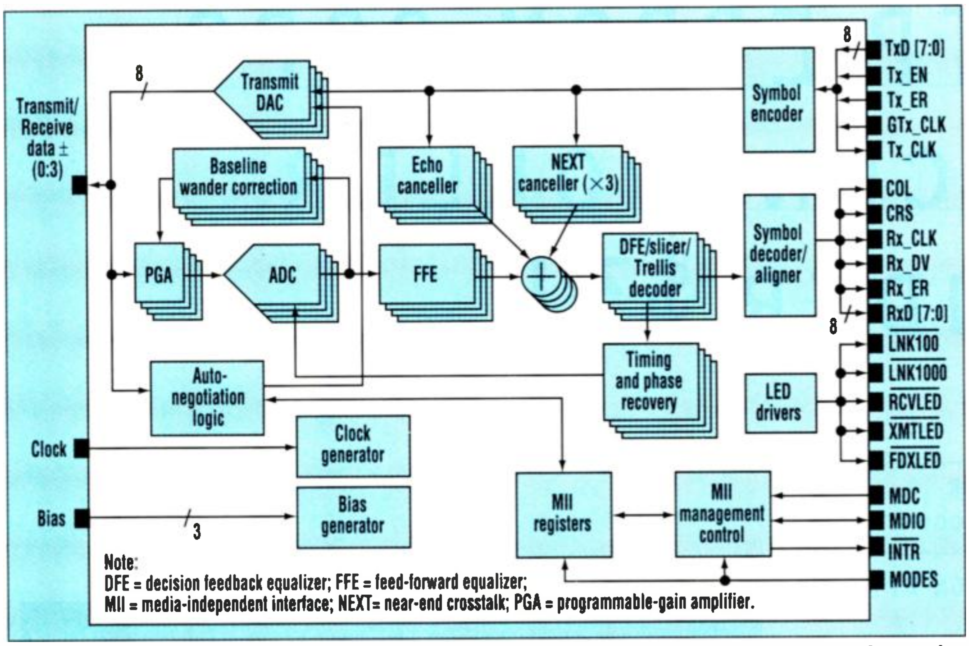

Broadcom's BCM5400 contains all the functional blocks to implement a physical-layer connection for Gigabit Ethernet. Since it transmits across four wire pairs, the chip integrates four each of every line component, including echo cancellers and equalizers. In addition, each channel has three crosstalk cancellers (one for each adjacent line). For simplicity, this block diagram illustrates the components for a single channel.

UTP copper. Performing this near-impossible feat actually requires high levels of integration and processing that are more than equivalent to those of the CPUs found in today's powerful workstations.

There are several important analog functions on the chip, such as the high-speed ADC and DAC circuitry, phase-locked loops (PLLs), clock recovery, and an active analog hybrid for the line interface. But, the BCM5400 performs the vast majority of its signal processing in the digital domain. Receiving each bit in an Ethernet frame requires around 150 logical operations to perform the adaptive filtering, equalization, and processing operations described above. Since the magnitude of this task far exceeds any commercially available DSP, the BCM5400 uses a distributed array of tightly designed logic cores. The pipelined network of distributed-feedback equalizers (DFEs), finite-impulse-response (FIR) filters, and other DSP blocks simultaneously accomplishes the many tasks which consume a cool 150,000 million DSP operations (150 GOPS) per second!

At first glance, using the equivalent of a small supercomputer's processing power to simply shove a bunch of bits down a few feet of cable would seem to be a case of gross overkill. On second glance, however, a seasoned engineer might find it a miracle that such a feat is possible at all. To understand why, it might be a good idea to look a bit more closely at the line impairments that a copper Gigabit transceiver faces—as well as possible remedies.

A Look At The Chip

The first phenomenon Broadcom's designers needed to worry about was attenuation. Over the 100-meter distance of a connection, the twisted-pair line displays sharp and nonlinear attenuation characteristics. These tend to vary with temperature and time. Experience with 100-Mbit/s Fast Ethernet taught Broadcom's designers the value of using high-speed digital DFE to perform complex, real-time compensation to solve this sort of problem.

For a Gigabit Ethernet transceiver to work successfully, it must deal with the echo from its own transmitter. A digital echo canceller on each receiver handles this task nicely. More challenging to deal with is the phenomenon of near-end crosstalk (NEXT), which results from the close proximity of the other three wire pairs. This requires that each receiver employ three separate cancellation filters per channel. Each of these samples the energy from its neighbors and produces error signals to cancel crosstalk at the receiver input.

The chip itself has been fabricated in 0.3-µm CMOS with four metallization layers. In its transceiver, the Gigabit Medium Independent Interface (GMII) receives data in byte-wide format at the rate of 125 MHz. The GMII passes this data on to the physical coding sublayer (PCS), which performs scrambling, coding, and a variety of control functions.

To keep the chip's block diagram from becoming totally unreadable, it shows only one of the four channels operating simultaneously.

The PCS block generates four 1-dimensional symbols, each representing 2 bits of data, for the four channels. The corresponding symbol for each channel goes through a shaping function, followed by a 125-MHz DAC, low-pass filtering, and line-driver/hybrid circuitry.

The received analog signal is preconditioned on the receive path. The signal is passed through a 125-MHz ADC that's sampled by a clock provided by a decision-directed timing-recovery circuit. A feed-forward equalizer (FFE), which is an LMS-type adaptive filter performing channel equalization and precursor Inter Symbol Interference (ISI) cancellation, filters the ADC's output. As said earlier, the symbols sent by the other three local transmitters cause impairments in the received signal for each channel through a NEXT mechanism between the pairs.

Since each receiver has access to the data for the other three pairs causing this interference, it's possible to nearly cancel the effect. This is accomplished with three adaptive NEXT canceling filters *(see the figure, again)*. Adding the outputs of these filters directly to the FFE output cancels the NEXT impairment. Similarly, because of the bi-directional nature of the channel, an echo impairment results from each transmitter on its own receiver signal. Once again, using another adaptive filter with an output directly added to the FFE output nearly cancels this impairment.

The outputs of the FFE, echo canceller, and the three NEXT cancellers

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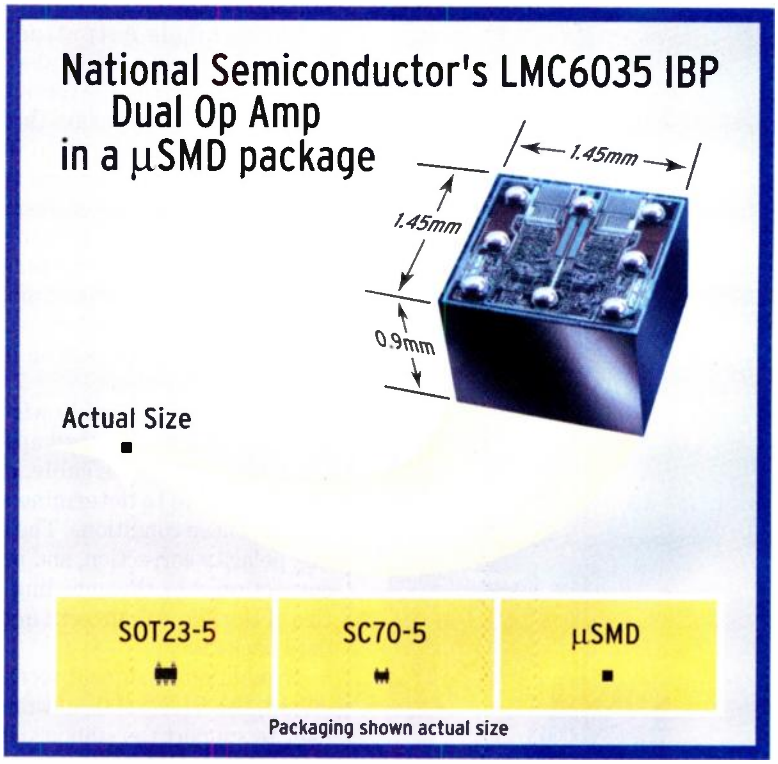

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combine with the output of an adaptive feedback filter in the Decision Feedback Sequence Estimation (DFSE) block to form a signal known as the soft decision. This signal is fed to a slicer output, which has the input of the adaptive feedback filter as its output. Using past decisions, this filter estimates postcursor inter-symbol interference caused by the channel for the current symbol. By subtracting it from the FFE + NEXT canceller + echo canceller, it forms the soft decision signal and does Viterbi decoding.

The symbols outputted by the Viterbi decoder or slicer are decoded and descrambled by the receive section of the PCS. Channel delays through the four pairs may vary by up to 50 ns (due to the variations in the way the pairs are twisted). Because of this, the PCS also is responsible for determining the relative skew of the four streams of 1D symbols, as well as adjusting their delay before the Viterbi decoder, so that the decoder can operate on properly composed 4D symbols.

To cope with possible wire swaps within a pair and pair swaps among the four pairs of the cable, the PCS should be able to determine and correct for these conditions. The deskewing, polarity correction, and pair-swap correction uses the encoding properties of the idle stream sent in between data packets.

In addition its signal-processing circuitry, the BCM5400 contains all the logic to support the standard interface and protocol requirements for the 802.3ab standard, including a full-function GMII. It can also interface directly to an older style, 10-bit serializer/deserializer (SERDES) physical-medium-attachment (PMA) host interface.

When the folks at Broadcom say it's a complete GMII-to-magnetics solution, they mean it. Many features have been incorporated to make it easy and inexpensive to design into a line card or networking device. For example, it's designed to simplify the line interface. Its on-chip wave shaping tailors the output signals' spectral content to keep crosstalk emissions within IEEE specifications—without the need for external passive components. The BCM5400 also has been designed to run off a 3.3-V supply, but can tolerate 5-V signal levels on many of its inputs.

Another added-value feature of the transceiver are its on-chip 1000Base-T hybrids, which permit it to connect directly to a simple magnetics module. This eliminates external passive components that add design time, board space, and production cost. Other "must-have" features include baseline wander correction and auto-negotiation. Baseline wander correction is essential because 1000Base-T signals are susceptible to dc drift if a long string of mostly ones or zeroes is sent. To prevent this, the BCM5400 contains baseline correction circuitry that keeps the signal's zero crossings centered around the middle of its range.

Auto-negotiation is a protocol that enables a transceiver to poll the device on the other end of the wire. It can then negotiate the type of connection and the fastest transmission speed they can both reliably support. Using its internal auto-negotiation logic, the BCM5400 senses and makes connections with both 1000Base-T Gigabit Ethernet and 100Base-Tx Fast Ethernet transceivers. In the 100Base-Tx mode, the transceiver transmits data on one Cat-5 wire pair, and receives it on another using a standard MLT3-encoded data stream.

Interesting Times Ahead

With a practical, cost-effective, copper-capable Gigabit interface now available, we may see a new interest in bringing these fat pipes to the desk. Until now, workstation and multimedia servers have been clamoring for more bandwidth from overloaded networks. For at least a little while, the ball is going to be in the computer, server, and switchmaker's courts as they try to figure out what to do with all that bandwidth. The next couple of years should be very interesting, indeed.

References:

1. *Author of "The New Colossus," written in 1883 and inscribed on the base of the Statue of Liberty in 1903.*

PRICE AND AVAILABILITY

The BCM5400 is housed in a 256-contact TBGA package. It's sampling before the end of this year, and will be in full production during the first half of 1999. Pricing is $59 each in quantities of 25,000 pieces.

For more information, contact Broadcom Corp., 16251 Laguna Canyon Rd., Irvine, CA 92618; (714) 450-8700; fax (714) 450-8710; www.broadcom.com. **CIRCLE 519**

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Next-generation digital communications designs are crying out for higher throughput, lower system cost, and the flexibility needed to handle changing multiple standards and features. But, these requirements far exceed the traditional uniscalar digital-signal processors' (DSPs) ability to meet them. To understand why, it helps to take a detailed look at the design objectives for these next-generation end systems.

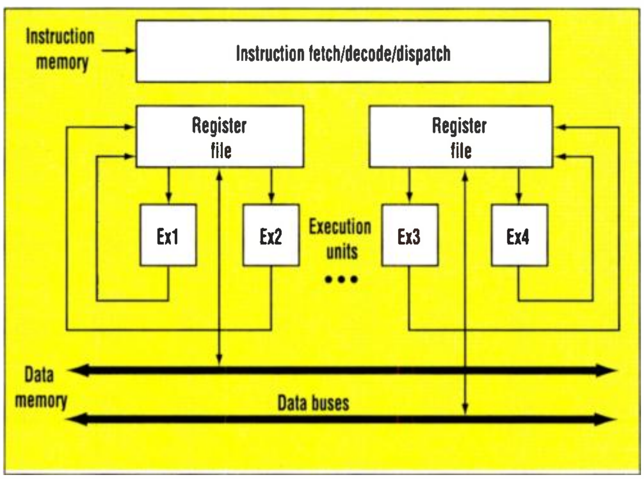
System cost: This factor, which has many components, is a universal objective of any OEM. The benchmark used to measure it is actually the "minimum cost per channel" required to implement the necessary DSP functions. Factors to take into consideration include the DSP devices, external memory, and support logic, as well as the cost of power supplies and cooling. In an effort to reduce system cost, DSPs must be able to perform multiple functions for multiple channels. This "multichannel processing" requires very high DSP throughput, but must not adversely affect the power dissipation and memory required to implement DSP functions.

Size and capacity: Infrastructure equipment is frequently limited by the size of an existing chassis or hardware footprint. The need for additional capacity and features, however, continues to rise. This impacts the system design in terms of DSP package size, number of channels per DSP, number of DSPs per board, support devices required, power, and thermal dissipation. All must be kept at a minimum.

Flexibility: Enter the dynamic world of digital communications. Features, standards, and requirements shift constantly. But, changes to the system should not require the customer—the service provider—to keep investing in new hardware. Thus, system designers must build hardware that can meet the current and future demands of communications systems—hardware that can be configured on-the-fly in the field or the factory. This impacts the DSP system by requiring programmable, RAM-based devices that have plenty of horsepower for new functions.

Development cost and time: Possibly the most difficult design objective to measure is the cost of developing a DSP system that includes both hardware and software components. The task of the DSP system may include speech coding, error correction, modem functions, and/or network functions. These must be implemented in software for execution on a programmable DSP. Even when a third party or the DSP vendor supplies some of the software, the OEM is usually responsible for any additional features, tying the software modules together for the particular system implementation, and for testing system performance. This is the most time-consuming development task for a multichannel DSP system. And, risk is directly related to the length of this task. Next-generation DSPs must address this time-to-market issue with advanced development tools and high-level-language (HLL) compatibility.

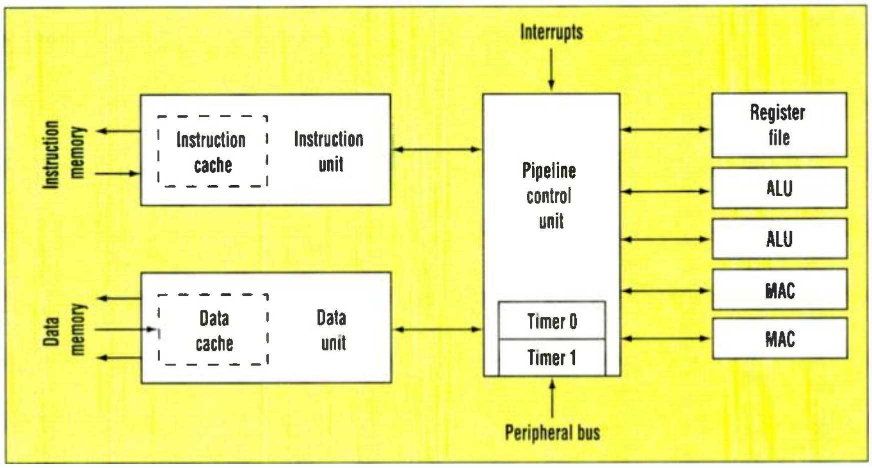
To summarize, it's the overall objective of the DSP system designer of digital communications systems to lower the cost per channel, increase the capacity, and retain or reduce the system's size and power dissipation. At the same time, the designer has to make it flexible to accommodate future needs and minimize development time and cost. These objectives drive the architecture design requirements of next-generation DSPs.



1. A simple view of a very-long-instruction-word processor shows the multiple execution units used to achieve highly parallel operation. The execution units are controlled in parallel by the wide words decoded from the instruction memory.

DSPs: Can They Hack It?

In the last year or two, several new, more efficient DSP architectures have appeared that borrow design techniques and architectures from the realm of high-performance microprocessors. These new designs employ aspects of superscalar microprocessors. Plus, they're reprogrammable, can handle multiple functions in less space, and deliver greater reliability for less cost and lower power than previous-generation solutions. But, they vary in the way they ad-



2. Multiple execution units, under the coordination of the pipeline control unit, form the heart of most RISC superscalar DSP processors. One such implementation is the ZSP16400 from ZSP.

dress system cost and development time. Examples of these next-generation DSPs include the RISC-superscalar (RISC-SS) and very-long-instruction-word (VLIW) architectures, each of which can deliver about 10 times the performance of many traditional DSPs.

To sustain a high throughput, which is a combination of architectural efficiency and processor speed, VLIW architectures employ multiple execution units that operate in parallel *(Fig. 1)*. Instructions that direct the action of each execution unit are combined together for execution in the same cycle, forming a "very-long instruction word." This is very similar to the way the old bit-slice microcoding was done.

Multiple execution units are not the only factor contributing to high throughput. This approach also must work at high speed. So, a long, visible pipeline is often employed. But, a long pipeline creates long latencies when a change of context is required, and a visible pipeline doesn't check for data or resource dependencies. These factors contribute to the difficulty in programming a VLIW machine. Further, the "very-long instruction words" executed every cycle adversely impact code density.

When VLIW techniques are applied to DSPs, the result can be a processor that's more "general purpose" than "special purpose." The VLIW machine is a load/store architecture with a register file. It contains execution units for both logic and math functions. These features contribute to this architecture's HLL-compiler efficiency. The efficiency of this compiler, as well as related develop-

LISTING 1

```
/*************************************************************/
/* unopt.c - Unmodified C source  for DOT product           */
/* 2033 cycles                                               */
/*************************************************************/
short mac(const short *a, const short *b, long *sum)
{
    short i;
    long dotp = *sum;

    for (i = 0; i < 150; i++)
    {
        dotp += b[i] * a[i];
    }

    *sum = dotp;
}

#include "data.h"

main(short argc, char *argv[])
{
    short c = 0x3;
    short output;

    c = mac(a, b, (long *) output);
}
```

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ment tools, is critical to the software development of any multiple-execution device, especially a VLIW machine.

Finally, to sustain the machine's maximum throughput, the VLIW implementation must move enough data per cycle that all the execution units remain busy. This requires wide buses and frequent memory accesses—both of which dissipate power and add cost.

Summing up the features associated with the typical VLIW processor, you end up with the following list:

- High speed coupled with parallel execution
- Good compiler efficiency
- Poor code density
- High power dissipation
- Difficult to program by hand
- High speed = long pipeline = long latencies
- Scalable

DSP circuits built with RISC-SS architectures also employ multiple execution units that operate in parallel to achieve high throughput *(Fig. 2)*. This contributes to a high code density for minimizing the system memory required, thereby decreasing power dissipation and cost. However, RISC-SS approaches utilize a fixed-length instruction word coupled with the scheduling performed in hardware. By removing the scheduling burden from the programmer or compiler, this makes the machine easy to program. The pipeline is hidden from the programmer and managed by hardware using a fixed set of "rules." If the pipeline is kept short, and some degree of caching and branch prediction is employed, latencies can be minimized.

Like VLIW approaches, the RISC-SS implementations use a load/store architecture with a register file that serves as source and destination for the execution units. As stated earlier, this is a major factor that contributes to HLL-compiler efficiency. The fea-

LISTING 2

```
/*************************************************************************/
/* optC.c - Modified C source for DOT product                           */
/* This is the Version modified to take advantage of the                */
/* ZSP16400 "C" Compiler                                                */
/* 602 cycles w/o full optimization                                     */
/* 170 cycles w/ full optimization enabled                              */
/*************************************************************************/
long L_mac2a(long, long, long);

q15 mac(const q15 *a, const q15 *b, long *sum)
{
        q15 i;
        accum_a dotp;

        dotp = *sum;
        for (i=0; i< 150; i+=2) {
           dotp = L_mac2a(dotp, * (long*) &(b[i]), * (long*) &(a[i]));
        }
        *sum = dotp;
}

#include "data.h"

main(q15 argc, char *argv[])
{
        q15 c = 0x3;
        q15 output;

        c = mac(a, b, (long *) output);
}
```

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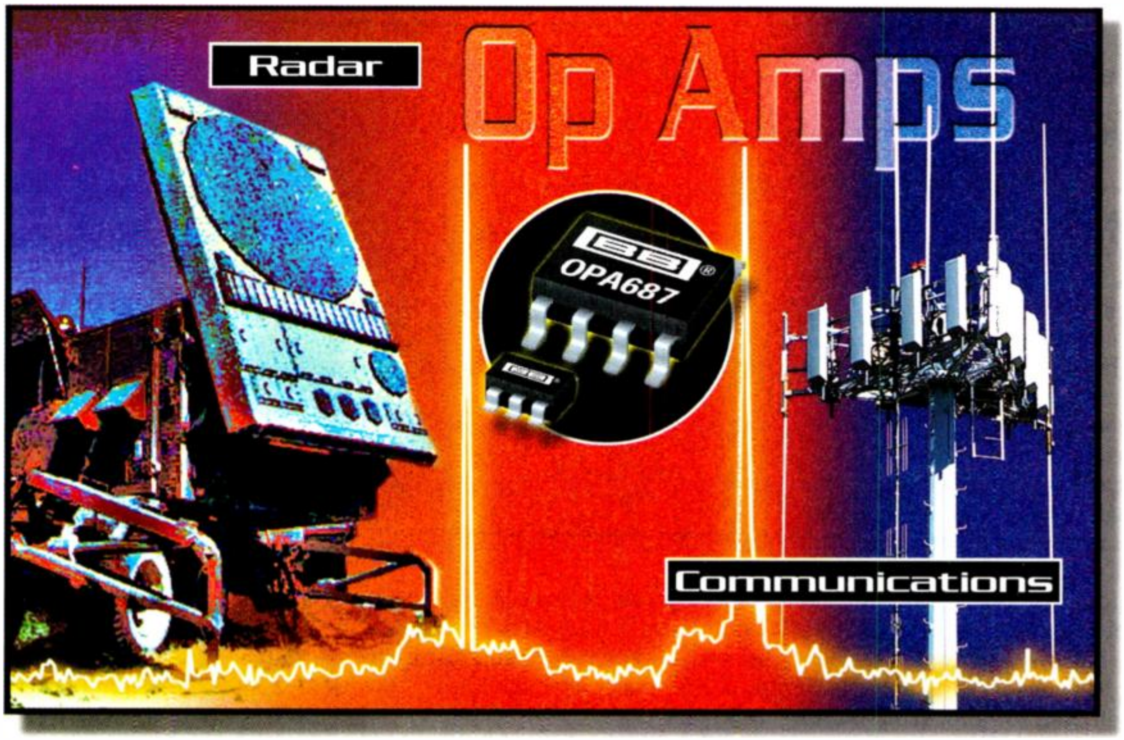

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- High speed coupled with parallel execution
- Good compiler efficiency
- Good code density
- Low power dissipation
- Easily programmed by hand
- Easily scaled or tailored to an application

DSP Software Challenges

When designing a system around one of the next-generation superscalar DSPs, many software-related issues must be addressed. Some of those issues include what to expect from a parallel processor, control-code efficiency, code density, and HLL-compiler efficiency.

Generally, a communications system is analyzed by a high-level simulation tool for performance and complexity. Frequently, the result of this simulation is a system model described either in part or entirely in C. Once the hardware and software partitioning has been done, a target DSP can be selected for executing major portions of the software.

To see how this all comes together, let's examine a DSP system design using a model of the DSP algorithm written in C code. The task will be to implement the algorithm represented in the HLL description as assembly code. This assembly code executes a multichannel, real-time communications function on the target superscalar DSP hardware.

Parallel Processing

Both VLIW and RISC-SS machines are parallel processors that employ multiple execution units which work in parallel in the same data path. This parallelism permits the processors to achieve a high throughput, often quoted in millions of instructions per second (MIPS). Not all tasks are parallel tasks, however, and scheduling independent tasks on a machine with a unified data path is close to impossible. The system designer must therefore evaluate the following aspects when considering DSPs based on VLIW or RISC-SS techniques:

- The "architectural efficiency" (defined as how well the DSP can execute a specific task) of these DSPs excels in tasks with a high degree of parallelism. A speech coder and many classical DSP tasks, such as filtering, have this quality.
- Conversely, the architectural efficiency of these DSPs will greatly diminish when executing a serial or control task. An example of a serial task is a convolutional encoder used for error correction, where a bit stream must be processed in time order. A typical control task is the parsing of control bits to determine the need for retransmission of a data packet.
- More hardware isn't always better. There's a point of diminishing returns in a parallel processor because not all tasks have a high degree of parallelism. In a digital communications system where there's a mix of signal processing, bit processing, and control functions, a maximum utilization of one or two operations per cycle can be expected. Additional execution units will not improve this efficiency if implemented in the same data path.

LISTING 3

```
/*************************************************************************/
/* dotp.s - Dot product hand-assembly code equivalent                   */
/* 95 cycles                                                            */
/*************************************************************************/
.segment "text"

        lda r13, a              /* pointer to vector a */
        lda r14, b              /* pointer to vector b */
        lda r15, c              /* pointer to result */

        mov %loop0, 74          /* loop count is N-1 */

lp_start:
        lddu r4, r13, 2         /* load a[i] and a[i+1] */
        lddu r6, r14, 2         /* load b[i] and b[i+1] */
        mac2.a r4, r6           /* a[i] * b[i] */
        agn0 lp_start

        st r1, r15              /* write sum to memory */
        halt
```

Control-Code Processing

Every DSP application is a mix of signal and control processing. The former is the classical "multiply/accumulate" repetitive task, which is block-oriented. Historically, it's within this type of task that DSPs are designed to excel. A control-processing task is decision-oriented—the typical "if-then-else" decision construct. Rough estimates say that the typical DSP system is 80% signal processing and 20% control processing. Thus, in a multichannel environment, the control processing portion increases above 20%.

Control processing typically degrades a DSP's throughput, since most DSPs aren't optimized to excel at control operations. These next-generation DSPs, with their roots in microprocessor architectures, have been tailored to handle multichannel systems. The DSP system designer, though, should concentrate on the several key aspects that follow when trying to decide which DSP implementation to apply to their system.

Interrupt structure: In a dynamic, multichannel environment, the DSP architecture must support a flexible, multilevel interrupt structure. This typically requires a minimum of three levels of interrupt nesting. The program control of the processor's interrupt level and support for the change of context also require attention.

Latency: Latencies occur in pipelined architectures when there's a change of program flow. Such latencies can happen because of interrupt handling, as well as the conditional branching frequently found in control code. Conditions in the machine that

are non-interruptible also will cause response delays. Features such as branch prediction, caching, and short pipelines can reduce latencies and improve performance.

I/O overhead: The processor's input/output overhead also can affect performance. This I/O overhead occurs when a change of context is required for the processor to service an I/O port (interrupt). It can be greatly reduced if the processor has and uses direct-memory-access (DMA) hardware support. The DMA hardware services the port without interrupting the processor, so the pipeline remains intact until the DMA transfer is complete. The DMA support must work in a non-cycle-stealing fashion and have no major restrictions. To service an I/O interrupt without the support of DMA, the maximum latency for entry and exit of an interrupt service routine must be understood.

Control-code efficiency: The efficiency of the control code can directly impact chip performance. Both the RISC-SS and VLIW DSP architectures have multiple arithmetic logic units (ALUs) that can operate in parallel, offering good control-code processing. To evaluate how efficiently the control code runs, a type of state-machine benchmark can be used to gauge the control-code processing efficiency. If the application requires bit manipulation like parsing data, a separate benchmark should be used to exercise the DSP's bit-banging ability.

Availability and fit of an RTOS: To ensure that the applications can run efficiently, another major factor that should be examined is the availability and fit of a real-time operating system (RTOS). With the increase in popularity of DSPs, a number of third-party vendors offer RTOSs for various target devices. In general, both DSP architectures are well suited to an RTOS due to their load/store architecture, high control-code processing efficiency, multilevel interrupt structure, and HLL support. In addition to checking with the DSP vendors as to the availability of an RTOS, designers should delve deeper to determine the software's feature set and overhead to the processor. Also, inquire whether the OS can be tailored to the specific application. Check the size of the kernel and key modules, and whether the modules can be added or removed easily (that allows the RTOS to be optimized for a particular application). Even a system manufacturer that plans to create its own "scheduler" for the DSP can probably learn something from the commercially available operating systems.

Dense Code Saves Memory

As mentioned earlier, minimizing the off-chip memory system helps lower system cost. Thus, the program code's efficiency and density become key to minimizing the memory footprint (the instruction memory space) required by the application code to implement a specific function. Superscalar devices have one common trait with respect to such a yardstick—they can trade code size for speed.

For example, both the RISC-SS

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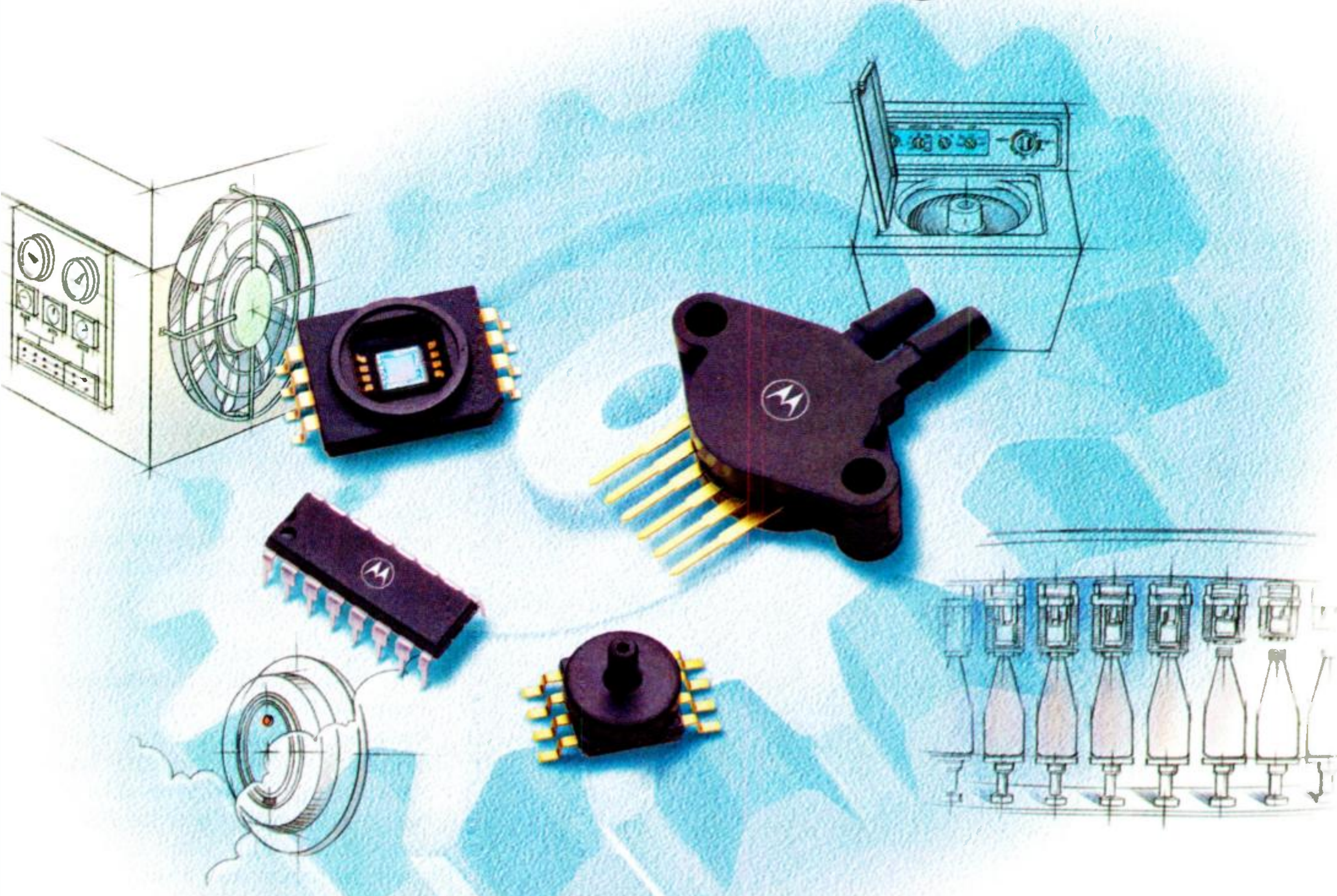

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and VLIW architectures can use a technique called "loop unrolling." In that scheme, the amount of code required will increase. But, all the delays associated with executing a loop will be eliminated, permitting the code to run faster. In loop unrolling, the loop construct is replaced with repetitive straight-line code, thereby avoiding pointer manipulation within the loop.

VLIW and RISC-SS processors offer users the ability to make this memory/speed trade-off in varying degrees. When assessing benchmarks from a DSP vendor, both the execution cycles and the program memory should be evaluated together. In general, a VLIW architecture will require more instruction memory than a RISC-SS for the same function.

HLL compilers also offer many benefits to designers who want to develop their applications using C or another high-level language. The most obvious benefit is a quick, easy port from a C model to assembly code. This can decrease the time-to-market, and gives the C-model code a high degree of portability. By changing compilers, the C code can be compiled into a different processor's assembly-code instruction set. That, in turn, makes it much easier to switch target DSPs without rewriting all the software. Also, code maintainability is much easier if the code is in C rather than in assembly code.

While porting a real-time application is easier with an efficient C compiler, however, it's unlikely that software development will end with compiled code. In a multichannel system, DSP throughput comes at a premium. Some level of hand optimization will typically be done, as well.

Compiler Friendly

Superscalar DSP architectures are compiler-friendly due to their load/store architecture, large register file, stack support, and other hardware resources. Proof of compiler efficiency—a function of both the DSP architecture and the compiler implementation—can be obtained by examining several C benchmarks. When evaluating C benchmarks for DSP devices, the original C source, assembly code, program size, and cycle count should be obtained for the identical algorithm. Also, factor in the changes to the C source required to obtain the benchmark results, since they could impact the code's portability. Ideally, the vendor's coding recommendations for optimal compiler performance should also be obtained.

One area of divergence between the VLIW and RISC-SS processors has to do with their assembly-programmer friendliness. VLIW offers the challenges of scheduling multiple tasks, varying instruction latencies, and a visible pipeline. RISC-SS performs the scheduling in hardware, so the programmer only needs to craft linear code that will be executed in order. A hidden pipeline in the RISC-SS architecture resolves the data and resource dependencies in the instruction sequence.

This generally makes the RISC-SS

machine easier to program at the assembly level. In addition, the compiler and debugger must be able to accommodate a mix of C and assembly code, as well as some hand coding.

Running The Algorithms

As a very simple example of an algorithm targeted for a next-generation processor, a vector-multiply routine illustrates the possible steps required to optimize the routine for implementation. The basic routine merely multiplies the corresponding elements of two vectors and accumulates the products so that one sum is output. That entire operation represents a single pass of a cross-correlation routine. The C compiler and DSP used to illustrate the RISC-SS compiler and architecture consists of the RISC-SS ZSP16400 DSP chip offered by ZSP and a generic, uniscalar processor model.

As previously stated, many DSP systems start as a high-level model. In this case, the sample algorithm is implemented as a C program *(Listing 1)*. The original source C code that performs the multiplication and accumulation of two vectors (one pass of a simple DOT product) compiles into an assembly-code block. To execute, this block requires 2033 cycles because the compiler could not take advantage of the DSP chip's resources.

This code is unmodified ANSI C, which can be compiled for execution on any target processor. The result is extremely inefficient DSP assembly code that takes no advantage of the fixed-point DSP target. That's because ANSI C has many features that make it incompatible with a fixed-point DSP architecture. For example, it has no fixed-point data type and no way to assign variables to specific registers. Thus, the compiler doesn't directly take advantage of the special features of the DSP hardware. And, it incurs a large overhead for function calls.

To better match the fixed-point DSP architecture to the HLL, the C code can be modified to produce more optimal DSP assembly code (assuming that the compiler can support such modifications). The C program can be modified to add an intrinsic function that maps the algorithm's multiply-accumulate (MAC) function to the DSP's dual-MAC instruction, making

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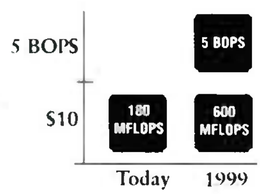

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more efficient use of the DSP's hardware (*Listing 2*).

Also, a fixed-point data type has been added (q15). It uses the upper 16 bits of a product and an accumulator data type to assign the results of the MAC function to a specific register pair. The resulting DSP assembly code shows almost a four-fold cycle reduction versus the C code in Listing 1. But, this code still doesn't take full advantage of the architectural features of the DSP hardware.

By having the compiler use two aspects of the processor chip's architecture, rather than modify the algorithm's code, a further optimization of the compilation can be achieved. For comparative purposes, Listing 3 shows a hand-coded DSP assembly program for the DOT product. This program requires just 95 cycles to execute when optimized for the ZSP16400 architecture. That's less than 1/20th the number of cycles required by the basic compilation, and would permit many more computations to be done in a fixed amount of time.

The first aspect of the compilation optimization uses the processor's low-overhead looping construct. The second, a feature called "link registers," utilizes a specific set of DSP registers as data pointers to prefetch data. The same C code used in Listing 2 will now compile and execute in less than twice the number of cycles as the hand-coded assembly of Listing 3.

This was a very simple example. More complex algorithms may require restructuring of the code for better optimization, including loop unrolling. The overall objective, however, is optimal compiler efficiency of execution time and memory usage, combined with maximum source portability. Selecting the best architectural approach can be done once all the pluses and minuses of RISC-SS and VLIW are understood. The guidelines outlined here should provide a good starting point. Still, each application is different—and those differences must be taken into account.

John Sweeney, currently a senior applications engineer for ZSP Corp., has more than 10 years of experience in fixed-point DSP applications. He received a BSEE degree from Villanova University, Villanova, Pa., in 1985.

DECEMBER

IEEE International Electron Devices Meeting (IEDM), Dec. 6-9. San Francisco, California. Contact Phyllis Mahoney, Widerkehr & Associates, 101 Lakeforest Boulevard, Suite 270, Gaithersburg, Maryland 20877; (301) 527-0900; fax (301) 527-0994; e-mail: pwmahoney@aol.com.

12th Systems Administration Conference (LISA '98), Dec. 6-11. Marriott Hotel, Boston, MA. Contact USENIX Conference Office, 22672 Lambert St., Suite 613, Lake Forest, CA 92630; (714) 588-8649; (714) 588-9706; e-mail: conference@usenix.org; www.usenix.org.

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IEEE/IAS Industrial & Commercial Power Systems Technical Conference (I&CPS), May 3-6. Nuggett Hotel, Sparks, NV. Contact Kerry Flannigan, Sierra-Nevada Power Co., P.O. Box 10100, Reno, NV 89520; (702) 689-4848; fax (702) 689-4139.

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International Symposium on VLSI Technology, Systems, & Applications, June 8-10. Taipei, Taiwan, R.O.C. Contact Tak H. Ning, IBM T.J. Watson Research Center, P.O. Box 218, Rt. 134 & Taconic Pkwy., Yorktown Heights, NY 10598; (914) 945-2579; fax (914) 945-3623; e-mail: ning@watson.ibm.com.

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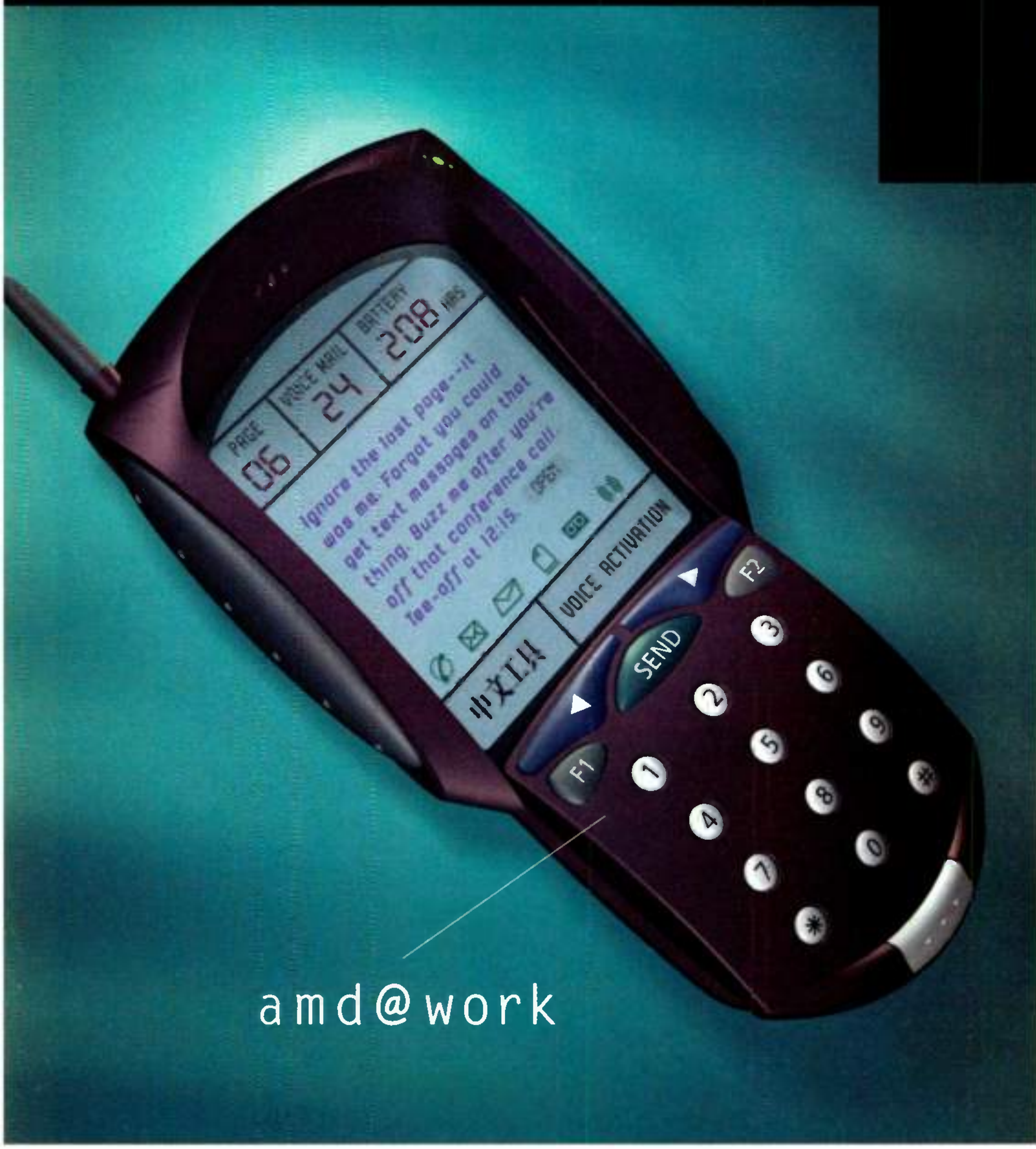

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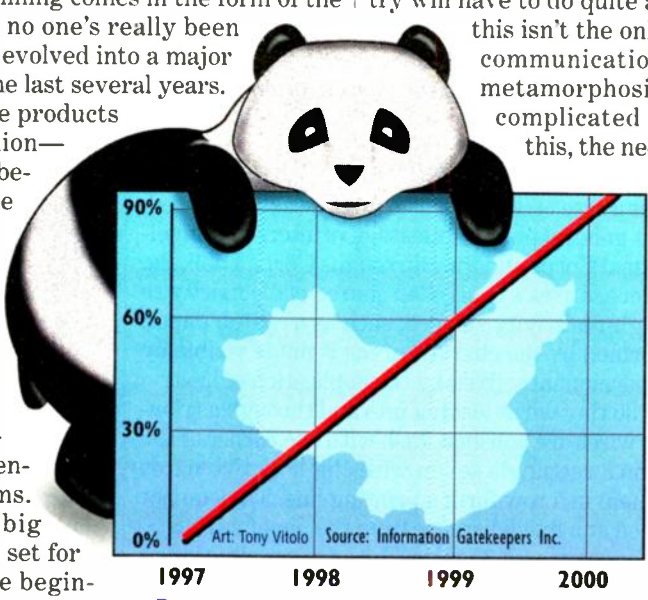
MARKET FACTS

Investors Bear Down On China's Software Industry

Sure, a lot of people are still talking and worrying about the current economic situation in Asia. Aside from the financial headaches, they wonder if it might slow down the growth and development of the electronics industry. The remedy that's often repeated is that if we would just put foreign money into the countries suffering this crisis, it would give them a chance to stabilize. But, people have been scared that they'll lose their money if they do that. As usual, there's a silver lining to every cloudy sky. In China, that lining comes in the form of the software industry. While no one's really been watching, this market has evolved into a major high-growth sector over the last several years. The total sales of software products in 1997 reached $1.35 billion—22% growth over the year before. At this point, Chinese software firms that have applications software as their main products take hold of about 30% of that total market. So, who's taking care of the rest of China's market? The other 70% is held by foreign companies that concentrate on operating systems. And, that's not all. The big news is that this market is set for growth. Going back to the beginning, growth gets investors hyped up and ready to spend. Professor Zhu Qiliang, director general of the R&D Center at Beijing University of Posts and Telecom (BUPT), has spent a great deal of time following this economy and forecasting statistics. During the 9th Five Year Plan period, which runs from 1996 to 2000, Professor Zhu's forecast says that China's software market will grow at over 30% annually. Total sales are expected to hit $3.5 billion in the year 2000. Professor Zhu points out that one of the characteristics of China's software industry is that it was developed without any large-scale investment directly from the Chinese government. None of the Chinese software companies are state owned. Of the country's software companies, 60% are collectively owned or operated as a joint stock company. The problem, according to Zhu, is that these companies cannot meet the rapidly increasing market demand or successfully compete with the foreign software developers if they continue to only accumulate investment funds by themselves. China's software industry suffers its largest hurdle in this lack of capital. To solve this problem, it's expected that China will absorb foreign venture investment. The country will have to do quite a juggling act, however, because this isn't the only market set to grow. The telecommunications network has been steadily metamorphosing into something much more complicated and sophisticated. Because of this, the need for telecom network management software is ever increasing. In an effort to meet this demand, BUPT developed a cellular network management system. With this system, the Ministry of Information Industry will construct a mobile network management center in Beijing, as well as 18 provincial network management centers. It's Professor Zhu's belief that this market also will see accelerated growth at a very high speed. How the country will handle this predicted growth remains uncertain. Already, the software industry has taken some interesting turns to cope with its gains. The software and hardware industries are converging. And, some profitable hardware suppliers in China have entered the software business in an effort to meet the increasing market demand for software applications. In any case, China's software industry is bearing fruit—and the pickings are ripe with profit potential.



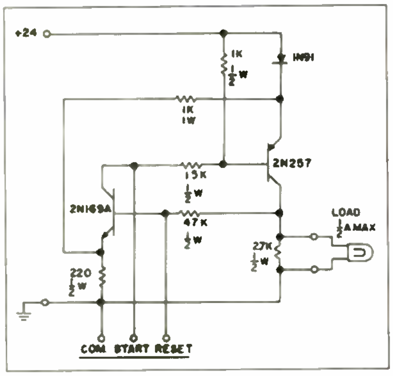
Forecasts predict that China's software market will grow over 30% annually, reaching $3.5 billion in the year 2000.

For more information on China's software industry, contact Information Gatekeepers Inc. at their web site: www.igigroup.com.—NK

40 YEARS AGO IN ELECTRONIC DESIGN

Reliable Annunciator Control Works From High-Resistance Lines

We needed an exceptionally reliable annunciator control which could be controlled through complex telephone circuitry. It had to require very little maintenance. The transistorized flip-flop shown did the trick. It is based on the pnp-npn "hook" circuit. It can be triggered and reset by control circuits with as much as 5000 ohms internal resistance and, unlike conventional flip-flops, it requires only about 20 ma of idle current. By changing the 1N91 diode to a larger one, one can control 2-amp lamp loads.



Here's how it works: In the non-operating state, both transistors are cut off by biases developed across the 1N91 diode and the 220 ohm resistor. Grounding the start lead switches on the 2N257, and the drop across the lamp load switches on the 2N169A. Upon release of the start circuit, the 2N169A collector current flows through the 1500 and 1000 ohm 2N257 base-drive divider. This locks the 2N257 on. Grounding the release lead cuts off the 2N169A. The current to the 2N257 is interrupted, after which both transistors are held off by their normal biases. Elbert S. Kennedy, Chief Electrical Engineer, Telecom Inc., 1019 Admiral Blvd., Kansas City, Mo. (Electronic Design, November 12, 1958, p. 166)

By late 1958, Ideas for Design was bringing in an increasing number of transistor circuits as semiconductors pervaded the industry.—Steve Scrupski

Teletypewriter Prints 3000 Words Per Minute

A teletypewiter which prints at a rate of 3000 words per min was announced. The device, reportedly the fastest general purpose message printer, was developed jointly by the U.S. Army Signal Corps and the Burroughs Corp., Paoli, Pa.

The electrostatic recording process uses a controlled source of electricity to form small charged areas on a high-resistivity surface, such as a coated paper. The electrostatic latent image formed by the charged areas is made visible by the application of powdered ink, permanently fixed by the application of heat.

The recording head comprises 35 tiny wires leading into and through a triangular-shaped piece of plastic. The wires are polished flush with one corner of the triangle, or printing head, to form a rectangle seven wires high by five wires wide. This is the matrix—72 of them in a row form a printing line. They do not touch the paper, but are maintained at a fixed distance from the paper surface.

Electric pulses will selectively charge all 35 wires, or any combination of those wires, in each head. A normal line of type, such as appears on this page, is made possible by setting up the first character in the line across all 72 heads. The only head that prints is the one selected by a coincident pulse to the back plate, or "anvil." The electrostatic charge can be deposited in one millionth of a second.

The second character in the word would be set up across the line and printed serially in a similar manner. Obviously, a line of 72 characters wide would require only a small fraction of a second. Operating at a lower speed of 750 words a minute to meet Army Signal Corps requirements, the new electronic messenger will be a major unit in the Army's new family of teletypewriter devices, all operating at 750 words a minute. (*Electronic Design, November 26, 1958, p. 8*)

Here's another step in the development of printer technology. It's an unusual item—a dot-matrix print head and what appears to be a xerographic method for fixing the image on the paper.—Steve Scrupski

Steve Scrupski is a former Editor-in-Chief of Electronic Design. Now semi-retired, he can be reached at scrupski@worldnet.att.net.

E-Mail By Phone

Wired workers who travel have probably all experienced this: You're in transit in the rental car, trying to find your way to an important meeting, and you know you've received important information via e-mail. But, you don't have time to pull over, get out the laptop, and log into it. Lucky for you, the e-mail-accessing wireless phone has become a reality.

TWS Inc., a developer and distributor of wireless telecom software, has joined with BellSouth New Zealand to upgrade its wireless e-mail product, called bulletIN. TWS now supplies BellSouth with the software necessary to let their customers get Internet e-mail over their mobile phones.

Version 2.0 of bulletIN will supposedly give the BellSouth New Zealand customers more access to e-mail from their mobile phones. According to TWS, the new version actually adds to the customers' ability to access their e-mail. The customers should now be able to both receive and reply to e-mail messages from the phones.

TWS isn't stopping here, however. With this version come plans for a future in which there are other forms of integration between the mobile phone and the Internet. Just imagine surfing the World Wide Web while you're stuck in traffic.

The BulletIN technology comprises a complete software package. By tying into a network operator's digital message center, it can forward information from the Internet or corporate LAN to a subscriber's wireless phone.

Aside from this convenience, the bulletIN version 2.0 offers upgraded e-mail messaging capabilities like enhanced billing and alarming. It also provides increased functionality for Internet access, which was the company's goal when upgrading the software.

For more information about bulletIN, contact Telecom Wireless Solutions, 6120 Windward Parkway, Suite 200, Alpharetta, GA 30005; (770) 752-7033; fax (770) 752-7136; www.tws-inc.com.—**NK**

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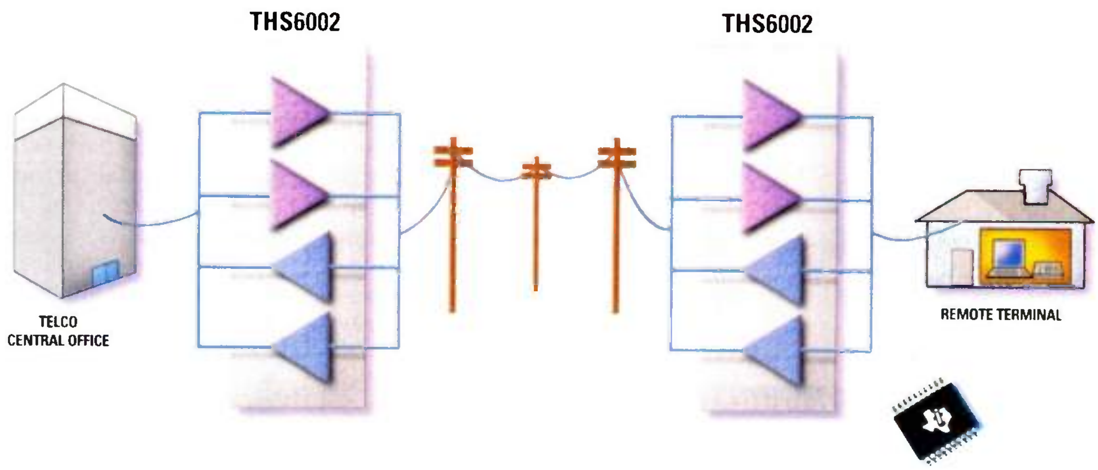

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High-speed xDSL Internet access technology requires drivers and receivers that transmit high data rates over low-impedance telephone lines with minimal distortion. The THS6002 from Texas Instruments is the answer. Its high 500-mA output drive and fast 1,000-V/µs slew rate combine to ensure ultralow THD under heavy loads. This integrated solution minimizes crosstalk by providing separate power supply connections to each amplifier. And because the THS6002 is packaged in TI's innovative surface-mount SOIC PowerPAD™ package, more heat can be dissipated in less PCB space than with heat sink or plug-type thermal packages.

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READER SERVICE 139

MANAGING THE DESIGN FACTORY

Testing: Annoyance Or Opportunity

Ogg, the Cro-Magnon development engineer, is at work again on a new ax design. Since few ax users want their stone axes to break during operation, the Bison Valley Ax Manufacturing Company has a pretty demanding life test procedure for new designs. Among other things, axes go through 50,000 "thump" cycles before they're qualified. The problem is that it takes a long time to get any new design through testing. Ogg has complained about this. But, his well-reasoned arguments are lost on Grnk, the Neanderthal test engineering manager.

Grinning, Grnk answers, "Well, Mr. Big Brain, come down and help us do the tests. That will speed it up!" Ogg tries this until his arms get tired and suggests, "You guys really need to automate the testing process." Grnk rolls his eyes up towards his sloping brow and says, in his eloquent Neanderthal way, "$%&#," which means, "Don't hold your breath until the next ice age!"

DON REINERTSEN

Even today, many companies view development testing as an annoyance. They argue that we only do development tests because development engineers make too many mistakes. Invoking the sacred gospel of total quality management (TQM), they assert that we should invest in preventing errors—not in finding and fixing them. But, does this really make sense?

TQM asserts that it's always cheaper to prevent errors than it is to find and fix them. In fact, finding and fixing errors is often cheaper than preventing them. Consider your word processor's spellchecker. How long would it take to perfect both your spelling and typing to the level where you can outspell the spellchecker? It's much cheaper and faster to use a spellchecker to correct spelling defects than it is to prevent them.

You see, this is a quantitative problem, not a question of philosophy. We should always inspect in quality if this is cheaper than preventing errors. Virtually all designs have some classes of errors that can be more efficiently found through testing than they can be avoided during design.

This is true when prevention would force us to use design margins that burden the product with excessive unit costs. It's true when system performance cannot be measured without a human operator "in the loop." It's also true when we get near the ragged edge of our engineering models. Thus, in the real world, we'll always have design defects that are best found through testing.

If this is the case, we need to recognize development testing as a value-added process and ask how we might improve it. We can start by recognizing that testing is a critical development competence—not a minor issue to be relegated to an under-resourced and poorly staffed test group.

Are you doing this? Take a simple test. Look at your own product and ask yourself how many hours it took you to test your product three years ago. How many hours does it take you today? Has there been any improvement? The average company has no quantified goals to improve their test department, nobody assigned to do this, no budget to do this with, and no plan for doing it. Is it surprising that its test process improves at a glacial rate?

In contrast, a handful of companies emphasize testing and achieve extraordinary improvements by doing so. I've seen organizations improve testing time and costs by factors of 20 to 30 times. For the smart developer, development testing is an opportunity—not an annoyance.

Don Reinertsen is a consultant specializing in product development management. He is coauthor of "Developing Products in Half the Time" and author of the new book, "Managing the Design Factory." Reinertsen & Associates, (310) 373-5332; e-mail: DonReinertsen@compuserve.com.

Free $ To Study Robots

Do you know an undergraduate student who's involved with robotics and is interested in a scholarship? The Robotic Industries Association (RIA), Ann Arbor, Mich., has announced that it will award three $1000 scholarships for robotics. The awards will be presented to winners at a special presentation during RIA's International Robots & Vision Show, taking place May 11-13, 1999, at the Cobo Center in Detroit, Mich.

Entry candidates are required to submit a paper that outlines a technical problem and offers a solution involving the use of robotics. The paper should explain how the robots will be used and why the problem is best solved by robotics versus hard automation or other manufacturing methods. The RIA is accepting individual or team entries.

"There are many students out there whose talents would be a great asset to the robotics industry," says Donald A. Vincent, RIA executive vice president. "By sponsoring this competition, we hope to stimulate their creativity and encourage them to put their ideas into practice," he adds.

Submitted papers must not exceed 20 double-spaced pages, including a one-page abstract and any charts, figures, or appendices. All undergraduates enrolled in a North American college or technical school are eligible to compete, regardless of the major they study.

Entrants must submit a competition participation form and the one-page abstract to the RIA by Dec. 11, 1998. Papers are due by Feb. 19, 1999. A panel of technical representatives from the RIA's member companies will judge the entries next March, and winners will then be notified in April.

For complete requirements and a scholarship participation form, contact Mary Lehtinen at (734) 994-6088. Or, visit the RIA's web site at www.robotics.org.

Roger Allan

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READER SERVICE 156

TECH INSIGHTS/QUICKLOOK

JUST 4 THE KIDS

Watch out, Barney and Big Bird lovers. A new rival is in town in the shape of a bright blue dog named Blue, and preschoolers love him. For those of you who don't know what I'm talking about, Blue is a character on Nickelodeon's "Blue's Clues" television show. In the show, Steve—Blue's owner—tries to figure out what Blue is thinking by putting together the three clues that Blue leaves for him. Children are encouraged to help Steve solve the mystery by yelling out the answers.

Those of you with preschoolers already know this. Just like in many other households, your child probably approaches you on a daily basis with a barrage of questions like: "When is Blues Clues going to be on? Is it time for Blues Clues yet? I want to see Blue!" Often, these questions are thrown at you in a high-pitched, whiny voice and accompanied by tears. Take heart. There may now be a solution to ease your pain. Best of all, it's just in time for Christmas.

The Washington-based Humongous Entertainment and New York-based Nickelodeon have teamed up to develop two separate CD-ROMs. They're taking the concept of the Blue's Clues television show and bringing it to the computer screen in Blue's Birthday Adventure and Blue's ABC Time Activities CD-ROM series.

These CD-ROMs, targeted at children ages three to six, feature Steve as the live-action host. He interacts with the child during the mission to decipher Blue's thoughts. Along the way, the child is able to touch, move, and interact with everything they see in Blue's world.

The first CD-ROM, Blue's Birthday Adventure, is a compilation of two discs. Each of these discs offers two distinct pathways which contain three clues. The discs may be played in any order, and it's never necessary to switch discs in the middle of a pathway.

Blue's Birthday Adventure builds on one of the most special days in a child's early life—his or her birthday. The child helps Steve plan Blue's birthday party by searching for clues. He or she meets a host of characters, including Baby Bear, Cash Register, Felt Friends, Magenta, Mailbox, Paprika, Mr. Salt and Mrs. Pepper, Shovel and Pail, Slippery Soap, and Tickety Tock.

MARIFRANCES WILLIAMS

The CD-ROM features four new Blue's Clues games, nine multilevel learning activities, and four creativity games. While searching for clues, the child can visit one of four different locations, or "skidoos," like the present store, the farm, storybook land, and birthday land. There's also games to play: find my friend, Tickety's puzzles, mixed-up music, and flower picking. Clues are found and recorded in the interactive handy dandy notebook. Adjustable difficulty levels keep the child challenged, while the user-friendly Help File assists with any questions.

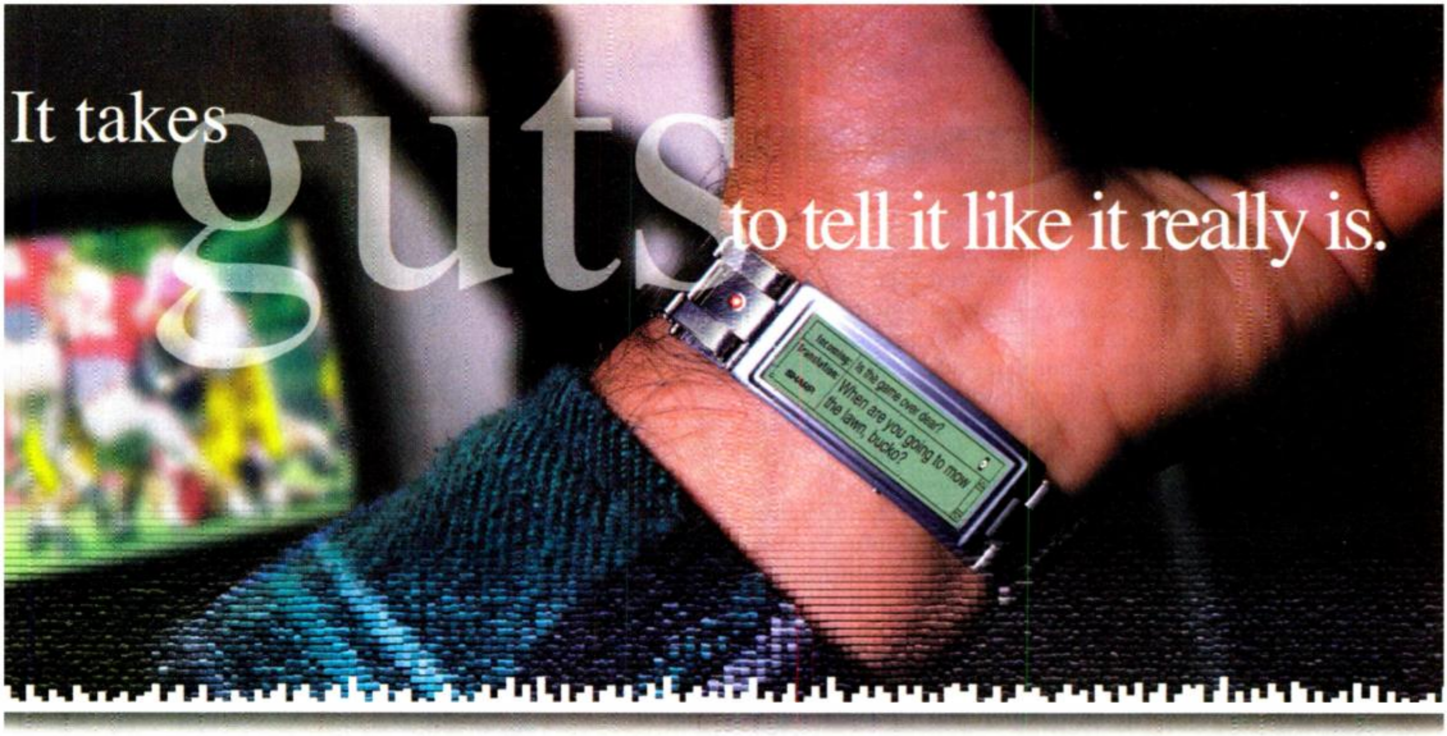
The second CD-ROM, Blue's ABC Time Activities, features seven multilevel learning activities that reinforce such pre-reading skills as letter recognition, phonics, and vocabulary. The child helps Blue create stories for the Word Book and interacts with a bunch of fun characters. Along the way, the child can play games. In alphabet maze, he or she follows the alphabet to reach Shovel and Pail. Helping Slippery Soap make rhymes is the point of bathtime rhymes. The child plays with shapes and words in Felt Friend's word puzzles, and helps Mailbox fill in the missing letters in messages. In safari snapshots, the child follows the Lion Prince on a jungle safari and helps Blue find animals and take photographs of them. With snacktime, the child aids Mr. Salt and Mrs. Pepper as they fix their torn shopping list.

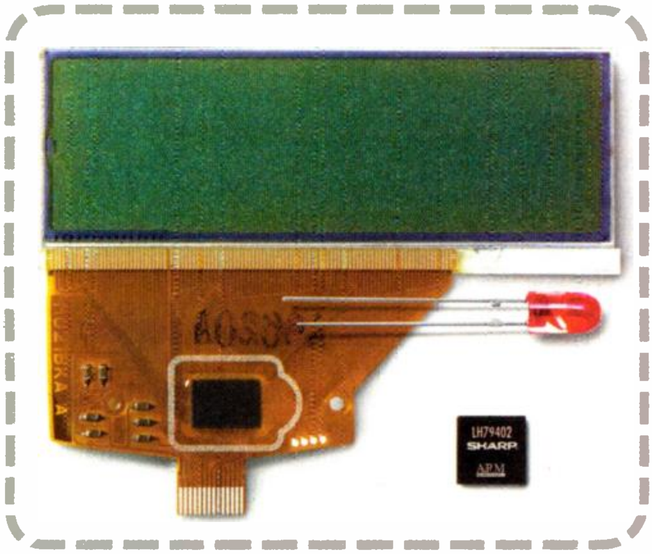
Upon completing each activity, the child earns a letter toward a word for Blue's Word Book. When an entire word has been collected, it can be used. The letters are color-coded to match specific pages in the book. For added emphasis and learning away from the computer, the Word Book may be printed blank for the child to write in his or her own words. Or, words may be collected and added to the book prior to printing.

The Blue's Birthday Adventure and Blue's ABC Time Activities CD-ROMs are now available at local retailers. They sell for $29.99 and $19.99, respectively. If your child enjoys these CD-ROMs, you might want to check out Pajama Sam 2, Thunder and Lightning Aren't So Frightening, Freddi Fish 3, The Case of the Stolen Conch Shell, and Big Thinkers Kindergarten and First Grade.

For more information, contact Humongous Entertainment, 13110 N.E. 177 Pl., Suite B101, Box 180, Woodinville, Washington 98072; (425) 486-9258; www.humongous.com.

Marifrances D. Williams holds a degree in Liberal Studies from San Diego State University, Calif. She is currently a fifth-grade teacher at Los Ranchos Elementary, San Luis Obispo, Calif. Williams specializes in the identification of advanced technology for the use of child-focused applications. She may be reached at williamsofsm@lightspeed.net.





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READER SERVICE 123

HEADS UP

You'd be surprised at what you can find at some off-the-beaten-path trade shows. I recently visited the POPAI Trade & Tech Expo in New York City, a small exhibition geared toward point-of-purchase advertising and merchandising personnel. What I saw there was the future in electronic signage.

For example, plasma-display panels (PDPs), those 40- to 50-in. flat-panel displays, abounded at this show. Why? Because vendors see them as forming a key part of an exciting new visual medium that will capture consumer eyeballs with advertisements. Wouldn't it be great, they argue, if all of those static cardboard, paper, and transparencies in light boxes could be made to come alive with moving images?

"In three years," says John Kirkpatrick, vice president of business and applications development at FRED Systems, Waterloo, Ontario, "I think we will see a boom in digital signage networks as significant as the Internet phenomenon. In five years, it will be a required part of any advertising and marketing mix." Heady stuff.

What he sees coming is a whole new advertising network that will rival traditional television, print, and radio outlets. Partly enabled by the rise of the Internet, advertisers already can create and distribute commercial messages to stores throughout the world. A credit card promotion, for instance, could appear simultaneously in stores like Sears, Citibank, or Burger King on a worldwide scale.

And, touch technology can make it interactive. Interactive Sales Systems, Peekskill, N.Y., offers a touch technology that doesn't place a screen over the PDP. Instead, they mount the entire PDP on a large plate strain gage that's a little bit bigger than a bathroom scale. Touching the panel in the upper right corner produces a torque that's detected in the strain gage. But, just pressing an inch or two further away produces a different strain.

Software maps the strains to positions on the screen. A user simply presses the screen and an interactive button is activated. Questa Corporation, Cambridge, Mass., showed a PDP with an active matrix LCD and full-function PC all integrated into one large, flat module. The LCD includes a more traditional touchscreen and acts as the interface for the PDP. Press a button and watch the big screen change.

One of the most compelling new visual environments is a moving video image that hovers in air. Using one or two video image sources, images can be made to "float" in air so that viewers can actually pass their hands right through them.


CHRIS CHINNOCK

Several companies have been working on this technology for a few years. The latest products are looking a lot better. For example, imedia, New York, N.Y., demonstrated a new prototype with a clear, floating video image that hovered about 15 inches in front of a smoked plastic sheet. The sheet works to conceal the optics. The prototype has a wide field of view, perhaps 70 degrees.

Dimensional Media, New York, N.Y., has a product with a less impressive packaging design. But, it does offer the capability to tie floating images to a company's web site. By modifying the HTML code to add metatags, specific pages can trigger local video loops that display as separate floating images on in-store kiosks.

Off the show floor, Airimages Unlimited showed me three models. The one that was most impressive was a device they call the cannon millennium projector. It produces curved, floating video images that improve the three dimensional feel of the imagery.

These floating images can even be superimposed over a second background image to create a 3D space between the two images. This type of display is definitely an attention getter for point-of-purchase, trade shows, or kiosk applications.

American Electric Glass, Columbus, Ohio, plans to bring back one of the original LCD technologies—dynamic scattering. While the technology doesn't have the high contrast of many other LCD implementations, it does produce a "frosted" image that can be made into many signage configurations.

The LCDs will be produced by sister company Blue Star Materials Development, Columbus, Ohio. One of it's main advantages, according to general manager Jeff Koster, is its low production cost. The company recently set up a new manufacturing facility that can produce displays up to 20 by 30 in., which Koster believes is the largest LC cell size available anywhere.

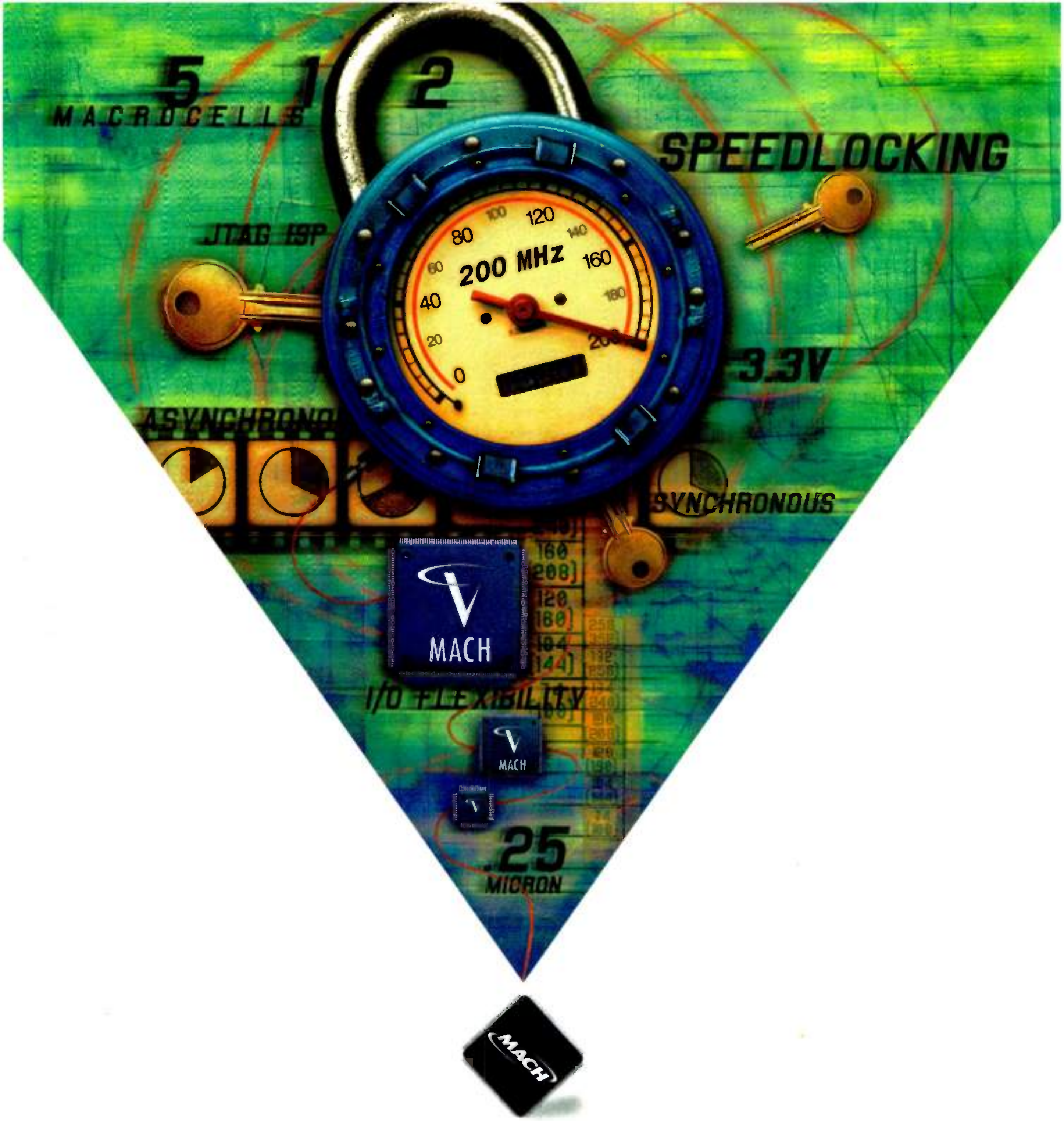
The company is also working on a new screen-printing technique for the transparent electrode materials used in almost all displays—indium tin oxide (ITO). If they're successful, expensive sputtering and photolithographic equipment could be eliminated from the manufacturing of some types of LCDs, potentially lowering costs.

Also up for the viewing were electroluminescent backlights that can be used to replace larger lamps. Visually interesting displays also can be created using rotating polarizers. Frank Woolley & Company, Reading, Pa., dubbed it "polarized animation."

The effects are impressive. When used with a light box, transparencies, and spinning polarization films, waterfalls look like they have moving water. Or, hydraulic plant schematics can show fluid motion.

All of these visual devices need no special viewing aids to see them. I guess you never can tell where you'll spot the next "signs" of a transformation.

Chris Chinnock holds a BSEE from the University of Colorado. He's the editor of the "Microdisplay Report," a newsletter covering all technologies for projection and virtual-based display systems (www.mdreport.com). Chris can be reached at (203) 849-8059; fax (203) 849-8069; or e-mail: chinnock@mdreport.com.



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A 42-in. Plasma Display—The Ultimate Fashion Statement

So, what do you get that special person in your life who has everything? How about trading in some of your stock options for a 42-in., plasma flat-panel television that costs $13,995? Photos of a romantic trip to the Mediterranean won't impress guests nearly as much as one of these babies planted smack in the middle of a $10,000 home-theater setup. While good audio also can impress, it has to be turned on to do so. The PlasmaWall PL-42 from Runco International just has to sit (or hang) there—all 86 lbs. of it. When turned on, the 3.5-in. thick display demonstrates the extraordinary depth of color of which this technology is now capable. The unit features 8-bit video processing—instead of the more common 4- or 6-bit systems—to deliver higher resolution, more saturated colors, and improved black levels and contrast ratios. Ideal for the soon-to-be available digital transmissions, the display has a 16:9 aspect ratio, a 160° off-axis viewing angle, and is currently compatible with NTSC, PAL, and SECAM formats. To cement its centerpiece appeal, the display comes with a backlit universal remote controller capable of commanding the audio-video functions of an entire home theater.

When the first 21-in. plasma displays were introduced to the mass market by Fujitsu about four years ago, the technology was most notable for its cost ($10,000) and its rather poor resolution (640 by 480). Further renditions over the next year or two raised the size of the display to 42 in. with similar resolution. But, with a cost in excess of $20,000, it was more a "proof of concept" than a marketable display. The PlasmaWall PL-42, while still on the expensive side, shows dramatic improvement in the technology with a resolution of 852 (RGB) by 480 at almost half the cost. Other key features include a lifespan of 30,000 hours, a contrast ratio of 120:1, a power consumption of 350 W, and built-in, 2-W stereo speakers.

For more information, contact Kevin Miller at Runco International, 2463 Tripaldi Way, Hayward, CA 94545; (510) 293-9154; fax (510) 293-0201.

Patrick Mannion

Jump Into Information Technology—It's Worth $2 Trillion

Fueled by the explosion of the Internet and intranets, everyone knows that information technology is big business. But, have you ever wondered what the numbers are? The first major study of global information technology spending and economic impact documents reveal an industry valued at almost $2 trillion and growing at a rate substantially faster than worldwide gross domestic product (GDP). In addition, the results suggest that the national GDP grows when information and communication technology (ICT) spending increases.

Even in the face of worsening economic conditions, the effect on ICT spending is muted. The World Information Technology and Services Alliance (WITSA) released dramatic findings last month at the Organization for Economic Cooperation and Development meeting in Ottawa, Ontario.

Called "Digital Planet: The Global Information Economy," the alliance's report provides a systematic exploration of the size and shape of the ICT marketplace around the globe. The study presents its findings based on data gathered in the 50 largest country markets (in GDP terms). In aggregate, this group represents 98% of worldwide ICT spending.

At $1.8 trillion, information technology is now one of the top industries worldwide. The forecast shows that the 'information economy' is not a vague abstraction, but a powerful economic force contributing 6% of aggregate global GDP to the world economy. To put that in perspective, that's nearly twice the size of California's gross domestic product.

According to the report, the U.S. spent $643 billion on ICT in 1997—twice as much as Japan at $317 billion. Together, the U.S. and Japan represent over 53% of the world marketplace. Other "top five spenders" are Germany, the United Kingdom, and France. Brazil is the leading spender in South America with $34 billion in 1997. The top five IT spenders in Asia and the Pacific Rim are Japan, Australia, the People's Republic of China, Korea, and Taiwan.

This boom also is revealed over the Internet. Over half the countries included in the survey have increased their representation on the World Wide Web by over 100% per annum between 1992 and 1997.

Published by WITSA, "Digital Planet: The Global Information Economy" is now available to the public for $500. Order it from the WITSA web site at www.itaa.org/digitalplanet.htm. An executive summary is available for free at www.witsa.org. Or, contact Bob Cohen of WITSA at (703) 284-5333; e-mail: bcohen@itaa.org.

Jeff Child

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- Prototypes in two weeks
- J.I.T. delivery

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M Series
Modouflex® Power Supplies

- 1,000,000 + Models
- 250 - 1500 Watts
- 1 - 7 Outputs
- AC and DC Inputs
- Competitive Prices

Deltron inc.
POWER PRODUCTS

SPECIFICATIONS

INPUT
90-132 VAC or 180-264 VAC, 47-63 Hz. Strappable. 40-60 VDC for DM Series.

EMISSIONS
FCC 20780 Part 15/EN 55022, Class A Conducted. EN 61000-3-3, Voltage Fluctuations.

IMMUNITY
IEC 1000-4-2/EN 61000-4-2, Electrostatic Discharge. IEC 1000-4-3/EN 61000-4-3, Radiated Field. IEC 1000-4-4/EN 61000-4-4, Electrical Fast Transients. IEC 1000-4-5/EN 61000-4-5, Level 3 Surge. IEC 1000-4-6/EN 61000-4-6, Conducted Field.

INPUT SURGE
34 amps peak from cold start for units under 400 watts, 68 amps for other models.

EFFICIENCY
75% typical.

HOLDUP TIME
20 milliseconds after loss of nominal AC power. 3 milliseconds for DM Series.

OUTPUTS
See model selection table. Outputs are trim adjustable ±5%.

OUTPUT POLARITY
All outputs are floating from chassis and each other and can be referenced to each other or ground as required.

LINE REGULATION
Less than ±0.1% or ±5mV for input changes from nominal to min. or max. rated values.

LOAD REGULATION
±0.2% or ±10mV for load changes from 50% to 0% or 100% of max. rated values.

MINIMUM LOAD
Main output requires a 10% minimum load for full output from auxiliaries. Use Option 08 if no minimum load is available for mains up to 500 watts. Singles require no minimum load.

RIPPLE & NOISE
1% or 100 mV, pk.-pk., 20 MHz bandwidth.

OPERATING TEMPERATURE
0-70°C. Derate 2.5%/°C above 50°C.

COOLING
A min. of 6 LFS* for models under 400 watts, 10 LFS for others, directed over the unit for full rating. Two test locations on chassis rated for max. temperature of 90°C. For convection ratings consult factory.
*Linear feet/second.

TEMPERATURE COEFFICIENT
±0.02%/°C.

DYNAMIC RESPONSE
Peak transient less than ±2% or ±200 mV for step load change from 75% to 50% or 100% max. ratings.

RECOVERY TIME
Recovery within 1%. Main output - 200 microseconds. Auxiliary outputs - 500 microseconds.

SAFETY
Units meet UL 1950, CSA 22.2 No. 950, EN 60 950, IEC 950.

ISOLATION
Conforms to safety agency standards.

INPUT UNDERVOLTAGE
Protects against damage for undervoltage operation.

SOFT START
Units have soft start feature to protect critical components.

OVERVOLTAGE PROTECTION
Standard on all outputs. VX Series - standard on main output.

REVERSE VOLTAGE PROTECTION
All outputs are protected up to load ratings.

OVERLOAD & SHORT CIRCUIT
Outputs protected by duty cycle current foldback circuit with automatic recovery. Standard auxiliaries have additional backup fuse protection. Options 04 and 16 have square current limiting with automatic recovery when overload is removed.

THERMAL SHUTDOWN
Circuit cuts off supply in case of local over temperature. Units reset automatically when temperature returns to normal.

FAN OUTPUT
Nominal 12 VDC @ 12 watts maximum.

INHIBIT
TTL compatible system inhibit provided. Option 16 has individual output inhibit.

REMOTE SENSING
On all outputs except standard and 04 Option outputs 75 watts or less.

SHOCK & VIBRATION
Shock per MIL-STD 810-E Method 516.4, Procedure I. Vibration per MIL-STD 810-E Method 514.4, Category 1, Procedure I.

MECHANICAL

CASE	WATTS	H	x	W	x	L	
1	250W/425W	2.50"	x	4.15"	x	8.00"	
2	400W/500W	2.50"	x	5.05"	x	9.00"	
3	600W/750W	2.50"	x	5.20"	x	9.63"	
4	600W/750W	2.50"	x	6.50"	x	9.63"	Config. 40 & 50 only.
5	600W/750W	2.50"	x	6.00"	x	9.63"	Option 32 only.
6	1000W	5.00"	x	5.05"	x	10.40"	
7	1500W	5.00"	x	5.20"	x	11.00"	

OPTIONS

POWER FAIL MONITOR
Optional circuit provides isolated TTL and VME/VXI compatible ACFAIL signal providing 4 milliseconds warning before main output drops by 5% after an input failure. A SYSRESET signal following VME timing requirements is provided when an N module is used as a main output. Both logic signal outputs can sink current per the VME specification.

AUTO RANGER
Optional circuit provides automatic operation at specified input ranges without strapping. Not applicable to DM Series.

CURRENT LIMIT
Option provides on all outputs:
- Square current limit with auto recovery.
- Wireless droop current share for parallel or N+1 redundant operation.

ZERO PRELOAD
Optional circuit removes need for preload on main output. Available for mains up to 500 watts.

ENHANCED
Option provides on all outputs:
- Square current limit with auto recovery.
- Single wire active current share for parallel or N+1 redundant operation.
- DC output good logic signal with LED indicator.
- Logic inhibit.
- Nominal 5V bias.
- Margining.

END FAN COVER
Optional cover with brushless DC ball bearing end fan which provides the required air flow for full rating.

TOP FAN COVER
Same as above with fan mounted on top of the power supply.

Specifications subject to change without notice.

Deltron inc.
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M ■ DM ■ VX SERIES MODUFLEX® SWITCHERS

DESCRIPTION

Moduflex® Series form a comprehensive line of open frame power supplies assembled from standard "off the shelf" modules. The design features "State of the Art" topology, a meticulous thermal structure and the use of high efficiency circuits and components to attain the desired power density. The modular system concept reduces manufacturing to submodule assembly, capable of high volume production with a superior quality level at moderate costs.

M Series are available in output power ratings from 250-750 watts. **DM Series** are available with a 48VDC input and output power ratings of 400 and 600 watts. **VX Series** units consist of four specialty units with output power ratings of 500, 750, 1000 and 1500 watts having the VXI standard voltages and currents.

Three classes of output modules are available. The **STANDARD** outputs allow short duration surge currents on all auxiliaries for hard starting loads. Optional **CURRENT LIMITED** outputs have square current limiting and feature wireless droop current sharing. Optional **ENHANCED** outputs have square current limiting, one wire star point current share, output good logic signal with LED, nominal 5V local bias, individual inhibit and margining. For requirements that cannot provide minimum load on the main output, the **ZERO PRELOAD** option is available for main outputs up to 500 watts.

DELIVERY

Choose stocked units or construct a model number using stocked modules for fast delivery. Otherwise, form a model from the adjacent page to meet your specific requirements. Contact factory for deliveries on models derived from non-stocked modules.

FEATURES

- UL, CSA, TÜV (IEC, EN), CE.
- 6 watts per cubic inch.
- 1-7 outputs, 250-1500 watts.
- AC & DC input models.
- VXI rated specialty models.
- 120 kilohertz MOSFET design.
- All outputs:
  - *Adjustable*
  - *Fully regulated*
  - *Floating*
  - *Overload and short circuit protected*
  - *Overvoltage protected*
- Standard features include:
  - *System inhibit*
  - *Load proportional DC fan output*
- Options include:
  - *Auto ranger*
  - *VME/VXI Monitor*
  - *End fan cover*
  - *Top fan cover*
  - *Current Limited Outputs*
  - *Enhanced Outputs*
  - *Zero Preload*
- Fast delivery.
- Replaces expensive high density systems using potted modules.

STOCKED MODELS - Available in 3 days.

Max Power	Output 1	Output 2	Output 3	Output 4	Model*
425W	5V @ 50A	12V @ 12A	5V @ 10A	12V @ 6A	M44R2323-47P
425W	5V @ 50A	24V @ 6A	12V @ 6A	12V @ 6A	M44R2633-47P
600W	5V @ 60A	12V @ 12A	12V @ 12A	5V @ 10A	M46C2332-47P
600W	5V @ 60A	12V @ 12A	24V @ 6A	12V @ 6A	M46C2363-47P

Models shown in table include power fail monitor, auto ranger, current limited modules, zero preload and end fan cover options. 600W models Case #3.

UNITS FROM STOCKED MODULES - Available in 2 weeks.

M 44 B 2 3 3 6 - YY X

- M — Series
- 44 — Configuration
- B — Power Code
- 2 — Output #1 Code
- 3 — Output #2 Code
- 3 — Output #3 Code
- 6 — Output #4 Code
- YY — Sum of Option Codes
- X — Output #1 Variant

Configuration: Allowable quad output configurations are 42, 44, 46 and 48.
Power Code: Choose Power Code P, R, A through D for 250-750W models.
Output Codes: Select any outputs from the shaded area on the Output Types table consistent with the configuration chosen.
Option Code: Specify Option Code. Refer to the Option table. Codes 02 (redundancy) and 16 (enhanced) are excluded from models available in 2 weeks.

OPTIONS

Option Code	Function
00	None
01	Power Fail Monitor
02	Auto Ranger
04	Current Limited
08	Zero Preload
16	Enhanced
32	End Fan Cover*
64	Top Fan Cover

*Replace the YY with the sum of the option codes. *600 & 750 watt units require Case 5.*

MODEL SELECTION

Models are available in power ratings of 250 to 1500 watts, with corresponding code letters P, R and A through D. See Power Code chart. Contact factory for 1000 and 1500 watt models.

Output modules are available in six types—J, K, L, M, N and P in nominal power outputs from 75-500 watts. Type M, N and P modules are variable power rated depending upon the unit power rating. The M, N and P Module table directly below shows the corresponding multiplier applicable to the output current ratings of the M modules and allowable power ratings for the N and P modules. For example, a 750 watt multiple will have its M type module configured to produce 120A @ 5V or 12A @ 48V. The voltage and current rating of output modules are listed in the table of output types. This table assigns an alpha-numeric code designating the nominal voltage rating of the module.

Power Code	Unit Power Rating	M Module Current Multipliers: Single Output	M Module Current Multipliers: Multiple Output	N/P Module* Allowable Power Ratings
P	250W	0.5	0.3	175W
R	425W	0.85	0.5	250W
A	400W	0.8	0.6	250W
B	500W	1.0	0.8	300W
C	600W	1.2	1.0	400W
D	750W	1.5	1.2	500W

When an N or P module is used as the main output, the allowable power and the module current ratings must not be exceeded.

Output Types*: Output Code	Output Volts	Module Type J Amps	K Amps	L Amps	M Amps	N/P Amps
0	2	10	20	30	100	60
1	3.3	10	20	30	100	60
2	5	10	20	30	100	60
3	12	6	12	24	42	42
4	15	5	10	20	33	33
5	18	4	8	16	28	28
6	24	3	6	12	21	21
7	28	2.5	5	10	18	18
8	36	2	4	8	14	14
9	48	1.5	3	6	10	10
A	2.2	10	20	30	100	60
B	2.4	10	20	30	100	60
C	2.7	10	20	30	100	60
D	3	10	20	30	100	60
E	3.6	10	20	30	100	60
F	4	10	20	30	100	60
G	4.5	10	20	30	100	60
H	5.7	10	20	30	90	60
J	6.3	10	20	30	80	60
K	7	9	18	30	70	60
L	8	8	16	30	62	60
M	9	8	15	30	56	56
N	10	7	14	30	50	50
P	11	7	13	27	45	45
Q	13.5	6	11	22	37	37
R	17	5	9	18	30	30
S	19	4	8	16	26	26
T	21	4	7	14	24	24
U	23	4	7	13	22	22
V	26	3	6	12	19	19
W	29	3	5	10	17	17
X	32	2	5	9	16	16
Y	40	2	4	8	13	13
Z	44	2	4	7	12	12

*Multiple output modules of a given type are arranged in ascending order by voltage magnitude in the same sense as the output number sequence in the configuration diagrams. *Shaded ratings are stock.*

HOW TO ORDER

To form the proper model number defining a custom requirement, select the letters M or DM to designate the series, then choose the desired configuration of output modules and list the configuration code. Insert the power code letter for the power level and follow with the output code numbers or letters for each specific output. Enter a dash and from the option table insert the sum of the option codes. Where lower power is desired for the main module, an N module can be substituted and is denoted by a letter N in the output variant position. In addition, when no preload is available for the main output, choose Option Code 08 and add a P in the output variant position. For an **enhanced** main and **current limited** auxiliaries, specify both 04 and 16 option codes.

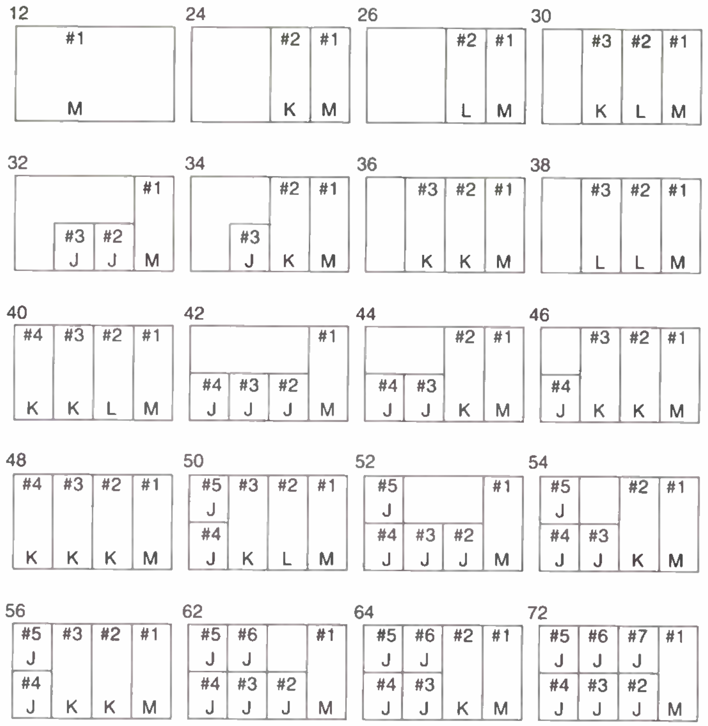
MODUFLEX 400W QUAD SWITCHER

D M 44 A 2 3 3 6 - YY X

- D — DC Input
- M — Series
- 44 — Configuration
- A — Power Code
- 2 — Output #1 Code
- 3 — Output #2 Code
- 3 — Output #3 Code
- 6 — Output #4 Code
- YY — Sum of Option Codes
- X — Output #1 Variant

OUTPUT CONFIGURATIONS

The boxes below are diagrammatic representations of the power supplies as viewed from the output end. The two-digit numbers above the boxes are the configuration codes.



Refer to the table below for allowable configurations by series.

Output Configuration	250W	400W	425W	500W	600W	750W
12	x	• x	x	x	• x	x
24	x	• x	x	x	• x	x
26					• x	x
30					• x	x
32	x	• x	x	x	• x	x
34	x	• x	x	x	• x	x
36		• x	x	x	• x	x
38					• x	x
40						x
42	x	• x	x	x	• x	x
44		• x	x	x	• x	x
46		• x		x	• x	x
48		• x			• x	x
50						x
52		• x	x	x	• x	x
54		• x		x	• x	x
56		• x			• x	x
62		• x		x	• x	x
64		• x			• x	x
72		• x			• x	x

• Represents allowable configurations for the DM Series.
x Represents allowable configurations for the M Series.

SPECIFICATIONS

INPUT
90-132 VAC or 180-264 VAC, 47-63 Hz. Strappable. 40-60 VDC for DM Series.

EMISSIONS
FCC 20780 Part 15/EN 55022, Class A Conducted. EN 61000-3-3, Voltage Fluctuations.

IMMUNITY
IEC 1000-4-2/EN 61000-4-2, Electrostatic Discharge. IEC 1000-4-3/EN 61000-4-3, Radiated Field. IEC 1000-4-4/EN 61000-4-4, Electrical Fast Transients. IEC 1000-4-5/EN 61000-4-5, Level 3 Surge. IEC 1000-4-6/EN 61000-4-6, Conducted Field.

INPUT SURGE
34 amps peak from cold start for units under 400 watts, 68 amps for other models.

EFFICIENCY
75% typical.

HOLDUP TIME
20 milliseconds after loss of nominal AC power. 3 milliseconds for DM Series.

OUTPUTS
See model selection table. Outputs are trim adjustable ±5%.

OUTPUT POLARITY
All outputs are floating from chassis and each other and can be referenced to each other or ground as required.

LINE REGULATION
Less than ±0.1% or ±5mV for input changes from nominal to min. or max. rated values.

LOAD REGULATION
±0.2% or ±10mV for load changes from 50% to 0% or 100% of max. rated values.

MINIMUM LOAD
Main output requires a 10% minimum load for full output from auxiliaries. Use Option 08 if no minimum load is available for auxiliaries. Singles require no minimum load.

RIPPLE & NOISE
1% or 100 mV, pk.-pk., 20 MHz bandwidth.

OPERATING TEMPERATURE
0-70°C. Derate 2.5%/°C above 50°C.

COOLING
A min. of 6 LFS* for models under 400 watts, 10 LFS for others, directed over the unit for full rating. Two test locations on chassis rated for max. temperature of 90°C. For convection ratings consult factory.
*Linear feet/second.

TEMPERATURE COEFFICIENT
±0.02%/°C.

DYNAMIC RESPONSE
Peak transient less than ±2% or ±200 mV for step load change from 75% to 50% or 100% max. ratings.

RECOVERY TIME
Recovery within 1%. Main output - 200 microseconds. Auxiliary outputs - 500 microseconds.

SAFETY
Units meet UL 1950, CSA 22.2 No. 950, EN 60 950, IEC 950.

ISOLATION
Conforms to safety agency standards.

INPUT UNDERVOLTAGE
Protects against damage for undervoltage operation.

SOFT START
Units have soft start feature to protect critical components.

OVERVOLTAGE PROTECTION
Standard on all outputs. VX Series - standard on main output.

REVERSE VOLTAGE PROTECTION
All outputs are protected up to load ratings.

OVERLOAD & SHORT CIRCUIT
Outputs protected by duty cycle current foldback circuit with automatic recovery. Standard auxiliaries have additional backup fuse protection. Options 04 and 16 have square current limiting with automatic recovery when overload is removed.

THERMAL SHUTDOWN
Circuit cuts off supply in case of local over temperature. Units reset automatically when temperature returns to normal.

FAN OUTPUT
Nominal 12 VDC @ 12 watts maximum.

INHIBIT
TTL compatible system inhibit provided. Option 16 has individual output inhibit.

REMOTE SENSING
On all outputs except standard and 04 Option outputs 75 watts or less.

SHOCK & VIBRATION
Shock per MIL-STD 810-E Method 516.4, Procedure I. Vibration per MIL-STD 810-E Method 514.4, Category 1, Procedure I.

MECHANICAL

CASE	WATTS	H	x	W	x	L	
1	250W/425W	2.50"	x	4.15"	x	8.00"	
2	400W/500W	2.50"	x	5.05"	x	9.00"	
3	600W/750W	2.50"	x	5.20"	x	9.63"	
4	600W/750W	2.50"	x	6.50"	x	9.63"	Config. 40 & 50 only.
5	600W/750W	2.50"	x	6.00"	x	9.63"	Option 32 only.
6	1000W	5.00"	x	5.05"	x	10.40"	
7	1500W	5.00"	x	5.20"	x	11.00"	

OPTIONS

POWER FAIL MONITOR
Optional circuit provides isolated TTL and VME/VXI compatible ACFAIL signal providing 4 milliseconds warning before main output drops by 5% after an input failure. A SYSRESET signal following VME timing requirements is provided when an N module is used as a main output. Both logic signal outputs can sink current per the VME specification.

AUTO RANGER
Optional circuit provides automatic operation at specified input ranges without strapping. Not applicable to DM Series.

CURRENT LIMIT
Option provides on all outputs:
- Square current limit with auto recovery.
- Wireless droop current share for parallel or N+1 redundant operation.

ZERO PRELOAD
Optional circuit removes need for preload on main output. Available for mains up to 500 watts.

ENHANCED
Option provides on all outputs:
- Square current limit with auto recovery.
- Single wire active current share for parallel or N+1 redundant operation.
- DC output good logic signal with LED indicator.
- Logic inhibit.
- Nominal 5V bias.
- Margining.

END FAN COVER
Optional cover with brushless DC ball bearing end fan which provides the required air flow for full rating.

TOP FAN COVER
Same as above with fan mounted on top of the power supply.

Specifications subject to change without notice.

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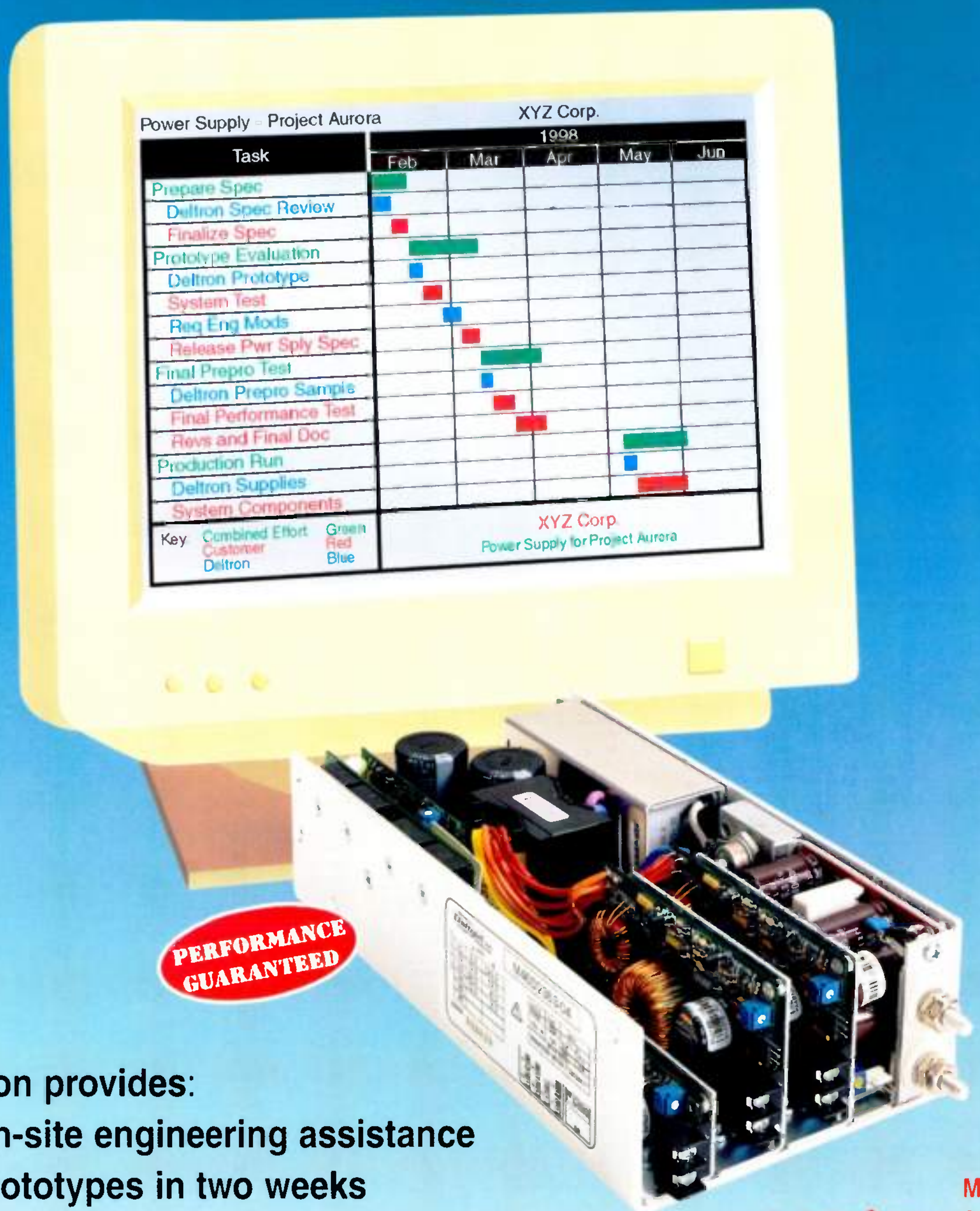

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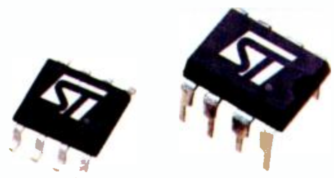

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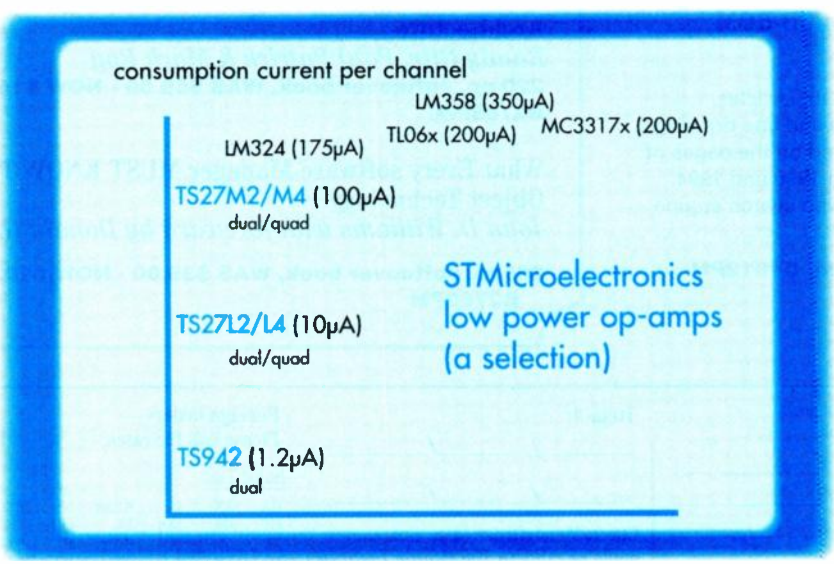

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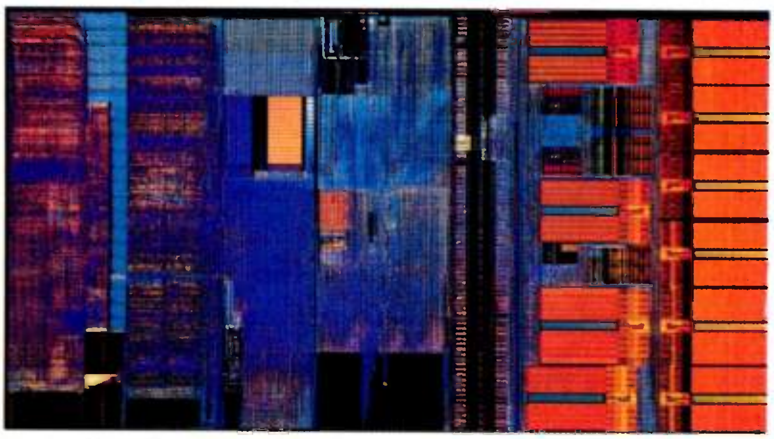
Advanced Processes And Architectures Boost x86 CPU Performance Levels

Pushing Clock Speeds To 500 MHz And Beyond, x86 Processors Can Now Deliver Supercomputing Performance On The Desktop.

Dave Bursky

SPECIAL REPORT

Designers face a veritable triathlon challenge when bringing an x86 processor to market: They must craft a chip that delivers the highest performance at the lowest cost, and with 100% compatibility with the existing base of operating-system and application software. The standard set by the Intel x86, Pentium, Pentium II, Celeron, and now Xeon (formerly code-named Deschutes) processors has become the target that other manufacturers must meet and surpass to garner attention from system manufacturers. Competitive offerings must be faster and cheaper, yet still meet the system and software compatibility requirements. At the same time, designers at Intel must remain nimble, continually crafting higher-performance CPUs that set new standards. The result of this competition has been the availability of CPU chips and systems that can deliver the computing power close to that of supercomputers.



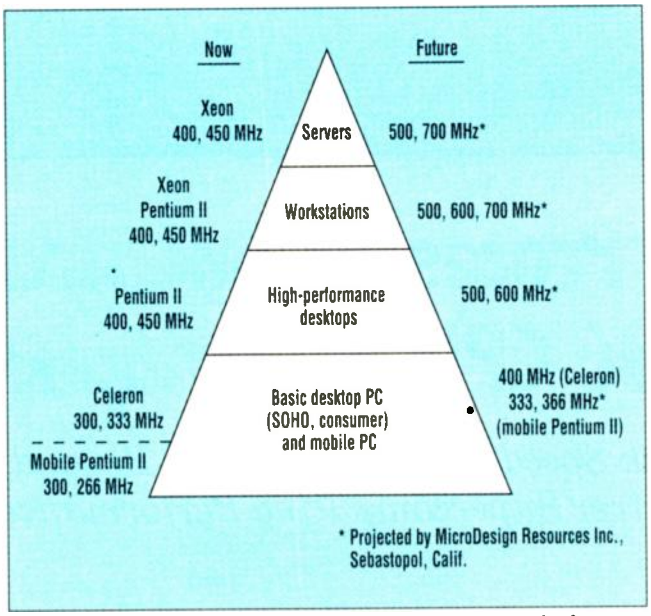
Art Courtesy: Advanced Micro Devices

PC manufacturers have divided the industry into four basic configurations, each with its own CPU requirements *(Fig. 1)*. As a result, CPU manufacturers can no longer just offer a single CPU and try to shoehorn it into multiple product classes. Rather, they must create multiple versions of their CPUs, each targeted at different classes of systems, just as Intel has done for its IA-32 architecture.

At the highest end of the performance spectrum are the server and workstation-class system ranks, which demand the highest performance from the CPUs and are willing to deal with the high power-consumption demands of from one to four or more CPUs in a single system. Such systems demand CPUs capable of four-way or even N-way multiprocessing and the system logic that can support multiple CPUs. Of course, beyond the Xeon class processor for servers, Intel is working hard on the Merced processor, which it expects to sample late 1999. Intel does not expect that CPU to be used in workstations or PC-class systems at the outset.

At last-month's Microprocessor Forum conference held by MicroDesign Resources, Sebastopol, Calif., Intel divulged several additional members to both its forthcoming IA-64 and the current IA-32 families. At the high end, the company unveiled new code names for higher-performance processors beyond the Merced, the first of which is McKinley, which will add an on-chip L2 cache and some enhancements to the microarchitecture. After McKinley, the company will split the IA-64 into two paths: one will focus on high performance with a part dubbed Madison, and the other will focus on lower-cost options with a device called Deerfield, which will target workstation platforms. In the IA-32 realm, following the Xeon processor is Tanner, which will implement the Katmai instruction set enhancements and then processors dubbed Cascades and Foster. The Cascades processor will add an on-chip level 2 cache, while Foster will sport an enhanced microarchitecture for higher performance.

Next down the slope are the high-performance "business" desktops that are typically uniprocessor (sometimes dual-processor) systems and provide top-of-the-line performance for typical business applications. Sort of in parallel with the business desktops, the business-class laptop/portable computers must now keep pace with desktop performance, delivering with a single CPU some top-notch software performance at much-reduced power levels. Lowest in the ranking are the no-frills "consumer"/gaming PCs and some budget-priced laptops—low-cost systems that include a single CPU with enough horsepower to run 3D games while, at the same time, providing more than adequate performance for most typical business applications. And, just emerging in the same rank is talk of a "value" low-cost portable computer platform that targets the consumer and will sell for about half the price of today's typical laptops.



1. In the PC world, the market is roughly partitioned into the four tiers as shown in this pyramid. Each tier has its own performance and cost requirements that demand theuse of a different CPU to meet perceived performance needs. This is shown by the "mapping" of various Intel CPUs to different tiers.

To meet the wide range of system requirements, there has been and will continue to be a veritable explosion of CPU variations. These variants will provide a wide range of system interfaces, speed grades, integrated primary and secondary caches, graphics support in either hardware or software, and multimedia support for imaging and audio. Thus far, manufacturers such as Advanced Micro Devices, Cyrix/National Semiconductor (and IBM), Centaur/Integrated Device Technology, Intel, and most recently, newcomer Rise Technology, have been able to meet that challenge.

They have done it through a combination of high levels of integration (larger caches), novel architectural enhancements and implementations, lower power-supply voltages, and aggressive use of multilevel metallization and deep-submicron lithography to keep chip size and power consumption as small as possible.

Such a wide variety of chip options gives system designers much flexibility in selecting the optimal device to meet cost and performance goals. In addition, the competitive nature of the system market has made its way to CPUs. Thus, as new low-cost and high-performance CPU implementations arise, new market opportunities also open—Windows terminals, Internet appliances, and others—to give even previous-generation processors (with clock speeds below about 200 MHz) a new lease on life.

Many of the chips that compete with Intel's processors are no longer drop-in replacements. Intel has moved away from the single-chip "Socket 7" package used by its Pentium series. All the latest Intel Pentium II CPUs now come in the form of a single-edge cartridge module that not only includes the CPU, but the tightly coupled secondary cache, a clock-timing generator, and special thermal arrangements that allow the module to dissipate close to 28 W. For the Pentium II modules, the cartridge bus interface is referred to as Slot 1, while for the new Xeon processor modules, which include an enhanced interface that supports four-way and more-complex multiprocessor systems, the bus interface is referred to as the Slot 2 interface. Xeon modules also consume a bit more power—about 38 W for a 400-MHz module with a 1-Mbyte cache.

Both the Slot 1 and Slot 2 processor electrical interfaces employ what Intel calls assisted Gunning transistor logic (GTL+), which the company feels provides the best signaling option for its high-speed processor buses. The popular Socket 7 interface used with most PGAs, though, employs a more LVTTL-like signal swing and may not be able to offer interface speeds much beyond the 100 MHz of the Super7 (an enhanced Socket 7 interface).

However, a new standard, dubbed Socket 370, seems to have caught on at

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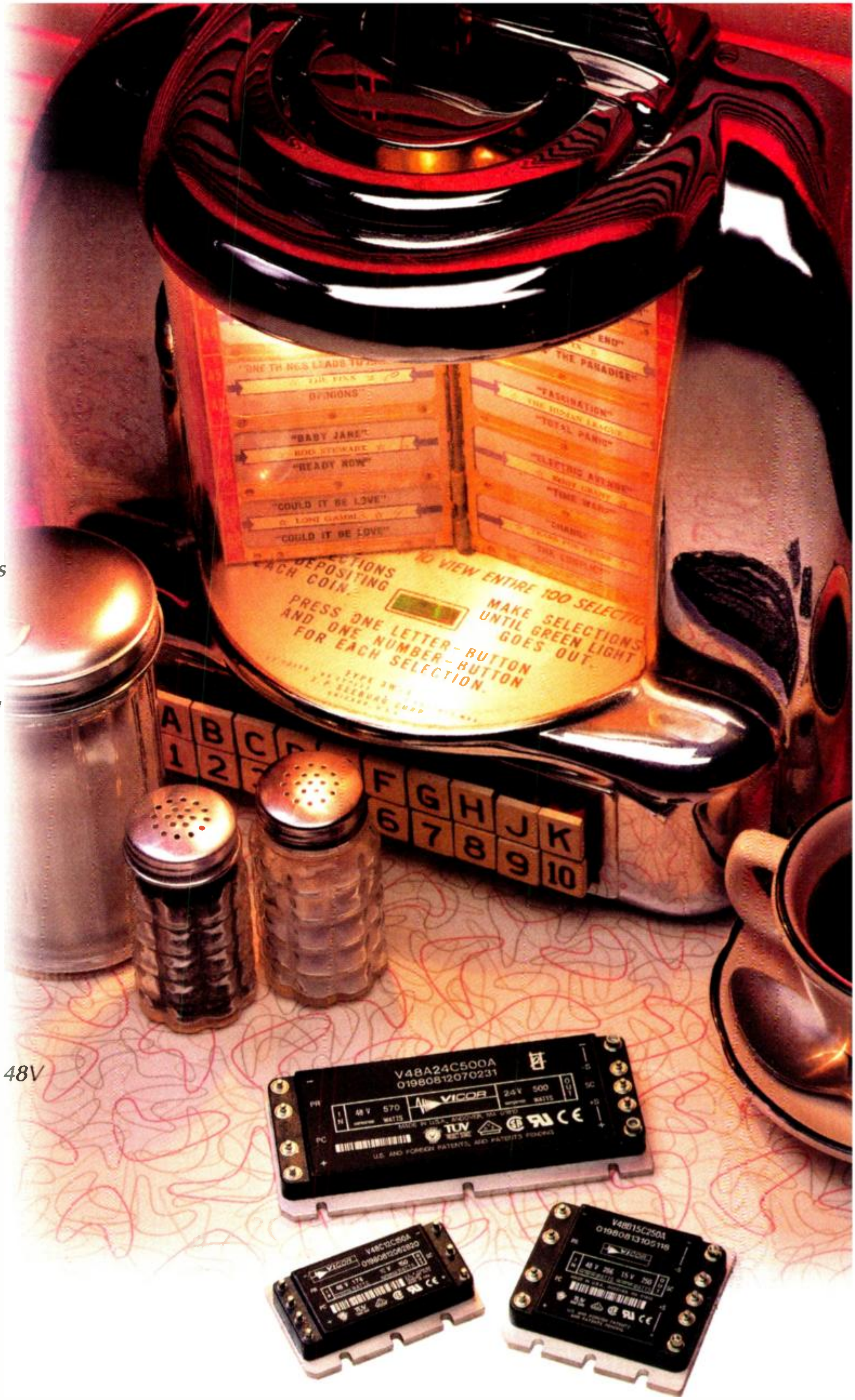

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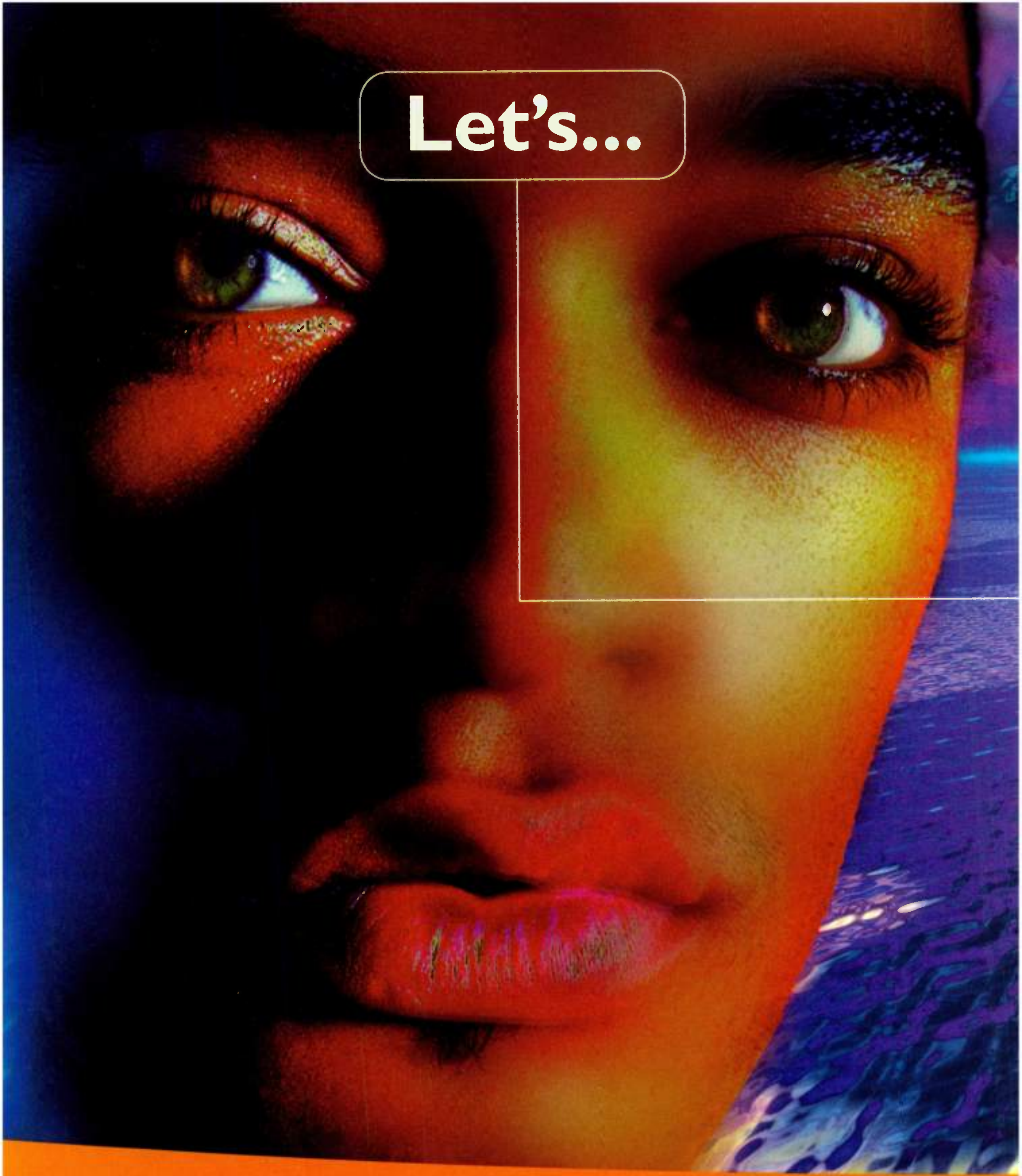

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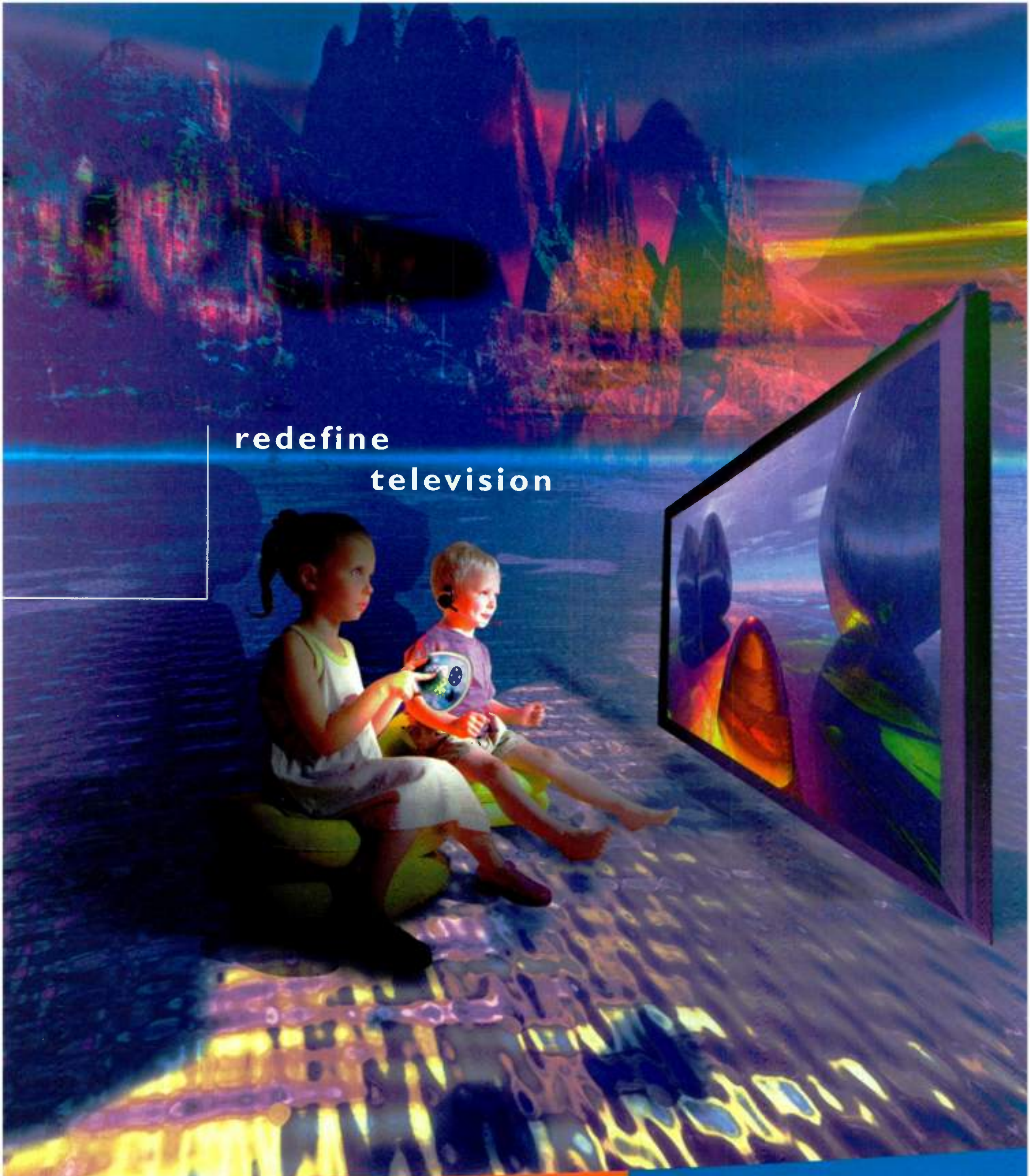

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many system vendors now that Intel is expected to re-adopt the PGA package for its Mendocino and future versions of the Celeron processor. The Socket 370 interface will (physically) be the socket to hold a PGA-housed CPU, but the signal set and electrical interface will have the signaling characteristics of a Slot 1 interface. Implemented with GTL+ signaling, the Socket 370 interface will provide a lower-noise and higher-speed interface than possible with the Super7 standard.

Patent Options

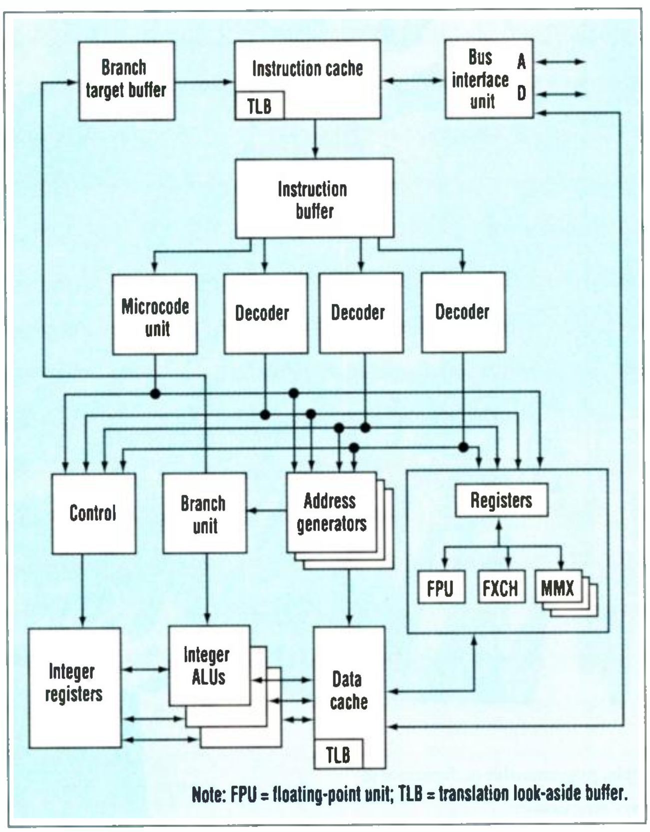
Intel currently holds patents on the signaling used in the Slot 1 and Slot 2 interfaces, and tightly controls the intellectual property, requiring that companies license that interface to implement motherboard chip sets. To avoid the licensing restrictions or expense, other CPU vendors have opted to try and extend the Pentium CPU socket interface, typically referred to as the Socket 7 interface. There is already an extension referred to as the Super 7 interface, which includes 100-MHz main memory and cache interfaces, and much work is going on at AMD to create a higher-performance interface for its forthcoming K7 processor. That interface will be based on a bus developed for the Alpha processor licensed by AMD from Digital Equipment Corp., Hudson, Mass.

Known as the EV 6 bus, this interface will allow independent address and data transfers at 200 MHz and permit designers to easily implement multiway-processor systems. To achieve the high performance, the bus actually employs two unidirectional address buses and a bidirectional data bus. A clock-forwarding scheme is used in which the clock is sent along with the data, thus keeping the data in sync with the clock and permitting the high-speed transfers on low-cost motherboards that don't require many layers of routing and ground planes.

Intel's designers, though, are still setting the pace. They've upped the ante for the different processor levels with the introduction of the 7.5-million-transistor version of the Xeon Pentium II processor for workstations and servers, and 400- and 450-MHz speed grades of the Pentium II for mid-range platforms. For consumer and portable systems, the company released the Mendocino processor upgrade (also known as Celeron-A) to the Celeron, which packs roughly 19-million transistors due to the addition of an on-chip 128 kbyte level-2 cache. The cache improves the performance of Celeron-based systems and reduces component count for cost-sensitive platforms and limited-board-space portable systems. Also available are special low-profile packaging options for the Celeron and Pentium II CPUs that ease their use in portable systems.

Rise Technology, a newcomer to the PC CPU market, has developed a processor it feels is superior in performance to Intel's Celeron/Mendocino processors. Rise's MP6 family includes two versions of the basic CPU, both of which are designed for low-power consumption. One of the target markets Rise would like to serve is notebook computers and other portable systems. The MP6 processor packs a level-1 cache of 16 kbytes, and the 100-MHz Super7 bus interface. This chip is targeted at systems that can provide an external level-2 cache or run without a level-2 cache. The more aggressive device is the MP6-II CPU, which adds a 256-kbyte level-2 cache to the chip—double the size of the level-2 cache available on Intel's Mendocino CPU.

To get higher performance than what the Celeron offers, Rise's designers took several approaches. First, they crafted a highly parallel superscalar and superpipelined architecture and a superpipelined floating-point unit to greatly speed up graphics and other multimedia applications *(Fig. 2)*. The three-way superscalar approach and native execution of x86 instructions (rather than the atomic-RISC execution approach used by AMD and Cyrix/National Semiconductor) allows the MP6 to deliver high instruction throughputs. The MP6-II's large on-chip cache also will reduce external memory fetches and further speed instruction throughput.



2. A three-way superscalar and superpipelined architecture is employed in Rise Technology's MP6 processor. The processor executes native x86 instructions (including MMX commands). It has better performance than Intel's Celeron and Pentium with MMX when running at an equivalent clock speed.

The Horn Of Plenty

Intel, though, has a cornucopia of enhancements still to come—faster and enhanced versions of the Celeron, Pentium II and Xeon processors with clock speeds for some of the CPUs hitting 500 MHz and higher in early 1999. Additionally, the forthcoming Katmai processor, targeted at workstation-class systems, is expected to be sampled in the first half of 1999. The processor will initially come in both 450- and 500-MHz speed grades and offer a second-generation set of extensions to the Pentium instruction set. An upgrade in 1999 also is planned for the Xeon Slot 2 processors. Code-named "Tanner," the processor module will offer larger cache sizes and higher clock speeds.

That second-generation set of extensions will supplant the

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MMX instruction set enhancements Intel introduced several years ago on the Pentium processor. The over 70 new instructions added to the Katmai processor, in conjunction with an enhanced ALU, will allow the processor to perform single-instruction/multiple-data (SIMD) operations for imaging, graphics, and audio applications. With the SIMD ability, the CPU will be able to deliver performance improvements of from two to five times the throughput of the 450-MHz Pentium for the aforementioned applications. The processor has new instructions that lets it stream data from the memory to greatly improve I/O throughput and reduce bus latency.

To achieve the higher throughput, the eight registers in the floating-point unit have been extended to 128 bits, allowing two double-precision floating-point numbers to be held in one register. That allows more numbers to be held in the register file and permits much faster computations to be performed since fewer data transfers are needed. The SIMD floating-point extensions will allow the Katmai processor, when running at 500 MHz, to deliver a peak throughput of 2 GFLOPs. However, the core of the Katmai is basically the same as that of the Pentium II. Thus, for the older instructions that both processors share, the performance of the processors will be comparable running at the same clock speed.

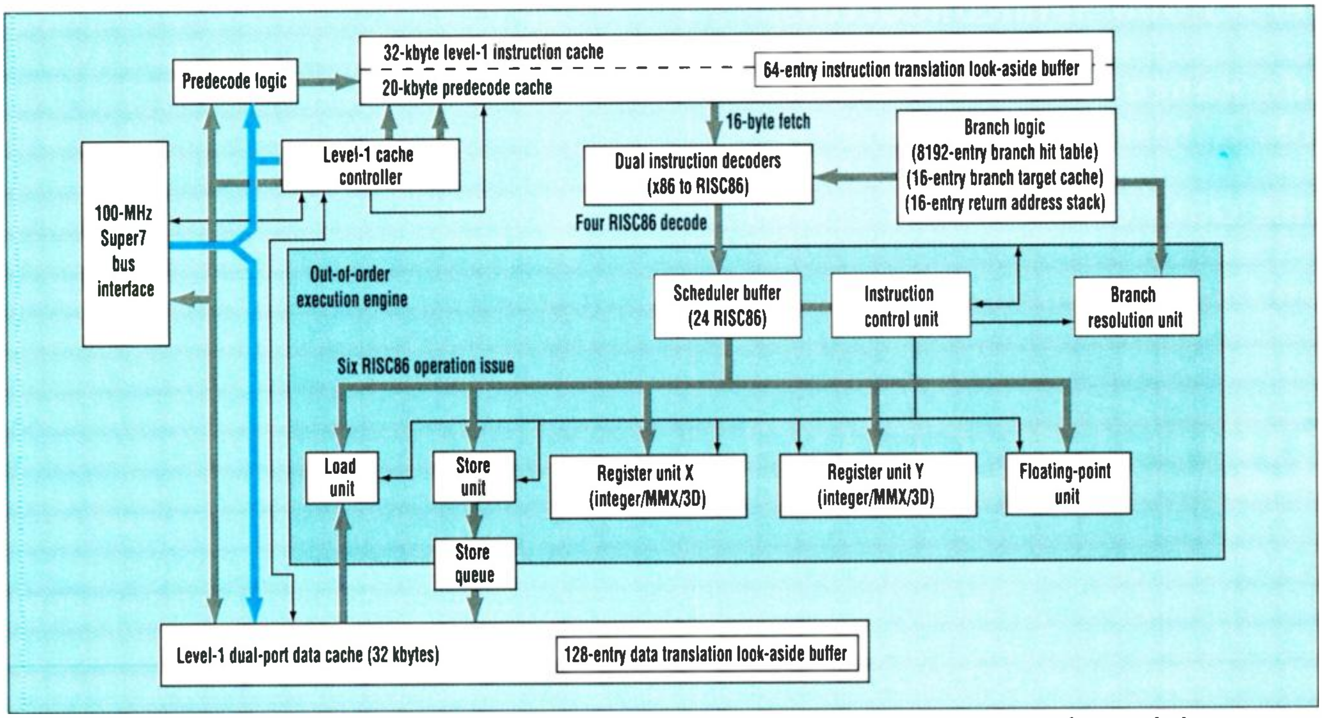
As software applications become more graphics and multimedia intensive, the need to process audio-video (AV) data streams or 3D graphics without bogging down the computational aspects of the system becomes paramount. And, since many video and graphic data structures contain large arrays of data that can be divided and processed in parallel, the use of SIMD operations becomes a very efficient approach for accelerating computational throughput. The use of the SIMD approach takes its cue from the high-end RISC processor market. CPU chips from DEC (now Compaq Computer Corp.); Hewlett-Packard Co., Palo Alto, Calif.; MIPS Technologies Inc. and Sun Microsystems Inc., both of Mountain View, Calif.; all have SIMD extensions to their instruction sets.

Although Intel has not revealed plans to perform any radical revisions to the Pentium II architecture, it will continue to improve the performance of the processor family. Those improvements will come in the form of reduced level-2 cache latencies, process shrinks to achieve higher clock speeds, and lower power-supply voltages to reduce chip power consumption.

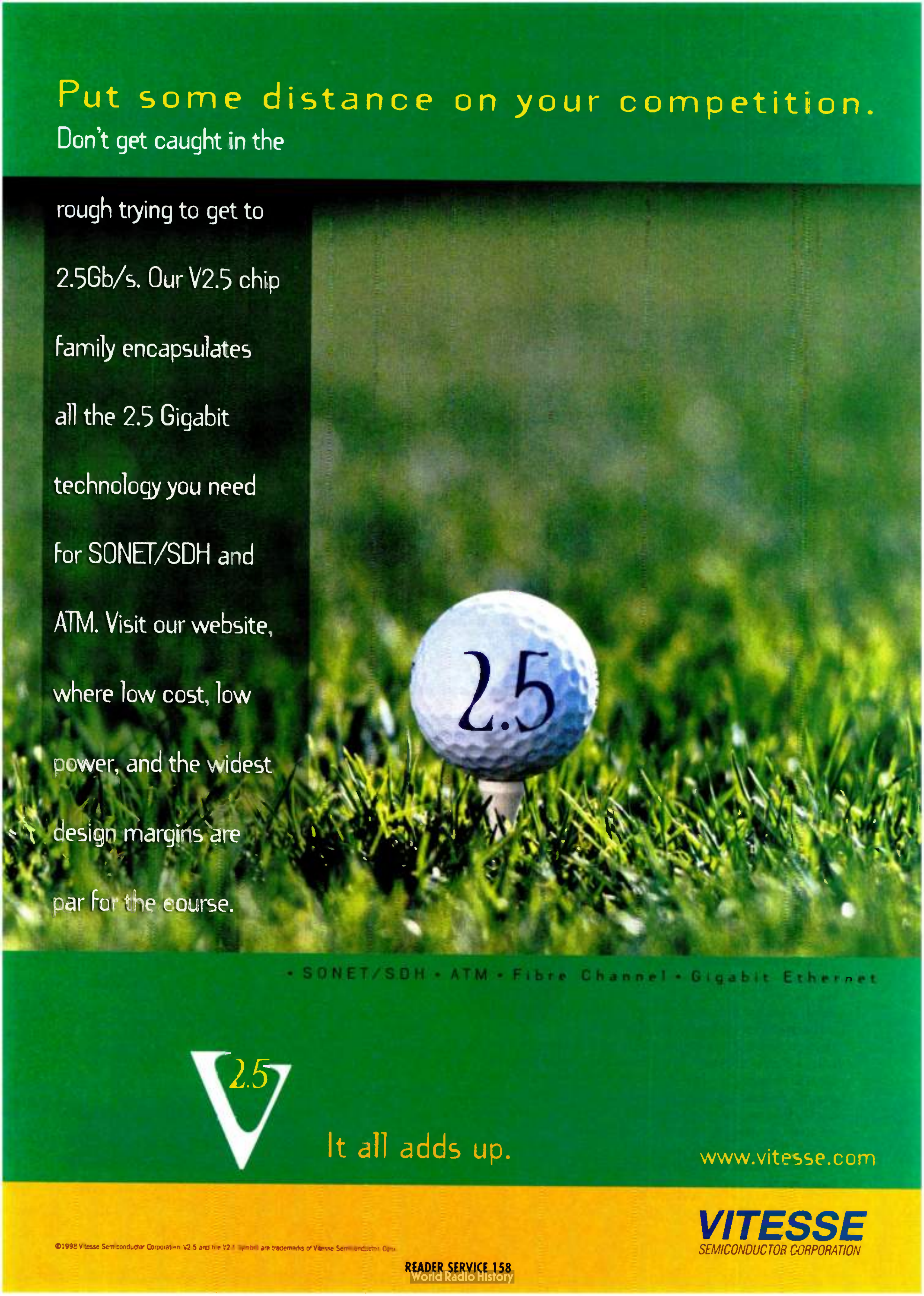
For Intel's Celeron family, which is targeted at cost-sensitive and board-space critical applications, the just-released Medocino version of the processor, which integrates a 128-kbyte level-2 cache onto the CPU, provides a significant performance boost to previous Celeron processor systems, which were bogging down due to the many external memory accesses caused by lack of the L2 cache. Thus, the 300- and 333-MHz Medocino CPUs will deliver throughputs that are within a few fractions of a Winstone98 benchmark point of a Pentium-II/300 CPU, but at a much lower overall system implementation cost.

Alternatives To Pentium II

Trying to deliver performance exceeding that of the Pentium II, the forthcoming K7 developed by AMD will meet that goal by first incorporating large on-chip level-1 caches—64 kbytes each for the instruction and data caches. The caches are also dual-ported. That allows the K7 to perform two loads and two stores simultaneously, doubling of the data-transfer rate between the caches and the processor. Approximately 22 million transistors are used in the K7—about 12 million for the level-1 caches and associated tag memories. The rest are used to implement many on-chip com-



3. The first microprocessor to incorporate the 3D Now! enhanced instruction set is Advanced Micro Devices' K6-2. It features dual integer units and an enhanced floating-point unit that allow single-instruction/multiple-data operations.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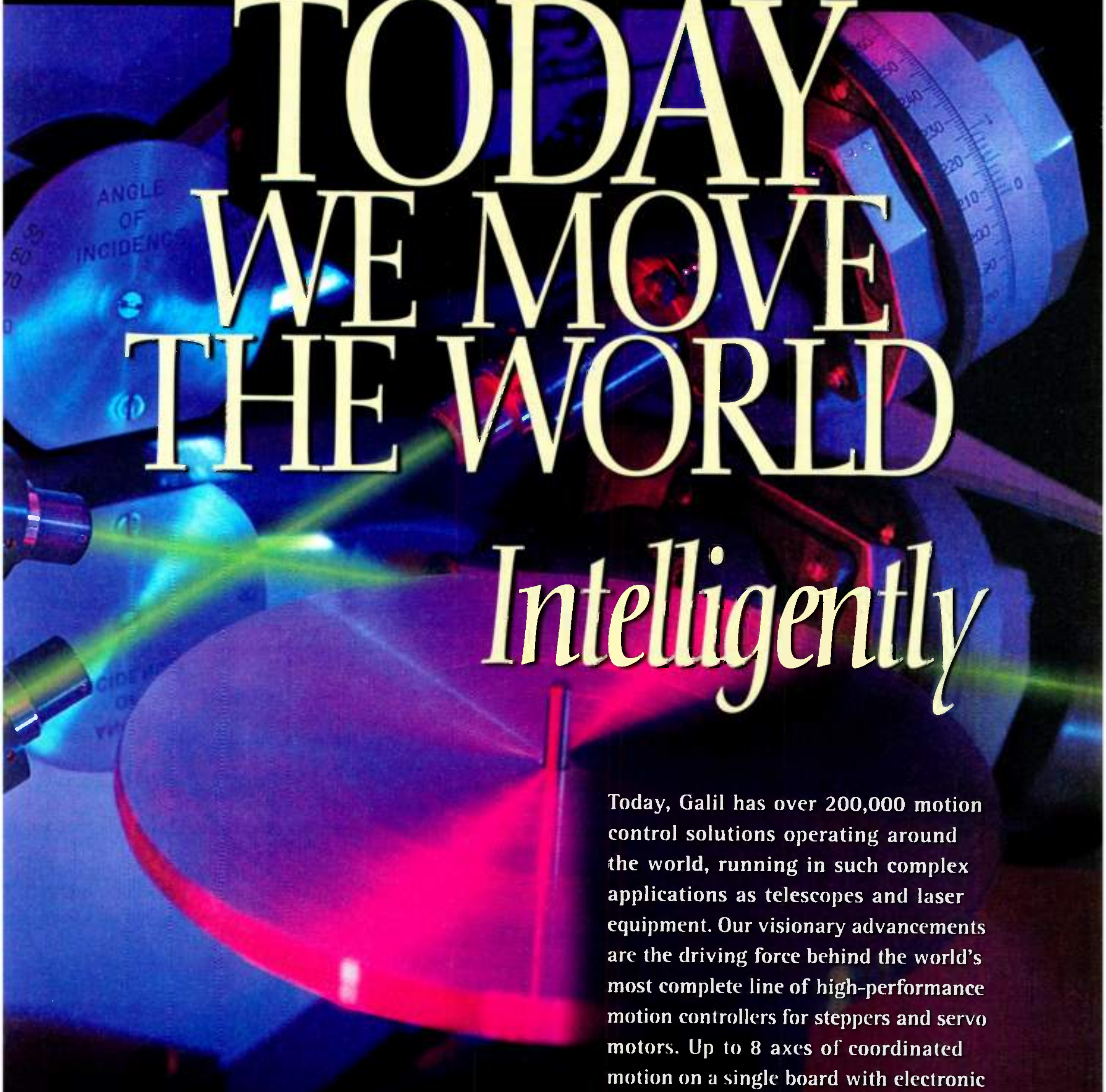

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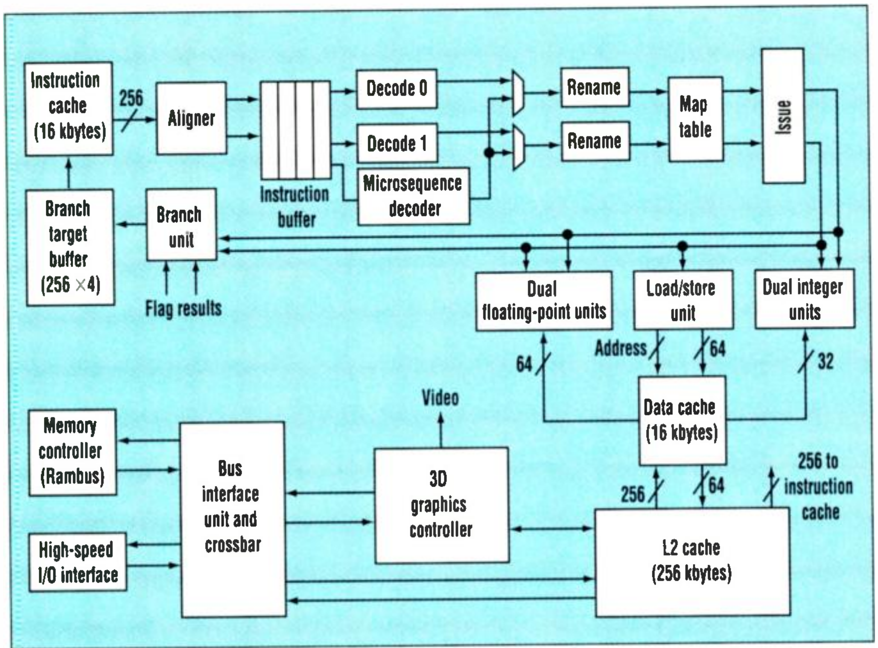

4. The forthcoming "Jalapeno" core under development at Cyrix/National Semiconductor will employ a deep, 11-stage pipeline, 16-kbyte level-1 data and instruction caches, as well as a 256 kbyte, 8-way associative level-2 cache to minimize off-chip memory accesses. At the heart of the CPU is a dual-issue engine with two integer units, two floating-point/MMX execution units, and both a branch and a load/store unit.

putational resources. Although the transistor count is pretty high, the chip area will be relatively small—just 184 mm^2—thanks to the aggressive use of 0.25-µm design rules and six levels of metal interconnections (plus local interconnects on the base level).

To speed the instruction execution stream, the K7's pipeline includes three identical integer execution units, and a floating-point unit with three execution pipelines. The floating-point unit is the first to handle superscalar and out-of-order execution of the floating-point instructions, reducing computational latency. To feed the integer and floating-point pipelines, separate schedulers are included, each of which manages 15 instructions. The processor incorporates the company's 3D Now! instruction set and MMX-compatible multimedia extensions. Those instructions allow the ALU to handle either two, four, or eight integer operations in parallel (for 32-, 16-, or 8-bit data values), thus providing some SIMD computational capability.

The 3D Now! instruction set was first implemented on the AMD K6-2 processor and is in the latest version of the K6, as well (model 9). An extension of the MMX-compatible multimedia instruction set, the 3D Now! commands are intended to open up what programmers feel is a major processing bottleneck in 3D graphics applications—the floating-point operations typically encountered when the processor performs geometry transformations, clipping, lighting calculations, object physics, and other image computations. To speed those operations, the K6-2 350-MHz processor and K6 model 9 300-MHz processor have had their ALUs and floating-point math units enhanced for single-instruction/multiple-data operations.

The added instructions facilitate operations such as pixel-motion compensation, required in MPEG image processing. To reduce the wait time for new data to arrive, the CPU also includes a new Prefetch instruction that can be used to ensure that the desired data is in the level-1 cache when needed. Fast entry/exit instructions also speed up the time required by the processor to switch between the MMX and x87 system states, eliminating much of the overhead time associated with mode switching.

Still faster versions of the K6-2 are coming out. AMD expects to release a 400-MHz version this quarter and a 450-MHz version first quarter 1999. The K6-2 also includes the 100-MHz Super7 processor/memory interface, improving data transfers between main memory and the CPU. Just over 9 million transistors are employed on the K6-2, interconnected with five layers of metal plus some local interconnects.

The 3D Now! instruction set will also be part of the CPU offerings from Cyrix/National Semiconductor in its forthcoming "Cayenne" and "Jalapeno" cores, and from Centaur/Integrated Device Technology as part of the WinChip 2 processor family. Unveiled at the recent Microprocessor Forum Conference in San Jose, Calif., the Cayenne and Jalapeno cores developed by National's Cyrix subsidiary provide designers with two new choices of CPU performance and integration levels.

For low-cost mainstream computer systems, the Jalapeno x86 core includes a dual-instruction issue CPU with register renaming and out-of-order execution. In the CPU are two integer units, two floating-point/MMX units, a branch unit, and a load/store unit. The 11-stage pipeline on the processor is much deeper than on previous versions of the CPU (typically about six stages), which allows more parallelism. Improved branch prediction, with a thousand-entry four-way branch target cache, 7-bit history and prediction memory, and 16-entry return stack, also will be incorporated on the chip.

Level-1 data and instruction caches are both 16 kbytes and four-way set associative, and an eight-way set associative 256 kbyte level-2 cache will also be on the chip. The Jalapeno core includes a 3D graphics controller and support for the 3D Now! instruction set extensions jointly defined with AMD.

The integrated graphics subsystem with multimedia support is in the form of integrated-hardware MPEG-2 and DVD playback circuits. The graphics block will include a legacy VGA controller, a setup engine, a rasterizer, and other support logic that will leverage the L2 cache for graphics functions such as textures, or for use as a composite buffer for multipass graphics features. The graphics engine will be capable of delivering 3 million polygons/s and with an external RAMDAC, and will deliver up to 266 million pixels/s.

A novel aspect of the core will be its use of a unified memory architecture (UMA) and the inclusion of a Rambus direct RDRAM memory controller on

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the chip. The UMA negates the need for a separate frame buffer memory for the graphics subsystem, lowering system cost. The Rambus controller will allow the memory subsystem to keep 32 pages open, improving memory bandwidth. In contrast, most motherboard-based memory controllers only allow about half as many pages to stay open, limiting memory bandwidth.

The Jalapeno core will be used in a CPU chip the company has dubbed the M3. Initial estimates for the chip include an area of just 120 mm^2 when fabricated in a 0.18-µm process. Expected to be sampled in the fourth quarter of 1999, the chip will be able to operate at clock frequencies of 600 MHz and higher.

A Highly Integrated Solution

A little closer to reality is the Cayenne core, a CPU based on the M2 core but with an enhanced floating-point unit that supports the SIMD functions required by the 3D Now! instruction set extensions. Company plans call for the integration of the Cayenne core into a full processor in the second quarter of 1999. That processor will be a highly integrated system-on-a-chip, the MXi processor, which will pack a 64-kbyte unified cache, a dual-issue pipelined integer and floating-point/MMX unit, a 3D graphics accelerator, MPEG acceleration hardware, and a 66-MHz PCI expansion interface. An integrated memory controller supports a 128-bit-wide SDRAM-based main memory and can provide bandwidth of more than 2 Gbytes/s.

Along with a companion southbridge-like motherboard circuit that includes the popular Super I/O functions and other system-support functions, as well as a display driver circuit, a pretty-complete PC-like system (minus memory) can be built with just four chips. Initial samples are expected by year's end and will operate at clock speeds of 366 MHz. Fabricated in a 0.25-µm process, the chip will pack about 9 million transistors yet occupy just 90 mm^2 thanks to the use of five levels of metal interconnect and C4 metal bump contacts that reduce the space required by the I/O connections.

The graphics engine on this chip could very well have been a standalone 3D graphics chip. It will support resolutions of up to 1600 by 1200 pixels, deliver more than 2 million triangles/s, and perform 3D fills at more than 120 million pixels/s while doing bilinear and trilinear filtering, Alpha blending/fog, Gouraud shading, MIP mapping, perspective-correct texturing, Z buffering, and many other graphics operations. The graphics block also delivers top-notch 2D performance, with a 1.6-Gpixel/s fill rate and 800-Mpixel/s screen-to-screen bit-block transfers. The block is also Direct 3D-compliant and is compatible with AGP software driver requirements.

Application-Specific Versions

Both the Cayenne and Jalapeno cores can be used by Cyrix/National Semiconductor to craft application-specific versions of a processor to meet focused market needs. For instance, with a little more circuitry, such as an Ethernet support block, the processor could become a network terminal or the heart of an Internet appliance.

Targeting the budget-priced PC, designers at Centaur/Integrated Device Technology have a two-pronged game plan to deliver higher-performance CPUs as part of the WinChip family. Earlier this year, the company unveiled a roadmap that included a second version of the WinChip 2 processor, the WinChip 2-3d, with an enhanced floating-point unit that can execute the SIMD 3D Now! instruction set extensions.

The chip also includes a 100-MHz main memory interface that will be Super7 socket compatible. Samples of the 233- and 266-MHz versions are slated for the first quarter of 1999, while 200-MHz Super7 versions and 225- and 240-MHz Socket 7 versions are immediately available. One additional off-shoot of the WinChip 2 is the WinChip 3, which is basically the same CPU core but packs a larger level-1 cache of 128 kbytes.

Following those CPUs is a major architectural overhaul in the form of the WinChip 4 core . The WinChip 4 will operate in the 400 to 500 MHz range, pack 128 kbytes of level-1 cache, and deliver a clock-per-instruction rate as good as the Intel Mendocino processor if the Mendocino CPU were available at the 500-MHz clock-speed option.

Like the Jalapeno core from Cyrix, the WinChip 4 will employ an 11-stage pipeline with in-order execution rather than the six-stage pipeline in the previous WinChip processors. The caches also are pipelined (1-cycle throughput) to provide synchronized operation with the deeper pipeline. Extensive use was made of programmable logic arrays and custom logic for much of the processor's control logic, and dynamic logic for many of the computational blocks to get high-performance circuits with minimal chip area.

Improving Branch Prediction

Several areas designers are paying special attention to on the WinChip 4 include improving the branch prediction with a proprietary prediction algorithm, and reducing the bus traffic. This is achieved by using large on-chip level-1 caches (64 kbytes each for the data and instruction caches), and lots of buffering and smart prefetching. By reducing the bus traffic and applying transistors that might otherwise have been used to implement out-of-order execution, WinChip4 designers estimate that the CPU will actually deliver performance comparable to the out-of-order approaches, but with a much simpler architecture.

The resulting chip, when fabricated with 0.25-µm design rules and six levels of metal interconnects, will be considerably smaller than most of the other processors—just 100 mm^2 versus 131 mm^2 and larger. That chip is targeted for production in the second half of 1999 and will include a Super7/Socket7 bus interface. When the company switches over to its 0.18-µm process, the chip area will shrink still further—down to about 60 mm^2. The scaled version is targeted for sampling in late 1999 and should be able to operate at clock frequencies of 500 to 700 MHz.

A Wide Range Of Options

The range of performance and features available to designers on x86 processors spans a wide gamut, allowing system designers to optimize the performance and cost of their systems. It's no longer a "one CPU fits all" design scenario. The abundant CPU offerings also show that through innovative architectural implementations, differing approaches can all still meet the software compatibility requirements of the PC industry while delivering top-notch performance.

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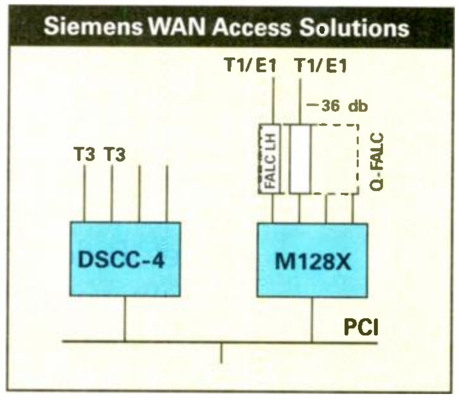

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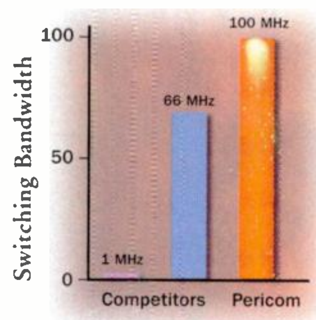

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Mobile PC with GPS

The PC–510 is a ruggedized PC with a GPS interface, 48 lines of digital I/O, 6 serial ports, flat panel and CRT video with GUI accelerator, LCD bias supply, watchdog timer, up to 72 MB flash memory, up to 48 MB EDO DRAM, NT compatibility, 133 MHz CPU, EBX outline, resident DOS, PC/104 expansions, –40° to 70° C operations, opto–isolated interrupts and 5V supply. The GPS interface accepts the Rockwell Jupiter module as a daughterboard. The 48 digital I/O are bit programmable and drive opto–module racks directly. The PC–510 has advanced power management with a dissipation range of 3.5–8W.

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Pentium® performance at low power

The 5066 uses 100% CMOS circuitry and a 3.3V CPU to reduce heat generation and improve reliability. The stock unit includes embedded DOS 6.22 and diagnostic software in flash, two serial ports, floppy and enhanced parallel port, watchdog timer, opto–isolated interrupt, ISA Bus interface and –40° to 70° C operation. The antivibration DIMM socket allows DRAM expansion to 33 MB. The card can operate in any ISA Bus backplane or be a stand–alone SBC with the application of 5V.

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Palm–sized PC replaces 2–3 cards

The 6040 is a complete PC with 10 channels of 12–bit analog I/O and 24 lines of digital I/O in a tiny 4.5" x 4.9" format. The 6040 operates stand–alone (connect 5V) as a data acquisition and control system, or it can be expanded in an ISA Bus card cage. The card comes complete with DOS 6.22, a multitasking control language, utilities, DRAM, battery–backed SRAM and flash memory. The two serial ports are RS–232 with an optional opto–isolated RS–485 for multidrop operation. RTC, watchdog timer, opto–isolated interrupts, parallel port, and floppy disk ports are also standard. The –40° to 85° C operation excels in any environment.

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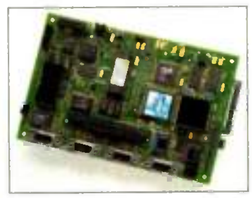

The PC–325D is a mobile PC with a GPS interface, PCMCIA, 24 lines of digital I/O, 6 serial ports with IEC1000 ESD protection, bulkhead style connectors, floppy/hard disk ports, 1.5 MB flash memory, 16 MB DRAM, NT compatible, 133 MHz CPU, resident DOS 6.22, PC/104 expansion, –40° to 85° C operation, and 5V supply. The PC–325D has a small 5.9" x 7.5" footprint, dissipates less than 5W, withstands high shock and vibration, and has a MTBF of 16.3 years.

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5664 SNAP I/O interface

The 5664 provides a seamless interface to the OPTO 22, SNAP I/O™ systems. It supports 32 opto–isolated analog and digital I/O modules (max. 64 analog or 128 digital channels). The analog modules support RTD, thermocouple, voltage and current inputs and outputs. The digital modules support high voltage/current inputs/outputs with 2500V of isolation. The SNAP I/O systems allows mixing and matching within the same rack. The 5664 operates from –40° to 85° C, requires only 5V, is ISA Bus compatible and withstands 40g of shock and 10g of vibration. The number of I/O modules can be expanded to 224 in a single Octagon card cage.

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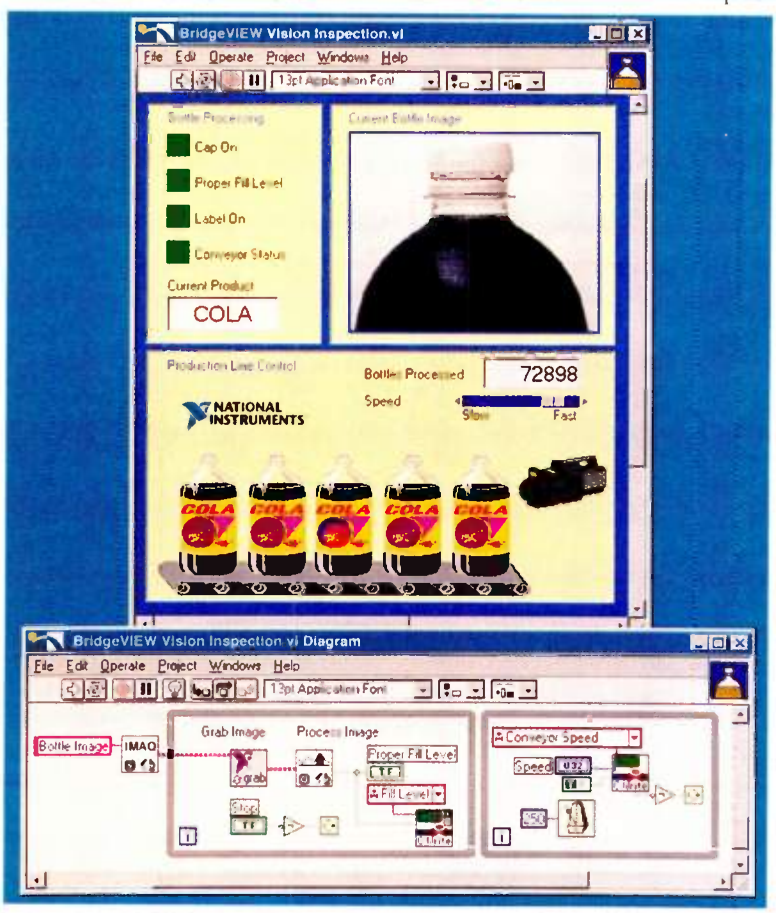
Visual Tools Heat Up Automation And Process-Control Development

Object-Oriented Languages And Software Suites Are Bringing Open Architectures Like OPC And ActiveX To The Factory Floor.

Joseph Desposito

SPECIAL REPORT

Factory automation systems are undergoing a paradigm shift from closed proprietary systems to open architectures. Traditional hardware, such as programmable logic controllers (PLCs), is being augmented or replaced by such standard automation hardware as VME, VXI, Compact PCI, and PXI controller and data-acquisition boards. Proprietary software is being replaced by software based on open system technologies, such as OLE for Process Control (OPC), Distributed Component Object Model (DCOM), and ActiveX. One driving force behind these changes is the Microsoft Windows NT operating system. Windows NT is a natural for the factory floor, since it's also the operating system used for many corporate MIS systems. This gives large organizations the ability to work with one OS—and the industry standards developed for it—throughout the enterprise. And, just as commercial software for Windows NT is developed with visual programming tools, so too is industrial automation software.

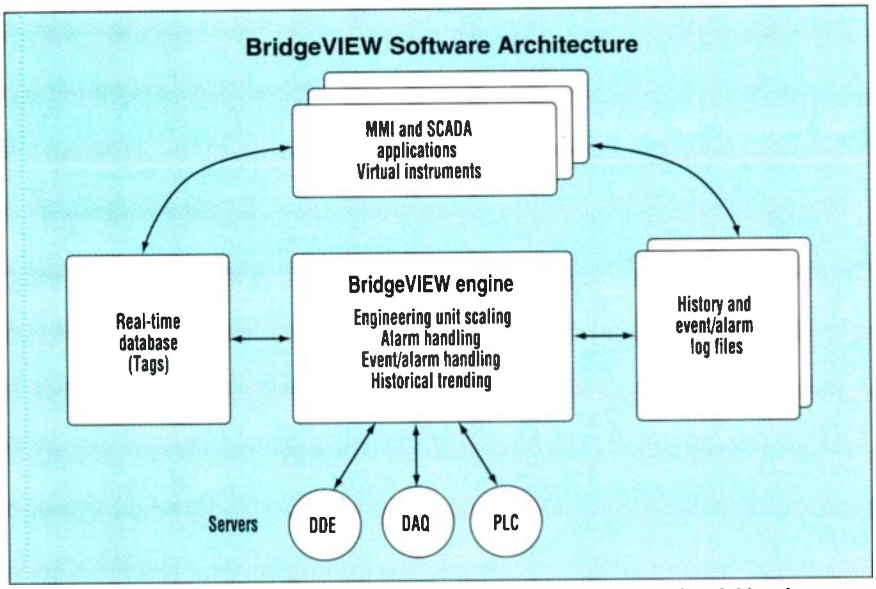


Art Courtesy: National Instruments

The visual tools available for developing industrial automation systems have many differences. But, they have similarities, too. For instance, most visual tools give you the ability to create HMI (human-machine interface) and SCADA (supervisory control and data acquisition) software, as well as historical trending and alarm software. And, most visual tools support computer industry software standards such as OPC (see *"What Is OPC?," p. 88*), DCOM, and ActiveX.

Programming In G

One way to meet the factory floor's development challenge is to tap the power of National Instruments' G programming language, the foundation of NI's LabVIEW and BridgeVIEW products. G is an object-oriented language in which you graphically assemble software function blocks to develop HMI, data acquisition, analysis, and supervisory control applications. What is the difference between the two products? According to Ryan McDonald, BridgeVIEW marketing manager, "We really consider BridgeVIEW as LabVIEW IA—



1. The National Instruments BridgeVIEW architecture is open, modular and scalable. The engine maintains up-to-date I/O values and status information in a high-performance, real-time database that's accessible to human-machine-interface (HMI) and control applications.

LabVIEW for industrial automation. We had a number of customers using LabVIEW for process control and factory automation systems. In fact, even going back to 1991, we had a set of graphic symbols for LabVIEW users—pipes, valves, and so forth based on the ISA standards for graphic symbols. We saw a need for stepping up the tag-based I/O system of LabVIEW, and BridgeVIEW just evolved out of that."

Ray Almgren, the director of test and measurement marketing at National Instruments, points out that LabVIEW plays two roles in factory-systems development. One role is in the programming of the measurement devices themselves, so that you can make the measurements, do the real-time control and analysis, and send the data over the Internet or network. As a visual tool, it also can be used in another role to build the user interface. "This is really what makes LabVIEW a unique product: It is a user-interface builder, as well as the measurement tools builder," says Almgren.

He continues, "These are things a test and measurement engineer doesn't need to do, but a process engineer does. We coded that capability into BridgeVIEW. If you just used LabVIEW, you would be writing code over and over again for no reason. But BridgeVIEW supplies a lot of that code, as well as all the servers for industrial devices such as PLCs."

BridgeVIEW has a modular, open system architecture *(Fig. 1)*. The BridgeVIEW engine maintains up-to-date I/O values and status information which it receives from device servers in a real-time database. This database is accessible to HMI and control applications written with G. The engine also performs other system functions, such as engineering unit conversion, event monitoring, alarm processing and logging, historical logging and trending, and system security.

Earlier this year, National Instruments introduced BridgeVIEW 2.0. This version features multithreading, full OPC client support, distributed computing tools, translation and documentation tools, programmatic menu bars, and multistep undoing. BridgeVIEW 2.0 also is an ActiveX container, automation server, as well

What Is OPC?

OPC, or OLE for Process Control, is an emerging software standard based on Microsoft's Object Linking and Embedding/Component Object Model (OLE/COM) and Distributed COM (DCOM) technologies. Essentially, OPC gives factory automation applications access to industrial-plant-floor data.

The specification is managed by the OPC Foundation and is also a trademark of that foundation. The OPC Foundation expresses its charter as follows: To develop an open and interoperable interface standard, based upon the functional requirements of OLE/COM and DCOM technology, that fosters greater interoperability between automation/control applications, field systems/devices, and business/office applications.

In the past, each application developer had to write a custom interface, or server/driver, to exchange data with hardware field devices. OPC eliminates this. By using this common, high-performance interface, the server/driver is developed once, and then reused by human-machine interface (HMI), Supervisory Control and Data Acquisition (SCADA), control, and custom applications.

As a point of comparison, the inclusion of a standard interface between the operating system, printers and applications allows any program running in the Microsoft Windows environment to print to any printer. In the same way, OPC allows any OPC-compliant SCADA database or HMI to communicate with any compliant remote terminal unit (RTU) or programmable logic controller (PLC), with no additional software required to complete the interface.

Central to the OPC specification is a client/server model where the OPC server provides a standard interface to OPC objects. This allows client applications to control devices and manage device data in a generic way. OPC-enabled applications can communicate with any OPC server, whether that server represents a sensor, valve, or PLC.

To learn more about the OPC Foundation, visit its Web site at *www.opcfoundation.com*.

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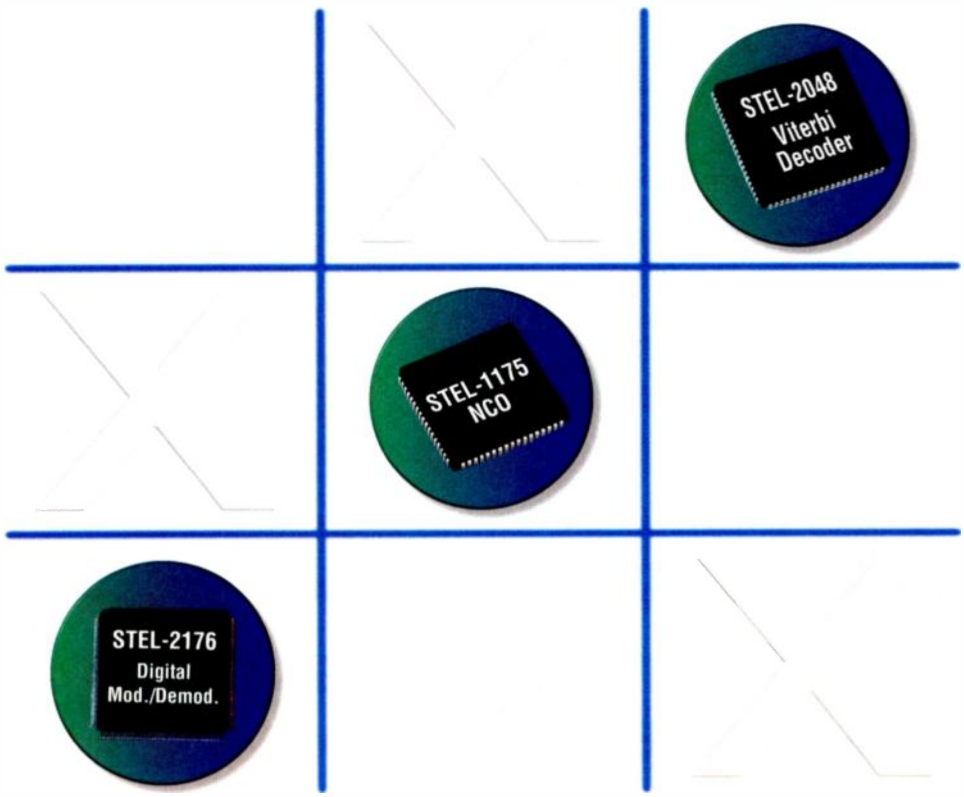

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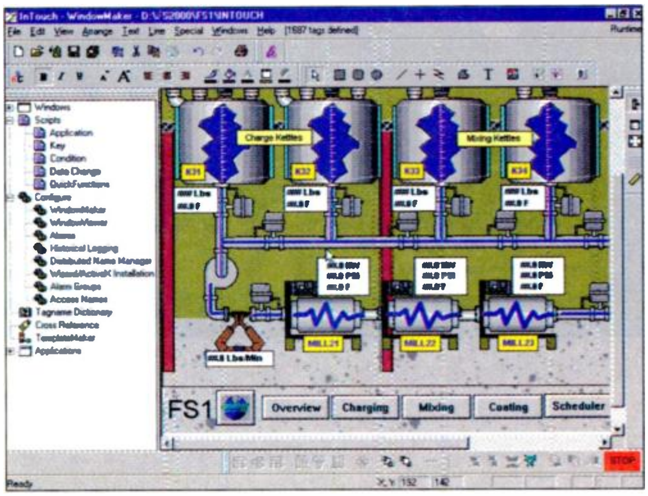
as a TCP/IP server.

National Instruments has developed a number of toolkits that work with BridgeVIEW. These include the statistical process control (SPC), SQL, PID Control, Picture Control, and Internet Developers Toolkits. The SPC Toolkit, for example, includes all the functions needed to incorporate SPC analysis and presentation into automation applications. It provides three primary SPC functions: control charts, process statistics, and Pareto analysis.



2. FactorySuite 2000 from Wonderware Corp. includes InTouch 7.0 for WindowsNT 4.0, a 32-bit object-oriented, graphical HMI application generator. This is a typical screen produced by InTouch.

How Suite It Is

It's not surprising that some industrial automation software companies are integrating their offerings into suites of products. After all, most PC business software is sold this way. Wonderware is one company trying to take advantage of this approach with its latest version of FactorySuite 2000 *(Fig. 2)*.

All application modules in this client/server package make extensive use of Microsoft's ActiveX technology to enhance the product's ease of use. The core components of the suite are InTouch, a human-machine interface for visualization; InControl for Windows NT-based machine and process control; IndustrialSQL Server, a real-time relational database for the plant floor; and Scout, an Internet/intranet tool for remote data viewing. Two application components also are included: InTrack, for resource management, and InBatch for batch management. Finally, the suite includes Wonderware I/O servers to connect FactorySuite 2000 to data on the plant floor.

"A primary feature of the suite is the new Version 7.0 module of our Wonderware InTouch human-machine interface program, which serves as the common GUI and client visualization portion of the FactorySuite," explains Roy Slavin, Wonderware president and CEO. "It includes the Application Explorer to enhance navigation among the integrated suite components. And, it functions as an ActiveX container so users can also drop any third-party ActiveX objects into any FactorySuite application window for plug-and-play extension of FactorySuite application capabilities."

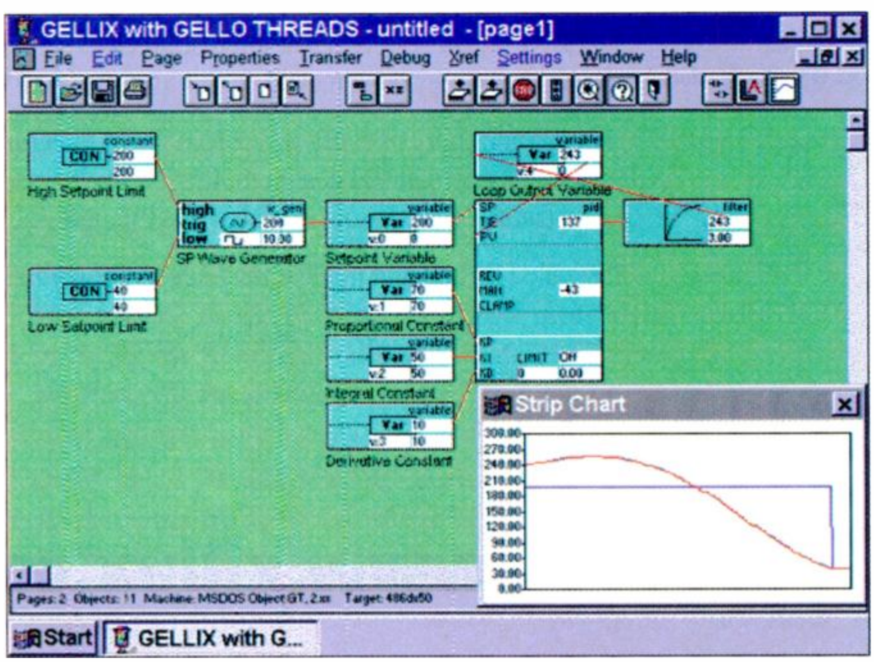
InTouch 7.0 visualization software for Windows NT 4.0 is a 32-bit object-oriented, graphical HMI application generator. Figure 2 shows a typical screen produced by the product. InTouch features an extensive set of predefined industrial graphics Wizards. Using these wizards, a developer can create complex operator-interface displays. InTouch also includes a scripting language for customizing logic and operator interaction.

A new product from the Foxboro Company, called WonderLink, integrates real-time data from Foxboro's I/A Series intelligent automation system into Wonderware's InTouch HMI software. WonderLink provides engineers and managers in I/A Series-equipped plants with real-time process graphics and global alarm-acknowledge capabilities on their PCs via Wonderware displays. These process graphics can reflect a broad array of both Foxboro and Wonderware data sources. WonderLink also works with Wonderware's Scout Web browser, providing I/A Series users with secure Web access to dynamic, real-time process data.

Joint Development

Developed jointly by the Foxboro Company and Wonderware Corp., WonderLink is part of Foxboro's suite of Plant Information Management System (PIMS) software products. Foxboro and Wonderware are both part of the Siebe Intelligent Automation division of Siebe plc.

Rockwell Automation also has integrated software for process-control applications in the Rockwell Software



3. Gello from Event Technologies is an object-oriented programming language for control applications. Gello Threads is an optional flowchart front end for Gellix, the Gello editor.

ProcessPak family. "In ProcessPak, we've done more than copy software products onto one CD," says Charlie Norz, senior marketing engineer. "We've actually taken our batch, programming, human-machine interface, and communications software, and integrated them into a one scalable solution for process-control applications."

Rockwell Software will have two versions of ProcessPak—one for batch applications and another for continuous applications. ProcessPak for batch includes the core functionality of Rockwell Software: RSBatch, RSLogix, RSLogix Frameworks, RSView32, RSView32 Active Display System, RSLinx, and Library Manager. ProcessPak for continuous applications will be similar, but won't include the batch option. Rockwell Software also is offering application-specific templates optimized for specific industries. The first set of templates, designed for the brewing industry, includes custom graphics and control code.

Function-Block Programming

RSLogix Frameworks lets you graphically program systems using function-block programming. A function block is a set of instructions contained in a graphic block that can be connected to other blocks, forming a program. RSLogix is the same software used to program the Allen-Bradley PLC family.

ProcessPak HMI capabilities are based on RSView32, a Windows-based program for data-acquisition monitoring and controlling industrial-automation applications. RSView32 includes real-time animated graphics, trending and alarm summaries, and integrates with third-party software products to maximize the features of ActiveX, Visual Basic for Applications (VBA), Open Database Connectivity (ODBC), and OPC technology. ProcessPak's client/server features are based on the RSView32 Active Display System. This gives ProcessPak users the option to immediately access any information regarding batch status. Users can monitor system information locally or from a remote client server by viewing and interacting with real-time animated graphics.

Communication capabilities are based on RSLinx, a communications solution for Microsoft Windows NT OSs. Users can view all active networks through a single window, as well as run any combination of supported applications simultaneously through communication interfaces.

OOP For Control Applications

An object-oriented programming (OOP) language for creating and executing control-application programs is Gello from Event Technologies Inc. (ETI). Gello works together with several other software components like Gellix, Gellor Threads, and the Object GT Engine. Gellix, a Microsoft Windows editor, lets you create, modify, and save Gello control programs. Gello Threads is an optional flowchart front end to Gellix, which gives you the ability to tightly define the execution of a control program *(Fig. 3)*. The Object GT Engine is the run-time execution code running in the target controller's CPU and executing the downloaded Gello program.

Gello offers a visual presentation of control logic. Each object contains a description and an industry-standard symbol as its icon, which makes the object's function clear. Each object can have a comment associated with it. Connections between objects are colored to indicate the type of data being passed from one to the next (integer, binary, etc.). One of the most powerful features of the Gellix editor is simulation, permitting you to see exactly how the logic you created will execute in the Object GT Engine before ever powering up the controls.

ETI has licensed VenturCom's Hard Real-Time Extension (RTX4.1) for use with Gello control software. "Our Gello software, running on an NT open-architecture environment with hard real-time performance capabilities, will provide the industry with a suite of productivity tools offering a high level of scalable, determinate control performance," says Rick Pryce, president of Event Technologies.

VenturCom just recently announced the availability of an enhanced version of its real-time extension, RTX 4.2 for Windows NT. According to the company, the RTX 4.2 enhanced vesion includes extensive performance improvements, new real-time programming tools and functions, as well as capabilities that allow easy porting of NT applications to Windows CE environments.

The products mentioned here are just a sampling of the visual tools available for industrial automation and process control. But, they each have one thing in common. They all seem to point toward a new, open direction for software and hardware on the factory floor.

Companies Mentioned In This Article

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Observing Complex Signals In Embedded Systems Is Easier To Do With The Right Kind Of Waveform Display Tool.

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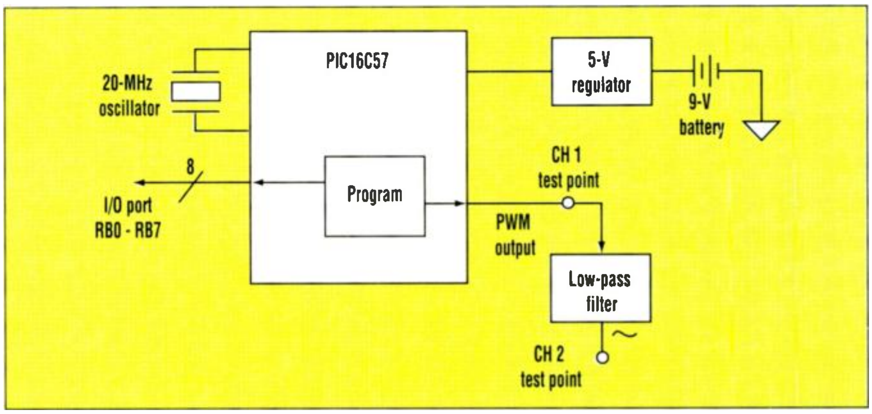
Embedded 8-bit microcontrollers have become ubiquitous today, especially in industrial, consumer, telecommunications, and automotive applications. Products that used to be based on simple mechanical (pulleys and levers) and electrical (switches and motors) designs now have microcontrollers at the heart of their operation. Chances are, if the product plugs into the wall or is battery operated, it has a microcontroller inside. Just take a look around the typical home or office. The inclusion of 8-bit embedded control doesn't only add competitive functionality. It usually improves electrical efficiency and reduces overall product cost, too.

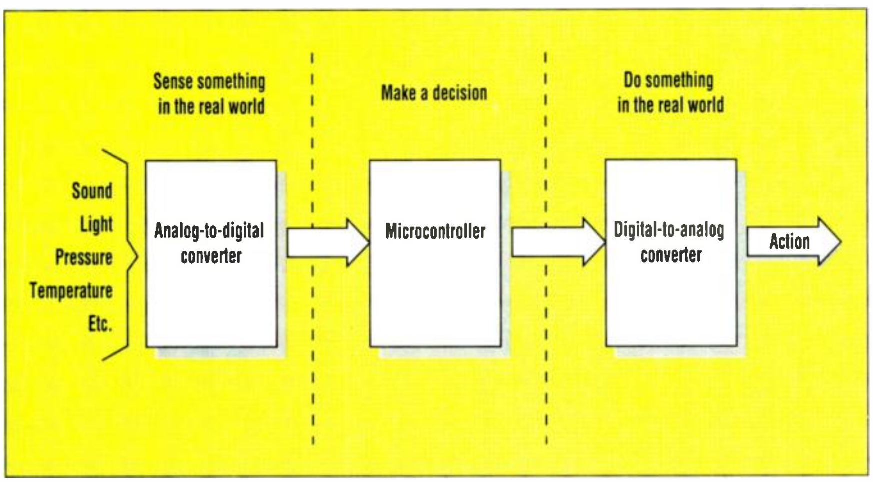


2. Parallax's BASIC Stamp II is an embedded-control module based on a Microchip PIC16C57 8-bit microcontroller. Like many designs based on 8- and 16-bit microcontrollers, the hardware is simple. But, the signals generated by these designs are often complex.

These microcontroller unit-based products provide a new challenge: How does the embedded designer test the hardware and software of these designs? Since the key to debugging any electronic design is "seeing" the signals, engineers traditionally used the dual-channel oscilloscope as their workhorse instrument. While the dual-channel scope works fine for simpler electronic designs, it's not the best choice for the more complex microcontroller designs. Often, multiple analog and digital I/O signals must be monitored simultaneously.

Figure 1 shows a simplified block diagram of an embedded design based on an 8-bit microcontroller. There are three major blocks: the analog-to-digital converter (ADC), the microcontroller unit (MCU), and the digital-to-analog converter (DAC). Although shown as separate blocks in the figure, many of today's microcontrollers have converters embedded on the chip. Embedded systems usually monitor, or are driven by, some type of real-world analog-input phenomena such as sound, temperature, pressure, and so forth.

The MCU block is responsible for decision-making, timing, and generating a digital or analog response—or both. In an embedded system, analog signals tend to be much slower in frequency compared to the digital control signals in the microcontroller block.



1. This simplified block diagram of a typical microcontroller-based design shows how real-world analog signals, such as temperature, are processed so that the system can perform real-world actions like raising or lowering the temperature.

Design-Testing Alternatives

One problem surfaces when testing microcontroller-based designs: How do you test and monitor the slow analog inputs and outputs, while monitoring the much faster digital control sig-

DESIGN NOTES

New Charger Topology Maximizes Battery Charging Speed

Design Note 194

Fran Hoffart

Introduction

Battery charging in notebook computers and other portable products generally involves compromises. A notebook computer's AC adapter is usually sized to charge the battery at its maximum rate when the computer is off. In this condition, the computer draws essentially no power, so the full capacity of the adapter can be used for charging the battery. However, when the computer is turned on, charging current is usually reduced to a low rate to avoid overloading the AC adapter. You can use your computer or fast charge your battery, but not both at the same time.

Linear Technology has developed a new battery charger topology that maximizes the battery charging rate, even when the computer is on, without increasing the size or capacity of the AC adapter power source. Instead of simply reducing the charging current to an arbitrarily low level, the charger monitors the current drawn from the AC adapter and automatically reduces the charging current only when necessary to avoid overloading the AC adapter. At all other times, the charging current can be at the maximum programmed value if the battery demands it. Since average notebook power consumption is considerably lower than peak demand, battery charging can now continue at nearly the same rate whether the computer is on or off. This translates to faster battery charging and, in many cases, a smaller, less expensive AC adapter.

LT®1511 Battery Charger IC

The block diagram in Figure 1 shows the basic functions performed by a battery charger IC using this patented topology*. The LT1511 is a high efficiency 200kHz switching regulator IC in a step-down configuration suitable for charging lithium-ion batteries. It contains multiple feedback loops for constant charge voltage, constant charge current and input current limit. Low value resistors (R_{S1} and R_{S2}) are used to sense the charge current and the current drawn from the input power source (AC adapter). The input current limit control loop allows the input power supply or AC adapter to provide current to power notebook circuitry and simultaneously charge a battery without overloading the input power supply. As the notebook current requirements increase, the LT1511 begins adjusting the battery charging current downward to keep the input power supply current below a predetermined limit.

Also included on the die are a 4A switching transistor, precision 0.5% voltage reference, adjustable undervoltage lockout and autoshutdown control (3µA battery drain when input power is removed).

The oscilloscope photo in Figure 2 illustrates how the charging current (center) decreases as the load current (top) increases, so as not to exceed the AC adapter current

*US patent number 5,723,970

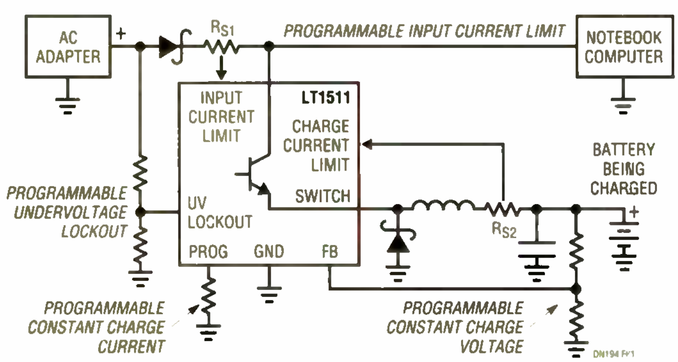


Figure 1. Block Diagram of LT1511 Step-Down Battery Charger Illustrating Input Current and Charge Current Limit Functions

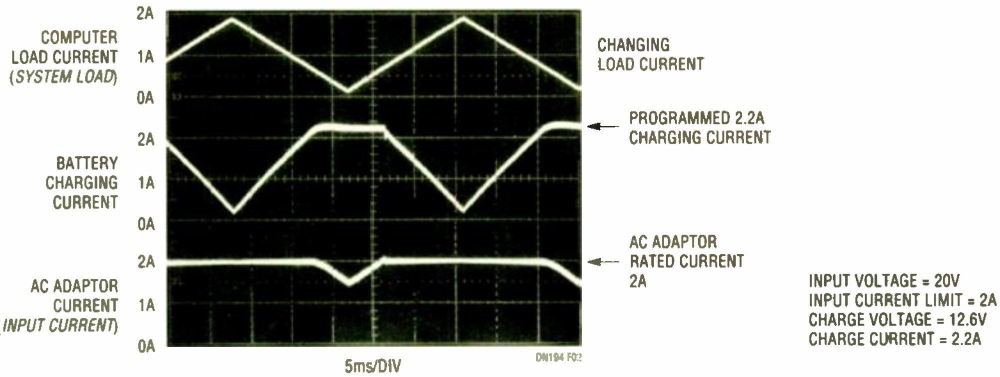


Figure 2. Current Waveforms Show How Charging Current (Middle) Drops When Laptop Computer Current (Top) Rises to Ensure That AC Adapter Current (Bottom) Does Not Exceed Programmed Limit

limit (bottom). Note: for this photo, the changing computer load current is shown as a triangle waveform. The actual computer load current waveform will be much different.

All Surface Mount Lithium-Ion Charger

The circuit shown in Figure 3 is a CC/CV charger that can be used to charge up to five series lithium-ion cells at currents up to 3A. Charge current is easily adjustable using a single resistor, a control voltage, a PWM signal or a DAC output. The circuit values shown are for 12.6V out (3 cells) and 2.2A charge current. The input current limit is set at 2A by the 0.05Ω current sense resistor, R4, which develops the required 100mV sense voltage. Resistors R1 and R2 program undervoltage lockout, which keeps the charger off until the input voltage reaches 11V.

Battery manufacturers recommend terminating the charge after a fixed amount of time has passed. Using an external timer, the charging can be stopped by programming the charge current to zero by using the program pin (Pin 19), pulling the program pin low, or pulling the V_C pin low. For additional circuit information, please consult the LT1511 data sheet, Design Note 124 or Design Note 144.

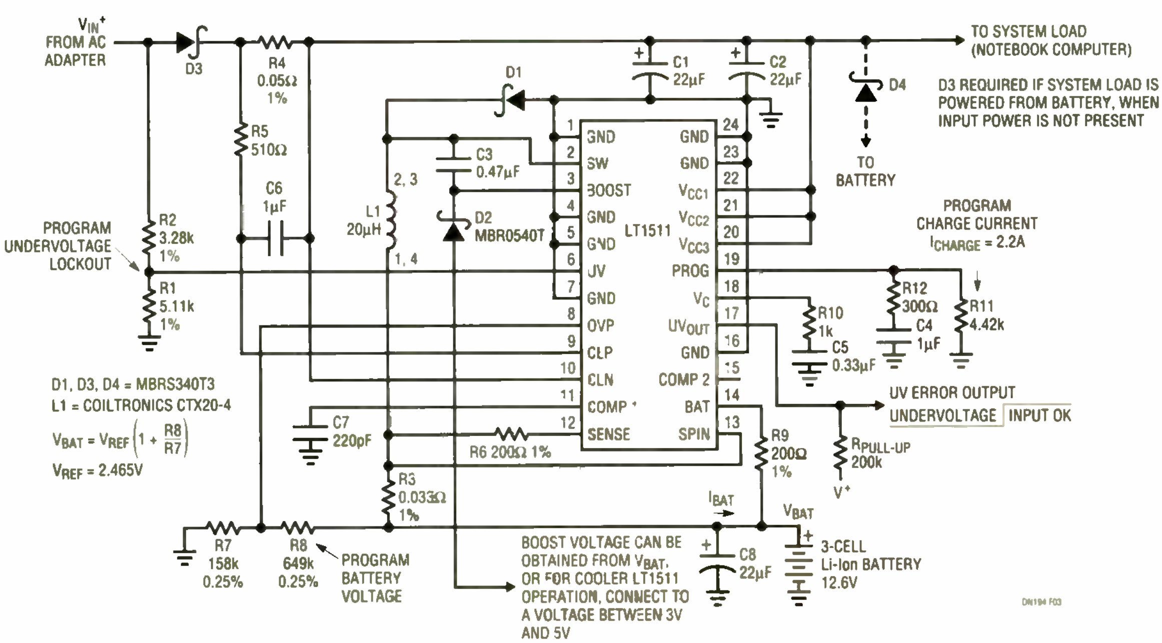


Figure 3. Programmable Constant Current/Constant Voltage Battery Charger with Input Current Limit

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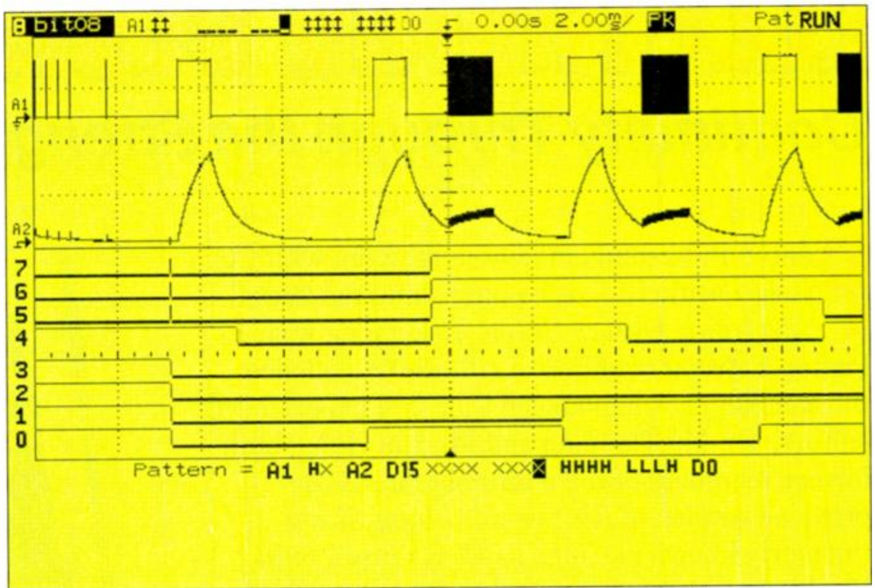


4. This screen shot shows the same 10 waveforms captured in Figure 3. But this time, the display of repetitive acquisitions is stable. This is the result of triggering the scope on a unique pattern condition that occurs only once in each cycle of the MCU's program code.

nals at the same time? For instance, how do you determine if the MCU's software generated the correct digital response based on the analog input? With a conventional dual-channel oscilloscope, it may be impossible to monitor both the analog and digital signals due to the extreme difference in timing required for each signal type. In addition, two channels can be very limiting. It's only possible to monitor one analog and one digital signal simultaneously, and logic triggering is usually not available on dual-channel oscilloscopes. Due to its slow speed, noise, or lack of definition, triggering on the analog signal may not be an option anyway.

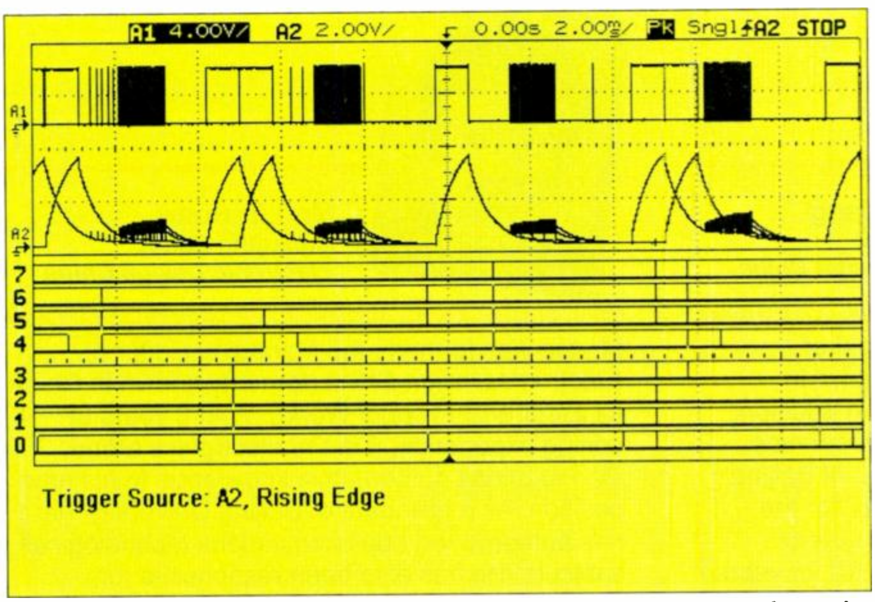
Suppose the design engineer wants the scope to trigger when a sensor indicates that the temperature of an industrial furnace has dropped below 1500°C. To do this, the first step is to determine the level of the calibrated analog signal that corresponds to 1500°C. Compounding the triggering problem is the fact that the analog signal may be changing so slowly that a small amount of noise on the temperature sensor's output could trigger the scope prematurely.

A better solution may be to trigger on a particular digital response of the microcontroller corresponding to the 1500-degree temperature threshold. To overcome the temperature sensor noise problem, the microcontroller might have to be programmed to include hysteresis. However, triggering on a microcontroller output is not possible with a dual-channel scope. A four-channel scope is a better option for testing microcontroller-based designs because of the ability to monitor up to three digital I/O lines together with one analog input or output. In addition, many four-channel scopes are capable of establishing a trigger condition based on all four scope inputs. Unfortunately, even four channels aren't always enough to see what's going on in the system.

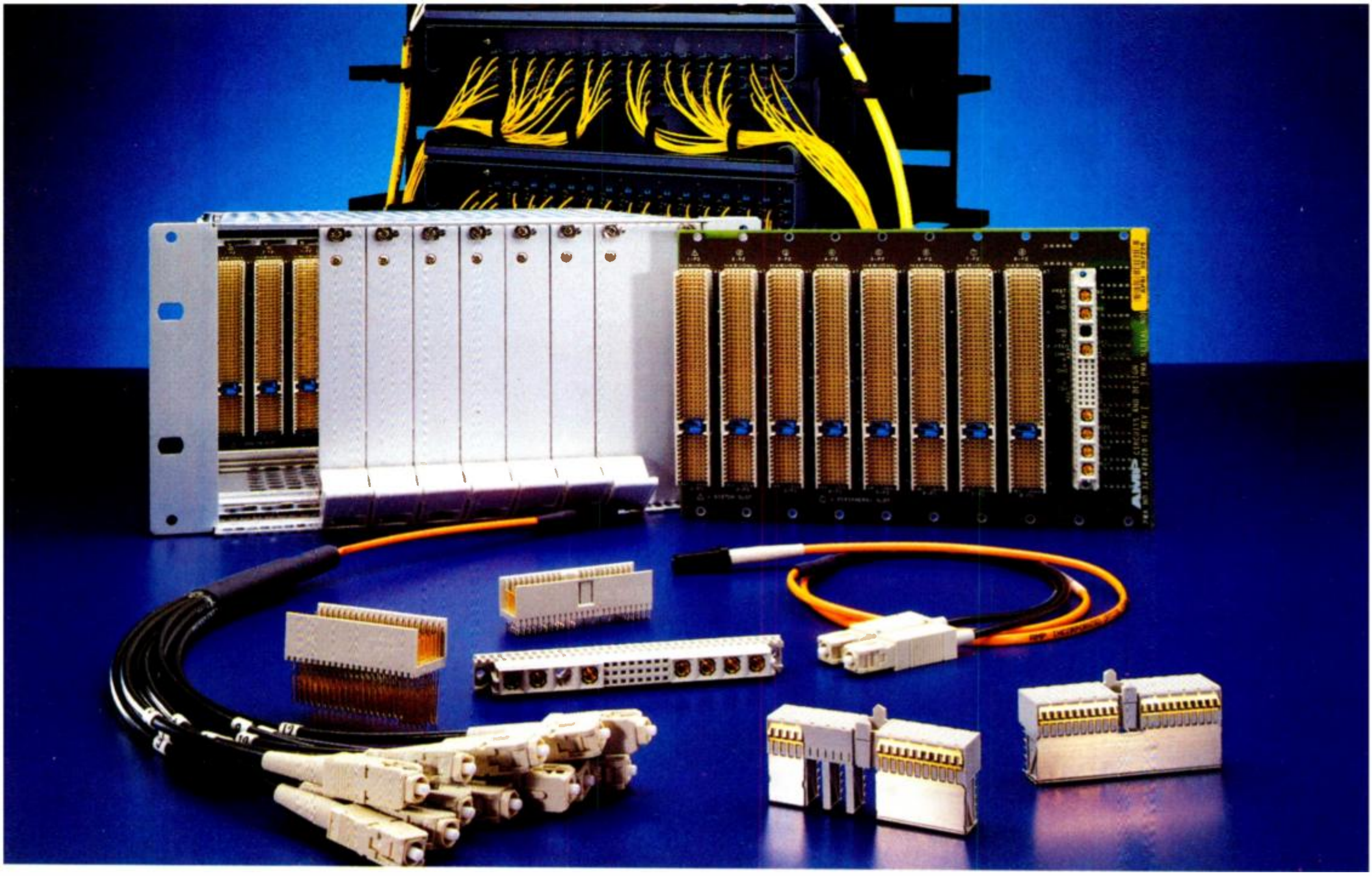
A Logic Analyzer?

Another measurement solution is a logic analyzer, maybe one with built-in scope capabilities. Most designers of 8-bit systems wouldn't consider this option for very long, though. The majority of 8-bit designs don't warrant the full digital-measurement power and complexity, not to mention the expense, of a full-blown logic analyzer. Logic analyzers usually have large numbers of acquisition channels (greater than 48), primarily intended to capture bus-based microprocessor signal activity. The typical 8-bit microcontroller doesn't even provide pins for its address and data buses. Also, when compared to the familiar scope, logic analyzers have slower updates and can be difficult to set up. It's often faster to just poke and probe with a dual-channel scope until the signal problems are found, rather than spend hours learning or re-learning how to set up the logic analyzer to capture a few additional signals.

Probably the best measurement solution for debugging 8-bit embedded systems is a hybrid scope/logic analyzer such as Hewlett-Packard's mixed-signal oscilloscope (MSO). These instruments look and run more



3. This screen shot shows a repetitive capture—using a mixed-signal oscilloscope—of 10 analog and digital I/O signals from the BASIC Stamp II MCU-based control module. The multiple, phase-shifted images captured in this set of acquisitions are caused by trying to trigger on the rising edge of channel A2.



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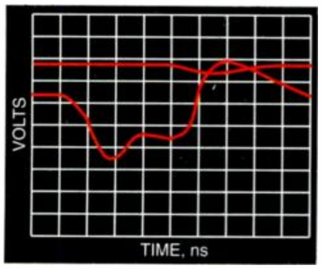

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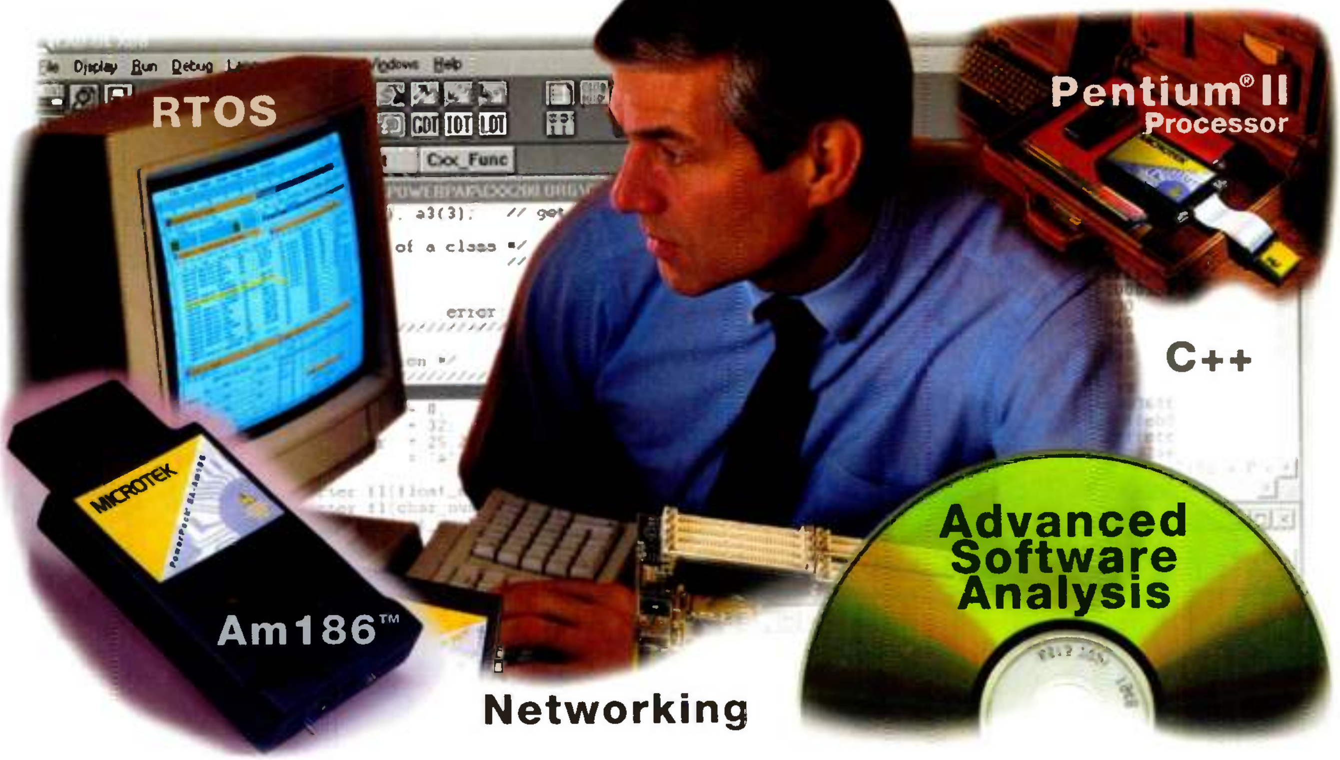

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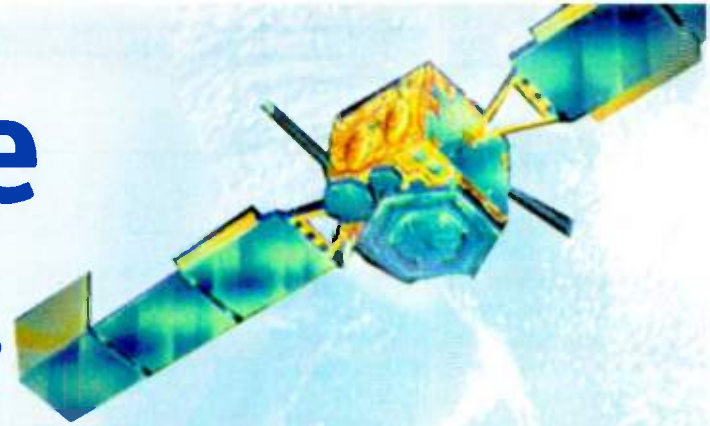

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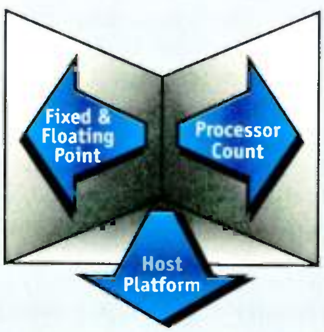

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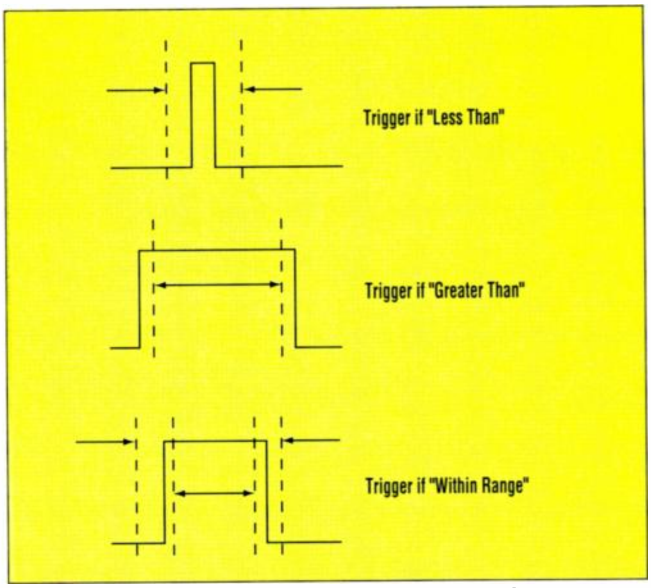
Pattern Triggering

The following examples illustrate how logic triggering can enhance the viewing of complex MCU-based signals on an oscilloscope. Figure 2 shows a diagram of Parallax's BASIC Stamp II, an embedded-control module based on a Microchip PIC16C57 8-bit microcontroller. Easily programmed, the BASIC Stamp is often designed into various industrial and consumer products. Like many designs based on 8- and 16-bit microcontrollers, the hardware is simple. The signals generated by these designs, however, are often complex. In the first example, the BASIC Stamp II was programmed to generate a series of repetitive signals representing a variety of real-world embedded-control signals.

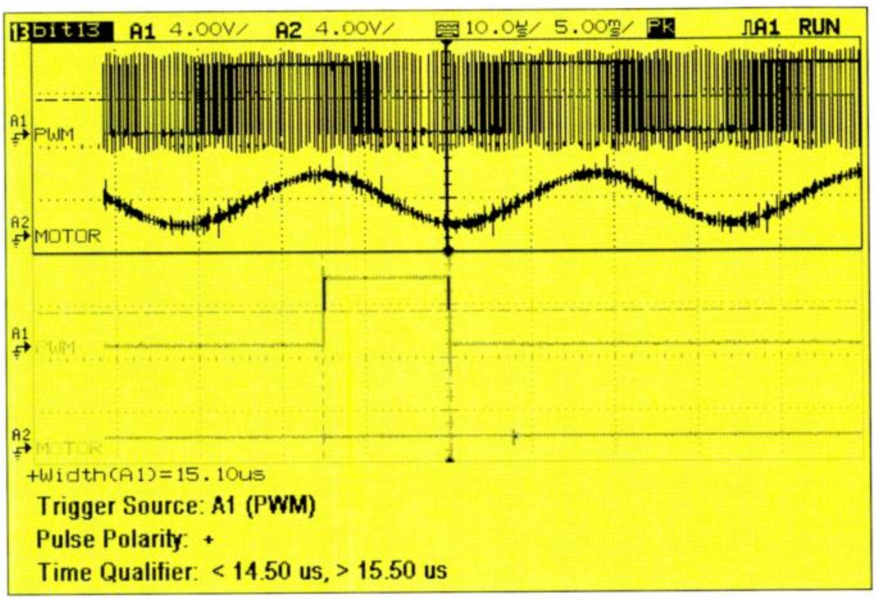
Figure 3 shows a repetitive capture—using an MSO—of 10 analog and digital I/O signals from the BASIC Stamp II MCU-based control module. The scope's two analog input channels (A1 and A2) captured a complex pulse-width-modulated (PWM) signal (top waveform) and an RC-filtered version of the same signal. The scope's logic inputs (0 through 7) acquired eight outputs from the MCU's RB0-RB7 I/O port. For this set of repetitive acquisitions, the oscilloscope was set up to trigger on a rising edge of channel 2 (the analog-filtered PWM signal). Note the multiple, phase-shifted images captured in this repetitive set of acquisitions. They're the result of not establishing unique trigger criteria based on the MCU's long, repetitive cycle time.



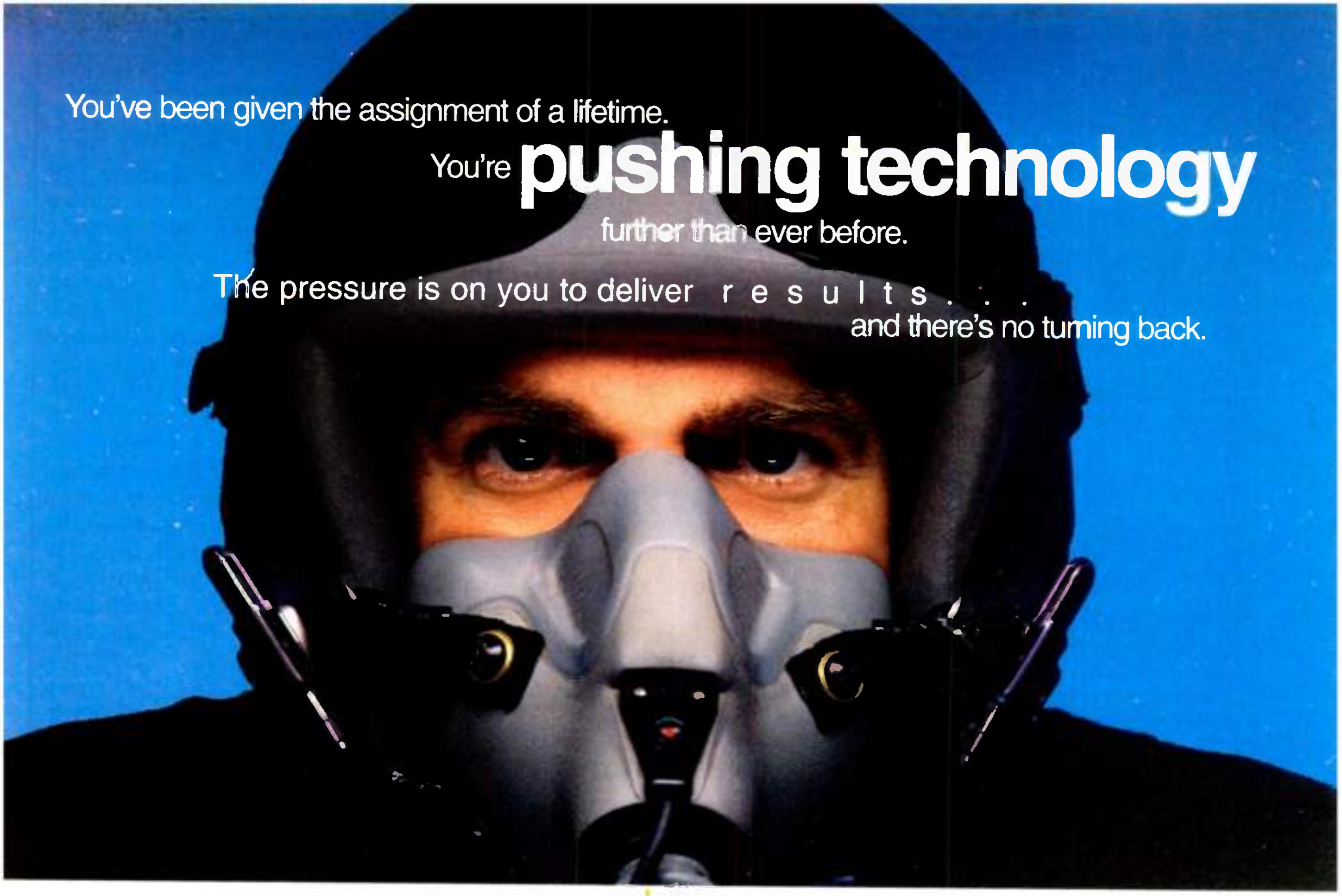
5. Shown above are three time-qualified trigger options for positive-going pulses only. The "Less Than" time qualifier is handy for finding narrow glitches, while the "Greater Than" time qualifier is good for locating and triggering on long dropouts or latched conditions. The "Within Range" time qualifier can be used to trigger on unique pulses within a serial pulse train.

With most dual-channel oscilloscopes that provide only *edge* triggering, an unstable display of complex waveforms, similar to the top two shown in Figure 3, is about the best one could expect to achieve. But, if the MCU's program cycle time is known, most scopes offer the possibility of locking onto the signal more precisely by using *trigger hold-off*. Adjusting the hold-off, however, is not easy to do.

A better solution is to synchronize the scope's triggering on a known output pattern of the MCU's I/O port. This pattern may represent a specific temperature reading or the speed (revolutions per second) of an induction motor controlled by the PWM output. Figure 4 shows the same 10 waveforms captured earlier. But this time, the display of repetitive acquisitions is stable. This is the result of triggering the scope on a unique pattern condition that occurs only once in each cycle of the MCU's program code. With the 0.00 seconds delay indicated in the figure, the default trigger position point is at center screen. The selected pattern specification was set to trigger when a "high" occurred on analog channel 1 (A1) at the same time that F1 (hex) occurred on the lower eight bits of the logic inputs. The remaining nine inputs were specified as "don't cares" (X). Note that the actual trigger condition is specified as highs (H) and lows (L), rather than in true



6. This is an example of triggering on a unique PWM pulse using the "Within Range" (less than/greater than) time qualifier. In this example, the scope was set up to trigger on a positive pulse of A1 if it occurred for greater than 14.50 µs but less than 15.50 µs. The scope found and triggered repetitively on a 15.10-µs wide pulse (shown expanded by the delayed time base in the lower portion of the scope's display).



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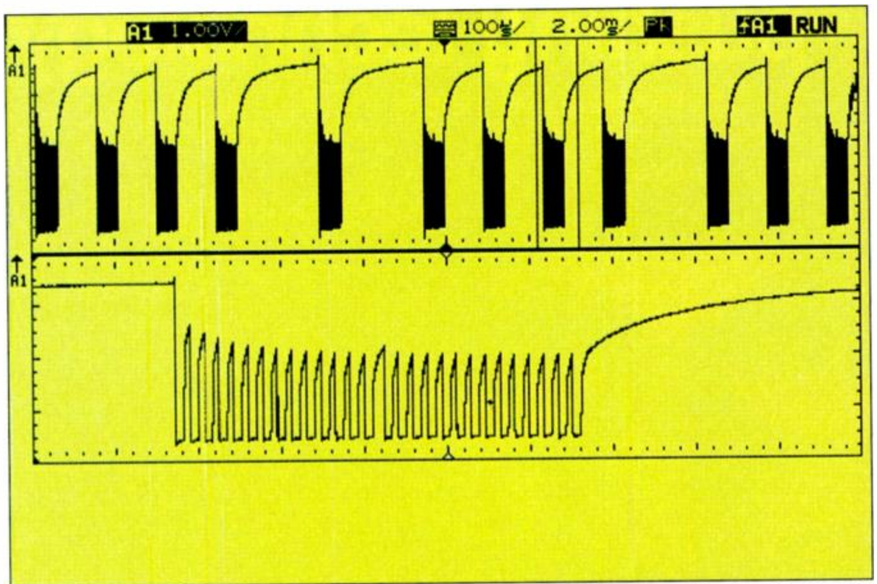

7. This screen shot shows a complex infrared (IR) signal generated from a microcontroller-based portable transmitter. Rather than trying to establish a complex condition to trigger on this signal, the deep memory acquisition of a scope can be used to capture the waveform. The delayed time base (lower waveform) can zoom in on various segments of the complex signal.

hexadecimal or binary (1s and 0s) format. As mentioned earlier, triggering on pattern conditions also is possible with many four-channel DSOs. But, a multiple-channel MSO provides even more flexibility in finding a specific word to trigger on, without the complexity of a logic analyzer.

Time-Qualified Triggering

Another alternative for triggering on complex signals of MCU-based systems is *time-qualified* triggering. Some scope manufacturers refer to this mode as *pulse-width* or *glitch* triggering. Whatever the name it's called by, the functionality is the same. Time-qualified triggering lets you set up the scope to trigger on a specific time duration of either a positive or negative pulse.

Figure 5 illustrates three time-qualified options for positive-going pulses only. The "Less Than" time qualifier can be handy for finding narrow glitches, hence the name—glitch triggering. For locating and triggering on long dropouts or latched conditions, the "Greater Than" time qualifier is the best bet. As for the "Within Range" time qualifier, it's advantage is that it can trigger on unique pulses within a serial pulse train.

MCU-based motor-control applications are good candidates for time-qualified triggering. The extremely noisy environment often found in motors makes triggering on an edge of an induction-motor drive signal almost impossible. The time-qualified triggering mode can establish a more stable trigger by synchronizing acquisition on a particular pulse of the PWM output signal. Plus, since each pulse of the PWM signal is phase-related to the ac-motor drive signal, this technique lets you synchronize the display on particular phases of the analog signal. (Note: The ac-motor drive signal is simply a low-pass, filtered version of the PWM pulse train.)

Triggering "Within Range"

The waveform display inFigure 6 shows an example of triggering on a unique PWM pulse using the "Within Range" (less than/greater than) time qualifier. In this example, the scope was set up to trigger on a positive pulse of channel A1 if it occurred for a duration greater than 14.50 µs but less than 15.50 µs.

The scope found and triggered repetitively on a 15.10 µs-wide pulse (shown expanded by the delayed time base in the lower portion of the scope's display). This pulse relates to a specific phase of the motor drive signal. As shown, using edge triggering on the ac-motor drive signal could have resulted in an unstable display because of the high level of noise picked up by the scope's A2 input.

What's next after exhausting all choices in attempting to establish a stable trigger point on a complex MCU-based signal? Perhaps the scope doesn't have a particular triggering feature, such as pattern or time-qualified triggering. Or, maybe the signals are too complex. There's another option. If the scope has sufficient acquisition memory, you can set up the instrument to capture a wide window of single-shot waveform information. Then, you can zoom in on any portion of the stored waveform. Since the waveform is stored, it will appear to be triggered. If the scope's memory is deep enough, effectively capturing "everything" from a single acquisition is possible.

Figure 7 exemplifies capturing a complex infrared (IR) signal generated from a microcontroller-based portable transmitter. Setting up a unique trigger condition to capture this signal is a difficult assignmentat best But, rather than trying to establish a complex condition to trigger on this signal, you may want to merely have the scope capture and display waveforms based on a simple edge-trigger condition.

However, this usually produces an unstable display. But all is not lost. To remedy this situation, merely scale the time base to ensure capturing a wide window. Then select the single-acquisition mode on your deep-memory scope to randomly digitize the complex signals. Once the signal is digitized, stored, and displayed on screen, it appears stable as seen in the figure. With the deep memory acquisition of this scope (1 Mbyte), the delayed time base (lower waveform) is used to zoom in on various segments of the complex IR signal. Again, the key to using this method of triggering—or, to be more exact, non-triggering—is sufficient acquisition memory.

Johnnie Hancock is a program manager for Hewlett-Packard's Electronic Measurements Division. He began his career with Hewlett-Packard in 1979 as an embedded hardware designer and holds a patent for digital oscilloscope triggering. Hancock graduated from the University of South Florida, Tampa, Fla., with a degree in electrical engineering.

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READER SERVICE 162

Circle 520

Extended Crystal Model For PSPICE Simulation

DETLEF GÖEHRIG, JÖRG HAFFELDER
TELE QUARZ Group, D-74924 Neckarbischofsheim, Germany;
phone: +49 7268/801-308; fax: +49 7268/1764.

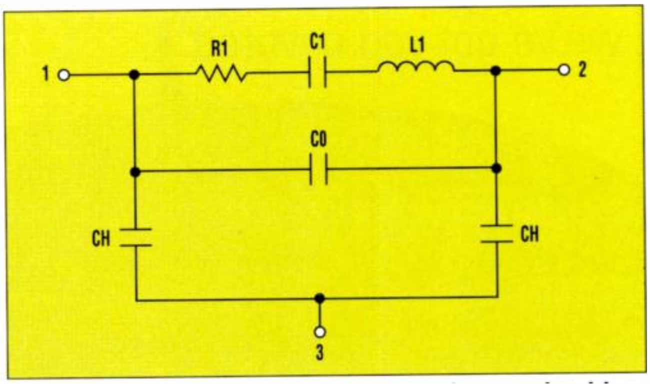
Certain limitations exist for modeling temperature-dependent crystal models when using standard Spice. The components typically used for quartz crystal models (resistor, inductor, and capacitor) only offer a quadratic temperature coefficient *(Fig. 1)*.

Also it's not possible to access the temperature as a global variable in original Spice. Therefore, modeling a crystal is possible only at one temperature.

Now, though, the temperature characteristic of the quartz crystal can be simulated by accessing the global variable temperature via ABM-sources in Pspice version 8.0. It's important to replace the inductor with an inductor model that uses controlled current and voltage sources. The value of the inductor can be replaced with a formula that directly accesses the global temperature variable, when using other simulation software such as ICAP/4. But, in Pspice simulations, it's necessary to take the roundabout method by using controlled sources to get there.

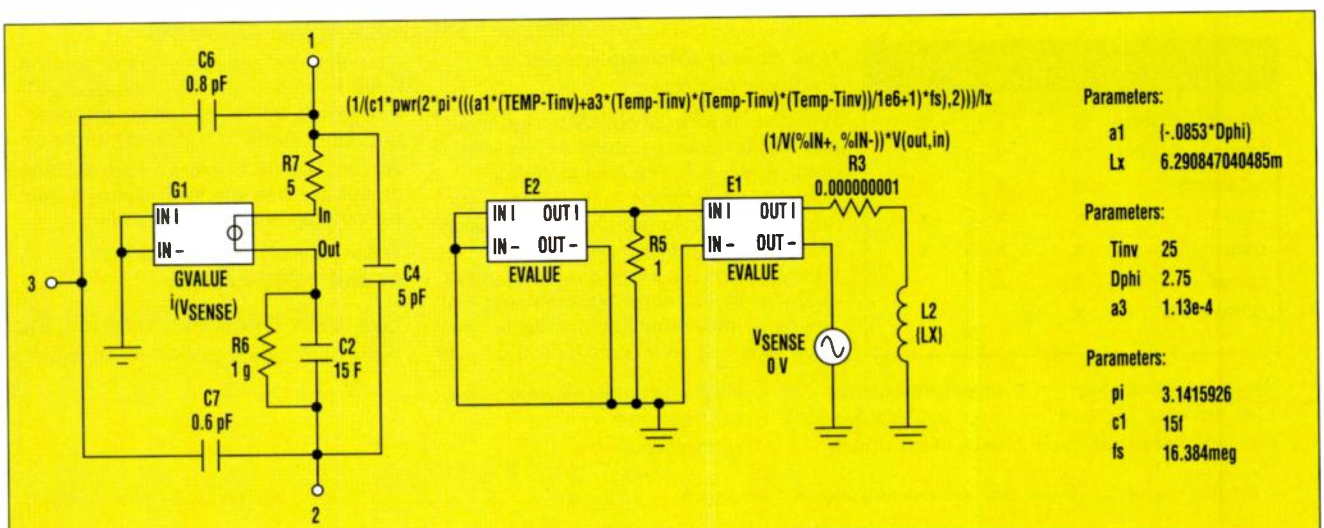
The temperature-independent Spice Model for a quartz crystal is given in Listing 1 below. This model represents the equivalent circuit of Figure 1. The frequency-determining element is the series-resonance circuit C1 and L1. Therefore, the temperature dependency of the frequency can be observed by changing the value of C1 and/or L1.

Every parameter of a crystal is usually temperature-dependent (crystal frequency, C0, C1, R1,...). The variation of C1 and C0 can be neglected for the simulation. The changes of a real crystal's series resistance R1 can't be described with a simple formula. Therefore, we assumed a temperature-independent R1 value for the model, and assumed that the value of C1 and C0 is constant over temperature. Consequently, the frequency variation over temperature is realized by a variation of the inductance value. Unfortunately, it's impossible to simply replace the inductance value by a formula that includes the global variable temperature. Thus, the entire inductor must be replaced by an ABM-source. This ABM-source allows use of the global variable



1. The components used in a typical quartz-equivalent crystal model only offer a quadratic temperature coefficient.

```
*******************************************************
* Frequency (nominal) fN: 16,384 MHz
* Load resonance = 30.00 pF
.subckt TQQuarz1 1 2 3
* TQQuarz1            : Specification
* 1 2                 : Connection leads
* 3                   : Case
*******************************************************
R1      1       10      5.0000000000000e+000
C1      11      2       2.0000000000000e+001fF
C0      1       2       4.6000000000000e+000pF
L1      10      1       1 LTOL 4.7208625264698e-003H
CH1     1       3       8.0000000000000e-001pF
CH2     3       2       8.0000000000000e-001pF
RH1     1       3       1.0000000000000e+011
RH2     3       2       1.0000000000000e+011
.model LTOL ind(L=1 dev=0.0020000000004%)
.ends TQQuarz1
```



2. Shown is the typical structure of an extended crystal model, which uses ABM sources to build the temperature coefficient.

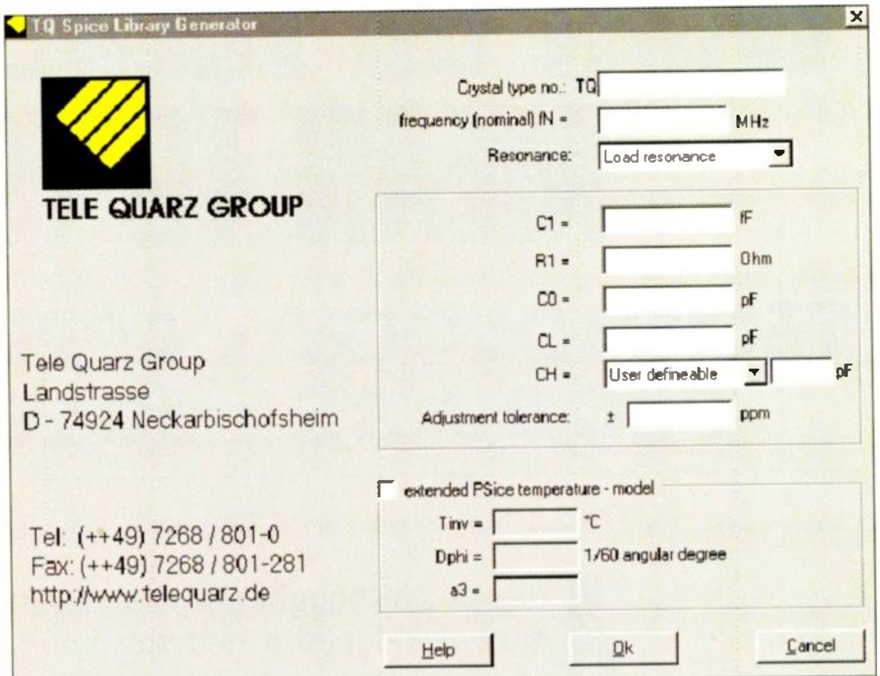
```
***********************************************************
* Frequency (nominal) fN: 16.384 MHz
* Load resonance = 39.00 pF
.subckt TQtest4 1 2 3
* TQtest4: Specification
* 1 2                    : Connection leads
* 3                      : Case
***********************************************************
.param c1=1.8000000000000e+001f
.param fs=1.6380587732963e+007
.param pi=3.14159265359
.param a3=1.1400000000000e-004
.param Dphi=2.7500000000000e+000
.param Tinv=2.9000000000000e+001
.param a1=(-0.0853*Dphi)
.param Lges=5.2445568559368e-003

R1    1    10   5.0000000000000e+000
C1    11   2    1.8000000000000e+001fF
C0    1    2    4.2000000000000e+000pF
R_C1  11   2    100G
***********************************************************
** Spulenersatz ABM Quellen
R7       0        21 1
L3       0        23 Ltol (Lges)
E_E5     21       0 VALUE {
+ (1/(c1*pwr(2*pi*(((a1*(Temp-Tinv)+a3*
+ (Temp-Tinv)*(Temp-Tinv)*
+ (Temp-Tinv))/1e6+1)*fs),2)))/Lges }
V_Vsense          24  0 DC 0V AC 0V
G_G3     11       10 VALUE { i(V_Vsense) }
R_R8     22       23 0.000000001
E_E6     22       24 VALUE { (1/V(21,0))*V(10,11) }
***********************************************************
CH1     1    3    1.6000000000000e+000pF
CH2     3    2    1.6000000000000e+000pF
RH1     1    3    1.0000000000000e+011
RH2     3    2    1.0000000000000e+011
.model LTOL ind(L=1 dev=0.0020000000004%)
.ends TQtest4
```

temperature in Pspice Version 8. Shown is the typical structure of a crystal model using ABM sources to build the temperature coefficient *(Fig. 2)*.

The inductor L1 has been replaced by the current source G3, which itself has a mirror function for the current through the reference inductor L3 at the operating point. The measured voltage V(out,in) is muitiplied with a factor to change the inductor's value. This factor, built using the voltage source E5, is a temperature-dependent function according to the cubic temperature behavior of the quartz crystal.

The library file for this crystal model has the following structure is shown in Listing 2 above. Tele Quarz offers a small program to simplify the construction of this model *(Fig. 3)*. This program generates the crystal model with the well-known equivalent circuit, including the effects of crystal parameters: frequency, load capacitance, C1, R1, and C0. As an option, this program also can generate the so-called "extended Pspice temperature model," including the temperature coefficient of the quartz crystal. This program can be downloaded from the Tele Quarz home page at *www.telequarz.de*.



3. Tele Quarz's QSlib Version 3 can generate more accurate, temperature-dependent models for quartz crystals. This program can be downloaded at *www.telequarz.de*.

Circle 521

Generate IIR Coefficients From Analog Filter Prototypes

FRANK N. VITALJIC
514 13th St., Bellingham, WA 98225.

The C source listing shown is a complete operating program that generates first and second-order IIR digital filter coefficients from analog filter prototypes. The program prompts users for all of the required parameter inputs, then it outputs the frequency-scaled analog prototype filter and IIR filter coefficients.

As an option, users can execute a prototype frequency prewarp or do straight frequency scaling. Note that the target frequency (TargetFreq) is the desired IIR corner frequency for low-pass/ high-pass filters, or the center frequency for bandpass/notch filters. Also, the prototype frequency (ProtoFreq) is the corresponding unscaled frequency.

Check your program with this third-order low pass:

$$H(s) = \frac{1}{1+S} \times \frac{1}{1+S+S*S}$$

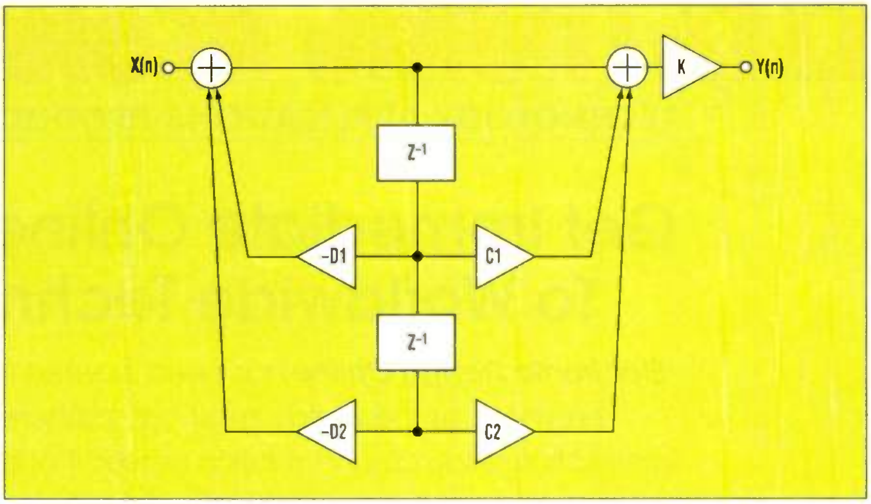
IIR FILTER

First Order	Second Order
C0 = 1.0	C0 = 1.0
C1 = 1.0	C1 = 2.0
D0 = 1.0	C2 = 1.0
D1 = -0.5095	D0 = 1.0
K = 0.2452	C0 = 1.2504
	D2 = 0.5457
	K = 0.0738

normalized ($W_C = 1$)

where TargetFreq = 100 Hz; ProtoFreq = 0.15915 Hz; and Prewarp = Yes.

See the figure for signal flow diagram conventions.



An IIR-digital filter biquad combines biquad sections in cascade to form high-order filters.

```
// C-source listing    calculates 1st and 2nd order IIR filter coefficients

#include <stdio.h>
#include <math.h>

// Global variables
        int FilterOrder;                        // Filter order, 1 or 2
        double Fs,                              // sampling frequency in Hz
                ProtoFreq,                      // Prototype filter frequency in Hz
                TargetFreq,                     // IIR filter target frequency in Hz
                A[3], B[3],                     // Prototype filter num, denom
                                                // coefficients
                C[3], D[3],                     // IIR filter num, denom
                                                // coefficients
                convMatrix[3][3]; // Filter conversion matrix

// Function definitions
void GetProtoCoefficients ( void )
{
        if (Filterorder == 1)       {           // Get prototype first order
                                                // coefficients
          puts( "\nEnter A0 A1 numerator coefficients: " );
          scanf( "%lf%lf", &A[0], &A[1] );
          puts( "\nEnter B0 B1 denominator coefficients: " );
          scanf("%lf%lf", &B[0], &B[1] );
        } else {                                // Get prototype second order
                                                // coefficients
          puts( "\nEnter A0 A1 A2 numerator coefficients: " );
          scanf( "%lf%lf%lf", &A[0], &A[1], &A[2] ) ;
          puts( "\nEnter B0 BI B2 denominator coefficients: " );
          scanf( "%lf%lf%lf", &B[0], &B[1], &B[2] );
        }
}       // end GetProtoCoefficients()

void GetFilterParameters ( void )
{
        puts( "\nEnter filter order [1 or 2]: " );
        scanf( "%d", &FilterOrder );
        puts( "\nEnter sampling frequency in Hertz: " );
        scanf( "%lf", &Fs);
        puts( "\nEnter prototype frequency in Hertz: " );
        scanf( "%lf", &ProtoFreq);
        puts( "\nEnter target frequency in Hertz: " );
        scanf( "%lf", &TargetFreq );
        GetProtoCoefficients();
}       // end GetFilterParameters()

void DefineConvMatrices ( void )
{
        if ( Filterorder == 1)      {           // First-order filter conversion
                                                // matrix
          ConvMatrix[0][0] = 0.5; ConvMatrix[0][1] =  Fs;
          ConvMatrix[1][0] = 0.5; ConvMatrix[1][1] = -Fs;
        } else  {                               // Second-order filter conversion
                                                // matrix
          ConvMatrix[0][0] = 0.25; ConvMatrix[0][1] = Fs / 2.0;
          ConvMatrix[0][2] = Fs * Fs; ConvMatrix[1][0] = 0.5;
          ConvMatrix[1][1] = 0.0;           ConvMatrix[1][2] = -2.0*Fs*Fs;
          ConvMatrix[2][0] = 0.25;          ConvMatrix[2][1] = -Fs / 2.0;
          ConvMatrix[2][2] = Fs * Fs;
        }
}       // end DefineConvMatrices()

void CalculateFilterCoefficients ( void )
{
        int             i, j;
        double          sum1, sum2;
        for ( i = 0 ; i < Filterorder+1 ; ++i ) {
          suml = 0.0; sum2 = 0.0;               // Reset accumulators
          for ( j = 0 ; j < Filterorder+1 ; ++j )  {
             sum1 += ConvMatrix[i][j] * A[j];
             sum2 += ConvMatrix[i][j] * B[j];
          }
          C[i] = sum1; D[i] = sum2;             // Assign IIR filter coefficients
        }
}       // end CalculateFilterCoefficients()

void PrewarpFilterCoefficients (void)
{
        double Cw;                              // Freq  prewarp coefficient
        Cw = Fs * tan(M_PI*TargetFreq/Fs) / (M_PI*ProtoFreq);
        A[1] /=Cw; A[2] /= Cw * Cw;             // Frequency scale
        B[1] /+Cw; B[2] /= Cw * Cw;             // coefficients.
}       // end PrewarpFilterCoefficients ()

void FreqScaleCoefficients ( void )
{
        double scale;
        scale = TargetFreq / ProtoFreq;         // Frequency scale factor
        A[1] /= scale; A[2] /= scale * scale;   // Frequency scale
        B[1] /= scale; B[2] /= scale * scale;   // coefficients.
        // end FreqScaleCoefficients()
}

void NormalizeCoefficients (void)
{
        double C1, C2, D1, D2, K;               // IIR filter coefficients
        C1 = C[1] / C[0]; C2 = C[2] /C[0];      // Numerator coefficients
        D1 = D[1] / D[0]; D2 =.D[2] / D[0];     // Denominator coefficients
        K = C[0] / D[0];                        // IIR filter multiplier
        printf("\n\nIIR FILTER COEFFICIENTS:");
        printf("\nC1,= %14.8lf    C2 = %14.8lf", C1, C2 );
        printf("\nD1 = %14.8lf    D2 = %14.8lf", D1, D2 );
        printf("\nK = %14.81f", K);
}       // end  NormalizeCoefficients()

void main (void)                                //Program begins here
{
        char ch;
        GetFilterParameters ();
        puts ( "\nFrequency prewarp filter coefficients (Y/N)?: ");
        ch = getche();
        if (ch == 'y' || ch == 'Y')
           PrewarpFilterCoefficients();
        else
           FreqScaleCoefficients();
        printf ("\n\nSCALED PROTOTYPE COEFFICIENTS:")
        printf ("\nA0 = %14.8lf  A1 = %14.8lf  A2 = %14.8lf",  A[0],A[1],A[2]);
        printf ("\nBC = %14.8lf  B1 = %14.8lf  B2 = %14.8lf",  B[0],B[1] B[2]);
        DefineConvMatrices();
        CalculateFilterCoefficients();
        NormalizeCoefficients();
        getch();                                // Pause
}       // end main()
```

Circle 522

Use Coil Impedance To Detect Position of Latching Relay

DR. ING. HARTMUT HENKEL
Von Hoerner & Sulger GmbH, Schlossplatz 8, D-68723 Schwetzingen, Germany; fax: +49 6202 24303; e-mail: 100327.1365@compuserve.com

Latching relays, which are switched back and forth by short current pulses applied to either of two relay coils, retain their last contact position after the coil is de-energized. Detecting the actual contact position typically requires an auxiliary contact. Many relays, such as high-voltage (HV) types, don't provide additional contacts for determining the position.

The circuit shown detects the actual contact position of a latching Kilovac HV-relay from the small difference between the inductances of the two relay coils (see the figure), which stems from the different magnetic paths inside the relay mechanism. The circuit produces a continuous output signal, valid shortly after the relay coils are de-energized, even after power (V_{CC} = +5 V) was interrupted.

Op amp OP1A generates a square wave (f ≈ 1 kHz), which pulses the two relay coils through diode D1 and resistors R1 and R2. The induced voltage peaks charge capacitors C1 and C2 through Schottky diodes D4 and D5. The voltage difference ΔV, mainly dc, is amplified by OP1B, which works as comparator. Finally, the LED signals the contact position. The output of OP1B, V_{OUT}, also can drive CMOS logic inputs.

D1, R3, and R4 protect the circuit against the nominal relay drive pulses (amplitude V_{DD} = 26 V) through transistors Q1 and Q2. Capacitors C1 and C2 are slowly discharged through resistors R7 and R8. Resistors R5 and R6, along with potentiometer P1, are used for offset adjustment, which corrects for the asymmetries of the relay coils and diodes D4 and D5. The setting of P1 is correct when the voltage ΔV is approximately symmetric around 0 V for the two contact positions (e.g., with the prototype after driving coil X, ΔV = +17.0 mV was measured, and ΔV = −17.1 mV after driving coil Y).

The bodies of diodes D4 and D5 should be in thermal contact to compensate for their thermal drifts. The circuit draws approximately 2.5 mA/8.8 mA (LED off/on). Since other relays might use different latching principles, experimenting and modified dimensioning of the circuit might be required.

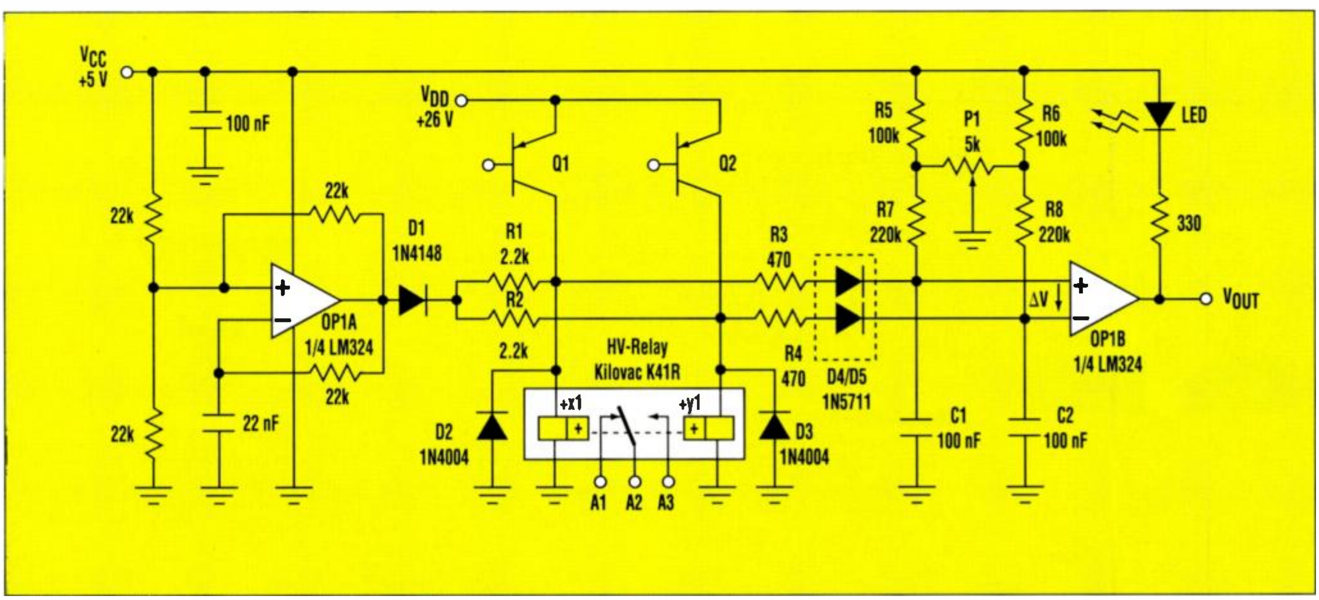
IFD WINNER

Mehrzad Koohian, Aura Systems, 2335 Alaska Ave., El Segundo, CA 90245; e-mail: mkoohian@aurasystems.com. The idea: *"Use Your Serial Port For Isolated Data Acquisition"*. September 15, 1997 Issue.

M. J. Salvati, Flushing Communications, 150-46 35th Avenue, Flushing, NY 11354; (718) 358-0932. The idea: *"LW/MW Converter For Ham-Only Receivers"*. October 23, 1997 Issue.

Fred Franke, Project Engineer, Cursor Control Corp., P.O. Box 808, Kings Park, NY 11754; (516) 265-4971,. The idea: *"Wattmeter Employs Switching -Regulator IC"*. November 3, 1997 Issue.

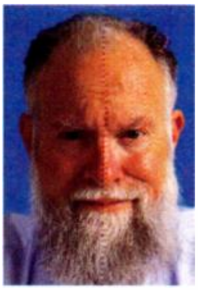
W. Stephen Woodward, Univ. of North Carolina, Venable Hall, CB3290, Chapel Hill, NC, 27599-3290; (919) 966-1358; e-mail: woodward@net.chem.unc.edu. The idea: *"Circuit-Break Locator For The Holidays"*. November 17, 1997 Issue.



This circuit detects the contact position of a latching relay from the small difference between the inductances of the two internal relay coils.

BOB PEASE

Bob's Mailbox



Dear Bob:

Your comments on waking up with a song in your head in your "Obsessions" column *(ELECTRONIC DESIGN, June 8, p. 179)* reminded me of another aspect of music in your head. Sometimes when I'm tinkering at home at my workbench, and I'm stuck trying to figure out a problem or a new piece of circuitry, I'll slide away from the bench and grab my guitar. I'll stumble through a few songs I know, or string together a few amusing cord changes, and then return to the bench. Often, I find this psychic dusting 'n cleaning gives me a new perspective and I can get to the solution I sought.

I believe the playing of music uses the other side of the brain than that used for the intellectual pursuits of electronic design. Maybe the making of music does for me some of what chanting one's mantra or doing yoga does for others. Too bad I can't bring a guitar to work.

BRAD ALBING
via e-mail

Okay, I'm going to go out and buy a guitar.—RAP

Hi, Bob:

Thank you for your clarity and levelheadedness regarding the speaker cable issue! The degree of deliberate disinformation on this topic, and the success with which it masks the established scientific facts, are truly frightening. I never would have thought it possible to deceive so many people so much of the time. The only scam that compares to this is the old "patent medicine" scam that was run on our grandparents. The universal claim was that, "MY product will cure anything that ails you." That scam ended when the U.S. Government stepped in and formed the Food and Drug Administration.

This High-End Audio Hysteria must settle down, or this industry will surely either self destruct or be brought under control. As things stand, the high-end audio industry is just begging for government intervention to stop the deceptive sales practices that go on every day in high-end audio salons. I can think of no other industry where such routine blatant technological deception is an everyday occurrence. It's time to put the scamsters on notice: Let the LIARS beware!

JOHN L. MURPHY
Physicist/Audio Engineer
True Audio
www.trueaudio.com

John, I would hate to think that anybody would ever catch me agreeing with a Republican. But, I don't want our STATE or FEDERAL government sending out more edicts on what people can or cannot do. If people catch on to the hoaxes of "ultra high-end audio" and learn to think for themselves, fine. If they figure out that nobody can hear the difference between super cables and inexpensive wire, fine. I have no objection to advice for consumers. But, forbidding such claims is not the American way. Laughing at them is!—RAP

All for now. / Comments invited!
RAP / Robert A. Pease / Engineer
rap@web team.nsc.com—or:

Address:
Mail Stop D2597A
National Semiconductor
P.O. Box 58090
Santa Clara, CA 95052-8090

Note: Back in the "Obsessions" column, I said I planned to pick up a heavy porter's load and stand up, using ONLY a tump line. I made up a load of 90.2 lbs. in two duffel bags and tied them all up. I stood up, unassisted, and carried it a couple hundred yards. I did it again at 88 lbs. So, it's not THAT hard. It's just a matter of know-how. By the time you read this, I'll already have tried this last month in Nepal: trekking to the base camp for Kangchenjunga at Pangpema, at 16,500 ft. I'll let you know how I made out. /rap

CDMA Baseband Cellular Chip Set Supports IS-95B Standard

The D5421 WorldCDMA chip set is an integrated baseband processor that supports the IS-95B specification for CDMA-based wireless handsets. The chip set combines an ARM7 RISC CPU integrated with an OAK DSP core, a CDMA digital ASIC, and an analog interface ASIC. It supports both 8- and 13-kbit/s QCELP, as well as EVRC vocoders. The chip set operates on 2.5 V and is housed in a 100-contact BGA. LG

***DSP Communications Inc.**, 20300 Stevens Creek Blvd., Cupertino, CA 95104; (408) 777-2700, fax (408) 777-2770, www.dspc.com.* **CIRCLE 553**

2.5-GHz Detector Makes RF Measurement And Control Easier

The AD8313 2.5-GHz RF detector simplifies the measurement and control of RF circuits by directly converting high-frequency modulated RF signal envelopes into accurate dc signals. The monolithic device offers a 65-dB dynamic range with an accuracy of ±1%. It receives a modulated RF input, then detects and amplifies it according to a linear approximation of a logarithmic function. The resulting dc signal represents the logarithm of the input signal envelope, which can be used to monitor or control signal levels in base stations, WLL systems, broadcast TV, cable, instrumentation, or avionics systems.

Packaged in a micro-SO8 housing, the AD8313 is available now. Pricing is $7.90 each in 1000-piece lots. LG

***Analog Devices Inc.**, Ray Stata Technology Center, 804 Woburn St., Wilmington, MA 01887; (781) 937-1428; fax (781) 821-4273; www.analog.com.* **CIRCLE 554**

Comm-Oriented RTOS Supports Lucent's DSP16000

The OSE real-time operating system (RTOS) and development tools provide full support for Lucent technologies' powerful DSP16000 family of digital signal processors and related cores. Designed to address the specific needs of the telecommunications industry, it makes it easier to manage and control complex, distributed DSP-based systems, such as wireless base stations. The OSE RTOS is integrated within Lucent's LUxWORKS development tools, which gives developers the ability to view a DSP's internal operation in real time and quickly correct system-level problems. Its message-based architecture allows easy upgrades and code swaps. The RTOS features diagnostic and correction functionality that lets it re-route signals, debug selected parts, and even swap out DSP chips without needing to power-down the system. LG

***Enea OSE Systems Inc.**, 5949 Cherry Ln., Suite 1710, Dallas, TX 75225; (214) 346-9339; fax (214) 346-9344; www.enea.com;e-mail: info@enea.com.* **CIRCLE 555**

Two-Part Baseband Chip Set Handles IS-136 TDMA

WorldTDMA D5204 is an IS-136A-compliant baseband processor chip set that offers a higher level of integration, lower power consumption, and lower overall system cost than previous generations. The two-chip D5204 set consists of a baseband engine chip (BEC) for performing core IS-136A voice processing, channel coding, modem and control functions, and an interface chip (IFC) with an integrated audio codec for interfacing to the RF/IF and audio sections of the subscriber unit. This highly compact solution is intended for cellular, PCS, and WLL applications. The D5204 features improvements in audio, proportional sidetone, transmit and receive filtering, and AFC resolution. The chip set operates at 2.7 V minimum. The BEC is available in a 100-pin TQFP or 121-pin BGA package, while the IFC comes in an 80-pin TQFP package. LG

***DSP Communications Inc.**, 20300 Stevens Creek Blvd., Suite 465, Cupertino, CA 95014; (408) 777-2700; fax (408) 777-2770; www.dspc.com.* **CIRCLE 556**

Versatile Silicon RF Amplifiers Cover 100-to-2000 MHz Range

The RF232x series of RF power amplifiers incorporate silicon bipolar junction process technology to deliver high performance and 3-V operation for applications ranging from 100 to 2000 MHz. They can be used as output stage drivers for ISM-band equipment, PCS power amp drivers, loop oscillator drivers, or buffer amplifiers.

The RF2321 offers +3-dBm output IP3, with 12 dB of gain at 900 and 1900 MHz. The RF2322 features high isolation (38 dB at 900 MHz) and a gain of 19 dB at 900 MHz. It is unconditionally stable and internally matched to 50 Ω. The RF2323's capacitative compensation extends its bandwidth and gives it a low noise figure of 2.3 dB. Gain ranges from 20 dB at 900 MHz, to 12 dB at 1900 MHz. The RF2325 provides +17 dB output IP3 ,and has an internally matched 50-Ω input and output. It's gain is 16 dB and 12 dB at 900 and 1900 MHz , respectively. The RF2326 also features internally matched input and output, plus a +17 dBm output IP3. Gain is 12 dB at 900 MHz and 10 dB at 1900 MHz.

The amplifiers are available now in SOT-23, 5-lead packages. Pricing is less than $0.60 each in 10,000-unit orders. LG

***RF Micro Devices Inc.**, 7625 Thorndike Rd., Greensboro, NC 27409; (336) 664-1233; www.rfmd.com; e-mail: afiney@rfmd.com.* **CIRCLE 557**

MMIC Mixer Includes LO and Amplifier

The MD57-0001 is a low-cost MMIC mixer with local oscillator (LO) and amplifier intended for use in cellular handsets. Its on-chip LO amplifier reduces the LO drive level to as low as –5 dBm, suiting it for power-conscious applications. The mixer is designed for functions such as frequency conversion and I/Q modulation in digital receivers and transmitters. High isolation between sections keeps the LO signal from feeding through to the RF port. The device is available now, and is housed in a SOT26 6-lead package. LG

***MA/COM Inc.**, 1011 Pawtucket Blvd., Lowell, MA 01853-3295; (800) 366-2266, (978) 442-5000, www.amp.com.* **CIRCLE 558**

High-Stability Frac-N Synths Cut Radio Cost, Boost Performance

With a high-frequency resolution of one part in eight million, the PS-xx00 family of fractional-N synthesizer ICs are designed as building blocks for the software-programmable radios of the future. The PS-xx00's level of resolution allows system designers to use a high reference frequency, which reduces phase noise. Because a higher reference frequency also allows for an in-

(continued on page 117)

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creased phase-locked-loop bandwidth frequency, a lower-cost voltage-controlled oscillator (VCO) can be selected.

The synthesizer's extreme accuracy permits the use of low-cost crystals to replace expensive temperature-compensated references. In addition, crystal temperature drift can be corrected in software. It also can perform direct digital modulation of the VCO, which eliminates the D/A modulator portion from the transmitter. Consequently, it offers considerable savings in cost and power.

Samples of 1.2-, 2.5- and 6.5-GHz versions of the PS-xx00 synthesizer will be available in the second quarter of 1999. Production is scheduled for the fourth quarter of 1999. In 10,000- piece quantities, pricing for the 1.2-and 2.5-GHz versions is $4.00. For the 6.5-GHz version, the 10,000-piece cost is $10.00. LG

***Philsar Electronics Inc.**, 81 Metcalfe St., 3rd Floor, Ottawa, Ontario, Canada K1P 6K7; (613) 567-4604; fax: (613) 567-5578; www.philsar.com.*
CIRCLE 559

Mixer/Downconverter Finds Homes In Cellular, PCS, Satcom

The TQ5M31 is a general-purpose mixer/downconverter that's been designed to work in a wide variety of wireless applications. These include mobile phone, CDPD, ISM, satcom, and WLAN data networks. The device integrates a buffered local oscillator input, a GaAs MESFET mixer, and an IF output amplifier. Its RF range of 500 to 2500 MHz and IF output range of 45 to 500 MHz allow it to support a most receiver frequency plans.

The RFIC has on-chip impedance control elements that require minimal off-chip matching. A small handful of other external components are used to adjust buffer LO frequency response and IF gain response for a particular application. The TQ5M31 displays a typical conversion gain of 2.0 to 3.5 dB, and a third-order intercept point of 9.0 dB with a 9.5 dB noise figure.

Housed in a 6-pin SOT-23 package, the TQ5M31 is available now. Pricing is $2.08 each in 1000-piece quantities. LG

***TriQuint Semiconductor Inc.**, 2300 N.E. Brookwood Pkwy., Hillsboro, OR 97124; (503) 615-9000; fax (503) 615-8900; www.triquint.com.* **CIRCLE 560**

Upconverter Mixers Run From 400 MHz To 2.5 GHz

Designed for applications in 400-MHz, 900-MHz, and 2.5-GHz ISM-bands, the MAX266x and MAX267x series of upconverter mixers offer excellent linearity and modest power consumption. Applications include handheld radios, wireless LANs, PCS systems, cellular phones, and cordless phones. The device's typical third-order intercept points are 9.6 dBm at 11.8 mA and 11 dB of gain. Power consumption is nearly constant over the part's 2.7- to 5.5-V operating range.

The MAX2660, 2661, 2663, and 2671 are available in 6-pin SOT-23 packages. The MAX 2673 incorporates a balanced IF port and is housed in an 8-pin µMAX package. Pricing for the mixers starts at $0.76 each in 1000-piece quantities. LG

***Maxim Integrated Products**, 120 San Gabriel Dr., Sunnyvale, CA 94806; (800) 998-8800 or (408) 737-7600, ext. 6087; www.maxim-ic.com.* **CIRCLE 561**

Integrated RF Transceivers Support IS-136, GSM

Two single-chip RF transceivers are now available for use in digital cellular handsets based on the IS-136 and GSM TDMA air interface standards. The µPC8011 and µPC8013 support the IS-136 and GSM standards, respectively. They combine receiver, transmitter, and synthesizer functions on one chip. Included on-chip is control logic, a frequency synthesizer, pre-scalers, and I/O buffers. Analog circuitry provided by the transceivers includes elements such as filter networks, a power amplifier, and a duplexer. All of these features help save space, power, and cost over discrete solutions.

Operating from a 2.7- to 3.6-V supply, typical power consumption is 107 mA in receive mode. Standby power consumption is around 30 mA. An evaluation board is available for both parts.

Available now, the µPC8013 and µPC8011 are housed in a 100-pin TQFP. Pricing is under $5.00 each in quantities of 100,000. LG

***NEC Electronics Inc.**, 2880 Scott Blvd., P.O. Box 58062, Santa Clara, CA 95052-8062; (800) 366-9782 or (408) 588-6000; fax (800) 729-9288; www.nec.com.* **CIRCLE 562**

Dual FibreChanel Card Speeds On RACEway

Marrying FibreChannel as a data-transfer link to the RACEway system architecture gets you a very powerful throughput capability. The Myriad Logic model FC-2930/R is a high-performance dual Fibre Channel (FC) adapter for Mercury Computer Systems' 9U RACEway systems. Optimized for real-time applications requiring high bandwidth and low latency, the FC-2930/R provides two fully programmable, ANSI-compliant Fibre Channel ports. Each are capable of sustained 90-Mbyte/s data transfer.

The FC-2930/R is compatible with FibreChannel Class 1 and 2 operation and is designed to connect Mercury compute nodes, RAIDs, general-purpose computers, or other real-time systems in arbitrated loop, point-to-point, or switched topologies.

The FC-2930/R uses two 1.063-Gbit/s fiber-optic modules to implement FC layer 0. The modules are replaceable, allowing the FC-2930/R to be configured for operation with multimode fiber or single-mode fiber.

Two Hewlett-Packard Tachyon FibreChannel controllers are used to implement FibreChannel. The FC-2930/R incorporates two full-featured RACEway interfaces that are used for data transfer between the Fibre Channel ports and compute node memory, as well as control. An on-board processor controls all aspects of the FC-2930R's operation, including commanding of both Tachyon Fibre Channel controllers, FIFO buffer management, and initiating and monitoring direct memory access of data to and from RACEway memory. The processor operates from an EPROM-based program that supports both a standard and application-specific operation. JC

***Myriad Logic Inc.**, 1109 Spring St., Silver Spring, MD 20910; (301) 588-1900; fax (301) 588-0605; Internet: www.myriadlogic.com.* **CIRCLE 525**

233-MHz Pentium Single-Board Computer Supports MMX

The MMX instruction set in today's Pentium processors provides a great solution for embedded applications like vision systems and medical imaging. The PCps233, a single-board computer series containing Intel's 430HX chip set, Pentium MMX processor, PCI performance, and a host of other on-board high-performance peripherals, sets new trends in the embedded industry. The SBC, which integrates 512 Mbytes of error checking and correction (ECC) DRAM and 512 kbytes of burst cache, protects data integrity and achieves high reliability for demanding and high-performance applications.

In addition, the PCps233 features on-board 10/100Base-T Ethernet Adapter, UltraWide SCSI with data transfers of up to 40 Mbytes/s, SVGA with simultaneous CRT and flat panel displays. The board has dual high-performance PCI bus EIDE interfaces, two floppy-drive interfaces, two Universal Serial Bus (USB) ports, up to 8 Mbits of bootable flash disk, two 16C550 serial ports, a bidirectional PC/AT parallel port, a watchdog timer, independent temperature monitoring system for the CPU, PCI-to-PCI bridge support, and backward compatibility with the existing ISA and PCI specifications.

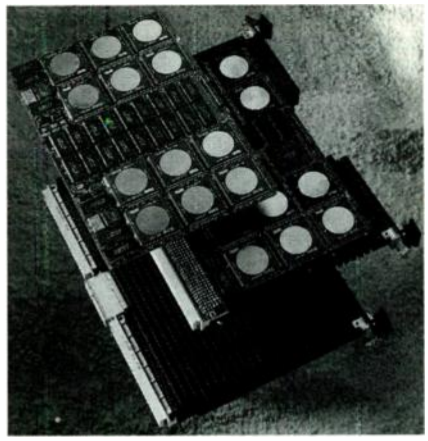
Available now, the PCps233 has a list price of $ 1430. JC

***Industrial CPU Systems Inc.**, 111 D.W. Dyer Rd, Santa Ana, CA 92707; (714) 957-2815; fax: (714) 957-3128; www.icpu.com.* **CIRCLE 526**

Boards Pack 24 SHARCs In A VME Slot

When high-performance real-time processing is required, the more digital signal processors on board the merrier. Providing up to 24 SHARC DSPs in a motherboard and daughterboard format, the Vantegra board is capable of yielding up to 2.88 GFLOPS performance in a single 6U VME slot. It complies with either IEEE 1101.2 Conduction Cooled or Air Cooled formats.

The board design exploits the full potential of Analog Devices' SHARC DSP by using clusters of six ADSP-2106x devices, each with local SRAM and flash memory, as the system's basic building block. This architecture eases and accelerates software development by providing symmetrical compute segments. As a result, resource allocation becomes simple and easily scaled over multiple clusters and board sets.



Each cluster of six SHARCs provides six link ports to give up to 240-Mbyte/s data transfers between the adjacent cluster of SHARCs on the same board. Each cluster on the board then provides a further six link ports for the motherboard/daughterboard interconnection.

Similarly, up to 24 link ports (six per cluster) are available at the front, providing interconnection of multiple boards and giving an aggregate transfer rate of up to 480 Mbytes/s peak between multiple boards. A number of link ports are available at the P2 connector for the purpose of multiple board interconnection or data acquisition. Pricing for the Vantegra starts at $11,495 for the 12 SHARC variant. JC

***Radstone Technology Corp.**, 50 Craig Road, Montvale, NJ 07645; (800) 368-2738; fax (201) 391-2899; Internet: www.radstone.com.* **CIRCLE 527**

CompactPCI SBC Supports Socket-7 Microprocessors

Harsh industrial environments need the ruggedness of Compact PCI combined with the convenience of the familiar Socket-7 PC architecture. The new PEP CP312 is a complete PC on a single 3U format board. It can be used as a standalone single board computer, or as the CPU in a CompactPCI system. The CP312 can accommodate all current Socket-7 microprocessors, including low-power versions and those with clock rates in excess of 300 MHz.

It features built-in numeric coprocessor support, and a SiS 5598 Pentium system controller. The SiS 5598 provides all of the latest system controls, including level-2 write-back

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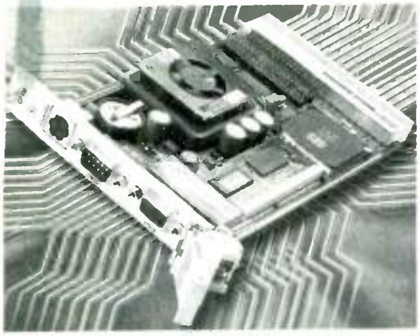
cache controller, burst DRAM controller, PCI/ISA interface, and more.

Various memory options are offered to match customers' system requirements, including 32- or 64-Mbyte



on-board RAM with the expansion capability of 64 Mbytes of EDO or SDRAM on a small-outline DIMM module. The CP312 also contains 64-kbyte internal CPU cache and 512-kbyte burst-SRAM pipelined L2 expansion cache.

The CP312 has high-performance SVGA video support, and an embedded 64-bit GUI accelerator is provided along with two Enhanced IDE interfaces and a floppy-disk interface supporting two drives.

The board is designed so that the microprocessor can be kept within its operating temperature range with just a passive heat sink. Thus, the board is a natural choice for harsh environment industrial applications with operating temperatures ranging from 0° to 60°C. The 8HP version enables operations at temperatures up to 75°C. Pricing for PEP's CP312 starts at $1789. JC

***PEP Modular Computers Inc.**, 750 Holiday Dr., Bldg. 9, Pittsburgh, PA 15220; (412) 921-3322; fax (412) 921-3356; www.pep.de.* **CIRCLE 528**

EBX SBC Runs At 300 MHz And Features Industrial I/O

Non-backplane embedded applications are embracing the EBX embedded motherboard form factor. VersaLogic Corp. offers a new Pentium MMX-class single board computer that mixes performance and a complete I/O offering. The EBX-compliant board includes PCI-based video, flat-panel BIOS support, 10Base-T Ethernet, PCI 104-Plus expansion, and USB interface.

In addition, the board includes a full complement of on-board industrial features, such as eight 12-bit analog channels, two RS-422/485 COM ports (plus two standard RS-232 COM ports), and three extra counter-timers. For high reliability applications, the board includes ECC circuitry that will detect and correct one-bit memory errors on the fly, as well as a watchdog timer with true hardware reset capability.

The VSBC-6 accepts all Socket-7 processors up to 300-MHz K6 and 233-MHz Pentium. The board will be initially available in 200-MHz (K6), 233-MHz (Pentium), and 300-MHz (K6) speeds.

Memory options include 8- to 128-Mbyte EDO or true error correcting SDRAM, 2- to 72-Mbyte DiskOnChip flash disk, 512 kbytes of battery-backed SRAM, and 256-kbyte level 2 cache. It's all provided in a single 8- by 5.75- by 2-in. board.

The VSBC-6 with a 200-MHz K6 CPU is priced at $793 in 100-unit quantities. Customized versions also are available. JC

***VersaLogic Corp.**, 3888 Stewart Rd, Eugene, OR 97402; (800) 824-3163; fax (541) 485-5712; Internet: www.versalogic.com.* **CIRCLE 529**

Slot 2 Motherboard Sports Dual Xeons

PC processors are no longer considered a performance tradeoff. Exemplyfing this shift, the Thunder X is a dual Slot 2 motherboard that supports two Intel Pentium II Xeon processors. The new board is designed in a standard ATX form factor identical to Intel's Marlinspike Slot 2 motherboard.

The Thunder X is designed for maximum expendability with five 32-bit PCI Bus Master slots, one shared ISA Slot, and one AGP slot. The board features a built-in twin-channel Ultra2 Wide SCSI controller (Adaptec AIC7896) with LVD support, as well as two UDMA/33 IDE ports.

Based on the Intel 440GX AGPset, the Thunder X also is Tyan's first motherboard to support up to 2 Gbytes of PC/100 SDRAM. Combined with the Pentium II Xeon's full speed level 2 cache, this will give memory performance at RISC workstation levels. Other features include Super I/O support; AMI Plug 'n' Play BIOS; and advanced system management features such as LM81 sensor chips with on-board alarm to monitor fans, temperature, and voltage levels. Intel's LANDesk Client Manager software also is included.

Available now, the OEM pricing for Thunder X in 1000-piece quantities is below $600. JC

***Tyan Computer Corp.**, 3288 Laurelview Court, Fremont, CA, 94538; (510) 651-8868; fax (510) 651-7688; www.tyan.com.* **CIRCLE 530**

Penitum II Compact PCI Uses Mobile Modules

Demand for high-performance embedded computing is skyrocketing, particularly in applications such as telecomm, computer telephony, and high-end industrial control. Motorola Computer Group seeks to capitalize on this trend with first CompactPCI single-board computer sporting Intel's recently announced "Pentium" II processor mobile module. Unlike the awkward packaging of the desktop Pentium II, these mobiles fit flat on the board, enabling the CPV5300 to take up just two Compact PCI slots.

Called the CPV5300, the board incorporates a 233- or 266-MHz Pentium II processor, 512-kbyte L2 cache, the high-performance 440BX chip set, and up to 512 Mbytes of DIMM memory. The board includes an Ultra-SCSI interface, AGP video featuring the i740 graphics accelerator with 8-Mbyte video memory, and optional on-board flash, floppy, and hard drives.

Also included are dual 10/100-Mbit 82559 Ethernet controllers with Alert-On-Lan technology and network heartbeat and system monitoring of voltages, temperature, airflow, and chassis status. Standard on-board PC peripherals include dual serial ports; dual enhanced-IDE ports; and parallel, keyboard, mouse, and floppy interfaces. All I/O is available through both the front panel and rear J4/J5 connectors.

CPV5300 is priced beginning at $2395, with samples available in August 1998.

***Motorola Computer Group**, 2900 South Diablo Way, Tempe, AZ 85282; (800) 759-1107; Internet: www.mot.com/computer.* **CIRCLE 531**

(continued from page 118)
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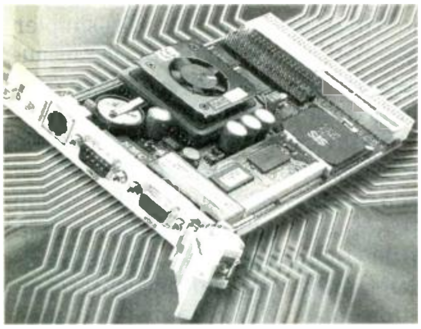

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CPV5300 is priced beginning at $2395, with samples available in August 1998.

Motorola Computer Group, 2900 South Diablo Way, Tempe, AZ 85282; (800) 759-1107; Internet: www.mot.com/computer. **CIRCLE 531**

Enhanced ARM Core Offers Throughput Of 400-Dhrystone 2.1 MIPS

Targeted to deliver over 400-Dhrystone 2.1 MIPS when clocked at 300 MHz, the ARM10TDMI core will be backwards-binary-compatible with the ARM7TDMI processor core. An enhanced on-chip AMBA (ARM multimaster bus architecture) intermodule bus makes it easy to attach coprocessors and other functional enhancements to the processor core.

The ARM10TDMI core also is the first core to implement the new ARMv5T instruction-set architecture. It is a superset of the ARMv4 ISA implemented by the StrongARM, the ARMv4T ISA implemented by the ARM Thumb family, and the ARM9 Thumb family processors.

The core, which is capable of parallel instruction execution, includes branch prediction and the ability to continue executing in the presence of a cache miss. As a result, the processor can achieve high performance on real applications. A second version of the core, the ARM1020T adds 32-kbyte instruction and data caches, a memory-management unit with demand-paged virtual memory support, and a write buffer to the basic ARM10TDMI core.

To address the high-computational-throughput requirements of applications such as 3D graphics and floating-point DSP algorithms, there's an optional vector floating-point coprocessor that can be integrated with the core. The VFP10 coprocessor performs single- and double-precision floating-point computations by adopting a RISC approach. Here, simple common operations that can be executed in parallel are implemented. A seven-stage ALU pipeline and five-stage load/store pipeline provide the vector unit with its parallel-execution capability. Thus, the unit can deliver a throughput of 600 MFLOPS (peak), when clocked at 300 MHz.

Expected to be ready for evaluation in the first quarter of 1999, the ARM10 cores can be licensed from ARM or will be available through ASIC suppliers that will, in turn, have licensed the core from ARM. Typical licensing arrangements include a base fee and royalty arrangements, which are negotiated on a company-by-company basis.

ARM Inc.
985 University Ave., Ste. 5
Los Gatos, CA 95032
Reynette Au, (408) 399-4635
www.arm.com
CIRCLE 532
DAVE BURSKY

Flash-Based Microcontrollers Provide Memory Migration Options

A pair of 8-bit microcontrollers—the PIC16F877 and 16F876—both pack 8 kwords (14 bits/word) of electrically reprogrammable flash memory, yet offer an operating voltage range that spans 2.0 to 5.5 V. This suits the chips for a wide range of programmable and battery-powered applications. The flash-based parts also are also socket-compatible with ROM and OTP versions of the same microcontrollers. Designers can therefore start with the flash device and transition to the OTP or ROM-based devices when system volumes require a lower-cost solution.

The microcontrollers also include a 5-to-8-channel, 10-bit, ±1 LSB analog-to-digital converter, an RS-485-type UART for multidrop data-acquisition applications, I_2C or SPI communications capability for peripheral expansion, and two 8-bit timers and one 16-bit timer. When clocked at 20 MHz, the controller can deliver a throughput of about 5 MIPS. Precision timing interfaces are accommodated through two CCP (capture and compare processor) modules. Capture can be done with an accuracy of 12.5 ns with 16-bit resolution, compares with 200-ns maximum accuracy and 16-bit resolution, and pulse-width modulation at 20 kHz with accuracies to within 10-bit resolution.

The flash-memory block on the chips can handle 1 million erase/write cycles, thus delivering the highest endurance for any flash-based MCU in the industry. Also included on the MCUs is the company's in-circuit serial programming interface. This allows the microcontroller to be programmed after being mounted on the target system board, which reduces the cost of system field upgrades, and provides simpler system calibration setup during manufacturing. Just two pins are required for the programming interface.

Future family members will include from 512 to 8k words of flash program memory, from 36 to 368 bytes of on-chip SRAM-based data storage, and from 16 to 256 bytes of byte-alterable EEPROM. Additional chip functions will include options like 10-bit, 12-channel ADCs; capture, compare, and PWM functions; and I_2C, SPI, and a high-performance USART communications interface. The 28-pin PIC16F876 sells for $7.97 apiece in lots of 1000 units, while the higher I/O count 40-pin 16F877 goes for $8.57 each, also in 1000s.

Microchip Technology Inc.
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
(602) 786-7668
www.microchip.com
CIRCLE 533
DAVE BURSKY

PLL-Based Clock Circuit Generates Timing for DVDs

The PLL1700, a phase-locked-loop timing generator, provides the multiple clock signals required in DVD systems to synchronize audio and video clocks. A 27-MHz master MPEG-2 clock signal is used by the chip to derive all system clocks that control the surroundsound AC-3 decoder, the digital signal processor, and the digital-to-analog converters. Based on an analog PLL that has a clock jitter of less than 150 ps and a zero PPM error, the chip delivers clock outputs that are perfectly accurate. The PLL1700 can interface to 3.3-V logic, operates from dual supplies (+5 and +3.3 V) for maximum stability, and typically dissipates about 75 mW. Housed in a 20-lead shrink small-outline surface-mount package, the chip sells for $1.95 each in 1000-unit lots. Delivery is from stock.DB

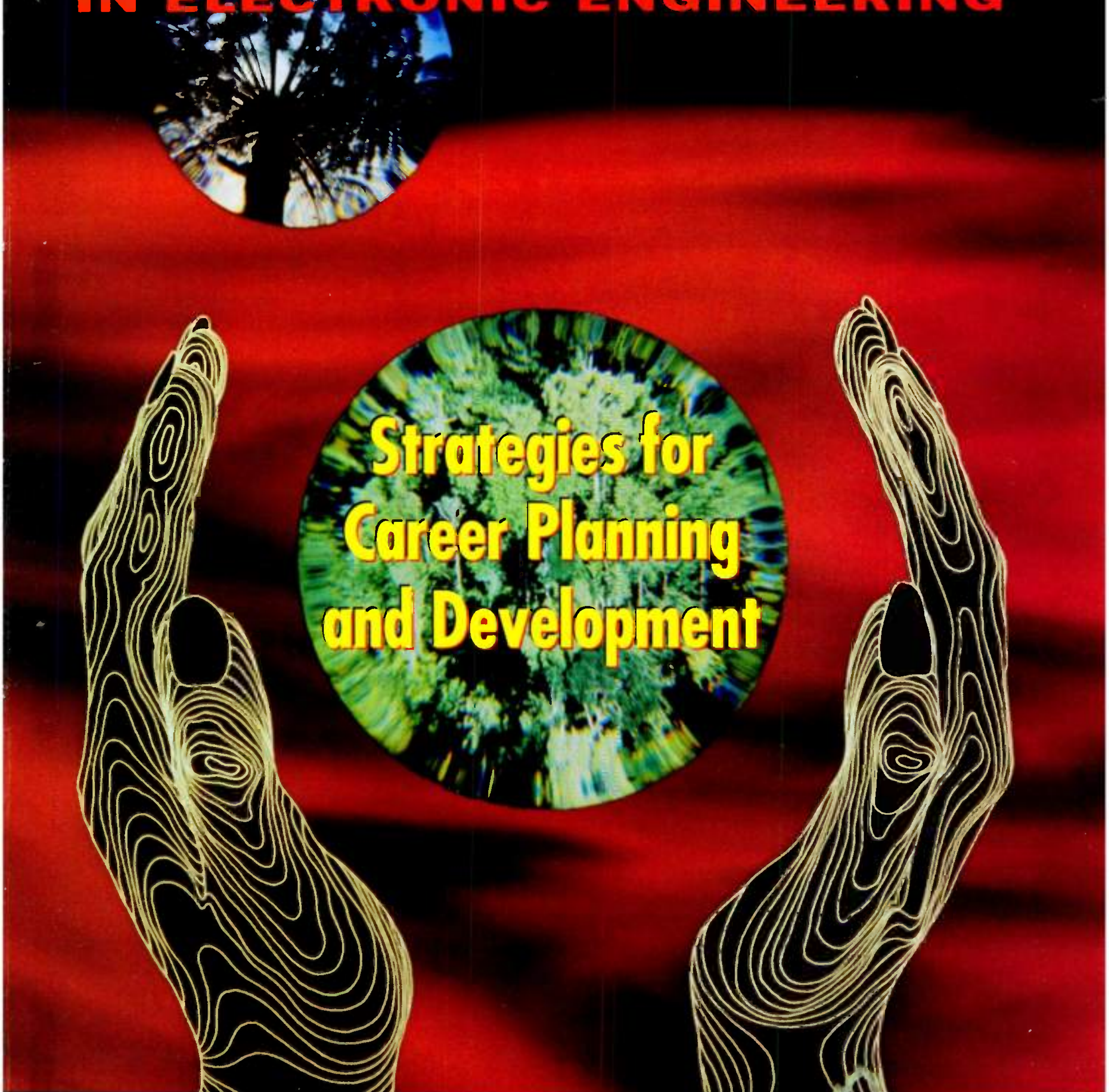
***Burr-Brown Corp.**, 6730 S. Tucson Blvd., Tucson, AZ 85706; (520) 746-1111; www.burr-brown.com.*
CIRCLE 534

A Penton Publication

November 1998

CAREER OPPORTUNITIES

IN ELECTRONIC ENGINEERING



Strategies for Career Planning and Development

A Special Career Supplement to Penton Publications

WIRELESS SYSTEMS DESIGN

ELECTRONIC DESIGN

Microwaves & RF

ONLINE SURVEYS SHOW THE KEYS TO SUCCESS

STYLE, PERFORMANCE INCENTIVE, AND COMMUNICATION ARE KEY TO MANAGEMENT SUCCESS.

DEBRA SCHIFF

The process of gaining access to information has greatly changed with the advent of the World Wide Web. When companies want to find out things quickly, they just jump on their T1 lines and ride the waves of facts that come streaming at them through their search engines. Other companies are using the web to reach out and communicate with their customers or even their competitors (the "true" competitor is gone anyway, with all of the licensing and partnering that's been going on in the last few years). Either way, the online process is ever-present, and being used to gain a broader look at all kinds of data.

One example of using the web to obtain perspective-shaping information is Paul-Tittle Associates' recent online survey of over 1500 high-technology professionals, a continuation of an online survey done early last year. Paul-Tittle Associates is an executive search and large-scale recruiting firm serving the information technology (IT), telecommunications, and electronic commerce industries.

Paul-Tittle Associates decided to perform the surveys online rather than on paper because the old-fashioned way would have required many more resources and much more time to compile. Using online "live" tallying software, the company was able to automatically sort and statistically analyze their results as the survey participants logged their entries.

The first survey discusses compensation, career paths, job retention, start-up companies, and where the high-tech jobs are. As far as compensation goes, nearly 90% of the executives who responded to the survey said that their salaries were $50,000 or higher. About 54% said that they earned over $75,000, and 25% reported that annual wages were $100,000 or more (*Fig. 1*).

As far as their raises go, a third of the respondents said they only expect to receive a base salary increase of 5% or less in the next year in their current positions. Two-thirds of the survey's participants expect less than a 10% raise, but if they moved to another company, four in 10 of the respondents predicted that they would receive a pay increase up to 25%.

The message here is that the fastest way to receive a pay increase is to move to another job at another company. The survey proves this point by questioning participants as to how long they've been at their current positions. Over a third of the respondents have only been in their current position for less than a year. Over two-thirds of those polled are in their position for two years or less (*Fig. 2*).

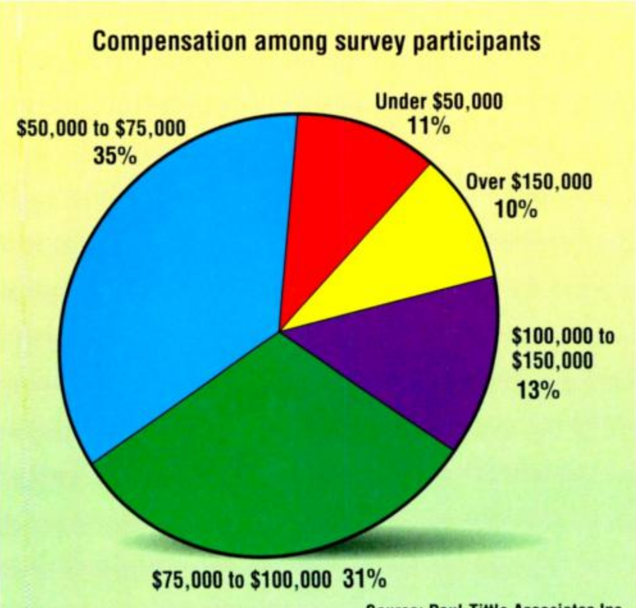


Fig. 1

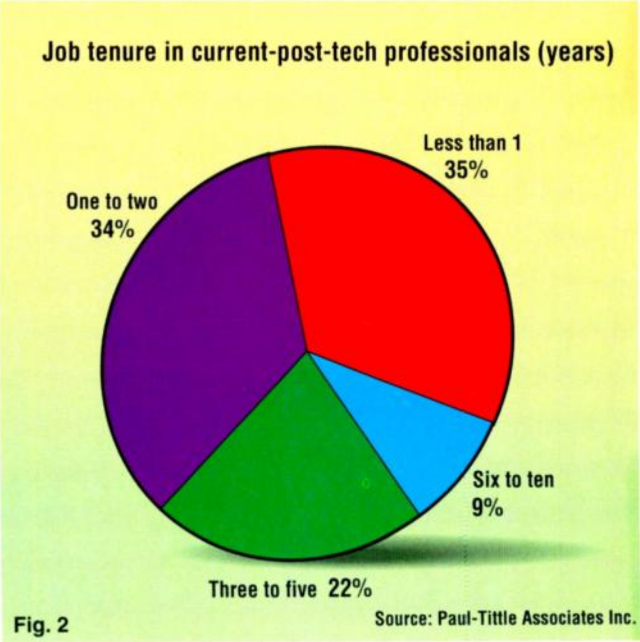


Fig. 2

What managers have to look at is that it's a "buyer's market." Basically, high-tech jobs can be bought by the highest bidder. The survey shows that 87% of those asked are receptive to performance-based compensation, so these individuals are willing to work hard for their compensation.

What makes companies attractive to potential hires comes down to three points, according to the study: a dynamic work environment, potential to advance, and commitment to being an industry leader. Of course, increased compensation and stock ownership are high on the list as well. Joining a start-up company appealed to some study participants because it gives them the "chance to build something," and the "ability to participate in a company's growth."

Wrapping up the first study, Paul-Tittle Associates asked participants which U.S. cities ranked highest for high-tech jobs. These individuals listed Washington, D.C., and San Francisco, Calif., at the head of the list, with Atlanta, Ga., third. To put this information into perspective, half of the study's respondents are located within the Mid-Atlantic region. The draw to Washington, D.C., for high-tech jobs is driven by the large telecommunications companies and the defense spin-offs located in the area.

The second online study, which focused on management skills, included participants who were mainly (75%) middle- or senior-level professionals. Of surveyed, 10% sit at the executive level. What the company was looking for in this survey was the impression people have of their managers.

Of course, good management is crucial to a company's success; 90% of those surveyed said so. And, 65% said the companies they work for aren't making use of all of their resources, including their managers.

What makes a great manager? In fact, what makes what 82% of those surveyed said an "outstanding manager?" Individual management style should encompass the "willingness to give staff the freedom and resources to accomplish its mission," say 43% of the respondents. Second at 15% was "the ability to motivate people." Unpopular choices were "emphasis on sharing success with others," "an in-depth understanding of the business,"

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"The engineers that we're placing are with offshore companies," he says. "They see a slowdown like this as an opportunity where they can expand their capacity."

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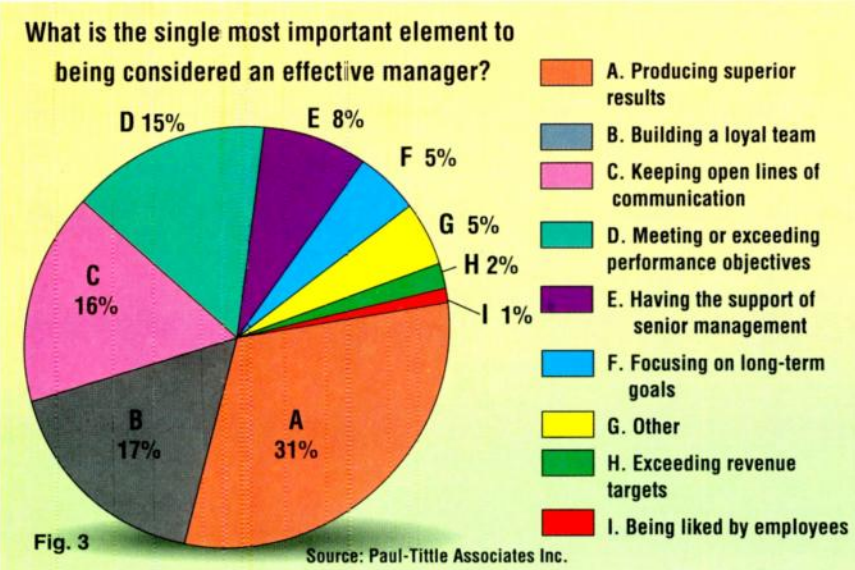


Fig. 3

Fig. 4

"dedication to professional development," and "a talent for making the company/department more successful."

From the results of this survey, one might say that these individuals are "show me" people. Of those surveyed, 73% said the managers they thought were outstanding, produced "superior" results. And, 71% of those managers had been promoted. The most important element in being an effective manager according to survey participants is "producing superior results" *(Fig. 3)*. Otherwise, managers must build a loyal team, keep communication lines open, and meet or exceed performance objectives.

Management styles are reflecting the idea that managers are not working to police their employees, but to make their jobs easier. They're making sure that everyone has the tools they need to get the job done effectively.

As far as training goes, survey participants are convinced (81%) that effective management skills can be learned through training (*Fig. 4*). Of the respondents, 62% said they were managing a team at the time the survey was taken, and 61% said they would benefit from participating in a management training program.

Study participants included telecommunications managers (23%), IT professionals (18%), Internet professionals (13%), management consultants (12%), systems integration specialists (12%), and multimedia professionals (6%). Over half of the participants came from companies with over 500 employees, of which 47% are publicly owned.

Debra Schiff is a former copy chief at Electronic Design. She may be contacted via e-mail at: debras@csnet.net

Does This Black Cloud Really Have A Silver Lining In It?

LAYOFFS IN THE SEMICONDUCTOR INDUSTRY HAVE DAMPENED, BUT NOT DRENCHED, THE OVERALL EMPLOYMENT MARKET.

LISA HOCHGRAF

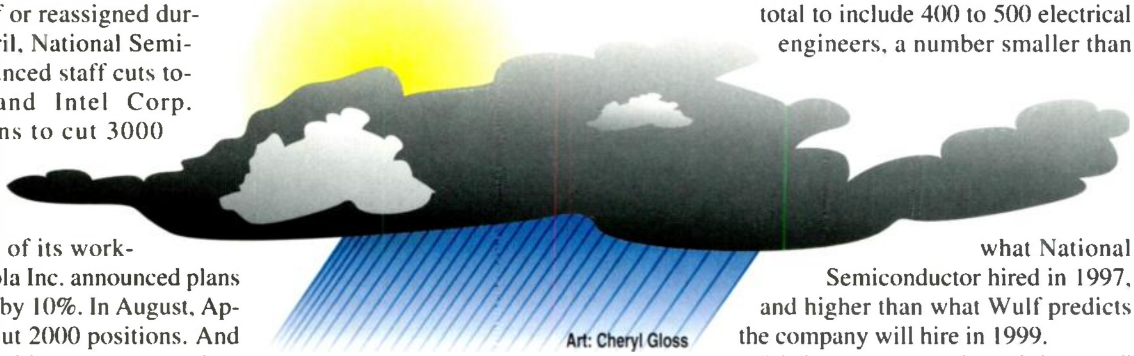
Recent announcements from leading semiconductor companies and suppliers have somewhat darkened the tremendously sunny hiring outlook that had become the norm for electrical and electronics engineers.

As of this writing, thousands of employees, including some engineers, had been laid off or reassigned during 1998. In April, National Semiconductor announced staff cuts totaling 1300, and Intel Corp. announced plans to cut 3000 jobs. In June, Lam Research announced it would trim 25% of its workforce and Motorola Inc. announced plans to cut its staffing by 10%. In August, Applied Materials cut 2000 positions. And the list goes on, with some reports placing the tally of displaced employees—by attrition and by layoff—at over 100,000.

The impact of these changes have been hiring freezes at companies that previously couldn't hire fast enough.

"The hiring forecasts are a little cloudy, but it's not a big depression," says Michael Richey, manager of university relations at Motorola in Phoenix, Ariz. "Our (hiring) numbers will probably not be as great as in recent years."

This shift from a hiring craze to a hiring freeze at many semiconductor industry companies reflects the economic turmoil in Asia, which has decreased demand for computer chips, as well as a changed relationship with suppliers, and the cyclical nature of the industry.



Art: Cheryl Gloss

Providing that the world and U.S. economic markets don't take a deeper plunge than they already have, the rain clouds over the semiconductor market may clear up by next year, some say. And, even while the semiconductor industry pauses to regroup, other industries and companies continue to hire with sunny enthusiasm.

"Electrical engineering is a very broad field," says John Rosica, president of Management Recruiters International of the Silicon Valley Inc., San Jose, Calif. "If you're talking about digital design, there's a certain amount of saturation, but there are plenty of other fields that will be strong. Analog design is going to be at a premium."

THE CURRENT CLOUD

The announced and realized cutbacks in the semiconductor industry are part of an overall effort to reduce staff levels--especially in the manufacturing area--to better match recent decreases in demand for product. The layoffs and reductions also marked the start of a widespread hiring freeze.

"In the last five years, they (companies) beefed up heavy duty on the fabrication side," Rosica says. "Those people have been let go, but design people are OK for now."

The "beefing up" Rosica describes was definitely played out at Intel, which grew very rapidly in 1997, reaching the 60,000-employee mark.

"We went through a major growth ramp in '97," says Dave Woolsey, staffing manager for the lab and product groups at Intel Corp., Portland, Ore. "In 1998, we've focused on getting people established. This year's been a year of heavy internal placement. We don't see the kind of growth we saw in '97 when we were hiring 1000 (new employees) a month."

At National Semiconductor, Santa Clara, Calif., Director of Staffing Tom Wulf says he expects this year's hiring total to include 400 to 500 electrical engineers, a number smaller than what National Semiconductor hired in 1997, and higher than what Wulf predicts the company will hire in 1999.

"It's just an uncertainty right now," Wulf says. Hiring in this climate "tends to be more focused."

At Micron Technologies, hiring is also on hold, but for very specific strategic offers of employment.

"During good times we might bring on 20 to 25 people a year into our research area, including technicians and engineers," says Guy Blalock, process development engineering manager based in Boise, Idaho. "We've been in a low spot in the industry so we've been basically in a hiring freeze—except for critical experts."

RAIN FROM FAR AND NEAR

Financial analysts and industry experts cite a number of reasons for the cur-

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In addition, Silverstein says, the smaller and medium-sized suppliers in the printed-circuit board industry are doing fine. "It's the high-volume companies that are competing with the offshore groups that are getting creamed," Silverstein says. "Currency devaluation is hurting the big groups."

Supplier issues are also of concern to operations at Micron, according to Blalock. When a big supplier of equipment announces a set of layoffs, big questions arise that may make companies more hesitant to staff up, he explains.

These questions include: Will the supplier be able to maintain our current equipment? Will it be able to provide the cutting-edge equipment that will help us keep a competitive edge? Will it be able to meet our supply demands with a smaller staff? And finally, will they be able to make necessary changes at a moment's notice?

Semiconductors are a "very cyclical business," adds National Semiconductor's Wulf. "People tend to think it won't be around in the future. People kind of hope it won't be."

Silverstein says such cycles are common with companies that make basic components important to many final products. "With any kind of commodity, if there are shortages at one point, everyone jumps on the bandwagon," he says.

Then later, when demand decreases, it's not unusual to find the whole industry overbuilt and overstaffed.

"This is not a unique phenomena," Motorola's Richey says. "Every eight to 12 years, each company is going through it. It really makes us take a look at the overall situation and forces us to be more strategic."

BRIGHT SPOTS

While staffing managers at the major semiconductor industry companies predict that the sky may clear as early as next year, others close to the marketplace believe that the impact of the Asian market crisis has only just begun. While only time will tell for sure, companies in many other employment areas open to electrical and electronics engineers continue to recruit personnel quite heavily.

Blalock is optimistic that the end of the hiring freeze at Micron is near. "Hopefully we're seeing the end of the dark moments, but the end of the dark moments can be pretty tough," he says. "We're looking forward to being able to make requisitions for new personnel."

At Intel, Woolsey says recruiters are looking for people with experience in microprocessor design, Computer-Aided Design (CAD) tool development, and the hardware and software aspects of networking. "We may be facing some issues, but it will be mitigated very shortly and we'll return to some exciting times."

"I don't think there's ever been a bet-

PERCENTAGE OF ELECTRICAL AND ELECTRONICS ENGINEERS BY INDUSTRY SECTOR

Because electrical engineering is such a broad field, employment opportunities may continue to abound in other sectors despite recent changes in staffing levels and hiring strategies in the computer chip industry.

Sector	1987	1989	1991	1993	1995	1997
Aerospace	20%	15%	13%	11%	10%	11%
Communications	5	7	7	11	13	18
Computers	9	10	10	11	12	12
Defense	20	15	12	12	10	10
Electronics	4	7	11	11	12	16
Utilities	11	9	11	11	11	11

Source: IEEE U.S. Member Salary & Fringe Benefit Surveys, 1987-1997 editions

ter time to be in the industry," he continues. "There's an opportunity to be in on the front end of the development efforts. People are going to be challenged to help pioneer the next generation of where technology will take us."

Amidst these optomistic forecasts of clear skies, Silverstein believes the full blow of the world economic crisis has not been fully realized. "The reports of doom and gloom in the global economy are getting worse and worse," he says. "We've just seen the first round of the impact."

Whatever happens with semiconductor industry hiring, the overall employment picture for electrical and electronics engineers does appear positive. And this applies to the short and long term. A recent survey by Management Recruiters International Inc., headquartered in Cleveland, Ohio, found that the outlook for hiring executives, professionals and sales people in electronics and electrical products is quite favorable. Following are the numbers to back it up.

Of those executives with the responsibility for hiring in this sector of the electronics industry, the survey found that 55.4% had plans to increase their staffs in the second half of 1998, down by 4.6 percentage points from the first half of the year. Another 36.9% plan to maintain current staff sizes, up by eight-tenths of a point. Only 7.7% of these executives report plans to decrease staff, up 3.8 percentage points.

Interestingly, while the overall industry outlook is less rosy than earlier this year, it is still a better scenario than in 1996, when the survey found that only 40.1% of executives planned to increase staff, and 12.3% planned to decrease the number of employees at their companies. In other words, despite the "doom and gloom" forecasts by economic naysayers, there is a silver lining after all.

A case in point of a company in the broader industry planning to increase hiring is Lutron Electronics Company Inc., a manufacturer of lighting equipment located in Coopersburg, Pa. According to Staffing Program Manager Corinne Snell, the company already plans to double the number of electrical engineers it hires next year.

"We know it's going to be another tough year of competing for the best candidates," she says. "Double Es will be our target this year more than MEs."

Snell says she has read extensively about the layoffs on the West Coast, but she doesn't think the situation out there will make her job of hiring quality engineers in Pennsylvania any easier. The feeling here is that quality does not always "migrate" to open areas that easily.

"It's not like we're going to be able to lay back," she says, noting the continuing competition for electrical engineering talent. "We're going to have to go and recruit and hopefully we'll get our numbers nice and early."

Lisa Hochgraf is president of Top-Notch Text Writing and Editing Services. She can be reached via e-mail at lisa@topnotchtext.com.

If Times Get Tough At My Company, Should I Stay Or Should I Go?

CONSIDER THESE STRATEGIES TO KEEP YOURSELF MARKETABLE IF YOUR COMPANY HITS A ROUGH PATCH.

LISA HOCHGRAF

When engineers sense their company is in trouble or, worse yet, when layoffs are on the horizon, two distinct strategies can help them stay employed, according to San Francisco career consultant Charles Prugh.

The first is to focus on maintaining their current jobs by making themselves seem indispensable to their employers. The second is to carefully decide when to make a career move, whether to another department or another company, and to make that shift successfully.

"One is positioning how to make themselves valuable to an employer, to detect a needed niche and fill it," Prugh says, although neither strategy is an absolute guarantee of continued employment. "That is one way to ensure job security. The other is to know when to go up, over and out in your own best interest and at the right time."

ALL IN YOUR ATTITUDE

When trying to keep a position with your current company, your focus should be to make yourself stand out from other employees in a positive way.

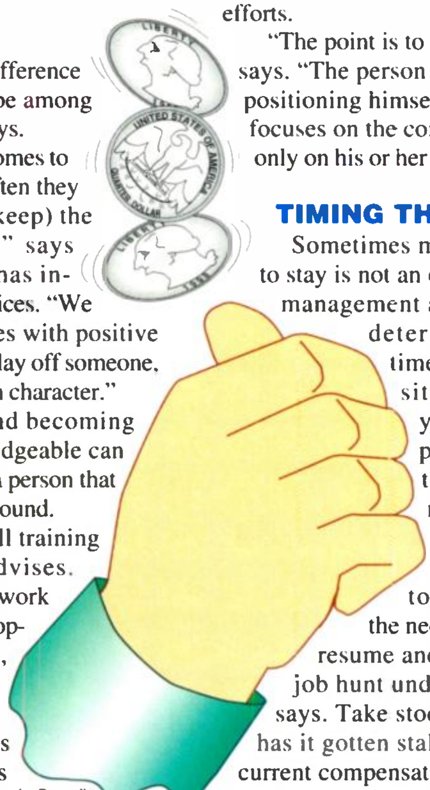
"This starts with a personal evaluation," says Bob Lenburg, president of the Human Resources Group, a human resources consulting company in Madison, Wis. "It's being brutal. 'Show me, tell me. What can I show that separates me from the others?'"

One thing that you can show is that you're positive about the company and your work. This simple shift in attitude can make a tremendous difference in whether or not you'll be among those laid off, Lenburg says.

"Deep down when it comes to making decisions, very often they (managers) choose (to keep) the more positive person," says Lenburg, whose work has included outplacement services. "We like to surround ourselves with positive people. If you're going to lay off someone, the obvious one is the pain character."

Actively learning and becoming more technically knowledgeable can also make you seem like a person that a company should keep around.

"Take advantage of all training offered," Lenburg advises. "Technical folks tend to work within a narrow niche. If opportunities seem broad, they may not take them," but they should.



L. Gravell

Prugh advises his clients to keep their eyes open as they look for needed niches to fill, especially in this changeable employment marketplace.

"Some people fall asleep once they get a job," Prugh says. "I'm emphasizing staying awake and acquiring the skills that are needed. Apply creative reasoning to see what needs are likely to arrive and then propose solutions."

And don't forget to promote your efforts. When you read extra manuals, mention it to your supervisor. Try to maintain a high profile with the powers-that-be.

"Some people hunker down and take a low profile," Lenburg says. "I would recommend the opposite. Jump in with great vigor."

Lenburg says an employee's high profile doesn't necessarily come from solving the most difficult technical problems. Leading the annual United Way campaign or brainstorming new product ideas can be just as effective at raising management's awareness of your good efforts.

"The point is to stand out," Prugh says. "The person who succeeds in positioning himself is the one who focuses on the company goals, not only on his or her objectives."

TIMING THE CHANGE

Sometimes making the effort to stay is not an option. Watching management actions can help determine when it's time to give up "positioning" within your current company and make the decision to move "up, over, or out."

Various factors may point to the need to update your resume and get an external job hunt underway, Lenburg says. Take stock in your work: has it gotten stale? Look at your current compensation situation: are benefits being trimmed? Consider your relationships with others in your department: how are things going with your supervisor?

Prugh says figuring out when it's time to make a move depends on the changes management makes in structure and technology.

For example, if a company decides that an entire engineering function will be outsourced, that's a major change in priority for the company's structure, and may suggest it's time to look for work elsewhere.

Similarly, "systems and technology are many-headed beasts" that affect career decisions, Prugh says. "Technology can reshape a person's position or it can revise it so it becomes much more impor-

Successful As A "CMP"

Today's most successful and talented employees are frequently those most willing to change jobs and careers, according to San Francisco career consultant Charles Prugh.

•Prugh calls these employees "career mobility practitioners," and defines the following characteristics and attitudes that most "CMPs" demonstrate:
•They show evidence of being and wanting to be self directing.
•They prefer to choose and pursue their own career positions.
•They are flexible and willing to change their career direction.
•When employed, they work hard to advance themselves with their current employer.
•They show self-confidence, flexibility, and willingness to resign from one employer to accept or create a better position with another employer.
•They speak of work as though every job has a beginning, a midpoint, and an end.
•They are quick to perceive the end of their present position when it arrives.
•Seldom do they show long-term patience with, or extend long-term loyalty to, managers who offer them only vague offers of promotion. They execute major or minor moves in their own best interests and at the right time.

tant because the person is the only who knows how to get the information out of the computer. It also can downgrade a job or eliminate it altogether."

Sometimes it's difficult for people to decide to leave their jobs, even when the demise of the company—or even just many jobs—is evident, Prugh says.

"Some of those people who become centered in holding a position, they're pluggers," he says. They resist change. They remain loyal to the company even more than they remain loyal to their level of skills."

Prugh recalls a company that was really going under. The people who fit his "plugger" characterization would actually buy stock in the troubled company from those who left the organization for other positions.

"This is like the people in the Titanic who were trying to plug the hole," Prugh says. "They just stay there until the thing hits the beach, and they all go down to the unemployment agency together."

MAKING THE LEAP

If you see the writing on the wall that it's time to make a job change, you might test the idea out with close friends or family to see what their response is, Lenburg suggests. Then, if you want to proceed, you'll need to update your resume, and brush up your interviewing and salary negotiating skills.

Company Profiles

Spectrian Corp.

Headquartered in Sunnyvale, Calif., Spectrian is the leading supplier of ultra-linear high-power amplifiers to cellular infrastructure manufacturers worldwide. They offer many design engineering opportunities, and have doubled their product portfolio and set a record for annual revenue for the sixth year in a row. Spectrian's high-power linear RF amplifiers have captured over 40% of the global market. They received a Gold Circle Award for being one of the 50 fastest growing technology companies in the U.S. Founded in1984, Spectrain currently employs 150 engineers and plans to add 50 more in the next year.

Company headquarters is located at: 350 West Java Dr., Sunnyvale, CA 94089

Separation Protections

Employees over 40 have certain special rights under the Older Worker Benefits Protection Act when they are being offered a separation package, according to Bob Lenburg, president of the Human Resources Group, a human resources consulting company in Madison, Wis.

Often companies offer separation packages in exchange for employees' agreement not to sue the corporation for any unfair treatment. For such an agreement to be valid, the company must give former employees 21 days to think over the offered agreement, Lenburg says. Even after signing, former employees still have seven days to rescind.

The law was passed to protect employees from corporate practices that would present them with these agreements at 3 p.m. Friday and require them to make this big life decision by the end of the day, Lenburg says. Now, companies must encourage employees to see a lawyer and even a financial planner before signing.

"Older employees were being given a take it or leave it package," Lenburg says. "People were giving away all rights. This (law) is something people should be aware of."

Besides helping you get a new job, updating your resume can be a positive step for managing the emotions that go along with changing jobs, whether you're laid off or not.

Another tip from Lenburg: When interviewing for new jobs, be careful when answering the question, "Why are you looking for new employment?"

"Many people answer that question by dumping on their current employer," he says. "You always want to make as positive a statement as possible."

In addition, if the hiring marketplace feels a little tight because of economic trends, "keep reasonable expectations about salary," Lenburg advises. "A 20% increase isn't realistic."

Plus or minus 10% from your current salary is much more likely, he adds. "And it may well be the minus, especially if you have been working for a company for a long time and have very specialized knowledge. Some people hold out for a big pay increase and miss a few opportunities."

ATTITUDE AGAIN

Staying positive is key to positioning yourself within your current company and to successfully making a job change when the time is right. Doing so under the stress of employment turmoil means taking care of the strong emotions that may surface, and finding ways to turn them to the positive.

__Lisa Hochgraf__ is president of Top-Notch Text Writing and Editing Services. She can be reached via e-mail at lisa@topnotchtext.com.

Control Design Offers Buying Information Online

Have you ever needed immediate information from an electronic or electromechanical distributor? Well, now there's one place you can get it. Control Design, Sanford, Fla., just launched a web site designed to assist its customers in the buying process at *www.controldesign.net.*

All of the products that Control Design offers are listed on the web site, and there are even links to suppliers' sites. The site also includes a map of locations, press releases on new product lines, and in-depth information on featured products. Customers can now get information on pricing, availability, samples, and catalogs almost instantly.

The map on the site is particularly helpful. Just click on an area and then the address, and up comes the phone number of the office closest to that spot. Information on services provided by that Control Design office is also available.

Control Design is riding another interesting turn of events. It plans to open its first office outside the continental U.S. This sales location in Puerto Rico is scheduled to have its grand opening on April 16, 1999. After selling electronic and electromechanical components in Puerto Rico for better than two years, Control Design made this move to support its growing customer base there. This facility is also much less expensive and more convenient to its primary customers, OEMs.

Another new facility opened in Atlanta, Ga., on September 1, 1998. Its purpose is to help cut lead times and provide clients with customized products. This location will specialize in custom packaging and kitting, subassembly of terminal blocks, rail assemblies and switches, and custom labeling. The facility was designed to improve customer service. The company believes that the greatest improvement will be in the reduction of lead times.

For more information on Control Design, visit its web site at www.controldesign.net. Contact the new Puerto Rico sales location by phone at (954) 782-1311 or fax at (954) 942-2458. Reach the new facility in Atlanta at (770) 979-3500 or by fax at (770) 979-3906.

Electronic Connections Doubles Up On DDK's Offerings

Electronic Connections from Englishtown, N.J., just agreed to take on some of the newer products from DDK Electronics Inc., Santa Clara, Calif. Electronic Connections is a full-line, franchised distributor for DDK Electronics Inc.

Among the new additions is the DHA series of shielded 0.050-in. centerline I/O connectors for bidirectional IEEE 1284 interfaces for printers. It's meant to be used with computers and peripherals for telecom and network hubs. The CE05 Series MIL-C-5015-style circular connectors are also offered. The series connectors use a space-saving, half-pitch design, provide reliable ribbon-style contacts, and presend IDC termination for the plug. The D-shaped shell polarization of the connectors cuts out mismating, while offering a secure mating lock design. The connector gets ESD protection from the closed front insulator, while the solid metal shell suppresses EMI.

The HSB Series of serial I/O connectors, designed to meet the connector and cable-assembly specifications for the IEEE 1394 Serial Bus, is another new addition. The HSB connectors are also small in size, which makes them easy to connect and disconnect. With six gold-plated, ribbon-style contacts, they're rated for a minimum of 1500 mating and unmating cycles. The design protects from ESD, and the power and ground contacts have a premating design for circuit protection. The connectors are hot-pluggable for plug-and-play applications, and support data-transmission rates of 100, 200, and 400 Mbits/s.

To find out more, contact Electronic Connections by calling (800) 295-0900 or (732) 446-4544.

Fairchild Signs Up With All American Semiconductor

All American Semiconductor Inc., Miami, Fla., recently announced an expanded all-location authorization for Fairchild Semiconductor Corp., centered in South Portland, Maine. Fairchild is a leading supplier of multimarket semiconductors, which are used in the telecommunications, consumer, industrial, personal computer, digital video, and automotive markets.

According to All American, this deal benefits the company by permitting it to offer a great variety of semiconductor products to its customers. Fairchild, meanwhile, bets on gaining an expanded customer base and multiple market segments.

For more information, take a look at All American's web site at www.semi.com.

Bisco Industries Expands With Facility In Tempe

Bisco Industries Inc., Orange, Calif., cut the ribbon at the opening of a new facility in Tempe, Ariz. The Tempe facility is Bisco's fifteenth in the U.S. and Canada. Officially, it opened its doors on August 3, 1998. Its purpose is to improve customer service. The facility is located at 2405 East Southern Ave. Suite #2, Tempe, AZ 85282. For more information, visit Bisco's web site at www.biscoind.com, call (602) 456-1815, or fax (602) 456-5218.

Richardson Announces Deal To Distribute For BARCO

Richardson Electronics of LaFox, Ill., has become the first to distribute medical products on behalf of BARCO Display Systems, Kortrijk, Belgium. Richardson distributes display monitors and imaging components to the medical industry.

Additions to the Richardson line include BARCO's MWD321 21-in. high-resolution color medical workstation display with a resolution of 1600 by 1200 and the MGD521 5 MegaPixel medical gray-scale display, which boasts a resolution of 2048 by 2560. The MeDis 5MP 5 MegaPixel diagnostic display system comes with the MGD521 diagnostic gray-scale display. The 5MP PCI 2048 by 2560 medical imaging board is available as well. Each display comes with BARCO's

TrueGrey system, designed to allow accurate, consistent, and neutral display of a wide range of gray scales.

For more information, visit Richardson Electronics' web site at www.rell.com.

■ Jameco Electronics Makes Buying A Breeze

Like many other distributors, Jameco Electronics, Belmont, Calif., is making it easy to order its products over the Internet. The online catalog has been up and running for a while, but recently became even better. Now, it's got photos of the products, more detailed descriptions, wider search possibilities, and quicker ordering from a secure commerce web server.

Jameco also just released a 140-page catalog. Three hundred new products have been added to it, including refurbished Macs and peripherals, vacuum tubes, 100BaseTX Ethernet products, LEDs, LED displays, and more.

For a free copy of the catalog, call (800) 831-4242, fax (800) 237-6948, or e-mail info@jameco.com. To find your way to the updated web site, type in www.jameco.com.

■ Stanley Electric Cuts Deal With Surface Mount Distribution

Stanley Electric Sales of America, Irvine, Calif., has announced an agreement with Surface Mount Distribution Inc. According to the particulars of the deal, Surface Mount Distribution will stock the full line of Stanley's surface-mount technology (SMT) LED products. The "NovaBright" ultra-thin, right-angle, reverse and standard mount, and bicolor SMTs come with the deal. These products and more are available at Surface Mount Distribution's four regional facilities, located in Huntington Beach, Calif.; San Jose, Calif.; Woburn, Mass.; and Boca Raton, Fla.

For more information, visit Surface Mount Distribution's web site at www.smdinc.com, or Stanley Electric's web site at www.stanleyelec.com.

Compiled and edited by Lisa Calabrese, editorial intern.

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ELECTRONIC DESIGN CATALOG/LITERATURE REVIEW

New Board Stacking Interconnect Selector

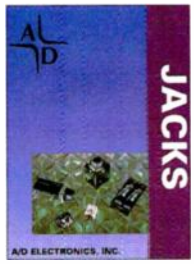
Samtec's popular Board Stacking Interconnect Selector has been expanded with a new 13th edition. This easy-to-use reference book takes the work out of finding the right interconnect for board stacking applications. Thousands of interconnect types and combinations are shown, including new 1mm and 0.50" micro pitch and surface mount interconnects. 800-SAMTEC9; Fax: 812-948-5047.

CIRCLE 248

SAMTEC

JACKS

A/D Electronics' free Jacks catalog features a variety of Jacks in different configurations. This 20-page catalog offers 2.5mm, 3.5mm, 4.5mm and 6.3mm styles. The design engineer can obtain complete specs, dimensional drawings and evaluation samples upon request. A/D Electronics also supplies a variety of interconnects for the OEM. (253) 851-8005; Fax: (253) 858-9869; www.adelectronics.com



CIRCLE 249

A/D ELECTRONICS

LCR METERS

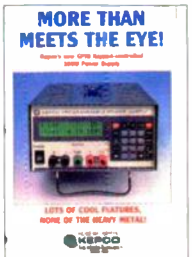
The SR700 Series LCR meters measure R+Q, L+Q, C+R and C+D with a basic accuracy as high as 0.05%. Features include variable test frequencies from 100 Hz to 100 kHz, internal or external DC bias, series and parallel equivalent circuits, and external capacitor biasing. An RS-232 computer interface is standard. GPIB (IEEE-488) and parts handler interfaces are optional.

CIRCLE 250

STANFORD RESEARCH SYSTEMS

A POWER SUPPLY AS SIMPLE AS ABC

Kepco's 100W-class bench power supplies, called series ABC, combine a GPIB-controlled voltage-current stabilizer with a univeral input, power factor corrected zero-up switcher, to produce a low-cost, lightweight high efficiency instrument. Outputs range from 0-10V at 10A to 0-125V at 1A. A panel keypad provides local control and a 2-line LCD display report both settings and actual values.



CIRCLE 251

KEPCO, INC.

POWER SOLUTIONS CATALOG

The latest Vicor Express catalog (#21) highlights a new family of 48Vin 2nd Generation high-density DC-DC converters. These converters are available in 3 package sizes - MaxiMods, MiniMods, and MicroMods - and offer output power from 50 - 500W. In addition, the catalog includes first generation DC-DC power components, AC Front Ends, configurable power supplies, and custom power services.

CIRCLE 252

VICOR CORPORATION

BOARD STIFFENERS DATA SHEET

Send for a Circuit Components Inc. Data sheet of Board Stiffeners and Bus Bars for PCBs. Minimize board warpage; Can double up as Rigidizer and power distribution device; Can be purchased in any length and available in 3 standard body heights - .250", .375", and .500" which correspond to current carrying capacities of 32-, 48-, or 64-amps for use in power, noise suppressing or grounding applications. 602-967-0624; Fax: 602-967-9385.

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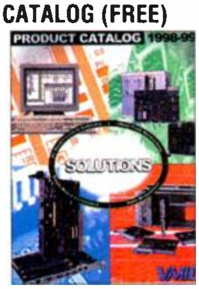
CIRCUIT COMPONENTS

NEW VMIC PRODUCT CATALOG (FREE)

VMIC is a supplier of PC-based Control Software (IOWorks®), embedded PC single board computers for VMEbus and Compact PCI®, RTnet™ - real-time networking products (Reflective Memory) for most popular computer systems, PLCs, and bus structures; I/O products for VMEbus, CompactPCI, PCI, USB, and ISA; and industrial I/O systems based upon VME and CompactPCI. 800-322-3616; http://www.vmic.com

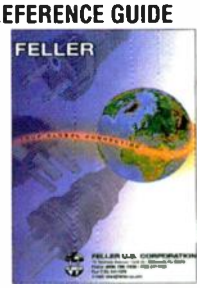


CIRCLE 254

VMIC

NEW POWER CORD REFERENCE GUIDE

This all new 48-page catalog portrays Feller's complete line of high quality domestic, hospital grade and international power cords. It provides detailed specifications illustrations, application, features and benefits. Many new products and services were added, including in-house cord assemblies, extensive packaging services and custom molding capabilities. 800-736-7333; Fax: 732-247-7279; E-mail: sales@feller-us.com; http://www.feller-at.com



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IMAGINEERING

FREE VXI SOLUTIONS GUIDE

The 1998 VXI Solutions Product Guide is a catalog and technical reference featuring product information on controllers, software, and our new VXI-DAQ instruments. VXI Solutions also includes a directory of over twenty VXI system experts from our Alliance program. (512) 794-0100; (800) 667-5347 (U.S. and Canada), Fax: (512) 794-8411; e-mail: info@natinst.com; www.http://www.natinst.com

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ACCUTRACE INC.

FREE PCB DESIGN DEMO CD!

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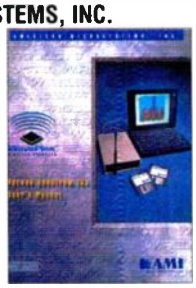
American Microsystems, Inc. (AMI) provides proven netlist conversion technology and a true vectories flow for synchronous designs. With over 15 years of translation ASIC experience, AMI has the greatest success rate for all netlist conversions. For more information on NETRANS products, call 1-800-639-7264 or visit our home page www.amis.com

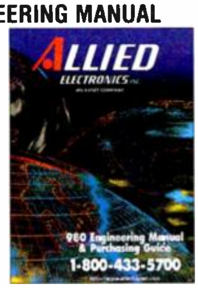


CIRCLE 260

AMI

ELECTRONICS ENGINEERING MANUAL

Allied Electronics Engineering Manual & Purchasing Guide contains reference data plus electronics from over 275 manufacturers. The Allied Catalog is available on CD-ROM. Allied Electronics is an Avnet Company with access to hundreds of millions of dollars of inventory. This breadth and depth gives you service capabilities found only at Allied Electronics, Inc. http://www.allied.avnet.com; 1-800-433-5700.



CIRCLE 261

ALLIED ELECTRONICS

FREE VHDL SIMULATOR

Aldec, Inc., announces the release of Active-VHDL version 3.1 a complete VHDL design environment. Active-VHDL is a complete IEEE 1076-93 VHDL design environment, including a VHDL editor, Behavioral Simulator, Automatic Test Bench Generator, interface to logic synthesis & FPGA/CPLD vendor P/R tools, VHDL design browser & Structural VHDL simulation. (800) 487-8743; (702) 456-1222; www.aldec.com

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ALDEC, INC.

ELECTRONIC DESIGN CATALOG/LITERATURE REVIEW

SuperTAP™ Emulator for x86

The new standard in high-end in-circuit emulators, SuperTAP solves tough hardware/software integration problems, debugs firmware and software, maximizes embedded system quality and performance. Palm-sized, full processor speed, easy set up, at half the price of chassis-based emulators 1-800-426-3925.

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APPLIED MICROSYSTEMS

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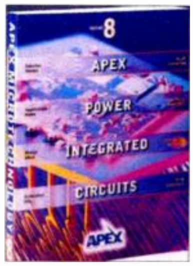
The 8th edition Apex Integrated Circuits data book contains complete product data sheets and applications notes for Apex Microtechnology's Power Amplifier, PWM Amplifier and DC/DC Converter product lines. Call: 1-800-862-1021; FAX: 1-520-888-3329; E-MAIL: prodlit@apexmicrotech.com



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APEX

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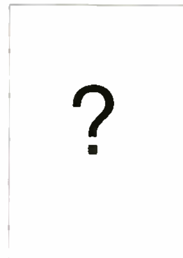

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YOUR COMPANY

ENCLOSURES & ACCESSORIES

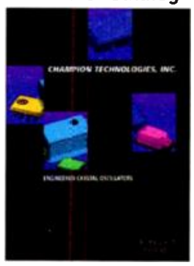
Bud Industries' new Standard Products Catalog provides technical data and ordering information on over 3,000 products ranging from large relay racks and cabinets to desktop and portable instrument cases including a full line of NEMA and other plastic enclosures. Also included is information on computer workstations, custom fabrication and a wide range of enclosure accessories.

CIRCLE 265

BUD INDUSTRIES, INC.

New & Expanded Crystal Oscillator Catalog

Champion Technologies' new crystal oscillator catalog and selection guide features technical information, electrical specifications and mechanicals for its newly expanded offering of frequency control products. Catalog provides detailed information on Champion's low cost clock oscillators and VCXOs, plastic SMT clocks, SMT VCXOs and TCXOs and high frequency TCXOs. 847-451-1000 or 800-888-1499, Fax: 847-451-7585. Website: www.champtech.com



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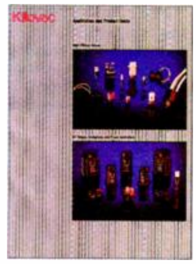
CHAMPION TECHNOLOGIES, INC.

HIGH VOLTAGE RF & DC RELAY CATALOG

Product Guide from Kilovac, a division of CII Technologies, features a broad line of high voltage RF & DC power relays and contactors. Feature ratings and specifications on relays up to 70 KV including QPL. Choose from 28 Vdc 270 Vdc aerospace power relays, contactors and power controllers. Industrial contactors to 750 Vdc. Contact: Pat McPherson, 805-684-4560; 550 Linden Ave., Carpinteria, CA 93013.



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KILOVAC Div. of CII TECHNOLOGIES

Commercial / Medical Power Supplies

Condor's 60-page catalog offers commercial and medical switching and linear D.C. power supplies. Commercial products meet latest international safety standards and medical products are certified to UL544, VDE0750 and IEC601. Call 800-235-5929, FAX (805) 487-8911. www.condorpower.com /~condordc

CIRCLE 268

CONDOR

Free LCD Design Guide & Specifications

Crystaloid® Product Guide helps designers and users specify passive LCDs and display modules using twisted nematic, supertwist nematic, RCTN™ and related technologies for commercial, industial, avionics and military applications. See LCD Primer at www.crystaloid.com or contact Crystaloid, 5282 Hudson Dr., Hudson, OH 44236-3769, 1-888-BEST-LCD, E-mail: salesdept@crystaloid.com

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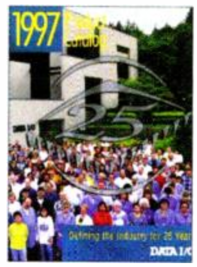
CRYSTALOID

DEVICE PROGRAMMERS & HANDLERS

The Data I/O catalog is the direct-order source of affordable tools for users of programmable devices. From design software to device programming and automated handling systems, the Data I/O catalog offers unbeatable values on the high quality tools you need. Call 1-800-332-8246, ext. 806



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DATA I/O

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MicroGrtid precision expanded foils in ferrous, nonferrous, precious and alloyed metals, ligt. flexible, mesh-like material for EMI/RFI/ESD shielding, electrical and heat conductivity. Process variations include: annealing, stretching, flattening & sellvage edging.

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DELKER CORPORATION

NEW OEM POWER SUPPLY CATALOG

Deltron's full line catalog presents many new products including 1kW to 7.5kW T Series power factor corrected front ends for telecommunications systems, DeviceNet power modules, new generation modular F Series 0.99 power factor corrected switchers and Moduflex® M Series switchers. The catalog also details a full complement of time tested hi-grade industrial and commercial power supplies. For free copy call 800-523-2332 or fax 215-699-2310.

CIRCLE 272

DELTRON

INTERCONNECT SOLUTIONS

This catalog enables design engineers to easily locate the correct adapters, clips and test accessories. The catalog includes a Ball Grid Array Reference Guide along with information on over 4000 ET products, including emulator tools, logic analyzer/scope adapters, programming adapters, production/test adapters, debugging accessories, prototyping adapters, field-configurable adapters and custom adapters. 1-800-ADAPTER www.emulatior.com

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EOS CORP.

FREE SRAM CATALOG

Galvantech, Inc. designs, manufactures and markets high speed, high performance static random access memories (SRAMs). A broad product line includes 1-meg, 2-meg and 4-meg densities available in both asynchronous and synchronous versions.

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GALVANTECH, INC.

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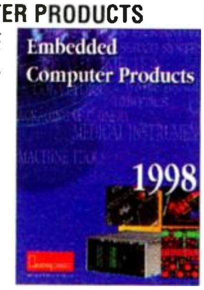
Gespac's 1998 catalog features a full line of 3U embedded PCs, 68XXO SBCs, motion control and over 200 I/O functions. The G-windows GUI for real-time systems running OS-9 is also offered. www.gespac.com or Phone 800-443-7722



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IRONWOOD ELECTRONICS

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"No-Power" Cholesteric Crystal Displays

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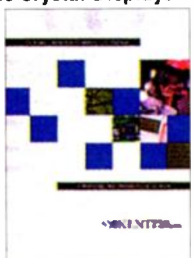
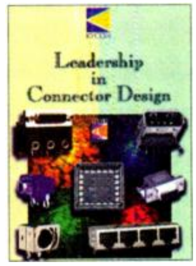


CIRCLE 280

KENT DISPLAYS

CONNECTOR CATALOG ON CD ROM

This 100 page catalog is available in both the standard full-line catalog and on CD ROM and includes many new products with complete specifications. Among the product highlights in Kycon's Catalog #11 are: •D-Sub-miniature connectors •Modular jacks •Mini-DINs •Stereo jacks •Power connectors •USB connectors •High temperature connectors •Ferrite and shielded connectors.



CIRCLE 281

KYCON, INC.

MICROPAK® INSTRUMENT ENCLOSURES

Lansing Instrument Corp. offers enclosures for smaller, free standing electronic instruments used in hand-held or desktop applications. Three body styles and a choice of end cap configurations are available, along with several finishes and colors. Literature includes information for stock and custom choices, and a no-risk offer at a special price. Contact Rich Kippola at Lansing Instrument Corp., (800) 847-3535.

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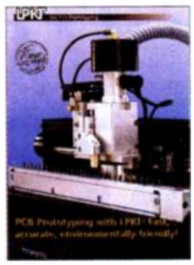

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MENTOR GRAPHICS

MELCHER 1998 DATA BOOK

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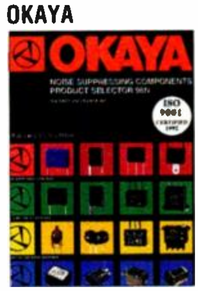

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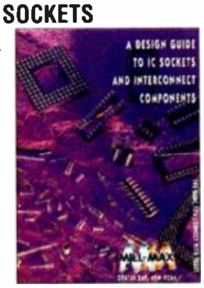

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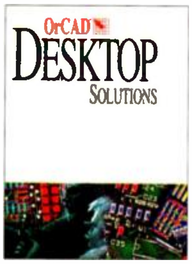

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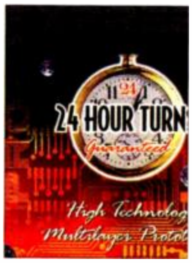

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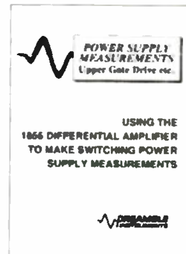

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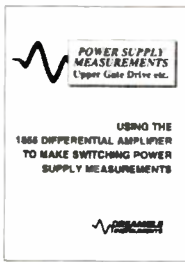

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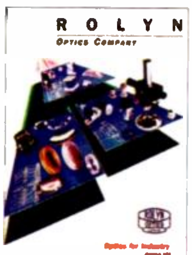

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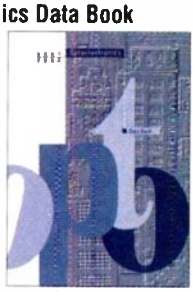

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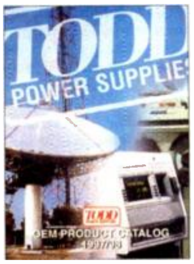

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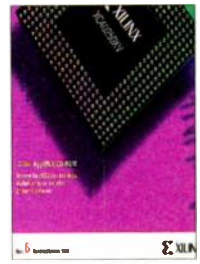

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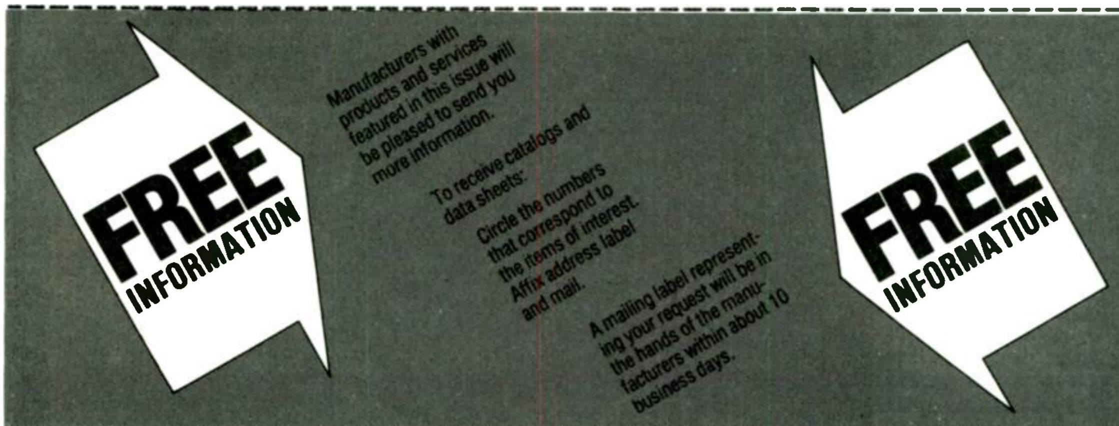

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Application Notes and Data Sheets:
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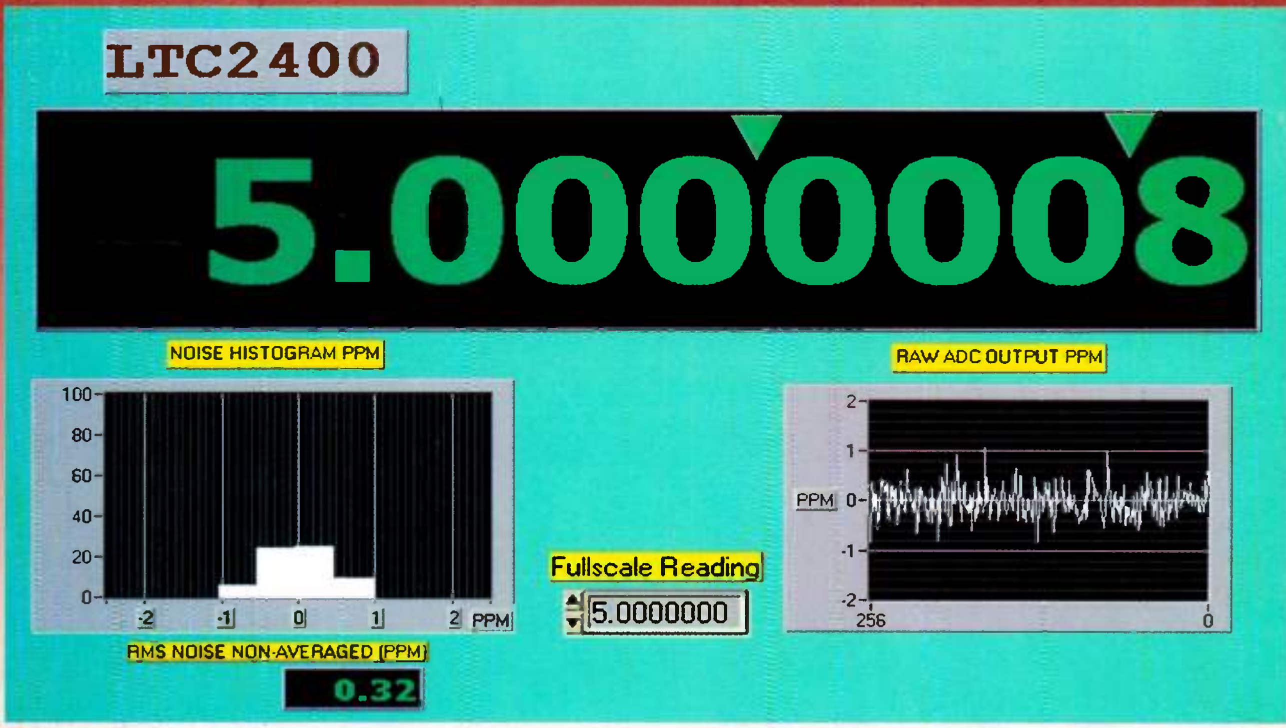
MUSIC SEMICONDUCTORS

24-Bit ADC in SO-8



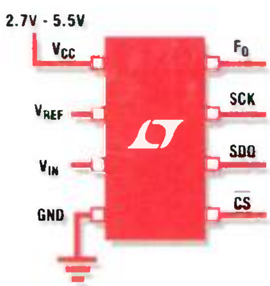
LTC2400: 1ppm Accurate Without Calibration

No calibration and very accurate – the pictures tell the story. The LTC2400 analog-to-digital converter comes in an SO-8 package and that's about all you need to know to start measuring 1ppm accuracy. No calibration registers to configure, no external crystal, no special filtering. The most important savings is time; it's so simple it saves design time!

Features

- 24 Bit ADC in SO-8 Package
- 2 ppm INL, No Missing Codes
- 15µV Full-Scale Error
- 5µV Offset
- 0.4ppm Noise
- Internal Clock
- 110dB Min, 50Hz/60Hz Notch Filter
- Single Conversion Settling Time for Multiplexed Applications
- Reference Input Voltage: 0.1 to V_{CC}
- Extended Input Range Accommodates 12% Overrange and Underrange
- Single Supply 2.7V to 5.5V Operation
- Low Supply Current (200µA) and Auto Shutdown
- $6.95 each for 1k Piece Quantities

LTC2400 Block Diagram



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