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# ELECTRONIC DESIGN

## TECHNOLOGY · APPLICATIONS · PRODUCTS · SOLUTIONS

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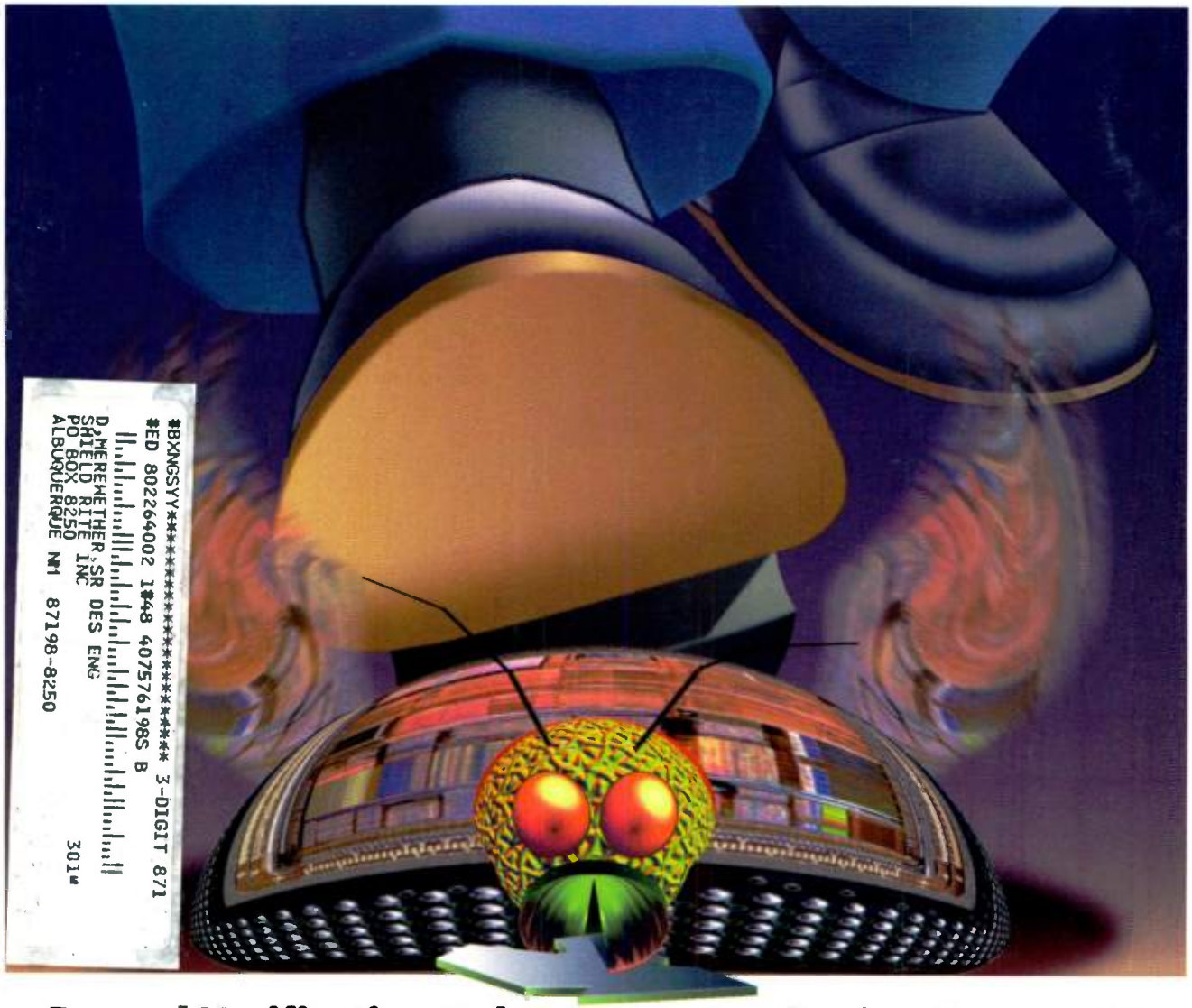


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**Previewing IEDM:** Get The Scoop On Memories/Speedy Logic, Analog And Power, Exacting Device Models, MEMS Sensors, And Brilliant Displays p. 37

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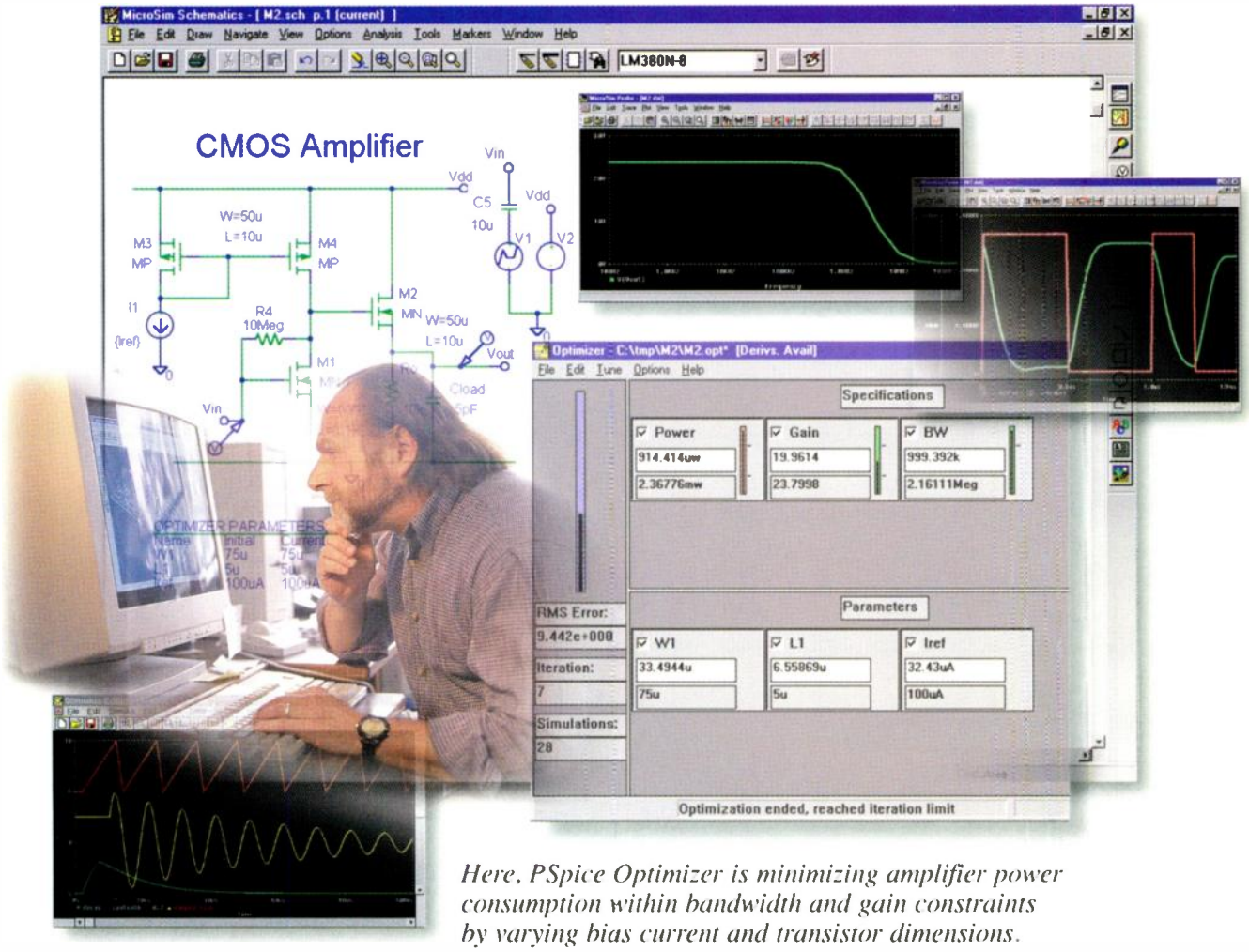
**Power, Packaging, And Components Supplement**

# Don't Just Simulate Your Design.




*Here, PSpice Optimizer is minimizing amplifier power consumption within bandwidth and gain constraints by varying bias current and transistor dimensions.*

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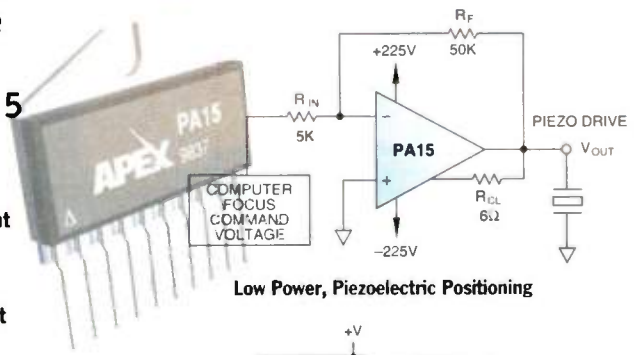
# Automatic Schematics

New Sample Circuit Center,
New 450V Power Amplifier,
New 10A Power Amplifier


## New High Voltage Power Op Amp in Power SIP: PA15

### Features

- 450 supply (±225V)
- 3.8mA MAX standby current
- 200mA output current
- 1.0" L x .25" W footprint
- Programmable current limit

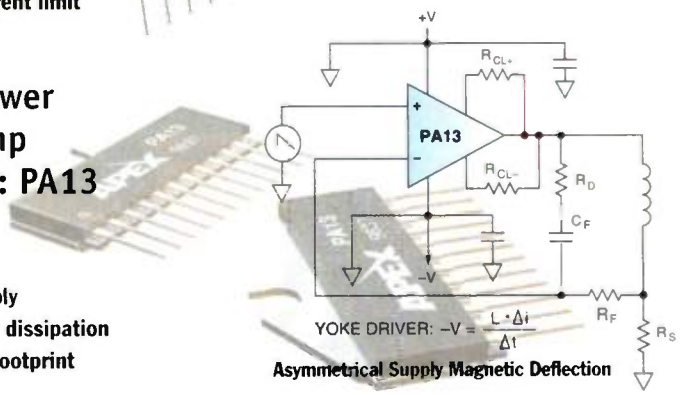



**Low Power, Piezoelectric Positioning**

## New High Power Power Op Amp in Power SIP: PA13

### Features

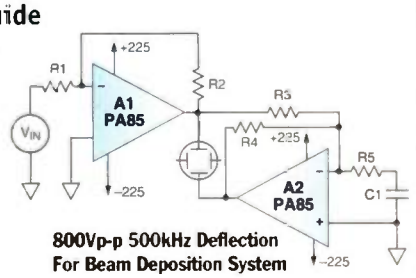
- 10A output PEAK
- ±10V to ±45V supply
- 135 internal power dissipation
- 1.22" L x .25" W footprint




**Asymmetrical Supply Magnetic Deflection**

## High Voltage Amplifiers Product Selector Guide

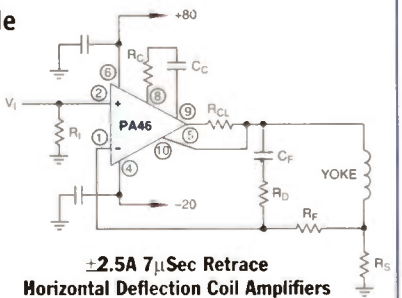
| Model | Supply | $I_{OUT}$ Peak | $I_{STANDBY}$ | Slew Rate | Package |
|---|---|---|---|---|---|
| PA08 | 30V-300V | 200mA | 8.5mA | 30V/µs | TO-3 |
| PA15 | 100V-450V | 300mA | 2mA | 20V/µs | PowerSIP |
| PA41 | 100V-350V | 120mA | 2mA | 40V/µs | TO-3 |
| PA42 | 100V-350V | 120mA | 2mA | 40V/µs | SIP |
| PA44 | 100V-350V | 120mA | 2mA | 40V/µs | PSOP |
| PA85 | 30V-450V | 350mA | 25mA | 1000V/µs | TO-3 |
| PA88 | 30V-450V | 200mA | 2mA | 30V/µs | TO-3 |
| PA89 | 150V-1200V | 100mA | 6mA | 16V/µs | PowerDip |




**800Vp-p 500kHz Deflection For Beam Deposition System**

## High Current Amplifiers Product Selector Guide

| Model | Supply | $I_{OUT}$ Peak | Slew Rate | Power Dissipation | Package |
|---|---|---|---|---|---|
| PA03 | 30V-150V | 30A | 8V/µs | 500W | PowerDip |
| PA04 | 30V-200V | 20A | 50V/µs | 200W | PowerDip |
| PA05 | 30V-100V | 30A | 100V/µs | 250W | PowerDip |
| PA10 | 20V-90V | 5A | 3V/µs | 67W | TO-3 |
| PA12 | 20V-90V | 10A | 4/µs | 125W | TO-3 |
| PA13 | 20V-90V | 10A | 4/µs | 135W | PowerSIP |
| PA26 | 5V-40V | 2.5A x 2 | 1.2V/µs | 36W | SIP |
| PA45 | 30V-150V | 5A | 27V/µs | 85W | TO-3 |
| PA46 | 30V-150V | 5A | 27V/µs | 85W | PowerSIP |

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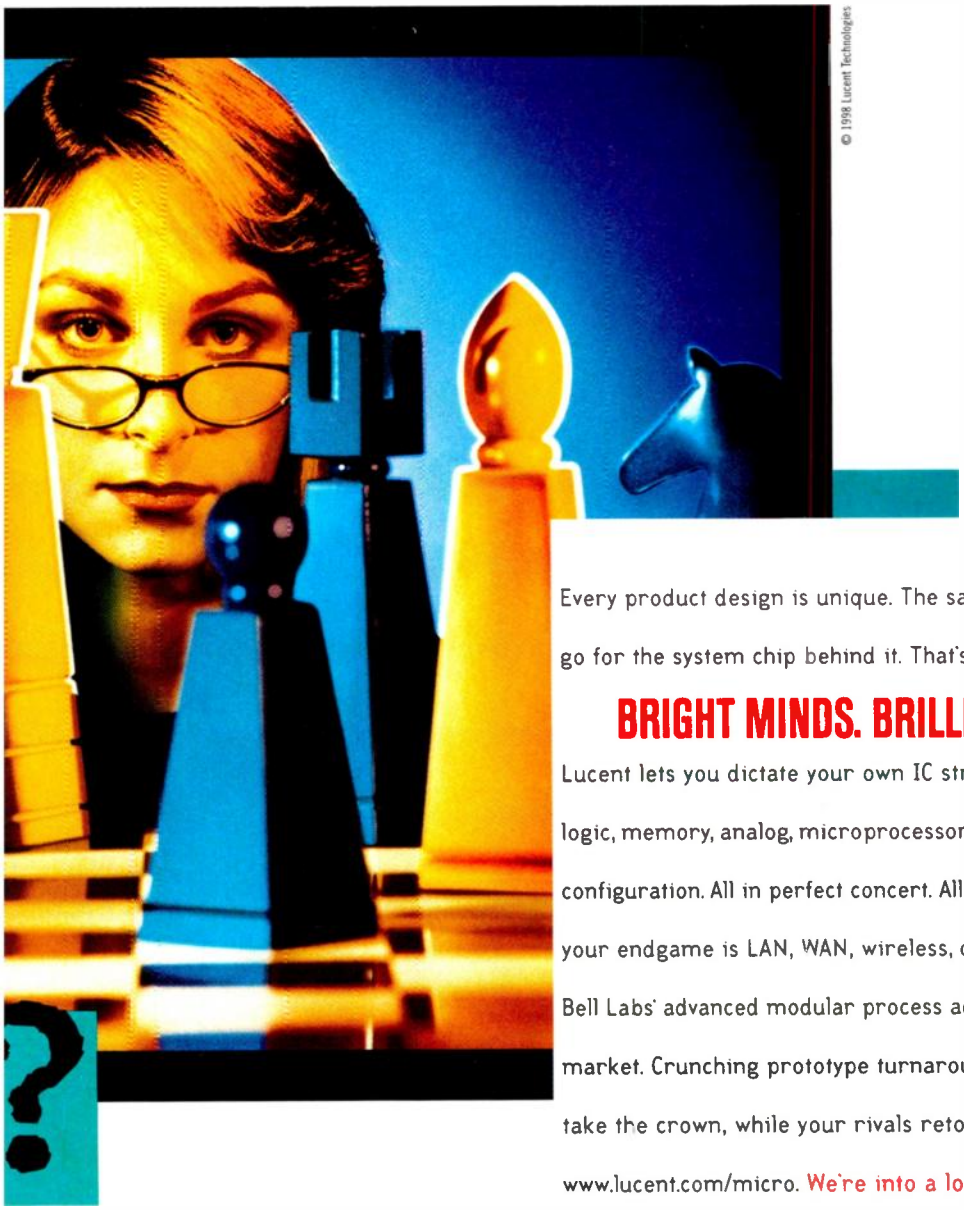
# TO DESIGN EACH SYSTEM CHIP WITH A CUSTOM STRATEGY





Every product design is unique. The same should go for the system chip behind it. That's why

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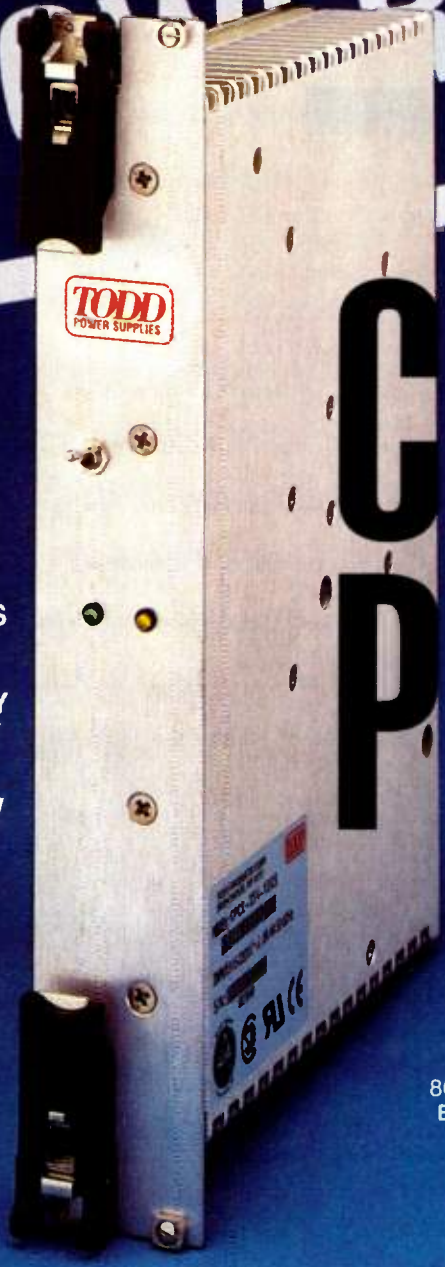


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*December 1, 1998 Volume 46, Number 27*

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### DEPARTMENTS



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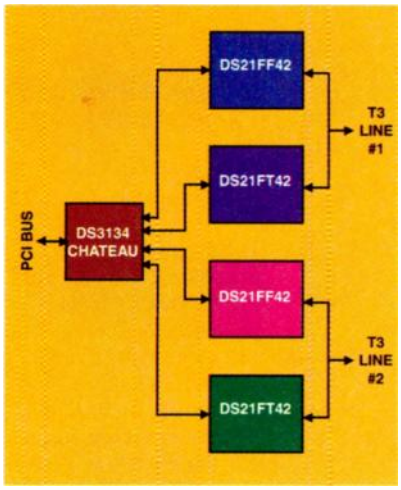
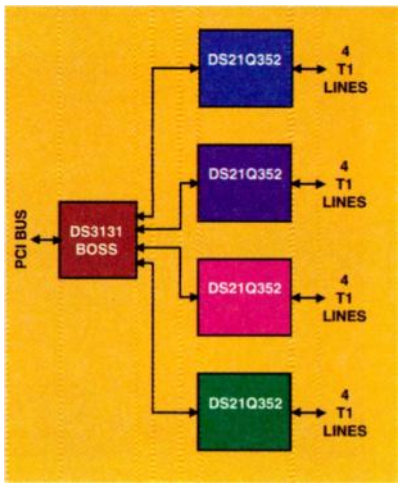
ELECTRONIC DESIGN (ISSN 0013-4872) is published twice monthly except for three issues in May and October, three issues in February, and three issues in November by Penton Media Inc., 1100 Superior Ave., Cleveland, OH 44114-2543. Paid rates for a one year subscription are as follows: $100 U.S., $170 Canada, $180, $200 International. Periodicals postage paid at Cleveland, OH, and additional mailing offices. Editorial and advertising addresses: ELECTRONIC DESIGN, 611 Route #46 West, Hasbrouck Heights, NJ 07604. Telephone (201) 393-6060. Facsimile (201) 393-0204. Printed in U.S.A. Title registered in U.S. Patent Office.

# PACK IT IN.
## HIGH DENSITY T1/E1 CHIPS FROM DALLAS SEMICONDUCTOR

At crowded T1 and E1 junctions, you need more interface in less space. To meet the challenge, new chips from Dallas Semiconductor define density at a higher level. For instance—




**Need an HDLC controller for a channelized T1/E1 design? Try putting 256 channels through one chip. The new DS3134 CHATEAU docks 64 T1 or E1 lines—or two T3/E3/HSSI lines.**



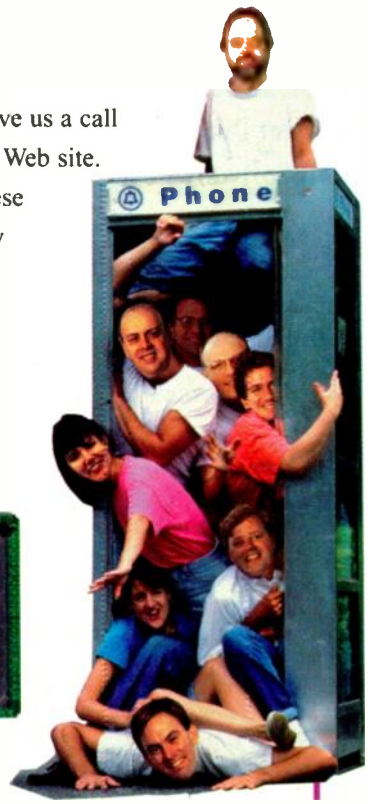

**Designing a DSLAM? POS? Any high-density, clear-channel T1/E1 application? One DS3131 BOSS (Bit- and Octet-SynchronouS) HDLC Controller masters up to 40 DSL lines or 40 T1/E1 lines.**

In each case, five high-density chips from Dallas Semiconductor replace 16 fluffier chips from the competition. Both controllers rely on extra-deep FIFOs and super-efficient DMA engines to boost performance. Programmable options, onboard Bit Error Rate Testing and local bus access give them flexibility.

Alongside the HDLC controllers starring here, supporting players star on their own:

- **4- 12- and 16-Channel T1 & E1 Framers:** These chips supply multiple density options for maximum flexibility with the smallest footprint and lowest cost.
- **Quad T1 & E1 Transceivers:** Four long- and short-haul line interfaces and four full-featured framers team up in one space-saving package, available in 3.3V and 5V options.

Enough talk. Give us a call or check out our Web site. Find out how these new high-density chips can help your design win the T1/E1 game.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*December 1, 1998 Volume 46, Number 27*

## EDITORIAL OVERVIEW

### BOARDS & BUSES



### PIPS



### COMMUNICATIONS TECHNOLOGY



### QUICKLOOK



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## LOOKING AHEAD: December 14, 1998

- **Test & Measurement Special Report—AWGs:.....** A Special Cover Story Report by Test & Measurement Editor Joseph Desposito examines aribitrary waveform generators, and how they're satisfying new testing needs.
- **Digital technology—application article on FPGA design:.....** A contributed Design Application article shows how careful HDL coding can maximize the performance of FPGA designs that are based on lookup tables.
- **Communications—overcoming obstacles to Gbit designs:.....** A contributed Design Application article explains how to overcome high-frequency (2.5-Gbit/s) design obstacles by making astute decisions at both the system and silicon level.

COVER ILLUSTRATION BY: BRUCE JABLONSKI



Jesse H. Neal Editorial Achievement

| | |
|---|---|
| 1967 First Place Award | 1978 Certificate of Merit |
| 1968 First Place Award | 1980 Certificate of Merit |
| 1972 Certificate of Merit | 1986 First Place Award |
| 1975 Two Certificates of Merit | 1989 Certificate of Merit |
| 1976 Certificate of Merit | 1992 Certificate of Merit |


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**ONLINE OVERVIEW**

*December 1, 1998 Volume 46, Number 27*

## See Electronic Design Online's Table of Contents to preview what's in store for you on the web!

### NOW ONLINE:

### The TechSide

In conjunction with Interaction Inc., a new feature now makes its debut this month on Electronic Design Online's **Comedy Club** page. **The TechSide,** produced by Interaction and Techside.com, is an animated cartoon tailored for the engineering and technical community. Readers will now get the chance to enjoy a more interactive portion of the web-site, and have an opportunity to inject a little humor into their everyday worklives.

In addition, readers will have an opportunity to submit their own ideas for future cartoons right from the **Comedy Club** page. If something at work got you upset, depressed, or made you smile, see your idea come to life on **The TechSide.**

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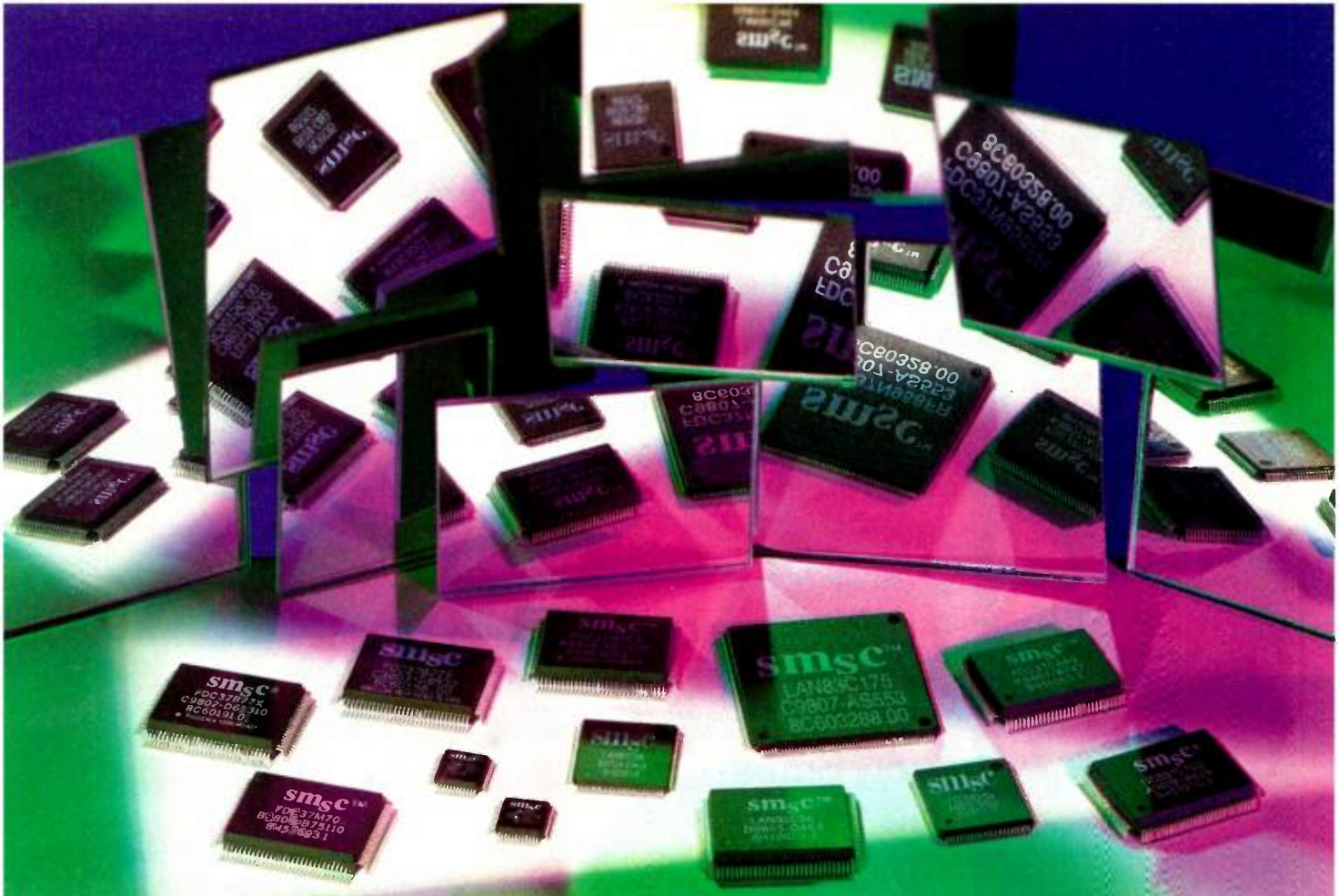


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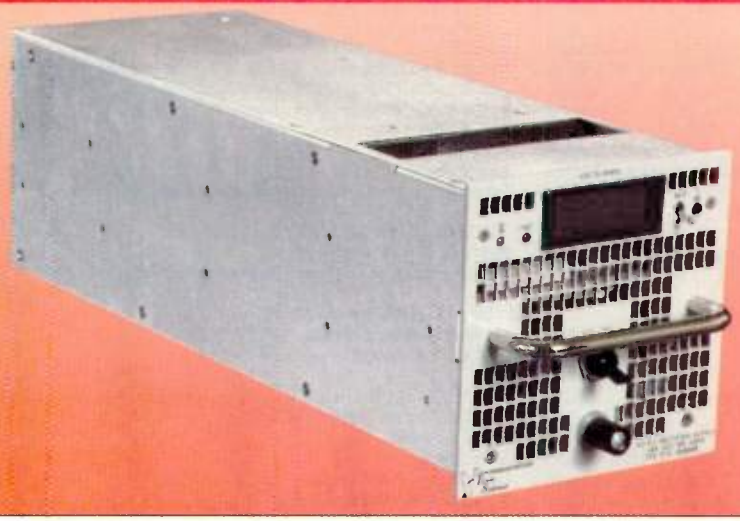

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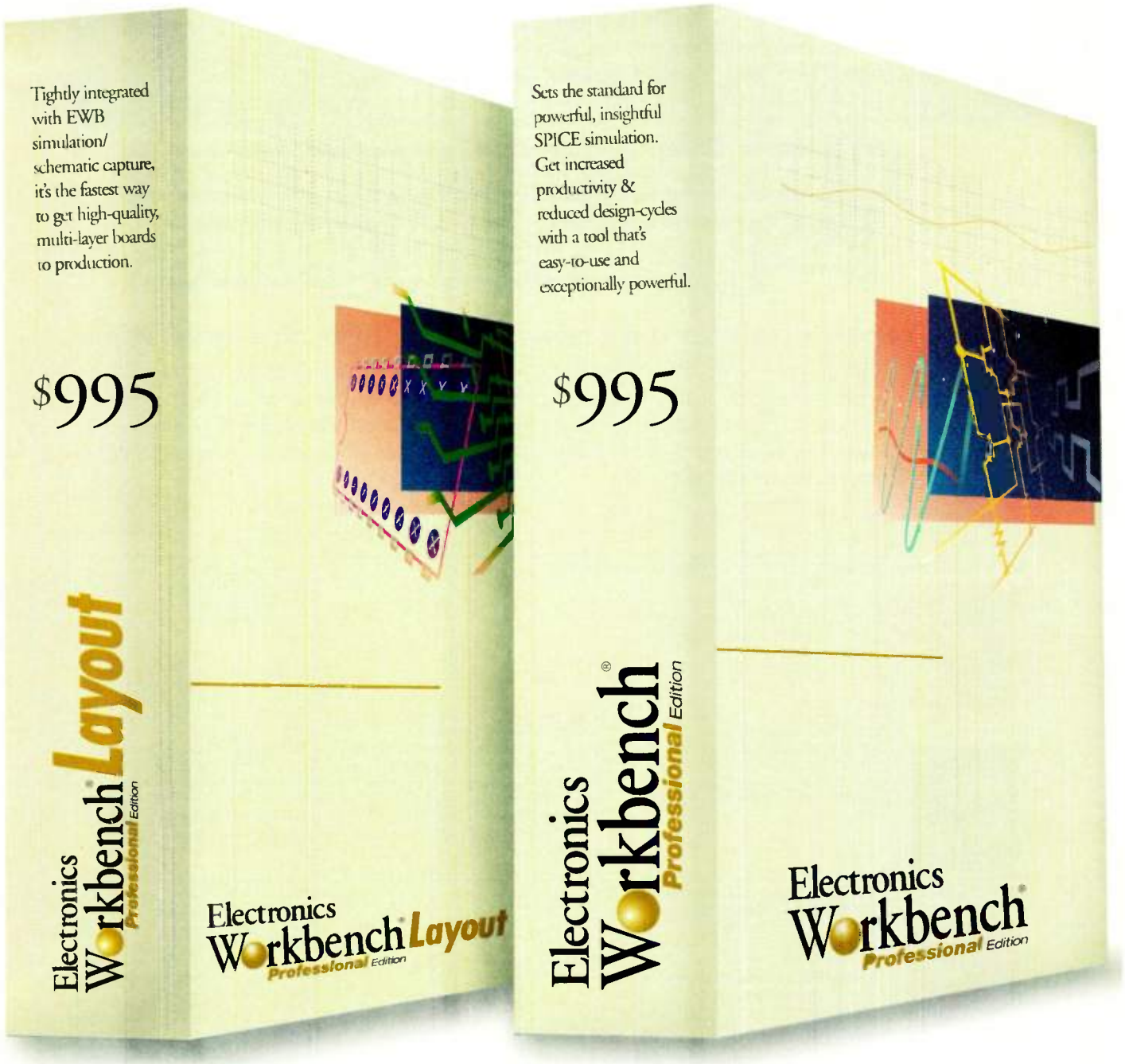


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EDITORIAL

# The Digital Age Is (Almost) Here

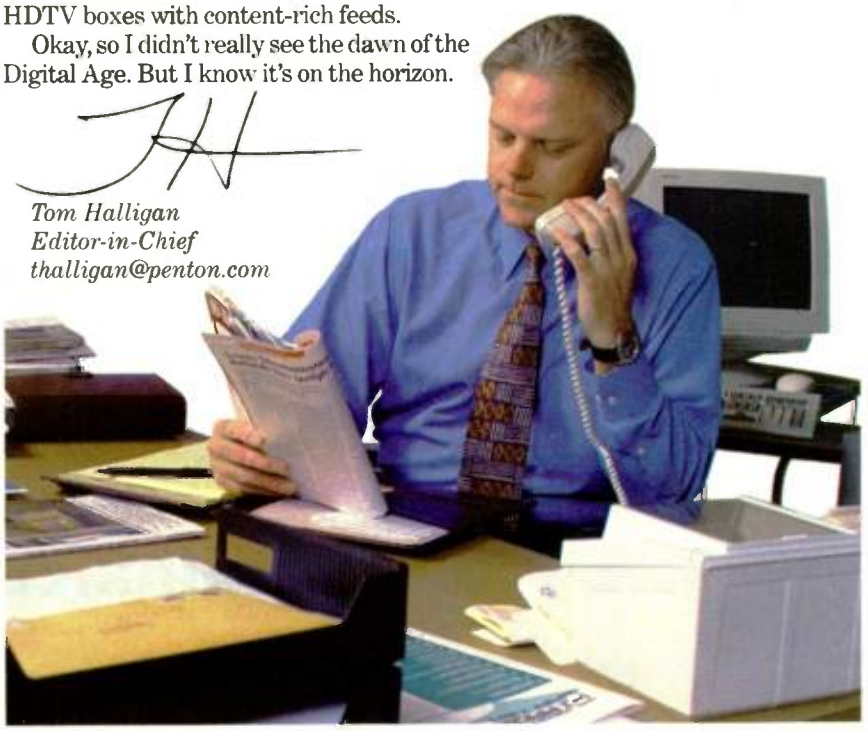
I don't know about you, but I awoke very early on Sunday, Nov. 1, to look out my window. I was there to witness the official dawn of the Digital Age. Funny thing, though—my scruffy backyard looked its regular brownish, nondescript self, barely lit by a waning, ho-hum November sun. And, when I quickly flicked the TV remote, there was only...analog. "Hey, what happened to the Digital Age?" I snapped to myself. I'd been anticipating this day for months. Newspapers, magazines, and TV told me it was coming. Even the Oct. 26 cover of *Business Week* screamed, "Digital D-Day" in big type. So, what happened?

As you know, Nov. 1 was the day when the government-mandated switch to digital broadcasting went into effect. To jump into the Digital Age, however, I would have had to pony up about $8000 for the HDTV and $1500 for a digital tuner set-top box. That doesn't even count the cost of paying a moving company to pick up and deliver the 250-lb., 4-by-4-ft. behemoth. Even if I tapped into my son's college fund to partake in the Digital Age, there are only a handful of TV networks offering very limited broadcasts in digital format. What's wrong with this picture?

Again, hype supercedes reality. A pure digital broadcast on an HDTV box is outstanding. Colors are vibrant, shades are pronounced, and you can see the fine details of a face, hand, or any other object. Couple that with a quality, surround-sound audio system and you're in multimedia heaven. But, there are problems. You have to play with the antenna to zero in on the signal. And, because digital signals are affected by obstructions such as tall buildings, they can vanish or freeze. The upside of this is that consumers are becoming aware of technical conditions and terms like "multipath," the "cliff effect," and "graceful degradation."

The real dawn of the Digital Age for consumers will kick in maybe five years from today, when the entry price point is more realistic. The chips alone for an HDTV set account for some $2000 of the total price. When Moore's Law kicks in and mass production brings economics into the process, prices will drop. But, history says the price will have to go below the $500 mark before consumers start scrapping their analog boxes for HDTVs. And, content providers won't invest in producing digital content until there's a mass market of consumers equipped to receive digital broadcasts. Finally, there's the ongoing battle among the cable, network, software, and Internet companies, along with equipment and computer manufacturers and others—all of whom want the masses glued to millions of HDTV boxes with content-rich feeds.

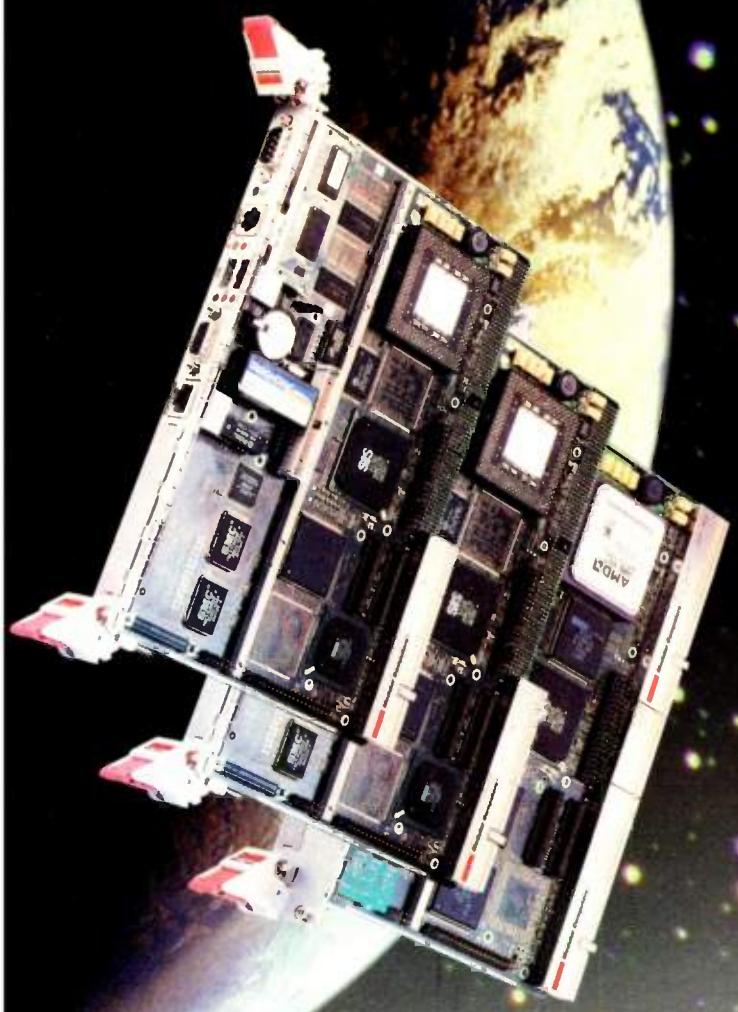
Okay, so I didn't really see the dawn of the Digital Age. But I know it's on the horizon.



*Tom Halligan*
*Editor-in-Chief*
*thalligan@penton.com*

# No-Limits Multiprocessing for CompactPCI.

## When you need high performance CompactPCI multiprocessing... it's time for a PEP talk.



PEP, the company that delivers maximum computing performance and functionality, does it again with no-limits multiprocessing for CompactPCI. For starters, our new CP611 offers:

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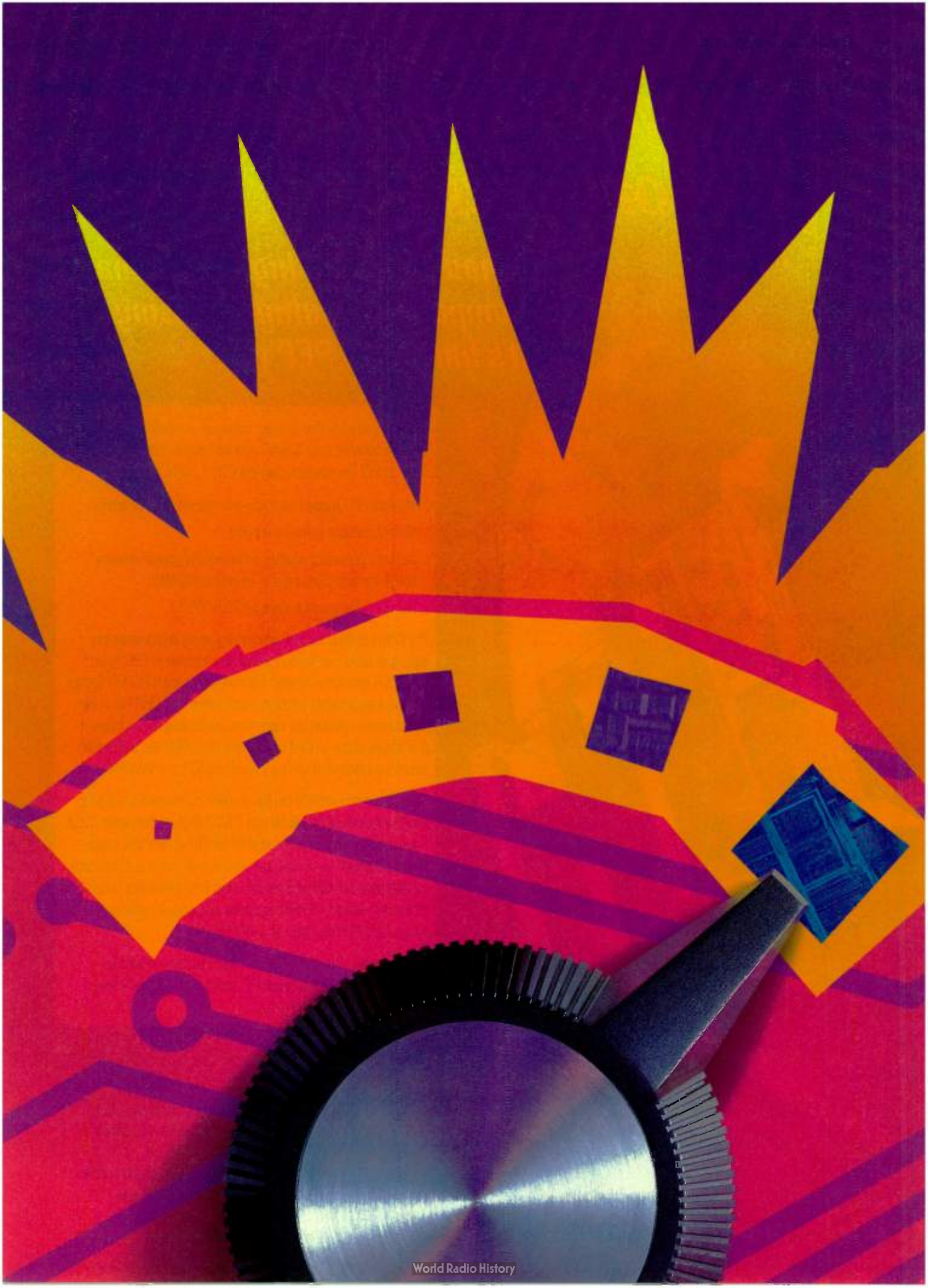

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# Acronyms Revisited?

A few issues ago (*ELECTRONIC DESIGN*, Sept. 1), I penned an article on acronyms. To my delight, and somewhat surprise, I was inundated with e-mails. As it turns out, I'm not the only one with such disdain for the use of acronyms. But, before we get into that subject again, let me clarify one point.

That earlier article referred to IP and PC as acronyms, as opposed to abbreviations. While technically this may be incorrect, nowadays we tend to use the two terms interchangeably. Some continue to dispute this point. But, I submit that whether you call something an acronym or an abbreviation, the problem is still the same: We often use these terms without really knowing what they mean.

Granted, this stems from the fact that there is typically more than one definition for a specific acronym. But as Jim Storm, chairman of Qwk Inc., Reno, Nev., explains, "We have brought most of the clutter on ourselves. The people who came up with ATM must have known it already meant automated teller machine to millions of people. Or, what about EDA? A check in *Webster's New World Dictionary* defines it as the acronym for 'Economic Development Administration,' which most likely predated the term electronic design automation by quite a number of years."

**CHERYL AJLUNI**
ELECTRONIC DESIGN AUTOMATION

But, this is only part of the story. Many people use these acronyms to make themselves sound smarter than they really are. You know what I'm talking about. You've just started a new job and you feel slightly out of place. So, you listen and pick up on the acronyms being used around you. You learn to "talk the talk," even if you can't yet "walk the walk."

If, by accident, you use an acronym incorrectly, no problem. Someone corrects you and you make sure to use it the right way the next time. But, there's an even more sinister use of acronyms lurking out there. It exists in the people who are eager to use as many as they can to, as one German reader put it, "impress the astonished crowd with their specialist knowledge. What they really prove is that they don't know the first thing about the topic they're discussing."

Which brings me to my next point. As far as I can tell, acronyms do little more than create a lot of confusion and make reading written material difficult. Half the time, they're not even used the way they were originally intended. So, what's the point? I guess you could argue that they save a few keystrokes here and there. To that I say, "Hey, this is the computer age. There's a little something called copy and paste. Learn to use it!"

Then again, on days when I'm feeling especially cynical, I start to imagine that there's another reason we use acronyms. In my Dilbert-like vision of the world, I imagine a grouchy, maniacal, and somewhat mentally challenged manager. He's sitting in his office, trying to think of something he can do to make his employees' lives miserable. As the light bulb appears above his head, it suddenly dawns on him that he can best torment his employees by coming up with a new way of communicating with them. All he has to do is use a secret code. He decides to call this code, "Acronyms." Then, he laughs so hard that he falls out of his seat and knocks himself unconscious.

I'll leave it to you to decide which version to believe. In the meantime, we can all help minimize the confusion. At the very least, we should require authors to define an acronym when it is first used. We might also try bolding the acronym, along with its definition, for easy reference.

Just in case that doesn't work, I've decided to start a support group for those people who are fed up with the acronym problem. I think I'll call it, "Acronym Haters Anonymous"—AHA for short! Be sure to look for me at the first meeting. I'll be the one in the back who says, "Hi, my name is Cheryl and I'm an acronymaholic." Until then, you can reach me at *cjajluni@class.org*.

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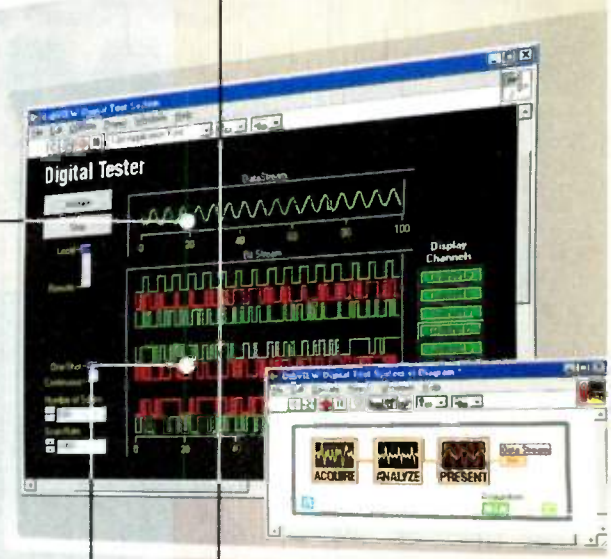


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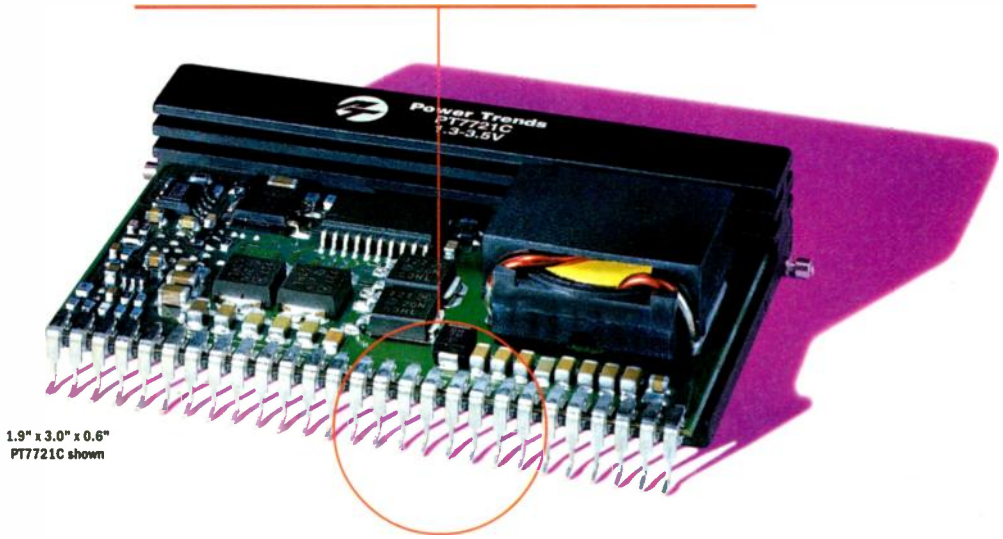


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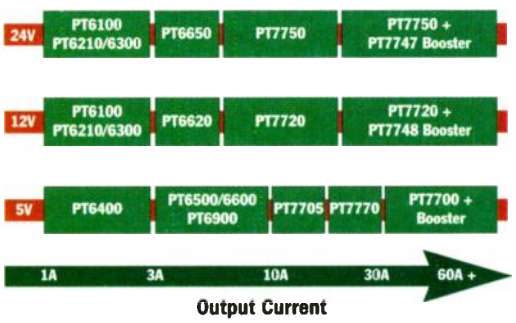


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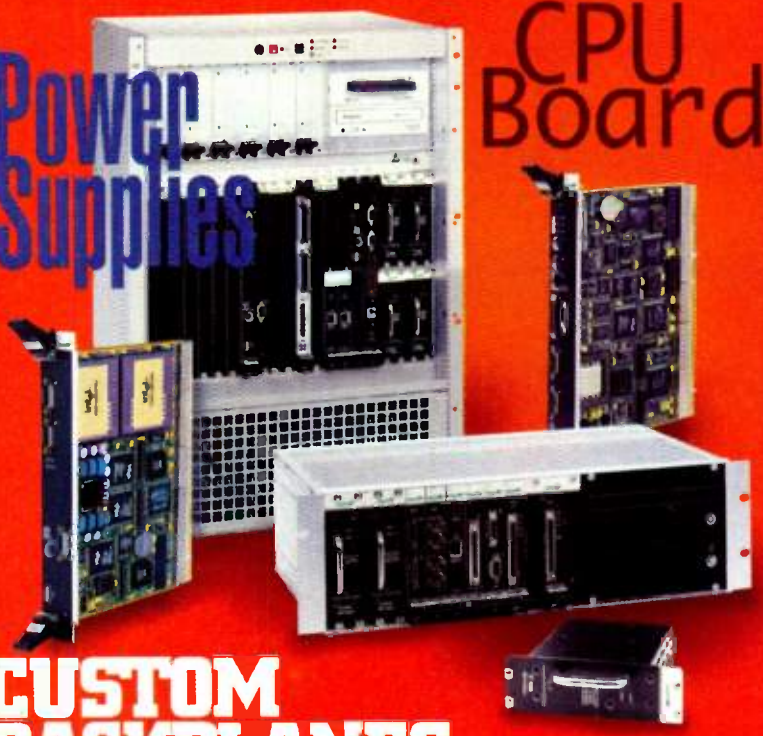

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# Networking Startup Brings Low-Cost Fiber Equipment To Desktop

As part of the drive to bring fiber optics all the way to the desktop, Gemflex Networks, Vancouver, B.C., Canada, a LAN-equipment manufacturer, announced its plans to provide low-cost fiber-optic switches and media converters exclusively with the VF-45 fiber interface. The company will offer a complete line of 10- and 100-Mbit media converters, transceivers, and switches beginning in the fourth quarter of 1998. The products are positioned to be priced up to 50% lower than any fiber-optic electronics equipment to date.

IT managers are struggling with enterprise bandwidth needs and the uncertainty over the ability of existing copper cabling systems to handle gigabit speeds and beyond. As a result, fiber LAN systems that capitalize on new fiber alignment technologies are positioned for explosive growth. According to Vincent Wong, president of Gemflex, the enabling technology behind the high-speed products is the VF-45 fiber interface, which allows extremely robust fiber connections at new price parameters. This, he believes, has radically changed the economics of fiber.

The VF-45 interface is a standards-compliant small-form-factor fiber interface currently used in the Volition Cabling System created by 3M. The interface, which is the next-generation fiber connector most widely adopted by end users, enables fiber-networking solutions to finally be cost competitive with enhanced copper.

In the past, fiber-networking equipment was one of the single biggest expenses associated with using fiber in the LAN. Now, some predict the fiber LAN market to grow by as much as 20% per year with the advent of new cabling systems and electronics based on the VF-45 solution. With 3M's development of a complete, industry-wide solution, Gemflex Networks was convinced to solely concentrate on VF-45-compatible products. As Wong explains, "the infrastructure supporting VF-45 is in place with patch cables, cleaning kits, and patch panels currently shipping and numerous customers worldwide using 3M's new cabling system. The VF-45 interface is rapidly emerging as the industry standard for next-generation fiber."

Contact Steve Swift at (604) 303-9752 ext. 105; e-mail: *steves@gemflex.com*; *www.gemflex.com*. PM

# BiMOS3D Process Being Readied For Motion-Control ICs

Hoping to address the integration and cost issues of mass storage ICs, Philips Semiconductors has added power capability to its proven 0.56-mm l-effective BiMOS3 process, which the manufacturer has been using to build highly integrated TV chips. The result is a smart-power BiMOS3D process that combines high voltage lateral transistors with high density digital functions, and analog power devices on a single die.

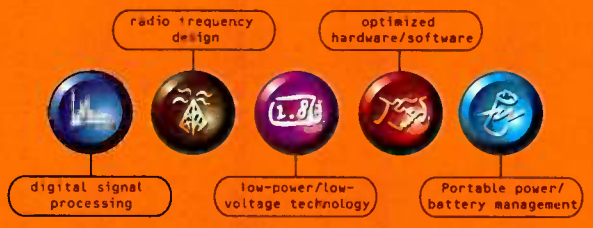
With BiCMOS3D, logic gates are implemented in CMOS, while the output stages use bipolar and lateral DMOS transistors to accommodate high-current, high-voltage and high-power devices. According to Arnaud Moser, marketing manager for motion-control ICs at Philips Semiconductors, incorporating power components adds only few masks, thereby minimizing the impact on wafer cost. Moreover, adds Moser, the utilization of the core process allows the reuse and sharing of a large library of functional blocks.

Because high-density smart-power processes are vulnerable to latchup, special care was taken to eliminate this problem in BiMOS3D, says Moser. In this latchup-prevention scheme, which also can obtain the required breakdown voltage, the power transistors are isolated from other components by p isolation rings.

Buried p and n layers are included to minimize the injection of minority carriers into the substrate, thereby lowering the parasitics. Also, the thickness of the epitaxial layer in BiMOS3D is optimized so that the breakdown voltage of the critical component, power LDMOS, is 25 V, which is suitable for 12-V applica-

*(continued on page 28)*

# Let's...

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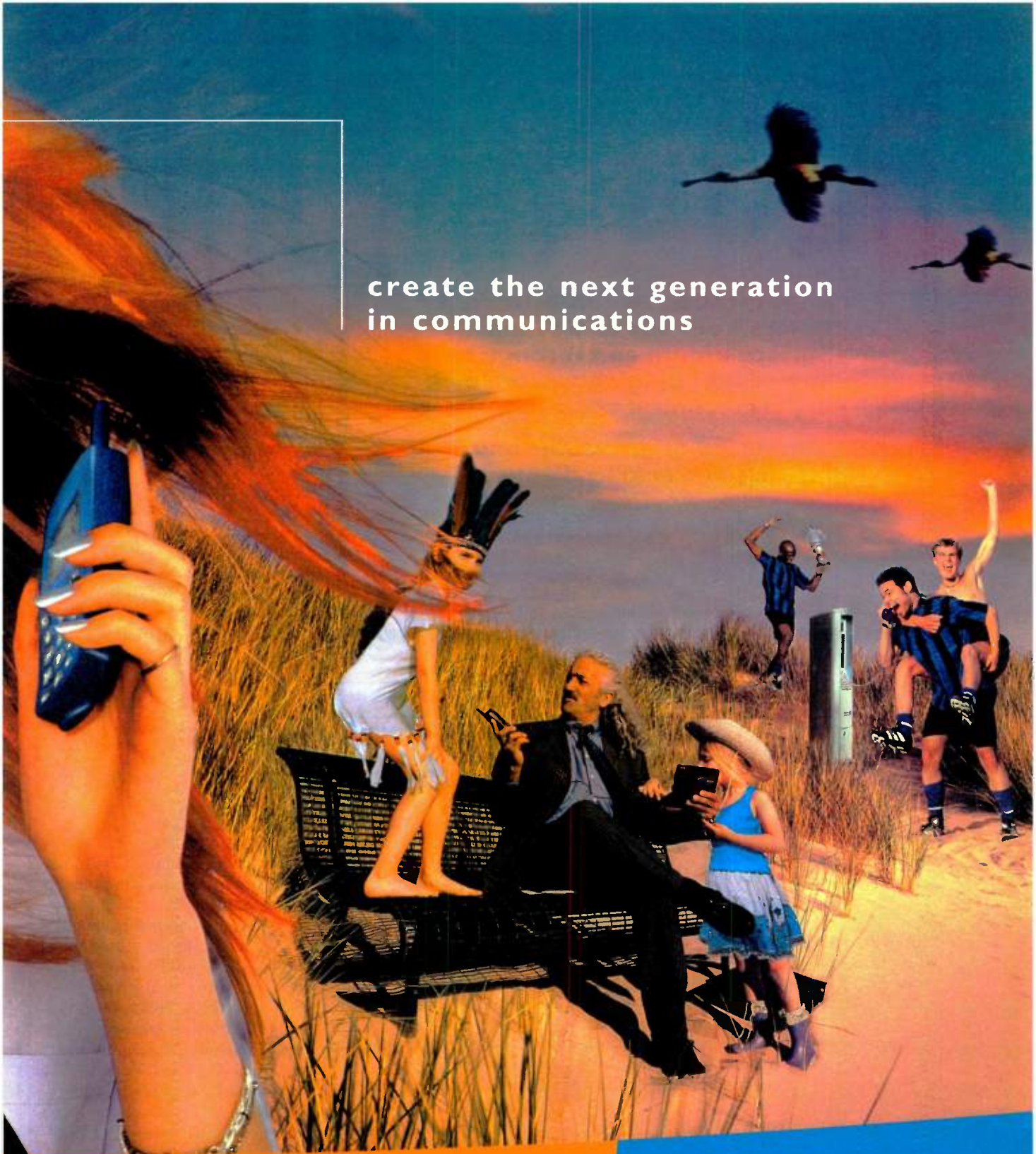


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*(continued from page 25)*

tions. Other features of the process include power extended-drain PMOS (EPMOS), high ohmic polysilicon resistance, high-voltage high-value capacitance, and high immunity against latchup and crosstalk.

Based on this smart-power process, several system-level ICs are under development, with plans for sampling in the second quarter and production by the end of 1999. One such chip, designated TDA6001, is a 12-V spindle and voice-coil-motor (VCM) driver combination for 3.5-in. disk drive. Also integrated are on-chip 12-bit DAC, multiplexer, bandgap voltage reference, regulators, oscillator, buffers, digital position sensing, programmability, and other features to deliver a highly integrated solution for HDD motion-control applications.

For more information, call (408) 991-4484; Internet: *www.semiconductors.philips.com.* AB

# Voice-Transmission-Standard Project Initiated By TIA

The Telecommunications Industry Association announced a new project for creating a voice-transmission performance standard that will include products used for Internet telephony. The scope of the new standard will expand on TIA/EIA-579-A, "Telecommunications Telephone Terminal Equipment Transmission Requirements for Digital Wireline Telephones." As such, handset, headset, and hands-free audio performance will be included. Also, IP-based and PCM-based interfaces will be covered, with codecs of 64 kbits/s and lower.

Efforts will be made to ensure interoperability and quality of service definitions with IP network standards organizations, such as the Internet Engineering Task Force (IETF). Contact T-41.3 chairman Steve Whitesell at (732) 544-3017, or e-mail at: *swhitesell@lucent.com.* RE

*Edited by Roger Engelke*

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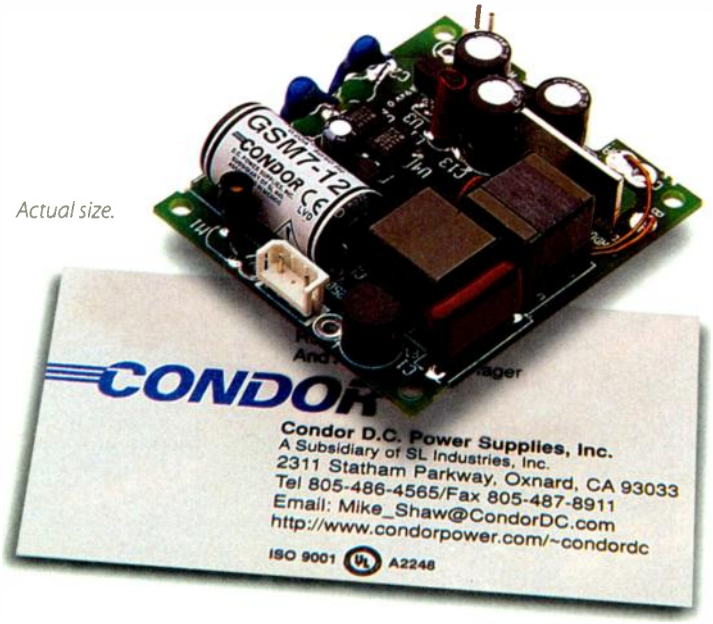


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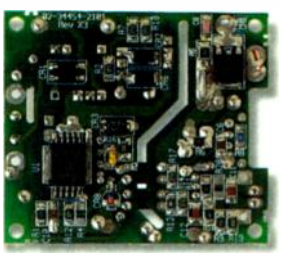

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# Ultra-Small MEMS Combination Lock Promises To Foil The Best Computer Hackers

Its developers call it "the world's smallest combination lock." It's a miniscule microelectromechanical-system (MEMS) device developed at Sandia National Laboratories, Albuquerque, N.M. And, it promises to build a virtually impenetrable computer firewall that even the best hackers can't defeat.

The Recodable Locking Device is so small that it takes a microscope to see it *(see the photo)*. It consists of a series of notched gears that move to the unlocked position only when the right code is entered. According to its developers, "It's the first known mechanical hardware designed to keep unwanted guests from breaking codes and illegally entering computer and other secure systems."

"Computer firewalls have always been dependent on software, which means they are 'soft' and subject to manipulations," says Larry Dalton, manager of Sandia's high-integrity software systems engineering department. "Our device is hardware and it's extremely difficult to break into. You have one and only one chance in a million of picking exactly the right code, compared to a one in 10,000 chance, with many additional chances, in most software firewalls. After one failed try, this new device mechanically shuts down and can't be reset and reopened except by the owner."

## Patent Filed

Sandia, a U.S. Department of Energy (DOE) national security laboratory, recently filed for a patent for the mechanism. The first working units were fabricated in July. The Sandia team, which is refining the device and performing reliability tests, expects to have it ready for commercialization in about two years. Once it's perfected, a commercial partner will be tapped to produce and sell it.

"The Recodable Locking Device should be of great interest to businesses and individuals who have computer networks, have sites on the Web, or require secure computers," says Frank Peter, an engineer who designed the device. "It would make it virtually impossible for break-ins to Web sites, like what occurred with *The New York Times* in September," he adds. (Hackers broke into the *Times'* electronic edition in mid-September and shut it down for several hours.)

Dalton says he's had the notion of the device for three years, calling it the "digital isolation and incompatibility" project. Digital was for the digital world. Isolation and incompatibility are important concepts in "strong links," which are mechanical locks used as safety devices in weapons. He turned to Sandia's electromechanical engineering department, headed by David Plummer, to make the design because of that group's expertise in strong links, as well as its ability to design using MEMS technology.

## Simple System

It took Sandia about three months to go from concept to the final design. Explains Peter, "Based on a code-storage scheme used in existing weapon surety subsystems, we were able to design a very simple device. And, it's the simplicity of the device that makes it easy to analyze from a vulnerability standpoint."

A working model was built consisting of a series of six code wheels, each less than 300-µm in diameter, driven by electrostatic comb drives that turn electrical impulses into mechanical motion. The lock's owner sets a lock combination to any value from one to one million. The entire device is about 9.4 by 4.7 mm, roughly the size of a button on a dress shirt.

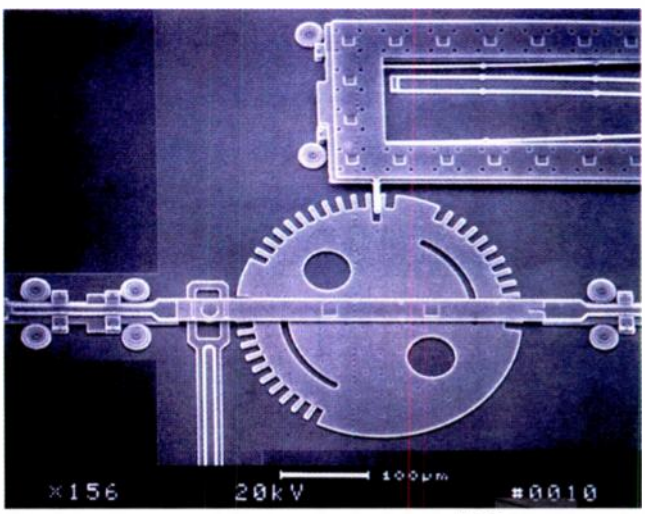
The Recodable Locking Device consists of two sides: the user side and the secure side. To unlock the device, a user must enter a code that identically matches the code stored mechanically in the six code wheels. If the user makes even one wrong entry—and close doesn't count—the device mechanically "locks up" and doesn't allow any further tries until the owner resets it from the secure side.

The six gears and the comb drives can be put on a small chip and incorporated into any computer, computer network, or security system. Because the chip is built using IC fabrication techniques, hundreds can be constructed on a single, 6-in. silicon wafer, making the chip very inexpensive to produce.

"Besides being a deterrent to hackers, the device has other security applications," Peter says. For example, controlled information could be made available only in a window of opportunity. The information owner could tell the party needing the data that he or she has five minutes to enter in a specific code and gain access. Then, after the five minutes is up, the code would be reset and access denied.

A variety of potential safety applications also are possible with the device. The mechanism can confirm that a critical system is operating as expected. If it detects a problem, it will not permit execution of a function. In this safety capacity the device could, for example, ensure that a radiation therapy machine delivers the correct radiation dosage.

"This device has a powerful potential—one that is readily




**This photo shows one of the six code wheels in the MEMS combination lock developed by Sandia National Laboratories. The wheel, pictured here in the enabled position after the correct code was entered, is 300-µm across—about the size of the period at the end of this sentence.**

understood by most everyone," Dalton says. "I've been told by the Department of Defense that this is the first real technical advancement in information security that they've seen in a long time."

Computer crime is a growing problem nationwide. The Computer Security Institute, together with the U.S. Federal Bureau of Investigation, recently surveyed 520 security practitioners in U.S. corporations, government agencies, financial institutions, and universities. Results showed that 64% of the respondents reported computer security breaches within the last 12 months. Although 72% said they suffered financial losses from these breaches, only 42% were able to quantify their losses—estimating them to be more than $136.8 million.

For more information, contact Sandia's Larry Dalton at (505) 844-2520; e-mail: ljdalto@sandia.gov; David Plummer at (505) 845-9564; e-mail: dwplumm@sandia.gov; or Frank Peter at (505) 844-1763; e-mail: fjpeter@sandia.gov.

**Roger Allan**

# New Version Of RACEway Architecture Boosts Bus Bandwidth To 1 Gbyte/s

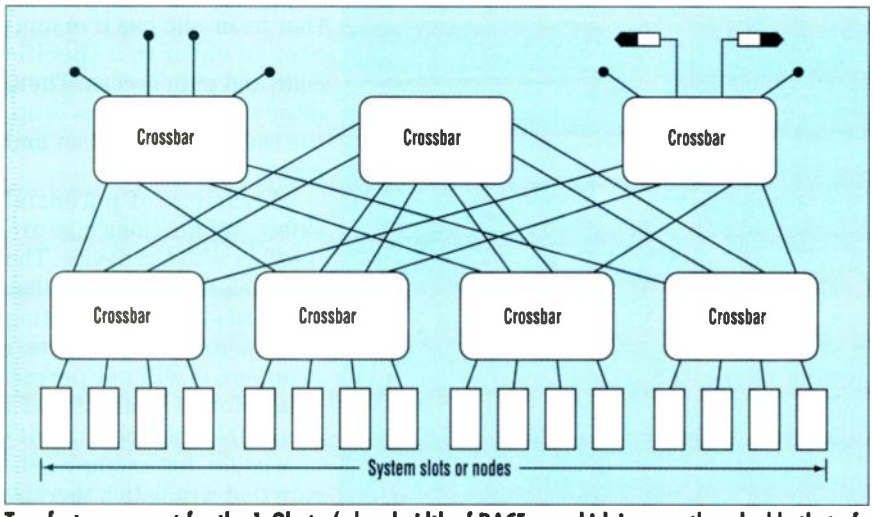
In the demanding realm of high-end multicomputing, faster data movement is the name of the game. High-speed secondary bus technologies are one way to achieve that when the backplane speeds of VME and PCI aren't enough. Among the more widely used secondary buses is RACEway, a circuit switched fabric offering 480-Mbyte/s aggregate bandwidth via a six-port interface chip. With an eye toward evolving RACEway for greater performance and function, Mercury Computer Systems, Chemlsford, Mass., has introduced a new version of the open ANSI standard, called RACE++.

"It's managed evolution of RACEway," says Barry Isenstein, vice president of Mercury's advanced technology group. "Yet, it gives existing RACEway third parties a way to move forward. It lets you do more in the same power budget." While RACE++ is Mercury's own implementation of the new scheme, the company is already sharing the technology with its RACEway partners. The technology spec also is available on Mercury's web site, and the company eventually plans to make RACE++ an open ANSI standard.

RACE++ increases the aggregate bandwidth of RACE crossbars to 1 Gbyte/s—more than double that of the current RACE crossbar. At the system level, bisection bandwidth improvements over the current RACE architecture range from two to four times. System-processor scalability can increase up to four times.

RACE++ is backward-compatible with the current RACE architecture. It's also backward-compatible with the 60-plus products made by more than 45 third-party adopters of the industry-standard RACEway Interlink (ANSI/VITA 5-1994).

The crossbar ASIC—the key component of the interconnect fabric—has an eight-port crossbar in RACE++, compared to six ports in the current-generation RACE architecture *(see the figure)*. This, plus a modest increase in data rates from 40 to 66 MHz, further extends per-ASIC bandwidth. Beyond higher data speed and greater system bandwidth, RACE++ includes enhancements to scalability, routing, and endpoints.




**Two factors account for the 1-Gbyte/s bandwidth of RACE++, which is more than double that of the original specification. The key—the crossbar ASIC—has eight ports rather than the six in the RACE architecture. An increase in data rates from 40 to 66 MHz further extends per-ASIC bandwidth. RACE++ also includes enhanced scalability, routing, and endpoints.**

## 4000 Processors Per System

On the scalability side, RACE++ lets designers build larger computing systems with mixes of DSP, RISC, and specialty processors. Whereas the current RACE architecture supports systems containing 1000 processors, RACE++ boosts this number to more than 4000 processors in one system.

The RACE architecture features adaptive routing, which allows data to make real-time choices of the least congested data paths between the source and destination. Adaptive routing is executed entirely in hardware, so it doesn't incur any system or user software overhead. RACE++ greatly extends this capability. In the current generation of RACE, two out of six ports can implement adaptive routing. In RACE++, all eight ports can implement it.

"You'll be able to choose adaptive routing like in the past. But if you're using RACE++, you might see a throughput increase even at 40 MHz because of the topology and routing changes," says Isenstein. "The software and peripherals attached wouldn't have to change. The only reason the hardware would change is if you wanted to take advantage of the 66-

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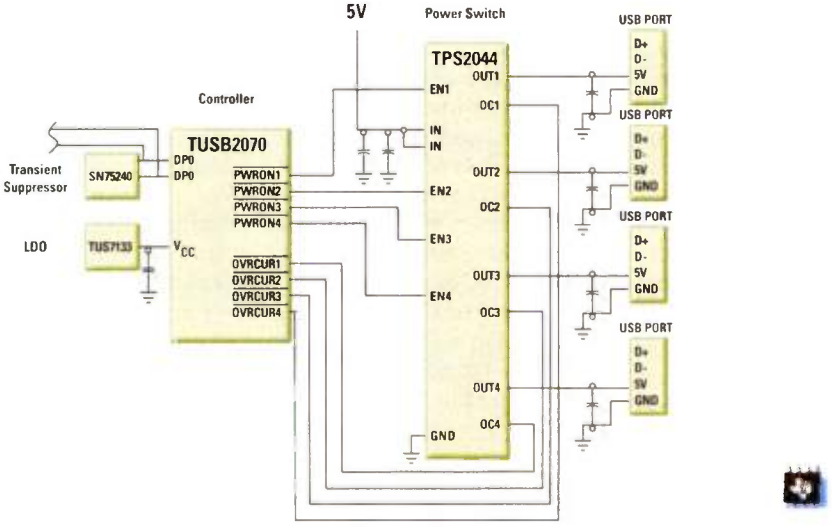


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MHz capability. Basically, it's the same signals and the same signaling. In the embedded environment, 66 MHz isn't super fast. But in mission-critical systems, it's important that this stuff work reliably. It's rock solid at 66 MHz using off-the-shelf FPGAs. A switch fabric that ties things together through multiple layers of boards, backplanes, and many connectors in between needs reliable signaling."

## Handles For Adaptive Routing

In the RACE architecture, endpoints are sources and destination terminations for data transfers. These include arrays in local memory, shared-memory buffers, and foreign bus address spaces. They need not be limited to an intelligent processor's memory or bound to any specific process. RACE++ extends the concept of endpoints to encompass the crossbar ASIC itself. This permits designers to include handles for users to control adaptive routing and new ways to reconfigure routing in real time.

RACE++ increases data bandwidth while retaining the advantages of a switched-fabric data backbone. This topology eliminates isolated bottlenecks prone to congestion, provides multiple paths between source and destination, and allows data to travel through a richly connected, multidimensional mesh/fabric. It also provides the determinism required for real-time computing.

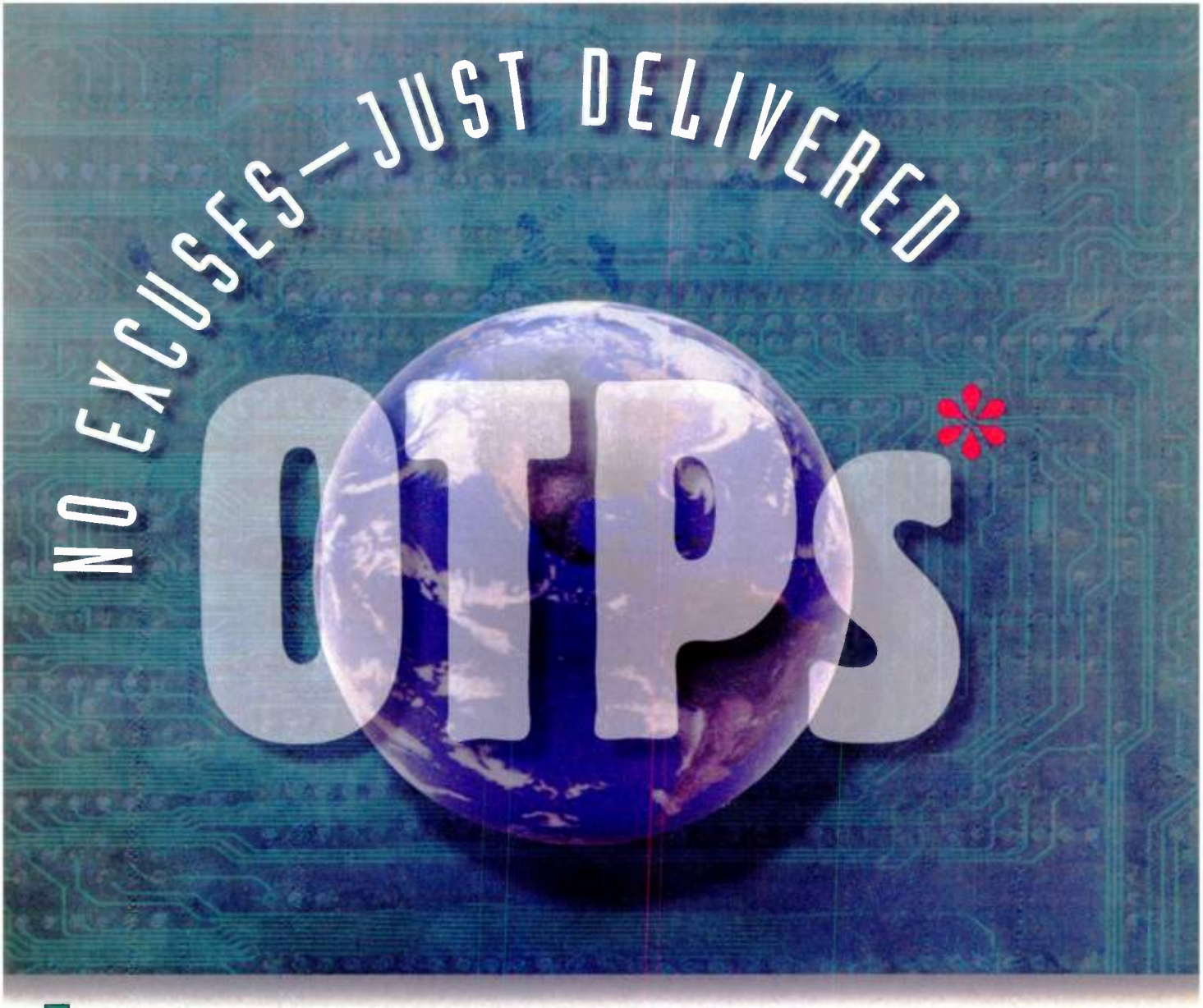
This increased bandwidth enhances the RACE design philosophy of offering more ports per board, rather than driving fewer ports at problematic, high speeds. The RACE scheme also avoids the need to stress the thermal envelope of individual components in order to achieve higher speeds. In fact, the RACE++ ASIC delivers its 1-Gbyte/s bandwidth at a power cost of only 1 W.

Mercury is working with existing and potential RACEway partners and RACE customers to effect a smooth transition to the RACE++ architecture. A number of board and systems vendors offer products incorporating the RACEway standard Interlink. Among these are Blue Wave Systems, Carrollton, Texas; Catalina Research Inc., Colorado Springs, Colo.; Celerity Systems Inc., Cupertino, Calif.; ICS, Gloucester, Ontario; Micro Memory Inc., Chatsworth, Calif.; Myriad Logic, Silver Spring, Md.; Pentek Inc., Upper Saddle River, N.J.; Ramix Inc., Chatsworth, Calif.; Synergy Microsystems Inc., San Diego, Calif.; and VMETRO Inc., Houston, Texas.

All current Mercury products, including the VantageRT and OmniStream PCI solutions, as well as the MultiPort and RACE Series VME product families, will evolve to support RACE++. Mercury also will introduce new RACE++ products.

Mercury anticipates the introduction of initial RACE++-based products in early 1999, with production shipments available in mid-1999. For more information on RACE++ and the RACEway open standard, contact Mercury Computer Systems at (978) 256-1300 or www.mc.com.

**Jeff Child**

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| 68HC705P6A | 4.6K | 176 | 28 | M68ICS05P | KITMMEVS05P6A | KITMMDS05P6A |
| 68HC705C8A | 8K | 304 | 40,44 | M68ICS05C | KITMMEVS05C | KITMMDS05C |
| 68HC705C9A | 16K | 352 | 40,44 | M68ICS05C | KITMMEVS05C | KITMMDS05C |
| 68HC705B16 | 15K | 352 | 52,64 | M68ICS05B | KITMMEVS05B | KITMMDS05B |
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# TECH INSIGHTS

**Previewing the latest developments at the 1998 International Electron Devices Meeting**

# Annual IEDM Conference Offers A Look At Leading-Edge Electron Devices

*The "Shrink-Everything" Syndrome Hits Devices Smack In The Substrate.*

Where do designers congregate to catch a glimpse of the electron devices that will be heading their way? One sure bet is this year's 44th annual International Electron Devices Meeting (IEDM), to be held at the San Francisco Hilton and Towers Hotel, Dec. 6-9. Its rich technical program of 37 sessions covers a wide range of electron devices and the processes and tools that make them. What are some of the highlights 1998's attendees can expect to see? Well, there's the fastest three-terminal semiconductor ever built (350 GHz). New developments are afoot using copper in computer chips. And, a session devoted to device-manufacturing issues has been added. Look for a lot of activity centering around transistors suitable for cheap, flexible, plastic flat-panel displays.

The technical program begins on Monday, Dec. 7 *(see the table)*. It is preceded by two short, all-day courses on Sunday, Dec. 6: "Reliability for Logic and Memory Technologies" and "Next-Generation TCAD: Models and Methods." On Monday at 9:00 a.m., the plenary session will consist of three presentations: "Trends in Semiconductor Equipment, Materials, and Processing Technology"; "Executing System on a Chip: Requirements of SOC Implementation"; and "Intercontinental Migration of Dominant Technologies."

So turn the page, and let Technology Editors Dave Bursky, Ashok Bindra, and Cheryl Ajluni take you on the grand tour.

## 1998 INTERNATIONAL ELECTRON DEVICES MEETING

**Session 1: Plenary Sessions—1.1: Executing system on a chip: Requirements of SOC implementation; 1.2: Intercontinental migration of dominant technologies; 1.3: Trends in semiconductor equipment, materials, and processing technology**

| | | | | | |
|---|---|---|---|---|---|
| **Session 2:** Detectors, sensors, and displays: image sensors | **Session 3:** Quantum electronics and compound semiconductor devices: power | **Session 4:** Modeling and simulation: compact modeling | **Session 5:** Solid-state devices: single electron devices | **Session 6:** Device interconnect technology: STI/ retention time | **Session 7:** CMOS devices and reliability: ultra-thin gate oxide reliability |
| **Session 8:** Integrated circuits: high performance CMOS/BiCMOS | **Session 9:** Quantum electronics and compound semiconductor devices: high electron mobility transistors | **Session 10:** Detectors, sensors, and displays: thin-film transistors | **Session 11:** Modeling and simulation: interconnect modeling | **Session 12:** Special manufacturing session: advanced process technology | **Session 13:** Integrated circuits: advanced DRAMs and FRAMs |
| **Session 14:** Device interconnect technology: high k gate dielectrics/ metal gate | **Session 15:** CMOS devices and reliability: low-voltage CMOS: SOI and DTMOS | **Session 16:** Quantum electronics and compound semiconductor devices: quantum effect devices | **Session 17:** Detectors, sensors, and displays: Micro Electro Mechanical systems | **Session 18:** Modeling and simulation: process modeling | **Session 19:** Solid state devices: on-chip inductors |
| **Session 20:** CMOS devices and reliability: MOS physics and characterization | **Session 21:** Device interconnect technology: gate dielectrics | **Session 22:** CMOS devices and reliability: advanced CMOS devices and technology | **Session 23:** 1998 IEDM evening panel discussion | **Session 24:** 1998 IEDM evening panel discussion | **Session 25:** Quantum electronics and compound semiconductor devices: heterojunction bipolar transistors and photo-detectors |
| **Session 26:** Solid state devices: SiGe and high power devices | **Session 27:** Modeling and simulation: process/ device model characterization and applications | **Session 28:** Special manufacturing session: advanced device and simulation | **Session 29:** CMOS devices and reliability: metal gate and alternate gate dielectrics | **Session 30:** Device interconnect technology: capacitor materials for advanced memories | **Session 31:** Device interconnect technology: advanced interconnects |
| **Session 32:** Detectors, sensors and displays: emissive display technologies | **Session 33:** Modeling and simulation: advanced device modeling | **Session 34:** CMOS devices and reliability: analog CMOS and hot-carrier reliability | **Session 35:** Solid state devices: rf devices | **Session 36:** Integrated circuits: flash memory technology | **Session 37:** Device interconnect technology: device technology |

CONFERENCE PREVIEW

# Hit Up IEDM For Gigabit And Denser DRAMs And Merged Logic/Memory

*Advances In DRAM Storage Cells Push Capacities To 16 Gbits, While Lower-Resistance Interconnects And New Structures Let DRAMs And Logic Merge.*

**Dave Bursky**

With an eye set on reaching memory capacities of 16 Gbits on a chip and operating speeds of 2 GHz for logic circuits, this year's International Electron Devices Meeting (IEDM) portends major advances in chip-fabrication technology. Of course, presentations will cover a much broader scope, including advances in nonvolatile memory cells, metallization and dielectric systems, and quantum electronics.

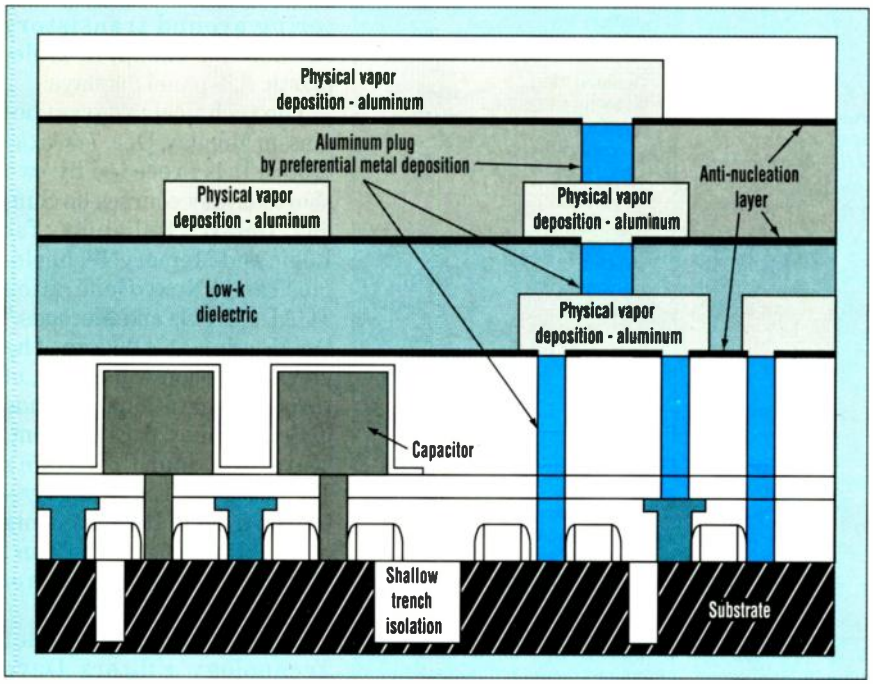
Dynamic RAM storage-cell structures have long been a proving ground for process-technology improvements. This year's DRAM papers are no exception. In a "late-news" paper in Session 31 (31.7), researchers from Samsung Electronics Co., Kyungki-Do, Korea, show off cell structures that they feel would be good candidates for use in 16-Gbit DRAMs. Still many years from production, the test cells do show that enough capacitance can be obtained from structures fabricated with 0.12-µm and smaller minimum features.

The scheme employs a preferential metal-deposition process for aluminum that completely fills deep, small contacts and via holes. One advantage is its need for a preceding barrier-layer deposition step, which forms a diffusion barrier to prevent the aluminum from going into undesired regions. The use of low temperatures (typically less than 450°C) minimizes the aluminum diffusion.

An anti-nucleation layer covers the top of the contacts and withstands the hydrogen-induced reducing environment during the aluminum-deposition process (done with chemical vapor deposition, or CVD). The resulting effect of this layer is that aluminum growth is suppressed on the upper edges of the contacts, while the aluminum plug forms inside the contact opening *(Fig. 1)*. High-aspect-ratio structures, with ratios of up to 20:1, can be filled with this process. Using a titanium/titanium-nitride layer prior to aluminum deposition prevents any "spiking" of the aluminum through the bottom of the contact region. The Samsung researchers believe the same approach can be used with copper deposition.

Session 13 focuses on advances in DRAMs and ferroelectric RAMs. Another Samsung paper (13.2) examines a new DRAM cell structure that researchers feel would fit 4-Gbit and denser memory chips. The cell eliminates the critical lithography between the memory-cell buried contact (BC) and the storage-node polysilicon by merging formation processes into a single process. In normal buried-contact formation, a deep, vertical etch step must be done to open the contact window. But, deep etches on structures with small features can cause undercutting of the key structures, leading to poor performance or early failure. By merging the two process steps—creating the contact and depositing the polysilicon—researchers both eliminated undercutting and dealt with the smaller features to be used by next-generation DRAMs.

Instead of forming the buried contact first and then depositing the polysilicon storage material over the contact, the new approach initially builds up several layers. An interlayer di-




**1. The preferential deposition of aluminum for future 16-Gbit memory cells is possible. Thank Samsung Electronics for developing a conformal titanium/titanium-nitride layer that prevents nucleation of the aluminum at the top edge of the contact.**

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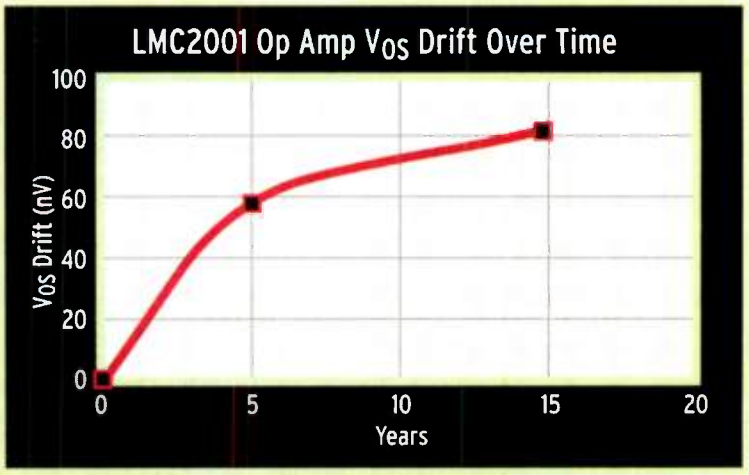




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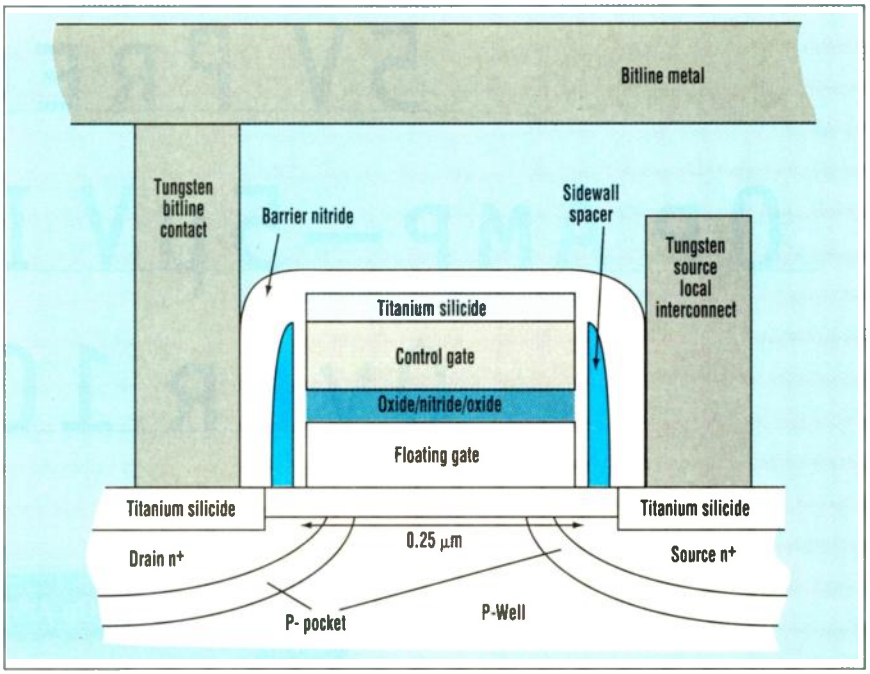
electric layer comes first, followed by a silicon-nitride/silicon-dioxide etch-stop layer. A thick interlayer dielectric (about 1 μm) follows. Next, the contact hole is etched through the thick dielectric, the etch-stop layer, and the underlying dielectric. This leaves the pad region of the memory-cell transistor exposed.

A single-step deposition of the contact and storage-node polysilicon then fills the deep contact hole formed by the etching. After deposition, the surface of the wafer is chemically, mechanically polished to remove all polysilicon except for the material that filled the trenches. The thick dielectric layer is then removed with a wet-etch step, leaving a "pillar" of polysilicon that forms the storage node. Lastly, a polysilicon sidewall oxide spacer can be formed on the sides of the pillar to further enhance the surface area of this storage node. When fabricated with 0.15-μm features, the capacitor area is about 1 $\mu m^2$. The total measured capacitance, with an oxide-equivalent thickness of about 3 nm of tantalum-pentoxide dielectric, is about 12.77 fF/cell at 1.2 V. If hemispherical grain enhancement is used, the capacitance can increase to about 25 fF/cell.

Examining trends in memory-cell approaches, an invited presentation by Toshiba Corp., Yokohama, Japan (paper 13.3), looks at the various planar and vertical memory-cell structures (both trench and stacked versions) developed thus far. Future market needs for low-cost, high-speed, and embedded-logic/DRAM requirements also get reviewed. The presentation focuses on the fully planarized trench capacitor cell and the 3D capacitor structure employing barium-strontium-titanate (BST) storage cells. Both are promising for gigabit-generation DRAMs.

To achieve gigabit densities, approaches are expected to include oxynitride as the gate dielectric and a combination polysilicon/metal-conductor structure, as well as cobalt-silicide, on gate electrode and source/drain regions. This will reduce sheet resistances. Using low-dielectric-constant interlayer dielectrics will reduce parasitic capacitances and crosstalk, while copper wiring formed by Damascene processing will minimize interconnect resistance.




**2. The use of shallow trench isolation by Toshiba in this NOR-type flash-memory cell permits the memory designers to reduce cell-to-cell spacing. They also can trim the cell size to just 0.44 $\mu m^2$ when fabricated with 0.25-μm design rules.**

As DRAM densities increase, the on-chip, word-line, resistance-capacitance delay often becomes a performance-limiting factor. To find a way around that potential problem, designers at Toshiba Corp., Yokohama, Japan, detail a polymetal approach for dual-gate CMOS circuits in next-generation 1-Gbit DRAMs and beyond. The polymetal scheme layers tungsten-silicon-nitride on top of polysilicon, with a coating of tungsten on top of the WSiN. The combination results in a sheet resistance of just 4.5 Ω/square for the word line, with a 40-nm-thick layer of tungsten.

For packing transistors closer, shallow trench isolation (STI) has become popular. But with DRAMs, companies like Mitsubishi Electric Corp., Hyogo, Japan, are concerned with the stress in the trenches and how it affects DRAM performance. In paper 6.3, Mitsubishi researchers describe techniques that lower the stress generated during oxidation steps, when layers such as the sacrificial oxide and gate oxide are deposited. The researchers then expect to be able to use STI processes down to feature sizes as little as 0.1 μm.

Still on the topic of stress, researchers at Samsung Electronics and NEC Corp., Tokyo, Japan, are presenting results in papers 6.4 and 6.5. Samsung focuses on the cumulative thermomechanical stress produced by shallow trench isolation for 1-Gbit and denser memories. NEC stays with the subject of sidewall stress in the trenches and its effect on data-retention time. When filled with oxide deposited by electron-cyclotron-resonance CVD, designers found that shallower and more tapered trenches provide better data-retention times.

As DRAMs get denser, refresh times stretch out, meaning the DRAM cells must maintain their data longer. In paper 6.7, researchers at Hitachi Ltd., Tokyo, Japan, delve into what happens when densities hit 1 Gbit and beyond. They found that by controlling the energy-level distribution of traps in the oxide, they could increase the storage-cell retention time. Reducing the space-charge-region field variation, together with the field itself, also helped improve the retention time.

Better cell capacitors are keys that can improve data retention. In Sessions 28 and 30, more than a half-dozen papers cover new capacitor structures and material combinations for 1-Gbit and denser memories. Hitachi Ltd., Tokyo, Japan, in paper 28.3, details the use of a 1.5-nm, equivalent-thickness, tantalum-oxide high-dielectric-con-

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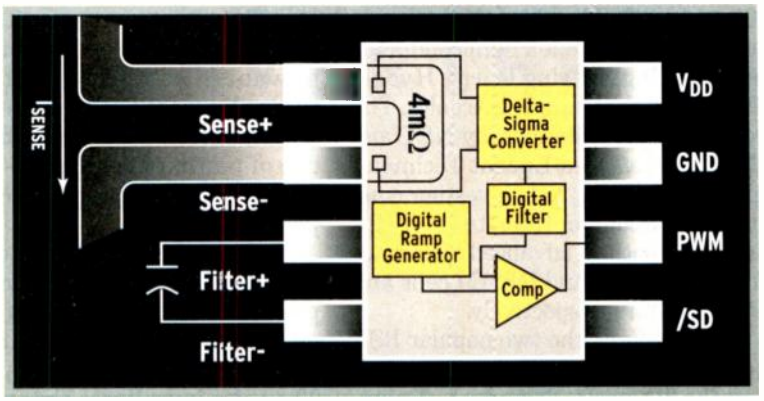


| Device | Range | Method | Speed |
|---|---|---|---|
| LM3812-1/7 | 1A/7A | High-side | Precision |
| LM3813-1/7 | 1A/7A | Low-side | Precision |
| LM3814-1/7 | 1A/7A | High-side | Fast |
| LM3815-1/7 | 1A/7A | Low-side | Fast |



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# ±0.5% CURRENT GAUGE WITH 4mΩ INTERNAL RESISTOR

National Semiconductor

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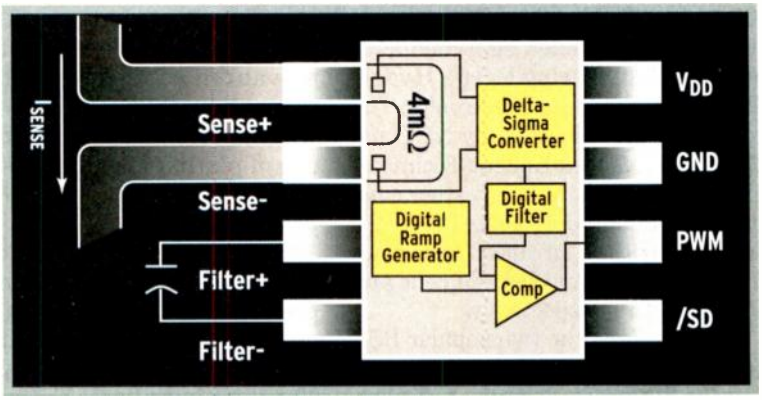


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In the first four papers in session 30, BST cell structures are discussed by Mitsubishi; Toshiba; Mitsubishi in conjunction with Ryoden Semiconductor System Engineering Corp., Hyogo, Japan; and Samsung Electronics. The remaining presentations, by NEC and Bell Laboratories/Lucent Technologies, Murray Hill, N.J., investigate using lead-zirconium-titanate (PZT) for the cell capacitor, advanced dielectrics for gate oxides, and DRAM cells and RF capacitors, respectively.

In examining the two popular BST capacitor structures—the planar cell and the 3D stack—Mitsubishi designers feel that the planar cell will be self limiting to chip capacities of 256 Mbits and less. The area required at higher densities would make the chips too large, which means the 3D stack cell structures will predominate for densities above 256 Mbits. The contact material also is critical, taking into account materials such as platinum, iridium, iridium-oxide, ruthenium, and ruthenium-oxide. For densities up to 1 Gbit, researchers feel that platinum, iridium, and iridium-oxide would be appropriate. At 4- and 16-Gbit densities, ruthenium and ruthenium-oxide would be more scalable.

Experimenting with an all-Perovskite capacitor (APEC) technology (30.2), researchers at Toshiba checked out how well the structure could scale down to feature sizes of 0.1 μm. The use of conductive Perovskite oxide (polycrystalline strontium-ruthenium oxide) as the top and bottom electrodes for the BST storage capacitor promises lower leakage currents. It also ensures less damage from a hydrogen-based process atmosphere, better thermal stability during BST film deposition and annealing, and higher reliability.

The joint presentation by Mitsubishi and Ryoden (30.3) examines ways to integrate the manufacturing of a sputter-deposited BST capacitor with a thick platinum electrode. It could then be used in a logic-compatible process. Once production-worthy, such a process can combine with logic structures to create chips which merge logic and blocks of high-density DRAM.

Overcoming some of the processing limitation that held back BST capacitors, researchers at Samsung point out several tricks they developed to perform post-process annealing. They increased capacitance and prevented barrier oxidation and any unwanted patterning of the electrode. A concave capacitor structure with a buried barrier combines the use of platinum and metal-organic-CVD-deposited BST to solve those problems.

Ferroelectric PZT-based capacitors also are highlighted in several presentations. NEC designers examine various optimization attempts on the PZT material composition. They also investigate the sputtering conditions required for the top electrodes to achieve a highly reliable capacitor for a ferroelectric RAM (paper 30.5). Such a device would keep a wide operating margin over $10^9$ switching cycles.

Additional ferroelectric developments were discussed in papers 13.4 and 13.5 by NEC and Toshiba, respectively. NEC detailed the development of a 0.25-μm CMOS-logic-compatible FERAM memory cell. The cell occupies an area of just 3.2 $\mu m^2$, making it one of smallest FERAM cells yet reported. Toshiba researchers concentrated on developing a cell with a high immunity to fatigue, which can be used at Mbit-class densities when powered by a 3-V supply. Employing a single-transistor/single-capacitor structure, the cell has a lifetime several times that of conventional FERAM cell structures.

## Merging DRAM And Logic

The ability to combine DRAMs and logic on the same chip has become a hot topic due to the potential performance gains. But, there are drawbacks. Processes optimized for DRAMs don't allow the co-integration of high-performance logic. And, processes for high-performance logic don't permit high-density DRAM arrays to be co-integrated. The research done by NEC Corp., Tokyo, Japan, however, may change that. In paper 13.1, NEC researchers cover a multiple-thickness, gate-oxide scheme that employs dual-gate transistor structures to co-integrate high-performance logic with embedded DRAM blocks.

The multiple-thickness gate oxides are formed using argon and nitrogen implants, along with impurity doping into the dual-gate polysilicon, using self-aligned thermal oxidation. The process achieves about a 20% difference in oxide thickness. To achieve high performance, the thin oxide is used for the logic-circuits NMOS and PMOS devices. The thicker oxide gates are used by the NMOS transistors associated with each DRAM cell, providing better storage control. In conjunction with a silicon-nitride cap on the PMOS transistor's gate, the doping process suppresses boron penetration. That produces better capacitors for the memory cells.

Focusing on another aspect of the ability to create logic-friendly merged DRAMs, designers at NEC use shared tungsten structures to deal with the processing differences for logic and memory circuits (31.6). If tungsten-based Damascene bit lines, storage capacitors, and contact plugs are used in the DRAM portion of the processing, the same metal can be shared as local-interconnect lines and stacked contacts/vias in the logic circuitry. The designers feel this scheme can realize a 40-to-65% interconnect resistance reduction, in addition to the optimal use with tantalum-pentoxide dielectric full-metal capacitors. The shared tungsten structures also help reduce some process steps, improve the thermal budget, and minimize the aspect ratio and surface step height—all of which enhance the processes' ability to combine the DRAM and logic on the same chip.

Researchers at IBM Corp., Hopewell Junction, N.Y., also pursue the goal of integrating the DRAM and logic. They have developed a 0.18-μm logic/DRAM technology that's fully compatible with their most advanced logic technology. And, it requires no redesign of preexisting logic circuits. Detailed in paper 37.5, the technology can integrate 0.617-$\mu m^2$ DRAM cells on the same chip as a 4.2-$\mu m^2$ SRAM cell. They employ a dual-Damascene copper-metallization system so the chip achieves the highest performance operating from a 1.5-V supply. The DRAM cell also has a very high data retention time—over 256 ms at 85° C.

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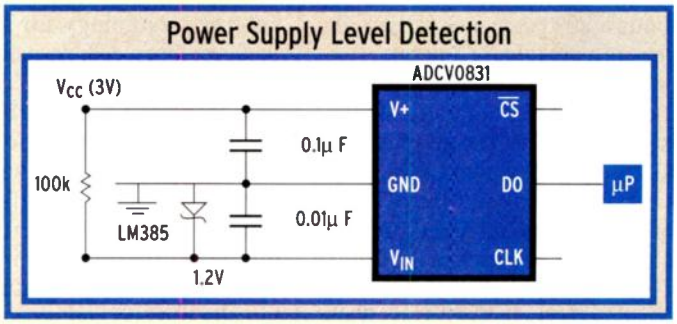


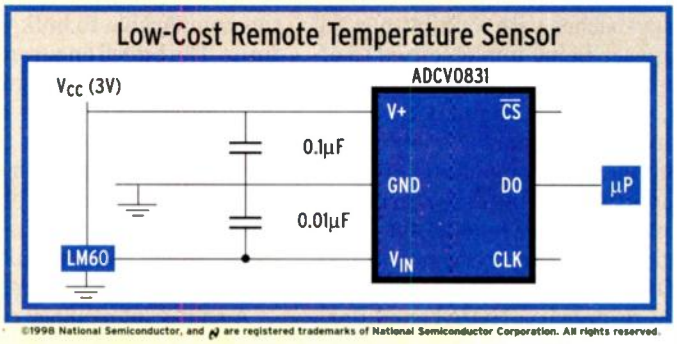




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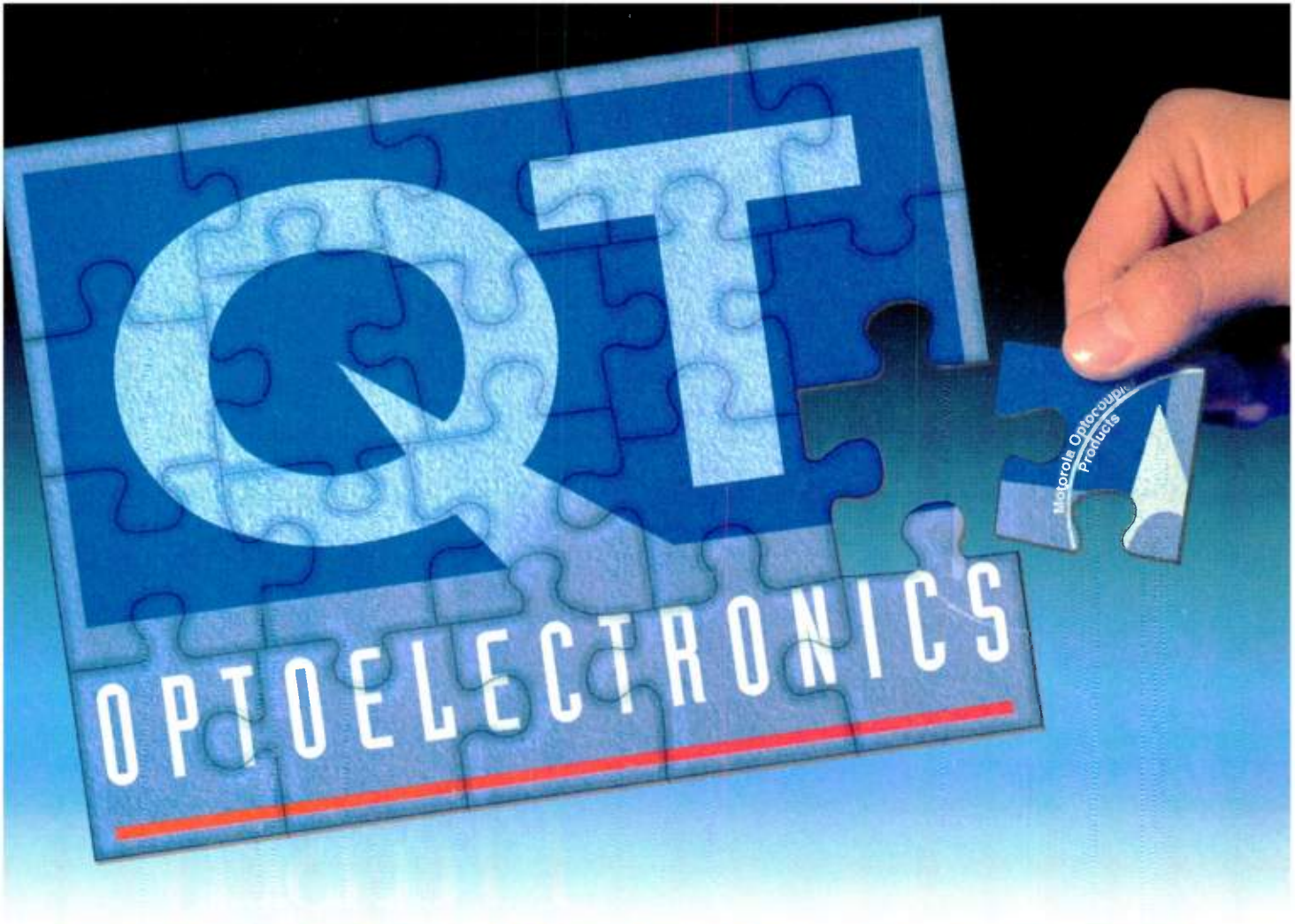


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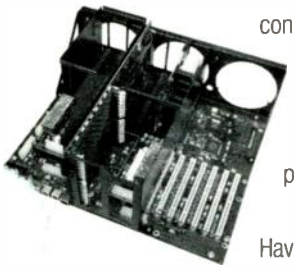

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# Compound Semiconductors And Power Devices Are Rising Stars At IEDM

*Integrated Inductors, Fastest GaAs HBTs, SOI Transistors, And Novel InP-Based HEMTs Get Their Share Of The Limelight.*

**Ashok Bindra**

Scientists and researchers around the world continue to battle hurdles so they can extend the performance of semiconductor chips and discrete components. This ongoing effort will be the center of focus at the International Electron Devices Meeting (IEDM). Some key developments sure to grab attention include compound semiconductor devices like high-electron-mobility transistors (HEMTs) and silicon-on-insulator- (SOI) based power MOSFETS. Wide-bandgap semiconductor power electronics, low-voltage bipolar power transistors, CMOS RF ICs, and silicon-germanium (SiGe) devices also fall into this category. Other papers will explore advancements in areas such as low-voltage CMOS and on-chip or integrated inductors. Merged processes combining bipolar and CMOS technologies (necessary for system-level integration) also get their share of attention.

In the HEMT arena, researchers from NTT System Electronics Laboratories, Kanagawa, Japan, will demonstrate the fastest three-terminal, InP-based, lattice-matched HEMT device developed to date. It exhibits a cutoff frequency ($f_T$) as high as 350 GHz. According to the researchers, this implies gate delays of 3 ps. With this technology, NTT scientists believe digital circuits can be fabricated for communication networks. These networks would be able to handle data rates in excess of 100 Gbits/s—a factor of ten improvement in speed. This is attributed to the 30-nm gate length made possible by the use of a single-layer fullerene, noncomposite resist in electron-beam (EB) lithography (*Fig. 1*).

Other papers in Session 9 also propose improvements in InP-based HEMTs. They come from the University of Padova, Italy; Massachusetts Institute of Technology (MIT), Cambridge, Mass.; and Sanders, a Lockheed Martin Company in Nashua, N.H. To improve threshold voltage ($V_{TH}$) reproducibility, as well as suppress kink effects in InP-based HEMTs, scientists at the University of Padova incorporated an InP recess-etch stopper layer in the structure of InAlAs/InGaAs. In addition, the researchers observed improved long-term stability with these devices.

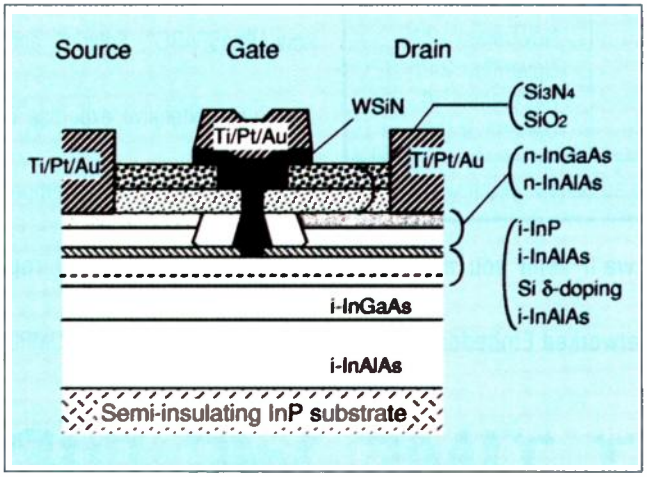
Another serious concern for InP HEMTs is the introduction of hydrogen during processing, which results in circuit failures. A joint paper by MIT and Sanders highlights two independent degradation mechanisms that affect the intrinsic and extrinsic portions of the device. Yet, the paper does not propose any solutions to these problems.

Work on a metamorphic (MM) I AlAs/InGaAs HEMT on a GaAs st strate is being done at the Institute Electronics and Microelectronics North (IEMN), Lille, France. T study shows the impact of indium co position on such transistors. The searchers demonstrate the potential o MM-HEMT for low-noise applications up to 100 GHz. It's also a good alternative to lattice-matched InAlAs/InGaAs/InP HEMTs.

Scientists also continue to push the performance envelope of GaAs-based heterojunction bipolar transistors (HBTs). While the HBTs run faster than silicon bipolar transistors, power dissipation and thermal management have been perennial problems. Several papers in Session 25 discuss performance improvements in HBTs for high-speed data transmission.

A notable paper from Hitac Central Research Lab, Tokyo, Ja reveals a method to reduce para capacitance in the base-collector j tion of the device. To ach high $f_T$ and $f_{MAX}$, the searchers have refined t self-aligned, dry-etchin process for the base-collecto mesa formation. At the same time, they've reduced the width of the base contact down to 0.25 µm.

The researchers also minimized the area of the base electrode by controlling the side etching of WSi/Ti. The process has been further enhanced in terms of planarization, double photo-resi coating, and etchback pr sion. Employing th process improvements, tachi researchers redu




**1. This cross-sectional view shows NTT's 30-nm T-gate InAlAs/InGaAs HEMT lattice matched to an InP substrate. The device is reported to exhibit a cutoff frequency of 350 GHz.**

the Department of EECS, the University of California at Berkeley, researchers have fabricated MOSFETS on low-cost SPIMOX wafers. To be precise, NMOS transistors with a gate-oxide thickness of 6.5 nm were fabricated on a SPIMOX substrate. For a transistor with a channel width of 10 μm and a length of 10 μm, the threshold voltage and subthreshold swing were found to be 0.27 V and 96.8 mV/decade, respectively. These results were unsatisfactory. Also, the drain/source resistance was a high value of 432 Ω. And, the buried oxide (BOX) for the SPIMOX samples was found to be leaky. According to the researchers, the process needs improvements on several fronts before such a technology can become commercially feasible. The aim of this work was to show that SPIMOX is a promising low-cost fabrication process for SOI.

## SiGe And High Power

Low bandgap and compatibility with silicon has made silicon germanium (SiGe) an attractive combination for high-frequency bipolar transistors and RF ICs. Development efforts around the world are pushing this technology into the mainstream. Philips Research Laboratories now extends the benefits of SiGe to a new area, namely ultra-fast power rectifiers. Philips researchers have produced discrete $p^+$(SiGe)-$n^-$-$n^{++}$ diodes with low forward voltage drop ($V_F$), low stored charge ($Q_S$), and a soft recovery. As per Philips paper 26.6, the SiGe diodes far exceed the performance of conventional pin diodes without resorting to lifetime killing, thereby lending themselves to integration. Plus, the SiGe diode can be inherently tuned during manufacture by varying layer thickness and Ge percentage in the $p^+$ layer. Consequently, to suit particular applications, the manufacturer can select the optimum trade-off between the diode's $V_F$, reverse leakage current $I_R$, and $Q_S$ parameters.

The quest to push the frequency limits of bipolar transistors continues with the same zeal. A joint paper (26.7) written by the Institute for Semiconductor Physics, Frankfurt, Germany, and Lucent Technologies' Bell Labs, Murray Hill, N.J., will discuss a heterojunction bipolar transistor. This transistor is based on C-doped SiGe layers (Si/SiGe:C) grown by LPCVD epitaxy with low defect density. The HBT, fabricated in an epi-free, n-well, single polysilicon technology, displays $f_T$ and $f_{MAX}$ values up to 65 GHz. The single-stage delays of a ring oscillator based on the Si/SiGe:C HBT is down to 16 ps. The scientists claim that this technology is suitable for integration into a modular, cost-effective, high-performance BiCMOS process.

Concurrently, researchers at Texas Instruments Inc., Dallas, Texas, have made substantial progress in the properties of lateral DMOS (LDMOS), making it compatible for integration into present-generation BiCMOS power technologies. Besides giving a short overview of the LDMOS evolution, TI's paper examines experimental, dual-channel oxide construction as a compromise for maintaining good breakdown voltage (BV) and figure-of-merit performance with logic-level inputs. In addition, for the first time, TI discloses the use of electroplated copper surface wires to alleviate debias problems and enhance device operating efficiency. Since its effect is independent of current flow and device operation, the copper improves both forward and reverse operation, says TI paper 26.1. Two types of devices are described: 30-to-100-V field LDMOS and 12-to-25-V planar LDMOS.

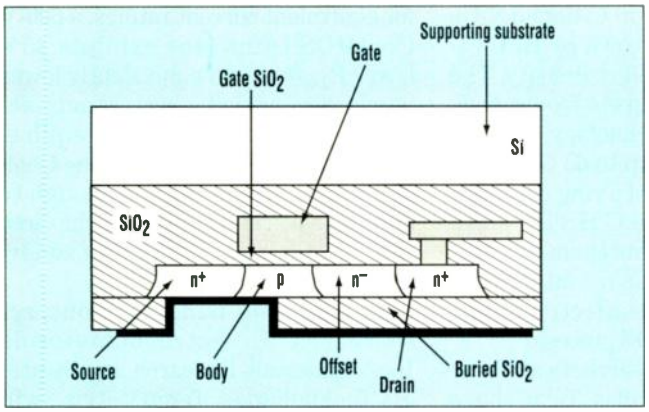
Siemens AG, Munchen, Germany, reveals its CoolMOS structure for new-generation, high-voltage power MOSFETS. The structure offers an area-specific on-resistance of 3.5 Ω-mm$^2$. To obtain such a dramatic reduction of on-resistance for a given chip area, Siemens introduced charge-compensating columns in the drift region of the transistor. In this scheme, the doping of the vertical drift region is increased substantially. This additional charge is further counterbalanced by the implementation of fine-structured columns of the opposite doping type. As a result, the blocking voltage of the transistor remains unaltered. For higher blocking voltages, the depth of the columns has to be increased, but the doping levels don't have to be altered. Thus, according to Siemens' paper (26.2), there's a linear relationship between blocking voltage and on-resistance. The paper measures this relationship between 200 to 1000 V. Test results indicate that for equivalent current ratings, a 600-V CoolMOS transistor exhibits 35% lower $R_{DS}$(on), and equivalently lower power dissipation—with about one-half the gate-charge drive requirement. Also, claims Siemens, the CoolMOS structure is rugged enough to offer an avalanche energy per chip area that closely matches that of zener-clamped devices.

On the wide-bandgap front, researcher C.E Weitzel of Motorola Inc.'s Materials Research and Strategic Technologies, Tempe, Ariz., will explore the RF properties of semiconductor power devices. These devices include SiC MESFETs, GaAs MESFETs, and AlGaN heterostructure FETs (HFETs). This invited paper (3.1) aims to address some of the manufacturing and packaging challenges confronting these wide-bandgap semiconductor devices.

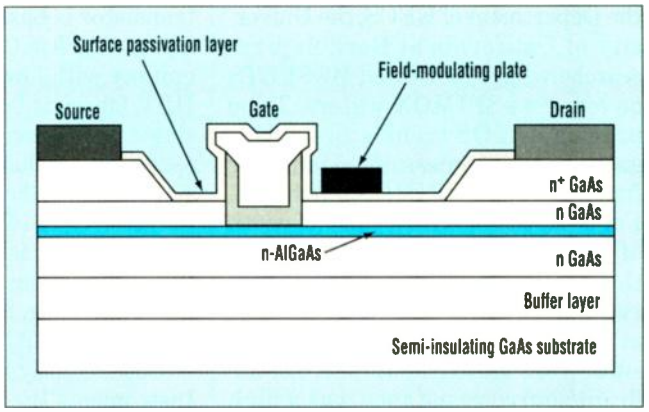
Another presentation of interest in this session is 3.3, a paper by NEC Corp.'s ULSI Device Development Labs. NEC unveils a novel, high-power AlGaAs/GaAs HFET with a field-modulating plate: the FP-HFET. According to the authors, the field-modulating plate reduces the electric field at the gate edge, and simultaneously controls the channel opening in the recessed region. The field-modulating plate is formed on the $SiO_2$ surface-passivation layer (*Fig. 3*) in the gate/drain recessed region of the HFET structure. This results in increased gate-drain breakdown voltage to 47 V. Also, the FP-HFET exhibits an improvement in output power up to 35 V at 1.5 GHz, with a PAE of more than 55% up to 30-V breakdown voltage. The FP-HFET is being targeted as a high-power, solid-state amplifier for wireless-communications applications.

## Integrated Inductors

As the system-on-a-chip effort progresses, designers bring more and more passive elements on board to make the design as complete as possible. The biggest challenge has been the inductors. Obstacles confronting the integration of high-quality spiral inductors on-chip is the focus of Session 19. This session kicks off with an invited paper on, "Progress in RF Inductors on Silicon-Understanding Substrate Losses," by Joachim N. Burghartz of the IBM Research Divi-




**2. The quasi-SOI MOSFET structure depicted here uses a reversed-silicon-wafer direct-bonding (RSDB) process to bond a high-resistivity silicon substrate to the active region of the power MOSFET. The device exhibits a power-added efficiency of 64% at 2 GHz and 2.4 V.**




**3. NEC researchers propose a high-power AlGaAs/GaAs heterostructure FET (HFET) with a field-modulating plate to improve the gate-drain breakdown voltage to 47 V. This results in increased power-added efficiency at high voltages.**

parasitic capacitance in small-scale InGaP/GaAs HBTs by about 20%. Consequently, they achieved an $f_T$ of 156 GHz and an $f_{MAX}$ of 255 GHz, with an emitter size of 0.5 by 4.5 $mm^2$. According to the authors, these developments heighten the potential for using these devices for high-speed, low-power circuit applications.

Meanwhile, others take a different route to obtain better performance from HBTs. At the University of Michigan, Ann Arbor, Mich., department of EECS researchers developed a high-gain, high-bandwidth monolithic amplifier for optoelectronics receivers using GaInP/GaAs HBTs. They deployed non-alloy metal contacts for the emitter, base, and collector, with a laterally etched undercut applied between the base and collector region. This reduces capacitance, while avoiding base-resistance degradation. To improve HBT reliability, silicon nitride was utilized as a passivation layer. Incorporating the improved GaInP/GaAs HBTs in monolithic-microwave-IC (MMIC) technology, a transimpedance amplifier was realized that offered a flat gain of 52 dB over a bandwidth of 13.5 GHz.

## RF Devices

While compound semiconductor devices are being architected for use in mm and sub-mm wave regions, efforts are underway to push the limits of silicon-based MOSFETS into the microwave domain. These efforts aim to make silicon attractive for RF applications, especially from the standpoint of power and efficiency. Six papers in Session 35 attempt to address some of these issues.

For instance, a paper by NTT Wireless Systems Labs, Tokyo, Japan, focuses on a high-efficiency, quasi-SOI power MOSFET for multi-gigahertz applications. Using reversed-silicon-wafer direct bonding, it employs a high-resistivity substrate (*Fig. 2*). As per the NTT paper, the fabricated quasi-SOI MOSFET demonstrated a power-added efficiency of 64% at 2 GHz and 2.4 V. Because the new structure suppresses parasitic bipolar effects, the breakdown voltage realized for the quasi-SOI device was as high as 13.8 V. In addition, the source resistance of the new device was lower—achieving an $f_{MAX}$ of 11 GHz.

Similarly, researchers at Philips Research Laboratories, Eindhoven, The Netherlands, have increased power-added efficiency of low-voltage RF bipolar power transistors. By reducing the output capacitance, Philips claims a record power-added efficiency (PAE) of 71% at 0.5-W output power and 1.8 GHz, with a 3.5-V supply voltage. The lower output capacitance of 2.1 pF was obtained by using proper layout techniques and lower interconnect capacitance. This high efficiency, in conjunction with low cost and simple impedance matching, ensures that silicon bipolar technology is—and will remain—a viable technology for present and future cellular and other RF applications.

A paper from Toshiba Corp.'s Advanced Semiconductor Devices Research Laboratories, Kawasaki, Japan, unveils a new structure for realizing a low-power, high-performance, SOI-lateral bipolar-junction transistor (BJT). In this scheme, the developers employ a self-aligned, external base-formation process to attain a very low base resistance of 1.5 kΩ, as well as reduced parasitics. Using this process, the fabricated BJT exhibited an $f_{MAX}$ of 31 GHz at a collector current of 330 μA.

## Scaling SOI

The trend toward low voltage opens up the big question: Can SOI scale down to the dimensions required for future-generation chips? At IBM Microelectronics, Hopewell Junction, N.Y., paper 15.1 argues yes. IBM researchers describe a 0.13-μm, 1.2-V SOI technology with effective transistor channel lengths as short as 0.055 μm—the smallest ever reported for SOI. The paper indicates that this technology offers more than 25% improvement in speed over the conventional bulk CMOS in a ring oscillator. It also requires 50% less active power for an inverter with the same gate delay as one built in bulk CMOS. Furthermore, based on partially depleted, scaled SOI MOSFETS, the IBM researchers built a 288-kbit SRAM to show that the SRAM works down to a supply voltage of 0.8 V.

To exploit the advantages of SOI devices in future CMOS scaling, however, low-cost, high-throughput fabrication methods are most desirable. Separation by plasma implantation of oxygen (SPIMOX) process, a low-cost version of the commercial SIMOX wafers, has been reported. And, its feasibility has been demonstrated. At

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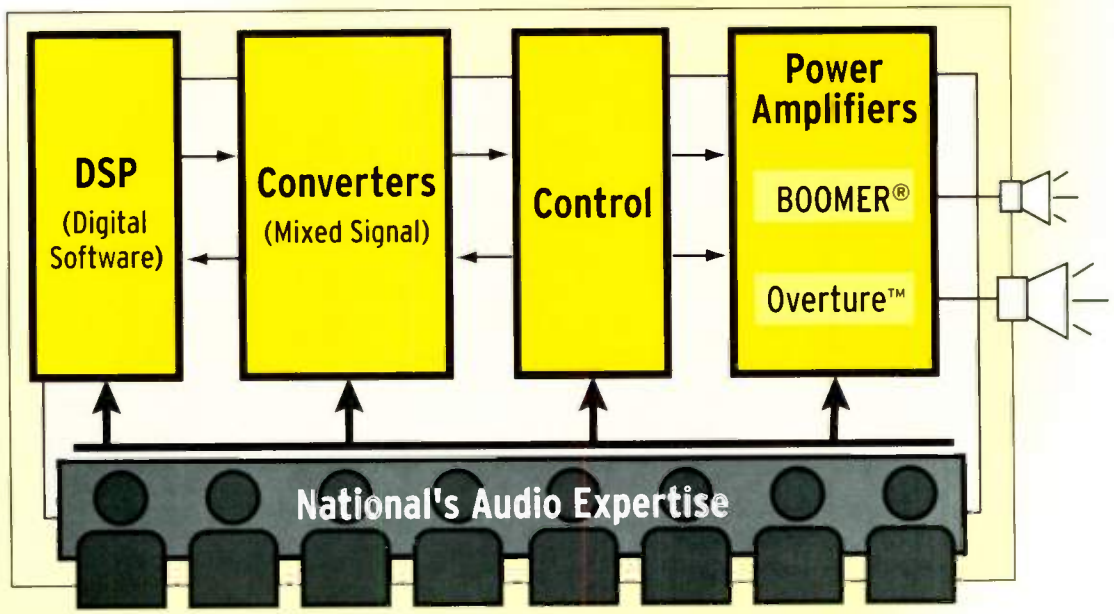
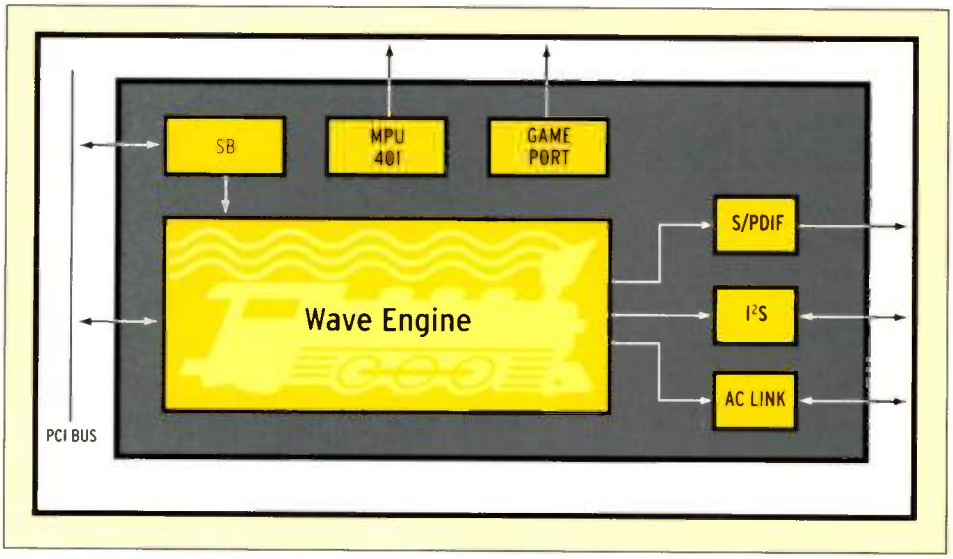



**Full Audio Chain**

National Semiconductor features complete lines of audio products optimized for superior end-to-end integration in your audio designs, enabling incredible gains in application performance, efficiency and footprint size.

National Semiconductor

# DC'97 Digital Audio Controller




**LM4560 Block Diagram**

**National's advanced PCI audio accelerator provides integrated DSP and legacy compatibility on a single chip.**

## LM4560 Advanced PCI Audio Accelerator

The LM4560 provides significant system level performance enhancement over an equivalent ISA audio controller.

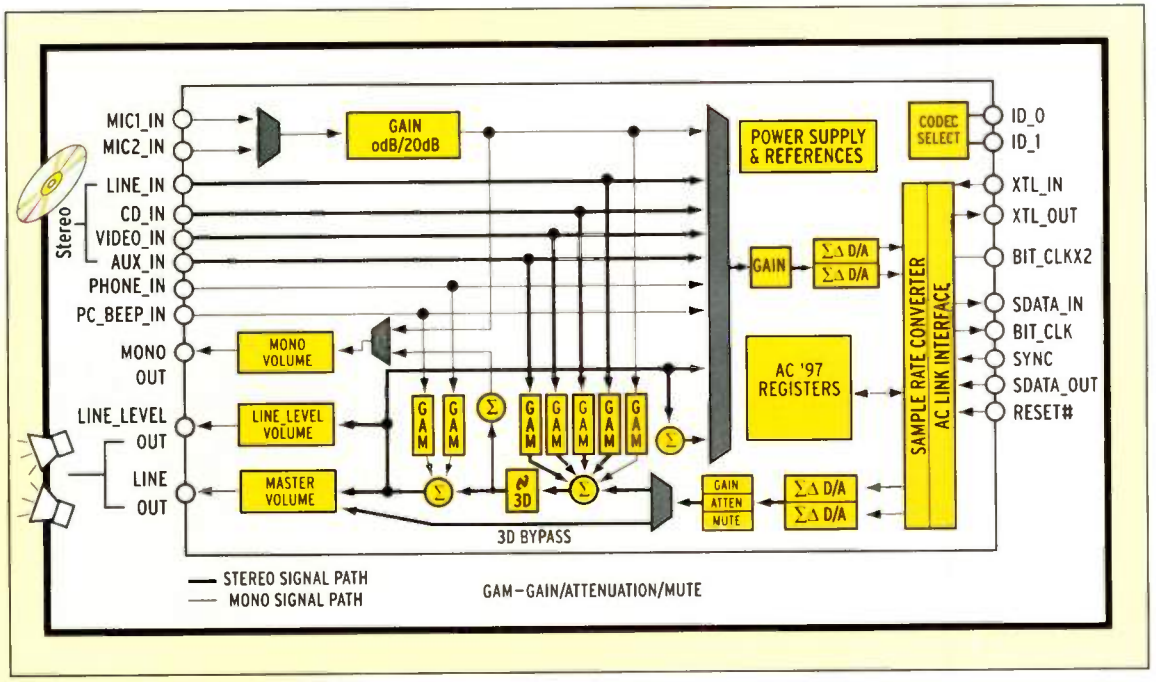
- Full legacy compatibility (SoundBlaster and DMA), wavetable synthesis, DirectMusic™ DirectSound™ 2D/3D
- Integrated 64-voice wave table engine with per-voice effect processing capability
- Microsoft® WDM Streaming architecture compliant with dynamic "re-routable endpoint" per channel support for I²S, SP/DIF audio output
- CD quality audio with >90dB SNR using AC '97/'98 codec
- PCI 2.1-compliant Bus Master optimized for multiple stream operation
- 3.3V process
- Space-saving 100-pin TQFP package
- Compliant with AC '97 specifications Rev 2.0 for AMC codec and multiple codecs

Ideal for applications such as adaptor cards and motherboards

## National and AC '97

In May 1996, we joined forces with other industry leaders such as Intel, ADI, Yamaha and Creative Labs to develop the AC '97 standard for higher levels of performance and design flexibility.

# AC '97 CODECs




**LM4548 Block Diagram**

NATIONAL AC '97 HAS A FULL RANGE OF CODECS FOR AUDIO SYSTEM DESIGN NEEDS.

## LM4546/7/8 AC '97 Rev 2.0/PC98 Compliant CODECs

THE LM454X CODECS PROVIDE HIGH QUALITY AUDIO OPTIONS AND FUNCTIONALITY FOR COMPLETE PC AUDIO SYSTEM DESIGNS.

- LINE-OUT SNR: 95dB TYP
- DAC AND ADC DYNAMIC RANGE: 90dB TYP
- NATIONAL'S 3D SOUND CIRCUITRY
- STEREO 18-BIT SIGMA-DELTA A/DS AND D/AS WITH 128X OVERSAMPLING
- POWER MANAGEMENT SUPPORT

## National's Current AC '97 CODEC Family

| CODECs | AC '97 Rev | 3.3V Digital | SRC | Headphone Amp | 2nd Line Out | Video IN | Secondary Line Volume Control | AUX IN | Multiple CODEC | Analog 3D |
|---|---|---|---|---|---|---|---|---|---|---|
| LM4540 | 1.03 | ✓ | | | | | | | | ✓ |
| LM4543 | 1.03 | ✓ | | | | ✓ | | ✓ | | ✓ |
| LM4545 | 1.03 | ✓ | | ✓ | ✓ | ✓ | ✓ | ✓ | | ✓ |
| LM4546 | 2.0 | ✓ | ✓ | | | | | | ✓ | ✓ |
| LM4547 | 2.0 | ✓ | | | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| LM4548 | 2.0 | ✓ | ✓ | | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |

IDEAL FOR APPLICATIONS SUCH AS MOTHERBOARD AND PORTABLE PC AUDIO SYSTEMS, ENTERTAINMENT PC SOLUTIONS

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# BOOMER®
# Low-Voltage Audio Power Amplifiers

**THE ORIGINAL BOOMER FAMILY FROM NATIONAL PROVIDES A COMPLETE AUDIO AMPLIFIER SOLUTION — SUPERIOR PERFORMANCE, CLEAR AND POWERFUL SOUND AND SMALL FOOTPRINT FOR TODAY'S COMPUTER, MOBILE PHONE AND OTHER PORTABLE AUDIO DESIGNS.**

THE INDUSTRY STANDARD ORIGINAL BOOMER SERIES OF AMPLIFIERS OFFER HIGH OUTPUT POWER, HIGH-FIDELITY SOUND WITH LOW VOLTAGE AND ARE AVAILABLE IN A WIDE VARIETY OF PACKAGES, DESIGNS AND POWER RATINGS.

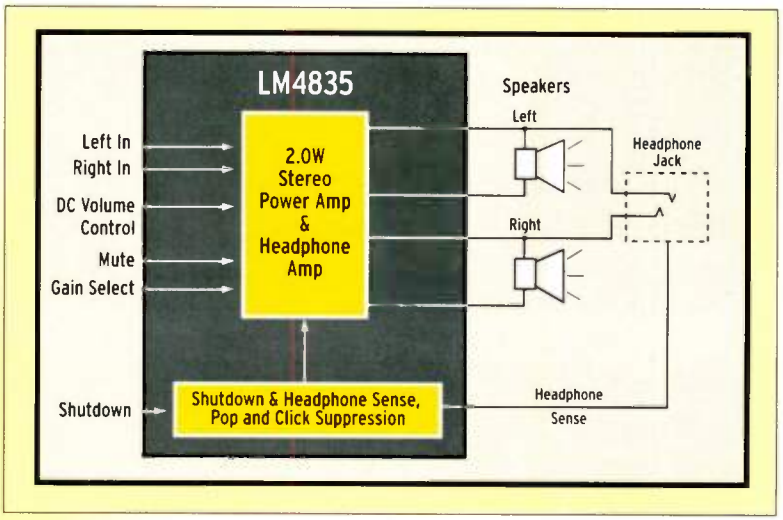
IN ADDITION TO BEING ONE OF THE MOST COST-EFFICIENT ICs, BOOMER'S ULTRA-LOW 0.7µA OF SHUTDOWN CURRENT WILL EXTEND THE BATTERY LIFE OF PORTABLE SYSTEMS. COMBINED WITH ITS PATENTED "POP AND CLICK" SUPPRESSION AND INTERNAL THERMAL SHUTDOWN PROTECTION CIRCUITRY, NATIONAL'S BOOMER ICs DELIVER EXTREMELY SMOOTH-SOUNDING, STABLE AUDIO DESIGNS.

| Family Description | Base Part # | Description | Stereo | Bridged |
|---|---|---|---|---|
| LM483x Integrated | LM4830 | Two-Way Audio Amplification System with Volume Control | | ✓ |
| | LM4831 | Stereo 1W Audio Amplifier with 3 Input Mixer | ✓ | ✓ |
| | LM4832 | Digitally Controlled Tone and Volume with Stereo Audio Power Amplifier | ✓ | |
| | LM4834 | 1.1W Audio Power Amplifier with DC Volume Control and Mic Preamp | | ✓ |
| | LM4835 | Stereo 2W Audio Power Amplifier with DC Volume Control | ✓ | ✓ |
| LM486x Bridged | LM4860 | 1 Watt Audio Power Amplifier with Shutdown Mode | | ✓ |
| | LM4861 | 1.1W Audio Power Amplifier with Shutdown Mode | | ✓ |
| | LM4862 | 400mW Audio Power Amplifier with Shutdown Mode | | ✓ |
| | LM4863 | Stereo 2.2W Audio Amplifier with Stereo Headphone | ✓ | ✓ |
| | LM4864 | 300mW Audio Power Amplifier with Shutdown Mode | | ✓ |
| LM487x Bridged | LM4870 | 1.1W Audio Power Amplifier with Shutdown Mode | | ✓ |
| | LM4871 | 1.1W Audio Power Amplifier with Shutdown Mode | | ✓ |
| | LM4873 | Stereo 2.1W Audio Amplifier with Stereo Headphone and Input Mux | ✓ | ✓ |
| LM488x Single Ended | LM4880 | Stereo 250mW Audio Power Amplifier with Shutdown Mode | ✓ | |
| | LM4881 | Stereo 200mW Headphone Amplifier with Shutdown Mode | ✓ | |
| | LM4882 | 250mW Audio Power Amplifier with Shutdown Mode | | |

**Wide Selection of BOOMER Audio Power Amplifiers**

IDEAL FOR THE EXPLODING PORTABLE AUDIO MARKET

## LM4835 Block Diagram



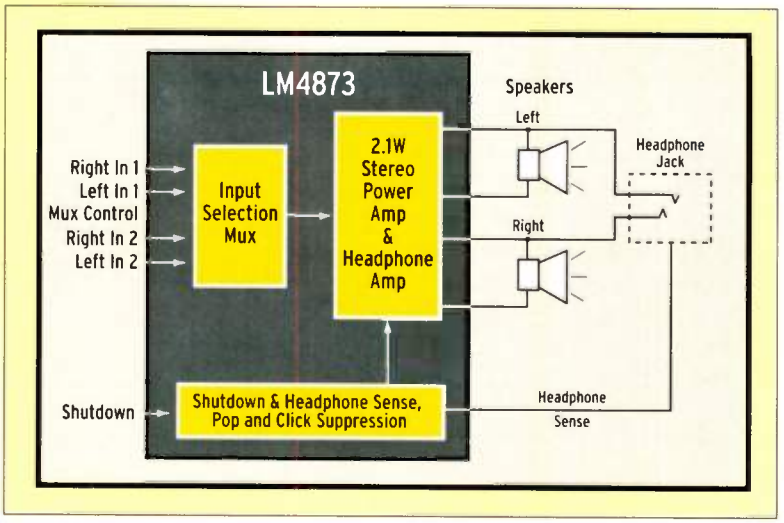

### LM4835
### BOOMER STEREO 2W POWER AMPLIFIER WITH DC VOLUME CONTROL

THE LM4835'S FULLY INTEGRATED PC98 COMPLIANT IC DESIGN PROVIDES SUPERIOR AUDIO QUALITY WHILE REQUIRING LESS EXPENSIVE EXTERNAL COMPONENTS, RESULTING IN LOWER SYSTEM COST.

- 2.0W AMP — LM4835MTE; 1.1W AMP — LM4835MT
- STEREO 85mW HEADPHONE DRIVER
- DC VOLUME CONTROL W/BYPASS
- BASS BOOST (GAIN SELECT PIN)
- EXTERNAL OR INTERNAL GAIN SET
- ULTRA LOW SUPPLY CURRENT IN SHUTDOWN MODE: 0.7µA
- THERMAL SHUTDOWN PROTECTION
- "POP AND CLICK" SUPPRESSION

IDEAL FOR APPLICATIONS SUCH AS PCS, MULTIMEDIA MONITORS AND OTHER PORTABLE AUDIO PRODUCTS

## LM4873 Block Diagram




### LM4873
### BOOMER STEREO 2.1W POWER AMPLIFIER PLUS STEREO HEADPHONE AND INPUT MUX

- 2.1W STEREO POWER AMP (LM4873MTE)
- STEREO HEADPHONE AMP
- INPUT SELECTION MUX
- ULTRA LOW SHUTDOWN CURRENT (0.7µA)
- 20-PIN TSSOP: SMALLEST PACKAGE AVAILABLE FOR BRIDGED STEREO POWER AMPLIFIER

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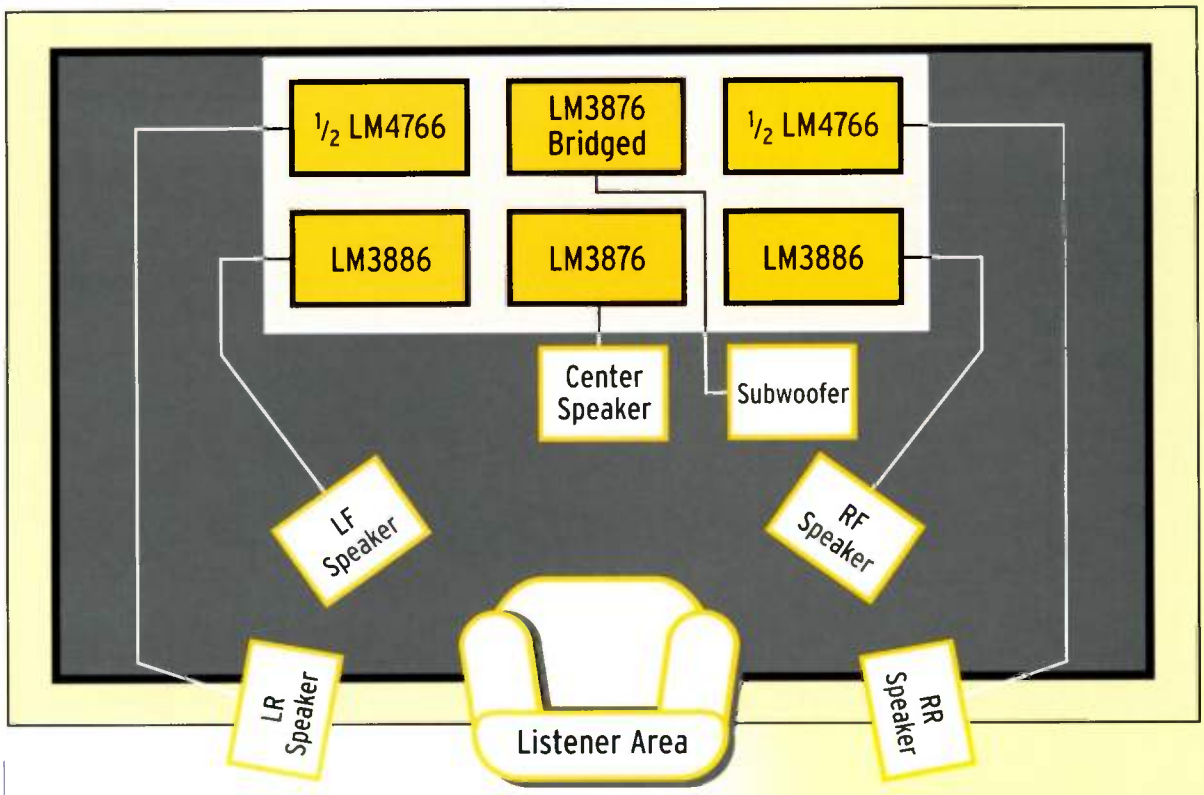
# HIGH-PERFORM

## National's Overture Solution for a 6-Channel A/V Receiver




NATIONAL'S OVERTURE AMPLIFIERS DELIVER HIGH OUTPUT POWER AND SMALLER FOOTPRINTS WHILE MAINTAINING HIGH AUDIO QUALITY NEEDED IN TODAY'S HIGH-PERFORMANCE A/V ENTERTAINMENT DESIGNS.

### LM4700/LM4701

30W AUDIO POWER AMP W/MUTE AND STANDBY MODES

- THD+N AT 1KHZ FROM 20HZ TO 20KHZ AT 30W INTO 8Ω: 0.08% TYP
- INPUT MUTE FUNCTION
- SPIKE: SELF PEAK INSTANTANEOUS TEMPERATURE (K°) PROVIDES DYNAMICALLY PROTECTED SAFE OPERATING AREA (SOA)
- OUTPUT OVER-VOLTAGE PROTECTION AGAINST TRANSIENTS FROM INDUCTIVE LOADS

### LM2876/LM3876/LM3886

HIGH-PERFORMANCE AUDIO POWER AMP W/MUTE — NATIONAL'S MOST POWERFUL OVERTURE AMPLIFIERS, FEATURING SPIKE™ PROTECTION TO COMPLETELY SAFEGUARD AGAINST VOLTAGE OVER/UNDERLOADS AND TEMPERATURE PEAKS.

IDEAL FOR APPLICATIONS SUCH AS HOME ENTERTAINMENT A/V SYSTEMS AND MULTIMEDIA PCS

# ANCE AMPLIFIERS

## Mono Overture Amplifiers

| Amplifier | SNR | Power (type) | Power (peak) | Package TO-220 |
|---|---|---|---|---|
| LM4700* | > 98dB | 30W | 60W | 11 lead |
| LM4701 | > 98dB | 30W | 60W | 9 lead |
| LM2876* | > 95dB | 40W | 75W | 11 lead |
| LM3876* | > 95dB | 56W | 100W | 11 lead |
| LM3886* | > 92dB | 68W | 135W | 11 lead |

*Pin-compatible

## Stereo Overture Amplifiers

| AMP | Power | SPiKe™ | Mute Mode | Standby Mode | Standby Current | Package TO-220 |
|---|---|---|---|---|---|---|
| LM1876* | 20W | ✓ | ✓ | ✓ | 4.2mA | 15 lead |
| LM4765* | 30W | ✓ | ✓ | ✓ | 6.5mA | 15 lead |
| LM4766* | 40W | ✓ | ✓ | | | 15 lead |
| LM4753 | 10W | | ✓ | ✓ | 5mA | 15 lead |

*Pin-compatible

### LM1876
DUAL 20W AUDIO POWER AMP W/MUTE AND STANDBY MODES
- THD+N AT 1KHZ AT CONTINUOUS AVERAGE OUTPUT POWER OF 2X20W INTO 8Ω: 0.009% TYP

### LM4765
DUAL 30W AUDIO POWER AMP W/MUTE AND STANDBY MODES
- THD+N AT 1KHZ AT CONTINUOUS AVERAGE OUTPUT POWER OF 2X30W INTO 8Ω: 0.009% TYP

### LM4766
DUAL 40W AUDIO POWER AMP W/MUTE MODE
- THD+N AT 1KHZ AT CONTINUOUS AVERAGE OUTPUT POWER OF 2X40W INTO 8Ω: 0.009% TYP

### LM4753
DUAL 10W AUDIO POWER AMP W/MUTE, STANDBY AND DC VOLUME CONTROL
- 10W OUTPUT POWER INTO 8Ω AT 10% THD
- MAXIMUM OPERATING VOLTAGE: 32V
- POWER OUTPUT STAGE NOISE FLOOR: 3mV
- LINE OUTPUT NOISE FLOOR: 20μV
- 0-5V DC CONTROLLED VOLUME ATTENUATION: 80dB
- STEREO VARIABLE LINE-OUT PINS

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# Audio Power Amp Selection Guide

## BOOMER Products

| User Supply Voltage | Part Number | Power [THD ≤1% (Typ)]† 4 Ω | 8 Ω | 16 Ω | Power [THD ≤10% (Typ)]† 4 Ω | 8 Ω | 16 Ω | Typical THD Ratings | THD Measurement Conditions | Supply Range (V) | Single/ Dual | Package (Pin Count) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 3V & 5V | LM4830 | 1.5W | 1.15W | 0.6W | 2W | 1.4W | 0.85W | 0.20% | $P_O$=1W @ $V_S$=5V | 2.7V to 5.5V | Single | SO(24) DIP(24) |
| | LM4831 | 1.5W | 1.1W | N/A | 1.9W | 1.4W | N/A | 0.50% | $P_O$=1W @ $V_S$=5V | 2.7V to 5.5V | Dual | TQFP(44) |
| | M4832 | 0.33W | 0.25W | N/A | 0.42W | 0.33W | N/A | 0.15% | $P_O$=0.22W @ $V_S$=5V | 4.5V to 5.5V | Dual | SO(28) DIP(28) |
| | LM4834 | 1.75W | 1.1W | 0.65W | 2.2W | 1.5W | 0.85W | 0.3% | $P_O$=1W @ $V_S$=5V | 4.5V to 5.5V | Single/Dual | SSOP(28) |
| | M4835 | N/A | 1.1W | 0.6W | 2W | 1.5W | 0.85W | 0.3% | $P_O$=1W @ $V_S$=5V | 2.7V to 5.5V | Dual | TSSOP(28) |
| | | 2.0W | 1.1W | 0.6W | 2W | 1.5W | 0.85W | 0.3% | $P_O$=1W @ $V_S$=5V | 2.7V to 5.5V | Dual | TSSOP Exp(28) |
| | LM4860 | .55W | 1.15W | 0.6W | 1.9W | 1.45W | 0.85W | 0.72% | $P_O$=1W @ $V_S$=5V | 2.7V to 5.5V | Single | SO(16) |
| | LM4861 | 1.55W | 1.15W | 0.6W | 1.9W | 1.45W | N/A | 0.72% | $P_O$=1W @ $V_S$=5V | 2.0V to 5.5V | Single | SO(8) |
| | M4862 | 0.52W | 0.68W | 0.53 | 0.69W | 0.83W | 0.66W | 0.50% | $P_O$=.4W @ $V_S$=5V | 2.7V to 5.5V | Single | SO(8) DIP(8) |
| | LM4863 | N/A | 1.1W | 0.6W | N/A | 1.5W | 0.85W | 0.45% | $P_O$=.5W @ $V_S$=5V | 2.0V to 5.5V | Dual | SO(16) DIP(16) |
| | | N/A | 1.1W | 0.6W | N/A | 1.5W | 0.85W | 0.45% | $P_O$=.5W @ $V_S$=5V | 2.0V to 5.5V | Dual | TSSOP(20) |
| | | 2.2W | 1.1W | 0.6W | 2.7W | 1.5W | 0.85W | 0.45% | $P_O$=.5W @ $V_S$=5V | 2.0V to 5.5V | Dual | TSSOP Exp(20) |
| | M4864 | N/A | 0.68W | 0.55W | N/A | 0.84W | 0.72W | 0.7% | $P_O$=.3W @ $V_S$=5V | 2.7V to 5.5V | Single | SO(8) DIP(8) |
| | | N/A | 0.3W | 0.55W | N/A | 0.3W | 0.3W | 0.7% | $P_O$=.3W @ $V_S$=5V | 2.7V to 5.5V | Single | MSOP(8) |
| | M4870 | 1.7W | 1.18W | 0.65W | 2.15W | 1.5W | 0.85W | 0.25% | $P_O$=1W @ $V_S$=5V | 2.0V to 5.5V | Single | SO(8) |
| | LM4871 | 1.7W | 1.18W | 0.65W | 2.15W | 1.5W | 0.85W | 0.25% | $P_O$=1W @ $V_S$=5V | 2.0V to 5.5V | Single | SO(8) DIP(8) |
| | LM4873 | N/A | 1.1W | 0.65W | N/A | 1.5W | 0.85W | 0.3% | $P_O$=2W @ $V_S$=5V | 2.0V to 5.5V | Dual | TSSOP(20) |
| | | 2.1W | 1.1W | 0.65W | 2.6W | 1.5W | 0.85W | 0.3% | $P_O$=2W @ $V_S$=5V | 2.0V to 5.5V | Dual | TSSOP Exp |
| | LM4880 | 0.34W | 0.27W | 0.17W | 0.43W | 0.33W | 0.2W | 0.03% | $P_O$=.2W @ $V_S$=5V | 2.7V to 5.5V | Dual | SO(8) DIP(8) |
| | LM4881 | N/A | 0.25W | 0.15W | N/A | 0.3W | 0.2W | 0.04% | $P_O$=.2W @ $V_S$=5V | 2.7V to 5.5V | Dual | SO(8) DIP(8) MSOP(8) |
| | M4882 | 0.38W | 0.27W | 0.17W | 0.43W | 0.33W | 0.2W | 0.03% | $P_O$=.2W @ $V_S$=5V | 2.4V to 5.5V | Single | SO(8) MSOP(8) |
| ($V_S$=6V) | LM386 | 0.25W | 0.25W | 0.15W | 0.32W | 0.3W | 0.2W | 0.25% | $P_O$=.125W @ $V_S$=6V | 4V to 18V | Single | SO(8)DIP(8)MSOP(8) |
| 12V | LM380 | 1.5W | 1.0W | N/A | 2.25W | 1.5W | N/A | 0.50% | $P_O$=4W @ $V_S$=22V | 10V to 22V | Single | DIP(14) DIP(8) |
| | LM384 | N/A | N/A | N/A | 1.75W | N/A | N/A | 0.25% | $P_O$=4W @ $V_S$=22V | 12V to 26V | Single | DIP(14) |
| | LM386 | 0.25W | 0.6W | 0.6W | 0.35W | 0.8W | 0.95W | 0.25% | $P_O$=.125W @ $V_S$=6V | 4V to 18V | Single | SO(8)DIP(8)MSOP(8) |
| | LM1877 | 1.5W | 1.0W | 0.55W | 1.75W | 1.3W | 0.75W | 0.06% | $P_O$=1W @ $V_S$=14V | 6V to 24V | Dual | DIP(14) SO(14) |
| 14V | LM380 | 2.5W | 1.75W | N/A | 3.25W | 2.25W | N/A | 0.20% | $P_O$=4W @ $V_S$=22V | 10V to 22V | Single | DIP(14) DIP(8) |
| | LM384 | N/A | N/A | N/A | 3.25W | N/A | N/A | 0.25% | $P_O$=4W @ $V_S$=22V | 12V to 26V | Single | DIP(14) |
| ($V_S$=16V) | LM386 | N/A | 0.6W | 1.0W | N/A | 0.8W | 1.6W | 0.25% | $P_O$=.125W @ $V_S$=6V | 4V to 18V | Single | SO(8) DIP(8) |
| | LM1877 | 2.0W | 1.3W | 0.85W | 2.5W | 1.75W | 1.0W | 0.06% | $P_O$=1W @ $V_S$=14V | 6V to 24V | Dual | DIP(14) SO(14) |
| | M2879 | N/A | 1.25W | N/A | N/A | 2W | N/A | 0.05% | $P_O$=1W @ $V_S$=12V | 6V to 32V | Dual | TO-220(11) |

## Overture Products 20V & Above

| User Supply Voltage | Part Number | Power [THD ≤1% (Typ)]† 4 Ω | 8 Ω | 16Ω | Power [THD ≤10% (Typ)]† 4Ω | 8 Ω | 16 Ω | Typical THD Ratings | THD Measurement Conditions | Supply Range (V) | Single/ Dual | Package (Pin Count) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ($V_S$ = ±22V) | LM1876 | 23W | 20W | 11W | 29W | 26W | 14W | 0.08% | $P_O$=15W @ $V_S$ = ±20V | 20V to 54V | Dual | TO-220(15)* |
| ($V_S$ = 20V) | LM1877 | 2.0W | 2.0W | N/A | 2.5W | 3.0W | N/A | 0.06% | $P_O$=1W @ $V_S$ = 14V | 6V to 24V | Dual | DIP(14) SO(14) |
| $V_S$ = 28V) | LM2879 | 3.5W | 7.0W | 9W | 4W | 8W | 12 | 0.05% | $_O$=1W @ $V_S$ = 12 | 6V to 32V | Dual | TO-220(11) |
| ($V_S$ = 22V) | LM380 | N/A | 4.0W | 2.5W | N/A | 5W | 3.25W | 0.20% | $P_O$=4W @ $V_S$ = 22V | 10V to 22V | Single | DIP(14) DIP(8) |
| ($V_S$ = 26V) | LM384 | N/A | 5.5W | N/A | 2.5W | 7W | 5W | 0.25% | $P_O$=4W @ $V_S$ = 22V | 12V to 26V | Single | DIP(14) |
| ($V_S$ = ±25V) | LM1875 | 20W | 20W | N/A | 25W | 30W | N/A | 0.02% | $P_O$=20W @ $V_S$ = ±25V | 16V to 60V | Single | TO-220(5) |
| ($V_S$ = ±30V | LM2876 | 25W | 40W | 22W | 35W | 50W | 26W | 0.06% | $P_O$=25W @ $V_S$ = ±30V | 20V to 60V | Single | TO-220(11)* |
| ($V_S$ = ±35V) | LM3875 | 45W ($V_S$ = ±25V) | 56W | 30W | 56W ($V_S$ = ±25V) | 70W | 39W | 0.06% | $P_O$=40W @ $V_S$ = ±35V | 20V to 84V | Single | TO-220(11)* |
| ($V_S$ = ±35V) | LM3876 | 45W ($V_S$ = ±25V) | 56W | 30W | 56W ($V_S$ = ±25V) | 70W | 39W | 0.06% | $P_O$=40W @ $V_S$ = ±35V | 20V to 84V | Single | TO-220(11)* |
| ($V_S$ = ±35V) | LM3886 | 68W ($V_S$ = ±28V) | 63W | 33W | 87W ($V_S$ = ±28V) | 78W | 41W | 0.03% | $P_O$=60W @ $V_S$ = ±28V | 20V to 84V | Single | TO-220(11)* |
| ($V_S$ = ±28V) | LM4700 | 23W | 34W | 19W | 29W | 42W | 24W | 0.08% | $P_O$=30W @ $V_S$ = ±28V | 20V to 64V | Single | TO-220(11)* |
| ($V_S$ = ±28V | LM470 | 23W | 34W | 19W | 29W | 42W | 24W | 0.08% | $P_O$=30W @ $V_S$ = ±28V | 20V to 64V | Single | TO-220(9) |
| ($V_S$ = 24V) | LM4752 | 8W | 4.8W | 3W | 11W | 7W | 4W | 0.05% | $P_O$=4.5W @ $V_S$ = 24V | 10V to 32V | Dual | TO-220(7) |
| ($V_S$ = 24V) | LM4755 | 8W | 4.8W | 3W | 11W | 7W | 4W | 0.05% | $P_O$=4.5W @ $V_S$ = 24 | 10V to 32V | Dual | TO-220(9) |
| ($V_S$ = ±28V) | LM4765 | 24W | 32W | 18W | 28W | 40W | 22W | 0.08% | $P_O$=30W @ $V_S$ = ±28V | 20V to 64V | Dual | TO-220(15) |
| ($V_S$ = ±30V | LM4766 | 26W | 42W | 23W | 37W | 53W | 28 | 0.06% | $P_O$=25W @ $V_S$ = ±30V | 20V to 60V | Dual | TO-220(15) |

† Power Specified as Continuous RMS  * Isolated Packages Available

FOR INFORMATION ON CODECs AND CONTROLLER PRODUCTS, SEE THE TABLE ON PAGE 3.

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sion, T.J.Watson Research Center, Yorktown Heights, N.Y. This talk (19.1) will provide new insights into the inductor characteristics' dependence on the substrate configuration. It will also explore different options to provide ground shields between the spiral coil and lossy silicon. Using a three-level interconnect process, the researchers at IBM have fabricated several inductors. As long as the chip is mounted onto a lossless substrate, such as glass or quartz, results indicate that thinning the silicon leads to a higher $Q_{MAX}$ and frequency $f_O$, with a virtually unchanged L. Mounting the chip into a conventional package—a metal substrate—will result in detrimental effects if the silicon is thinned.

The second part of this study, concerning shielding, shows that introducing a perforated-metal ground provides the best shielding between the spiral coil and the silicon. But, this comes at the cost of reduced $Q_{MAX}$ and self-resonance frequency $f_{SR}$. The author cautions against having a closed-loop metal ring contact any of the ground-shield structures, as it will have a degrading effect.

The next paper in this session discusses the subtleties of extracting Q, the key performance metric, from a wide range of inductor structures fabricated in a bipolar process. On-chip planar transformers are implemented and simulated in paper 19.3. Substrate modifications to enhance the inductor Q are detailed in papers 19.4 and 19.5. To achieve $Q_{MAX}$ of up to 20 for L = 2 nH, the Institute for Semiconductor Physics in Frankfurt, Germany, has developed a method for realizing a thick, selectively grown oxide in the silicon substrate immediately under the spiral inductor.

Unlike the others, the last paper in this session, 19.7, proposes the exploitation of widely used wirebonding technology. At the School of Electronics Engineering, Ajou University, Suwon, Korea, researchers have demonstrated that gold-bondwire inductors have a very high Q-factor at desirable values of inductance. Since the inductance is controlled using the wirebonding machine, the bondwire inductors offer high flexibility in design and fabrication. According to the researchers, they could even be useful in low-cost MMICs.

# PWM Drivers

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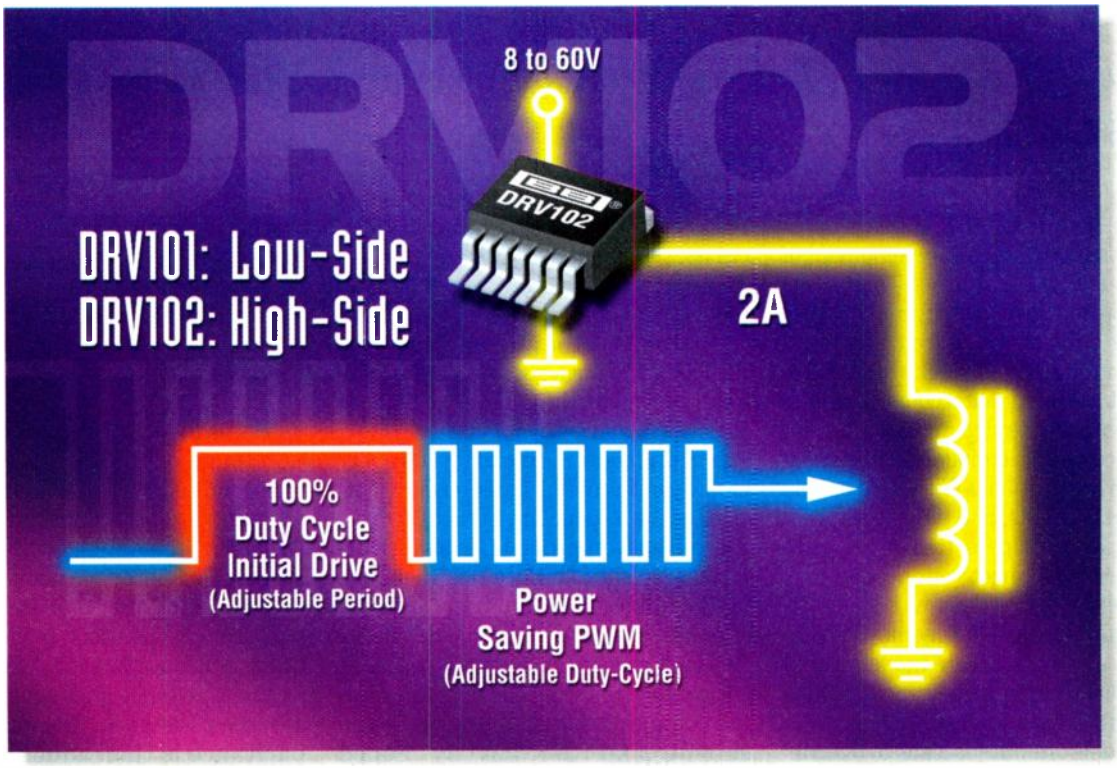


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| Product | Description | Load Current | Adjustable Initial Drive & Duty Cycle | Thermal & Current Limit Protection | Supply Voltages | Power Packages | Price (1kpcs) |
|---|---|---|---|---|---|---|---|
| DRV101 | Low-Side PWM Driver | 2A | YES | YES | +9 to +60V | TO-220 & DDPAK | $3.60 |
| DRV102 | High-Side PWM Driver | 2A | YES | YES | +8 to +60V | TO-220 & DDPAK | $3.60 |

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# IEDM Zeroes In On Advanced Models For Complex Devices

*Models Offer New Hope For Tackling The Issues Of Deep-Submicron Design, Process Accuracy, And Interconnects.*

**Cheryl Ajluni**

In the past, the IEDM conference served as an excellent source of information regarding the development of new models and simulators. This year is no exception, as the conference offers sessions on everything from advanced device modeling, process modeling, compact modeling, interconnect modeling, advanced device and simulation, and process/device model characterization and applications. With such a wide range of sessions, and a more impressive variety of papers, there's bound to be something to meet your needs.

For example, as designs become increasingly complex and geometries continue to shrink, accurate modeling and simulation techniques become crucial to a design's overall success. Lack of accurate models oftentimes leads to overdesigning—and in some cases even underdesigning—by the engineer. If you overdesign, you fail to take full advantage of the possible performance capabilities of the technology you're using. With underdesigning, you run the risk of the design not working at all.

Ultimately, you need to use accurate models right from the start. That way, when you simulate your design, you're doing so with the most accurate representation possible. This is a key point. In a deep-submicron (DSM) design environment, the chance for propagating errors resulting from inaccurate design information becomes too great a risk. Indeed, it's a gamble that could end in design failure. Accurate models and simulation tools must be the designer's first line of defense in preventing this catastrophe.

## Process Modeling

This is exactly why researchers at Texas Instruments, Dallas, Texas, in conjunction with Louisiana Technical University, Ruston, La., have devised a new approach for modeling the contact resistance of silicide-source/drain structures. The approach combines TSUPREM-4 simulations, physical models, and optimally chosen electrical test structures for the simulation and modeling of the silicide-source/drain region, as well as the contact resistance for silicided devices.

Such a model is crucial for a variety of low-power and mixed-signal applications, since a reduction in contact resistance equals improved transistor performance. But to reduce this value, the designer must first accurately and fully simulate and model it. Unfortunately, this isn't as easy as it sounds, because the contact resistance is dependent on the complex interactions between the silicide and the heavily doped source/drain diffusion region.

With the new modeling approach, though, designers now have a way to link electrical performance with the processing and structural variables forming the silicide-source/drain region. Researchers have tested this approach over a wide range of fabrication-process variables. It was shown to not only significantly improve transistor performance, but also reduce manufacturing costs. Accurate predictions minimize the number of experiments required for technology development. Further details of this approach are highlighted in paper 27.5, "An Integrated Approach for Accurate Simulation and Modeling of the Silicide-Source/Drain Structure and the Silicide-Diffusion Contact Resistance."

## Advanced Device Simulation

The Massachusetts Institute of Technology, Cambridge, Mass., and IBM Austin Research Laboratory, Austin, Texas, have come up with a new methodology. Using timing analysis, coupled with post-extraction net adjustment, they can account for interconnect-structure variation. The method is so efficient that researchers predict it can analyze thousands of nets for variation without having to modify current computer-aided design (CAD) tools.

Effectively, this methodology works as follows: During extraction of nominal net capacitance and resistance, additional intermediate information regarding the geometry of neighboring shapes is obtained and stored. This information is then used to analyze the effects of each source of variation. A linearized model is subsequently created that represents the delta capacitance and, when appropriate, the resistance. The change in capacitance is then added to or subtracted from the nominal parameter capacitance extractions.

Finally, the RC network is formed, moments are generated, and a timing analysis based on RICE is performed. Further details on this approach are presented in paper 28.6, "Modeling of the Effects of Manufacturing Variation and High-Speed Microprocessor Interconnect Performance."

## Process Modeling

Also worth noting is paper 18.7, "Monte Carlo 2-D and 3-D Simulation of Ion Implantation in Topographically Complex Structures," from the University of Texas, Austin, Texas. The simulator described in the paper—the Topography-based Monte Carlo Transport (TOMCAT)—is capable of predicting the impurity and defect concentrations in 2D structures. The topography is arbitrary and specified by the user. A variety of materials, whether crystalline or amorphous, can be handled by the tool. As an added benefit, impurity and defect concentration profiles from a

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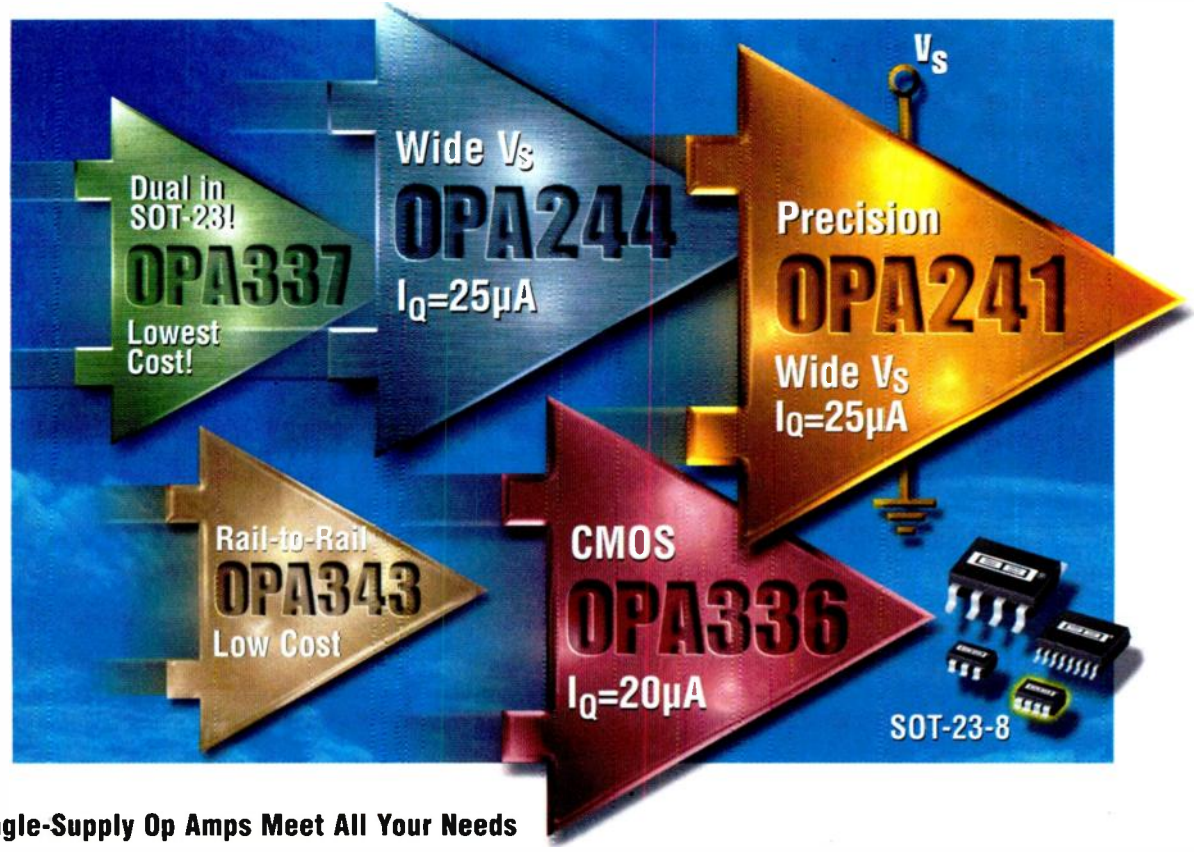


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|---|---|---|---|---|---|---|---|---|
| OPA241 | Precision, Wide $V_S$, *micro*Power | S, D, Q | SO-8 | +2.7 to +36 | 0.025 | 0.035 | 0.25 | $0.88 |
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| OPA337 | CMOS, Lowest Cost, Smallest | S, D | SOT (incl. dual!) | +2.5 to +5.5 | 0.525 | 3 | 3 | $0.25 |
| OPA340 | CMOS, High Speed, Rail-to-Rail I/O | S, D, Q | SOT, MSOP, SSOP | +2.5 to +5.5 | 0.750 | 5.5 | 0.5 | $0.46 |
| *OPA342** | CMOS, Gen. Purpose, Rail-to-Rail I/O | S, D, Q | SOT, MSOP, SSOP | +2.5 to +5.5 | 0.150 | 1 | 6 | $0.51 |
| OPA343 | CMOS, Low Cost, Rail-to-Rail I/O | S, D, Q | SOT, MSOP, SSOP | +2.5 to +5.5 | 0.850 | 5.5 | 8 | $0.33 |
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previous sequence of implants can be specified as a part of the structure.

The proposed tool is so flexible that it even allows the generating of model parameters for arbitrary combinations of ions and target materials. Researchers report that using the simulator results in improvements in CPU time over standard UT-MARLOWE simulations by up to three orders of magnitude with no loss of accuracy.

Paper 18.8, "New Analytic Models and Efficient Parameter Extraction for Computationally Efficient 1-D and 2-D Ion Implantation Modeling," also hails from the University of Texas. It proposes computationally efficient analytic models that consider local damage levels for 2D implantation. This development is significant, since the rapid progress of CMOS-process technology has led to increased process complexity and fabrication cost, making accurate, computationally efficient ion-implantation models a must. And, the paper details a new approach to 2D analytic ion implant simulation. Taking implant-induced damage into account, it also generates 2D interstitial/vacancy and impurity profiles.

## Interconnects

Aside from death and taxes, one thing in life is certain. As designers venture into an increasingly complex DSM environment, interconnects will play a major role in the design process. Recognizing this fact, researchers from Stanford University's Center for Integrated Systems, Stanford, Calif., and Ericsson Components, Kista, Sweden, have devised a 3D modeling approach for the characterization and design optimization of bonding wires.

This method captures the geometry from scanning-electronic-microscope (SEM) photos. Based on that geometry, the electrical parameters are then extracted. A Java program was developed to extract the 3D bondwire geometry and generate the input files. The simulators can then extract the electrical parameters for the structure. Research shows the extracted electrical parameters standing in good agreement with measured data. Other details of this development are highlighted in paper 11.5, "A Fast 3-D Modeling Approach to Parasitics Extraction of Bonding Wires for RF Circuits."

A similar effort comes from Carnegie Mellon's Department of Electrical and Computer Engineering, Pittsburgh, Pa. Detailed in paper 11.6, "Equipotential Shells for Efficient Partial Inductance Extraction," their technique relies on the use of filament currents, rather than point-like current distributions, and equipotential shells for the partial-inductance extraction. This spherical shell partial-inductance approximation is shown working for both on-chip and system-level extraction.

## Compact Modeling

In the past, extensive studies were performed on 1/f noise for a number of reasons: its influence on certain critical VLSI design parameters, such as noise figure and oscillator phase noise; its insight into device physics; and its role as an evaluation tool assessing oxide reliability. One discovery uncovered by these studies is the fact that random-

telegraph-signal (RTS) events, and the associated 1/f noise, are becoming critical issues for advanced, low-power analog and mixed-mode circuitry.

To address this concern, Rockwell Semiconductor Systems, Newport Beach, Calif., and the University of California, Irvine, Calif., developed BSIM3-compatible noise models. As detailed in paper 4.3, "BSIM3 Based RTS and 1/f Noise Models Suitable for Circuit Simulators," the models are based on the effects of band-bending fluctuations associated with single-carrier trapping. To date, their use has led to very accurate modeling of the gate- and drain-bias dependence of 1/f noise.

Paper 4.4, "A Physically Based Model for Low Frequency Noise of Poly-Silicon Resistors," details the work of researchers from Siemens AG Corporate Technology, Munich, Germany, and the Technical University of Munich in Munich, Germany. Their development is significant because analog parameters (in this case the noise of resistors realized by polysilicon layers) have become an increasingly important issue in CMOS integrated-circuit design. This new model, which can be implemented into a circuit simulator, addresses this by effectively explaining the 1/f noise behavior of highly doped polysilicon resistors as a function of frequency and operating point.

Similarly, Paper 4.5, "Ratio Based Hot-Carrier Degradation Modeling for Aged Timing Simulation of Millions of Transistors Digital Circuits," from Matshushita Electric Industrial Co., Kyoto, Japan, and BTA Technology, Santa Clara, Calif., details how researchers devised a model for aged-timing simulation of large circuits. Relying on the use of gate-level representation, the model makes aged-timing simulation much larger and faster than the conventional transistor-level approach, which used CMOS I-V characteristics.

## Advanced Device Modeling

Silicon-germanium (SiGe) devices are believed to be the most promising candidates for improving PMOSFET performance in silicon ICs. Recognizing this fact, researchers from the University of Bremen, Bremen, Germany, developed full-band Monte Carlo simulations to be used with such devices. The full-band Monte Carlo code is based on scattering models and band structures calculated with the non-local empirical pseudopotential method. The valence and conduction bands are discretized with non-uniform grids. Particle transfers via hetero interfaces are treated consistently with the full-band structure. Further details of this development are summarized in paper 33.4, "Full-Band Monte Carlo Simulation of a 0.12-μm Si-PMOSFET with and without a Strained SiGe-Channel."

Paper 33.5, "A New Model of Tunneling Current and SILC in Ultrathin Oxides," from researchers at the University of Padova, Padova, Italy, spotlights another modeling development. Based on a double-box approximation of the oxide conduction band, the model can quantitatively fit the characteristics of the MOS tunneling current, such as quantum oscillations of the Fowler-Nordheim current and low-field, stress-induced leakage current (SILC).

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# Sensors And Displays Take The Spotlight At IEDM

*Advanced Device Structures And New Technologies Open The Door For Newly Emerging Display And Sensor-Based Applications.*

**Cheryl Ajluni**

In recent years, detectors, displays, and sensors have garnered a lot of attention at conferences like IEDM. In part, this is because of the new, innovative, and often low-cost applications they enable in areas ranging from medical and instrumentation to consumer products. Undeniably, these technologies will continue to have an enormous impact on the way we live and work.

## TFTs

One area where a great deal of innovation is occurring is thin-film transistors (TFTs). TFTs, often integrated into active-matrix liquid-crystal displays (AMLCDs), are a means to address (or switch) each display pixel. While the technology offers significant benefits compared to other display technologies, it's not without shortcomings. Recognizing its failings, many have sought to improve its long-term shot at success by identifying and developing solutions that overcome any limitations.

One shortcoming is the choice of substrate. Glass panels are used for such things as large-area electronic applications. Such substrates are available in large areas, at low cost, and with flat and smooth surfaces that simplify device processing. But, glass is also heavy and fragile. Plastic, on the other hand—or some other flexible substrate—makes a more mechanically robust display for handheld computer or other low-cost electronic applications and displays.

With this in mind, researchers from Pennsylvania State University in University Park came up with a low-temperature process for combining a 250°C hydrogenated amorphous silicon (a-Si:H) TFT process with polymeric substrates. The result is a-Si:H TFT ICs fabricated on flexible polymeric Kapton substrates. Their performance matches that of similar devices fabricated on glass, but also is sufficient for low-cost, flexible electronics.

As detailed in paper 10.2, "Tri-Layer a-Si:H Integrated Circuits on Polymeric Substrates," researchers were able to use standard processing techniques (plasma-enhanced chemical-vapor deposition) and a silicone-gel mountant to fabricate the ICs. The silicone gel used for the adhesive layer was crucial for maintaining substrate flatness. Due to its inherently pressure-sensitive nature, it also improved thermal transfer.

In a similar development, researchers from the Lawrence Livermore National Laboratory, Livermore, Calif., in conjunction with the University of California at Berkeley, found a method for fabricating polysilicon TFTs at 100°C on a flexible plastic substrate. As highlighted in paper 10.3, "Polysilicon Thin Film Transistors Fabricated at 100°C on a Flexible Plastic Substrate," the substrate of choice was polyethylene terephthalate (PET). This low-cost, flexible, and rugged material was chosen for a number of reasons. Optically transparent, it's suitable for both transmissive and reflective displays. An excimer laser was used for the laser-doping process to crystallize the undoped channel regions of the polysilicon film. A second laser step then doped the source/drain regions. The resulting TFTs fabricated displayed $I_{ON}/I_{OFF}$ ratios greater than $10^6$, and electron mobilities greater than 5 $cm^2/V_S$.

Finding the appropriate TFT substrate is only one part of the problem. If you can't model or quantify the effects of various parameters, such as grain-size variation on poly-TFTs, it's virtually impossible to quickly estimate device variation when a process is changed.

Until now, such a capability hasn't existed. But, thanks to researchers from California's Stanford University, a model for grain-size variation now exists. As explained in paper 10.8, "Modeling of Grain Size Variation in Polycrystalline Thin Film Transistors," the number of grains in a given transistor can be modeled using a Poisson area scatter. The method is similar to that used for the basic modeling of manufacturing-defect densities. Now, technologies that can remove the source of randomness, or device variation, such as seeded crystallization and sequential-lateral solidification (both of which are now under development), may finally improve device-to-device uniformity.

## FEDs

An option to the more traditional AMLCD, the field-emission display (FED) offers a number of significant features, including the ability to produce bright images. But, it too has its drawbacks. Its high-emissions threshold voltage and lack of low-voltage phosphors necessitate large power consumption.

One way to deal with this obstacle is to develop better field-emitter arrays (FEAs). Researchers at the Massachusetts Institute of Technology (MIT) in Cambridge did this when they made a 100-nm aperture FEA. As summarized in paper 32.1, "100-nm Aperture Field Emitter Arrays for Low Voltage Applications," interferometric lithography was used to fabricate the FEA. This resulted in the highest cone densities reported to date, turn-on voltages as low as 12 V, and the ability for current densities to increase by 1000 just by varying the gate voltage by 5 V.

A scaled-down silicon (Si) FEA with 90-nm-diameter gates hails from NEC Corp., Kanagawa, Japan. Summarized in paper 32.2, "A Si Field Emitter Array with 90-nm Diameter Gate Holes," this FEA has a threshold voltage of 22 V at 1 nA/tip. A unique two-step thick insula-




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tor underneath the gate electrode enables the insulator to be kept thick. The long, creeping distance between emitter and gate electrodes is maintained even if gate diameter is reduced.

Something else of interest comes from researchers at Lehigh University, Bethlehem, Pa., in conjunction with FED Corp., Hopewell Junction, N.Y. The first of its kind—a VGA polysilicon, active-matrix organic LED (OLED) display—also features an innovative new driving method. The method calls for connecting the address line to the drains of all the pixel transistors. Data is then written to the transistor gates. Two different versions of this display type were built so researchers could investigate OLED performance characteristics. Both displays featured VGA resolution with a 40-mm diagonal. But, one was a single transistor/pixel design with a 50-µm pixel size, while the other used two TFTs per 100-µm pixel.

## LEDs

Until now, only passive monochrome displays have been built from OLEDs. That's what's significant about the VGA polysilicon OLED development. With an active-TFT display design, the technology can be scaled down to miniature sizes. This development is highlighted in paper 32.5, "Polysilicon VGA Active Matrix OLED Displays—Technology and Performance."

The Microelectronics Institute, Athens, Greece, and the National Institute for Microtechnology, Bucharest, Romania, teamed up to provide another application for LEDs: a monolithic integration of LEDs, detectors, and silicon-nitride fibers on a silicon chip. This emitter/detector system couples light with 30% efficiency—a big improvement compared to the 1% coupling efficiencies in compound semiconductor devices integrated by microbonding techniques. The LEDs are silicon avalanche diodes that emit light when reverse-biased beyond the breakdown voltage. The detectors—standard pn junctions—are optically coupled to the light emitters by $Si_3N_4$ waveguides.

This innovation derives from the way in which the $Si_3N_4$ fiber aligns to the emitter and detector, as well as the way it bends from the field oxide to the optical link's end points. Coupling to the light-emitter and detector planar devices occurs by bending the fiber so that it contacts both at a normal angle. To minimize light loss, $SiO_2$ spacers are then created at emitting and receiving ends. An overall field-oxide thickness of 2.5 µm assures relatively smooth bending and enough distance between the long horizontal segment of the fiber and silicon interface to minimize substrate losses. Further details can be found in paper 2.2, "Monolithic Integration of Light Emitting Diodes, Detectors, and Optical Fibers on a Silicon Wafer: a CMOS Compatible Optical Sensor."

## Image Sensors

CCD image sensors have recently been in the spotlight because they offer a number of benefits in digital-imaging applications, including night-vision sensors and digital still cameras (DSCs). For night vision, for example, researchers from MIT's Lincoln Labora-

tory, Lexington, Mass., developed a low-noise, 640-by-480 back-illuminated CCD image sensor capable of handling 106X optical overloads. Effectively, it offers high resolution down to starlight illumination levels. Further details of this CCD image are highlighted in paper 2.4, "640 x 480 Back-Illuminated CCD Imager with Improved Blooming Control for Night Vision."

Researchers from Philips Imaging Technology, Eindhoven, The Netherlands, have devised a 2/3-in., 2-Mpixel sensor for DSCs. While 1-Mpixel cameras remain common and 1.3-Mpixel cameras are now being introduced, this is the first report of a 2-Mpixel version. The sensor is a progressive scan, 1600-by-1280 frame-transfer CCD (FT-CCD) imager with 5.1-by-5.1-$\mu m^2$ pixels optimized for DSC applications. This pixel size yields a 10-bit dynamic range, with a small chip size of only 90 $mm^2$.

By combining a 1:4 subsample scheme, electronic optical low-pass filtering, and optimized and flexible subsample schemes, the imager lets up to 40 subsampled images at 280 line images/s be generated with a 25-MHz readout. This is detailed in paper 2.3, "A 2/3⊕ 2-Megapixel Progressive-Scan FT-CCD for Digital-Still-Camera Applications."

Researchers from the Jet Propulsion Laboratory, Pasadena, Calif., also could grab your interest. They've found a way to implement a snapshot CMOS imager without modifying the standard CMOS process or adding in-pixel storage elements. Their design calls for an electronically shuttered, snapshot CMOS imager implemented in a single-polysilicon standard CMOS process. The result is a chip capable of imaging at high shutter speeds and producing high-quality images free from motion artifacts. The 128-by-128-pixel prototype imager is fabricated in a 0.5-µm standard CMOS technology. Refer to paper 2.7, "A Snap Shot CMOS Active Pixel Imager fo Low-Noise, High-Speed Imaging," fo more on this technology.

## MEMS

The advent of design tools and pro cessing equipment have made it poss ble to realize micromachined micro electromechanical systems (MEMS) in silicon. Advances in this field will take center stage in Session 17.

In a noteworthy advance, researchers from the University of Michigan in Ann Arbor will describe a microscopic RF mixer/filter comprising interlinked microelectromechanical resonators and a low-loss capacitive mixe for frequency translation. Aimed a portable communications applications the MEMS mixer plus filter (paper 17.4 provides down-conversion of signals from 50 to 200 MHz. It also offers subsequent selective filtering at an IF of 34 MHz, with less than 5 dB of combined conversion and filter insertion loss.

Scientists at the Institute of Microelectronics, Singapore, have developed a novel, trench oxide-isolation techniqu for a single-crystal silicon, micromachined accelerometer. The aim is to us inexpensive single-crystal silicon fo fabricating surface micromachined a celerometers with better yield and pe formance. The results of this work w be presented in paper 17.5.

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# FT • FS SERIES MODUFLEX ® SWITCHERS

## DESCRIPTION

The FT and FS Series are comprehensive lines of ultra compact power factor corrected models derived from our Moduflex® family of switching power supplies. This series utilizes advanced technology to produce a high quality input current wave form that is compliant to the harmonic requirements of EN61000-3-2. Based on modular construction, "off the shelf" modules permit high volume manufacturing with an outstanding quality level assuring timely delivery at a competitive cost.

Three classes of output modules are available. The **STANDARD** outputs allow short duration surge currents on all auxiliaries for hard starting loads. Optional **CURRENT LIMITED** outputs have square current limiting and feature wireless droop current sharing. Optional **ENHANCED** outputs have square current limiting, one wire star point current share, output good logic signal with LED, nominal 5V local bias, individual inhibit and margining. For requirements that cannot provide minimum load on the main output, the **ZERO PRELOAD** option is available for main outputs up to 500 watts.

## DELIVERY

Choose stocked units or construct a model number using stocked modules for fast delivery. Otherwise, form a model from the adjacent page to meet your specific requirements. Contact factory for deliveries on models derived from non-stocked modules.

## FEATURES

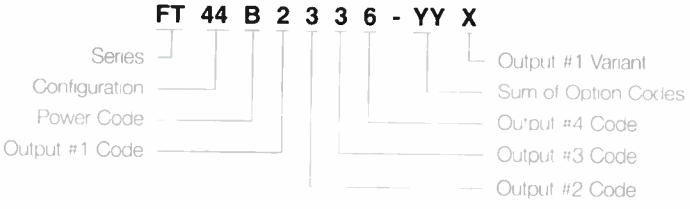
- 0.99 power factor.
- 5.5 watts per cubic inch.
- 1-7 outputs, 400-1000 watts.
- 120 kilohertz MOSFET design.
- Universal input.
- UL, CSA, TÜV (IEC, EN), CE.
- FCC, EN Class A EMI.
- IEC, EN Immunity.
- All outputs:
  - *Adjustable*
  - *Fully regulated*
  - *Floating*
  - *Overload and short circuit protected*
  - *Overvoltage protected*
- Standard features include:
  - *System inhibit*
  - *Fan output*
- Options and accessories include:
  - *Power fail monitor*
  - *Redundancy*
  - *Current Limited Outputs*
  - *Enhanced Outputs*
  - *Zero Preload*
  - *End fan cover*
  - *Top fan cover*
  - *Rack Assemblies*

## STOCKED MODELS - Available in 3 days.

| Max Power | Output 1 | Output 2 | Output 3 | Output 4 | Model* |
|---|---|---|---|---|---|
| 400W | 5V @ 50A | 12V @ 12A | 12V @ 12A | 5V @ 10A | FT46A2332-45P |
| 400W | 5V @ 50A | 12V @ 12A | 24V @ 6A | 12V @ 6A | FT46A2363-45P |
| 600W | 5V @ 60A | 12V @ 12A | 12V @ 12A | 5V @ 10A | FT46C2332-13P |
| 600W | 5V @ 60A | 12V @ 12A | 24V @ 6A | 12V @ 6A | FT46C2363-13P |

**400W models include power fail monitor, current limited modules, zero preload and end fan cover options. 600W models include the same options except fan cooling is built into the unit.*

## UNITS FROM STOCKED MODULES - Available in 2 weeks.




**Configuration:** Allowable quad output configurations are 42, 44, 46 and 48.

**Power Code:** Choose Power Code A through D for 400-750W models.

**Output Codes:** Select any outputs from the shaded area on the Output Types table consistent with the configuration chosen.

**Option Code:** Specify Option Code. Refer to the Option table. Codes 02 (redundancy) and 16 (enhanced) are excluded from models available in 2 weeks. Fan cooling is built into 600 and 750W units.

## OPTIONS

| Option Code | Function |
|---|---|
| 00 | None |
| 01 | Power Fail Monitor |
| 02 | Redundancy |
| 04 | Current Limited |
| 08 | Zero Preload |
| 16 | Enhanced |
| 32 | End Fan Cover |
| 64 | Top Fan Cover |

*Replace the YY with the sum of the Option Codes.*

## MODEL SELECTION

Models are available in power ratings of 400 to 1000 watts, with corresponding code letters A through E. See Power Code chart.

Output modules are available in six types: J, K, L, M, N and P in nominal power ratings from 75 - 500 watts. Type M, N and P modules are variable power rated depending upon the unit power rating. The M, N and P Module table directly below shows the corresponding multiplier applicable to the output current ratings of the M modules and allowable power ratings for the N and P modules. For example, a 750 watt multiple will have its M type module configured to produce 120A @ 5V or 12A @ 48V. The voltage and current rating of output modules are listed in the table of output types. This table assigns an alpha-numeric code designating the nominal voltage rating of the module.

| Power Code | Unit Power Rating | M Module Current Multiplier | | N/P Module* |
|---|---|---|---|---|
| | | Single Output | Multiple Output | Allowable Power Rating |
| A | 400W | 0.8 | 0.5 | 250W |
| B | 500W | 1.0 | 0.6 | 300W |
| C | 600W | 1.2 | 0.8 | 400W |
| D | 750W | 1.5 | 1.2 | 500W |
| E | 1000W | 2.0 | 1.5 | 750W |

**When an N or P module is used as the main output, the allowable power and the module current ratings must not be exceeded.*

| Output Types* | | | | | | |
|---|---|---|---|---|---|---|
| Output | | Module Type | | | | |
| Code | Volts | J Amps | K Amps | L Amps | M Amps | N/P Amps |
| 0 | 2 | 10 | 20 | 30 | 100 | 60 |
| 1 | 3.3 | 10 | 20 | 30 | 100 | 60 |
| 2 | 5 | 10 | 20 | 30 | 100 | 60 |
| 3 | 12 | 6 | 12 | 24 | 42 | 42 |
| 4 | 15 | 5 | 10 | 20 | 33 | 33 |
| 5 | 18 | 4 | 8 | 16 | 28 | 28 |
| 6 | 24 | 3 | 6 | 12 | 21 | 21 |
| 7 | 28 | 2.5 | 5 | 10 | 18 | 18 |
| 8 | 36 | 2 | 4 | 8 | 14 | 14 |
| 9 | 48 | 1.5 | 3 | 6 | 10 | 10 |
| A | 2.2 | 10 | 20 | 30 | 100 | 60 |
| B | 2.4 | 10 | 20 | 30 | 100 | 60 |
| C | 2.7 | 10 | 20 | 30 | 100 | 60 |
| D | 3 | 10 | 20 | 30 | 100 | 60 |
| E | 3.6 | 10 | 20 | 30 | 100 | 60 |
| F | 4 | 10 | 20 | 30 | 100 | 60 |
| G | 4.5 | 10 | 20 | 30 | 100 | 60 |
| H | 5.7 | 10 | 20 | 30 | 90 | 60 |
| J | 6.3 | 10 | 20 | 30 | 80 | 60 |
| K | 7 | 9 | 18 | 30 | 70 | 60 |
| L | 8 | 8 | 16 | 30 | 62 | 60 |
| M | 9 | 8 | 15 | 30 | 56 | 56 |
| N | 10 | 7 | 14 | 30 | 50 | 50 |
| P | 11 | 7 | 13 | 27 | 45 | 45 |
| Q | 13.5 | 6 | 11 | 22 | 37 | 37 |
| R | 17 | 5 | 9 | 18 | 30 | 30 |
| S | 19 | 4 | 8 | 16 | 26 | 26 |
| T | 21 | 4 | 7 | 14 | 24 | 24 |
| U | 23 | 4 | 7 | 13 | 22 | 22 |
| V | 26 | 3 | 6 | 12 | 19 | 19 |
| W | 29 | 3 | 5 | 10 | 17 | 17 |
| X | 32 | 2 | 5 | 9 | 16 | 16 |
| Y | 40 | 2 | 4 | 8 | 13 | 13 |
| Z | 44 | 2 | 4 | 7 | 12 | 12 |

*Multiple output modules of a given type are arranged in ascending order by voltage magnitude in the same sense as the output number sequence in the configuration diagrams.*
**Shaded ratings are stock.*

## HOW TO ORDER

To form the proper model number defining a custom requirement, select the letters FS or FT to designate the series, then choose the desired configuration and list the configuration code. Insert the power code letter for the power level and follow with the output code numbers or letters for each specific output. Enter a dash and from the option table insert the sum of the option codes. Where lower power is desired for the main module, an N module can be substituted and is denoted by a letter N in the output variant position. In addition, when no preload is available for the main output, choose Option Code 08 and add a P in the output variant position. For an enhanced **main** and **current** limited auxiliaries, specify both 04 and 16 option codes.

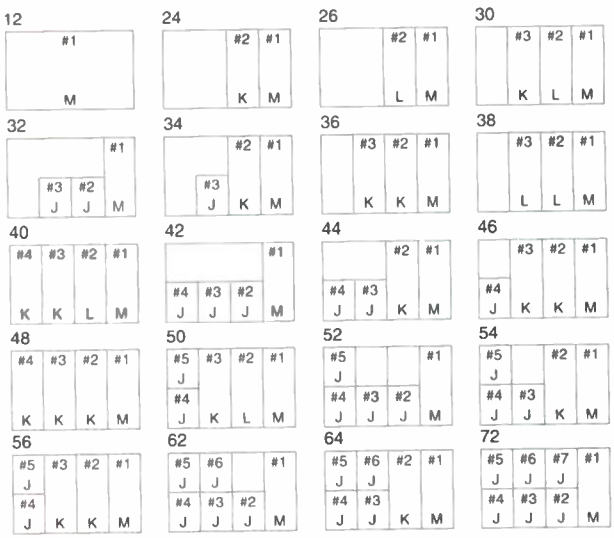
### HARMONIC CORRECTED 500W QUAD SWITCHER

**FT 44 B 2 3 3 6 - YY X**

- FT — Series
- 44 — Configuration
- B — Power Code
- 2 — Output #1 Code
- 3 — Output #2 Code
- 3 — Output #3 Code
- 6 — Output #4 Code
- YY — Sum of Option Codes
- X — Output #1 Variant

### OUTPUT CONFIGURATIONS

The boxes below are diagrammatic representations of the power supplies as viewed from the output end. The two-digit numbers above the boxes are the configuration codes.

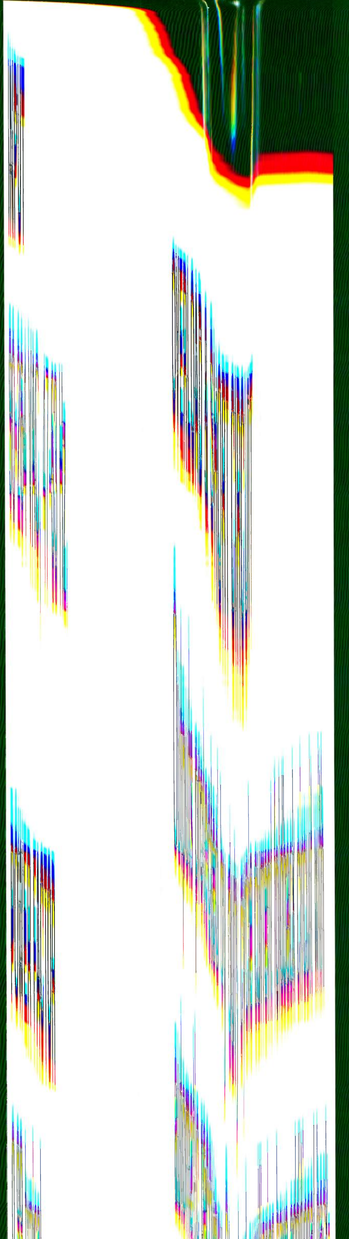



*Refer to the table below for allowable configurations by series.*

| Output Config | Unit Power Rating | | | | |
|---|---|---|---|---|---|
| | 400W | 500W | 600W | 750W | 1000W |
| 12 | • | • | • x | • x | x |
| 24 | • | | | • x | |
| 26 | | • | • x | • x | x |
| 30 | | | | | x |
| 32 | • | | | • x | |
| 34 | • | • | • x | • x | |
| 36 | • | • | • x | • x | x |
| 38 | | | | | x |
| 40 | | | | | x |
| 42 | • | • | • x | • x | |
| 44 | • | • | • x | • x | x |
| 46 | | • | • x | • x | x |
| 48 | | | x | | x |
| 50 | | | | | x |
| 52 | • | • | • x | • x | x |
| 54 | | • | • x | • x | x |
| 56 | | | x | | x |
| 62 | | • | • x | • x | x |
| 64 | | | x | | x |
| 72 | | | x | | x |

• *Represents allowable configurations for the FT Series.*
x *Represents allowable configurations for the FS Series.*

## SPECIFICATIONS



FCC 20780 Part 15/EN 55022, Class A Conducted. EN 61000-3-2, Harmonics. EN 61000-3-3, Voltage Fluctuations.

**IMMUNITY**
IEC 1000-4-2/EN 61000-4-2, Electrostatic Discharge. IEC 1000-4-3/EN 61000-4-3, Radiated Field. IEC 1000-4-4/EN 61000-4-4, Electrical Fast Transients. IEC 1000-4-5/EN 61000-4-5, Level 3 Surge. IEC 1000-4-6/EN 61000-4-6, Conducted Field.

**INPUT SURGE**
230 VAC - 38 amps max. 115 VAC - 19 amps max.

**EFFICIENCY**
75% typical

**HOLDUP TIME**
20 milliseconds from loss of AC power.

**OUTPUTS**
See model selection table. Outputs are trim adjustable ±5%.

**OUTPUT POLARITY**
All outputs are floating from chassis and each other and can be referenced to each other or ground as required.

**LINE REGULATION**
Less than ±0.1% or ±5mV for input changes from nominal to min. or max. rated values.

**LOAD REGULATION**
±0.2% or ±10mV for load changes from 50% to 0% or 100% of max. rated values.

**MINIMUM LOAD**
Main output requires a 10% minimum load for full output from auxiliaries. Use Option 08 if no minimum load is available for mains up to 500 watts. Singles require no minimum load.

**RIPPLE & NOISE**
1% or 100 mV, pk -pk, 20 MHz bandwidth.

**OPERATING TEMPERATURE**
0.70°C. Derate 2.5% / C above 50°C.

**COOLING**
A min. of 10 LFS* for models without internal fans directed over the unit for full rating. Two test locations on chassis rated for max. temperature of 90°C. 600 watt, 750 watt and 1000 watt models have built-in ball bearing fans.
*Linear feet/second.

**TEMPERATURE COEFFICIENT**
±0.02%/°C

**DYNAMIC RESPONSE**
Peak transient less than ±2% or ±200 mV for step load change from 75% to 50% or 100% max. ratings.

**RECOVERY TIME**
Recovery within 1%. Main output - 200 microseconds. Auxiliary outputs - 500 microseconds.

**SAFETY**
Units meet UL 1950, CSA 22.2 No. 950, EN 60 950, IEC 950.

**ISOLATION**
Conforms to safety agency standards.

**INPUT UNDERVOLTAGE**
Protects against damage for undervoltage operation.

**SOFT START**
Units have soft start feature to protect critical components. Standard on all outputs.

**REVERSE VOLTAGE PROTECTION**
All outputs are protected up to load ratings.

Mini automatic recovery when overload is removed.

**THERMAL SHUTDOWN**
Circuit cuts off supply in case of local over temperature. Units reset automatically when temperature returns to normal.

**FAN OUTPUT**
Nominal 12 VDC @ 12 watts maximum.

**INHIBIT**
TTL compatible system inhibit provided. Option 16 has individual output inhibit.

**REMOTE SENSING**
On all outputs except standard and 04 Option outputs 75 watts or less.

**SHOCK & VIBRATION**
Shock per MIL-STD 810-E Method 516.4, Procedure I. Vibration per MIL-STD 810-E Method 514.4, Category 1, Procedure I.

**MECHANICAL**

| CASE | SERIES | WATTS | H | x | W | x | L |
|---|---|---|---|---|---|---|---|
| 1 | FT | 400W/500W | 2.50" | x | 4.93" | x | 8.00" |
| 3 | FT | 600W | 2.56" | x | 5.08" | x | 11.00" |
| 4 | FS | 500W | 2.56" | x | 5.08" | x | 11.00" |
| 5 | FT | 750W | 2.63" | x | 5.20" | x | 10.00" |
| 6 | FS | 750W | 2.63" | x | 5.20" | x | 11.63" |
| 7 | FS | 1000W | 2.56" | x | 7.13" | x | 11.63" |

**OPTIONS**

**POWER FAIL MONITOR**
Optional circuit provides isolated TTL and VME SYF compatible ACFAIL signal providing 4 milliseconds warning before main output drops by 5% after an input failure. A SYSRESET signal following VME timing requirements is provided when an N module is used as a main output. Both logic signal outputs can sink current per the VME specification.

**REDUNDANCY**
Optional Or-ing diodes for hot pluggable N+1 redundant operation. For FS Series 500 watt & 750 watt models with 1:4 outputs. Main output current limited to 100 amps. Remaining outputs 16 amps max.

**CURRENT LIMIT**
Option provides on all outputs:
- Square current limit with auto recovery.
- Foldback droop current share for parallel or N+1 redundant operation.

**ENHANCED**
Option provides on all outputs:
- Square current limit with auto recovery.
- Single wire active current share for parallel or N+1 redundant operation.
- DC output good logic signal with LED indicator.
- Logic inhibit
- Nominal 5V bias.
- Margining.

**END FAN COVER**
Optional cover with brushless DC ball bearing end fan which provides the required air flow for full rating.

**TOP FAN COVER**
Same as above with fan cover mounted on top of the power supply.

**ACCESSORIES**
RA50 and RA75 Series 2U high rack assemblies provide hot pluggable interface and hold up to 3 FT Series 500 watt or 750 watt units respectively.



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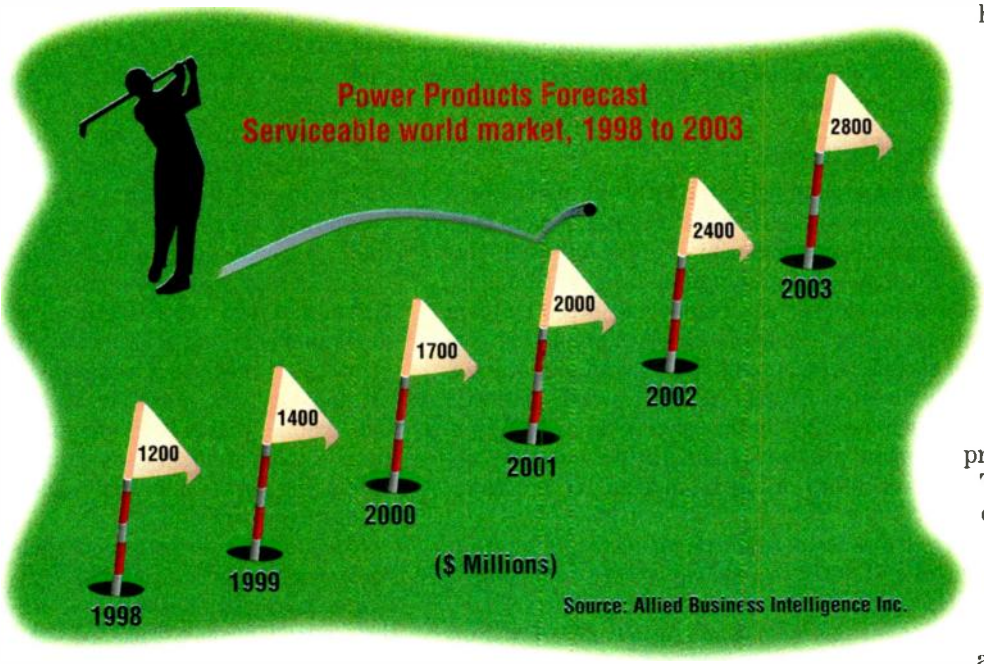
# ELECTRONIC DESIGN QUICK LOOK

Edited by Nancy Konish

MARKET FACTS

## Technology Chips Power Semiconductors Onto The Green

You're playing one of the toughest holes at the infamous Semiconductor Pines Course (and home for burnt-out professionals). You've got one shot to make it onto the green, and it's now decision time. Should you use the MESFET driver? Maybe that new HBT club? Or, perhaps your trusty old GaAs iron. You confidently stroll over to your golf cart and pull out a binder with "Allied Business Intelligence Inc." (ABI) on the cover. As the crowd watches, you quickly thumb through the pages, titled "Wireless Power Devices, Transistors, ICs, and Power Modules: Strategies, Technologies, and Trends." With a satisfied smile, you reach into your golf bag and pull out the cellular/PCS pitching wedge. You chip the ball right towards the 2003 flag, because that's when the power-semiconductor market will be worth a whopping $2.8 billion. That's after a predicted gain of 19% each year, which will be driven by cellular/personal communications service (PCS). As a result of the prominence of mobile voice-communications platforms, gallium-arsenide power-amplifier ICs are expected to grow at an average annual rate of 26% over the next five years. Still, not all semiconductor markets will benefit equally from the cellular/PCS boom. Manufacturers of GaAs transistors already lost a lot of their cellular segment to LDMOS power transistors for base stations, as well as GaAs monolithic microwave integrated circuits (MMICs) for handsets. Their growth rate is only expected to be 5% over the next five years. This minimal growth will stem almost completely from high-frequency applications like LMDS, broadband satellite projects, and point-to-point millimeter wave radio. Unfortunately, they're not the only suppliers set to experience a diminishing share. According to ABI, heterojunction-bipolar-transistor (HBT) processes account for close to 30% of the market for GaAs power-amplifier ICs. More gains are anticipated at the cost of MESFET processes. There will be double-digit growth for MESFET producers, but HBT is expected to account for a greater share of that future market. Suppliers of power-amplifier ICs might have bigger things to worry about, however. Currently, there's a lot of renewed interest in power modules from producers of cellular/PCS handsets. The rise of handset producers with less knowledge in RF/microwave design, combined with diminishing design times, are leading many manufacturers to use power modules. These modules offer easy installation at a low price, especially considering the cost of design time. Most of the existing cellular/PCS modules are silicon-based, but GaAs MMIC technology stands to become more prevalent in the future.

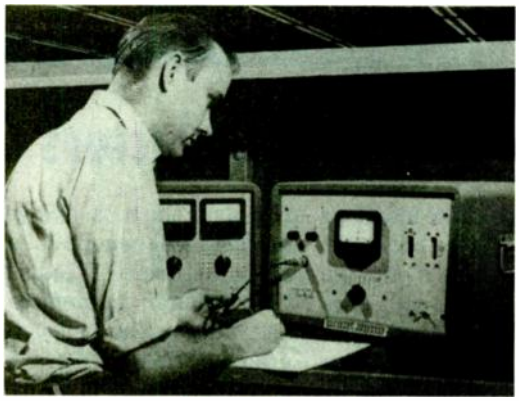



To obtain a copy of the report, contact Allied Business Intelligence Inc., 202 Townsend Square, Oyster Bay, NY 11771; (516) 624-3113; fax (516) 624-3115; www.alliedworld.com.—NK

## 40 YEARS AGO IN ELECTRONIC DESIGN

# Measuring RF Power Between 10 mW And 10 W

Conventional calorimeters and bolometers are useful instruments for the measurement of microwave power, but their range is limited. The calorimeter has a lower power limit in the 1 to 10 w range. The bolometer has an upper limit of 10 to 100 mw. The Hewlett-Packard model 434A rf power meter uses both calorimeter and bolometer techniques to close this gap. This description of the instrument's design is from B.P. Hand, HP development engineer.



The input of the 434A is a type-N connector which accepts power for measurement at any frequency from dc to 12 kmc. Power is read directly in watts and dbw on the meter, on ranges from 10 mw full scale to 10 w full scale. Response time is less than 5 sec, and an accuracy of about ±2 percent is obtainable.

The instrument consists of a self-balancing bridge, which has identical temperature-sensitive resistors (gages) in two legs, an indicating meter, and two load resistors—one for the unknown input power and one for the comparison power.

The input connector is terminated in a 50-ohm axial resistor, over which flows a thin film of oil. The oil, which is heated by the resistor, then flows over a nickel-wire resistance gage. A rise in oil temperature results in an increased gage resistance. When power is applied to the input, the resistance of the corresponding gage increases, unbalancing the bridge. The resulting signal is amplified, rectified, and fed to the feedback-head load resistor. This heats the corresponding gage and brings the bridge back toward balance. The meter reads the dc voltage across the feedback load resistor required to produce the matching rate of heat transfer. *(ELECTRONIC DESIGN, December 10, 1958, p. 40)*

*I'm still fascinated by the fact that a good engineer can get a variety of physical effects under control, as well as their sources of error, and make an instrument like this actually work.—Steve Scrupski*

## Tiny "Brains" Seen For Vending Machines

Doubling of sales in the automatic merchandising industry within the next five years will go hand in hand with new advances in control systems, says D.M. Strathern, Controls Co. of America v-p. Vending machines of the future, he told the National Automatic Merchandising Assn.'s 22nd annual convention in St. Louis, will have controls with the same degree of efficiency achieved by giant electronic computers. But they must be much smaller—in effect, miniature control systems. Research aimed at modification, simplification, and miniaturization of controls is being intensively directed, Strathern said, toward solution of control problems. These include such vending factors as mixing or blending, meter or measure, stop and start, control pressure, temperature and flow, control pressure differential, and control rotary or lateral motion. *(ELECTRONIC DESIGN, December 10, 1958, p. 9)*

*This is the first direct mention that I've seen of an embedded controller. However, even with today's microcontrollers, getting a good cup of coffee from a machine is still a little iffy.—Steve Scrupski*

*Steve Scrupski is a former Editor-in-Chief of ELECTRONIC DESIGN. Now semi-retired, he can be reached at scrupski@worldnet.att.net.*

# Let 'Em In On It

A common complaint from most employees is that they're never in on the "big plan." Decisions are made, departments are altered, personnel suffers drastic changes—and nobody outside of upper management has any idea what's happening. Well, it's common sense that this trend doesn't exactly boost morale. But even so, the bigwigs usually stand by their decision to keep information exclusive.

Aside from the employees' feelings, however, it's been found that keeping secrets can actually stifle a company's growth. This is especially true when it comes to a company's operations strategy. According to Rensselaer's Lally School of Management and Technology, if a company's operations strategy is not made clear to every employee, that strategy will be weakened by thousands of decisions made by the employees each day.

The school's research unearthed a large lack of consensus on corporate strategy between the managers and the people who operate the machines on the factory floor. In separate interviews, each group was asked to rank the importance that the company places on cost, quality, delivery, and flexibility. In most of the companies, operators and managers disagreed on what was most important to the company. In fact, the two groups only chose the same priority in a few instances.

According to Lally, the critical factor in determining a strategy's success is not necessarily which competitive priority is stressed (delivery, cost, quality, or flexibility). It's how well the priority is translated into a consistent set of decisions that support corporate strategy. If there isn't a consensus on the strategy, members of the firm will not pull in the same direction. It's this effort of each individual pulling for the team that makes the strategy work.

To find out more contact Chris McDermott, Lally School of Management and Technology, (518) 276-4861; e-mail: mcderc@rpi.edu.—**NK**

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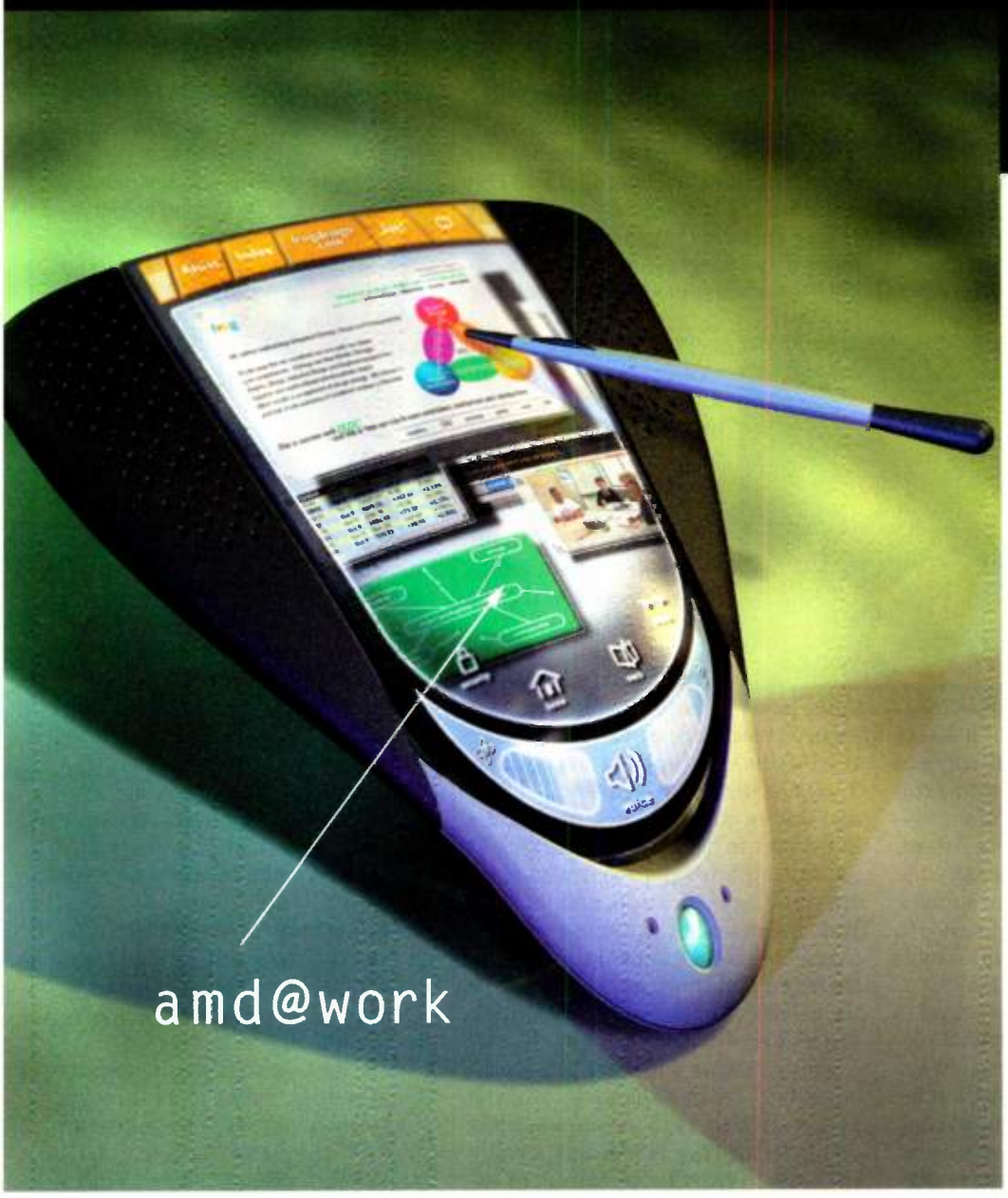


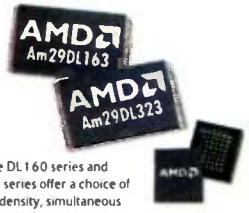


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MANAGING THE DESIGN FACTORY

# The Commander's Intent

The battlefield has always been a domain of great uncertainty. It's also a swift and unforgiving judge of sloppy thinking. Before the Germans attacked France in May 1940, French tacticians argued that it would take at least nine days for the Germans to pass through dense Belgian forests. They reasoned that the Germans, like the French, would not operate armor without support from the slower-moving infantry and artillery.

The Germans didn't follow the rules. They moved their armor forward without this support, crossing the Meuse river into France in four days. The French were so unprepared for this that the Germans ended up at the English Channel seven days later. The French tacticians were logical and articulate, but wrong.

DON REINERTSEN

This combination of high uncertainty and unambiguous feedback makes the military a useful place to look for some time-tested ways of dealing with uncertainty. In this column, I want to focus on one of these—the concept of Commander's Intent. Any operational plan produced by the military has a brief statement summarizing what the commander intends to accomplish by the operation. Why is this statement so important?

To answer this question, we need to understand the military attitude towards planning. Planning has always been important in the military, but for very different reasons than most civilians suspect. The military doesn't plan because it believes that war is predictable. In fact, it's a classic military adage that, "No war plan survives the first shot of battle." The military plans meticulously so that they have a common baseline, or reference point, from which to make changes. You can't move up all the events in the plan by one hour if there is no plan.

How, then, does the military deal with the situations that hadn't been anticipated in the plans? They place intelligent, well-trained forces on the battlefield and make sure that these forces understand the intent of their mission. Far from encouraging mindless robotic behavior, the modern military believes that battles are won by soldiers who can both fight and think.

The military correctly recognizes that many unanticipated obstacles and opportunities will come up in the course of the battle. They realize that the people closest to the situation must make judgments on how to exploit the advantages and overcome the hurdles.

This is where intent comes in. When you know what the overall objective is, you can make judgments in such a way that you're relentlessly driving to achieve this objective. Without this, you're stuck mindlessly adhering to the letter of the plan.

What does this have to do with product development? Too often, development teams are clueless regarding the business intent of the product. They are simply given a detailed plan and told to adhere to it. Granted, it's important to have a plan. One should not attempt development without a schedule, specification, and budget. But, if you do not communicate the overall business intent of the project, teams cannot intelligently deal with the inevitable obstacles and opportunities that appear along the way.

Never create a project plan without briefly stating the mission of the product. This is the compass that points to the true North and permits the team to react to the turbulent environment of modern development. If you want a self-managed team, you better give them a clear sense of their mission.

*Don Reinertsen is a consultant specializing in product development management. He is coauthor of "Developing Products in Half the Time" and author of the new book, "Managing the Design Factory." Reinertsen & Associates, (310) 373-5332; e-mail: DonReinertsen@compuserve.com.*

# Data On The Fly

To gain insight into nature's problem-solving strategies, the NEC Research Institute, Princeton, N.J., is investigating signal processing in the visual system of the blowfly. Compared to humans, the fly has a sophisticated visual sensing, processing, and control system. It can stop instantly in midflight, hover, turn on its longitudinal body axis, fly with its legs up, loop the loop, somersault, and sit on the ceiling—all in a fraction of second.

The work is expected to help NEC develop better sensor and signal-processing products. But, just how do you investigate such a small and active insect? "Simple," answers researcher R.R. de Ruyter van Stevenink. "We capture them in a bucket outside our facility, and keep them fed once they're caught and in the lab."

"Then, we snake the fly through a tubing that gets narrower and narrower until the fly's head projects at the end of the tube, but its shoulders prevent it from coming out. We insert a microprobe into its head (brain) for connections to an oscilloscope, mount it on a stand, and view it through a microscope."

So far, results indicate that flies have an "optimal processing" system. They make the best possible use of the information gathered by their sense organs. Somewhat similar to a CCD camera, a fly's eye consists of an array of about 5000 pixels. Acting as photoreceptors that operate at noise levels approaching those of photon shot noise, they're close to being ideal photon counters.

The fly's neurons receive signals from the photoreceptors through chemical synapses. This suggests that the information the fly acts on is not significantly degraded by synaptic transmission. Also, the fly's brain follows the general rule of an optimal processor. The computational quality level increases in a high signal-to-noise ratio environment, and vice versa.

For more information, contact the NEC Research Institute at (609) 520-1555, or e-mail: info@research.nj.nec.com.

**Roger Allan**

# The Day The World stood Still

The Wizard of Ooze and his Slimy Sycophantic Syndicate of Psychos hit Teletropolis; oozies blazing. Now the network capital wakens to find itself mired in muck, stuck in slime, and steeped in sludge. And the weather's lousy too.

Ladies first! Up and ATM, sister.

We get results Ether way.

Teletropolis is too slug-ish for my taste.

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Thanks to HI FIBER's robust character and the LAN-WAN TWINS' fast response, traffic's flowing faster than ever! So, fellow superheroes, take care crossing the streets!!!


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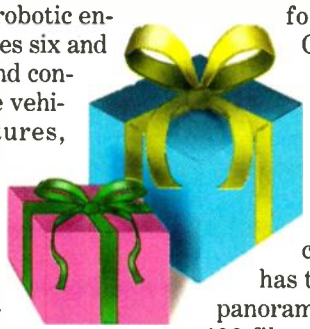
## JUST 4 THE KIDS

As the holiday season draws closer, many search for that one special gift for the children in their lives. To help you, I've put together a list of my top 10 favorite electronic toys. If you come across any other favorites, please e-mail them to me at *williamsofsm@lightspeed.net*. I will periodically update my list throughout the year and I'd love to get your ideas. In the meantime, I wish you all a very Happy Holidays and the best of luck shopping for toys. Take my advice—start early!

**1. Robotic Arm Trainer.** This device was developed to assist children ages ten to twelve in understanding robotics. Using the Robotic Arm, the young engineer can build and then command the unit with five switches. A wire controller lets the child manipulate the grippers of the arm to grab, release, lift, lower, rotate, rest, and pivot sideways 360 degrees. The five motors and joints allow full flexibility. It retails for about $69.95. For more information, contact Elekit Company, 1160 Mahalo Pl., Compton, CA 90220; (310) 638-7970; *www.owirobot.com*.

**2. Robotix Construction System.** The Robotix Construction System is based on the science of real robotic engineering. Children ages six and up can build, power, and control intergalactic space vehicles, futuristic creatures, and lifesize working robots. Both starter sets and more complicated sets, such as Robo-Rex and Task Force Beta, are available. They sell for approximately $7.99 to $199.99, respectively. Contact Learning Curve International, 314 West Superior St., Chicago, IL 60610; (800) 704-8697; *www.learningcurve.com*.



**3. Power Tower Crane.** This product includes 1555 pieces and motors that children nine to twelve can transform into a 5 1/2-feet tall working tower with a giant swinging boom. The boom can be controlled by the child using a power controller. The Power Tower Crane sells for approximately $109.99. To find out more, contact K'NEX Industries Inc., 2990 Bergey Rd., Hatfield, PA 19440; (800) 543-5639; Internet: *www.knex.com*.

**4. Tonka Workshop CD-ROM Playset.** This interactive product is for children ages three and up. They create, build, and play dozens of fix-it missions while using a user-friendly interface. Simply fit the playset over the keyboard and strap it into place. Then, insert the CD-ROM. The tools control the action on the computer screen. The Tonka Workshop CD-ROM set sells for approximately $39.95. For more information, contact Hasbro Interactive, 50 Dunham Rd., Beverly, MA 01915; (800) 683-5847; *www.hasbro-interactive.com*.

MARIFRANCES WILLIAMS

**5. MathShark.** This product starts with teaching basic math and advances to pre-algebra practice. Children ages six to twelve can use this electronic handheld device to move through all the basic major math skills. It includes a full-functioning calculator and eight levels of difficulty in seven skill categories. MathShark sells for approximately $39.95. Contact Educational Insights Inc., 16941 Keegan Ave., Carson, CA 90746; (800) 995-4436; Internet: *www.edin.com*.

**6. Advantix Switchable.** This one-time-use camera for children ages six to twelve has the ability to switch to two panoramic print sizes. Loaded with 400 film, the camera permits your child to learn to take pictures and observe their environment and the people in it. Advantix Switchable sells for approximately $16.95. Find out more from Eastman Kodak, 343 State St., Rochester, NY 14650; (800) 242-2424; *www.kodak.com*.

**7. BabyWow!** This software program is intended for babies and toddlers ages nine months to three years. Based on research that indicates babies learn and benefit from early stimulation, this program uses sound and colorful images to stimulate the child mentally. Available in eight different languages, it's meant to be an extension to the attention and playfulness a baby needs. Now available, it sells for approximately $34.99. Contact BowWow House at (408) 264-4334; *www.babywow.com*.

**8. Teddy Ruxpin.** This lovable teddy bear is made for children ages two to seven. He blinks his eyes and moves his mouth as he reads stories, watches a video, or uses the computer with your child. Teddy Ruxpin sells for approximately $49.99 at local retailers. For more information, contact Yes! Entertainment, 3875 Hopyard Rd., Suite 375, Pleasanton, CA 94588; (800) 222-9376; *www.yesent.com*.

**9. Mindforge Fractions.** This CD-ROM introduces children ages four to nine to fraction concepts. Using pictures, animation, demonstration, text, narration, and music, it brings fractions to life. It includes practice with characters called Instructrons. Priced at about $32.95, it comes from from Mindforge Inc., 441 S. Spring St., Burlington, NC 27216; (888) 633-6743; *www.mindforge.com*.

**10. National Geographic Really Wild Animals.** This interactive electronic toy is aimed at children ages six to eight. Using packs of talking animal and country cards, the children learn geography and animal facts. As the child takes their own safari to the seven continents and the major oceans of the world, the animals and habitats come to life in sound. National Geographic Really Wild Animals is available for approximately $69.95 at local retailers. Contact Leapfrog Toys, 1250 45th St., Suite 150, Emeryville, CA 94608; (510) 595-2470; *www.leapfrogtoys.com*.

*Marifrances D. Williams holds a degree in Liberal Studies from San Diego State University, Calif. She is currently a fifth-grade teacher at Los Ranchos Elementary, San Luis Obispo, Calif. Williams specializes in the identification of advanced technology for the use of child-focused applications. She may be reached at williamsofsm@lightspeed.net.*

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| VR5432™ | | | |
|---|---|---|---|
| CPU Speed | 167 MHz | Dhrystone MIPS | 347 |
| System Interface | 32 Bit | On-Chip Debugging | Yes |
| Bus Speed | 67 MHz | Power Consumption | 2.5W Peak |
| I Cache Size | 32 KB | Multimedia Extensions | Yes |
| D Cache Size | 32 KB | Floating Point Unit | IEEE-754 |
| Pin Count/Package | 208 PQFP | Chip Set Support | Yes |



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NEC

# The Sony Challenge: Will Peers Give To Schools In Need?

Sony Electronics, Park Ridge, N.J., is challenging other electronic companies to raise nearly $1 million for a cause. The company wants to build awareness for one of the industry's most important strategic issues: developing and training workers for high-tech careers. Focused on grades kindergarten through 12, the goal is to change the way students learn.

Through its membership in the Consumer Electronic Manufacturing Association (CEMA), Sony is contributing the seed money to begin the Math and Science Education Program for Underserved Schools. The contribution will stand with the Electronics Industry Foundation (EIF), Arlington, Va.—the philanthropic arm of the 2100-member Electronics Industry Alliance (EIA). Designed to provide teachers and students with resources, the initiative also can assist them in building programs that raise awareness of math, science, electronics, and high-tech careers. In addition, it should function to change teaching methods, making learning more interactive.

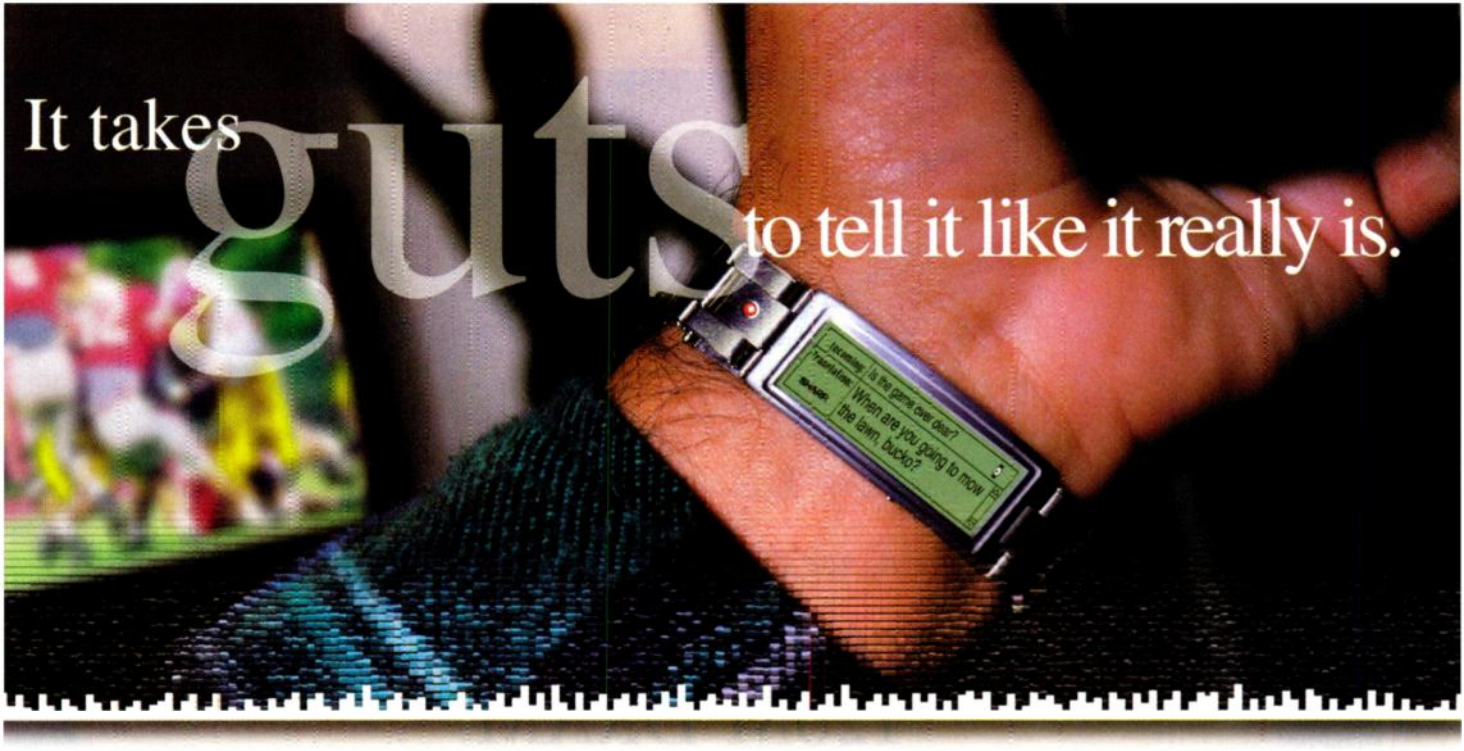
"Underserved, unfortunately, has now become a synonym for forgotten," says John MacDonald, chairman of the EIF. "Sony Electronics and EIF are dedicated to changing that. We hope to tap into the incredible resources existing in schools that have either been neglected or ignored. Innovation and creativity cannot and should not be limited by geography or lack of funds. Our goal is to uncover these overlooked areas, invest in them, and channel the resulting energies into building the digital and electronics frontier. Sony's grant takes the first step in that direction."

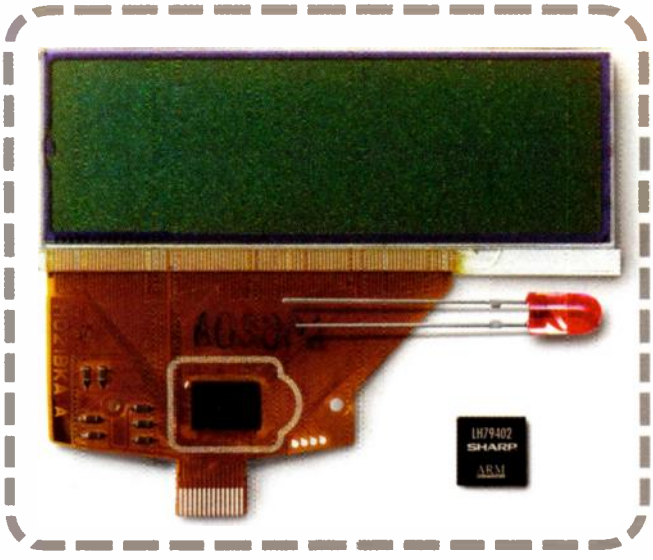
The company also believes that this investment will pay off for the electronics industry. "Education and training is a critical, strategic, and competitive issue to Sony Electronics and the electronics industry," states Jason Farrow, senior vice president of public affairs for Sony. "Although we have been dedicating significant resources to bolster our capabilities, Sony believes it is time to step up our efforts in this area. Working with EIF provides us more leverage to make a meaningful impact on the workforce of the future."

EIF's K-12 Math and Science Education Program for Underserved Schools was formally unveiled at EIA's Annual Fall Conference in Scottsdale, Ariz. Planned activities under the initiative are expected to include enrichment grants to local schools, developing best-practice templates that can be easily duplicated, and creating partnerships between electronics companies and schools.

For more information, contact Michael Cabot of Sony Electronics at (201) 930-6646, or via e-mail at michael_cabot@mail.sel.sony.com.

**Roger Allan**

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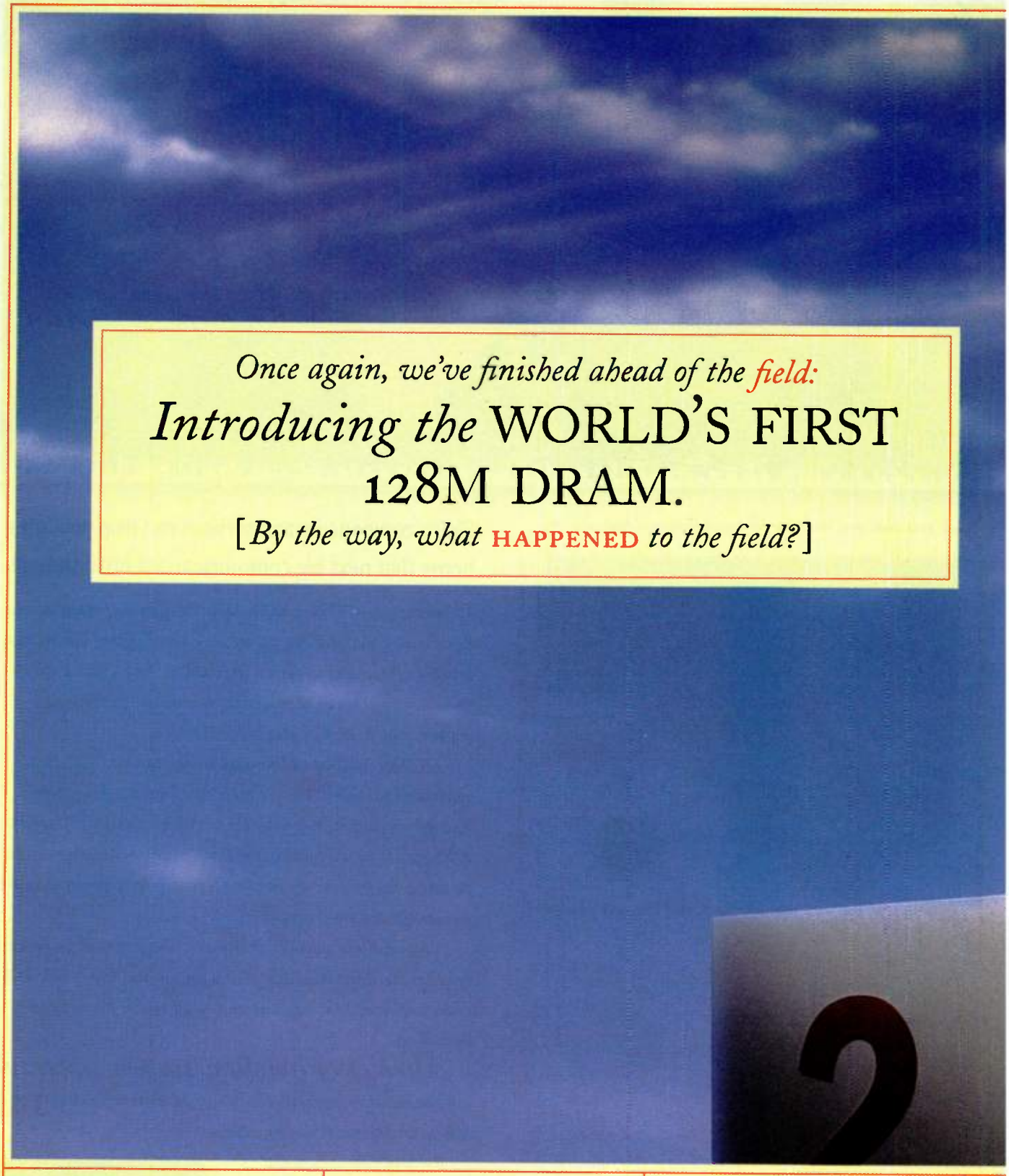

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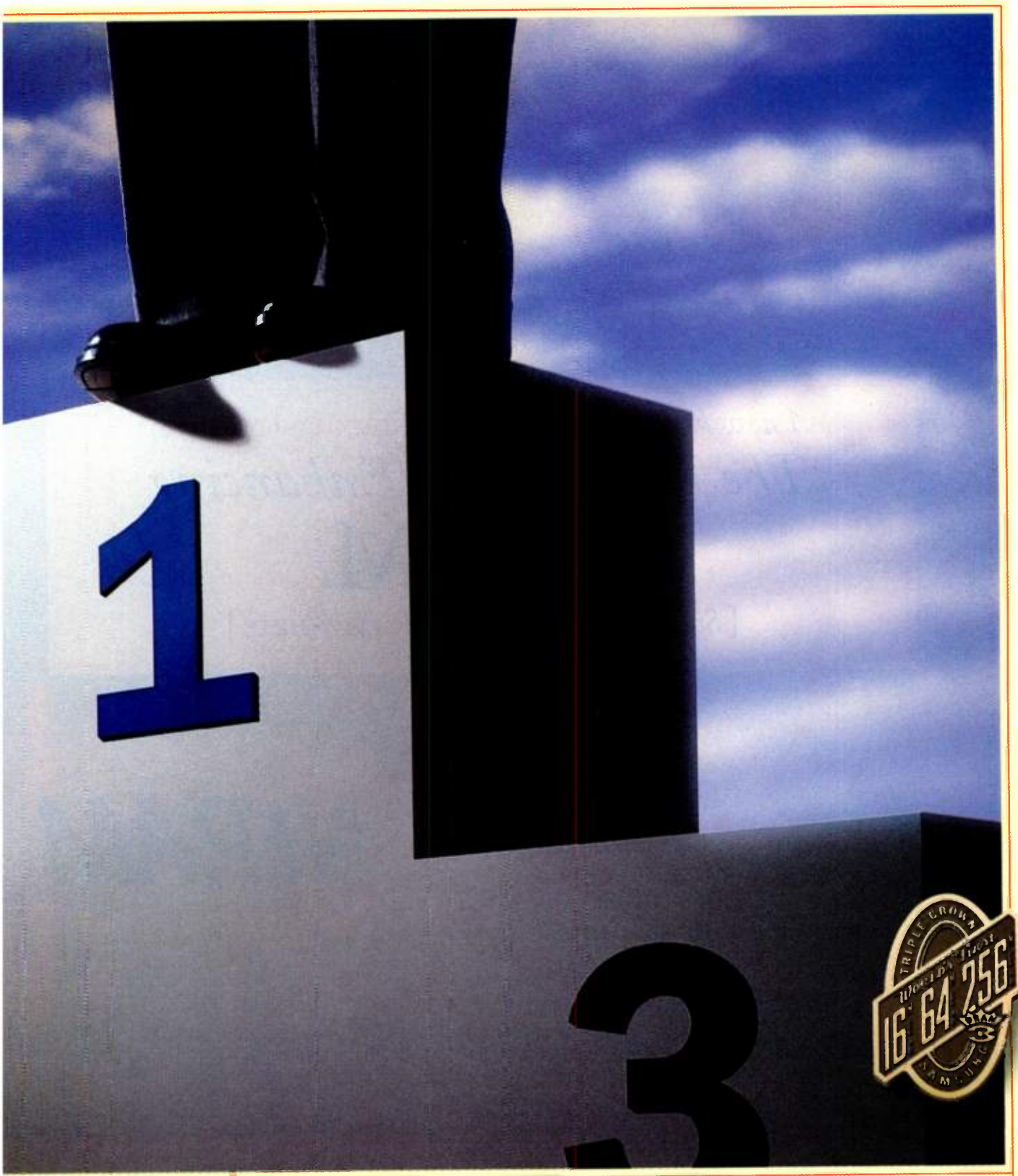


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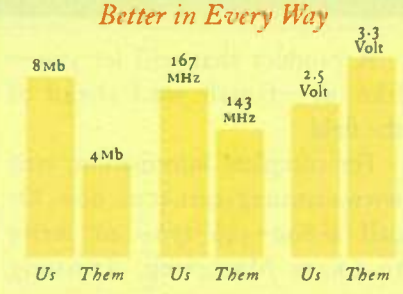


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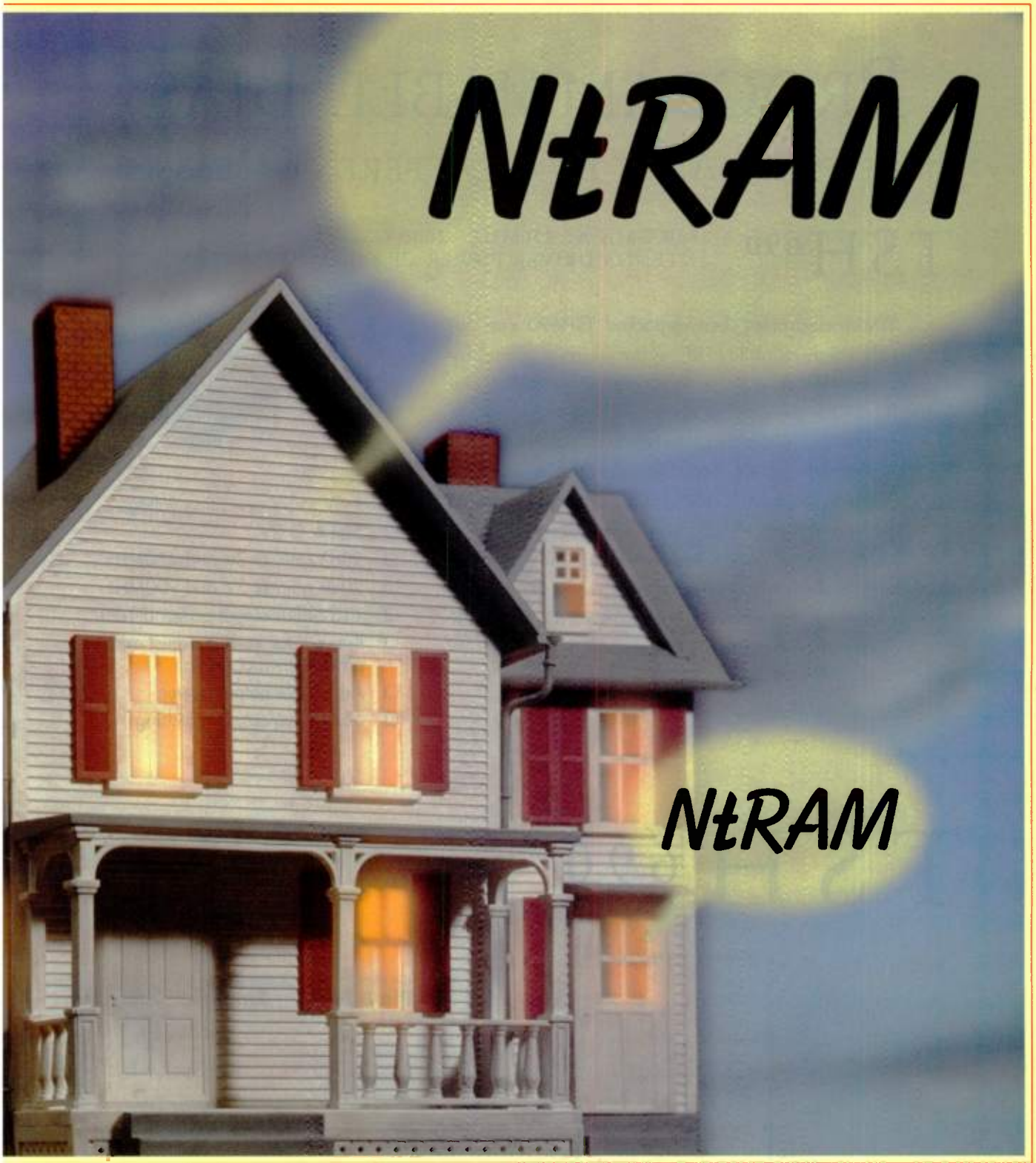


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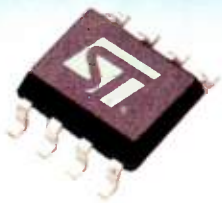

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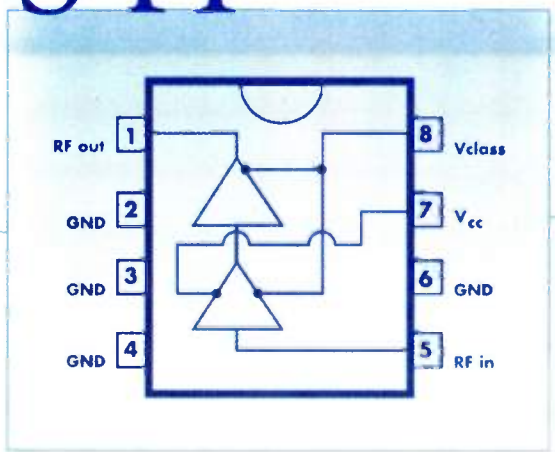


| Pin 8 Bias | Amplifier Operation |
|---|---|
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| $V_{cc}$> >Gnd | Class A-B |
| Gnd | Power-Down |



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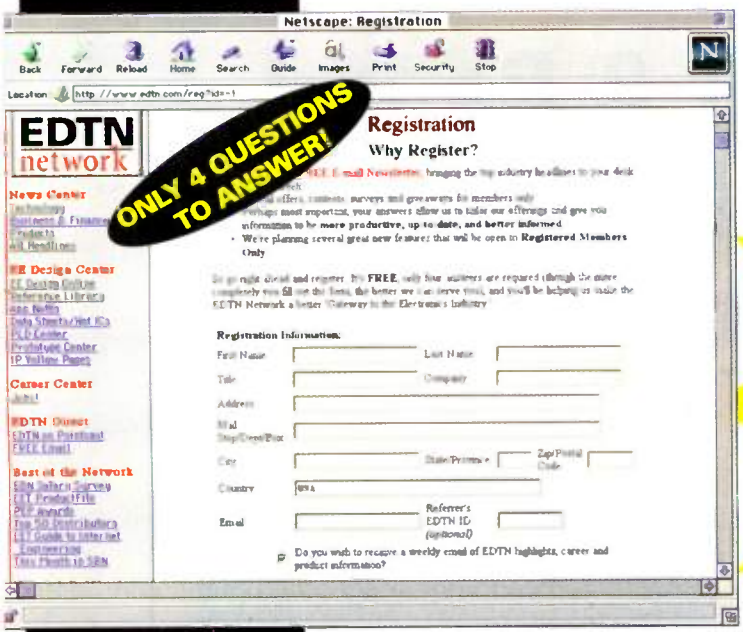


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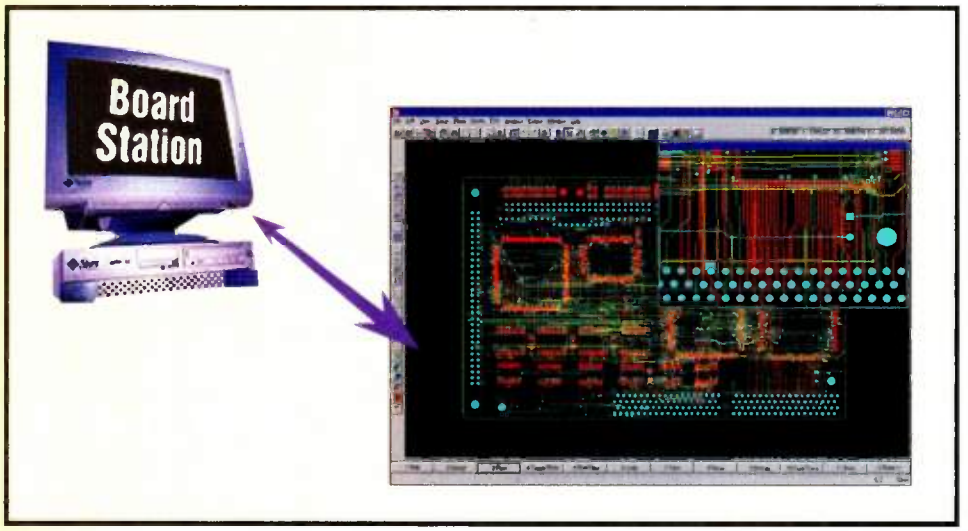


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# Formal Verification Helps Stamp Out Design Bugs

*Formal Techniques Offer New Hope For Solving The Verification Problem And Helping You Design The Right Thing From The Start.*

Cheryl Ajluni

COVER FEATURE

Formal verification is reemerging with a vengeance. This isn't a new technology, having been around for many years. But, I bet if I asked you to tell me what it means, you'd be hard pressed to find an answer. That's partly because formal verification is an umbrella covering a wide range of techniques. It can be very intimidating. Very mathematically intensive, formal verification often requires that the designer understand the design process and the design itself in an entirely new way. For many, this is a scary—if not uncomfortable—proposition.

But, regardless of your understanding or lack of understanding, and any long-held misconceptions you may have on this technology, you'll undoubtedly come face to face with it soon *(see "Debunking The Formal-Verification Myths," p. 68)*. That's because its core mission is to help you find more bugs faster than you ever thought possible. So, for better or worse, it's time to face your fear and enter the mysterious world of formal verification. Hang onto your hats. It's going to be a bumpy ride.

## Back To Basics

First things first. When people talk about formal verification today, they typically either mean model checking or equivalence checking. While these are certainly not the only categories under the formal-verification umbrella, they are the most well known. Both have been introduced to the market in the form of commercial tools. Of the two, equivalence checking is the most mature and closest to gaining mainstream acceptance. Model checking is still in the "kick-the-tires" stage. It's not expected to fully mature and take its place in the mainstream for at least two to three years.

Formal verification is an algorithmic-based approach to logic verification. In general terms, it refers to any tool that mathematically and exhaustively proves something about a design. The key word here is "prove." This is much different from simulation, which gives you the answer, "I think it works." Formal verification uses no test vectors. And unlike simulation, which is a point tool, it can be used for verification from the beginning of the design process to help avoid bugs. Johan Sandstrom, founder of Sandstrom Engineering, explains it this way: "The promise of formal verification is that all the various representations of the original functional design (RTL code), through all the downstream ASIC activities, can be compared back to the original without functional or structural vectors." Other benefits of the technology include 100% coverage and the ability to verify much quicker than with simulation alone.

Many reasons have contributed to the recent renewed interest in, and usage of, formal verification. Up until about three years ago, most people still relied on simulation as the only means of verification. Today, formal verification is quickly becoming a cornerstone of verification for complex circuits.

One reason behind this movement is simply that the technology, particularly equivalence checking, has matured to the point where it could be made into a commercial product. From an industry perspective, the growing complexity of

designs, the migration to systems-on-a-chip (SoC), and the use of IP all have contributed to a simulation bottleneck. With simulation the only means of verification, a lot of time and money gets invested in creating test benches for simulation and actually performing regression testing. Simulation alone has proven ineffective against such complex designs. Inherently, it's not exhaustive and can miss bugs.

As Dino Caporossi of Cadence Design Systems explains, "Multimillion gate designs take far too long to simulate at the gate-level, and equivalence checking offers complete coverage with significant time savings. Increased design complexity also makes it easier for costly bugs to slip through the design and specification process—thus the increased interest in model checking." By employing formal verification as a complement to simulation, you have a strong defense against those pesky bugs that threaten to ruin your company's time-to-market edge and ultimately destroy your design.

## Equivalence Checking

The formal-verification market is overwhelmingly dominated by equivalence checking, primarily because using the technology is such a "no-brainer." It boils down to one thing: If you use gate-level simulation, stop and replace it with equivalence checking. But, equivalence checking isn't just a substitute for functional gate-level simulation. Used to determine if one design is functionally identical to another, it addresses the issue, "Have I corrupted my design with changes?", by exhaustively proving that the design is correct against what is known to be correct.

It can verify that functional bugs are not introduced during the various stages of implementation—from high-level RTL to the final post place-and-route netlist. And, it can be used to compare two designs, such as for FPGA to ASIC conversion (gate to gate), design reuse (gate to RTL), language migration (VHDL to Verilog), and design refinement (RTL to RTL).

Of all the formal-verification techniques, equivalence checking is the most mainstream. It answers the easiest problem: Are two things functionally equivalent? And, it fits into existing design methodologies. This is an important point, because many are confused about how these tools will work in existing flows. Let me spell it out for you. Equivalence-checking tools will NOT change the way you de-

# Debunking The Formal-Verification Myths

One reason that engineers have such a hard time getting comfortable with the topic of formal verification is that a number of myths exist out there about this technology. These myths, having never been rebuked, prevent more people from using formal-verification tools. Here are some of the more common myths encountered:

1. *Formal verification is immature.* False. Large corporations have been signing off for many years using static methods. And, today's tools are handling multimillion-gate designs successfully.

2. *Formal-verification tools require a restricted design style.* False. Most tools support the full synthesis subset.

3. *Equivalence checkers are slower than simulation.* False. Some early tools were slow. But newer, more advanced algorithms can verify multimillion-gate designs in a matter of minutes or hours instead of the days or weeks required for gate simulation.

4. *Equivalence checkers require lots of user guidance.* False. Tools which use automatic functional matching instead of structural matching report no false differences and require no user guidance.

5. *Equivalence checkers are only good for gate-to-gate comparisons.* False. Tools which can automatically handle structurally dissimilar designs are good at handling RTL.

6. *Equivalence checkers that use binary decision diagrams (BDDs) are slow.* False. Early tools that used only BDDs could be slow. Modern tools, which combine BDD methods with other algorithms, are very fast and powerful.

7. *Sign-off always occurs at gate level.* False. Late functional changes may occur during place and route, such as placement-based optimization, scan reordering, or clock-tree insertion. Thus, it's important to check the design at the DEF physical netlist level to ensure that these changes are verified.

8. *Equivalence checkers can't handle multipliers.* Partially true. Proving a behavioral description against a particular gate-level architecture can still be a difficult task, depending on the width. If the two designs being compared have similar architectures, the proof can be easy for any width.

9. *Equivalence checkers are hard to use.* False. Gaining debugging expertise still requires some training and hands-on experience, but running the tools is fairly straightforward. Integration with familiar tools, such as simulation and schematics, has shortened the learning curve even further.

10. *Some equivalence checkers are sign-off certified.* False. Functional analysis is only one part of sign-off; timing analysis also is required. Complicating matters, sign-off simulation may give conflicting results, since many equivalence checkers do not share a common database with simulation. Finally, there's still a need to validate the original RTL specification by using cycle/event-based simulation and/or model checking.

11. *Model checkers are hard to use.* Partially true. Learning a new methodology always requires the development of new skills, but modern model checkers have graphical user interfaces which greatly accelerate this learning process. Counter-example debugging is simple, since the output is a familiar simulation vector.

*Contributed by Dino Caporossi, product marketing manager, Affirma Equivalence Checker, Cadence Design Systems. For more information on formal verification, check out the Cadence web site at www.cadence.com.*

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sign today. As Craig Cochrane, group marketing manager for formal verification at Synopsys, puts it, "It's like using the same word-processing tool, but with a different spell checker."

This doesn't imply that everyone should use these types of tools. On the contrary, whether you use these tools really depends on the size of the design that you're working on and how long your design window is. Generally, a good rule of thumb is that if you're working with about 200k gates, it's time to use equivalence checking. If you're working below this point, say at 50k to 100k gates designing one chip a year on average, it's not really going to be worth your while to adopt an equivalence-checking tool.

A number of commercial equivalence-checking tools are now available, typically performing roughly 1 million gates in three hours *(see "Formal-Verification Tools Now Available," below)*. Improvements to the technology continue at a furious pace. Much of the work deals with things like improving tool usability, providing better RTL support, and automating for the users what they now do manually. Efforts also are being made to integrate equivalence checking with other verification techniques as part of a complete verification flow.

Other areas, such as performance and capacity, are being addressed as well. Silicon complexity doesn't stop at a specific gate count, and most commercial tools today can only handle around two-million-gate devices. Next-generation tools will have to be capable of handling upwards of 4 million gates.

## Model Checking

The formal-verification technique known as model checking addresses a much harder, but perhaps inherently more important, problem than equivalence checking. It tackles the quality-of-source issue by asking, "Have I designed what I wanted to design?" Like equivalence checking, it's not a simulation test-vector-like methodology. Rather, it requires the user to create a specification by entering properties about the design. Today, this is typically done simply by writing down on a piece of paper, in English for example, what function the design will have.

Once you've specified the design's abstraction, model checking is able to prove properties about the design. Especially useful for debugging a design early in the design cycle, this method rigorously verifies that a design behaves correctly under a given set of specifications for all possible input stimuli. This means that, for example, a specification can be created to verify

# Formal-Verification Tools Now Available

A number of companies now have equivalence-checking tools available for purchase. While each tool has its own unique look and feel, they all share the same general approach to solving the equivalency problem. Most of the tools load the designs directly, although Chrysalis Symbolic Design first compiles the design into what it refers to as "symbolic logic." The designs are then broken down into logic cones, and algorithms—either one at a time or cooperatively—are automatically applied to each individual cone to try and prove or disprove equivalency. In many cases, the choice of algorithms is based on a complex set of heuristics. Some of the algorithms the companies employ are very well-known solvers, such as the binary decision diagram (BDD), while others are homegrown and proprietary in nature.

What makes each company's tool unique is its pool of algorithms and how they're applied. On the current market, equivalence-checking tools can be differentiated by two features: how easy the tool is to use and whether it can be easily integrated into the user's design flow.

If you haven't already purchased an equivalence-checking tool, here are some hints. Do your research beforehand to familiarize yourself with the formal-verification tools and vendors. As you do, keep your eye out for the following things: speed, capacity, accuracy, usability, and compatibility with other tools.

Speed plays an important role in the tool's usability, since it must be able to run significantly faster than gate-level simulation in order to justify the methodology shift and learning curve you will undoubtedly experience. With gate counts rapidly rising, you want to ensure that whatever tool you purchase will be able to accommodate this increase. Accuracy is important as well. It will determine how easily the tool is prone to false positives ( saying two designs are equivalent when they are not) and false negatives (saying two design are not equivalent when they actually are). If the tool is prone to false negatives and positives, it may require you to physically go in and guide it through. Or, it may be unable to complete the proof at all.

Here is a brief line-up of the tools now available:

StructureProver II from *Verysys Design Automation*

This equivalence-checking tool features an intuitive, flow-based graphical user interface (GUI), built-in diagnostics, and algorithmic improvements capable of handling multimillion-gate designs. The cockpit of the verification environment—its GUI—integrates the entire verification process, including debugging steps. The tool cost is roughly $75,000. The company is currently working on a next-generation equivalence-checking tool, which will feature newer algorithms that complement formal verification.

Formality from *Synopsys*

This tool is capable of verifying million-gate, system-on-a-chip (SoC) designs. It contains multiple algorithms (solvers) for proving equivalence, as opposed to relying on a single solver to perform this function. Automatic hierarchy management allows the user to verify designs where the hierarchy does not match. Fast and easy debugging is possible through the tool's powerful diagnostic analysis and schematic debugging feature. Formality, integrated within the company's synthesis-based design flow, is well suited for design projects where a high percentage of the logic is synthesized with Design Compile—each IC is larger than 100,000 gates (or equivalent), and gate-level simulation is expected to run for several days.

Design VERIFYer from *Chrysalis Symbolic Design*

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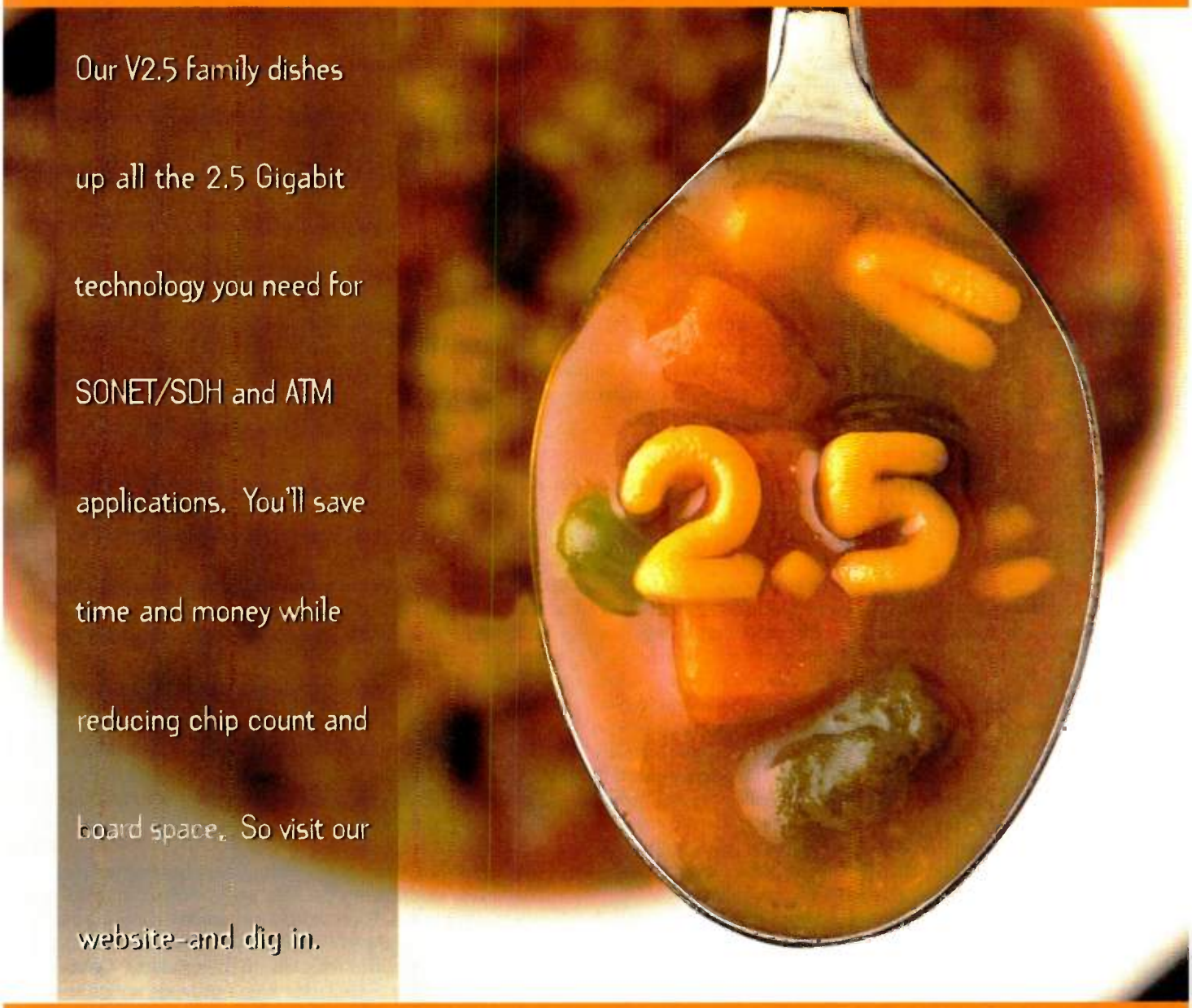


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Isadore Katz, Chrysalis Symbolic Design, explains it this way: "Model checking is an attempt to selectively replace or complement simulation with formal proofs, at a number of different levels, and in cases where simulation is inefficient or the test bench is ineffective in finding answers."

Model checking has gathered interest because it's now moving from the laboratory to commercialization. But, it's still in the early adopter stage. This technology is expected to play a major role in IP-block authoring and integration by helping the designer check the interfaces between the blocks.

Companies such as Cadence Design Systems, Chrysalis Symbolic Design, Verysys Design Automation, and Sandstrom Engineering all have versions of a model-checking tool now on the market. Cadence's tool, known as Affirma FormalCheck, was formerly known as the FormalCheck tool developed by Bell Labs Design Automation Group (BLDA) from Lucent Technologies. Murray Hill, N.J. Chrysalis' offering is Design INSIGHT, a family of modular model-checking products that include such modules as State Machine Analyzer and Design INSIGHT Assertions.

Verysys' model-checking tool, PropertyProver, is no longer being sold. In its place, the company plans to release a new tool that combines the best of its PropertyProver and DesignProver Equivalence Checker, which handles sequential equivalence for both synchronous and asynchronous designs.

Sandstrom Engineering offers a verification tool that addresses one aspect of the model-checking problem. Called PreSynth.vhd, the tool supplements simulation by analyzing your RTL. It checks for nonsense constructs, the dreaded "reset problem," non-synthesizable constructs, and performs hundreds of lint-type checks. It also permits you to use an expanded subset of VHDL, which PreSynth.vhd converts to synthesizable VHDL.

## Easier To Use

But before these tools become viable in a more mainstream market, a number of things must happen. For starters, the tools must be easier to use and provide more meaningful results. Assuming these two things can be accomplished, the next step—the issue of capacity—is even more daunting.

The Design VERIFYer formal equivalence-checking software is based on an architecture that incorporates a unique symbolic logic representation with a powerful logic-manipulation engine. Signal-mapping and logic-comparison algorithms are added to the mix to provide independent proof that gate (or switch) implementations are functionally equivalent to the corresponding RTL specification, and that gate-level design revisions do not inadvertently change a design's logical functionality. This tool is fully independent of the logic-synthesis process and shares its language-neutral compiler with other Chrysalis tools. Once compiled into the symbolic logic representation, designs can be formally compared using Design VERIFYer and debugged using Design EXPLORE. Design EXPLORE lets you interact directly with the logic of your designs, so you get conclusive answers to functional questions when debugging unexpected results or analyzing complex digital logic.

Affirma Check from *Cadence Design Systems*

The Affirma Check tool is able to perform multiple whole-chip RTL through gate functional-verification runs per day on entire multimillion-gate designs. It proves RTL against physical netlist (DEF) with the company's timing-driven place-and-route flows. Integrated as part of the company's Interleaved Native Compiled Architecture (INCA) mixed-language, mixed-cycle/event architecture, it maintains compatibility with existing simulation methodologies. Specific features of the Affirma Check equivalence-checking tool include functional mapping to compare logic gates to logic RTL and multiple algorithms that operate in a cooperative fashion. It uses existing Verilog gate-level sign-off libraries, supports industry-standard language compilers, and features debug capabilities with simulation, RTL source, and gate-level schematic user interfaces.

Tuxedo-LEC from *Verplex Systems*

Tuxedo-LEC can perform equivalence checks on large SoC designs ranging from half a million to several million gates. Based on correlation-learning technology, it explores the structural and functional relationships between golden and revised designs. A comparison engine uses multiple techniques to compare the equivalence of two designs. An automatic key-point mapping feature allows the tool to identify key points quickly and automatically in a push-button environment. Tuxedo-LEC can be used with the company's Tuxedo-LDD logic debugging and analysis tool for automatic diagnosis and analysis of the differences in the two designs. The tool features built-in capabilities for the designer to specify constraints. To explore these differences, the tool automatically generates online schematics for graphical debugging and provides links between the RTL source and the gate-level design.

Lynx from *Avant! Corp.*

The Lynx family provides an automatic and exhaustive validation of a design's functionality and specifications at all levels of abstraction. It provides functionality checking at the RTL level, exhaustively verifying that the RTL designs meet functional specifications. One of the products, Lynx-VHDL, verifies functionality through synthesis, optimization, test-logic insertion, or other transformations by equivalence checking between different descriptions of a design. In particular, it checks that two different descriptions of a design are equivalent (RTL to RTL, RTL to gates, and gates to gates), finds common RTL coding errors, directly pinpoints error locations, doesn't require test benches or vector sets, and supports all synthesizable constructs at any level of abstraction.

*Mentor Graphics Corp.*

While the company has yet to introduce a tool in this space, it's making significant investments in the formal-verification area. A great deal of its efforts are targeted at creating a product.


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As design complexity continues to increase, all EDA tools are at some point faced with the question, "How do you handle a bigger design?" For model-checking tools, this isn't an easy question. This is because there's no easy answer. A fundamental breakthrough in technology must occur for model checking to be able to address the capacity issue of multimillion-gate designs. This development may still be a few years away.

In the meantime, there will soon be hope for those who want to take advantage of the model-checking technology in its present form. The answer, according to some, is to create automatic blocks of the tool or prepackaged checks. These could be used out of the box by identifying today's applications in which model checking, with its current limitations, can still be of use. Chrysalis' Isadore Katz acknowledges this move, saying, "Chrysalis anticipates the need for prepackaged checks, as well as general-purpose model checking."

Prepackaged checks are expected to have the greatest benefit for the basic ASIC designer who would like to reap the benefits of model-checking assertions, but isn't an expert on the technology. Because the technology would be presented in a modular form addressed at specific application problems, designers would presumably not need to be experts. These solutions would require zero engineering time and cost much less than a general-purpose model-checking tool.

As designers begin to understand the benefits of the technology and get accustomed to its problem-solving approach, a market for model-checking tools may slowly be carved out. Then, questions about what the target market for such a technology is may finally get answered. But again, the key to making this technology mainstream will be in figuring out a practical way to introduce it to the market. Prepackaged checks may be a comfortable migration path for some, at least until the more general-purpose model-checking tools can successfully address the issues of ease of use, meaningfulness of results, and capacity.

## Theorem Proving

A discussion on formal verification would not be complete without mentioning theorem provers. Theorem proving is an extremely rich technology. Compared to other formal-verification applications, it sits at the top of the food chain. In other words, equivalence checking is a subset of model checking, which in turn is itself a subset of theorem proving. Theorem proving is much more mathematical in nature than equivalence checking or model checking, and in fact solves a much different problem.

Today, a design is often defined as a machine that will do something in response to a stimulus. With theorem proving, you would take this same machine and turn it into a mathematical proposition. By defining it at such a high level, you could literally convert the entire design to a formal approach from top to bottom. For example, it provides a way to create a mathematical specification of how a multiplier works and then be able to prove it. This will play an important role in future design processes, since it allows you to reason arithmetically in a way that is simply not possible with other areas of formal verification. This could be extremely useful in applications like DSPs.

While Chrysalis' Isadore Katz points out that today, theorem proving is used at a very high level to model power grids and high-level traffic controls, it's still important to note that this technology is nowhere near ready for commercialization. Even if it were, there is not yet a market waiting to welcome it. This will require a dramatic paradigm shift in the industry, prompted by some sort of radical event that makes accepted design practices painful. Ultimately, this will occur and the market for the tools will develop. But, many believe that this may still be five years or so away.

So, while you may hear the term "theorem proving" thrown about in the industry, it's certainly nothing you should concern yourself with—at least for the time being.

## Hybrid Alternatives

The viability of formal techniques in a wide range of applications has recently spurred a great deal of attention onto what has come to be known as semiformal techniques, or hybrid formal-verification solutions. These hybrids use formal techniques to augment simulation, static-timing analysis, and even the test bench. Some examples include formal verification/simulation and equivalence checking/static-timing analysis (STA) hybrids.

A formal verification/simulation

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Regardless of what verification tool you're evoking, you'll still have a consistent view of the design.

Cadence Design Systems and Synopsys, along with other EDA tool vendors, are now working toward this goal. In particular, Cadence Design Systems is looking into what it calls "smart verification"—the combination of formal methods, simulation, and code coverage to find the maximum amount of bugs in the least amount of time. One component that might be useful for this or any other unified verification approach is the development of an equivalent to code coverage for model checking.

Today, a design is typically divided into hierarchical blocks. Some blocks are handled with simulation, and some with formal verification. Problems occur when the blocks don't match up and you end up using both technologies on the same block. This duplication of work is simply a sheer waste of time. Model-checking code-coverage tools would provide the user with some measure of ability to pinpoint what questions weren't asked yet, what bugs were and were not missed by the test bench, and ultimately, if one tool took care of the problem.

## Into The Mainstream

The instigation for a unified verification methodology will come when formal-verification tools are accepted into the mainstream. Equivalence checking has just about reached this point, and model checking is expected to follow in the next few years. But, this will require both the user and the tools to give a bit. Users, for example, will need to better understand the internal workings of their designs. They'll have to put aside their simulation-centric view of verification and open up to using formal-verification tools in a way that's entirely different from how they utilize simulators. And, design and verification engineers who are used to a serial mode of operation will need to come together to work on a parallel approach to design and verification.

Formal-verification tools will need to become easier to use and learn. After all, if you have five different types of tools, you'll never become a verification expert. But if you only have one tool to learn, you can become an expert or at the very least learn the verification process really well. Having a unified view of verification, where all the different verification-point tools are interfaced, will help eliminate this problem. All the tools will then have similar outputs. Consequently, if you know how to use a simulator, you would presumably be able to use all the other component-verification tools.

A couple of options exist to make this unified view of verification happen. Large EDA tool vendors could buy all the component-verification technologies or develop them in-house and put them together in one flow. Or, EDA tool vendors could agree to link their verification tools together in a design flow that's governed by some sort of standard language, GUI, and interface protocol. Of course, remember that these options rely on EDA tool vendors working *together*. What are the chances of getting that to happen?

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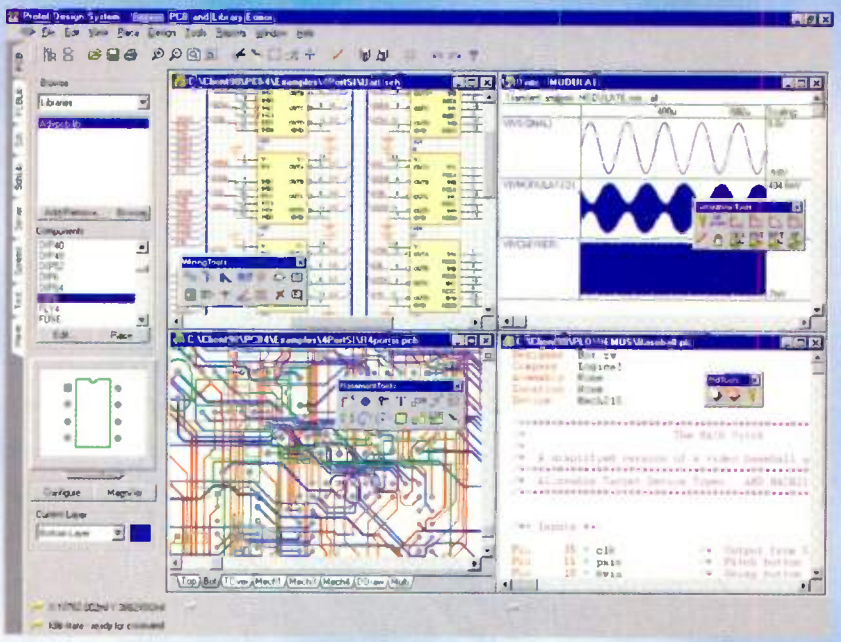

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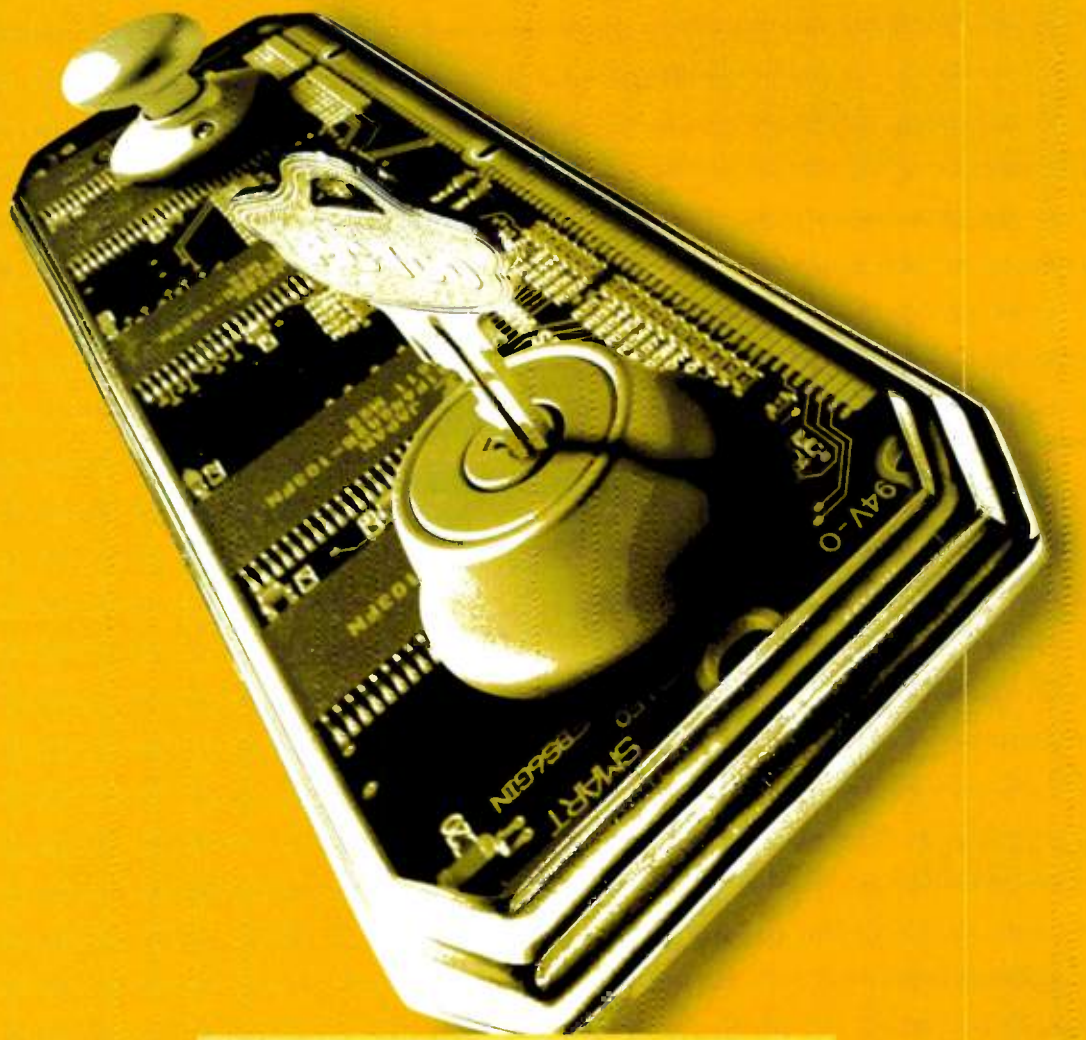


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# Clever DSP Board Architectures Attack Data Bottlenecks

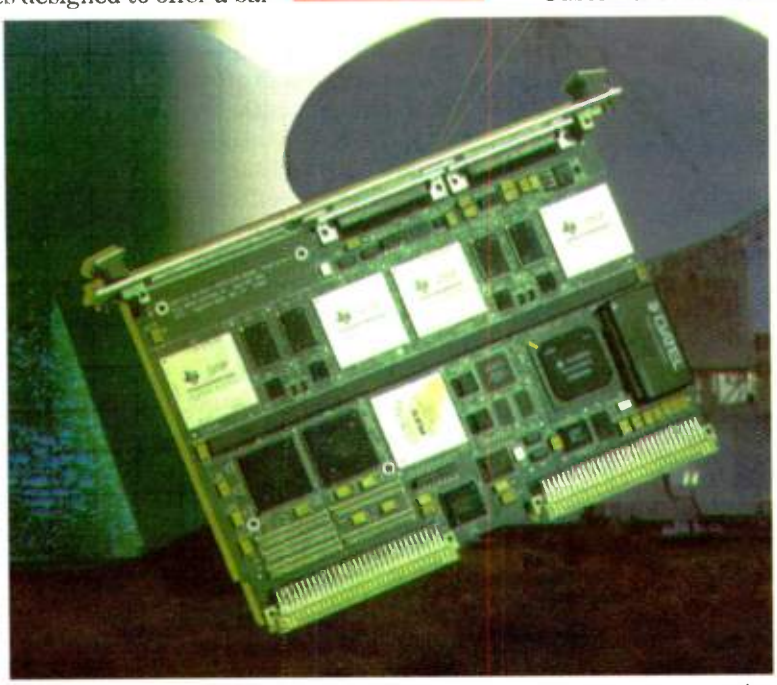
*As Board Vendors Craft Ways To Feed Speedier DSPs, Crossbar Switches, FIFOs, And Secondary Links Offer Solutions.*

**Jeff Child**

SPECIAL REPORT

Applications ranging from sonar/radar and medical imaging to high-end telecommunications depend on board-level, digital-signal processor (DSP) systems. As DSP chips race to faster and faster speeds, the I/O is becoming a bottleneck. Cutting-edge processing muscle is wasted if you can't move the data around the board and over buses at comparable rates. The solution is board-level architectures designed to offer a balanced I/O throughput.

Achieving the right balance of processing power (both in MFLOPS and in MIPS) and throughput (in Mbytes/s) is no easy task. For designers of DSP boards, leading-edge DSP chips emerging on the market are both the solution and the problem. They offer plenty of performance. The two leading DSP chip vendors, Analog Devices Inc. (ADI) and Texas Instruments (TI), continue to move forward on the performance curve, with GFLOPS chips ready to emerge early next year. Meanwhile, Motorola Semiconductor offers a third alternative in certain members of its PowerPC line of processors. The more advanced PowerPC chips offer floating-point capabilities that thrust them into the DSP realm of choices.



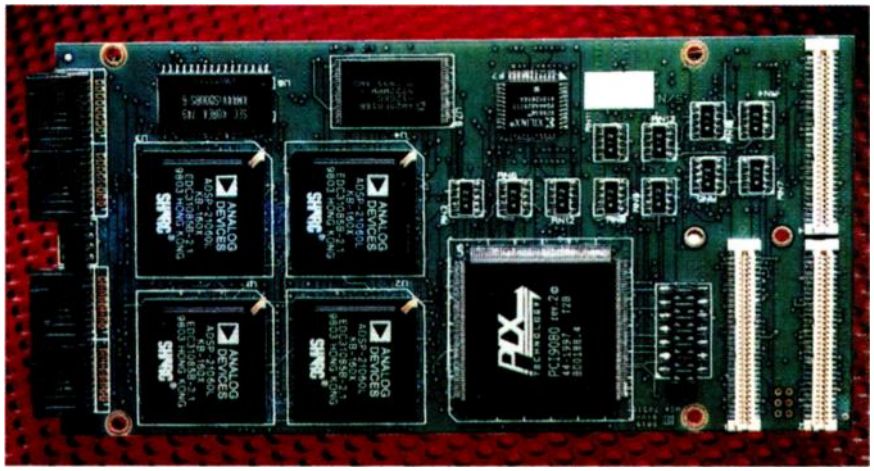
Art Courtesy: BlueWave Systems

Unfortunately, these chip architectures stem from DSP families that are targeted for few-chip and single-chip embedded applications. As such, the DSP vendors offer little to ease the task of cramming several DSP chips on board for high-end, board-level multiprocessing. ADI's SHARC DSP at least offers Link-ports that help the designer implement I/O transfers. DSP board designers are otherwise left to how to handle the problem themselves.

"Customers that want to talk about buying a board these days have usually already done their MFLOPS calculation and know that they can do their application on the processor," explains Keith Burgess, chief technology officer at Blue Wave Systems Inc. "They can calculate that on a simulator sometimes long before the chip even exists. But, what they're concerned about is how their data moves around their systems. That's the limiting factor—more than the DSP's processing ability."

## Different Strokes

TI's TMS320C6x DSP architecture is attracting a slew of DSP board design wins. For its part, Blue Wave Systems is taking an application focus for its latest board products. Defense, intelligence and surveillance, wireless communications, and wireline telecommunications are some of the largest and most promising emerging markets for DSP-based systems.



**The IXZMPC4 Quad SHARC PCI Mezzanine Card (PMC) from Ixthos can work as a high-powered, on-board compute engine or as a high-performance bridge to external SHARC processors needing to link to the PCI bus.**

Blue Wave Systems is attacking those markets with a new family of VME DSP boards.

The family consists of three separate products, the VME/C6450 *(see the opening photo)*, the VME/C6420, and the VME/C6400. Each product has been carefully tuned to meet the unique requirements of a specific vertical application. The VME/C6450 is targeted toward the high-performance multiprocessing applications typical in defense and high-end image processing. The VME/C6420 offers scalability and high-bandwidth data throughput, which are essential in wireless communications and surveillance applications. The cost-effective VME/C6400 completes the family. It's ideal for channelized wireline-communications applications requiring standard telecom interfaces.

The VME/C6450 provides up to 4 GFLOPS and 6400 MIPS from four TMS320C6000 DSPs. A crossbar sits at the heart of the board and acts as a high-speed switch, providing a fully interconnected solution.

The VME/C6420 is fully compatible with the SoftBand Software Radio product line. Its architecture has the same type of crossbar interconnection, but is optimized for digital radio systems.

The VME/C6400 is a quad processor board with a channelized architecture. It's designed for wireline telecommunication applications such as transcoding, echo cancellation, voice-over IP, and speech recognition.

VME isn't the only bus architecture being considered for high-end DSPs. CompactPCI boards sporting C6x DSPs have begun to emerge. The latest example is Spectrum's Baja board. Optimized for telecommunications applications and powered by eight 'C6202 processors, it provides a total of 16,000 MIPS of processing power in a single slot. Other features include a Motorola MPC860 PowerQUICC processor, an ECTF H.110 bus, hot-swap capability, and driver support for high-availability systems.

According to Spectrum, sharing data across multiple DSPs is the key to implementing efficient multichannel algorithms for telecom applications such as wireless base-transceiver stations, voice-over IP (VOIP) gateways, and remote-access servers (RASs). Baja's architecture is based on a new, Spectrum-developed ASIC which enables high-speed interprocessor communication between the 'C6202 processors.

## SHARCs Bite Back

When high-performance, real-time processing is required, the more DSPs on board the merrier. ADI's SHARC DSP chip offers Link-ports that make it easier to pack more chips on a board. Providing up to 24 SHARC DSPs in a motherboard and daughterboard format, the Vantegra board from Radstone Technology Inc. is capable of yielding up to 2.88 GFLOPS of performance in a single 6U VME slot. It's compliant with either IEEE 1101.2 Conduction Cooled or Air Cooled formats.

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The board design exploits the full potential of ADI's SHARC DSP by using clusters of six ADSP-2106x devices, each with local SRAM and flash memory, as the system's basic building block. This architecture eases and accelerates software development by providing symmetrical compute segments. This in turn ensures that resource allocation is simple and easily scaled over multiple clusters and board sets.

Each cluster of six SHARCs provides six Link-ports to give up to 240-Mbyte/s data transfers between the adjacent cluster of SHARCs on the same board. Each cluster on the board then provides a further six Link-ports for the motherboard/daughterboard interconnection.

Similarly, there are up to 24 Link-ports (six per cluster) available at the front, providing interconnection for multiple boards and giving an aggregate peak transfer rate of up to 480 Mbytes/s between multiple boards. A number of Link-ports are available at the P2 connector for multiple board interconnection or data acquisition.

### SHARC On PMC

Longtime SHARC board vendor Ixthos Inc. offers a scalable solution by putting SHARCs on PCI mezzanine cards. The Quad SHARC PCI mezzanine card (PMC) can work as a high-powered, on-board compute engine or as a high-performance bridge to external SHARC processors needing to link to the PCI bus *(Fig. 1)*. Called the

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The 5V and 3.3V Full Performance K1526B Series comes in a 6 J-leads SOJ-20 ceramic package including a standard tri-state selectable pin with optional -40°C to +85°C operating temperature range.

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# Champion

## LOW COST SMT VCXO

An efficient, low cost option in surface mount VCXOs, the K1526LC Series features an Absolute Pull Range (APR) that meets your PLL tuning needs. Tri-state output selectable with a frequency range from 2 to 55 MHz and 3.3 Volt optional supply.


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## NEW SMT VCXO

The K1526C Series, Champion's newest innovation in 5 Volt Full Performance SMT VCXOs, features a 4 J-leads SOJ-20 industry-standard footprint. It also provides ±25ppm stability, optional 3.3 Volt operation and frequency performance to 55 MHz.


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## 5x7mm SMT VCXO

Champion's newest SMT configuration is a 5 x 7mm 5V and 3.3V extremely low profile ceramic leadless chip carrier (CLCC). The CMV Series offers an operating temperature range option of -40°C to +85°C as well as a frequency range of 2 to 52 MHz.


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IXZPMC4, the board incorporates four SHARC DSPs to deliver 480 MFLOPS of computing power completely within the host-board environment. And, it has a PCI-SHARC throughput of 132 Mbytes/s (80 Mbytes/s sustained) on a 32-bit, 33-MHz PCI bus.

This computing power effectively reduces the delay between data acquisition and processing by eliminating the need to perform off-board data transfers to another DSP engine. On baseboards containing two PMC slots, almost a full GLOP of computational power can be delivered before resorting to off-board units for additional processing power.

In applications requiring off-board data communications, data can be transferred between the IXZPMC4 and other DSP boards through the SHARC Link-ports and the serial port. Eight front-panel IXLinks can simultaneously transfer data at rates up to 40 Mbytes/s for an aggregate transfer rate of 320 Mbytes/s. Through the Pn4 connector (which maps to the P2 connector), the user can transmit data via four Link-ports (20 Mbytes/s each) and one serial port.

## Secondary Bus Alternative

One approach to accommodating the high-throughput needs of DSP applications is the use of secondary buses. The most popular of these include RACEway, SKYchannel, and Myrinet. CPSI, the main driver of the Myrinet specification, uses Myrinet in its 2641 MultiComputer, a high-performance processing module for the 2000 series systems.

Each computational node of the 2641 MultiComputer is equipped with a 300-MHz PowerPC that's capable of processing signals at up to 600 MFLOPS. It features a cache-coherent, 64-Mbyte local memory and a 320-Mbyte/s Myrinet connection to other nodes within the system. It provides more than 2.4 GFLOPS of computational power within the standard VME 6U form factor.

Alacron is another DSP board vendor who is offering Myrinet-connected products. The first product in the company's FT-Dominator series provides both VME64 and PMC interfaces. Through the FT-Dominator's PMC interface, the SHARC DSPs can provide DMA capability directly to Myrinet, making possible a network of full-duplex communication in excess of 1 Gbit/s—ten times the speed of Fast Ethernet. In this manner, the FT-Dominators can be employed in in-cabinet clusters connected by a Myrinet system-area network (SAN) or can serve as compute nodes in large distributed systems connected by a Myrinet LAN.

The board is a scalable array of up to eight SHARC processors interconnected using Alacron's Dual Ported Local Memory (DPLM) architecture. The DPLM design eliminates processor contention for off-chip memory, permitting memory bandwidth of the SHARC array to scale linearly with the number of SHARC processors.

A two-dimensional DMA engine isolates the SHARC array from the system bus, shielding it from the impact of system bus traffic while performing data movement and scatter-gather operations.

## Reach For The Sky

Another secondary bus alternative is SKYchannel, a 320-Mbyte/s 64-bit packet bus. Last year, the bus was approved as an ANSI standard (ANSI/VITA 10-1995) for high-performance communication over VME P2.

Up to 256 VME boards can be connected in a single SKYchannel system. When used with SKY compute daughtercards, SKYchannel enables up to 4096 PowerPC, SHARC, or Intel i860 microprocessors to work together in a distributed shared memory architecture. SKY provides design support for other VME vendors who have products with a SKYchannel VME P2 interface.

SKY's newest board is a 333-MHz version of its Excalibur line. Excalibur 333 delivers 2.66 GFLOPS in a 6-↔-6-in. daughtercard. The Excalibur 333 extends the Excalibur family to include both 250- and 333-MHz versions.

Each Excalibur 333 includes four PowerPC 604e microprocessors. One Excalibur 333 configured on a 6U VME motherboard delivers 2.66 GFLOPS of performance. On a 9U VME motherboard, four Excalibur 333 daughtercards deliver 10.66 GFLOPS, with total performance in a single VME chassis of 170 GFLOPS. Coupled with SKY's advanced memory system design, the

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PowerPC 604e microprocessor sustains memory bandwidth at 667 Mbytes/s and executes a 1k complex fast Fourier transform (FFT), (memory to memory) in 174 µs. Recently, Sky announced that it will use Motorola's new, fourth-generation PowerPC microprocessor with AltiVec technology in its next generation of embedded high-performance computers, expected in the field by mid-1999.

## RACEway Races Ahead

Among the high-speed, secondary bus choices, RACEway, developed by Mercury Computer Systems, enjoys the most third-party support. Part of RACEway's success is its link to PCI. A RACEway-to-PCI bridge provides a method for handling legacy VME hardware. This helps many companies who have invested fortunes in VME-based hardware. The RACEway-to-PCI interface allows a mix of VME and PCI boards in a chassis. The boards can interface through a RACEway-PCI chip.

Mercury recently began offering RACE systems featuring Motorola's PowerPC 750 microprocessor operating at a core voltage of 1.9 V. Motorola's 1.9-V PowerPC 750 microprocessor will be available for PCI, VME, and MultiPort form-factor systems.

## Software Radio On RACEway

As an open standard, RACEway has moved beyond Mercury as third-party vendors embrace the technology. Pentek offers the newest RACEway product, the 6526, aimed at bandwidth-hungry applications. Bandwidth is the name of the game for high-end software-based radio systems. They require high-density, DSP-intensive performance for such applications as beamforming, signal tracking, and mobile communications systems.

The 6526 is the first digital receiver to attack the bandwidth need with RACEway. The RACEway communications fabric can span up to 20 VME-bus slots, provide simultaneous data paths, and support an aggregate transfer rate of over 1 Gbytes/s.

The 6526 16-channel, two-input narrowband digital receiver can sample signals at up to 62.5 MHz with 16-bit accuracy. This single-slot 6U VME board has front-panel connections for input clock, data, and synchronization signals. It includes a 32-bit, VMEbus slave interface for control and status. The parallel inputs operate at TTL or differential ECL logic levels and support up to 16 bits of data at sampling rates up to 62.5 MHz for ECL, 50 MHz for TTL, and 40 MHz for front-panel data port (FPDP) levels.

Using four Graychip GC4014 quad narrowband digital tuner chips, the board provides a total of 16 receiver channels. The 16 identical channel formatter sections accept serial output data from the GC4014s, convert the data to 32-bit parallel words, and then form single-channel data packets. The 160-Mbyte/s RACEway interface lets individual packets of data from each receiver channel be directed to specific processors on any RACEway-equipped DSP boards in the VMEbus system.

## On The Small Side

Bittware, a maker of small form-factor DSP boards, is one of the few vendors of single-processor SHARC boards. Its latest product, the Spinner, is a high-performance audio board designed for professional-audio OEM applications. By integrating 24-bit, 96-kHz analog and digital audio interfaces with ADI's new, low-cost ADSP-21065L SHARC chip, the Spinner provides audio equipment designers with a signal-processing platform for demanding audio applications.

The Spinner achieves 360 MFLOPS of floating-point power from the board's two 30-MHz ADSP-21065L processors. It has up to four channels of analog-to-digital and digital-to-analog conversion. The board supports standard interface protocols, such as AES/EBU, for transferring digital audio data between professional digital audio equipment like PCM and DAT mastering recorders, modular multitrack recorders, and other equipment.

The Spinner is available with either one SHARC processor and an 8-bit digital I/O port for data acquisition, or with two SHARC processors and a 16-bit digital I/O port. A Mbyte of flash is available as nonvolatile memory. A 16-Mbyte bank of SDRAMs is available to the 21065L processors at a 60-MHz clock rate. A dual UART allows the Spinner to communicate with external serial devices.

STANDARDS WATCH

# Happy 10th Anniversary For VESA, New Activities Ahead

**Bill Lempesis,** VESA Executive Director

As the Video Standards Electronics Association (VESA) approaches its tenth anniversary, it continues to play its role as the worldwide forum for setting industry-wide interface standards for PC, workstation, and computing environments. VESA has been accepted by ANSI/ISO under its JTC 100 program for fast-track electronic-industry standardization. As a Publicly Acceptable Submitter (PAS) of standards, VESA has been acknowledged worldwide for its organizational structure and standards development process.

VESA includes the Display, Display Metrology, Marketing, Home Network, PC Theatre, and VPort Committees. Each committee has its own charter and reports to the VESA board of directors.

The Display Committee, established in 1998, combines the membership and activities of the VESA Monitor, FPDI, and Plug and Display (P&D) committees. Its goals are to create standards related to computer displays and graphics controller hardware, including standards for display timings, interfaces, specifications, and measurement procedures, as well as all display control and identification forms. It oversees 11 workgroups, which cover technical areas related to Display Power Management, Enhanced Video Connector/Plug and Display (EVC/P&D-A), Signal Standards, Flat-Panel Display Measurements (FPDM), Electro Magnetic Currents (EMC), Display Timing, and P&D Document. The groups also delve into Display Committee Marketing, Transition-Minimized Differential Signaling (TMDS), Digital Flat Panel (DFP), and the Color Workgroup.

The Home Network Committee, founded in 1995, is developing an open industry architecture standard for consumer digital home networks, with an interoperability specification which will allow the orderly transfer of information between devices in the home—between different networks, from low to high bandwidth, and from analog to digital. This specification also will provide directory services for devices in the home and a common interface on the home side of the network interface unit (NIU).

The PC Theatre Committee, formed in 1997, has developed a PC Theatre Interconnectivity standard. This should permit PC and CE manufacturers to produce PC Theatre computer and display products that are compatible, easy to use, work together as a single system, and support automatic configuration. The PC Theatre Standard was published in September.

The VPort Committee's first standard, Video Interface Port (VIP), is an interface standard between the graphics controller and video devices, such as DVD, HDTV, and video decoders. The committee has been working on Version 2 of the standard. It'll be backward-compatible with VIP1.1, but with added features and much higher performance to support more demanding applications like HDTV. VIP2 standard development is essentially complete. Final ratification is expected in the fourth quarter.

VESA also sponsors special interest groups (SIGs). At Display Works '99 starting Feb. 2, 1999, at the San Jose Convention Center in Calif., VESA will initiate the VESA Micro-Display SIG. This first meeting will introduce the concepts of microdisplays, such as the four types of devices, products using these devices, and standardization. Participants will explore upcoming technology challenges related to product enhancement, including flexible and expandable data-path bandwidth requirements, function/product integration, and bi-directional data flow (to and from the chip).

Looking back over the years, it's clear that this anniversary year marks a record accomplishment of the development and publication of new standards. Among these are the PC Theatre, Display Data Channel Command Interface (DDC/CI), VBE 3.0, Monitor Control Command Set (MCCS), and Display Monitor Timings (DMT).

*Bill Lempesis is executive director of VESA. He can be reached at (408) 435-0333 ext. 226, or e-mail: bill@vesa.org. For more on VESA, go to www.vesa.org.*

wireless

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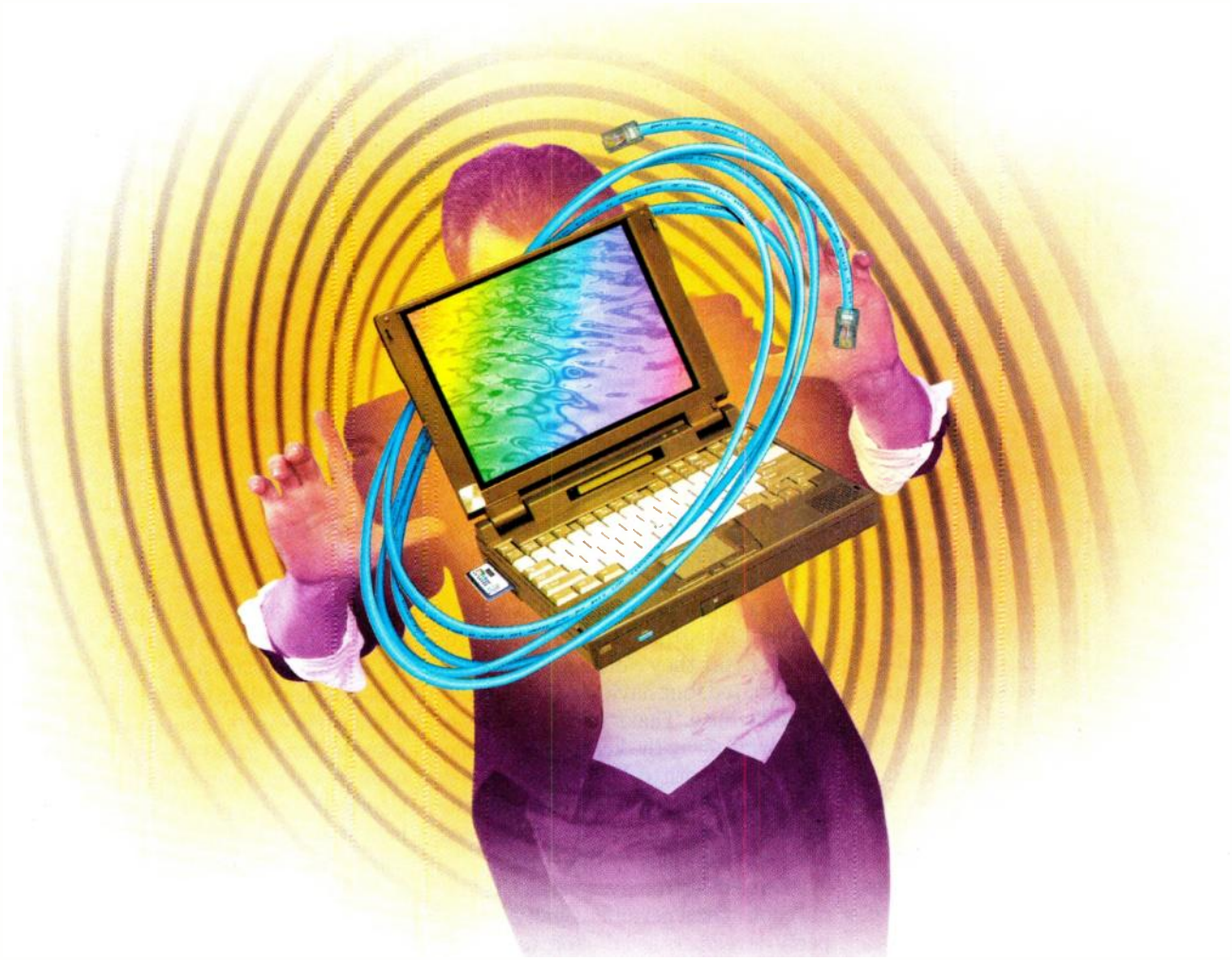

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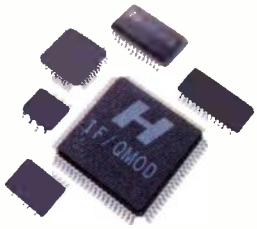


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# Scorched Earth Strategy

So far this year, I've received press releases from three embedded real-time operating-systems companies announcing the availability of their kernels royalty-free. One of them provides their source code on the web. Rumors abound that other kernel vendors will do the same. What's going on here? Why are they giving away their very complex products and forgoing royalties?

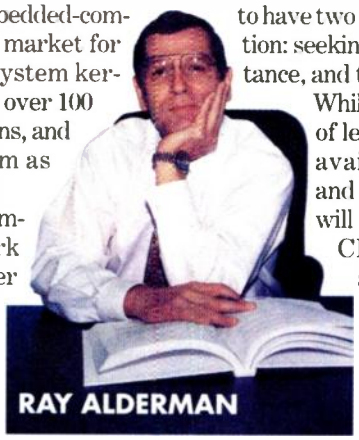
History teaches us never to invade Russia in the winter. Napoleon tried it, and the Russian farmers destroyed their crops, killed the animals, and burned the farms, leaving the invading army with no source of food or shelter in the harsh winter months. Germany invaded Russia in the winter in WWII, and met with the same disastrous result. The Russian "scorched earth" policy caused tremendous pain and suffering, as well as frustration and defeat, for the invaders.

The Russian army never mounted a serious frontal defense against invaders. They didn't have to in either case. Russian farmers changed the rules of war to a battle of attrition, instead of victory by strength of force. It was General Santayana who said, "Those who are not students of history are doomed to repeat it" (or something to that effect).

In traditional embedded applications (industrial, military, transportation, communications, medical, etc.), there's a cold and icy region of determinism that's very demanding of real-time kernel performance. Many of those applications require very fast responses to interrupts, context switches, and signals from all types of I/Os. Kernel and memory footprints range from a few kbytes to many Mbytes. Computer architectures span the spectrum, from single-processor systems in industrial controls to very complex multiple-processor architectures for military signal processing.

The real-time kernel market for 1998 is about $400 million. This shows why over 100 companies have grown and prospered, and why a one-size-fits-all kernel offering will have a very tough time of it. From a software perspective, these footprint and performance requirements create the equivalent characteristics of a Russian winter.

Enter Microsoft and the CE kernel, originally aimed at consumer products and now targeted at embedded-computer applications. The market for embedded-operating-system kernels is fragmented, with over 100 different APIs, tool chains, and driver structures from as many small companies.




Like the Russian farmers, these vendors work their own land, but never act together as a group. The kernel vendors are independent and mutually exclusive in their purpose of survival. Not one of them could put up a good fight against the invading CE forces. If they banded together under a single "kernel standard," they would lose their differentiation and still be ineffective in defeating the invader.

If they form small bands called "IDEs" (Integrated Development Environments), they can keep the market fragmented, but have some collective, small defense. That's what they're doing: giving away the kernel and enhancing its value with tools, support, and services. Kernel vendors are changing the rules of war for embedded software, and Microsoft can't play by those rules.

Microsoft's strategy is to sell CE kernal copies for a per-unit royalty. Third-party developers sell the software tools, drivers, compilers, simulators, and development environments for CE. If traditional kernel vendors give their kernels away, Microsoft faces the same "scorched earth" strategy as Napoleon and Hitler. Vendors will make money by selling API-specific tools, services, and support now—not from kernel royalties.

And, Microsoft could be trapped without food and shelter in the middle of that cold and icy region of real-time embedded applications. If my observations are correct, Microsoft will have to retreat from Russia and concentrate their troops in less-demanding markets, like consumer and entertainment appliances, where performance demands are less stringent and manufacturers will pay a per-unit royalty. CE will have to show its buyers a better value proposition than a free kernel, which could be like slogging through a Russian snowstorm.

Embedded-software markets seem to have two basic principles of operation: seeking the path of least resistance, and the lowest possible cost. While CE may offer the path of least resistance with the availability of many tools and the Win32-subset API, will that be enough to offset CE kernel royalty? After all, tools are a one-time purchase that can be expensed or amortized over many units. Per-unit royalties are a variable cost included in each product shipped.

Whether you're a high- or low-volume embedded-system manufacturer, the primary business objective is to reduce variable costs in a competitive market. You can't do that paying royalties on the software in your products, particularly if you're a high-volume producer. Besides, it's estimated that over 50% of all the real-time kernels in use are homegrown. These users have accepted their software as "fixed" costs and amortize them over thousands and millions of copies. Captive kernel users might just be willing to pay for a "free" kernel with good support services and tool availability.

Gillette gives away razors to get the razor-blade business. Ttelephone companies give away cell phones to get the service revenue. Netscape gives away the browser to get market share and to do an IPO. What can Microsoft give up to be successful with CE? They have to surrender the notion that they can make the traditional embedded-software markets homogeneous like the desktop markets. It doesn't work that way. That's why they haven't been forthcoming with a lot of real-time determinism and performance-enhancing features that bring CE up to par with many existing real-time kernels. That would be like invading Russia in the winter.

Microsoft gave away Explorer to keep up in the desktop operating-system business. But when they give away CE, they're at the end of the food chain. Redmond, Washington could be in for a tough winter this year.

*Ray Alderman is the executive director at VITA. He can be reached at exec@vita.com.*

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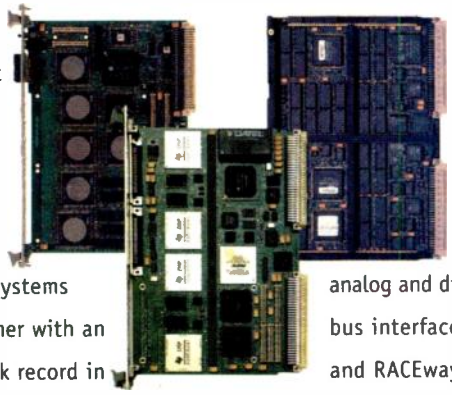

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## WHAT'S ON BOARD

**The combination of a high-performance graphics-display controller** and a high-resolution, 17.3-in. diagonal digital flat-panel monitor (FPM) allows designers and integrators to eliminate a typical 19-in., over 40-lb. CRT monitor. The 1600SW FPM, jointly developed by Silicon Graphics Inc. (SGI), Mountain View, Calif., and Mitsubishi Electric Co. Ltd., Itami, Japan, delivers the industry's best resolution at 110 dots/in. Full-screen resolution of 1600 by 1024 pixels is set up in an HDTV-like widescreen format. With the high resolution, extremely small font sizes can be displayed with high readability. And, two 8.5-by-11-in. pages can be displayed side by side. The FPM includes color management and white balance adjustment, and delivers the best color saturation of any commercial flat-panel monitor. To achieve such control, it uses a low-voltage differential signaling interface between the panel and the host. That interface uses an OpenLDI data-transfer protocol that supports resolutions up to 1600 by 1200 pixels. The display, with its adjustable height-weighted base, is only 7 3/8-in. deep and weighs 16 lb. In a wall-mount configuration, it's 3-in. deep and weighs just 8 lb....

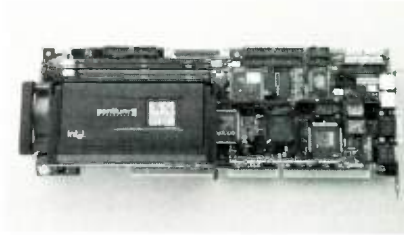
**...To deal with the interface's host-system portion,** SGI struck a deal with Number Nine Visual Technology, Lexington, Mass., to enhance Number Nine's just released Revolution-IV 3D graphics accelerator by adding digital outputs that can drive the OpenLDI interface. Based on the fourth-generation Ticket-to-Ride graphics-accelerator chip, the Revolution IV-FP card will include 32 Mbytes of graphics memory and drivers for Windows 95, 98, and NT. It'll have full Direct 3D V6.0 support for Win95 and 98, and an optimized OpenGL driver for NT. The accelerator provides 128-bit 2D/3D graphics processing at resolutions up to 1600 by 1024 pixels with 16 million colors. The Revolution IV-FP card and 16-lb. 1600SW monitor come as a $2795 set for PCI- and AGP 2X-based PCs and NT systems from Number Nine. A monitor-only option for the O2 workstations, available through SGI, lists for $2595. Support for the Apple Macintosh also is planned. Contact Silicon Graphics at (650) 950-1980 or www.sgi.com/go/flatpanel. To reach Number Nine, call (781) 674-0009 or go to www.nine.com/products/rev4fp.

**Targeted at PC companion and other portable products,** the SA-1101, a companion chip for the previously released SA-1100 StrongARM CPU from Intel Corp., Santa Clara, Calif., is a highly integrated solution for mobile systems. The 190-MHz CPU consumes less than 1/3 W when powered by 1.5 V. The SA-1101 adds a dual-mode display controller that supplements the SA-1100's color LCD controller. It allows the storage and display of different data on an external high-resolution projector and a handheld screen simultaneously. The chip also includes a USB controller, two PS/2-style serial ports, an IEEE 1284 parallel port, a keyboard-matrix interface, and general-purpose I/O lines. Operating systems for the StrongARM include WindowsCE, OS9, pSOS, Inferno, JavaOS, EPOC32, and VxWorks. In 10,000-unit lots, the SA-1100 sells for $33 apiece. The SA-1101 goes for $21 each. Contact Intel at (408) 765-8080, or at www.intel.com.

**Able to operate at a supply of just 1.8 V,** a 16-Mbit flash memory from Mitsubishi Electronics America Inc., Sunnyvale, Calif., includes a background operation (BGO) capability that lets it perform program and erase operations while reading data—a feature that lowers chip count in wireless handsets and other systems that must update stored data while operating. The BGO mode partitions the flash memory and dedicates some blocks for concurrent writes. The durable memory allows 100,000 program-erase cycles. To save space, it can be housed in molded, chip-scale packages optimized for mobile applications. The 16-Mbit BGO will come in 2.7- or 3.6-V versions (the M5M29GB/T160, 161B) with either a 2-Mword-by-8-bit or 1-Mword-by-16-bit organization, as well as 1.8-V versions (the M5M29WB/T161B) initially offered in a 1-Mword-by-16-bit organization. In lots of 10,000 units, chip-scale-packaged devices sell for $7 apiece with samples immediately available. Call Doug Llewellyn at Mitsubishi at (408) 730-5900, or go to www.msm.mea.com.

## Single-Board Computer Packs Dual Pentium II Punch

PC-compatible processors such as the Pentium are no longer considered a performance trade-off. And two of them are packed onto one board, the processing power will suit even the most demanding applications. The



TR-DP2 board combines dual Pentium II processors with on-board 10/100Base-T Ethernet, Ultra Wide SCSI and AGP SVGA interfaces to provide optimum performance for telecommunications, server, and imaging applications. Intel's 440BX AGPset supports the system/memory bus at 100 MHz.

The TR-DP2 offers symmetric-multiprocessing (SMP) capabilities to increase performance and system throughput. SMP applications are divided into threads that can run concurrently, allowing the operating system to assign tasks on demand to the next available processor. This maximizes the dual Penfium II processors' capacity.

Two dual in-line memory module (DIMM) sockets support auto detection of memory to up to 512 Mbytes of SDRAM. Rounding out this full-featured SBC are two independently programmable FIFO serial ports, a floppy interface, a parallel port, a PS/2 mouse, and two USB 1.0 ports. A system hardware monitor provides monitoring of system voltages, temperatures, and fan speeds. The TR-DP2 is in full compliance with the PCI Local Bus 2.1 and PICMG 2.0 specifications.

The TR-DP2 SBC is available in four performance models up to 450 MHz. Evaluation and production boards are available this month with prices starting at $3569.

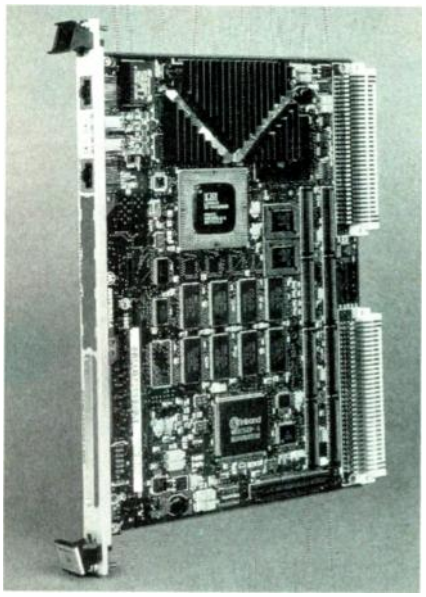
***Trenton Technology Inc.,*** *2350 Centennial Dr., Gainsville, GA 30504; (800) 875-6031; fax (770) 287-3150; www.trentonprocessors.com.*

**CIRCLE 519**

## PowerPC VME Boards Push Performance Curve

The PowerPC processor architecture still dominates the world of RISC VME board-level computers. VME market leader Motorola unveiled the next set of products on its VME PowerPC roadmap by announcing updates to existing PowerPlus VME Architecture SBC families. These updates include versions with the latest PowerPC microprocessors, including the 366-MHz PowerPC 750 and the 333-MHz PowerPC 604, plus several new derivatives.

New models introduced include the MVME2700 single-board computer, with the 366-MHz PowerPC 750 microprocessor and 1 Mbyte backside Level 2 cache; the MVME2300SC, a derivative of the MVME2300 with a P2 I/O pinout that provides access to a SCSA TDM backplane bus (SC-bus) from both PMC sites; the MVME2300LC, an entry level version of the MVME2300 with a 100-MHz PowerPC 604 processor; and the MVME2600 single-board computer family with the 333-MHz PowerPC 604 microprocessor.



Also available in the PowerPlus VME Architecture family are the MVME3600 and MVME4600 system boards. They possess single and dual PowerPC 604 microprocessor configurations, respectively.

The MVME2300, MVME2600, MVME2700, MVME3600, and MVME4600 are available in a variety of models for immediate production needs. The 366-MHz MVME2700, the MVME2300SC and the MVME2300LC will be available this month (December). Single unit pricing begins at $1695 for PowerPC 604 boards.

***Motorola Computer Group,*** *2900 S. Diablo Way, Tempe, AZ 85282; (602)-438-3025; www.mcg.mot.com*

**CIRCLE 553**

## CPU Board Supports 14 Compact PCI Slots

By supporting dual Compact PCI buses off the same CPU board, users can get a hefty slot count. One such CPU, known as the CP610, represents a complete PC on a single 6U format board. It can be used as a standalone single-board computer, or as the CPU

*(continued on page 98)*

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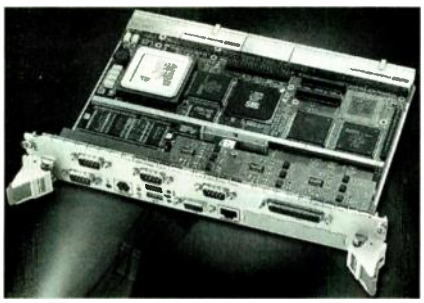
READER SERVICE 156

*(continued from page 96)*
in a CompactPCI system with two CompactPCI buses, thereby enabling it to drive up to 14 I/O modules. It also includes an on-board PMC slot.

The CP610 can accommodate most



current Socket-7 microprocessors, including low-power versions and those with clock rates in excess of 300 MHz. It's designed for CompactPCI systems that require a large number of I/O slots, providing two CompactPCI buses on connector pairs P1,P2 and P4,P5 on one slot (4HP).

The CP610 has built-in numeric coprocessor support, and has a SiS 5598 Pentium System Controller. The SiS 5598 provides all of the latest system controls, including a Level 2 write-back cache controller, burst DRAM controller, PCI/ISA interface, and more. Various memory options are offered to match customers' system requirements, including 32 or 64 Mbytes of on-board RAM with the expansion capability of 64 Mbytes of EDO or SDRAM on a SO-DIMM module.

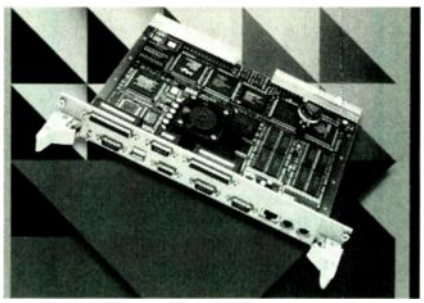
The CP610 is designed to operate with just passive cooling, providing an operating temperature range from 0 to +60°C. An optional 8HP version has an operating temperature of –25 to +75°C.

Mass-storage support is provided by two EIDE interfaces and a floppy-disk interface supporting two drives. In addition, the CP610 features up to four serial ports and a parallel port, two USB interfaces, and a Fast Ethernet (10Base-T/100Base-TX) interface. Pricing for the CP610 starts at $1965.

***PEP Modular Computers Inc.**, 750 Holiday Dr., Bldg. 9, Pittsburgh, PA 15220; (412) 921-3322; fax (412) 921-3356; www.pep.com.* **CIRCLE 554**

## Compact PCI Board Musters Up For Harsh Duty

For harsh and rugged military and industrial applications, VME is no longer the only game in town. Compact PCI boards fit for rough duty are starting to emerge. SBS Embedded Computers



offers a new 6U Compact PCI Pentium CPU board designed specifically for such environments. In a single slot design, the CR6 combines all relevant PC platform components on one board, plus additional features like a CAN (controller area network) interface for

*(continued on page 100)*

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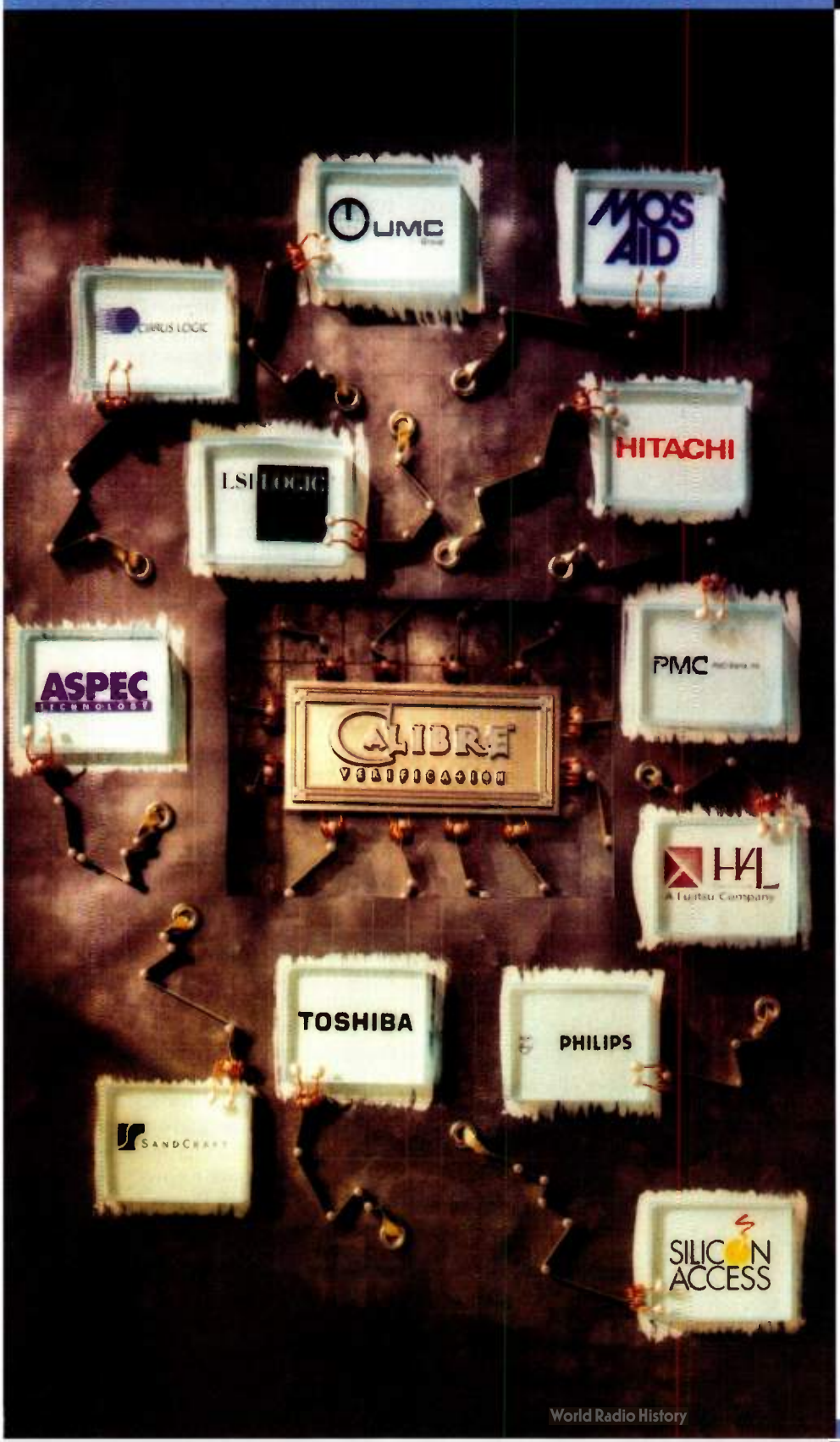


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*(continued from page 98)*
distributed I/O, and solid-state flash disk drives.

The CR6 routes all I/O functions to the backplane. With all I/O on the backplane and options for various levels of ruggedization, including conduction cooled, the board is suited for harsh environments applications with high shock, vibration, and extended temperature operating environments.

The board supports Pentium MMX CPUs up to 233 MHz; K6 CPUs up to 300 MHz; 128-Mbyte DRAM; 256-kbyte L2 cache; on-board flash drive options up to 240 Mbytes; PCI SVGA with a 64-bit Windows accelerator and LCD flat panel interface; and so on. The CR6 is available in various build grades from commercial to ruggedized extended temperature with a –40 to +85°C operating temperature range.

Pricing varies depending on board build configuration. A commercial version (CP5) starts at $2100, while a fully ruggedized, conduction-cooled CR6 starts at $6400.

***SBS Embedded Computers,*** *6301 Chapel Hill Rd, Raleigh, NC 27607-5115; (919) 851-1101; fax (919) 851-2844; www.sbs-embedded.com.*

**CIRCLE 555**

## 450-MHz Motherboard Targets Sub-$1000 PCs

What's interesting about the push for PCs priced under $1000 is that cutting-edge processor speeds are part of the picture. Along such lines, the Tigercub 100 is a Pentium II Micro ATX motherboard for system integrators and OEMs. The board supports up to 450-MHz Pentium II processors, as well as the latest Celeron CPUs.

The board's footprint is actually smaller than the MicroATX standard, but it will easily mount inside a MicroATX or standard ATX chassis. The design is based on the Intel 440BX chip set. With a 66- to 100-MHz bus, the motherboard features ample expansion capacity with three PCI bus master slots, one shared ISA slot, and one AGP port.

System assemblers can populate the AGP port with a high-performance 2x AGP graphics accelerator for extremely responsive 3D graphics, or an entry level AGP adapter for more cost-effective systems. The board includes three 168-pin DIMM sockets to support up to 768 Mbytes of SDRAM.

Drive support includes Ultra DMA/33, which gives users access to the fastest hard drives available while maintaining compatibility with older EIDE/IDE drives. The board also features dual channel PCI Bus Mastering ports, two serial ports, a parallel port, a floppy disk connector, and Twin Universal Serial Bus (USB) ports for up to 126 compatible peripheral devices.

Standard power- and system-management features include Wake-on LAN support, power recovery after interrupt, Win95 Soft Power Down, and memory autodetect. List price is $189, with "street" prices expected to be $150.

***Tyan Computer Corp.,*** *3288 Laurelview Court, Fremont, CA 94538; (510) 651-8868; fax (510) 651-7688; www.tyan.com.* **CIRCLE 556**

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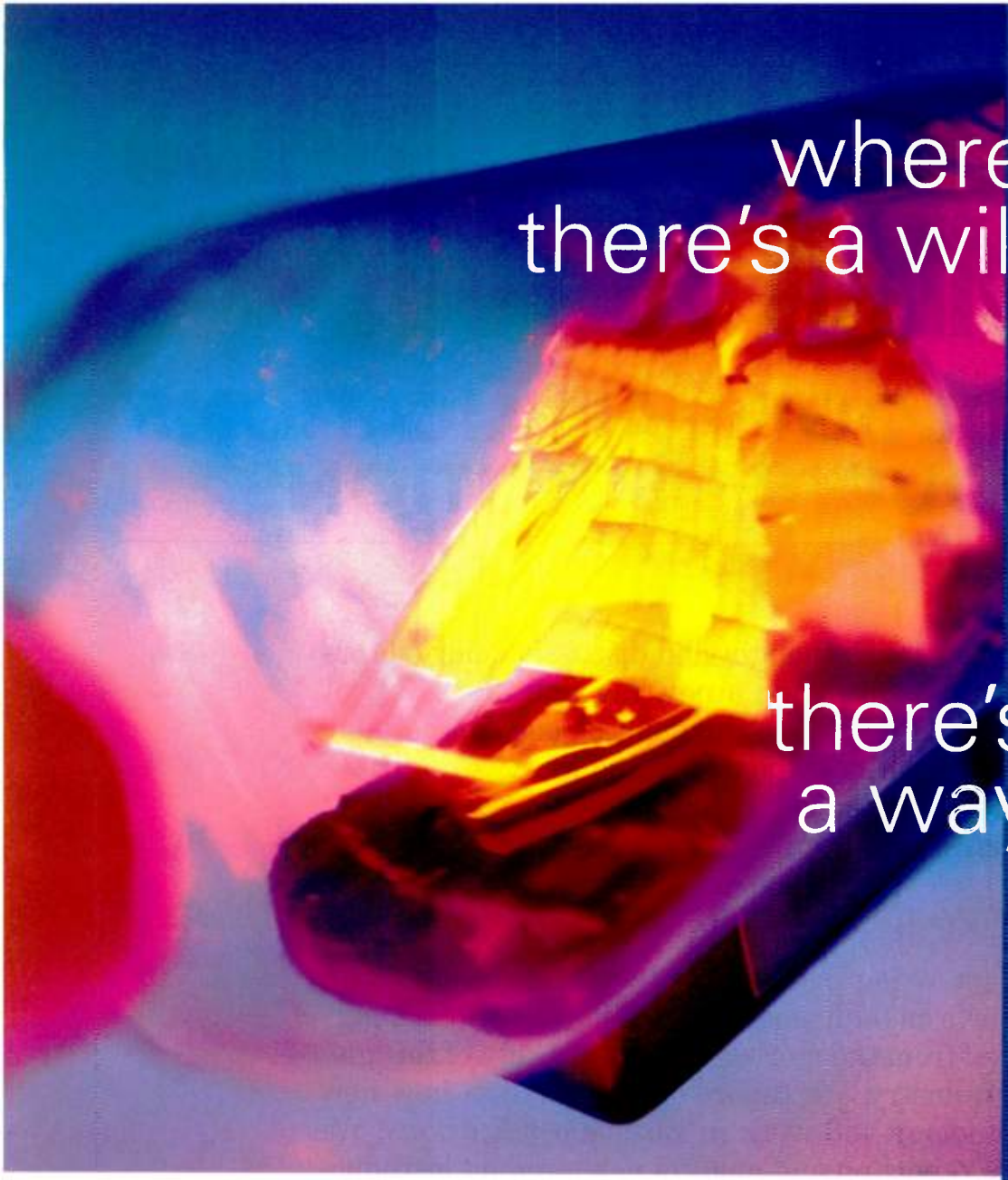

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# PIPS

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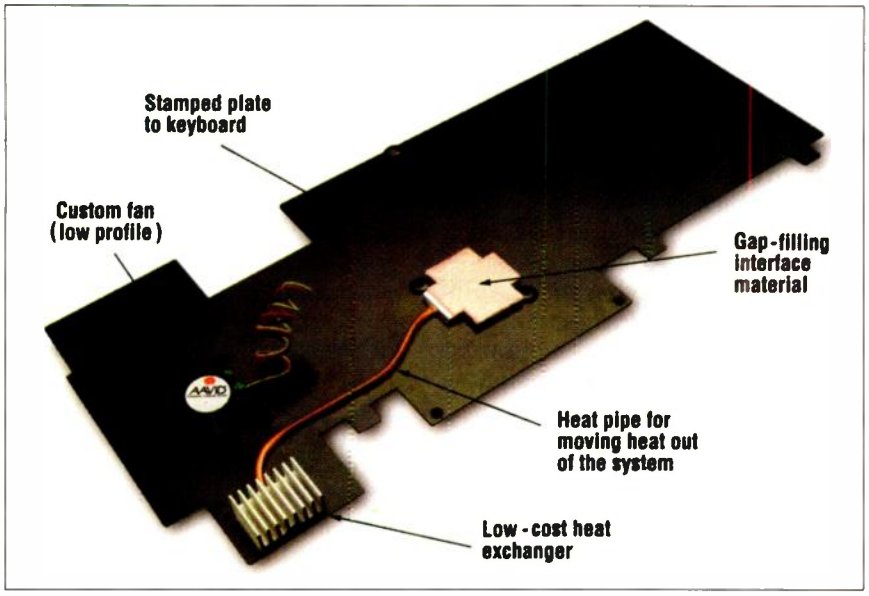
# Notebook Computers: Get That Heat Out!

*Despite Rising System Integration Levels, Thoughtful Foresight Can Eliminate Heat And Make For A Really Cool Design.*

**CHRIS CHAPMAN,** Aavid Thermal Products Inc., 143 North Main St., Suite 206, Concord, NH 03301; (603) 629-2235; fax (603) 223-1738; www.aavid.com.

Electrical issues traditionally take precedence in the design of notebook computers. But, as system functionality per square inch shoots skyward, thermal issues are now moving closer to the forefront. With heat-generating microprocessors and other electronic components being packed into a limited space with restricted airflow, heat inevitably becomes a problem. It can cause anything from erratic behavior to complete system failure.

To date, methods to alleviate thermal effects range from an extensively modeled, optimum component layout that minimizes system cost to a sophisticated high-power fan with speed control to maximize battery life. Since every notebook is different, however, a unique thermal solution exists for each system. Heatsink manufacturers, thermal-modeling software providers, and others active in thermal issues can assist the designer in this complex area.



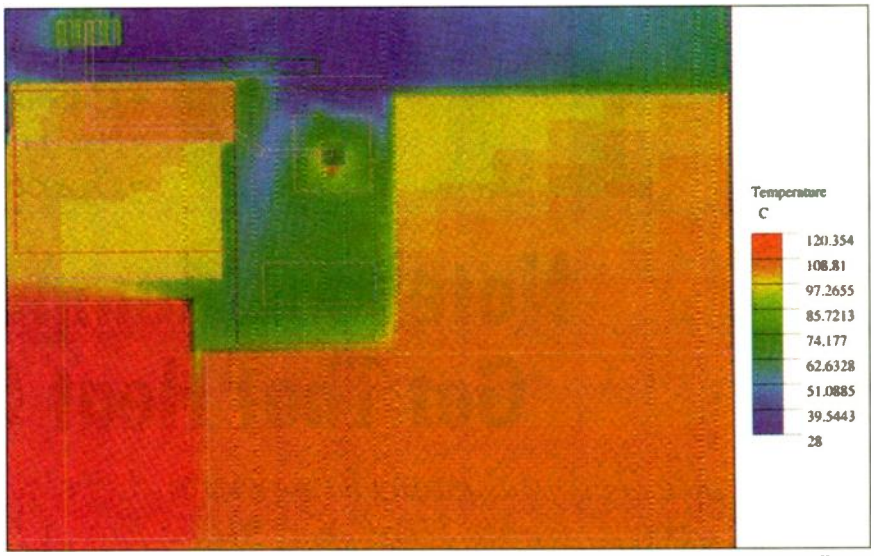

**1. A custom cooling solution for a high-end notebook design requires the integration of many subcomponents into one assembly. These components can include a stamped plate for passive cooling and a gap-filling thermal-interface material that provides a thermal pathway from the CPU (not shown) to both the stamped plate and the heat pipe. They might also feature a heat exchanger where directional airflow from the custom, low-profile fan can take the heat out of the system.**

In addition, the global requirements for notebooks may suggest the use of a thermal consultant with global expertise and support. Whatever method is chosen, space constraints, battery life, weight, and system cost all demand that the thermal issues be addressed during the early phases of system design.

## Design Constraints

Thermal design in notebooks is particularly challenging because system heat tends to increase the temperature of all components—even those that generate little heat themselves. The heat-removal rate is driven by the temperature differential between the inside and the outside of the notebook. The chassis itself can dissipate only a limited amount of heat, as it must remain comfortable to the touch. Furthermore, long battery life is a selling feature for notebooks, so optimal solutions must minimize the draw on the battery. Portability also is necessary, so the thermal design must not add significant weight to the package. To add to this issue's complexity, notebooks restrict the maximum height of the thermal solution to under one inch.

Heat from low-end notebooks can be eliminated with proper component placement and inexpensive heatsinks. Yet the high-end notebooks, with their greater power draw, require high-performance fan systems as well as strategic vent placement to optimize airflow. To preserve battery life, the smallest




**2. While the heatsink effectively cools the CPU (located left and up from center), there is still significant heat transfer from the CPU to the hard drive (red section, lower left). Unless the layout is modified, the hard drive will be subject to frequent failure.**

fan possible must be used. This minimal airflow requires that the heatsinks and pipes conform to tight operational tolerances. Ease of installation also is important. Attachment of the heatsink and heat pipe usually occurs after the CPU has been installed. These thermal components must align with both the CPU and the chassis, so they must also conform to tight physical tolerances.

## Thermal Solutions

*Heat pipes and heat plates:* Solutions for low-end notebooks can be very cost-effective. Here, the primary heat generator is the CPU. Simply keeping the CPU away from the hard drive maintains hard-drive reliability at essentially no cost. The heat from the CPU can then be piped out using a 3-mm-diameter heat pipe that's connected to a stamped aluminum plate on the back of the keyboard. The aluminum plate can typically absorb 2 to 4 W without significant temperature rise. The heat is then dissipated through the keypad.

A straight, round heat pipe can dissipate up to 15 W. Maintaining the low profile of the more expensive notebooks requires more intricate designs. These designs increase the need to bend and flatten the heat pipe, decreasing the amount of heat dissipated. Adding 90° bends or flattening the pipe can reduce effectiveness to as little as 6 W. These low-profile notebooks require additional thermal solutions.

*Heatsinks:* For low-end to mid-range notebooks, small, inexpensive extruded heatsinks provide sufficient additional cooling when the heat pipe cannot carry the whole load. Finned heatsinks dissipate the most power in the smallest amount of space, incrementally increasing the ability of the designer to dissipate heat passively. This is a low-cost solution. But for some applications, more fin density may be needed. This, in turn, requires more space. Folding the fin increases the surface area available without increasing the space occupied. The folded-fin heatsinks are more expensive than the simple extruded variety. Still, the amount this adds to the cost of manufacturing is more than compensated for by the increase in the retail price of the higher-end notebook.

*Airflow control:* Properly placed vents provide airflow to remove the remainder of the heat from the system. As the notebook's complexity increases, simple fans can raise the airflow, thereby improving heat transfer out of the system. A variable-speed control fan is an innovative solution to battery life limitations, offering additional margin on high-end systems. Whenever the user accesses high levels of computing capacity, and the CPU is generating the maximum amount of heat, this type of high-performance fan operates at maximum speed. When computing levels decrease, the fan slows down to conserve battery power.

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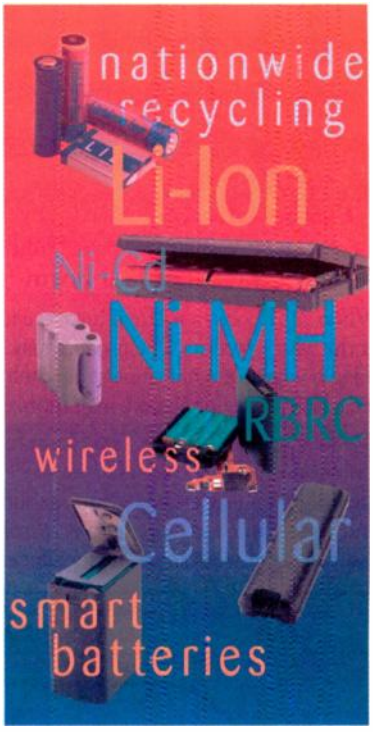


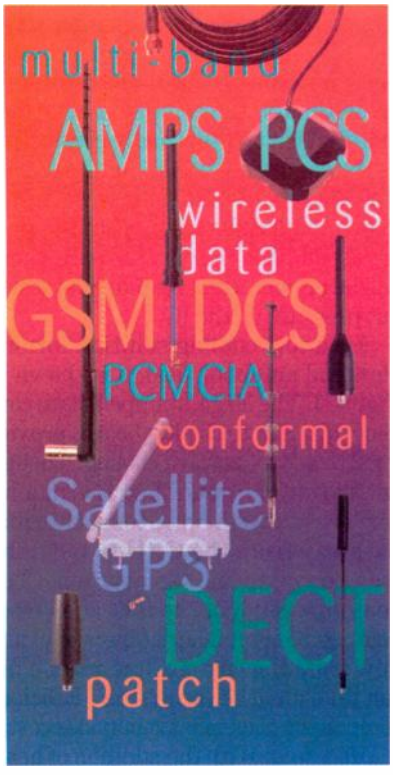


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This solution also reduces acoustic noise, since the noise associated with the fan is proportional to fan speed. Though these fans are approximately 10% more expensive than the conventional ones, the extension of the battery life increases the marketability of the notebook, justifying the added cost.

*Thermal materials:* Pliable, compressible thermal-interface materials can also play a role in keeping notebooks cool. The aluminum plate is located on top of the chassis under the keypad, while the IC is mounted to the bottom of the chassis. Tolerance stackup between the CPU and the chassis creates a variable gap in the thermal-conduction path. By compressing gap-filling, compliant, interface materials between the CPU and the chassis-mounted heatsink, thermally conductive material replaces the air gaps. Doing this ensures good thermal contact between the CPU and the heatsink. Even though the compliant interface material isn't as thermally conductive as the commonly used 5-mil-thick pad, it also isn't subject to the tolerance mismatch that might occur with that pad. If the pad is too thin for the space, there will be no contact. If it's too thick, it will put pressure on the IC.

A custom cooling solution for one high-end notebook design is shown in Figure 1. The large, stamped plate connects directly to the keyboard, providing 2 to 4 W of passive cooling. Though not shown, the gap-filling thermal-interface material creates a thermal pathway from the CPU to both the stamped plate and the heat pipe. The heat pipe conducts heat to a low-cost heat exchanger, where directional airflow from the custom, low-profile fan can take it out of the system. Efficient component placement minimizes cost.

*Modeling:* With the addition of heat-generating ICs other than the CPU, the thermal issues become much more involved. Thermal solutions for these more complex notebooks typically cost two to three times that of a low-end notebook. The standard, 3-mm heat pipe isn't large enough to dissipate the heat generated in these systems. By using a thermal modeling package, such as Icepak from Fluent Inc., Lebanon, N.H., the designer can optimize board layout to take advantage of the natural thermal convection and directional airflow provided by a fan.

# Problem:

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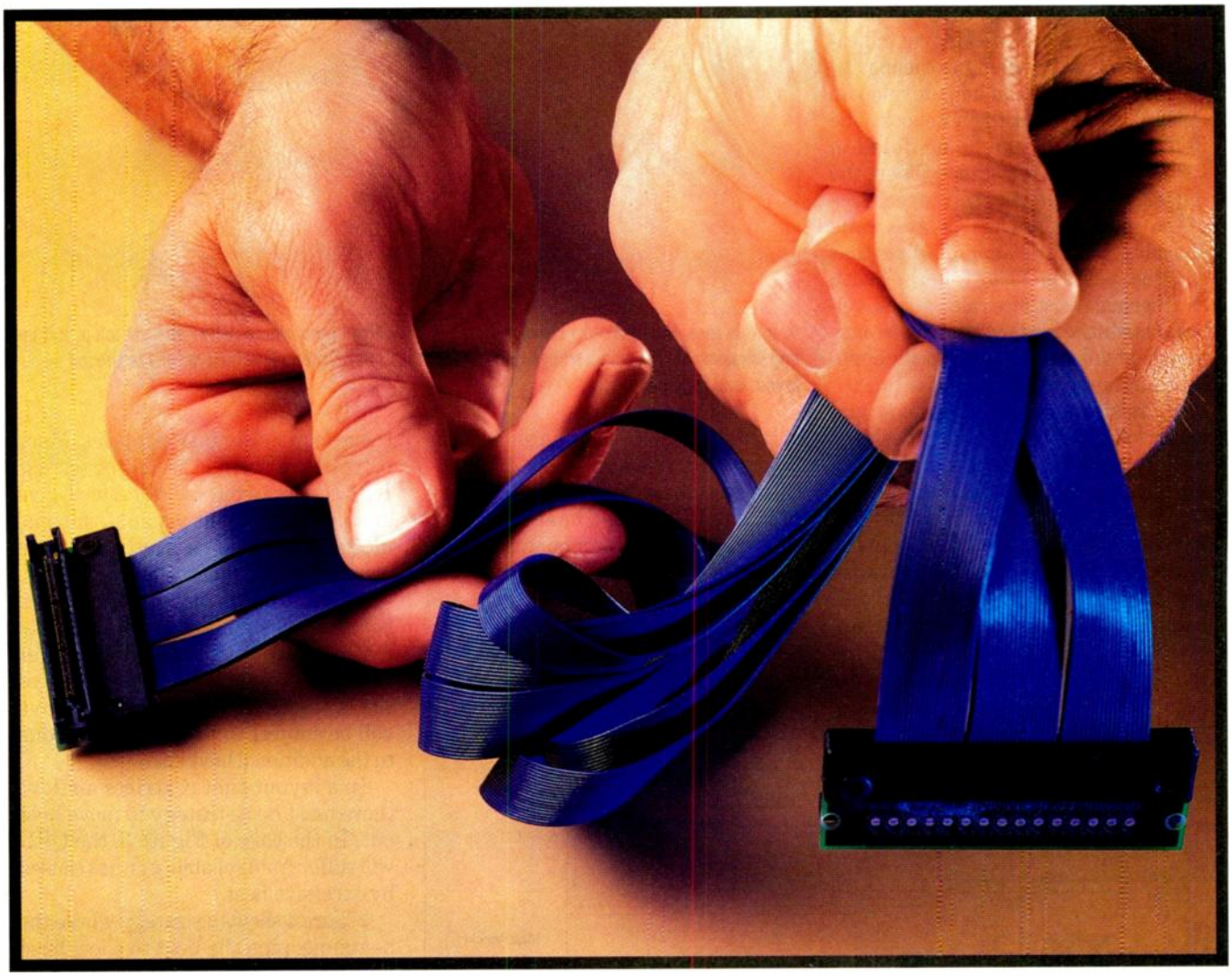

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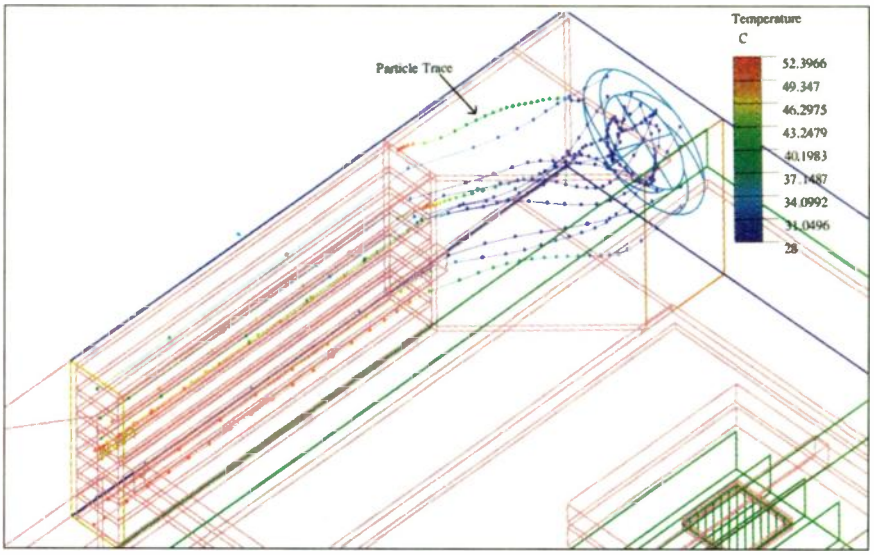
Thermal modeling can predict the heat generated by each component in a particular system and model the effectiveness of the thermal solution. Such programs are capable of taking existing CAD files and determining the airflow direction and velocity at any point in the notebook. They also calculate thermal resistance, offering an indication of thermal transfer and cooling.

The same tools can help develop an optimal heatsink for the notebook. The heatsink design can be modeled in terms of volume resistance. Then, the modeling package can analyze each face of the heatsink for the free-area ratio characterizing the amount of air that can flow past the face. Together with the thermal resistance calculations, volume resistance is a powerful tool to optimize heatsink design for a specific application in the shortest amount of time.

By modeling different low-cost and passive thermal solutions, the designer can reduce the overall cost of the thermal solution. Without modeling, the designer will need to prototype the system and try "what-if" scenarios in hardware. Often, "what-if" scenarios are difficult or impossible to cover with a single prototype. So, additional prototypes must be built and tested. Although modeling increases up-front design time, it allows for multiple "what-if" analyses—typically reducing system test time and often eliminating the need for redesign.




**4. In this case, the heatsinks bring the heat to a localized area where active airflow can pick it up and eliminate it. The temperature chart shows that this strategy is effective for the chosen layout and component mix.**

In systems with multiple heat generators, designing a heatsink to address several hot components in close vicinity may minimize the height of the heatsink itself. Now, the layout and heatsink design phase must occur simultaneously. The complexity of the thermodynamics with two heat generators makes thermal modeling of the new heatsink imperative. Without it, the design-cycle time increases. Much more time is spent in prototype testing. It's also easy to miss a critical heat-generating component without thermal modeling. Any shortcuts to these processes can result in missed data.

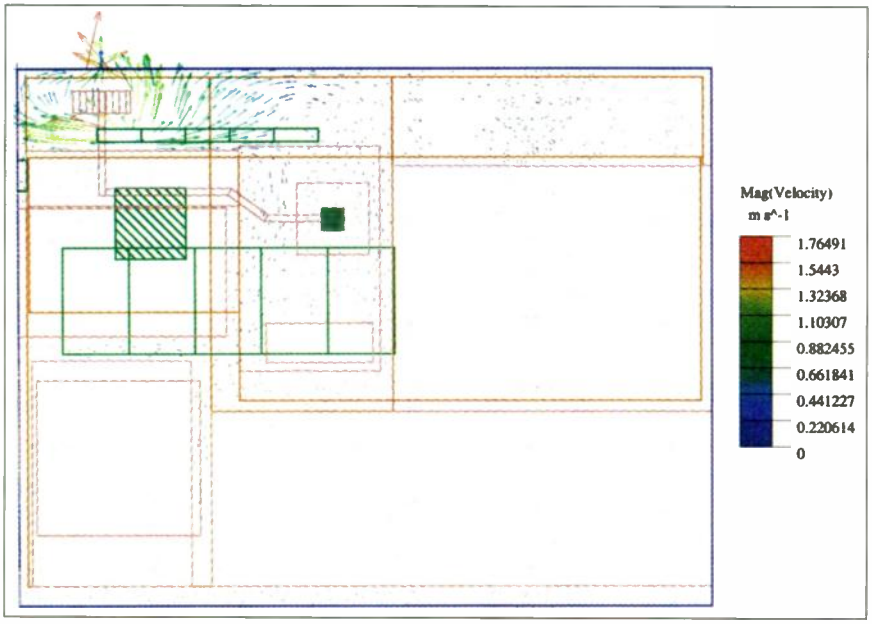
Figure 2 shows a layout in which the heatsink effectively cools the CPU. Yet it also shows significant heat transfer from the CPU to the hard drive. Unless the layout is modified, the hard drive will be subject to frequent failure due to the additional heat load.

In a layout that restricts airflow, there must be a strategy to move heat out. In the case of Figure 3, the CPU will suffer from reliability issues caused by excessive heat.

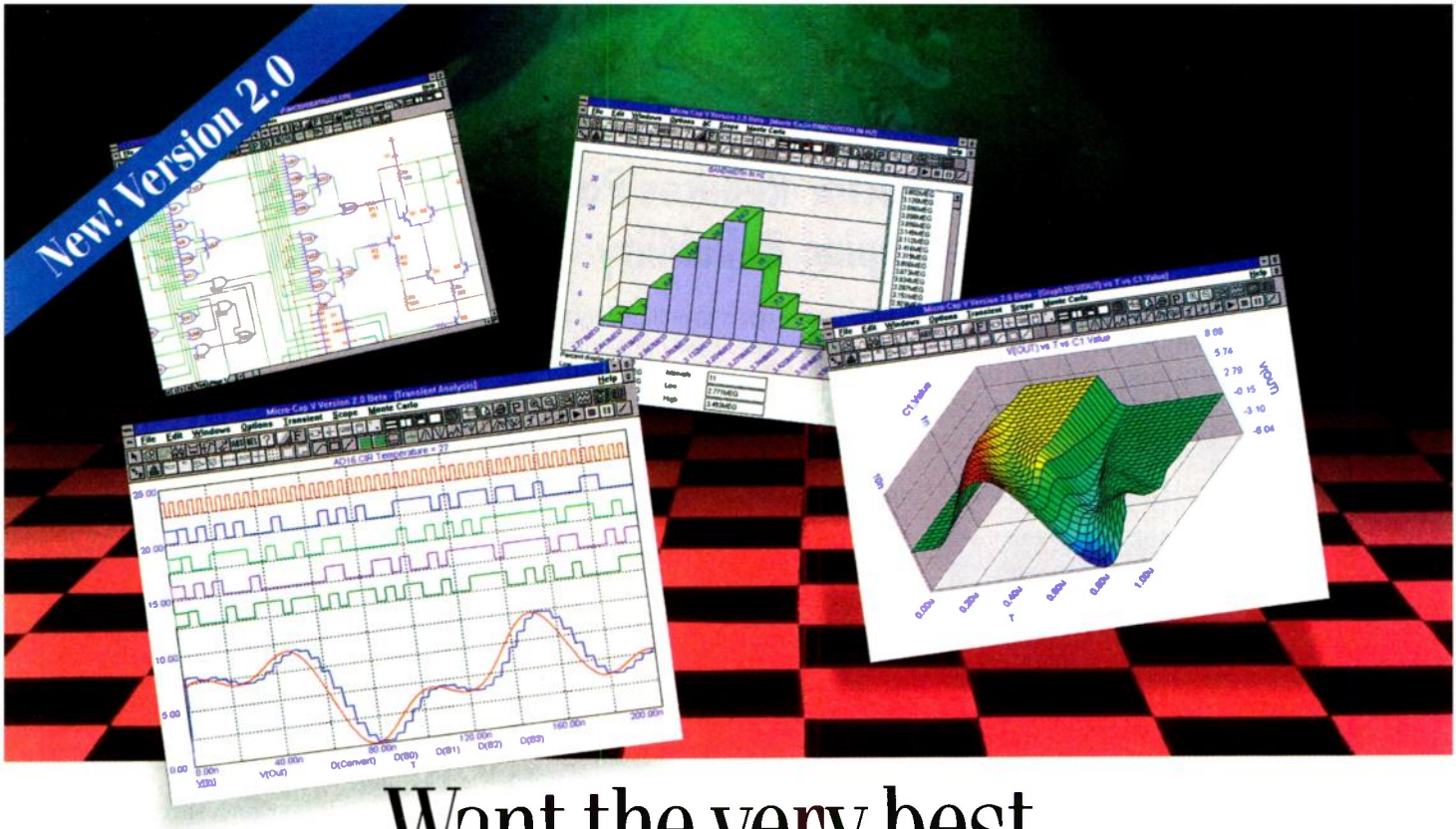
Figure 4 shows a strategy where the heatsinks pipe the heat to a localized area where active airflow can pick it up and eliminate it. The temperature chart shows that this strategy is effective for the chosen layout and component mix.

These examples display how thermal modeling identifies thermal problems before the hardware is built. Such modeling exemplifies how the lowest-cost solutions, such as layout and passive heatsinks, can be tested and compared with more expensive solutions to generate the most robust, reliable package.

*Chris Chapman is a computer industry manager at Aavid. Prior to joining Aavid eight years ago, he graduated from the University of New Hampshire at Durham with a degree in chemical engineering.*




**3. A layout that restricts airflow without a strategy to move heat out of the areas with no airflow can compromise the CPU's reliability. In this case, the heat pipe channels the heat from the CPU (left and up from center) to the heatsink (striped square). Unfortunately, the fan (upper left corner) is ineffective because of an obstruction between it and the heatsink.**




# Want the very best in Analog/Digital simulation? Introducing Micro-Cap V Version 2.0

Micro-Cap V is a fast, precision, 32-bit analog/digital simulator with an intuitive fifth generation user interface, and a library of more than 10,000 pre-modeled parts. Based on Spice3 and PSpice™, it offers the best features and capability of both.

Its finely crafted simulation tools include schematic probing, during the run plotting, performance plots, 3D plots, multidimensional stepping, analog and digital behavioral modeling, an optimizing model generator, and Monte Carlo analysis. Compiled models, behavioral primitives, and a huge library of commercial parts make modeling of both analog and digital devices easy. New devices in Version 2.0 include BSIM 1.0, 2.0, and 3.3, sample and holds, Z transforms, and three new animation devices.

Download the free working demo at www.spectrum-soft.com.

We offer the very best in analog/digital simulation and we guarantee it with a 30 day money back guarantee!

You can't lose. Call us for a free brochure and working demo or download the demo from our Web site.

Micro-Cap V runs on PCs under all Windows systems from 3.1 and up. Cost is $3495 complete.

## Features

| | |
|---|---|
| • Mixed Analog/Digital | Yes |
| • Analog Engine | Spice3 & PSpice™ |
| • Digital Engine | Native PSpice™ |
| • During the Run Plots | Yes |
| • Analog/Digital Primitives | 200+ |
| • Analog/Digital Parts | 10,000+ |
| • Performance Plots | Yes |
| • Parameter Stepping | Multidimensional |
| • Optimizing Parts Modeler | Yes |
| • 3D Plots | Yes |
| • Schematic Probing | Yes |
| • Behavioral Modeling | Analog & Digital |
| • Monte Carlo | Yes |
| • Device Temperatures | Individually Set |
| • BSIM Devices | Yes. 1.0, 2.0, and 3.3 |
| • Animation Devices | Yes |
| • Import/export Netlists | Yes |
| • Guarantee | 30 Day Money Back |
| • Technical Support | By EEs for EEs |

spectrum

**Spectrum Software**

Phone 408-738-4387
FAX 408-738-4702
Internet www.spectrum-soft.com
E-mail sales@spectrum-soft.com

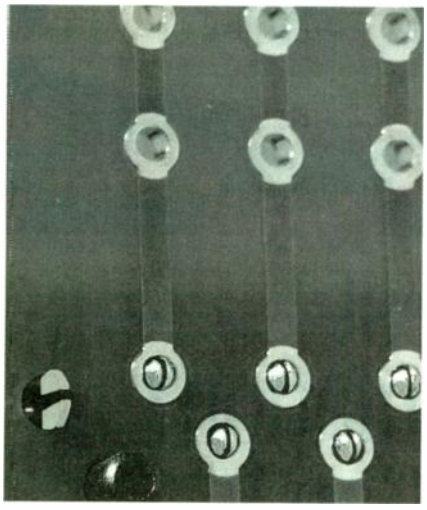


READER SERVICE 186

PRODUCT FEATURE

# Novel Board-Level Connector Reduces Parts Count And Cost While Upping Reliability

Using patent-pending encircled electronic compression (EECOM) technology, Ranoda Electronics Inc. has demonstrated a board-level connector that could go a long way toward slashing the cost of board-level connectors—while raising their reliability. The connector system eliminates the female part completely, and instead plugs directly into plated through holes in the host pc board.



The connector achieves electrical contact with compressible transverse terminals (split pins) that plug directly into the 1-mm-diameter pc-board holes. Each opposing pin half presses against its side of the hole circumference with a force of 10 g. Any shock or vibration in one direction that would tend to pull the contact faces apart is nullified by the opposing g forces. These opposing forces simultaneously push the opposite faces together.

According to the company, the two simultaneous contacts result in higher reliability and lower contact resistance. Figures given for each are 1000 mate/demate cycles and 1 mΩ or less, respectively.

Each connector comes molded in a high-temp thermoplastic housing that secures the pins in place. The housing also includes an orientation pin and two spring clips that locate the header into position and fix it to the pc board. The contacts are tin-lead plating over copper alloy—no gold is used. The per-contact insertion force is rated at 50 g maximum, while the withdrawal force is 60 g minimum.

Other features include a contact voltage rating of 100 V ac, a current rating of 1 A, an insulation resistance of 500-MΩ minimum, and a dielectric withstand voltage of 1000 V ac for 1 minute. Along with raising reliability and lower cost, the connector's advantages also include reduced space and speedier time to market. Pricing is $0.02 to $0.06 per contact per million. Delivery is four weeks.

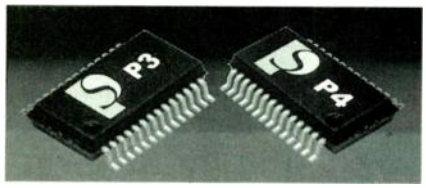
***Ranoda Electronics Inc.***
*1010 Depot Hill Rd. #104*
*Broomfield, CO 80020*
*Sales Dept. (303) 404-9880*
*fax (303) 404-9878*
**CIRCLE 485**
**PATRICK MANNION**

# SMBus/I²C Smart-Battery ICs Are The Most Accurate And Programmable To Date

Designed for use with all battery chemistries, the P4 and P3 families of high-accuracy, programmable smart-battery ICs come with on-chip flash EEPROM or expandable nonvolatile memory, respectively. Although both are fully SMBus-compliant, the P4 also can be configured as a non-Smart Battery System (SBS) device for implementing custom I²C protocols and data values.

Stemming from an Intel partnership with Duracell, the SBS is an open battery- and computer-interface specification that allows for greater than 98% accuracy on remaining battery-power readings. Other features of the standard include the use of Smart Battery chargers, which allow the battery to control its own charge to prolong battery life; the ability to use any battery chemistry in any Smart Battery-compliant system; and the inclusion of hooks so that a Smart Battery can be used by the Advanced Configuration and Power Interface (ACPI) standard. Information on the standard, including the recently introduced version 1.08, is available at *www.SBS-Forum.org/*. Comments on the new version are invited.

The latest additions to the company's line of SBS-compliant devices, the P3 and P4 use an integrating, self-calibrating, 14-bit, analog-to-digital converter (ADC) to ensure precise measurements with an accuracy of




±1%. The devices also employ patented, self-learning, three-dimensional cell models to compensate for self-discharge, temperature, charge/discharge efficiencies, and other factors. An advanced RISC processor accelerates computations.

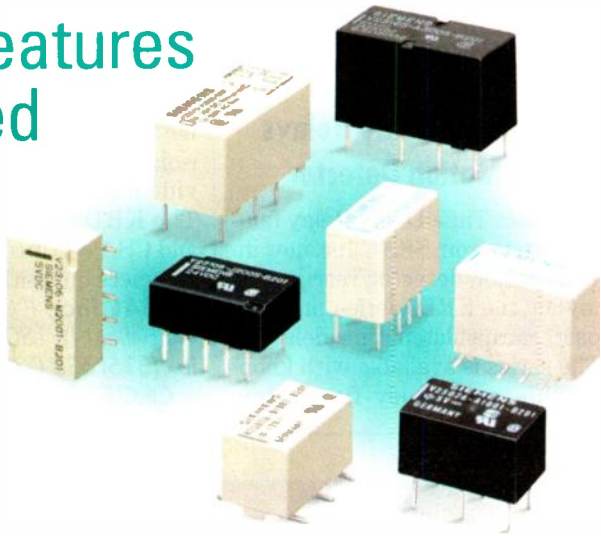
The P4's 6 kbytes of EEPROM contain the core battery control algorithms, cell-chemistry performance models, and associated equations for battery-capacity calculations. The block also includes pack calibration information and all learned and historical data. With supplied configuration and utility software, over 250 preprogrammed battery parameters and algorithms can be modified as needed by battery manufacturers for their particular cell chemistries and applications. The P3 uses external EEPROM of various sizes and densities for programmable parameters and algorithms. Program modifications and updates are possible via the SMBus interface, even after pack assembly.

The devices come in a standard 28-pin, 209-mil SSOP. Pricing is under $4 each in quantity. Samples of the P4 are available now, with production in February. P3 production is scheduled for January.

***PowerSmart Inc.***
*One Research Dr.*
*Shelton, CT 06484*
*Michael Mattera (203) 225-2423*
*Fax (203) 925-1714*
*www.powersmart.com*
**CIRCLE 486**
**PATRICK MANNION**

SIEMENS

# Our new low-signal relays offer more of the features you need



## You wanted more, and we've got it

Your designs demand more, so we're providing more! We've expanded our line of low-signal relays. New models provide just the features you need for application in telecommunications equipment, computer peripherals, security systems, office automation and more. These relays offer:

- Through-hole and surface mount termination options.
- Choice of low-profile or minimal PC board area types.
- Isolation meeting FCC Part 68 and Bellcore specs.
- Single-pole as well as double-pole designs.
- Load carrying capability to 150W or 250VA.
- Non-latching, single-coil latching and dual-coil latching models.
- Ultra-sensitive coils.

## There's still more

Great product features are just the beginning. You're assured of consistent quality, as these relays are produced on fully automated lines. Of course, we support you with the same level of service you've come to expect from Potter & Brumfield Products Division, an ISO9001/QS9000 registered company that's been delivering dependable, innovative switching solutions for more than 60 years.

| Series | V23026 | V23106 | V23079 | V23105 | V23042 |
|---|---|---|---|---|---|
| Contacts | SPDT | DPDT | DPDT | DPDT | DPDT |
| Dim. (mm) | 13 x 7.9 x 6.9h | 14 x 9 x 5h | 14.5 x 7.2 x 9.9h | 20 x 9.8 x 12h | 20.1 x 10 x 10.6h |
| Contact Rating | 30W 60VA | 30W 62.5VA | 60W 62.5VA | 60W 125VA | 50-150W 250VA |
| Nominal Coil Power | 30-150mW | 100-200mW | 70-140mW | 150-300mW | 75-360mW |
| Terminals | Pin or SMD | Pin or SMD | Pin or SMD | Pin | Pin |
| Fax Doc. # | 8026 | 8106 | 8079 | 8105 | 8042 |

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Peachtree City, GA 30269-1498
Fax 770.371.2604
e-mail: info@sec.siemens.com


READER SERVICE 184

## Monolithic Pressure Sensor Tackles Tough Applications

The 4000PC Series monolithic pressure sensor from Honeywell's Micro Switch Division offers accurate sensing and a wide temperature range. Its


stainless-steel port construction affords users product reliability and increased quality for touch applications. The monolithic design enables the elimination of discrete amplifiers and temperature-compensation circuitry.

The fully signal-conditioned sensor offers accuracy of 0.2% at 25°C, 2% at –45 to 85°C, and 3% at –45 to 125°C. It operates on a 5-V dc supply voltage and has a 4-V dc span. Operating temperature range is –45 to 125°C.

Typical applications include liquid-level indication systems, part-positioning equipment, and pressure monitoring systems. List price at the 50 to 99 piece quantity is $68, with availability in two to four weeks. Price discounts are available for OEM quantities.

***Honeywell's Micro Switch Division,*** *11 W. Spring St., Freeport, IL 61032;(800) 537-6945; fax (815) 235-6545; www.honeywell.com/sensing/.*

**CIRCLE 530**

## Family Of Time-Delay Relays Includes A Motion Detector

The Compact Time Delay Relay family of products from SSAC Inc. now includes a motion detector/retriggable single shot, the KRD9 series, an ultra-compact, encapsulated, time delay relay. The series is available with knob-adjustable or factory-fixed time


delays from 100 ms to 1000 minutes six ranges. Its repeat accuracy is ±1' Input voltages include 12, 24, and 1 V dc or 24 and 120 V ac. All models o fer 10-A SPDT relay contacts that a isolated from the input voltage to pr vide maximum switching flexibilit The KRD9 series is UL recognize and CSA certified. Pricing is $20.80 100-piece quantities.

***SSAC Inc.,*** *P.O. Box 1000, Baldwinsville, NY 13027;(315) 638-1300; fax (315) 638-0333; www.ssac.com.*

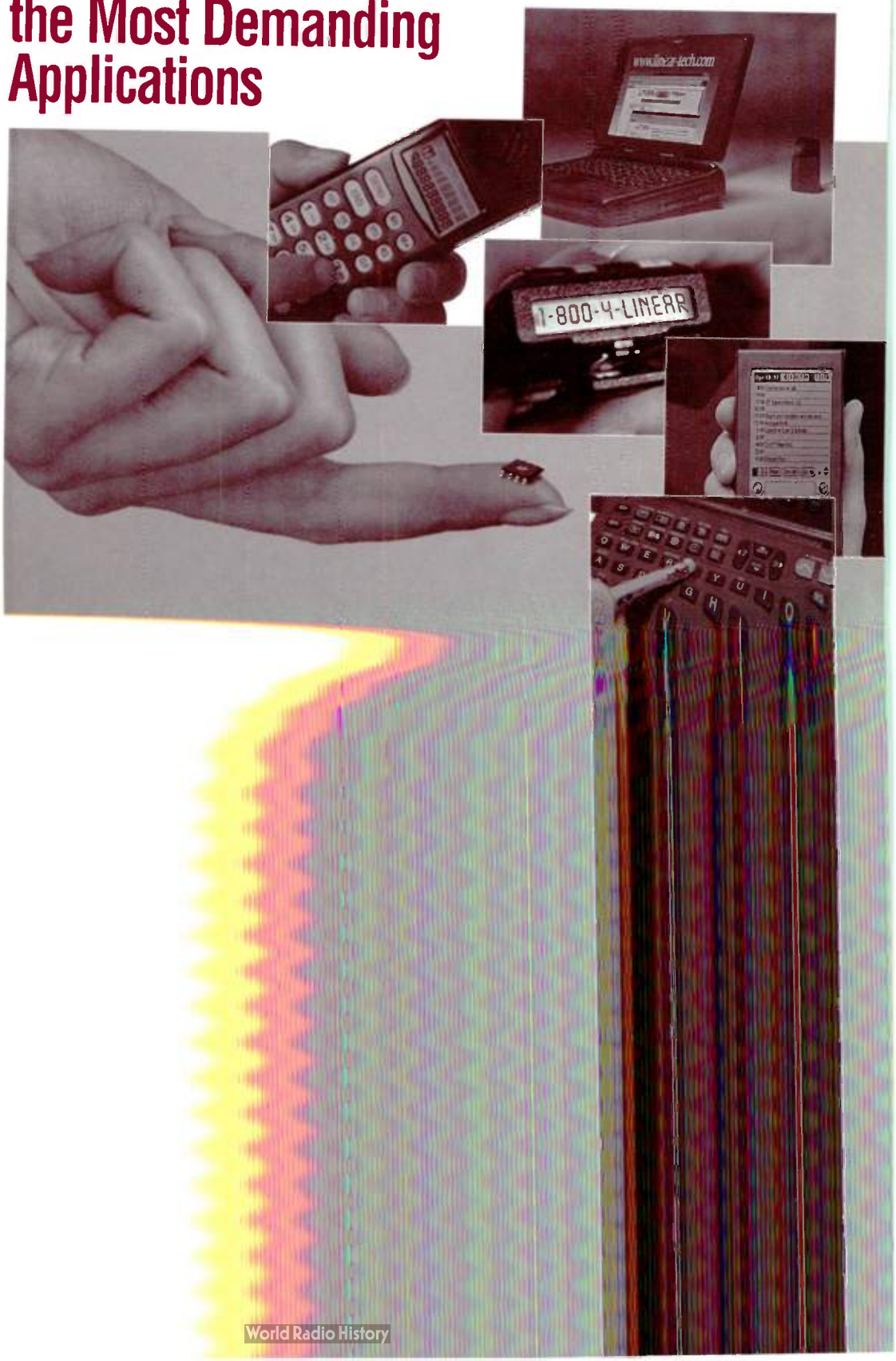
**CIRCLE 531**

LINEAR TECHNOLOGY

# LinearSolutions

## Battery Management

# High Performance Battery Management Solutions for the Most Demanding Applications



# World's Smallest PWM Battery Charger

**FEATURES:**

- Voltage-programmable charge current up to 1.5A with up to 90% efficiency
- Constant-current/constant-voltage for Li-Ion or constant-current for NiCd/NiMH
- 0.5% $V_{REF}$ accuracy and 3% typical charge current accuracy
- 3µA quiescent current in shutdown - no blocking diode needed
- 8V to 28V input voltage range - works with any wall adapter
- Current sensing at either battery terminal
- LT1510: 200kHz, 16-lead SO, SSOP and DIP
- LT1510-5: 500kHz, 16-lead SSOP

The LT1510-5 is the smallest, most integrated solution for charging batteries used in portable electronics. Its 500kHz operating frequency and small 16-lead SSOP package make it ideal as an embedded charger in cellular phones, PDAs and other hand-held instruments.

**www.linear-tech.com/go/LT1510**

LT1510: $3.00 ea. for 1K-piece Qty.

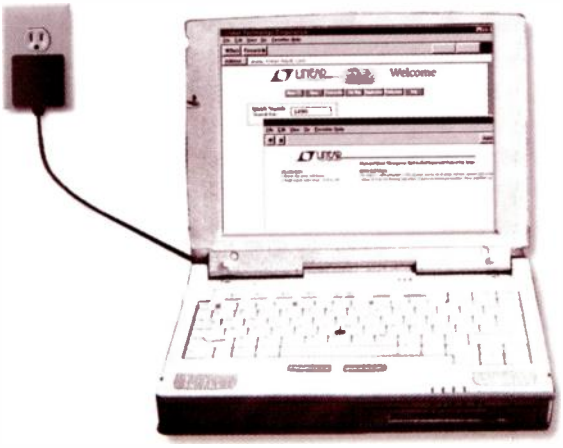
# Fast Charge While You Work

**FEATURES:**

- Input current sharing allows maximum charging current while system is operating - without overloading the wall adapter
- Constant-current/constant-voltage for Li-Ion or constant-current for NiCd/NiMH
- Internal 4A switch provides up to 90% charging efficiency
- 8V to 28V input voltage range - works with any wall adapter
- Resistor-programmable charge current
- 200kHz switching frequency
- 24-lead SO package

The LT1511 is a high efficiency switched mode constant-current/constant-voltage source that charges batteries with up to 3A while protecting the wall adapter from current overloads.

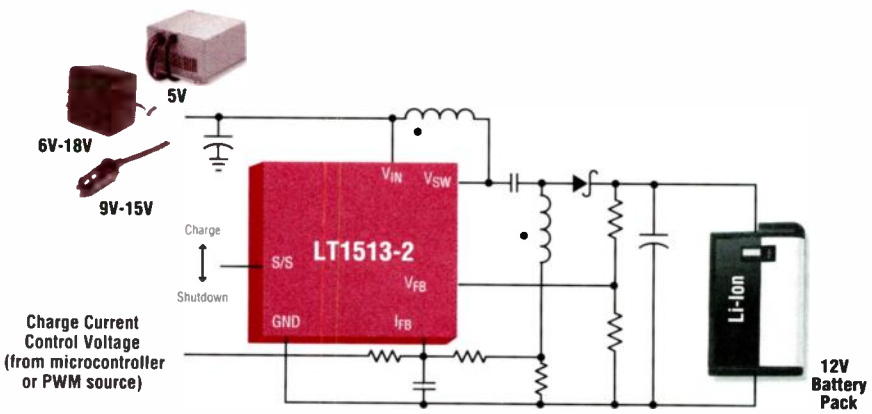
**www.linear-tech.com/go/LT1511**



# SEPIC Charger Operates From Wide Input Voltage Range

**FEATURES:**

- SEPIC topology with a 2.7V to 30V input voltage range allow charging from input voltage sources that are above, below or equal to the battery voltage
- Simple charge current programming from milliamps to over 2A, depending on the control voltage (LT1513-2)
- 500kHz switching frequency minimizes inductor size
- Current sensing is separate from battery path, allowing battery to be grounded
- LT1513: 3A switch in 7-lead DD or TO-220 packages
- LT1512: 2A switch in SO-8 package




The LT1513 is a 3A, 500kHz PWM battery charger that uses a SEPIC (Single Ended Primary Inductance Converter) topology to allow constant current regulation when the input voltage is above or below the battery voltage.

**www.linear-tech.com/go/LT1513**

LT1513-2: $4.20 ea. for 1K-Piece Qty.

# High Efficiency, Low Dropout Charge Current Controller

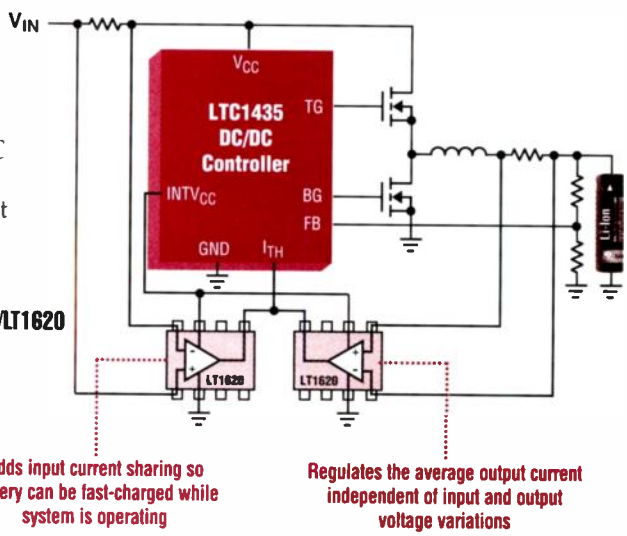
**FEATURES:**

- Up to 97% charging efficiency when used with LTC synchronous switchers
- Voltage-programmable charge current control
- Input current sensing allows minimum charging time
- LT1620: 8-lead SO/MSOP or 16-lead SSOP*
- LT1621: Dual LT1620s in 16-lead SSOP

* 16-lead package includes current comparator that can terminate charge in Li-Ion and SLA applications

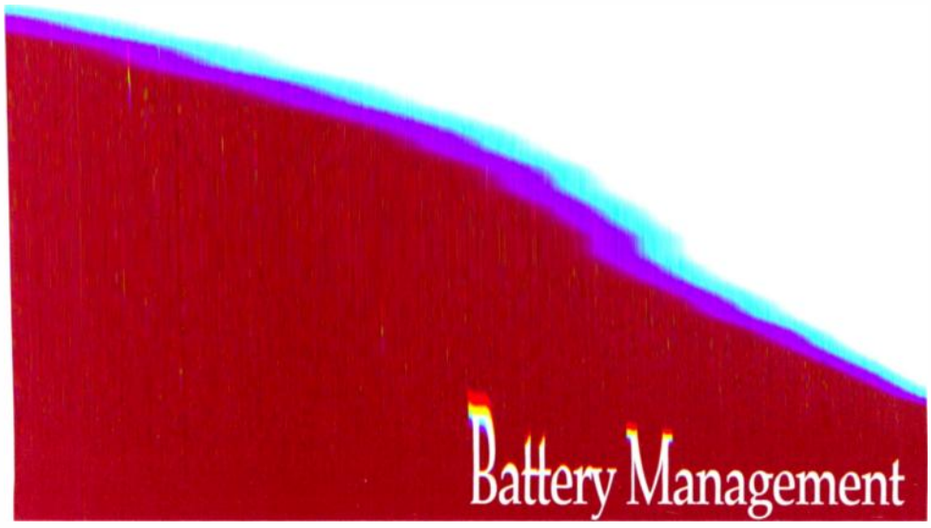
The LT1620 current sense amplifier transforms LTC current mode DC/DC controllers into high efficiency, high current battery chargers with very low dropout.

**www.linear-tech.com/go/LT1620**




LT1620: $1.80 ea. for 1K-piece Qty.

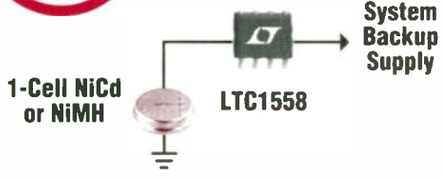
For literature only: call **1-800-4-LINEAR** www.linear-tech.com




# Battery Backup System Provides Power From Single NiCd Cell

**No More Li-Ion Backup Battery Stacks**

The LTC1558 provides a complete rechargeable battery backup solution that operates from a single NiCd or NiMH cell, making it ideal for use in notebook computers, PDAs and other space-limited portable applications.




**FEATURES:**

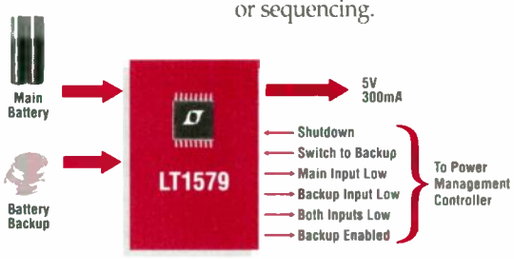
- Fully integrated battery backup solution includes 1.2V synchronous boost converter, 2-stage smart charger with gas gauge, automatic backup switching logic and µP reset generator in SO-8 package
- Provides all functions necessary to implement a 100mW backup power supply using a single NiCd or NiMH cell
- Smart charger minimizes recharge time and prevents overcharging battery
- Includes power-on reset, short circuit protection and thermal limiting
- SO-8 or 16-lead SO/SSOP packages with 3.3V or 5V monitor and reset

**www.linear-tech.com/go/LTC1558**

LTC1558: $3.15 ea. for 1K-piece Qty.

# Low Dropout Backup Regulator Provides Uninterruptible Output Voltage

Operating from two independent power inputs from 3.5V to 20V, the LT1579 produces a glitch-free output regardless of input voltages or sequencing.




**FEATURES:**

- Maintains continuous output voltage regulation with dual inputs - no protection diodes needed
- 300mA output with only 0.4V dropout
- Automatic or logic-controlled input switching
- 70µA quiescent current, 7µA in shutdown
- Adjustable and fixed 3V, 3.3V and 5V outputs
- Includes reverse battery protection, current limiting and reverse current protection
- SO-8 package with basic features
- 16-lead SO/SSOP packages include low battery comparators and extra logic control

**www.linear-tech.com/go/LT1579**

LT1579: $3.40 ea. for 1K-piece Qty.

For more details, contact Linear Technology Corporation,
1630 McCarthy Blvd., Milpitas, CA 95035-7417, Web Site: www.linear-tech.com.
(408) 432-1900. Fax: (408) 434-0507. For literature only: 1-800-4-LINEAR.

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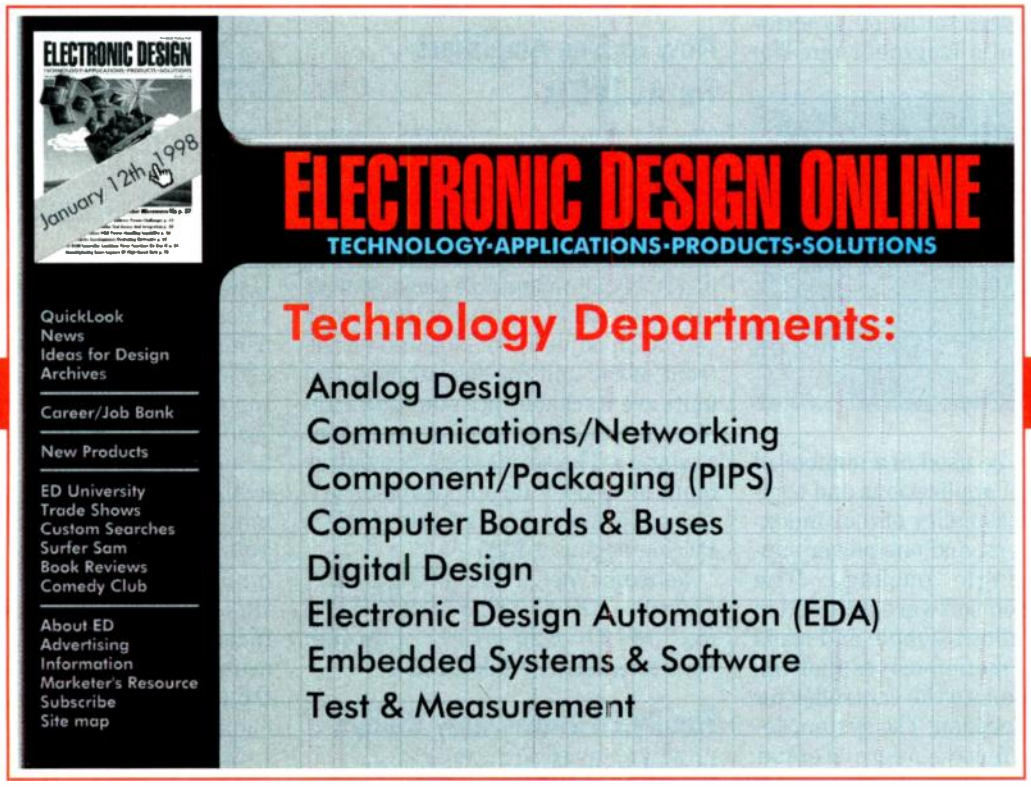



**www.elecdesign.com**

# Turn-Key Motion-Control Package Takes Guesswork Out Of Compatibility Issues

Available off the shelf, the AXI-PAK servo axis package is a complete turn-key motion-control package that uses pre-engineered, pre-matched components. The system comprises a high-torque BLX brushless servo motor with IP65 sealing, a Thomson Omnidrive digital servo drive, molded cables, and Omnilink setup software. Designed to take the guesswork out of compatibility and installation issues, the system also comes with UL, CUL, and CE certifications.

Key features of the system include the ability to operate in torque, velocity, or position modes; the ability to accept the standard ±10-V analog command signal from either a host computer or a serial link; and programmable I/O and preset speeds. The system also is available in an indexing version that can execute up to eight different position moves initiated by the digital I/O.

Other features include a continuous torque rating from 4.2 to 280 in.-lb., a peak torque rating of 11.0 to 840 in.-lb., MS-style fluid-tight connectors, oversize bearings, a winding thermal switch and an internal line-commutating encoder. The system can operate as a smart, standalone drive, or it can connect to the Thomson TMC-2000 motion controller for complex or multi-axis systems. Pricing is $1500.

***Thomson Industries Inc.***
*2 Channel Dr.*
*Port Washington, NY 11050*
*Sales Dept. (516) 883-8000*
*Fax (516) 883-9039*
**CIRCLE 532**
**PATRICK MANNION**

## Motion Controller Fits A Wide Range Of Uses

The MCL-400 multi-axis controller is the latest addition to the MCL series from Continuum Engineering. The

controller can be used in a number of motion control applications and combines the functionality of four indexers, four drivers, and one power supply in a single package. The Windows-based software included in the package allows simple and rapid generation of motion moves that can be downloaded into the controller for standalone operation. The system delivers cost-effective micro-stepper control performance. Base price for the MCL-400 four-axis indexer/driver is $3825.

***Continuum Engineering Inc.,*** *18740 Oxnard St., Tarzana, CA 91356;(818) 654-8950; fax (818) 654-8955; e-mail: sarfati@ceusa.com.* **CIRCLE 533**

## New In-Line Amplifiers For AC LVDTs

The DLD In-Line Amplifier series from Sensotec is designed for ac LVDTs and features two models to address linear displacement application needs. The amplifiers are housed in a DIN-rail-mountable package with all electrical connections and zero/span adjustments located on the front of the unit for easy access. The units are stackable on a standard DIN 35-mm mounting rail for ease of installation. The series accepts a power input of 18-36-V dc and provides 3-V ac excitation at 5 kHz to the LVDT. Pricing begins at $325.

***Sensotec Inc.,*** *2080 Arlingate Ln., Columbus, OH 43228;(614) 850-5000; fax (614) 850-1111; Internet: www.sensotec.com.* **CIRCLE 534**

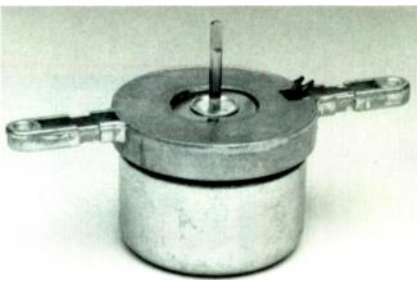
## Family Of Time-Delay Relays Includes A Motion Detector

The DMC-2000 series of motion controllers from Galil Motion Control Inc. are now available for the Universal Serial Bus (USB.) They are available in 1- through 8-axis formats which enable control of both step and servo motors on any combination of axes. Performance features include sinusoidal commutation for brushless motors, two encoder inputs for each axis, 96 configurable I/O, and forward and reverse limits and home inputs for each axis. Modes of motion include independent axis positioning, linear and circular interpolation, contouring, electronic gearing, and ecam. Pricing is $2995 for a single four-axis controller, and $1295 each for quantities of 100.

***Galil Motion Control Inc.,*** *203 Ravendale Dr., Mountain View, CA 94043;(800) 377-6329; fax (650) 967-1751; www.galilmc.com.* **CIRCLE 535**

## Brushless DC Motor Features Ball Bearing Motor Design

The DE19 Brushless DC (BLDC) motor from Comair Rotron features a ball bearing motor design for high performance, reliability, and long life.



Used in pumps and air-moving devices, the DE19's core includes a dynamically balanced rotor that ensures efficient operation, high starting torque, and minimal torque ripple. Two-wire control allows quick connection to dc power. The motor is available in 2800-rpm models with a minimum start torque of 0.25 in.-oz. and 3600-rpm models with a minimum start torque of 0.3 in.-oz. Options such as performance sensors, tachometers, and clockwise rotation are available. Prices start at $17 in OEM quantities with delivery in eight weeks.

***Comair Rotron,*** *2675 Customhouse Ct., San Ysidro, CA 92173; (619) 661-6688; fax (619) 661-6057; Internet: www.comairrotron.com.* **CIRCLE 536**

# Shake, Rattle, & Roll!

## Our Seismic Cabinet Rack can take it!

- Meets latest Bellcore Zone 4 Testing Specs.
- Certified for 400 lb. Inside Equipment Load.
- 100 lb. Top Cable Load.
- Features Integral Panel Mounting Rails.
- Panel Space: 19" x 70" with Clear Inside Depth of 29.75"
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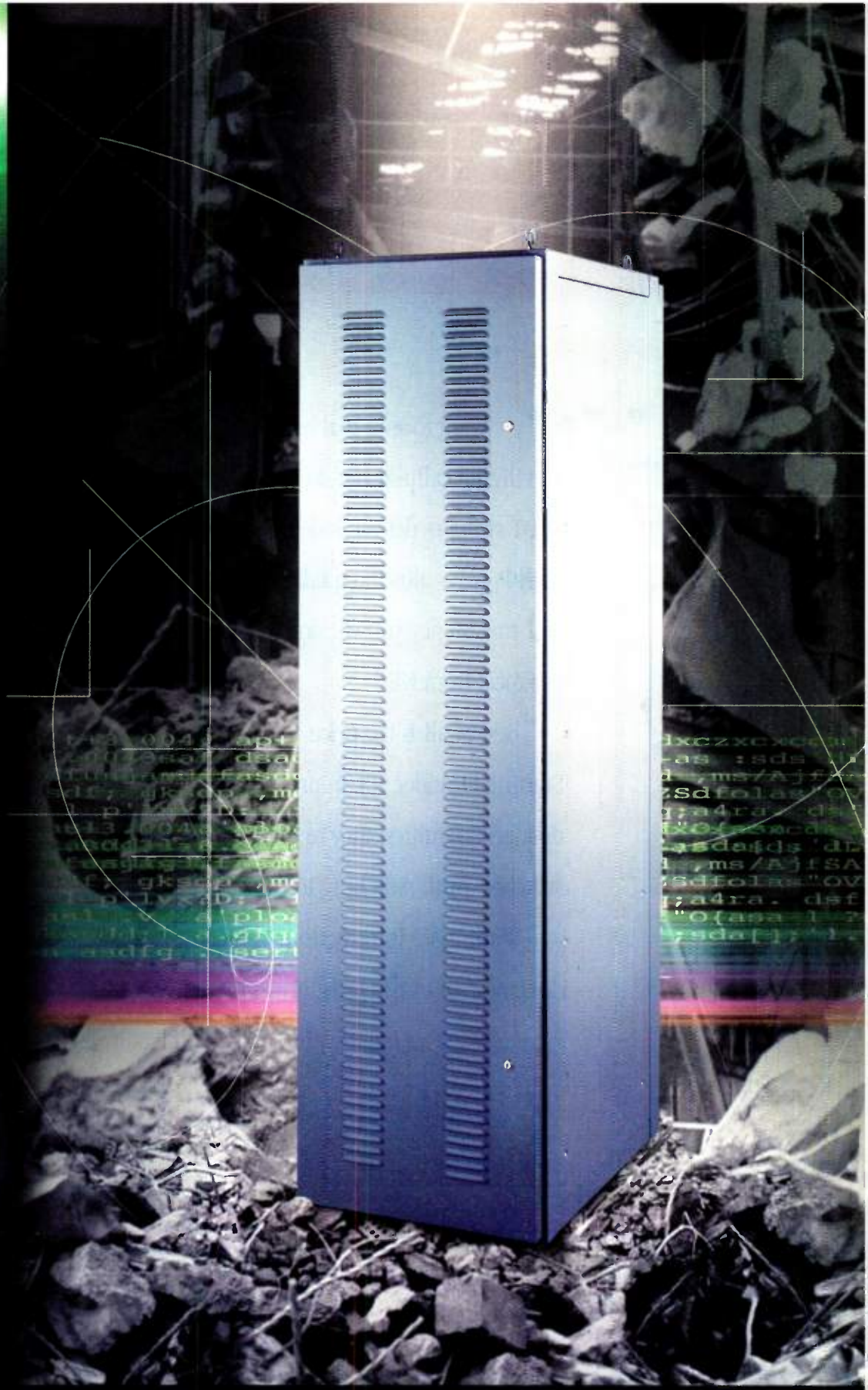

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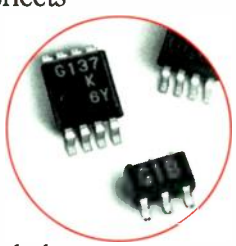

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# A Look At Software Radios: Are They Fact Or Fiction?

*Fully Programmable, DSP-Based Radios And Cell Phones Are The Future, But When? Here's An Insider's View On Theory Vs. Practice.*

**BRAD BRANNON, DIMITRIOS EFSTATHIOU, and TOM GRATZEK,** Analog Devices Inc., 7910 Triad Center Dr., Greensboro, NC 27409; e-mail: Brad.Brannon@analog.com.

Software radio is a buzzword that's been around for many years, with deep roots in the military. These were "be all and do all" receivers, the workhorses of military intelligence.[1,2] As the cold war melted, software-radio enthusiasts found a new home for their technology: cellular-radio applications.[3] This article reviews the concept, architecture, technology challenges, and economics of the software-defined radio.

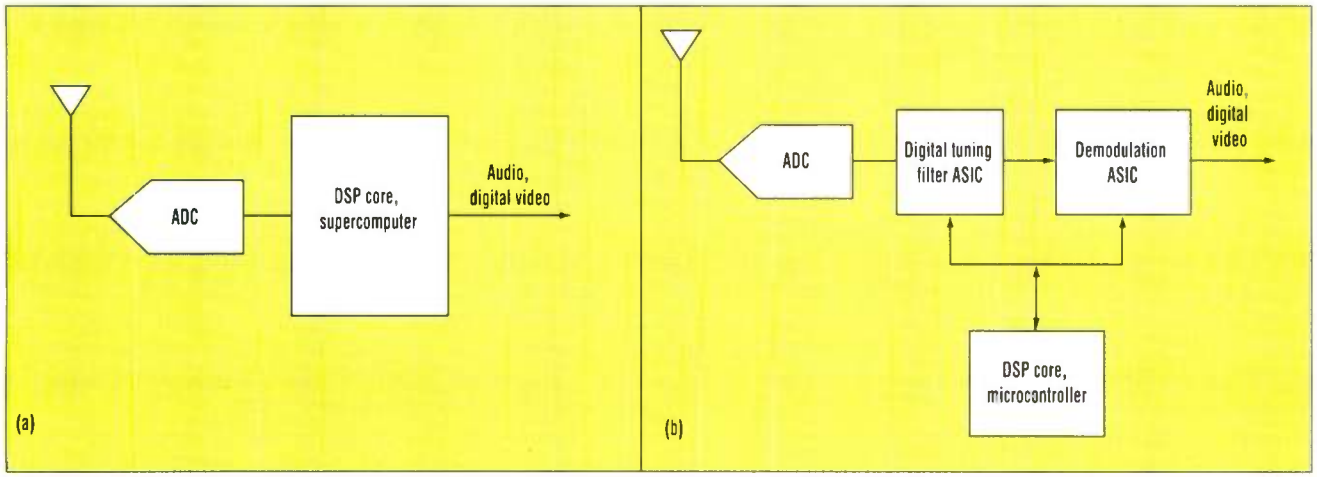
Historically, the relatively low number of prevalent standards, as well as the state of the art and high cost of key components, have limited the benefits and use of software radios. The second generation of wireless systems has offered a variety of different modulation formats and multiple-access technologies to be covered by a single radio.

Dual-mode operation and compatibility requirements with analog systems make this task even more challenging. The main goal of current developments in dual-mode (and eventually triple-mode) transceivers, which cover drastically different data rates and modulation formats, is often reduction of cost, power, and size.[4]

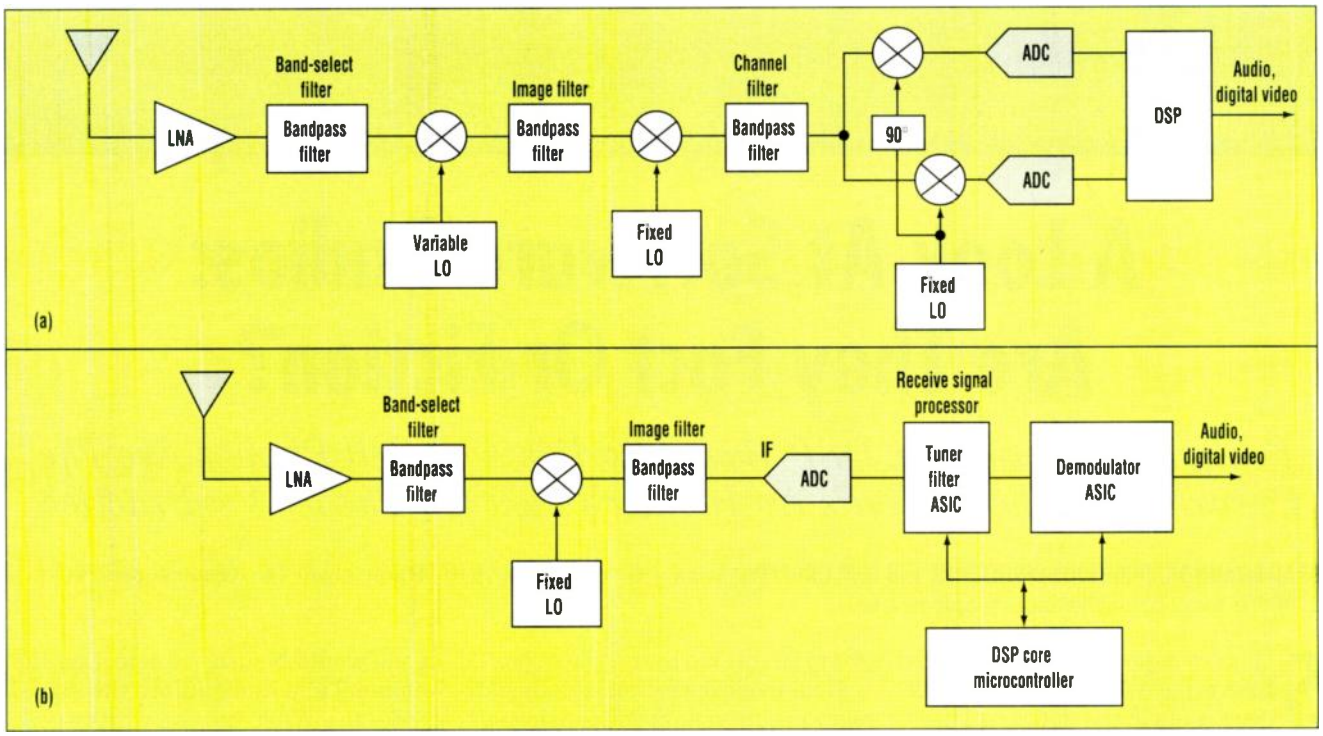
## Defining Software Radio

The most literal translation of software radio would be a radio where signals on the antenna, or perhaps at an intermediate frequency, are digitized with a high-performance analog-to-digital converter (ADC) and sent to a terminal (computer, mobile phone, etc.). Once digitized and inside the terminal, code would be used to select an RF channel and demodulate the signal *(Fig. 1a)*. While this is a worthy goal, it's only now becoming practical for specific applications.

A more reasonable name for this desired technology would be a "digital reprogrammable radio." (Note that digital receivers can be designed to receive digitally modulated signals, as well as analog, or FM, signals.) As with a software radio, an ADC is used to digitize the signal at the antenna or at an intermediate frequency. Instead of processing the digitized data solely in software, however, a variety of flexible, reconfigurable ASICs and general-purpose digital signal processors (DSPs) are used to reduce system power dissipation, size, and cost *(Fig. 1b)*. These ASICs




**1. In the "ideal" software radio, RF signals are digitized directly at the antenna (a). All other radio functions are performed in the digital domain via software. With a digital programmable radio, some of the digital processing is accomplished with specialized reconfigurable hardware (b).**




**2. In early digital radios, signals were sampled at the baseband frequencies. This was due to ADC performance limitations which restricted the highest frequencies that could be sampled (a). Improvements in ADC performance allowed sampling at the IF (b).**

are programmable and can be adjusted for different channel characteristics and modulation schemes. These implementations, which include ASICs or field-programmable gate arrays (FPGAs), are more economical than fully flexible DSP implementations.[5]

A practical definition of software radio includes radios with a set of predefined hardware modules (such as ASICs or FPGAs). These modules must be selectable through software as common hardware for several different systems.

These modules provide multirate signal-processing functions (like decimators and interpolators), digital down/up conversion capabilities, and filter programmability via RAM-coefficient, finite-impulse-response (FIR) filters. This approach enables the efficient realization of transceiver functions in terms of power consumption, minimal component count, and compactness. In effect, the filters and demodulation that would have run on the terminal have been generalized and committed to silicon with programmable characteristics.

Thus, a software radio that's practical for today is one where selected functions have been committed to silicon. But, enough flexibility must be retained in order to reconfigure it for a variety of different standards.

## What Technology Is Needed?

In recent years, there's been significant improvement in critical technologies such as low-noise amplifiers (LNAs), mixers, data conversion, and DSPs. Only now do these enhancements make "software radios" possible.

Whether sampled at the antenna or at an intermediate frequency (IF), the signal must still be sampled with an analog-to-digital converter (ADC). In the case of the military archetype *(Fig. 1a, again)*, the usual specification was for a 16-bit, 1-GHz sampler. Needless to say, if such a converter ever existed, it was quite expensive. Although advances have been made in RF-bandpass sigma-delta converters, a much more practical solution is to sample at an IF frequency.

A key breakthrough in the commercialization of software radios has been to limit the bandwidth of the receiver. The personal communications services (PCS) and cellular industries have done this through the licenses granted to operators (typically under 15 MHz per operator). Technically, this means that as long as the band of interest has bounds, images and other spurious signals can be managed and placed out of band. When applied to software radio, a defined bandwidth means that a system's sample rate and dynamic range can be reasonably limited.

This means that the IFs able to be selected also can be directly sampled with current ADC technology. Five years ago, data converters required that the RF signal be converted to baseband. Present technology allows the sampling of IF signals up to 250 MHz. An added benefit of IF sampling is that one or more downconvert stages can be eliminated. This results in very small receiver designs and, thereby, reduced cost.

Figure 2a shows a baseband-sampling receiver. This is a triple downconvert to near baseband with analog channel filtering. The final downconvert incorporates an IQ separation feeding separate baseband ADCs. The ADC datastream goes to the DSP, where demodulation is done in software. In addition to the RF band-select filter on the front end of this receiver, a channel-select filter is implemented in the analog domain.

Although the software could be altered to support a different air interface, the channel characteristics cannot be changed since the bandwidth of the

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analog filters is fixed. Certainly, different analog filters could be switched in and out. But often, these filters are quite expensive and add complexity.

Figure 2b depicts a similar IF sampling receiver. In this case, a single analog mixer is used to downconvert to a convenient IF where the signal is digitized. I and Q separation is done digitally in the receive-signal-processor (RSP) chip, along with channel-filter and data-rate selection. In this instance, the DSP is only used for demodulation and the receiver is fully programmable. Both the channel characteristics and demodulation methodology can be changed. In a narrow sense, software radios as presented here are "future proof" in that they permit incremental channel or standards changes with little or no impact on the hardware. Since this architecture lends itself well to IF sampling, such receivers are both smaller and cheaper.[6]

## Bridging The 2G/3G Gap

Development of multicarrier, second-generation picocell and microcell base stations has become practical, thanks to progress in fully digital modem techniques. These techniques including synchronization, equalization, and multirate signal processing. In a multicarrier base-transceiver-station (BTS) receiver, the constituent RF and bearer channels are only treated as individual signals once they've entered the digital domain. This permits the radio to be independent of modulation, access methodology, and channel spacing.

An efficient hardware design takes advantage of digital algorithmic approaches. And, with proper architectural partitioning, it also makes software-radio communications products practical. The flexibility of software-radio-based solutions enables the migration to third-generation system designs. Software-radio techniques also can provide a seamless evolutionary path from the second- to third-generation systems, thereby reducing network operators' future capital costs.

## ADC And DAC Limitations

In typical base-station implementations, a wideband ADC may convert an entire system band at the IF (extended GSM = 35 MHz, IS-136 = 25 MHz, IS-95 = 25 MHz). This allows digital channelization and demodulation.

From a software-radio point of view, there are engineering limits related to data-converter technology and ASIC reprogrammable functions. These include the bandwidth and dynamic range of the ADCs and DACs, as well as the processing capacity of the digital-processing hardware, including reprogrammable ASICs, FPGAs, DSP chips, and general-purpose processors.

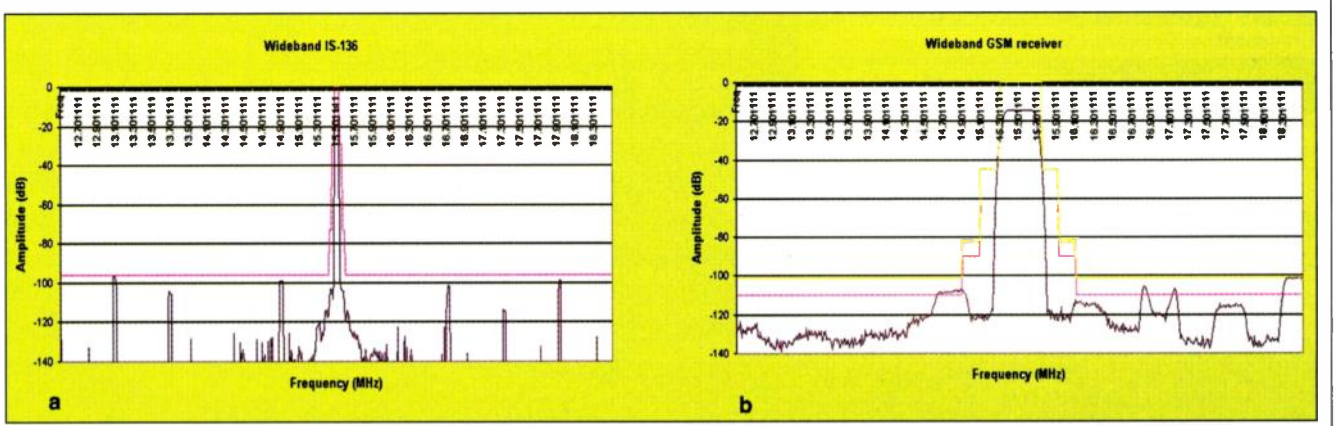
ADCs, in particular, have always been seen as key components of signal-processing systems. They often dictate system architectures due to their limitations on sampling rate, resolution, and dynamic range. Over the last decade, most ADC research has been aimed at monolithic, power-efficient ADCs, rather than high-performance, high-power converters.

Over the last few years, however, the maturation of monolithic converter technology has returned the focus to high performance. High-speed DACs have been considered easier to implement when compared to high-speed ADCs. DAC specifications have been reviewed in the light of wideband, multicarrier transmission requirements where high-speed DACs should operate at medium-to-high IFs. Wider, dynamic-range DACs are needed for multitone applications, which transmit many channels of information over several MHz of bandwidth and have a high peak-to-average output-signal ratio.

The illustrations that follow provide insight into the capabilities of current ADC technology. While some air interfaces can't yet take advantage of wideband sampling, converter technology has matured to the point where many popular standards can now be handled. Notable standards potentially implementing this technology are PHS, PDC, IS-136, AMPS, and GSM picocells. The remainder of current standards will be implemented shortly, when next-generation converters become available.

The graphs shown in figure 3 illustrate the spurious response from a prototyped receiver which uses the architecture shown in Figure 2b. This receiver was programmed to filter an IS-136 channel *(Fig. 3a)*, then reprogrammed to filter a Groupe Speciale Mobile (GSM) channel *(Fig. 3b)*. In each case, the RSP was tuned across the band to illustrate receiver performance. These figures show blocker rejection, along with the performance required by the standard.

One key reason that the setup fails to meet minimum, standard-defined




**3. These spectral plots illustrate the typical wideband-receiver performance expected from current- generation data converters. One plot shows the spurious response when the receiver is programmed to filter an IS-136 channel (a). The other plot depicts the receiver's performance when reprogrammed for a GSM channel (b).**

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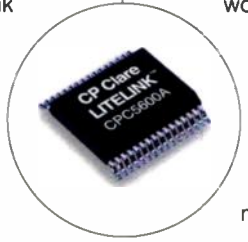


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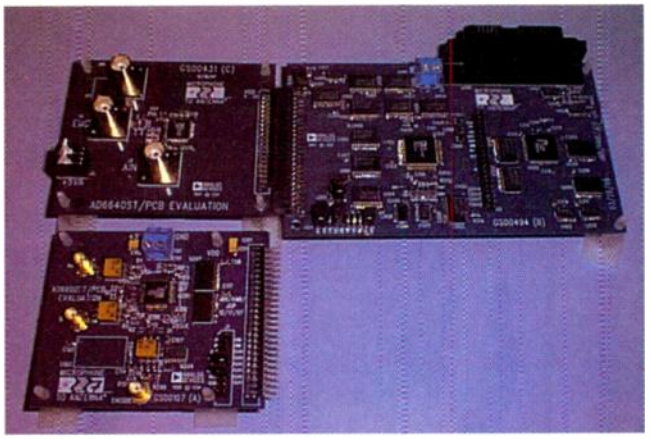
performance levels is the limitation in the spurious performance of the ADC. Current ADC technology provides about 80 dB of dynamic range without dither. The converter used in this case is an IF-sampling ADC (AD6640). Standard vendor-supplied evaluation boards are used *(Fig. 4)*. If dither techniques are utilized, spurious performance will be improved from 15 to 20db to 100 dB.[7]



**4. Vendor-supplied modular evaluation boards simplify the prototyping of digital receivers. The AD6640-based unit depicted here was used to generate the spectral plots of Figure 3.**

## DSP Limitation Factors

Software-radio solutions set the demand for high-speed components for IF and baseband processing. Third-generation architectures will require 1000 MIPS of digital-IF processing power, and up to 2000 MIPS of baseband DSP power. Some functions of a wideband code-division multiple access (W-CDMA), third-generation technology receiver system, such as matched filtering and despreading, are computationally intense. They'll probably be implemented as dedicated ASICs, or at least hardware accelerators within a DSP core.

The peak computational demand of a software radio for a 4.096-MHz W-CDMA mode is about 400 MIPS per finger, or 1600 MIPS. An FPGA or DSP-core based ASIC could more easily deliver the required computational capacity today. The software-radio DSP could be reprogrammed for GSM, IS-136, or IS-95. Advanced decision-/data-directed or nondecision-directed techniques can be implemented within a DSP for time-division multiple-access (TDMA) receivers.[8]

The DSP industry is currently undergoing a generational change driven by three factors: architectural innovation, process technology, and system integration. Architecturally, DSPs have to improve their performance by means of higher levels of parallelism and incorporating multiple data paths and execution units. Process technology remains the primary driver of performance by increasing clock rates and transistor counts. At the same time, DSP power consumption should decrease. DSPs with drawn geometries of 0.35-µm in the 1995 to 1996 timeframe are now being delivered in 0.25-µm, with 0.18-µm expected in late 1999.

A software radio could offer more flexibility by realizing multimode and multiband radio. It could present "on-the-fly" specification change and additional functions and/or services. It also could offer autonomous selection of air-interface standards according to environments (home, office, outdoor, vehicle) and user needs (voice, data, audio).

The driver for the development of software-radio base stations is likely to be the introduction of third-generation systems. But, huge investments are needed for first- and second-generation wireless systems. These make it unattractive—at least for the present time—for operators to consider a software-radio network deployment in the near future.

We can expect, then, that worldwide base-station and handset manufacturers see the software radio as a remote opportunity (a technological vision) and will focus on a commercially viable version of it. This pragmatic approach results in the digital programmable radio, which bridges the gap between second- and third-generation systems. We can also predict the acceleration of the development of software-radio architectures. The market discontinuity, represented by third-generation systems, will create a demand in the same way GSM did for real-time DSP in the late 1980s and early 1990s.

References:

1. Mitola, J., "The Software Radio," *Proceedings of the IEEE National Telesystems Conference*, Feb. 1998, Boston, Mass.

2. Lackey and Upmall, "SPEAKeasy: The Military Software Radio," *IEEE Communications Magazine*, May 1995, pp. 56-61.

3. Gratzek, T., "Software Radios for Cellular/PCS Base Stations: Fact or Fiction," *Proceedings of the 1998 International Symposium on Advanced Radio Technologies*, Sept. 1998, Boulder, Colo.

4. *Proceedings of First International Workshop on Software Radios*, June 1998, Rhodes, Greece.

5. Efstathiou, D., Zvonar, Z., "Transmitter and Receiver Design for Software Radio Base Stations: Enabling Technologies and Components," *Proceedings of 3rd ACTS Mobile Communications Summit '98*, June 1998, Rhodes, Greece.

6. Brannon, B., "Wide-Dynamic Range A/D Converters Pave the Way for Wideband Digital Radio Receivers," *EDN*, Nov. 7, 1996, pp. 187-205.

7. Brannon, B., "Overcoming Converter Non-Linearities with Dither," Analog Devices Application Note, number AN-410.

8. Efstathiou, D., Aghvami, A. H., "Preamble-less Non-Decision-Aided (NDA) Feed-forward Synchronisation Techniques for 16-QAM TDMA Demodulators," *IEEE Transactions on Vehicular Technology*, Vol. 47, No. 2, May 1998, pp. 673-685.

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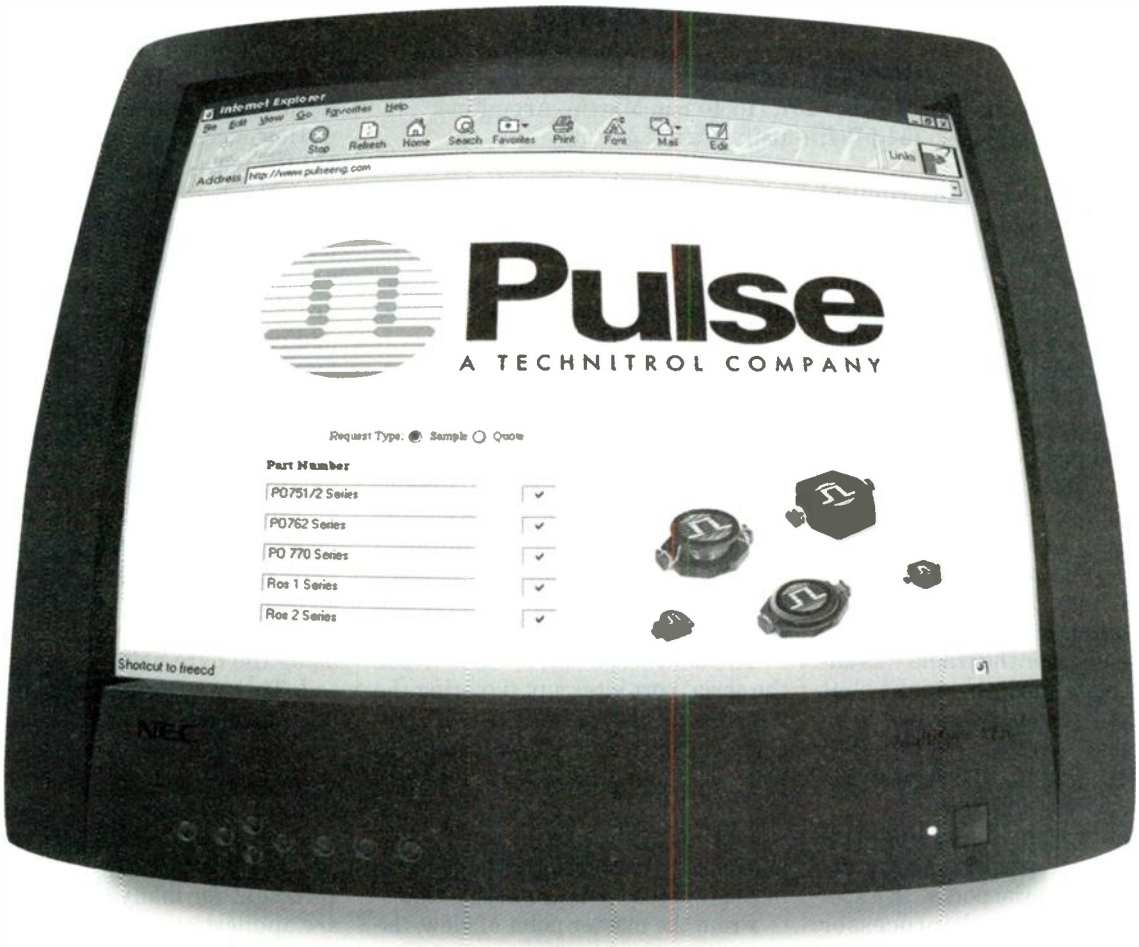


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# Use The PC's UART With 9-Bit Protocols

**ALEJANDRO J. FORMICHELLI**
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A typical system for distributed monitoring and/or control consists of a multidrop network—a PC acts as the host and communicates with 8-bit microcontrollers acting as slaves *(see the figure)*. Usually, the physical layer of such a network is based on the RS-485 standard, while the logical layer is a commercial or user-defined protocol. In either case there's an address byte within the transmitted frame that identifies the target slave device.

With early-generation microcontrollers, all slaves had to search for this address byte within the frame to determine whether the frame was addressed to them. This meant that every slave in the network had to be interrupted by every byte being transmitted, wasting the slaves' precious CPU processing time.

Later microcontrollers, like Motorola's 68HC05C8 or Intel's 8051, implemented their serial port with a special mode for multiprocessor communications. In this mode, 9 bits are received. The 9th bit goes to a special register. The serial port can be configured to activate the serial-port interrupt, depending on the state (i.e., a logical one) of the 9th bit.

When the master wants to transmit a block of data to one of several slaves, it first sends out an address byte that identifies the target slave. An address byte has its 9th bit set, while a data byte has it cleared. Because of this bit state, the address byte will interrupt all slaves. Each one examines the received byte and see if it's being addressed.

The addressed slave will activate the serial port interrupt (ignoring the 9th bit state of successive bytes) to receive the data following the address byte. The non-addressed slaves will continue with their program, ignoring the incoming data bytes until a new address byte interrupts them, minimizing wasted CPU processing time.

From the master point of view, the main problem with this addressing method is that the PC UART (originally 8250-based and now 16x50-based) doesn't have the newer 9-bit word capability. It would be necessary to add hardware to the PC, such as another microcontroller to handle communications with the slaves or a UART with 9-bit communciations mode (e.g., Intel's 82521).

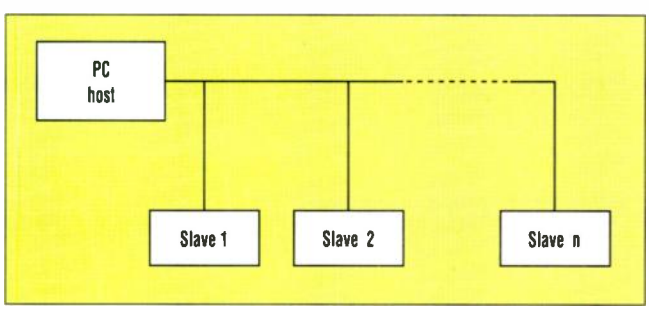
However, it's possible to use the PC UART with 9-bit protocols without any extra hardware. The trick is to use the parity bit as the 9th bit. Suppose we want to send a string, such as "ABC," to the slave processor at address 41h and that we've established odd parity for communications. The frame to be transmitted would look like that shown in the table.

The 8th bit is used to change the quantity of "ones" in the byte, causing the parity (9th) bit to be set properly to meet the parity used. This can be accomplished rather easily using two lookup tables: one for the byte as an address byte and one for the byte as a data byte. The table is indexed using the byte value to be transmitted. This way, any byte can behave both as an address byte or as a data byte (like 41h and "A").

Due to the use of the 8th bit, this method limits the data byte length to 7 bits (i.e., standard ASCII) and slave addressing to 128 slaves. While this is sufficient for many networks, there are applications (code downloading,

**FRAME TRANSMISSION FOR 9TH BIT**

| parity (9th bit) | 8th bit | address/data | |
|---|---|---|---|
| 1 | 0 | 1000001 | slave #41h address |
| 0 | 1 | 1000001 | data byte - 'A' |
| 0 | 1 | 1000010 | data byte - 'B' |
| 0 | 0 | 1000011 | data byte - 'C' |



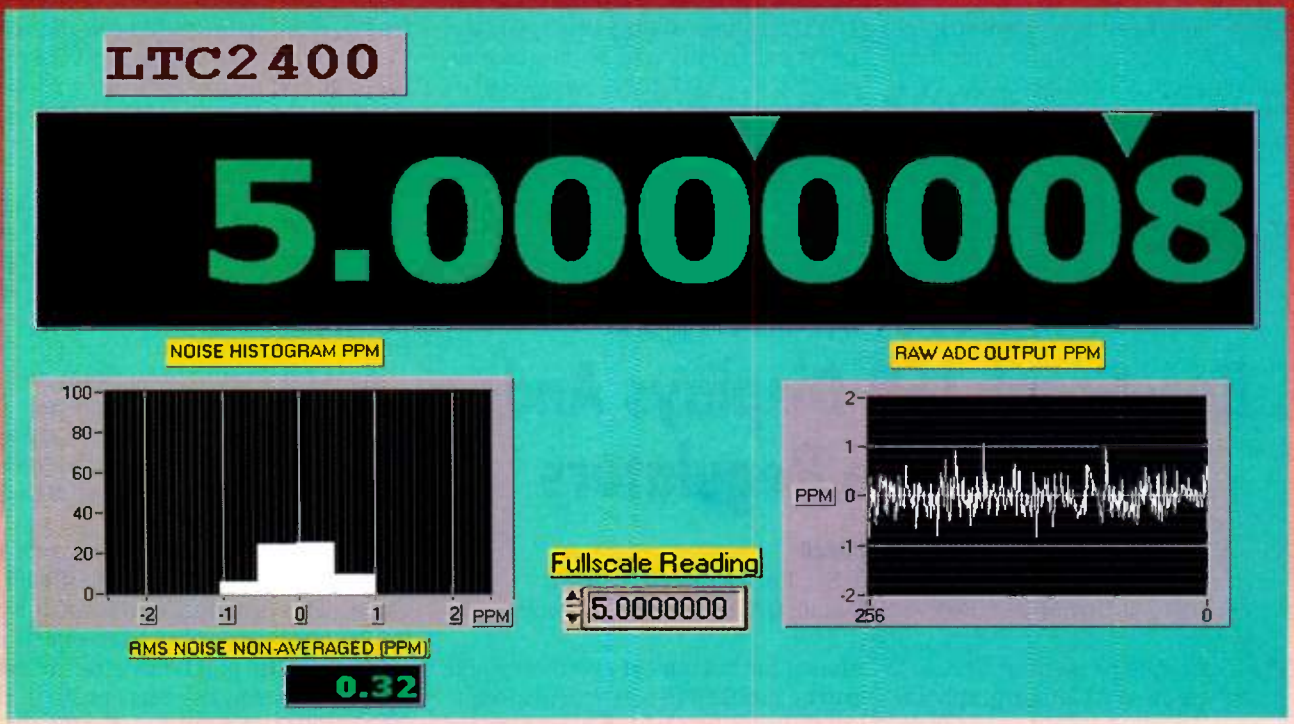

**In this typical multidrop microcontroller network, the PC acts as the host and communicates with 8-bit microcontrollers that are acting as slaves.**

```
// Use The PC's UART
// With 9-Bit Protocols
// Author: Alejandro J. Formichelli
//
SendFrame( char bfr[], int bfrLen )
{
   SetParity( bfr[0], ADDR );      // first byte of buffer is slave address
   SendByte( bfr[0] );

   for( i = 1; i < bfrLen; i++ ) {
      SetParity( bfr[i], DATA );
      SendByte( bfr[i] );
   }
}


SetParity( char byte, int byteType )
{
   if( byteType == ADDR )          // get the new register value
         regVal = addrTbl[byte]; // depending on the byte type
   else
         regVal = dataTbl[byte];
   while( inTx )                   // waits end of transmission of last byte,
         ;                         // before reconfiguring the UART
   WriteParityReg( regVal );       // reprogram the parity register
}
```

# 24-Bit ADC in SO-8

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- 5µV Offset
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- Reference Input Voltage: 0.1 to $V_{CC}$
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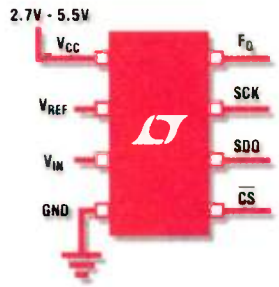
### LTC2400 Block Diagram

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sending a CRC, etc.) where 8-bit-length words are needed. The code listing shows two C-like pseudocode routines as an example of how to avoid this restriction.

The trick here is to reconfigure the UART parity before each byte transmission, according to the type of byte to transmit. If we send a frame to slave #E9h (decimal 233, binary 11101001) the *SetParity()* function retreives the 233th element of "addrTbl". This is the value to be written in the parity register of the UART. Here, it will configure the UART to use even parity; so, the parity (9th) bit will be set to one, causing this byte to be recognized as an address byte.

Once the address byte is transmitted, the function looks up in "dataTbl" to find the parity register values that convert (9th bit cleared) the next bytes of the frame into data bytes. If byte E9h appears within the frame, SetParity() will reconfigure the UART to use odd parity. Therefore, the 9th (parity) bit will be cleared and, this time, the network will see it as a data byte.

---

Circle 521

# Recursive Circuit For Bar-Graph LED Displays And Shunt Voltage Regulators

**STEVEN DUNBAR**
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The example presented here is a four-element LED bar-graph display. The LEDs light up sequentially from left to right as the current (I) is increased. Because the circuit is entirely analog, the LEDs turn on gradually until the current limit for each stage is reached. Once the limit is reached, the next LED begins to turn on. A current source isn't strictly needed to drive the circuit; a voltage source with a series-limiting resistor will work just as well.

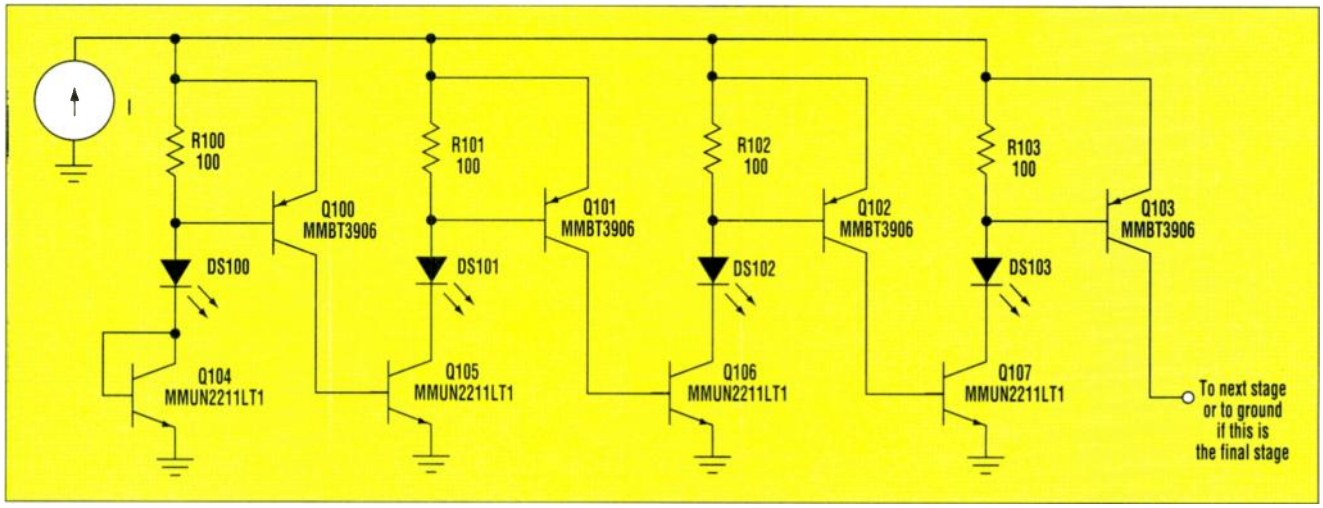
The npn transistor of the first stage (Q104) is connected as a diode. This is shown for reasons of symmetry and can be omitted in a practical circuit. As the current (I) increases, it flows through R100 and DS100, causing the LED to begin to glow. As the current increases, the LED intensifies. This continues until the voltage drop across R100 reaches about 0.65 V at room temperature. At this point, the base-emitter junction of Q100 becomes forward-biased, which turns on the second stage of the array.

As the current is further increased, the intensity of the first LED remains constant due to the current-limiting action of R100 and Q100. Additional current then flows through the second stage of the array and the intensity of the second LED increases until its current limit is reached.

As the current through the network continues to rise, this process is repeated for each successive stage in sequential order. There is no theoretical limit to the number of stages that can be connected.

The main design criterion for this circuit is the current limit of each stage. This is simply determined by the resistor across the base-emitter junction of the pnp transistor. In the example shown, the current limit is 0.65 V/100 Ω = 6.5 mA *(see the figure)*. Typically, all stages would be identical, but this isn't required. By using different current limits for each stage, some interesting functions are possible, such as a logarithmic bar-graph display. A logarithmic display also would include resistors to shunt excess current around the LEDs so that the full intensity of each LED would be the same.

One drawback of this simple design is that the current limits are a weak




**In addition to implementing both linear and nonlinear bar-graph displays, this circuit can alternatively be used in shunt-regulator applications.**

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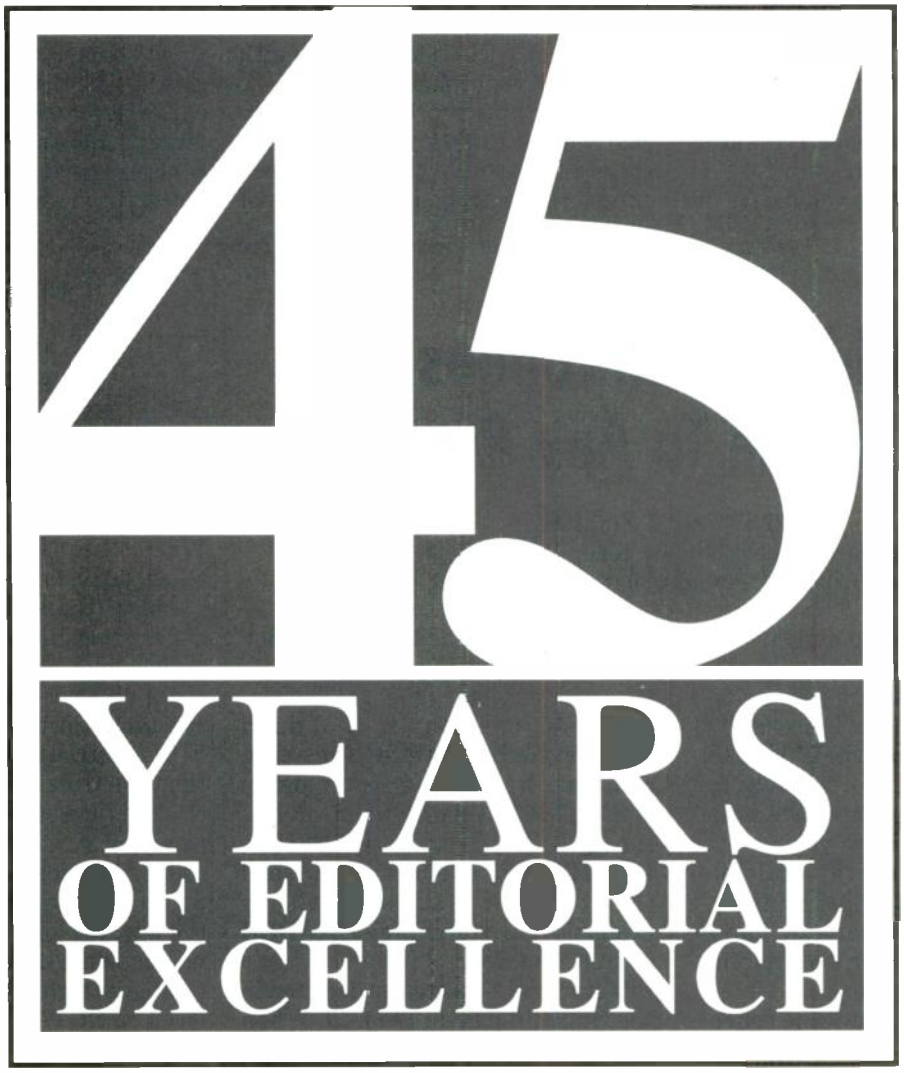


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function of temperature due to the nature of the pn junctions in the transistors. Series resistors aren't needed at the bases of the MMUN2211 devices because they contain internal resistive networks to serve the same purpose.

The usefulness of this circuit as a bar-graph LED display is already evident from the example. A side effect of the recursive stages is that they clamp the voltage appearing across all of the stages. In this regard, the circuit behaves as a shunt voltage regulator. The clamp voltage depends on the loads driven by the stages. If the loads are LEDs with a voltage of 1.6 V at 6.5-mA bias, the clamp voltage for the network will be approximately 2.9 V. In the example, this is the sum of the voltages across Q104 (connected as a diode), the LED, and the resistor.

Of course, shunt voltage regulators are extremely inefficient for most applications. However, they do possess a unique property that can be quite useful in certain circumstances. Shunt regulators are superb at dissipating excess energy from a source, such as when float-charging a lead-acid battery with an array of photovoltaic solar cells.

As the battery becomes fully charged, the excess energy from the solar cells would typically be consumed as electrolysis in the cells of the battery. This depletes the battery of electrolytes, eventually destroying it. A shunt regulator connected across the battery prevents excessive current from entering the battery, saving it from destruction.

The main advantage of this circuit compared to other shunt-regulator topologies is the ability to discern how much extra current is available from the source. In the aforementioned battery example, this circuit acts as a kind of fuel gauge that indicates the current battery-charge level. If more stages are on, less current is entering the battery and the battery is in a higher state of charge.

Circle 522

# Add A Synchronous Clock Enable To Any Register

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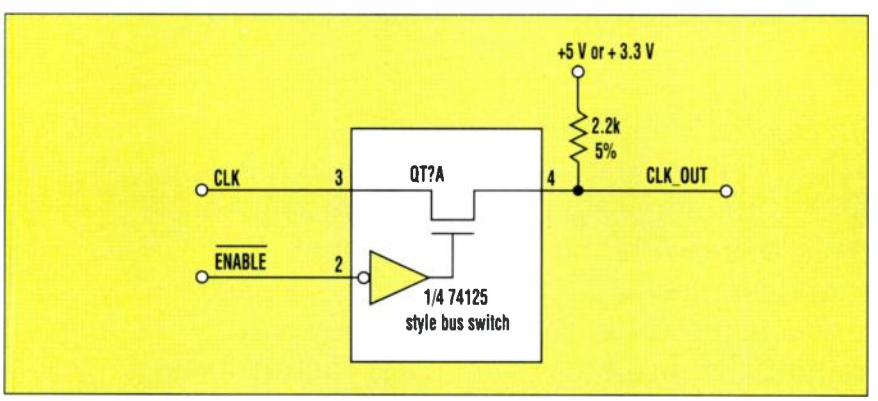
When designing synchronous digital systems with data paths, registers possessing a synchronous clock enable are needed. Use of standard off-the-shelf parts also is required. Unfortunately, few of the standard registers have a clock enable capability. However, by using only an inexpensive, multiple-sourced IC and a single resistor, a synchronous clock enable can be added to any register with minimal effects on system timing.

The schematic shows the connections required to add a synchronous $\overline{\text{ENABLE}}$ input to a positive-edge-triggered register *(Fig. 1)*. The circuit uses one-fourth of a quad 74125-style bus switch. These are available from Texas Instruments (74CBT3125), Quality Semiconductor (QS3125), Pericom (PI5C3125), IDT (IDT74FST3125), and Fairchild (FST3125). A 74126 style also is available if an active high ENABLE input is required.

The circuit operates as depicted in the timing diagram *(Fig. 2)*. When $\overline{\text{ENABLE}}$ isn't asserted, there's no connection between CLK and CLK_OUT, and the resistor pulls CLK_OUT high. $T_{CO}$ after CLK goes high, $\overline{\text{ENABLE}}$ is asserted. Then $T_{EN}$ after $\overline{\text{ENABLE}}$ is asserted, the connection between CLK and CLK_OUT, via the 5-Ω resistance of the pass transistor, is established. When CLK then goes low, it drives CLK_OUT low. When CLK again goes high, CLK_OUT is driven high, and the register is clocked. The propagation delay added by the pass transistor depends solely on the RC time constant, which is less than 500 ps.




**1. Using only an inexpensive, multiple-sourced IC and a single resistor, a synchronous clock enable can be added to any register. The circuit can be easily adapted for 3V systems.**

The critical timing parameters are the time from the rising edge of the clock to the enable/disable of the connection from CLK to CLK_OUT. The connection must be enabled by $T_H$ after CLK goes high to avoid distorting the low time of CLK_OUT. The connection must be disabled by $T_H$ after CLK goes high to avoid a second pulse on CLK_OUT. The limiting factor is:

$$T_H >= MAX(T_{CO} + T_E,\ T_C + T_{DIS})$$

A typical bus switch has a worst case enable/disable time of 5 ns. Assuming a 50% CLK duty cycle and a $T_{CO}$ of 5 ns, a clock rate of up to 50 MHz can be supported.

In actual implementations, there are several caveats. The connection between the bus switch's output and the CLK input to the register should be as short as possible. Although the CLK_OUT is driven high by CLK, when the switch turns off, it's only driven by the pull-up resistor. For a

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DESIGN NOTES

# Get 100dB Stopband Attenuation with the LTC1562 Universal Filter Family – Design Note 195

Max W. Hauser

The LTC®1562 and LTC1562-2 are compact, high performance, "universal" continuous-time filter products, each containing four 2nd order Operational Filter™ blocks. These low noise, DC-accurate filters let you tailor their center frequencies ($f_0$) over a range of roughly 10kHz to 150kHz (LTC1562) or 20kHz to 300kHz (LTC1562-2) and replace several precision capacitors, resistors and op amps. All frequency-setting components are internal and trimmed, except for one resistor per block, which is desensitized (1% error in this external resistor's value contributes only 0.5% error to the programmed $f_0$). Additional components program each block's Q and gain. A complete application circuit using either the LTC1562 or LTC1562-2 on a surface mount board is about the size of a dime (155mm²).

Figure 1 shows one block, or 2nd order section (each LTC1562 contains four of these), with external resistors to set the standard 2nd order filter parameters $f_0$, Q and gain. In this example, the section is configured so that the two outputs give lowpass and bandpass responses.

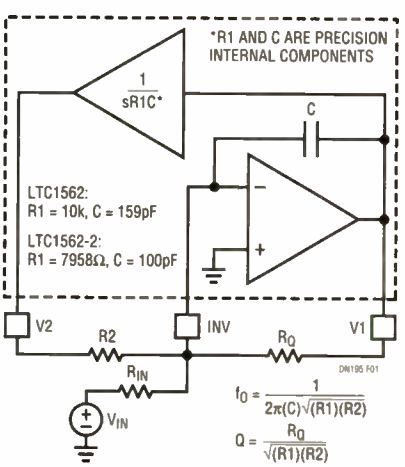



**Figure 1. An Operatonal Filter Block (Inside Dashed Line) Configured with External Resistors for Lowpass (at V2) and Bandpass (at V1) Responses. Each LTC1562 or LTC1562-2 Contains Four Such Blocks**

Cascades of Figure 1 circuits, with appropriate resistor values, can realize any all-pole lowpass or bandpass filter response form such as Chebyshev, Bessel or Butterworth. Adding external capacitors permits highpass forms. These filters can suppress undesired frequencies by 100dB while maintaining low noise and distortion.

Operational Filter blocks, however, have many more creative applications. Each block has a flexible virtual-ground input (INV) and two outputs, V1 and V2. V2 is a time integrated version of V1 and therefore lags V1 by 90° over a very wide range of frequencies. Parallel paths into the virtual-ground input or from the two different outputs permit transfer-function zeroes, of which one of the most useful is the imaginary-axis zero pair, or notch.

Figure 2 shows a simple and robust notch-filtering method. A notch filter has zero gain at some frequency $f_N$. Notch filters are useful not only to remove frequencies *per se* but also to improve selectivity in lowpass or highpass filters by placing notches in the stopband, as illustrated below. (Such responses are broadly called "elliptics" or "Cauers.")

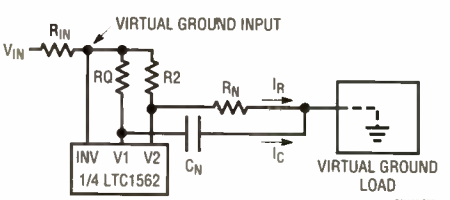



**Figure 2. Robust Notch Filtering Using a 1/4 LTC1562 Operational Filter Section. $R_N$ and $C_N$ Control Notch Frequency**

In Figure 2, a notch occurs when a 2nd order section drives a virtual-ground input through two paths: one through a capacitor and one through a resistor. The virtual ground can be an op amp input, or as in Figure 3, another Operational Filter input. Capacitor $C_N$ adds a further 90° to the 90° phase difference between the V1 and V2 voltages.

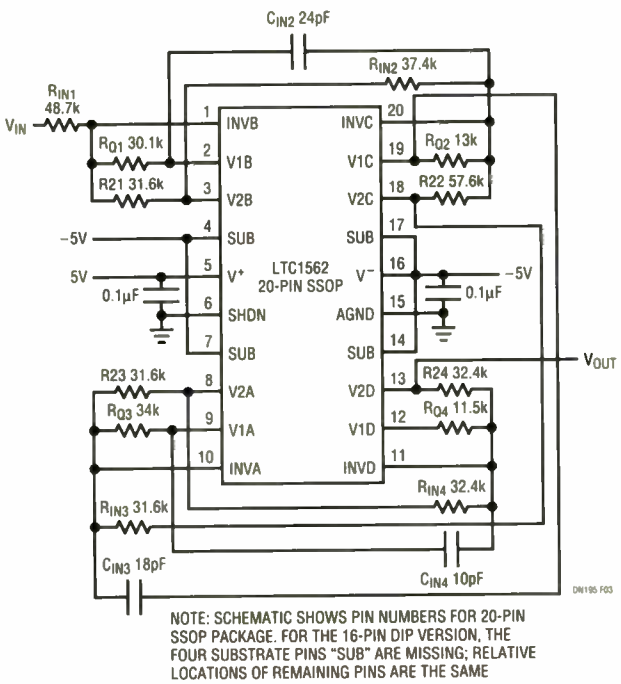
At the frequency where currents $I_C$ and $I_R$ have equal magnitude, the two paths cancel and a 2nd order notch occurs. This frequency is:

$$f_N = \sqrt{\frac{f1}{2\pi(R_N)(C_N)}}$$

Here, f1 is a parameter internally trimmed in each Operational Filter product (100kHz in the LTC1562, 200kHz in the LTC1562-2). The notch frequency, $f_N$, is independent of the center frequencies, $f_0$, programmed separately for each 2nd order section, as in Figure 1.

A remarkable feature of Figure 2 is its inherently deep notch response—the depth does not come from component matching as with other notch-filter circuits. Errors in $R_N$ or $C_N$ values change the notch frequency, $f_N$, but not the depth of the notch at $f_N$. Moreover, the square root dependence in the $f_N$ expression desensitizes the notch frequency to errors in the $R_N$ and $C_N$ values.

Figure 3 shows an 8-pole modified elliptic response 50kHz lowpass filter using the notch method of Figure 2. In this filter, three operational filter blocks ("B," "C" and "A" in the pinout, in sequence) drive RC combinations as in Figure 2, giving notches at approximately 133kHz, 167kHz and 222kHz, respectively. A 2nd order lowpass section, per Figure 1 with $f_0$ = 55.5kHz, follows (the "D" block in the pinout). Figure 4 shows measured frequency response, which falls 100dB in a little more than one octave. The choice of notch frequencies trades off passband flatness against stopband ripple; the user can explore this trade-off via analog filter design software such as FilterCAD™ for Windows®, available free from Linear Technology (1-800-4-LINEAR). The values in Figure 3 give stopband attenuations exceeding 100dB above 140kHz. This circuit has output noise (in 500kHz bandwidth) of 60μ$V_{RMS}$ with approximately rail-to-rail input and output swings, or a peak signal-to-noise ratio of 95dB when operating from ±5V supplies. THD is –95dB with 1$V_{RMS}$ (2.8$V_{P-P}$) output at 20kHz.




NOTE: SCHEMATIC SHOWS PIN NUMBERS FOR 20-PIN SSOP PACKAGE. FOR THE 16-PIN DIP VERSION, THE FOUR SUBSTRATE PINS "SUB" ARE MISSING; RELATIVE LOCATIONS OF REMAINING PINS ARE THE SAME

**Figure 3. LTC1562 50kHz Elliptic Lowpass Filter with 100dB Stopband Rejection**

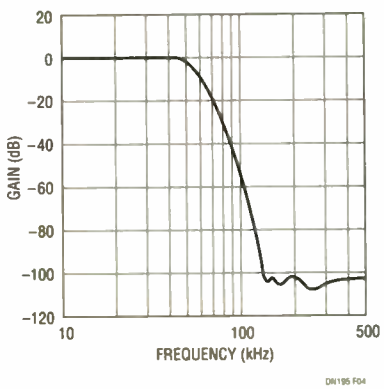



**Figure 4. Measured Frequency Response for Figure 3**

Note that 100dB attenuation at hundreds of kilohertz requires electrically clean, compact construction, with good grounding and supply decoupling, and minimal parasitic capacitances in critical paths (such as the INV inputs). For example, 0.1μF capacitors near the LTC1562 provide adequate decoupling from a clean, low inductance power source. But several inches of wire (i.e., a few microhenrys of inductance) from the power supplies, unless decoupled by substantial (≥10μF) capacitance near the chip, can cause a high-Q LC resonance (at hundreds of kHz) in the LTC1562's supplies or ground reference, impairing SNR and stopband rejection at those frequencies.



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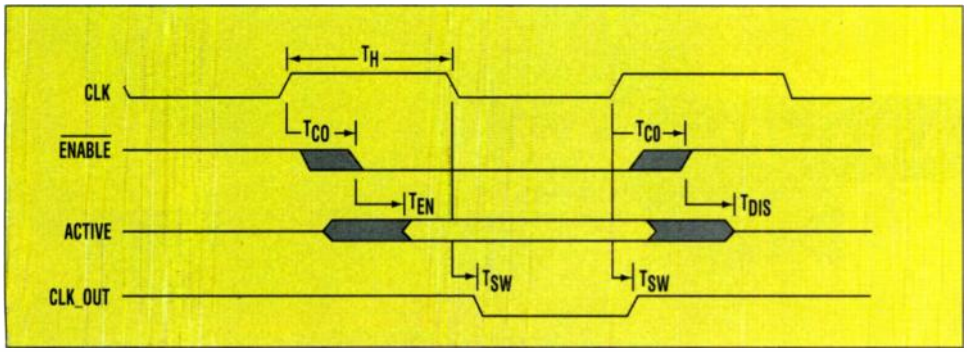


**2. The additional propagation delay, $T_{SW}$, added by the pass transistor in the 74125 IC, depends solely on the RC time constant. This delay is typically less than 500 ps.**

long CLK_OUT trace, transmission line effects can cause ringing on the low-to-high edge due to the relatively high impedance of the pull-up resistor. Short traces, such as those required to tie both CLK inputs on a 16-bit-wide device to the same CLK_OUT, aren't a problem.

Because a bus switch is essentially a controllable wire, it has the effect of changing the loading on the CLK line whenever $\overline{\text{ENABLE}}$ is asserted. This must be considered when looking at the transmission-line effects on the CLK signal. In some cases, this "problem" can actually be an advantage. When several registers are connected to the same clock signal and only one of the registers is enabled at a time, the clock loading is reduced by 1/N (where N is the number of registers).

The bus switch is powered by 5 V. The effective resistance of the pass transistor goes up well above 5 Ω for input voltages above about 3.5 V. The net effect on the CLK_OUT low-to-high transition is a quick rise to 3.5 V, driven by the CLK signal, followed by a slower rise from 3.5 to 5 V driven by the pull-up resistor. However, even at 3.5 V, the CLK_OUT signal still meets the 5-V TTL-level requirement of 2.4 V minimum output high voltage.

In 3.3-V systems, the same circuit can be used to switch a 3.3-V clock signals, as long as the CLK_OUT output signal is pulled up to 3.3 V instead of 5 V. In this case, there is no slow low-to-high transition on CLK_OUT. The $\overline{\text{ENABLE}}$ input can be driven with a 3.3-V TTL-level output if necessary.

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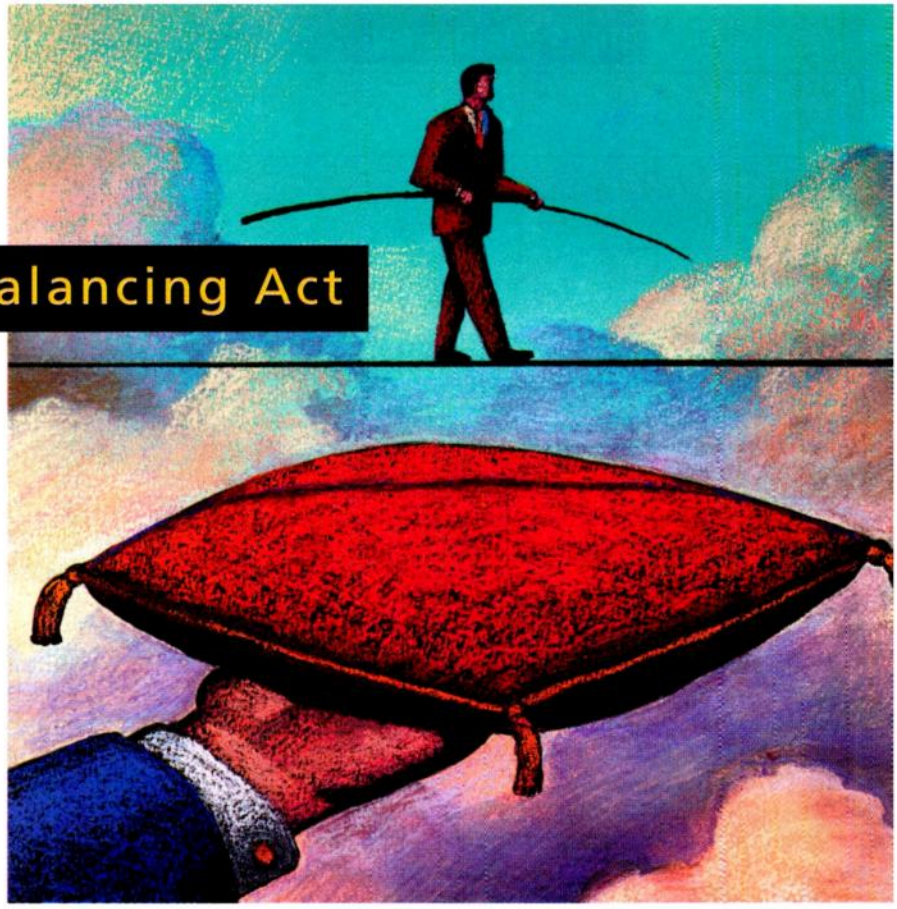

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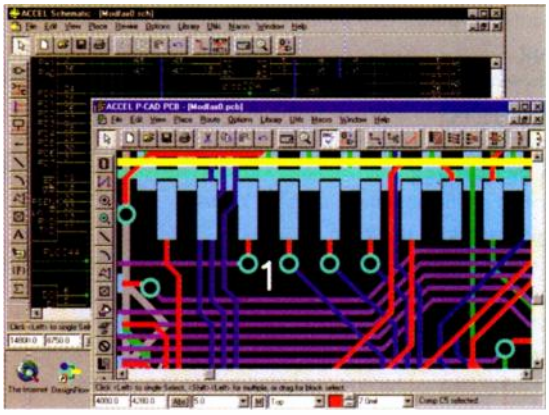

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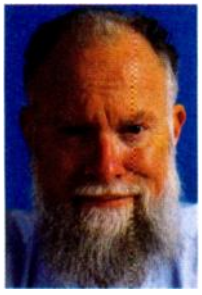
BOB PEASE

# What's All This Manic Stuff, Anyhow?

A while back, I was invited to give a lunchtime lecture at the Bipolar Circuits and Technology Meeting (BCTM) in Minneapolis. I talked about "What's All this Bipolar Stuff, Anyhow?" and that also turned into a column (*ELECTRONIC DESIGN, Aug. 7, 1995, p. 95*).

At this lecture, I told a story about a journal my wife was reading. Nancy said, "Bob—this article in this magazine says that people with Bipolar Disorder have a lot of problems, conflicts, fights, suicides, and murders... is that what this conference is about?" I roared, "Yeah, those are all my friends!" When I told this story at the lunchtime lecture, all the audience roared and laughed. And I did, too.

At the time it was amusing because I was not really very familiar with "Bipolar Disorder." But, I have gotten a little more education. First of all, bipolar transistors and bipolar disorder have NOTHING in common. Bipolar *transistors* mean ordinary NPN and PNP transistors, as distinguished from JFETs and MOSFETS. A bipolar transistor has holes and electrons, an emitter and base, and a collector. If you (as I do) still work with bipolar transistors and want information on this conference, contact Jan Jopke at *jjopke@aol.com*.



**BOB PEASE** OBTAINED A BSEE FROM MIT IN 1961 AND IS STAFF SCIENTIST AT NATIONAL SEMICONDUCTOR CORP., SANTA CLARA, CALIF.

"Bipolar Disorder" simply means a person who is alternately depressed, seriously unhappy, and then very positive and cheerful. "Bipolar" just means alternating from depression to happiness. This definition is not widely appreciated. Even the article my wife was reading was kind of vague about it.

Then a couple months ago, I was absentmindedly listening to the radio at 3 a.m. The guy was talking about people who have this manic phase, are very enthusiastic, and get along on three hours of sleep. I perked up my ears and said, "HECK! They are talking about me!" I listened some more and realized that when a person who has bipolar disorder is in the POSITIVE phase, he (she) is very enthusiastic and positive and gets along great on very little sleep. Conversely, when a person is in the negative phase, they need lots of sleep and are quite unhappy and depressed. I read some more about this in a book by Colette Dowling (*You Mean I Don't Have to Feel This Way?*, Scribners, New York, N.Y., 1991). Well, I have almost always been a positive and happy person. I don't think I have ever been *depressed*, even in the case of the loss of a great person or friend. Almost nobody gets out of here alive, but most of us survivors will find ways to keep on going and make the world a better place.

When I was a kid, I learned that the St. Germain family up the road came from Maine. Lucien, Bobby, Patsy, and Janora—nice kids. We kids sometimes called them "Mainiacs." It was just a part of learning how to use words—or to CONJURE with words—and I don't think we caused them any pain. It was all in good fun. To this day, I would never fail to call a person from Maine a "Mainiac" if it would make us all smile.

But, what is a "Maniac?" Is that you—or is it me? Maybe so. You guys may have noticed that I am sometimes DRIVEN with a passion—a *mania*. Are all manias bad? I dunno. Maybe if taken to excess.

Mark Twain really did say this, probably: "Too much of anything is an excess, bad; but too much whiskey is just right." As usual, he got some parts of the story wrong, but he got some parts right.

What is an excessive enthusiasm? Good for some, not for others. I cannot give all the facts on this, but all you readers will recognize that I've been CRUSADING for several ideas for years, and my energies can be pretty extreme. Many charities that do good for people are similarly endowed with people who are "off on a rant." Good for them. The world needs people who give a damn and are *driven* and obsessed.

By the way, I sometimes used to read *Machine Design* magazine. But, then it was taking too much of my time. I found a cache of a dozen unread *Machine Design* magazines from '92. I realized there was NO WAY I could read them all, so I recycled them even before my wife began to gripe. But more recently, I acquired a subscription and began reading the recent columns (editorials) of Ron Kohl. He is almost as fine a madman as I am. While he is constrained to a mere 3 kbytes of column every issue, he does really well. I LOVE most of his editorials. I hate to say it, but his magazine and editorials have some EXCELLENT ideas. To sign up, e-mail to *circulation@penton.com*, or go to their web site at *www.penton.com/md/subscribe/index.html*. To buy a book of a collection of Ron's editorials (about $16), called *Mad as Hell*, just dial (800) 213-9150.

On a good day, manics contribute a lot to the world. I try to. I have boundless energy (except when my wife wants me to clean out something).

Is there a CURE for bipolar disorder? Apparently, some of the lithium-based drugs can help relieve the extreme manic state and decrease the depression. It's standard treatment, prescribed by your doctor. I have never heard ANYBODY propose that there is (or should be) a cure for the mania or enthusiasm. What do you think?

All for now. / Comments invited!
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WALT JUNG

# Op-Amp Audio

## *Realizing High Performance: Bandwidth Limitations*

For this November *Analog Special* installment, we'll take a look at some of the very basic issues surrounding op amps used within high-quality audio circuits. A parameter which ultimately affects a gamut of op-amp performance specs is device gain-bandwidth. This is related to the device's open-loop bandwidth and gain in predictable ways. These interrelated issues, along with the nature of the feedback for a particular application, ultimately become major quality determinants.

**The open-loop bandwidth problem:** Virtually all conventional voltage-feedback-type op amps have a high open-loop gain (≅ 100 dB), and a relatively low open-loop bandwidth (10 to 100 Hz). By voltage feedback, we specifically mean the classic op-amp types with symmetrical ± inputs, and are excluding current-feedback types (at least for now). Of course, this voltage-feedback category includes audio-specialized types, as well as more conventional non-audio ones.

All such amplifiers are designed to be flexible and easily applied within an overall feedback system with closed-loop stability usually down to unity gain. For unity-gain stability, the application of feedback demands a controlled rate of open-loop roll-off. This roll-off is a uniform 6 dB/octave gain reduction with frequency. The associated 90° phase lag of such an open-loop response will guarantee closed-loop stability for any feedback level.

But herein lies the rub. What seems like a relatively simple system trade-off in design philosophy may not actually be so. Why is this? Isn't any op-amp-based audio design more simple than a classic RC-coupled transistor gain stage? A more complete answer here is a rather complex one, and it involves an understanding of the feedback process. It also involves implications of applying the feedback around what can often be imperfect amplifier hardware. For example, a nonlinear op-amp input stage, combined with less-than-optimum-bandwidth.

We do know that an op-amp-based gain stage can be just about as simple as it gets system-wise—at least on the surface. It consists simply of the op-amp device itself, plus a pair of resistors to set the desired gain (*see the figure from Part 1*, ELECTRONIC DESIGN, *Sept. 1, p. 166*). Unfortunately, the underlying weaknesses of how such a feedback-based amplifier can degrade some aspects of overall performance often gets bypassed, particularly when there is pressure to employ only standard, low-cost ICs (such as 5532 types and their derivatives).

An op-amp gain stage is unrivaled in *utility*, a feature which is very compelling. But, it trades off open-loop gain for bandwidth, operating within the constraints of a constant gain-bandwidth product. For the 5532 mentioned, the applicable gain-bandwidth is 10 MHz, and the open-loop gain is 100 dB ($10^5$ V/V). Thus, the open-loop bandwidth is 100 Hz. Actually, a close examination of the 5532 data sheet shows more like 200 Hz, due to the fact that this particular topology uses a feedforward technique, which boosts gain-bandwidth at lower frequencies. But, in general, the available *small-signal* gain at any given frequency is defined by the op amp's gain-bandwidth. Note the emphasis here on the small-signal aspect. And, it's helpful to understand that the application of different feedback does not change a given device's basic gain-bandwidth—it only reallocates it to some different closed-loop gain and bandwidth.

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All of this may seem reasonable enough, until we go a step further, and consider the fact that the op-amp gain-bandwidth is based upon the small-signal transconductance ($g_m$) of the input-stage transistors, plus a fixed compensation capacitor (usually internal). If we consider this compensation cap fixed (for this discussion, at least), it should be obvious that the $g_m$ of the input devices is also fixed, ideally. In other words, it doesn't vary with the input signal level.

But, within real devices, the $g_m$ most certainly *does* vary. In fact, those devices that are best in terms of voltage noise performance—bipolar junction transistors (BJTs)—are worst in terms of their *transconductance linearity*. Barrie Gilbert has explored many of these non-ideal op-amp performance limitations in some recent *EDTN* columns.[1,2] Reference 2 includes a mathematical distortion analysis of an op amp. The analysis shows how an undegenerated BJT input stage (as just described) is actually quite poor in terms of standalone-mode distortion. The fundamental source of this distortion is the nonlinear $g_m$ of the emitter-coupled BJT pair, which follows a hyperbolic tangent (tanh) function. Ideally this $g_m$ would be highly linear, i.e., the inverse of a fixed resistance. While it isn't linear with a simple emitter-coupled BJT pair, it's much more so when the pair is operated with emitter-degeneration resistors, or the bipolars are replaced by JFET devices.

In an op-amp feedback circuit using such a nonlinear BJT input stage, the forward gain path typically includes the input stage as described, followed by an integrator stage which includes the aforementioned compensation cap, and a final output stage for load isolation.

When such an amplifier is placed within a simple, flat-frequency-response feedback setup, it's useful to contemplate what happens with a wideband audio signal passing through it. Consider, for example, a given input-signal level, and a flat voltage vs. frequency characteristic at the *output*. Increasing signal frequencies above the amplifier's open-loop corner frequency will result in a higher and higher input driving voltage to the op amp. (Not the signal input, but the actual voltage between the ± terminals.) This is a natural consequence of the feedback error correction, and the gain-vs.-frequency reduction within the op amp.

But, since the BJT input stage $g_m$ is nonlinear, and is followed by a low-pass filter in the form of the integrator, higher signal frequencies require higher amplifier driving voltages to maintain the same output levels. This means higher frequencies must neces-

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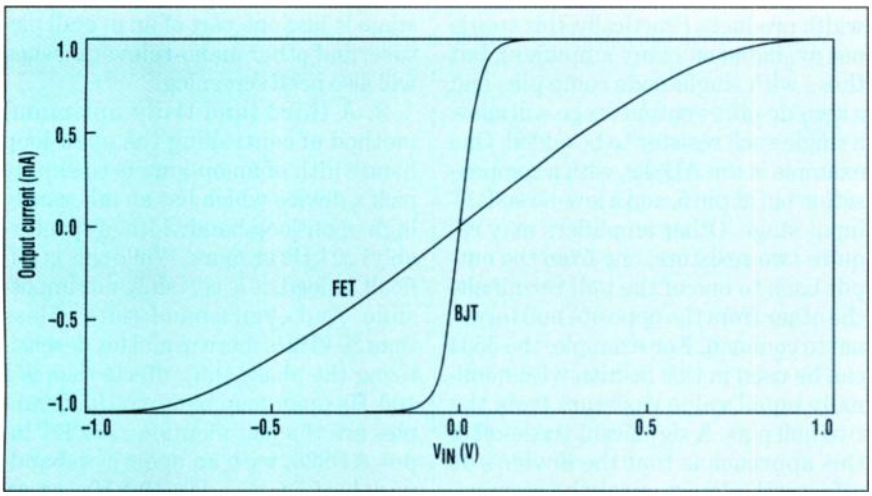


**The relative transconductance characteristics for a ±1-V input range are displayed for both BJT and JFET differentially paired transistors. Both types use no emitter (source) resistance, and are biased by a fixed current of 1 mA. These curves were generated by PSpice, using 2N2222A and 2N5457 models available with that simulation package.**

sarily drive the input stage harder, to counteract the filter roll-off. Because the input stage's $g_m$ is different with a greater input drive, it produces a different corner frequency and phase shift (compared to lower frequencies, which require less amplitude drive). Considering just a case of one output level, this is a frequency-dependent nonlinear phase response.

When the output level is further increased, this phenomenon gets worse, until at some combination of amplitude and frequency, the op amp finally reaches its slew-rate limit. By definition, this occurs when the input stage is totally overloaded by the peak error voltage, at which point the output voltage from the op amp reaches its maximum rate-of-change.

So, in the absence of any corrective means, it can be shown that virtually all BJT-input-stage op amps (either IC or otherwise) can be limited in terms of input-overload sensitivity. And, they are nonlinear prior to their overload point. This is due to their extremely high and exponentially related $g_m$.

To put all of this in an overall perspective, a balanced BJT differential pair will develop around 1% THD for input signals which are just under 20 mV in peak amplitude. When such an input stage is used within a 10-MHz-gain-bandwidth op amp handling a 20-kHz, 10-V peak output signal, the actual amplifier driving signal will be 20 mV peak—it is just beginning to distort. If the amplifier were instead a 1-MHz "741-speed" device, the driving signal theoretically would be 200 mV peak. In practice, such an amplifier would more likely be operating in its slew-limited mode, and producing gross output distortion.

For today's audio op amps with bandwidths of 10 MHz or more, it could be argued that only the most extreme high-level, high-frequency audio signals even begin to push a non-degenerated BJT-input op amp into the nonlinear region. On the other hand, for digital signal byproducts, and other spurious out-of-band high-frequency components, the distinction may not be so clear. Here, an amplifier with more-linear input stages may be a better choice. And, if you've ever experienced spurious AM-band signal detection by a bipolar input stage op amp, you'll be able to relate to all of this, for sure!

**...the BJT-device $g_m$ is both higher and more nonlinear than that of the JFET.**

A positive aspect of this situation is that the BJT-input amplifier can easily achieve low input-noise performance, and it is good for low-level signals. But, the not-so-good side is that it can possibly show increasing distortion and phase shift effects for high-level, high-frequency signals above the open-loop corner frequency.

**Comparing BJT/JFET $g_m$:** Since op amps are available with front ends consisting of either bipolar or JFET transistors, it is useful to compare them for overload. The $g_m$ characteristics of both 2N2222A npn BJT and 2N5457 N-channel JFET differential-pair transistors make for a good comparison *(see the figure)*.

In these simulation plots, both transistor pairs are biased at the emitters (sources) by a 1-mA current source. The BJT-pair output is represented by the more steeply sloped trace in the center, with an input dynamic range of about ±200 mV for the ±1-mA output current. Also shown is the more-linear, gradually sloped $g_m$ plot of the JFET pair, which has an input dynamic range of nearly ±1V for the same output current. That is quite a contrast!

These data indicate the two major points just discussed above. Namely, that the BJT-device $g_m$ is both higher and more nonlinear than that of the JFET. In fact, the degree of nonlinearity for the BJT case isn't readily apparent from this view, but it is easily revealed by comparing plots of differentiated data.

**Extending open-loop bandwidth:** Since the presence of an amplifier open-loop corner within the audio range, combined with feedback around a nonlinear BJT input stage, can give rise to dynamic phase shifts, a question arises: what can be done counteract it? Solutions are available in 3 forms.

1. One solution is by extending the effective open-loop bandwidth, so as to move the open-loop corner upward to 20 kHz or more. This step doesn't change the distortion in the input stage. But, it can reduce or remove the phase-modulation effects due to $g_m$ variations—as the open-loop corner is moved upward to a region where (presumably) signals either do not occur, or they occur less frequently, or at lower levels.

The route to achieving this step can be as simple as adding one (or two) resistor(s) across the amplifier integrator. This damps the integrator and lowers the open-loop gain, thus moving the open-loop corner upward in frequency (again, within the constraints of the device's gain-band-

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width product). Practically, this step is not available on many amplifiers, but those with single-node comp pins and a zero-dc-offset output stage will allow a single such resistor to be added. One example is the AD829, with a compensation pin at pin 5, and a low-noise BJT input stage. Other amplifiers may require two resistors, one from the output back to one of the null terminals, the other from the opposite null terminal to common. For example, the 5534 can be used in this fashion with nominally equal value resistors from the two null pins. A significant trade-off of this approach is that the device's dc offset will almost surely be compromised by this inner-loop connection. This can in theory be corrected by a trim adjustment, but this step isn't likely to be practical.

Unfortunately, there are no common standards of what pin(s) are used for these secondary-bandwidth control functions, or what the relevant resistance(s) are, so some user experimentation is appropriate here, once given the proper amp.

Viewed from a system-level perspective, there's a more elegant and less compromising solution to optimizing the open-loop bandwidth of an op-amp circuit. Use multiple-stage feedback, so that the overall input-stage-to-integrator interface is controlled by local, signal-independent transfer characteristics.

Of course, this is a much more complex solution, and a useful working example will need to wait until a later installment. It also happens to be about the only practical way one can realistically implement the open-loop bandwidth control trick using dual (or quad) amplifier packages.

2. Use more-linear devices for the input transistors, which lessens the signal phase-modulation problem by reducing $g_m$ nonlinearity. This is simply achieved by using a well chosen op-amp. For example, one using a JFET input stage, either PFET or NFET. Both types typically have the desired lower $g_m$. A wide variety of general purpose FET input devices are available for this task, from the TL07X series of early JFET designs, to more recent devices such as the AD744 family, and the recent AD825 device. Of course, one does need to be selective here, as the JFET input stage is just one part of an overall picture, and other audio-relevant issues will also need screening.

3. A third (and truly optimum) method of controlling the open-loop bandwidth of an op-amp is to simply pick a device which has an inherently high open-loop bandwidth of (preferably) 20 kHz or more. While this is difficult indeed, it is certainly not impossible. And even a bandwidth of less than 20 kHz is more useful for desensitizing the phase shift effects than is a 100-Hz open-loop bandwidth. Examples are the just mentioned JFET input AD825, with an open-loop bandwidth of just under 10 kHz, or an AD817, with a similar bandwidth. The AD817 uses a BJT input stage with emitter degeneration, which gives it very good linearity.

On the downside, amplifiers that have lower-$g_m$ input stages will typically tend to be more noisy than will their lower-noise, non-degenerated BJT cousins. This makes them useful for higher-level signals, as opposed to low-level front end applications. It is another of those system-level tradeoffs a designer must make in honing a final high-performance design.

**TIP:** One or more of these bandwidth-extension and/or linearization methods can be useful in practice, and they are recommended to you for further experimentation. In a future column, we'll show an example of a multiple-feedback-stage design which uses method 1 above for bandwidth extension and input linearization.

References:

1. Gilbert, Barrie, "Op-amp Myths," *EDTN* web site, March 9, 1998, *www.edtn.com/analog/barrie1.htm.*

2. Gilbert, Barrie, "Are Op-amps Really Linear?" *EDTN* web site, June 10, 1998, *www.edtn.com/analog/barrie4.htm.*

Suggested Reading:

Otala, Matti, "Feedback-generated Phase Modulation in Audio Amplifiers," 65th Convention AES, 1980, London, U.K., Preprint # 1576.

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ANALOG

## Pipelined 12-Bit, 20-MSPS ADC Consumes Ultra-Low Power

Designed to operate from a 3.3-V power supply, the SPT7935 is a 12-bit analog-to-digital converter (ADC) that samples at the rate of 20 Msamples/s. In addition, it burns only about


79 mW. This ultra-low power consumption is attributed to a pipelined architecture and a 0.5-µm CMOS process. To maintain high dynamic range, the SPT7937 features an on-chip track-and-hold amplifier. The input capacitance of the converter is only 1.4 pF. With low distortion, high dynamic range, and ultra-low power consumption, the ADC is best suited for imaging, multichannel communications, instrumentation, and digital radio applications.

In production, the SPT7935 comes in a 44-lead thin quad flat-pack (TQFP) package. It's rated for the commercial temperature range of 0 to +70°C. In quantities of 1000, the 12-bit SPT7935 is priced at $9.90. AB

***Signal Processing Technologies,*** *4755 Forge Rd., Colorado Springs, CO 80907; (719) 528-2300; www.spt.com.*
**CIRCLE 557**

## Low-Dropout Regulator Works With Any Capacitor

The ADP3307/08/09 precision low-dropout voltage regulators can deliver high accuracy and stability with any type of 0.47-µF output capacitor, regardless of its equivalent series resistance (ESR). This new anyCAP technique employs a single loop for regulation and reference, which is controlled by a very high gain error amplifier. A noninverting driver between the error amplifier and the pass transistor is designed to provide the compensation. This reduces sensitivity to the value, type, and ESR of the load


capacitance, according to Analog Devices.

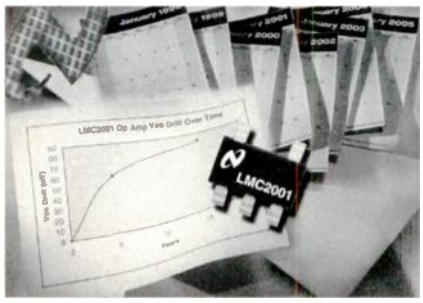
Designed for medium load currents, the ADP3307/08/09 offer high accuracy dropout regulation of ±1.4%, ±2.2% and ±2.2%, respectively. While ADP3307/09 maintain a low-dropout voltage of 160 mV(typ.) at 100 mA, the ADP3308 offers 80 mV (typ.) at 50 mA. The ADP3308/09 are pin-compatible with National's LP2980 and Micrel's MIC5205 LDOs.

The ADP3307 comes in 6-lead SOT-23, and the ADP3308/09 are available in 5-pin SOT-23s. In 1000 pieces, the ADP3307 is priced at $0.94, the ADP3308 at $0.81, and the ADP3309 at $0.91. AB

***Analog Devices Inc.,*** *Ray Stata Technology Center, 804 Woburn St., Wilmington, MA 01887; (781) 937-1428; www.analog.com.* **CIRCLE 558**

## Op Amp Offers High Precision Over Ten-Year Span

The LMC2001 represents a new class of operational amplifier that guarantees high precision over a period of ten




years. As a result, the LMC2001 ensures 5-µV offset error drift over ten years, while eliminating 1/f noise as a source of signal error. This is made possible by a proprietary error-correction technique that self-corrects voltage offset over time and temperature.
*(continued on page 136)*

(continued from page 135)

Key features include input offset voltage of less than 40 µV after a mere 15 ms of startup time, drift over temperature of less than 0.030 µV/°C, and a gain bandwidth product of over 6 MHz. Its slew rate is 4 V/µs. In dc performance, the LMC achieves 117 dB of common-mode rejection ratio (CMRR), 118 dB of power-supply rejection ratio (PSRR), and 120 dB of open loop gain at a 2-kΩ load.

It's implemented in a sub-micron biCMOS process for reduction in die size and cost. Housed in 5-pin SOT-23 and 8-pin SOIC packages, the LMC2001 is priced at $1.20 in 1000-unit quantities. AB

***National Semiconductor Corp.**, 2900 Semiconductor Dr., Santa Clara, CA 95052-8090; (408) 721-5000; www.national.com.* **CIRCLE 559**



## Audio Sample-Rate Converter Eliminates Compatibility Issues

The CS8420 is a highly integrated 24-bit digital audio sample-rate converter for consumer and professional audio systems. It supports a wide array of audio standard rates, ranging from 8 to 96 kHz. Consequently, it can be used in compact discs, PC audio, movie soundtracks, and professional audio systems, thereby eliminating compatibility issues and simplifying audio system design. In addition, it incorporates a digital audio receiver and transmitter functions, which comply with standards such as AES/EBU and S/PDIF. As a result, the digital audio data can be sent at any commonly used sample rate required, and the CS8420 will automatically convert the data to the sample rate required by the specific digital audio system. According to Cirrus Logic, this simplifies the clocking architecture of the audio system because it only has to support one sample rate internally.

Because the device supports 24-bit input and output resolution, it allows users to connect a 24-bit audio source or 24-bit digital-to-analog converter to the unit without degrading performance. The CS8420 also employs a truncation technique to output word sizes of 16 or 20 bits, thereby maintaining audio quality across a variety of systems. Consequently, digital audio inputs and outputs may be 24, 20, or 16 bits. This allows the input data to be asynchronous to the output data, with the output data being synchronous to an external system clock.

Furthermore, the CS8420 offers high clock jitter rejection, and provides flexible three-wire serial digital I/O ports. The unit offers 120-dB dynamic range, and a total harmonic distortion plus noise (THD+N) of –117 dB. These features allow the CS8420 to modify the input frequency smoothly to avoid sound-quality distortion due to aliasing.

Sampling now, the CS8420 converter is set for production in the next quarter. In quantities of 1000 units, the sample rate converter is priced at $13.90. AB

***Cirrus Logic Inc.**, Crystal Semiconductor Products, P.O.Box 17847, Austin, TX 78760; (512) 445-7222; www.cirrus.com.* **CIRCLE 560**

DIGITAL ICs

## 8-kgate FPGA Delivers 4-ns Clock-To-Output Delays

The smallest member of the Actel SX FPGA family, the SX08, provides users with 8000 usable gates. It also delivers some of the shortest propagation delays at just 4 ns (clock to output). The short delays allow for very high clock rates—the chip can handle internal clock signals of up to 320 MHz—suiting the device for many high-performance applications.

Functions such as a 32-bit-wide decode can be executed in just 7.7 ns, pin-to-pin, and applications like 8b/10 encoding for gigabit Ethernet routers, and high-speed interfaces for DS3 networks, can readily be implemented with the SX-family devices. Input setup times are less than 0.6 ns for all the SX devices. These range in density from 8000 to 32,000 usable gates, and provide mixed 5-V/3.3-V support with 3.3-V output drive and 5-V tolerant inputs.

The 8000-gate chip will be housed in packages that offer a variety of I/O pin-count options ranging from 84 to 208 pins, and will sell for as little as $8.90 each in large quantities. Samples are available now. DB

***Actel Corp.**, 955 East Arques Ave., Sunnyvale, CA 94086-4533; Deon Spicer, (408) 739-1010, www.actel.com.* **CIRCLE 561**

## Revamped Z8 Microcontroller Lowers Cost Of OTP Versions

By selling for just $0.39 each in 500,000-unit lots, the Z8E000 now becomes one of the lowest-cost one-time programmable microcontrollers available. The MCU includes 512 bytes of one-time-programmable program memory, 32 bytes of register-file SRAM, a 16-bit timer, and a watchdog timer. As a result, it provides a simple solution for many control applications.

Available in both commercial (0 to 70°C) and extended-temperature (–40 to +85°C) versions, the Z8E000 comes in either an 18-pin DIP or a small-outline surface-mount package. The controller is part of the company's extensive Z8 family, which includes over 100 processor derivatives. It can meet the needs of applications such as sensors, battery chargers, motor controllers, handheld meters, thermostats, and many others. To aid system development, Zilog also offers the Z8ICE000ZEM, a low cost ($99) real-time in-circuit emulator that includes the programmer, assembler, and graphical-user-interface software. Samples of the processor are available now. DB

***Zilog Inc.**, 910 East Hamilton Ave., Ste. 110, Campbell, CA 95008; Mike Thompson, (408) 558-8500; www.zilog.com.* **CIRCLE 562**

## Silicon DAA Takes On International Callers

A highly programmable architecture forms the heart of the Si3034 chip set—a silicon data access arrangement (DAA) that can meet worldwide telecommunications interface standards. The circuits are a pin-compatible upgrade to the company's already available Si3032 silicon DAA chip set that's used for U.S. telecommunications systems. The world DAA includes the company's patented ISOLink technology. ISOLink improves performance over traditional transformer-based implementations, reduces board space by about 75%, and lowers DAA costs by about 40%, as compared to existing DAAs.

The programmable aspects of the chip allow it to handle FCC, CTR21, NET4, and JATE standards, as well as PTT specific requirements. Programmable aspects include ac and dc termination, ringer impedance, and ringer threshold. These aspects are programmed via simple control commands sent by the modem control logic.

The Si3034's architecture also can handle the most difficult international requirements for out-of-band energy, billing tone immunity, lightning surge protection and isolation, and advanced modem features such as caller ID and on-hook line monitoring.

The Si3034 chip set consists of the Si3014-KS and Si3021-KS, which are housed in 16-lead SOIC packages. The chip set sells for $7.86 per set in lots of 10,000 units, and samples are immediately available. An evaluation board, the Si3034-EVB, is priced at $175. DB

***Silicon Laboratories Inc.**, 2024 E. St. Elmo, Austin, TX 78744; Gary Gay, (512) 416-8500; www.silabs.com.*

**CIRCLE 563**

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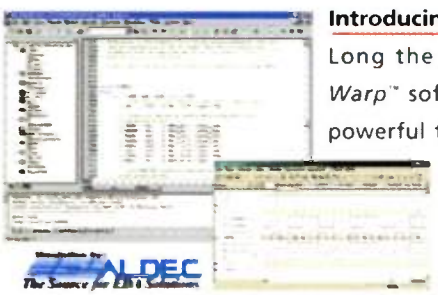


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