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DECEMBER 14, 1998



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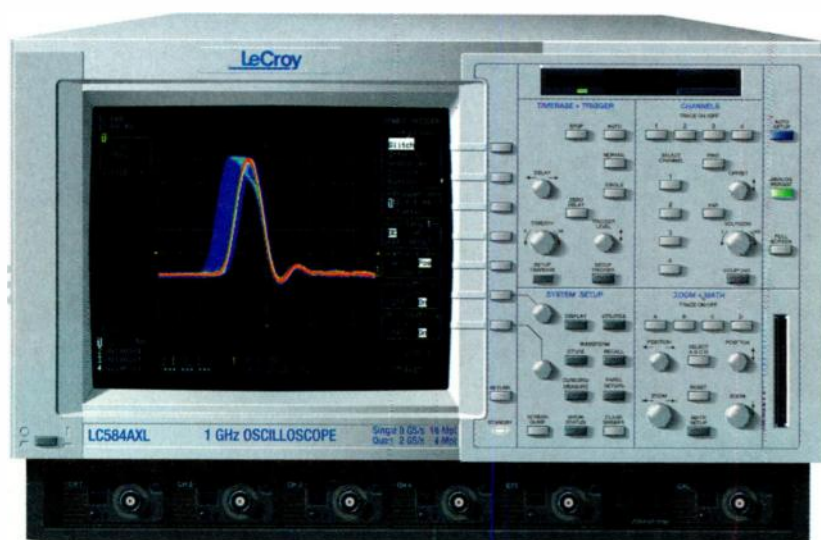
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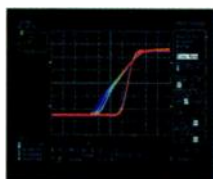
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December 14, 1998 Volume 46, Number 28

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### ■ AWGs Tackle Digital Modulation And MEMS Testing 33

■ Process Simulator Analyzes Contamination Impact On MEMS Layouts 27

■ Careful HDL Coding Maximizes LUT-Based FPGA Performance 51

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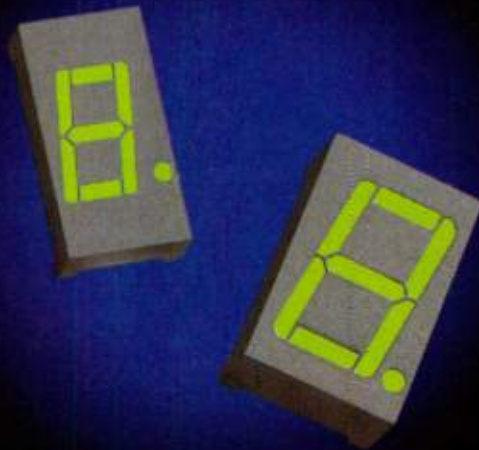
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## LOOKING AHEAD: January 11, 1999

### Engineering In The New Millennium:

The entire editorial staff leverages its many years of experience and takes an insightful look at how engineering will change as the clock strikes 2000. There are three main thrusts in this forecast: seven technology-specific reports addressing the issues shaping that technology; a series of viewpoints on the state of international engineering; and a final section addressing themes that cut across all technologies and will decidedly affect how engineering is performed.

● **The Technology Beats.....**Each of our seven technology editors speaks out on future design trends, challenges, and solutions in their particular area of expertise. Hear their opinions on what will drive the industry along the fast-paced millennium highway. Don't be surprised if the system-on-a-chip is a common thread in many areas of electronics.

● **Global Outlook.....**Our international correspondents take a look at tomorrow's global engineering environment. You'll get perspectives from Europe, China, Japan, and South America. Find out how far Europe will push smart-card technology.

● **Supplemental Topics.....**Additional topics getting their share of attention will be matters that concern engineers not only as designers, but as people, too: Professional Issues, Green Engineering, Nanotechnology, the Internet as a Tool, and Safety Concerns.

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December 14, 1998 Volume 4 Number 28

See Electronic Design Online's  
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what's in store for you on the web!

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And so, with the end of the year, we're asking you to send us your thoughts on what happened during the year in engineering. What were some of the most important events that took place during the year?

What were the best products? What companies do you see having a major impact in the marketplace in 1999? Has your company taken the necessary steps to overcome the Y2K bug?

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- \$3,450† High Performance MADS Development Kits (complete-fully assembled)

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DEVICE	EPROM (bytes)	RAM	PIXS	DESIGN-IN HIT	MMEVS HIT	MADS HIT
68HC705KJ1	1.2K	64	16	M681CS05J	KITMMEVS05KJ	KITMMDS05KJ
68HC705J1A	1.2K	64	20	M681CS05J	KITMMEVS05KJ	KITMMDS05KJ
68HC705P6A	4.6K	176	28	M681CS05P	KITMMEVS05P6A	KITMMDS05P6A
68HC705C8A	8K	304	40,44	M681CS05C	KITMMEVS05C	KITMMDS05C
68HC705C9A	16K	352	40,44	M681CS05C	KITMMEVS05C	KITMMDS05C
68HC705B16	15K	352	52,64	M681CS05B	KITMMEVS05B	KITMMDS05B
68HC705L16	16K	512	80	KITPGMR05L16	KITMMEVS05L16	KITMMDS05L16

†Suggested resale



PICO

## Low Profile .2" ht. Surface Mount Transformers & Inductors



All PICO surface mount units utilize materials and methods to withstand extreme temperature (220°C) of vapor phase, IR, and other reflow procedures without degradation of electrical or mechanical characteristics.

### AUDIO TRANSFORMERS

Impedance Levels 10 ohms to 10,000 ohms, Power Level 400 milliwatt, Frequency Response  $\pm 2$ db 300Hz to 50kHz. All units manufactured and tested to MIL-T-27.

### POWER and EMI INDUCTORS

Ultra-miniature Inductors are ideal for Noise, Spike and Power Filtering Applications in Power Supplies, DC-DC Converters and Switching Regulators. All units manufactured and tested to MIL-T-27.

### PULSE TRANSFORMERS

10 Nanoseconds to 100 Microseconds. ET Rating to 150 Volt-Microsecond. All units manufactured and tested to MIL-T-21038.

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## Telecom Is Shaping DSP Architectures

While x86 and derivative microprocessors keep their stranglehold on the PC motherboard, programmable DSPs have snuck into the center of the digital revolution in communications. And, digital signal processing is getting stronger with each generation of digital wireless—as well as wireline telecom—applications. Now, third-generation (3G) digital cellular phones and basestations, in conjunction with other high-performance emerging markets like wideband communications systems, software radio, MPEG-4, and video-on-demand, ask a lot more from DSPs. Their demands are in terms of MIPS, multiply/accumulates (MACs), and other processing power. The result is the evolution of a whole generation of DSP architectures with a completely different way of thinking. The DSP battlefield has risen to a much higher level. On this plane, compilers, high-level languages, and the right set of integrated development tools are the ammunition required to gain ground in this expanding market.

Some of these developments were unwrapped at the recent Microprocessor Forum in San Jose, Calif. The first result of collaboration between Lucent Technologies' Microelectronics Group and Motorola's Semiconductor Sector, the Star\*Core 400, was revealed. Compiler-friendly and highly scalable, this 400 DSP architecture departs from the traditional multi-MACs, superscalar, or very-long instruction-word (VLIW) types. The partners call it a post-VLIW architecture that offers a scalable instruction model with variable-length execution sets (VLES) and explicitly parallel instruction computing (EPIC). Planned for implementation in 0.13- $\mu$ m CMOS, the Star\*Core 400 is architected to offer 1200 DSP MIPS at a 300-MHz clock frequency. Complete tools and design details are expected to be released in the first half of 1999, with core silicon implementation in the second half.

The same session also witnessed the unfolding of a third-generation SHARC architecture from Analog Devices Inc. Designated TigerSHARC, it implements a static superscalar design that promises to perform 2 billion MACs/s using 16-bit data at a 250-MHz clock—or 500 million 32-bit MACs. In fact, it provides native support for 8-, 16-, and 32-bit data processing. Based on 0.25- $\mu$ m CMOS, ADI plans to sample the 250-MHz TigerSHARC by early next year.

Other late developments came from the DSP Group and Siemens AG. The DSP Group described its newest, fixed-point engine PalmDSPCore with a high level of parallelism using a dual-MAC architecture, a configurable data path (16-, 20-, or 24-bit), and a variable-size instruction set. Meanwhile, Siemens unveiled a configurable LIW (CLIW) DSP core developed by its design and development arm, IC Com, Azor, Israel. Combining flexible instruction-set capability with a superscalar architecture, Siemens' Carmel processes 120 multiple MIPS at 120 MHz and 2.5 V. Performing 15 elementary operations in one cycle translates into 1800 MOPS. An evaluation board with Carmel is slated for sampling early next year. The Carmel roadmap shows 180 multiple MIPS at 1.8 V using 0.18- $\mu$ m CMOS, with plans to push it to 240 multiple MIPS at 1.3 V by the year 2000. Like the DSP Group, Siemens' strategy is to license the soft DSP core.

These announcements come on the heels of Texas Instruments' plan to extend the advanced VLIW-based C6000 DSP platform with powerful members like the C6202 and C6211. The compiler-friendly TMS320C6202 is rated to operate at 250 MHz and offer 2000 MIPS or 500 million MACs. These players and more will compete for a portion of the communications pie for DSPs, which is expected to reach \$5 billion next year and over \$7 billion by 2000, according to Forward Concepts, Tempe, Ariz. To be successful in this market, it will take more than architecture and tools. These powerful DSPs must work with high-performance, front-end analog and mixed-signal data converters and interfaces. Such expertise will play a key role in the success of the system-level DSP solution in this applications space.

Please send your comments to [abindra@penton.com](mailto:abindra@penton.com).



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### Leaner Design for Faster Processing Speed

Dallas' recipe starts with a pin-compatible 8051 processor core, then cuts the fat of wasted clock cycles. 33 MHz works like 99 at no extra charge. On one side of the processor, a 10-bit, eight-channel A/D converter inputs analog signals. On the other side, a Pulse Width Modulator (PWM) outputs four channels of 8-bit signals, or cascades to two 16-bit channels. Four capture and three compare registers monitor background events and can trigger processor activity.

### Deluxe Stacking=More Good Stuff

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With abundant features you get flexibility. Need to communicate with old, slow peripherals? A Stretch Cycle feature automatically inserts wait states into external MOVX operations. Faster data pointers? You get two, able to both increment *and* decrement.

### When Less is Better

The DS87C550's Power Management Mode slows the clock speed to use less power than Idle Mode. For less noise, EMI Reduction Mode shuts off the ALE signal when not needed.

When you want it all for your embedded system design, give us a call and order up the full menu on one chip. The DS87C550 EPROM Microcontroller with A/D and PWM. (Even the name's a mouthful.)



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WR3



### PCB Mount High Isolation Transformers

14A Series—provides high isolation, creepage, and clearance necessary to comply with international safety standards.



- UL 94 V0 flame-retardant, double-reinforced insulation
  - 2.5 to 56 VA
  - 100% hipot tested @ 4 kV RMS
  - UL recognized Class F (155°C) insulation system
- Agency approvals: UL 506, VDE 0805 / EN60950 / IEC 950, CSA C22.2 #66 1988; also designed to meet construction requirements of UL 478, 544, 1411, 1563, 1585, 2601-1, IEC 601-1, IEC 65, IEC 1010

See Specs: [www.signaltransformer.com/14A/ed](http://www.signaltransformer.com/14A/ed)

### Greater Performance In Less Space

M4L Series—featuring main isolation for high-power applications.



- UL 94 V0 flame-retardant, double-reinforced insulation
  - 300, 600, and 1000 VA sizes
  - 100% hipot tested @ 4.0 kV RMS
  - UL recognized Class H (180°C) insulation system
  - IEC Touch-safe Eurostyle-type terminals
- Agency approvals: UL 544, 506, CSA C22.2 #66 1988, VDE 0805 / IEC 950 / EN60950, also designed to meet construction requirements of IEC 601-1, IEC 65, IEC 1010, UL 478, 1411, 1563, 2601-1, 1585

See Specs: [www.signaltransformer.com/M4L/ed](http://www.signaltransformer.com/M4L/ed)

### High Performance With Greater Volumetric Efficiency

MPI Series—higher volumetric efficiency for improved performance compared to conventional 50/60 Hz transformers.



- 200 to 900 VA
  - International safety isolation and distribution
  - 25-amp rated 5-mil copper screen
  - 100% hipot tested @ 4.0 kV RMS
  - UL recognized Class F (155°C) insulation system
  - IEC Touch-safe Eurostyle-type terminals
- Agency approvals: UL 506, CSA C22.2 #66 1988, TUV Rheinland EN60742 / IEC 742

See Specs: [www.signaltransformer.com/MPI/ed](http://www.signaltransformer.com/MPI/ed)

### Greater Performance In Less Space and Weight

HPI Series—features coil construction complying with international safety standards.



- 1250 to 3500 VA
  - High-power isolation, compact package
  - UL 94 V0 flame-retardant ground insulation
  - 100% hipot tested @ 4.0 kV RMS
  - UL recognized Class H (180°C) insulation system
  - 25-amp rated 5-mil copper screen
  - IEC Touch-safe Eurostyle-type terminals
- Agency approvals: (HPI-20, 27, 35) VDE 0550, UL 506, UL 2601-1, CSA C22.2 #66 1988; (HPI-12, 15, 17) TUV Rheinland, EN 60950 / IEC 950, CSA C22.2 #66 1988, NRTL / C ANSI UL 506

See Specs: [www.signaltransformer.com/HPI/ed](http://www.signaltransformer.com/HPI/ed)

### International Standards at Lower Cost and Better Performance

A41 Series—transformers provide the high isolation, creepage, and clearance necessary to comply with international safety standards.



- Chassis mount isolation and distribution
  - UL 94 V0 flame-retardant, double-reinforced insulation
  - 25 to 175 VA
  - 100% hipot tested @ 4 kV RMS
  - UL recognized Class F (155°C) insulation system
- Agency approvals: UL 506, VDE 0805 / EN60950 / IEC 950, CSA C22.2 #66 1988; also designed to meet construction requirements of IEC 601-1, IEC 65, IEC 1010, UL 478, 544, 1411, 1563, 1585, 2601-1

See Specs: [www.signaltransformer.com/A41/ed](http://www.signaltransformer.com/A41/ed)

### Low Profile Direct Plug-in Replacement for Industry Standard Pin Configuration

LPI Series—low profile pin compatibility with North American industry standards.



- 2 to 18 VA (12 and 18 pending)
  - UL recognized Class B (130°C) insulation system
  - Hermetically sealed and 100% board washable
  - Ridged pins for reliable board insertion
  - 100% hipot tested @ 4.0 kV RMS
- Agency approvals: TUV Rheinland EN60950 / IEC 950, CSA NRTL / C22.2 #66 1988, ANSI / UL 506; also designed to meet construction requirements of UL 478, 544, 1411, 1563, 1585, 2601-1, EN60742, IEC 601-1, IEC 1010

See Specs: [www.signaltransformer.com/LPI/ed](http://www.signaltransformer.com/LPI/ed)

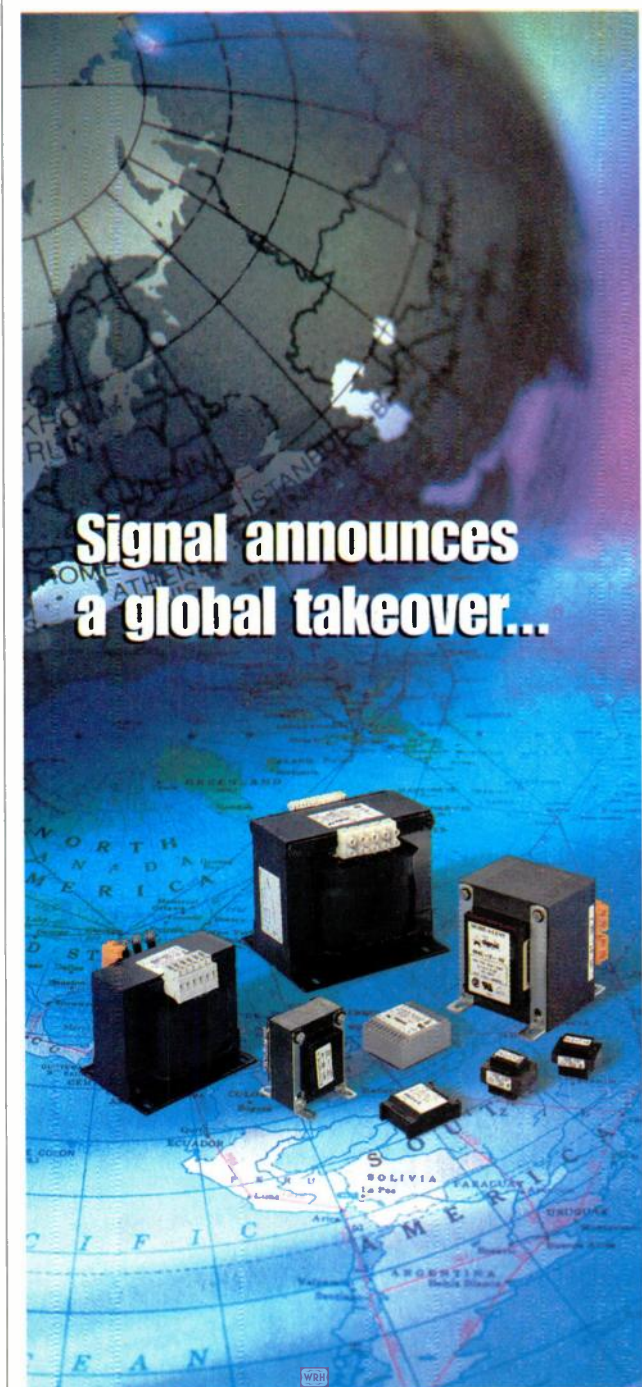
### For Critical Height and International Safety Requirements

IF Series—fully encapsulated, low profile transformers with international mounting format.



- 2 to 30 VA
  - UL recognized Class B (130°C) insulation system
  - Passes VDE dust test
  - 100% hipot tested @ 4.0 kV RMS
  - 100% board washable
  - Double-reinforced insulation
- Agency approvals: VDE 0805 / EN60950 / IEC 950, CSA C22.2 #66 1988, UL 506; also designed to meet construction requirements of UL 478, 1411, 1563, 1585, 2601-1, EN60742, IEC 601-1, IEC 742, IEC 65, IEC 1010

See Specs: [www.signaltransformer.com/IF/ed](http://www.signaltransformer.com/IF/ed)



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- The 14A Series for low-power PC-board applications.
- The LPI Series is a superior pin-to-pin replacement of industry-standard, low-profile transformers.
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## Electronic Nose Technology Enables Sub-Second Smell

**C**yrano Sciences, Pasadena, Calif., has developed a portable, inexpensive technology that's adaptable to practically any odor-detecting task. It's much like the complex system of receptors and neurons that "fingerprint" and store electrical signatures to the brain in the human nose. The essentially limitless number of different patterns generated by combinations of unique polymers enables the company to offer a wide range of odor-detection capabilities from one technology base. The technology was demonstrated at this year's ISA Expo Show held in Houston, Texas.

Using a broadly tuned array of sensors, the technology offers minimal (currently sub-second) cycle time, is able to detect multiple odors, can work in almost any environment without special sample preparation or isolation conditions, and doesn't require advanced sensor design or cleansing between tests. Cyrano Sciences is the worldwide exclusive licensee of the patented original electronic nose technology, developed by professors at the California Institute of Technology.

The underlying principle of the electronic nose is simple. An array of sensors, consisting of dispersed conductive particles within organic polymers, expands like a sponge when it comes in contact with a vapor, increasing the resistance of the composite. The normalized change in resistance then is transmitted to a processor to identify the type, quantity, and quality of the odor based on the pattern change in the sensor array.

Polymers swell to varying degrees because of their unique response to different vapors. Regardless of whether an odor results from a complex mixture of chemicals in vapor or from a single chemical, the technology contains enough polymer arrays to yield a distinct electrical "fingerprint" for each vapor. In the end, the pattern of resistance changes on the array is diagnostic of the vapor, while the am-

plitude of the patterns indicates the concentration of the vapor.

Cyrano Sciences is in product development discussions with several companies. The company plans to introduce its first handheld model by the end of this year. A product is expected to follow by the next calendar year.

For more details, contact Steven Sunshine, president of Cyrano Sciences at (626) 744-1700; fax (626) 744-1777; [www.cyranosciences.com](http://www.cyranosciences.com). JC

## Data-Acquisition Standard Targets Interoperability

**A** group of PC-based data-acquisition product manufacturers recently formed a new association, the Open Data Acquisition Association (ODAA). Its objective is to provide users of data-acquisition systems

with a universal, open standard. The purpose of this standard, called the Open Data Acquisition Standard, is to achieve interoperability between hardware and software products from multiple vendors.

The specification defines a software interface for PC data-acquisition hardware. This interface functions as a standard software driver for PC-based data-acquisition products. There are separate software specifications for the five primary subsystems found on most data-acquisition hardware: Analog In, Analog Out, Digital In, Digital Out, and Counter/Timer. The specification is based on Microsoft COM (Component Object Model) based driver technologies, rather than any one vendor's current software implementation.

Programmers have several choices when writing software to use with PC-based data-acquisition hardware. They can write in their computer language of choice, such as Visual Basic



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Founding members of the ODAA are OMEGA Engineering, Inc., Andover, Mass.; Hewlett-Packard Co., Palo Alto, Calif.; LABTECH Corp., Andover, Mass.; ComputerBoards Inc., Middleboro, Mass.; Data Translation Inc.,

Marlboro, Mass.; and Strawberry Tree Inc., Sunnyvale, Calif.

Any company who designs and manufactures data-acquisition hardware and software products are invited to join the association and utilize the Open Data Acquisition Standard specification. Questions about how to become a member of the ODAA can

be directed to John Coschigano, OMEGA Engineering, by phone at (203) 359-7808; or by e-mail at [coschigano@omega.com](mailto:coschigano@omega.com). More information on this group can be obtained from the association's web site located at [www.opendaq.com](http://www.opendaq.com). JD

## Transistors Created On Silicon Sphere Solve Space Woes

Being able to fabricate a transistor on a 1-mm diameter sphere of silicon puts Ball Semiconductor Inc., Allen, Texas, one step closer to being able to produce diodes, transistors, circuits, and certain types of sensors on a spherical shape. What this means is a compact form factor for functions that might otherwise require many square millimeters of lateral area.

The process used to form the transistor combines traditional and company-unique semiconductor manufacturing processes. Researchers were able to fabricate a large NMOS transistor with a 5- $\mu$ m gate that had electrical characteristics comparable to those of a transistor formed on a traditional planar substrate. The next challenge will be to fabricate a simple integrated circuit on a sphere.

To create the spherical structure on the ball, researchers had to generate the mask data. Then they fabricated the structures with a combination of atmospheric chemical vapor deposition, high temperature oxidation (1250°C), spherical resist coating, spherical lithography, etching, and finally probe testing.

Unique to Ball Semiconductor are the spherical processing steps. For one, the spherical lithography makes it possible to align and expose six individual masks onto the sphere. Also, there's the resist coating process, in which the 1-mm spheres drop through an 8-m tube through a "soap bubble" of coating material and then dry within one second. Furthermore, the company had to develop the atmospheric CVD process to deposit material on the sphere's surface. Check out [www.ballsemi.com](http://www.ballsemi.com) for more info. DB

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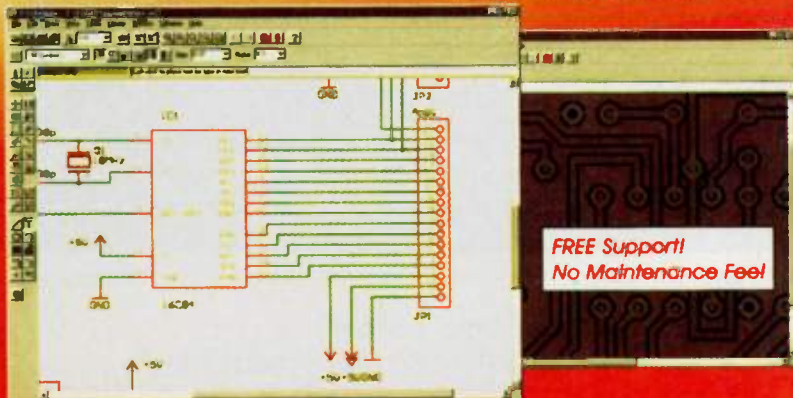
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# Winter



# UNITRODE

## Highlights

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Issue 7

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### UCC3958

The UCC3958 single cell lithium-ion battery protection circuit enhances the useful operating life of single-cell rechargeable lithium-ion battery packs. The device is ideally suited to portable equipment utilizing single-cell lithium-ion battery packs, such as cell phones, pagers and PDAs.

[www.unitrode.com/products/portable/ucc3958.htm](http://www.unitrode.com/products/portable/ucc3958.htm)

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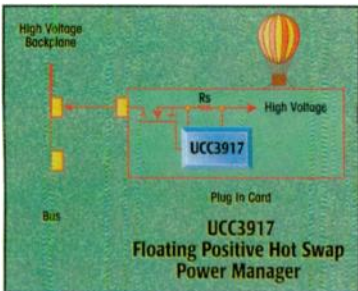


### UCC3882

The UCC3882 Synchronous Buck Controller includes functionality to meet Intel VRM specifications. This product is usable in a wide variety of high performance, low output voltage DC/DC applications, and offers superior load-sharing capability for modular solutions. The UCC3882 is available in a small footprint TSSOP package.

[www.unitrode.com/products/powsup/ucc3882.htm](http://www.unitrode.com/products/powsup/ucc3882.htm)

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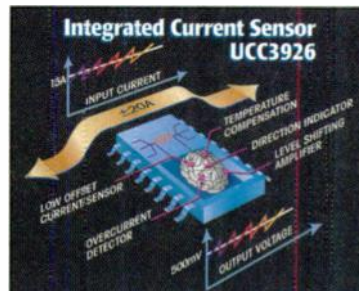


### UCC3917

The UCC3917, part of Unitrode's family of positive hot swap power managers, features a unique floating topology to allow essentially unlimited voltage operation. The device is designed for high voltage communication and EDP equipment, and is ideal for high voltage and high power hot swap power management.

[www.unitrode.com/products/hotswap/ucc3917.htm](http://www.unitrode.com/products/hotswap/ucc3917.htm)

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### UCC3926

The UCC3926 converts up to  $\pm 20$  Amp current through an internal non-inductive shunt resistor into a proportional voltage. The current to voltage conversion is done with a low offset, high bandwidth, temperature compensated amplifier and a second programmable gain amplifier.

[www.unitrode.com/products/powsup/ucc3926.htm](http://www.unitrode.com/products/powsup/ucc3926.htm)

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### bq2000

Unitrode's bq2000 8-pin low-cost switching charge-control IC provides chemistry-independent and high-accuracy charge management for both lithium-ion and nickel-based rechargeable batteries. Applications include cellular telephones, portable PCs, digital cameras, and other consumer electronics.

[www.benchmark.com/prod/bq2000.html](http://www.benchmark.com/prod/bq2000.html)

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### bq2060

Unitrode's bq2060 Smart Battery System v1.0 compliant Gas-Gauge IC monitors critical battery pack parameters, controls a battery's fast charge, and communicates information to the host system. Advanced features include single-cell voltage monitoring, adaptive capacity adjustment and backup safety control for Li-Ion systems.

[www.benchmark.com/prod/bq2060.html](http://www.benchmark.com/prod/bq2060.html)

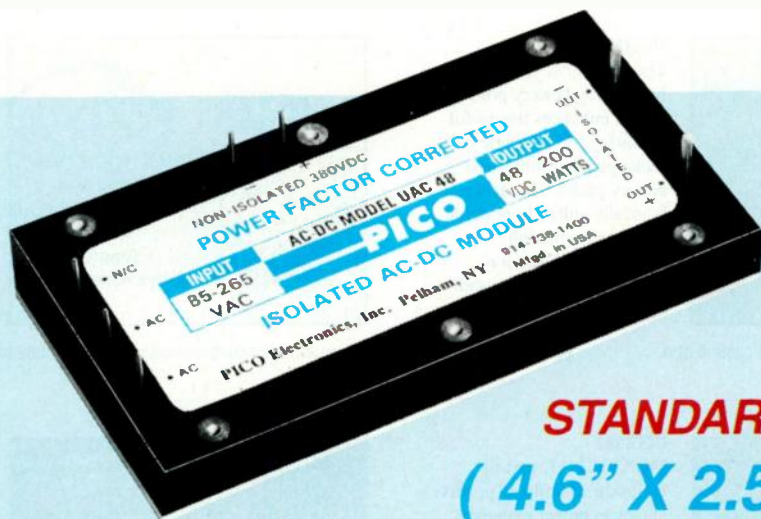
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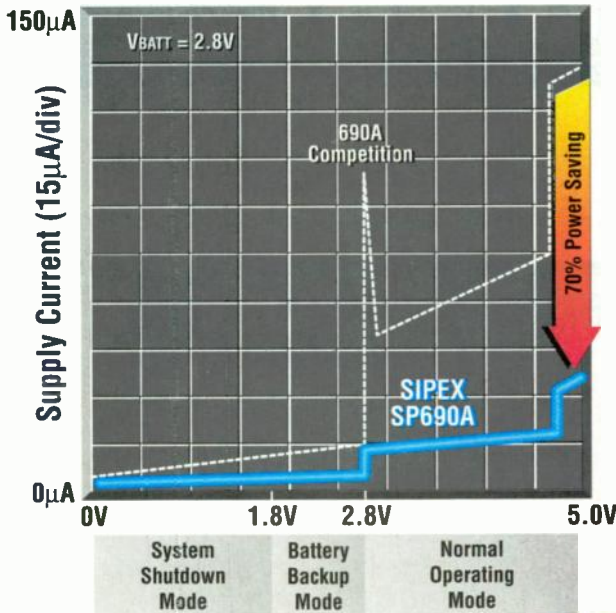
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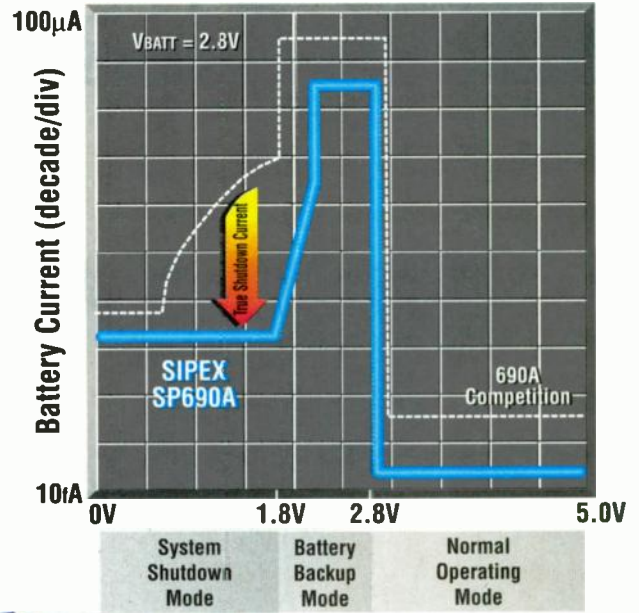
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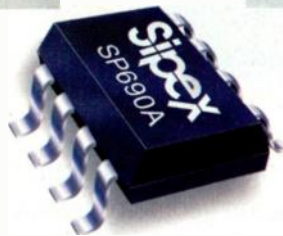
$V_{CC}$  vs. Supply Current



$V_{CC}$  vs. Battery Current



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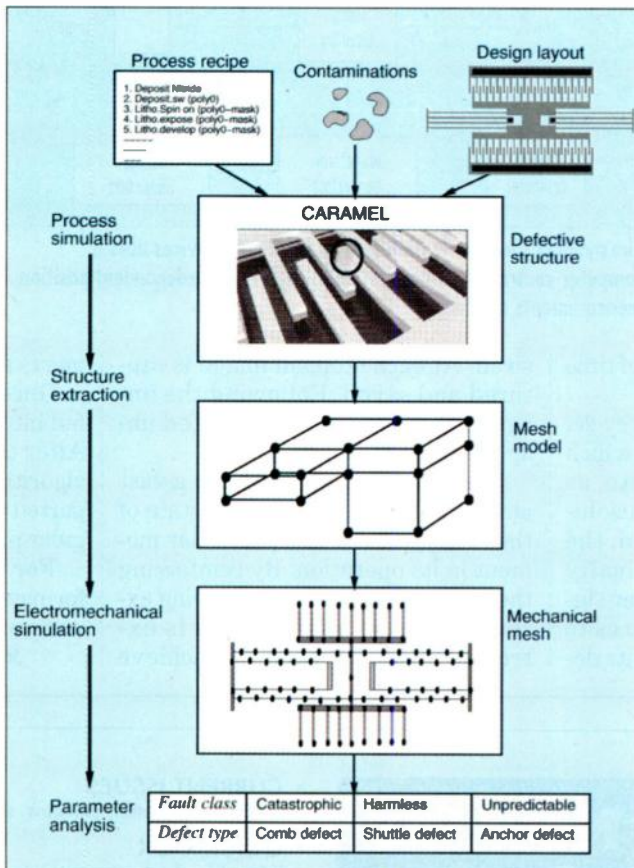
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# Process Simulator Analyzes The Impact Of Contamination On MEMS Layouts

Mapping particle contaminations to defective microstructures with a process simulator may help designers to analyze the impact of this type of contamination on the layout of microelectromechanical systems (MEMS). The new simulator is called CAMEL (contamination and reliability analysis of microelectromechanical layout). It is built around a tool called CODEF, a contamination-to-defect-to-fault mapper for pure electrical layouts.

According to the developers of CAMEL, Abhijeet Kolpekwar, Chris Kellen, and R. D. Blanton, all of Carnegie Mellon University, the success of any testing methodology is highly dependent on the fault models employed. Fault models that do not cover real defective behavior can reduce defect coverage and degrade test quality. MEMS fault models, unlike their digital and analog counterparts, must explicitly consider the impact of defects on the micromechanical structures. The trio presented their work at the International Test Conference, Washington, D.C., in October.

CAMEL is an integral compo-



The CAMEL process simulator requires three inputs to analyze particle contamination of a MEMS layout: the process recipe, contaminations, and the design layout.

nent of the authors' MEMS fault model generation (see the figure). The simulator requires three inputs:

- *Design definition:* Typically, this

is a layout of the design in the Caltech intermediate form (CIF).

- *Process definition:* This includes a sequence of process steps with all the required details, such as deposition thickness, etching rate, etching time, etc.

- *Contamination definition:* This consists of the geometrical and material characteristics of the particulate contamination, its location in the MEMS layout, and the process step in which it was introduced.

CAMEL performs process simulation and creates a three-dimensional representation of the defective microelectromechanical layout. From that defective layout, it then extracts a mesh representation whose form is completely compatible with the mechanical simulator, Abaqus. By mechanically simulating the mesh, the user can link the contamination of concern to a defective structure and faulty behavior. Observed faulty behaviors are classified and used to form models at the next level of abstraction. Monte Carlo iteration around the flow shown in the figure then provides a mechanism for creating realistic fault models for MEMS.

For more information about CAMEL, contact the ECE Department at Carnegie Mellon University, Pittsburgh, PA.

**Joseph Desposito**

# MEMS Performance-Analysis System Uses Automated Video-Imaging Techniques

Researchers at Sandia National Laboratories, Albuquerque, N.M., have devised a dynamic characterization system for microelectromechanical systems (MEMS). Based on the capture and analysis of video images, the Performance Analysis System uses stroboscopic illumination to facilitate the collection of time-dependent position measurements.

Instead of tracking all device features, the system quickly traces key device topological features. It boasts a high degree of accuracy under varying illumination conditions and in the presence of background interferences, such as motion drift in the test setup.

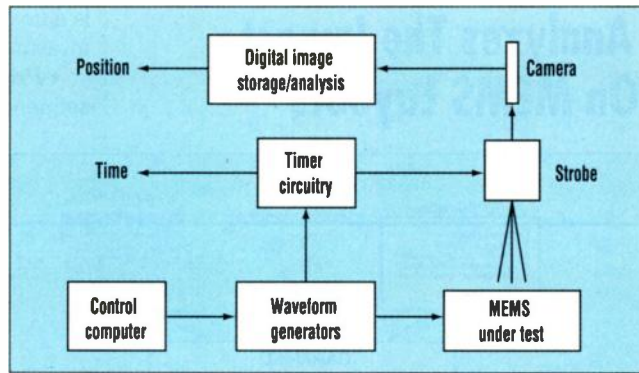
The figure on the next page shows the basic operational flow of the Performance Analysis System, which was

described in a paper presented by Glenn F. La Vigne and Sam L. Miller at the International Test Conference in Washington, D.C., this past October. The system consists of a central computer that controls a strobe light source, a video camera, waveform generators, and digital timer circuitry. The computer system creates the drive signals to run the MEMS device under test. These are then downloaded to the waveform generators.

The control computer also generates a trigger marker at the start of each cycle of the drive signals. This

trigger is fed into the timer circuitry. By performing a divide-by-N function, the timer circuitry steps down the signal—possibly from the multiple kilohertz range—to the operational range of the strobe light. Also in the timer, the divided trigger signal is time-delayed by an amount dictated by the control computer. This pulse triggers both the strobe and the acquisition of a video image. By adjusting the strobe light phase relative to the start of the periodic drive signal, the position of the images as a function of time is directly determined.

In a typical data-acquisition cycle, the user sets the frequency at which the MEMS device is to operate, as well as the desired position resolution for the data. Once started, the control computer automatically changes the delay on the trigger signal in fixed increment steps so as to acquire the number of data points de-



**The dynamic characterization system for MEMS devices uses a computer-controlled strobe system to capture time-dependent position measurements on video.**

sired. At each step, an image is captured and saved. Following the image-capture process, automated image analysis is performed.

These video images contain a vast amount of information on the state of the MEMS device at a particular moment in its operation. By reinforcing the desired features and removing extraneous information, data is extracted from the images. To achieve

this, the images are fed through a series of image-processing filters.

For example, to characterize the rotational motion of a microengine, it's necessary to find two unique points: one on the rotating surface, and the other point on a stationary surface. For the Sandia microengine, the center hub and the gear/drive linkage provide such points. A series of contrast enhancement and binary morphological filters accents these features and removes unnecessary elements from the images.

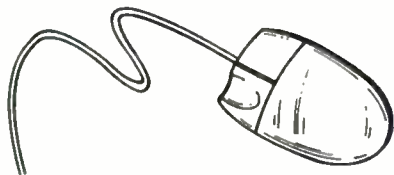
Once filtered, the image series is fed into a template search algorithm. After this is done, additional analysis algorithms convert x-y coordinates reported by the search algorithm to an angular position versus time data set.

For more information on the Performance Analysis System, check out [www.mdl.sandia.gov/Micromachine](http://www.mdl.sandia.gov/Micromachine).

**Joseph Desposito**

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AD7417	4	I <sup>2</sup> C	$\pm 1$	0.2 mW @ 1 kSPS	2.95	SOIC, TSSOP	16
AD7817	4	SPI	$\pm 1$	3.0 $\mu$ W @ 10 SPS	2.95	SOIC, TSSOP	16
AD7418	1	I <sup>2</sup> C	$\pm 2$	0.2 mW @ 1 kSPS	2.25	SOIC, $\mu$ SOIC	8
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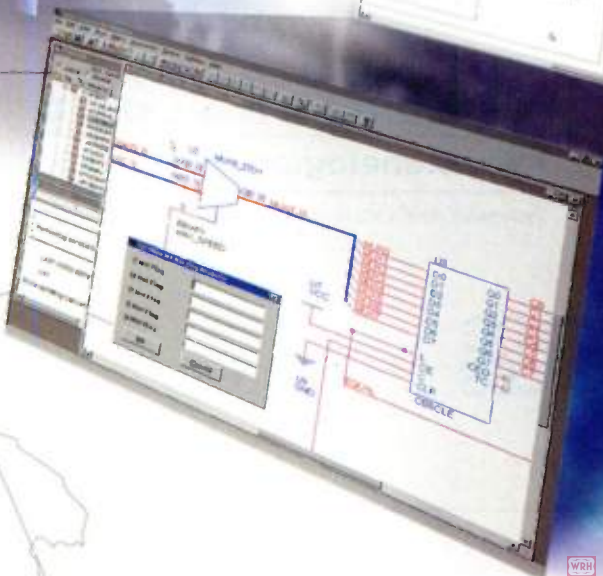
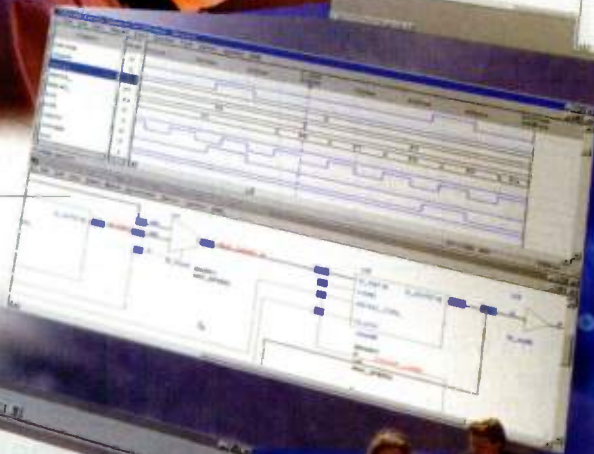
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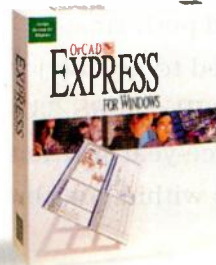
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## Versatile AWGs Tackle New Digital Modulation And MEMS Testing

*Greater Speed, Deeper Memory, Lower Cost, And More Flexibility Make Arbitrary Waveform Generators "Must Have" Items.*

Joseph Desposito

As electronic signals become faster and more complex, design engineers are demanding arbitrary waveform generators (AWGs) that are more powerful, easier to use, and less expensive. To meet these needs, a new crop of AWGs are offering faster sampling rates, deeper memories, improved software, and other goodies—at competitive prices. This doesn't mean older models are becoming obsolete. Instead, some AWGs and arbitrary function generators (AFGs) introduced a few years ago are still the mainstays of some companies' product lines. After all, many engineers still have to deal with the same signals they have worked with for years.

Several forces are driving the market for AWGs. One is performance. According to Chris Martinez, worldwide business development manager for Tektronix' Measurement Business Division, Beaverton, Ore., "Continued advancements in the performance of all types of digital equipment, the emergence of more complex industry standards, and the ever-present pressures to shorten product development cycles are increasing the demand for AWGs." Tektronix responded to these challenges earlier this year by introducing its AWG 500 series of arbitrary waveform generators.

Another market force favoring AWGs and AFGs is the movement



away from older function generators—sine, square, and triangle waves—to the more flexible AWGs. Hewlett-Packard (HP), Palo Alto, Calif., is one company capitalizing on this trend. According to Cheryl Diller, product manager for signal sources at HP's Electronic Measurements Division, "Customers are realizing that they can now buy what I like to call multipurpose function generators—function generators that include AWG and pulse capabilities—at the same or often a lower price than their previous function generator. Yet, customers are still using AFGs primarily as a function generator if they were previously using that instrument. So, they're buying

these multipurpose AWG systems to fill their old needs."

Diller continues, "Sometimes customers wonder if they could get the instrument at a lower cost if it did not have the arbitrary waveform capability. But, fundamentally, the hardware is there. We're writing firmware to provide greater access to the hardware so customers can download their own waveforms."

New applications also play a part in increasing the demand for AWGs. Take, for example, microelectromechanical systems (MEMS). One company with experience in this area is Pragmatic Instruments Inc., San Diego, Calif., "MEMS is a unique application where you really need a good sequence generator," says Henry Reinecke Jr., Pragmatic's president. "Generally, to operate a MEMS accelerometer, there is sort of a startup curve where you have to apply acceleration, since the device is typically at a standstill. There is an accelerate portion, and then a constant velocity or constant rotation portion, which can be at different speeds. Therefore, you have different sample lengths for the different speeds or velocities. Then, there's generally a deceleration waveform. For all of these to be seamless, they have to be stored in the memory of the AWG with a sequence generator capable of calling

## ARBITRARY WAVEFORM GENERATORS

Manufacturer	Model/price	Vertical resolution (bits)	Maximum sampling rate (Msamples/s)	Waveform memory (points)	Number of channels	Maximum amplitude (V p-p)	Remarks
Analogic Corp. 8 Centennial Dr. Peabody, MA 01960 (978) 977-3000 fax (978) 977-6814 e-mail: jlong@analogic.com www.analogic.com	DBS8751A \$3770	16	0.2	64k per ch.	4	12	C-size VXI module
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	DBS8750 \$4190	16	0.4	32k per ch.	2	20	C-size VXI module; math entry capability
	2030/\$4195	12	50	256k	1	10	
	2020-100 \$9495	12	100	512k	1	10	Math entry capability
	2040/\$13.995	8	800	512k	1	1	Math entry capability; true and inverted outputs; 1 Gsamples/s opt.; 2-Mpoint memory opt.
	2045/\$13.995	8	800	512k	1	5/1*	Math entry capability; 1 Gsamples/s opt.; 2-Mpoint memory opt.; *5-V output at 400-MHz bandwidth
Berkeley Nucleonics Corp. 3060 Kerner Blvd., #2 San Raphael, CA 94901-5418 (415) 453-9955 fax (415) 453-9956 e-mail: berkeley@berkeley-nucleonics.com www.BerkeleyNucleonics.com	625A/\$995	12	40	32k	1	5	Multi-unit phase lock capability
Datel Inc. 11 Cabot Blvd. Mansfield, MA 02048 (508) 339-3000 (800) 233-2765 fax (508) 339-6356 www.datel.com	PC-423/\$1250	12	1	1k per ch.	4	10	ISA bus card; four independent channels; four 16-bit digital pattern generators; Delphi Windows virtual instrument software, \$95; \$1495 with 8k/ch. memory
	PC-420/\$1645	12	40	32k per ch.	2	10	ISA bus card; two simultaneous channels; external clock, trigger, and gate; eight software programmable output filters; Virtual Basic software, \$95; LabVIEW drivers, \$50
Hameg Instruments Inc. 266 East Meadow Ave. East Meadow, NY 11554 (800) 247-1241 fax (516) 794-1855 e-mail: hameg@aol.com www.hameg.com	HM8130 \$1110	10	10	1024	1	10	Trigger output; sine, square, pulse, and ramp functions; AM modulation; RS-232, \$235; IEEE-488, \$285
	HM8131 \$1488	12	40	4k	1	10	Sine, square, ramp, and triangle functions; AM, phase, FSK/PSK modulation; RS-232, \$235; IEEE-488, \$285
Hewlett-Packard Co. Direct Marketing Org. P.O. Box 58059 MS51L-SJ Santa Clara, CA 95051-8059 (800) 452-4844 www.tmo.hp.com	HP 33120A \$1795	12	40	16,000	1	10	Direct digital synthesis; nine built-in waveforms plus dc; stores four 16,000 point waveforms; linear and log sweeps; AM, FM, FSK, and burst modulation; IEEE-488, RS-232 std.; waveform generation software, \$300; can lock multiple units together with option 001, \$403
	HP E1340A \$2680	12	92	16k	1	10.2 (20.4 using E1446)	B-size VXI module; direct digital synthesis; includes seven standard waveforms; sweep, FSK, and burst capability; sine, square, ramp, triangle, sine(x)/x, noise and haversine; can store four waveforms in active memory
	HP E1441A \$2850	12	40	16,000	1	10	C-size VXI module; 11 standard waveforms; AM, FM, FSK and burst modulation; option 001, \$395; includes high stability time-base with PLL and TCXO
	HP 3245A \$5495	12	4	2k	1	10	Arbitrary voltage and current, dc, ac source; 24-bit dc voltage and current resolution; second channel, \$3495; 10X voltage amplifier, \$1590

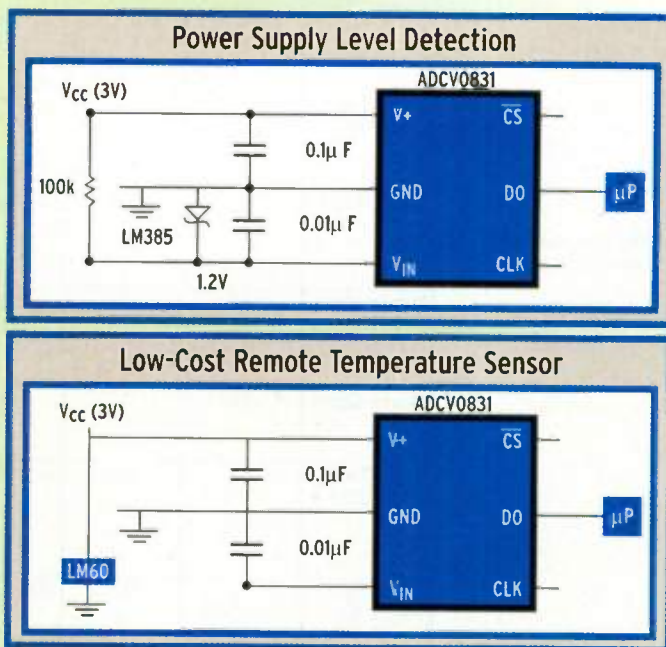
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	LW420A \$18,950	8	400	256k	2	10	Same as LW410, but with two channels
National Instruments 11500 N. Mopac Expwy. Austin, TX 78759-3504 (512) 794-0100 fax (512) 794-8411 info@natinst.com www.natinst.com	NI 5411 \$3495	12-bit	40	4M	1	10	PCI or ISA bus; VirtualBench-Arb and VirtualBench-FG software
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Pragmatic Instruments Inc. 7313 Carroll Rd. San Diego, CA 92121-2319 (619) 271-6770 fax (619) 271-9567 e-mail: awgsales@pragmatic.com www.pragmatic.com	2711A \$1995		2	64k	1	10	WaveWorks Jr. software, RS-232, IEEE-488 std.; sequence generator opt., \$695
	2714A/\$1995	12	20	128k	1	10	Same as 2711A
	2411A/\$2495	16	2	64k	1	10	RS-232 std., IEEE-488, \$395; sequence generator, \$695; WaveWorks Pro software (Windows), \$495
	2414A/\$2495	12	20	128k	1	10	Same as 2411A
	2416A/\$2695	12	100	64k	1	10	IEEE-488 and sequence generator std.; WaveWorks Pro software
	3511A/\$2695	16	2	64k	1	10	RS-232, HarmonicLink (GUI) software std.; IEEE-488, \$395; sequence generator, \$695
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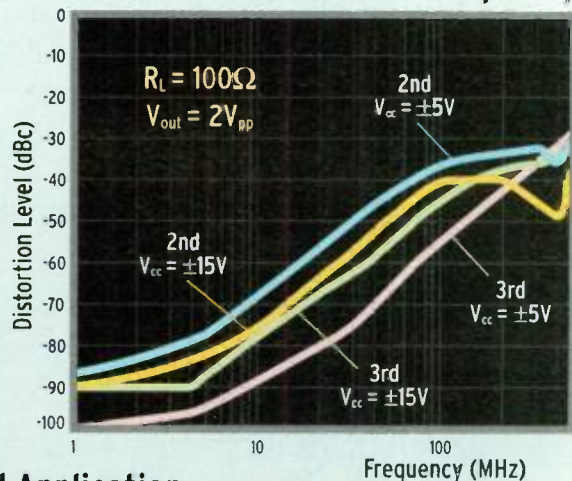
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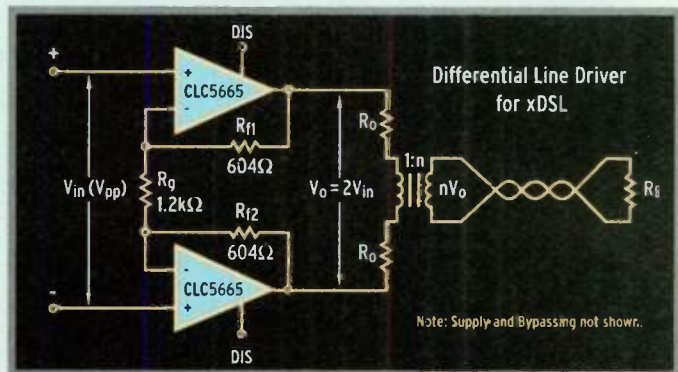
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## ARBITRARY WAVEFORM GENERATORS

Manufacturer	Model/price	Vertical resolution (bits)	Maximum sampling rate (Msamples/s)	Waveform memory (points)	Number of channels	Maximum amplitude (V p-p)	Remarks
Racal Instruments Inc. 4 Goodyear St. Irvine, CA 92618 (800) 722-2528 (949) 859-8999 fax (949) 859-7139 www.racalinst.com	3161/\$9495	12	300	256k	1	5	C-size VXI card; phase lock, counter, phase and amplitude modulation; frequency hopping; D-sub waveform control; 1-to-4M waveform memory points opt.
	3171/\$10,950	12	80	128k per ch.	3	22	C-size VXI card; one AWG ch. and two 50-MHz pulse channels
	3162A \$13,450	12	500	1M	1	5	C-size VXI card; 500 Msamples/s version of 3161; 4M waveform memory points opt.
	3162B \$22,450	12	500	1M per ch.	2	5	C-size VXI card; two-channel version of 3162A; can generate I&Q signals
Stanford Research Systems 1290-D Reamwood Ave. Sunnyvale, CA 94089 (408) 744-9040 fax (408) 744-9049 e-mail: info@srsys.com www.srsys.com	DS340/\$1195	12	40	16,300	1	10	Arbitrary waveforms; sine, square, ramp, and triangle waveforms; lin-
	DS345/\$1595	12	40	16,300	1	10	Arbitrary waveforms; sine, square, ramp, and triangle waveforms; linear and log sweeps; amplitude, frequency, phase, burst, and arbitrary modulation
Tektronix Inc. Measurement Business Div. P.O. Box 3960 Portland, OR 97208-3960 (800) 426-2200 e-mail: info@tek.com www.tektronix.com	AFG 310 \$1895	12	16	4 by 16k	1	10	Function and arbitrary waveform generator; direct waveform transfer via GPIB from all Tektronix scopes; waveform editing software included
	AFG 320 \$2695	12	16	4 by 16k	2	10	
	VX 4790A \$3825	12	25	256k	1	10	C-size VXI card; waveform sequencing; 512-kbyte and 1-Mbyte memory options; programmable output attenuator
	AWG 2005 \$8495	12	20	64k	2 or 4	10	Digital editor for data generation; waveform sequencing; GUI waveform editing; options: frequency sweep, four channels, 24 digital outputs
	AWG 2021 \$11,995	12	250	256k	2	5	Digital editor for data generation; waveform sequencing; GUI waveform editing; options: two channels, 12 or 24 digital outputs
	AMIQ \$14,950	14	100	4M per ch.	2	1	Includes WinIQSIM software for W-CDMA, IS-95 and multicarrier signal detection
	AWG 510 \$21,995	10	1000	4M	1	2 (4-V differential)	Digital editor for data generation; waveform sequencing; GUI waveform editing; options: 4-Mbyte record length; 10 digital outputs
	AWG 520 \$28,995	10	1000	4M	2	2 (4-V differential)	Same as AFG 510
Telulex Inc. 2455 Old Middlefield Way S. Mountain View, CA 94043 (650) 938-0240	SG-100A \$1295	12	40	32k	1	10	fax (650) 938-0241 e-mail: sales@telulex.com www.telulex.com
Wavetek Corp. 9045 Balboa Ave. San Diego, CA 92123 (800) 854-2708 (619) 279-2200 fax (619) 450-0325 e-mail: testsupport@wavetek.com www.wavetek.com	29/\$1295	10	27	1024	1	10	Frequency hopping, AM and FSK
	39/\$1695	12	30	64k	1	10	Pulse, sequencing, frequency hopping, AM, sweep
	395/\$3995	12	100	64k	1	10	Pulse, noise, AM, FM; RS-232; IEEE-488 opt.; 256k memory opt.
	1375/\$4795	12	20	32k	1	10	C-size VXI card; 128-kpoint memory, \$295; 512-kpoint memory, \$395
	1385/\$6395	12	50	128k	1	11	C-size VXI card; floating main output; 512-kpoint memory, \$395
	1396/\$6395	12	50	512k	1	15	C-size VXI card; 4096 sequences digital output; 2-Mpoint memory opt.
	296/\$7995	12	50	512k	1	15	4096 seq.; dig. out.; 2-Mpoint mem. opt.; up to 4 ind. ch., \$3795 each; 100-V p-p out. into 500 $\Omega$ opt.

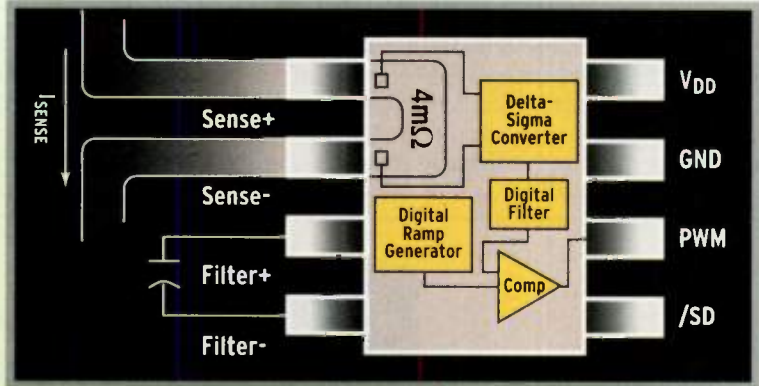


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LM3815-1/7	1A/7A	Low-side	Fast

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them up in a step routine. It's accelerate, then some rpm, then a different rpm, then go from one rpm to another, and then decelerate to go back to a halt."

Another hot application area for AWGs is communications. Reinecke points out that dual-channel AWGs are often needed for communications, especially for in-phase and quadrature (I&Q) modulation. "Most of the digital modula-

tion is of the I&Q form," says Reinecke. "You need two channels and, in general, the clocks have to be very close together—clocks without any skew. Then, you need sample rates normally between 5 and 10 Msamples/s. And the two channels often contain a packet of information; therefore, you need relatively long memories. For IS-95 CDMA, 26.7 ms is the total message length. For wideband CDMA, it's about 10 ms."

Reinecke adds: "When you factor that out at 5 or 10 Msamples/s, you need a lot of memory to get one packet in the instrument. Data typically is generated by means of some software program like SystemView from Elanix Inc. (Westlake Village, Calif.). They have a very comprehensive software package for doing most of the communications file generation. Then the files are downloaded into the memory, and they simply play back out of the memory. There isn't much for the instrument to do other than receive the file and play it back consistently at the data rates required."

### Latest AWG Features

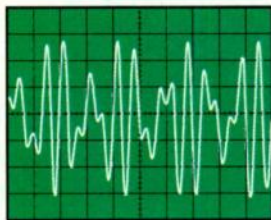
So how are the current crop of AWGs distinguishing themselves in the marketplace? In the case of the AWG 500 from Tektronix, one compelling feature is digital outputs. This feature targets the digital designer and mixed-signal applications.

"We've actually added in this hardware capability for people working on semiconductors who need to have both analog and digital signal control," says Bruce Virell, product marketing manager. "Tektronix actually pioneered this capability; it's in all of our AWGs. The newer instruments provide more specific tools for design engineers in digital applications—things like channel-to-channel skew control and independent amplitude control on the digital output. It's been an evolution of the products."

Another new feature of the AWG 500 series is an integrated hardware noise generator that's capable of generating truly random white noise. Why did Tektronix include this feature? According to Mike Phipps, U.S. business development manager, "We made a number of field visits to customers and looked at their applications. It's pretty obvious to us when the customer has an AWG connected up to an external noise source. They didn't have to tell us this would be a good feature to build into our product."

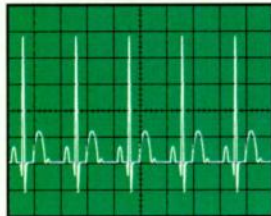
At LeCroy, Chestnut Ridge, N.Y., the LW410A and LW420A are the mainstays of the company's AWG product line. "People like them pretty much the way they are," notes Mike Lauterbach, director of product management. "We did increase the size of the hard drive built into the AWGs. Two reasons: Larger hard drives became much cheaper, and designers are creating more long, complicated waveforms. So,

# Three Lab Sources



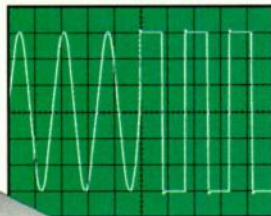
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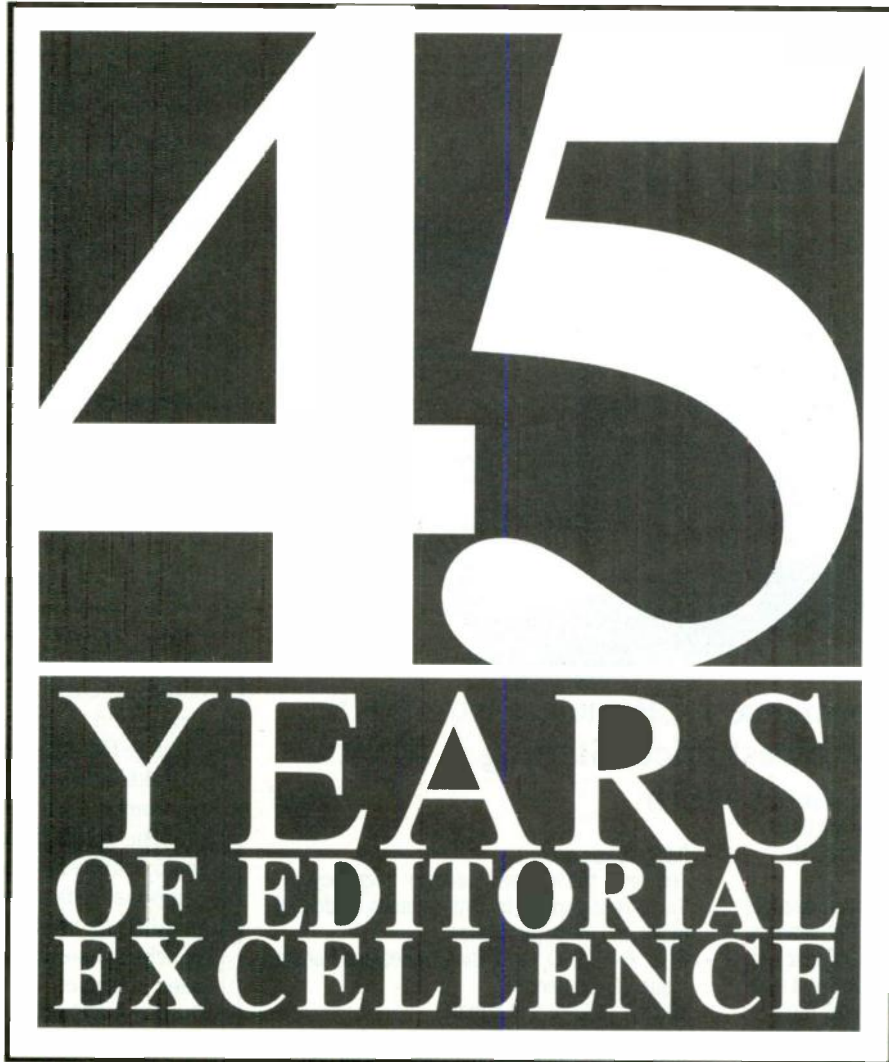
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they want larger hard drives."

According to LeCroy's product manager, Fred Lauricella, the most significant change recently is the sample clock. It is now continuous from 6 kHz to 400 MHz with 1-Hz resolution. "That was a big request," notes Lauricella. "There used to be bands of allowed clock rates to output the waveform; it wasn't continuously variable. If a designer wanted to create a 92.8-MHz signal for some

GSM test, it couldn't be done. But now, the AWG is continuously variable."

### PC-Based AWGs

AWGs on plug-in cards have been around for a while, predominantly for the VXI platform. Last year, however, National Instruments (NI), Austin, Texas, announced an AWG card for the PC, the NI 5411. This card comes in two flavors: one for the PCI bus, and the

other for the ISA bus. Usually, a computer-based or plug-in type AWG is designed into an automated test or automated stimulus system. But this isn't always the case.

Ed McConnell, the strategic marketing manager for computer-based instruments at NI, notes the use of computer-based instruments in university labs. "We're finding that universities want to replace a lot of older instruments with the newer virtual or computer-based instruments, such as AWGs and multimeters. But, the real benefit in a computer-based AWG, be it a VXI-, PXI- or PCI-based AWG, is that you can build test systems that perform the measurement of the stimulus more rapidly than, say, a GPIB-based AWG. Plus, these instruments are easier to integrate in a system, using the instrument drivers and software."

### A Specialty AWG

AWGs are typically general-purpose instruments. But sometimes, a product will be geared to a specific industry. Such is the case with the AMIQ from Rohde&Schwarz, sold in this country by Tektronix. The primary purpose of this AWG is as an IQ modulation source for digital modulation. Although an AWG, it has been designed specifically for the communications industry. It is programmed and set with its own WinIQSIM software.

Tektronix's Virell makes an interesting comparison between the AWG 500 and the AMIQ interfaces. "One of the major differences between our general-purpose instrument and our focused product is that we actually provide benchtop operation through a graphical user interface—a waveform display—for the AWG 500 series. You can see the waveform as it's edited and created.

"One of the early claims to fame of our general-purpose AWGs was the fact that you didn't need software or a controller to create, edit, and output waveforms," says Virell. "You can do all of that right inside the box. The primary reason for having that built-in interface is for on-the-bench debugging—a really popular application. You can download your vectors out of the computer into the AWG and output those signals. But then, if you want to inject anomalies or do debug testing, you can make changes right there in the instrument and automatically update your output."

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OPA244	Wide $V_S$ , Best Speed/Power	S, D	SOT, MSOP	+2.2 to +36	0.040	0.3	1.5	\$0.37
OPA336	CMOS, Precision, <i>microPower</i>	S, D, Q	SOT, MSOP, SSOP	+2.1 to +5.5	0.020	0.1	0.125	\$0.42
OPA337	CMOS, Lowest Cost, Smallest	S, D	SOT (incl. dual!)	+2.5 to +5.5	0.525	3	3	\$0.25
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**Annual Reliability & Maintainability Symposium (RAMS), Jan. 19-21.** Washington Hilton, Washington, DC. Contact V.R. Monshaw, Consulting Services, 1768 Lark Lane, Cherry Hill, NJ 08003; (609) 428-2342.

**Embedded Executive Conference, Jan. 26-27.** La Quinta Resort, Palm Springs, CA. Contact Douglas St. John, Miller Freeman Inc., (415) 538-3848; (888) 239-5563; e-mail; esc@mfi.com; www.embedded.com.

**IEEE Power Engineering Society Winter Meeting, Jan. 31-Feb. 4.** New York, NY. Contact Frank Schink, 14 Middlebury Lane, Cranford, New Jersey 07016; (908) 276-8847; fax (908) 276-8847; ieee.org/power.

**FEBRUARY**

**EcoDesign '99, Feb. 1-3.** Manufacturing Science & Technology Center, Tokyo, Japan. Contact Point Business Center for Academic Societies Japan, 5-16-9, Honkomagome, Bunkyo-ku, Tokyo 113, Japan; +81 3 5814-1440; fax +81 3 5814 1459; e-mail: van@bcasj.or.jp; www.bcasj.or.jp/EcoDesign/.

**Photonics West, February 6-12.** San Jose, CA. Contact SPIE Exhibits Dept., P.O. Box 10, Bellingham, WA 98227-0010; (360) 676-3290; fax (360) 647-1445; e-mail: exhibits@spie.org.

**Seventh Automated Imaging Association (AIA) Business Conference, Feb. 10-12.** Buena Vista Palace, Orlando FL. Contact Kirsten Erickson, (734) 994-6088; e-mail: kerickson@automated-imaging.org.

**IEEE International Solid-State Circuits Conference (ISSCC '99), February 15-17.** San Francisco Marriott, San Francisco, CA. Contact Diane Suiters, Courtesy Associates, Suite 710, 2000 L St., N.W., Washington, DC 20036; (202) 331-2000; fax (202) 331-0111; e-mail: isscc@courtesyassoc.com.

**Gigabit Ethernet Conference (GEC), Feb. 16-18.** San Jose, CA. Contact Conference Pros, P.O. Box 9126, San Jose, CA 95157, (800) 351-6000 or (408) 526-9194; fax (408) 526-9195; e-mail: conference\_pros@compuserve.com; www.geconf.com.

**Portable by Design, February 21-25.** Santa Clara Convention Center, Santa Clara, CA. Contact Rich Nass, Electronic Design, 611 Rte. 46 West, Hasbrouck Heights, New Jersey 07604; (201) 393-6090; fax (201) 393-0204; e-mail: portable@class.org.

**The Wireless Symposium and Exhibition, Feb. 21-25.** San Jose Convention Center, Santa Jose, CA. Contact Bill Rutledge, Penton Publishing, 611 Rte. 46 West, Hasbrouck Heights, NJ 07604; (201) 393-6259; fax (201) 393-6297; instant faxback (800) 561-7469; e-mail: www.penton.com/wireless.

**MARCH**

**Embedded Systems Conference, Spring, Mar. 2-4.** McCormick Place South, Chicago, IL. Contact FS Communications Inc., 888 Villa St., Suite 410, Mountain View, CA 94041; (650) 691-1488; fax (650) 960-0541.

**IPC Printed Circuits Expo '99, Mar. 14-18.** Long Beach Convention Center, Long Beach, CA. Contact IPC (847) 509-9700 ext. 361; fax (847) 509-9798; www.ipc.org/html/expo99.htm; e-mail: registration@ipc.org.

**Southeastcon '99, Mar. 25-29.** Hyatt Regency Hotel, Lexington, KY. Contact Don Hill, 1676 Donelwal Dr., Lexington, KY 40511-9021; (606) 257-8487; fax (606) 323-1034; e-mail: d.w.hill@ieee.org.

**APRIL**

**IEEE/PES Transmission & Distribution Conference & Exposition, Apr. 10-17.** Ernest N. Morial Convention Center, New Orleans, LA. Contact Grace Juneau, c/o Entergy, P.O. Box 61000, New Orleans, LA 70161-1000; (504) 576-2400; fax (504) 576-5989; e-mail: gjuneau@entergy.com.

**41st IEEE Cement Industry Technical Conference, Apr. 11-15.** Roanoke, Virginia. Contact Margaret Peterson, Roanoke Cement Co., P.O. Box 27, Cloverdale, Virginia 24077; (540) 992-1501; fax 966-1542.

**IEEE Radar Conference, Apr. 20-22.** Boston, MA. Contact Robert Alongi, 255 Bear Hill Rd., Waltham, MA 02154; (617) 890-5290; fax (617) 890-5294; sec.boston@ieee.org.

**MAY**

**IEEE/IAS Industrial & Commercial Power Systems Technical Conference (I&CPS), May 3-6.** Nuggett Hotel, Sparks, NV. Contact Kerry Flannigan, Sierra-Nevada Power Co., P.O. Box 10100, Reno, NV 89520; (702) 689-4848; fax (702) 689-4139.

**Sensors Expo Spring '99, May 4-6.** Baltimore Convention Center, Baltimore, MD. Contact (203) 256-4700 ext. 173; www.sensorsexpo.com.

**Sixth IFIP/IEEE International Symposium on Integrated Network Management (IM '99), May 9-14.** Boston Park Plaza Hotel, Boston, Massachusetts. Contact Judy Keller, IEEE/COMSOC, 305 E. 47th St., New York, NY 10017; (212) 705-8248; fax (212) 705-7865; e-mail: j.keller@ieee.org.

**The Robotics and Vision Show, May 11-13.** Colocated with the International Automotive Manufacturing Show and Motion Expo; Cobo Convention Center, Detroit, MI. Contact (203) 256-4700 ext. 173, www.motioncontrol-expo.com.

**JUNE**

**International Symposium on VLSI Technology, Systems, & Applications, June 8-10.** Taipei, Taiwan, R.O.C. Contact Tak H. Ning, IBM T.J. Watson Research Center, Post Office Box 218, Rt. 134 & Taconic Parkway, Yorktown Heights, New York 10598; (914) 945-2579; fax (914) 945-3623; e-mail: ning@watson.ibm.com.

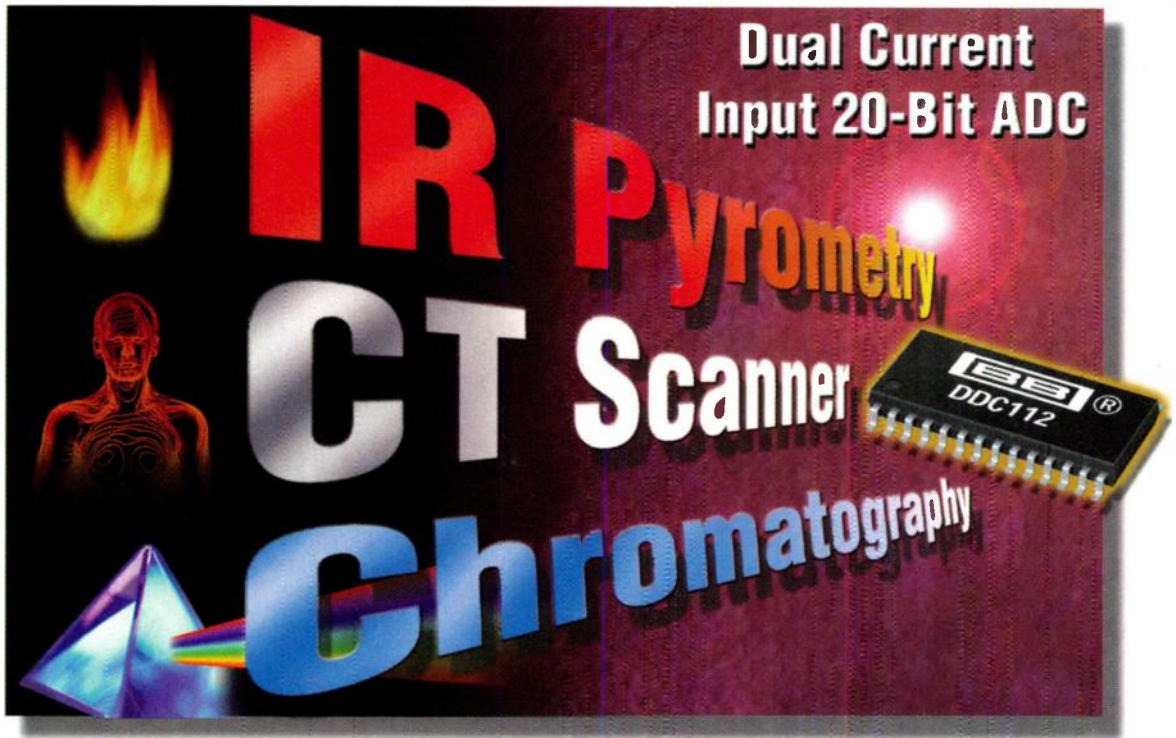
**IEEE/MTT-S International Microwave Symposium (MTT '99), June 13-18.** Anaheim Convention Center, Anaheim, CA. Contact Robert Eisenhart, Eisenhart & Associates, 5982 Ellenview Ave., Woodland Hills, CA 91367; (818) 716-1995; fax (818) 713-1161; r.l.eisenhart@ieee.org.

**JULY**

**IEEE Power Engineering Society Summer Meeting, July 18-22.** Edmonton, Alberta, Canada. Contact Dave Fraser, Edmonton Power Capital Square, Edmonton, Alberta, T5J 3B1, Canada; (403) 448-3554; fax (403) 448-3192.



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The DDC112 is a precision, dual current input, wide dynamic range A/D converter with 20-bit resolution operating from a single supply. It combines the functions of dual current-to-voltage conversion, programmable full-scale range, A/D conversion, and digital filtering—all in a single chip, low cost solution.

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# ELECTRONIC DESIGN QUICKLOOK

■ Edited by Nancy Konish

## MARKET FACTS

### Holographic Market Zooms Out To Hit \$2.8 Billion

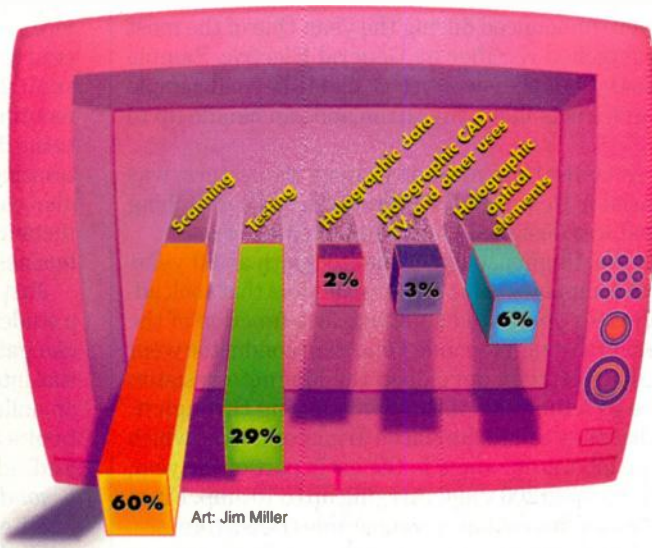
Think of a hologram, and most of us think of characters on science fiction shows that could go on and off with a flick of a button. Holograms appear to have a physical body, but it's just an illusion. They seem like the stuff of the future, along with robots that do our cooking and cleaning and hovercrafts that are available to the average consumer. But the reality is that the holographic market is flourishing right now. Products that are less flashy, but

technically still very vital, are building on the industry's quality. Indeed, holographic elements make lights shine brighter, CD-ROM drives run faster, and machines see better. They can be found in a variety of industrial machines, which results in the making of smaller, cheaper, more efficient machines. These work much faster and with greater precision. Designers use them to create machines and factories digitally, and can then express them as virtual reality in the form of holograms. Though it's not as glorious, another common

everyday representative of industrial holography is in retail scanners for both pricing and reading bar codes. This technology also tracks products from the warehouse and during transportation to delivery. But, what's this market worth? Well, Business Communications Co. Inc., Norwalk, Conn., resolved to answer this same question. The worldwide market for industrial holography is up to \$2.8 billion for this year. Business Communications' study, "RGB-225B Holography for Industrial Applications," reveals a total U.S. market for industrial holographic uses at \$1.7 billion. Many different technologies and products employ holography, and all stand to make more money. Holographic scanning, for instance, has evolved into a \$1 billion per year business. It holds 60% of the total industrial market share for holography. Testing comes in second, com-

prising 29% of this market and bringing in \$455 million in 1998. Holographic optical elements (HOEs) hold only 6%, but this is a high-growth sector and may be the area to keep an eye on. These elements make heads-up displays possible. They're also the element that lets the pick-up head for compact disk readers work extraordinarily fast. And, because they're gaining importance in the \$18 billion optoelectronic component market, expect HOEs to start

#### Industrial Market Share For Holography



hoarding more of the profits. Plus, the U.S. government has backed the development of these materials in an effort to capture a larger share of the photonics component manufacturing market. The U.S. manufactured 9% of the world's optoelectronic components in 1994, but consumed 40%. In 1995, Japan manufactured 72% of these components. These elements are set to take a bigger role as switching elements in electro-optical and communications systems, especially in holographic spectroscopy, interferometry,

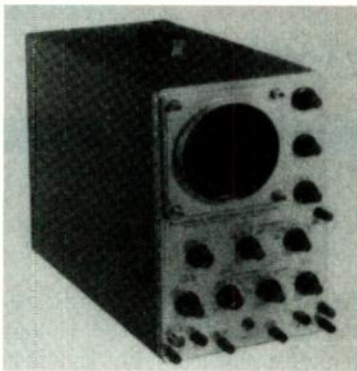
microscopy, telescoping, and other measuring instruments. They join together to form a \$100 million per year business. Next year, keep an eye out for the first prototype optical computers. These machines will use holograms as storage material for data. Able to deliver trillions of bits of information at speeds faster than current computers deliver millions, these computers are expected to revolutionize the industry and society at large. They'll quickly move into industrial and corporate applications, and it should only be a matter of time before they're taking over more of the world.

To get a copy of the Business Communications Company's study, contact them at 25 Van Zant St., Norwalk, CT 06855; (203) 853-4266; fax (203) 853-0348; www.buscom.com.—NK

## 40 YEARS AGO IN ELECTRONIC DESIGN

## Oscilloscope Kit: 0 To 4.5 Mc

Professional oscilloscope kit OP-1 has dc-coupled amplifiers and a dc-coupled crt unblanking. The triggered sweep circuit operates on internal or external signals and may be ac- or dc-coupled. The polarity of the triggering signal may be selected, and a triggering level control can start the sweep at any point on the waveform. The sweep frequencies are provided by switch-selected base rates of 2 and 0.2 msec, and 20, 2, and 1  $\mu$ sec per cm in conjunction with the continuously variable 10 to 1 multiplier. Sweep frequencies are calibrated to within 10% at all control settings. Vertical frequency response is within 1 db from dc to 2.2 mc, and within 6 db from dc to 4.5 mc. Rise time is under 0.1  $\mu$ sec. Horizontal frequency response is within 1 db from dc to 450 kc, and within 6 db from dc to 900 kc.—Heath Co., Dept. ED, Benton Harbor, Mich. (*ELECTRONIC DESIGN*, December 24, 1958, p. 36)



*It's too bad that this item didn't include a price—I'd say it was about \$300 in kit form, but I could be way off. What's your guess? In any case, the Heath Co. did a good job of keeping up with instrument technology, while holding its prices within the reach of home experimenters.—Steve Scrupski*

## The Year In Review: Components

Thousands of new products were announced during the year. One of the most important was the silicon-controlled rectifier by General Electric. Sample models created a stir in the industry, but they weren't available beyond sample lots until now. The solid state device acts like a thyatron and can handle up to about 60 amp.

A four-layer switch, ten times faster than most switching transistors, was made available by General Transistor Research Laboratory. It had a switching time of from 0.03 to 0.05  $\mu$ sec., and was designed for driving memory cores.

Ohio Semiconductor, Inc. and Westinghouse experimented with an 80-year-old principle: the Hall effect. Both companies came out with devices that took advantage of this principle. The devices generated a voltage as a function of the current and a magnetic field passing through the unit. Ohio Semiconductor went one step further. Using the Hall effect, they developed the Magneto-resistor. This unit changes its resistance as a function of the field passing through it. Westinghouse also developed what they called the silicon Trinistor triode, which is a high power switch. Still in the laboratory stage in the early part of the year, these units were capable of blocking up to 200 v and carrying up to 10 amp. From the on to off time, the unit is ten times faster than a comparable transistors.

Another component still in the laboratory stage was the constant-current varistor. Work on it is being done by Bell Laboratories. This two-terminal passive semiconductor is applicable as a current regulator, where load or supply varies from 20 to 120 v. It can be used as a coupling choke or ac switch.

And Lockheed Missile Systems announced a "fuel cell," which attains unprecedented efficiencies in electrochemical conversions and "could revolutionize conventional propulsion systems." Almost 100 per cent fuel utilization and 70 per cent energy conversion efficiencies were reportedly achieved in lab tests. Electrochemical fuel is stored outside the fuel cell, so cell components are not consumed in the electrode reactions. (*ELECTRONIC DESIGN*, December 24, 1958, p. 17)

*Well, that wraps things up for the important events in the electronics industry in 1958. Here's wishing all of you a healthy and prosperous 1999, when we'll look back at some truly significant developments, including the first public showing of Texas Instruments' first integrated circuit.—Steve Scrupski*

*Steve Scrupski is a former Editor-in-Chief of ELECTRONIC DESIGN. Now semi-retired, he can be reached at [scrupski@worldnet.att.net](mailto:scrupski@worldnet.att.net).*

## Virtual School

**W**hen you buy a computer nowadays, you expect it to come loaded with lots of nifty applications. But, did you ever think you'd get a university thrown in? Well, that's just what Micron Electronics, Nampa, Idaho is doing.

The company is launching an Internet-based component of all Micron personal computers, called Micron University. The idea behind this virtual learning center is to let power consumers, mid-market businesses, and the government make the most of their personal computers. To create it, Micron teamed up with ZDU, Ziff Davis' online training division.

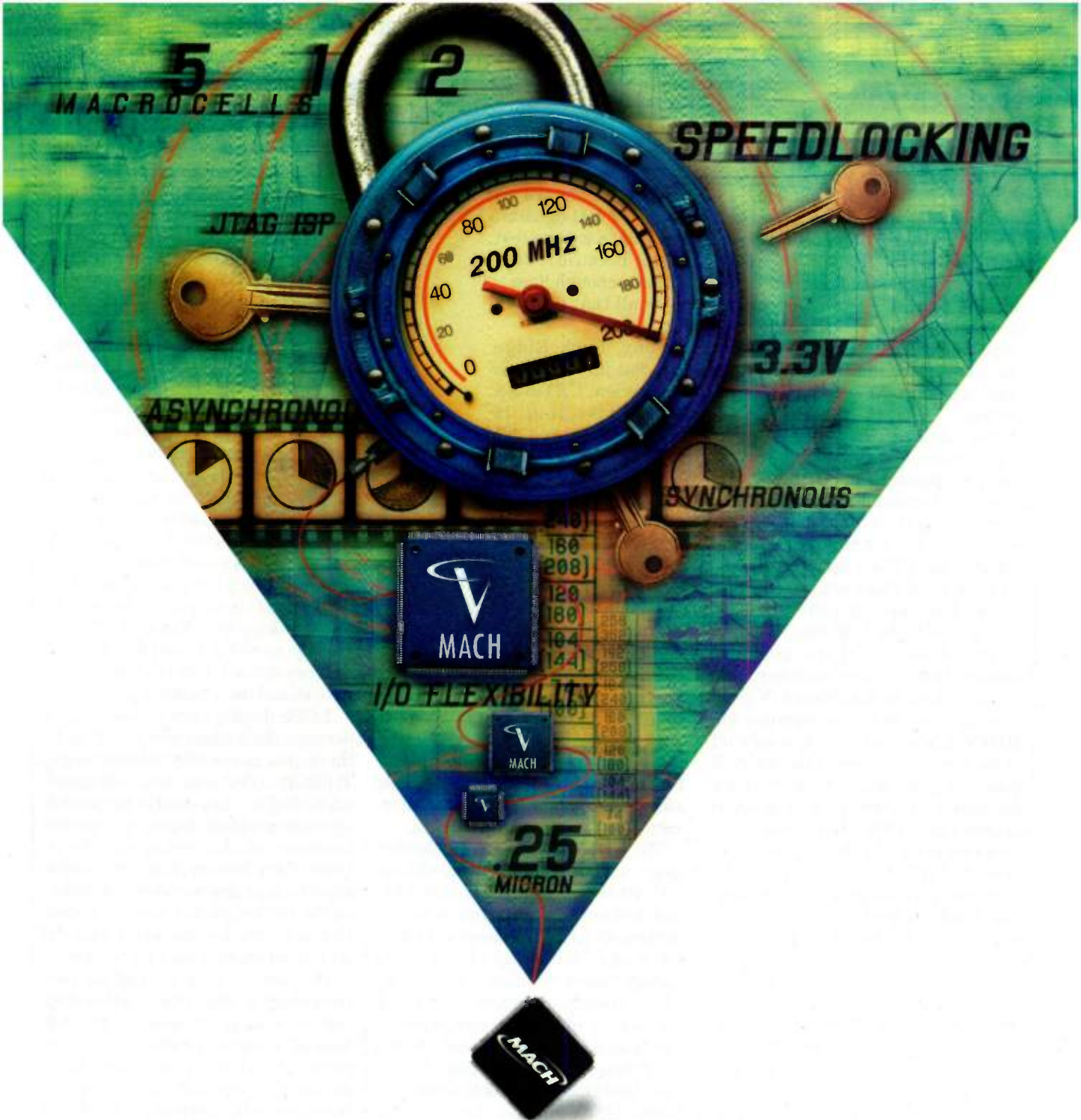
So, what can you expect if you decide to go back to school? Industry experts and professionals will teach online, instructor-lead courses and self-study tutorials from ZDU, technology and business seminars, and other community and support services. You can sign up for over 100 courses, including timely topics such as: dynamic HTML, implementing Intranets, Internet advertising, investing on the Web, and optimizing web site performance. You also can opt for one- to two-week technical clinics and single-session business seminars.

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## HEADS UP

**A**s broadcasters begin to transmit HDTV signals this fall, a whole slew of new, high-definition televisions are coming into the market. It's a very confusing environment with many signal formats, television specifications, and options. Now, just imagine yourself a consumer walking into your local high-tech electronics emporium. You decide to peruse all the latest wares in the TV section. Some are direct-view, others rear-projection.

Most of these TVs are the wide 16:9 aspect ratio, but a small number remain the standard 4:3. High-end systems incorporate all of the digital electronics inside, while some offer a set-top box for this purpose. But, one point is clear. You'd better be pretty well-heeled if you want to bring one home. They are all quite pricey—mostly over \$7000 to \$8000.

This January, that's going to change. At the winter Consumer Electronics Show in Las Vegas, Nev., a very special, 50-in., rear-projection HDTV will be on display in a suite off of the main show floor. This device is bound to create waves in the industry for two reasons. One, it has an unheard of price tag of \$2000. And two, it uses a new display technology that offers true, full HD resolution of 1920 by 1080 pixels. The company that's behind this intention to rock the industry is Digital Reflection Inc. (DRI), Los Gatos, Calif.

To understand how revolutionary this development could be, consider the other options currently available for HDTVs. Hitachi Home Electronics America, Atlanta, Ga., for example, just announced a new 61-in., rear-screen HDTV. It has a suggested retail price of \$7999 and uses three high-resolution, miniature CRTs to create a full-color 16:9 image. But a CRT is an analog device, so the digital signal must be converted to drive the CRTs, leading to the potential for artifacts.

Hitachi's, and many other HDTVs, can display HD signals in the 1080-line interlaced (1080i) format, which means it actually displays two 540-line sub-fields every second. This is the same way that NTSC signals are displayed on standard TVs. The TV also can upgrade 480-line progressive

(480p) signals into a 540p format.

Progressive scanning is the way computer monitors present images. But, if the HD signal is a 720p format, some data will be lost. This is because it doesn't have enough lines to show all that information.

Sony, Park Ridge, N.J., has just released a direct-view, CRT-based HDTV. It is a 34-in., 16-by-9 widescreen TV with a suggested retail price of \$8999. It can present 1080i, 480p, and NTSC signals. But again, this HDTV will lose information on higher resolution signals like 720p.

Plasma display panels (PDPs) and plasma address liquid crystals (PALC) from a number of companies also are arriving on the market. The big setback is that it'll cost you over \$10,000 for a 40/42-in., direct-view TV/monitor. Yes, these are digital devices—but the resolutions are typically 853 by 480. That means they can show 480p signals with full resolution, but will lose information for 720p or even 1080i data.

The HDTV from Digital Reflection uses a liquid-crystal-on-silicon (LCOS) display technology. It is a hybrid device whereby the active display electronics (the backplane) are fabricated on CMOS silicon lines. LCD manufacturing techniques are used to add a liquid crystal layer on top. Light is reflected off of the device, which is less than an inch in diagonal. With a full 1920 by 1080 pixel format, this device should have no trouble displaying 1080p HDTV signals—or twice the native resolution of the CRT, PDP, or PALC systems.

IBM, Yorktown Heights, N.Y., makes an SXGA LCOS display that's being used by several customers in large venue projection systems. "I know how to make an HDTV system with that kind of resolution," says Paul Alt, IBM's manager for exploratory display technology, "but I don't know how to do it at that price point. If DRI can do it, this is a really big deal."

According to DRI principle Inge-

mar Jansson, their new HDTV will only be about 15-in. deep and weigh less than 75 lb.—once again trouncing the other rear-screen competition. They are now shipping samples to certain OEMs, and predict that they'll be selling the sets to consumers by the third quarter of 1999.



CHRIS CHINNOCK

Industry analysts point out that there are three challenging technologies that must be overcome if such sets are to become reality. The first is the microdisplays themselves. Second are the rear screens needed to present the

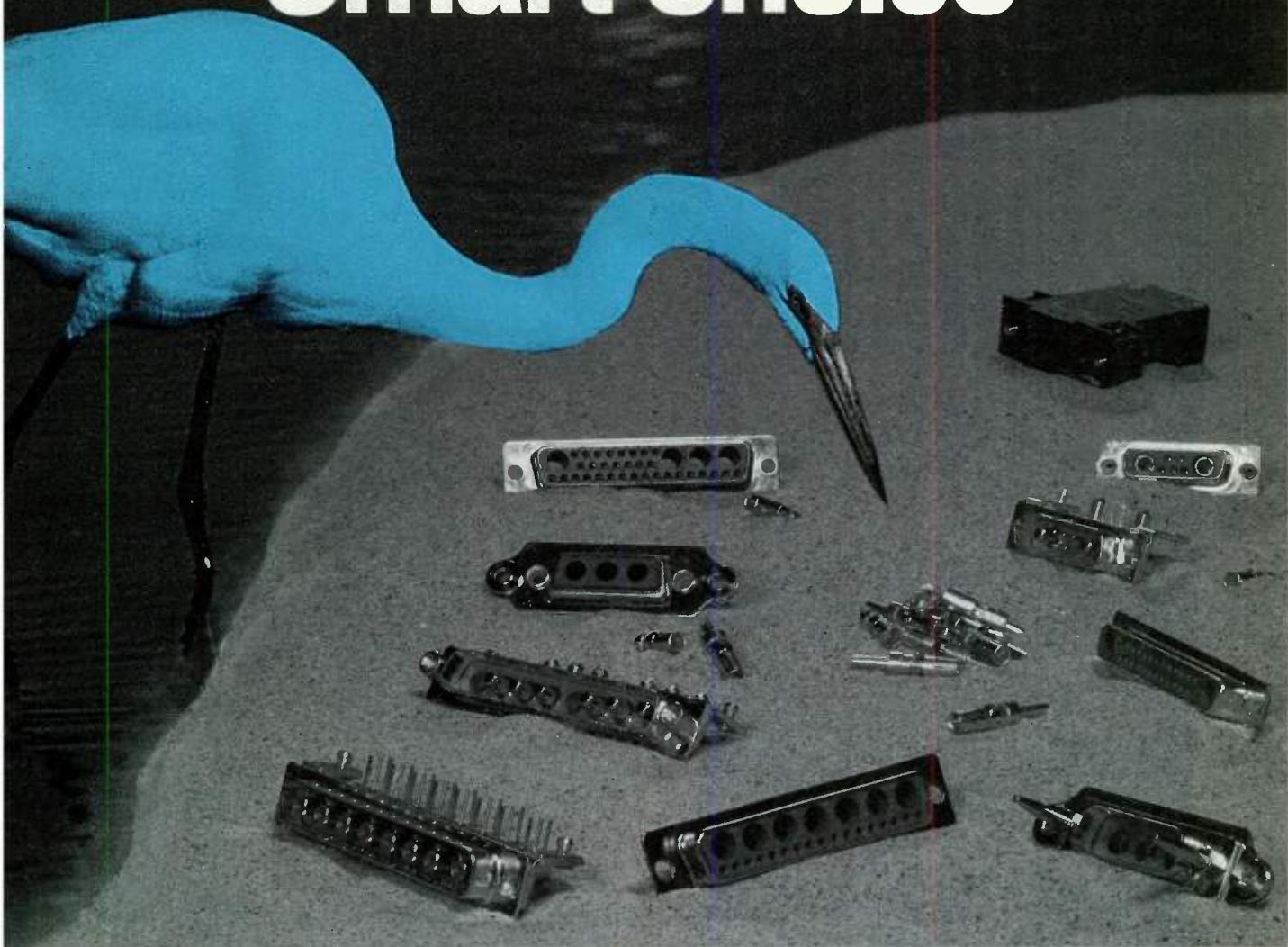
magnified image, and the lamp and illumination optics stand third. The small size of the display makes it difficult to efficiently reflect light off of the display, so compact and bright light sources are needed. DRI says they have solved these problems, however.

LCOS displays are an example of perhaps the hottest new category in the display community: microdisplays. Typically under about 3 in. in diagonal, microdisplays are used in projection systems or virtual display systems for head-mounted or bring-to-the-eye types of applications. There are probably 50 companies worldwide working on the transmissive, emissive, reflective, or scanned systems that are used for projection or virtual applications.

Of course, the potential for this technology is huge. But, whether they can reach the price points so that millions of consumer products can incorporate them has yet to be proven. As for me, I've personally jumped on the bandwagon by starting a newsletter devoted to tracking this promising new segment of the industry. We'll keep you posted on exciting developments like this.

*Chris Chinnock holds a BSEE from the University of Colorado. He's the editor of the "Microdisplay Report," a newsletter covering all technologies for projection and virtual-based display systems (www.mdreport.com). Chris can be reached at (203) 849-8059; fax (203) 849-8069; or e-mail: chinnock@mdreport.com.*

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## JUST 4 THE KIDS

When was the last time you purchased an interactive software program that you could use just as much as your child? If your answer is never, don't despair. Many of us purchase software for our children, show them how to use it, and never look at it again. But, if you're looking for something for both you and your child, Microsoft may have the answer: the interactive Encarta Reference Suite 1999 CD-ROM and DVD.

While Encarta was first developed in 1993 to assist both children and adults with research, its newest incarnation goes far beyond this capability. Using state of the art technology, the Encarta Reference Suite 1999 CD-ROM and DVD was specifically designed to foster lifelong learning and achievement through discovery.

It's comprised of three separate software programs: Encarta Encyclopedia Deluxe 1999, Encarta Virtual Globe 1999, and Microsoft Bookshelf 1999. To assist anyone researching a topic, the Deluxe 1999 version of the popular Encarta Encyclopedia software tool features over 40,000 updated articles and 20 million words, including 8000 new and 3500 revised articles.

It also boasts a number of new capabilities. Content Page is a home page that allows you to see all the information available on a subject. Encarta Explorer enables you to explore the best of the encyclopedia. You can use common phrases to search for a subject with Natural Language Searching. And finally, Encarta Study provides a research organizer, report creation tool, and lesson collection. These new features are invaluable for children who have difficulty narrowing down a subject matter to one topic, or for those learning to write a research paper or report for the first time.

The second software program, Encarta Virtual Globe 1999, features detailed maps with more than 1.2 million place names. It also boasts 18 different customizable map styles; 10,000 articles about the countries of the world,

including land and climate, society and culture, and geographic features; 65 global themes; and 19 world tours that bring images and sound together.

As if this weren't enough, web links permit you to search for additional information not contained in the software program's resources. The user can even compare traditions, customs, and the social and economic conditions of countries around the world. I particularly liked the virtual flight feature, which lets you soar above the country of your choice to get a bird's view of the area's landscape. If this isn't exciting enough for you, you can always try exploring the lunar surface of the moon—just another innovative feature of this software tool.

The third program, Bookshelf 1999, contains nine frequently used reference titles. You'll find the *Encarta Manual of Style and Usage*; *Encarta 1999 New World Almanac*; *The American Heritage Dictionary of the English Language, Third Edition*; *The Original Roget's Thesaurus of English Words and Phrases*; and more. With such a breadth of material available, this program is ideal not only for adults in the workplace, but also the at-home writer— young or old.

Using the Quickshelf Information Retrieval Tool and Quick Synonym, Bookshelf 1999 conducts searches with shortcuts. Such innovations as Quick Footnote, Quick Define, Quick Quote, and over 6000 web links make it easy to enhance whatever you write. And, the Dictionary and Thesaurus can be installed directly on your hard drive, giving you easy access to these resources at any time. Also, for those of you concerned about your child gaining access to potentially offensive words or articles, Bookshelf 1999 comes equipped with a parental con-



MARIFRANCES WILLIAMS

trol feature that hides these inappropriate references.

The DVD version includes high-resolution, full-screen video playback, MPEG video enhancements, and better quality sound. Its brightest star, however, is Suite Links, which permits the user to follow a train of thought from one suite CD-ROM to another using one of

more than 6000 connections. I found this feature particularly helpful when going back and forth between the three CD-ROM programs. Once you've used it, you'll wonder why all programs don't have this capability. The DVD version also includes 35% more videos, 20% more 360-degree views, high resolution, full-screen video playback, and high-quality audio with the ability to store uncompressed audio files.

What sets the Encarta Reference Suite 1999 apart is the user's ability to explore every corner of the globe from the desktop, while learning to enrich writing with quotations, know precise definitions, and use more exact word choices. It also integrates all three CD-ROM titles so seamlessly that the ability to use one program will enable the user to interact with the other titles easily. It uses the same tool bars, menu commands, navigation features, and powerful pinpoint search engine. Students and adults alike will find it user friendly.

The Encarta Reference Suite 1999 CD-ROM is now available and sells for \$99.95. The DVD sells for \$139.95. For more information, contact Microsoft Corporation, One Microsoft Way, Redmond, WA 98052; (425) 882-8080; [www.microsoft.com](http://www.microsoft.com).

Marifrances D. Williams holds a degree in Liberal Studies from San Diego State University, Calif. She is currently a fifth-grade teacher at Los Ranchos Elementary, San Luis Obispo, Calif. Williams specializes in the identification of advanced technology for the use of child-focused applications. She may be reached at [williamsofsm@lightspeed.net](mailto:williamsofsm@lightspeed.net).



# The Day The World stood still

The Wizard of Ooze and his Slimy Sycophantic Syndicate of Psychos hit Teletropolis; oozees blazing. Now the network capital wakens to find itself mired in muck, stuck in slime, and steeped in sludge. And the weather's lousy too.



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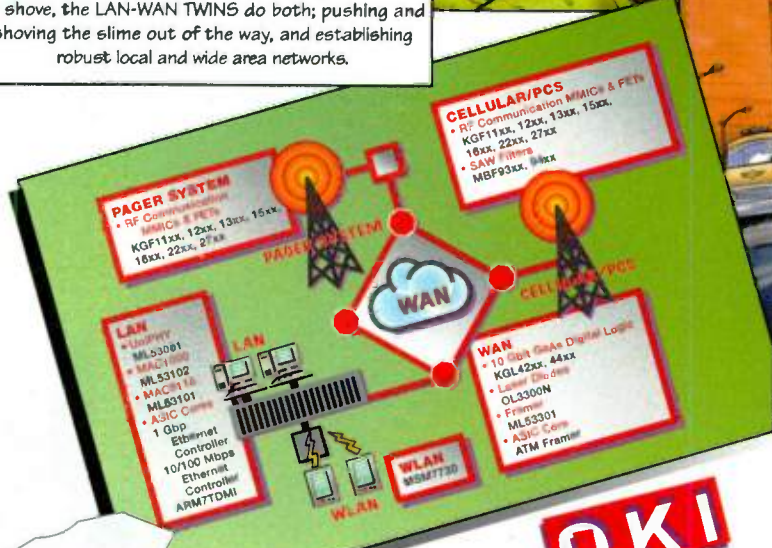


Teletropolis is too slug-ish for my taste.

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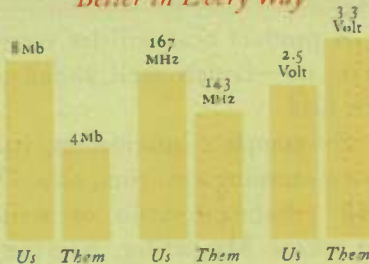
[ Soon, it'll be a HOUSEHOLD WORD. ]

# NtRAM

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In that sense, NtRAM is comparable to some other products.

On the other hand, it's not all *that* comparable.

# NtRAM

## NtRAM

After all, we give you a 167-MHz part and they give you 143 MHz. We give you a 2.5-volt part while they give you a 3.3-volt part. And we're already at 8 Mb—while their densest part is 4 Mb.

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## MANAGING THE DESIGN FACTORY

## Modularity And Flexibility

Many people notice that SOME modular designs are flexible. This has led some observers to conclude that ALL modular designs are inherently flexible. Let's take a closer look at this issue.

Although modularity itself may be a fairly fuzzy concept, most of us would probably agree on certain characteristics. For example, modularity implies some ability to achieve different configurations by mixing and matching modules. We normally expect to be able to alter the capabilities of a modular system by changing modules. If we can provide a wide range of capabilities, with minimal effort and cost, we consider the design to be flexible.

Yet, some modular designs are nightmarishly complex and very difficult to reconfigure. Alter a single module and you must make a large number of subtle adjustments in many unexpected corners of the system. Why do some modular designs seem to easily adapt to changing conditions, while others are fragile and inflexible? The key is not whether the design is modular, but rather how you modularize it.

To make a modular design flexible, you need to do four things. First, partition the design to isolate the effects of change. Ask yourself what functionality is most likely to change. Then, try to place this functionality into isolated modules. For example, if you expect a lot of changes in the user interface, you should isolate it from the rest of the system. That way, everything else doesn't have to change when you inevitably alter the user interface.

Second, reduce the number of interfaces that you create between your modules. This is a classic architectural heuristic, and justifiably so. It's important because the number of interfaces in a system can far exceed the number of modules. Since each interface is an interaction between modules, and each interaction is a poten-

tial failure mode, more interfaces means more ways for the system to break when you change a single module. So, shared modules can often reduce system flexibility.

Third, reduce the complexity of interfaces that you create between your modules. The more contact points between modules, the more interactions you create. There are two obvious ways to reduce the complexity of interfaces: Make modules more self-sufficient, and pass data at a

higher level of abstraction. For example, the reduced interface complexity of object-oriented programming comes from its higher abstraction level.

Finally, pay careful attention to the degree of coupling between modules. As I mentioned in a column earlier this year, interface margins are critical to preventing re-

work when individual modules change. They provide the buffer, permitting changes in a single module to stay within that module. The more tightly we couple the system, the broader the effects of any change and the higher the cost of making such changes.

For example, shared software modules often create cross-coupling problems that are fiendishly difficult to troubleshoot. Many computer users have probably experienced this when they load a new Windows program that writes over shared DLL files, thereby breaking another program.

You see, flexibility is not the automatic companion of modularity. It arises from specific architectural choices in the design. Once we realize this, we can truly exploit the benefits of modularity.

*Don Reinertsen is a consultant specializing in product development management. He is coauthor of "Developing Products in Half the Time" and author of the new book, "Managing the Design Factory." Reinertsen & Associates, (310) 373-5332; e-mail: Don.Reinertsen@compuserve.com.*



DON REINERTSEN

## BOOK REVIEWS

Journey into the future of microelectronics with *The Quantum Dot*. A computer officer in the physics department at the University of Newcastle Upon Tyne in England, Richard Turton employs analogies to explain the physical effects used in the design of semiconductor devices. Much of the book deals with more basic semiconductor principles (in the author's words, it's directed at first-year undergraduates in electrical engineering and physics, as well as readers without previous knowledge of these topics).

Yet it's quite entertaining, particularly the epilogue on "Computing the Future." Here, the author pontificates on how far we can go with conventional technology. Even experienced electrical engineers and physicists will find this 211-page paperback refreshing, if only to catch up on basic principles that were forgotten in a fast-moving and dynamic semiconductor device world.

*The Quantum Dot* is available from Oxford University Press for \$14.95; ISBN 0-19-510959-7.

Serious surveillance and counter-surveillance buffs should welcome Tom Larsen's 72-page book, *More Benchtested Circuits*, which concentrates on stealthy telephone-tapping and countermeasures circuits. It shows how to build a range of circuits that cost less than \$100 each. The "poor man's component signature analyzer" ostensibly checks to see if an ac power line is bugged, while another circuit provides "simple, reliable radio control for bugs."

As the author points out, all these circuits were benchtested to make sure they work. This follows up Larsen's earlier book, *Benchtested Circuits for Surveillance and Countersurveillance Technicians*. Need to build a circuit that performs "incendiary destruction of inaccessible taps and line-connected bugs?" This book is for you.

*More Benchtested Circuits* is available for \$21.00 from Paladin Press, Boulder, CO; www.paladinpress.com; ISBN 1-58160-007-0.

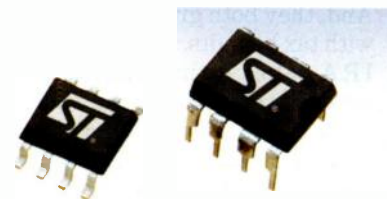
Roger Allan



# MICROPOWER OP AMP GIVES RAIL TO RAIL PERFORMANCE

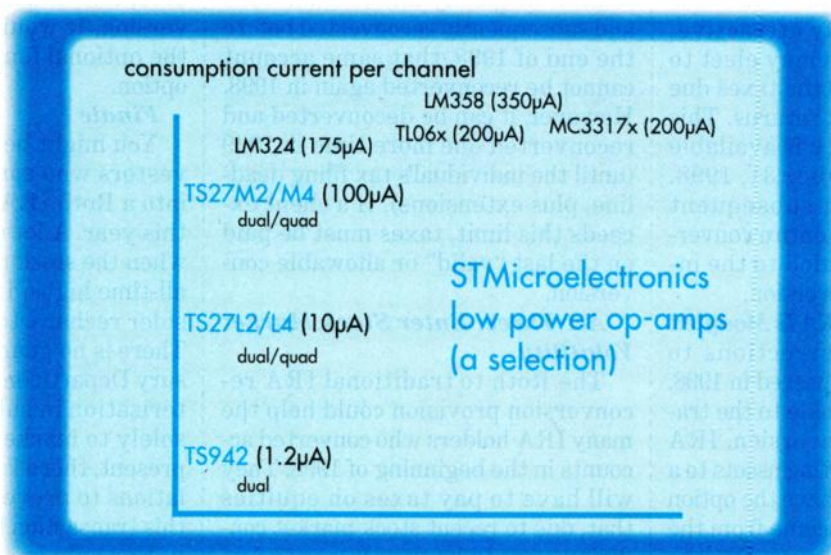
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## TS942



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## TIPS ON INVESTING

# The Roth IRA: A New Family Play For All Ages

**O**verture: What is an IRA? It is an Individual Retirement Account that comes in two basic flavors, the traditional IRA and the new Roth IRA.

Both permit you to save up to \$2000 a year (\$4000 with a spouse). And, they both grow and provide you with tax benefits. Here, the new Roth IRA takes a turn that currently makes it the more popular choice.

Contributions to a Roth IRA are not tax-deductible and participation has AGI limits. But, there is one major benefit (subject to special provisions). After a five-year holding period, all withdrawals are tax free. That means that after five years, you can take out this money and not have to claim it.

## Act One: A Star Is Born

The legislation that spawned the Roth IRA phenomenon also gave those with traditional IRAs the option to convert these accounts to a Roth IRA. Many IRA account holders did the math and decided that this was a prudent course of action for them.

Initiating a conversion in 1998 has also been particularly attractive, since account holders may elect to spread the income and the taxes due over the next four tax returns. This window of opportunity is available only through December 31, 1998. Conversions done in subsequent years will result in the entire conversion amount being added to the income in the year of conversion.

## Act Two: The Roth IRA Is Modified

Some technical corrections to 1997's legislation were passed in 1998. They added a new wrinkle to the traditional Roth IRA conversion. IRA account holders converting assets to a Roth IRA in 1998 now have the option to include the entire income from the conversion in 1998, or spreading the income equally over the next four years. For those investors who expect their tax bracket to rise in the future, this could be an attractive option.

Also, the income realized from Roth IRA conversions may affect the taxation of Social Security benefits. Those collecting Social Security

might want to take all the income from a Roth conversion in 1998. This way, they could shelter more of their Social Security income from taxes in future years.

Since many people effecting traditional to Roth conversions will not know if they qualify until they file their income taxes, the question arises: What if a conversion were done in 1998, and then the taxpayer found out that his adjusted gross income was above the \$100,000 qualification mark for doing a conversion? The 1998 legislation also set forth the mechanism for undoing a traditional to Roth conversion.

The IRS has just released new rules pertaining to Roth IRA conversions. Effective November 1, 1998, an individual can only deconvert and subsequently reconvert the same account one time per calendar year. For example, if an account is originally converted in 1998 and subsequently reconverted before the end of 1998, that same account cannot be reconverted again in 1998. However, it can be deconverted and reconverted one more time in 1999 (until the individual's tax filing deadline, plus extensions). If a client exceeds this limit, taxes must be paid on the last "valid" or allowable conversion.

## Act Three: Enter Stock Market Volatility

The Roth to traditional IRA re-conversion provision could help the many IRA holders who converted accounts in the beginning of 1998. They will have to pay taxes on equities that, due to recent stock market conditions, could be worth less today. The question then becomes: Can these accounts be converted back to a traditional IRA, and then subsequently be reconverted to a Roth IRA, in order to reduce the tax liability? You can breathe a sigh of relief, because the answer is yes.

If you converted to a Roth IRA

earlier in the year, you may find that market volatility has now eliminated some of your gains. But, the taxes due remain the same. By undoing your earlier Roth conversion and returning to a traditional IRA, and then reconverting the assets at their (lower) current market value, you eliminate the inflated tax liability. Technically, the unwinding of a Roth conversion is called a recharacterization.

If you recharacterize your Roth IRA, you may immediately reconvert back to another Roth IRA. However, you have until your tax filing deadline, plus extensions, to do the initial recharacterization. That would mean a 1998 conversion could be reversed through April 15, 1999, plus extensions. However, if—for example—you undo a 1998 conversion in January 1999

and convert it again in February 1999, this would count as a 1999 conversion. It would not be eligible for the optional four-year tax payment option.

## Finale

You might be one of the many investors who converted IRA assets into a Roth IRA at the beginning of this year. A lot of investors did this when the stock market was reaching all-time highs. If so, you should consider recharacterizing those assets. There is no guarantee that the Treasury Department will allow recharacterization in subsequent years due solely to market conditions. But at present, there is nothing in the regulations to prevent you from making this transaction for any reason.

For help in creating a new Roth IRA or traditional IRA for yourself or a family member, or to review *Is Recharacterization Right For You?*, contact Henry Wiesel, vice president, qualified plans coordinator at Salomon Smith Barney, 1040 Broad St., Shrewsbury, NJ 07702; (800) 631-2221, ext. 8653.



**HENRY WIESEL**  
CONTRIBUTING EDITOR

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# FT • FS SERIES MODUFLEX® SWITCHERS

## DESCRIPTION

The FT and FS Series are comprehensive lines of ultra compact power factor corrected models derived from our Moduflex® family of switching power supplies. This series utilizes advanced technology to produce a high quality input current wave form that is compliant to the harmonic requirements of EN61000-3-2. Based on modular construction, "off the shelf" modules permit high volume manufacturing with an outstanding quality level assuring timely delivery at a competitive cost.

Three classes of output modules are available. The **STANDARD** outputs allow short duration surge currents on all auxiliaries for hard starting loads. Optional **CURRENT LIMITED** outputs have square current limiting and feature wireless droop current sharing. Optional **ENHANCED** outputs have square current limiting, one wire star point current share, output good logic signal with LED, nominal 5V local bias, individual inhibit and margining. For requirements that cannot provide minimum load on the main output, the **ZERO PRELOAD** option is available for main outputs up to 500 watts.

## DELIVERY

Choose stocked units or construct a model number using stocked modules for fast delivery. Otherwise, form a model from the adjacent page to meet your specific requirements. Contact factory for deliveries on models derived from non-stocked modules.

## FEATURES

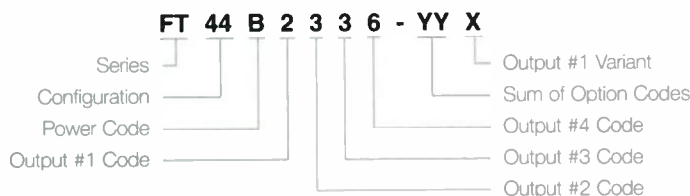
- 0.99 power factor.
- 5.5 watts per cubic inch.
- 1-7 outputs, 400-1000 watts.
- 120 kilohertz MOSFET design.
- Universal input.
- UL, CSA, TÜV (IEC, EN), CE.
- FCC, EN Class A EMI.
- IEC, EN Immunity.
- All outputs:
  - Adjustable*
  - Fully regulated*
  - Floating*
  - Overload and short circuit protected*
  - Overvoltage protected*
- Standard features include:
  - System inhibit*
  - Fan output*
- Options and accessories include:
  - Power fail monitor*
  - Redundancy*
  - Current Limited Outputs*
  - Enhanced Outputs*
  - Zero Preload*
  - End fan cover*
  - Top fan cover*
  - Rack Assemblies*

## STOCKED MODELS - Available in 3 days.

Max Power	Output 1	Output 2	Output 3	Output 4	Model*
400W	5V @ 50A	12V @ 12A	12V @ 12A	5V @ 10A	FT46A2332-45P
400W	5V @ 50A	12V @ 12A	24V @ 6A	12V @ 6A	FT46A2363-45P
600W	5V @ 60A	12V @ 12A	12V @ 12A	5V @ 10A	FT46C2332-13P
600W	5V @ 60A	12V @ 12A	24V @ 6A	12V @ 6A	FT46C2363-13P

\*400W models include power fail monitor, current limited modules, zero preload and end fan cover options.  
600W models include the same options except fan cooling is built into the unit.

## UNITS FROM STOCKED MODULES - Available in 2 weeks.



- Configuration:** Allowable quad output configurations are 42, 44, 46 and 48.
- Power Code:** Choose Power Code A through D for 400-750W models.
- Output Codes:** Select any outputs from the shaded area on the Output Types table consistent with the configuration chosen.
- Option Code:** Specify Option Code. Refer to the Option table. Codes 02 (redundancy) and 16 (enhanced) are excluded from models available in 2 weeks. Fan cooling is built into 600 and 750W units.

## OPTIONS

Option Code	Function
00	None
01	Power Fail Monitor
02	Redundancy
04	Current Limited
08	Zero Preload
16	Enhanced
32	End Fan Cover
64	Top Fan Cover

Replace the YY with the sum of the Option Codes.

## MODEL SELECTION

Models are available in power ratings of 400 to 1000 watts, with corresponding code letters A through E. See Power Code chart.

Output modules are available in six types: J, K, L, M, N and P in nominal power ratings from 75 - 500 watts. Type M, N and P modules are variable power rated depending upon the unit power rating. The M, N and P Module table directly below shows the corresponding multiplier applicable to the output current ratings of the M modules and allowable power ratings for the N and P modules. For example, a 750 watt multiple will have its M type module configured to produce 120A @ 5V or 12A @ 48V. The voltage and current rating of output modules are listed in the table of output types. This table assigns an alpha-numeric code designating the nominal voltage rating of the module.

Power Code	Unit Power Rating	M Module Current Multiplier		N/P Module <sup>†</sup>
		Single Output	Multiple Output	Allowable Power Rating
A	400W	0.8	0.5	250W
B	500W	1.0	0.6	300W
C	600W	1.2	0.8	400W
D	750W	1.5	1.2	500W
E	1000W	2.0	1.5	750W

<sup>†</sup>When an N or P module is used as the main output, the allowable power and the module current ratings must not be exceeded.

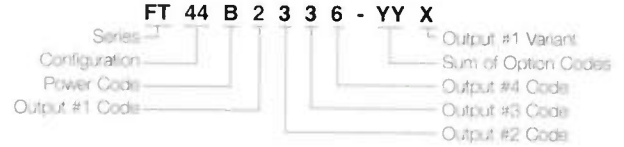
Output Types*						
Output		Module Type				
Code	Volts	J Amps	K Amps	L Amps	M Amps	N/P Amps
0	2	10	20	30	100	60
1	3.3	10	20	30	100	60
2	5	10	20	30	100	60
3	12	6	12	24	42	42
4	15	5	10	20	33	33
5	18	4	8	16	28	28
6	24	3	6	12	21	21
7	28	2.5	5	10	18	18
8	36	2	4	8	14	14
9	48	1.5	3	6	10	10
A	2.2	10	20	30	100	60
B	2.4	10	20	30	100	60
C	2.7	10	20	30	100	60
D	3	10	20	30	100	60
E	3.6	10	20	30	100	60
F	4	10	20	30	100	60
G	4.5	10	20	30	100	60
H	5.7	10	20	30	90	60
J	6.3	10	20	30	80	60
K	7	9	18	30	70	60
L	8	8	16	30	62	60
M	9	8	15	30	56	56
N	10	7	14	30	50	50
P	11	7	13	27	45	45
Q	13.5	6	11	22	37	37
R	17	5	9	18	30	30
S	19	4	8	16	26	26
T	21	4	7	14	24	24
U	23	4	7	13	22	22
V	26	3	6	12	19	19
W	29	3	5	10	17	17
X	32	2	5	9	16	16
Y	40	2	4	8	13	13
Z	44	2	4	7	12	12

Multiple output modules of a given type are arranged in ascending order by voltage magnitude in the same sense as the output number sequence in the configuration diagrams.  
\*Shaded ratings are stock.

## HOW TO ORDER

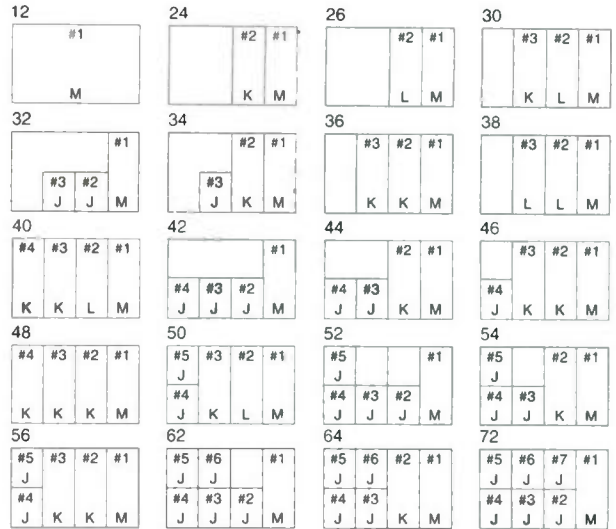
To form the proper model number defining a custom requirement, select the letters FS or FT to designate the series, then choose the desired configuration and list the configuration code. Insert the power code letter for the power level and follow with the output code numbers or letters for each specific output. Enter a dash and from the option table insert the sum of the option codes. Where lower power is desired for the main module, an N module can be substituted and is denoted by a letter N in the output variant position. In addition, when no preload is available for the main output, choose Option Code 08 and add a P in the output variant position. For an enhanced main and current limited auxiliaries, specify both 04 and 16 option codes.

### HARMONIC CORRECTED 500W QUAD SWITCHER



## OUTPUT CONFIGURATIONS

The boxes below are diagrammatic representations of the power supplies as viewed from the output end. The two-digit numbers above the boxes are the configuration codes.



Refer to the table below for allowable configurations by series.

Output Config	Unit Power Rating				
	400W	500W	600W	750W	1000W
12	•	•	• X	• X	N
24	•			• X	
26		•	• X	• X	X
30					X
32	•			• X	
34	•	•	• X	• X	
36	•	•	• X	• X	X
38					X
40					X
42	•	•	• X	• X	
44	•	•	• X	• X	X
46		•	• X	• X	X
48			X		X
50					X
52	•	•	• X	• X	X
54		•	• X	• X	X
56			X		X
62		•	• X	• X	X
64			X		X
72			X		X

• Represents allowable configurations for the FT Series.  
x Represents allowable configurations for the FS Series.

# SPECIFICATIONS

## INPUT

90-264 VAC, 47-63 Hz.

## POWER FACTOR

0.99 typical.

## EMISSIONS

FCC 20780 Part 15/EN 55022, Class A Conducted. EN 61000-3-2, Harmonics. EN 61000-3-3, Voltage Fluctuations.

## IMMUNITY

IEC 1000-4-2/EN 61000-4-2, Electrostatic Discharge. IEC 1000-4-3/EN 61000-4-3, Radiated Field. IEC 1000-4-4/EN 61000-4-4, Electrical Fast Transients. IEC 1000-4-5/EN 61000-4-5, Level 3 Surge. IEC 1000-4-6/EN 61000-4-6, Conducted Field.

## INPUT SURGE

230 VAC - 38 amps max. 115 VAC - 19 amps max.

## EFFICIENCY

75% typical.

## HOLDUP TIME

20 milliseconds from loss of AC power.

## OUTPUTS

See model selection table. Outputs are trim adjustable  $\pm 5\%$ .

## OUTPUT POLARITY

All outputs are floating from chassis and each other and can be referenced to each other or ground as required.

## LINE REGULATION

Less than  $\pm 0.1\%$  or  $\pm 5\text{mV}$  for input changes from nominal to min. or max. rated values.

## LOAD REGULATION

$\pm 0.2\%$  or  $\pm 10\text{mV}$  for load changes from 50% to 0% or 100% of max. rated values.

## MINIMUM LOAD

Main output requires a 10% minimum load for full output from auxiliaries. Use Option 08 if no minimum load is available for mains up to 500 watts. Singles require no minimum load.

## RIPPLE & NOISE

1% or 100 mV, pk.-pk., 20 MHz bandwidth.

## OPERATING TEMPERATURE

0-70°C. Derate 2.5%/°C above 50°C.

## COOLING

A min. of 10 LFS\* for models without internal fans directed over the unit for full rating. Two test locations on chassis rated for max. temperature of 90°C. 600 watt, 750 watt and 1000 watt models have built-in ball bearing fans.

\*Linear feet/second.

## TEMPERATURE COEFFICIENT

$\pm 0.02\%/^{\circ}\text{C}$ .

## DYNAMIC RESPONSE

Peak transient less than  $\pm 2\%$  or  $\pm 200\text{ mV}$  for step load change from 75% to 50% or 100% max. ratings.

## RECOVERY TIME

Recovery within 1%. Main output - 200 microseconds. Auxiliary outputs - 500 microseconds.

## SAFETY

Units meet UL 1950, CSA 22.2 No. 950, EN 60 950, IEC 950.

## ISOLATION

Conforms to safety agency standards.

## INPUT UNDERVOLTAGE

Protects against damage for undervoltage operation.

## SOFT START

Units have soft start feature to protect critical components.

## OVERVOLTAGE PROTECTION

Standard on all outputs.

## REVERSE VOLTAGE PROTECTION

All outputs are protected up to load ratings.

## OVERLOAD & SHORT CIRCUIT

Outputs protected by duty cycle current foldback circuit with automatic recovery. Standard auxiliaries have additional back-up fuse protection. Options 04 and 16 have square current limiting with automatic recovery when overload is removed.

## THERMAL SHUTDOWN

Circuit cuts off supply in case of local over temperature. Units reset automatically when temperature returns to normal.

## FAN OUTPUT

Nominal 12 VDC @ 12 watts maximum.

## INHIBIT

TTL compatible system inhibit provided. Option 16 has individual output inhibit.

## REMOTE SENSING

On all outputs except standard and 04 Option outputs 75 watts or less.

## SHOCK & VIBRATION

Shock per MIL-STD 810-E Method 516.4, Procedure I. Vibration per MIL-STD 810-E Method 514.4, Category 1, Procedure I.

## MECHANICAL

CASE	SERIES	WATTS	H	x	W	x	L
1	FT	400W/500W	2.50"	x	4.93"	x	8.00"
3	FT	600W	2.56"	x	5.08"	x	10.03"
4	FS	600W	2.56"	x	5.08"	x	11.00"
5	FT	750W	2.63"	x	5.20"	x	10.03"
6	FS	750W	2.63"	x	5.20"	x	11.63"
7	FS	1000W	2.56"	x	7.13"	x	11.63"

## OPTIONS

### POWER FAIL MONITOR

Optional circuit provides isolated TTL and VME/VXI compatible ACFAIL signal providing 4 milliseconds warning before main output drops by 5% after an input failure. A SYSRESET signal following VME timing requirements is provided when an N module is used as a main output. Both logic signal outputs can sink current per the VME specification.

### REDUNDANCY

Optional Or-ing diodes for hot pluggable N+1 redundant operation. For FT Series 500 watt & 750 watt models with 1-4 outputs. Main output current limited to 100 amps. Remaining outputs 16 amps max.

### CURRENT LIMIT

Option provides on all outputs:

- Square current limit with auto recovery.
- Wireless droop current share for parallel or N+1 redundant operation.

### ZERO PRELOAD

Optional circuit removes need for preload on main output up to 500 watts.

### ENHANCED

Option provides on all outputs:

- Square current limit with auto recovery.
- Single wire active current share for parallel or N+1 redundant operation.
- DC output good logic signal with LED indicator.
- Logic inhibit.
- Nominal 5V bias.
- Margining.

### END FAN COVER

Optional cover with brushless DC ball bearing end fan which provides the required air flow for full rating.

### TOP FAN COVER

Same as above with fan cover mounted on top of the power supply.

### ACCESSORIES

RA50 and RA75 Series 2U high rack assemblies provide hot pluggable interface and hold up to 3 FT Series 500 watt or 750 watt units respectively.

Specifications subject to change without notice.



98703A

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## Careful HDL Coding Maximizes Performance In LUT-Based FPGAs

*It's High Time You Understand The Interaction Between HDL Coding Style, FPGA Device Architectures, And Design Software.*

SAMIR SAMHOURI, Lucent Technologies Inc., 555 Union Blvd., Allentown, PA 18103; (800) 372-2447.

In an ideal world, synthesis tools would understand and exploit all field-programmable gate array (FPGA) architectures and their special features without designer intervention. In the real world, however, this isn't the case. Applications that are speed- and area-intensive require that designers be aware of the consequences of coding style. To obtain optimal results, an understanding of the FPGA's architecture, the synthesis tool, and the back-end layout software also becomes necessary.

Most FPGAs are not fine-grained. Instead, they're made up of programmable functional units (PFUs) that implement combinational logic in lookup tables (LUTs) and a certain number of flip-flops or latches. The following lists some FPGA features that synthesis tools may have difficulties implementing:

- The flip-flops inside the PFUs share some control signals, such as the clock, clock enable, and reset/set. In an ORCA architecture, for example, four flip-flops will fit inside a single PFU only if they have the same mentioned signals. Most synthesis tools don't understand this. If a design is coded without keeping this fact in mind, the tools might utilize some of the flip-flops inefficiently. This results in an inflated chip size.

- Memory elements inside some FPGAs can be implemented in the LUT portion of the PFU. This method of constructing RAM or ROM inside FPGAs saves a large number of gates and drastically improves the speed of a device.

Unfortunately, there's no one way to implement memory in HDL. Hence, the synthesis tools can't detect their presence to utilize the FPGA's LUT feature.

- Counters and state machines also are difficult. With so many different kinds of these circuits, the reason for using one over another is mostly dependent on the application. A knowledge of an FPGA's architecture also helps in deciding which method is most efficient.

- Design hierarchy and floorplanning is hard for synthesis tools to implement.

- Global Set Reset (GSR) signal is an internally routed reset signal that doesn't consume any of a chip's routing resources. There's currently no way to implement this feature in VHDL. Consequently, synthesis tools can't utilize this feature unless the GSR compo-

nent gets instantiated in the HDL code.

There are three basic techniques for writing VHDL code. Starting with the least efficient method, they are:

1. A generic code that has not been targeted to an architecture.
2. A generic code targeted towards a device architecture.
3. An HDL code with macro instantiation.

It helps to compare these three methods, incorporating coding styles that would be targeted to reduce the aforementioned synthesis inefficiencies.

### Synchronous Logic

Flip-flops and latches in most LUT-based FPGAs can be configured in synchronous set/reset mode using the Local Set Reset (LSR) assigned by the

### Listing 1

```
entity fig25a is
  Port ( clk_w, reset, wr: in std_logic;
         add_in : integer range 0 to 15;
         data_in : in std_logic_vector(7 downto 0);
         data_out : out std_logic_vector(7 downto 0));
end fig25a;
architecture synth of fig25a is
  constant depth : integer := 16;
  type data_array is array ( integer range <> ) of std_logic_vector ( 7 downto 0);
  signal data : data_array (0 to depth - 1);
begin
  process (clk_w)
  begin
    if (clk_w = '1' and clk_w'event) then
      if wr = '0' then
        data (add_in) <= data_in;
      end if;
    end if;
  end process;
  data_out <= data (add_in);
end synth;
```

## Listing 2

```

entity fig25b is Port (clk_w, wr
: in std_logic;
  add_in : integer range 0 to 15;
  data_in : in std_logic_vector(7 downto 0);
  data_out : out std_logic_vector(7 downto 0));
end fig25b;
architecture synth of fig25b is
  constant depth : integer := 16;
  constant idepth : integer := (depth - 1);
  type data_array is array ( integer range <> ) of std_logic_vector (7 downto 0);
  signal data : data_array (0 to depth - 1);
begin
  GEN_LABEL : for I in idepth downto 0 generate
    data_out <= DATA(I) when (wr='1' and I=add_in) else
    (others=>'Z');
  Process begin
    wait until (clk_w'event and clk_w = '1');
    if (I = add_in and wr = '0') then
      data(I) <= data_in;
    end if;
  end process;
end generate GEN_LABEL;
end synth;

```

designers. In order for a latch or flip-flop to be implemented correctly, the synthesis tool must instantiate the proper library macro. But, this won't happen unless the HDL code contains the correct description. A basic understanding of the FPGA architecture to be used is a must.

Designers have to keep in mind the kinds of flip-flops and latches that are available in the vendor's macro library. If the code implements a register functionality that's not represented by a corresponding macro in the library, the extra functionality will be added to the circuit using additional logic. Most of the time, this extra logic ends up on the registers' datapath, increasing area and delay.

Each PFU can implement up to a certain number of latch and/or flip-flops that share some of its inputs. To get the highest area utilization out of the device, latches and flip-flops are best grouped in multiples of the PFU's register capacity.

If synchronous functionality of the flip-flops is required, the Global Set Reset signal can't implement the set/reset signal. This is because the GSR has asynchronous functionality. It can, however, be used in addition to the LSR signal.

If the code implies a gated Clock Enable (CE) signal, the synthesis tool tends to duplicate the enable logic for every register in the design. To avoid this, it's recommended to keep the gated signals in a separate process. Also, pass their output to the CE input of the main module.

In order to use the correct flip-flop,

the HDL code has to describe the correct functionality. For instance, the following code listing is used to implement a two-bit register with a +V<sub>E</sub> level synchronous reset and a +V<sub>E</sub> level enable signal.

```

DO <= D1 AND D2;
SYNC_RST : Process (CLK,RST)
begin
  if (CLK'event and CLK='1') then
    if (RST = '1') then
      DATA_OUT <= (others => '0');
    elsif (DO = '1') then
      DATA_OUT <= DATA_IN ;
    end if;
  end if;
end process SYNC_RST;

```

Note that to implement a synchronous reset correctly the "if (RST = '1') then" statement has to be entered after the CLK'event inside the process. And for "DO" to be connected to the CE input of the flip-flop, the "elsif (DO = '1') then" statement must go after the "if (RST = '1') then".

Be vigilant with this approach, because some synthesis tools have known limitations in implementing synchronous reset/set. They can produce some unpredictable results that, although

functionally correct, would affect the area and signal would be connected to the CE of the flip-flops only if the code is implemented, as shown in the previous HDL example.

Also, some signals weren't meant to get connected to the CE port. But, be aware that they will be if designers don't know what kind of coding algorithm will result in a CE connection. Consider:

```

SYNC_RST : Process (CLK,RST)
begin
  if (CLK'event and CLK='1') then
    if (D1 = '0' and DATA_IN = "10") then
      DATA_OUT(0) <= DATA_IN(0) ;
    elsif (D2 = '0' and DATA_IN = "01") then
      DATA_OUT(1) <= DATA_IN(1);
    end if;
  end if;
end process SYNC_RST;

```

The code in this listing will generate two flip-flops with two different CE signals for a couple of reasons. First, there are some undefined states in the process (such as the state when D1= '1' and DATA\_IN= '10'). Also, not all of the outputs for the defined states were defined under every "if" statement.

Both of these issues will force the synthesis tool to use the CE port of the flip-flops in order to retain their previous values. As a result, this circuit will consume two programmable logic cells (PLCs) instead of one. To avoid these kinds of inefficiencies, try the following when writing HDL code:

- Always attempt to group multiples of four flip-flops under every "if" statement.
- Try to define all the states of the control signals and the status of the register outputs for every state.

```

if (CLK'event and CLK='1') then
  if (D1 = '0') then
    DATA_OUT <= "01" ;
  elsif (D2 = '0') then
    DATA_OUT <= "10";
  else
    DATA_OUT <= DATA_IN;
  end if;

```

## Listing 3

```

architecture ram16x8z of ram16x8z is
  component ram16x8z
    Port ( clk_w : in std_logic;
          reset : in std_logic;
          add_in : in std_logic_vector(3 downto 0);
          data_in : in std_logic_vector(7 downto 0);
          wr : in std_logic;
          data_out : out std_logic_vector(7 downto 0));
  end component;
begin
  u1: ram16x8z port map (clk_w, reset, add_in, data_in, wr, data_out);
end ram16x8z;

```

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## Listing 4

```

process (clk,reset)
begin
  if reset = '1' then
    RD_ADD <= (others => 000);
    WR_ADD <= (others => 000);
    DIFF_PTR <= 0;
  elsif (clk = '1' and clk'event) then
    if wr = '1' and (status=not_empty or status = empty) then
      WR_ADD <= WR_ADD + '1';
      DIFF_PTR <= DIFF_PTR + 1;
    elsif rd = '1' and (status=not_empty or status = full) then
      RD_ADD <= RD_ADD + '1';
      DIFF_PTR <= DIFF_PTR - 1;
    end if;
  end if;
end process;
status <= empty when DIFF_PTR = 0 else
full when DIFF_PTR = depth else
not_empty;

```

This listing shows an example of code that will not try to utilize the CE inputs of the flip-flops.

### Memory Modules

The most efficient way to implement memory in an SRAM FPGA is by using the internal lookup tables inside of the PFU. In a Lucent FPGA, for example, each PFU can implement two RAM or ROM arrays: a single 16-by-4 element or two 16-by-2 memory blocks. Multiple PFUs can then be used to implement other array sizes (such as 16 by 8, 32 by 4, and 64 by 8). Let's discuss three methods for implementing a 16-by-8 memory block.

The first method is generic VHDL code (see *Code Listing 1*). When the VHDL code in this listing is implemented in a 2C04, the design uses 128 flip-flops, 76 out of 100 PFUs, and 0 out of 800 three-state buffers (TBUFs). The timing report states that 38 MHz is the maximum frequency for this circuit after map, place, and route.

Method two is generic VHDL code targeted towards FPGAs (see *Code Listing 2*). When this VHDL code is implemented in a 2C04, the design utilizes 128 flip-flops, 41 out of 100 PFUs, and 128 out of 800 TBUFs. According to the timing report, 40 MHz is the maximum frequency for this circuit after map, place, and route.

The third and final method is instantiation of RAM (see *Code Listing 3*). When the VHDL code in the listing is implemented in a 2C04, the design uses 20 flip-flops, six out of 100 PFUs, and eight out of 800 TBUFs. The timing report states that 52 MHz is the maximum frequency for this circuit after

map, place, and route.

The advantages to the first method are that it maintains generic VHDL code that can be targeted to any technology. Plus, no knowledge of the FPGA architecture is required. There are, however, disadvantages to this method. There's no utilization of the FPGA's architectural features. And, it produces poor area and timing results.

Method two flaunts several advantages. It maintains a generic VHDL code that can be targeted to any technology. Compared to method one, it offers an improvement of almost 50% in terms of area. It also beats the first method out with an almost 200% improvement of clock-to-out delays.

Yet, method two also has its weak points. One disadvantage is its use of the FPGA's tri-state buffers, which might make routing difficult in bigger designs. Also, this method doesn't exploit the FPGA's architectural features.

The last method has two main advantages. It offers an improvement of almost 25% in the overall timing performance of the design, and provides a reduction of almost 35 PFUs over method two. Unfortunately, though, this method's VHDL code is locked to a specific technology.

### Counters And State Machines

There are many types of counters and state machines that can be implemented through VHDL. Each type is application-specific, with its own efficiencies and inefficiencies.

Binary counter circuits are the easiest to implement in HDL. They also fit very efficiently in some of today's LUT-

based FPGAs. In an ORCA architecture, for instance, each LUT can be configured in a ripple mode so that the PFU can implement up to 4-bit arithmetic functions. Moreover, most common synthesis tools understand this FPGA feature and can take advantage of it, while still keeping the HDL code generic. The following code reveals a simple HDL implementation of a synchronous 8-bit upcounter with an enable line.

```

SYNC_CNTR : Process (CLK,RST)
begin
  if (RST = '1') then
    CNT <= (others => '0');
  elsif (CLK'event and CLK='1') then
    if (ENBL = '1') then
      CNT <= CNT + '1';
    end if;
  end if;
end process SYNC_CNTR;
DATA_OUT <= CNT;

```

Implemented in a 2C04, the counter uses eight flip-flops and two out of 100 PFUs. The maximum frequency for this circuit after map, place, and route is 91.542 MHz.

Its advantages are very straightforward. It's very simple to implement, and fits efficiently in most LUT-based FPGAs. But, there is one main disadvantage. If the counter's output needs to be decoded for applications like a state-machine controller or a generic memory block, the decode logic will add a considerable amount of gates to the circuit. This will most probably degrade the performance.

If performance is the desired goal, using one hot key or shift-register counters is more suitable than the previous solution. Still, this method has a serious drawback: It consumes a large number of gates. The following listing shows the HDL code for a 4-bit counter implemented in a one hot key configuration.

```

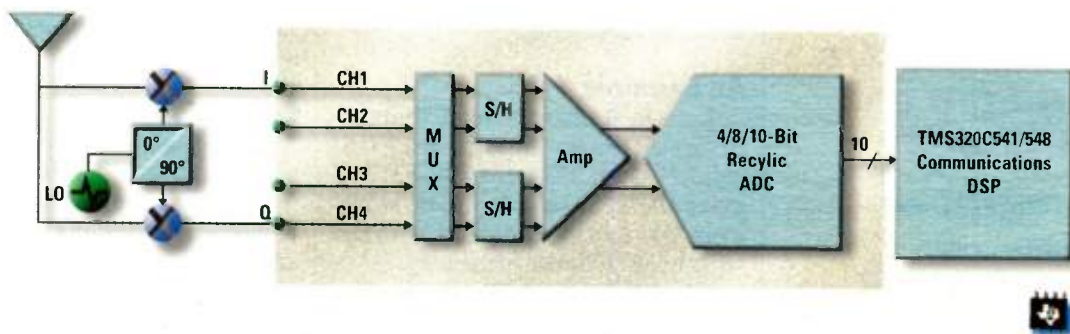
SYNC_CNTR : Process (CLK,RST)
begin
  if (RST = '1') then
    CNT(3 downto 0) <= "0000";
    CNT(4) <= '1';
  elsif (CLK'event and CLK='1') then
    if (ENBL = '1') then
      CNT <= CNT(3 downto 0) & CNT(4);
    end if;
  end if;
end process SYNC_CNTR;
DATA_OUT(3 downto 0) <= CNT(3 downto 0);

```

The resulting circuit, implemented in a 2C04, uses five flip-flops and two out of 100 PFUs. After map, place, and route, the maximum frequency for this circuit is 109 MHz.

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binary implementation, especially when it's combined with some sort of a machine controller. This is because the decoding of the counter's output will be done on just a single bit. In addition, this circuit is easy to implement in VHDL. As can be seen from the preceding software listing, it takes only one line of code using the concatenation operation (and).

On the down side, implementing the circuit requires a large number of flip-flops. Assume that an N-bit counter is to be built. Using this method,  $[(2^N)+1]$  registers will be needed to implement all of the counter states. This form of counter or state machine doesn't take advantage of the FPGA's architectural features, which would allow for a straightforward implementation of arithmetic functions.

### An Example

Let's look at an example that discusses the implementation of a FIFO memory block. The size of the FIFO is going to be 127 by 4. It will be implemented in two methods: both with and without instantiation of memory.

The FIFO is a single-port device, meaning that the memory array can only be read or written at one time. FULL\_L and EMPTY\_L signals indicate the status of the FIFO. WRL and RDL are the active low write and read signals.

First, let's try a generic VHDL description for a 127-by-4 FIFO. For this method, the whole FIFO design is placed under one process and then synthesized as a single block. Due to the limitation on the length of this article, the code for this method will not be shown. When implemented in a 2C15 FPGA, the design uses 528 flip-flops and 200 out of 400 PFUs. The timing report reveals that 20 MHz is the maximum frequency after map, place, and route.

Now, let's try an instantiated VHDL code approach. The same code that was used for the previous method is now divided into two blocks. Block one is a single process with the following functions:

- Calculates the Write and Read addresses depending on the addresses' previous values, as well as the FULL\_L, EMPTY\_L, WRL, and RDL signals.
- Calculates a value named

DIFF\_PTR that gets incremented by 1 in a write operation and decremented by the same value during a read operation. This value gets used to set the FULL\_L and EMPTY\_L signals of the FIFO.

This first block includes everything except the RAM\_ARRAY entity. The process for this block can be found in Code Listing 4.

Block two is created with instantiated VHDL code. In this entity, there's an instantiation for eight RPP16-by-4z macros from the ORCA FPGA library. These macros were netlisted so as to create the 127-by-4 memory block of the FIFO (RAM\_ARRAY).

Implemented in a 2C15 device, the design uses 20 flip-flops and 25 out of 400 PFUs. After map, place, and route, the maximum frequency for this circuit is 29 MHz.

### Conclusion

For designs that aren't speed- and area-sensitive, it's probably enough to write generic, synthesizable HDL code. However, for designs in which speed and area are critical, a basic knowledge of the FPGA architecture and the correct HDL coding style for that architecture is a must.

Synthesis vendors are currently working with the FPGA suppliers in hopes of advancing the tools to a level where they automatically exploit all of a device's architectural features. But for now, designers must apply their digital hardware experience *while* coding HDL. This is the only way to get the highest utilization out of FPGAs.

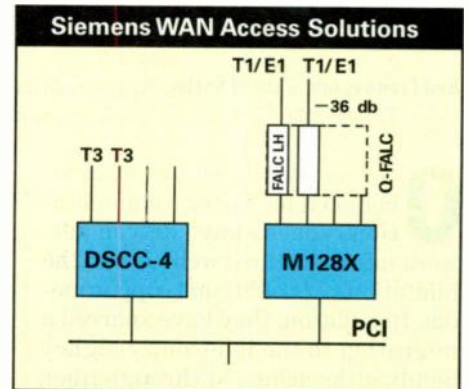
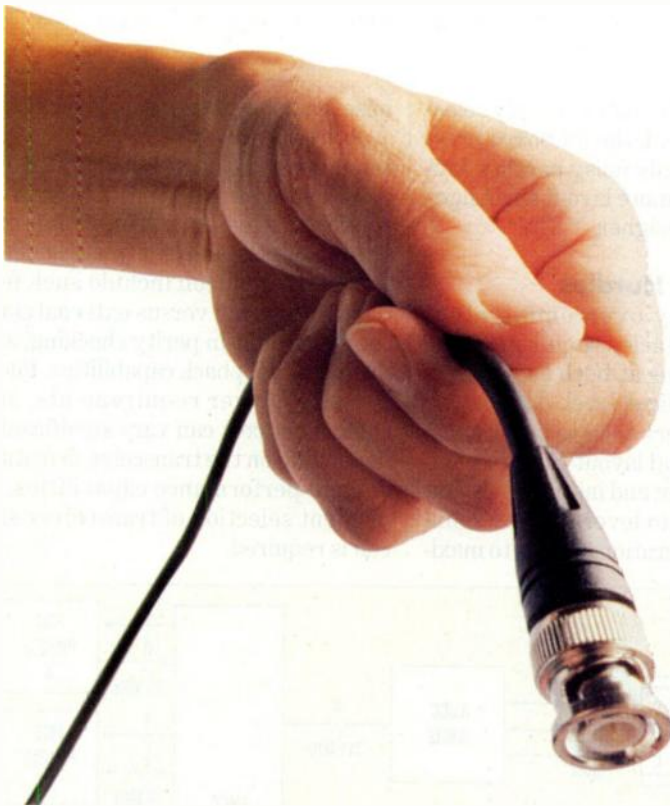
### Recommended Reading:

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2. Lucent Technologies Inc., *1996 Field-Programmable Gate Arrays Data Book*, Oct. 1996.
3. Lucent Technologies Inc., *ORCA FPGAs HDL Design Guide*, 1996.
4. Ott, D., and Wilderotter, T., *A Designer's Guide to VHDL Synthesis*, Kulwer Academic Publishers, 1994.

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## Advance Transceiver Designs To Meet 2.5-Gbit/s Data Rates

*Overcoming The Obstacles Posed By High Frequencies Requires Astute Design Decisions At Both The System And Silicon Level.*

Ken Prentiss and Richard Spehn, Applied Micro Circuits Corp. (AMCC), 6290 Sequence Dr., San Diego, CA 92121-4358; (800) 755-2622 or (619) 450-9333; www.amcc.com.

Over the past decade, the escalating need for faster communications speeds have driven network infrastructures well beyond the limitations of traditional copper media. In addition, they have spurred a migration to the inherently higher bandwidths achieved through fiber optics. Optical links, running at speeds from 622 Mbits/s to 2.5 Gbits/s, have already emerged as the preferred media for campus backbone LANs, storage area networks (SANs), metropolitan area networks (MANs), and wide area networks (WANs). However, from the designers' standpoint, making the leap from 10/100BaseT speeds to 2.5-Gbit/s data rates presents a host of new design challenges.

Many of the tried-and-true basic digital design assumptions that provided ample extra margins and headroom at 10/100BaseT speeds must now be reconsidered in light of the constraints imposed by multi-gigabit data rates. Designing robust transceiver systems that can reliably deal with such high frequencies at the board-edge connector requires pushing the on-board circuitry into a whole new realm, where even relatively short traces can exhibit characteristics of analog transmission lines rather than crisp digital waveforms.

In addition, the higher frequencies show much greater susceptibility to the effects of transient noise on the board and/or to jitter in the data line. Ground and power bus isolation becomes a paramount consideration,

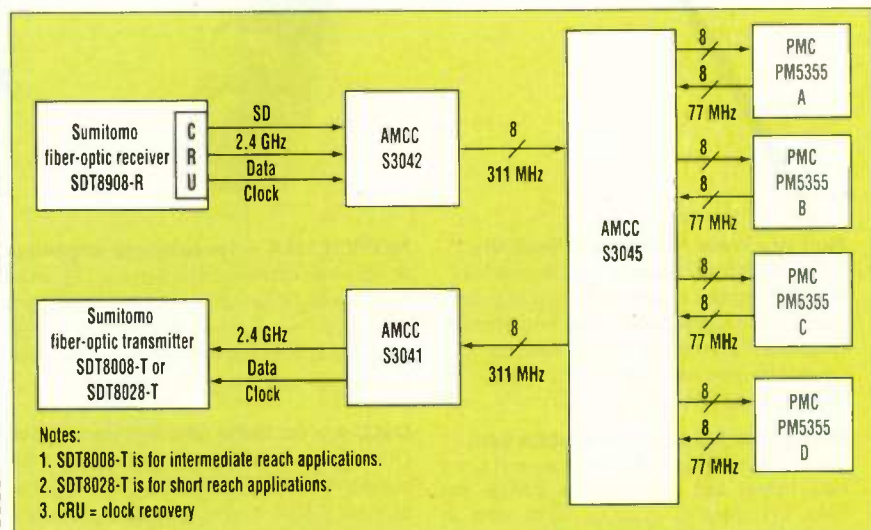
along with careful power-supply selection criteria. And, the on-board presence of potentially noisy parallel data buses provides more layout challenges for the board designer.

### Clearing The Hurdles

Successfully overcoming all of these new obstacles requires astute design decisions at both the system level and the silicon level. Not only do system engineers need to use optimal board design and layout rules to minimize noise, jitter, and interference, but they also need to leverage new semiconductor-integration options to maxi-

mize available margins and headroom.

A critical first step in effective system design is the selection of transceiver components that match your architectural design requirements. Options in the newest generation of transceiver silicon include such features as internal versus external clock recovery, built-in parity checking, and diagnostic loopback capabilities. Package size, power requirements, and component cost can vary significantly depending on the transceiver's feature set and performance capabilities, so prudent selection of transceiver silicon is required.



1. Shown is a block diagram for a SONET STS-48/STM-16 transceiver application designed to provide a fully integrated 2.488-Gbit/s PMD layer. The 2.5-GHz data and clock lines between the board-edge fiber-optic components and the multiplexer/demultiplexer chips represent critical pc-board layout challenges. In addition, the multiple 311-MHz and 77-MHz data streams can present significant noise problems.



For example, let's look at a block diagram for a SONET STS-48/STM-16 transceiver application designed to provide a fully integrated 2.488-Gbit/s PMD layer (Fig. 1). The Sumitomo fiber-optic receiver and fiber-optic transmitter components are paired respectively with integrated demultiplexer and multiplexer devices, which provide the deserialization and serialization functions to convert between high-speed bit-serial and byte-serial data. In turn, the 311-MHz byte-serial data streams to and from these components are interfaced (via an integrated multiplexer/demultiplexer) to a bank of four PMC-Sierra PM5355 devices, each handling a 77-MHz data stream.

As will be discussed in more detail, the 2.5-GHz data and clock lines between the board-edge fiber-optic components and the multiplexer/demultiplexer chips represent critical pc-board layout challenges. In addition, the multiple 311-MHz and 77-MHz data streams can present significant noise possibilities.

### Integration Benefits

Silicon-level integration of transceiver components offers the immediate benefits of sharing the cost of packaging and common reference and threshold generators, as well as opening the door to simplifying the design of complex multi-channel boards. At the silicon-level, having the transmitter multiplexer, receiver demulti-

plexer, and clock recovery all in the same chip set allows for on-chip implementation of closely-coupled loop-timing structures.

For instance, by wrapping the receive timing back around on the transmitter, a channel can essentially be made to look like a complete low-cost terminal to the system on the other side of the transmission link. And by migrating much of the channel-switching functionality down onto a four- to eight-channel transceiver board, designers can better leverage new high-speed system-level switching fabrics, such as serial backplane architectures, that yield improved overall throughput and lower cost per channel.

Not only does sharing the receive clock with the transmitter greatly simplify the clock and timing distribution within the system, it also allows for simple on-chip implementation of repeater timing. The matching of chip-level timing with the network's overall clock synchronization can be especially important as higher-level optical network topologies migrate toward wavelength-switched capabilities (such as wavelength division multiplexing).

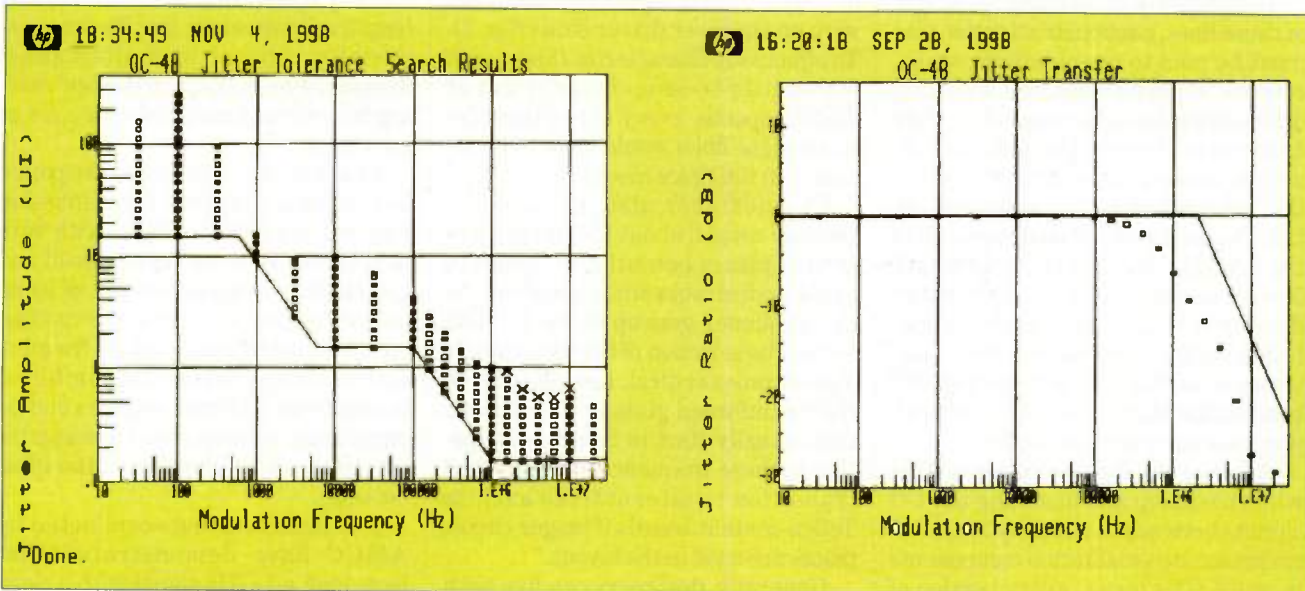
From an architectural standpoint, it's beneficial to conduct chip-level switching of separate wavelength data transmissions while staying completely within the overall network's time domain. Using the same bit-synchronous timing at the chip level also

enables cost-effective implementation of integrated performance monitoring on-the-fly at the repeater level.

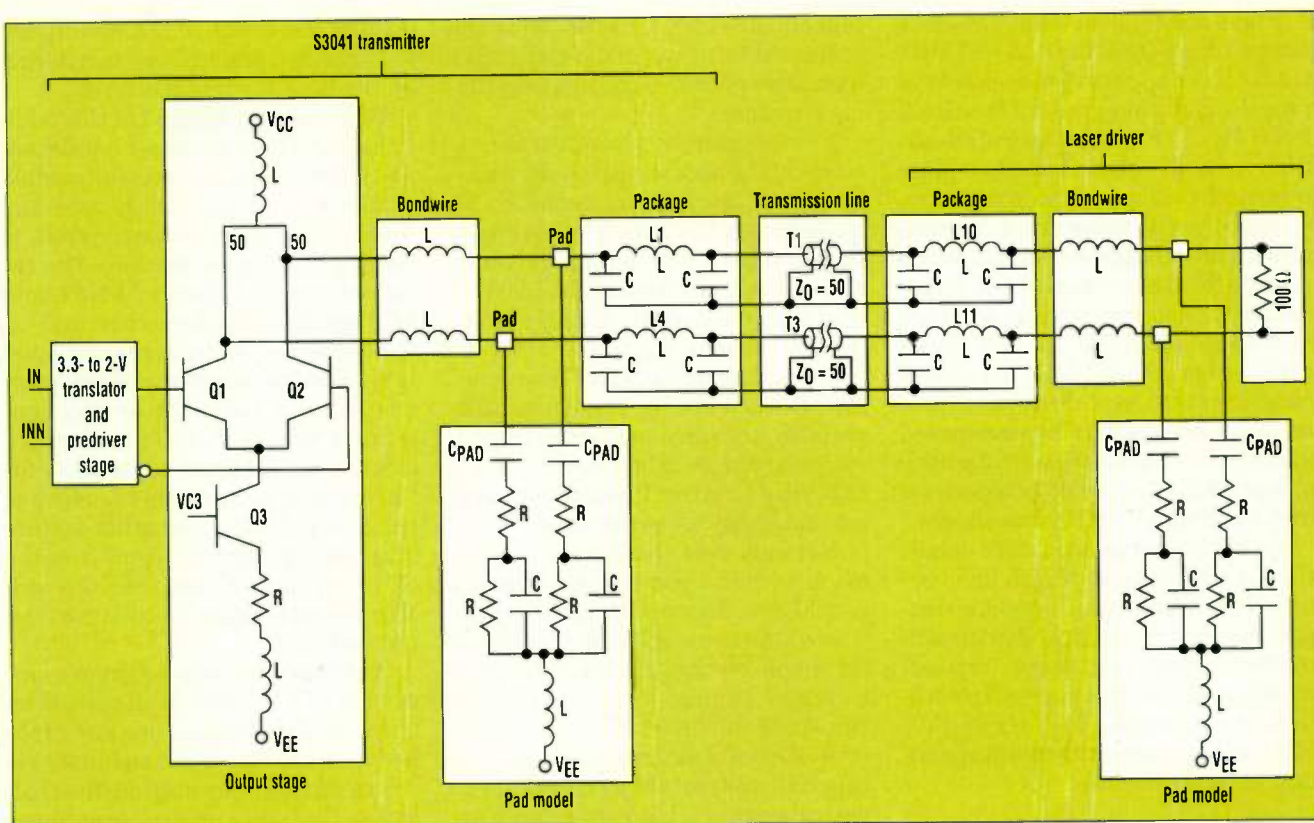
Of course, packing all of this additional functionality onto a multichannel, board-level, transceiver module at 2.5-Gbit/s speeds pushes noise and jitter management to the forefront of design challenges. Because the requirements of Bellcore, ANSI, and ITU specifications have to be met "at the connector," designers must build in appropriate margins at every point where noise and/or jitter may contribute to the overall problem. In essence, the designer has to allow for the nonideal behavior of the electro-optics, equalizers, and other factors involved in getting the signal from the off-board media to and from the serializer/deserializer circuitry in the transceiver.

As transceiver board designs move up above OC-12 (622 Mbits/s) and on to OC-48 (2.5 Gbits/s), one key problem in controlling noise and jitter revolves around transmission-line challenges that were negligible at lower frequencies. In an OC-48 design, both the tolerance for input jitter and the acceptable jitter-transfer ratio drop off significantly as the modulation frequency increases (Fig. 2).

At multi-gigabit speeds, maintaining acceptable circuit-routing and board-layout practices become even more stringent constraints for controlling jitter on the input circuits. In Fig-



2. Above OC-12 (622 Mbits/s), transmission-line effects really come into play. In an OC-48 (2.5 Gbits/s) design, both the tolerance for input jitter and the acceptable jitter-transfer ratio drop off significantly as the modulation frequency increases.



3. The circuit chain between the 3041 transmitter die and the laser driver includes a series of intermediate links between the transmitter's die, bond wire, pad, package, the pc-board transmission line, and then the package and bond wire on the laser driver side. To effectively characterize this overall transmitter-to-laser-driver circuit at 2.5-Ghz speeds, every one of these intermediate links would have to be included in the Spice model.

ure 1, for example, the 2.5-GHz lines between the fiber optics and the multiplexer/demultiplexer chips will by default take on all the characteristics of a transmission line for any connection longer than 2.5 cm.

In addition to minimizing the length of these lines, particular attention also must be paid to terminations, stubs, corners on circuit lines, and balancing differential lines to make sure they have equal electrical lengths. Termination resistors should be as close to the end-point of the line as possible. In the Figure 1 reference design, all of the 2.5-GHz circuits are equal length 50-ohm transmission lines, terminated directly at 50-ohm resistors that are embedded in the S3045 device. Other key issues in layout are to avoid any 90-degree turns in the high-speed lines and to always use adequate decoupling.

Another key factor to keep in mind when modeling and matching the I/O circuits between the fiber optic and serialization/deserialization components is, at 2.5-GHz levels, every portion of the circuit can have a significant impact on the final jitter-tolerance of the

overall link. For example, the circuit chain between the 3041 transmitter die and the laser driver includes a series of intermediate links between the transmitter's die, bond wire, pad, package, the pc-board transmission line, and then the package and bond wire on the laser driver side (Fig. 3). To effectively characterize this overall transmitter-to-laser-driver circuit at 2.5-GHz speeds, every one of these intermediate links would have to be included in the Spice model.

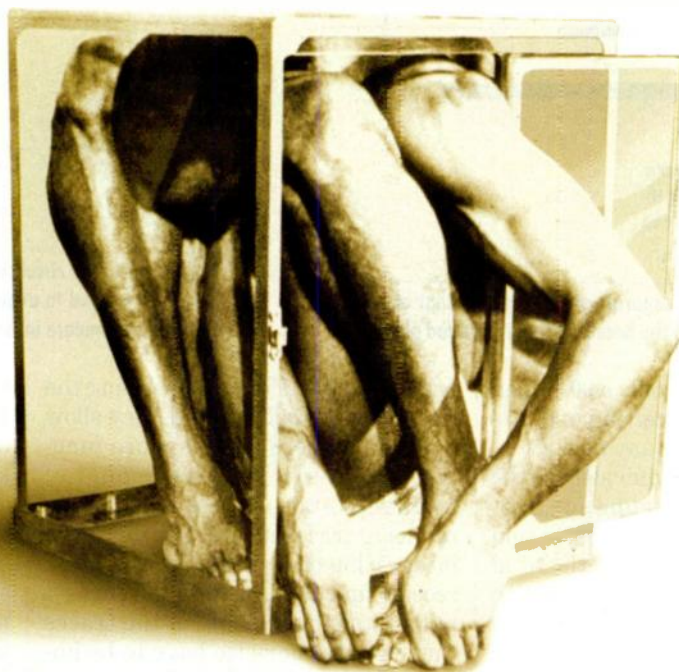
The designer also must be extremely careful about the integrity of ground planes beneath the signals to avoid undesirable cross-coupling. As the frequency gets up beyond 1-GHz levels, the selection of board materials also becomes critical. Less expensive fiber-reinforced glass (FR-4) boards may actually start to become dissipative at these frequencies, requiring a transition to alternatives such as Teflon-content boards if longer circuit traces are used in the layout.

Generally, designers can live with lower-cost FR-4 if they keep high-speed runs very short, about two

inches or less. Here again, the trade-offs in choice of transceiver features and packaging size can play an important role. Keep the transceivers small so that they can be moved closer to the board-edge fiber-optic components, thereby minimizing transmission-line lengths. Transceiver size becomes especially critical in multichannel designs, where both card-edge spacing and overall board real estate are at a premium.

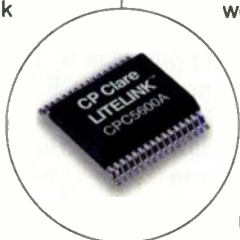
In addition to substrate dissipation issues, longer on-board transmission lines can run into problems with both skin losses from the copper itself and attenuation losses as a result of using only the outer portions of the conductor for signal propagation. At frequencies around 1 GHz, the combined losses from all these sources can be empirically measured as inter-symbol interference or blurring of the ideal bit-edge.

For instance, tests conducted by AMCC have demonstrated that launching a 1-GHz signal with a clean 100% open eye-diagram across a one-foot-long 50-ohm transmission line on an



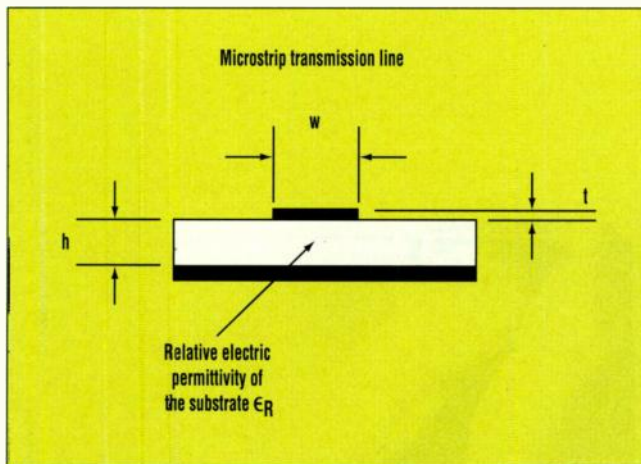
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4. A microstrip provides a separate strip connector that can be dielectrically isolated from the board's primary ground plane.

FR-4 substrate yields only a 90% open eye-diagram at the receiving end. Attenuation losses across any media typically roll-off at a rate equivalent to the square root of the frequency. But when combined with skin-losses and dielectric dissipative losses, the total signal loss begins to drop directly with the frequency increase for frequencies above 1.5 GHz.

Radiated losses also can easily occur at these high frequencies unless return paths and ground planes are carefully maintained in a very clean board layout. If the high-speed trace begins to act as an antenna, it obviously results in two major problems—loss of adequate signal at the destination optic module, and injection of unwanted noise into the rest of the system (such as EMI and/or cross-talk between channels that increases jitter).

Good board design practices include making sure that high-speed traces don't have to jump between different board layers. In some cases, for a trace that has to be longer than an inch or two, it may even be useful to bring it down a layer and make it a microstrip embedded within the board. Essentially, a microstrip provides a separate strip connector that can be dielectrically isolated from the board's primary ground plane (Fig. 4). If the thickness, width, and height of the line above the ground plane are carefully controlled, the microstrip will exhibit a consistent characteristic impedance.

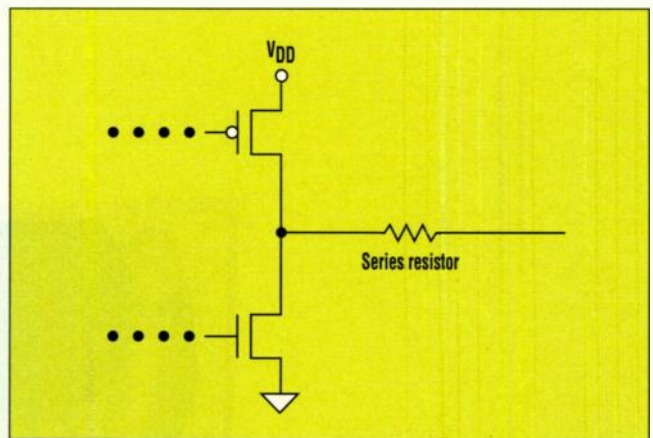
New-generation integrated transceiver chip sets also help with the maintenance of noise and jitter in two

primary ways. First, by reducing the size of the overall package, they allow board designers to pack more functionality into a smaller amount of board real estate while simultaneously reducing trace lengths. Secondly, the integration of both the transmit and receive functions into a single chip set pulls into silicon many of the traces that would otherwise have to be implemented on the pc board.

For example, consider that all of the diagnostic loopback and line loopback circuits are included on-chip, thereby avoiding the need for the board designer to manage a series of inch-long board traces that would have a high potential for radiated losses. Pulling such circuitry into the chip and eliminating the requirement for driving several high-speed board traces also yields a significant power savings, greatly simplifying the overall challenge of power and ground management.

### Bus Isolation Challenges

Maintenance of a low-noise environment relies heavily on the choice of the multilayer board structure and the effective placement of ground planes, along with the type and location of the power supply. While modern switching power supplies can be relatively cheap in terms of power efficiency, in a high-speed 2.5-Gbit/s communications board, they can turn out to be quite expensive in terms of the noise budget. Selecting a power supply rated for 95% efficiency and a seemingly reasonable 200 mV of peak-to-peak noise could create real problems when at-



5. Referring to the circuit in Figure 1, appropriate use of series-damping resistors is needed to avoid ringing from the CMOS output transistors, which can accumulate into noise problems throughout the system.

tempting clock recovery on signals that have only one volt of amplitude outside the chip and amplitudes as small as 0.25 V inside the chip.

Therefore, good power-supply decoupling is required in at least two areas. First, whatever noise the power supply is intrinsically generating must be filtered and smoothed by distancing it at the far end of the board from the critical high-speed analog-like traces. Then the use of distributed decoupling capacitors can effectively average out the noise, thereby getting down to the 20- to 50-mV levels typically required at the PLL power supply pins. Using good low-impedance filter capacitors at the devices themselves, with a direct low-inductance path to the pins, is critical to managing power line noise. And keeping the decoupling capacitors on the same side of the board as the component helps to minimize unwanted inductance due to vias.

### Parallel Bus Interface

Another potential noise generator is the inevitable on-board presence of multiple chips required for functions like framing, segmentation, and re-assembly of data. These are usually CMOS devices that have large single-ended parallel buses operating at various frequencies. For example, the feeds to a large 32-bit, 155-MHz device could easily fall down within the loop bandwidth of the clock-recovery or transmit PLLs, thereby causing significant interference problems. Such a possibility becomes especially likely if the switching bus on the CMOS device

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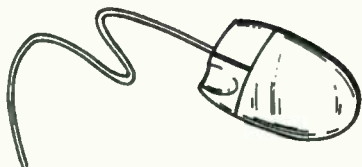
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is processing long patterns of 00-to-FF rollover counts, which are often used in system testing.

The intricacies of parallel bus interface management further underscore the need for good distributed decoupling throughout the board design, not just between the transceivers and the power supply. Referring again to Figure 1, the series of 8-bit 77-MHz interfaces between the four PMC-Sierra devices and the S3045 device would need to be carefully routed to maximize timing margin and minimize coupling risk. Line spacing between all signals of different origin should be at least three to four line widths to reduce the potential for coupling and interference. In addition, the appropriate use of series-damping resistors is needed to avoid ringing from the CMOS output transistors, which can accumulate into noise problems throughout the system (Fig. 5).

### Margins And Headroom

As demonstrated above, next-generation OC-12 through OC-48 multi-channel transceiver systems will rely heavily upon semiconductor-level integration as a key for achieving required performance, simplifying overall board-level design issues, and managing the noise and jitter issues that emerge at higher speeds. In addition to leveraging the further refinement of existing bipolar and CMOS processes, next generation transceiver designs also will benefit from new high-speed and high-integration processes, such as Silicon Germanium (SiGe), which will provide more performance headroom and low-power capabilities.

With almost every component on the transceiver board design (except for the optical module) now available in a 3.3-V configuration, the goals of cost-reduction and noise management are helped by using only one power source and the elimination of multiple requirements for on-board power conversion.

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*Richard Spehn is senior staff applications engineer at AMCC. He holds a BSEE and MSEE from the University of California, Irvine.*



# DESIGN NOTES

## LTC1626: Step-Down Converter Operates from Single Li-Ion Cell – Design Note 196

Tim Skovmand

### Introduction

The LTC1626 is a low voltage, high efficiency, monolithic step-down DC/DC converter featuring an input supply voltage range of 2.5V to 6V, which makes it ideal for single-cell Li-Ion applications. A built-in low  $R_{DS(ON)}$  switch provides high efficiency and allows up to 0.6A of output current. The LTC1626 incorporates automatic power saving Burst Mode™ operation to reduce gate-charge losses when the load current drops. With no load, the converter draws only 160 $\mu$ A and in shutdown it draws a mere 1 $\mu$ A, making it ideal for current-sensitive applications.

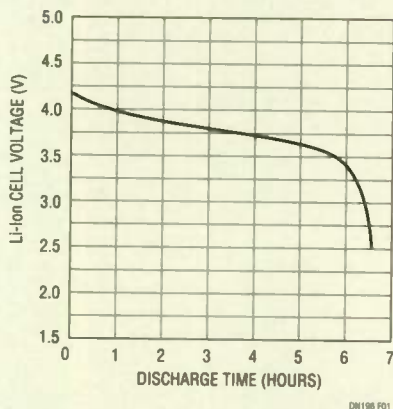


Figure 1. Typical Single-cell Li-Ion Discharge Curve

### Single-Cell Li-Ion Operation

As shown in Figure 1, a fully charged single-cell Li-Ion battery begins the discharge cycle between 4.1V and 4.2V. During most of the discharge period, the cell produces between 3.5V and 4.0V. Toward the end of discharge, the cell voltage drops fairly quickly below 3V. The discharge is typically terminated somewhere around 2.5V (depending upon the manufacturer's specifications).

The LTC®1626 is specifically designed to accommodate a single-cell Li-Ion discharge curve. For example, using the circuit shown in Figure 2, it is possible to produce a stable 2.5V/0.25A regulated output voltage with as little as a 2.7V from the battery, thus obtaining the maximum run time possible.

### 100% Duty Cycle in Dropout Mode

As the Li-Ion cell discharges, the LTC1626 smoothly shifts from a high efficiency switch mode DC/DC regulator to a low dropout linear regulator (that is, 100% duty cycle). In this mode, the voltage drop between the battery input and the regulator output is limited only by the load current and the series resistance of the PMOS switch, the current sense resistor and the inductor. When the battery voltage rises again, the LTC1626 smoothly shifts back to a high efficiency DC/DC converter.

⚡, LTC and LT are registered trademarks of Linear Technology Corporation. Burst Mode is a trademark of Linear Technology Corporation.

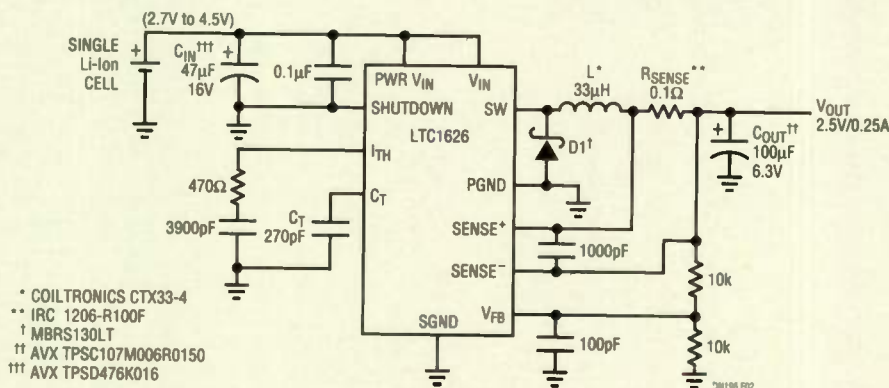


Figure 2. Single-Cell Li-Ion Battery to 2.5V Converter

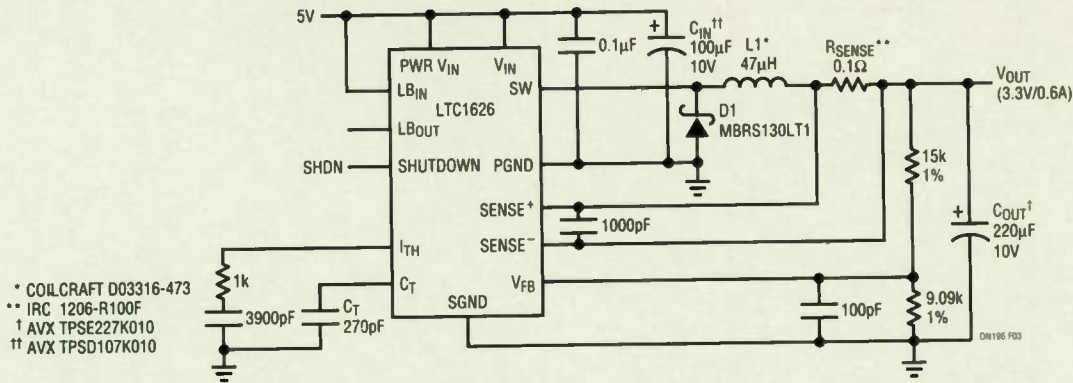


Figure 3. High Efficiency 5V to 3.3V Step-Down Converter

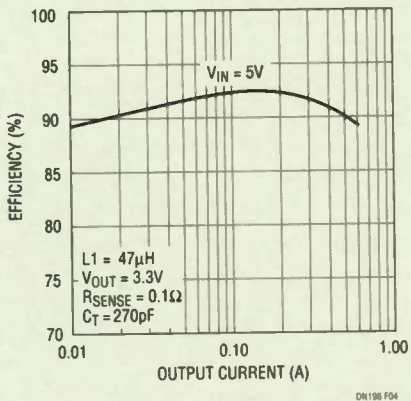


Figure 4. Efficiency vs Load Current

### High Efficiency 5V to 3.3V Conversion

The circuit of Figure 3 shows the LTC1626 being used for board-level conversion of 5V to 3.3V at up to 0.6A. Although a linear regulator could also perform this function, it would result in an additional 1W of power loss. The high efficiency of the LTC1626 (Figure 4) reduces this loss to only 230mW.

### Current Mode Architecture

The LTC1626 is a current mode DC/DC converter with Burst Mode operation. This results in a power supply that has very high efficiency over a wide load-current range, fast transient response and very low dropout characteristics. Further, the inductor current is predictable and well controlled under all operating conditions, making the selection of the inductor much easier.

Current mode control also gives the LTC1626 excellent start-up and short-circuit recovery characteristics. For example, when the output is shorted to ground, the off-time is extended to prevent inductor current runaway. When the short is removed, the output capacitor begins to charge and the off-time gradually decreases. The output returns smoothly to regulation without overshooting.

### Low Voltage Low $R_{DS(ON)}$ Switch

The integrated PMOS switch in the LTC1626 is designed to provide extremely low resistance at low supply voltages. Figure 5 is a graph of switch resistance versus supply voltage.

Note that the  $R_{DS(ON)}$  is typically  $0.32\Omega$  at 4.5V and only rises to approximately  $0.40\Omega$  at 3.0V. This low switch resistance ensures high efficiency switching as well as low dropout DC characteristics at low supply voltages.

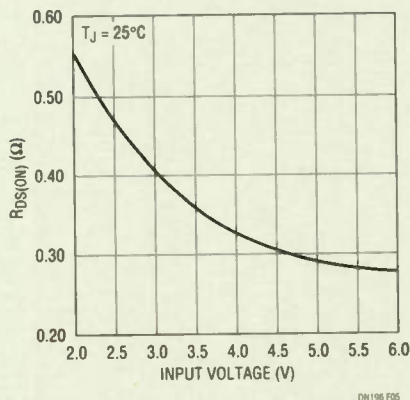


Figure 5. PMOS Switch Resistance vs Input Supply Voltage

### Conclusion

The LTC1626 is specifically designed to operate from a single-cell Li-Ion battery pack. With its low dropout, high efficiency and micropower operating modes, it is ideal for cellular phones and handheld industrial and medical instruments.

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# ANALOG OUTLOOK

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## Class-D Amps Raise Low-Power Systems To The Next Level

*Use Integrated Class-D Amplifiers To Reduce Size, Cost, And Heat Dissipation In Battery-Powered Audio Systems.*

RICHARD PALMER, Texas Instruments Inc., P.O. Box 660199, Dallas, TX 75266-0199; rpalmer@ti.com.

Class-D audio power amplifiers (APAs) were first introduced nearly 50 years ago. Since then, they have been used sparingly in a relatively small number of applications with limited bandwidth, such as public address systems and telephony equipment. This will soon change as a new class of integrated Class-D APAs make their way into such mainstream applications as portable computers, battery-operated music systems, wireless communication devices, and other compact low-power systems.

It's becoming clear that moving to next-generation designs requires taking advantage of this technology's greater power efficiency and its resulting reduction in heat dissipation. The bottom line is that Class-D amplifiers have the potential to reduce system size and cost while extending the life of battery-powered systems.

Only recently have advances in semiconductor fabrication processes made integrated Class-D audio amplifiers possible. Fast-switching, rugged DMOS power MOSFETs can now be integrated with analog circuitry, eliminating the need for a discrete output power stage. The resulting Class-D APA is an effective, highly efficient solution for compact, battery-powered audio applications in the music bandwidth.

In a laboratory test designed to compare the power efficiency of Class-AB and Class-D APAs, a Class-D amplifier extended the life of a battery by 2.5 times. The test took a linear Class-

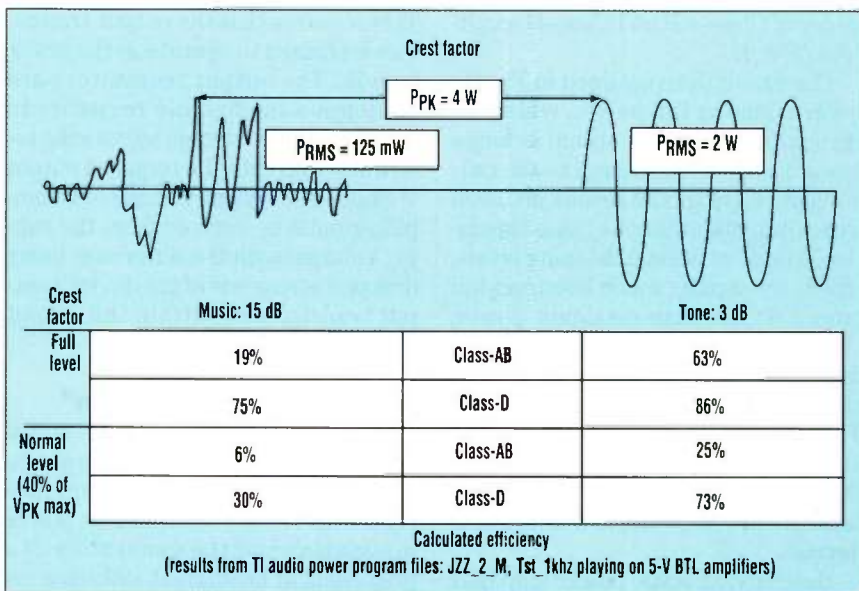
AB APA and placed it on an evaluation platform in a test system with bass/treble volume control modules, dc-dc converter modules, and one 9-V alkaline battery. The test system ran until the dc/dc converter tripped its undervoltage lock-out/lockout at 5.2 V. Subsequently, the voltage in the battery would drift upwards and the system would turn on again. After three such incidents, the test was deemed complete. Then, a Class-D APA was substituted for the Class-AB amplifier and the same procedure was repeated.

It's important to note that the test

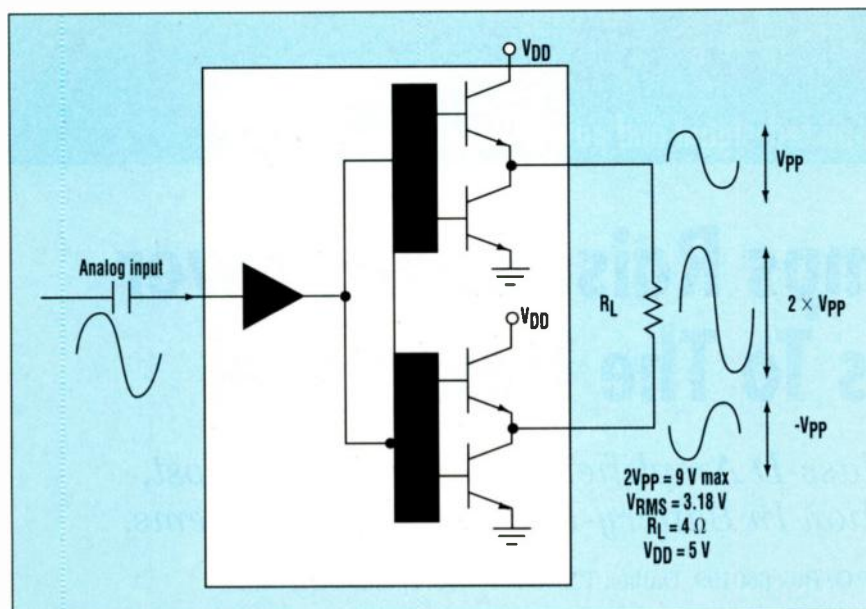
utilizes a real-world signal. Music was used instead of the sine waves or tones that are typically used in a lab to assess the power efficiency of audio amplifiers. Unlike the widely varying and often unruly music signals, tones are uniform and well behaved. In other words, the crest factor of music is much higher than that of a tone.

### Using Crest Factor

Crest factor can be used to analyze the differences between the amplifiers. Essentially, crest factor represents the difference between a signal's



1. The crest factor of music is much higher than that of the sine waves or tones typically used in a lab test of efficiency. This is important to note when comparing test results because crest factor significantly affects an audio power amplifier's power efficiency as these calculated efficiencies show.



2. This diagram illustrates the architecture of a typical Class-AB linear power amplifier used in a bridge-tied-load configuration. The input capacitor forms an RC high-pass filter with the input resistance of the amplifier, and attenuates signals below 20 Hz.

peaks and its RMS power:

$$\text{Crest factor} = 10 \log (P_{PK}/P_{RMS})$$

This is sometimes referred to as headroom. Music signals can have crest factors as high as 15 dB, which means that peaks of over 30 times the RMS value can occur. There is a dramatic difference in test results when music signals rather than sine waves are used to determine the power-efficiency of Class-AB and Class-D amplifiers (Fig. 1).

The simulations outlined in Figure 1 were done at full power, which occurs when the input signal is large enough to drive the output to the rails without clipping. The results are even more dramatic when the same simulation is done at normal listening levels, which are usually much less than full power. At less-than-maximum power, the efficiency of linear amplifiers drops considerably faster than does the efficiency of Class-D devices. These simulation results support the empirical battery-life tests that found that Class-D APAs are two to three times more power efficient than linear devices.

Basically, an audio power amplifier is a special type of operational amplifier optimized to drive low-impedance loads—typically speakers or headphones—at frequencies in the 20-Hz to

20-kHz range. Consider the architecture of a typical Class-AB linear APA used in a bridge-tied-load (BTL) configuration (Fig. 2). The input capacitor forms an RC high-pass filter with the input resistance of the amplifier, and attenuates signals below 20 Hz.

Linear amplifiers derive their name from the fact that they produce an instantaneous output that's equal to a given input multiplied by a constant, known as the gain of the amplifier. This requires that the output transistors be biased to operate in the linear region. The output transistors are analogous to variable resistors in which the input voltage adjusts the resistance to create the required output voltage. The output voltage of an amplifier must be derived from the supply voltage, with the difference being dropped across one of the device's output transistors to attain the output voltage level.

### Linear Amps Always "On"

Even when there is no input signal present, the output transistors are on and drawing precious quiescent current. This results in inefficient power dissipation and the generation of a great deal of heat. Heat sinks are required to transfer the excess heat to the ambient air.

The only way to improve the power efficiency of such an APA is to operate

the output transistors as switches rather than as variable resistors. This means that when the output transistors are turned on, current is passed through the circuit but very little voltage is developed across it. When the switches are off, the circuit has the full supply voltage across it and virtually no current, minimizing  $I^2R$  power losses. This type of switching arrangement is precisely how Class-D APAs operate.

So a Class-D amplifier is essentially a switch-mode power delivery circuit, much like the switch-mode voltage regulators that are found in most personal computers. Rather than using a dc reference to set the output voltage, as switch-mode regulators do, Class-D amplifiers use the audio input signal as the reference.

Class-D APAs rely on a technique known as pulse width modulation (PWM) to sample the input signal and then recreate it as an audio signal at the load. PWM resembles digital data in that it has an on state and an off state. With PWM, a wider time pulse will represent a signal with greater amplitude. These pulses are used to modulate the power FETs on and off so that power is efficiently delivered from the power supply to the load. An output filter smoothes the Class-D amp's PWM output back into an analog waveform that is sent to the speaker.

In a Class-D APA using linear PWM, a square-wave signal with a 50% duty cycle and a frequency much higher than the audio is fed into an integrator to create a triangle waveform at the same frequency (Fig. 3). A comparator then compares the triangle wave with the audio input signal to create a variable-duty-cycle square wave. In effect, a pulse-train is created with a duty cycle proportional to the audio signal level. These pulses then turn the output transistors on and off at a frequency that's much greater than that of the audio input frequency. Finally, a passive inductor-capacitor (LC) low-pass filter is used to remove the high-frequency content of the output signal so that only an amplified version of the input signal is delivered to the load.

The architecture shown in Figure 3 is of an integrated Class-D APA. More specifically, DMOS power FETs are

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integrated on the same piece of silicon as the analog circuitry. This integration reduces the size of the output drive circuit, saving space and decreasing the number of components.

It's important to have a stable power supply, a linear triangle signal, and an accurate and fast voltage comparator to minimize the PWM's distortion level. Feedback can be taken from the output of the PWM just prior to the low-pass filter with little difficulty.

### System Design Issues

With a Class-D APA, the layout of the pc board is critical to the overall performance of the amplifier and the entire system. Faulty layout practices can affect the system's total harmonic distortion and noise by orders of magnitude. Electromagnetic interference (EMI) also can be minimized with care and forethought.

Adding decoupling capacitors close to the power supply and locating high-frequency bypass capacitors close to the power pins will reduce noise from

the supply and help provide current to the amplifier. It's especially important to filter the analog sections of the amplifier because any noise and distortion in this stage will be amplified in the output stage. The input circuitry should be isolated as much as possible from the output circuit, with care taken to avoid ground loops. Adherence to these and other current layout standards will minimize the distortion introduced by the input power and ground loops.

Another aspect of board layout that is central to an effective audio system using Class-D amplifiers is the use of a demodulation filter. This low-pass filter, which removes the high-frequency carrier (the PWM signal) from the amplified audio signal, must be properly located in order to ensure effectiveness.

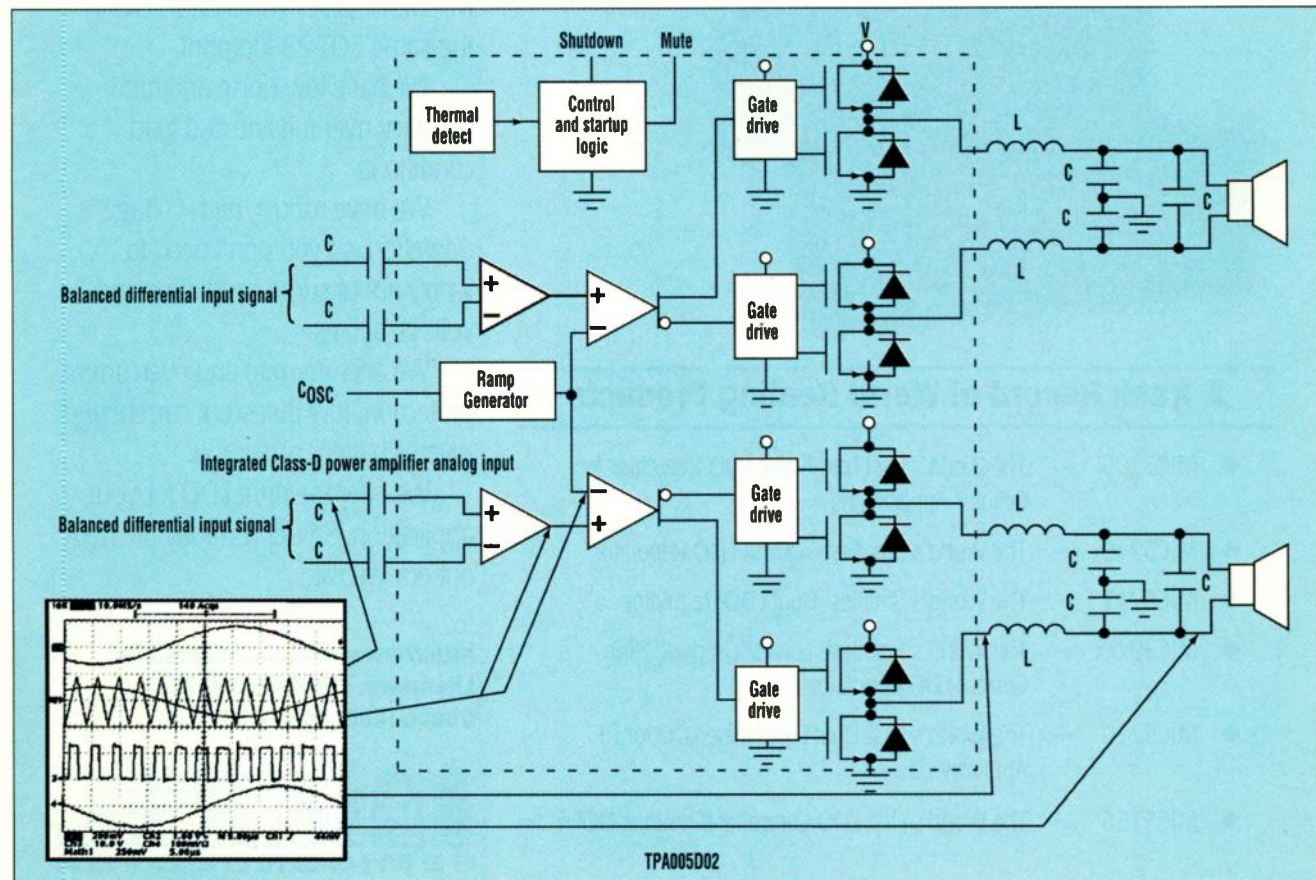
If the Class-D APA output is configured as an H-bridge or full-bridge, a low-pass filter must be used on both outputs. The designer can use a simple passive LC arrangement (Fig. 3,

again). The filter should have a maximally flat magnitude response within the passband, which results in minimal ripple. Ripple would reduce the dynamic swing of the output, lowering the crest factor and introducing asymmetric distortion in the output. The corner frequency is set by the equation:

$$F_0 = 1/(2\pi LC)$$

This is a second-order filter, characterized by a -40-dB per decade attenuation of the output above the corner frequency. As frequency is increased by a factor of 10, the inductive impedance increases by a factor of 10 and the capacitive impedance decreases by a factor of 10. Because the inductor blocks high frequency and the capacitor readily passes it, these factors multiply and the effect is to decrease the high-frequency component seen by the load by a factor of 100 (-40 dB) per decade.

Designers must consider a number of issues when creating this filter.



3. The general architecture of a Class-D audio power amplifier shows that the device is essentially a switch-mode power delivery circuit, much like the switch-mode voltage regulators that are found in most PCs. But rather than using a dc reference to set the output voltage as switch-mode regulators do, Class-D amplifiers use the audio input signal as the reference to create a variable-duty-cycle square wave.

They can increase the filter order by two for each LC combination added. The choice of components and the order of the filter will depend on the switching frequency, since the filter's sole purpose is to remove the switching frequency component from the output. This, in effect, averages the output pulse over one duty cycle. To accurately represent it at the output, the switching frequency should then be much higher than the audio input waveform's highest frequency component. There is a trade-off, however, in that as the switching frequency increases, the switching losses increase as well, reducing the efficiency of the amplifier.

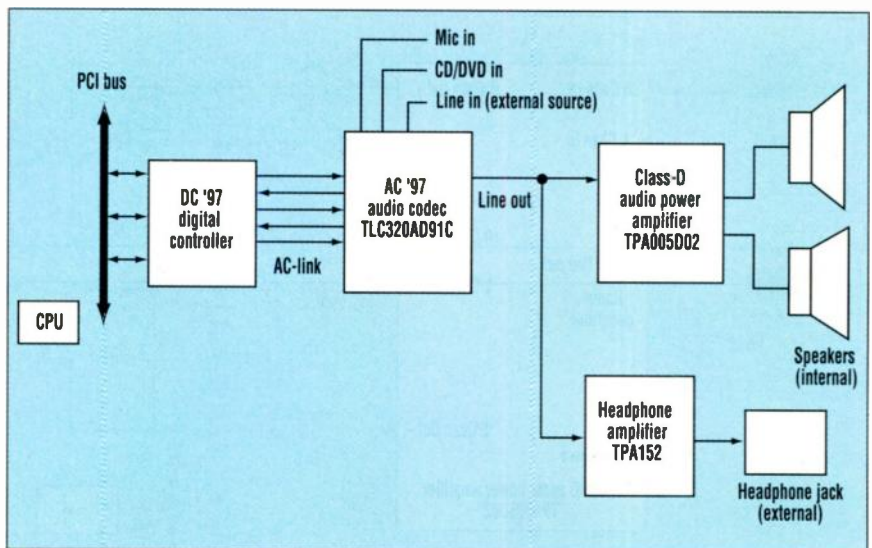
Careful consideration should be given to the low-pass filter because peaking will occur at  $F_0$  when a speaker, which is reactive instead of purely resistive, is placed at the output. Placing a dampening resistor in series with a capacitor across the load or speaker can reduce the peaking.

Power losses also must be taken into consideration during the design of the low-pass filter. Because the inductor is in series with the power signal path, the series resistance of the inductor will reduce the power delivered to the speaker, decreasing the efficiency of the amplifier. The use of low-resistance inductors will lessen this problem.

### Inductor Saturation

The inductors' saturation current also is critical. If the inductor saturates during operation, it looks like a short and will not influence the output signal. As a result, distortion will substantially increase. In the case of a BTL configuration, the inductors' tolerance should be tight for good matching. The capacitors' tolerance should also be tight. Variations in these components can lead to increased harmonic distortion and reduced filter performance through changes in the frequency response.

The filter also contributes a portion of the quiescent current used by the Class-D APA. Because the output of a Class-D amplifier's H-bridge is a switching signal, the capacitors in the filter are either partially charged or partially discharged with each signal transition. Low-leakage, low equivalent series resistance capacitors



**4. A notebook computer is an excellent application for a Class-D amplifier. The digital controller receives and transmits data from the PCI bus, and performs high-quality sample conversions for the audio codec. The codec functions as a slave to the controller, which then performs digital-to-analog conversions, analog-to-digital conversions, analog processing, and mixing.**

should be used to minimize the power dissipated in the amplifier.

If the system allows users access to the speaker terminals, several other issues relating to the low-pass filter should be considered by the designer. First, the output of most low-voltage Class-D amplifiers is usually transferred across a BTL or H-bridge configuration of power MOSFETs in order to increase the maximum output power from a given power supply voltage. In a BTL configuration, neither terminal is grounded and problems could arise if users attempt to plug ground-referenced leads into the output terminals.

A final consideration comes from the fact that the low-pass filter must be designed for a specific load impedance. For example, if the filter is designed for an 8- $\Omega$  speaker and a 4- $\Omega$  speaker is connected to the system, the high-frequency response will be reduced because the bandwidth is reduced. Likewise, if an output filter is designed for a 4- $\Omega$  speaker and an 8- $\Omega$  speaker is attached to it, the corner frequency is increased, which increases harmonic distortion, and the maximum power output is decreased.

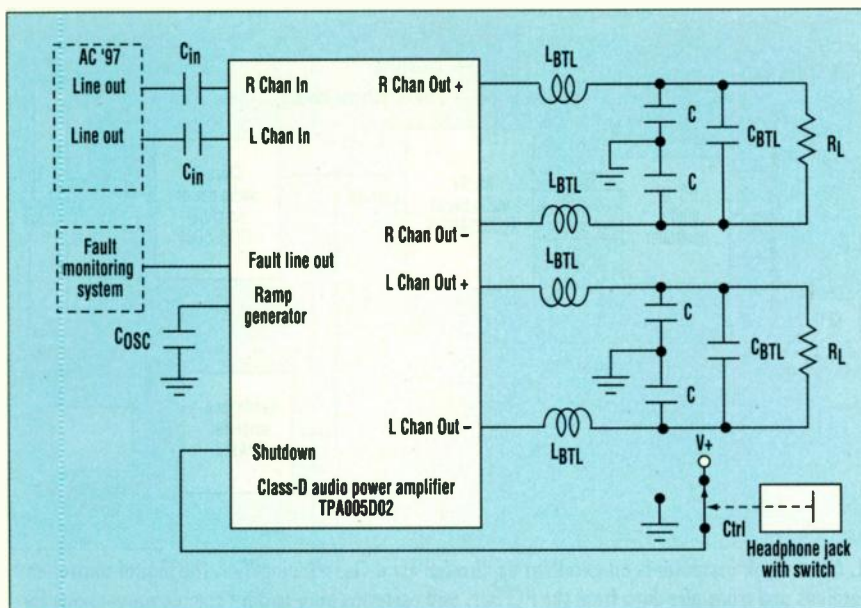
Class-D amplifiers rely on high-frequency switching for their operation, and whenever switching is present in a system, the risk of EMI increases. The output of a typical Class-D APA prior to the output filter consists of

200- to 500-kHz rail-to-rail square waves. EMI will be generated from the pc-board traces connecting the output of the H-bridge to the low-pass filter, and from the inductor. EMI can be minimized by using a shielded inductor and minimizing the trace length between the H-bridge and the filter.

Other sources of EMI are the rise and fall times of the output PWM. Faster rise and fall times require higher frequencies and this, in turn, produces more EMI. There's a trade-off to consider between the higher efficiency provided by the reduced switching losses in the H-bridge and the EMI created. With a tight, well-placed component layout, the EMI produced by high frequencies is minimized, as long as the more sensitive analog circuitry is not close to the EMI-producing power stage.

### Notebook Computer

An excellent application for a Class-D amplifier is a notebook computer because it has certain space restrictions and must operate efficiently to prolong its battery life (*Fig. 4*). The digital controller (DC '97) receives and transmits data from and to the PCI bus. It performs high-quality sample conversions for the audio codec (AC '97). The codec functions as a slave to the controller, which then performs digital-to-analog conversions, analog-



5. This block diagram shows the connection between an audio codec in a notebook computer, a Class-D audio power amplifier, and speakers. The input capacitors are in series with the input resistance of the amplifier, forming a high-pass filter that blocks any dc signals.

to-digital conversions, analog processing such as tone and 3D stereo enhancement, and mixing.

The audio codec accepts analog input from a microphone, CD or DVD, or an external source (Line in) for mixing. It may provide external outputs for connecting headphones (with or without microphones), speakers, speakerphones, or modem connections. A Class-D amplifier can connect to the codec via an analog output (Line out).

Consider the connection between the notebook computer's audio codec, a Class-D APA, and a set of speakers (Fig. 5). The input capacitors, in series with the amplifier's input resistance, form a high-pass filter. This filter blocks any dc signal and sets the low-frequency ( $F_{LO}$ ) -3-dB point at 20 Hz according to:

$$F_{LO} = 1/(2\pi RC)$$

Because the input signal is small, these capacitors can be small, surface-mount ceramics. Ceramic capacitors offer a smaller footprint, lower equivalent series resistance, and a longer life than do electrolytic capacitors. In an environment where high, widely varying ambient temperatures are expected, it's important that the capacitor tolerance and temperature stability be taken into account. As

noted, the second-order, low-pass (LC) filter at the output sets the high-frequency corner ( $f_{HI}$ ) of the desired bandwidth, and must be designed for a specific load impedance.

In the case of a BTL load configuration, the equations used to determine the capacitance and inductance for a given load are:

$$C_{BTL} = 1/(\sqrt{2} R_L \omega_0)$$

$$L_{BTL} = (\sqrt{2} R_L) / (2 \omega_0)$$

where  $\omega_0 = 2\pi f_{HI}$  is the frequency in radians per second.

The high-frequency corner should be far enough above the highest-frequency component of the Class-D APA to avoid attenuation of the audio signals, yet low enough to limit the switching losses due to the switching frequency ( $f_S$ ). For example, to filter  $f_S = 250$  kHz to about 1% (-40 dB) of the amplitude of the audio signal at the speaker requires an  $f_{HI}$  of 25 kHz for a second-order filter. This is high enough to have minimal impact on the audio band. Substituting  $f_{HI}$  into the equation for  $\omega_0$  yields 157 radians/sec. For a 4- $\Omega$  load,  $R_L = 4 \Omega$ ,  $L_{BTL} = 18 \mu\text{H}$  and  $C_{BTL} = 1.1 \mu\text{F}$ . Standard values of  $C = 1 \mu\text{F}$  and  $L = 18 \mu\text{H}$  can be used. Surface-mount capacitors and inductors can be used for the output, reducing the space required for

the filter.

The two other capacitors in the output filter, labeled C, may be added to provide a high-frequency bypass to ground. These capacitors should be approximately 10% of  $2C_{BTL}$ . If the switching frequency is set close to the audio band, then a dampening resistor should be placed in series with  $C_{BTL}$ . The choice of this resistor is based on the impedance characteristics of the speaker.

The frequency of the ramp, or triangle, generator in the APA can be adjusted by an external capacitor,  $C_{OSC}$ , over a wide range. A ceramic capacitor with stable temperature characteristics and a tight tolerance over the desired frequency range should be used because any nonlinearity introduced here will ripple through the system. Increasing  $f_S$  will increase the resolution and attenuation through the output filter. However, this also will increase power losses in the transistors and filter.

The designer also must consider the control pins. Most audio power amplifiers have a shutdown pin so that the amplifier can be placed in a low-power sleep mode. This pin can be connected to the headphone jack so that the APA will be shut down and the speakers disabled when the headphone amplifier is in use. An added benefit of a Class-D amplifier is the device's ability to alert the system when a fault condition, such as under-voltage or thermal overload, is present. These pins can be monitored by the system for a fault condition, making diagnosis quick and efficient.

### Be Well Grounded

When well-established layout practices are followed, a solid ground plane is as effective at reducing electrical noise on a board as a split ground plane or a star configuration. In a star configuration, one location provides a ground connection and all of the traces on the board's network are connected to it. A split ground is often found in mixed-signal systems because it's sometimes necessary to isolate the analog ground plane from the digital ground plane.

The split ground plane has inductance between both sections of the plane that dampens the noise and can cause uneven voltage potentials. How-

ever, a solid ground plane has low resistance so that when a voltage or current spike hits the ground plane, the entire plane shifts up or down. By using a solid ground plane, the overall design of the board can be simpler and will be less prone to errors in layout.

Successful use of a solid ground plane is sometimes dependent upon the architecture of the Class-D amplifier. If the device is configured in such a way that the designer can keep the input and output sections of the chip separated from each other, then the chances are reduced that high- and mid-frequency return currents will make a path to the analog input section of the chip.

The traces for the analog circuit grounds should be extremely short and connected to the ground directly underneath the chip by vias. The power circuit grounds connected to the ground plane should be placed slightly farther out from the chip and closer to the signal and power outputs. This type of arrangement uses the ground plane to separate the large current traces of the output from the input circuitry.

### Next-Generation Amplifiers

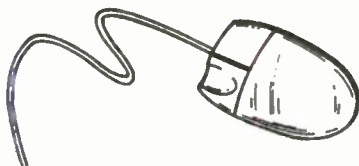
Class-D APAs offer many capabilities that will allow designers to advance many systems to the next generation. Improved power efficiency will extend the battery life of portable systems. Higher efficiency also means less heat dissipation, which in turn reduces the need for heat sinks and other thermal management techniques. This is particularly important for portable applications because it saves board space and allows smaller enclosures.

Because Class-D amplifiers are based on a different technology than Class-AB audio power amplifiers, a different set of design issues must be taken into consideration as Class-D devices are implemented. Just as switch-mode voltage regulators required some getting used to, designers will have to learn the requirements of Class-D amps. But, as with switch-mode regulators, the benefits far outweigh the learning curve.

*RICHARD PALMER is an applications engineer at Texas Instruments Inc. He received his BSEE from the University of Tennessee, Knoxville.*

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Circle 520

# Broken Bulb Safety Trip

C.J.D. CATTO

11 Church Lane, Elsworth, Cambs. CB3 8HU, England, U.K.

A classic safety requirement involves disconnecting the ac mains supply from a light bulb should the glass envelope become broken. Although the filament can draw a much higher than normal current upon exposure to air prior to burning out, this can't be relied on to blow a fuse or trip a miniature circuit breaker (MCB).

With the solution shown, on the other hand, the current through the bulb is sensed by means of the low-value resistor R19 (see the figure). That resistor is then compared with a reference derived from the mains voltage so that fluctuations in the ac mains are compensated out. R9 to R11 act as a voltage divider for the sense voltage developed across R19, and R3-R5, R7, and R8 act similarly

for the mains voltage reference (rectified by D3). D5 and D4 provide rectification and protection.

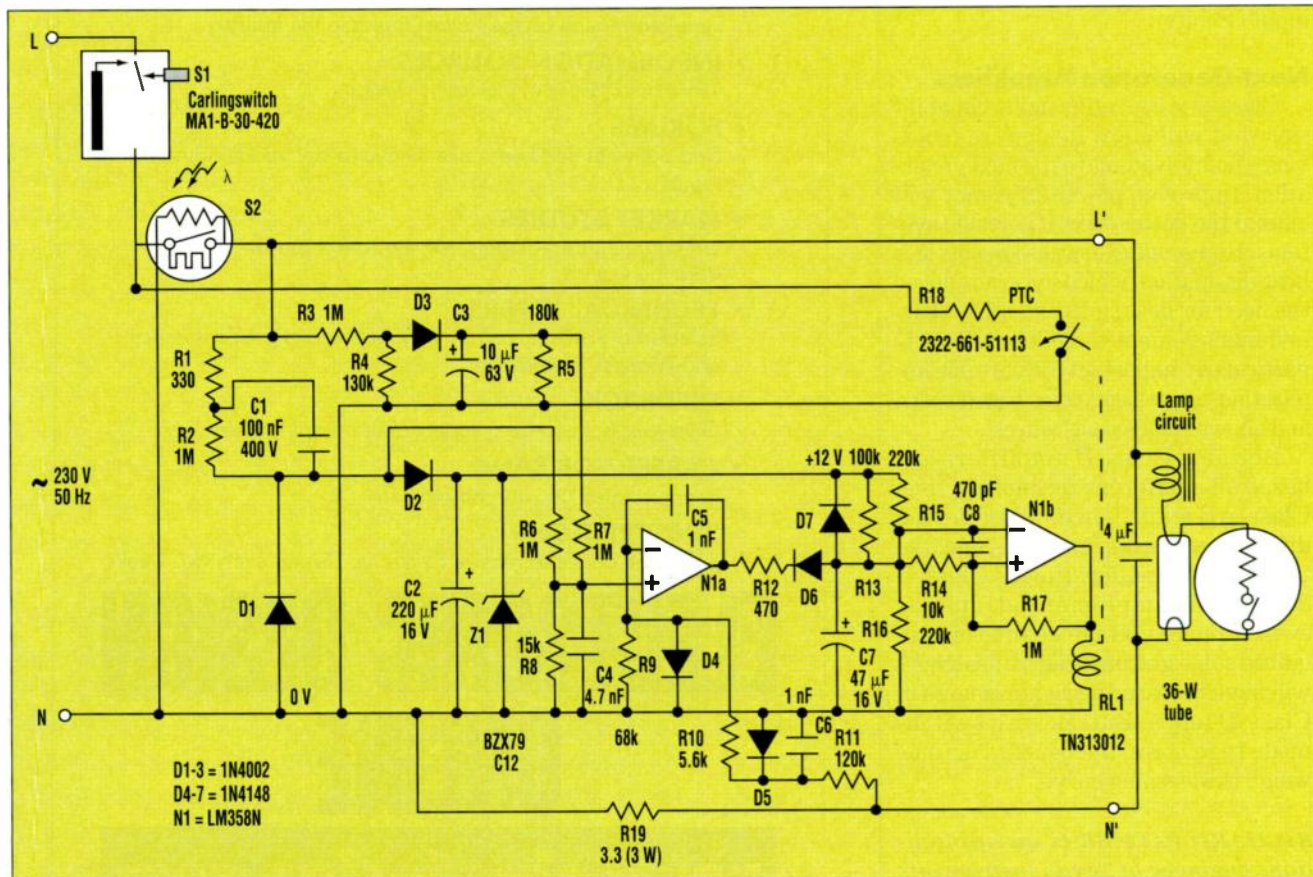
Usually, the output of op-amp N1a is a series of pulses at the mains frequency that keeps C7 discharged via R12 and D6. However, if the bulb current falls substantially below the reference level for more than a few seconds, the voltage on C7 rises until the comparator N1b toggles, activating relay RL1. This, in turn, draws a large pulse of current through the PTC resistor R18, causing the MCB S1 to trip. Thus, the bulb-holder is rendered "dead." Note that S1 also will trip if the bulb is removed, rendering the contacts "safe." A triac may be used in place of the relay.

The current-limiter disk R18 was chosen for reasons of compactness. Its

resistance remains low for just long enough to trip S1, whereas even a large wirewound resistor will often fuse during the surge. Initially, this circuit was developed to offer safety for a 60-W tungsten bulb, but in the arrangement illustrated, a phase-angle detector has been added. As a result, the lamp may take the form of a fluorescent tube.

With a conventional ballast, consisting of a series inductor and a parallel capacitor, one has to be able to tell the difference between "normal" current (which is roughly in phase with the mains voltage) and the "no tube" current (which can be appreciable, but leads the voltage by 90° due to the large compensating capacitor). A leading ac reference from C1 is fed into N1a via R6, making the latter behave as a phase-sensitive detector. The output pulses at R12, D6 spend much more time high than low if the tube is removed or broken (and the in-phase current consequently disappears).

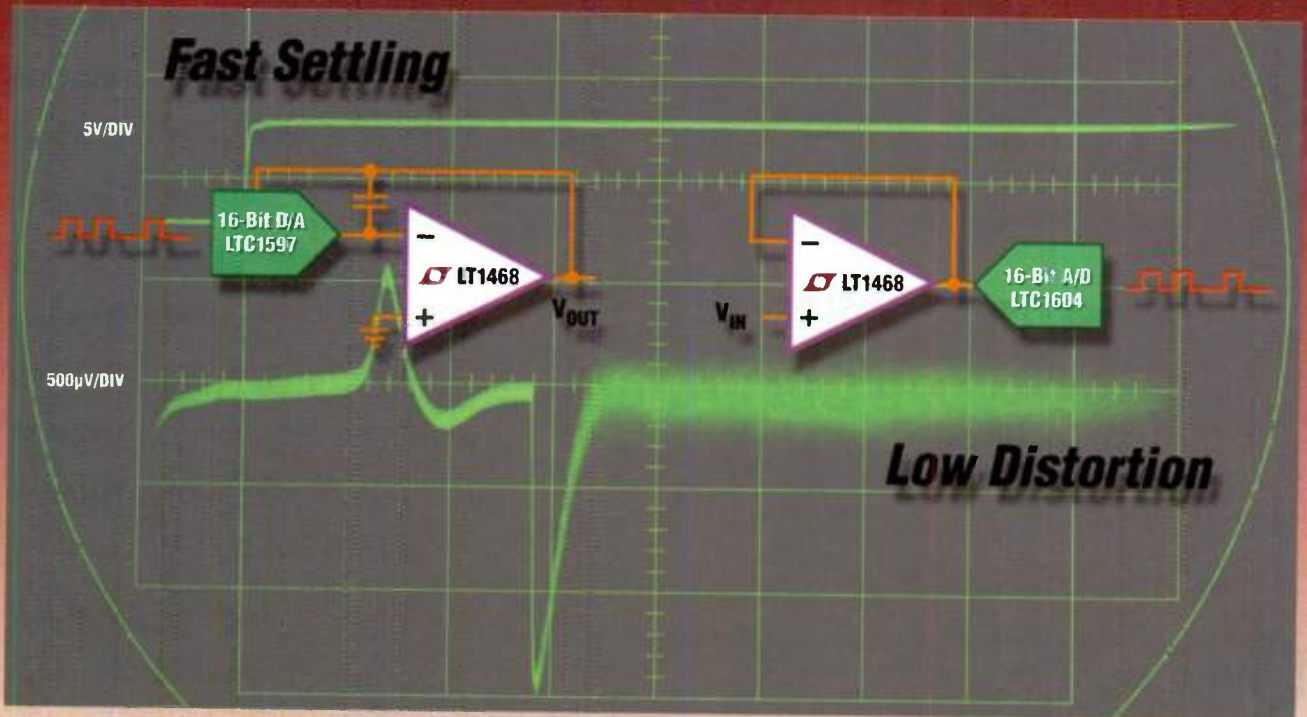
This can be understood by seeing what happens in the absence of the



This design eliminates the weakness in conventional earth-leakage circuit breakers, which don't trip until they have delivered a shock to someone touching the live wire. The addition of phase-angle detector circuitry allows it to be used with fluorescent lamps.



# Fast Settling, Low Distortion Op Amp For 16-Bit Data Conversion



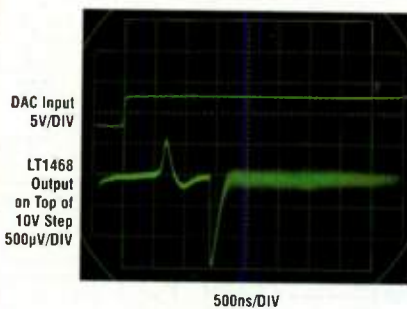
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tube: Appreciable current is drawn through the compensating capacitor, but the signal produced at N1a's inverting input is overcome by the signal from C1 at the noninverting input. Thus, the output goes high. C1 additionally serves as a capacitive-divider or charge-pump to create the 12-V rail to power the circuit. To allow for random firing of the discharge upon

initial switch-on, R13, C7 provides a delay of four seconds. A photoelectric switch S2 can be added to provide dusk-to-dawn lighting control.

Note that for the circuit as drawn, the MCB is tripped through overcurrent when RL1 closes. However, if an MCB with an additional high-resistance coil ("voltage coil") is available, this coil can be employed for

tripping. Hence, R18 can be omitted. Unfortunately, such MCBs aren't common. As an overall safety device, the novel system described here has an advantage over an earth-leakage circuit breaker alone, since it trips with a broken lamp even if no earth-leakage has occurred. Thus, the remnants of the lamp are "dead," not "live" until touched!

Circle 521

# Microcontroller-Based Sine-Wave Generator Has Crystal Accuracy

YONGPING XIA

Teldata Inc., 8723A Bellanca Ave., Los Angeles, CA 90045.

One way to generate a sine wave is to pass a square wave through a low-pass filter. The high-order harmonics will be filtered out, leaving only the fundamental. The higher the order of the filter, the purer the sine wave produced.

The MAX292 is an 8th-order Bessel low-pass switched-capacitor filter. Its -3-dB corner frequency is controlled by its clock frequency in a 1:100 ratio.

Using a 1:64 input-signal/clock ratio will produce a very clean sine wave. If this ratio is kept constant across the entire input frequency range, the amplitude of the filter output will be independent to the frequency.

Here, a high-speed microcontroller (Atmel's AT90S1200) is used to generate square-wave and clock signals (*see the figure*). Meanwhile, the microcontroller accepts 13-bit frequency-con-

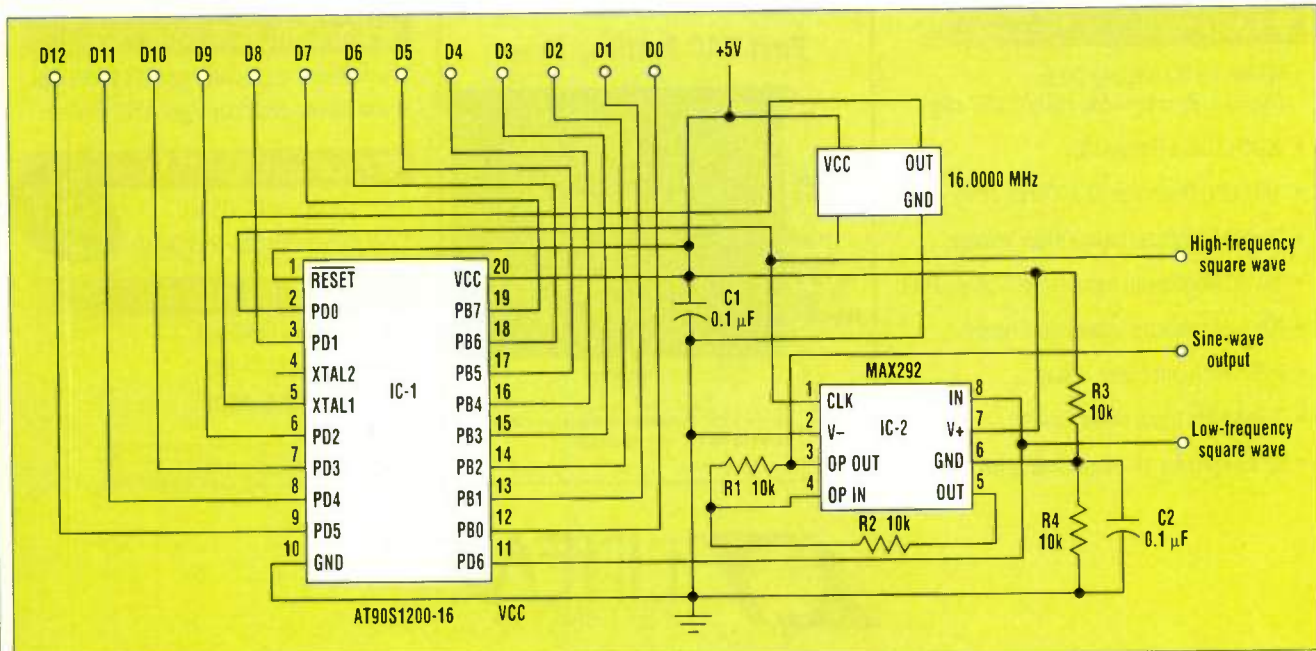
trol signals. The 13 bits are divided into two parts—the lower eight bits (D7-D0) are named delay\_1, and the upper five bits (D12-D8) are named delay\_2. No matter what frequency is selected, the base square wave and the clock will maintain a 1:64 ratio. Thus, the circuit will generate both sine-wave and square-wave signals at the base frequency, as well as a higher (64x) frequency square wave.

The frequency of the sine wave is given by:

$$f_{OUT} = f_{OSC} / (98688 * (\text{delay\_2} - 1) + 384 * \text{delay\_1} + 1408)$$

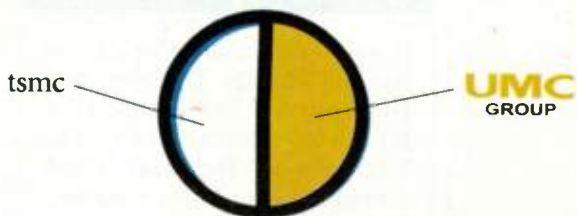
where  $f_{OUT}$  is the sine-wave frequency and  $f_{OSC}$  is the clock frequency of the microcontroller.

To generate a specific frequency sine wave, the values of delay\_1 and delay\_2 can be calculated from the equation above. For instance, assume  $f_{OSC}$  is 16 MHz and a 60-Hz sine wave

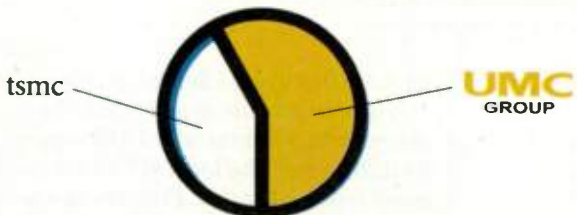


This programmable signal generator can generate sine waves between 5.2282 Hz and 8928.6 Hz when operating with a 16-MHz clock.

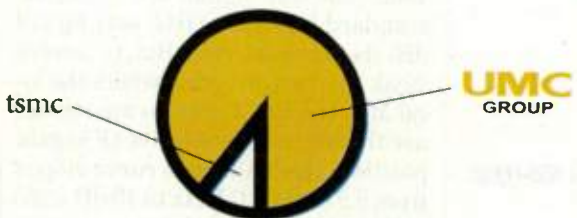
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```

; Microcontroller-Based Sine-Wave Generator
; Author: Yongping Xia
;
#include "1200def.inc"
device AT90S1200

.def cnt          =r16
.def out_data     =r17
.def delay_1      =r18
.def delay_2      =r19

RESET:
ser      out_data          ; pull-up resistors on
out      PORTB, out_data  ; pull-up resistors on
out      PORTD, out_data
ldi      out_data, $00    ; set PORTB direction
out      DDRB, out_data
ldi      out_data, $41    ; set PORTD direction
out      DDRD, out_data

loop_1:
in       delay_2, PINB    ; read PORTD
ror      delay_2
andi    delay_2, $if
in       delay_1, PINB    ; read PORTB

loop_2:
dec      delay_1
brne    loop_2
mov     out_data, cnt
dec     delay_2
brne    loop_2
ori     out_data, $3e
out     PORTD, out_data  ; send out signals
dec     cnt
rjmp    loop_1
    
```

is needed. By using this equation, you can determine that delay\_1 and delay\_2 should be 177 and 3, respectively. Plugging these numbers back into the equation, the calculated output frequency will be 59.98 Hz.

The useful frequency range that can be generated by this circuit is between 5.2282 Hz and 8928.6 Hz when the microcontroller operating at a 16-MHz clock frequency.

**IFD WINNER**

R. N. Schouten, Faculty of Applied Physics, DIMES, Delft University of Technology, P. O. Box 546, 2600A Delft, The Netherlands. The idea: "High-Voltage Power Pulse Circuit". December 1, 1997 Issue.

**Circle 522**

# Frequency-Selective Gain Increases Dynamic Range Of An Active Antenna

M.J. SALVATI

Flushing Communications, 150-46 35th Ave., Flushing, NY 11354; (718) 358-0932.

This much-improved version of the "High-Gain Broadband Active Antenna" (ELECTRONIC DESIGN, Jan. 6, 1997, p. 164) features wider bandwidth and lower noise at half the power consumption and a fraction of the cost (the IC complement here costs about \$1.20 versus \$10 for the previous version). But its most important difference is a method of coping with the problem that plagues all active broadband antennas: How to achieve high gain for weak shortwave signals without being overloaded by the local medium-wave broadcast transmitters.

The figure-eight polar pattern of an electrically short dipole has sharp nulls, allowing you to null out on-frequency interference by rotating a short dipole antenna. However, the output impedance of an electrically short dipole is too high to drive a receiver directly.

Therefore, dual FET source followers are used to present a high impedance to the antenna elements, and provide power gain to drive the LM733 integrated circuit. This, in turn, supplies voltage gain to compensate for the small capture area of the antenna elements. The toroidal transformer that follows provides differential-to-single-ended conversion and impedance matching to the 75-Ω load. Moreover, it multiplexes the output signal and dc supply voltage on the coax connecting the antenna unit with the power supply/receiver end of the system (where another circuit separates power and signal).

To facilitate this multiplexing, the circuit is configured for single-ended operation by biasing the LM733 inputs (pins 1 and 14) at approximately 6 Volts. Total power requirement is

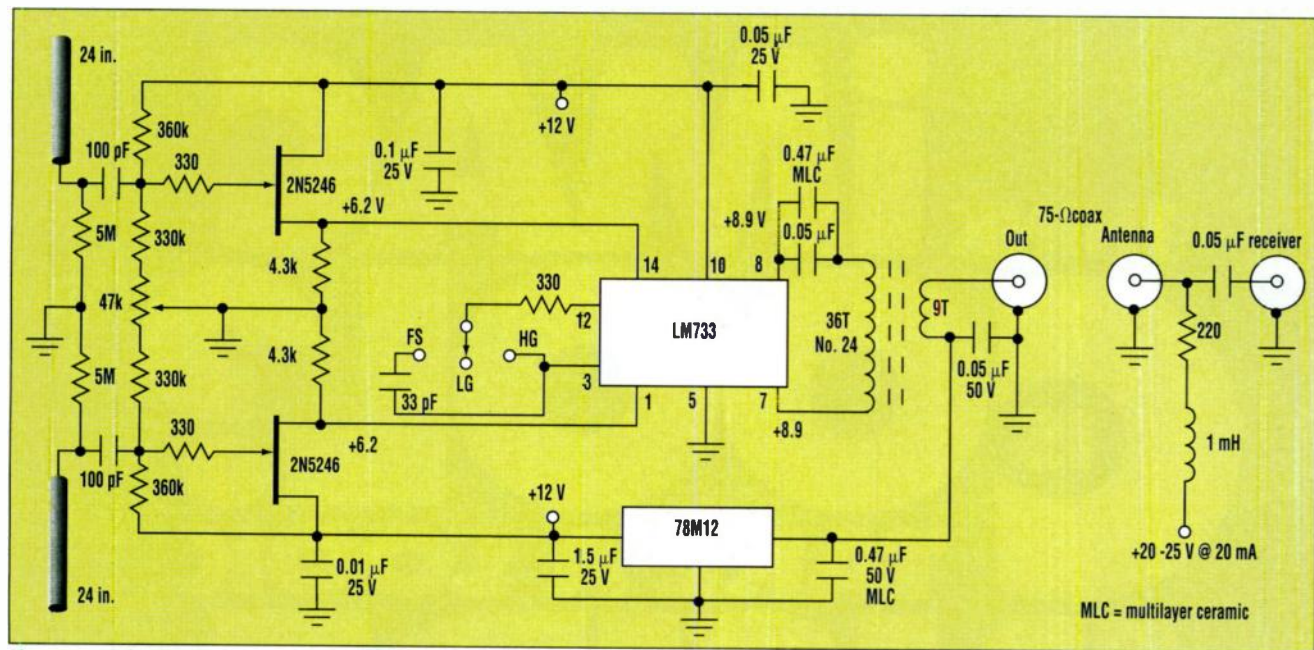
20 mA when using a 20-25 V dc supply.

The circuit gain is selectable by a subminiature center-off SPDT toggle switch to suit the local RF environment (see the figure). For strong-signal areas, the low gain (9 dB) position is best. When all signals are weak, the standard high gain (HG) setting (19 dB) should be selected. But, to receive weak shortwave signals where the local MW broadcast stations are strong, use the frequency-selective (FS) gain position. Here, the gain curve slopes from 9.9 dB at 1.6 MHz to 19 dB at 25 MHz, so you get high shortwave amplification with simultaneously low medium-wave amplification.

The frequency response at low gain is very flat (±0.2 dB) from 200 kHz to 35 MHz, and is only 0.4 dB down at 60 MHz. At standard high gain, the response is very flat to 25 MHz and -3 dB at 50 MHz. The maximum output level in all gain configurations is over 500 mV rms into a 75-Ω load.

A matched pair of high-frequency low-capacitance FETs, such as the 2N5246 with an I<sub>DSS</sub> of about 3 mA, is the best choice for the input stage. It's important to minimize the input capacitance by using miniature carbon-film resistors and minimal board footprints for the gate connections.

The toroidal transformer's primary is 36 turns of No.24 enameled wire wound on a core from a Sony 1-421-



This improved version of the "High-Gain Broadband Active Antenna" from a previous Idea For Design has much wider bandwidth and lower noise, at half the power consumption and a fraction (approximately 12%) of the original parts cost.

302 line choke. Its secondary is nine lengths of 3/8-in. thin-walled aluminum tubing (old TV antenna elements are ideal). The 50k trim pot should be adjusted for equal clipping of the output signal peaks at just past maximum output.

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BOB PEASE

# Bob's Mailbox

## Dear Mr. Pease:

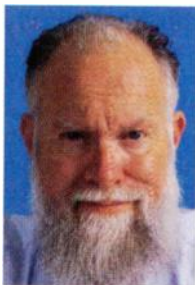
In the Aug. 3 issue of *Electronic Design*, you mention the Heathkit C.D. ignition system. I believe it was the same as the Delta unit that I have been using for many years. I have one installed in my '69 Bronco, and another in my '71 Ford F-250. Both were installed sometime around 1972, and have been functioning with no failures. I recently came across a box full of the same at an auction—some working and some not—cheap. My experience with these is that the usual failure is the SCR, and second the inverter transistors. The whole system is fairly simple. The inverter supplies the high voltage to charge a capacitor. There's a trigger circuit, and that's about it.

Now, on another subject, Home Circuits: I have a front and rear entrance. The front has a motion detector, but I normally park in front and use the rear entrance. Being in a rural area, it gets black out here. I didn't want a motion detector in the rear, as I didn't want it on at times.

What I did was wire a relay to "Blip the motion detector," which would cycle it. The motion detector lights also turn on the side and rear lights at the same time. So, I have three minutes to park, unload, and walk to the rear—under lights. The reverse is the neat part.

I rewired the rear doorbell with an SPDT switch. I charge a large (2000  $\mu$ F) capacitor through a resistor. The switch grounds the doorbell and Blips the motion detector relay by discharging the capacitor through the relay to the ground. The resistor controls the rate the capacitor charges (to prevent anyone from holding the switch in and keeping the lights off). Now, on leaving the rear door, I can cycle the motion detector by hitting the doorbell, and visitors are greeted by the lights coming on. Or, I have the lights for my normal exit and they turn themselves off. The system works quite well, and I had a similar setup in a house I used to own.

**JOSEPH J. SYCZYLO**  
*Sy-Enterprises*  
 North Fork, Idaho



*Isn't it amazing how a study of our different "consumer needs"—and a little customizing of circuits, delays, interlocks, and interactions—can lead to some very versatile applications? And surprise the heck out of the deer and raccoons, too!—RAP*

## Robert:

You learned to type the HARD way. I took a typing and shorthand class (only two males in our class!) when I was in the 11th grade of high school. (No, because I learned in the 4th or 5th grade. Learning skills there are better than in the 11th grade. /rap) I was thinking those two skills would come in handy when I entered Ohio State University (taking notes during lectures, typing English essays, etc.).

Well, I did quite well in both typing AND shorthand, being "certified" at 125 wpm in both (mechanical typewriters, I might add!). I made one big mistake, however: I didn't continue with the typing and shorthand classes during my Senior year. So, by the time I entered university the following fall, I'd TOTALLY lost my shorthand skills. I DID manage to keep my typing speed up.

Now that I'm much older, I can still do a respectable 80 to 90 wpm in "straight text" on a decent keyboard. I come to a screeching halt, however, when numbers are thrown in.

Thank you, Robert, for all your erudite writing(s). Please don't ever stop!

**KARL H. KANALZ**

via e-mail

*Hey, I'm happy with 30 wpm.—RAP*

All for now. / Comments invited!  
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READER SERVICE 84

# Op-Amp Audio

## Minimizing Input Errors

**F**or this second December issue, the column looks at a number of op-amp issues regarding their use in high quality audio circuits. For now, this wraps up the series on this topic. As noted below, this final 1998 installment also marks my departure from this regular monthly column, in order to partake in a new project.

**Op-amps and audio:** Recalling the imperfect op-amp gain stage model printed in the Sept. 1 column, we will first review it with regard to the error sources, V1-V5 (Fig. 1). There is an errata note for the OP177 data sheet circuit originally referenced. It was Figure 3 on early revisions, but Figure 24 now.

In the first two parts of the series, we discussed using buffers (both IC and discrete), along with their role in minimizing output-to-input power-related errors. This error source is symbolized by V5, with the dotted coupling indicated. With the use of an appropriate U2 buffer or load-immune op amp U1, we'll consider V5 errors negligible, and then move on to the others.

The remaining errors are V1-V2 and V3-V4, four in all. But note that these are *paired* error sources, so if you understand how to deal with one of the pair, you also can deal with its twin. In essence, these pairs reduce to two basic types of error sources, each with distinct minimization solutions.

**V1-V2 source-impedance-related errors:** V1 and V2 are ac errors, and they are proportional to the impedances seen at the op amp's (+) and (-) inputs (again as indicated by the dotted coupling). Understanding a very basic semiconductor distortion mechanism is helpful here.

A byproduct of semiconductor manufacture is the fact that often, the junction capacitance is a nonlinear function of applied voltage. Applied ac (audio) modulates this capacitance, which gives rise to even-order harmonic distortion. You can see the basis of this by studying various transistor data sheet C/V curves. Note that it doesn't matter if such junctions are

within a discrete transistor or an IC, the result is the same.

For audio circuits, taking various steps can help to minimize distortion due to this nonlinear capacitance. One is to bias the capacitance to a high dc voltage. Another is keeping the ac signal swings small. A third step is to choose devices with less raw capacitance (and therefore, less sensitivity), and, finally, operating with low source impedances.

In op-amp circuit configurations, it is important to note this input stage distortion mechanism applies to *non-inverting-mode operation*, such as in Figure 1, where the applied common-mode (CM) voltage is highest. And, in terms of susceptible device categories, by and large it is found in op amps using *junction-isolated* FETs (JFETs). Note also that it is not a factor in inverting mode circuits, since by nature these don't see CM voltage.

Within JFET-input op amps there are actually two such capacitors present, corresponding to V1 and V2 errors. They are directly in the signal path, with one appearing at each input terminal, i.e., the gate of the FET input devices. The capacitance is formed as part of the manufacturing process. It electrically appears between the corresponding input and one supply rail, or ac common (for p-channel FET amplifiers the rail is typically  $-V_S$ ).

In Figure 1, source resistance  $R_S$  and the internal nonlinear capacitance of U1 form a low pass filter at some high frequency—usually well above the audio bandwidth. However, this seemingly innocuous relationship doesn't fully reveal what can happen in sensitive, low-distortion circuits, or if  $R_S$  is high. Or, worse yet, when the op amp has appreciably higher input capacitance (as it might in the case of large-junction, low-noise input transistors). All these factors exacerbate the distortion generation.

Normally it is an audio rule-of-

thumb to use low feedback resistances to minimize noise contribution. In Figure 1, the feedback source resistance ( $R_{S(-)} = R_F \parallel R_{IN}$ ) is  $<1 \text{ k}\Omega$ , but the input  $R_S$  may be higher, so the amplifier's  $R_{S(+)}$  and  $R_{S(-)}$  aren't necessarily equal. In practice, given the very-low-distortion capability of today's op amps, (THD+N of  $-100 \text{ dB}$  or better), it is easily possible to see distortion effects due to mismatched  $R_{S(+)}$ .

Fortunately a neat distortion solution is at hand, involving profitable use of the op amp's basic nature. Any such op amp always has *two* similar nonlinear capacitances, and with the input devices matched, it can be assumed the capacitors are the same. So, the distortion effects can be balanced and nulled, if within the external circuit,  $R_{S(-)}$  is made equal to  $R_{S(+)}$ . Or, more precisely, when the total impedance seen looking out of the (-) input is made equal to that at the (+) input.

With an equal source impedance condition, the two sets of distortion components generated by the nonlinear capacitances match, or  $V1 = V2$ . Since this distortion is CM to the op amp (not differential), it is rejected. A distinct operational "sweet spot" occurs, with even-order output THD going to a minimum.

Therefore, to optimize noninverting op-amp circuits against V1-V2 errors, choose  $R_{IN}$  and  $R_F$  so their Thevenin equivalent value is equal to  $R_S$ , which minimizes distortion.  $C_F$ , if used, can upset exact high-frequency balance. For such cases, a compensating value can be used, from pin 3 to ground.

Wondering about your favorite op amp's susceptibility to this distortion? A good test for it is a noninverting gain stage of 2X (with  $R_{S(-)} < 1 \text{ k}\Omega$ ), and  $R_S$  switchable between  $<R_{S(-)}$ ,  $=R_{S(-)}$ , and  $>R_{S(-)}$ . With V1-V2 errors, THD+N plots vs.  $R_S$  can reveal higher distortion for mismatches.<sup>1</sup>

Extrapolating JFET-input op amps to even more sensitive topologies leads us to Sallen-Key active filters, which, by definition, use noninverting amplifiers (often unity-gain, JFET-based followers). For absolutely lowest distortion here, a mirror-image



WALT JUNG



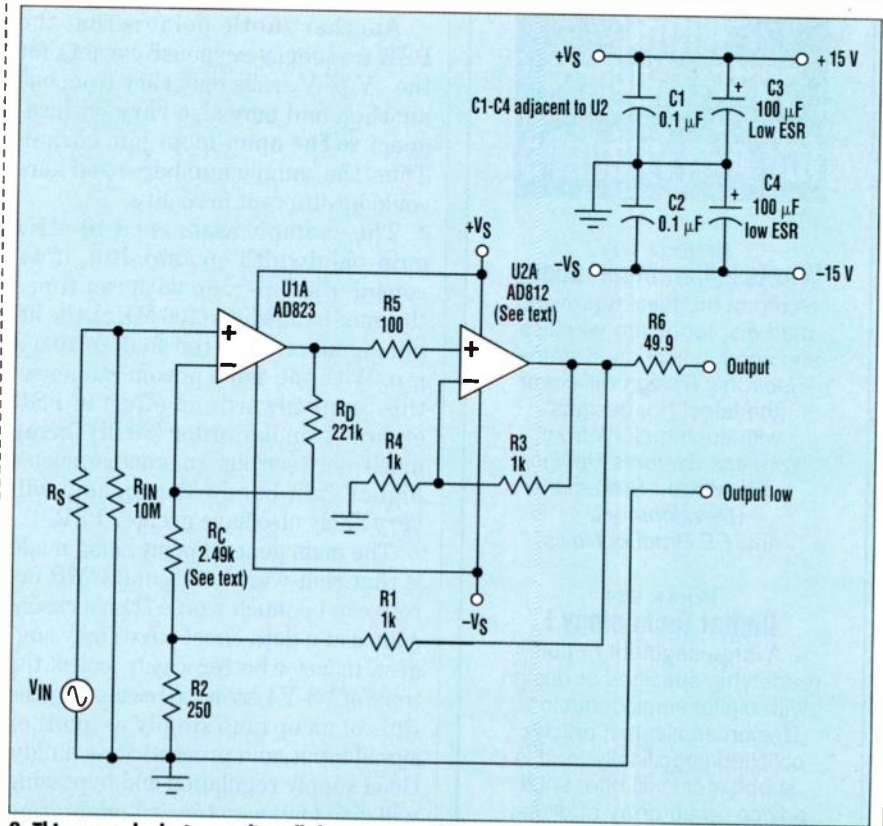
network “ $Z_S(-)$ ” can be used in the feedback path, in lieu of a direct connection.  $Z_S(-)$  is simply a dummy RC component set, to mimic the real  $Z_S(+)$  filter elements, as seen looking out from the op amp’s (+) input.<sup>2</sup> Other JFET-input op-amp circuits also can optimize  $R_S$ , as described below.

**V3-V4 power-supply-related errors:**

The two remaining errors are V3-V4, which relate  $+V_S$  and  $-V_S$  supply-rail noise to the amplifier inputs. These power supply rejection (PSR) errors are usually given in dB. Some might think these errors straightforward. But in real life, things are a bit more complex. Let’s see why.

If you study a typical op-amp data sheet, you’ll notice that there is a PSR spec for both  $+V_S$  and  $-V_S$ , as well as one for common-mode rejection (CMR). But, close inspection reveals that *these are dc specs*. Over audio frequencies, typical PSR behavior is plotted, and it degrades with frequency at 6 dB/octave. Common values are 100 dB or more of dc PSR (or CMR), dropping to 80 dB at 1 kHz. Ironically, such popular audio op amps as the 5532 and 5534 don’t provide their users PSR and CMR curves!

Also, note that PSR will often be poorer for one of the supplies, sometimes noticeably so. CMR and PSR are related—both measuring front-end response to signals common to the normal inputs, or via the rail(s) as a signal source. It is typical to specify PSR for symmetrically varying ( $\pm$ ) supply volt-



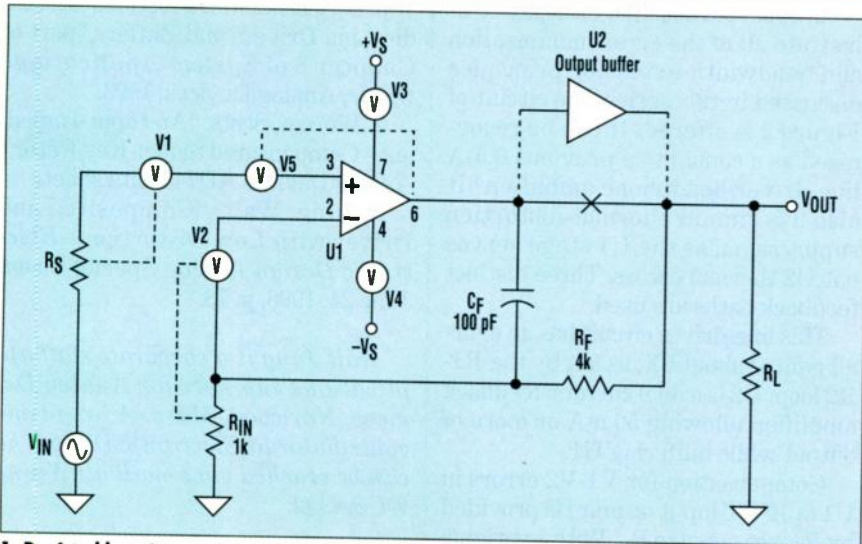
**2. This example design applies all the concepts of the audio series, in an optimized gain-of-five stage. In addition to minimizing V1-V5 errors, it also eliminates thermal distortion and crosstalk in output stage U2. Open-loop bandwidth of the first stage is set by local feedback, and is about 100 kHz.**

ages. Unfortunately, real-world power sources don’t always vary neatly. So, a realistic audio consideration would be to analyze things in terms of the *worst* PSR/CMR curve from the data sheet, and use that data at various frequen-

cies. We’ll assume an 80 dB/1 kHz PSR error in an example calculation.

An error 80dB down may sound good, until we add some mitigating factors. In Figure 1, for example, the 5X noise gain makes an 80 dB/1 kHz error about 14 dB worse, or 66 dB/1 kHz, as referred to the output. And in almost every case with conventional op amps, this still gets worse by 6 dB/octave with increasing frequency.

Putting it in perspective with an actual output signal, we’ll talk in terms of op-amp input-referred errors (since that’s where PSR errors couple). Assume 1 V p-p output at 1 kHz, and an op amp gain-bandwidth of 10 MHz. This means that to produce the 1 V p-p, the amplifier’s input signal will be 100  $\mu$ V p-p. If the supply rail sees a 1 mV p-p/1 kHz noise (for whatever reason), this noise referred at the amplifier input will be 0.1  $\mu$ V p-p. The ratio of the desired signal to the noise is 60 dB—not such a good ratio. Also, consider the possibility that CMR or PSR could be worse than 80 dB, or the power-rail noise higher.



**1. Depicted here is a noninverting op-amp gain stage with five error sources, V1-V5. Output buffering or a load-immune op amp minimizes V5. V1-V2 are minimized by matching source impedances, and V3-V4 are minimized by careful power-supply design.**

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 Penton

Another subtle point is that the PSR frequency-response corners for the  $+V_S/-V_S$  rails may vary from one another, and may also vary with respect to the open-loop-gain corner. Thus, the sample numbers used here could be different in reality.

The example assumed a 10-MHz gain-bandwidth op amp. But, if we consider an op-amp with ten times the gain-bandwidth (100 MHz), the input signal reduces ten-fold, to 10  $\mu$ V p-p. With the same power-rail noise, this tends towards an effect of PSR errors of similar order (80 dB) being much more serious. In practice, such a higher gain-bandwidth op amp will very likely also have greater PSR.

The main general point being made is that real-world PSR and CMR errors can be much worse than a casual glance at a data-sheet curve may suggest. In fact, a better way to look at the topic of V3-V4 errors is to consider the rails of an op amp simply as another signal input, and proceed accordingly. Good supply regulation and bypassing will go a long way toward minimizing and controlling these errors. In fact, it isn't unrealistic to set V3-V4 error goals referred to a working op-amp input signal of -100 dB (or better). This will generally require some careful supply regulation, since you can't always count on an op amp providing 100 dB of V3-V4 error isolation over the applicable frequency range. Current-feedback types, for example, have typical PSR and CMR of 60-70 dB.

**An optimized amplifier example:** To illustrate all of the error-minimization and bandwidth-extension principles discussed in this series, the circuit of Figure 2 is offered. It can be recognized as a cousin to a previous 0.5-A line-driver/headphone amplifier.<sup>3</sup> It also has similar thermal-distortion suppression, as the U1 stage servos out U2 thermal errors. Three distinct feedback paths are used.

This line-driver circuit has an overall gain of about 5X, as set by the R1-R2 loop. U2 is a dual current-feedback amplifier, allowing 50 mA or more of output while buffering U1.

Compensation for V1-V2 errors in U1 (a JFET-input op amp) is provided by R<sub>C</sub>, set equal to R<sub>S</sub>. With a variable R<sub>S</sub> such as a volume control, a nominal gain value is used, in this case 2-3 k $\Omega$ .

First-stage open-loop bandwidth

control is exercised in this circuit, as it applies to U1 and the local feedback loop R<sub>D</sub>-R<sub>C</sub>. For the values shown, U1's open-loop bandwidth is about 100 kHz. Were R<sub>D</sub> open, the U1 stage would function as a more-conventional (narrow bandwidth) op-amp.

Control of V3-V4 errors is not integral to this amplifier, except for the local bypassing shown. Tight regulation of  $\pm V_S$  will aid this, and is recommended for noise minimization.

#### Summary of audio op-amp series notes:

The discussions above wrap up our look into various op-amp and circuit issues which help determine high audio performance. Over the years, I have found all of these techniques useful for improving audio circuits, and hope you will also.

**Some parting comments:** This column wraps up a two-year run of "Walt's Tools and Tips," an experience I have enjoyed immensely. I hope you have as well, and I thank all those who have contributed comments.

Over the next year (or more), I will be embarking on a major new project. Unfortunately, this will preclude the time expenditure it takes to put together the kind of material I like in this column. Therefore, I am taking a column sabbatical for a period of time. I hope to return to these pages sometime soon to continue these analog-oriented talks. Happy Holidays to all.

#### References:

1. Jung, Walt, "Op-amp Device/Topology Related Distortions" of 'Audio Line Drivers and Buffers,' part of Chapter 8 of *System Applications Guide*, Analog Devices, 1993.
2. Wurcer, Scott, "An Input-Impedance Compensated Sallen-Key Filter," Analog Devices AD743 data sheet.
3. Jung, Walt, "Composite Line Driver with Low Distortion," *Electronic Design* Analog Special Issue, June 24, 1996, p. 78.

*Walt Jung is a corporate staff applications engineer for Analog Devices, Norwood, Mass. A long-time contributor to Electronic Design, he can be reached via e-mail at: Wjung@USA.net.*

Walt, it's been a real pleasure Tooling and Tipping with you. We'll miss you.—*Bob Milne, Managing Editor*

## Cost-Reducing Flat-Panel Controller Converts RGB Signals Into Digital Signals

The plummeting cost of thin-film-transistor (TFT) flat panels makes them attractive for monitors that replace the bulky CRTs now sitting on everyone's desk. However, to drive the TFT panels from the computer's RGB outputs requires an interface circuit that can accurately convert the RGB signals into the digital drive signals required by the flat panel. Just such a chip is the Bridge 120 from Paradise Electronics, a circuit that combines a triple 8-bit analog-to-digital converter, a clock/source timing generator, scaling engine, on-screen display control panel, and panel control modules. The on-screen display control block includes a character ROM and provides a choice of four background and four foreground colors as well as some special effects.

All of the B120's functions let the chip handle displays with up to SXGA resolution (1280 by 1024 pixels) and with 16.8 million colors. When used in conjunction with an 80251 or H8-type microcontroller, which controls the Bridge 120 with API calls to the operating system, the Bridge 120 can convert the analog R,G,B, HSync, and VSync signals to produce the digital control signals required by the display panel.

After sampling the input video source timing with a 200-MHz precision reference clock, the chip's source sampling clock is programmed. After that clock is programmed, the destination clock is derived, based on the ratio of the total pixels per frame of the source and destination images. Direct digital

synthesis is used for the clock generation. The triple analog-to-digital converter employs a two-stage pipelined design, and has separate gain (full scale) and offset (zero scale) adjustments for each channel. The converter also can handle the full range of RGB inputs from 0.4 to 1 V. In addition, the chip can detect the interlace timing to support even/odd field displays for TV/video playback.

To minimize the potential jitter, an internal digital-to-analog converter provides inputs for separate calibration signals on the R,G, and B channels. This cancels out the random offset and gain mismatch common among the R, G, and B channels. The same adjustment also can be used to adjust real graphics image patterns (a gray-scale image, for example), thus delivering perfect color balance among the three channels. Color brightness, contrast, black level, and white level can all be adjusted thanks to an internal filter and various on-chip line buffers. Colors are blended after interpolation to reduce artifacts, and images are gamma-corrected and dithered before they're sent to the TFT panels.

In lots of 1000 units, the B120 chip sells for \$35 each. Production quantities are immediately available.

### Paradise Electronics Inc.

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**CIRCLE 485**

**DAVE BURSUKY**

## CrossVOLT Logic Gets 1.8-V Operating Spec

The VCX family of logic circuits, already optimized for 2.5-V operation, now has a guaranteed set of performance specifications for operation at a 1.8-V nominal supply voltage (1.65 to 1.95 V). The 1.8-V VCX chips possess propagation delays of less than 10 ns and include 3.6-V overvoltage-tolerant inputs and outputs, providing designers with a simple interface as supplies change from 3.3 to 2.5 and 1.8 V. The chips also operate at low current levels—just 10- $\mu$ A  $I_{CC}$ —and offer func-

tions with 16-, 18-, and 20-bit data paths.

Some of the first available devices with the guaranteed 1.8-V specifications include the 74VCX16500, 16600, and the 162601, which are a series of bus transceiver chips. For example, the 162601 is an 18-bit universal bus transceiver that combines D-type latches and D-type flip-flops so that data can flow in transparent, latched, and clocked modes.

The chip packs 26- $\Omega$  series resistors in the outputs and deliver static drive currents of  $\pm 3$  mA at its worst-case supply level of 1.65 V. It has a propagation delay of 9.8 ns (maximum) over the 1.65-

to-1.95-V supply range. The remainder of the 1.8-V portfolio, totaling about 22 functions, will be available by the end of this year.

Devices are available in thin, shrink small-outline packages (TSSOPs). Prices start at \$2.67 apiece in 1000-unit quantities. DB

**Fairchild Semiconductor**, 333 West-ern Ave., South Portland, ME 94106; (207) 775-8100; Internet: [www.fairchildsemi.com/pf/74/](http://www.fairchildsemi.com/pf/74/).

**CIRCLE 486**

## 64-Bit RISC Core Delivers 800 MIPS And 800 MFLOPS

The SR1 64-bit RISC processor core is designed to serve as the central processing engine for applications such as digital set-top boxes, 3D gaming consoles, Internet TV systems, and network subsystems. The reason for these target areas is that it can deliver 800 Dhrystone (2.1) MIPS and 800 MFLOPS of computational throughput.

Implemented in a 0.18- $\mu$ m technology, the core will be able to operate at clock rates of up to 400 MHz yet consume just a little more than 1 W when powered by a 1.8-V supply. The core is based on a new two-way superscalar pipeline that implements the MIPS IV instruction set. However, architects extended the instruction set with 16 additional multiply and multiply-accumulate instructions, rotate instructions, debug instructions, and count leading zeros or ones operations for data normalization.

The company also plans to use the new architecture to create a family of cores that can be licensed to semiconductor and system manufacturers. Complete with 16-kbyte data and instruction caches and the floating-point unit, the core occupies an area of just 16 mm<sup>2</sup> when implemented in a 0.18- $\mu$ m process. The architecture, though, is configurable and extendable, and can be ported to different processes, ranging from 0.15 to 0.25  $\mu$ m. The core also includes a 133-MHz, 64-bit R5000-compatible bus interface. The SR1 will be available in the second quarter of 1999 as a hard macro, designed to a customer-specific process. Contact the company for licensing and fee information. DB

**SandCraft Inc.**, 3003 Bunker Hill Lane, Ste. 101, Santa Clara, CA 95054; Dirk Smits, (408) 490-3200, Internet: [www.sandcraft.com](http://www.sandcraft.com). **CIRCLE 487**

## New AWG Targets Aircraft Accelerometer Testing

The Model 9011 accelerometer power-supply system is specially designed for testing aircraft accelerometers. This system can be programmed with specific amplitude, phase, and frequency to create a wide range of sine-wave outputs. It features accurate and stable waveforms with 0.005% distortion and

phase resolution of 0.001 degree. The 9011 system combines a 9011A waveform generator and a 9011B power amplifier. With six flexible output channels, the unit may be configured in two dual channels and two single independent channels. Output frequencies range from 1.6 to 32 kHz with output voltages up to 8.0 V rms. Both in-phase and quadrature signals are available. All phases use phase-lock feedback to guarantee

precise output signal synchronization. Interchannel timing is digitally controlled to assure phase integrity and waveform fidelity. The 9011 is priced at \$56,500, with availability 90 days ARO. Dedicated software is included. JD

**Pragmatic Instruments, 7313 Carroll Rd., San Diego, CA; (619) 271-6770; fax (619) 271-9567; e-mail: awgsales@pragmatic.com; Internet: www.pragmatic.com. CIRCLE 488**

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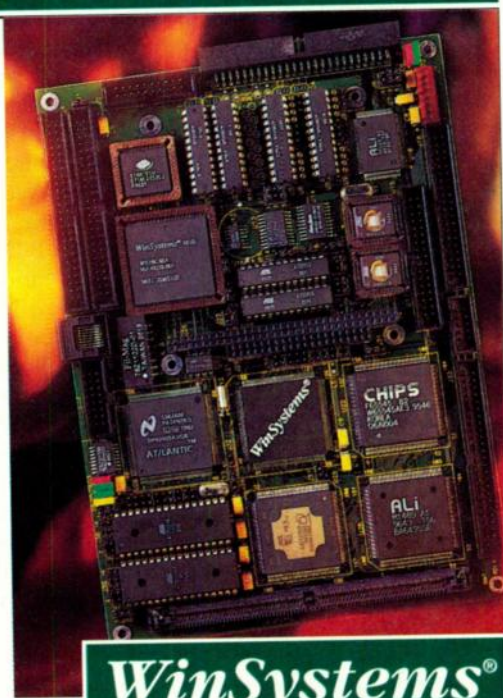


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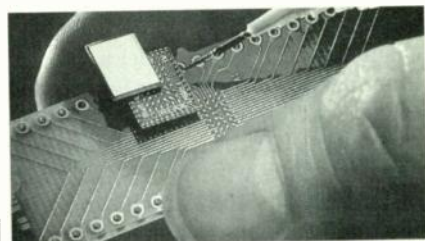


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The Signal Access Tool Kit (SAT) helps designers test micro-ball-grid-array ( $\mu$ BGA) chip-size packages (CSP). The SAT delivers a convenient signal access solution for debug/func-



tional validation during the design and prototype stage of product development. The SAT is footprint-compatible to the  $\mu$ BGA package and fits directly on the printed-circuit board landpad site, so there's no need to re-design the pc board. The  $\mu$ BGA package then is secured on top of the SAT.

The SAT connects the pc board and  $\mu$ BGA package in a two-step reflow process via solder paste or flux using standard rework equipment. Once in place, the SAT provides test point access around the perimeter of the  $\mu$ BGA package to all input/output signals. The company has modified its MicroGripper to further simplify access to  $\mu$ BGA packages by rotating the tynes 90 degrees. The MicroGripper fits into holes on the SAT and connects the signals from the  $\mu$ BGA package to test equipment. The Signal Access Tool Kit is sold in packages containing three SAT units and ten MicroGrippers. Pricing is \$595 per package. Standard orders are filled in ten days. JD

**Emulation Technology Inc., 2344 Walsh Ave., Bldg. F, Santa Clara, CA 95051-1301; (408) 982-0660; fax (408) 982-0664; www.emulation.com. CIRCLE 489**

**TEST & MEASUREMENT**

**Notebook-Based Analyzer Tackles Ultra2 SCSI**

The Model SV-3000 is a notebook-based SCSI bus analyzer. A 5-ns timing resolution makes the SV-3000 capable of analyzing Ultra2 LVD SCSI systems. The device also features a two-million-event capture buffer, which is needed for tackling Fast-40 transfer rates, according to the company. The SV-3000 connects to a notebook PC through a PCMCIA PC Card interface that's included with the package. Also included is Release 3 of SCSI-View for Windows 95 software. This release consists of a DOS protected-mode application and a 32-bit VxD driver that accesses the analyzer hardware. This combination uses Windows95 plug-and-play services to allocate I/O and interrupt resources to the VxD. The current release of the software includes features for the SV-3000, such as recirculate capture and phase filter. Price of the SV-3000 is \$7995. An SV-3000/P model is integrated with an IBM 600 ThinkPad for \$11,995. JD

**Verisys Inc., 335-H Spreckels Dr., Aptos, CA 95003; (831) 662-7900; fax (831) 662-7910; www.verisys.com.**

**CIRCLE 490**

**Facsimile Tester Offers Remote Monitoring Via A Modem**

The FaxProbe Kit, a PC-based analysis tool, can remotely originate, answer, or monitor a facsimile transmission via modem for fast and efficient diagnosis. The kit consists of software (FaxProbe) and hardware (FaxTrap). FaxProbe helps locate errors by graphically representing transmissions in colors—by results or by modulation. It offers easy replication of configurations and transmission pages when multiple FaxTrap devices are involved, and produces a results database in Microsoft Access format. Featuring a client/server architecture, FaxProbe can be used on a network, attached locally, or connected via a phone line. Users can remotely log onto the fax test hardware via a modem from anywhere in the world. This offers the ability to troubleshoot remote problems from a local site. The FaxProbe Kit is available at a cost of \$6955. JD

**Genoa Technology Inc., 5401 Tech Circle, Moorpark, CA 93021; (805) 531-9030; fax (805) 531-9045; www.gentech.com. CIRCLE 491**

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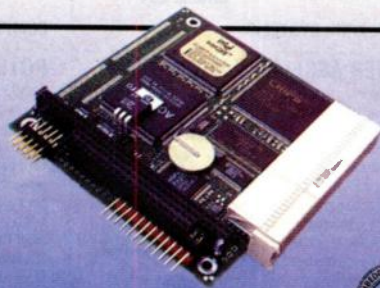
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# ELECTRONIC DESIGN CATALOG/LITERATURE REVIEW

## GIANT NEW SWITCH CATALOG

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APEM

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THARO SYSTEMS

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OCTAGON SYSTEMS

## 1999 Measurement & Automation Catalogue

1999 catalogue features hundreds of software & hardware products for your computer-based measurement and automation applications. Products include additions to our modular CompactPCI (PXI) platform, new computer-based instruments, & latest versions of our instrumentation and automation software such as LabVIEW. (512) 794-0100; (800) 433-3488 (US and Canada); Fax: (512) 683-8411; E-mail: [info@natinst.com](mailto:info@natinst.com); [www.natinst.com](http://www.natinst.com)



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NATIONAL INSTRUMENTS

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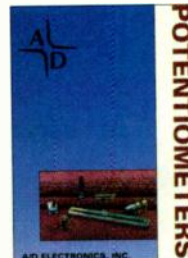


CIRCLE 255

COMPUTER DYNAMICS

## POTENTIOMETERS

A/D Electronics free Potentiometers catalog features a variety of different configurations. This 68 page catalog offers rotary, slide, cermet, and wire wound style potentiometers along with information on rotary encoders. Design engineer can obtain complete specifications, dimensional drawings and evaluation samples upon request. Included are rotary styles in body diameters ranging from 9mm-24mm. 253-851-8005; fax: (253) 858-9869; [www.adelectronics.com](http://www.adelectronics.com) A/D ELECTRONICS



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CIRCLE 261

## NEW XILINX AppLINX CD-ROM

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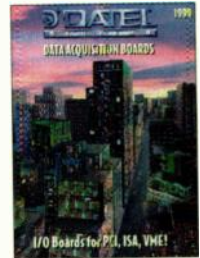


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XILINX

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DATEL SYSTEMS

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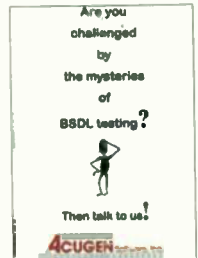


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VICOR

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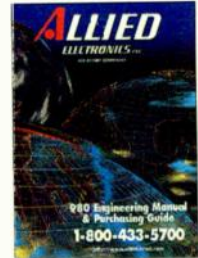


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## ELECTRONICS ENGINEERING MANUAL

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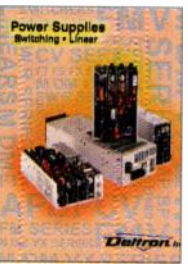


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CIRCUIT COMPONENTS

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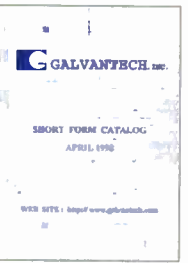


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DELTRON

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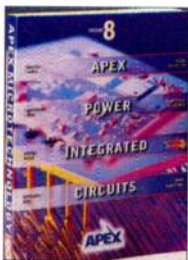


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AMERICAN HIGH VOLTAGE

## POWER INTEGRATED CIRCUITS

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APEX

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CONDOR

## INTERCONNECT SOLUTIONS

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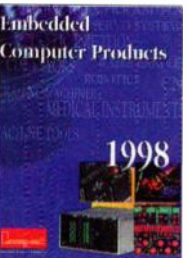


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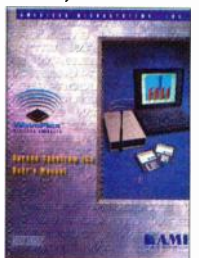


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GESPAC INC.

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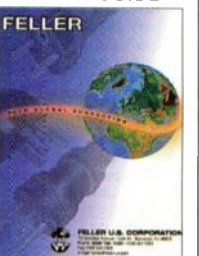


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DATA I/O

## NEW POWER CORD REFERENCE GUIDE

This all new 48-page catalog portrays Feller's complete line of high quality domestic, hospital grade and international power cords. It provides detailed specifications illustrations, application, features and benefits. Many new products and services were added, including in-house cord assemblies, extensive packaging services and custom molding capabilities. 800-736-7333; Fax: 732-247-7279; E-mail: sales@feller-us.com; http://www.feller-at.com

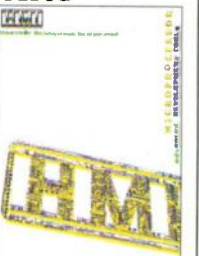


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# ELECTRONIC DESIGN CATALOG/LITERATURE REVIEW

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## INNOVATIVE INTEGRATION

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CIRCLE 281

## ITT POMONA ELECTRONICS

## MICROPAK® INSTRUMENT ENCLOSURES

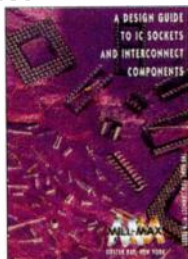
Lansing Instrument Corp. offers enclosures for smaller, free standing electronic instruments used in hand-held or desktop applications. Three body styles and a choice of end cap configurations are available, along with several finishes and colors. Literature includes information for stock and custom choices, and a no-risk offer at a special price. Contact Rich Kippola at Lansing Instrument Corp., (800) 847-3535. LANSING INSTRUMENT CORP.



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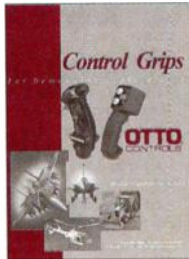


CIRCLE 287

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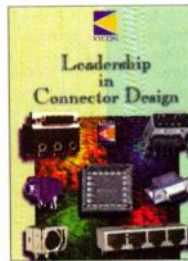


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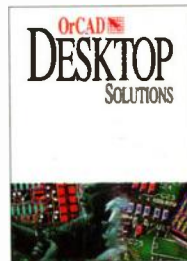


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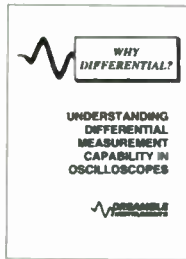
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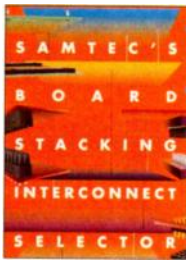


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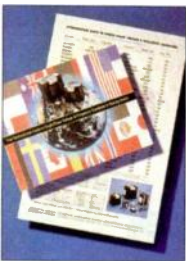


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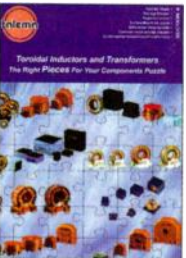


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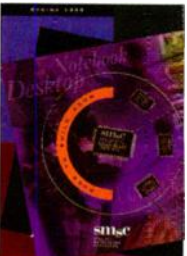


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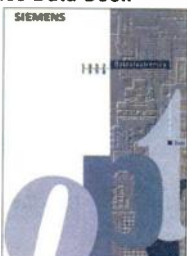


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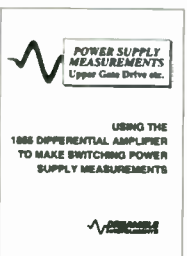


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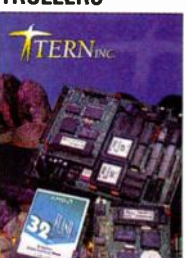


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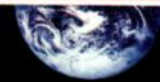
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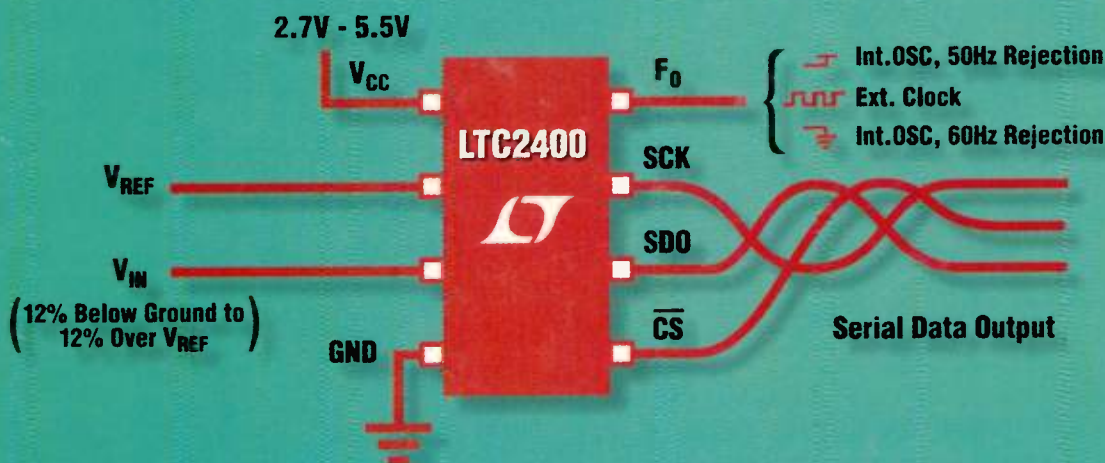
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